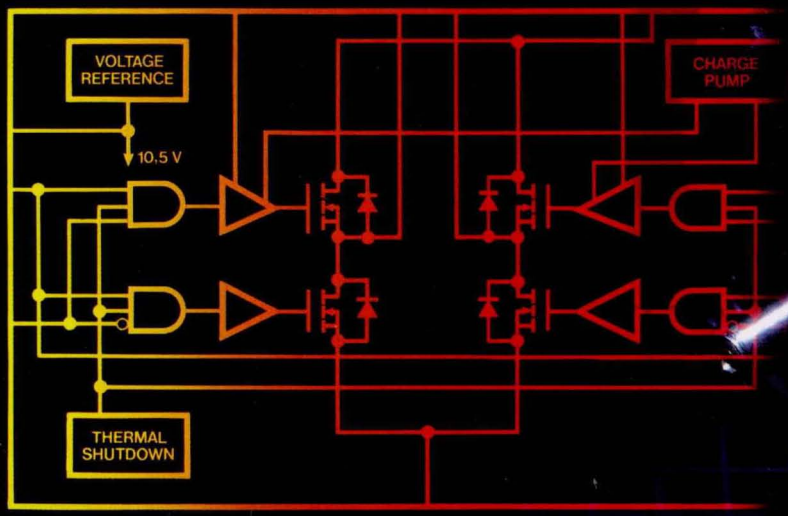
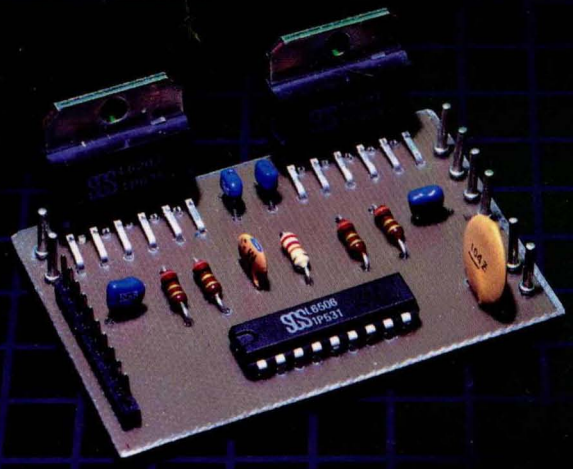
SGS

SGS®

Technology and Service

MOTION CONTROL APPLICATION MANUAL





MOTION CONTROL APPLICATION MANUAL

Motion Control Application Manual

January, 1987

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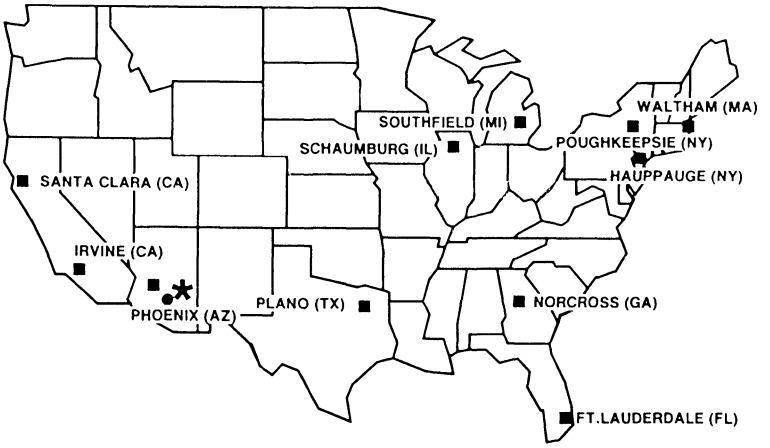
SGS IN NORTH AMERICA



SGS IN ASIA/PACIFIC

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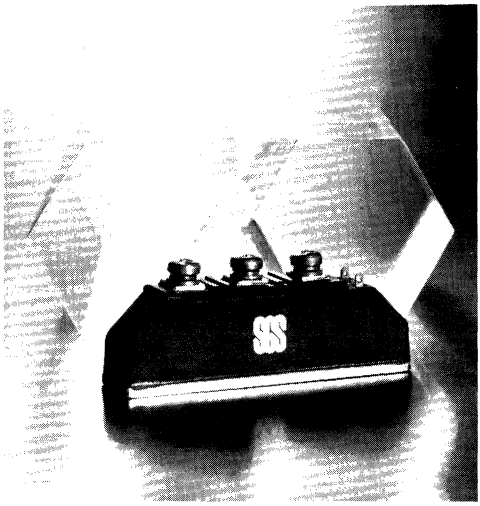
is used for the VB010 self protected switch which features a 400V Power Darlington capable of 10A output current with built-in protection circuits.

SGS has also kept ahead in POWER MOS transistors by exploiting high density cell structures. The SGSP322HD has a reduced chip area but equal overall performance to the original SGSP322 so offers a cost reduction for the user.



TO-240 — The unique SGS combination of advanced chip technology in a truly "user friendly" package, gives the solution to meet all high power system requirements.

Moving up in power, the SGS150MA010D1 isolated TRANSPACK module containing SGS POWER MOS transistors is designed for high switching speed DC motor control applications. On resistance is as low as 0.009Ω and the easy drive and rugged DMOS technology make this module ideal for high power applications.

These advances do not stop with silicon technology, SGS's established expertise in packaging has led to the recent introduction of a fully isolated package for power transistors. Used in place of the SOT-93 (TO-218), the ISOWATT218™ provides guaranteed isolation of 4kV DC and compliance with VDE specifications for creepage distance and clearance in electrical equipment.

All of these products are included in this book, along with the application information you'll need to use them. The Motion Control Application Manual also contains a selection of SGS' innovative power supply products which will be useful in your system.

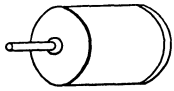
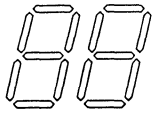
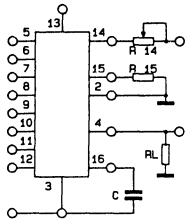
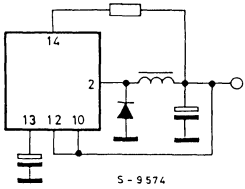
Dependable Delivery

Advanced technology and innovation are just two of the reasons for SGS' remarkable growth performance. The third is manufacturing science — the ability to produce advanced products in high volumes, dependably, and with competitive quality & reliability. Just for bipolar linear and mixed bipolar/MOS ICs SGS has four 5" wafer fabs — in France, Italy and Singapore. Another two state-of-the-art 5" wafer fabs are dedicated to power transistor production. In addition, the company has highly-automated assembly facilities in Italy, France, Malta, Malaysia and Singapore.

SGS also has local design centers in all major semiconductor markets — USA, England, France, West Germany, Singapore and Italy — to speed the development of new products to satisfy the special needs of your application. And a worldwide network of sales offices and distributors means that SGS technology is never far away.

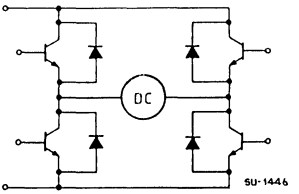
New diffusion facilities give SGS the advantage in Service, Quality and cost. State-of-the-art 5" wafer fabs are used for both linear ICs and power transistors.

PRODUCT SELECTOR (Integrated Circuits)

Applications	Type and Functions
DC MOTORS 	**L290** – Tachometer Converter **L291** – 5 Bit D/A Converter and Position Amplifier **L292** – Switch-Mode Driver for DC Motors **L149** – 4A Linear Driver **L165** – 3A Power Operational Amplifier **L272/M** – Dual Power Operational Amplifiers **L2720/2** – Low Drop Dual Power Operational Amplifiers **L293/E** – Push-Pull Four Channel Drivers **L293C** – Push-Pull Four Channel/Dual H-Bridge Driver **L293D** – Push-Pull Four Channel Driver With Diodes **L298N** – Dual Full-Bridge Driver **L9350** – Low Saturation Driver **TDA7272** – Full Bridge DC Motor Regulator **TDA8115** – Dual Motor Driver
DISPLAYS 	**M5450/1** – Led Display Drivers **M5480/81/82** – Led Display Drivers **L3654S** – Printer Solenoid Driver **L601/2/3/4** – Darlington Arrays **ULN2001A/2A/3A/4A** – Seven Darlington Arrays **ULQ2001R/2R/3R/4R** – Seven Darlington Arrays
SPECIAL FUNCTIONS 	**AM26LS31** – Quad High Speed Differential Line Driver **AM26LS32/3** – RS422 and RS423 Quad Differential Line Receivers **MC1488** – RS232C Quad Line Driver **MC1489/A** – Quad Line Receiver **DAC0806/7/8** – 8 Bit D/A Converters **AM6012/A** – 12 Bit High Speed Multypling D/A Converters **L6570A/B** – 2-Channel Floppy Disk Read/Write Circuits
POWER SUPPLIES 	**L200** – Adjustable Voltage and Current Regulator **L296/P** – High Current Switching Regulators **L387A** – Very Low Drop 5V Regulator **L4901/2/3/4** – Dual 5V Regulators with Reset **L4920/1** – Very Low Drop Adjustable Regulators **L4941** – Very Low Drop 1A Regulator **L4960/2** – Power Switching Regulators **SG1524/1525/1527/2524/2525/2527/3524/3525/3527** – Regulating Pulse width modulator **TDA4601** – Switch-Mode Power Supply Controller **TDA8130/2** – Current Mode PWM Controllers **TL7700 series** – Supply Voltage Supervisors **UC1840/2840/3840** – Programmable, Off-Line, PWM Controllers **UC1842/3/4/5 - UC2842/3/4/5 - UC3842/3/4/5** – Current Mode PWM Controllers

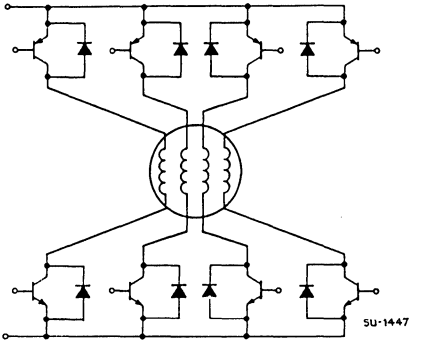
PRODUCT SELECTOR (Transistors, Diodes and TO-240 Modules)

DC MOTORS



220V ~		96V		48V		28V	
Type	Nom. KVA	Type	Nom. KVA	Type	Nom. KVA	Type	Rating, A
SGS50DA045D	15	SGS100DA025D	10	SGS150MA010D1	3.5	SGSP592/492	25.0
SGS40TA045D	12	BUR51	3.0	BUR50	2.0	SGSP482/382	15.0
SGS30MA050D1	4.0	SGSP577/477	1.0	SGSP571/471	0.7	SGSP422/322	6.5
SGSP574/474	1.8	SGSP567/467	0.5	SGSP561/461	0.4	SGSP358	4.0
SGSP579/479	1.5	2N7056	1.0				
2N7059	1.5						
SGSD310	4.0						
BUX98A	5.0						
BUX48A	2.5						
BUW42	2.5						
BUW32	1.5						
BUW22	1.0						

STEPPER MOTORS



200V		96V		48V		28V	
Type	Config. Rating, A	Type	Config. Rating, A	Type	Config. Rating, A	Type	Config. Rating, A
BUR20	25.0	BUR50	35.0	SGSD100	10.0	BDW93	5.0
BUV21	12.0	BUV20	25.0	SGSD200	-10.0	BDW94	-5.0
BUV22	10.0	BUX10P	10.0	BDW93C	5.0	SGSP386	25.0
BUX11	6.0	BDX53F	2.0	BDW94C	-5.0	SGSP592/492	25.0
SGSP573/473	13.0	BDX54F	-2.0	BDX53C	3.0	SGSP482/382	15.0
SGSP463/363	6.5	SGSP577/477	13.0	BDX54C	-3.0	SGSP422/322	6.5
SGSP516/316	3.5	SGSP467/367	6.5	SGS132	4.0	SGSP358	3.0
		SGSP517/317	3.5	SGS137	-4.0		
				SGSP572/472	19.0		
				SGSP562/362	10.0		
				SGSP512/312	4.5		
				SGSP352	3.0		

ALPHANUMERICAL INDEX

ALPHANUMERICAL INDEX (continued)

ALPHANUMERICAL INDEX (continued)

ALPHANUMERICAL INDEX (continued)

APPLICATION NOTES

APPLICATION NOTES INDEX

NEW DEVELOPMENTS IN INTELLIGENT POWER TECHNOLOGY

Recent developments in power IC technology greatly expand the capabilities of integrated circuits combining control circuits and high power drive stages. This note describes the new power processes, new packages and the latest generation of power ICs.

While chips integrating both signal and power elements have been with us for several years, recent developments have greatly expanded the capabilities of these technologies. With the latest processes designers can integrate many circuits that were previously uneconomic or simply impossible. Moreover, the enlarged horizons of intelligent power technology—and packaging—are prompting new trends in the partitioning of systems.

Not only are intelligent power ICs becoming more common, they are also becoming more intelligent, to the point where designers can aim to integrate a complete power subsystem. Moreover, the current and voltage capabilities of these technologies have increased dramatically, enlarging the field of applications.

Since system designers are often responsible for partitioning electronic systems and specifying new devices it is important for them to understand the capabilities of the latest technologies. This is now more true than ever, both because IC technology has advanced so rapidly and because the latest generation of power ICs have a much greater 'system' content.

THE NEW TECHNOLOGIES

Intelligent power technologies have evolved from two earlier species: linear IC technology and discrete transistor technology.

Processes of the first type are enhancements of the basic planar IC structure where all of the connections are on the top surface of the chip. In contrast, those intelligent power technologies that have been developed from discrete transistor processes have a collector, or drain, contact on the lower surface of the die. A fundamental consequence of this structural difference is that with processes of the first type it is possible to integrate any number of isolated power transistors and interconnect them in any configuration. SGS calls these Multipower processes.

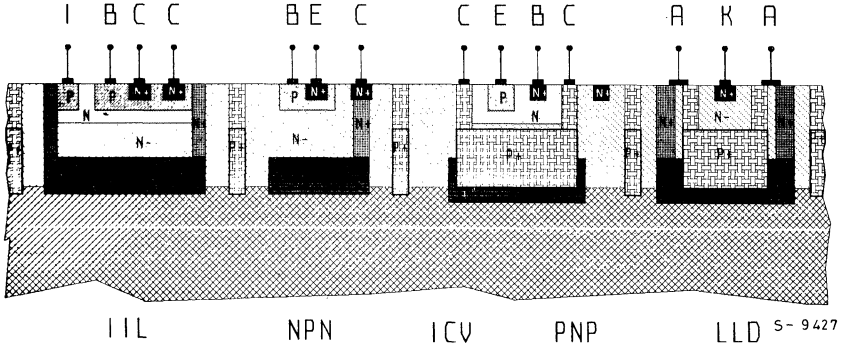
Where a bottom contact is used it is only possible to integrate a single power transistor, or several with common collectors (or drains), therefore configurations such as the H-bridge cannot be integrated but higher current and voltage capability of several hundred volts is possible. SGS has named this type of process VIPower™ (Vertical Intelligent Power). Both technologies can be further subdivided into those which are pure bipolar and mixed technologies containing a mixture of bipolar and MOS structures. In both fields significant progress has been made recently.

PURE BIPOLAR MULTIPOWER PROCESSES

Just how far bipolar technology has advanced is illustrated by SGS' new Multipower-S^2P^2 and Multipower-HDS^2P^2 processes.

Multipower-S^2P^2 (figure 1) is a 60V process that integrates bipolar linear, IIL logic, NPN and PNP power transistors and a new low leakage diode structure.

Fig. 1 - Multipower-S^2P^2, a 60V bipolar process, combines linear, IIL logic, ICV PNP power transistors and low leakage diodes.



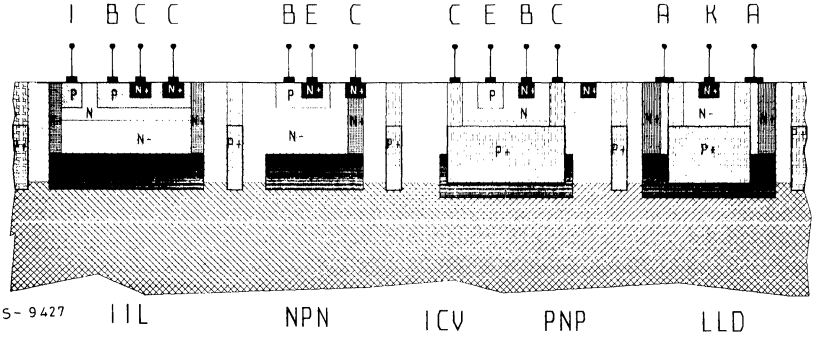
Multipower-HDS^{2}P^3 (figure 4) is a similar pure bipolar process. Like Multipower-S^{2}P^2 it integrates linear, IIL, LLD and ICV PNP structures. In addition it also offers ECL logic.

But the most important characteristic of this process is high density. Dimensioned for 20V capability, it is aimed at low voltage applications where more complex signal processing circuits are needed —up to 270 IIL gates can be shoehorned into one square millimeter of silicon.

Multipower-HDS^{2}P^2 is also characterized by an exceptionally high current density: 6A/mm^2 for NPN transistors; 2A/mm^2 for PNP (at V_{sat}= 1V and H_{fe}= 10).

This process has been applied to produce a custom stepper motor control/drive chip, where the high density of the process allows translator and chopper circuits to be integrated economically on the power drive chip. It is also used for a new 1.5A voltage regulator, the L4940, where the ICV PNP provides very low voltage drop and low quiescent current.

Fig. 4 - Multipower HDS^{2}P^2 is a 20V process characterized by very high density in the signal part (270 IIL gates/mm^2) and exceptionally high current density.



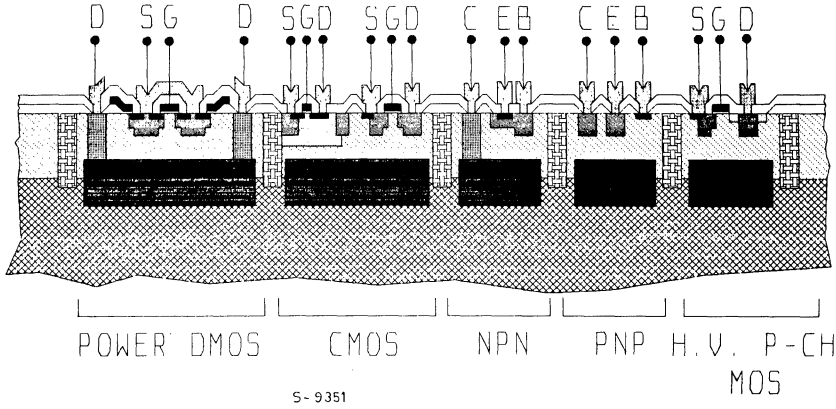
MIXED MULTIPOWER TECHNOLOGY

Another area where remarkable progress has been made is in mixed bipolar/MOS technology. Though several mixed technologies of the 'vertical' type are available, a much more significant development is SGS' Multipower-BCD process (figure 5), which combines linear, CMOS logic and DMOS power transistors without placing any limit on the number and connection of the power devices.

Thanks to the DMOS power transistors this process allows efficiencies above 95% and switching frequencies up to 500kHz. In addition, there are no secondary breakdown limitations, paralleling of devices is simpler and there is an intrinsic 'fast' recirculation diode in the power DMOS structure which is adequate for most applications.

For intelligent power devices the very high efficiency of power DMOS is an important advantage. The power output of a chip is limited by the maximum dissipation allowed in the package. By reducing dissipation in the chip it is possible to put power ICs in low cost packages with modest power handling capability. Alternatively, packaged in existing high power packages, DMOS chips can deliver hitherto unreachable power levels.

Fig. 5 - A mixed technology, Multipower-BCD integrates linear, CMOS logic and power DMOS devices on the same chip. Unlike other mixed technologies it places no limit on the number or connection of the power transistors.



VERTICAL PROCESSES

While the "Multipower" processes are more versatile SGS is also developing bipolar and mixed vertical technologies, called VIPower-M1 and VIPower-M2.

VIPower-M1 (figure 8) combines 400V NPN power transistors and bipolar low voltage (up to 30V V_{ceo}) drive circuits, while VIPower-M2 (figure 9) will offer 80V DMOS power transistors and mixed CMOS/bipolar drive circuits.

Though these processes cannot be used for devices with bridge and half-bridge output stages, they offer higher voltage capability and VIPower-M2 features a lower ON resistance than Multipower-BCD.

VIPower-M2 is suitable for applications such as high current high side drivers and DC-DC converters while VIPower-M1 is suitable for applications like high voltage solenoid drivers, motor drives and off-line power supplies.

Fig. 8 - VIPower-M1 technology integrates 400V NPN power transistors and 30V drive circuitry.

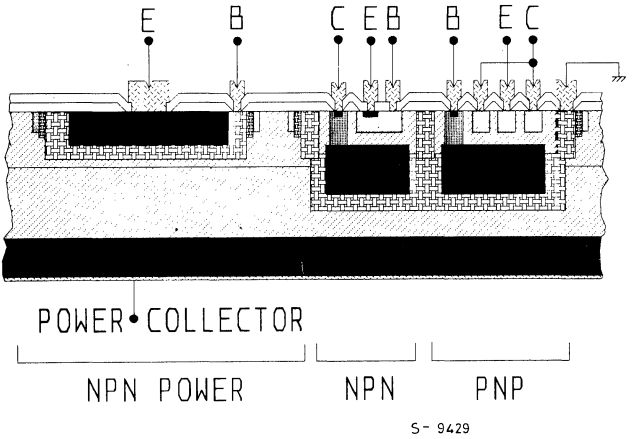
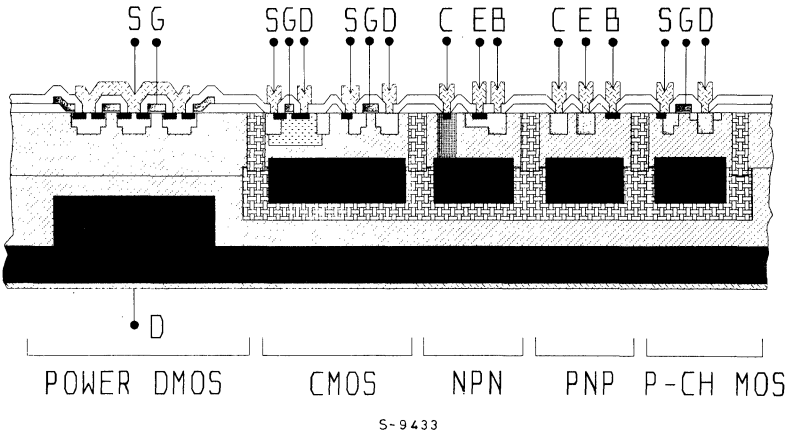


Fig. 9 - Another 'vertical' power process, VIPower-M2 combines 80V DMOS power transistors and mixed CMOS/bipolar drive circuits.



The first products proposed in VIPower-M1 are 400V 5A to 10A NPN darlington switches (figure 10) with direct logic compatible drive. In addition on chip thermal, overcurrent and overvoltage sensing can shutdown the power switch and provide a diagnostic output to inform the system microprocessor of the overload condition.

Fig. 11 - The leadframe of a plastic chip carrier can be modified to reduce thermal resistance. This '33+11' lead configuration allows power dissipation up to 2W

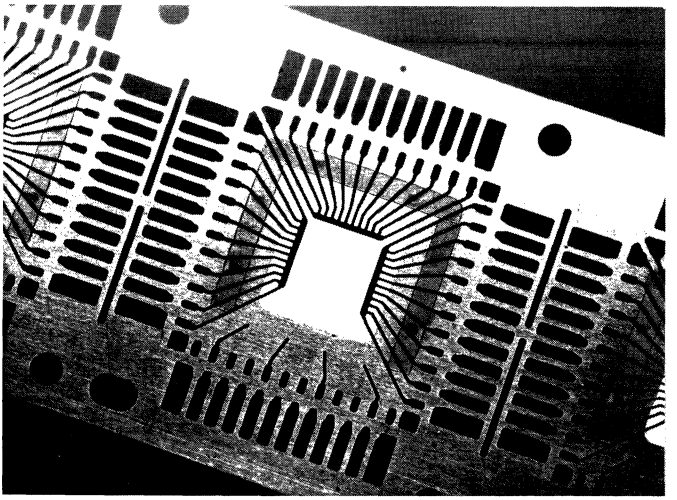
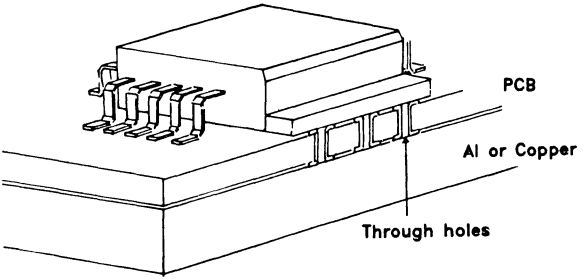


Fig. 12 - For power dissipation above 2W new surface mounting packages are being developed. This type, compatible with SO-package handling equipment, has a thermal resistance of about 5° C/W.



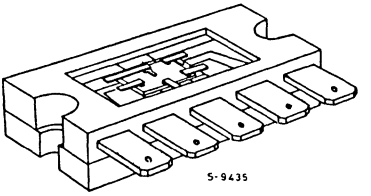
S-9434

In view of this trend there is now considerable interest in high conductivity substrates and the various alternatives, such as a plastic board bonded to an aluminum or copper sheet. Plated-through holes in the PCB reduce the thermal resistance between the package and the metal sheet.

Another development area is the inclusion of a copper heat spreader on the under-side of plastic chip carriers. These power chip carriers will, like many new packages, be pre-molded types, which eliminates stress on the die caused by polymerization shrinkage of the molding resin.

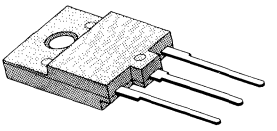
New packaging concepts are being studied for chips like the L9480 which need no external components. Since there is no need to mount such devices on a substrate they will probably be assembled in packages designed to be bolted to the load (figure 13) and equipped with 'Faston'-type connectors.

Fig. 13 - New packaging concepts are being studied for 'silicon-only' circuits where there is no point in mounting the device on a conventional substrate because there are no other components needed.



S-9435

Fig. 14 - In the ISOWATT-218 package the copper frame is completely surrounded by molding resin to isolate the device from the heatsink.



A HIGH EFFICIENCY, MIXED-TECHNOLOGY MOTOR DRIVER

A new mixed technology called Multipower-BCD allows the integration of bipolar linear circuits, CMOS logic and DMOS power transistors on the same chip. This note describes a H-bridge motor driver IC realized with this technology.

The miniaturization and integration of complex systems and subsystems has led in recent years to the implementation of monolithic circuits integrating logic functions and power sections.

For these applications SGS has developed a new technology called Multipower BCD which allows the integration on the same chip of isolated Power DMOS elements, bipolar transistors and C-MOS logic.

Thanks to high efficiency, fast switching speed and the absence of secondary breakdown, this technology is particularly suitable for fast, high current solenoid drivers and high frequency switching motor control. The free-wheeling diode intrinsic to the DMOS structure (necessary if the device drives an inductive load) and the great flexibility available in the choice of the logic and driving section components allow the complete integration of power actuators without further expense in silicon area-and a compact implementation of complex signal functions.

This technology has been applied to produce a switching power driver – the L6202/3 – capable of delivering 4A per phase, which is suitable for speed and position control in D.C. motor applications.

Fig. 1 - A schematic cross section of Bipolar, C-MOS, DMOS structures (BCD)

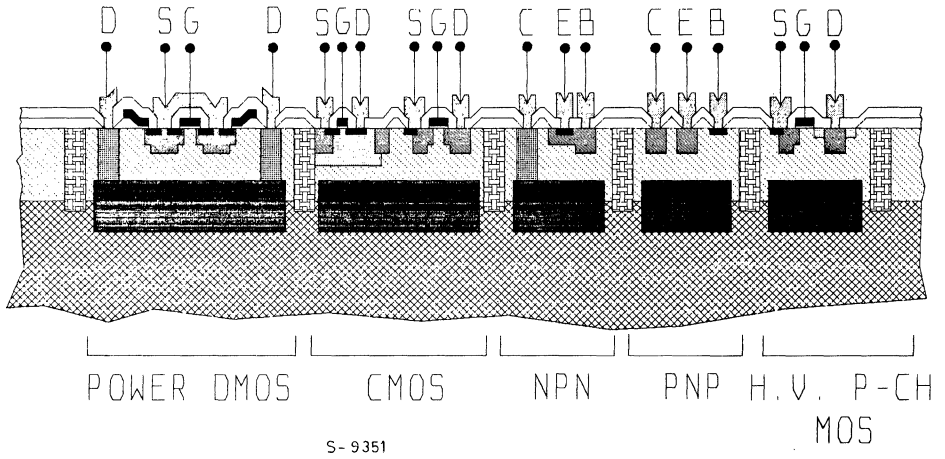
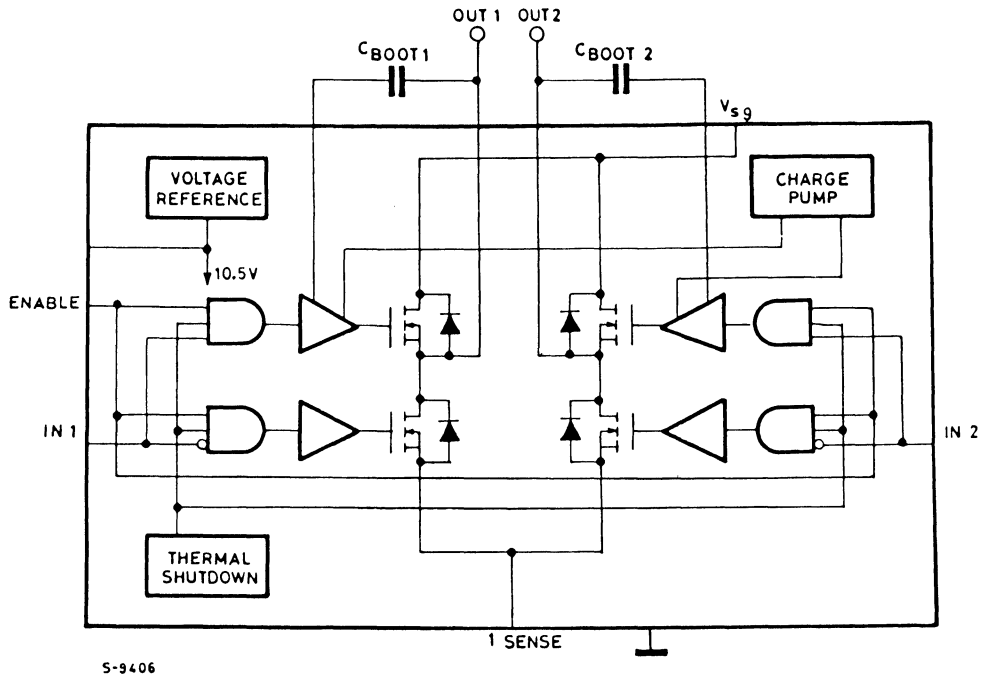


Fig. 3 - L6202-6203 BLOCK DIAGRAM



The integrated circuit has 3 Inputs: Enable, Input 1, Input 2. When Enable is "low" all power devices are off; when it is "high" their conduction state is controlled by the logic signals Input 1 and Input 2 that drive independently a single branch of the full bridge. When Input 1 (Input 2) is "high" DMOS 1 (DMOS 1') is "on" and DMOS 2 (DMOS 2') is "off", when is "low" DMOS 1 (DMOS 1') is "off" and DMOS 2 (DMOS 2') is "on".

A thermal protection circuit has been included that will disable the device if the junction temperature reaches 150°C. When the thermal protection is removed the device restarts under the control of the Input and Enable signals.

ON-OFF SYNCHRONIZATION CIRCUIT

ON-OFF synchronization of the power devices located on the same leg of the bridge must prevent simultaneous conduction, with obvious advantages in terms of power dissipation and of spurious signals on the ground and on sensing resistors.

Because of the very short turn-on, turn-off times characteristic of POWER MOS devices a dead time (time in which all power transistors are "off") of 40 ns is sufficient to prevent rail-to rail shorts. The circuit that provides this time interval is shown in fig. 4 with the voltage waveforms that explain how it works. Let us suppose Enable = "high". Because of the delay times introduced by INV1 and INV2, V2 and V3 are two waveforms contained one in the other and of polarity suitable to assure that the turn-on of a power transistor happens only after the turn-off of the other. The gate voltages V5 and V6 of DM1 and DM2 are represented in fig. 5. In fig. 3 we can see also the modality of operation of the Enable signal, charge pump and bootstrap circuits.

Concerning POWER MOS driving, it must be noted that it is necessary to assure to all DMOS N-channel a gate-source voltage of about 10V to guarantee full conduction of the POWER MOS itself. While there are no particular problems for driving the lower POWER MOS device (its terminals is referred to ground) for the upper one it is necessary to provide a gate voltage higher than the positive supply because it has the drain connected to the positive supply itself.

This is obtained using a system that combines a charge pump circuit, that assures DC operation, with a boostrapping technique suitable to provide high switching requencies. The circuit that satisfies to all these requirements is represented in the schematic diagram of fig. 6.

Fig. 6 - Schematic representation of charge PUMP and BOOSTRAP circuit used to drive the gate of the upper DMOS device

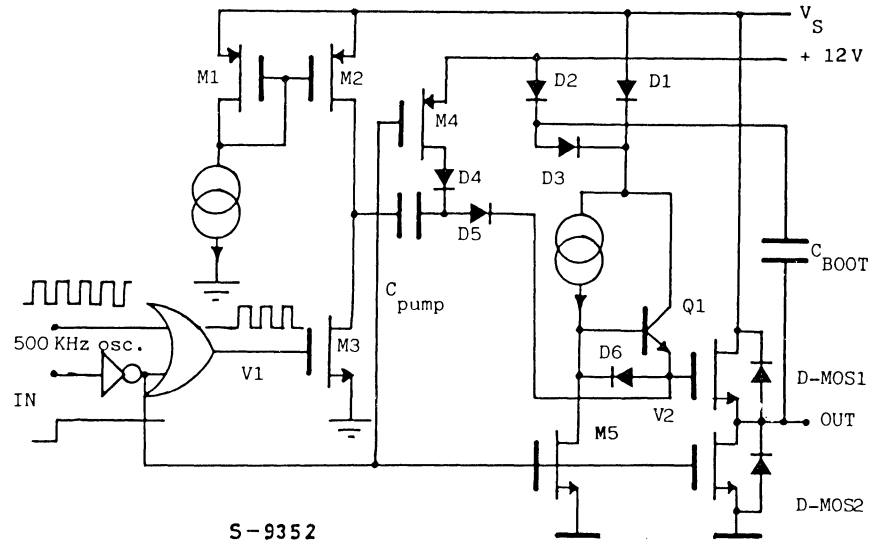


Fig. 7 - Charge PUMP abilitation signal and gate voltage of DMOS upper device

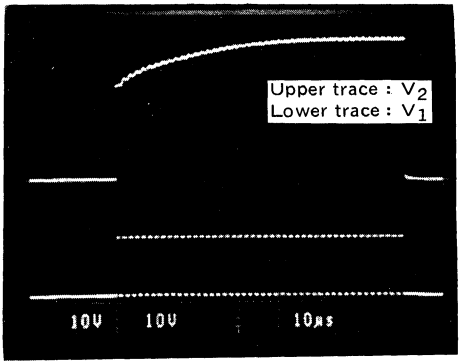
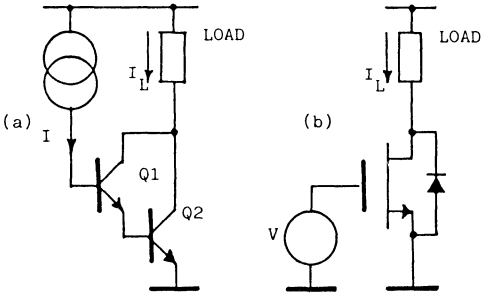


Fig. 8 - Darlington Bipolar and DMOS power stages



Neglecting the power dissipation in the driving section, in static conditions, the total dissipation of the two stages when they are "on" is in the case (a):

$$P_{d(a)} = (V_{CESAT1} + V_{BE2}) \times I_L$$

and in the case (b):

$$P_{d(b)} = R_{DS(ON)} \times I_L^2$$

where I_L is the load current.

Because the saturation loss of a power DMOS transistor can be reduced by increasing the silicon area it is possible to satisfy the condition

$$R_{DS-ON} \times I_L < (V_{CESAT1} + V_{BE2})$$

and then to obtain lower dissipation.

Concerning to the driving section, an other essential difference must be emphaisised.

While in case (a) during the time in which the power is "ON" it is necessary to supply a current for maintaining Q1 saturated, in the case (b) power is dissipated only during the commutation of the gate voltage.

About AC operation, it must be noted that the greatest advantage, always in terms of power dissipation, is due to the inherently fast turn-on, turn-off times of power MOS devices. In fact, if we suppose that the load is of inductive type and that the current waveform is triangular on the voltage commutation of the output, the total power dissipation is:

$$P_d = V_S \, I_L \, T_{COM.} \, f_{SWITCH}$$

STEPPER MOTOR DRIVING

Dedicated integrated circuits have dramatically simplified stepper motor driving. To apply these ICs designers need little specific knowledge of motor driving techniques, but an understanding of the basics will help in finding the best solution. This note explains the basics of stepper motor driving and describes the drive techniques used today.

From a circuit designer's point of view stepper motors can be divided into two basic types: unipolar and bipolar.

A stepper motor moves one step when the direction of current flow in the field coil(s) changes, reversing the magnetic field of the stator poles. The difference between unipolar and bipolar motors lies in the may that this reversal is achieved (Figure 1):

Fig. 1a - BIPOLAR — with one field coil and two chargeover switches that are switched in the opposite direction.

Fig. 1b - UNIPOLAR — with two separate field coils and are chargeover switch.

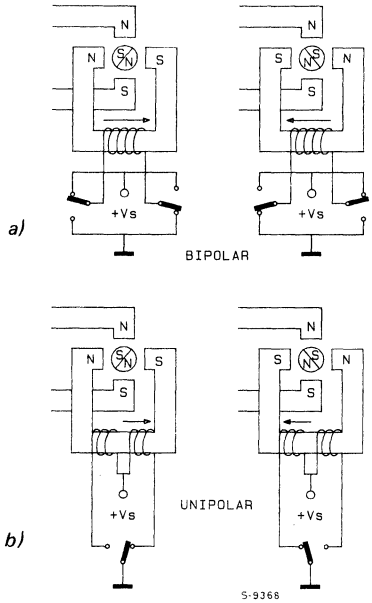
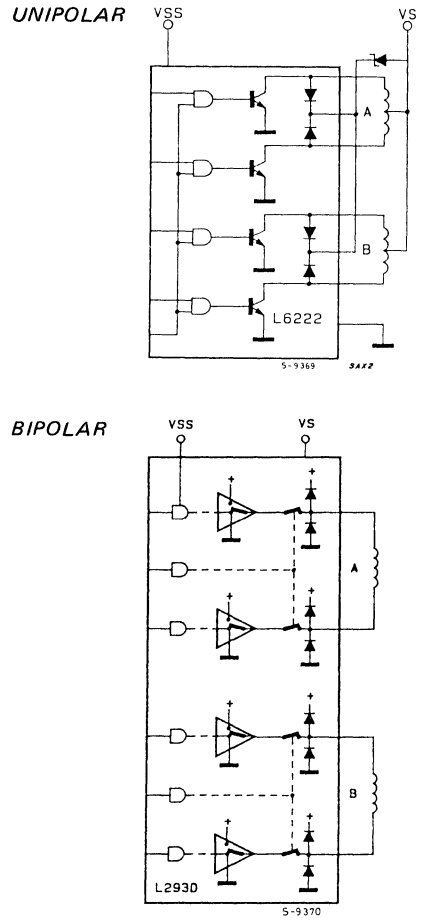


Fig. 2 - ICs for unipolar and bipolar driving



quency, the current no longer reaches its saturating value because of the limited change time; the power and also the torque diminish clearly at increasing number of revolutions (Fig. 5).

MORE TORQUE AT A HIGHER NUMBER OF REVOLUTIONS

Higher torque at faster speeds are possible if a current generator as shown in Fig. 4b is used. In this application the supply voltage is chosen as high possible to increase the current's rate of change. The current generator itself limits only the phase current and becomes active only the moment in which the coil current has reached its set nominal value. Up to this value the current generator is in saturation and the supply voltage is applied directly to the winding.

Fig. 6, shows that the rate of the current increase is now much higher than in Figure 5. Consequently at higher step rates the desired current can be maintained in the winding for a longer time. The torque decrease starts only at much higher speeds.

Fig. 7 shows the relation between torque and speed in the normal graphic scheme, typical for the stepper motor. It is obvious that the power increases in the upper torque range where it is normally needed, as the load to be driven draws most energy from the motor in this range.

Fig. 6 - With a step current slew it is not a problem to obtain, even at high step frequencies sufficient current in windings.

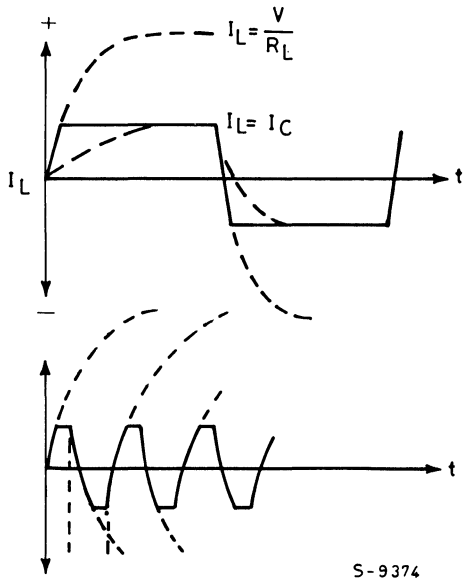
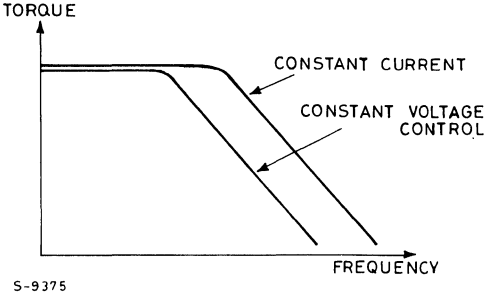


Fig. 7 - Constant current control of the stepper motor means more torque at high frequency.



EFFICIENCY - THE DECISIVE FACTOR

The current generator combined with the high supply voltage guarantees that the rate of change of the current in the coil is sufficiently high.

At the static condition or at low numbers of revolutions, however, this means that the power loss in the current generator dramatically increases, although the motor does not deliver any more energy in this range; the efficiency factor is extremely bad.

Help comes from a switched current regulation using the switch-transformer principle, as shown in Fig. 8. The phase winding is switched to the supply voltage until the current, detected across R_S, reaches the desired nominal value. At that moment the switch, formerly connected to $+V_s$, changes position and shorts out the winding. In this way the current is stored, but it decays slowly because of inner winding losses. The discharge time of the current is determined during this phase by a monostable or pulse oscillator. After this time one of the pole changing switches changes back to $+V_s$, starting an induction recharge and the clock-regulation-cycle starts again.

Since the only losses in this technique are the saturation loss of the switch and that of the coil resistance, the total efficiency is very high.

The average current that flows from the power supply line is less than the winding current due to the concept of circuit inversion. In this way also the power unit is discharged. This king of phase current control that has to be done separately for each motor phase leads to the best ratio between the supplied electrical and delivered mechanical energy.

POSSIBLE IMPROVEMENTS OF THE UNIPOLAR CIRCUIT

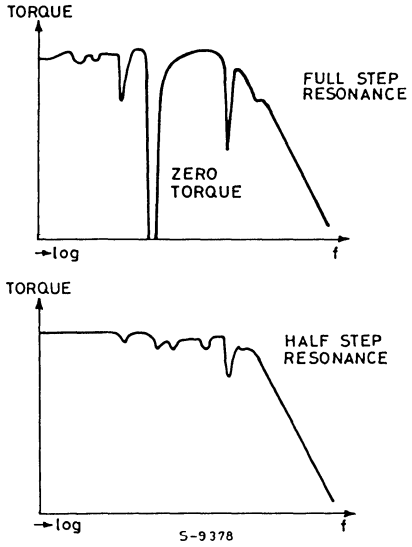
It would make no sense to apply the same principle to a stabilized current controlled unipolar circuit, as two more switches per phase would be necessary for the shortening out of the windings during the free phase and thus the number of components would be the same as for the bipolar circuit; and moreover, there would be the well known torque disadvantage.

ADVANTAGES AND DISADVANTAGES OF THE HALF-STEP

An essential advantage of a stepper motor operating at half-step conditions is its position resolution increased by the factor 2. From a 3.6 degree motor you achieve 1.8 degrees, which means 200 steps per revolution.

This is not always the only reason. Often you are forced to operate at half-step conditions in order to avoid that operations are disturbed by the motor resonance. These may be so strong that the motor has no more torque in certain step frequency ranges and looses completely its position (Fig. 10). This is due to the fact that the rotor of the motor, and the changing magnetic field of the stator forms a spring-mass-system that may be stimulated to vibrate. In practice, the load might deaden this system, but only if there is sufficient frictional force.

Fig. 10 - The motor has no more torque in certain step frequency ranges with full step driving.



In most cases half-step operation helps, as the course covered by the rotor is only half as long and the system is less stimulated.

The fact that the half-step operation is not the dominating or general solution, depends on certain disadvantages:

- the half-step system needs twice as many clock-pulses as the full-step system; the clock-frequency is twice as high as with the full-step.
- In the half-step position the motor has only about half of the torque of the full-step.

For this reason many systems use the half-step operation only if the clock-frequency of the motor is within the resonance risk area.

The dynamic loss is higher the nearer the load moment comes to the limit torque of the motor. This effect decreases at higher numbers of revolutions.

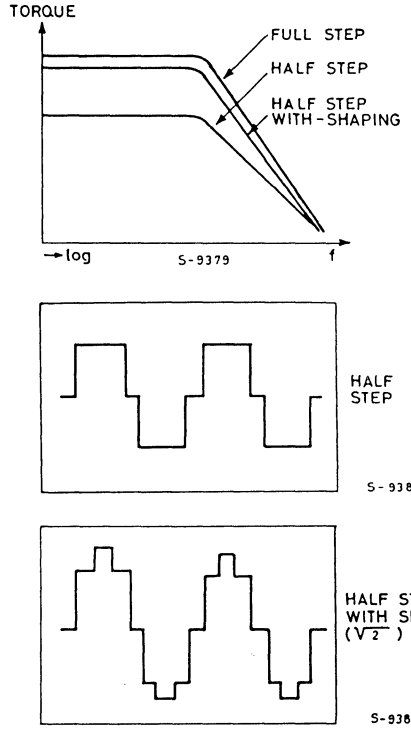
TORQUE LOSS COMPENSATION IN THE HALF-STEP OPERATION

It's clear that, especially in limit situations, the torque loss in half-step is a disadvantage. If one has to choose the next larger motor or one with a double resolution operating in full-step because of some insufficient torque percentages, it will greatly influence the costs of the whole system.

In this case, there is an alternative solution that does not increase the coats for the bipolar chopping stabilized current drive circuit.

The torque loss in the half-step position may be compensated for by increasing the winding current by the factor $\sqrt{2}$ in the phase winding that remains active. This is also permissible if, according to the motor date sheet, the current limit has been reached, because this limit refers always to the contemporary supply with current in both windings in the full-step position. The factor $\sqrt{2}$ increase in current doubles the stray power of the

Fig. 11 - Half step driving with shaping allows to increase the motor's torque to about 95% of that of the full step.



DRIVE SIGNALS FOR THE MICRO ELECTRONIC

A direct current motor runs by itself if you supply if with voltage, whereas the stepping motor needs the commutation signal in for of several separated but linkable commands. In 95% of the applications today, the origin of these digital commands is a microprocessor system.

In its simplest form, a full-step control needs only two rectangular signals in quadrature. According to which phase is leading, the motor axis rotates clockwise or counter-clockwise, whereby the rotation speed is proportional to the clock frequency.

In the half-step system the situation becomes more complicated. The minimal two control signals become four control signals. In some conditions as many as six signals are needed. if the Tri-state-command for the phase ranges without current, necessary for high motor speeds, may not be obtained from the 4 control signals. Fig. 12 shows the relationship between the phase current diagram and the control signal for full and half-step.

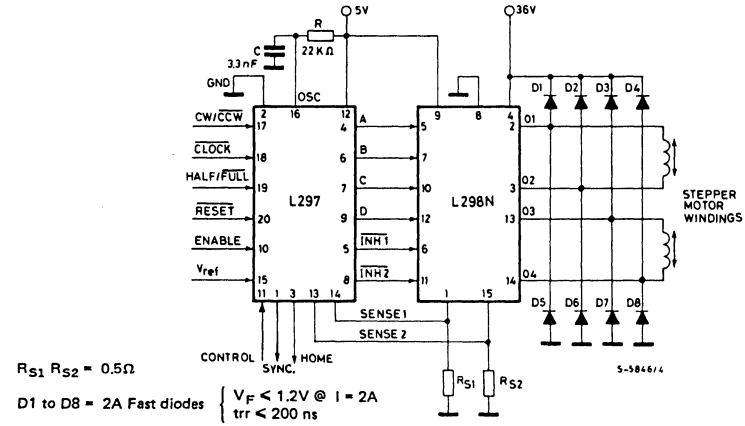
Since all signals in each mode are in defined relations with each other, it is possible to generate them using standard logic. However, if the possibility to choose full and half-step is desired, a good logic implementation becomes quite expensive and an application specific integrated circuit would be better. Such an application specific integrated circuit could reduce the number of outputs required from a microprocessor from the 6 required to 3 static and dynamic control line.

A typical control circuit that meets all these requirements is the L297 unit (Fig. 13).
Four signals control the motor in all operations:

1. CLOCK: The clock signal, giving the stepping command
2. RESET: Puts the final level signals in a defined start position
3. DIRECTION: Determines the sense of rotation of the motor axis
4. HALF/FULL: Desides whether to operate in full or in half-step.

Another inhibit input allows the device to switch the motor output into the Tri-state-mode in order to prevent undesired movements during undefined operating conditions, such as those that could occur during.

Fig. 13 - The L297 avoids the use of complicated standard logic to generate both full and half-step driving signals together with chopper current control.



SWITCH-MODE CURRENT REGULATION

The primary function of the current regulation circuit is to supply enough current to the phase windings of the motor, even at high step rates.

The functional blocks required for a switchmode current control are the same blocks required in switching power supplies; flip-flops, comparators; and an oscillator are required. These blocks can easily be included in the same IC that generates the phase control signals. Let us consider the implementation of chopper current control in the L297.

The oscillator on pin 16 of the L297 resets the two flip-flops at the start of each oscillator period. The flip-flop outputs are then combined with the outputs of the translator circuit to form the 6 control signals supplied to the power bridge (L298).

When activated, by the oscillator, the current in the winding will raise, following the L/R time constant curve, until the voltage across the sense resistor (pin 1, 15 of L298) is equal to the reference voltage input. (pin 15, L297) the comparator then sets the flip-flop, causing the output of the L297 to change to an equiphase condition, thus effectively putting a short circuit across the phase winding. The bridge is activated into a diagonally conductive state when the oscillator resets the flip-flop at the start of the next cycle.

with two resistance and one small signal transistor as changeover switch for the reference input. With another resistance and transistor it is possible to resolve 2 Bits and consequently 4 levels. That is sufficient for all imaginable causes.

Fig. 16 shows a optimal phase current diagram during a positioning operation.

Fig. 15 - Because of the set-dominant latch inside the L297 it is possible to hide current spikes and noise across the sense resistors thus avoiding external filters.

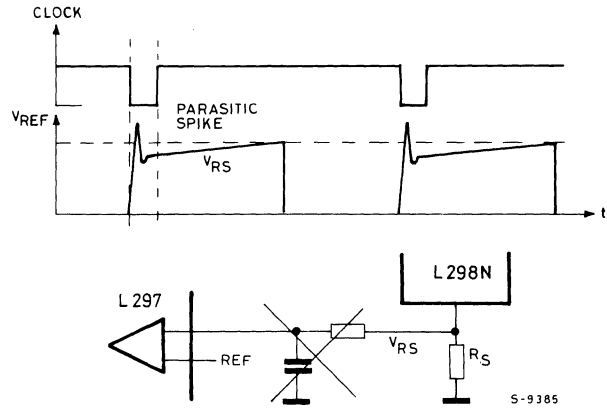
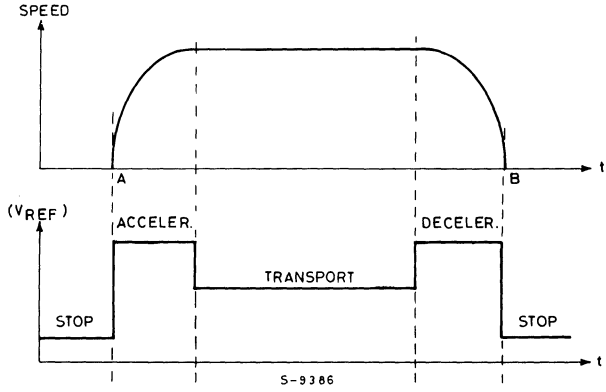


Fig. 16 - More energy is needed during the acceleration and break phases compared the continuous operation, neutral or stop position.



HIGH MOTOR CLOCK RESETS IN THE HALF-STEP SYSTEM

In the half-step position one of the motor phases has to be without current. If the motor moves from a full-step position into a half-step position, this means that one motor winding has to be completely discharged. From the logic diagram this means for the high level bridge an equivalent status of the input signals A/B, for example in the HIGH-status. For the coil this means short circuit (Fig. 17 up) and consequently a low reduction of the current. In case of high half-step speeds the short circuit discharge time constant of the phase winding is not sufficient to discharge the current during the short half-step phases. The current diagram is not neat, the half step is not carried out correctly (Fig. 17 center).

For this reason the L297 controller-unit generates an inhibit-command for each phase bridge, that switches the specific bridge output in the half-step position into Tri-state. In this way the coil can start swinging freely over the external recovery diodes and discharge quickly. The current decrease rate of change corrisponds more or less to the increase rate of change (Fig. 17 below).

In case of full-step operation both inhibit-outputs of the controller (pin 5 and 8) remain in the HIGH-status.

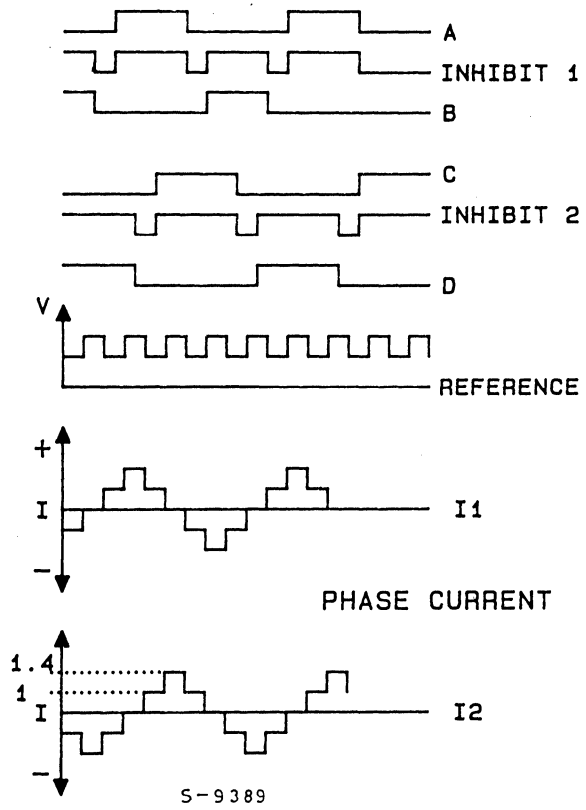
MORE TORQUE IN THE HALF-STEP POSITION

A topic that has already been discussed in detail. So we will limit our considerations on how it is carried out, in fact quite simply because of the reference voltage controlled phase current regulation.

With the help of the inhibit-signals at outputs 5 and 8 of the controller, which are alternatively active only when the half-step control is programmed, the reference voltage is increased by the factor 1.41 with a very simple additional wiring (Fig. 18), as soon as one of the two inhibit-signals switches LOW. This increases the current in the active motorphase proportionally to the reference voltage and compensates the torque loss in this position. Fig. 19 shows clearly that the diagram of the phase current is almost sinusoidal, in principle the ideal form of the current graph.

To sum up we may say that this half-step version offers most advantages. The motor works with poor resonance and a double position resolution at a torque, that is almost the same as that of the full-step.

Fig. 19 - The half-step with shaping positioning is achieved by simply changing reference voltages.



BETTER GLIDING THAN STEPPING

If a stepper motor is supposed to work almost gliding and not step by step, the form of the phase current diagram has to be sinusoidal.

The advantages are very important:

- no more phenomena of resonance
- drastic noise reduction
- connected gearings and loads are treated with care
- the position resolution may be increased further.

However, the use of the L297 controller-unit described until now is no longer possible of the more semplicated form of the phase current diagram the Controller may become simpler in its functions.

Fig. 20 shows us an example with the L6505 unit. This IC contains nothing more than the clocked phase current regulation which works according to

PRECISION OF THE MICRO STEP

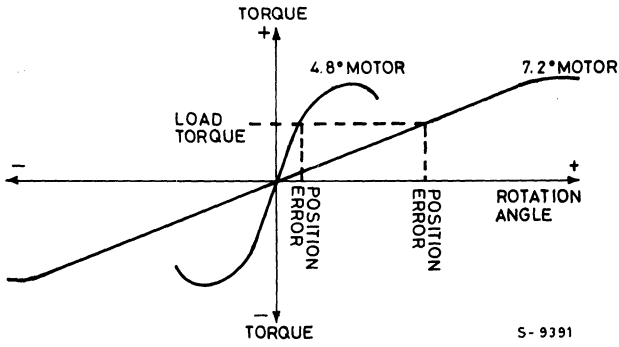
Any desired increase of the position resolution between the full step position has its physical limits. Those who think it is possible to resolve a 7.2° - stepper motor to 1.8° with the same precision as a 1.8° - motor in full-step will be received, as there are several limits:

The rise rate of the torque diagram corresponding to the twisting angle of the rotor for the 7.2° - motor is flatter by a factor of 4 then for the original 1.8° - motor. Consequently with friction or load moment, the position error is larger (Fig. 21).

For most of the commercial motors there isn't a sufficiently precise, linear relationship between a sinusoidal-current-diagram and an exact micro step angle. The reason is a dishomogeneous magnetic field between the rotor and the two stator fields.

Above all, problems have to be expected with motors with high pole feeling. However, there are special stepper motors in which an optimized micro step operation has already been considered during the construction phase.

Fig. 21 - Better resolution is achieved with low degree motor but more torque is delivered with high degree motor.



CONCLUSIONS

The above described application examples of modern integrated circuits show that output and efficiency of stepper motors may be remarkably increased without any excessive expense increase like before.

Working in limit areas, where improved electronics with optimized drive sequences allow the use of less expensive motors, it is even possible to obtain a cost reduction.

CONSTANT-CURRENT CHOPPER DRIVE UPS STEPPER-MOTOR PERFORMANCE

Pulse width-modulated drive improves motor torque and speed yet adds no complexity to circuit

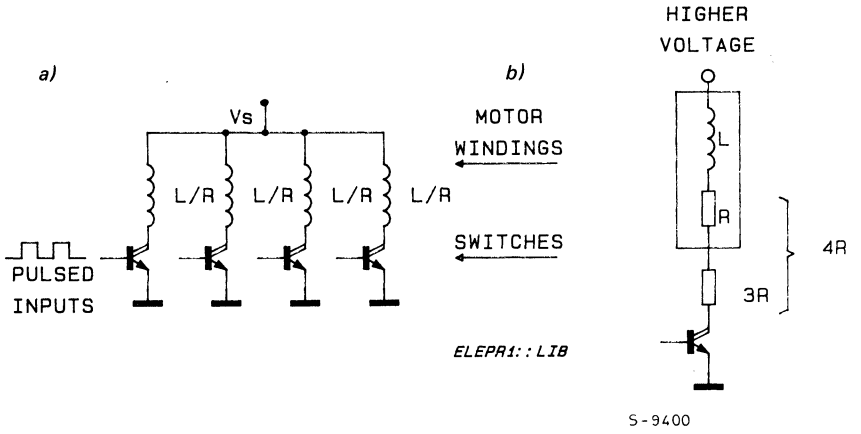
Designers opting to use a fractional-horsepower stepper motor in applications such as computer printers can improve the motor's efficiency and its torque and speed characteristics by using a constant-current pulse-width-modulated (PWM) chopper-drive circuit. What's more, for high-power drives, dedicated control chips and a constant-current chopper drive can be as simple to use as direct drive.

A basic problem for a directly driven stepper is that the motor winding's time constant (L/R) causes the current to increase slowly in the winding during each pulsed input. It may, therefore, never reach full-rated value, especially at high speed, or high pulsing rates, unless the voltage (V_S) across the terminals is high. In the simplest stepper drive (see Fig. 1a), transistor or Darlington switches sequentially activate the windings to drive the motor (see box, "Stepper motor basics").

This type of drive performs poorly because the supply voltage must be low so that the steady-state current is not excessive. As a result, the average winding current - and hence the torque - is very low at high drive motor speed.

Often, this problem is overcome by introducing a series resistance, thereby increasing the overall value by a factor of four - giving an L/4R ratio - and also by increasing the supply voltage (see Fig. 1b). This arrangement reduces the motor's time constant, which improves torque at high step rates. However such an approach is inefficient, because the series resistor constitutes a substantial waste of power.

Fig. 1 - Common unipolar stepping drives (a) produce insufficient torque output because their supply voltage must be kept low to limit current. Adding series resistance to an L/4R ratio (b) and raising the supply voltage proportionately improves torque output, especially at high step rates.



STEPPER-MOTOR BASICS

In computer-peripheral office-equipment applications, the most popular stepper motors are permanent-magnet types with two-phase bipolar windings or bifilar-wound unipolar windings. Stripped to the essentials, both types consist of a permanent-magnet rotor surrounded by stator poles carrying the windings.

A two-pole motor would have a step angle of 90°. However, most motors have multiple poles to reduce the step angle to a few degrees.

A bipolar permanent-magnet stepper motor has a single winding for each phase - and the current must be reversed to reverse the stator field. Bifilar/ hybrid unipolar motors, however, have two windings wound in opposite directions for each phase, so that the field can be reversed with a single-polarity drive. Unipolar motors were once popular because the drive was simpler. But with today's dual bridge (H-bridge) ICs, it is just as easy to drive a bipolar motor.

In the most popular drive technique - two-phase-on - both phases are always energized, and the rotor poles are aligned is stator poler between steps. In another method - called the wave drive - one phase is energized at a time.

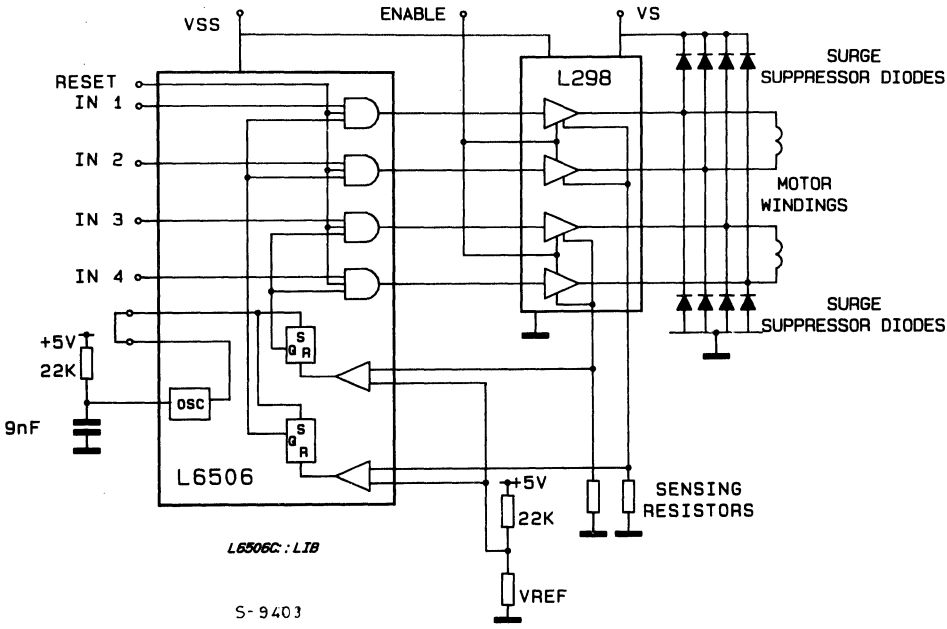
A third technique combines the two sequences and drives the motor one half-step at a time. Half-stepping is very useful because motor mechanically designed for very small step angles are much more complex - and costly - to built. It is more economical to use a 100-step motor in half steps rather than a 200-step motor in full step.

Recently designers have started microstepping, or driving the motor at one-quarter stepping rather or less. This type of operation can obtain fine step control without using mechanically complex motors with small step angles.

A two-phase bipolar motor needing up to 1A/ phase can be driven by a single IC - the SGS L298 dual bridge (see Fig. 4). It contains two H-bridges with all the necessary level shifters and gates to directly interface low-level input logic signals.

As before, a complete chopper drive can be built by adding a current-controller chip and the necessary protective diodes, an RC network to define the oscillator frequency and a reference-voltage divider to set the current level. Four-phase signals to the controller are provided by a controlling micro-

Fig. 4 - A dual-bridge IC provides a simple power-stage design solution for a bipolar stepper motor.



USING THE L6506 FOR CURRENT CONTROL OF STEPPING MOTORS

The L6506 is a linear integrated circuit designed to sense and control the current in stepping motors and other similar devices. When used in conjunction with power stages like the L293, L298N, or L7180 the chip set forms a constant current drive for inductive loads and performs all the interface functions from the control logic through the power stage.

The L6506 may be used with either two phase bipolar or four phase unipolar motor configurations. The circuit in Figure 1 shows the L6506 used in conjunction with the L298N in a 2 phase bipolar stepper motor application. The circuit in Figure 2 implements a similar 4 phase unipolar application.

CURRENT CONTROL LOGIC

In these two circuits, the L6506 is used to sense and control the current in each of the load windings. The current is sensed by monitoring the voltage across a sense resistor (R_{sense}) and using a Pulse Width Modulated control to maintain the current at the desired value.

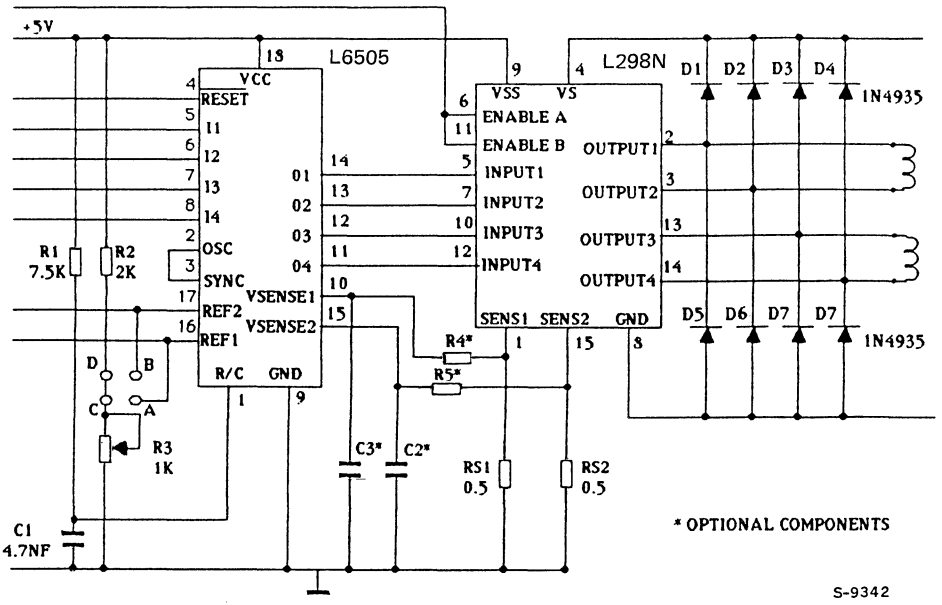
An on-chip oscillator drives the dual chopper and sets the operating frequency. An RC network on pin 1 sets the operating frequency, which is given by the equation:

$$f \simeq \frac{1}{0.69\ R1\ C1} \qquad (1)$$

for $R1 > 10K\Omega$

The oscillator provides pulses to set the two flip-flops, which in turn cause the outputs to activate the power actuator. Once the outputs have been activated the current in the load starts to increase, limited by the inductive characteristic of the load.

Fig. 1 - Application circuit for Bipolar 2 phase stepper motor



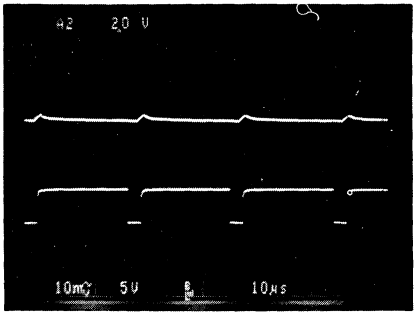
the voltage across the motor during the recirculation time is much less than the power supply voltage. Figure 4 shows the ripple current for bipolar motor applications using the L6506 and the L298.

When implementing a half step drive, both outputs of the L6506 will be low during the half step of one phase. This means a very long time is required for the current in the "off" winding to decay when driving bipolar motors.

Alternately, the power stage (L298) may be inhibited to put the output in the state and achieve a faster current decay.

Since separate V_{ref} inputs are provided for each channel, each of the loads may be programmed independently allowing the device to be used to implement microstepping or applications with different peak and hold currents. In this type of application, changing the reference voltage (V_{ref}) will change the load current, effectively implementing a transconductance amplifier.

Fig. 4 - Ripple current in Bipolar motors



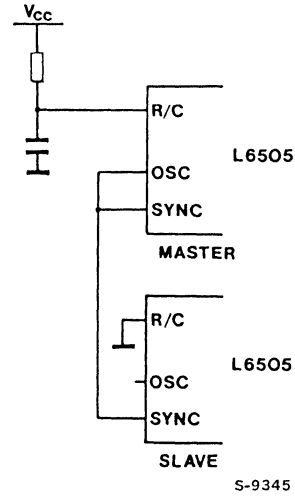
SYNCHRONIZING MULTIPLE DEVICES

Ground noise problems in multiple configurations can be avoided by synchronizing the oscillators. This may be done by connecting the sync pins of each of the devices with the oscillator output of the master device and connecting the R/C pin of the unused oscillators to ground as shown in Figure 5. The devices may be synchronized to external circuits by applying synchronizing pulses to the sync pins. It should be noted, however, that the input pulse sets the minimum on time of the outputs and will therefore set a minimum output average current.

SELECTING THE OSCILLATOR COMPONENTS

When selecting the values for the external components for the oscillator one of the primary considerations is the operating frequency. In addition there is another important consideration for these components.

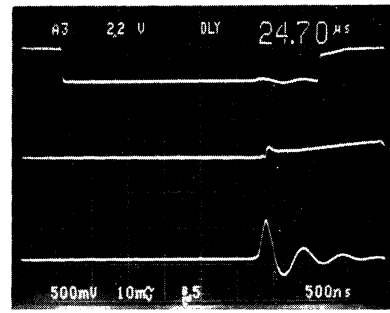
Fig. 5 - Synchronizing multiple devices



In many applications the reverse recovery current of the free wheeling diodes and of parasitic elements in the power stage will flow through the sensing resistor in addition to the load current. Also there is sometimes noise generated in the system when the power stage is switched on. These two sources of error can fool the current limiting stage and make it appear to operate at a subharmonic of the desired frequency. With the proper selection of the oscillator components this behavior can be avoided.

The design of the L6506 is such that the flip-flops used in the device are set dominant so that whenever the sync input is low the Q output of the flip-flop will be high even if the reset is applied by the comparator at the same time. This characteristic of the flip-flops can be used to make the current sensing immune to the recovery currents and noise spikes that occur when the power devices switch. If the sync pulse is longer than the turn on delay time of the power stage, as shown in Figure 6, these two sources of errors will be ignored.

Fig. 6 - Load current and sync pulse

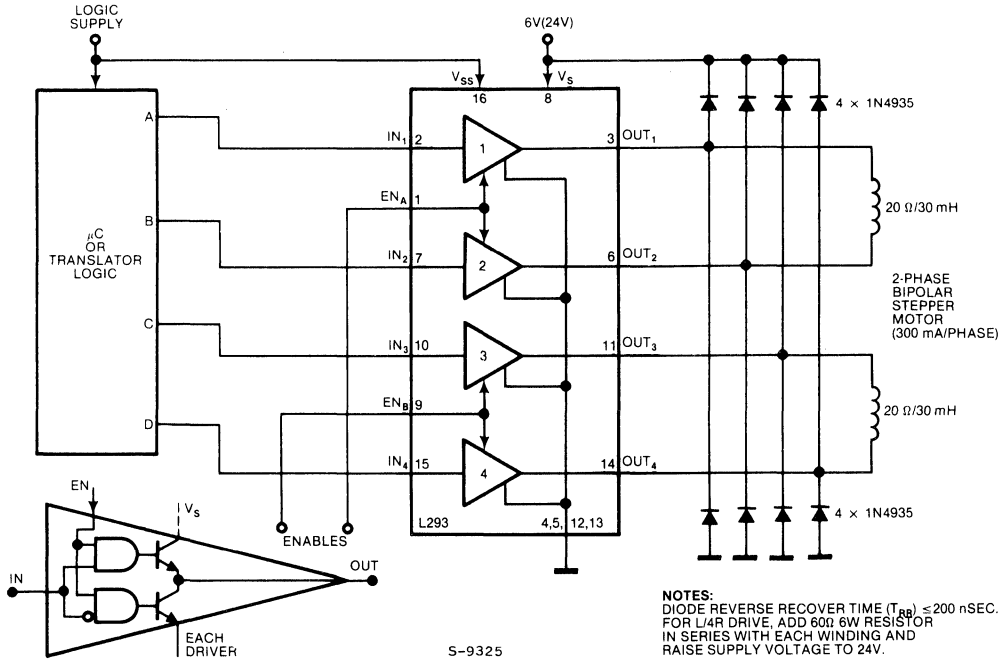


HIGH-POWER, DUAL-BRIDGE ICs EASE STEPPER-MOTOR-DRIVE DESIGN

In addition to simplifying design problems, a family of dedicated chips improves stepper-motor drive-circuit reliability by significantly reducing the component count.

The L293, L293E and L298N dual-bridge ICs (see **box**, "Inside the dual-bridge ICs") significantly reduce the problems encountered in the design of stepper-motor drive circuitry. They can, for example, simplify the design and increase the efficiency of constant--current choppers. And with a single chip replacing the transistors and predriver stages, circuit performance improves. Best of all, the devices have applications in complex as well as basic driver networks.

Fig. 1 - The simplest stepper-motor drive technique is the basic L/R configuration. Adding series resistors and raising the supply to make an L/4R drive improves torque at high steps rates but reduces efficiency.



MULTIPLE SUPPLIES BOOST PERFORMANCE

A dual-level supply also improves the performance of a basic L/R circuit. A high supply voltage yields good torque characteristics when the motor is running. A lower-than-rated voltage provides some holding torque when the motor is at rest, thereby saving power when the motor is idle.

Fig. 2 shows a suitable voltage-switch circuit. R_X sets the holding current, which can be low because a permanent magnet or hybrid stepper motor provides some holding torque at zero current. However, make certain the L293's motor-supply input never goes below the logic-supply voltage. While there's no danger of damaging the device, it's impossible to drive the output transistors correctly under such conditions.

The dual bridge's enable inputs offer a means of extending the chip's flexibility. For example, you can connect them directly to the logic supply — no resistors are needed — to enable the chip permanently. As an alternative, use the enable inputs to disable the motor during the power-on reset sequence.

In wave-drive and half-step modes, use the enable inputs to increase torque at high speeds. When a winding de-energizes, flux collapse is a function of the current-decay rate. During this decay, the de-energized winding opposes the efforts of the next winding in sequence, partially cancelling the torque. You can minimize this effect by disabling a bridge only when the winding it drives is turned off; because the $\Delta i/\Delta t$ of an inductor equals E/L, disabling the bridge accelerates the current decay. This action discharges the winding's stored energy through its supply and maintains the terminal voltage E at V_S plus two diode drops. If you were to leave the bridge enabled, the current would flow to ground through one diode and one transistor, and it would lower the terminal voltage. This scheme doesn't apply with drives with two phases on because no winding ever de-energizes.

Fig. 2 - Switching the supply to a lower voltage when the motor is idle saves current without compromising driving power

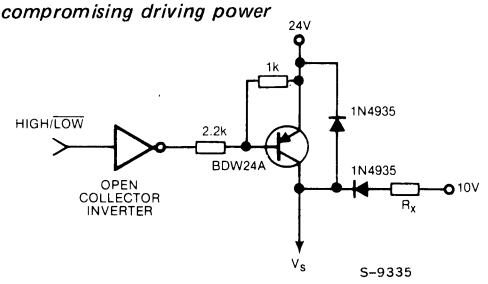
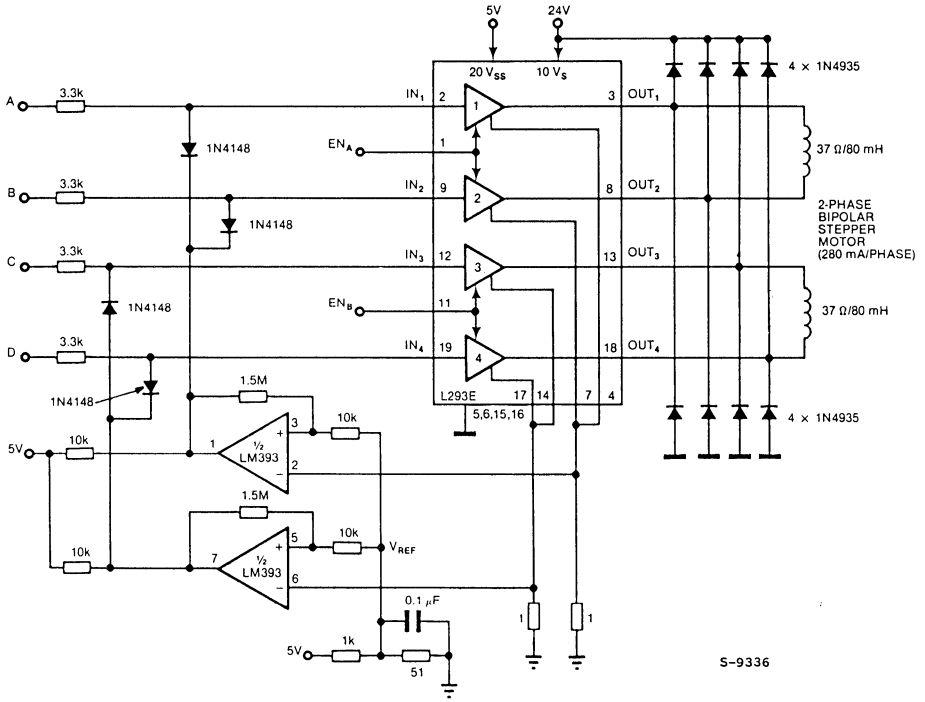


Fig. 3 - Maintaining a constant-average phase current this fixed-ripple chopper provides improved performance and efficiency V_{REF} controls the phase current



Often a μC controls the translator, setting the direction line and providing a pulse for each step. Software is thus simplified, and if you use a programmed interrupt scheme, the μC is free to handle other tasks. Fig. C describes an absolute-positioning routine for a step with a direction-control translator; Fig. D outlines how programmed timer interrupts are used to relieve the burden on the μC.

Two special cases call for hardware translation. The first is in a system for which you have already designed in control circuitry to provide step and direction signals. The second case involves single-quantity and small-run applications, in which the cost of a few ICs is a small price to pay for simplified software.

Fig. C - For use with a hardware translator this a absolute-positioning routine sets the direction line and sends the appropriate number of step pulses.

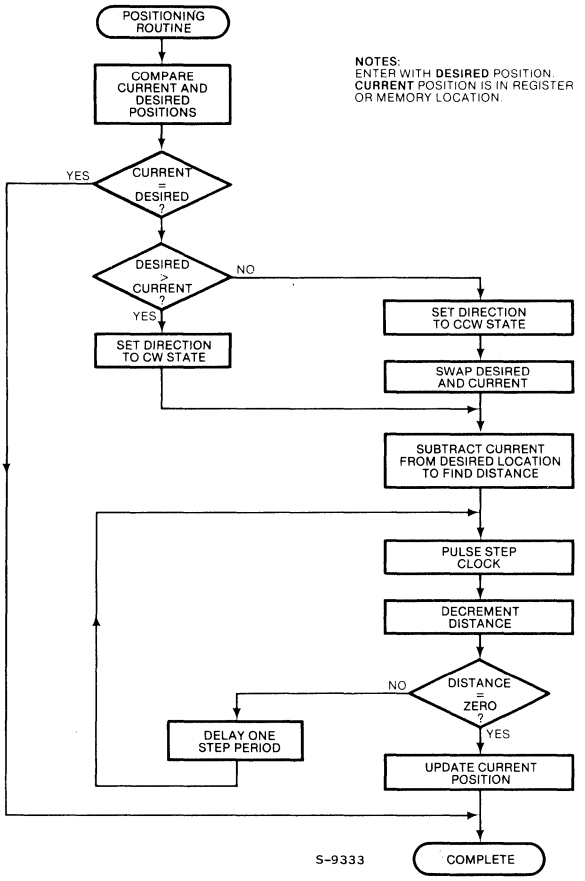


Fig. D - To set a motor step rate, used programmed timer interrupts in place of software timing loops.

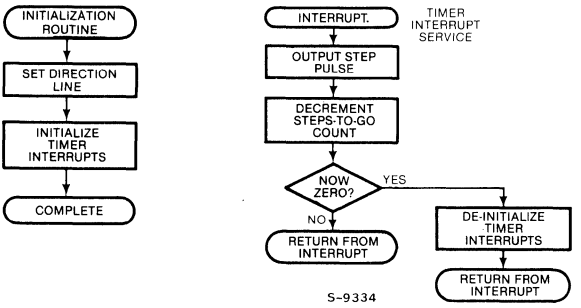
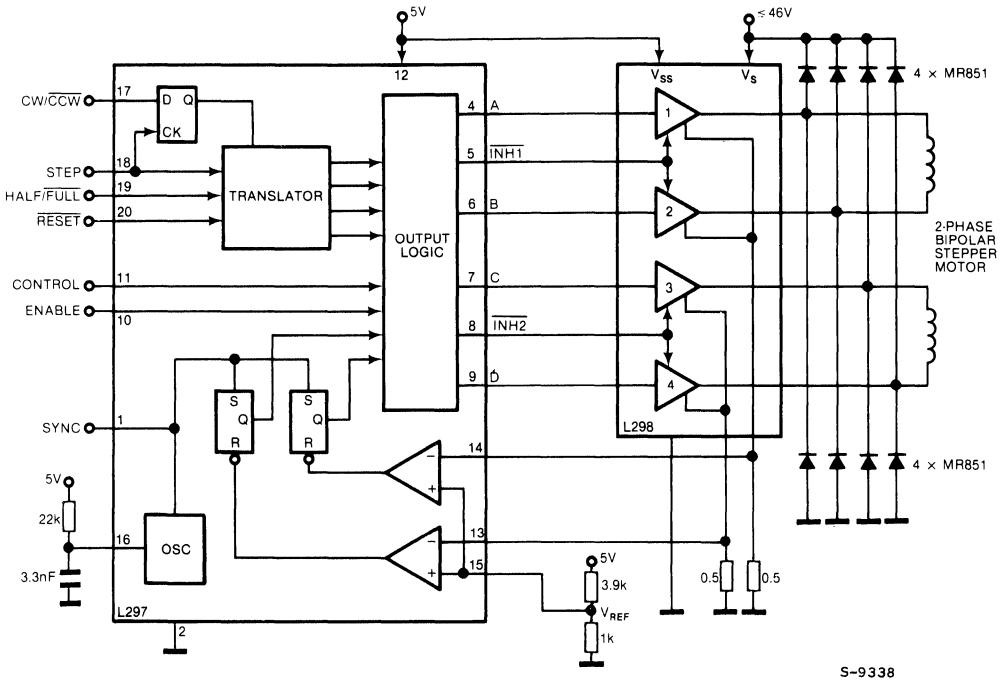


Fig. 5 - A special translator-chopper control circuit cuts the drivers components count to the minimum



CONTROLLER IC REDUCES COMPONENT COUNT

If you're using a hardware translation and constant-current choppers, you can further reduce the component count by using a controller chip such as the L297 – a 20-pin DIP that houses a translator and a dual fixed-frequency chopper circuit. Under the control of step and direction inputs, the L297 generates normal, wave-drive and half-step sequences.

As shown in Fig. 5, the controller connects directly to a dual bridge. External component requirements are minimal: and RC network to set the chopper frequency and a resistive divider to establish the comparator reference voltage (V_{ref}).

To accommodate motors with a phase current as great as 3.5A, replace the single dual-bridge IC with two devices configured in parallel (input to input, enable to enable, etc) to form a single bridge. It's extremely important that you pair the half bridges – 1 with 4 and 2 with 3 – to ensure optimum current sharing.

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INTRODUCING THE L297 STEPPER MOTOR CONTROLLER

The L297 integrates all the control circuitry required to control bipolar and unipolar stepper motors. Used with a dual bridge driver such as the L298N forms a complete microprocessor-to-bipolar stepper motor interface. Unipolar stepper motor can be driven with an L297 plus a quad darlington array. This note describes the operation of the circuit and shows how it is used.

The L297 Stepper Motor Controller is primarily intended for use with an L298N or L293E bridge driver in stepper motor driving applications.

It receives control signals from the system's controller, usually a microcomputer chip, and provides all the necessary drive signals for the power stage. Additionally, it includes two PWM chopper circuits to regulate the current in the motor windings.

With a suitable power actuator the L297 drives two phase bipolar permanent magnet motors, four phase unipolar permanent magnet motors and four phase variable reluctance motors. Moreover, it handles normal, wave drive and half step drive modes. (This is all explained in the section "Stepper Motor Basics").

Two versions of the device are available: the regular L297 and a special version called L297A. The L297A incorporates a step pulse doubler and is designed specifically for floppy-disk head positioning applications.

ADVANTAGES

The L297 + driver combination has many advantages: very few components are required (so assembly costs are low, reliability high and little space required), software development is simplified and the burden on the micro is reduced. Further, the choice of a two-chip approach gives a high degree of flexibility – the L298N can be used on its own for DC motors and the L297 can be used with any power stage, including discrete power devices (it provides 20mA drive for this purpose).

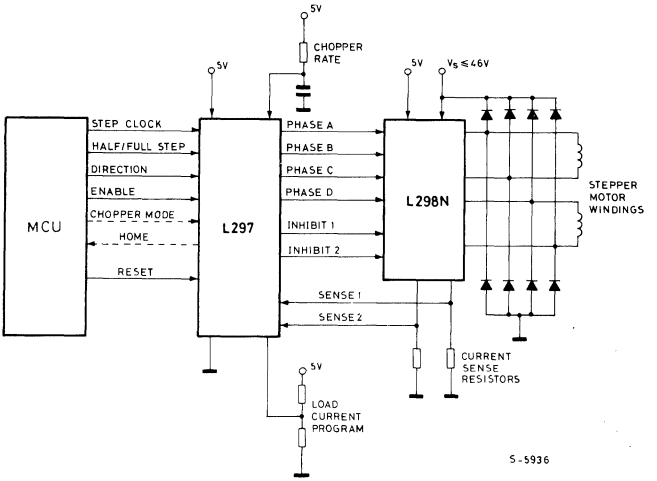
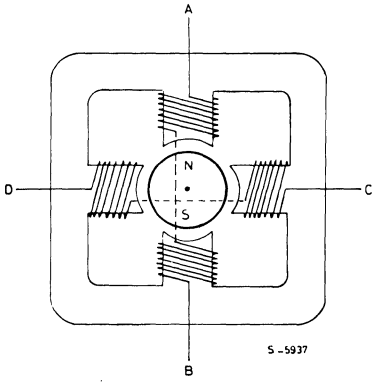


Fig. 1 – In this typical configuration an L297 stepper motor controller and L298 dual bridge driver combine to form a complete microprocessor to bipolar stepper motor interface.

Fig. 3 - Greatly simplified, a bipolar permanent magnet stepper motor consist of a rotating magnet surrounded by stator poles as shown.



energized but in the opposite sense). This sequence is known as "one phase on" full step or wave drive mode. Only one phase is energized at any given moment (figure 4a).

The second possibility is to energize both phases together, so that the rotor always aligns itself between two pole positions. Called "two-phase-on" full step, this mode is the normal drive sequence for a bipolar motor and gives the highest torque (figure 4b).

The third option is to energize one phase, then two, then one, etc., so that the motor moves in half step increments. This sequence, known as half step mode, halves the effective step angle of the motor but gives a less regular torque (figure 4c).

For rotation in the opposite direction (counter-clockwise) the same three sequences are used, except of course that the order is reversed.

As shown in these diagrams the motor would have a step angle of 90°. Real motors have multiple poles to reduce the step angle to a few degrees but the number of windings and the drive sequences are unchanged. A typical bipolar stepper motor is shown in figure 5.

Fig. 4 - The three drive sequences for a two phase bipolar stepper motor. Clockwise rotation is shown.

Fig. 4a - Wave drive (one phase on)

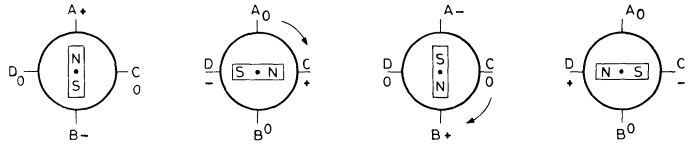


Fig. 4b - Two phase on drive

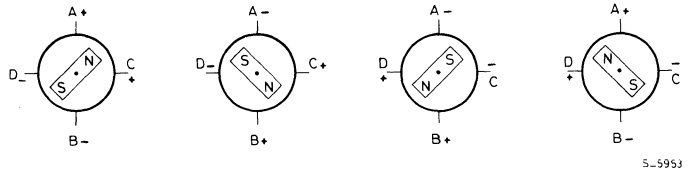
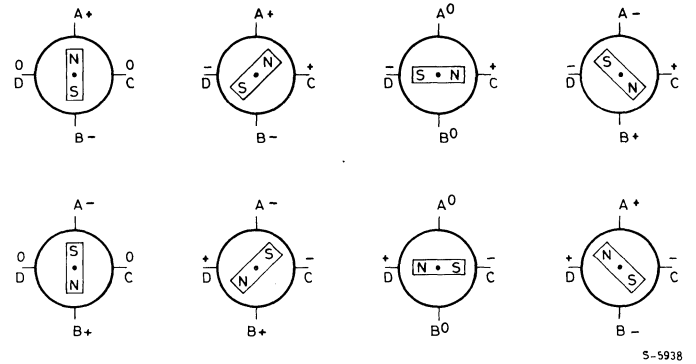


Fig. 4c - Half step drive



The output waveforms for this sequence are shown in figure 10.

Note that two other signals, $\overline{INH1}$ and $\overline{INH2}$ are generated in this sequence. The purpose of these signals is explained a little further on.

The full step modes are both obtained by skipping alternate states in the eight-step sequence. What happens is that the step clock bypasses the first stage of the 3-bit counter in the translator. The least significant bit of this counter is not affected therefore the sequence generated depends on the state of the translator when full step mode is selected (the HALF/$\overline{FULL}$ input brought low).

If full step mode is selected when the translator is at any odd-numbered state we get the two-phase-on full step sequence shown in figure 11.

By contrast, one-phase-on full step mode is obtained by selecting full step mode when the translator is at an even-numbered state (figure 12).

Fig. 8 - The L297 contains translator (phase sequence generator), a dual PWM chopper and output control logic.

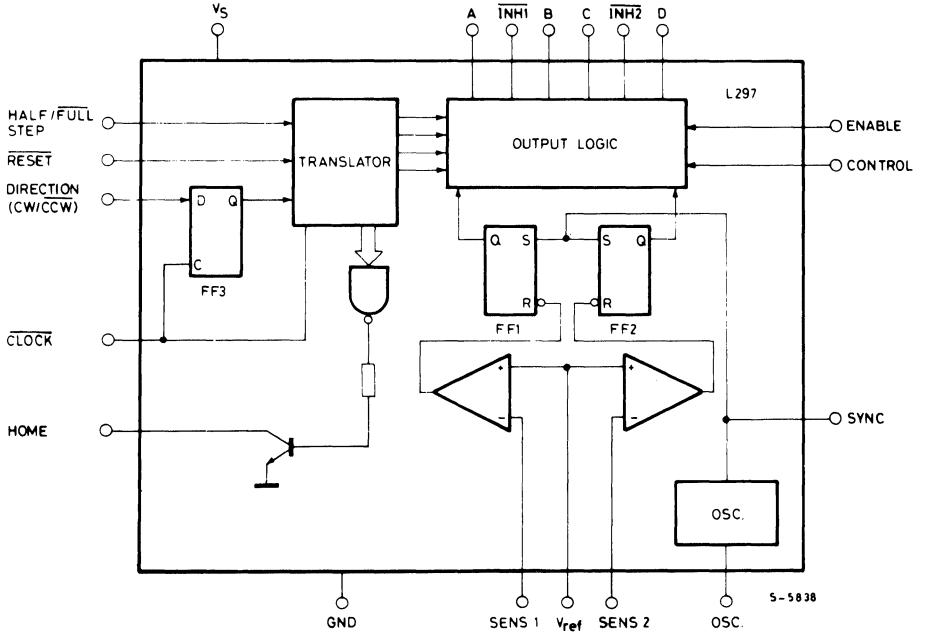


Fig. 9 - The eight step master sequence of the translator. This corresponds to half step mode. Clockwise rotation is indicated.

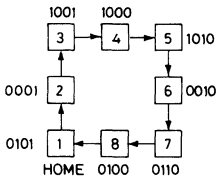


Fig. 10 - The output waveforms corresponding to the half step sequence. The chopper action in not shown.

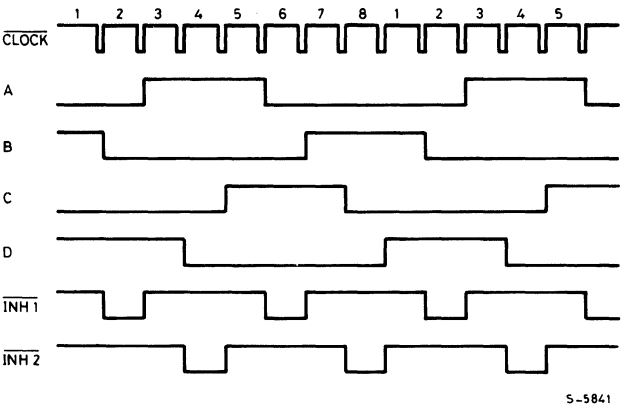
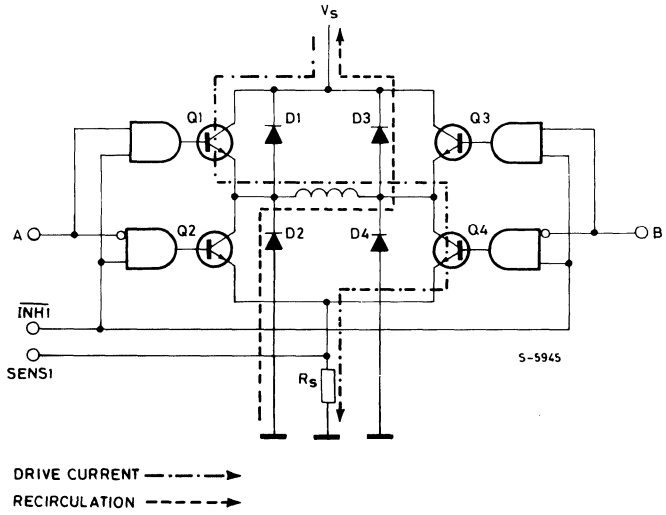


Fig. 13 - When a winding is switched off the inhibit input is activated to speed current decay. If this were not done the current would recirculate through D2 and Q4 in this example. Dissipation in R_S is also reduced.



OTHER SIGNALS

Two other signals are connected to the translator block: the RESET input and the HOME output.

RESET is an asynchronous reset input which restores the translator block to the home position (state 1, ABCD = 0101). The HOME output (open collector) signals this condition and is intended to be ANDed with the output of a mechanical home position sensor.

Finally, there is an ENABLE input connected to the output logic. A low level on this input brings $\overline{INH1}$, $\overline{INH2}$, A, B, C and D low. This input is useful to disable the motor driver when the system is initialized.

LOAD CURRENT REGULATION

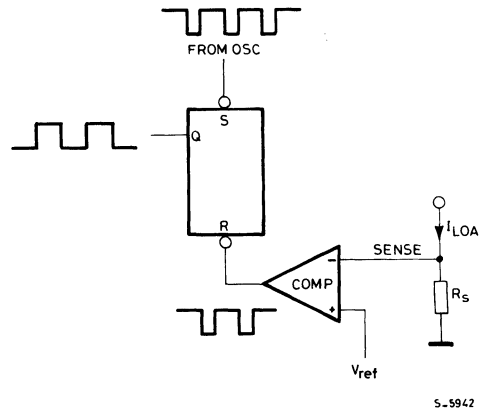
Some form of load current control is essential to obtain good speed and torque characteristics. There are several ways in which this can be done – switching the supply between two voltages, pulse rate modulation chopping or pulse width modulation chopping.

The L297 provides load current control in the form of two PWM choppers, one for each phase of a bipolar motor or one for each pair of windings for a unipolar motor. (In a unipolar motor the A and B windings are never energized together so thay can share a chopper; the same applies to C and D).

Each chopper consists of a comparator, a flip flop and an external sensing resistor. A common on-chip oscillator supplies pulses at the chopper rate to both choppers.

In each chopper (figure 14) the flip flop is set by each pulse from the oscillator, enabling the output and allowing the load current to increase. As it increases the voltage across the sensing resistor increases, and when this voltage reaches V_{ref} the flip flop is reset, disabling the output until the next oscillator pulse arrives. The output of this circuit (the flip flop's Q output) is therefore a constant rate PWM signal. Note that V_{ref} determines the peak load current.

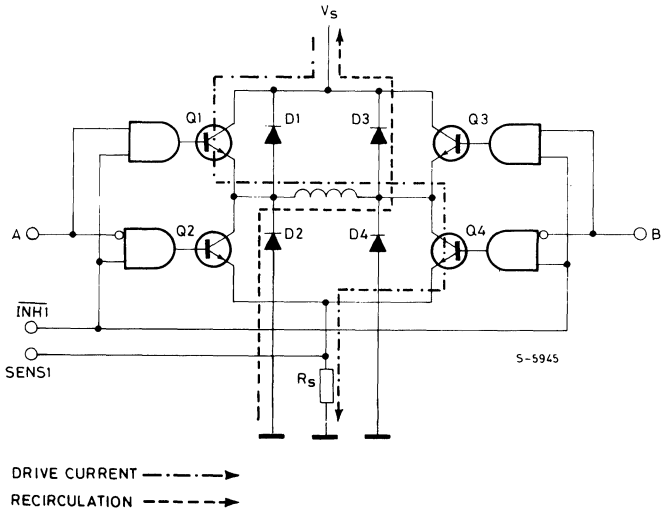
Fig. 14 - Each chopper circuit consists of a comparator, flip flop and external sense resistor. A common oscillator clocks both circuits.



This explains why phase chopping is not suitable for unipolar motors: when the A winding is driven the chopper acts on the B winding. Clearly, this is no use at all for a variable reluctance motor and would be slow and inefficient for a bifilar wound permanent magnet motor.

The alternative is to tie the CONTROL input to ground so that the chopper acts on $\overline{INH1}$ and $\overline{INH2}$. Looking at the same example, A is high and B low. Q1 and Q4 are therefore conducting and current flows through Q1, the winding, Q4 and R_S (figure 17).

Fig. 17 - Inhibit chopping. The drive current (Q1, winding, Q4) in this case is interrupted by activating $\overline{INH1}$. The decay path through D2 and D3 is faster than the path Y of figure 15.



In this case when the voltage across R_S reaches V_{REF} the chopper flip flop is reset and $\overline{INH1}$ activated (brought low). $\overline{INH1}$, remember, turns off all four transistors therefore the current recirculates from ground, through D2, the winding and D3 to V_S. Discharged across the supply, which can be up to 46V, the current decays very rapidly (figure 18).

The usefulness of this second faster decay option is fairly obvious; it allows fast operation with bipolar motors and it is the only choice for unipolar motors. But why do we offer the slower alternative, phase chopping?

The answer is that we might be obliged to use a low chopper rate with a motor that does not store much energy in the windings. If the decay is very fast the average motor current may be too low to give an useful torque. Low chopper rates may, for example, be imposed if there is a larger motor in the same system. To avoid switching noise on the ground plane all drivers should be synchronized and the chopper rate is therefore determined by the largest motor in the system.

Multiple L297s are synchronised easily using the SYNC pin. This pin is the squarewave output of the on-chip oscillator and the clock input for the choppers. The first L297 is fitted with the oscillator components and outputs a squarewave signal on this pin (figure 19). Subsequent L297s do not need the oscillator components and use SYNC as a clock input. An external clock may also be injected at this terminal if an L297 must be synchronized to other system components.

Fig. 18 - Inhibit chopper waveforms. Winding AB is energized and CONTROL is low.

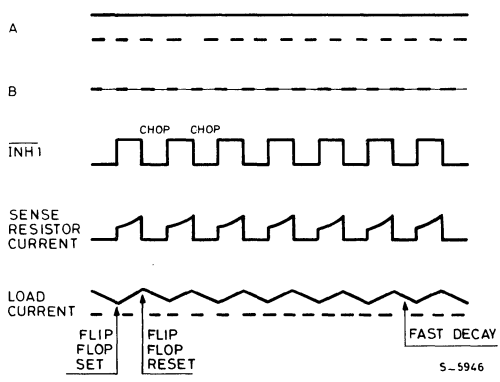
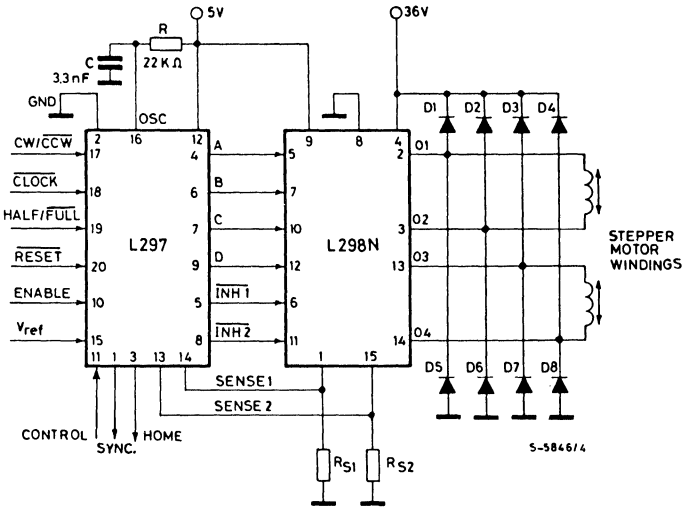


Fig. 21 - This typical application shows an L297 and L298N driving a bipolar stepper motor with phase currents up to 2A



R_{S1} R_{S2} = 0.5Ω

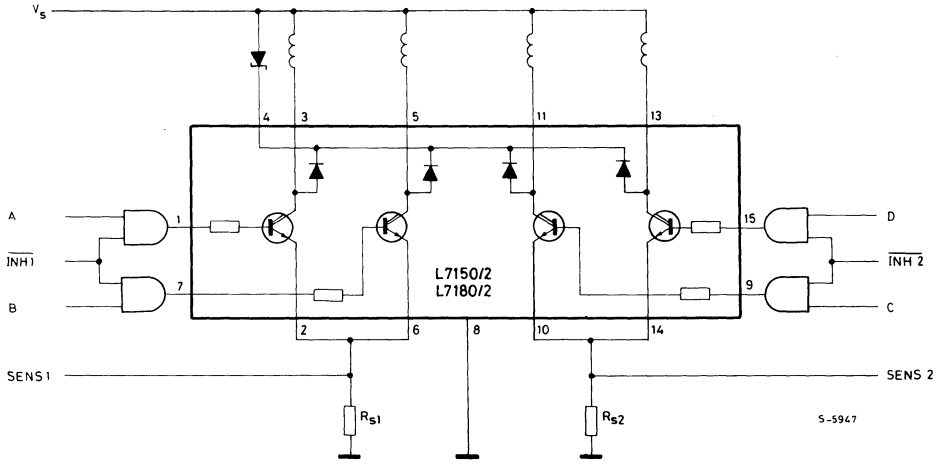
D1 to D8 = 2 Fast Diodes { $V_F \leqslant 1{,}2V$ @ I = 2A; trr ⩽ 200 ns

made with discrete transistors. For currents up to 3.5A two L298N's with paralleled outputs may be used.

For unipolar motors the best choice is a quad darlington array. The L702 can be used if the choppers are not required but an L7150 or L7180 is preferred. These quad darlingtons have external emitter connections which are connected to sensing resistors (figure 22). Since the chopper acts on the inhibit lines, four AND gates must be added in this application.

Also shown in the schematic is a zener diode in series with the suppression diodes. This serves to increase the voltage across which energy stored in

Fig. 22 - For unipolar motors a quad darlington array is coupled to the L297. Inhibit chopping is used so the four AND gates must be added.



PIN FUNCTIONS – L297 (continued)

N°	NAME	FUNCTION
7	C	Motor phase C drive signal for power stage.
8	$\overline{INH2}$	Active low inhibit control for drive stages of C and D phases. Same functions as $\overline{INH1}$.
9	D	Motor phase D drive signal for power stage.
10	ENABLE	Chip enable input. When low (inactive) $\overline{INH1}$, $\overline{INH2}$, A, B, C and D are brought low.
11	CONTROL	Control input that defines action of chopper. When low chopper acts on $\overline{INH1}$ and $\overline{INH2}$; when high chopper acts on phase lines ABCD.
12	V_s	5V supply input.
13	$SENS_2$	Input for load current sense voltage from power stages of phases C and D.
14	$SENS_1$	Input for load current sense voltage from power stages of phases A and B.
15	V_{ref}	Reference voltage for chopper circuit. A voltage applied to this pin determines the peak load current.
16	OSC	An RC network (R to V_{CC}, C to ground) connected to this terminal determines the chopper rate. This terminal is connected to ground on all but one device in synchronized multi - L297 configurations. $f \cong 1/0.69\ RC$, $R > 10\ k\Omega$.
17	CW/$\overline{CCW}$	Clockwise/counterclockwise direction control input. Physical direction of motor rotation also depends on connection of windings. Synchronized internally therefore direction can be changed at any time.
18	$\overline{CLOCK}$	Step clock. An active low pulse on this input advances the motor one increment. The step occurs on the rising edge of this signal.
19	HALF/$\overline{FULL}$	Half/full step select input. When high selects half step operation; when low selects full step operation. One-phase-on full step mode is obtained by selecting FULL when the L297's translator is at an even-numbered state. Two-phase-on full step mode is set by selecting FULL when the translator is at an odd numbered position. (The home position is designated state 1).

APPLICATIONS OF MONOLITHIC BRIDGE DRIVERS

High power monolithic bridge drivers are an attractive replacement for discrete transistors and half bridges in applications such as DC motor and stepper motor driving. This application guide describes three such devices – the L293, L293E and L298 – and presents practical examples of their application.

The L293, L293E and L298 each contain four push-pull power drivers which can be used independently or, more commonly, as two full bridges. Each driver is controlled by a TTL-level logic input and each pair of drivers is equipped with an enable input which controls a whole bridge. All three devices feature a separate logic supply input so that the logic can be run on a lower supply voltage, reducing dissipation. This logic supply is internally regulated.

Additionally, the L293E and L298 are provided with external connections to the lower emitters of each bridge to allow the connection of current sense resistors. The L293E has separate emitter connections for each channel; the L298 has two, one for each bridge.

Figure 1 shows the internal structure of the L293, L293E and L298. The L293 and L293E are represented as four push pull drivers while the internal schematic is given for the L298. Though they are drawn differently the L293E and L298 are identical in structure; the L293 differs in that it does not have external emitter connections.

Fig. 1 - The L293, L293E and L298 contain four push pull drivers. Each driver is controlled by a logic input and each pair (a bridge) is controlled by an enable input. Additionally, the L293E has external emitter connections for each driver and the L298 has emitter connections for each bridge.

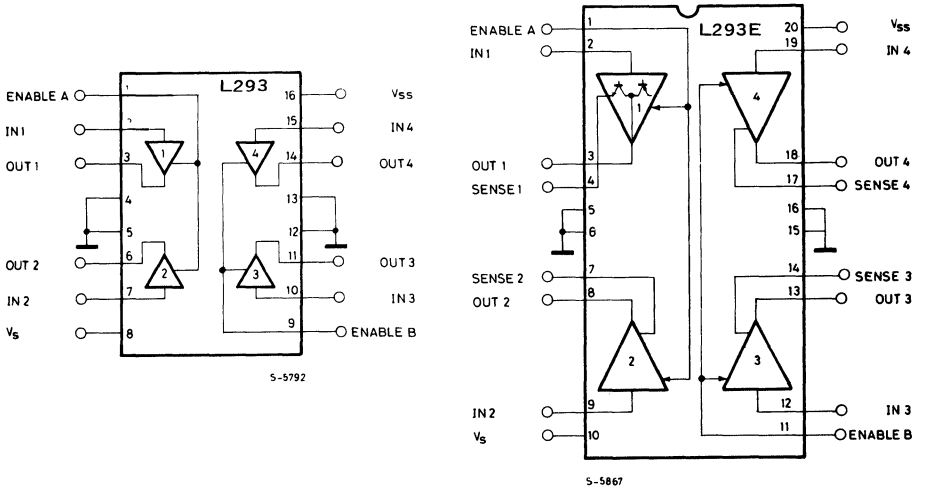


Fig. 3 - This circuit protects a driver from output short circuits to ground.

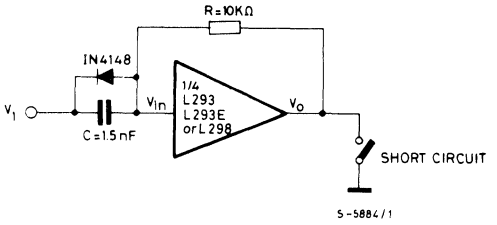
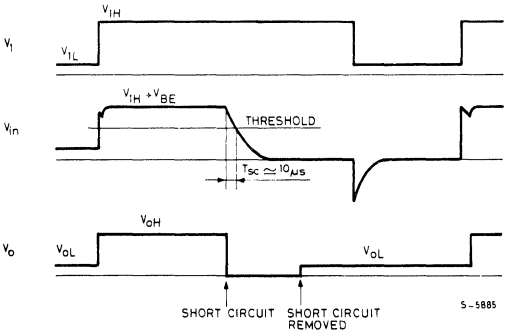


Fig. 4 - Waveforms illustrating the short circuit protection provided by the circuit of fig. 3.



DC MOTOR DRIVING

In applications where rotation is always in the same sense a single driver (half bridge) can be used to drive a small DC motor. The motor may be connected either to supply or to ground as shown in figure 5.

The only difference between these two alternatives is that the control logic is inverted — a useful fact to remember when minimising control logic.

Each device can drive four motors connected in this way. The maximum motor current is 1A for the L293 and 2A for the L298N. However if several motors are driven continuously care should be taken to avoid exceeding the maximum power dissipation of the package.

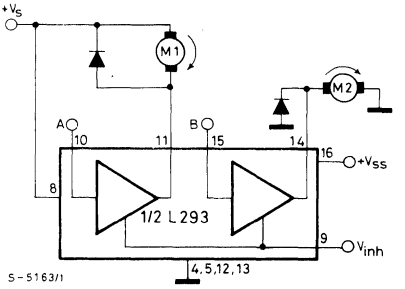
Each motor in this configuration is controlled by its own logic input which gives two alternatives: run and fast stop (the motor shorted by one of the transistors).

The enable/inhibit inputs also allow a free running motor stop by turning off both transistors of the driver. Since these inputs are common to two channels (one bridge) this feature can only be used when both channels are disabled together.

A full bridge configuration is used to drive DC motors in both directions (figure 6). Using the logic inputs of the two channels the motor can be made to run clockwise, run anticlockwise or stop rapidly.

Again, the enable/inhibit input is used for a free running stop — it turns off all four transistors of

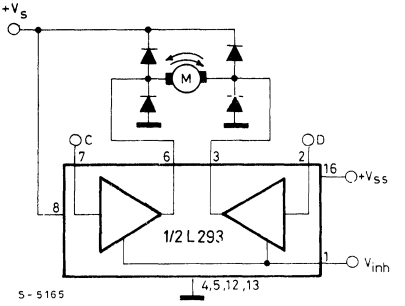
Fig. 5 - For rotation in one direction DC motors are driven by one channel and can be connected to supply or ground.



V_{inh}	A	M1	B	M2
H	H	Fast motor stop	H	Run
H	L	Run	L	Fast motor stop
L	X	Free running motor stop	X	Free running motor stop

L = Low H = High X = Don't care

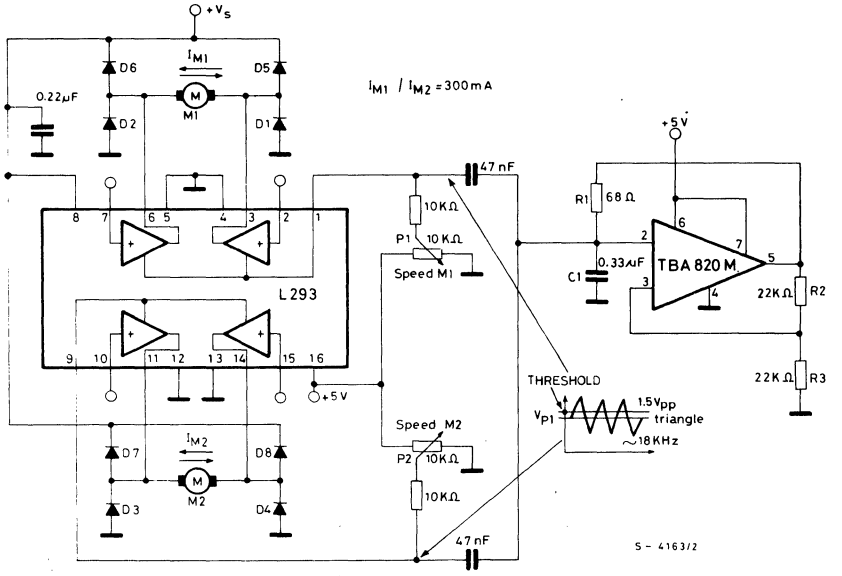
Fig. 6 - A bridge is used for bidirectional drive of DC motors.



INPUTS		FUNCTION
V_{inh}= H	C = H; D = L	Turn right
	C = L; D = H	Turn left
	C = D	Fast motor stop
V_{inh}= L	C = X; D = X	Free running motor stop

L = Low H = High X = Don't care

Fig. 8 - This circuit illustrates PWM control of the motor speed. The speed of each motor is controlled independently.



STEPPER MOTOR DRIVING

Monolithic bridge drivers are extremely useful for stepper motor driving because they simplify the use of bipolar motors. This is an important point since a bipolar stepper motor costs less than an equivalent unipolar motor (it has fewer windings) and gives more torque per unit volume, other things being equal.

The basic configuration for bipolar stepper motor driving is shown in figure 9. In this example it is assumed that a suitable translator (phase sequence generator) is connected to the four channel inputs.

Either an L293 or an L298N can be used in this circuit; an L293E would be wasted compared to an L293 because load current regulation, and hence the sense resistor connection, is not used.

But load current regulation is highly desirable to exploit the performance characteristics of the motor. Using an L293E or L298N this can be implemented by adding an LM339 quad comparator as shown in figure 10.

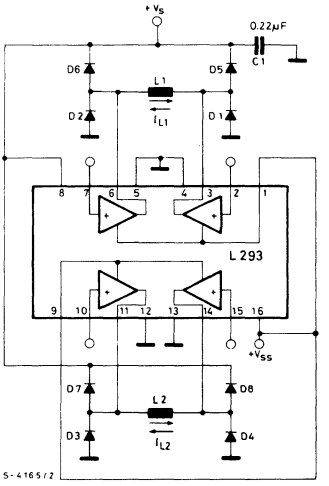
This is another circuit that requires an external translator but it provides independent PWM chopper regulation of the current in each winding.

Looking at motor phase one, the comparator output is initially high, enabling the bridge through pin 1.

The current in the motor winding rises until the voltage across the sensing resistor R2 produces a voltage at the inverting input of the comparator equal to the voltage on the non-inverting input (370 mV). This value is produced by the divider R10/R11 and by the hysteresis determined by R6 and R8.

At this point the comparator switches, disabling the bridge. The current in the winding recirculates through D5 and D6 until the voltage across R2 falls below the lower threshold of the comparator. The comparator then switches again and the cycle repeats.

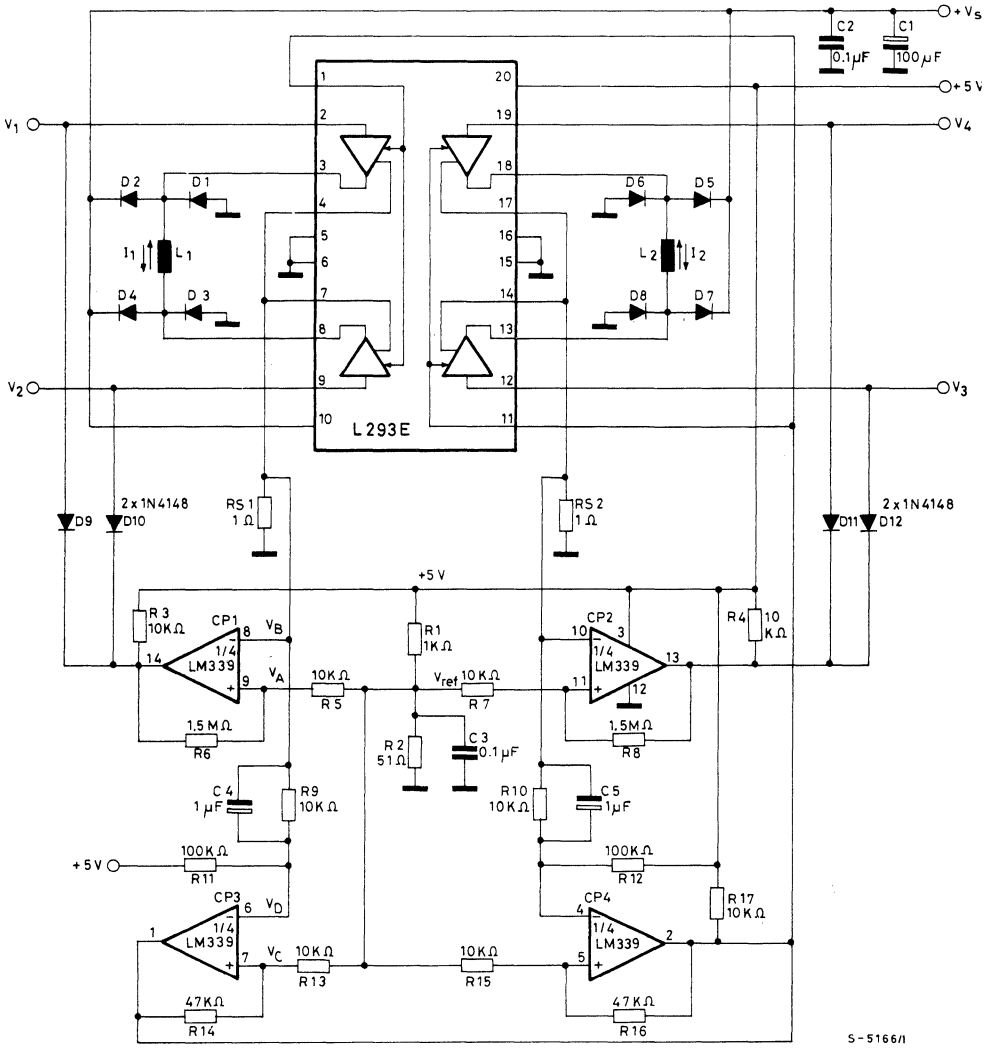
Fig. 9 - A single device can be used to drive a two phase bipolar stepper motor.



In this configuration the motor is controlled through the L297. A step clock moves the motor one increment, the CW/$\overline{CCW}$ input controls the direction and the HALF/$\overline{FULL}$ input selects half step or normal operation. The input V_{ref} is connected to a suitable voltage reference and sets the peak winding current in the motor. The choppers in the L297 can operate on the phase lines or the inhibit lines, depending on the state of the logic input called CONTROL.

For a more detailed description of the L297 see "Introducing the L297 Stepper Motor Controller".

Fig. 11 - With a quad comparator both current regulation and short circuit protection can be obtained.



SWITCH-MODE DRIVERS FOR SOLENOID DRIVING

This design guide describes the operation and applications of the L294 and L295 switch-mode solenoid drivers. Integrating control circuitry and power stage on the same chip, these devices replace complex discrete circuits, bringing space and cost savings.

Many applications, particularly in computer peripherals, require a high power, fast solenoid driver circuit. In the past these circuits have been realised with discrete components because the high powers required precluded the use of monolithic technology.

SGS has overcome this problem with a new high power bipolar technology that uses an innovative implanted isolation technique. This technology is used to fabricate two switchmode solenoid driver chips, the L294 and L295, which both incorporate high power output stages and control circuitry. Both circuits are designed for efficient switchmode operation and are mounted in SGS' Multiwatt® plastic package.

THE L294 SOLENOID DRIVER

The L294 is designed for solenoid driving applications where both very high speed and high current are essential; needle and hammer driving in printer mechanisms, for example. It delivers 4A with supply voltages up to 46V, handling effective powers up to 180W.

Shown in figure 1, the L294 is controlled by a TTL — level logic input and the peak load current is

Fig. 1 - Internal block diagram of the L294 switchmode solenoid driver.

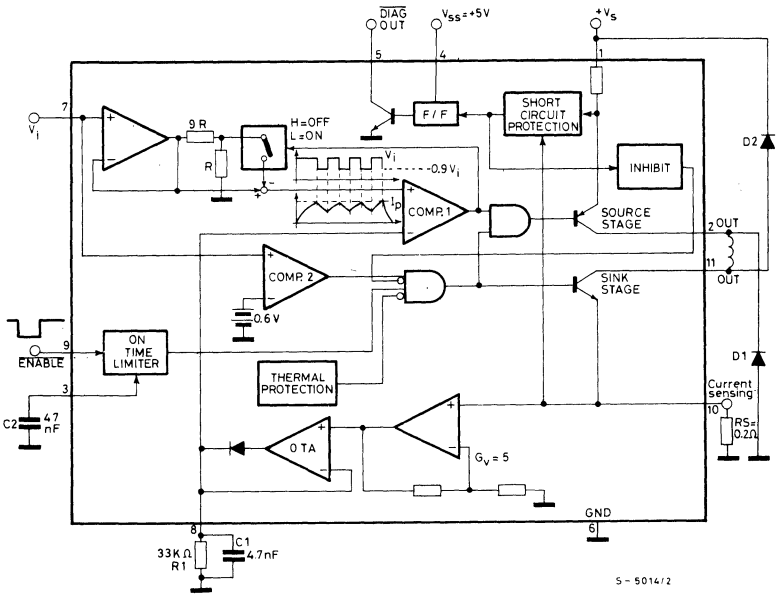
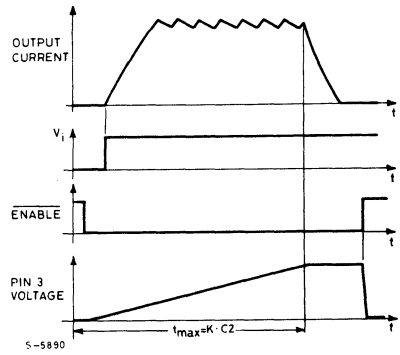


Fig. 4 - On-time limiter waveforms. After a period defined by C2 the output is disabled regardless of the state of ENABLE, protecting against overdriving.



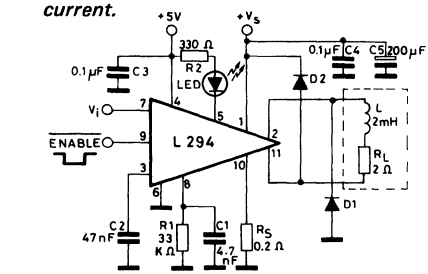
PROTECTION

To protect the load and the L294 from overdriving an on-time limiter inhibits the output stage independently of the ENABLE input if the duration of the input pulse exceeds a period set by the external capacitor C2 (figure 4). This circuit is reset by taking the ENABLE input high. The on-time limiter can be disabled by grounding pin 3.

Protection against overheating is incorporated in the form of a thermal shutdown circuit which disables the output stage when the junction temperature exceeds 150°C. The circuit restarts when the temperature has fallen about 20°C.

The L294 is also protected against short circuits to ground, to supply and across the load. Triggered when the source stage current exceed 5A or the sink stage current exceed $1V/R_S$, the short circuit protection block inhibits the output stage and sets a flip flop which is supplied by a separate supply voltage V_{SS}. This flip flop is connected to the diagnostic output and signals that all is not well — a shorted solenoid, for example. The diagnostic flip flop is reset by removing the supply V_S.
A LED can be connected to the diagnostic output as shown in figure 5. If the diagnostic function is not required the V_{SS} supply can be omitted. The short circuit protection, however, still functions, even without V_{SS}.

Fig. 5 - Standard solenoid driving application of the L294. Pin 7 must be connected to a suitable reference voltage to set the peak current.



USING THE L294

The basic application circuit for the L294 is shown in figure 5; a suggested layout is given in figure 6. The circuit is complete except for the source of V_i. In most cases this will be provided by a simple resistive divider dimensioned to set the desired peak current. With a 0.2 Ω sense resistor as shown, the L294 has a transconductance of 1A/V for V_i above 600 mV. The device will not work with V_i less than 450 mV and operation is not guaranteed for V_i between 450 mV and 600 mV.

The on-time limiter delay — set by C2 — is approximately 120 000 x C2. Pin 3 must be grounded if the on-time limiter isn't used.

Switching frequency depends partly on the timing network R1C1 and partly on the load characteristics.

Fig. 6 - Suggested printed circuit board layout for the application circuit of figure 5.

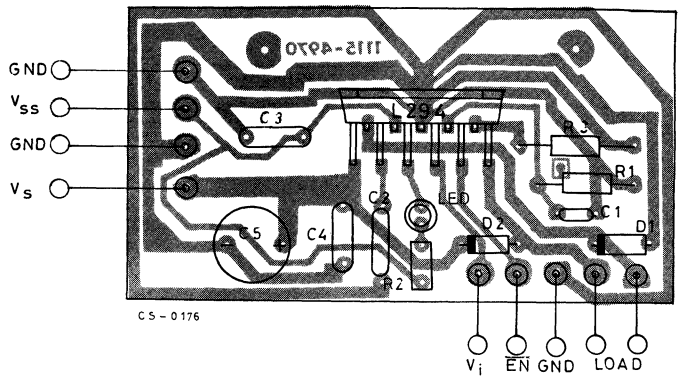


Figura 8 – Pin functions of the L294.

N°	FUNCTION
1	Solenoid supply voltage V_S (12-46V).
2	Output, source stage.
3	On-time limiter time constant. A capacitor to ground sets delay period (120 000 x C2 seconds). On-time limiter is disabled by grounding this pin.
4	Supply input (5V) for diagnostic flip flop.
5	Diagnostic output, open collector. Signals intervention of latched short circuit protection. Reset by removing pin 1 supply.
6	Ground.
7	V_i reference input. Peak output current is proportional to V_i. Transconductance is 1A/V for R_S = 0.2 Ω and $V_i \geqslant 600$ mV.
8	Timing. A parallel RC network from this pin to ground sets the minimum recirculation time constant. The capacitor must be 2.7-10 nF to ensure stability. The resistor must be greater than 10 kΩ.
9	$\overline{\text{ENABLE}}$. TTL-compatible logic input that controls the solenoid current. The solenoid is driven when this input is at a low level. The on-time limiter overrides enable.
10	Connection for load current sense resistor.
11	Output, sink stage.

THE L295 DUAL SWITCHMODE DRIVER

The L295 is a dual switchmode solenoid driver which handles up to 2.5A per channel at voltages up to 46V – a total effective power handling of 220W. Compared to the L294 it offers a more economical solution when 2.5A is sufficient because there are two drivers per chip. Like the L294 it features switchmode regulation of the output current and thermal shutdown. Additionally it has a separate logic supply input so that the logic can be run at a lower voltage, reducing dissipation.

Intended for inductive load driving, the L295 is particularly suitable for solenoids and stepper motors. One L295 drives two solenoids and two L295s can drive the four phases at a unipolar stepper motor or the two phases of a bipolar stepper motor in bridge configuration.

Each channel of the L295 is controlled by a TTL-level digital input and the peak load current is programmed, independently for each channel, by a voltage reference input. A chip enable input is also provided to disable both channels together.

INSIDE THE L295

Internally the L295 (figure 9) bears little resemblance to the L294. Looking at channel one, when the V_{IN1} input goes high the output transistors Q1 and Q2 are switched on (the enable input $\overline{\text{EN}}$ is assumed to be active, i.e. low). The current in the load then rises exponentially, as shown in figure 10, until the voltage across the external sense resistor R_{S1} reaches the current program reference voltage V_{ref1}.

The comparator COMP1 switches and sets the flip flop FF1 which turns off the source transistor Q1. The load current now recirculates through D2-Q2-R_{S1} and decays.

What happens next is determined by the oscillator components R and C on pin 9. If these components are present the flip flop is reset by the next clock pulse before the current decays very far. The output stage is therefore turned on again and the load current rises.

When it reaches the peak value COMP1 switches again, setting the flip flop and disabling the output stage. This process is repeated, regulating the load current until V_{in1} goes low. The output stage is then disabled and the current falls off rapidly, recirculating through D1 and D2 (figure 10).

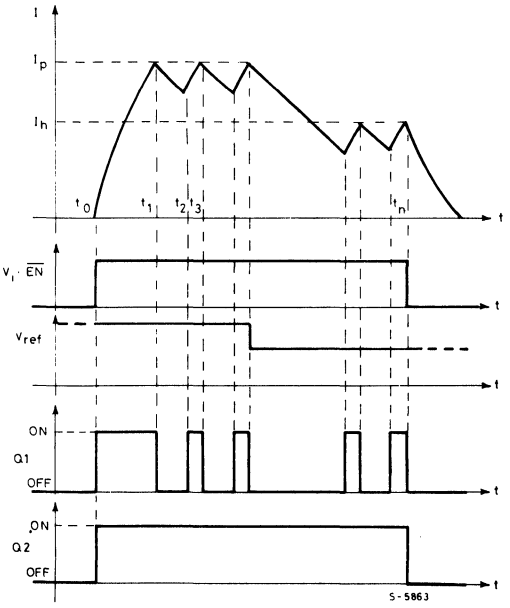
If the oscillator components are omitted and pin 9 grounded the current simply decays slowly until V_{in1} goes low. The output stage is then disabled and the load current recirculates through D1 and D2. This case is illustrated by the waveforms of figure 11. Note that in this case the peak current level is controlled.

Unlike the L294, the switching frequency of the current regulation loop is determined by the oscillator components R and C (the L294 is also affected by the load). Typically, the switching frequency will be 10-30 kHz. Another difference between the two devices is that the L294 gives a constant ripple, the L295 does not.

TWO LEVEL CONTROL

Since the peak load current is programmed by the reference voltage (for each channel), two level current control can be obtained by switching between two reference voltages. A high V_{ref} is selected initially to give a high initial current peak. Then, after a suitable interval, V_{ref} is reduced to give the lower holding current (figure 12). Two level current control is very useful for solenoids which require a high initial current peak for fast actuation.

Fig. 12 - Two level current control is obtained by switching V_{ref} between two values.



L295 APPLICATION HINTS

The basic application circuit of the L295 is shown in figure 14. A suitable layout is given in figure 15.

Suitable values for the oscillator components, R and C, can be found from the nomogram, figure 16. The value for the reference voltages depends on the desired peak current and is equal to I_pR_s; it must be in the range 0.2V to 2V.
If the V_{ref} inputs are left open circuit the L295 assumes an internal default value of 2.5V giving a peak current of $2.5/R_s$ amperes.

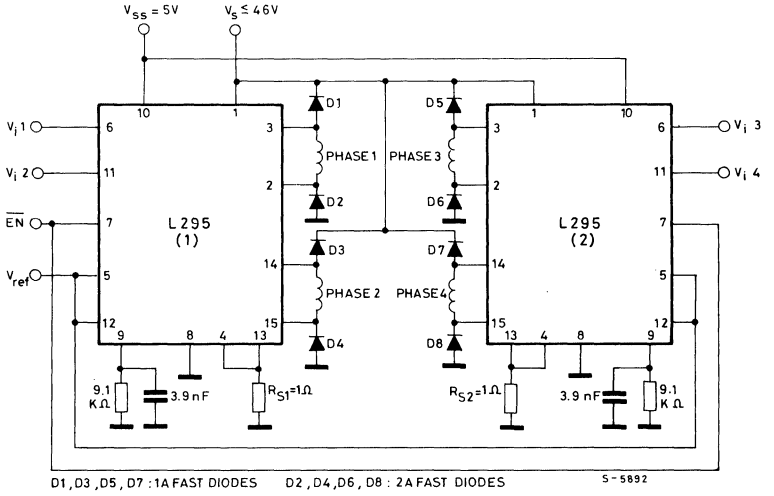
The L295 can also be used to drive unipolar stepper motors. For a four phase motor two devices are used, connected as shown in figure 17. This circuit provides switchmode regulation of the load current with a chopper rate of about 25 kHz. The enable inputs ($\overline{EN}$, connected together) enable/disable the whole circuit and the channel inputs V_{in1} . . . V_{in4} are driven by a suitable translator circuit. Phases 1 and 2 must not be energised together because they share the same sense resistor. The same applies to channels 3 and 4. However, 'two phase on' drive is still possible for bifilar motors where phases one and two represent one winding and 3 & 4 the other, and also for variable reluctance motors with phase 1 adjacent to phase 3 etc.

Two L295s could also be used to drive a bipolar stepper motor in systems where a translator already exists.

Figure 13 - Pin functions of the L295.

N°	FUNCTION
1	Solenoid supply voltage, V_s (12-46V).
2	Channel one output, source stage.
3	Channel one output, sink stage.
4	R_{S1}. Sense resistor connection, channel one.
5	V_{ref1}. A voltage on this pin sets peak current of channel one. If this pin is left open or connected to V_{ss} a default V_{ref} of 2.5V is assumed. An externally applied V_{ref} must be in the range 0.2 to 2V.
6	V_{in1}. Logic input for channel one. Driver is active when V_{in1} is high and $\overline{EN}$ low.
7	$\overline{EN}$. Chip enable (active low). When high both channels are disabled.
8	Ground.
9	Oscillator timing network. This pin is grounded to produce a single peak.
10	V_{ss}. Logic supply voltage, internally regulated. (4.75 - 10V).
11	V_{in2}. Logic input for channel two. Driver is active when V_{in2} is high and EN low.
12	V_{ref2}. Voltage input, controls peak current of channel two. If left open or connected V_s an internal 2.5V reference is assumed. An externally applied V_{ref} must be in the range 0.2 to 2V.
13	R_{S2}. Sense resistor connection, channel two.
14	Channel two output, sink stage.
15	Channel two output, source stage.

Fig. 17 - Two L295s, connected as shown, can be used to drive a four phase unipolar stepper motor.



SPEED CONTROL OF DC MOTORS WITH THE L292 SWITCH-MODE DRIVER

Power dissipation in DC motor drive systems can be reduced considerably with an L292 switchmode driver. This application guide describes two speed control systems based on this device; one voltage controlled and one controlled by a 6-bit binary word. Both examples are designed for 60W motors equipped with tacho dynamos.

The L292 is a monolithic power IC which functions effectively as a power transconductance amplifier. It delivers a load current proportional to an input voltage, handling up to 2A at 18-36V with a bridge output stage. Completely self-contained, it incorporates internal switchmode circuitry and all the active components to form a current feedback loop.

The L292 is designed primarily for use with an L290 and L291 in DC motor servopositioning applications. However, the L292 can be useful in a wide range of applications as the two examples here show. The first is a simple tachometer feedback circuit, the speed of which is controlled by a DC voltage; direction is controlled by the polarity of this voltage. The second circuit is controlled digitally and includes an L291 D/A converter.

SYSTEM WITH DC CONTROL

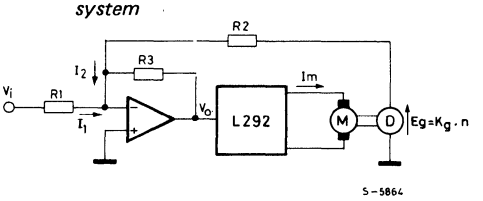
In this system the control quantity is a dc voltage variable between

$$+ V_{iM} \text{ and } - V_{iM}$$

Since the quantity under control is the speed of the motor, it is required that it varies linearly in function of the control voltage.
A simplified circuit diagram of the system is shown in fig. 1.

The current I_1, proportional to the set voltage V_i, and the current I_2, proportional to the speed of the motor, are fed to the sum point of the error amplifier. Assuming that the motor does not drain current, the system is in a steady-state condition whenever $I_1 = -I_2$; as a matter of fact, in this case the output from the error emplifier V_o is OV. During transients, the voltage V_o will assume a value $V_o = - R3 (I_1 + I_2)$ and consequently, since the L292 integrated circuit operates as a transconductance (G_m), a mean current $I_m = G_m \cdot V_o$ will flow in the motor determining an acceleration proportional to it.

Fig. 1 - Simplified circuit diagram of DC control system



Calculation of R1, R2, R3

Let us call:

V_{iM} the maximum control voltage value
n_M the maximum speed allowed for the motor
K_g voltage constant of the dynamo

By imposing that the balance condition be met in correspondance to the maximum rotation speed the following equation is obtained:

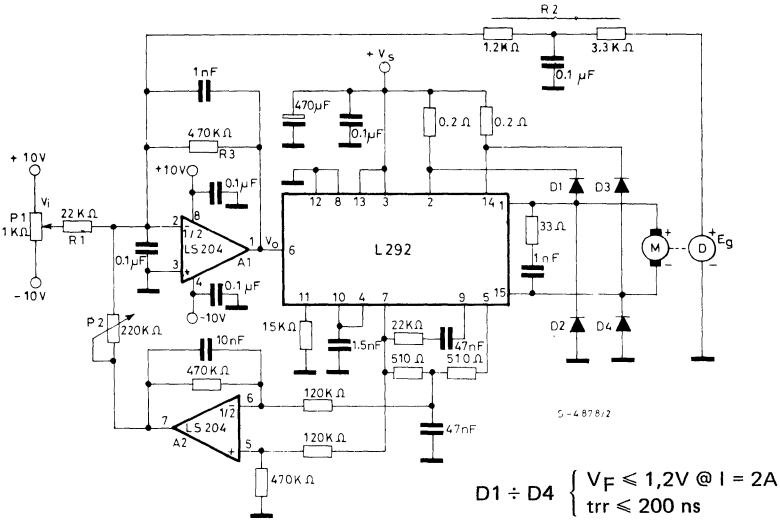
$$I_1 = - I_2 ; \quad \frac{V_{iM}}{R1} = - \frac{K_g \cdot n_M}{R2}$$

Since R2 is the impedance which the tachometer dynamo is loaded on to and its value is recommended by the manufacturer, it is possible from the previous relationship to determine the value of R1.
Resistor R3 determines the system gain. It's best to keep the gain as high as possible (and consequently R3 as high as possible) to obtain a high response speed of the system, even for small variations in the control voltage. On the other hand, an excessive gain would cause excessive overshoot around the balance conditions at the end of transients. Consequently, a trade-off must be made between the two opposing requirements in select-

In this case too, the variation Δ n is as much lower as the error amplifier gain is higher. With the circuit shown in fig. 2 Δ n is approximately 30 turns/min. with Δ I = 800 mA, Δ n = 0.037 turns/mA.min approx.

It is possible to adopt a circuit which prevents the variation in the number of turns in function of motor current. The problem is to "sense" the current flowing through the motor and to send a current proportional to it to the sum point of the error amplifier. The complete circuit which includes, beside the voltage feed-back loop, also a current feed-back loop, is illustrated in fig. 4.

Fig. 4 - Complete circuit with current feedback

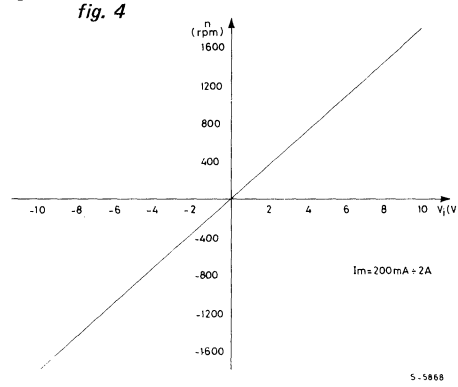


In the integrated circuit L292, a current proportional to the mean current drained by the motor flows between pin 5 and pin 7.
An operational amplifier amplifies the voltage drop provoked by this current across a 510 Ω resistor and sends a current to the sum point which is consequently proportional to the mean current in the motor, the value of which can be made vary by acting on potentiometer P2. By properly adjusting P2, a condition can be achieved in which the speed does not change when the current drained by the motor varies.

The discontinuity around the origin, which was present in the previous circuit (fig. 2), is practically negligible in the circuit shown in fig. 4.

The characteristic n = f (V_i) relevant to the circuit of fig. 4 is shown in fig. 5, and this characteristic does not substantially change over the whole range of currents allowed by the L292 (up to 2A).
In the circuit described above if the motor stall condition is requested. it is preferable to act on the inhibits of the integrated circuit L292, for instance by grounding pin 13, instead of adjusting potentiometer P1: as a matter of fact, the exact position of this potentiometer is difficult to obtain, since the characteristic crosses the axis V_i in one only point (this means that n is only 0 for a very narrow interval of V_i).

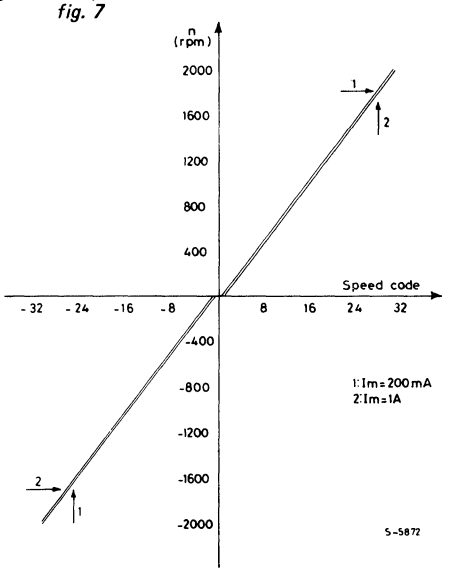
Fig. 5 - Output characteristic of the circuit in fig. 4



SYSTEM WITH DIGITAL CONTROL

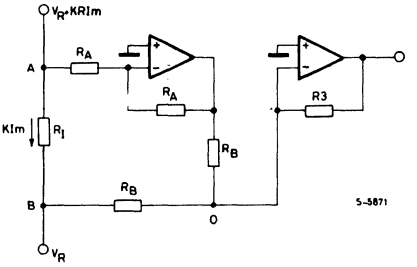
In this system the speed information is given to the circuit by a binary code made up of 5 information bits plus one sign bit, which determines whether the movement shall be clockwise or counter-clockwise. For the circuit implementation, the integrated circuits L291 (which includes a D/A converter and two operational amplifiers) and L292 are used.
A simplified circuit diagram is shown in fig. 6.

Fig. 8 - Output characteristic of the circuit in fig. 7



prevent that the speed vary in function of the motor load, by adding a current loop in the control circuit, by using the remaining operational amplifier available in the integrated circuit L291.
Since this amplifier has only the inverting input available, while the non-inverting input is grounded, a circuit arrangement as schematically shown in fig. 9 has been adopted in order to have an output signal referred to ground, given an input signal referred to a reference voltage (in L292) of approximately 8V.

Fig. 9 - Translator circuit

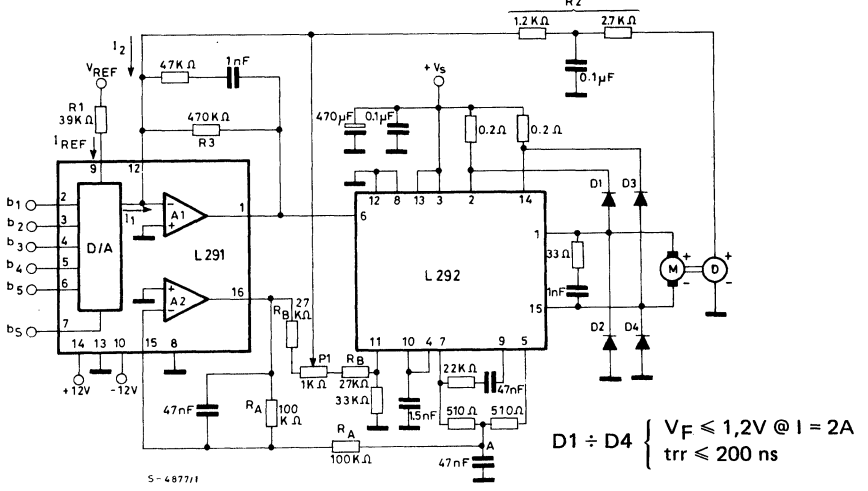


Resistors R_A and R_B must be high-precision resistors in order to have output 0 with no I_m current present. In the practical implementation, resistors with an accuracy of 5% are used and the ends of a potentiometer are interposed between resistors R_B and the output to the sum point of the error amplifier is made through the cursor. The gain of this current loop is proportional to the ratio $R3/R_B$. A complete circuit diagram is shown in fig. 10.

Since, for reasons of gain, resistor R_B must be 27 kΩ and, if connected to pin 7 of L292, should have subtracted too much current by thus affecting the correct operation of L292, it has been connected to pin 11, having the same potential as pin 7. Consequently, the resistance value between pin 11 and ground has been modified, in order to maintain the switching frequency of L292 unchanged. In order to have a correct adjustment of potentiometer P1, it is enough to set the 0 speed code (b_1 through b_5 high) and turn the cursor until the motor stops.

The input versus output characteristic obtained with the circuit of fig. 10 is indicated in fig. 11.

Fig. 10 - Complete circuit with current feedback

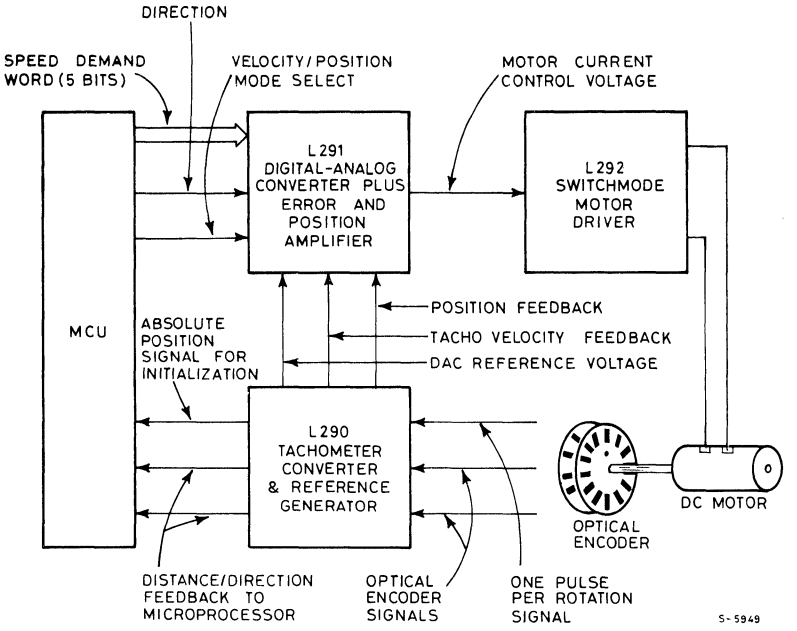


A DESIGNER'S GUIDE TO THE L290/L291/L292 DC MOTOR SPEED/POSITION CONTROL SYSTEM

The L290, L291 and L292 together form a complete microprocessor-controlled DC motor servopositioning system that is both fast and accurate. This design guide presents a description of the system, detailed function descriptions of each device and application information.

The L290, L291 and L292 are primarily intended for use with a DC motor and optical encoder in the configuration shown schematically in figure 1. This system is controlled by a microprocessor, or microcomputer, which determines the optimum speed profile for each movement and passes appropriate commands to the L291, which contains the system's D/A converter and error amplifiers. The L291 generates a voltage control signal to drive the L292 switchmode driver which powers the motor. An optical encoder on the motor shaft provides signals which are processed by the L290 tachometer converter to produce tacho voltage feedback and position feedback signals for the L291 plus distance/direction feedback signals for the control micro.

Fig. 1 - The L290, L291 and L292 form a complete DC motor servopositioning system that connects directly to microcomputer chips.



THE L290 TACHOMETER CONVERTER

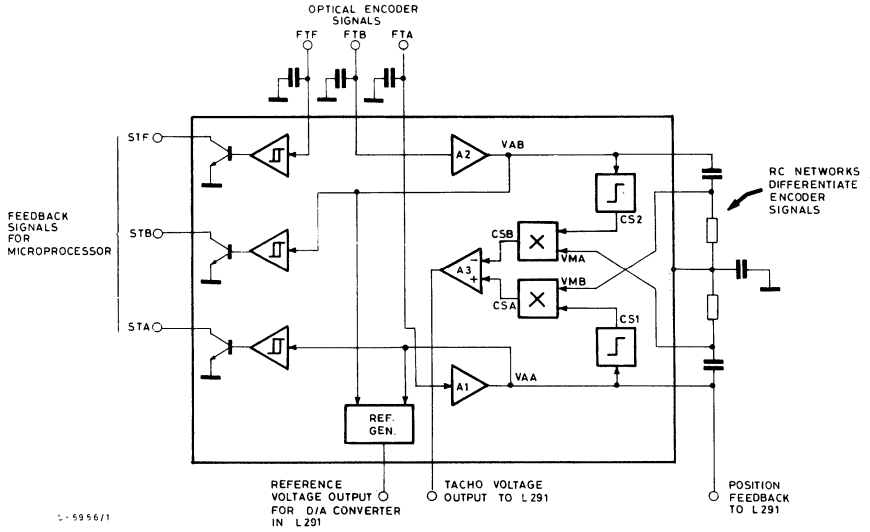
The L290 tachometer converter processes the three optical encoder signals FTA, FTB, FTF to generate a tachometer voltage, a position signal and feedback signals for the microprocessor. It also generates a reference voltage for the system's D/A converter.

Analytically, the tacho generation function can be expressed as:

$$\text{TACHO} = \frac{dV_{AB}}{dt} \cdot \frac{FTA}{|FTA|} - \frac{dV_{AA}}{dt} \cdot \frac{FTB}{|FTB|}$$

In the L290 (block diagram, figure 4) this function is implemented by amplifying FTA and FTB in A1 and A2 to produce V_{AA} and V_{AB}. V_{AA} and V_{AB} are differentiated by external RC networks to give the signals V_{MA} and V_{MB} which are phase

Fig. 4 - The L290 processes the encoder signals, generating a tacho voltage and position signal for the L291 plus feedback signals for the microprocessor. Additionally, it generates a refence voltage for the L291's D/A converter.



shifted and proportional in amplitude to the speed of rotation. V_{MA} and V_{MB} are passed to multipliers, the second inputs of which are the sign of the **other** signal before differentiation.

The sign ($\frac{FTA}{|FTA|}$ or $\frac{FTB}{|FTB|}$) is provided by the comparators CS1 and CS2. Finally, the multiplier outputs are summed by A3 to give the tacho signal. Figure 5 shows the waveforms for this process.

This seemingly complex approach has three important advantages. First, since the peaks and nulls of CSA and CSB tend to cancel out, the ripple is very small. Secondly, the ripple frequency is the fourth harmonic of the fundamental so it can be filtered easily without limiting the bandwidth of the speed loop. Finally, it is possible to acquire tacho information much more rapidly, giving a good response time and transient response.

Feedback signals for the microprocessor, STA, STB and STF, are generated by squaring FTA, FTB and FTF. STA and STB are used by the micro to keep track of position and STF is used at initialization to find the absolute position.

Position feedback for the L291 is obtained simply from the output of A1.

Fig. 5 - These waveforms illustrate the generation of the tacho voltage in the L290. Note that the ripple is fourth harmonic. The amplitude of TACHO is proportional to the speed of rotation.

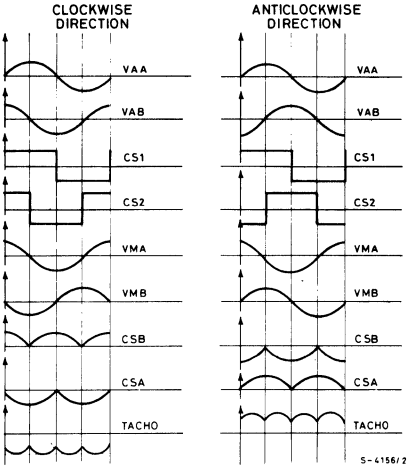
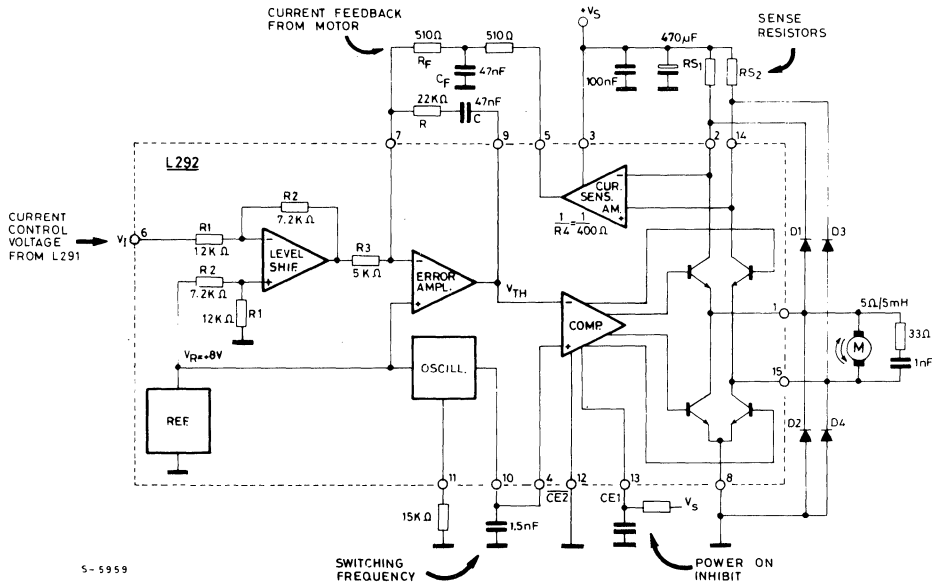


Fig. 7 - The L292 switchmode driver receives a control voltage from the L291 and delivers a switchmode regulated current to the motor.



The L292 incorporates its own voltage reference and all the functions required for closed loop current control of the motor. Further, it features two enable inputs, one of which is useful to implement a power on inhibit function.

The L292's output stage is a bridge configuration capable of handling up to 2A at 36V. A full bridge stage was chosen because it allows a supply voltage to the motor effectively twice the voltage allowed if a half bridge is used. A single supply was chosen to avoid problems associated with pump-back energy.

In a double supply configuration, such as the example in figure 8a, current flows for most of the time through D1 and Q1. A certain amount of power is thus taken from one supply and pumped back into the other. Capacitor C1 is charged and its voltage can rise excessively, risking damage to the associated electronics.

By contrast, in a single supply configuration like figure 8b the single supply capacitor participates in both the conduction and recirculation phases. The average current is such that power is always taken from the supply and the problem of an uncontrolled increase in capacitor voltage does not arise.

Fig. 8 - A simple push pull output (a) needs a split supply and the device can be damaged by the voltage built up on C1. The L292 has a bridge output to avoid these problems. Only one supply is needed and the voltage across the single capacitor never rises excessively. Moreover, the motor can be supplied with a voltage up to twice the voltage allowed with a half bridge.

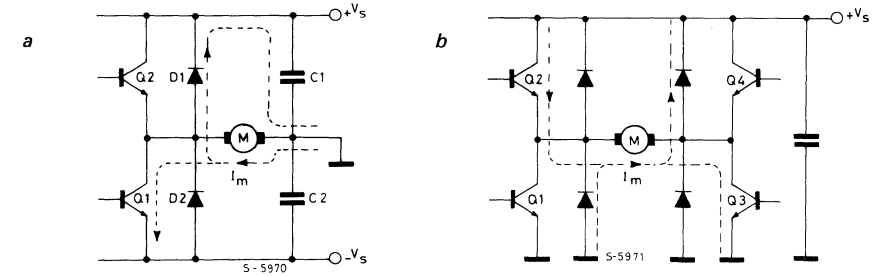


Fig. 12 - Complete application circuit of the system.

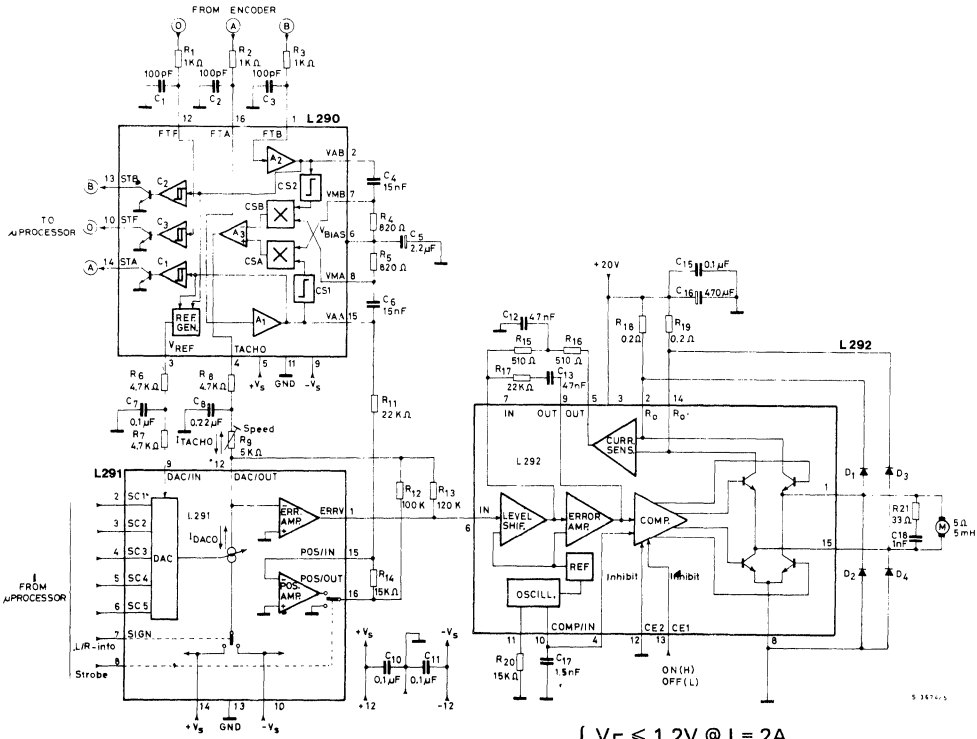
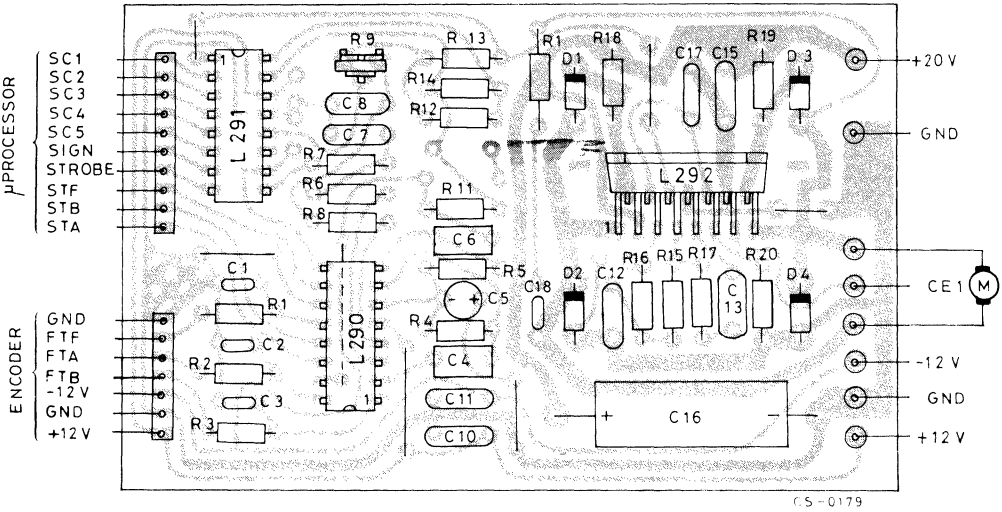


Fig. 13 - P.C. board and component layout (1:1 scale)



When the system is powered up the mechanical subsystem may be in any position so the first step is to initialize it. In applications where the optical encoder never rotates more than one revolution – the daisy wheel of a typewriter, for example – this is simply done by rotating the motor slowly until the STF signal (one-pulse-per-rotation) is detected.

Where the optical encoder rotates more than once the 'one-pulse-per-rotation' signal is not sufficient. An example of this is the carriage positioning servo of a computer printer. In this case the simplest solution is to fit a microswitch on one of the endstops. First the motor is run backwards slowly until the carriage hits the endstop. Then it moves forward until the STF signal is detected. The beauty of this solution is that the endstop microswitch does not need to be positioned accurately.

APPLICATION CIRCUITS

The complete circuit is shown in figure 12; a suitable layout for evaluation is given in figure 13. Component values indicated are for a typical system using a Sensor Technology STRE1601 encoder and a motor with a winding resistance of 5Ω and an inductance of 5 mH (this motor is described fully in figure 17). How to calculate values for other motors is explained further on.

Figure14 explains what each component does and what happens if it is varied. Maximum and minimum values are also indicated where appropriate.

ADDING DISCRETE TRANSISTORS FOR HIGHER POWER

In the basic application, the L292 driver delivers 2A to the motor at 36V. This is fairly impressive for an integrated circuit but not enough for some applications – robots, machine tools etc. The basic system can be expanded to accomodate these applications by adding external power transistors to the L292. This is preferable to simply adding a discrete driver stage in place of the L292 because the L292's current control loop is very useful.

Figure 15 shows how four transistors are added to increase the current to 4, 6 or 8A, depending on the choice of transistor. When coupled to the L290 and L291 this configuration appears to the system as an L292.

The average motor current, I_m, is found from:

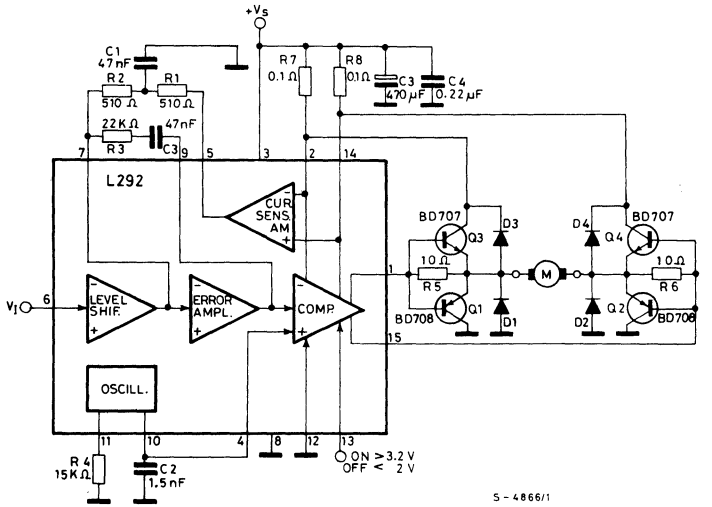
$$I_m = \frac{V_i \ 0.044}{R_x}$$

where V_i is the input voltage and R_x is the value of the sense resistors R7 and R8.

Suitable transistors for this configuration are indicated below:

I (A)	V_i(V)	R_x(mΩ)	Q1, Q2	Q3, Q4	D1 – D4
4	9.1	100	BD708	BD707	2A Fast diodes
6	9.1	65	BD908	BD907	3A Fast diodes
8	9.1	50	BDW52A	BDW51A	4A Fast diodes

Fig. 15 - For higher power external transistors are added to the L292. This circuit delivers up to 4A, if 2 BDW51A and 2 BDW52A are used it can deliver 8A.



DESIGN CONSIDERATIONS

The application circuit of figure 12 will have to be adapted in most cases to suit the desired performance, motor characteristics, mechanical system characteristics and encoder characteristics. Essentially this adaptation consists of choosing appropriate values for the ten or so components that determine the characteristics of the L290, L291 and L292.

The calculations include:

- Calculation of maximum speed and acceleration; useful both for defining the control algorithm and setting the maximum speed.
- Calculation of R8 and R9 to set maximum speed.
- Laplace analysis of system to set C8, R11, R12, R13 and R14.
- Laplace analysis of L292 loop to set the sensing resistors and C12, C13, R15, R16, R17.
- Calculation of values for C4 and C6 to set max level of tacho signal.
- Calculation of values for R6 and R7 to set D/A reference current.
- Calculation of R20 to set desired switching frequency.

MAXIMUM ACCELERATION

For a permanent magnet DC motor the acceleration torque is related to the motor current by the expression:

$$T_a + T_f = K_T \; I_m$$

where:

I_m is the motor current
K_T is the motor torque constant
T_a is the acceleration torque
T_f is the total system friction torque

The acceleration torque is related to angular acceleration and system inertia by:

$$T_a = (J_m + J_{oe} + J_L)\; a$$

where:

J_m is the moment of inertia of the motor
J_{oe} is the moment of inertia of the encoder
J_L is the moment of inertia of the load
a is the angular acceleration.

In a system of this type the friction torque T_f is normally very small and can be neglected. Therefore, combing these two expressions we can find the angular acceleration from:

$$a = \frac{K_T}{J_m + J_{oe} + J_L} \cdot I_m$$

It follows that for a given motor type and control loop the acceleration can only be increased by increasing the motor current, I_m.

The characteristics of a typical motor are given in figure 17. From this table we can see that:

$K_T = 4.3$ N cm/A (6.07 oz.in/A)

$J_m = 65$ g · cm^2 (0.92×10^{-3} oz.in.s^2)

We also know that the maximum current supplied by the L292 is 2A and that the moment of inertia of the STRE1601 optical encoder, J_{oe}, is 0.3×10^{-4} oz.in.s^2.

The moment of inertia of the load J_L, is unknown but assume, for example, that $J_{oe} + J_L \cong 2\, J_m$. Therefore the maximum angular acceleration is:

$$a = \frac{6.07 \times 2}{2 \times 0.92 \times 10^{-3}} = 6597.8 \text{ rad/s}^2$$

Fig. 17 - The characteristics of a typical DC motor.

Motor - Parameter	Value
U_{BB} (V_s)	18V
C. emf. K_E	4.5 mV/min^{-1}
N_o (without load)	3800 rpm
I_{om} (without load)	190 mA
T_f (friction torque)	0.7 N cm
K_T (motor constant)	4.3 N cm/A
Amature moment of inertia	65 g. cm^2
R_M of the motor	5.4 Ω
L_M of the motor	5.5 mH

MAXIMUM SPEED

The maximum speed can be found from:

$$V_{S\ min} = 2\, V_{CEsat} + R_S\, I_m + K_e\, \Omega + R_m\, I_m$$

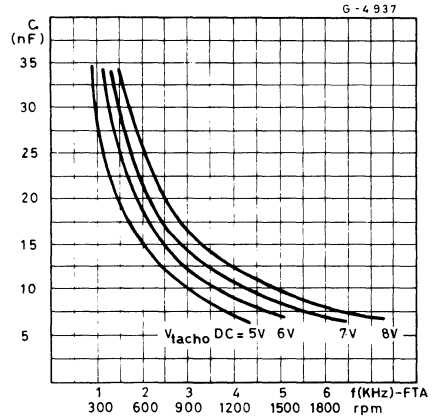
where:

E = $K_e\, \Omega$ is the internally generated voltage (EMF)
K_e is the motor voltage constant
Ω is the rotation speed of the motor.

For example, if $V_{s\ min} = 20$V
$2\, V_{CEsat} + R_s\, I_m = 5$V (from L292 datasheet)
$R_m\, I_m = 10.8$V ($R_m = 5.4\ \Omega$)
we obtain:

$$K_e\, \Omega\ (E) = 4.2\text{V}$$

Fig. 18 - C4 and C6 value versus rotation speed for various maximum tacho voltage values.



LAPLACE ANALYSIS OF THE SYSTEM

Suitable values for the components R11,R12,R13, R14 and C8 can be found from a Laplace analysis of the system. Figure 19 shows a simplified block diagram of the system which will be useful for the analysis.

The analysis is based on the angular speed Ω and on the motor position θ. The motor is represented, to a first approximation, by the current I_m and by the acceleration torque, T_a, which drives an inertial load J.

There are two conversion factors, K_{sp} and $K\theta$. They link the mechanical parameters (position and speed) with the equivalent feedback signals for the two loops. The values of K_{sp} and $K\theta$ are determined by the encoder characteristics and the gain parameters of the integrated circuits. The open-loop and closed-loop gains are fixed by four external resistors:

- R_{ref} – fixes the reference current (R6 + R7)
- R_{speed} – fixes the speed loop gain (R8 + R9)
- R_{pos} – controls the position loop gain (R12)
- R_{err} – controls the system loop gain (R13).

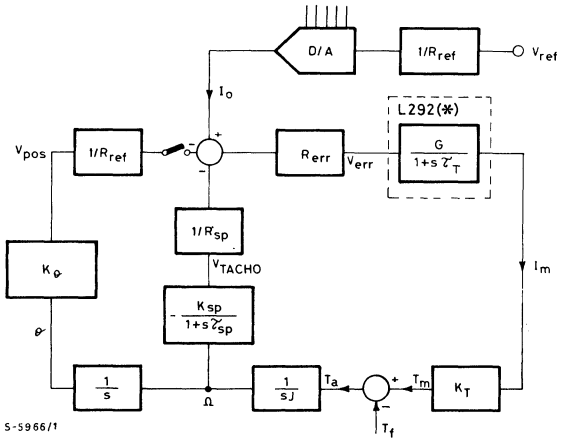
The stability both of the speed loop and of the speed-position loop are defined by external components.

The fundamental characteristics of the speed control system can thus be determined by the designer.

τ_{sp} is the time constant that determines the dominant pole of the speed loop and is determined by C8, R8 and R9

$$\tau_{sp} = C8 \frac{R8\ R9}{R8 + R9}.$$

Fig. 19



(*) See L292 datasheet for an accurate analysis of this block.

List of terms

s : Laplace variable
K_T : Motor torque constant
T_a : Acceleration torque
T_f : Total system friction torque
J : Total moment of inertia ($J = J_{oe} + J_m + J_L$).
Ω : Speed
θ : Angular position
K_{sp} : Conversion factor that links the motor rotation speed and the TACHO signal.
K_T : Conversion factor that links the motor position and the V_{pos} signal.

and $$\Delta I_m = 0.1\ I_{m\ max}$$

$$\Rightarrow 0.1\ I_{m\ max} = \frac{V_s}{2f\ L_{M\ min}}$$

$$\Rightarrow L_{M\ min} = \frac{5\ V_s}{f\ I_{m\ max}}$$

Therefore there is a minimum inductance for the motor which may not always be satisfied. If this is the case, a series inductor should be added and the value is found from:

$$L_{series} = \frac{5\ V_s}{f\ I_{m\ max}} - L_M$$

EFFICIENCY AND POWER DISSIPATION

Neglecting the losses due to switching times and the dissipation due to the motor current, the efficiency of the L292's bridge can be found from:

$$\eta = 1 - \frac{\Delta t1}{\Delta t1 - \Delta t2} \cdot \frac{V_{sat}}{V_s} - \frac{\Delta t1}{\Delta t1 - \Delta t2} \cdot \frac{V_{over}}{V_s}$$

where:

$V_{over} \cong 2V\ (2\ V_{BE} + R_S\ I_m)$

$V_{sat} \cong 4V\ (2\ V_{CEsat} + 3\ V_{BE})$

$\Delta t1$ = transistor conduction period

$\Delta t2$ = diode conduction period.

If $\Delta t1 \gg \Delta t2$ and V_s = 20V we obtain:

$$\eta = 1 - \frac{4}{20} = 80\%$$

In practice the efficiency will be slightly lower as a results of dissipation in the signal processing circuit (about 1W at 20V) and the finite switching times (about 1W).

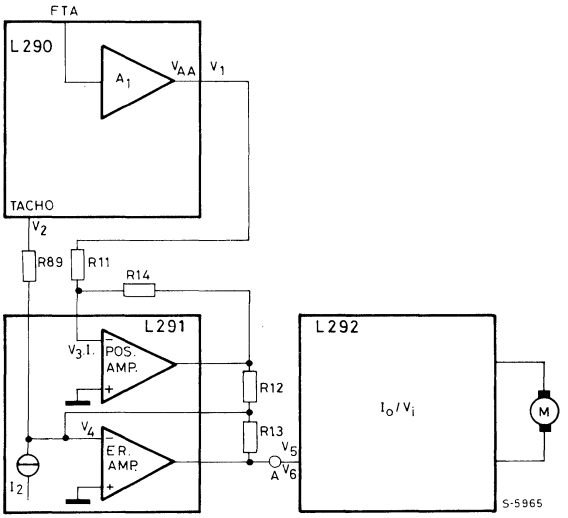
If the power transferred to the motor is 40W, the 80% efficiency implies 10W dissipated in the bridge and a total dissipation of 12W. This gives an actual efficiency of 77%. Since the L292's Multiwatt package can dissipate up to 20W it is possible to handle continuous powers in excess of 60W.

POSITION ACCURACY

The main feature of the system L290, L291, L292 is the accurate positioning of the motor. In this section we will analyse the influence of the offsets of the three ICs on the positioning precision.

When the system is working in position mode, the signal FTA coming from the optical encoder, after suitable amplification, is sent to the summing point of the error amplifier (L291). If there were no offset and no friction, the motor would stop in a position corresponding to the zero crossing of the signal FTA, and then at the exact position required. With a real system the motor stops in a position where FTA has such a value to compensate the offsets and the friction; as a consequence there is a certain imprecision in the positioning. The block diagram, fig. 20, shows the parts of the 3 ICs involved in the offsets. First we will calculate the amount of the offsets at the input of the IC L292 (point A of fig. 20).

Fig. 20



$$V_{5A} = 350\ mV$$

$$V_{6A} = \frac{50}{205} = 244\ mV$$

$$V_A = 2.346V$$

$$V_{FTA} = 2.329 \cdot \frac{100}{120} \cdot \frac{22}{15} \cdot \frac{1}{12.6} = 0.228V$$

$$\alpha = \sin^{-1} \frac{0.226}{0.4} \cong 35°$$

If we consider an optical encoder with 200 tracks/turn and a daisy wheel with 100 characters, the phase between two consecutive characters is $\alpha_c = 720°$, and then the maximum percentage error we can have is.

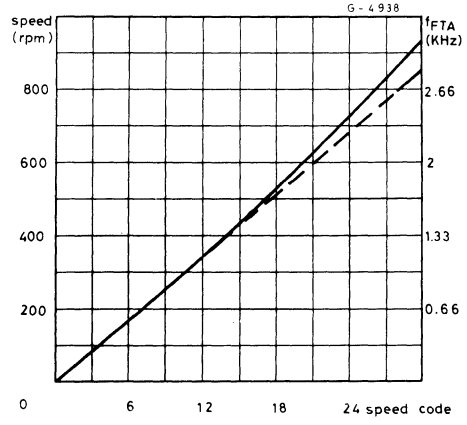
$$\epsilon = \frac{35}{720} \cdot 100 \cong 4.8\%$$

From this numerical example we can see that the main contribution to the positioning error is given by the offset of the TACHO signal (V_{2A}), other big contributions are given by the input offset voltage of L292 (V_{5A}) and by the voltage necessary to compensate the dynamic friction of the motor (V_{6A}). This last term is only determined by the motor and can also have greater values.

The error we have calculated is the maximum possible and it happens when all the offsets have the max value with the same sign, i.e. with a probability given by the product of the single probabilities. Considering as an example every offset has a probability of 1% to assume the max value, the probability the error assumes the max value is:

$$P = (10^{-2})^7 = 10^{-14}$$

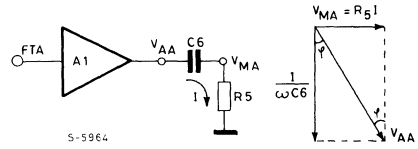
Fig. 21



SPEED ACCURACY

If we consider the complete system with L290-L291-L292 driving a DC MOTOR with optical encoder, we can note the speed of the motor is not a linear function of the speed digital code applied to L291. The diagram of fig. 21 shows this function and it is evident that the speed increases more than a linear function, i.e. if the speed code doubles, the speed of the motor becomes more than the double. The cause of this non linearity is the differentiator network R4 C4 and R5 C6 (see fig. 22) that has not an ideal behaviour at every frequency.

Fig. 22



1) $V_{MA} = V_{AA} \sin \varphi$

$\varphi = tg^{-1}\ \omega\ R5\ C6$ $\qquad \omega = 2\pi f$

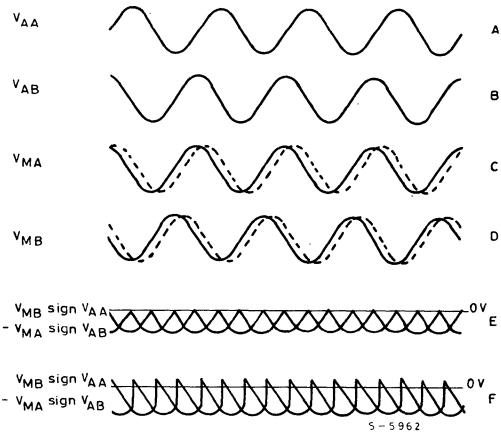
2) $V_{MA} = V_{AA} \sin tg^{-1}\ \omega\ R5\ C6$

f = frequency of the signal FTA

This last relation gives the amplitude of the signal V_{MA}; it is evident there is not a linear function between V_{MA} and ω, like $V_{MA} = K\omega$ and the difference is greater if the product ω R5 C6 doesn't respect the disequation ω R5 C6 $\ll 1$. , i.e. at high frequencies.

The phase angle between V_{MA} and V_{AA} should be 90° and then $\varphi = 0$, in our case φ increases with the frequency according to the equation $\varphi = tg^{-1}\ \omega$ R5C6, and influences the amplitude of the output signal TACHO. In fig. 23 are shown the waveforms that contribute to generate the TACHO signal. A and B are the signals V_{AA} and V_{AB} in phase with the input signals FTA and FTB. C and

Fig. 23



With the guaranteed values on the L291 data sheet we can calculate for $\epsilon 4$ the max value:

$$\epsilon 4 = \frac{21\ \mu A}{1.4\ mA} \cdot 100 = 1.5\%$$

Another characteristic of a D/AC is the linearity, that in our case is better than ± 1/2 LSB. This value is sufficient to guarantee the monotonicity of I_O, and then of the speed of the motor, as a function of the input digital code. The precision of ± 1/2 LSB implies a spread of the speed at every configuration of the input code of ± 1.61% referred to the maximum speed. The max percentage error we can have is then greater at low level speed (± 50% at min speed) and has its minimum value at the maximum speed (1.61%).

ACCURACY DUE TO THE ENCODER

The amplitude of the signals FTA and FTB determines the value of the TACHO signal. This amplitude must be constant on the whole range of the frequency, otherwise it is not possible to have a linear function between the TACHO signal and the frequency. The spread of the amplitudes of the two signals FTA and FTB between several encoder can be compensated by adjusting the potentiometer R9 (see fig. 12). The phase between the two signals should be 90°. If there is a constant difference from this value, a constant factor reduction of the TACHO signal results that can be compensated with the potentiometer R9. If the difference from 90° is random, also the reduction of the TACHO signal is random in the same way, and by means of R9 it is possible to compensate only the mean value of that reduction.

DESIGNING WITH THE L296 MONOLITHIC POWER SWITCHING REGULATOR

A cost-effective replacement for costly hybrids, the SGS L296 Power Switching Regulator delivers 4A at an output voltage of 5.1V to 40V and includes many popular supply features. This comprehensive application guide explains how the device operates and how it is used. Typical application circuits are also presented.

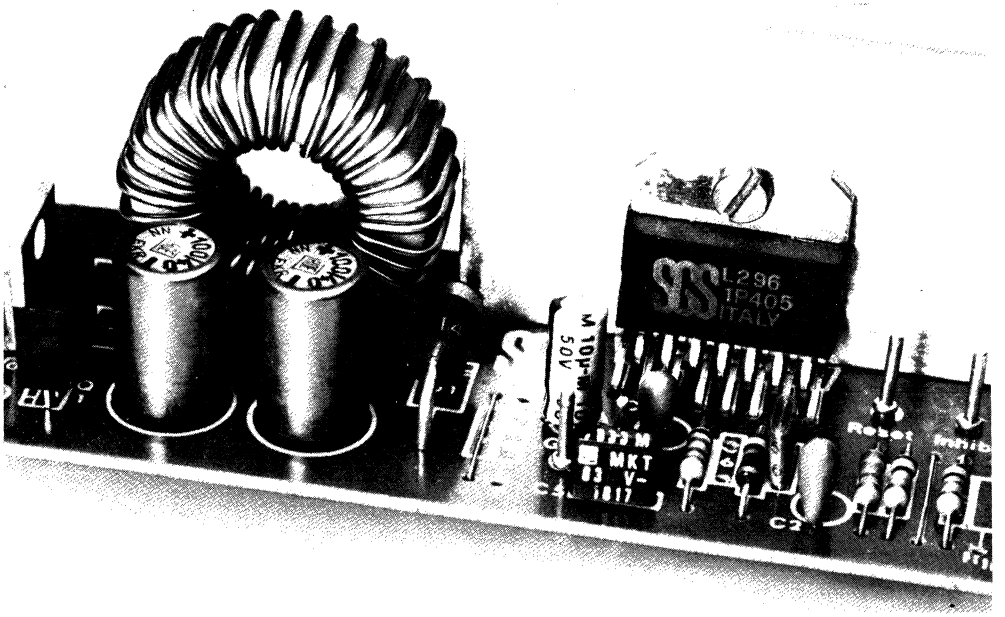
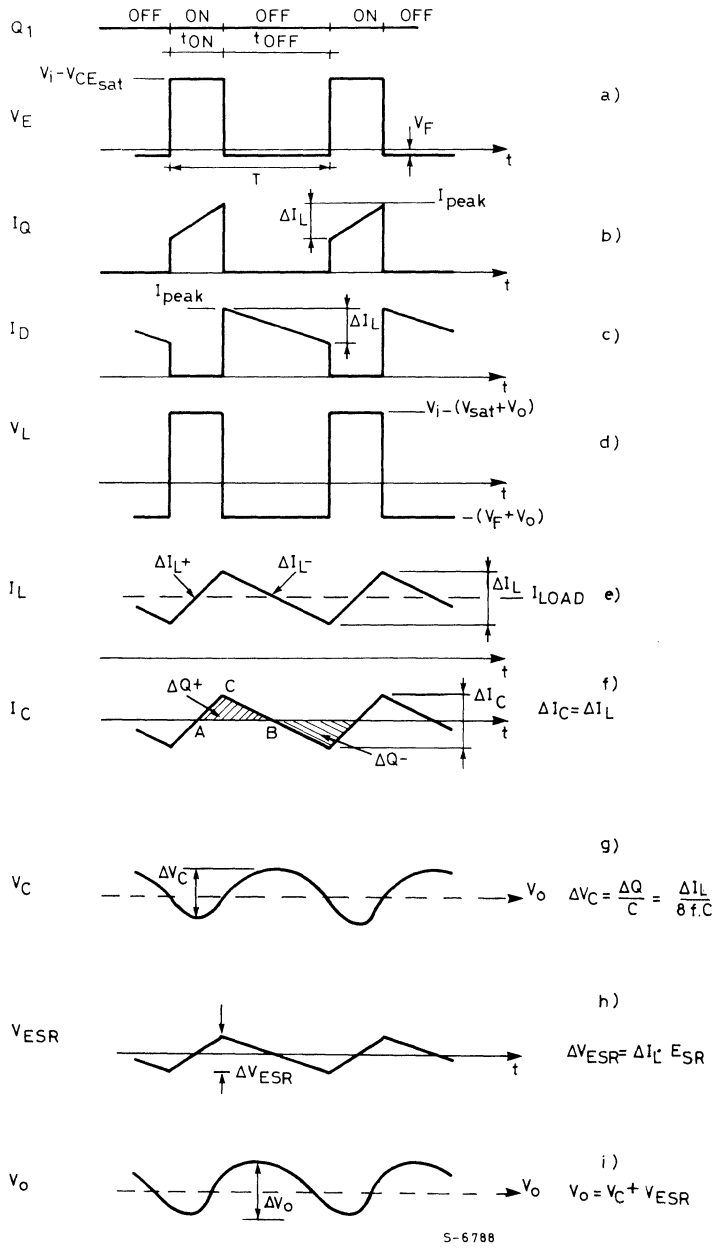


Fig. 2 — Principal circuit waveforms of the fig. 1 circuit.



where:

$$v_C = V_o$$

$$\frac{di_L}{dt} = -(V_F + V_o)/L \qquad (6)$$

It follows therefore that:

$$i_L(t) = -\frac{V_F + V_o}{L} t \qquad (7)$$

The negative sign may be interpretated with the fact that the current is now decreasing. Assuming that V_F may be neglected against V_o, during the OFF time the following behaviour occurs:

$$I_L = \frac{V_o}{L} t \qquad (8)$$

therefore:

$$\Delta I_L^- = \frac{V_o}{L} T_{OFF} \qquad (9)$$

But, because

$\Delta I_L^+ = \Delta I_L^-$ if follows that:

$$\frac{(V_i - V_o)\ T_{ON}}{L} = \frac{V_o\ T_{OFF}}{L}$$

which allows us to calculate V_o:

$$V_o = V_i \frac{T_{ON}}{T_{ON} + T_{OFF}} = V_i \frac{T_{ON}}{T} \qquad (10)$$

where T is the switching period.

Expression (10) links the output voltage V_o to the input voltage V_i and to the duty cycle. The relationship between the currents is the following:

$$I_{iDC} = I_{oDC} \cdot \frac{T_{ON}}{T}$$

EFFICIENCY

The system efficiency is expressed by the following formula:

$$\eta\% = \frac{P_o}{P_i} 100$$

where $P_o = V_o I_o$ (with $I_o = I_{LOAD}$)

is the output power to the load and P_i is the input power absorbed by the system. P_i is given by P_o, plus all the other system losses. The expression of the efficiency becomes therefore the following:

$$\eta = \frac{P_o}{P_o + P_{sat} + P_D + P_L + P_q + p_{sw}} \qquad (12)$$

DC LOSSES

P_{sat}: saturation losses of the power transistor Q. These losses increase as V_i decreases.

$$P_{sat} = V_{sat} \cdot I_o \frac{T_{ON}}{T} = V_{sat}\ I_o \frac{V_o}{V_i} \qquad (13)$$

where $\frac{T_{ON}}{T} = \frac{V_o}{V_i}$ and V_{sat} is the power transistor saturation at current I_o.

P_D: losses due to the recirculation diode. These losses increase as V_i increases, as in this case the ON time of the diode is greater.

$$P_D = V_F\ I_o \frac{V_i - V_o}{V_i} = V_F\ I_o\ (1 - \frac{V_o}{V_i}) \qquad (14)$$

where V_F is the forward voltage of the recirculation diode at current I_o.

P_L: losses due to the series resistance R_S of the coil

$$P_L = R_S\ I_o^2 \qquad (15)$$

P_q: losses due to the stand-by current and to the power driving current:

$$P_q = V_i\ I'_{3q} + V_i\ I''_{3q} \frac{T_{ON}}{T} \qquad (16)$$

where being:

$\frac{T_{ON}}{T} = \frac{V_o}{V_i}$ it follows that:

$P_q = V_i\ I'_{3q} + V_o\ I''_{3q}$ in which:

$I'_{3q} = I_{3q}$ at 0% duty cycle

$I''_{3q} = I_{3q\,(100\%\,d.c.)} - I_{3q\,(0\%\,d.c.)}$

SWITCHING LOSSES

p_{sw}: switching losses of the power transistor:

$$p_{sw} = V_i\ I_o \frac{t_r + t_f}{2T}$$

The switching losses of the recirculation diode are

Calculating dv_c and equalizing it to ΔV_o, it follows that:

$$\Delta V_o = \frac{L \Delta I_o^2}{C(V_i - V_o)} \qquad (24) \quad \text{for} + \Delta I_o$$

$$\Delta V_o = \frac{L \Delta I_o^2}{C V_o} \qquad (25) \quad \text{for} - \Delta I_o$$

From these two expressions the dependence of overshoots and undershoots on the L and C values may be observed. To minimize ΔV_o it is therefore necessary to reduce the inductance value L and to increase the capacitance value C. Should other auxiliary functions be required in the circuit like reset or crowbar protections and very variable loads may be present, it is worthwhile to take special care for minimizing these overshoots, which could cause spurious operation of the crowbar, and the undershoot, which could trigger the reset function.

DEVICE DESCRIPTION

Fig. 4 shows the package in which the device is mounted and the pin function assignments.
The internal structure of the device is shown in fig. 5. Each block will now be examined.

Power supply

The device is provided with an internal stabilized power supply that, besides supplying the reference voltage of 5.1V for the whole system, also supplied the internal analog blocks.
Special features of the voltage reference are its accuracy, temperature stability and high line rejection. Through zener-zap trimming, the voltage is within ± 2% limits.

Fig. 4 – Pin assignments of the L296.

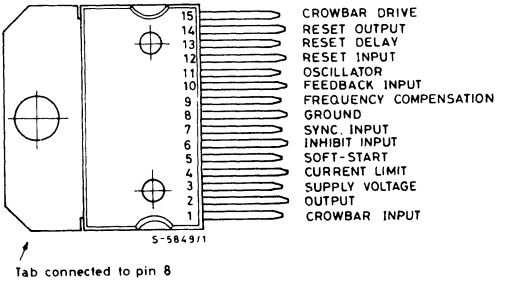
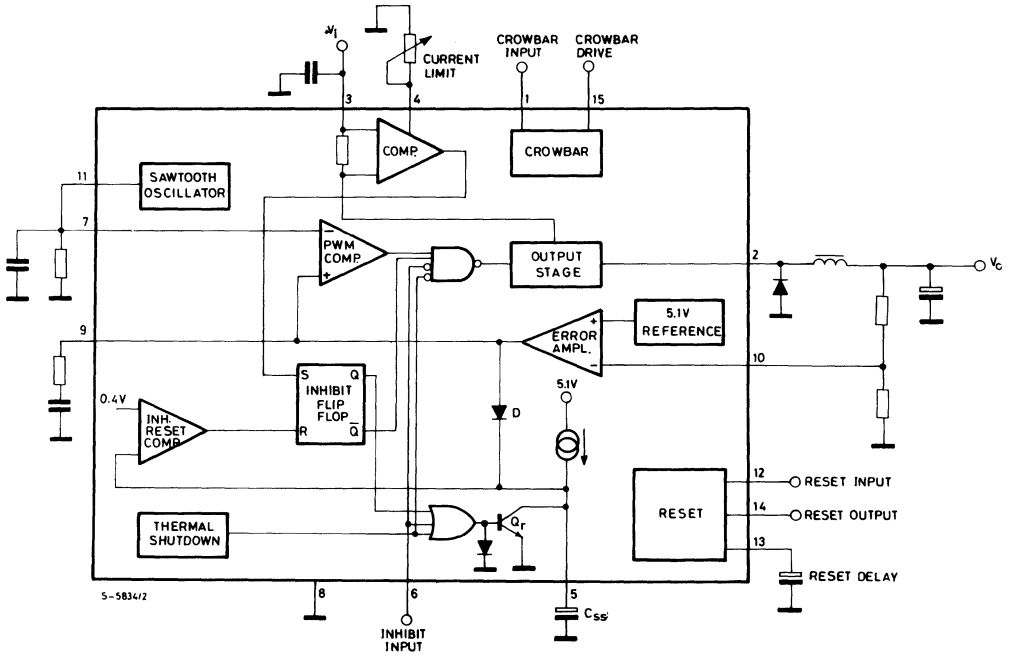


Fig. 5 – Block diagram of the L296. In addition to the basic regulation loop the device includes functions such as reset, crowbar and current limiting.



due to the switching delays of the comparator. This inaccuracy in caused by an excessively short rise time of the voltage. A capacitance value too high gives rise to a charging time which is too long compared to the discharging time. An additional inaccuracy cause would be therefore present for the switching frequency, now due to spread of the charge current.

The oscillation frequency is given by the following formula:

$$f_{osc} = \frac{1}{R_{osc}\ C_{osc}} \qquad (26)$$

PWM (see fig. 9)

The PWM signal is generated on the comparator output; the triangular-shaped waveform and the continuous signal coming from the output of the transconductance error amplifier are sent to its inputs. The PWM signal is then transferred to the driving stage of the output power transistor.

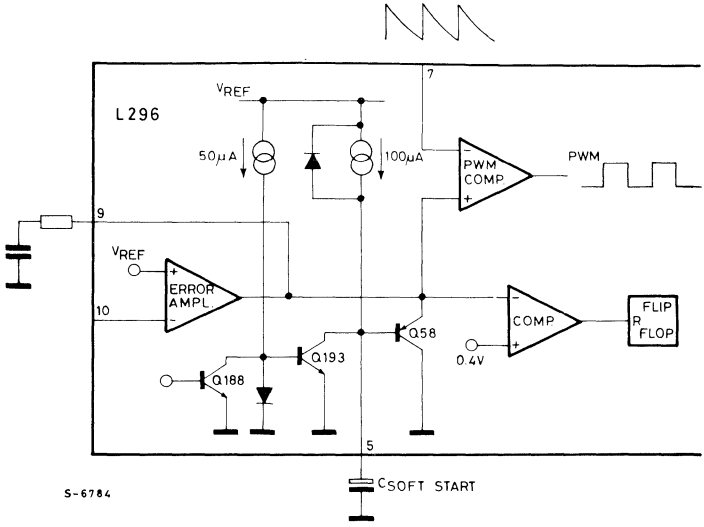
SOFT START (see fig. 9)

Soft start is an essential function for correct start-up, to prevent stresses and possible breakdown from occurring in the power transistor and to obtain a monotonically increasing output voltage.
In particular, the L296, as it does not have any duty cycle limitation and due to the type of current limitation does not allow the output to be forced to a steady state without the aid of the soft-start facility. Soft-start operates at the start-up of the system, after the inhibit has been activated, after an intervention of the current limitation and after the intervention of the thermal protection.

The soft-start function is realized through a capacitor connected to pin 5 which is charged at constant current ($\cong 100\mu A$) up to a value of about V_{REF}. During the charging time, through PNP transistor Q58, the voltage on pin 9 is forced to increase with the same rising speed as on pin 5. Starting from the discharged capacitor condition (pin 5 voltage = 0V) the power transistor is in the OFF condition, as the voltage on pin 9 is smaller than the minimum level of the ramp voltage. As the capacitor is charged, the PWM signal begins to be generated as soon as the error amplifier output voltage crosses the ramp; the power stage starts to switch with steadily increasing duty cycle. This behaviour is shown in fig. 10. As soon as the steady condition is reached the duty cycle sets itself to the right value due to the effect of the feedback network while the soft-start capacitor completes its charging to a value very close to V_{REF}.

The soft-start effect is determined, apart from the switch-on time, when the current limitation operates, due to either an overload or a short circuit, to keep the mean value of the current absorbed by the power supply low.
Moreover from fig. 11 it may be observed that since the voltage on pin 9 can decrease under the minimum ramp level and increase over the maximum level no limitations have been provided on the duty cycle, which therefore may vary between 0 and 100%.

Fig. 9 – Partial internal schematic showing PWM and soft start blocks.



$$t_{start\text{-}up} = \frac{C_{ss}\ (V_r - 0.5V)}{I_{5so}}$$

where C_{ss} is the soft-start capacitor and I_{5so} is the charging current.

Considering as the soft-start time the time required for the soft-start capacitor to charge from (1.2V-0.5V) to $V_r - 0.5V$, gives:

$$t_{ss} = \frac{C_{ss}\ (V_r - 1.2)}{I_{sso}} \qquad (28)$$

substituting V_r from (27) gives:

$$V_r = E\ e^{-\left(1 - \frac{V_o}{V_i}\right)}$$

substituting into (28) gives:

$$t_{ss} = \frac{C_{ss}}{I_{sso}} \left(E\ e^{\left(\frac{V_o}{V_i} - 1\right)} - 1.2 \right)$$

SYNCHRONIZATION

The synchronization function is available on pin 7, this function allows the device to be switched at an externally generated frequency (leaving pin 11 open), or to mutually synchronize several devices, using one of them as master and the others as slave (Fig. 12).

This allows several devices to be operated at the same frequency, avoiding undesirable intermodulation phenomena. The number of mutually synchronizable devices is obviously much greater than the three devices shown in the figure. It is anyway difficult to establish an exact maximum number of devices, as it depends on different conditions.

The first consideration concerns the accuracy which must be achieved and maintained on the oscillation frequency. Since the bias current on pin 7 is an output current, the sum of all the bias currents must be much smaller than the capacitor discharge current in close proximity to the lower discharge threshold. Therefore, assuming $C_{osc} = 2.2$ nF and $R_{osc} = 4.3$ KΩ, it follows that:

$$\frac{1.2V}{4.3\ K\Omega} = 280\mu A$$

Assuming that a 10% variation may be accepted, it follows therefore that the number of synchronizable devices is given by:

$$N = \frac{28\ \mu A}{I_{bias\ max}}$$

This means that if the overall I_{bias} is too high it may modify the discharging time of the capacitor.

The second consideration concerns the layout design.
In the presence of a great number of devices to be synchronized, the lenght of the paths may become significant and therefore the distributed inductance introduced along the paths may begin to modify the triangular shaped waveform, particularly the rising edge which is very steep. This effect would affect the devices that are physically located more distant from the master device.

The amplitude of the saw-tooth to be externally connected must be within 0.5V and 3.5V, values also representing the maximum swing of the error amplifier output.

Fig. 12 – In multiple supplies several L296's can be synchronized as shown here.

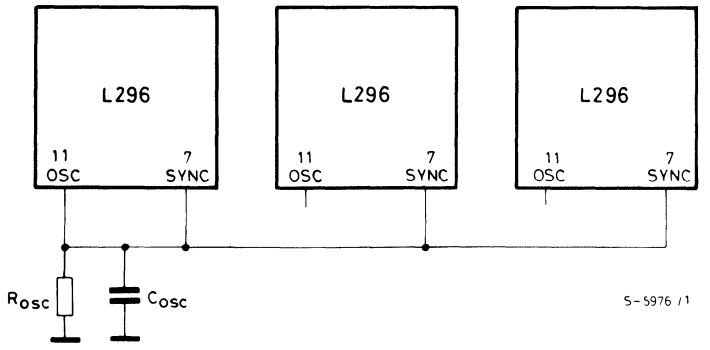


Fig. 14a – Current limiter waveforms.

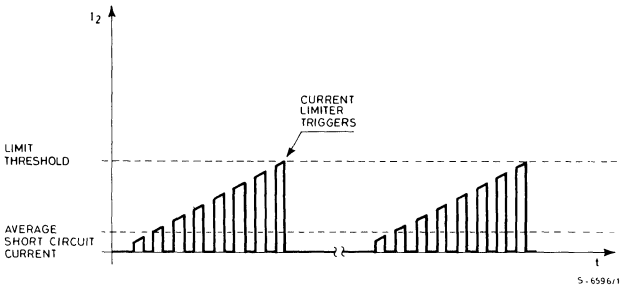


Fig. 14b – Load current in short circuit conditions ($V_i = 40v$, $L = 300\ \mu H$, $f = 100\ KHz$)

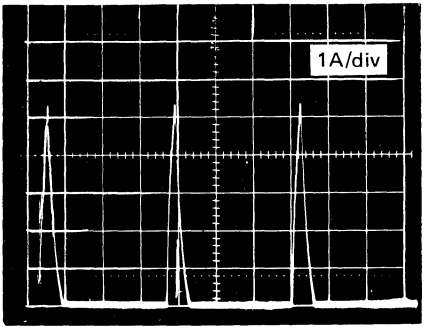
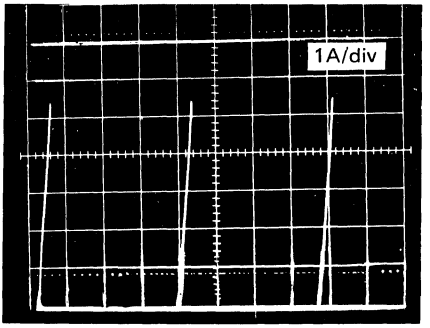


Fig. 14c – Current at pin 2 when the output is short circuited.



RESET

The reset function is of great importance when the device is used to supply microprocessors, logic devices, and so on. This function differentiates the SGS L296 device from all previous devices. The block diagram of the function is shown in fig. 15. A reset signal is generated when the output voltage is within the limits required to supply the microprocessor correctly.

The reset function is realized through the use of 3 pins: the reset input pin 12, the reset delay pin 13 and the reset output pin 14. When the voltage on pin 12 is smaller than 5V the comparator output is high and the reset capacitor is not charged because the transistor Q is satured and the voltage on pin 14 is at low level, since Q2 is saturated, too. When the voltage on pin 12 goes above 5V, the transistor Q switches OFF and the capacitor can start to charge through a current generator of about 100 μA. When the voltage on pin 13 goes above 4.5V the output of the related comparator switches low and the pin 14 goes high. As the output consists of an open collector transistor, a pull-up external resistance is required. In contrast, when the reset input voltage goes below 5V, less a hysteresis voltage of about 100 mV, the comparator triggers again and instantaneously sets the voltage on pin 14 low, therefore forcing to saturation the Q1 transistor, that starts the rapid discharge of the capacitor. Obviously, the reset delay is again present when the voltage on pin 13 is allowed to go under 4.5V.

To achieve switching operations without uncertainties the two comparators have been provided with an hysteresis of about 100 mV. In every operating condition the reset switching is guaranteed with a minimum reset input of 4.75V, the value required for correct operation of the microprocessor even in the presence of the minimum V_{REF} value.

Normally pin 12 is used connected to pin 10. When it is connected to the output, the function may be more properly called "reset"; on the other hand, when it is connected through resistive divider, to the input voltage, the function is called "power fail". Fig. 16 and fig. 17 show the two possible usages.

The "power-fail" function is used to predict, with a given advance, the drop of the regulator output voltage, due to main failures, which is enough to save the data being processed into protected memory areas. Fig. 18 summarises the reset function operation.

CROWBAR

This protection function is realized by a completely independent block, using pin 1 as input and pin 15 as output. It is used to prevent dangerous overvoltages from occurring when the output exceeds 20% of rated value. Pin 15 is able to output a 100 mA current to be sent to the gate of a SCR which, triggering, short circuits either output or the input. When connected to the input, as the SCR is triggered a fuse in series connected to power supply is blown and to bring the system back to operation manual intervention is requested. Figs. 19, 20 and 21 show the different configurations.

When the voltage on pin 1 exceeds by about 20% the V_{REF} value the output stage is activated, which sends a current to the SCR gate, after a delay of about 5 μsec to make the system insensitive to low-duration spikes. When activated, the output stage delivers about 100mA; when not activated, it drains about 5 mA and shows a low impedance to the SCR gate to avoid uncorrect triggering due to random noise. If the crowbar function is not used connect pin 1 to ground.

Fig. 19 – Connection of crowbar circuit at output for 5.1V output applications.

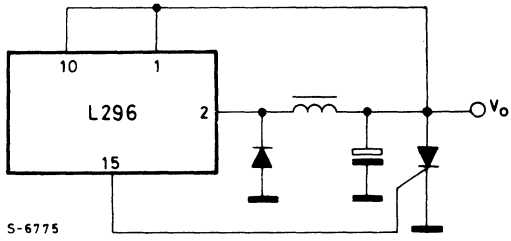


Fig. 20 – Connection of crowbar circuit at output for output voltages above 5.1V.

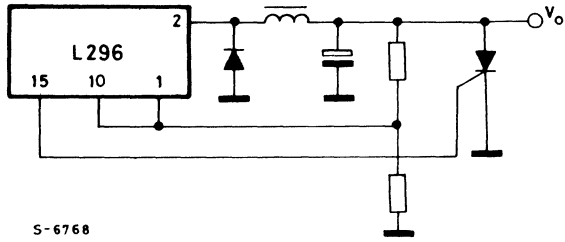
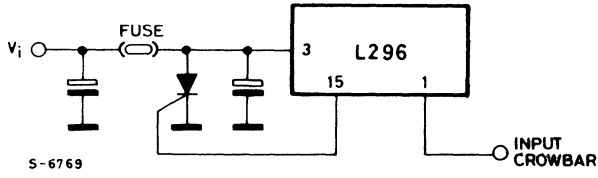


Fig. 21 – Connection of crowbar circuit to protect input. When triggered, the SCR blows the fuse.



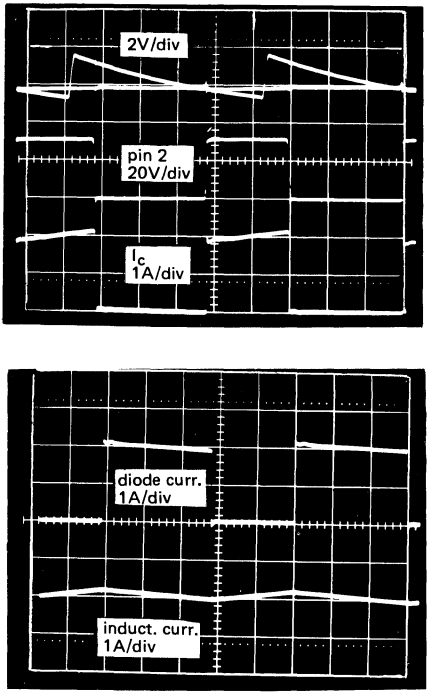
INHIBIT

The inhibit input (pin 6) is TTL compatible and is activated when the voltage exceeds 2V and deactivated when the voltage goes under 0.8V. As may be seen in the block diagram, the inhibit acts on the power transistor, instantaneously switching it off and also acts on the soft-start, discharging its capacitor. When the function is unused, pin 6 must be grounded.

THERMAL PROTECTION

The thermal protection function operates when the junction temperature reaches 150°C; it acts directly on the power stage, immediately switching it off, and on the soft-start capacitor, discharging it. The thermal protection is provided with hysteresis and, therefore, after an intervention has occurred, it is necessary to wait for the junction temperature to decrease of about 30°C below the intervention threshold.

Fig. 23 – Oscilloscope photographs showing main waveforms of the figure 22 circuit.



The oscilloscope photographs of the main waveforms are shown in fig. 23. The output voltage ripple ΔV_O depends on the current ripple in the coil and on the performance of the output capacitor at the switching frequency (100 kHz). A capacitor suitable for this kind of application must have a low ESR and be able to accept a high current ripple, at the working frequency. For this application the Roederstein EKR series capacitors have been selected, designed for high frequency applications (>200 kHz) and manufactured to show low ESR value and to accept high current ripples. To minimize the effects of ESR, two 100 μF/40V capacitors have been connected in parallel. The behaviour of the impedance as a function of frequency is shown in fig. 24.

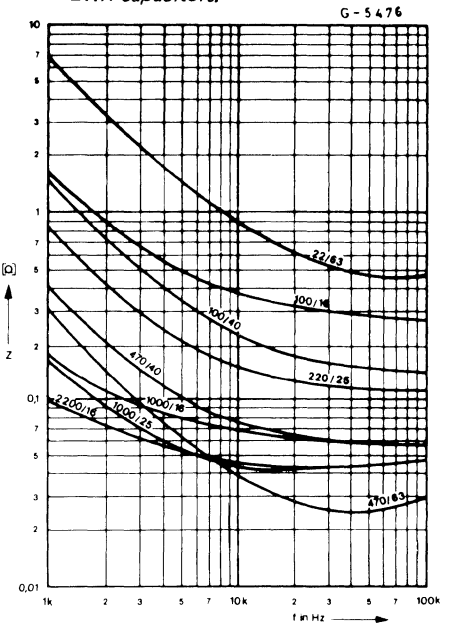
Also the selection of the catch diode requires special care. The best choice is a Schottky diode which minimizes the losses because of its smaller forward voltage drop and greater switching frequency rate. A possible limitation comes from the backward voltage, that generally reaches 40V max.
When the full input voltage range of the device is required in this application it is possible to use super fast diodes with 35 to 50 ns rated recovery time, where no more problems on the backward voltage occur (on the other hand, they show a greater forward voltage). The use of slower diodes, with trr = 100 ns or more is not recommended; The photographs in fig. 25 show the effects on the power current and on the voltage on pin 2, due to the diodes showing different speeds. Diodes showing trr greater than 35-50 ns will reduce the overall efficiency of the system, increasing the power dissipated by the device.

The third component requiring care is the inductor. Fig. 22a shows the part numbers of some types used for testing. Besides having the required inductance value, the coil has to show a very high saturation current.
Therefore, a correct dimensioning requires a saturation current above the maximum value of I_{2L}, the current limit threshold.

To achieve high saturation with ferrite cores an air gap between the two core halves must be provided; the air gap causes a leakage flux which is radiated in the surrounding space. To better limit this phenomenon "pot cores" may be used, whose geometry is such to better limit the flux radiated to the outside.
Using toroidal cores, for instance of Magnetic 58930-A2 moly-permalloy kind, both the requirements of high saturation and low leakage flux are satisfied. The saturation is softer that the saturation shown by the ferrite materials. The air gap is not concentrated in one area, but is finely distributed along the whole core; this gives the low leakage flux value.

Careful selection of the external components therefore allows the realization of a power supply system whose benefits are significant when compared to a system with the same performance but realized with the linear technique.

Fig. 24 – Typical impedance/frequency curves for EKR capacitors.



	Linear	Switching
Transformer	62 VA	30 VA
Heatsink	0.8 °C/W	11 °C/W

This comparison shows that the L296 switching regulator allows a saving of roughly 50% on the cost of the transformer and an impressive 80-90% on the cost of the heatsink. Considering also the extra functions integrated by the L296 the total cost of active and passive components is roughly the same for both types.

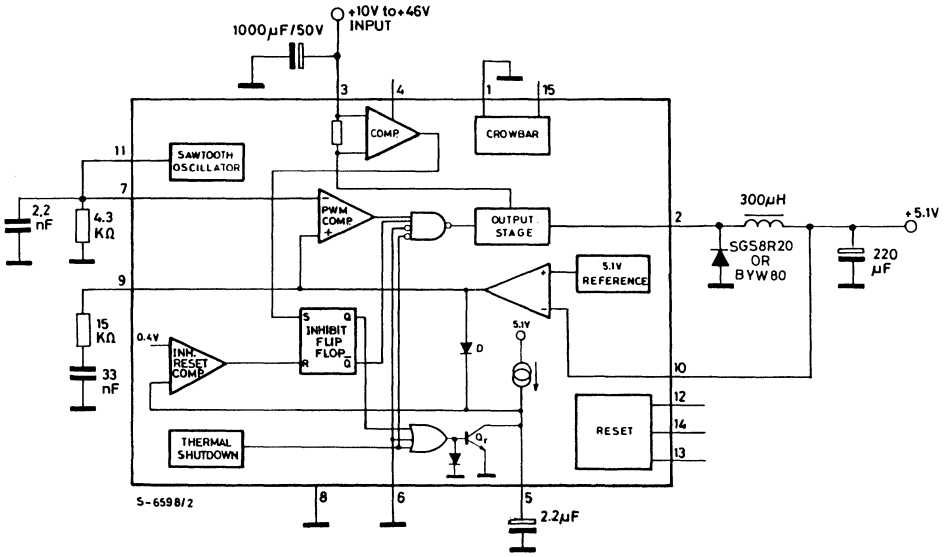
Finally, it is important to note that a lower power dissipation means that the ambient temperature in the regulator enclosure can be lower - particularly when the circuit is enclosed in a box - with all the advantages cooler operation brings.

If for some reason it is necessary to use higher supply voltages the switching technique, and hence the L296, becomes even more advantageous.

LOW COST APPLICATION AND PREREGULATOR

Fig. 26 shows the low cost application of a 4A and V_o = 5.1V power supply. A minimum amount of essential external components is required, which are necessary for correct operation. It is impossible to save other components, specially the soft-start capacitor. Without soft-start, the system cannot reach the steady state and there is also a serious risk of damaging the device.

Fig. 26 – A minimal component count 5.1V/4A supply.



This application is very well suited not only as a low-cost power supply, but also as pre-regulator for post-regulators distributed in different circuit points, or even on different boards (Fig. 27). The post-regulators may be selected among the low-drop types, like L4805 and L387 for example, still obtaining a high efficiency, combined with an excellent regulation. The use of L387 device allows us to use also the reset function, useful to power a micropocessor.

POWER SUPPLY COMPLETE WITH TRANSFORMER

Fig. 28 shows a power supply complete of transformer, bridge and filter, with regulation on the output voltage from 5.1V to 15V.

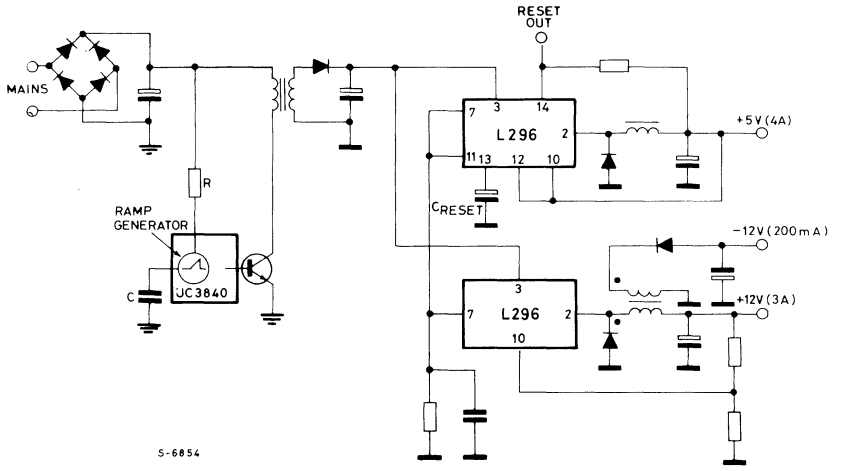
As already stated above, the output capacitors have to show some speciale features, like low ESR and high current ripple, to obtain low voltage ripple values and high reliability. The input filter capacitors must not be neglected because they have to show excellent features, too, having to supply a pulsed current, required by the device at the switching frequency. The current ripple is rather high, greater than the load current. For this application, two parallel connected 3300 µF/50V EYF (ROE) capacitors have been used.

POWER SUPPLY WITH MAINS SWITCHING PREREGULATOR

When it is desirable to eliminate the 50/60 Hz transformer – in portable or volume-limited equipment – a mains preregulator can be added to reduce the input voltage to a level acceptable for the L296.

In this case the pre-regulator circuit is connected to the primary of the transformer which now operates at the switching frequency and is therefore smaller and lighter.

Fig. 28A – A multiple output supply using a switching preregulator rather than a mains transformer.



POWER SUPPLY WITH 0 – 30V ADJUSTABLE VOLTAGE

When output voltages lower than 5V are required, the circuit shown in fig. 29 may be used.

Calibration is performed by grounding the P1 slider. Acting on P2, the current which flows through the 10 kΩ resistor is fixed at approximately 2.5mA to obtain an output voltage of 30V. The equivalent circuit is shown in fig. 30.

Acting now on the slider of P1, the current flowing through the divider may be varied. The new equivalent circuit is shown in fig. 31.

Reducing the current flowing, also the voltage drop across the 10kΩ resistance is reduced, together with V_o. When the current reaches zero, it follows that $V_o = V_{REF}$. When the voltage on the slider of P1 exceeds V_{REF}, the current start to flow in opposite direction and V_o begins to decrease below 5V.

When $I_1 \times 10K\Omega = V_{REF}$ it follows that $V_o = 0$.

Fig. 29 – Variable 0-30 V supply illustrating how output voltages below 5.1V are obtained.

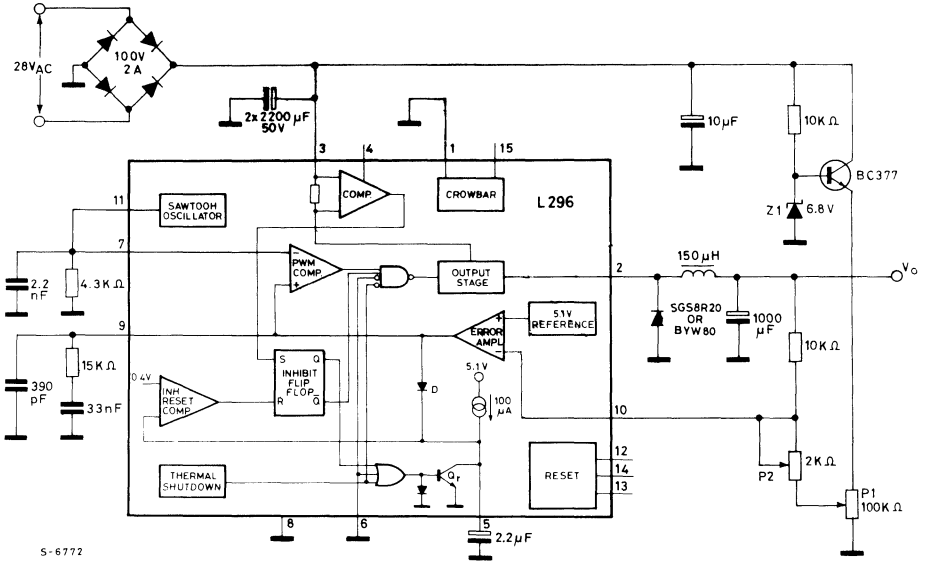
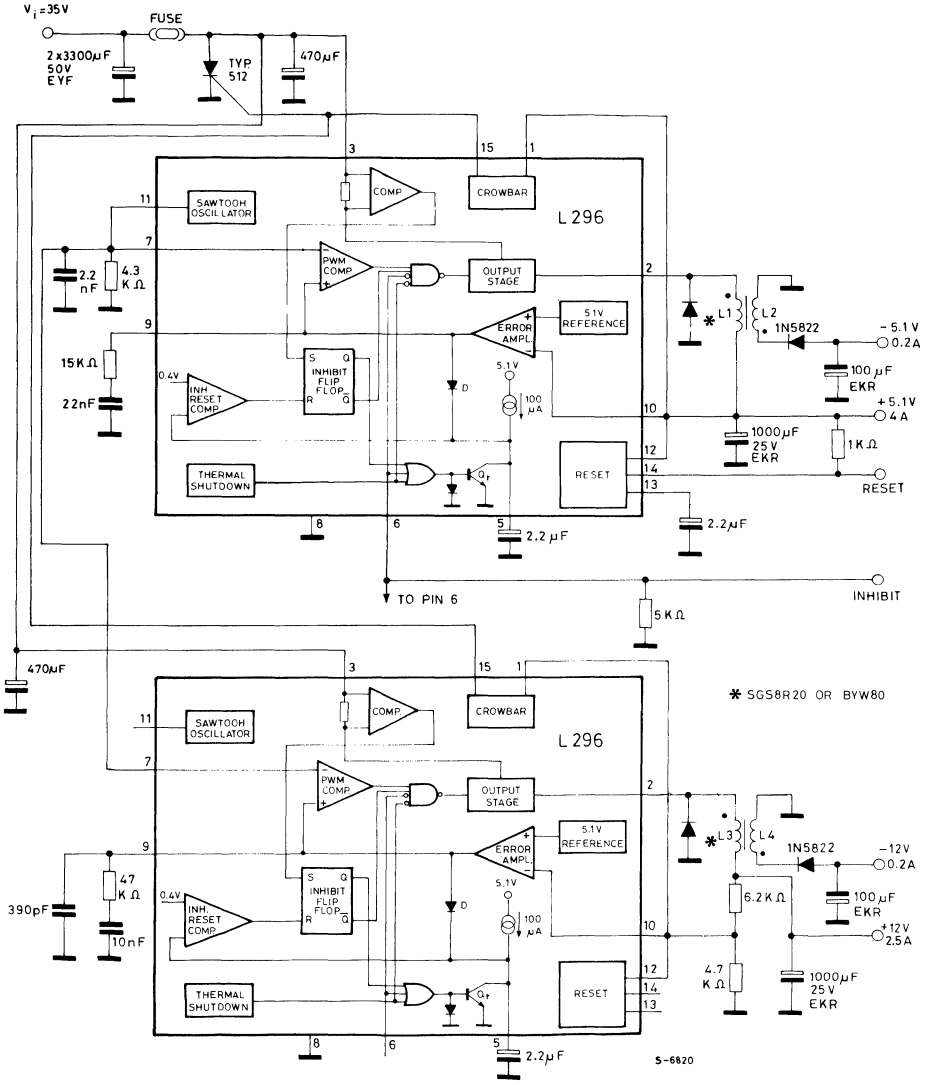


Fig. 33 – Microcomputer supply with 5V, -5V, 12V and -12V outputs.



The two devices are mutually synchronized not to give rise to intermodulation which could generate unpleasant noise and, at the same time, a further component saving is achieved.

The crowbar function is implemented on both 5V and 12V outputs, using a single SCR connected to the input. The latter, by discharging to ground the electrolytic filter capacitors, blows the fuse connected in series with the devices power supply. In this way, should a faulty be present on either of the main outputs, the supply is switched off for whole system.

To inhibit both the devices with a single input signal, it is possible to connect the two inhibit inputs (pin 6) together; the 5KΩ resistance is used when the inhibit input is left open. If this input is not used it must be grounded.

As may be noted in the diagram, to obtain the two auxiliary voltages is very simple and cost-effective.

It is suggested that the diodes are fast types (trr< 50 nsec); should slower diodes be required some more turns have to be added to the auxiliary winding.

MOTOR CONTROL

The L296 is also suitable for use in motor controls applications. Fig. 36 shows how to use the device to drive a motor with a maximum power of about 100W and provided with a tachometer generator for a good speed control.

HIGHER CURRENT REGULATORS

It is possible to increase the output current to the load above 4A through the use of an external power transistor. Fig. 37 shows a suitable circuit. The frequency is around 40 kHz to prevent the device from loosing excessive power due to switching on the external power.

The circuits shown in fig. 38 and fig. 39 show how current limitation may be realized in two different ways: through a sensing resistor connected in series with the collector of the external power transistor or through a current transformer.

In the first case, the sensing resistor is a low value resistor able to withstand the maximum load current required. The V_{CE} of the power transistor is higher than its V_{CEsat}; when the resistor is connected in series to the collector V_{CE} is reduced; consequently since the overall dissipated power is constant, the power dissipated by the sensing resistor is subtracted from that dissipated by the power transistor. The values indicated in figs. 38 and 39 realize adjustable current limitation for load currents around 10A.

Fig. 36 – With a tacho dynamo supplying feedback the L296 can be used as a motor speed controller.

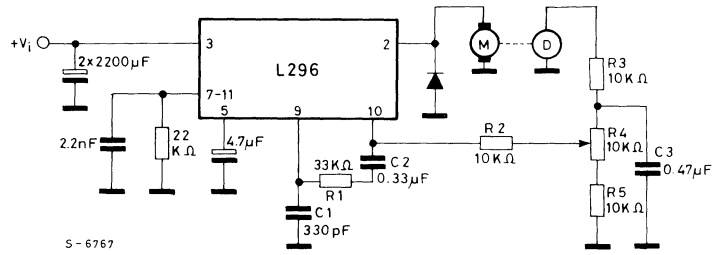


Fig. 37 – The output current may be increased by adding a power transistor as shown in this circuit.

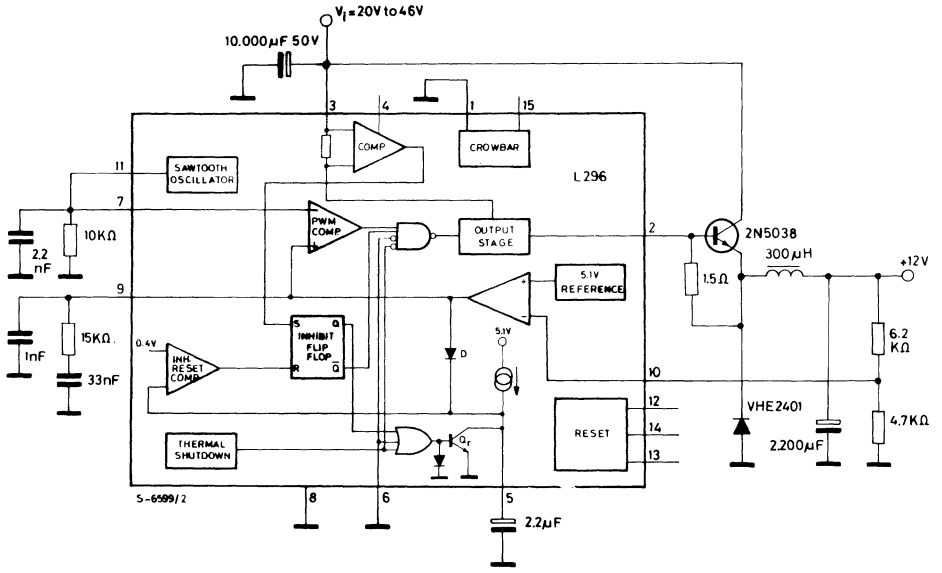


Fig. 40 – A step-up converter using a power MOS transistor.

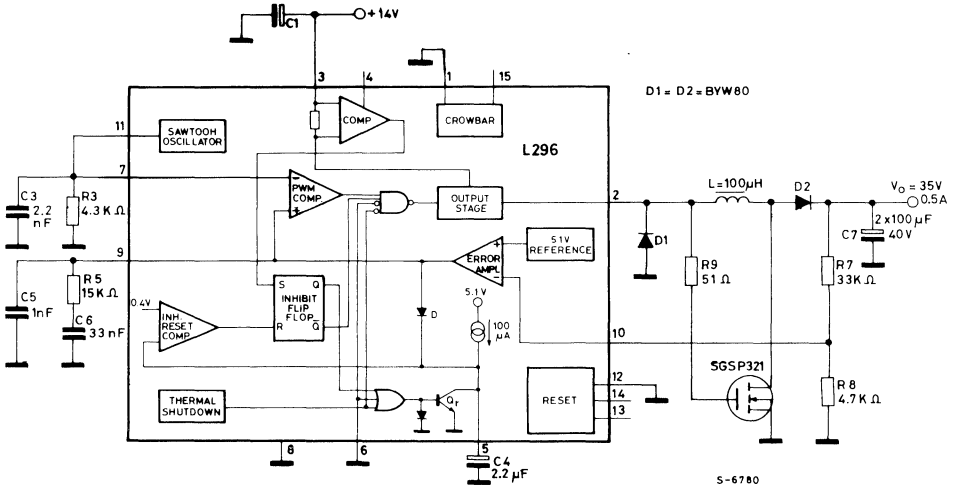
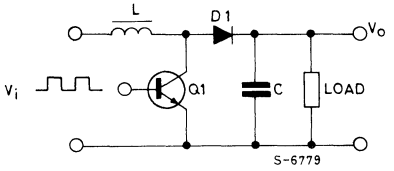


Fig. 41 – Basic schematic for step-up configurations.



In this configuration, unlike the step-down configuration, the peak current is not strictly related to the load current. The energy stored in the coil is successively discharged across the load when the transistor switches OFF. To calculate the I_o load current, the following procedure may be used:

$$\frac{1}{2} L I_{peak}^2 = V_o I_o T$$

$$I_o = \frac{L I_{peak}^2}{2 V_o T} = \frac{V_i^2 T_{ON}^2}{2 L V_o T}$$

For a greater output power to be available, the internal limitation must be replaced by an external circuit to protect the external power devices and to limit the current peak to a convenient value. A dual comparator (LM393) with hysteresis is used to avoid uncertainties when the current limitation operates. The electric diagram is shown in fig. 42.

LAYOUT CONSIDERATIONS

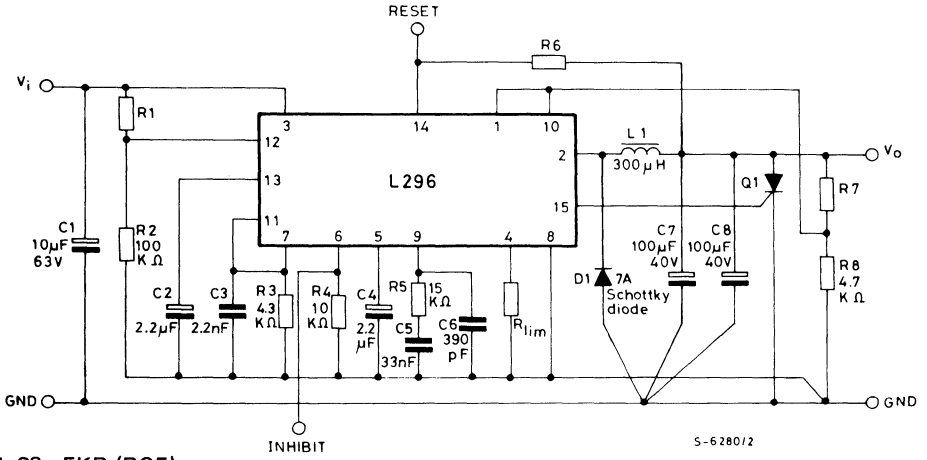
Both for linear and switching power supplies when the current exceeds 1A a careful layout becomes important to achieve a good regulation. The problem becomes more evident when designing switching regulators in which pulsed currents are over imposed on dc currents. In drawing the layout, therefore, special care has to be taken to separate ground paths for signal currents and ground paths for load currents, which generally show a much higher value.

When operating at high frequencies the path length becomes extremely important. The paths introduce distributed inductances, producing ringing phenomena and radiating noise into the surrounding space.

The recirculation diode must be connected close to pin 2, to avoid giving rise to dangerous extra negative voltages, due to the distributed inductance.

Fig. 43 and fig. 44 respectively show the electric diagram and the associated layout which has been realized taking these problems into account. Greater care must be taken to follow these rules when two or more mutually synchronized devices are used.

Fig. 43 – Typical application circuit showing how the signal and power grounds are connected.



C7, C8 : EKR (ROE)

Suggested Inductor (L1)

Core Type	No Turns	Wire Gauge	Air Gap
Magnetics 58930 - A2MPP	43	1.0 mm.	–
Thomson GUP 20x16x7	65	0.8 mm.	1 mm.
Siemens EC 35/17/10 (B6633& - G0500 - X127)	40	2 x 0.8 mm.	–
VOGT 250 µH Toroidal coil, part number 5730501800			

Resistor values for standard output voltages		
V_o	R8	R7
12V	4.7 kΩ	6.2 kΩ
15V	4.7 kΩ	9.1 kΩ
18V	4.7 kΩ	12 kΩ
24V	4.7 kΩ	18 kΩ

Fig. 44 – A suitable PCB layout for the figure 43 circuit realized in accordance with the suggestions in the text (1 : 1 scale).

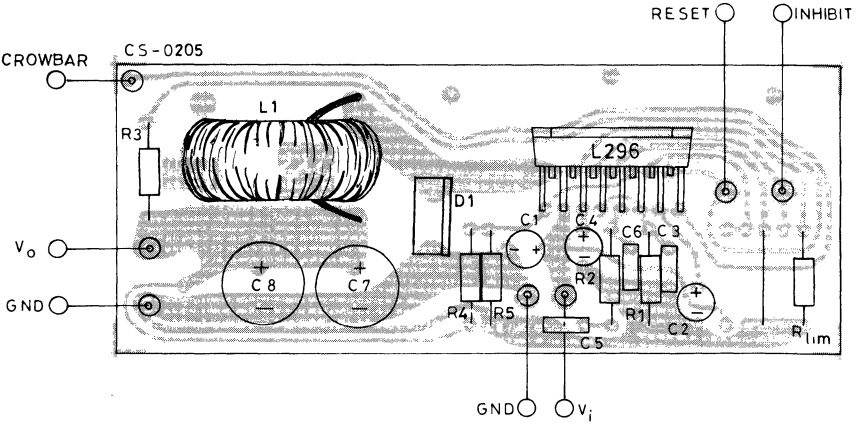


Fig. 50

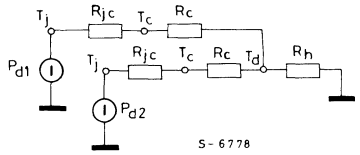


Fig. 52 shows the trend of the temperature as a function of the distance between two dissipating elements whose dissipated power is fairly different (ratio 1 to 4). This graph may be useful in application with two L296 synchronized.

Fig. 51

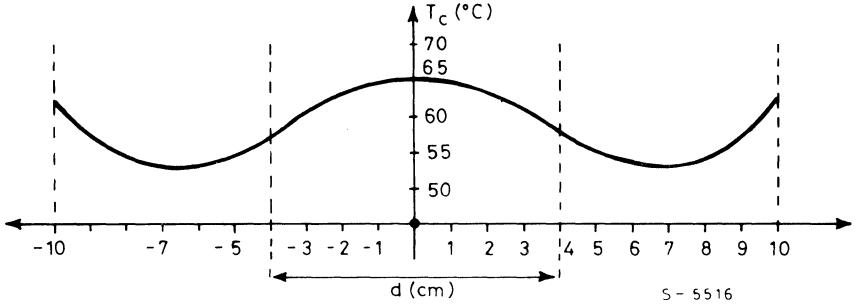
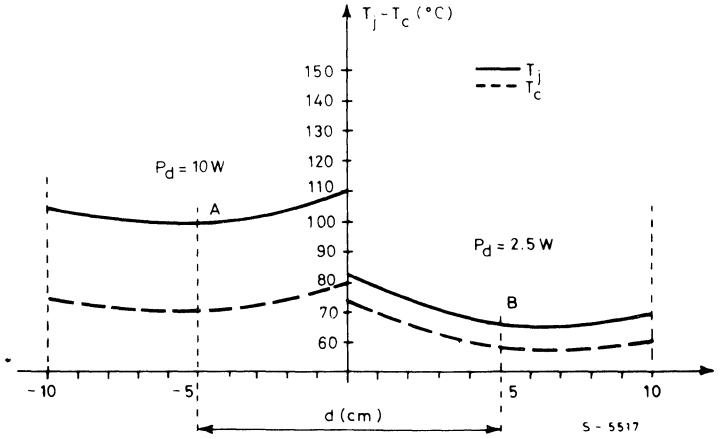


Fig. 52



In the application a series RC network is recommended which gives high system gain at low frequency – to ensure good precision and mains ripple rejection and a lower gain at high frequencies to ensure stability of the system. Figure A2 shows the gain and phase curves of the uncompensated error amplifier.

The amplifier has one pole at about 7 kHz and a phase shift which reaches about – 90° at frequencies around 1 MHz.

The introduction of a series network R_C C_C between the output and ground modifies the circuit as shown in figure A3.

Figure A4 shows the gain and phase curves of the compensated error amplifier.

Fig. A3 – Compensation network of the error amplifier.

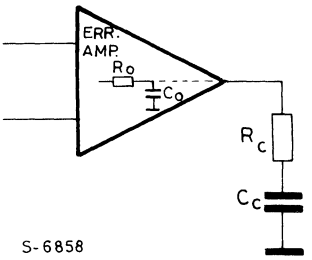
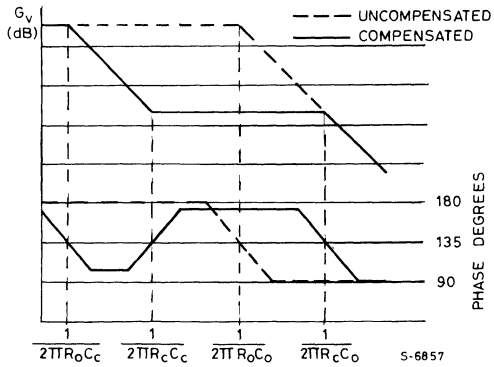


Fig. A4 – Bode plot showing gain and phase of compensated error amplifier.



CALCULATING THE STABILITY

For the stability calculation refer to the block diagram shown in figure A5.

The transfer functions of the various blocks are rewritten as follows.

The simplified transfer function of the compensated error amplifier is:

$$G_{EA} = g_m Z_c = g_m \frac{1 + s R_c C_c}{s C_c} \qquad (g_m = \frac{1}{2500})$$

The DC gain must be considered equal to

$$A_o = g_m R_o$$

PWM block and output stage:

$$G_{PWM} = \frac{V_i}{V_{ct}}$$

LC FILTER:

$$G_{LC} = \frac{1 + s\,C \cdot ESR}{s^2 LC + s\,C\,ESR + 1}$$

where ESR is the equivalent series resistance of the output capacitor which introduces a zero at high frequencies, indispensable for system stability. Such a filter introduces two poles at the angular frequency.

$$\omega_o = \frac{1}{\sqrt{LC}}$$

Refer to the literature for a more detailed analysis.

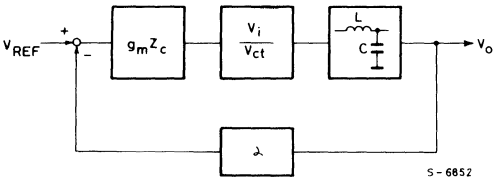
Feedback: consists of the block labelled α

$\alpha = 1$ when $V_o = V_{REF}$ (and therefore $V_o = 5.1V$)

and

$$\alpha = \frac{R_2}{R_1 + R_2} \quad \text{when } V_o > V_{REF}$$

Fig. A5 – Block diagram used in stability calculation



To analyse the stability we will use a Bode diagram. The values of L and C necessary to obtain the required regulator output performance, once the frequency is fixed, are calculated with the following formulae:

$$L = \frac{(V_i - V_o)\,V_o}{V_i\,f\,\Delta I_L}$$

$$C = \frac{(V_i - V_o)\,V_o}{8\,L\,f^2\,\Delta V_o}$$

Since this filter introduces two poles at the angular frequency

$$\omega_o = \frac{1}{\sqrt{LC}}$$

we place the zero of the R_c C_c network in the same place:

$$\omega_z = \frac{1}{R_c C_c}$$

generally found distributed along the strips of the printed circuit board.

Fast switching of the power transistors tends to cause ringing and oscillations as a result of the parasitic elements. The use of a diode with a fast reverse recovery time (trr) contributes to a reduction in the noise flowing by the current peak generated when the diode is reverse biased.

Radiated interference is usually reduced by enclosing the regulator in a metal box.

To reduce conducted electromagnetic interference (or radio frequency interferences – RFI) to the levels permitted a suitably dimensioned filter is added on the supply line. The best method, generally, to reduce conducted noise is to filter each output terminal of the regulator. The use of a fixed switching frequency allows the use of a filter with a relatively narrow bandwidth. For off-line switching regulators this filter is usually costly and bulky. In contrast, if the device is supplied from a 50/60 Hz transformer the RFI filter problem is greatly reduced.

Tests have been carried out at the laboratories of Roederstein to determine the dimensions of a mains supply filter which satisfies the VDE 0871/6.78, class B standard. The measurements (see figs. B1 and B2) refer to the application with the L296 supplied with a filtered secondary voltage of about 30V, with V_o = 5.1V and I_o = 4A. The switching frequency is 100 kHz.

Figure B1 shows the results obtained by introducing on the transformer primary a 0.01 μF/250V~ class X capacitor (type ERO F1772-310-2030). To reduce interference further below the limit set by the standards an additional inductive filter must be added on the primary of the transformer.

Figure B2 shows the curves obtained by introducing this inductive filter (type ERO F1753-210-124).

Measurements have also been performed beyond 30 MHz; the maximum value measured is still well below the limit curve.

Fig. B1 – EMI measurements with a capacitor connected across the primary transformer with screen grounded (A) and floating (B)

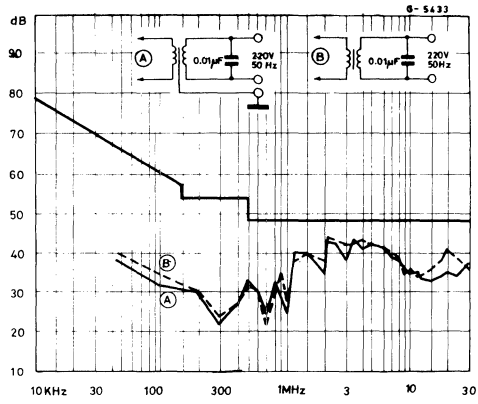
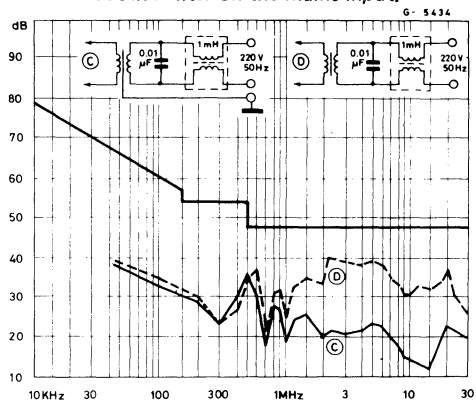
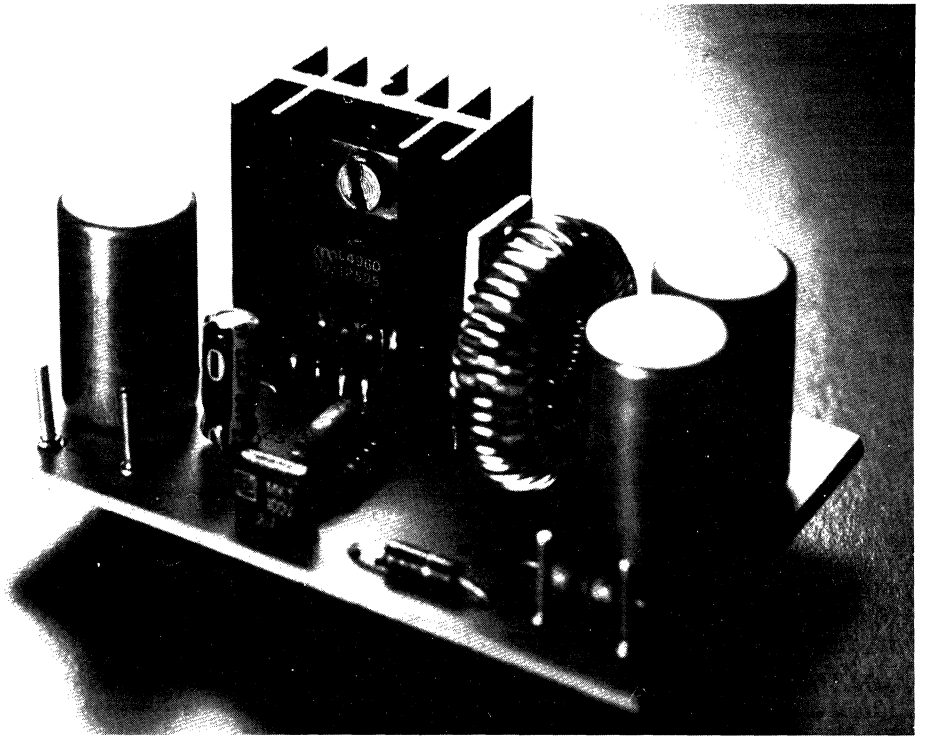


Fig. B2 – EMI results with the addition of an inductive filter on the mains input.



DESIGNING MULTIPLE-OUTPUT POWER SUPPLIES WITH THE L296 AND L4960

Multiple output supplies can be realized simply and economically using the SGS L296 and L4960 high power switching regulators. This note describes several practical circuits of this type.



Most of the switching regulators produced today have multiple outputs. The output voltages most frequently used – at least for powers up to 50W - are +5V -5V, +12V and -12V. In these supplies the 5V output is normally the output which delivers the highest current and requires the highest precision. For the other voltages – particularly the negative outputs – less precision (±5% ±7%) is usually sufficient. Often, however, for high current 12V outputs better stabilization and greater precision (typically ±4% - the output tolerance of an L7800 series linear regulator) are required.

Multiple output supplies which satisfy these requirements can be realized using the SGS L296 and L4960 high power switching regulator ICs, Several practical supply designs are described below to illustrate how these components are used to build compact and inexpensive multi-output supplies.

DUAL OUTPUT 15W SUPPLY

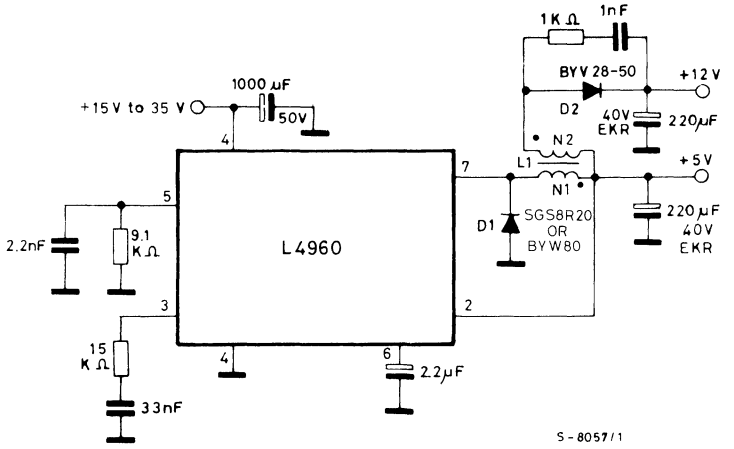
V_{o1} = 5V/3A, V_{o2} = 12V/150mA

A single L296 is used in this application to produce two outputs. The application circuit, Figure 1, illustrates how the second output (12V) is obtained by adding a second winding to the output inductor. Energy is transferred to the secondary during the recirculation period when the internal power device of the L296 is OFF.

Since the 12V output is not separated from the 5V output fewer turns are necessary for the second winding, therefore less copper is needed and load regulation is improved.

In applications of this type it is a good rule to ensure that the power drain on the auxiliary output is no more than 20-25% of the power delivered by the main output.

Fig. 2 - Dual output DC-DC converter (5V/1.5A, 12V/100mA)



Transformer: magnetics 58206, N1 = 30 turns, N2 = 40 turns

TABLE 2

Parameter		V_{o1}	V_{o2}	Unit
Output voltage I_{o1} = 1.5A	V_i = 25V I_{o2} = 100mA	5.050	12.010	[V]
Output ripple		50	30	[mV]
Line regulation I_{o1} = 1.5A	15V ⩽ V_i ⩽ 35V I_{o2} = 100mA	7	75	[mV]
Line regulation I_{o1} = 500mA	15V ⩽ V_i ⩽ 35V I_{o2} = 50mA	7	60	[mV]
Load regulation I_{o1} = 0.5A → 1.5A	V_i = 25V I_{o2} = 100mA	3	100	[mV]
Load regulation I_{o1} = 500mA	V_i = 25V I_{o2} = 50mA → 100mA	0	55	[mV]
Load regulation I_{o1} = 1.5A	V_i = 25V I_{o2} = 50mA → 100mA	0	50	[mV]
Efficiency	V_i = 25V I_{o1} = 1.5A I_{o2} = 100mA	78		%

TRIPLE OUTPUT 15W SUPPLY

V_{o1} = 5V/3A, V_{o2} = 12V/100mA, V_{o3} = -12V/100mA

Figure 3 shows how to obtain two auxiliary outputs (± 12V) which are isolated from the 5V output. For this output power range an L296 is used.

To ensure good tracking of the 12V and -12V outputs the secondary outputs in this application should be bifilar wound.

This circuit operates at 50KHz and gives the performance indicated in Table 3.

Fig. 4 - Triple output DC-DC converter (5V/1.5A, 12V/50mA, -12V/50mA)

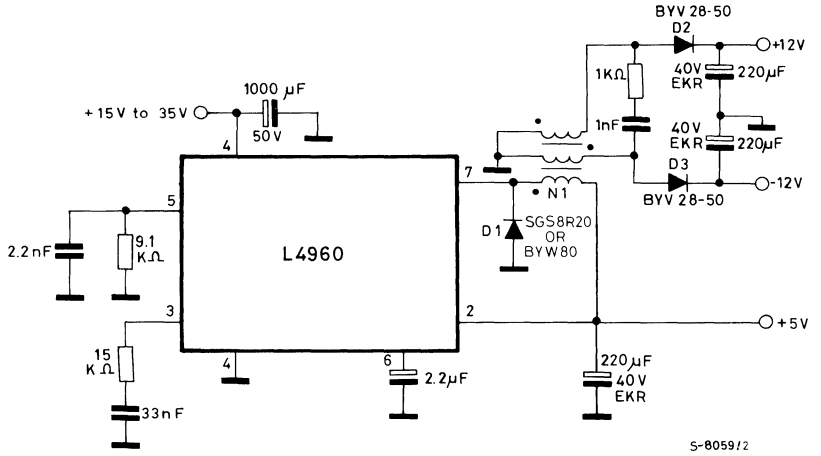


TABLE 4

Parameter		V_{o1}	V_{o2}	V_{o3}	Unit
Output Voltage I_{o1} = 1.5A	V_i = 25V $I_{o2} = I_{o3}$ = 50mA	5.040	12.020	-12.020	[V]
Output ripple		60	30	30	[mV]
Line regulation I_{o1} = 500mA	$15 \leqslant V_i \leqslant 35V$ $I_{o2} = I_{o3}$ = 50mA	5	80	80	[mV]
Line regulation I_{o1} = 1.5A	$15 \leqslant V_i \leqslant 35V$ $I_{o2} = I_{o3}$ = 50mA	4	60	60	[mV]
Load regulation I_{o1} = 0.5 → 1.5A	V_i = 25V $I_{o2} = I_{o3}$ = 50mA	5	120	120	[mV]
Load regulation I_o = 1.5A I_{o3} = 20 → 50mA	V_i = 25V I_{o2} = 50mA	0	15	50	[mV]
Load regulation I_{o1} = 1.5A I_{o2} = 20 → 50mA	V_i = 25V I_{o3} = 100mA	0	50	15	[mV]
Efficiency			70		%

THE L296 AND L4960 HIGH POWER SWITCHING REGULATORS

The SGS L296 is a monolithic stepdown switching regulator assembled in the 15-pin Multiwatt package. Operating with supply input voltages up to 46V it provides a regulated 4A output variable from 5.1V to 40V.

Internally the device is equipped with current limiter, soft start and reset (or power fail) functions, making it particularly suitable for supplying microprocessors and logic.

The precision of the L296's internal reference (±2%) eliminates the need for external dividers or trinning to obtain a 5V output.

The synchronization pin allows synchronous operation of several devices at the same frequency to avoid generating undesirable beat frequencies.

The L4960 is a similar device assembled in the 7-lead Heptawatt package. Like the L296 it has a maximum input voltage of 46V and it provides a regulated output voltage variable from 5V to 40V with a maximum load current of 2.5A. Current limiting, soft start and thermal protection functions are included.

30W DC-DC CONVERTER

Designing power supplies in the 30-40W range is becoming increasingly difficult because it is here that there is the greatest need to maintain performance levels and reduce costs. The application proposed here is very competitive because it exploits new ICs to reduce size, number of components and assembly costs.

This solution, the DC-DC converter, compares very favourable with off-line switching supplies in terms of cost. DC-DC converters can, in fact, be realized even by designers with little experience and allows the convenience of working with low voltages, Off-line switching supplies are only preferable when the weight and size of the mains transformer in a DC-DC converter would be excessive.

In this circuit, figure 6 two devices are used, an L296 and an L4960. The L296 is used, to supply a 5V output with a current of 3A and the auxiliary -5V/100mA output and the L4960 is used to provide the 12V/1.5A output and the auxiliary -12V/100mA output.

Fig. 6 - Multioutput DC-DC converter with L296 and L4960 (5V/3A, 12V/1.5A, -12V/100mA, -5V/100mA)

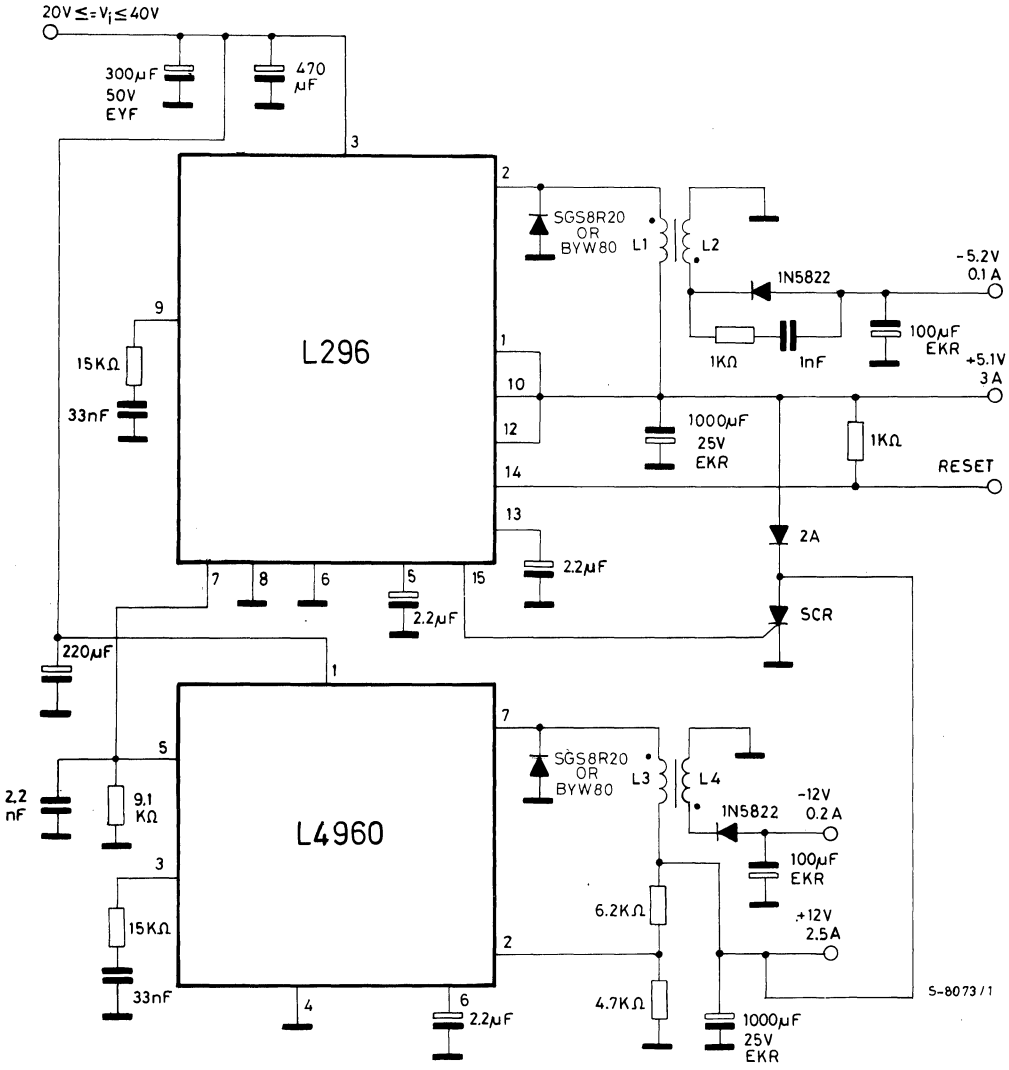
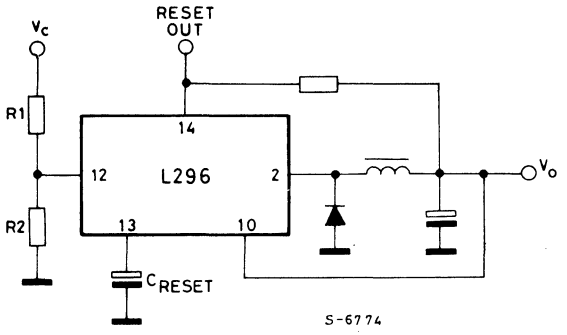


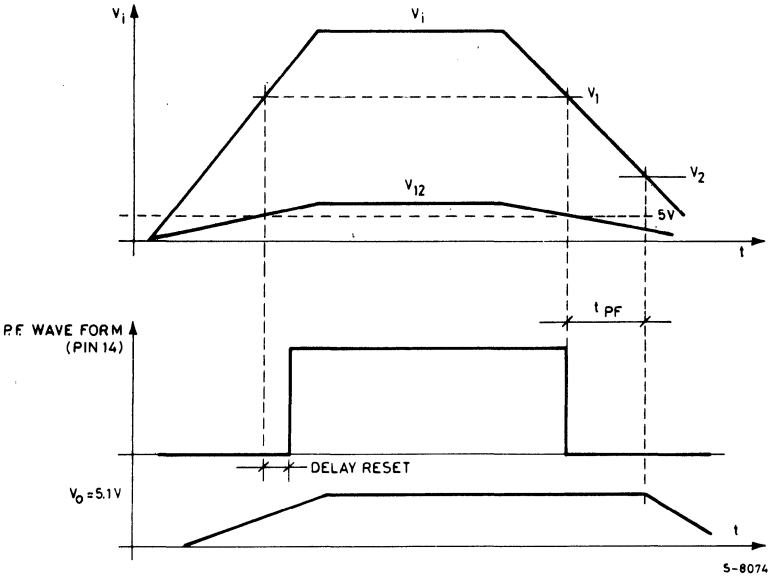
Fig. 8



CALCULATING THE POWER FAIL TIME

The 'power fail time' is defined as the time from when the power fail output (pin 14) goes low to the time when the input voltage falls to the minimum level required to maintain the regulated output (see Figure 9). From this definition we can evaluate the energy balance.

Fig. 9



The energy which the filter capacitor C supplies to the operating device while it discharges is:

$$E = 1/2C\,(V_1^2 - V_2^2) \qquad (1)$$

The load drains a power of $P_o = V_o I_o$. Taking into consideration the average efficiency η (derived with the input between V_1 and V_2), the power to be supplied at the input of the device is:

$$P_{o2} = \frac{P_o}{\eta} \qquad (2)$$

Equating the expressions (1) and (2) gives:

$$1/2C\,(V_1^2 - V_2^2) = \frac{P_o}{\eta} \cdot t_{PF}$$

where V_1 is the input voltage at which the voltage on pin 12 reaches 5V (through the divider R_1/R_2); V_2 is the maximum input voltage below which the device no longer regulates.

Rearranging this expression to obtain C:

$$C = \frac{2\,P_o\,t_{PF}}{\eta\,(V_1^2 - V_2^2)}$$

DUAL REGULATORS SIMPLIFY MICRO SYSTEM SUPPLY DESIGN

Combining two 5V regulators and a reset circuit on a single chip, special purpose regulator chips simplify the design of power supplies for microprocessor systems incorporating battery backup RAMs or shadow-type NV RAMs.

Power supplies for microprocessor systems are often complicated by the need to take care of the special requirements of non-volatile read/write memory. Where battery backup CMOS RAMs are used, for example, it is important to ensure that the RAMs are disabled when the primary supply is removed. And when shadow-type NV memory is included the backup transfer must be initiated and completed when the supply is interrupted. Designed specifically for such applications, the SGS L4901, and L4902 dual voltage regulators combine two 5V regulators plus a reset circuit on a single chip, simplifying the designer's task.

Assembled in the SGS Heptawatt [TM] 7-lead package, the L4901 and L4902 contain separate voltage regulators rated at 5V/300mA (the "V1" output) and 5V/400mA (the "V2" output).

Both the V1 and V2 regulators have an output voltage precision of ± 2% and include protection against output short circuits and 60V input transients. Also included on the chip is a reset circuit with externally programmable timing which depends on the input voltage and the output of the V1 regulator.

Functionally, the two devices are identical except that the L4901 has separate inputs to the two regulators and the L4902 has a common input plus a disable input which controls the V2 output. (Fig. 1)

Generally the V1 regulator is used to supply circuits which must be powered continuously — volatile memory, a time-of-day clock and so on — while the V2 output supplies other 5V circuits which may be powered down when the equipment is inactive.

The V1 output features a very low leakage current at the output — less than 1μA — to allow the use a backup battery. The V1 regulator also features a low quiescent current at the input (0.6mA typical) to minimize battery drain in applications where the V1 regulator is permanently connected to a battery supply.

Fig. 1a - TWO 5V OUTPUTS — The L4901 Dual Regulator provides 300mA and 400mA 5V outputs and includes a microprocessor reset function. This device is ideal for microprocessor systems with battery backup or shadow RAM.

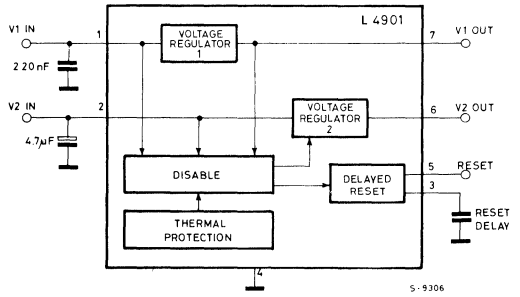


Fig. 1b - DISABLE INPUT — The L4902 is similar to the L4901 but also features a disable input for the V2 regulator.

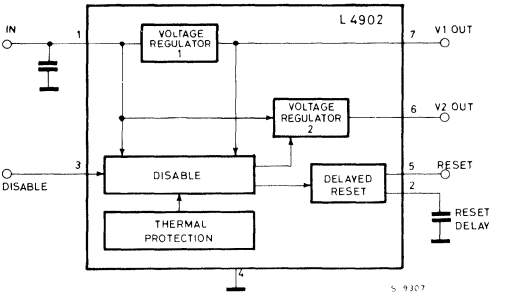


Fig. 4 - LOW LEAKAGE at the V1 output makes the L4901 ideal for battery backup operation.

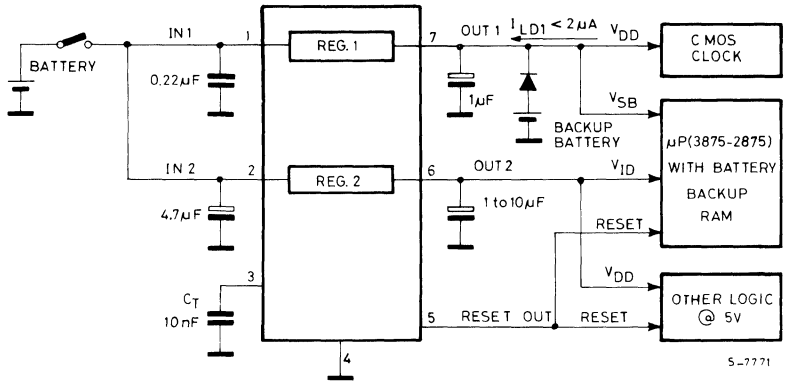
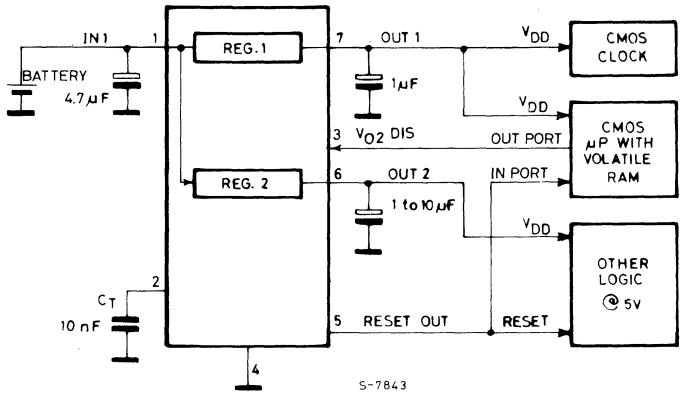


Fig. 5 - STANDBY — The L4902 can be used in applications where the supply is connected permanently and the disable function used to turn off non-essential circuits in the standby state.



It is important to make sure that the RAMs are disabled because the lithium cells used as backup batteries have a high internal resistance. If the RAMs were not forced into the low consumption standby state the battery voltage could drop so low that memory contents are corrupted. Moreover, to prevent latch up, no input of a CMOS RAM should ever be higher than the supply voltage.

IDEAL FOR SHADOW MEMORIES

Another interesting application for the L4902 is supplying a shadow-ram microcomputer chip like the SGS M38SH72 where a fast non-volatile memory is backed up on-chip by a slow EEPROM (figure 7). For these chips it is important to ensure that the backup command is generated when the supply is removed, a function which the L4902's reset output can perform. Since the L4902's reset function depends on the INPUT voltage the power fail condition is sensed early enough to guarantee that the backup transfer will be successful.

In figure 7 the reset output is forced low when the input voltage falls below 6.3V or when the V1 output goes below 4.8V. This allows 10µs for the backup transfer (with 10µF capacitors) which is more than sufficient.

Similarly, the L4902 can be used with shadow-type RAMs such as the Xicor X2201. In the figure 8 circuit a capacitor on the V1 input ensures that the X2201 is powered during the transfer operation. When the input voltage is removed or goes below 6.3V the L4902's reset output, connected to

Fig. 8 - SHADOW RAMs — The L4901's reset function also serves in systems using shadow type NV RAMs like the X2201 to ensure that the backup transfer is executed correctly.

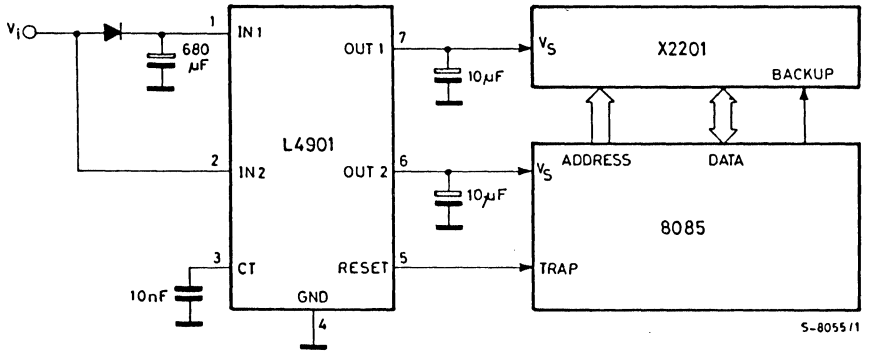
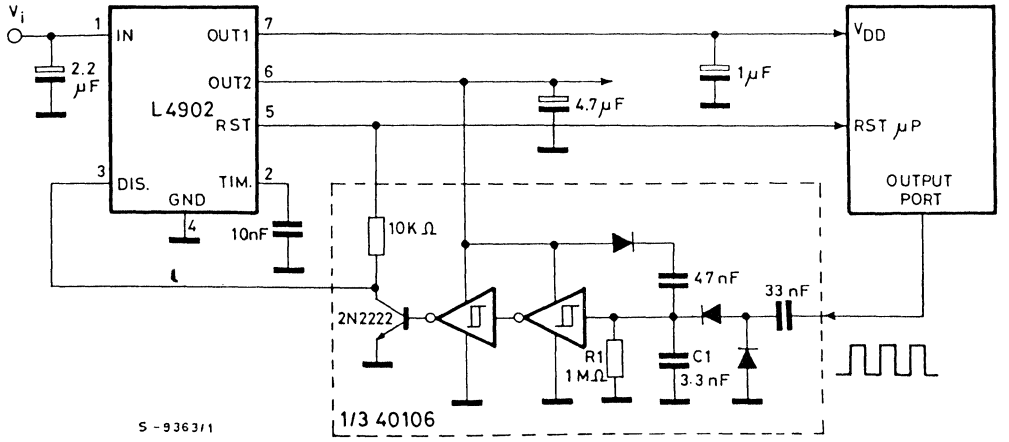


Fig. 9 - With a CMOS Schmitt trigger and a few components a watchdog function can be added for critical applications.



UC3842 PROVIDES LOW-COST CURRENT-MODE CONTROL

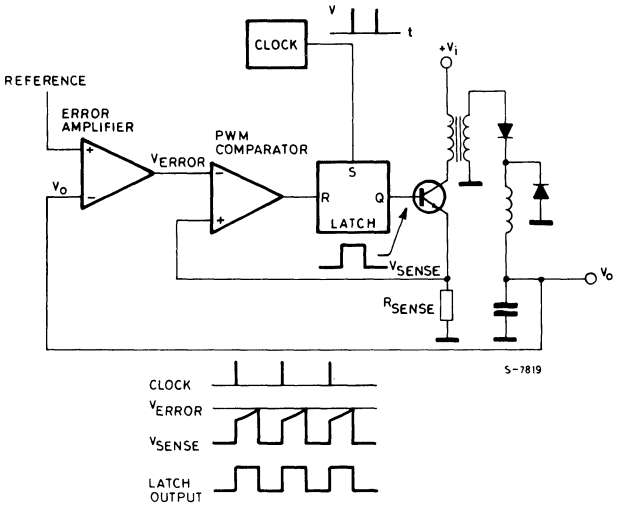
The fundamental challenge of power supply design is to simultaneously realize two conflicting objectives: good electrical performance and low cost. The UC3842 is an integrated pulse width modulator (PWM) designed with both these objectives in mind. This IC provides designers an inexpensive controller with which they can obtain all the performance advantages of current-mode operation. In addition, the UC3842 is optimized for efficient power sequencing of off-line converters and for driving increasingly popular POWERMOS.

This application note gives a functional description of the UC3842 and suggests how to incorporate the IC into practical power supplies. A review of current-mode control and its benefits is included and methods of avoiding common pitfalls discussed. The final section presents designs of two power supplies utilizing UC3842 control.

CURRENT-MODE CONTROL

Figure 1 shows the two-loop current-mode control system in a typical buck regulator application. A clock signal initiates power pulses at a fixed frequency. The termination of each pulse occurs when an analog of the inductor current reaches a threshold established by the error signal. In this way the error signal actually controls peak inductor current. This contrasts with conventional schemes in which the error signal directly controls pulse width without regard to inductor current.

Fig. 1 - Two-loop current-mode control system



Current limiting is simplified with current-mode control. Pulse-by-pulse limiting is, of course, inherent in the control scheme. Furthermore, an upper limit on the peak current can be established by simply clamping the error voltage. Accurate current limiting allows optimization of magnetic and power semiconductor elements while ensuring reliable supply operation.

Finally, current-mode controlled power stages can be operated in parallel with equal current sharing. This opens the possibility of a modular approach to power supply design.

FUNCTIONAL DESCRIPTION

A block diagram of the UC3842 appears in Figure 4. This IC will operate from a low impedance DC source of 10V to 30V. Operation between 10V and 16V requires a start-up bootstrap to a voltage greater than 16V in order to overcome the under-voltage lockout. V_{cc} is internally clamped to 34V for operation from higher voltage current-limited sources ($I_{cc} \leq 30mA$).

Under-Voltage Lockout (UVLO)

This circuit insures that V_{cc} is adequate to make the UC3842 fully operational before enabling the output stage. Figure 5a shows that the UVLO turn-on and turn-off thresholds are fixed internally at 16V and 10V respectively. The 6V hysteresis prevents V_{cc} oscillations during power sequencing. Figure 5b shows supply current requirements. Start-up current is less than 1mA for efficient bootstrapping from the rectified input of an off-line converter, as illustrated by Figure 6. During normal circuit operation, V_{cc} is developed from auxiliary winding W_{AUX} with D_1 and C_{IN}. At start-up, however, C_{IN} must be charged to 16V through R_{IN}. With a start-up current of 1mA, R_{IN} can be as large as 100kΩ and still charge C_{IN} when V_{AC} = 90V RMS (low line). Power dissipation in R_{IN} would then be less than 350mW even under high line (V_{AC} = 130V RMS) conditions.

During UVLO, the UC3842 output driver is biased to a high impedance state. However, leakage currents (up to 10μA), if not shunted to ground, could pull high the gate of a POWERMOS. A 100kΩ shunt, as showing in Figure 6, will hold the gate voltage below 1V.

Fig. 5 (a) - Under-voltage lockout and (b) supply current requirements.

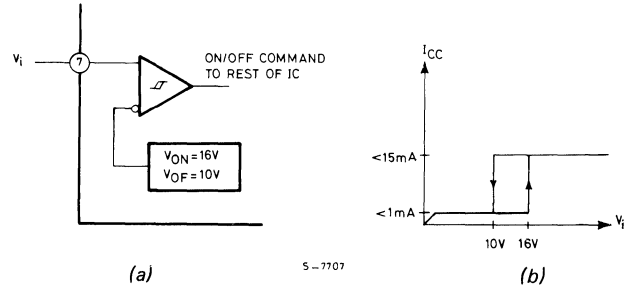
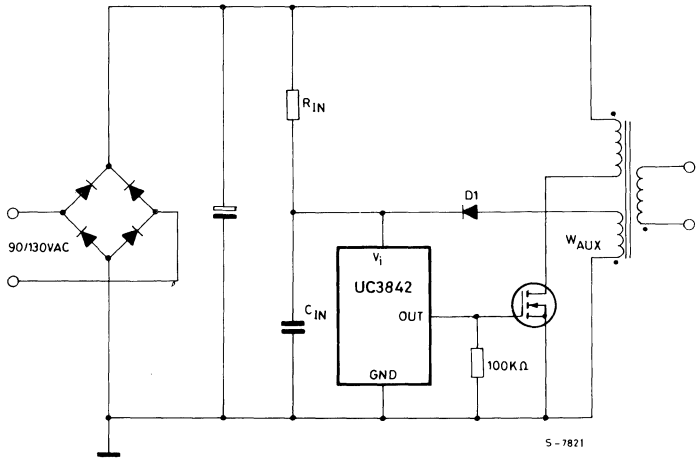


Fig. 6 - Providing power to the UC3842



unity (0dB) at f ≈ $f_{switching}/4$. This technique insures converter stability while providing good dynamic response.

Continuous-inductor-current boost and flyback converters each have a right-half-plane zero in their transfer function. An additional compensation pole is needed to roll off loop gain at a frequency less than that of the RHP zero. R_p and C_p in the circuit of Figure 10b provide this pole.

The E/A output will source 0.5mA and sink 2mA. A lower limit for R_f is given by:

$$R_{f(MIN)} \approx \frac{V_{E/A\ OUT(MAX)} - 2.5V}{0.5mA} = \frac{6V - 2.5V}{0.5mA} = 7k\Omega$$

E/A input bias current (2μA max) flows through R_i, resulting in a DC error in output voltage (V_O) given by:

$$\Delta V_{O(MAX)} = (2\mu A)\, R_i$$

It is therefore desirable to keep the value of R_i as low as possible.

Figure 11 shows the open-loop frequency response of the UC3842 E/A. The gain represent an upper limit on the gain of the compensated E/A. Phase lag increases rapidly as frequency exceeds 1MHz due to second-order poles at ~ 10MHz and above.

Fig. 9 - UC3842 error amplifier

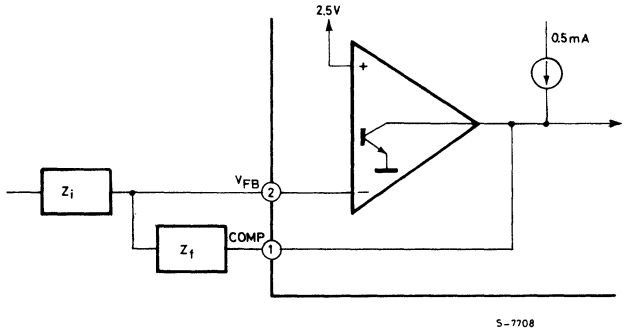


Fig. 10 - (a) Error amplifier compensation addition pole and (b) needed for continuous inductor-current boost ad flyback.

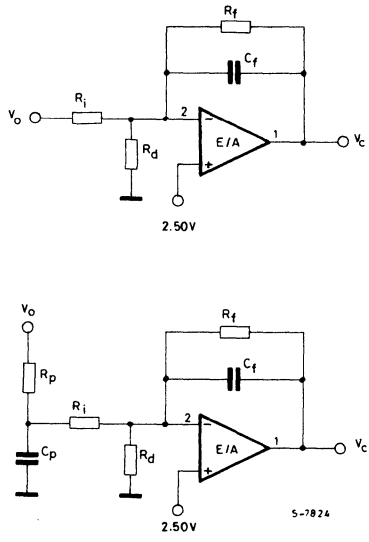
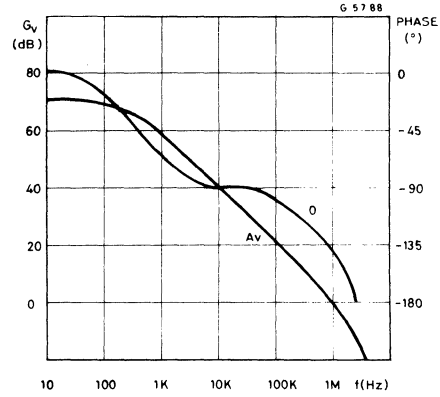


Fig. 11 - Error amplifier open-loop frequency response



Current Sensing and Limiting

The UC3842 current sense input is configured as shown in Figure 12. Current-to-voltage conversion is done externally with ground-referenced resistor R_S. Under normal operation the peak voltage across R_S is controlled by the E/A according to

Figures 15-17 show suggested circuits for driving POWERMOS and bipolar transistors with the UC3842 output. The simple curcuit of Figure 15 can be used when the control IC is not electrically isolated from the power MOS. Series resistor R_1 provides damping for a parasitic tank circuit formed by the power MOS input capacitance and any series wiring inductance. Resistor R_2 shunts output leakage currents (10μA maximum) to ground when the under-voltage lockout is active. Figure 16 shows an isolated power MOS drive circuit which is appropriate when the drive signal must be level-shifted or transmitted across an isolation boundary. Bipolar transistors can be driven effectively with the circuit of Figure 17. Resistors R_1 and R_2 fix the on-state base current. Capacitor C_1 provides a negative base current pulse to remove stored charge at turn-off.

Fig. 15 – Direct POWERMOS drive

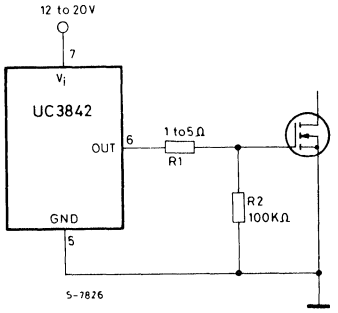


Fig. 16 – Isolated POWERMOS drive

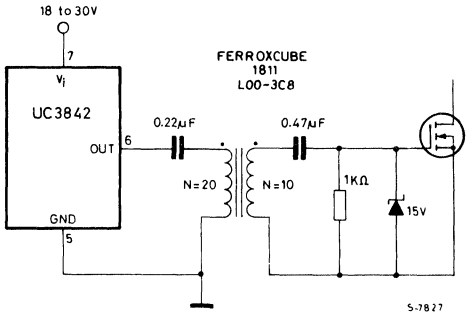
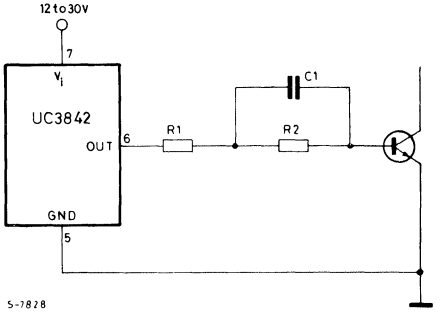


Fig. 17 – Bipolar drive with negative turn-off bias



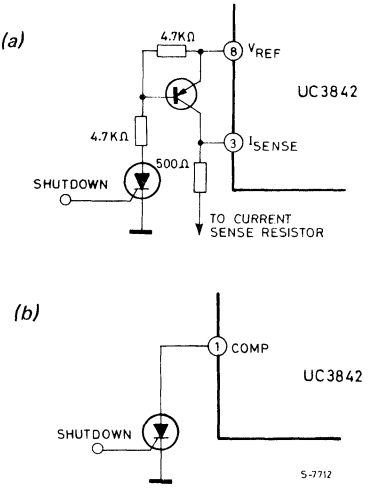
PWM Latch

This flip-flop, shown in Figure 4, ensures that only a single pulse appears at the UC3842 output in any one oscillator period. Excessive power transistor dissipation and potential saturation of magnetic elements are thereby averted.

Shutdown Techniques

Shutdown of the UC3842 can be accomplished by two methods; either raise pin 3 above 1V or pull pin 1 below 1V. Either method causes the output of the PWM comparator to be high (refer to block diagram, Figure 4). The PWM latch is reset dominant so that the output will remain low until the first clock pulse following removal of the shutdown signal at pin 1 or pin 3. As shown in Figure 18, an externally latched shutdown can be accomplished by adding an SCR which will be reset by cycling V_{CC} below the lower under-voltage lockout threshold (10V). At this point all internal bias is removed, allowing the SCR to reset.

Fig. 18 – Shutdown achieved by
a) Pulling pin 3 high
b) Pulling pin 1 Low



AVOIDING COMMON PITFALLS

Current-mode controlled converters can exhibit performance peculiarities under certain operating conditions. This section explains these situations and how to correct them when using the UC3842.

Slope Compensation Prevents Instabilities

It is well documented that current-mode controlled converters can exhibit subharmonic oscillations

Note that in order for the error amplifier to accurately replicate the ramp, Z_F must be constant over the frequency range f_s to at least $3f_s$.

In order to eliminate this last constraint, an alternative method of slope compensation is shown in Figures 19c and 20b. Here the artificial slope is added to the current sense waveform rather than subtracted from the control signal. The magnitude of the added slope still relates to the downslope of inductor current as described above. The requirement for R_{SLOPE} is now:

$$m = \frac{\Delta V_{RAMP}}{\Delta t_{RAMP}}\left(\frac{R_f}{R_f + R_{SLOPE}}\right) = \frac{0.7}{\tau/2}\left(\frac{R_f}{R_f + R_{SLOPE}}\right)$$

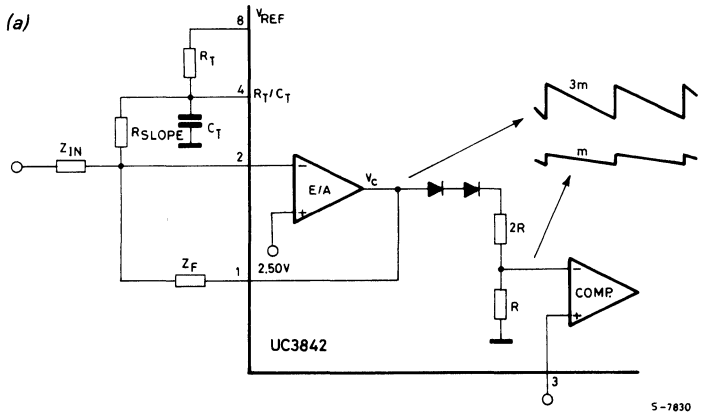
$$R_{SLOPE} = \frac{1.4\,R_f}{m\tau} - R_f = R_f\left(\frac{1.4}{m\tau} - 1\right)$$

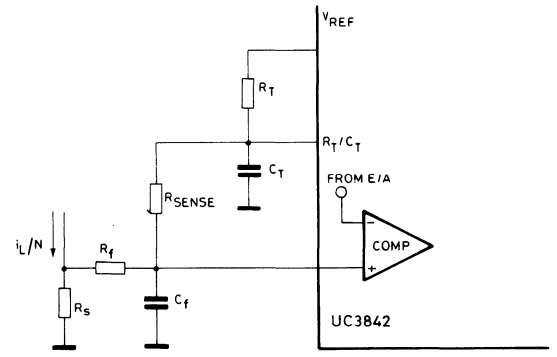
For $m = m_2$:

$$R_{SLOPE} = R_f\left(\frac{1.4NL}{R_S\,(V_F + V_O)\,\tau} - 1\right)$$

R_{SLOPE} loads the UC3842 R_T/C_T terminal so as to cause a decrease in oscillator frequency. If $R_{SLOPE} >> R_T$ then the frequency can be corrected by decreasing R_T slightly. However, with $R_{SLOPE} \lesssim 5R_T$ the linearity of the ramp degrades noticeably, causing over-compensation of the supply at low duty cycles. This can be avoided by driving R_{SLOPE} with an emitter-follower as shown in Figure 21.

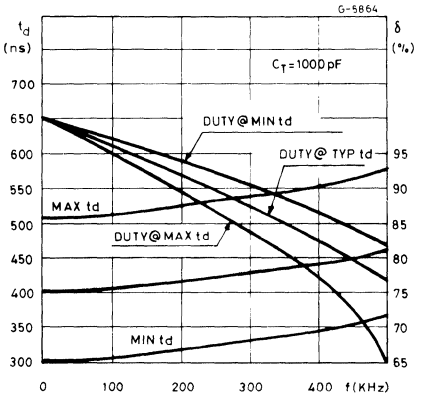
Fig. 20 - Slope compensation added (a) to control signal or (b) to current sense waveform





The speed of the UC3842 current sense section poses an additional constraint on maximum operating frequency. A maximum current sense delay of 400ns represents 10% of the switching period at 250kHz and 20% at 500kHz. Magnetic components must not saturate as the current continues to rise during this delay period, and power semiconductors must be chosen to handle the resulting peak currents. In short, above ~250kHz, may of the advantages of higher-frequency operation are lost.

Fig. 23 - Deadtime and maximum obtainable duty-cycle vs. frequency with minimum recommended C_T.



CIRCUIT EXAMPLES

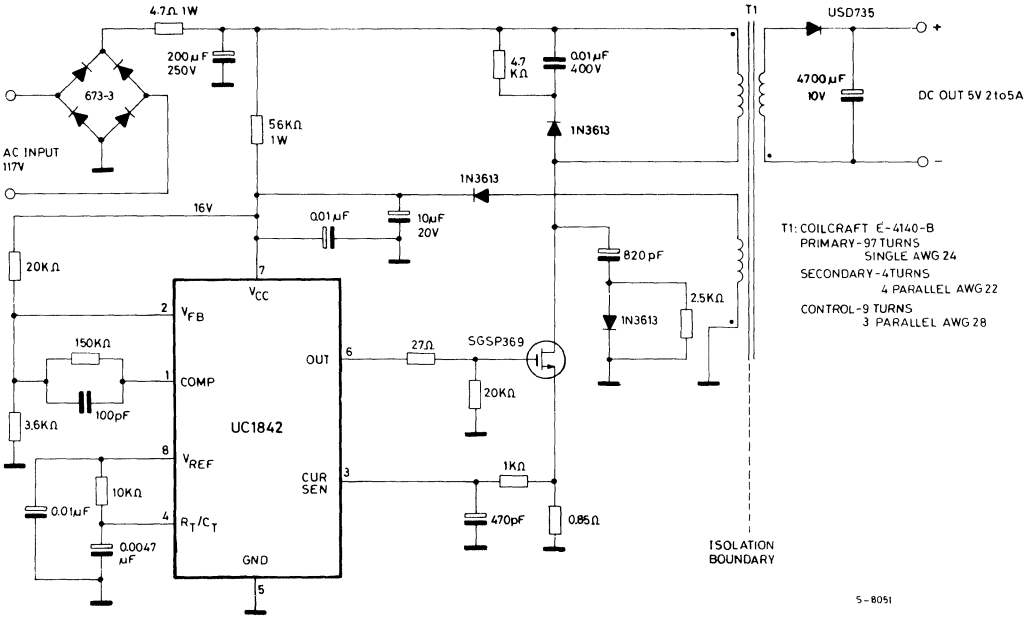
1. Off-Line Flyback

Figure 24 shows a 25W multiple-output off-line flyback regulator controlled with the UC3842. This regulator is low in cost because it uses only two magnetic elements, a primary-side voltage sensing technique, and an inexpensive control circuit. Specifications are listed below.

SPECIFICATIONS:

Input Voltage	95 VAC to 130 VAC (50Hz/60Hz)
Output Voltage:	A. +5V, 5%: 1A to 4A load Ripple voltage: 50mV P-P Max.
	B. +12V, 3% : 0.1A to 0.3A load Ripple voltage: 100mV P-P Max
	C. -12V, 3% 0.1A to 0.3A load Ripple voltage: 100mV P-P Max
Line Isolation:	3750V
Switching Frequency:	40kHz
Efficiency @ full load:	70%

Fig. 24 - 25W off-line flyback regulator



A 25W OFF-LINE FLYBACK SWITCHING REGULATOR

INTRODUCTION

This note describes a low cost switching power supply for applications requiring multiple output voltages, e.g. personal computers, instruments, etc. . . The discontinuous mode flyback regulator used in this application provides good voltage tracking between outputs, which allows the use of primary side voltage sensing. This sensing technique reduces costs by eliminating the need for an isolated secondary feedback loop.

The low cost, (8 pin) UC1842 current mode control chip employed in this power supply provides performance advantages such as:

1) Fast transient response
2) Pulse by pulse current limiting
3) Stable operation

To simplify drive circuit requirements, a TO-220 power MOS SGSP369 is utilized for the power switch. This switch is driven directly from the output of the control chip.

Power Supply Specifications

1. Input voltage: 95VAC to 130VAC (50Hz/60Hz)
2. Output voltage:
   A. +5V, ± 5%: 1A to 4A load
      Ripple voltage: 50mV P-P Max
   B. +12V, ± 3%: 0.1A to 0.3A load
      Ripple voltage: 100mV P-P Max
   C. -12V, ± 3%: 0.1A to 0.3A load
      Ripple voltage: 100mV P-P Max.
3. Line Isolation: 3750V
4. Switching Frequency: 40KHz
5. Efficiency @ Full Load: 70%

Basic Circuit Operation

The 117VAC input line voltage is rectified and smoothed to provide DC operating voltage for the circuit. When power is initially applied to the circuit, capacitor C2 charges through R2. When the voltage across C2 reaches a level of 16V the output of IC1 is enabled, turning on power MOS Q1.

During the on time of Q1, energy is stored in the air gap of transformer (inductor) T1. At this time the polarity of the output windings is such that all output rectifiers are reverse biased and no energy is transferred. Primary current is sensed by a resistor, R10, and compared to a fixed 1V reference inside IC1. When this level is reached, Q1 is turned off and the polarity of all transformer windings reverses, forward biasing the output rectifiers. All the energy stored is now transferred to the output capacitors. Many cycles of this store/release action are needed to charge the outputs to their respective voltages. Note that C2 must have enough energy stored initially to keep the control circuitry operating until C4 is charged to a level of approximately 13V. The voltage across C4 is fed through a voltage divider to the error amplifier (pin 2) and compared to an internal 2.5V reference.

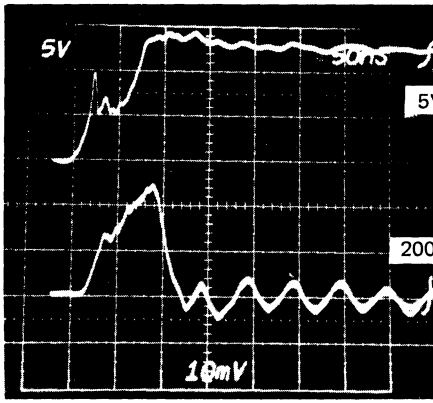
Energy stored in the leakage inductance of T1 causes a voltage spike which will be added to the normal reset voltage across T1 when Q1 turns off. The clamp consisting of D4, C9 and R12 limits this voltage excursion from exceeding the BVDSS rating of Q1. In addition, a turn-off snubber made up of D5, C8 and R11 keeps power dissipation in Q1 low by delaying the voltage rise until drain current has decreased from its peak value. This snubber also damps out any ringing which may occur due to parasitics.

Less than 3.5% line and load regulation is achieved by loading the output of the control winding Nc, with R9. This resistor dissipates the leakage energy associated with this winding. Note that R9 must be isolated from R2 with diode D2, otherwise C2 could not charge to the 16V necessary for initial start-up.

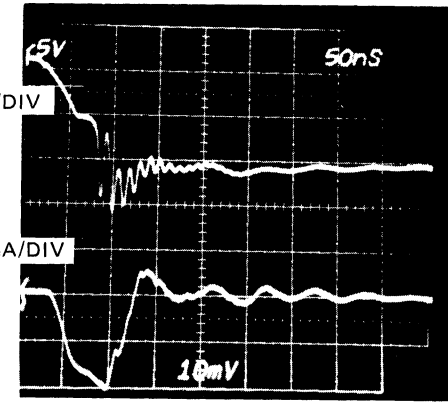
A small filter inductor in the 5V secondary is added to reduce output ripple voltage to less than 50mV. This inductor also attenuates any high frequency noise.

TYPICAL SWITCHING WAVEFORMS

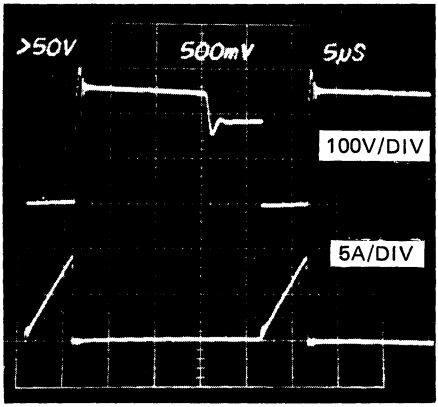
T_{on} - Drive waveforms



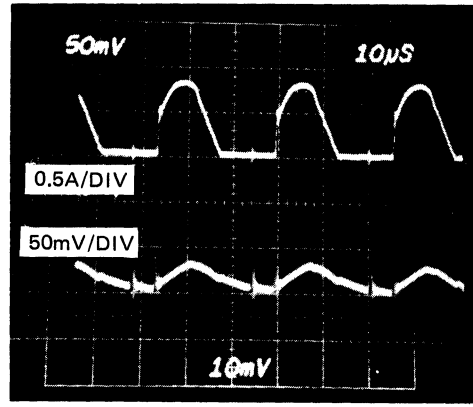
T_{off} - Drive waveforms



Upper trace: Q_1 - Gate to source voltage
Lower trace: Q_1 - Gate current



Upper trace: Q_1 - Drain to source voltage
Lower trace: Primary current - I_D



Upper trace: +5V charging current
Lower trace: +5V output ripple voltage

APPLYING THE UC1840 TO PROVIDE TOTAL CONTROL FOR LOW-COST, PRIMARY-REFERENCED SWITCHING POWER SYSTEMS

INTRODUCTION

There are many potential approaches to be considered in switch mode power supply design; however, the contradictory requirements of minimum cost and compatibility with ever more demanding line isolation specifications make primary control very attractive. Application of the UC1840 as a primary-side, off-line controller presents an extremely cost-effective approach to supplying isolated power from a widely varying input line while maintaining a high degree of efficiency.

Primary control means referencing all of the control electronics along with the power switching device on the input line side of an isolation transformer. An obvious advantage to this approach is the simplified interface between the control and

Fig. 1 - The overall block diagram of the UC1840, an integrated circuit optimized for primary-side control of off-line switching power supplies.

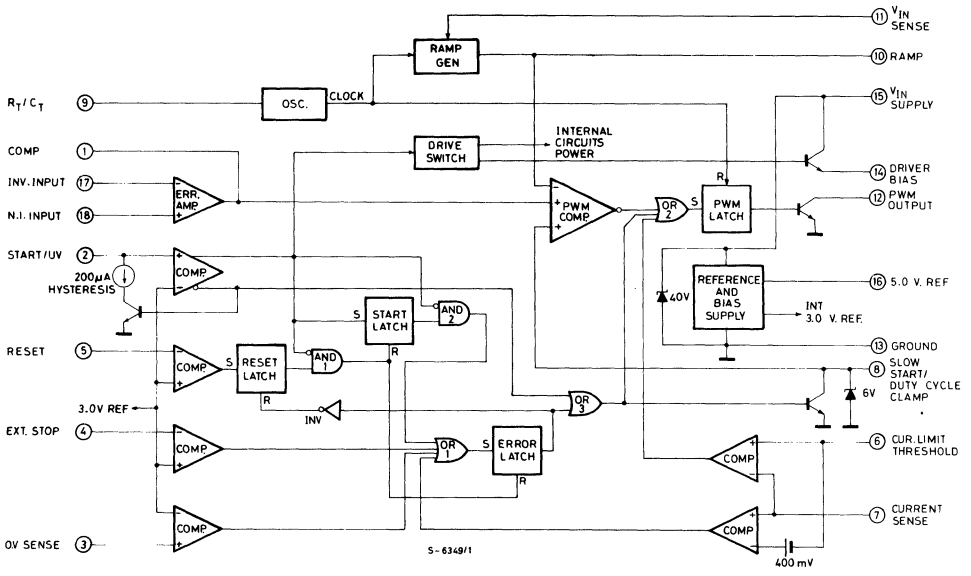
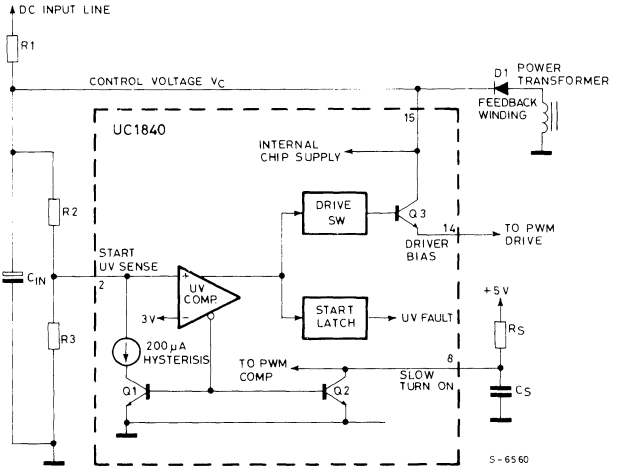


Fig. 3 - The UC1840's start circuitry requires low starting current from the DC input line with normal operating current supplied from a low-voltage feedback winding on the power transformer.



(1) While the control voltage, V_C, is low enough so that the voltage on pin 2 is less than 3V, the Start/UV Comparator does the following:

(a) A 200μA hysteresis current is flowing into pin 2 through Q1 causing an added drop across R2.

(b) The drive switch is holding the Driver Bias transistor, Q3, OFF. This insures that the only current required through R1 is the start-up current of the UC1840, plus external dividers (R2, R3, R_S, etc.).

(c) The Slow Turn-on transistor, Q2, is ON, holding pin 8 and C_S low.

(d) The Start Latch keeps the under-voltage signal from being defined as a fault.

(2) The start level is defined by:

$$V_C \text{ (start)} = 3 \left(\frac{R2 + R3}{R3}\right) + 0.2\ R2.$$

When V_C rises to this level, the Start/UV. Comparator then does the following:

(a) Turns off Q1, eliminating the 200μA hysteresis current. This allows the voltage on V_C to drop before reaching the under-voltage fault level defined by:

$$V_C \text{ (U.V. fault)} = 3 \left(\frac{R2 + R3}{R3}\right)$$

(b) Sets the Start Latch to monitor for an under-voltage fault.

(c) Activates Q3 providing Driver Bias to the power switch, pulling the added current out of C_{IN}.

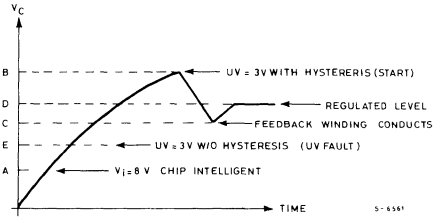
(d) Turns off Q2 allowing for programmed slow turn-on defined by R_S and C_S.

(3) A normal start-up occurs with the control voltage, V_C, following the path shown in Figure 4. If the power supply does not start, V_C will fall to an under-voltage fault which will then either initiate a restart attempt or hold the power switch off, depending upon the status of the Reset terminal as defined under Fault Sequencing. If start-up does not occur because of some fault in the Driver Bias line, V_C will continue to rise until the 40V zener across the reference circuit conducts. This will then clamp V_C to that level, protecting the control chip.

After start-up occurs, current will continue to flow in R1 providing a power loss of:

$$Pd = \frac{(V_{line} - V_C)^2}{R1}$$

Fig. 4 - Under a normal turn-on, the supply voltage to the UC1840, V_C, would rise lightly loaded to the start level, fall under the turn-on load, and then regulate at some intermediate level.



by connecting R_S to the DC input line. The divider voltage:

$$V_{Pin\ 8} = \left(\frac{R_{DC}}{R_S + R_{DC}}\right) V_{DC\ input}$$

should be equal to the ramp voltage level that yields the desired maximum duty cycle, at the same DC input level.

PWM control

Pulse-Width Modulation within the UC1840 consists of the blocks shown in Figure 7. This architecture, with the possible exception of the separation between the time-base and ramp functions, is fairly conventional. It is described in greater detail in the paragraphs which follow.

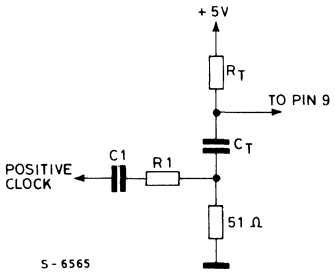
Oscillator

A constant clock frequency is established by connecting R_T from pin 9 to the 5V reference and C_T from pin 9 to ground. The frequency is approximated by:

$$f \approx \frac{1}{R_T\ C_T}$$

where the value of R_T can range from 1 kΩ to 100KΩ and C_T from 300pF to 0.1μF. The best temperature coefficients occur with C_T in the range of 1000 to 3000 pF. Although the clock output pulse is not available external to the UC1840, synchronization to an external clock can still be accomplished with the circuit of Figure 8, where R1 and C1 are selected to provide a 0.5V, 200 ns pulse across the 51Ω resistor, and R_T and C_T define a frequency slightly lower than the synchronizing source.

Fig. 8 - Synchronization to an external time base can be accomplished by adding a 51Ω resistor in series with C_T.

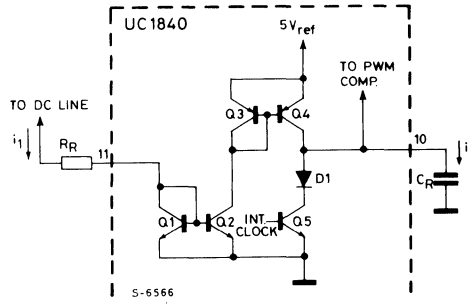


To achieve minimum start-up current, the oscillator is not activated until the input voltage is high enough to give a start command to the drive switch.

Ramp generator

The ramp generator function of the UC1840 is shown in simplified form in Figure 9.

Fig. 9 - Current mirrors Q1-Q4 are used to make the ramp charging current i_2, linearly proportional to the DC input line.



The NPN and PNP current mirrors provide a charging current to C_R of:

$$i_2 = i_1 = \frac{V_{line} - 0.7V}{R_R} \cong \frac{V_{line}}{R_R}$$

The current mirrors are useful over a current range of 1μA to 1mA, but optimum tracking occurs between 30μA and 300μA. Since the voltage across Q1 is very small, i_2 accurately represents the input line voltage. The ramp slope, therefore, is:

$$\frac{dv}{dt} = \frac{V_{line}}{R_R\ C_R}$$

The peak voltage across C_R is clamped to approximately 4.2V while the valley, or low voltage, is determined by the on-voltage of the discharge network, D1 and Q5. This is typically 0.7V.

If line sensing is not required, R_R should be connected to the 5V reference for constant ramp slope.

Error amplifier

This is a voltage-mode operational amplifier with an uncommitted NPN differential input stage and an output configuration as shown in Figure 10.

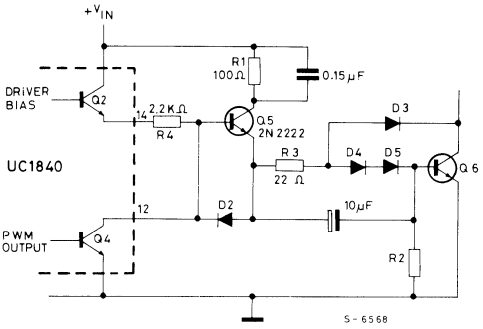
The 1KΩ output resistor, R_O, is used both for short circuit protection and to limit the peak output voltage to less than 4.0V so it cannot rise above the clamped ramp waveform. At sink currents less than 300 μA, the low output level will be within 200mV of ground but it rises to 1V at higher current levels.

The input common mode range is from 1V to within 2V of the input supply voltage. V_{in}, and thus either input can be connected directly to the 5V reference.

At the same time Q2 turns on, the clamping transistor at the slow-start terminal, pin 8, turns off allowing the voltage on pin 8 to rise according to the external slow-start time constant described earlier. This allows PWM pulses to begin to activate Q4 – narrow at first and widening to the point where the error amplifier takes command.

The interface between the UC1840 and the primary power switch may be implemented in several different ways to meet varying system requirements. One obvious application is when the use of a bipolar transistor switch requires more drive current than the Driver Bias output can provide. Figure 13 shows a more typical bipolar drive scheme where Q5 has been added to boost the turn-on current with the UC1840 still providing the high speed turn-off. The circuit now serves as a more efficient "totem-pole" driver since Q5 turns off when Q4 conducts. It also illustrates the use of a Baker Clamp to minimize storage time in Q6 and the capacitors for rapid turn-on and high-current pulse turn-off.

Fig. 13 - Adding Q5 as a switched, drive-boost transistor provides added base drive for Q6 while reducing the steady-state current through both Q2 and Q4.

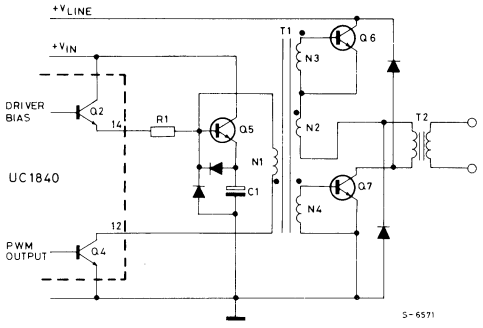


Another application is the two-transistor, off-line, forward converter topology shown in Figure 14. This circuit uses proportional base drive where the UC1840 need only supply a short, turn-off current pulse with transformer regeneration through T1 providing the steady-state drive. The magnetizing current is controlled by R1, with Q5 added to rapidly recharge C1 from which the turn-off current is supplied.

Fault protection

A significant benefit in using the UC1840 is the multi-faceted fault-sensing and programming capability built into the device. With the intent to provide complete control to the power system under all types of potential malfunctions, fault-sensing circuitry has been included to sense over-voltage, under-voltage, or over-current conditions. Additionally, high-speed, pulse-by-pulse digital current limiting is included as a separate function. The operation of these circuits is described below.

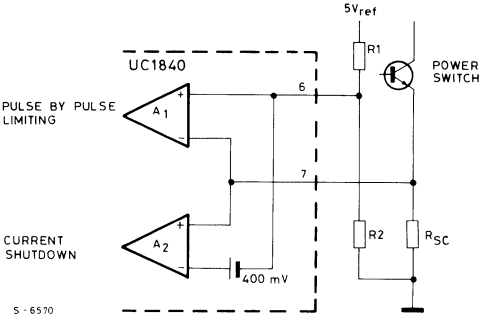
Fig. 14 - Interfacing the UC1840 single PWM output to a two-transistor off-line forward converter which uses proportional base drive.



Current limiting

The current limit comparators have differential inputs for noise rejection but are intended to be used with ground-referenced current sensing as in Figure 15. Comparator A1 is delegated to pulse-by-pulse current limiting. The output of this comparator drives the PWM comparator, where it activates the PWM latch, terminating each pulse when the current sensed by R_{SC} reaches a threshold defined by divider R1, R2, and the 5V reference.

Fig. 15 - Current limiting and overcurrent shutdown are implemented with comparators of different thresholds and a single current sense resistor.

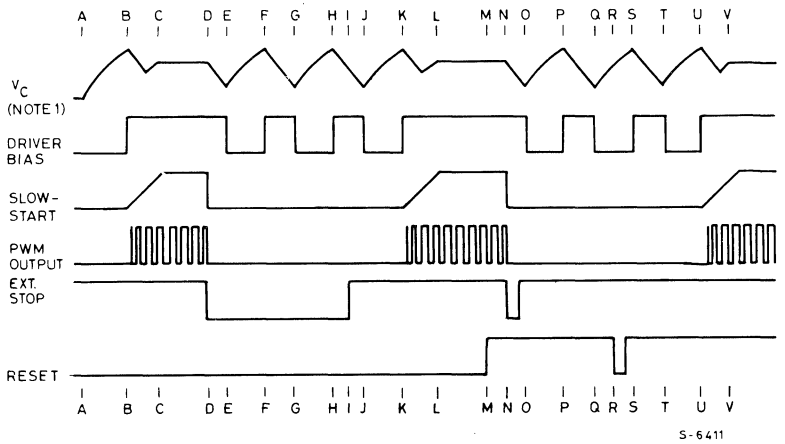


state commanded by pin 5: high if pin 5 is low and vice-versa. The latch allows merely a pulse to set the Reset Latch; the voltage on pin 5 need not be steady state.

With a high Reset Latch output, the Error Latch still does not reset until a low signal is sensed on the Start/UV sense terminal. At that point, AND1 then resets both the Error Latch and the Start Latch re-establishing the initial conditions for a normal start after fully charging the input capacitor. Of course, if the fault is still present, when the Start/UV input reaches the start level terminating the Error Latch reset signal, this latch will immediately set again.

To aid in the understanding of this logic, Figure 17 gives a pictorial representation of its operation with both steady-state and momentary signals on both the Ext. Stop and Reset terminals.

Fig. 17 - The interrelationship between the functions controlled by the fault sequence logic is illustrated with both static and pulse commands on the ext. stop and reset terminals.



Note 1: V_C represents an analog of the supply output voltage generated by a primary - referenced secondary winding on the power trasformer. It is the voltage monitored by the start/UV comparator and in most cases is the supply voltage V_{IN} for the UC1840.

TIME	EVENT
A	INITIAL TURN-ON V_C RISES WITH LIGHT LOAD.
B	START THRESHOLD DRIVER BIAS LOADS V_C.
C	OPERATING PWM REGULATES V_C.
D	STOP INPUT SETS. ERROR LATCH TURNING OFF PWM.
E	UV LOW THRESHOLD. ERROR LATCH REMAINS SET.
F	START TURNS ON DRIVER BIAS BUT ERROR LATCH STILL SET.
G	V_C AND DRIVER BIAS CONTINUE TO CYCLE.
H	
I	STOP COMMAND REMOVED.
J	ERROR LATCH RESET AT UV LOW THRESHOLD.
K	START THRESHOLD NOW REMOVES SLOW-START CLAMP.
L	RETURN TO NORMAL RUN STATE.
M	RESET LATCH SET SIGNAL REMOVED.
N	ERROR LATCH SET WITH MOMENTARY FAULT.
O	ERROR LATCH DOES NOT RESET AS RESET LATCH IS RESET.
P	V_C AND DRIVER BIAS RECYCLE WITH NO TURN-ON.
Q	
R	RESET LATCH IS SET WITH MOMENTARY RESET SIGNAL.
S	V_C MUST COMPLETE CYCLE TO TURN ON.
T	START AND ERROR LATCHES RESET.
U	NORMAL START INITIATED.
V	RETURN TO NORMAL RUN STATE.

50W OFF-LINE SWITCHING POWER SUPPLY USING THE UC3840

INTRODUCTION

This power supply has been designed to provide an easy way to gain familiarity with the operating characteristics of the UC3840 PWM Control Circuit in a pratical off-line power supply application. As any switching power supply represents a series of compromises between size, cost, efficiency, performance, and many other variables; no claim is made that this supply optimizes any particular characteristics; only that it provides an easy means to gain an understanding which, hopefully, the designer can use to extrapolate to many specific applications.

This power supply, shown schematically in Fig. 4 implements a 50 watt discontinuous mode flyback power supply with multiple outputs, and features primary-side control with full protection from fault conditions. Additional performance characteristics include simple off-line starting, voltage feed-forward for good line regulation (without feedback across the isolation boundary), pulse-by-pulse current limiting, over- and under-voltage sensing with protective shutdown and automatic restart, and freedom from the need for any circuit adjustments.

For additional information on the operation of the UC3840, reference should be made to TN 168 and data sheet.

DESIGN CONSIDERATIONS

The following description of the design decisions made for this power supply will be with respect to the complete schematic shown in Fig. 4. No significant theoretical discussion is offered and only nominal values are used in the analysis, but hopefully the equations given can be used to either extrapolate to other design problems or to optimize the supply to a particular characteristics.

Input section

Input bridge D1 rectifies the line voltage while resistors R1 and R2 are used to limit the peak charging current to capacitors C1 and C2. The values for C1 and C2 are usually determined by either the ripple voltage allowable for V_{DC} or the minimum hold-up time.
Ripple calculations are worse-case for the 110V voltage doubler configuration where:

RMS line voltage = 90 to 130 VAC
peak no-load input = 253 to 368 volts.

At the minimum line voltage, each capacitor alternately charges to a peak of 126 volts. Allowing for a total input voltage sag at full load of 50 volts, the minimum capacitor voltage must be held to 92 volts. Since each capacitor must provide one-half the energy requirements of the power supply, the required energy for each line cycle is:

$$W_{in} = \frac{\text{Power out}}{\text{Efficiency x Frequency}} = \frac{50}{0.7 \times 60} = 1.2 \text{ Joule}$$

and the capacitor value can be calculated from:

$$\tfrac{1}{2} W_{in} = \tfrac{1}{2} C_1 \ (V_{pk}^2 - V_{min}^2) \text{ or}$$

$$C_1 = \frac{W_{in}}{V_{pk}^2 - V_{min}^2} = \frac{1.2}{126^2 - 92^2} = 162\mu F$$

If, instead of ripple voltage, we choose the input capacitors to hold the input DC above 200 volts for a least two cycles of line drop-out, then:

$$C_1 = \frac{2 (Po/2) \text{ (no. of cycles drop-out) } 1/f}{\text{Efficiency } (V_{pk}^2 - V_{min}^2)}$$

$$= \frac{2 (25) (2) \ 1/60}{0.7 \ (126^2 - 92^2)} = 331\mu F$$

In this application, 470μF was picked as a standard size which would allow loose tolerances.

Transformer

A major task with any flyback power supply is the design of the transformer as many tradeoffs are normally required between regulation, leakage inductance (and corresponding transistor stress), isolation, size, and cost. In this application, the core selected is a Ferrox-cube EC35-3C8 which has the following characteristics:

Effective core area, $A_e = 0.84 \text{ cm}^2$
Max flux density, $B_{sat} = 2800$ gauss
Bobbin = 35 PC B I

The design starts with a calculation of maximum duty cycle which is defined by the voltage capability of the power switch. This voltage was allocated as follows:

VDC max	= 370V
Reset voltage	= 120V
Leakage inductance spike	= 100V
Max total voltage	= 590V

With a reset voltage of 120V, at minimum input voltage,

$$D_{max} = \frac{120V}{120V + 200V} = 37.5\%$$

The primary inductance can then be calculated as:

$$L_p = \frac{\text{Efficiency}}{2 P_o f} (V_{in\ min} \times D_{max})^2 =$$

$$= \frac{0.7 \ (200 \times 0.375)^2}{2 \times 50 \times 40 \times 10^3}$$

$$L_p \approx 1\text{mh}$$

The peak current at full load is:

$$I_p = \frac{2P_o}{\text{eff } (V_{in\ min} \times D_{max})} =$$

$$= \frac{2 \times 50}{0.7 \times 200 \times 0.375} = 1.9A$$

The maximum energy storage requirement within the primary is calculated on the basis of maximum current, in this case assumed to be short circuit current = 120% x I_p or 2.3A.

$$W = \tfrac{1}{2} L \ I_{sc}^2 = \tfrac{1}{2} (1 \times 10^{-3}) (2.3)^2 = 2.65 \text{ m Joule}$$

The equation defining energy storage in an inductor is:

$$W = \tfrac{1}{2} \frac{B A_c H \ell_e \times 10^{-8}}{0.4\pi} \text{ Joules}$$

start-up signal, the Drive Bias transistor in the UC3840 is off insuring that there is no quiescent current being drawn by any of this interface circuitry. At start-up, the Drive Bias switch turns on providing a pull-up for the UC3840's PWM output. The current through R16 is multiplied by the gain of Q1 to provide a forward base drive in excess of 250mA for the power switch Q3. Diodes D5 and D6 form a Baker clamp to keep Q3 out of hard saturation and improve turn-off, especially al lower collector currents.

Transistor Q2, driven on by the turn-off of Q1, provides a low-impedance path for reverse base current of Q3, and together with the use of the Baker clamp, results in a storage time for Q3 of less than 800nsec.

Snubbing circuits

There are two snubber circuits incorporated into this supply. The network of C12, D7, and R27 is used for load line shaping of transistor Q3 by delaying the voltage rise at the collector of Q3 while the current falls at turn off.

The values for the components in this network are calculated as follows:

$$C12 = \frac{I_{sc}\, t_f}{2\, V_{in(max)}} = \frac{2.3 \times 0.25 \times 10^{-6}}{2 \times 370} \approx 680pF$$

The resistor R27 is selected to discharge C12 with a time constant of one-half the minimum on time, which — under short circuit conditions — is approximately 2.5μs.

$$R27 = \frac{t_{on\,(min)}}{2C12} = \frac{2.5 \times 10^{-6}}{2 \times 680 \times 10^{-12}} \approx 1.8K\Omega$$

The power dissipated in this resistor is

$$P = \tfrac{1}{2}\, C12\, (V_{in\ max})^2\, f = \tfrac{1}{2}\, (680 \times 10^{-12})\, (370)^2\, 40 \times 10^3$$

$$P \approx 2 \text{ watts}$$

The second network of R26, C11, and D2 limits the voltage spike at turn off caused by the leakage inductance of the power transformer. The energy stored in this inductance is transferred into C11 via D2 after the power switch turns off and the voltage rises above the supply plus reset voltage.

C11 is defined by:

$$C11 = \frac{L_e\, I_{sc}^2}{(V_{reset} + \Delta V_{pp})^2 - V_{reset}^2}$$

Where L_e = Leakage inductance ($\approx 50\mu H$)
V_{reset} = Reset voltage across transformer (120V)
V_{pp} = Allowable leakage inductance Voltage spike (100V)

$$\therefore C11 = \frac{50 \times 10^{-6}\, (2.3)^2}{(120 + 100)^2 - 120^2} = 0.0078 \approx 10nF$$

Resistor R26 is selected to discharge C11 during the remainder of the period leaving a residual voltage equal to the reset voltage at the time turn-off next occurs.

$$R26 = \frac{(V_{reset} + \Delta V_{pp})\, 0.63\, \tau}{\Delta V_{pp}\, C11} =$$

$$= \frac{220}{100} \quad \frac{0.63\, (25 \times 10^{-6})}{(0.01 \times 10^{-6})} = 3.5K\Omega$$

In this application, R26 was increased to 4.7k due to second order effects such as reverse recovery of D2 which aids in discharging C11.

The power loss in R26 comes from the energy stored in the leakage inductance which is

$$P = \tfrac{1}{2} L_e\, I_{sc}^2\, f = \tfrac{1}{2}\, 50 \times 10^{-6}\, (2.3)^2\, 40 \times 10^3$$

$$P \approx 5.3 \text{ watts}$$

but here again, second order effects tend to reduce this value to less than 3 watts in this power supply.

Operating frequency

The frequency is set by R14 and C4 as

$$f = \frac{1}{R_T\, C_T} = \frac{1}{R_{14}\, C_4} = \frac{10^3}{12 \times 0.0022} \approx 40kHz$$

Supply start-up

The supply must reliably start with V_{DC} minimum = 250V. The value of R3 + R4 is defined by the total current requirement of the control electronics prior to start. If a start threshold of 12 volts is assumed, total control current is:

UC3840 max	= 7.0mA
R7 + R8	= 0.70mA
R10 + R11	= 0.27mA
C4 charging current	= 0.40mA
R17 + R18	= 0.22mA
Total Turn-On Current	8.59mA

$$\text{and } R3 + R4 = \frac{250 - 12}{8.59} = 27K\Omega$$

$$\therefore R15\ C8 = \frac{200V}{0.34V/\mu s} = 581\mu sec$$

With the knowledge that the ramp generator has greatest linearity with currents in the 100μA to 300μA range, we can pick:

R15 = 1.5MΩ and C8 ≅ 390pF.

Duty cycle clamp

The above analysis has provided a maximum duty cycle of 43% at minimum operating voltage. When the AC line voltage is removed, however, the input voltage will fall below 200 volts with the supply still running. As this voltage falls, the ramp slope will reduce and at the same time the error amplifier output will increase in an attempt to maintain regulation. This could extend the pulse width beyond 43% except for the action of the duty cycle clamp divider of R19 and R20 which is set to provide 3.9V at pin 8 with V_{DC} = 200V. Therefore, as V_{DC} falls, the voltage on pin 8 will also fall, taking command away from the error amplifier and maintaining a constant pulse width until the Under-Voltage sensing circuit gives a shutdown command.

Voltage control

In this power supply, output voltage regulation is controlled from the primary side by sensing V_C with R10 and R11 and closing a control loop with the error amplifier and 5V reference in the UC3840. The output voltage is then:

$$V_o\ (5V) = \left(\frac{N2}{N4}\right) V_{ref} \left(\frac{R10 + R11}{R11}\right)$$

Although the UC3840 optimizes this approach by the use of feed-forward which provides first-order automatic line regulation, there will still be inaccuracies caused by inadequate coupling beetween the windings, IR drops within the windings, and unequal losses in the rectifiers. If greater voltage accuracy is required, the feedback loop must be connected directly to one of the outputs with either on optical coupler or the UC1901 Isolated Feedback Generator used to maintain isolation.

The gain and phase plots for this supply are shown in Figure 3. Overall loop stability is aided by the fact that a discontinous-mode flyback topology is inherently a single pole system defined by the output load. Its transfer function, excluding the error amplifier, is shown by the dashed curve of Figure 3. The DC gain from the modulator input v_C, to the output, v_O, is:

$$\frac{v_O}{v_C} = K \sqrt{\frac{T R_{L\,min}}{2L_P}}$$

where K is defined by the feed-forward slope as

$$K = \frac{(\text{Max duty cycle})\ (V_{in\ min})}{\text{Ramp peak - Ramp valley}} = \frac{0.43 \times 200}{4.2 - 0.5}$$

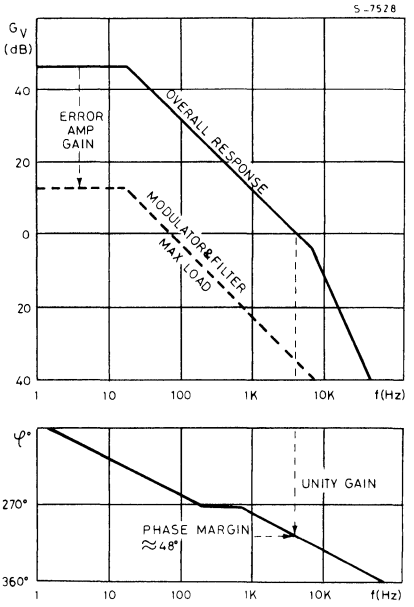
and the minimum load resistance reflected to the primary control supply is:

$$R_{L\,min} = \frac{V^2}{P_{O\,max}} = \frac{12^2}{50} = 2.88\Omega$$

$$\therefore \frac{v_O}{v_C} = \frac{0.43 \times 200}{4.2 - 0.5} \sqrt{\frac{25 \times 10^{-6} \times 2.88}{2 \times 1 \times 10^{-3}}} =$$

$$= 4.41 = 13db$$

Fig. 3 — Power supply loop gain and phase



The effective output capacitance, also reflected to the control supply, is:

$$C_E = C14 \left(\frac{N2}{N4}\right)^2 + C13 \left(\frac{N3}{N4}\right)^2 + C3$$

;

$$= 4700 \left(\frac{4}{9}\right)^2 + 2200 \left(\frac{9}{9}\right)^2 + 200$$

$$= 3328\mu F$$

Reset jumper on pin 5
(leave out if it is desired to latch the supply off after any fault)

Note that there is nothing connected to pin 4. A low signal here will shut down the supply.

Small signal diodes

The seven small axial lead diodes, D2 through D8 should next be installed insuring correct polarity as shown in Figure 5.

Passive devices

Install the low-power resistors and small capacitors first. Follow with the four high-power resistors, R3, R4, R26 and R27. When inserting R26, keep the body of the resistor $\approx$ ¾ inch above the PC board. This resistor will get hot and it is best to have it above, rather than next to C11. At this time, the input diode bridge, D1, and the IC socket can be inserted. Note that pin 1 of the UC3840 is to the front of the PC board.

Large components

Assembly can be completed by installing the remaining components as follows:

a. Two small signal transistors, Q1 and Q2
b. Transformer
c. Electrolytic capacitors: C1, C2, C3, C13 and C14. Check polarity against signs of foil side of PC board.
d. Power transistor Q3 inserts with its front to the left, or input, inside of the PC board. Insertion is easier if the heat sink is clipped on first.

NOTE: THIS HEAT SINK IS AT THE SAME POTENTIAL AS THE COLLECTOR AND WILL HAVE UP TO 600 VOLTS PRESENT: KEEP IT CLEAR OF OTHER COMPONENTS, TEST LEADS, AND YOUR FINGERS.

e. Install the 5 volt output rectifier, D9 with its front facing the right, or output side of the board. It also gets a clip-on heat sink.

Check to see that all components are installed and match the drawing of Fig. 5 . Insert the UC3840 into the socket.

CHECKOUT PROCEDURES

With the power supply fully assembled, the following checkout procedure is recommended before any input voltage is applied. This procedure is also useful for trouble-shooting a unit which is not operating properly. Checkout will be aided if the user has installed test points at all indicated positions in the PC board. Reference should be made to Figure 5 for test point locations.

1. Insure that there is no AC input voltage applied
2. Double check all connections including diode and capacitor polarities. Insure that the UC3840 is correctly inserted into the socket.
3. Connect a minimum load on one or both outputs equivalent to 25 watts total. i.e., 2Ω on the 5V output and 12Ω on the 12V output. Be careful of the heat from these loads.
4. Install a temporary jumper shorting the base and emitter of Q3 together. Use test points provided on PC board.
5. Connect a 0 to 30 volt, 500mA lab supply to simulate the control voltage, V_C. Connect the positive lead to IC-15 and ground to IC-13. Note that IC-13 will be the ground reference point for all primary side measurements. Set V_C = Zero volts and add a 1kΩ, ½ W resistor in shunt across the power supply terminals.
6. Increase V_C to 10 volts and check the following:
   a. IC-16: should have 5V if the reference is working.
   b. IC-2: Should be 2.3V if hysteresis current is on.
   c. IC-14: Should be < 0.1V as Driver Bias is off.
7. Increase V_C to 14 volts and ckeck the following:
   a. IC-2: Should be 4.7 volts if hysteresis current is off.
   b. IC-14: Should be 12 volts with Driver Bias on.
   c. IC-9: Oscillator should show 40kHz exponential waveform.
   d. Return V_C to Zero volts but leave connected.
8. Apply the high voltage, V_{DC}. This can be done either with a DC lab supply with 300V capability or the input AC line voltage.

   A fuse rated at no more than two amps should be in series with the input line to prevent excessive damage in the event of a failure.

   NOTE: BE SURE TO USE AN ISOLATION TRANSFORMER WHEN LINE POWER IS USED AS PRIMARY GROUND IS ONE SIDE OF THE LINE.

   An AC variac will also be helpful in varying the input voltage.

   If a DC power supply is used, connect the positive line to the V_{DC} test point at the top of the board. The negative line will connect to ground on IC-13. Insure that the base-emitter short is still connected to Q3.
9. With V_{DC} = 200 volts, set V_C = 10 volts and check the following:
   a. IC-14: Should be < 0.1V if Driver Bias is off
   b. IC-8: Should be < 0.1V of Slow Start clamp is on.
   c. IC-6: Should be 2.3V to establish current limit threshold.

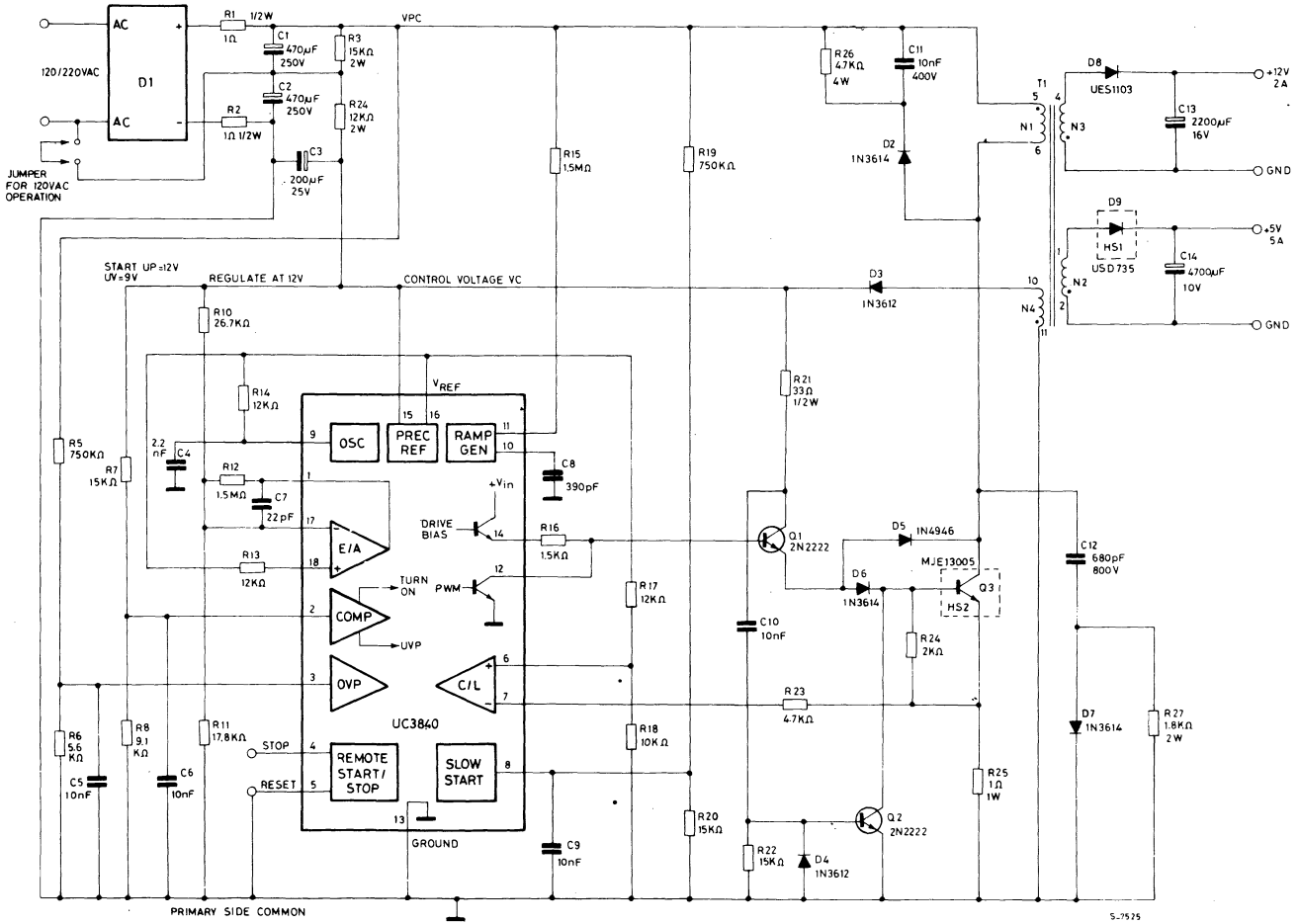


Fig. 4 — UC3840 PWM control circuit

A SECOND-GENERATION IC SWITCH MODE CONTROLLER OPTIMIZED FOR HIGH FREQUENCY POWER MOS DRIVE

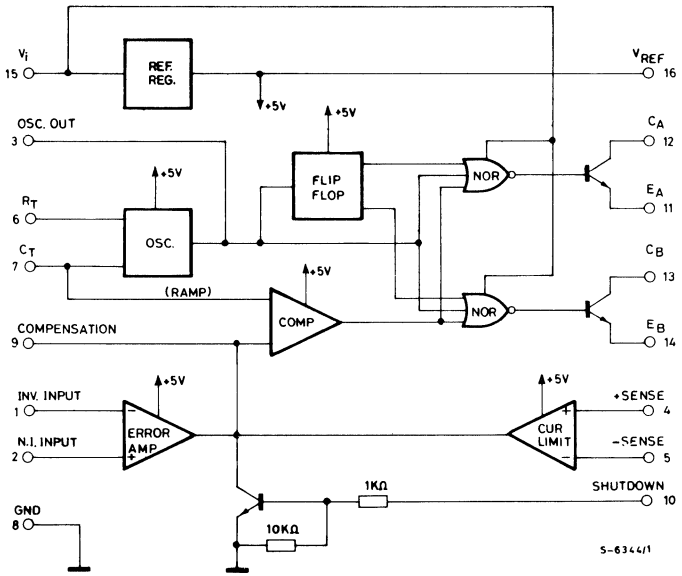
INTRODUCTION

Since the introduction of the SG1524 in 1976, integrated circuit controllers have played an important role in the rapid development and exploitation of high-efficiency switching power supply technology. The 1524 soon became an industry standard and was widely second-sourced.
Although this device contained all the basic control elements required for switching regulator design, practical power supplies still required other functions which had to be implemented with additional external discrete circuitry.

An additional development within the semiconductor industry was the introduction of practical Power Mos which offered the potential of higher efficiencies at higher speeds with resultant lower overall system costs.
In order to be able to take full advantage of the speed capabilities of power MOS, it was necessary to provide high peak currents to the gate during turn-on and turn-off to quickly charge and discharge the gate capacitances of 800 to 2000pF present in higher current units.

The development of a second-generation regulating PWM IC, the SG1525A, and its complimentary output version, the SG1527A, was a direct result of the desire to add more power supply elements to the control IC, as well as to optimize the interfacing of high current power devices.

Fig. 1 – The SG1524 regulating PWM block diagram.
This design was the first complete I.C. control chip for switch mode power supplies.

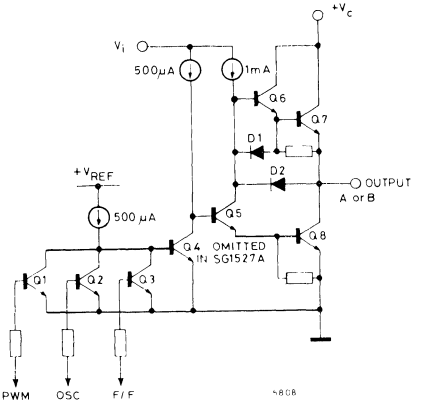


"TOTEM-POLE" OUTPUT STAGE

One of the most significant benefits in using the SG1525A is its output configuration. For the first time it has been recognized in an IC controller that it is more difficult to turn a power switch off than turn it on. With the SG1525A, a high-current, fast transition, low impedance drive is provided for both turn-on and turn-off of an external power transistor or Power MOS. The circuit schematic of one of the two output stages contained within the device is shown in Figure 3. This is a two-state output, either Q_8 is on, forming a low saturation voltage pull-down, or Q_7 is on, pulling the output up to V_C. Note that V_C is a separate terminal from the V_i supply to the rest of the device.

This offers the benefits of potentially operating the output drive from a lower supply than the rest of the circuit for power efficiencies, decoupling of drive transients from more sensitive circuits, and a third terminal for extracting a drive signal. Note that even though V_C can be set either higher or lower than V_i, the output cannot rise higher than approximately 1½ volts below V_i.

Fig. 3 – One of two power output stages contained within the SG1525A which conduct alternately due to the internal flip-flop.



During the transition between states, there is a slight conduction overlap between source and sink which results in a pulse of current flowing from V_C to ground. However, due to the high-speed design configuration of this stage, this current spike lasts for only about 100 ns. A typical current waveform at V_C is shown in Figure 4. This transient will normally be decoupled from the rest of the control power by a 0.1μF capacitor from V_C to ground but it should not, otherwise, cause a problem unless very high frequency operation is contemplated where it will contribute to overall device power dissipation, by becoming a significant portion of the total duty cycle.

The output saturation characteristics of this stage are shown in Figure 5. The source transistor, Q_7 is a straight forward Darlington and its saturation voltage remains between 1 and 2V out to 400 mA under the assumption that $V_i \geq V_{CC}$. The sink transistor, Q_8, however, has a non-uniform characteristic which needs explanation. At low sink currents, the 1mA current source through Q_5 insures a very low saturation voltage at the output. As load current increases past 50 mA, Q_8 begins to come out of saturation for lack of base drive but only up to about 2V. Here diode D_2 becomes forward biased shunting a portion of the load current through Q_5 to boost the base current into Q_8. With this circuit, the sink transistor can both support high peak discharge currents from a capacitive load, as well as insure the low static hold-off voltage required for bipolar transistors.

Fig. 4 – Current "spiking" on the V_C terminal caused by conduction overlap between source and sink is minimized by high-speed design techniques.

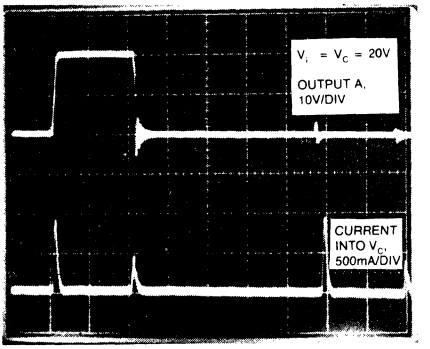
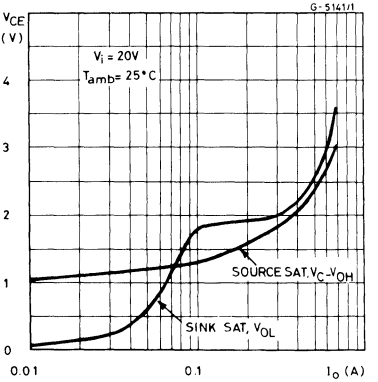
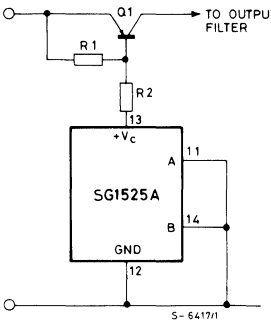


Fig. 5 – The output saturation characteristics of the SG1525A provide both high drive current and low hold-off voltage.



A typical output configuration for a push-pull bipolar transistor power stage is shown in Fig. 6. With a steady state base drive current from the SG1525A of 100mA, this stage should be able to switch 1 to 5A of transformer primary current, depending

Fig. 10 — A single-ended ground-referenced power stage for a flyback or boost regulator.



CONTROLLING POWER SUPPLY START-UP

Although the advantages of the SG1525A's output stage will often be reason enough for its selection, there are several other important and useful features incorporated within this product. One problem previously overlooked in PWM circuits is keeping the output under control as the supply voltage is turned on and off. Undefined states, particularly the possibility of turning on an output before the oscillator is running, can be quite awkward, if not catastrophic. To prevent this, the SG1525A has incorporated an under-voltage lockout circuit which effectively clamps the outputs to the off state with as little as 2½V of supply voltage which is less than the voltage required to turn the outputs on. This clamp is maintained until the supply reaches approximately 8V insuring that all the remaining SG1525A circuitry is fully operational prior to enabling the outputs. The clamp reactivates when the supply is lowered to approximately 7.5V. There is about 500mV of hysteresis built in to eliminate clamp oscillation at threshold.

Another important aspect of power sequencing is restraining the outputs from immediately commanding a 100% duty cycle when they are activated. This is accomplished by a slow turn on (soft-start) which is defined by an internal 50 μA current source in conjunction with an externally applied capacitor. The details of this power sequencing system are shown in Figure 11.

Q_3 and Q_4 are the output gates normally driven by the oscillator through D_2 to provide output blanking between pulses. (One of these transistors is shown as Q_2 in Figure 3). At low supply voltages, Q_2 conducts with base drive from the 20μA current source. Q_2 provides three functions. First, current through R_4 activates the output gates with minimum voltage drop. Second, current through R_5 activates the shutdown transistor Q_5 holding the soft-start capacitor, C_{SS}, discharged. Third, R_2 provides a small bucking voltage across R_3 for hysteresis at the switch point.

When the input voltage becomes high enough to provide a little more than one volt at the base of Q_1, that transistor turns on. This turns off Q_2, activating the outputs and allowing C_{SS} to begin to charge from the internal 50 μA current source. The time to reach approximately 50% duty cycle will be

$$t = \left(\frac{2 \text{ volts}}{50\ \mu A} \right) C_{SS}$$

Fig. 11 — The internal power turn-on, soft-start, and shutdown circuitry of the SG1525A.

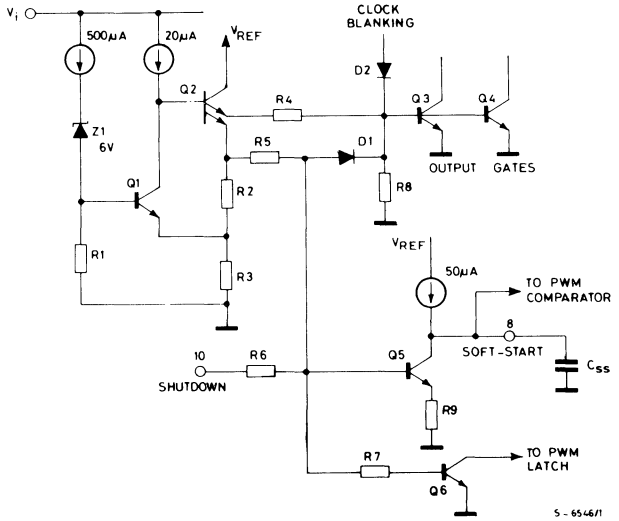


Fig. 12 – A simplified schematic of the SG1525A's oscillator circuitry.

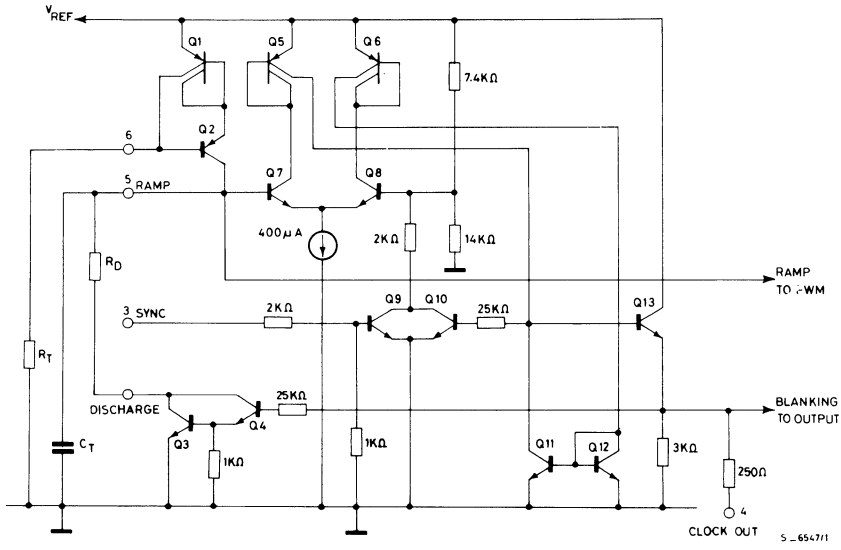


Fig. 13 – 200W, Off-Line Forward Converter.

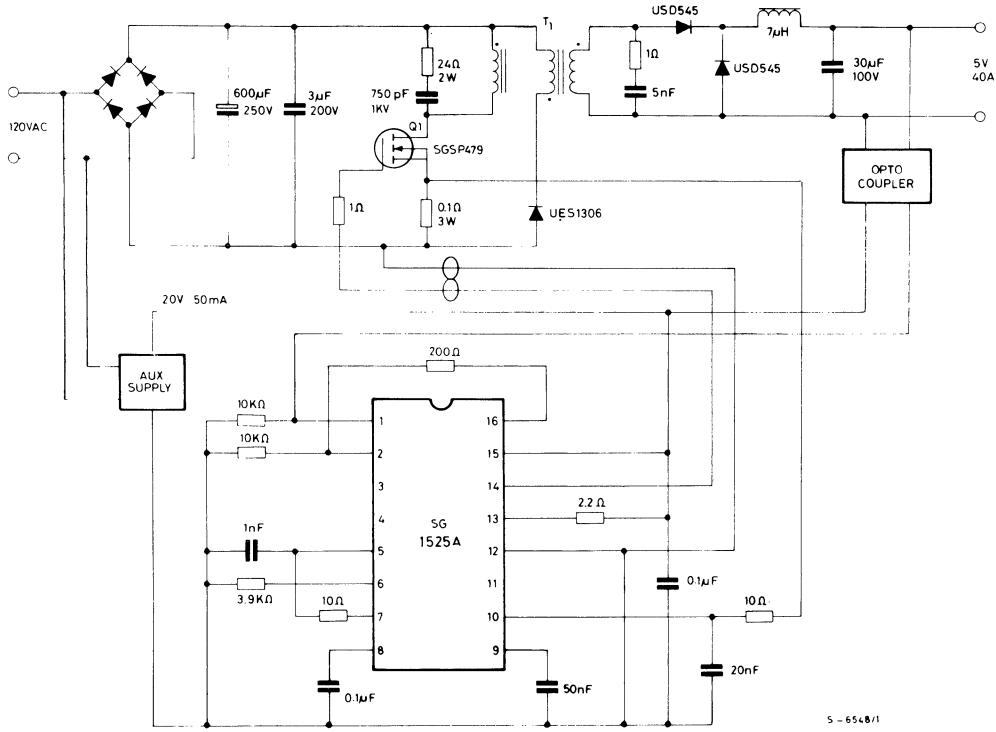
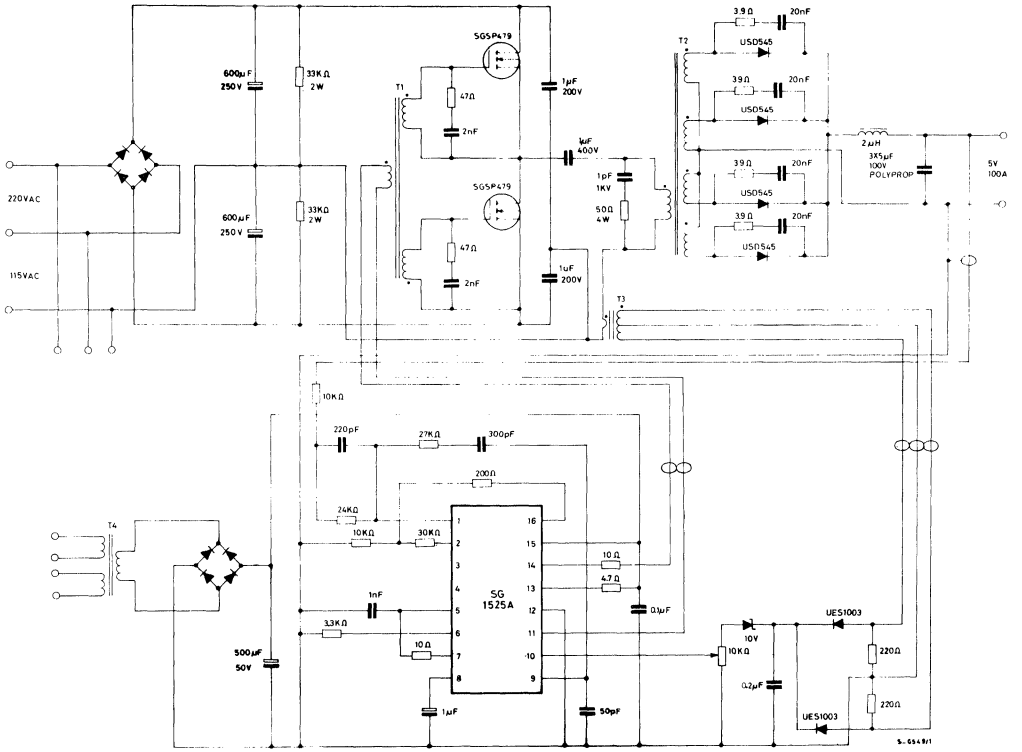


Fig. 15 — 500W, 100 kHz Half-Bridge Schematic.



Transformer Winding Data

500W, 100kHz, Off-Line, Half-Bridge Converter:

T1 Core: Ferrox 486T250-3C8
Pri: 14T #22AWG
Sec (2): 7T #22AWG

T2 Core: Ferrox EC52-3C8 (EE)
Pri: 14T, 2 layers, 2 #16AWG in parallel
Sec (2): each 2T, C.T., copper strap 0.01" x 0.8"

T3 Core: Ferrox 486T250-3C8
Pri: 1T
Sec: 20T, C.T. #22AWG

T4 117V/220V, 25V, 0.15A, 50-60 Hz

L1 Core: Ferrox IF30-3C8
4 turns, 5 #12AWG in parallel

500 WATT, OFF-LINE, HALF-BRIDGE CONVERTER

The circuit shown in Figure 15 uses a pair of SGSP479 power MOS in a half-bridge configuration with the SG1525A chip referenced to the secondary side of the power transformer.
The power MOS gates are driven directly from the control chip output through step down and isolation transformer T1. The SG1525A output terminals (pins 11 and 14) provide active pull-up and pull-down (dual source/sink) for the primary of T1. This provides the fast, high current turn-on and turn-off pulses needed for the power MOS gates. In addition, the two ends of the primary windings are shorted to ground during deadtime, which prevents accidental turn-on by transients. Note that the current supplied by the SG1525A outputs drops to a small value when the gate capacitance has been charged or discharged to the desired gate voltage. Damping resistors with series blocking capacitors across the two secondaries of T1 minimize ringing due to the power MOS gate capacitance and the inductance of T1 and lead inductance, particularly during deadtime.

Deadtime for the SG1525A is set very simply by a single resistor between pins 5 and 7. Only a small amount of deadtime is needed since the power MOS have no storage time and a very short delay time.

Slow turn-on is accomplished by a single capacitor at pin 8.

A DESIGNER'S GUIDE TO THE L200 VOLTAGE REGULATOR

Delivering 2A at a voltage variable from 2.85V to 36V, the L200 voltage regulator is a versatile device that simplifies the design of linear supplies. This design guide describes the operation of the device and its applications.

The introduction of integrated regulator circuits has greatly simplified the work involved in designing supplies. Regulation and protection circuits required for the supply, previously realized using discrete components, are now integrated in a single chip. This has led to significant cost and space saving as well as increased reliability. Today the designer has a wide range of fixed and adjustable, positive and negative series regulators to choose from as well as an increasing number of switching regulators.

The L200 is a positive variable voltage regulator which includes a current limiter and supplies up to 2A at 2.85 to 36V.

The output voltage is fixed with two resistors or, if a continuously variable output voltage is required, with one fixed and one variable resistor.

The maximum output current is fixed with a low value resistor. The device has all the characteristics common to normal fixed regulators and these are described in the datasheet. The L200 is particularly suitable for applications requiring output voltage variation or when a voltage not provided by the standard regulators is required or when a special limit must be placed on the output current.

The L200 is available in two packages:

Pentawatt — Offers easy assembly and good reliability. The guaranteed thermal resistance ($R_{th\ j\text{-}case}$) is 3°C/W (typically 2°C/W) while if the device is used without heatsink we can consider a guaranteed junction-ambient thermal resistance of 50°C/W.

TO-3 — For professional and military use or where good hermeticity is required.
The guaranteed junction-case thermal resistance is 4°C/W, while the junction-ambient thermal resistance is 35°C/W.
The junction-case thermal resistance of this package, which is greater than that of the Pentawatt, is partly compensated by the lower contact resistance with the heatsink, especially when an electrical insulator is used.

CIRCUIT OPERATION

As can be seen from the block diagram (fig. 1) the voltage regulation loop is almost identical to that of fixed regulators. The only difference is that the negative feedback network is external, so it can be varied (fig. 3). The output is linked to the reference by:

$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) \qquad (1)$$

Considering V_{out} as the output of an operational amplifier with gain equal to $G_V = 1 + R2/R1$ and input signal equal to V_{ref}, variability of the output voltage can be obtained by varying R1 or R2 (or both). It's best to vary R1 because in this way the current in resistors R1 and R2 remains constant (this current is in fact given by $V_{ref}/R1$).

(Equation (1) can also be found in another way which is more useful in order to understand the descriptions of the applications discussed.

$$V_{out} = R1\ i_1 + R2\ i_2$$

and since in practice $i_1 \gg i_4$ (i_4 has a typical value of 10 μA) we can say that

$$V_{out} = R1\ i_1 + R2\ i_1 \quad \text{with} \quad i_1 = \frac{V_{ref}}{R1}$$

Therefore

$$V_{out} = \frac{R2}{R1}V_{ref} + V_{ref} = V_{ref}\left(1 + \frac{R2}{R1}\right)$$

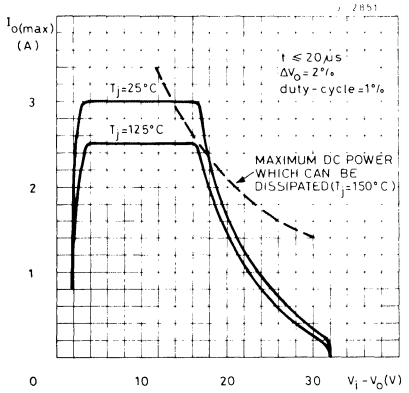
In other words R1 fixes the value of the current circulating in R2 so R2 is determined.

Overload protection

The device has an overload protection circuit which limits the current available.

Referring to fig. 2, R24 operates as a current sensor. When at the terminals of R24 there is a voltage drop sufficient to make Q20 conduct, Q19 begins to draw current from the base of the power transistor (darlington formed by Q22 and Q23) and the output current is limited. The limit depends on the current which Q21 injects into the base of Q20. This current depends on the drop-out and the temperature which explains the trend of the curves in fig. 4.

Fig. 4



Thermal protection

The junction temperature of the device may reach destructive levels during a short circuit at the output or due to an abnormal increase in the ambient temperature. To avoid having to use heatsinks which are costly and bulky, a thermal protection circuit has been introduced to limit the output current so that the dissipated power does not bring the junction temperature above the values allowed. The operation of this circuit can be summarized as follows.

In Q17 there is a constant current equal to:

$$\frac{V_{ref} - V_{BE17}}{R17 + R16} \qquad (V_{ref} = 2.75V \text{ typ})$$

The base of Q18 is therefore biased at:

$$V_{BE18} = \frac{V_{ref} - V_{BE17}}{R16 + R17} \cdot R16 \cong 350 \text{ mV}$$

Therefore at T_j = 25°C Q18 is off (since 600 mV is needed for it to start conducting). Since the V_{BE} of a silicon transistor decreases by about 2 mV/°C, Q18 starts conducting at the junction temperature:

$$T_j = \frac{600-350}{2} + 25 = 150°C$$

Current limitation

The innovative feature of this device is the possibility of acting on the current regulation loop, i.e. of limiting the maximum current that can be supplied to the desired value by using a simple resistor (R3 in fig. 2). Obviously if R3 = 0 the maximum output current is also the maximum current that the device can supply because of its internal limitation.

The current loop consists of a comparator circuit with fixed threshold whose value is V_{sc}. This comparator intervenes when $I_o \cdot R3 = V_{sc}$, hence $I_o = \frac{V_{sc}}{R3}$ (V_{sc} is the voltage between pins 5 and 2 with typical value of 0.45V).

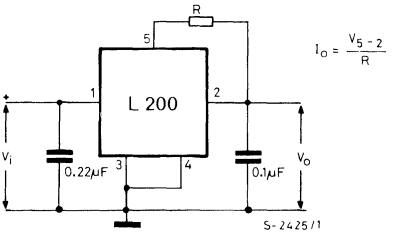
Special attention has been given to the comparator circuit in order to ensure that the device behaves as a current generator with high output impedance.

TYPICAL APPLICATIONS

Programmable current regulator

Fig. 5 shows the device used as current generator. In this case the error amplifier is disabled by short-circuiting pin 4 to ground.

Fig. 5



The output current I_o is fixed by means of R:

$$I_o = \frac{V_{5-2}}{R}$$

The output voltage can reach a maximum value $V_i - V_{drop} \cong V_i - 2V$ (V_{drop} depends on I_o).

Programmable voltage regulator

Fig. 6 shows the device connected as a voltage regulator and the maximum output current is the maximum current that the device can supply. The output voltage V_o is fixed using potentiometer R2. The equation which gives the output voltage is as follows:

$$V_o = V_{ref}\left(1 + \frac{R2}{R1}\right)$$

By substituting the potentiometer with a fixed resistor and choosing suitable values for R1 and R2, it is possible to obtain a wide range of fixed output voltages.

The formula for calculating R is as follows:

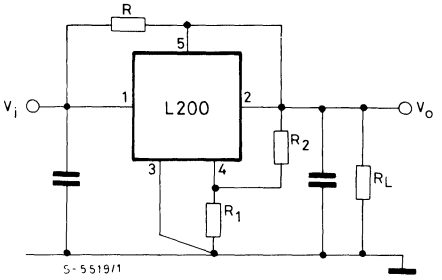
$$R = \frac{V_{i\,min} - (V_o + V_{drop})}{I_o}$$

Where V_{drop} is the minimum differential voltage between the input and the output of the device at current I_o. $V_{in\,min}$ is the minimum input voltage. V_o is the output voltage and I_o the output current.

With constant load, resistor R can be connected between pins 1 and 2 of the IC instead of in series with the input (fig. 10). In this way, part of the load current flows through the device and part through the resistor. This configuration can be used when the minimum current by the load is:

$$I_{o\,min} = \frac{V_{drop}}{R} \quad \text{(instant by instant)}$$

Fig. 10



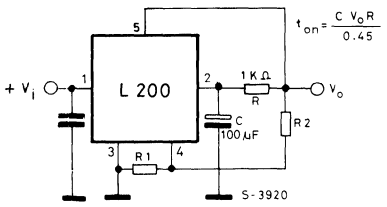
Soft start

When a slow rise time of the output voltage is required, the configuration in fig. 11 can be used. The rise time can be found using the following formula:

$$t_{on} = \frac{CV_o R}{0.45}$$

At switch on capacitor C is discharged and it keeps the voltage at pin 2 low; or rather, since a voltage of more than 0.45V cannot be generated between pins 5 and 2, the V_o follows the voltage at pin 2 at less than 0.45V.

Fig. 11



Capacitor C is charged by the constant current i_c.

$$i_c = \frac{V_{sc}}{R}$$

Therefore the output reaches its nominal value after the time t_{on}:

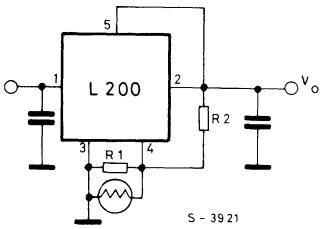
$$V_o - V_{sc} = \frac{i_c \cdot t_{on}}{C}$$

$$t_{on} = C \cdot \frac{(V_o - 0.45)}{0.45} \cdot R \cong \frac{CV_o R}{0.45}$$

Light controller

Fig. 12 shows a circuit in which the output voltage is controlled by the brightness of the surrounding environment. Regulation is by means of a photoresistor in parallel with R1. In this case, the output voltage increases as the brightness increases. The opposite effect, i.e. dimming the light as the ambient light increases, can be obtained by connecting the photoresistor in parallel with R2.

Fig. 12



Light dimmer for car display

Although digital displays in cars are often more aesthetically pleasing and frequently more easily read they do have a problem. Under varying ambient light conditions they are either lost in the background or alternatively appear so bright as to distract the driver. With the system proposed here, this problem is overcome by automatically adjusting the display brightness during daylight conditions and by giving the driver control over the brightness during dusk and darkness conditions.

The circuit is shown in fig. 13. The primary supply is shown taken straight from the car battery however it is worth noting that in a car there is always the risk of dump voltages up to 120V and it is recommended that some form of protection is included against this.

Under daylight conditions i.e. with sidelights off and T1 not conducting the output of the device is determined by the values of R1, R2 and the photoresitor (PTR). The output voltage is given by

$$V_{out} = V_{ref}\left(1 + \frac{R2}{PTR//R1}\right)$$

If the ambient light intensity is high, the resistance of the photoresistor will be low and therefore V_{out} will be high. As the light decreases, so V_{out} decreases dimming the display to a suitable level.

The designer must take into account the dissipated power and the SOA of the preregulation transistor. For example, using the BDX53, the maximum input voltage can reach 56V (fig. 16). In these conditions we have 20V of V_{CE} on the transistor and with a load current of 2A the operation point remains inside the SOA. The preregulation used in fig. 16 reduces the ripple at the input of the device, making it possible to obtain an output voltage with negligible ripple.

If high output voltages are also required, a second zener, V_Z, is used to refer the ground pin of an IC to a potential other than zero; diode D1 provides output shortcircuit protection (fig. 18).

Fig. 18

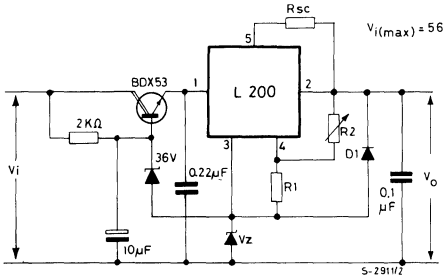
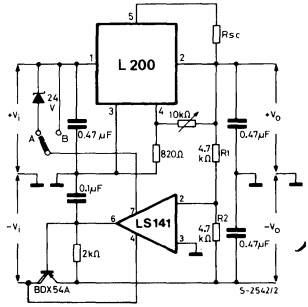


Fig. 19



A : $V_{i(max)} \leq \pm 34V$ $3 < V_o < 30$

B : $V_{i(max)} \leq \pm 22V$ $3 < V_o < 18$

Positive and negative voltage regulators

The circuit in fig. 19 provides positive and negative balanced, stabilized voltages simultaneously. The L200 regulator supplies the positive voltage while the negative is obtained using an operational amplifier connected as follower with output current booster.

Tracking of the positive voltage is achieved by putting the non-inverting input to ground and using the inverting input to measure the feedback voltage coming from divider R1-R2.

The system is balanced when the inputs of the operational amplifier are at the same voltage, or, since one input is at fixed ground potential, when the voltage of the intermediate point of the divider goes to 0 Volts. This is only possible if the negative voltage, on command of the op-amp, goes to a value which will make a current equal to that in R1 flows in R2. The ratio which expresses the negative output voltage is:

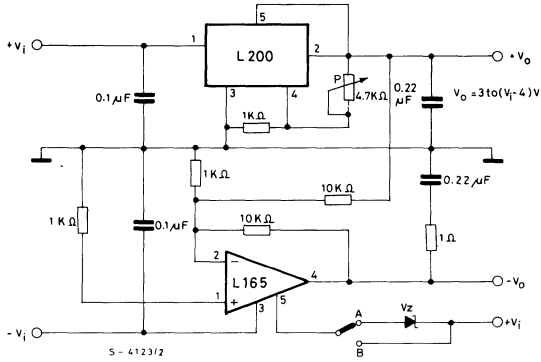
$$V^- = V^+ \cdot \frac{R2}{R1} \qquad \text{(If R2= R1, we'll get } V^- = V^+\text{)}$$

Since the maximum supply voltage of the op amp used is ± 22V, when pin 7 is connected to point B output voltages up to about 18V can be obtained. If on the other hand pin 7 is connected to point A, much higher output voltages, up to about 30V, be obtained since in this case the input voltage can rise to 34V.

Fig. 20 shows a diagram is which the L165 power op amp is used to produce the negative voltage. In this case (as in fig. 19) the output voltage is limited by the absolute maximum rating of the supply voltage of the L165 which is ± 18V. Therefore to get a higher V_{out} we must use a zener to keep the device supply within the safety limits.

If we have a transformer with two separate secondaries, the diagram of fig. 21 can be used to obtain independent positive and negative voltages. The two output diodes, D1 and D2, protect the devices from shortcircuits between the positive and negative outputs.

Fig. 20



A: for $\pm 18V \leq V_i \leq 32V$

Note: V_Z must be chosen in order to verify $2V_i - V_Z = 36V$

B: for $V_i \leq \pm 18V$

Motor speed control

Fig. 25 shows how to use the device for the speed control of permanent magnet motors. The desired speed, proportional to the voltage at the terminal of the motor, is obtained by means of R1 and R2.

$$V_M = V_{ref}\left(1 + \frac{R2}{R1}\right)$$

To obtain better compensation of the internal motor resistance, which is essential for good regulation, the following equation is used:

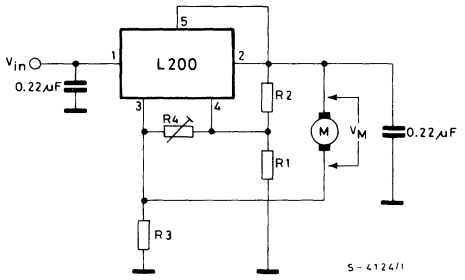
$$R3 \leqslant \frac{R1}{R2} \cdot R_M$$

This equation works with infinite R4. If R4 is finite, the motor speed can be increased without altering the ratio R2/R1 and R3. Since R4 has a constant voltage (V_{ref}) at its terminals, which does not vary as R4 varies, this voltage acts on R2 as a constant current source variable with R4. The voltage drop on R2 thus increases, and the increase is felt by the voltage at the terminals of the motor. The voltage increase at the motor terminals is:

$$V_M = \frac{V_{ref}}{R4 + R3} \cdot R2.$$

A circuit for a 30W motor with $R_M = 4\Omega$, $R1 = 1\,k\Omega$, $R2 = 4.3\ k\Omega$, $R4 = 22\ k\Omega$ and $R3 = 0.82\Omega$ has been realized.

Fig. 25



Power amplitude modulator

In the configuration of fig. 26 the L200 is used to send a signal onto a supply line. Since the input signal V_i is DC decoupled, the V_o is defined by:

$$V_o = V_{ref}\left(1 + \frac{R2}{R1}\right)$$

The amplified signal V_i whose value is:

$$G_v = -\frac{R2}{R3}$$

is added to this component. By ignoring the current entering pin 4, we must impose $i_1 = i_2 + i_3$ (1) and since the voltage between pin 4 and ground remains fixed (V_{ref}) as long as the device is not in saturation, $i_1 = 0$ and equation (1) becomes:

$i_2 = -i_3$ with $i_3 = \frac{V_i}{R3}$ (for $X_c \ll R3$) -Therefore:

$$v_o = R2\ i_2 = -\frac{V_i}{R3} \cdot R2.$$

An application is shown in fig. 27. If the DC level is to be varied but not the AC gain, R1 should be replaced by a potentiometer.

Fig. 26

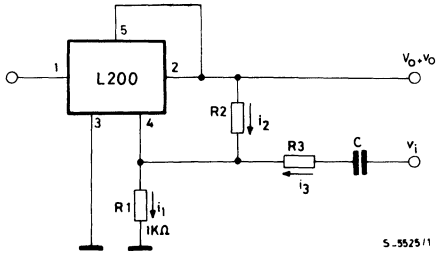
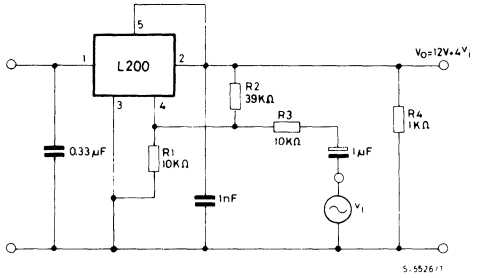


Fig. 27



HIGH CURRENT REGULATORS

To get a higher current than can be supplied by a single device one or more external power transistors must be introduced. The problem is then to extend all the device's protection circuits (short-circuit protection, limitation of T_j of external power devices and overload protection) to the external transistors. Constant current or foldback current limitation therefore becomes necessary.

When the regulator is expected to withstand a permanent shortcircuit, constant current limitation becomes more and more difficult to guarantee as the nominal V_o increases. This is because of the increase in V_{CE} at the terminals of the transistor, which leads to an increase in the dissipated power. The heatsink has to be calculated in the heaviest working conditions, and therefore in shortcircuit. This increases weight, volume and cost of the heatsink and increase of the ambient temperature (because of high power dissipation). Besides heatsink, power transistors must be dimensioned for the short-circuit.

Fig. 31

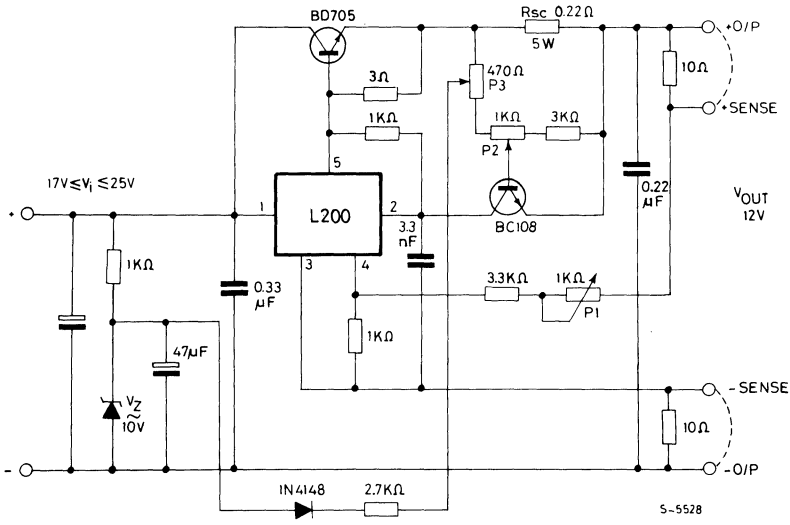


Fig. 32

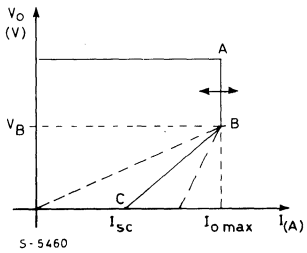


Fig. 34

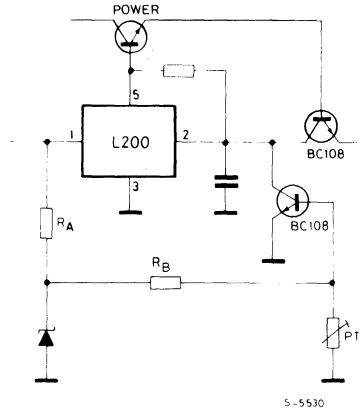
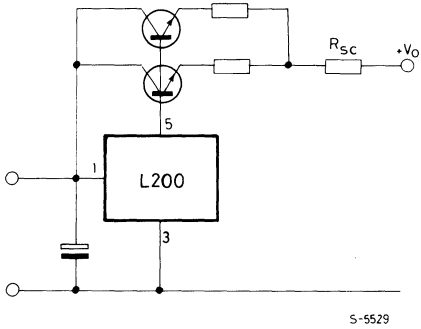


Fig. 33



Voltage regulator from 0V to 16V - 4.5A

Fig. 35 shows an application for a high current supply with output voltage adjustable from 0V to 16V, realized with two L200 regulators and an external power transistor. With the values indicated, the current can be regulated from 2A to 4.5A by potentiometer PT2. PT1, on the other hand, is used for constant current or foldback current limitation. The integrated circuit IC2, which does not require a heatsink and has excellent temperature stability, is used to obtain the 0V output. It is connected so as to lower pin 3 of IC1 until pin 4 reaches 0V. Q1 and Q2 ensure correct operation of the supply at switch-on and switch-off.

LAYOUT CONSIDERATIONS

The performance of a regulator depends to a great extent on the case with which the printed circuit is produced. There must be no impulsive currents (like the one in the electrolytic filter capacitor at the input of the regulator) between the ground pin of the device (pin 3) and the negative output terminal because these would increase the output ripple. Care must also be taken when inserting the resistor connected between pin 4 and pin 3 of the device.

The track connecting pin 3 to a terminal of this resistor should be very short and must not be crossed by the load current (which, since it is generally variable, would give rise to a voltage drop on this stretch of track, altering the value of V_{ref} and threfore of V_o.

When the load is not in the immediate proximity of the regulator output "+ sense" and "– sense" terminals should be used (see fig. 37). By connecting the "+ sense" and "– sense" terminals directly at the charge terminals the voltage drop on the connection cable between supply and load are compensated. Fig. 37 shows how to connect supply and load using the sensing clamps terminals.

Fig. 37

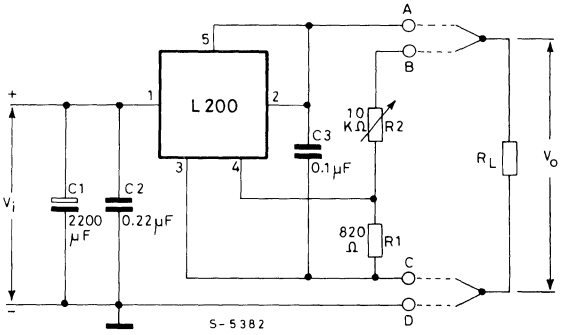
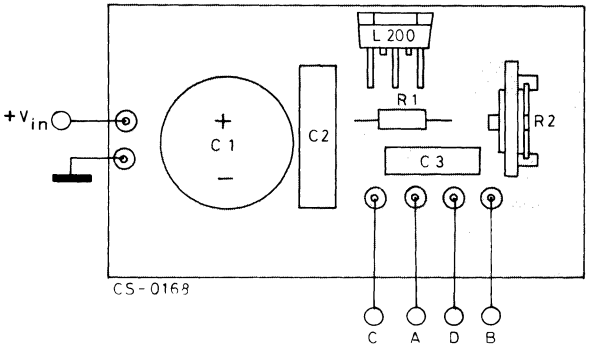


Fig. 38

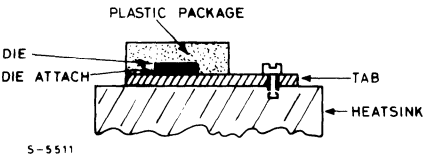


HEATSINK DIMENSIONING

The heatsink dissipates the heat produced by the device to prevent the internal temperature from reaching values which could be dangerous for device operation and reliability.

Integrated circuits in plastic package must never exceed 150°C even in the worst conditions. This limit has been set because the encapsulating resin has problems of vitrification if subjected to temperatures of more than 150°C for long periods or of more than 170°C for short periods (24 h). In any case the temperature accelerates the ageing process and therefore influences the device life; an increase of 10°C can halve the device life. A well designed heatsink should keep the junction temperature between 90°C and 110°C. Fig. 39 shows the structure of a power device. As demonstrated in thermodynamics, a thermal circuit can be considered to be an electrical circuit where R1, 2 represent the thermal resistance of the single elements (expressed in °C/W);

Fig. 39



of 3 between the two sides. The temperature jump will depend on the dissipated power and one the device geometry but we want to show that there exists an optimal position between the two devices:

$$d = \frac{1}{2} \cdot \text{side of the plate}$$

Fig. 46 shows the trend of the temperature as a function of the distance between two dissipating elements whose dissipated power is fairly different (ratio 1 to 4).

This graph may be useful in applications with the L200 + external transistor (in which the transistor generally dissipates more than the L200) where the temperature of the L200 has to be kept as low as possible and especially where the thermal protection of the L200 is to be used to limit the transistor temperature in the case of an overload or abnormal increase in the ambient temperature. In other words the distance between the two elements can be selected so that the power transistor reaches the $T_{j\ max}$ (200°C for a TO-3 transistor) when the L200 reaches the thermal protection intervention temperature.

Fig. 45

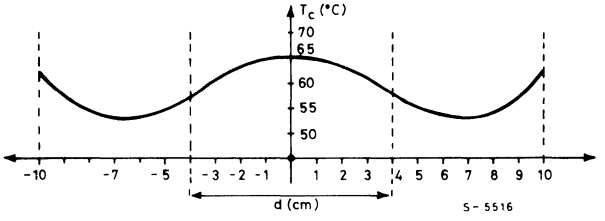
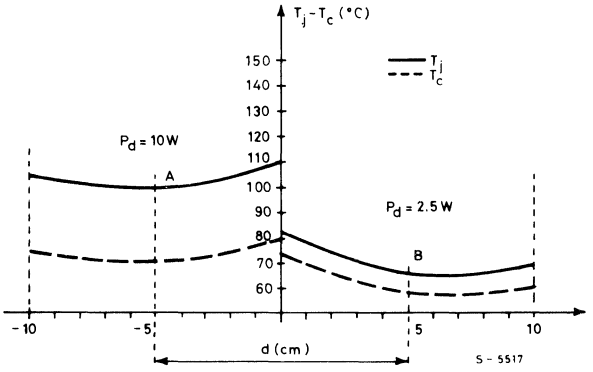


Fig. 46



A : Position of the device with high power dissipation (10W)
B : Position of the device with low power dissipation (2.5W)

CONTROL OF A DC MOTOR USING TRANSPACK

microprocessor based fully integrated solution

INTRODUCTION

This article covers the design of a controller for a DC permanent magnet motor. The design is preceded by a mathematical simulation of the controller. The controller design is complete with working drawings and a programme for the microprocessor. A comprehensive collection of diagrams and photos shows the operational performance of the design under normal and adverse working conditions.

Simulation of Motor Behaviour

The motor chosen for the design is a constant current type with a permanent magnet with a stator flux nearly constant and a good power to weight ratio compared with classic DC motors.

Simulation forcast: – Max. peak current, Ripple current at various chopper frequencies, Response speed of the system. Function in steady state.

The parameters are studied for extreme working conditions to optimise the choice of inverter components.

The Control Hardware

The hardware design is implemented with a microprocessor, D/A converter, switchmode driver and two power modules for the high current drive for a simple and integrated solution.

The bridge is constructed with two TO-240 TRANSPACK power modules of half bridge configuration, SGS30DB040D which permit fast acceleration of the motor and a compact structure.

The microprocessor allows simplicity and flexibility e.g. motor speed is controlled by a six bit word which accurately sets the speed between 0.5% and maximum.

Study of the System Behaviour

The system behaviour is studied to analyse the maximum stress conditions on the bridge corresponding to possible operating conditions, the algorithm of acceleration, braking, and inversion of the speed are demonstrated. The objective is to obtain the maximum performance possible with the transistors chosen for the bridge.

Balance of the Bridge

The evaluation of power absorbed by the various parts of the system demostrates the efficiency of the design.

Detailed analysis of power absorbed in the motor and power dissipated in the bridge qualifies this design.

This study involves particularly heavy operating conditions for the power circuitry which verifies the excellent performance of the TRANSPACK devices above all in terms of switching speeds and low losses i.e. efficiency.

following:

1) $V_A = RA\ I_A + LA\ di_A/dt + E$

2) $C_M = J\ d\Omega/dt + D\Omega + Cr$

3) $E = K_v\ \phi\ \Omega$

4) $C_M = K_T\ \phi\ I_A$

Where:

V_A	= Armature Voltage	(Volts)
I_A	= Armature Current	(Ampere)
R_A	= Stator Resistance	(Ω)
L_A	= Stator Inductance	(H)
E	= Electro Motive Force	(Volts)
C_M	= Torque	(Nm)
C_r	= Friction	(Nm)
J	= Inertial Moment	(Kg. m^2)
Ω	= Angular Velocity	(rad/sec)
ϕ	= Stator Magnetic Flux	(Weber)
D	= Kinetic Friction	(Nm)
K_v	= Back EMF Constant	(V.s)
K_T	= Torque Constant	(Nm A^{-1})

From the balance of energy:

$C.\Omega = E.I_A$ where C equals the motor output (Watts)

$$= \frac{E}{K_v\ \phi} K_c\ \phi\ I_A \text{ from which } K_c = K_v$$

The differential equations were resolved by the Runga – Kutta method for solving non linear equations.

With the simulation it was proposed to forecast the following behaviour:

- Maximum Peak Current
- Ripple current at various chopper frequencies
- Response speed of the system
- Function in steady state

The phenomena were studied with the intention of seeing the maximum values of the observed parameters rather than instantaneous values in order to optimise the choice of inverter components. The simulation was made supposing a supply voltage of 200V.

N.B. — In Appendix A is the programme used for the simulation run on VAX.

Figures 2, 3 & 4 illustrate the simulated motor currents at chopper frequencies of 5, 10 & 20 KHz with the motor blocked and a 50% duty cycle (A = 5).

It can be seen that ripple current decreases in a practically linear relationship to the frequency, passing from 3A at 5KHz, to 0.9A at 20KHz.

The average of the current is zero as is the torque. The absorbed power is however dissipated in the motor, becoming lower as the chopper frequency increases.

Figures 5 & 6 show the trend of velocity, at 10 & 20KHz, with a 70% duty cycle (A = 7) and load torque zero. Also the ripple on the speed is strongly influenced by the chopper frequency, going from 4.22% at 10KHz to 0.84% at 20KHz. Assuring a steady state speed of 237 rad/sec the ripple varies from 10 rad/sec at 10KHz to 2 rad/sec at 20KHz.

Under identical conditions (frequency and duty cycle) the motor current analysis shown in figures 7 & 8 was made.

The ripple current and hence the torque merit observations similar to those made for the speed. From the simulations it was decided to operate with a frequency close to 20KHz both in terms of reduced losses in the motor as well as the ripple effects on speed and torque.

Fig. 2

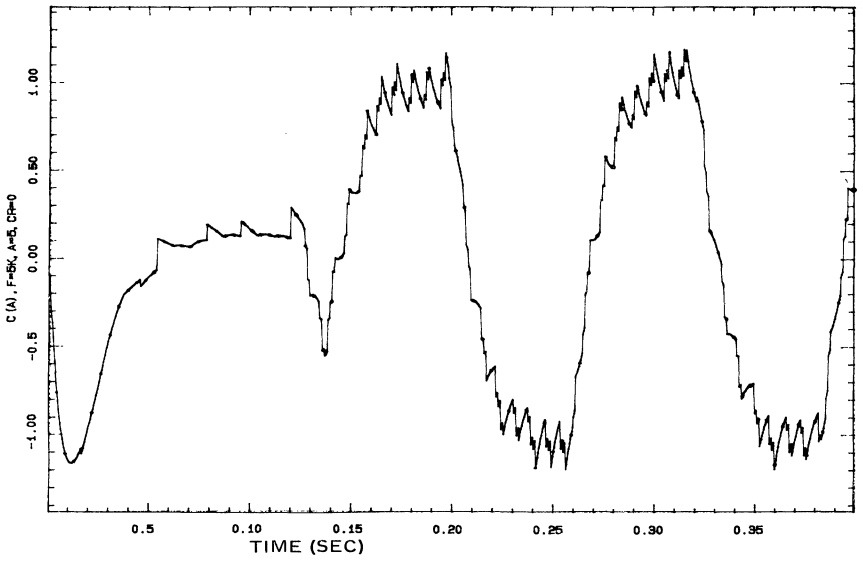


Fig. 4

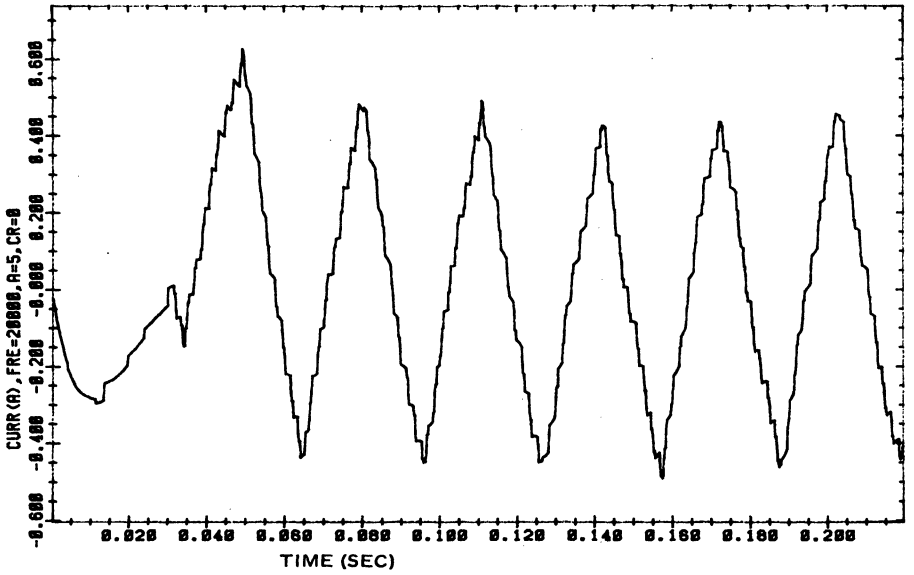

CURR(A), FRE=20000, A=5, CR=0
0.600
0.400
0.200
0.000
-0.200
-0.400
-0.600
0.020
0.040
0.060
0.080
0.100
0.120
0.140
0.160
0.180
0.200
TIME (SEC)

Fig. 5

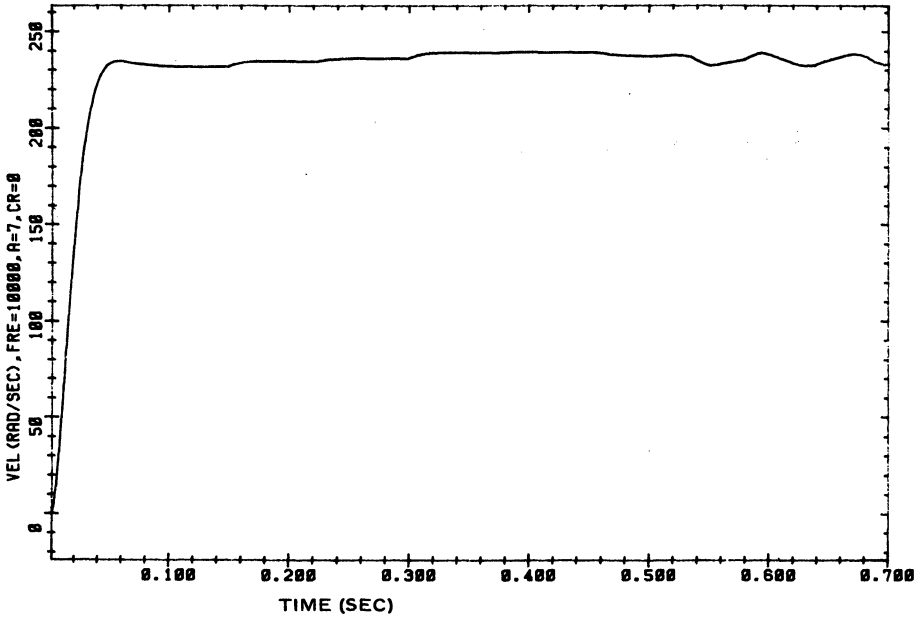

VEL (RAD/SEC), FRE=10000, A=7, CR=0
250
200
150
100
50
0
0.100
0.200
0.300
0.400
0.500
0.600
0.700
TIME (SEC)

Fig. 8

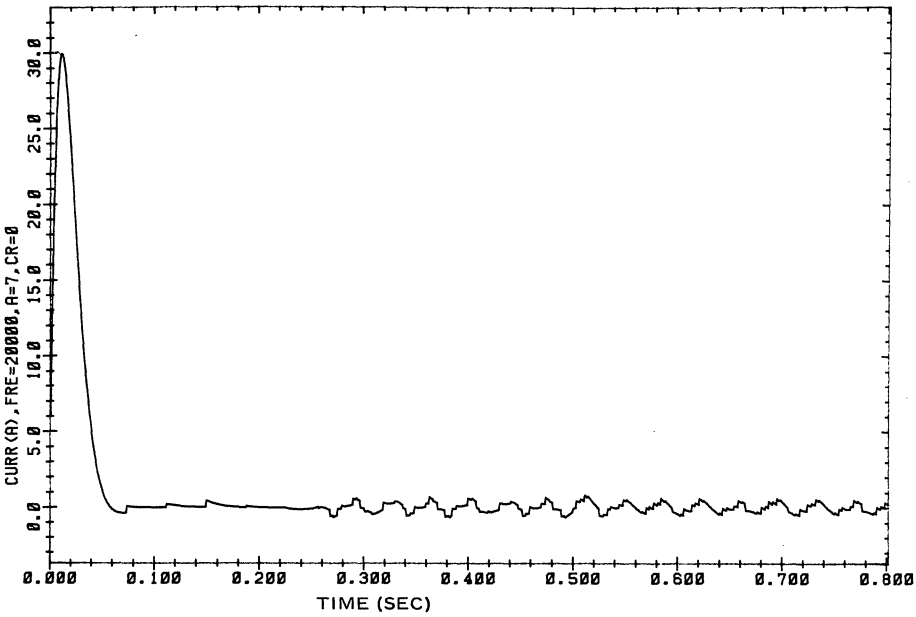
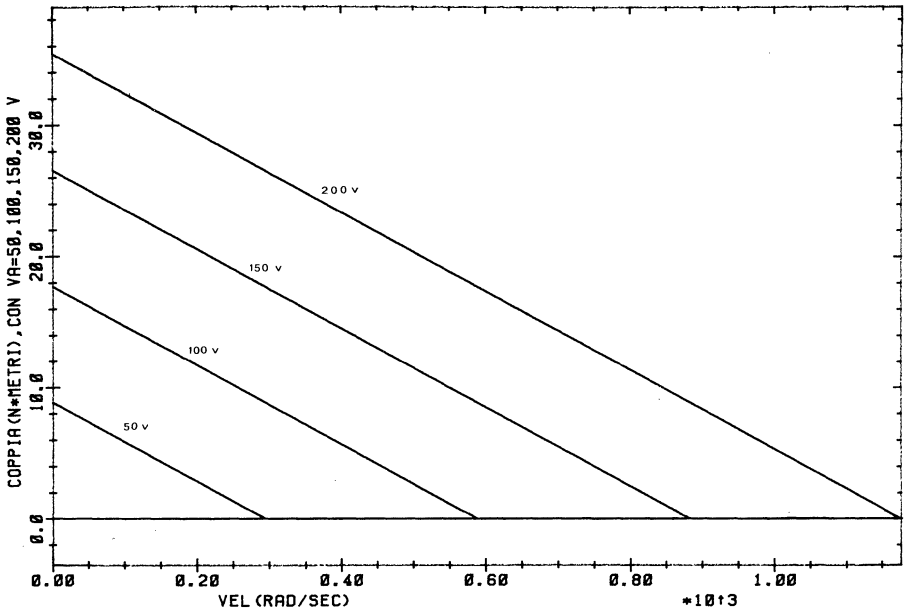

CURR(A), FRE=20000, A=7, CR=0
0.0
5.0
10.0
15.0
20.0
25.0
30.0
0.000
0.100
0.200
0.300
0.400
0.500
0.600
0.700
0.800
TIME (SEC)

Fig. 9


COPPIA(N*METRI), CON VA=50, 100, 150, 200 V
0.0
10.0
20.0
30.0
200 v
150 v
100 v
50 v
0.00
0.20
0.40
0.60
0.80
1.00
VEL (RAD/SEC)
*10↑3

Also it is possible to impose a delay between the end of one signal and the start of the complement, essential to avoid the short circuit condition on the bridge. The transfer of the signal from the controller to the high side of the bridge is via Q5 and Q6. These transistors are power devices working in the active zone with very low current and must sustain a voltage 5V greater than the voltage applied to the motor (fig. 11a).

This solution avoids the use of a transformer and is aimed towards the eventual integration of the power stage. The drive of the transistors in the bridge was realised with a simple integrated solution of the SGS L149, whose power for the high side is referred to the voltage at the motor terminals which follows the variations.

The power for the motor is provided by a full bridge circuit permitting operation in all 4 quadrants.

The two half bridge TRANSPACK, SGS30DB040D, are built using darlingtons without integrated collector – emitter diodes which permits full use of the fast freewheel diodes incorporated in the power module and high frequency drive of the motor. The voltage waveforms on the motor are illustrated in photo 1.

Fig. 11a

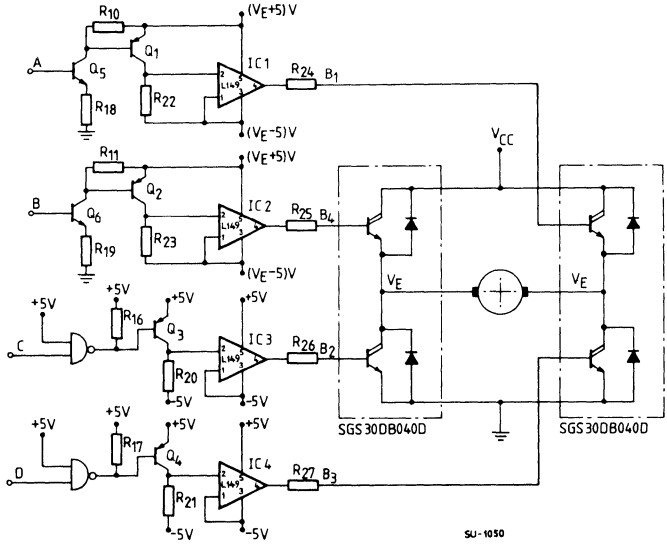
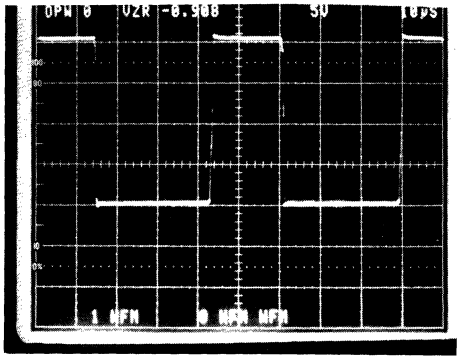
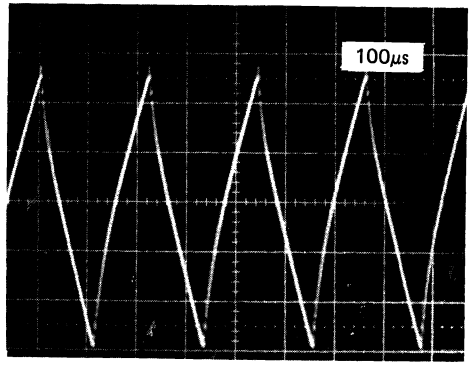


Photo 1 – Motor voltage



V = 50V/div
t = 10μs/div

Photo 2A – Ripple of 3A at 5KHz



I = 0.5A/div

Study of the system behaviour

To analyse the maximum stress condition on the bridge corresponding to possible operating conditions, the algorithm of acceleration, braking and inversion of the speed were performed. The objective was to obtain the maximum performance possible with the transistor s chosen for the bridge.

The strategy followed was to choose a speed of 3000rpm analysing the time needed to reach the speed.

Acceleration Tests

Firstly the motor was accelerated with a duty cycle corresponding to the chosen speed (steady acceleration with a drive signal duty cycle of 70%). The result of this test is shown in photo 3 & 4.

Photo 3 - Trend of the speed with only voltage changing (560 rpm/div)

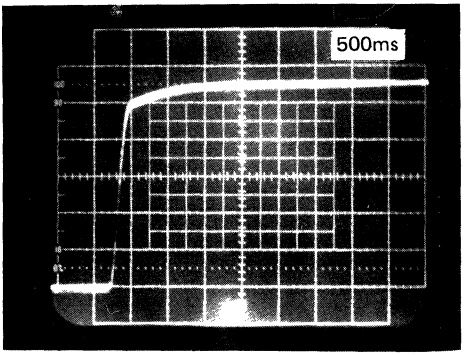
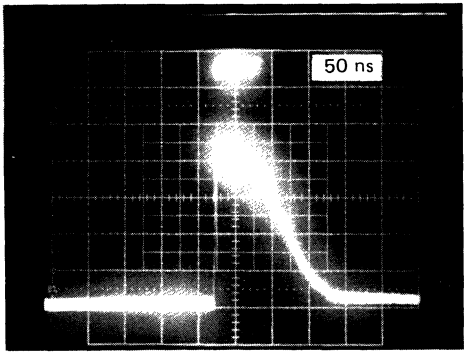


Photo 4 - Trend of the current under the same conditions as photo 3 (5A/div)



In photo 4 it is seen that the current reaches a peak of 23A in a limited number of pulses and then goes to full speed much more slowly, with a current of 0.6A. Regarding the speed, the period of the transition may be estimated as around 1.2s.

Photo 5 - The trend of the velocity with four progressive steps of voltage at intervals of 25ms (560 rpm/div)

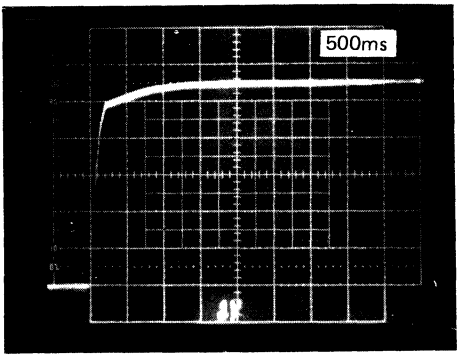
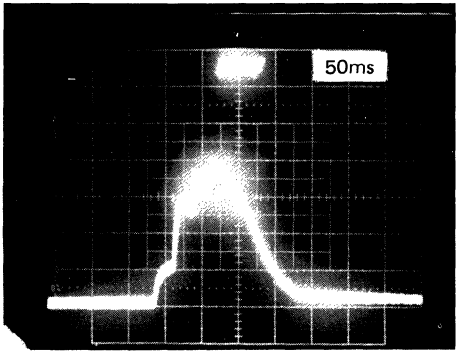


Photo 6 - The trend of the current under the conditions of photo 5 (5A/div)



Also a ramp of acceleration was tested imposing 4 increases in duty cycle of 5% with a 25ms delay between each (photo 5 & 6).

In this way the maximum current during acceleration is reduced to 20A without any significant variation of the time to reach full speed.

Photo 7 - The trend of the speed with the drive of figure 13 (560 rpm/div)

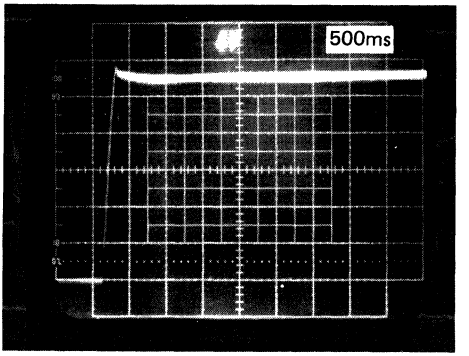
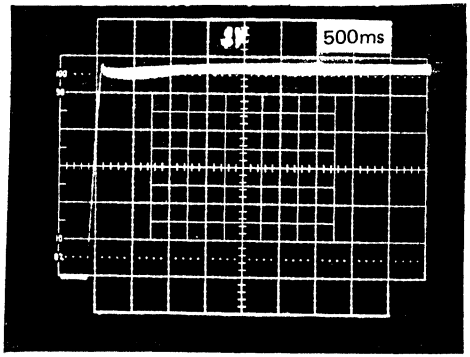
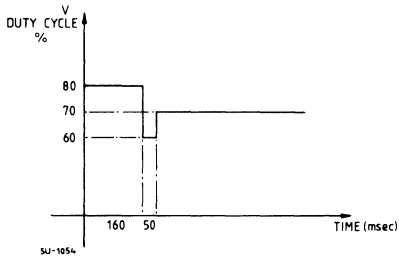


Photo 11 - Trend of velocity with a initial drive to produce 3750 rpm followed after 160ms by a drive to produce 2250 rpm and finally after 50ms by a drive to produce 3000 rpm





Speed Reversal

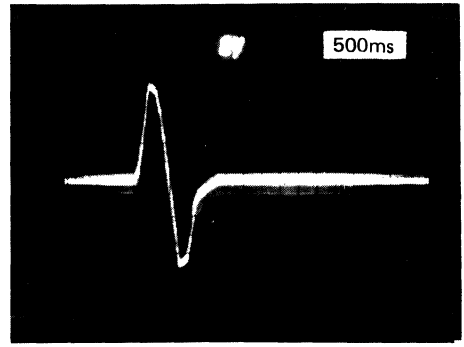
Having reached the maximum, the objective was to achieve the maximum steady acceleration and to estimate the time needed to achieve an inversion of the speed passing from +3000rpm to -3000rpm having supposed that this is the most critical stress on the bridge.

There was first analysed the phenomena of braking and it was seen that braking too quickly may cause a change of function, making the motor a generator and creating excess emitter base voltage up to a situation intolerable for correct operation of the bridge components.

This phenomena was taken into account to achieve the most rapid braking possible without over-stressing the bridge components.

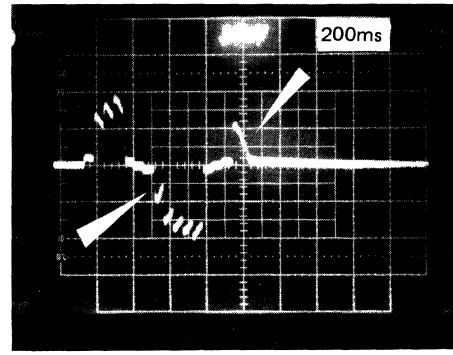
We succeeded in this way to obtain a time, from +3K to - 3Krpm, of about 500ms, as shown in photo no. 12 where the achievment of a steady state is not considered but only the transition from one speed to another.

Photo 12 - Trend of velocity (1090 rads/sec/div)



The behaviour of the relevant currents are shown in photo 13 where points shown by the arrows are relative to the transformation of the motor into a generator.

Photo 13 - Current absorbed by the motor with the described speed invertion (10A/div)



Both the tests of acceleration and speed reversal were made with repetitive cycles, with appropriate programmes in the Nanocomputer® , for periods of several hours without creating problems for the SGS30DB040D.

Balance of the Bridge

The evaluation of the power absorbed by the various parts of the system is analysed in the following paragraph.

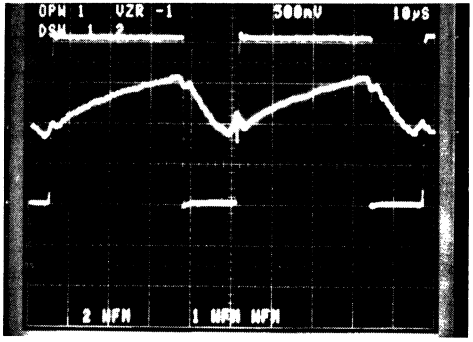
The estimates obtained give an indication of the efficiency of the control system in that it permits a ratio of the power absorbed to that of the motor.

The power was measured using the following system (fig. 14).

The chosen conditions were:

- Duty cycle of 76%
- Average motor current 1.25A

Photo 16



The power dissipated during the turn-on phase and the respective voltage and current waveforms are shown in photos 17 & 18.

Photo 17

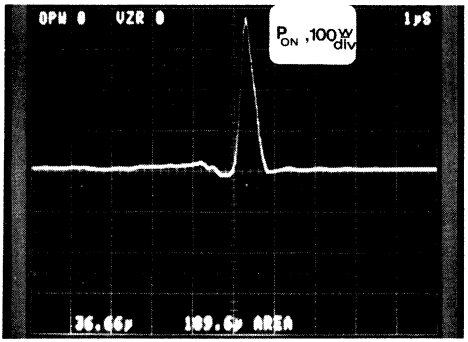
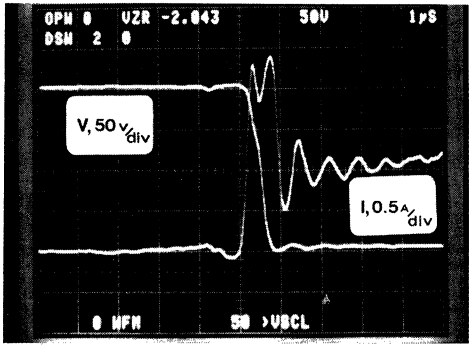


Photo 18



From the photo of the power it is possible also to measure the energy dissipated. This corresponds to an average power of:

P_{ON} = E x F = 189.6μJ x 21700Hz = 4.1W

The power dissipated during the turn-off phases and the respective waveforms are shown in photo 19 & 20.

The energy dissipated in this case is 118μJ thus:

P_{OFF} = E x F = 118.5 x 21700 = 2.47W

Photo 19

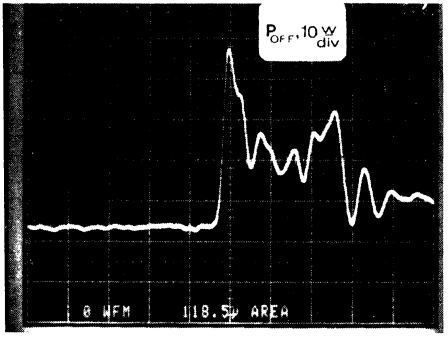
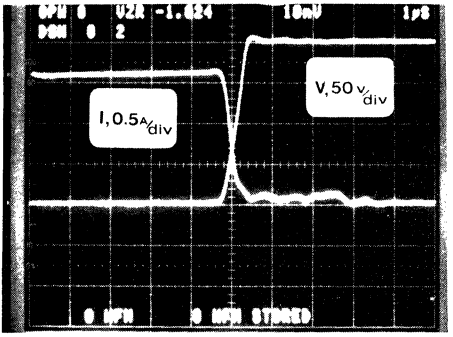


Photo 20



The dissipation of the conduction phase is not conveniently measured by the method used so it was preferred to make an estimate.

At the average current of 1.25A from the characteristic curves a $V_{CE(sat)}$ of 0.8V is found.

$P_{COND.}$ = 1.25A x 0.8V x 0.76 = 0.76W

Taking into consideration that the conduction phase is 76% of the full period:

The power dissipated in a transistor of the bridge is thus:

$P_{TOT} = P_{ON} + P_{OFF} + P_{COND}$ = (4.1 + 2.57 + + 0.76) W = 7.43W

CONCLUSION

During this work a study was made, both in theory and application, of the control of a DC motor. For this study, advantage was taken of the flexibility offered by using a microprocessor to make many tests. This allowed a comprehensive analysis of the behaviour of the SGS30DB045D TRANSPACK.

This involved the recreation of particularly heavy operating conditions for the power circuitry, which verified the excellent performance of the TRANSPACK devices, above all in terms of switching speed and low losses. Also studies were made of a number of drive circuits for the power transistors, useful for future projects.

APPENDIX A (continued)

```
      CLOSE (UNIT=11)
      STOP
      END


      SUBROUTINE RKUTTA(N,X,Y,FUNC,H,XF,YF,CR,RA,XLA,FL,CM,E,RJ,
      Kc,Kv,L,T,T1,T2)
      DIMENSION Y (20),YI(20),YF(20),D(20),A(5)
      REAL KC,KV
      A (1) = H/2
      A (2) = A (1)
      A (3) = H
      A (4) = H
      A (5) = A (2)
      XF=X
      DO 10 K=1,N
      YF (K) = Y (K)
10    YI (K) = Y (K)
      DO 20 J=1,4
      CALL FUNC (XF,YI,N,D,CR,RA,XLA,FL,CM,E,RJ,Kc,Kv,L,T,T1,T2)
      XF=X+A (J)
      DO 20 K=1,N
      YI(K)=Y(K)+A(J)*D(K)
20    YF(K)=YF(K)+A(J+1)*D(K)/3
      RETURN
      END


      SUBROUTINE FUNC (X,Y,N,D,CR,RA,XLA,FL,CM,E,RJ,Kc,Kv,L,T,T1,T2
      DIMENSION Y (20),D (20)
      REAL KC,KV
      DO 16 M=0,(L-1)
      IF(X-M*T).LE.T1) GO TO 11
      IF((X-M*T).LE.(T1+T2)) GO TO 12
18    CONTINUE
11    VA=400.
      GO TO 21
12    VA = - 400.
      GO TO 21
21    CONTINUE
      D (1) = (VA-E-RA*Y(1))/XLA
      D (2) =(CM-CR)/RJ
      RETURN
      END
```

```
'dc motor control'
ln  addr  obj code t e i line   source statement

 1  D85F  3E02              58  exit2   ld      a,02h
 2  D861  26FF              59  loop1   ld      h,0ffh
 3  D863  2EFF              60  loop2   ld      l,0ffh
 4  D865  2D                61  loop3   dec     l
 5  D866  C265D8            62          jp      nz,loop3
 6  D869  25                63          dec     h
 7  D86A  C263D8            64          jp      nz,loop2
 8  D86D  3D                65          dec     a
 9  D86E  C261D8            66          jp      nz,loop1
10  D871  79                67          ld      a,c
11  D872  B7                68          or      a
12  D873  C21CD8            69          jp      nz,main
13  D876  16FF              70  init2   ld      d,0ffh
14  D878  1E1F              71          ld      e,1fh
15  D87A  0608              72          ld      b,08h
16  D87C  0E08              73          ld      c,08h
17  D87E  7A                74          ld      a,d
18  D87F  D309              75          out     (piod),a
19  D881  3E08              76          ld      a,08h
20  D883  26FF              77  loop4   ld      h,0ffh
21  D885  2EFF              78  loop5   ld      l,0ffh
22  D887  2D                79  loop6   dec     l
23  D888  C287D8            80          jp      nz,loop6
24  D88B  25                81          dec     h
25  D88C  C285D8            82          jp      nz,loop5
26  D88F  3D                83          dec     a
27  D890  C283D8            84          jp      nz,loop4
28  D893  78                85  exit3   ld      a,b
29  D894  B7                86          or      a
30  D895  CAACD8            87          jp      z,ind6
31  D898  78                88          ld      a,b
32  D899  D605              89          sub     05h
33  D89B  FAA5D8            90          jp      m,ind5
34  D89E  05                91          dec     b
35  D89F  15                92          dec     d
36  D8A0  15                93          dec     d
37  D8A1  15                94          dec     d
38  D8A2  C3C5D8            95          jp      out1
39  D8A5  05                96  ind5    dec     b
40  D8A6  14                97          inc     d
41  D8A7  14                98          inc     d
42  D8A8  14                99          inc     d
43  D8A9  C3C5D8           100          jp      out1
44  D8AC  79               101  ind6    ld      a,c
45  D8AD  B7               102          or      a
46  D8AE  CAC5D8           103          jp      z,out1
47  D8B1  79               104          ld      a,c
48  D8B2  D605             105          sub     05h
49  D8B4  FABED8           106          jp      m,ind7
50  D8B7  0D               107          dec     c
51  D8B8  1D               108          dec     e
52  D8B9  1D               109          dec     e
53  D8BA  1D               110          dec     e
54  D8BB  C3C5D8           111          jp      out1
55  D8BE  0D               112  ind7    dec     c
56  D8BF  1C               113          inc     e
57  D8C0  1C               114          inc     e
```

```
'dc motor control'
ln   addr   obj code t e i line   source statement

 1   D926   D605              172           sub     05h
 2   D928   FA32D9            173           jp      m,ind10
 3   D92B   0D                174           dec     c
 4   D92C   1D                175           dec     e
 5   D92D   1D                176           dec     e
 6   D92E   1D                177           dec     e
 7   D92F   C339D9            178           jp      out2
 8   D932   0D                179   ind10   dec     c
 9   D933   1C                180           inc     e
10   D934   1C                181           inc     e
11   D935   1C                182           inc     e
12   D936   C339D9            183           jp      out2
13   D939   78                184   out2    ld      a,b
14   D93A   B7                185           or      a
15   D93B   CA44D9            186           jp      z,exit9
16   D93E   7A                187           ld      a,d
17   D93F   D309              188           out     (piod),a
18   D941   C347D9            189           jp      exit7
19   D944   7B                190   exit9   ld      a,e
20   D945   D309              191           out     (piod),a
21   D947   3E01              192   exit7   ld      a,01h
22   D949   265F              193   loop13  ld      h,5fh
23   D94B   2E5F              194   loop14  ld      l,5fh
24   D94D   2D                195   loop15  dec     l
25   D94E   C24DD9            196           jp      nz,loop15
26   D951   25                197           dec     h
27   D952   C24BD9            198           jp      nz,loop14
28   D955   3D                199           dec     a
29   D956   C249D9            200           jp      nz,loop13
30   D959   79                201           ld      a,c
31   D95A   B7                202           or      a
32   D95B   C207D9            203           jp      nz,exit6
33   D95E   16FF              204   init4   ld      d,0ffh
34   D960   0604              205           ld      b,04h
35   D962   7A                206           ld      a,d
36   D963   D309              207           out     (piod),a
37   D965   3E08              208           ld      a,08h
38   D967   26FF              209   loop16  ld      h,0ffh
39   D969   2EFF              210   loop17  ld      l,0ffh
40   D96B   2D                211   loop18  dec     l
41   D96C   C26BD9            212           jp      nz,loop18
42   D96F   25                213           dec     h
43   D970   C269D9            214           jp      nz,loop17
44   D973   3D                215           dec     a
45   D974   C267D9            216           jp      nz,loop16
46   D977   78                217   exit8   ld      a,b
47   D978   B7                218           or      a
48   D979   CA80D9            219           jp      z,ind11
49   D97C   05                220           dec     b
50   D97D   15                221           dec     d
51   D97E   15                222           dec     d
52   D97F   15                223           dec     d
53   D980   7A                224   ind11   ld      a,d
54   D981   D309              225           out     (piod),a
55   D983   3E01              226           ld      a,01h
56   D985   265F              227   loop19  ld      h,5fh
57   D987   2E5F              228   loop20  ld      l,5fh
```

TRANSISTOR OVERSTRESS IN BRIDGE CIRCUITS FOR MOTOR CONTROL APPLICATIONS

Interference by the anti-parallel diodes

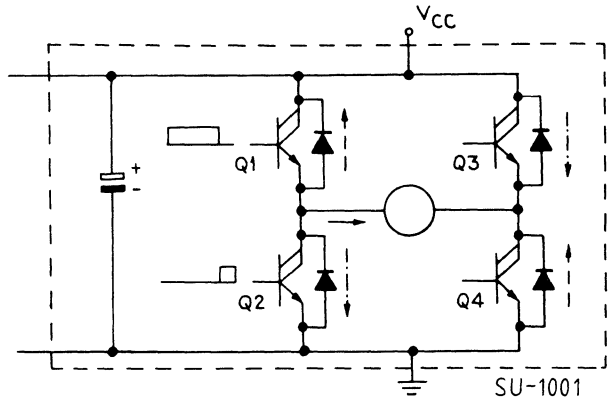
INTRODUCTION

Certain industrial drives used in robots, servos and avionics must be capable of exceptional performance to allow for very rapid speed variations. The phenomena involved, especially when braking, has been analysed to determine the stresses on the power devices in a bridge circuit driving a small dc permanent magnet motor. Although this investigation was carried out on a dc motor, the conclusions are of general validity for almost all motors. The purpose of the investigation was to locate the dangerous conditions created by the reciprocal influence of the power transistor (or darlington) and the associated fast recovery diode.

When braking the motor abruptly, the motor current reverses with respect to the previous phase, this is a consequence of the rotational energy stored in the motor which is converted into electrical energy and fed back to the filtering capacitor in parallel with the bridge.

Very high di/dt values are associated with these conditions due to both the switching of the bridge components and the fact that the supply generator faces a low impedance. These are highly critical conditions and the result can be very dangerous for the electronic components.

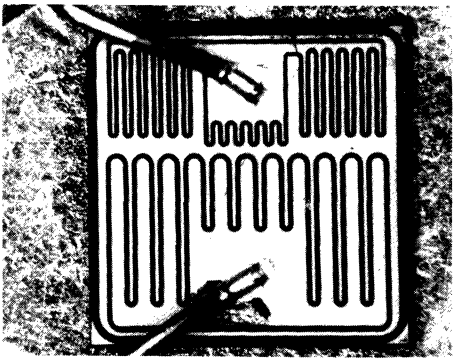
Fig. 1 - Current flows during normal drive and braking conditions



- Continuous line - current path during normal drive conditions
- Dashed line - current path during braking when Q2 and Q3 are off
- Dash-dot line - current path during the conduction of Q2 and Q3

To make measurement easier a single chip darlington type SGSD310, analogous to the SGS50DB045D, was damaged intentionally on the curve tracer by a reverse collector to emitter breakdown (the SGSD310 chip can typically withstand up to 12 or 14V in this condition).
It is evident that the failure mechanism is the same in both cases and consequently, the operating conditions that can force the transistors into reverse conduction must be investigated.

Photo 3 - The SGSD310 chip which failed during simulated overstress conditions



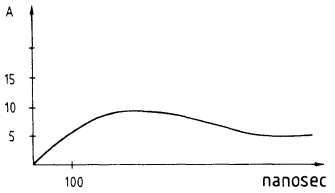
PEAK FORWARD VOLTAGE OF THE DIODE

The peak forward overvoltage (V_{FP}) on the bridge diodes is generated by very rapid current variations. In order to evaluate these variations a discrete bridge was constructed to make the diodes accessible for measurement. Each switch in the bridge was made up from three SGSD310 darlington transistors and one SGS8R20 diode. i.e. the configuration as one switch inside the TRANSPACK module.

The motor was accelerated abruptly bringing the duty cycle from 50% (zero speed) to 85% , and then braking to zero speed again in four subsequent steps. Values of di/dt as high as 50A/μs caused by the current generated during braking were observed on the diodes.

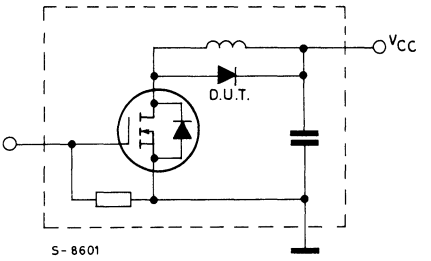
Taking into account that the discrete simulation implies stray inductances substantially larger than those inside the TRANSPACK module, the di/dt values inside the TRANSPACK are expected to be greater. In practice the connections inside a TRANSPACK are approximately 3cm long, while in the bridge constructed with discrete devices they are about 15cm long.

Fig. 2 - Waveform of the braking current through the diode



Following the above findings, some SGS8R20 diodes were tested with di/dt = 50A/μs using the circuit shown in Fig. 3.

Fig. 3 - Basic schematic of the circuit used to measure V_F



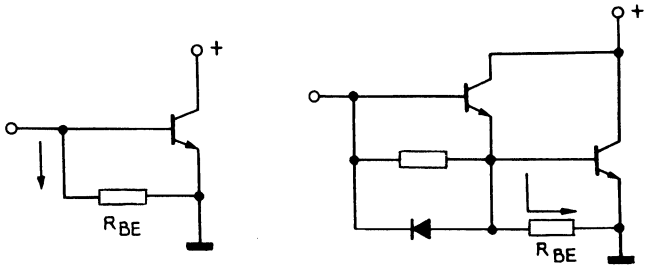
The peak voltages obtained under these conditions ($V_{F\ dyn.}$) range from 7 to 9V.

A direct measurement of V_{FP} inside the TRANSPACK module was also carried out. A special configuration was used putting a 2.2KΩ resistor in series with the diode chip where the forward voltage peak was measured. In this case peak voltages of about 18V were recorded, such a high value is due to both the V_{FP} of the diode as well as the stray inductance of internal connections. The oscilloscope photograph (Photo 5) shows the diode peak forward voltage inside the TRANSPACK module.

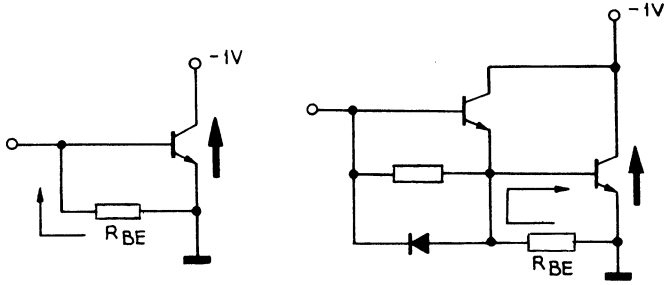
In the cases described the energy level is never high enough to imply transistor failure, due to the relatively low voltage and short length of time under stress.

During the braking phase (when the anti-parallel diode conducts) the base to emitter resistance becomes a path for positive base current when the emitter is more positive than the collector. This is the origin of reverse conduction in a transistor (or a darlington which has an integrated R_{BE} in the final transistor). The value of R_{BE} is of prime importance as the smaller it is, the larger the reverse conduction current.

Fig. 4 - The R_{BE} of the final transistor becomes a positive bias element if the collector is negative



4A) Positive collector: R_{BE} sinks the leakage current and ensures the off-state.



SU-1002

4B) Negative collector (V_F of the anti-parallel diode):

- The emitter acts as a collector and vice-versa;
- R_{BE} acts as a negative base current;
- I_B is multiplied by the gain (in reverse mode);
- A substantial charge is stored in the forward biased collector to base junction.
- It can take a few microseconds for this junction to recover to the off-state when the collector becomes positive again.

CONCLUSIONS

The analysis shows that the biasing of the collector-emitter junction of the bridge transistor by conduction of the free-wheeling diode, can overstress it and even induce a failure. The origin of the failure is not only due to the peak overvoltage of the diode, since its duration is too short (about 100ns) but primarily to the reverse conduction of the transistor during turn-off of the bridge switch. The c-b junction therefore acts as a slow recovery anti-parallel diode and if charge has been stored in this junction it causes the greatest stress on the device.

The transistor failure (disregarding the overstresses induced on purpose), is in practice triggered by more than the single switching phase described above, it is more a series of subsequent stresses at each switching cycle which leads the device into a critical state. It is also easy to appreciate that the failure concludes a phase of abnormal heating in a concentrated spot on the chip.

PARALLELING TRANSPACK MODULES

A practical example

INTRODUCTION

The requirement for a higher current rating than a single module can provide is not uncommon, but the circuit designer probably questions the practical feasibility of paralleling large transistor modules such as the SGS TRANSPACK.

Although these device are more complex than discrete transistors, in practice they can be paralleled quite easily, the main point to keep in mind is current sharing between the paralleled modules during turn-off when loaded inductively.

THE MOST COMMON CASE

Different kinds of SGS TRANSPACK modules offer practically the same power switching capability. If a device is rated for a higher voltage, it will consequently be rated for a lower current.

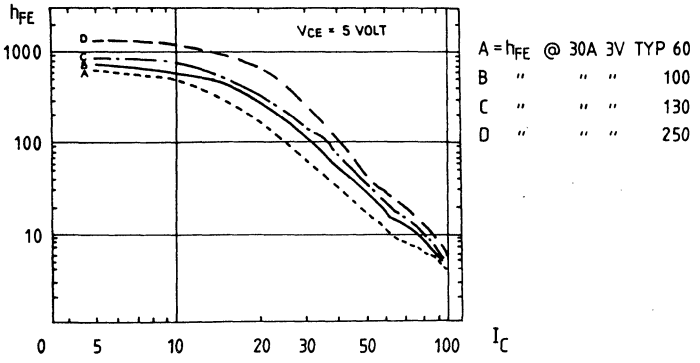
As a result, it is clear that the most common case of paralleling occurs with high voltage parts.

The SGS30DA070D has been selected for this example as it represents the highest current rating in the high voltage range of TRANSPACK modules.

SGS30DA070D IN PARALLEL

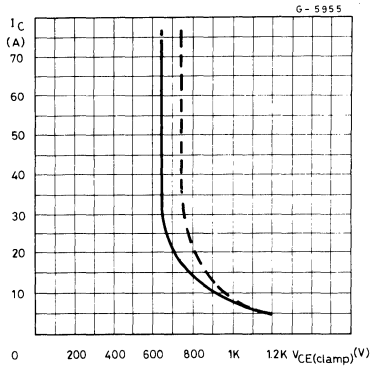
Four modules were used for the practical investigation and the relevant h_{FE} curves versus I_C can be seen in Fig. 1.

Fig. 1 - h_{FE} curves of four SGS30DA070D modules



The reverse bias safe operating area was obtained using the test driving circuit shown in Fig. 5. The RBSOA characteristics for a single module (Fig. 6) and the three modules in parallel (Fig. 7) show that the high voltage boundary is the same for both arrangements.

Fig. 7 - RBSOA of the three devices in parallel



The addition of a 1.2Ω resistor in the test driving circuit to limit the negative base current improves the high voltage boundary of both RBSOA characteristic curves, the dotted line corresponds to the new boundary.

THE BEST CHOICE

This example demonstrates the performance of devices which were not specifically selected for the test. A further improvement can be achieved if parts with very close h_{FE} values are paralleled together, ideally the three parts should remain within a ± 10% h_{FE} range.

h_{FE} matching ensures that the paralleled parts have almost the same storage time and that none of them supports the entire load current, during the interval between turn-off of one module and turn-off of the other two.

The high switching speed of SGS devices helps to minimise any minor variations between matched modules.

CONCLUSIONS

Care must be taken to ensure that current is equally shared between paralleled modules and layout is optimised to reduce stray inductance in the interconnection leads.

The easiest way to ensure a fair sharing of the current is by adding a seperate speed up diode and bias resistor network to each module. However, this will not prevent the possibility of current overshoot in one module during turn-off (as shown in Fig. 4) so for optimum results it is best to ensure current matching during turn-off.

The most practical way is to use parts with h_{FE} values within a ± 10% band for paralleled operation. SGS TRANSPACK power modules can be supplied in gain groups to suit customer applications.

ROBUSTNESS OF HIGH VOLTAGE POWER TRANSISTORS

INTRODUCTION

Most semiconductor manufacturers publish safe operating area (SOA) curves of some form in their data-sheets. These published curves are intended to convey to the user, the electronic equipment designer, a measure of the device robustness. The forward bias safe operating area (FBSOA) indicates the collector emitter voltage and current capability with the base emitter junction forward biased. The reverse bias safe operating area (RBSOA), as the name implies, indicates the collector emitter voltage and current capability with the base emitter junction reverse biased. This curve is used to determine the locus of the transistor operating point during the transition from forward biased conduction to the cut-off state.

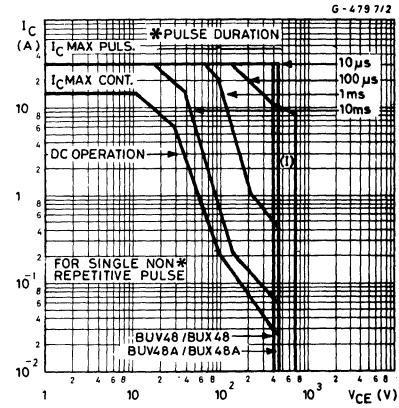
Generally speaking, safe operating area curves have been published for the transistor case temperature at 25°C. Derating is required, the amount being dependent on the transistor operating temperature and the temperature derating factor. Different derating factors are applied by some manufacturers to different parts of the SOA curve, depending on the failure mechanism which limits the transistor performance in that area. Thus, it is common to see both 'power derating' and '$I_{s/b}$ (second breakdown) derating' factors published. Additions to the standard SOA curves are being made as the capabilities and the understanding of the process technology are improved. In particular, extensions above the V_{CEO} rating of the transistor are seen in both FBSOA and RBSOA curves to indicate the transistor capability during 'switch-on' and 'switch-off' transitions.

Non repetitive overload safe area curves are also appearing, and these will be found particularly useful in the motor control area However, a degree of caution is necessary on the part of the design engineer in interpretation of this additional information. The semiconductor manufacturer will have defined the test conditions for which the overload safe area curve applies. Disparity between the application circuit and the semiconductor manufacturers test circuit, including any preconditioning, can cause significant differences in the ability of the transistor to withstand an overload.

FORWARD BIAS SAFE OPERATING AREA

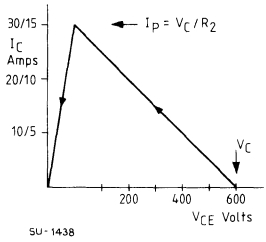
The forward bias safe area for the SGS BUX48/ SGS BUV48 transistor families is shown in figure 1. The curves apply for a case temperature of 25°C. The lower curve represents the continuous conduction case, with collector current, I_C, limited to 15 amps and collector emitter voltage, V_{CE} limited to 400V, or 450V for the 'A' part, 600V for the 'B' part or 700V for the 'C' part. Beyond the 15A 10V point on the curve, the current rating falls in conformance to the maximum power rating of the transistor. There are 2nd and 3rd break points (charge of gradient) on the curve at 6A and 0.2A. In these areas the transistor is no longer limited by total power rating, but by second breakdown.

Fig. 1 - BUX48/BUV48 forward bias safe operating area



The outer set of curves represent the pulse current capability, as opposed to the DC capability of the transistor. The rating applies for a single pulse, so that the duty cycle effect and resulting temperature increase is discounted. All of these curves are terminated at the V_{CEO} rating (400V - 700V) of the transistor. A small additional area, marked

Fig. 5 - Theoretical operating locus in FBSOA test

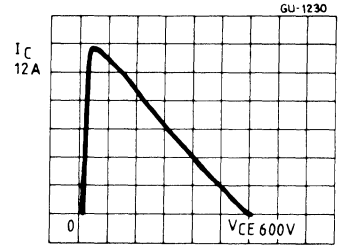


returning the inductive energy stored in L to the supply, V_B. Resistor R3 connected in series with the rectifier D1 shapes the load line and so determines the locus of the operating point of the T.U.T. during 'turn off'. The peak voltage across the T.U.T. will be:

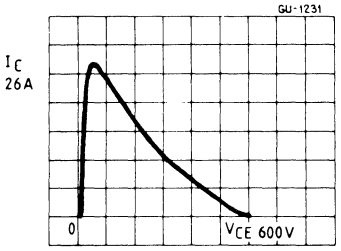
$$V_{CEpk} = V_B + I_{Cpk} \cdot R3 + V_F\ D1$$

This simple equation neglects the effects of circuit wiring inductance and the forward recovery time of the rectifier, D1. Some adjustment in V_B or R3 value may be required to compensate for these effects. Figures 8 and 9 illustrate the locus of the operating point of the T.U.T. during 'turn off'.

Fig. 6 - Oscilloscope display of operating locus in FBSOA test



a) BUX48A



b) BUX98A

Fig. 7 - Reverse bias safe area test circuit

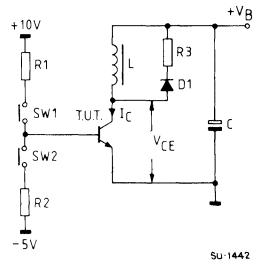
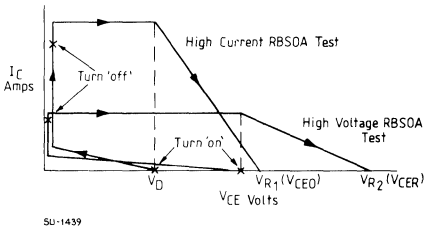


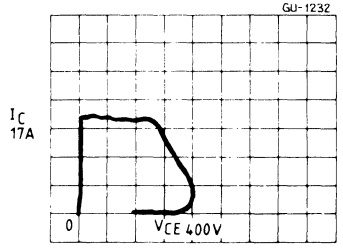
Fig. 8 - Theoretical operating loci in RBSOA tests



The reverse bias SOA test is performed in 2 stages. This is to achieve a 'best fit' to the SOA curve. The first part of the test exercises the high current RBSOA extending up to the V_{CEO} for the transistor. The second part exercises the low current, high voltage area extending to V_{CER}. Figure 7. Illustrates the test circuit. Switch 1 closes to turn the T.U.T. 'on'. The condition time is controlled to limit the peak collector current.

As switch 1 opens, switch 2 closes reverse biasing the base emitter junction of the T.U.T. Following the storage time delay, during which time the excess charge in the collector base junction is extracted, the collector emitter voltage rises instantaneously to V_B when the rectifier, D1 conducts

Fig. 9 - Oscilloscope display of operating loci in RBSOA test



a) BUX48A High Current RBSOA

TECHNOLOGY RELIABILITY AND APPLICATIONS OF SGS HIGH VOLTAGE NPN TRANSISTORS

Introduction

The basic technology chosen for high voltage (V_{CEO} > 400V - V_{CBO} > 600V) transistors is fundamental to their in-circuit performance as well as their "built-in" reliability.

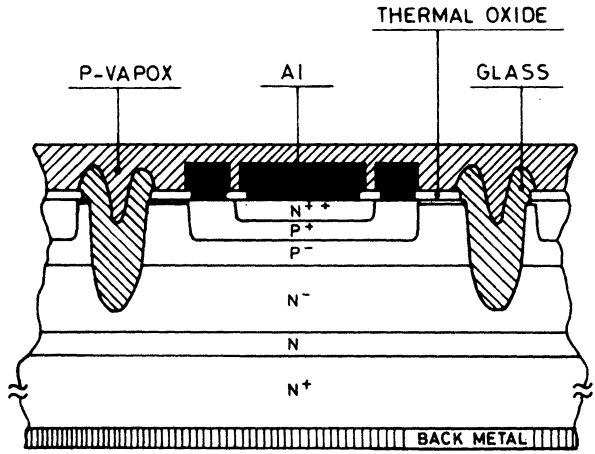
Also the technology effects the wafer size which may be used in production, as well as the yields. In some cases also packaging options may be restricted. These are important factors influencing the price and availability for any semiconductor device.

Subject

This note discusses the SGS Multiepitaxial Mesa process used for a wide variety of industry standard products as well as some innovative types.

This technology is illustrated in simplified form in figure 1, figure 2 shows an actual cross section of the edge of a die made up of several scanning electron microscope pictures.

Fig. 1a - Multiepitaxial Mesa wafer simplified cross section



handled allowing SGS to use 4" and 5" wafers with ease.

Following diffusion is the etching of the mesa which is filled with a very pure glass by an SGS patented selective deposition process which avoids any contaminants such as photoresist which may not be entirely evaporated during the fusion of the glass. The aluminium top metal is now deposited and the pattern defined. The entire top of the wafer is now protected by a thick deposited oxide in which windows are opened for bonding the base and emitter connecting wires.

Finally the wafer is reduced to the correct thickness, removing the excess N^+ silicon by grinding the back of the wafer, after which the back is metallized.

Packaging

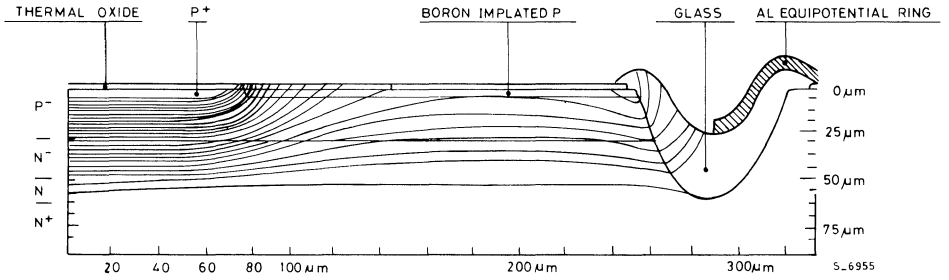
As the die must be separated from the wafer before mounting in the package the fact that SGS cuts the silicon outside the mesa and its glass filling, eliminates the risk of mechanical damage to the passivation.

As the sawing creates a short circuit at the edge of the die from the collector to the field plate no "flashover" can occur in the package between the header which is at collector potential and the top of the die, which in alternative half mesa technologies will be at base potential. The surface is covered with a thick oxide as previously mentioned so no arcing occurs along the surface.

This process of passivation also ensures high reliability in plastic packages.

This technology also allows wafers to be 100% probe tested to high voltage specifications, an important point for users of high voltage transistors in chip form for hybrid assemblies.

Fig. 3 - Section of Mesa with simulated equipotential lines



Reliability

In the reliability of a high voltage transistor the voltage stress on the surface of the silicon in the region of the collector/base interface is very important. This region must be protected from contamination. By terminating the collector-base junction on the edge of the mesa, and using glass the sealing against potential contaminants is assured. The use of the aluminium field plate ensures the glass is kept at a constant charge. The surface of the P layer is treated with an ion implantation to ensure a very well controlled surface doping thus aiding close control of the electric field strength distribution and leakage currents. SGS has developed computer simulation programs which can predict the field strength enabling the design to be optimised for reliability. Figure 3 shows the equipotential lines superimposed on the actual device cross section demonstrating the low stress on the surface.

SGS continually monitors the reliability of the process by sampling production on a weekly basis. The high temperature reverse bias test (HTRB) is used to evaluate the stability and quality of the passivation.

Devices are subjected to T_{amb} = 125°C with the base-emitter shorted, and 600V d.c. is applied to the collector. Figure 4 shows typical results of leakage currents measured at V_{ces} = 900V, a point on the line at 45 degrees indicates no drift in

Fig. 4 - Leakage current stability in HTRB life tests

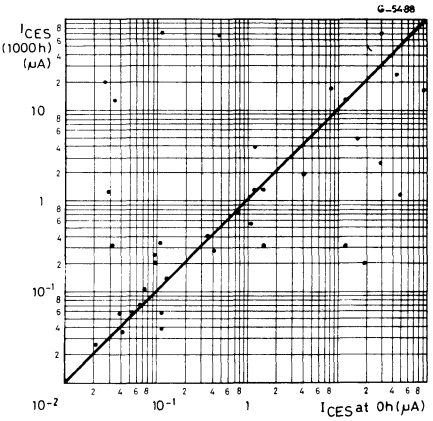
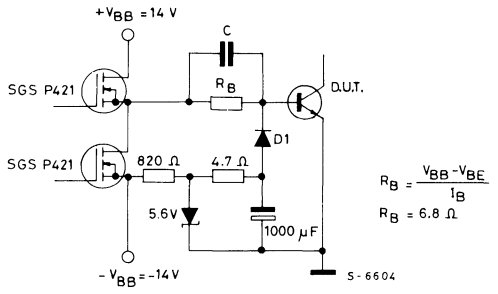


Fig. 9 - I_{B1} waveform for improved dynamic saturation

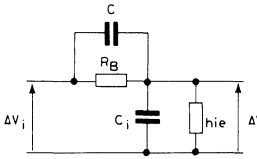
$V_{CE\ (sat)}$ dynamic test circuit



$R_B = \frac{V_{BB} - V_{BE}}{I_B}$

$R_B = 6.8\ \Omega$

Equivalent input schematic circuit at turn-on



$\Delta V_o = \Delta V_i \frac{C}{C_i + C}$

if $C \gg C_i$ $\Delta V_o = \Delta V_i$

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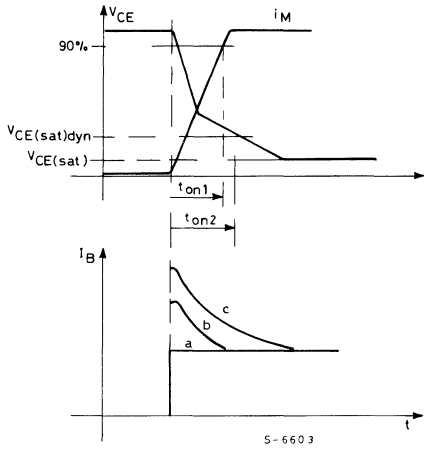
Remarks to $V_{CE\ (sat)}$ dyn. test circuit



The speed-up capacitor decreases the $V_{CE\ (sat)}$ dyn. as shown in the diagram and modifies the shape of the base current with an overshoot.

SECOND BREAKDOWN IN POWER TRANSISTORS

One of the basic failure machanisms in power transistors is second breakdown.

Under this term, various physical phenomena which are completely different are included. They depend on the different use of transistors in the circuits and have in common the electrical and thermal instability inherent in transistors themselves.

The conduction behaviour of an emitter base junction and the current gain of a transistor depend significantly on the temperature and increase as a function of the temperature. Electrical and thermal instabilities may simultaneously act within the device, thereby giving rise to destructive second breakdown mechanism.

An understanding of this mechanism is of great importance for a safer and optimum application of a power transistor.

A distinction should be made between direct second breakdown ($I_{s/b}$ or more commonly SOA), which is distinguished by a normal direction of base current I_B (entering in an NPN transistor) and inverse second breakdown ($E_{s/b}$), when I_B is in the opposite direction (extracted from an NPN transistor). The limits to which a transistor may be used without entering into $E_{s/b}$ are defined by the reverse bias safe operating area (RBSOA).

DIRECT SECOND BREAKDOWN ($I_{s/b}$)

An important information for the power circuit designer is the locus of I_C - V_{CE} points defining the boundary between stable and unstable operation of forward biased transistors. This locus defines the SOA (safe operating area) that is the area of the $\log I_C$ - $\log V_{CE}$ plane which may be used without any risk in DC current conditions or with different width pulses at a known temperature. A typical SOA is shown in Fig. 1.

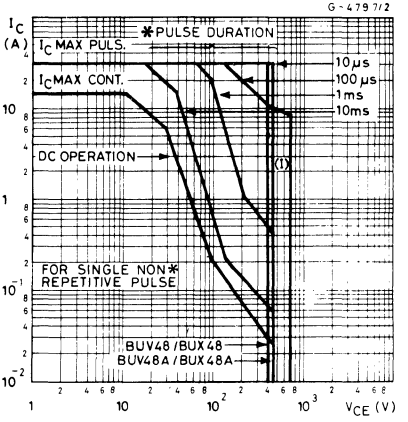
The limits of this area are the following:

1) The A-B section represents the upper limit of the collector current that may normally be used, generally limited by wire bonds. Operation at higher currents may cause damage to the wires of their bonding.

2) The B-C section is the -1 slope curve section (i.e. the section with constant dissipation) defined by:

$$V_{CE} \times I_C = P_{max} = \frac{(T_j max - T_o)}{R_{th}}$$

Fig. 1 - Safe operating areas



A side drop of 26mV reduces by a 1/e factor the injected emitter current.

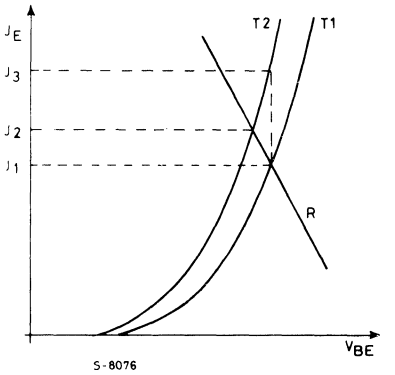
A concentration is therefore generated of the current at the emitter periphery, therefore the active silicon area is reduced and hot spots occur, leading to an effective increase of the thermal resistance. As a result, the maximum dissipable power is decreased.

When V_{CE} is increased the effect of the base - collector electric field is to increase the base current concentration.

Different techniques may be adopted to limit the $I_{s/b}$ phenomenon. Fundamentally, they consist of minimising the mechanisms that trigger electrical and thermal instabilities in the transistor. The basic techniques are:

1) Minimization of crystal damages, metal impurities and of doping disuniformities.
2) Optimization of package and die attach techniques, to minimize the thermal resistance on which the stability factor S depends. Disuniformities of silicon die bondings to the case may give rise to adverse variations of R_{th} as a macroscopic parameter for the dice as a whole, but also to significant variations between different points, giving rise to premature second breakdown.
3) Increase of the base thickness to reduce the high current densities (due to emitter crowding) flowing through the collector base junction (where the electric field is localized), so that the density of the dissipated power is decreased. High base thicknesses, however, will result in lower cut off frequencies and slower switching times.
4) Optimization of the horizontal geometry.
5) Introduction of distributed ballast resistances connected in series with the base, the emitter or both, which tend to give a negative feedback to thermal runaway, therefore stabilizing the device. Fig. 3 shows the J_E/V_{BE} characteristic curves for two points in the junction, at different temperatures (T2 > T1).

Fig. 3



It may be seen that the introduction of a ballast resistance in series with the base or the emitter may reduce from J_3 to J_2 the current density in the hot spot.

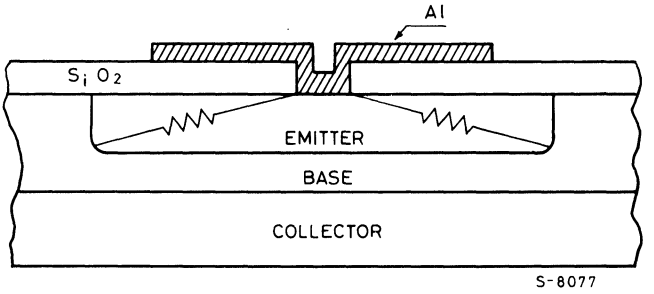
The emitter ballast resistance is generally obtained by opening emitter contacts thinner than the emitter strip (Fig. 4).

In this way it is possible to limit the current density at the boundaries of the emitter. These resistances show the drawback of increasing the saturation voltage of the transistor by the amount $V_{CE\,sat} = R_E \times I_{C\,sat}$.

On the other hand, the base ballast resistance is obtained through a "N^+ pocket" (in the case of NPN), around the emitter area (see Fig. 5). This N^+ diffusion, being unbiased, can't be traversed by the base current, that is therefore forced to flow below the N^+ through a small section and, in the case of a diffused base, encounters a higher resistance on the way to the edge of the emitter. In this way, it is possible to significantly improve $I_{s/b}$.

It should be noted that the SOA limits are temperature dependant and suitable derating must be applied.

Fig. 4



For low V_{CE} values, M is an insignificant factor, being very close to 1. M increases when V_{CE} is increased according to the following expression:

$$M = \frac{1}{1 - (V_{CE}/BV_{CBO})^n} \quad (2)$$

From expression (1) and (2) it is evident that h_{FE} depends on V_{CE}, becoming infinite when $M \times a_F = 1$ (BV_{CEO}).

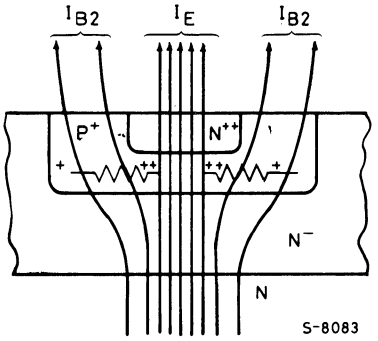
The negative slope section, which is a feature of the curves with $I_B < 0$ is due to the fact that a_F decreases at low values of the emitter current.

During turn off with an inductive load, the transistor has to operate with negative base current and a high value of I_C. It has often to reach a working area above V_{CEO}, remaining there all the time required for the inductance to be discharged (see Fig. 7). Fig. 8 shows the behaviours of I_C, V_{CE}, I_B and the power dissipated by the transistor during turn off.

The area of the dissipated power corresponds to the energy stored by the inductance $1/2 \times L \times I^2$, which is discharged into the transistor and this is called second breakdown energy ($E_{s/b}$).

Similarly to $I_{s/b}$, the voltage drop due to the reverse I_B flowing through the side resistance rbb' makes the centre of the emitter strip more biased than its periphery (Fig. 9). In this way, a current concentration occurs at the emitter centre.

Fig. 9



Let's analyse the case of an NPN transistor with diffused base and epitaxial collector, i.e. with constant concentration ND of donors doping particles.

Poisson's equation is recalled below:

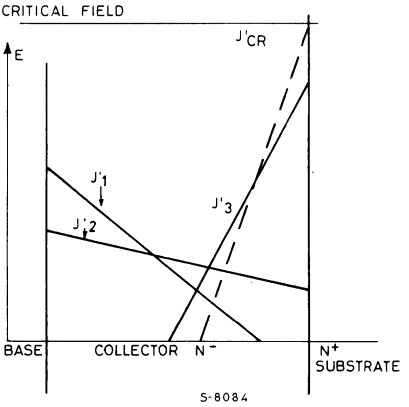
$$\frac{\partial E}{\partial X} = -\frac{\partial^2 V}{\partial X^2} = \frac{\rho(x)}{\epsilon} \quad (3)$$

The X axis is normal to the silicon dice surface, $\rho(x)$ is the charge per unit volume, ϵ is the dielectric constant of silicon. When the collector current is limited to low values, expression (3) becomes (q being the electron charge):

$$\frac{\partial E}{\partial X} = \frac{qNo}{\epsilon} \quad (4)$$

and the electric field behaviour is similar to that shown in figure 10 for $J_C = J'_1$.

Fig. 10



The voltage V_{CB} (= V_{CE}) is that given by the area of the E-X graph and is smaller than primary breakdown voltage, due to the reaching of critical field E_{cr}. In the presence of significant values of current density J_C, the expression (4) is modified due to the n concentration of electrons flowing at the speed V through the depletion layer.

$$\frac{\partial E}{\partial X} = \frac{q(ND - n)}{\epsilon} \quad \text{where } n = \frac{J_C}{qV} \quad (5)$$

At constant V_{CB}, the area limited by E has to remain constant. When J_C increases, the E-X slope varies (J'_2) until its sign is changed (J'_3) and E_{cr} is reached (J'_{cr}). At this point avalanche multiplication occurs locally of electron - hole pairs with an uncontrolled current increase and so a strip is formed with a very high temperature that gives rise to either crystal damage or silicon melting. Possible crystal defects, metal ions, junction disuniformities just further exagerate this phenomenon. The avalanche multiplication is a very fast and very localized process, therefore the device remains externally cold. The $E_{s/b}$ behaviour isn't practically influenced by the die bonding quality. High $E_{s/b}$ values can be obtained with a proper design of geometry, to limit the current crowding and, most of all, by inserting a second epitaxial layer N of intermediate doping between the collector and the substrate.

The intermediate layer creates the condition shown in Fig. 11. When the current density increases (J'_2) the electric field at the interface N^-/N is in-

SGS HIGH VOLTAGE FAST RECOVERY DIODES AND THEIR SWITCHING PERFORMANCE

INTRODUCTION

SGS decided to introduce its line of power switching modules in the TO-240 TRANSPACK package.

To solve the problem of providing fast recovery rectifiers capable of matching the high voltage/high current of the transistor chips in the TO-240 package, SGS was able to exploit its technological leadership in power semiconductors. The rectifiers were fabricated by epitaxial growth with high voltage termination structures.

SGS was the first in the industry to introduce epitaxial growth for all its power transistors. Its epitaxy capability, fully in house, makes use of the fastest epitaxy reactors in the industry.

This note describes the switching behaviour of the fast recovery rectifiers used in SGS TRANSPACK power transistor modules and the SGS35R120 series of diodes.

The turn-off and turn-on behaviour is described and the characterization is oriented to the conditions of practical use.

The TRANSPACK product range and the internal diodes

This report deals with the first three diode chips developed, table 1 gives their main characteristics.

TABLE 1

Type	I_F (A)	V_{RRM} (V)
SGS35R80	35	800
SGS35R120	35	1200
SGS60R40	60	400

The second table below shows the TRANSPACK product range and the relevant fast recovery rectifier used in each device.

TABLE 2

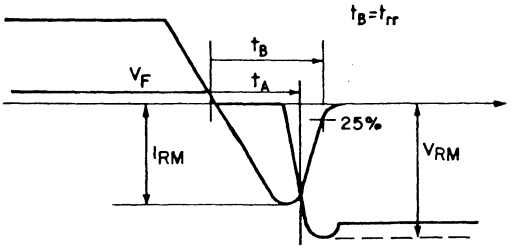
Type C/E diode = D	Quart /Half	Trans /Darl	V_{CEO} (V)	V_{CEX} (V)	$I_{C(sat)}$ (A)	V_C sat	at I_b	t_{off} (μs) typ. induct.	Diode type
SGS80DA020D	Q	D	200	300	80	2.0	1	1.9	SGS60R40
SGS40TA045	Q	T	450	850	40	2.0	8	2.2	none
SGS40TA045D	Q	T	450	850	40	2.0	8	2.2	SGS35R120
SGS50DA045D	Q	D	450	850	50	2.5	2	2.0	SGS35R120
SGS25DB070D	H	D	700	1000	25	3.0	2.5	2.4	SGS35R120
SGS25DB080D	H	D	800	1200	25	3.0	2.5	2.4	SGS45R80
SGS30DB040D	H	D	400	500	30	3.0	2	2.0	SGS45R80
SGS30DB045D	H	D	450	600	30	3.0	2	2.0	SGS45R80
SGS30DA060D	Q	D	600	1000	30	2.5	1.5	3.0	SGS35R120
SGS30DA070D	Q	D	700	1200	30	2.5	1.5	3.0	SGS35R120
SGS50DB040D	H	D	400	500	50	3.5	5.0	3.0	SGS45R80
SGS50DB045D	H	D	450	600	50	3.0	5.0	3.0	SGS45R80
SGS15DB070D	H	D	700	1000	15	3.0	1.5	2.5	SGS35R120
SGS15DB080D	H	D	800	1200	15	3.0	1.5	2.5	SGS35R120

T_{rr} definition

Figures 3 shows two possible definitions for the recovery time, t_A and t_B. In practice t_{rr} is defined as t_B in the figure.

In cases like that shown in Fig. 2, it is important to consider that only t_A is representative of the duration of the power pulse that the recovery of the diode induces in the transistor.

Fig. 3 - t_{rr} measurement methods



SU-1076

T_{rr} characterization

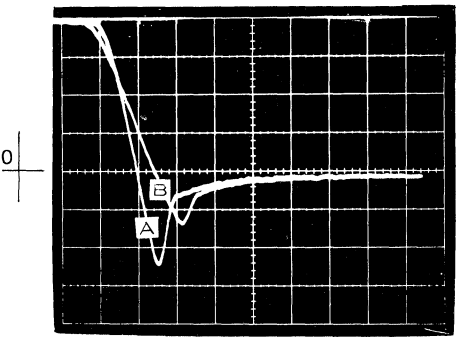
Photographs 1 and 2 show how different test conditions (I_F and di/dt) imply markedly different results for t_{rr}, for the same diode.

The blocking voltage V_{RM} can be disregarded as its influence on t_{rr} is not direct. di/dt is the significant factor and V_{RM} is of importance only to the extent where it modifies di/dt.

Photographs 3 to 5 show the behaviour of the SGS fast recovery rectifier diodes in conditions representing the real environment in which the devices are expected to work. For instance, t_A for SGS45R80 at 40A is 150ns. In a circuit like the one in figure 4, with 40A current in the inductor, the power pulse that the transistor must sustain (I_C peak x V_{CE}) will last for 150ns.

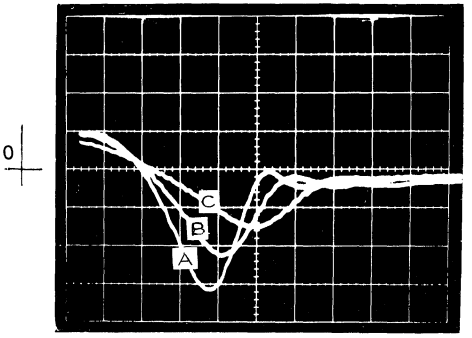
The capacity that SGS transistors have to safely absorb this energy is guaranteed in their FBSOA diagram.

Photo 2 - Recovery times vs. di/dt at 40A for SGS35R120



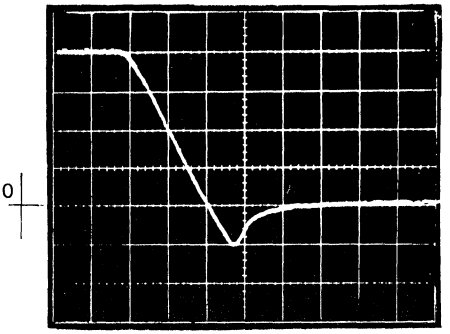
I_F = 40A; A : di/dt = 250A/μs;
B : di/dt = 100A/μs; V_R = 30V;
t = 200ns/div; y = 10A/div

Photo 1 - Recovery times vs. di/dt at 1A for SGS35R120



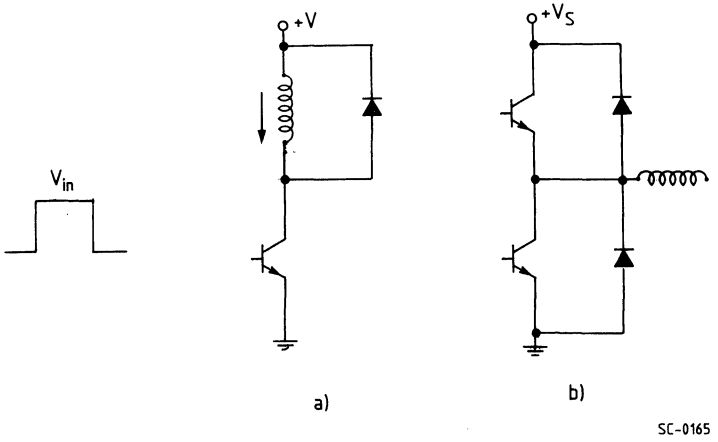
I_F = 1A; A : di/dt = 100A/μs;
B : di/dt = 50A/μs; C : di/dt = 25A/μs;
V_R = 30V; t = 20ns/div; y = 1A/div

Photo 3 - t_{rr} for SGS45R80



I_F = 40A; di/dt = 100μs; V_R = 30V;
t = 200ns/div; y = 20A/div

Fig. 5 - Typical configurations for transistors switching



V_{FP} and t_{FR} definition

The turn-on phase of a diode in a practical situation is shown in Fig. 6.

V_{FP} is defined as the peak transient voltage.

For the same current, the turn-on overvoltage is higher for diodes that can withstand a higher reverse voltage. This can be seen in Fig. 7.

This is mainly related to the thicker epitaxial layer needed to implement a higher reverse voltage rating.

At the turn-on of a diode, a thicker epitaxial layer causes a higher resistance, before the conductivity modulation by the minority carriers takes place.

Fig. 7 - Direct overvoltage vs. di/dt

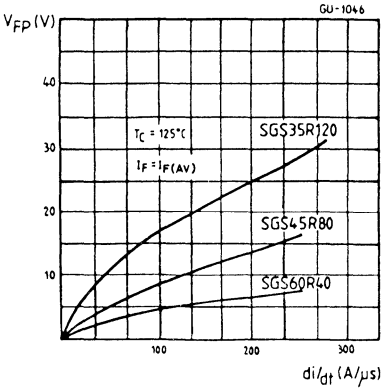
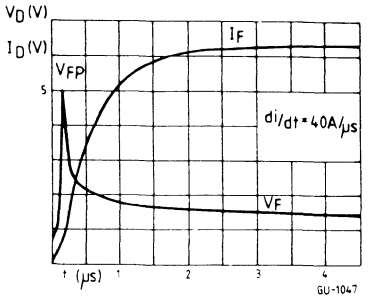


Fig. 6 - Turn-on transient of the diode



T_{FR} Characterization

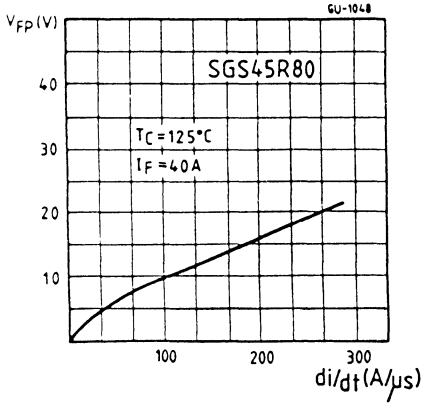
In Fig. 8, the turn-on times, t_{fr}, for the SGS fast recovery rectifiers SGS45R80, SGS35R120 and SGS60R40 are shown as a function of di/dt.

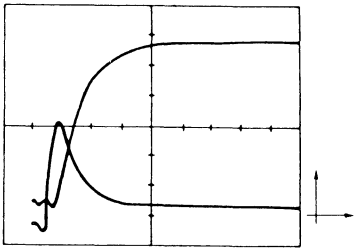
t_{fr} is defined as the time from the instant V_F becomes positive till the time V_{FP} decreases to +2V.

V_{FP} Characterization

Figs. 9 to 11 characterize V_{FP} in all possible di/dt conditions of practical use for the diodes

Fig. 11 - Direct overvoltage vs. di/dt





V = 5V/div; I_F = 25A; di/dt = 200A/μs
t = 100ns/div

Fig. 12a - Final stage of power amplifier

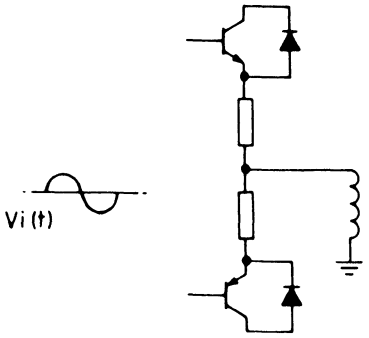


Fig. 12b - Bridge configuration for motor driving

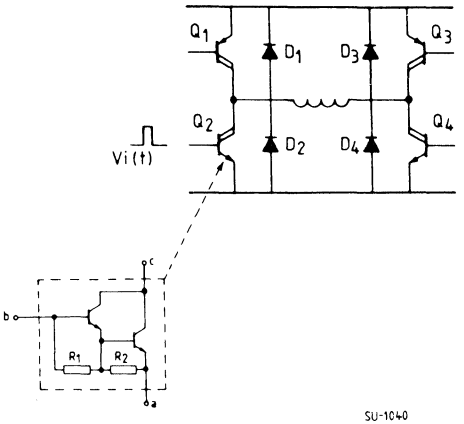
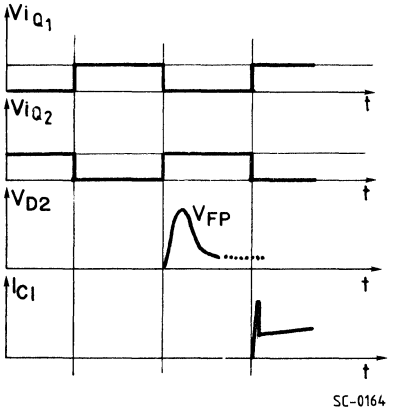


Fig. 12c - Voltage and current waveforms with reference to Fig. 12b



If Q_2 is a darlington, this negative voltage may be enough to reverse bias (through the integrated resistances of the darlington) the final transistor and make it conduct a reverse current I_X.

The current I_X may be a significant proportion of the current that is expected to flow only through D_2, and it can store a significant charge Q_r in the final darlington transistor.

The final darlington transistor base collector junction acts as a slow recovery diode.

As a result, when Q_1 is again turned on, it senses the behaviour of an 'equivalent D_2' with a much longer reverse recovery time. The peak current is higher than expected, creating reliability hazards or possibly the destruction of Q_1.

SGS produces safe operating area diagrams (FBSOA) which specify the maximum V_C/I_C boundary for each device in the range so the

HANDLING AND MOUNTING ICs IN PLASTIC POWER PACKAGES

Integrated circuits mounted in plastic power packages can be damaged, or reliability compromised, by inappropriate handling and mounting techniques. Avoiding these problems is simple if you follow the suggestions in this section.

Advances in power package design have made it possible to replace metal packages with more economical plastic packages in many high power applications. Most of SGS' power driver circuits, for example, are mounted in the innovative MULTIWATT® package, developed originally for high power audio amplifiers. Though the intrinsic reliability of these packages is now excellent the use of inappropriate techniques or unsuitable tools during mechanical handling can affect the long term reliability of the device, or even damage it. With a few simple precautions, careful designers and production engineers can eliminate these risks, saving both time and money.

BENDING AND CUTTING LEADS

The first danger area is bending and cutting the leads. In these processes it is important to avoid straining the package and particularly the area where the leads enter the encapsulating resin. If the package/lead interface is strained the resistance to humidity and thermal stress are compromised, affecting reliability.

There are five basic rules to bear in mind:

- Clamp the leads firmly between the package and the bend/cut point (figure 1).
- Bend the leads at least 3 mm from the package (figure 2a).
- Never bend the leads more than 90° and never bend more than once (figure 2b).
- Never bend the leads laterally (figure 2c).
- Make sure that the bending/cutting tool does not damage the leads.

Fig. 1 - Clamp the leads between the package and bend/cut point.

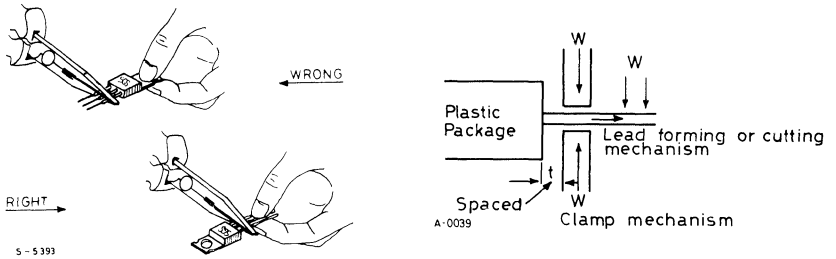


Fig. 2 - Bend the leads at least 3 mm. from the package, never bend leads more than 90° and never attempt to splay the leads out.

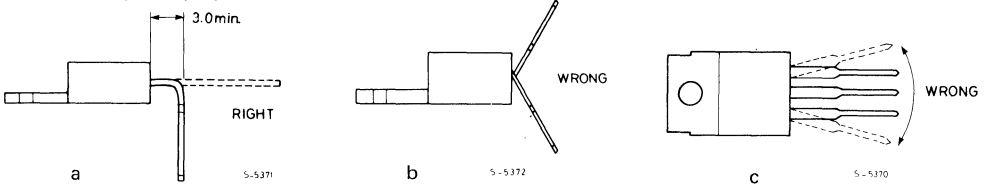


Fig. 5 - MULTIWATT, PENTAWATT and VERSAWATT packages are attached to the heatsink with a single screw or a spring clip.

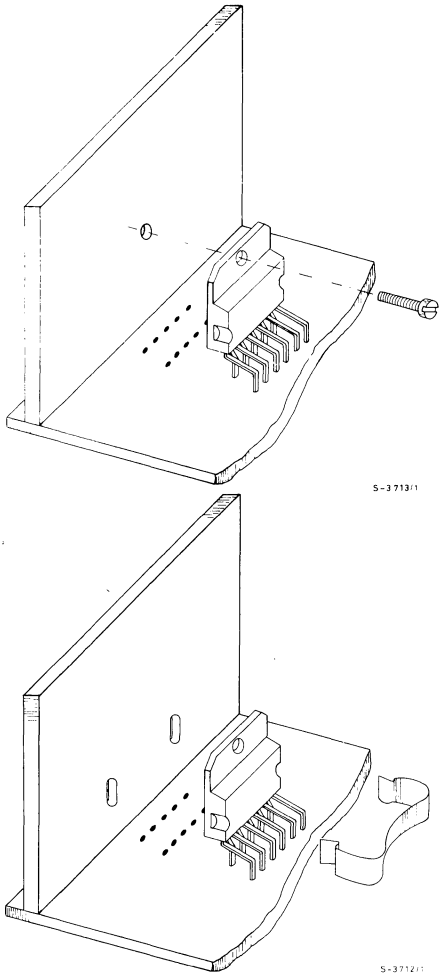
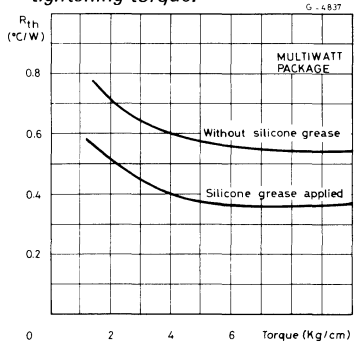
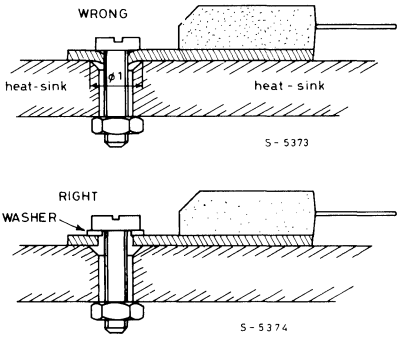


Fig. 6 - Contact thermal resistance depends on tightening torque.



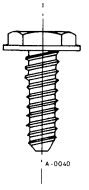
heatsink must be better than 50μm for PENTAWATT and VERSAWATT packages and less than 40μm for MULTIWATT packages.

Fig. 7 - The heatsink tab may be deformed if a washer or a wide-headed screw is not used.



Similar problems may arise if the screwhead is too narrow compared to the hole in the heatsink (figure 7).
The solution here is to use a washer to distribute the pressure over a wider area. An alternative is to use screws of the type shown in figure 8 which have a wide flat head. When self-tapping screws are used it is also important to provide an outlet for the material deformed as the thread is formed. Poor contact will result if this is not done. Another possible hazard arises when the hole in the heatsink is formed with a punch: a circular depression may be formed around the hole, leading to deformation of the tab. This may be cured by using a washer or by modifying the punch.

Fig. 8 - The recommended screw type looks like this.



Serious reliability problems can be encountered if the heatsink and plrinted circuit board are not rigidly connected. Either the heatsink must be rigidly attached to the printed circuit board or both must be securely attached to the chassis. If this is not done the stresses and strains induced by vibration will be applied to the device and in particular to the lead/resin interface. This problem is more likely to arise when large boards and large heatsinks are used or whenever the equipment is subjected to heavy vibrations.

DEVELOPMENTS IN SURFACE MOUNTING PACKAGES FOR POWER INTEGRATED CIRCUITS

Thermal dissipation is recognized as a major problem in Surface Mount Technology. New packages are needed, having good thermal characteristics and meeting the SMT requirements: reduced size, automatic placement, compatibility with the SMT soldering systems.

In this paper, thermal data and measurement methods for the most popular SO and PLCC packages are reviewed; some new solutions for surface mountable medium power (up to 2W) and high power (more than 2W) devices are presented.

INTRODUCTION

A number of problems have been met in introducing the high density, high reliability mass production of SM systems. This can explain the experimental work and the complex characterization activity of both ICs suppliers and users.

As discussed elsewhere /1/, the four main areas of such activity are: standardization, quality, reliability after soldering on PC boards and power dissipation.

Fast progress has been made and more confidence in the SM technology has been achieved in the first three areas. For example, it was demonstrated that the most common conditions used in double wave soldering and vapour phase reflow soldering do not affect the final reliability of SO packaged devices (Fig. 1).

On the contrary, referring to heat dissipation, progress is less fast, even if this point can strongly limit PERFORMANCE and COST of the system, thus losing the two main advantages of the SM technology, to a certain amount.

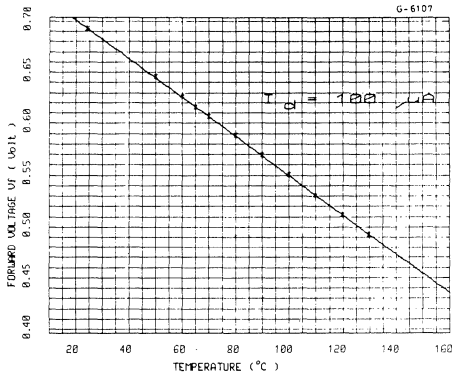
A development activity is needed, to cover the following points:

1) study of the relationship between thermal resistance of the package and board characteristics (density, lay-out, dissipated power). As it will be discussed later, this point cannot be ignored, even at dissipation levels (0.5W or less), typical of the "signal" packages like SO and PLCC packages;
2) study of the thermal properties in pulsed conditions, in order to avoid redundancy and cost increase;
3) development of new power packages with reduced thermal resistance and heat transfer features.

Moreover, a lack of standardized methodology exists when the thermal parameters have to be measured and compared.

In the present paper the above mentioned points are considered. The characterization activity running in SGS is presented, together with experimental data and details on development of new power packages.

Fig. 3 - Calibration curve for P432 sensing diode



The test pattern design ensures that the diode is positioned on the temperature plateau generated when the two transistors are biased in parallel; it is than possible to know the transistor T_j, through the junction temperature of the diode.

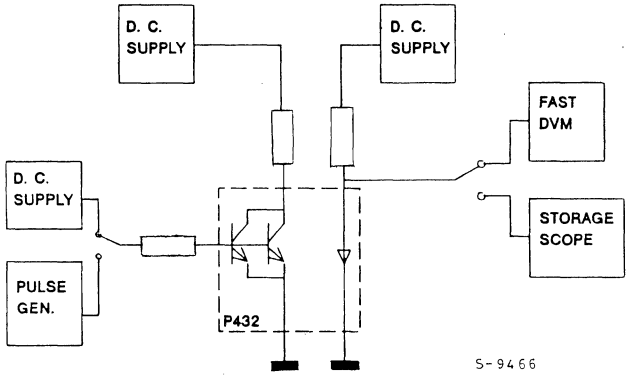
The evaluation die can be cut in different sizes, in order to quantify the effect of the die area on the thermal resistance.

MEASUREMENT TECHNIQUE

The measurement technique is simple /2/ and does not need to switch the power element from the dissipation condition to the sensing condition, thus offering a better accuracy if short pulses are considered. Indeed, the same resolution cannot be achieved with other test patterns, in which the sensing diode is missing (as single power transistors or diode, ICs substrate diode, etc.).

The measurement circuit is shown in fig. 4. A DC power supply or a pulse generator biases the transistors in parallel; a fast voltmeter or a storage oscilloscope records the diode V_f. Resolution better than 50ns is obtained with this circuit.

Fig. 4 - Measurement circuit with P432



UNMOUNTED (FLOATING) SAMPLES

In order to simulate the thermal behaviour of the package in the worst condition (as in a high density, double sided card), samples are connected to 8 thin wires, needed for biasing the two transistors and the sensing diode. Measurement is performed on such devices, suspended horizonthally in a one cubic foot plastic box, to prevent draft.

SAMPLES SOLDERED ON TEST SUB-STRATES

In order to characterize the thermal properties of parts mounted on a substrate, samples are reflow soldered on ceramic and epoxy glass substrates.

For the evaluation of SO packages, the size of the plastic FR4 test board is fixed while the copper pattern lay-out can be changed. Seven different test boards are obtained from the basic configuration of Fig. 5, as summarized in Tab. 1.

Table 1 – CHARACTERISTICS OF THE TEST BOARDS FOR SO PACKAGE EVALUATION

Type	Trace area (x 1000 sq. mils)	Heatsink
SM PCB 1 SGS	136	yes
1B	136	no
1A	21	no
1C	50	no
1D	71	no
1E	93	no
1F	102	no

substrate: FR4
size: 00.9" x 0.8" x 0.056"

Fig. 7 - Alloy 42 SO-8, 14, 16 R_{th} on board

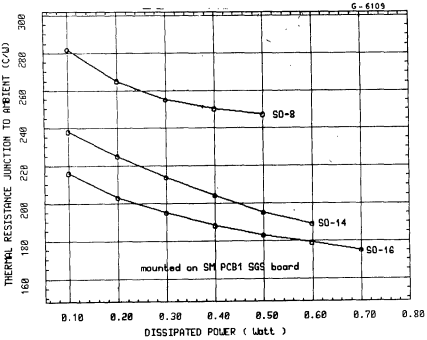


Fig. 8 - R_{th} of copper SO-14 with different substrates

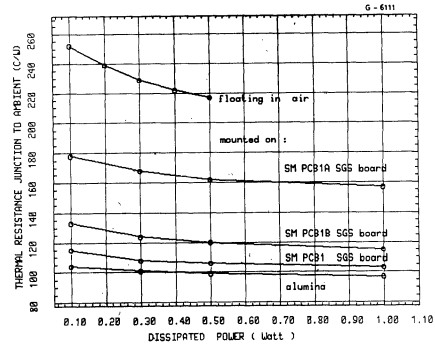


Fig. 9 - R_{th} of copper SO-14 vs. board trace area

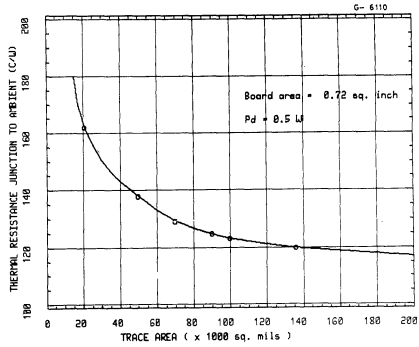
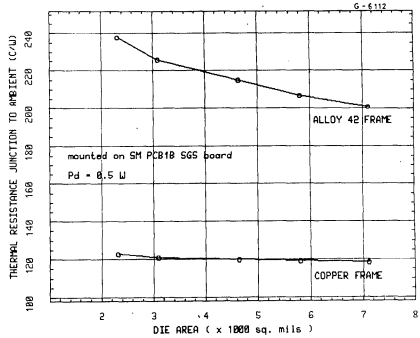


Fig. 10 - R_{th} of on board SO-14 packages vs. die area



THERMAL RESISTANCE OF 68 LEADS PLCC PACKAGE

Data concerning DC and pulsed conditions are obtained for this package /3/, which has Jedec outline and copper crame.

Fig. 11 - R_{th} of "FLOATING" 68 lead PLCC

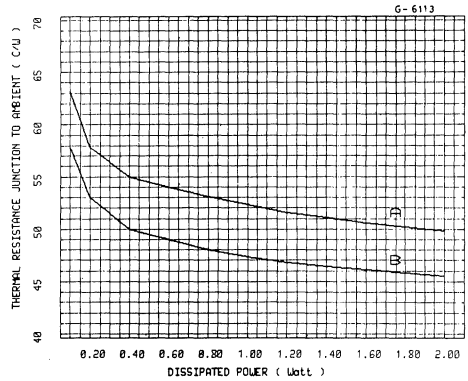


Fig. 12 - R_{th} of 68 lead PLCC mounted on board (Die pad area A = 300x300 sq. mils; B = 425x 425 sq. mils)

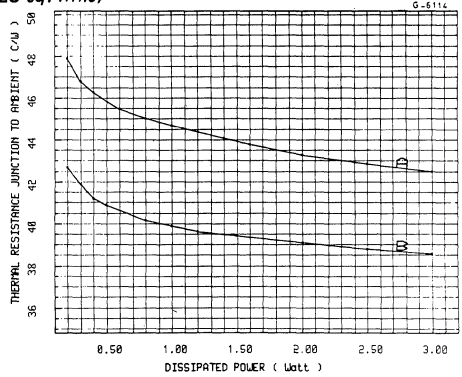
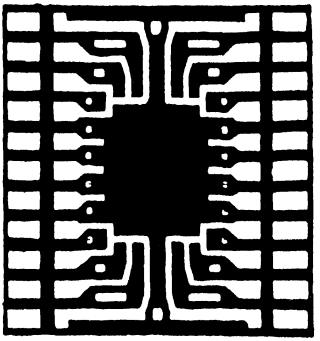
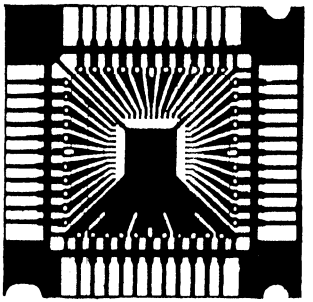


Fig. 16 - Medium power SO-20 frame



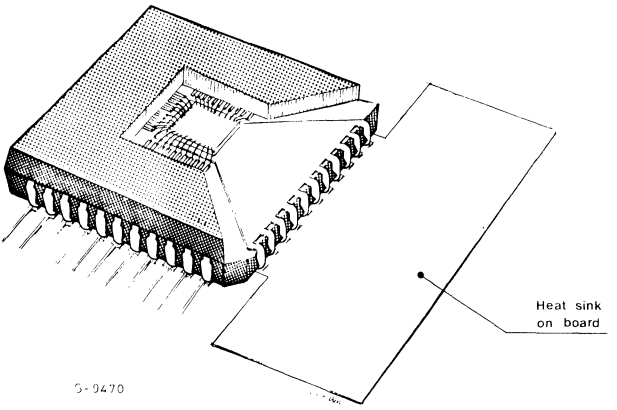
$R_{thj\text{-}amb}$	90° C/W
$R_{thj\text{-}sub}$	14° C/W
Max die size	125x205 mils

Fig. 17 - Medium power 33+11 lead PLCC frame



$R_{thj\text{-}amb}$	55° C/W
$R_{thj\text{-}sub}$	12° C/W
Max. die size	195x195 mils

Fig. 18 - Typical application (2W) of PLCC+11 with external heatsink integrated are the printed board



Additionally, the frame can be modified to incorporate dissipating 'fins' within the plastic body for a further reduction of the junction-to-ambient thermal resistance. In PLCC these fins are obtained easily at the corner of the package by sacrificing signal pins.

Due to availability of a high number of leads mils in PLCC, the reduction of useful pins is not a problem and junction to-ambient thermal resistances can be obtained in the range of 30-40° C/W, for the dissipation of 1.5-2W without any need of external heatsinks.

HIGH POWER SM PACKAGES

For IC's dissipating more than about 2W a different approach is needed.

One obvious solution is simply to form the leads of standard power packages so that they can be

DATASHEETS

AM26LS31

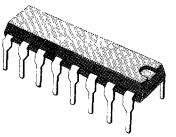
PRELIMINARY DATA

QUAD HIGH SPEED DIFFERENTIAL LINE DRIVER

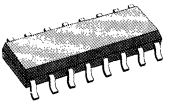
- OUTPUT SKEW -2.0ns TYPICAL
- INPUT TO OUTPUT DELAY -12ns
- OPERATION FROM SINGLE +5V SUPPLY
- OUTPUTS WON'T LOAD LINE WHEN $V_{CC} = 0$
- OUTPUT SHORT-CIRCUIT PROTECTION
- COMPLEMENTARY OUTPUTS
- MEETS THE REQUIREMENTS OF EIA STANDARD RS-422
- HIGH OUTPUT DRIVE CAPABILITY FOR 100Ω TERMINATED TRANSMISSION LINES

The AM26LS31 is a quad differential line driver, designed for digital data transmission over balanced lines. The AM26LS31 meets all the requirements of EIA standard RS-422 and federal standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

The circuit provides an enable and disable function common to all four drivers. The AM26LS31 features 3-state outputs and logical OR-ed complementary enable inputs. The inputs are all LS compatible and are all one unit load.



DIP-16 Plastic (0.25) **and Ceramic**

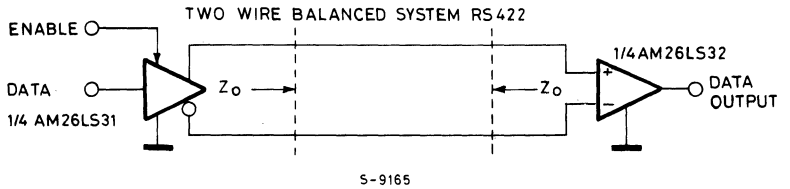


SO-16J

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	7	V
V_i	Input voltage	7	V
V_o	Output voltage	5.5	V
T_{stg}	Storage temperature range	-65 to 150	°C

Fig. 1 - Typical Application



THERMAL DATA

			DIP-16 Ceramic	DIP-16 Plastic	SO-16
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max.	150°C/W	200°C/W	165°C/W

ELECTRICAL CHARACTERISTICS (The following conditions apply unless otherwise specified: T_{amb} = -55°C to 125°C, V_{CC} = 5V ± 10%; T_{amb} = 0 to +70°C, V_{CC} = 5V ± 5%)

Parameter		Test Conditions	Min.	Typ. (Note 1)	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}= Min., I_{OH}= -20mA	2.5	3.2		V
V_{OL}	Output LOW Voltage	V_{CC}= Min., I_{OL}= 20mA		0.32	0.5	V
V_{IH}	Input HIGH Voltage	V_{CC}= Min.	2.0			V
V_{IL}	Input LOW Voltage	V_{CC}= Max.			0.8	V
I_{IL}	Input LOW Current	V_{CC}= Max., V_{IN}= 0.4V		-0.20	-0.36	mA
I_{IH}	Input HIGH Current	V_{CC}= Max., V_{IN}= 2.7V		0.5	20	µA
I_I	Input Reverse Current	V_{CC}= Max., V_{IN}= 7.0V		0.001	0.1	mA
I_O	Off-State (High Impedance) Output Current	V_{CC} = Max., V_O= 2.5V		0.5	20	µA
		V_{CC} = Max., V_O= 0.5V		0.5	-20	µA
V_I	Input Clamp Voltage	V_{CC}= Min., I_{IN}= 18mA		-0.8	-1.5	V
I_{SC}	Output Short Circuit Current	V_{CC}= Max.	-30	-60	-150	mA
I_{CC}	Power Supply Current	V_{CC}= Max., all outputs disabled		60	80	mA
t_{PLH}	Input to Output	V_{CC}= 5.0V, T_{amb}= 25°C, Load = Note 2		12	20	ns
t_{PHL}	Input to Output	V_{CC}= 5.0V, T_{amb}= 25°C, Load = Note 2		12	20	ns
SKEW	Output to Output	V_{CC}= 5.0V, T_{amb}= 25°C, Load = Note 2		2.0	6.0	ns
t_{LZ}	Enable to Output	V_{CC}= 5.0V, T_{amb}= 25°C, C_L = 10pF		23	35	ns
t_{HZ}	Enable to Output	V_{CC}= 5.0V, T_{amb}= 25°C, C_L= 10pF		17	30	ns
t_{ZL}	Enable to Output	V_{CC}= 5.0V, T_{amb}= 25°C, Load = Note 2		35	45	ns
t_{ZH}	Enable to Output	V_{CC}= 5.0V, T_{amb}= 25°C, Load = Note 2		30	40	ns

Notes: 1. A typical values are V_{CC} = 5.0V, T_{amb} = 25°C
2. C_L = 30pF, V_{IN} = 1.3V to V_{OUT} = 1.3V, V_{PULSE} = 0V to +3.0V, See Below.

AM26LS32
AM26LS33

PRELIMINARY DATA

RS422 AND RS423 QUAD DIFFERENTIAL LINE RECEIVERS

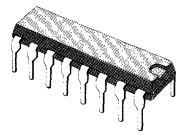
- THE AM26LS32 MEETS ALL THE REQUIREMENTS OF RS-422 AND RS-423
- 6K MINIMUM INPUT IMPEDANCE
- 30mV INPUT HYSTERESIS
- OPERATION FROM SINGLE +5V SUPPLY
- FAIL SAFE INPUT-OUTPUT RELATIONSHIP. OUTPUT ALWAYS HIGH WHEN INPUTS ARE OPEN
- THREE-STATE DRIVE, WITH CHOICE OF COMPLEMENTARY OUTPUT ENABLES, FOR RECEIVING DIRECTLY ONTO A DATA BUS
- PROPAGATION DELAY 17ns TYPICAL

The AM26LS32 is quad line receiver designed to meet the requirements of RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

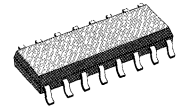
The AM26LS32 features an input sensitivity of 200mV over the input voltage range of ± 7V.

The AM26LS33 features an input sensitivity of 500mV over the input voltage range of ± 15V.

The AM26LS33 provide an enable and disable function common to all four receivers. Both parts feature 3-state outputs with 8mA sink capability and incorporate a fail safe input-output relationship which keeps the outputs high when the inputs are open.



DIP-16 Plastic (0.25) **and Ceramic**



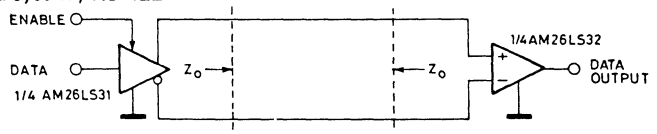
SO-16J

ABSOLUTE MAXIMUM RATINGS

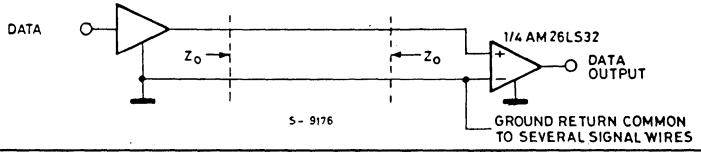
V_s	Supply voltage	7	V
CMR	Common mode range	± 25	V
V_i	Differential input voltage	± 25	V
V_E	Enable voltage	7	V
I_{os}	Output sink current	50	mA
T_{stg}	Storage temperature range	-65 to 150	°C

Fig. 1 - Typical Applications

Two wire balanced system, RS-422



Single wire with common ground imbalanced system, RS-423



ELECTRICAL CHARACTERISTICS (The following conditions apply unless otherwise specified: $T_{amb} = -55°C$ to $125°C$, $V_{CC} = 5V \pm 10\%$; $T_{amb} = 0$ to $70°C$, $V_{CC} = 5V \pm 5\%$)

Parameter		Test Conditions		Min.	Typ. (1)	Max.	Unit
V_{TH}	Differential Input Voltage .	$V_{OUT} = V_{OL}$ or V_{OH}	AM26LS32, $-7V \leq V_{CM} \leq +7V$	-0.2	±0.06	+0.2	V
			AM26LS33, $-15V \leq V_{CM} \leq +15V$	-0.5	±0.12	+0.5	
R_{IN}	Input Resistance	$-15V \leq V_{CM} \leq +15V$ (One input AC ground)		6.0	9.8		KΩ
I_{IN}	Input Current (Under Test)	$V_{IN} = +15V$, Other Input $-15V \leq V_{IN} \leq +15V$				2.3	mA
I_{IN}	Input Current (Under Test)	$V_{IN} = -15V$, Other input $-15V \leq V_{IN} \leq +15V$				-2.8	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., $\Delta V_{IN} = +1.0V$	COM'L	2.7	3.4		V
		$V_{\overline{ENABLE}} = 0.8V$, $I_{OH} = -440\mu A$	MIL	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min., $\Delta V_{IN} = -1.0V$	$I_{OL} = 4.0mA$			0.4	V
		$V_{ENABLE} = 0.8V$	$I_{OL} = 8.0mA$			0.45	
V_{IL}	Enable LOW Voltage					0.8	V
V_{IH}	Enable HIGH Voltage			2.0			V
V_I	Enable Clamp Voltage	V_{CC} = Min., $I_{IN} = -18mA$				-1.5	V
I_O	Off-State (High Impedance) Output Current	V_{CC} = Max.	$V_O = 2.4V$			20	μA
			$V_O = 0.4V$			-20	
I_{IL}	Enable LOW Current	$V_{IN} = 0.4V$			-0.2	-0.36	mA
I_{IH}	Enable HIGH Current	$V_{IN} = 2.7V$			0.5	20	μA
I_I	Enable Input High Current	$V_{IN} = 5.5V$			1	100	μA
I_{SC}	Output Short Circuit Curr.	$V_O = 0V$, V_{CC} = Max., $\Delta V_{IN} = +1.0V$		-15	-50	-85	mA
I_{CC}	Power Supply Current	V_{CC} = Max., All V_{IN} = GND, Output Disabled			52	70	mA
V_{HYST}	Input Hysteresis	$T_{amb} = 25°C$, $V_{CC} = 5.0V$, $V_{CM} = 0V$			30		mV
t_{PLH}	Input to Output	$T_{amb} = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below			17	25	ns
t_{PHL}	Input to Output	$T_{amb} = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below			17	25	ns
t_{LZ}	Enable to Output	$T_{amb} = 25°C$, $V_{CC} = 5.0V$, $C_L = 5pF$, see test cond. below			20	30	ns
t_{HZ}	Enable to Output	$T_{amb} = 25°C$, $V_{CC} = 5.0V$, $C_L = 5pF$, see test cond. below			15	22	ns
t_{ZL}	Enable to Output .	$T_{amb} = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below			15	22	ns
t_{ZH}	Enable to Output	$T_{amb} = 25°C$, $V_{CC} = 5.0V$, $C_L = 15pF$, see test cond. below			15	22	ns

(1) All typical values are $V_{CC} = 5.0V$, $T_{amb} = 25°C$

AM6012
AM6012A

PRELIMINARY DATA

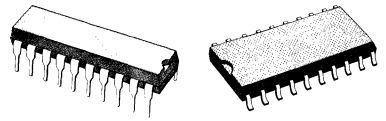
12-BIT HIGH SPEED MULTIPLYING D/A CONVERTERS

The AM6012 is an industry standard monolithic 12-bit digital-to analog converter. Complementary current output and high speed multiplying capability make the AM6012 useful in a wide range of applications such as video displays, process control circuitry and fast A/D converters. The 6012 is the first D/A to achieve 12-bit differential linearity without the use of thin film resistors or active trimming. The 6012's unique circuit design insures monotonicity without the precision trimming associated with most other 12-bit DAC architectures.

The AM6012 is packaged in a 20-pin plastic DIP and is SO-20L for surface mounting. Although tested and specified at ±15V, the AM6012 works well over a wide range of power supply voltages. Performance is essentially independent of supply voltage over the range of +5 volts, −12 volts to ±18 volts. The AM6012 series guarantees full 12-bit monotonicity for all grades and differential nonlinearity as high as 0.012% (13 bits) for the A grades and 0.025% (12 bits) for the standard grades over the entire temperature range.

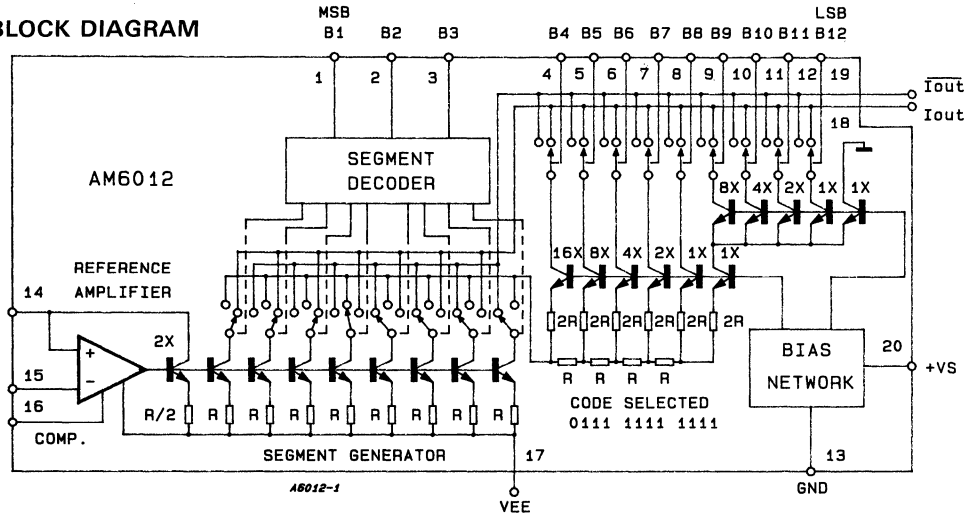
Guaranteed monotonicity and low cost make the AM6012 an ideal choice for high volume applications requiring fine local resolution. Typical applications include printer graphics and video displays. These applications need a minimum of 12 bits of resolution, although conformance to an ideal straight line from zero to full scale is less important.

- ALL GRADES 12-BIT MONOTONIC OVER TEMPERATURE
- DIFFERENTAL NONLINEARITY TO ±0.012% (13 BITS) MAX OVER TEMPERATURE (A GRADES)
- 250ns TYPICAL SETTLING TIME
- FULL SCALE CURRENT 4mA
- HIGH SPEED MULTIPLYING CAPABILITY
- TTL/CMOS/ECL/HTL COMPATIBLE
- HIGH OUTPUT COMPLIANCE: −5V TO +10V
- COMPLEMENTARY CURRENT OUTPUTS
- LOW POWER CONSUMPTION: 230mW



DIP-20 Plastic (X3P2) **SO-20L**

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

These specifications apply for $V_S = +15V$, $V_{EE} = -15V$, $I_{REF} = 1.0mA$, over the operating temperature range unless otherwise specified

Param.	Description	Test Conditions	AM6012A			AM6012			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
	Resolution		12	12	12	12	12	12	Bits
	Monotonicity		12	12	12	12	12	12	Bits
D.N.L.	Differential Nonlinearity	Deviation from ideal step size	–	–	±.012	–	–	±.025	%FS
			13	–	–	12	–	–	Bits
N.L.	Nonlinearity	Deviation from ideal straight line	–	–	±.05	–	–	±0.05	%FS
I_{FS}	Full Scale Current	$V_{REF} = 10.000V$ $R_{14} = R_{15} = 10.000k\Omega$ $T_A = 25°C$	3.967	3.999	4.031	3.935	3.999	4.063	mA
TCI_{FS}	Full Scale Temp.Co.		–	±5	±20	–	±10	±40	ppm°C
			–	±.0005	±.002		±.001	±.004	%FS°C
V_{OC}	Output Voltage Compliance	D.N.L. Specification guaranteed over compliance range $R_{OUT} > 10$ megohme typ.	−5	–	+10	−5	–	+10	V
I_{FSS}	Full Scale Symmetry	I_{FS}-I_{FS}	–	±0.2	±1.0	–	±0.4	±2.0	μA
I_{ZS}	Zero Scale Current		–	–	0.10	–	–	0.10	μA
I_S	Setting Time	To ±1/2 LSB, all bits ON or OFF, $T_A = 25°C$	–	250	500	–	250	500	nSec
t_{PLH} t_{PHL}	Propagation Delay - all bits	50% to 50%	–	25	50	–	25	50	nSec
C_{OUT}	Output Capacitance		–	20	–	–	20	–	pF
V_{IL}	Logic Input Levels — Logic "0"		–	–	0.8	–	–	0.8	V
V_{IH}	Logic Input Levels — Logic "1"		2.0	–	–	2.0	–	–	
I_{IN}	Logic Input Current	$V_{IN} = -5$ to $+18V$	–	–	40	–	–	40	μA
V_{IS}	Logic Input Swing	$V_{EE} = -15V$	−5	–	+18	−5	–	+18	V
I_{REF}	Reference Current Range		0.2	1.0	1.1	0.2	1.0	1.1	mA
I_{15}	Reference Bias Current		0	−0.5	−2.0	0	−0.5	−2.0	μA

APPLICATION INFORMATION

FUNCTIONAL DESCRIPTION

The segmented design of the AM6012, shown in the block diagram, insures that there are no significant differential nonlinearities in the transfer characteristic. The eight major carries of the most significant bits are not subject to the gross differential nonlinearities that can occasionally occur in an R-2R type DAC. This advantage is due to the fundamentally different way that the current is handled in an AM6012. In a conventional R-2R type DAC, when the input code is increemented past a major carry, a current representing the new code is substituted for the sum of all the less significant bit currents that were previously on. To avoid any nonlinearities, the two total currents must be extremely well matched. In the case of the MSB major carry in a 12-bit DAC, the match must be better than one part in 2048 to maintain monotonicity. However, in the AM6012, a new current is never substituted for the sum of several smaller ones, but redirected through alternate channels and incremented one step at a time.

For example, consider the MSB carry in an AM6012. In the initial state of 011111111111 as shown in the block diagram, the switches in the segment generator are set in such a way that currents I_0, I_1 and I_2 are steered directly into the noninverting output I_{OUT}. In addition, a portion of I_3 is directed through the 9-bit DAC that is controlled by the 9 least significant bits into I_{OUT}. With the 9LSBs set to "I", all of the I_3 current is directed to I_{OUT} except for the 1/512 that goes to ground through the right-most transistor in the 9-bit DAC. After the input word is changed to 100000000000, the segment decoder switch for I_3 will be all the way to the right, the switch for I_4 will be in the middle, and all the switches in the 9-bit DAC will be to the left. I_{OUT} will be composed of I_0, I_1, I_2 and I_3. None of I_4 will be directed into I_{OUT} until a higher code is reached. In other words, I_3 is now steered directly to I_{OUT} instead of being divided by a factor of 511/512 in the 9-bit DAC. Since no major current substitution occurs, there is less chance of a large nonlinearity at this transition than in a comparable R-2R DAC.

RELATIVE ACCURACY VS. DIFFERENTIAL NONLINEARITY

SGS defines relative accuracy as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn between the lowest code output voltage and the highest code output voltage) for any bit combination. Relative accuracy is often referred to as nonlinearity. The DAC transfer function shown in Figure 1 has a bow that results in a maximum relative accuracy error of 3LSB. This must be distinguished from a differential linearity error. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a ILSB change in digital input code.

For example, for a 4mA full scale output, a change of ILSB in digital input code should result in a 0.98μA change in the analog output current (ILSB = 4mA x 1/4096 = 0.98μA). If in actual use, however, a ILSB change in the input code results ina change of only 0.24μA (1/4LSB) in output current, the differential linearity error would be 0.74μA or 3/4LSB.

The AM6012 has very good differential linearity in spite of the porr relative accuracy. Conversely, the DAC of Figure 1 has very good relative accuracy but poor differential linearity. The anomaly in the middle of the transfer function is the result of a positive differential linearity error followed by a negative differential linearity error greater than 1LSB. A negative output step for an increase in digital input code is referred to as nonmonotonic behavior. In general, if a DAC has a differential linearity error specification greater than 1LSB, it may be nonmonotonic at one or more of the major carries. In most case the worst differential linearity error will occur at the MSB transition point.

As noted in the functional description, the 6012's unique design minimizes differential linearity errors at the transition points of the 3MSBs. This results in a tight specification on maximum differential nonlinearity over temperature. Differential linearity is verified on all AM6012s with 100% final testing. In many converter applications, uniform step size (or minimum differential linearity error) is more important than conformance to an ideal straight line. Twelve-bit onverters are usually needed for high resolution rather than high linearity as evidenced by the fact that few transducers are more linear than 0.1%. This is also true in video graphics, where the human eye has difficulty discerning nonlinearity of less than 5%. The AM6012 is especially well suited for these applications since it has inherently low differential linearity error.

APPLICATION INFORMATION (Continued)

Fastest operation can be octained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference, and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1μF capacitors at the supply pins provide full transient protection.

REFERENCE AMPLIFIER SETUP

The AM6012 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full range output current is a linear function of the reference current and is given by:

$$I_{RF} = \frac{4095}{4096} \times 4 \times (I_{REF}) = 3.999\ I_{REF},$$

where $I_{REF} = I_{14}$

In positive reference applications, an external positive reference voltage forces current through R14 into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15. Reference current flows from ground through R14 into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R15 (nominally equal to R14) is used to cancel bias current errors. (Figure 3).

Bipolar references may be accommodated by offsetting V_{REF} or pin 15. The negative common-mode range of the reference amplifier is given by: $V_{CM-} = V-$ plus ($I_{REF} \times 3k\Omega$) plus 1.8V. The positive common-mode range is V+ less 1.23V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R14 should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R14, or by using a potentiometer for R14.

MULTIPLYING OPERATION

The AM6012 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 1mA to 1μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 1.0mA.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V−. The value of this capacitor depends on the impedance presented to pin 14. For R14 values of 1.0, 2.5 and 5 OkΩ; minimum values of C_C are 5, 12 and 25 pF. Larger values of R14 require proportionately increased values of C_C for proper phase margin (See Figure 4 and 5).

For fastest response to a pulse, low values of R14 enabling small C_C values should be used. If pin 14 is driven be a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall compensated which will decrease overall bandwidth and slew rate. For R14 = 1kΩ and C_C = 5pF, the reference amplifier slews at 4mA/ms enabling a transition from $I_{REF} = 0$ to I_{REF} = 1mA in 250ns.

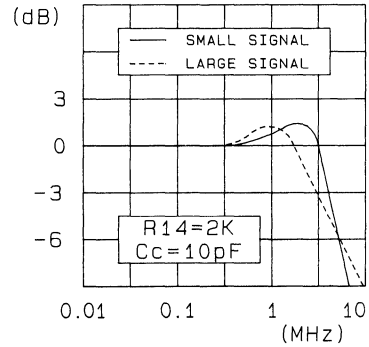
Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff ($I_{REF} = 0$) condition. Full scale transition (0 to 1mA) occurs in 62.5ns when the equivalent impedance at pin 14 is 800Ω and $C_C = 0$. This yields a reference slew rate of 8mA/μs which is relatively independent of R_{IN} and V_{IN} values.

Fig. 4 - Minimum size compensation capacitor (I_{FS}=4mA, I_{REF}=1.0mA)

$R_{14(EQ)}$(KΩ)	C_C(pF)
10	50
5	25
2	10
1	5
5	0

Note: A 0.01 μF capacitor is recommended for fixed reference operation.

Fig. 5 - Reference Amplifier Frequency response



A6012-11: : DI

Fig. 6 - Interfacing Circuits

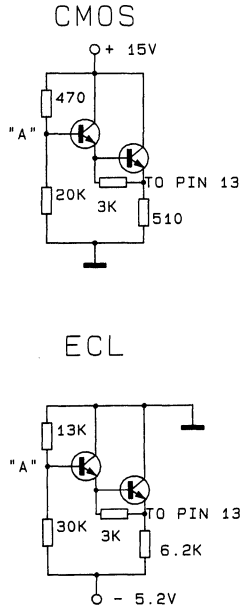
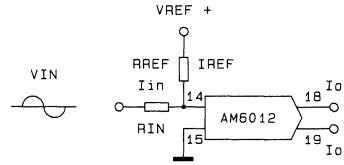
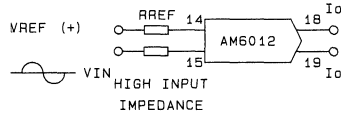


Fig. 7 - Accomodating Bipolar Reference



IREF > PEAK NEGATIVE SWING OF Iin



VREF (+) MUST BE ABOVE PEAK POSITIVE SWING OF VIN

Fig. 9 - Basic Negative Reference Operation

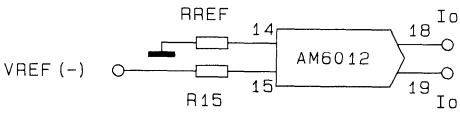


Fig. 10 - Recommended Full-scale Adjustment Circuit

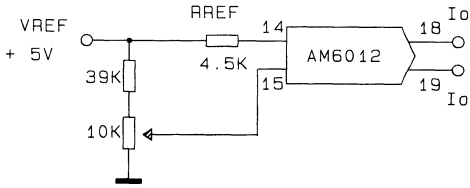


Fig. 11 - CRT Display Driver

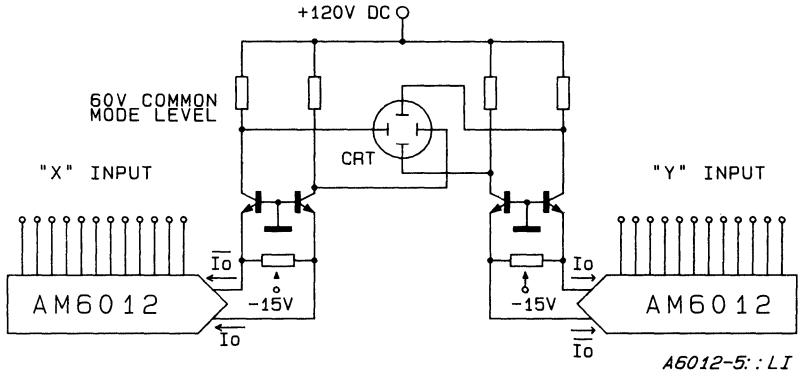
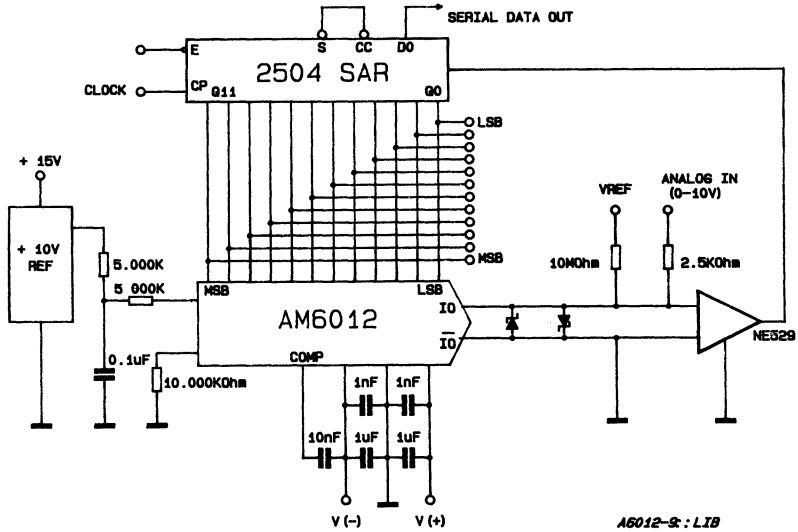


Fig. 12 - 12-BIT High-Speed A/D Converter



DAC0808
DAC0807
DAC0806

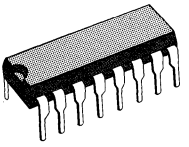
PRELIMINARY DATA

8-BIT D/A CONVERTERS

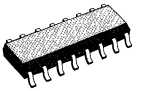
- RELATIVE ACCURACY: ±0.19% ERROR MAXIMUM (DAC0808)
- FULL SCALE CURRENT MATCH: ±1 LSB TYP
- 7 AND 6-BIT ACCURACY AVAILABLE(DAC0807, DAC0806)
- FAST SETTING TIME: 150 ns TYP
- NONINVERTING DIGITAL INPUTS ARE TTL AND CMOS COMPATIBLE
- HIGH SPEED MULTIPLYING INPUT SLEW RATE: 8 mA/μs
- POWER SUPPLY VOLTAGE RANGE: ±4.5V to ±18V
- LOW POWER CONSUMPTION: 33 mW @ ±5V

The DAC0808 series is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 $I_{REF}/256$. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 series are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC0808 will interface directly with popular TTL, or CMOS logic levels, and is a direct replacement for the MC1508/MC1408.

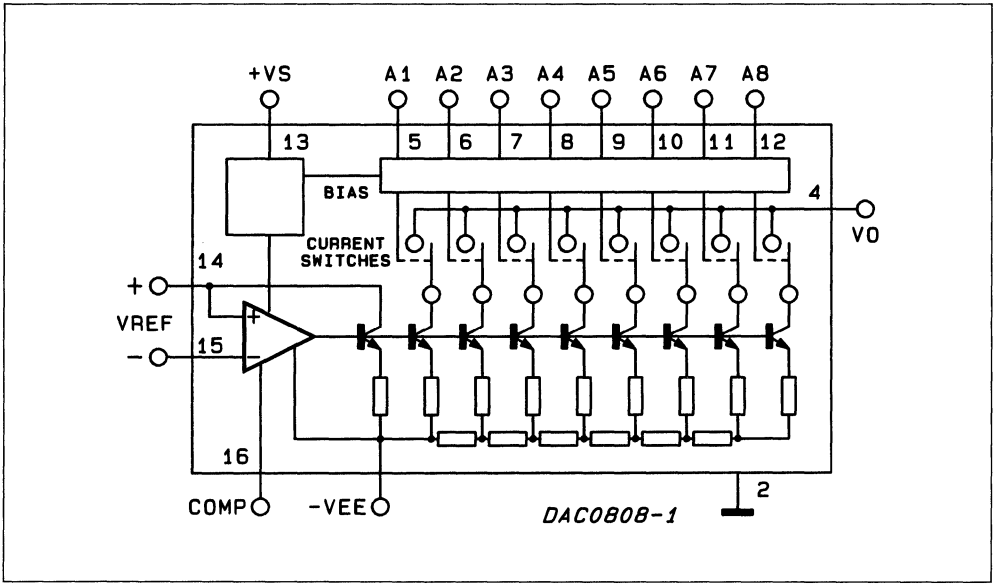


DIP-16 Plastic (0.25) **and Ceramic**



SO-16

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

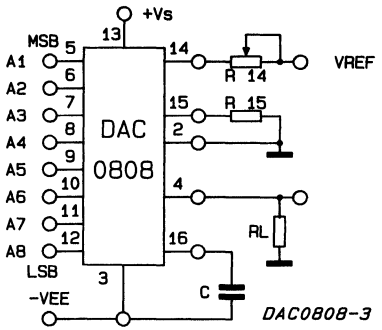
($V_S = 5V$, $V_{EE} = -15V$, $V_{REF}/R14 = 2$ mA, $T_A = T_{MIN}$ to T_{MAX} and all digital inputs at high logic level unless otherwise noted.)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
E_r	Relative Accuracy (Error Relative to Full Scale I_O)	*(Figure 10)*				%
	DAC0808L				±0.19	%
	DAC0807LC/D1 (Note 1)				±0.39	%
	DAC0806LC/D1 (Note 1)				±0.78	%
	Settling Time to Within 1/2 LSB (Includes t_{PLH})	$T_A = 25°C$ (Note 2) *(Figure 11)*		150		ns
t_{PLH} t_{PHL}	Propagation Delay Time	$T_A = 25°C$ *(Figure 11)*		30	100	ns
TCI_O	Output Full Scale Current Drift			±20		ppm/°C
MSB	Digital Input Logic Levels	*(Figure 9)*				
V_{IH}	High Level, Logic "1"		2			V_{DC}
V_{IL}	Low Level, Logic "0"				0.8	V_{DC}
MSB	Digital Input Current	*(Figure 9)*				
	High Level	$V_{IH} = 5V$		0	0.040	mA
	Low Level	$V_{IL} = 0.8V$		−0.003	−0.8	mA
I_{15}	Reference Input Bias Current	*(Figure 3)*		−1	−3	μA
	Output Current Range	*(Figure 9)*				
		$V_{EE} = -5V$	0	2.0	2.1	mA
		$V_{EE} = -15V$, $T_A = 25°C$	0	2.0	4.2	mA
I_O	Output Current	$V_{REF} = 2.000V$. $R14 = 1000\Omega$				
		(Figure 9)	1.9	1.99	2.1	mA
	Output Current, All Bits Low	*(Figure 9)*		0	4	μA
	Output Voltage Compliance	$E_r \leq 0.19\%$, $T_A = 25°C$				
	$V_{EE} = -5V$				−0.55, +0.4	V
	V_{EE} Below −10V				−5.0 , +0.4	V
SRI_{REF}	Reference Current Siew Rate	*(Figure 14)*	4	8		mA/μs
	Output Current Power Supply Sensitivity	$-5V \leq V_{EE} \leq -16.5V$		0.05	2.7	μA/V
Power Supply Current (All Bits Low)		*(Figure 9)*				
I_S				2.3	22	mA
I_{EE}				−4.3	−13	
Power Supply Voltage Range		$T_A = 25°C$ *(Figure 9)*				
V_S			4.5	5.0	5.5	V
V_{EE}			−4.5	−15	−16.5	
	Power Dissipation					
	All Bits Low	$V_S = 5V$. $V_{EE} = -5V$		33	170	mW
		$V_S = 5V$. $V_{EE} = -15V$		106	305	mW
	All Bits High	$V_S = 15V$. $V_{EE} = -5V$		90		mW
		$V_S = 15V$. $V_{EE} = -15V$		160		mW

Note 1: All current switches are tested to guarantee at least 50% of rated current.
Note 2: All bits switched.
Note 3: Range control is not required.

Test Circuits

FIGURE 9. Notation Definitions



The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left(\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right)$$

where $K \cong \frac{V_{REF}}{R14}$

and A_N = "1" if A_N is at high level
A_N = "0" if A_N is at low level

FIGURE 10. Relative Accuracy

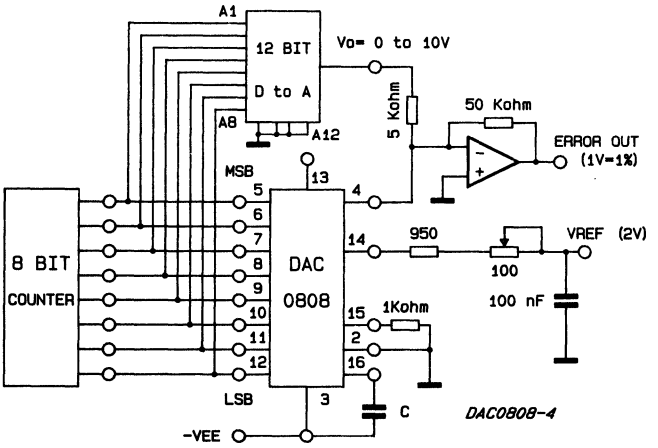
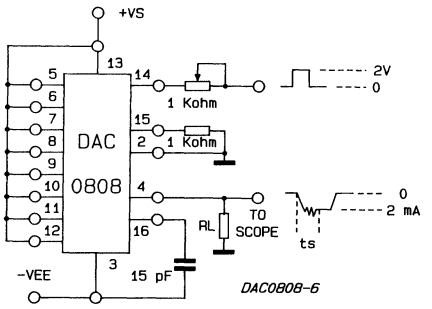


FIGURE 14. Reference Current Slew Rate Measurement



APPLICATION INFORMATION

CIRCUIT DESCRIPTION

The DAC0808 consists of a reference current amplifier, an R-2R ladder, and eight high-speed current switches. For many applications, only a reference resistor and reference voltage need be added.
The switches are noninverting in operation, therefore a high state on the input turns on the specified output current component. The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching and provides a low impedance termination of equal voltage for all legs of the ladder. The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the switches. Nota that there is always a remainder current which is equal to the last significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992 mA for a 2.0 mA reference amplifier current if the NPN current source pair is perfectly matched.

REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I_{14}, must always flow into pin 14, regardless of the set-up method or reference voltage polarity.

Connections for a positive voltage are shown in *Figure 12.* The reference voltage source supplies the full current I_{14}. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1, 2.5 and 5 kΩ, minimum capacitor values are 15,37 and 75 pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in *Figure 13.* A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 3V above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a DC reference voltage is used, capacitive by pass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to 5V through another resistor and bypassing the junction of the 2 resistors with 0.1 μF to ground. For reference voltages greater than 5V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

PROGRAMMABLE GAIN AMPLIFIER OR DIGITAL ATTEPUATOR

When used in the multiplying mode can be applied as a digital attenuator. See Figure 15. One advantage of this technique is that if $R_S = 50$ ohms, no compensation capacitor is needed. The small and large signal band are now identical and are shown in Figure 8C.

The best frequency response is obtained by not allowing I_{14} to reach zero. However, the high impedance node, pin 16, is clamped to prevent saturation and insure fast recovery when the current through R14 goes to zero. R_S can be set for a ± 1.0 mA variation in relation to I_{14}. I_{14} can never be negative. The output current is always unipolar. The quiescent dc output current level changes with the digital word which makes accoupling necessary.

CURRENT TO VOLTAGE CONVERSION

Voltage output of a larger magnitude are obtainable with the circuit of fig. 16 which uses an external operational amplifier as a current to voltage converter. This configuration automatically keeps the output of the DAC0808 ground potential and the operational amplifier can generate a positive voltage limited only by its positive supply voltage. Frequency response and setting time are primarily determined by the characteristics of the operational amplifier. In addition, the operational amplifier must be compensated for unity gain, and in some cases over compensation may be desirable.
Note that this configuration results in a positive output voltage only, the magnitude of which is dependent on the digital input. The LM301 can be used in a feedforwerd mode resulting in a full scale setting time on the order of 2.0 μs.

COMBINED OUTPUT AMPLIFIER AND VOLTAGE REFERENCE

For many of its applications the DAC0808 requires a reference voltage and an operational amplifier. Normally the operational amplifier is used as a current to voltage converter and its output need only go positive. With the popular LM723 voltage regulator both of these functions are provided in a single package with the added bonus of up to 150 mA output current. See Figure 17. The reference voltage is developed with respect to the negative voltage and appears as a common-mode signal to the reference amplifier in the D-to-A converter. This allows use of its amplifier as a classic current-to-voltage converter with the non-inverting input grounded.
Since ± 15V and $+5.0$V are normally available in a combination digital-to-analog system, only the -5.0 V need be developed. A resistor divider is sufficiently accurate since the allowable range on pin 5 is from -2.0 to -8.0 volts. The 5.0 kilohm pulldown resistor on the amplifier output is necessary for fast negative transitions.
Full scale output may be increasing R_O and raising the $+15$V supply voltage to 35 V maximum. The resistor divider should be altered to comply with the maximum limit of 40 volts across the LM723 C_O may be decreased to maintain the same R_OC_O product if maximum speed is desired.

PROGRAMMABLE POWER SUPPLY

The circuit of figure 17 can be used as a digitally programmed power supply by the addition of thumbwheel switches and a BCD-to-binary converter. The output voltage can be scaled in several ways, including 0 to $+25.5$ volts in 0.1 $-$volt increments, ± 10 mV.

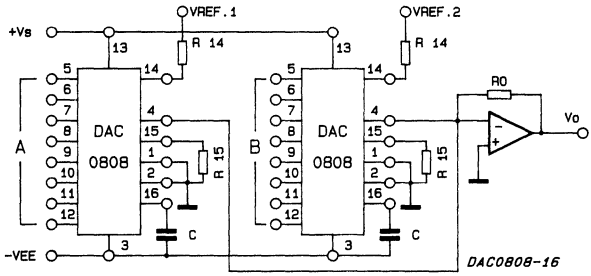
PANEL METER READOUT

The DAC0808 can be used to read out the status of BCD or binary registers or counters a digital control system. The current output can be used to drive directly an analog panel meter. External meter shunts may be necessary if a meter of less than 20 mA full scale is used. Full scale calibration can be done by adjusting R14 or V_{ref} (see fig. 18).

CHARACTER GENERATOR

In a character generation system fig. 19 one DAC0808 circuit uses a fixed reference voltage and its digital input defines the starting point for a stroke. The second converter circuit has a ramp input for the reference and its digital input defines the slope of the stroke. Note that this approach does not result in a 16-bit D-to-A converter (see Accuracy Section).

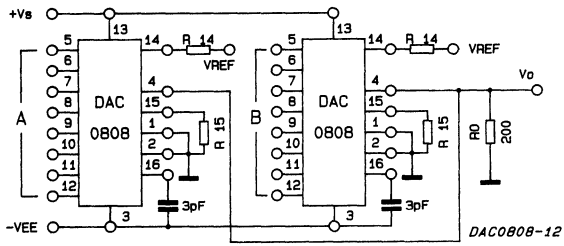
FIGURE 19. Digital summing and character generation



$$V_O = (I_{O1} + I_{O2})\, R_O$$

$$V_O = \left[\frac{V_{ref1}}{R14_1}\{A\} + \frac{V_{ref2}}{R14_2}\{B\}\right] R_O$$

FIGURE 20. Analog product of two digital words (High Speed Operation)



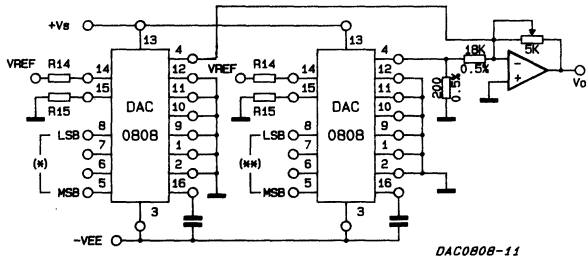
$$V_O = -I_{O1}\, R_O = \frac{V_{ref}}{R14_1}\{A\}\, R_O$$

$$I_{O2} = \frac{\{B\}\,|V_O|}{R14_2} = \frac{\{B\}}{R14_2}\left[R_O\left(\frac{V_{ref}}{R14_1}\right)\{A\}\right]$$

Since $R_O = R14_2$ and $K = \dfrac{V_{ref}}{R14_1}$

$$\boxed{I_{O2} = K\,\{A\}\,\{B\}}$$ K can be an analog variable

FIGURE 21. Two-digit BCD conversion



(*) MOST SIGNIFICANT BCD WORD
(**) LEAST SIGNIFICANT BCD WORD

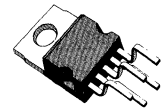
L149

4A LINEAR DRIVER

- HIGH OUTPUT CURRENT (4A PEAK)
- HIGH CURRENT GAIN (10.000 TYP.)
- OPERATION UP TO ± 20V
- THERMAL PROTECTION
- SHORT CIRCUIT PROTECTION
- OPERATION WITHIN SOA
- HIGH SLEW-RATE (30V/μs)

The L149 is a general purpose power booster in Pentawatt® package consisting of a quasi-complementary darlington output stage with the associated biasing system and inhibit facility.

The device is particularly suited for use with an operational amplifier inside a closed loop configuration to increase output current.



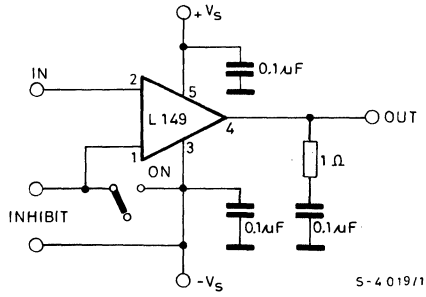
Pentawatt®

ORDERING NUMBER: L149V

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 20	V
V_i	Input voltage	V_s	
$V_5 - V_4$	Upper power transistor V_{CE}	40	V
$V_4 - V_3$	Lower power transistor V_{CE}	40	V
I_o	DC output current	3	A
I_o	Peak output current (internally limited)	4	A
V_{INH}	Input inhibit voltage	$-V_s$ +5	V
		$-V_s$ -1.5	V
P_{tot}	Power dissipation at T_{case}= 75°C	25	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

TEST CIRCUIT



THERMAL DATA

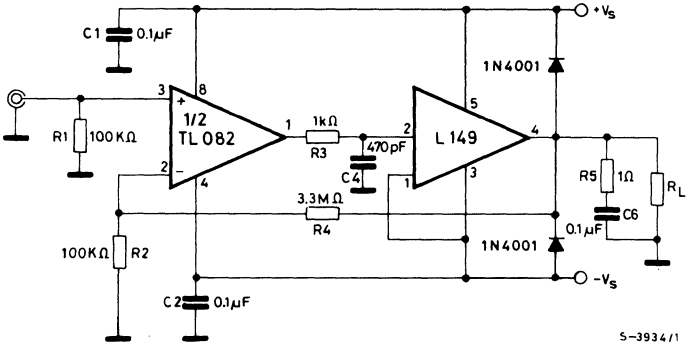
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS ($T_j = 25°C$, $V_s = \pm 16V$)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage				± 20	V
I_d	Quiescent drain current	$V_s = \pm 16V$		30		mA
I_{in}	Input current	$V_s = \pm 16V$ $V_i = 0V$		200	400	μA
h_{FE}	DC current gain	$V_s = \pm 16V$ $I_o = 3A$	6000	10000		—
G_v	Voltage gain	$V_s = \pm 16V$ $I_o = 1.5A$		1		—
V_{CEsat}	Saturation voltage (for each transistor)	$I_o = 3A$			3.5	V
V_{os}	Input offset voltage	$V_s = \pm 16V$			0.3	V
V_{INH}	Inhibit input voltage (pins 1-3)	ON condition			± 0.3	V
		OFF condition	± 1.8			
R_{INH}	Inhibit input resistance			2.0		KΩ
SR	Slew rate			30		V/μs
B	Power bandwidth	$V_o = \pm 10V$, d = 1%, $R_L = 8\Omega$		200		KHz

APPLICATION INFORMATION

Fig. 1 - High slew-rate power operational amplifier (SR = 13V/μs)

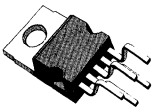


L165

3A POWER OPERATIONAL AMPLIFIER

- OUTPUT CURRENT UP TO 3A
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGES
- SOA PROTECTION
- THERMAL PROTECTION
- ± 18V SUPPLY

The L165 is a monolithic integrated circuit in Pentawatt® package, intended for use as power operational amplifier in a wide range of applications, including servo amplifiers and power supplies. The high gain and high output power capability provide superior performance wherever an operational amplifier/power booster combination is required.



Pentawatt®

ORDERING NUMBER: L165V

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 18	V
$V_5 - V_4$	Upper power transistor V_{CE}	36	V
$V_4 - V_3$	Lower power transistor V_{CE}	36	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 15	V
I_o	Peak output current (internally limited)	3.5	A
P_{tot}	Power dissipation at $T_{case} = 90°C$	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

APPLICATION CIRCUITS

Fig. 1 - Gain > 10

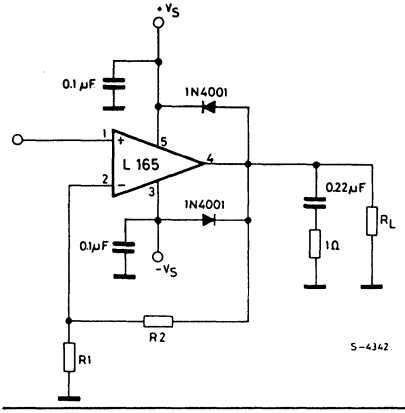
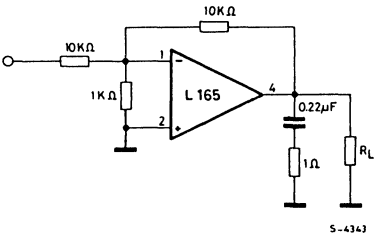


Fig. 2 - Unity gain configuration

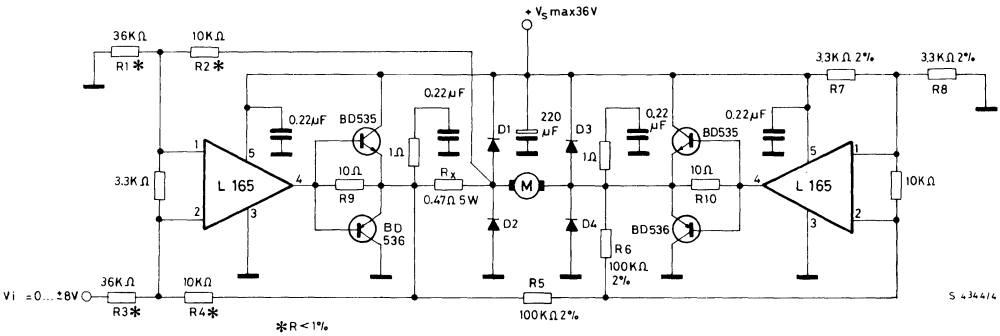


ELECTRICAL CHARACTERISTICS (V_s = ± 15V, T_j = 25°C unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			± 6		±18	V
I_d	Quiescent drain current	V_s = ± 18V			40	60	mA
I_b	Input bias current				0.2	1	μA
V_{os}	Input offset voltage				± 2	±10	mV
I_{os}	Input offset current				±20	±200	nA
SR	Slew-Rate	G_v= 10			8		V/μs
		G_v= 1 (°)			6		
V_o	Output voltage swing	f = 1 kHz	I_p = 0.3A		27		V_{pp}
			I_p = 3A		24		
		f = 10 kHz	I_p = 0.3A		27		V_{pp}
			I_p = 3A		23		
R_i	Input resistance (pin 1)	f = 1 KHz		100	500		KΩ
G_v	Voltage gain (open loop)				80		dB
e_N	Input noise voltage	B = 10 to 10 000 Hz			2		μV
i_N	Input noise current				100		pA
CMR	Common mode rejection	$R_g \leqslant$ 10 KΩ G_v= 30 dB			70		dB
SVR	Supply voltage rejection	R_g= 22 kΩ V_{ripple}= 0.5 V_{rms} f_{ripple}= 100 Hz	G_v = 10		60		dB
			G_v = 100		40		dB
η	Efficiency	f = 1 kHz R_L= 4Ω	I_p = 1.6A; P_o = 5W		70		%
			I_p = 3A; P_o = 18W		60		%
T_{sd}	Thermal shut-down case temperature	P_{tot}= 12W			110		°C
		P_{tot}= 6W			130		

(°) Circuit of fig. 2

Fig. 10 - Motor current control circuit with external power transistors ($I_{motor} > 3.5A$)

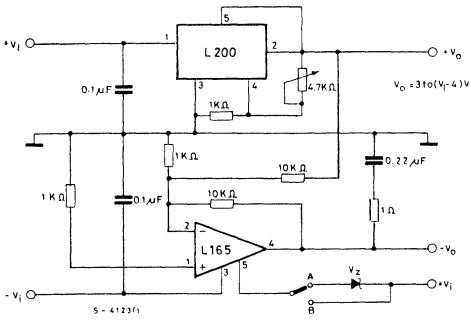


D1 to D4 : $\begin{cases} V_F \leqslant 1.2V @ I = 4A \\ trr \leqslant 500\ ns \end{cases}$

Note: The input voltage level is compatible with L291 (5-BIT D/A converter).

The transfer function is : $\frac{I_M}{V_i} = \frac{R4}{Rx\ R3}$

Fig. 11 - High current tracking regulator

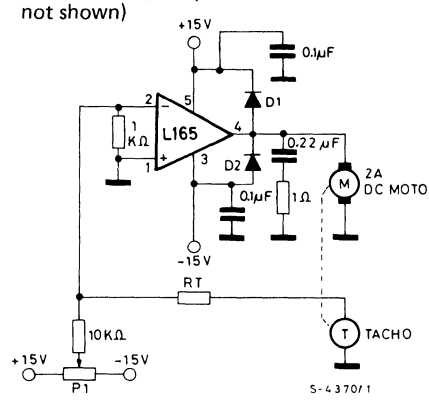


A: for $\pm 18 \leqslant V_i \leqslant \pm 32$

Note – V_z must be chosen in order to verify $2\,V_i - V_z \leqslant 36V$

B: for $V_i \leqslant \pm 18V$

Fig. 12 - Bidirectional speed control of DC motor (Compensation networks not shown)



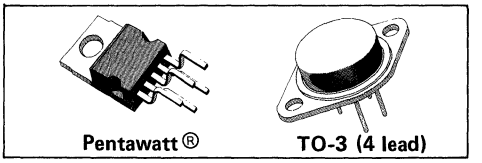
D1, D2 : $\begin{cases} V_F \leqslant 1.2V @ I = 2A \\ trr \leqslant 500\ ns \end{cases}$

L200

ADJUSTABLE VOLTAGE AND CURRENT REGULATOR

- ADJUSTABLE OUTPUT CURRENT UP TO 2A (GUARANTEED UP TO T_j = 150°C)
- ADJUSTABLE OUTPUT VOLTAGE DOWN TO 2.85V
- INPUT OVERVOLTAGE PROTECTION (UP TO 60V, 10ms)
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR S.O.A. PROTECTION
- THERMAL OVERLOAD PROTECTION
- LOW BIAS CURRENT ON REGULATION PIN
- LOW STANDBY CURRENT DRAIN

The L200 is a monolithic integrated circuit for voltage and current programmable regulation. It is available in Pentawatt® package or 4-lead TO-3 metal case. Current limiting, power limiting, thermal shutdown and input overvoltage protection (up to 60V) make the L200 virtually blow-out proof. The L200 can be used to replace fixed voltage regulators when high output voltage precision is required and eliminates the need to stock a range of fixed voltage regulators.



Pentawatt® TO-3 (4 lead)

ABSOLUTE MAXIMUM RATINGS

V_i	DC input voltage	40 V
V_i	Peak input voltage (10 ms)	60 V
ΔV_{i-o}	Dropout voltage	32 V
I_o	Output current	internally limited
P_{tot}	Power dissipation	internally limited
T_{stg}	Storage temperature	-55 to 150 °C
T_{op}	Operating junction temperature for L200C	-25 to 150 °C
	for L200	-55 to 150 °C

APPLICATION CIRCUITS

Fig. 1 - Programmable voltage regulator with current limiting

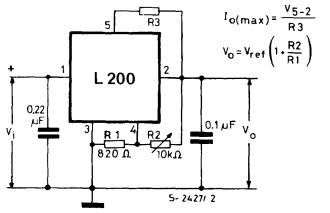
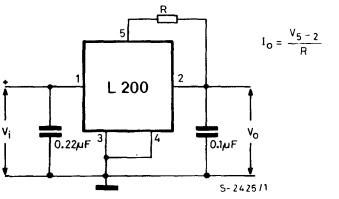
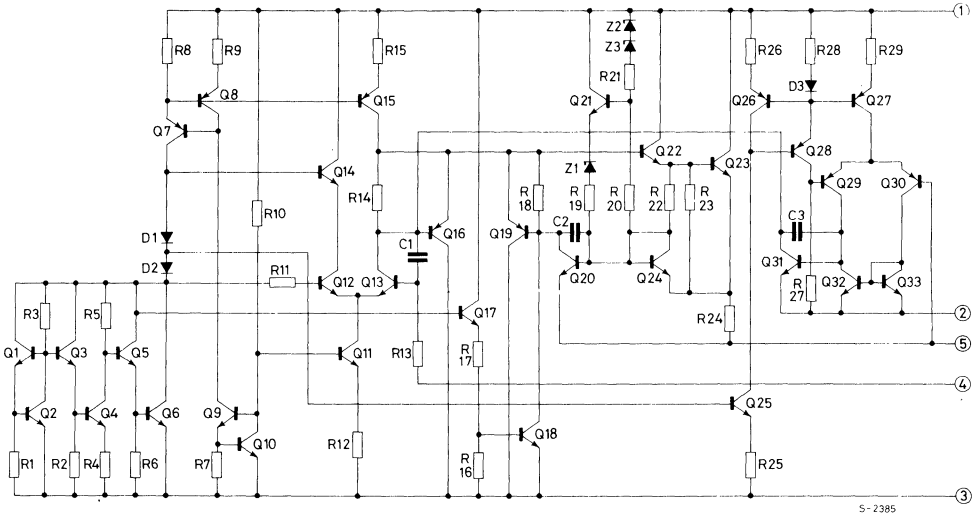


Fig. 2 - Programmable current regulator



SCHEMATIC DIAGRAM



THERMAL DATA

			TO-3	Pentawatt®
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4 °C/W	3 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	35 °C/W	50 °C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
VOLTAGE REGULATION LOOP						
I_d	Quiescent drain current (pin 3)	V_i = 20V		4.2	9.2	mA
e_N	Output noise voltage	$V_o = V_{ref}$ I_o = 10 mA B = 1 MHz		80		μV
V_o	Output voltage range	I_o = 10 mA	2.85		36	V
$\frac{\Delta V_o}{V_o}$	Voltage load regulation (note 1)	ΔI_o = 2A ΔI_o = 1.5A		0.15 0.1	1 0.9	% %
$\frac{\Delta V_i}{\Delta V_o}$	Line regulation	V_o = 5V V_i = 8 to 18V	48	60		dB
SVR	Supply voltage rejection	V_o = 5V I_o = 500 mA ΔV_i = 10 V_{pp} f = 100 Hz (note 2)	48	60		dB

Fig. 3 - Typical safe operating area protection

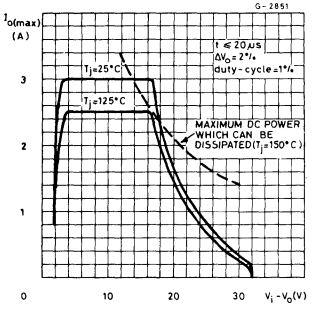


Fig. 4 - Quiescent current vs. supply voltage

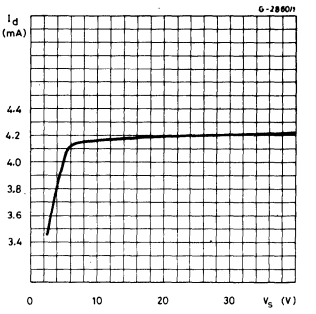


Fig. 5 - Quiescent current vs. junction temperature

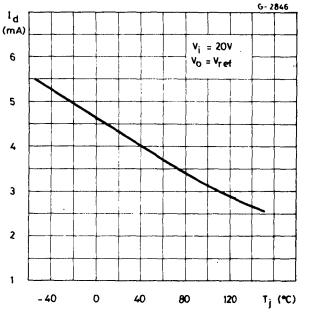


Fig. 6 - Quiescent current vs. output current

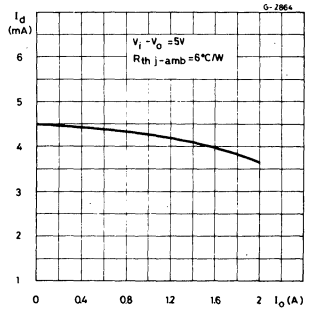


Fig. 7 - Output noise voltage vs. output voltage

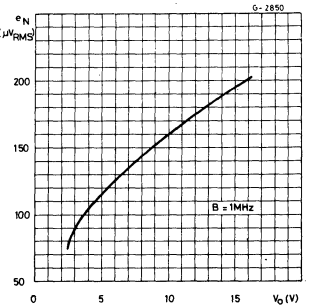


Fig. 8 - Output noise voltage vs. frequency

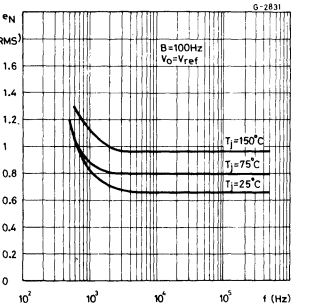


Fig. 9 - Reference voltage vs. junction temperature

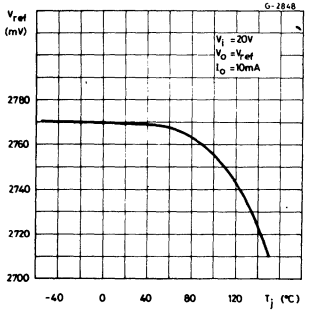


Fig. 10 - Voltage load regulation vs. junction temperature

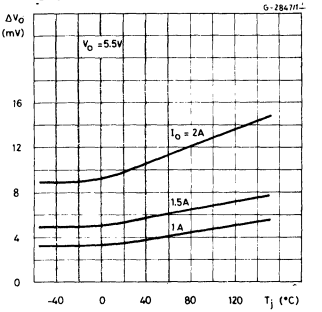
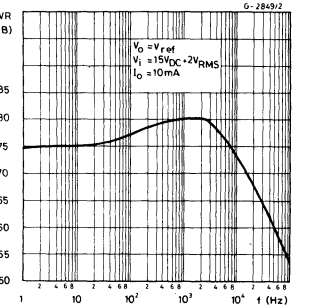


Fig. 11 - Supply voltage rejection vs. frequency



APPLICATION CIRCUITS

Fig. 19 - Programmable voltage regulator

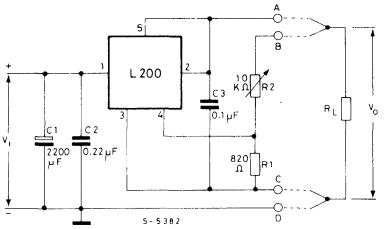


Fig. 20 - P.C. board and components layout of fig. 19. (1 : 1 scale)

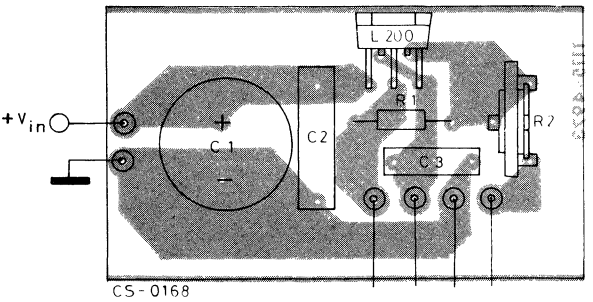


Fig. 21 - High current voltage regulator with short circuit protection

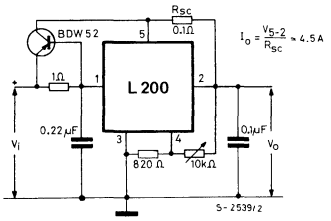


Fig. 22 - Digitally selected regulator with inhibit

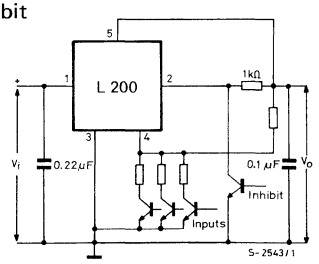
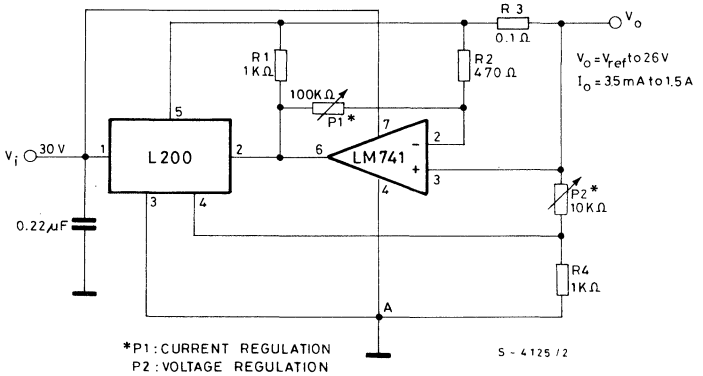


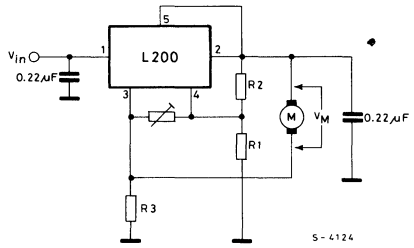
Fig. 23 - Programmable voltage and current regulator



Note: Connecting point A to a negative voltage (for example -3V/10 mA) it is possible to extend the output voltage range down to 0V and to obtain the current limiting down to this level (output short-circuit condition).

APPLICATION CIRCUITS (continued)

Fig. 28 - 30W Motor speed control



$$R_3 = \frac{R_1}{R_2} \cdot R_M$$

$$V_M = V_{ref} \cdot (1 + \frac{R_2}{R_1})$$

Fig. 29 - Low turn on

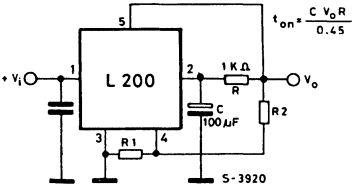
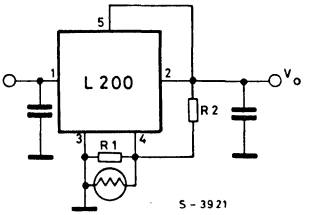


Fig. 30 - Light controller



L272
L272M

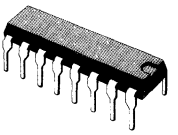
PRELIMINARY DATA

DUAL POWER OPERATIONAL AMPLIFIERS

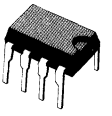
- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN

The L272 and L272M are monolithic integrated circuits in powerdip and minidip packages intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies, compact disc, VCR, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.



Powerdip 8 + 8



Minidip Plastic

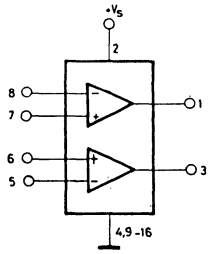
ORDERING NUMBERS:

L272 L272M

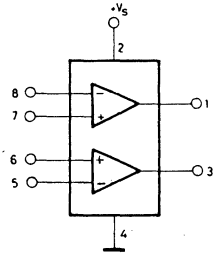
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	28	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at T_{amb} = 80°C (**L272**), T_{amb} = 50°C (**L272M**)	1	W
	T_{case} = 75°C (**L272**)	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

BLOCK DIAGRAM



L272



L272M

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			4		28	V
I_s	Quiescent drain current	$V_o = \frac{V_s}{2}$	V_s = 24V		8	12	mA
			V_s = 12V		7.5	11	mA
I_b	Input bias current				0.3	2.5	μA
V_{os}	Input offset voltage				15	60	mV
I_{os}	Input offset current				50	250	mA
SR	Slew rate				1		V/μs
B	Gain-bandwidth product				350		KHz
R_I	Input resistance			500			KΩ
G_v	O.L. voltage gain	f = 100Hz		60	70		dB
		f = 1KHz			50		dB
e_N	Input noise voltage	B = 20KHz			10		μV
I_N	Input noise current	B = 20KHz			200		pA
CRR	Common Mode rejection	f = 1KHz		60	75		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ±12V V_s = ± 6V	54	70 62 56		dB dB dB
V_o	Output voltage swing		I_p = 0.1A I_p = 0.5A	21	23 22.5		V V
C_s	Channel separation	f = 1KHz; R_L = 10Ω; G_v = 30dB	V_s = 24V V_s = ± 6V		60 60		dB dB
d	Distortion	f = 1KHz V_s = 24V	G_v = 30dB R_L = ∞		0.5		%
T_{sd}	Thermal shutdown junction temperature				145		°C

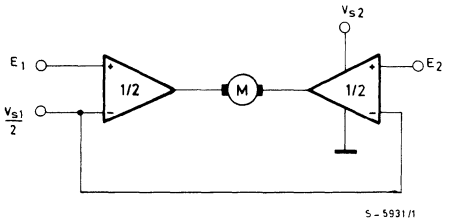
APPLICATION SUGGESTION

NOTE

In order to avoid possible instability occurring into final stage the usual suggestions for the linear power stages are useful, as for instance:

- layout accuracy;
- A 100nF capacitor corrected between supply pins and ground;
- boucherot cell (0.1 to 0.2μF + 1Ω series) between outputs and ground or across the load.

Fig. 9 - Bidirectional DC motor control with μP compatible inputs



V_{S1} = logic supply voltage

Must be $V_{S2} > V_{S1}$

E1, E2 = logic inputs

Fig. 10 - Servocontrol for compact-disc

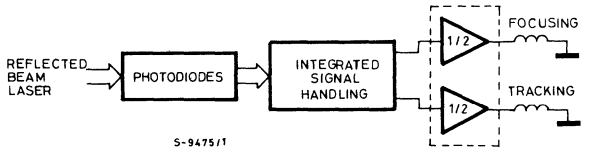
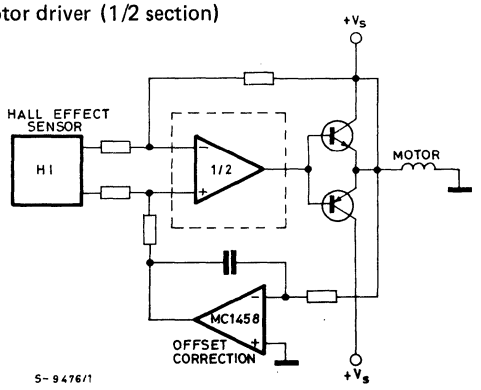


Fig. 11 - Compact-disc motor driver (1/2 section)

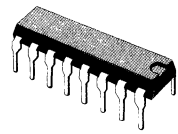


TACHOMETER CONVERTER

The L290, a monolithic LSI circuit a 16-lead dual in-line plastic package, is intended for use with the L291 and L292 which together from a complete **3-chip DC motor positioning system** for applications such as carriage/daisy-wheel position control in typewriters.

The L290/1/2 system can be directly controlled by a microprocessor. The L290 integrates the following functions:

- tacho voltage generator (F/V converter)
- reference voltage generator
- position pulse generator



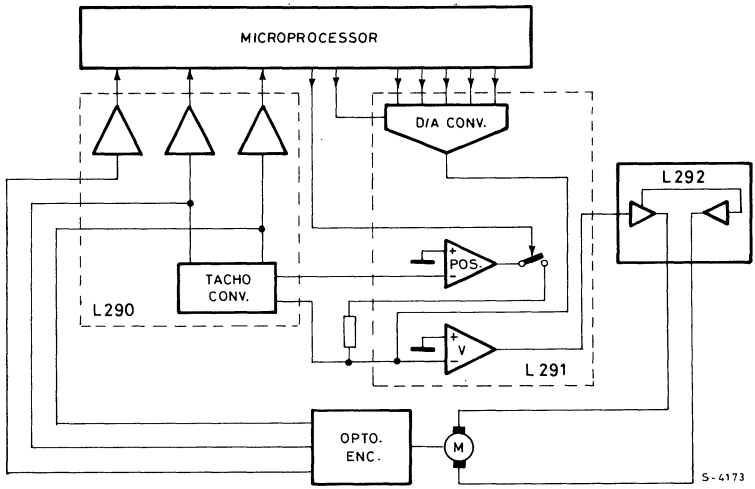
DIP-16 Plastic
(0.4)

ORDERING NUMBER: L290B

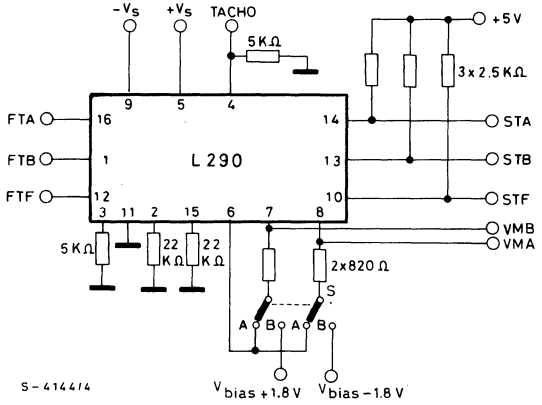
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 15	V
V_i (FTA, FTB, FTF)	Input signals	± 7	V
P_{tot}	Total power dissipation T_{amb} = 70°C	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to +150	°C

SYSTEM BLOCK DIAGRAM



TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

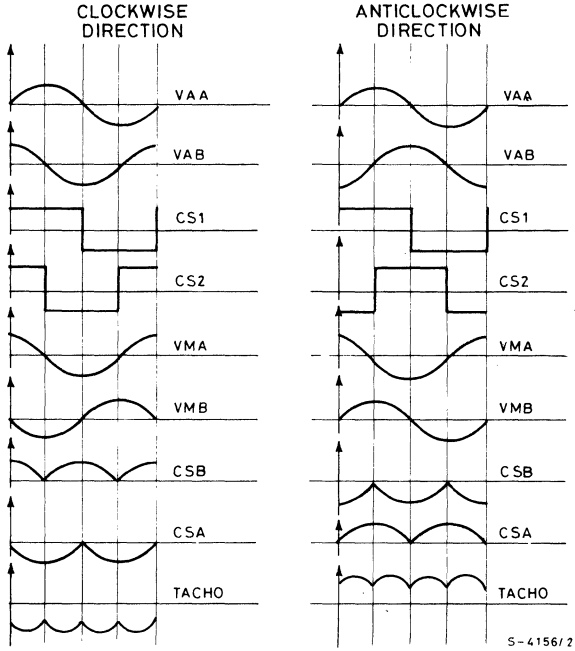
ELECTRICAL CHARACTERISTICS (Refer to the test circuit, S in (A), $V_s = \pm 12V$, $T_{amb} = 25°C$ unless otherwise specified)

Parameters		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		±10		±15	V
I_d	Quiescent drain current	$V_s = \pm 15V$		13	20	mA

INPUT AMPLIFIERS (A_1 and A_2)

FTA, FTB	Input signal from encoder (pin 1, 16)	$f_{max} = 20$ KHz	±0.4		±0.6	V_p
V_{os}	Output offset voltage (pin 2, 15)	FTA = FTB = 0V			± 55	mV
I_b	Input bias current (pin 1, 16)			0.15		μA
G_v	Voltage gain	f = 10 KHz FTA=FTB=$\pm 0.6V_p$	22	23	24	dB
V_o	Output voltage swing (pin 2, 15)	FTA= FTB= $\pm$ 1 V_p	±9.5			V

WAVEFORMS (Neglecting threshold voltage level of the comparators)



SYSTEM DESCRIPTION : refer to the L292 data sheet

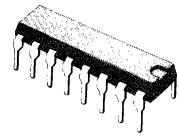
5 BIT - D/A CONVERTER AND POSITION AMPLIFIER

The L291, a monolithic LSI circuit in a 16-lead dual in-line plastic package, is intended for use with the L290 and L292 to form a complete **3 chip DC motor positioning system for** applications such as carriage/daisy-wheel position control in typewriters.

The L290/291/292 system can be directly controlled by a microprocessor.

The L291 integrates the following functions:

- 5 bit D/A converter (½ LSB max linearity error);
- error amplifier;
- position amplifier.



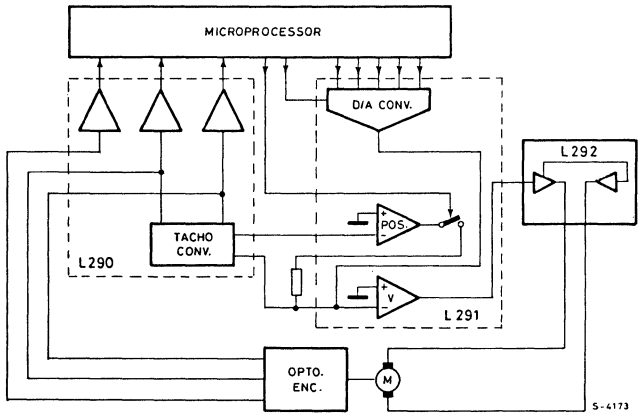
DIP-16 Plastic
(0.4)

ORDERING NUMBER: L291B

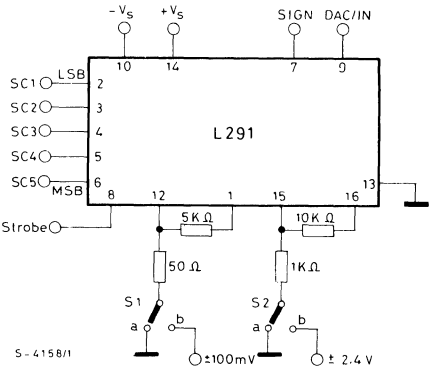
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 15	V
P_{tot}	Total power dissipation T_{amb} = 70°C	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

SYSTEM BLOCK DIAGRAM



TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the circuit, S1 and S2 in (a), $V_s = \pm 12V$, $T_{amb} = 25°C$, unless otherwise specified)

Parameters		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		± 10		± 15	V
I_d	Quiescent drain current			6.5	10	mA

POSITION AMPLIFIER

V_{strobe}	Enable voltage level	V_L (S in (a)) *	0		0.8	V
		V_H (S in (b)) *	2.4		$+V_s$	V
V_{os}	Output offset voltage (pin 16)	$V_{strobe} = V_L$; $G_v = 20$ dB			± 50	mV
I_b	Input bias current (pin 15)	$V_{strobe} = V_L$			0.3	μA
V_o	Output voltage swing (pin 16)	$V_{strobe} = V_L$; S2 in(b); $V_s = \pm 10.8V$	± 9			V
V_R	Residual output voltage (pin 16)	$V_{strobe} = V_H$			± 20	mV

* See block diagram and the note for Position Amplifier.

D/A Converter

The L291 contains a 5-bit D/A converter accepting a binary code and generating a bipolar output current, the polarity of which depends on the SIGN input. The amplitude of the output current is a multiple of a reference current I_{ref}.
The maximum output current is

$$I_{FS} = \pm \frac{31}{16} I_{ref}$$

The following table shows the value of I_o for different input codes. Note that the input bits are active low.

DIGITAL INPUT WORD						Output Current I_o
SIGN	SC5 MSB	SC4	SC3	SC2	SC1 LSB	
L	L	L	L	L	L	$-\frac{31}{16} I_{ref}$
L	H	H	H	H	L	$-\frac{1}{16} I_{ref}$
X	H	H	H	H	H	0
H	H	H	H	H	L	$+\frac{1}{16} I_{ref}$
H	L	L	L	L	L	$+\frac{31}{16} I_{ref}$

X = indifferent
L = low
H = high

This D/A converter has a maximum linearity error equal to ± 1/2 LSB (or ± 1.61% Full Scale); that guarantees its monotonicity.

Error Amplifier

In order to have a good stability, the Error Amplifier must work with a closed loop gain greater or equal than 20 dB.

Position Amplifier

It is inserted by means of the strobe signal, TTL and microprocessor compatible. Its output is connected to pin 16 when V_{strobe}= Low; pin 16 is grounded for V_{strobe}= High.

SYSTEM DESCRIPTION: refer to the L292 data sheet.

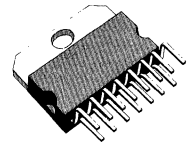
L292

SWITCH-MODE DRIVER FOR DC MOTORS

The L292 is a monolithic LSI circuit in 15-lead Multiwatt® package. It is intended for use, together with L290 and L291, as a complete **3-chip motor positioning system** for applications such as carriage/daisy-wheel position control in typewrites.

The L290/1/2 system can be directly controlled by a microprocessor. The outstanding characteristics of the L292 are:

- Driving capability: 2A, 36V, 30KHz
- 2 Logic chip enable
- External loop gain adjustment
- Single power supply (18 to 36V)
- Input signal symmetric to ground
- Thermal protection



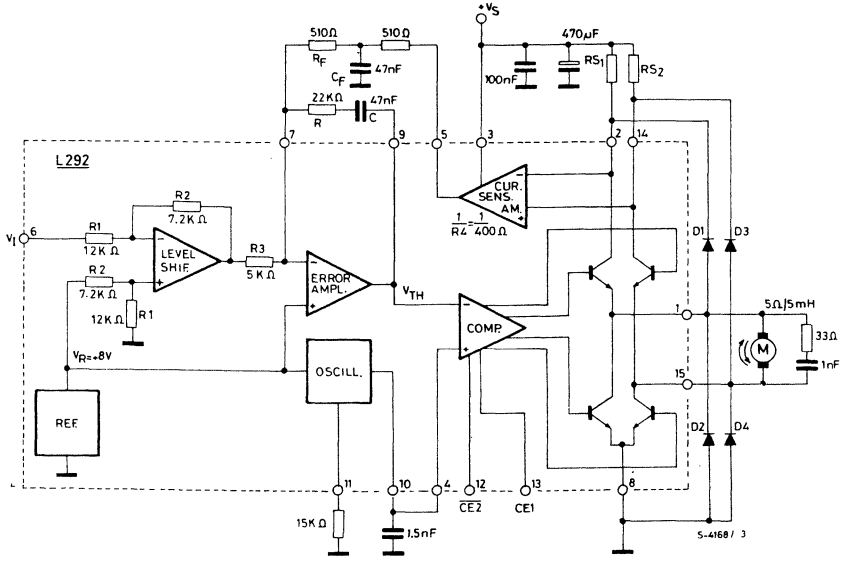
Multiwatt 15

ORDERING NUMBER: L292

ABSOLUTE MAXIMUM RATINGS

V_s	Power supply	36	V
V_i	Input voltage	-15 to $+V_s$	V
$V_{inhibit}$	Inhibit voltage	0 to V_s	V
I_o	Output current	2.5	A
P_{tot}	Total power dissipation (T_{case} = 75°C)	25	W
T_{stg}	Storage and junction temperature	-40 to +150	°C

BLOCK DIAGRAM AND TEST CIRCUIT

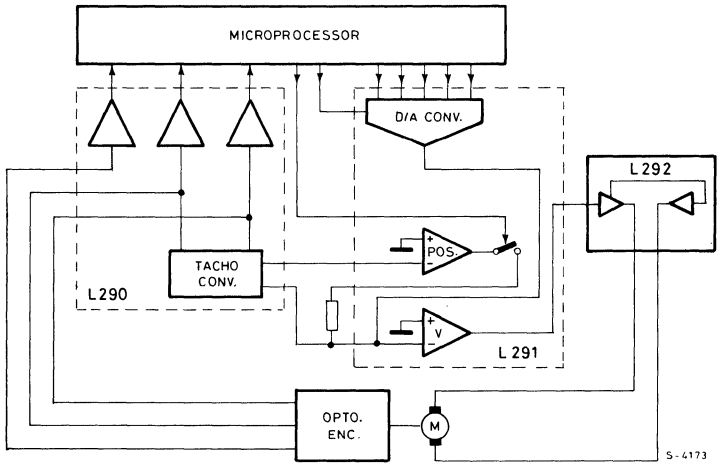


D1 · D2 · D3 · D4 = High speed diodes { $V_F \leq 1.2V$ @ I = 2A; trr ≤ 200 ns

SYSTEM DESCRIPTION

The L290, L291 and L292 are intended to be used as a 3-chip microprocessor controlled positioning system. These devices may be used separately - particularly the L292 motor driver - but since they will usually be used together, a description of a typical L290/1/2 system follows.

Fig. 1 - System block diagram



The system operates in two modes to achieve high-speed, high-accuracy positioning.
Speed commands for the system originate in the microprocessor. It is continuously updated on the motor position by means of pulses from the L290 tachometer chip, which in turn gets its information from the optical encoder. From this basic input, the microprocessor computes a 5-bit control word that sets the system speed dependent on the distance to travel.
When the motor is stopped and the microprocessor orders it to a new position, the system operates initially in an open-loop configuration as there is no feedback from the tachometer generator. Therefore maximum current is fed to the motor. As maximum speed is reached, the tachometer chip output backs off the processor signal thus reducing accelerating torque.
The motor continues to run at top speed but under closed-loop control.
As the target position is approached, the microprocessor lowers the value of the speed-demand word; this reduces the voltage at the main summing point, in effect braking the motor. The braking is applied progressively until the motor is running at minimum speed.
At that time, the microprocessor orders a switch to the position mode, (strobe signal at pin 8 of L291) and within 3 to 4 ms the L292 drives the motor to a null position, where it is held by electronic "detenting".

SYSTEM DESCRIPTION (continued)

The ERRV signal (from pin 1, L291) is fed to pin 6 of the final chip, the L292 H-bridge motor-driver. This input signal is bidirectional so it must be converted to a positive signal because the L292 uses a single supply voltage. This is accomplished by the first stage - the level shifter, which uses an internally generated 8V reference.

This same reference voltage supplies the triangle wave oscillator whose frequency is fixed by the external RC network (R_{20}, C_{17} - pins 11 and 10) where:

$$f_{osc} = \frac{1}{2RC} \qquad \text{(with } R \geqslant 8.2\ K\Omega\text{)}$$

The oscillator determines the switching frequency of the output stage and should be in the range 1 to 30 KHz.

Motor current is regulated by an internal loop in the L292 which is performed by the resistors R_{18}, R_{19} and the differential current sense amplifier, the output of which is filtered by an external RC network and fed back to the error amplifier.

The choice of the external components in these RC network (pins 5, 7, 9) is determined by the motor type and the bandwidth requirements. The values shown in the diagram are for a 5Ω, 5 mH motor. (See L292 Transfer Function Calculation in Application Information).

The error signal obtained by the addition of the input and the current feedback signals (pin 7) is used to pulse width modulate the oscillator signal by means of the comparator. The pulse width modulated signal controls the duty cycle of the H-bridge to give an output current corresponding to the L292 input signal.

The interval between one side of the bridge switching off and the other switching on, τ, is programmed by C_{17} in conjunction with an internal resistor R_τ.

This can be found from:

$$\tau = R_\tau \cdot C_{pin\ 10}. \quad (C_{17} \text{ in the diagram})$$

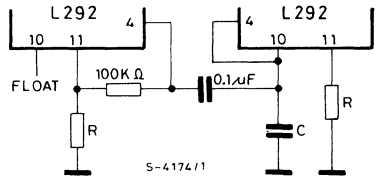
Since R_τ is approximately 1.5 KΩ and the recommended τ to avoid simultaneous conduction is 2.5 μs $C_{pin\ 10}$ should be around 1.5 nF.

The current sense resistors R_{18} and R_{19} should be high precision types (maximum tolerance ± 2%) and the recommended value is given by:

$$R_{max} \cdot I_{o\ max} \leqslant 0.44V$$

It is possible to synchronize two L292's, if desired, using the network shown in fig. 2.

Fig. 2

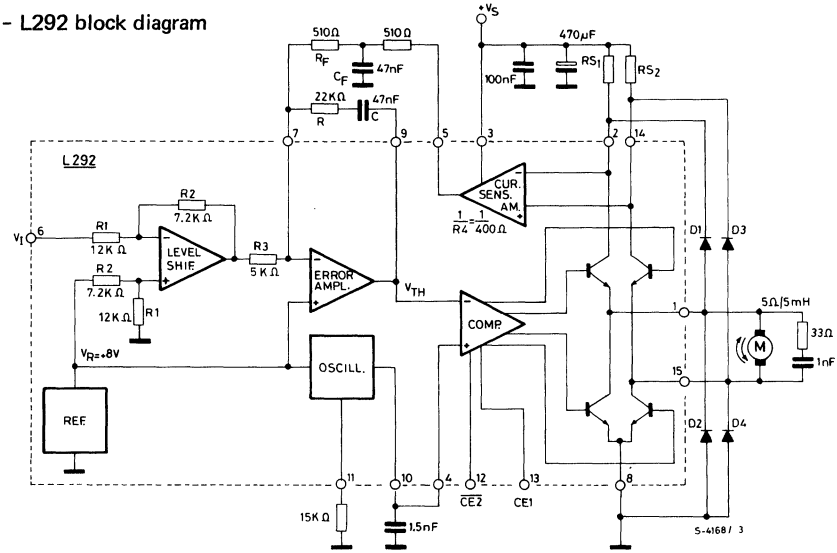


Finally, two enable inputs are provided on the L292 (pins 12 and 13-active low and high respectively).

APPLICATION INFORMATION

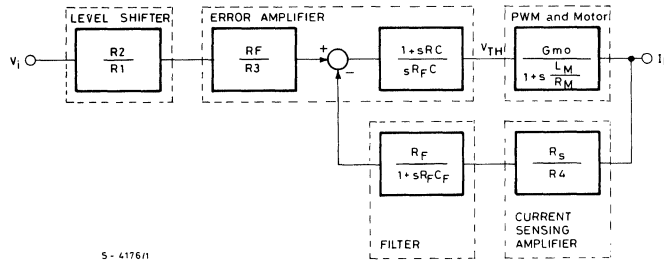
This section has been added in order to help the designer for the best choise of the values of external components.

Fig. 5 - L292 block diagram



The schematic diagram used for the Laplace analysis of the system is shown in fig. 6.

Fig. 6



$R_{S1} = R_{S2} = R_S$ (sensing resistors)

$\frac{1}{R_4} = 2.5 \cdot 10^{-3}\ \Omega$ (current sensing amplifier transconductance)

L_M = Motor inductance

R_M = Motor resistance

I_M = Motor current

$G_{mo} = \frac{I_M}{V_{TH}}\Big|_{s=0}$ (DC transfer function from the input of the comparator (V_{TH}) to the motor current (I_M)).

APPLICATION INFORMATION (continued)

Closed-loop system step response

a) **Small-signals analysis.**

The transfer function (3) can be written as follows:

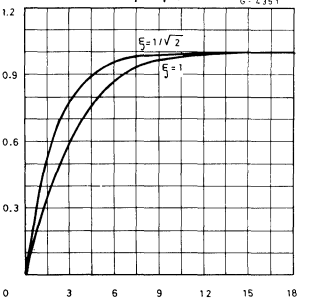
$$\frac{I_M}{V_I}(s) = \frac{0.044}{R_s} \frac{1 + \frac{s}{2\xi\omega_o}}{1 + \frac{2\xi s}{\omega_o} + \frac{s^2}{\omega_o^2}} \qquad (7)$$

where: $\omega_o = \sqrt{\frac{G_{mo} R_s}{R_4 C R_F C_F}}$ is the cutoff frequency

$\xi = \sqrt{\frac{R_4 C}{4 R_F C_F G_{mo} R_s}}$ is the dumping factor

By choosing the ξ value, it is possible to determine the system response to an input step signal. Examples:

Fig. 8 - Small signal step response (normalized amplitude vs. $t/R_F C_F$)



1) $\xi = 1$ from which

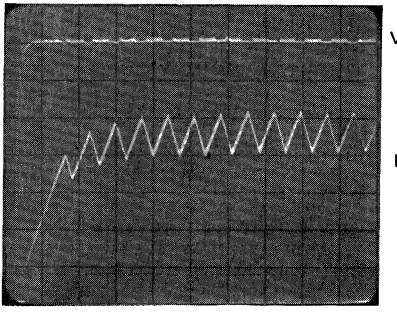
$$I_M(t) = \frac{0.044}{R_s}\left[1 - e^{-\frac{t}{2R_F C_F}}\left(1 + \frac{t}{4 R_F C_F}\right)\right] \cdot V_i$$

(where V_i is the amplitude of the input step).

2) $\xi = \frac{1}{\sqrt{2}}$ from which

$$I_M(t) = \frac{0.044}{R_s}\left(1 - \cos\frac{t}{2R_F C_F} e^{-\frac{t}{2R_F C_F}}\right) V_i$$

Fig. 9 - Motor current and pin 7 voltage waveforms (application of fig. 5). Small signal response



V_7 = 200mV/div.
I_M = 100mA/div.
t = 100μs/div.
with V_I = 1.5 Vp.

From fig. 9, it is possible to verify that the L292 works in "closed-loop" conditions during the entire motor current rise-time: the voltage at pin 7 (inverting input of the error amplifier) is locked to the reference voltage V_R, present at the non-inverting input of the same amplifier.
The previous linear analysis is correct for this example.
Decreasing the ξ value, the rise-time of the current decreases. But for a good stability, from relationship (6), the minimum value of ξ is:

$$\xi_{min} = \frac{1}{2\sqrt[4]{2}} \qquad \text{(phase margin} = 45°\text{)}$$

APPLICATION INFORMATION (continued)

Example:

a) Data

- Motor characteristics : $L_M = 5$ mH, $R_M = 5\Omega$, $L_M/R_M = 1$ msec
- Voltage and current characteristics: $V_s = 20V$ $I_M = 2A$ $V_I = 9.1V$
- Closed loop bandwidth: 3 kHz.

b) Calculation

- From relationship (4):

$$R_s = \frac{0.044}{I_M} \quad V_I = 0.2\Omega$$

and from (1):

$$G_{mo} = \frac{2\,V_s}{R_M\,V_R} = 1\ \Omega^{-1}$$

- $RC = 1$ msec [from expression (2)].
- Assuming $\xi = 1/\sqrt{2}$; from (7) follows:

$$\xi^2 = \frac{1}{2} = \frac{400\,C}{4\,R_F C_F \cdot 0.2}$$

- The cutoff frequency is:

$$f_T = \frac{143 \cdot 10^{-3}}{R_F C_F} = 3\ \text{kHz}$$

c) Summarising

- $RC = 1 \cdot 10^{-3}$ sec
- $\frac{1000\,C}{R_F\,C_F} = 1$
- $R_F C_F \cong 47\ \mu s$

$C = 47$ nF
$R = 22$ KΩ
For $R_F = 510\ \Omega \rightarrow C_F = 92$ nF

L293
L293E

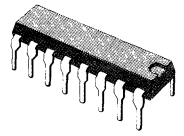
PUSH-PULL FOUR CHANNEL DRIVERS

- OUTPUT CURRENT 1A PER CHANNEL
- PEAK OUTPUT CURRENT 2A PER CHANNEL (NON REPETITIVE)
- INHIBIT FACILITY
- HIGH NOISE IMMUNITY
- SEPARATE LOGIC SUPPLY
- OVERTEMPERATURE PROTECTION

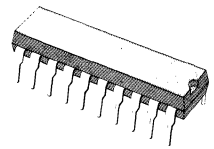
The L293 and L293E are quad push-pull drivers capable of delivering output currents to 1A per channel. Each channel is controlled by a TTL-compatible logic input and each pair of drivers (a full bridge) is equipped with an inhibit input which turns off all four transistors. A separate supply input is provided for the logic so that it may be run off a lower voltage to reduce dissipation.

Additionally, the L293E has external connection of sensing resistors, for switchmode control.

The L293 and L293E are packaged in 16 and 20-pin plastic DIPs respectively; both use the four center pins to conduct heat to the printed circuit board.



DIP-16 Plastic
(0.4)



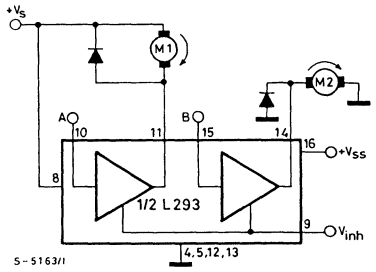
Powerdip
16 + 2 + 2

ORDERING NUMBERS: L293B (16 leads)
L293E (20 leads)

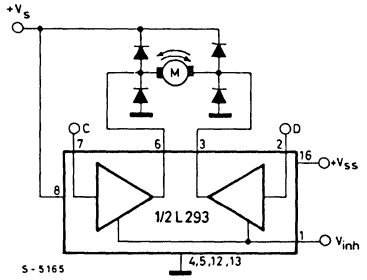
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	36	V
V_{ss}	Logic supply voltage	36	V
V_i	Input voltage	7	V
V_{inh}	Inhibit voltage	7	V
I_{out}	Peak output current (non-repetitive t = 5ms)	2	A
P_{tot}	Total power dissipation at $T_{ground-pins}$ = 80°C	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

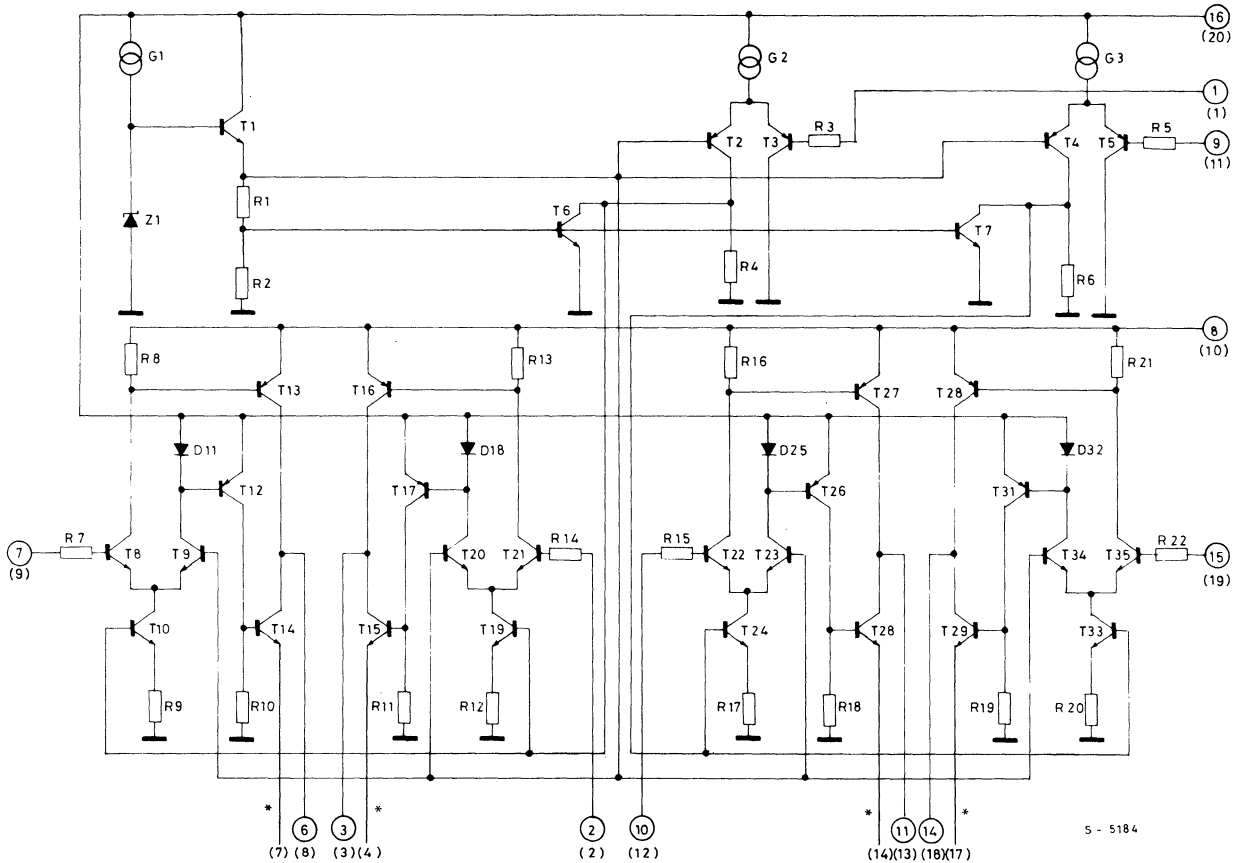
DC motor control



Bidirectional DC motor control



SCHEMATIC DIAGRAM



(*) In the L293 these points are not externally available. They are internally connected to the ground (substrate).

○ Pins of L293 ( ) Pins of L293E

TRUTH TABLE

V_i (eacn channel)	V_o	$V_{inh.}$ (°°)
H	H	H
L	L	H
H	X (°)	L
L	X (°)	L

(°) High output impedance.
(°°) Relative to the considerate channel.

Fig. 1 - Switching times

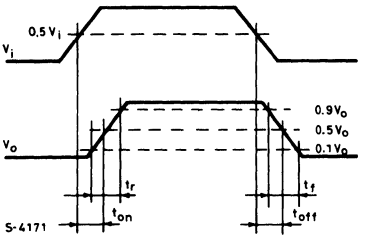


Fig. 2 - Saturation voltage vs. output current

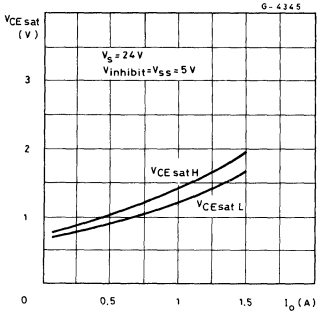


Fig. 3 - Source saturation voltage vs. ambient temperature

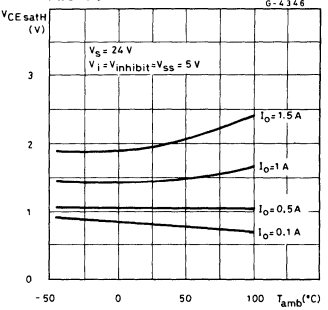


Fig. 4 - Sink saturation voltage vs. ambient temperature

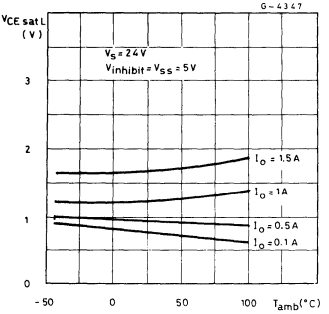


Fig. 5 - Quiescent logic supply current vs. logic supply voltage

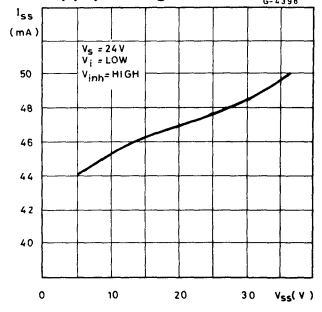


Fig. 6 - Output voltage vs. input voltage

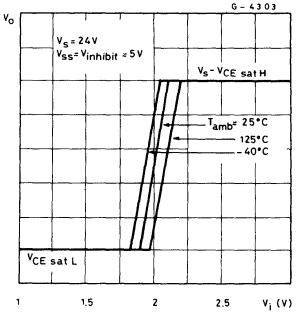
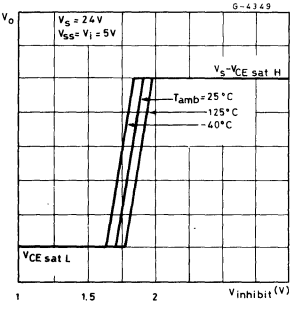
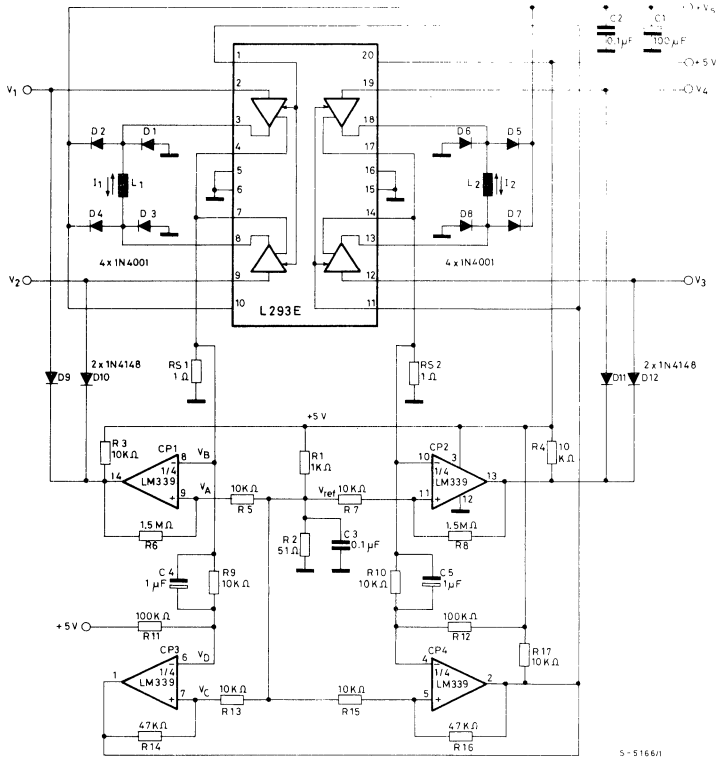


Fig. 7 - Output voltage vs. inhibit voltage



APPLICATION INFORMATION (continued)

Fig. 11 - Stepping motor driver with phase current control and short circuit protection



D1 to D8 : $\begin{cases} V_F \leqslant 1.2V \text{ @ } I = 300 \text{ mA} \\ trr \leqslant 200 \text{ ns} \end{cases}$

L293C

ADVANCE DATA

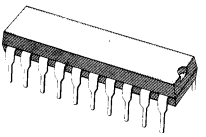
PUSH-PULL FOUR CHANNEL/DUAL H-BRIDGE DRIVER

- 600mA OUTPUT CURRENT CAPABILITY PER CHANNEL
- 1.2A PEAK OUTPUT CURRENT (NON REPETITIVE) PER CHANNEL
- ENABLE FACILITY
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5V (HIGH NOISE IMMUNITY)
- SEPARATE HIGH VOLTAGE POWER SUPPLY (UP TO 44V)

The L293C is a monolithic high voltage, high current integrated circuit four channel driver in a 20 pin DIP. It is designed to accept standard TTL or DTL input logic levels and drive inductive loads (such as relays, solenoids, DC and stepping motors) and switching power transistors.

The device may easily be used as a dual H-bridge driver: separate chip enable and high voltage power supply pins are provided for each H-bridge. In addition, a separate power supply is provided for the logic section of the device.

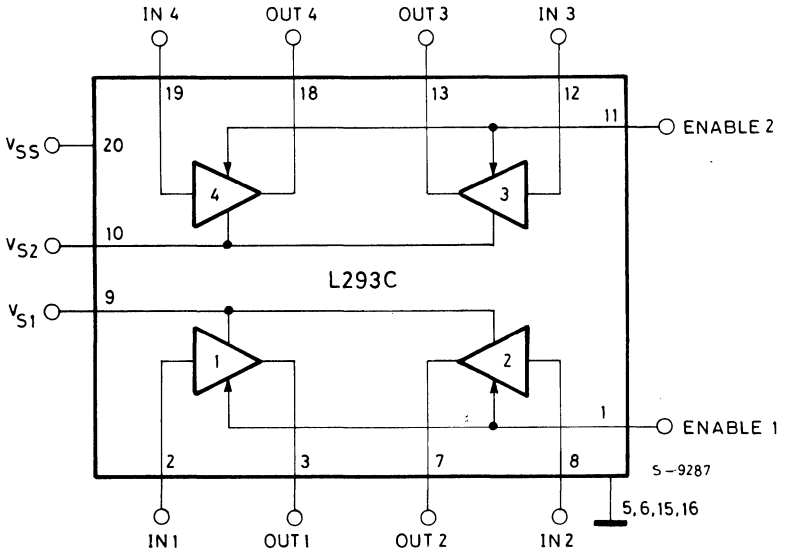
The L293C is assembled in a 20 lead plastic package which has 4 center pins connected together and used for heatsinking.



Powerdip
16+2+2

ORDER CODE: L293C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (For each channel, V_S = 24V, V_{SS} = 5V, T_{amb} = 25°C, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply voltage (pin 9, 10)		V_{SS}		44	V
V_{SS}	Logic supply voltage (pin 20)		4.5		7	V
I_S	Total quiescent supply current (pin 9, 10)	V_i = L; I_o = 0; V_{EN} = H		2	6	mA
		V_i = H; I_o = 0; V_{EN} = H		16	24	mA
		V_{EN} = L			4	mA
I_{SS}	Total quiescent logic supply current (pin 20)	V_i = L; I_o = 0; V_{EN} = H		44	60	mA
		V_i = H; I_o = 0; V_{EN} = H		16	22	mA
		V_{EN} = L		16	24	mA
V_{IL}	Input low voltage (pin 2, 8, 12, 19)		-0.3		1.5	V
V_{IH}	Input high voltage (pin 2, 8, 12, 19)		2.3		V_{SS}	V
I_{IL}	Low voltage input current (pin 2, 8, 12, 19)	V_i = 1.5V			-10	μA
I_{IH}	High voltage input current (pin 2, 8, 12, 19)	2.3V ≤ V_i ≤ V_{SS} -0.6V		30	100	μA
V_{ENL}	Enable low voltage (pin 1, 11)		-0.3		1.5	V
V_{ENH}	Enable high voltage (pin 1, 11)		2.3		V_{SS}	V
I_{ENL}	Low voltage enable current (pin 1, 11)	V_{ENL} = 1.5V		-30	-100	μA
I_{ENH}	High voltage enable current (pin 1, 11)	2.3V ≤ VENH ≤ V_{ss} -0.6			± 10	μA
$V_{CE(sat)H}$	Source output saturation voltage (pins 3, 7, 13, 18)	I_o = -0.6A		1.4	1.8	V
$V_{CE(sat)L}$	Sink output saturation voltage (pins 3, 7, 13, 18)	I_o = +0.6A		1.2	1.8	V
t_r	Rise time (*)	0.1 to 0.9 V_o		250		ns
t_f	Fall time (*)	0.9 to 0.1 V_o		250		ns
t_{on}	Turn-on delay (*)	0.5 V_i to 0.5 V_o		750		ns
t_{off}	Turn-off delay (*)	0.5 V_i to 0.5 V_o		200		ns

(*) See switching times diagram

L293D

PRELIMINARY DATA

PUSH-PULL FOUR CHANNEL DRIVER WITH DIODES

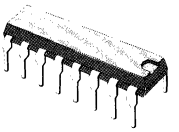
- 600mA OUTPUT CURRENT CAPABILITY PER CHANNEL
- 1.2A PEAK OUTPUT CURRENT (NON RE-PETITIVE) PER CHANNEL
- ENABLE FACILITY
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VILTAGE UP TO 1.5V (HIGH NOISE IMMUNITY)
- INTERNAL CLAMP DIODES

The L293D is a monolithic integrated high voltage, high current four channel driver designed to accept standard DTL or TTL logic levels and drive inductive loads (such as relays solenoides, DC and stepping motors) and switching power transistors.

To simplify use as two bridges each pair of channels is equipped with an enable input. A separate supply input is provided for the logic, allowing operation at a lower voltage and internal clamp diodes are included.

This device is suitable for use in switching applications at frequencies up to 5 kHz.

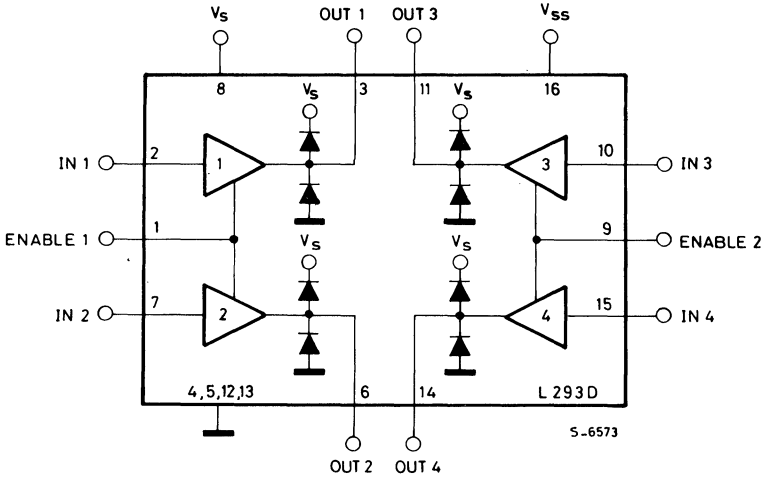
The L293D is assembled in a 16 lead plastic package which has 4 center pins connected together and used for heatsinking.



Powerdip
12 + 2 + 2

ORDERING NUMBER: L293D

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (For each channel, V_s = 24V, V_{ss} = 5V, T_{amb} = 25°C, unless otherwise specified)

Parameter		Test condition	Min.	Typ.	Max.	Unit
V_s	Supply voltage (pin 8)		V_{ss}		36	V
V_{ss}	Logic supply voltage (pin 16)		4.5		36	V
I_s	Total quiescent supply current (pin 8)	V_i = L I_o = 0 V_{en} = H		2	6	mA
		V_i = H I_o = 0 V_{en} = H		16	24	
		V_{en} = L			4	
I_{ss}	Total quiescent logic supply current (pin 16)	V_i = L I_o = 0 V_{en} = H		44	60	mA
		V_i = H I_o = 0 V_{en} = H		16	22	
		V_{en} = L		16	24	
V_{IL}	Input low voltage (pin 2, 7, 10, 15)		-0.3		1.5	V
V_{IH}	Input high voltage (pin 2, 7, 10, 15)	$V_{ss} \leq 7V$	2.3		V_{ss}	V
		$V_{ss} > 7V$	2.3		7	
I_{IL}	Low voltage input current (pin 2, 7, 10, 15)	V_{IL} = 1.5V			-10	μA
I_{IH}	High voltage input current (pin 2, 7, 10, 15)	$2.3V \leq V_{IH} \leq V_{ss} - 0.6V$		30	100	μA
V_{enL}	Enable low voltage (pin 1, 9)		-0.3		1.5	V
V_{enH}	Enable high voltage (pin 1, 9)	$V_{ss} \leq 7V$	2.3		V_{ss}	V
		$V_{ss} > 7V$	2.3		7	
I_{enL}	Low voltage enable current current (pin 1, 9)	V_{enL} = 1.5V		-30	-100	μA
i_{enH}	High voltage enable current (pin 1, 9)	$2.3V \leq V_{enH} \leq V_{ss} - 0.6V$			± 10	μA
V_{CEsatH}	Source output saturation voltage (pins 3, 6, 11, 14)	I_o = - 0.6A		1.4	1.8	V
V_{CEsatL}	Sink output saturation voltage (pins 3, 6, 11, 14)	I_o = + 0.6A		1.2	1.8	V
V_F	Clamp diode forward voltage	I_o = 600 mA		1.3		V
t_r	Rise time (*)	0.1 to 0.9 V_o		250		ns
t_f	Fall time (*)	0.9 to 0.1 V_o		250		ns
t_{on}	Turn-on delay (*)	0.5 V_i to 0.5 V_o		750		ns
t_{off}	Turn-off delay (*)	0.5 V_i to 0.5 V_o		200		ns

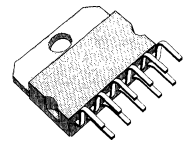
(*) See fig. 1

SWITCH-MODE SOLENOID DRIVER

- HIGH VOLTAGE OPERATION (UP TO 50V)
- HIGH OUTPUT CURRENT CAPABILITY (UP TO 4A)
- LOW SATURATION VOLTAGE
- TTL-COMPATIBLE INPUT
- OUTPUT SHORT CIRCUIT PROTECTION (TO GROUND, TO SUPPLY AND ACROSS THE LOAD)
- THERMAL SHUTDOWN
- OVERDRIVING PROTECTION
- LATCHED DIAGNOSTIC OUTPUT

The L294 is a monolithic switchmode solenoid driver designed for fast, high-current applications such as hammer and needle driving in printers and electronic typewriters. Power dissipation is reduced by effecient switchmode operation. An extra feature of the L294 is a latched diagnostic output which indicates when the output is short circuited.

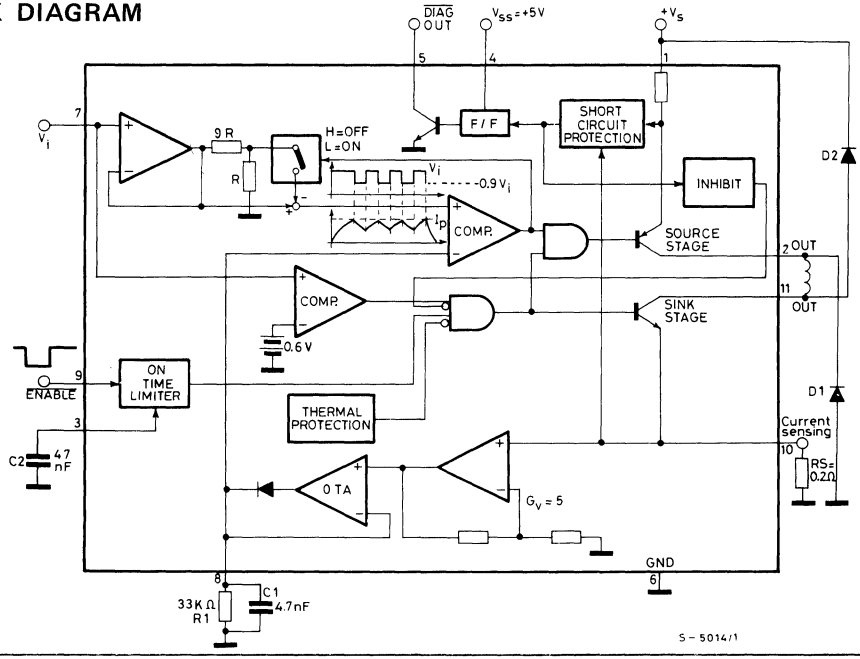
The L294 is supplied in a 11-lead Multiwatt® plastic power package.



Multiwatt 11

ORDER CODE: L294

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $V_s = 40V$, $V_{ss} = 5V$, $T_{amb} = 25°C$, unless otherwise specified).

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Power supply voltage (pin 1)	Operative condition	12		46	V
I_d	Quiescent drain current (pin 1)	$V_{ENABLE} = H$		20	30	mA
		$V_i \geq 0.6V$; $V_{ENABLE} = L$		70		
V_{ss}	Logic supply voltage (pin 4)		4.5		7	V
I_{ss}	Quiescent logic supply current	$V_{DIAG} = L$		5	8	mA
		DIAG output at high impedance		10	100	μA
V_i	Input voltage (pin 7)	Operating output	0.6			V
		Non-operative output			0.45	
I_i	Input current (pin 7)	$V_i \geq 0.6V$		-1		μA
		$V_i \leq 0.45V$		-3		
V_{ENABLE}	Enable input voltage (pin 9)	Low level	-0.3		0.8	V
		High level	2.4			
I_{ENABLE}	Enable input current (pin 9)	$V_{ENABLE} = L$			-100	μA
		$V_{ENABLE} = H$			100	
I_{load}/V_i	Transconductance	$R_s = 0.2\ \Omega$ $V_i = 1V$	0.95	1	1.05	A/V
		$V_i = 4V$	0.97	1	1.03	
$V_{sat\ H}$	Source output saturation voltage	$I_p = 4A$		1.7		V
$V_{sat\ L}$	Sink output saturation voltage	$I_p = 4A$		2		V
$V_{sat\ H} + V_{sat\ L}$	Total saturation voltage	$I_p = 4A$			4.5	V
$I_{leakage}$	Output leakage current	$R_s = 0.2\Omega$; $V_i \leq 0.45V$		1		mA
K	On time limiter constant (°)	$V_{ENABLE} = L$		120		
V_{DIAG}	Diagnostic output voltage (pin 5)	$I_{DIAG} = 10$ mA			0.4	V
I_{DIAG}	Diagnostic leakage current (pin 5)	$V_{DIAG} = 40V$			10	μA
$\frac{V_{pin\ 8}}{V_{pin\ 10}}$	OP AMP and OTA DC voltage gain (°°)	$V_{pin\ 10} = 100$ to 800 mV		5		
V_{SENS}	Sensing voltage (pin 10) (°°°)				0.9	V

(°) After a time interval $t_{max} = KC_2$, the output stages are disabled.
(°°) See the block diagram.
(°°°) Allowed range of V_{SENS} without the intervention of the short circuit protection.

CIRCUIT OPERATION (continued)

voltage at pin 1 and then by switching the device on again. After that, two cases are possible: the reason for the "bad operation" is still present and the protection acts again; the reason has been removed and the device starts to work properly.

Fig. 1 - Output current waveforms

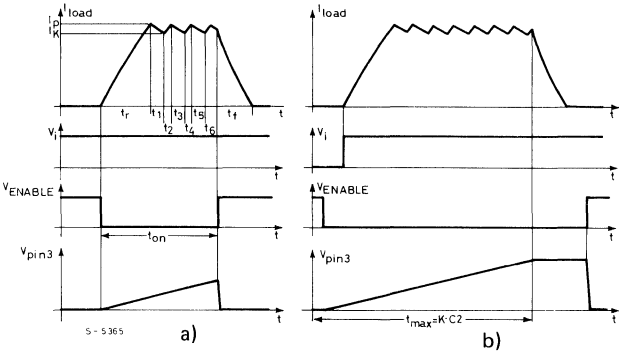
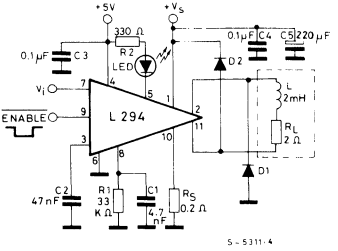


Fig. 2 - Test and typical application circuit



D1: 3A fast diode
D2: 1A fast diode
} trr ≤ 200 ns

Fig. 3 - Peak output current vs. input voltage

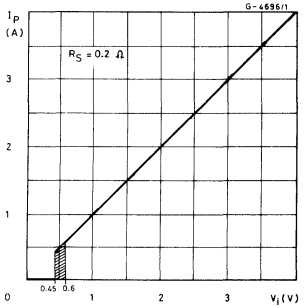


Fig. 4 - Output saturation voltages vs. peak output current

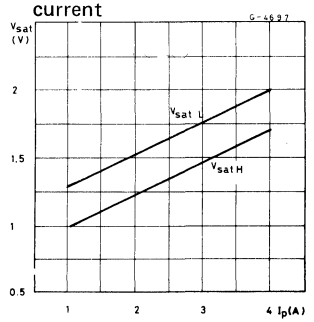


Fig. 5 - Safe operating areas

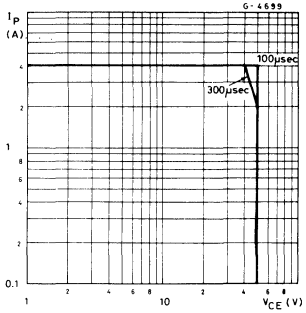
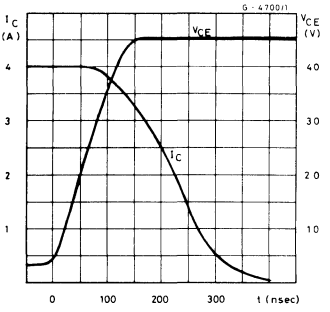


Fig. 6 - Turn-off phase



L295

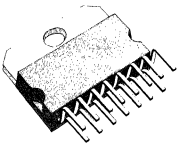
PRELIMINARY DATA

DUAL SWITCH-MODE SOLENOID DRIVER

- HIGH CURRENT CAPABILITY (UP TO 2.5A PER CHANNEL)
- HIGH VOLTAGE OPERATION (UP TO 46V FOR POWER STAGE)
- HIGH EFFICIENCY SWITCHMODE OPERATION
- REGULATED OUTPUT CURRENT (ADJUSTABLE)
- FEW EXTERNAL COMPONENTS
- SEPARATE LOGIC SUPPLY
- THERMAL PROTECTION

The L295 is a monolithic integrated circuit in a 15-lead Multiwatt® package; it incorporates all the functions for direct interfacing between digital circuitry and inductive loads. The L295 is designed to accept standard microprocessor logic levels at the inputs and can drive 2 solenoids. The output current is completely controlled by means of a switching technique allowing very efficient operation. Furthermore, it includes an enable input and dual supplies (for interfacing with peripherals running at a higher voltage than the logic).

The L295 is particularly suitable for applications such as hammer driving in matrix printers, step motor driving and electromagnet controllers.



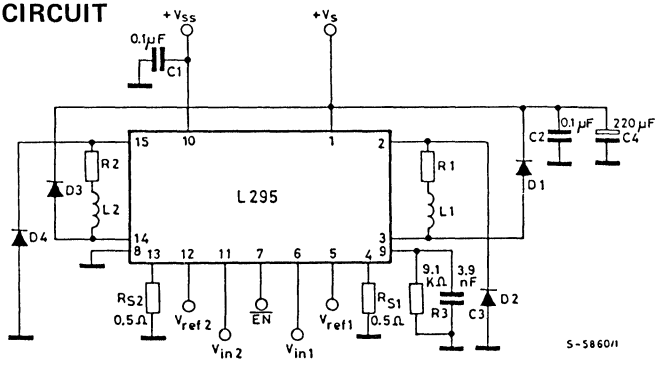
Multiwatt 15

ORDERING NUMBER: L295

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	50	V
V_{ss}	Logic supply voltage	12	V
V_{EN}, V_i	Enable and input voltage	7	V
V_{ref}	Reference voltage	7	V
I_o	Peak output current (each channel)		
	– non repetitive (t = 100 μsec)	3	A
	– repetitive (80% on -20% off; t_{on} = 10 ms)	2.5	A
	– DC operation	2	A
P_{tot}	Total power dissipation (at T_{case} = 75°C)	25	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

APPLICATION CIRCUIT



ELECTRICAL CHARACTERISTICS (Refer to the application circuit, V_{SS}= 5V; V_s= 36V; T_j = 25°C; L = low; H = high; unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply Voltage			12		46	V
V_{ss}	Logic Supply voltage			4.75		10	V
I_d	Quiescent drain current (from V_s)	V_s = 46V; V_{i1}= V_{i2}= V_{EN}= L				4	mA
I_{ss}	Quiescent drain current (from V_{ss})	V_{ss} = 10V				46	mA
V_{i1}, V_{i2}	Input Voltage		Low	-0.3		0.8	V
			High	2.2		7	
V_{EN}	Enable Input Voltage		Low	-0.3		0.8	V
			High	2.2		7	
I_{i1}, I_{i2}	Input Current		V_{i1}= V_{i2}= L			-100	μA
			V_{i1}= V_{i2}= H			10	
I_{EN}	Enable Input Current		V_{EN}= L			-100	μA
			V_{EN}= H			10	
V_{ref1}, V_{ref2}	Input Reference Voltage			0.2		2	V
I_{ref1}, I_{ref2}	Input Reference Current					-5	μA
f_{osc}	Oscillation Frequency	C = 3.9 nF;	R = 9.1 KΩ		25		KHz
$\frac{I_p}{V_{ref}}$	Transconductance (each ch.)	V_{ref}= 1V	R_s = 0.5Ω	1.9	2	2.1	A/V
V_{drop}	Total output voltage drop (each channel) (*)	I_o = 2A			2.8	3.6	V
$V_{sens\ 1}$ $V_{sens\ 2}$	External sensing resistors voltage drop					2	V

(*) V_{drop}= $V_{CEsat\ Q1}$ + $V_{CEsat\ Q2}$.

The current increases until the voltage on the external sensing resistor, R_{S1}, reaches the reference voltage, V_{ref1}. This peak current, I_{p1}, is given by:

$$I_{p1} = \frac{V_{ref1}}{R_{S1}}$$

At this point the comparator output, Comp1, sets the RS flip-flop, FF1, that turns off the output transistor, Q1. The load current flowing through D2, Q2, R_{S1}, decreases according to the law:

$$I = \left(\frac{V_A}{R1} + I_{p1}\right) e^{\frac{-R1\,t}{L1}} - \frac{V_A}{R1}$$

where

$$V_A = V_{CE\,sat\ Q2} + V_{sense\ 1} + V_{D2}$$

If the oscillator pin (9) is connected to ground the load current falls to zero as shown in fig. 1.

At the time t_2 the channel 1 is disabled, by taking the inputs V_{in1} low and/or $\overline{EN}$ high, and the output transistor Q2 is turned off. The load current flows through D2 and D1 according to the law:

$$I = \left(\frac{V_B}{R1} + I_{T2}\right) e^{\frac{-R1\,t}{L1}} - \frac{V_B}{R1}$$

where

$$V_B = V_s + V_{D1} + V_{D2}$$

I_{T2} = current value at the time t_2.

Fig. 2 in shows the current waveform obtained with an RC network connected between pin 9 and ground. From to t_1 the current increases as in fig. 1. A difference exists at the time t_2 because the current starts to increase again. At this time a pulse is produced by the oscillator circuit that resets the flip flop, FF1, and switches on the output transistor, Q1. The current increases until the drop on the sensing resistor R_{s1} is equal to V_{ref1} (t_3) and the cycle repeats.

The switching frequency depends on the values of R and C, as shown in fig. 4 and must be chosen in the range 10 to 30 KHz.
It is possible with external hardware to change the reference voltage V_{ref} in order to obtain a high peak current I_p and a lower holding current I_h (see fig. 3).

The L295 is provided with a thermal protection that switches off all the output transistors when the junction temperature exceeds 150°C. The presence of a hysteresis circuit makes the IC work again after a fall of the junction temperature of about 20°C.

The analog input pins (V_{ref1}, V_{ref2}) can be left open or connected to V_{ss}; in this case the circuit works with an internal reference voltage of about 2.5V and the peak current in the load is fixed only by the value of R_S:

$$I_p = \frac{2.5}{R_S}$$

L296
L296P

ADVANCE DATA

HIGH CURRENT SWITCHING REGULATORS

- 4A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 100% DUTY CYCLE RANGE
- PRECISE (±2%) ON-CHIP REFERENCE
- SWITCHING FREQUENCY UP TO 200KHz
- VERY HIGH EFFICIENCY (UP TO 90%)
- VERY FEW EXTERNAL COMPONENTS
- SOFT START
- RESET OUTPUT
- EXTERNAL PROGRAMMABLE LIMITING CURRENT (L296P)
- CONTROL CIRCUIT FOR CROWBAR SCR
- INPUT FOR REMOTE INHIBIT AND SYNCHRONUS PWM
- THERMAL SHUTDOWN

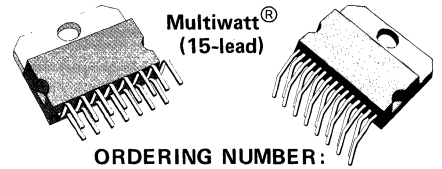
The L296 and L296P are stepdown power switching regulators delivering 4A at a voltage variable from 5.1V to 40V.

Features of the devices include soft start, remote inhibit, thermal protection, a reset output for microprocessors and a PWM comparator input for synchronization in multichip configurations.

The L296P includes external programmable limiting current.

The L296 and L296P are mounted in a 15-lead Multiwatt® plastic power package and requires very few external components.

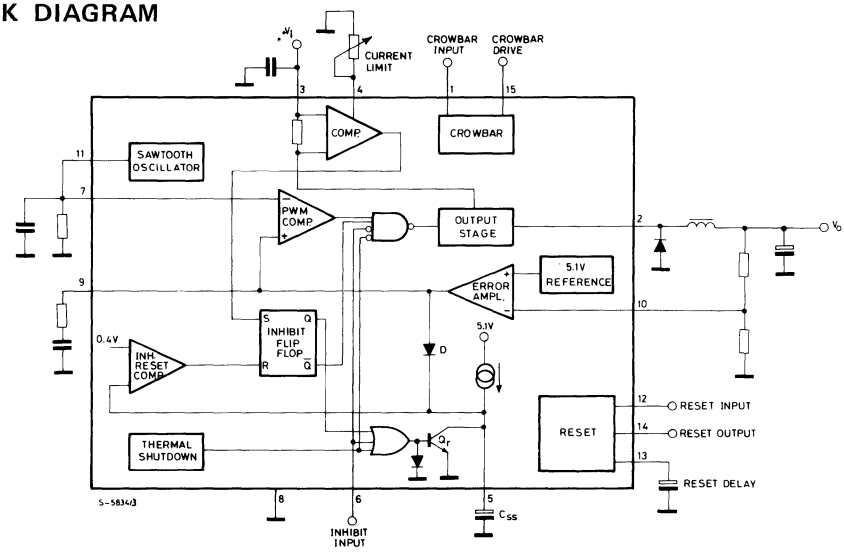
Efficient operation at switching frequencies up to 200KHz allows a reduction in the size and cost of external filter components. A voltage sense input and SCR drive output are provided for optional crowbar overvoltage protection with an external SCR.



ORDERING NUMBER:

L296	L296HT
L296P	L296PHT

BLOCK DIAGRAM



PIN FUNCTIONS

N°	NAME	FUNCTION
1	CROWBAR INPUT	Voltage sense input for crowbar overvoltage protection. Normally connected to the feedback input thus triggering the SCR when V_{out} exceeds nominal by 20%. May also monitor the input and a voltage divider can be added to increase the threshold. Connected to ground when SCR not used.
2	OUTPUT	Regulator output.
3	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the L296's internal logic.
4	CURRENT LIMIT	A resistor connected between this terminal and ground sets the current limiter threshold. If this terminal is left unconnected the threshold is internally set (see electrical charateristics).
5	SOFT START	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
6	INHIBIT INPUT	TTL – level remote inhibit. A logic high level on this input disables the device.
7	SYNC INPUT	Multiple L296s are synchronized by connecting the pin 7 inputs together and omitting the oscillator RC network on all but one device.
8	GROUND	Common ground terminal.
9	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
10	FEEDBACK INPUT	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
11	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency. This pin must be connected to pin 7 input when the internal oscillator is used.

CIRCUIT OPERATION (continued)

Fig. 1 - Reset output waveforms

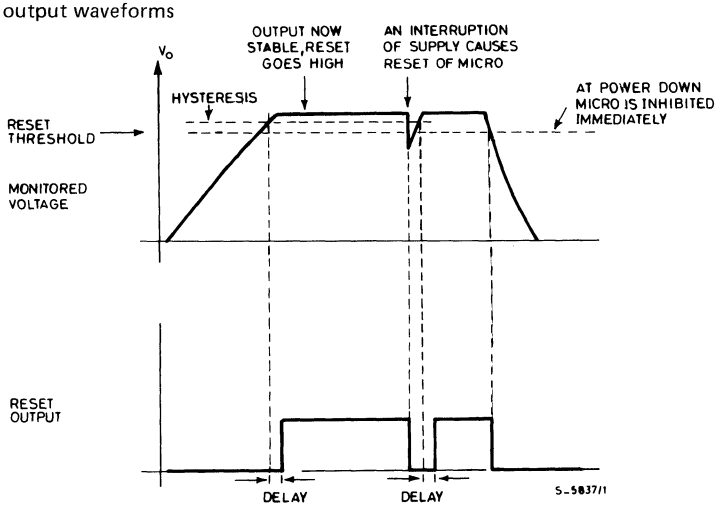


Fig. 2 - Soft start waveforms

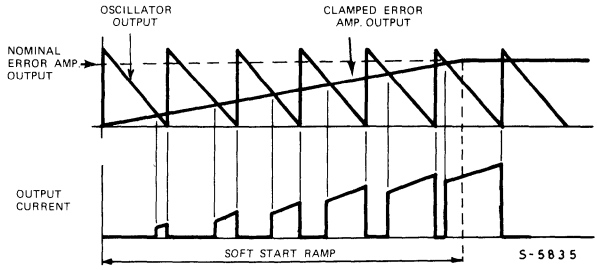
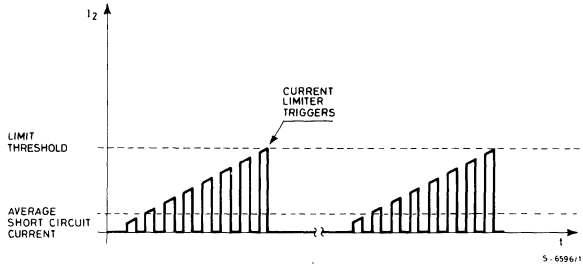


Fig. 3 - Current limiter waveforms



ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit	Fig.
SOFT START								
I_{5so}	Source current	V_6 = 0V, V_5 = 3V		100	130	160	μA	6b
I_{5si}	Sink current	V_6 = 3V, V_5 = 3V		50	70	120	μA	6b
INHIBIT								
V_{6L}	Low input voltage	V_i = 9V to 46V S1 : B S2 : B		-0.3		0.8	V	6a
V_{6H}	High input voltage	V_7 = 0V		2		5.5	V	6a
$-I_{6L}$	Input current with low input voltage	V_i = 9V to 46V	V_6 = 0.8V			10	μA	6a
$-I_{6H}$	Input current with high input voltage	V_7 = 0V S1 : B S2 : B	V_6 = 2V			3	μA	6a
ERROR AMPLIFIER								
V_{9H}	High level output volt.	V_{10} = 4.7V, I_9 = 100μA, S1 : A, S2 : A		3.5			V	6c
V_{9L}	Low level output volt.	V_{10} = 5.3V, I_9 = 100μA, S1 : A, S2 : E				0.5	V	6c
I_{9si}	Sink output current	V_{10} = 5.3V, S1 : A, S2 : B		100	150		μA	6c
$-I_{9so}$	Source output current	V_{10} = 4.7V, S1 : A, S2 : D		100	150		μA	6c
I_{10}	Input bias current	V_{10} = 5.2V S1 : B			2	10	μA	6c
		V_{10} = 6.4V, S1 : B, L296P			2	10	μA	6c
G_v	DC open loop Gain	V_9 = 1V to 3V, S1 : A, S2 : C		46	55		dB	6c
OSCILLATOR AND PWM COMPARATOR								
$-I_7$	Input bias current of PWM comparator	V_7 = 0.5V to 3.5V				5	μA	6a
$-I_{11}$	Oscillator source curr.	V_{11} = 2V, S1 : A S2 : B		5			mA	6A
RESET								
V_{12R}	Rising threshold voltage	V_i = 9V to 46V, S1 : B, S2 : B		V_{ref} -150mV	V_{ref} -100mV	V_{ref} -50mV	V	6d
V_{12F}	Falling threshold voltage			4.75	V_{ref} -150mV	V_{ref} -100mV	V	6d
V_{13D}	Delay threshold volt.	V_{12} = 5.3V, S1 : A, S2 : B		4.3	4.5	4.7	V	6d
V_{13H}	Delay threshold voltage hysteresis				100		mV	6d
V_{14S}	Output saturation volt.	I_{14} = 16mA; V_{12} = 4.7V; S1, S2 : B				0.4	V	6d
I_{12}	Input bias current	V_{12} = 0V to V_{ref}, S1 : B, S2 : B			1	3	μA	6d
$-I_{13so}$	Delay source current	V_{13} = 3V S1 : A S2 : B	V_{12} = 5.3V	70	110	140	μA	6d
I_{13si}	Delay sink current		V_{12} = 4.7V	10			mA	6d
I_{14}	Output leakage curr.	V_i = 46V, V_{12} = 5.3V, S1 : B, S2 : A				100	μA	6d

Fig. 6 - DC test circuits

Fig. 6a

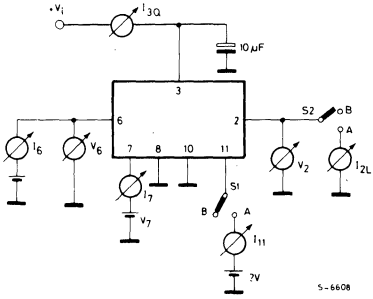


Fig. 6b

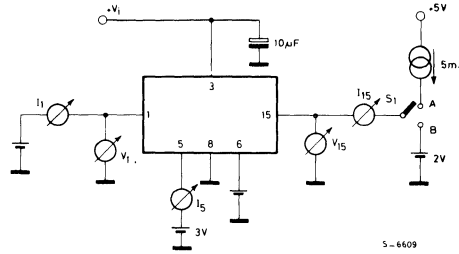


Fig. 6c

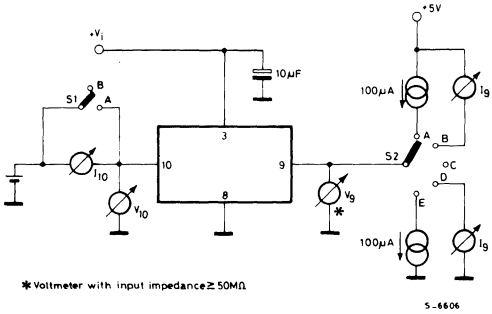
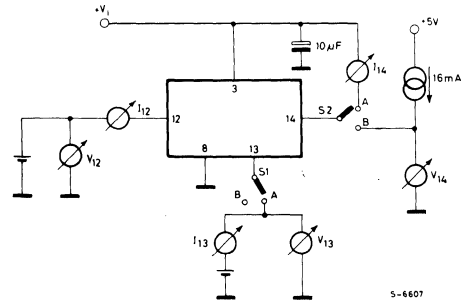


Fig. 6d



1 - Set V_{10} for $V_9 = 1V$

2 - Change V_{10} to obtain $V_9 = 3V$

3 - $G_V = \frac{\Delta V_9}{\Delta V_{10}} = \frac{2V}{\Delta V_{10}}$

Fig. 16 - Switching frequency vs. R1 (see fig. 4)

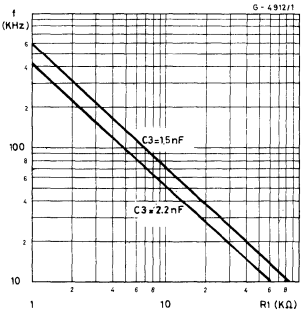


Fig. 17 - Line transient response (see fig. 4)

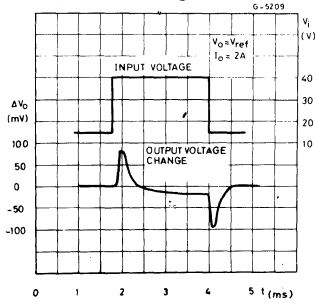


Fig. 18 - Load transient response (see fig. 4)

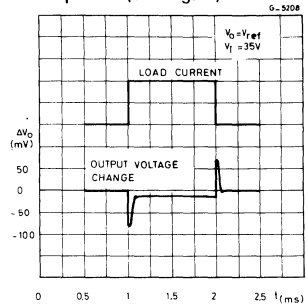


Fig. 19 - Supply voltage ripple rejection vs. frequency (see fig. 4)

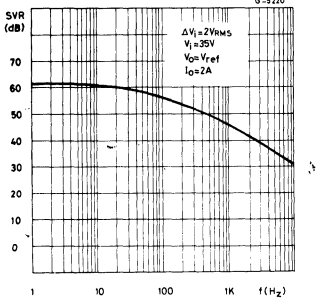


Fig. 20 - Dropout voltage between pin 3 and pin 2 vs. current at pin 2

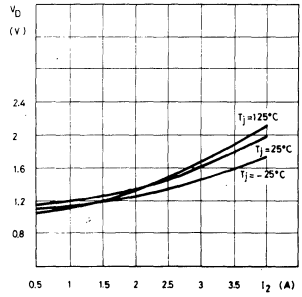


Fig. 21 - Dropout voltage between pin 3 and pin 2 vs. junction temperature

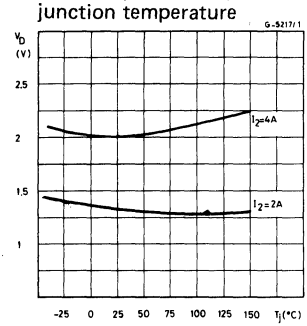


Fig. 22 - Power dissipation derating curve

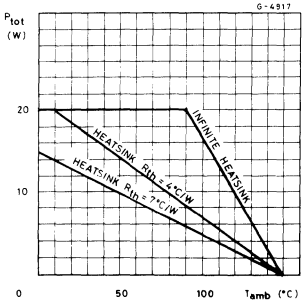


Fig. 23 - Power dissipation (device only) vs. input voltage

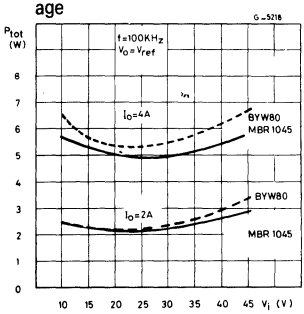
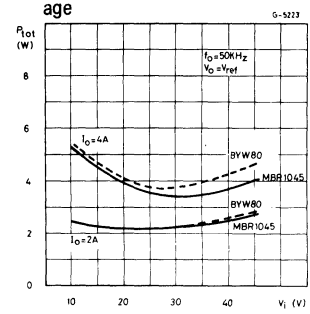
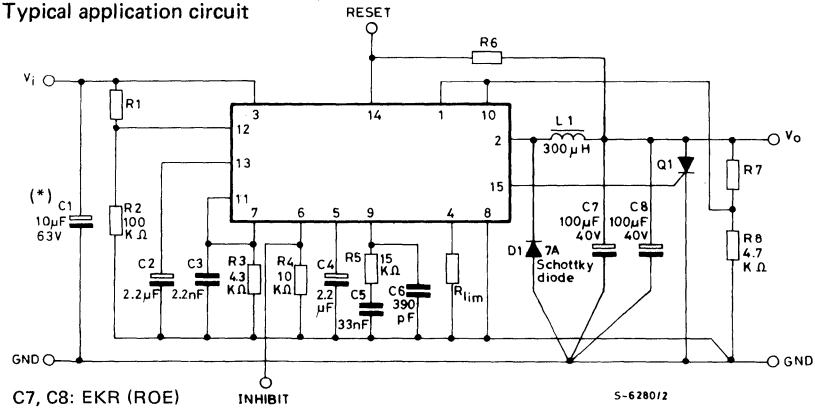


Fig. 24 - Power dissipation (device only) vs. input voltage



APPLICATION INFORMATION

Fig. 34 - Typical application circuit



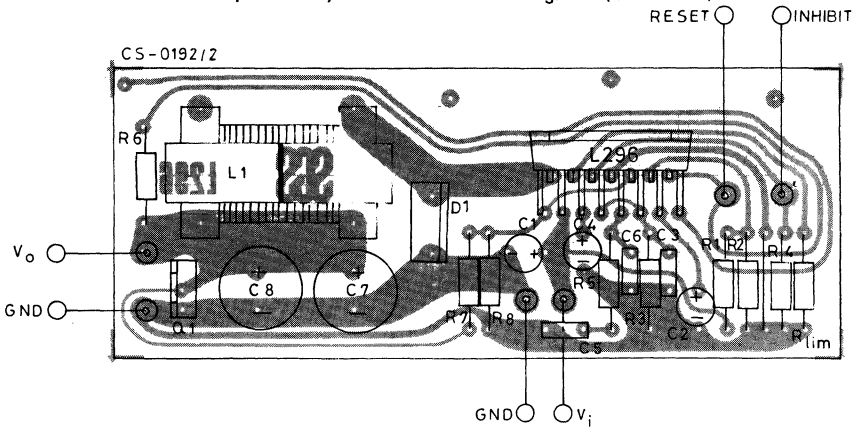
(*) Minimum value (10μF) to avoid oscillations; ripple consideration leads to typical value of 1000μF or higher
L1: 58930 - MPP COGEMA 946044; GUP 20 COGEMA 946045

SUGGESTED INDUCTOR (L1)

Core Type	No Turns	Wire Gauge	Air Gap
Magnetics 58930 - A2MPP	43	1.0 mm.	–
Thomson GUP 20x16x7	65	0.8 mm.	1 mm.
Siemens EC 35/17/10 (B6633& - G0500 - X127)	40	2 x 0.8 mm.	–
VOGT 250 μH Toroidal coil, part number 5730501800			

Resistor values for standard output voltages		
V_o	R8	R7
12V	4.7 kΩ	6.2 kΩ
15V	4.7 kΩ	9.1 kΩ
18V	4.7 kΩ	12 kΩ
24V	4.7 kΩ	18 kΩ

Fig. 35 - P.C. board and component layout of the circuit of fig. 34 (1 : 1 scale)



APPLICATION INFORMATION (continued)

Fig. 36 - A minimal 5.1V fixed regulator. Very few components are required

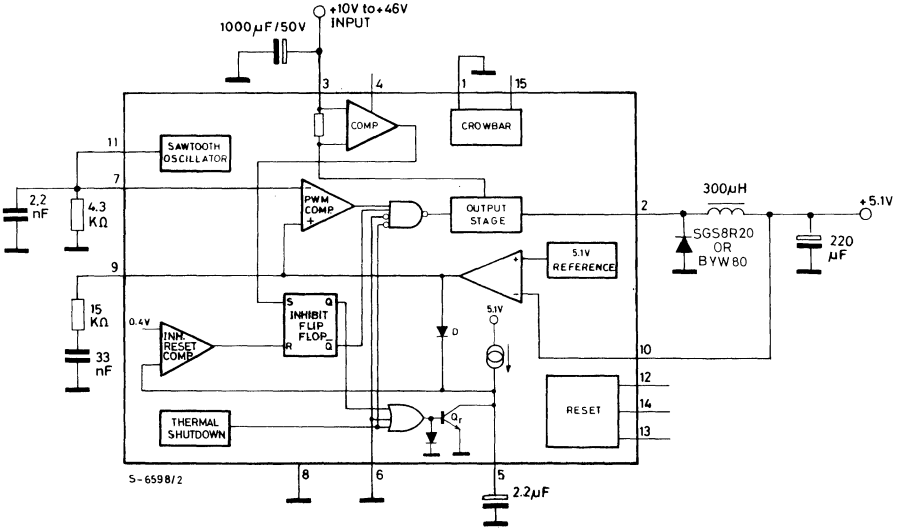
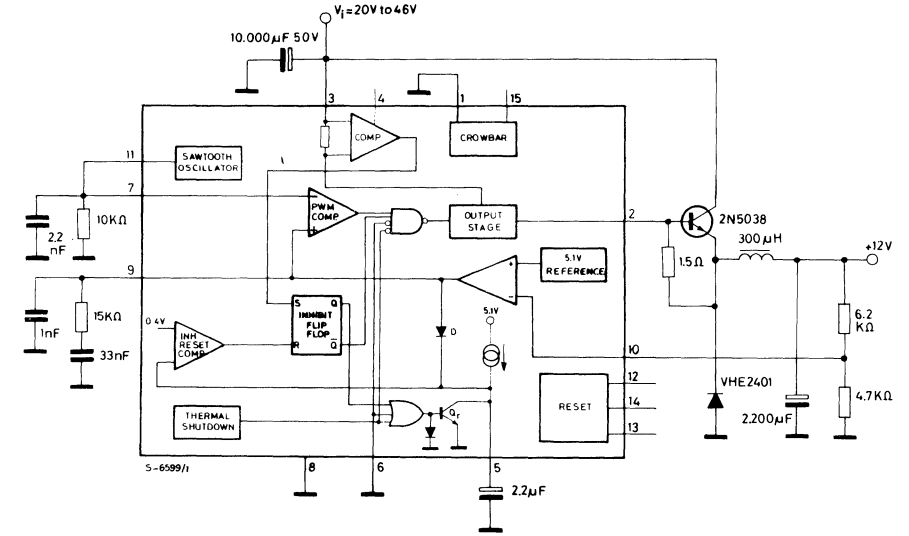


Fig. 37 - 12V/10A Power supply



APPLICATION INFORMATION (continued)

Fig. 40 - In multiple supplies several L296s can be synchronized as shown.

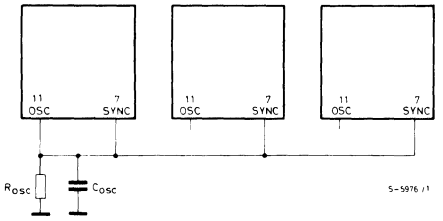


Fig. 41 - Voltage sensing for remote load

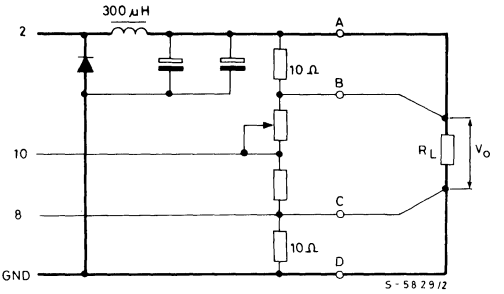
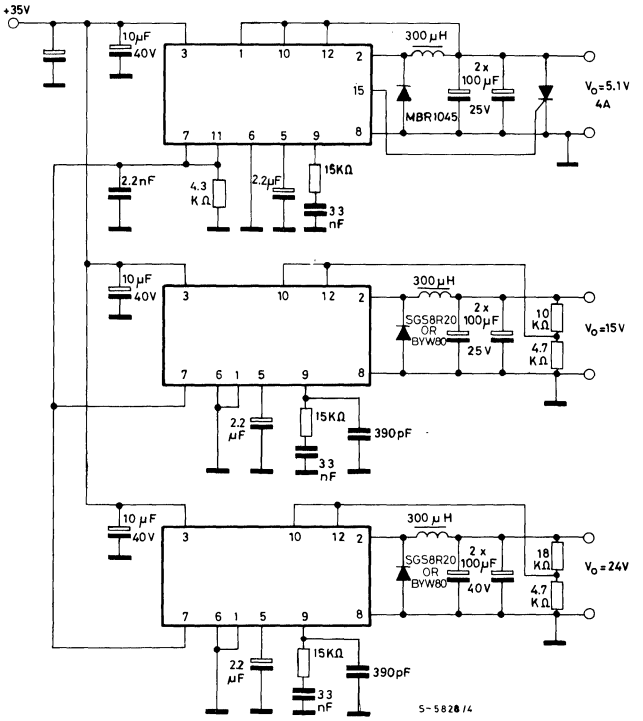


Fig. 42 - A 5.1V/15V/24V multiple supply. Note the synchronization of the three L296s.



HOW TO OBTAIN BOTH RESET AND POWER FAIL

Figure 46 illustrates how it is possible to obtain at the same time both the power fail and reset functions simply by adding one diode (D) and one resistor (R).

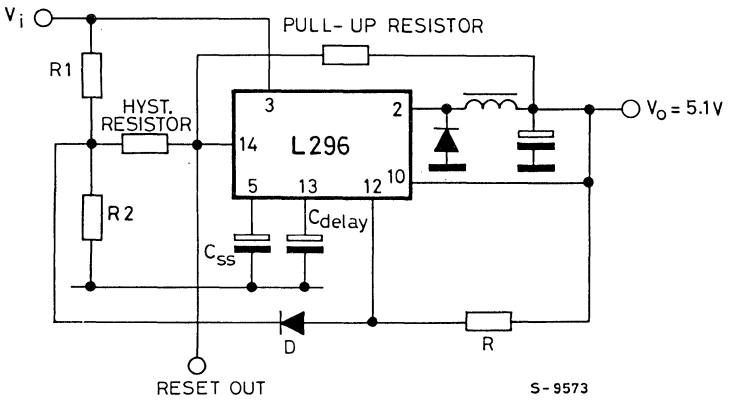
In this case the reset delay time (pin 13) can only start when the output voltage is $V_o \geqslant V_{REF}$ - 100mV and the voltage across R2 is higher than 4.5V.

With the hysteresis resistor it is possible to fix the input pin 12 hysteresis in order to increase immunity to the 100Hz ripple present on the supply voltage.

Moreover, the power fail and reset delay time are automatically locked to the soft start. Soft start and delayed reset are thus two sequential functions.

The hysteresis resistor should be in the range of about 100KΩ and the pull-up resistor of 1 to 2.2KΩ.

Fig. 46

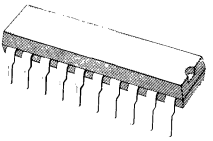


L297
L297A

STEPPER MOTOR CONTROLLERS

- NORMAL/WAVE DRIVE
- HALF/FULL STEP MODES
- CLOCKWISE/ANTICLOCKWISE DIRECTION
- SWITCHMODE LOAD CURRENT REGULATION
- PROGRAMMABLE LOAD CURRENT
- FEW EXTERNAL COMPONENTS
- RESET INPUT & HOME OUTPUT
- ENABLE INPUT
- STEP PULSE DOUBLER (L297A ONLY)

The L297 Stepper Motor Controller IC generates four phase drive signals for two phase bipolar and four phase unipolar step motors in microcomputer-controlled applications. The motor can be driven in half step, normal and wave drive modes and on-chip PWM chopper circuits permit switchmode control of the current in the windings. A feature of this device is that it requires only clock, direction and mode input signals. Since the phase are generated internally the burden on the microprocessor, and the programmer, is greatly reduced. Mounted in a 20-pin plastic package, the L297 can be used with monolithic bridge drives such as the L298N or L293E, or with discrete transistors and darlingtons. The L297A also includes a clock pulse doubler.



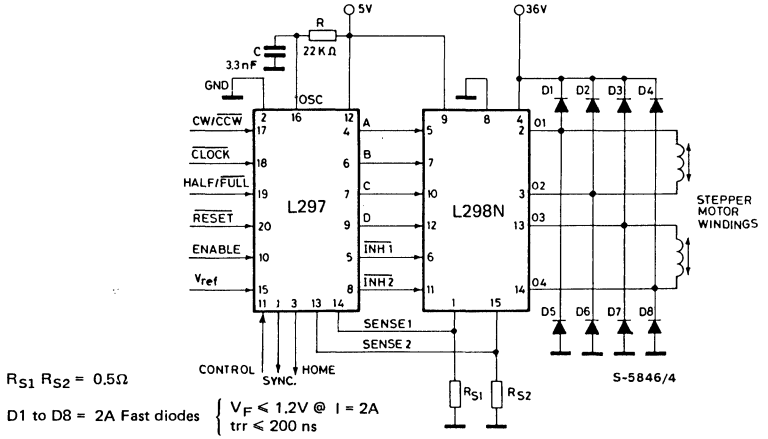
DIP-20 Plastic
(0.4)

ORDERING NUMBERS: L297 – L297A

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	10	V
V_i	Input signals	7	V
P_{tot}	Total power dissipation (T_{amb} = 70°C)	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to +150	°C

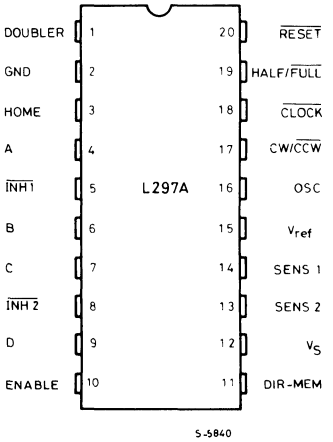
TWO PHASE BIPOLAR STEPPER MOTOR CONTROL CIRCUIT



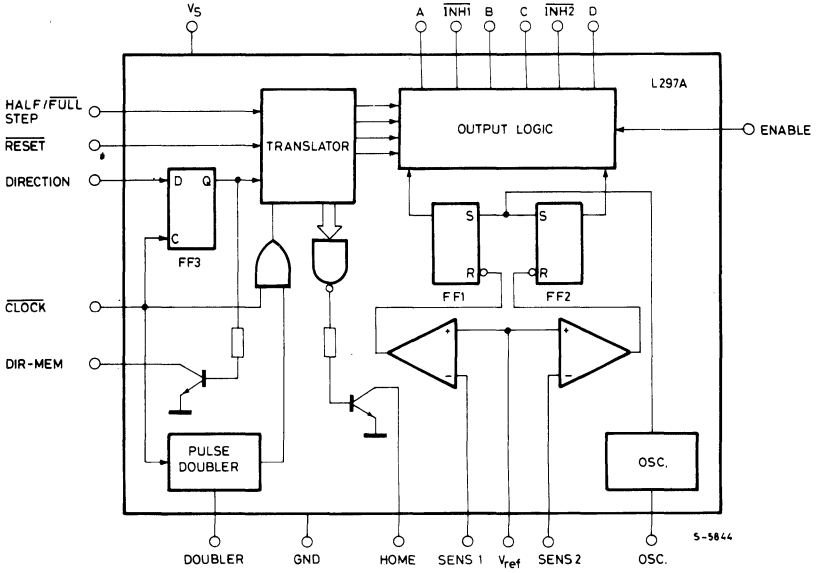
R_{S1} R_{S2} = 0.5Ω

D1 to D8 = 2A Fast diodes { $V_F \leq 1.2V$ @ I = 2A; trr ≤ 200 ns

CONNECTION DIAGRAM



BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max.	80	°C/W

PIN FUNCTIONS – L297 (continued)

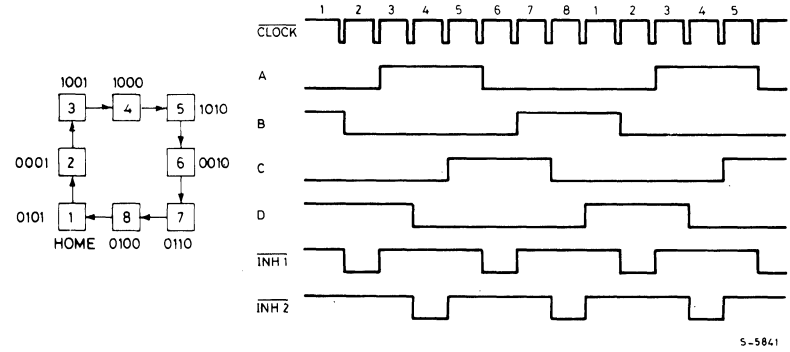
N°	NAME	FUNCTION
14	$SENS_1$	Input for load current sense voltage from power stages of phases A and B.
15	V_{ref}	Reference voltage for chopper circuit. A voltage applied to this pin determines the peak load current.
16	OSC	An RC network (R to V_{CC}, C to ground) connected to this terminal determines the chopper rate. This terminal is connected to ground on all but one device in synchronized multi - L297 configurations. $f \cong 1/0.69\ RC$, $R > 10\ k\Omega$.
17	CW/$\overline{CCW}$	Clockwise/counterclockwise direction control input. Physical direction of motor rotation also depends on connection of windings. Synchronized internally therefore direction can be changed at any time.
18	$\overline{CLOCK}$	Step clock. An active low pulse on this input advances the motor one increment. The step occurs on the rising edge of this signal.
19	HALF/$\overline{FULL}$	Half/full step select input. When high selects half step operation; when low selects full step operation. One-phase-on full step mode is obtained by selecting FULL when the L297's translator is at an even-numbered state. Two-phase-on full step mode is set by selecting FULL when the translator is at an odd numbered position. (The home position is designated state 1).
20	$\overline{RESET}$	Reset input. An active low pulse on this input restores the translator to the home position (state 1, ABCD = 0101).

MOTOR DRIVING PHASE SEQUENCES

The L297's translator generates phase sequences for normal drive, wave drive and half step modes. The state sequences and output waveforms for these three modes are shown below. In all cases the translator advances on the low to high transistion of $\overline{\text{CLOCK}}$.
Clockwise rotation is indicated; for anticlockwise rotation the sequences are simply reversed. $\overline{\text{RESET}}$ restores the translator to state 1, where ABCD = 0101.

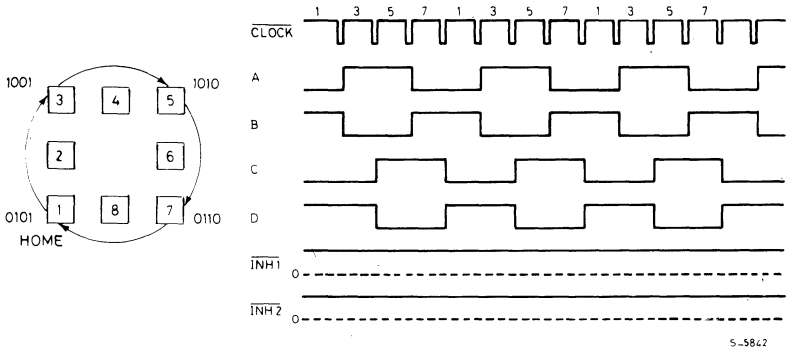
Half step mode

Half step mode is selected by a high level on the HALF/$\overline{\text{FULL}}$ input.



Normal drive mode

Normal drive mode (also called "two-phase-on" drive) is selected by a low level on the HALF/$\overline{\text{FULL}}$ input when the translator is at an odd numbered state (1, 3, 5 or 7). In this mode the $\overline{\text{INH1}}$ and $\overline{\text{INH2}}$ outputs remain high throughout.

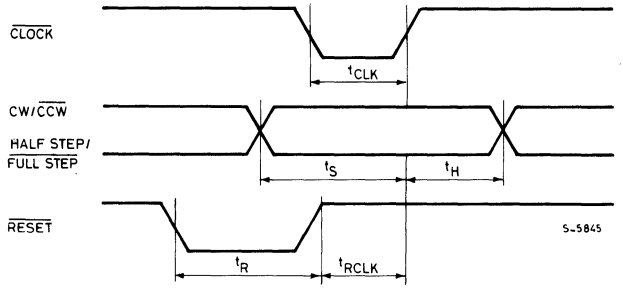


ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_o	Phase output voltage (pins 4, 6, 7, 9)	I_o = 10mA	V_{OL}			0.4	V
		I_o = 5mA	V_{OH}	3.9			V
V_{inh}	Inhibit output voltage (pins 5, 8)	I_o = 10mA	$V_{inh\ L}$			0.4	V
		I_o = 5mA	$V_{inh\ H}$	3.9			V
I_{leak}	Leakage current (pins 3, 11 *)	V_{CE}= 7V				1	μA
V_{sat}	Saturation voltage (pins 3, 11 *)	I = 5 mA				0.4	V
V_{off}	Comparators offset voltage (pins 13, 14, 15)	V_{ref} = 1V				5	mV
I_b	Comparator bias current (pins 13, 14, 15)			-100		10	μA
V_{ref}	Input reference voltage (pin 15)			0		3	V
t_{CLK}	Clock time			0.5			μs
t_S	Set up time			1			μs
t_H	Hold time			4			μs
t_R	Reset time			1			μs
t_{RCLK}	Reset to clock delay			1			μs

* L297A only.

Fig. 1



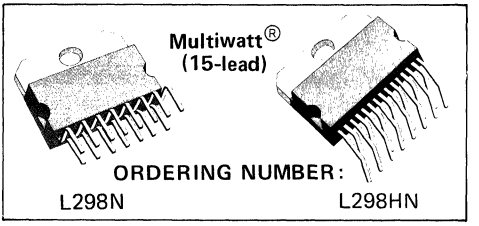
L298N

PRELIMINARY DATA

DUAL FULL-BRIDGE DRIVER

- POWER SUPPLY VOLTAGE UP TO 46V
- TOTAL DC CURRENT UP TO 4A
- LOW SATURATION VOLTAGE
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5V (HIGH NOISE IMMUNITY)

The L298N is an integrated monolithic circuit in a 15-lead Multiwatt® package. It is a high voltage, high current dual full-bridge driver designed to accept standard TTL logic levels and drive inductive loads such as relays, solenoids, DC and stepping motors. Two inhibit inputs are provided to disable the device independently of the input signals. The emitters of the lower transistors of each bridge are connected together and the corresponding external terminal can be used for the connection of an external sensing resistor. An additional supply input is provided so that the logic works at a lower voltage.

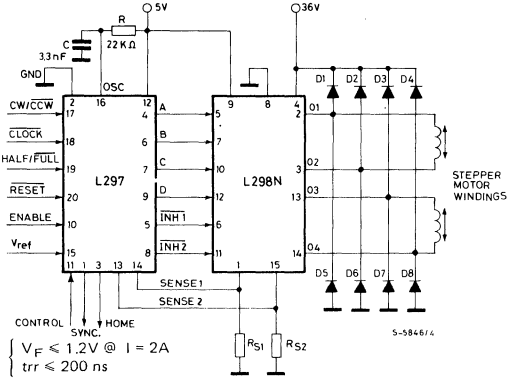


ORDERING NUMBER:
L298N L298HN

ABSOLUTE MAXIMUM RATINGS

V_s	Power supply	50	V
V_{ss}	Logic supply voltage	7	V
V_i, V_{inh}	Input and inhibit voltage	-0.3 to 7	V
I_o	Peak output current (each channel)		
	– non repetitive (t = 100 μs)	3	A
	– repetitive (80% on - 20% off; t_{on} = 10 ms)	2.5	A
	– DC operation	2	A
V_{sens}	Sensing voltage	-1 to 2.3	V
P_{tot}	Total power dissipation (T_{case} = 75°C)	25	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

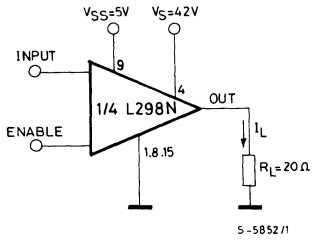
STEPPER MOTOR CONTROL CIRCUIT



R_{S1} R_{S2} = 0.5Ω

D1 to D8 = 2A Fast diodes { $V_F \leq 1.2V$ @ I = 2A; trr ≤ 200 ns

Fig. 1 - Switching times test circuits



Note: For INPUT chopper, set EN = H

Fig. 1a - Source Current Delay Times vs. Input or Enable Chopper.

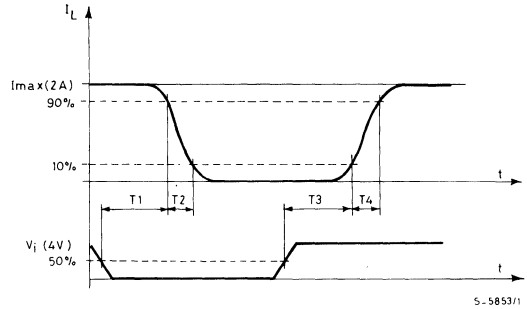
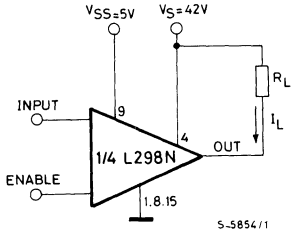
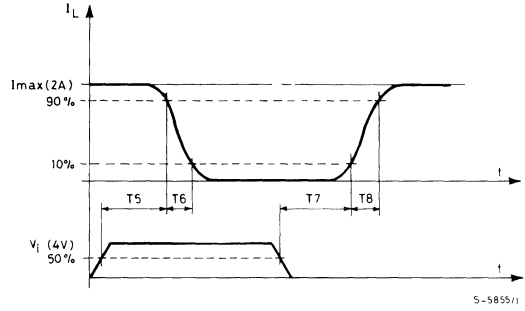


Fig. 2 - Switching times test circuits



Note: For INPUT chopper, set EN = H

Fig. 2a - Sink Current Delay Times vs. Input or Enable Chopper.

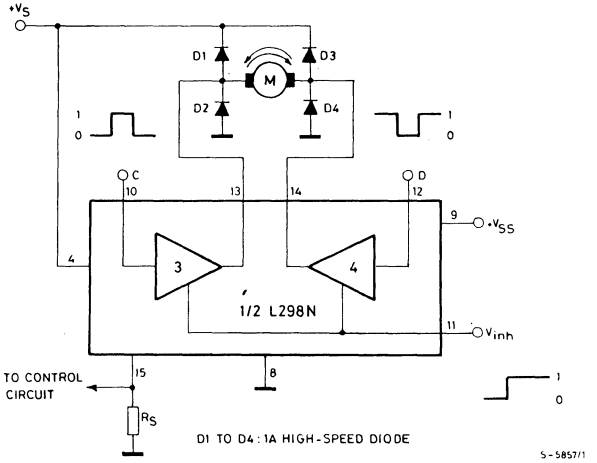


ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max	Unit
T_4 (V_i)	Source current rise time	0.1 I_L to 0.9 I_L (2)		0.35		µs
T_5 (V_i)	Sink current turn-off delay	0.5 V_i to 0.9 I_L (3)		0.7		µs
T_6 (V_i)	Sink current fall time	0.9 I_L to 0.1 I_L (3)		0.2		µs
T_7 (V_i)	Sink current turn-on delay	0.5 V_i to 0.1 I_L (3)		1.5		µs
T_8 (V_i)	Sink current rise time	0.1 I_L to 0.9 I_L (3)		0.2		µs
f_c	Commutation frequency	I_L = 2A		25	40	KHz

1) Sensing voltage can be -1V for t ⩽ 50 µsec; in steady state V_{sens} min ⩾ -0.5V.
2) See fig. 1a.
3) See fig. 2a.
* The correct sequence for power-on, is: 1. V_{ss} on with EN = L - 2. V_s on - 3. EN = H and for power-off 1. EN = L - 2. V_s off - 3. V_{ss} off

Fig. 4 - Bidirectional DC motor control



INPUTS		FUNCTION
V_{inh} = H	C = H; D = L	Turn right
	C = L; D = H	Turn left
	C = D	Fast motor stop
V_{inh} = L	C = X; D = C	Free running motor stop

L = Low H = High X = Don't care

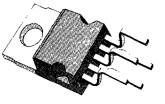
L387A

ADVANCE DATA

VERY LOW DROP 5V REGULATOR

- PRECISE OUTPUT VOLTAGE (5V ± 4%)
- VERY LOW DROPOUT VOLTAGE
- OUTPUT CURRENT IN EXCESS OF 500mA
- POWER-ON, POWER-OFF INFORMATION (RESET FUNCTION)
- HIGH NOISE IMMUNITY ON RESET DELAY CAPACITOR

The L387A is a very low drop voltage regulator in a Pentawatt® package specially designed to provide stabilized 5V supplies in consumer and industrial applications. Thanks to its very low input/output voltage drop this device is very useful in battery powered equipment, reducing consumption and prolonging battery life. A reset output makes the L387A particularly suitable for microprocessor system. This output provide a reset pulse when power is applied (after a external programmable delay) and goes low when power is removed inhibiting the microprocessor. An hysteresis on reset delay capacitor raises the immunity to the ground noise.



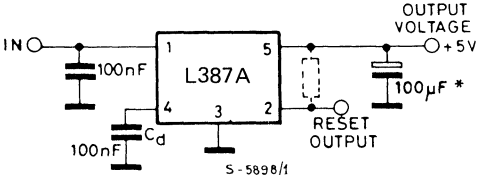
Pentawatt®

ORDERING NUMBER: L387A

ABSOLUTE MAXIMUM RATINGS

V_i	Forward input voltage	35 V
V_i	Reverse input voltage	-18 V
V_t	Positive transient voltage (t < 300ms)	60 V
V_t	Negative transient voltage (t < 100ms)	-60 V
T_{op}	Operating junction temperature	-40 to 150 °C
T_{stg}	Storage temperature	-55 to 150 °C

TEST CIRCUIT



* Min 33µF and max. ESR ⩽ 3Ω over temperature range

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, V_i = 14,4, T_j = 25°C, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	I_o = 5mA to 500mA	4.80	6	5.20	V
V_i	Operating input voltage	(*)			26	V
ΔV_o	Line regulation	V_i = 6V to 26V I_o = 5mA		5	50	mV
ΔV_o	Load regulation	I_o = 5mA to 500mA		15	60	mV
$V_i - V_o$	Dropout voltage	I_o = 500mA		0.60	0.8	V
I_q	Quiescent cuttent	I_o = 0mA I_o = 150mA I_o = 350mA I_o = 500mA V_i = 6.2V I_o = 500mA		5 20 60 100 170	15 35 100 160 180	mA
$\frac{\Delta V_o}{\Delta T}$	Temperature output t voltage drift			-0.5		mV/°C
SVR	Supply voltage rejection	I_o = 350mA f = 120Hz C_o = 100μF V_i = 12V ± 5 Vpp		60		dB
I_{sc}	Output short circuit current			0.8	1.5	A
V_R	Reset output voltage	I_R = 16mA V_o < 4.75V			0.8	V
I_R	Reset output leakage current	V_o in regulation			50	μA
t_d	Delay time for reset output	Cd = 100nF		30		ms
$V_{RT(off)}$	Reset threshold (delay charging current on)		4.75	V_o -0.15	V_o -0.04	V
I_{C4}	Charging current (current generator)	V_4 = 3V	10		30	μA
$C_{RT(on)}$	Reset threshold (low)			$V_{RT(off)}$ -10mV		V
V_4	Comparator threshold (pin 4)	Reset out = "0"	3.3		3.7	V
		Reset out = "1"	3.7		4.3	V
V_H	Hysteresis voltage			500		mV

(*) For a DC voltage 26 < V_i < 35V the device is not operating

L601 L603
L602 L604

DARLINGTON ARRAYS

- EIGHT DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 400mA PER DRIVER (500mA PEAK)
- OUTPUT VOLTAGE 90V ($V_{CE(sus)}$ = 70V)
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL / CMOS / PMOS / DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT

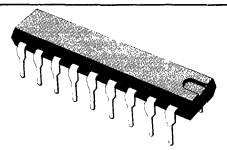
The L601, L602, L603 and L604 are high voltage, high current darlington arrays each containing eight open collector darlington pairs with common emitters. Each channel is rated at 400 mA and can withstand peak currents of 500mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

The four versions interface to all common logic families:

L601	General purpose
L602	14-25V PMOS
L603	5V TTL, CMOS
L604	6 - 15V CMOS, PMOS

These versatile devices are useful for driving a wide range of loads, including solenoids, relays DC motors, LED dispalys, filament lamps, thermal printheads and high power buffers.

The L601, L602, L603 and L604 are supplied in 18 pin plastic DIP packages with a copper leadframe to reduce thermal resistance.



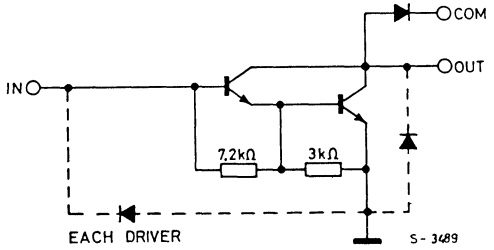
DIP-18 Plastic
(U7P2)

ORDERING NUMBERS: L601B, L603B
L602B, L604B

ABSOLUTE MAXIMUM RATINGS

V_{CEX}	Collector emitter voltage (input open)	90	V
I_C	Collector current	0.4	A
I_C	Collector peak current	0.5	A
V_i	Input voltage (for L602, L603 and L604)	30	V
I_i	Input current (for L601 only)	25	mA
P_{tot}	Total power dissipation a T_{amb} = 25°C	1.8	W
T_{op}	Operating junction temperature	-25 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

SCHEMATIC DIAGRAM (L601 – One darlington only)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_{CEX}	Output leakage current	V_{CE}= 90V			10	μA
$V_{CE(sat)}$	Collector emitter saturation voltage	I_C= 300 mA I_B= 500 μA I_C= 200 mA I_B= 350 μA I_C= 100 mA I_B= 250 μA			2 1.7 1.2	V V V
h_{FE}	DC forward current gain (L601 only)	V_{CE}= 3V I_C= 300 mA	1000			—
V_i	Minimum input voltage (ON condition)	V_{CE}= 3V I_C= 300 mA for L602 for L603 for L604			 11.5 2.5 2.5	 V V V
V_i	Maximum input voltage (OFF condition)	V_{CE}= 90V I_C= 25 μA for L601 for L602 for L603 for L604	 0.55 7 0.75 1			 V V V V
I_R	Clamp diode reverse current	V_R= 90V			50	μA
V_F	Clamp diode forward voltage	I_F= 300 mA		2	2.4	V
t_{on}	Turn-on delay	0.5 V_i to 0.5 V_o		0.4		μs
t_{off}	Turn-off delay	0.5 V_i to 0.5 V_o		0.4		μs

L702

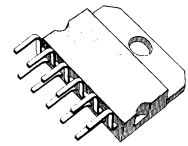
PRELIMINARY DATA

2A QUAD DARLINGTON SWITCH

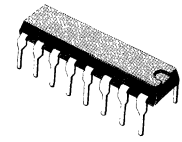
- SUSTAINING VOLTAGE: 70V
- 2A OUTPUT
- HIGH CURRENT GAIN
- IDEAL FOR DRIVING SOLENOIDS, DC MOTORS, STEPPER MOTORS, RELAYS, DISPLAYS, ETC.

The L702 is a monolithic integrated circuit for high current and high voltage switching applications it comprises four darlington transistors with common emitter and open collector suitable for current sinking applications, mounted on the new POWERDIP and Multiwatt® packages.

This circuit reduces components, sizes and costs; it can provide direct interface between low level logic and a variety of high current applications.



Multiwatt-11



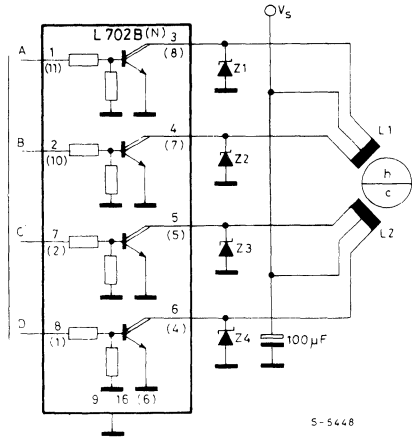
Powerdip 8 + 8
(V6P2)

ORDERING NUMBER: L702B - Powerdip
L702N - Multiwatt

ABSOLUTE MAXIMUM RATINGS

V_{CEX}	Collector-emitter voltage (input open)		90	V
V_i	Input voltage		30	V
I_C	Collector current		3	A
P_{tot}	Total power dissipation at $T_{pin\ 9\ to\ 16} \leqslant 90°C$	Powerdip	4	W
	Total power dissipation at $T_{amb} \leqslant 70°C$	Powerdip	1.1	W
	Total power dissipation at $T_{case} \leqslant 90°C$	Multiwatt	20	W
T_{stg}	Storage temperature		-55 to 150	°C
T_j	Operating junction temperature		-25 to 150	°C

Stepping motor buffer



ELECTRICAL CHARACTERISTICS (T_{case}= 25°C unless otherwise specified)

Parameter			Test conditions	Min.	Typ.	Max.	Unit
I_{CEX}	Output leakage current		V_{CE}= 90V		10	50	μA
$V_{CE\ (sust)}$	Collector emitter (°) sustaining voltage		I_C = 100 mA	70			V
$V_{CE\ (sat)}$	Collector emitter saturation voltage		I_C = 1.25A I_i = 2 mA		1.3	1.9	V
h_{FE}	DC forward current gain		I_C = 1A V_{CE}= 3V	1000	4000		
I_i	Input current		V_i = 3.75V V_i = 2.4V open collector		7 3	11 6	mA mA
V_i	Input voltage	off condition	V_{CE}= 70V $I_C \leqslant$ 0.1 mA			0.4	V
		on condition	V_{CE}= 3V $I_C \geqslant$ 1A	2.4			V
t_{on}	Turn on time		V_s = 12V		0.3		μs
t_{off}	Turn off time		R_L= 10 Ω		1		μs

(°) Pulsed: pulse duration = 300 μs, duty cycle = 1.5%.

Fig. 1 - Switching time

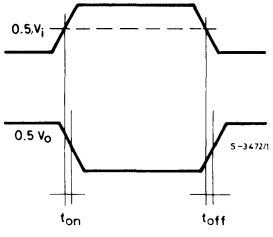


Fig. 2 - t_{on} and t_{off} test circuit

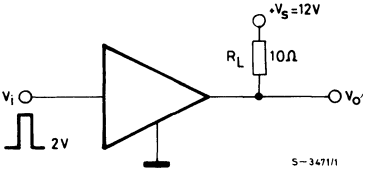
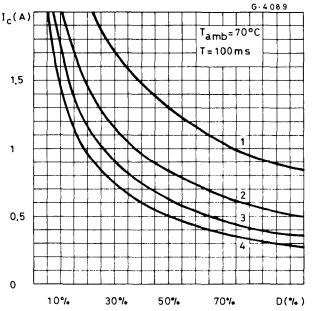


Fig. 3 - Peak collector current vs. duty cycle and number of outputs(L702B only)



L2720
L2722

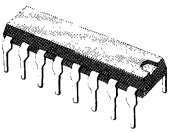
ADVANCE DATA

LOW DROP DUAL POWER OPERATIONAL AMPLIFIERS

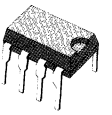
- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- LOW INPUT OFFSET VOLTAGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN

The L2720 and L2722 are monolithic integrated circuits in powerdip and minidip packages, intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies. They are particularly indicated for driving, inductive loads, as motor and finds applications in compact-disc, VCR automotive, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.



Powerdip 8 + 8



Minidip Plastic

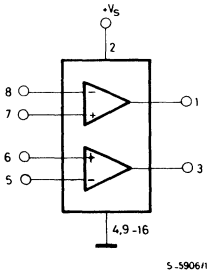
ORDERING NUMBERS:

L2720 L2722

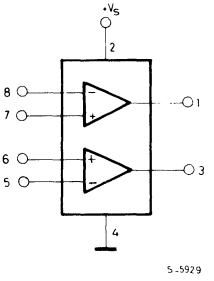
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	28	V
V_s	Peak supply voltage (50ms)	50	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at T_{amb} = 80°C **(L2720)**, T_{amb} = 50°C **(L2722)**	1	W
	T_{case} = 75°C **(L2720)**	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

BLOCK DIAGRAMS



L2720



L2722

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

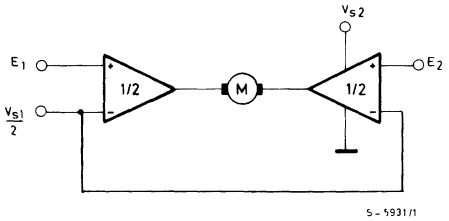
Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Single supply voltage			4		28	V
V_s	Split supply voltage			± 2		± 14	V
I_s	Quiescent drain current	$V_o = \frac{V_s}{2}$	V_s = 24V		10	15	mA
			V_s = 8V		9	15	mA
I_b	Input bias current				0.2	1	μA
V_{os}	Input offset voltage					15	mV
I_{os}	Input offset current				10	50	nA
SR	Slew rate				2		V/μs
B	Gain-bandwidth product				1.2		MHz
R_i	Input resistance			500			KΩ
G_v	O.L. voltage gain	f = 100Hz		70	80		dB
		f = 1KHz			60		dB
e_N	Input noise voltage	B = 22Hz to 22KHz			10		μV
I_N	Input noise current				200		pA
CMR	Common Mode rejection	f = 1KHz		66	84		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ±12V V_s = ± 6V	54	70 75 81		dB dB dB
$V_{DROP\ (HIGH)}$		V_s = ±2.5V to ±12V	I_p = 100mA		0.7		V
			I_p = 500mA		1.0	1.5	V
$V_{DROP\ (LOW)}$			I_p = 100mA		0.3		V
			I_p = 500mA		0.5	1.0	V
C_s	Channel separation	f = 1KHz; R_L = 10Ω; G_v = 30dB	V_s = 24V V_s = ± 6V		60 60		dB dB
T_{sd}	Thermal shutdown junction temperature				145		°C

APPLICATION SUGGESTION

In order to avoid possible instability occurring into final stage the usual suggestions for the linear power stages are useful, as for instance:

- layout accuracy;
- A 100nF capacitor corrected between supply pins and ground;
- boucherot cell (0.1 to 0.2μF + 1Ω series) between outputs and ground or across the load.

Fig. 8 - Bidirectional DC motor control with μP compatible inputs



V_{S1} = logic supply voltage

Must be $V_{S2} > V_{S1}$

E1, E2 = logic inputs

Fig. 9 - Servocontrol for compact-disc

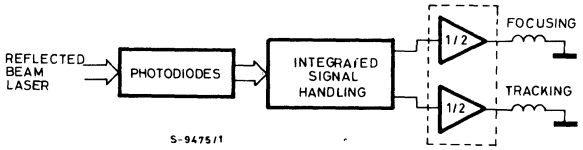


Fig. 10 - Compact-disc motor driver (1/2 section)

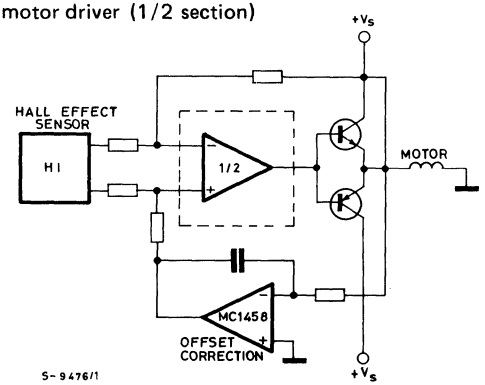
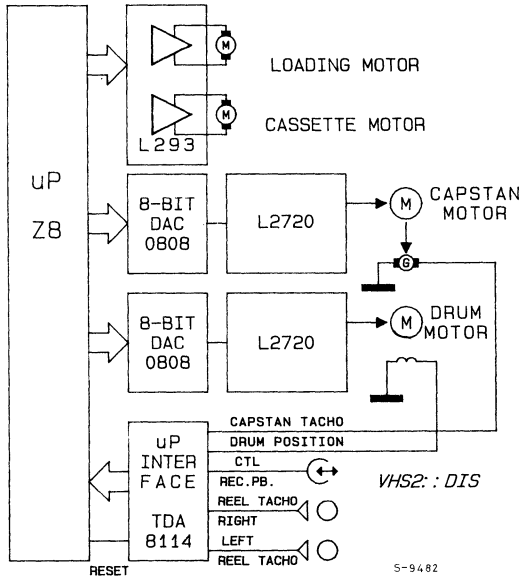


Fig. 14 - VHS-VCR Motor control circuit



L3654S

PRELIMINARY DATA

PRINTER SOLENOID DRIVER

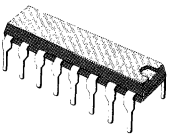
The L3654S is a printer solenoid driver containing ten open-collector driver outputs and a ten-bit serial-in, parallel-out register.

Data is clocked into the shift register serially and transferred to the open-collector outputs by an enable input. Serial input data is loaded by the rising edge of the clock. A serial output from the tenth bit is provided which changes at the falling edge of the clock. This output is not controlled by the enable input and remains active at all time.

The L3654S is pin to pin compatible with the standard L3654, but can work with V_s down to 4.75V.

Each output is rated at 250mA (sink) and is clamped to ground internally at 50V to dissipate stored energy in inductive loads.

The L3654S is supplied in a 16 lead dual in-line plastic package, and its main fields of application comprise thermal printers, cash registers and printing pocket calculators.



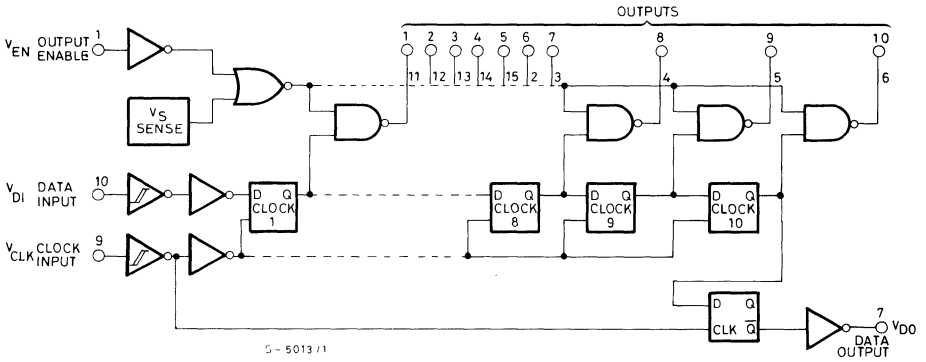
DIP-16 Plastic
(0.25)

ORDERING NUMBER: L3654S

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	9.5	V
V_i	Input voltage	9.5	V
V_E	External supply voltage	45	V
I_o	Output current (single output)	0.4	A
I_g	Ground current	4.0	A
P_{tot}	Total power dissipation (T_{amb} = 70°C)	1	W
T_{stg}, T_j	Storage and junction temperature	-65 to 150	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS ($V_s = 5V$, $V_E = 30V$, $T_{amb} = 0°$ to $70°C$, unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			4.75		9.5	V
I_S	Supply current	$T_{amb} = 25°C$	$V_{EN} = 0V$; $V_{DO} = 0V$		27	40	mA
		$V_s = 9.5V$	$V_{EN} = 2.6V$ $I_o = 250$ mA (each bit)		55	70	mA
V_E	External operating supply voltage					40	V
I_{leak}	Output leakage current (each output)	$V_E = 40V$	$V_{EN} = 0V$			1	mA
V_Z	Internal clamp voltage	$I_Z = 0.3A$ *	$V_{EN} = 0V$	45	50	65	V
$V_{CE\ sat}$	Output saturation voltage	$I_o = 250$ mA	$V_{EN} = 2.6V$			1.6	V
V_{DI} V_{CLK} V_{EN}	Input logic levels (pins 1, 9, 10)	Low State (L)				0.8	V
		High state (H)		2.6			
I_{DI}	Data input current	$V_{DI} = 2.6V$	$T_{amb} = 70°C$	0.3	0.57		mA
			$T_{amb} = 0°C$		0.57	0.75	
		$V_{DI} = 1V$	$T_{amb} = 70°C$		220		μA
I_{CLK}	Clock input current	$V_{CLK} = 2.6V$	$T_{amb} = 70°C$	0.2	0.33		mA
			$T_{amb} = 0°C$		0.33	0.5	
		$V_{CLK} = 1V$	$T_{amb} = 70°C$		125		μA
I_{EN}	Enable input current	$V_{EN} = 2.6V$	$T_{amb} = 70°C$	0.2	0.33		mA
			$T_{amb} = 0°C$		0.33	0.5	
		$V_{EN} = 1V$	$T_{amb} = 70°C$		125		μA
R_{IN}	Input pull-down resistance Clock input	$T_{amb} = 25°C$	$V_{CLK} < V_s$		8		KΩ
	Enable input	$T_{amb} = 25°C$	$V_{EN} < V_s$		8		
	Data input	$T_{amb} = 25°C$	$V_{DI} < V_s$		4.5		
V_{DO}	Output logic levels (pin 7)	Low state (L) $V_{DI} = 0V$	I_{DO}(pin 7) = 0		0.01	0.5	V
		High state (H) $V_{DI} = 2.6V$ I_{DO} (pin 7) = −0.75 mA		2.6	3.4		V
R_{DO}	Output pull-down resistance (pin 7)	$V_{DI} = 0V$	$V_{DO} = 1V$		14		KΩ

* Pulsed: pulse duration = 300μs, duty cycle = 2%

L4901

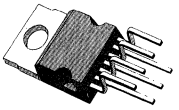
PRELIMINARY DATA

DUAL 5V REGULATOR WITH RESET

- OUTPUT CURRENTS: I_{01} = 300mA
  I_{02} = 400mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- LOW QUIESCENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4901 is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.



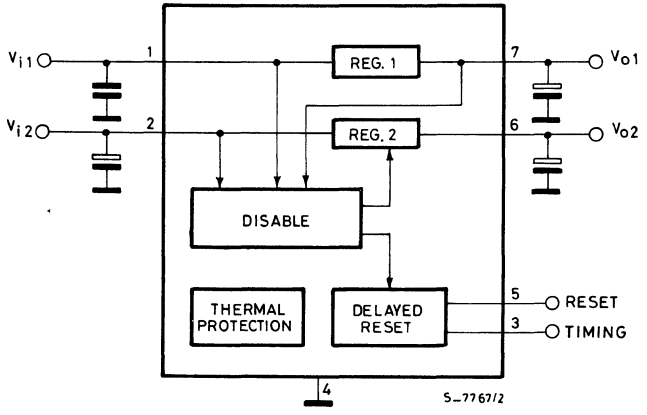
Heptawatt

ORDERING NUMBER: L4901

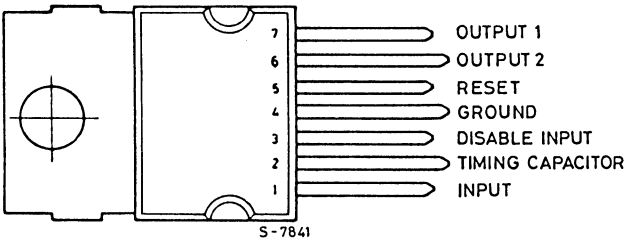
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
	DC operating input voltage	20	V
	Transient input overvoltage (t = 40ms)	60	V
I_o	Output current	internally limited	
T_j	Storage and junction temperature	-40 to 150	°C

BLOCK DIAGRAM



CONNECTION DIAGRAM
(Top view)



PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 300mA regulator input.
2	INPUT 2	400mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 5μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
5	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{5\mu A} \right)$; t_{RD} (ms) = C_t (nF)
6	OUTPUT 2	5V - 400mA regulator output. Enabled if $V_O 1 > V_{RT}$ and $V_{IN2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
7	OUTPUT 1	5V - 300mA regulator output with low leakage (in switch-OFF condition).

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis			50	160	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	6	10	14	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 140°C	-0.8	0.3	+0.8	mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 140°C	-0.8	0.3	+0.8	mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 100mA	54	84		dB
SVR2	Supply voltage rejection		50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4901 makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:

– an input overvoltage
– an overload on the output 1 ($V_{01} < V_{RT}$);
– a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.
An overload on output 2 does not switch Reg. 2 ($V_{02} - V_R = V_{CE\,sat}$; $I_{02} = I_{SC2}$) and does not influence Reg. 1.

The V_{01} output features:

– 5V internal reference without voltage divider between the output and the error comparator;
– very low drop series regulator element utilizing current mirrors;

permit high output impedance and then very low leakage current error even in power down condition.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery without a

APPLICATION SUGGESTION (continued)

Fig. 2

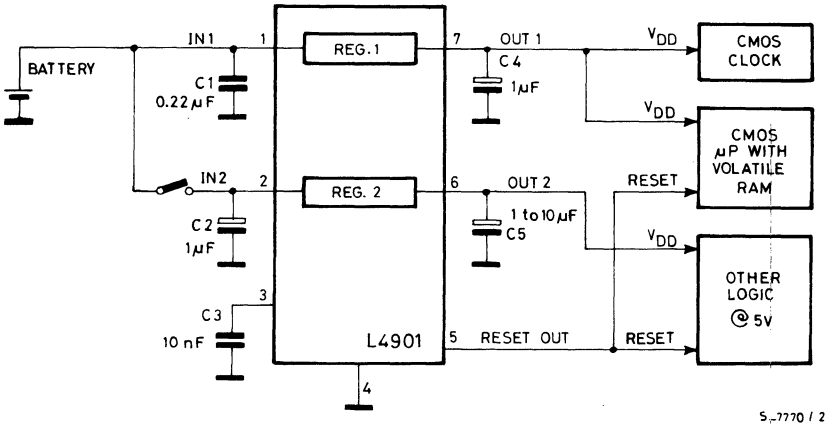
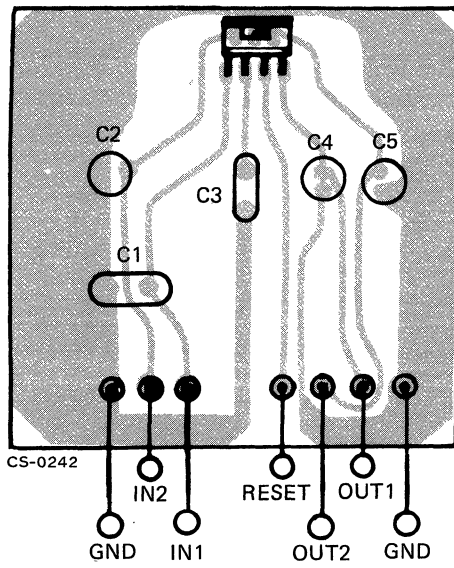


Fig. 3 - P.C. board component layout of fig. 2 (1 : 1 scale)



APPLICATION SUGGESTION (continued)

Fig. 6

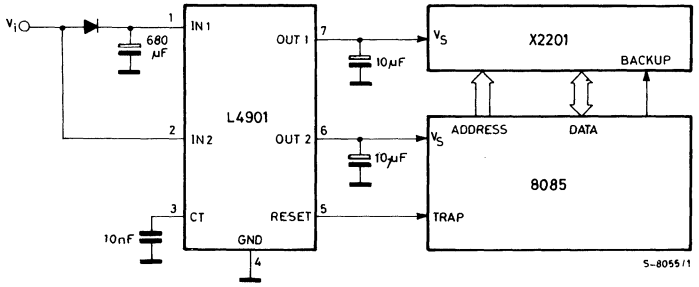


Fig. 7 - Quiescent current (Reg. 1) vs. output current

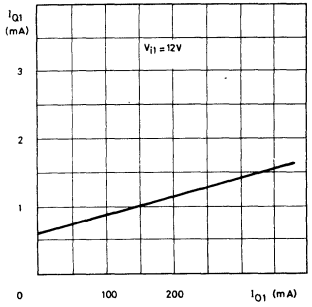


Fig. 8 - Quiescent current (Reg. 1) vs. input voltage

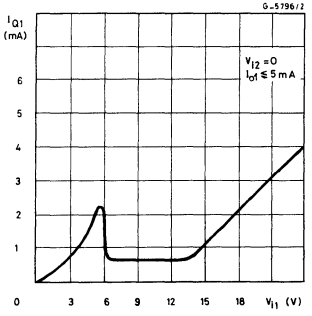


Fig. 9 - Total quiescent current vs. input voltage

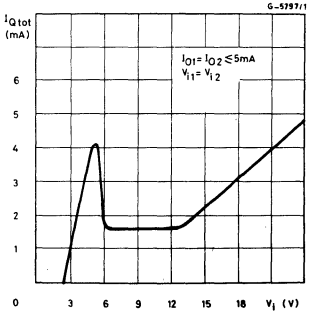


Fig. 10 - Regulator 1 output current and short circuit current vs. input voltage

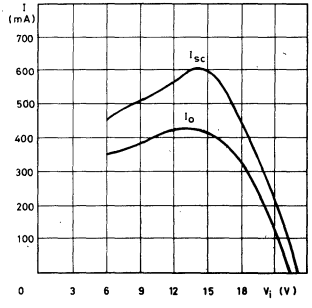


Fig. 11 - Regulator 2 output current and short circuit current vs. input voltage

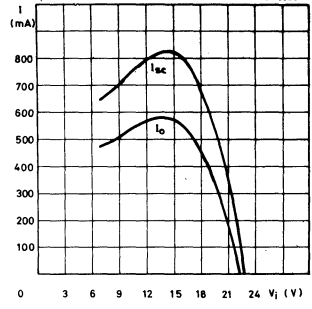
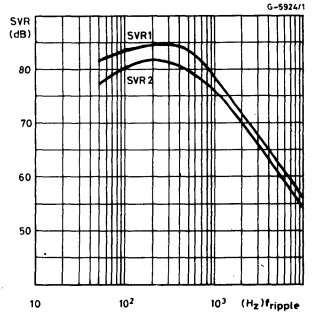


Fig. 12 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



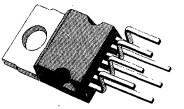
L4902

PRELIMINARY DATA

DUAL 5V REGULATOR WITH RESET AND DISABLE FUNCTIONS

- OUTPUT CURRENTS: I_{o1} = 300mA
  I_{o2} = 400mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- OUTPUT 2 DISABLE LOGICAL INPUT
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- RESET OUTPUT HIGH
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4902 is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.
Reset and data save functions and remote switch on/off control can be realized.



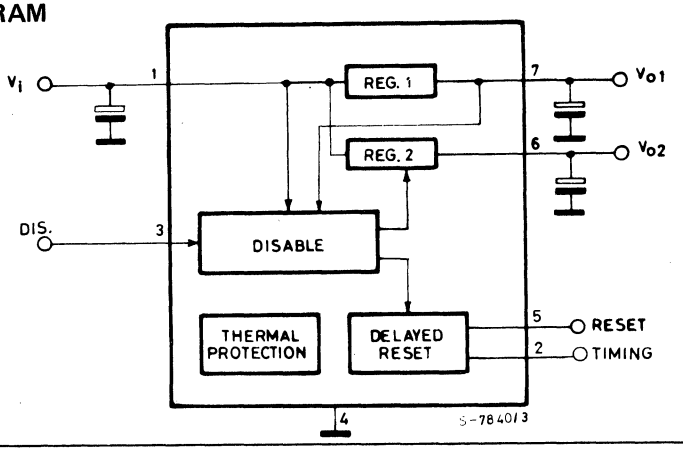
Heptawatt

ORDERING NUMBER: L4902

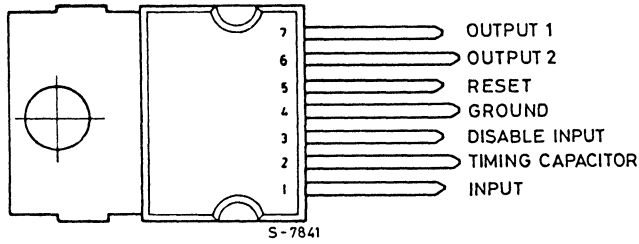
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
	DC operating input voltage	20	V
	Transient input overvoltage (t = 40ms)	60	V
I_o	Output current	internally limited	
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

BLOCK DIAGRAM



CONNECTION DIAGRAM
(Top view)



PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Regulators common input.
2	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 5μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
3	V_{02} DISABLE INPUT	A high level ($> V_{DT}$) disable output Reg. 2.
4	GND	Common ground.
5	RESET OUTPUT	When pin 2 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{5\mu A}\right)$; t_{RD} (ms) = C_t (nF).
6	OUTPUT 2	5V - 400mA regulator output. Enabled if $V_O 1 > V_{RT}$. DISABLE INPUT $< V_{DT}$ and $V_{IN} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
7	OUTPUT 1	5V - 300mA. Low leakage (in switch-OFF condition) output.

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	6	10	14	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
V_{DT}	V_{02} disable threshold voltage			1.25	2.4	V
I_D	V_{02} disable input current	$V_D \leq 0.4V$ $V_D \geq 2.4V$		-100 -2		μA μA
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 140°C$	-0.8	0.3	0.8	mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 140°C$	-0.8	0.3	0.8	mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R=0.5V I_o = 100mA	54	84		dB
SVR2	Supply voltage rejection		50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4902 makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with common inputs plus a reset output for the data save function and a Reg. 2 output disable.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:
- a high level ($> V_{DT}$) is applied on pin 3;
- an input overvoltage;
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.
An overload on output 2 does not switch Reg. 2 ($V_{02} - V_R = V_{CE\,sat}$; $I_{02} = I_{SC2}$) and does not influence Reg. 1.

The V_{01} output features:
- 5V internal reference without voltage divider between the output and the error comparator
- very low drop series regulator element utilizing current mirrors

permit high output impedance and then very low leakage current error in power down condition.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery without a separation diode.

APPLICATION SUGGESTION (continued)

Fig. 2

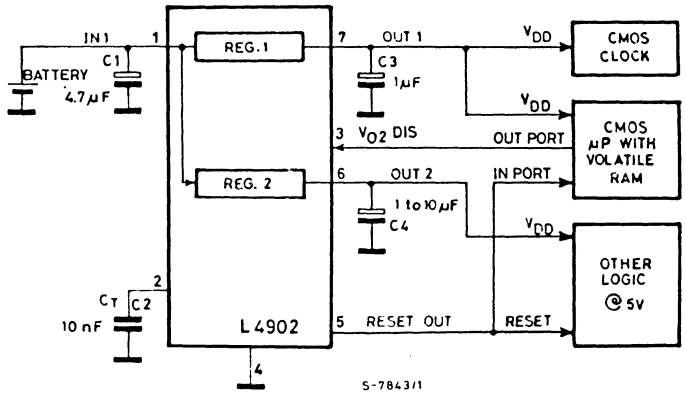
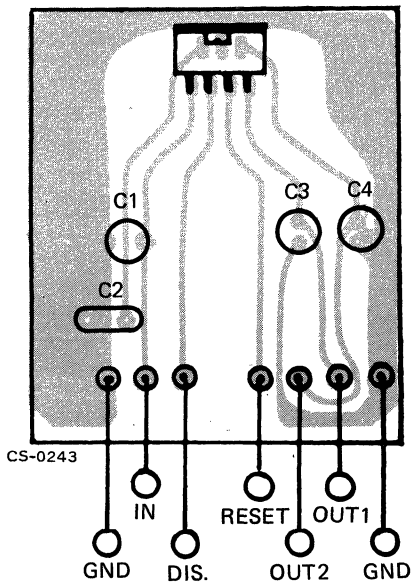


Fig. 3 - P.C. board and component layout of the circuit of Fig. 2 (1 : 1 scale)



APPLICATION SUGGESTION (continued)

Fig. 6 - Quiescent current vs. output current

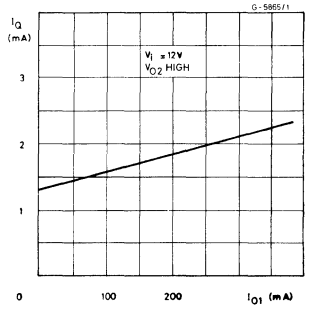


Fig. 7 - Quiescent current vs. input voltage

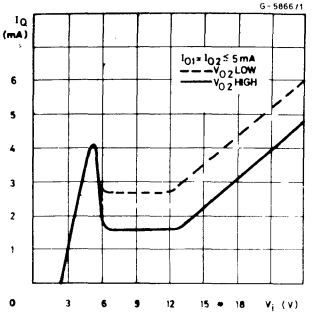


Fig. 8 - Regulator 1 output current and short circuit current vs. input voltage

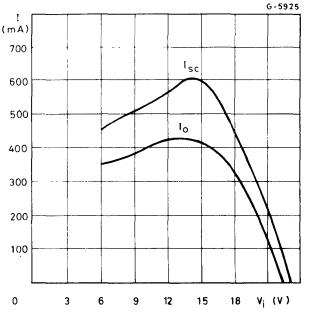


Fig. 9 - Regulator 2 output current and short circuit current vs. input voltage

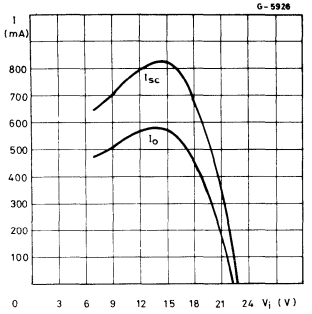
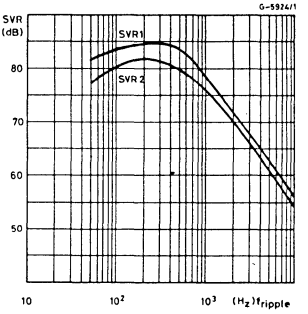


Fig. 10 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



L4903

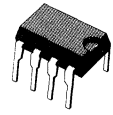
ADVANCE DATA

DUAL 5V REGULATOR WITH RESET AND DISABLE FUNCTIONS

- OUTPUT CURRENTS: I_{o1} = 50mA, I_{o2} = 100mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- OUTPUT 2 DISABLE LOGICAL INPUT
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT LOW
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4903 is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset, data save functions and remote switch on/off control can be realized.



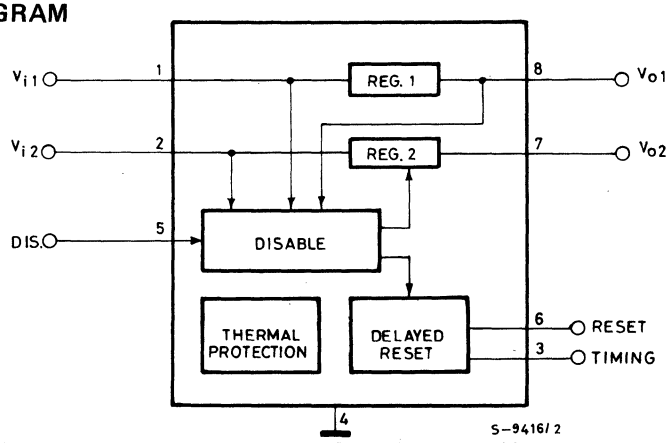
Minidip Plastic

ORDERING NUMBER: L4903

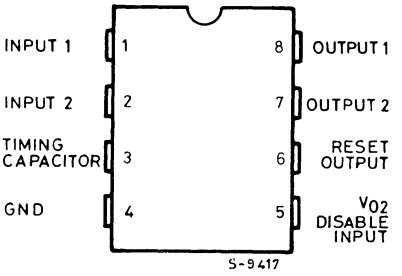
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
V_{IN}	DC operating input voltage	20	V
V_t	Transient input overvoltage (t = 40ms)	60	V
P_{tot}	Power dissipation at T_{amb} = 50°C	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

BLOCK DIAGRAM



CONNECTION DIAGRAM
(Top view)



PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 50mA regulator input.
2	INPUT 2	100mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 5μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
5	V_{02} DISABLE INPUT	A high level ($> V_{DT}$) disable output Reg. 2.
6	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched low. Therefore $t_{RD} = C_t \left(\frac{5V}{5\mu A}\right)$; t_{RD} (ms) = C_t (nF).
7	OUTPUT 2	5V - 100mA regulator output. Enabled if V_O 1 $> V_{RT}$. DISABLE INPUT $< V_{DT}$ and $V_{IN\,2} > V_{IT}$. If Reg. 2 is switched OFF the C_{02} capacitor is discharged.
8	OUTPUT 1	5V - 50mA regulator output with low leakage in switch-OFF condition.

THERMAL DATA

$R_{th\,j\text{-}pin}$	Thermal resistance junction-pin 4	max	70	°C/W
$R_{th\,j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.4	4.7	V_{02}-0.2	V
V_{RTH}	Reset threshold hysteresis			50	160	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	6	10	14	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
V_{DT}	V_{02} disable threshold voltage			1.25	2.4	V
I_D	V_{02} disable input current	$V_D \leq 0.4V$ $V_D \geq 2.4V$		-100 -2		μA μA
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 140°C$	-0.8	0.3	0.8	mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 140°C$	-0.8	0.3	0.8	mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 50mA	54	84		dB
SVR2	Supply voltage rejection	I_o = 100mA	50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current conditions.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4903 makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with separate inputs plus a reset output for the data save function and Reg. 2 output disable.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) goes low after a programmable time T_{RD} (timing capacitor).

V_{02} is switched at low level and V_R at high level when one of the following conditions occurs:

- a high level ($> V_{DT}$) is applied on pin 5;
- an input overvoltage;
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2 ($V_{02} - V_R = V_{CE\,sat}$; $I_{02} = I_{SC2}$) and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator
- very low drop series regulator element utilizing current mirrors

permit high output impedance and then very low leakage current error in power down conditions.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery without a separation diode.

Fig. 3 - Quiescent current (Reg. 1) vs. output current

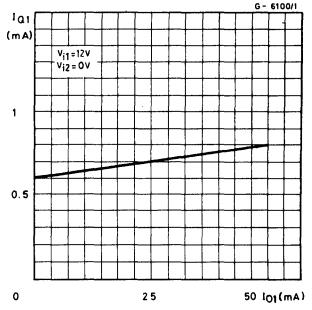


Fig. 4 - Quiescent current (Reg. 1) vs. input voltage

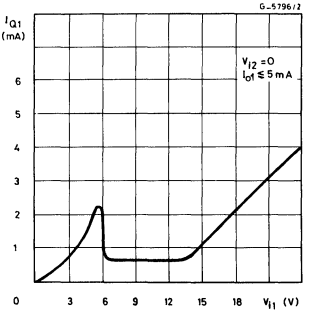


Fig. 5 - Total quiescent current vs. input voltage

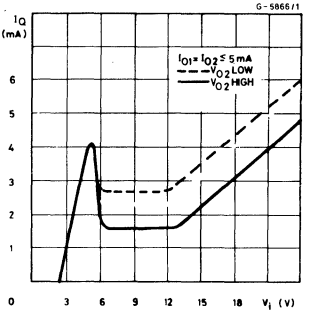
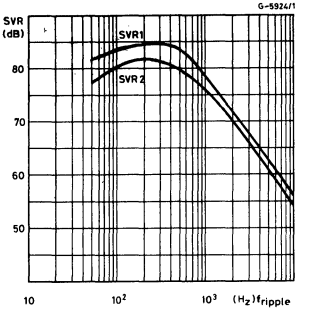


Fig. 6 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



L4904

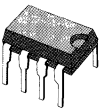
ADVANCE DATA

DUAL 5V REGULATOR WITH RESET

- OUTPUT CURRENTS: I_{o1} = 50mA, I_{o2} = 100mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- LOW QUIESCENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4904 is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.



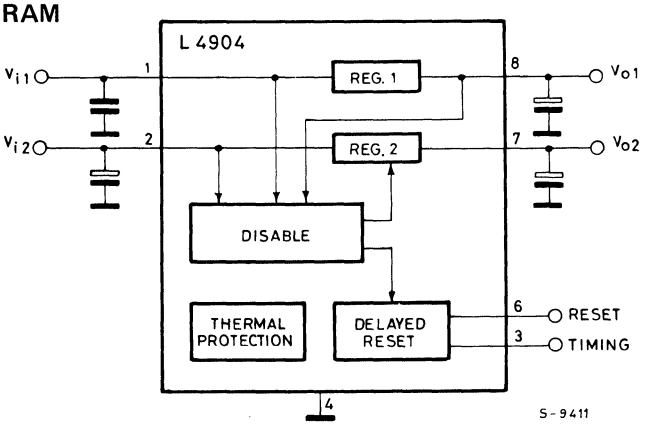
Minidip Plastic

ORDERING NUMBER: L4904

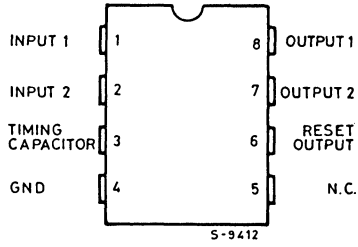
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
	DC operating input voltage	20	V
	Transient input overvoltage (t = 40ms)	60	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation at T_{amb} = 50°C	1	W
T_j	Storage and junction temperature	-40 to 150	°C

BLOCK DIAGRAM



CONNECTION DIAGRAM
(Top view)



PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 50mA regulator input.
2	INPUT 2	100mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 5μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
6	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{5\mu A}\right)$; t_{RD} (ms) $= C_t$ (nF).
7	OUTPUT 2	5V - 100mA regulator output. Enabled if $V_O 1 > V_{RT}$ and $V_{IN\,2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
8	OUTPUT 1	5V - 50mA regulator output with low leakage in switch-OFF condition.

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis			50	160	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	6	10	14	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 140°C	-0.8	0.3	+0.8	mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 140°C	-0.8	0.3	+0.8	mV/°C
SVR1	Supply voltage rejection	f = 100Hz, V_R = 0.5V, I_o = 50mA	54	84		dB
SVR2	Supply voltage rejection	f = 100Hz, V_R = 0.5V, I_o = 100mA	50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4904 makes it very easy to supply such equipments; it provides two voltage regulators (booth 5V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:

- an input overvoltage
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2 ($V_{02} - V_R = V_{CE\,sat}$; $I_{02} = I_{SC2}$) and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator;
- very low drop series regulator element utilizing current mirrors;

permit high output impedance and then very low leakage current error in power down condition.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery without a separation diode. The V_{01} regulator also features

APPLICATION SUGGESTIONS (continued)

Application Circuits of a Microprocessor system (Fig. 2) or with data save battery (Fig. 3). The reset output provide delayed rising front at the turn-off of the regulator 2.

Fig. 2

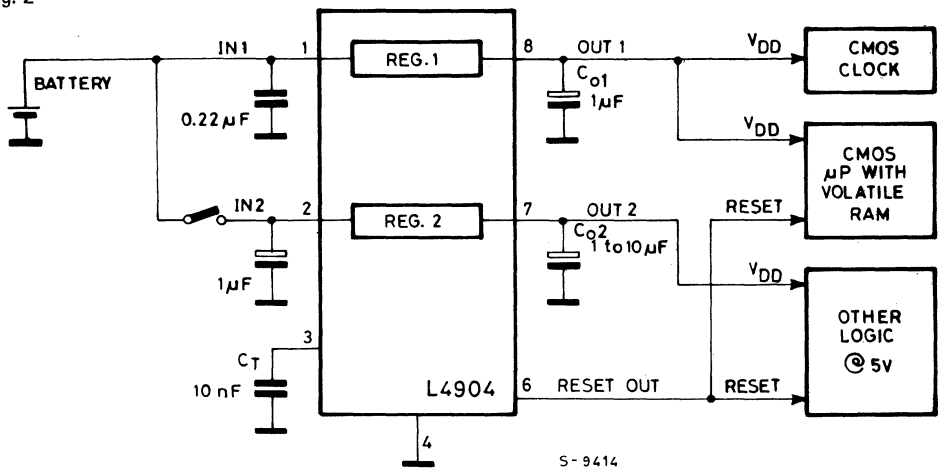
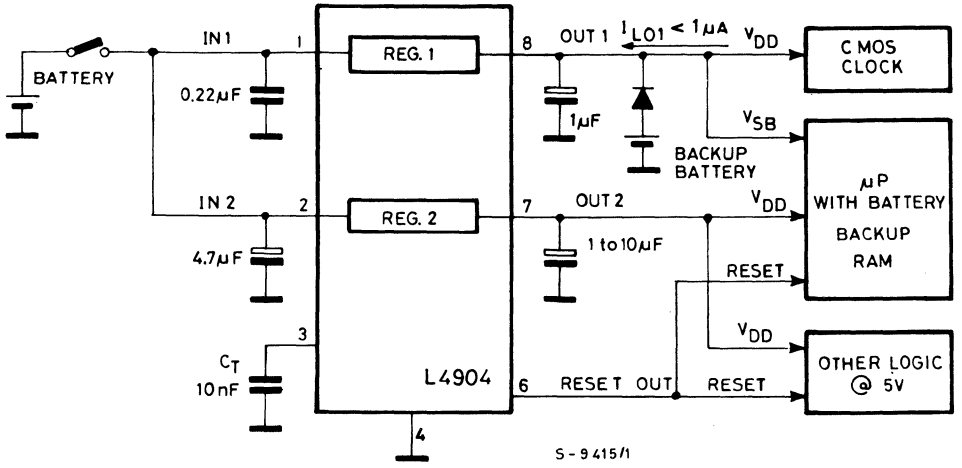


Fig. 3



L4920
L4921

PRELIMINARY DATA

VERY LOW DROP ADJUSTABLE REGULATOR

- VERY LOW DROP VOLTAGE
- ADJUSTABLE OUTPUT VOLTAGES FROM 1.25V TO 20V
- 400mA OUTPUT CURRENT
- LOW QUIESCENT CURRENT
- OVERVOLTAGE AND REVERSE VOLTAGE PROTECTION
- +60/-60 TRANSIENT PEAK VOLTAGE
- SHORT CIRCUIT PROTECTION WITH FOLDBACK CHARACTERISTICS
- THERMAL SHUT-DOWN

The L4920 and L4921 are adjustable voltage regulators with a very low voltage drop (0.4V typ. at 0.4A), low quiescent current and comprehensive on-chip protection.

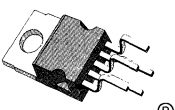
These devices are protected against load dump transients of ± 60V, input overvoltage, polarity reversal and over heating.

A foldback current limiter protects against load short circuits.

The output voltage is adjustable through an external divider from 1.25V to 20V. The minimum operating input voltage is 5.2V.

These regulators are designed for automotive, industrial and consumer applications where low consumption is particularly important.

In battery backup and standby applications the low consumption of these devices extends battery life.



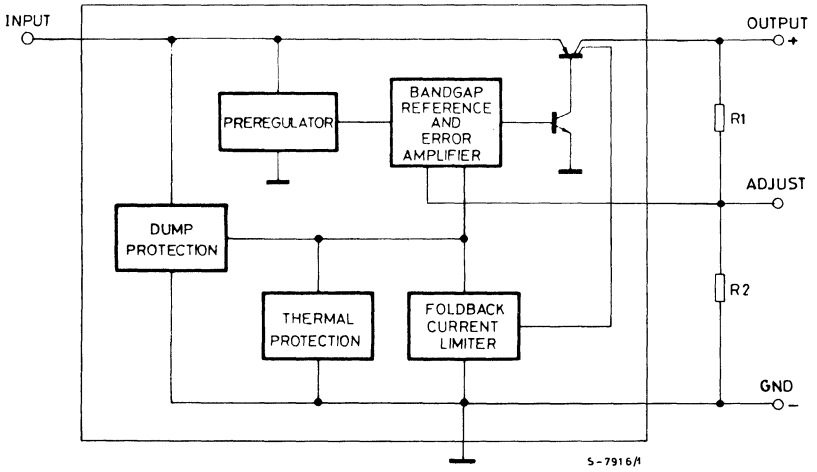
Pentawatt®

Minidip (4 + 4)

ORDERING NUMBERS:

L4920 L4921

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (For V_i = 14.4V V_o = 5V; T_j = 25°C; C = 100μF; R2 = 6.2KΩ unless otherwise noted)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	Operating input voltage	$V_o \geq 4.5V$ I_o = 400mA	V_o+0.7		26	V
		$V_{REF} \leq V_o < 4.5V$ I_o = 400mA	5.2		26	V
V_{REF}	Reference voltage	$5.2V < V_i < 26V$ $I_o \leq 400mA$ (*)	1.20	1.25	1.30	V
ΔV_o	Line regulation	$V_o + 1V < V_i < 26V$ $V_o \geq 4.5V$ I_o = 5mA		1	10	mV/V_o
ΔV_o	Load regulation	$5mA < I_o < 400mA$ (*) $V_o \geq 4.5V$		3	15	mV/V_o
V_D	Dropout voltage	I_o = 10mA I_o = 150mA I_o = 400mA		0.05 0.2 0.4	 0.4 0.7	V V V
I_D	Quiescent current	I_o = 0mA $V_o + 1V < V_i < 26V$		0.8	3	mA
		I_o = 400mA (*) $V_o + 1V < V_i < 26V$		65	100	mA
I_o	Maximum output current			650	900	mA
I_{OSC}	Short circuit output current (*)		200	350	500	mA
V_R	Reverse polarity input voltage (DC)	$V_o \geq -1.5V$ $R_L \leq 500\Omega$			-18	V

(*) Foldback protection

L4941

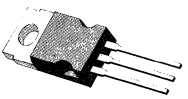
ADVANCE DATA

VERY LOW DROP 1A REGULATOR

- PRECISE 5V OUTPUT (± 2%)
- LOW DROPOUT VOLTAGE (450mV TYP. AT 1A)
- VERY LOW QUIESCENT CURRENT
- THERMAL SHUT DOWN
- SHORT CIRCUIT CURRENT LIMITER
- OVERVOLTAGE PROTECTION
- REVERSE POLARITY PROTECTION

The L4941 is a very low input/output voltage drop, low quiescent current and high output current capability IC particularly useful in applications such as battery powered systems where power dissipation is a design constraint.

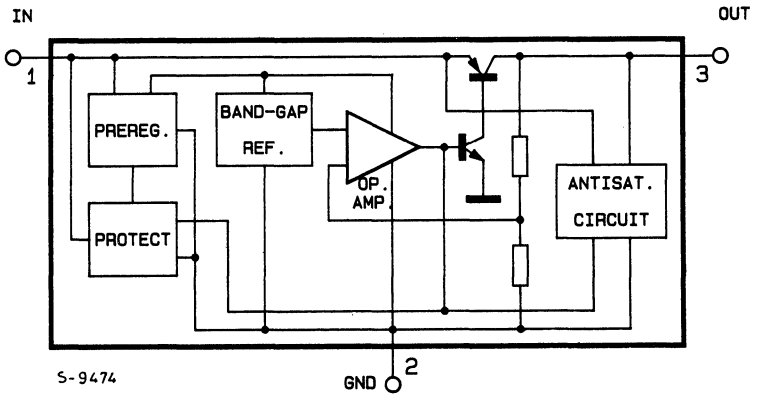
Standard regulator features such as thermal shut down, current limiter and overvoltage protection are also provided.



TO-220

ORDERING NUMBER: L4941BV

BLOCK DIAGRAM



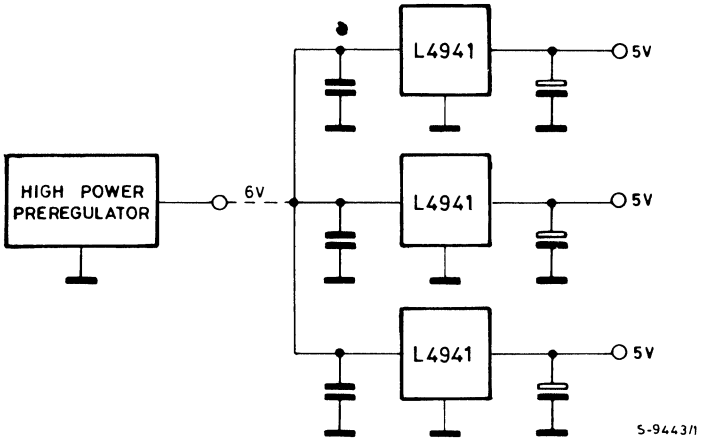
ELECTRICAL CHARACTERISTICS (V_i = 14V, T_j = 25°C)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	I_O = 5mA	4.9	5	5.1	V
V_O	Output voltage	V_i = 6V to 14V I_O = 5mA to 1A	4.8	5	5.2	V
V_i	Operating input voltage	(*) See note			16	V
V_O	Line regulation	6V ≤ V_i ≤ 16V I_O = 5mA		5	25	mV
V_O	Load regulation	I_O = 50mA to 1A		15	35	mV
I_d	Quiescent current	6V ≤ V_i ≤ 16V I_O = 5mA		3.5	10	mA
		I_O = 1A		20	50	
V_i-V_O	Dropout voltage	I_O = 1A		450	700	mV
		I_O = 100mA		150	250	
$\Delta V_O/\Delta T$	Output voltage drift			0.6		mV/°C
SVR	Supply voltage rejection	f = 120Hz I_O = 1A	60			dB
I_O	Current limit			1.3		A
Z_O	Output impedance	I_O = 200mA f = 120Hz		30		mΩ
E_N	Output noise voltage	f = 100Hz to 100KHz I_O = 10mA		100		μV rms

(*) For a DC input voltage 16V < V_i < 40V the device is not operating

APPLICATION INFORMATION

Fig. 8 - Distributed supply with on-card L4941 low-drop regulators



Advantages of this application are:

- Card isolation
- Thermal and short-circuit protection
- High efficiency (80%), like switching regulators, but without radiation and intermodulation problems

L4960

PRELIMINARY DATA

2.5A POWER SWITCHING REGULATOR

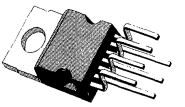
- 2.5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- PRECISE (± 2%) ON-CHIP REFERENCE
- HIGH SWITCHING FREQUENCY
- VERY HIGH EFFICIENCY (UP TO 90%)
- VERY FEW EXTERNAL COMPONENTS
- SOFT START
- INTERNAL LIMITING CURRENT
- THERMAL SHUTDOWN

The L4960 is a monolithic power switching regulator delivering 2.5A at a voltage variable from 5V to 40V in step down configuration.

Features of the device include current limiting, soft start, thermal protection and 0 to 100% duty cycle for continuous operation mode.

The L4960 is mounted in a Heptawatt plastic power package and requires very few external components.

Efficient operation at switching frequencies up to 150KHz allows a reduction in the size and cost of external filter components.



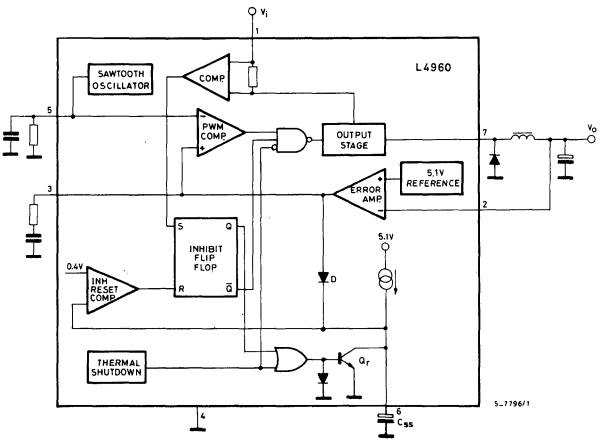
Heptawatt

ORDERING NUMBER: L4960 (Vertical)
L4960H (Horizontal)

ABSOLUTE MAXIMUM RATINGS

V_1	Input voltage	50	V
$V_1 - V_7$	Input to output voltage difference	50	V
V_7	Negative output DC voltage	-1	V
	Negative output peak voltage at t = 0.1μs; f = 100KHz	-5	V
V_3, V_6	Voltage at pin 3 and 6	5.5	V
V_2	Voltage at pin 2	7	V
I_3	Pin 3 sink current	1	mA
I_5	Pin 5 source current	20	mA
P_{tot}	Power dissipation at $T_{case} \leqslant 90°C$	15	W
T_j, T_{stg}	Junction and storage temperature	-40 to 150	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $T_j = 25°C$, $V_I = 35V$, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS						
V_o	Output voltage range	$V_I = 46V$ $I_o = 1A$	V_{ref}		40	V
V_I	Input voltage range	$V_o = V_{ref}$ to 36V $I_o = 2.5A$	9		46	V
ΔV_o	Line regulation	$V_I = 10V$ to 40V $V_o = V_{ref}$ $I_o = 1A$		15	50	mV
ΔV_o	Load regulation	$V_o = V_{ref}$ $I_o = 0.5A$ to 2A		10	30	mV
V_{ref}	Internal reference voltage (pin 2)	$V_I = 9V$ to 46V $I_o = 1A$	5	5.1	5.2	V
$\frac{\Delta V_{ref}}{\Delta T}$	Average temperature coefficient of refer. voltage	$T_j = 0°C$ to $125°C$ $I_o = 1A$		0.4		mV/°C
V_d	Dropout voltage	$I_o = 2A$		1.4	3	V
I_{om}	Maximum operating load current	$V_I = 9V$ to 46V $V_o = V_{ref}$ to 36V	2.5			A
I_{7L}	Current limiting threshold (pin 7)	$V_I = 9V$ to 46V $V_o = V_{ref}$ to 36V	3		4.5	A
I_{SH}	Input average current	$V_I = 46V$; output short-circuit		30	60	mA
η	Efficiency	$f = 100KHz$ $V_o = V_{ref}$		75		%
		$I_o = 2A$ $V_o = 12V$		85		%
SVR	Supply voltage ripple rejection	$\Delta V_I = 2V_{rms}$ $f_{ripple} = 100Hz$ $V_o = V_{ref}$ $I_o = 1A$	50	56		dB
f	Switching frequency		85	100	115	KHz
$\frac{\Delta f}{\Delta V_I}$	Voltage stability of switching frequency	$V_I = 9V$ to 46V		0.5		%
$\frac{\Delta f}{\Delta T_j}$	Temperature stability of switching frequency	$T_j = 0°C$ to $125°C$		1		%
f_{max}	Maximum operating switching frequency	$V_o = V_{ref}$ $I_o = 2A$	120	150		KHz
T_{sd}	Thermal shutdown junction temperature			150		°C

CIRCUIT OPERATION (refer to the block diagram)

The L4960 is a monolithic stepdown switching regulator providing output voltages from 5.1V to 40V and delivering 2.5A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to ± 2%).

This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage.

The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 3. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_{ss} and allowed to rise, linearly, as this capacitor is charged by a constant current source. Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V.

The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network. The thermal overload circuit disables circuit operation when the junction temperature reaches about 150°C and has hysteresis to prevent unstable conditions.

Fig. 1 - Soft start waveforms

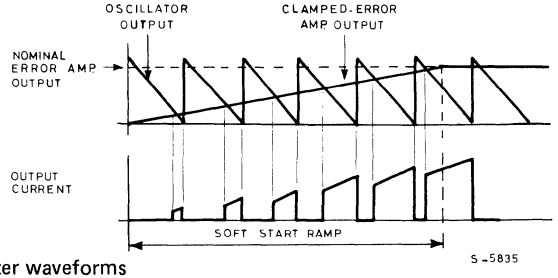


Fig. 2 - Current limiter waveforms

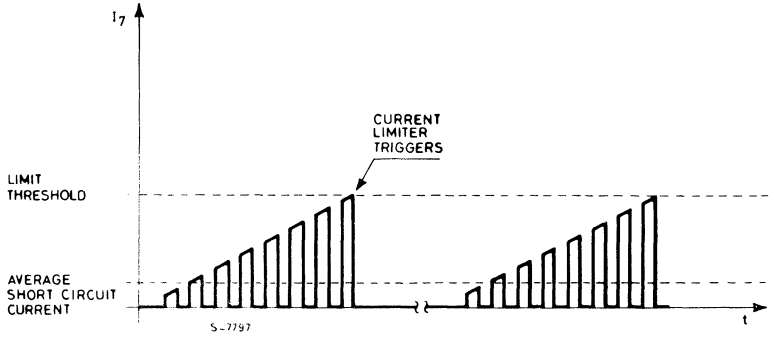


Fig. 7 - Quiescent drain current vs. junction temperature (100% duty cycle)

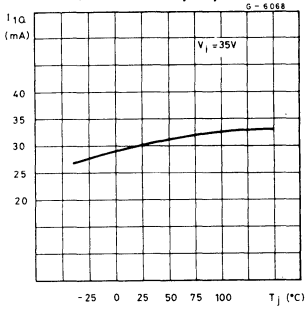


Fig. 8 - Reference voltage (pin 2) vs. V_i

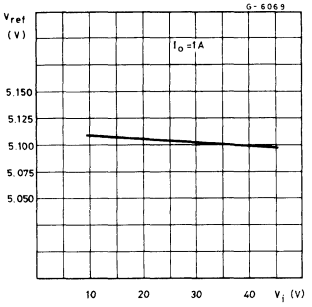


Fig. 9 - Reference voltage vs. junction temperature (pin 2)

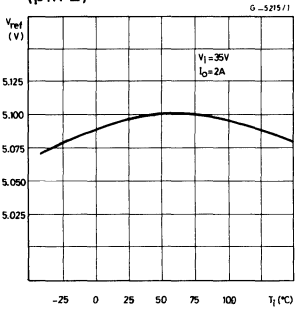


Fig. 10 - Open loop frequency and phase responde of error amplifier

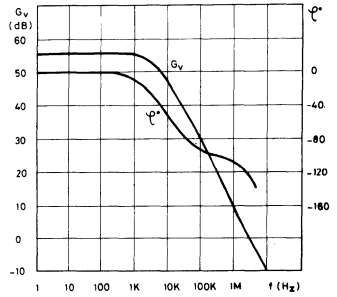


Fig. 11 - Switching frequency vs. input voltage

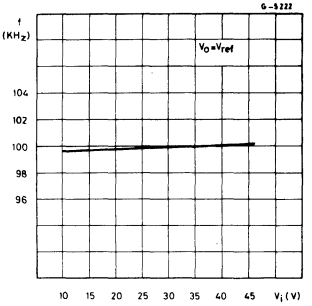


Fig. 12 - Switching frequency vs. junction temperature

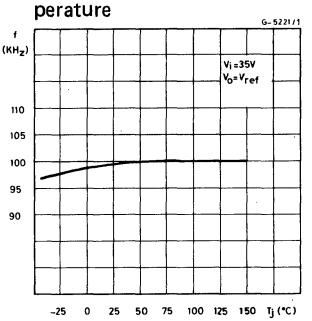


Fig. 13 - Switching frequency vs. R2 (see test circuit)

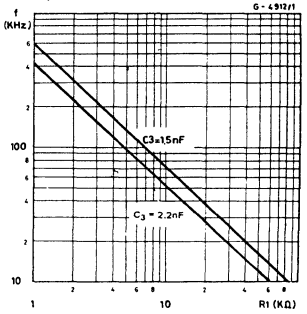


Fig. 14 - Line transient response

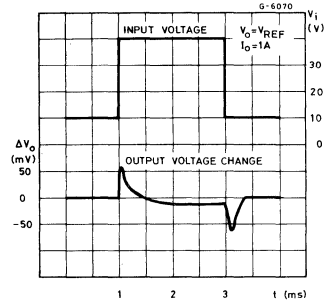
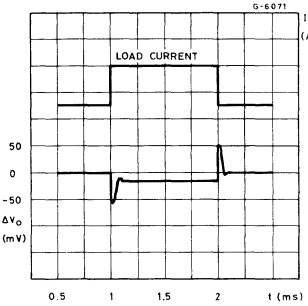
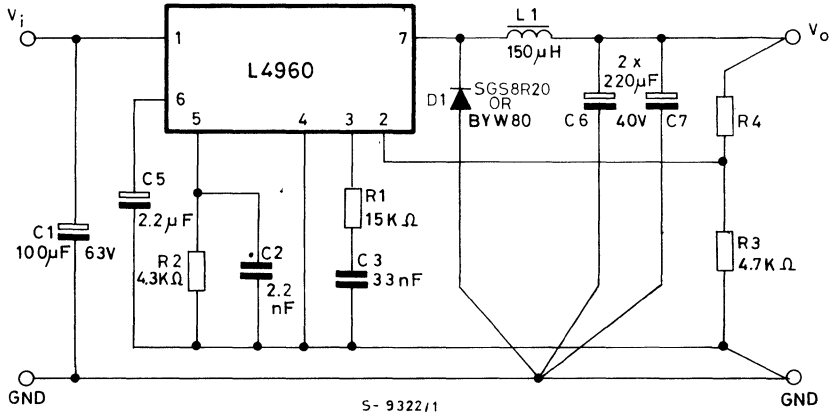


Fig. 15 - Load transient response



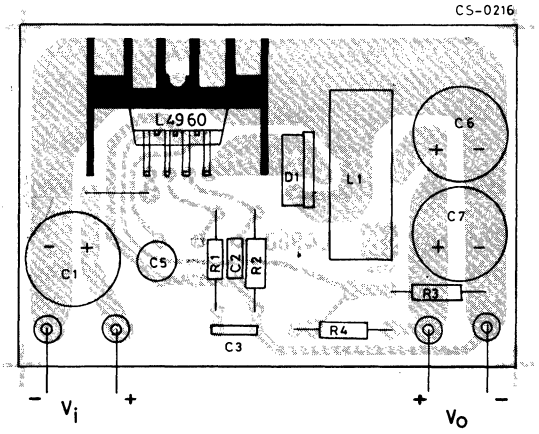
APPLICATION INFORMATION

Fig. 24 - Typical application circuit



C_1, C_6, C_7: EKR (ROE)
D_1: BYW80 OR 5A SCHOTTKY DIODE
SUGGESTED INDUCTOR: L_1 = 150µH at 5A
CORE TYPE: MAGNETICS 58206 - A2 - MPP
N° TURNS: 45, WIRE GAUGE: 0.8mm (20 AWG), COGEMA 946042
U15/GUP15: N° TURNS: 60, WIRE GAUGE: 0.8mm (20 AWG), AIR GAP: 1mm, COGEMA 969051.

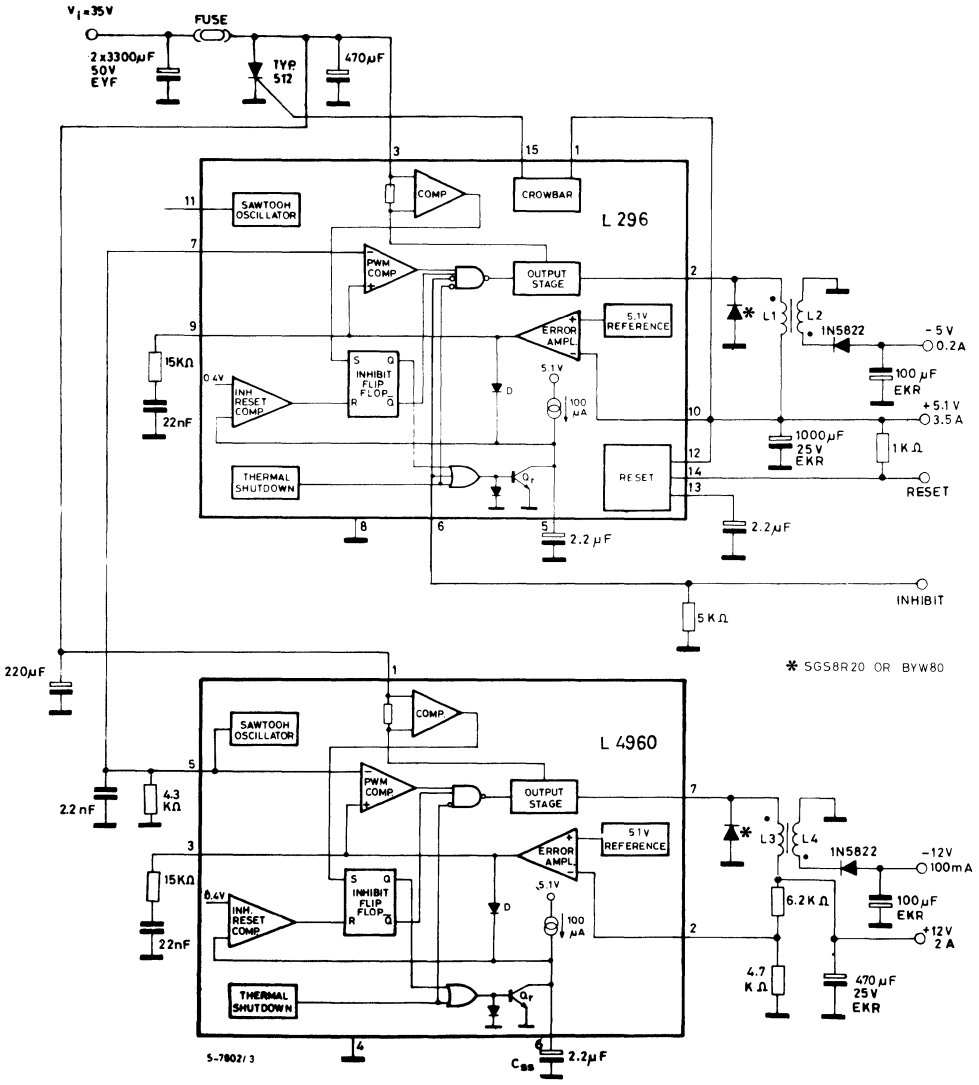
Fig. 25 - P.C. board and component layout of the Fig. 24 (1 : 1 scale)



Resistor values for standard output voltages		
V_o	R3	R4
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

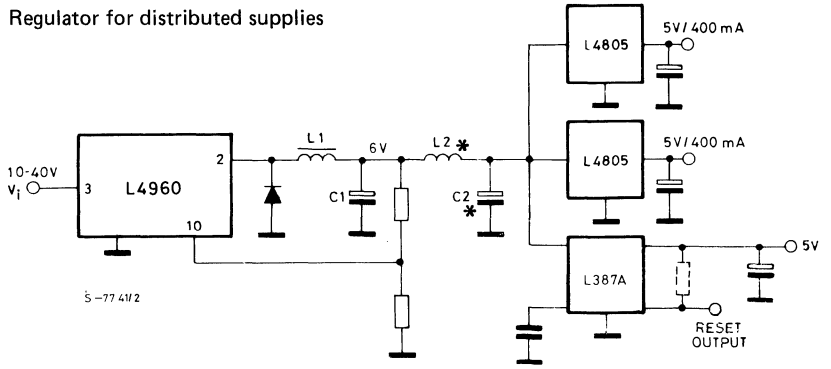
APPLICATION INFORMATION (continued)

Fig. 28 - Microcomputer supply with + 5.1V, -5V, +12V and -12V outputs



APPLICATION INFORMATION (continued)

Fig. 31 - Regulator for distributed supplies

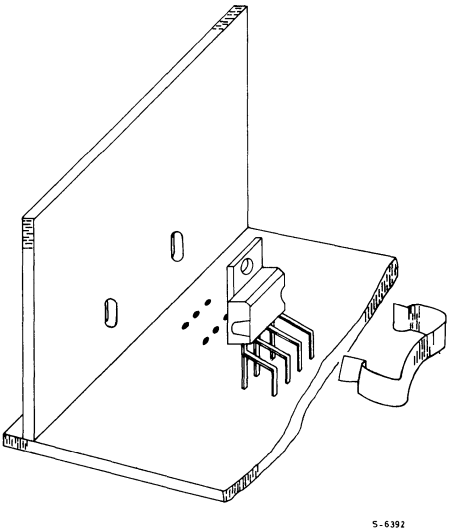


* L2 and C2 are necessary to reduce the switching frequency spikes when linear regulators are remote from L4960

MOUNTING INSTRUCTION

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the Heptawatt package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact, no electrical isolation is needed between the two surfaces.

Fig. 32 - Mounting example



L4962

PRELIMINARY DATA

1.5A POWER SWITCHING REGULATOR

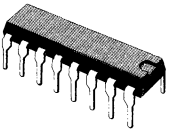
- 1.5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- PRECISE (± 20%) ON-CHIP REFERENCE
- HIGH SWITCHING FREQUENCY
- VERY HIGH EFFICIENCY (UP TO 90%)
- VERY FEW EXTERNAL COMPONENTS
- SOFT-START
- INTERNAL LIMITING CURRENT
- THERMAL SHUTDOWN

The L4962 is a monolithic power switching regulator delivering 1.5A at a voltage veriable from 5V to 40V in step down configuration.

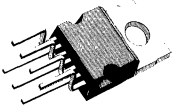
Features of device include current limiting, soft start, thermal protection and 0 to 100% duty cycle for continuous operating mode.

The L4962 is mounted in a 16-lead Powerdip plastic package and Heptawatt package and requires very few external components.

Efficient operation at switching frequencies up to 150KHz allows a reduction in the size and cost of external filter components.



Powerdip
(12 + 2 + 2)



Heptawatt

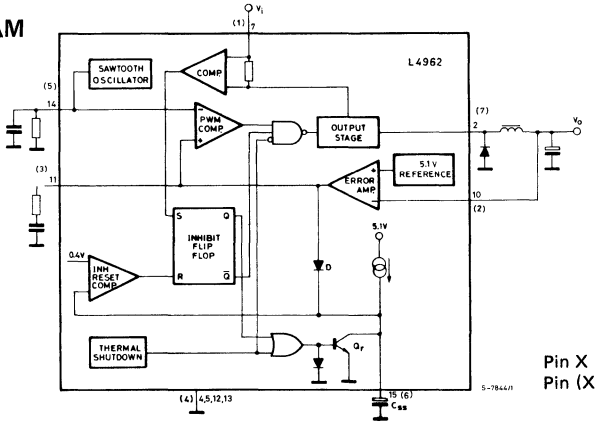
ORDERING NUMBER:

L4962 (12 + 2 + 2 Powerdip)
L4962E (Heptawatt)
L4962EH (Horizontal Heptawatt)

ABSOLUTE MAXIMUM RATINGS

V_7	Input voltage	50	V
$V_7 - V_2$	Input to output voltage difference	50	V
V_2	Negative output DC voltage	-1	V
	Output peak voltage at t = 0.1μs, f = 100KHz	-5	V
V_{11}, V_{15}	Voltage at pin 11, 15	5.5	V
V_{10}	Voltage at pin 10	7	V
I_{11}	Pin 11 sink current	1	mA
I_{14}	Pin 14 source current	20	mA
P_{tot}	Power dissipation at $T_{pins} \leqslant 90°C$ (Powerdip)	4.3	W
	$T_{case} \leqslant 90°C$ (Heptawatt)	15	W
T_j, T_{stg}	Junction and storage temperature	-40 to 150	°C

BLOCK DIAGRAM



Pin X = Powerdip
Pin (X) = Heptawatt

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $T_j = 25°C$, $V_i = 35V$, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS						
V_o	Output voltage range	V_i = 46V I_o = 1A	V_{ref}		40	V
V_i	Input voltage range	$V_o = V_{ref}$ to 36V I_o = 1.5A	9		46	V
ΔV_o	Line regulation	V_i = 10V to 40V $V_o = V_{ref}$ I_o = 1A		15	50	mV
ΔV_o	Load regulation	$V_o = V_{ref}$ I_o = 0.5A to 1.5A		8	20	mV
V_{ref}	Internal reference voltage (pin 10)	V_i = 9V to 46V I_o = 1A	5	5.1	5.2	V
$\frac{\Delta V_{ref}}{\Delta T}$	Average temperature coefficient of refer. voltage	T_j = 0°C to 125°C I_o = 1A		0.4		mV/°C
V_d	Dropout voltage	I_o = 1.5A		1.5	2	V
I_{om}	Maximum operating load current	V_i = 9V to 46V $V_o = V_{ref}$ to 36V	1.5			A
I_{2L}	Current limiting threshold (pin 2)	V_i = 9V to 46V $V_o = V_{ref}$ to 36V	2		3.3	A
I_{SH}	Input average current	V_i = 46V; output short-circuit		15	30	mA
η	Efficiency	f = 100KHz $V_o = V_{ref}$		70		%
		I_o = 1A V_o = 12V		80		%
SVR	Supply voltage ripple rejection	$\Delta V_i = 2V_{rms}$ f_{ripple} = 100Hz $V_o = V_{ref}$ I_o = 1A	50	56		dB
f	Switching frequency		85	100	115	KHz
$\frac{\Delta f}{\Delta V_i}$	Voltage stability of switching frequency	V_i = 9V to 46V		0.5		%
$\frac{\Delta f}{\Delta T_j}$	Temperature stability of switching frequency	T_j = 0°C to 125°C		1		%
f_{max}	Maximum operating switching frequency	$V_o = V_{ref}$ I_o = 1A	120	150		KHz
T_{sd}	Thermal shutdown junction temperature			150		°C

CIRCUIT OPERATION (refer to the block diagram)

The L4962 is a monolithic stepdown switching regulator providing output voltages from 5.1V to 40V and delivering 1.5A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to ± 2%).

This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage.

The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 11. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_{ss} and allowed to rise, linearly, as this capacitor is charged by a constant current source. Output overload protection is provided in the form of a current limiter. The load current is sensed by a internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V.

The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network. The thermal overload circuit disables circuit operation when the junction temperature reaches about 150°C and has hysteresis to prevent unstable conditions.

Fig. 1 - Soft start waveforms

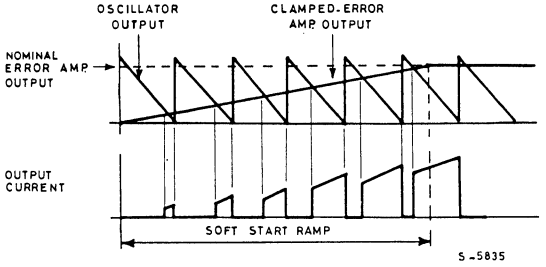


Fig. 2 - Current limiter waveforms

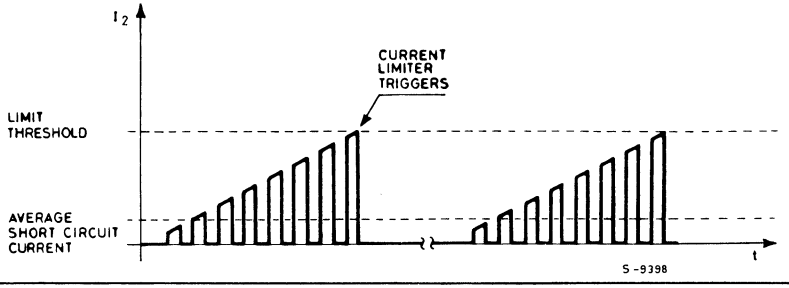


Fig. 7 - Quiescent drain current vs. junction temperature (100% duty cycle)

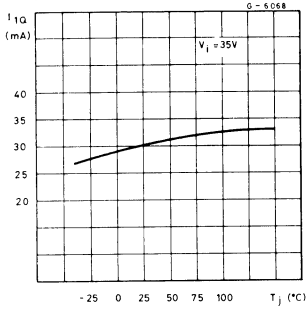


Fig. 8 - Reference voltage (pin 10) vs. V_I rdip) vs. V_I

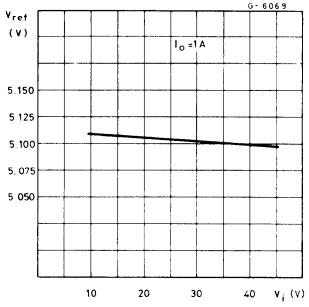


Fig. 9 - Reference voltage (pin 10) vs. junction temperature

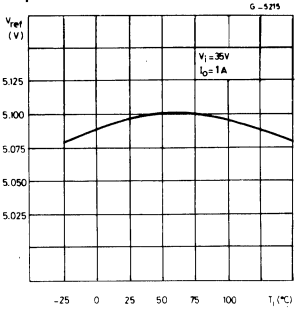


Fig. 10 - Open loop frequency and phase response of error amplifier

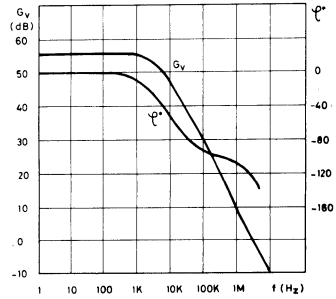


Fig. 11 - Switching frequency vs. input voltage

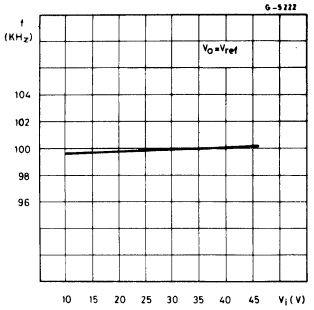


Fig. 12 - Switching frequency vs. junction temperature

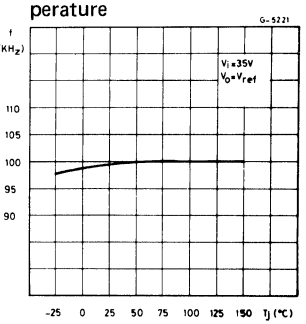


Fig. 13 - Switching frequency vs. R2 (see test circuit)

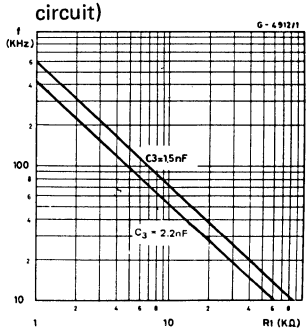


Fig. 14 - Line transient response

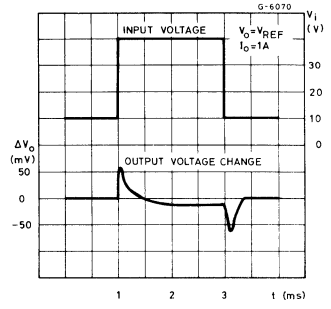
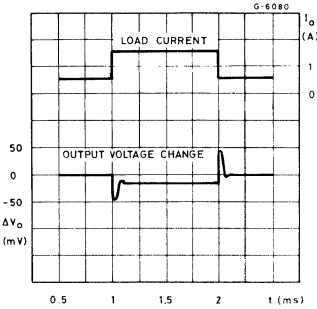
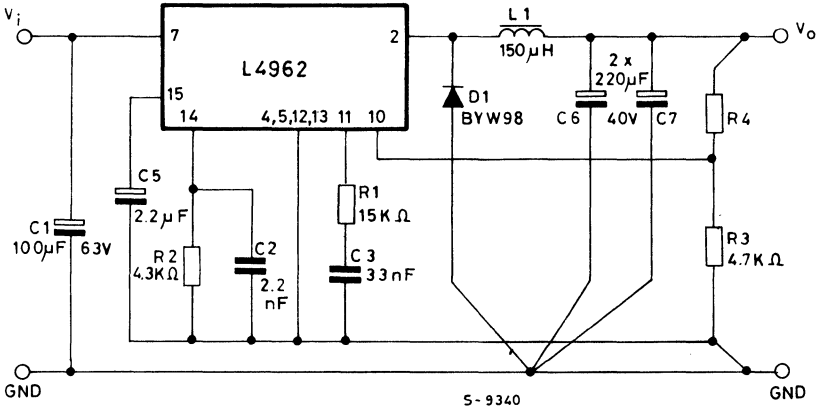


Fig. 15 - Load transient response



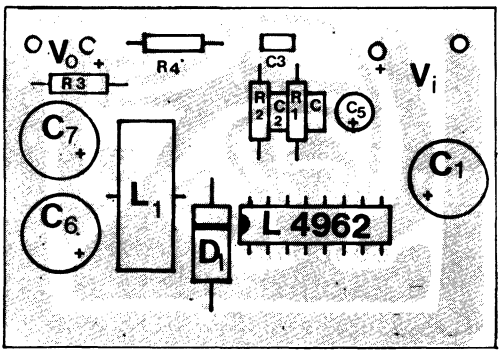
APPLICATION INFORMATION

Fig. 25 - Typical application circuit



C_1, C_6, C_7: EKR (ROE)
D_1: BYW98 OR VISK340 (SCHOTTKY)
SUGGESTED INDUCTORS (L_1): MAGNETICS 58120 - A2MPP - 45 TURNS - WIRE GAUGE 0.8mm (20AWG) - COGEMA 946043
OR U15, GUP15, 60 TURNS 1mm, AIR GAP 0.8mm (20AWG) - COGEMA 969051

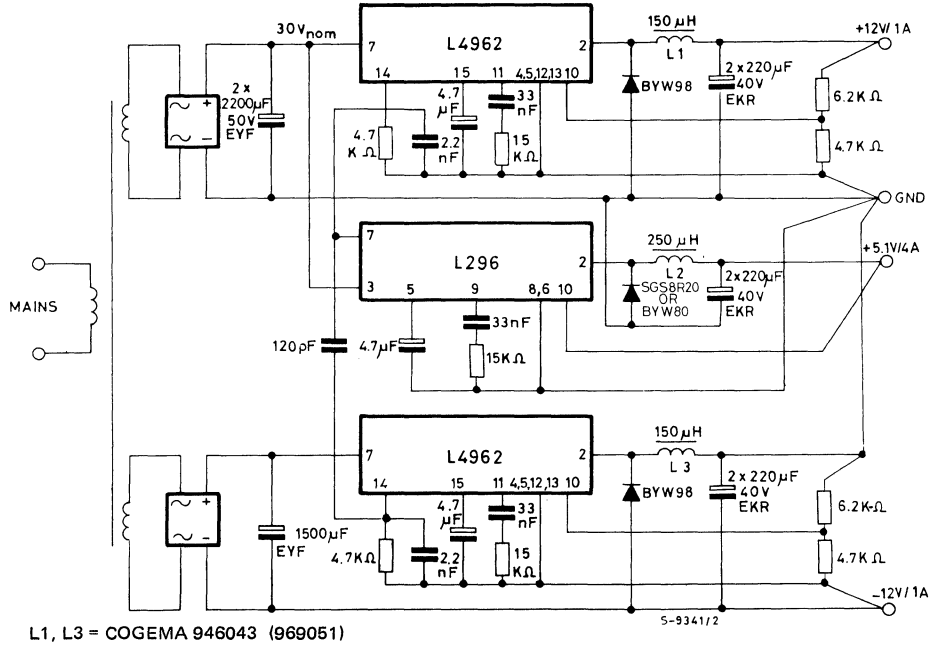
Fig. 26 - P.C. board and component layout of the circuit of Fig. 25 (1 : 1 scale)



Resistor values for standard output 7 voltages		
V_o	R8	R7
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

APPLICATION INFORMATION (continued)

Fig. 29 - DC-DC converter 5.1V/4A, ± 12V/1A. A suggestion how to synchronize a negative output



L1, L3 = COGEMA 946043 (969051)
L2 = COGEMA 946044 (946045)

Fig. 30 - In multiple supplies several L4962s can be synchronized as shown

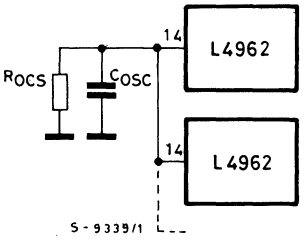
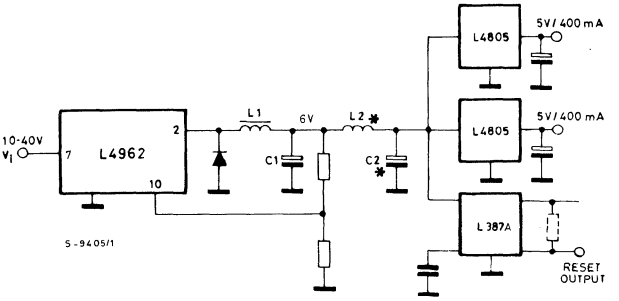


Fig. 31 - Preregulator for distributed supplies



* L2 and C2 are necessary to reduce the switching frequency spikes when linear regulators are remote from L4962

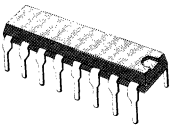
L5832

SOLENOID CONTROLLER

- DRIVES ONE OR TWO EXTERNAL DARLINGTONS
- DUAL AND SINGLE LEVEL CURRENT CONTROL
- SWITCHMODE CURRENT REGULATION
- ADJUSTABLE PEAK DURATION
- WIDE SUPPLY RANGE (4.75-46V)
- TTL-COMPATIBLE LOGIC INPUTS
- THERMAL PROTECTION

The L5832 Solenoid Controller is designed for use with one or two external darlington transistors in solenoid and relay driving applications. The device is controlled by two logic inputs and features switchmode regulation of the load current. A key feature of the L5832 is flexibility. It can be used with a variety of darlingtons to match the requirements of the load and it allows both simple and two level current control Moreover, the drive waveshape can be adjusted by external components. Other features of the device include thermal shutdown, a supply voltage range of 4.75-46V and TTL-compatible inputs.

The L5832 is supplied in a 12 + 2 + 2 - lead Powerdip package which uses the four center pins to conduct heat to the PC board copper.



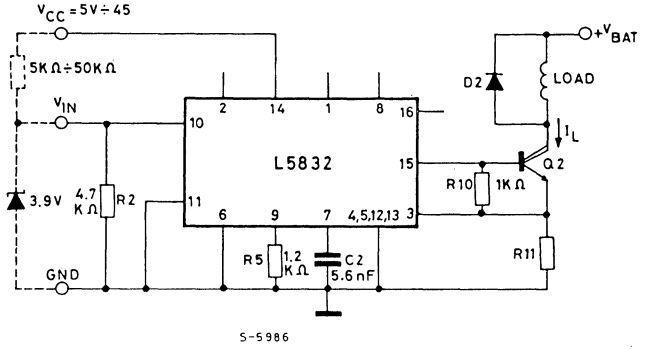
Powerdip
12 + 2 + 2

ORDERING NUMBER: L5832

ABSOLUTE MAXIMUM RATINGS

V_s	DC Supply voltage	46	V
V_8	(Positive transient voltage at pin 8)	60	V
V_{en}	Enable input voltage (pin 11)	7	V
V_i	Input voltage (pin 10)	7	V
V_R	External reference voltage (pin 2)	2	V
P_d	Power dissipation (T_{case} = 80°C)	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

APPLICATION CIRCUIT USING ONE DARLINGTON



PIN FUNCTIONS

N°	NAME	FUNCTION
1	NC	Not connected. Must be left open circuit.
2	HOLDING CURRENT CONTROL	A voltage applied to this pin sets the holding current level. If left open circuit an internal 75 mV reference is used and $I_h = I_p/6$.
3	SENSING	Connection for load current sense resistor. Value sets the maximum load current. $I_p = 0.45/R_s$.
4	GROUND	Ground connection. With pins 5, 12 and 13 conducts heat to printed circuit board copper.
5	GROUND	See pin 4.
6	C1	A capacitor connected between this pin and ground sets the duration of the current peak (t2 in fig. 3). If left open, the switchmode control of the peak is suppressed. If grounded, the current does not fall to the holding level.
7	DISCHARGE TIME CONSTANT	A capacitor connected between this pin and ground sets the duration of t_{off} (fig. 3). If grounded, switchmode control is suppressed.
8	PNP DRIVING OUTPUT	Current drive output for external PNP darlington (for recirculation). $I = 35\ I_{ref}$.
9	REFERENCE VOLTAGE	A resistor connected between this pin and ground sets the internal current reference, I_{ref}. The recommended value is 1.2 kΩ, giving $I_{ref} = 1$ mA.
10	INPUT	TTL-compatible input. A high level on this pin activates the output, driving the load.
11	INHIBIT	TTL-compatible inhibit input. A high level on this input disables the output stages and logic circuitry, irrespective of the state of pin 10.
12	GROUND	See pin 4.
13	GROUND	See pin 4.
14	SUPPLY VOLTAGE	Supply voltage input.
15	NPN DRIVING OUTPUT	Current drive for external NPN darlington (in series with the load). $I = 100\ I_{ref}$.
16	INTERNAL CLAMPING	Internal zener clamp available for fast turnoff.

APPLICATION INFORMATION

The L5832 solenoid controller is intended for use with one or two external darlington transistors to drive inductive loads such as solenoids, relays, electric valves and DC motors.

Controlled by a logic input and an inhibit input (both TTL compatible), the device drives the external darlington(s) to produce a load current waveform as shown in figure 3. This basic waveform shows that the device produces an initial current peak followed by a lower holding current. Both the peak and holding current levels are regulated by the L5832's switchmode circuitry.

The duration of the peak, the peak current level and holding current level can all be adjusted by external components.
Moreover, by omitting C1, C2 or both it is possible to realize single-level current control, a transitory peak followed by a regulated holding current or a simple peak (figure 1).

Fig. 1 - Components connected to pins 6 and 7 determine the load current waveshape

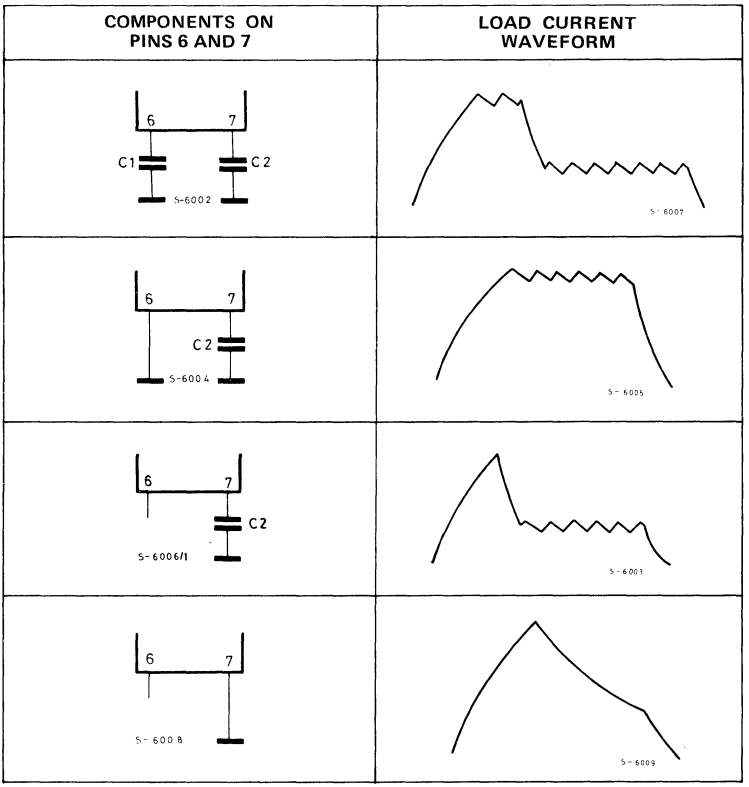
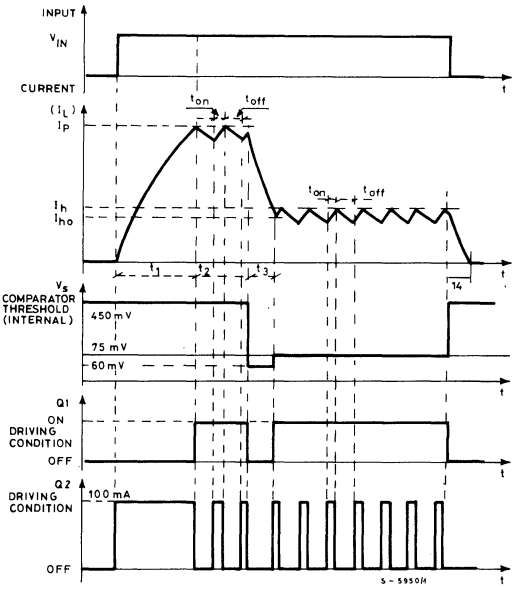


Fig. 3 - Waveforms of the typical application circuit of fig. 2.



The discharge time constant (t_{off} in figure 3) is set by a capacitor between pin 7 and ground and is found from:

$$t_{off} = \frac{12C2}{I_{ref}}$$

The t_{off} and t_{on} times are also related to the current ripple, ΔI:

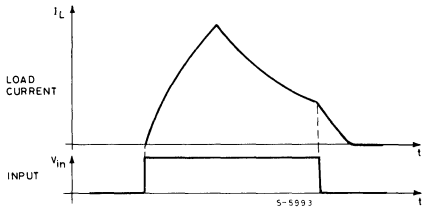
$$t_{off} = \frac{L \Delta I}{V_{off}} \quad \text{and} \quad t_{on} = \frac{L \Delta I}{V_{on}}$$

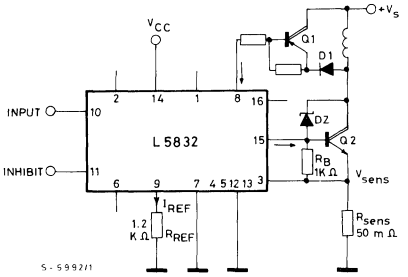
where $V_{off} = V_{diode} + V_{CEQ1} + R_L I_L$
$V_{on} = V_s - V_{CEQ2} - V_{RS} - R_L I_L$
L = load inductance
R_L = load resistance
ΔI = load current ripple.

Note that t_{off} is the same for both the peak and holding currents.

Fig. 6 - Switchmode control of the current can be suppressed entirely by leaving pin 6 open and grounding pin 7. The peak current is still controlled.

I_o (A)	Q1	Q2
4	BDX54	BDX53
8	BDW94	BDW93
10	BDV64	BDV65





For fast turnoff an internal zener clamp is available on pin 16.
This is used with an external divider, R8 R9, as shown in figure 2. Suitable values can be found from:

$$V_{pin\ 16} \cong 15V + V_{BEQ2} + VRsense$$

$$V_{CQ2} \cong V_{pin\ 16} \cdot \frac{R9 + R8}{R8}$$

(V_{CQ2} is the voltage at the collector of Q2).

To ensure stability, a small capacitor (about 200 pF) must be connected between the base and collector of Q2 when pin 16 is used.

For the application circuit of figure 7 $t_{off} = 12C2/I_{ref}$, as before, and the current ripple is given by:

$$t_{off} = -\frac{L}{R} \frac{\ln (I_{LP} - \Delta I) \cdot R_L + V_L}{I_{LP} \cdot R_L + V_L}$$

where V_L is the voltage across the inductor during recirculation.

Note that if the load is a motor $V_L = Eg + V_D$.

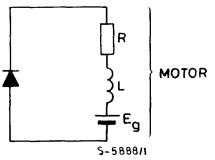


Fig. 8 - P.C. board and component layout of the circuit of fig. 7 (1:1 scale)

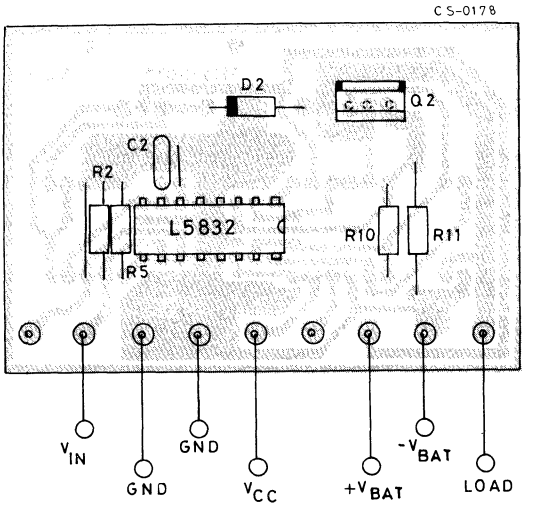
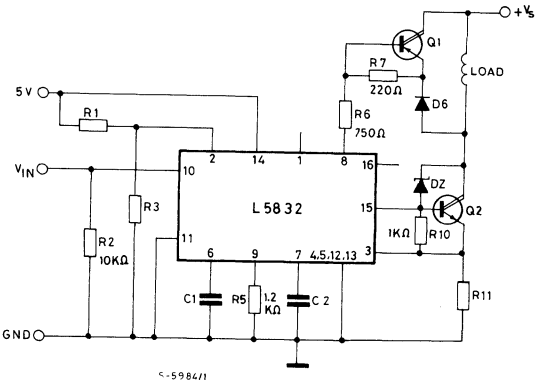


Fig. 9 - Application circuit showing how two separate supplies can be used.



L6100
L6101
L6102

ADVANCE DATA

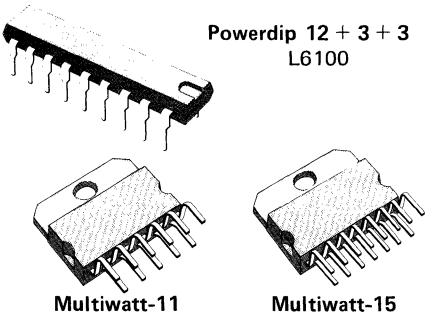
100V-1A, QUAD DMOS POWER SWITCH

The L6100, L6101 and L6102 are DMOS quad transistor array realized with a new process called Multipower-BCD which allows the integration of multiple isolated DMOS transistors - plus bipolar linear and CMOS logic circuits on a single chip.

Each of the four power DMOS transistors is a parallel combination of one thousand elementary cells with a packing density in excess of 1600 cells/mm^2.

The device is assembled in three package: 12+3+3 lead powerdip; 11-lead Multiwatt® and 15-lead Multiwatt®.

MultiPower BCD Technology



Powerdip 12 + 3 + 3
L6100

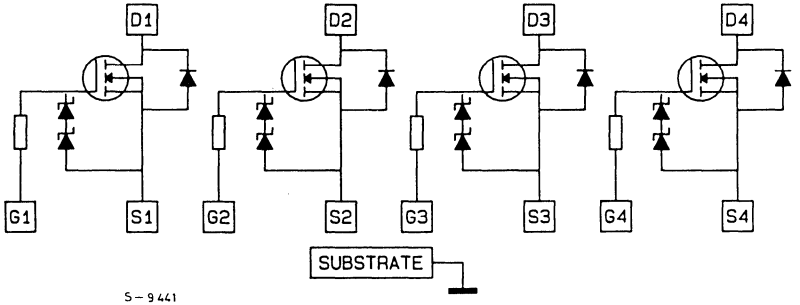
Multiwatt-11
L6101

Multiwatt-15
L6102

ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage	100	V
V_{DGR}	Drain-gate voltage (R_{GS} = 14KΩ)	100	V
V_{GS}	Gate-source voltage	+14 to -0.6	V
I_D	Drain current		
	– DC operation	1	A
	– Pulsed (300μs, 1% duty cycle)	2.5	A
T_{stg}, T_j	Storage and junction temperature range	-40 to +150	°C

SCHEMATIC DIAGRAM



S-9441

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-source breakdown voltage	@ I_D = 1mA V_{GS} = 0V	100			V
V_{GS} (TH)	Threshold voltage	@ I_D = 1mA V_{GS} = V_{DS}	2		4	V
I_{GSS}	Gate-source leakage	@ V_{GSS} = 10V			1	μA
R_{DS} (ON)	Static drain-source on-state resistance	@ V_{GS} = 10V I_D = 1A			1.2	Ω

Fig. 1 - Saturation characteristics

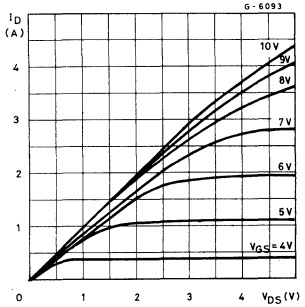


Fig. 2 - Normalized ON-resistance vs. temperature

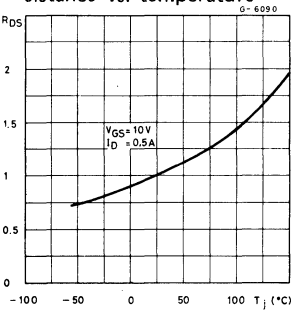


Fig. 3 - Transconductance vs. drain current

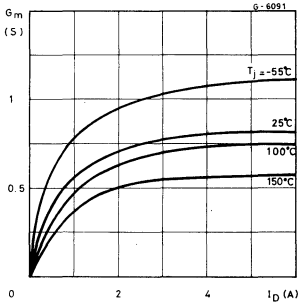
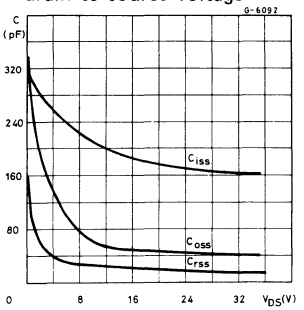


Fig. 4 - Capacitance vs. drain to source voltage



L6202

ADVANCE DATA

1.5A DMOS FULL BRIDGE DRIVER

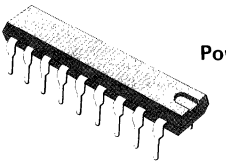
- POWER SUPPLY VOLTAGE UP TO 52V
- TOTAL DC CURRENT UP TO 1.5A
- LOW SATURATION VOLTAGE
- LOW POWER DISSIPATION
- NO CROSS CONDUCTION
- TTL COMPATIBLE INPUTS
- OVERTEMPERATURE PROTECTION

Realized with mixed bipolar/CMOS/DMOS technology, the L6202 is a full bridge driver for motor control applications. Delivering up to 1.5A output current at motor supply voltages up to 52V, the device uses DMOS output transistors to obtain very high efficiency and fast switching speed.

Each channel (half-bridge) of the device is controlled by a separate logic input, while a common enable input controls both channels. All inputs are TTL, CMOS and μC-compatible.

The L6202 is assembled in a Powerdip 12+3+3 package an 18-lead DIP using the six center pins to conduct heat to the PCB. Thanks to the very high efficiency of the DMOS output stage no external heatsink is necessary, even when operating at the full rated current and voltage.

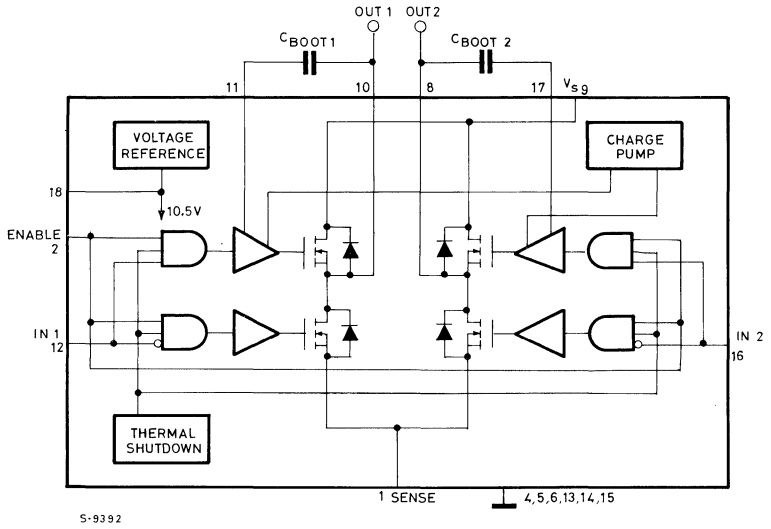
MultiPower BCD Technology



Powerdip 12 + 3 + 3

ORDERING NUMBER: L6202

BLOCK DIAGRAM



Note: suggested value for $C_{BOOT\,1,2}$: 10nF

PIN FUNCTIONS

N°	NAME	FUNCTION
1	SENSE	A resistance R_{sense}, connected to this pin, allows motor current control.
2	ENABLE	Enable Input. A logic low level on this pin switches off the DMOS POWER transistors.
3	NOT CONNECTED	
4	GROUND	Common ground terminal.
5	GROUND	Common ground terminal.
6	GROUND	Common ground terminal.
7	NOT CONNECTED	
8	OUT 2	Output of the half bridge.
9	V_S	Supply voltage.
10	OUT 1	Output of the half bridge.
11	BOOT 1	A capacitor $C_{BOOT\,1}$, connected to this terminal allows the upper DMOS transistor driving for high switching frequencies.
12	IN 1	Input from the controller device.
13	GND	Common ground terminal.
14	GND	Common ground terminal
15	GND	Common ground terminal.
16	IN 2	Input from the controller device.
17	BOOT 2	A capacitor $C_{BOOT\,2}$, connected to this terminal, allow the upper DMOS transistor driving for high switching frequencies.
18	V_{ref}	Internal reference voltage.

CIRCUIT OPERATION

The L6202 is a monolithic full bridge switching motor driver realized in the new Multipower-BCD technology which allows the integration of multiple, isolated DMOS power transistors plus mixed CMOS/bipolar control circuits.

The power stage of the L6202 consists of four N-channel DMOS transistors with an $R_{DS\ (ON)} \cong 0.3\Omega$ over whole current range. Each transistor has an intrinsic drain-source diode. During recirculation the behaviour of these diodes depends on the operating mode.

When one of the POWER DMOS transistor is ON it behaves almost symmetrically in terms of current - like, in fact, a resistor with the value $R_{DS\ (ON)}$ in parallel with the drain-source diode.

During recirculation with the ENABLE input high, the voltage drop across the transistor is $R_{DS\ (ON)} \times I_L$ for voltages less than 0.7V and is clamped at a voltage depending on the characteristics of the diode for greater voltages.

When the ENABLE input is low, the POWER MOS is OFF and the diode carry the whole recirculation.

Although the device guarantees the absence of cross-conduction, the presence of the intrinsic diodes in the POWER DMOS structure causes the generation of current spikes on the sensing terminals due to charge-discharge phenomena in the capacitors C1 & C2 associated with the drain source junctions (Fig. 1). When the output switches from high to low a current spike is generated associated with the capacitor C1. On the low-to-high transition a spike of the same polarity is generated by C2, preceded by a spike of the opposite polarity due to the charging of the input capacity of the lower POWER DMOS transistor. (Fig. 2)

To ensure that the POWER DMOS transistors are driven correctly a gate-source voltage of about 10V must be guaranteed for all of the N-channel DMOS transistors. While there is no problem in driving the lower POWER DMOS devices (their source terminals are referred to ground) it is necessary to provide a gate voltage higher than the positive supply for the upper transistors because they have the drain connected to the supply itself.

This obtained by a system that combines a charge pump circuit, which assures correct DC operation, with a boostrapping technique suitable for high switching frequencies.

In the boostrap circuit the external C_B capacitors are charged to a voltage of about 10V when the upper power transistor is OFF and the lower one is ON. To guarantee efficient driving of the upper power transistor in the conduction condition the value of C_B must be greater than the value of the input capacitance, C_{IN}, of the power transistor itself. Since the estimated value of the input capacity is about 1nF, C_B should be $> = 10$nF to guarantee correct operation.

An ON-OFF synchronisation circuit provides a dead time (the period in which all four power transistors are OFF) of 40ns, sufficient to prevent simultaneous conduction with obvious advantages in terms of power dissipation and of spurious signals on the ground and in the sensing resistors.

A thermal protection circuit has been included that will disable the device if the junction temperature reaches 150°C. When the temperature has fallen to a safe value the device restarts under the control of the input and enable signals.

Fig. 1 - Intrinsic structures in the POWER DMOS transistors

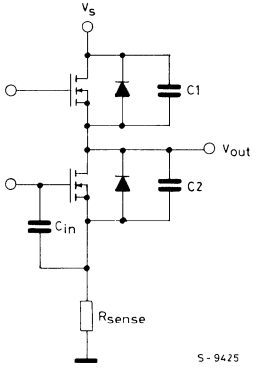


Fig. 2 - Current typical spikes on the sensing pin

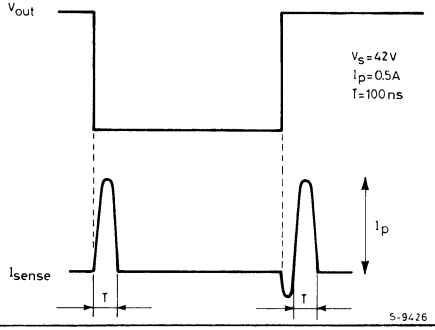
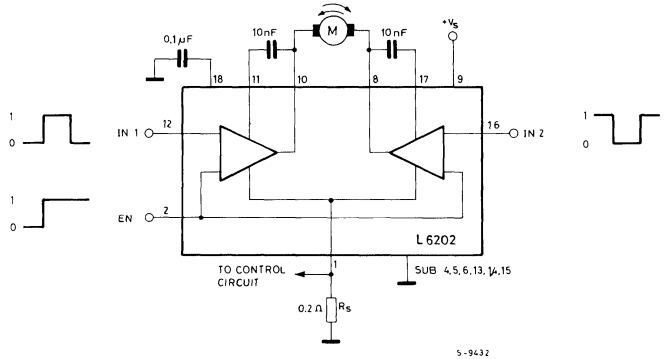


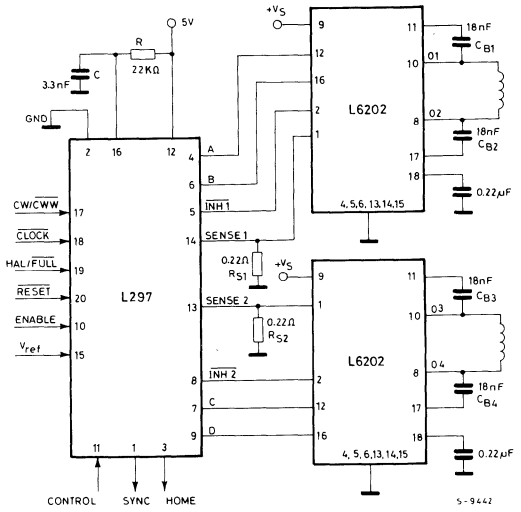
Fig. 7 - Bidirectional DC motor control



	INPUTS		FUNCTION
V_{EN} = H	IN1 = H	IN2 = L	Turn right
	IN1 = L	IN2 = H	Turn left
	IN1 = IN2		Fast motor stop
V_{EN} = L	IN1 = X	IN1 = IN2	Free running motor stop

L = Low H = High X = Don't care

Fig. 8 - Application circuit



L6203

ADVANCE DATA

3A DMOS FULL BRIDGE DRIVER

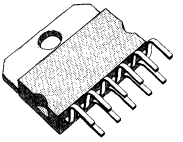
- OPERATING SUPPLY VOLTAGE UP TO 52V
- TOTAL DC CURRENT UP TO 3A
- LOW SATURATION VOLTAGE
- LOW POWER DISSIPATION
- NO CROSS CONDUCTION
- TTL COMPATIBLE INPUTS
- OVER TEMPERATURE PROTECTION

Realized with mixed bipolar/CMOS/DMOS technology, the L6203 is a full bridge driver for motor control applications. Delivering up to 3A output current at motor supply voltages up to 52V, the device uses DMOS output transistors to obtain very high efficiency and fast switching speed.

Each channel (half-bridge) of the device is controlled by a separate logic input, while a common enable input controls both channels. All inputs are TTL, CMOS and μC-compatible.

The L6203 is assembled in a 11-lead Multiwatt® package.

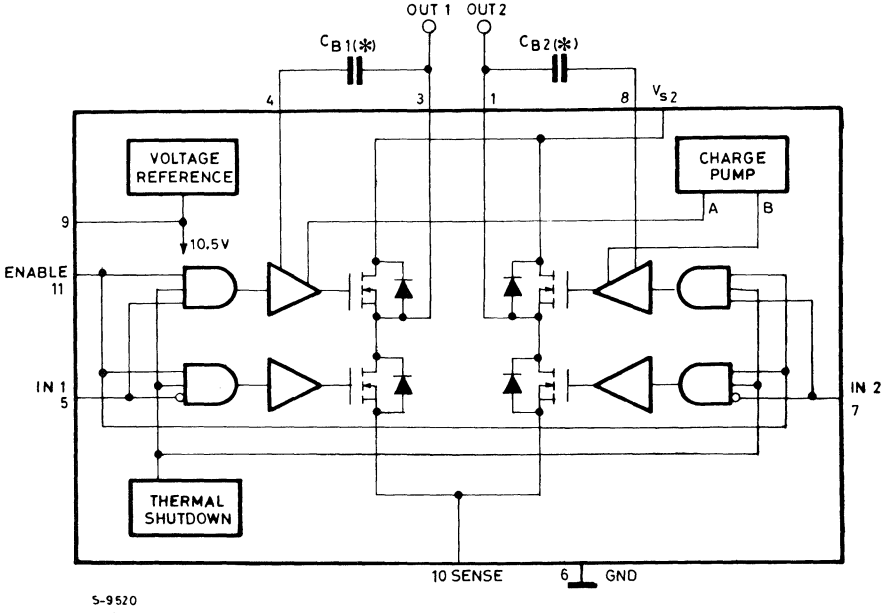
MultiPower BCD Technology



Multiwatt-11

ORDERING NUMBER: L6203

BLOCK DIAGRAM



(*) Suggested value for C_{BOOT1} and C_{BOOT2}: 10nF

PIN FUNCTIONS

N°	NAME	FUNCTION
1	OUT 2	Output of the half bridge.
2	V_S	Supply voltage.
3	OUT 1	Output of the half bridge.
4	BOOT. 1	A capacitor C_{B1}, connected to this terminal allows the upper DMOS transistor driving for high switching frequencies.
5	IN 1	Input from the controller device.
6	GND	Common ground terminal.
7	IN 2	Input from the controller device.
8	BOOT. 2	A capacitor C_{B2}, connected to this terminal allows the upper DMOS transistor driving for high switching frequencies.
9	V_{REF}	Internal reference voltage.
10	SENSE	A resistance R_{SENSE}, connected to this terminal, allows motor current control.
11	ENABLE	Enable input. A logic low level on this pin switches off the DMOS power transistors.

CIRCUIT OPERATION

The L6203 is a monolithic full bridge switching motor driver realized in the new Multipower-BCD technology which allows the integration of multiple, isolated DMOS power transistors plus mixed CMOS/bipolar control circuits.

The power stage of the L6203 consists of four N-channel DMOS transistors with an $R_{DS\ (ON)} \cong 0.3\Omega$ over the whole current range. Each transistor has an intrinsic drain source diode. During recirculation the behaviour of these diodes depends on the operating mode.

When one of the POWER DMOS transistors is ON it bahaves almost symmetrically in terms of current like, in fact, a resistor with the value $R_{DS\ (ON)}$ in parallel with the drain-source diode.

During recirculation with the ENABLE input high, the voltage drop across the transistor is $R_{DS\ (ON)} \times I_L$ for voltages less than 0.7V and is clamped at a voltage depending on the characteristics of the diode for greater voltages.

When the enable input is low, the POWER MOS is off and the diode carry the whole recirculation.

Although the device guarantees the absence of cross-conduction, the presence of the intrinsic diodes in the POWER MOS structure causes the generation of current spikes on the sensing pin due to charge-discharge phenomena in the reverse capacitor, C1 & C2 associated with the drain-source junctions (Fig. 1). When the output switches from high to low, a current spike is generated associated with the capacitor C1. On the low-to-high transition, a spike of the same polarity is generated by C2, preceded by a spike of the opposite polarity due to the charging of the input capacity of the lower POWER DMOS transistor (Fig. 2).

To ensure that the POWER DMOS transistors are driven correctly a gate-source voltage of about 10V must be guaranteed for all of the N-channel DMOS transistors. While there is no problem in driving the lower POWER DMOS devices (their source terminals are referred to ground) it is necessary to provide a gate voltage higher than the positive supply for the upper transistors because they have the drain connected to the supply itself.

This is obtained by a system that combines a charge pump circuit, which assures correct DC operation, with a boostrapping technique suitable for high switching frequencies.

In the boostrap circuit the external C_B capacitors are charged to a voltage of about 10V when the upper power transistor is OFF and the lower one is ON. To guarantee efficient driving of the upper power transistor in the conduction condition, the value of C_B must be greater than the value of the input capacitance, C_{IN}, of the power transistor itself. Since the estimated value of the input capacity is about 1nF, C_B should be $> = 10nF$ to guarantee correct operation.

An ON-OFF synchronization circuit provides a dead time (the period in which all four power transistors are OFF) of 40ns, sufficient to prevent simultaneous conduction with obvious advantages in terms of power dissipation and of spurious signals on the ground and in the sensing resistors.

A thermal protection circuit has been included that will disable the device if the junction temperature reaches 150°C. When the temperature has fallen to a safe value the device restarts under the control of the input and enable signals.

Fig. 1 - Intrinsic structures in the POWER DMOS transistors

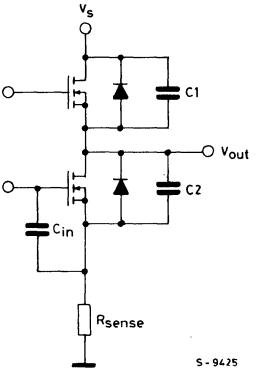


Fig. 2 - Typical current spikes on the sensing pin

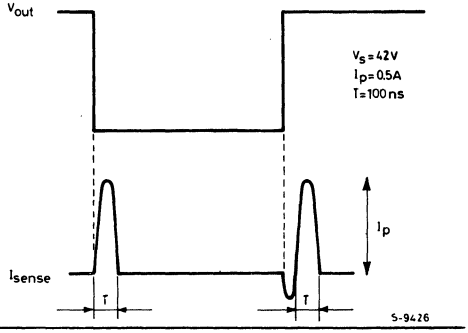
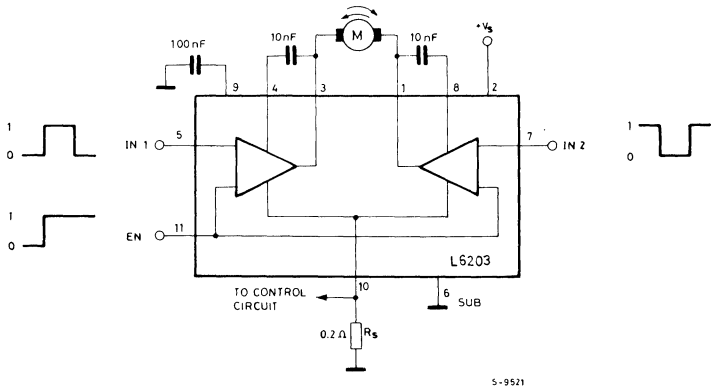


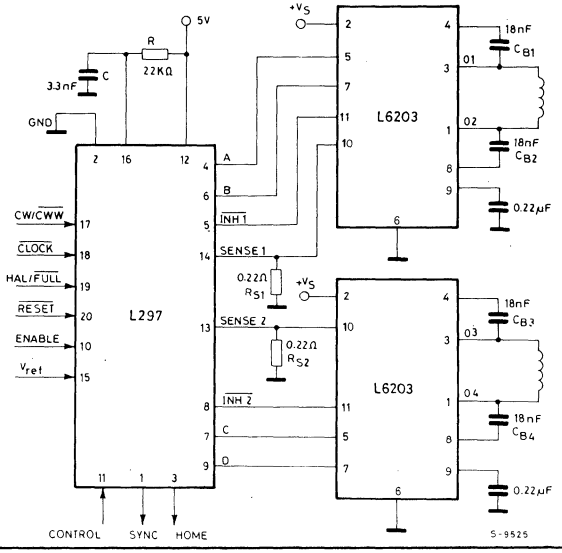
Fig. 7 - Bidirectionale DC motor control



INPUTS			FUNCTION
V_{EN} = H	IN1 = H	IN2 = L	Turn right
	IN1 = L	IN2 = H	Turn left
	IN1 = IN2		Fast motor stop
V_{EN} = L	IN1 = X	IN1 = IN2	Free running motor stop

L = Low H = High X = Don't care

Fig. 8 - Application circuit



L6207

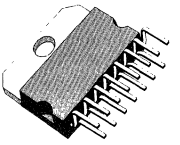
ADVANCE DATA

DUAL FULL BRIDGE DRIVER

- POWER SUPPLY VOLTAGE UP TO 46V
- LOW SATURATION VOLTAGE
- OVERTEMPERATURE PROTECTION
- LOGIC "0" INPUT VOLTAGE UP TO 1.5V (HIGH NOISE IMMUNITY)

The L6207 is an integrated monolithic circuit in a 15-lead multiwatt package. It is a high current dual full-bridge driver designed to accept standard TTL logic levels and drive inductive load such as relays, solenoids, DC and stepper motors.

Two inhibit inputs are provided to disable the device independently of the input signals. The emitters of the lower transistors of each bridge are connected togheter and the corresponding external terminal can be used for the connection of an external sensing resistor. An additional supply input is provided so that the logic works at a lower voltage.



Multiwatt 15

ORDERING NUMBER: L6207

BLOCK DIAGRAM

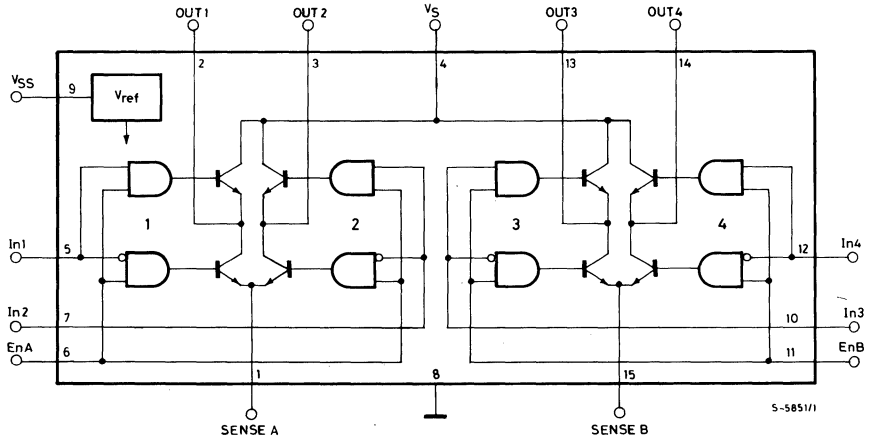
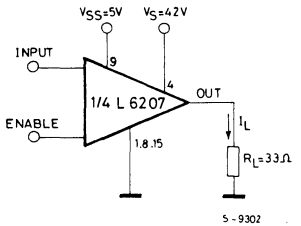


Fig. 1 - Switching times test circuit



note: For INPUT chopper, set EN = H

Fig. 1a - Source current delay times vs. input chopper

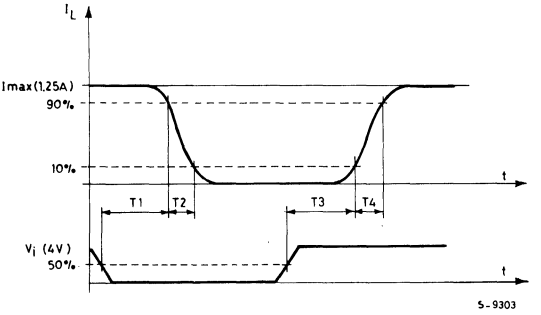
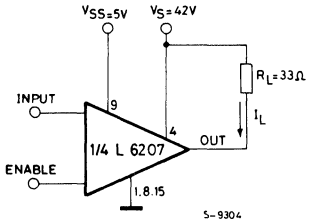
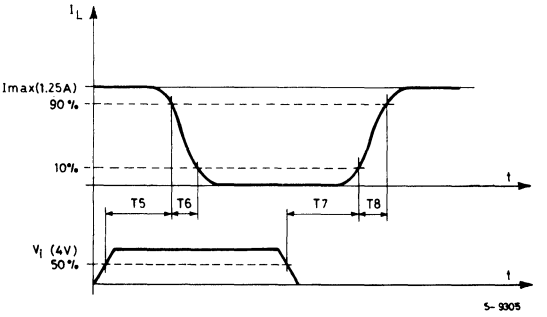


Fig. 2 - Switching time test circuits



note: For INPUT chopper, set EN = H

Fig. 2a - Sink current delay times vs. input chopper



ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
T5 (V_i)	Sink current turn-off delay	0.5 V_i to 0.9 I_L (***)		0.7		μs
T6 (V_i)	Sink current fall time	0.9 I_L to 0.1 I_L (***)		0.2		μs
T7 (V_i)	Sink current turn on delay	0.5 V_i to 0.1 I_L (***)		1.5		μs
T8 (V_i)	Sink current rise time	0.1 I_L to 0.9 I_L (***)		0.2		μs
f_C	Commutation frequency	I_L = 1.25A		25	40	KHz

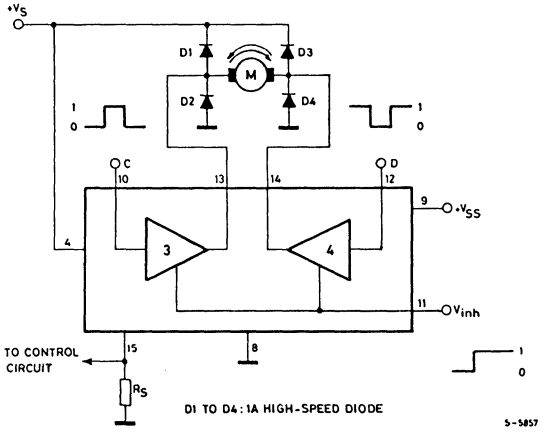
(*) Sensing voltage can be -1V for t < 50μs; in steady state $V_{sens\ min}$ > -0.5V; (**) See fig. 1a; (***) See fig. 2a

(1) The value of the current is related to only one channel

- The correct sequence for power on is:
  1. V_{SS} ON with EN = L
  2. V_S ON
  3. EN = H

  for power off is:
  1. EN = L
  2. V_S ON
  3. V_{SS} OFF

Fig. 3 - Bidirectional DC motor control



TRUTH TABLE

	INPUTS	FUNCTION
V_{EN} = H	C = H D = L	Turn right
	C = L D = H	Turn left
	C = D	Fast motor stop
V_{EN} = L	C = X D = X	Free running motor stop

L = Low H = High X = Don't care

L6209

ADVANCE DATA

3A FULL BRIDGE DRIVER WITH DIODES

- SUPPLY VOLTAGE UP TO 46V
- OUTPUT CURRENT UP TO 3A (4A PEAK)
- SEPARATE CONNECTIONS FOR SUPPLIES AND DIODES
- CONNECTION FOR EXTERNAL SENSE RESISTOR
- LOW SATURATION VOLTAGE (3.5V TYP AT 3A)
- THERMAL SHUT DOWN WITH HYSTERESIS
- μP COMPATIBLE LOGIC INPUTS W'TH HIGH NOISE IMMUNITY
- LOW LEAKAGE FAST RECOVERY DIODES
- NO CURRENT FROM HIGH VOLTAGE SUPPLIES WHEN ENABLE PIN IS LOW

The L6209 is a high voltage, high current full-bridge driver with internal fast recovery diodes.

The cathodes of the upper recirculation diodes and the anodes of the lower ones are externally available to allow flexibility in application.

The device is designed to accept standard TTL logic levels and drive inductive loads such as relays, solenoids, DC motors and stepping motors.

An enable input allows all four transistors of the bridge to be switched off independently of the input commands.

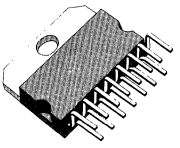
Each half bridge can be connected to an external sense resistor and have a separate high voltage supply.

An additional supply input is provided so that the logic can operate at a lower voltage, reducing dissipation.

The device is equipped with a thermal protection which, switches off the input and output stages when the temperature reaches 150°C and switches on with hysteresis when the temperature decreases.

Another important feature is the switching speed (less than 1.5μs).

The L6209 is supplied in a 15-lead Multiwatt® package.



Multiwatt-15

ORDERING NUMBER: L6209

BLOCK DIAGRAM

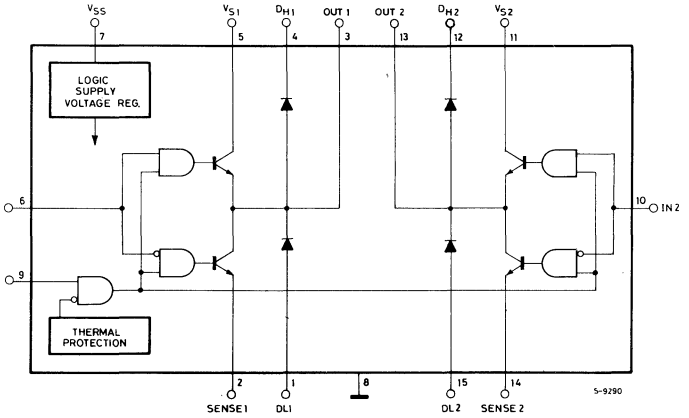
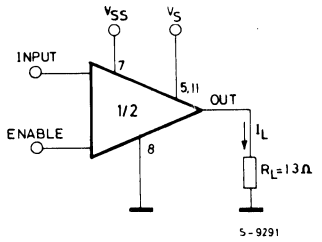


Fig. 1 - Switching times test circuits



Note: For INPUT chopper, set EN = H

Fig. 1a - Source current delay times vs. input chopper

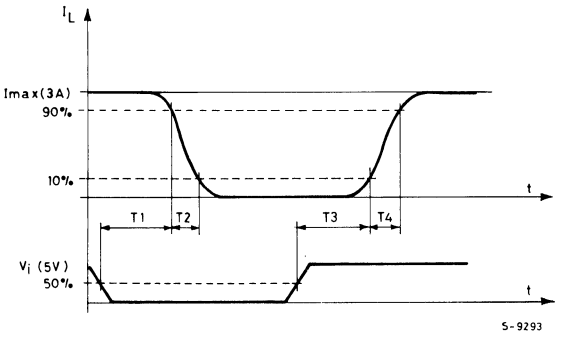
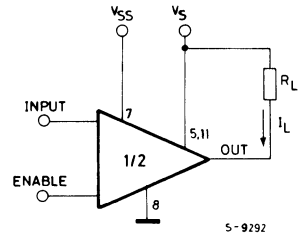


Fig. 2 - Switching times test circuits



Note: For INPUT chopper, set EN = H

Fig. 2a - Sink current delay times vs. input chopper

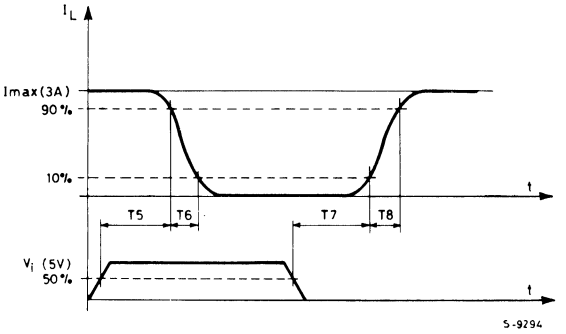
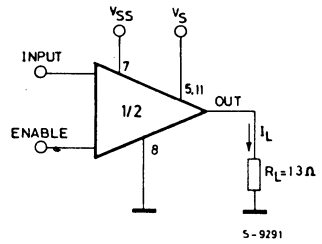
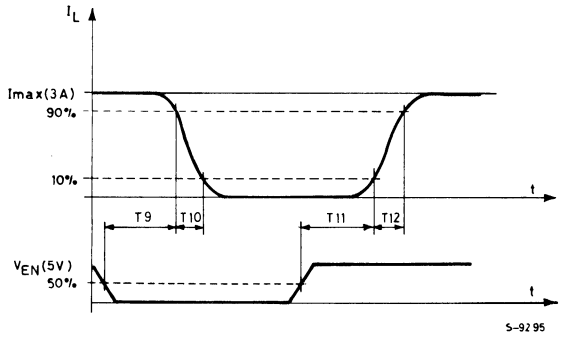


Fig. 3 - Switching times test circuits



Note: For enable chopper in this configuration, set, INPUT = H

Fig. 3a - Source current delay times vs. enable chopper.



ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
$V_{CE\ sat\ (L)}$	Saturation voltage	I_L = 1A		1		V
		I_L = 3A				
$V_{CE\ sat}$	Total drop	I_L = 1A		2.1	3	V
		I_L = 3A		3.5	4.5	
V_F	Diode forward voltage drop	I_O = 1A		1		V
		I_O = 3A		1.5		
t_{rr}	Diode reverse recovery time	I_f = 1A dI_f/dt = -50A/µs I_{RM} = 2.5A V_R = 42V		100		ns
t_{fr}	Diode forward recovery time	I_f = 1A dI_f/dt = 100A/µs Measured at V_F = 1V		100		ns
T1 (V_{IN})	Source current turn-off delay	0.5 V_i to 0.9 I_L (2)		750		ns
T2 (V_{IN})	Source current fall time	0.9 I_L to 0.1 I_L (2)		430		ns
T3 (V_{IN})	Source current turn-on delay	0.5 V_i to 0.1 I_L (2)		1.1		µs
T4 (V_{IN})	Source current rise time	0.1 I_L to 0.9 I_L (2)		500		ns
T5 (V_{IN})	Sink current turn-off delay	0.5 V_I to 0.9 I_L (3)		700		ns
T6 (V_{IN})	Sink current fall time	0.9 I_L to 0.1 I_L (3)		500		ns
T7 (V_{IN})	Sink current turn-on delay	0.5 V_i to 0.1 I_L (3)		950		ns
T8 (V_{IN})	Sink current rise time	0.1 I_L to 0.9 I_L (3)		400		ns
T9 (V_{IN})	Source current turn-off delay	0.5 V_i to 0.9 I_L (4)		450		ns
T10 (V_{IN})	Source current fall time	0.9 I_L to 0.1 I_L (4)		250		ns
T11 (V_{IN})	Source current turn-on delay	0.5 V_i to 0.1 I_L (4)		550		ns
T12 (V_{IN})	Source current rise time	0.1 I_L to 0.9 I_L (4)		250		ns
T13 (V_{IN})	Sink current turn-off delay	0.5 V_i to 0.9 I_L (5)		350		ns
T14 (V_{IN})	Sink current fall time	0.9 I_L to 0.1 I_L (5)		200		ns
T15 (V_{IN})	Sink current turn-on delay	0.5 V_i to 0.1 I_L (5)		800		ns
T16 (V_{IN})	Sink current rise time	0.1 I_L to 0.9 I_L (5)		200		ns
f_c	Commutation frequency	I_L = 3A		35	60	KHz

NOTE: (1) Sensing voltage can be -1V for t ⩽ 50µs; in steady state V_{sens} min ⩾ -0.5V
(2) See fig. 1a. (INPUT chopper)
(3) See fig. 2a. (INPUT chopper)
(4) See fig. 3a. (ENABLE chopper)
(5) See fig. 4a. (ENABLE chopper)

L6210

ADVANCE DATA

DUAL SCHOTTKY DIODE BRIDGE

- MONOLITHIC ARRAY OF EIGHT SCHOTTKY DIODES
- HIGH EFFICIENCY
- 4A PEAK CURRENT
- LOW FORWARD VOLTAGE
- FAST RECOVERY TIME
- TWO SEPARATED DIODE BRIDGES

The L6210 is a monolithic IC containing eight Schottky diodes arranged as two separated diode bridges.

This diodes connection makes this device versatile in many applications.

They are used particular in bipolar stepper motor applications, where high efficient operation, due to low forward voltage drop and fast reverse recovery time, are required.

The L6210 is available in a 16 Pin Powerdip Package (12+2+2) designed for the 0 to 70°C ambient temperature range.

Powerdip 12 + 2 + 2
(V6P2)

ORDERING NUMBER: L6210

ABSOLUTE MAXIMUM RATINGS

I_f	Repetitive forward current peak	2	A
V_r	Peak reverse voltage (per diode)	50	V
T_{amb}	Operating ambient temperature	70	°C
T_{stg}	Storage temperature range	-55 to 150	°C

BLOCK DIAGRAM

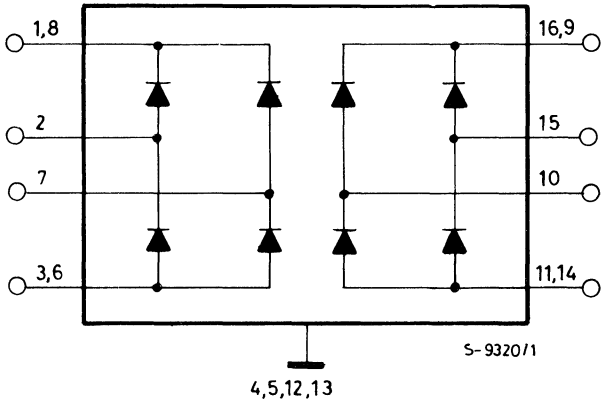


Fig. 1 - Reverse current vs. voltage

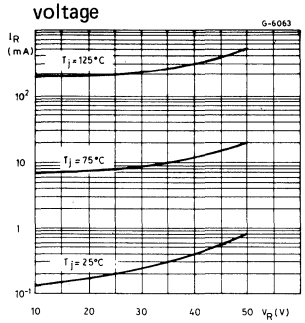
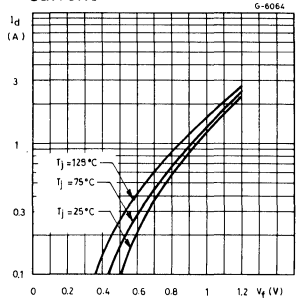


Fig. 2 - Forward voltage vs. current



MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ of the L6210 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board as shown in figure 3 or to an external heatsink (Figure 4).

During soldering the pin temperature must not exceed 260°C and the soldering time must not be longer then 12s. The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 3 - Example of P.C. board copper area which is used as heatsink

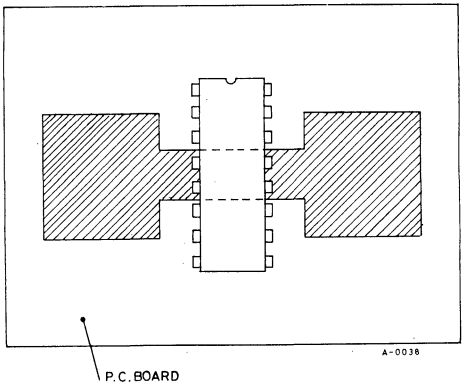
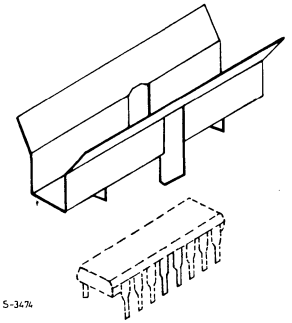


Fig. 4 - Example of an external heatsink



L6212

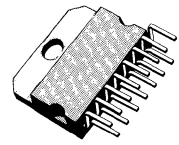
ADVANCE DATA

HIGH CURRENT SOLENOID DRIVER

- HIGH VOLTAGE OPERATION (UP TO 50V)
- HIGH OUTPUT CURRENT CAPABILITY (UP TO 6A)
- LOW SATURATION VOLTAGE
- TTL-COMPATIBLE INPUT
- OUTPUT SHORT CIRCUIT PROTECTION (TO GROUND, TO SUPPLY AND ACROSS THE LOAD)
- THERMAL SHUTDOWN
- OVERDRIVING PROTECTION
- LATCHED DIAGNOSTIC OUTPUT

The L6212 is a monolithic switch-mode solenoid driver designed for fast, high-current applications such as hammer driving in printers and electronic typewriters. Power dissipation is reduced by efficient switch-mode operation. An extra feature of the L6212 is a latched diagnostic output which indicates when the output is short circuit.

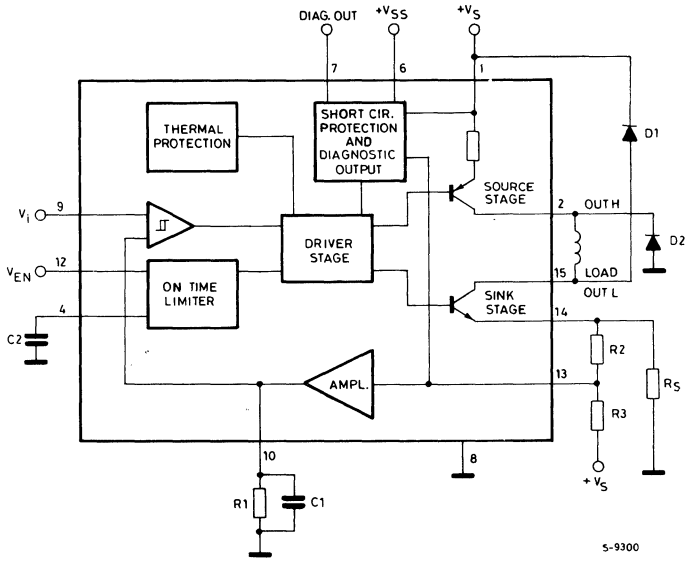
The L6212 is supplied in an 15-lead Multiwatt plastic power package.



Multiwatt-15

ORDERING NUMBER: L6212

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

(Refer to the test circuit, V_s = 37V, V_{ss} = 5V, T_{amb} = 25°C, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Power supply voltage (Pin 1)		12		46	V
I_d	Quiescent drain current	V_{EN} = H		20	30	mA
		$V_i \geq 0.6V$ V_{EN} = L		70		mA
V_{ss}	Logic supply voltage (Pin 6)		4.5		7	V
I_{ss}	Quiescent logic supply current	V_{DIAG} = L		5	8	mA
		DIAG Output at high impedance		10	100	μA
V_i	Input voltage (Pin 9)	Operating output	0.6			V
		Non-operative output			0.45	V
I_i	Input current (Pin 9)	$V_i \geq 0.6V$ $V_i \leq 0.45V$			-2 -5	μA μA
V_{ENABLE}	Enable input current (Pin 12)	Low level High level	-0.3 2.4		0.8	V
I_{ENABLE}	Enable input current	V_{EN} = L V_i = 0.8V V_{EN} = H V_e = 2.4V			-100 100	μA
$V_{sat\ H}$	Source output saturation volt.	I_p = 5.5A			2.5	V
$V_{sat\ L}$	Sink output saturation volt.	I_{out} = 5.5A			2.5	V
$V_{sat\ H} + V_{sat\ L}$	Total saturation voltage	I_{out} = 5.5A			4.5	V
$I_{leakage}$	Output leakage current source PNP	V_s = 45V $V_i \leq 0.45V$			2	mA
$I_{leakage}$	Output leakage current sink NPN	V_s = 45V $V_i \leq 0.45V$			2	mA
K	On time limiter constant (*)	V_{EN} = L		120		
V_{DIAG}	Diagnostic saturation voltage (Pin 7)	I_{DIAG} = 10mA			0.4	V
I_{DIAG}	Diagnostic leakage current (Pin 7)	V_{DIAG} = 40V			10	μA
$\frac{V_{pin\ 10}}{V_{pin\ 13}}$	OP AMP DC voltage gain	$V_{pin\ 13}$ = 100 to 800mV		5		
$V_{pin\ 10}$		$I_{pin\ 10}$ = 1mA	4.5			V
$I_{pin\ 10}$		$V_{pin\ 10}$ = 4V $V_9 = V_{13} = 0$ $V_{pin\ 10}$ = 2V V_{13} = 0.9V	1		10 1.5	μA mA
I_{sense}	Input bias current (Pin 13)			-1		μA
V_{sense}	Sensing voltage (Pin 14) (**)				0.9	V

(*) After a time interval $t_{max} = KC_2$, the output stages are disabled.
(**) Allowed range of V_{sense} without the intervention of the short circuit protection.

CIRCUIT OPERATION

The L6212 works as a transconductance amplifier: it can supply an output current directly proportional to an input voltage level (V_i). Furthermore, it allows complete switching control of the output current waveform (see Fig. 1).

The following explanation refers to the Block Diagram, to Fig. 1 and to the typical application circuit of Fig. 2.

The t_{on} time is fixed by the width of the Enable input signal (TTL compatible): it is active low and enables the output stages "source" and "sink". At the end of t_{on}, the load current I_{load} recirculates through D1 and D2, allowing fast current turn-off.

The rise time t_r depends on the load characteristics, on V_i and on the supply voltage value (V_s, pin 1).

During the t_{on} time, I_{load} is converter into a voltage signal by means of the external sensing resistance R_s connected to pin 13. This signal, amplified by the op amp charges the external RC network at pin 10 (R1, C1). The voltage at this pin is sensed by the inverting input of a comparator. The voltage on the non-inverting input of this one is fixed by the external voltage V_i (pin 9).

After, t_r, the comparator switches and the output stage "source" is switched off. The comparator output is confirmed by the voltage on the non-inverting input, which decreases of a constant fraction of V_i (1/10), allowing hysteresis operation. The current in the load now flows through D2.

Two cases are possible: the time constant of the recirculation phase is higher than R1, C1; the time constant is lower than R1, C1. In the first case, the voltage sensed on the non-inverting input of the comparator is just the value proportional to I_{load}. In the second case, when the current decreases too quickly, the comparator senses the voltage signal stored in the R1, C1 network.

In the first case t_1 depends on the load characteristics, while in the second case it depends only on the value of R1, C1.

In other words, R1, C1 fixed the minimum value of t_1 ($t_1 \geqslant 1/10$ R1 x C1. Note that C1 should be chosen in the range 2.7 to 10nF for stability reasons of the op amp).

After t_1, the comparator switches again: the output is confirmed by the voltage on the non-inverting input, which reaches V_i again (hysteresis).

Now the cycle starts again: t_2, t_4 and t_6 have the same characteristics as t_r, while t_3 and t_5 are similar to t_1. The peak current I_p depends on V_i as shown in the typical transfer function of Fig. 3.

It can be seen that for V_i lower than 450mV the device is not operating.

For V_i included between 450 and 600mV, the operation is not guaranteed.

The other parts of the device have protection and diagnostic functions. At pin 4 is connected an external capacitor C2, charged at constant current when the Enable is low.

After a time interval equal to K · C1 (K is defined in the table of Electrical Characteristics and has the dimensions of Ω) the output stages are switched off independently by the Input signal.

This avoids the load being driven in conduction for an excessive period of time (overdriving protection).

The action of this protection is shown in Fig. 1b. Note that the voltage ramp at pin 4 starts whenever the Enable signal becomes active (low state), regardless of the Input signal. To reset pin 4 and to restore the normal conditions, pin 12 must return high. This protection can be disabled by grounding pin 4.

In order to keep constant the energy delivered to the load, when the supply voltage changes, it's possible to modify the output maximum peak current (I_p) by means the external voltage divider R2 and R3 which "senses" the supply voltage.

I_p is given by:

$$I_p = \frac{V_i\,(R_s + R2 + R3) - 5\,V_s\,(R2 + R_s)}{5\,R3\,R_s}$$

so the variation of I_p versus V_s is:

L6217

ADVANCE DATA

STEPPER MOTOR DRIVER

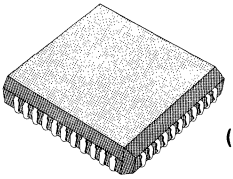
- MICROSTEPPING
- BIPOLAR OUTPUT CURRENT UP TO 400mA
- LOW SATURATION VOLTAGE
- BUILT-IN FAST RECOVERY DIODES
- OUTPUT CURRENT DIGITALLY PROGRAMMABLE
- 6 BIT D/A CONVERTERS SET OUTPUT CURRENT
- THERMAL SHUTDOWN

The L6217 is a monolithic IC that controls and drives both phases of a Bipolar Stepper Motor with PWM control of the phase current. The output current level of each phase is programmed by a 6 bit D/A converter so that the device may be used in full-step, half-step and micro-step applications. The inputs for the D/A converters and the phase inputs to select the direction of current flow are latched to minimize the interface to a microprocessor.

The power section of the device is a dual H-Bridge drive with internal clamp diodes for current recirculation. To maintain the degree of accuracy required for micro-stepping, the motor current is internally sensed and compared to the output of the D/A converter.

A monostable, programmed by and RC network sets the motor current decay time.

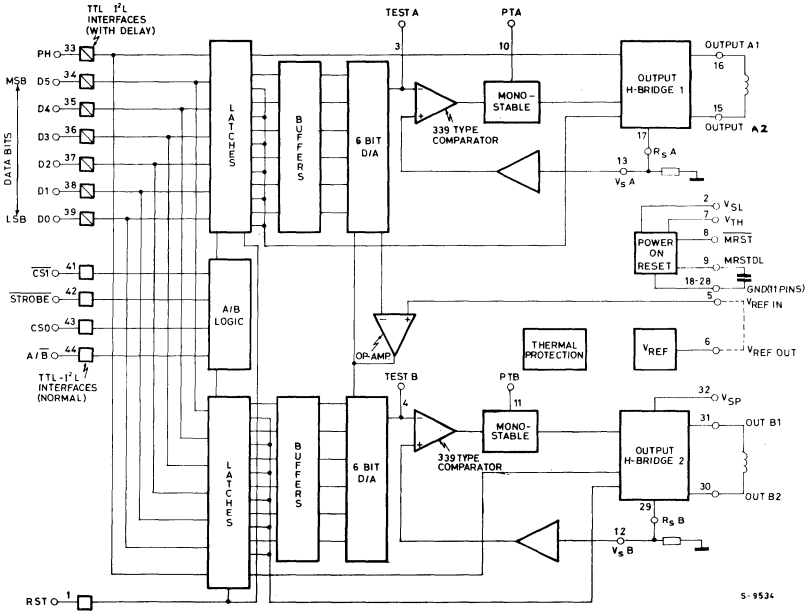
The L6217 is supplied in a 44 pin PLCC with 11 of the 44 pins used for heatsinking.



PLCC 44
(Plastic Chip-Carrier)

ORDERING NUMBER: L6217

BLOCK DIAGRAM



PIN FUNCTION DESCRIPTION

N°	NAME	FUNCTION
1	$\overline{R_{st}}$	Active low input resets the D/A latches to 0 and disables the output.
38, 39	D0 - D5	Data inputs for the D/A converter. (D0 = LSB) For a data input of 00, the corresponding outputs are held in the off state.
44	A/B	Channel select for input data. Pin A/$\overline{B}$ selects channel A when high.
33	PH	Logic input selects direction of current flow in output bridge from A1 (B1) to A2 (B2) for PH = 1.
42	$\overline{\text{Strobe}}$	Active low input latches input data (D0 - D5 and PH) into input latch.
9	MRST DL	The capacitor on this pin programs the power on reset delay according to the formula: $t_d = (0.35)\ (C)\ 10^6$
8	$\overline{\text{MRST}}$	Power-on reset circuit output. (Micro reset signal). This output remains low from power on until the delay capacitor has charged past the delay threshold.
10	P_tA	Pulse time A, an external parallel RC network tied to ground defines t_{off} time for channel A. (t_{off} = 0.69 R2C2).
11	P_tB	Pulse time B, an external parallel RC network tied to ground defines toll time for channel B. (t_{off} = 0.69 R3C3).
5	$V_{ref\ in}$	Voltage applied to this point sets the reference for the D/A converter and threfore sets the maximum output current. (See equation 1, next two pages).
18 to 28	Gnd	Ground connection and also conducts heat to the P.C. board.
40	Gnd 0	Pin must be connected to ground.
2	V_{sl}	Logic supply voltage
32	V_{sp}	Motor supply voltage

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
MONOSTABLE						
t_{off}	Cutoff time	R_t = 56KΩ C_t = 820pF	27		37	μs
t_d	Turn-off delay				2	μs
I_{off}	Output leakage current	Data = 00 (Hex)			100	μA
RESET CIRCUITRY						
V_{th}	Reset threshold voltage		3.9	4.1	4.3	V
	Reset threshold hysteresis		70	100		mV
I_{so}	Delay capacitor charging current	V_C = 2.5V	7	10	14	μA
I_{sl}	Delay capacitor discharge current	V_C = 2.5V	10			mA
V_{dth}	Delay threshold voltage		3.25	3.5	3.75	V
V_{dhys}	Hysteresis voltage on delay threshold		70	100		mV
I_{ol}	Output leakage current	V_O = 5V			200	μA
V_{sat}	Output saturation of reset out	I_O = 2mA			0.4	V
SOURCE DIODE-TRANSISTOR PAIRS						
V_{sat}	Saturation voltage	I_O = 400mA		1.3	1.8	V
V_f	Diode forward voltage	I_O = 400mA		0.8	1.2	V
SINK DIODE-TRANSISTOR PAIRS						
V_{sat}	Saturation voltage	I_O = 400mA		1.1	1.5	V
V_f	Diode Forward voltage	I_O = 400mA		0.6	1.0	V
AC CHARACTERISTICS						
t_s	Set-up time				100	ns
t_h	Hold time				500	ns
t_w	Minimum input pulse width				600	ns

CIRCUIT OPERATION

The current control section of the L6217 is a pulse width modulated control that senses the motor current. When the motor current reaches the peak programmed current the comparator will trigger the monostable turning off the upper transistors. After the t_{off} time equal to 0.69 RC the upper drivers are enabled again.

The peak current is given by the equation:

When the input data is 00, the output stages are disabled by internal logic so that the output current decays rapidly to zero.

An internal generated lockout time avoids the use of an external RC network between the sensing resistor (R_sA, R_sB) and the corresponding input (V_sA, V_sB), by disabling the comparator sensing during the lockout time. This time is typically 2.5ms.

$$I_{op} = \frac{V_{ref}}{4.69 \cdot R_{sense}} \cdot \frac{D}{64}$$

D = Input data (0 - 63)

Fig. 4 - Motor current (half step mode)

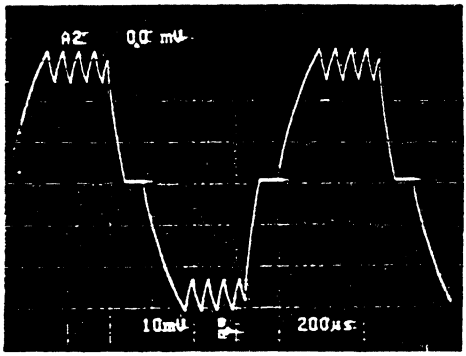


Fig. 5 - Monostable voltage and motor current repetitive steps.

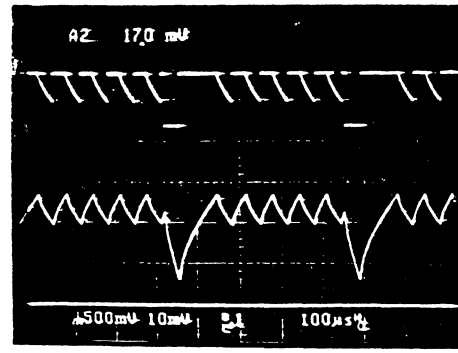
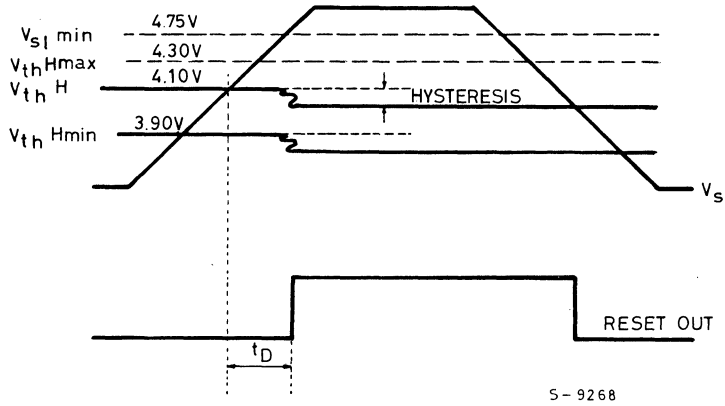


Fig. 6 - Reset waveforms



L6217A

ADVANCE DATA

STEPPER MOTOR DRIVER

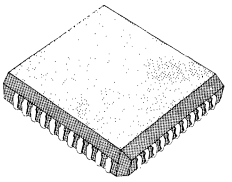
- MICROSTEPPING
- BIPOLAR OUTPUT CURRENT UP TO 400mA
- LOW SATURATION VOLTAGE
- BUILT-IN FAST RECOVERY DIODES
- OUTPUT CURRENT DIGITALLY PROGRAMMABLE
- 7 BIT D/A CONVERTERS SET OUTPUT CURRENT
- THERMAL SHUTDOWN

The L6217A is a monolithic IC that controls and drives both phases of a Bipolar Stepper Motor with PWM control of the phase current. The output current level of each phase is programmed by a 7 bit D/A converter so that the device may be used in full-step, half-step and micro-step applications. The inputs for the D/A converters and the phase inputs to select the direction of current flow are latched to minimize the interface to a microprocessor.

The power section of the device is a dual H-Bridge drive with internal clamp diodes for current recirculation. To maintain the degree of accuracy required for microstepping, the motor current is internally sensed and compared to the output of the D/A converter.

A monostable, programmed by and RC network sets the motor current decay time.

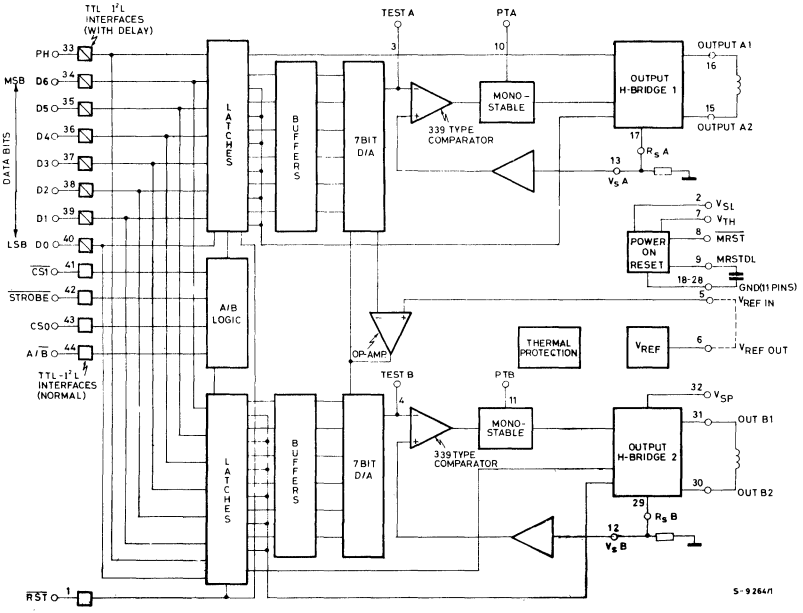
The L6217A is supplied in a 44 pin in PLCC with 11 of the 44 pins used for heatsinking.



PLCC 44
(Plastic Chip-Carrier)

ORDERING NUMBER: L6217A

BLOCK DIAGRAM



PIN FUNCTION DESCRIPTION

N°	NAME	FUNCTION
1	$\overline{R_{st}}$	Active low input resets the D/A latches to 0 and disables the output.
40, 34	D0 - D6	Data inputs for the D/A converter. (D0 = LSB) For a data input of 00, the corresponding outputs are held in the off state.
44	A/$\overline{B}$	Channel select for input data. Pin A/$\overline{B}$ selects channel A when high.
33	PH	Logic input selects direction of current flow in output bridge from A1 (B1) to A2 (B2) for PH = 1.
42	$\overline{Strobe}$	Active low input latches input data (D0 - D5 and PH) into input latch.
9	MRST DL	The capacitor on this pin programs the power on reset delay according to the formula: $t_d = (0.35)\ (C)\ 10^6$
8	$\overline{MRST}$	Power-on reset circuit output. (Micro reset signal). This output remains low from power on until the delay capacitor has charged past the delay threshold.
10	P_tA	Pulse time A, an external parallel RC network tied to ground defines t_{off} time for channel A. (t_{off} = 0.69 R2C2).
11	P_tB	Pulse time B, an external parallel RC network tied to ground defines t_{off} time for channel B. (t_{off} = 0.69 R2C2)
5	$V_{ref\ in}$	Voltage applied to this point sets the reference for the D/A converter and threfore sets the maximum output current. (See equation 1, next two pages).
18 to 28	Gnd	Ground connection and also conduct heat to the P.C. board.
2	V_{sl}	Logic supply voltage
32	V_{sp}	Motor supply voltage
16, 15 31, 30	Out A1-A2 B1-B2	H-Bridge outputs.

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
MONOSTABLE						
t_{off}	Cutoff time	R_t = 56KΩ C_t = 820pF	27		37	μs
t_d	Turn-off delay				2	μs
I_{off}	Output leakage current	Data = 00 (Hex)			100	μA
RESET CIRCUITRY						
V_{th}	Reset threshold voltage		3.9	4.1	4.3	V
	Reset threshold hysteresis		70	100		mV
I_{so}	Delay capacitor charging current	V_C = 2.5V	7	10	14	μA
I_{si}	Delay capacitor discharge current	V_C = 2.5V	10			mA
V_{dth}	Delay threshold voltage		3.25	3.5	3.75	V
V_{dhys}	Hysteresis voltage on delay threshold		70	100		mV
I_{ol}	Output leakage current	V_O = 5V			200	μA
V_{sat}	Output saturation of reset out	I_O = 2mA			0.4	V
SOURCE DIODE-TRANSISTOR PAIRS						
V_{sat}	Saturation voltage	I_O = 400mA		1.3	1.8	V
V_f	Diode forward voltage	I_O = 400mA		0.8	1.2	V
SINK DIODE-TRANSISTOR PAIRS						
V_{sat}	Saturation voltage	I_O = 400mA		1.1	1.5	V
V_f	Diode Forward voltage	I_O = 400mA		0.6	1.0	V
AC CHARACTERISTICS						
t_s	Set-up time				100	ns
t_h	Hold time				500	ns
t_w	Minimum input pulse width				600	ns

CIRCUIT OPERATION

The current control section of the L6217A is a pulse width modulated control that senses the motor current. When the motor current reaches the peak programmed current the comparator will trigger the monostable turning off the upper transistors. After the t_{off} time equal to 0.69 RC the upper drivers are enabled again.

The peak current is given by the equation:

$$I_{op} = \frac{V_{ref}}{4.69 \cdot R_{sense}} \cdot \frac{D}{128}$$

D = Input data (0 - 7F H)

When the input data is 00, the output stages are disabled by internal logic so that the output current decays rapidly to zero.

An internal generated lockout time avoids the use of an external RC network between the sensing resistor (R_sA, R_sB) and the corresponding input (V_sA, V_sB), by disabling the comparator sensing during the lockout time. This time is typically 2.5μs.

Fig. 4 - Motor current (half step mode)

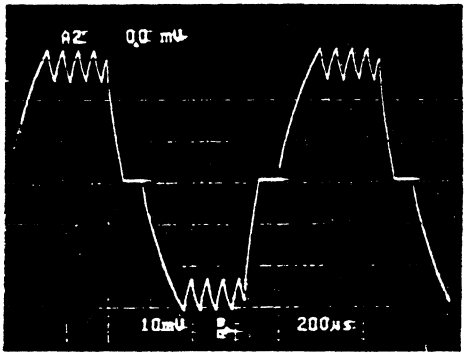


Fig. 5 - Monostable voltage and motor current for repetitive steps.

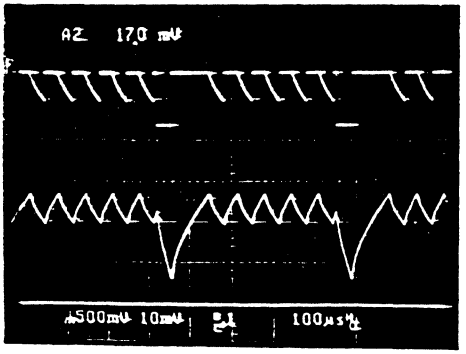
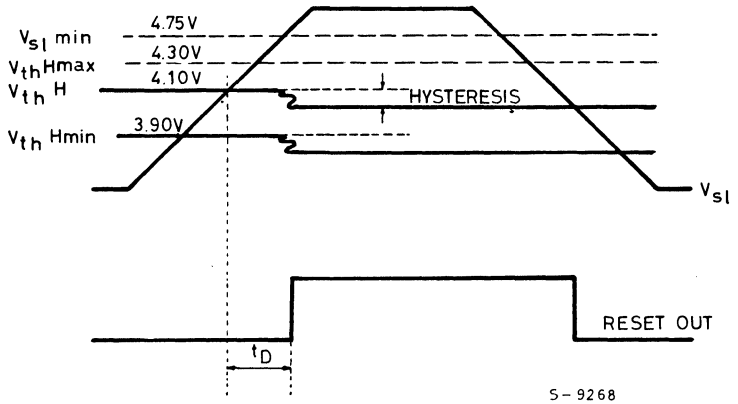


Fig. 6 - Reset waveforms



L6221A
L6221N

ADVANCE DATA

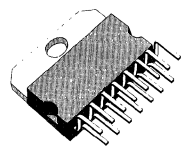
QUAD DARLINGTON SWITCHES

- OUTPUT VOLTAGE TO 50V
- OUTPUT CURRENT TO 1.8A
- VERY LOW SATURATION VOLTAGE
- TTL COMPATIBLE INPUTS
- INTEGRAL FAST RECIRCULATION DIODES

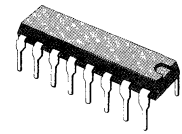
The L6221 monolithic quad darlington switch is designed for high current, high voltage switching applications. Each of the four switches is controlled by a logic input and all four are controlled by a common enable input. All inputs are TTL-compatible for direct connection to logic circuits.

Each switch consists of an open-collector darlington transistor plus a fast diode for switching applications with inductive loads. The emitters of the four switches are commoned. Any number of inputs and outputs of the same device may be paralleled.

Two versions are available: the L6221A mounted in a Powerdip 12+2+ 2 package and the L6221N mounted in a 15-lead Multiwatt package.



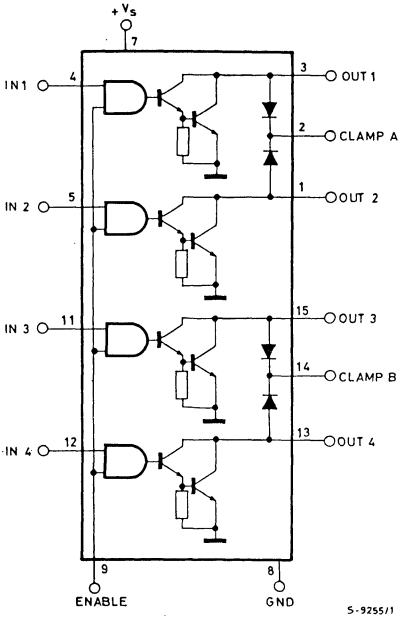
Multiwatt 15



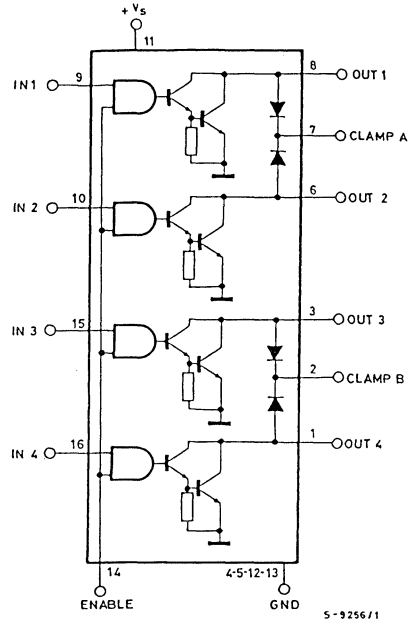
Powerdip 12 + 2 + 2
(V6P2)

ORDERING NUMBER :
L6221N L6221A

BLOCK DIAGRAMS



L6221N
Multiwatt



L6221A
Powerdip

PIN FUNCTIONS

L6221N Multiwatt	L6221A Powerdip	Name	Function
4	9	IN 1	Input to driver 1
5	10	IN 2	Input to driver 2
3	8	OUT 1	Output of driver 1
1	6	OUT 2	Output of driver 2
2	7	CLAMP A	Diode clamp to driver 1 and driver 2
11	15	IN 3	Input to driver 3
12	16	IN 4	Input to driver 4
15	3	OUT 3	Output of driver 3
13	1	OUT 4	Output of driver 4
14	2	CLAMP B	Diode clamp to driver 3 and driver 4
9	14	ENABLE	Enable input to all drivers
7	11	V_{SS}	Logic supply voltage
8	4	GND	Ground
–	5	GND	Ground
–	12	GND	Ground
–	13	GND	Ground
6	–	NC	Not connected
10	–	NC	Not connected

L6222

ADVANCE DATA

QUAD TRANSISTOR SWITCH

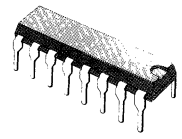
- OUTPUT VOLTAGE TO 50V
- OUTPUT CURRENT TO 1.2A
- VERY LOW SATURATION VOLTAGE
- TTL COMPATIBLE INPUTS
- INTEGRAL SUPPRESSION DIODE

The L6222 monolithic quad transistor switch is designed for high current, high voltage switching applications.

Each of the four switches is controlled by a logic input and all four are controlled by a common enable input. All inputs are TTL-compatible for direct connection to logic circuits. Each switch consists of an open-collector transistor plus a clamp diode for applications with inductive loads.

The emitters of the four switches are commoned. Any number of inputs and outputs of the same device may be paralleled.

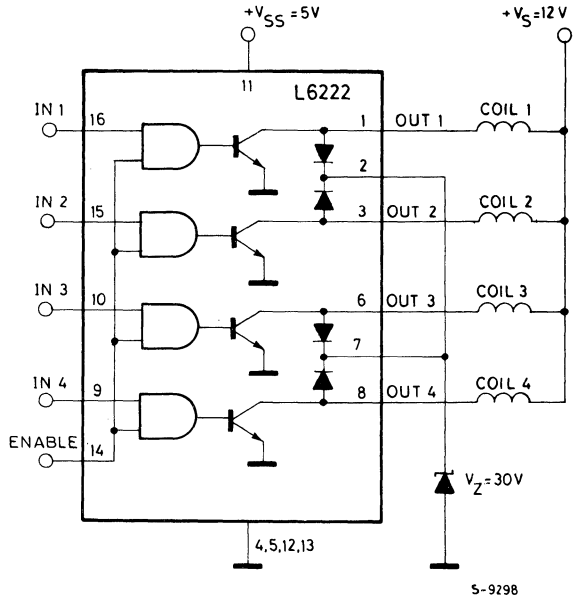
This device is intended to drive coils such as relays, solenoids, unipolar stepper motors, LED, etc.



Powerdip 12 + 2 + 2
(V6P2)

ORDERING NUMBER: L6222

Fig. 1 - Unipolar stepper motor drive



ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_{SS}	Logic supply voltage			4.50		7	V
$V_{CE(sus)}$	Output sustaining voltage	V_{IN} = 0.8V I_C = 100mA		46			V
I_{CEX}	Output leakage current	V_{CE} = 50V V_{IN} = 0.8V				1	mA
$V_{CE(sat)}$	Collector emitter saturation voltage	$V_{IN} \geqslant$ 2.0V	I_C = 0.1A			0.2	V
			I_C = 0.4A			0.5	
			I_C = 0.7A			0.9	
V_{IL}	Input low voltage					0.8	V
I_{IL}	Input low current	V_{IN} = 0.4V				-100	μA
V_{IH}	Input high voltage			2.0			V
I_{IH}	Input high current	$V_{IN} \geqslant$ 2.0V				± 10	μA
I_S	Logic supply current	V_{SS} = 5V	All outputs ON I_C = 0.7A		50	85	mA
			All outputs OFF		8		mA
I_R	Clamp diode leakage current	V_R = 50V				100	μA
V_F	Clamp diode forward voltage	I_F = 0.7A				1.6	V
		I_F = 1.2A				2.0	

L6230

ADVANCE DATA

BIDIRECTIONAL THREE-PHASE BRUSHLESS DC MOTOR DRIVER

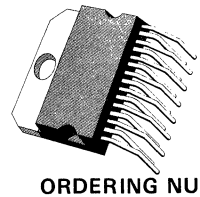
- 3A OUTPUT CURRENT, CONTROLLED IN LINEAR MODE
- SUPPLY VOLTAGE UP TO 18V
- COMPATIBLE WITH ANI F-TO-V CONVERTER AND PLL SPEED CONTROL SYSTEM
- SLEW RATE LIMITING FOR EMI REDUCTION
- CONNECTS DIRECTLY TO HALL EFFECT CELLS
- THERMAL SHUTDOWN WITH HYSTERESIS
- THREE-STATE OPERATION ALLOWS NEGLIGIBLE POWER DISSIPATION DURING 1/3f CYCLE
- INTERNAL PROTECTION DIODES
- FEW EXTERNAL COMPONENTS

The L6230 is a single-chip driver for three-phase brushless DC motors capable of delivering 3A output current with supply voltages to 18V. Designed to accept differential input from the Hall effect sensors, the device drives the three phases of a brushless DC motor and includes all the commutation logic required for a three phase bidirectional drive. Both delta and wye configurations may be used.

To limit EMI esmission the L6230 operates in a linear mode and controls the rise and fall times of the output stage. In addition the device is designed to limit power dissipation: during recirculation the output stage is switched to an off state, reducing dissipation to a very low value and minimizing torque ripple.

A speed control input controls the base current to the lower transistors to limit the motor current and hence control the speed. Any type of speed control system, including F to V and PLL systems, may be used with the L6230 by providing an analog signal at this input. The motor current may be sensed by an external resistor connected to a sensing pin on the device.

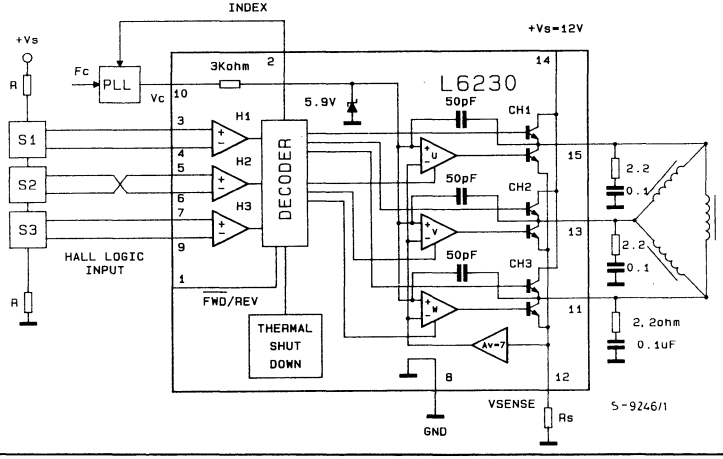
The power stage of the device is designed to eliminate the possibility of simultaneous conduction of the upper and lower power transistors of one output driver, when operating in the right loop.



Multiwatt-15
(Horizontal)

ORDERING NUMBER: L6230H

BLOCK DIAGRAM



PIN FUNCTIONS

N°	NAME	I/O	FUNCTION
1	FWD/REV	I	Direction Control. When this pin is low, the motor will run in the forward direction. A high will drive the motor in the reverse direction. Direction is defined by the position of the sensors in the motor.
2	INDEX	O	Signal pulse proportional to the motor speed. In PLL speed control applications, this is the feedback to the PLL. One pulse per electrical rotation. This is an open collector output.
3	H1 (+)	I	Positive input of differential amplifier on channel 1. Interfaces with Hall Effect sensor, S1, from motor.
4	H1 (-)	I	Negative input of differential amplifier on channel 1. Interfaces with Hall Effect sensor, S1, from motor.
5	H2 (+)	I	Same as pin 3 for channel 2.
6	H2 (-)	I	Same as pin 4 for channel 2.
7	H3 (+)	I	Same as pin 3 for channel 3.
8	GND		Ground connection.
9	H3 (-)	I	Same as pin 4 for channel 3.
10	V_C	I	Speed control input. Connected to output of PLL in PLL speed control applications.
11	OUT3	O	Output motor drive for phase 3.
12	SENSE	I	Current Sensing. Input for load current sense voltage for output stage.
13	OUT2	O	Output motor drive for phase 2.
14	V_S		Motor supply voltage.
15	OUT1	O	Output motor drive for phase 1.

DESCRIPTION

The L6230 is a three-phase brushless motor driver IC containing all the power stages and commutation logic required for a three-phase bidirectional drive.

Logic signals from the motor's Hall effect sensors are decoded to generate the correct driving sequence according to the truth-table of Fig. 1.

The direction of rotation is controlled by the forward/reverse input (pin 1). When this pin is at a low level the motor rotates in the forward direction.

When one of the push-pull output drivers is activated the upper transistor is always in saturation while the lower transistor is controlled in linear mode to set the desired speed in steady state conditions.

In PLL speed control applications the device provides a signal proportional to the motor speed at pin 2 (it is the buffered H1 input). The output of the PLL is connected to the speed control input on the device at pin 10, V_C.

In addition, a 1V offset is added to the speed demand voltage to match the minimum output of the PLL.

An external resistor, R_s, senses the output stage current. The sensing voltage across this resistor is amplified in the device by a factor of 7 to allow a reduction in the voltage drop in the resistor.

The amplified sensing voltage is then compared with the speed demand signal from the PLL and the resulting error signal sets the amplifier output accordingly.

The output current is related to the speed control voltage by:

$$I_o = (V_C - 1) / 7\ R_s$$

The value of the sensing resistor is given by:

$$R_s = (V_X - 1) / (7\ I_{max})$$

where V_X is the full scale voltage of V_C (see fig. 2).

In this way the V_C/I_{out} characteristics can be modified as shown in Fig. 2. Note that V_X max is clamped at 5.9V.

The most important feature of the L6230 is slew rate control. With this device a typical value of 0.1V/μs is achieved, reducing EMI to a very low value.

In a delta configuration a key feature is three-state operation; when the current is recirculating the corresponding phase driver is switched off and power dissipation is negligible. Current recirculates through the integrated free-wheeling diodes in the acceleration phase and through the motor in steady-state conditions. Torque ripple is also minimized.

The L6230 can also operate with a brushless motor connected in a star configuration, leaving the center floating.

The Hall inputs are ground compatible comparators and can work with direct active digital Hall signals on three terminals (of the same polarity) and a TTL level on the other three terminals.

Fig. 1 - **TRUTH TABLE FOR FORWARD ROTATION**

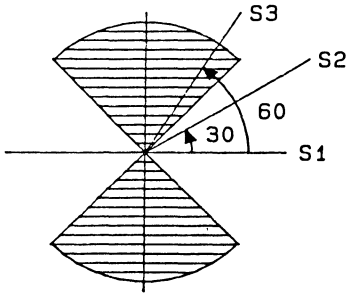
HALL EFFECT DIFF. INPUT 1 = POSITIVE 0 = NEGATIVE			UPPER DRIVER STATUS 1 = ON 0 = OFF			LOWER DRIVER STATUS 1 = ON 0 = OFF		
H1	H2	H3	UD1	UD2	UD3	LD1	LD2	LD3
1	0	0	1	0	0	0	0	1
1	1	0	0	1	0	0	0	1
1	1	1	0	1	0	1	0	0
0	1	1	0	0	1	1	0	0
0	0	1	0	0	1	0	1	0
0	0	0	1	0	0	0	1	0

DETERMINING HALL EFFECT SENSOR CODING

The L6230 assumes that the positioning of the Hall Effect sensors in a three-phase brushless DC bipolar motor are at 30 intervals. One can imagine two "windows" on the rotor each of which is 90 wide and 180 apart, see fig. 4. As a window passes over a sensor, the sensor output goes high. The timing diagram, fig. 3, shows the waveforms produced. These waveforms must appear at the Hall Effect Inputs of the L6230. Note that the rotation in fig. 4 must be counter-clockwise for forward rotation of the motor in whatever manner that is defined for the motor.

Fig. 4 is a stylized concept for determining the Hall Effect code pattern and does not reflect the actual direction of rotation of the motor in a physical sense. If a motor is chosen whose sensor outputs do not match the L6230 desired input pattern, a signal set conversion must be determined. It is helpful to visualize this by developing a diagram similar to that of fig. 4.

Fig. 4



For example, let us ecamine the output pattern of a different type of motor (fig. 5). Assuming 90 windows at 180 intervals, then with respect to fig. 4, a similar diagram, fig. 6, results in sensors 60 apart with the windows rotating clockwise. This situation results in a "forward" rotation of the motor.

Since S3 is the first sensor encountered by the window in fig. 6, this should be used for the L6230 Hall Effect Input, H1. After 30 of rotation CW, the H2 input of the L6230 must go high. The inverse of S1 from the motor would satisfy this. After an additional 30 of rotation, the H3 input must go high. The S2 sensor is encountered by the window. Thus, S2 is applied to this input, H3. By continuing around the diagram, one can develop a pattern which matches that for the L6230.

Fig. 5

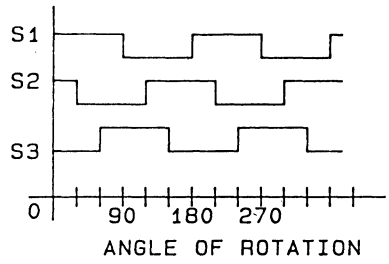
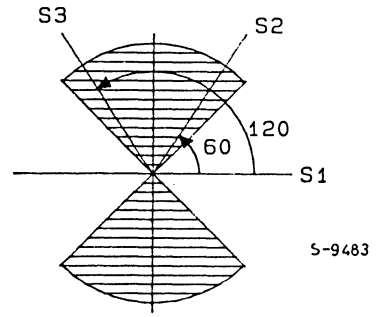


Fig. 6



Thus, the conversion table for this particular motor is:

Motor Sensors	L6230 Inputs
S3	H1
S1	H2
S2	H3

Note, for the inverted signal from S1 an actual inverter gate is not necessary with the L6230. Since the L6230 has differential inputs, the negative input pin may be used. Therefore, with TTL compatible Hall Effect sensors, the positive input is connected to a reference point along with the other negative inputs.

L6231

ADVANCE DATA

THREE-PHASE BRUSHLESS DC MOTOR DRIVER

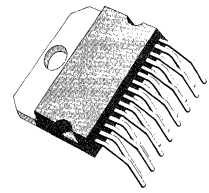
- 3A OUTPUT CURRENT, CONTROLLED IN LINEAR MODE
- SUPPLY VOLTAGE UP TO 18V
- COMPATIBLE WITH ANI F-TO-V CONVERTER AND PLL SPEED CONTROL SYSTEM
- INHIBIT FUNCTION
- SLEW RATE LIMITING FOR EMI REDUCTION
- CONNECTS DIRECTLY TO HALL EFFECT CELLS
- THERMAL SHUTDOWN WITH HYSTERESIS
- THREE-STATE OPERATION ALLOWS NEGLIGIBLE POWER DISSIPATION DURING 1/3f CYCLE
- INTERNAL PROTECTION DIODES
- FEW EXTERNAL COMPONENTS

The L6231 is a single-chip driver for three-phase brushless DC motors capable of delivering 3A output current with supply voltages to 18V. Designed to accept differential input from the Hall effect sensors, the device drives the three phases of a brushless DC motor and includes all the commutation logic required for a three phase drive.

To limit EMI emission the L6231 controls the rise and fall times of the output stage. In addition the device is designed to limit power dissipation: during recirculation the output stage is switched to an off state, reducing dissipation to a very low value and minimizing torque ripple.

A speed control input controls the base current to the lower transistors to limit the motor current and hence control the speed. Any type of speed control system, including F to V and PLL systems, may be used with the L6231 by providing an analog signal at this input. The motor current may be sensed by an external resistor connected to a sensing pin on the device.

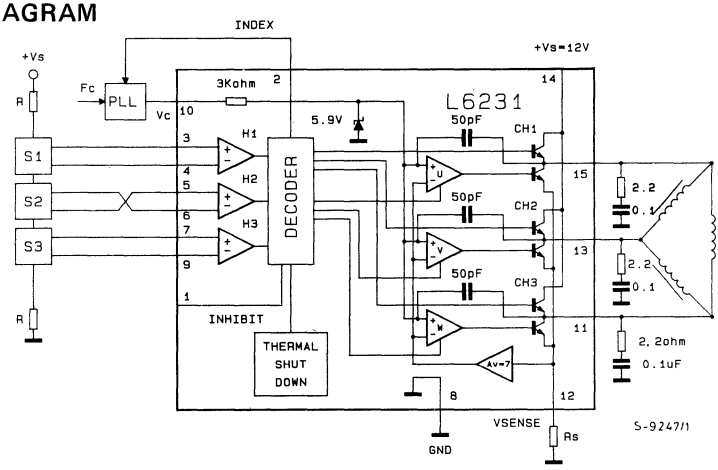
The power stage of the device is designed to eliminate the possibility of simultaneous conduction of the upper and lower power transistors of one output driver, when operating in the right loop.



Multiwatt-15
(Horizontal)

ORDERING NUMBER: L6231H

BLOCK DIAGRAM



PIN FUNCTIONS

N°	NAME	I/O	FUNCTION
1	INHIBIT	I	Output stage inhibit. When this pin is high all three output stages are in a high impedance state!
2	INDEX	O	Signal pulse proportional to the motor speed. In PLL speed control applications, this is the feedback to the PLL. One pulse per electrical rotation. This is an open collector output.
3	H1 (+)	I	Positive input of differential amplifier on channel 1. Interfaces with Hall Effect sensor, S1, from motor.
4	H1 (-)	I	Negative input of differential amplifier on channel 1. Interfaces with Hall Effect sensor, S1, from motor.
5	H2 (+)	I	Same as pin 3 for channel 2.
6	H2 (-)	I	Same as pin 4 for channel 2.
7	H3 (+)	I	Same as pin 3 for channel 3.
8	GND		Ground connection.
9	H3 (-)	I	Same as pin 4 for channel 3.
10	V_C	I	Speed control input. Connected to output of PLL in PLL speed control applications.
11	Out 3	O	Output motor drive for phase 3.
12	Sense	I	Current Sensing. Input for load current sense voltage for output stage.
13	Out 2	O	Output motor drive for phase 2.
14	V_S		Motor supply voltage.
15	Out 1	O	Output motor drive for phase 1.

DESCRIPTION

The L6231 is a three-phase brushless motor driver IC containing all the power stages and commutation logic required for a three-phase drive. When the INHIBIT INPUT is high all three OUTPUTS ARE PLACED in a high - IMPEDANCE STATE.

Logic signals from the motor's Hall effect sensors are decoded to generate the correct driving sequence according to the truth-table of Fig. 1.

When one of the push-pull output drivers is activated the upper transistor is always in saturation while the lower transistor is controlled in linear mode to set the desired speed in steady state conditions.

In PLL speed control applications the device provides a signal proportional to the motor speed at pin 2 (it is the buffered H1 input). The output of the PLL is connected to the speed control input of the device at pin 10, V_C.

In addition, a 1V offset is added to the speed demand voltage to match the minimum output of the PLL.

An external resistor, R_s, senses the output stage current. The sensing voltage across this resistor is amplified in the device by a factor of 7 to allow a reduction in the voltage drop the resistor.

The amplified sensing voltage is then compared with the speed demand signal from the PLL and the resulting error signal sets the amplifier output accordingly.

The output current is related to the speed control voltage by:

$$I_o = \frac{(V_C - 1)}{7\ R_s}$$

The value of the sensing resistor is given by:

$$R_s = (V_X - 1)/(7\ I_{max})$$

where V_X is the full scale voltage of V_C (see fig. 2).

In this way the V_C/I_{out} characteristics can be modified as shown in Fig. 2. Note that V_X max is clamped at 5.9V.

The most important feature of the L6231 is slew rate control. With this device a typical value of 0.1V/μs is achieved, reducing EMI to a very low value.

Another key feature is three-state operation; when the current is recirculating the corresponding phase driver is switched off and power dissipation is negligible. Current recirculates through the free-wheeling diodes in the acceleration phase and through the motor in steady-state conditions. Torque ripple is also minimized.

The L6231 can also operate with a brushless motor connected in a star configuration, leaving the center floating.

The Hall inputs are ground compatible comparators and can work with direct active digital Hall signals on three terminals (of the same polarity) and a TTL level on the other three terminals.

Fig. 1 - **TRUTH TABLE**

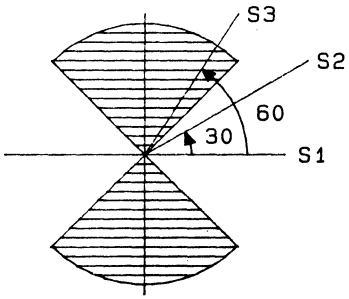
HALL EFFECT DIFF. INPUT 1 = POSITIVE 0 = NEGATIVE			UPPER DRIVER STATUS 1 = ON 0 = OFF			LOWER DRIVER STATUS 1 = ON 0 = OFF		
H1	H2	H3	UD1	UD2	UD3	LD1	LD2	LD3
1	0	0	0	0	1	1	0	0
1	1	0	0	0	1	0	1	0
1	1	1	1	0	0	0	1	0
0	1	1	1	0	0	0	0	1
0	0	1	0	1	0	0	0	1
0	0	0	0	1	0	1	0	0

DETERMINING HALL EFFECT SENSOR CODING

The L6231 assumes that the positioning of the Hall Effect sensors in a three-phase brushless DC bipolar motor are at 30 intervals. One can imagine two "windows" on the rotor each of which is 90 wide and 180 apart, see fig. 4. As a window passes over a sensor, the sensor output goes high. The timing diagram, fig. 3, shows the waveforms produced. These waveforms must appear at the Hall Effect Inputs of the L6231. Note that the rotation in fig. 4 must be counter-clockwise for forward rotation of the motor in whatever manner that is defined for the motor.

Fig. 4 is a stylized concept for determining the Hall Effect code pattern and does not reflect the actual direction of rotation of the motor in a physical sense. If a motor is chosen whose sensor outputs do not match the L6231 desired input pattern, a signal set conversion must be determined. It is helpful to visualize this by developing a diagram similar to that of fig. 4.

Fig. 4



For example, let us examine the output pattern of a different type of motor (fig. 5). Assuming 90 windows at 180 intervals, then with respect to fig. 4, a similar diagram, fig. 6, results in sensors 60 apart with the windows rotating clockwise. This situation results in a "forward" rotation of the motor.

Since S3 is the first sensor encountered by the window in fig. 6, this should be used for the L6231 Hall Effect Input, H1. After 30 of rotation CW, the H2 input of the L6231 must go high. The inverse of S1 from the motor would satisfy this. After an additional 30 of rotation, the H3 input must go high. The S2 sensor is encountered by the window. Thus, S2 is applied to this input, H3. By continuing around the diagram, one can develop a pattern which matches that for the L6231.

Fig. 5

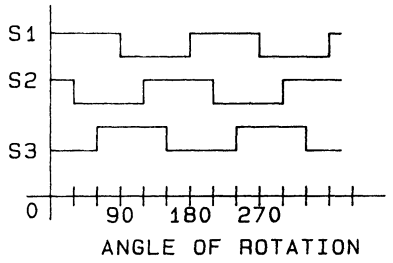
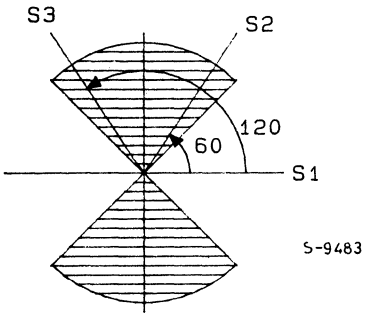


Fig. 6



Thus, the conversion table for this particular motor is:

Motor Sensors	L6231 Inputs
S3	H1
S1	H2
S2	H3

Note, for the inverted signal from S1 an actual inverter gate is not necessary with the L6231. Since the L6231 has differential inputs, the negative input pin may be used. Therefore, with TTL compatible Hall Effect sensors, the positive input is connected to a reference point along with the other negative inputs.

L6233

ADVANCE DATA

PHASE LOCKED FREQUENCY CONTROLLER

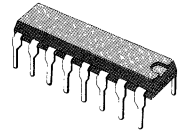
- PRECISION PHASE LOCKED FREQUENCY CONTROL SYSTEM
- XTAL OSCILLATOR
- PROGRAMMABLE REFERENCE FREQUENCY DIVIDERS
- PHASE DETECTOR WITH ABSOLUTE FREQUENCY STEERING
- DIGITAL LOCK INDICATOR
- DOUBLE EDGE OPTION ON THE FREQUENCY FEEDBACK SENSE AMPLIFIER
- TWO HIGH CURRENT OP-AMPS
- 5V REFERENCE OUTPUT

The L6233 is designed for use in phase locked frequency control loops. While optimized for precision speed control of DC motors, these device is universal enough for most applications that require phase locked control. A precise reference frequency can be generated using the device's high frequency oscillator and programmable frequency dividers. The oscillator operates using a broad range of crystals, or, can function as a buffer stage to an external frequency source.

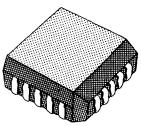
The phase detector on these integrated circuit compares the reference frequency with a frequency/phase feedback signal. In the case of a motor, feedback is obtained at a hall output or other speed detection device. This signal is buffered by a sense amplifier that squares up the signal as it goes into the digital phase detector. The phase detector responds proportionally to the phase error between the reference and the sense amplifier output. This phase detector includes absolute frequency steering to provide maximum drive signals when any frequency error exists. This feature allows optimum start-up and lock times to be realized.

Two op-amps are included that can be configured to provide necessary loop filtering. The outputs of these op-amps will source or sink in excess of 16mA, so they can provide a low impedance control signal to driving circuits.

Additional features include a double edge option on the sense amplifier that can be used to double the loop reference frequency for increased loop bandwidths. A digital lock signal is provided that indicates when there is zero frequency error and a 5V reference output allows DC operating levels to be accurately set.



DIP-16 Plastic (0.25)

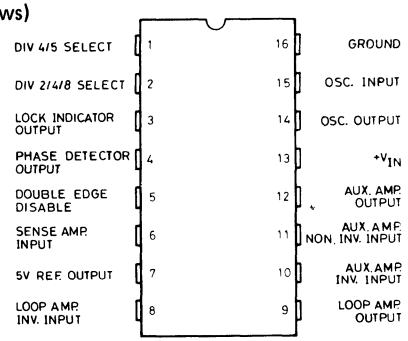


20 PLCC

ORDERING NUMBERS: L6233 (DIP-16)
L6233P (20 PLCC)

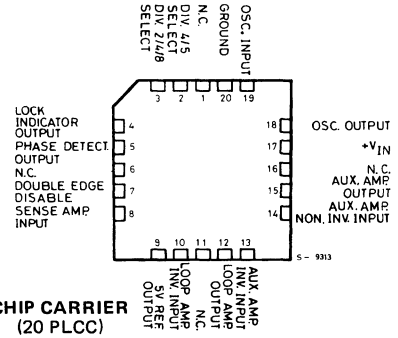
CONNECTION DIAGRAMS

(Top views)



DIP-16

5-9312



CHIP CARRIER (20 PLCC)

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, specifications hold for T_{amb} = 0°C to +70°C; $+V_{IN}$ = 12V)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
I_S	Supply current			20		mA
REFERENCE						
V_{REF}	Output voltage		4.75	5.0	5.25	V
ΔV_{REF}	Load Regulation	I_{OUT} = 0 to 7mA		5.0	20	mV
ΔV_{REF}	Line regulation	$+V_{IN}$ = 8 to 12V		2.0	20	mV
I_{SC}	Short circuit current	V_{OUT} = 0V		35		mA
OSCILLATOR						
G_v	DC voltage gain	Oscillator input to oscillator output		16		dB
V_{IB}	Input DC level	Oscillator input pin open, T_j = 25°C		1.3		V
Z_{IN} *	Input impedance	$V_{IN} = V_{IB} \pm 0.5V$, T_j = 25°C		1.6		KΩ
V_o	Output DC level	Oscillator input pin open T_j = 25°C		1.4		V
f_{oMAX}	Maximum operating frequency		10			MHz
DIVIDERS						
f_{oMAX}	Maximum input frequency	Input = $1V_{PP}$ at oscillator input	10			MHz
	Div. 4/5 input current	Input = 5V (Div. by 4)		150	500	μA
		Input = 0V (Div. by 5)	-5.0	0.0	5.0	μA
V_{TH}	Div. 4/5 threshold		0.5	1.6	2.2	V
	Div. 2/4/8 input current	Input = 5V (Div. by 8)		150	500	μA
		Input = 0V (Div. by 2)	-500	-150		μA
	Div. 2/4/8 open circuit voltage	Input current = 0μA (Div. by 4)	1.5	2.5	3.5	V
	Div. by 2 threshold		0.35	0.8		V
	Div. by 4 threshold		1.5		3.5	V
	Div. by 8 threshold	Volts below V_{REF}	0.35	0.8		V
SENSE AMPLIFIER						
V_T	Threshold voltage	Percent of V_{REF}		30		%
H_T	Threshold hysteresis			10		mV
I_b	Input bias current	Input = 1.5V		-0.2		μA
DOUBLE EDGE DISABLE INPUT						
V_i	Input current	Input = 5V (Disabled)		150	500	μA
		Input = 0V (Enabled)	-5.0	0.0	5.0	μA
V_T	Threshold voltage		0.5	1.6	2.2	V

APPLICATION INFORMATION

Determining the Oscillator Frequency

The frequency at the oscillator is determined by: the desired RPM of the motor, the divide ratio selected, the number of poles in the motor, and the state of the double edge select pin.

f_{osc} (Hz) = (Divide Ratio) • (Motor RPM) • (1/60 SEC/MIN) • (No. of Rotor Poles/2) • (× 2 if Pin 5 Low)

The resulting reference frequency appearing at the phase detector inputs is equal to the oscillator frequency divided by the selected divide ratio. If the double edge option is used, (Pin 5 low), the frequency of the sense amplifier input signal is doubled by responding to both the rising and falling edges of the input signal. Using this option the loop reference frequency can be doubled for a given motor RPM.

Fig. 1 - Recommended Oscillator Configuration Using AT Cut Quartz XTAL

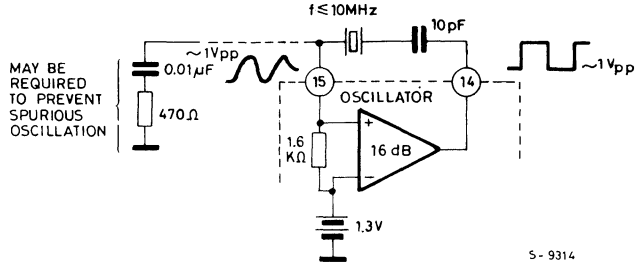


Fig. 2 - External Reference Frequency Input

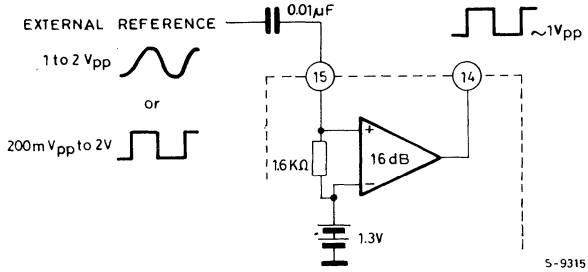
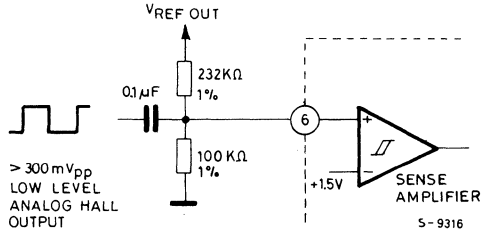


Fig. 3 - Method for Deriving Rotation Feedback Signal From Analog Hall Effect Device



* This signal may require filtering if chopped mode drive scheme is used.

Fig. 5 - Phase Detector State Diagram

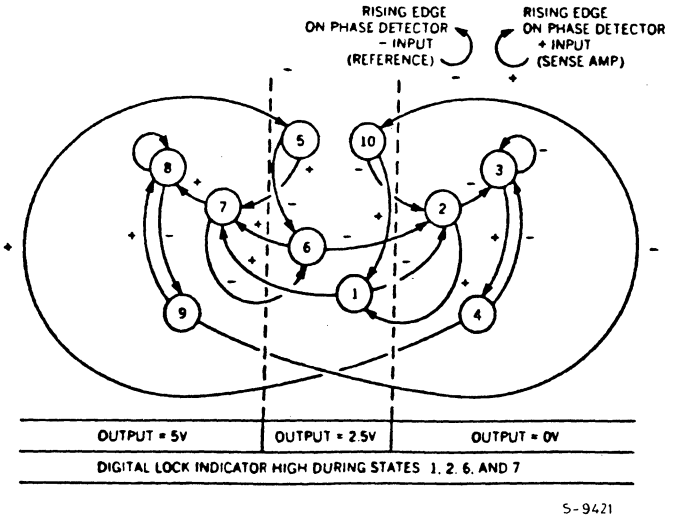
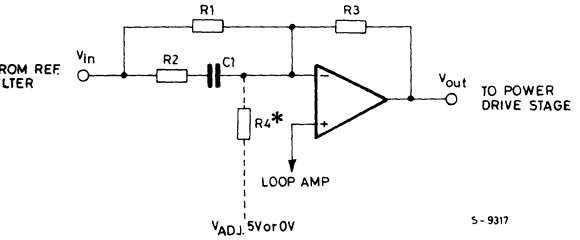


Fig. 6 - Suggested Loop Filter Configuration



$$\frac{V_{OUT}}{V_{IN}}(S) = \frac{R3}{R1} \cdot \frac{1 + S/\omega Z}{1 + S/\omega P}$$

$$\omega P = \frac{1}{R2\,C1}$$

$$\omega Z = \frac{1}{(R1 + R2)\,C1}$$

* The statistic phase error of the loop is easily adjusted by adding resistor, R4, as shown. To lock at zero phase error R4 is determined by :

$$R4 = \frac{2.5V \cdot R3}{|\Delta V_{OUT}|}$$

Where: $|\Delta V_{OUT}| = |V_{OUT} - 2.5V|$
and V_{OUT} = DC Operating Voltage At Loop Amplifier Output During Phase Lock

$(V_{OUT} - 2.5) > 0$ R4 Goes to 0V
$(V_{OUT} - 2.5) < 0$ R4 Goes to 5.0V

L6503

ADVANCE DATA

HAMMER SOLENOID CONTROLLER

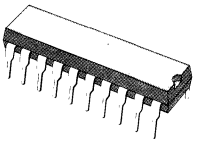
- DRIVES FOUR DARLINGTONS WITH UP TO 2.5mA DRIVE CURRENT
- FEEDBACK LOOP CONTROLS DARLINGTON CURRENT
- PRESETTABLE CONDUCTION TIME
- LATCHED μC-COMPATIBLE INPUTS
- DIAGNOSTIC CIRCUITRY

Designed primarily for solenoid driving applications, the L6503 Hammer Solenoid Controller includes all the circuitry needed to control four darlington power devices or a quad darlington array such as the SGS L7180.

The device is controlled by four latched logic inputs, which may be connected directly to a microcomputer chip, plus an analog input which sets the load current. Additionally, the conduction time of the outputs is controlled by a clock input which drives internal timers.

Fault conditions may be detected thanks to diagnostic circuitry which allows the control micro to read (serially) the load current status of the external darlingtons.

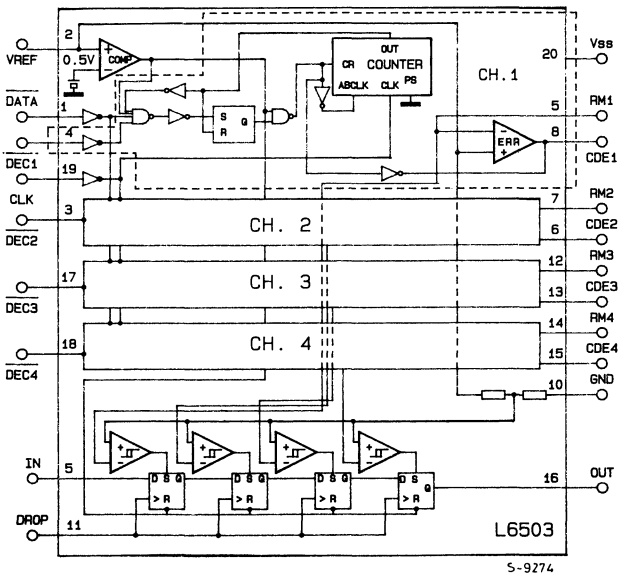
Assembled in a 20-pin DIP package, the L6503 operates on a single 5V supply and is suitable for computer printers, solenoid valves and similar applications.



DIP-20 Plastic
(X3P2)

ORDERING NUMBER: L6503

BLOCK DIAGRAM



PIN FUNCTION DESCRIPTION

N°	NAME	FUNCTION
1	$\overline{DATA}$	Latches control command into the four inputs DEC1-DEC4 on the high-low transition.
2	V_{ref}	Analog reference input which sets the load current for all four channels; when lower than 0.5V resets the logic circuitry.
3	$\overline{DEC2}$	Data input for channel 2. Data is latched on the high-low transition of the DATA input.
4	$\overline{DEC1}$	Data input for channel 1.
5	IN	Input for diagnostic shift register used to cascade several device.
6	CDE2	Channel 2 output (connect to base of darlington). Up to 2.5mA drive.
7	RM2	Feedback input from sensing resistor of channel 2 darlington.
8	CDE1	Channel 1 output.
9	RM1	Feedback input for channel 1 sense resistor.
10	GND	Ground.
11	DROP	Clock input for diagnostic register.
12	RM3	Feedback input for channel 3 sense resistor.
13	CDE3	Channel 3 output.
14	RM4	Feedback input for channel 4 sense resistor.
15	CDE4	Channel 4 output.
16	OUT	Output of diagnostic register.
17	$\overline{DEC3}$	Input for channel 3.
18	$\overline{DEC4}$	Input for channel 4.
19	CLK	Input for clock signal which sets conduction time for all four channels. $T_{on} = 128/f_{CLK}$.
20	V_{ss}	5V supply input voltage.

FUNCTIONAL DESCRIPTION

The L6503 Hammer Solenoid Controller is designed to control a quad darlington array, such as the SGS L7180, in solenoid driving applications.

Compatible with 5V microcomputer and peripheral chips, the L6503 is controlled by four logic inputs - one per channel ($\overline{DEC1}$-$\overline{DEC4}$) - which are latched by a high-low transition on the DATA input.

When one of the channels is activated the corresponding darlington is driven, with up to 2.5mA drive current. The conduction period is determined by the frequency applied to the CLK input which clocks the 7-bit timer in each channel. The conduction time is therefore 128/fCLK. Typically the CLK frequency will be of the order of 100KHz but the L6503's internal logic will operate at any clock rate within the range of practical conduction times.

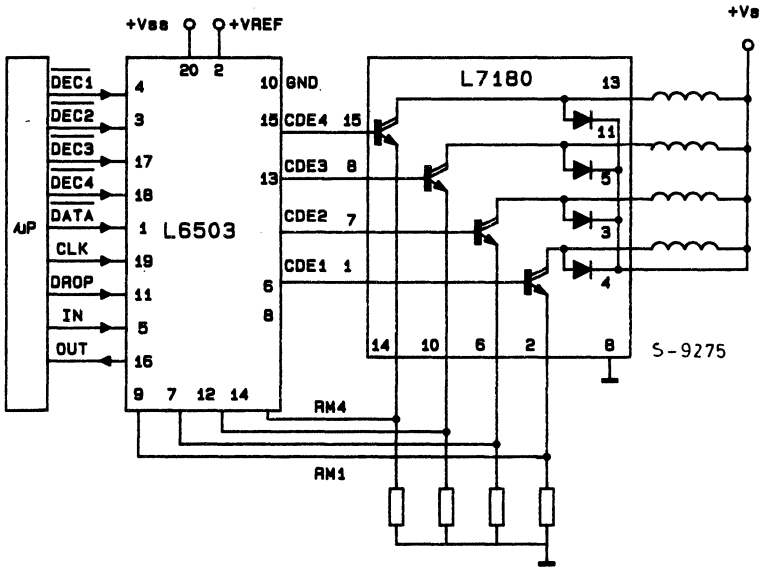
During the conduction period the load current is controlled by feedback from a sense resistor in the darlington's emitter and set by the voltage applied to the V_{ref} input. The current depends on both the values of V_{ref} and the sensing resistor: $I = V_{ref}/R_{sense}$.

The control microcomputer may verify correct operation of the complete drive subsystem thanks to a diagnostic circuit in the L6503. A four bit PISO shift register in the device monitors the feedback signals from the four output darlingtons and may be read serially after each command to check that the loads were driven.

Typically, this register, clocked by the DROP input, will be read a short time after each drive command has been latched into the device.

The input of this register (IN) is available externally so that multiple devices may be cascaded.

Fig. 1 - Application diagram



SGS Technology and Service

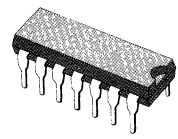
L6504

ADVANCE DATA

SOLENOID CONTROLLER

- SWITCH MODE CURRENT REGULATION
- TTL COMPATIBLE LOGIC INPUTS
- DRIVES ONE OR TWO EXTERNAL POWER TRANSISTORS
- VERY PRECISE ON-CHIP REFERENCE
- ANALOG CURRENT CONTROL INPUT
- ADJUSTABLE CURRENT RISE AND FALL TIME CONTROL INDEPENDENT OF SOLENOID SUPPLY VOLTAGE
- UNDERVOLTAGE LOCKOUT

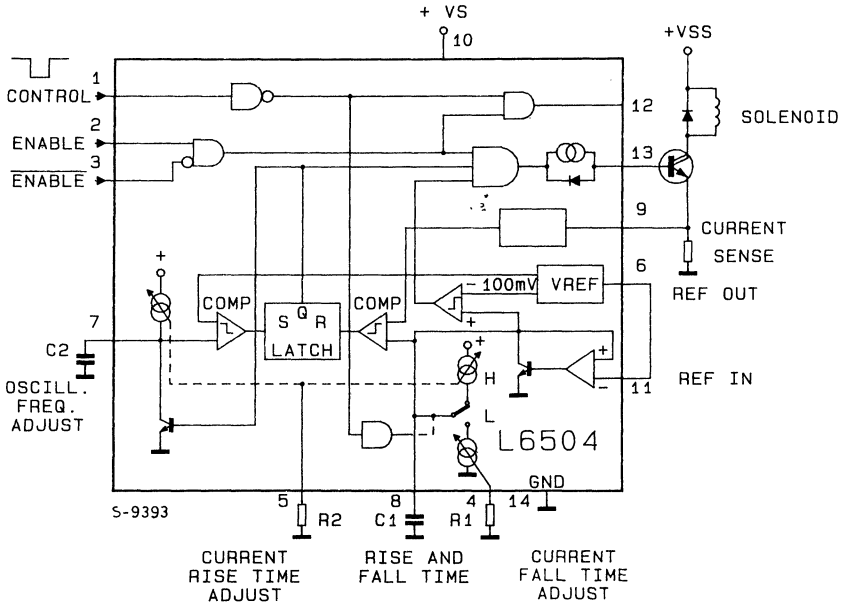
Designed for use with one external power transistor, the L6504 drives the hammer solenoid in daisywheel printers and typewrites. The device is controlled by three logic inputs and features switchmode regulation of the load current. A key feature of the device is that the rise and fall time of the load current can be set by external components. Additionally an analog input allows the load current to be set by an external DC voltage. An undervoltage lockout circuit guarantees the output off state for switch on phase.



DIP-14 Plastic
(0.25)

ORDERING NUMBER: L6504

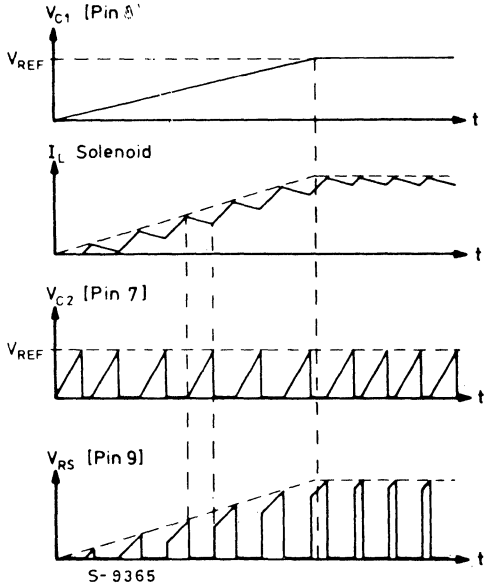
BLOCK DIAGRAM



PIN FUNCTION

N°	NAME	FUNCTION
1	CONTROL	TTL compatible control input. A low level activates the output, driving the load. Internal pull-up resistor.
2	ENABLE	TTL compatible enable input. A low level disables the output stage.
3	$\overline{\text{ENABLE}}$	TTL compatible enable input. A high level disables the output stage.
4	R1	The value of this resistor sets slope of trailing edge of load current.
5	R2	The value of this resistor sets slope of leading edge of load current.
6	REFERENCE OUT	Output for internal reference voltage.
7	C2	The value of this capacitor set the duration of power transistor switch off time.
8	C1	The value of this capacitor sets slope of leading and trailing edge of load current.
9	SENSING	Connection for load current sense resistor. Value sets the maximum load current : $I = V_{ref}/R_s$.
10	SUPPLY VOLTAGE	Supply voltage input.
11	REFERENCE IN	Input for external reference voltage to control load current by DC-level.
12	PNP DRIVING OUTPUT	Output to control external PNP-transistor for fast current discharge.
13	NPN DRIVING OUTPUT	Output for basecharge and discharge of external power transistor.
14	GROUND	Ground.

Fig. 1 - Timing diagram start phase



APPLICATION INFORMATION

Fig. 2 - Free running load current leading and trailing edge

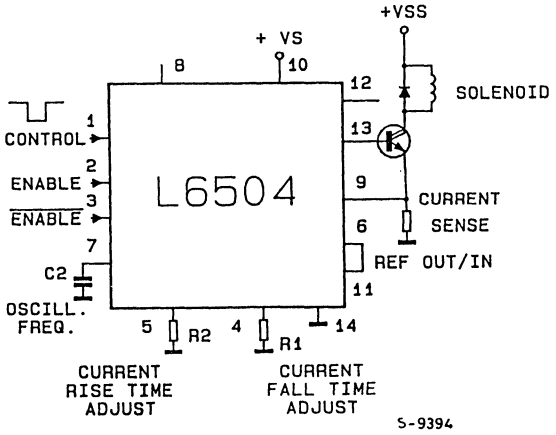
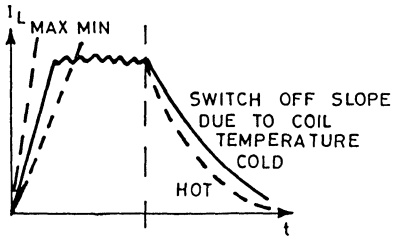


Fig. 3



APPLICATION INFORMATION (continued)

Fig. 8 - Free running leading edge fast current slope at trailing edge

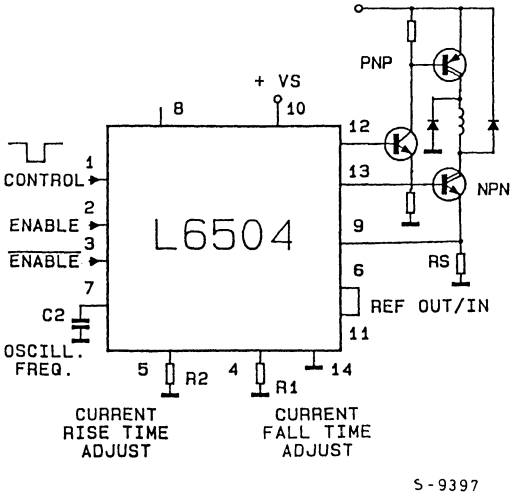
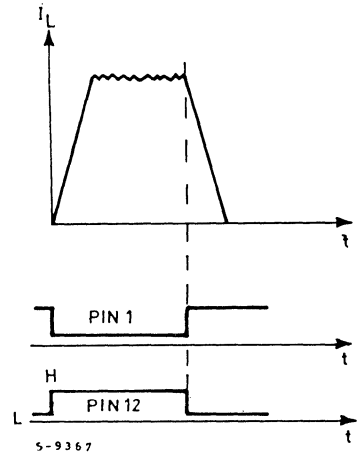


Fig. 9



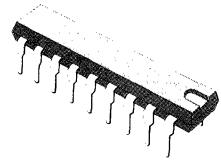
L6506

ADVANCE DATA

CURRENT CONTROLLER FOR STEPPING MOTORS

The L6506 is a linear integrated circuit designed to sense and control the current in stepping motors and similar devices. When used in conjunction with the L293, L298, L7150, or L7180, the chip set forms a constant current drive for an inductive load and performs all the interface function from the control logic thru the power stage.

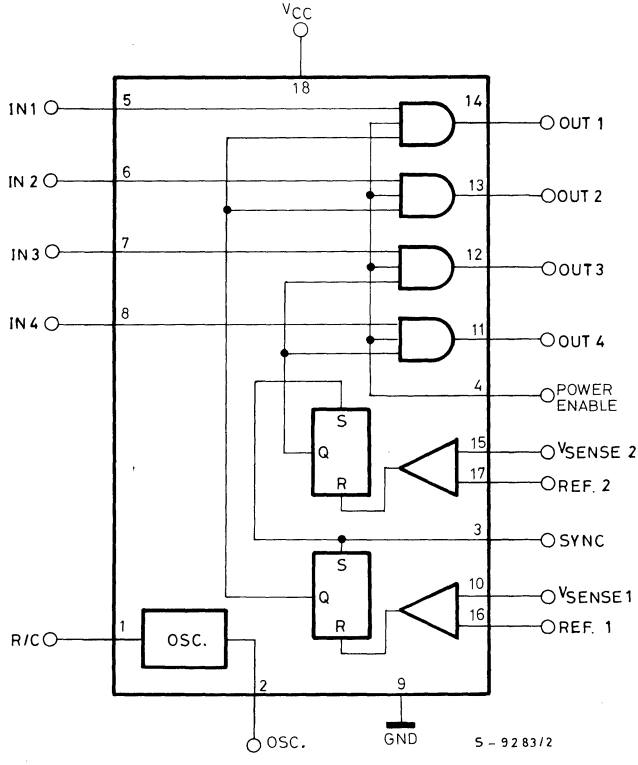
Two or more devices may be synchronized using the sync pin. In this mode of operation the oscillator in the master chip sets the operating frequency in all chips.



DIP-18 Plastic
(U7P2)

ORDERING NUMBER: L6506

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_{amb} = 25°C unless otherwise noted)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		4.5		7	V
I_{CC}	Quiescent supply current	V_{CC} = 7V			25	mA
COMPARATOR SECTION						
V_{IN}	Input voltage range	V_{sense} inputs	-0.3		3	V
V_{IO}	Input offset voltage	V_{IN} = 1.4V			± 5.0	mV
I_{IO}	Input Offset Current				± 200	nA
I_{IB}	Input bias current				1	μA
	Response time	V_{REF} = 1.4V V_{SENS} = 0 to 5V		0.8	1.5	μs
COMPARATOR SECTION PERFORMANCE (over operating temperature range)						
V_{IO}	Input offset voltage	V_{IN} = 1.4V			± 20	mV
I_{IO}	Input offset current				± 500	nA
LOGIC SECTION (over operating temperature range) - (TTL compatible inputs & outputs)						
V_{IH}	Input high voltage		2.0		V_s	V
V_{IL}	Input low voltage				0.8	V
V_{OH}	Output high voltage	V_{CC} = 4.75V I_{OH} = 400μA	2.5	3.5		V
V_{OL}	Output low voltage	V_{CC} = 4.75V I_{OL} = 4.0mA		0.25	0.4	V
I_{OH}	Output source current Outputs 1 - 4	V_{CC} = 4.75V	2.75			mA
OSCILLATOR						
f_{osc}	Frequency Range		5		70	KHz
$V_{th\,L}$	Lower threshold voltage			0.33V_{CC}		V
$V_{th\,H}$	Higher threshold voltage			0.66V_{CC}		V
R_i	Internal discharge resistor		0.7	1	1.3	KΩ

APPLICATIONS INFORMATION

The circuits shown in figures 2 and 3 use the L6506 to implement constant current drives for stepper motors. Figure 2 shows the L6506 used with the L298 to drive a 2 phase bipolar motor. Figure 3 shows the L6506 used with the L7180 to drive a 4 phase unipolar motor. The peak current can be calculated using the equation:

$$I_{peak} = \frac{V_{ref}}{R_{sense}}$$

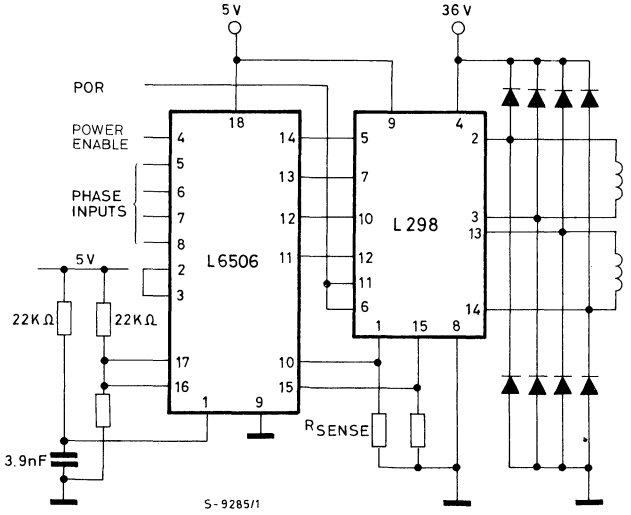
The circuit of Fig. 2 can be used in applications requiring different peak and hold current values by modifying the reference voltage.

The L6506 may be used to implement either full step or half step drives. In the case of 2 phase bipolar stepper motor applications, if a half step drive is used, the bridge requires an additional input to disable the power stage during the half step. If used in conjunction with the L298 the enable inputs may be used for this purpose.

For quad darlington array in 4 phase unipolar motor applications half step may be implemented using the 4 phase inputs.

The L6506 may also be used to implement microstepping of either bipolar or unipolar motors.

Fig. 2 - Application circuit bipolar stepper motor driver



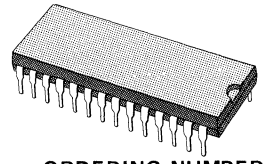
L6570A
L6570B

ADVANCE DATA

2-CHANNEL FLOPPY DISK READ/WRITE CIRCUITS

- TWO GAIN VERSIONS (A AND B)
- COMPATIBLE WITH 8", 5.25" AND 3.5" DRIVES.
- INTERNAL WRITE AND ERASE CURRENT SOURCES, EXTERNALLY SET
- INTERNAL CENTER TAP VOLTAGE SOURCE
- CONTROL SIGNALS ARE TTL COMPATIBLE
- TTL SELECTABLE WRITE CURRENT BOOST
- OPERATES ON +12 AND +5V POWER SUPPLIES

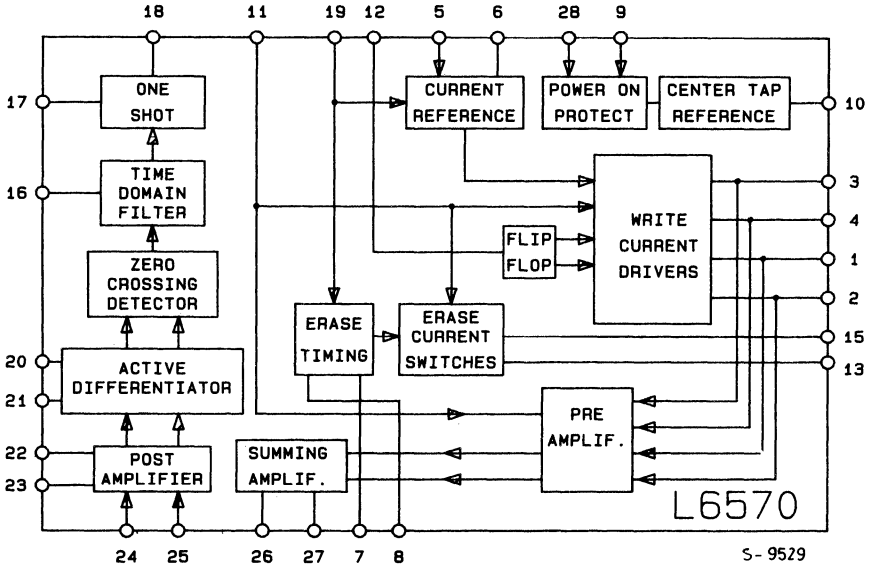
The L6570A/B are integrated circuits which perform the functions of generating write signals and amplifying and processing read signals required for a double sided floppy disk drive. The L6570A features a gain of 85 min and the L6570B of 300 min. All logic inputs and outputs are TTL compatible and all timing is externally programmable for maximum design flexibility.



DIP-28 Plastic

ORDERING NUMBER: L6570A
L6570B

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Unless otherwise specified, 4.75V ⩽ V_{CC} ⩽ 5.25V; 11.4V ⩽ V_{DD} ⩽ 12.6V; 0°C ⩽ T_{amb} ⩽ 70°C; R_W = 430Ω; R_{ED} = 62KΩ; C_E = 0.012μF; R_{EH} = 62KΩ; R_{EC} = 220Ω)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
POWER SUPPLY CURRENTS						
I_{CC}	5V supply current	Read Mode Write Mode			35 38	mA mA
I_{DD}	12V supply current	Read Mode **L6570A** **L6570B**			26 35	mA mA
		Write Mode (exclude Write and Erase currents) **L6570A** **L6570B**			24 35	mA mA
LOGIC SIGNALS — READ/$\overline{\text{WRITE}}$ (R/$\overline{\text{W}}$), CURRENT BOOST (CB)						
V_{IL}	Input Low voltage				0.8	V
I_{IL}	Input Low current	V_{IL} = 0.4V			-0.4	mA
V_{IH}	Input High voltage		2.0			V
I_{IH}	Input High current	V_{IH} = 2.4V			20	μA
LOGIC SIGNALS — WRITE DATA INPUT (WDI), HEAD SELECT (HS0/HS1)						
V_T+	Threshold voltage, Positive-going		1.4		1.9	V
V_T-	Threshold voltage, Negative-going		0.6		1.1	V
V_T+, V_T-	Hysteresis		0.4			V
I_{IH}	Input High current	V_{IH} = 2.4V			20	μA
I_{IL}	Input Low current	V_{IL} = 0.4V			-0.4	mA
CENTER TAP VOLTAGE REFERENCE						
V_{CT}	Output voltage	I_{WC} + I_E = 3mA to 60mA	V_{DD}-1.5		V_{DD}-0.5	V
V_{CC}	Turn-Off threshold		4.0			V
V_{DD}	Turn-Off threshold		9.6			V
V_{CT}	Disabled voltage				1.0	V
ERASE OUTPUTS (E1, E0)						
	Unselected head leakage	V_{E0}, V_{E1} = 12.6V			100	μA
V_{E1}, V_{E0}	Output on voltage	I_E = 50mA			0.5	V
WRITE CURRENT						
	Unselected head leakage	V_{E1}, V_{E0} = 12.6V			25	μA
	Write current range	R_W = 820Ω to 180Ω	3		10	mA
	Current reference accuracy	I_{WC} = 2.3/R_W V_{CB} (current boost) = 0.5V	-5		+5	%

ELECTRICAL CHARACTERISTICS (continued);

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PREAMPLIFIER – SUMMING AMPLIFIER					
Power supply rejection ratio	ΔV_{DD} = 300mV$_{pp}$ @ 500KHz Inputs shorted to V_{CT}	50			dB
Channel isolation	Unselected channel V_{IN} = 100mV$_{pp}$ @ 500KHz. Selected channel input connected to V_{CT}	40			dB
Equivalent input noise	Power BW = 10KHz to 1MHz Inputs shorted to V_{CT}			10	μV_{rms}
V_{CT} Center tap voltage			1.5		V
POSTAMPLIFIER – ACTIVE DIFFERENTIATOR					
A0, diff. voltage gain +IN, -IN to D1, D2	Freq. = 250KHz	8.5		11.5	V/V
Bandwidth (-3dB) +IN, -IN to D1, D2	C_D = 0.1μF, R_D = 2.5KΩ	3			MHz
Gain flatness +IN, -IN to D1, D2	Freq. = DC to 1.5MHz C_D = 0.1μF, R_D = 2.5KΩ			± 1.0	dB
Max. diff. output voltage swing	V_{IN} = 250KHz sine wave, AC coupled. ⩽ 5% THD in voltage across C_D	5.0			V_{pp}
Max. diff. input voltage	V_{IN} = 250KHz sine wave, AC coupled. ⩽ 5% THD in voltage across C_D, R_G = 1.5KΩ	2.5			V_{pp}
Diff. input impedance		10			KΩ
Gain control accuracy $\frac{\Delta A_R}{A_R} \times 100\%$	$A_R = A_O R_G / (8 \times 10^3 + R_G)$ R_G = 2KΩ	-25		+25	%
Threshold differential input voltage	Min. diff. input voltage at post amp. that results in a change of state at RDP V_{IN} = 250KHz square wave, C_D = 0.1μF, R_D = 500Ω, T_R, T_F ⩽ 0.2μs. No overshoot; Data pulse from each V_{IN} transition			3.7	mV$_{pp}$
Peak differential Network current		1.0			mA
TIME DOMAIN FILTER					
Delay accuracy $\frac{\Delta T_{TD}}{T_{TD}} \times 100\%$	$T_{TD} = 0.58\ R_{TD} \cdot (C_{TD} + 10^{-11}) + 150ns$. R_{TD} = 5KΩ to 10KΩ C_{TD} = 56pF V_{IN} = 50mV$_{pp}$ @ 250KHz sq. wave T_R, T_F ⩽ 20ns, AC coupled. Delay measured from 50% input amplitude to 1.5V data pulse	-15		+15	%
Delay range	$T_{TD} = 0.58\ R_{TD} = (C_{TC} + 10^{-11}) + 150ns$. R_{TD} = 5KΩ to 10KΩ C_{TD} = 56pF to 240pF R_D = 500Ω C_D = 0.1μF.	240		2370	ns

L7150
L7152

PRELIMINARY DATA

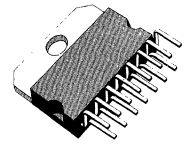
50V QUAD DARLINGTON SWITCHES

- FOUR NPN DARLINGTONS WITH ISOLATED CONNECTIONS
- OUTPUT CURRENT TO 1.5A EACH DARLINGTON
- MINIMUM BREAKDOWN 50V
- SUSTAINING VOLTAGE AT LEAST 35V
- MULTIWATT PACKAGE ALLOWS OPERATION AT 1.5A, 50V, 100% DUTY CYCLE, ALL FOUR DEVICES ON
- INTEGRAL SUPPRESSION DIODES
- VERSIONS FOR 5V AND 6-15V LOGIC FAMILIES

The L7150 and L7152 are 1.5A quad darlington arrays mounted in the 15-lead Multiwatt® plastic package. Each darlington is equipped with a suppression diode for inductive loads and all three terminals are isolated. A minimum breakdown of 50V is specified and the minimum sustaining voltage is 35V, measured at 100mA.

The L7150 has 350Ω input resistors and is compatible with TTL, DTL, LSTTL and 5V CMOS logic. The L7152 has 3KΩ input resistors for use with 6-15V CMOS and PMOS logic.

These devices are suitable for driving a wide range of inductive and non-inductive loads including DC motors, stepper motors, solenoids, relays, lamps, multiplexed LEDs and heaters.



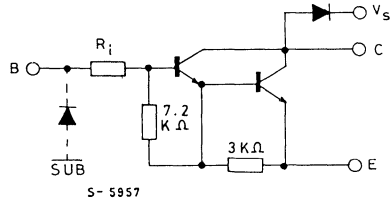
Multiwatt 15

ORDERING NUMBER: L7150
L7152

ABSOLUTE MAXIMUM RATINGS

V_{CEX}	Output voltage	50	V
$V_{CE(sus)}$	Output sustaining voltage	35	V
I_o	Output current	1.75	A
V_i	Input voltage	30	V
I_B	Input current	25	mA
P_{tot}	Power dissipation (T_{case} = 75°C)	25	W
T_{amb}	Operating ambient temperature range	0 to 70	°C
T_{stg}	Storage temperature	-55 to 150	°C

SCHEMATIC DIAGRAM



L7150 : R_{IN} = 350Ω
L7152 : R_{IN} = 3 KΩ

TEST CIRCUITS

Fig. 1

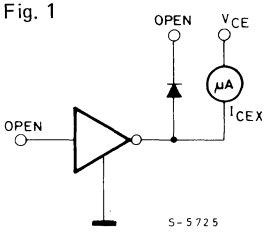


Fig. 2

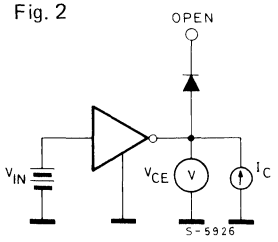


Fig. 3

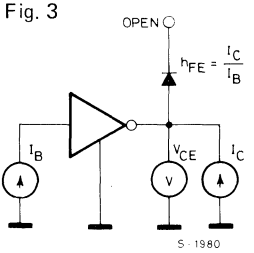


Fig. 4

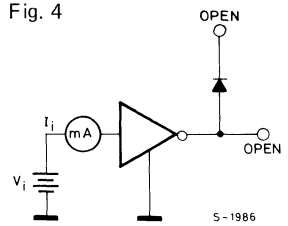
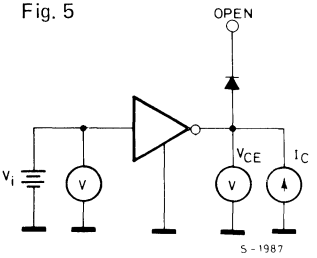


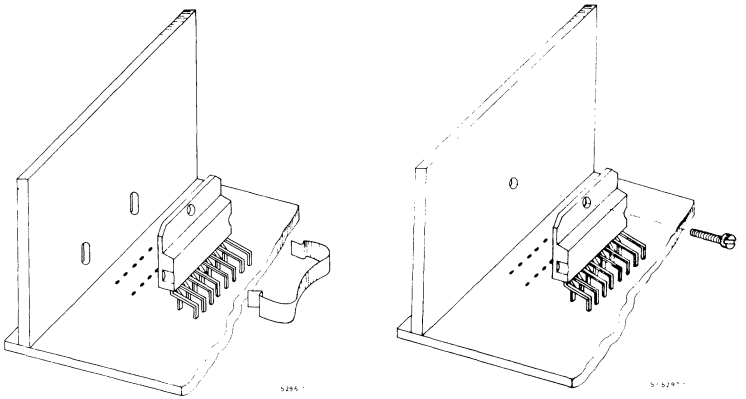
Fig. 5



MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the Multiwatt® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

Fig. 6 - Mounting example



L7180
L7182

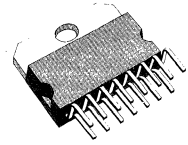
80V QUAD DARLINGTON SWITCHES

- FOUR NPN DARLINGTONS WITH ISOLATED CONNECTIONS
- OUTPUT CURRENT TO 1.5A EACH DARLINGTON
- MINIMUM BREAKDOWN 80V
- SUSTAINING VOLTAGE AT LEAST 50V
- MULTIWATT PACKAGE ALLOWS OPERATION AT 1.5A, 80V, 100% DUTY CYCLE, ALL FOUR DEVICES ON
- INTEGRAL SUPPRESSION DIODES
- VERSIONS FOR 5V AND 6-15V LOGIC FAMILIES

The L7180 and L7182 are 1.5A quad darlington arrays mounted in the 15-lead Multiwatt® plastic package. Each darlington is equipped with a suppression diode for inductive loads, and all three terminals are isolated. A minimum breakdown of 80V is specified and the minimum sustaining voltage is 50V.

The L7180 has 350Ω input resistors and is compatible with TTL, DTL, LSTTL and 5V CMOS logic. The L7182 has 3KΩ input resistors for use with 6-15V CMOS and PMOS logic.

These devices are suitable for driving a wide range of inductive and non-inductive loads including DC motors, stepper motors, solenoids, relays, lamps, multiplexed LEDs and heaters.



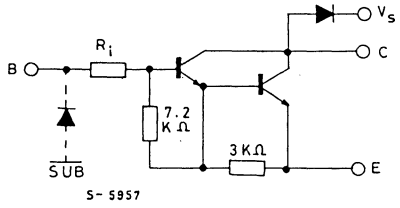
Multiwatt 15

ORDERING NUMBER: L7180
L7182

ABSOLUTE MAXIMUM RATINGS

V_{CEX}	Output voltage	80	V
$V_{CE\ (sus)}$	Output sustaining voltage	50	V
I_o	Output current	1.75	A
V_i	Input voltage	60	V
I_B	Input current	25	mA
P_{tot}	Power dissipation (T_{case} = 75°C)	25	W
T_{amb}	Operating ambient temperature range	0 to 70	°C
T_{stg}	Storage temperature	-55 to 150	°C

SCHEMATIC DIAGRAM



L7180 : R_{IN} = 350 Ω
L7182 : R_{IN} = 3 KΩ

TEST CIRCUITS

Fig. 1

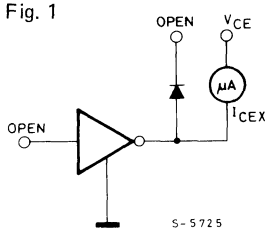


Fig. 2

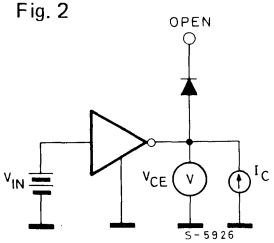


Fig. 3

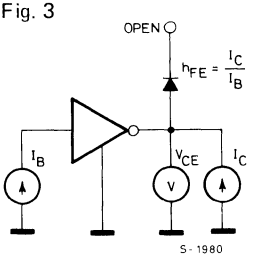


Fig. 4

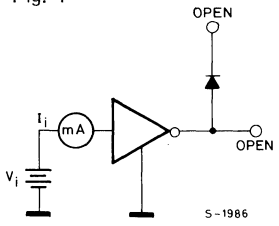
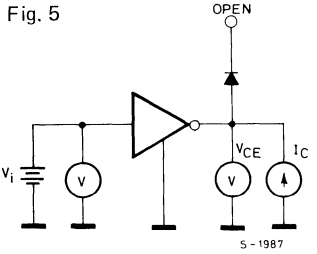


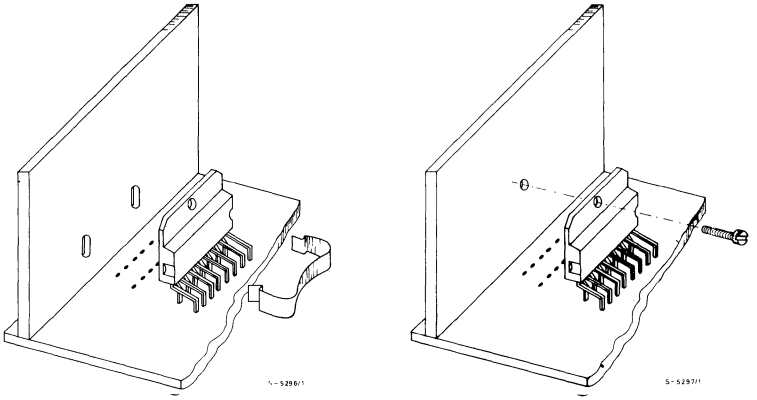
Fig. 5



MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the Multiwatt® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

Fig. 6 - Mounting example



L9222

ADVANCE DATA

QUAD INVERTING TRANSISTOR SWITCHES

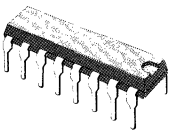
- OUTPUT VOLTAGE TO 50V
- OUTPUT CURRENT TO 1.2A
- VERY LOW SATURATION VOLTAGE
- TTL COMPATIBLE INPUTS
- INTEGRAL SUPPRESSION DIODE

The L9222 monolithic quad transistor switch is designed for high current, high voltage switching applications.

Each of the four switches is controlled by a logic input and all four are controlled by a common enable input. All inputs are TTL-compatible for direct connection to logic circuits.

Each switch consists of an open-collector transistor plus a clamp diode for applications with inductive loads. The emitters of the four switches are commoned. Any number of inputs and outputs of the same device may be paralleled.

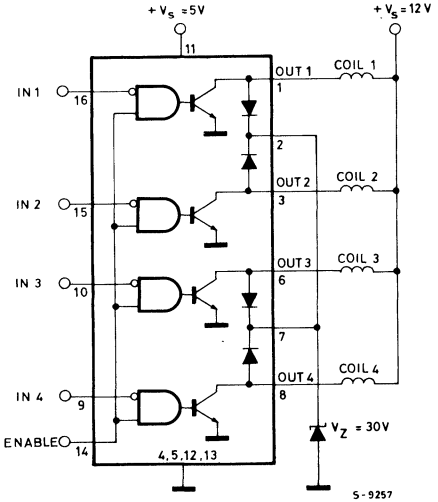
The device is intended to drive coils such as relays, solenoids, unipolar stepper motors, LED etc.



Powerdip 12 + 2 + 2
(V6P2)

ORDERING NUMBER: L9222

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
$V_{CE(sus)}$	Output sustaining voltage	V_{IN} = 2V V_{EN} = 2V I_C = 100mA		46			V
I_{CEX}	Output leakage current	V_{CE} = 50V V_{IN} = 2V				1	mA
$V_{CE(sat)}$	Collector emitter saturation voltage	$V_{IN} \leqslant$ 0.8V	I_C = 0.1A			0.2	V
			I_C = 0.4A			0.5	
			I_C = 0.7A			0.7	
V_{IL}	Input low voltage					0.8	V
I_{IL}	Input low current	V_{IN} = 0.4V				-100	µA
V_{IH}	Input high voltage			2.0			V
I_{IH}	Input high current	$V_{IN} \geqslant$ 2.0V				± 10	µA
I_s	Logic supply current	V_{ss} = 5V	All outputs ON I_C = 0.7A		50	85	mA
			All outputs OFF		8		mA
I_R	Clamp diode leakage current	V_R = 50V				100	µA
V_F	Clamp diode forward voltage	I_F = 1A				1.6	V
		I_F = 1.2A				2.0	
V_{ss}	Logic supply voltage			4.50		7	V

L9305A
L9305C

ADVANCE DATA

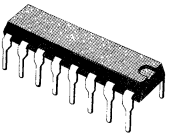
DUAL HIGH CURRENT RELAY DRIVER

- HIGH OUTPUT CURRENT
- HYSTERESIS INPUT COMPARATOR WITH WIDE RANGE COMMON MODE OPERATION AND GROUND COMPATIBLE INPUTS
- SHORT CIRCUIT PROTECTION OF OUTPUT TO 18V (FOR L9305A) AND 12V (FOR L9305C)
- INTERNAL THERMAL PROTECTION WITH HYSTERESIS
- OVERVOLTAGE CLAMP OF THE OUTPUT
- SINGLE SUPPLY VOLTAGE FROM 18V DOWN TO 3.5V

The L9305A and L9305C are a monolithic interface circuit with differential input comparator and open collector output able to sink high current specially to drive relays, lamps, d.c. motors.
Particular care has been taken to protect the device against destructive failures - short circuit of outputs to V_S, output overvoltages, supply overvoltage.

A built in thermal shut-down switches off the device when the IC's internal dissipation becomes too great and the chip temperature exceeds a setted security threshold.

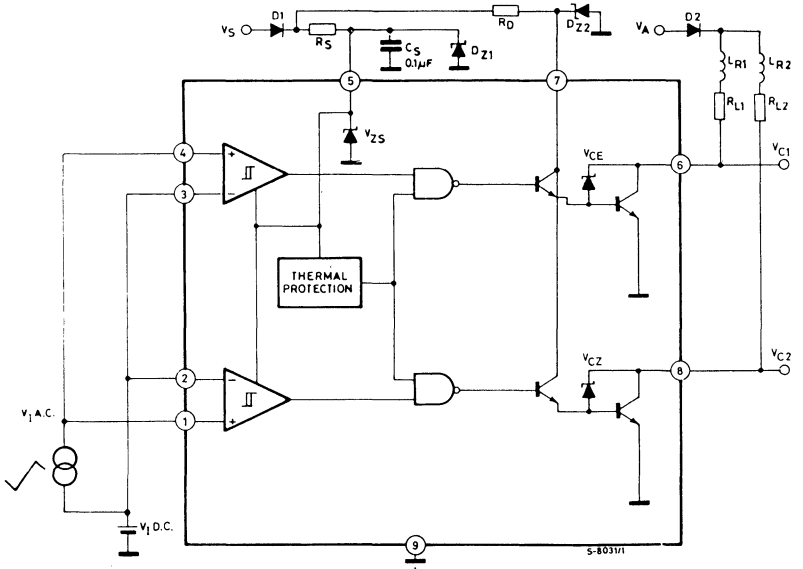
A hysteresis input comparator increases the interface's noise immunity, allowing the correct use also in critical environments as automotive or industrial applications.



Powerdip (8 + 8)

ORDERING NUMBER: L9305A
L9305C

TEST AND APPLICATION CIRCUIT



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

ELECTRICAL CHARACTERISTICS (V_{ST} = 14.4V, T_{amb} = 25°C; refer to block diagram unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_S	Supply voltage			3.5		18 (**)	V
$I_{S\ "st.by"}$	Supply current	$V_i^+ - V_i^- \geq 70mV$	for **L9305A** for **L9305C**		5 5	8 12	mA mA
$I_{"SON"}$	Supply current	$V_i^+ - V_i^- > 70mV$			18	30	mA
V_{CZ}	Voltage clamp at the output of each channel	I_{CZ} = 1A		20		27	V
V_{ZS}	Voltage clamp supply protection	I_Z = 10mA		20		27	V
V_{IH}	Hysteresis of the input comparator	V_{IN} = 20mV$_{pp}$ f = 1KHz		20		70	mV
I_B	Input bias current	$V^+ = V^-$ = 0V			0.2	1	μA
I_{OS}	Input offset current	$V^+ = V^-$ = 0V			± 20	± 200	nA
CMR	Input common mode range	V_{ST} = 3.5V to 18V		0		V_{ST}-1.6	V
I_{SC}	Output short circuit	$V_i^- - V_i^+ \geq 70mV$; V_S = 6V;	for **L9305A**	1.2		2.6	A
		V_S = 16V;	for **L9305A**	0.25		0.7	A
		V_S = 6 to 12V;	for **L9305C**	1		2.3	A
I_{CD}	Driver transistor curr.	$V_i^- - V_i^+ \geq 70mV$	DC			300	mA
			Pulsed (*)			600	
T_j	Thermal shut-down threshold				145		°C
T_j	Thermal shut-down hysteresis				15		°C
$V_{C\ (sat)}$	On status saturation voltage	$V_i^+ - V_i^- \geq 70mV$ I_{CD} = 100mA $I_{C\,OUT}$ = 1.2A $I_{C\,OUT}$ = 1A	for **L9305A** for **L9305C**			1	V
I_{OL}	Output leakage current	$V_i^- - V_i^+ \geq 70mV$	for **L9305A** for **L9305C**			250 500	μA μA

(*) $T_{ON} \leq 2.5ms$; repetition time ≥ 30ms

(**) The maximum allowed supply voltage without limiting resistors is limited by the built-in protection zener diodes see V_{CZ}, V_{ZS} Spec. values

(1) The L9305 has a SOA short circuit protection – (See Fig. 1).

L9306
L9306C

ADVANCE DATA

DUAL RELAY DRIVER

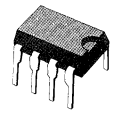
- HIGH OUTPUT CURRENT
- HYSTERESIS INPUT COMPARATOR WITH WIDE RANGE COMMON MODE OPERATION AND GROUND COMPATIBLE INPUTS
- SHORT CIRCUIT PROTECTION OF OUTPUT TO V_S (16V MAX. FOR L9306) AND (12V MAX. FOR L9306C)
- INTERNAL THERMAL PROTECTION WITH HYSTERESIS
- OVERVOLTAGE CLAMPING OF THE OUTPUT
- SINGLE SUPPLY VOLTAGE FROM 3.5V UP TO 18V

The L9306 and L9306C are a monolithic interface circuit with differential input comparator and open collector output able to sink current specifically to drive high inductive loads, relays, d.c. motors, electro valves etc.

Particular care has been taken to protect the device against destructive failures - short circuit of outputs to V_S, output overvoltages, supply overvoltage.

A built in thermal shut-down switches off the device when the IC's internal dissipation becomes too great and the chip termperature exceeds a setted security threshold.

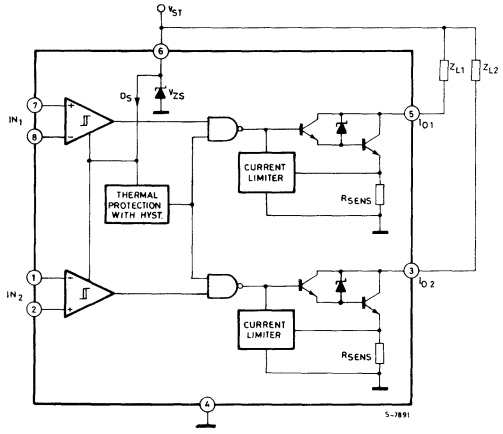
A hysteresis input comparator increases the interface's noise immunity, allowing the correct use also in critical environments as automotive or industrial applications.



Minidip Plastic

ORDERING NUMBER: L9306
L9306C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (V_{ST} = 14.4V, T_{amb} = 25°C refer to block diagram unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{ST}	Supply voltage		3.5		18 (*)	V
I_S "st. by" I_S "ON"	Supply current Supply current	$V_I^+ - V_I^- \geq 70mV$ $V_I^- - V_I^+ \geq 70mV$		5 18	8 30	mA mA
V_{ZS}	Voltage clamp - supply protection -	I_{ZS} = 10mA	20	23	27	V
V_{CSAT}	On status saturation voltage voltage	$V_I^- - V_I^+ \geq 70mV$ for **L9306** I_{COUT}= 300mA for **L9306C** I_{COUT}= 250mA		0.8	1.4	V
I_{SC}	Output short circuit current for each channel	$V_I^- - V_I^+ \geq 70mV$ for **L9306** for **L9306C**	300 250	550 550	700 1200	mA mA
V_{CZ}	Voltage clamp at the output - each channel	I_{CZ} = 300mA	20	24	27	V
I_{OL}	Output leakage current	$V_I^+ - V_I^- \geq 70mV$ T_{amb} = 25°C			500	μA
I_B	Input bias current	$V_I^+ = V_I^- = 0$		0.2	1	μA
I_{OS}	Input offset current	$V_I^+ = V_I^- = 0$		± 20	± 200	nA
V_{IH}	Hysteresis of the input comparator	V_{IN} = 200mV_{pp} f = 1kHz	20		70	mV
CMR	Input common mode range	V_{ST} = 3.5 to 18V	0	V_{ST}-1.6V		V

(*) The maximum allowed supply voltage without limiting resistors is limited by the built-in protection zener diodes: see V_{CZ}, V_{ZS} spec. values

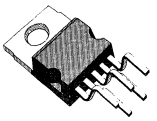
L9335
L9336

ADVANCE DATA

SOLENOID DRIVERS

- WIDE SUPPLY VOLTAGE RANGE 6 TO 24V
- INTERNAL CURRENT SENSING
- PRECISION OUTPUT CURRENT LEVELS 2.4A/0.6A (L9335) AND 4A/1A (L9336)
- LOW OUTPUT SATURATION VOLTAGE 2.5V AT I_O = 1.5A (L9335) AND 3V AT I_O = 3A (L9336)
- WIDE OPERATION JUNCTION TEMPERATURE RANGE -40°C TO 150°C
- MICROPROCESSOR COMPATIBLE INPUT
- DISABLE INPUT APPLICABLE FOR SWITCHING OFF DURING LOAD DUMP
- INTERNAL COMPENSATION
- INTERNAL SUPPLY STABILIZING ZENER DIODE

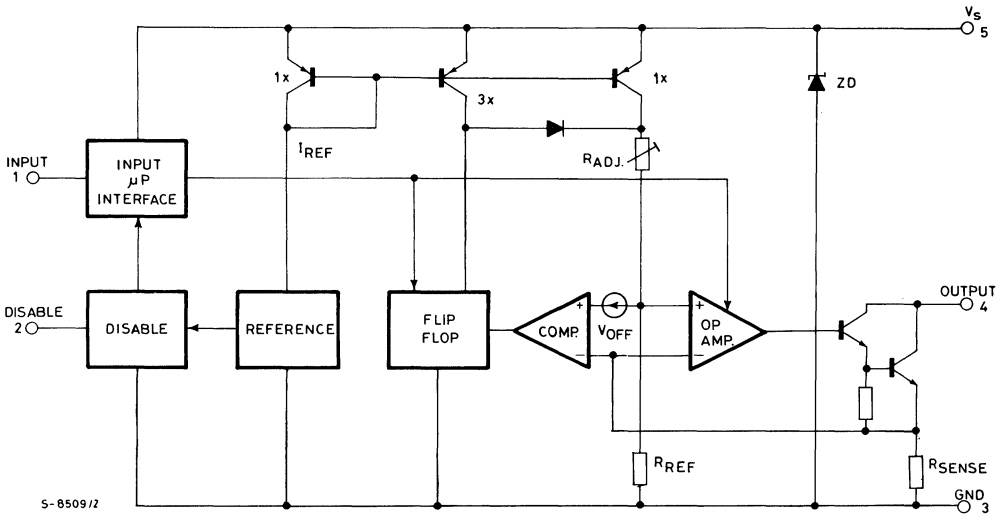
The L9335 and L9336 are monolithic integrated constant current sink drivers with internal current sensing and precision stable output current. The output current waveform for inductive load with switching to the holding current level after the peak current level has been reached is fitted for driving fuel injectors.



Pentawatt

ORDERING NUMBER: L9335
L9336

BLOCK DIAGRAM



PIN FUNCTION

N°	NAME	FUNCTIONS
1	INPUT	Logical input. If high, output current sink stage is activated.
2	DISABLE	Voltage at this pin higher than the disable threshold disables the output stage and reset the reference to the I_{OP} value.
3	GRUOND	Common ground terminal.
4	OUTPUT	Open collector output of the current sink darlington transistor.
5	SUPPLY	Internal zener diode between pin 5 and 3 stabilizes the supply voltage for the signal processing circuitry.

THERMAL DATA

$R_{th\,j\text{-}case}$	Thermal resistance junction case	max	4	°C/W

ELECTRICAL CHARACTERISTICS (V_S = 14.4V; T_j = 25°C, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
I_{OP}	Output peak current (L9335) (L9336)	V_i = 5V V_2 = 0	1.74 3.4	2.3 4.2	2.8 5.1	A
I_{OH}	Output hold current (L9335) (L9336)	V_i = 5V V_2 = 0	0.51 0.95	0.6 1.1	0.69 1.25	A
V_{OS}	Output saturation voltage (L9335) (L9336)	I_O = 1.5A V_i = 5V I_O = 3 A V_2 = 0		1 1.5	2.5 3	V
I_{OL}	Output leakage current	V_i = 0 V_2 = 0			1	mA
BV_O	Output sustaining voltage	I_O = 2mA; V_i = 0; V_2 = 0	42			V
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage		2			V
I_i	Input current	V_i = 5V			450	μA
V_{2T}	Disable input threshold voltage		1.25	1.5	1.75	V
V_{2H}	Disable input hysteresis			50		mV
I_{DB}	Disable input bias current				450	μA
V_{ZD}	Supply stabilizing zener	I_S = 20mA	6	7.5	9	V
I_Q	Quiescent current	V_S = 5.5V		2.5	10	mA

L9342

ADVANCE DATA

SIX-SOLENOID DRIVER

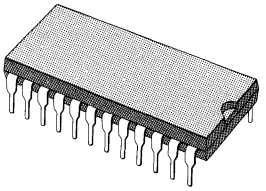
- DRIVES SIX INJECTOR SOLENOIDS
- CUTOFF FUNCTION
- ADJUSTABLE PEAK CURRENT
- INJECTOR STATUS OUTPUT
- TTL-COMPATIBLE INPUTS
- LOW POWER CONSUMPTION
- WIDE TEMPERATURE RANGE
- HIGH DENSITY I2L/LINEAR TECHNOLOGY

Designed for multipoint fuel injection systems, the L9342 Multipoint Injector Driver includes six drivers for external darlingtons with TTL-compatible inputs and circuitry which controls the peak current.

A separate logic input controls each driver. In addition a common logic input enables all six and a single reference input sets the peak current level. A status feedback output allows the control processor to monitor correct operation.

The L9342 is realized with a high density mixed I2L/analog technology.

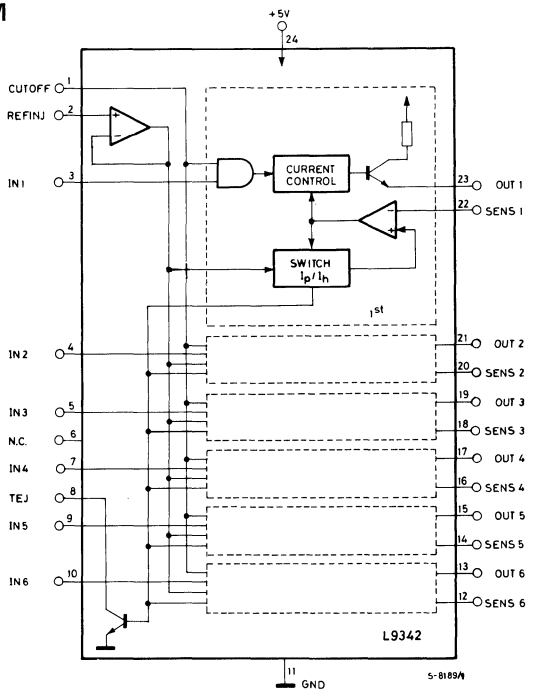
Features include low power consumption and a wide operating temperature range.



DIP-24 Plastic

ORDERING NUMBER: L9342

BLOCK DIAGRAM



PIN FUNCTIONS

N°	NAME	FUNCTION
1	CUTOFF	Enable input. When this pin is high the six drivers are enabled. When this input is low all six outputs are OFF, irrespective of the inputs.
2	REFINJ	Injector reference. A voltage applied to this pin sets the peak current $I_p = V_{REFINJ}/R_S$. The hold current is $I_h = \frac{I_p}{6}$
3, 4, 5 7, 9, 10	IN1 - IN6	Injector logic inputs. The output at each driver is active when its input is high.
8	TEI	Injector test output; an open-collector output used to monitor injector operation. This output is inactive until the injector current reaches the peak value. It remains active during the hold phase.
12, 14, 16 18, 20, 22	SENS1 - SENS2	Current sensing feedbach inputs for the six drivers.
13, 15, 17 19, 21, 23	OUT1 - OUT6	Outputs for power darlington driving.

ELECTRICAL CHARACTERISTICS ($V_S = 5V$; $T_j = 25°C$, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		4.75	5	5.25	V
I_S	Supply Current			15		mA
V_{IH}	Input High Voltage		2.5		V_S	V
V_{IL}	Input Low Voltage				0.8	V
I_{IH}	Input High Current	$V_{IH} = 2.5V$		120		μA
I_{IL}	Input Low Current	$V_{IL} = 0.4V$		18		μA
I_o	Output Current	$V_o = 1.4V$		36	50	mA
I_i	Input Current at pin 2			100	150	nA
BV_{CEO}	Collector emitter output voltage	$I_C = 10\mu A$	10			V
R_i	Input Resistance (pin 1, 3, 4, 5, 7, 9, 10)			22		KΩ
$\frac{I_p}{I_h}$	Peak to holding current ratio		5.7	6	6.3	

CIRCUIT OPERATION (continued)

Fig. 2 - Timing

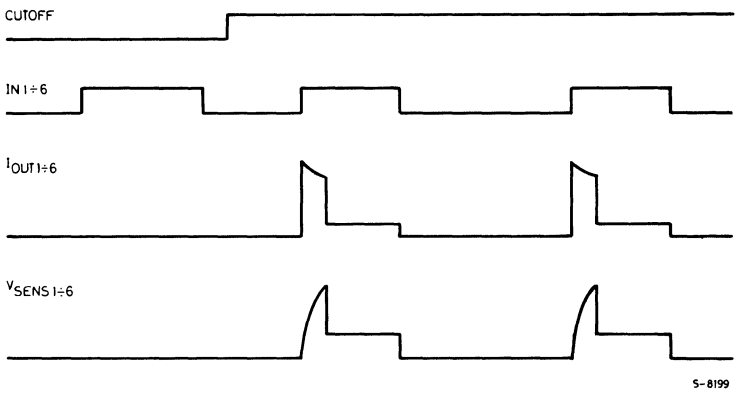
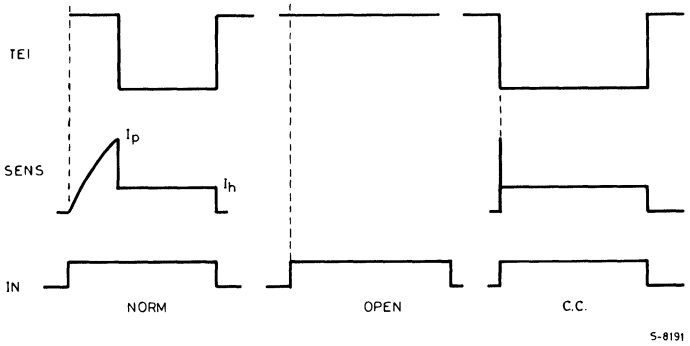


Fig. 3 - Injector test timing



L9350

ADVANCE DATA

LOW SATURATION DRIVER

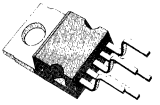
- LOW SATURATION VOLTAGE
- TTL COMPATIBLE INPUT
- WIDE SUPPLY VOLTAGE
- NO EXTERNAL COMPONENTS
- INTERNAL RECIRCULATION PATH FOR FAST DECAY OF INDUCTIVE LOAD CURRENT
- SHORT CIRCUIT PROTECTION
- THERMAL SHUTDOWN
- LOAD DUMP AND REVERSE BATTERY PROTECTION
- FAILSAFE OPERATION: OUTPUT IS OFF IF THE LOGIC INPUT IS LEFT OPEN

The L9350 is a monolithic integrated circuit designed to drive grounded resistive, inductive or mixed loads from the power supply positive side. Very low stand-by current (100μA typ.) and internally implemented protections against load dump and reverse voltages make the device very useful in automotive applications.

No external components are required because the output recirculation clamping zener is included in the chip. This zener can withstand an initial current of 550mA going down through an 80mH and 25Ω load.

Other safety features of the device include thermal shutdown, short circuit protection, a supply voltage range of 4.5 - 24V and a shut off condition of the output if the logic input (pin 5) is left open.

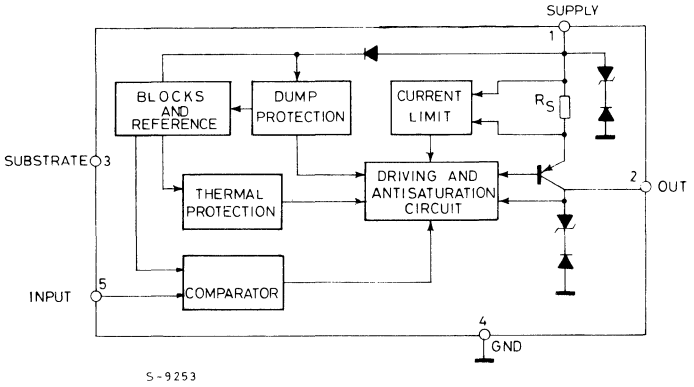
ON and OFF delay times of 25μs max in any output status, including recirculating situation, allows PWM use of L9350.



Pentawatt

ORDERING NUMBER: L9350

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (V_s = 14.4V, T_j = +25°C, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Operating supply voltage		4.5		24	V
V_{AH}	Input voltage High	4.5 < V_s < 24V	2			V
V_{AL}	Input voltage Low				0.8	
I_i	Input current	0.8 < V_i < 5.5V		20	50	μA
I_l	Output leakage current	V_o = 0V V_s = 24V V_i < 0.8V			1	mA
V_{sat}	Output saturation voltage	I_o = 150mA V_s = 4.5V		0.3	0.6	V
		I_o = 400mA V_s = 14.4V		0.5	0.7	V
		I_o = 550mA V_s = 14.4V		0.7	1	V
I_{sc}	Output short circuit current			1.5		A
I_Q	Quiescent current	V_i > 2V		50	80	mA
		V_i < 0.8V stand-by condition		100	200	μA
V_{zo}	Negative output zener voltage	R_L = 25Ω L = 80mH on V_i transition from "1" to "0"	-36	-30	-24	V
t_{on}	Turn ON delay	Only resistive load R_L = 25Ω (Fig. 2)			20	μs
t_{off}	Turn OFF delay				25	μs
t_{dc}	Turn ON delay while output is clamped	R_L = 25 L = 80mH any time during clamping internal (Fig. 3)			20	μs

For V_s > 26 the device is not operating.

Fig. 4 - 5V self-oscillating SMPS

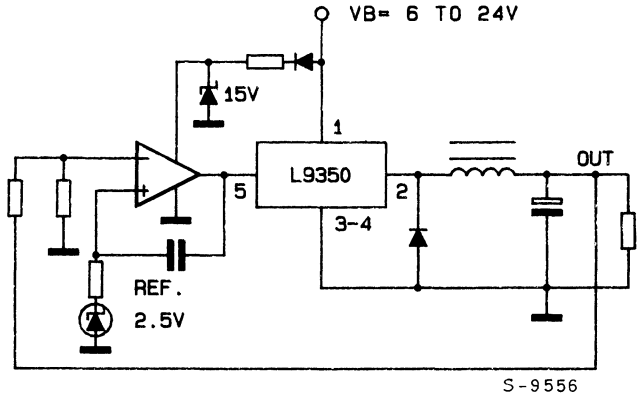
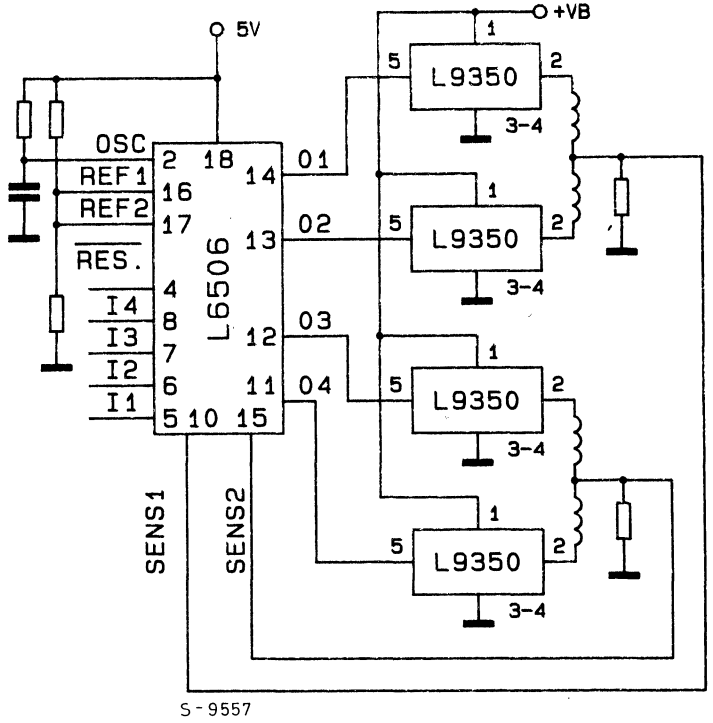


Fig. 5 - DC stepper motor driver



M5450
M5451

PRELIMINARY DATA

LED DISPLAY DRIVERS

- M5450 34 OUTPUTS/15mA SINK
- M5451 35 OUTPUTS/15mA SINK
- CURRENT GENERATOR OUTPUTS (NO EXTERNAL RESISTORS REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- ENABLE (ON M5450)
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

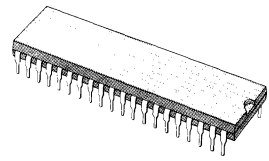
Application examples:

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5450 and M5451 are monolithic MOS integrated circuits produced with an N-channel silicon gate technology. They are available in 40-pin dual in-line plastic packages.

A single pin controls the LED display brightness by setting a reference current through a variable resistor connected to V_{DD} or to a separate supply of 13.2V maximum.

The M5450 and M5451 are improved pin-to-pin replacements of the NS MM 5450 and MM 5451.



DIP-40 Plastic

ORDERING NUMBERS: M5450 B7
M5451 B7

ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage	-0.3 to 15	V
V_I	Input voltage	-0.3 to 15	V
$V_{O\,(off)}$	Off state output voltage	15	V
I_O	Output sink current	40	mA
P_{tot}	Total package power dissipation	at 25°C	1W
		at 85°C	560 mW
T_j	Junction temperature	150	°C
T_{op}	Operating temperature range	-25 to 85	°C
T_{stg}	Storage temperature range	-65 to 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, V_{DD}= 4.75V to 13.2V, V_{SS}= 0V, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD}= 13.2V			7	mA
VI	Input Voltage Logical "0" Level Logical "1" Level	± 10 μA input bias 4.75 ⩽ V_{DD} ⩽ 5.25 V_{DD} > 5.25	 -0.3 2.2 V_{DD}-2		 0.8 V_{DD} V_{DD}	 V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 19)	Input current = 750 μA	3		4.3	V
$V_{O(off)}$	Off State Out. Voltage				13.2	V
I_O	Out. Sink Current (note 3) Segment OFF Segment ON	 V_O = 3V V_O = 1V (note 4) Brightness In. = 0 μA Brightness In. = 100 μA Brightness In. = 750 μA	 0 2 12	 2.7 15	 10 10 4 25	 μA μA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

Notes : 1. Output matching is calculated as the percent variation from I_{MAX} + I_{MIN}/2.

2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.

3. Absolute maximum for each output should be limited to 40 mA.

4. The V_O voltage should be regulated by the user. See figures 5 and 6 for allowable V_O versus I_O operation.

FUNCTIONAL DESCRIPTION

Both the M5450 and the M5451 are specifically designed to operate 4 or 5-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display.
Outputs change only if the serial data bits differ from the previous time.
Display brightness is determined by control of the output current LED displays.
A 1nF capacitor should be connected to brightness control, pin 19, to prevent possible oscillations.
A block diagram is shown in figure 1. For the M5450 a $\overline{\text{DATA ENABLE}}$ is used instead of the 35th output. The $\overline{\text{DATA ENABLE}}$ input is a metal option for the M5450.

Fig. 3

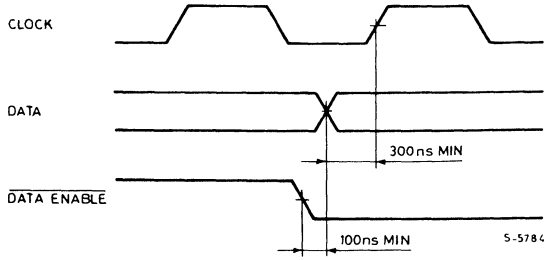


Fig. 4

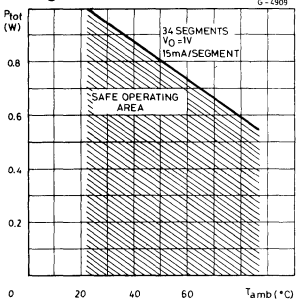


Fig. 5

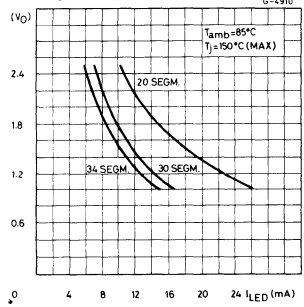
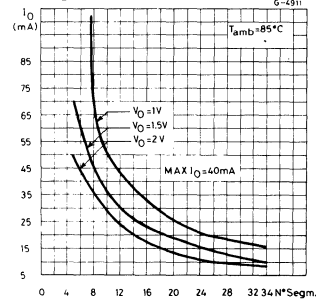
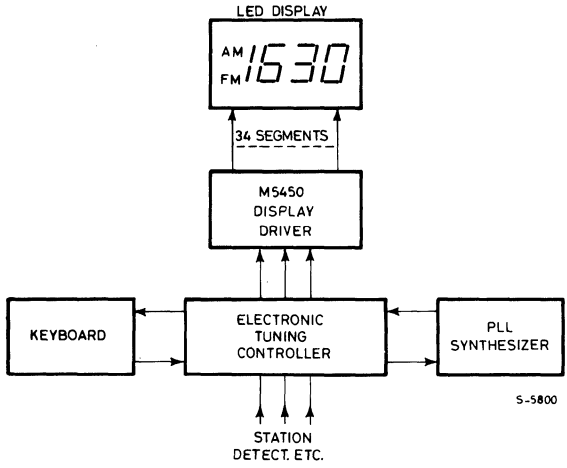


Fig. 6



TYPICAL APPLICATIONS

Basic electronically tuned Radio or TV system

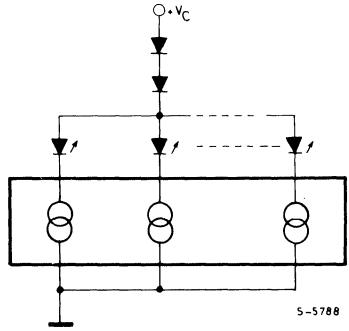


In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated

$$R = \frac{V_C - V_{D\,MAX} - V_{O\,MIN}}{N_{MAX} \cdot I_D}$$

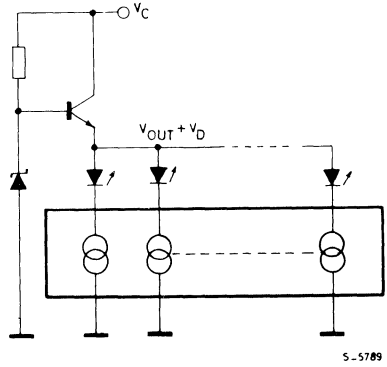
The worst case condition for the device is when roughly half of the maximum number of segments are activated.
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.
In critical cases more resistors can be used in conjunction with groups of segments.
In this case the current variation in the single resistor is reduced and P_{tot} limited.

b)



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.
The total power dissipation of the IC depends, in a first approximation, only on the number of segments activated.

c)



In this configuration $V_{OUT} + V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

M5480

LED DISPLAY DRIVER

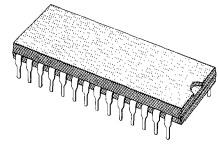
- 3 DIGIT LED DRIVER (23 SEGMENTS)
- CURRENT GENERATOR OUTPUTS (NO RESISTORS REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- NO LOAD SIGNAL REQUIRED
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Applications examples:

- MICROPROCESSOR DISPALYS
- INDUSTRIAL CONTROL INDICATION
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5480 is a monolithic MOS integrated circuit produced with a N-channel silicon gate technology. It utilizes the M5451 die packaged in a 28-pin plastic package making it ideal for a 3½ digit dispaly. A single pin controls the LED dispaly brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 13.2V maximum.

The M5480 is an improved pin-to-pin replacement of the NS MM 5480.



DIP-28 Plastic

ORDERING NUMBER: M5480 B7

ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage	-0.3 to 15	V
V_I	Input voltage	-0.3 to 15	V
$V_{O(off)}$	Off state output voltage	15	V
I_O	Output sink current	40	mA
P_{tot}	Total package power dissipation	at 25°C	940 mW
		at 85°C	490 mW
T_j	Junction temperature	150	°C
T_{op}	Operating temperature range	-25 to 85	°C
T_{stg}	Storage temperature range	-65 to 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, V_{DD}= 4.75V to 13.2V, V_{SS}= 0V, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD}= 13.2V			7	mA
V_I	Input Voltages Logical "0" Level Logical "1" Level	± 10 μA Input Bias 4.75 ⩽ V_{DD} ⩽ 5.25 V_{DD} > 5.25	 -0.3 2.2 V_{DD}-2		 0.8 V_{DD} V_{DD}	 V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 13)	Input Current = 750 μA	3		4.3	V
$V_{O(off)}$	Off State Output Voltage				13.2	V
I_O	Output Sink Current (note 3) Segment OFF Segment ON	 V_O = 3V V_O = 1V (note 4) Brightness In. = 0 μA Brightness In. = 100 μA Brightness In. = 750 μA	 0 2 12	 2.7 15	 10 10 4 25	 μA μA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

Notes: 1. Output matching is calculated as the percent variation from $I_{MAX} + I_{MIN}/2$.
2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40 mA.
4. The V_O voltage should be regulated by the user.

FUNCTIONAL DESCRIPTION

The M5480 is specifically designed to operate $3^1/_2$ digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display.
Outputs change only if the serial data bits differ from the previous time.
Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 13, to prevent possible oscillations.

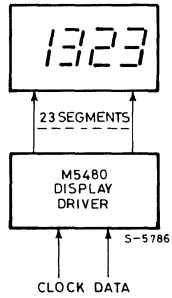
A block diagram is shown in figure 1. The output current is typically 20 times greater than the current into pin 13, which is set by an external variable resistor.
There is an internal limiting resistor of 400Ω nominal value.

Fig. 4 - Serial Data Bus/Outputs Correspondence

5451	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	START
5480	X	23	22	21	20	19	X	X	18	X	17	16	15	14	13	12	X	X	X	X	11	10	9	8	X	X	X	7	6	5	4	3	2	1	X	START

TYPICAL APPLICATION

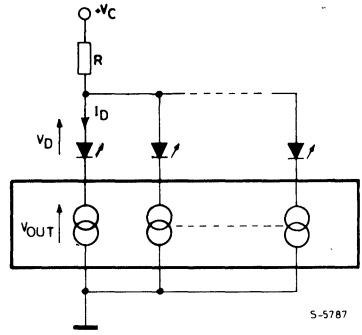
BASIC $3^1/_2$ Digit interface.



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)



In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated.

$$R = \frac{V_C - V_{D\,MAX} - V_{OUT\,MIN}}{N_{MAX} \cdot I_D}$$

The worst case condition for the device is when roughly half of the maximum number of segments are activated.
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.
In critical cases more resistors can be used in conjunction with groups of segments.
In this case the current variation in the single resistor is reduced and P_{tot} limited.

M5481

LED DISPLAY DRIVER

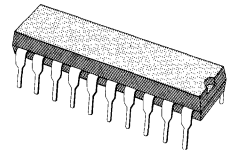
- 2 DIGIT LED DRIVER (14 SEGMENTS)
- CURRENT GENERATOR OUTPUTS (NO RESISTOR REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- DATA ENABLE
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Application examples:

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5481 is a monolithic MOS integrated circuit produced with a N-channel silicon gate technology. It utilizes the M5450 die packaged in a 20-pin plastic package copper frame, making it ideal for a 2-digit display. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 13.2V maximum.

The M5481 is an improved pin-to-pin replacement of the NS MM 5481.



DIP-20 Plastic
(0.25)

ORDERING NUMBER: M5481 B7

ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage	-0.3 to 15	V
V_I	Input voltage	-0.3 to 15	V
$V_{O\,(off)}$	Off state output voltage	15	V
I_O	Output sink current	40	mA
P_{tot}	Total package power dissipation	at 25°C	1.5W
		at 85°C	800 mW
T_j	Junction temperature	150	°C
T_{op}	Operating temperature range	-25 to 85	°C
T_{stg}	Storage temperature range	-65 to 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, V_{DD}= 4.75V to 13.2V, V_{SS}= 0V, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD}= 13.2V			7	mA
V_I	Input Voltages Logical "0" Level Logical "1" Level	± 10 μA Input Bias 4.75 ⩽ V_{DD} ⩽ 5.25 V_{DD} > 5.25	 -0.3 2.2 V_{DD}-2		 0.8 V_{DD} V_{DD}	 V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 9)	Input Current = 750 μA	3		4.3	V
$V_{O(off)}$	Off State Output Voltage				13.2	V
I_O	Output Sink Current (note 3) Segment OFF Segment ON	 V_O = 3V V_O = 1V (note 4) Brightness In. = 0 μA Brightness In. = 100 μA Brightness In. = 750 μA	 0 2 12	 2.7 15	 10 10 4 25	 μA μA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

Notes: 1. Output matching is calculates as the percent variation from $I_{MAX} + I_{MIN}/2$.
2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40 mA.
4. The V_O voltage should be regulated by the user.

FUNCTIONAL DESCRIPTION

The M5481 uses the M5450 die which is packaged to operate 2-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal.
The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 9, to prevent possible oscillations.

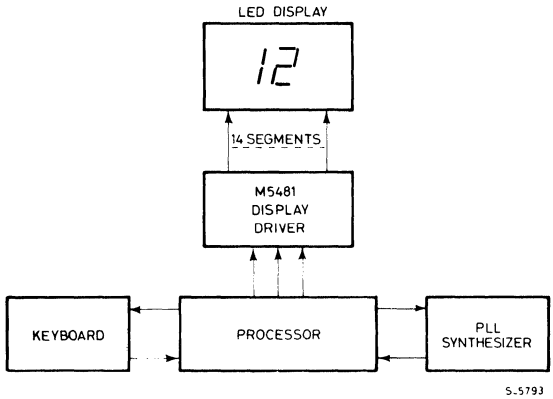
A block diagram is shown in figure 1. The output current is typically 20 times greater than the current into pin 9, which is set by an external variable resistor.
These is an internal limiting resistor of 400Ω nominal value.

Fig. 4 - Serial Data Bus/Outputs Correspondence

5450	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	START
5481	X	X	X	X	14	13	X	X	X	X	12	11	10	9	X	X	X	X	8	7	6	5	X	X	X	X	4	3	2	1	X	X	X	X	START

TYPICAL APPLICATION

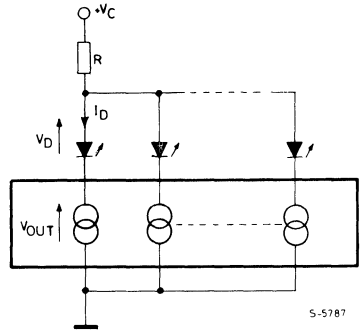
BASIC electronically tuned TV system



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)



In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated.

$$R = \frac{V_C - V_{D\,MAX} - V_{O\,MIN}}{N_{MAX} \cdot I_D}$$

The worst case condition for the device is when roughly half of the maximum number of segments are activated.
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.
In critical cases more resistors can be used in conjunction with groups of segments. In this case the current variation in the single resistor is reduced and P_{tot} limited.

M5482

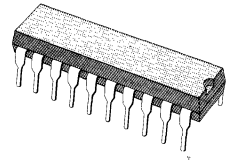
LED DISPLAY DRIVER

- 2 DIGIT LED DRIVER (15 SEGMENTS)
- CURRENT GENERATOR OUTPUTS (NO RESISTOR REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Application examples:

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5482 is a monolithic MOS integrated circuit produced with an N-channel silicon gate technology. It utilizes the M5450 die packaged in a 20-pin plastic package copper frame, making it ideal for a 2-digit display. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 13.2V maximum.



DIP-20 Plastic
(0.25)

ORDERING NUMBER: M5482 B7

ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage	-0.3 to 15	V
V_I	Input voltage	-0.3 to 15	V
$V_{O\,(off)}$	Off state output voltage	15	V
I_O	Output sink current	40	mA
P_{tot}	Total package power dissipation	at 25°C	1.5W
		at 85°C	800 mW
T_j	Junction temperature	150	°C
T_{op}	Operating temperature range	-25 to 85	°C
T_{stg}	Storage temperature range	-65 to 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, V_{DD}= 4.75V to 13.2V, V_{SS}= 0V, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD}= 13.2V			7	mA
V_I	Input Voltages Logical "0" Level Logical "1" Level	± 10 μA Input Bias 4.75 ≤ V_{DD} ≤ 5.25 V_{DD} > 5.25	 -0.3 2.2 V_{DD}-2		 0.8 V_{DD} V_{DD}	 V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 9)	Input Current = 750 μA	3		4.3	V
$V_{O(off)}$	Off State Output Voltage				13.2	V
I_O	Output Sink Current (note 3) Segment OFF Segment ON	 V_O = 3V V_O = 1V (note 4) Brightness In. = 0 μA Brightness In. = 100 μA Brightness In. = 750 μA	 0 2 12	 2.7 15	 10 10 4 25	 μA μA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

Notes: 1. Output matching is calculated as the percent variation from $I_{MAX} + I_{MIN}/2$.
2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40 mA.
4. The V_O voltage should be regulated by the user.

FUNCTIONAL DESCRIPTION

The M5482 uses the M5451 die which is packaged to operate 2-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal.
The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 9, to prevent possible oscillations.

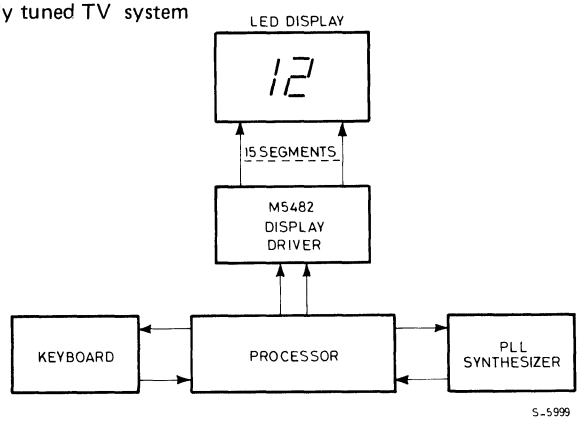
A block diagram is shown in figure 1. The output current is typically 20 times greater than the current into pin 9, which is set by an external variable resistor.
There is an internal limiting resistor of 400Ω nominal value.

Fig. 4 - Serial Data Bus/Outputs Correspondence

5451	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	START
5482	15	X	X	X	X	14	13	X	X	X	X	12	11	10	9	X	X	X	X	8	7	6	5	X	X	X	X	4	3	2	1	X	X	X	X	START

TYPICAL APPLICATION

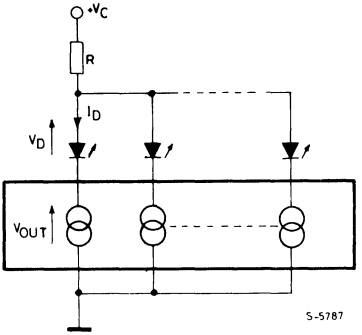
BASIC electronically tuned TV system



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)



In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated.

$$R = \frac{V_C - V_{D\,MAX} - V_{O\,MIN}}{N_{MAX} \cdot I_D}$$

The worst case condition for the device is when roughly half of the maximum number of segments are activated.
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.
In critical cases more resistors can be used in conjunction with groups of segments. In this case the current variation in the single resistor is reduced and P_{tot} limited.

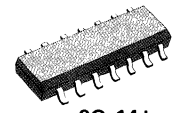
MC1488

RS232C QUAD LINE DRIVER

- CURRENT LIMITED OUTPUT ± 10mA TYP.
- POWER-OFF SOURCE IMPEDANCE 300Ω MIN.
- SIMPLE SLEW RATE CONTROL WITH EXTERNAL CAPACITOR
- FLEXIBLE OPERATING SUPPLY RANGE
- INPUTS ARE TTL AND μP COMPATIBLE

The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS232C.

DIP-14 Plastic and Ceramic



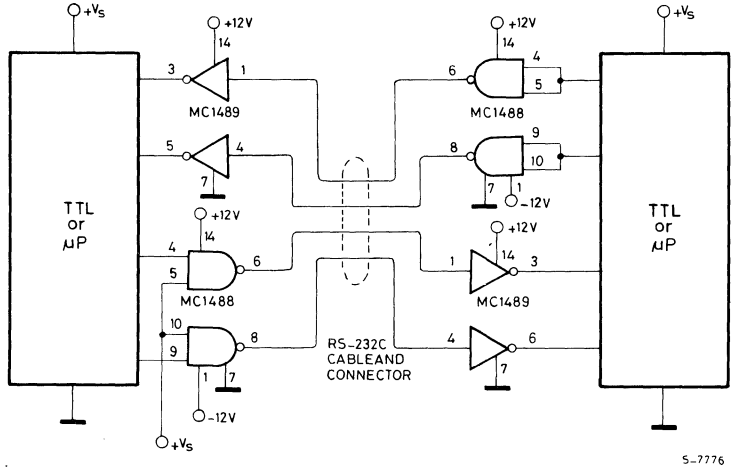
SO-14J

ORDERING NUMBER: MC1488P (Plastic DIP)
MC1488L (Ceramic DIP)
MC1488D (SO-14)

ABSOLUTE MAXIMUM RATINGS

V_S	Power supply voltage	15	V
V_{EE}	Power supply voltage	-15	V
V_{IR}	Input voltage range	$-15 \leqslant V_{IR} \leqslant 7$	V
V_O	Output signal voltage	± 15	V
T_{amb}	Operating ambient temperature	0 to 75	°C
T_{stg}	Storage temperature range	-65 to 150	°C

Typical Application: RS232C data transmission



ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit	Fig.
I_S	Positive supply current ($R_l = \infty$)	V_{IH} = 1.9V V_{IL} = 0.8V V_{IH} = 1.9V V_{IL} = 0.8V V_{IH} = 1.9V V_{IL} = 0.8V	V_S = 9V V_S = 9V V_S = 12V V_S = 12V V_S = 15V V_S = 15V		15 4.5 19 5.5	20 6 25 7 34 12	mA	5
I_{EE}	Negative supply current ($R_L = \infty$)	V_{IH} = 1.9V V_{IL} = 0.8V V_{IH} = 1.9V V_{IL} = 0.8V V_{IH} = 1.9V V_{IL} = 0.8V	V_{EE} = -9V V_{EE} = -9V V_{EE} = -12V V_{EE} = -12V V_{EE} = -15V V_{EE} = -15V		-13 -18	-17 -15 -23 -15 -34 -2.5	mA µA mA µA mA mA	5
P_C	Power consumption	V_S = 9V V_S = 12V	V_{EE} = -9V V_{EE} = -12V			333 576	mW	

SWITCHING CHARACTERISTICS ($V_S = \pm 9 \pm 1\%$ V, $V_{EE} = -9 \pm 1\%$ V, $T_{amb} = 25°C$)

t_{PLH}	Propagation delay time	Z_l = 3KΩ and 15pF		275	350	ns	6
t_{THL}	Fall time	Z_l = 3KΩ and 15pF		45	75	ns	6
t_{PHL}	Propagation delay time	Z_l = 3KΩ and 15pF		110	175	ns	6
t_{TLH}	Rise time	Z_l = 3KΩ and 15pF		55	100	ns	6

* Maximum package power dissipation may be exceeded if all outputs are shorted simultaneously

TEST CIRCUITS

Fig. 1 - Input current

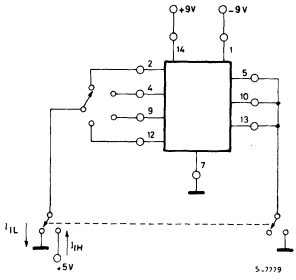


Fig. 2 - Output voltage

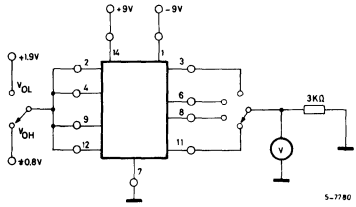
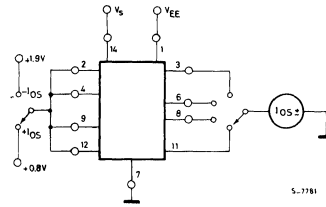


Fig. 3 - Output short-circuit current



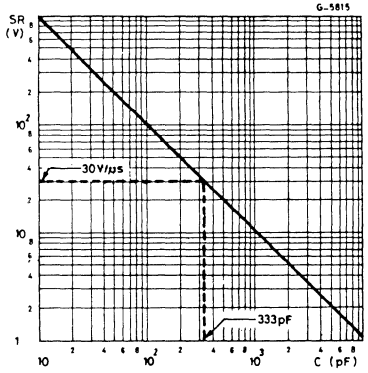
APPLICATIONS INFORMATION

The Electronic Industries Association (EIA) has released the RS232C specification detailing the requirements for the interface between data processing equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined levels. The RS232C requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5 and 15V in magnitude and are positive for a logic "0" and negative for a logic "1". These voltages are so defined when the drivers are terminated with a 3000 to 7000Ω resistor. The MC1488 meets this voltage requirement by converting a DTL/TTL logic level into RS232C levels with one stage of inversion.

The RS232C specification further requires that during transitions, the driver output slew rate must not exceed 30V per μs. The inherent slew rate of the MC1488 is much too fast for this requirement. The current limited output of the device can be used to control this slew rate by connecting a capacitor to each driver output. The required capacitor can be easily determined by using the relationship $C = I_{OS} \times \Delta T/\Delta V$ from which Figure 12 is derived. Accordingly, a 330pF capacitor on each output will guarantee a worst case slew rate of 30V per μs.

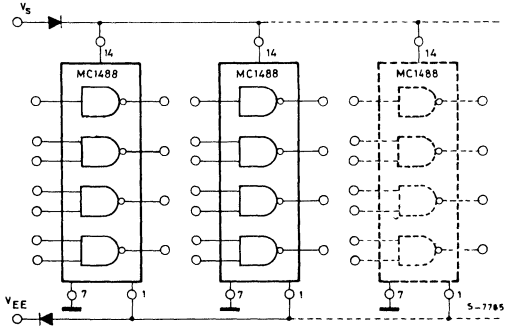
Fig. 12 - Slew rate vs. capacitance for I_{SC} = 10mA



The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15V, 500mA source. The MC1488 is designed to indefinitely withstand such a short to all four outputs in a package as long as the power-supply voltages are greater than 9.0V (i.e., $V_S \geq 9.0V$; $V_{EE} \leq -9.0V$). In some power-supply designs, a loss of system power causes a low impedance on the power-supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the MC1488 effectively shorting the 300Ω output resistor to ground. If **all four outputs** were then shorted to plus or minus 15V, the power dissipation in these resistors would be excessive. Therefore, if the system is designed to permit low impedances to ground at the power-supplies of the drivers, a diode should be placed in each power-supply lead to prevent over-heating in this fault condition. These two diodes, as shown in Figure 13, could be used to decouple all the driver packages in a system. (These same diodes will allow the MC1488 to withstand momentary shorts to the ± 15V limits specified in the earlier Standard RS232B). The addition of the diodes also permits the MC1488 to withstand faults with power-supplies of less than the 9.0V stated above.

The maximum short-circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10mA output current limiting.

Fig. 13 - Power supply protection to meet power-off fault conditions

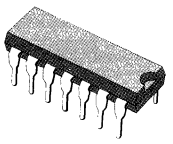


MC1489
MC1489A

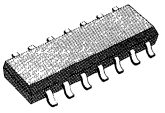
QUAD LINE RECEIVERS

- INPUT RESISTANCE – 3.0K to 7.0KΩ
- INPUT SIGNAL RANGE – ± 30V
- INPUT THRESHOLD HYSTERESIS BUILT-IN
- RESPONSE CONTROL:
  a) LOGIC THRESHOLD SHIFTING
  b) INPUT NOISE FILTERING

The MC1489 monolithic quad line receivers are designed to interface data therminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.



DIP-14 Plastic and Ceramic



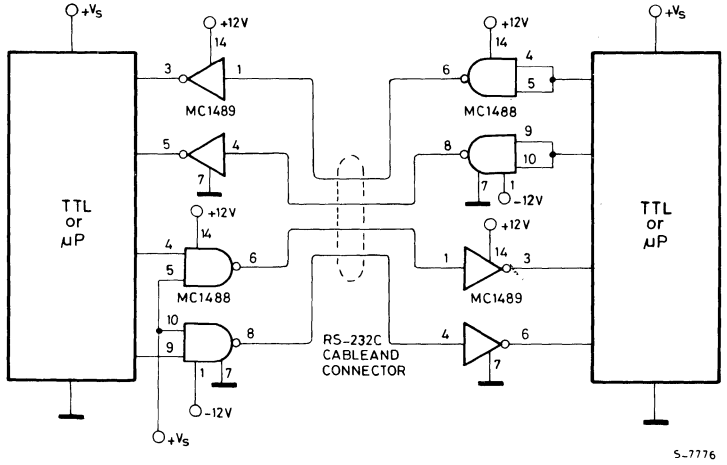
SO-14J

ABSOLUTE MAXIMUM RATINGS

V_S	Power supply voltage	10	V
V_i	Input voltage range	± 30	V
I_{OL}	Output load current	20	mA
P_{tot}	Power dissipation	1	W
T_{amb}	Operating ambient temperature	0 to 75	°C
T_{stg}	Storage temperature range	-65 to 150	°C

ORDERING NUMBER: MC1489L, MC1489AL (DIP-14 Ceramic)
MC1489P, MC1489AP (DIP-14 Plastic)
MC1489D, MC1489AD (SO-14)

Typical Application: RS232C data transmission



TEST CIRCUITS

Fig. 1 - Switching response

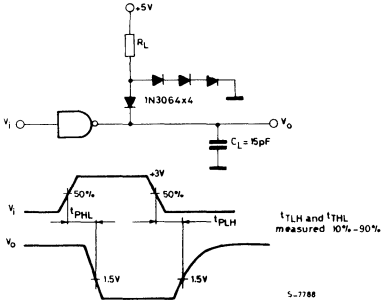
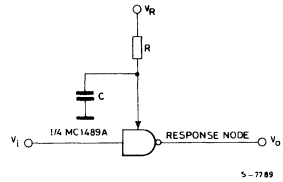


Fig. 2 - Response control node



C, capacitor is for noise filtering
R, resistor is for threshold shifting

Fig. 3 - Input current

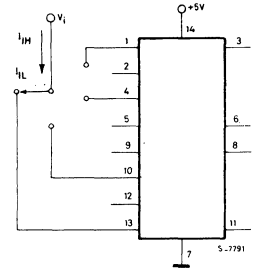


Fig. 4 - Output short-circuit current

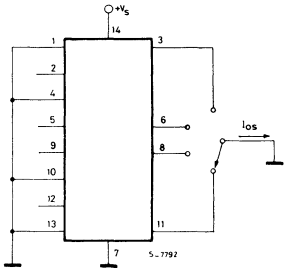


Fig. 5 - Output voltage and input threshold voltage

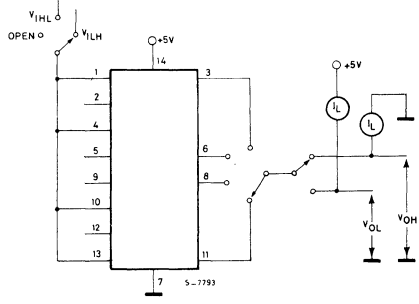
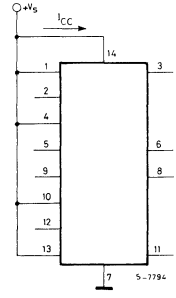


Fig. 6 - Power supply current



TYPICAL CHARACTERISTICS (V_S = 5V, T_{amb} = 25°C unless otherwise specified)

Fig. 7 - Input current

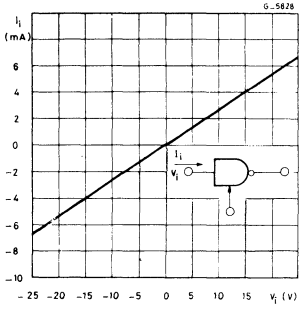


Fig. 8 - MC1489 input threshold voltage adjustament

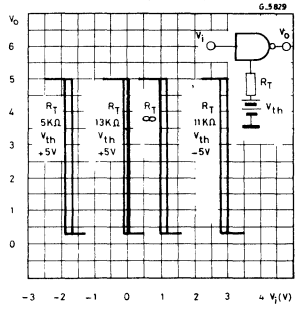
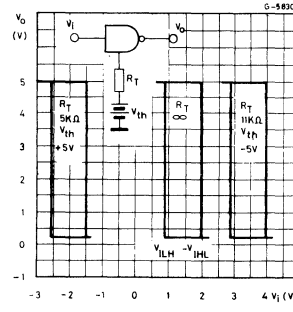


Fig. 9 - MC1489A input threshold voltage adjustment



APPLICATION INFORMATION (continued)

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above gorund or less than one diode below ground. This feature is demonstrated in Figure 11 where two receivers are slaved to the same line that must still meet the RS-232C impedance requirement.

Fig. 12 - Typical Turn-on threshold vs. capacitance from response control pin to GND

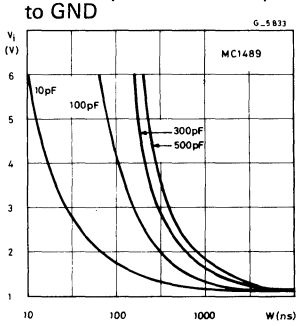


Fig. 13 - Typical Turn-on threshold vs. capacitance from response control pin to GND

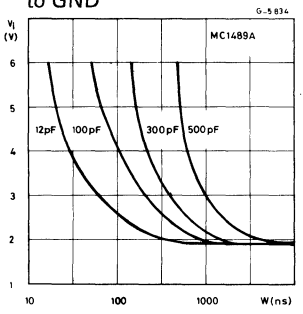
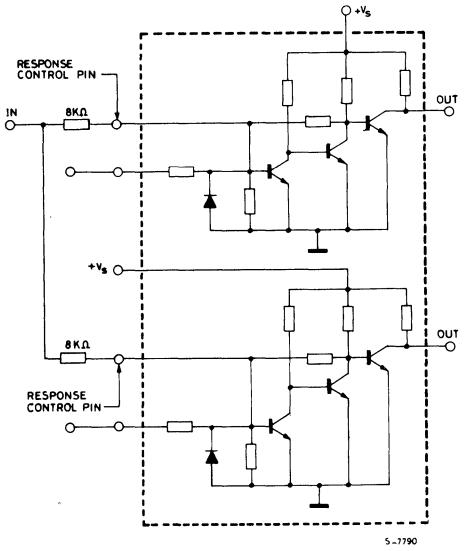


Fig. 14 - Typical paralleling of two MC1489/A receivers to meet RS-232C



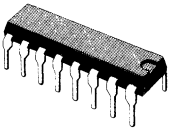
MC3479C

ADVANCE DATA

STEPPER MOTOR DRIVER

- SINGLE SUPPLY OPERATION +7.2V TO +16.5V
- 350mA/COIL DRIVE CAPABILITY
- CLAMP DIODES PROVIDED FOR BACK-EMF SUPPRESSION
- SELECTABLE $\overline{CW}$/CCW AND $\overline{FULL}$/HALF STEP OPERATION
- SELECTABLE HIGH/LOW OUTPUT IMPEDANCE (HALF STEP MODE)
- TTL/CMOS COMPATIBLE INPUTS
- INPUT HYSTERESIS: 250mV TYP.
- $\overline{PHASE\ LOGIC}$ CAN BE INITIALIZED TO $\overline{PHASE\ A}$
- $\overline{PHASE\ A}$ OUTPUT DRIVE STATE INDICATION

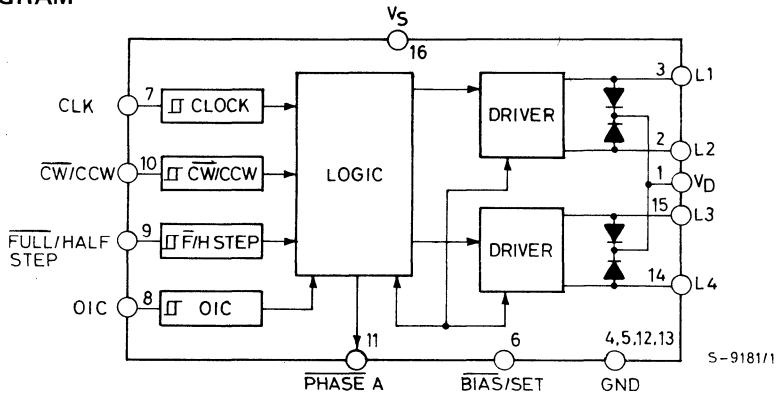
The MC3479C is designed to drive a two-phase stepper motor in the bipolar mode. The circuit consists of four input selections a logic decoding/sequencing section two driver stages for the motor coils and an output to indicate the Phase A drive state.



Powerdip
12 + 2 + 2

ORDERING NUMBER: MC3479C

BLOCK DIAGRAM



INPUT TRUTH TABLE

	INPUT LOW	INPUT HIGH
$\overline{CW}$/CCW	CW	CCW
$\overline{F}$/HS	Full Step	Half Step
OIC	High Z	Low Z
CLK	Positive Edge Triggered	

PIN DESCRIPTION

NAME	SYMBOL	PINS	DESCRIPTION
POWER SUPPLY	V_S	16	Power supply pin for both the logic circuit and the motor coil current. Voltage range is 7.2V to 16V.
GROUND	GND	4-5-12-13	Ground pins for the logic circuit and the motor coil current. The physical configuration of the pins dissipating heat from within the package.
CLAMP DIODE	V_D	1	This pin is used to protect the outputs where large voltage spikes may occur as the motor coils are switched. Typically a diode is connected between this pin and pin 16. See fig. 5.
DRIVER OUTPUTS	L1, L2 L3, L4	2-3 14-15	High current outputs for the motor coils. L1 and L2 are connected to one coil and L3 and L4 to the other coil.
$\overline{\text{BIAS}}$/SET	$\overline{\text{B}}$/S	6	This pins is typically 0.7V below V_S. The current out of this pin (through a resistor to ground) determines the maximum output sink current. If the pin is opened ($I_{BS} < 5.0\mu A$) the outputs assume a high impedance condition while the internal logic presets to a Phase A condition.
CLOCK	CK	7	The positive edge of the clock input switches the outputs to the next position. This input has no effect if pin 6 is open.
$\overline{\text{FULL}}$/HALF STEP	$\overline{\text{F}}$/HS	9	When low (logic 0) each clock pulse will cause the motor to rotate one full step. When high, each clock pulse will cause the motor to rotate one-half step. (See fig. 4 for sequence).
$\overline{\text{CLOCKWISE}}$ COUNTERCLOCKWISE	$\overline{\text{CW}}$/CCW	10	This input allows reversing the rotation of the rotation of the motor. (See fig. 4 for sequence).
OUT IMPEDANCE CONTROL	OIC	8	This input is relevant only in the half step mode (pin 9 > 2V). When low (logic 0) the two driver out of the non-energized coil will be in a high impedance condition. When high the same driver outputs will be at a low impedance reference to V_S. (See fig. 4).
$\overline{\text{PHASE A}}$	$\overline{\text{Ph A}}$	11	This outputs indicates (when low) that the driver outputs are in the phase A condition ($L1 = L3 = V_{OHD}$; $L2 = L4 = V_{OLD}$)

AC SWITCHING CHARACTERISTICS (T_{amb} = 25°C; V_M = 12V)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
f_{CK}	Clock frequency		0		30	KHz
PWCKH	Clock pulse width	HIGH	10			µs
PWCKL	Clock pulse width	LOW	20			µs
t_{SU}	Set-up time $\overline{CW}$/CCW and $\overline{F}$/HS		5			µs
t_{HO}	Hold time $\overline{CW}$/CCW and $\overline{F}$/HS		10			µs
t_{PCD}	Propagation delay CLK-to driver out			8		µs
t_{PBSD}	Propagation delay $\overline{Bias}$/set to driver output			1		µs
t_{PHLA}	Propagation delay CLK-to phase A LOW			12		µs
t_{PLHA}	Propagation delay CLK-to phase A HIGH			5		µs

Fig. 1 - AC test circuit

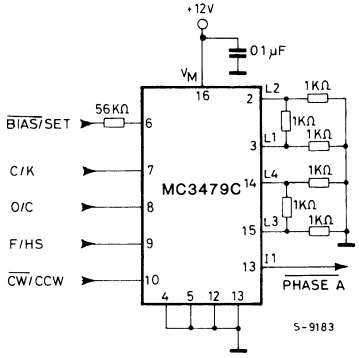


Fig. 2 - BIAS/SET TIMING (refer to fig. 1)

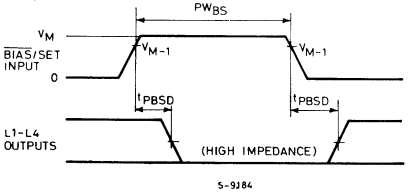


Fig. 3 - CLOCK TIMING (refer to fig. 1)

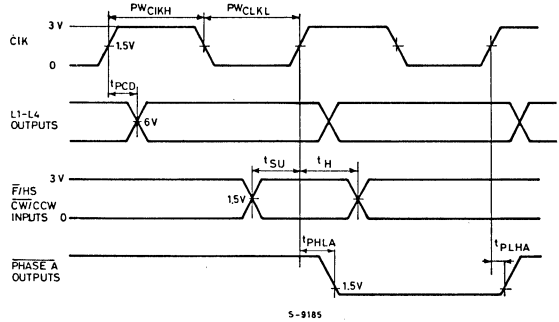
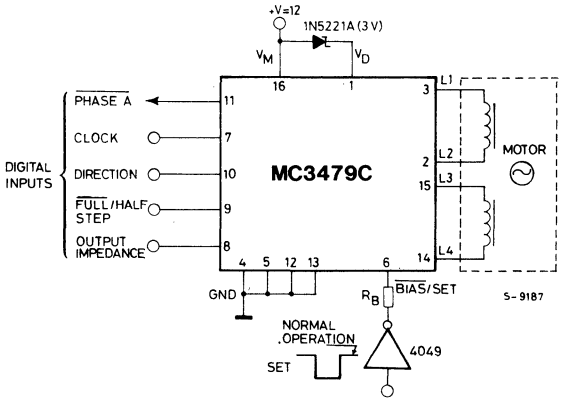


Fig. 5 - Typical application circuit



PBL3717A

PRELIMINARY DATA

STEPPER MOTOR DRIVER

- FULL STEP - HALF STEP - QUARTER STEP OPERATING MODE
- BIPOLAR OUTPUT CURRENT UP TO 1A
- FROM 10V UP TO 46V MOTOR SUPPLY VOLTAGE
- LOW SATURATION VOLTAGE WITH INTEGRATED BOOTSTRAP
- BUILT IN FAST PROTECTION DIODES
- EXTERNALLY SELECTABLE CURRENT LEVEL
- OUTPUT CURRENT LEVEL DIGITALLY OR ANALOGUE CONTROLLED
- THERMAL PROTECTION WITH SOFT INTERVENTION

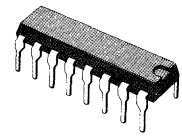
The PBL3717A is a monolithic IC which controls and drives one phase of a bipolar stepper motor with chopper control of the phase current. Current levels may be selected in three steps by means of two logic inputs which select one of three current comparators. When both of these inputs are high the device is disabled. A separate logic input controls the direction of current flow.

A monostable, programmed by an external RC network, sets the current decay time.

The power section is a full H-bridge driver with four internal clamp diodes for current recirculation. An external connection to the lower emitters is available for the insertion of a sensing resistor. Two PBL3717As and few external components form a complete stepper motor drive subsystem.

The raccomended operating ambient temperature range is from 0 to 70°C.

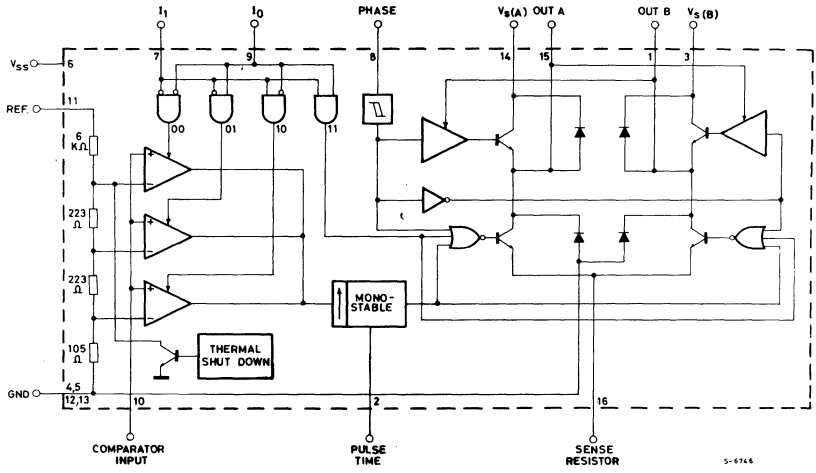
The PBL3717A is supplied in a 12 + 2 + 2 lead Powerdip package.



Powerdip 12 + 2 + 2

ORDERING NUMBER: PBL3717A

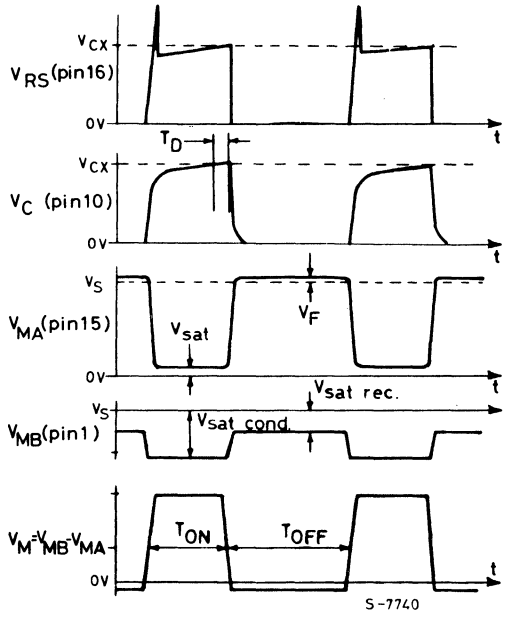
BLOCK DIAGRAM



PIN FUNCTIONS

N°	NAME	FUNCTION
1	OUTPUT B	Output connection (with pin 15). The output stage is a "H" bridge formed by four transistors and four diodes suitable for switching applications.
2	PULSE TIME	A parallel RC network connected to this pin sets the OFF time of the lower power transistors. The pulse generator is a monostable triggered by the rising edge of the output of the comparators ($t_{off} = 0.69\ R_T C_T$).
3	SUPPLY VOLTAGE B	Supply voltage input for halp output stage. see also pin 14.
4	GROUND	Ground connection. With pins 5, 12 and 13 also conducts heat from die to printed circuit copper.
5	GROUND	See pin 4.
6	LOGIC SUPPLY	Supply voltage input for logic circuitry.
7	INPUT 1	This pin and pin 9 (INPUT 0) are logic inputs which select the outputs of the three comparators to set the current level. Current also depends on the sensing resistor and reference voltage. See truth table.
8	PHASE	This TTL-compatible logic input sets the direction of current flow through the load. A high level causes current to flow from OUTPUT A (source)to OUTPUT B (sink). A schmitt trigger on this input provides good noise immunity and a delay circuit prevents output stage short circuits during switching.
9	INPUT 0	See INPUT 1 (pin 7).
10	COMPARATOR INPUT	Input connected to the three comparators. The voltage across the sense resistor is feedback to this input through the low pass filter $R_c\ C_c$. The lower power transistor are disabled when the sense voltage exceeds the reference voltage of the selected comparator. When this occurs the current decays for a time set by $R_T\ C_T$, $t_{off} = 0.69\ R_T\ C_T$.
11	REFERENCE	A voltage applied to this pin sets the reference voltage of the three comparators, this determining the output current (also thus depending on R_s and the two inputs INPUT 0 and INPUT 1).
12	GROUND	See pin 4.

Fig. 2 - Waveforms with MA regulating (phase = 0)



ELECTRICAL CHARACTERISTICS (Refer to the test circuit V_s = 36V, V_{ss}= 5V, T_{amb}= 25°C unless otherwise specified)

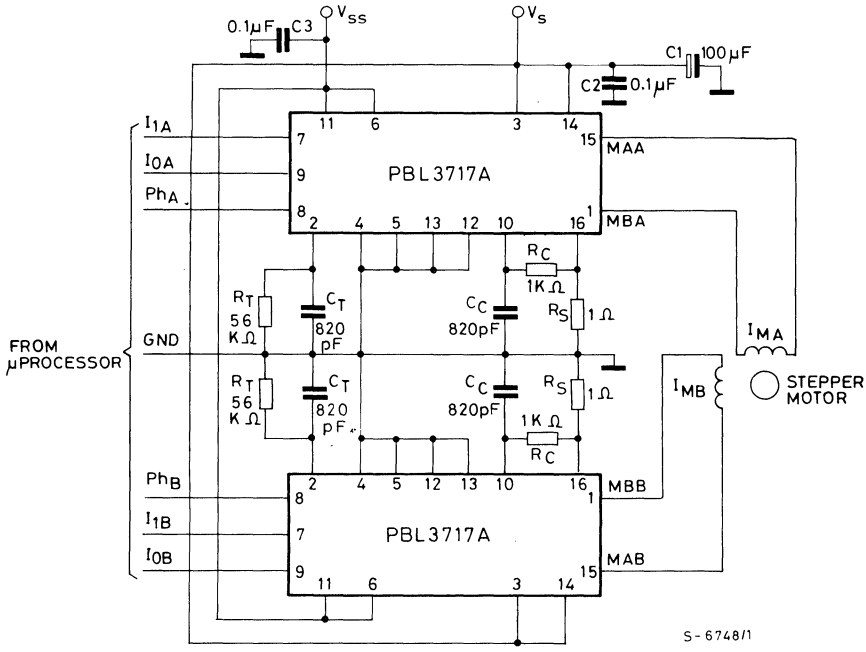
Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage (pins 3, 14)		10		46	V
V_{ss}	Logic supply voltage (pin 6)		4.75		5.25	V
I_{ss}	Logic supply current (pin 6)			7	15	mA
I_R	Reference input current (pin 11)	V_R = 5V		0.75	1	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
SINK DIODE-TRANSISTOR PAIR						
V_{sat}	Saturation voltage (pins 1, 15)	I_M = 0.5A		1.1	1.35	V
		I_M = 1A		1.6	2.3	V
I_{LK}	Leakage current	V_s = 46V			300	μA
V_F	Diode forward voltage	I_M = 0.5A		1.1	1.5	V
		I_M = 1A		1.4	2	

APPLICATION CIRCUIT

Fig. 3 - Two phase bipolar stepper motor driver



APPLICATION INFORMATIONS

Fig. 3 shows a typical application in which two PBL3717A control a two phase bipolar stepper motor.

Programming

The logic inputs I_0 and I_1 set at three different levels the amplitude of the current flowing in the motor winding according to the truth table of page 2. A high level on the "PHASE" logic input sets the direction of that current from output A to output B; a low level from output B to output A.
It is recommended that unused inputs are tied to pin 6 (V_{ss}) or pin 4 (GND) as appropriate to avoid noise problem.
The current levels can be varied continuously by changing the ref. voltage on pin 11.

Control of the motor

The stepper motor can rotate in either directions according to the sequence of the input signals. It is possible to obtain a full step, a half step and a quarter step operation.

Full step operation

Both the windings of the stepper motor are energized all the time with the same current $I_{MA} = I_{MB}$.
I_0 and I_1 remain fixed at whatever torque value is required.
Calling A the condition with winding A energized in one direction and $\overline{A}$ in the other direction, the sequence for full step rotation is:

$$A\,B \rightarrow \overline{A}\,B \rightarrow \overline{A}\,\overline{B} \rightarrow A\,\overline{B} \text{ etc.}$$

For the rotation in the other direction the sequence must be reversed.
In the full step operation the torque is constant each step.

Half step operation

Power is applied alternately to one winding then both according to the sequence:

$$A\,B \rightarrow B \rightarrow \overline{A}\,B \rightarrow \overline{A} \rightarrow \overline{A}\,\overline{B} \rightarrow \overline{B} \rightarrow A\,\overline{B} \rightarrow A \text{ etc.}$$

Like full step this can be done at any current level; the torque is not constant but it is lower when only one winding is energized
A coil is turned off by setting I_0 and I_1 both high.

Quarter step operation

It is preferable to realize the quarter step operation at full power otherwise the steps will be of very irregular size.
The extra quarter steps are added to the half step sequence by putting one coil on half current according to the sequence.

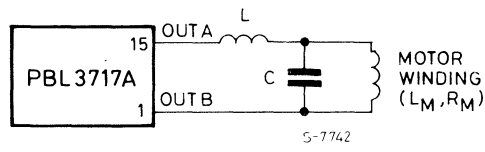
$$A\,B \rightarrow \frac{A}{2}B \rightarrow B \rightarrow \frac{\overline{A}}{2}B \rightarrow \overline{A}\,B \rightarrow \overline{A}\,\frac{B}{2} \rightarrow \overline{A} \text{ etc.}$$

Motor selection

As the PBL3717A provides constant current drive, with a switching operation, care must be taken to select stepper motors with low hysteresis losses to prevent motor over heat.

L-C filter

To reduce EMI and chopping losses in the motor a low pass L-C filter can be inserted across the outputs of the PBL3717A as shown on the following picture.



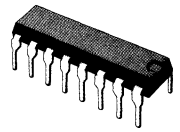
$$L \cong \frac{1}{10} L_M \qquad C \cong \frac{4 \cdot 10^{-10}}{L}$$

SG1524
SG2524
SG3524

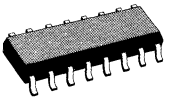
REGULATING PULSE WIDTH MODULATORS

- COMPLETE PWM POWER CONTROL CIRCUITRY
- UNCOMMITTED OUTPUTS FOR SINGLE-ENDED OR PUSH PULL APPLICATIONS
- LOW STANDBY CURRENT..8mA TYPICAL
- OPERATION UP TO 300 KHz
- 1% MAXIMUM TEMPERATURE VARIATION OF REFERENCE VOLTAGE

The SG1524, SG2524, and SG3524 incorporate on a single monolithic chip all the function required for the construction of regulating power supplies inverters or switching regulators. They can also be used as the control element for high power-output applications. The SG1524 family was designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers and polarity converter applications employing fixed-frequency, pulse-width modulation techniques. The dual alternating outputs allows either single-ended or push-pull applications. Each device includes an on-chip reference, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted output transistors, a high-gain comparator, and current-limiting and shut-down circuitry.



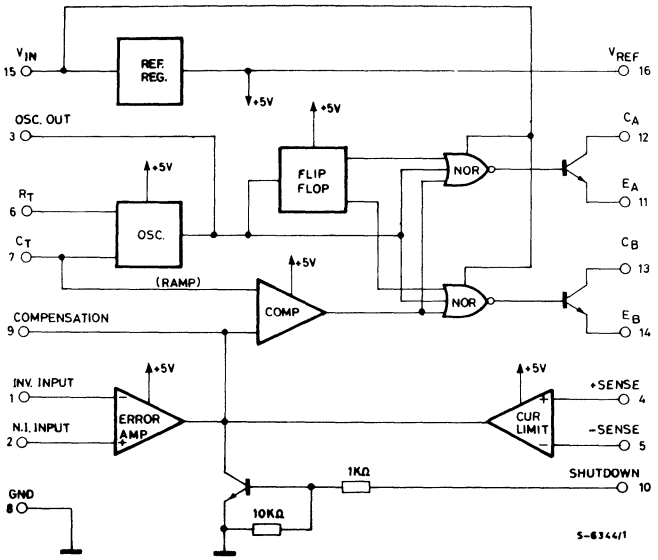
DIP-16 Plastic (0.25) **and Ceramic**



SO-16P

ORDERING NUMBERS: SG1524J - SG2524J - SG3524J (Ceramic)
SG2524N - SG3524N (Plastic)
SG2524P - SG3524P (SO-16P)

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_j = -55°C to + 125°C for the SG1524, -25°C to + 85°C for the SG2524, and 0°C to + 70°C for the SG3524, V_{IN} = 20V, and f = 20KHz).

Parameter		Test condition	SG1524/SG2524			SG3524			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
REFERENCE SECTION									
V_{REF}	Output Voltage		4.8	5	5.2	4.6	5	5.4	V
ΔV_{REF}	Line Regulation	V_{IN} = 8 to 40V		10	20		10	30	mV
ΔV_{REF}	Load Regulation	I_L = 0 to 20mA		20	50		20	50	mV
	Ripple Rejection	f = 120Hz, T_j = 25°C		66			66		dB
	Short Circuit Curr. Limit	V_{REF} = 0, T_j = 25°C		100			100		mA
$\Delta V_{REF}/\Delta T$	Temp. Stability	Over Operating Temp. Range		0.3	1		0.3	1	%
ΔV_{REF}	Long Term Stability	T_j = 25°C, t = 1000 Hrs.		20			20		mV
OSCILLATOR SECTION									
f_{MAX}	Maximum Frequency	C_T = 0.001μF, R_T = 2kΩ		300			300		kHz
	Initial Accuracy	R_T and C_T Constant		5			5		%
	Voltage Stability	V_{IN} = 8 to 40V, T_j = 25°C			1			1	%
$\Delta f/\Delta T$	Temperature Stability	Over Operating Temp. Range			2			2	%
	Output Amplitude	Pin 3, T_j = 25°C		3.5			3.5		V
	Output Pulse Width	C_T = 0.01μF, T_j = 25°C		0.5			0.5		μs
ERROR AMPLIFIER SECTION									
V_{os}	Input Offset Voltage	V_{CM} = 2.5V		0.5	5		2	10	mV
I_b	Input Bias Current	V_{CM} = 2,5V		2	10		2	10	μA
G_V	Open Loop Volt. Gain		72	80		60	80		dB
CMV	Common Mode Volt.	T_j = 25°C	1.8		3.4	1.8		3.4	V
CMR	Comm. Mode Rejec.	T_j = 25°C		70			70		dB
B	Small Signal Bandwidth	A_V = 0dB, T_j = 25°C		3			3		MHz
V_o	Output Voltage	T_j = 25°C	0.5		3.8	0.5		3.8	V
COMPARATOR SECTION									
	Duty-Cycle	% Each Output On	0		45	0		45	%
V_{IT}	Input Threshold	Zero Duty-Cycle		1			1		V
V_{IT}	Input Threshold	Maximum Duty-Cycle		3.5			3.5		V
I_b	Input Bias Current			1			1		μA
CURRENT LIMITING SECTION									
	Sense Voltage	Pin 9 = 2V with Error Amplifier Set for Max. Out, T_j = 25°C	190	200	210	180	200	220	mV
	Sense Voltage T.C.			0.2			0.2		mV/°C
CMV	Common Mode Volt.		-1		+1	-1		+1	V
OUTPUT SECTION (Each Output)									
	Collector-Emitter Volt.		40			40			V
	Collector Leackage Cur.	V_{CE} = 40V		0.1	50		0.1	50	μA
	Saturation Voltage	I_c = 50mA		1	2		1	2	V
	Emitter Out. Voltage	V_{IN} = 20V	17	18		17	18		V
t_r	Rise Time	R_c= 2KΩ, T_j = 25°C		0.2			0.2		μs
t_f	Fall time	R_c= 2KΩ, T_j= 25°C		0.1			0.1		μs
I_q*	Total Standby Curr.	V_{IN} = 40V		8	10		8	10	mA

(*) Excluding oscillator charging current, error and current limit dividers, and with outputs open.

outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current limiting and shutdown circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier, or to provide additional control to the regulator.

RECOMMENDED OPERATING CONDITIONS

Supply voltage V_{IN}	8 to 40	V
Reference Output Current	0 to 20	mA
Current through C_T Terminal	-0.03 to -2	mA
Timing Resistor, R_T	1.8 to 100	KΩ
Timing Capacitor, C_T	0.001 to 0.1	μF

TYPICAL APPLICATIONS DATA

Oscillator

The oscillator controls the frequency of the SG1524 and is programmed by R_T and C_T according to the approximate formula:

$$f \simeq \frac{1.18}{R_T C_T}$$

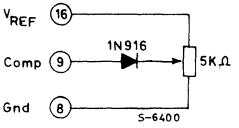
where R_T is in KΩ
C_T is in μF
f is in KHz

Pratical values of C_T fall between 0.001 and 0.1μF. Pratical values of R_T fall between 1.8 and 100KΩ. This results in a frequency range typically from 120Hz to 500KHz.

Blanking

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse width is controlled by the value of C_T. If small values of C_T are required for frequency control, the oscillator output pulse width may still be increased by applying a shunt capacitance of up to 100pF from pin 3 to ground. If still greater dead-time is required, it should be accomplished by limiting the maximum duty cycle by clamping the output of the error amplifier. This can easily be done with the circuit below:

Fig. 6

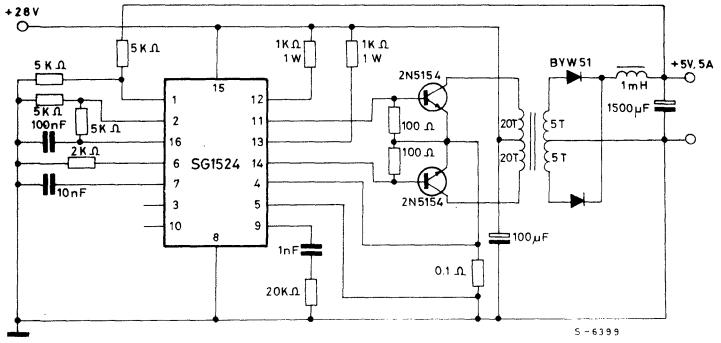


Synchronous Operation

When an external clock is desired, a clock pulse of approximately 3V can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2KΩ. In this configuration R_T C_T must be selected for a clock period slightly greater than that of the external clock.

If two more SG1524 regulators are to be operated synchronously, all oscillator output terminals should be tied together, all C_T terminals connected to a single timing capacitor, and the timing resistor connected to a single R_T terminal. The other R_T terminals can be left open or shorted to V_{REF}. Minimum lead lengths should be used between the C_T terminals.

Fig. 7 - Push-pull transformer-coupled circuit.



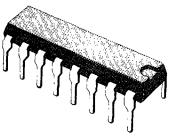
SG1525A/27A
SG2525A/27A
SG3525A/27A

REGULATING PULSE WIDTH MODULATORS

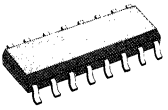
- 8 to 35V OPERATION
- 5.1V REFERENCE TRIMMED TO ± 1%
- 100Hz to 500KHz OSCILLATOR RANGE
- SEPARATE OSCILLATOR SYNC TERMINAL
- ADJUSTABLE DEADTIME CONTROL
- INTERNAL SOFT-START
- PULSE-BY-PULSE SHUTDOWN
- INPUT UNDERVOLTAGE LOCKOUT WITH HYSTERESIS
- LATCHING PWM TO PREVENT MULTIPLE PULSES
- DUAL SOURCE/SINK OUTPUT DRIVERS

The SG1525A/1527A series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip + 5.1V reference is trimmed to ± 1% and the input common-mode range of the error amplifier includes the reference voltage eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between the C_T and the discharge terminals provide a wide range of dead time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required.

A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages. this lockout circuitry includes approximately 500mV of hysteresis for jitter-free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWN pulses has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200mA. The SG1525A output stage features NOR logic, giving a LOW output for an OFF state. The SG1527A utilizes OR logic which results in a HIGH output level when OFF.



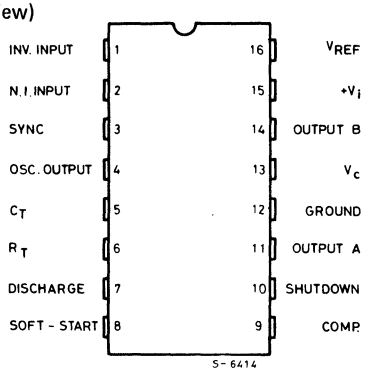
DIP-16 Plastic (0.25) **and Ceramic**



SO-16P

CONNECTION DIAGRAM AND ORDERING NUMBERS

(top view)



Type	Plastic DIP	Ceramic DIP	SO-16P
SG1525A	–	SG1525AJ	–
SG1527A	–	SG1527AJ	–
SG2525A	SG2525AN	SG2525AJ	SG2525AP
SG2527A	SG2527AN	SG2527AJ	SG2527AP
SG3525A	SG3525AN	SG3525AJ	SG3525AP
SG3527A	SG3527AN	SG3527AJ	SG3527AP

ELECTRICAL CHARACTERISTICS (V_i = 20V, and over operating temperature, unless otherwise specified)

Parameter		Test conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
REFERENCE SECTION									
V_{REF}	Output voltage	T_j = 25°C	5.05	5.1	5.15	5	5.1	5.2	V
ΔV_{REF}	Line regulation	V_i = 8 to 35V		10	20		10	20	mV
ΔV_{REF}	Load regulation	I_L = 0 to 20 mA		20	50		20	50	mV
$\Delta V_{REF}/\Delta T$*	Temp. stability	Over operating range		20	50		20	50	mV
*	Total output variation	Line, load and temperature	5		5.2	4.95		5.25	V
	Short circuit current	V_{REF}= 0 T_j = 25°C		80	100		80	100	mA
*	Output noise voltage	10Hz ⩽ f ⩽ 10kHz, T_j=25°C		40	200		40	200	μVrms
ΔV_{REF}*	Long term stability	T_j = 125°C, 1000 hrs		20	50		20	50	mV
OSCILLATOR SECTION**									
*, •	Initial accuracy	T_j = 25°C		± 2	± 6		± 2	± 6	%
*, •	Voltage stability	V_i = 8 to 35V		± 0.3	± 1		± 1	± 2	%
$\Delta f/\Delta T$*	Temp. stability	Over operating range		± 3	± 6		± 3	± 6	%
f_{MIN}	Minim. frequency	R_T = 200 KΩ C_T= 0.1 μF			120			120	Hz
f_{MAX}	Maxim. frequency	R_T = 2 KΩ C_T= 470 pF	400			400			KHz
	Current mirror	I_{RT}= 2 mA	1.7	2	2.2	1.7	2	2.2	mA
*, •	Clock amplitude		3	3.5		3	3.5		V
*, •	Clock width	T_j = 25°C	0.3	0.5	1	0.3	0.5	1	μs
	Sync threshold		1.2	2	2.8	1.2	2	2.8	V
	Sync input current	Sync voltage = 3.5V		1	2.5		1	2.5	mA
ERROR AMPLIFIER SECTION (V_{CM} = 5.1V)									
V_{OS}	Input offset voltage			0.5	5		2	10	mV

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
OUTPUT DRIVERS (Each output) (V_C = 20V)									
	Output low level	I_{sink} = 20 mA		0.2	0.4		0.2	0.4	V
		I_{sink} = 100 mA		1	2		1	2	V
	Output high level	I_{source} = 20 mA	18	19		18	19		V
		I_{source} = 100 mA	17	18		17	18		V
	Under-voltage lockout	V_{comp} and V_{ss} = high	6	7	8	6	7	8	V
I_C	Collector leakage	V_C = 35V			200			200	μA
t_r*	Rise time	C_L = 1 nF, T_j = 25°C		100	600		100	600	ns
t_f*	Fall time	C_L = 1 nF, T_j = 25°C		50	300		50	300	ns
TOTAL STANDBY CURRENT									
I_S	Supply current	V_i = 35V		14	20		14	20	mA

* These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

• Tested at f_{osc}= 40 KHz (R_T = 3.6 KΩ, C_T = 0.1 μF, R_D = 0Ω). Approximate oscillator frequency is defined by:

$$f = \frac{1}{C_T (0.7\ R_T + 3\ R_D)}$$

▪ DC transconductance (g_M) relates to DC open-loop voltage gain (G_V) according to the following equation: $G_V = g_M R_L$ where R_L is the resistance from pin 9 to ground. The minimum g_M specification is used to calculate minimum G_V when the error amplifier output is loaded.

RECOMMENDED OPERATING CONDITIONS (•)

Input voltage (V_i)	8 to 35 V
Collector supply voltage (V_C)	4.5 to 35 V
Sink/source load current (steady state)	0 to 100 mA
Sink/source load current (peak)	0 to 400 mA
Reference load current	0 to 20 mA
Oscillator frequency range	100 Hz to 400 KHz
Oscillator timing resistor	2 KΩ to 150 KΩ
Oscillator timing capacitor	0.001 μF to 0.1 μF
Dead time resistor range	0 to 500 Ω

(•) Range over which the device is functional and parameter limits are guaranteed.

Fig. 1 - Oscillator charge time vs. R_T and C_T

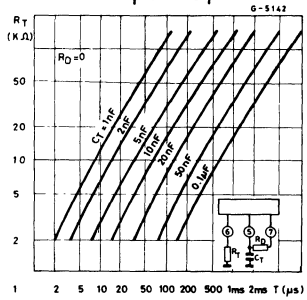


Fig. 2 - Oscillator discharge time vs. R_D and C_T

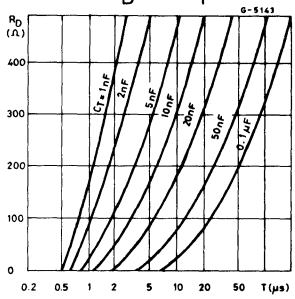


Fig. 3 - SG1525A output saturation characteristics

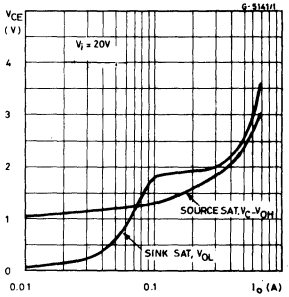


Fig. 4 - Error amplifier voltage gain and phase vs. frequency

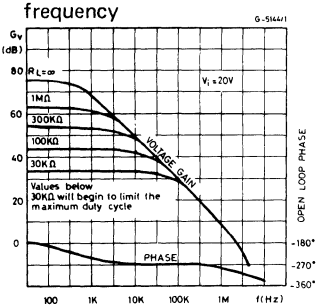
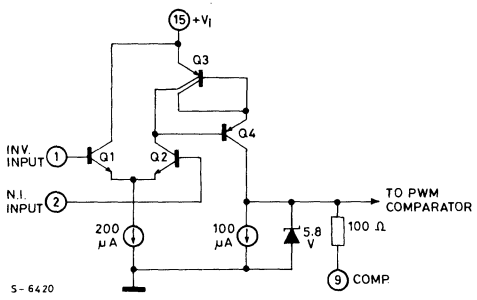


Fig. 5 - SG1525A error amplifier



PRINCIPLES OF OPERATION

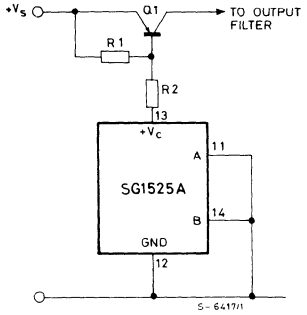
SHUTDOWN OPTIONS (See Block Diagram)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100 μA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions: the PWM latch is immediately set providing the fastest turn-off signal to the outputs; and a 150 μA current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

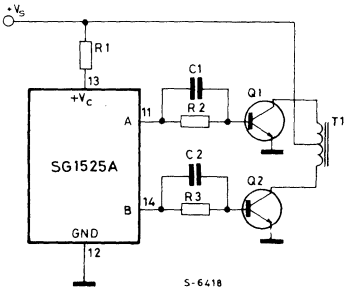
Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

Fig. 7



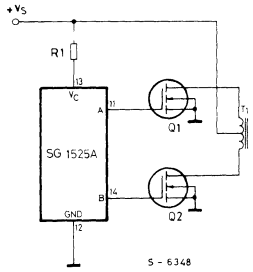
For single-ended supplies, the driver outputs are grounded. The V_c terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

Fig. 8



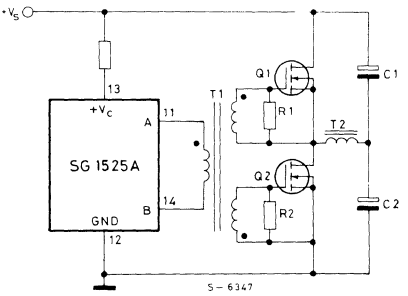
In conventional push-pull bipolar designs, forward base drive is controlled by R_1-R_3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C_1 and C_2.

Fig. 9



The low source impedance of the output drivers provides rapid charging of Power Mos input capacitance while minimizing external components.

Fig. 10



Low power transformers can be driven directly by the SG1525A. Automatic reset occurs during dead time, when both ends of the primary winding are switched to ground.

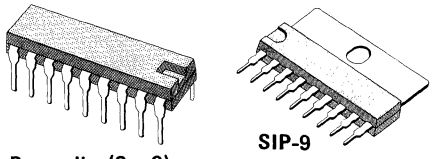
TDA4601

SWITCH-MODE POWER SUPPLY CONTROLLER

- LOW START-UP CURRENT
- DIRECT CONTROL OF SWITCHING TRANSISTOR
- COLLECTOR CURRENT PROPORTIONAL TO BASE-CURRENT INPUT
- REVERSE-GOING LINEAR OVERLOAD CHARACTERISTIC CURVE.

The TDA4601 is a monolithic integrated circuit designed to regulate and control the switching transistor of a switching power supply.

Because of its wide operational range and high voltage stability even at high load changes: this IC can be used not only in TV receivers and video recorders but also in power supplies in Hi-Fi sets and active speakers.

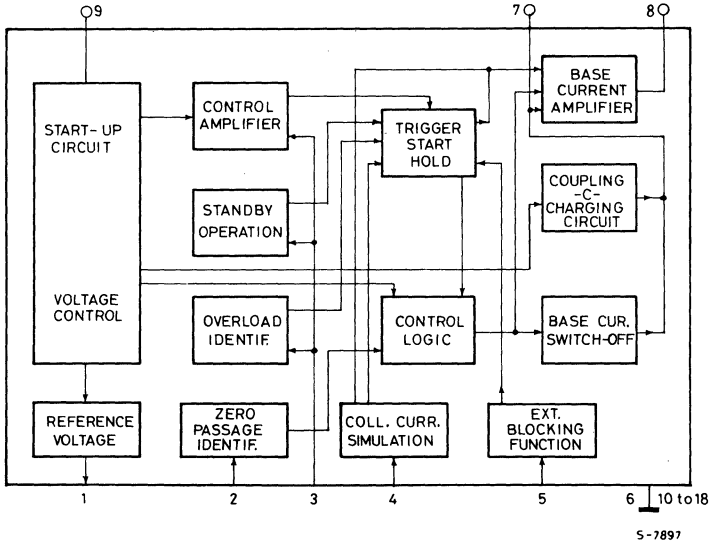


SIP-9

Powerdip (9 + 9)

ORDERING NUMBER: TDA4601 (SIP-9)
TDA4601B (9 + 9)

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_9	Operating supply voltage range		7.8		18	V

Start condition (according to test circuit of fig. 1)

I_9	Supply current (V_1 not yet switched on)	V_9 = 2V V_9 = 5V V_9 = 10V		 1.5 2.4	0.5 2.0 3.2	mA mA mA
V_9	Switch threshold (V_1)		11	11.8	12.3	V

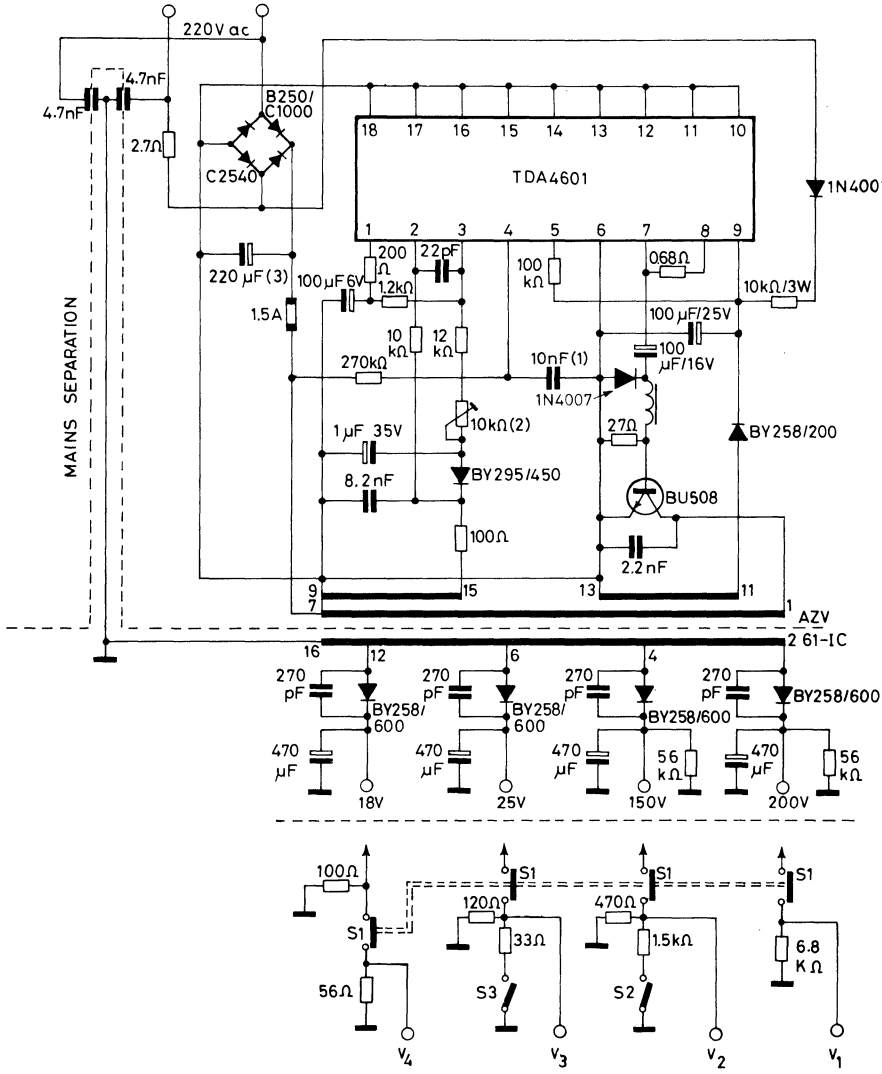
Normal operation (V_9 = 10V, V_{cont} = -10V, V_{clock} = ±0.5V, f = 20KHz, duty cycle 1:2 after switch on)

I_9	Supply current	V_{cont} = -10V V_{cont} = 0V	110 50	135 75	160 100	mA mA
V_{ref}	Voltage reference at pin 1	I_1 < 0.1 mA I_1 = 5 mA	4 4	4.2 4.2	4.5 4.4	V V
V_3	Control voltage	V_{cont} = 0V	2.3	2.6	2.9	V
V_4	Collector current simulation voltage	V_{cont} = 0V (see Note 1)	1.8	2.2	2.5	V
ΔV_4	Collector current simulation voltage	V_{cont} = 0V to -10V (see note 1)	0.3	0.4	0.5	V
V_5	External protection threshold		6	7	8	V
V_7	Pin 7 output voltage	V_{cont} = 0V (see note 1)	2.7	3.3	4.0	V
V_8	Pin 8 output voltage	V_{cont} = 0V (see note 1)	2.7	3.4	4.0	V
V_8	Pin 8 output voltage change	V_{cont} 0V to -10V (see note 1)	1.6	2	2.4	V
V_2	Feedback voltage	(see note 1)		0.2		V
T_{K1}	Reference voltage temperature coeffic.			10^{-3}		1/K

Protection operation (V_9 = 10V; V_{cont} = -10V; V_{clock} = ± 0,5V; f = 20KHz; duty cycle 1 : 2)

I_9	Supply current	$V_5 \leq 1.8V$	14	22	28	mA
V_7	Switch-off voltage	$V_5 \leq 1.8V$	1.3	1.5	1.8	V
V_4			1.8	2.1	2.5	V

Fig. 2 - Test and application circuit



1) C limits the max. collector current of BU508 at overshooting the permissible output power.
2) Adjustment of secondary voltage.
3) Must be discharged before IC change.

Fig. 3 - Frequency vs. output power (test circuit of fig. 2).

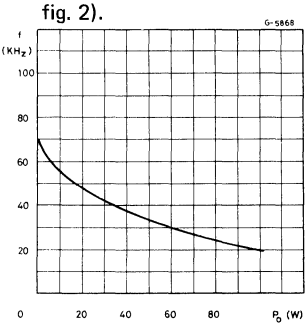


Fig. 4 - Efficiency vs. output power test circuit of fig. 2).

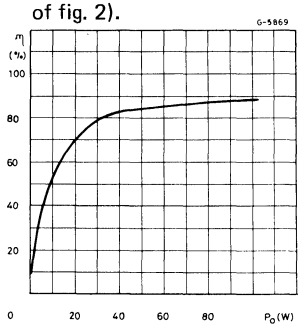


Fig. 5 - Load characteristics V_2-f (Iq2) (test circuit of fig. 2).

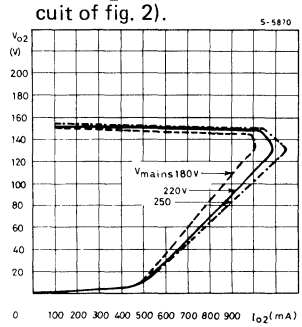


Fig. 6 - Output voltage V_2 (mains change) (test circuit of fig. 2).

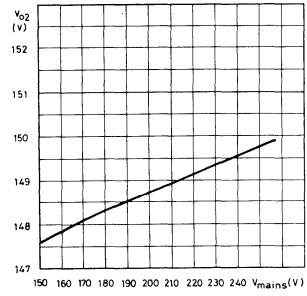
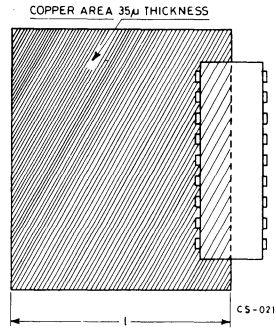


Fig. 7 - Example of a PC heatsink (35°C/W)



TDA7272

ADVANCE DATA

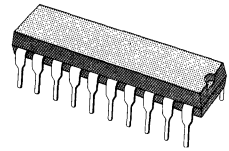
HIGH PERFORMANCE MOTOR SPEED REGULATOR

- TACHIMETRIC SPEED REGULATION WITH NO NEED FOR AN EXTERNAL SPEED PICK-UP
- V/I SUPPLEMENTARY PREREGULATION
- DIGITAL CONTROL OF DIRECTION AND MOTOR STOP
- SEPARATE SPEED ADJUSTMENT
- 5V TO 18V OPERATING SUPPLY VOLTAGE
- 1A PEAK OUTPUT CURRENT
- OUTPUT CLAMP DIODES INCLUDED
- SHORT CIRCUIT CURRENT PROTECTION
- THERMAL SHUT DOWN WITH HYSTERESIS
- DUMP PROTECTION (40V)

TDA7272 is an high performance motor speed controller for small power DC motors as used in cassette players.

Using the motor as a digital tachogenerator itself the performance of true tacho controlled systems is reached.

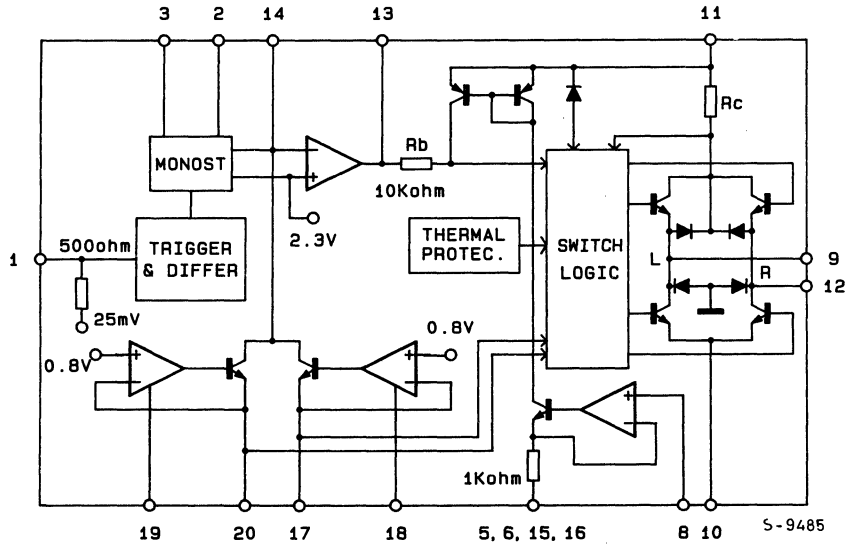
A dual loop control circuit provides long term stability and fast settling behaviour.



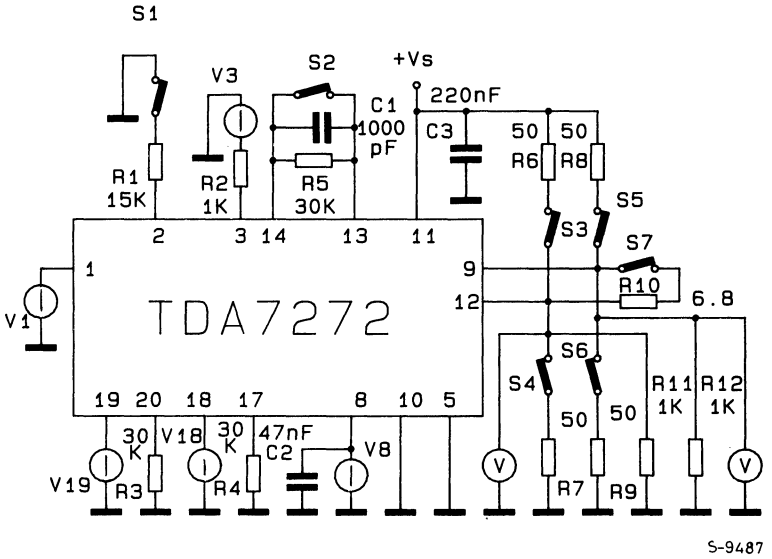
Powerdip (16 + 2 + 2)

ORDERING NUMBER: TDA7272

BLOCK DIAGRAM



TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C; V_S = 13.5V unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating supply voltage		5		18	V
I_S	Supply current	No load		5	12	mA
OUTPUT STAGE						
I_O	Output current pulse		1			A
I_O	Output current continuous		250			mA
$V_{10-9,\ 12}$	Voltage drop	I_O = 250mA		1.2	1.5	V
$V_{11-9,\ 12}$	Voltage drop	I_O = 250mA		1.7	2	V

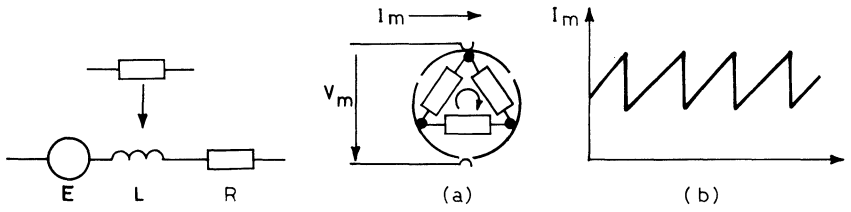
OPERATING PRINCIPLE

The TDA7272 novel applied solution is based on a tachometer control system without using such extra tachometer system. The information of the actual motor speed is extracted from the motor itself. A DC motor with an odd number of poles generates a motor current which contains a fixed number of discontinuitues within each rotation. (6 for the 3 pole motor example on Fig. 1)

Deriving this inherent speed information from the motor current, it can be used as a replacement of a low resolution AC tachometer system. Because the settling time of the control loop is limited on principle by the resolution in time of the tachometer, this control principle offers a poor reaction time for motors with a low number of poles. The realized circuit is extended by a second feed forward loop in order to improve such system by a fast auxiliary control path.

This additional path senses the mean output current and varies the output voltage according to the voltage drop across the inner motor resistance. Apart from a current averaging filter, there is no delay in such loop and a fast settling behaviour is reached in addition to the long term speed motor accuracy.

Fig. 1 - Equivalent of a 3 pole DC motor (a) and typical motor current waveform (b)



S-9494

BLOCK DESCRIPTION

The principle structure of the element is shown in Fig. 2. As to be seen, the motor speed information is derived from the motor current sense drop across the resistor R_S; capacitor CD together with the input impedance of 500Ω at pin 1 realizes a high pass filter.

This pin is internally biased at 25mV, each negative zero transition switches the input comparator. A 10mV hysteresis improves the noise immunity.

The trigger circuit is followed by an internal delay time differentiator.

Thus, the system becomes widely independent of the applied waveform at pin 1, the differentiator triggers a monostable circuit which provides a constant current duration. Both, output current magnitude and duration T, are adjustable by external elements CT and RT.

The monostable is retriggerable; this function prevents the system from fault stabilization at higher harmonics of the nominal frequency.

The speed programming current is generated by two separate external adjustable current sources. A corresponding digital input signal enables each current source for left or right rotation direction. Resistor RP1 and RP2 define the speed, the logical inputs are at pin 18 and 19.

At the inverting input (pin 14) of the main amplifier the reference current is compared with the pulsed monostable output current.

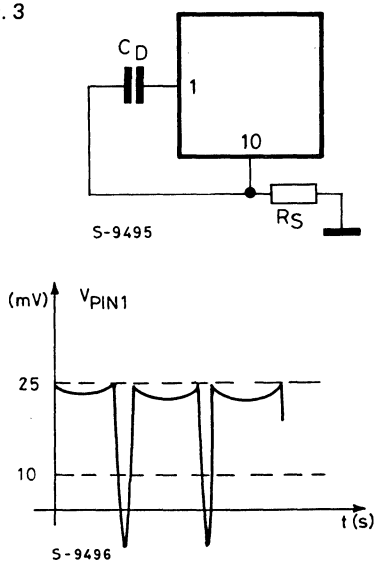
For the correct motor speed, the reference current matches the mean value of the pulsed monostable current. In this condition the charge of the feedback capacitor becomes constant.

PIN FUNCTION AND APPLICATION INFORMATION

Pin 1

Trigger input. Receives a proper voltage which contains the information of the motor speed. The waveform can be derived directly by the motor current (Fig. 3). The external resistor generates a proper voltage drop. Together with the input resistance at pin 1 [R_{IN} (1) = 500Ω] the external capacitor C_D realize a high pass filter which differentiates the commutation spikes of the motor current. The trigger level is 0V.

Fig. 3

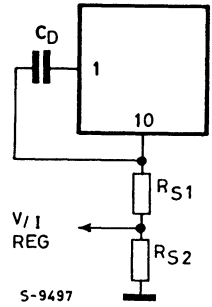


The biasing of the pin 1 is 25mV with a hysteresis of 10mV. So the sensing resistance must be chosen high enough in order to obtain a negative spike of the least 30mV on pin 1, also with minimum variation of motor current:

$$R_S \geqslant \frac{30mV}{\Delta I_{MOT}\ min.}$$

Such value can be too much high for the pre-regulation stage V-I and it could be necessary to split them into 2 series resistors $R_S = R_{S1} + R_{S2}$ (see fig. 4) as explained on pin 8 section.

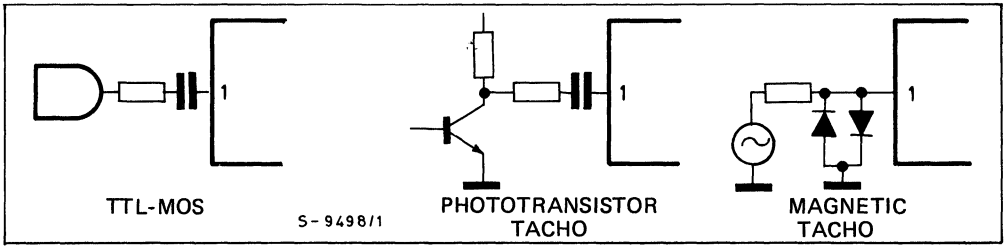
Fig. 4



The information can be taken also from an external tachogenerator. Fig. 5 shows various sources connections:

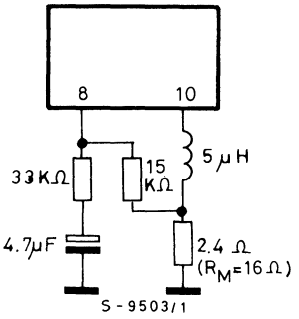
the input signal mustn't be lower than -0.7V.

Fig. 5



The low pass filter R_L, C_L must be calculated in order to reduce the ripple of the motor commutation at least 20dB. Another example of possible pins 10-8 connections is showed on Fig. 9. A choke can be used in order to reduce the radiation.

Fig. 9



Pin 9

Output motor left. The four power transistors are realized as darlington structures. The arrangement is controlled by the logic status at pins 18 and 19.

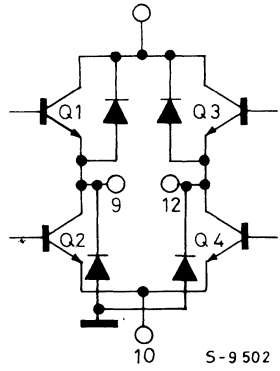
As before explained (see block description), in the normal left or right mode one of the lower darlington becomes saturated whereas the other remains open. The upper half of the bridge operates in the linear mode.

In stop condition both upper bridge darlingtons are off and both lower are on. In the high output impedance state the bridge is switched completely off.

Connecting the motor between pins 9 and 12 both left or right rotation can be obtained. If only one rotation sense is used the motor can be connected at only one output, by using only the upper bridge half. Two motors can be connected each at the each output: in such case they will work alternatively (See Application Section).

The internal diodes, together with the collector substrate diodes, protect the output from inductive voltage spikes during the transition phase.

Fig. 10



Pin 10

Common sense output. From this pin the output current of the bridge configuration (motor current) is fed into R_S external resistor in order to generate a proper voltage drop.

The drop is supplied into pin 1 for tachometric control and into pin 8 for V/I control (See pin 1 and pin 8 sections).

Pin 11

Supply voltage.

Pin 12

Output motor right. (See pin 9 section)

Pin 13

Output main amplifier. The voltage on this pin results from the tachometric speed control and feeds the output stage.

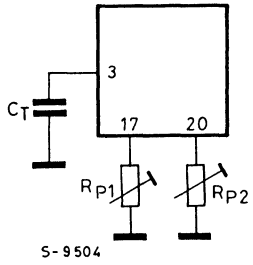
The value of the capacitor C_F (Fig. 4), connected from pins 13 and 14, must be chosen low enough in order to obtain a short reaction time of the tachometric loop, and high enough in order to reduce the output ripple.

A compromise is reached when the ripple voltage (peak-to-peak) V_{ROP} is equal to 0.1 V_{MOTOR}:

$$C_F = 2.3 \frac{C_T}{V_{RIP}} \left(1 - \frac{R_T}{R_P}\right)$$

$$\text{with } V_{RIP} = \frac{V_{FEM} + I_{MOT} \cdot R_{MOT}}{10} \text{ and}$$

Fig. 14



Pin 14

Inverting input of main amplifier. In this pin the current reference programmed at pins 20, 17 is compared with the current from the monostable (stream of rectangular pulses).

In steady-state condition (constant motor speed) the values are equal and the capacitor C_F voltage is constant.

This means for the speed n (min -1) :

$$n = \frac{10.435}{C_T \ m \ R_P}$$

where "m" is the number of collector segments. (poles)

The non inverting input of the main amplifier is internally connected to a reference voltage (2.3V).

Pin 15

Ground.

Pin 16

Ground.

Pin 17

Left speed adjustment. The voltage at this pin is fixed to a reference value of 0.8V. A resistor from this pin and ground (Fig. 14) fixes the reference current which will be compared with the medium output current of the monostable in order to fix the speed of the motor at the programmed value. The correct value of R_P would be:

$$R_P = \frac{10.435}{C_T \cdot m \cdot n} =$$

n = motor speed, (min -1)
m = poles number

Fig. 15

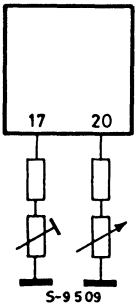


Fig. 16

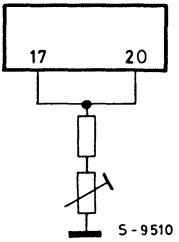


Fig. 17

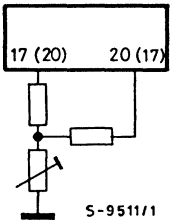


Fig. 18

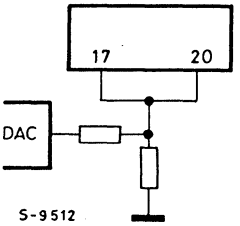


Fig. 21 - Tacho only speed regulation

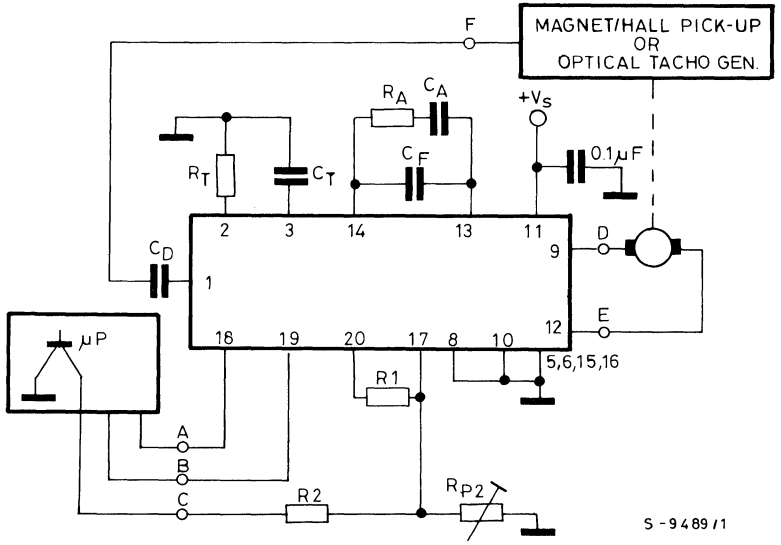


Fig. 22 - One direction reg. of one motor, or alternatively of two motors

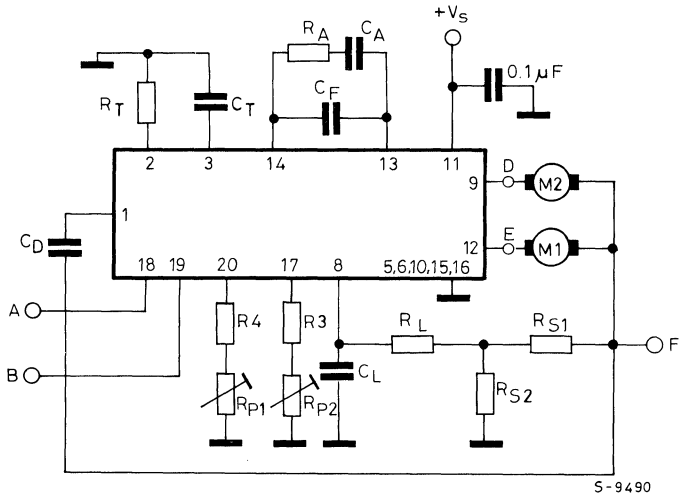


Fig. 24 - Speed regulation versus supply voltage (Circuit of Fig. 20)

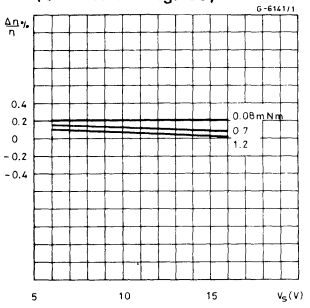


Fig. 25 - High current TDA7272 + 2 x L149 application

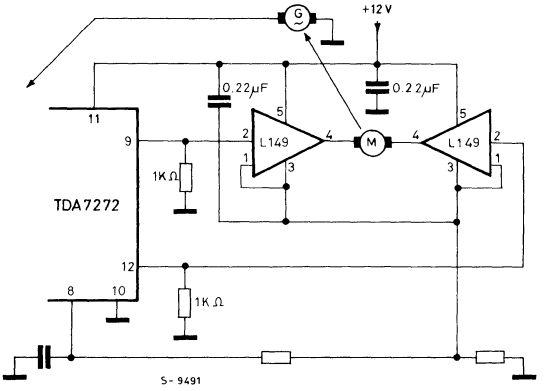
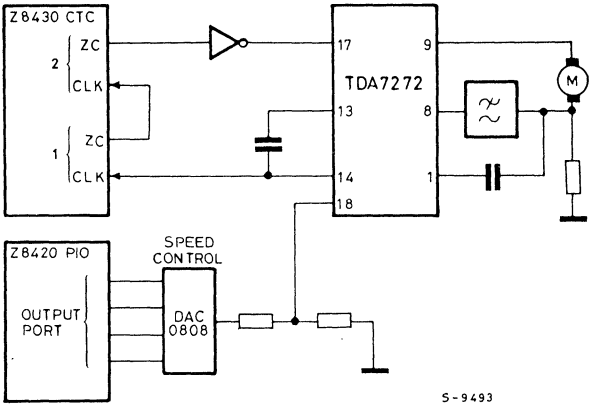


Fig. 26 - In connection with a presettable counter and I/O peripheral the TDA7272 controls the speed through a D/A converter



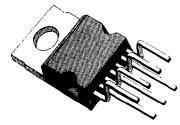
TDA8115

ADVANCE DATA

DUAL MOTOR DRIVER

- HIGH OUTPUT CURRENT, EACH CHANNEL UP TO 1A
- WIDE SUPPLY VOLTAGE RANGE, 4V UP TO 28V
- SHORT CIRCUIT PROTECTION
- SAFE OPERATING AREA CURRENT LIMITING
- TEMPERATURE SHUT DOWN WITH HYSTERESIS
- HIGH INPUT IMPEDANCE
- GROUND COMPATIBLE INPUT

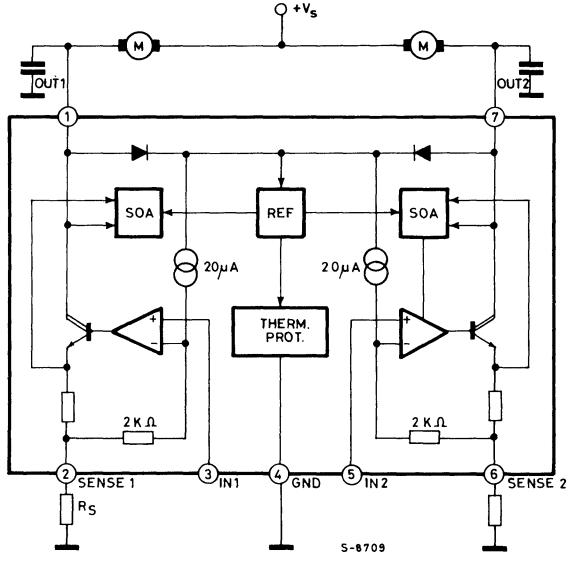
The TDA8115 is a monolithic integrated circuit which realizes two independent programmable current sources. The device is well suited for motor driving applications such as reel motors in video recorders. A wide supply voltage range permits battery operation.



Heptawatt

ORDERING NUMBER: TDA8115

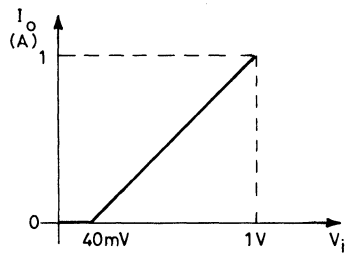
BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, unless otherwise specified)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply voltage		4		23	V
I_Q	Quiescent current			2	5	mA
I_O	Output current range				1	A
V_{IR}	Input voltage range		0		V_S -3	V
V_{OS}	Positive input offset for current starting point		50	60	80	mV
	Thermal shut down			150		°C
	Hysteresis			20		°C
I_L	Output current limit V_S = 10V V_S = 20V			 1.4 0.4		 A A
I_b	Input bias current				1	μA
V_{sat}	Saturation voltage	I_{OUT} = 0.9A		1.4	2	V
R_B	Bond resistance			60		mΩ

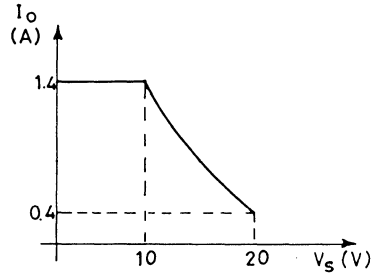
Fig. 1 - Transconductance characteristic



S-8711

with $I_O = \frac{V_{IN} - 40mV}{(R_S + 60m\Omega)}$

Fig. 2 - Max output current vs. supply voltage (SOA)



S-8712

TDA8116

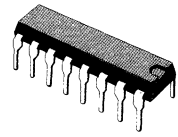
ADVANCE DATA

FOUR PHASE BRUSHLESS MOTOR DRIVER

- WIDE OPERATING VOLTAGE RANGE 6V TO 14V
- HIGH CURRENT CAPABILITY UP TO 1A
- OUTPUT DC CURRENTS UP TO 0.4A
- TWO LOGICAL INPUTS FOR THE CODED COMUNICATION SIGNAL
- LIMITED SLEW RATE OF THE OUTPUT VOLTAGE
- ANALOG INPUT WITH FIXED VOLTAGE GAIN
- INTEGRATED FLYBACK DIODES AT EACH OUTPUT
- THERMAL PROTECTION

The TDA 8116 is a monolithic integrated circuit in bipolar technology.

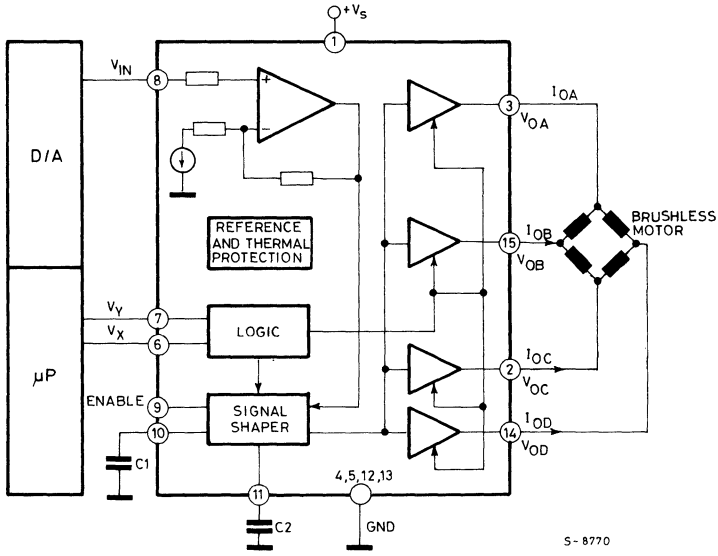
It is intended for driving a four phase brushless video head motor in microcomputer controlled servo systems.



Powerdip
12 + 2 + 2

ORDERING NUMBER: TDA 8116

BLOCK DIAGRAM



THERMAL DATA

Parameter		Min.	Typ.	Max.	Unit
T_{JSTD}	Thermal shut down threshold		150		°C
T_{JSDH}	Thermal shut down hysteresis		20		°C
$R_{th\ j\text{-}case}$	Thermal resistance junction-ground pins			14	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient			80	°C/W

ELECTRICAL CHARACTERISTICS ($6V < V_S < 14V$, $T_j = 25°C$, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{Sop}	Operating sypply voltage range		6		14	V
V_{SO}	Source stage saturation voltage	$V_{IN} = 5V$ $I_O = 1A$ $I_O = 0.4A$		1.4 1	2 1.4	V V
V_O	Sink stage saturation voltage	$V_{IN} = 5V$ $I_O = 1A$ $I_O = 0.4A$		1.4 1	2 1.4	V V
A_V	Voltage gain	$V_{IN} = 1V$ $R_L = 50\Omega$	2.5	2.75	3.0	V
V_{INth}	Input voltage threshold		0.6	0.7	0.8	V
I_N	Input current	$V_{IN} = 5V$	-5	-1	+5	μA
V_{IN}	Input voltage operating voltage range		0		V_S -1	V
$V_{X,Y\ High}$	Control input HIGH level		1.7	2.4	7	V
$I_{X,\ Y\ High}$	Control input HIGH current	$V_{IN} = 5V$			20	μA
$V_{X,\ Y\ Low}$	Control input LOW level		0.3		0.8	V
$I_{X,\ Y\ Low}$	Control input LOW current	$V_{IN} = 0.4V$	-20		20	μA
$V_{EN\ Low}$	Enable input LOW level		-0.3		1.5	V
$V_{EN\ High}$	Enable input HIGH level		2.4		7	V
$I_{EN\ Low}$	Enable input LOW current	$V_{EN} = 0V$		-20	-40	μA
$I_{EN\ High}$	Enable input HIGH current	$V_{EN} = 5V$		1		μA
$VH_{X,\ Y,\ EN}$	Control and enable inputs hysteresis			150		mV
$\frac{dV_{out}}{dt}$	Output voltage slope	$C_{1,2} = 10nF$		6		V/ms
$\lvert I_{OST} \rvert$	Starting output current	$V_{IN} = 5V$ $V_S = 12V$			1	A
I_S	Quiescent supply current	$V_{IN} = 0$		3	5	mA
I_S	Supply current	$V_{IN} = 5V$		8	15	mA

TDA8130

ADVANCE DATA

CURRENT MODE PWM CONTROLLER

- FEW EXTERNAL COMPONENTS
- FIXED FREQUENCY OPERATION
- HIGH CURRENT TOTEM POLE OUTPUT
- INTERNALLY TRIMMED BAND GAP REFERENCE
- DOUBLE PULSE SUPPRESSION
- PULSE-BY-PULSE CURRENT LIMITING
- LOW START UP CURRENT (< 1mA)
- UNDER VOLTAGE LOCKOUT
- ANTIMAGNETIZATION CIRCUIT
- EXTERNAL DUTY-CYCLE LIMITATION

Designed primarily for TV/Monitor applications, the TDA8130 control IC provides the necessary features to implement off line, fixed frequency current mode control schemes with a minimal external parts count.

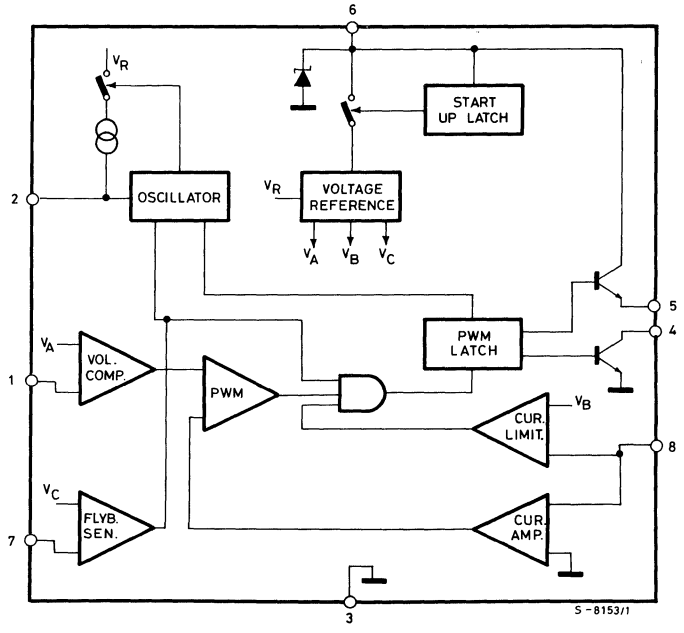
The advantages for this tecnique can be measured in improved line regulation, enhanced load regulation and a simplier control loop.

Protection circuitry includes buit-in under voltage lockout, pulse-by-pulse current limiting and an antimagnetization circuit.

Plastic Minidip

ORDERING NUMBER: TDA8130

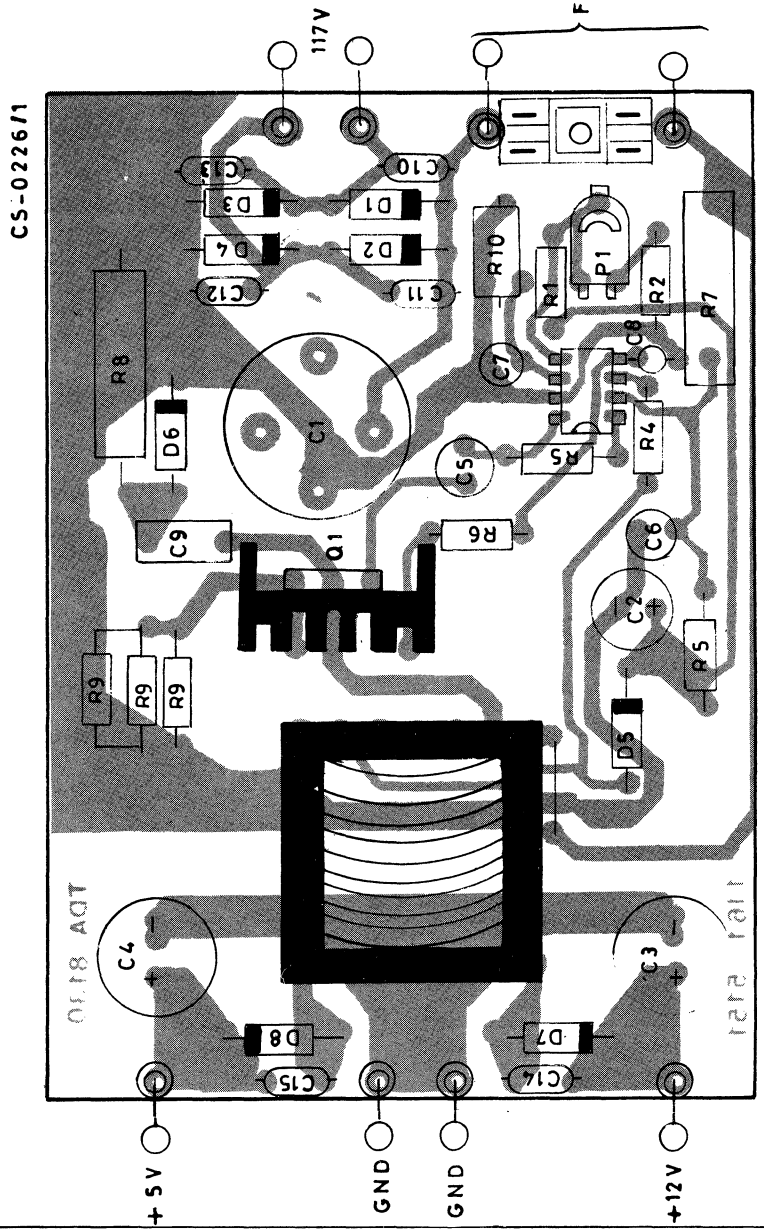
BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (V_S = 8V, T_{amb} = 25°C)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Operating supply voltage	After start-up		8		V
I_s	Supply current (without load)	V_s = 8V after start-up		20		mA
V_{st}	Start-up threshold			8.4		V
V_{so}	Switch-off threshold			5.6		V
I_{sl}	Supply current before start-up				1	mA
V_r	Internal supply voltage			3.2		V
V_a	Reference voltage			1.2		V
V_b	Current limiter threshold			0.75		V
V_c	Flyback sense threshold			0.4		V
f_o	Oscillator free running frequency	with C = 3.3nF R = 3.3KΩ		40		kHz
f_m	Maximum oscillator free running frequency		100			kHz
V_{oh}	Source saturation voltage	I_o = 100mA			0.8	V
V_{ol}	Sink saturation voltage	I_o = 0.5A			1	V

Fig. 4 - Printed circuit and component layout of the circuit of fig. 3 (1 : 1 scale)



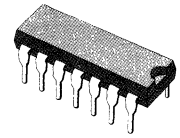
TDA8132

ADVANCE DATA

CURRENT MODE PWM CONTROLLER

- FIXED FREQUENCY OPERATION
- HIGH CURRENT TOTEM POLE OUTPUT
- INTERNALLY TRIMMED BAND GAP REFERENCE
- DOUBLE PULSE SUPPRESSION
- PULSE-BY-PULSE CURRENT LIMITING
- LOW START UP CURRENT (< 1mA)
- UNDER VOLTAGE LOCKOUT
- ANTIMAGNETIZATION CIRCUIT
- EXTERNAL DUTY CYCLE LIMITATION
- RAMP GENERATOR WITH SYNCHRONIZATION FACILITY
- ENABLE INPUT
- OVER AND UNDER VOLTAGE DETECTORS
- OVERLOAD IDENTIFICATION

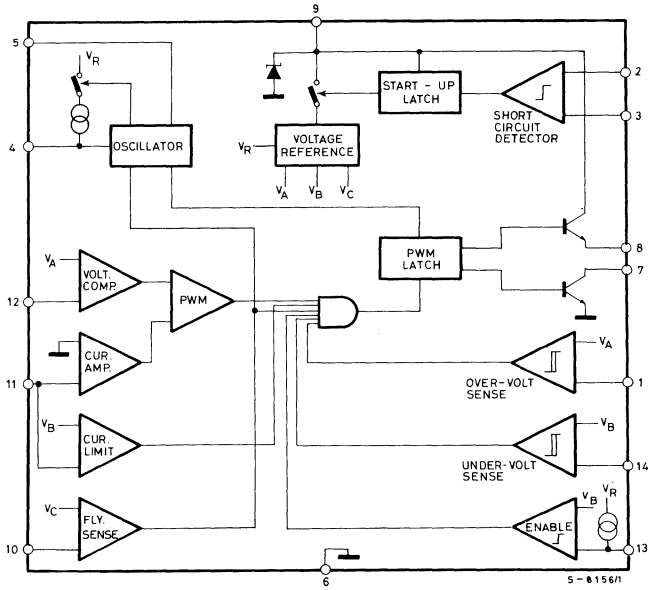
Designed primarily for TV/Monitor applications, the TDA8132 control IC provides the necessary features to implement off line, fixed frequency current mode control schemes with a minimal external parts count. The advantages of this technique can be measured in improved line regulation, enhanced load regulation and a simplier control loop. Protection circuitry includes built-in under voltage, lockout, phase-by-pulse current limiting and an antimagnetization circuit.



DIP-14 Plastic

ORDERING NUMBER: TDA8132

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (V_S = 8V, T_{amb} = 25°C)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Operating supply voltage	After start-up		8		V
I_s	Supply current (without load)	V_s = 8V after start-up		20		mA
V_{st}	Start-up threshold			8.4		V
V_{so}	Switch-off threshold			5.6		V
I_{sl}	Supply current before start-up				1	mA
V_r	Internal supply voltage			3.2		V
V_a	Reference voltage			1.2		V
V_b	Current limiter threshold			0.75		V
V_c	Flyback sense threshold			0.4		V
f_o	Oscillator free running frequency	with C = 3.3nF R = 3.3KΩ		40		kHz
f_m	Maximum oscillator free running frequency		100			kHz
V_{oh}	Source saturation voltage	I_o = 100mA			0.8	V
V_{ol}	Sink saturation voltage	I_o = 0.5A			1.5	V
I_{sync}	Synchronous input current (positive going)		100			μA
V_{ov}	Over-voltage threshold			1.2		V
V_{uv}	Under-voltage threshold			0.75		V
V_e	Enable threshold			0.5		V

Fig. 4 - Output voltages vs. 5V output current ($I_{o\,5}$)

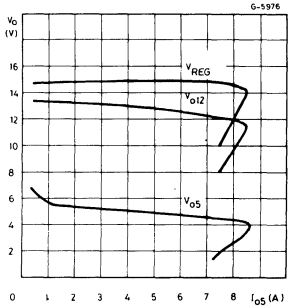
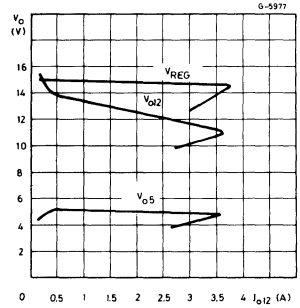


Fig. 5 - Output voltages vs. 12V output current ($I_{o\,12}$)



TL7700A Series

SUPPLY VOLTAGE SUPERVISORS

- POWER-ON RESET GENERATOR
- AUTOMATIC RESET GENERATION AFTER VOLTAGE DROP
- WIDE SUPPLY VOLTAGE RANGE . . . 3V .TO 18V
- PRECISION VOLTAGE SENSOR
- TEMPERATURE-COMPENSATED VOLTAGE REFERENCE
- TRUE AND COMPLEMENT RESET OUTPUTS
- EXTERNALLY ADJUSTABLE PULSE WIDTH

The TL7700A series are monolithic integrated circuit supply voltage supervisors specifically designed for use as reset controllers in microcomputer and microprocessor systems. During power-up the device tests the supply voltage and keeps the RESET and $\overline{\text{RESET}}$ outputs active (high and low, respectively) as long as the supply voltage has not reached its nominal voltage value. Taking $\overline{\text{RESIN}}$ low has the same effect. To ensure that the microcomputer system has reset, the TL7700A then initiates an internal time delay that delays the return of the reset outputs to their inactive states. Since the time delay for most microcomputers and microprocessors is in the order of several machine cycles, the device internal time delay is determined by an external time delay is determined by an external capacitor connected to the C_T input (pin 3).

$t_d = 1.3 \times 10^4 \times C_T$

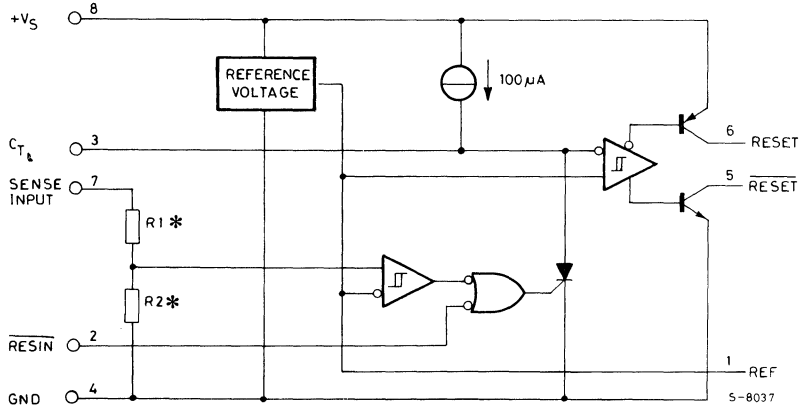
Where: C_T is in farads (F) and t_d is in seconds(s)

In addition, when the supply voltage drops below the nominal value, the outputs will be active until the supply voltage returns to the nominal value. An external capacitor (typically 0.1μF) must be connected to the REF output (pin 1) to reduce the influence of fast transients in the supply voltage.

The TL7700AI series is characterized for operation from -25°C to 85°C; the TL7700AC series is characterized from 0°C to 70°C.

Plastic Minidip SO-8

BLOCK DIAGRAM



* TL7702A R1 = 0Ω, R2 = open; TL7705A R1 = 7.8KΩ, R2 = 10KΩ; TL7709A R1 = 19.7KΩ, R2 = 10KΩ; TL7712A R1 = 32.7KΩ, R2 = 10KΩ; TL7715A R1 = 43.4KΩ, R2 = 10KΩ

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max.	120	°C/W

ELECTRICAL CHARACTERISTICS

These specifications unless otherwise specified, apply for: T_{amb} = -40 to 85°C (TL77XXAI); T_{amb} = 0 to 70°C (TL77XXAC)

Parameter			Test Conditions (1)	Min.	Typ.	Max.	Unit
V_{OH}	High-level output voltage at RESET		I_{OH} = -16mA	V_S-1.5			V
V_{OL}	Low-level output voltage at $\overline{RESET}$		I_{OL} = 16mA			0.4	V
V_{ref}	Reference voltage		T_{amb} = 25°C	2.48	2.53	2.58	V
V_T	Threshold Voltage at SENSE input	TL7702A	V_S = 3.6V to 18V T_{amb} = 25°C	2.48	2.53	2.58	V
		TL7705A		4.5	4.55	4.6	
		TL7709A		7.5	7.6	7.7	
		TL7712A		10.6	10.8	11.0	
		TL7715A		13.2	13.5	13.8	
V_T	Threshold voltage at SENSE input	TL7702A	V_S = 3.6V to 18V	2.45	2.53	2.58	V
		TL7705A		4.45	4.55	4.6	
		TL7709A		7.4	7.6	7.7	
		TL7712A		10.4	10.8	11.0	
		TL7715A		13.0	13.5	13.8	
V_{T+}, V_{T-}	Hysteresis (2) at SENSE input	TL7702A	V_S = 3.6V to 18V T_{amb} = 25°C		10		mV
		TL7705A			15		
		TL7709A			20		
		TL7712A			35		
		TL7715A			45		
I_I	Input current at $\overline{RESIN}$ input		V_i = 2.4V to V_S			20	μA
			V_i = 0.4V			-100	
I_I	Input current at SENSE input	TL7702A	$V_{ref} < V_I < V_S$ -1.5V		0.5	2	
I_{OH}	High-level output current at $\overline{RESET}$		V_O = 18V			50	
I_{OL}	Low-level output current at RESET		V_O = 0V			-50	
I_S	Supply current		All inputs and out. open		1.8	3	mA

1. All characteristics are measured with C = 0.1μF from Pin 1 to GND, and with C = 0.1μF from Pin 3 to GND
2. Hysteresis is the difference between the positive going input threshold voltage. V_{T+}, and the negative going input threshold voltage, V_{T-}.

UC1840
UC2840
UC3840

PRELIMINARY DATA

PROGRAMMABLE, OFF-LINE, PWM CONTROLLER

- ALL CONTROL, DRIVING, MONITORING, AND PROTECTION FUNCTIONS INCLUDED
- LOW-CURRENT, OFF-LINE START CIRCUIT
- FEED-FORWARD LINE REGULATION OVER 4 TO 1 INPUT RANGE
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- PULSE-BY-PULSE CURRENT LIMITING PLUS SHUTDOWN FOR OVER-CURRENT FAULT
- NO START-UP OR SHUTDOWN TRANSIENTS
- SLOW TURN-ON AND MAXIMUM DUTY-CYCLE CLAMP
- SHUTDOWN UPON OVER- OR UNDER-VOLTAGE SENSING
- LATCH OFF OR CONTINUOUS RETRY AFTER FAULT
- REMOTE, PULSE-COMMANDABLE START/STOP
- PWM OUTPUT SWITCH USABLE TO 1A PEAK CURRENT
- 1% REFERENCE ACCURACY
- 500 kHz OPERATION

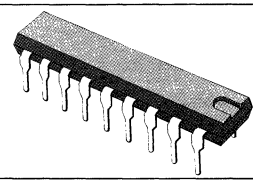
Although containing most of the features required by all types of switching power supply controllers, the UC1840 family has been optimized for highly-efficient boot-strapped primary-side operation in forward or flyback power converters. Two important features for this mode are a starting circuit which requires little current from the primary input voltage and feed-forward control for constant volt-second operation over a wide input voltage range.

In addition to startup and normal regulating PWM functions, these devices offer built-in protection from over-voltage, under-voltage, and over-current fault conditions. This monitoring circuitry contains the added features that any fault will initiate a complete shutdown with provisions for either latch off or automatic restart. In the latch-off mode. the controller may be started and stopped with external pulsed or steady-state commands.

Other performance features of these devices include a 1% accurate reference, provision for slow-turn-on and duty-cycle limiting, and high-speed pulse-by-pulse current limiting in addition to current fault shutdown.

The UC1840's PWM output stage includes a latch to insure only a single pulse per period and is designed to optimize the turn off of an external switching device by conducting during the "OFF" time with a capability for both high peak current and low saturation voltage. These devices are available in an 18-pin dual-in-line plastic or ceramic package.

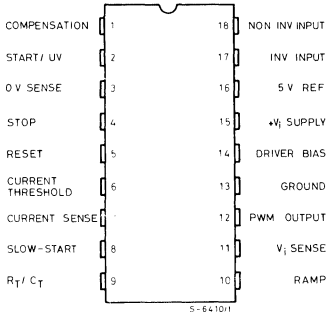
The UC1840 is characterized for operation over the full military temperature range of -55°C to +125°C. The UC2840 and UC3840 are designed for operation from -25°C to +85°C and 0°C to +70°C, respectively.



DIP-18 Plastic (U7P2) and Ceramic

CONNECTION DIAGRAM AND ORDERING NUMBERS

(top view)



Type	Plastic	Ceramic
UC1840	—	UC1840J
UC2840	UC2840N	UC2840J
UC3840	UC3840N	UC3840J

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

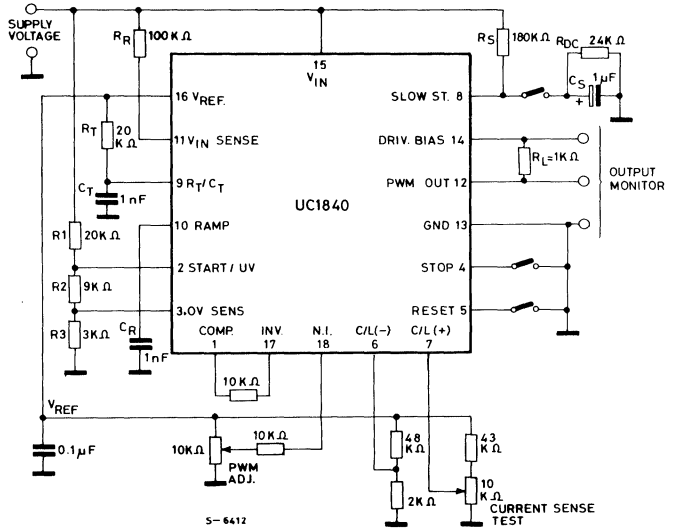
FUNCTIONAL DESCRIPTION

Name	Function
PWM CONTROL	
OSCILLATOR	Generates a fixed-frequency internal clock from an external R_T and C_T. Frequency $= \frac{K_c}{R_T C_T}$ where K_c is a first-order correction factor $\approx$ 0.3 log (C_T X 10^{12}).
RAMP GENERATOR	Develops a linear ramp with a slope defined externally by $\frac{dv}{dt} = \frac{\text{sense voltage}}{R_R\ C_R}$. C_R is normally selected $\leqslant C_T$ and its value will have some effect upon valley voltage. C_R terminal can be used as an input port for current mode control.
ERROR AMPLIFIER	Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance: unity-gain stable.
REFERENCE GENERATOR	Precision 5.0V for internal and external usage to 50 mA. Tracking 3.0V reference for internal usage only with nominal accuracy of ± 2%. 40V clamp zener for chip O.V. protection, 100mA maximum current.
PWM COMPARATOR	Generates output pulse which starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs.
PWM LATCH	Terminates the PWM output pulse when set by inputs from either the PWM comparator, the pulse-by-pulse current limit comparator, or the error latch. Resets with each internal clock pulse.
PWM OUTPUT SWITCH	Transistor capable of sinking current to ground which is off during the PWM on-time and turns on to terminate the power pulse. Current capacity is 400mA saturated with peak capacitance discharge in excess of one amp.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit. Unless otherwise stated, these specifications apply for T_j = -55 to + 125°C for the UC1840, -25°C to + 85°C for the UC2840 and 0 to 70°C for the UC3840; V_i = 20V, R_T = 20KΩ, C_T = 0.001 μF, C_R = 0.001 μF, current limit threshold = 200mV

Parameter		Test conditions	UC1840 UC2840			UC3840			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
POWER INPUTS									
I_{ST}	Start-up current	V_i = 30V, Pin 2= 2.5V, T_j = 25°C		4	5.5		4	5.5	mA
	*Start-up current T.C.	V_i = 30V, Pin 2= 2.5V		-0.1	-0.2		-0.1	-0.2	%/°C
I_i	Operating current	V_i = 30V, Pin 2= 3.5V	5	10	15	5	10	15	mA
V_{SOV}	Supply O.V. clamp	I_i = 20mA	33	40	45	33	40	48	V
REFERENCE SECTION									
V_{REF}	Reference voltage	T_j = 25°C	4.95	5	5.05	4.9	5	5.1	V
ΔV_{REF}	Line regulation	V_i = 8 to 30V		10	15		10	20	mV
ΔV_{REF}	Load regulation	I_L = 0 to 20 mA		10	20		10	30	mV
$\Delta V_{REF}/\Delta T$*	Temperat. coeff.	Over op. temp. range			± 0.4			± 0.4	mV/°C
I_{SC}	Short circuit curr.	V_{REF}= 0, T_j = 25°C		-80	-100		-80	-100	mA
OSCILLATOR									
f_s	Nominal frequency	T_j = 25°C	47	50	53	45	50	55	KHz
	Voltage stability	V_i = 8 to 30V		0.5	1		0.5	1	%
	* Temperature coeff.	Over op. temp. range			±0.8			± 0.8	%/°C
$f_{s(max)}$	Maxim. frequency	R_T= 2KΩ, C_T= 330pF	500			500			KHz
RAMP GENERATOR									
	Ramp current min.	I_{SENSE}= -10 μA		-11	-14		-11	-14	μA
	Ramp current max.	I_{SENSE}= 1 mA	-0.9	-0.95		-0.9	-0.95		mA
	Ramp valley		0.3	0.5	0.7	0.3	0.5	0.7	V
	Ramp peak	Clamping level	3.9	4.2	4.5	3.9	4.2	4.5	V
ERROR AMPLIFIER									
V_{os}	Input offset voltage	V_{CM}= 5V		0.5	5		2	10	mV
I_b	Input bias current			0.5	2		1	5	μA
I_{os}	Input offset current				0.5			0.5	μA
G_v	Open loop gain	ΔV_o= 1 to 3V	60	66		60	66		dB
	Output swing (max Out ≤ Ramp peak -100 mV)	Minimum total range	0.3		3.5	0.3		3.5	V
CMR	Common mode rejection	V_{CM}= 1.5 to 5.5V	70	80		70	80		dB
SVR	Supply voltage rejection	V_i = 8 to 30V	40	50		40	50		dB

Fig. 1 - Open loop test circuit



Nominal frequency = $\frac{1}{R_T C_T}$ = 50 kHz

Start voltage = $3\ (\frac{R1 + R2 + R3}{R2 + R3})$ + 0.2 R1 = 12V

U.V. fault voltage = $3\ (\frac{R1 + R2 + R3}{R2 + R3})$ = 8V

O.V. fault voltage = $3\ (\frac{R1 + R2 + R3}{R3})$ = 32V

Current limit = 200 mV
Current fault voltage = 600 mV
Duty cycle clamp = 50%

Fig. 2 - Start U.V. hysteresis current

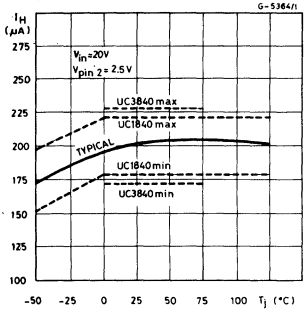


Fig. 3 - PWM Output saturation voltage

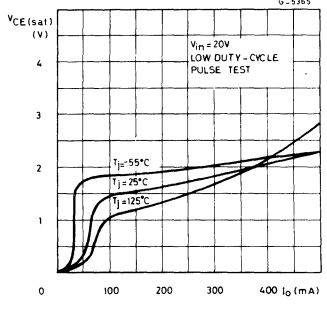
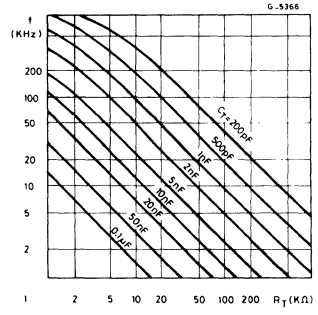


Fig. 4 - Oscillator frequency



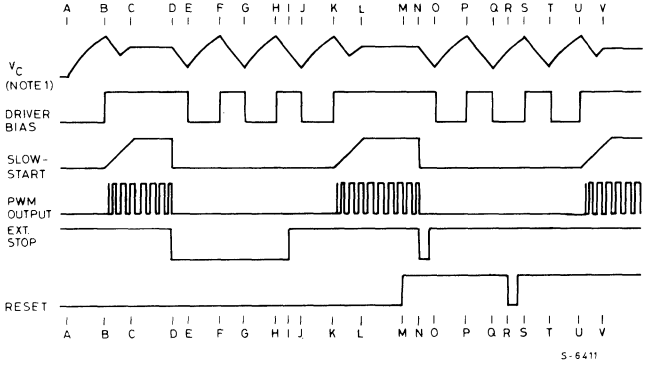
APPLICATION INFORMATION (continued)

In this application (see Fig. 8) complete control is maintained on the primary side. Control power is provided by R_{IN} and C_{IN} during start-up, and by a primary-referenced low voltage winding. N2, for efficient operation after start. The error amplifier loop is closed to regulate the DC voltage from N2 with other outputs following through their magnetic coupling – a task made even easier with the UC1840's feed-forward line regulation.

The UC1840 will readily accept digital start/stop commands transmitted from the secondary side by means of optical couplers.

Not shown are protective snubbers or additional interface circuitry which may be required by the choice of the high-voltage switch, Qs, or the application.

Fig. 9 - Power sequencing functions



Notes: 1. VC represents an analog of the output voltage generated by a primary-referenced secondary winding on the power transformer. It is the voltage monitored by the start/U.V. comparator and, in most cases, is the supply voltage, V_i, for the UC1840.

2. Although input to External Stop, Pin 4, is shown, results are the same for any fault input which sets the Error Latch.

Power Frequency Functions

Time	Event
A	Initial turn-on, V_c rises with light load
B	Start threshold. Driver Bias loads V_c
C	Operating PWM regulates V_c
D	Stop input sets Error Latch turning off PWM
E	U.V. low threshold. Error Latch remain set
F	Start turns on Driver Bias bus Error Latch still set
G, H	V_c and Driver Bias continue to cycle
I	Stop command removed
J	Error Latch reset at U.V. low threshold
K	Start threshold now removes slow-start clamp
L	Return to normal run state
M	Reset Latch set signal removed
N	Error Latch set with momentary fault
O	Error Latch does not reset as Reset Latch is reset
P, Q	V_c and Driver Bias recycle with no turn-on
R	Reset Latch set is set with momentary Reset signal
S	V_c must complete cycle to turn-on
T	Start and Error Latches reset
U	Normal start initiated
V	Return to normal run state

UC1842/3/4/5
UC2842/3/4/5
UC3842/3/4/5

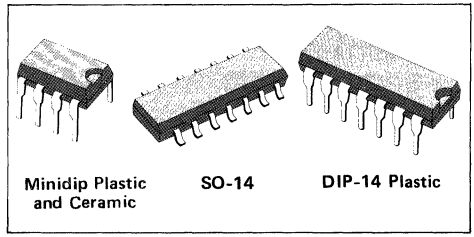
ADVANCE DATA

CURRENT MODE PWM CONTROLLER

- OPTIMIZED FOR OFF-LINE AND DC TO DC CONVERTERS
- LOW START-UP CURRENT (< 1mA)
- AUTOMATIC FEED FORWARD COMPENSATION
- PULSE-BY-PULSE CURRENT LIMITING
- ENHANCED LOAD RESPONSE CHARACTERISTICS
- UNDER-VOLTAGE LOCKOUT WITH HYSTERESIS
- DOUBLE PULSE SUPPRESSION
- HIGH CURRENT TOTEM POLE OUTPUT
- INTERNALLY TRIMMED BANDGAP REFERENCE
- 500KHz OPERATION
- LOW R_O ERROR AMP

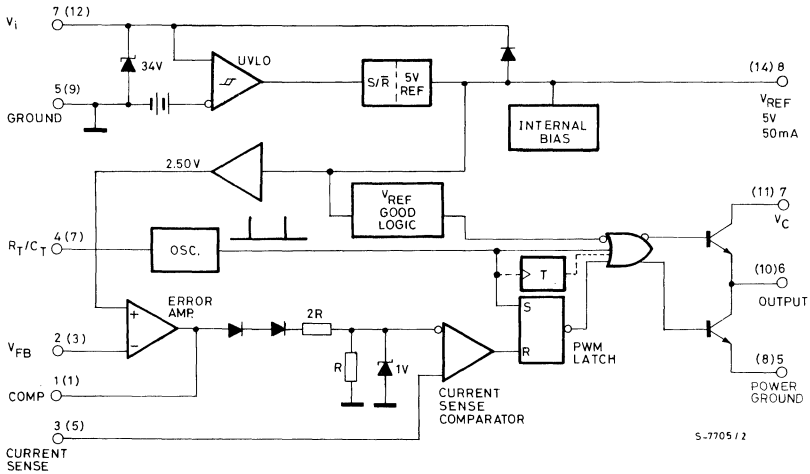
The UC1842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under voltage lockout featuring start-up current less than 1mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off-state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of 16V (on) and 10V (off), ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.5V and 7.9V. The UC1842 and UC1843 can operate to duty cycles approaching 100%. A range of zero to < 50% is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.



Minidip Plastic and Ceramic — SO-14 — DIP-14 Plastic

BLOCK DIAGRAM (Toggle flip flop used only in UC1844 and UC1845)



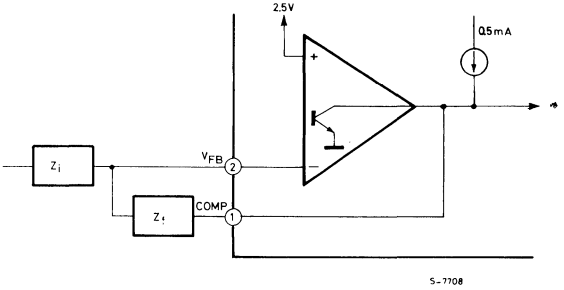
THERMAL DATA

		Ceramic Minidip	Plastic Minidip	DIP-14 Plastic	SO-14
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	200°C/W	100°C/W	100°C/W	165°C/W

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $-55 \leq T_{amb} \leq 125°C$ for UC184X; $-25 \leq T_{amb} \leq 85°C$ for UC284X; $0 \leq T_{amb} \leq 70°C$ for UC384X; $V_i = 15V$ (Note 5); $R_T = 10K$; $C_T = 3.3nF$)

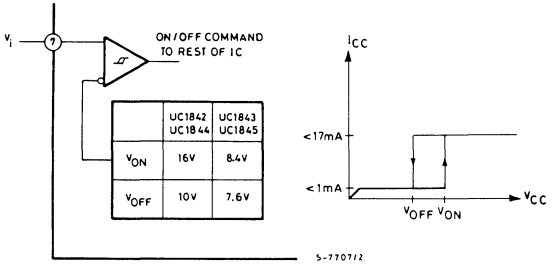
Parameter		Test Conditions	UC184X UC284X			UC384X			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
REFERENCE SECTION									
V_{REF}	Output voltage	$T_j = 25°C$ $I_o = 1mA$	4.95	5.00	5.05	4.90	5.00	5.10	V
ΔV_{REF}	Line regulation	$12V \leq V_i \leq 25V$		6	20		6	20	mV
ΔV_{REF}	Load regulation	$1 \leq I_o \leq 20mA$		6	25		6	25	mV
$\Delta V_{REF}/\Delta T$	Temperature stability	(Note 2)		0.2	0.4		0.2	0.4	mV/°C
	Total output variation	Line, Load, Temperature (Note 2)	4.9		5.1	4.82		5.18	V
e_N	Output noise voltage	$10Hz \leq f \leq 10KHz$ $T_j = 25°C$ (Note 2)		50			50		μV
	Long term stability	$T_{amb} = 125°C$, 1000 Hrs (Note 2)		5	25		5	25	mV
I_{sc}	Output short circuit		-30	-100	-180	-30	-100	-180	mA
OSCILLATOR SECTION									
f_s	Initial accuracy	$T_j = 25°C$ (Note 6)	47	52	57	47	52	57	KHz
	Voltage stability	$12 \leq V_i \leq 25V$		0.2	1		0.2	1	%
	Temperature stability	$T_{MIN} \leq T_{amb} \leq T_{MAX}$ (Note 2)		5			5		%
V_4	Amplitude	$V_{PIN\ 4}$ peak to peak		1.7			1.7		V
ERROR AMP SECTION									
V_2	Input voltage	$V_{PIN\ 1} = 2.5V$	2.45	2.50	2.55	2.42	2.50	2.58	V
I_b	Input bias current			-0.3	-1		-0.3	-2	μA
	A_{VOL}	$2 \leq V_o \leq 4V$	65	90		65	90		dB
B	Unity gain bandwidth	(Note 2)	0.7	1		0.7	1		MHz
SVR	Supply voltage rejection	$12 \leq V_i \leq 25V$	60	70		60	70		dB
I_o	Output sink current	$V_{PIN\ 2} = 2.7V$ $V_{PIN\ 1} = 1.1V$	2	6		2	6		mA
I_o	Output source current	$V_{PIN\ 2} = 2.3V$ $V_{PIN\ 1} = 5V$	-0.5	-0.8		-0.5	-0.8		mA
	V_{OUT} High	$V_{PIN\ 2} = 2.3V$; $R_L = 15K\Omega$ to ground	5	6		5	6		V
	V_{OUT} Low	$V_{PIN\ 2} = 2.7V$, $R_L = 15K\Omega$ to Pin 8		0.7	1.1		0.7	1.1	V

Fig. 1 - Error amp configuration



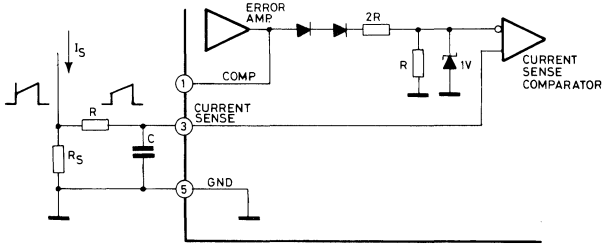
Error amp can source or sink up to 0.5mA

Fig. 2 - Under voltage lockout



During Under-Voltage Lockout, the output driver is biased to sink minor amounts of current. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with extraneous leakage currents.

Fig. 3 - Current sense circuit

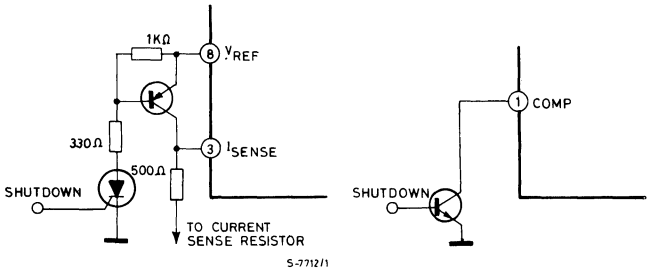


PEAK CURRENT (I_S) IS DETERMINED BY THE FORMULA

$$I_{S\,max} \approx \frac{1.0V}{R_S}$$

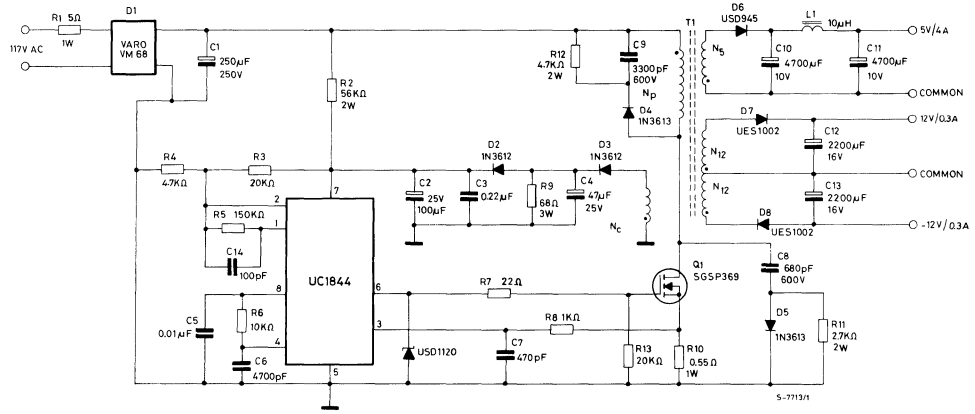
A SMALL RC FILTER MAY BE REQUIRED TO SUPPRESS SWITCH TRANSIENTS.

Fig. 10 - Shutdown techniques



Shutdown of the UC1842 can be accomplished by two methods; either raise pin 3 above 1V or pull pin 1 below a voltage two diode drops above ground. Either method cause the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pins 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling V_i below the lower UVLO threshold. At this point the reference turns off, allowing the SCR to reset.

Fig. 11 - Off-line flyback regulator



Power Supply Specifications

1. Input Voltage: 95VAC to 130VAC (50Hz/60Hz)
2. Line Isolation: 3750V
3. Switching Frequency: 40KHz
4. Efficiency @ Full Load: 70%
5. Output Voltage:
   A. +5V, ±5%: 1A to 4A load
      Ripple voltage: 50mV P-P Max.
   B. +12V, ±3%: 0.1A to 0.3A load
      Ripple voltage: 100mV P-P Max.
   C. -12V, ±3%: 0.1A to 0.3A load
      Ripple voltage: 100mV P-P Max.

SEVEN DARLINGTON ARRAYS

- SEVEN DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 500mA PER DRIVER (600mA PEAK)
- OUTPUT VOLTAGE 50V
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL/CMOS/PMOS/DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT

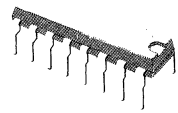
The ULN2001A, ULN2002A, ULN2003A and ULN2004A are high voltage, high current darlington arrays each containing seven open collector darlington pairs with common emitters. Each channel is rated at 500mA and can withstand peak currents of 600mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

The four versions interface to all common logic families:

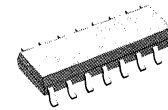
ULN2001A	General purpose, DTL, TTL, PMOS, CMOS
ULN2002A	14-25V PMOS
ULN2003A	5V TTL, CMOS
ULN2004A	6-15V CMOS, PMOS

These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors, LED displays filament lamps, thermal printheads and high power buffers.

The ULN2001A/2002A/2003A and 2004A are supplied in 16 pin plastic DIP packages with a copper leadframe to reduce thermal resistance. They are available also in small outline package (SO-16) as ULN2001D/2002D/2003D/2004D.



DIP-16 Plastic (0.25)



SO-16

ORDERING NUMBER:
ULN2001A/2A/3A/4A (DIP-16)
ULN2001D/2D/3D/4D (SO-16)

ABSOLUTE MAXIMUM RATINGS

V_o	Output voltage	50	V
V_{in}	Input voltage (for ULN2002A/D - 2003A/D - 2004A/D)	30	V
I_c	Continuous collector current	500	mA
I_b	Continuous base current	25	mA
T_{amb}	Operating ambient temperature range	-20 to 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Junction temperature	150	°C

THERMAL DATA

			DIP-16	SO-16
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70°C/W	165°C/W

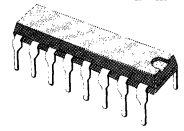
ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output leakage current	V_{CE} = 50V			50	μA	1a
		T_{amb} = 70°C V_{CE} = 50V			100	μA	1a
		T_{amb} = 70°C for **ULN2002A** V_{CE} = 50V V_i = 6V			500	μA	1b
		for **ULN2004A** V_{CE} = 50V V_i = 1V			500	μA	1b
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 100mA I_B = 250 μA		0.9	1.1	V	2
		I_C = 200mA I_B = 350 μA		1.1	1.3	V	2
		I_C = 350mA I_B = 500 μA		1.3	1.6	V	2
$I_{i(on)}$	Input current	for **ULN2002A** V_i = 17V		0.82	1.25	mA	3
		for **ULN2003A** V_i = 3.85V		0.93	1.35	mA	3
		for **ULN2004A** V_i = 5V		0.35	0.5	mA	3
		V_i = 12V		1	1.45	mA	3
$I_{i(off)}$	Input current	T_{amb} = 70°C I_C = 500 μA	50	65		μA	4
$V_{i(on)}$	Input voltage	for **ULN2002A** V_{CE} = 2V I_C = 300 mA			13	V	5
		for **ULN2003A** V_{CE} = 2V I_C = 200 mA			2.4	V	5
		V_{CE} = 2V I_C = 250 mA			2.7	V	5
		V_{CE} = 2V I_C = 300 mA			3	V	5
		for **ULN2004A** V_{CE} = 2V I_C = 125 mA			5	V	5
		V_{CE} = 2V I_C = 200 mA			6	V	5
		V_{CE} = 2V I_C = 275 mA			7	V	5
		V_{CE} = 2V I_C = 350 mA			8	V	5
h_{FE}	DC forward current gain	for **ULN2001A** V_{CE} = 2V I_C = 350 mA	1000			–	2
C_i	Input capacitance			15	25	pF	–
t_{PLH}	Turn-on delay time	0.5 V_i to 0.5 V_o		0.25	1	μs	–
t_{PHL}	Turn-off delay time	0.5 V_i to 0.5 V_o		0.25	1	μs	–
I_R	Clamp diode leakage current	V_R = 50V			50	μA	6
		T_{amb} = 70°C V_R = 50V			100	μA	6
V_F	Clamp diode forward voltage	I_F = 350 mA		1.7	2	V	7

50V - 1.5A QUAD DARLINGTON SWITCHES

- OUTPUT CURRENT TO 1.5A EACH DARLINGTON
- MINIMUM BREAKDOWN 50V
- SUSTAINING VOLTAGE AT LEAST 35V
- INTEGRAL SUPPRESSION DIODES (ULN2064B, ULN2066B, ULN2068B AND ULN2070B)
- ISOLATED DARLINGTON PINOUT (ULN2074B, ULN2076B)
- VERSIONS COMPATIBLE WITH ALL POPULAR LOGIC FAMILIES

Designed to interface logic to a wide variety of high current, high voltage loads, these devices each contain four NPN darlington switches delivering up to 1.5A with a specified minimum breakdown of 50V and a sustaining voltage of 35V measured at 100mA. The ULN2064B, ULN2066B, ULN2068B and ULN2070B contain integral suppression diodes for inductive loads have common emitters. The ULN2074B and ULN2076B feature isolated darlington pinouts and are intended for applications such as emitter follower configurations. Inputs of the ULN2064B, ULN2068B and ULN2074B are compatible with popular 5V logic families and the ULN2066B and ULN2076B are compatible with 6-15V CMOS and PMOS. Types ULN2068B and ULN2070B include a predriver stage to reduce loading on the control logic.

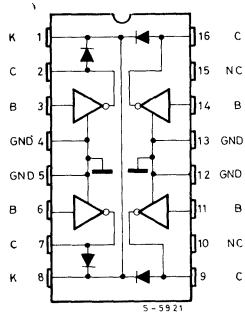


Powerdip
12 + 2 + 2

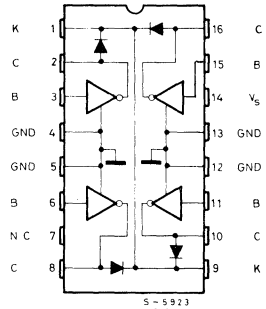
ABSOLUTE MAXIMUM RATINGS

V_{CEX}	Output voltage	50	V
$V_{CE\ (sus)}$	Output sustaining voltage	35	V
I_o	Output current	1.75	A
V_i	Input voltage for ULN2066B/70B/74B/76B	30	V
	for ULN2064B/68B	15	V
I_i	Input current	25	mA
V_s	Supply voltage for ULN2068B	10	V
	for ULN2070B	20	V
P_{tot}	Power dissipation: at T_{amb} = 90°C	4.3	W
	at T_{amb} = 70°C	1	W
T_{amb}	Operating ambient temperature range	-20 to 85	°C
T_{stg}	Storage temperature	-55 to 150	°C

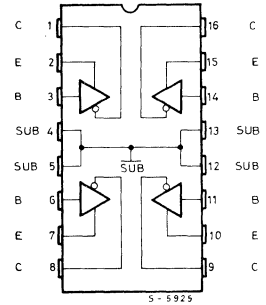
CONNECTION DIAGRAM (Top view) and ORDERING NUMBERS



ULN2064B
ULN2066B

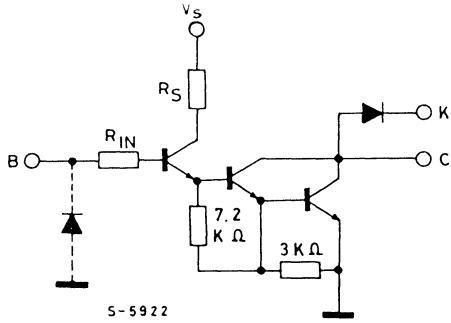


ULN2068B
ULN2070B



ULN2074B
ULN2076B

SCHEMATIC DIAGRAM



ULN2068B : R_{IN} = 2.5 kΩ R_s = 900Ω
ULN2070B : R_{IN} = 11.6 kΩ R_s = 3.4 KHΩ

ELECTRICAL CHARACTERISTICS (V_s = 5V for ULN2068B, V_s = 12V for ULN2070B, T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.	Fig.
I_{CEX}	Output leakage current	for **ULN2068B-ULN2070B** V_{CE} = 50V V_{CE} = 50V T_{amb} = 70°C			 100 500	 µA µA	1
$V_{CE(sus)}$	Collector-emitter sustaining voltage	for **ULN2068B-ULN2070B** I_C = 100mA V_i = 0.4V	35			V	2
$V_{CE(sat)}$	Collector-emitter saturation voltage	for **ULN2068B** I_C = 500 mA V_i = 2.75V I_C = 750mA V_i = 2.75V I_C = 1A V_i = 2.75V I_C = 1.25A V_i = 2.75V for **ULN2070B** I_C = 500mA V_i = 5V I_C = 750mA V_i = 5V I_C = 1A V_i = 5V I_C = 1.25A V_i = 5V			 1.1 1.2 1.3 1.4 1.1 1.2 1.3 1.4	 V V V V V V V V	2
$I_{i(on)}$	Input current	for **ULN2068B** V_i = 2.75V for **ULN2068B** V_i = 3.75V for **ULN2070B** V_i = 5V for **ULN2070B** V_i = 12V			550 1000 400 1250	µA µA µA µA	4
$V_{i(on)}$	Input voltage	V_{CE} = 2V I_C = 1.5A for **ULN2068B** for **ULN2070B**			 2.75 5	 V V	5
I_s	Supply current	for **ULN2068B** I_C = 500mA V_i = 2.75V for **ULN2070B** I_C = 500mA V_i = 5V			 6 4.5	 mA mA	8
t_{PLH}	Turn-on delay time	0.5V_i to 0.5V_o			1	µs	
t_{PHL}	Turn-off delay time	0.5V_i to 0.5V_o I_C = 1.25A			1.5	µs	
I_R	Clamp diode leakage current	for **ULN2068B-ULN2070B** V_R = 50V V_R = 50V T_{amb} = 70°C			 50 100	 µA µA	6
V_F	Clamp diode forward voltage	I_F = 1A I_F = 1.5A			1.75 2	V V	7

TEST CIRCUITS

Fig. 1

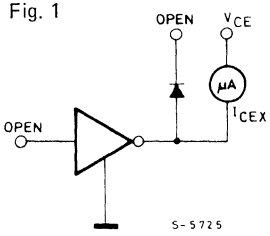


Fig. 2

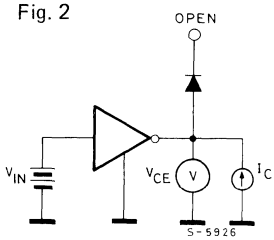


Fig. 3

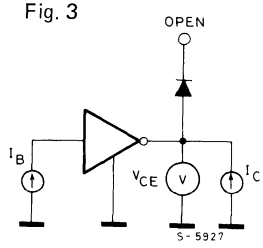


Fig. 4

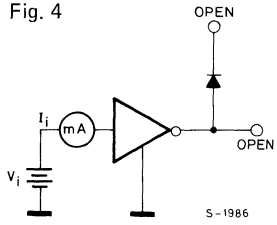


Fig. 5

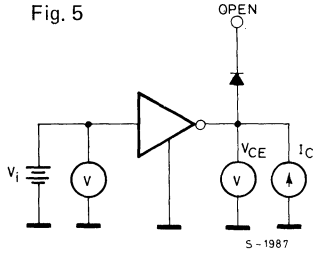


Fig. 6

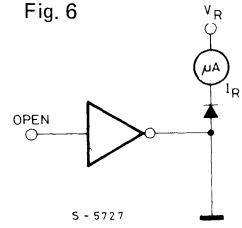


Fig. 7

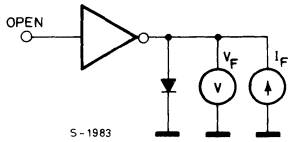
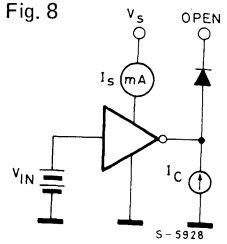


Fig. 8



MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 14) or to an external heatsink (Fig. 15).
The diagram of figure 16 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having a thickness of 35μ (1.4 mils).
During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 14 - Example of P.C. board copper area which is used as heatsink.

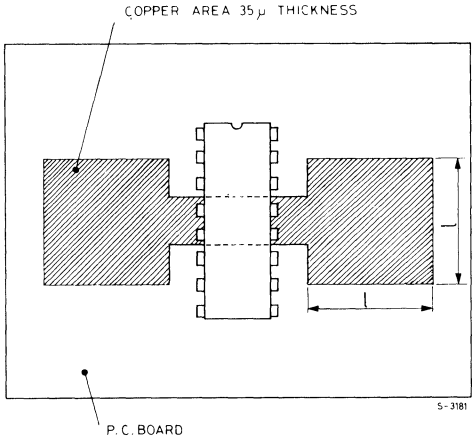


Fig. 15 - External heatsink mouting example

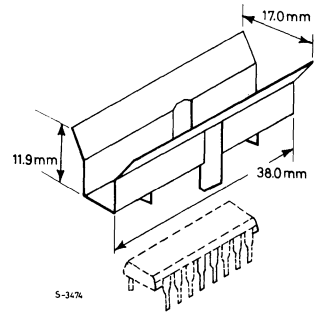


Fig. 16 - Maximum dissipable power and junction to ambient thermal resistance vs. side "ℓ"

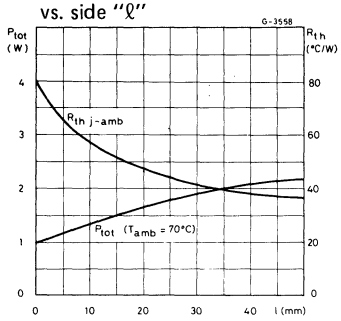
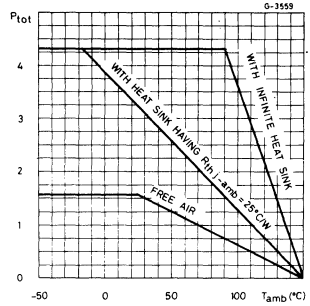


Fig. 17 - Maximum allowable power dissipation vs. ambient temperature



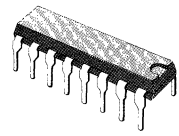
ULN2065B ULN2071B
ULN2067B ULN2075B
ULN2069B ULN2077B

PRELIMINARY DATA

80V - 1.5A QUAD DARLINGTON SWITCHES

- OUTPUT CURRENT TO 1.5A EACH DARLINGTON
- MINIMUM BREAKDOWN 80V
- SUSTAINING VOLTAGE AT LEAST 50V
- INTEGRAL SUPPRESSION DIODES (ULN2065B, ULN2067B, ULN2069B AND ULN2071B)
- ISOLATED DARLINGTON PINOUT (ULN2075B AND ULN2077B)
- VERSIONS COMPATIBLE WITH ALL POPULAR LOGIC FAMILIES

Designed to interface logic to a wide variety of high current, high voltage loads, these devices each contain four NPN darlington switches delivering up to 1.5A with a specified minimum breakdown of 80V and a sustaining voltage of 50V. The ULN2065B, ULN2067B, ULN2069B and ULN2071B contain integral suppression diodes for inductive loads and have common emitters; the ULN2075B and ULN2077B feature isolated darlington pinouts and are intended for applications such as emitter follower configurations. Inputs of the ULN2065B, ULN2069B and ULN2075B are compatible with popular 5V logic families and the ULN2067B, ULN2071B and ULN2077B are compatible with 6-15 CMOS and PMOS. The ULN2069B and ULN2071B include a predriver stage to provide extragain, reducing the load on control logic.

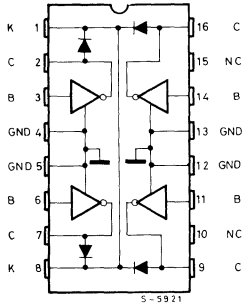


Powerdip
12 + 2 + 2

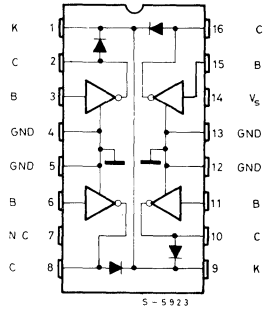
ABSOLUTE MAXIMUM RATINGS

V_{CEX}	Output voltage	80	V
$V_{CE\ (sus)}$	Output sustaining voltage	50	V
I_o	Output current	1.75	A
V_i	Input voltage for ULN2075B - 2077B	60	V
	for ULN2067B - 2071B	30	V
	for ULN2065B - 2069B	15	V
I_j	Input current	25	mA
V_s	Supply voltage for ULN2069B	10	V
	for ULN2071B	20	V
P_{tot}	Power dissipation: at $T_{pins} = 90°C$	4.3	W
	at $T_{amb} = 70°C$	1	W
T_{amb}	Operating ambient temperature range	-20 to 85	°C
T_{stg}	Storage temperature	-55 to 150	°C

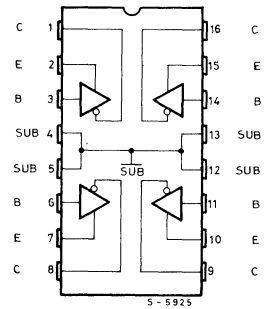
CONNECTIONS DIAGRAMS (Top view) and ORDERING NUMBERS



ULN2065B
ULN2067B

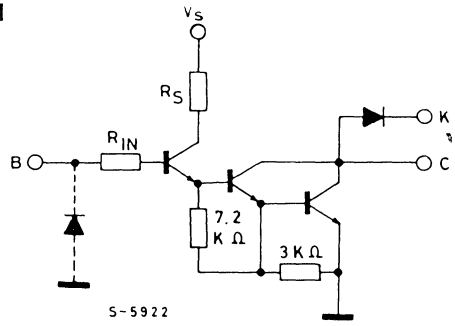


ULN2069B
ULN2071B



ULN2075B
ULN2077B

SCHEMATIC DIAGRAM



ULN2069B : R_{IN} = 2.5 kΩ, R_s = 900Ω
ULN2071B : R_{IN} = 11.6 kΩ, R_s = 3.4 kΩ

ELECTRICAL CHARACTERISTICS (V_s = 5V for ULN2069B, V_s = 12V for ULN2071B, T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.	Fig.
I_{CEX}	Output leakage current	for **ULN2069B-ULN2071B** V_{CE} = 80V V_{CE} = 80V T_{amb} = 70°C			 100 500	 μA μA	1
$V_{CE(sus)}$	Collector-emitter sustaining voltage	for **ULN2069B-ULN2071B** I_C = 100mA V_i = 0.4V	50			V	2
$V_{CE(sat)}$	Collector-emitter saturation voltage	for **ULN2069B** I_C = 500 mA V_i = 2.75V I_C = 750mA V_i = 2.75V I_C = 1A V_i = 2.75V I_C = 1.25A V_i = 2.75V I_C = 1.5A V_i = 2.75V for **ULN2071B** I_C = 500mA V_i = 5V I_C = 750mA V_i = 5V I_C = 1A V_i = 5V I_C = 1.25A V_i = 5V I_C = 1.5A V_i = 5V			 1.1 1.2 1.3 1.4 1.5 1.1 1.2 1.3 1.4 1.5	 V V V V V V V V V V	2
$I_{i(on)}$	Input current	for **ULN2069B** V_i = 2.75V for **ULN2069B** V_i = 3.75V for **ULN2071B** V_i = 5V for **ULN2071B** V_i = 12V			550 1000 400 1250	μA μA μA μA	4
$V_{i(on)}$	Input voltage	V_{CE} = 2V I_C = 1.5A for **ULN2069B** for **ULN2071B**			 2.75 5	 V	5
I_s	Supply current	for **ULN2069B** I_C = 500mA V_i = 2.75V for **ULN2071B** I_C = 500mA V_i = 5V			 6 4.5	 mA mA	8
t_{PLH}	Turn-on delay time	0.5V_i to 0.5V_o			1	μs	
t_{PHL}	Turn-off delay time	0.5V_i to 0.5V_o I_C = 1.25A			1.5	μs	
I_R	Clamp diode leakage current	for **ULN2069B-ULN2071B** V_R = 80V V_R = 80V T_{amb} = 70°C			 50 100	 μA μA	6
V_F	Clamp diode forward voltage	I_F = 1A I_F = 1.5A			1.75 2	V V	7

TEST CIRCUITS

Fig. 1

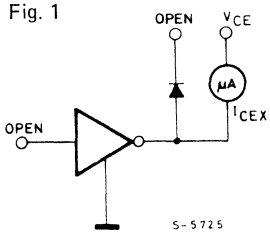


Fig. 2

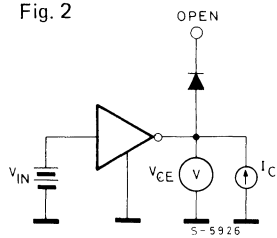


Fig. 3

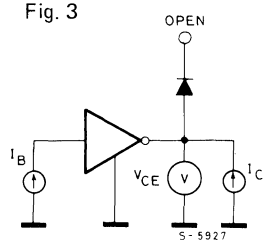


Fig. 4

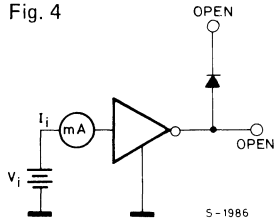


Fig. 5

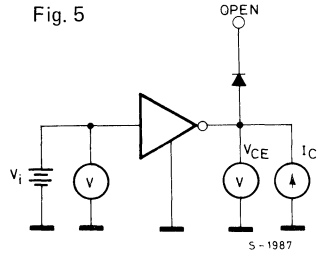


Fig. 6

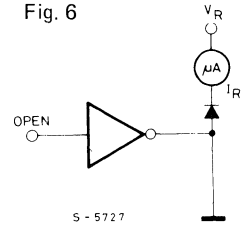


Fig. 7

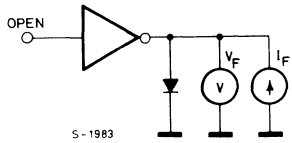


Fig. 8

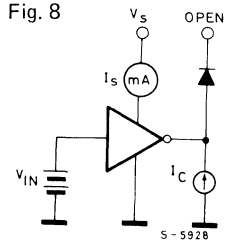


Fig. 9 - Input current as a function of input voltage

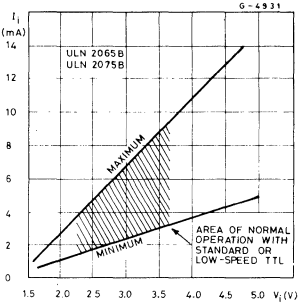


Fig. 10 - Input current as a function of input voltage

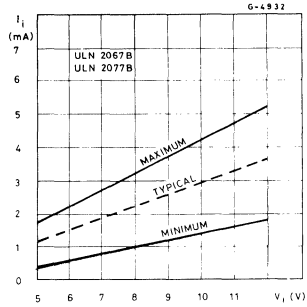
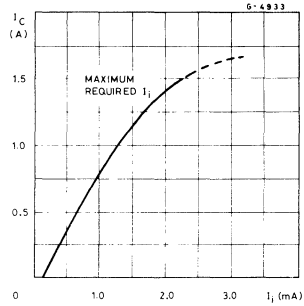


Fig. 11 - Collector current as a function of input current



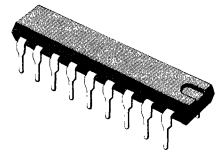
EIGHT DARLINGTON ARRAYS

- EIGHT DARLINGTONS WITH COMMON EMITTERS
- OUTPUT CURRENT TO 500mA
- OUTPUT VOLTAGE TO 50V
- INTEGRAL SUPPRESSION DIODES
- VERSIONS FOR ALL POPULAR LOGIC FAMILIES
- OUTPUT CAN BE PARALLELED
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY BOARD LAYOUT

The ULN2801A -ULN2805A each contain eight darlington transistors with common emitters and integral suppression diodes for inductive loads. Each darlington features a peak load current rating of 600mA (500mA continuous) and can withstand at least 50V in the off state. Outputs may be paralleled for higher current capability.

Five versions are available to simplify interfacing to standard logic families: the ULN2801A is designed for general purpose applications with a current limit resistor; the ULN2802A has a 10.5KΩ input resistor and zener for 14-25V PMOS; the ULN2803A has a 2.7KΩ input resistor for 5V TTL and CMOS; the ULN2804A has a 10.5KΩ input resistor for 6-15V CMOS and the ULN2805A is designed to sink a minimum of 350mA for standard and Schottky TTL where higher output current is required.

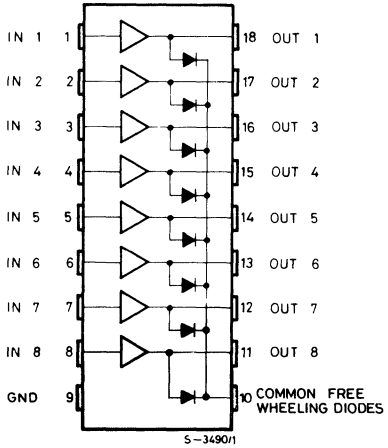
All types are supplied in a 18-lead plastic DIP with a copper lead from and feature the convenient input-opposite-output pinout to simplify board layout,



DIP-18 Plastic
(U7P2)

CONNECTION DIAGRAM

(top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	55	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C unless otherwise specified)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output leakage current	V_{CE}= 50V			50	μA	1a
		T_{amb}= 70°C V_{CE}= 50V			100	μA	1a
		T_{amb}= 70°C for **ULN 2802A** V_{CE}= 50V V_i = 6V			500	μA	1b
		for **ULN 2804A** V_{CE}= 50V V_i = 1V			500	μA	1b
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 100 mA I_B = 250 μA		0.9	1.1	V	
		I_C = 200 mA I_B = 350 μA		1.1	1.3	V	2
		I_C = 350 mA I_B = 500 μA		1.3	1.6	V	
$I_{i(on)}$	Input current	for **ULN 2802A** V_i = 17V		0.82	1.25	mA	
		for **ULN 2803A** V_i = 3.85V		0.93	1.35	mA	
		for **ULN 2804A** V_i = 5V		0.35	0.5	mA	3
		V_i = 12V		1	1.45	mA	
		for **ULN 2805A** V_i = 3V		1.5	2.4	mA	
$I_{i(off)}$	Input current	T_{amb}= 70°C I_C = 500 μA	50	65		μA	4
$V_{i(on)}$	Input voltage	for **ULN 2802A** V_{CE}= 2V I_C = 300 mA			13	V	
		for **ULN 2803A** V_{CE}= 2V I_C = 200 mA			2.4	V	
		V_{CE}= 2V I_C = 250 mA			2.7	V	
		V_{CE}= 2V I_C = 300 mA			3	V	
		for **ULN 2804A** V_{CE}= 2V I_C = 125 mA			5	V	5
		V_{CE}= 2V I_C = 200 mA			6	V	
		V_{CE}= 2V I_C = 275 mA			7	V	
		V_{CE}= 2V I_C = 350 mA			8	V	
		for **ULN 2805A** V_{CE}= 2V I_C = 350 mA			2.4	V	
h_{FE}	DC forward current gain	for **ULN 2801A** V_{CE}= 2V I_C = 350 mA	1000			–	2
C_i	Input capacitance			15	25	pF	–
t_{PLH}	Turn-on delay time	0.5 V_i to 0.5 V_o		0.25	1	μs	–
t_{PHL}	Turn-off delay time	0.5 V_i to 0.5 V_o		0.25	1	μs	–
I_R	Clamp diode leakage current	V_R = 50V			50	μA	6
		T_{amb}= 70°C V_R = 50V			100	μA	
V_F	Clamp diode forward voltage	I_F = 350 mA		1.7	2	V	7

Fig. 8 - Collector current as a function of saturation voltage

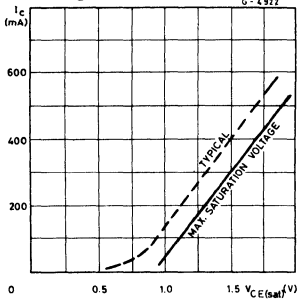


Fig. 9 - Collector current as a function of input current

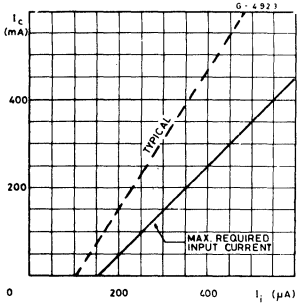


Fig. 10 - Allowable average power dissipation as a function of ambient temperature

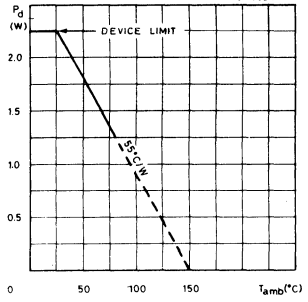


Fig. 11 - Peak collector current as a function of duty cycle

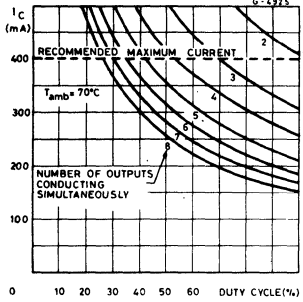


Fig. 12 - Peak collector current as a function of duty cycle

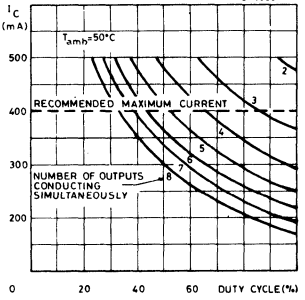


Fig. 13 - Input current as a function of input voltage (for ULN 2802A)

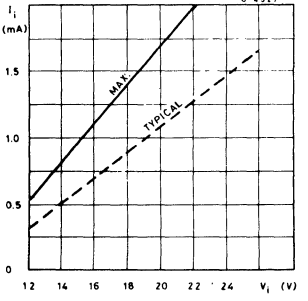


Fig. 14 - Input current as a function of input voltage (for ULN 2804A)

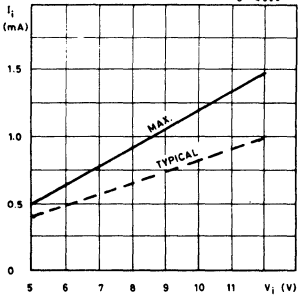


Fig. 15 - Input current as a function of input voltage (for ULN 2803A)

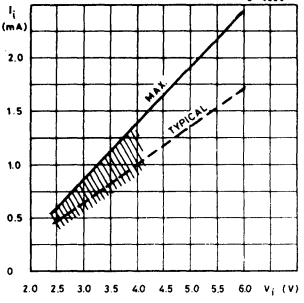
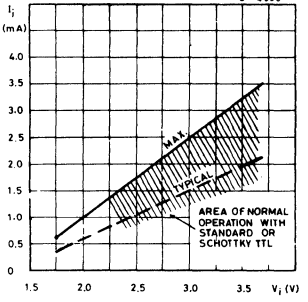


Fig. 16 - Input current as a function of input voltage (for ULN 2805A)



SEVEN DARLINGTON ARRAYS

- SEVEN DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 500mA PER DRIVER (600mA PEAK)
- OUTPUT VOLTAGE 50V
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL/CMOS/PMOS/DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT

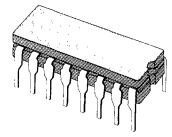
The ULQ2001R, ULQ2002R, ULQ2003R and ULQ2004R are high voltage, high current darlington arrays each containing seven open collector darlington pairs with common emitters. Each channel is rated at 500mA and can withstand peak currents of 600mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

The four versions interface to all common logic families.

ULQ2001R	General purpose, DTL, TTL, CMOS
ULQ2002R	14-25V PMOS
ULQ2003R	5V TTL, CMOS
ULQ2004R	6-15V CMOS, PMOS

These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors, LED displays, filament lamps, thermal printheads and high power buffers.

The ULQ2001R, ULQ2002R, ULQ2003R and ULQ2004R are supplied in 16 pin ceramic DIP packages.



DIP-16 Ceramic

ABSOLUTE MAXIMUM RATINGS

V_o	Output voltage	50	V
V_{in}	Input voltage (for ULQ2002R/2003R/2004R)	30	V
I_c	Continuous collector current	500	mA
I_b	Continuous base current	25	mA
T_{amb}	Operating ambient temperature range	-20 to + 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	150	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output leakage current	V_{CE} = 50V			50	μA	1a
		T_{amb} = 70°C V_{CE} = 50V			100	μA	1a
		T_{amb} = 70°C for **ULQ2002R** V_{CE} = 50V V_i = 6V			500	μA	1b
		for **ULQ2004R** V_{CE} = 50V V_i = 1V			500	μA	1b
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 100mA I_B = 250 μA		0.9	1.1	V	2
		I_C = 200mA I_B = 350 μA		1.1	1.3	V	2
		I_C = 350mA I_B = 500 μA		1.3	1.6	V	2
$I_{i(on)}$	Input current	for **ULQ2002R** V_i = 17V		0.82	1.25	mA	3
		for **ULQ2003R** V_i = 3.85V		0.93	1.35	mA	3
		for **ULQ2004R** V_i = 5V		0.35	0.5	mA	3
		V_i = 12V		1	1.45	mA	3
$I_{i(off)}$	Input current	T_{amb} = 70°C I_C = 500 μA	50	65		μA	4
$V_{i(on)}$	Input voltage	for **ULQ2002R** V_{CE} = 2V I_C = 300 mA			13	V	5
		for **ULQ2003R** V_{CE} = 2V I_C = 200 mA			2.4	V	5
		V_{CE} = 2V I_C = 250 mA			2.7	V	5
		V_{CE} = 2V I_C = 300 mA			3	V	5
		for **ULQ2004R** V_{CE} = 2V I_C = 125 mA			5	V	5
		V_{CE} = 2V I_C = 200 mA			6	V	5
		V_{CE} = 2V I_C = 275 mA			7	V	5
		V_{CE} = 2V I_C = 350 mA			8	V	5
h_{FE}	DC forward current gain	for **ULQ2001R** V_{CE} = 2V I_C = 350 mA	1000			–	2
C_i	Input capacitance			15	25	pF	–
t_{PLH}	Turn-on delay time	0.5 V_i to 0.5 V_o		0.25	1	μs	–
t_{PHL}	Turn-off delay time	0.5 V_i to 0.5 V_o		0.25	1	μs	–
I_R	Clamp diode leakage current	V_R = 50V			50	μA	6
		T_{amb} = 70°C V_R = 50V			100	μA	6
V_F	Clamp diode forward voltage	I_F = 350 mA		1.7	2	V	7

VB010

ADVANCE DATA

A MONOLITHIC HIGH VOLTAGE DARLINGTON WITH ON-CHIP INTELLIGENCE FOR PROTECTION AND DIAGNOSTIC OUTPUT

- CONTROL CIRCUIT AND POWER ON ONE CHIP
- 10A OUTPUT CURRENT
- INTEGRATED 400V POWER DARLINGTON
- PROGRAMMABLE BASE CURRENT
- SHORT CIRCUIT PROTECTION
- DIRECT SOA PROTECTION
- THERMAL SHUTDOWN
- DIAGNOSTIC OUTPUT
- TTL/CMOS COMPATIBLE INPUT
- STAND BY MODE

The VB010 is a fully protected high voltage darlington with a TTL/CMOS compatible driving circuit.

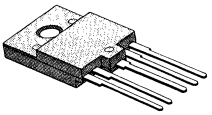
Features of the device include programmable base current, thermal shutdown, short circuit protection, a combined voltage and current detection circuit for direct SOA protection and a diagnostic output.

The VB010 is mounted in the fully isolated ISOWATT5 package and needs no external components.

The VB010 can be used in numerous applications which require an intelligent high voltage, high current power switch driven by a logic level input. The base current is externally programmed by a resistor on the control circuit supply.

A series of built-in protection circuits switch-off the power darlington before safe operating levels are exceeded.

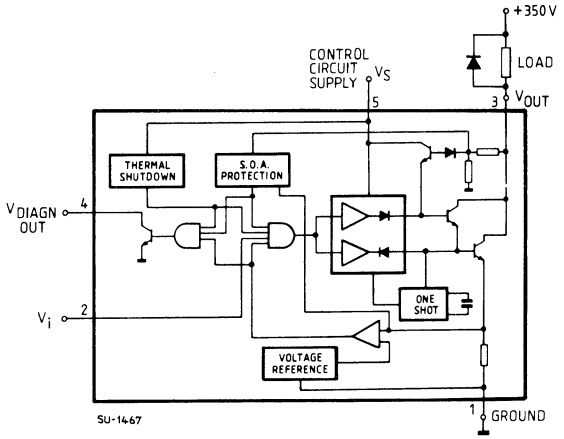
VIPower™ Technology



ISOWATT5

ORDERING NUMBER: VB010

BLOCK DIAGRAM



VB100

ADVANCE DATA

AN INTELLIGENT HIGH VOLTAGE DUTY CYCLE CONTROLLER FOR D.C. MOTOR CONTROL AND INDUCTIVE LOAD DRIVER APPLICATIONS

- CONTROL CIRCUIT AND POWER ON ONE CHIP
- 3A OUTPUT CURRENT
- INTEGRATED 450V POWER DARLINGTON
- PROGRAMMABLE DRIVER CURRENT
- SWITCHING FREQUENCY UP TO 100KHz
- THERMAL SHUTDOWN
- COMPARATOR INPUT PROTECTION
- HIGH IMPEDANCE DIFFERENTIAL INPUTS
- DUTY CYCLE CONTROL LINEARITY WITHIN 1.5%
- MINIMUM EXTERNAL COMPONENTS

The VB100 is an intelligent duty cycle controller with a high voltage, high current open collector darlington output.

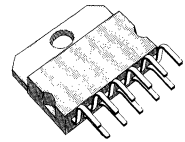
Features of the device include programmable driver current, thermal protection, high impedence differential input, integrated protection at comparator inputs and switching frequency up to 100KHz.

The VB100 is mounted in a 11-lead Multiwatt® plastic power package and requires very few external components.

The VB100 can be used as a D.C. motor controller and driver or as a high voltage inductive load driver, the output voltage duty cycle is adjusted as a function of the input control voltage, at a frequency set by a stable internal sawtooth generator.

A built-in thermal shutdown circuit switches off the power darlington whenever the junction temperature exceeds an internally set value.

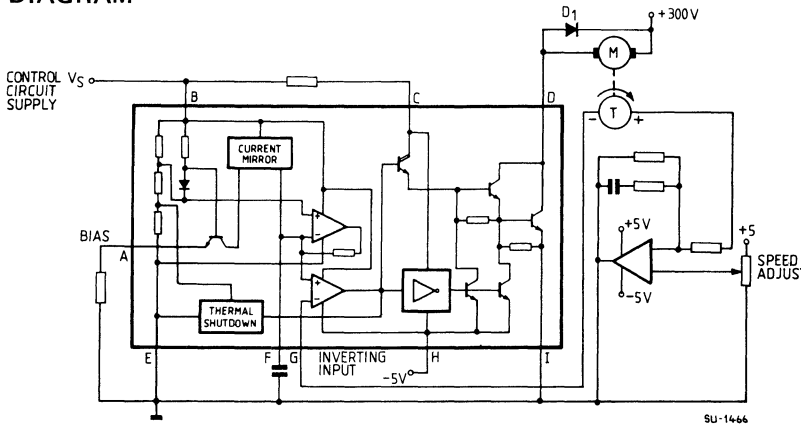
VIPower™ Technology



Multiwatt-11®

ORDERING NUMBER: VB100

BLOCK DIAGRAM



BUR50
BUR50S

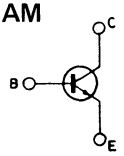
HIGH CURRENT, HIGH SPEED, HIGH POWER TRANSISTOR

The BUR50 is a silicon multiepitaxial planar NPN transistor in modified Jedec TO-3 metal case, the BUR50S is the same type in Jedec TO-3 metal case, intended for use, in switching and linear applications in military and industrial equipment.

ABSOLUTE MAXIMUM RATINGS

V_{CBO}	Collector-base voltage ($I_E=0$)	200	V
V_{CEO}	Collector-emitter voltage ($I_B=0$)	125	V
V_{EBO}	Emitter-base voltage ($I_C=0$)	10	V
I_C	Collector current	70	A
I_{CM}	Collector peak current ($t_p=10$ ms)	100	A
I_B	Base current	20	A
P_{tot}	Total power dissipation at $T_{case} \leq 25$ °C	350	W
T_{stg}	Storage temperature	-65 to 200	°C
T_j	Junction temperature	200	°C

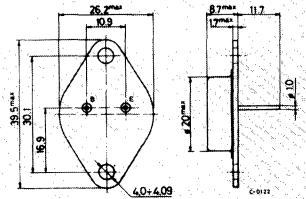
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

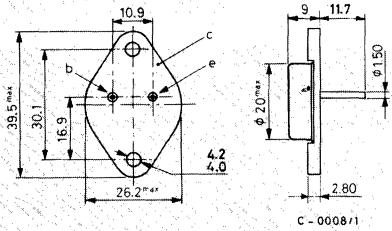
Dimensions in mm

Collector connected to case



BUR 50S

Collector connected to case



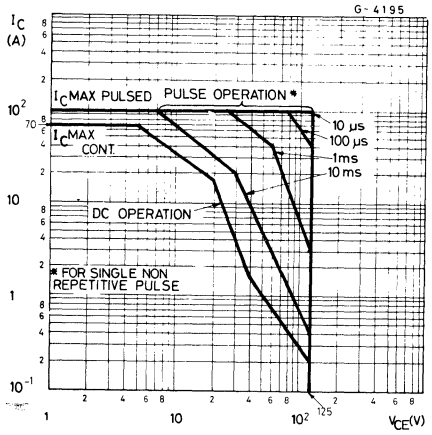
BUR50

ELECTRICAL CHARACTERISTICS (continued)

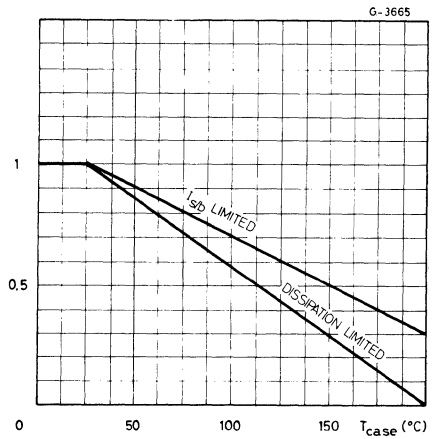
	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{on}	Turn-on time (fig. 2)	I_C =70A I_{B1} =7A V_{CC}=60V		0.5	1.2	µs
t_s	Storage time (fig. 2)	I_C =70A I_{B1} =7A I_{B2} =-7A V_{CC}=60V		0.82	2	µs
t_f	Fall time (fig. 2)			0.1	0.5	µs
	Clamped $E_{s/b}$ Collector current (fig. 1)	V_{clamp}=125V L=500µH	70			A

* Pulsed: pulse duration =300 µs, duty cycle ≤2%

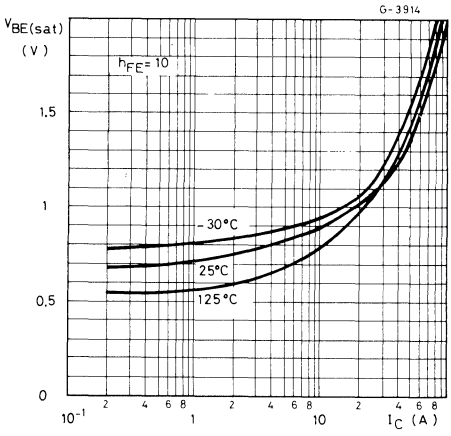
Safe operating areas



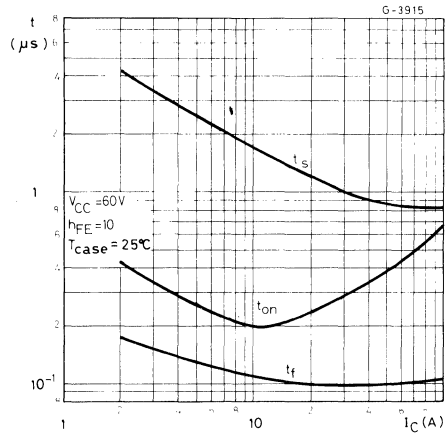
Derating curves



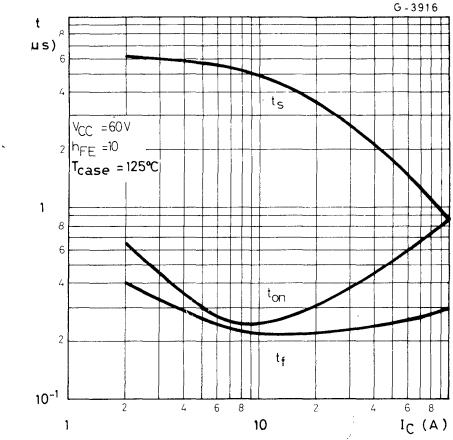
Base-emitter saturation voltage



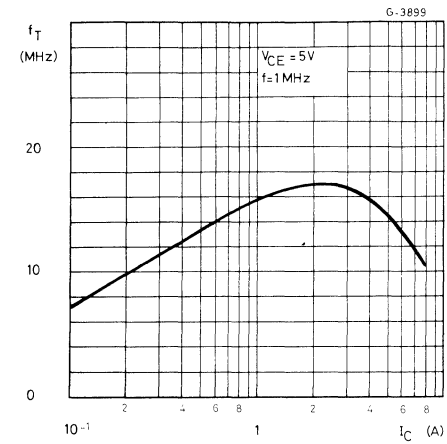
Saturated switching characteristics



Saturated switching characteristics



Transition frequency



BUR51

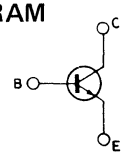
HIGH CURRENT, HIGH SPEED, HIGH POWER TRANSISTOR

The BUR 51 is a silicon multiepitaxial planar NPN transistor in modified Jedec TO-3 metal case, intended for use in switching and linear applications in military and industrial equipment.

ABSOLUTE MAXIMUM RATINGS

V_{CBO}	Collector-base voltage ($I_E=0$)	300	V
V_{CEO}	Collector-emitter voltage ($I_B=0$)	200	V
V_{EBO}	Emitter-base voltage ($I_C=0$)	10	V
I_C	Collector current	60	A
I_{CM}	Collector peak current ($t_p=10$ ms)	80	A
I_B	Base current	16	A
P_{tot}	Total power dissipation at $T_{case} \leq 25$ °C	350	W
T_{stg}	Storage temperature	-65 to 200	°C
T_j	Junction temperature	200	°C

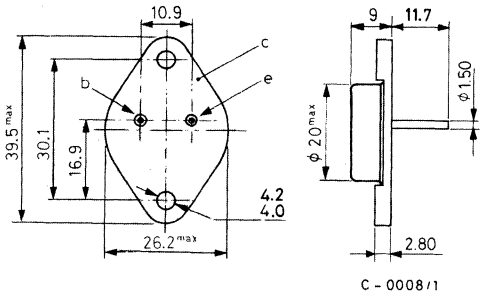
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Collector connected to case



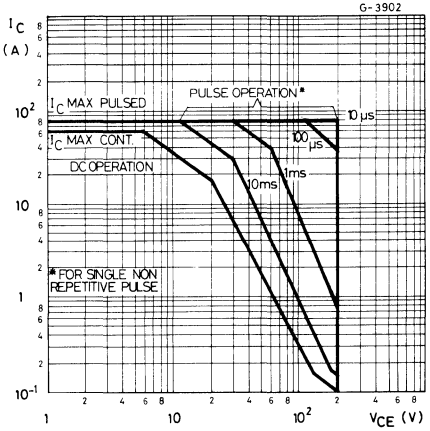
Modified TO-3

ELECTRICAL CHARACTERISTICS (continued)

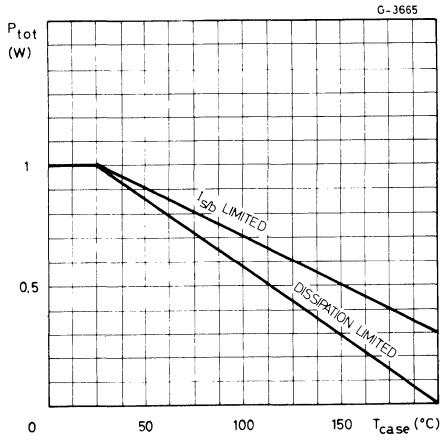
Parameter		Test conditions	Min.	Typ.	Max.	Unit
t_{on}	Turn-on time (fig. 2)	I_C =50A I_{B1} =5A V_{CC}=100V		0.35	1	µs
t_s	Storage time (fig. 2)	I_C =50A I_{B1} =5A I_{B2} =-5A V_{CC}=100V		0.9	2	µs
t_f	Fall time (fig. 2)			0.24	0.6	µs
	Clamped $E_{s/b}$ Collector current (fig. 1)	V_{clamp}=200V L =500µH	50			A

* Pulsed: pulse duration =300 µs, duty cycle ≤2%

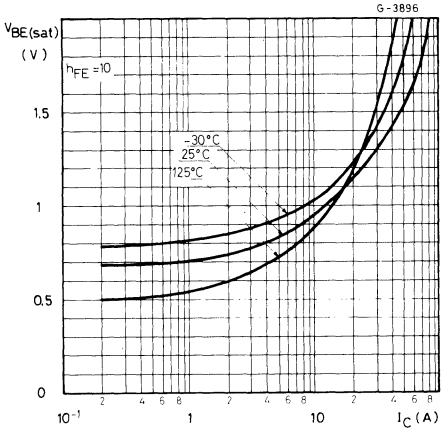
Safe operating areas



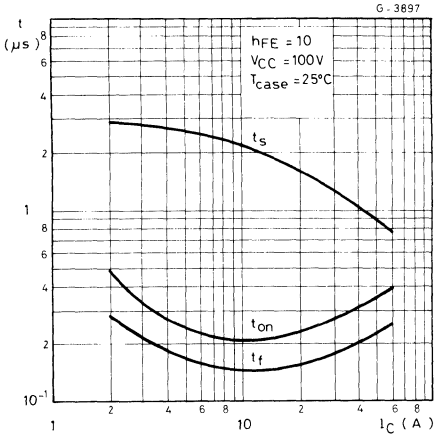
Derating curves



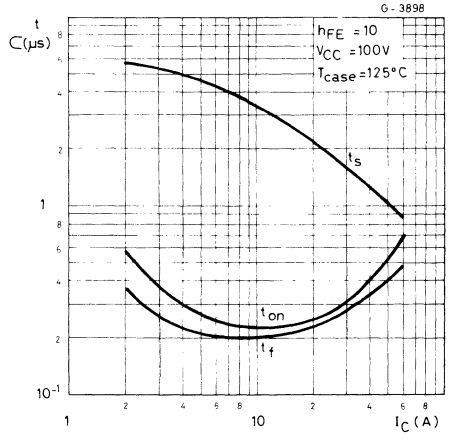
Base-emitter saturation voltage



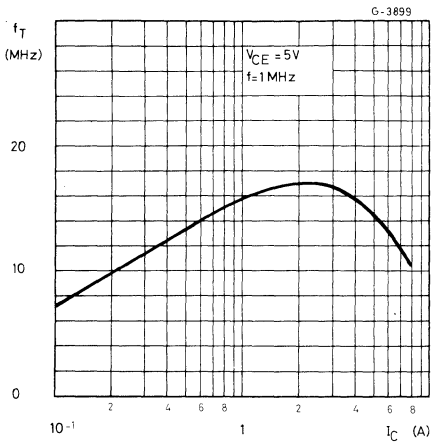
Saturated switching characteristics



Saturated switching characteristics



Transition frequency



BUR52

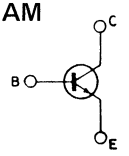
HIGH CURRENT, HIGH SPEED, HIGH POWER TRANSISTOR

The BUR 52 is a silicon multiepitaxial planar NPN transistor in modified Jedec TO-3 metal case, intended for use in switching and linear applications in military and industrial equipment.

ABSOLUTE MAXIMUM RATINGS

V_{CBO}	Collector-base voltage ($I_E=0$)	350	V
V_{CEO}	Collector-emitter voltage ($I_B=0$)	250	V
V_{EBO}	Emitter-base voltage ($I_C=0$)	10	V
I_C	Collector current	60	A
I_{CM}	Collector peak current ($t_p=10$ ms)	80	A
I_B	Base current	16	A
P_{tot}	Total power dissipation at $T_{case} \leq 25$ °C	350	W
T_{stg}	Storage temperature	-65 to 200	°C
T_j	Junction temperature	200	°C

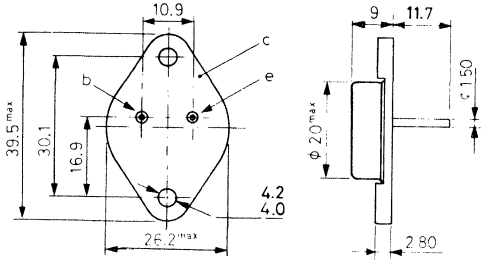
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Collector connected to case



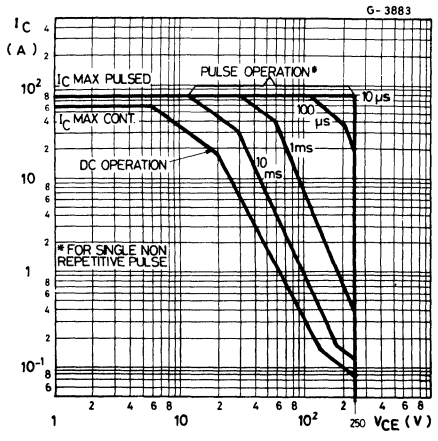
Modified TO-3

ELECTRICAL CHARACTERISTICS (continued)

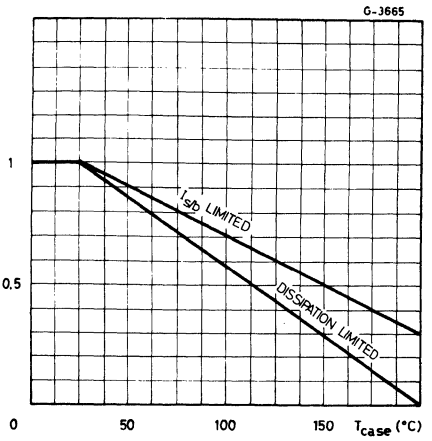
	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_s	Storage time (fig. 2)	I_C =40A I_{B1} =4A I_{B2} =-4A V_{CC}=100V		1.2	2	µs
t_f	Fall time (fig. 2)			0.20	0.6	µs
	Clamped $E_{s/b}$ Collector current (fig. 1)	V_{clamp}=250V L=500µH	40			A

* Pulsed: pulse duration =300 µs, duty cycle ≤2%

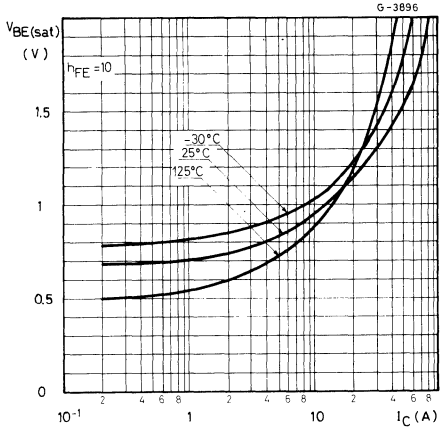
Safe operating areas



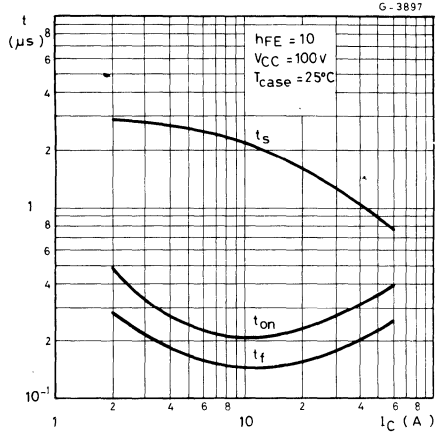
Derating curves



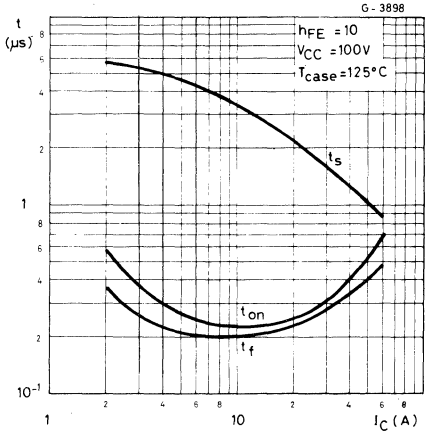
Base-emitter saturation voltage



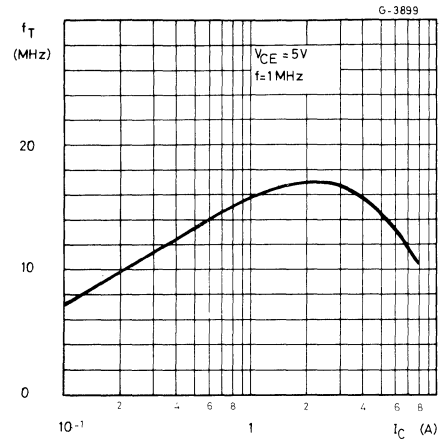
Saturated switching characteristics



Saturated switching characteristics



Transition frequency



BUW22
BUW22A
BUW22AP
BUW22P

ADVANCE DATA

ADVANCE DATA

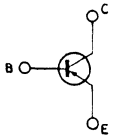
HIGH VOLTAGE POWER SWITCH

The BUW22, BUW22A are silicon miltiepitaxial mesa PNP transistor, in Jedec TO-3, metal case, particularly intended for high voltage, fast switching applications.
The BUW22P, BUW22AP are mounted in TO-220 plastic package.

ABSOLUTE MAXIMUM RATINGS

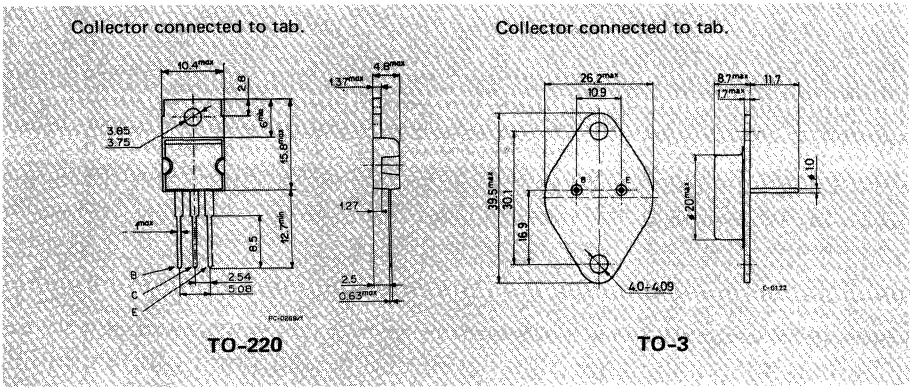
		BUW22/P	BUW22A/P
V_{CES}	Collector-emitter voltage (V_{BE} = o)	-400V	-450V
V_{CEO}	Collector-emitter voltage (I_B = 0)	-350V	-400V
V_{EBO}	Emitter-base voltage (I_C = 0)	-5V	-7V
I_C	Collector current	-6A	
I_{CM}	Collector peak current ($t_p \leqslant$ 10ms)	-8A	
I_B	Base current	-2A	
I_{BM}	Base peak current ($t_p \leqslant$ 10ms)	-4A	
P_{tot}	Total power dissipation at $T_{case} \leqslant 25°C$	(TO-3) 75W	(TO-220) 60W
T_{stg}	Storage temperature	-65 to 175°C	-65 to 150°C
T_j	Junction temperature	175°C	150°C

INTERNAL SCHEMATIC DIAGRAM



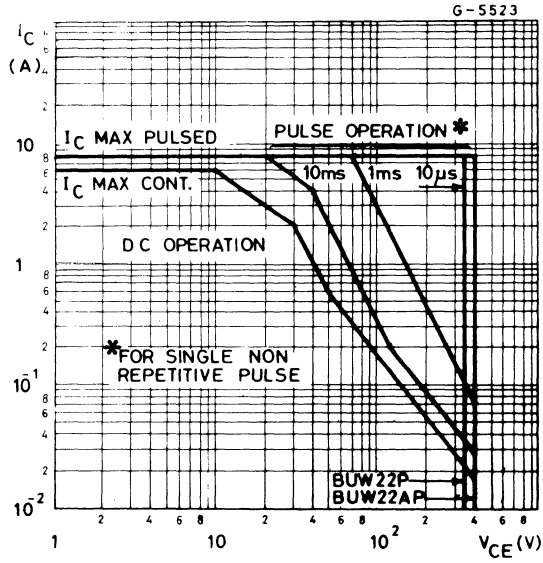
MECHANICAL DATA

Dimensions in mm

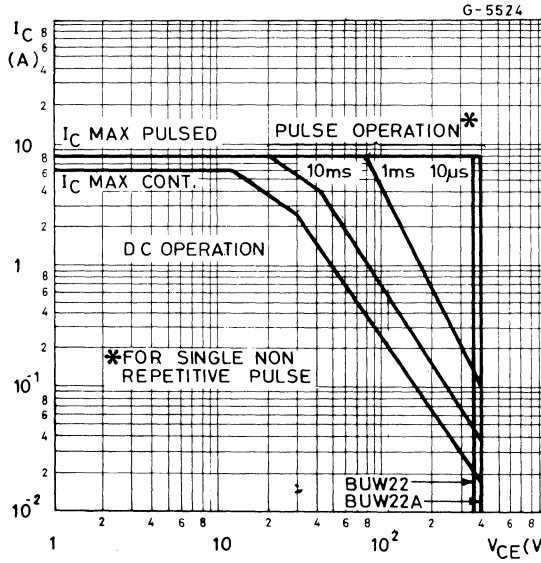


This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

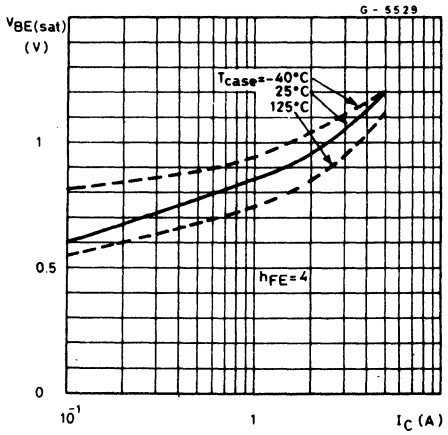
Safe operating areas
(BUW22AP - BUW22P)



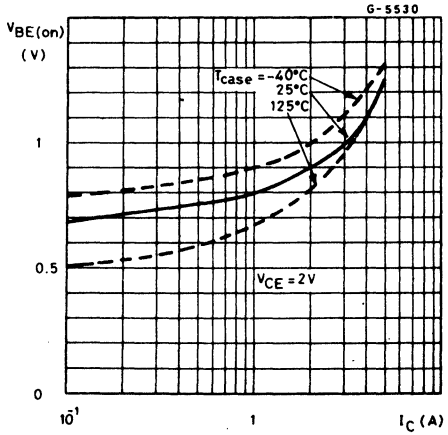
Safe operating areas
(BUW22 - BUW22A)



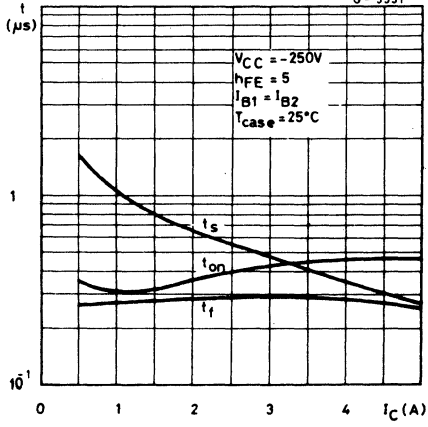
Base-emitter saturation voltage



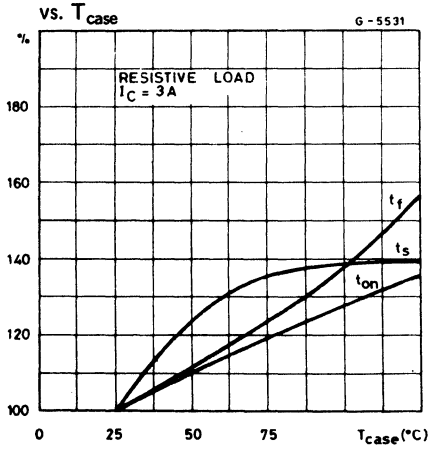
Base-emitter on voltage



Switching times resistive load (test circuit fig. 1)



Switching times percentage variation vs. T_{case}



TEST CIRCUITS

Fig. 1

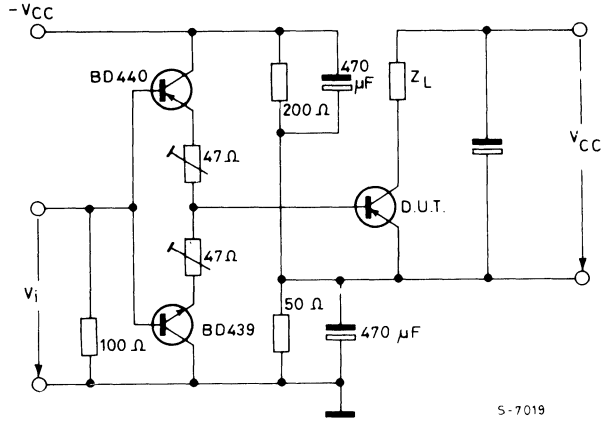
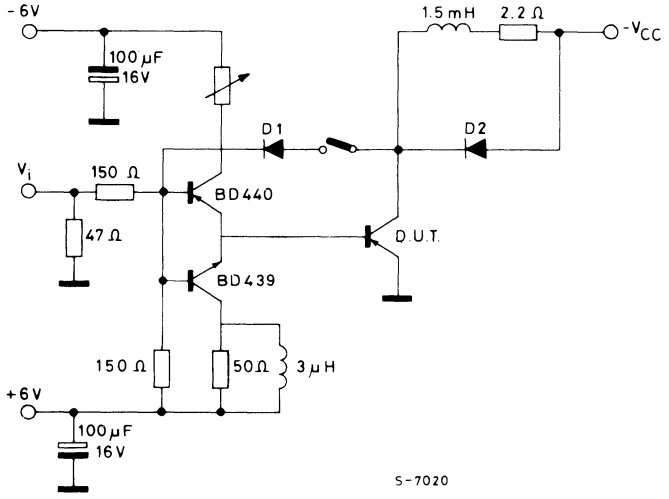


Fig. 2

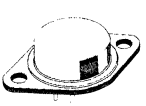


BUW32/BUW32A
BUW32P/BUW32AP
SGSIW32/SGSIW32A

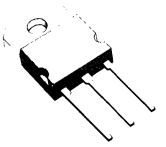
HIGH VOLTAGE POWER SWITCH

- FAST SWITCHING APPLICATIONS
- INDUSTRIAL APPLICATION

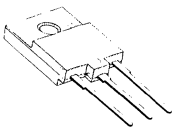
The BUW32/A, BUW32P/AP and SGSIW32/A are silicon multiepitaxial mesa PNP transistors mounted respectively in TO-3 metal case, SOT-93 plastic package and ISOWATT218 fully isolated package.



TO-3

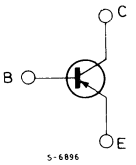


SOT-93 (TO-218)



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

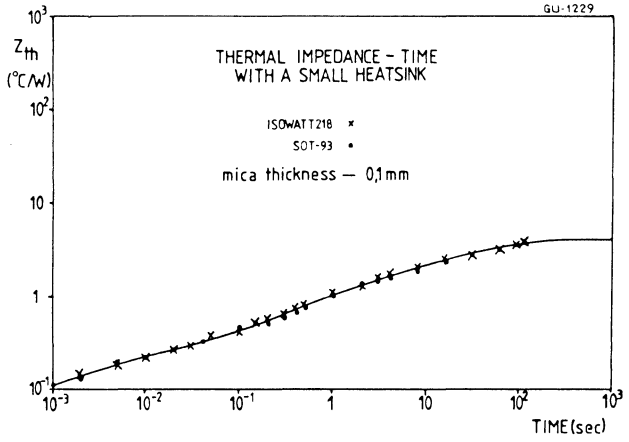
		TO-3 / SOT-93 / ISOWATT218	BUW32 / BUW32P / SGSIW32	BUW32A / BUW32AP / SGSIW32A	
V_{CES}	Collector-emitter voltage (V_{BE} = 0)		−400	−450	V
V_{CEO}	Collector-emitter voltage (I_{BE} = 0)		−350	−400	V
V_{EBO}	Emitter-base voltage (I_C = 0)		−5	−7	V
I_C	Collector current		−10		A
I_B	Base current		− 5		A
			TO-3	SOT-93	ISOWATT218	
V_{ISO}	Isolation voltage (DC)			4000	V
P_{tot}	Total dissipation at $T_c \leqslant 25°C$		125	105	50	W
T_{stg}	Storage temperature		−65 to 175	−65 to 150	−65 to 150	°C
T_j	Max. operating junction temperature		175	150	150	°C

THERMAL RESISTANCE OF THE ISOWATT218

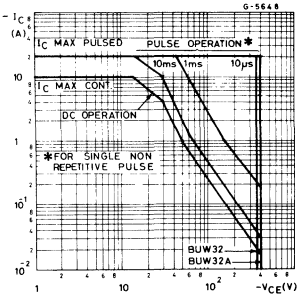
The junction to case thermal resistance of 2.5 °C/W for the ISOWATT218 package may seem quite high at first glance but if compared to a conventional SOT-93 (TO-218) package with a 0.1 mm mica insulating washer, the differences are marginal. The 0.1 mm isolating washer gives 1500V to 2000V DC isolation for the SOT-93 package, SGS guarantee 4000V DC isolation for the ISOWATT 218.

The comparison in fig. 1 shows the dynamic thermal resistance of both devices mounted using a thermal compound. The test illustrate that the ISOWATT218 has an R_{th} very close to that of conventional SOT-93 (TO-218) and any small increase is more than compensated for by the convenience of the ISOWATT218 package. The collector to heatsink capacitance of the ISOWATT218 is typically 17pF.

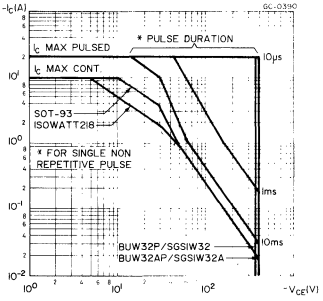
Fig. 1



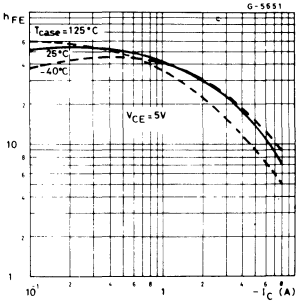
Safe operating areas



Safe operating areas



DC current gain



TEST CIRCUITS

Fig. 1

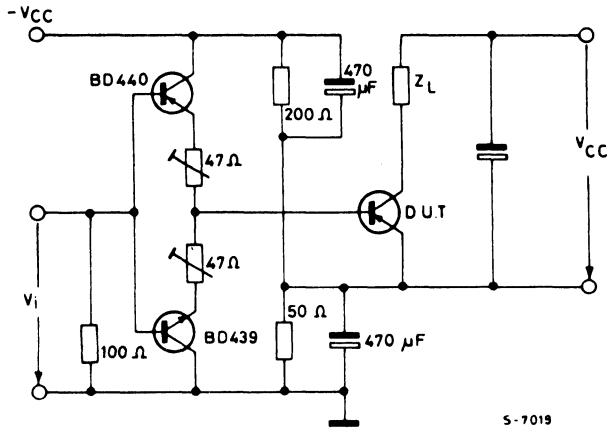
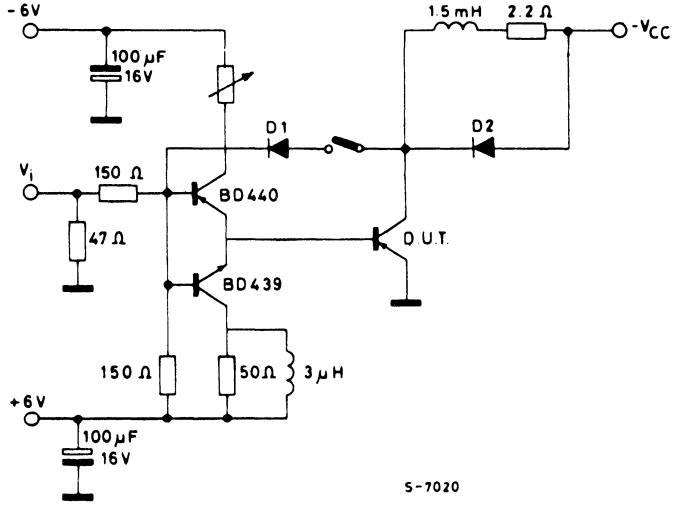


Fig. 2

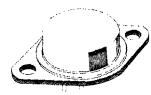


BUW42/BUW42A
BUW42P/BUW42AP
SGSIW42/SGSIW42A

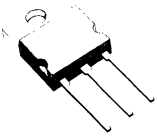
HIGH VOLTAGE POWER SWITCH

- FAST SWITCHING APPLICATIONS
- INDUSTRIAL APPLICATION

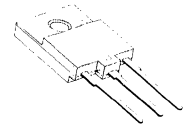
The BUW42/A, BUW42P/AP and SGSIW42/A are silicon multiepitaxial mesa PNP transistors mounted respectively in TO-3 metal case, SOT-93 plastic package and ISOWATT218 fully isolated package.



TO-3

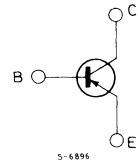


SOT-93 (TO-218)



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

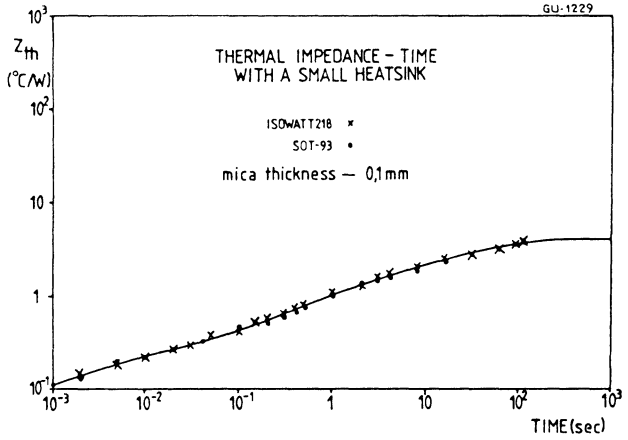
		TO-3 SOT-93 ISOWATT218	BUW42 BUW42P SGSIW42		BUW42A BUW42AP SGSIW42A	
V_{CES}	Collector-emitter voltage (V_{BE} = 0)		−400		−450	V
V_{CEO}	Collector-emitter voltage (I_{BE} = 0)		−350		−400	V
V_{EBO}	Emitter-base voltage (I_C = 0)		−5		−7	V
I_C	Collector current			−15		A
I_{CM}	Collector peak current			−30		A
I_B	Base current			−10		A
			TO-3	SOT-93	ISOWATT218	
V_{ISO}	Isolation voltage (DC)				4000	V
P_{tot}	Total dissipation at $T_c \leqslant 25°C$		150	105	50	W
T_{stg}	Storage temperature		−65 to 175	−65 to 150	−65 to 150	°C
T_j	Max. operating junction temperature		175	150	150	°C

THERMAL RESISTANCE OF THE ISOWATT218

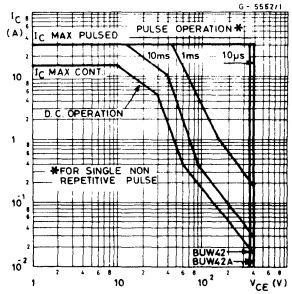
The junction to case thermal resistance of 2.5 °C/W for the ISOWATT218 package may seem quite high at first glance but if compared to a conventional SOT-93 (TO-218) package with a 0.1 mm mica insulating washer, the differences are marginal. The 0.1 mm isolating washer gives 1500V to 2000V DC isolation for the SOT-93 package, SGS guarantee 4000V DC isolation for the ISOWATT 218.

The comparison in fig. 1 shows the dynamic thermal resistance of both devices mounted using a thermal compound. The test illustrate that the ISOWATT218 has an R_{th} very close to that of conventional SOT-93 (TO-218) and any small increase is more than compensated for by the convenience of the ISOWATT218 package. The collector to heatsink capacitance of the ISOWATT218 is typically 17pF.

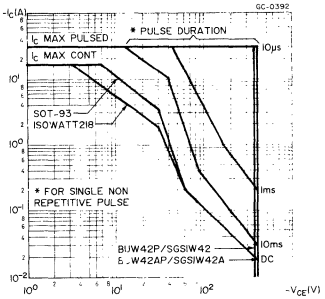
Fig. 1



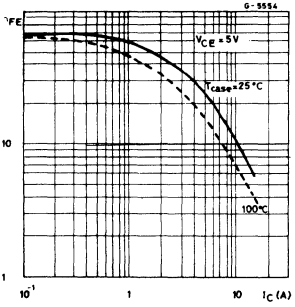
Safe operating area



Safe operating areas



DC current gain



BUX48/BUX48A
BUV48/BUV48A
SGSIV48/SGSIV48A

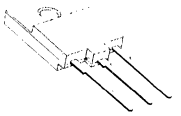
HIGH VOLTAGE POWER SWITCH

- DC, AC MOTOR CONTROL
- SWITCH MODE POWER SUPPLY

The BUX48, BUX48A, BUV48, BUV48A, SGSIV48 and SGSIV48A are multiepitaxial mesa NPN transistors mounted in respectively in TO-3 metal case, SOT-93 plastic package and ISOWATT218 fully isolated package.
They are particularly intended for switching applications directly from the 220V and 380V mains.

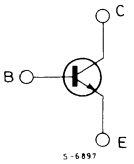
TO-3

SOT-93 (TO-218)



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



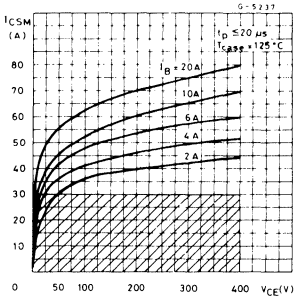
ABSOLUTE MAXIMUM RATINGS

		TO-3 SOT-93 ISOWATT218	BUX48 BUV48 SGSIV48		BUX48A BUV48A SGSIV48A	
V_{CES}	Collector-emitter voltage (V_{BE} = 0)		850		1000	V
V_{CER}	Collector-emitter voltage (R_{BE} = 10Ω)		850		1000	V
V_{CEO}	Collector-emitter voltage (I_{BE} = 0)		400		450	V
V_{EBO}	Emitter-base voltage (I_C = 0)			7		V
I_C	Collector current			15		A
I_{CM}	Collector peak current I_{CP} ($t_p \leqslant$ 5 ms)			30		A
I_{CP}	Collector peak current non rep. ($t_p \leqslant 20\ \mu s$)			55		A
I_B	Base current			4		A
I_{BM}	Base peak current ($t_p \leqslant$ 5 ms)			20		A
			TO-3	SOT-93	ISOWATT218	
V_{ISO}	Isolation voltage (DC)				4000	V
P_{tot}	Total dissipation at $T_c \leqslant 25°C$		175	125	50	W
T_{stg}	Storage temperature		−65 to 200	−65 to 150	−65 to 150	°C
T_j	Max. operating junction temperature		200	150	150	°C

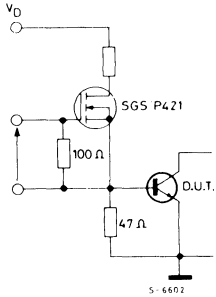
ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
RESISTIVE LOAD					
t_{on} Turn-on time	for **BUX48/BUV48/SGSIV48** V_{CC} = 150 V I_C = 10 A I_{B1} = 2 A for **BUX48A/BUV48A/SGSIV48A** V_{CC} = 150 V I_C = 8 A I_{B1} = 1.6 A			1 1	μs μs
t_s Storage time	for **BUX48/BUV48/SGSIV48** V_{CC} = 150 V I_C = 10 A $I_{B1} = -I_{B2}$ = 2 A for **BUX48A/BUV48A/SGSIV48A** V_{CC} = 150 V I_C = 8 A $I_{B1} = -I_{B2}$ = 1.6 A			3 3	μs μs
t_f Fall time	for **BUX48/BUV48/SGSIV48** V_{CC} = 150 V I_C = 10 A $I_{B1} = -I_{B2}$ = 2 A for **BUX48A/BUV48A/SGSIV48A** V_{CC} = 150 V I_C = 8 A $I_{B1} = -I_{B2}$ = 1.6 A			0.8 0.8	μs μs
INDUCTIVE LOAD					
t_s Storage time	for **BUX48/BUV48/SGSIV48** V_{CC} = 300 V I_C = 10A L_B = 3μH I_{B1} = 2 A V_{BE} = −5 V same T_c = 125°C for **BUX48A/BUV48A/SGSIV48A** V_{CC} = 300 V I_C = 8 A L_B = 3 μH I_{B1} = 1.6 A V_{BE} = −5 V same T_c = 125°C		2.7 3	5 5	μs μs μs μs
t_f Fall time	for **BUX48/BUV48/SGSIV48** V_{CC} = 300 V I_C = 10 A L_B = 3μH I_{B1} = 2 A V_{BE} = −5 V same T_c = 125°C for **BUX48A/BUV48A/SGSIV48A** V_{CC} = 300 V I_C = 8 A L_B = 3μH I_{B1} = 1.6 A V_{BE} = −5 V same T_c = 125°C		0.16 0.13	0.4 0.4	μs μs μs μs

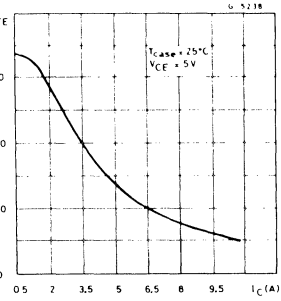
Forward biased accidental overload area



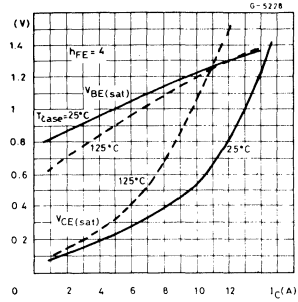
Forward biased accidental overload area test circuit.



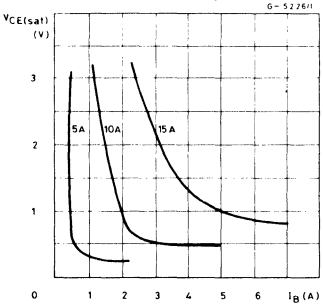
DC current gain



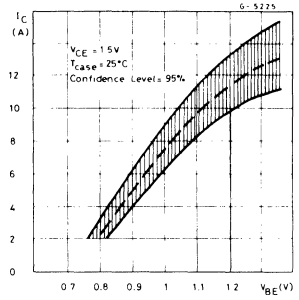
Saturation voltages



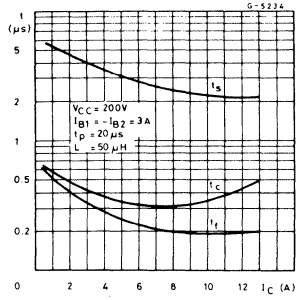
Collector-emitter saturation voltage



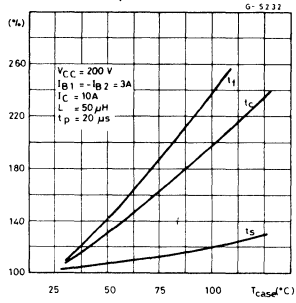
Collector current spread vs. base emitter voltage



Switching times vs. collector current with I_B constant



Switching times percentage variation vs. case temperature



Switching times with and without antisaturation network (See fig.**6**)

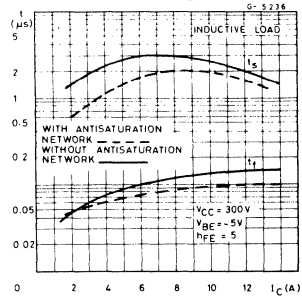


Fig. 5 - Switching times test circuit on resistive load.

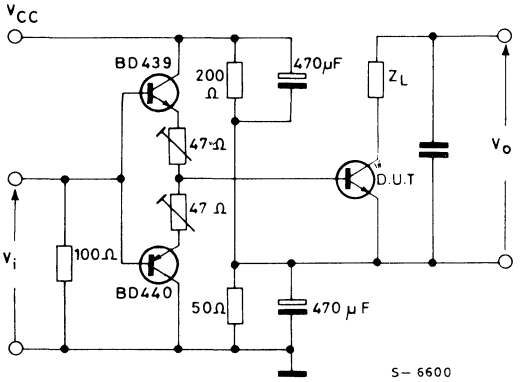
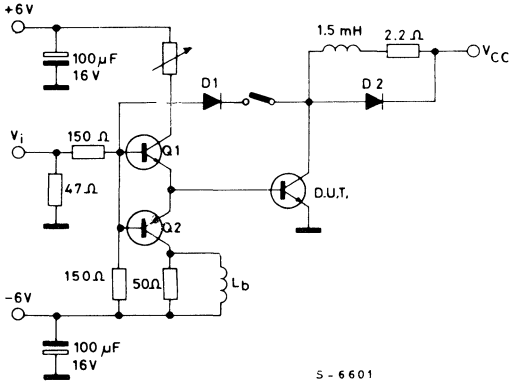


Fig.6 - Switching times test circuit on inductive load, with and without antisaturation network



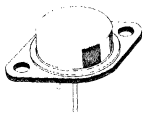
D1, D2 - Fast recovery diodes
Q1, Q2 - Transistors SGS: 2N5191, 2N5195

BUX48B/BUX48C
BUV48B/BUV48C
SGSIV48C

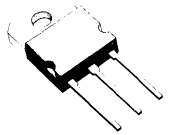
HIGH VOLTAGE POWER SWITCHING

- INDUSTRIAL APPLICATIONS

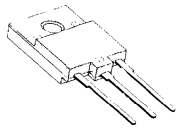
The BUX48B, BUX48C, BUV48B, BUV48C and SGSIV48C are multiepitaxial mesa NPN transistors mounted respectively in TO-3 metal case SOT-93 plastic package and ISOWATT218 fully isolated package.
They are particularly intended for switching and industrial applications from single and three-phase mains.



TO-3

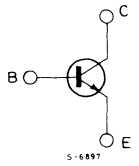


SOT-93 (TO-218)



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

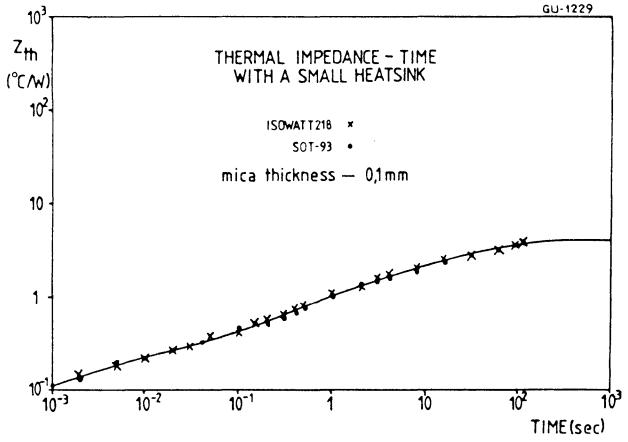
		TO-3 / BUX48B / BUV48B	SOT-93	ISOWATT218 / BUX48C / BUV48C / SGSIV48C	
V_{CER}	Collector-emitter voltage (R_{BE} = 10Ω)	1200		1200	V
V_{CES}	Collector-emitter voltage (V_{BE} = 0)	1200		1200	V
V_{CEO}	Collector-emitter voltage (I_B = 0)	600		700	V
V_{EBO}	Emitter-base voltage (I_C = 0)		7		V
I_C	Collector current		15		A
I_{CM}	Collector peak current ($t_p \leqslant$ 5 ms)		30		A
I_{CP}	Collector peak current non rep. ($t_p \leqslant 20\mu s$)		55		A
I_B	Base peak current		4		A
I_{BM}	Base peak current ($t_p \leqslant$ 5 ms)		20		A
		TO-3	**SOT-93**	**ISOWATT218**	
V_{ISO}	Isolation voltage (DC)			4000	V
P_{tot}	Total dissipation at $T_c \leqslant 25°C$	175	120	50	W
T_{stg}	Storage temperature	−65 to 200	−65 to 150	−65 to 150	°C
T_j	Max. operating junction temperature	200	150	150	°C

THERMAL RESISTANCE OF THE ISOWATT218

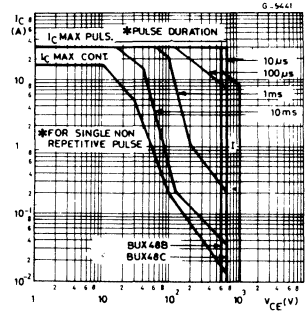
The junction to case thermal resistance of 2.5 °C/W for the ISOWATT218 package may seem quite high at first glance but if compared to a conventional SOT-93 (TO-218) package with a 0.1 mm mica insulating washer, the differences are marginal. The 0.1 mm isolating washer gives 1500V to 2000V DC isolation for the SOT-93 package, SGS guarantee 4000V DC isolation for the ISOWATT 218.

The comparison in fig. 1 shows the dynamic thermal resistance of both devices mounted using a thermal compound. The test illustrate that the ISOWATT218 has an R_{th} very close to that of conventional SOT-93 (TO-218) and any small increase is more than compensated for by the convenience of the ISOWATT218 package. The collector to heatsink capacitance of the ISOWATT218 is typically 17pF.

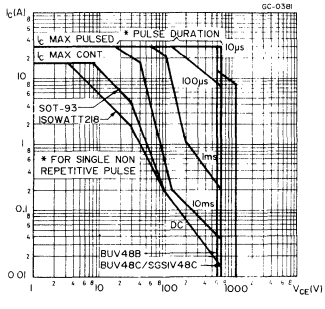
Fig. 1



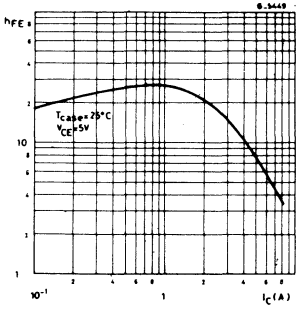
Safe operating areas



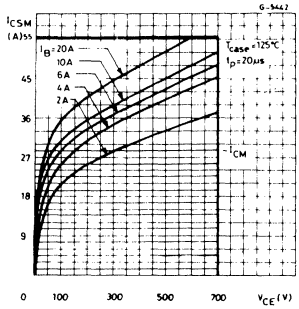
Safe operating areas



DC current gain



Forward biased accidental overload area



Clamped reverse bias safe operating areas

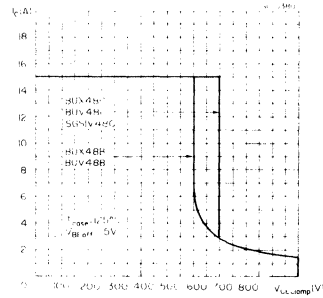


Fig. 2 - Switching times test circuit on resistive load.

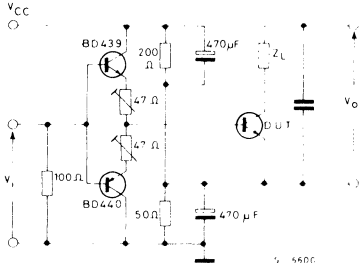
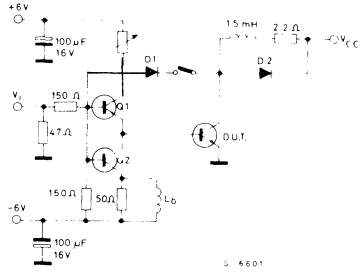


Fig.3 - Switching times test circuit on inductive load, with and without antisaturation network



D1, D2 - Fast recovery diodes
Q1, Q2 - Transistors SGS: 2N5191, 2N5195

BUX98
BUX98A

ADVANCE DATA

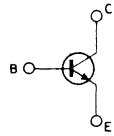
HIGH VOLTAGE FAST SWITCHING

The BUX98 and BUX98A are silicon multiepitaxial mesa NPN transistors in Jedec TO-3 metal-case intended for use in switching and industrial applications from single and three-phase mains operation.

ABSOLUTE MAXIMUM RATINGS

		BUX98	BUX98A
V_{CER}	Collector-emitter voltage ($R_{BE} = 10\Omega$)	850V	1000V
V_{CES}	Collector-base voltage ($V_{BE} = 0$)	850V	1000V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	400V	450V
V_{EBO}	Emitter-base voltage ($I_C = 0$)	7V	
I_C	Collector current	30A	
I_{CM}	Collector peak current ($t_p < 5$ms)	60A	
I_{CP}	Collector peak current non rep. ($t_p < 20\mu$s)	80A	
I_B	Base current	8A	
I_{BM}	Base peak current ($t_p < 5$ms)	30A	
P_{tot}	Total power dissipation at $T_{case} < 25°C$	250W	
T_{stg}	Storage temperature	-65 to 200°C	
T_j	Junction temperature	200°C	

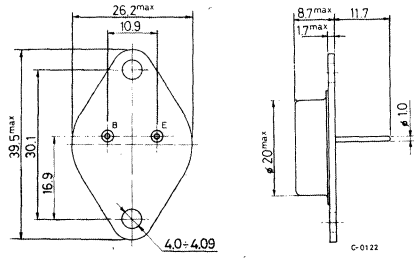
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Collector connected to case



TO-3

BUX98C

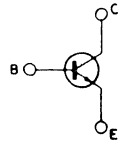
HIGH VOLTAGE SWITCH

The BUX98C, is a multiepitaxial mesa NPN transistors in Jedec TO-3 metal-case intended for use in switching and industrial applications from single and three-phase mains operation.

ABSOLUTE MAXIMUM RATINGS

V_{CER}	Collector-emitter voltage ($R_{BE} = 10\Omega$)	1200	V
V_{CES}	Collector-base voltage ($V_{BE} = 0$)	1200	V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	700	V
V_{EBO}	Emitter-base voltage ($I_C = 0$)	7	V
I_C	Collector current	30	A
I_{CM}	Collector peak current (tp $<$ 5ms)	60	A
I_{CP}	Collector peak current non repetitive (tp $<$ 20μs)	80	A
I_B	Base current	8	A
I_{BM}	Base peak current (tp $<$ 5ms)	30	A
P_{tot}	Total power dissipation at $T_{case} < 25°C$	250	W
T_{stg}	Storage temperature	-65 to 200	°C
T_j	Junction temperature	200	°C

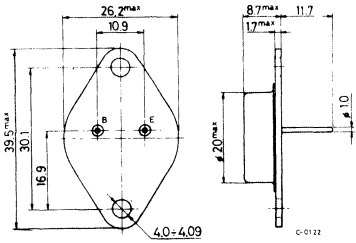
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

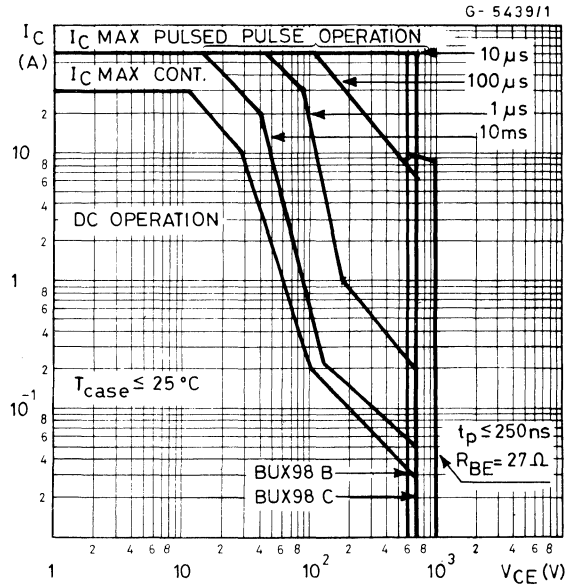
Dimensions in mm

Collector connected to case

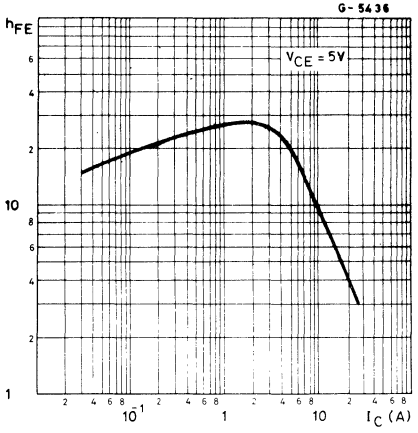


TO-3

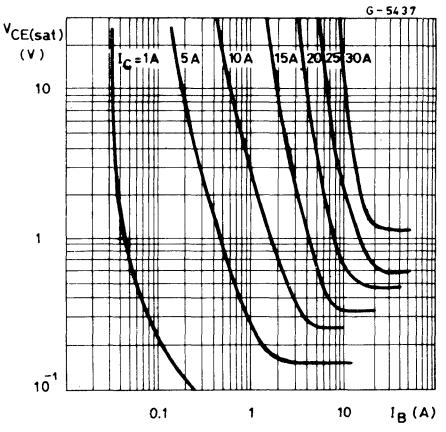
Safe operating areas



DC current gain



Collector-emitter saturation voltage

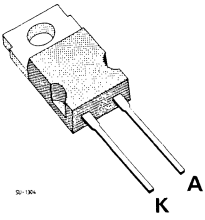


BYW29-50
BYW29-100
BYW29-150
BYW29-200

HIGH SPEED SWITCHING APPLICATIONS SECONDARY RECTIFICATION

- VOLTAGE RANGE: 50V - 200V
- AVERAGE CURRENT: 7.6A
- VERY LOW REVERSE RECOVERY TIME: t_{rr} 35ns
- VERY LOW SWITCHING LOSSES
- LOW NOISE TURN-OFF SWITCHING

Typical applications include secondary rectification in high frequency switching power supplies and freewheel diodes in stepper motor control systems.



DIOWATT1

ABSOLUTE MAXIMUM RATINGS

		BYW29				
		−50	−100	−150	−200	
V_{RRM}	Peak repetitive reverse voltage	50	100	150	200	V
V_{RWM}	Working peak reverse voltage	50	100	150	200	V
V_R	Continuous reverse voltage	50	100	150	200	V
I_{FRM}	Repetitive peak forward current (t = 10μs)	80				A
$I_{F(AV)}$	Average forward current T_{case} = 70°C (switching operation, δ = 0.5)	7.6				A
I_{FSM}	Surge non repetitive forward current (t = 10ms)	80				A
P_{tot}	Total dissipation at T_{case} = 70°C	18				W
T_{stg}	Storage temperature	−40 to 150				°C
T_j	Max. junction temperature	150				°C

MJE13006
MJE13007
MJE13007A

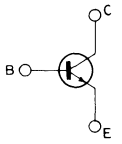
MOTOR CONTROL, SWITCH REGULATORS

The MJE13006, MJE13007 and MJE13007A are silicon multiepitaxial mesa NPN transistors. They are mounted in Jedec TO-220 plastic package, intended for use in motor controls, switching regulator's etc.

ABSOLUTE MAXIMUM RATINGS

		MJE13006	MJE13007	MJE13007A
V_{CEO}	Collector-emitter voltage ($V_B = 0$)	300V	400V	400V
V_{CEV}	Collector-emitter voltage	600V	700V	850V
V_{EBO}	Emitter-base voltage ($I_C = 0$)		9V	
I_C	Collector current		8A	
I_{CM}	Collector peak current		16A	
I_B	Base current		4A	
I_{BM}	Base peak current		8A	
I_E	Emitter current		12A	
I_{EM}	Emitter peak current		24A	
P_{tot}	Total power dissipation at $T_{case} \leqslant 25°C$		80W	
T_{stg}	Storage temperature		-65 to 150°C	
T_j	Junction temperature		150°C	

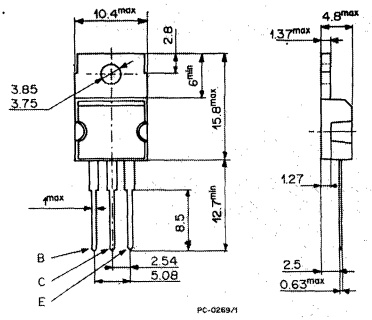
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Collector connected to tab.



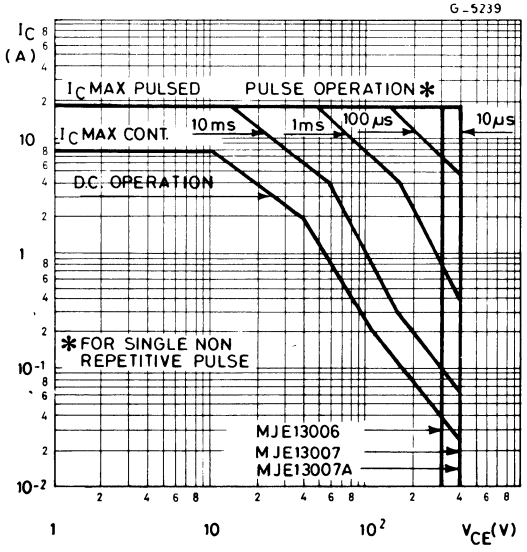
TO-220

ELECTRICAL CHARACTERISTICS (Continued)

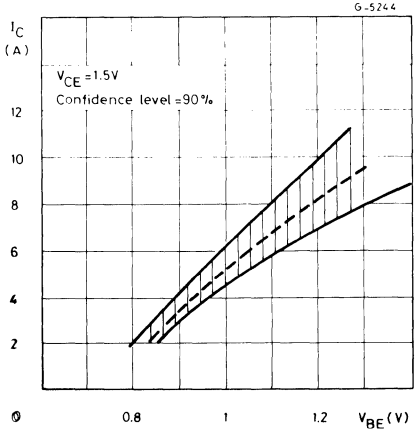
Parameter		Test conditions	Min.	Typ.	Max.	Unit
RESISTIVE SWITCHING TIMES (Fig. 2)						
t_{on}	Turn-on time	$V_{CC}=125V$ $I_C=5A$			0.7	μs
t_s	Storage time	$I_{B1}=-I_{B2}=1A$			3	μs
t_f	Fall time	$t_p=25\mu s$ Duty Cycle $<1\%$			0.7	μs
INDUCTIVE SWITCHING TIMES (Fig. 1)						
t_f	Fall time	$V_{CC}=125V$ $I_C=5A$ $I_{B1}=1A$ $t_p=25\mu s$ Duty cycle $<1\%$ $T_{case}=100°C$			0.3	μs
		$V_{CC}=125V$ $I_C=5A$ $I_{B1}=1A$ $t_p=25\mu s$ Duty cycle $\leqslant 1\%$			0.6	μs

* Pulsed: pulse duration $\leqslant 300\mu s$, duty cycle $\leqslant 1.5\%$

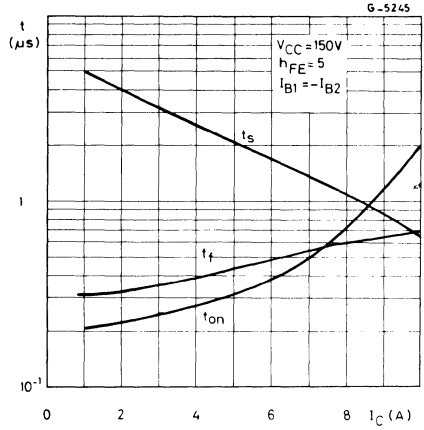
Safe operating areas



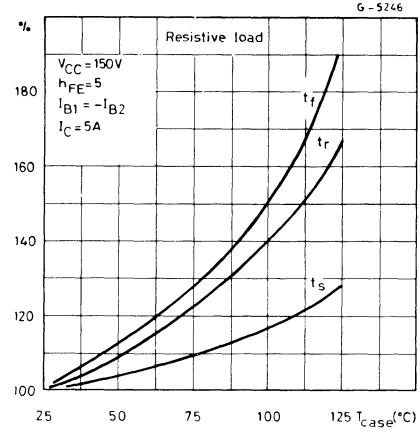
Collector current spread vs. base emitter voltage



Switching times resistive load (See fig. 2)



Switching times percentage variation vs. case temperature



Switching times inductive load (See fig. 1)

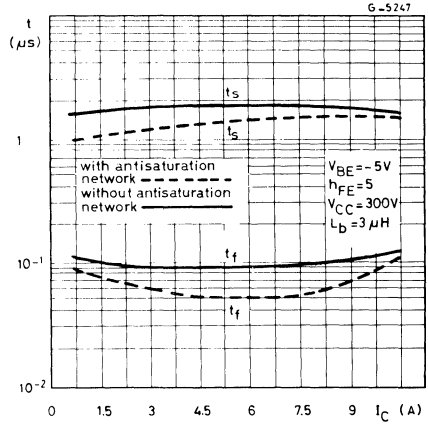
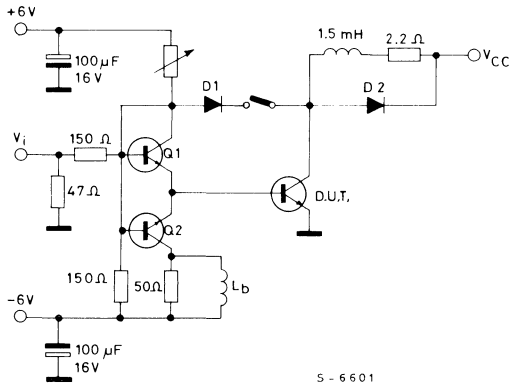


Fig. 1 - Switching times test circuit on inductive load, with and without antisaturation network



D1, D2 - Fast recovery diodes
Q1, Q2 - Transistors SGS: 2N5191, 2N5195

Fig. 2 - Switching times test circuit on resistive load.

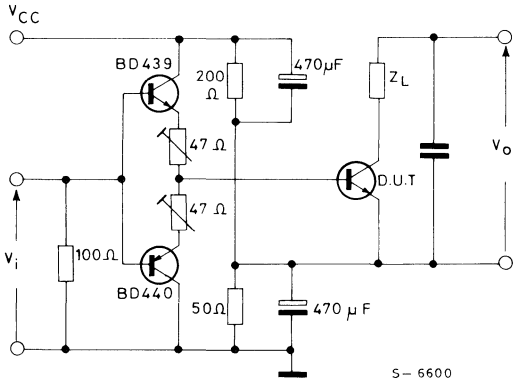
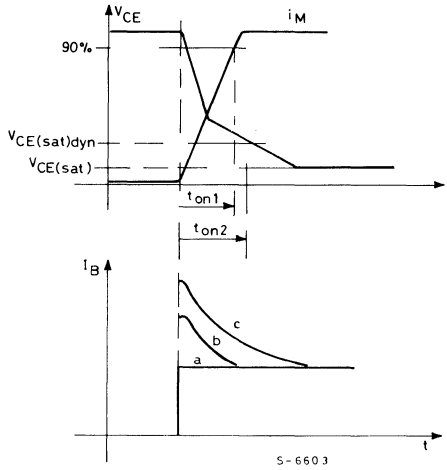


Fig. 6 - Remarks to $V_{CE(sat)}$ dyn. test circuit (fig. 4)



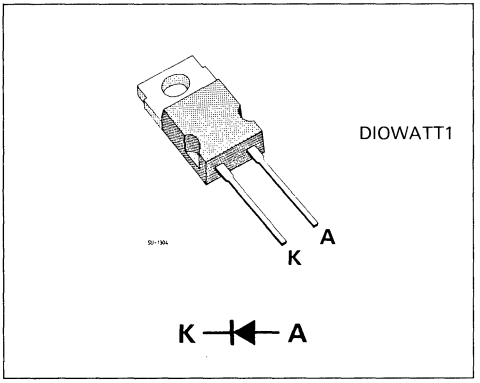
The speed-up capacitor decreases the $V_{CE\ (sat)}$ dyn. as shown in diagram (figure 6).
The 50nF capacitor modifies the shape of base current with a overshoot.

SGS8R05
SGS8R10
SGS8R15
SGS8R20

HIGH SPEED SWITCHING APPLICATIONS SECONDARY RECTIFICATION

- VOLTAGE RANGE: 50V - 200V
- AVERAGE CURRENT: 8A
- VERY LOW REVERSE RECOVERY TIME: t_{rr} 35ns
- VERY LOW SWITCHING LOSSES
- LOW NOISE TURN-OFF SWITCHING

Typical applications include secondary rectification in high frequency switching power supplies and freewheel diodes in stepper motor control systems.



ABSOLUTE MAXIMUM RATINGS

		SGS				
		8R05	8R10	8R15	8R20	
V_{RRM}	Peak repetitive reverse voltage	50	100	150	200	V
V_{RWM}	Working peak reverse voltage	50	100	150	200	V
V_R	Continuous reverse voltage	50	100	150	200	V
I_{FRM}	Repetitive peak forward current (t = 10μs)	100				A
$I_{F(AV)}$	Average forward current T_{case} = 70°C (switching operation, δ = 0.5)	8				A
I_{FSM}	Surge non repetitive forward current (t = 10ms)	80				A
P_{tot}	Total dissipation at T_{case} = 70°C	50				W
T_{stg}	Storage temperature	−65 to 150				°C
T_j	Max. operating junction temperature	150				°C

Fig. 4 Recovery time and peak reverse current vs. I_F

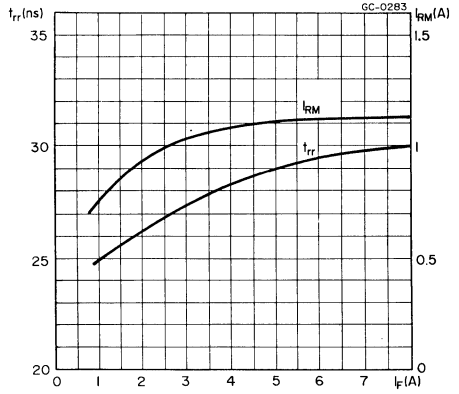


Fig. 5 Recovered charge vs. di_F/dt

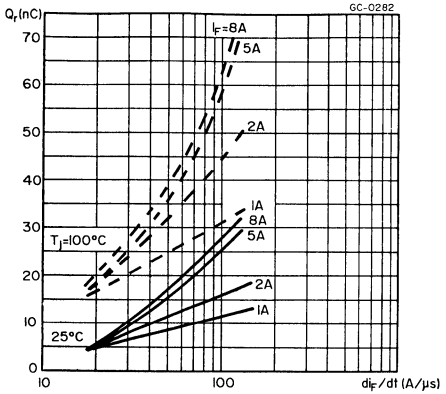


Fig. 6 Recovery time vs. di_F/dt

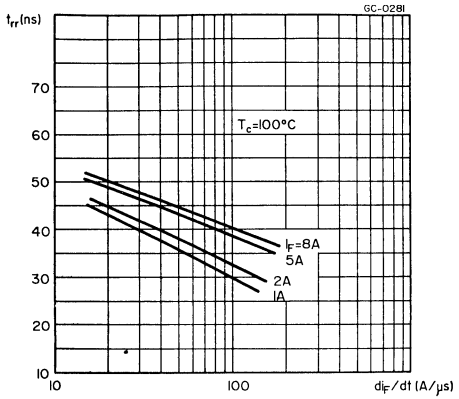
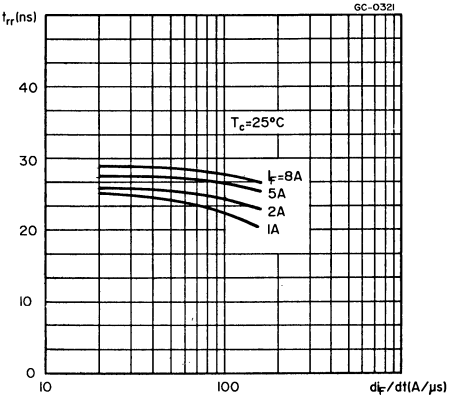


Fig. 7 Recovery time vs. di_F/dt



SGS15DB070D
SGS15DB080D

TRANSPACK NPN POWER DARLINGTON MODULE

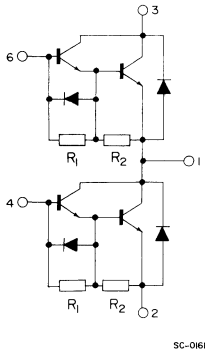
APPLICATIONS: These products are silicon NPN power darlingtons in half bridge configuration for industrial switching applications with three-phase mains operation.

ISOLATED POWER MODULE (15KVA - 375W)	FAST FREEWHEEL DIODES

ABSOLUTE MAXIMUM RATINGS

		SGS15DB070D	SGS15DB080D	
V_{CBO}	Collector-base voltage (I_E = 0)	1000	1200	V
V_{CES}	Collector-emitter voltage (V_{BE} = 0)	1000	1200	V
V_{CEX}	Collector-emitter voltage (V_{BE} = −1.5V)	1000	1200	V
V_{CEO}	Collector-emitter voltage (I_B = 0)	700	800	V
V_{CEOL}	Overload switch-off at 1.5 times $I_{C\ (sat)}$*	650		V
V_{EBO}	Emitter-base voltage (I_C = 0)	7		V
I_C	Collector current	23		A
I_{CM}	Collector peak current (t_p<10 ms)	60		A
I_{CP}	Collector peak current non repetitive (t_p<20 μs)	100		A
I_B	Base current	6		A
I_{BP}	Base peak current non repetitive (t_p<20 μs)	30		A
T_{stg}	Storage temperature	− 40 to 150		°C
T_j	Max. operating junction temperature (continuous)	150		°C
T_j	Max. operating junction temperature (1 minute)	175		°C

INTERNAL SCHEMATIC DIAGRAM

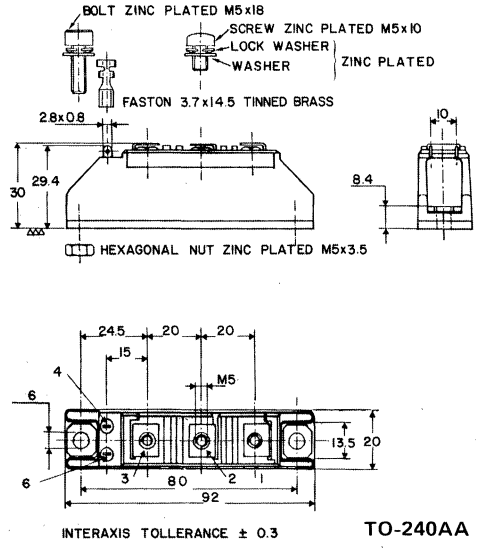


R_1 typ. 10 Ω

R_2 typ. 50 Ω

MECHANICAL DATA

Dimensions in mm



TO-240AA

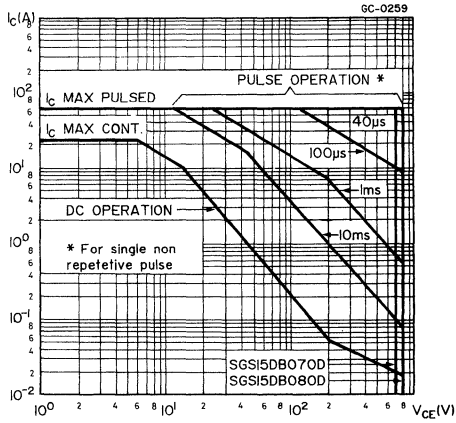
ELECTRICAL CHARACTERISTICS (Continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
t_{rr}	Diode reverse recovery time	I_f = 15 A di/dt = 100A/μs		0.20	0.5	μs
I_{rm}	Diode reverse recovery current			12		A
I_{frm}	Diode forward current	t = 1ms	160			A

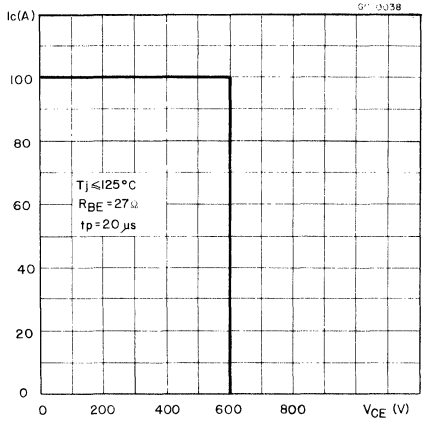
INSULATION TESTING

The insulation between the live parts and the base plate of TO-240 is tested before delivery for one second at 2500 V a.c.
If this test is repeated by the user either as a goods inwards check or as a test of the final equipment, in accordance with IEC Publication 146 (1973), clause 492.1 or DIN 57558 part 1/VDE 0558 part 1/8.77, section 5.7.9., only a voltage slowly increasing up to the above value should be used. If the voltage is applied for one minute as recommended by the above standards then the specified value of 2000 V should be taken.
During the test all electrical terminals including the drive terminals must be connected with each other in order to avoid damage by inductively or capacitively induced voltage transients. The test voltage is applied between the connected terminals and the base plate.

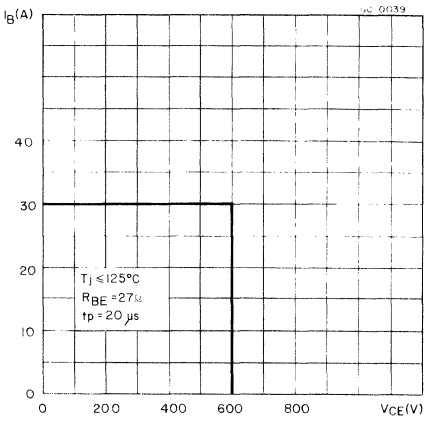
Safe operating areas for each section



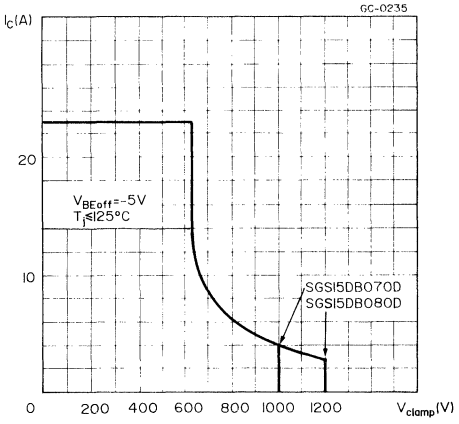
Collector overload SOA (see fig. 1)



Base overload SOA (see fig. 1)



Reverse biased SOA (see fig. 2)



Switching times inductive load (see fig. 3)

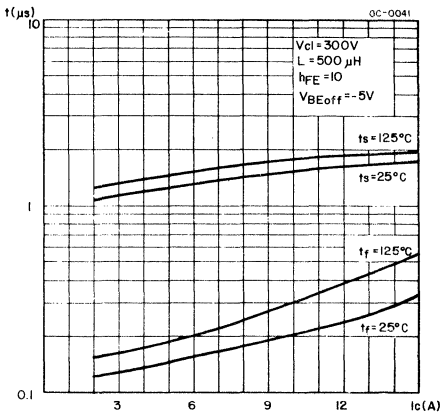


Fig. 2 RBSOA TEST CIRCUIT

RBSOA test circuit has been driven by the switching times test circuit with $R_{B2} = O$.
RBSOA sensitivity to T_j variations is very limited, so that the limits shown can be kept valid at ambient temperature as well.

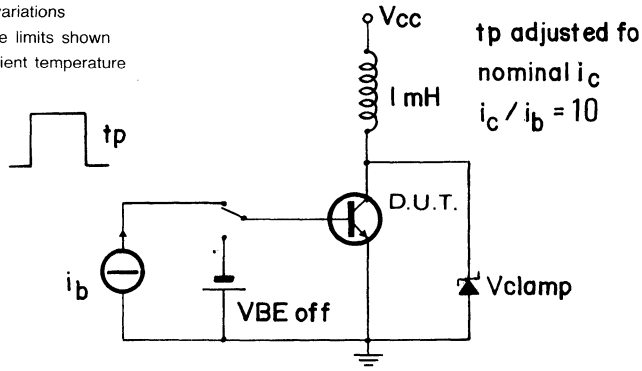
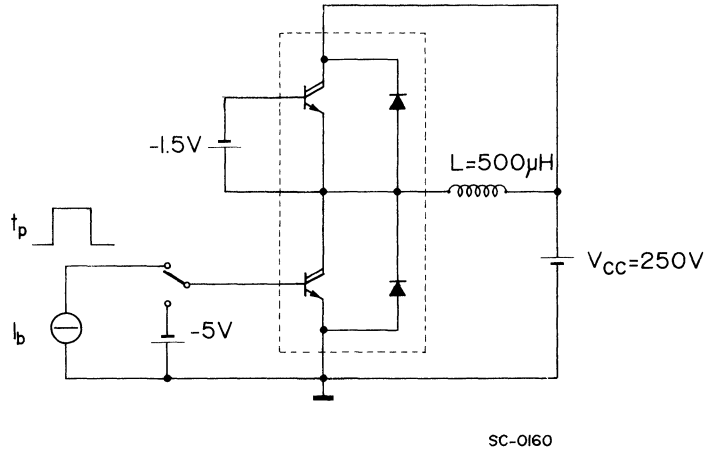


Fig. 3 Switching times test circuit

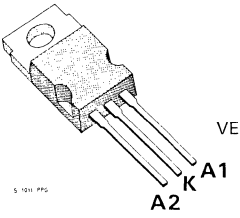


SGS16DR05
SGS16DR10
SGS16DR15
SGS16DR20

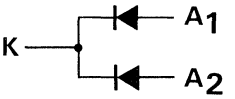
HIGH SPEED SWITCHING APPLICATIONS

- VOLTAGE RANGE: 50V→200V
- AVERAGE CURRENT: 16A
- VERY LOW REVERSE RECOVERY TIME: t_{rr} 35ns
- VERY LOW SWITCHING LOSSES
- LOW NOISE TURN-OFF SWITCHING

Typical applications include secondary rectification in high frequency switching power supplies.



TO-220
VERSAWATT



ABSOLUTE MAXIMUM RATINGS

		SGS				
		16DR05	16DR10	16DR15	16DR20	
V_{RRM}	Peak repetitive reverse voltage	50	100	150	200	V
V_{RWM}	Working peak reverse voltage	50	100	150	200	V
V_R	Continuous reverse voltage	50	100	150	200	V
I_{FRM}	Repetitive peak forward current (t = 10μs)	120				A
$I_{F(AV)}$	Average forward current T_{case} = 70°C (switching operation, δ = 0.5)	16				A
I_{FSM}	Surge non repetitive forward current (t = 10ms)	100				A
P_{tot}	Total dissipation at T_{case} = 70°C	70				W
T_{stg}	Storage temperature	−65 to 150				°C
T_j	Max. operating junction temperature	150				°C

Fig. 4 Recovery time and peak reverse current vs. I_F

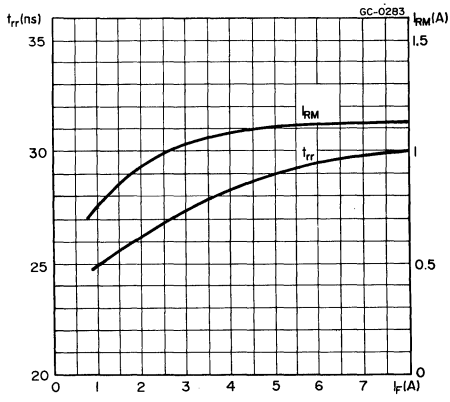


Fig. 5 Recovered time vs. di_F/dt

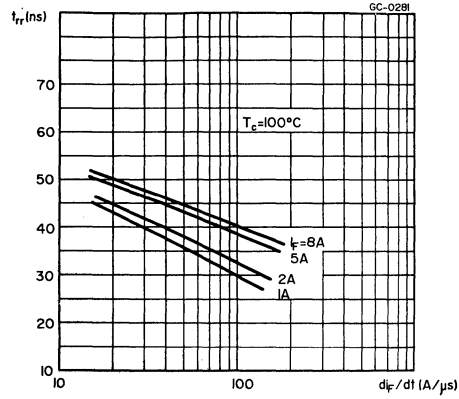


Fig. 6 Recovery charge vs. di_F/dt

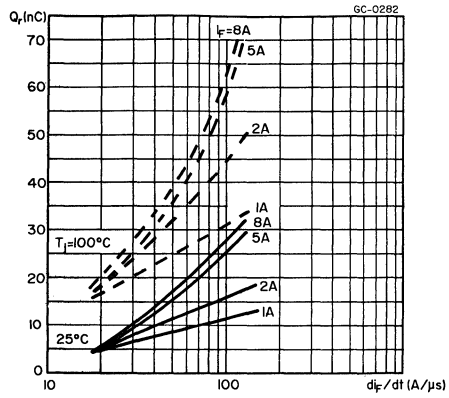
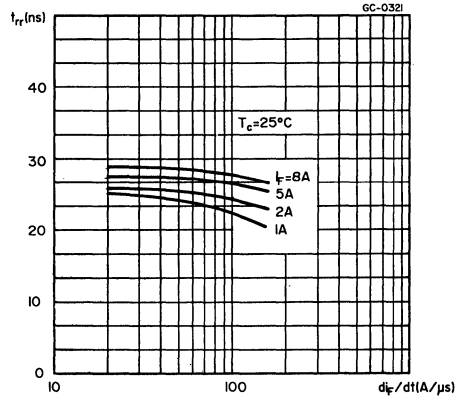


Fig. 7 Recovery time vs. di_F/dt



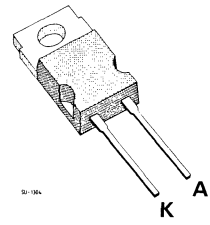
SGS20R05
SGS20R10
SGS20R15
SGS20R20

ADVANCE DATA

HIGH SPEED SWITCHING APPLICATIONS SECONDARY RECTIFICATION

- VOLTAGE RANGE: 50V→200V
- AVERAGE CURRENT: 20A
- VERY LOW REVERSE RECOVERY TIME: t_{rr} 35ns
- VERY LOW SWITCHING LOSSES
- LOW NOISE TURN-OFF SWITCHING

Typical applications include secondary rectification in high frequency switching power supplies and freewheel diodes in stepper motor control systems.



DO-220
DIOWATT1

ABSOLUTE MAXIMUM RATINGS

		SGS				
		20R05	20R10	20R15	20R20	
V_{RRM}	Peak repetitive reverse voltage	50	100	150	200	V
V_{RWM}	Working peak reverse voltage	50	100	150	200	V
V_R	Continuous reverse voltage	50	100	150	200	V
I_{FRM}	Repetitive peak forward current (t = 10μs)	250				A
$I_{F(AV)}$	Average forward current T_{case} = 70°C (switching operation, δ = 0.5)	20				A
I_{FSM}	Surge non repetitive forward current (t = 10ms)	200				A
P_{tot}	Total dissipation at T_{case} = 70°C	60				W
T_{stg}	Storage temperature	−65 to 150				°C
T_j	Max. operating junction temperature	150				°C

SGS25DB070D
SGS25DB080D

TRANSPACK NPN POWER DARLINGTON MODULE

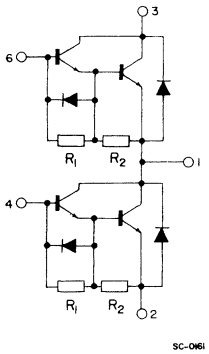
APPLICATIONS: The SGS25DB070D and SGS25DB080D are silicon NPN power fast darlingtons in half bridge configuration for industrial switching applications with three-phase mains operation.

ISOLATED POWER MODULE (24KVA-375W)	FAST FREEWHEEL DIODES

ABSOLUTE MAXIMUM RATINGS

		SGS25DB070D	SGS25DB080D	
V_{CBO}	Collector-base voltage ($I_E = 0$)	1000	1200	V
V_{CES}	Collector-emitter voltage ($V_{BE} = 0$)	1000	1200	V
V_{CEX}	Collector-emitter voltage ($V_{BE} = -1.5V$)	1000	1200	V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	700	800	V
V_{CEOL}	Overload switch-off at 1.5 times $I_{C\,(sat)}$*	650		
V_{EBO}	Emitter-base voltage ($I_C = 0$)	7		V
I_C	Collector current	37		A
I_{CM}	Collector peak current (t_p<10 ms)	80		A
I_{CP}	Collector peak current non repetitive (t_p<20 μs)	150		A
I_B	Base current	9		A
I_{BP}	Base peak current non repetitive (t_p<20 μs)	30		A
T_{stg}	Storage temperature	− 40 to 150		°C
T_j	Max. operating junction temperature (continuous)	150		°C
T_j	Max. operating junction temperature (1 minute)	175		°C

INTERNAL SCHEMATIC DIAGRAM

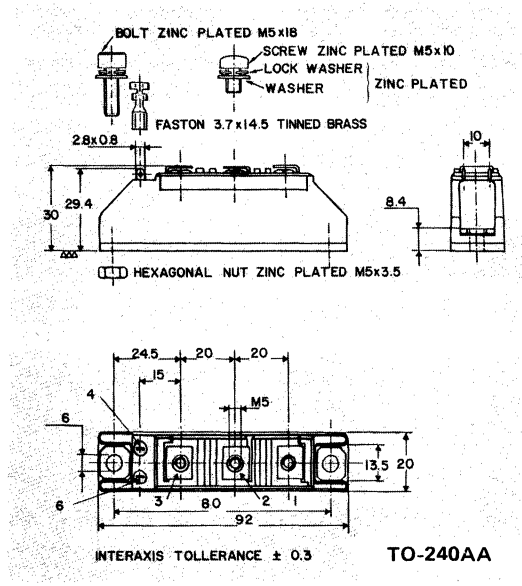


R_1 typ 10 Ω

R_2 typ 50 Ω

MECHANICAL DATA

Dimensions in mm



TO-240AA

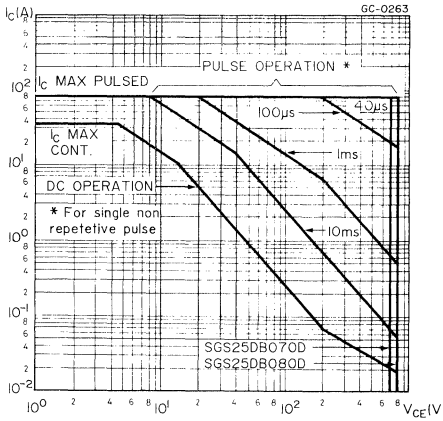
ELECTRICAL CHARACTERISTICS (Continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_f	Diode forward voltage	I_f = 25 A I_f = 25 A T_j = 125 °C		1.4 1.4	2	V V
t_{rr}	Diode reverse recovery time	I_f = 25 A di/dt = 100A/µs		0.2	0.5	µs
I_{rrm}	Diode reverse recovery time			12		A
I_{frm}	Diode forward current	t = 1ms	200			A

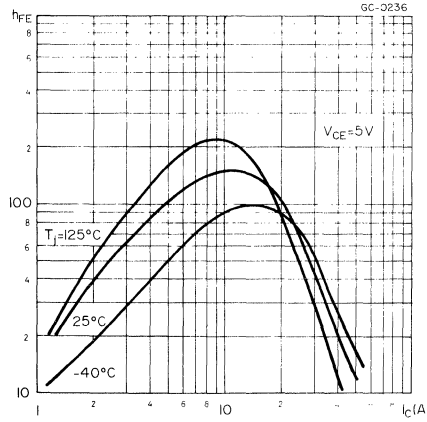
INSULATION TESTING

The insulation between the live parts and the base plate of TO-240 is tested before delivery for one second at 2500 V a.c.
If this test is repeated by the user either as a goods inwards check or as a test of the final equipment, in accordance with IEC Publication 146 (1973), clause 492.1 or DIN 57558 part 1/VDE 0558 part 1/8.77, section 5.7.9., only a voltage slowly increasing up to the above value should be used. If the voltage is applied for one minute as recommended by the above standards then the specified value of 2000 V should be taken.
During the test all electrical terminals including the drive terminals must be connected with each other in order to avoid damage by inductively or capacitively induced voltage transients. The test voltage is applied between the connected terminals and the base plate.

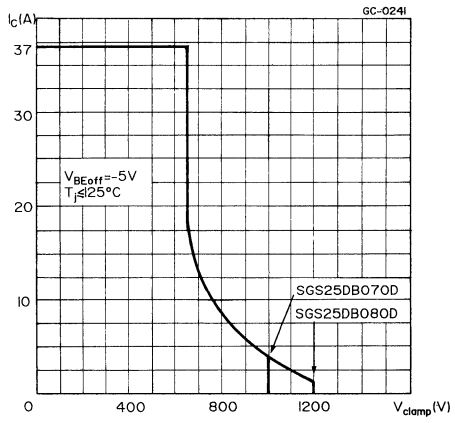
Safe operating areas for each section



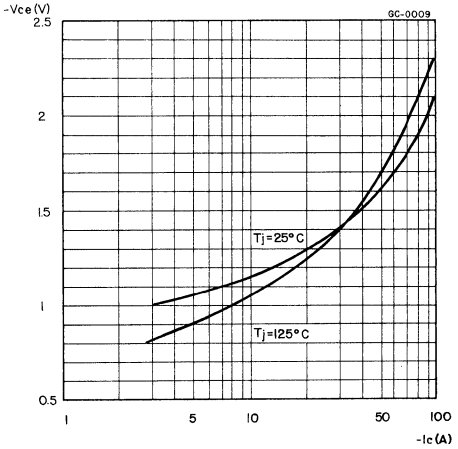
DC current gain



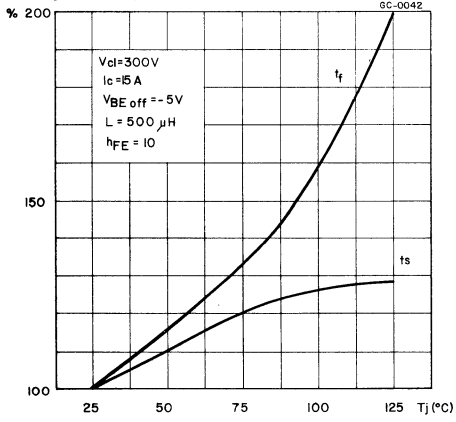
Reverse biased SOA (see fig. 2)



Typical V_F versus $-I_C$



Switching times inductive load vs junc temp



Switching times inductive load (see fig. 3)

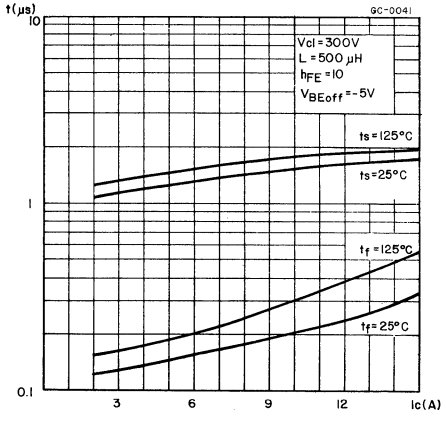
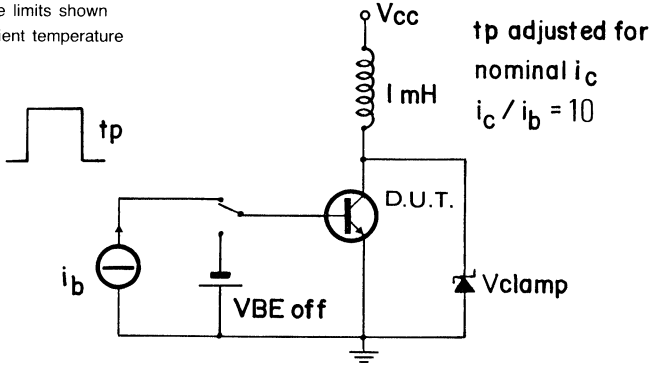


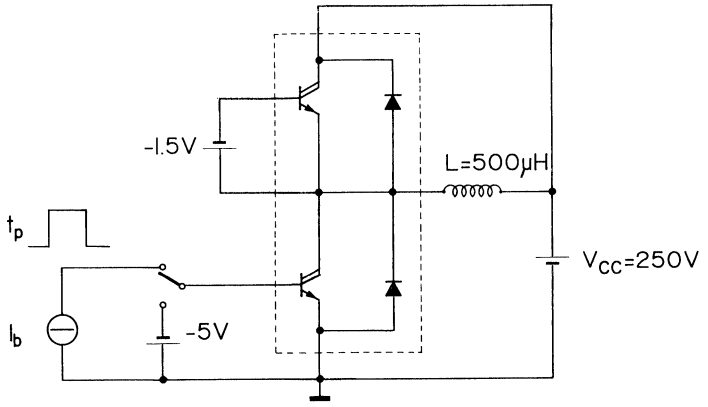
Fig. 2 RBSOA TEST CIRCUIT

RBSOA test circuit has been driven by the switching times test circuit with $R_{B2} = O$.
RBSOA sensitivity to T_j variations is very limited, so that the limits shown can be kept valid at ambient temperature as well.



SC-0002

Fig. 3 Switching times test circuit



SC-0160

SGS30DA060D
SGS30DA070D

TRANSPACK NPN POWER DARLINGTON MODULE

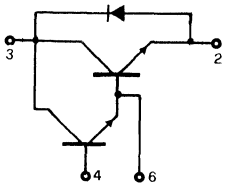
APPLICATIONS: These products are silicon NPN power darlingtons for industrial switching applications with three-phase mains operation.

ISOLATED POWER MODULE (30KVA - 375W)	FAST FREEWHEEL DIODE

ABSOLUTE MAXIMUM RATINGS

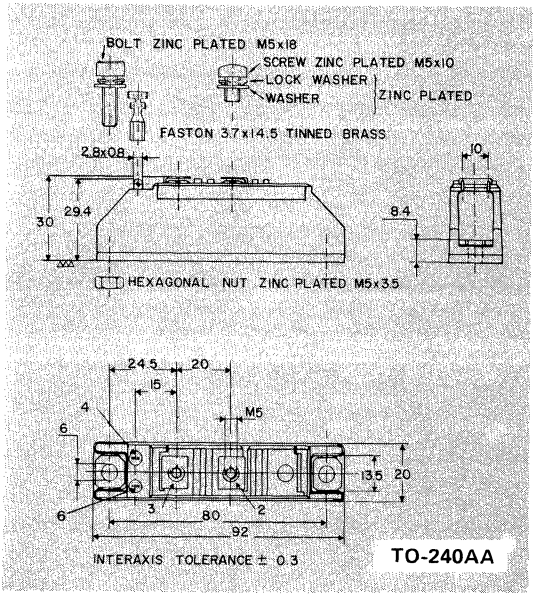
		SGS30DA060D	SGS30DA070D	
V_{CBO}	Collector-base voltage (I_E = 0)	1000	1200	V
V_{CES}	Collector-emitter voltage (V_{BE} = 0)	1000	1200	V
V_{CEX}	Collector-emitter voltage (V_{BE} = −1.5V)	1000	1200	V
V_{CEO}	Collector-emitter voltage (I_B = 0)	600	700	V
V_{CEOL}	Overload switch-off at 1.5 times $I_{C\ (sat)}$*	650		V
V_{EBO}	Emitter-base voltage (I_C = 0)	7		V
I_C	Collector current	45		A
I_{CM}	Collector peak current (t_p<10 ms)	120		A
I_{CP}	Collector peak current non repetitive (t_p<20 μs)	200		A
I_B	Base current	3		A
I_{BP}	Base peak current non repetitive (t_p<20 μs)	20		A
T_{stg}	Storage temperature	− 40 to 150		°C
T_j	Max. operating junction temperature (continuous)	150		°C
T_j	Max. operating junction temperature (1 minute)	175		°C

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



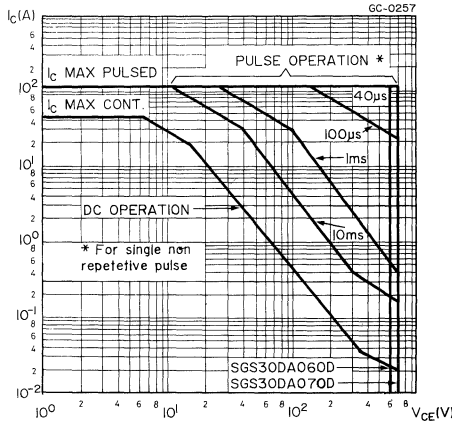
ELECTRICAL CHARACTERISTICS (Continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_f	Diode forward voltage	I_f = 30 A T_j = 25°C		1.4	2	V
		T_j = 125°C		1.4		V
t_{rr}	Diode reverse recovery time	I_f = 30 A di/dt = 100A/µs		0.2	0.5	µs
I_{rm}	Diode reverse recovery current			10		A
I_{frm}	Diode forward current	t = 1ms	200			A

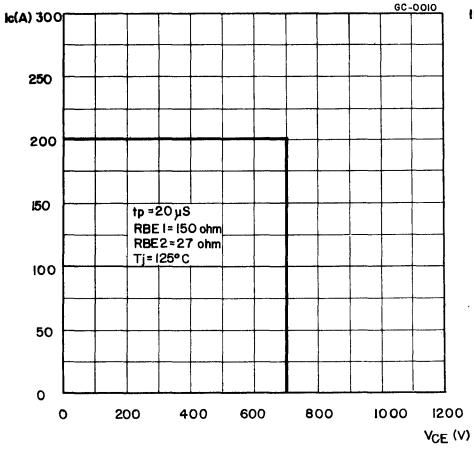
INSULATION TESTING

The insulation between the live parts and the base plate of TO-240 is tested before delivery for one second at 2500 V a.c.
If this test is repeated by the user either as a goods inwards check or as a test of the final equipment, in accordance with IEC Publication 146 (1973), clause 492.1 or DIN 57558 part 1/VDE 0558, section 5.7.9., only a voltage slowly increasing up to the above value should be used. If the voltage is applied for one minute as recommended by the above standards then the specified value of 2000 V should be taken.
During the test all electrical terminals including the drive terminals must be connected with each other in order to avoid damage by inductively or capacitively induced voltage transients. The test voltage is applied between the connected terminals and the base plate.

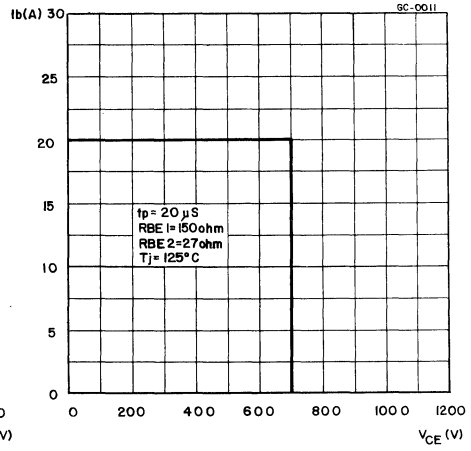
Safe operating areas



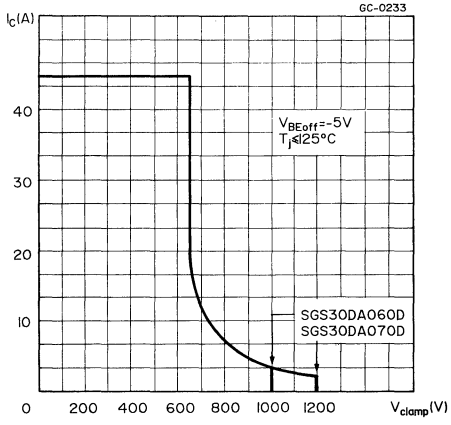
Collector overload SOA (see fig. 1)



Base overload SOA (see fig. 1)



Reverse biased SOA (see fig. 2)



Switching times inductive load (see fig. 3)

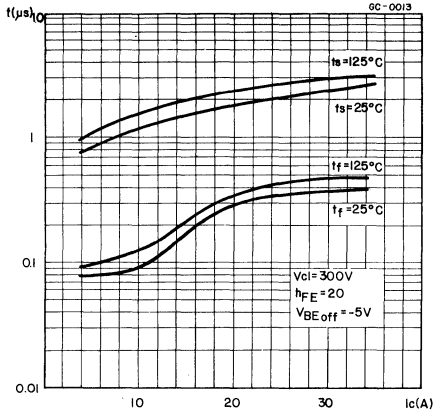
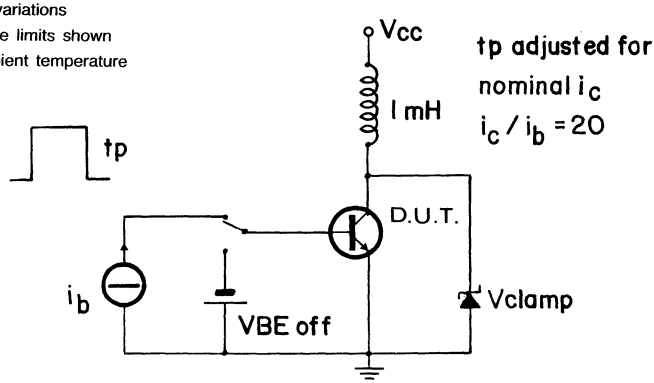


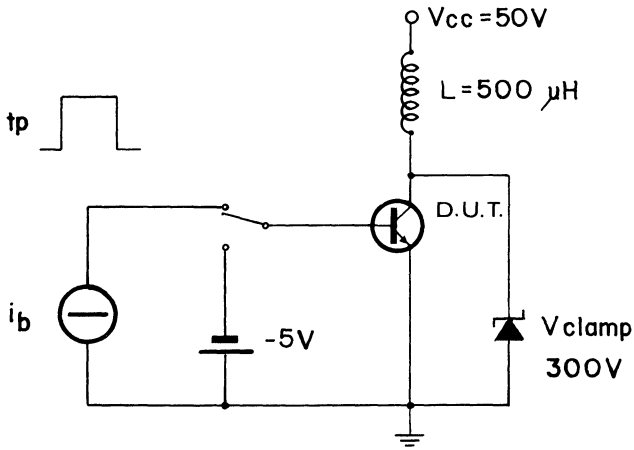
Fig. 2 RBSOA TEST CIRCUIT

RBSOA test circuit has been driven by the switching times test circuit with $R_{B2} = O$.
RBSOA sensitivity to T_j variations is very limited, so that the limits shown can be kept valid at ambient temperature as well.



SC-0002

Fig. 3 Switching times test circuit.



SC-0003

SGS30DB040D
SGS30DB045D

TRANSPACK NPN POWER DARLINGTON MODULE

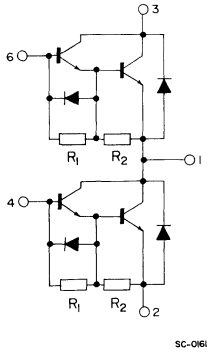
APPLICATIONS: These products are silicon NPN power fast darlingtons in half bridge configuration for industrial switching applications from the mains.

ISOLATED POWER MODULE (15KVA - 375W)	FAST FREEWHEEL DIODES

ABSOLUTE MAXIMUM RATINGS

		SGS30DB040D	SGS30DB045D	
V_{CBO}	Collector-base voltage (I_E = 0)	500	600	V
V_{CES}	Collector-emitter voltage (V_{BE} = 0)	500	600	V
V_{CEX}	Collector-emitter voltage (V_{BE} = −1.5V)	500	600	V
V_{CEO}	Collector-emitter voltage (I_B = 0)	400	450	V
V_{CEOL}	Overload switch-off at 1.5 times $I_{C\ (sat)}$*	400		V
V_{EBO}	Emitter-base voltage (I_C = 0)	7		V
I_C	Collector current	45		A
I_{CM}	Collector peak current (t_p<10 ms)	60		A
I_{CP}	Collector peak current non repetitive (t_p<20 μs)	200		A
I_B	Base current	6		A
I_{BP}	Base peak current non repetitive (t_p<20 μs)	10		A
T_{stg}	Storage temperature	− 40 to 150		°C
T_j	Max. operating junction temperature (continuous)	150		°C
T_j	Max. operating junction temperature (1 minute)	175		°C

INTERNAL SCHEMATIC DIAGRAM

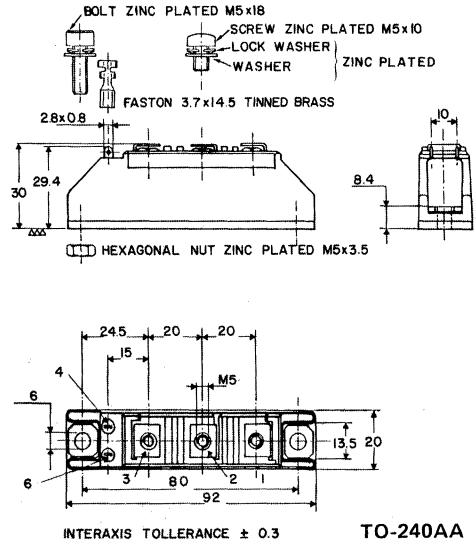


R_1 typ. 80 Ω

R_2 typ. 150 Ω

MECHANICAL DATA

Dimensions in mm



TO-240AA

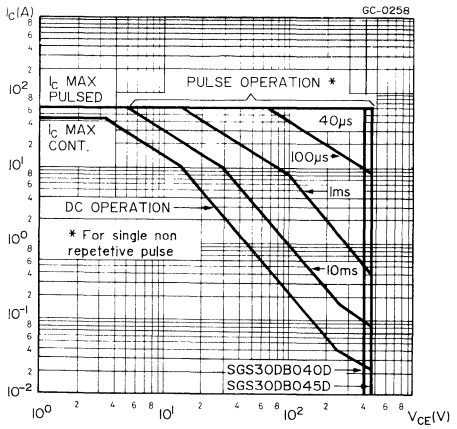
ELECTRICAL CHARACTERISTICS (Continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_f	Diode forward voltage	I_f = 30 A T_j = 25°C		1.30	2.0	V
		T_j = 125°C		1.20		V
t_{rr}	Diode reverse recovery time	I_f = 30 A di/dt = 100A/µs		0.20	0.5	µs
I_{rm}	Diode reverse recovery current			10		A
I_{frm}	Diode forward current	t = 1ms	250			A

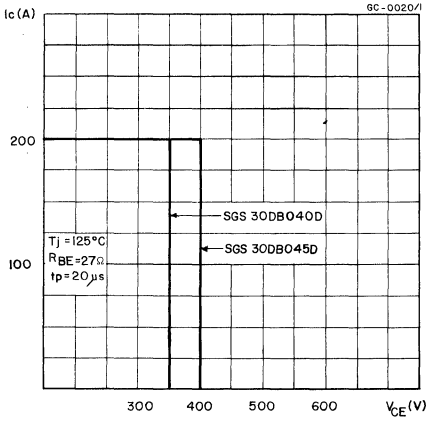
INSULATION TESTING

The insulation between the live parts and the base plate of TO-240 is tested before delivery for one second at 2500 V a.c.
If this test is repeated by the user either as a goods inwards check or as a test of the final equipment, in accordance with IEC Publication 146 (1973), clause 492.1 or DIN 57558 part 1/8.77, section 5.7.9 , only a voltage slowly increasing up to the above value should be used. If the voltage is applied for one minute as recommended by the above standards then the specified value of 2000 V should be taken.
During the test all electrical terminals including the drive terminals must be connected with each other in order to avoid damage by inductively or capacitively induced voltage transients. The test voltage is applied between the connected terminals and the base plate.

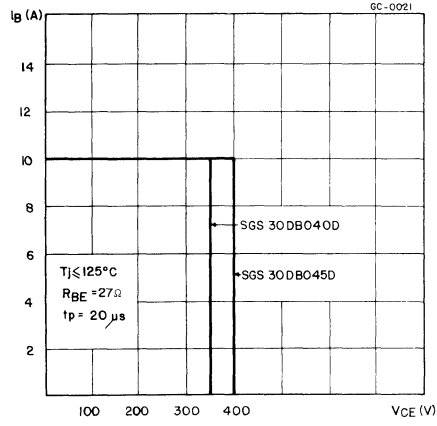
Safe operating areas for each section



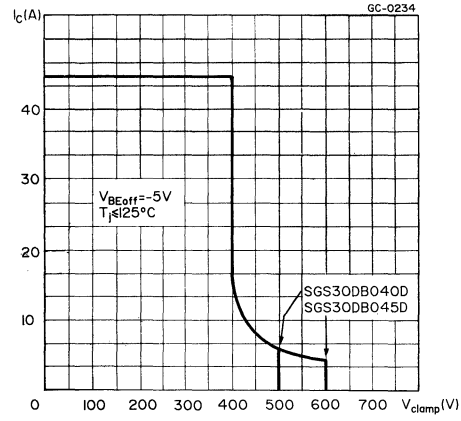
Collector overload SOA (see fig. 1)



Base overload SOA (see fig. 1)



Reverse biased SOA (see fig. 2)



Switching times inductive load (see fig. 3)

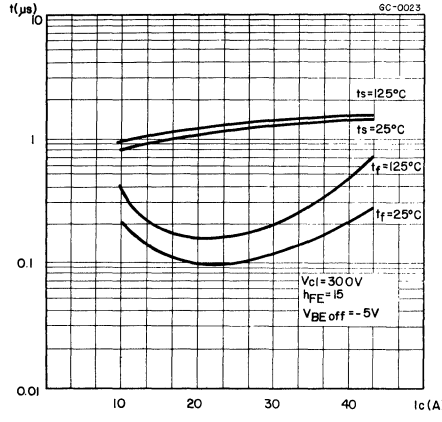


Fig. 2 RBSOA TEST CIRCUIT

RBSOA test circuit has been driven by the switching times test circuit with R_{B2} = O.
RBSOA sensitivity to T_j variations is very limited, so that the limits shown can be kept valid at ambient temperature as well.

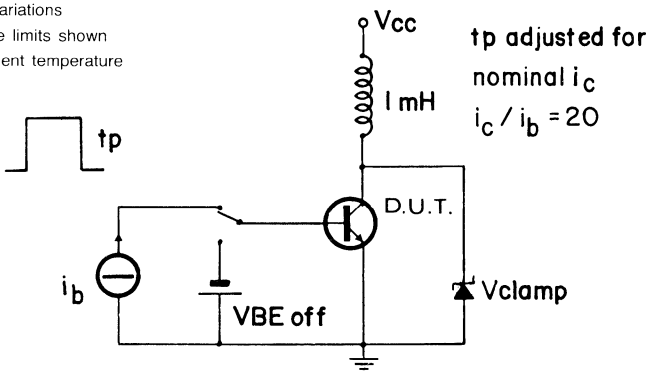
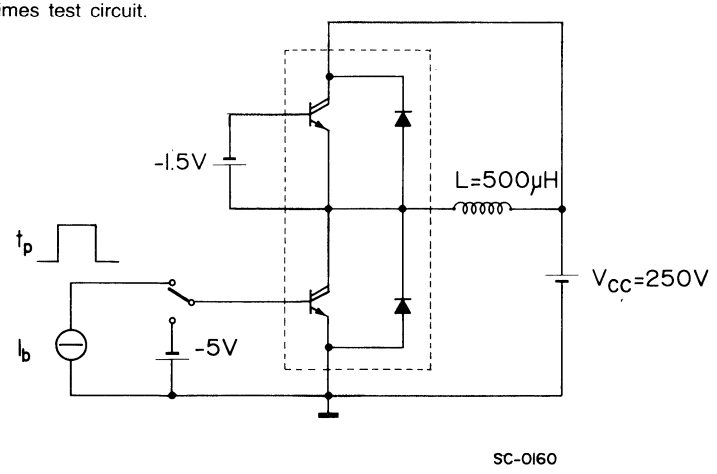


Fig. 3 Switching times test circuit.



SGS30MA050D1

ADVANCE DATA

TRANSPACK N-CHANNEL POWER MOS MODULE

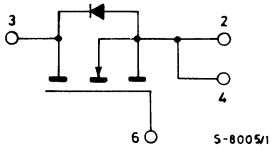
APPLICATIONS: The SGS30MA050D1 is a N-Channel POWER MOS MODULE for industrial applications (quarter bridge configuration).

ISOLATED POWER MODULE (15KVA - 375W)	INTERNAL FREEWHEEL DIODE

ABSOLUTE MAXIMUM RATINGS

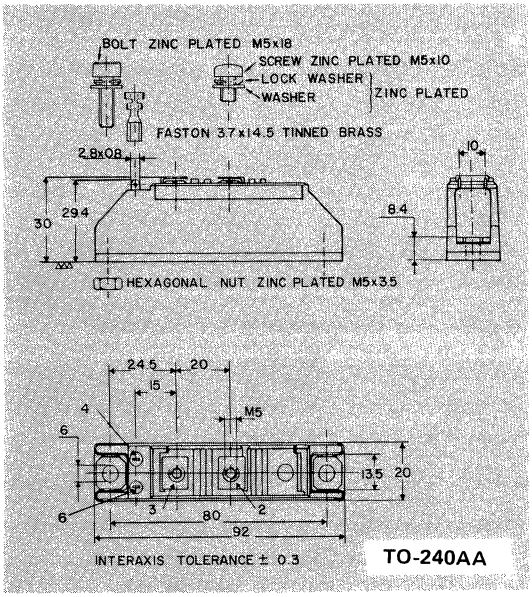
		SGS30MA050D1	
V_{DS}	Drain-source voltage (V_{GS} = 0)	500	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	500	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) T_C = 25 °C	30	A
I_{DM}	Drain current (t_p < 10 ms, repetitive)	45	A
I_{DLM}	Drain current (t_p = 20μs, not repetitive)	75	A
P_{tot}	Total dissipation at T_C < 25 °C	300	W
	Derating factor	3	W/°C
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature (continuous)	150	°C
T_j	Max. operating junction temperature (1 minute)	175	°C

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



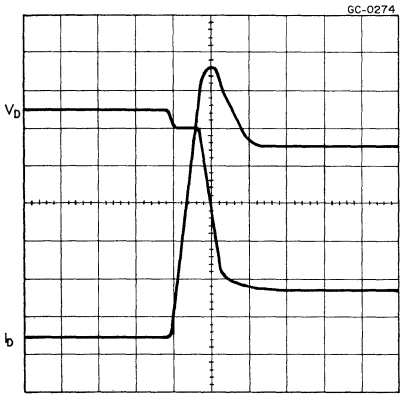
This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

ELECTRICAL CHARACTERISTICS (Continued)

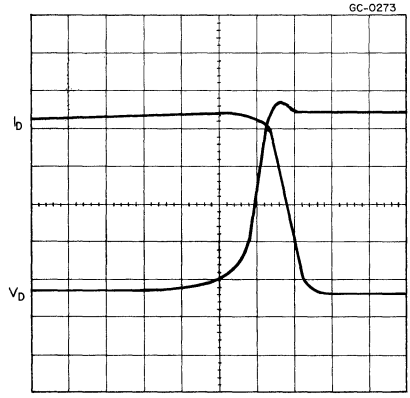
Parameter		Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE (see note B)						
I_{SD}	Source-drain current (continuous)				30	A
I_{SDM}	Source-drain current (pulsed)				45	A
V_{SD}	Forward on voltage	I_{SD} = 30 A V_{GS} = 0			2	V
t_{rr}	Reverse recovery time	I_{SD} = 30 A V_{GS} = 0 di/dt = 150 A/µs		600		ns

Note A: switching times inductive load have been tested by the circuit shown in fig. 1 (by paralleling the load with SGS fast recovery diode...).
Typical waveforms obtained for V_D and I_D are schematically shown here below.

I_D-V_D at turn-on



I_D-V_D at turn-off



Note that di/dt does not depend on the perfomances of the freewheeling diode, but on the D.U.T. and its drive circuit only.

SGS35MA050D1

ADVANCE DATA

N-CHANNEL POWER MOS TRANSISTORS

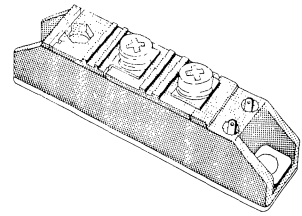
HIGH SPEED SWITCHING APPLICATIONS

V_{DSS}	$R_{DS\ (on)}$	I_D
500V	0.16Ω	35A

- ISOLATED POWERMOS MODULE
- HIGH POWER
- FAST SWITCHING
- EASY DRIVE
- EASY TO PARALLEL

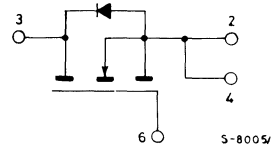
INDUSTRIAL APPLICATION:

- SWITCHING MODE POWER SUPPLIES
- UNINTERRUPTIBLE POWER SUPPLIES



TO-240AA

INTERNAL SCHEMATIC DIAGRAM



N-Channel enhancement mode POWERMOS field effect transistors. Easy drive and fast switching of these TRANSPACK modules make them ideal for high power, high speed switching applications.
Typical applications include DC motor control (speed, soft start and torque), AC motor control (variable frequency control) switching mode power supplies, uninterruptible power supplies, DC/DC convertors and high frequency welding equipment.
The large RBSOA and absence of second breakdown in POWERMOS make these TRANSPACK modules very rugged. This, together with the isolated package with its optimised thermal performance, make these modules extremely effective in high power application.

ABSOLUTE MAXIMUM RATINGS

		SGS30MA050D1	
V_{DS}	Drain-source voltage (V_{GS} = 0)	500	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	500	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) T_c = 25°C	35	A
I_{DM}	Drain current ($t_p \leqslant 10$ ms, repetitive)	50	A
I_{DLM}	Drain current, ($t_p = 20\mu s$, not repetitive)	80	A
P_{tot}	Total dissipation at $T_{case} < 25°C$	400	W
	Derating factor	3.2	W/°C
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature (continuous)	150	°C

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

ELECTRICAL CHARACTERISTICS (continued)

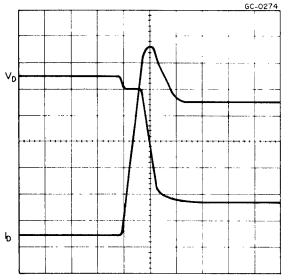
Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SOURCE DRAIN DIODE (see note B)						
I_{SD}	Source-Drain current (continuous)				35	A
I_{SDM}	Source-Drain current (pulsed)				50	A
V_{SD}	Forward on voltage	I_{SD} = 35A V_{GS} = 0			2	V
t_{rr}	Reverse recovery time	di/dt = 150A/μs I_{SD} = 30A V_{GS} = 0		600		ns

INSULATION TESTING

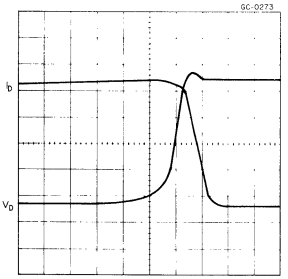
The insulation between the live parts and the base plate of TO-240 is tested before delivery for one second at 2500 V a.c.
If this test is repeated by the user either as a good inwards check or as a test of the final equipment, in accordance with IEC Publication 146 (1973), clause 492.1 or DIN 57558 part 1/VDE 0558, part 1/8.77, section 5.7.9., only a voltage slowly increasing up to the above standards then the specified value of 2000 V should be taken.
During the test all electrical terminals including the drive terminals must be connected with each other in order to avoid damage by inductively or capacitively induced voltage transients. The test voltage is applied between the connected terminals and the base plate.

Note A: switching times inductive load have been tested by the circuit shown in fig. 1 (by paralleling the load with SGS fast recovery diode SGS45R80).
Typical waveforms obtained for V_D and I_D are schematically shown here below.

I_D-V_D af turn-on



I_D-V_D af turn-off



Note that di/dt does not depend on the performances of the freewheeling diode, but on the D.U.T. and its drive circuit only.

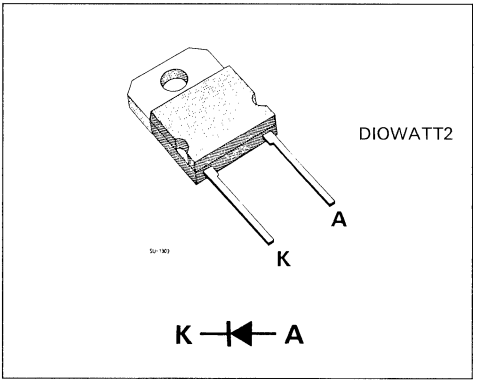
SGS35R120

ADVANCE DATA

HIGH SPEED SWITCHING APPLICATIONS

- VOLTAGE RANGE: 1200V
- AVERAGE CURRENT: 35A
- VERY LOW REVERSE RECOVERY TIME: t_{rr} 150ns
- VERY LOW SWITCHING LOSSES
- LOW NOISE TURN-OFF SWITCHING

Typical applications include freewheel diodes in motor control systems.



ABSOLUTE MAXIMUM RATINGS

V_{RRM}	Peak repetitive reverse voltage	1200	V
V_{RWM}	Working peak reverse voltage	1200	V
V_R	Continuous reverse voltage	1200	V
I_{FRM}	Repetitive peak forward current (t = 10μs)	500	A
$I_{F(AV)}$	Average forward current T_{case} = 70°C (switching operation, δ = 0.5)	35	A
I_{FSM}	Surge non repetitive forward current (t = 10ms)	350	A
P_{tot}	Total dissipation at T_{case} = 70°C	90	W
T_{stg}	Storage temperature	– 65 to 150	°C
T_j	Max. operating junction temperature	150	°C

SGS40TA045
SGS40TA045D

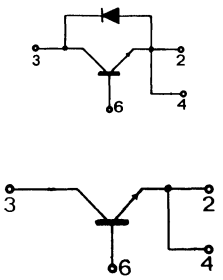
TRANSPACK NPN POWER TRANSISTOR MODULE

APPLICATIONS: These products are silicon NPN power transistors for industrial switching applications from the mains.

ISOLATED POWER MODULE (30KVA - 375W)	FAST FREEWHEEL DIODE (D - suffix)

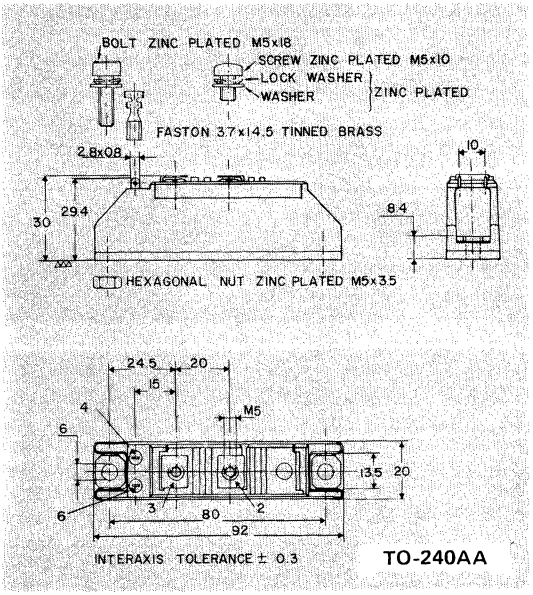
ABSOLUTE MAXIMUM RATINGS		SGS40TA045	SGS40TA045D	
V_{CBO}	Collector-base voltage (I_E = 0)	850		V
V_{CES}	Collector-emitter voltage (V_{BE} = 0)	850		V
V_{CEX}	Collector-emitter voltage (V_{BE} = −1.5V)	850		V
V_{CEO}	Collector-emitter voltage (I_B = 0)	450		V
V_{CEOL}	Overload switch-off at 1.5 times $I_{C\ (sat)}$*	500		V
V_{EBO}	Emitter-base voltage (I_C = 0)	7		V
I_C	Collector current	60		A
I_{CM}	Collector peak current (t_p<10 ms)	120		A
I_{CP}	Collector peak current non repetitive(t_p<20 μs)	300		A
I_B	Base current	12		A
I_{BP}	Base peak current non repetitive (t_p<20 μs)	50		A
T_{stg}	Storage temperature	− 40 to 150		°C
T_j	Max. operating junction temperature (continuous)	150		°C
T_j	Max. operating junction temperature (1 minute)	175		°C

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



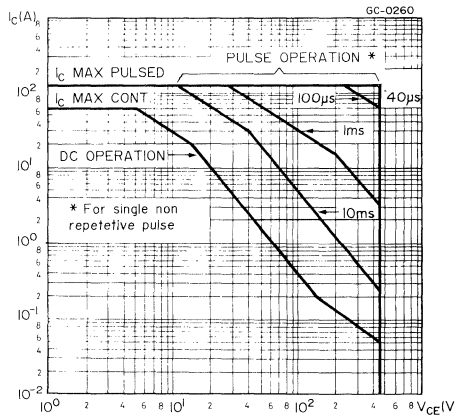
ELECTRICAL CHARACTERISTICS (Continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_f	Diode forward voltage	I_f = 40 A T_j = 25°C **for SGS40TA045D**		1.50	2.0	V
		T_j = 125°C		1.55		V
t_{rr}	Diode reverse recovery time	I_f = 40 A		0.20	0.5	µs
		di/dt = 100A/µs **for SGS40TA045D**				
I_{rm}	Diode reverse recovery current			10		A
I_{frm}	Diode forward current	t = 1ms **for SGS40TA045D**	250			A

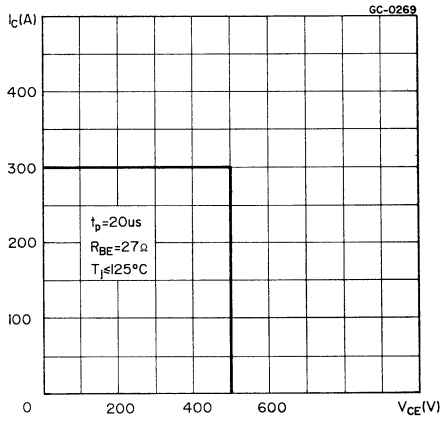
INSULATION TESTING

The insulation between the live parts and the base plate of TO-240 is tested before delivery for one second at 2500 V a.c.
If this test is repeated by the user either as a goods inwards check or as a test of the final equipment, in accordance with IEC Publication 146 (1973), clause 492.1 or DIN 57558 part 1/VDE 0558, section 5.7.9., only a voltage slowly increasing up to the above value should be used. If the voltage is applied for one minute as recommended by the above standards then the specified value of 2000 V should be taken.
During the test all electrical terminals including the drive terminals must be connected with each other in order to avoid damage by inductively or capacitively induced voltage transients. The test voltage is applied between the connected terminals and the base plate.

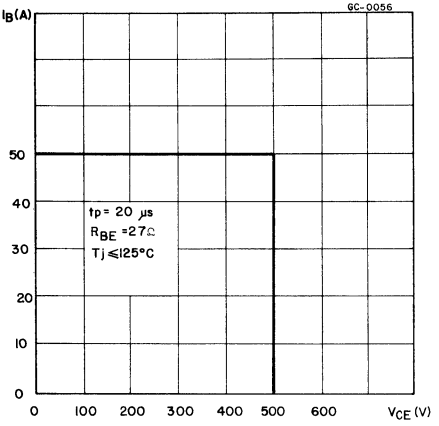
Safe operating areas



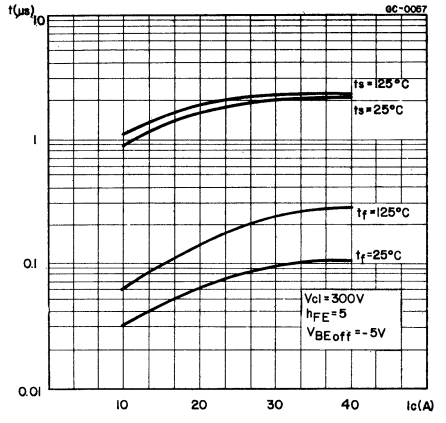
Collector overload SOA (see fig. 1)



Base overload SOA (see fig. 1)



Switching times inductive load (see fig. 3)



Switching times inductive load vs junc. temp.

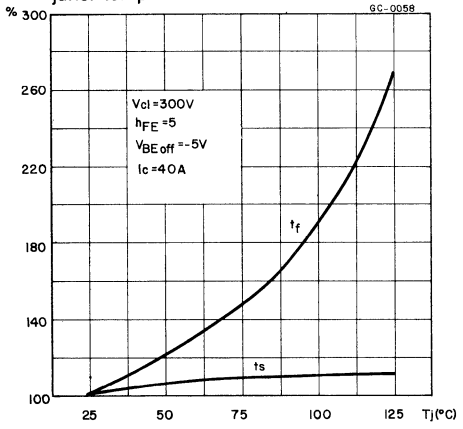
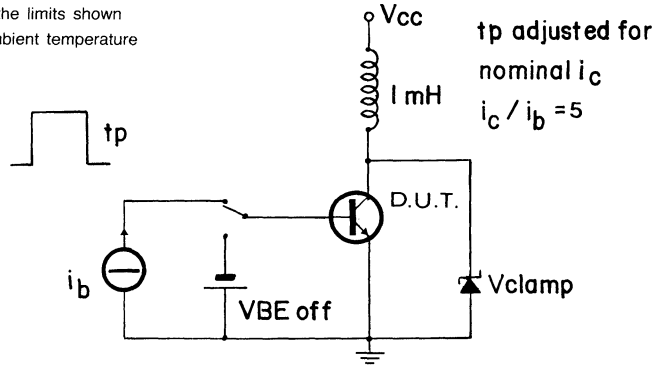


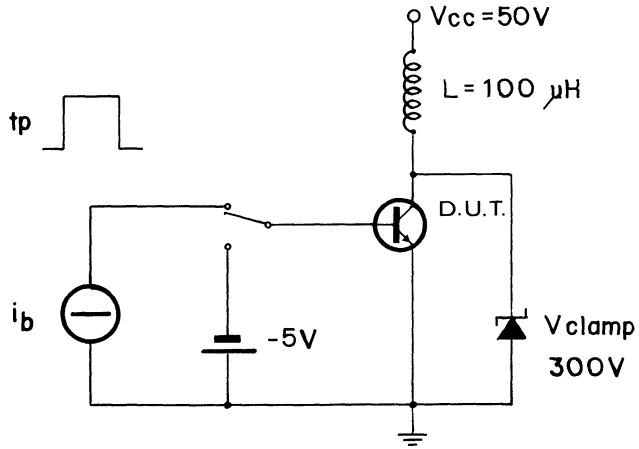
Fig. 2 RBSOA TEST CIRCUIT

RBSOA test circuit has been driven by the switching times test circuit with $R_{B2} = O$.
RBSOA sensitivity to T_j variations is very limited, so that the limits shown can be kept valid at ambient temperature as well.



SC-0002

Fig. 3 Switching times test circuit.



SC-0003

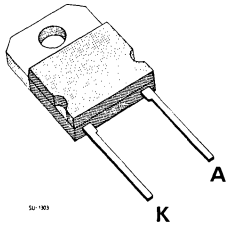
SGS45R80

ADVANCE DATA

HIGH SPEED SWITCHING APPLICATIONS

- VOLTAGE RANGE: 800V
- AVERAGE CURRENT: 45A
- VERY LOW REVERSE RECOVERY TIME: t_{rr} 125ns
- VERY LOW SWITCHING LOSSES
- LOW NOISE TURN-OFF SWITCHING

Typical applications include freewheel diodes in motor control systems.



DIOWATT2

ABSOLUTE MAXIMUM RATINGS

V_{RRM}	Peak repetitive reverse voltage	800	V
V_{RWM}	Working peak reverse voltage	800	V
V_R	Continuous reverse voltage	800	V
I_{FRM}	Repetitive peak forward current ($t = 10\mu s$)	600	A
$I_{F(AV)}$	Average forward current $T_{case} = 70°C$ (switching operation, $\delta = 0.5$)	45	A
I_{FSM}	Surge non repetitive forward current ($t = 10ms$)	450	A
P_{tot}	Total dissipation at $T_{case} = 70°C$	90	W
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C

SGS50DA045D

TRANSPACK NPN POWER DARLINGTON MODULE

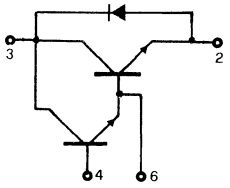
APPLICATIONS: The product is a silicon NPN power darlington for industrial switching applications from the mains.

ISOLATED POWER MODULE (37KVA - 375W)	FAST FREEWHEEL DIODE

ABSOLUTE MAXIMUM RATINGS

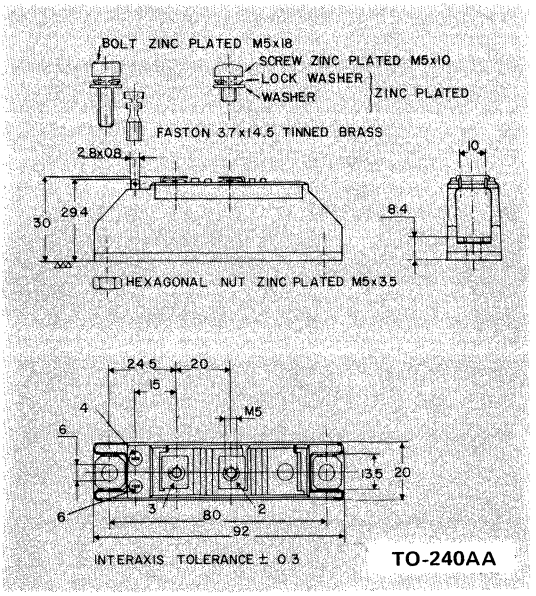
		SGS50DA045D	
V_{CBO}	Collector-base voltage (I_E = 0)	850	V
V_{CES}	Collector-emitter voltage (V_{BE} = 0)	850	V
V_{CEX}	Collector-emitter voltage (V_{BE} = −1.5V)	850	V
V_{CEO}	Collector-emitter voltage (I_B = 0)	450	V
V_{CEOL}	Overload switch-off at 1.5 times $I_{C\ (sat)}$*	500	V
V_{EBO}	Emitter-base voltage (I_C = 0)	7	V
I_C	Collector current	75	A
I_{CM}	Collector peak current (t_p<10 ms)	120	A
I_{CP}	Collector peak current non repetitive (t_p<20 μs)	300	A
I_B	Base current	3	A
I_{BP}	Base peak current non repetitive (t_p<20 μs)	10	A
T_{stg}	Storage temperature	− 40 to 150	°C
T_j	Max. operating junction temperature (continuous)	150	°C
T_j	Max. operating junction temperature (1 minute)	175	°C

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



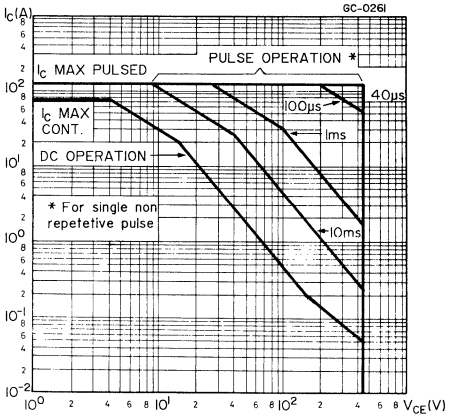
ELECTRICAL CHARACTERISTICS (Continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_f	Diode forward voltage	I_f = 50 A T_j = 25°C		1.60	2.2	V
		T_j = 125°C		1.70		V
t_{rr}	Diode reverse recovery time	I_f = 50 A di/dt = 100A/μs		0.20	0.5	μs
I_{rm}	Diode reverse recovery current			12		A
I_{frm}	Diode forward current	t = 1ms	250			A

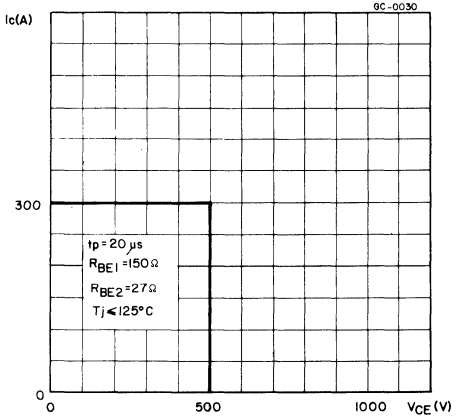
INSULATION TESTING

The insulation between the live parts and the base plate of TO-240 is tested before delivery for one second at 2500 V a.c.
If this test is repeated by the user either as a goods inwards check or as a test of the final equipment, in accordance with IEC Publication 146 (1973), clause 492.1 or DIN 57558 part 1/VDE 0558, part 1/8.77, section 5.7.9., only a voltage slowly increasing up to the above value should be used. If the voltage is applied for one minute as recommended by the above standards then the specified value of 2000 V should be taken.
During the test all electrical terminals including the drive terminals must be connected with each other in order to avoid damage by inductively or capacitively induced voltage transients. The test voltage is applied between the connected terminals and the base plate.

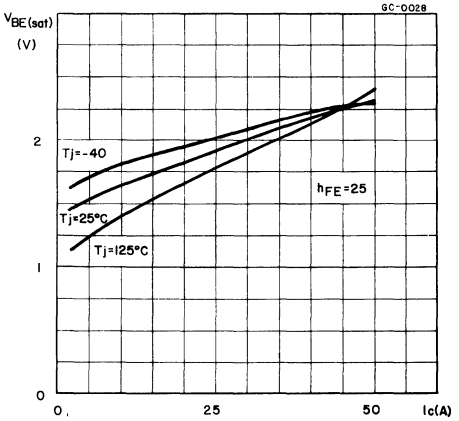
Safe operating areas



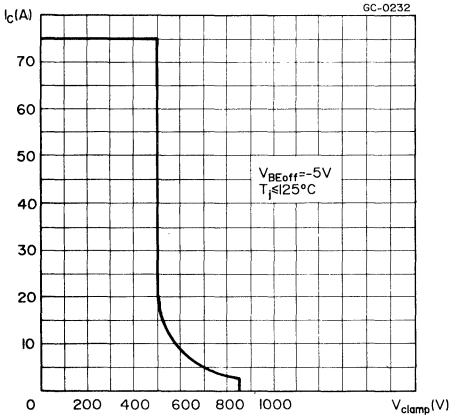
Collector overload SOA (see fig. 1)



Base-emitter saturation voltage



Reverse biased SOA (see fig. 2)



Switching times inductive load (see fig. 3)

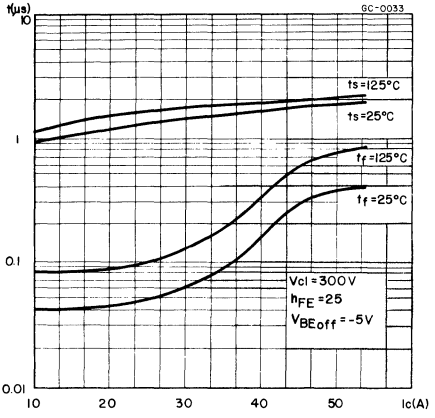


Fig. 2 RBSOA TEST CIRCUIT

RBSOA test circuit has been driven by the switching times test circuit with $R_{B2} = O$.
RBSOA sensitivity to T_j variations is very limited, so that the limits shown can be kept valid at ambient temperature as well.

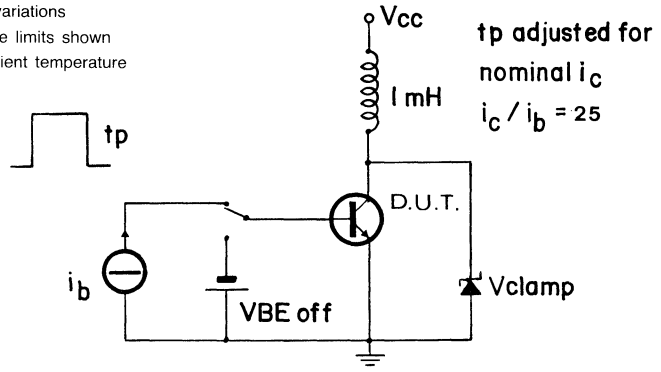
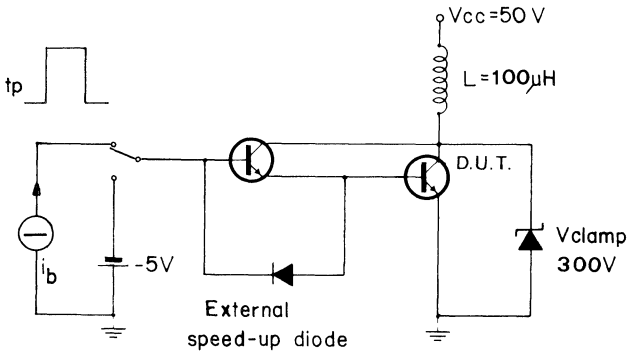


Fig. 3 Switching times test circuit.



SGS50DB040D
SGS50DB045D

TRANSPACK NPN POWER DARLINGTON MODULE

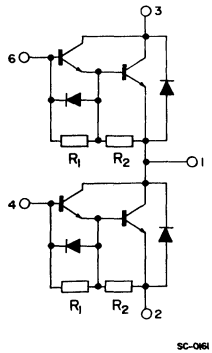
APPLICATIONS: The SGS50DB040D and SGS50DB045D are silicon NPN power fast darlingtons in half bridge configuration for industrial switching applications from the mains.

ISOLATED POWER MODULE (26KVA-375W)	FAST FREEWHEEL DIODES

ABSOLUTE MAXIMUM RATINGS

		SGS50DB040D	SGS50BD045D	
V_{CBO}	Collector-base voltage (I_E = 0)	500	600	V
V_{CES}	Collector-emitter voltage (V_{BE} = 0)	500	600	V
V_{CEX}	Collector-emitter voltage (V_{BE} = −1.5V)	500	600	V
V_{CEO}	Collector-emitter voltage (I_B = 0)	400	450	V
V_{CEOL}	Overload switch-off at 1.5 times $I_{C\ (sat)}$*	400		V
V_{EBO}	Emitter-base voltage (I_C = 0)	7		V
I_C	Collector current	75		A
I_{CM}	Collector peak current (t_p<10 ms)	120		A
I_{CP}	Collector peak current non repetitive (t_p<20 μs)	250		A
I_B	Base current	10		A
I_{BP}	Base peak current non repetitive (t_p<20 μs)	20		A
T_{stg}	Storage temperature	− 40 to 150		°C
T_j	Max. operating junction temperature (continuous)	150		°C
T_j	Max. operating junction temperature (1 minute)	175		°C

INTERNAL SCHEMATIC DIAGRAM

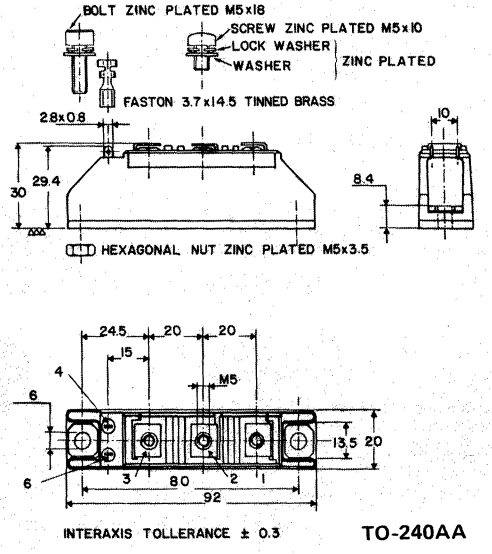


R_1 typ 80 Ω

R_2 typ 150 Ω

MECHANICAL DATA

Dimensions in mm



TO-240AA

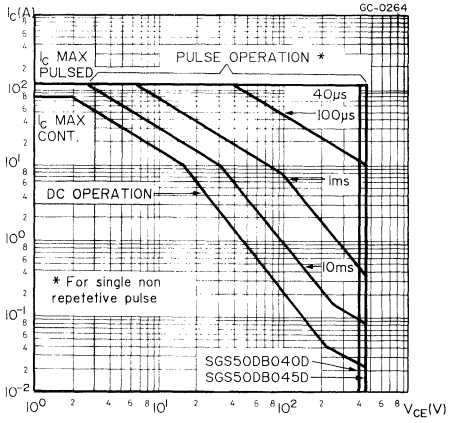
ELECTRICAL CHARACTERISTICS (Continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_f	Diode forward voltage	I_f = 50 A I_f = 50 A T_j = 125 °C		1.4 1.5	2	V V
t_{rr}	Diode reverse recovery time	I_f = 50 A di/dt = 100A/µs		0.2	0.5	µs
I_{rm}	Diode reverse recovery time			10		A
I_{frm}	Diode forward current	t = 1ms	250			A

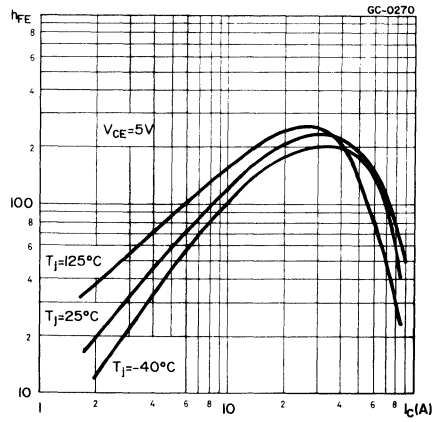
INSULATION TESTING

The insulation between the live parts and the base plate of TO-240 is tested before delivery for one second at 2500 V a.c.
If this test is repeated by the user either as a goods inwards check or as a test of the final equipment, in accordance with IEC Publication 146 (1973), clause 492.1 or DIN 57558 part 1/VDE 0558 part 1/8.77, section 5.7.9., only a voltage slowly increasing up to the above value should be used. If the voltage is applied for one minute as recommended by the above standards then the specified value of 2000 V should be taken.
During the test all electrical terminals including the drive terminals must be connected with each other in order to avoid damage by inductively or capacitively induced voltage transients. The test voltage is applied between the connected terminals and the base plate.

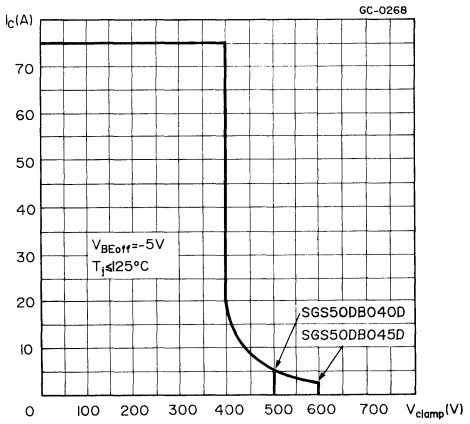
Safe operating areas for each section



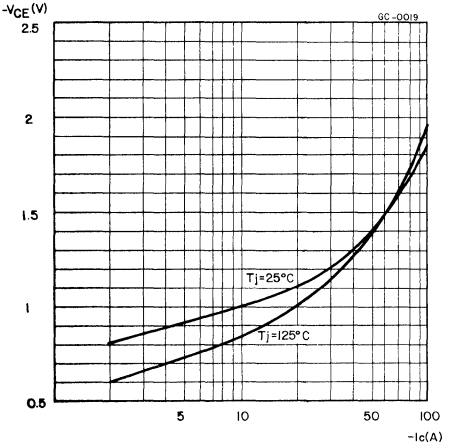
DC current gain



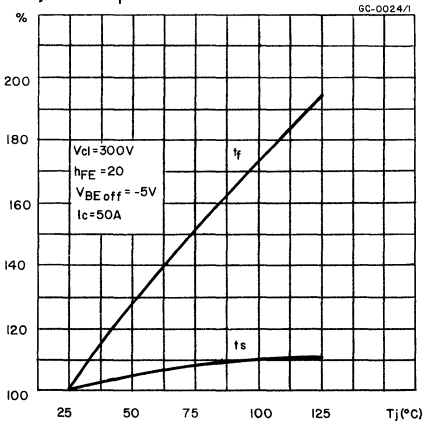
Reverse biased SOA (see fig. 2)



Typical V_F versus $-I_C$



Switching times inductive load vs junc temp



Switching times inductive load (see fig. 3)

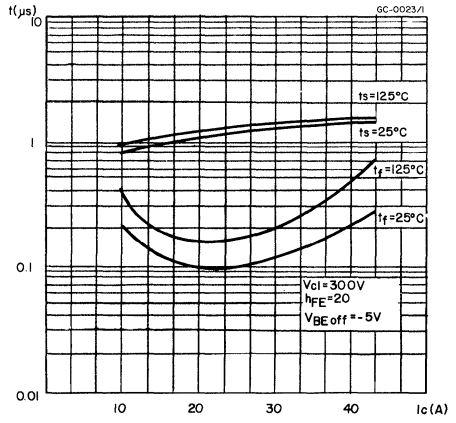
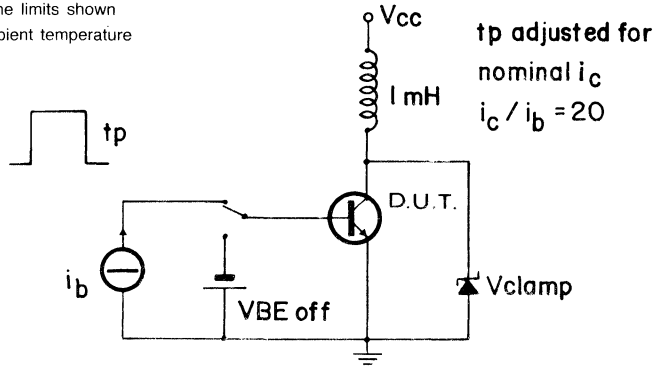


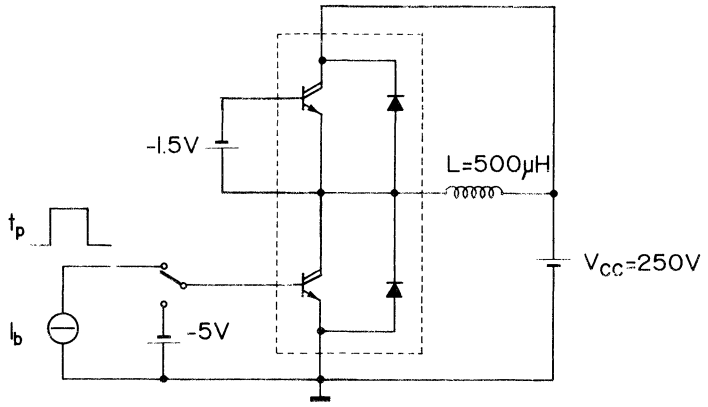
Fig. 2 RBSOA TEST CIRCUIT

RBSOA test circuit has been driven by the switching times test circuit with $R_{B2} = O$.
RBSOA sensitivity to T_j variations is very limited, so that the limits shown can be kept valid at ambient temperature as well.



SC-0002

Fig. 3 - Switching time test circuit



SC-0160

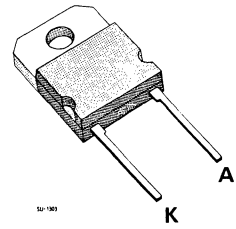
SGS60R40

ADVANCE DATA

HIGH SPEED SWITCHING APPLICATIONS

- VOLTAGE RANGE: 400V
- AVERAGE CURRENT: 60A
- VERY LOW REVERSE RECOVERY TIME: t_{rr} 125ns
- VERY LOW SWITCHING LOSSES
- LOW NOISE TURN-OFF SWITCHING

Typical applications include freewheel diodes in motor control systems.



DIOWATT2

ABSOLUTE MAXIMUM RATINGS

V_{RRM}	Peak repetitive reverse voltage	400	V
V_{RWM}	Working peak reverse voltage	400	V
V_R	Continuous reverse voltage	400	V
I_{FRM}	Repetitive peak forward current ($t = 10\mu s$)	700	A
$I_{F(AV)}$	Average forward current $T_{case} = 70°C$ (switching operation, $\delta = 0.5$)	60	A
I_{FSM}	Surge non repetitive forward current ($t = 10ms$)	600	A
P_{tot}	Total dissipation at $T_{case} = 70°C$	90	W
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C

SGS80DA020D

TRANSPACK NPN POWER DARLINGTON MODULE

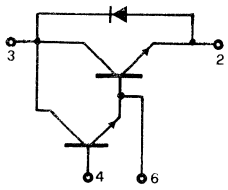
APPLICATIONS: The product is a silicon NPN power darlington for industrial applications.

ISOLATED POWER MODULE (30KVA - 375W)	FAST FREEWHEEL DIODE

ABSOLUTE MAXIMUM RATINGS

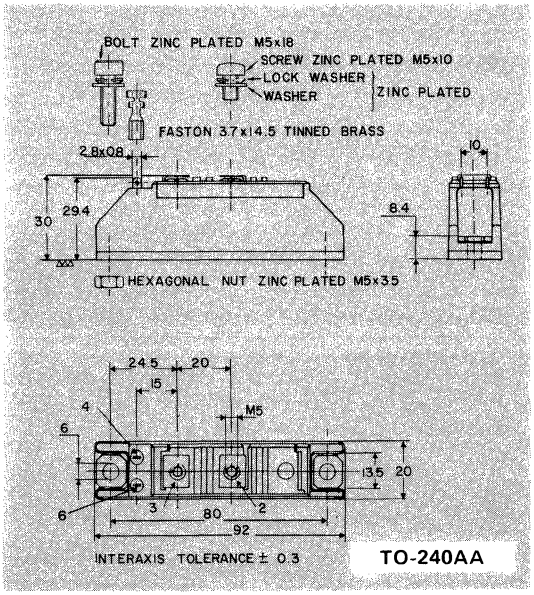
		SGS80DA020D	
V_{CBO}	Collector-base voltage (I_E = 0)	300	V
V_{CES}	Collector-emitter voltage (V_{BE} = 0)	300	V
V_{CEX}	Collector-emitter voltage (V_{BE} = −1.5V)	300	V
V_{CEO}	Collector-emitter voltage (I_B = 0)	200	V
V_{CEOL}	Overload switch-off at 1.5 times $I_{C\ (sat)}$*	250	V
V_{EBO}	Emitter-base voltage (I_C = 0)	7	V
I_C	Collector current	120	A
I_{CM}	Collector peak current (t_p<10 ms)	240	A
I_{CP}	Collector peak current non repetitive (t_p<20 μs)	500	A
I_B	Base current	2	A
I_{BP}	Base peak current non repetitive (t_p<20 μs)	50	A
T_{stg}	Storage temperature	− 40 to 150	°C
T_j	Max. operating junction temperature (continuous)	150	°C
T_j	Max. operating junction temperature (1 minute)	175	°C

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



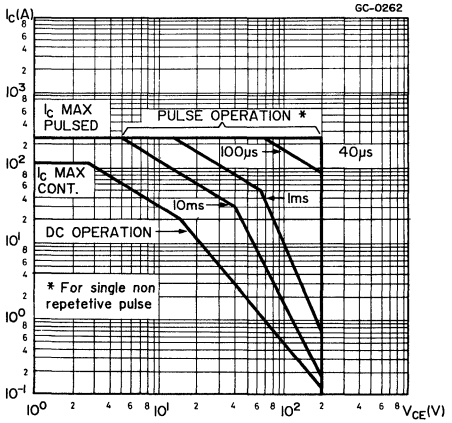
ELECTRICAL CHARACTERISTICS (Continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_f	Diode forward voltage	I_f = 80 A T_j = 25°C		1.60	2	V
		T_j = 125°C		1.70		V
t_{rr}	Diode reverse recovery time	I_f = 80 A di/dt = 100A/µs		0.20	0.5	µs
I_{rm}	Diode reverse recovery current			12		A
I_{frm}	Diode forward current	t = 1ms	300			A

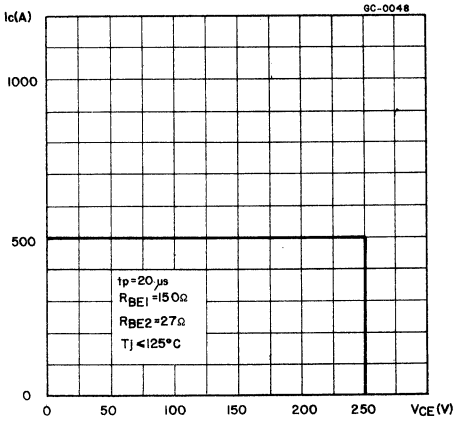
INSULATION TESTING

The insulation between the live parts and the base plate of TO-240 is tested before delivery for one second at 2500 V a.c.
If this test is repeated by the user either as a goods inwards check or as a test of the final equipment, in accordance with IEC Publication 146 (1973), clause 492.1 or DIN 57558 part 1/VDE 0558, part 1/8.77, section 5.7.9., only a voltage slowly increasing up to the above value should be used. If the voltage is applied for one minute as recommended by the above standards then the specified value of 2000 V should be taken.
During the test all electrical terminals including the drive terminals must be connected with each other in order to avoid damage by inductively or capacitively induced voltage transients. The test voltage is applied between the connected terminals and the base plate.

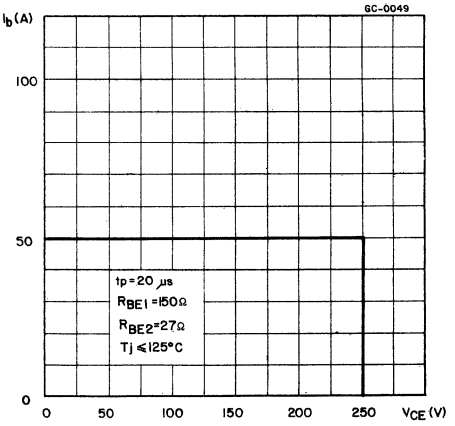
Safe operating areas



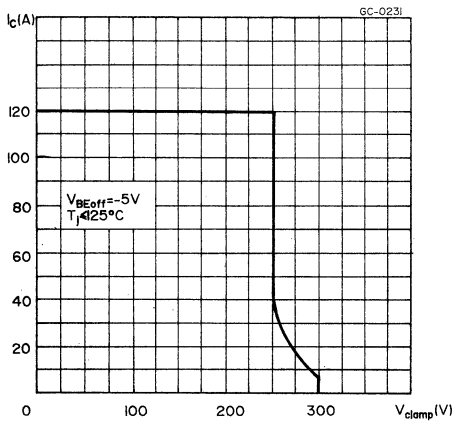
Collector overload SOA (see fig. 1)



Base overload SOA (see fig. 1)



Reverse biased SOA (see fig. 2)



Switching times inductive load (see fig. 3)

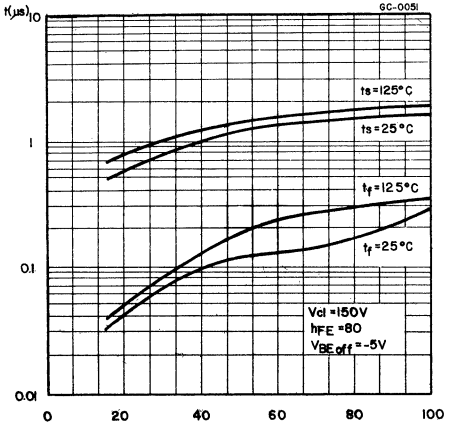


Fig. 2 RBSOA TEST CIRCUIT

RBSOA test circuit has been driven by the switching times test circuit with $R_{B2} = O$.
RBSOA sensitivity to T_j variations is very limited, so that the limits shown can be kept valid at ambient temperature as well.

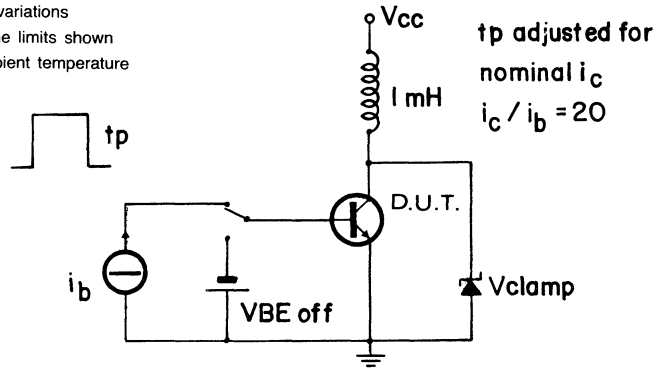
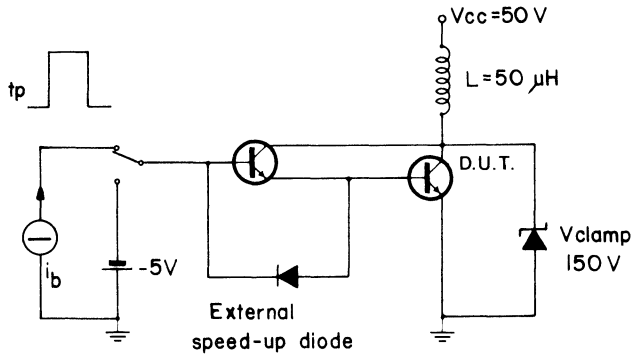


Fig. 3 Switching times test circuit.



SGS100DA025D

PRELIMINARY DATA

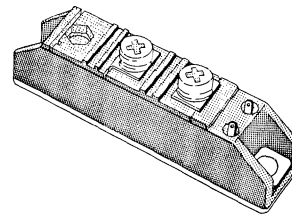
TRANSPACK NPN POWER DARLINGTON MODULE

APPLICATONS: The product is a silicon NPN power darlington for industrial applications.

- ISOLATED POWER MODULE (UP TO 2500V)
- FAST FREEWHEEL DIODE
- VERY HIGH CURRENT
- VERY HIGH POWER (UP TO 37.5 KVA)

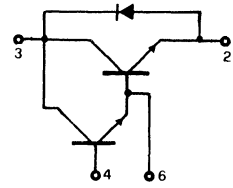
INDUSTRIAL APPLICATIONS

- MOTOR CONTROLS
- UNINTERUPTABLE POWER SUPPLIES
- HIGH POWER REGULATED DC SUPPLIES



TO-240AA

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS		SGS100DA025D	
V_{CBO}	Collector-base voltage (I_E = 0)	300	V
V_{CES}	Collector-emitter voltage (V_{BE} = 0)	300	V
V_{CEX}	Collector-emitter voltage (V_{BE} = −1.5V)	300	V
V_{CEO}	Collector-emitter voltage (I_B = 0)	250	V
V_{CEOL}	Overload switch-off at 1.5 times $I_{C\ (sat)}$*	250	V
V_{EBO}	Emitter-base voltage (I_C = 0)	7	V
I_C	Collector current	150	A
I_{CM}	Collector peak current (t_p < 10 ms)	300	A
I_{CP}	Collector peak current non repetitive (t_p < 20 μs)	600	A
I_B	Base current	2	A
I_{BP}	Base peak current non repetitive (t_p < 20 μs)	60	A
T_{stg}	Storage temperature	−40 to 150	°C
T_j	Max. operating junction temperature (continuous)	150	°C
T_j	Max. operating junction temperature (1 minute)	175	°C

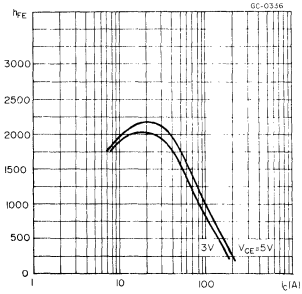
ELECTRICAL CARACTERISTICS (Continued)

Parameter		Test Condition	Min.	Typ.	Max.	Unit
V_f	Diode Forward voltage	I_f = 100A I_f = 100A T_j = 125°C		1.6 1.7	2	V
t_{rr}	Diode reverse recovery time	I_f = 100A di/dt = 100A/μs		0.2	0.5	μs
I_{rm}	Diode reverse recovery current			15		A
I_{frm}	Diode forward current	t = 1ms	300			A

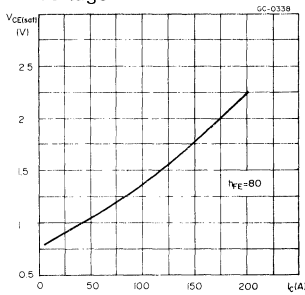
INSULATION TESTING

The insulation between the live parts and the base plate of TO-240 is tested before delivery for one second at 2500 V a.c.
If this test is repeated by the user either as a goods inwards check or as a test of the final equipment, in accordance with IEC Publication 146 (1973), clause 492. 1 or DIN 57558 part. 1/VDE 0558, part 1/8.77, section 5.7.9., only a voltage slowly increasing up to the above standards then the specified value of 2000 V should be taken.
During the test all electrical terminals including the drive terminals must be connected with each other in order to avoid damage by inductively or capacitively induced voltage transients. The test voltage is applied between the connected terminals and the base plate.

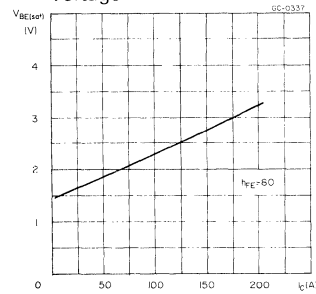
DC current gain



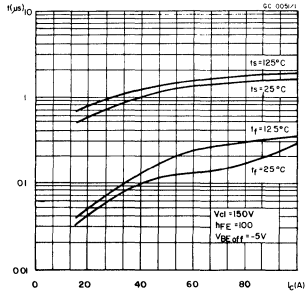
Collector-emitter saturation voltage



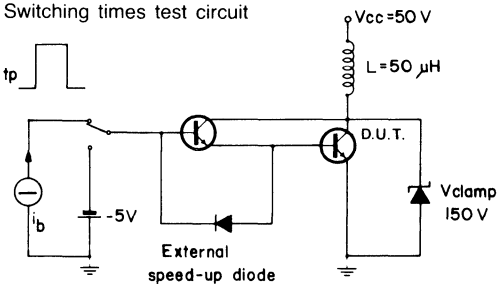
Base-emitter saturation voltage



Switching times inductive load

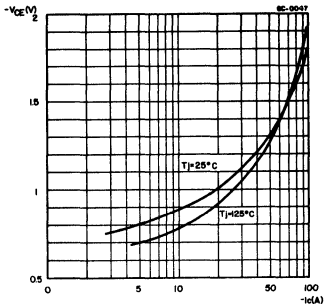


Switching times test circuit

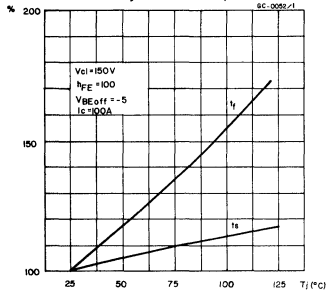


SC-0004

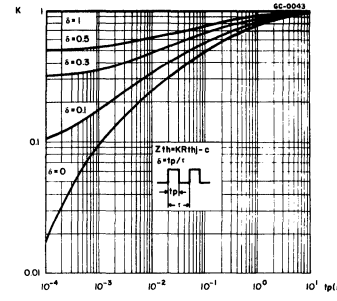
Typical V_F versus - Ic



Switching times inductive load vs. junc. temp.



Thermal impedance



SGS100MA010D1

ADVANCE DATA

TRANSPACK N-CHANNEL POWER MOS MODULE

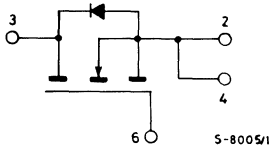
APPLICATIONS: The SGS100MA010D1 is a N-Channel POWER MOS MODULE for industrial applications (quarter bridge configuration).

ISOLATED POWER MODULE (10KVA - 375W)	INTERNAL FREEWHEEL DIODE

ABSOLUTE MAXIMUM RATINGS

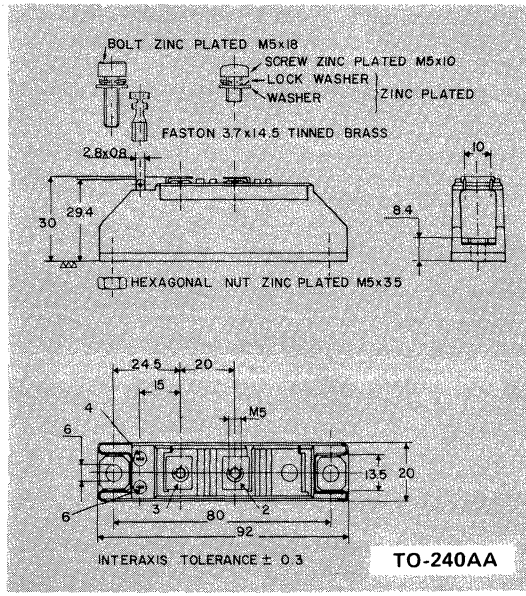
		SGS100MA010D1	
V_{DS}	Drain-source voltage (V_{GS} = 0)	100	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	100	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) T_C = 25 °C	100	A
I_{DM}	Drain current (t_p < 10 ms, repetitive)	150	A
I_{DLM}	Drain current (t_p = 20μs, not repetitive)	250	A
P_{tot}	Total dissipation at T_C < 25 °C	300	W
	Derating factor	3	W/°C
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature (continuous)	150	°C
T_j	Max. operating junction temperature (1 minute)	175	°C

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



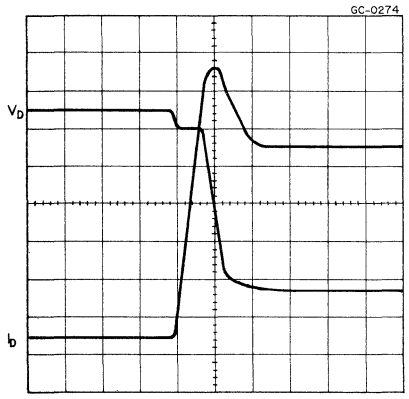
This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

ELECTRICAL CHARACTERISTICS (Continued)

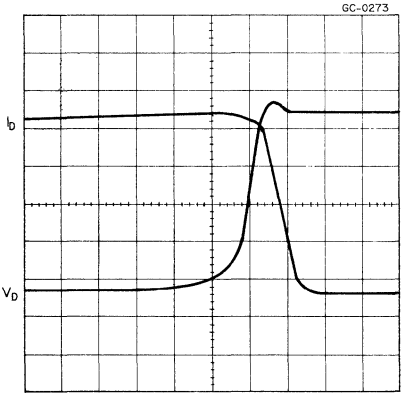
Parameter		Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE (see note B)						
I_{SD}	Source-drain current (continuous)				100	A
I_{SDM}	Source-drain current (pulsed)				250	A
V_{SD}	Forward on voltage	I_{SD} = 100 A V_{GS} = 0			2	V
t_{rr}	Reverse recovery time	I_{SD} = 100 A V_{GS} = 0 di/dt = 250 A/µs		400		ns

Note A: switching times inductive load have been tested by the circuit shown in fig. 1 (by paralleling the load with SGS fast recovery diode...).
Typical waveforms obtained for V_D and I_D are schematically shown here below.

I_D-V_D at turn-on



I_D-V_D at turn-off



Note that di/dt does not depend on the perfomances of the freewheeling diode, but on the D.U.T. and its drive circuit only.

SGS150MA010D1

ADVANCE DATA

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

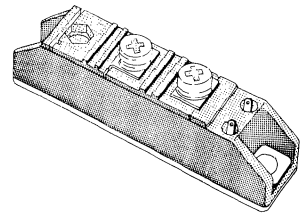
V_{DSS}	$R_{DS\ (on)}$	I_D
100V	0.009Ω	150A

- ISOLATED POWERMOS MODULE
- HIGH POWER
- FAST SWITCHING
- EASY DRIVE
- EASY TO PARALLEL

INDUSTRIAL APPLICATION:

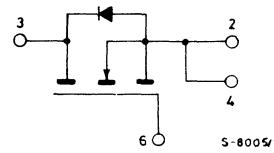
- SWITCHING MODE POWER SUPPLIES
- UNINTERRUPTIBLE POWER SUPPLIES
- MOTOR CONTROLS
- INVERTERS

N-Channel enhancement mode POWERMOS field effect transistors. Easy drive and fast switching of these TRANSPACK modules makes them ideal for high power, high speed switching applications.
Typical applications include DC motor control (speed, soft start and torque), switching mode power supplies, uninterruptible power supplies, DC/DC convertors and high frequency welding equipment.
The large RBSOA and absence of second breakdown in POWERMOS make these TRANSPACK modules very rugged. This, together with the isolated package with its optimised thermal performance, make these modules extremely effective in high power application.



TO-240AA

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		SGS150MA010D1	
V_{DS}	Drain-source voltage (V_{GS} = 0)	100	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	100	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) T_c = 25°C	150	A
I_{DM}	Drain current ($t_p \leqslant 10$ ms, repetitive)	225	A
I_{DLM}	Drain current, ($t_p = 20\mu s$, not repetitive)	375	A
P_{tot}	Total dissipation at $T_{case} < 25°C$	400	W
	Derating factor	3.2	W/°C
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature (continuous)	150	°C

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

ELECTRICAL CHARACTERISTICS (continued)

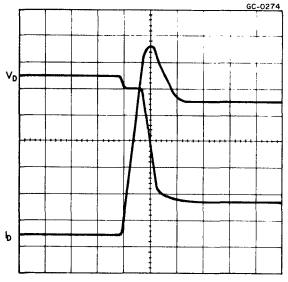
Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SOURCE DRAIN DIODE						
I_{SD}	Source-Drain current (continuous)				150	A
I_{SDM}	Source-Drain current (pulsed)				375	A
V_{SD}	Forward on voltage	I_{SD} = 150A V_{GS} = 0			2	V
t_{rr}	Reverse recovery time	di/dt = 250A/μs I_{SD} = 150A V_{GS} = 0		400		ns

INSULATION TESTING

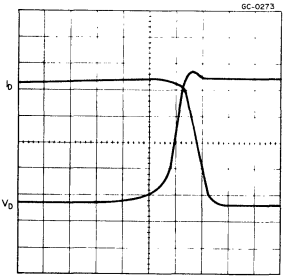
The insulation between the live parts and the base plate of TO-240 is tested before delivery for one second at 2500 V a.c.
If this test is repeated by the user either as a goods inwards check or as a test of the final equipment, in accordance with IEC Publication 146 (1973), clause 492.1 or DIN 57558 part 1/VDE 0558, part 1/8.77, section 5.7.9., only a voltage slowly increassing up to the above standards then the specified value of 2000 V should be taken.
During the test all electrical terminals including the drive terminals must be connected with each other in order to avoid damage by inductively or capacitively induced voltage transients. The test voltage is applied between the connected terminals and the base plate.

Note A: switching times inductive load have been tested by the circuit shown in fig. 1 (by paralleling the load with SGS fast recovery diode SGS45R80).
Typical waveforms obtained for V_D and I_D are schematically shown here below.

I_D-V_D af turn-on



I_D-V_D af turn-off



Note that di/dt does not depend on the performances of the freewheeling diode, but on the D.U.T. and its drive circuit only.

SGS10004
SGS10004P
SGS10005
SGS10005P

ADVANCE DATA

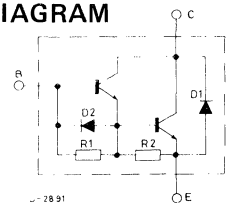
HIGH VOLTAGE FAST SWITCHING

The SGS10004/10005 are silicon power Darlington transistors with integrated base-emitter speed-up diode, mounted in Jedec TO-3 metal case designed for high-power, fast switching applications. The SGS10004P and SGS10005P are mounted in SOT-93 case similar to TO-218. This family is an economic alternative to MJ10004 or MJ10005 particularly suitable for applications at 8A operating currents.

ABSOLUTE MAXIMUM RATING

		SOT-93 TO-3	SGS10004P SGS10004	SGS10005P SGS10005
V_{CEO}	Collector-emitter voltage ($I_B = 0$)		350V	400V
V_{CEX}	Collector-emitter voltage ($V_{BE} = -5V$)		400V	450V
V_{CEV}	Collector-emitter voltage ($V_{BE} = 1.5V$)		450V	500V
V_{EBO}	Emitter-base voltage ($I_C = 0$)		8V	
I_C	Collector current		16A	
I_{CM}	Collector peak current		25A	
I_B	Base current		2.5A	
I_{BM}	Base peak current		5A	
P_{tot}	Total power dissipation at $T_{case} \leqslant 25°C$		(TO-3) 175W	(SOT-93) 150W
T_{stg}	Storage temperature		-65 to 200°C	-65 to 175°C
T_j	Junction temperature		200°C	175°C

INTERNAL SCHEMATIC DIAGRAM

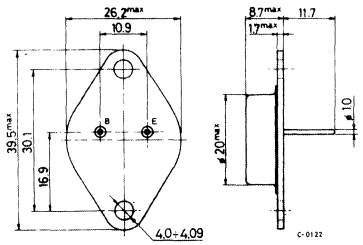


R1 Typ. 100Ω
R2 Typ. 350Ω

MECHANICAL DATA

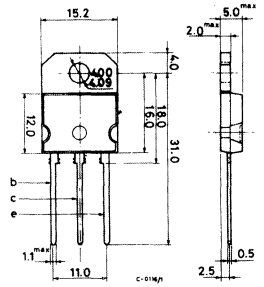
Dimension in mm

Collector connected to case



TO-3

Collector connected to tab



(sim. to TO-218) SOT-93

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_f*	Diode forward voltage	$I_F = 10A$		3	5	V
h_{fe}	Small-signal current gain	$I_C = 1A$ $V_{CE} = 10V$ $f_{test} = 1MHz$	10			–
C_{OB}	Output capacitance	$V_{CB} = 10V$ $I_E = 0$ $f_{test} = 100MHz$	100		325	pF
t_{on}	Turn-on time	V_{CC}=250V $I_C = 8A$ $I_{B1} = -I_{B2} = 400mA$ $V_{BE\ (off)} = 5V$		0.22	0.8	μs
t_r	Rise Time			0.6	1.5	μs
t_f	Fall time	$t_p = 50\mu s$ duty cycle $\leqslant 2\%$		0.15	0.5	μs

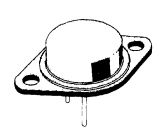
*Pulsed: pulse duration = 300μs duty cycle = 1.5% .

SGSD00030
SGSD00031
SGSID312

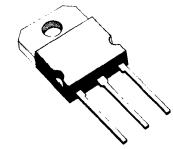
HIGH VOLTAGE, HIGH POWER, FAST SWITCHING

- INTEGRATED SPEED-UP DIODE
- MOTOR CONTROLS

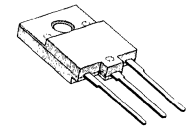
The SGSD00031, SGS00030 and SGSID312 are silicon multiepitaxial planar NPN transistors in monolithic darlington configuration with integrated speed-up diode, mounted respectively in Jedec TO-3 metal case, SOT-93 plastic package and ISOWATT218 fully isolated package.
No parasitic collector-emitter diode, so that an external fast recovery free wheeling diode can be added.
They are particulary suitable as output stage in high power, fast switching applications.



TO-3

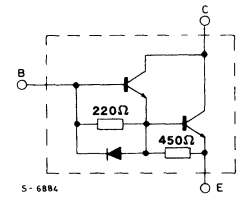


SOT-93 (TO-218)



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

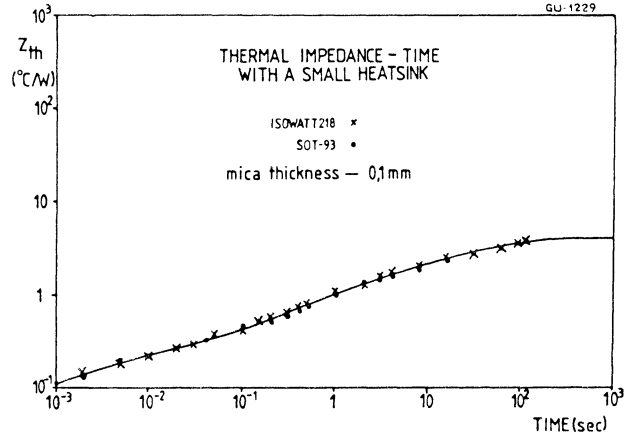
V_{CER}	Collector-emitter voltage (R_{BE} = 50 ohm)		600		V
V_{CEO}	Collector-emitter voltage (I_B = 0)		400		V
I_C	Collector current		28		A
I_{CM}	Collector peak current ($t_p \leqslant$ 10ms)		40		A
I_B	Base current		6		A
I_{BM}	Base peak current ($t_p \leqslant$ 10ms)		12		A
		TO-3	**SOT-93**	**ISOWATT218**	
V_{ISO}	Isolation voltage (DC)			4000	V
P_{tot}	Total dissipation at $T_c \leqslant 25°C$	150	125	50	W
T_{stg}	Storage temperature	−65 to 175	−65 to 150	−65 to 150	°C
T_j	Max. operating junction temperature	175	150	150	°C

THERMAL RESISTANCE OF THE ISOWATT218

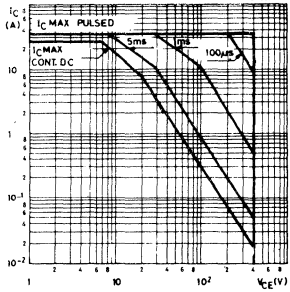
The junction to case thermal resistance of 2.5 °C/W for the ISOWATT218 package may seem quite high at first glance but if compared to a conventional SOT-93 (TO-218) package with a 0.1 mm mica insulating washer, the differences are marginal. The 0.1 mm isolating washer gives 1500V to 2000V DC isolation for the SOT-93 package, SGS guarantee 4000V DC isolation for the ISOWATT218.

The comparison in fig. 1 shows the dynamic thermal resistance of both devices mounted using a thermal compound. The test illustrates that the ISOWATT218 has an R_{th} very close to that of conventional SOT-93 (TO-218) and any small increase is more than compensated for by the convenience of the ISOWATT218 package. The collector to heatsink capacitance of the ISOWATT218 is typically 17pF.

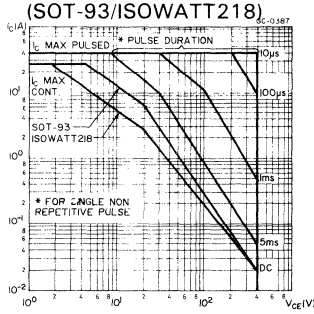
Fig. 1



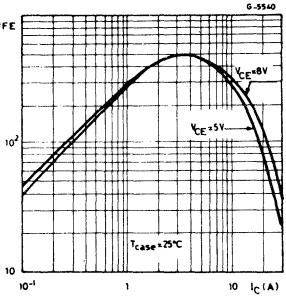
Safe operating area (TO-3)



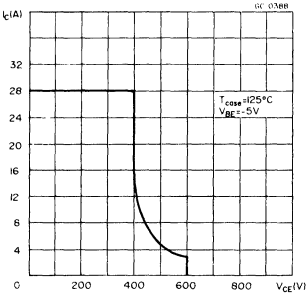
Safe operating area (SOT-93/ISOWATT218)



DC current gain

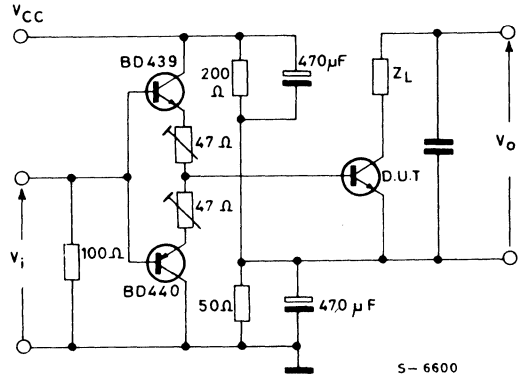


Clamped reverse bias safe operating areas



TEST CIRCUIT

Fig. 2

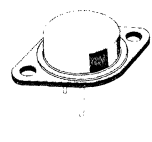


SGSD310
SGSD311
SGSID311

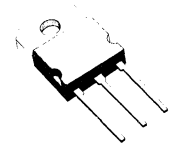
HIGH VOLTAGE, HIGH POWER, FAST SWITCHING

- INTEGRATED SPEED-UP DIODE
- MOTOR CONTROLS

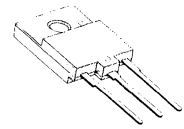
The SGSD310, SGSD311 and SGSID311 are silicon multiepitaxial planar NPN transistors in monolithic darlington configuration with integrated speed-up diode, mounted respectively in Jedec TO-3 metal case, SOT-93 plastic package and ISOWATT218 fully isolated package.
No parasitic collector-emitter diode, so that an external fast recovery free wheeling diode can be added.
They are particulary suitable as output stage in high power, fast switching applications.



TO-3

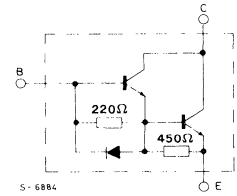


SOT-93 (TO-218)



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

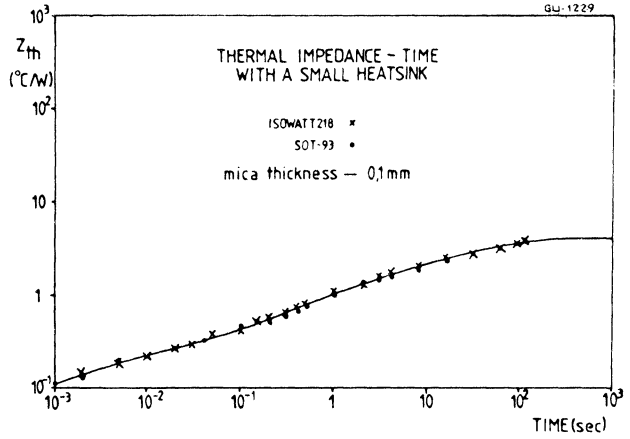
V_{CER}	Collector-emitter voltage (R_{BE} = 50 ohm)		600		V
V_{CEO}	Collector-emitter voltage (I_B = 0)		400		V
I_C	Collector current		28		A
I_{CM}	Collector peak current ($t_p \leqslant$ 10ms)		40		A
I_B	Base current		6		A
I_{BM}	Base peak current ($t_p \leqslant$ 10ms)		12		A
		TO-3	SOT-93	ISOWATT218	
V_{ISO}	Isolation voltage (DC)			4000	V
P_{tot}	Total dissipation at $T_c \leqslant 25°C$	150	125	50	W
T_{stg}	Storage temperature	−65 to 175	−65 to 150	−65 to 150	°C
T_j	Max. operating junction temperature	175	150	150	°C

THERMAL RESISTANCE OF THE ISOWATT218

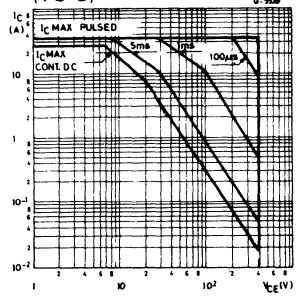
The junction to case thermal resistance of 2.5 °C/W for the ISOWATT218 package may seem quite high at first glance but if compared to a conventional SOT-93 (TO-218) package with a 0.1 mm mica insulating washer, the differences are marginal. The 0.1 mm isolating washer gives 1500V to 2000V DC isolation for the SOT-93 package, SGS guarantee 4000V DC isolation for the ISOWATT218.

The comparison in fig. 1 shows the dynamic thermal resistance of both devices mounted using a thermal compound. The test illustrates that the ISOWATT218 has an R_{th} very close to that of conventional SOT-93 (TO-218) and any small increase is more than compensated for by the convenience of the ISOWATT218 package. The collector to heatsink capacitance of the ISOWATT218 is typically 17pF.

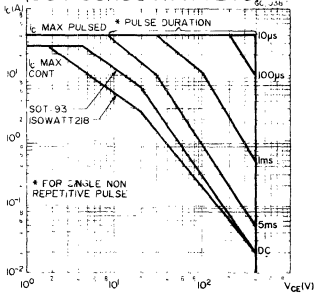
Fig. 1



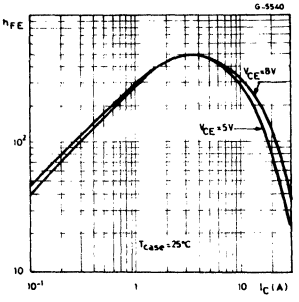
Safe operating area (TO-3)



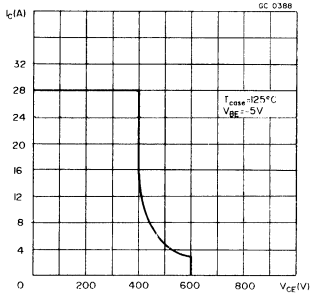
Safe operating area (SOT-93/ISOWATT218)



DC current gain

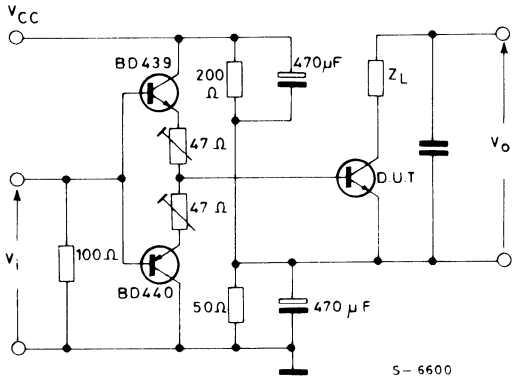


Clamped reverse bias safe operating areas



TEST CIRCUIT

Fig. 2



SGSP221/P222
SGSP321/P322
SGSP421/P422
SGSP521/P522

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

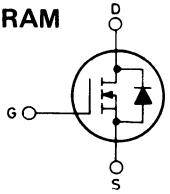
V_{DSS}	$R_{DS(ON)}$	I_D
50V/60V	0.13Ω	10A

ABSOLUTE MAXIMUM RATINGS

		SOT-82 TO-220 SOT-93 TO-3	SGSP221 SGSP321 SGSP421 SGSP521	SGSP222 SGSP322 SGSP422 SGSP522
V_{DS}	Drain-source voltage (V_{GS} = 0)		60V	50V
V_{DGR}	Drain gate voltage (R_{GS} = 20KΩ)		60V	50V
V_{GS}	Gate-source voltage		± 20V	
I_D	Drain current (continuous) at T_{case} = 25°C		10A	
	at T_{case} = 100°C		6.5A	
I_{DM} (•)	Drain current (pulsed)		40A	
I_{DLM} (•)	Drain inductive current, clamped		40A	
			SOT-82	TO-220/SOT93/TO-3
P_{tot}	Total power dissipation at $T_{case} \leqslant 25°C$		50W	75W
	Derating factor		0.4W/°C	0.6W/°C
T_{stg}	Storage temperature		-55 to 150°C	
T_j	Junction temperature		150°C	

(•) Pulse width limited by safe operating area

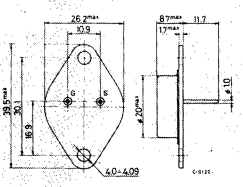
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

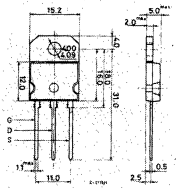
Dimensions in mm

Drain connected to case



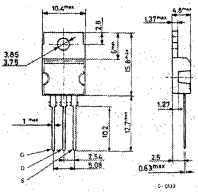
TO-3

Drain connected to tab



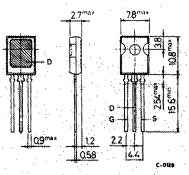
(sim. to TO-218) SOT-93

Drain connected to tab



TO-220

Drain connected to tab



SOT-82

ELECTRICAL CHARACTERISTICS (Continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
SWITCHING						
$t_{d(on)}$	Turn-on delay time	V_{cc} = 25V V_i = 10V		30		ns
t_r	Rise time	I_D = 5A R_i = 50 Ω		130		ns
$t_{d(off)}$	Turn-off delay time	(see test circuit)		80		ns
t_f	Fall time			130		ns
SOURCE DRAIN DIODE						
I_{SD}	Source-drain current				10	A
I_{SDM} (•)	Source-drain current (pulsed)				40	A
V_{SD}	Forward on voltage	I_{SD} = 10A V_{GS} = 0			1.4	V
t_{on}	Turn-on time	di/dt = 25A/μs		60		ns
t_{rr}	Reverse recovery time	I_{SD} = 10A V_{GS} = 0		100		ns

* Pulsed: pulse duration ≤ 300 μs, duty cycle ≤ 2%

(•) Pulse width limited by safe operating area

SGSP363/P367
SGSP463/P467
SGSP563/P567

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

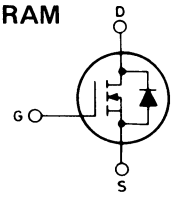
V_{DSS}	$R_{DS(ON)}$	I_D
200V	0.33Ω	10A
250V	0.45Ω	10A

ABSOLUTE MAXIMUM RATINGS

		TO-220 SOT-93 TO-3	SGSP363 SGSP463 SGSP563	SGSP367 SGSP467 SGSP567
V_{DS}	Drain-source voltage (V_{GS} = 0)		250V	200V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)		250V	200V
V_{GS}	Gate-source voltage		± 20V	
I_D	Drain current (continuous) T_{case} = 25°C		10A	
	T_{case} = 100°C		6.4A	
I_{DM}(•)	Drain current (pulsed)		40A	
I_{DLM}(•)	Drain inductive current, clamped		40A	
		TO-220	**SOT-93/TO-3**	
P_{tot}	Total power dissipation T_{case} = 25°C	100W	125W	125W
	Derating factor	0.8W/°C	1W/°C	1W/°C
T_{stg}	Storage temperature		− 55 to 150° C	
T_j	Junction temperature		150°C	

(•) Pulse width limited by safe operating area

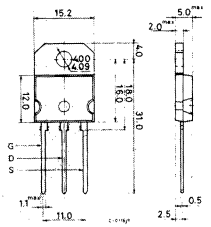
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

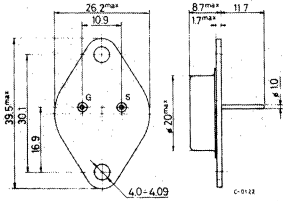
Dimensions in mm

Drain connected to tab



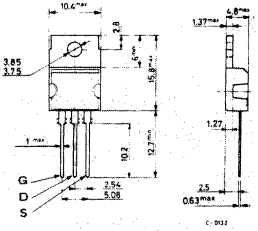
(sim. to **TO-218**) **SOT-93**

Drain connected to case



TO-3

Drain connected to tab



TO-220

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
DYNAMIC						
C_{iss}	Input capacitance	$V_{DS} = 25V$ $f = 1MHz$		980	1200	pF
C_{oss}	Output capacitance	$V_{GS} = 0$		200	260	pF
C_{rss}	Reverse transfer Capacitance			80	100	pF
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	$V_{CC} = 25V$ $V_i = 10V$		10		ns
t_r	Rise time	$I_D = 5A$ $R_i = 15\ \Omega$		25		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		50		ns
t_f	Fall time			32		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current				10	A
I_{SDM} (·)	Source drain current (pulsed)				40	A
V_{SD}	Forward on voltage	$I_{SD} = 10A$ $V_{GS} = 0$			1.3	V
t_{on}	Turn-on time	$I_{SD} = 10A$ $V_{GS} = 0$		130		ns
t_{rr}	Reverse recovery time	$di/dt = 100A/\mu s$		250		ns

* Pulsed: pulse duration $\leqslant 300\mu s$, duty cycle $\leqslant 0.2\%$

(·) Pulse width limited by safe operating area

SGSP364/P365/P366
SGSP464/P465/P466
SGSIP464/IP465/IP466
SGSP564/P565/P566

HIGH SPEED SWITCHING APPLICATIONS

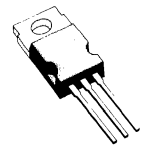
V_{DSS}	$R_{DS\ (on)}$	I_D
350/400 V	1 Ω	6 A
450 V	1.5 Ω	6 A

- HIGH VOLTAGE - FOR ELECTRONIC LAMP BALLAST
- ULTRA FAST SWITCHING
- EASY DRIVE - REDUCES COST AND SIZE

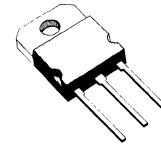
INDUSTRIAL APPLICATIONS:

- ELECTRONIC LAMP BALLAST
- DC SWITCH

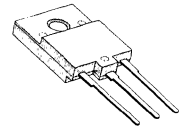
N-Channel enhancement mode POWERMOS field effect transistors. Easy drive and very fast switching times make these POWERMOS transistors ideal for high speed switching applications.
Applications include DC switch, constant current source, ultrasonic equipment and electronic ballast for fluorescent lamps.
The package range for this device includes the isolated case ISOWATT218. This provides isolation to 2500V ac, 4000V dc and the creepage distance requirement of VDE, IEC and UL specifications.



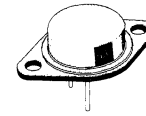
TO-220



SOT-93 (TO-218)

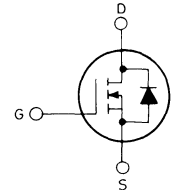


ISOWATT218



TO-3

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	TO-220 / SOT-93 / ISOWATT218 / TO-3	SGSP364 / SGSP464 / SGSIP464 / SGSP564	SGSP365 / SGSP465 / SGSIP465 / SGSP565	SGSP366 / SGSP466 / SGSIP466 / SGSP566	
V_{DS}	Drain-source voltage (V_{GS} = 0)	450	400	350	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	450	400	350	V
V_{GS}	Gate-source voltage		± 20		V
I_D	Drain current (continuous) T_c = 25°C		6		A
	at T_c = 100°C		4		A
I_{DM}(•)	Drain current (pulsed)		24		A
I_{DLM}	Drain inductive current, clamped		24		A
		TO-220	SOT-93	ISOWATT218	TO-3	
V_{ISO}	Isolation voltage (DC)			4000		V
P_{tot}	Total dissipation at T_{case} = 25°C	100	125	50	125	W
	Derating factor	0.8	1	0.4	1	W/°C
T_{stg}	Storage temperature		−55 to 150			°C
T_j	Max. operating junction temperature		150			°C

(•) Pulse width limited by safe operating area.

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25V I_D = 3A	3			mho
C_{iss}	Input capacitance			780	1000	pF
C_{oss}	Output capacitance	V_{DS} = 25V f = 1 MHz		150	200	pF
C_{rss}	Reverse transfer capacitance	V_{GS} = 0		100	130	pF
$C_{D\text{-}HS}$	Drain-Heatsink capacitance	$V_{D\text{-}HS}$ = 25V f = 1 MHz		19	23	pF
SWITCHING						
$t_{d(on)}$	Turn-on time	V_{CC} = 250V I_D = 3A		30		ns
t_r	Rise time	V_i = 10V R_i = 10Ω		30		ns
$t_{d(off)}$	Turn off delay time	(see test circuit)		100		ns
t_f	Fall time			50		ns
SOURCE DRAIN DIODE						
I_{SD}	Source-Drain current				6	A
I_{SDM} (•)	Source-Drain current (pulsed)				24	A
V_{SD}	Forward on voltage	I_{SD} = 6A V_{GS} = 0			1.2	V
t_{on}	Turn-on time	I_{SD} = 6A V_{GS} = 0		250		ns
t_{rr}	Reverse recovery time	di/dt = 25A/μs		350		ns

* Pulsed: Pulse duration = 300μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

SGSP368/369
SGSP468/469
SGSIP468/469
SGSP568/569

HIGH SPEED SWITCHING APPLICATIONS

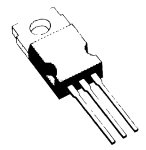
V_{DSS}	$R_{DS\ (on)}$	I_D
500V	1.5 Ω	5A
550V	2.5 Ω	5A

- HIGH VOLTAGE - FOR ELECTRONIC LAMP BALLAST AND SMPS
- ULTRA FAST SWITCHING - UP TO 200KHz OPERATIONS
- EASY DRIVE - REDUCES COST AND SIZE

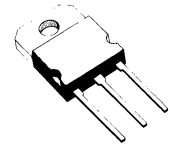
INDUSTRIAL APPLICATIONS:

- SMPS
- ELECTRONIC LAMP BALLAST
- DC SWITCH

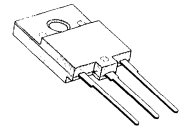
N-Channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications.
Applications include DC switch, constant current source, ultrasonic equipment electronic ripple control and electronic ballast for fluorescent lamps.
The package range for this devices includes the isolated case ISOWATT218. This provides isolation to 2500V ac, 4000V dc and the creepage distance requirement of VDE, IEC, and UL specifications.



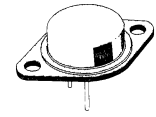
TO-220



SOT-93 (TO-218)

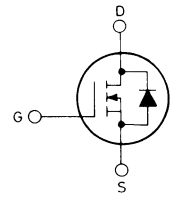


ISOWATT218



TO-3

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-220 SOT-93 ISOWATT218 TO-3	SGSP368 SGSP468 SGSIP468 SGSP568	SGSP369 SGSP469 SGSIP469 SGSP569	
V_{DS}	Drain-source voltage (V_{GS} = 0)		550	500	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)		550	500	V
V_{GS}	Gate-source voltage		± 20		V
I_D	Drain current (continuous) T_c = 25°C		5		A
	at T_c = 100°C		3.2		A
I_{DM}(•)	Drain current (pulsed)		20		A
I_{DLM}	Drain inductive current, clamped		20		A
		TO-220	**SOT-93**	**ISOWATT218**	**TO-3**	
V_{ISO}	Isolation voltage (DC)			4000		V
P_{tot}	Total dissipation at T_{case} = 25°C	100	125	50	125	W
	Derating factor	0.8	1	0.4	1	W/°C
T_{stg}	Storage temperature			−55 to 150		°C
T_j	Max. operating junction temperature			150		°C

(•) Pulse width limited by safe operating area.

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on time	$V_{CC} = 250V$ $I_D = 2.5A$		30		ns
t_r	Rise time	$V_i = 10V$ $R_i = 10\Omega$		15		ns
$t_{d(off)}$	Turn off delay time	(see test circuit)		80		ns
t_f	Fall time			40		ns
SOURCE DRAIN DIODE						
I_{SD}	Source-Drain current				5	A
I_{SDM} (•)	Source-Drain current (pulsed)				20	A
V_{SD}	Forward on voltage	$I_{SD} = 5A$ $V_{GS} = 0$			1.15	V
t_{on}	Turn-on time	$I_{SD} = 5A$ $V_{GS} = 0$		85		ns
t_{rr}	Reverse recovery time	$di/dt = 150A/\mu s$		320		ns

* Pulsed: Pulse duration = 300/μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

SGSP386/SGSP387
SGSP486/SGSP487
SGSP586/SGSP587

PRELIMINARY DATA

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

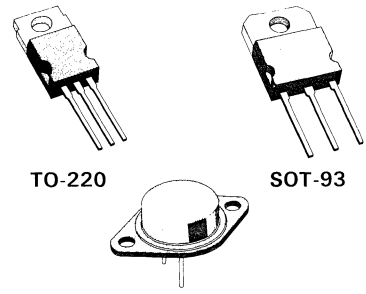
These products are diffused multi-cells silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

V_{DSS}	$R_{DS\ (on)}$	I_D
60V	0.04 Ω	40A
50V	0.04 Ω	40A

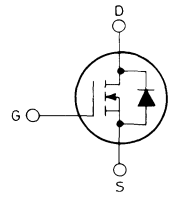
- HIGH CURRENT
- VERY LOW THERMAL RESISTANCE
- VERY LOW ON-LOSSES
- EASY DRIVE

AUTOMOTIVE APPLICATIONS

- POWER ACTUATORS



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-220 SOT-93 TO-3 SGSP386 SGSP486 SGSP586	SGSP387 SGSP487 SGSP587	
V_{DS}	Drain-source voltage (V_{GS} = 0)	60	50	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	60	50	V
V_{GS}	Gate-source voltage	±20		V
I_D	Drain current (continuous) T_{case} = 25°C	40		A
	at T_{case} = 100°C	25		A
I_{DM}(•)	Drain current (pulsed)	120		A
I_{DLM}	Drain inductive current, clamped	120		A
P_{tot}	Total dissipation at T_{case} = 25°C	125		W
	Derating factor	1		W/°C
T_{stg}	Storage temperature	−55 to 150		°C
T_j	Max. operating junction temperature	150		°C

• Pulse width limited by safe operating area

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 30V I_D = 15A		40		ns
t_r	Rise time	V_{GS} = 10V R_{GS} = 50 Ω		150		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		150		ns
t_f	Fall time			180		ns
SOURCE DRAIN DIODE						
I_{SD}	Source-Drain current				40	A
I_{SDM} (•)	Source-Drain current (pulsed)				120	A
V_{SD}	Forwaed on voltage	V_{GS} = 0 I_{SD} = 40A			1.8	V
t_{rr}	Reverse recovery time	I_{SD} = 40A di/dt = 100 A/μs		80		ns
Q_{rr}	Reverse recovered charge			0.2		μC

* Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area.

SGSP473/P477
SGSIP473/IP477
SGSP573/P577

HIGH SPEED SWITCHING APPLICATIONS

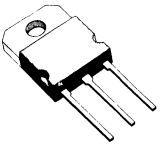
V_{DSS}	$R_{DS\ (on)}$	I_D
200 V	0.17 Ω	20 A
250 V	0.22 Ω	20 A

- 200-250V - FOR TELECOMS APPLICATIONS
- HIGH CURRENT - FOR PULSED LASER DRIVES
- ULTRA FAST SWITCHING
- EASY DRIVE - REDUCES COST AND SIZE

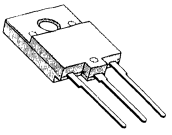
INDUSTRAIL APPLICATIONS:

- SWITCHING MODE POWER SUPPLY
- MOTOR CONTROL FOR ROBOTICS

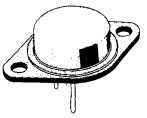
N-Channel enhancement mode POWERMOS field effect transistors. Easy drive and fast switching times make these POWERMOS transistors ideal for high speed switching applications.
Typical applications include electronics, laser diode drivers, UPS, SMPS, DC/DC, DC switch for telecoms and electronic vehicle drivers.
The package range for this device includes the isolated case ISOWATT218. This provides isolation to 2500V ac, 4000V dc and the creepage requirements of VDE, IEC and UL specifications.



SOT-93 (TO-218)

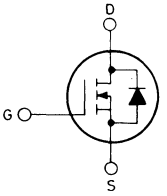


ISOWATT218



TO-3

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		SOT-93 ISOWATT218 TO-3	SGSP473 SGSIP473 SGSP573	SGSP477 SGSIP477 SGSP577	
V_{DS}	Drain-source voltage (V_{GS} = 0)		250	200	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)		250	200	V
V_{GS}	Gate-source voltage		± 20		V
I_D	Drain current (continuous) T_c = 25°C		20		A
	at T_c = 100°C		13		A
I_{DM}(•)	Drain current (pulsed)		80		A
I_{DLM}	Drain inductive current, clamped		80		A
		SOT-93	ISOWATT218	TO-3	
V_{ISO}	Isolation voltage (DC)		4000		V
P_{tot}	Total dissipation at T_{case} = 25°C	150	50	150	W
	Derating factor	1.2	0.4	1.2	W/°C
T_{stg}	Storage temperature		−55 to 150		°C
T_j	Max. operating junction temperature		150		°C

(•) Pulse width limited by safe operating area.

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25V I_D = 10A	8			mho
C_{iss}	Input capacitance	V_{DS} = 25V f = 1 MHz V_{GS} = 0		1900	2200	pF
C_{oss}	Output capacitance			450	550	pF
C_{rss}	Reverse transfer capacitance			200	260	pF
$C_{D\text{-}HS}$	Drain-Heatsink capacitance	$V_{D\text{-}HS}$ = 25V f = 1 MHz		19	23	pF
SWITCHING						
$t_{d(on)}$	Turn-on time	V_{CC} = 75V I_D = 10A		30		ns
t_r	Rise time	V_i = 10V R_i = 10Ω		25		ns
$t_{d(off)}$	Turn off delay time	(see test circuit)		90		ns
t_f	Fall time			20		ns
SOURCE DRAIN DIODE						
I_{SD}	Source-Drain current				20	A
I_{SDM} (•)	Source-Drain current (pulsed)				80	A
V_{SD}	Forward on voltage	I_{SD} = 20A V_{GS} = 0			1.3	V
t_{on}	Turn-on time	I_{SD} = 18A V_{GS} = 0		300		ns
t_{rr}	Reverse recovery time	di/dt = 100A/μs		300		ns

* Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

SGSP474/P475/476
SGSIP474/IP475/IP476
SGSP574/P575/P576

HIGH SPEED SWITCHING APPLICATIONS

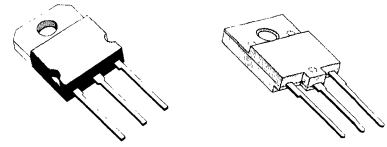
V_{DSS}	$R_{DS\ (on)}$	I_D
350/400 V	0.55 Ω	12 A
450 V	0.7 Ω	12 A

- HIGH VOLTAGE - FOR OFF-LINE SMPS
- HIGH CURRENT - FOR UP TO 350W
- ULTRA FAST SWITCHING - FOR OPERATION AT ⩾100KHz
- EASY DRIVE - REDUCES SIZE AND COST

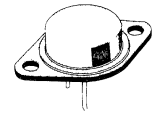
INDUSTRIAL APPLICATIONS:

- SWITCHING MODE POWER SUPPLIES
- MOTOR CONTROLS

N-Channel enhancement mode POWERMOS field effect transistors. Fast switching and easy drive make these POWERMOS transistors ideal for high voltage switching applications.
These applications include electronic welders, switched mode power supplies and sonar equipment. The package range for this devices includes the isolated case ISOWATT218. This provides isolation to 2500V ac, 4000V dc and the creepeage distance requirement of VDE, IEC and UL specifications.

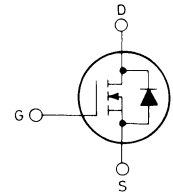


SOT-93 (TO-218) **ISOWATT218**



TO-3

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		SOT-93 ISOWATT218 TO-3	SGSP474 SGSIP474 SGSP574	SGSP475 SGSIP475 SGSP575	SGSP476 SGSIP476 SGSP576	
V_{DS}	Drain-source voltage (V_{GS} = 0)		450	400	350	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)		450	400	350	V
V_{GS}	Gate-source voltage			± 20		V
I_D	Drain current (continuous)	T_c = 25°C		12		A
		at T_c = 100°C		7.6		A
I_{DM}(•)	Drain current (pulsed)			48		A
I_{DLM}	Drain inductive current, clamped			48		A
			SOT-93	ISOWATT218	TO-3	
V_{ISO}	Isolation voltage (DC)			4000		V
P_{tot}	Total dissipation at T_{case} = 25°C		150	50	150	W
	Derating factor		1.2	0.4	1.2	W/°C
T_{stg}	Storage temperature			−55 to 150		°C
T_j	Max. operating junction temperature			150		°C

(•) Pulse width limited by safe operating area.

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25V I_D = 6A	6			mho
C_{iss}	Input capacitance	V_{DS} = 25V f = 1 MHz V_{GS} = 0		1600	2100	pF
C_{oss}	Output capacitance			300	390	pF
C_{rss}	Reverse transfer capacitance			200	260	pF
$C_{D\text{-}HS}$	Drain-Heatsink capacitance	$V_{D\text{-}HS}$ = 25V f = 1 MHz		19	23	pF
SWITCHING						
$t_{d(on)}$	Turn-on time	V_{CC} = 100V I_D = 6A V_i = 10V R_i = 4.7Ω (see test circuit)		20		ns
t_r	Rise time			25		ns
$t_{d(off)}$	Turn off delay time			70		ns
t_f	Fall time			20		ns
SOURCE DRAIN DIODE						
I_{SD}	Source-Drain current				12	A
I_{SDM} (•)	Source-Drain current (pulsed)				48	A
V_{SD}	Forward on voltage	I_{SD} = 12A V_{GS} = 0			1.2	V
t_{on}	Turn-on time	I_{SD} = 12A V_{GS} = 0 di/dt = 25A μs		700		ns
t_{rr}	Reverse recovery time			800		ns

* Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

SGSP478/479
SGSIP478/479
SGSP578/579

HIGH SPEED SWITCHING APPLICATIONS

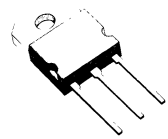
V_{DSS}	$R_{DS\ (on)}$	I_D
500V	0.7 Ω	10A
550V	1 Ω	10A

- HIGH VOLTAGE - 500 FOR OFF-LINE SMPS
- HIGH CURRENT - 10A FOR UP 350W SMPS
- ULTRA FAST SWITCHING - FOR OPERATION AT ⩾ 100KHz
- EASY DRIVE - REDUCES COST AND SIZE

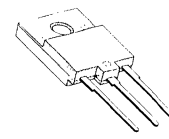
INDUSTRIAL APPLICATION:

- SWITCHING MODE POWER SUPPLIES
- MOTOR CONTROL

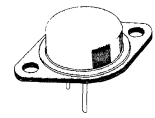
N-Channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications.
Typical applications include switched mode power supplies, uninteruptable power supplies and motor speed control.
The package range for this devices includes the isolated case ISOWATT218. This provides isolation to 2500V ac, 4000V dc and the creepage distance requirement of VDE, IEC, and UL specifications.



SOT-93 (TO-218)

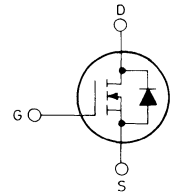


ISOWATT218



TO-3

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		SOT-93 ISOWATT218 TO-3	SGSP478 SGSIP478 SGSP578	SGSP479 SGSIP479 SGSP579	
V_{DS}	Drain-source voltage (V_{GS} = 0)		550	500	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)		550	500	V
V_{GS}	Gate-source voltage		± 20		V
I_D	Drain current (continuous) T_c = 25°C		10		A
	at T_c = 100°C		6.3		A
I_{DM}(•)	Drain current (pulsed)		40		A
I_{DLM}	Drain inductive current, clamped		40		A
		SOT-93 ISOWATT218		TO-3	
V_{ISO}	Isolation voltage (DC)		4000		V
P_{tot}	Total dissipation at T_{case} = 25°C	150	50	150	W
	Derating factor	1.2	0.4	1.2	W/°C
T_{stg}	Storage temperature		−55 to 150		°C
T_j	Max. operating junction temperature		150		°C

(•) Pulse width limited by safe operating area.

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on time	V_{CC} = 250V I_D = 5A		25		ns
t_r	Rise time	V_i = 10V R_i = 10Ω		30		ns
$t_{d(off)}$	Turn off delay time	(see test circuit)		80		ns
t_f	Fall time			20		ns
SOURCE DRAIN DIODE						
I_{SD}	Source-Drain current				10	A
I_{SDM} (•)	Source-Drain current (pulsed)				40	A
V_{SD}	Forward on voltage	I_{SD} = 10A V_{GS} = 0			1.15	V
t_{on}	Turn-on time	I_{SD} = 10A V_{GS} = 0		75		ns
t_{rr}	Reverse recovery time	di/dt = 100A/μs		500		ns

* Pulsed: Pulse duration = 300/μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

2N7056

ADVANCE DATA

HIGH SPEED SWITCHING APPLICATIONS

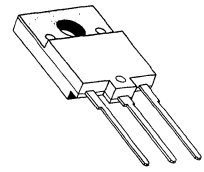
V_{DSS}	$R_{DS\ (on)}$	I_D
200V	0.100Ω	19A

- FULLY ISOLATED PACKAGE
- 200 VOLTS - FOR SMPS UPS AND DC/DC CONVERTERS
- ULTRA FAST SWITCHING
- EASY DRIVE - REDUCES EQUIPMENT SIZE AND COST

INDUSTRIAL APPLICATIONS:

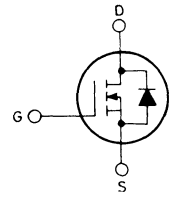
- DC/DC CONVERTERS
- MOTOR CONTROLS
- ROBOTICS

N-Channel enhancement mode POWER MOS field effect transistors. Easy drive, very fast switching times and simple mounting make these POWER MOS transistors ideal for high speed switching applications in a wide range of equipment.
The ISOWATT218 package requires only simple single hole mounting and provides isolation to 2500V ac, 4000V dc. and meets with the creepage distance requirements of VDE, IEC, and UL specifications. The package thermal characteristics are optimised to provide the best isolation with excellent thermal coupling.



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage (V_{GS} = 0)	200	V
V_{DGR}	Drain-gate voltage (R_{GS} = 1 MΩ)	200	V
I_D	Drain current (continuous) T_c = 25°C	±19	A
	T_c = 100°C	±12	A
I_{DM}(•)	Drain current (pulsed)	±120	A
V_{GS}	Gate-source voltage	±40	V
P_{tot}	Total dissipation at $T_c \leqslant 25°C$	70	W
	Total dissipation at T_c = 100°C	28	W
Junction to case - linear derating factor		0.56	W/°C
Junction to ambient - linear derating factor		0.029	W/°C
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature	150	°C
Lead Temperature - 1/16" from case for 10s		300	°C

(•) Pulse width limited by safe operating area.

This is advanced information on a new product in development or undergoing evaluation. Details are subject to change without notice.

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on time	V_{DD} = 750V I_D = 16A		25	35	ns
tr	Rise time	V_{gen} = 10V R_g = 5Ω		60	100	ns
$t_{d(off)}$	Turn off delay time	R_i = 4.5Ω		85	125	ns
t_f	Fall time			38	100	ns
SOURCE DRAIN DIODE						
I_{SD}	Source-Drain current	T_c = 100°C			19	A
					12	A
$I_{SDM\ (\bullet)}$	Source-Drain current (pulsed)				120	A
V_{SD}*	Forward on voltage	V_{GS} = 0 I_{SD} = 28A		1.6	2.0	V
t_{rr}	Reverse recovery	I_{SD} = 19A di/dt = 100A/μs		150	400	ns

* Pulsed: Pulse duration = 300μs, duty cycle 2%

(•) Pulse width limited by safe operating area

2N7059

ADVANCE DATA

HIGH SPEED SWITCHING APPLICATIONS

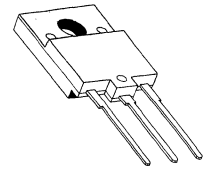
V_{DSS}	$R_{DS\ (on)}$	I_D
500V	0.45Ω	8A

- FULLY ISOLATED PACKAGE
- HIGH VOLTAGE - FOR OFF-LINE SMPS
- HIGH CURRENT - 8A FOR UP TO 1200W SMPS
- ULTRA FAST SWITCHING - FOR OPERATION AT ⩾ 100KHz
- EASY DRIVE - REDUCES EQUIPMENT SIZE AND COST

INDUSTRIAL APPLICATIONS:

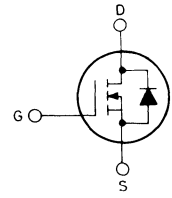
- SWITCHING MODE POWER SUPPLIES
- MOTOR CONTROLS

N-Channel enhancement mode POWER MOS field effect transistors. Easy drive, very fast switching times and simple mounting make these POWER MOS transistors ideal for high speed switching applications in a wide range of equipment.
The ISOWATT218 package requires only simple single hole mounting and provides isolation to 2500V ac, 4000V dc. and meets with the creepage distance requirements of VDE, IEC, and UL specifications. The package thermal characteristics are optimised to provide the best isolation with excellent thermal coupling.



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage (V_{GS} = 0)	500	V
V_{DGR}	Drain-gate voltage (R_{GS} = 1 MΩ)	500	V
I_D	Drain current (continuous) T_c = 25°C	±8	A
	T_c = 100°C	±5	A
I_{DM}(•)	Drain current (pulsed)	±52	A
V_{GS}	Gate-source voltage	±40	V
P_{tot}	Total dissipation at T_c ⩽ 25°C	70	W
	Total dissipation at T_c = 100°C	28	W
Junction to case - linear derating factor		0.56	W/°C
Junction to ambient - linear derating factor		0.029	W/°C
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature	150	°C
Lead Temperature - 1/16'' from case for 10s		300	°C

(•) Pulse width limited by safe operating area.

This is advanced information on a new product in development or undergoing evaluation. Details are subject to change without notice.

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on time	V_{DD} = 210V I_D = 7A		25	40	ns
tr	Rise time	V_{gen} = 10V R_g = 5Ω		25	50	ns
$t_{d(off)}$	Turn off delay time	R_i = 30Ω		75	150	ns
t_f	Fall time			31	70	ns
SOURCE DRAIN DIODE						
I_{SD}	Source-Drain current	T_c = 100°C			8	A
$I_{SDM\ (\bullet)}$	Source-Drain current (pulsed)	T_c = 100°C			5	A
					52	A
V_{SD}*	Forward on voltage	V_{GS} = 0 I_{SD} = 12A		1.2	1.5	V
t_{rr}	Reverse recovery	I_{SD} = 8A di/dt = 100A/μs		400	600	ns

* Pulsed: Pulse duration = 300μs, duty cycle 2%
(•) Pulse width limited by safe operating area

SGS Systems Division

GS-D200

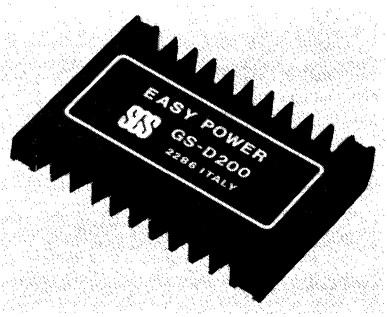
SWITCH MODE BIPOLAR STEPPER MOTOR DRIVER MODULE

The GS-D200 is a complete controller and driver for bipolar stepper motors that directly interfaces a microprocessor and two phase permanent magnet motors.

The motor current is controlled in a chopping mode up to 2 A. High flexibility in use is provided by GS-D200 that, furthermore, reduces the burden on the microprocessor and simplifies the software development in a complete microprocessor controlled stepper motor system.

FEATURES

- No external component required
- Normal, wave, half step drive capability
- Inputs TTL/CMOS compatible
- Chopper regulation of motor current
- Programmable motor current (2 A max)
- Wide voltage range (10-46 V)
- Selectable slow/fast current decay
- Synchronization for multiple application
- Remote inhibit/enable
- Home position indicator
- Overtemperature protection



Order Number: GS-D200

ABSOLUTE MAXIMUM RATINGS

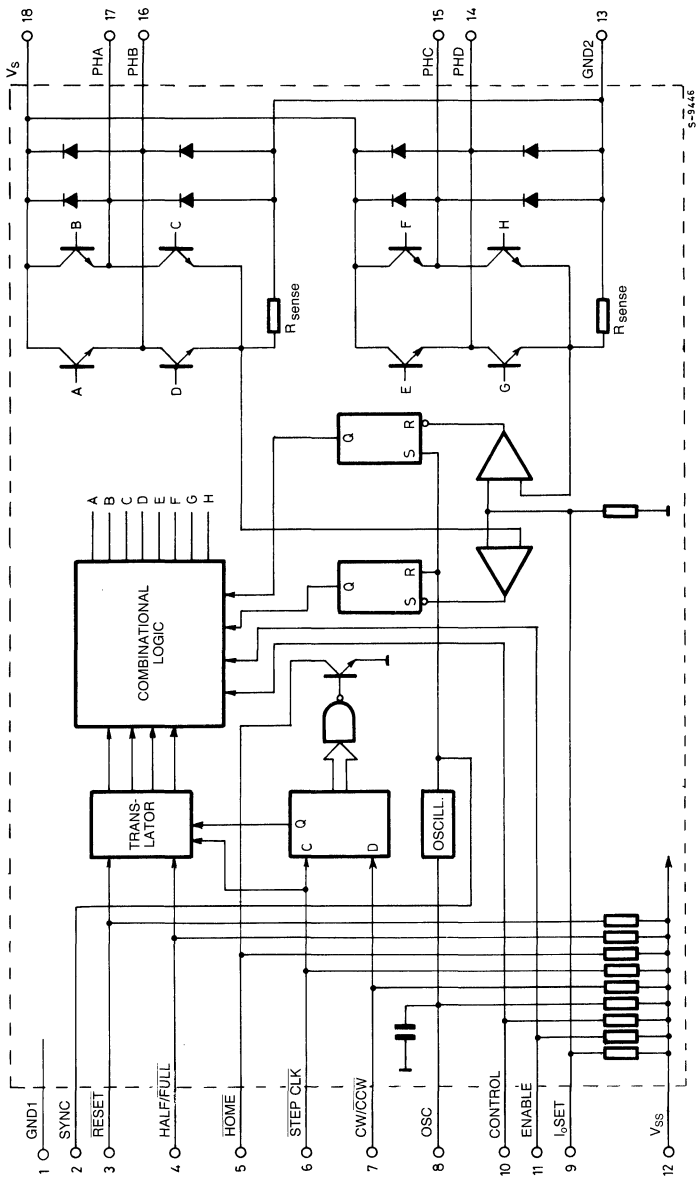
V_s	Supply voltage (pin 18)	48 V
V_{ss}	Supply voltage (pin 12)	7 V
I_o	Peak output current	2 A
T_{stg}	Storage temperature range	−40 to + 105°C
T_{cop}	Operating case temperature range	−20 to + 85°C

Recommended maximum operating input voltage is 46 V.

THERMAL DATA

$R_{th\ (c\text{-}a)}$ case-ambient thermal resistance	Max	5.0 °C/W

EQUIVALENT BLOCK DIAGRAM OF GS-D200



PIN FUNCTIONS (Continued)

PIN	FUNCTION
14—D	Phase D output
15—C	Phase C output
16—B	Phase B output
17—A	Phase A output
18—V_s	Module supply voltage. Maximum voltage must not exceed 46 V.

ELECTRICAL CHARACTERISTICS (T_{amb} =25°C unless otherwise specified)

	Parameter	Test Conditions	Min	Typ	Max	Unit
V_s	Supply Voltage	Pin 18	10		46	V
V_{ss}	Supply Voltage	Pin 12	4.75	5	5.25	
I_s	Quiescent Supply Current	Pin 18 I_{out} =0 V_s =42V		15	20	mA
I_{ss}	Quiescent Supply Current	Pin 12. All inputs high I_{out} =0 V_{ss} =5V		60		mA
V_i	Input Voltage	Pin 3, 4, 6, 7, 10 low high	 2.0		0.8 V_{ss}	V V
I_i	Input Current	Pin 3, 4, 6, 7, 10 V_i =low V_i =high			0.6 10	mA μA
V_{en}	Enable Input Voltage	Pin 11 low high	 2.0		0.8 V_{ss}	V V
I_{en}	Enable Input Current	Pin 11 V_{en} =low V_{en} =high			0.6 10	mA μA
V_{home}	Home Output Voltage	Pin 5 low I_{home} =5mA high			0.4 V_{ss}	V V
V_{sat}	Source Saturat. Voltage	Pin 14, 15, 16, 17 I_o =1A			1.8	V
V_{sat}	Sink Saturat. Voltage	Pin 14,15,16,17 I_o =1A			1.8	V
f_c	Chopper Freq.			17		KHz

MODULE OPERATION

The GS-D200 is a complete bipolar stepper motor driver that incorporates all the small signal and power functions to directly interface a microprocessor and a two phase permanent magnet motor (see the typical application). Very few information must be delivered by the microprocessor to the module:

— step clock
— direction (clockwise or counterclockwise)
— mode (half or full step)
— reset and enable
— current decay (slow or fast)

Based on this information, the module generates the proper four phases sequence to directly drive a two phase bipolar motor. Therefore the GS-D200 greatly simplifies the task of the microprocessor and of the system programmer.

No external component is needed to operate the GS-D200. However, to add flexibility in use, some internally set functions can be modified externally, like the maximum current flowing through the motor windings and the switching frequency of the current chopper, by addition of few inexpensive passive components (resistor and capacitor).

If any of logic input is left open, the module forces them to high level.

The GS-D200 is housed in a metal case that provides heatsink and shielding against radiated EMI. The thermal resistance case to ambient is about 5 °C/W. This means that for each watt of internal power dissipation the case temperature is + 5°C above ambient temperature. It is reccomended to keep the case temperature below 85°C in operating conditions.

According to ambient temperature and/or to power dissipation, an additional heatsink may be required: the mounting of optional heatsink is made easy by the four holes provided on the top of the metal case.

The GS-D200 incorporates a thermal protection that switches off the power stages when the junction temperature of active components reaches 150 °C.

To keep the power dissipation to a minimum, two level supply voltages must be applied to the module: 5 V for logic functions and V_s from 10 to 46 V for power section.

A2 - TWO-PHASE-ON or NORMAL DRIVE

This mode gives the highest torque since two windings are energized at any given time according to the sequence (for clockwise rotation)

AB & CD; CD & BA; BA & DC; DC & AB

Fig. 3 shows the sequence and the corresponding position of the rotor.

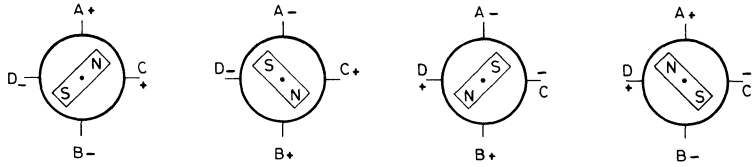


Fig. 3 - Two-phase-on (normal mode) drive

S-5953

A3 - HALF STEP DRIVE

This sequence halves the effective step angle of the motor but gives a less regular torque being one winding or two windings alternatively energized. Eight steps are required for a complete revolution of the rotor.
The sequence is:

AB; AB & CD; CD; CD & BA; BA; BA & DC; DC; DC & AB

as shown in fig. 4.

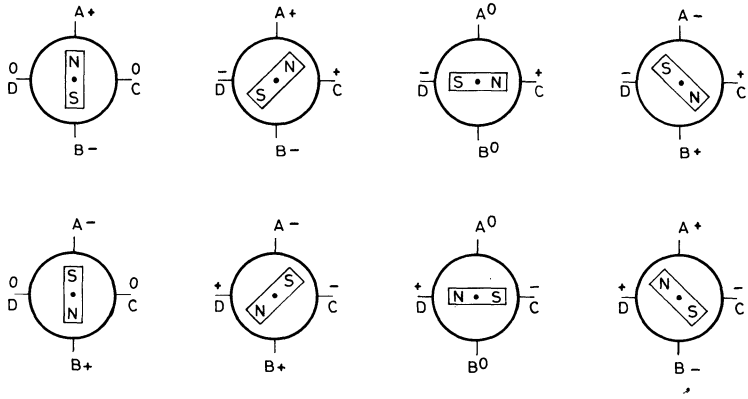


Fig. 4 - Half step sequence.

S-5938

By the configurations of fig. 2,3,4 the motor would have a step angle of 90° (or 45° in half step). Real motors have multiple poles pairs to reduce the step angle to a few degrees but the number of windings (two) and the drive sequence are unchanged.

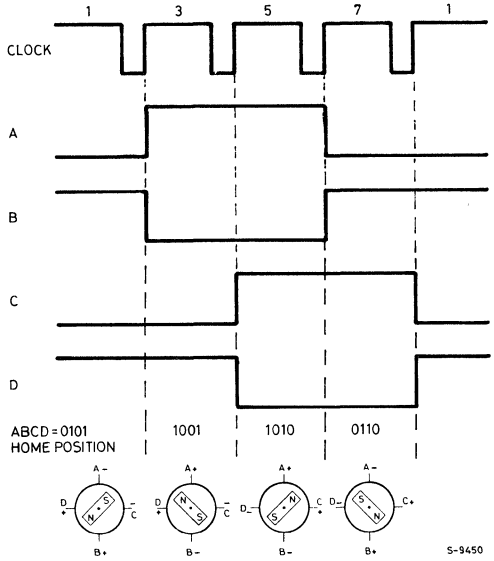


Fig. 6 - Two-phase-on (normal mode) drive

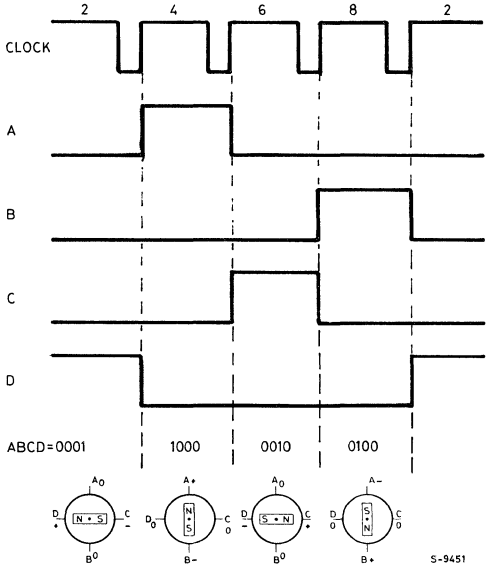


Fig. 7 - One-phase-on (Wave mode) drive.

When the CONTROL input is forced low, the decay is fast as shown in fig. 9.

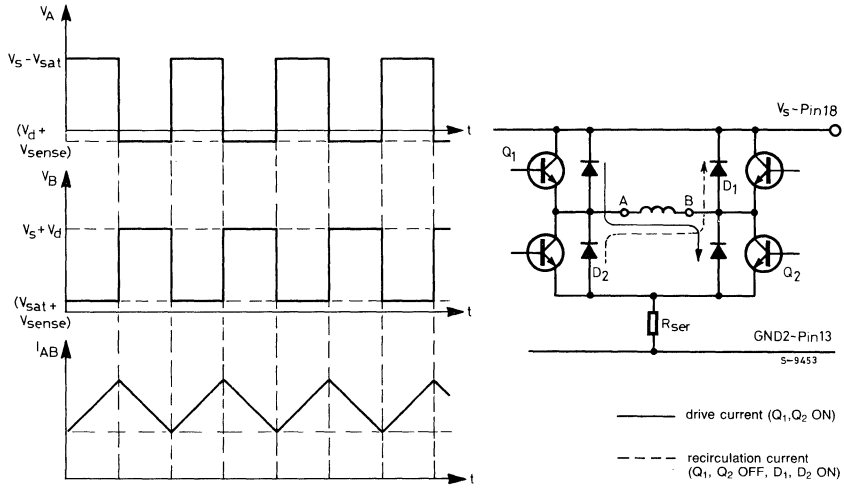


Fig. 9 - Chopper control with fast decay

The CONTROL input is provided on GS-D200 to allow maximum flexibility in application.

If the GS-D200 must drive a large motor that does not store much energy in the windings, the chopper frequency must be decreased: this is easily obtained by connecting an external capacitor between OSC pin and GND1.
In these conditions a fast decay (CONTROL LOW) would impose a low average current and the torque could be inadequate. By selecting CONTROL HIGH, the average current is increased thanks to the slow decay.

E - MODULE PROGRAMMING

When no external component is used, the GS-D200 is set at the following conditions:

$$Iout_{peak} \cong 1\ A$$

$$f_c \text{ chopper frequency} \cong 17\ KHz$$

By addition of inexpensive passive components the working conditions can be modified as follows.

Minimum Value of R2 is 10 kΩ.

This current programmability can be used in half step sequence to increase the current when only one phase is on: a more regular torque is so obtained.

E2 - CHOPPER FREQUENCY PROGRAMMING

The chopper frequency is internally set at about 17 KHz. This frequency can be changed by addition of external components as follows.

To increase the chopper frequency a resistor R3 must be connected between OSC pin and V_{ss} as shown in fig. 12.

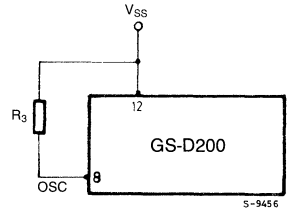


Fig. 12 - Chopper frequency increase

The new chopper frequency is given by:

$$f_c = 17\ (1 + \frac{18}{R3})\ \text{KHz} \quad \text{where R3 is in K}\Omega$$

For example, if $V_{ss} = 5$ V and R3 = 18 KΩ, $f_c \cong 34$ KHz

To decrease the chopper frequency a capacitor C must be connected between OSC pin and GND1 as shown in fig. 13.

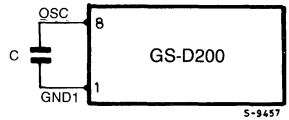


Fig. 13 - Chopper frequency decrease.

The new chopper frequency is given by:

$$f_c = \frac{80.5}{4.7 + C}\ \text{KHz} \quad \text{where C is in nF}$$

For example, if $V_{ss} = 5$ V and C = 4.7nF, $f_c \cong 8.5$ KHz.

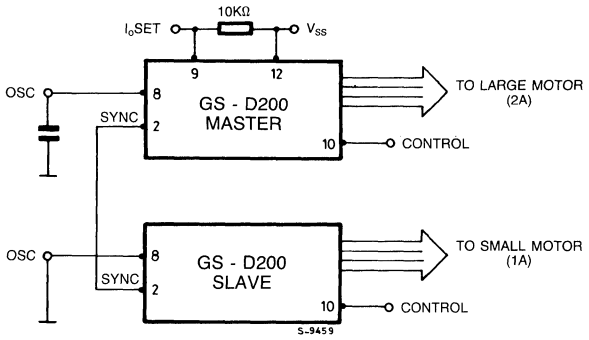


Fig. 15 - Multimotor synchronization. Large and small motors. Slow current decay.

G - THERMAL OPERATING CONDITIONS

In many cases the GS-D200 module does not require any additional cooling because the dimensions and the shape of the metal box are studied to offer the minimum possible thermal resistance case-to-ambient for a given volume.

It should be remembered that the GS-D200 module is a power device and, depending on ambient temperature, an additional heath-sink or forced ventilation or both may be required to keep the unit within safe temperature range. ($T_{case_{max}} < 85°C$ during operation).

The concept of maximum operating ambient temperature is totally meaningless when dealing with power components because the maximum operating ambient temperature depends on how a power device is used.

What can be unambiguously defined is the case temperature of the GS-D200 module.

To calculate the maximum case temperature of the module in a particular applicative environment the designer must know the following data:

— Input voltage
— Motor phase current
— Motor phase resistance
— Maximum ambient temperature

From these data it is easy to determine whether an additional heath-sink is required or not, and the relevant size i.e. the thermal resistance.

The step by step calculation is shown for the following example:

$V_{in} = 40$ V, $I_{phase} = 1$ A, Rph Phase resistance = 10 Ω, Max. $T_{amb} = 50$ °C

G1. Calculate the power dissipated by the indexer logic and the level shifter (see electrical characteristics):

$$P_{logic} = (5\ V \cdot 60\ mA) + (40\ V \cdot 20\ mA) = 1.1\ W$$

G4.5 HALF STEP. The power sequence, one phase ON, two phase ON forces the power dissipation to be 1.5 times higher than in WAVE MODE when the motor is running. In stall condition the worst case for power dissipation is with two phase ON i.e. a power dissipation as in NORMAL MODE.

The following table summarizes the power dissipations of the output power stage of the GS-D200 when running for this example:

	Wave	Normal	Half Step
Fast Decay	3.19 W	6.38 W	6.38 W
Slow Decay	3.30 W	6.60 W	6.60 W

G5. Calculate the total power dissipation for the GS-D200:

$$P_{tot} = P_{logic} + P_{pw}$$

In this example, for slow decay and normal mode

$$P_{tot} = 1.1 + 6.6 = 7.7 \text{ W}$$

G6. The case temperature can now be calculated:

$$T_{case} = Tamb + (P_{tot} \cdot R_{th}) = 55 + (7.7 \cdot 5) = 93.5 \text{ °C}$$

G7. If the calculated case temperature exceedes the maximum allowed case temperature, as in this example, an external heat-sink is required and the thermal resistance can be calculated according to:

$$Rth_{tot} = \frac{T_{cmax} - Tamb}{P_{tot}} = \frac{85 - 55}{7.7} = 3.9 \text{ °C/W}$$

and then

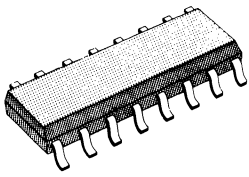
$$Rth_{hs} = \frac{Rth - Rth_{tot}}{Rth - Rth_{tot}} = \frac{5 \cdot 3.9}{5 - 3.9} = 17.7 \text{°C/W}$$

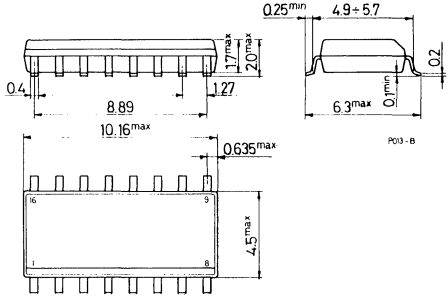
The following table gives the thermal resistance of some commercially available heath-sinks that fit on the GS-D200 module.

Manufacturer	Part Number	R_{th} (°C/W)	Mounting
Thermalloy	6177	3	Horizontal
Thermalloy	6152	4	Vertical
Thermalloy	6111	10	Vertical
Fischer	SK18	3	Vertical
Assman	V5440	4	Vertical
Assman	V5382	4	Horizontal

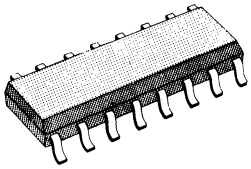
PACKAGES

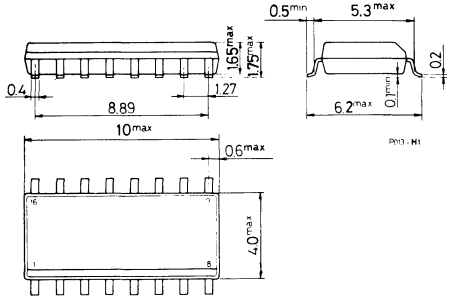
SO-16



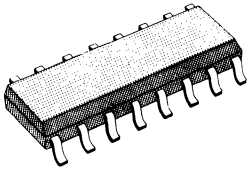


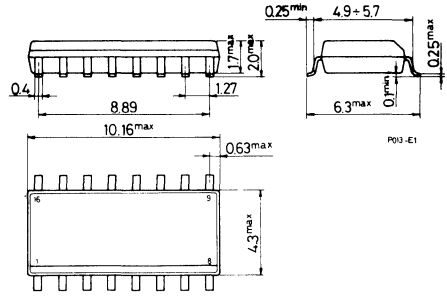
SO-16 Jedec



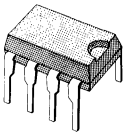


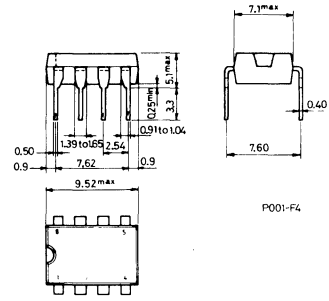
SO-16P



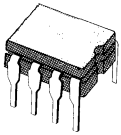


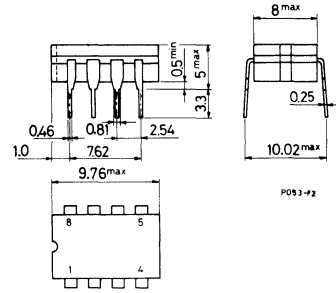
8 lead Plastic Minidip



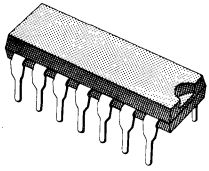


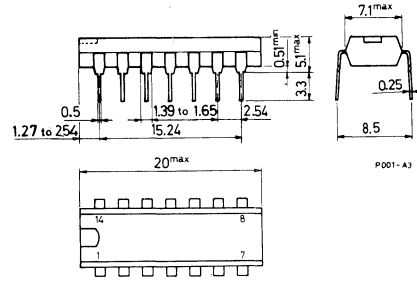
8 lead Ceramic Minidip



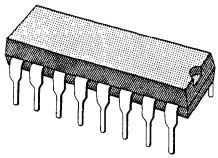


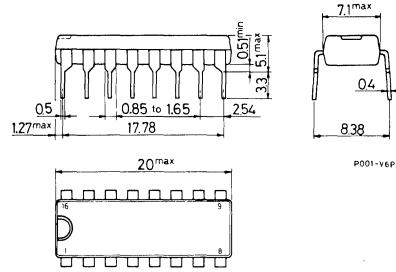
14 lead Plastic Dip



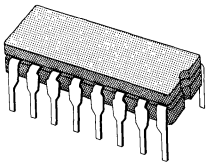


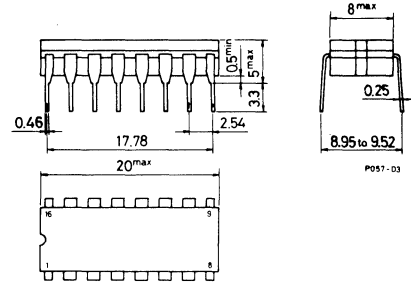
16 lead Plastic Dip (V6P2)
8 + 8 lead Powerdip (V6P2)
12 + 2 + 2 lead Powerdip (V6P2)



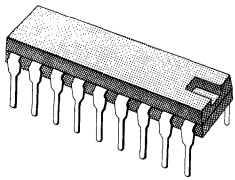


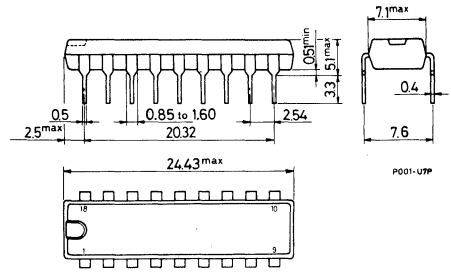
16-lead Ceramic Dip



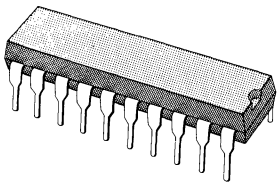


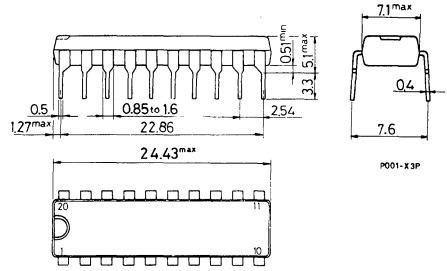
18 lead Plastic Dip (0.4)
9 + 9 lead Powerdip



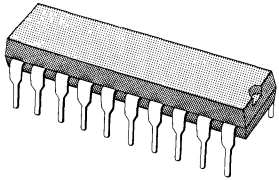


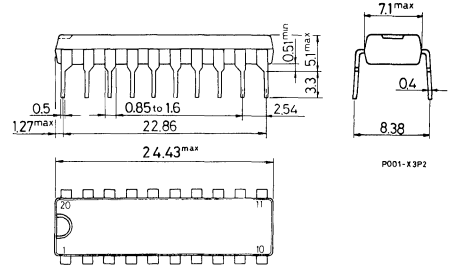
20 lead Plastic Dip (0.4)
16 + 2 + 2 lead Powerdip



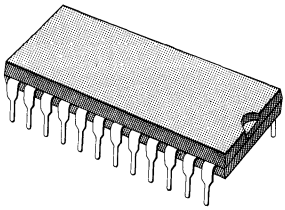


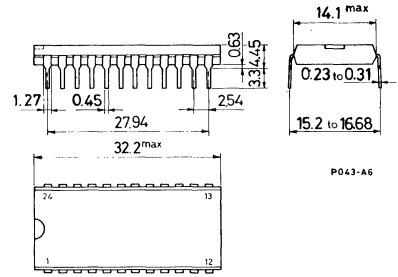
20 lead Plastic Dip (X3P2)



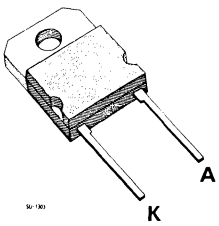


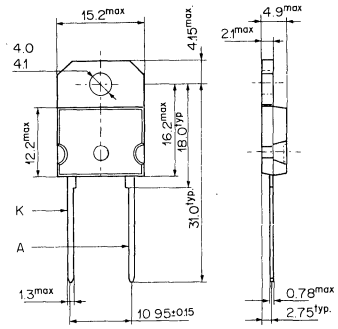
24 lead Plastic Dip



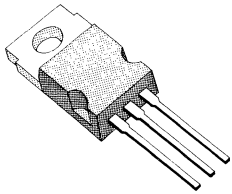


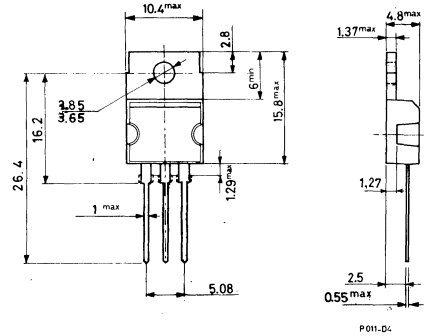
DIOWATT2



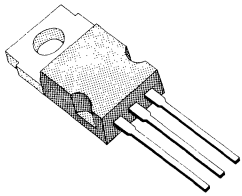


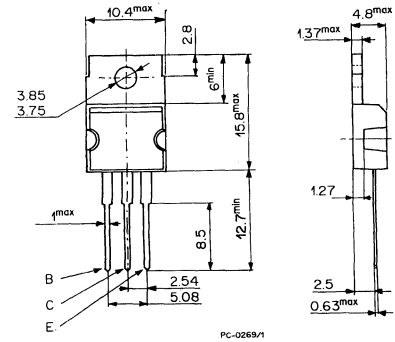
TO-220 (ICs)



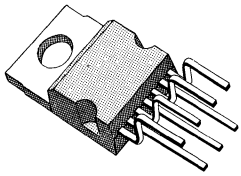


TO-220 (Discrete Power)

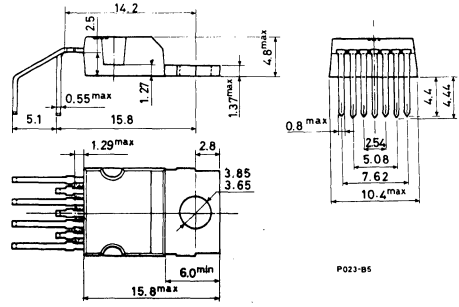




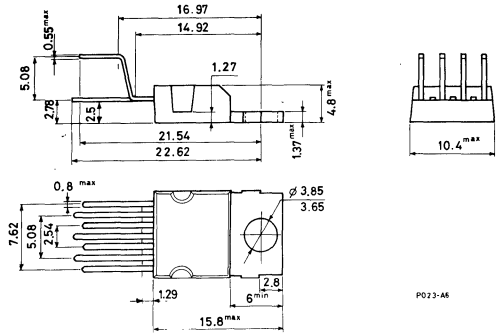
HEPTAWATT



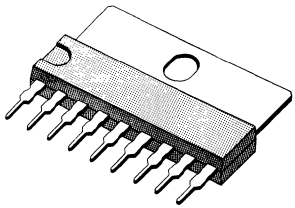
Horizontal Version

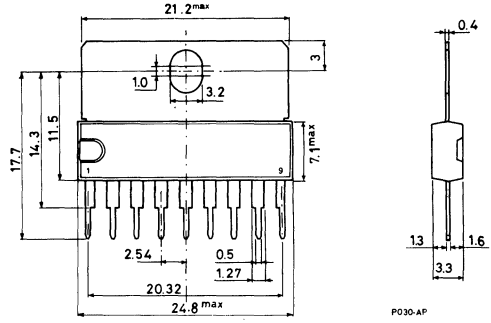


Vertical Version

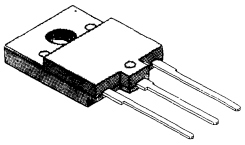


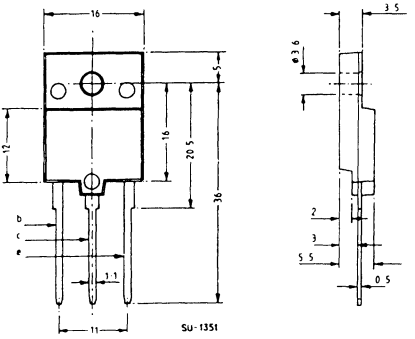
SIP-9



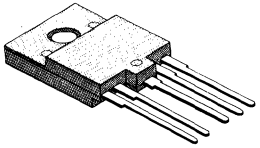


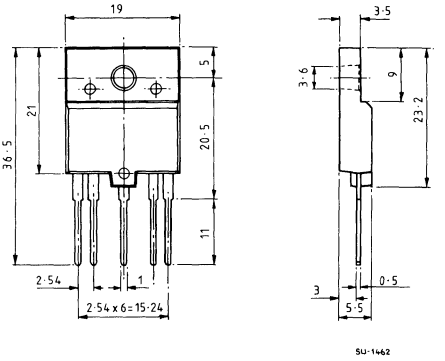
ISOWATT218



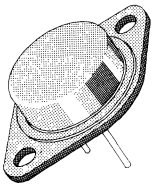


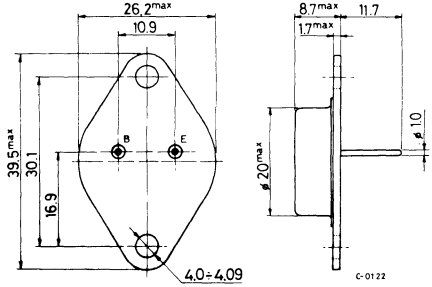
ISOWATT5





TO-3





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