

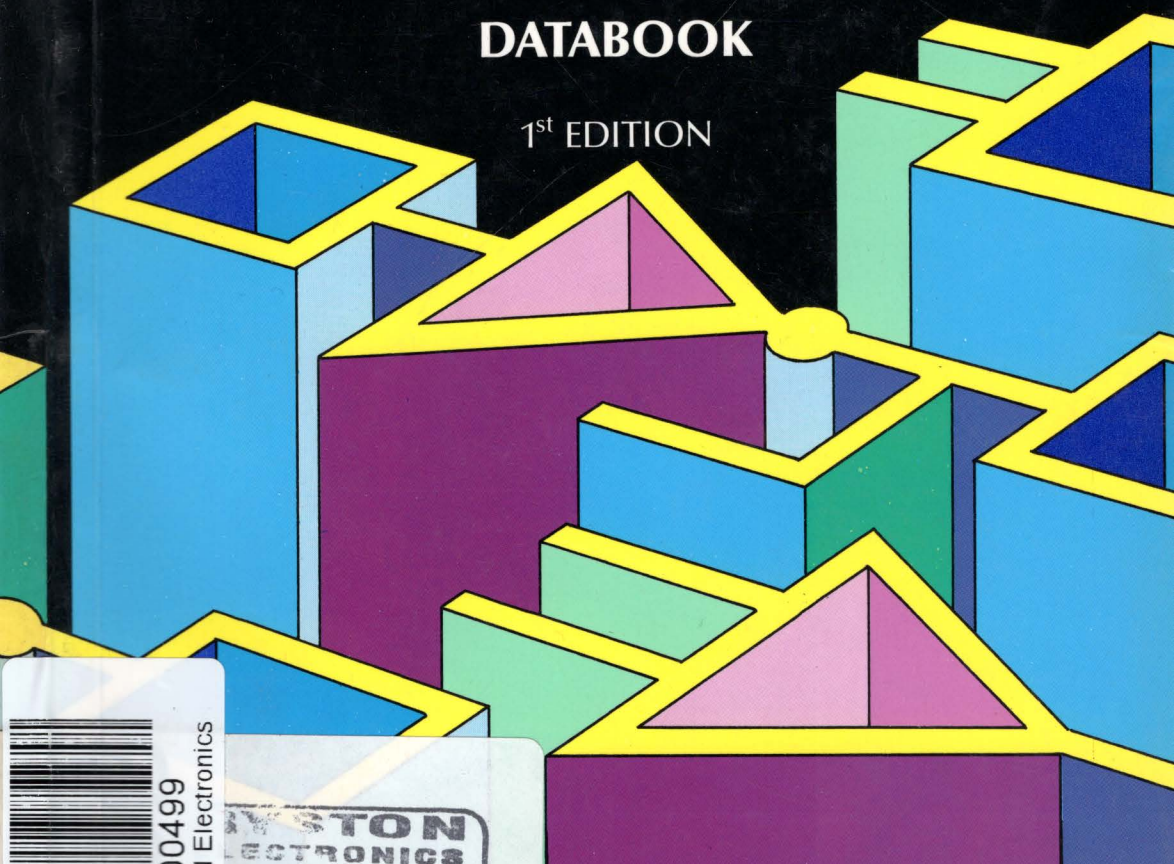


INNOVATIVE  
SILICON  
TECHNOLOGY

# ISB9000 SERIES CHANNELLESS LOGIC ARRAYS

## DATABOOK

1<sup>st</sup> EDITION



**RYSTON**  
**ELECTRONICS**  
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member of the SGS-THOMSON Group of Companies.

**SGS-THOMSON**  
MICROELECTRONICS

10025

# **ISB9000 SERIES**

## **CHANNELLESS LOGIC ARRAYS**

**DATABOOK**

**1<sup>st</sup> EDITION**

**September 1989**

**USE IN LIFE SUPPORT DEVICES FOR SYSTEMS MUST BE EXPRESSLY AUTHORIZED BY INNOVATIVE SILICON TECHNOLOGY.**

OUT PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER OF INNOVATIVE SILICON TECHNOLOGY.

1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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# INTRODUCTION

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## THE COMPANY

Innovative Silicon Technology was formed in May 1986 to meet the growing demand for User Specific Integrated Circuits.

As a member of the SGS-THOMSON Microelectronics Group the company enjoys the technological back-up and assured silicon foundry facilities of the parent company.

At the same time, a dedicated structure allows the company to meet the needs of a service-orientated sector, offering customers fast access to the most advanced processes, technologies and services.

## THE PRODUCT

The ISB9000 Series is a high performance Channelless HCMOS Logic Array intended for general purpose applications. It is manufactured with an oxide isolated 1.5 micron silicon gate process using double level metallization.

Ranging in complexity from approximately 300 to 20000 total equivalent gates, propagation delays for a 2-input NAND gate plus interconnect are 0.7 nanoseconds.

This series offers high gate utilization while enhancing routability thanks to the absence of predefined channels for intercell wiring. Instead the architecture allows active transistor area to merge with interconnection paths giving the user the benefits of reduced capacitance and larger transistor geometries for increased performance.

Additional information on the ISB9000 Series or other Innovative Silicon Technology products and services can be obtained from your nearest Sales Office.

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# **PRIMITIVES AND MULTICELLS**

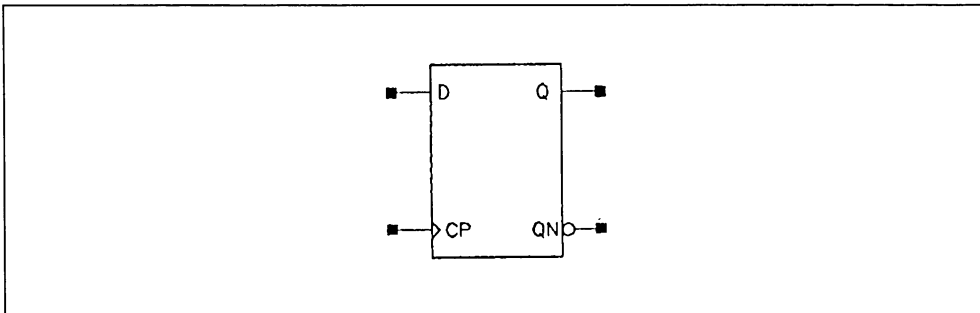
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This page explains how to read the ISB9000 DATABOOK using the model shown on the facing page.

- 1** The cell names appear on the outside corner of each page to facilitate searching for a cell.
- 2** The cell description appears in the title block.
- 3** The logic symbol is given for each cell.
- 4** The truth table is shown for each cell.
- 5** The propagation delay characteristics for various fanouts (or unit load for output buffers) are shown so that critical path delays can be estimated. These values are based on normal conditions and larger fanouts or capacitance can be extrapolated. Delays are measured at CMOS levels unless otherwise stated.
- 6** The cell usage is shown for implementation in a design.
- 7** The input load is expressed in unit loads. The maximum output load/drive capability is expressed in unit loads for core cells (and the core parts of bidirectional pad cells) and in picofarads (pF) for output cells.
- 8** The coding sequence is given for the Mozart Simulator. The sequence for other simulators can be derived from this.

<b>FD1</b>	<b>D FLIP FLOP</b> <b>2</b>	<b>FD1</b> <b>1</b>
------------	-----------------------------	---------------------

**SYMBOL** **3**



**TRUTH TABLE** **4**

Input		Output	
D	CP	Q	QN
L		L	H
H		H	L

**CHARACTERISTICS** **6**

		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
CP to QN	t <sub>PHL</sub>	3.0	3.2	3.3	3.4	3.9	4
	t <sub>PLH</sub>	3.2	3.4	3.5	3.6	4.1	

**7**

Input Load		Output Drive	
D	CP	Q	QN
1	1	20	20

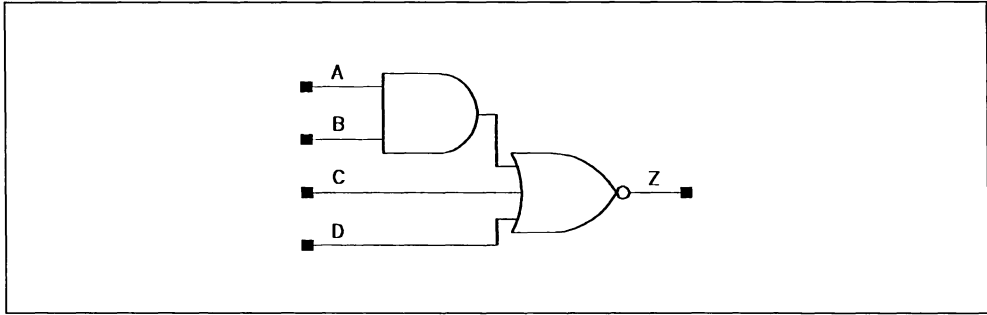
**8**

Coding Sequence	(q,qn;d,cp)
-----------------	-------------



<b>AO1</b>	<b>DOUBLE AND2 INTO NOR2</b>	<b>AO1</b>
------------	------------------------------	------------

**SYMBOL**



**TRUTH TABLE**

Input				Output
A	B	C	D	Z
H	H	X	X	L
X	X	X	H	L
X	X	H	X	L
X	L	L	L	H
L	X	L	L	H

**CHARACTERISTICS**

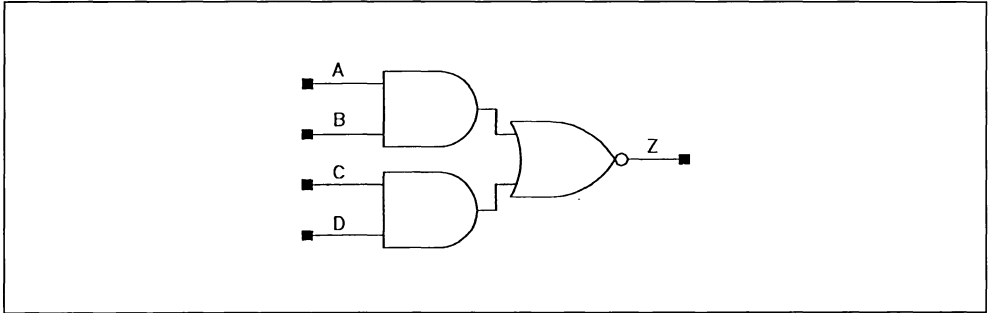
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A,B,C,D to Z	t <sub>PHL</sub>	1.10	1.39	1.67	1.96	3.11	2
	t <sub>PLH</sub>	2.28	2.87	3.46	4.05	6.42	

Input Load				Output Drive
A	B	C	D	Z
1	1	1	1	18

Coding Sequence	(z;a,b,c,d)
-----------------	-------------

<b>AO2</b>	<b>DOUBLE AND2 INTO NOR2</b>	<b>AO2</b>
------------	------------------------------	------------

**SYMBOL**



**TRUTH TABLE**

Input				Output
A	B	C	D	Z
A	B	C	D	Z
H	H	X	X	L
X	X	H	H	L
L	X	L	X	H
X	L	L	X	H
L	X	X	L	H
X	L	X	L	H

**CHARACTERISTICS**

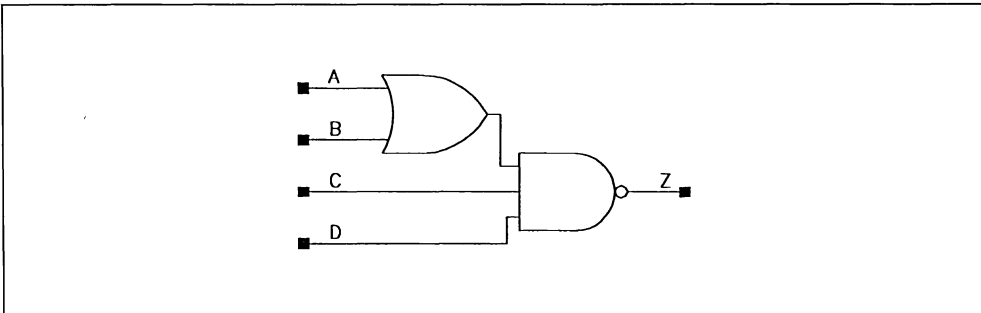
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A,B,C,D to Z	t <sub>PHL</sub>	0.93	1.21	1.49	1.77	2.89	2
	t <sub>PLH</sub>	1.06	1.38	1.70	2.02	3.30	

Input Load				Output Drive
A	B	C	D	Z
1	1	1	1	18

<b>Coding Sequence</b>	(z,a,b,c,d)
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<b>AO3</b>	<b>OR2 INTO NAND3</b>	<b>AO3</b>
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**SYMBOL**



**TRUTH TABLE**

Input				Output
A	B	C	D	Z
H	X	H	H	L
X	H	H	H	L
L	L	X	X	H
X	X	L	X	H
X	X	X	L	H

**CHARACTERISTICS**

	Propagation Delay (ns)					Cell Usage
	FO 1	FO 2	FO 3	FO 4	FO 8	
A,B,C,D to Z — t <sub>PHL</sub>	1.45	1.79	2.13	2.47	3.82	2
t <sub>PLH</sub>	1.82	2.26	2.69	3.12	4.85	

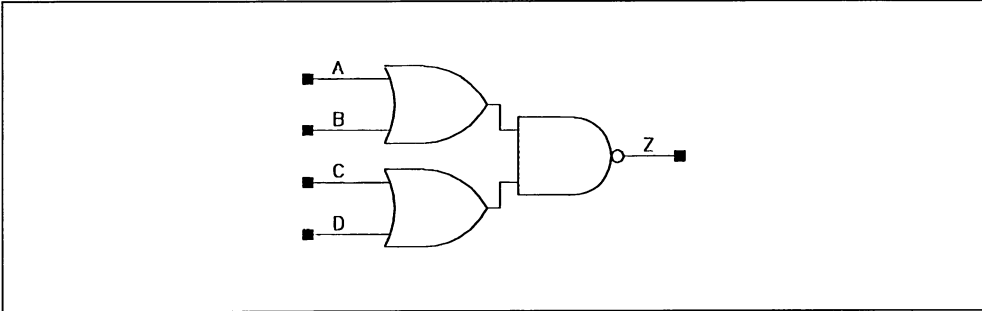
Input Load				Output Drive
A	B	C	D	Z
1	1	1	1	18

Coding Sequence	(z;a,b,c,d)
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<b>AO4</b>	<b>DOUBLE OR2 INTO NAND2</b>	<b>AO4</b>
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**SYMBOL**



**TRUTH TABLE**

Input				Output
A	B	C	D	Z
A	B	C	D	Z
L	L	X	X	H
X	X	L	L	H
H	X	H	X	L
X	H	H	X	L
H	X	X	H	L
X	H	X	H	L

**CHARACTERISTICS**

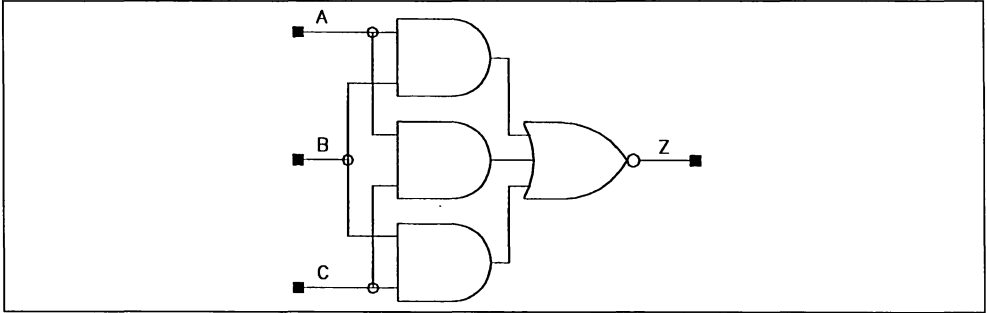
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A,B,C,D to Z	t <sub>PHL</sub>	1.05	1.26	1.48	1.69	2.55	2
	t <sub>PLH</sub>	1.77	2.19	2.60	3.02	4.70	

Input Load				Output Drive
A	B	C	D	Z
1	1	1	1	18

Coding Sequence	(z;a,b,c,d)
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<b>A05</b>	<b>2 OF 3 MAJORITY GATE (INVERTED OUTPUT)</b>	<b>A05</b>
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**SYMBOL**



**TRUTH TABLE**

Input			Output
A	B	C	Z
L	L	X	H
L	X	L	H
X	L	L	H
H	H	X	L
H	X	H	L
X	H	H	L

**CHARACTERISTICS**

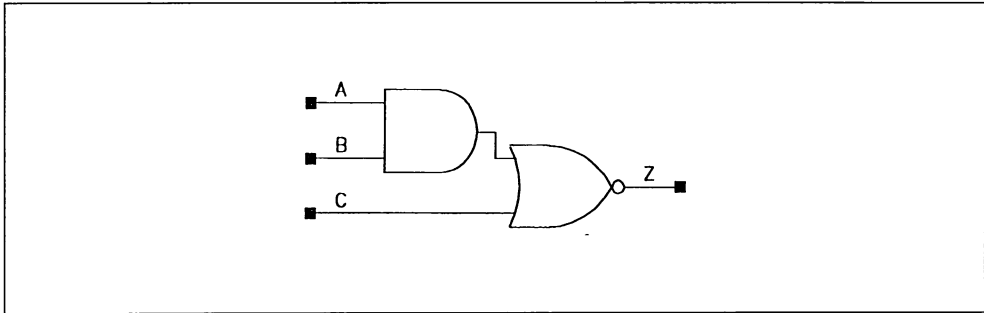
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A,B,C to Z	t <sub>PHL</sub>	1.30	1.55	1.81	2.07	3.10	2
	t <sub>PLH</sub>	1.83	2.25	2.66	3.08	4.76	

Input Load			Output Drive
A	B	C	Z
2	2	2	18

<b>Coding Sequence</b>	(z;a,b,c,)
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<b>A06</b>	<b>AND2 INTO NOR2</b>	<b>A06</b>
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**SYMBOL**



**TRUTH TABLE**

Input			Output
A	B	C	Z
H	H	X	L
X	X	H	L
X	L	L	H
L	X	L	H

**CHARACTERISTICS**

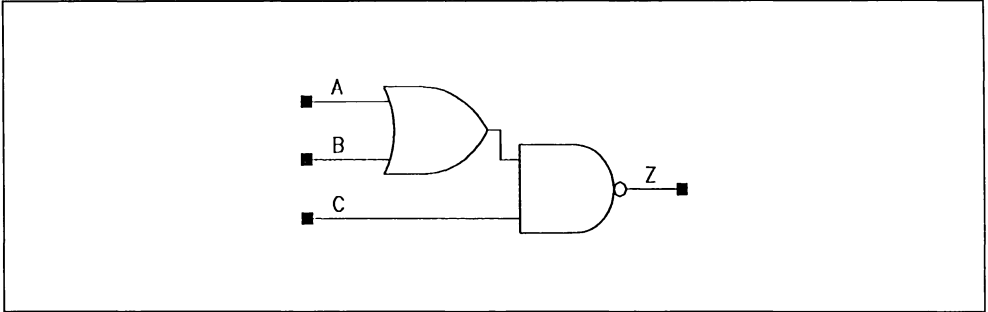
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A,B,C to Z	t <sub>PHL</sub>	0.98	1.26	1.54	1.82	2.94	1
	PLH	1.50	1.91	2.33	2.74	4.40	

Input Load			Output Drive
A	B	C	Z
1	1	1	18

Coding Sequence	(z;a,b,c)
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<b>A07</b>	<b>OR2 INTO NAND2</b>	<b>A07</b>
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**SYMBOL**



**TRUTH TABLE**

Input			Output
A	B	C	Z
X	X	H	L
X	H	H	L
L	L	X	H
X	X	L	H

**CHARACTERISTICS**

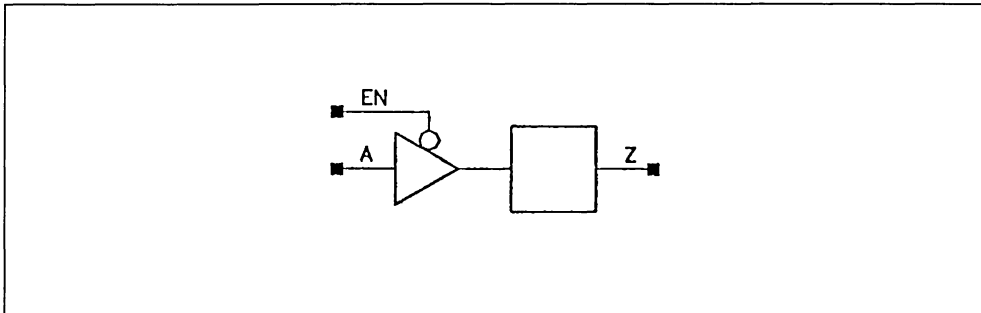
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A,B,C to Z	t <sub>PHL</sub>	1.06	1.32	1.58	1.84	2.89	1
	t <sub>PLH</sub>	1.57	1.99	2.40	2.82	4.50	

Input Load			Output Drive
A	B	C	Z
1	1	1	18

Coding Sequence	(z;a,b,c)
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<b>BTS1</b>	<b>TRISTATE OUTPUT BUFFER (4 mA)</b>	<b>BTS1</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	Hi-Z

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	t <sub>PHL</sub>	8.1	11.9	15.6	17.2	2
	t <sub>PLH</sub>	7.0	11.1	15.1	16.8	

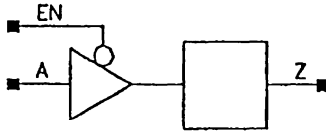
**Note:** Delays for Output are Measured at TTL Level.

Input Load		Output Drive
A	EN	Z
1	2	150

Coding Sequence	(z;a,en)
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<b>BTS14</b>	<b>TRISTATE OUTPUT BUFFER (1 mA)</b>	<b>BTS14</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	Hi-Z

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85		
A to Z	t <sub>PHL</sub>	13.6	28.6	43.6		2
	t <sub>PLH</sub>	13.4	29.4	45.5		

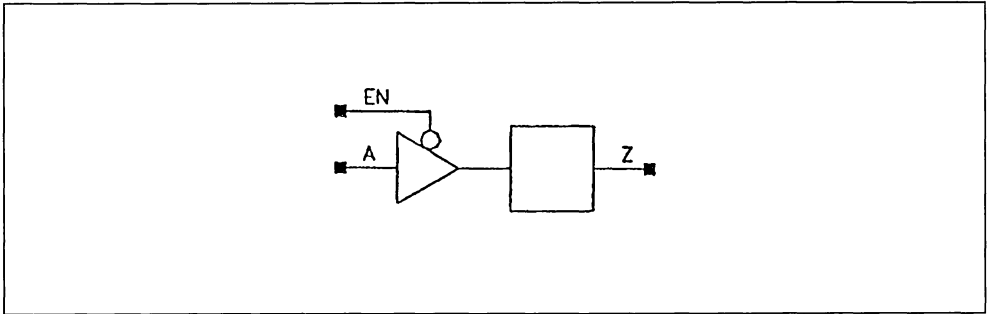
**Note:** Delays for Output are Measured at TTL Level.

Input Load		Output Drive
A	EN	Z
1	2	50

Coding Sequence	(z;a,en)
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<b>BTS18</b>	<b>TRISTATE OUTPUT BUFFER (2 mA)</b>	<b>BTS18</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	Hi-Z

**CHARACTERISTICS**

		Propagation Delay (ns)			Cell Usage
		C-15	C-50	C-85	
A to Z	t <sub>PHL</sub>	9.8	16.9	23.9	2
	t <sub>PLH</sub>	9.4	17.5	25.5	

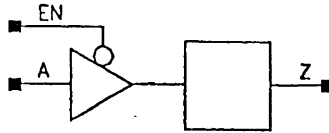
**Note:** Delays for Output are Measured at TTL Level.

Input Load		Output Drive
A	EN	Z
1	2	90

<b>Coding Sequence</b>	(z;a,en)
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<b>BTS2</b>	<b>TRISTATE OUTPUT BUFFER (8 mA)</b>	<b>BTS2</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	Hi-Z

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	t <sub>PHL</sub>	8.1	10.0	12.0	12.8	2
	t <sub>PLH</sub>	6.5	8.5	10.6	11.4	

**Note:** Delays for Output are Measured at TTL Level.

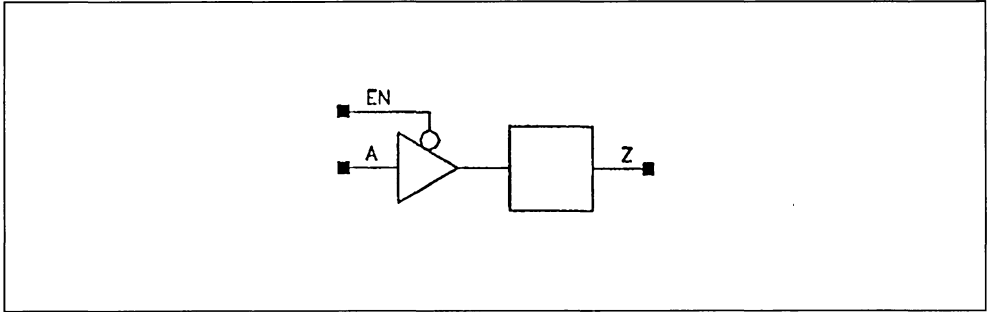
Input Load		Output Drive
A	EN	Z
1	2	240

Coding Sequence	(z;a,en)
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<b>BTS3</b>	<b>TRISTATE OUTPUT BUFFER (16 mA)</b>	<b>BTS3</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	Hi-Z

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	t <sub>PHL</sub>	7.5	8.7	9.8	10.3	4
	t <sub>PLH</sub>	8.1	9.1	10.1	10.6	

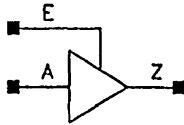
**Note:** Delays for Output are Measured at TTL Level.

Input Load		Output Drive
A	EN	Z
2	4	240

<b>Coding Sequence</b>	(z;a,en)
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<b>BTS4</b>	<b>TRISTATE INTERNAL BUS DRIVER</b>	<b>BTS4</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
E	A	Z
H	L	L
H	H	H
L	X	Hi-Z

**CHARACTERISTICS**

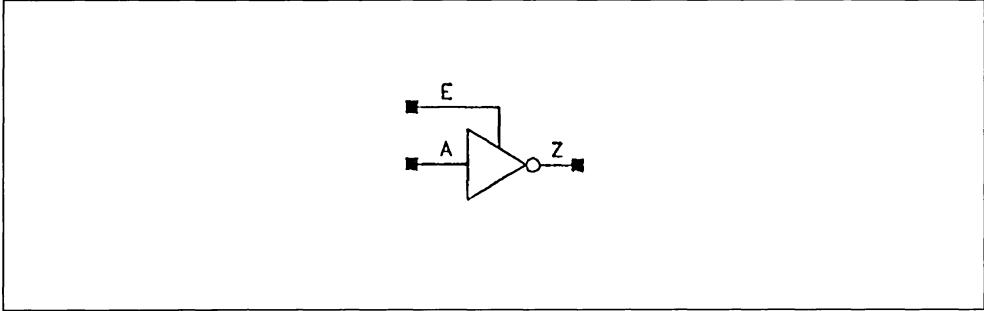
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A,E to Z	t <sub>PHL</sub>	1.4	1.6	1.7	1.8	2.3	3
	t <sub>PLH</sub>	1.3	1.5	1.6	1.8	2.4	

Input Load		Output Drive
A	E	Z
2	2	27

Coding Sequence	(z;a,e)
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<b>BTS5</b>	<b>INVERTING TRISTATE INTERNAL BUS DRIVER</b>	<b>BTS5</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
E	A	Z
H	L	H
H	H	L
L	X	Hi-Z

**CHARACTERISTICS**

		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A to Z	t <sub>PHL</sub>	2.0	2.2	2.3	2.4	2.8	4
	t <sub>PLH</sub>	2.1	2.5	2.7	2.8	3.4	

Input Load		Output Drive
A	E	Z
1	2	27

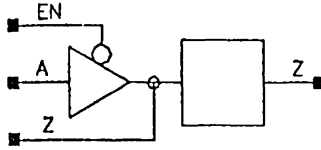
Coding Sequence	(z;a,b,c)
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BTS7

TRISTATE BIDIRECTIONAL BUFFER (4 mA)

BTS7

## SYMBOL



## TRUTH TABLE

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	Hi-Z

## CHARACTERISTICS

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	t <sub>PHL</sub>	7.9	11.2	14.6	16.0	2
	t <sub>PLH</sub>	6.8	10.4	14.1	15.6	

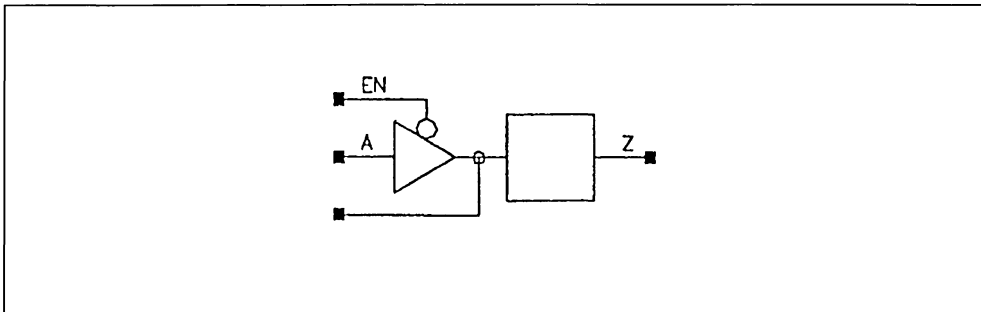
Note: Delays for Output are Measured at TTL Level.

Input Load		Output Drive
A	EN	Z
1	2	150

Coding Sequence	(z;a,en)
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<b>BTS7L</b>	<b>TRISTATE BIDIRECTIONAL BUFFER WITH LOW POWER OUTPUT (4 mA)</b>	<b>BTS7L</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	Hi-Z

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	$t_{PHL}$	7.9	11.2	14.6	16.0	2
	$t_{PLH}$	6.8	10.4	14.1	15.6	

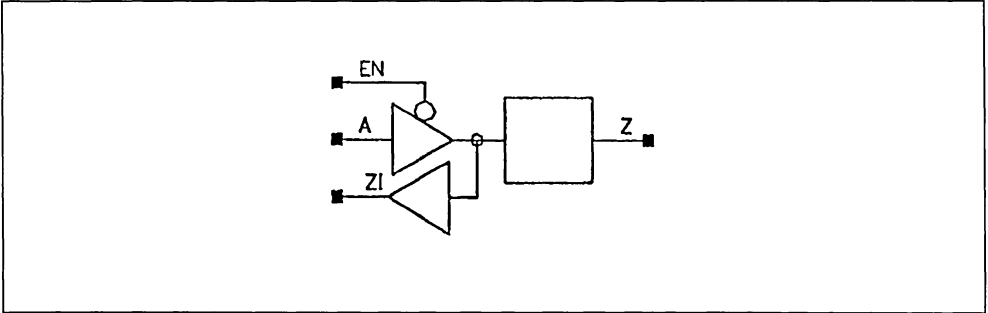
Note: Delays for Output are Measured at TTL Level.

Input Load		Output Drive
A	EN	Z
1	2	150

Coding Sequence	(z;a,en)
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<b>BTS7LM</b>	<b>TRISTATE BIDIRECTIONAL BUFFER WITH LOW POWER OUTPUT &amp; CMOS NON-INVERTING INPUT (4 mA)</b>	<b>BTS7LM</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	Hi-Z

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	t <sub>PHL</sub>	7.9	11.2	14.6	16.0	2
	t <sub>PLH</sub>	6.8	10.4	14.1	15.6	

Note: Delays for Output are Measured at TTL Level.

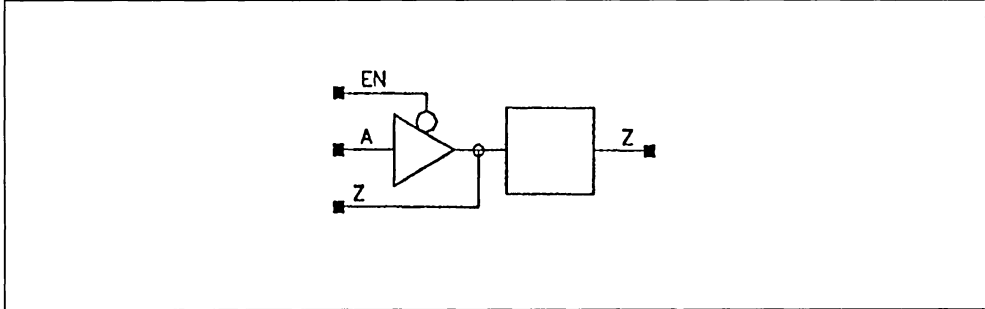
		FO 1	FO 2	FO 3	FO 4	FO 8
Z to ZI	t <sub>PHL</sub>	3.8	4.2	4.6	5.0	6.5
	t <sub>PLH</sub>	3.8	4.3	4.8	5.3	7.3

Input Load		Max. Output Load	
A	EN	Z	ZI
1	2	150 pF	3

Coding Sequence	(zi;a,en;z)
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<b>BTS7LO</b>	<b>TRISTATE BIDIRECTIONAL BUFFER WITH LOW POWER OUTPUT &amp; OPEN DRAIN, (4 mA)</b>	<b>BTS7LO</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
EN	A	Z
L	L	L
L	H	Hi-Z
H	X	Hi-Z

**CHARACTERISTICS**

	Propagation Delay (ns)	Cell Usage			
		C-15	C-50	C-85	C-100
A to Z $t_{PHL}$	8.2, 11.5, 14.9, 16.3	3			

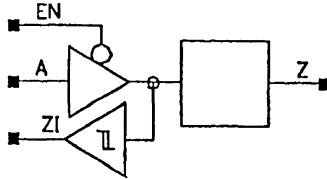
**Note:** Delays for Output are Measured at TTL Level.

Input Load		Max. Output Load (pF)
A	EN	Z
1	1	150

Coding Sequence	(z;a,en)
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**BTS7LS**

**TRISTATE BIDIRECTIONAL BUFFER WITH  
LOW POWER OUTPUT & SCHMITT  
NON-INVERTING INPUT (4 mA)**

**BTS7LS****SYMBOL****TRUTH TABLE**

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	Hi-Z

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	$t_{PHL}$	7.9	11.3	14.6	16.0	5
	$t_{PLH}$	6.9	10.5	14.1	15.6	

**Note:** Delays for Output are Measured at TTL Level.

		FO 1	FO 2	FO 3	FO 4	FO 8
Z to Zl	$t_{PHL}$	2.4	2.7	2.9	3.2	4.5
	$t_{PLH}$	1.8	1.9	2.0	2.1	2.6

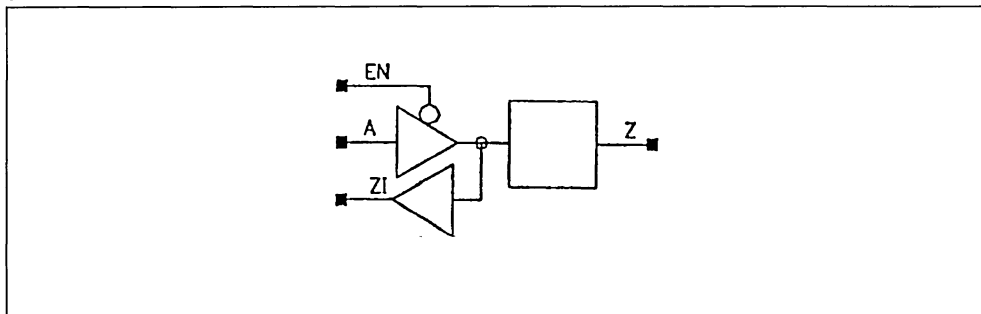
Input Load		Max. Output Load	
A	EN	Z	Zl
1	2	150 pF	22

Coding Sequence	(zi;a,en;z)
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<b>BTS7LT</b>	<b>TRISTATE BIDIRECTIONAL BUFFER WITH LOW POWER OUTPUT &amp; TTL NON-INVERTING INPUT (4 mA)</b>	<b>BTS7LT</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	Hi-Z

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	t <sub>PHL</sub>	9.6	13.1	16.5	18.0	5
	t <sub>PLH</sub>	8.2	11.9	15.7	17.3	

**Note:** Delays for Output are Measured at TTL Level.

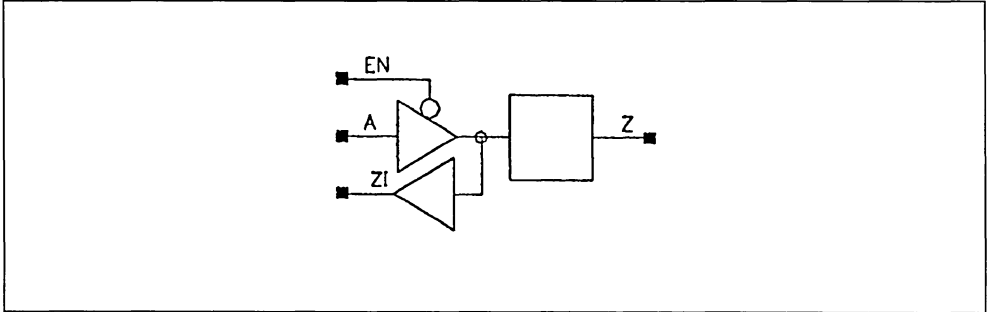
		FO 1	FO 2	FO 3	FO 4	FO 8
Z to ZI	t <sub>PHL</sub>	2.4	2.5	2.7	2.8	3.4
	t <sub>PLH</sub>	1.4	1.5	1.5	1.6	1.7

Input Load		Max. Output Load	
A	EN	Z	ZI
1	2	150 pF	37

Coding Sequence	(zi;a,en;z)
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<b>BTS7M</b>	<b>TRISTATE BIDIRECTIONAL BUFFER WITH CMOS NON-INVERTING INPUT (4 mA)</b>	<b>BTS7M</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	Hi-Z

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	t <sub>PHL</sub>	7.9	11.2	14.6	16.0	2
	t <sub>PLH</sub>	6.8	10.4	14.1	15.6	

**Note:** Delays for Output are Measured at TTL Level.

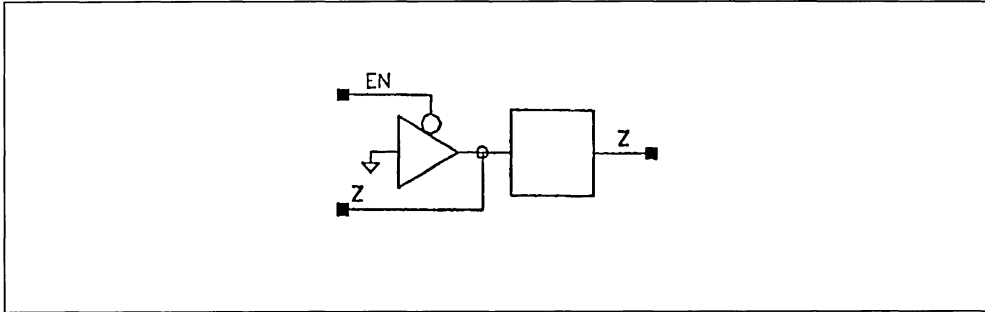
		FO 1	FO 2	FO 3	FO 4	FO 8
Z to ZI	t <sub>PHL</sub>	3.9	4.2	4.6	5.0	6.5
	t <sub>PLH</sub>	3.9	4.4	4.9	5.4	7.4

Input Load		Max. Output Load	
A	EN	Z	ZI
1	2	150 pF	27

Coding Sequence	(zi;a,en;z)
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<b>BTS70D</b>	<b>TRISTATE BIDIRECTIONAL BUFFER WITH OPEN DRAIN (4 mA)</b>	<b>BTS70D</b>
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**SYMBOL**



**TRUTH TABLE**

Input	Output
EN	Z
L	L
H	Hi-Z

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
EN to Z	$t_{PHL}$	6.4	9.7	13.1	14.5	1

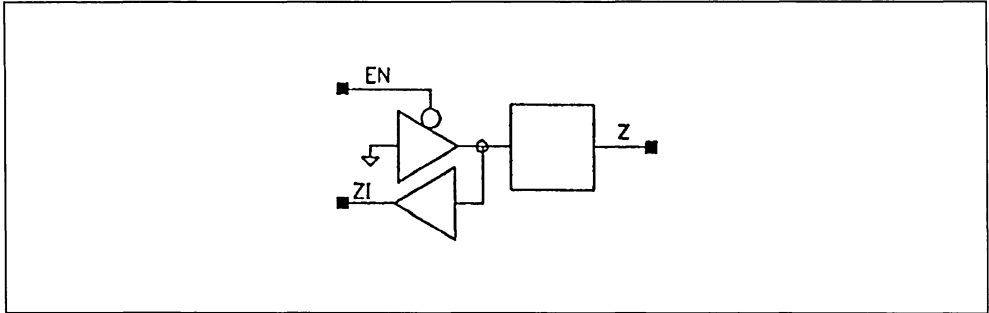
**Note:** Delays for Output are Measured at TTL Level.

Input Load	Max. Output Load (pF)
EN	Z
1	150

Coding Sequence	(z;en)
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<b>BTS70DM</b>	<b>TRISTATE BIDIRECTIONAL BUFFER WITH OPEN DRAIN &amp; CMOS NON-INVERTING INPUT (4 mA)</b>	<b>BTS70DM</b>
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**SYMBOL**



**TRUTH TABLE**

Input	Output
EN	Z
L	L
H	Hi-Z

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	$t_{PHL}$	6.4	9.7	13.1	14.5	1

**Note:** Delays for Output are Measured at TTL Level.

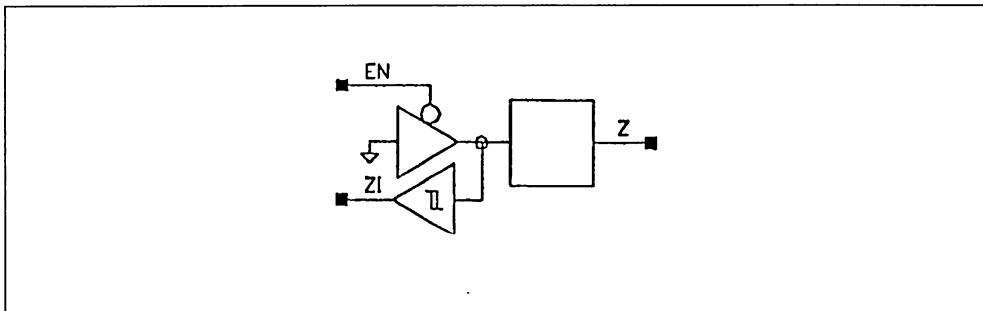
		FO 1	FO 2	FO 3	FO 4	FO 8
Z to ZI	$t_{PHL}$	3.9	4.2	4.6	5.0	6.5
	$t_{PLH}$	3.9	4.4	4.9	5.4	7.4

Input Load	Max. Output Load	
EN	Z	ZI
1	150 pF	27

Coding Sequence	(zi;en;z)
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<b>BTS70DS</b>	<b>TRISTATE BIDIRECTIONAL BUFFER WITH OPEN DRAIN &amp; SCHMITT NON-INVERTING INPUT (4 mA)</b>	<b>BTS70DS</b>
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**SYMBOL**



**TRUTH TABLE**

Input	Output
EN	Z
L	L
H	Hi-Z

**CHARACTERISTICS**

	Propagation Delay (ns)				Cell Usage
	C-15	C-50	C-85	C-100	
A to Z $t_{PHL}$	6.5	9.8	13.1	14.6	3

**Note:** Delays for Output are Measured at TTL Level.

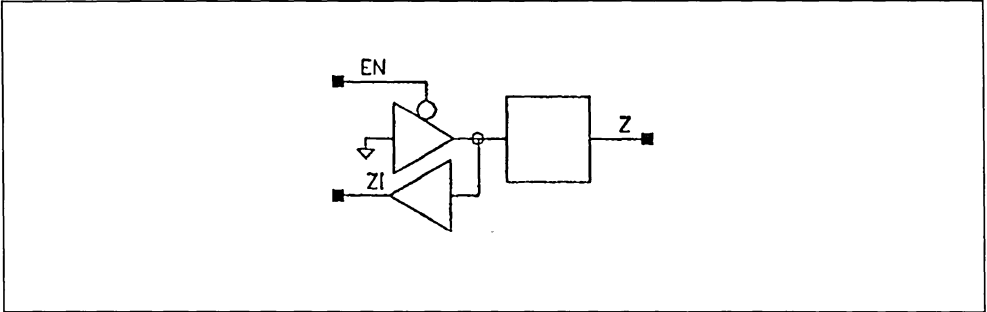
	FO 1	FO 2	FO 3	FO 4	FO 8
Z to ZI $t_{PHL}$	2.5	2.7	2.9	3.2	4.5
$t_{PLH}$	1.8	1.9	2.0	2.1	2.6

Input Load	Max. Output Load	
EN	Z	ZI
1	150 pF	22

Coding Sequence	(zi;en;z)
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<b>BTS70DT</b>	<b>TRISTATE BIDIRECTIONAL BUFFER WITH OPEN DRAIN &amp; TTL NON-INVERTING INPUT (4 mA)</b>	<b>BTS70DT</b>
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**SYMBOL**



**TRUTH TABLE**

Input	Output
EN	Z
L	L
H	Hi-Z

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	$t_{PHL}$	8.4	11.7	15.3	16.6	3

Note: Delays for Output are Measured at TTL Level.

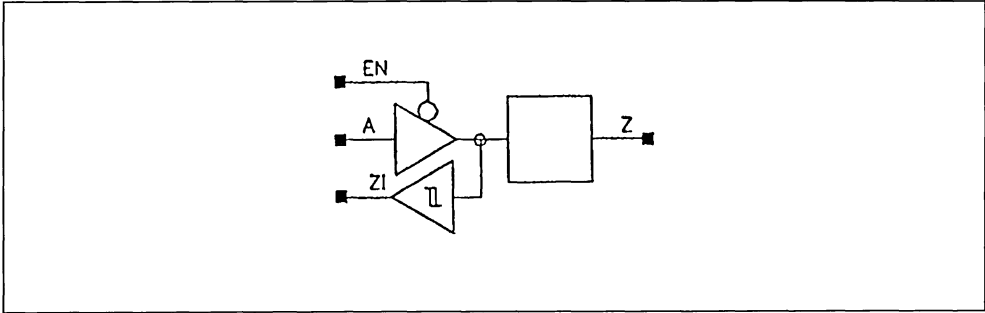
		FO 1	FO 2	FO 3	FO 4	FO 8
Z to ZI	$t_{PHL}$	2.4	2.5	2.6	2.7	3.4
	$t_{PLH}$	1.4	1.5	1.5	1.6	1.7

Input Load	Max. Output Load	
EN	Z	ZI
1	150 pF	37

Coding Sequence	(zi;en;z)
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<b>BTS7S</b>	<b>TRISTATE BIDIRECTIONAL BUFFER WITH SCHMITT NON-INVERTING INPUT (4 mA)</b>	<b>BTS7S</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	Hi-Z

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	$t_{PHL}$	7.9	11.3	14.6	16.0	5
	$t_{PLH}$	6.9	10.5	14.1	15.6	

**Note:** Delays for Output are Measured at TTL Level.

		FO 1	FO 2	FO 3	FO 4	FO 8
Z to ZI	$t_{PHL}$	2.5	2.7	2.9	3.1	4.4
	$t_{PLH}$	1.8	1.9	2.0	2.1	2.6

Input Load		Max. Output Load	
EN	A	Z	ZI
1	2	150 pF	22

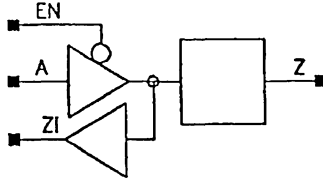
Coding Sequence	(zi;a,en;z)
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BTS7T

TRISTATE BIDIRECTIONAL BUFFER WITH  
TTL NON-INVERTING INPUT (4 mA)

BTS7T

## SYMBOL



## TRUTH TABLE

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	Hi-Z

## CHARACTERISTICS

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	t <sub>PHL</sub>	9.6	13.1	16.5	18.0	5
	t <sub>PLH</sub>	8.2	11.9	15.7	17.3	

Note: Delays for Output are Measured at TTL Level.

		FO 1	FO 2	FO 3	FO 4	FO 8
Z to ZI	t <sub>PHL</sub>	2.2	2.3	2.3	2.4	2.7
	t <sub>PLH</sub>	1.6	1.7	1.8	1.8	2.2

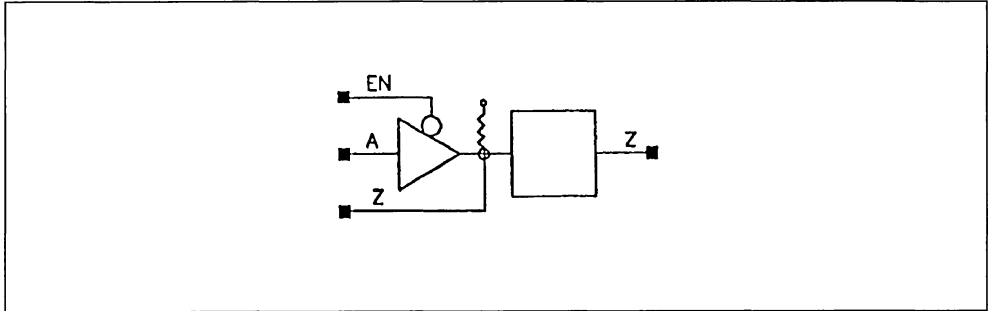
Input Load		Max. Output Load	
A	EN	Z	ZI
1	2	150 pF	37

Coding Sequence	(zi;a,en;z)
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<b>BTS7U</b>	<b>TRISTATE BIDIRECTIONAL BUFFER WITH PULL UP RESISTOR (4 mA)</b>	<b>BTS7U</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	H*

\* With pull up resistor

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	t <sub>PHL</sub>	7.9	11.2	14.6	16.0	2
	t <sub>PLH</sub>	6.8	10.4	14.1	15.6	

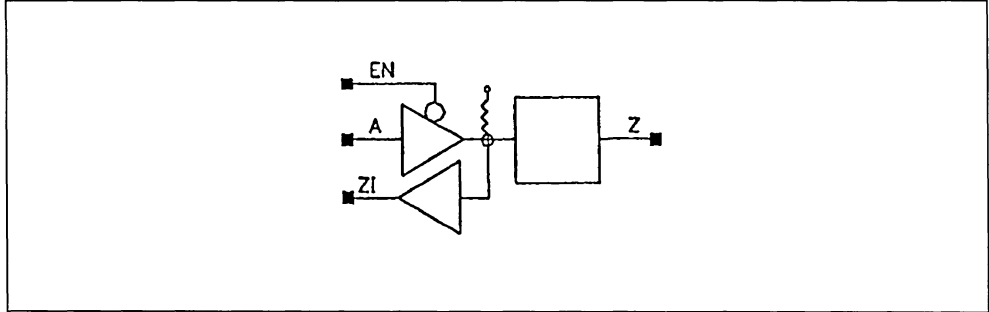
**Note:** Delays for Output are Measured at TTL Level.

Input Load		Max. Output Load (pF)
A	EN	Z
1	2	150

Coding Sequence	(z;a,en)
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<b>BTS7UM</b>	<b>TRISTATE BIDIRECTIONAL BUFFER WITH PULL UP RESISTOR &amp; CMOS NON-INVERTING INPUT (4 mA)</b>	<b>BTS7UM</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	H

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	t <sub>PHL</sub>	7.9	11.2	14.6	16.0	2
	t <sub>PLH</sub>	6.8	10.4	14.1	15.6	

**Note:** Delays for Output are Measured at TTL Level.

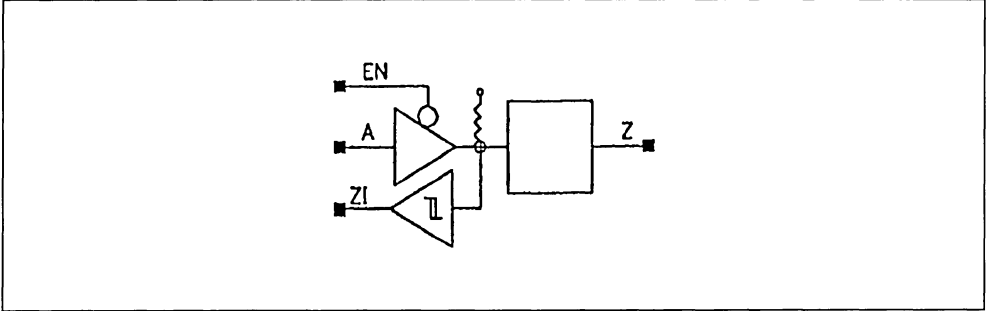
		FO 1	FO 2	FO 3	FO 4	FO 8
Z to ZI	t <sub>PHL</sub>	3.9	4.2	4.6	5.0	6.5
	t <sub>PLH</sub>	3.9	4.4	4.9	5.4	7.4

Input Load		Max. Output Load	
A	EN	Z	ZI
1	2	150 pF	27

Coding Sequence	(zi;a,en;z)
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<b>BTS7US</b>	<b>TRISTATE BIDIRECTIONAL BUFFER WITH PULL UP RESISTOR &amp; SCHMITT NON-INVERTING INPUT (4 mA)</b>	<b>BTS7US</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	H

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	t <sub>PHL</sub>	7.9	11.3	14.6	16.0	5
	t <sub>PLH</sub>	6.9	10.5	14.1	15.6	

**Note:** Delays for Output are Measured at TTL Level.

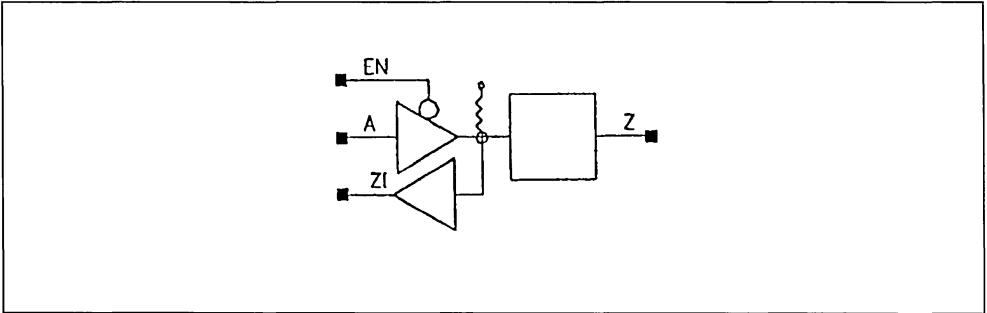
		FO 1	FO 2	FO 3	FO 4	FO 8
Z to ZI	t <sub>PHL</sub>	2.4	2.7	2.9	3.1	4.5
	t <sub>PLH</sub>	1.8	1.9	2.0	2.1	2.6

Input Load		Max. Output Load	
A	EN	Z	ZI
1	2	150 pF	22

Coding Sequence	(zi;a,en;z)
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<b>BTS7UT</b>	<b>TRISTATE BIDIRECTIONAL BUFFER WITH PULL UP RESISTOR &amp; TTL NON-INVERTING INPUT (4 mA)</b>	<b>BTS7UT</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	H

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	t <sub>PHL</sub>	9.5	13.0	16.4	17.9	4
	t <sub>PLH</sub>	8.1	11.8	15.6	17.2	

**Note:** Delays for Output are Measured at TTL Level.

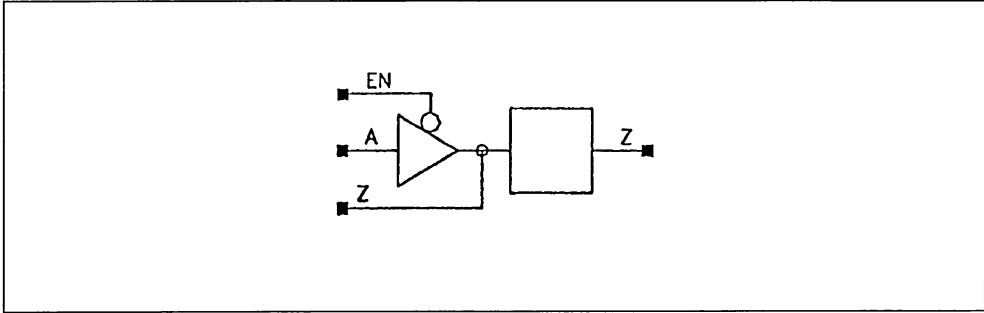
		FO 1	FO 2	FO 3	FO 4	FO 8
Z to Zi	t <sub>PHL</sub>	2.4	2.5	2.7	2.8	3.4
	t <sub>PLH</sub>	1.4	1.5	1.5	1.6	1.7

Input Load		Max. Output Load	
A	EN	Z	Zi
1	2	150 pF	37

Coding Sequence	(zi;a,en;z)
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<b>BTS78</b>	<b>TRISTATE BIDIRECTIONAL BUFFER (2 mA)</b>	<b>BTS78</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	Hi-Z

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85		
A to Z	t <sub>PHL</sub>	9.0	15.5	22.0		2
	t <sub>PLH</sub>	8.5	15.7	23.0		

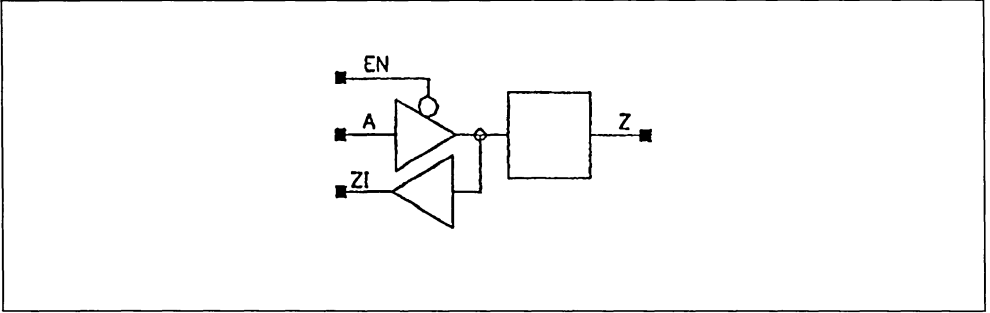
**Note:** Delays for Output are Measured at TTL Level.

Input Load		Max. Output Load (pF)
A	EN	Z
1	2	90

Coding Sequence	(z;a,en)
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<b>BTS78M</b>	<b>TRISTATE BIDIRECTIONAL BUFFER WITH CMOS NON-INVERTING INPUT (2 mA)</b>	<b>BTS78M</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	Hi-Z

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85		
A to Z	t <sub>PHL</sub>	9.0	15.5	22.0		2
	t <sub>PLH</sub>	8.5	15.7	23.0		

**Note:** Delays for Output are Measured at TTL Level.

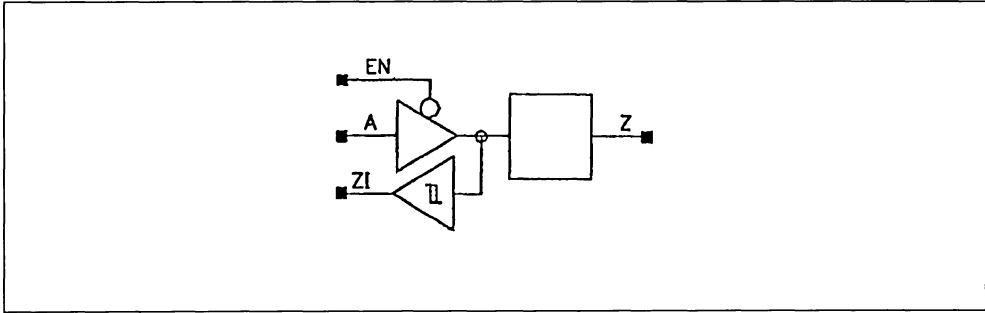
		FO 1	FO 2	FO 3	FO 4	FO 8
Z to Zi	t <sub>PHL</sub>	3.9	4.2	4.6	5.0	6.5
	t <sub>PLH</sub>	3.9	4.4	4.9	5.4	7.4

Input Load		Max. Output Load	
A	EN	Z	Zi
1	2	90 pF	27

Coding Sequence	(zi;a,en;z)
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<b>BTS78S</b>	<b>TRISTATE BIDIRECTIONAL BUFFER WITH SCHMITT NON-INVERTING INPUT (2 mA)</b>	<b>BTS78S</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	Hi-Z

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85		
A to Z	t <sub>PHL</sub>	9.1	15.6	22.1		5
	t <sub>PLH</sub>	8.6	15.8	23.1		

**Note:** Delays for Output are Measured at TTL Level.

		FO 1	FO 2	FO 3	FO 4	FO 8
Z to ZI	t <sub>PHL</sub>	2.4	2.7	2.9	3.2	4.5
	t <sub>PLH</sub>	2.2	1.9	2.0	2.1	2.6

Input Loading		Max. Output Loading	
A	EN	Z	ZI
1	2	90 pF	22

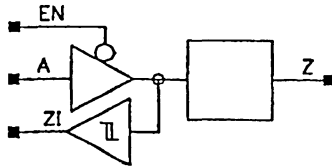
Coding Sequence	(zi;a,en;z)
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BTS78T

TRISTATE BIDIRECTIONAL BUFFER WITH  
SCHMITT INPUT (2 mA)

BTS78T

## SYMBOL



## TRUTH TABLE

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	Hi-Z

## CHARACTERISTICS

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85		
A to Z	$t_{PHL}$	10.7	17.6	24.5	5	
	$t_{PLH}$	9.7	17.2	24.7		

Note: Delays for Output are Measured at TTL Level.

		FO 1	FO 2	FO 3	FO 4	FO 8
Z to ZI	$t_{PHL}$	1.4	1.5	2.7	2.8	3.4
	$t_{PLH}$	1.4	1.5	1.5	1.6	1.7

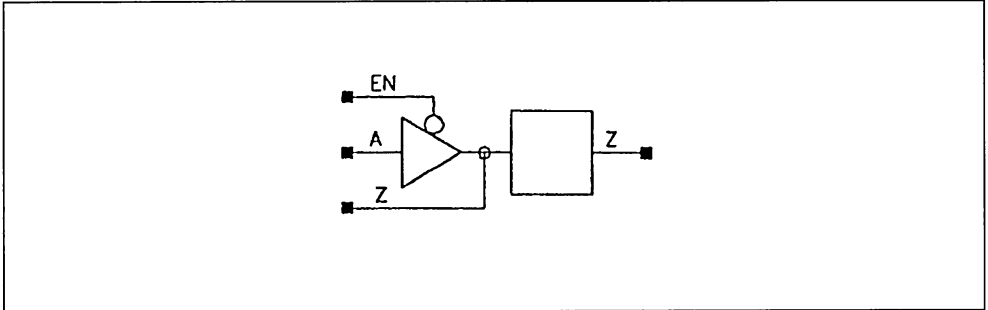
Input Load		Max. Output Load	
A	EN	Z	ZI
1	2	90 pF	37

Coding Sequence	(zi;a,en;z)
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<b>BTS8</b>	<b>TRISTATE BIDIRECTIONAL BUFFER (8 mA)</b>	<b>BTS8</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	Hi-Z

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	t <sub>PHL</sub>	8.0	9.7	11.4	12.2	2
	t <sub>PLH</sub>	6.4	8.2	10.0	10.0	

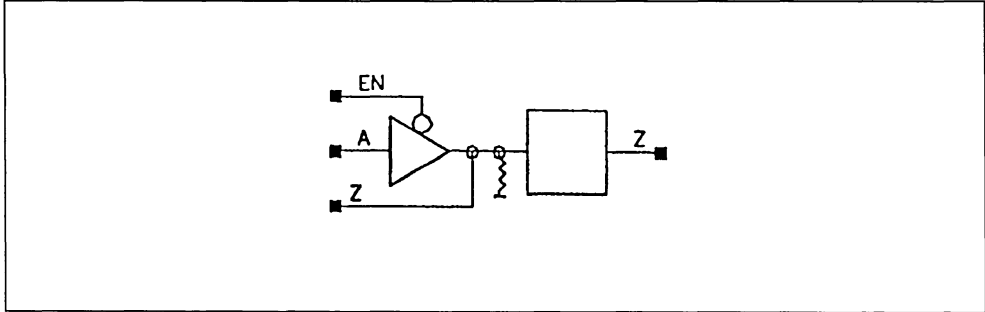
**Note:** Delays for Output are Measured at TTL Level.

Input Load		Max. Output Load (pF)
A	EN	Z
1	2	240

Coding Sequence	(z;a,en)
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<b>BTS8D</b>	<b>TRISTATE BIDIRECTIONAL BUFFER WITH PULL UP DOWN RESISTOR (8 mA)</b>	<b>BTS8D</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	L*

\* WITH PULL DOWN RESISTOR

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	t <sub>PHL</sub>	8.0	9.7	11.4	12.2	2
	t <sub>PLH</sub>	6.4	8.2	10.0	10.8	

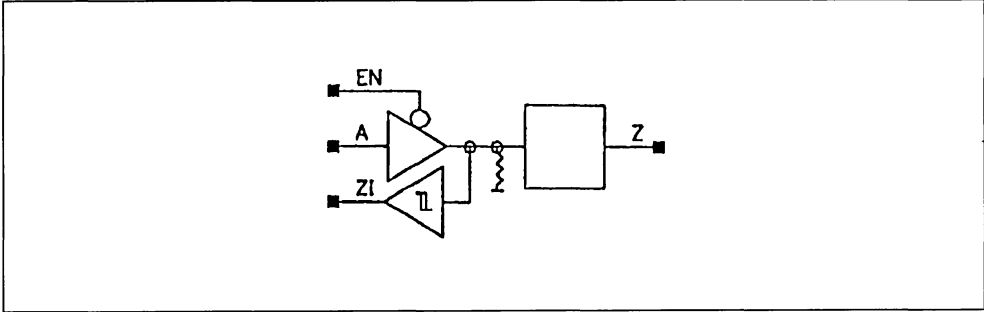
**Note:** Delays for Output are Measured at TTL Level.

Input Load		Max. Output Load (pF)
A	EN	Z
1	2	240

Coding Sequence	(z;a,en)
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<b>BTS8DS</b>	<b>TRISTATE BIDIRECTIONAL BUFFER WITH PULL DOWN RESISTOR &amp; SCHMITT NON-INVERTING INPUT (8 mA)</b>	<b>BTS8DS</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	L

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	t <sub>PHL</sub>	8.0	9.7	11.5	12.7	5
	t <sub>PLH</sub>	6.4	8.2	10.1	10.8	

**Note:** Delays for Output are Measured at TTL Level.

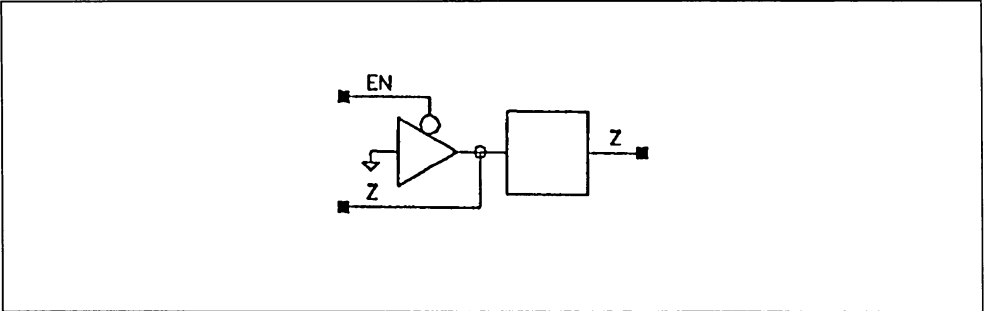
		FO 1	FO 2	FO 3	FO 4	FO 8
Z to ZI	t <sub>PHL</sub>	2.5	2.7	2.9	3.2	4.5
	t <sub>PLH</sub>	1.8	1.9	2.0	2.1	2.6

Input Load		Max. Output Load	
A	EN	Z	ZI
1	2	240 pF	22

<b>Coding Sequence</b>	(zi;a,en;z)
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<b>BTS80D</b>	<b>TRISTATE BIDIRECTIONAL BUFFER WITH OPEN DRAIN (8 mA)</b>	<b>BTS80D</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
EN		Z
L		L
H		Hi-Z

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-30	C-50	C-85	C-100	
A to Z	$t_{PHL}$	6.5	8.2	9.9	10.7	1

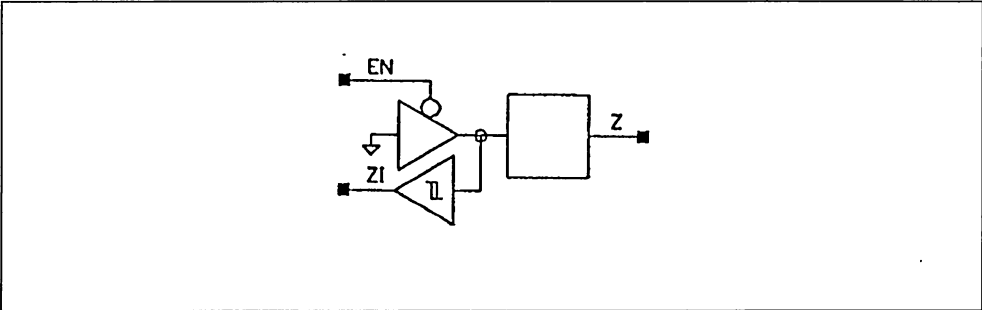
**Note:** Delays for Output are Measured at TTL Level.

Input Load	Max. Output Load (pF)
EN	Z
1	240

Coding Sequence	(z;en)
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<b>BTS80DS</b>	<b>TRISTATE BIDIRECTIONAL BUFFER WITH OPEN DRAIN &amp; SCHMITT INPUT (8 mA)</b>	<b>BTS80DS</b>
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**SYMBOL**



**TRUTH TABLE**

Input	Output
EN	Z
L	*L
H	Hi-Z

**CHARACTERISTICS**

		Propagation Delay (ns)					Cell Usage
		C-15	C-50	C-85	C-100	C-160	
A to Z	$t_{PHL}$	6.5	8.2	10.0	10.7	13.7	4

**Note:** Delays for Output are Measured at TTL Level.

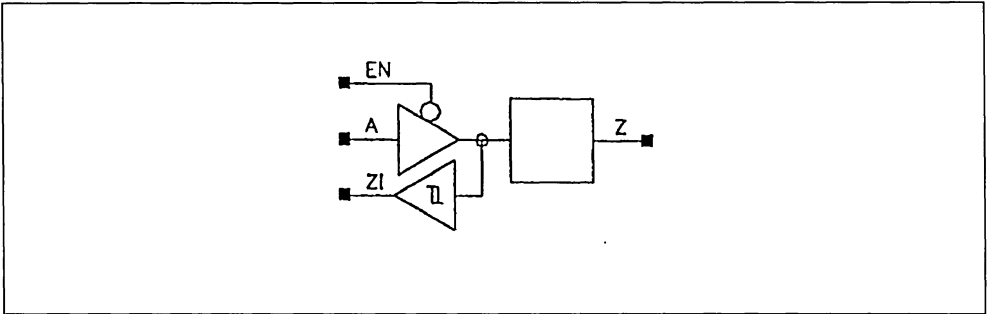
	FO 1	FO 2	FO 3	FO 4	FO 8	
Z to ZI	$t_{PHL}$	2.4	2.7	3.0	3.3	4.5
	$t_{PLH}$	1.8	1.9	2.0	2.1	2.6

Input Load	Max. Output Load	
EN	Z	ZI
1	240 pF	22

Coding Sequence	(zi;en;z)
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<b>BTS8S</b>	<b>TRISTATE BIDIRECTIONAL BUFFER WITH SCHMITT NON-INVERTING INPUT (8 mA)</b>	<b>BTS8S</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	Hi-Z

**CHARACTERISTICS**

		Propagation Delay (ns)					Cell Usage
		C-15	C-50	C-85	C-100	C-160	
A to Z	t <sub>PHL</sub>	8.0	9.7	11.5	12.2	15.2	5
	t <sub>PLH</sub>	6.4	8.2	10.1	10.8	14.0	

**Note:** Delays for Output are Measured at TTL Level.

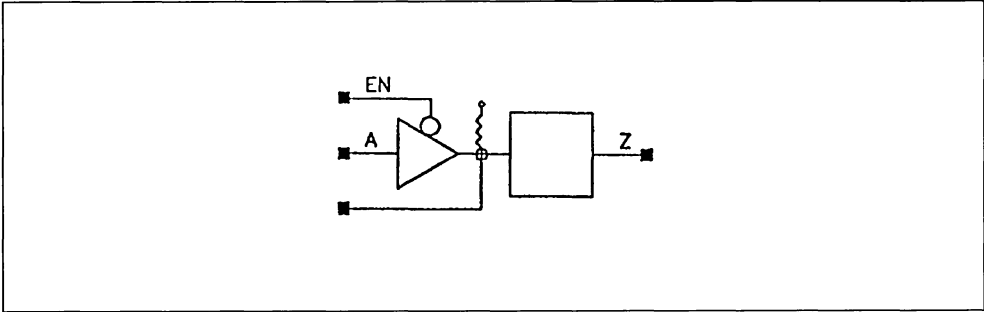
		FO 1	FO 2	FO 3	FO 4	FO 8
Z to ZI	t <sub>PHL</sub>	2.4	2.7	3.0	3.3	4.5
	t <sub>PLH</sub>	1.8	1.9	2.0	2.1	2.6

Input Load		Max. Output Load	
A	EN	Z	ZI
1	2	240 pF	22

Coding Sequence	(zi;a,en;z)
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<b>BTS8U</b>	<b>TRISTATE BIDIRECTIONAL BUFFER WITH PULL UP RESISTOR (8 mA)</b>	<b>BTS8U</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	H*

\* With pull up resistor

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	$t_{PHL}$	8.0	9.7	11.4	12.2	2
	$t_{PLH}$	6.4	8.2	10.0	10.8	

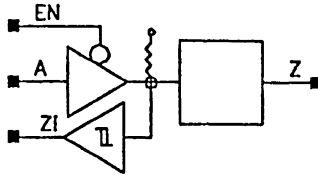
**Note:** Delays for Output are Measured at TTL Level.

Input Load		Max. Output Load (pF)
A	EN	Z
1	2	240

Coding Sequence	(z:a,en)
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<b>BTS8US</b>	<b>TRISTATE BIDIRECTIONAL BUFFER WITH PULL UP RESISTOR &amp; NON-INVERTING SCHMITT TRIGGER (8 mA)</b>	<b>BTS8US</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	H

**CHARACTERISTICS**

		Propagation Delay (ns)					Cell Usage
		C-15	C-50	C-85	C-100	C-160	
A to Z	t <sub>PHL</sub>	8.0	9.7	11.5	12.2	15.2	5
	t <sub>PLH</sub>	6.4	8.2	10.1	10.8	14.0	

**Note:** Delays for Output are Measured at TTL Level.

		FO 1	FO 2	FO 3	FO 4	FO 8
Z to ZI	t <sub>PHL</sub>	2.4	2.7	3.0	3.3	4.5
	t <sub>PLH</sub>	1.8	1.9	2.0	2.1	2.6

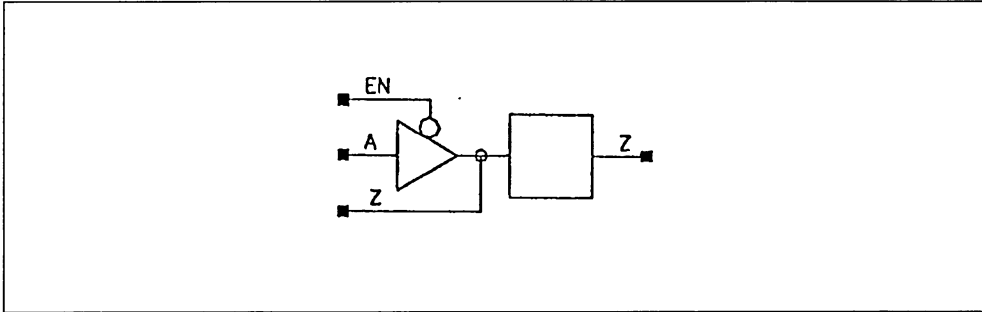
Input Load		Max. Output Load	
A	EN	Z	ZI
1	2	240 pF	22

Coding Sequence	(zi;a,en;z)
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<b>BTS9</b>	<b>TRISTATE BIDIRECTIONAL BUFFER (16 mA)</b>	<b>BTS9</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	Hi-Z

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	t <sub>PHL</sub>	7.5	8.7	9.8	10.3	4
	t <sub>PLH</sub>	8.1	9.1	10.1	10.6	

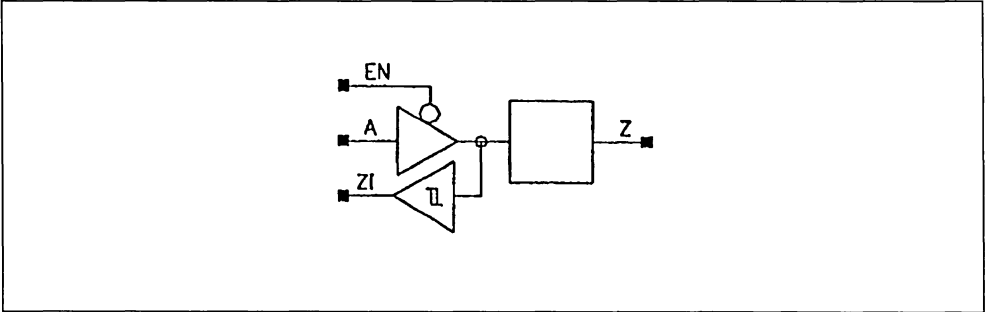
**Note:** Delays for Output are Measured at TTL Level.

Input Load		Max. Output Load (pF)
A	EN	Z
2	4	240

Coding Sequence	(z;a,en)
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<b>BTS9S</b>	<b>TRISTATE BIDIRECTIONAL BUFFER (16 mA) WITH NON-INVERTING SCHMITT TRIGGER</b>	<b>BTS9S</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
EN	A	Z
L	L	L
L	H	H
H	X	Hi-Z

**CHARACTERISTICS**

		Propagation Delay (ns)					Cell Usage
		C-15	C-50	C-85	C-100	C-160	
A to Z	t <sub>PHL</sub>	7.5	8.7	9.8	10.3	12.3	5
	t <sub>PLH</sub>	8.1	9.1	10.1	10.6	12.3	

Note: Delays for Output are Measured at TTL Level.

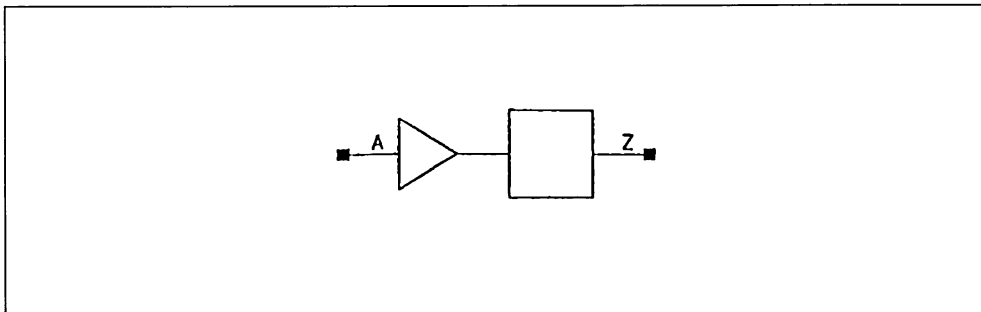
		FO 1	FO 2	FO 3	FO 4	FO 8
Z to ZI	t <sub>PHL</sub>	2.4	2.5	3.0	3.3	4.5
	t <sub>PLH</sub>	1.8	1.9	2.0	2.1	2.6

Input Load		Max. Output Load	
A	EN	Z	ZI
2	4	240pF	22

Coding Sequence	(zi;a,en;z)
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<b>B1</b>	<b>OUTPUT BUFFER (4 mA)</b>	<b>B1</b>
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**SYMBOL**



**TRUTH TABLE**

Input	Output
A	Z
L	L
H	H

**CHARACTERISTICS**

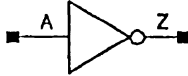
		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	$t_{PHL}$	6.4	9.9	13.4	14.9	0
	$t_{PLH}$	5.2	9.0	12.7	14.3	

Input Load	Max. Output Load (pF)
A	Z
2	150

Coding Sequence	(z;a)
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<b>B1A</b>	<b>INVERTING POWER BUFFER</b>	<b>B1A</b>
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**SYMBOL**



**TRUTH TABLE**

Input A	Output Z
L	H
H	L

**CHARACTERISTICS**

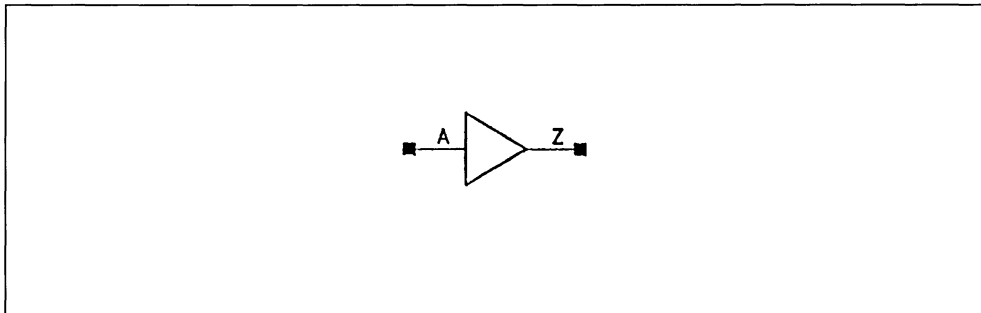
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A to Z	$t_{PHL}$	0.41	0.49	0.57	0.65	0.98	1
	$t_{PLH}$	0.64	0.73	0.81	0.90	1.24	

Input Load	Output Drive
A	Z
3	37

Coding Sequence	(z:a)
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<b>B1I</b>	<b>NON-INVERTING INTERNAL BUFFER</b>	<b>B1I</b>
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**SYMBOL**



**TRUTH TABLE**

Input	Output
A	Z
L	L
H	H

**CHARACTERISTICS**

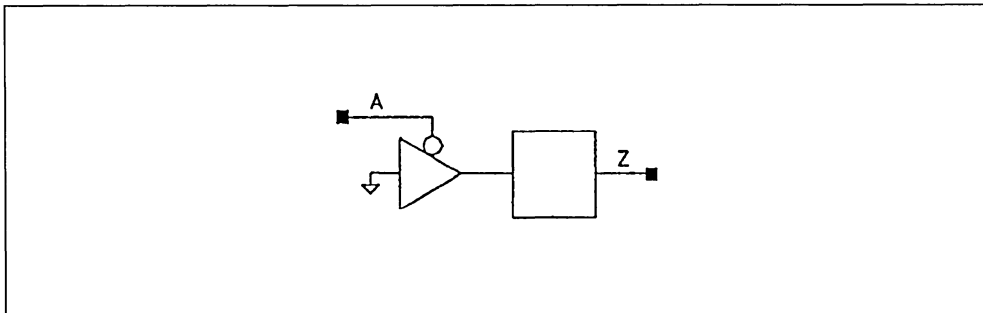
		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	$t_{PHL}$	3.5	7.5	11.5	13.2	2
	$t_{PLH}$	4.0	8.5	13.0	14.9	

Input Load	Max. Output Load (pF)
A	Z
2	12.6

Coding Sequence	(z;a)
-----------------	-------

<b>B10D</b>	<b>OUTPUT BUFFER WITH OPEN DRAIN (4 mA)</b>	<b>B10D</b>
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**SYMBOL**



**TRUTH TABLE**

Input	Output
A	Z
L	L
H	Hi-Z

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	$t_{PHL}$	6.4	10.4	14.1	15.7	0

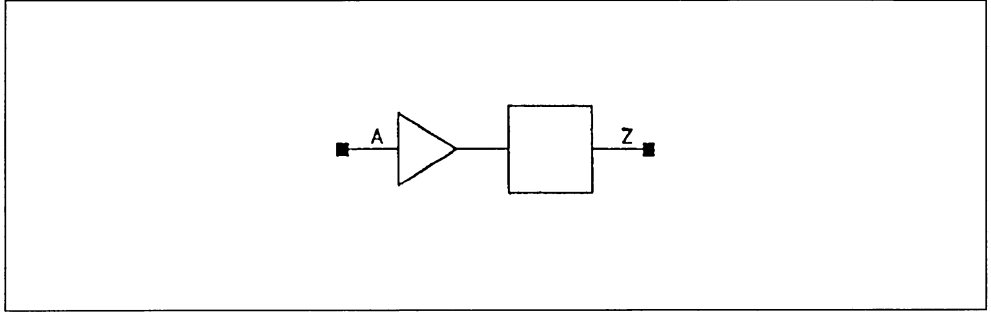
**Note:** Delays for Output are Measured at TTL Level.

Input Load	Max. Output Load (pF)
A	Z
1	150

Coding Sequence	(z;a)
-----------------	-------

<b>B14</b>	<b>OUTPUT BUFFER (1 mA)</b>	<b>B14</b>
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**SYMBOL**



**TRUTH TABLE**

Input	Output
A	Z
L	L
H	H

**CHARACTERISTICS**

		Propagation Delay (ns)		Cell Usage
		C-15	C-50	
A to Z	$t_{PHL}$	11.4	25.4	2
	$t_{PLH}$	11.1	26.1	

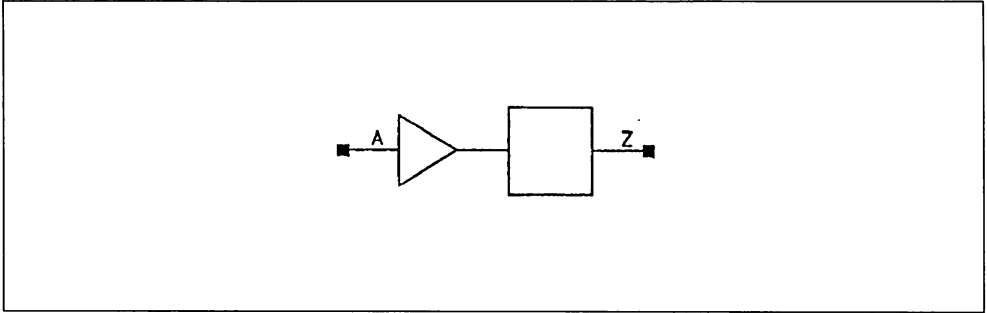
**Note:** Delays for Output are Measured at TTL Level.

Input Load	Max. Output Load (pF)
A	Z
2	50

<b>Coding Sequence</b>	(z;a)
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<b>B18</b>	<b>OUTPUT BUFFER (2 mA)</b>	<b>B18</b>
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**SYMBOL**



**TRUTH TABLE**

Input	Output
A	Z
L	L
H	H

**CHARACTERISTICS**

		Propagation Delay (ns)			Cell Usage
		C-15	C-50	C-85	
A to Z	$t_{PHL}$	7.6	14.3	20.9	2
	$t_{PLH}$	7.1	14.5	22.0	

**Note:** Delays for Output are Measured at TTL Level.

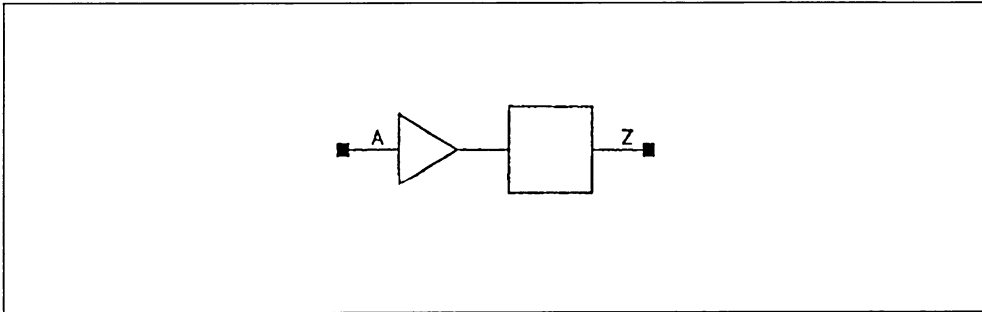
Input Load	Max. Output Load (pF)
A	Z
2	90

Coding Sequence	(z;a)
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<b>B2</b>	<b>OUTPUT BUFFER (8 mA)</b>	<b>B2</b>
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**SYMBOL**



**TRUTH TABLE**

Input	Output
<b>A</b>	<b>Z</b>
L	L
H	H

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	$t_{PHL}$	6.5	8.3	10.1	10.9	0
	$t_{PLH}$	4.7	6.6	8.5	9.4	

**Note:** Delays for Output are Measured at TTL Level.

Input Load	Max. Output Load (pF)
<b>A</b>	<b>Z</b>
2	240

<b>Coding Sequence</b>	(z;a,en)
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**B2A****INVERTING POWER BUFFER****B2A****SYMBOL****TRUTH TABLE**

Input	Output
A	Z
L	H
H	L

**CHARACTERISTICS**

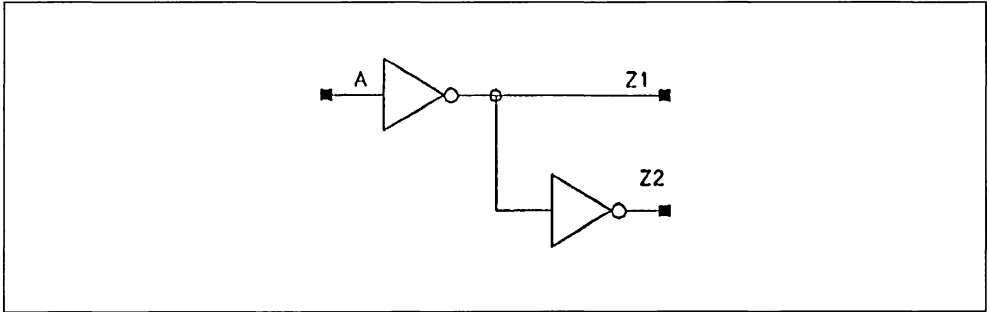
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A to Z	t <sub>PHL</sub>	0.41	0.45	0.49	0.54	0.70	2
	t <sub>PLH</sub>	0.67	0.71	0.75	0.79	0.96	

Input Load	Output Drive
A	Z
5	114

Coding Sequence	(z;a)
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<b>B2I</b>	<b>INVERTER INTO 3 PARALLEL INVERTERS</b>	<b>B2I</b>
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**SYMBOL**



**TRUTH TABLE**

Input	Output	
A	Z1	Z2
L	H	L
H	L	H

**CHARACTERISTICS**

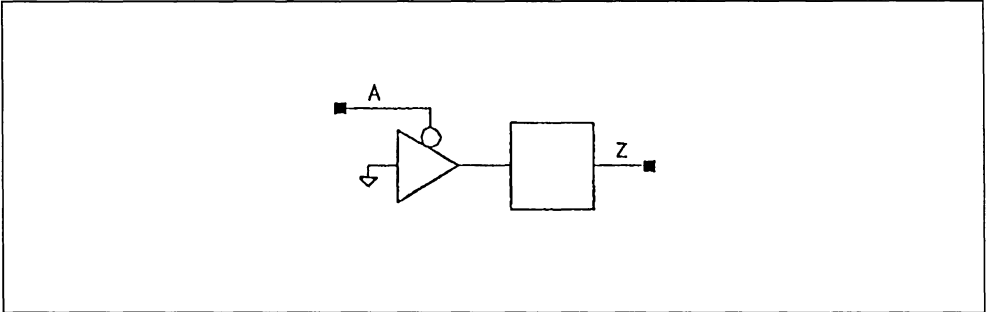
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A to Z1	t <sub>PHL</sub>	1.4	1.7	2.1	2.4	3.8	2
	t <sub>PLH</sub>	0.9	1.0	1.1	1.2	1.7	
Z1 to Z2	t <sub>PHL</sub>	0.5	0.6	0.7	0.8	1.3	
	t <sub>PLH</sub>	0.4	0.4	0.4	0.4	0.6	

Input Load	Output Drive	
A	Z1	Z2
1	20	40

Coding Sequence	(z1,z2;a)
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<b>B2OD</b>	<b>OUTPUT BUFFER WITH OPEN DRAIN (8 mA)</b>	<b>B2OD</b>
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**SYMBOL**



**TRUTH TABLE**

Input	Output
A	Z
L	L
H	Hi-Z

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	$t_{PHL}$	6.6	8.5	10.4	11.2	1

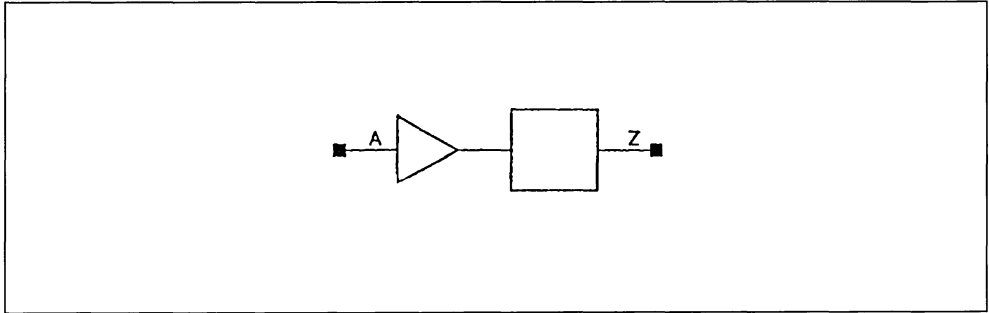
**Note:** Delays for Output are Measured at TTL Level.

Input Load	Max. Output Load (pF)
A	Z
1	240

Coding Sequence	(z;a)
-----------------	-------

<b>B3</b>	<b>OUTPUT BUFFER (16 mA)</b>	<b>B3</b>
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**SYMBOL**



**TRUTH TABLE**

Input	Output
A	Z
L	L
H	X

**CHARACTERISTICS**

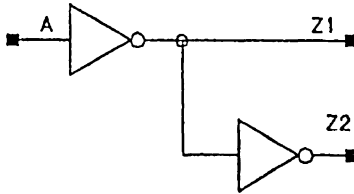
		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	$t_{PHL}$	6.4	7.2	8.1	8.4	0
	$t_{PLH}$	4.4	5.2	5.9	6.2	

Input Load	Max. Output Load (pF)
A	Z
4	240

Coding Sequence	(z;a)
-----------------	-------

<b>B3I</b>	<b>2X INVERTER IN 2X INVERTER</b>	<b>B3I</b>
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**SYMBOL**



**TRUTH TABLE**

Input	Output	
A	Z1	Z2
H	L	H
L	H	L

**CHARACTERISTICS**

		Propagation Delay (ns)					Cell Usage
		FO 2	FO 4	FO 8	FO 16	FO 32	
A to Z2	$t_{PHL}$	1.2	1.4	1.7	2.3	3.6	2
	$t_{PLH}$	1.2	1.4	1.8	2.7	4.4	

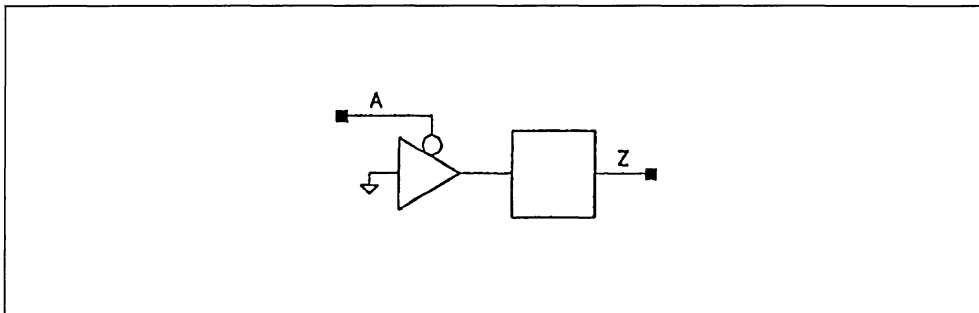
**Note:** Delays for Output are Measured at TTL Level.

Input Load	Output Drive	
A	Z1	Z2
2	36	36

Coding Sequence	(z1,z2;a)
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<b>B3OD</b>	<b>OUTPUT BUFFER WITH OPEN DRAIN (16 mA)</b>	<b>B3OD</b>
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**SYMBOL**



**TRUTH TABLE**

Input	Output
A	Z
L	L
H	Hi-Z

**CHARACTERISTICS**

		Propagation Delay (ns)				Cell Usage
		C-15	C-50	C-85	C-100	
A to Z	$t_{PHL}$	6.4	7.2	8.1	8.4	1

Input Load	Max. Output Load (pF)
A	Z
4	240

Coding Sequence	(z;a)
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B4I

4 PARALLEL INVERTERS

B4I

## SYMBOL



## TRUTH TABLE

Input	Output
A	Z
H	L
L	H

## CHARACTERISTICS

		Propagation Delay (ns)				
		FO 1	FO 2	FO 3	FO 4	FO 8
A to Z	t <sub>PHL</sub>	0.6	0.7	0.8	0.9	1.35
	t <sub>PLH</sub>	0.5	0.5	0.5	0.6	0.7

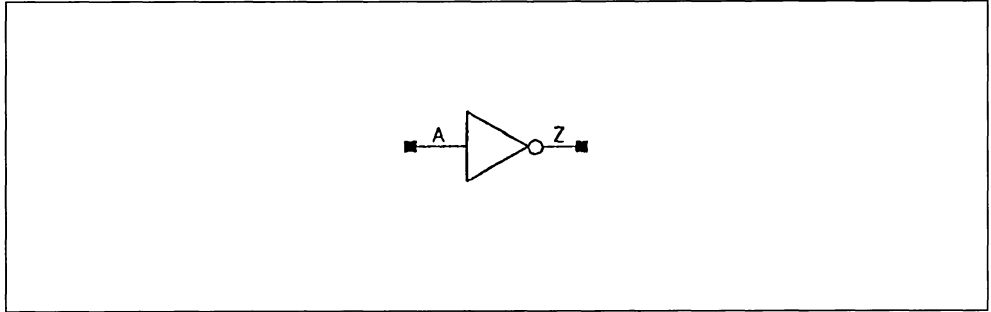
Input Load	Output Drive
A	Z
4	61

Coding Sequence	(z;a)



<b>B5I</b>	<b>3 PARALLEL INVERTERS</b>	<b>B5I</b>
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**SYMBOL**



**TRUTH TABLE**

Input	Output
A	Z
H	L
L	H

**CHARACTERISTICS**

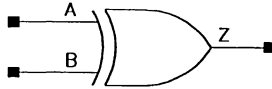
		Propagation Delay (ns)				
		FO 1	FO 2	FO 3	FO 4	FO 8
A to Z	$t_{PHL}$	0.41	0.49	0.57	0.65	0.98
	$t_{PLH}$	0.64	0.73	0.81	0.90	1.24

Input Load	Output Drive
A	Z
3	47

Coding Sequence	(z;a)
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<b>EO</b>	<b>2 INPUT EXCLUSIVE-OR</b>	<b>EO</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
A	B	Z
H	H	L
H	L	H
L	H	H
L	L	L

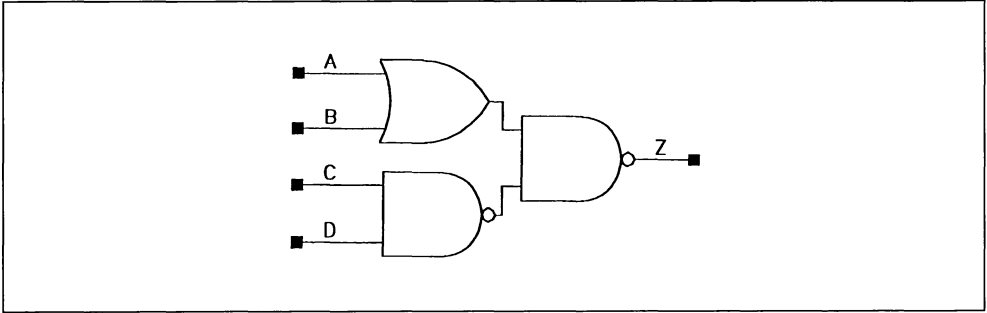
**CHARACTERISTICS**

		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A,B to Z	t <sub>PHL</sub>	2.2	2.4	2.5	2.7	3.4	2
	t <sub>PLH</sub>	2.4	2.6	2.9	3.1	4.2	

Input Load		Output Drive
A	B	Z
2	2	22

<b>EON1</b>	<b>OR2 &amp; NAND2 INTO NAND2</b>	<b>EON1</b>
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**SYMBOL**



**TRUTH TABLE**

Input				Output
A	B	C	D	Z
L	L	X	X	H
X	X	H	H	H
X	H	X	L	L
X	H	L	X	L
H	X	X	L	L
H	X	L	X	L

**CHARACTERISTICS**

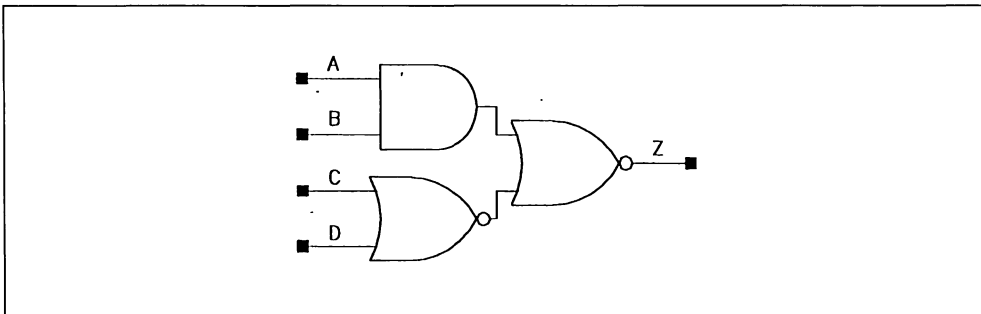
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A,B,C,D to Z	t <sub>PHL</sub>	1.36	1.56	1.76	1.96	2.76	2
	t <sub>PLH</sub>	1.56	1.98	2.39	2.81	4.49	

Input Load				Output Drive
A	B	C	D	Z
1	1	1	1	18

Coding Sequence	(z;a,b,c,d)
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<b>EO1</b>	<b>AND2 &amp; NOR2 INTO NOR2</b>	<b>EO1</b>
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**SYMBOL**



**TRUTH TABLE**

Input				Output
A	B	C	D	Z
H	H	X	X	L
L	X	M	X	H
L	X	X	H	H
X	L	H	X	H
X	L	X	H	H
X	X	L	L	L

**CHARACTERISTICS**

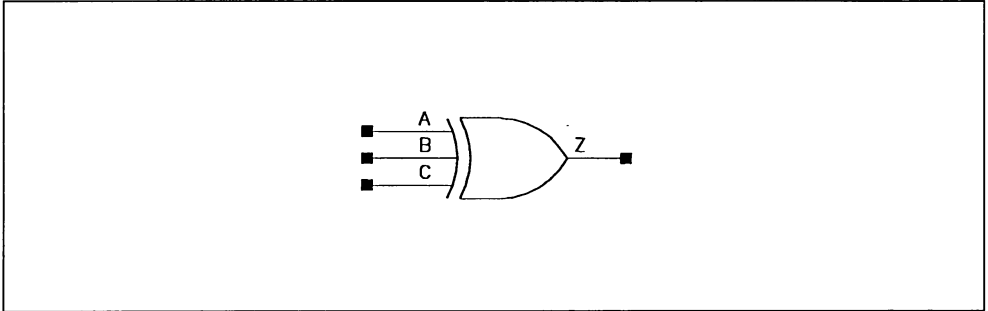
	Propagation Delay (ns)					Cell Usage	
	FO 1	FO 2	FO 3	FO 4	FO 8		
A,B,C,D to Z	$t_{PHL}$	1.49	1.68	1.87	2.06	2.84	2
	$t_{PLH}$	1.50	1.92	2.33	2.75	4.43	

Input Load				Output Drive
A	B	C	D	Z
1	1	1	1	18

Coding Sequence	(z;a,b,c,d)
-----------------	-------------

<b>EO3</b>	<b>3 INPUT EXCLUSIVE-OR</b>	<b>EO3</b>
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**SYMBOL**



**TRUTH TABLE**

Input			Output
A	B	C	Z
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	H

**CHARACTERISTICS**

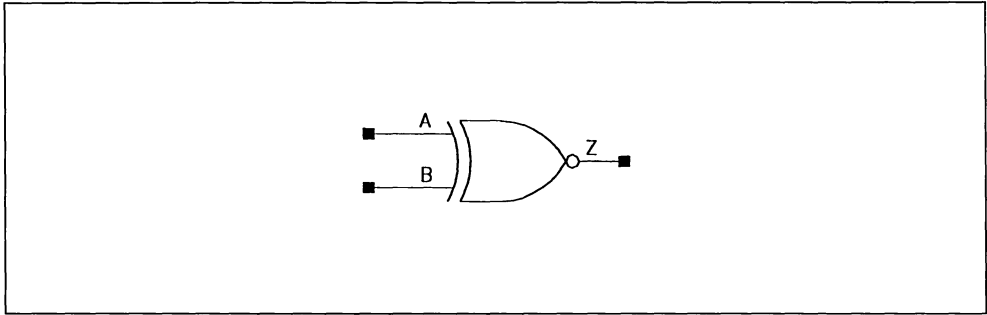
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A,B,C to Z	t <sub>PHL</sub>	5.00	5.20	5.40	5.60	6.30	4
	t <sub>PLH</sub>	4.80	5.00	5.20	5.50	6.50	

Input Load			Output Drive
A	B	C	Z
2	2	2	22

<b>Coding Sequence</b>	(z;a,b,c)
------------------------	-----------

<b>EN</b>	<b>2-INPUT EXCLUSIVE-NOR</b>	<b>EN</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
A	B	Z
L	L	H
H	L	L
L	H	L
H	H	H

**CHARACTERISTICS**

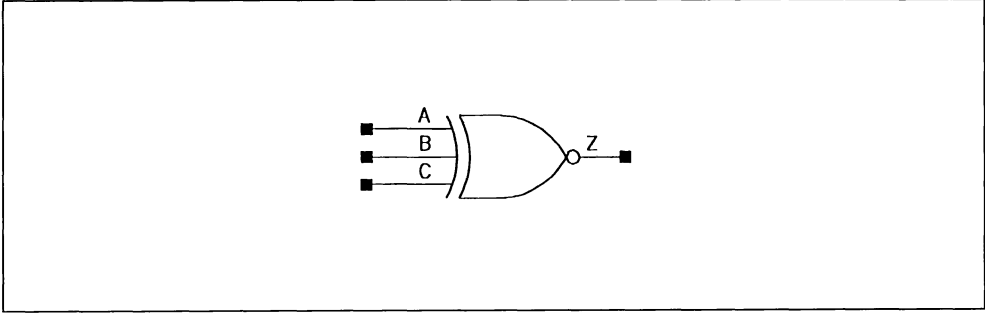
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A,B to Z	t <sub>PHL</sub>	2.17	2.35	2.53	2.70	3.42	2
	t <sub>PLH</sub>	2.37	2.63	2.88	3.14	4.16	

Input Load		Output Drive
A	B	Z
2	2	22

Coding Sequence	(z;a,b)
-----------------	---------

<b>EN3</b>	<b>3 INPUT EXCLUSIVE-NOR</b>	<b>EN3</b>
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**SYMBOL**



**TRUTH TABLE**

Input			Output
A	B	C	Z
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	H
H	H	H	L

**CHARACTERISTICS**

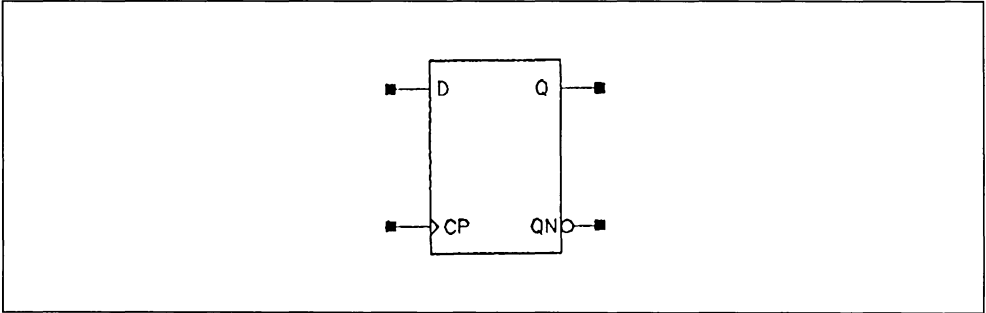
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A,B,C to Z	t <sub>PHL</sub>	4.2	4.4	4.6	4.8	5.7	4
	t <sub>PLH</sub>	4.7	4.9	5.1	5.4	6.3	

Input Load			Output Drive
A	B	C	Z
2	2	2	22

Coding Sequence	(z;a,b,c)
-----------------	-----------

<b>FD1</b>	<b>D FLIP FLOP</b>	<b>FD1</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output	
D	CP	Q	QN
L		L	H
H		H	L

**CHARACTERISTICS**

		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
CP to QN	t <sub>PHL</sub>	3.0	3.2	3.3	3.4	3.9	4
	t <sub>PLH</sub>	3.2	3.4	3.5	3.6	4.1	

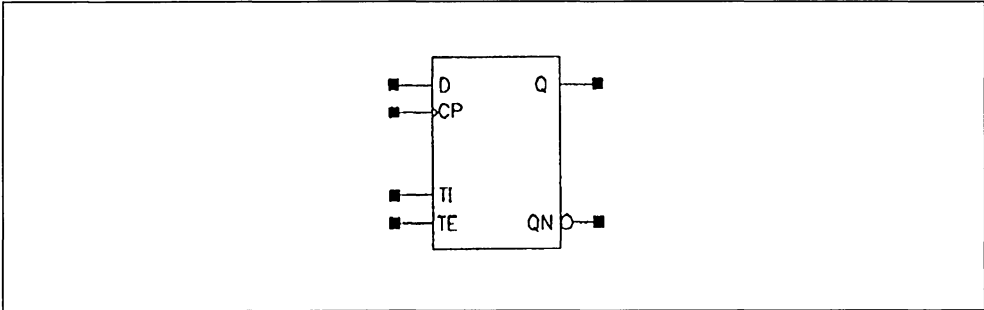
Input Load		Output Drive	
D	CP	Q	QN
1	1	20	20

Coding Sequence	(q,qn;d,cp)
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<b>FD1S</b>	<b>D FLIP FLOP WITH SCAN</b>	<b>FD1S</b>
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**SYMBOL**



**TRUTH TABLE**

Input				Output	
D	TI	TE	CP	Q	QN
L	X	L		L	H
H	X	L		H	L
X	L	H		L	H
X	H	H		H	L

**CHARACTERISTICS**

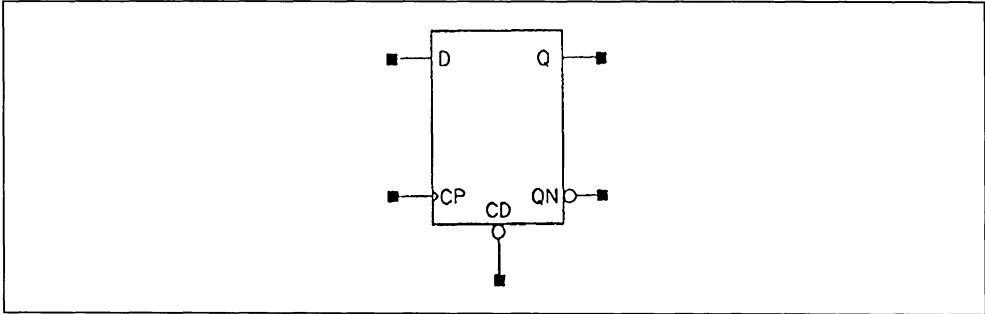
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
CP to QN	t <sub>PHL</sub>	3.7	3.9	4.1	4.3	5.1	7
	t <sub>PLH</sub>	3.7	3.9	4.1	4.3	5.2	

Input Load				Output Drive	
D	TI	TE	CP	Q	QN
1	1	1	2	20	20

Coding Sequence	(q,qn;d,cp,ti,te)
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<b>FD2</b>	<b>D FLIP FLOP WITH CLEAR</b>	<b>FD2</b>
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**SYMBOL**



**TRUTH TABLE**

Input			Output	
D	CP	CD	Q	QN
L		H	L	H
H		H	H	L
X	X	L	L	H

**CHARACTERISTICS**

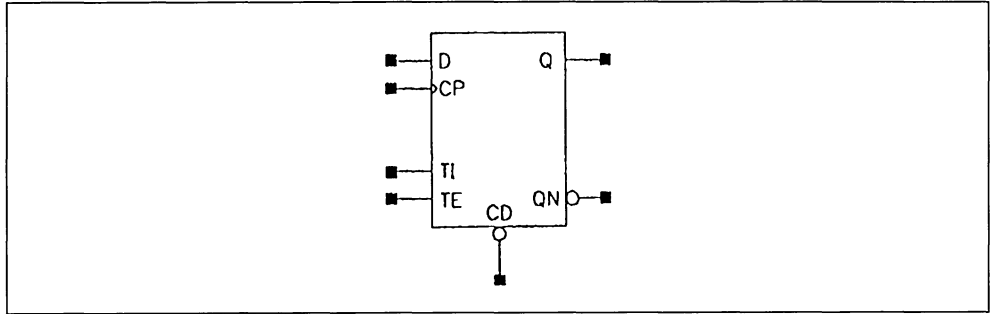
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
C to QN	t <sub>PHL</sub>	3.4	3.7	3.9	4.2	5.2	4
	t <sub>PLH</sub>	3.5	3.7	3.9	4.2	5.2	

Input Load			Output Drive	
D	CP	CD	Q	QN
1	1	2	20	20

Coding Sequence	(q,qn;d,cp,cd)
-----------------	----------------

<b>FD2S</b>	<b>D FLIP FLOP WITH SCAN &amp; CLEAR</b>	<b>FD2S</b>
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**SYMBOL**



**TRUTH TABLE**

Input					Output	
D	TI	TE	CP	CD	Q	QN
L	X	L		H	L	H
H	X	L		H	H	L
X	L	H		H	L	H
X	H	H		H	H	L
X	X	X	X	L	L	H

**CHARACTERISTICS**

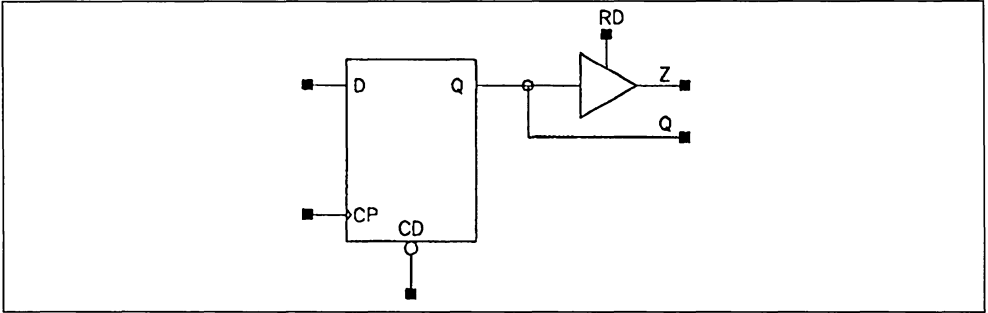
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
CP to QN	t <sub>PHL</sub>	3.5	3.7	4.0	4.2	5.1	8
	t <sub>PLH</sub>	3.5	3.7	4.0	4.2	5.1	

Input Load					Output Drive	
D	TI	TE	CP	CD	Q	QN
1	1	2	1	2	20	20

<b>Coding Sequence</b>	(q,qn;d,ti,te,cp,cd)
------------------------	----------------------

<b>FD2TS</b>	<b>D FLIP FLOP WITH CLEAR &amp; ADDED TRISTATE OUTPUT</b>	<b>FD2TS</b>
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**SYMBOL**



**TRUTH TABLE**

Input				Output	
D	CP	CD	RD	Z	Q
L		H	H	L	L
H		H	H	H	H
X	X	L	H	L	L
X	X	L	L	Z	L
H		H	L	Z	H
L		H	L	Z	L

**CHARACTERISTICS**

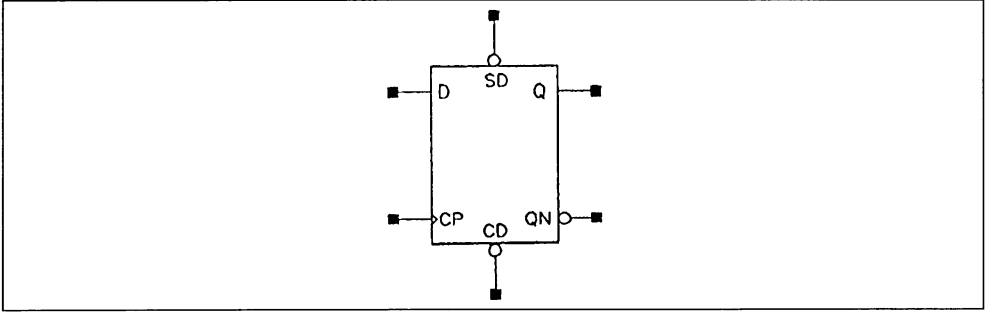
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
CP to QN	t <sub>PHL</sub>	4.1	4.2	4.4	4.5	5.1	7
	t <sub>PLH</sub>	4.4	4.7	4.9	5.1	6.0	

Input Load				Output Drive	
D	CP	CD	RD	Z	Q
1	1	2	2	20	20

Coding Sequence	(q,qn;d,cp,cd,rd)
-----------------	-------------------

<b>FD3</b>	<b>D FLIP FLOP WITH &amp; RESET</b>	<b>FD3</b>
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**SYMBOL**



**TRUTH TABLE**

Input				Output	
D	CP	CD	SD	Q	QN
L		H	H	L	H
H		H	H	H	L
X	X	L	H	L	H
X	X	H	L	H	L
X	X	L	L	H	H

**CHARACTERISTICS**

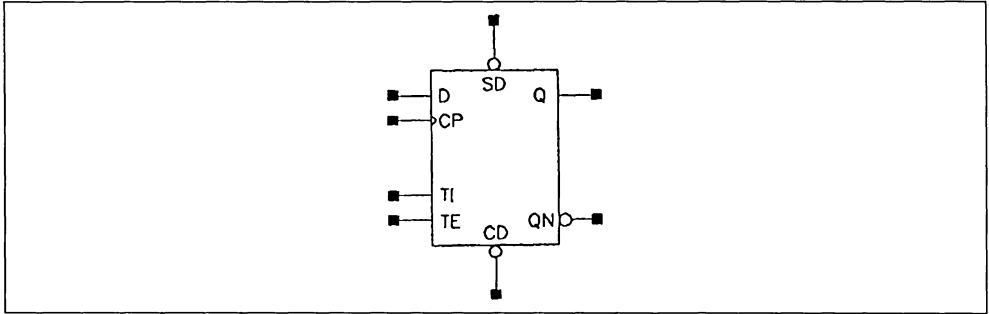
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
CP to QN	t <sub>PHL</sub>	4.4	4.9	5.5	6.0	8.0	6
	t <sub>PLH</sub>	4.5	5.0	5.5	6.0	7.9	

Input Load				Output Drive	
D	CP	CD	SD	Q	QN
1	1	2	2	20	20

<b>Coding Sequence</b>	(q,qn;d,cp,cd,sd)
------------------------	-------------------

<b>FD3S</b>	<b>D FLIP FLOP WITH SCAN, CLEAR &amp; PRESET</b>	<b>FD3S</b>
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**SYMBOL**



**TRUTH TABLE**

Input						Output	
D	TI	TE	CP	CD	SD	Q	QN
L	X	L	⌋	H	H	L	H
H	H	L	⌋	H	H	H	L
X	L	H	⌋	H	H	L	H
X	H	H	⌋	H	H	H	L
X	X	X	X	L	H	L	H
X	X	X	X	H	L	H	L
X	X	X	X	L	L	H	H

**CHARACTERISTICS**

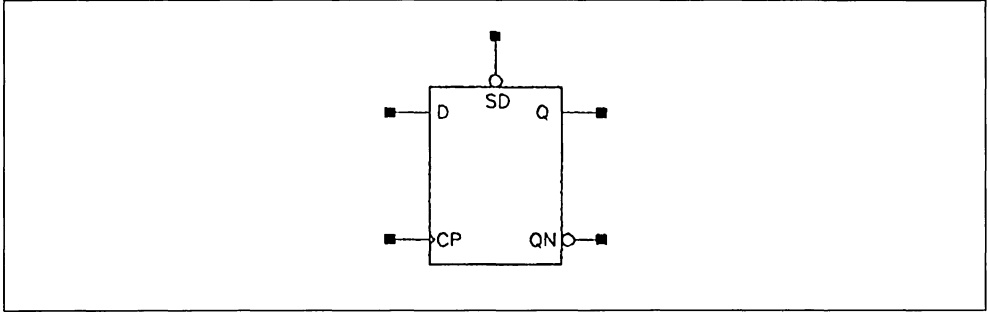
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
CP to QN	t <sub>PHL</sub>	1.3	5.0	5.5	6.9	7.8	10
	t <sub>PLH</sub>	1.3	5.1	5.5	6.0	7.9	

Input Load						Output Drive	
D	TI	TE	CP	CD	SD	Q	QN
1	1	2	1	2	2	20	20

<b>Coding Sequence</b>	(q,qn;d,ti,te,cp,cd,sd)
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<b>FD4</b>	<b>D FLIP FLOP WITH PRESET</b>	<b>FD4</b>
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**SYMBOL**



**TRUTH TABLE**

Input			Output	
D	CP	SD	Q	QN
L		H	L	H
H		H	H	L
X	X	L	H	L

**CHARACTERISTICS**

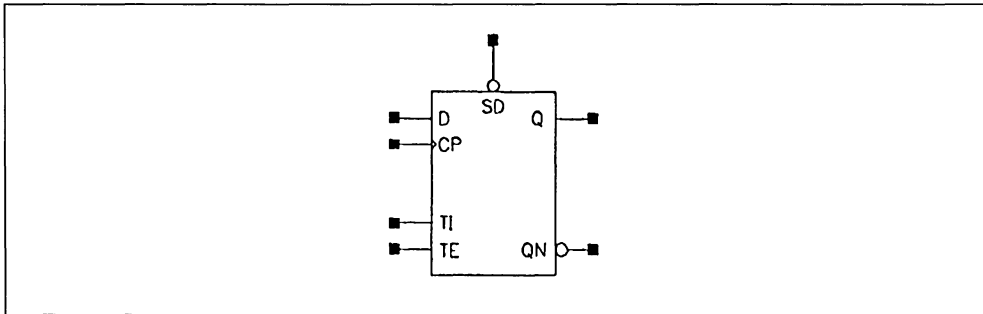
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
CP to QN	t <sub>PHL</sub>	4.3	4.7	5.0	5.4	6.9	8
	t <sub>PLH</sub>	4.5	5.0	5.4	5.9	7.7	

Input Load			Output Drive	
D	CP	SD	Q	QN
1	1	2	20	20

Coding Sequence	(q,qn;d,cp,sd)
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<b>FD4S</b>	<b>D FLIP FLOP WITH SCAN &amp; PRESET</b>	<b>FD4S</b>
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**SYMBOL**



**TRUTH TABLE**

Input					Output	
D	TI	TE	CP	SD	Q	QN
L	X	L		H	L	H
H	X	L		H	H	L
X	L	H		H	L	H
X	H	H		H	H	L
X	X	X	X	L	L	H

**CHARACTERISTICS**

		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
CP to QN	t <sub>PHL</sub>	4.2	4.6	4.9	5.3	6.8	8
	t <sub>PLH</sub>	4.4	4.9	5.3	5.8	7.6	

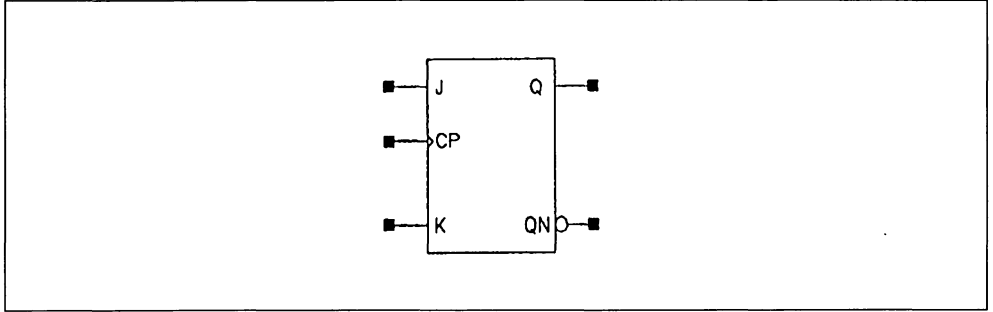
Input Load					Output Drive	
D	TI	TE	CP	SD	Q	QN
1	1	2	1	2	20	20

<b>Coding Sequence</b>	(q,qn;d,ti,te,cp,sd)
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<b>FJK1</b>	<b>J K FLIP FLOP</b>	<b>FJK1</b>
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**SYMBOL**



**TRUTH TABLE**

Input			Output	
J	K	CP	Q	QN
L	L		Q	QN
L	H		L	H
H	L		H	L
H	H		QN	Q

**CHARACTERISTICS**

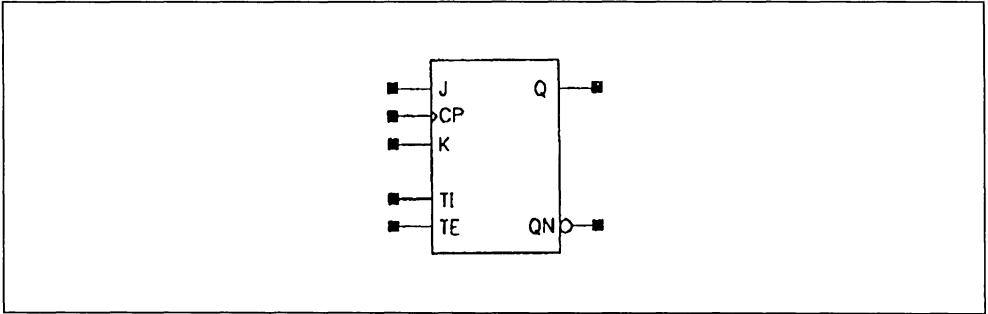
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
CP to QN	t <sub>PHL</sub>	3.1	3.2	3.3	3.4	3.8	6
	t <sub>PLH</sub>	3.2	3.3	3.5	3.6	4.2	

Input Load			Output Drive	
J	K	CP	Q	QN
1	1	1	20	20

<b>Coding Sequence</b>	(q,qn;j,k,cp)
------------------------	---------------

<b>FJK1S</b>	<b>J K FLIP FLOP WITH SCAN</b>	<b>FJK1S</b>
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**SYMBOL**



**TRUTH TABLE**

Input					Output	
J	K	TI	TE	CP	Q	QN
L	L	X	L		Q	QN
L	H	X	L		L	H
H	L	X	L		H	L
H	H	X	L		Q	QN
X	X	L	H		L	H
X	X	H	H		H	L

**CHARACTERISTICS**

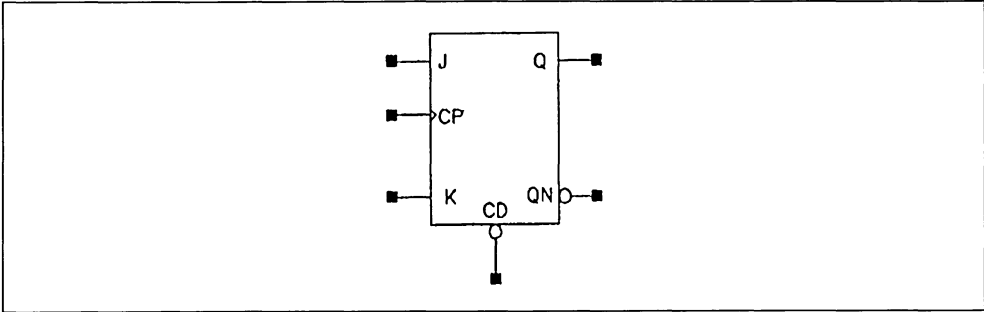
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
CP to QN	t <sub>PHL</sub>	3.7	3.9	4.1	4.3	5.1	9
	t <sub>PLH</sub>	3.7	3.9	4.2	4.4	5.2	

Input Load					Output Drive	
J	K	TI	TE	CP	Q	QN
1	1	1	2	1	20	20

<b>Coding Sequence</b>	(q,qn,j,k,ti,te,cp)
------------------------	---------------------

<b>FJK2</b>	<b>J K FLIP FLOP WITH CLEAR</b>	<b>FJK2</b>
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**SYMBOL**



**TRUTH TABLE**

Input				Output	
J	K	CP	CD	Q	QN
X	X	X	L	L	H
L	L		H	Q	QN
L	H		H	L	H
H	L		H	H	L
H	H		H	QN	Q

**CHARACTERISTICS**

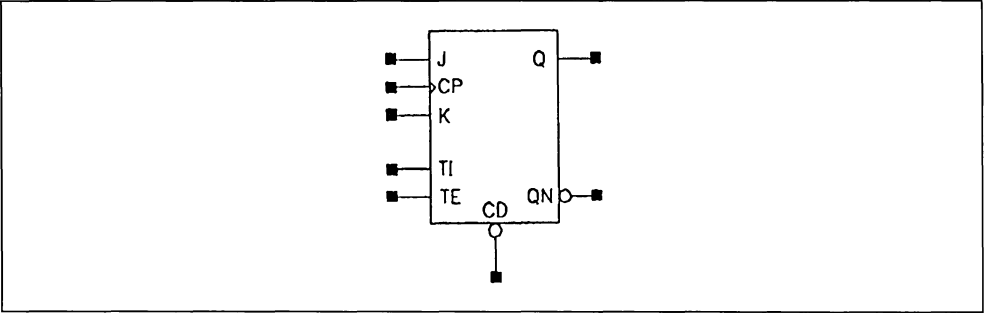
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
CP to QN	t <sub>PHL</sub>	3.5	3.8	4.0	4.3	5.3	6
	t <sub>PLH</sub>	3.6	3.8	4.0	4.3	5.2	

Input Load				Output Drive	
J	K	CP	CD	Q	QN
1	1	1	2	20	20

Coding Sequence	(q,qn,j,k,cp,cd)
-----------------	------------------

<b>FJK2S</b>	<b>J K FLIP FLOP WITH SCAN &amp; CLEAR</b>	<b>FJK2S</b>
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**SYMBOL**



**TRUTH TABLE**

Input						Output	
J	K	TI	TE	CP	CD	Q	QN
L	L	X	L		H	Q	QN
L	H	X	L		H	L	H
H	L	X	L		H	H	L
H	H	X	L		H	QN	Q
X	X	L	H		H	L	H
X	X	H	H		H	H	L
X	X	X	X	X	L	L	H

**CHARACTERISTICS**

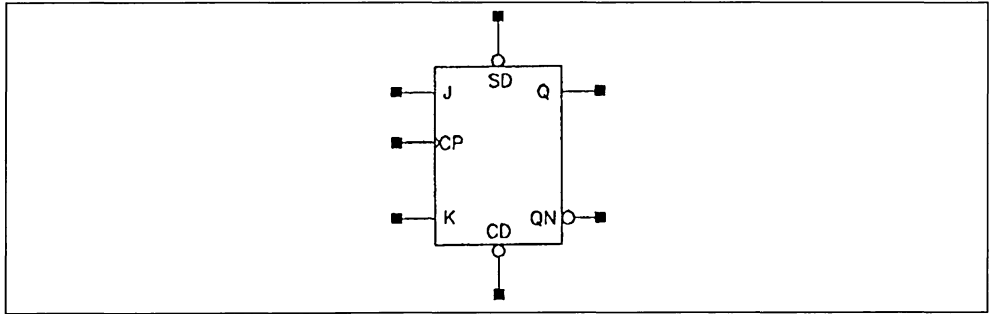
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
CP to QN	$t_{PHL}$	3.5	3.7	4.0	4.2	5.1	10
	$t_{PLH}$	3.6	3.8	4.0	4.2	5.1	

Input Load						Output Drive	
J	K	TI	TE	CP	CD	Q	QN
1	1	1	2	1	2	20	20

<b>Coding Sequence</b>	(q,qn;j,k,ti,te,cp,cd)
------------------------	------------------------

<b>FJK3</b>	<b>J K FLIP FLOP WITH CLEAR &amp; PRESET</b>	<b>FJK3</b>
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**SYMBOL**



**TRUTH TABLE**

Input					Output	
J	K	CP	CD	SD	Q	QN
X	X	X	L	H	L	H
X	X	X	H	L	H	L
X	X	X	L	L	H	H
L	L	⌋	H	H	Q	QN
L	H	⌋	H	H	L	H
H	L	⌋	H	H	H	L
H	H	⌋	H	H	QN	Q

**CHARACTERISTICS**

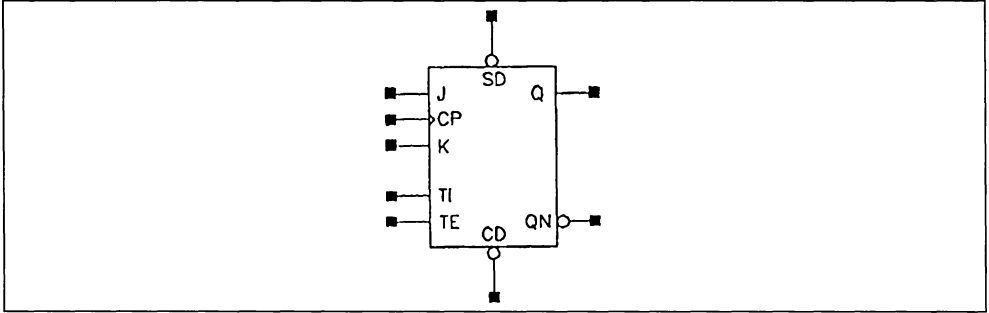
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
C to QN	t <sub>PHL</sub>	4.7	5.3	5.8	6.3	8.5	6
	t <sub>PLH</sub>	4.9	5.4	6.0	6.5	8.5	

Input Load					Output Drive	
J	K	CP	CD	SD	Q	QN
1	1	1	2	2	20	20

Coding Sequence	(q,qn,j,k,cp,cd,sd)
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<b>FJK3S</b>	<b>J K FLIP FLOP WITH SCAN, CLEAR &amp; PRESET</b>	<b>FJK3S</b>
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**SYMBOL**



**TRUTH TABLE**

Input							Output	
J	K	TI	TE	CP	CD	SD	Q	QN
L	L	X	L		H	H	Q	QN
L	H	X	L		H	H	L	H
H	L	X	L		H	H	H	L
H	H	X	L		H	H	QN	Q
X	X	L	H		H	H	L	H
X	X	H	H		H	H	H	L
X	X	X	X	X	L	H	L	H
X	X	X	X	X	H	L	H	L
X	X	X	X	X	L	L	H	H

**CHARACTERISTICS**

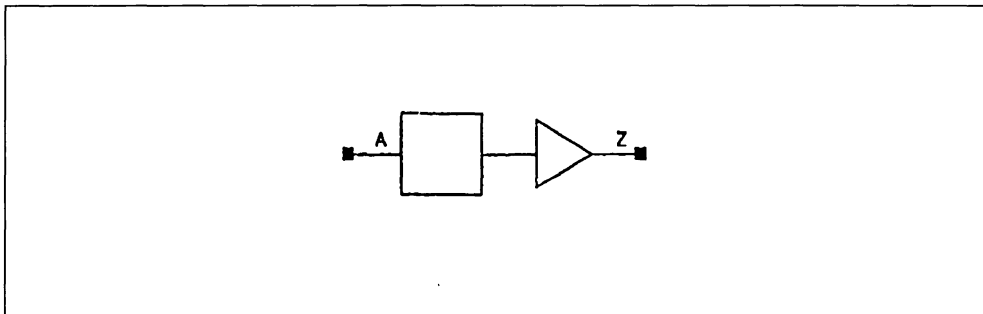
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
C to QN	t <sub>PHL</sub>	3.7	4.2	4.6	4.1	7.0	12
	t <sub>PLH</sub>	3.8	4.3	4.7	5.2	7.1	

Input Load							Output Drive	
J	K	TI	TE	CP	CD	SD	Q	QN
1	1	1	2	1	2	2	20	20

Coding Sequence	(q,qn,j,k,ti,te,cp,cd,sd)
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<b>IBUF</b>	<b>INPUT PAD WITH BUFFER FOR CMOS INPUT</b>	<b>IBUF</b>
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**SYMBOL**



**TRUTH TABLE**

A	Z
H	H
L	L

**CHARACTERISTICS**

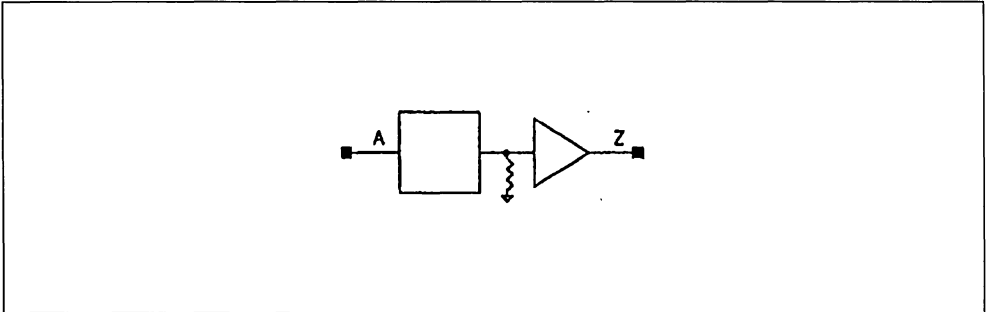
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A to Z	$t_{PHL}$	5.1	5.7	6.1	6.5	8.0	0
	$t_{PLH}$	4.1	4.6	5.1	5.6	7.6	

<b>Input Load</b>	<b>Output Drive</b>
A	Z
7	69

<b>Coding Sequence</b>	(z;a)
------------------------	-------

<b>IBUFD</b>	<b>INPUT PAD WITH PULL DOWN RESISTOR, BUFFER FOR CMOS INPUT</b>	<b>IBUFD</b>
--------------	---	--------------

**SYMBOL**



**TRUTH TABLE**

A	Z
H	H
L	L
Hi-Z	L

**CHARACTERISTICS**

		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A to Z	$t_{PHL}$	5.4	5.8	6.2	6.6	8.0	0
	$t_{PLH}$	4.2	4.7	5.2	5.7	7.7	

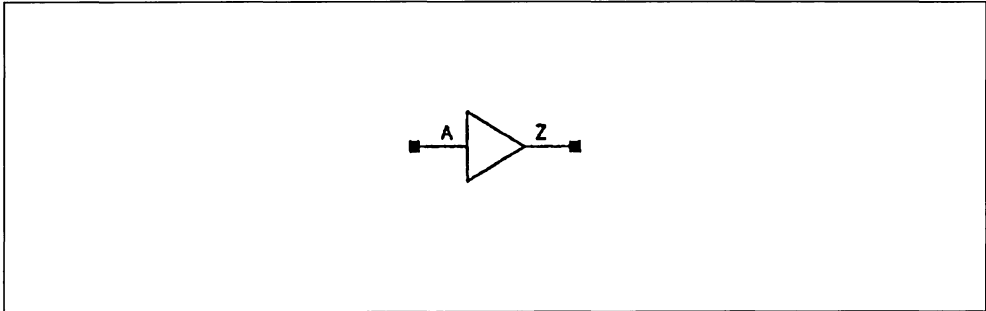
Input Load	Output Drive
A	Z
7	69

Coding Sequence	(z;a)
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<b>IBUFI</b>	<b>BUFFER FOR CMOS BIDIRECTIONAL INPUT</b>	<b>IBUFI</b>
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**SYMBOL**



**TRUTH TABLE**

<b>A</b>	<b>Z</b>
H	H
L	L

**CHARACTERISTICS**

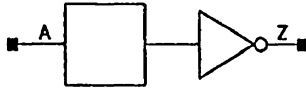
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A to Z	t <sub>PHL</sub>	1.4	1.6	1.7	1.9	2.6	2
	t <sub>PLH</sub>	1.5	1.7	1.9	2.1	3.2	

<b>Input Load</b>	<b>Output Drive</b>
<b>A</b>	<b>Z</b>
2	31

<b>Coding Sequence</b>	(z;a)
------------------------	-------

<b>IBUFN</b>	<b>INVERTING INPUT PAD WITH BUFFER FOR CMOS INPUT</b>	<b>IBUFN</b>
--------------	---	--------------

**SYMBOL**



**TRUTH TABLE**

A	Z
H	L
L	H

**CHARACTERISTICS**

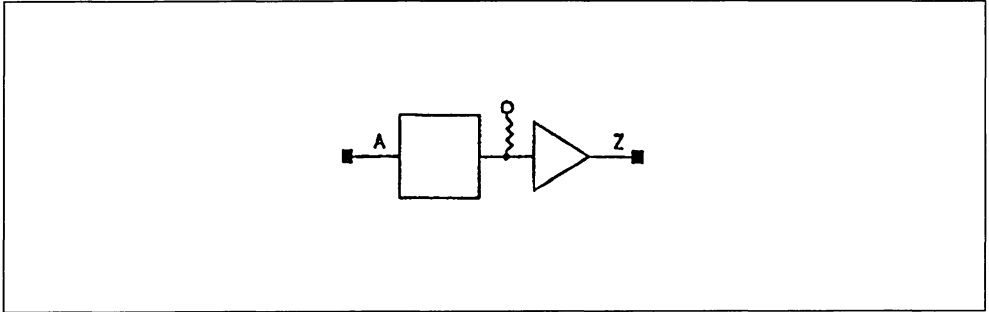
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A to Z	$t_{PHL}$	1.1	1.2	1.3	1.5	1.6	0
	$t_{PLH}$	0.8	0.9	1.0	1.0	1.3	

<b>Input Load</b>	<b>Output Drive</b>
A	Z
6	31

<b>Coding Sequence</b>	(z;a)
------------------------	-------

<b>IBUFU</b>	<b>INPUT PAD WITH PULL UP RESISTOR, BUFFER FOR CMOS INPUT</b>	<b>IBUFU</b>
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**SYMBOL**



**TRUTH TABLE**

A	Z
H	H
L	L
Hi-Z	H

**CHARACTERISTICS**

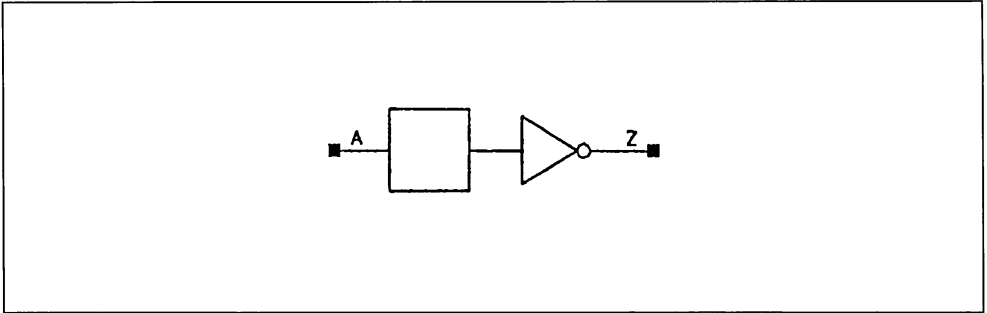
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A to Z	$t_{PHL}$	1.7	1.7	1.8	1.8	2.0	6
	$t_{PLH}$	1.0	1.0	1.1	1.6	1.3	

<b>Input Load</b>	<b>Output Drive</b>
A	Z
6	31

<b>Coding Sequence</b>	(z;a)
------------------------	-------

<b>ICK1</b>	<b>INVERTING CLOCK DRIVER</b>	<b>ICK1</b>
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**SYMBOL**



**TRUTH TABLE**

<b>A</b>	<b>Z</b>
H	L
L	H

**CHARACTERISTICS**

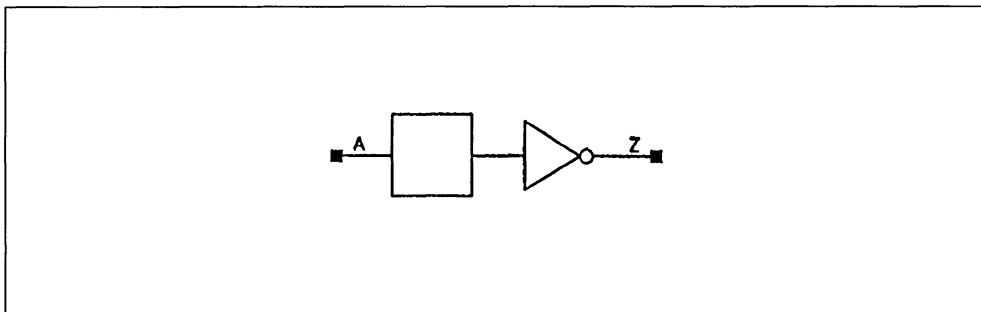
		Propagation Delay (ns)					Cell Usage
		FO 4	FO 8	FO 16	FO 32	FO 64	
A to Z	$t_{PHL}$	7.3	7.4	7.6	7.9	8.7	1
	$t_{PLH}$	8.3	8.4	8.6	9.0	9.9	

<b>Input Load</b>	<b>Output Drive</b>
<b>A</b>	<b>Z</b>
7	114

<b>Coding Sequence</b>	(z;a)
------------------------	-------

<b>ICK2</b>	<b>INVERTING CLOCK DRIVER</b>	<b>ICK2</b>
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**SYMBOL**



**TRUTH TABLE**

<b>A</b>	<b>Z</b>
H	L
L	H

**CHARACTERISTICS**

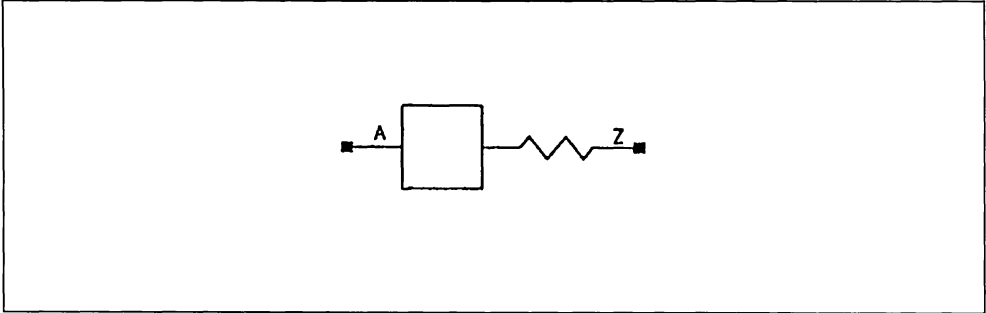
		Propagation Delay (ns)					Cell Usage
		FO 4	FO 8	FO 16	FO 32	FO 64	
A to Z	t <sub>PHL</sub>	10.3	10.4	10.5	10.7	11.0, 2,	
	t <sub>PLH</sub>	10.7	10.7	10.8	11.0	11.5	

<b>Input Load</b>	<b>Output Drive</b>
<b>A</b>	<b>Z</b>
7	114

<b>Coding Sequence</b>	(z;a)
------------------------	-------

<b>INPAD</b>	<b>INPUT PAD</b>	<b>INPAD</b>
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**SYMBOL**



**TRUTH TABLE**

<b>A</b>	<b>Z</b>
H	H
L	L

**CHARACTERISTICS**

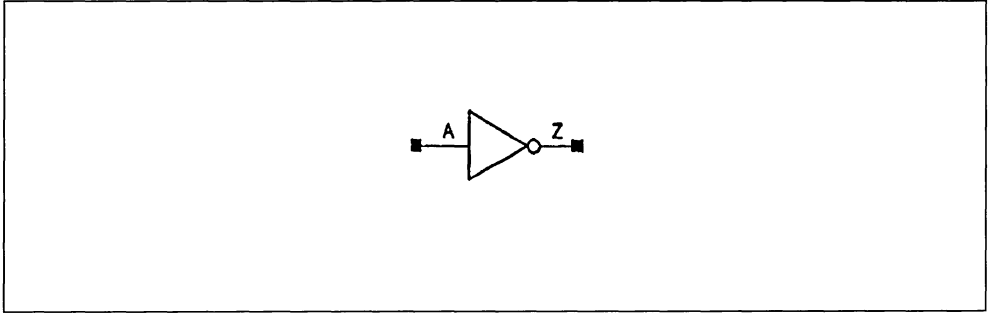
		Propagation Delay (ns)					Cell Usage
		FO 4	FO 8	FO 16	FO 32	FO 64	
A to Z	$t_{PHL}$	0.3	0.5	1.0	1.9	3.8	0
	$t_{PLH}$	0.3	0.5	1.0	1.9	3.8	

<b>Input Load</b>	<b>Output Drive</b>
<b>A</b>	<b>Z</b>
5	76

<b>Coding Sequence</b>	(z;a)
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<b>IV</b>	<b>INVERTER</b>	<b>IV</b>
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**SYMBOL**



**TRUTH TABLE**

Input	Output
A	Z
H	L
L	H

**CHARACTERISTICS**

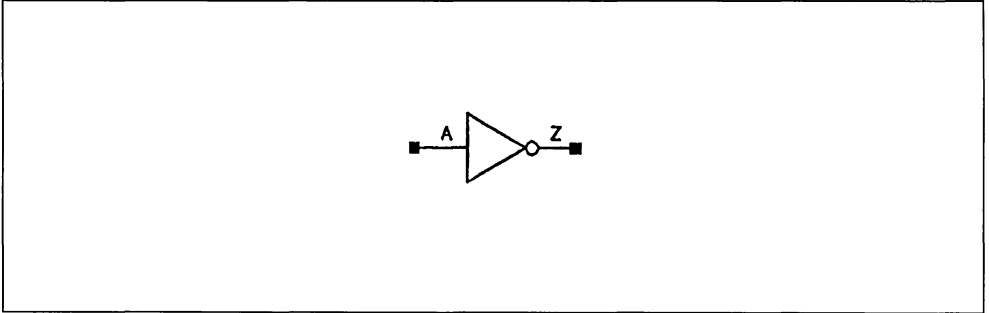
		Propagation Delay (ns)					Cell Usage
		FO 4	FO 8	FO 16	FO 32	FO 64	
A to Z	$t_{PHL}$	1.3	2.3	4.2	7.9	15.5	1
	$t_{PLH}$	1.6	2.6	4.6	8.6	16.6	

Input Load	Output Drive
A	Z
1	22

Coding Sequence	(z;a)
-----------------	-------

<b>IVA</b>	<b>POWER INVERTER</b>	<b>IVA</b>
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**SYMBOL**



**TRUTH TABLE**

Input	Output
A	Z
H	L
L	H

**CHARACTERISTICS**

		Propagation Delay (ns)					Cell Usage
		FO 4	FO 8	FO 16	FO 32	FO 64	
A to Z	$t_{PHL}$	0.8	1.3	2.3	4.2	8.1	1
	$t_{PLH}$	1.1	1.6	2.6	4.5	8.6	

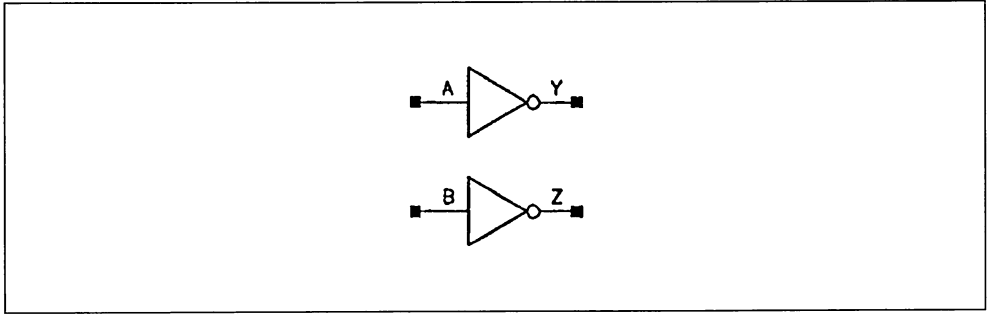
Input Load	Output Drive
A	Z
2	22

Coding Sequence	(z;a)
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<b>IVD</b>	<b>2 SINGLE INVERTERS</b>	<b>IVD</b>
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**SYMBOL**



**TRUTH TABLE**

Input	Output
A or B	Z or Y
H	L
L	H

**CHARACTERISTICS**

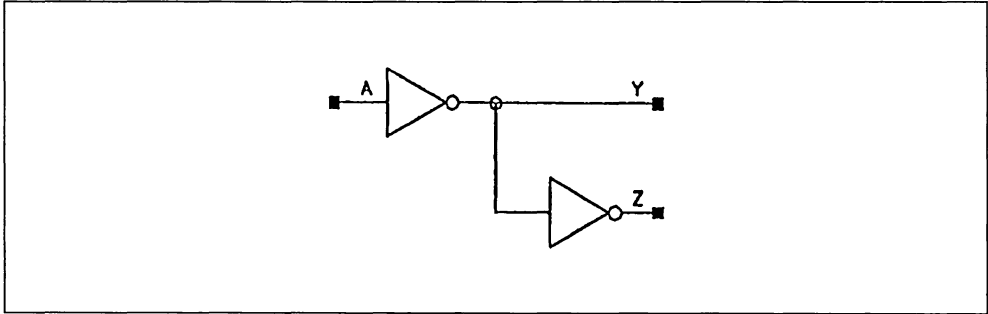
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A to Z	$t_{PHL}$	0.7	0.9	1.1	1.3	2.0	1
	$t_{PLH}$	1.0	1.2	1.4	1.6	2.5	

Input Load		Output Drive	
A	B	Y	Z
1	1	22	22

Coding Sequence	(y,z;a,b)
-----------------	-----------

<b>IVDA</b>	<b>INVERTER INTO INVERTER</b>	<b>IVDA</b>
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**SYMBOL**



**TRUTH TABLE**

Input	Output	
A	Y	Z
H	L	H
L	H	L

**CHARACTERISTICS**

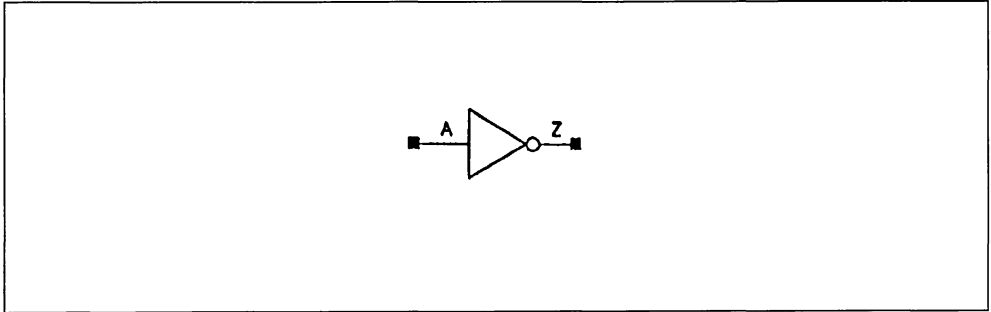
		Propagation Delay (ns)					Cell Usage
		FO 4	FO 8	FO 16	FO 32	FO 64	
A to Z	t <sub>PHL</sub>	2.1	2.4	2.8	3.1	4.5	1
	t <sub>PLH</sub>	1.5	1.6	1.7	1.8	2.2	

Input Load	Output Drive	
A	Y	Z
2	21	22

Coding Sequence	(y,z;a)
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<b>IVP</b>	<b>POWER INVERTER (2X)</b>	<b>IVP</b>
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**SYMBOL**



**TRUTH TABLE**

Input	Output
A	Z
H	L
L	H

**CHARACTERISTICS**

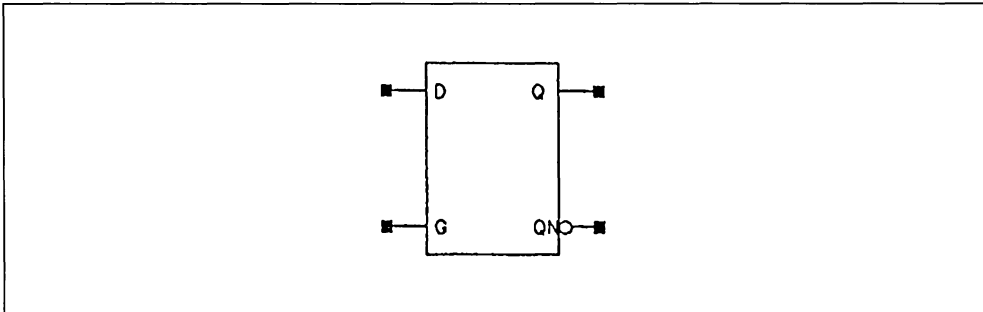
		Propagation Delay (ns)					Cell Usage
		FO 4	FO 8	FO 16	FO 32	FO 64	
A to Z	$t_{PHL}$	0.8	1.3	2.3	4.2	8.1	1
	$t_{PLH}$	1.1	1.6	2.6	4.6	8.6	

Input Load	Output Drive
A	Z
2	31

Coding Sequence	(z;a)
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<b>LD1</b>	<b>D TRANSPARENT LATCH WITH HIGH ENABLE</b>	<b>LD1</b>
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**SYMBOL .**



**TRUTH TABLE**

Input		Output	
D	G	Q	QN
L	H	L	H
H	H	H	L
X	L	Q	QN

**CHARACTERISTICS**

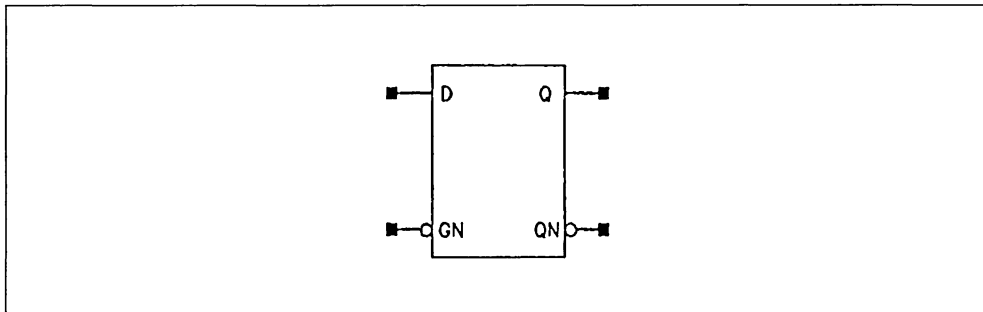
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
G to QN	t <sub>PHL</sub>	2.6	2.9	3.1	3.3	4.2	4
	t <sub>PLH</sub>	2.4	2.6	2.9	3.1	4.0	

Input Load		Output Drive	
D	G	Q	QN
1	1	20	20

<b>Coding Sequence</b>	(q,qn;d,g)
------------------------	------------

<b>LD2</b>	<b>D TRANSPARENT LATCH WITH LOW ENABLE</b>	<b>LD2</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output	
D	GN	Q	QN
L	L	L	H
H	L	H	L
X	H	Q	QN

**CHARACTERISTICS**

		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
GN to QN	t <sub>PHL</sub>	2.6	2.8	3.1	3.3	4.2	3
	t <sub>PLH</sub>	2.4	2.6	2.8	3.1	4.0	

Input Load		Output Drive	
D	GN	Q	QN
1	1	20	20

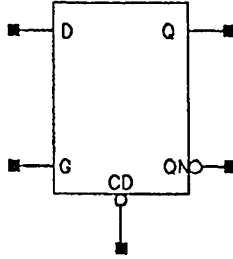
Coding Sequence	(q,qn;d,gn)
-----------------	-------------

LD3

D TRANSPARENT LATCH WITH  
HIGH ENABLE AND CLEAR

LD3

## SYMBOL



## TRUTH TABLE

Input			Output	
D	G	CD	Q	QN
L	H	H	L	H
H	H	H	H	L
X	L	H	Q	QN
X	X	L	L	H

## CHARACTERISTICS

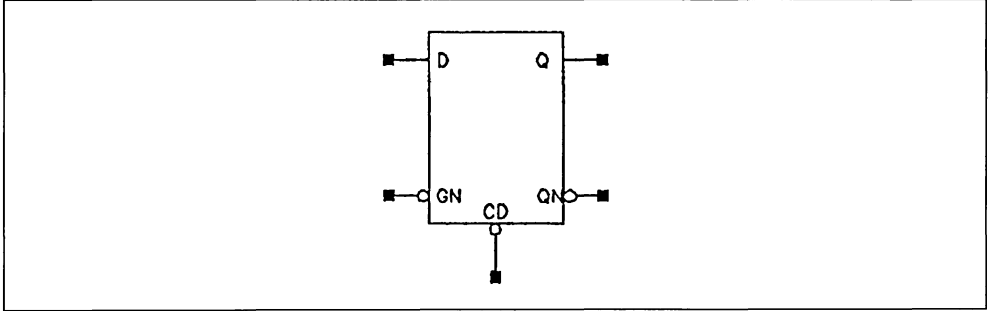
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
G to QN	t <sub>PHL</sub>	2.6	2.8	3.1	3.3	4.2	4
	t <sub>PLH</sub>	2.4	2.6	2.9	3.1	4.0	

Input Load			Output Drive	
D	G	CD	Q	QN
1	2	1	20	20

Coding Sequence	(q,qn;d,g,cd)
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<b>LD4</b>	<b>D TRANSPARENT LATCH WITH LOW ENABLE AND CLEAR DIRECT</b>	<b>LD4</b>
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**SYMBOL**



**TRUTH TABLE**

Input			Output	
D	GN	CD	Q	QN
L	L	H	L	H
H	L	H	H	L
X	X	L	L	H
X	H	H	Q	QN

**CHARACTERISTICS**

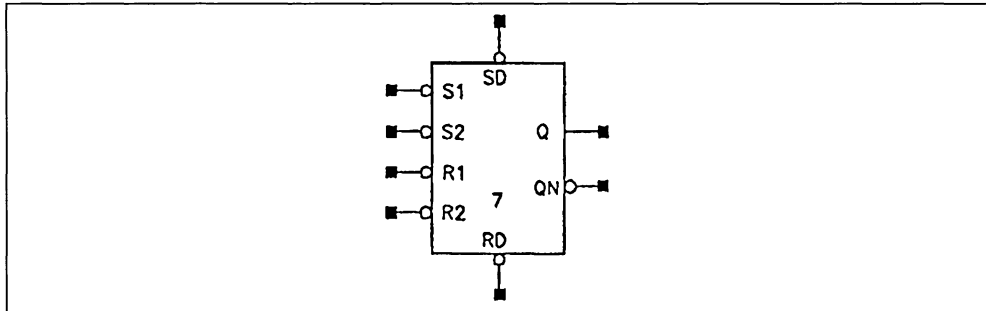
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
GN to QN	t <sub>PHL</sub>	2.6	2.8	3.1	3.3	4.2	4
	t <sub>PLH</sub>	2.4	2.6	2.9	3.1	4.0	

Input Load			Output Drive	
D	GN	CD	Q	QN
1	2	1	20	20

Coding Sequence	(q,qn;d,gn,cd)
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<b>LSR1</b>	<b>SR LATCH WITH SEPARATE GATED INPUTS</b>	<b>LSR1</b>
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**SYMBOL**



**TRUTH TABLE**

Input				Output	
S1,S2	R1,R2	SD	RD	Q	QN
X	X	L	H	H	L
X	X	H	L	L	H
X	X	L	L	H	H
H	H	H	H	Q	QN
H	L	H	H	L	H
L	H	H	H	H	L
L	L	H	H	H	H

**CHARACTERISTICS**

		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
C2 to Q	t <sub>PHL</sub>	4.1	4.8	5.6	6.4	9.5	4
	t <sub>PLH</sub>	2.3	2.7	3.1	3.6	5.3	

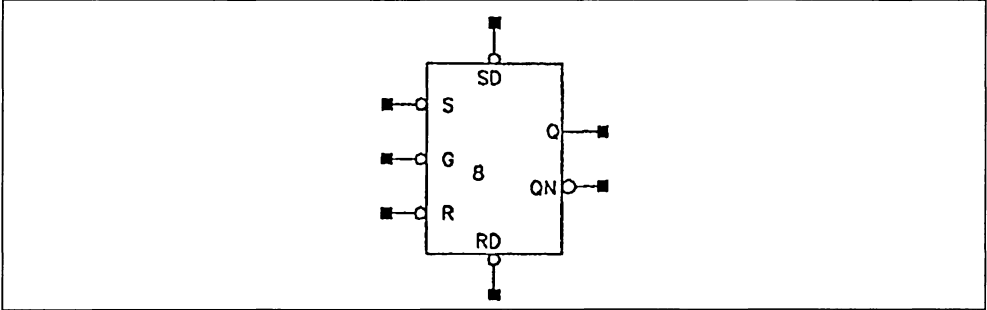
Input Load						Output Drive	
S1	S2	SD	R1	R2	RD	Q	QN
1	1	1	1	1	1	17	17

<b>Coding Sequence</b>	(q,qn;s1,s2,sd,r1,r2,rd)
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<b>LSR2</b>	<b>SR LATCH WITH COMMON GATED INPUTS</b>	<b>LSR2</b>
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**SYMBOL**



**TRUTH TABLE**

Input					Output	
S	R	G	SD	RD	Q	QN
X	X	X	L	H	H	L
X	X	X	H	L	L	H
X	X	X	L	L	H	H
X	X	H	H	H	Q	QN
H	H	L	H	H	Q	QN
H	L	L	H	H	L	H
L	H	L	H	H	H	L
L	L	L	H	H	H	H

**CHARACTERISTICS**

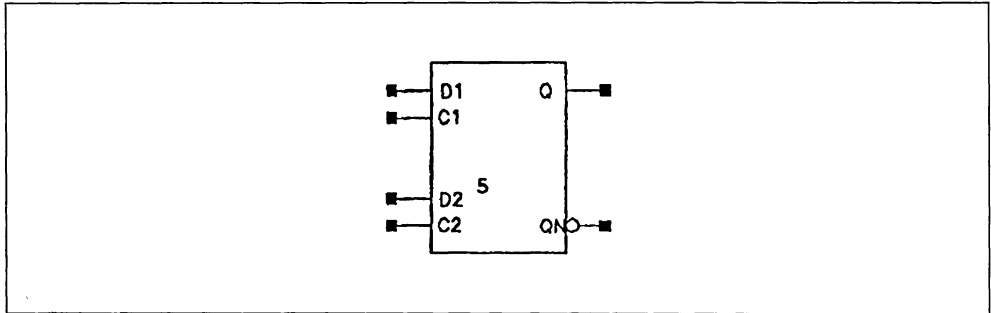
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
C3 to Q2N	t <sub>PHL</sub>	4.1	4.8	5.6	6.4	9.5	4
	t <sub>PLH</sub>	2.3	2.7	3.1	3.6	5.3	

Input Load					Output Drive	
S	R	G	SD	RD	Q	QN
1	1	1	1	1	17	17

Coding Sequence	(q,qn;s,r,g,sd,rd)
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<b>LS1</b>	<b>SR LATCH WITH COMMON GATED INPUTS</b>	<b>LS1</b>
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**SYMBOL**



**TRUTH TABLE**

Input				Output	
D1	C1	D2	C2	Q	QN
X	L	X	L	Q	QN
H	H	X	L	H	L
L	H	X	L	L	H
X	L	H	H	H	L
X	L	L	H	L	H
L	H	L	H	L	H
X	H	H	H	H	L
H	H	X	H	H	L

**CHARACTERISTICS**

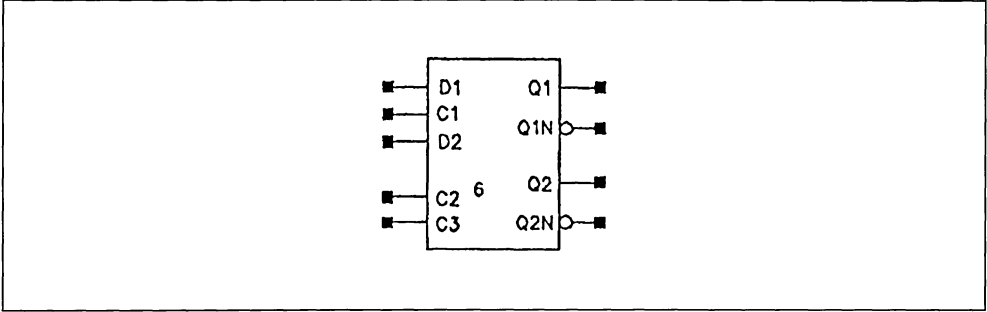
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
C2 to Q	t <sub>PHL</sub>	3.8	4.2	4.5	4.9	6.4	6
	t <sub>PLH</sub>	3.8	4.0	4.3	4.5	5.6	

Input Load				Output Drive	
D1	C1	D2	C2	Q	QN
1	2	1	2	18	18

Coding Sequence	(q,qn;d1,c1,d2,c2)
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LS2	SR LATCH WITH COMMON GATED INPUTS	LS2
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**SYMBOL**



**TRUTH TABLE**

Input					Output			
D1	C1	D2	C2	C3	Q1	Q1N	Q2	Q2N
X	X	X	X	L	—	—	Q2	Q2N
X	X	X	X	H	—	—	Q1	Q1N
X	L	X	L	X	Q1N	Q1N	—	—
H	H	X	L	X	H	L	—	—
L	H	X	L	X	L	H	—	—
X	L	H	H	X	H	L	—	—
X	L	L	H	X	L	H	—	—
L	H	L	H	X	L	H	—	—
X	H	H	H	X	H	L	—	—
H	H	X	H	X	H	L	—	—

**Note:** C3 input is the control clock for Q2/Q2N outputs and does not affect the state of Q1/Q1N.

**CHARACTERISTICS**

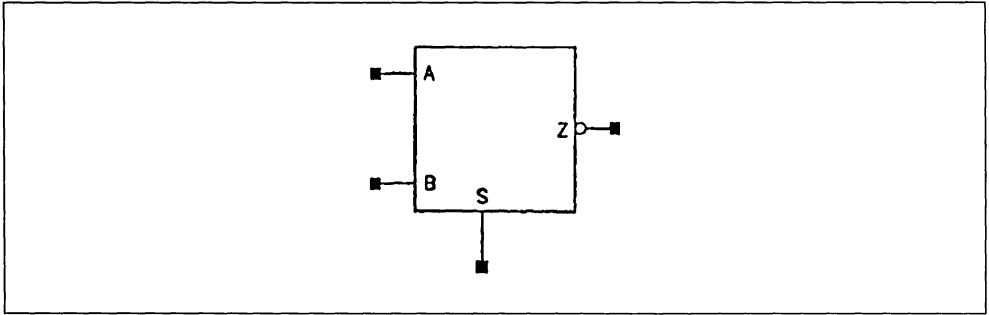
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
C3 to Q2N	t <sub>PHL</sub>	3.2	3.4	3.7	3.9	5.0	10
	t <sub>PLH</sub>	3.5	3.8	4.0	4.3	5.4	

Input Load					Output Drive			
D1	D2	C1	C2	C3	Q1	Q1N	Q2	Q2N
1	1	2	2	1	22	18	18	18

<b>Coding Sequence</b>	(q1,q1n,q2,q2n;d1,c1,d2,c2,c3)
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<b>MUX21L</b>	<b>INVERTING GATE MULTIPLEXER</b>	<b>MUX21L</b>
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**SYMBOL**



**TRUTH TABLE**

Input			Output
S	A	B	Z
L	L	X	H
L	H	X	L
H	X	L	H
H	X	H	L

**CHARACTERISTICS**

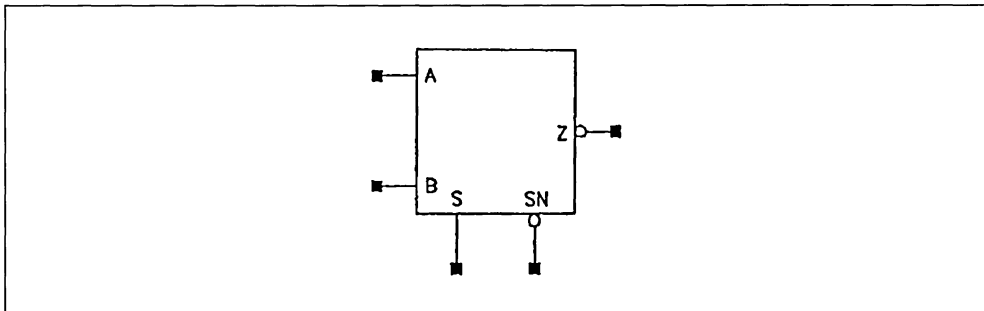
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A to Z	t <sub>PHL</sub>	1.22	1.32	1.42	1.52	1.93	2
	t <sub>PLH</sub>	1.15	1.27	1.40	1.53	2.04	

Input Load			Output Drive
A	B	S	Z
2	2	2	22

<b>Coding Sequence</b>	(z;a,b,s)
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<b>MUX21LA</b>	<b>2-1 TRANSMISSION GATE INVERTING MULTIPLEXER</b>	<b>MUX21LA</b>
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**SYMBOL**



**TRUTH TABLE**

Input				Output
A	SN	B	S	Z
H	H	H	X	L
X	X	H	H	L
L	X	L	X	H
X	L	L	X	H
L	X	X	L	H
X	L	X	L	H

**CHARACTERISTICS**

		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A to Z	t <sub>PHL</sub>	0.9	1.2	1.5	1.8	2.9	2
	t <sub>PLH</sub>	1.1	1.4	1.7	2.0	3.3	

Input Load				Output Drive
A	SN	B	S	Z
1	1	1	1	27

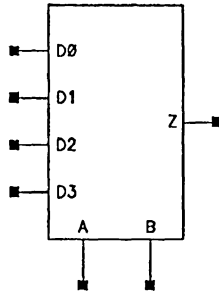
Coding Sequence	(z;sn,a,s,b)
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MUX41

4-BIT NON-INVERTING MULTIPLEXER

MUX41

## SYMBOL



## TRUTH TABLE

Input		Output
B	A	Z
L	L	D0
L	H	D1
H	L	D2
H	H	D3

## CHARACTERISTICS

		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A to Z	t <sub>PHL</sub>	2.7	2.8	2.9	3.0	3.4	6
	t <sub>PLH</sub>	2.6	2.7	2.9	3.0	3.5	

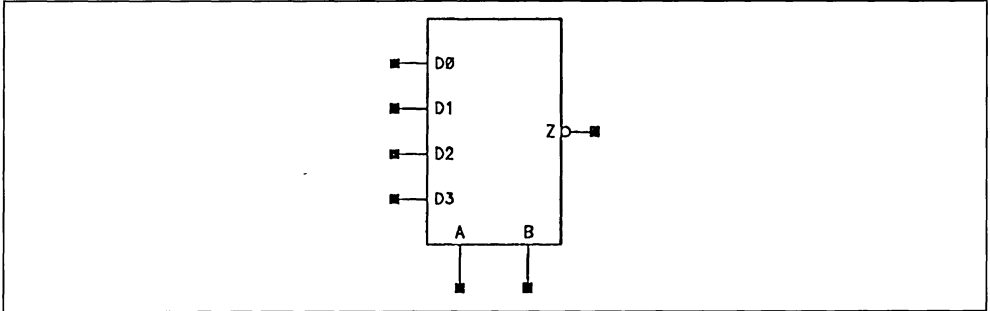
Input Load						Output Drive
D0	D1	D2	D3	A	B	Z
1	2	1	2	6	3	27

Coding Sequence

(z;d0,d1,d2,d3,a,b)

<b>MUX41L</b>	<b>4-TO-1 INVERTING MULTIPLEXER</b>	<b>MUX41L</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
B	A	Z
L	L	$\overline{D0}$
L	H	$\overline{D1}$
H	L	$\overline{D2}$
H	H	$\overline{D3}$

**CHARACTERISTICS**

		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A to Z	t <sub>PHL</sub>	3.1	3.3	3.4	3.6	4.1	7
	t <sub>PLH</sub>	3.4	3.6	3.8	4.1	5.0	

Input Load						Output Drive
A	B	D0	D1	D2	D3	Z
6	3	1	2	1	2	18

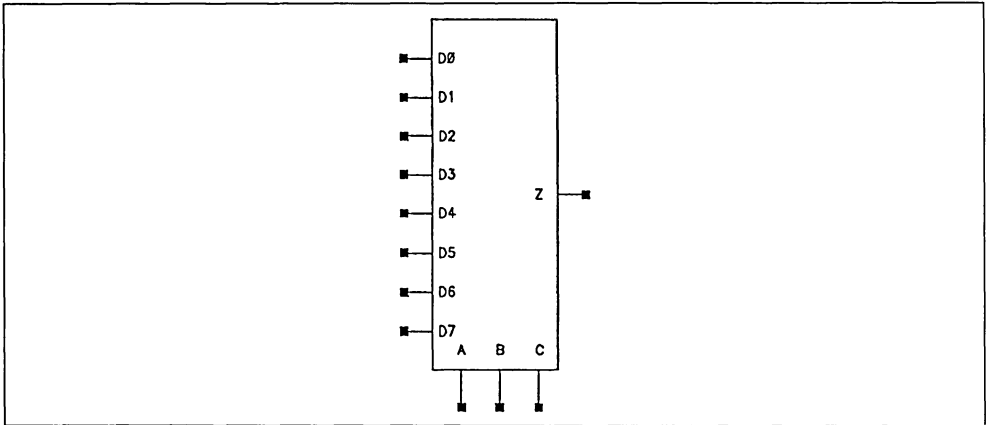
Coding Sequence	(z,d0,d1,d2,d3,a,b)
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**MUX81**

**8 BIT NON-INVERTING GATE MULTIPLEXER**

**MUX81**

**SYMBOL**



**TRUTH TABLE**

Input			Output
C	B	A	Z
L	L	L	D0
L	L	H	D1
L	H	L	D2
L	H	H	D3
H	L	L	D4
H	L	H	D5
H	H	L	D6
H	H	H	D7

**CHARACTERISTICS**

		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A to Z	t <sub>PHL</sub>	4.6	4.8	5.1	5.4	6.5	15
	t <sub>PLH</sub>	4.2	4.5	4.9	5.2	6.5	

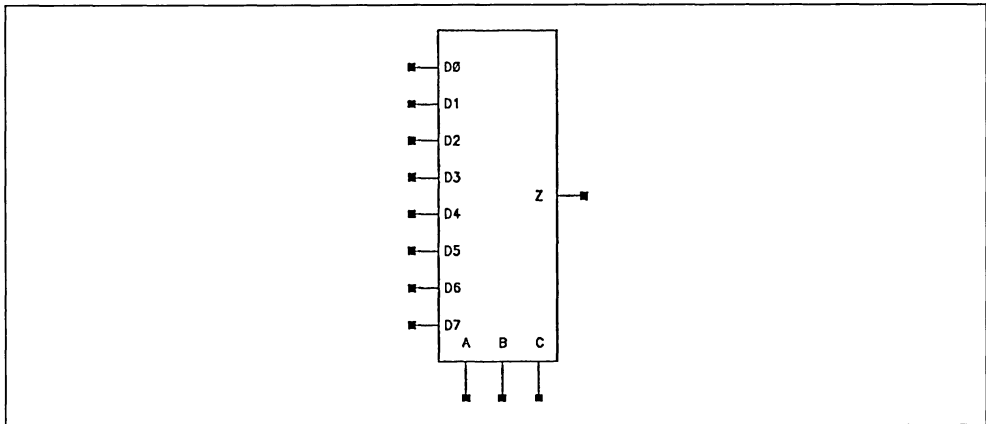
Input Load				Output Drive
A	B	C	D0 to D7	Z
6	5	2	1	18

Coding Sequence	(z;d0,d1,d2,d3,d4,d5,d6,d7,a,b,c)
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<b>MUX81H</b>	<b>8 BIT NON-INVERTING GATE MULTIPLEXER</b>	<b>MUX81H</b>
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**SYMBOL**



**TRUTH TABLE**

Input			Output
C	B	A	Z
L	L	L	D0
L	L	H	D1
L	H	L	D2
L	H	H	D3
H	L	L	D4
H	L	H	D5
H	H	L	D6
H	H	H	D7

**CHARACTERISTICS**

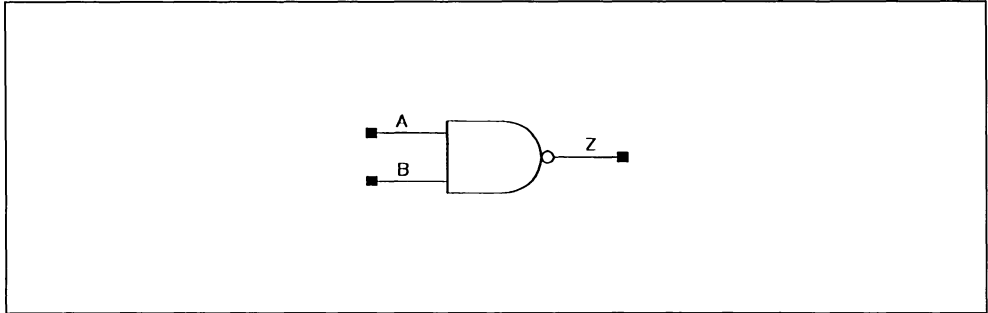
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A to Z	t <sub>PHL</sub>	4.5	4.8	5.1	5.4	6.5	15
	t <sub>PLH</sub>	4.2	4.6	4.9	5.2	6.5	

Input Load				Output Drive
A	B	C	D0 to D7	Z
6	5	2	1	18

Coding Sequence	(z;d0,d1,d2,d3,d4,d5,d6,d7,a,b,c)
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<b>ND2</b>	<b>2-INPUT NAND</b>	<b>ND2</b>
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**SYMBOL**



**TRUTH TABLE**

Input		Output
A	B	Z
H	H	L
X	L	H
L	X	H

**CHARACTERISTICS**

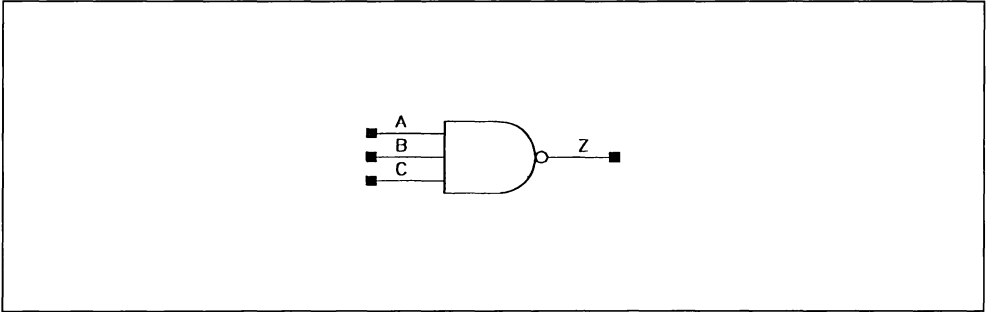
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A,B to Z	t <sub>PHL</sub>	0.81	1.08	1.35	1.62	2.69	1
	t <sub>PLH</sub>	1.01	1.25	1.50	1.74	2.71	

Input Load		Output Drive
A	B	Z
1	1	18

Coding Sequence	(z;a,b)
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<b>ND3</b>	<b>3-INPUT NAND</b>	<b>ND3</b>
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**SYMBOL**



**TRUTH TABLE**

Input			Output
A	B	C	Z
L	L	L	H
X	X	L	H
X	L	X	H
L	X	X	H

**CHARACTERISTICS**

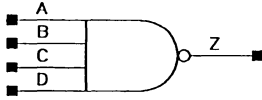
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A,B,C to Z	t <sub>PHL</sub>	1.14	1.47	1.80	2.13	3.46	1
	t <sub>PLH</sub>	1.15	1.40	1.65	1.89	2.88	

Input Load			Output Drive
A	B	C	Z
1	1	1	18

Coding Sequence	(z;a,b,c)
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<b>ND4</b>	<b>4-INPUT NAND</b>	<b>ND4</b>
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**SYMBOL**



**TRUTH TABLE**

Input				Output
A	B	C	D	Z
H	H	H	H	L
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H

**CHARACTERISTICS**

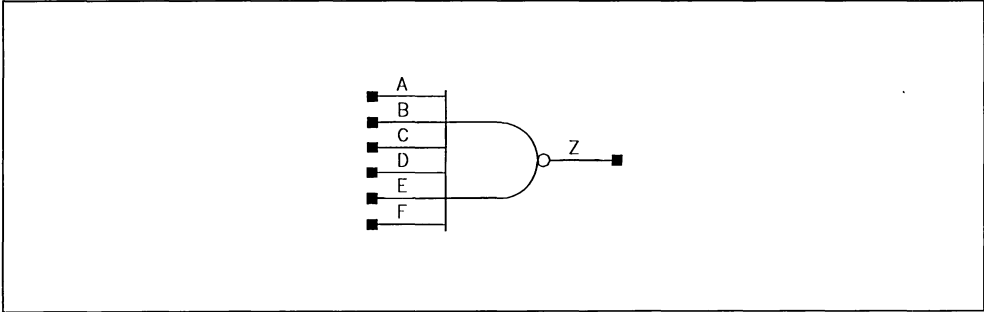
	Propagation Delay (ns)					Cell Usage
	FO 1	FO 2	FO 3	FO 4	FO 8	
A,B,C,D to Z — t <sub>PHL</sub>	1.7	2.1	2.5	2.9	4.5	2
— t <sub>PLH</sub>	1.3	1.6	1.8	2.1	3.1	

Input Load				Output Drive
A	B	C	D	Z
1	1	1	1	18

Coding Sequence	(z;a,b,c,d)
-----------------	-------------

<b>ND6</b>	<b>6-INPUT NAND</b>	<b>ND6</b>
------------	---------------------	------------

**SYMBOL**



**TRUTH TABLE**

Input						Output
A	B	C	D	E	F	Z
H	H	H	H	H	H	L
X	X	X	X	X	L	H
X	X	X	X	L	X	H
X	X	X	L	X	X	H
X	X	L	X	X	X	H
X	L	X	X	X	X	H
L	X	X	X	X	X	H

**CHARACTERISTICS**

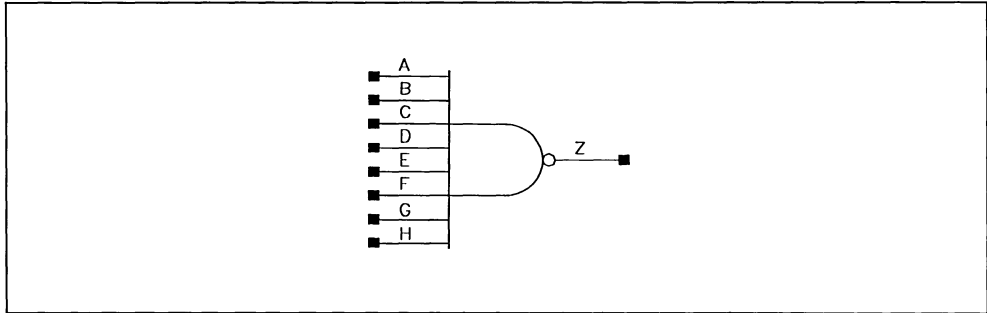
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A,B,C,D,E,F - Z	t <sub>PHL</sub>	2.51	2.70	2.89	3.08	3.86	3
	t <sub>PLH</sub>	2.17	2.42	2.67	2.93	3.93	

Input Load						Output Drive
A	B	C	D	E	F	Z
1	1	1	1	1	1	27

<b>Coding Sequence</b>	(z;a,b,c,d,e,f)
------------------------	-----------------

<b>ND8</b>	<b>8-INPUT NAND</b>	<b>ND8</b>
------------	---------------------	------------

**SYMBOL**



**TRUTH TABLE**

Input								Output
A	B	C	D	E	F	G	H	Z
H	H	H	H	H	H	H	H	L
X	X	X	X	X	X	X	L	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	L	X	X	X	X	H
X	L	X	X	X	X	X	X	H
L	X	X	X	X	X	X	X	H

**CHARACTERISTICS**

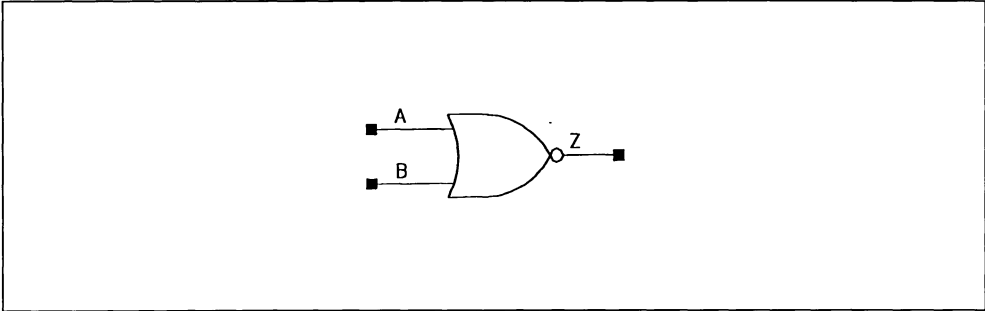
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A,B,C,D,E,F,G,H - Z	t <sub>PHL</sub>	3.27	3.39	3.51	3.63	4.11	4
	t <sub>PLH</sub>	2.41	2.53	2.66	2.79	3.30	

Input Load								Output Drive
A	B	C	D	E	F	G	H	Z
1	1	1	1	1	1	1	1	27

<b>Coding Sequence</b>	(z;a,b,c,d,e,f,g,h)
------------------------	---------------------

<b>NR2</b>	<b>2-INPUT NOR</b>	<b>NR2</b>
------------	--------------------	------------

**SYMBOL**



**TRUTH TABLE**

Input		Output
A	B	Z
L	L	H
H	X	L
X	H	L

**CHARACTERISTICS**

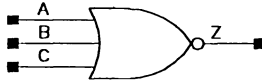
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A,B to Z	t <sub>PHL</sub>	0.7	0.9	1.2	1.4	2.3	1
	t <sub>PLH</sub>	1.2	1.6	2.0	2.4	4.1	

Input Load		Output Drive
A	B	Z
1	1	18

<b>Coding Sequence</b>	(z;a,b)
------------------------	---------

<b>NR3</b>	<b>3-INPUT NOR</b>	<b>NR3</b>
------------	--------------------	------------

**SYMBOL**



**TRUTH TABLE**

Input			Output
A	B	C	Z
L	L	L	H
H	X	X	L
X	H	X	L
X	X	H	L

**CHARACTERISTICS**

		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A,B,C to Z	t <sub>PHL</sub>	0.8	1.0	1.3	1.5	2.4	1
	t <sub>PLH</sub>	1.8	2.4	3.0	3.6	5.9	

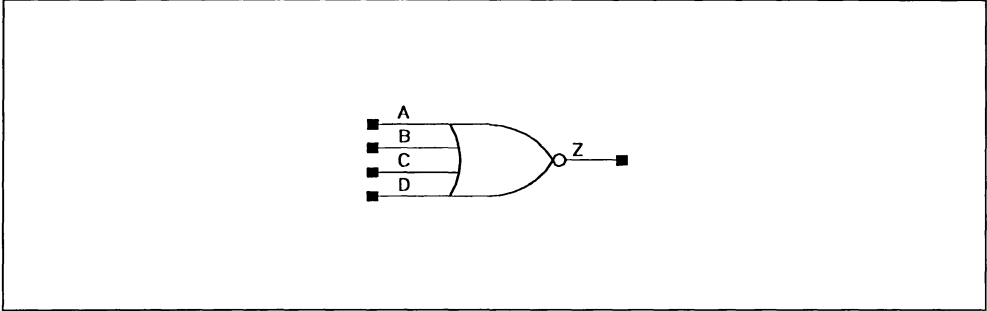
Input Load			Output Drive
A	B	C	Z
1	1	1	18

Coding Sequence	(z;a,b,c)
-----------------	-----------



<b>NR4</b>	<b>4-INPUT NOR</b>	<b>NR4</b>
------------	--------------------	------------

**SYMBOL**



**TRUTH TABLE**

Input				Output
A	B	C	D	Z
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

**CHARACTERISTICS**

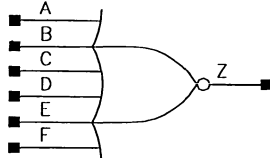
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A,B,C,D to Z	t <sub>PHL</sub>	0.95	1.16	1.38	1.59	2.45	2
	t <sub>PLH</sub>	2.77	3.54	4.30	5.06	8.12	

Input Load				Output Drive
A	B	C	D	Z
1	1	1	1	18

Coding Sequence	(z;a,b,c,d)
-----------------	-------------

<b>NR6</b>	<b>6-INPUT NOR</b>	<b>NR6</b>
------------	--------------------	------------

**SYMBOL**



**TRUTH TABLE**

Input						Output
A	B	C	D	E	F	Z
L	L	L	L	L	L	H
H	X	X	X	X	X	L
X	H	X	X	X	X	L
X	X	H	X	X	X	L
X	X	X	H	X	X	L
X	X	X	X	H	X	L
X	X	X	X	X	H	L

**CHARACTERISTICS**

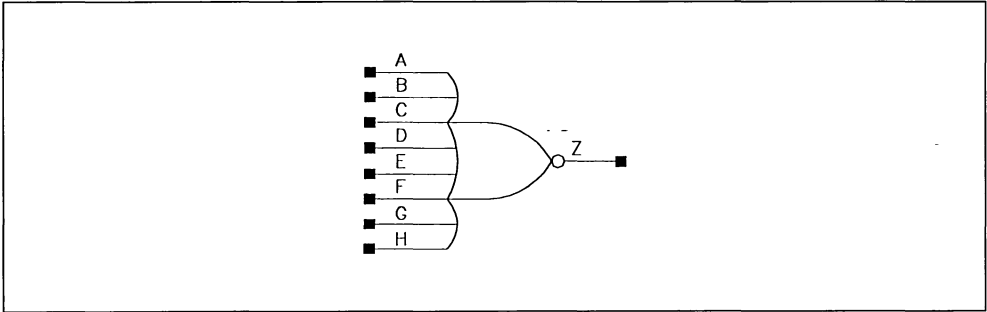
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A,B,C,D,E,F - Z	t <sub>PHL</sub>	1.93	2.11	2.29	2.46	3.18	3
	t <sub>PLH</sub>	2.93	3.19	3.44	3.70	4.72	

Input Load						Output Drive
A	B	C	D	E	F	Z
1	1	1	1	1	1	27

Coding Sequence	(z;a,b,c,d,e,f)
-----------------	-----------------

<b>NR8</b>	<b>8-INPUT NOR</b>	<b>NR8</b>
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**SYMBOL**



**TRUTH TABLE**

Input								Output
A	B	C	D	E	F	G	H	Z
L	L	L	L	L	L	L	L	H
H	X	X	X	X	X	X	X	L
X	H	X	X	X	X	X	X	L
X	X	H	X	X	X	X	X	L
X	X	X	H	X	X	X	X	L
X	X	X	X	H	X	X	X	L
X	X	X	X	X	H	X	X	L
X	X	X	X	X	X	H	X	L
X	X	X	X	X	X	X	H	L

**CHARACTERISTICS**

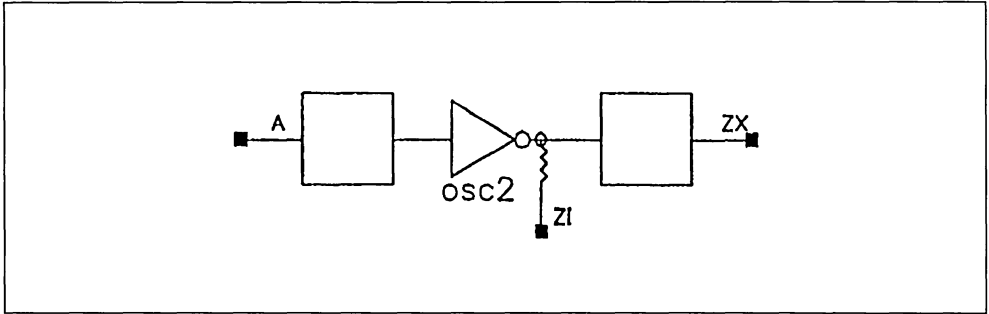
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A,B,C,D,E,F,G,H - Z	$t_{PHL}$	2.05	2.15	2.25	2.35	2.76	4
	$t_{PLH}$	4.10	4.24	4.39	4.53	5.11	

Input Load								Output Drive
A	B	C	D	E	F	G	H	Z
1	1	1	1	1	1	1	1	27

<b>Coding Sequence</b>	(z,a,b,c,d,e,f,g,h)
------------------------	---------------------

<b>OSC2</b>	<b>COMPLETE OSCILLATOR WITH XTL CONNECTIONS</b>	<b>OSC2</b>
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**SYMBOL**



**TRUTH TABLE**

Input	Output
<b>A</b>	<b>ZI-ZX</b>
H	L
L	H

**CHARACTERISTICS**

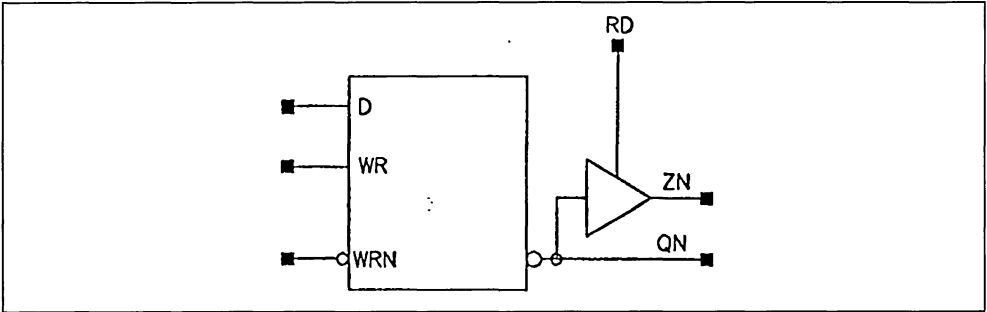
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A to ZX/ZI	t <sub>PHL</sub>	1.74	1.83	1.92	2.01	2.38	0
	t <sub>PLH</sub>	2.91	3.01	3.10	3.20	3.57	

Input Load	Output Drive	
<b>A</b>	<b>ZI</b>	<b>ZX</b>
8	5	240

Coding Sequence	(zx,zi;a)
-----------------	-----------

<b>RAM1</b>	<b>GATED D LATCH WITH ADDED TRISTATE OUTPUT</b>	<b>RAM1</b>
-------------	---	-------------

**SYMBOL**



**TRUTH TABLE**

Input				Output	
D	WR	WRN	RD	QN	ZN
L	H	L	H	H	H
H	H	L	H	L	L
X	L	H	H	QN	ZN
X	X	X	L	X	Hi-Z

**CHARACTERISTICS**

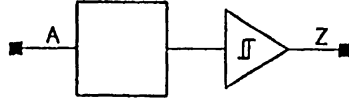
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A to Z	t <sub>PHL</sub>	1.5	1.7	1.8	1.9	2.4	5
	t <sub>PLH</sub>	1.4	1.6	1.7	1.9	2.5	

Input Load				Output Drive	
D	WR	WRN	RD	QN	ZN
1	1	1	2	18	27

<b>Coding Sequence</b>	(zn,qn;d,wr,wrn,rd)
------------------------	---------------------

<b>SCHMDT1</b>	<b>INPUT PAD WITH SCHMITT TRIGGER</b>	<b>SCHMDT1</b>
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**SYMBOL**



**TRUTH TABLE**

Input	Output
H	H
L	L

**CHARACTERISTICS**

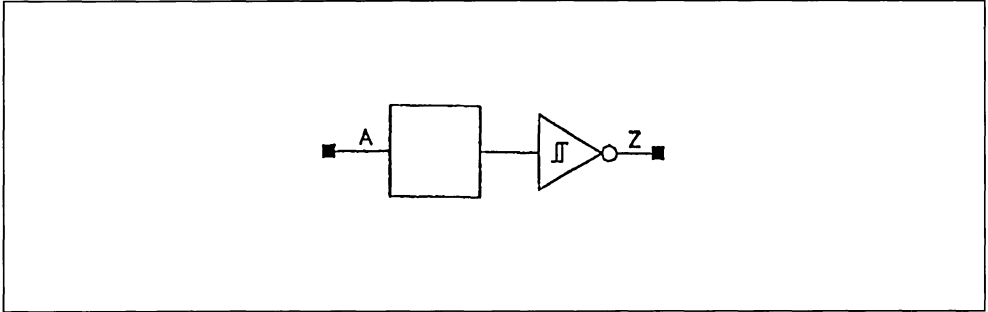
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A to Z	t <sub>PHL</sub>	1.7	1.8	1.9	2.0	2.3	0
	t <sub>PLH</sub>	2.9	3.0	3.1	3.2	3.5	

Input Load	Output Drive
A	Z
7	22

Coding Sequence	(z;a)
-----------------	-------

<b>SCHMDT2</b>	<b>INPUT PAD WITH INVERTING SCHMITT TRIGGER</b>	<b>SCHMDT2</b>
----------------	---	----------------

**SYMBOL**



**TRUTH TABLE**

Input	Output
<b>A</b>	<b>Z</b>
H	L
L	H

**CHARACTERISTICS**

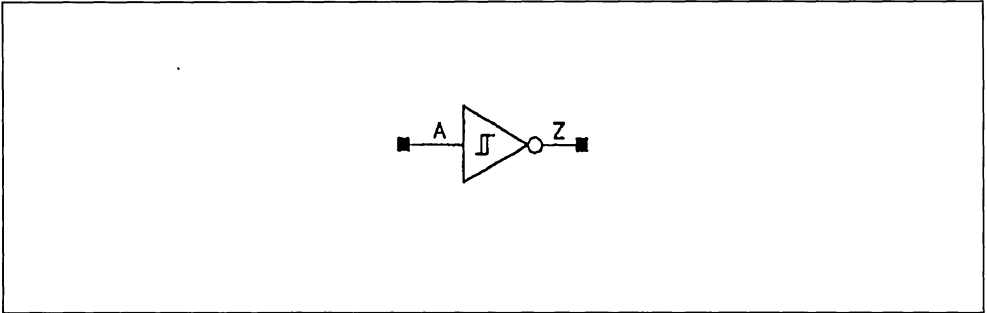
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A to Z	tPHL	4.1	4.2	4.4	4.5	5.1	0
	tPLH	2.2	2.3	2.3	2.4	2.5	

Input Load	Output Drive
<b>A</b>	<b>Z</b>
3	37

Coding Sequence	(z;a)
-----------------	-------

<b>ST</b>	<b>INVERTING SCHMITT TRIGGER FOR INTRACHIP WAVE SHAPING</b>	<b>ST</b>
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**SYMBOL**



**TRUTH TABLE**

Input	Output
<b>A</b>	<b>Z</b>
H	L
L	H

**CHARACTERISTICS**

		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A to Z	t <sub>PHL</sub>	1.39	1.64	1.89	2.15	3.15	2
	t <sub>PLH</sub>	1.47	1.84	2.22	2.59	4.09	

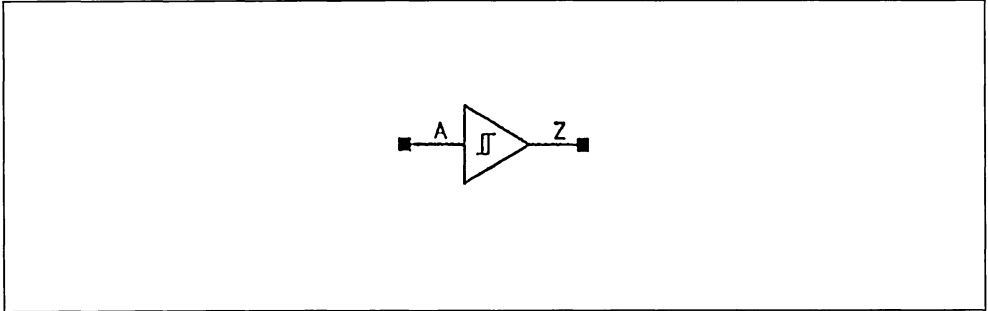
Input Load	Output Drive
<b>A</b>	<b>Z</b>
3	22

Coding Sequence	(z;a)
-----------------	-------



<b>ST1</b>	<b>NON-INVERTING SCHMITT TRIGGER FOR BIDIRECTIONAL USE</b>	<b>ST1</b>
------------	--	------------

**SYMBOL**



**TRUTH TABLE**

Input	Output
A	Z
H	H
L	L

**CHARACTERISTICS**

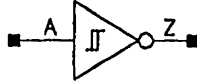
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A to Z	$t_{PHL}$	2.1	2.3	2.4	2.6	3.3	3
	$t_{PLH}$	2.0	2.3	2.5	2.7	3.6	

Input Load	Output Drive
A	Z
3	22

Coding Sequence	(z;a)
-----------------	-------

<b>ST2</b>	<b>INVERTING SCHMITT TRIGGER FOR BIDIRECTIONAL USE</b>	<b>ST2</b>
------------	--	------------

**SYMBOL**



**TRUTH TABLE**

Input	Output
A	Z
H	L
L	H

**CHARACTERISTICS**

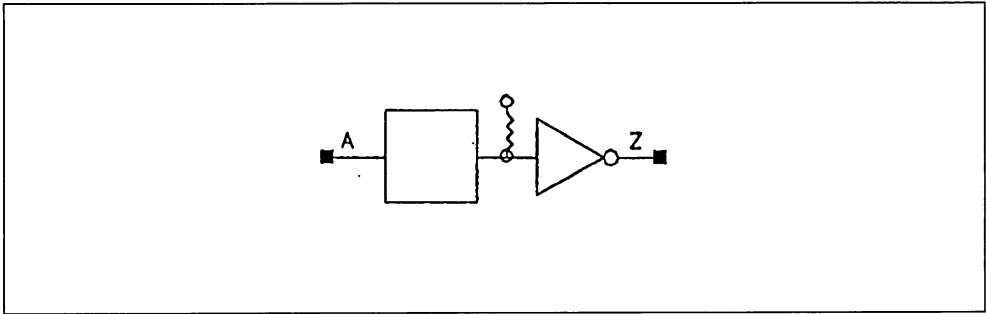
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A to Z	t <sub>PHL</sub>	1.4	1.6	1.9	2.2	3.2	2
	t <sub>PLH</sub>	1.5	1.8	2.2	2.6	4.1	

Input Load	Output Drive
A	Z
3	22

Coding Sequence	(z;a)
-----------------	-------

<b>TLCHN</b>	<b>INVERTING INPUT PAD WITH BUFFER FOR TTL INPUT</b>	<b>TLCHN</b>
--------------	--	--------------

**SYMBOL**



**TRUTH TABLE**

Input	Output
<b>A</b>	<b>Z</b>
H	L
L	H

**CHARACTERISTICS**

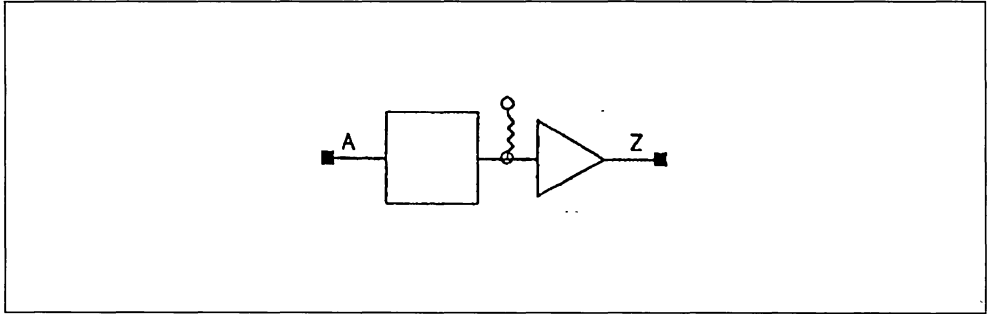
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A to Z	$t_{PHL}$	1.5	1.6	1.7	1.8	2.1	0
	$t_{PLH}$	2.5	2.7	3.0	3.3	4.3	

Input Load	Output Drive
<b>A</b>	<b>Z</b>
13	36

Coding Sequence	(z:a)
-----------------	-------

<b>TLCHT</b>	<b>INPUT PAD WITH BUFFER FOR TTL INPUT</b>	<b>TLCHT</b>
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**SYMBOL**



**TRUTH TABLE**

Input	Output
<b>A</b>	<b>Z</b>
H	H
L	L

**CHARACTERISTICS**

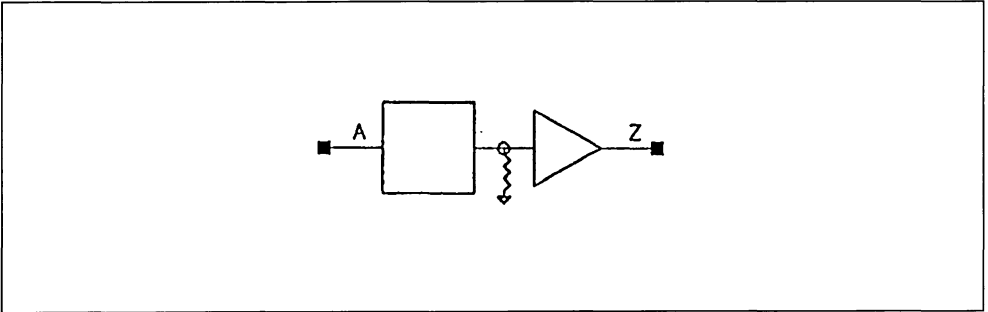
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A to Z	$t_{PHL}$	3.1	3.2	3.3	3.3	3.6	1
	$t_{PLH}$	3.0	3.0	3.1	3.1	3.3	

Input Load	Output Drive
<b>A</b>	<b>Z</b>
13	36

Coding Sequence	(z;a)
-----------------	-------

<b>TLCHTD</b>	<b>INPUT PAD WITH BUFFER &amp; PULL DOWN FOR TTL INPUT</b>	<b>TLCHTD</b>
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**SYMBOL**



**TRUTH TABLE**

Input	Output
A	Z
H	H
L	L

**CHARACTERISTICS**

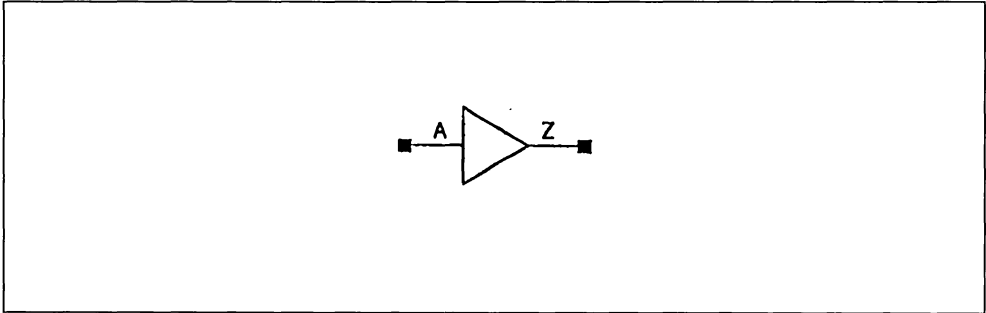
		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A to Z	$t_{PHL}$	3.0	3.1	3.2	3.2	3.5	0
	$t_{PLH}$	3.0	3.0	3.1	3.1	3.3	

Input Load	Output Drive
A	Z
3.5	36

Coding Sequence	(z;a)
-----------------	-------

<b>TLCHTI</b>	<b>BUFFER FOR BIDIRECTIONAL TTL INPUTS</b>	<b>TLCHTI</b>
---------------	--	---------------

**SYMBOL**



**TRUTH TABLE**

Input	Output
A	Z
L	L
H	H

**CHARACTERISTICS**

		Propagation Delay (ns)					Cell Usage
		FO 1	FO 2	FO 3	FO 4	FO 8	
A to Z	$t_{PHL}$	1.21	1.40	1.58	1.77	2.51	2
	$t_{PLH}$	1.92	2.16	2.41	2.65	3.62	

Input Load	Output Drive
A	Z
2	22

Coding Sequence	(z;a)
-----------------	-------



# **APPENDIX**





OUTPUT BUFFER SUMMARY TABLE

BUFFER NAME	CURRENT (mA)	I/O SLOTS	DT*
B14	1	1	0.25
B18	2	1	0.50
B1	4	1	1
B1OD	4	1	1
B1I	INTERNAL	1	1
B2	8	1	2
B2OD	8	1	2
OSC2	8	1	2
B3	16	2	4
B3OD	16	2	4
BTS14	1	1	0.25
BTS18	2	1	0.50
BTS1	4	1	1
BTS2	8	1	2
BTS3	16	2	4
BTS78	2	1	0.25
BTS7	4	1	1
BTS7L	4	1	1
BTS7LO	4	1	1
BTS7OD	4	1	1
BTS7U	4	1	1
BTS8	8	1	2
BTS8D	8	1	2
BTS8OD	8	1	2
BTS8U	8	1	2
BTS9	16	2	4

\* DT is a measurement of the drive capability of the I/Os using B1 as a standard drive capability equal to 1.

## NOTES



## NOTES



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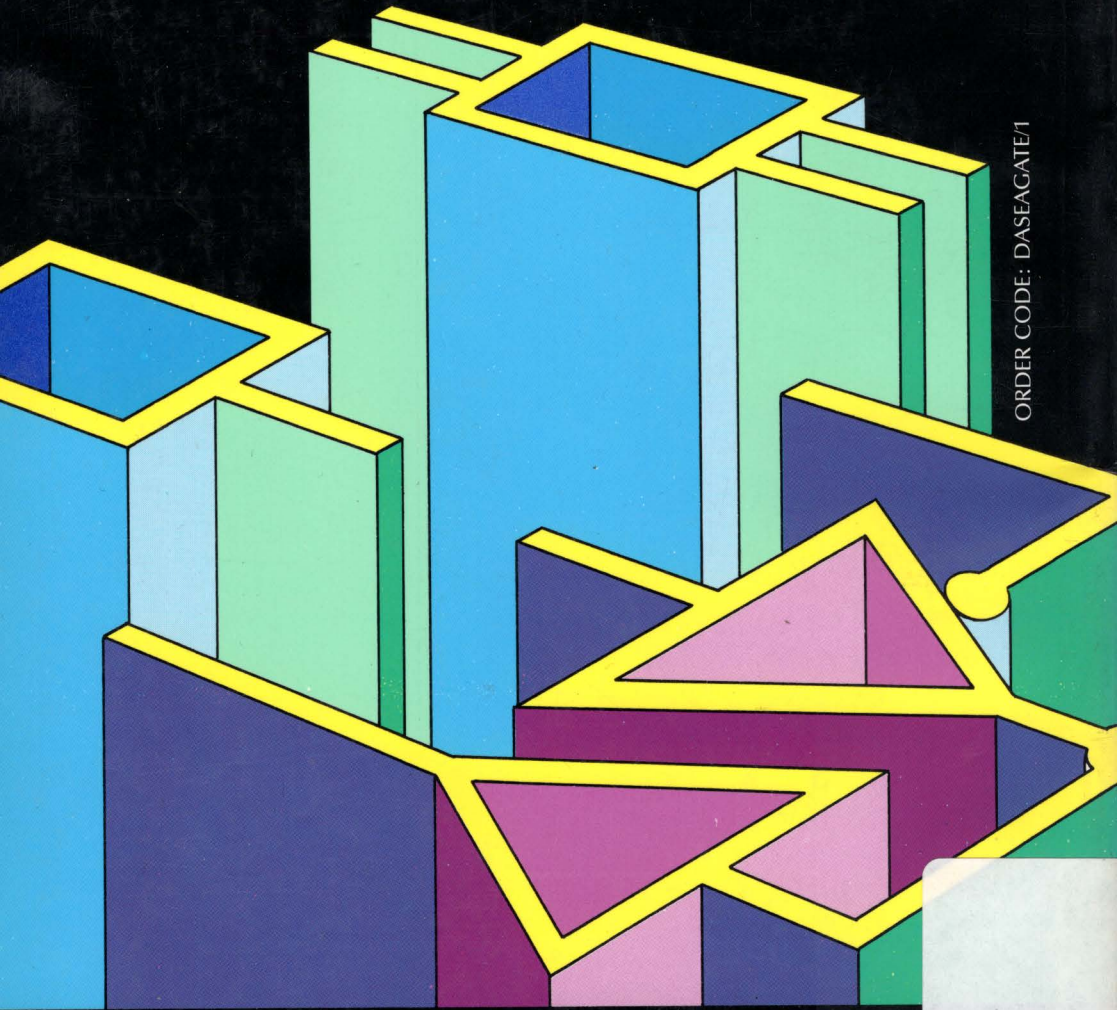


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