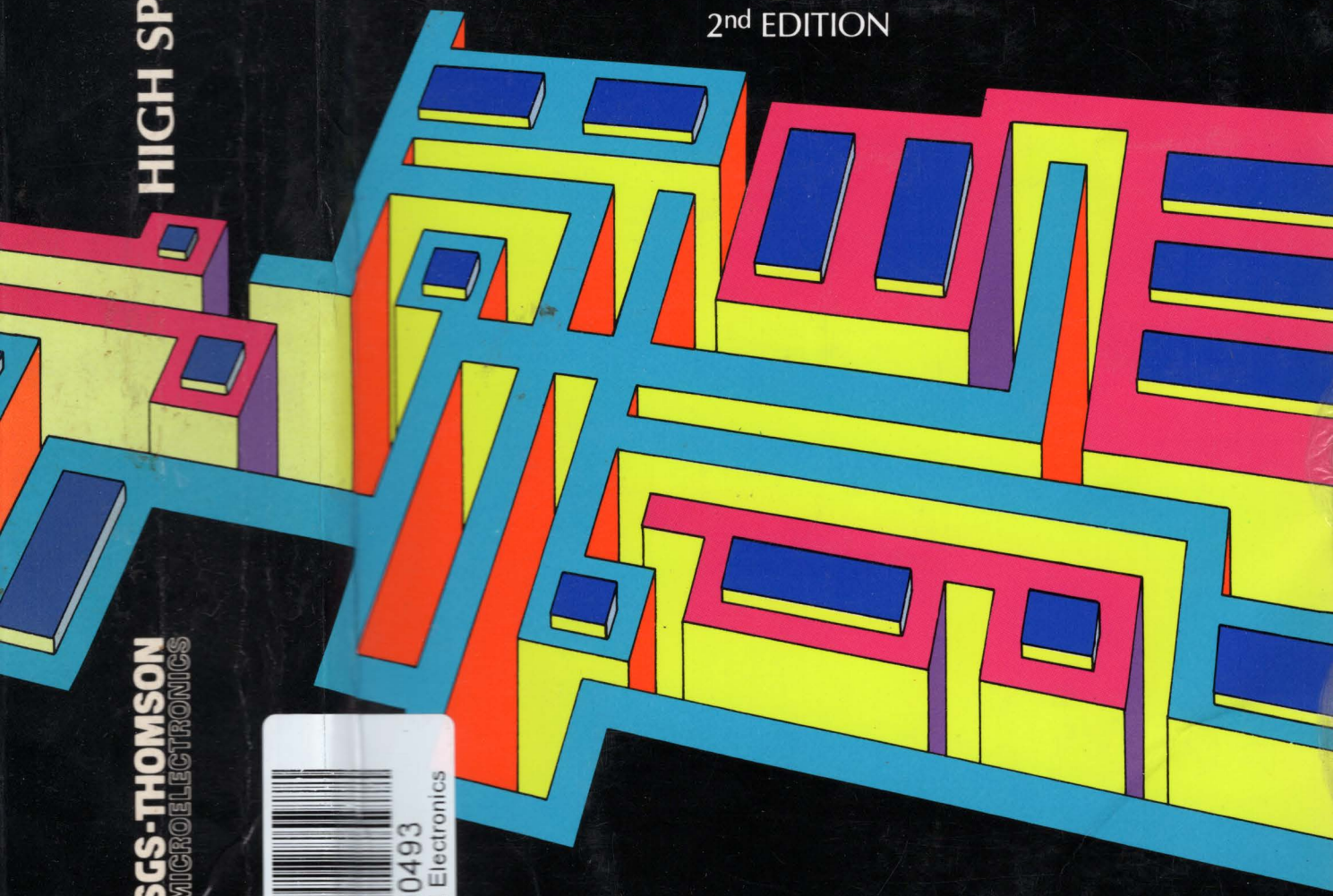
HIGH SPEED CMOS

DATABOOK

2nd EDITION



SGS-THOMSON MICROELECTRONICS

000493
RYSTON Electronics

HIGH SPEED CMOS

SGS-THOMSON MICROELECTRONICS

4664

HIGH SPEED CMOS

DATABOOK

2nd EDITION

MARCH 1994

USE IN LIFE SUPPORT DEVICES OR SYSTEMS MUST BE EXPRESSLY AUTHORIZED.

SGS-THOMSON PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

TABLE OF CONTENTS

INTRODUCTION Page 4

ALPHANUMERICAL INDEX 5

SELECTION GUIDE 11

GENERAL AND APPLICATION INFORMATION 51

IEC LOGIC SYMBOL EXPLANATION 67

TYPE NUMBER DESCRIPTION 73

RELIABILITY REPORT 75

DATASHEETS 93

PACKAGES 1221

INTRODUCTION

SGS-THOMSON has been producing high speed CMOS devices since 1983. The product has constantly evolved over the years and changes and improvements are reflected in the products covered in this databook.

The re-designed ("R") line offers improvements in terms of AC parameters, ESD and latch-up immunity. Innovative types have been introduced including devices with integrated pull-up resistors, high voltage devices, transmission gates supplied from 12V, monostable multivibrators with a range of timing constants, and a high current capability decoder latch. The product range has expanded particularly in the field of TTL compatible devices (the HCT series).

High speed CMOS offers designers logic integrated circuits with power consumption lower than other logic integrated circuits, and high switching speeds equal to that of LSTTL. These devices also have a better noise margin and an improved voltage and temperature operating range. In addition, they are pin-to-pin compatible with either LSTTL or the conventional CMOS B series. This reduces the need for logical re-design when they are adopted as replacements in designs using LSTTL or CMOS B series devices.

In response to the industry demand for surface mounting technologies, all devices are now offered with a surface mounting package option.

Finally, if the exact device cannot be found for a particular application, the technology offered by SGS-THOMSON allows custom devices to be designed to the exact requirements of the customer.

The comprehensive data provided in this databook makes it easy to evaluate the performance of the product within any design.

ALPHANUMERICAL INDEX

Type Number	Function	Package DIP	Page Number
HC00	Quad 2-Input NAND Gate	14	95
HCT00	Quad 2-Input NAND Gate	14	99
HC02	Quad 2-Input NOR Gate	14	103
HCT02	Quad 2-Input NOR Gate	14	107
HC03	Quad 2-Input NAND (open drain)	14	111
HC04	Hex Inverter	14	115
HCT04	Hex Inverter	14	119
HCU04	Hex Inverter	14	123
HC05	Hex Inverter	14	127
HC07	Hex Buffer	14	131
HC08	Quad 2-Input AND Gate	14	135
HCT08	Quad 2-Input AND Gate	14	139
HC09	Quad 2-Input AND Gate (open drain)	14	143
HC10	Triple 3-Input NAND Gate	14	147
HCT10	Triple 3-Input NAND Gate	14	151
HC11	Triple 3-Input AND Gate	14	155
HC14	Hex Schmitt Inverter	14	159
HCT14	Hex Schmitt Inverter	14	163
HC20	Dual 4-Input NAND Gate	14	167
HC21	Dual 4-Input AND Gate	14	171
HC27	Triple 3-Input NOR Gate	14	175
HCT27	Triple 3-Input NOR Gate	14	179
HC30	8-Input NAND Gate	14	183
HCT30	8-Input NAND Gate	14	187
HC32	Quad 2-Input OR Gate	14	191
HCT32	Quad 2-Input OR Gate	14	195
HC42	BCD to Decimal Decoder	16	199
HC51	Dual 2-Wide 2-Input AND/OR Inverter Gate	14	205
HC73	Dual J-K Flip-Flop with Clear	14	209
HC74	Dual D-Type Flip-Flop with Preset and Clear	14	215
HCT74	Dual D-Type Flip-Flop with Preset and Clear	14	221
HC75	4-Bit D-Type Latch	16	227
HCT75	4-Bit D-Type Latch	16	231
HC76	Dual J-K Flip-Flop with Preset and Clear	16	235
HC77	4-Bit D-Type Latch	14	241
HC85	4-Bit Magnitude Comparator	16	247
HC86	Quad exclusive OR Gate	14	253
HCT86	Quad exclusive OR Gate	14	257
HC107	Dual J-K Flip-Flop with Clear	14	261
HC109	Dual J-K Flip-Flop with Preset and Clear	16	267
HC112	Dual J-K Flip-Flop with Preset and Clear	16	273

ALPHANUMERICAL INDEX

Type Number	Function	Package DIP	Page Number
HC113	Dual J-K Flip-Flop with Preset	14	279
HC123	Dual Retrigg. Monostable Multivibrator with Clear	16	285
HC123A	Dual Retrigg. Monostable Multivibrator with Clear	16	285
HC125	Quad Bus Buffer (3-State)	14	295
HCT125	Quad Bus Buffer (3-State)	14	301
HC126	Quad Bus Buffer (3-State)	14	295
HCT126	Quad Bus Buffer (3-State)	14	301
HC131	3 to 8 Line Decoder Latch	16	307
HC132	Quad 2-Input Schmitt NAND Gate	14	325
HC133	13 Input NAND Gate	16	319
HC137	3 to 8 Line Decoder Latch (Inv.)	16	325
HCT137	3 to 8 Line Decoder Latch (Inv.)	16	331
HC138	3 to 8 Line Decoder (Inv.)	16	339
HCT138	3 to 8 Line Decoder (Inv.)	16	345
HC139	Dual 2 to 4 Line Decoder/Demultiplexer	16	351
HCT139	Dual 2 to 4 Line Decoder/Demultiplexer	16	355
HC147	10 to 4 Line Priority Encoder	16	359
HC148	8 to 3 Line Priority Encoder	16	365
HC151	8-Channel Multiplexer	16	371
HC153	Dual 4- Channel Multiplexer	16	377
HC154	4 to 16 Decoder/Demultiplexer	24	385
HC155	Dual 2 to 4 Line Decoder/ 3 to 8 Line Decoder	16	391
HC157	Quad 2-Channel Multiplexer	16	397
HCT157	Quad 2-Channel Multiplexer	16	403
HC158	Quad 2-Channel Multiplexer (Inv.)	16	397
HCT158	Quad 2-Channel Multiplexer (Inv.)	16	403
HC160	Synchronous Decade Counter with Async. Clear	16	409
HCT160	Synchronous Decade Counter with Async. Clear	16	421
HC161	Synchronous Binary Counter with Async. Clear	16	409
HCT161	Synchronous Binary Counter with Async. Clear	16	421
HC162	Synchronous Decade Counter with Sync Clear	16	409
HCT162	Synchronous Decade Counter with Sync Clear	16	421
HC163	Synchronous Binary Counter with Sync Clear	16	409
HCT163	Synchronous Binary Counter with Sync Clear	16	421
HC164	8 Bit SIPO Shift Register	14	433
HCT164	8 Bit SIPO Shift Register	14	441
HC165	8 Bit PISO Shift Register	16	449
HCT165	8 Bit PISO Shift Register	16	457
HC166	8 Bit PISO Shift Register	16	465
HC173	Quad D-Type Register (3-State)	16	473
HC174	Hex D-Type Flip-Flop with Clear	16	481

ALPHANUMERICAL INDEX

Type Number	Function	Package DIP	Page Number
HCT174	Hex D-Type Flip-Flop with Clear	16	487
HC175	Quad D-Type Flip-Flop with Clear	16	493
HC181	Arithmetic Logic Unit Function Generator	24	499
HC182	Function Look Ahead Carry Generator	16	509
HC190	BCD Synchronous Up/Down Counter	16	517
HC191	4 Bit Synchronous Binary Up/Down Counter	16	517
HC192	Synchronous Up/Down Decade Counter	16	527
HC193	Synchronous Up/Down Binary Counter	16	527
HC194	4 Bit PIPO Shift Register	16	537
HC195	4 Bit PIPO Shift Register	16	545
HC221	Dual Monostable Multivibrator	16	553
HC221A	Dual Monostable Multivibrator	16	553
HC237	3 to 8 Line decoder Latch	16	563
HC238	3 to 8 Line Decoder	16	569
HC240	Octal Bus Buffer (3-State/Inv.)	20	575
HC240HV	Octal Bus Buffer (3-State/Inv.)	20	583
HCT240	Octal Bus Buffer (3-State/Inv.)	20	589
HCT240PU	Octal Bus Buffer (3-State/Inv.)	20	597
HC241	Octal Bus Buffer (3-State)	20	575
HC241HV	Octal Bus Buffer (3-State)	20	583
HCT241	Octal Bus Buffer (3-State)	20	589
HCT241PU	Octal Bus Buffer (3-State)	20	597
HC242	Quad Bus Transceiver (3-State/Inv.)	14	603
HC243	Quad Bus Transceiver (3-State)	14	603
HC244	Octal Buffer (3-State)	20	575
HCT244	Octal Buffer (3-State)	20	589
HCT244PU	Octal Buffer (3-State)	20	597
HC245	Octal Bus Trasceiver (3-State)	20	609
HCT245	Octal Bus Trasceiver (3-State)	20	615
HC251	8-Channel Multiplexer (3-State)	16	621
HC253	Dual 4-Channel Multiplexer (3-State)	16	377
HC257	Quad 2-Channel Multiplexer	16	627
HCT257	Quad 2-Channel Multiplexer	16	635
HC258	Quad 2-Channel Multiplexer (3-State/Inv.)	16	627
HCT258	Quad 2-Channel Multiplexer (3-State/Inv.)	16	635
HC259	8 Bit Addressable Latch	16	643
HC266	Quad exclusive NOR Gate	14	651
HC273	Octal D-Type Flip-Flop with Clear	20	657
HCT273	Octal D-Type Flip-Flop with Clear	20	663
HC279	Quad S-R Latch	16	669
HC280	9 Bit Parity Generator	14	675

ALPHANUMERICAL INDEX

Type Number	Function	Package DIP	Page Number
HC283	4 Bit Binary Full Adder	16	681
HC292	Programmable Divider/Timer	16	687
HC294	Programmable Divider/Timer	16	687
HC298	Quad 2-Channel Multiplexer Register	16	697
HC299	8 Bit PIPO Shift Register (3-State)	20	703
HC323	8 Bit PIPO Shift Register (3-State)	20	703
HC352	Dual 4-Channel Multiplexer	16	713
HC353	Dual 3-Channel Multoplexer	16	713
HC354	8 Channel Multiplexer/Register (3-State)	20	719
HC356	8 Channel Multiplexer/Register (3-State)	20	727
HC365	Hex Bus Buffer	16	735
HC366	Hex Bus Buffer (3-State/Inv.)	16	735
HC367	Hex Bus Buffer (3-State/Inv.)	16	741
HCT367	Hex Bus Buffer (3-State/Inv.)	16	747
HC368	Hex Bus Buffer (3-State/Inv.)	16	741
HCT368	Hex Bus Buffer (3-State/Inv.)	16	747
HC373	Octal D-Type Latch (3-State/Inv.)	20	753
HCT373	Octal D-Type Latch (3-State/Inv.)	20	761
HC374	Octal D-Type Flip-Flop (3-State)	20	769
HCT374	Octal D-Type Flip-Flop (3-State)	20	777
HC375	Quad D-Type Latch	16	785
HC377	Octal D-Type Flip-Flop	20	791
HC386	Quad Exclusive OR Gate	14	797
HC390	Dual Decade Counter	16	801
HC393	Dual Binary Counter	14	809
HCT393	Dual Binary Counter	14	817
HC423	Dual Monostable Multivibrator with Clear	16	825
HC423A	Dual Monostable Multivibrator with Clear	16	825
HC533	Octal D-Type Latch (3-State/Inv.)	20	753
HCT533	Octal D-Type Latch (3-State/Inv.)	20	761
HC534	Octal D-Type Flip-Flop (3-State/Inv.)	20	769
HCT534	Octal D-Type Flip-Flop (3-State/Inv.)	20	777
HC540	Octal Bus Buffer (3-State/Inv.)	20	835
HCT540	Octal Bus Buffer (3-State/Inv.)	20	843
HC541	Octal Bus Buffer (3-State)	20	835
HCT541	Octal Bus Buffer (3-State)	20	843
HC563	Octal D-Type Latch (3-State/Inv.)	20	851
HCT563	Octal D-Type Latch (3-State/Inv.)	20	859
HC564	Octal D-Type Flip-Flop (3-State/Inv.)	20	867
HCT564	Octal D-Type Flip-Flop (3-State/Inv.)	20	875
HC573	Octal D-Type Latch (3-State)	20	851

ALPHANUMERICAL INDEX

Type Number	Function	Package DIP	Page Number
HCT573	Octal D-Latch (3-State)	20	859
HC574	Octal D-Type Flip-Flop (3-State)	20	867
HCT574	Octal D-Type Flip-Flop (3-State)	20	875
HC590	8 Bit Binary Counter Register (3-State)	16	883
HC592	8 Bit Binary Counter Register	16	893
HC593	8 Bit Binary Counter with input Register	20	901
HC595	8 Bit Shift Register Output Latch (3-State)	16	909
HC597	8 Bit Latch Shift Register	16	917
HC620	Octal Bus Transceiver (3-State/Inv.)	20	925
HC623	Octal Bus Transceiver (3-State)	20	925
HC640	Octal Bus Transceiver (3-State/Inv.)	20	609
HCT640	Octal Bus Transceiver (3-State/Inv.)	20	615
HC643	Octal Bus Transceiver (3-State)	20	609
HCT643	Octal Bus Transceiver (3-State)	20	615
HC646	Octal Bus Transceiver Register (3-State)	24	931
HCT646	Octal Bus Transceiver Register (3-State)	24	941
HC648	Octal Bus Transceiver Register (3-State/Inv.)	24	931
HCT648	Octal Bus Transceiver Register (3-State/Inv.)	24	941
HC651	Octal Bus Transceiver Register (3-State/Inv.)	24	951
HCT651	Octal Bus Transceiver Register (3-State/Inv.)	24	961
HC652	Octal Bus Transceiver Register	24	951
HCT652	Octal Bus Transceiver Register	24	961
HC670	4 Word x 4 Bit Register File (3-State)	16	971
HC688	8 Bit Equality Comparator	20	979
HCT688	8 Bit Equality Comparator	20	985
HC690	Decade Counter Register (3-State)	20	991
HC691	4 Bit Binary Counter Register (3-State)	20	991
HC692	Decade Counter Register (3-State)	20	991
HC693	4 Bit Binary Counter Register (3-State)	20	991
HC696	U/D Decade Counter Register (3-State)	20	1009
HC697	U/D 4-Bit Binary Counter Register (3-State)	20	1009
HC698	U/D decade Counter Register (3-State)	20	1009
HC699	U/D 4-Bit Binary Counter/Register (3-State)	20	1009
HC4002	Dual 4-Input NOR Gate	14	1027
HC4016	Quad Bilateral Switch	14	1031
HC4017	Decade Counter/Divider	16	1037
HC4020	14-Stage Binary Counter	16	1045
HC4022	Octal Counter/Divider	16	1053
HC4024	7-Stage Binary Counter	14	1061
HC4028	BCD to Decimal Decoder	16	1067
HC4040	12-Stage Binary Counter	16	1045

ALPHANUMERICAL INDEX

Type Number	Function	Package DIP	Page Number
HC4049	Hex Buffer/Converter (Inv.)	16	1073
HC4050	Hex Buffer/Converter	16	1073
HC4051	Analog Multiplexer	16	1079
HC4052	Analog Multiplexer	16	1079
HC4053	Analog Multiplexer	16	1089
HC4060	14-Stage Binary Counter/Oscillator	16	1089
HC4066	Quad Bilateral Switch	14	1097
HC4072	Dual 4 Input OR Gate	14	1103
HC4075	Triple 3-Input OR Gate	14	1107
HC4078	8-Input NOR/OR Gate	14	1111
HC4094	8-Bit SIPO Shift Register Latch (3-State)	16	1115
HC4316	Quad Bilateral Switch	14	1123
HC4351	Analog Multiplexer	20	1131
HC4352	Analog Multiplexer	20	1131
HC4353	Analog Multiplexer	20	1131
HC4511	BCD to 7-Segment L/D/D (LED)	16	1143
HC4514	4 to 16 Line Decoder Latch	24	1151
HC4515	4 to 16 Line Decoder Latch (Inv.)	24	1151
HC4518	Dual Decade Counter	16	1159
HC4520	Dual 4 Bit Binary Counter	16	1159
HC4538	Dual Monostable Multivibrator	16	1167
HC4543	BCD to 7-Segment L/D/D (LCD)	16	1177
HCT7007	Hex Buffer	14	1185
HC7240	Octal Bus Buffer	20	1189
HC7241	Octal Bus Buffer	20	1189
HC7244	Octal Bus Buffer	20	1189
HC7245	Bidirectional Octal Bus Buffer	20	1197
HCT7259	Decoder-Latch (open drain, 100 mA output)	16	1203
HC7266	Quad Exclusive NOR Gate	14	651
HC7292	Programmable Divider/Timer	16	687
HC7294	Programmable Divider/Timer	16	687
HC7640	Bidirectional Octal Bus Buffer	20	1197
HC7643	Bidirectional Octal Bus Buffer	20	1197
HC7645	Bidirectional Octal Bus Buffer	20	1197
HC40102	Dual BCD Programmable Down Counter	16	1211
HC40103	8 Bit Binary Programmable Down Counter	16	1211

SELECTION GUIDE

FUNCTION			STANDARD CODE
GATE BUFFER	NAND		HC00, HCT00, HC03, HC10, HCT10, HC20, HC30, HC133, HCT30
	NOR		HC02, HCT02, HC27, HCT27, HC4002, HC4078
	AND		HC08, HCT08, HC09, HC11, HC21
	OR		HC32, HCT32, HC4072, HC4075
	EX NOR		HC266, HC7266
	EX OR		HC86, HCT86, HC386
	INVERTER		HC04, HCU04, HCT04, HC05, HCT14, HC14
	BUFFER		HC07, HC4049, HC4050, HCT7007
		3-STATE	HC125, HCT125, HC126, HCT126, HC240, HC240HV, HCT240, HCT240PU, HC241, HC241HV, HCT241, HCT241PU, HC244, HCT244, HCT244PU, HC365, HC366, HC367, HCT367, HC368, HCT368, HC540, HCT540, HC541, HCT541, HC7240, HC7241, HC7244
		BIDIRECTIONAL	HC242, HC243, HC245, HCT245, HC620, HC623, HC640, HCT640, HC643, HCT643, HC7245, HC7640, HC7643, HC7645
	MULTIFUCTION		HC51, HC4078
	SCHMITT TRIGGER		HC14, HC132
FLIP-FLOP	J-K FLIP-FLOP		HC73, HC76, HC107, HC109, HC112, HC113
	D FLIP-FLOP		HC74, HCT74, HC174, HCT174, HC175, HC273, HCT273, HC377
		3-STATE	HC374, HCT374, HC534, HCT534, HC564, HCT564, HC574, HCT574, HC646, HCT646, HC648, HCT648, HC651, HCT651, HC652, HCT652
LATCH			HC75, HCT75, HC77, HC259, HC279, HC375, HCT7259
		3-STATE	HC373, HCT373, HC533, HCT533, HC563, HCT563, HC573, HCT573
MULTIVIBRATOR			HC123, HC123A, HC221, HC221A, HC423, HC423A, HC4538
DECODER			HC42, HC131, HC137, HCT137, HC138, HCT138, HC139, HCT139, HC154, HC155, HC237, HC238, HC4028, HC4514, HC4515
	7-SEGMENT		HC4511, HC4543
ENCODER			HC147, HC148
REGISTER			HC164, HCT164, HC165, HCT165, HC166, HC173, HC194, HC195, HC299, HC323, HC595, HC597, HC670, HC4094
COUNTER		BINARY	HC161, HCT161, HC163, HCT163, HC191, HC193, HC393, HCT393, HC590, HC592, HC593, HC691, HC693, HC697, HC699, HC4520
		DECADE	HC160, HC162, HC190, HC192, HC390, HC690, HC692, HC696, HC698, HC4518, HCT160, HCT162
		DIVIDER	HC292, HC294, HC4017, HC4020, HC4022, HC4024, HC4040, HC4060, HC40102, HC40103, HC7292, HC7294
MULTIPLEXER		ANALOG	HC4016, HC4066, HC4051, HC4052, HC4053, HC4316, HC4351, HC4352, HC4353
		DIGITAL	HC151, HC153, HC157, HCT157, HC158, HCT158, HC251, HC253, HC257, HCT257, HC258, HCT258, HC298, HC352, HC353, HC354, HC356
OTHERS	ADDER		HC283
	COMPARATOR		HC85, HC688, HCT688
	ALU		HC181, HC182
	PARITY TREE		HC280

GATE/BUFFERS

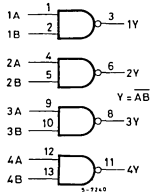
Type Number M54/74	Function	Functional Equivalent LSTTL 54/74	Functional Equivalent CMOS 4000B	Suggested Alternative LS 54/74 4000B	Package DIP
HC00	Quad 2-Input NAND Gate	LS00		4011B	14
HCT00	Quad 2-Input NAND Gate	LS00		4011B	14
HC02	Quad 2-Input NOR Gate	LS02		4001B	14
HCT02	Quad 2-Input NOR Gate	LS02		4001B	14
HC03	Quad 2-Input NAND (Open Drain)	LS03			14
HC04	Hex Inverter	LS04		4069UB	14
HCT04	Hex Inverter	LS04		4069UB	14
HCU04	Hex Inverter (Single Stage)	LS04		4069UB	14
HC05	Hex Inverter (Open Drain)				14
HC07	Hex Buffer (Open Drain)				14
HCT7007	Hex Buffer	LS07			14
HC08	Quad 2-Input AND Gate	LS08		4081B	14
HCT08	Quad 2-Input AND Gate	LS08		4081B	14
HC09	Quad 2-Input AND Gate (Open Drain)				14
HC10	Triple 3-Input NAND Gate	LS10		4023B	14
HCT10	Triple 3-Input NAND Gate	LS10		4023B	14
HC11	Triple 3-Input AND Gate	LS11		4073B	14
HC14	Hex Schmitt Inverter	LS14		40106B	14
HCT14	Hex Schmitt Inverter	LS14		40106B	14
HC20	Dual 4-Input NAND Gate	LS20		4012B	14
HC21	Dual 4-Input AND Gate	LS21		4082B	14
HC27	Triple 3-Input NOR Gate	LS27		4025B	14
HCT27	Triple 3-Input NOR Gate	LS27		4025B	14
HC30	8-Input NAND Gate	LS30		4068B	14
HCT30	8-Input NAND Gate	LS30		4068B	14
HC32	Quad 2-Input OR Gate	LS32		4071B	14
HCT32	Quad 2-Input OR Gate	LS32		4071B	14
HC51	Dual 2W-2I AND/OR Invert Gate	LS51		4085B	14
HC86	Quad Exclusive OR Gate	LS86		4030B	14
HCT86	Quad Exclusive OR Gate	LS86		4030B	14
HC125	Quad Bus Buffer (3-State)	LS125			14
HCT125	Quad Bus Buffer (3-State)	LS125			14
HC126	Quad Bus Buffer (3-State)	LS126			14
HCT126	Quad Bus Buffer (3-State)	LS126			14
HC132	Quad 2-Input Schmitt NAND	LS132		4093B	14
HC133	13 Input NAND Gate	LS133			16
HC240	Octal Bus Buffer (3-State/Inv.)	LS240			20
HC240HV	Octal Bus Buffer (3-State/Inv.)	LS240			20
HCT240	Octal Bus Buffer (3-State/Inv.)	LS240			20
HCT240PU	Octal Bus Buffer (3-State/Inv.)	LS240			20
HC241	Octal Bus Buffer (3-State)	LS241			20
HC241HV	Octal Bus Buffer (3-State)	LS241			20
HCT241	Octal Bus Buffer (3-State)	LS241			20
HCT241PU	Octal Bus Buffer (3-State)	LS241			20
HC242	Quad Bus Transceiver (3-State/Inv.)	LS242			14

GATE/BUFFERS (Cont'd)

Type Number M54/74	Function	Functional Equivalent LSTTL 54/74	Functional Equivalent CMOS 4000B	Suggested Alternative LS 54/74 4000B	Package DIP
HC243	Quad Bus Transceiver (3-State)	LS243			14
HC244	Octal Bus Buffer (3-State)	LS244			20
HCT244	Octal Bus Buffer (3-State)	LS244			20
HCT244PU	Octal Bus Buffer (3-State)	LS244			20
HC245	Octal Bus Transceiver (3-State)	LS245			20
HCT245	Octal Bus Transceiver (3-State)	LS245			20
HC266	Open drain outputs	LS266			14
HC7266	Quad Exclusive NOR Gate	LS266		4077B	14
HC365	Hex Bus Buffer (3-State)	LS365			16
HC366	Hex Bus Buffer (3-State/Inv.)	LS366			16
HC367	Hex Bus Buffer (3-State)	LS367		4503B	16
HCT367	Hex Bus Buffer (3-State)	LS367		4503B	16
HC368	Hex Bus Buffer (3-State/Inv.)	LS368			16
HCT368	Hex Bus Buffer (3-State/Inv.)	LS368			16
HC386	Quad Exclusive OR Gate	LS386		4030B	14
HC540	Octal Bus Buffer (3-State/Inv.)	LS540			20
HCT540	Octal Bus Buffer (3-State/Inv.)	LS540			20
HC541	Octal Bus Buffer (3-State)	LS541			20
HCT541	Octal Bus Buffer (3-State)	LS541			20
HC620	Octal Bus Transceiver (3-State/Inv.)	LS620			20
HC623	Octal Bus Transceiver (3-State)	LS623			20
HC640	Octal Bus Transceiver (3-State/Inv.)	LS640			20
HCT640	Octal Bus Transceiver (3-State/Inv.)	LS640			20
HC643	Octal Bus Transceiver (3-State)	LS643			20
HCT643	Octal Bus Transceiver (3-State)	LS643			20
HC4002	Dual 4-Input NOR Gate		4002B	LS02	14
HC4049	Hex Buffer/Converter (Inv.)		4049UB		16
HC4050	Hex Buffer/Converter		4050B		16
HC4072	Dual 4-Input OR Gate		4072B		14
HC4075	Triple 3-Input OR Gate		4075B		14
HC4078	8-Input NOR/OR Gate		4078B		14
HC7240	Octal Bus Buffer (3-State/Inv.)	LS240			20
HC7241	Octal Bus Buffer (3-State)	LS241			20
HC7244	Octal Bus Buffer (3-State)	LS244			20
HC7245	Octal Bus Transceiver (3-State)	LS245			20
HC7640	Octal Bus Transceiver (3-State/Inv.)	LS640			20
HC7643	Octal Bus Transceiver (3-State)	LS643			20
HC7645	Octal Bus Transceiver (3-State)	LS245			20

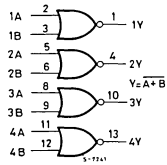
GATE/BUFFERS

HC00
HCT00



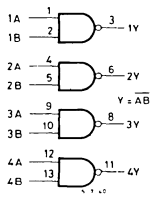
V_{CC} = Pin 14
GND = Pin 7

HC02
HCT02



V_{CC} = Pin 14
GND = Pin 7

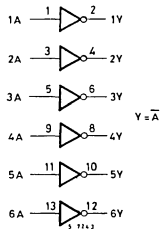
HC03



Open drain outputs

V_{CC} = Pin 14
GND = Pin 7

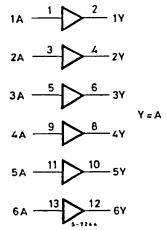
HC04
HCT04
HCU04 (**)
HC05 (*)



V_{CC} = Pin 14
GND = Pin 7

(*) Open drain outputs
(**) The internal circuits composed of single stage inverter.

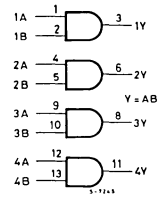
HCT7007
HC07 (*)



(*) Open drain outputs

V_{CC} = Pin 14
GND = Pin 7

HC08
HCT08
HC09 (*)

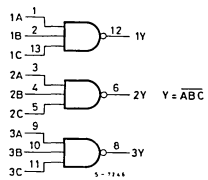


(*) Open drain outputs

V_{CC} = Pin 14
GND = Pin 7

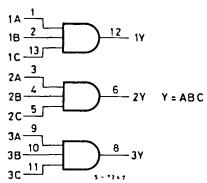
GATE/BUFFERS (Continued)

HC10
HCT10



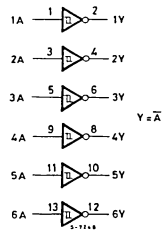
V_{CC} = Pin 14
GND = Pin 7

HC11



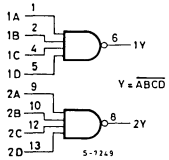
V_{CC} = Pin 14
GND = Pin 7

HC14
HCT14



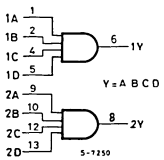
V_{CC} = Pin 14
GND = Pin 7

HC20



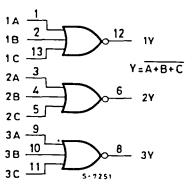
V_{CC} = Pin 14
GND = Pin 7
NC = Pins 3, 11

HC21



V_{CC} = Pin 14
GND = Pin 7
NC = Pins 3, 11

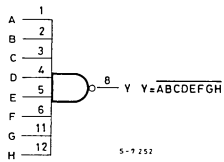
HC27
HCT27



V_{CC} = Pin 14
GND = Pin 7

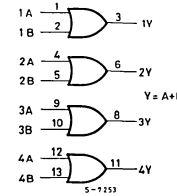
GATE/BUFFERS (Continued)

HC30
HCT30



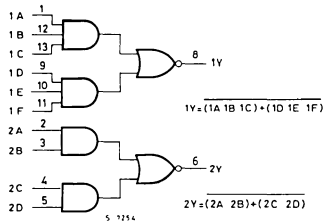
V_{CC} = Pin 14
GND = Pin 7
NC = Pins 9, 10, 13

HC32
HCT32



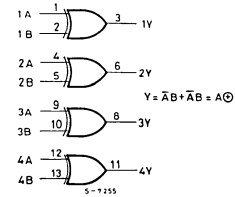
V_{CC} = Pin 14
GND = Pin 7

HC51



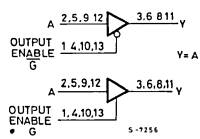
V_{CC} = Pin 14
GND = Pin 7

HC86
HCT86



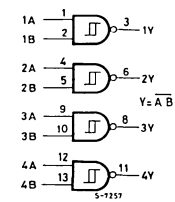
V_{CC} = Pin 14
GND = Pin 7

HC125
HC126
HCT125
HCT126



V_{CC} = Pin 14
GND = Pin 7

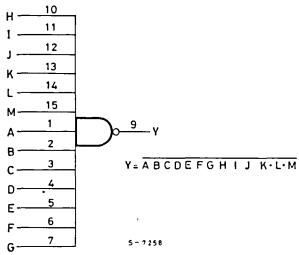
HC132



V_{CC} = Pin 14
GND = Pin 7

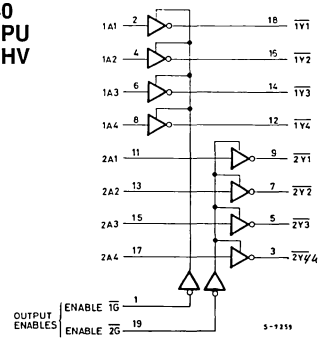
GATE/BUFFERS (Continued)

HC133



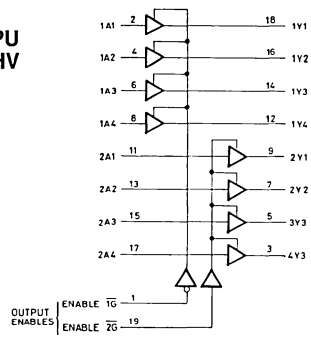
V_{CC} = Pin 16
GND = Pin 8

HC240
HCT240
HC240PU
HC240HV



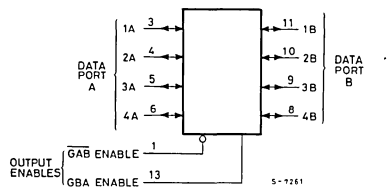
V_{CC} = Pin 20
GND = Pin 10

HC241
HCT241
HC241PU
HC241HV



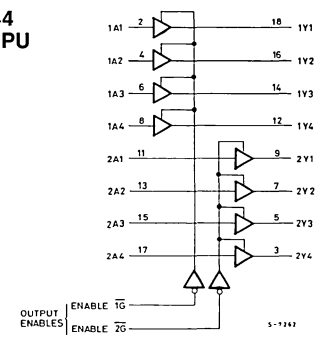
V_{CC} = Pin 20
GND = Pin 10

HC242
HC243



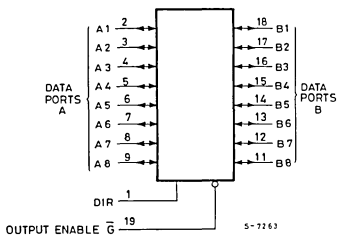
V_{CC} = Pin 14
GND = Pin 7
NC = Pins 2, 12

HC244
HCT244
HC244PU



V_{CC} = Pin 20
GND = Pin 10

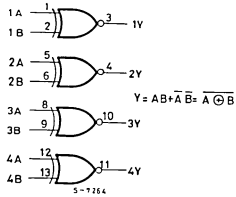
HC245
HCT245
HC7245
HC7645



V_{CC} = Pin 20
GND = Pin 10

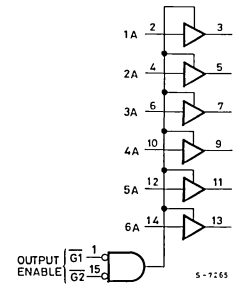
GATE/BUFFERS (Continued)

HC7266



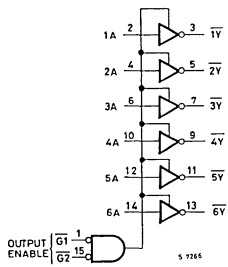
V_{CC} = Pin 14
GND = Pin 7

HC365



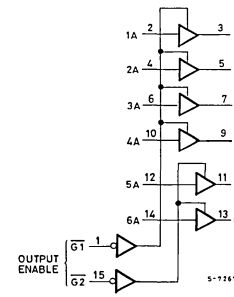
V_{CC} = Pin 16
GND = Pin 8

HC366



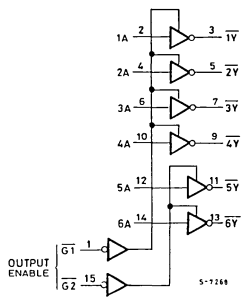
V_{CC} = Pin 16
GND = Pin 8

HC367
HCT367



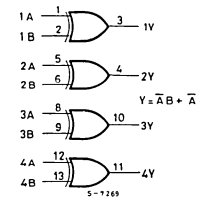
V_{CC} = Pin 16
GND = Pin 8

HC368
HCT368



V_{CC} = Pin 16
GND = Pin 8

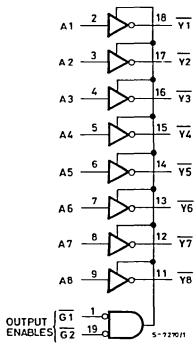
HC386



V_{CC} = Pin 14
GND = Pin 7

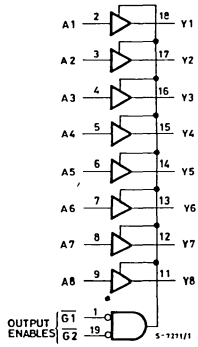
GATE/BUFFERS (Continued)

HC540
HCT540



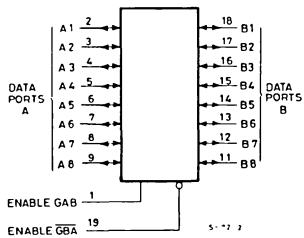
V_{CC} = Pin 20
GND = Pin 10

HC541
HCT541



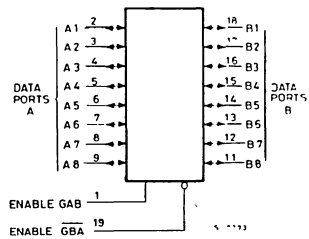
V_{CC} = Pin 20
GND = Pin 10

HC620 (Inverting)



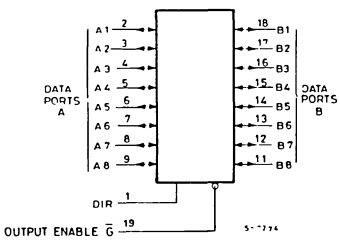
V_{CC} = Pin 20
GND = Pin 10

HC623 (Non Inverting)



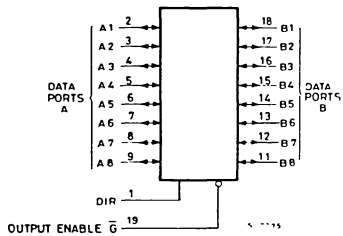
V_{CC} = Pin 20
GND = Pin 10

HC640 (Inverting)
HCT640
HC7640



V_{CC} = Pin 20
GND = Pin 10

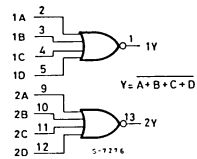
HC643
HCT643
HC7643



V_{CC} = Pin 20
GND = Pin 10

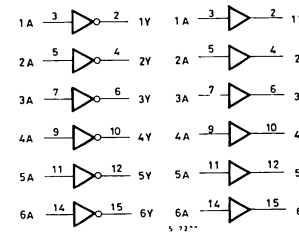
GATE/BUFFERS (Continued)

HC4002



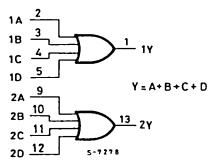
V_{CC} = Pin 14
GND = Pin 7
NC = Pins 6, 8

HC4049B
HC4050B



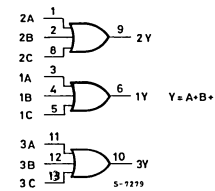
V_{CC} = Pin 1
GND = Pin 8
NC = Pins 13, 16

HC4072



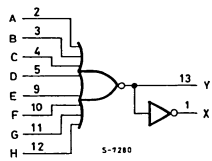
V_{CC} = Pin 14
GND = Pin 7
NC = Pins 6, 8

HC4075



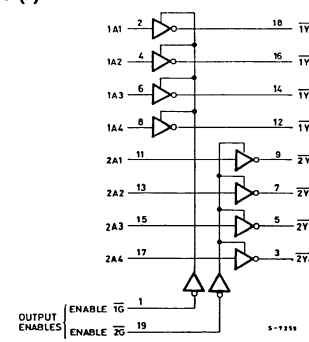
V_{CC} = Pin 14
GND = Pin 7

HC4078



V_{CC} = Pin 14
GND = Pin 7
NC = Pins 6, 8

HC7240 (*)

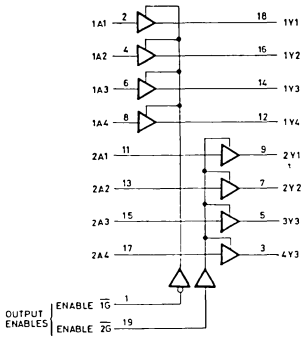


(*) Input with Hysteresis

V_{CC} = Pin 20
GND = Pin 10

GATE/BUFFERS (Continued)

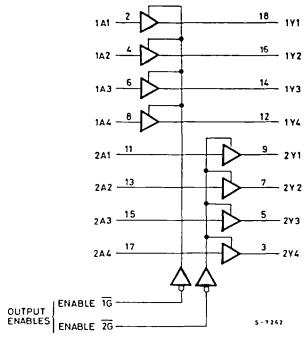
HC7241 (*)



(*) Input with Hysteresis

V_{CC} = Pin 20
GND = Pin 10

HC7244 (*)



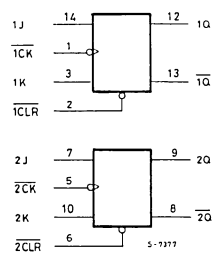
(*) Input with Hysteresis

V_{CC} = Pin 20
GND = Pin 10

FLIP-FLOP

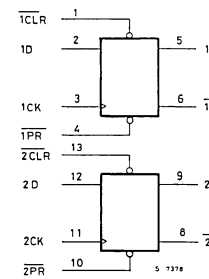
Type Number M54/74	Function	Functional Equivalent LSTTL 54/74	Functional Equivalent CMOS 4000B	Suggested Alternative LS 54/74 4000B	Package DIP
HC73	Dual J-K FLIP-FLOP with Clear	LS73		4027B	14
HC74	Dual D-Type FLIP-FLOP with Preset and Clear	LS74		4013B	14
HCT74	Dual D-Type FLIP-FLOP with Preset and Clear	LS74		4013B	14
HC76	Dual J-K FLIP-FLOP with Preset and Clear	LS76		4027B	16
HC107	Dual J-K FLIP-FLOP with Clear	LS107		4027B	14
HC109	Dual J-K FLIP-FLOP with Preset and Clear	LS109		4027B	16
HC112	Dual J-K FLIP-FLOP with Preset and Clear	LS112		4027B	16
HC113	Dual J-K FLIP-FLOP with Preset	LS113		4027B	14
HC174	Hex D-Type FLIP-FLOP with Clear	LS174		40174B	16
HCT174	Hex D-Type FLIP-FLOP with Clear	LS174		40174B	16
HC175	Quad D-Type FLIP-FLOP with Clear	LS175		40175B	16
HC273	Octal D-Type FLIP-FLOP with Clear	LS273			20
HCT273	Octal D-Type FLIP-FLOP with Clear	LS273			20
HC374	Octal D-Type FLIP-FLOP (3-State)	LS374			20
HCT374	Octal D-Type FLIP-FLOP (3-State)	LS374			20
HC377	Octal D-Type FLIP-FLOP	LS377			20
HC534	Octal D-Type FLIP-FLOP (3-State/Inv.)	LS534			20
HCT534	Octal D-Type FLIP-FLOP (3-State/Inv.)	LS534			20
HC564	Octal D-Type FLIP-FLOP (Inv./3-State)	LS564			20
HCT564	Octal D-Type FLIP-FLOP (3-State/Inv.)	LS564			20
HC574	Octal D-Type FLIP-FLOP (3-State)	LS574			20
HCT574	Octal D-F/F (3-State)	LS574			20
HC646	Octal Bus Transceiver Register (3-State)	LS646			24
HCT646	Octal Bus Transceiver Register (3-State)	LS646			24
HC648	Octal Bus Transceiver Register (3-State/Inv.)	LS648			24
HCT648	Octal Bus Transceiver Register (3-State/Inv.)	LS648			24
HC651	Octal Bus Transceiver Register (3-State/Inv.)	LS651			24
HCT651	Octal Bus Transceiver Register (3-State/Inv.)	LS651			24
HC652	Octal Bus Transceiver Register	LS652			24
HCT652	Octal Bus Transceiver Register	LS652			24

HC73



V_{CC} = Pin 4
GND = Pin 11

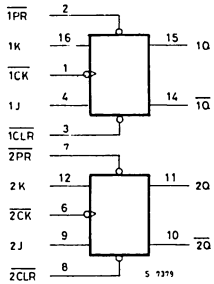
HC74
HCT74



V_{CC} = Pin 14
GND = Pin 7

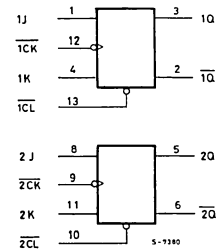
FLIP-FLOP (Continued)

HC76



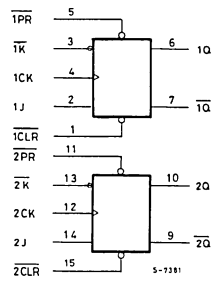
V_{CC} = Pin 5
GND = Pin 13

HC107



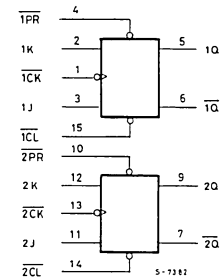
V_{CC} = Pin 14
GND = Pin 7

HC109



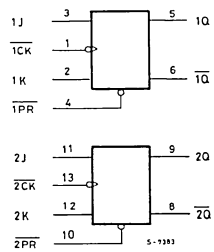
V_{CC} = Pin 16
GND = Pin 8

HC112



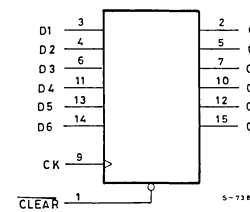
V_{CC} = Pin 16
GND = Pin 8

HC113



V_{CC} = Pin 14
GND = Pin 7

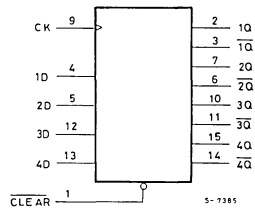
HC174
HCT174



V_{CC} = Pin 16
GND = Pin 8

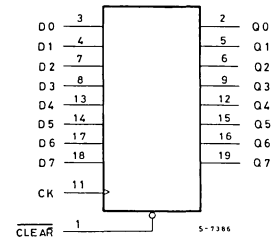
FLIP-FLOP (Continued)

HC175



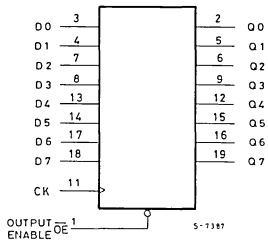
V_{CC} = Pin 16
GND = Pin 8

HC273
HCT273



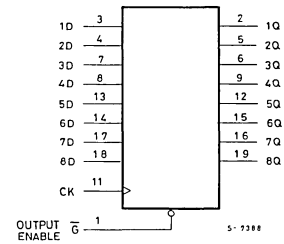
V_{CC} = Pin 20
GND = Pin 10

HC374
HCT374



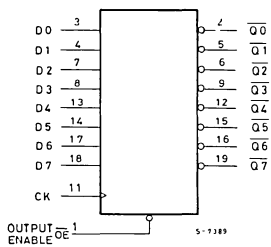
V_{CC} = Pin 20
GND = Pin 10

HC377



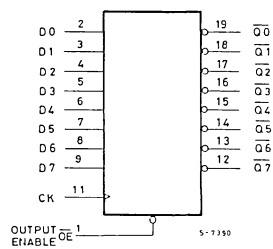
V_{CC} = Pin 20
GND = Pin 10

HC534
HCT534



V_{CC} = Pin 20
GND = Pin 10

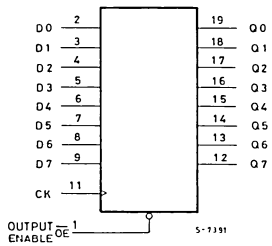
HC564
HCT564



V_{CC} = Pin 20
GND = Pin 10

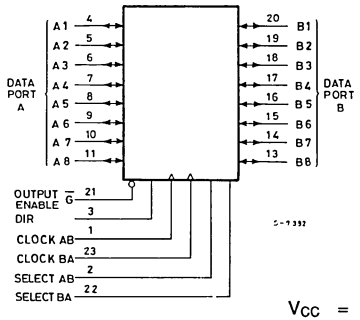
FLIP-FLOP (Continued)

HC574
HCT574



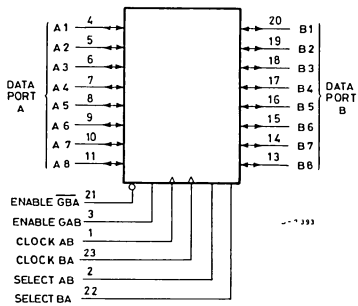
V_{CC} = Pin 20
GND = Pin 10

HC646/HCT646
HCT648/HCT648



V_{CC} = Pin 24
GND = Pin 12

HC651/HCT651
HC652/HCT652

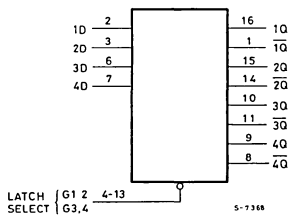


V_{CC} = Pin 24
GND = Pin 12

LATCHES

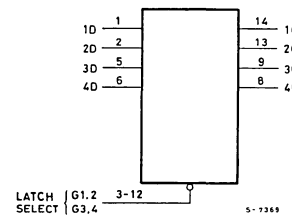
Type Number M54/74	Function	Functional Equivalent LSTTL 54/74	Functional Equivalent CMOS 4000B	Suggested Alternative LS 54/74 4000B	Package DIP
HC75	4-Bit D-Type Latch	LS75		4042B	16
HCT75	4-Bit D-Type Latch	LS75		4042B	16
HC77	4-Bit D-Type Latch	LS77		4042B	14
HC259	8 Bit Addressable Latch	LS259		4099B	16
HCT7259	8 Bit Addressable Latch (Open drain)	LS259		4099B	16
HC279	Quad R-S Latch	LS279			16
HC373	Octal D-Type Latch (3-State)	LS373			20
HCT373	Octal D-Type Latch (3-State)	LS373			20
HC375	Quad D-Type Latch	LS375		4042B	16
HC533	Octal D-Type Latch (3-State/Inv.)	LS533			20
HCT533	Octal D-Type Latch (3-State/Inv.)	LS533			20
HC563	Octal D-Type Latch (3-State/Inv.)	LS563			20
HCT563	Octal D-Type Latch (3-State/Inv.)	LS563			20
HC573	Octal D-Type Latch (3-State)	LS573			20
HCT573	Octal D-Type Latch (3-State)	LS573			20

HC75
HCT75



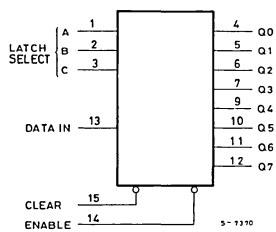
V_{CC} = Pin 5
GND = Pin 12

HC77



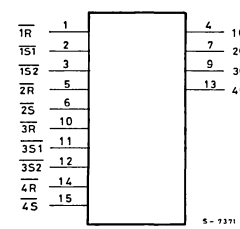
V_{CC} = Pin 4
GND = Pin 11
NC = Pins 7, 10

HC259
HCT7259



V_{CC} = Pin 16
GND = Pin 8

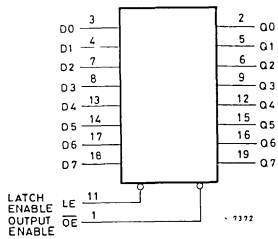
HC279



V_{CC} = Pin 16
GND = Pin 8

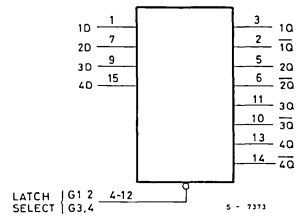
LATCHES (Continued)

HC373
HCT373



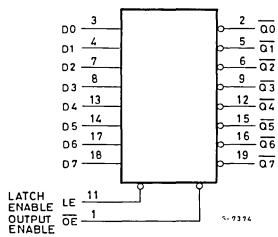
V_{CC} = Pin 20
GND = Pin 10

HC375



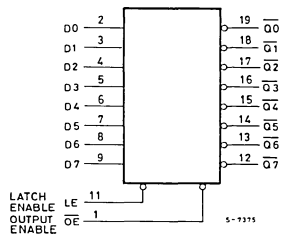
V_{CC} = Pin 16
GND = Pin 8

HC533
HCT533



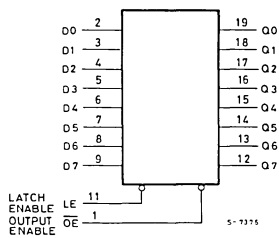
V_{CC} = Pin 20
GND = Pin 10

HC563
HCT563



V_{CC} = Pin 20
GND = Pin 10

HC573
HCT573

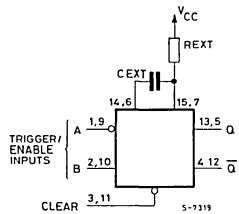


V_{CC} = Pin 20
GND = Pin 10

MULTIVIBRATOR

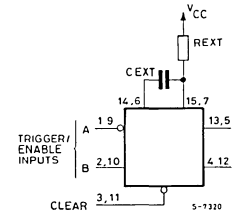
Type Number M54/74	Function	Functional Equivalent LSTTL 54/74·	Functional Equivalent CMOS 4000B	Suggested Alternative LS 54/74 4000B	Package DIP
HC123	Dual Retrigg. Monostable Multivib. with Clear	LS123		4538/4098	16
HC123A	Dual Retrigg. Monostable Multivib. with Clear	LS123		4538/4098	16
HC221	Dual Monostable Multivib. with Clear	LS221		4538/4098	16
HC221A	Dual Monostable Multivib. with Clear	LS221		4538/4098	16
HC423	Dual Retrigg. Monostable Multivib. with Clear	LS423		4538/4098	16
HC423A	Dual Retrigg. Monostable Multivib. with Clear	LS423		4538/4098	16
HC4538	Dual Retrigg. Monostable Multivibrator		4538B	LS423	16

HC123
HC123A



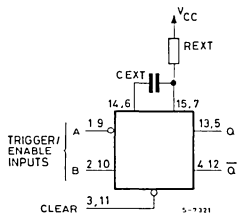
V_{CC} = Pin 16
GND = Pin 8

HC221
HC221A



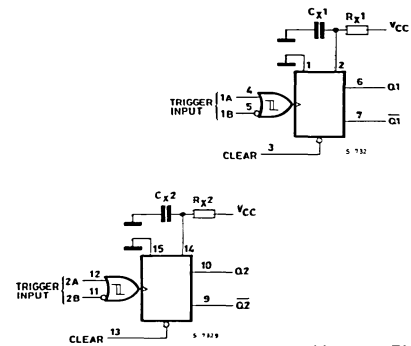
V_{CC} = Pin 16
GND = Pin 8

HC423
HC423A



V_{CC} = Pin 16
GND = Pin 8

HC4538

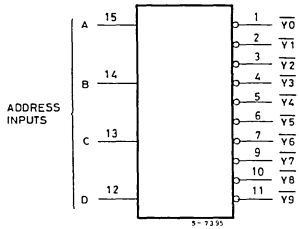


V_{CC} = Pin 16
GND = Pin 8

DECODER / ENCODER

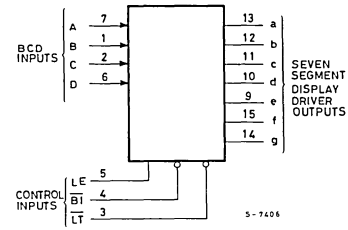
Type Number M54/74	Function	Functional Equivalent LSTTL 54/74	Functional Equivalent CMOS 4000B	Suggested Alternative LS 54/74 4000B	Package DIP
HC42	BCD to Decimal Decoder	LS42		4028B	16
HC131	3 to 8 Line Decoder Latch	LS131			16
HC137	3 to 8 Line Decoder Latch (Inv.)	LS137		4028B	16
HCT137	3 to 8 Line Decoder Latch (Inv.)	LS137		4028B	16
HC138	3 to 8 Line Decoder (Inv.)	LS138		4028B	16
HCT138	3 to 8 Line Decoder (Inv.)	LS138		4028B	16
HC139	Dual 2 to 4 Line Decoder/Demultiplexer	LS139		4556B	16
HCT139	Dual 2 to 4 Line Decoder/Demultiplexer	LS139		4556B	16
HC147	10 to 4 Line Priority Encoder	LS147			16
HC148	8 to 3 Line Priority Encoder	LS148			16
HC154	4 to 16 Line Decoder/Demultiplexer	LS154		4515B	24
HC155	Dual 2 to 4 Line Decoder / 3 to 8 Line Dec.	LS155			16
HC237	3 to 8 Line Decoder Latch			4028B	16
HC238	3 to 8 Line Decoder			4028B	16
HC4028	BDC to Decimal Decoder		4028B	LS42	16
HC4511	BDC to 7-Segment L/D/D (Led)		4511B	LS47/48/49	16
HC4514	4 to 16 Line Decoder Latch		4514B	–	24
HC4515	4 to 16 Line Decoder Latch (Inv.)		4515B	LS154	24
HC4543	BCD to 7-Segment L/D/D (LCD)		4543B	LS143	16

HC42



V_{CC} = Pin 16
GND = Pin 8

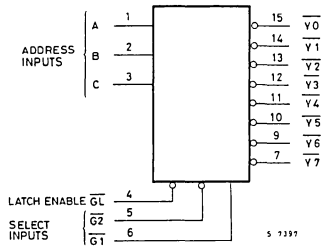
HC131



V_{CC} = Pin 16
GND = Pin 8

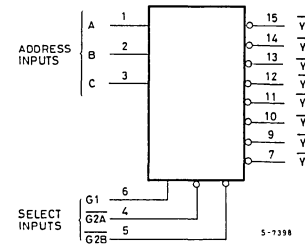
DECODER / ENCODER (Continued)

HC137
HCT137



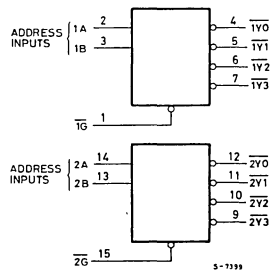
V_{CC} = Pin 16
GND = Pin 8

HC138
HCT138



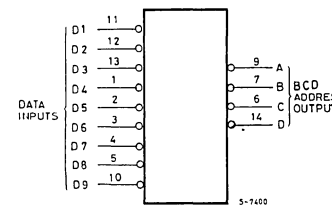
V_{CC} = Pin 16
GND = Pin 8

HC139
HCT139



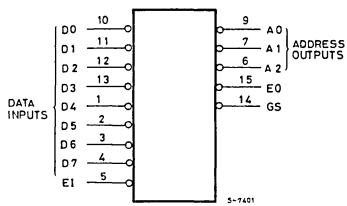
V_{CC} = Pin 16
GND = Pin 8

HC147



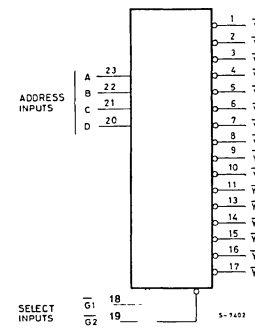
V_{CC} = Pin 16
GND = Pin 8

HC148



V_{CC} = Pin 16
GND = Pin 8

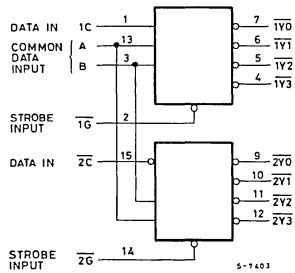
HC154



V_{CC} = Pin 24
GND = Pin 12

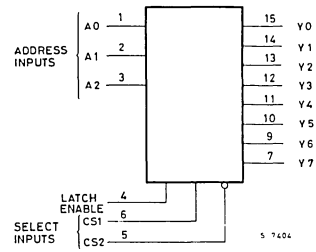
DECODER / ENCODER (Continued)

HC155



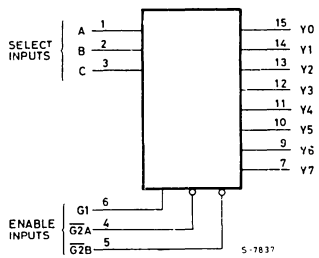
V_{CC} = Pin 16
GND = Pin 8

HC237



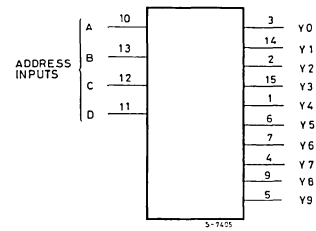
V_{CC} = Pin 16
GND = Pin 8

HC238



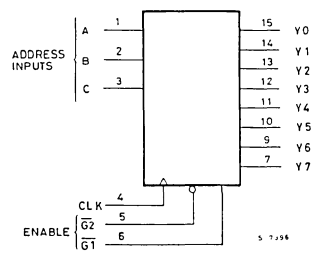
V_{CC} = Pin 16
GND = Pin 8

HC4028



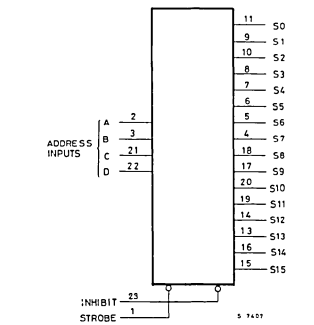
V_{CC} = Pin 16
GND = Pin 8

HC4511



V_{CC} = Pin 16
GND = Pin 8

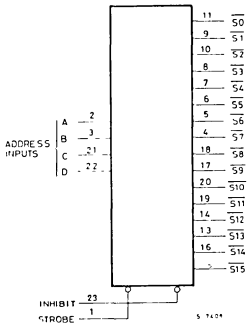
HC4514



V_{CC} = Pin 24
GND = Pin 12

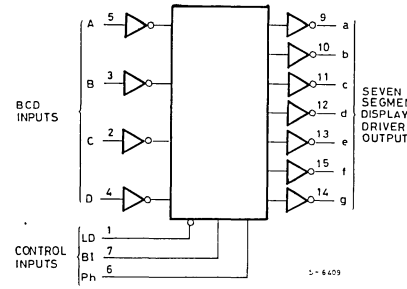
DECODER / ENCODER (Continued)

HC4515



V_{CC} = Pin 24
GND = Pin 12

HC4543

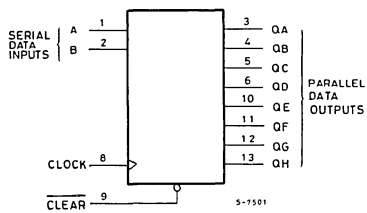


V_{CC} = Pin 16
GND = Pin 8

REGISTER

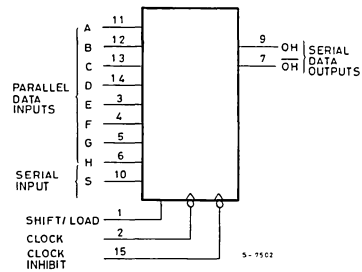
Type Number M54/74	Function	Functional Equivalent LSTTL 54/74	Functional Equivalent CMOS 4000B	Suggested Alternative LS 54/74 4000B	Package DIP
HC164	8 Bit SIPO Shift Register	LS164		4034B	14
HCT164	8 Bit PISO Shift Register	LS164		4034B	14
HC165	8 Bit PISO Shift Register	LS165		4021B	16
HCT165	8 Bit PISO Shift Register	LS165		4021B	16
HC166	8 Bit PISO Shift Register	LS166		4021B	16
HC173	Quad D-Type Register (3-State)	LS173			16
HC194	4 Bit PIPO Shift Register	LS194		40194B	16
HC195	4 Bit PIPO Shift Register	LS195		4035B	16
HC299	8 Bit PIPO Shift Register (3-State)	LS299			20
HC323	8 Bit PIPO Shift Register (3-State)	LS323			20
HC595	8 Bit Shift Register Latch (3-State)	LS595		4034B	16
HC597	8 Bit Latch Shift Register	LS597			16
HC670	4 Word x 4 Bit Register File (3-State)	LS670			16
HC4094	8 Bit SIPO Shift Register Latch (3-State)		4094B	LS164	16

HC164
HCT164



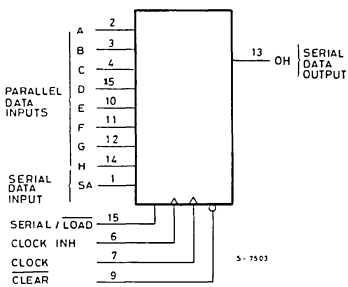
V_{CC} = Pin 14
GND = Pin 7

HC165
HCT165



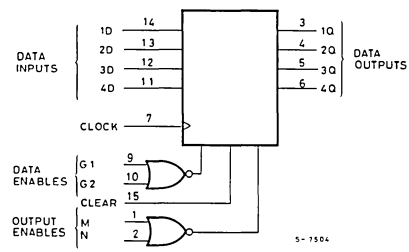
V_{CC} = Pin 16
GND = Pin 8

HC166



V_{CC} = Pin 16
GND = Pin 8

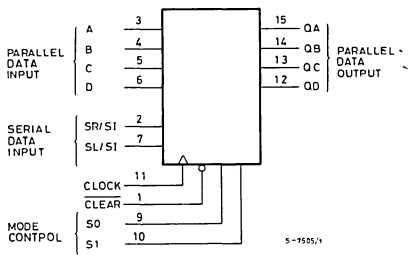
HC173



V_{CC} = Pin 16
GND = Pin 8

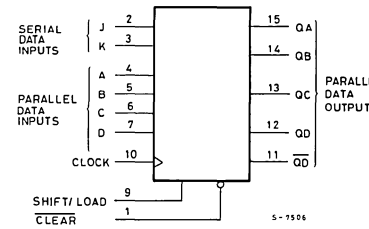
REGISTER (Continued)

HC194



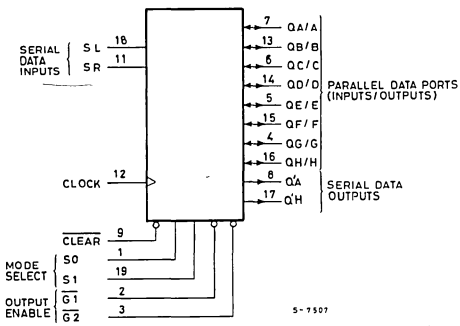
V_{CC} = Pin 16
GND = Pin 8

HC195



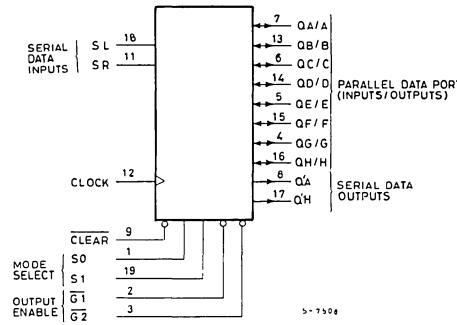
V_{CC} = Pin 16
GND = Pin 8

HC299



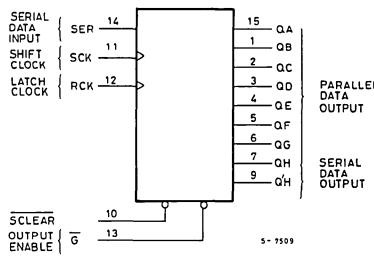
V_{CC} = Pin 20
GND = Pin 10

HC323



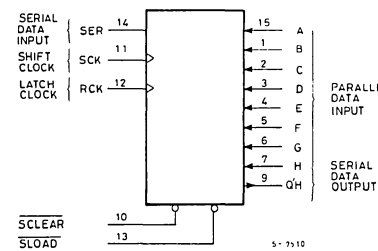
V_{CC} = Pin 20
GND = Pin 10

HC595



V_{CC} = Pin 16
GND = Pin 8

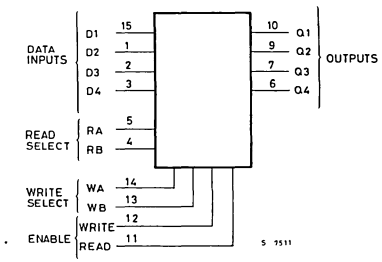
HC597



V_{CC} = Pin 16
GND = Pin 8

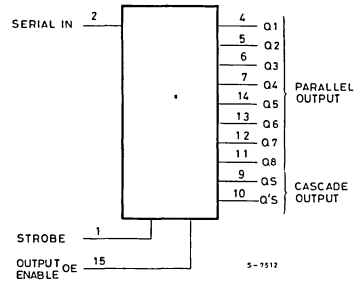
REGISTER (Continued)

HC670



V_{CC} = Pin 16
GND = Pin 8

HC4094



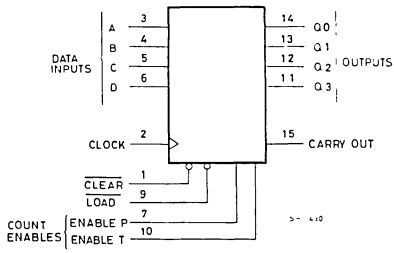
V_{CC} = Pin 16
GND = Pin 8

COUNTERS

Type Number M54/74	Function	Functional Equivalent LSTTL 54/74	Functional Equivalent CMOS 4000B	Suggested Alternative LS 54/74 4000B	Package DIP
HC160	Sync. Decade Counter with Async. Clear	LS160		40160B	16
HCT160	Sync. Decade Counter with Async. Clear	LS160		40160B	16
HC161	Sync. Binary Counter with Async. Clear	LS161		40161B	16
HCT161	Sync. Binary Counter with Async. Clear	LS161		40161B	16
HC162	Sync. Decade Counter with Sync. Clear	LS162		40162B	16
HCT162	Sync. Decade Counter with Sync. Clear	LS162		40162B	16
HC163	Sync. Binary Counter with Sync. Clear	LS163		40163B	16
HCT163	Sync. Binary Counter with Sync. Clear	LS163		40163B	16
HC190	BCD Up/Down Counter Sync.	LS190		4510B	16
HC191	4 Bit Binary Up/Down Counter Sync.	LS191		4516B	16
HC192	Sync. Up/Down Decade Counter	LS192		40192B	16
HC193	Sync. Up/Down Binary Counter	LS193		40193B	16
HC292	Programmable Divider/Timer	LS292			16
HC294	Programmable Divider/Timer	LS294			16
HC7292	Programmable Divider/Timer				16
HC7294	Programmable Divider/Timer				16
HC390	Dual Decade Counter	LS390		4518B	16
HC393	Dual Binary Counter	LS393		4520B	14
HCT393	Dual Binary Counter	LS393		4520B	14
HC590	8 Bit Binary Counter Register (3-State)	LS590			16
HC592	8 Bit Binary Counter Register	LS592			16
HC593	8 Bit Binary Counter with Input Register (3-State)	LS593			20
HC690	Decade Counter Register (3-State)	LS690			20
HC691	4 Bit Binary Counter Register (3-State)	LS691			20
HC692	Decade Counter Register (3-State)	LS692			20
HC693	4 Bit Binary Counter Register (3-State)	LS693			20
HC696	U/D Decade Counter Register (3-State)	LS696			20
HC697	U/D 4-Bit Binary Counter/Register (3-State)	LS697			20
HC698	U/D Decade Counter Register (3-State)	LS698			20
HC699	U/D 4-Bit Binary Counter/Register (3-State)	LS699			20
HC4017	Decade Counter/Divider		4017B		16
HC4020	14-Stage Binary Counter		4020B		16
HC4022	Octal Counter/Divider		4022B		16
HC4024	7-Stage Binary Counter		4024B		14
HC4040	12-Stage Binary Counter		4040B		16
HC4060	14-Stage Binary Counter/Oscillator		4060B		16
HC40102	Dual BCD Programmable Down Counter		40102B		16
HC40103	8 Bit Binary Prog. Down Counter		40103B		16
HC4518	Dual Decade Counter		4518B		16
HC4520	Dual 4 Bit Binary Counter		4520B		16

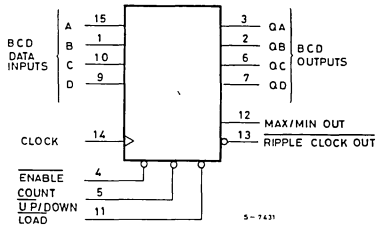
COUNTERS (Continued)

HC160/HC162
HC161/HC163
HCT160/HCT162
HCT161/HCT163



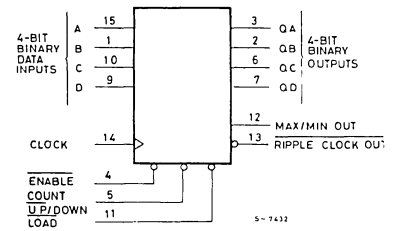
V_{CC} = Pin 16
GND = Pin 8

HC190



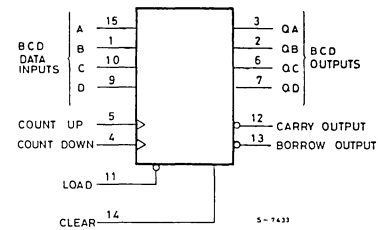
V_{CC} = Pin 16
GND = Pin 8

HC191



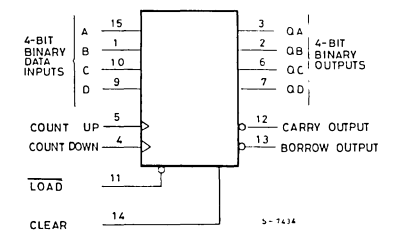
V_{CC} = Pin 16
GND = Pin 8

HC192



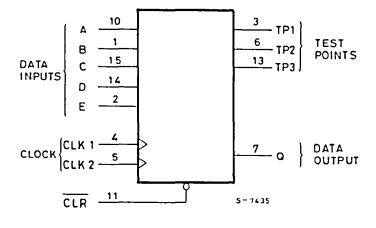
V_{CC} = Pin 16
GND = Pin 8

HC193



V_{CC} = Pin 16
GND = Pin 8

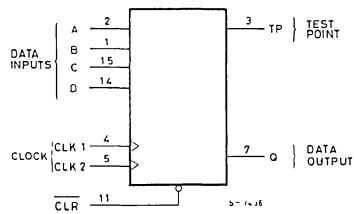
HC292/HC7292



V_{CC} = Pin 16
GND = Pin 8
NC = Pins 9, 12

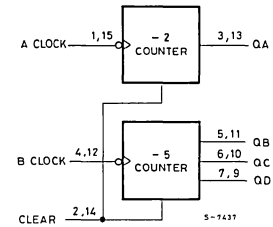
COUNTERS (Continued)

HC294/HC7294



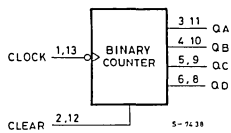
V_{CC} = Pin 16
GND = Pin 8
NC = Pins 6, 9, 10, 12, 13

HC390



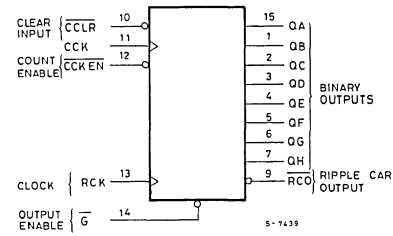
V_{CC} = Pin 16
GND = Pin 8

HC393
HCT393



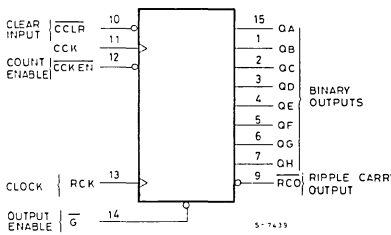
V_{CC} = Pin 14
GND = Pin 7

HC590



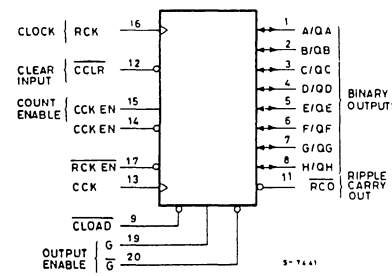
V_{CC} = Pin 16
GND = Pin 8

HC592



V_{CC} = Pin 16
GND = Pin 8

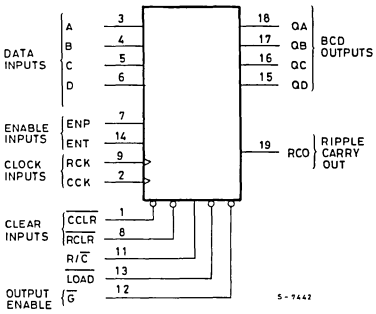
HC593



V_{CC} = Pin 20
GND = Pin 10

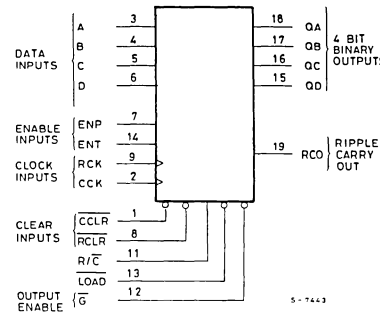
COUNTERS (Continued)

HC690



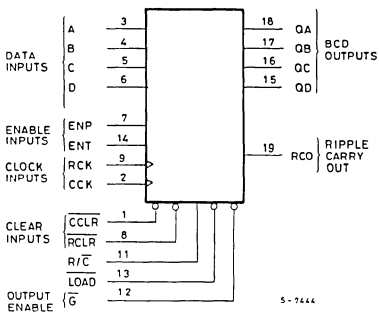
V_{CC} = Pin 20
GND = Pin 10

HC691



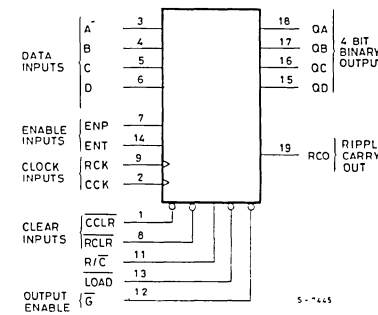
V_{CC} = Pin 20
GND = Pin 10

HC692



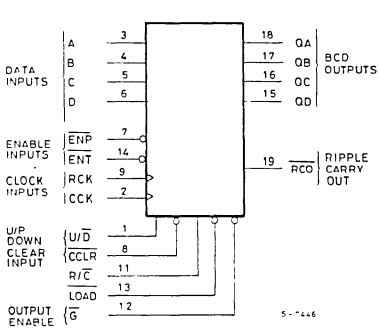
V_{CC} = Pin 20
GND = Pin 10

HC693



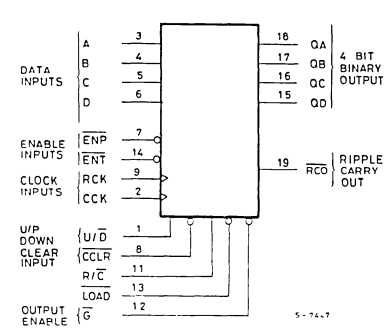
V_{CC} = Pin 20
GND = Pin 10

HC696



V_{CC} = Pin 20
GND = Pin 10

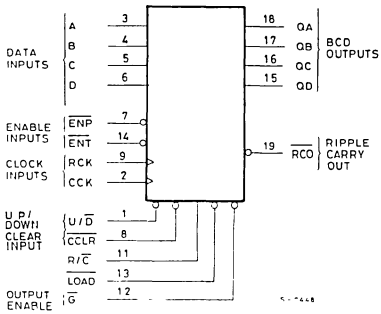
HC697



V_{CC} = Pin 20
GND = Pin 10

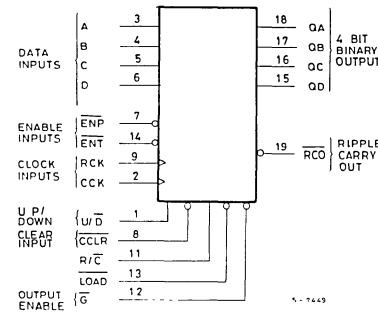
COUNTERS (Continued)

HC698



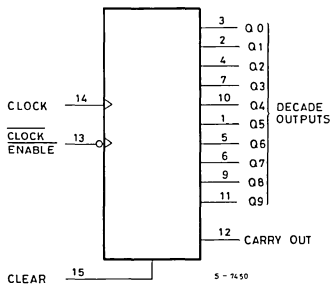
V_{CC} = Pin 20
GND = Pin 10

HC699



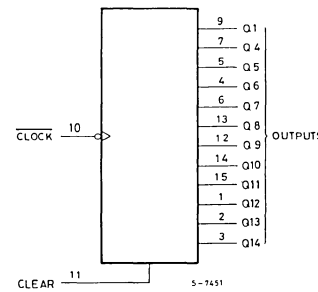
V_{CC} = Pin 20
GND = Pin 10

HC4017



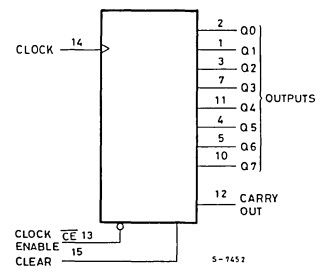
V_{CC} = Pin 16
GND = Pin 8

HC4020



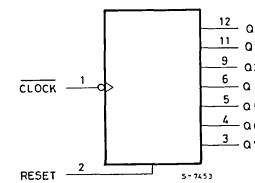
V_{CC} = Pin 16
GND = Pin 8

HC4022



V_{CC} = Pin 16
GND = Pin 8
NC = Pins 6, 9

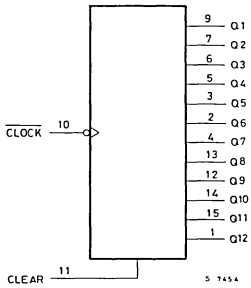
HC4024



V_{CC} = Pin 14
GND = Pin 7
NC = Pins 8, 10, 12

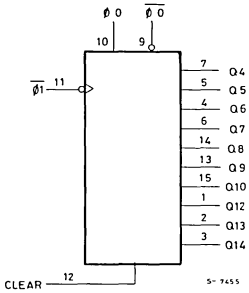
COUNTERS (Continued)

HC4040



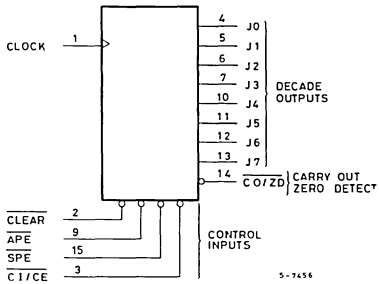
V_{CC} = Pin 16
GND = Pin 8

HC4060



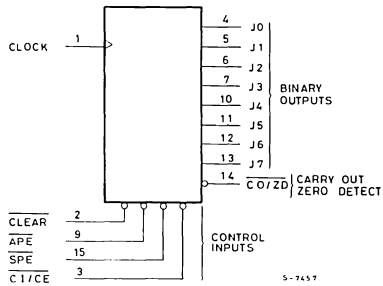
V_{CC} = Pin 16
GND = Pin 8

HC40102



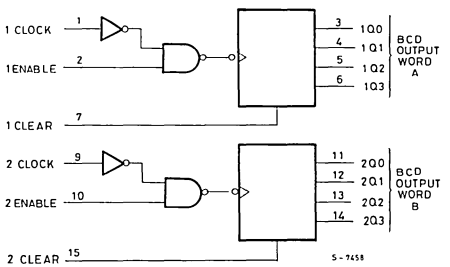
V_{CC} = Pin 16
GND = Pin 8

HC40103



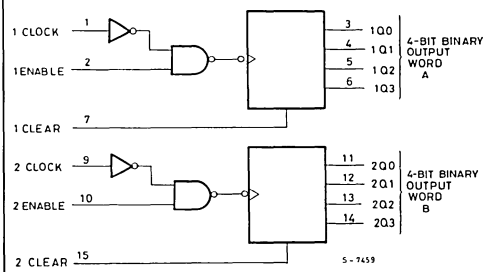
V_{CC} = Pin 16
GND = Pin 8

HC4518



V_{CC} = Pin 16
GND = Pin 8

HC4520

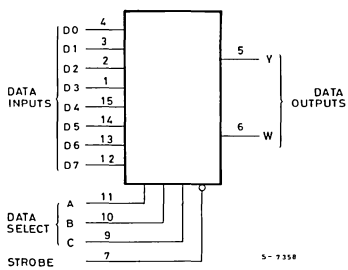


V_{CC} = Pin 16
GND = Pin 8

MULTIPLEXER

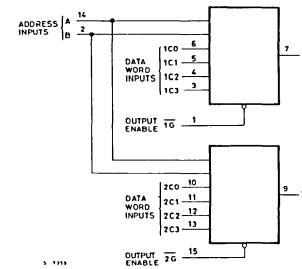
Type Number M54/74	Function	Functional Equivalent LSTTL 54/74	Functional Equivalent CMOS 4000B	Suggested Alternative LS 54/74 4000B	Package DIP
HC151	8-Channel Multiplexer	LS151		4512B	16
HC153	Dual 4-Channel Multiplexer	LS153			16
HC157	Quad 2-Channel Multiplexer	LS157			16
HCT157	Quad 2-Channel Multiplexer	LS157			16
HC158	Quad 2-Channel Multiplexer (Inv.)	LS158			16
HCT158	Quad 2-Channel Multiplexer (Inv.)	LS158			16
HC251	8-Channel Multiplexer (3-State)	LS251		4512B	16
HC253	Dual 4-Channel Multiplexer (3-State)	LS253			16
HC257	Quad 2-Channel Multiplexer (3-State)	LS257			16
HCT257	Quad 2-Channel Multiplexer (3-State)	LS257			16
HC258	Quad 2-Channel Multiplexer (3-State/Inv.)	LS258			16
HCT258	Quad 2-Channel Multiplexer (3-State/Inv.)	LS258			16
HC298	Quad 2-Channel Multiplexer Register	LS298			16
HC352	Dual 4-Channel Multiplexer (Inv.)	LS352			16
HC353	Dual 4-Channel Multiplexer (3-State)	LS353			16
HC354	8-Channel Multiplexer/Register (3-State)	LS354		4512B	20
HC356	8-Channel Multiplexer/Register (3-State)	LS356		4512B	20
HC4016	Quad Bilateral Switch		4016B		14
HC4051	8-Channel Analog Multiplexer/Demul.		4051B		16
HC4052	Dual 4 Channel Analog Multiplexer Demul.		4052B		16
HC4053	Triple two Channel Analog Multiplexer Demul.		4053B		16
HC4066	Quad Bilateral Switch		4066B		14
HC4316	Quad Bilateral Switch				16
HC4351	8-Channel Analog Multiplexer/Demul.		4051B		20
HC4352	Dual 4 Channel Analog Multiplexer Demul.		4052B		20
HC4353	Triple two Channel Analog Multiplexer Demul.		4053B		20

HC151



V_{CC} = Pin 16
GND = Pin 8

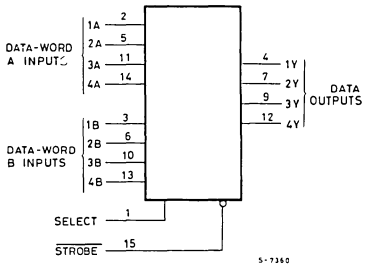
HC153



V_{CC} = Pin 16
GND = Pin 8

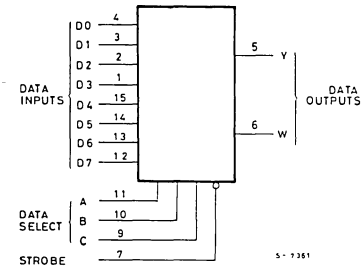
MULTIPLEXER (Continued)

HC157 / HCT157
HC158 / HCT158



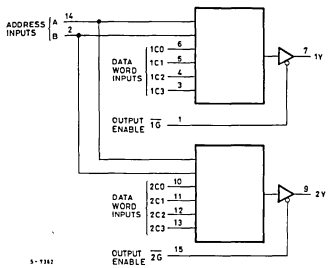
V_{CC} = Pin 16
GND = Pin 8

HC251



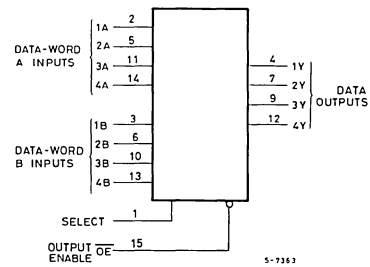
V_{CC} = Pin 16
GND = Pin 8

HC253



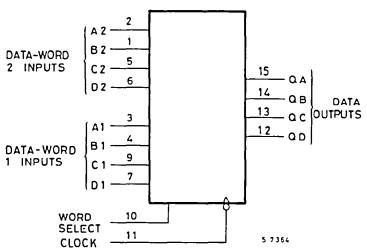
V_{CC} = Pin 16
GND = Pin 8

HC257 / HCT257 (Non Inverting Outputs)
HC258 / HCT258 (Inverting Outputs)



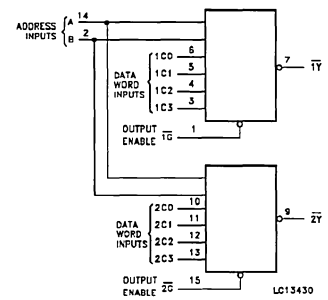
V_{CC} = Pin 16
GND = Pin 8

HC298



V_{CC} = Pin 16
GND = Pin 8

HC352

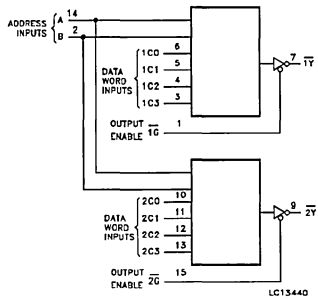


3-State Output

V_{CC} = Pin 16
GND = Pin 8

MULTIPLEXER (Continued)

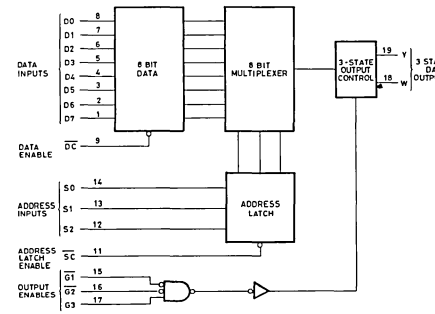
HC353



3-State Output

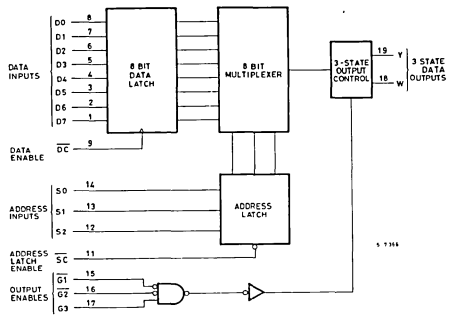
V_{CC} = Pin 16
GND = Pin 8

HC354



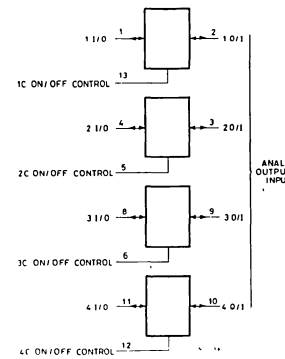
V_{CC} = Pin 20
GND = Pin 10

HC356



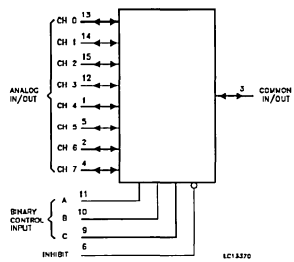
V_{CC} = Pin 20
GND = Pin 10

HC4016



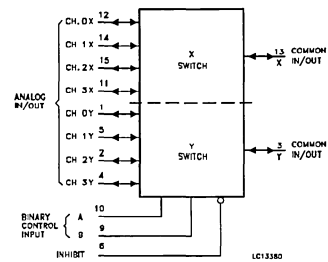
V_{CC} = Pin 14
GND = Pin 7

HC4051



V_{CC} = Pin 20 = Positive analog and digital power supply
V_{EE} = Pin 7 = Negative analog power supply
GND = Pin 8 = Negative digital power supply
Control inputs are referenced to GND analog channel are referenced to V_{EE}. V_{EE} must be ≤ GND

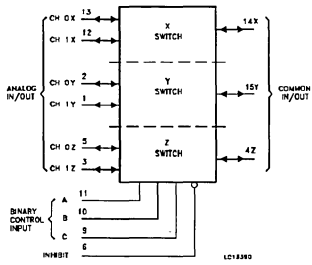
HC4052



V_{CC} = Pin 20 = Positive analog and digital power supply
V_{EE} = Pin 7 = Negative analog power supply
GND = Pin 8 = Negative digital power supply
Control inputs are referenced to GND channel are referenced to V_{EE}. V_{EE} must be ≤ GND

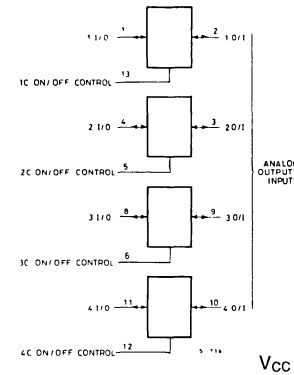
MULTIPLEXER (Continued)

HC4053



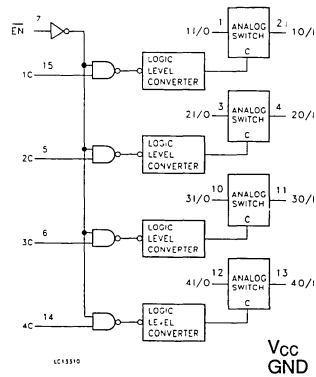
V_{CC} = Pin 20 = Positive analog and digital power supply
V_{EE} = Pin 7 = Negative analog power supply
GND = Pin 8 = Negative digital power supply
Control inputs are referenced to GND analog channel are referenced to V_{EE}. V_{EE} must be ≤ GND

HC4066



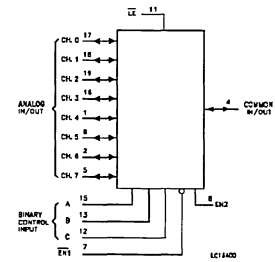
V_{CC} = Pin 14
GND = Pin 7
1I/O: 2I/O: 3I/O: 4I/O = Analog Inputs/Outputs

HC4316



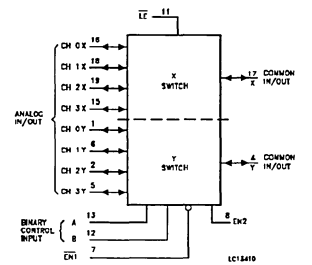
V_{CC} = Pin 16
GND = Pin 8

HC4351



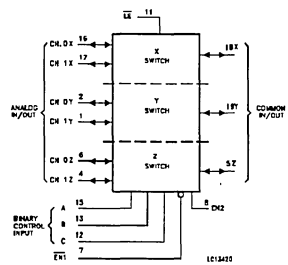
V_{CC} = Pin 20 = Positive analog and digital power supply
V_{EE} = Pin 9 = Negative analog power supply
GND = Pin 10 = Negative digital power supply
Control inputs are referenced to GND analog channel are referenced to V_{EE}. V_{EE} must be ≤ GND

HC4352



V_{CC} = Pin 20 = Positive analog and digital power supply
V_{EE} = Pin 9 = Negative analog power supply
GND = Pin 10 = Negative digital power supply
Control inputs are referenced to GND analog channel are referenced to V_{EE}. V_{EE} must be ≤ GND

HC4353

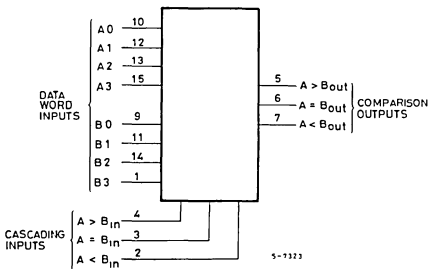


V_{CC} = Pin 20 = Positive analog and digital power supply
V_{EE} = Pin 9 = Negative analog power supply
GND = Pin 10 = Negative digital power supply
Control inputs are referenced to GND channel are referenced to V_{EE}. V_{EE} must be ≤ GND

COMPARATORS

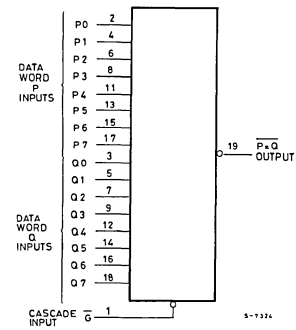
Type Number M54/74	Function	Functional Equivalent LSTTL 54/74	Functional Equivalent CMOS 4000B	Suggested Alternative LS 54/74 4000B	Package DIP
HC85	4-Bit Magnitude Comparator	LS85		4063B/4585B	16
HC688	8-Bit Equality Comparator	LS688			20
HCT688	8-Bit Equality Comparator	LS688			20

HC85



V_{CC} = Pin 16
GND = Pin 8

HC688 HCT688

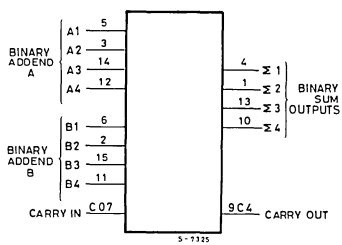


V_{CC} = Pin 20
GND = Pin 10

ADDER

Type Number M54/74	Function	Functional Equivalent LSTTL 54/74	Functional Equivalent CMOS 4000B	Suggested Alternative LS 54/74 4000B	Package DIP
HC283	4-Bit Binary Full-Adder	LS283		4008	16

HC283

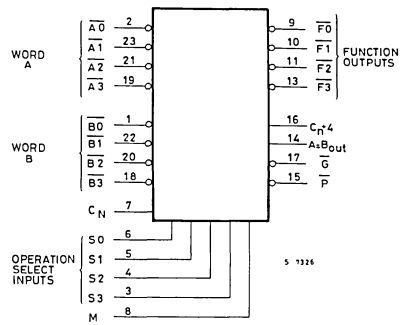


V_{CC} = Pin 16
GND = Pin 8

ALU

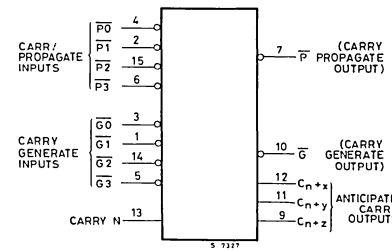
Type Number M54/74	Function	Functional Equivalent LSTTL 54/74	Functional Equivalent CMOS 4000B	Suggested Alternative LS 54/74 4000B	Package DIP
HC181	Arithmetic Logic Unit	LS181		40181B	24
HC182	Look Ahead Carry Generator	LS182		40182B	16

HC181



V_{CC} = Pin 24
GND = Pin 12

HC182

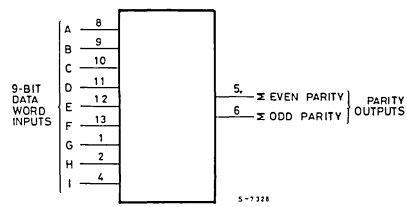


V_{CC} = Pin 16
GND = Pin 8

PARITY TREE

Type Number M54/74	Function	Functional Equivalent LSTTL 54/74	Functional Equivalent CMOS 4000B	Suggested Alternative LS 54/74 4000B	Package DIP
HC280	9-Bit Parity Generator / Checker	LS280		4001B	14

HC280



V_{CC} = Pin 14
GND = Pin 7
NC = Pin 3

GENERAL AND APPLICATION INFORMATION

INTRODUCING HS-C^2 MOS

The rapid advances recently made in silicon-gate CMOS technology have lead to the introduction of a logic family that sets new and much higher standards of performance.
This family called HS-C^{2}MOS*, exhibits a greatly improved speed/product performance when compared with other existing logic families and allows greater flexibility in both system design and configuration.
The HS-C^{2}MOS family is pin compatible with industry standard LSTTL and many of the CMOS 4000B types. It does, however, have considerable advantages over both LSTTL and earlier generation CMOS in terms of power consumption, speed, noise immunity and supply voltage range.
This new family of high performance devices is being jointly developed and manufactured by ST and Toshiba who between them have many years of production and marketing expertise in the field of CMOS logic. The synergism of two major manufacturers will ensure the rapid introduction of the family into the market place and will guarantee its continuity, and continuing development.
HS-C^{2}MOS will offer to the user a cost-effective and high performance solution to an ever increasing number of applications and open up the way to truly light weight field portable instruments and advanced systems.

High Speed

The HS-C^{2}MOS logic family has been designed to match or better the dynamic characteristics of LSTTL thus giving a high performance family which can be used wherever high speed as well as low power consumption is important. (See Fig. 3)
Propagation delays for the new family are around ten times lower than those for metal-gate CMOS devices and in the order of five times lower than earlier silicon-gate devices.

Figure 2 - Propagation Delay Time vs. Load Capacitance

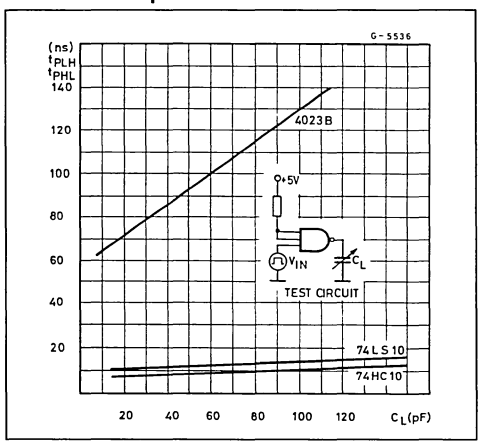


Figure 1 - Operating Frequency

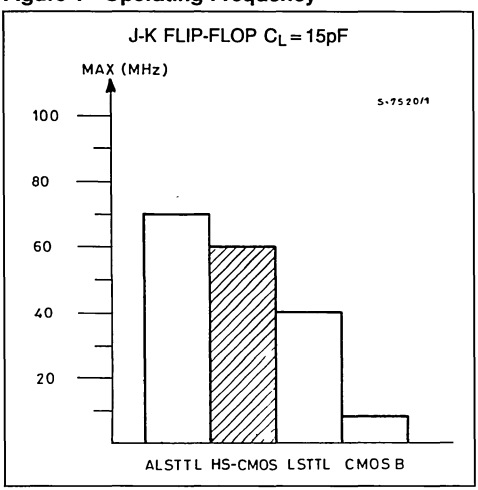
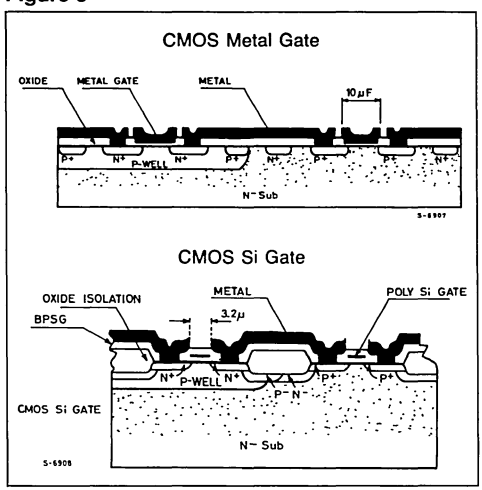


Figure 3



Low Power

For every reduction in system power there comes a corresponding reduction in system costs. Smaller, lighter power supplies can be used, heatsinks can be eliminated or drastically reduced in size, forced air cooling can often be dispensed with and more devices can be included on a single board. All this translates into better utilization of printed circuit board real-estate and a bottom line that reads "lower costs".

CMOS has an enormous and well established advantage over LSTTL in terms of power consumption. Typical quiescent dissipation per gate for CMOS is in the order of 10 nW whilst for LSTTL a typical value is up around the 8 mW mark. At a system level too the HS-C^{2}MOS family offers a power reduction of more than 100 times when compared with LSTTL.

Figure 4 - Current Dissipation vs. Operating Frequency

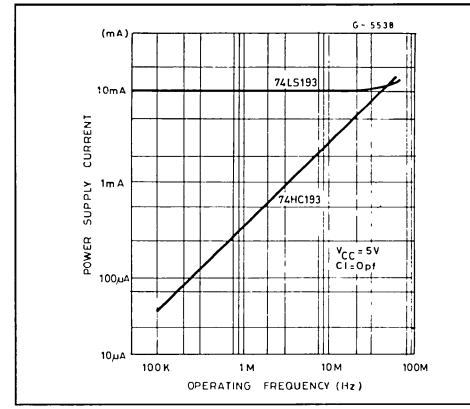
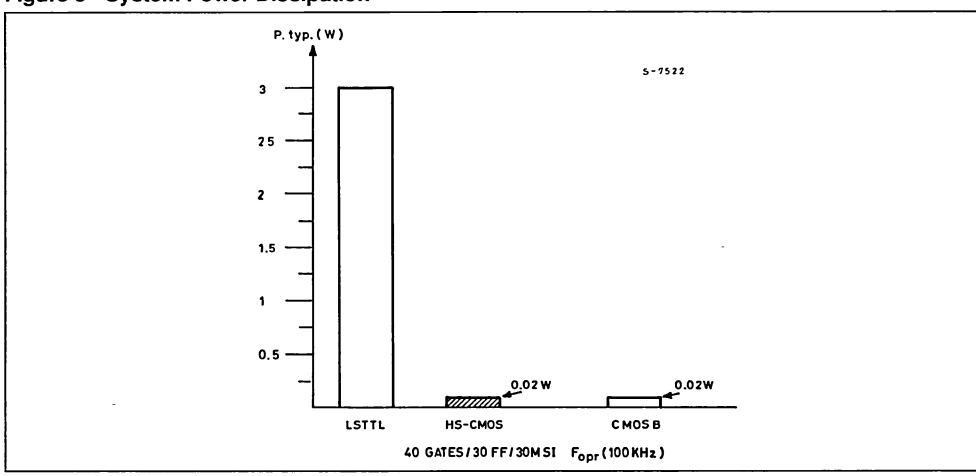


Figure 5 - System Power Dissipation



Wide Fanout

The output driving capabilities of LSTTL have been matched by the HS-C^{2}MOS family. Each device is able to sink or source up to 4 mA, in other words they can drive up to 10 LSTTL loads. Buffers and bus drivers have increased performance and can in fact drive up to 15 LSTTL loads. This has been achieved while maintaining the low input current, which is characteristic of CMOS, and without sacrificing either speed or noise immunity. Furthermore the design of the HS-C^{2}MOS devices has resulted in equal rise and fall times which results in easier design and allows optimum speed and AC performance to be obtained.

FANOUT FROM HS-C^{2}MOS TO CMOSB, LSTTL, TTL, STLL, ASLTTL

FROM \ TO	54/74HC	CMOSB	LSTTL	TTL	STLL	ALSTTL
54/74HC Standard	4000	4000	10	2	2	20
54/74HC Bus driver	> 4000	> 4000	15	4	3	30

Figure 6 - Output Driver Capability

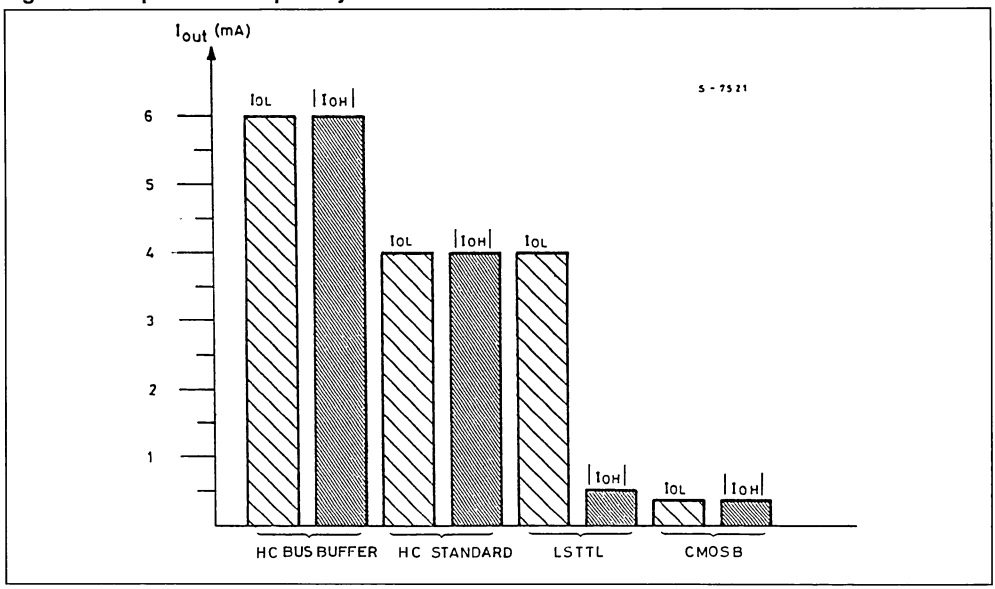
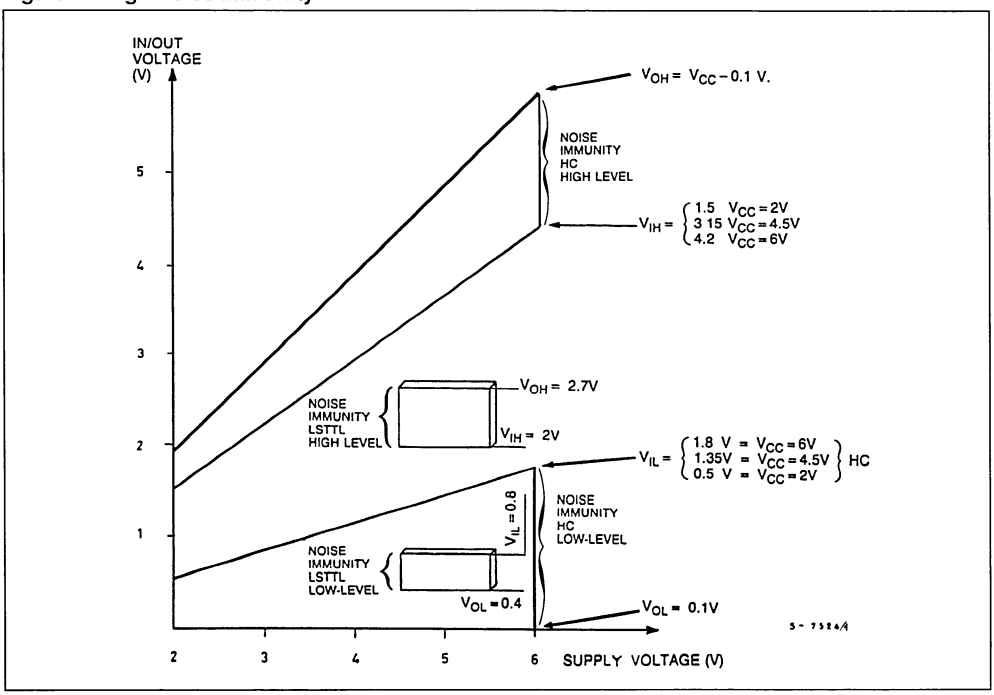


Figure 7 - High Noise Immunity



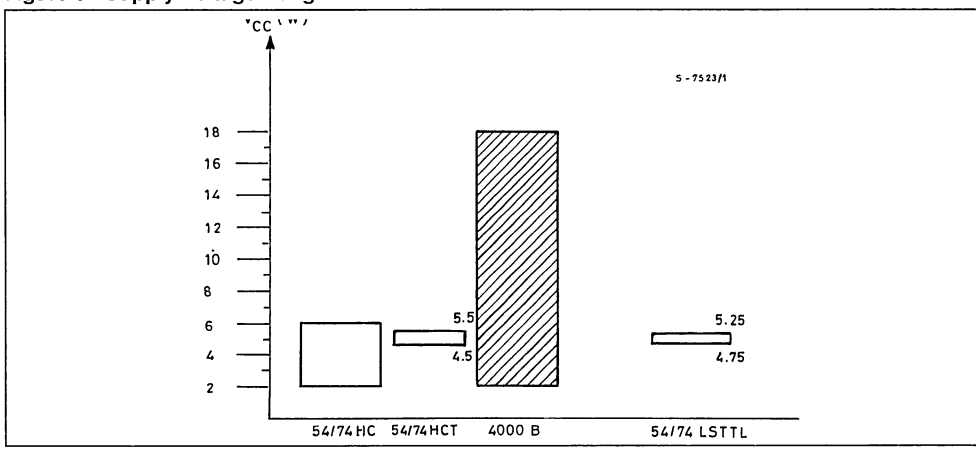
High Noise Immunity

In many applications high immunity to noise is of particular importance. This is why CMOS, with its characteristic high noise immunity, is already to be found in many computer peripherals, industrial circuits, telecommunications applications, and numerous other applications in high noise level environments. The LOW level and HIGH level noise immunity of the HS-C^{2}MOS family is better than 28% in both cases. This is notably better than for LSTTL where the margins are only 8% of V_{CC} at LOW level and 14% of V_{CC} at HIGH level. These figures assume a V_{CC} of 5 V, at higher voltages the superiority of HS-C^{2}MOS becomes even more apparent.

Wide Operating Voltage Range

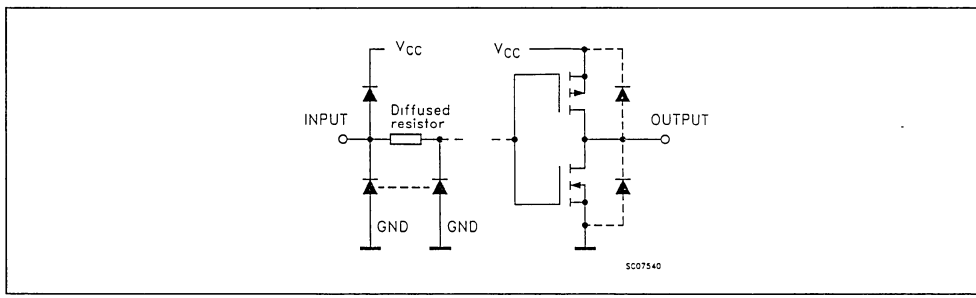
The HS-C^{2}MOS family devices are all capable of working with supply voltages ranging from 2 V up to 6 V. This is an important factor when viewed in the light of future developments, where the trend is towards memories and microprocessors which will work with supply voltages lower than 5 V. With the HS-C^{2}MOS family it is possible to use less precise, and therefore cheaper, power supplies or even low voltage batteries. This, coupled with the exceptionally low power consumption, common to the entire family, opens up the way for a whole new generation of light weight, high performance systems and instruments.

Figure 8 - Supply Voltage Range



Input Output Protection

The HS-C^{2}MOS, in addition to improved performance and power consumption, also feature improved input protection. This has been achieved by employing a resistor structure at all imputs. The resistor slows down the fast input transients generated by electrostatic discharge and dissipates some of the associated energy. Although these input resistors, in conjunction with the input diode, give improved levels of protection, it is still advisable to follow the usual CMOS handling precautions.



MAIN FEATURES OF THE HS-C^2 MOS SERIES

High Speed Operation	LSTTL speed f_{max} = 60 MHZ typical
Low Power Dissipation	Micro Watt Dissipation. Quiescent Current I_{CC} = 1μA SSI / 2 μA F/F / 4 μA MSI ; T_A = 25° C
High Output Current	Fanout of 10 LSTTL Loads (15 for buffers)
Symmetrical Output Buffer	Equal I_{OH} and I_{OL}
High Noise Immunity	$V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
Wide Operating Voltage Range	HC V_{CC} = 2 to 6 V HCT V_{CC} = 4.5 to 5.5V
Epitaxial Substrate to achieve Latch-up free operation.	
Protection networks on inputs and output pins guarantee >2KV ESD protection (class 2 MIL-STD-883D).	
Pin and Function Compatible with Equivalent LSTTL and Some Popular Types of HCC/HCF 4000 series.	
Wide Range of Products.	
Second Source Available.	

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	DC Input Voltage	– 0.5 to VCC + 0.5	V
V_O	DC Output Voltage	– 0.5 to VCC + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25 (± 35 buffer)	mA
I_{CC} or I_{GND}	DC VCC or Ground Current	± 50 (± 70 buffer)	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	– 65 to 150	°C

Absolute Maximum Rating are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≤ 65 °C derate to 300 mW by 10 mW/°C: 65 °C to 85 °C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
V_{CC}	Supply Voltage (HC)	2 to 6		V
V_{CC}	Supply Voltage (HCT)	4.5 to 5.5		V
V_I	Input Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	– 40 to 85 – 55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	ns
		V_{CC} = 6 V	0 to 400	ns

COMPARISON OF LOGIC FAMILIES

Parameter	Test Conditions	HC-C^2 MOS	LSTTL	CMOS B
Propagation Delay Time Gate (C_L = 15 pF)	VCC = 5 V	8 ns (typ)	10 ns (typ)	125 ns (typ)
Maximum Clock Frequency J/KF – F (C_L = 15 pF)	TA = 25 °C	60 MHz (typ)	45 MHz (typ)	7 MHz (typ)
Quiescent Power Dissipation (Gate)	Over all temperature and voltage range	0.01 µW (typ)	8 mW (typ)	0.01 µW (typ)
VIH VIL Noise Margin	V_{CC} = 5 V Over all temp. range	3.5 V (min) 1.5 V (max)	2 V (min) 0.8 V (max)	3.5 V (min) 1.5 V (max)
IOH IOL Output Current (Std.)	Over all temperature and voltage range	4 mA (min) 4 mA (min)	0.4 mA (min) 4 mA (min)	0.36 mA (min) 0.36 mA (min)
Operating Voltage Range		HCT 4.5 to 5.5V HC 2 to 6V	4.75 to 5.25 V	3 to 18 V
Operating Temperature Range	74HC/LS HCF 4000B 54HC/LS HCC 4000B	– 40 to 85 °C – 55 to 125 °C	0 to 70 °C – 55 to 125 °C	– 40 to 85 °C – 55 to 125 °C

THE HS-C^{2}MOS PROCESS

1. The Si-Gate Process

The M74HCXXX/54HCXXX family achieves its high speed operation, by means of an advance high performance Si-Gate process.
The advantages of Si-Gate versus metal gate CMOS are already well known and described. Here is a brief summary.

- The process uses self aligned source and draing diffusions which have the advantage of reducing gate to source and gate to drain overlap capacitance. This, in turn, reduces the Miller capacitance during the switching of the basic inverter which leads to an increase in speed.
- Better reliability: it has been proved that use of a silicon electrode as a gate of a MOS transistor gives better threshold voltage stability and therefore a more reliable basic structure under voltage stress.
- Recessed oxide isolation allows a thicker field oxide and therefore lower unit capacitance between interconnection and the grounded substrate. A decrease in the parasitic capacitance is therefore obtained and speed performance is improved.

2. The Scaling Theory

Despite its advantages, the use of a Si-Gate process instead of metal gate of equal dimensions is not sufficient to achieve speed performance comparable with LPS logic families.
Therfore a high performance Si-Gate process has been developed based on the "Scaling theory". The scaling theory of the physical dimensions of the transistor was developed originally by IBM (Dennard ed al.) in 1974.
Scaling is the step which has contributed most to the outstanding improvement in performance obtained by the MOS technologies in the last decade. This theory predicts that if the physical dimensions of a MOS transistor and the power supply voltage values are decreased by a constant factor K, and all the substrate doping level are increased by the same factor, the DC characteristics of the transistor remain unchanged.
The advantages of such an approach are quite straight forward

- the chip size is reduced by a factor K^2
- the delay times are reduced by a factor K^2

The Scaling theory is easy to explain, but it is much more difficult to obtain in a production enviroment because the progressive reduction of the physical dimensions put sever constaints on the type of equipment and on the spreads allowed in production control.

The recent improvement obtained by equipment manufactures in the field of photolithography and dry etching has been used extensively by ST to obtain a stable, reproducible production process, which is used in the production of all the devices in this new family.

3. The HS-C^{2}MOS Process

The following is a simplified description of the HS-C^{2}MOS process.
After initial oxidation of the starting material, which is N-type, windows are defined in the photoresist material and the initial oxide is removed (fig. 1). An implantation step is then performed (fig. 2) and after photoresist removal a diffusion step is carried out to define the P-well areas (fig. 3).

Figure 1 - Starting N-type with Windows in Oxide

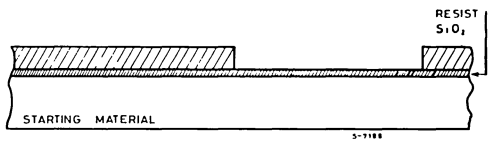


Figure 2 - P-Well Boron Implantation

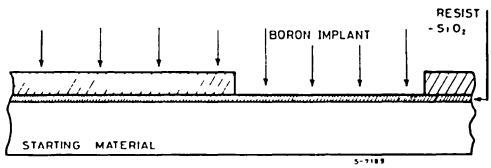


Figure 3 - P-Well Boron Redistribution

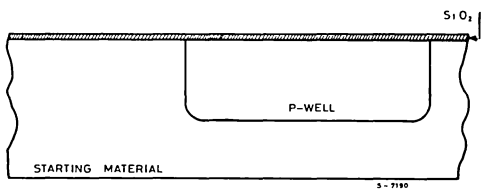


Figure 4 - Si3N4 Deposition

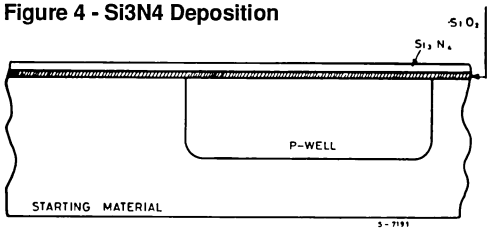


Figure 5 - Definition of Transistor Area

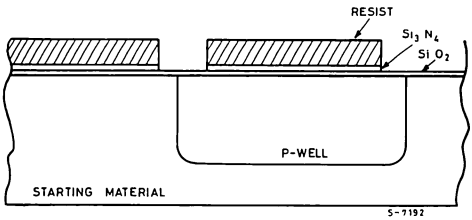
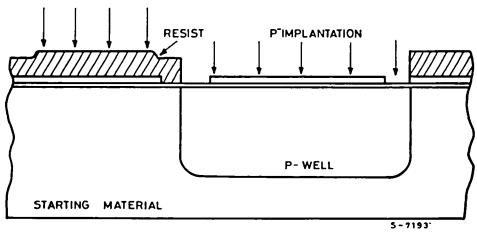


Figure 6 - P Implantation (Boron)



A-Silicon nitride layer is deposited on all the surface of the wafer (fig. 4) and by a masking step all the active areas (source, drain, gate) of both P-channel and N-channel transistors are defined (fig. 5).
The field threshold values are controlled by successive implantation steps both on the P-well surface (fig. 6) and substrate area (fig. 7).
After these steps the field oxide is grown (fig. 8). During the recessed oxidation step the diffusion of previous implanted dopants is effected.
After Gate oxidation, threshold voltage control of both the P-channel and the N-channel transistor is carried out using two successive masking steps. During these operations surface concentration of the gate areas is obtained to optimize the threshold voltage values against input noise and propagation delay time.
A crystalline silicon layer is deposited on all the surface of the wafer and then masked and etched to define the gates of all the transistors. (fig. 9).
Source and draing predeposition and diffusion of the N-channel transistors is the next step (fig. 10). The source and drain of the P-channel transistors are made, with an additional implantation step (fig. 11).

Contacts are defined and etched (fig. 12), an interconnection layer (metallization) is defined to interconnect all the active elements in the integrated circuits (fig. 13a, b).

Figure 7 - N Implantation Phospherais

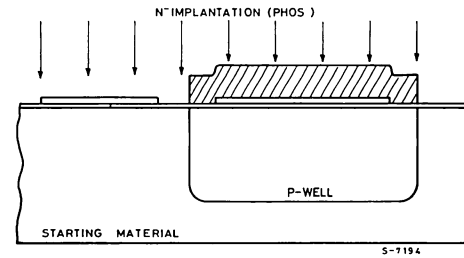


Figure 8 - Field Oxidation

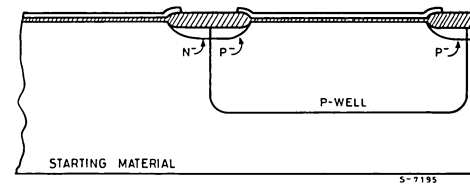


Figure 9 - Si Poly Gate Definition

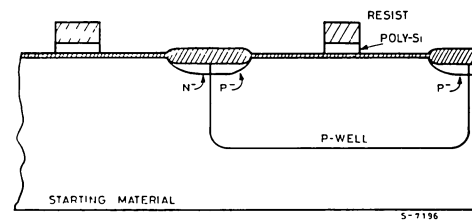


Figure 10 - N + Predeposition and Diffusion

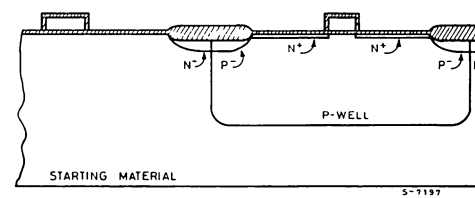


Figure 11 - P + Predeposition and Diffusion

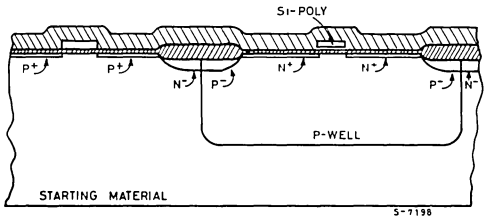


Figure 12 - Al-Si Deposition t_{Al-Si} = 7000 A

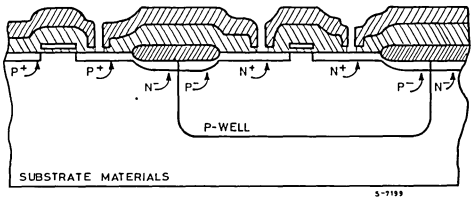


Figure 13a - Metal Interconnection

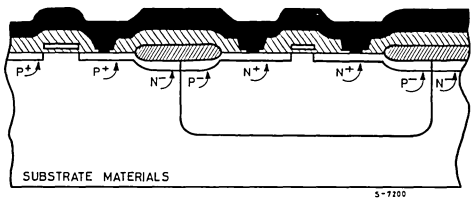
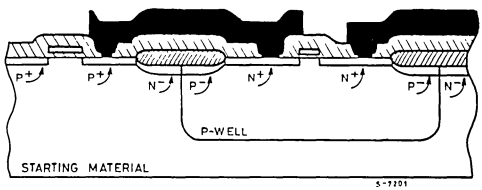


Figure 13b - Metal Interconnection Definition



Double Layer Glass Passivation

SGS-THOMSON HSCMOS family uses a double layer P-VAPOX and SI_3N_4 passivation that gives improved protection to die encapsulated in plastic packages.

Process Description

The process consists of a two layer film of P-Vapox (phosphorus doped silicon oxide) and Si_3N_4 (silicon nitride), obtained by two different masking and etching steps to avoid defects caused by lack of dielectric integrity.

The process gives good metal step coverage together with PECVD (Plasma Enhanced Chemical Vapox Deposition) to avoid cracking near metal edge and possible hillocks defects.

The double layer enables us, by means of an appropriate oversize, either at the boundaries of the die side or at the bonding pad side, to ensure full sealing of the underlying P-Vapox layer.

This prevents the layer from being exposed to moisture coming from the package. Thus the probability of metal corrosion on the bonding pad due to phosphoric acid is drastically reduced.

As a result the die is provided with a very good humidity immunity.

Process flow

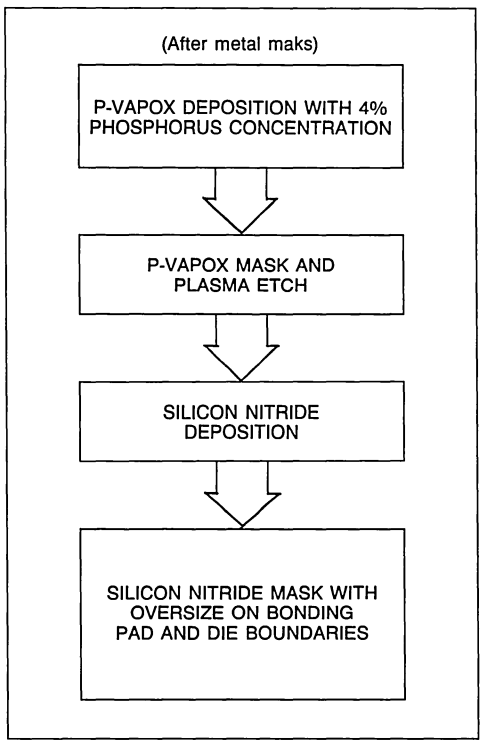


Figure 14a - Typical Microsection of an HSCMOS Device with Nitride Passivation

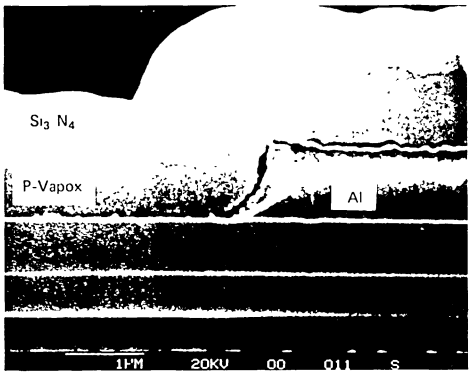


Figure 14b - Section Along the Scribing line of an HSCMOS Device

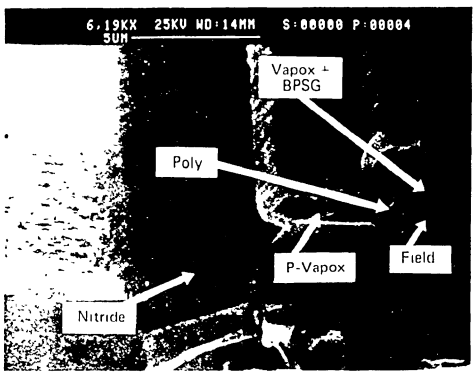
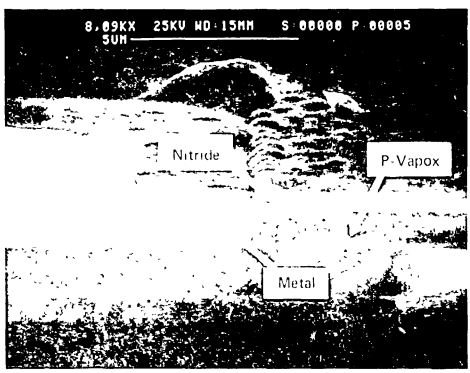


Figure 14c - Section Along the Pad of an HSCMOS Device

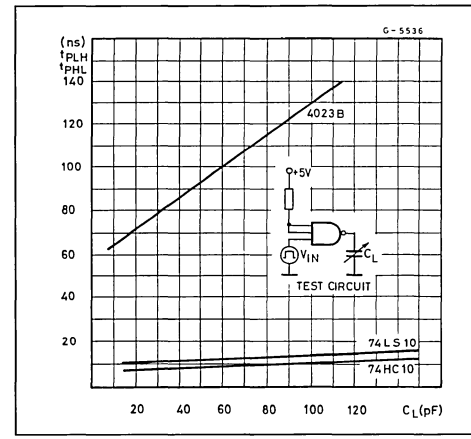


4. Summary

The scaling of the physical transistors combined with the Si-Gate process allows an outstanding improvement in the performance of the active elements and a drastic reduction of the parasitic capacitances.

Circuit performance at HSC^{2}MOS is comparable with LPS devices as shown in the following graph (fig. 15).

Figure 15 - Propagation delay vs. load Capacitance for 3-Input NAND Gate



INTERFACING TO HS-C²MOS LOGIC

In many applications it will be necessary to interface HC series logic devices with types from other logic families. Two main cases can easily be identified according to whether the supply voltage of the devices to be interfaced is different or not.
Where separate supplies are involved a logic level translator may be required. In most other cases only a very simple circuit, if any at all, will be required.

M54/74HC Driven by TTL

When interfacing TTL with HC devices using a common power supply of 4.5 to 5.5V, the guaranteed output-high voltage from TTL is only 2.4V. This is of course lower than the minimum input-high voltage for M54/74HC devices (see fig. 1).
Overcoming this problem is simply a matter of using an external pull-up resistor, Rp, which is the same as the resistor used for open collector output TTL. (See fig. 2).
Table 1 shows maximum and minimum values of Rp for various TTL families. When LSTTL is the driving logic, the value of Rp can be found using the graph shown in fig. 3.
Obviously the output-low level (0.8V) falls well within HC acceptable limits.
With HC devices supplied at more than 3V, the TTL minimum high voltage of 2.4V is enough to guarantee the logic 1 input.

Table 1

Rp min	74	74L	Unit
Rp min	390	1.5K	Ω
Rp max	4.7K	27K	Ω

M54/74HCT Driven by TTL

These devices, while retaining the intrinsic advantages of HS-C²MOS technology, allow direct interfacing with TTL devices.

Figure 2

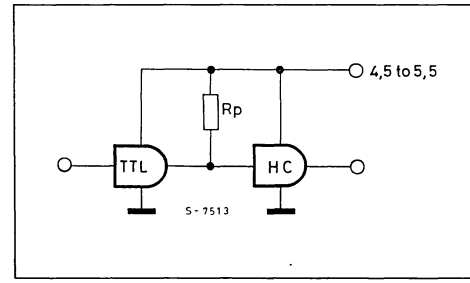


Figure 3

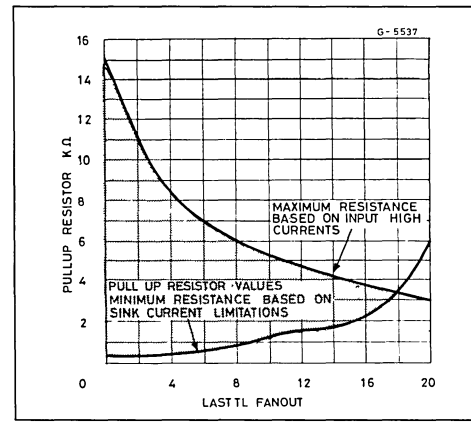
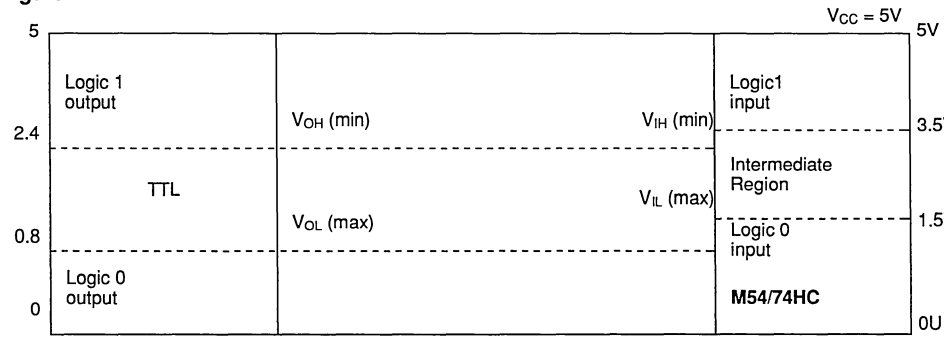


Figure 1



TTL Driven by M54/74HC

Given that HC devices have output-high levels close to VCC and output-low levels close to 0V, it is obvious that there are no difficulties in driving TTL devices which require 2V minimum input to guarantee a high level and 0.8V maximum input to guarantee a low level. Straightforward connection is therefore possible as is shown in fig. 4.
The output drive capability for M54/74HC devices is shown in table 2. This translates into a fan-out of 2 for TTL devices and 10 for LSTTL devices. In the case of bus drivers the fan-out is increased to 15 LSTTL loads.

Figure 4

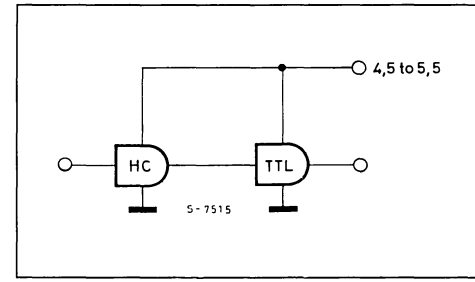


Table 2

	M54/74HC	TTL	LSTTL
I_{OH} (V_{OH} = 4.6V.) I_{OL} (V_{OL} = 0.4V.)	– 4mA 4mA		
I_{IH} (V_{IH} = 5.25V.) I_{IL} (V_{IL} = 0.4V.)		40µA max – 1.6mA max	20µA max – 0.4mA max

HS-C²MOS EQUIVALENT FAN-OUTS	LSTTL		TTL		S-TTL		ALS-TTL	
	Min.	Typ.	Min.	Typ.	Min.	Typ.	Min.	Typ.
STANDARD OUTPUTS	10	20	02	04	02	04	20	40
BUS DRIVERS OUTPUTS	15	30	04	08	03	06	30	60

Interfacing M54/74HC with NMOS/HMOS

The introduction of fast logic in C-MOS technology gy will allow the replacement of many bipolar devices currently used to support the majority of NMOS and HMOS LSI devices.
A pull-up resistor is required when HC devices are being driven from NMOS/HMOS devices since the minimum output-high level from NMOS/HMOS is only 2.4V and the minimum VIN to HC devices is 3.4V. (iF. VCC = 5V). Direct connection is possible when HC devices are driving NMOS/HMOS devices. An Example of an HC/NMOS system is shown in fig. 5.

M54/74HC Interfaced with CMOS LSI

Little need be said on this type of interface since both types of device can be supplied by the same voltage and have equivalent logic levels. Direct connection is therefore possible. An example of an HC/CMOS LSI system is shown in fig. 6.

Figure 5 - M4146 is 16384 x 1 Bit Dynamic Memory

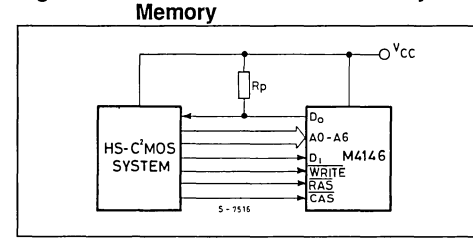
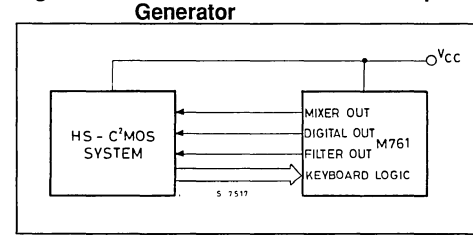


Figure 6 - M761 is Dual Tone Multifrequency Generator



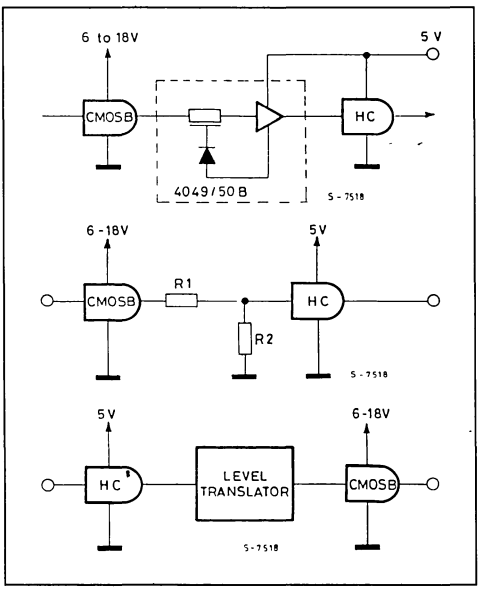
M54/74HC Interfaced with Standard CMOS B

When HC devices are to be connected to CMOSB devices, the level of supply voltage has to be taken into consideration. If the CMOSB supply is between 3 and 6 volts, direct interfacing is possible in both directions. When the supply is outside the HC range, level translators may be required. Fig. 7 shows possible connection configurations.

Interfacing HS-C MOS to ECL

Two of the many possible ways of interfacing between High Speed Logic and ECL logic are shown in fig. 8. In the first case level translators are used, while in the second case the HC logic is supplied by connecting V_{CC} to zero and the ground connection to –5.2V.

Figure 7



Unused Inputs

Unused Inputs should be connected either to + V_{CC} via a limiting resistor of between 100K and 1MΩ or directly to ground, depending on their logic function.

Handling Precautions

In addition to its high performance, HS-C^{2}MOS has improved input and output protection against electrostatic discharge and voltage transients. A resistor on the input is connected to two reverse biased diodes. Two reverse biased diodes are also included on the output as shown in fig. 9. The resistance limits input transients which are then eliminated by the two diodeds. The two diodes on the output carry out the same function.
Although HS-C^2 MOS includes improved protection it is still recommended that all the standard precautions for MOS devices are observed.

Figure 8

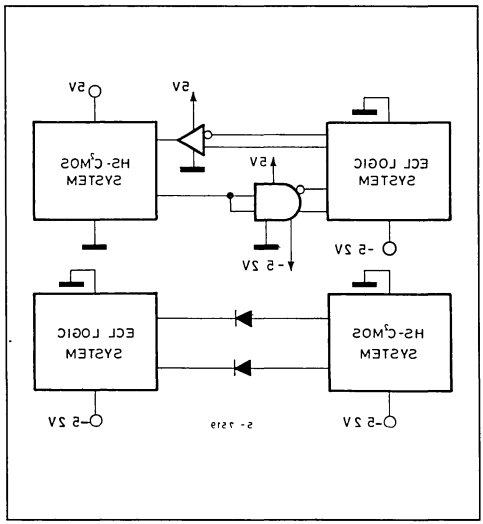
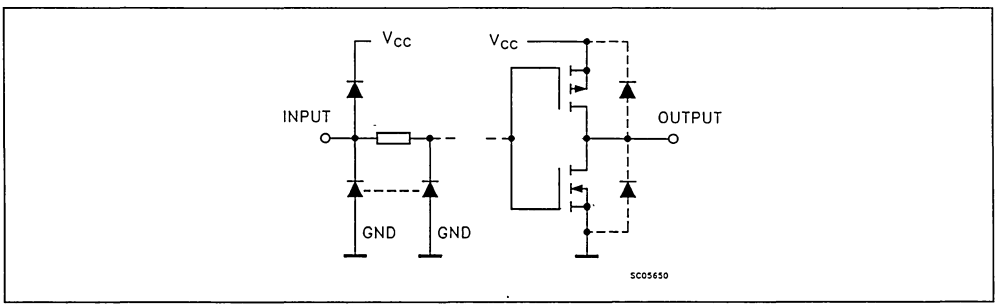


Figure 9



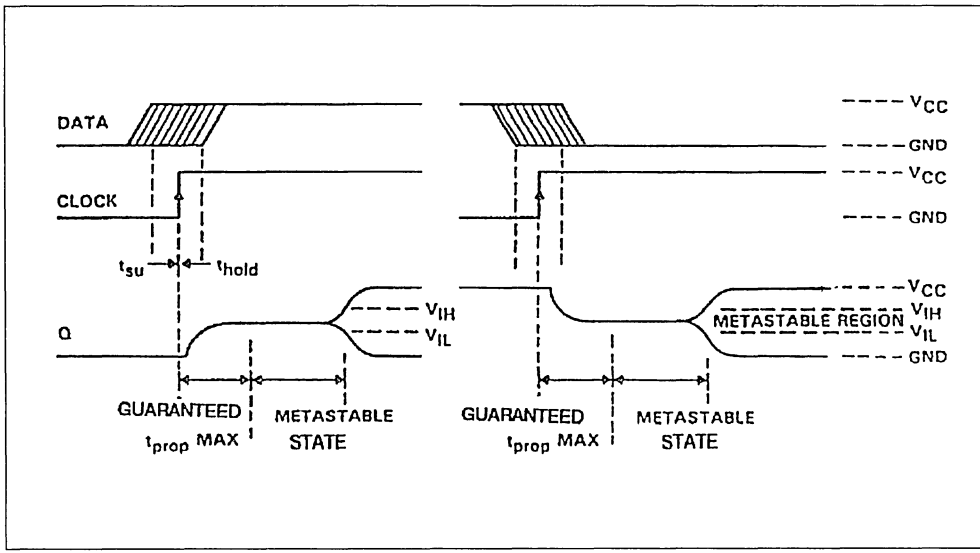
Metastable characteristic

When a setup, hold or recovery time is violated, the response of a flip-flop or a counter is uncertain. Reliable operation under this condition cannot be guaranteed, since there is the probability that the output locks in the metastable region for a certain period.

The metastable state is defined as that time period in which the output level is not at logic "0" nor at logic "1", but stays in the region between VIL and VIH.

This is illustrated in the following waveforms:

Figure 10. Metastable Timing Diagram



LOGICIEC SYMBOL EXPLANATION

1. General Explanation

The logic symbology considered follows the system established by the INTERNATIONAL ELECTRO-TECHNICAL COMMISSION (IEC).
IEC symbols show the relationship between every input and output of digital circuits.
In the symbols of more complex functions, use is made of "the dependency notation" that specifies the interrelationships of digital inputs/outputs. The fig. 1 shows the symbol composition.

The preferred direction of signal flow is from left to right; inputs are on the left and outputs are on the right. Arrows on the signal lines indicate exceptions to this convention.
Adjacent elements in a composite symbol may be joined by a common boundry.
A common control block can be used, as shown in fig. 2, when a composite symbol contains at least one input common to one or more of the elements.

Figure 1

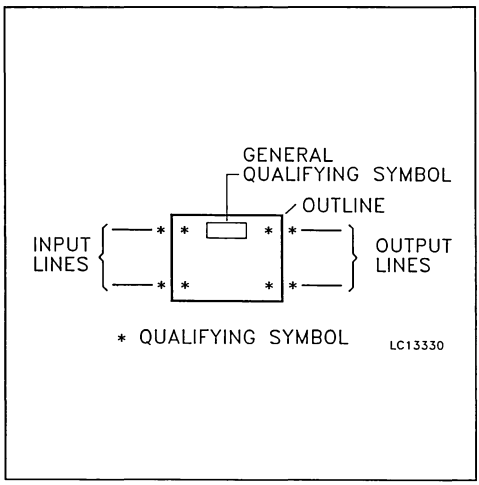
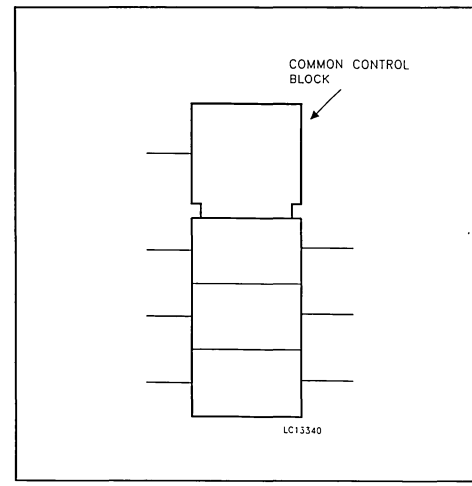


Figure 2

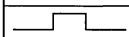
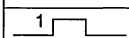
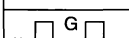
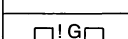
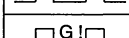
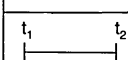


2. General Qualifyng Symbols

General qualifyng symbols feature the logic function of the element as shown in Table 1.

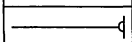
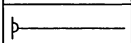
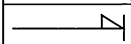
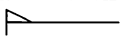
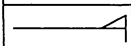
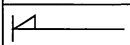
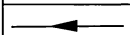
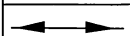
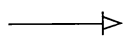
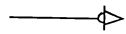
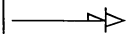
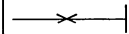
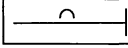
Table 1

Symbol	Definition
&	AND element
≥ 1	OR element
= 1	EXCLUSIVE OR element
=	Logic identify element. If all inputs have the same logic state then the output is at internal logic "1".
2K	Even element. If an even number of inputs are at internal logic "1" then the output is at internal logic "1".
2K + 1	Odd element. If an odd number of inputs are at internal logic "1" then the output is at internal logic "1".
1	Buffer element without amplified output.
	Buffer element with amplified output. The triangle points in the direction of signal flow.

Symbol	Definition
	Schmitt–trigger. It has hysterisis characteristic.
	Retriggerable monostable element.
	Non–Retriggerable monostable element.
	Astable element
	Synchronous–starting astable element.
	Synchronous–stopping astable element.
SRGm	Shift Register. "m" :numer of bits.
CTRm	Binary counter. "m" :number of bits. cycle legth: 2
CTRDIVm	Counter with cycle legth m.
RCTRm	Ripple carry counter. "m" :number of bits. cycle legth: 2
X / Y	Coder or code converter. X and Y may be replaced by appropriate indications of the codes used.
MUX	Multiplexer / data selector.
DMUX or DX	Demultiplexer.
Σ	Adder.
P – Q	Subtractor.
CPG	Look–ahead carry generator.
π	Multiplier.
COMP	Comparator.
ALU	Arithmetic logic unit.
ROM	Read only memory.
RAM	Random access memory.
FIFO	First–in First–out memory.
I = 0	When power is switched ON, the element goes to internal logic "0".
I = 1	When power is switched ON, the element goes to internal logic "1".
	Delay element with specified delay times.

3. Qualifyng Symbols for Inputs and Outputs. Symbols considered are used as shown in table 2. It should be noted that if the same symbols, general or related inputs/outputs, appear inside each element of an array, they are usually shown only in the first one.

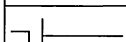
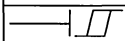
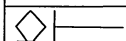
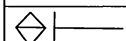
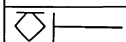
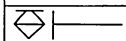
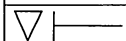
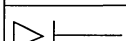
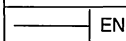
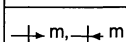
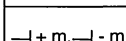
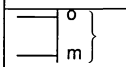
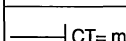
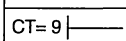
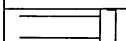
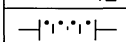
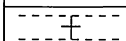
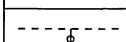
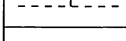
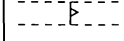
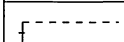
Table 2

Symbol	Definition
	Logic negation at an input. An external logic "0" ("1") produces an internal logic "1" ("0").
	Logic negation at an output. An internal logic "0" ("1") produces an external logic "1" ("0").
	Polarity indicator at an input. A "L" (Low) level active.
	Polarity indicator at an output. A "L" level active.
	Polarity indicator at an input where the signal flow is from right to left.
	Polarity indicator at an output where the signal flow is from right to left.
	Indicator for direction of signal flow.
	Bidirection information flow (alternate).
	Dynamic input Positive logic. 0 → 1 Negative logic. 1 → 0 Polarity indicate. L → H The above transitions produce the internal logic active.
	Dynamic input Positive logic. 1 → 0 Negative logic. 0 → 1 The above transitions produce the internal logic active.
	Dynamic input Polarity indicate. H → L The above transitions produce the internal logic active.
	Non–logic connection.
	Input for analog signals.

4. Symbols Inside the Outline

Table 3 shows the symbols used within the symbol outline.

Table 3

Symbol	Definition
	Delayed output. The output change is delayed until the input that indicated the change returns to its initial external state or level.
	Schmitt trigger input.
	Open–drain output without internal pulled–up resistor.
	Open–drain output with internal pulled-up resistor.
	Open–source output without internal pulled–down resistor.
	Open–source output with internal pulled–down resistor.
	Three state output.
	Buffered output. (The triangle points in the direction of signal flow)
	Enable input.
J, K, D	Information inputs of disable elements.
R, S, T, C	Control inputs of disable elements.
	Shift input. The direction of shift is to the right or down when the arrow points to the right, or to the left. "m" = 1,2,3, ..., however, the number may be omitted when "m" = 1.
	Counting input. Count–up or count–down are indicated by + and – respectively. The number "m" is the count per command and may be omitted when "m" = 1.
	Bit–grouping symbol. "m" is the highest power of 2 in the group.
	Content input. The internal logic "1" sets the element to the value "m".
	Content output. For example, when the input state is "1", the internal registor sets "7".
	Line–grouping symbol. The inputs enclosed by this symbol from a single logic input.
	Fixed–mode input, Fixed–state output. This input (output) is parmanently at internal logic "1".
	A logic "1" at the left–hand side produces a logic "0" at the right–hand side.
	Negated internal connection. A logic "1" at the left–hand side produces a logic "0" at the right–hand side.
	Dynamic internal connection. A transition from internal logic "0" to internal logic "1" at the left–hand side produces a transistory logic "1" at the right–hand side.
	Internal input (virtual). This input is always at internal logic "1" state unless this is overridden or modified.
	Internal output (virtual). This effect on the internal input connected to this output must be indicated by dependency notation.

5. Dependency Notation

Dependency notation makes IEC Logic Symbols compact yet meaningful; the relationship between inputs and outputs are illustrated without needing to show all the elements and interconnections involved, as shown in explanation example of fig. 3.

In dependency notation the terms "affecting" and "affected" are used.

The input (or output) affecting other inputs (or outputs) is labelled with the letter symbol that indicates the relationship involved, followed by an appropriately chosen identifyng number.

Each input (or output) affected by that affecting input (or output) is labelled with the same number.

If the affected input or output has a label to denote its function, this label will have the identifying number of the affecting input as a prefix.

If the labels denoting the function of affected inputs or outputs are numbers, the identifying number of both affecting inputs and affected inputs or outputs is replaced by another character (greek letter).

If it is the complement of the input's (or output's) internal logic state that does the affecting, a bar is placed over the identifying numbers at the affected inputs or outputs.

If two affecting inputs or outputs have the same letter and the same identifying number, they are ORed together.

If an input or output is affected by more than one affecting input, each identifying number separated by a comma will appear in the label of the affected one. The normal reading order of these numbers is the same as the sequence of the affecting relationship.

Symbol for dependency notation are shown in table 4.

Figure 3

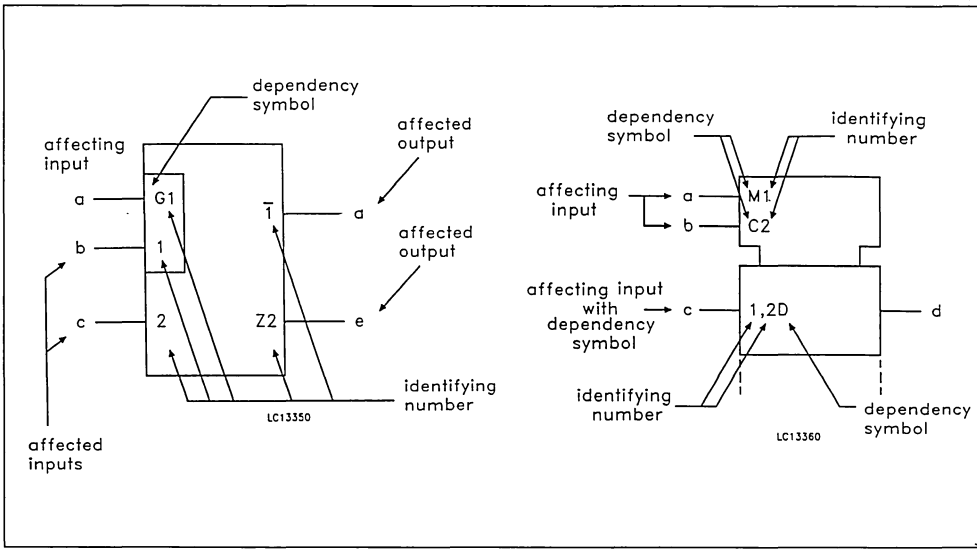
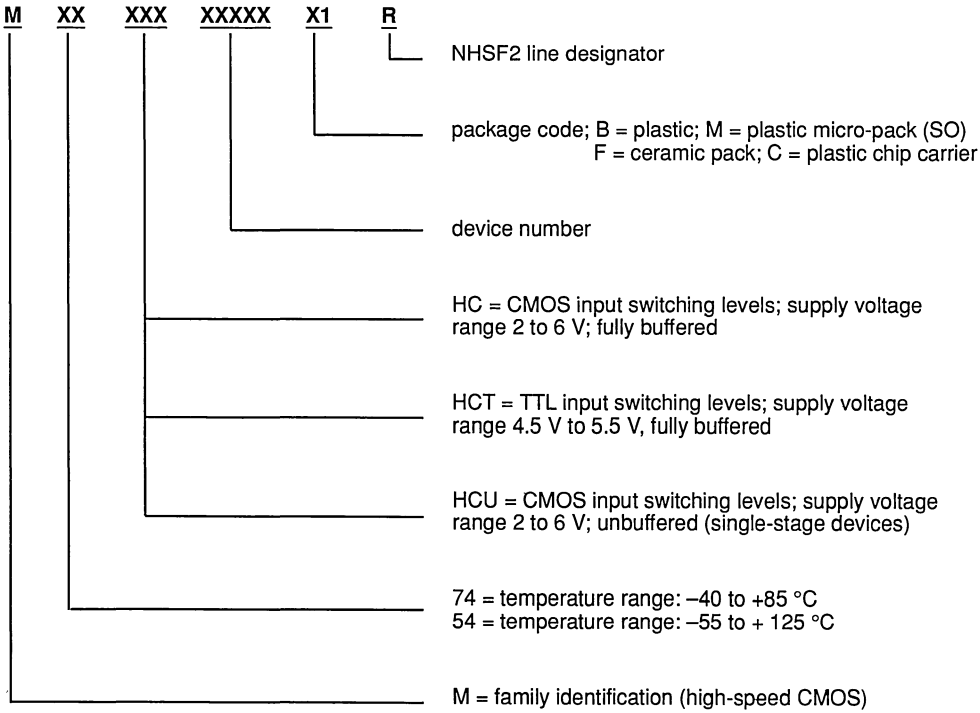


Table 4

Type of dependecy	Letter symbol	Affecting input at logic "1"	Affecting input at logic "0"
address	A	permits action (address selected)	prevents action (address not selected)
control	C	permits action	prevents action
enable	EN	permits action	prevents action of inputs; open outpus OFF; ∇ outputs at external high impedance, no change in internal logic state; outputs high performance "H" level; outputs high impedance "L" level; other outputs at internal "0" state
AND	G	permits action	imposes "0" state
mode	M	permits action (mode selected)	prevents action (mode not selected)
negate (EXCLUSIVE OR)	N	complements state	no effect
reset	R	affected output reacts as it would to S = "0", R = "1"	no effect
set	S	affected output reacts as it would to S = "1", R = "0"	no effect
OR	V	imposes "1" state	permits action
interconnection	Z	imposes "1" state	permits action

TYPE NUMBER DESCRIPTION



RELIABILITY REPORT

THE PRODUCT TECHNOLOGY

The sharp improvement in performance of the 74HC family, in comparison to the standard 4000B family, is mainly due to the 1980's technological progress, and to a systematic layout philosophy, high-speed-oriented.
The fabrication process exploits

- dieletric isolation:
  for higher density and lower parasitic capacitances (speed)
- photolitography scaling down
- tighter doping process control
- silicon gate technology

Even if some of these steps are well known to the semiconductor industry, their unique combination into an effective and reliable process is the key to the 74HC family success.
These circuits are typically employed in professional applications where quality and reliability are a major feature of the set.
A "no compromise" strategy is adopted at each stage of production from development to preproduction, to full production stage; quality and reliability are always priority targets.

We have envisaged 3 main check points:
1) Project validation at design stage
2) Prototypes qualification
3) Final product qualification

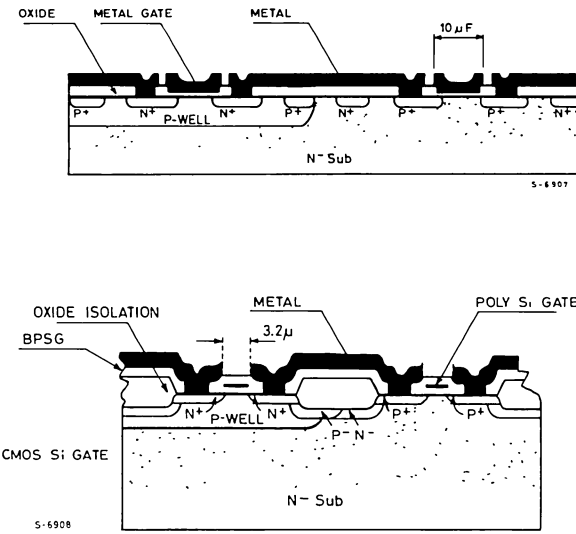
At design stage CAD tools (for simulation and design rules check) and quality council meeting are used for continuous monitoring of quality aspects of the circuits.
Qualification of the prototypes is performed by means of an agreed and fixed set of tests for reliability and product characterisation.

The final outputs are
a) Circuit characterisation manual
b) Circuit qualification report
c) Failure analysis reports (when needed)

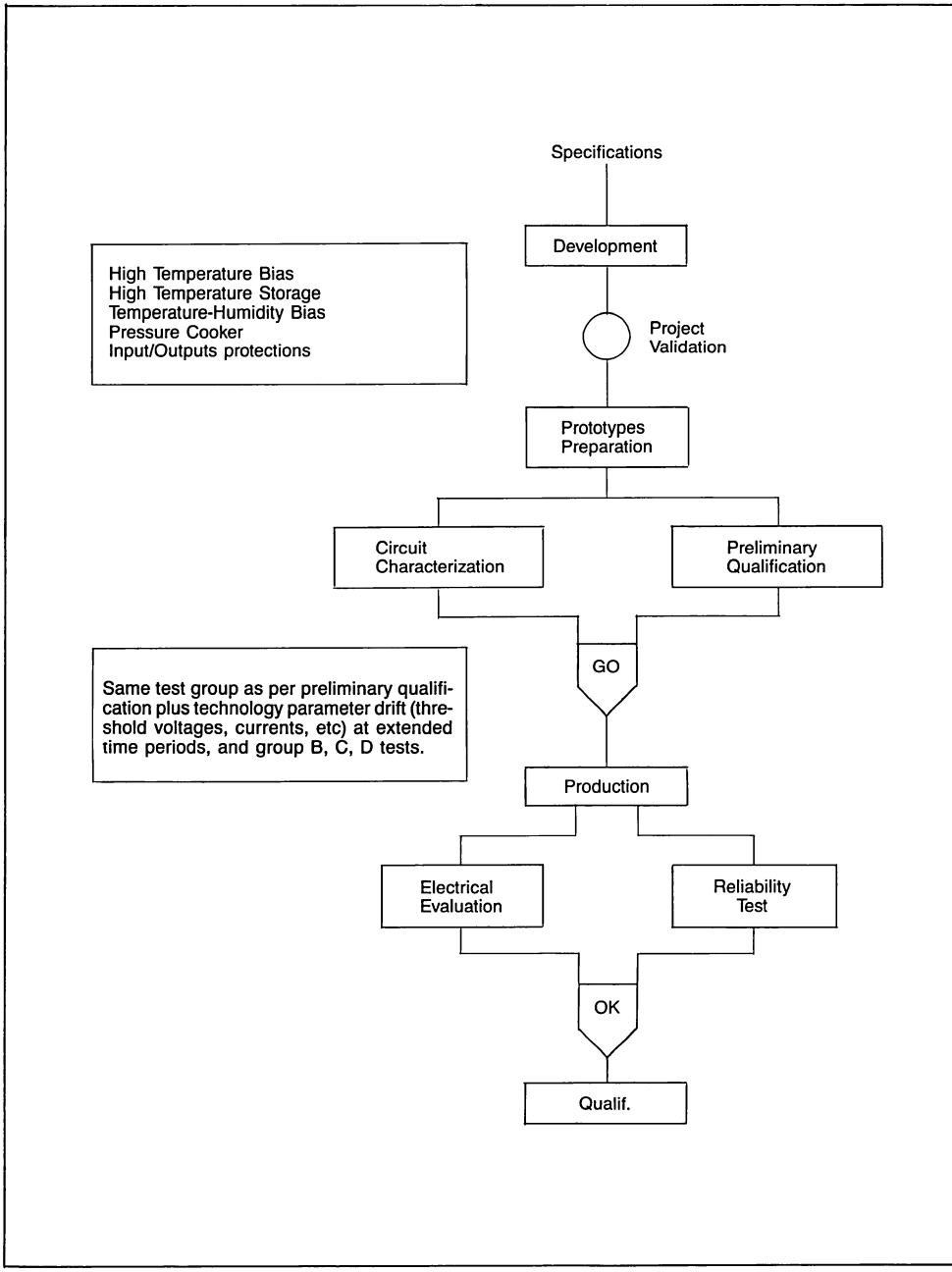
See next page for operative data and flow.

Finally product qualification at production stage is obtained with a set of reliability tests mainly based upon
d) Accelerated temperature life test
e) High temperature storage
f) Temperature-humidity accelerated conditions
g) High voltage stresses (inputs-outputs protection, latch-up)

Both circuit and process parameters are monitored.



PRODUCT QUALIFICATION FLOW CHART



DOUBLE LAYER GLASS PASSIVATION

SGS-THOMSON HSCMOS family uses a double layer P-VAPOX and Si_3N_4 passivation that gives improved protection to die encapsulated in plastic packages.

PROCESS DESCRIPTION

The process consists of a two layer film of P-Vapox (phosphorus doped silicon oxide) and Si_3N_4 (silicon nitride), obtained by two different masking and etching steps to avoid defects caused by lack of dielectric integrity.

The process gives good metal step coverage together with PECVD (Plasma Enhanced Chemical Vapox Deposition) to avoid cracking near metal edge and possible hillocks defects.

The double layer enable us, by means of an appropriate oversize either at the boundaries of the die side or at the bonding pad side, to ensure full sealing of the underlying P-Vapox layer.

This prevents the layer from being exposed to moisture coming from the package. Thus the probability of metal corrosion on the bonding pad due to phosphoric acid is drastically reduced.

As a result the die is provided with a very good humidity immunity.

PROCESS FLOW

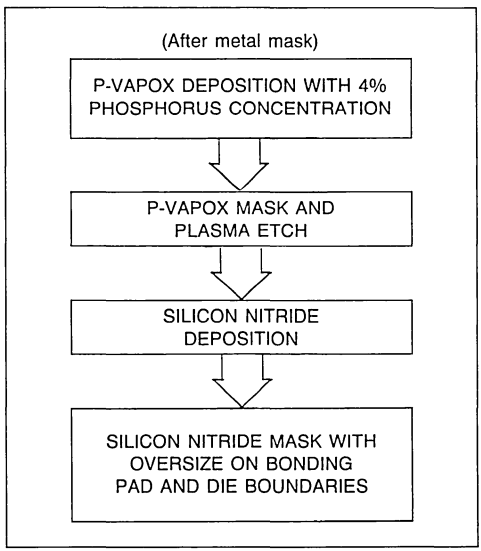


Figure 1 - Typical microsection of an HSCMOS device with nitride passivation.

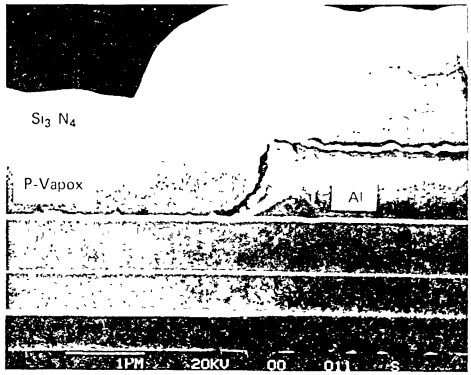


Figure 2 - Section along the scribing line of an HSCMOS device.

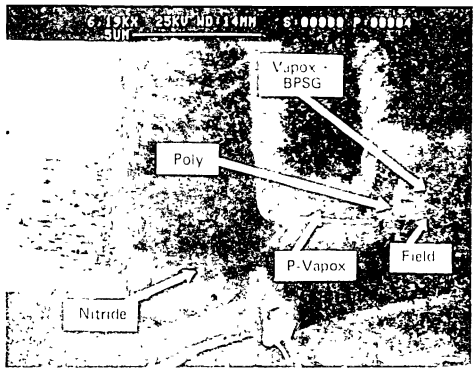
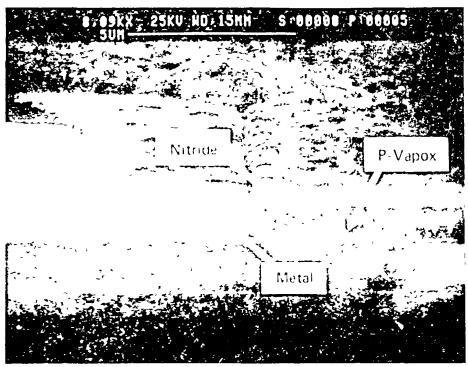


Figure 3 - Section along the Pad of an HSCMOS device.



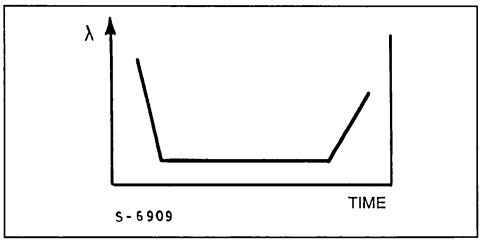
RELIABILITY AND FAILURE MECHANISMS

FUNDAMENTALS

-Through accelerated stresses we ascertain the value of the components failure rates, in terms of how many devices (in percent) are expected to fail every 1000 hours of operation (λ or F.R.)

-Failure rate versus time of activity shows the well-known trend.

-Failure rate



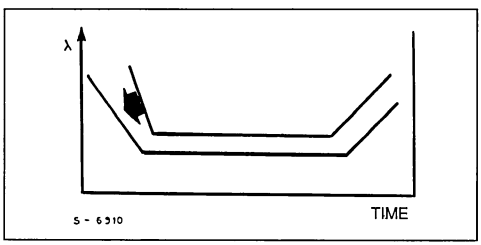
During the first time period the products are affected by the so-called "infant mortality" intrinsic to all semiconductor technologies. End users are very sensitive to this parameter which causes early operational failures in their equipment.

TARGETS

SGS-THOMSON periodically reviews and publishes lifetime results; at this time a new set of failure rate targets are being defined. These targets are translated into actual required test hours.

The goal is a steady shift of the limits.

Failure rate λ



TESTS

With accelerated tests we define the failure rate of the products, then, derating the data for different conditions, we know the life expectancy under the actual operating conditions.

In its simplest form the failure rate (at a given temperature) is:

$$F.R. = \frac{N}{D \cdot H} \qquad (1)$$

Where N = Number of failures
D = Number of components
H = Number of testing hours

If we intend to determine the failure rate at other temperatures an acceleration factor must be considered.
Some tests are accelerated by means of increased temperature, based on the assumption of the Arrhenius law:

$$F.R. = Ae^{-Ea/KTj} \qquad (2)$$

A = Constant

Ea = Activation energy

K = Boltzman's constant

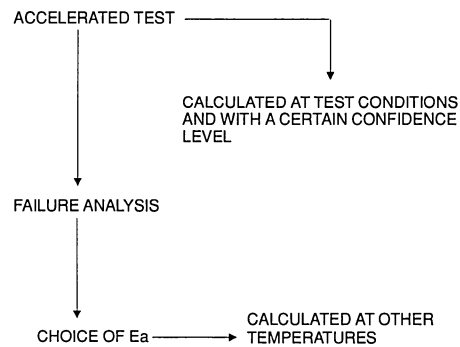
Tj = Junction Absolute temperature

For two different temp. $F.R.(T_1)=F(T_1, T_2)F.R.(T_2)$

from (2) it is: $F(T_1,T_2) \equiv EXP\left[\frac{-Ea}{K}\left(\frac{1}{T_1}-\frac{1}{T_2}\right)\right]$ (3)

Clearly the choice of an appropriate activation energy, Ea is of paramount importance.
The different mechanisms which could lead to circuit failure are characterized by specific activation energies whose values are published in the relevant literature.

THUS THE CORRECT PROCEDURE IS



Arrhenius equation (2) describes the rate of many processes responsible for degradation and failure of electronic components; it follows that if the transition of an item from an initial stable condition to a defined degraded state occurs by a thermally activated mechanism, then the time for the transition is given by an equation of the form:

MTBF = B EXP (Ea/Kt)

MTBF = Mean time between failure

B = Temperature-independent constant

MTBF can be defined as the time to suffer a device degradation. The dramatic effect of the choice of the Ea value can be seen by plotting equation (2).

The acceleration effect of a 125°C device junction test with respect to 70°C actual device junction operation is equal to a factor of 100 for Ea = 1eV and respectively 4 for Ea = 0.3eV.

Some words of caution are needed about published values of Ea:

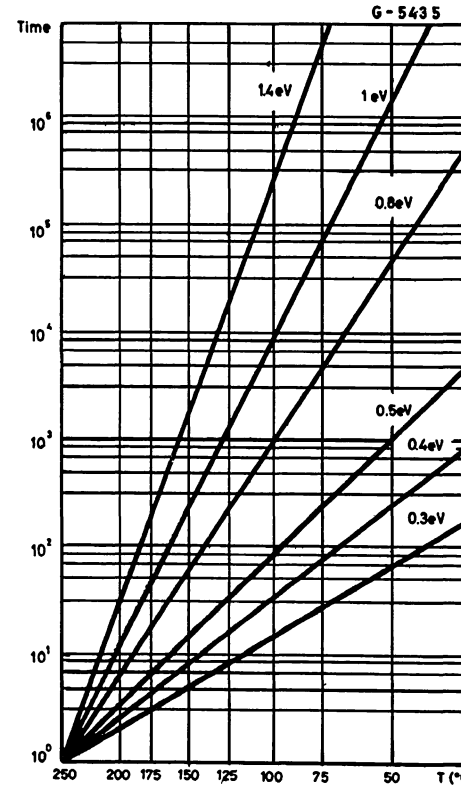
A)They are often related to high temperature test where a single Ea (with high value) mechanism has become significant.

B)They are specifically related to the devices produced by that supplier (and to its technology) and in that period of time.

C)They could be modified by the mutual action of other stresses (voltage, mechanical)

D)Field device-application conditions should be considered.

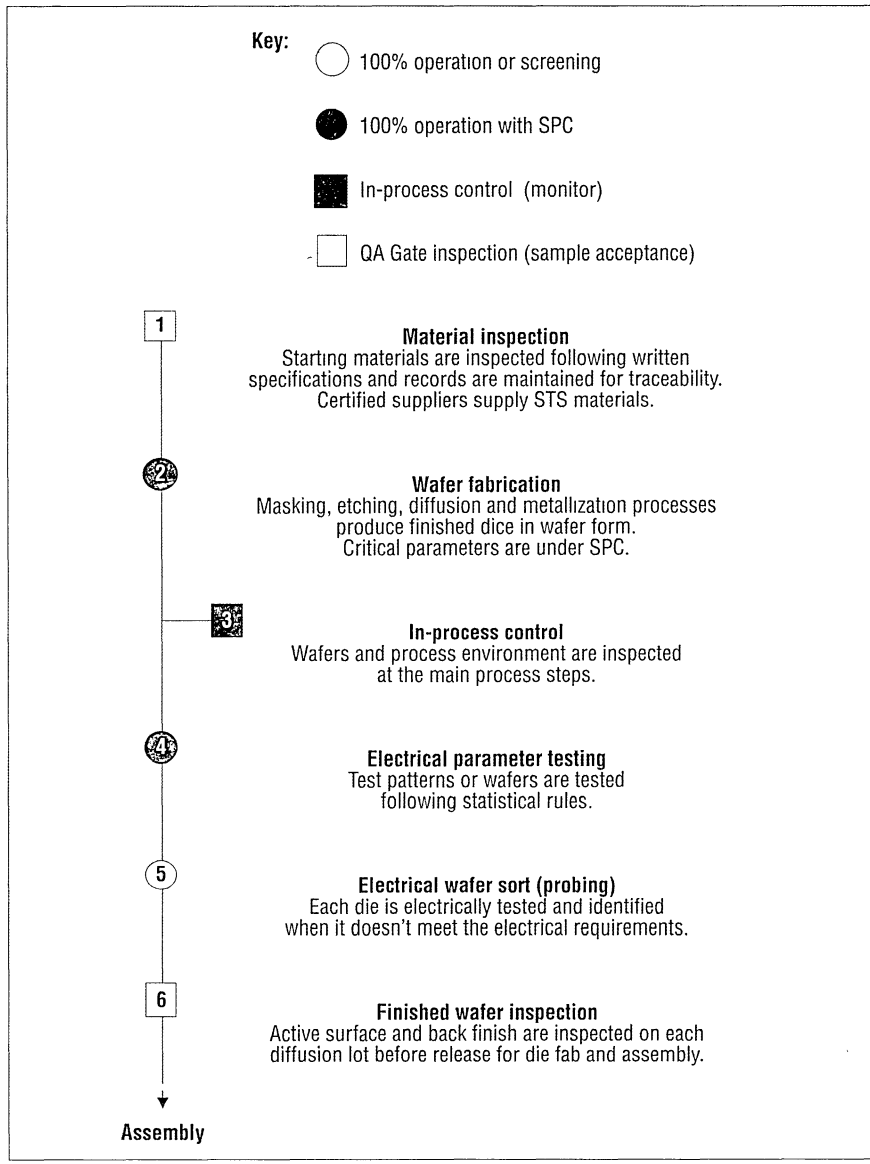
Life-Hours



Main Failure modes and relevant activation energies

Failure Mode	Activation Energy (eV)	Accelerating
SURFACE CHARGE	1.0 - 1.05	HIGH TEMPERATURE BIAS
IONIC CONTAMINATION	1.0 - 1.4	HIGH TEMPERATURE BIAS
DIELECTRIC DEFECTS	0.3 - 0.6	HIGH TEMPERATURE BIAS
ELECTROMIGRATION	0.5 - 1.2	HIGH TEMPERATURE BIAS
INTERMETALLIC GROWTH	1.0 - 1.05	HIGH TEMPERATURE BIAS, STORAGE
METAL CORROSION	0.3 - 0.8	HIGH HUMIDITY BIAS

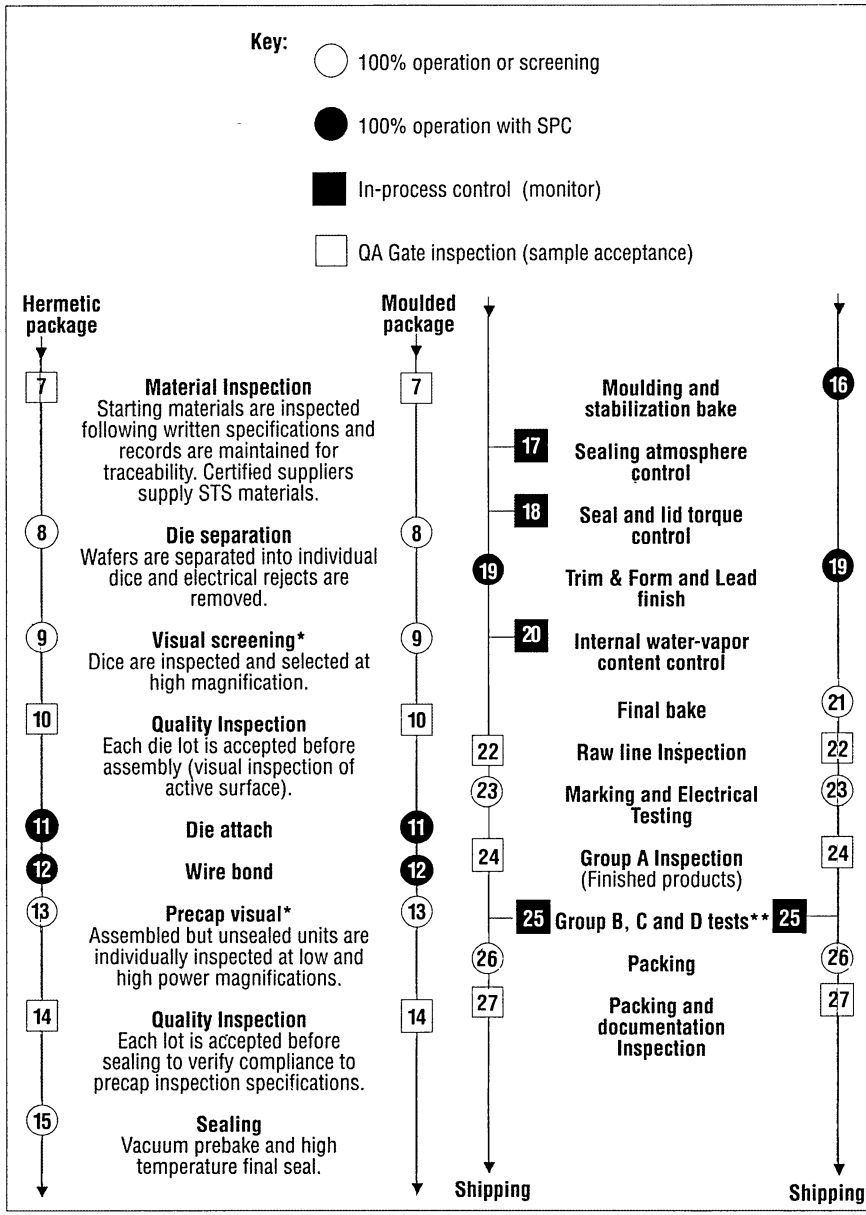
WAFER FAB TYPICAL PRODUCTION PROCESS FLOW CHART



In-process control during wafer fabrication
The table emphasizes the most important fabrication steps with the relevant SPC measures and/or monitors performed.

PROCESS STEPS	IN-PROCESS INSPECTIONS/MONITORS
OXIDATION	– Visual – Thickness – Refractive Index – CV plot (stability of ionic concentration and contamination control)
DEPOSITION: Nitride, Poly Si	– Visual – Thickness – Refractive index – Doping content
PHOTOLITHOGRAPHY	– Mask and wafer cleanliness – Alignment and focusing accuracy – Critical dimensions
ETCHING	– Quality of etching and wafer cleanliness – Critical dimensions
DOPING BY IMPLANT (P, As, B)	– Sheet resistance (dose and implant uniformity)
DOPING BY DIFFUSION ($POCl_3$, As)	– Sheet resistance – Thickness – CV plot (stability of ionic concentration and contamination control)
EPITAXIAL GROWTH	– Thickness – Resistivity – Crystal quality (stacking faults, bumps and others)
METALLIZATION	– Wafer cleanliness – Visual – SEM (step coverage and film quality) – Thickness – CV plot (stability of ionic concentration and contamination control)
INTERMEDIATE AND FINAL PASSIVATION	– Thickness – Doping content – Passivation integrity (density of pinholes and cracks) – Visual
BACK FINISHING	– Wafer thickness – Back metal thickness – Metal adherence
ELECTRICAL CHARACTERIZATION	– Main parameters for active and parasitic structures (e. g. threshold voltage, saturation current, h_{FE}, resistances, capacitances ...)
WAFER INSPECTION	– Visual (microscope and/or laser surface inspection system)
ALL DEPOSITIONS AND PHOTOLITHOGRAPHY	– Surface Scan (to detect and to measure foreign particles)

ASSEMBLY TYPICAL PRODUCTION PROCESS FLOW CHART



* Omitted when the intrinsic quality meets the specified quality level

** For non military products, these reliability tests can be performed after step 23 on 100% electrically tested samples (when requested)

In-process control during assembly process

The table emphasizes the most important fabrication steps with the relevant SPC measures and/or monitors performed.

PROCESS STEPS	TESTS	DESCRIPTION
11	DIE ATTACH	–Integrated Circuits MIL-STD-883 Method 2010 cond B (internal visual) and Method 2019 (die shear strength); CECC 90000
12	WIRE BOND	– Integrated Circuits MIL-STD-883 Method 2010 cond. B (internal visual) and Method 2011 cond. D (bond strength); CECC 90000
14	QUALITY INSPECTION	– Integrated Circuits MIL-STD-883 Methods 2010 cond. B (internal visual); CECC 90000
16	MOULDING AND STABILIZATION BAKE	– Visual and temperature process control
17	SEALING ATMOSPHERE CONTROL	Moisture content: < 200 ppm for Ceramic packages
18	SEAL CONTROL	Fine Leak – Integrated Circuits MIL-STD-883 Method 1014 cond. A1 Helium leak detector after pressurization in He for: 2h at 5.1 atm Limit: 5×10^{-8} cc/s for ICV < 0.05 cc 4h at 5.1 atm Limit: 5×10^{-8} cc/s for ICV ≥ 0.05 < 0.5 cc 2h at 3.0 atm Limit: 1×10^{-7} cc/s for ICV ≥ 0.5 < 1cc 5h at 3.0 atm Limit: 5×10^{-8} cc/s for ICV ≥ 1 < 10cc ICV = Internal Cavity Volume Gross Leak – Integrated Circuits MIL-STD-883 Method 1014 cond. C1 (fluorocarbon gross leak) 5 Torr vacuum for 30 minutes minimum followed by pressurization of the devices immersed in mineral oil and subsequent immersion in another mineral oil at Ta = 125°C

In-process control during assembly process (cont'd)

PROCESS STEPS	TESTS	DESCRIPTION
18 (cont.d)	LID TORQUE CONTROL	Ceramic packages only MIL-STD-883 Method 2024 (e.g. ≥ 60 Kg x cm for seal area values between 1.41 and 1.73 cm^2)
19	TRIM & FORM AND LEAD FINISH	– Dimensions, thickness and contamination control – Solderability control: Aging as per page 51 215 ± 5°C for 3 ± 0.5 sec. (SMD only) 235 ± 5°C for 2 ± 0.5 sec. 245 ± 5°C for 5 ± 0.5 sec.
20	INTERNAL WATER VAPOR CONTENT CONTROL	Dew Point method MIL-STD-883 Method 1018 procedure 3 5000 ppm max (dew point temperature less than - 15°C) Ceramic packages only
21	FINAL BAKE	For SMD only (according to internal specifications)
22	RAW LINE INSPECTION	External Visual – Integrated Circuits MIL-STD-883 Method 2009; CECC 90000 Note: at this step some reliability tests (pressure pot, temperature cycling, life test etc.) are performed as a monitor, generally on a weekly basis, to have fast feedback on process behaviour (Real Time Control Tests)
24	GROUP A INSPECTION	See page 87
25	GROUPS B, C AND D TESTS	Performed on the product family representative types (by rotation); the results are extended to all the other devices of the same family according to the structure similarity concept
27	PACKING AND DOCUMENTATION INSPECTION	Inspection for: – right quantity – right type – right boxing – right labelling – right documentation – various

GROUP A INSPECTION - FINISHED PRODUCT ACCEPTANCE

ICs and Discrete devices

SUBGROUP	PARAMETERS	MINIMUM SAMPLE SIZE	ACCEPTANCE NUMBER
A1	Visual and mechanical inspection	315	0
A2+A3+A4	Cumulative electrical and inoperative mechanical failures	315	0

Notes
- This product acceptance is valid for standard production, for agreed customer programs other sampling plans can be applied
- Specified temperature ranges according to SGS-THOMSON databooks

GROUPS B, C AND D TESTS

Integrated circuits - Groups B, C and D tests

Every week or every three months on raw line and/or finished products

SUBGROUP	TEST PROCEDURE	MIL-STD-883 METHOD	CECC 90000 METHOD	SGS-THOMSON TEST CONDITIONS	PACKAGE			MINIMUM SAMPLE SIZE	ACCEPTANCE NUMBER (C)	NOTES
					METAL	CERAMIC	PLASTIC			(1)
1	Physical dimension	2016	4.3	Data Sheet Drawing		x	x	2	0	
2	Resistance to solvents	2015	4.4	1 minute immersion in solvent solution followed by 10 strokes with a hard brush as per MIL-STD method (the procedure shall be repeated 3 times)		x	x	4	0	
3	Solderability	2003	4.6.10 Cond 1	215 ±5°C 3 ±0.5sec. 235 ±5°C 2 ±0.5sec. 245 ±5°C 5 ±0.5sec.		– x x	x x x	22	0	2
4	Operating Life Test or Intermittent Life Test (for Power devices) end point electrical parameters	1005 – 	4.8 – 	1000 h according to detail spec 5000 Cycles as per device spec.		x – x	x x x	45	0	3
5	Temperature cycling Constant acceleration Seal - fine - gross	1010 2001 1014	4.6.8 4.6.7 4.6.9	10 cycles Ta = -65°C to + 150°C 30000 g see page 85		x x x x	– – – x	22 –	0	 4
6	Pressure pot end point electrical parameters	–	–	Ta = 121°C, 2 atm, 240 h min. as per device spec.		– –	x x	22	0	
7	HAST (Highly Accelerated Stress Test) end point electrical parameters	–	4.6.3 Cond2	130°C/85%RH with bias t=150h according to detail specification as per device spec.		– –	x x	22	0	

Notes
1) Sample can be increased according to LTPD table, till c=2
2) Aging of 8h in steam vapor or 16h at 155°C Soldering temperature of 215°C for SMD only
3) Ta such to have $T_J=T_J$ max
4) 20000g for packages with cavity perimeter of 5cm or more and/or with a mass of 5 grams or more

Integrated circuits - Groups B, C and D tests

Every six months on raw line and/or finished products

SUBGROUP	TEST PROCEDURE	MIL-STD-883 METHOD	CECC 90000 METHOD	SGS-THOMSON TEST CONDITIONS	PACKAGE			MINIMUM SAMPLE SIZE	ACCEPTANCE NUMBER (C)	NOTES
					METAL	CERAMIC	PLASTIC			(1)
1	Lead integrity	2004	4.6 12 (1)	Tensile test (as per CECC 90000)		–	–	22	0	
			4 6 12 (2)	Lead Fatigue Cond B2 - wire leads a force of of 0.229 ±0.014 Kg for three 90 ±5° arcs on each lead bending cycle 2 to 5 sec - dual-in-line and power moulded packages the leads shall be bent 3 times simultaneously for at least 15° permanent bend, returning then to the original position		x	x			2
				Solder pad adhesion Cond D a force of 0 299 Kg min to each solder pad for 30sec minimum	-	x	-			3
	Seal - fine - gross	1014	4 6 9	see page 85		x x	- -			
2	Thermal shock	1011	4 6.8	Cond B, 15 shocks, Ta = -55 to + 125°C		x	-	22	0	
	Temperature cycling	1010	4 6 8	Cond. C, 100 cycles Ta = - 65 to + 150°C		x	x			4
	Moisture resistance	1004	4 6.3	Lead bend conditioning followed by 10 cycles of 24h; Ta = 25°C to 65°C RH = 80% to 100%, one 3h cycle at Ta = -10°C		x	-			
	Seal - fine - gross	1014	4 6 9	see page 85		x x	- -			
	Visual examination	1004 1010	–	without appraisal of marking		x	-			
	end point electrical parameters			as per device spec.		x	x			
3	Mechanical shock	2002	4 6 4	Cond B, 1500g, 0 5 msec, 5 blows in each of the 6 orientations, not operating		x	–	22	0	
	Vibration, variable frequency	2007	4 6 5	Cond A; 20g, 3 orientations; f = 20 to 2000 cps; four 4 minutes cycles, 48 minutes total, not operating		x	–			
	Constant accelerations	2001	4.6.7	Cond E, 30000 g, Y1 orientation only		x	–			5
	Seal - fine - gross	1014	4 6 9	see page 85		x x	– –			
	Visual examination	1010 1011	–			x				
	end point electrical parameters			as per device spec		x	–			
4	Salt atmosphere	1009	4 6 14	Cond A. 10 to 50 gr of NaCl per m² for 24 h at Ta= 35°C min		x	x	22	0	
	Seal - fine - gross	1014	4 6 9	see page 85		x x	– –			
	Visual examination	1009	4 6 14			x	x			
5	Humidity test	–	4 6 3 Cond 1	85°C/85% RH with biast = 1000h according to detail specification		–	x	45	0	
	end point electrical parameters			as per device spec		–	x			
6	Internal water-vapor content	1018	–	Dew point method procedure 3 (5000 ppm max)		x	–	3 5	0 1	6
7	Lid Torque	2024	–	see page 86		x	–	22	0	7

Notes:
1) Sample can be increased according to LTPD table, till c=2
2) Not for SMD
3) Leadless chip carrier only
4) For plastic packages Ta= -65/-40°C according to device type
5) 20000g for packages with cavity perimeter of 5cm or more and/or with a mass of 5 grams or more
6) Test three devices If one fails, test two additional devices with no failure
7) Applied only to packages which use glass-frit seal to lead the frame lead or package body (i e wherever frit seal establishes hermeticity or package integrity)

HSCMOS - RESULT SUMMARY

Test	Condition	Plastic				Ceramic				SO Package			
		1992		1993		1992		1993		1992		1993	
		SS	REJ	SS	REJ	SS	REJ	SS	REJ	SS	REJ	SS	REJ
HIGH TEMPERATURE BIAS	1000 hrs	2862	0	3078	0	870	0	630	0	1512	0	1674	0
TEMPERATURE HUMIDITY BIAS	1000 hrs	2592	0	2862	0					1332	0	1440	0
PRESSURE COOKER	336 hrs	3120	0	3360	0					1830	0	1890	0
THERMAL CYCLES	1000 cyc	1650	0	1830	0	420	0	330	0	780	0	870	0

FAILURE RATE EVALUATION

Package	Deviation x hours at 125°C	Fail	Failure rate at 60% confidence level			
			Lambda (x)*	Fit **		
			Point estimate	70°C	55°C	40°C
PLASTIC	5.94×10^6	0	0.015	6.0	2.1	0.6
CERAMIC	1.50×10^6	0	0.06	23.8	8.1	2.5
SO PACKAGE	3.19×10^6	0	0.029	11.2	3.8	1.2

* Lambda (X) = % of failures on 1000 hours of operation
** FIT = Failure in Time. Number of failure on 10^9 Hours of operation
The activation energy, from analisys, was choosen 0.7 eV based on our tests results: the failure rate at lower operating temperature can be estrapolated by the Arrhenius plot.

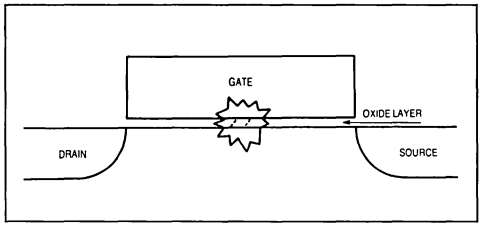
The actual junction temperature should be used; it can be computed using the relationship

$$T_j = T_A = (P \times \theta_{JA})$$

Where T_j = Junction temperature
T_A = Ambient temperature
θ_{JA} = Junction to ambient thermal resistance (typically 100 °C/watt for a 16 pin DIP)
P = Power actual consumption

ELECTROSTATIC DISCHARGE PROTECTION

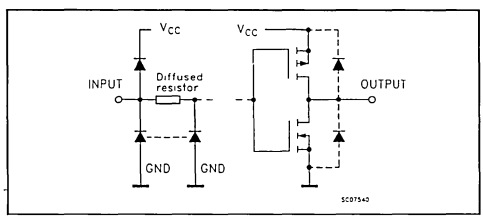
Electronic components have to be protected from the hazard of static electricity, from the manufacturing stage down to where they are utilized. MOS devices are typically voltage and electrical field sensitive; the thin oxide layers can be destroyed by an electric field.



This happens mostly because a charged conductor, typically a person, is rapidly discharged through the device.
There will be no net charge on any portion of the MOS structure; when the induced high field exceeds the breakdown voltage of the MOS capacitor structure we may have a self-healing breakdown, degradation or catastrophic failure.
The failure hazard is not limited to the gate region but it could occur wherever two conductive areas are separated by a thin insulator.
We have envisaged two sets of precautions: input protection networks and static discharge control (handling).

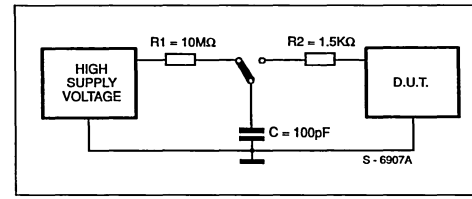
INPUT PROTECTION

The HSCMOS, in addition to improve performance and power consumption, also features improved input protection. This has been achieved by employing poly-silicon as a resistor structure at all inputs.
The resistor slows down the fast input transients generated by electrostatic discharges and dissipates some of the associated energy. Although these input resistors, in conjunction with the input diode, give improved levels of protection, it is still advisable to follow the usual CMOS has handling precautions.



The protection capability has been verified with the following discharge set.

Measurement with the MIL 883D-3015



The testing results are reported below

	MIL-STD-883D (C = 100pF R = 1.5 KΩ)
INPUT+	> 2 KV
INPUT−	> 2 KV
OUTPUT+	>2 KV
OUTPUT−	>2 KV

HANDLING

SGS-THOMSON has chosen a no-compromise strategy in the MOS ESD protection. From the wafer level to the shipping of finished units, each work station and processing of the party is guaranteed. This is achieved through total adoption of shielding and grownding media. Our final shipping is performed in antistatic tubes bags or boxes. The suppliers greatest efforts are in vain if the end user does not provide the same level of protection and care in application.
Here are the basic static control protection rules:

A - handle all components in a static-safe work area.
B - transport all components in static shielding containers.

To comply with the rules the following procedures must be set up.

1 - Static control wrist strap (from a qualified source) used and connected properly.
2 - Each table top must be protected with a conductive mat, properly grounded.
3 - Extensive use of conductive floor mats.
4 - Static control shoe straps, wearing typically insulating footwear, such as with crepe or thick rubber soles.
5 - Ionized air blowers are a necessary part of the protective system, to neutralize static charges on conductive items.
6 - Use only the grounded tip variety of soldering iron.
7 - Single components, tubes, printed circuit cards should always be contained in static shielding bags; keep our parts in the original bags up to the very last moment on the production line.
8 - If bigger containers (tote box) are used for inplant transport of devices or PC boards they must be electrically conductive, like the carbon loaded ones.

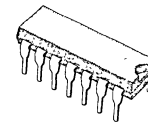
Hanglind (Continued)

9 - All tools, persons, testing machines, which could contact device leads must be conductive and grounded.
10 - Avoid using high dielectric materials (like polystyrene) for sub-assembly construction, storing and transportation.
11 - Follow a proper power supply sequence in testing and application. Supply voltage should be applied before and removed after input signals; insertion and removal from sockets should be done with no power applied.
12 - Filtration, noise suppression, slow voltage surges should be guaranteed on the supply lines.
13 - Any open (floating) input pin is a potential hazard to your circuit: ground or short them to V_{DD} whenever possible.

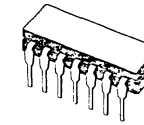
DATASHEETS

QUAD 2-INPUT NAND GATE

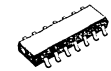
- HIGH SPEED
  t_{PD} = 6 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUTS DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS00
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

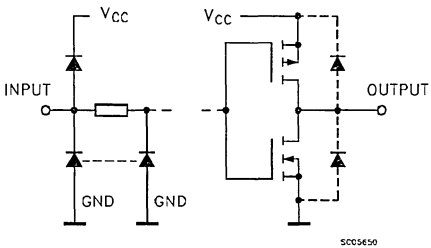
ORDER CODES :

M54HC00F1R M74HC00M1R
M74HC00B1R M74HC00C1R

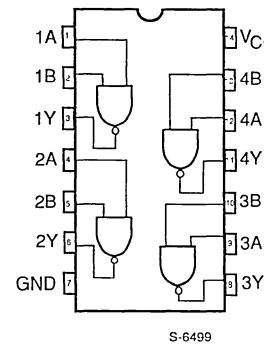
DESCRIPTION

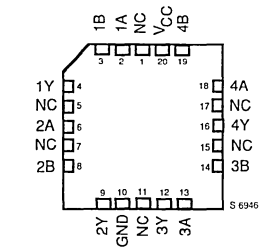
The M54/74HC00 is a high speed CMOS QUAD 2-INPUT NAND GATE fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



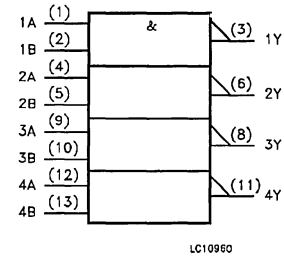


NC =
No Internal
Connection

TRUTH TABLE

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

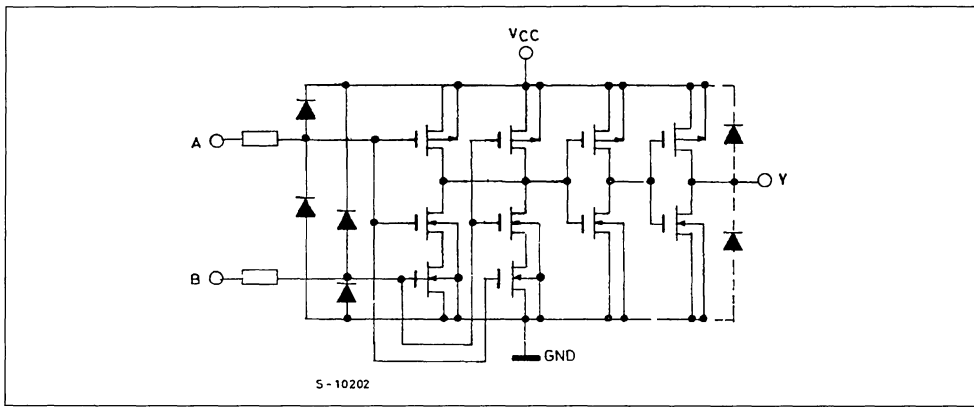
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data Inputs
2, 5, 10, 13	1B to 4B	Data Inputs
3, 6, 8, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

SCHEMATIC CIRCUIT (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series		-55 to +125	°C
	M74HC Series		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

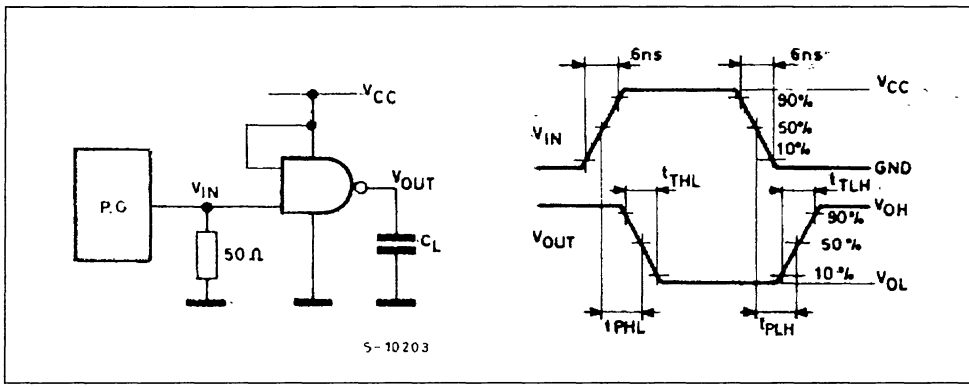
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

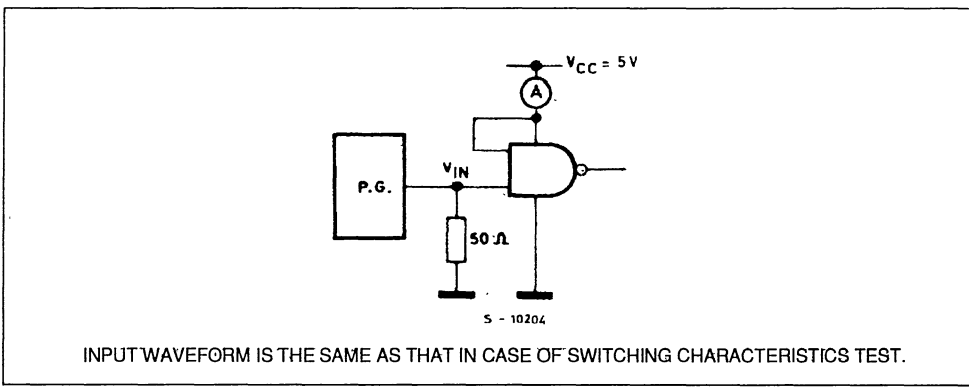
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			27	75		95		110	ns
		4.5			9	15		19		22	
		6.0			8	13		16		19	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				20						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



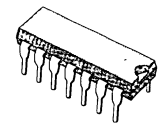
TEST CIRCUIT I_{CC} (Opr.)



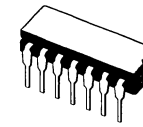
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

QUAD 2-INPUT NAND GATE

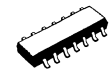
- HIGH SPEED
  t_{PD} = 12 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUTS DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS00
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

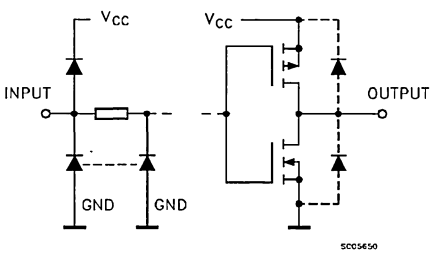
M54HCT00F1R M74HCT00M1R
M74HCT00B1R M74HCT00C1R

DESCRIPTION

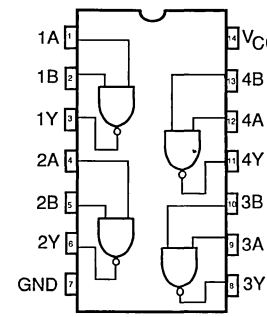
The M54/74HCT00 is a high speed CMOS QUAD 2-INPUT NAND GATE fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

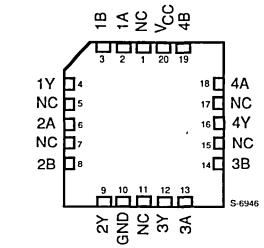
This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HC devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



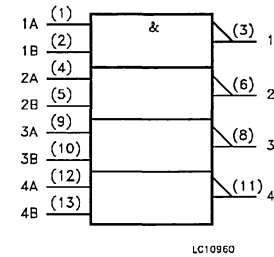


NC =
No Internal
Connection

TRUTH TABLE

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

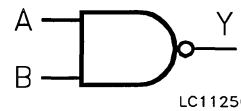
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data Inputs
2, 5, 10, 13	1B to 4B	Data Inputs
3, 6, 8, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied
(*) 500 mW: = 65 °C derate to 300 mW by 10mW/°C· 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

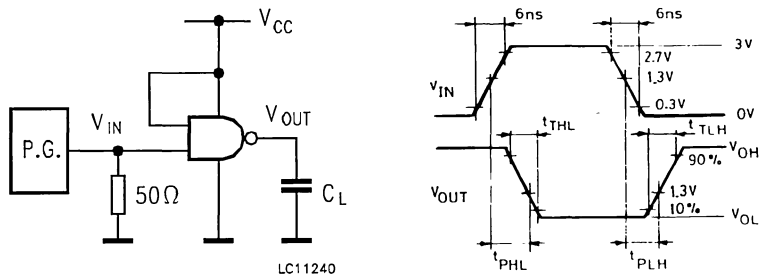
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.40	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				1		10		20	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9		3.0	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

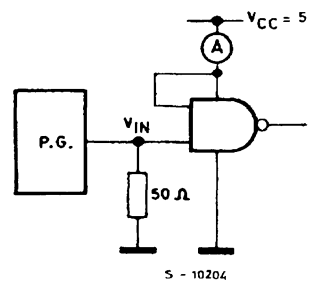
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			8	15		19		22	ns
t_{PLH} t_{PHL}	Propagation Delay Time	4.5			12	19		24		29	ns
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				40						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



TEST CIRCUIT I_{CC} (Opr.)



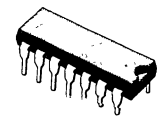
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

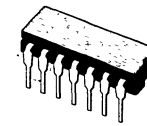
M54HC02
M74HC02

QUAD 2-INPUT NOR GATE

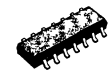
- HIGH SPEED
  t_{PD} = 6 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS02



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HC02F1R M74HC02M1R
M74HC02B1R M74HC02C1R

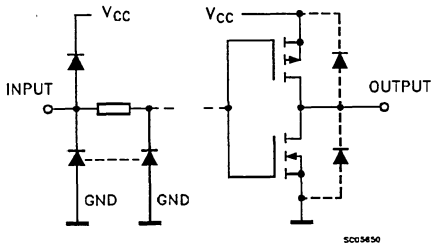
DESCRIPTION

The M54/74HC02 is a high speed CMOS QUAD 2-INPUT NOR GATE fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

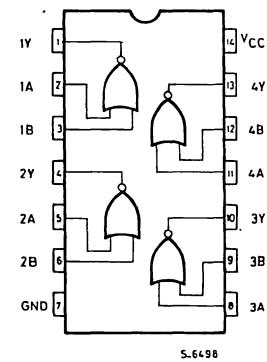
The internal circuit is composed of 3 stages including buffer output, which gives high noise immunity and stable output.

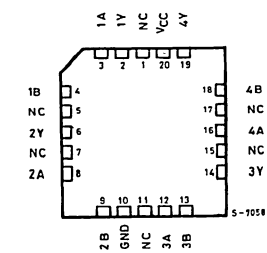
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



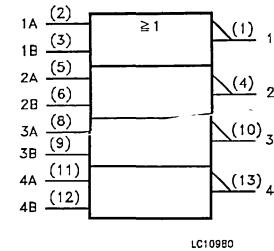


NC =
No Internal
Connection

TRUTH TABLE

A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

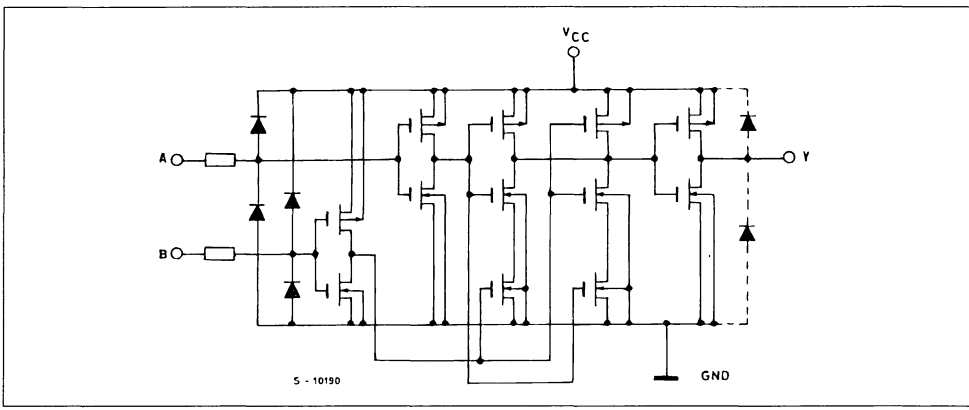
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
2, 5, 8, 11	1A to 4A	Data Inputs
3, 6, 9, 12	1B to 4B	Data Inputs
1, 4, 10, 13	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

SCHEMATIC CIRCUIT (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

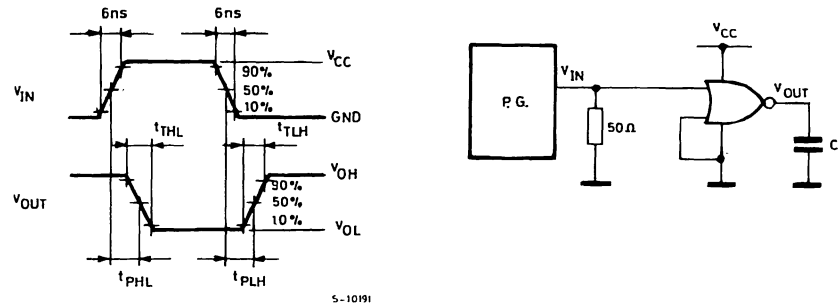
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4..31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

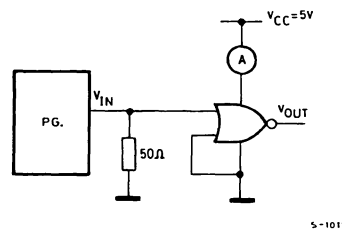
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			27	75		95		110	ns
		4.5			9	15		19		22	
		6.0			8	13		16		19	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				21						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



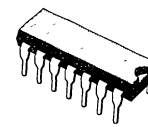
TEST CIRCUIT I_{CC} (Opr.)



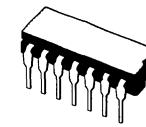
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

QUAD 2-INPUT NOR GATE

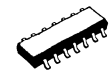
- HIGH SPEED
  t_{PD} = 11 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS02



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

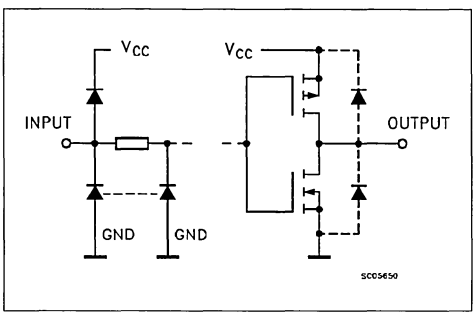
M54HCT02F1R M74HCT02M1R
M74HCT02B1R M74HCT02C1R

DESCRIPTION

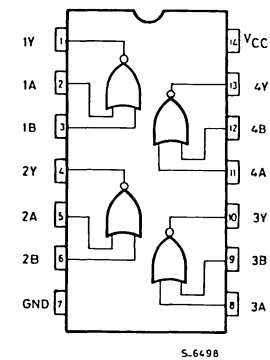
The M54/74HCT02 is a high speed CMOS QUAD 2-INPUT NOR GATE fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The internal circuit is composed of 3 stages including buffer output, which gives high noise immunity and stable output. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

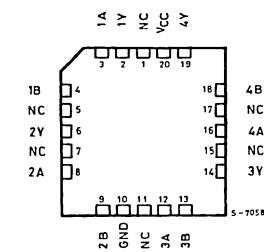
This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



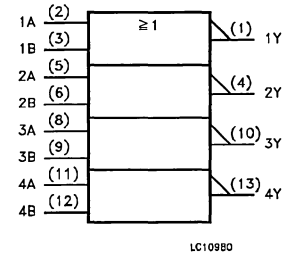


NC =
No Internal
Connection

TRUTH TABLE

A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

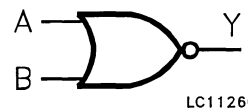
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
2, 5, 8, 11	1A to 4A	Data Inputs
3, 6, 9, 12	1B to 4B	Data Inputs
1, 4, 10, 12	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

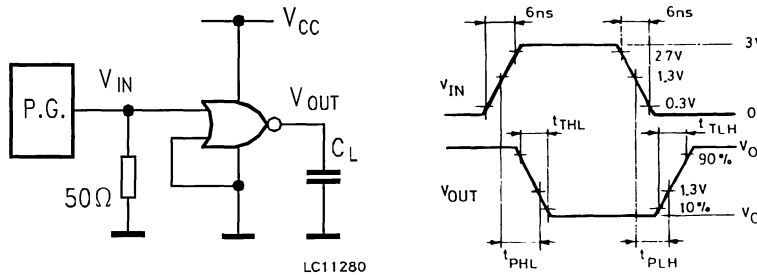
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				1		10		20	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9		3.0	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

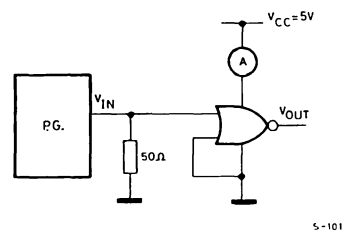
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			8	15		19		22	ns
t_{PLH} t_{PHL}	Propagation Delay Time	4.5			15	24		30		36	ns
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				25						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



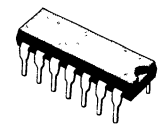
TEST CIRCUIT I_{CC} (Opr.)



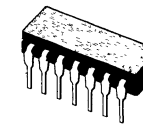
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

QUAD 2-INPUT OPEN DRAIN NAND GATE

- HIGH SPEED
  t_{PZ} = 5 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS03



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HC03F1R	M74HC03M1R
M74HC03B1R	M74HC03C1R

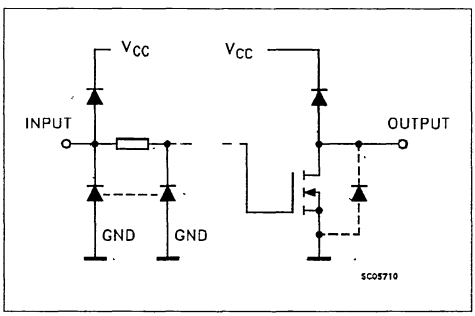
DESCRIPTION

The M54/74HC03 is a high speed CMOS QUAD 2-INPUT OPEN DRAIN NAND GATE fabricated in silicon gate C^2MOS technology.

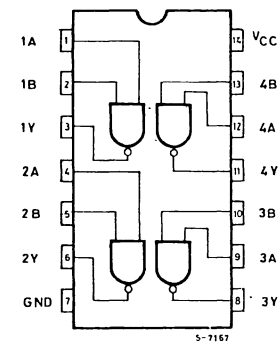
It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

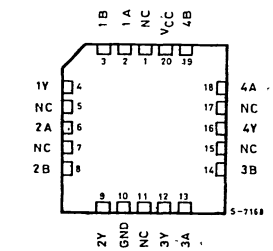
The internal circuit is composed of 3 stages including buffer output, which gives high noise immunity and stable output. This device can, with an external pull-up resistor, be used in wired AND configuration. This device can be also used as a led driver and in any other application requiring a current sink. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





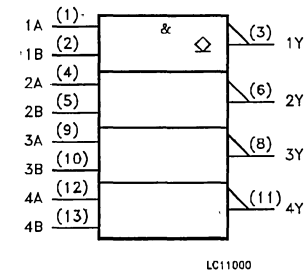
NC = No Internal Connection

TRUTH TABLE

A	B	Y
L	L	Z
L	H	Z
H	L	Z
H	H	L

Z = HIGH IMPEDANCE

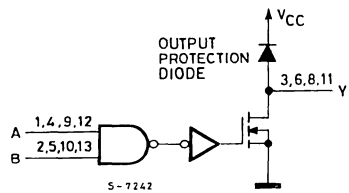
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data Inputs
2, 5, 10, 13	1B to 4B	Data Inputs
3, 6, 8, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

CIRCUIT DIAGRAM



VCC = Pin 14
GND = Pin 7
open–drain outputs

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Sink Current Per Output Pin	+ 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	Output Leakage Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	µA

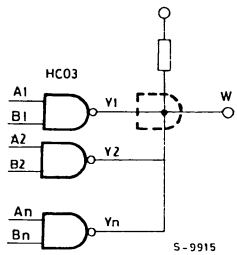
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLZ}	Propagation Delay Time	2.0	RL = 1 KΩ		16	60		75		90	ns
		4.5			9	12		15		18	
		6.0			8	10		13		15	
t_{PZL}	Propagation Delay Time	2.0	R_L = 1 KΩ		23	60		75		90	ns
		4.5			7	12		15		18	
		6.0			6	10		13		15	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				7						pF

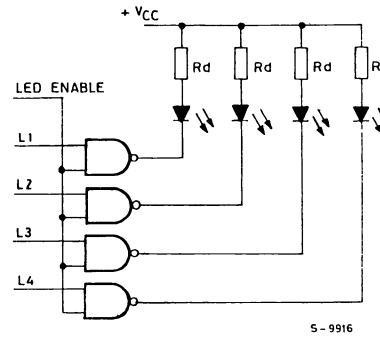
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Gate)

TYPICAL APPLICATIONS

Wired AND



LED Driver with Blanking



Typical values
V_{CC} = 5V
V_D = 2V
V_{DS} = 0.4V
R_D = 120 ÷ 270Ω

$W = Y1\ Y2 \ldots\ Yn = \overline{A1B1}\ \overline{A2B2} \ldots \overline{AnBn} = \overline{A1B1 + A2B2 + \ldots + AnBn}$

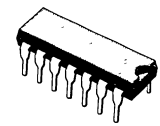
I_D = 10 ÷ 20 mA

$$R_D = \frac{V_{CC} - V_D - V_{DS}}{I_D} = \frac{5 - 2 - 0.4}{20 \times 10^{-3}} = 130\ \Omega\ (*)$$

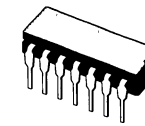
(*) 260 Ω with I_D = 10 mA.

HEX INVERTER

- HIGH SPEED
  t_{PD} = 6 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS04



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

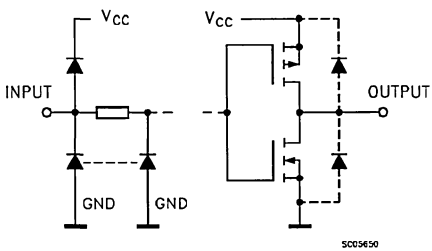
M54HC04F1R M74HC04M1R
M74HC04B1R M74HC04C1R

DESCRIPTION

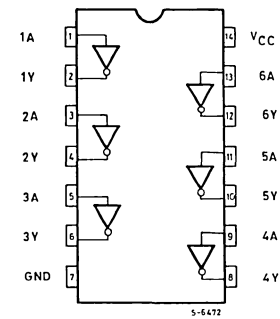
The M54/74HC04 is a high speed CMOS HEX INVERTER fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

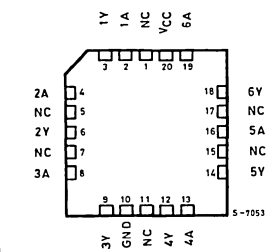
The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output. All inputs are equipped with circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



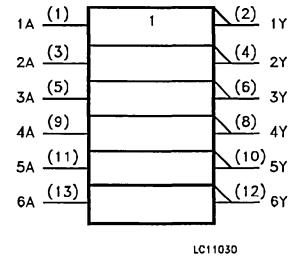


NC =
No Internal
Connection

TRUTH TABLE

A	Y
L	H
H	L

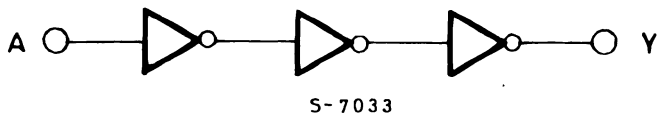
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	Data Inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

LOGIC DIAGRAM (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

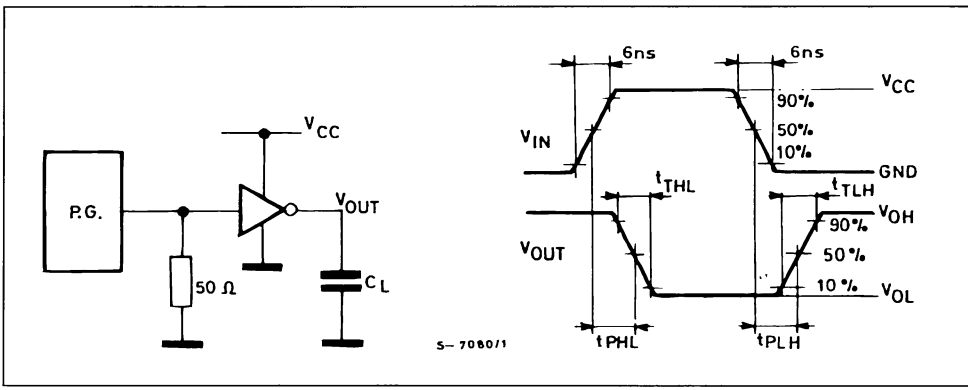
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

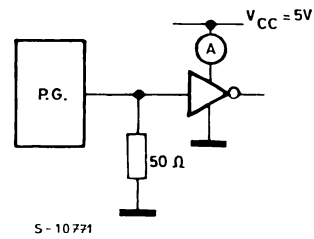
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			27	75		95		110	ns
		4.5			9	15		19		22	
		6.0			8	13		16		19	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				22						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



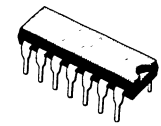
TEST CIRCUIT I_{CC} (Opr.)



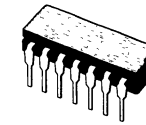
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

HEX INVERTER

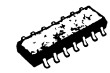
- HIGH SPEED
  t_{PD} = 8 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS04



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

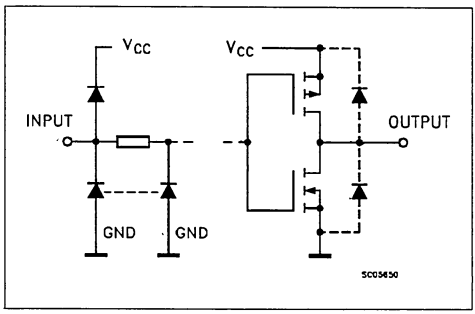
ORDER CODES :

M54HCT04F1R M74HCT04M1R
M74HCT04B1R M74HCT04C1R

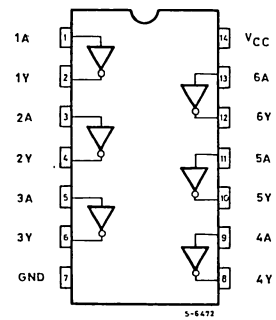
DESCRIPTION

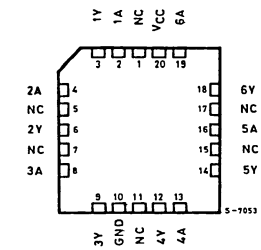
The M54/74HCT04 is a high speed CMOS INVERTER fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The internal circuit is composed of 3 stages including buffered output, which gives high noise immunity and a stable output.
All inputs are equipped with protection circuits against static discharge or transient excess voltage. This integrated circuit has input and output characteristic that are fully compatible with 54/74 LSTTL logic families. M54HCT/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



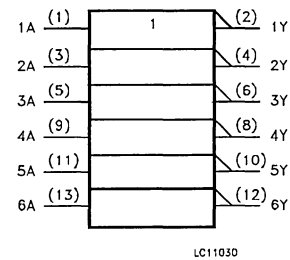


NC =
No Internal
Connection

TRUTH TABLE

A	Y
L	H
H	L

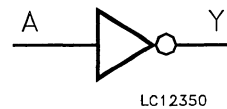
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	Data Inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

LOGIC DIAGRAM (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW ≅ 65 °C derate to 300 mW by 10mW/°C· 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

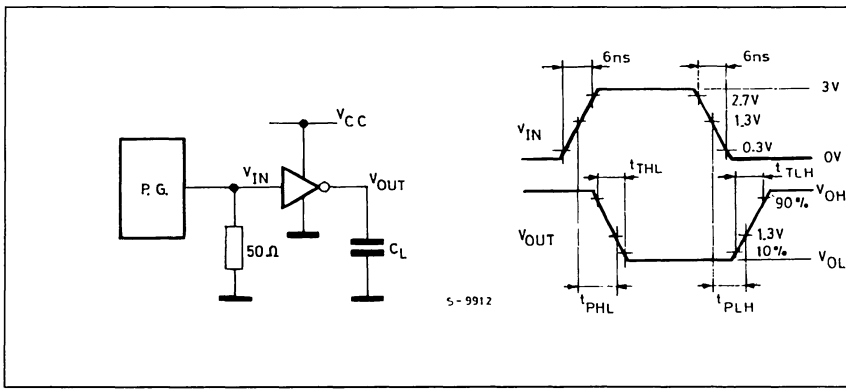
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				1		10		20	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9		3.0	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

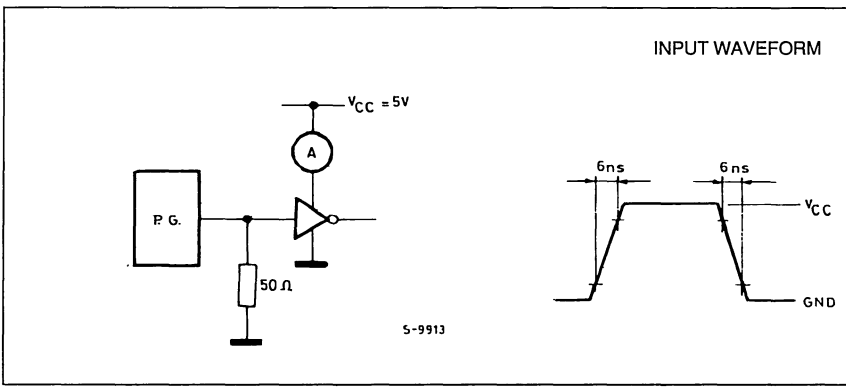
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			8	15		19		23	ns
t_{PLH} t_{PHL}	Propagation Delay Time	4.5			11	18		23		27	ns
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				20						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT

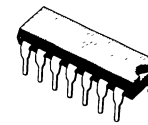


TEST CIRCUIT I_{CC} (Opr.)

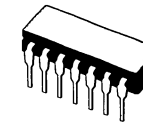


HEX INVERTER (SINGLE STAGE)

- HIGH SPEED
  t_{PD} = 5 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 10 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS04



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HCU04F1R M74HCU04M1R
M74HCU04B1R M74HCU04C1R

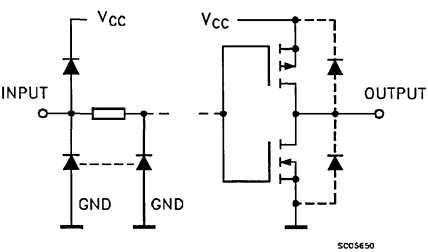
DESCRIPTION

The M54/74HCU04 is a high speed CMOS HEX INVERTER (SINGLE STAGE) fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

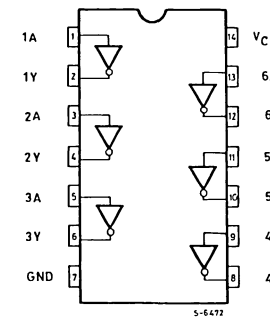
As the intrnal circuit is composed of a single stage inverter, it can be used in crystal oscillator.

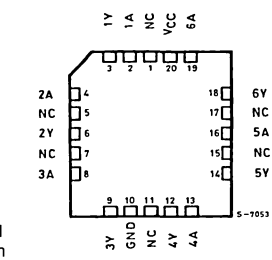
All inputs are equipped with circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



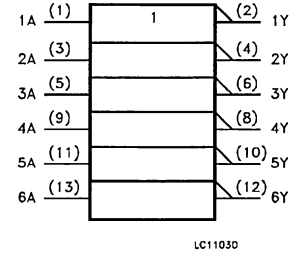


NC =
No Internal
Connection

TRUTH TABLE

A	Y
L	H
H	L

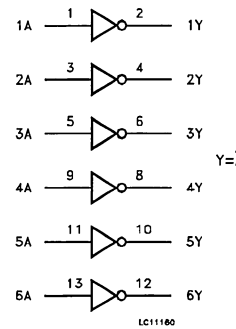
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	Data Inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

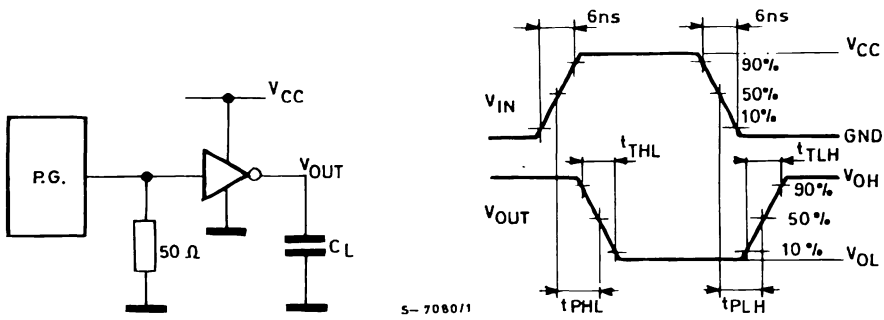
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.7			1.7		1.7		V
		4.5			3.6			3.6		3.6		
		6.0			4.8			4.8		4.8		
V_{IL}	Low Level Input Voltage	2.0					0.3		0.3		0.3	V
		4.5					0.9		0.9		0.9	
		6.0					1.2		1.2		1.2	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.8	2.0		1.8		1.8		V
		4.5			4.0	4.5		4.0		4.0		
		6.0			5.5	5.9		5.5		5.5		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.2		0.2		0.2	V
		4.5				0.0	0.5		0.5		0.5	
		6.0				0.1	0.5		0.5		0.5	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

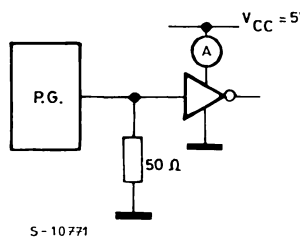
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			18	60		75		90	ns
		4.5			6	12		15		18	
		6.0			5	10		13		15	
C_{IN}	Input Capacitance				5	15		15		15	pF
C_{PD} (*)	Power Dissipation Capacitance				13						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST CIRCUIT



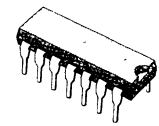
TEST CIRCUIT I_{CC} (Opr.)



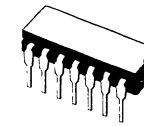
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

HEX INVERTER (OPEN DRAIN)

- HIGH SPEED
  t_{PD} = 8 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS05



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

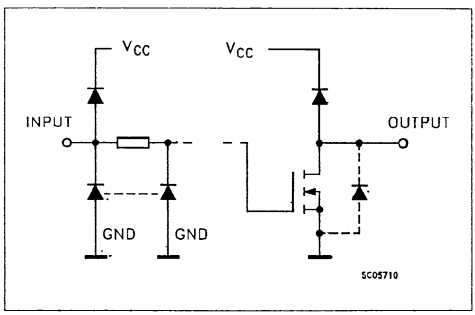
M54HC05F1R
M74HC05B1R
M74HC05M1R
M74HC05C1R

DESCRIPTION

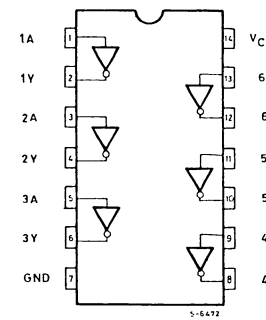
The M54/74HC05 is a high speed CMOS HEX OPEN DRAIN INVERTER fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

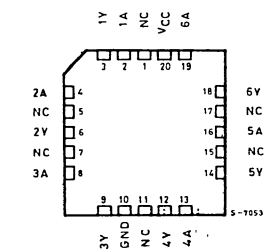
The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output. All inputs are equipped with circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





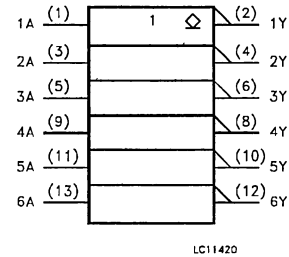
NC =
No Internal
Connection

TRUTH TABLE

A	Y
L	Z
H	L

Z = High impedance

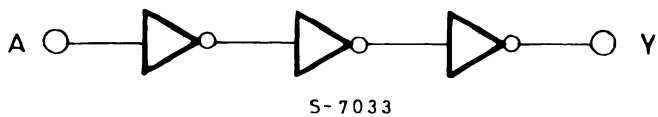
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	Data Inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

LOGIC DIAGRAM (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Sink Current Per Output Pin	25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series		-55 to +125	°C
	M74HC Series		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	Output Leakage Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	µA

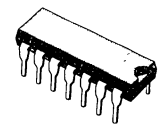
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLZ}	Propagation Delay Time	2.0	R_L = 1KΩ		20	90		115		135	ns
		4.5			11	18		23		27	
		6.0			10	15		20		23	
t_{PZL}	Propagation Delay Time	2.0	R_L = 1KΩ		33	90		115		135	ns
		4.5			9	18		23		27	
		6.0			8	15		20		23	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{OUT}	Output Capacitance				10						pF
C_{PD} (*)	Power Dissipation Capacitance				6.5						pF

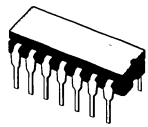
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

HEX BUFFER (OPEN DRAIN)

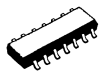
- HIGH SPEED
  t_{PD} = 5 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS07



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

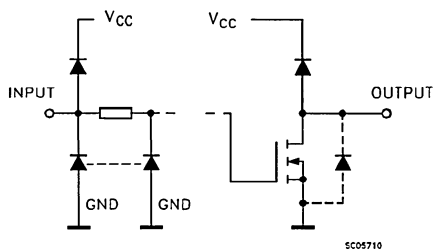
M54HC07F1R M74HC07M1R
M74HC07B1R M74HC07C1R

DESCRIPTION

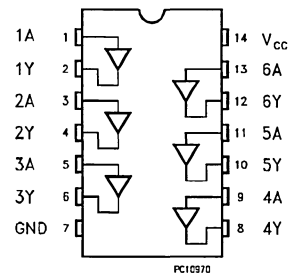
The M54/74HC07 is a high speed CMOS HEX OPEN DRAIN BUFFER fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

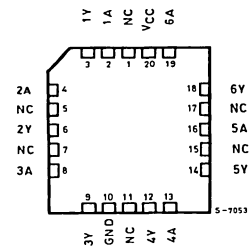
The internal circuit is composed of 2 stages including buffer output, which enables high noise immunity and stable output. All inputs are equipped with circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





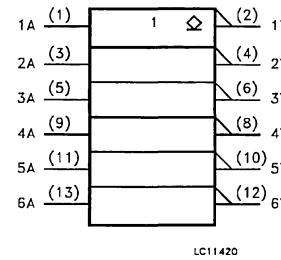
NC =
No Internal
Connection

TRUTH TABLE

A	Y
L	L
H	Z

Z = High impedance

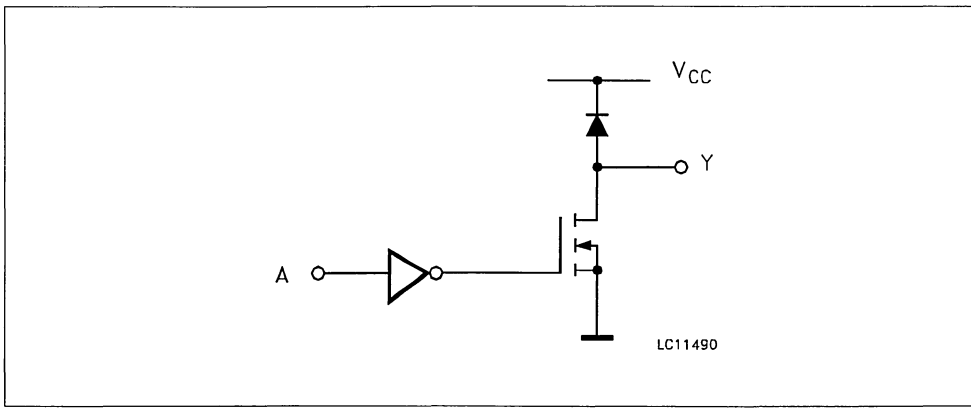
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	Data Inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

LOGIC DIAGRAM (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Sink Current Per Output Pin	25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	Output Leakage Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	µA

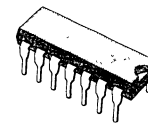
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLZ}	Propagation Delay Time	2.0	R_L = 1KΩ		10	90		115		135	ns
		4.5			7	18		23		27	
		6.0			6	15		20		23	
t_{PZL}	Propagation Delay Time	2.0	R_L = 1KΩ		17	90		115		135	ns
		4.5			7	18		23		27	
		6.0			5	15		20		23	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{OUT}	Output Capacitance				3						pF
C_{PD} (*)	Power Dissipation Capacitance				4						pF

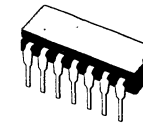
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$ (per Gate)

QUAD 2-INPUT AND GATE

- HIGH SPEED
  t_{PD} = 6 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS08



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HC08F1R M74HC08M1R
M74HC08B1R M74HC08C1R

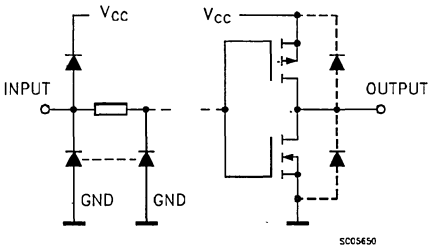
DESCRIPTION

The M54/74HC08 is a high speed CMOS QUAD 2-INPUT AND GATE fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

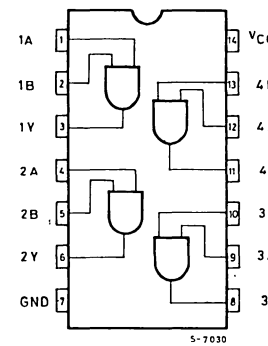
The internal circuit is composed of 2 stages including buffer output, which gives high noise immunity and stable output.

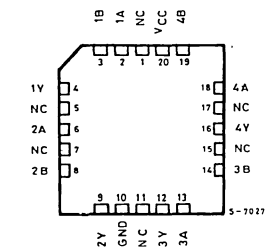
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



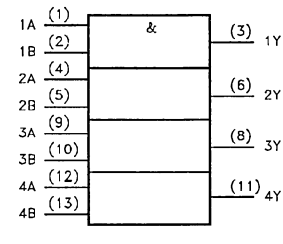


NC =
No Internal
Connection

TRUTH TABLE

A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

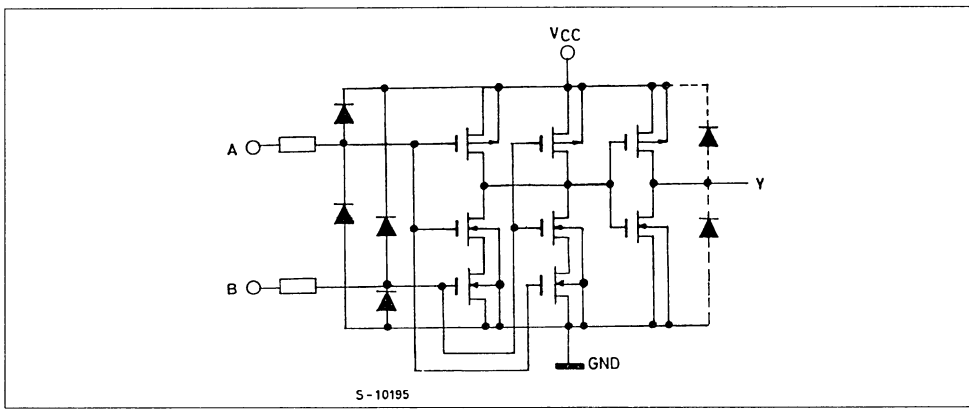
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data Inputs
2, 5, 10, 13	1B to 4B	Data Inputs
3, 6, 8, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

SCHEMATIC CIRCUIT (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series		-55 to +125	°C
	M74HC Series		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

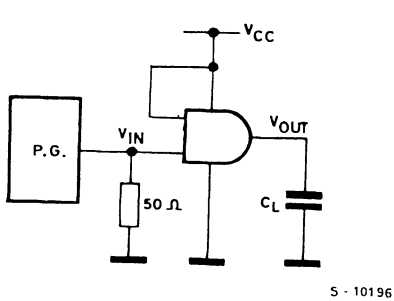
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	µA

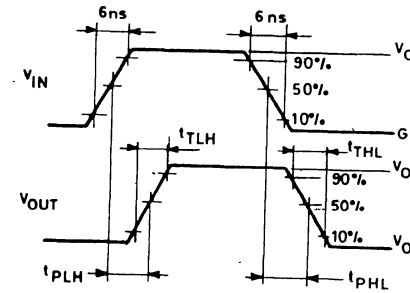
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			24	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				19						pF

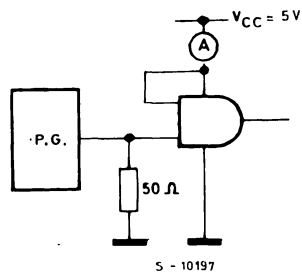
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit) Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT





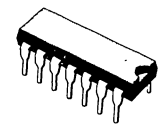
TEST CIRCUIT I_{CC} (Opr.)



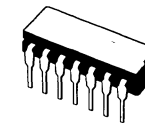
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

QUAD 2-INPUT AND GATE

- HIGH SPEED
  t_{PD} = 12 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS08



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

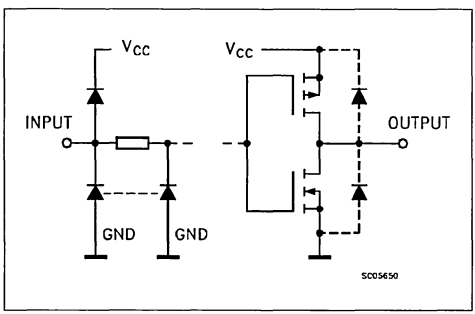
M54HCT08F1R M74HCT08M1R
M74HCT08B1R M74HCT08C1R

DESCRIPTION

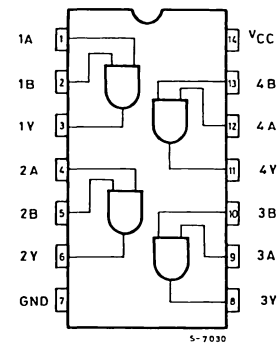
The M54/74HCT08 is a high speed CMOS QUAD 2-INPUT AND GATE fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The internal circuit is composed of 2 stages including buffer output, which gives high noise immunity and stable output. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

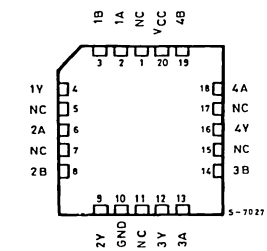
This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HC devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



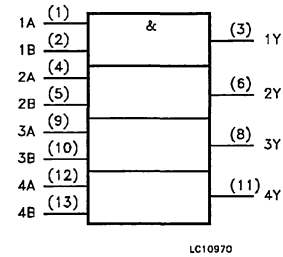


NC =
No Internal
Connection

TRUTH TABLE

A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

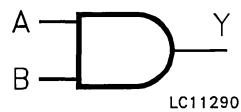
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data Inputs
2, 5, 10, 13	1B to 4B	Data Inputs
3, 6, 8, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

SCHEMATIC CIRCUIT (Per Gate)



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW. ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

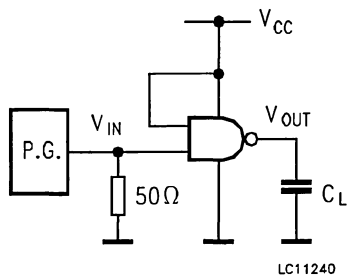
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				1		10		20	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9		3.0	mA

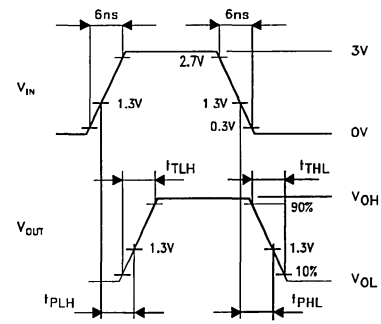
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			8	15		19		22	ns
t_{PLH} t_{PHL}	Propagation Delay Time	4.5			13	21		26		32	ns
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				38						pF

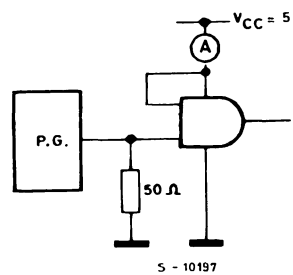
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT





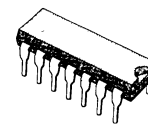
TEST CIRCUIT I_{CC} (Opr.)



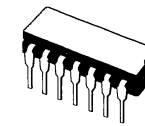
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

QUAD 2-INPUT AND GATE (OPEN DRAIN)

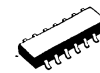
- HIGH SPEED
  t_{PD} = 6 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS09



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HC09F1R M74HC09M1R
M74HC09B1R M74HC09C1R

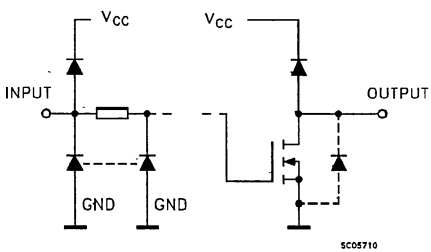
DESCRIPTION

The M54/74HC09 is a high speed CMOS QUAD 2-INPUT OPEN DRAIN AND GATE fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

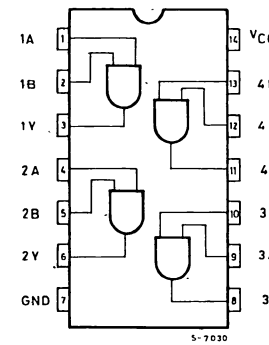
The internal circuit is composed of 3 stages including buffer output, which gives high noise immunity and stable output.

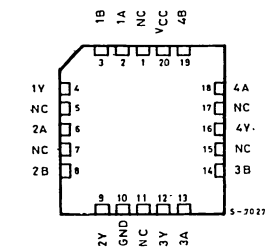
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





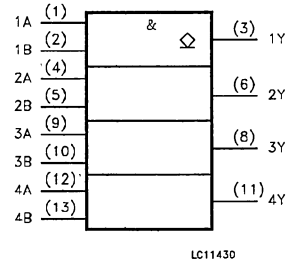
NC =
No Internal
Connection

TRUTH TABLE

A	B	Y
L	L	L
L	H	L
H	L	L
H	H	Z

Z = HIGH IMPEDANCE

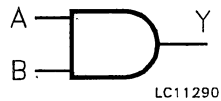
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data Inputs
2, 5, 10, 13	1B to 4B	Data Inputs
3, 6, 8, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Sink Current Per Output Pin	25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

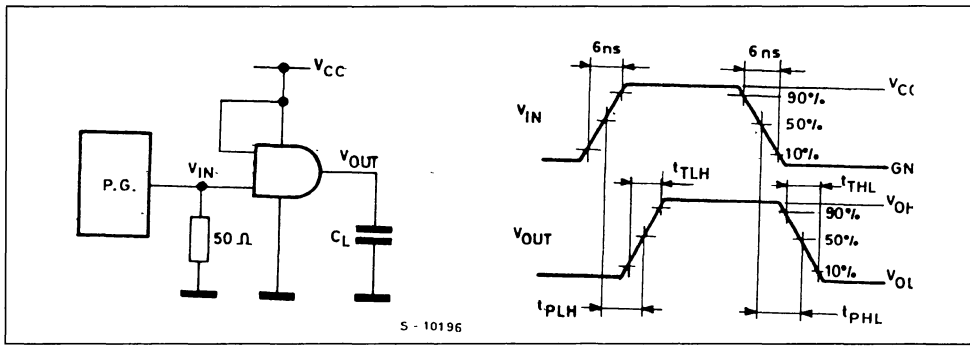
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	Output Leakage Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

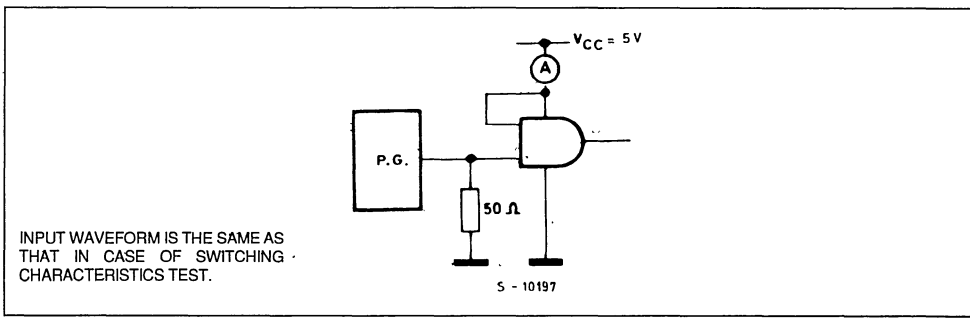
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLZ}	Propagation Delay Time	2.0	R_L = 1 KΩ		10	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PZL}	Propagation Delay Time	2.0	R_L = 1 KΩ		20	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{OUT}	Output Capacitance				3						pF
C_{PD} (*)	Power Dissipation Capacitance				5						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



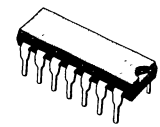
TEST CIRCUIT I_{CC} (Opr.)



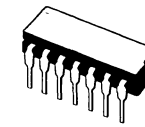
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TRIPLE 3-INPUT NAND GATE

- HIGH SPEED
  t_{PD} = 6 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS10



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HC10F1R M74HC10M1R
M74HC10B1R M74HC10C1R

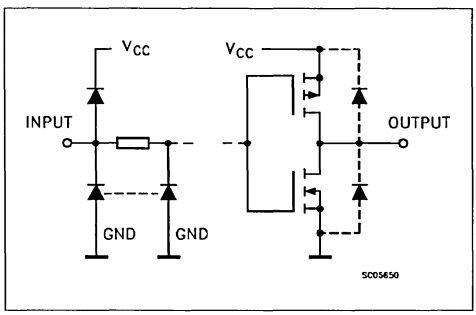
DESCRIPTION

The M54/74HC10 is a high speed CMOS TRIPLE 3-INPUT NAND GATE fabricated with silicon gate C^2MOS technology.

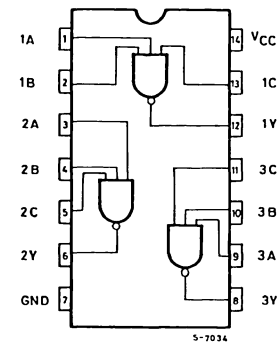
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output.

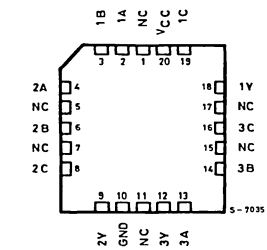
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



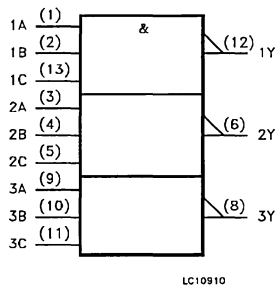


NC =
No Internal
Connection

TRUTH TABLE

A	B	C	Y
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

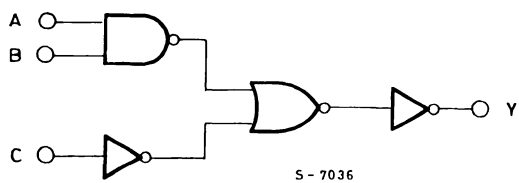
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A to 3A	Data Inputs
2, 4, 10	1B to 3B	Data Inputs
13, 5, 11	1C to 3C	Data Inputs
12, 6, 8	1Y to 3Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

SCHEMATIC CIRCUIT (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series		-55 to +125	°C
	M74HC Series		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

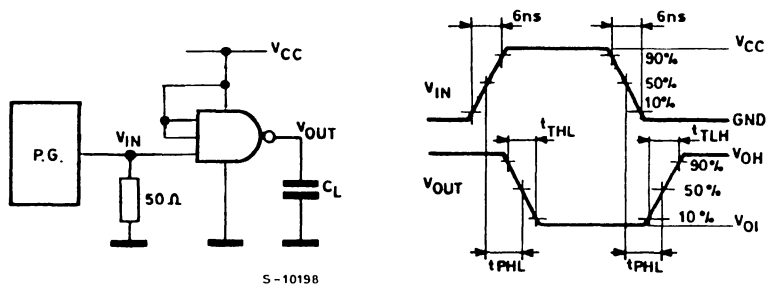
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

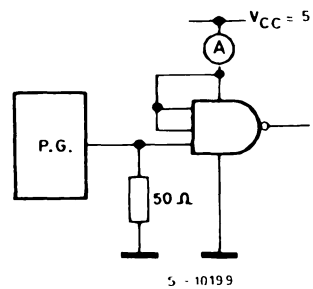
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			27	75		95		110	ns
		4.5			9	15		19		22	
		6.0			8	13		16		19	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				23						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/3$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



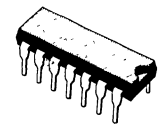
TEST CIRCUIT I_{CC} (Opr.)



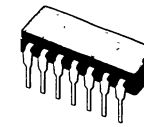
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TRIPLE 3-INPUT NAND GATE

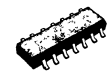
- HIGH SPEED
  t_{PD} = 11 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS10



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

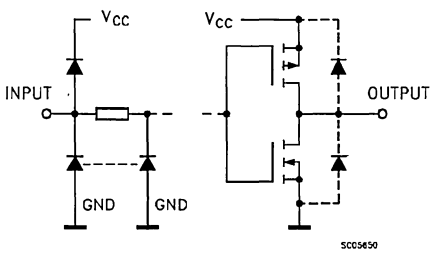
M54HCT10F1R M74HCT10M1R
M74HCT10B1R M74HCT10C1R

DESCRIPTION

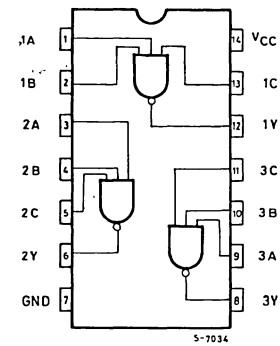
The M54/74HCT10 is a high speed CMOS TRIPLE 3-INPUT NAND GATE fabricated with silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

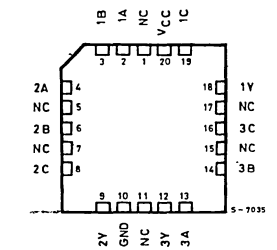
This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



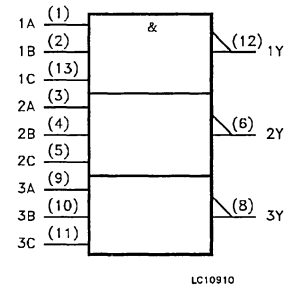


NC = No Internal Connection

TRUTH TABLE

A	B	C	Y
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

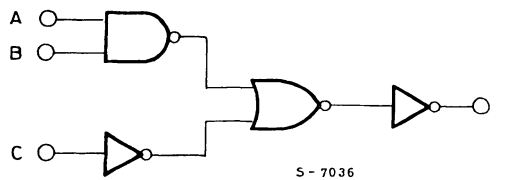
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A to 3A	Data Inputs
2, 4, 10	1B to 3B	Data Inputs
13, 5, 11	1C to 3C	Data Inputs
12, 6, 8	1Y to 3Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

SCHEMATIC CIRCUIT (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied

(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

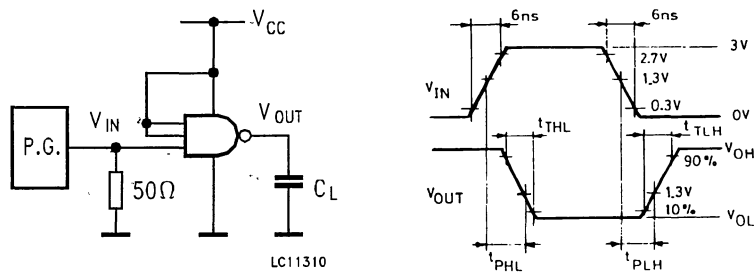
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				1		10		20	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9		3.0	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

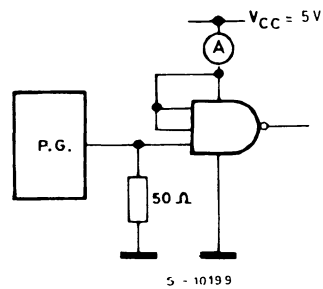
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			8	15		19		22	
t_{PLH} t_{PHL}	Propagation Delay Time	4.5			14	22		28		33	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				46						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation: $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/3$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



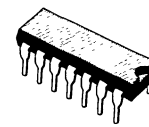
TEST CIRCUIT I_{CC} (Opr.)



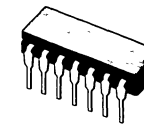
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TRIPLE 3-INPUT AND GATE

- HIGH SPEED
  t_{PD} = 7 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS11



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

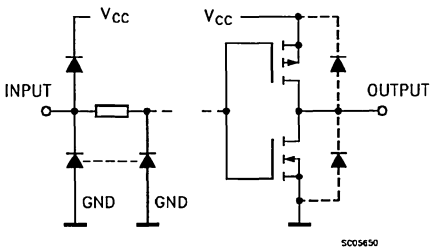
ORDER CODES :

M54HC11F1R M74HC11M1R
M74HC11B1R M74HC11C1R

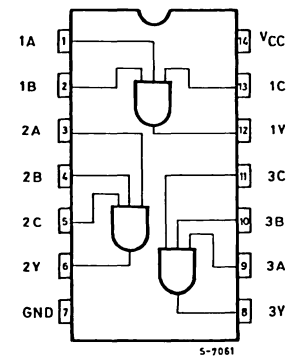
DESCRIPTION

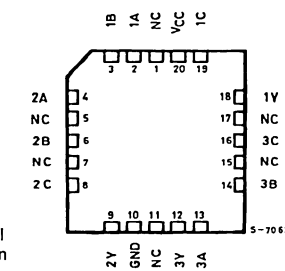
The M54/74HC11 is a high speed CMOS TRIPLE 3-INPUT AND GATE fabricated in silicon gate C^2MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The internal circuit is composed of 4 stages including buffered output, which gives high noise immunity and a stable output. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



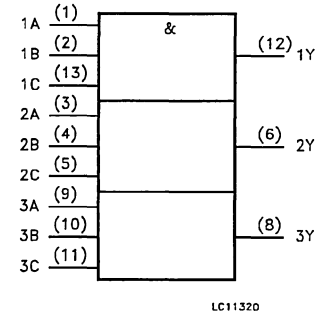


NC =
No Internal
Connection

TRUTH TABLE

A	B	C	Y
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

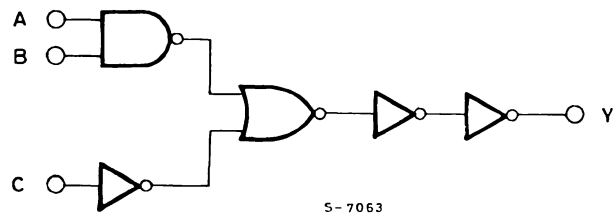
IEC Logic Symbol



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A to 3A	Data Inputs
2, 4, 10	1B to 3B	Data Inputs
13, 5, 11	1C to 3C	Data Inputs
12, 6, 8	1Y to 3Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

SCHEMATIC CIRCUIT (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

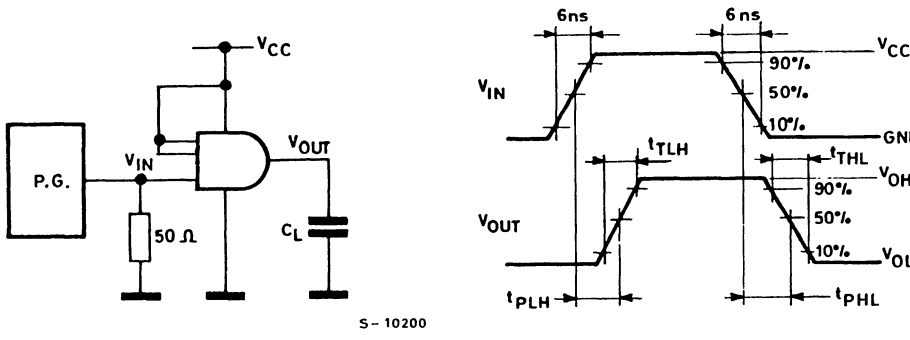
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

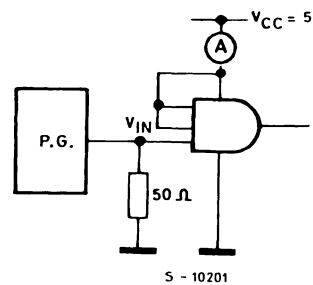
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			40	85		105		130	ns
		4.5			10	17		21		26	
		6.0			9	14		18		22	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				26						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/3$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



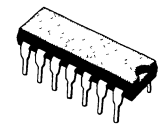
TEST CIRCUIT I_{CC} (Opr.)



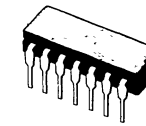
INPUT WAVEFORM IS THE SAVE AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

HEX SCHMITT INVERTER

- HIGH SPEED
  t_{PD} = 11 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  V_H = 1.1 V (TYP.) AT V_{CC} = 5 V
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS14



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

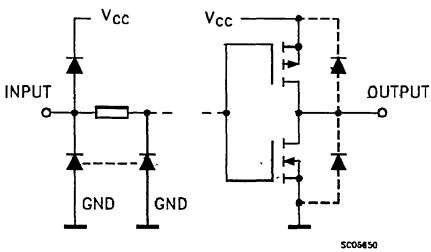
M54HC14F1R M74HC14M1R
M74HC14B1R M74HC14C1R

DESCRIPTION

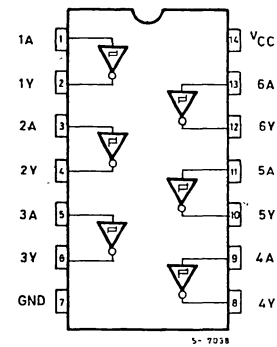
The M54/74HC14 is a high speed CMOS HEX SCHMITT INVERTER fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. Pin configuration and function are the same as those of the HC04 but all inputs have 20 % V_{CC} hysteresis level.

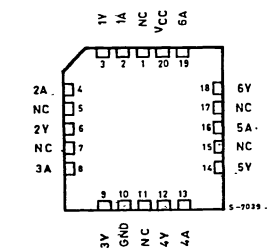
This together with its schmitt trigger function allows it to be used on line receivers with slow rise/fall input signals. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



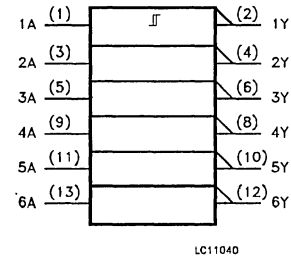


NC =
No Internal
Connection

TRUTH TABLE

A	Y
L	H
H	L

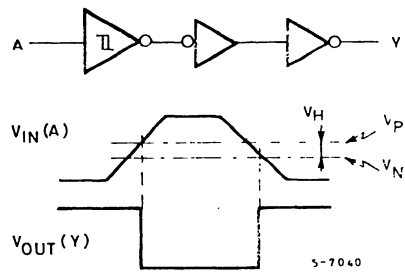
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	Data Inputs
2, 4, 6, 8, 10,12	1Y to 6Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

LOGIC DIAGRAM/WAVEFORM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	No Limits	

DC SPECIFICATIONS

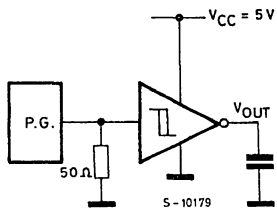
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_P	High Level Threshold Voltage	2.0			1.0	1.25	1.5	1.0	1.5	1.0	1.5	V
		4.5			2.3	2.7	3.15	2.3	3.15	2.3	3.15	
		6.0			3.0	3.5	4.2	3.0	4.2	3.0	4.2	
V_N	Low Level Threshold Voltage	2.0			0.3	0.65	0.9	0.3	0.9	0.3	0.9	V
		4.5			1.13	1.6	2.0	1.13	2.0	1.13	2.0	
		6.0			1.5	2.3	2.6	1.5	2.6	1.5	2.6	
V_H	Hysteresis Voltage	2.0			0.3	0.6	1.0	0.3	1.0	0.3	1.0	V
		4.5			0.6	1.1	1.4	0.6	1.4	0.6	1.4	
		6.0			0.8	1.2	1.4	0.8	1.7	0.8	1.7	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	µA

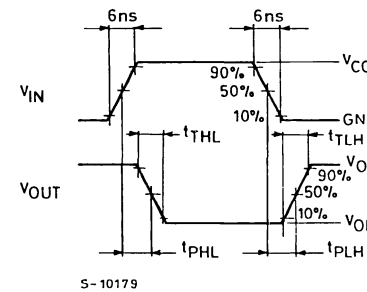
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			42	125		155		190	ns
		4.5			14	25		31		38	
		6.0			12	21		26		32	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				28						pF

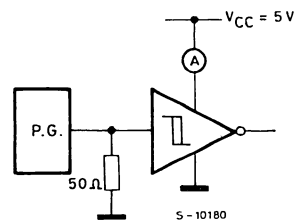
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST CIRCUIT





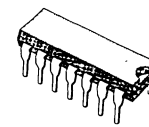
TEST CIRCUIT I_{CC} (Opr.)



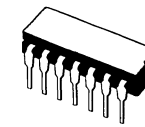
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

HEX SCHMITT INVERTER

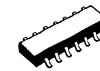
- HIGH SPEED
  t_{PD} = 16 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  V_H = 0.7 V (TYP.) AT V_{CC} = 5 V
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS14



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

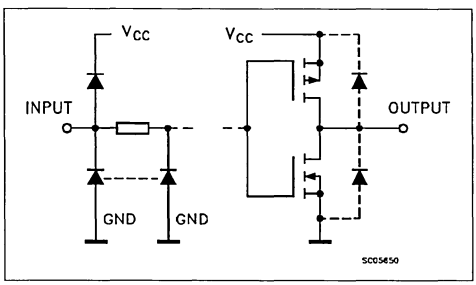
ORDER CODES :

M54HCT14F1R M74HCT14M1R
M74HCT14B1R M74HCT14C1R

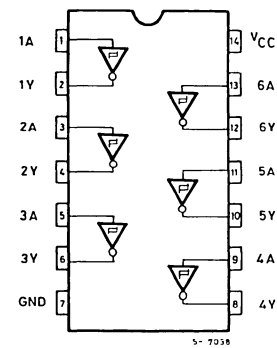
DESCRIPTION

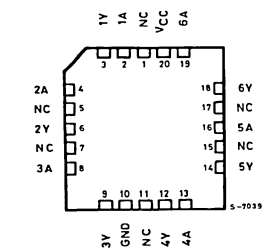
The M54/74HCT14 is a high speed CMOS HEX SCHMITT INVERTER fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. Pin configuration and function are the same as those of the HCT04 but all inputs have 0.7 V hysteresis level.This together with its schmitt trigger function allows it to be used on line receivers with slow rise/fall input signals. This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



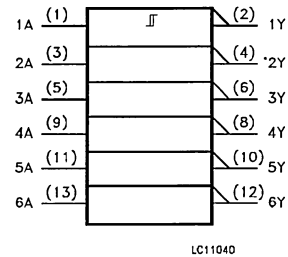


NC =
No Internal
Connection

TRUTH TABLE

A	Y
L	H
H	L

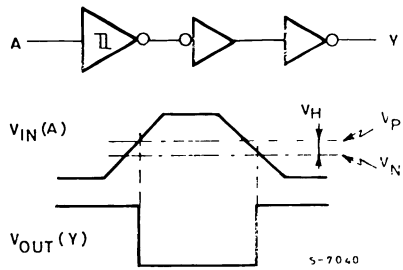
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	Data Inputs
2, 4, 6, 8, 10,12	1Y to 6Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

LOGIC DIAGRAM/WAVEFORM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C. 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C

DC SPECIFICATIONS

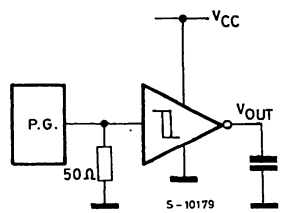
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_P	High Level Threshold Voltage	4.5			1.2	1.55	1.9	1.2	1.9	1.2	1.9	V
		5.5			1.4	1.75	2.1	1.4	2.1	1.4	2.1	
V_N	High Level Threshold Voltage	4.5			0.5	0.85	1.2	0.5	1.2	0.5	1.2	V
		5.5			0.6	1.1	1.4	0.6	1.4	0.6	1.4	
V_H	Hysteresis Voltage	4.5			0.4	0.7	1.4	0.4	1.4	0.4	1.4	V
		5.5			0.4	0.7	1.5	0.4	1.5	0.4	1.5	
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND			-	±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				1		10		20	µA

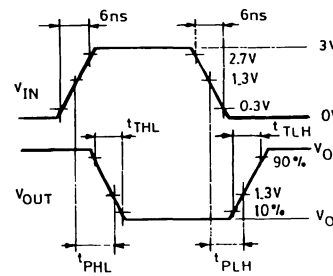
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			8	15		19		22	ns
t_{PLH} t_{PHL}	Propagation Delay Time	4.5			19	30		38		45	ns
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				45						pF

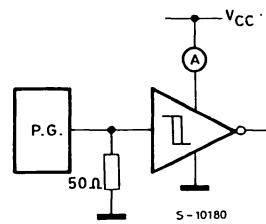
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST CIRCUIT





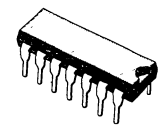
TEST CIRCUIT I_{CC} (Opr.)



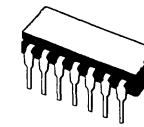
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

DUAL 4-INPUT NAND GATE

- HIGH SPEED
  t_{PD} = 8 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS20



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

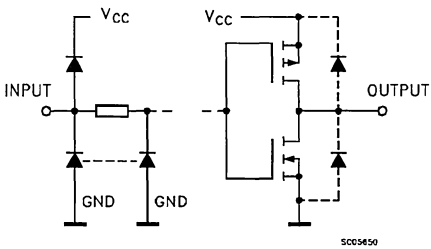
M54HC20F1R M74HC20M1R
M74HC20B1R M74HC20C1R

DESCRIPTION

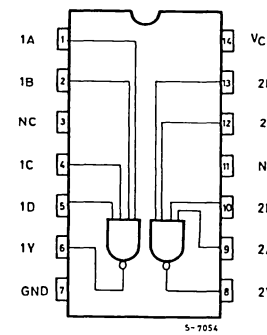
The M54/74HC20 is a high speed CMOS DUAL 4-INPUT NAND GATE fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

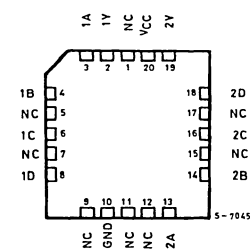
The internal circuit is composed of 3 stages including buffered output, which gives high noise immunity and a stable output. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



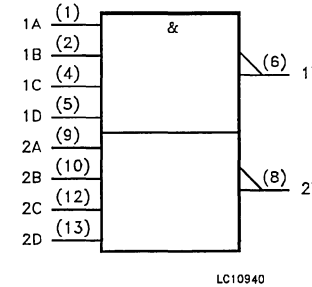


NC = No Internal Connection

TRUTH TABLE

A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

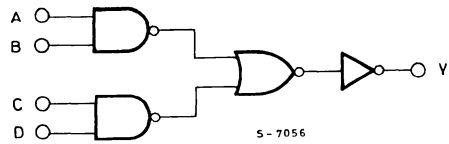
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 9	1A to 2A	Data Inputs
2, 10	1B to 2B	Data Inputs
3, 11	N. C.	Not Connected
4, 12	1C, 2C	Data Inputs
5, 13	1D, 2D	Data Inputs
6, 8	1Y to 2Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

SCHEMATIC CIRCUIT (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

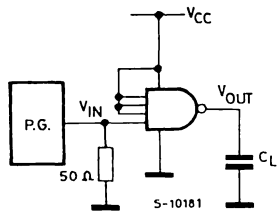
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	µA

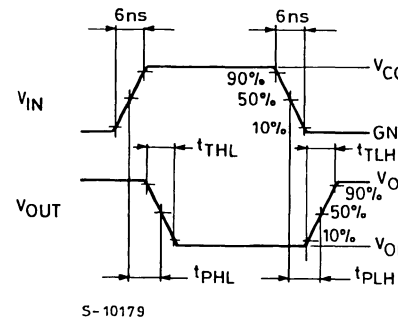
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			30	80		100		120	ns
		4.5			10	16		20		24	
		6.0			9	14		17		20	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				27						pF

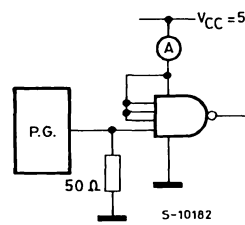
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT





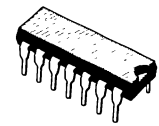
TEST CIRCUIT I_{CC} (Opr.)



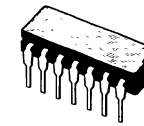
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

DUAL 4-INPUT AND GATE

- HIGH SPEED
  t_{PD} = 10 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS21



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HC21F1R M74HC21M1R
M74HC21B1R M74HC21C1R

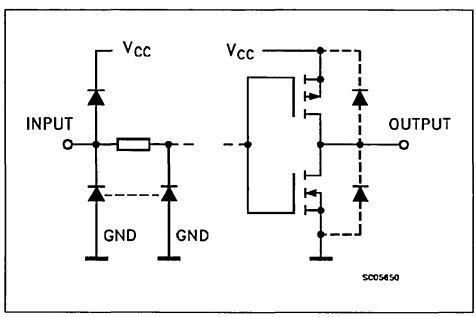
DESCRIPTION

The M54/74HC21 is a high speed CMOS DUAL 4-INPUT AND GATE fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

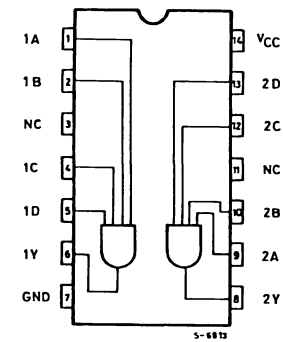
The internal circuits is composed of 3 stages including buffered output, which gives high noise immunity and a stable output.

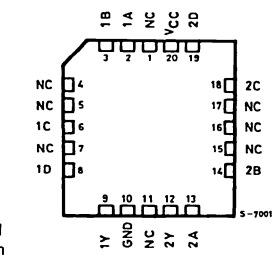
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



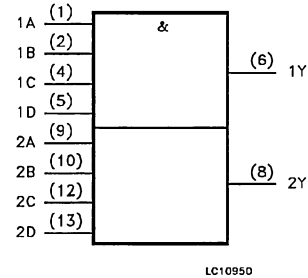


NC =
No Internal
Connection

TRUTH TABLE

A	B	C	D	Y
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

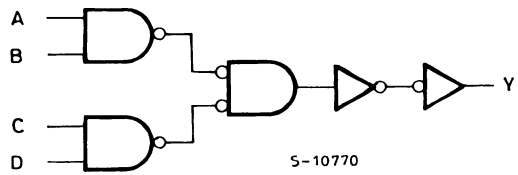
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 9	1A to 2A	Data Inputs
2, 10	1B to 2B	Data Inputs
3, 11	N C	Not Connected
4, 12	1C to 2C	Data Inputs
5, 13	1D to 2D	Data Inputs
6, 8	1Y to 2Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

SCHEMATIC CIRCUIT (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

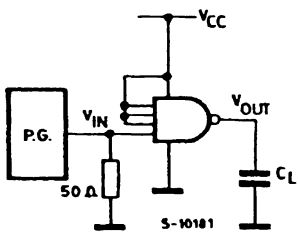
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	µA

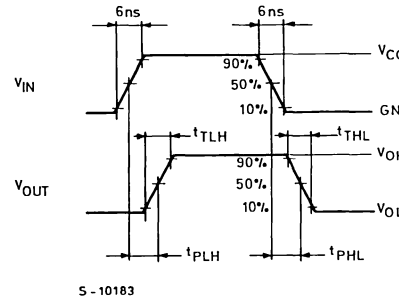
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			40	100		125		150	ns
		4.5			13	20		25		30	
		6.0			11	17		21		26	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				25						pF

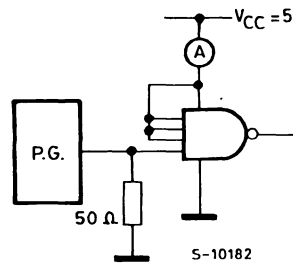
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT





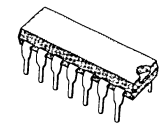
TEST CIRCUIT I_{CC} (Opr.)



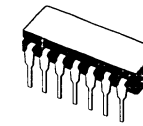
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TRIPLE 3-INPUT NOR GATE

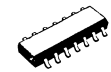
- HIGH SPEED
  t_{PD} = 7 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS27



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

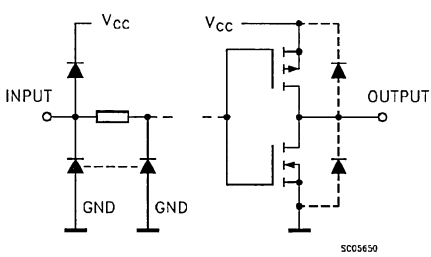
ORDER CODES :

M54HC27F1R M74HC27M1R
M74HC27B1R M74HC27C1R

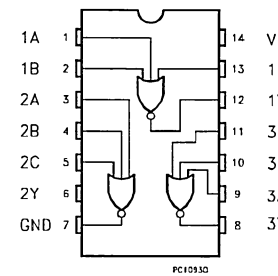
DESCRIPTION

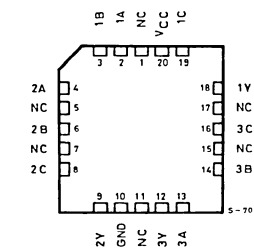
The M54/74HC27 is a high speed CMOS TRIPLE 3-INPUT NOR GATE fabricated in silicon gate C^2MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The internal circuit is composed of 3 stages including buffered output, which gives high noise immunity and a stable output. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



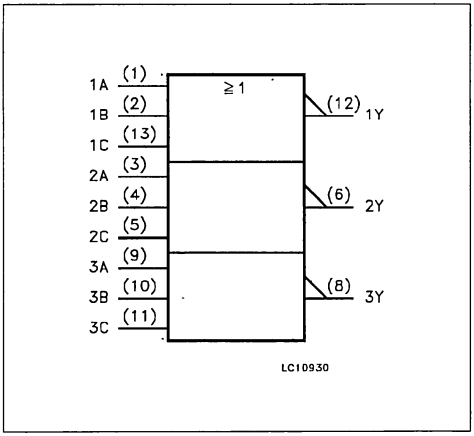


NC =
No Internal
Connection

TRUTH TABLE

A	B	C	Y
L	L	L	H
H	X	X	L
X	H	X	L
X	X	H	L

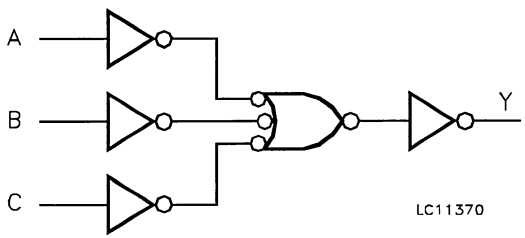
IEC Logic Symbol



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A to 3A	Data Inputs
2, 4, 10	1B to 3B	Data Inputs
13, 5, 11	1C to 3C	Data Inputs
12, 6, 8	1Y to 3Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

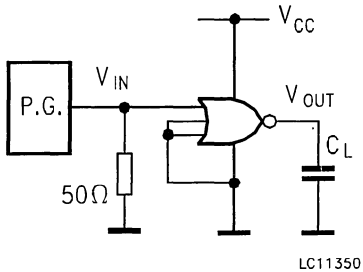
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	µA

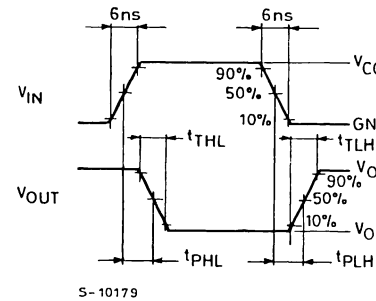
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			30	80		100		115	ns
		4.5			10	16		20		23	
		6.0			9	14		17		20	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				26						pF

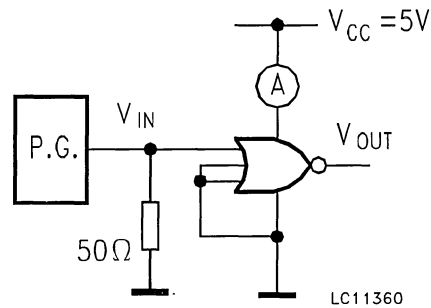
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/3$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT





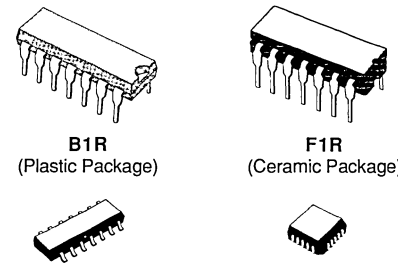
TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAVE AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TRIPLE 3-INPUT NOR GATE

- HIGH SPEED
  t_{PD} = 9 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS27



B1R (Plastic Package)

F1R (Ceramic Package)

M1R (Micro Package)

C1R (Chip Carrier)

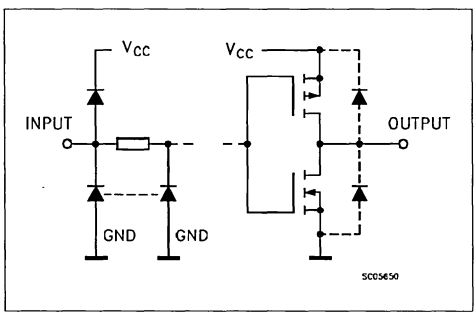
ORDER CODES :

M54HCT27F1R M74HCT27M1R
M74HCT27B1R M74HCT27C1R

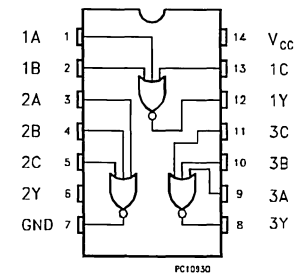
DESCRIPTION

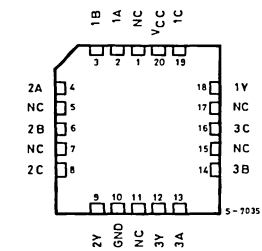
The M54/74HCT27 is a high speed CMOS TRIPLE 3-INPUT NOR GATE fabricated in silicon gate C^2MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The internal circuit is composed of 3 stages including buffered output, which gives high noise immunity and a stable output. All inputs are equipped with protection circuits against static discharge and transient excess voltage. This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



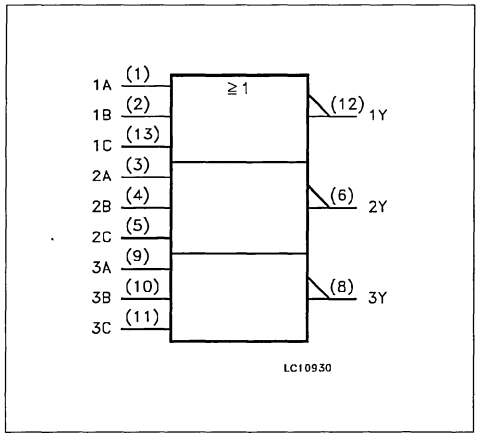


NC = No Internal Connection

TRUTH TABLE

A	B	C	Y
L	L	L	H
H	X	X	L
X	H	X	L
X	X	H	L

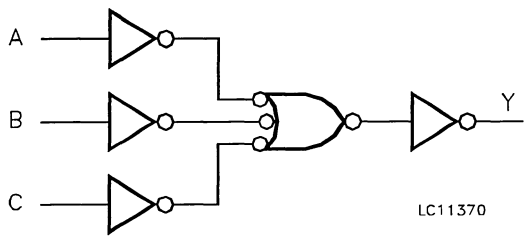
IEC Logic Symbol



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A to 3A	Data Inputs
2, 4, 10	1B to 3B	Data Inputs
13, 5, 11	1C to 3C	Data Inputs
12, 6, 8	1Y to 3Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

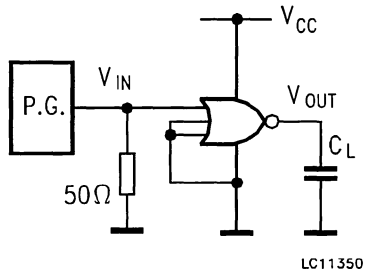
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				1		10		20	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9		3.0	mA

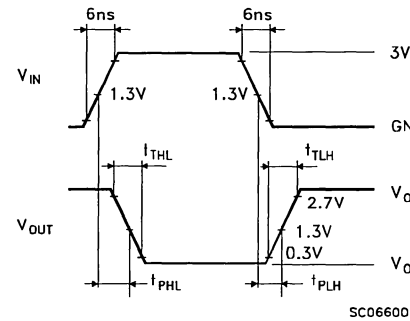
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			8	15		19		22	ns
t_{PLH} t_{PHL}	Propagation Delay Time	4.5			12	19		24		29	ns
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				48						pF

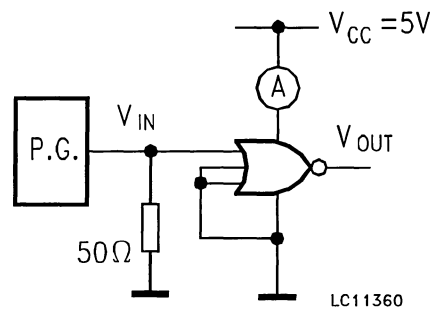
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/3$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT





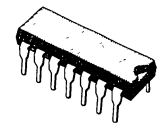
TEST CIRCUIT I_{CC} (Opr.)



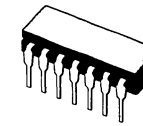
INPUT WAVEFORM IS THE SAVE AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

8 INPUT NAND GATE

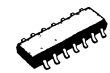
- HIGH SPEED
  t_{PD} = 12 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS30



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HC30F1R M74HC30M1R
M74HC30B1R M74HC30C1R

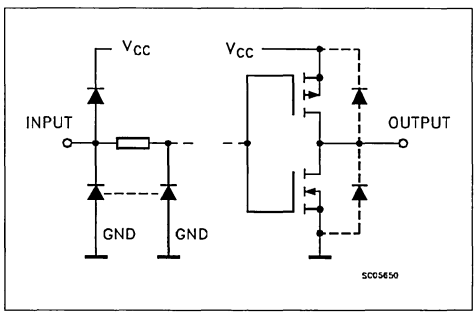
DESCRIPTION

The M54/74HC30 is a high speed CMOS 8-INPUT NAND GATE fabricated with silicon gate C^2MOS technology.

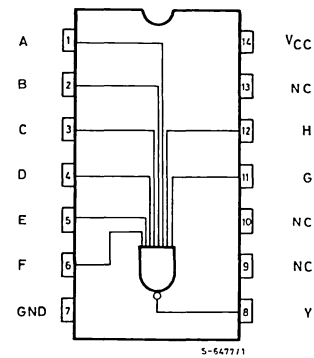
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The internal circuit is composed of 5 stages including buffer output, which gives high noise immunity and stable output.

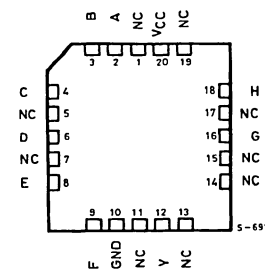
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



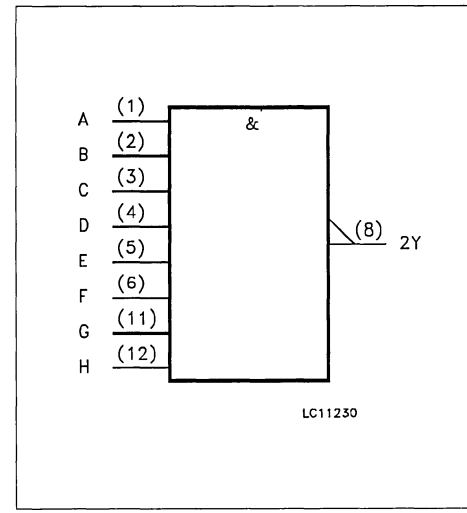


NC =
No Internal
Connection

TRUTH TABLE

A	B	C	D	E	F	G	H	Y
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

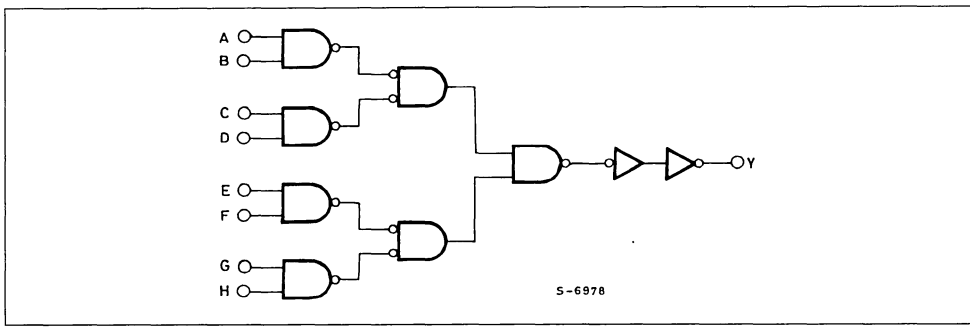
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 11, 12	A, B, C, D, E, F, G, H	Data Inputs
9, 10, 13	NC	Not connected
8	Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

SCHEMATIC CIRCUIT (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

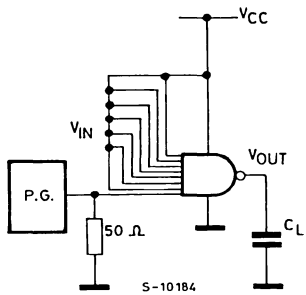
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	µA

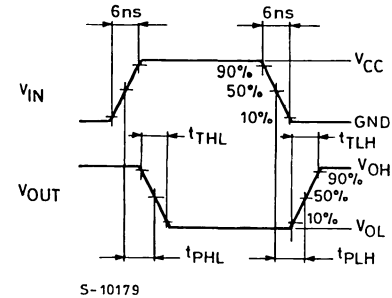
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			45	115		145		170	ns
		4.5			15	23		29		34	
		6.0			13	20		25		29	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				20						pF

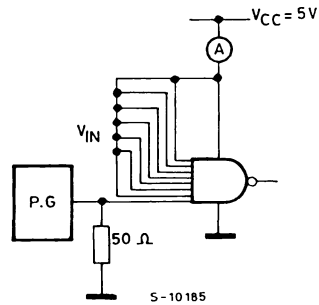
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST CIRCUIT





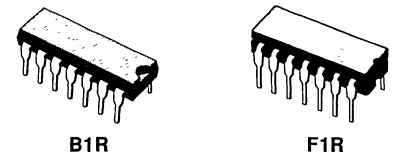
TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

8 INPUT NAND GATE

- HIGH SPEED
  t_{PD} = 15 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS30



B1R (Plastic Package)

F1R (Ceramic Package)

M1R (Micro Package)

C1R (Chip Carrier)

ORDER CODES :

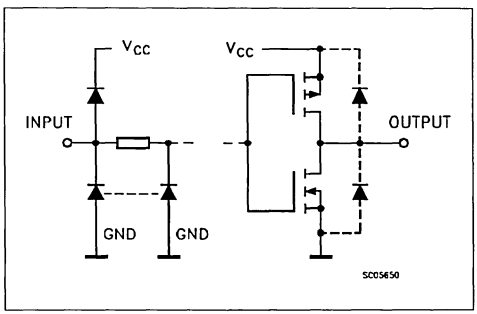
M54HCT30F1R M74HCT30M1R
M74HCT30B1R M74HCT30C1R

DESCRIPTION

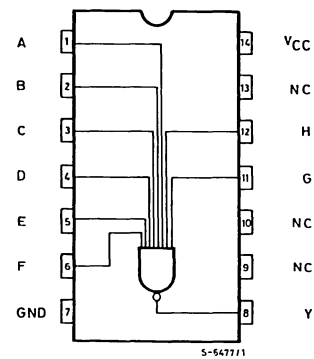
The M54/74HCT30 is a high speed CMOS 8-INPUT NAND GATE fabricated with silicon gate C^2MOS technology.

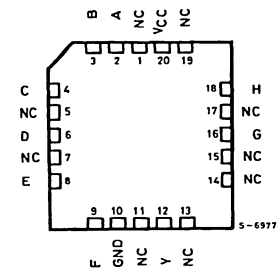
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The internal circuit is composed of 5 stages including buffer output, which gives high noise immunity and stable output. All inputs are equipped with protection circuits against static discharge and transient excess voltage.This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



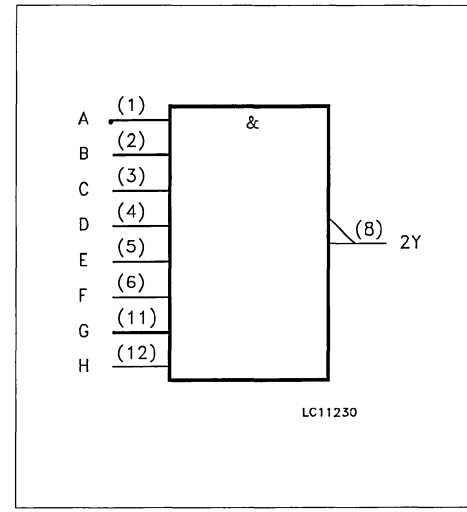


NC = No Internal Connection

TRUTH TABLE

A	B	C	D	E	F	G	H	Y
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

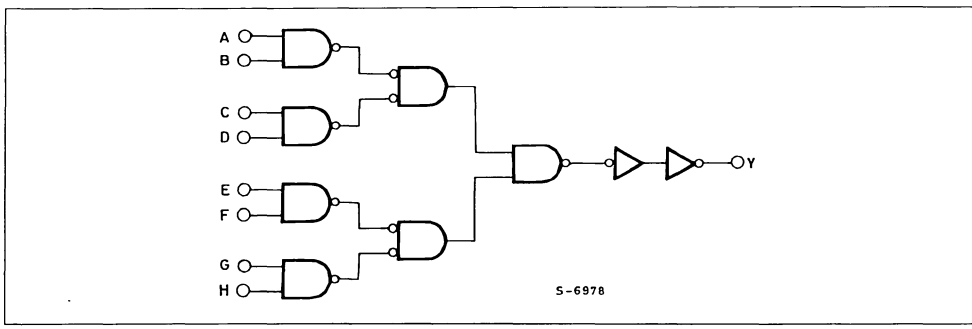
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 11, 12	A, B, C, D, E, F, G, H	Data Inputs
9, 10, 13	NC	Not connected
8	Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

SCHEMATIC CIRCUIT (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

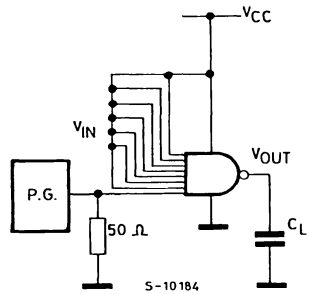
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				1		10		20	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9		3.0	mA

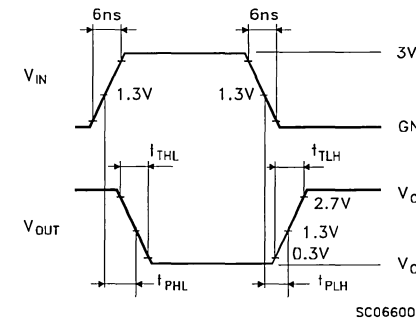
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			8	15		19		22	ns
t_{PLH} t_{PHL}	Propagation Delay Time	4.5			18	28		35		42	ns
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				34						pF

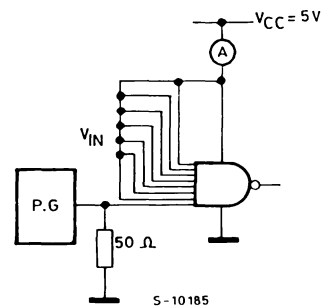
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST CIRCUIT





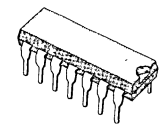
TEST CIRCUIT I_{CC} (Opr.)



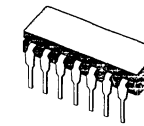
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

QUAD 2-INPUT OR GATE

- HIGH SPEED
  t_{PD} = 6 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS32



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

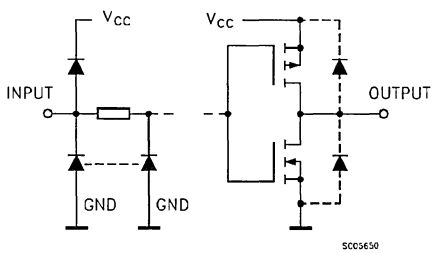
ORDER CODES :

M54HC32F1R M74HC32M1R
M74HC32B1R M74HC32C1R

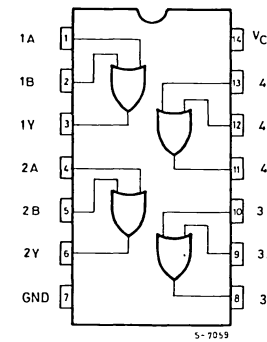
DESCRIPTION

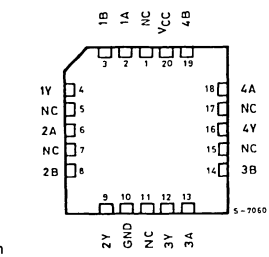
The M54/74HC32 is a high speed CMOS 2-INPUT OR GATE fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The internal circuit is composed of 2 stages including buffered output, which gives high noise immunity and a stable output. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



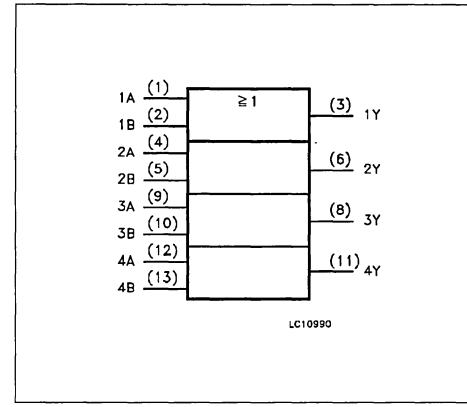


NC =
No Internal
Connection

TRUTH TABLE

A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

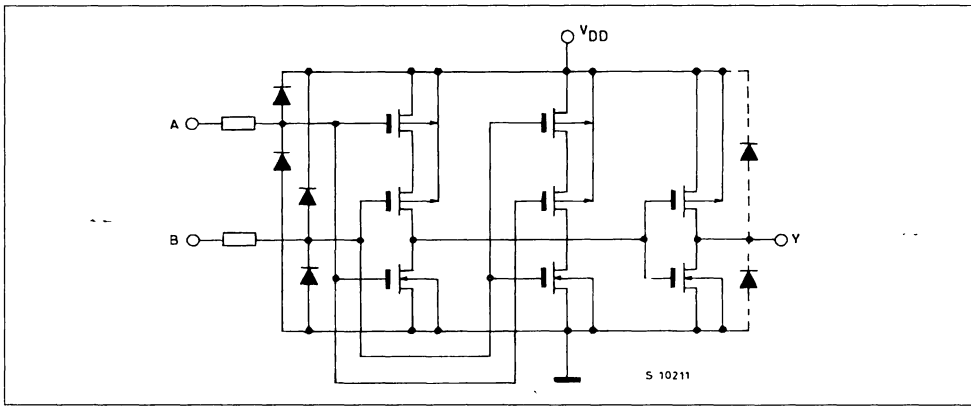
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data Inputs
2, 5, 10, 13	1B to 4B	Data Inputs
3, 6, 8, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

SCHEMATIC CIRCUIT (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

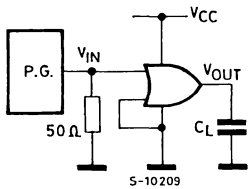
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	µA

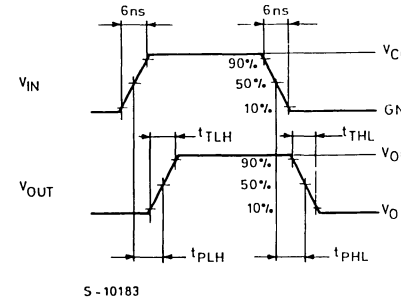
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			24	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				21						pF

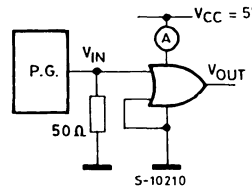
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT





TEST CIRCUIT I_{CC} (Opr.)

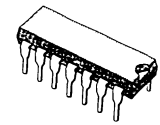


INPUT WAVEFORM IS THE SAVE AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

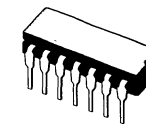
M54HCT32
M74HCT32

QUAD 2-INPUT OR GATE

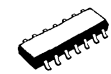
- HIGH SPEED
  t_{PD} = 12 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS32



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

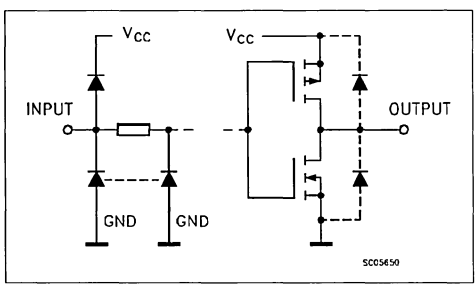
M54HCT32F1R M74HCT32M1R
M74HCT32B1R M74HCT32C1R

DESCRIPTION

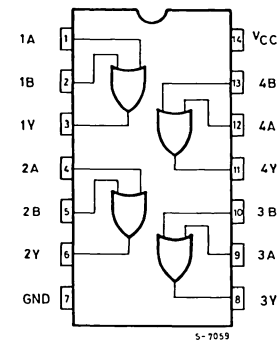
The M54/74HCT32 is a high speed CMOS 2-INPUT OR GATE fabricated in silicon gate C2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The internal circuit is composed of 2 stages including buffered output, which gives high noise immunity and a stable output. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

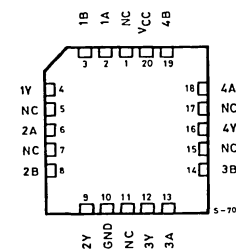
This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



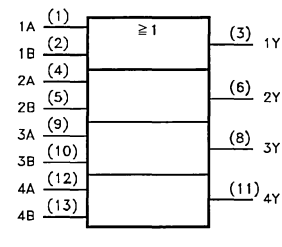


NC =
No Internal
Connection

TRUTH TABLE

A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

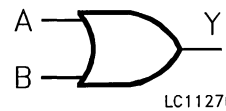
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data Inputs
2, 5, 10, 13	1B to 4B	Data Inputs
3, 6, 8, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

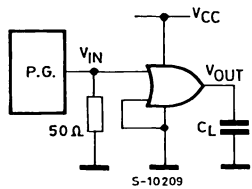
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.40	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				1		10		20	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9		3.0	mA

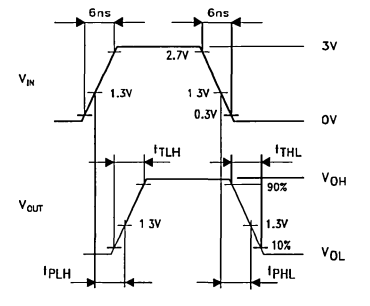
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			8	15		19		23	ns
t_{PLH} t_{PHL}	Propagation Delay Time	4.5			13	21		26		32	ns
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				39						pF

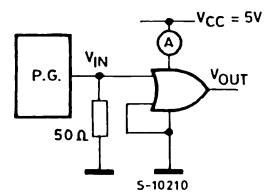
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT





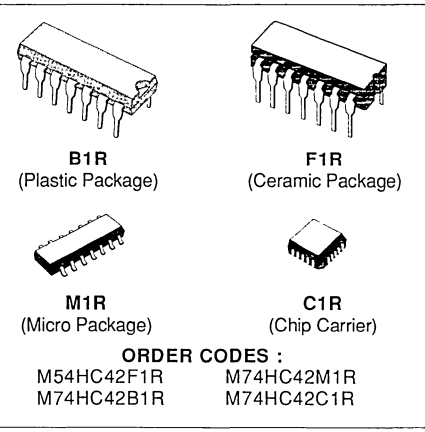
TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAVE AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

BCD TO DECIMAL DECODER

- HIGH SPEED
  t_{PD} = 13 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS42



B1R
(Plastic Package)

F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

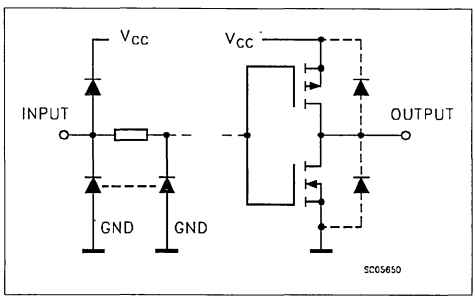
ORDER CODES :

M54HC42F1R M74HC42M1R
M74HC42B1R M74HC42C1R

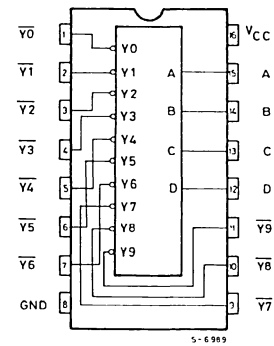
DESCRIPTION

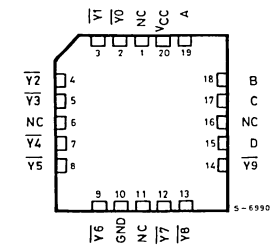
The M54/74HC42 is a high speed CMOS BCD-TO-DECIMAL DECODER fabricated in silicon gate C^2MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. A BCD code applied to the four inputs A-D selects one of ten decimal outputs $\overline{Y0}$-$\overline{Y9}$, which goes low to fifteen gives a high level at all outputs. This device also can be used as a 3-to-8 LINE DECODER, when the D input is assigned as a disable input. This device is useful for code conversion, address decoding, memory selection, demultiplexing, or readout decoding.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



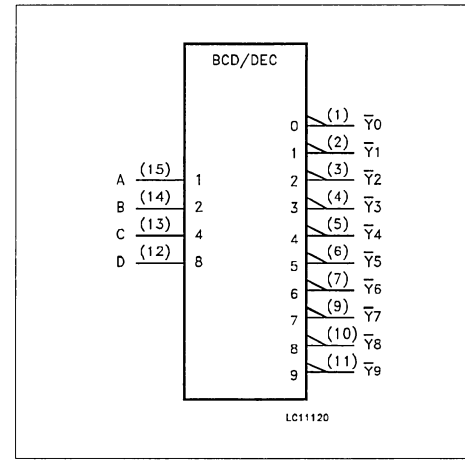


NC =
No Internal
Connection

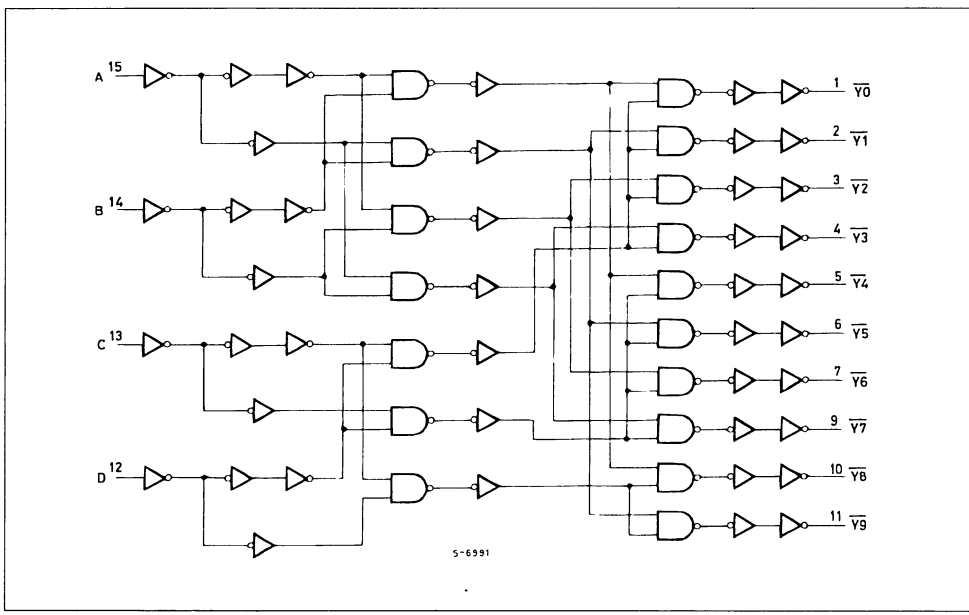
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
15, 14, 13, 12	A, B, C, D	Data Inputs
1, 2, 3, 4, 5, 6, 7, 9, 10, 11	$\overline{Y}_0$ to $\overline{Y}_9$	Multiplexer Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



LOGIC DIAGRAM



FUNCTIONAL TABLE

CODE No.	BCD INPUTS				DECIMAL OUTPUTS									
	D	C	B	A	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$	$\overline{Y}_8$	$\overline{Y}_9$
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
10	H	L	H	L	H	H	H	H	H	H	H	H	H	H
11	H	L	H	H	H	H	H	H	H	H	H	H	H	H
12	H	H	L	L	H	H	H	H	H	H	H	H	H	H
13	H	H	L	H	H	H	H	H	H	H	H	H	H	H
14	H	H	H	L	H	H	H	H	H	H	H	H	H	H
15	H	H	H	H	H	H	H	H	H	H	H	H	H	H

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied

(*) 500 mW. ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

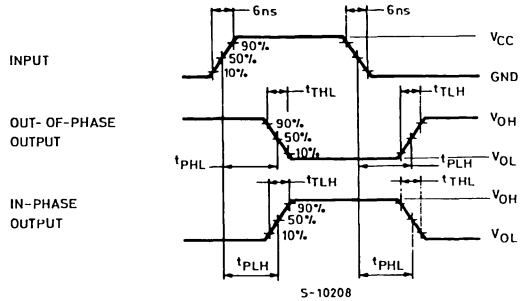
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1 35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

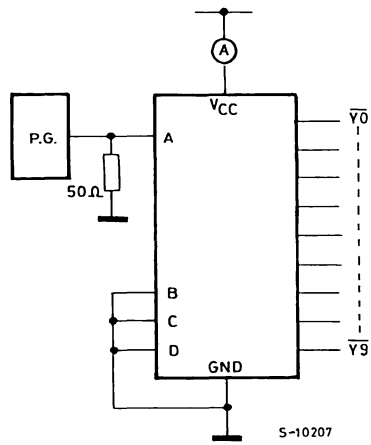
Symbol	Parameter	Test Conditions		Value						Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC	
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			64	130		165		195	ns
		4.5			16	26		33		39	
		6.0			14	22		28		33	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				60						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



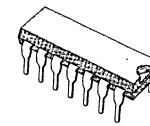
TEST CIRCUIT Icc (Opr.)



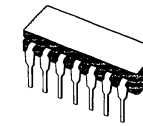
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTIC TEST

DUAL 2 WIDE 2 INPUT AND/OR INVERT GATE

- HIGH SPEED
  t_{PD} = 10 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS51



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

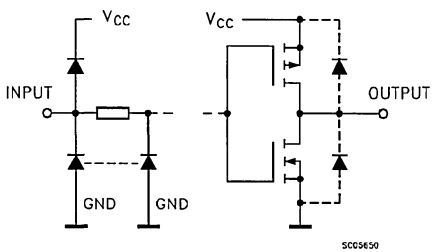
M54HC51F1R	M74HC51M1R
M74HC51B1R	M74HC51C1R

DESCRIPTION

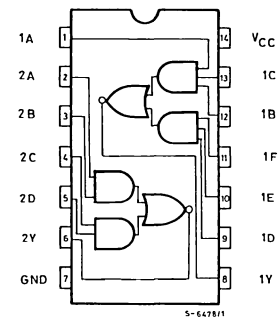
The M54/74HC51 is a high speed CMOS DUAL 2 WIDE-2 INPUT AND/OR INVERT GATE fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. It contains a 2-WIDE 2-INPUT AND-OR-INVERT GATE and a 2-WIDE 3-INPUT AND-OR-INVERT GATE.

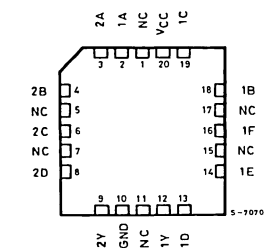
The internal circuit is composed of 3 stages (2-INPUT) or 5 stages (3-INPUT) including buffered output, which gives high noise immunity and a stable output. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



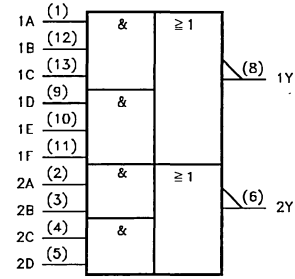


NC =
No Internal
Connection

PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 12, 13, 9, 10, 11	1A to 1F	Data Inputs
2, 3, 4, 5	2A to 2D	Data Inputs
8, 6	1Y, 2Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



TRUTH TABLE

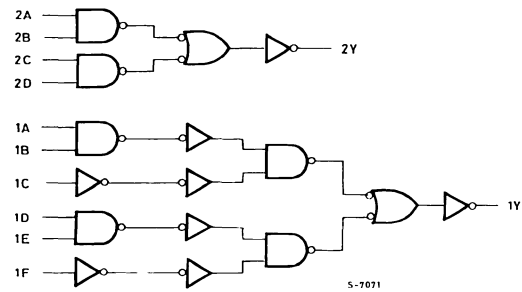
1A	1B	1C	1D	1E	1F	1Y
H	H	H	X	X	X	L
X	X	X	H	H	H	L
ALL OTHER COMBINATIONS						H

TRUTH TABLE

2A	2B	2C	2D	2Y
H	H	X	X	L
X	X	H	H	L
ALL OTHER COMBINATIONS				H

X = DON'T CARE

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW. ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

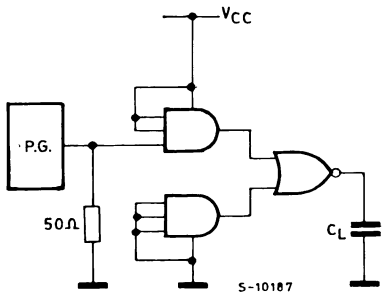
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	µA

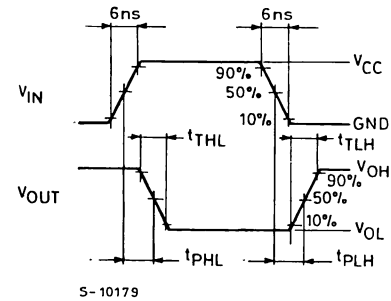
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			39	100		125		150	ns
		4.5			13	20		25		30	
		6.0			11	17		21		26	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				32						pF

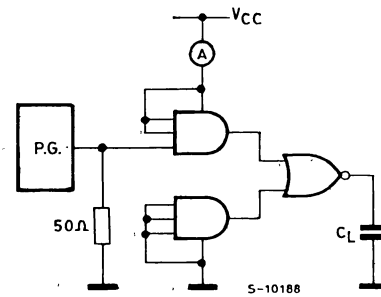
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST CIRCUIT





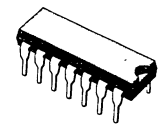
TEST CIRCUIT I_{CC} (Opr.)



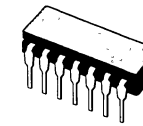
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

DUAL J-K FLIP FLOP WITH PRESET AND CLEAR

- HIGH SPEED
  f_{MAX} = 75 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 2 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS73



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

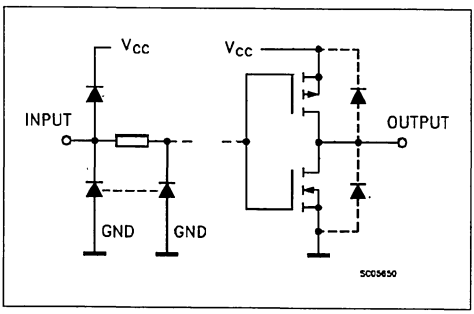
ORDER CODES :

M54HC73F1R M74HC73M1R
M74HC73B1R M74HC73C1R

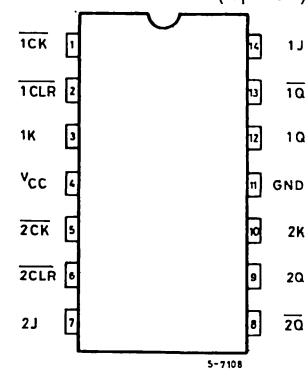
DESCRIPTION

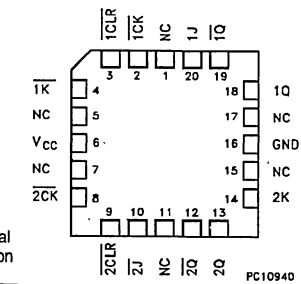
The M54/74HC73 is a high speed CMOS DUAL J-K FLIP FLOP WITH CLEAR fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. Depending on the logic level applied to J and K inputs, this device changes state on the negative going transition of clock input pulse ($\overline{CK}$). The clear function is accomplished independently of the clock condition when the clear input ($\overline{CLR}$) is taken low. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





TRUTH TABLE

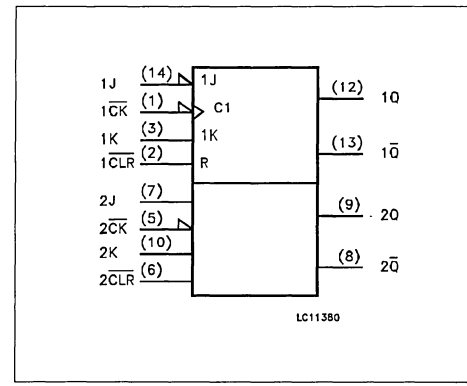
INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	X	X	X	L	H	CLEAR
H	L	L	⌐	Q_n	$\overline{Q}_n$	NO CHANGE
H	L	H	⌐	L	H	--
H	H	L	⌐	H	L	--
H	H	H	⌐	$\overline{Q}_n$	Q_n	TOGGLE
H	X	X	⌙	Q_n	$\overline{Q}_n$	NO CHANGE

X: Don't Care

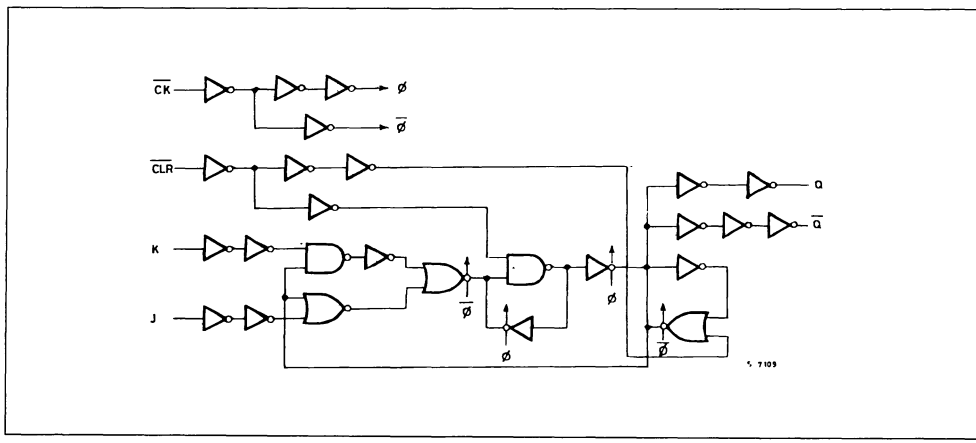
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 5	$1\overline{CK}$, $2\overline{CK}$	Clock Input
2, 6	$1\overline{CLR}$, $2\overline{CLR}$	Asyncronous Reset Inputs
12, 9	1Q, 2Q	True Flip-Flop Outputs
13, 8	$1\overline{Q}$, $2\overline{Q}$	Complement Flip-Flop Outputs
14, 7, 3, 10	1J, 2J, 1K, 2K	Synchronous Inputs; Flip-Flop 1 And 2
11	GND	Ground (0V)
4	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series		-55 to +125	°C
	M74HC Series		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

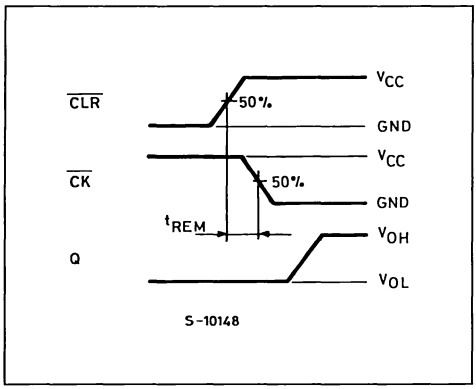
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				2		20		40	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

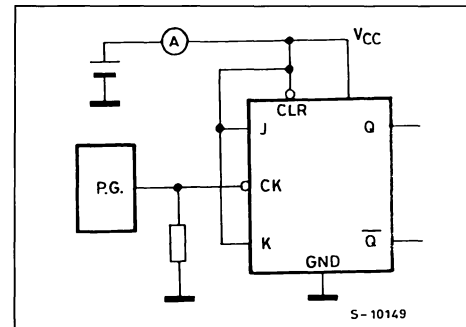
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLOCK}$ - Q)	2.0			42	125		155		190	ns
		4.5			14	25		31		38	
		6.0			12	21		26		32	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$ - Q)	2.0			54	145		180		220	ns
		4.5			18	29		36		44	
		6.0			15	25		31		37	
f_{MAX}	Maximum Clock Frequency	2.0		6	15		4.8		4		MHz
		4.5		30	60		24		20		
		6.0		35	80		28		24		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width ($\overline{CLOCK}$)	2.0			18	75		95		110	ns
		4.5			6	15		19		22	
		6.0			6	13		16		19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLEAR}$)	2.0			21	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
t_s	Minimum Set-up Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			6	13		16		19	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Minimum Removal Time	2.0			25	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				35						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per FLIP/FLOP)

SWITCHING CHARACTERISTICS TEST

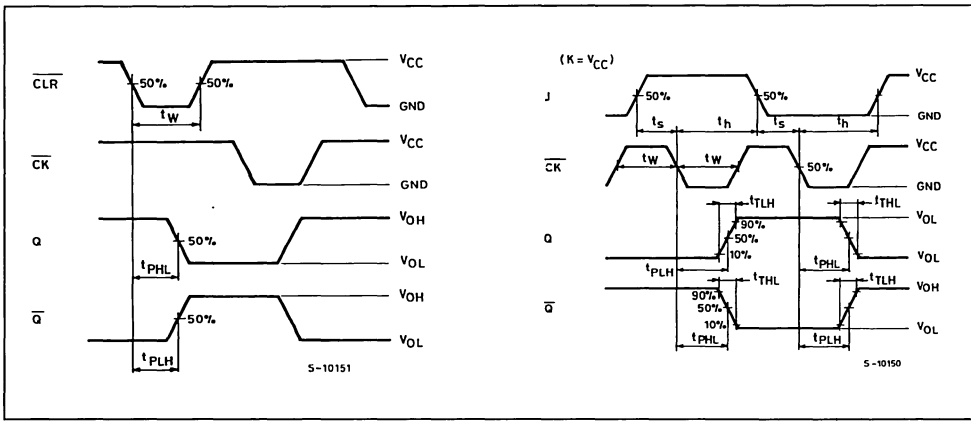


TEST CIRCUIT I_{CC} (Opr.)



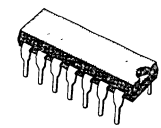
INPUT WAVEFORM IS THE SAVE AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SWITCHING CHARACTERISTICS TEST WAVEFORM

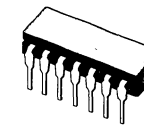


DUAL D TYPE FLIP FLOP WITH PRESET AND CLEAR

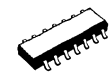
- HIGH SPEED
  f_{MAX} = 71 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 2 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS74



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

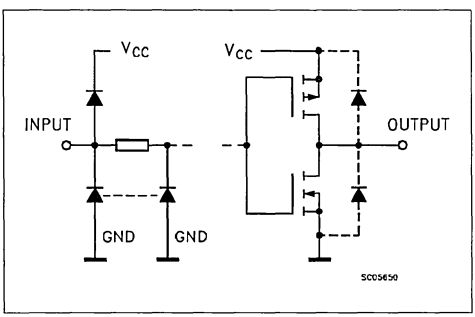
ORDER CODES :

M54HC74F1R M74HC74M1R
M74HC74B1R M74HC74C1R

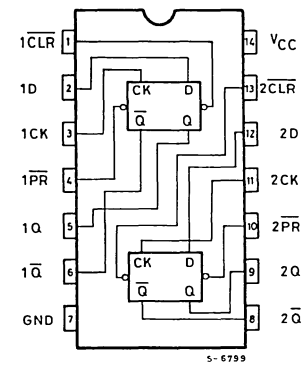
DESCRIPTION

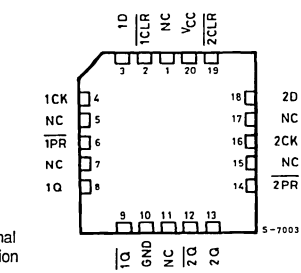
The M54/74HC74 is a high speed CMOS DUAL D TYPE FLIP FLOP WITH PRESET AND CLEAR fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. A signal on the D INPUT is transferred to the Q OUTPUT during the positive going transition of the clock pulse. CLEAR and PRESET are independent of the clock and accomplished by a low on the appropriate input. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





NC =
No Internal
Connection

TRUTH TABLE

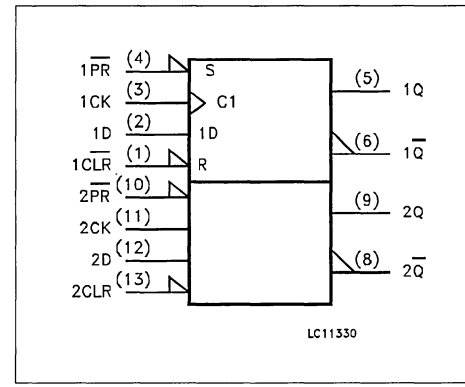
INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	
H	H	L	⌐¬	L	H	
H	H	H	⌐¬	H	L	
H	H	X	¬⌐	Q_n	$\overline{Q}_n$	NO CHANGE

X: Don't Care

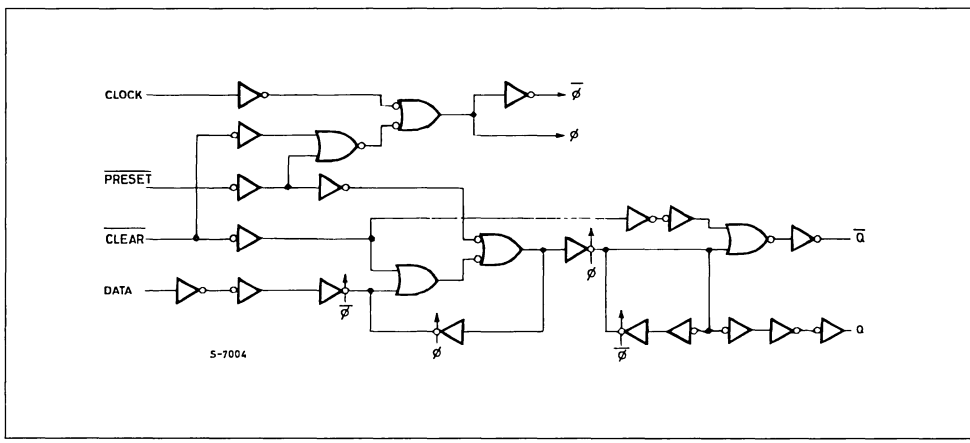
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 13	$1\overline{CLR}$, $2\overline{CLR}$	Asyncronous Reset - Direct Input
2, 12	1D, 2D	Data Inputs
3, 11	1CK, 2CK	Clock Input (LOW-to-HIGH, Edge-Triggered)
4, 10	$1\overline{PR}$, $2\overline{PR}$	Asyncronous Set - Direct Input
5, 9	1Q, 2Q	True Flip-Flop Outpus
6, 8	$1\overline{Q}$, $2\overline{Q}$	Complement Flip-Flop Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied

(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series		-55 to +125	°C
	M74HC Series		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

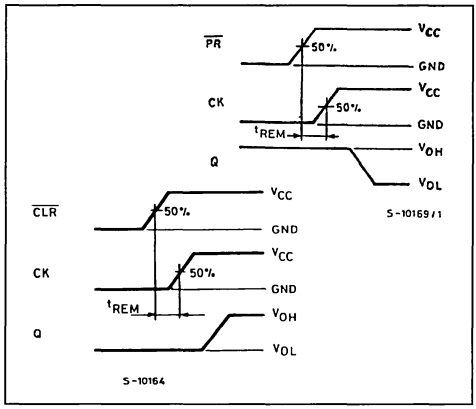
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				2		20		40	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

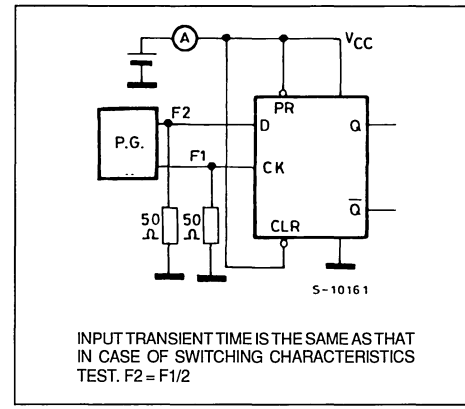
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q)	2.0			48	150		190		225	ns
		4.5			16	30		38		45	
		6.0			13	26		32		38	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CL}$, PR - Q)	2.0			51	150		190		225	ns
		4.5			17	30		38		45	
		6.0			15	26		32		38	
f_{MAX}	Maximum Clock Frequency	2.0		6.2	21		5		4.2		MHz
		4.5		31	63		25		21		
		6.0		37	67		30		25		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0			18	75		95		110	ns
		4.5			6	15		19		22	
		6.0			6	13		16		19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CL}$, $\overline{PR}$)	2.0			21	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
t_s	Minimum Set-up Time	2.0			15	75		95		110	ns
		4.5			4	15		19		22	
		6.0			3	13		16		19	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Minimum Removal Time ($\overline{CL}$, $\overline{PR}$)	2.0			0	25		30		35	ns
		4.5			0	5		6		7	
		6.0			0	4		5		6	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				34						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per FLIP/FLOP)

SWITCHING CHARACTERISTICS TEST WAVEFORM

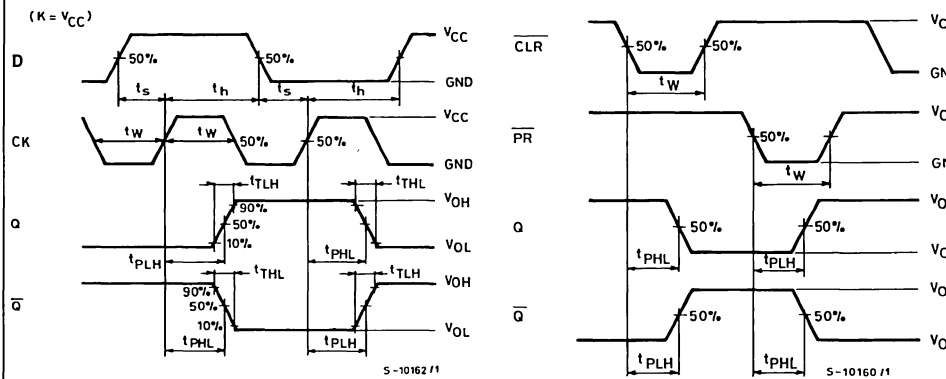


TEST CIRCUIT I_{CC} (Opr.)



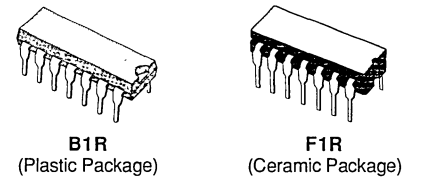
INPUT TRANSIENT TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST. F2 = F1/2

SWITCHING CHARACTERISTICS TEST WAVEFORM (K = V_{CC})



DUAL D TYPE FLIP FLOP WITH PRESET AND CLEAR

- HIGH SPEED
  f_{MAX} = 53 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 2 µA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS74



B1R
(Plastic Package)

F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

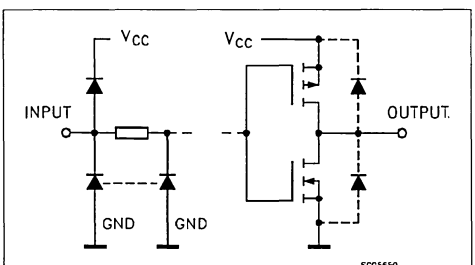
ORDER CODES :

M54HCT74F1R M74HCT74M1R
M74HCT74B1R M74HCT74C1R

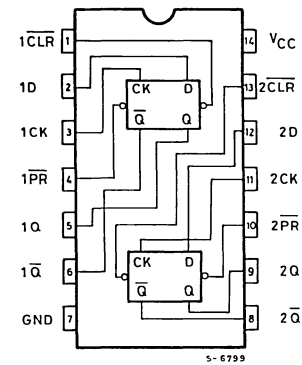
DESCRIPTION

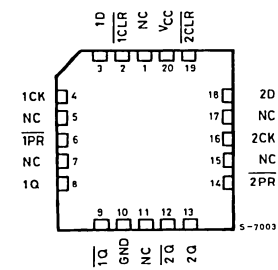
The M54/74HCT74 is a high speed CMOS DUAL D TYPE FLOP WITH PRESET AND CLEAR fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. A signal on the D INPUT is transferred to the Q OUTPUT during the positive going transition of the clock pulse. CLEAR and PRESET are independent of the clock and accomplished by a low on the appropriate input. All inputs are equipped with protection circuits against static discharge and transient excess voltage. This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





NC =
No Internal
Connection

TRUTH TABLE

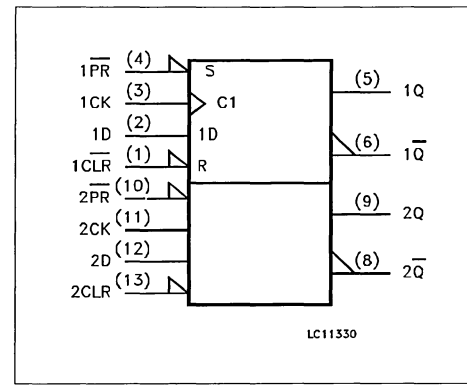
INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	
H	H	L	⌐	L	H	
H	H	H	⌐	H	L	
H	H	X	⌙	Q_n	$\overline{Q}_n$	NO CHANGE

X: Don't Care

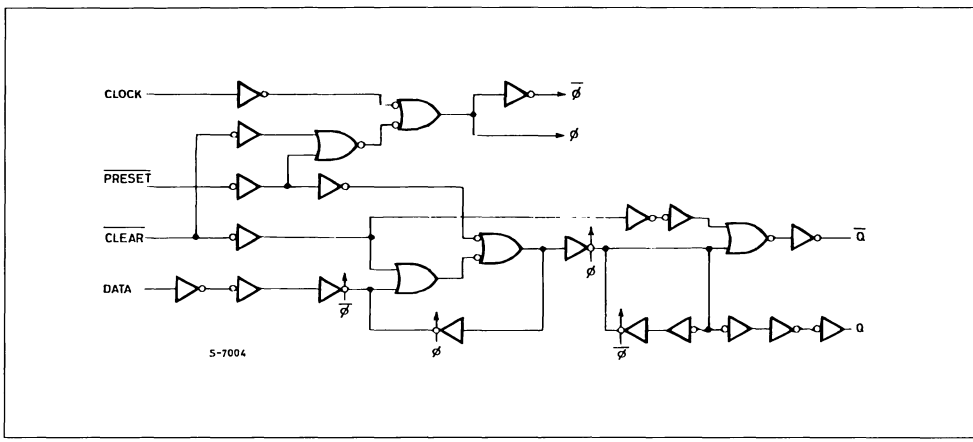
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 13	$1\overline{CLR}$, 2CLR	Asyncronous Reset - Direct Input
2, 12	1D, 2D	Data Inputs
3, 11	1CK, 2CK	Clock Input (LOW-to-HIGH, Edge-Triggered)
4, 10	$1\overline{PR}$, $2\overline{PR}$	Asyncronous Set - Direct Input
5, 9	1Q, 2Q	True Flip-Flop Outpus
6, 8	$1\overline{Q}$, $2\overline{Q}$	Complement Flip-Flop Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur Functional operation under these condition is not implied

(*) 500 mW. ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

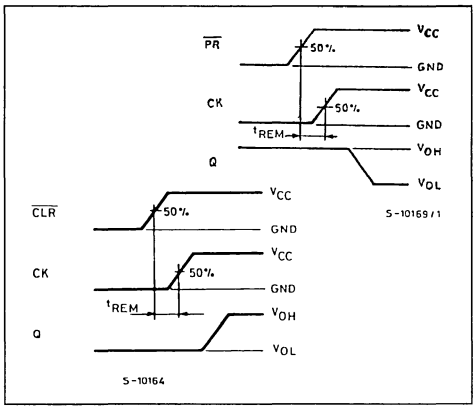
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				2		20		40	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9		3.0	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

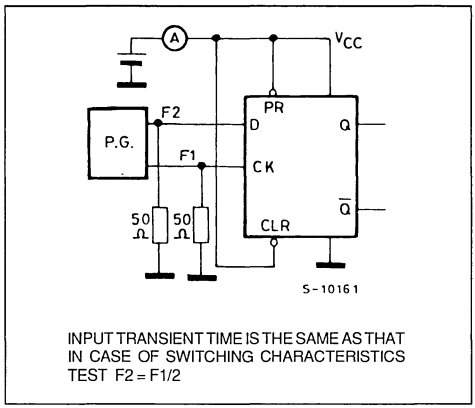
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			8	15		19		22	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q)	4.5			21	33		41		50	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CL}$, $\overline{PR}$ - Q, $\overline{Q}$)	4.5			18	30		38		45	ns
f_{MAX}	Maximum Clock Frequency	4.5		27	48		22		18		MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	4.5			6	15		19		23	ns
$t_{W(L)}$	Minimum Pulse Width ($\overline{CL}$, $\overline{PR}$)	4.5			8	15		19		23	ns
t_s	Minimum Set-up Time	4.5			7	15		19		23	ns
t_h	Minimum Hold Time	4.5				0		0		0	ns
t_{REM}	Minimum Removal Time ($\overline{CL}$, $\overline{PR}$)	4.5			1	5	5	6	5	8	ns
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				32						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit) Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per FLIP/FLOP)

SWITCHING CHARACTERISTICS TEST WAVEFORM

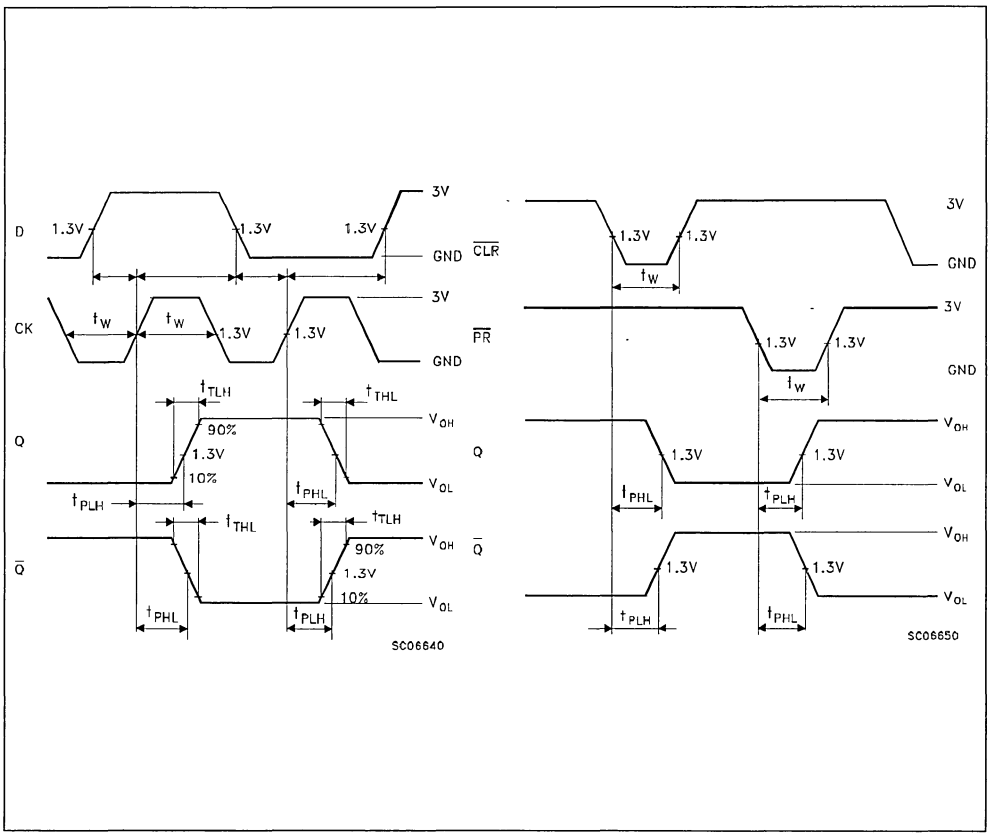


TEST CIRCUIT I_{CC} (Opr.)



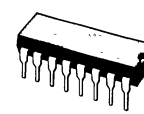
INPUT TRANSIENT TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST F2 = F1/2

SWITCHING CHARACTERISTICS TEST WAVEFORM

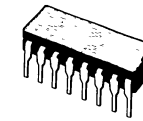


4 BIT D TYPE LATCH

- HIGH SPEED
  t_{PD} = 10 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 2 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} = (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS75



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

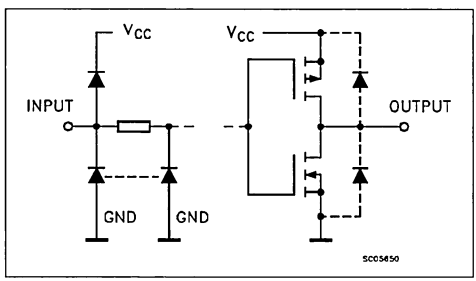
ORDER CODES :

M54HC75F1R M74HC75M1R
M74HC75B1R M74HC75C1R

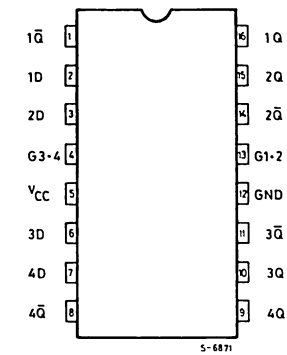
DESCRIPTION

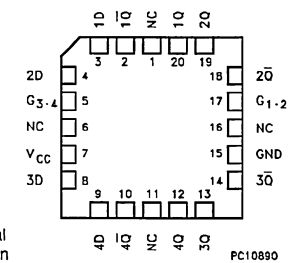
The M54/74HC75 is a high speed CMOS 4-BIT D-TYPE LATCH fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. It contains two groups of 2-bit latches controlled by an enable input (G1•2 or G3•4). These two latch groups can be used in different circuits. Each latch has Q and $\overline{Q}$ outputs (1Q - 4$\overline{Q}$ and 1Q - 4$\overline{Q}$). The data applied to the data input is transfered to the Q and $\overline{Q}$ outputs when the enable input is taken high and the outputs will follow the data input as long as the enable input is kept high. When the enable input is taken low, the information data applied to the data input is retained at the outputs. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



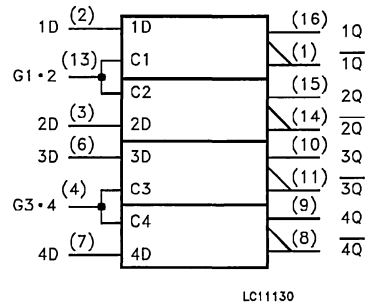


NC =
No Internal
Connection

TRUTH TABLE

INPUTS		OUTPUTS		FUNCTION
D	G	Q	$\overline{Q}$	
L	H	L	H	
H	H	H	L	
X	L	Qn	$\overline{Q}$n	LATCH

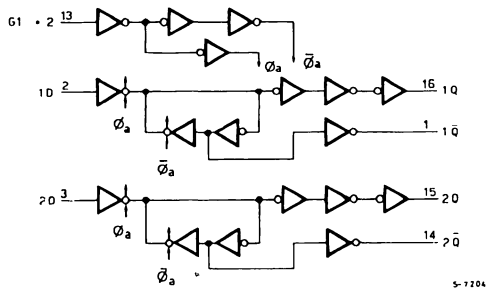
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 14, 11, 8	1$\overline{Q}$ to 4$\overline{Q}$	Complementary Latch Outputs
2, 3, 6, 7	1D to 4D	Data Inputs
4	G3 • 4	Latch Enable Input, latches 3 and 4
13	G1 • 2	Latch Enable Input, latches 1 and 2
16, 15, 10, 9	1Q to 4Q	Latch Outputs
12	GND	Ground (0V)
5	V_{CC}	Positive Supply Voltage

SCHEMATIC CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

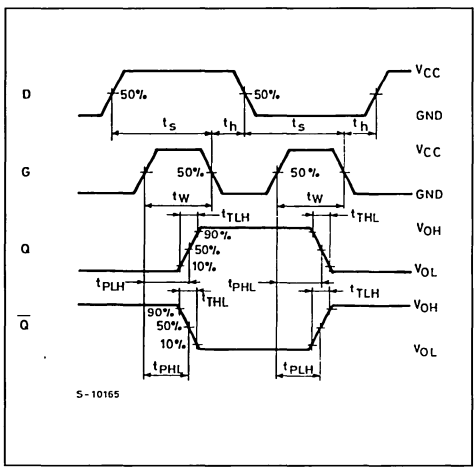
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				2		20		40	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

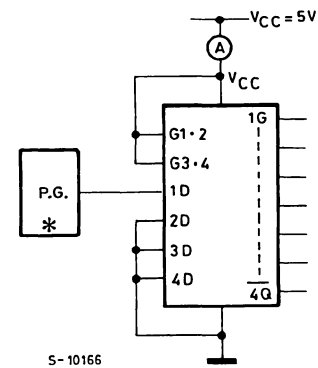
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			25	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (DATA-Q)	2.0			36	110		140		165	ns
		4.5			12	22		28		33	
		6.0			10	19		24		28	
t_{PLH} t_{PHL}	Propagation Delay Time (G-Q)	2.0			40	125		155		190	ns
		4.5			13	25		31		38	
		6.0			11	21		26		32	
$t_{W(H)}$	Minimum Pulse Width (G)	2.0			18	75		95		110	ns
		4.5			6	15		19		22	
		6.0			6	13		16		19	
t_s	Minimum Set-up Time	2.0				50		65		75	ns
		4.5				10		13		15	
		6.0				9		11		13	
t_h	Minimum Hold Time	2.0				25		30		40	ns
		4.5				5		6		8	
		6.0				4		5		7	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				30						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



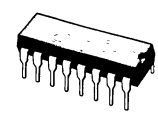
TEST CIRCUIT I_{CC} (Opr)



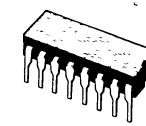
* INPUT WAVEFORM IS THE SAVE AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

4 BIT D TYPE LATCH

- HIGH SPEED
  t_{PD} = 15 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 2 μA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2 V (MIN.) V_{IL} = 0.8 V (MAX.)
- OUTPUT DRIVE CAPABILITY 10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS75



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

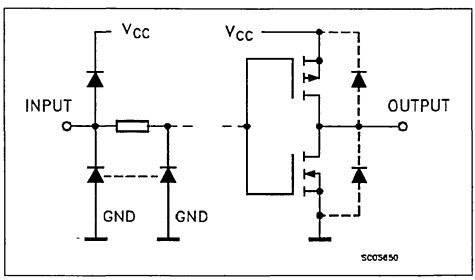
ORDER CODES :

M54HCT75F1R	M74HCT75M1R
M74HCT75B1R	M74HCT75C1R

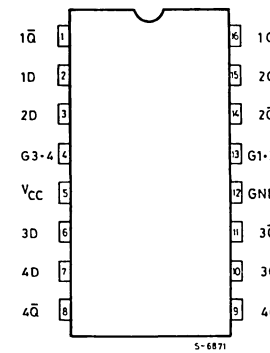
DESCRIPTION

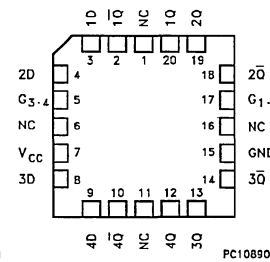
The M54/74HCT75 is a high speed CMOS 4-BIT D-TYPE LATCH fabricated in silicon gate C2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. It contains two groups of 2-bit latches controlled by an enable input (G1 • 2 or G3 • 4). These two latch groups can be used in different circuits. Each latch has Q and $\overline{Q}$ outputs (1Q - 4Q and 1Q - 4$\overline{Q}$). The data applied to the data input is transfered to the Q and $\overline{Q}$ outputs when the enable input is taken high and the outputs will follow the data input as long as the enable input is kept high. When the enable input is taken low, the information data applied to the data input is retained at the outputs. All inputs are equipped with protection circuits against static discharge and transient excess voltage. This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^{2}MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



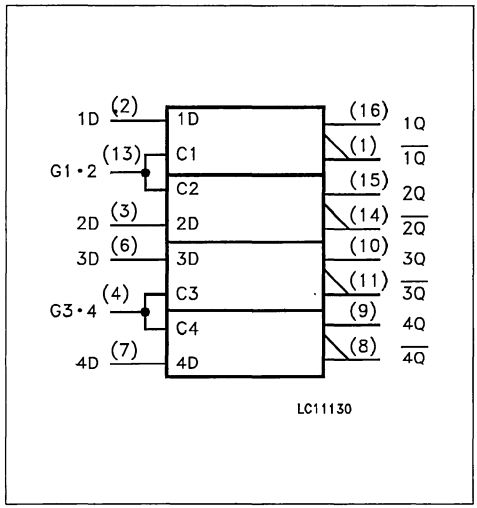


NC = No Internal Connection

TRUTH TABLE

INPUTS		OUTPUTS		FUNCTION
D	G	Q	$\overline{Q}$	
L	H	L	H	
H	H	H	L	
X	L	Qn	$\overline{Q}$n	LATCH

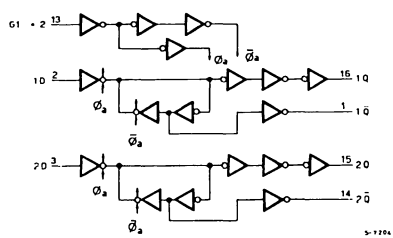
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 11, 8	1$\overline{Q}$ to 4$\overline{Q}$	Complementary Latch Outputs
2, 3, 6, 7	1D to 4D	Data Inputs
4	G3 • 4	Latch Enable Input, latches 3 and 4
13	G1 • 2	Latch Enable Input, latches 1 and 2
15, 15, 10, 9	1Q to 4Q	Latch Outputs
12	GND	Ground (0V)
5	V_{CC}	Positive Supply Voltage

SCHEMATIC CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

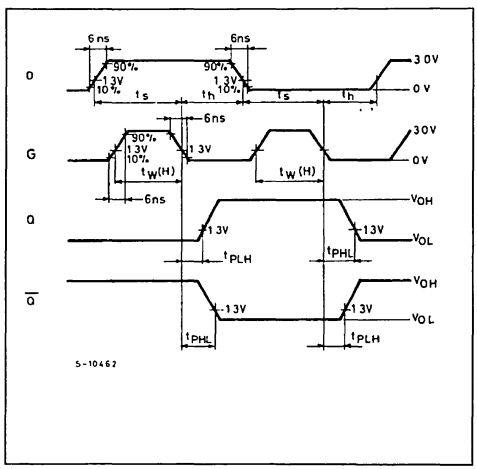
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				2		20		40	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9		3.0	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

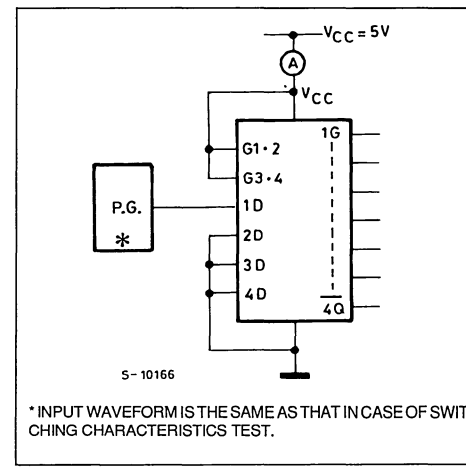
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			8	15		19		22	ns
t_{PLH} t_{PHL}	Propagation Delay Time (DATA-Q)	4.5			18	28		35		42	ns
t_{PLH} t_{PHL}	Propagation Delay Time (G-Q)	4.5			21	33		41		50	ns
$t_{W(H)}$	Minimum Pulse Width (G)	4.5			8	15		19		22	ns
t_s	Minimum Set-up Time	4.5			4	10		13		15	ns
t_h	Minimum Hold Time	4.5				5		5		8	ns
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				61						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



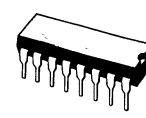
TEST CIRCUIT I_{CC} (Opr)



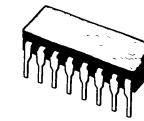
* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

DUAL J-K FLIP FLOP WITH PRESET AND CLEAR

- HIGH SPEED
  f_{MAX} = 65 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 2 µA (MAX.) AT 25 °C
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS76



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

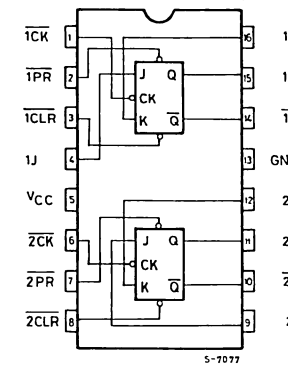
ORDER CODES :

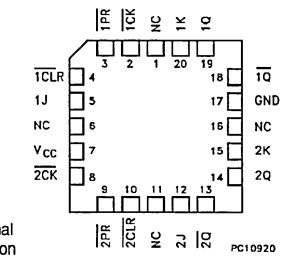
M54HC76F1R M74HC76M1R
M74HC76B1R M74HC76C1R

DESCRIPTION

The M54/74HC76 is a high speed CMOS DUAL J-K FLIP FLOP fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. Depending on with the logic level at the J and K inputs this device changes state on the negative going transition of the clock pulse. CLEAR and PRESET are independent of the clock and are accomplished by a logic low on the corresponding input. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

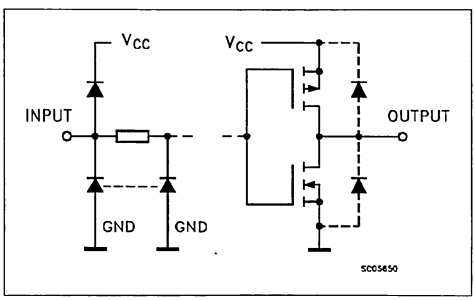
PIN CONNECTIONS (top view)





NC = No Internal Connection

INPUT AND OUTPUT EQUIVALENT CIRCUIT



TRUTH TABLE

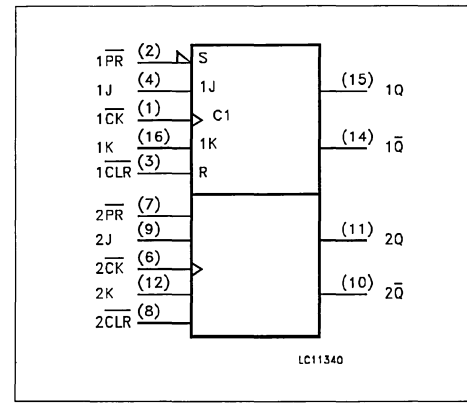
INPUTS					OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	L	↓	Q_n	$\overline{Q}_n$	NO CHANGE
H	H	L	H	↓	L	H	
H	H	H	L	↓	H	L	
H	H	H	H	↓	$\overline{Q}_n$	Q_n	TOGGLE
H	H	X	X	↑	Q_n	$\overline{Q}_n$	NO CHANGE

X: Don't Care

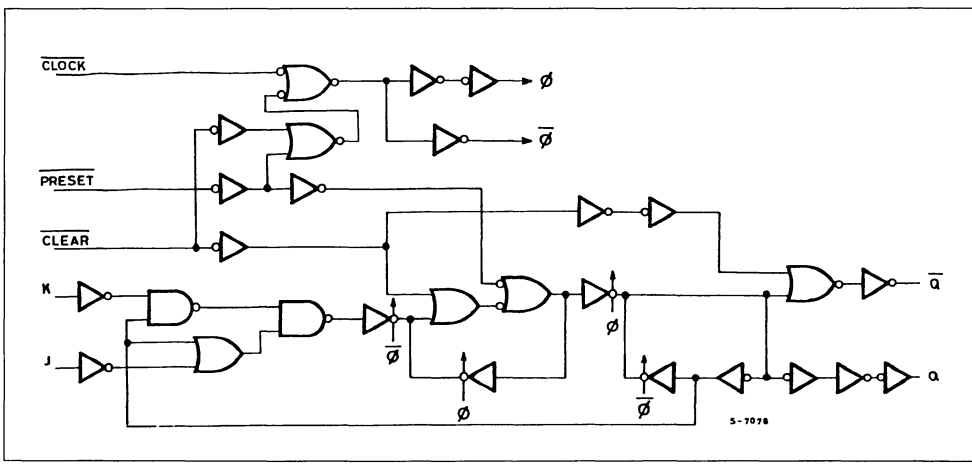
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 6	$1\overline{CK}$, $2\overline{CK}$	Clock Input (HIGH to LOW edge triggered)
2, 7	$1\overline{PR}$, $2\overline{PR}$	Set Inputs (Active LOW)
3, 8	$1\overline{CLR}$, $2\overline{CLR}$	Asynchronous Reset Inputs (Active LOW)
4, 9	1J, 2J	Data Inputs: Flip-Flop 1 and 2
10, 14	$1\overline{Q}$, $2\overline{Q}$	Complement Flip-Flop Outputs
11, 15	1Q, 2Q	True Flip-Flop Outputs
16, 12	1K, 2K	Data Inputs: Flip-Flop 1 and 2
5	GND	Ground (0V)
13	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



LOGIC DIAGRAM (1/2 Package)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

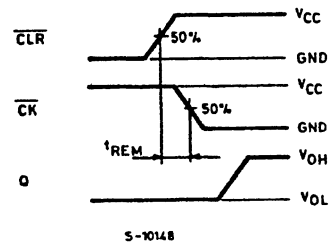
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				2		20		40	µA

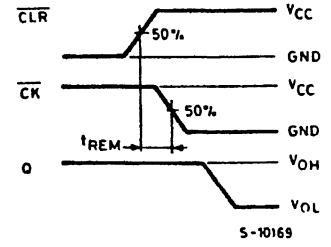
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

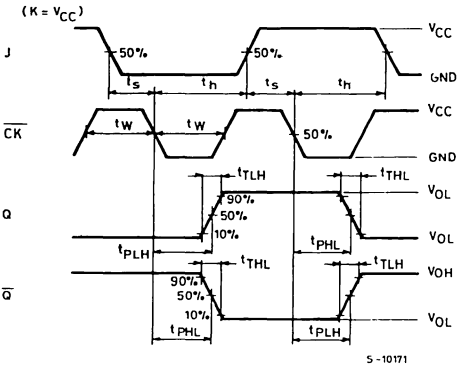
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CK}$ - Q, $\overline{Q}$)	2.0			60	125		155		190	ns
		4.5			15	25		31		38	
		6.0			13	21		26		32	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$ - Q, $\overline{Q}$)	2.0			76	140		175		210	ns
		4.5			18	28		35		42	
		6.0			16	24		30		36	
f_{MAX}	Maximum Clock Frequency	2.0		6.2	21		5.0		4.2		MHz
		4.5		31	63		25		21		
		6.0		37	67		30		25		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0			18	75		95		110	ns
		4.5			6	15		19		22	
		6.0			6	13		16		19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	2.0			22	75		95		110	ns
		4.5			6	15		19		22	
		6.0			6	13		16		19	
t_s	Minimum Set-up Time	2.0			25	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	2.0			20	75		95		110	ns
		4.5			6	15		19		22	
		6.0			5	13		16		19	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				38						pF

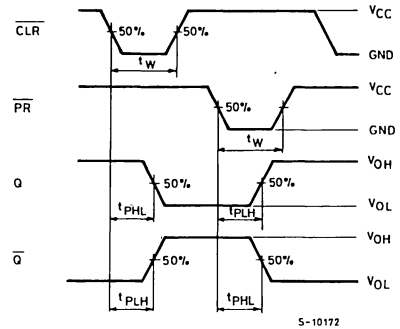
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per FLIP/FLOP)

SWITCHING CHARACTERISTICS TEST WAVEFORM

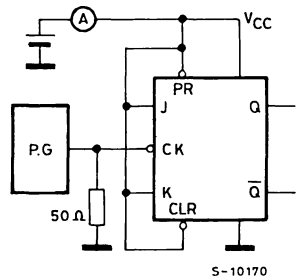








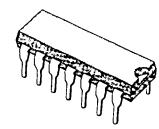
TEST CIRCUIT I_{CC} (Opr.)



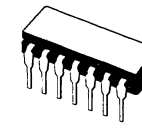
INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

4-BIT D-TYPE LATCH

- HIGH SPEED
  t_{PD} = 10 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 2 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS77



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

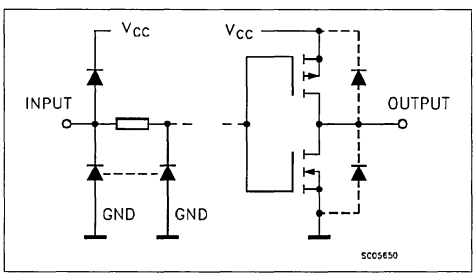
ORDER CODES :

M54HC77F1R M74HC77M1R
M74HC77B1R M74HC77C1R

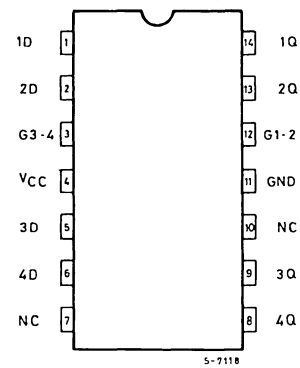
DESCRIPTION

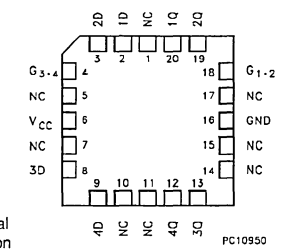
The M54/74HC77 is a high speed CMOS 4-BIT D-TYPE LATCH fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. It contains two groups of 2-bit latches controlled by an enable input (G1 • 2 or G3 • 4). These two latch groups can be used in different circuits. The data applied to the data inputs (1D, 2D, or 3D, 4D) are transfered to the Q outputs (1Q, 2Q, or 3Q, 4Q) respectively when the enable input (G1 • 2 or G3 • 4) is taken high. The Q outputs will follow the data inputs as long as the enable input is kept high. When the enable input is taken low, the information data applied to the data inputs is retained at the Q outputs. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





NC =
No Internal
Connection

TRUTH TABLE

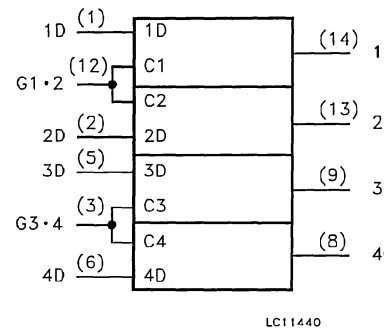
INPUTS		OUTPUTS	FUNCTION
D	G	Q	
L	H	L	
H	H	H	
X	L	Q_n	LATCH

X: Don't Care

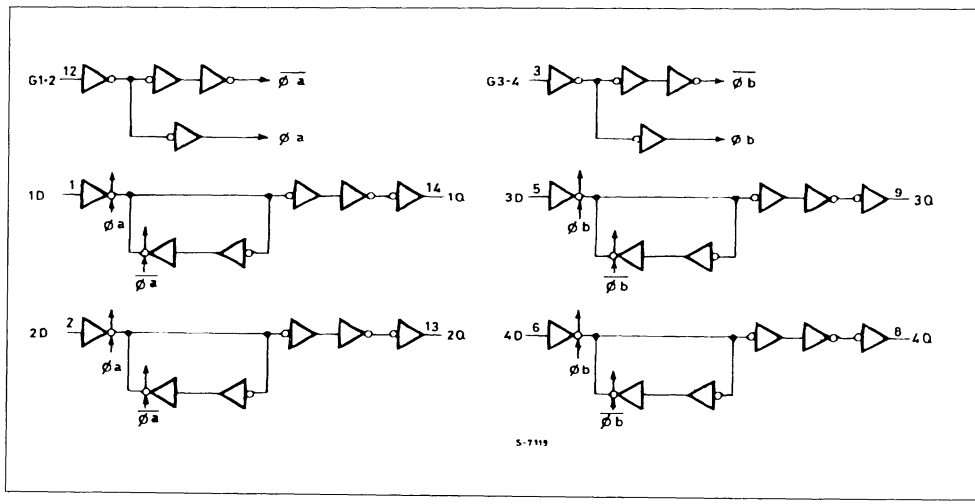
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 5, 6	1D to 4D	Data Inputs
3	G3 • 4	Latch Enable Input, Latches 3 and 4
7, 10	NC	No Internal Connection
8, 9, 13, 14	1Q to 4Q	Latch Outputs
12	G1 • 2	Latch Enable Input, Latches 1 and 2
11	GND	Ground (0V)
4	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

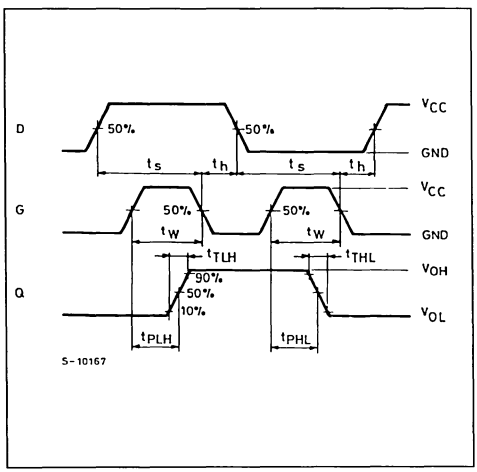
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				2		20		40	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

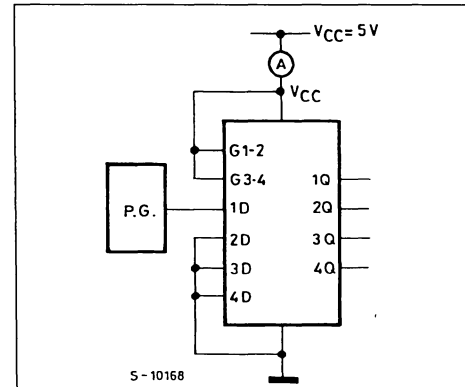
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (DATA - Q)	2.0			39	100		125		150	ns
		4.5			13	20		25		30	
		6.0			11	17		21		26	
t_{PLH} t_{PHL}	Propagation Delay Time (G - Q)	2.0			39	100		125		150	ns
		4.5			13	20		25		30	
		6.0			11	17		21		26	
$t_{W(H)}$	Minimum Pulse Width (G)	2.0			15	75		95		110	ns
		4.5			6	15		19		22	
		6.0			6	13		16		19	
t_s	Minimum Set-up Time	2.0			15	50		65		75	ns
		4.5			3	10		13		15	
		6.0			3	9		11		13	
t_h	Minimum Hold Time	2.0				25		30		40	ns
		4.5				5		6		8	
		6.0				4		5		7	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				20						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per FLIP/FLOP)

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr)



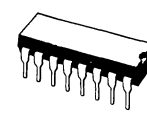
INPUT WAVEFORM IS THE SAVE AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

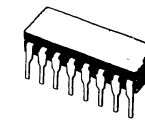
M54HC85
M74HC85

4-BIT MAGNITUDE COMPARATOR

- HIGH SPEED
  t_{PD} = 22 ns (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V to 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS85



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

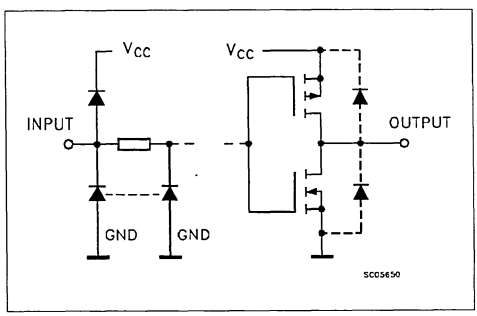
ORDER CODES :

M54HC85F1R M74HC85M1R
M74HC85B1R M74HC85C1R

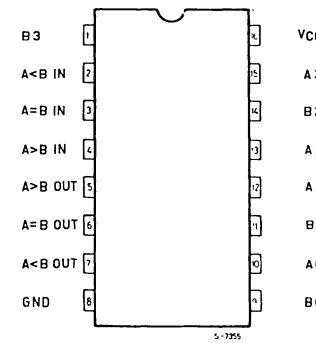
DESCRIPTION

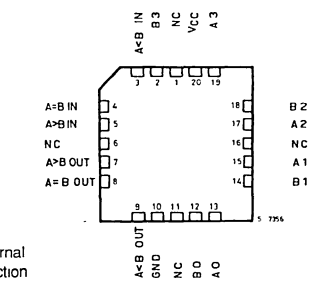
The M54/74HC85 is a high speed CMOS 4-BIT MAGNITUDE COMPARATOR fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This comparator compares two 4-bit words and provides a high voltage level on one of the A > B out, A = B out and A < B out outputs. The comparing bit number is easily expanded by cascading several devices as shown in the typical application. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



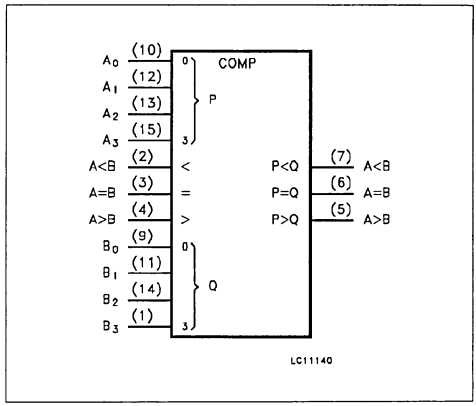


NC =
No Internal
Connection

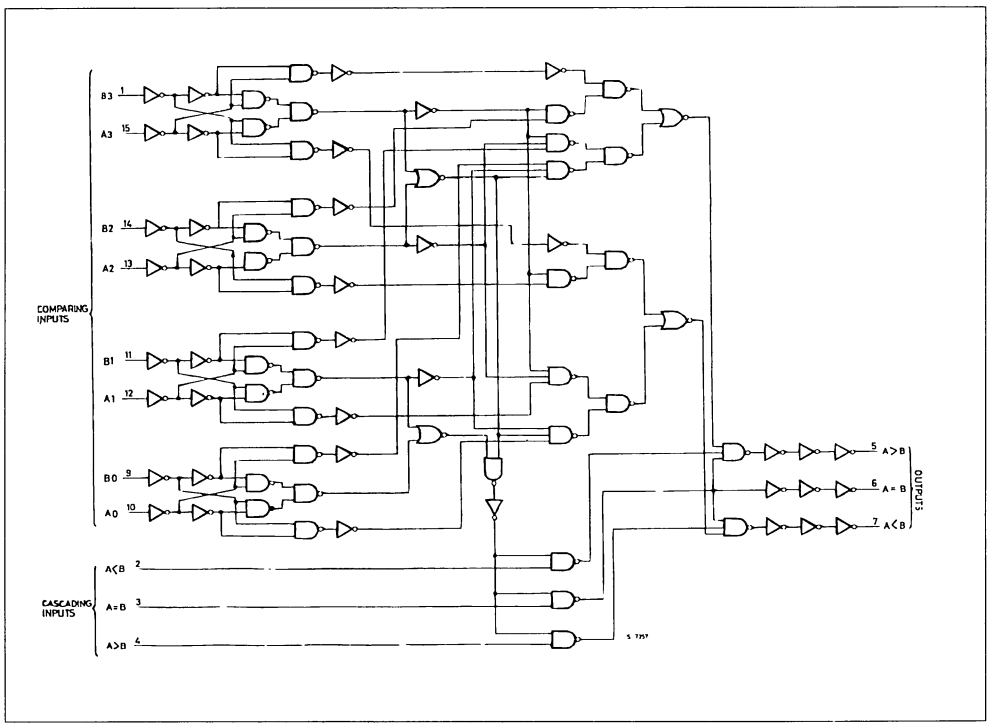
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
2	$IN_{A<B}$	A<B Expansion Input
3	$IN_{A=B}$	A=B Expansion Input
4	$IN_{A>B}$	A>B Expansion Input
5	$OUT_{A>B}$	A>B Expansion Output
6	$OUT_{A=B}$	A=B Expansion Output
7	$OUT_{A<B}$	A<B Expansion Output
9, 11, 14, 1	B_0 to B_3	Word B Inputs
10, 12, 13, 15	A_0 to A_3	Word A Inputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



LOCIG DIAGRAM



TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
				A>B	A<B	A=B	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L
				X	X	H	L	L	H
				L	H	L	L	H	L
				H	L	L	H	L	L
				H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3<B3	X	X	X	X	X	X	L	H	L

X: DON'T CARE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW· ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

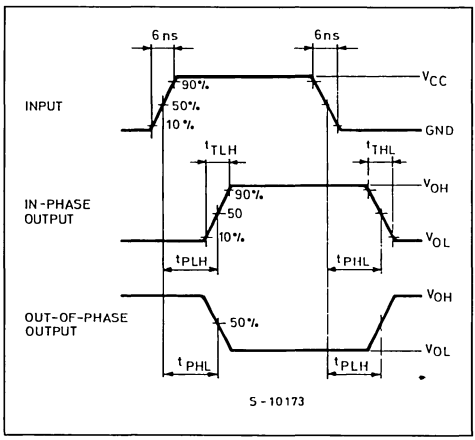
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

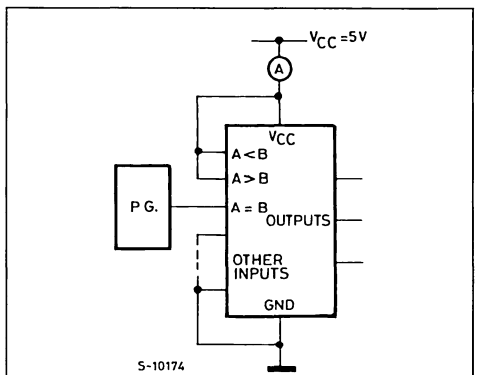
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (A, B-OUT)	2.0			96	185		230		280	ns
		4.5			24	37		46		56	
		6.0			20	31		39		48	
t_{PLH} t_{PHL}	Propagation Delay Time (CASCADE-OUT)	2.0			48	95		120		145	ns
		4.5			12	19		24		29	
		6.0			10	16		20		25	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				23						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

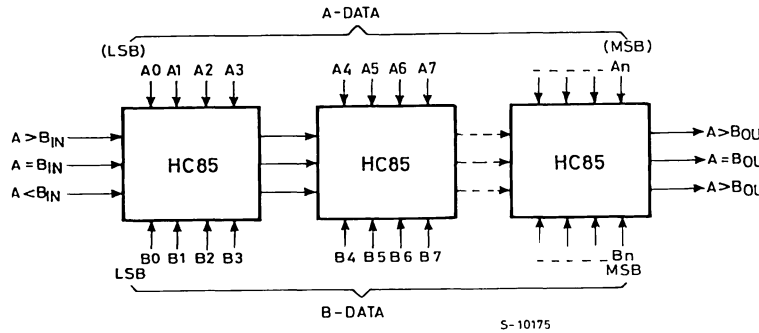


TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TYPICAL APPLICATION



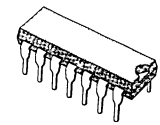
LSB = lowest significant bit MSB = MOST SIGNIFICANT BIT

COMPARING INPUTS	CASCADING INPUTS			OUTPUTS		
	A>B	A=B	A<B	A>B	A=B	A<B
(A)>(B)	X	X	X	H	L	L
(A)=(B)	H	L	L	H	L	L
	X	H	X	L	H	L
	L	L	H	L	L	H
(A)<(B)	X	X	X	L	L	H

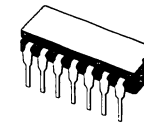
X: DON'T CARE

QUAD EXCLUSIVE OR GATE

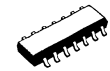
- HIGH SPEED
  t_{PD} = 10 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS86



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HC86F1R M74HC86M1R
M74HC86B1R M74HC86C1R

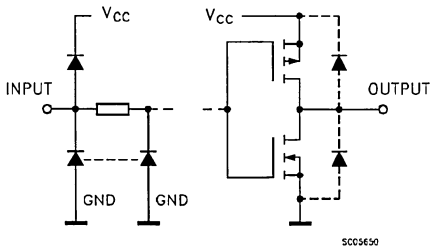
DESCRIPTION

The M54/74HC86 is a high speed CMOS QUAD EXCLUSIVE OR GATE fabricated in silicon gate C^2MOS technology.

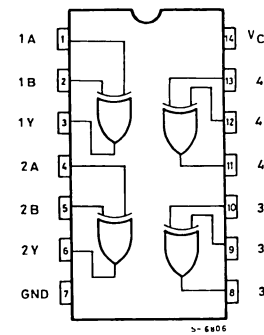
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. Input and output buffer are installed, which enables high noise immunity and stable output.

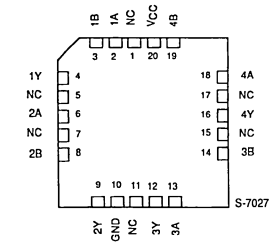
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



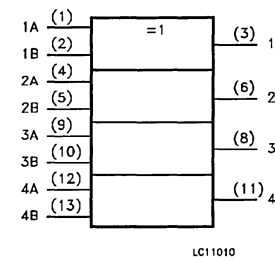


NC = No Internal Connection

TRUTH TABLE

A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

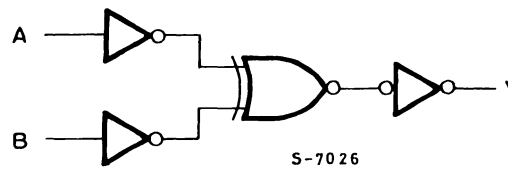
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data Inputs
2, 5, 10, 13	1B to 4B	Data Inputs
3, 6, 8, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

SCHEMATIC CIRCUIT (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

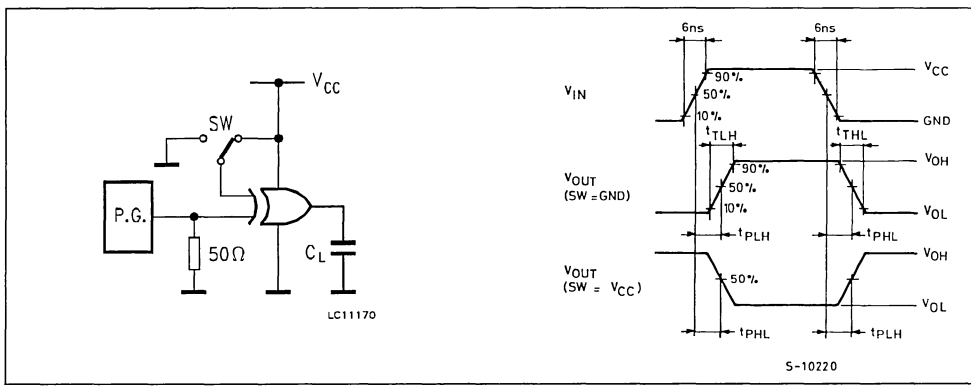
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

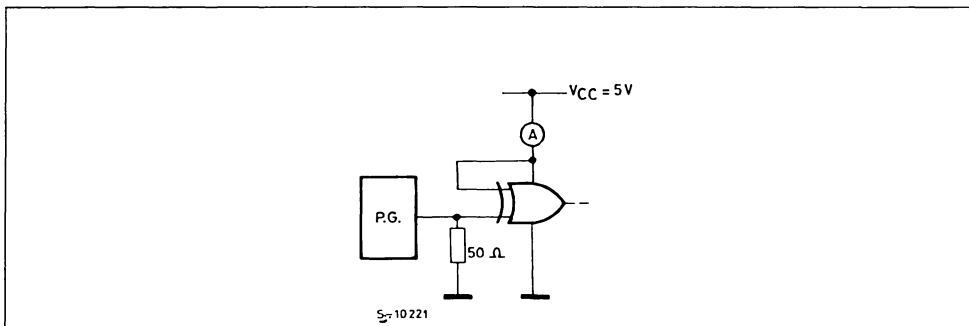
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			56	110		140		165	ns
		4.5			14	22		28		33	
		6.0			12	19		24		28	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				26						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



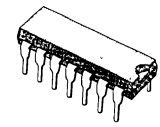
TEST CIRCUIT I_{CC} (Opr.)



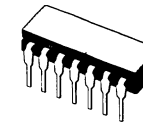
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

QUAD EXCLUSIVE OR GATE

- HIGH SPEED
  t_{PD} = 15 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS86



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HCT86F1R M74HCT86M1R
M74HCT86B1R M74HCT86C1R

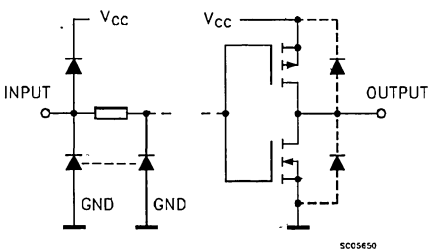
DESCRIPTION

The M54/74HCT86 is a high speed CMOS QUAD EXCLUSIVE OR GATE fabricated in silicon gate C^2MOS technology.

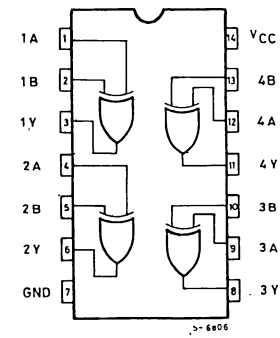
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. Input and output buffer are installed, which enables high noise immunity and stable output.

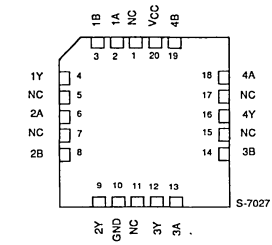
All inputs are equipped with protection circuits against static discharge and transient excess voltage.This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



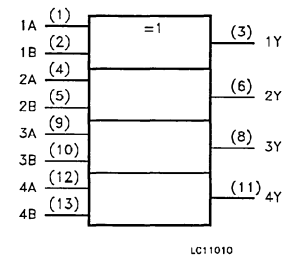


NC =
No Internal
Connection

TRUTH TABLE

A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

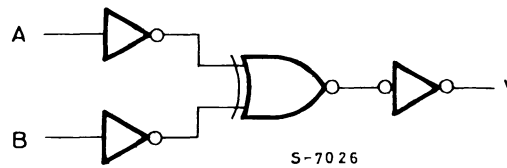
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data Inputs
2, 5, 10, 13	1B to 4B	Data Inputs
3, 6, 8, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

SCHEMATIC CIRCUIT (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur Functional operation under these condition is not implied
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

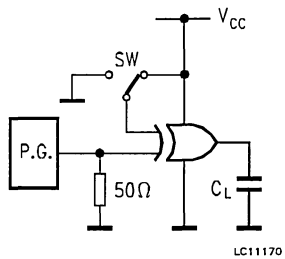
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				1		10		20	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9		3.0	mA

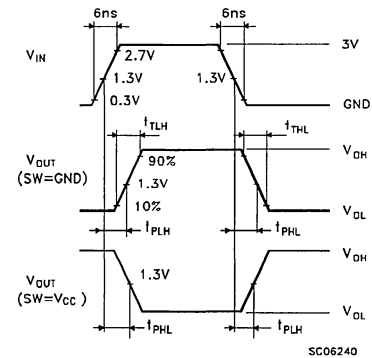
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			8	15		19		23	ns
t_{PLH} t_{PHL}	Propagation Delay Time	4.5			15	24		30		36	ns
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				48						pF

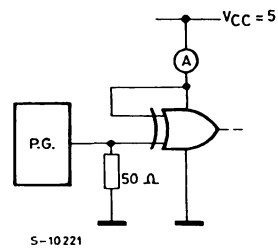
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT





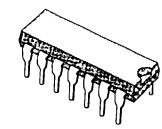
TEST CIRCUIT I_{CC} (Opr.)



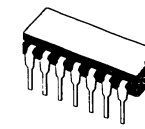
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

DUAL J-K FLIP FLOP WITH CLEAR

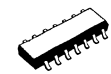
- HIGH SPEED
  f_{MAX} = 75 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 2 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS107



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

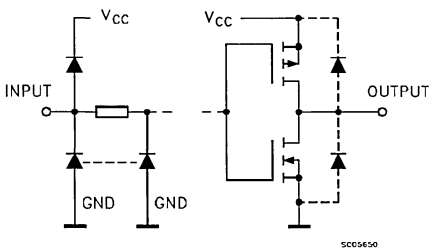
ORDER CODES :

M54HC107F1R M74HC107M1R
M74HC107B1R M74HC107C1R

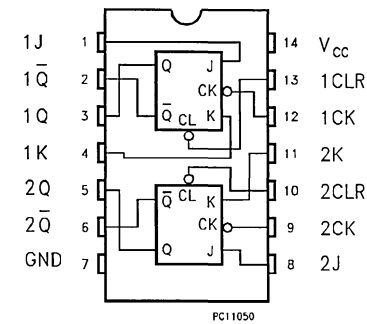
DESCRIPTION

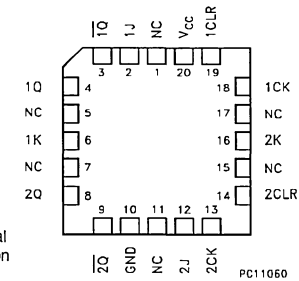
The M54/74HC107 is a high speed CMOS DUAL J-K FLIP FLOP fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. These flip-flop are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Each one has independent J, K, CLOCK, and CLEAR input and Q and $\overline{Q}$ outputs. CLEAR is independent of the clock and accomplished by a logic low on the input. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





NC =
No Internal
Connection

TRUTH TABLE

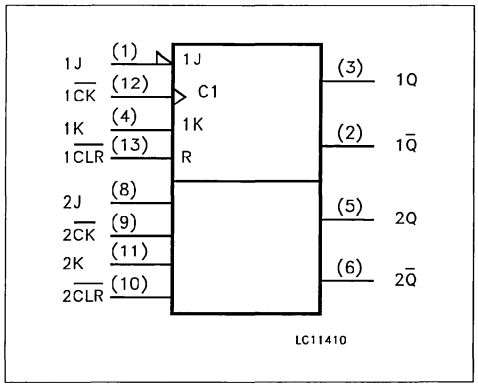
INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	J	K	CK	Q	$\overline{Q}$	
L	X	X	X	L	H	CLEAR
H	L	L	⊓	Q_n	$\overline{Q}_n$	NO CHANGE
H	L	H	⊓	L	H	
H	H	L	⊓	H	L	
H	H	H	⊓	$\overline{Q}_n$	Q_n	TOGGLE
H	X	X	⊔	Q_n	$\overline{Q}_n$	NO CHANGE

X: Don't Care

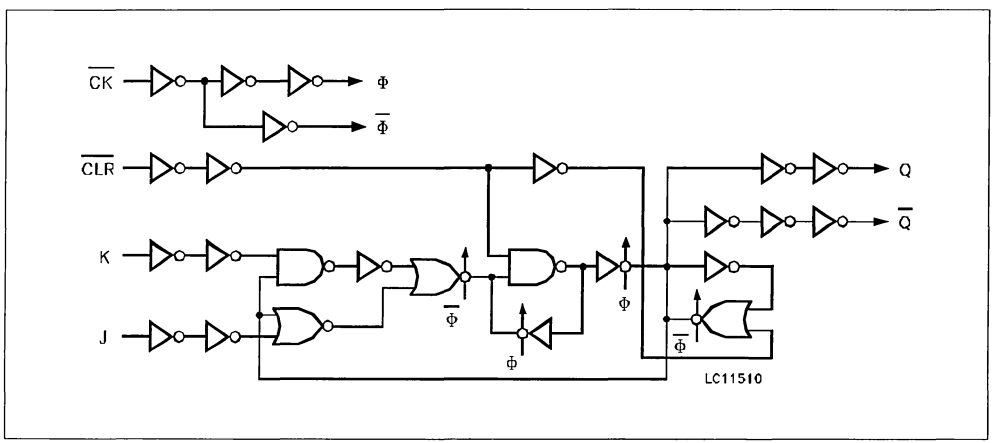
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 8, 4, 11	1J, 2J, 1K, 2K	Synchronous Inputs; Flip-Flop 1 And 2
2, 6	$1\overline{Q}$, $2\overline{Q}$	Complement Flip-Flop Outputs
3, 5	1Q, 2Q	True Flip-Flop Outputs
12, 9	$1\overline{CK}$, $2\overline{CK}$	Clock Input
13, 10	1CLR, 2CLR	Asynchronous Reset Inputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



LOGIC DIAGRAM (1/2 Package)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{DD} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW. ≡ 65 °C derate to 300 mW by 10mW/°C. 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

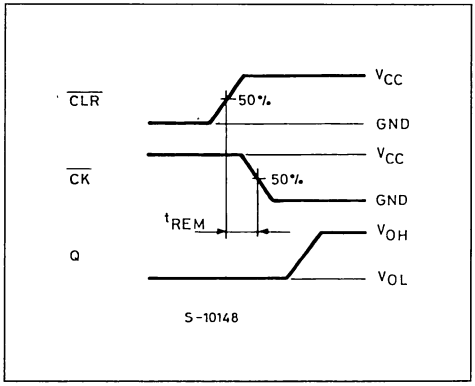
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				2		20		40	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

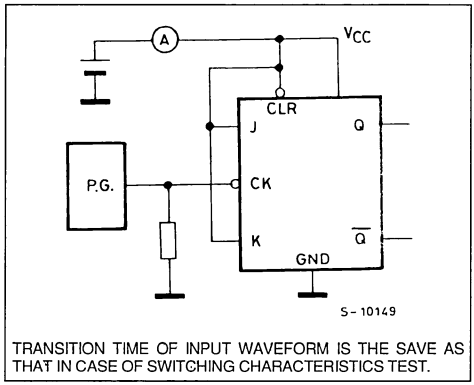
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CK - Q, $\overline{Q}$)	2.0			48	125		155		190	ns
		4.5			14	25		31		38	
		6.0			12	21		26		32	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$ - Q, $\overline{Q}$)	2.0			52	140		175		210	ns
		4.5			15	28		35		42	
		6.0			13	24		30		36	
f_{MAX}	Maximum Clock Frequency	2.0		6.2	23		5.0		4.2		MHz
		4.5		31	70		25		21		
		6.0		37	80		30		25		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLR}$)	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	
t_s	Minimum Set-up Time	2.0			28	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Minimum Removal Time ($\overline{CLR}$)	2.0				25		30		40	ns
		4.5				5		6		8	
		6.0				5		5		7	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				32						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per FLIP/FLOP)

SWITCHING CHARACTERISTICS TEST

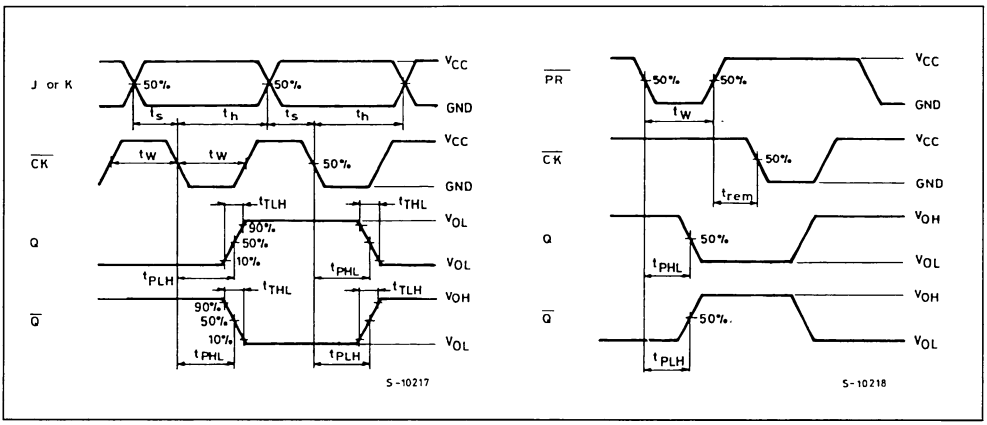


TEST CIRCUIT I_{CC} (Opr.)



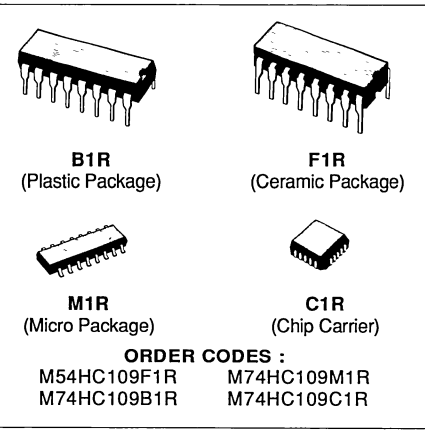
TRANSITION TIME OF INPUT WAVEFORM IS THE SAVE AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SWITCHING CHARACTERISTICS TEST WAVEFORM



DUAL J-K FLIP FLOP WITH PRESET AND CLEAR

- HIGH SPEED
  f_{MAX} = 63 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 2 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS109



B1R
(Plastic Package)

F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HC109F1R M74HC109M1R
M74HC109B1R M74HC109C1R

DESCRIPTION

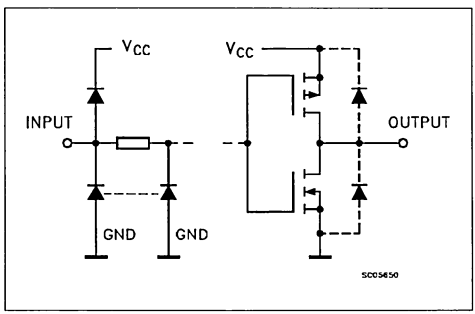
The M54/74HC109 is a high speed CMOS DUAL J-$\overline{K}$ FLIP-FLOP WITH PRESET AND CLEAR fabricated in silicon gate C^2MOS technology.

It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

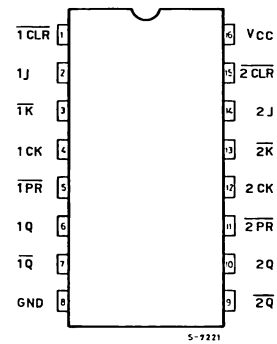
In accordance with the logic level on the J and $\overline{K}$ input is device changes state on positive going transitions of the clock pulse. CLEAR and PRESET are independent of the clock and accomplished by a low logic level on the corresponding input.

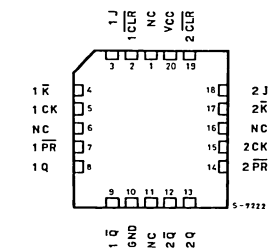
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



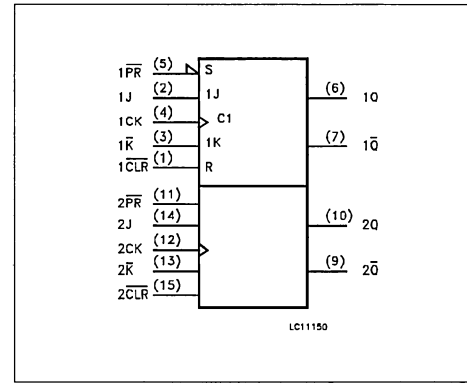


NC =
No Internal
Connection

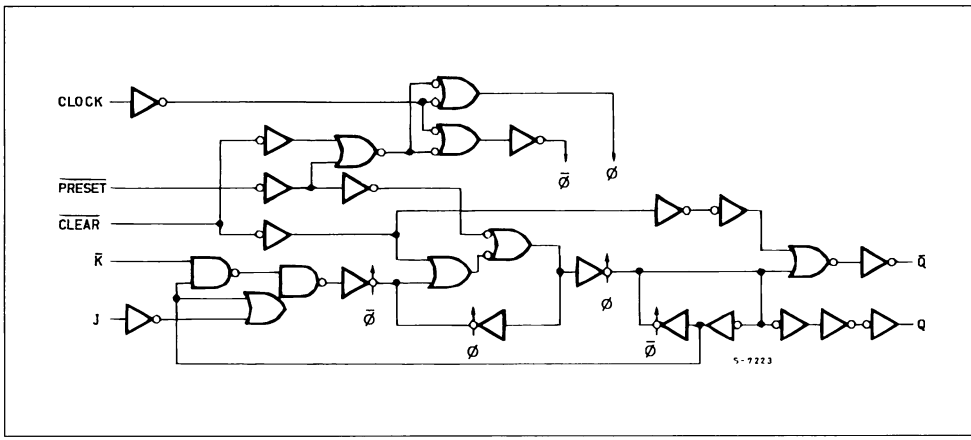
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{CLR}$, $2\overline{CLR}$	Asynchronous Reset Direct Input
2, 4, 3, 13	1J, 2J, $1\overline{K}$, $2\overline{K}$	Syncronous Inputs; Flip-flops 1 and 2
4, 12	1CK, 2CK	Clock Input
5, 11	$1\overline{PR}$, $2\overline{PR}$	Asynchronous Set Direct Input (Active LOW)
6, 10	1Q, 2Q	True Flip-flop Outputs
7, 9	$1\overline{Q}$, $2\overline{Q}$	Complement Flip-flop Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



LOGIC CIRCUIT



TRUTH TABLE

INPUTS					OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	J	$\overline{K}$	CK	Q	$\overline{Q}$	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	H	⎍	Qn	$\overline{Q}n$	NO CHANGE
H	H	⎍	L	⎍	L	H	
H	H	H	H	⎍	H	L	
H	H	H	L	⎍	$\overline{Q}n$	Qn	TOGGLE
H	H	X	X	⎌	Qn	$\overline{Q}n$	NO CHANGE

X = DON'T CARE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

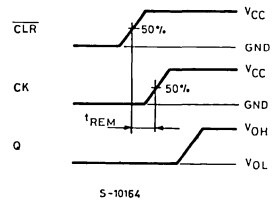
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				2		20		40	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

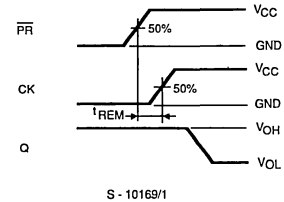
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CK-Q, $\overline{Q}$)	2.0			50	150		190		225	ns
		4.5			16	30		38		45	
		6.0			13	26		32		38	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$-Q, $\overline{Q}$)	2.0			50	150		190		225	ns
		4.5			16	30		38		45	
		6.0			13	26		32		38	
f_{MAX}	Maximum Clock Frequency	2.0		6.2	17		5		4.2		MHz
		4.5		31	59		25		21		
		6.0		37	67		30		25		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0			15	75		95		110	ns
		4.5			6	15		19		22	
		6.0			6	13		16		19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	2.0			15	75		95		110	ns
		4.5			6	15		19		22	
		6.0			6	13		16		19	
t_s	Minimum Set-up Time	2.0			17	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	2.0			13	50		65		75	ns
		4.5			4	10		13		15	
		6.0			3	9		11		13	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				41						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per Flip-flop)

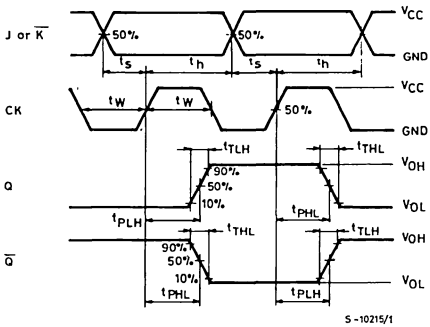
SWITCHING CHARACTERISTICS TEST WAVEFORM



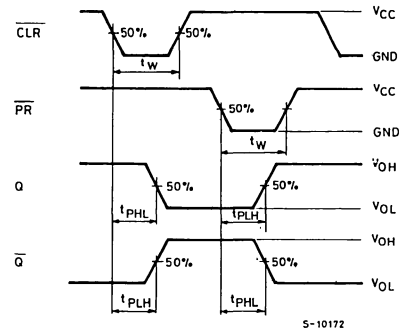
S-10164



S-10169/1

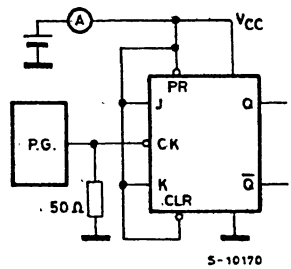


S-10215/1



S-10172

TEST CIRCUIT Icc (Opr.)

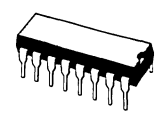


S-10170

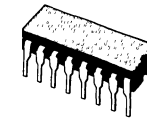
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

DUAL J-K FLIP FLOP WITH PRESET AND CLEAR

- HIGH SPEED
  f_{MAX} = 67 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 2 µA AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS112



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

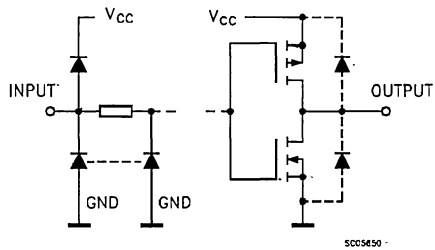
ORDER CODES :

M54HC112F1R M74HC112M1R
M74HC112B1R M74HC112C1R

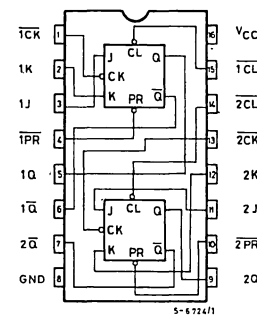
DESCRIPTION

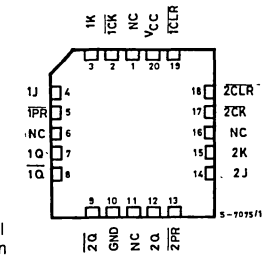
The M54/74HC112 is a high speed CMOS DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The M54HC112/M74HC112 dual JK flip-flop features individual J, K, clock, and asynchronous set and clear inputs for each flip-flop. When the clock goes high, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is high and the bistable will function as shown in the truth table. Input data is transferred to the input on the negative-going edge of the clock pulse. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





NC =
No Internal
Connection

TRUTH TABLE

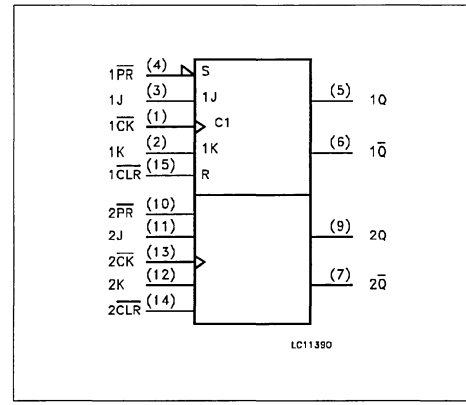
INPUTS					OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	J	K	CK	Q	$\overline{Q}$	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	L	⊓	Q_n	$\overline{Q}_n$	NO CHANGE
H	H	H	L	⊓	H	L	
H	H	L	H	⊓	L	H	
H	H	H	H	⊓	$\overline{Q}_n$	Q_n	TOGGLE
H	H	X	X	⊔	Q_n	$\overline{Q}_n$	NO CHANGE

X: Don't Care

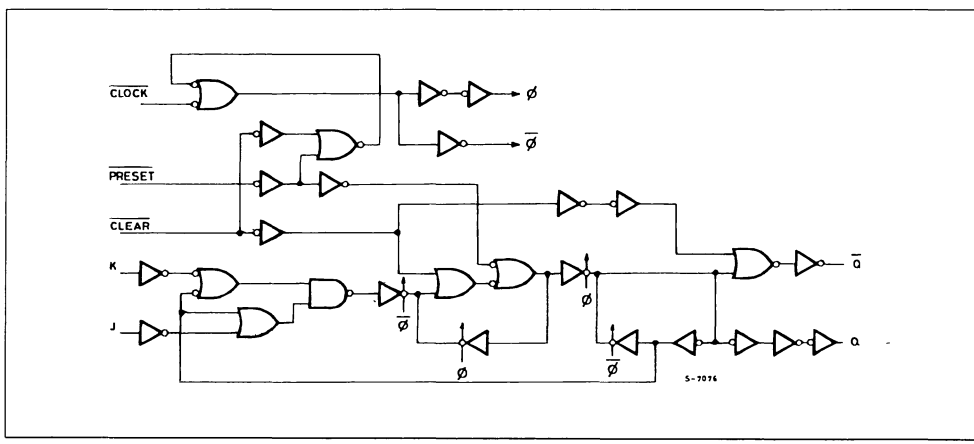
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 13	$1\overline{CK}$, $2\overline{CK}$	Clock Input (HIGH to LOW edge triggered)
2, 12	1K, 2K	Data Inputs: Flip-Flop 1 and 2
3, 11	1J, 2J	Data Inputs: Flip-Flop 1 and 2
4, 10	$1\overline{PR}$, $2\overline{PR}$	Set Inputs
5, 9	1Q, 2Q	True Flip-Flop Outputs
6, 7	$1\overline{Q}$, $2\overline{Q}$	Complement Flip-Flop Outputs
15, 14	$1\overline{CLR}$, $2\overline{CLR}$	Reset inputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



LOGIC DIAGRAM (1/2 Package)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series		-55 to +125	°C
	M74HC Series		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

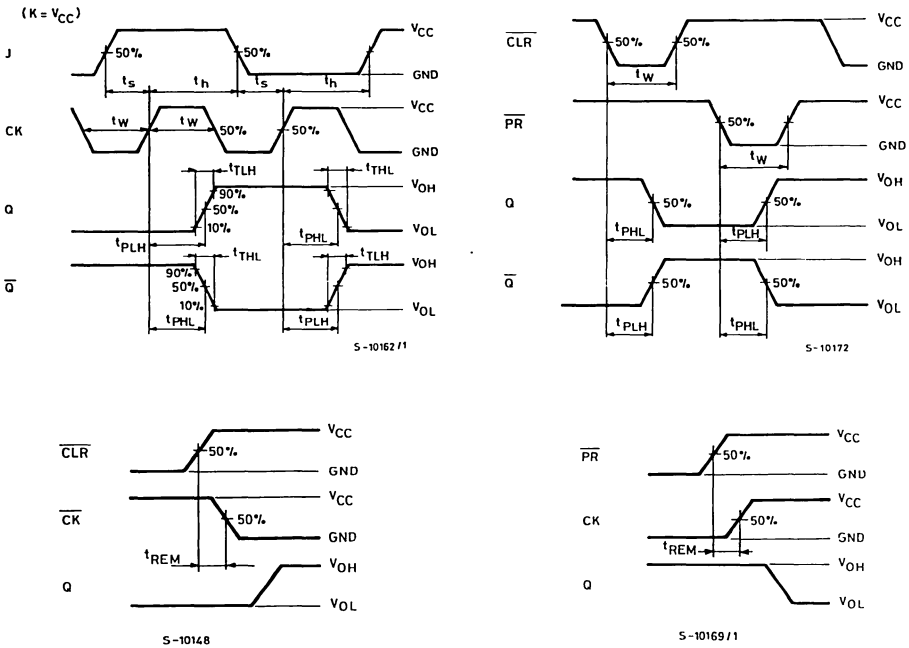
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				2		20		40	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

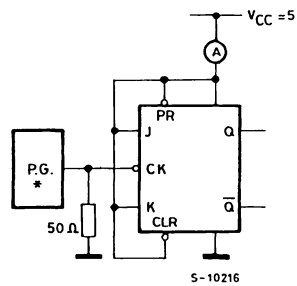
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CK}$ - Q, $\overline{Q}$)	2.0			52	125		155		190	ns
		4.5			16	25		31		38	
		6.0			14	21		26		32	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$ - Q, $\overline{Q}$)	2.0			68	135		170		205	ns
		4.5			17	27		34		41	
		6.0			14	23		29		35	
f_{MAX}	Maximum Clock Frequency	2.0		8	16		6.4		5.4		MHz
		4.5		40	68		32		27		
		6.0		47	79		38		32		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width ($\overline{CLOCK}$)	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	
t_s	Minimum Set-up Time	2.0			28	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	2.0			24	50		60		70	ns
		4.5			4	10		12		14	
		6.0			3	9		10		12	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				33						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per FLIP/FLOP)

SWITCHING CHARACTERISTICS TEST WAVEFORM



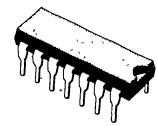
TEST CIRCUIT (Opr.)



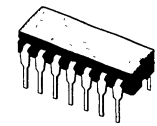
INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

DUAL J-K FLIP FLOP WITH PRESET

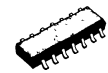
- HIGH SPEED
  f_{MAX} = 71 MHz (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 2 µA at T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V to 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS113



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

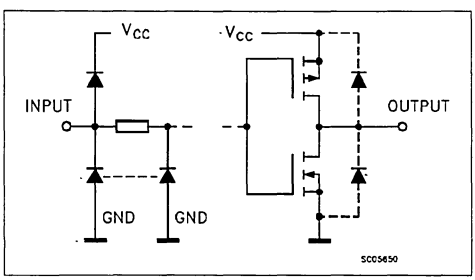
ORDER CODES :

M54HC113F1R M74HC113M1R
M74HC113B1R M74HC113C1R

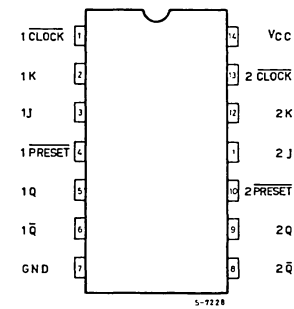
DESCRIPTION

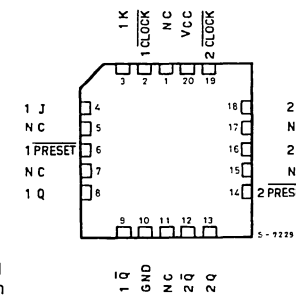
The M54/74HC113 is a high speed CMOS DUAL J-K FLIP FLOP WITH PRESET fabricated in silicon gate C2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This circuit offers individual J, K, set, and clock inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will function as shown in the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





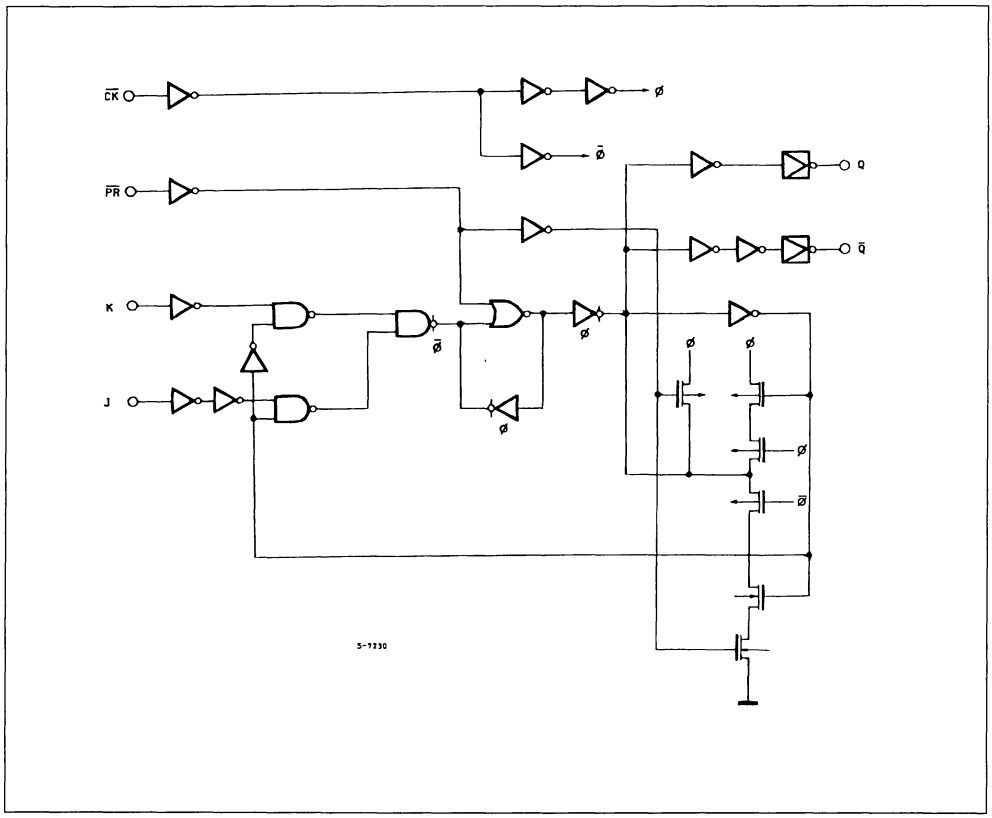
NC =
No Internal
Connection

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{PR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	X	X	X	H	L	PRESET
H	L	L	⊓↓	Q_n	$\overline{Q}_n$	NO CHANGE
H	L	H	⊓↓	L	H	
H	H	L	⊓↓	H	L	
H	H	H	⊓↓	$\overline{Q}_n$	Q_n	TOGGLE
H	X	X	↓⊓	Q_n	$\overline{Q}_n$	NO CHANGE

X: Don't Care

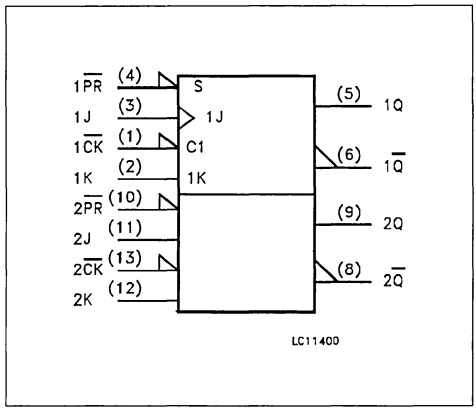
LOGIC DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 13	$1\overline{CK}$, $2\overline{CK}$	Clock Input (HIGH to LOW edge triggered)
2, 12	1K, 2K	Data Inputs: Flip-Flop 1 and 2
3, 11	1J, 2J	Data Inputs: Flip-Flop 1 and 2
4, 10	$1\overline{PR}$, $2\overline{PR}$	Set Inputs
5, 9	1Q, 2Q	True Flip-Flop Outputs
6, 8	$1\overline{Q}$, $2\overline{Q}$	Complement Flip-Flop Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

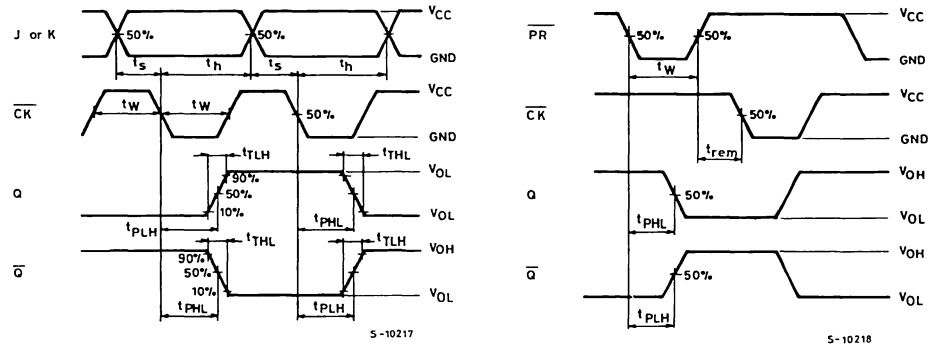
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				2		20		40	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

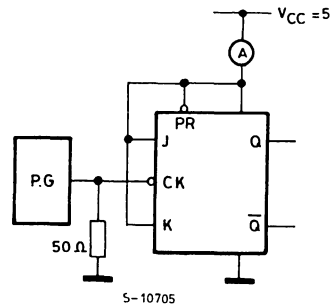
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CK}$ - Q, $\overline{Q}$)	2.0			46	125		155		190	ns
		4.5			16	25		31		38	
		6.0			12	21		26		32	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{PRESET}$ - Q, $\overline{Q}$)	2.0			48	125		155		190	ns
		4.5			16	25		31		38	
		6.0			13	21		26		32	
f_{MAX}	Maximum Clock Frequency	2.0		8	16		6.4		5.4		MHz
		4.5		40	63		32		27		
		6.0		47	79		38		32		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width ($\overline{CLOCK}$)	2.0			16	75		95		110	ns
		4.5			4	15		19		22	
		6.0			3	13		16		19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{PRESET}$)	2.0			16	75		95		110	ns
		4.5			4	15		19		22	
		6.0			3	13		16		19	
t_s	Minimum Set-up Time	2.0			16	50		65		75	ns
		4.5			4	10		13		15	
		6.0			3	9		11		13	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Minimum Removal Time ($\overline{PRESET}$)	2.0				5		5		5	ns
		4.5				5		5		5	
		6.0				5		5		5	
C_{IN}	Input Capacitance				5	10		10		1 0	pF
C_{PD} (*)	Power Dissipation Capacitance				37						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per FLIP/FLOP)

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT Icc (Opr.)

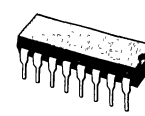


INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

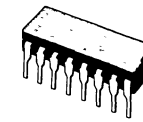
M54HC123/123A
M74HC123/123A

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

- HIGH SPEED
  t_{PD} = 25 ns (TYP) at V_{CC} = 5V
- LOW POWER DISSIPATION
  STANDBY STATE I_{CC}=4 µA (MAX.) AT T_A=25°C
  ACTIVE STATE I_{CC} = 200 µA (TYP.) AT V_{CC}=5V
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $I_{OH} = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- WIDE OUTPUT PULSE WIDTH RANGE
  t_{WOUT} = 120 ns ~ 60 s OVER AT V_{CC} = 4.5 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS123



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

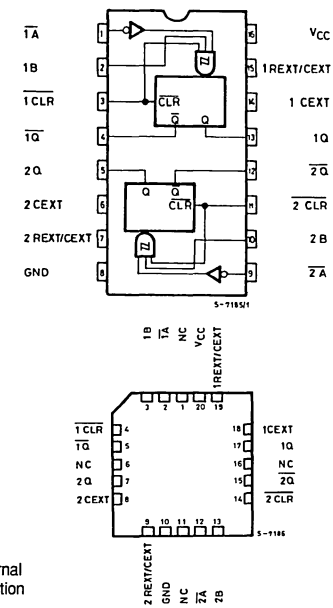
ORDER CODES :

M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

DESCRIPTION

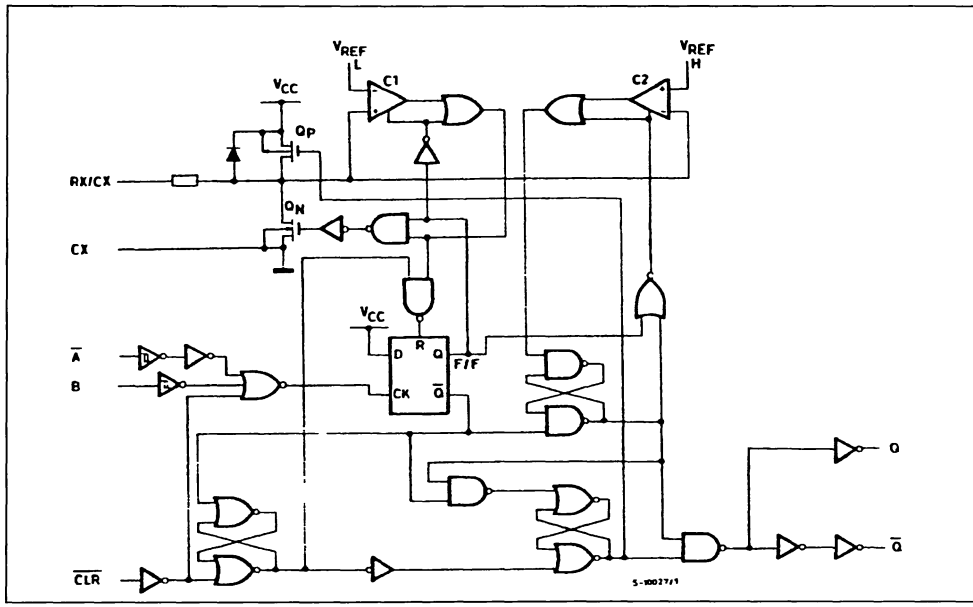
The M54/74HC123 is a high speed CMOS MONOSTABLE multivibrator fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. There are two trigger inputs, $\overline{A}$ INPUT (negative edge) and B INPUT (positive edge). These inputs are valid for slow rising/falling signals, (tr = tf = I sec). The device may also be triggered by using the CLR input (positive-edge) because of the Schmitt-trigger input ; after triggering the output maintains the MONOSTABLE state for the time period determined by the external resistor Rx and capacitor Cx. When Cx ≥ 10nF and Rx ≥ 10KΩ, the output pulse width value is approssimatively given by the formula: $t_{w(out)} = K \bullet Cx \bullet Rx$. Two different pulse width constant are available:
K ≅ 0.45 for HC123 K ≅ 1 for HC123A.
Taking $\overline{CLR}$ low breaks this MONOSTABLE STATE. If the next trigger pulse occurs during the MONOSTABLE period it makes the MONOSTABLE period longer. Limit for values of Cx and Rx :
Cx : NO LIMIT
Rx : V_{CC} < 3.0 V 5 K Ω to 1 M Ω
V_{CC} ≥ 3.0 V 1 K Ω to 1 M Ω
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)

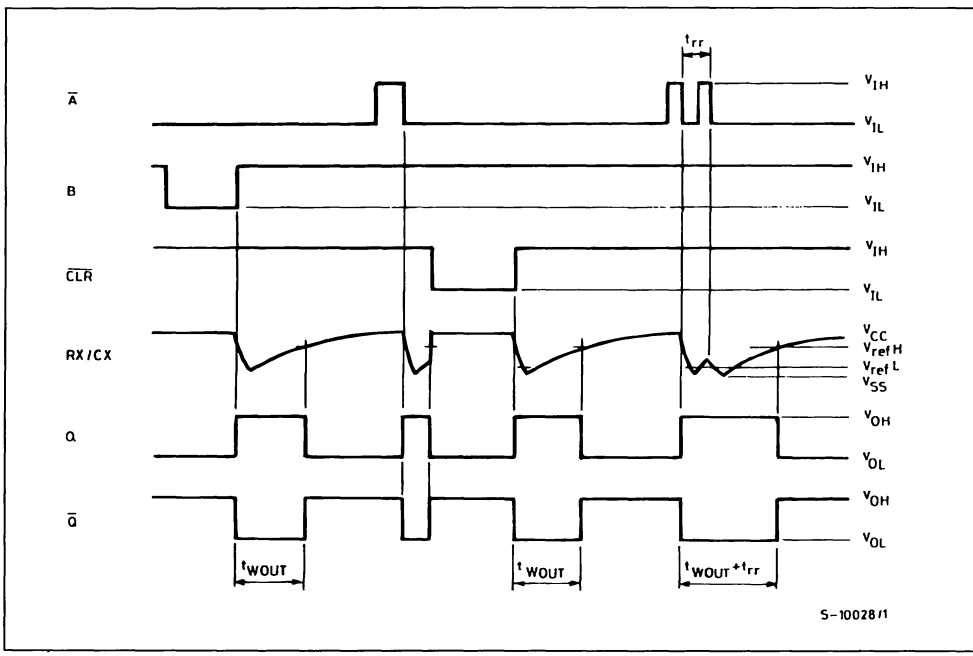


NC =
No Internal
Connection

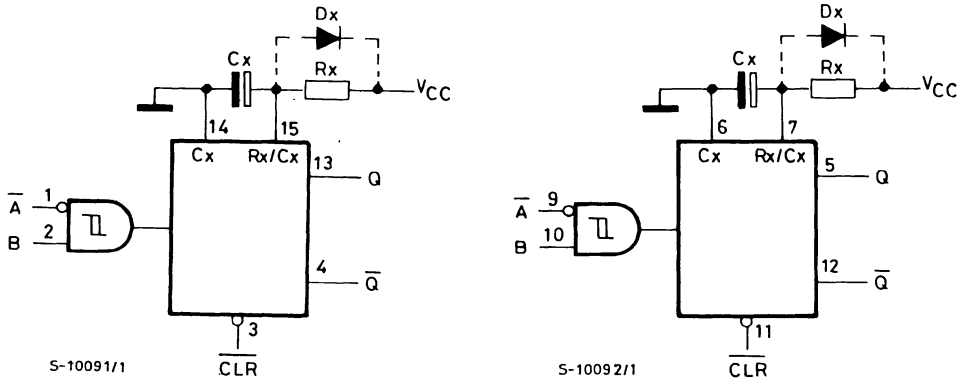
SYSTEM DIAGRAM



TIMING CHART



BLOCK DIAGRAM



Note :

(1) Cx, Rx, Dx are external components

(2) Dx is a clamping diode.

The external capacitor is charged to V_{CC} in the stand-by state, i.e. no trigger. When the supply voltage is turned off Cx is discharged mainly through an internal parasitic diode (see figures). If Cx is sufficiently large and V_{CC} decreases rapidy, there will be some possibility of damaging the I.C. with a surge current or latch-up If the voltage supply filter-capacitor is large enough and V_{CC} decrease slowly, the surge current is automatically limited and damage the I.C. is avoided The maximum forward current of the parasitic diode is approximately 20 mA. In cases where Cx is large the time taken for the supply voltage to fall to 0.4 V_{CC} can be calculated as follows :

$t_f \geq (V_{CC} - 0.7) \cdot Cx/20mA$

In cases where t_f is too short an external clamping diode is required to protect the I.C. from the surge current

FUNCTIONAL DESCRIPTION

STAND-BY STATE

The external capacitor, Cx, is fully charged to V_{CC} in the stand-by state. Hence, before triggering, transistor Qp and Qn (connected to the Rx/Cx node) are both turned-off. The two comparators that control the timing and the two reference voltage sources stop operating. The total supply current is therefore only leakage current.

TRIGGER OPERATION

Triggering occurs when :

1 st) A is "low" and B has a falling edge ;
2 nd) B is "high" and A has a rising edge ;
3 rd) A is low and B is high and C1 has a rising edge.

After the multivibrator has been retriggered comparator C1 and C2 start operating and Qn is turned on. Cx then discharges through Qn. The voltage at the node R/C external falls.

When it reaches V_{REFL} the output of comparator C1 becomes low. This in turn resets the flip-flop and Qn is turned off.

At this point C1 stops functioning but C2 continues to operate.

The voltage at R/C external begins to rise with a time constant set by the external components Rx, Cx.

Triggering the multivibrator causes Q to go high after internal delay due to the flip-flop and the gate. Q remains high until the voltage at R/C external rises again to V_{REFH}. At this point C2 output goes low and O goes low. C2 stop operating. That means that after triggering when the voltage R/C external returns to V_{REFH} the multivibrator has returned to its MONOSTABLE STATE. In the case where Rx · Cx are large enough and the discharge time of the capacitor and the delay time in the I.C. can be ignored, the width of the output pulse tw (out) is as follows :

$$t_{W(OUT)} = 0.46\ Cx \cdot Rx\ (HC123)$$

$$t_{W(OUT)} = Cx \cdot Rx\ (HC123A)$$

FUNCTIONAL DESCRIPTION (continued)

RE-TRIGGERED OPERATION

When a second trigger pulse follows the first its effect will depend on the state of the multivibrator. If the capacitor Cx is being charged the voltage level of R/C external falls to Vrefl again and Q remains high i.e. the retrigger pulse arrives in a time shorter than the period Rx · Cx seconds, the capacitor charging time constant. If the second trigger pulse is very close to the initial trigger pulse it is ineffective ; i.e. the second trigger must arrive in the capacitor discharge cycle to be ineffective; Hence the minimum time for a second trigger to be effective depends on V_{CC} and Cx.

RESET OPERATION

CL is normally high. If CL is low, the trigger is not effective because Q output goes low and trigger control flip-flop is reset.

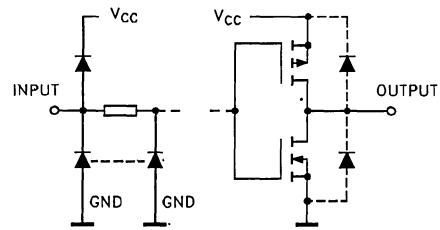
Also transistor Op is turned on and Cx is charged quicky to V_{CC}. This means if CL input goes low, the IC becomes waiting state both in operating and non operating state.

TRUTH TABLE

INPUTS			OUTPUTS		NOTE
$\overline{A}$	B	$\overline{CL}$	Q	$\overline{Q}$	
⌐	H	H	⌐¬	¬⌊	OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L	⌐	H	⌐¬	¬⌊	OUTPUT ENABLE
L	H	⌐	⌐¬	¬⌊	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X: Don't Care · Z: High Impedance

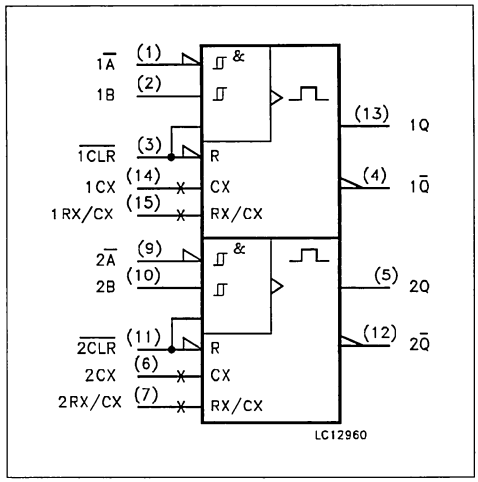
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 9	$1\overline{A}$, $2\overline{A}$	Trigger Inputs (Negative Edge Triggered)
2, 10	1B, 2B	Trigger Inputs (Positive Edge Triggered)
3, 11	$1\overline{CLR}$, $2\overline{CLR}$	Direct Reset LOW and Trigger Action at Positive Edge
4, 12	$1\overline{Q}$, $2\overline{Q}$	Outputs (Active LOW)
7	$2R_{EXT}/C_{EXT}$	External Resistor Capacitor Connection
13, 5	1Q, 2Q	Outputs (Active HIGH)
14, 6	$1C_{EXT}$ $2C_{EXT}$	External Capacitor Connection
15	$1R_{EXT}/C_{EXT}$	External Resistor Capacitor Connection
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C· 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time		0 to 1000	ns
			0 to 500	
			0 to 400	
C_X	External Capacitor		NO LIMITATION	pF
R_X	External Resistor	V_{CC} < 3 V	5K to 1M	Ω
		V_{CC} ≥ 3 V	1K to 1M	

(*) The maximum allowable values of Cx and Rx are a function of leakage of capacitor Cx, the leakage of device and leakage due to the board layout and surface resistance. Susceptibility to externally induced noise may occur for Rx > 1MΩ

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 μA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 μA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	μA
I_I	R/C Terminal Off State Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	μA
I_{CC}'	Active State Supply Current (1)	2.0	V_I = V_{CC} or GND Pin 7 or 15 V_{IN} = V_{CC}/2			45	200		260		320	μA
		4.5				500	600		780		960	μA
		6.0				0.7	1		1.3		1.6	mA

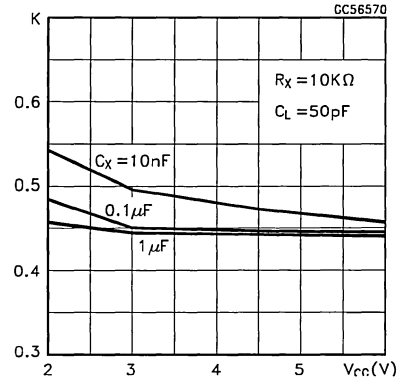
(1): Per Circuit

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

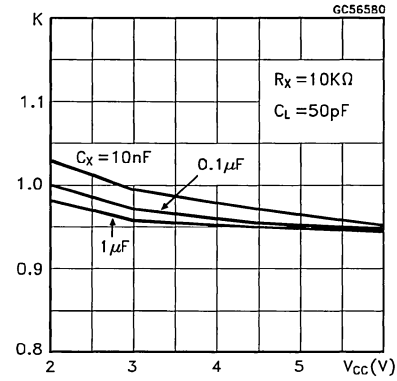
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{A}$, B - Q, $\overline{Q}$)	2.0			102	210		265		315	ns
		4.5			29	42		53		63	
		6.0			22	36		45		54	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$ TRIGGER - Q, $\overline{Q}$)	2.0			102	235		295		355	ns
		4.5			31	47		59		71	
		6.0			23	40		50		60	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$ - Q, $\overline{Q}$)	2.0			68	160		200		240	ns
		4.5			20	32		40		48	
		6.0			16	27		34		41	
t_{WOUT}	Output Pulse Width (for HC123)	2.0	C_X = 100 pF R_X = 10 KΩ		1.4						µs
		4.5			1.2						
		6.0			1.1						
		2.0	C_X = 0.1 µF R_X = 100 KΩ		4.6						ms
		4.5			4.4						
		6.0			4.3						
t_{WOUT}	Output Pulse Width (for HC123A)	2.0	C_X = 100 pF R_X = 10 KΩ		1.9						µs
		4.5			1.6						
		6.0			1.5						
		2.0	C_X = 0.1 µF R_X = 100 KΩ		9.8						ms
		4.5			9.5						
		6.0			9.4						
Δt_{WOUT}	Output Pulse Width Error Between Circuits in Same Package				±1						%
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width	2.0				75		95		110	ns
		4.5				15		19		22	
		6.0				13		16		19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLR}$)	2.0				75		95		110	ns
		4.5				15		19		22	
		6.0				13		16		19	
t_{rr}	Minimum Retrigger Time	2.0	C_X = 100 pF R_X = 1 KΩ		325						ns
		4.5			108						
		6.0			78						
		2.0	C_X = 0.1 µF R_X = 100 KΩ		5						µs
		4.5			1.4						
		6.0			1.2						
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				162						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$' Duty/100 + I_C/2 (per monostable) (I_{CC}': Active Supply Current) (Duty:%)

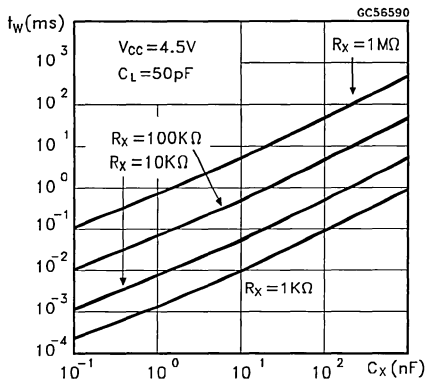
Output Pulse Width Constant Characteristics (for HC123)



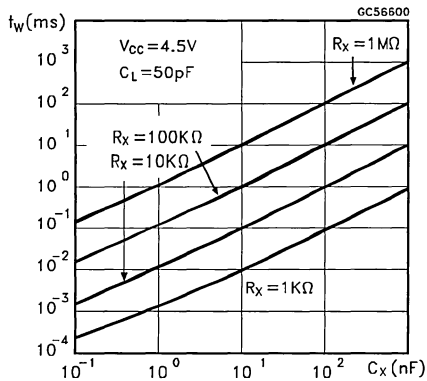
Output Pulse Width Constant Characteristics (for HC123A)



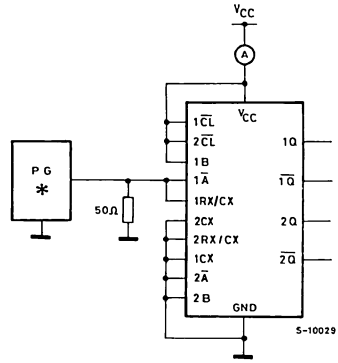
Output Pulse Width Characteristics (for HC123)



Output Pulse Width Characteristics (for HC123A)

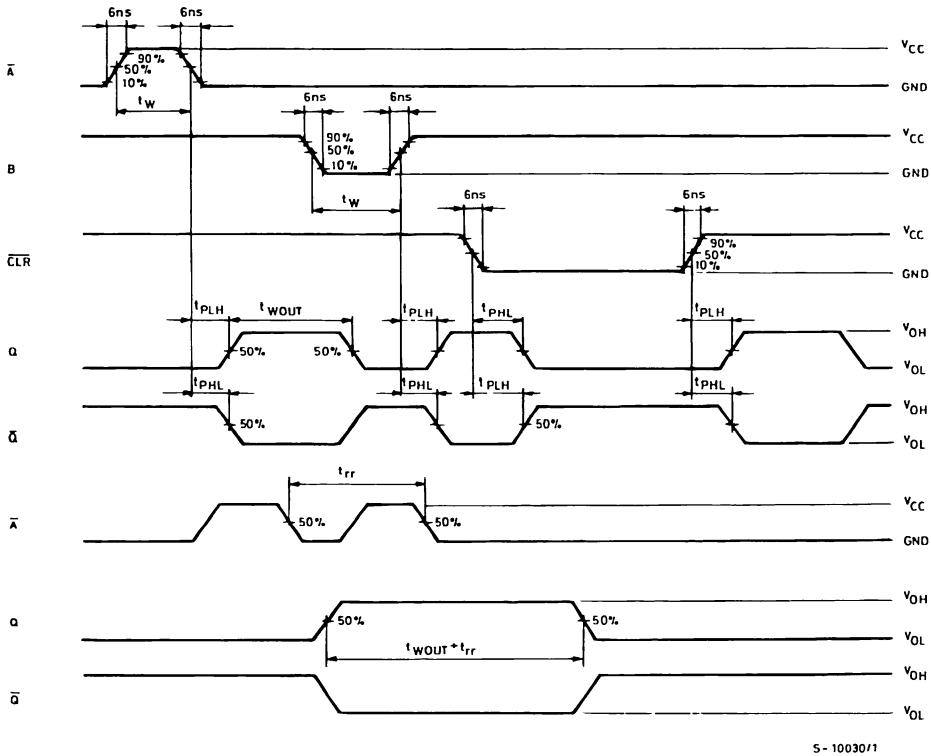


TEST CIRCUIT Icc (Opr)



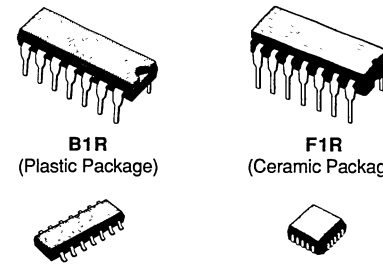
* TRANSITION TIME OF INPUT WAVEFORM IS THE SAME AS THAT IN SASE OF SWITCHING CHARACTERISTICS TESTS.

SWITCHING CHARACTERISTICS TEST WAVEFORM



QUAD BUS BUFFERS (3-STATE)

- HIGH SPEED
  t_{PD} = 8 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT 25 °C
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- SYMMETRICAL OUTPUT IMPEDANCE
  $I_{OL} = |I_{OH}|$ = 6 mA (MIN.)
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS125/126



B1R (Plastic Package)

F1R (Ceramic Package)

M1R (Micro Package)

C1R (Chip Carrier)

ORDER CODES :

M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

DESCRIPTION

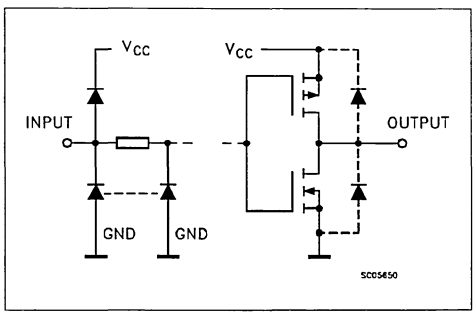
The M54/74HC125/126 are high speed CMOS QUAD BUS BUFFER (3-STATE) FABRICATED IN SILICON GATE C^2MOS technology.

They have the same high speed performance of LSTTL combined with true CMOS low power consumption.

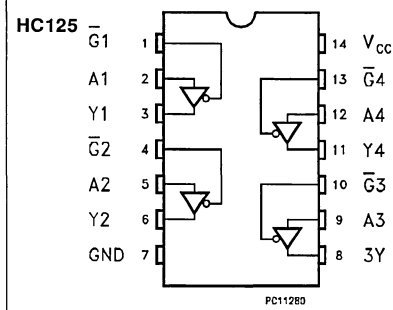
These devices require the same 3-STATE control input G to be taken high to make the output go into the high impedance state.

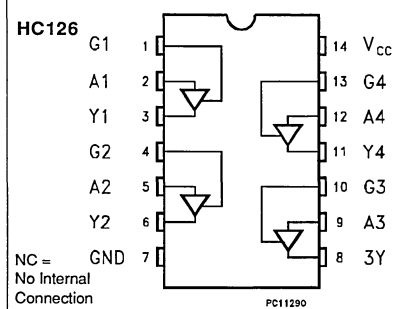
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



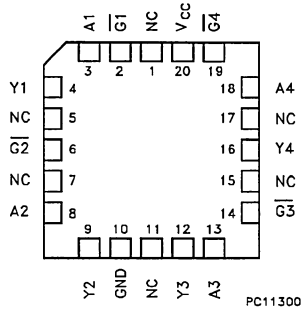
PIN CONNECTIONS (top view)



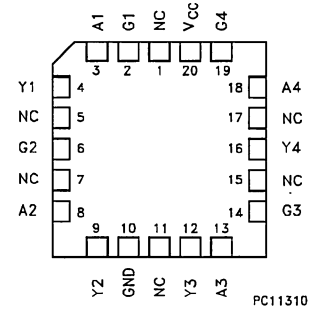


CHIP CARRIER

HC125



HC126



TRUTH TABLE (HC125)

A	$\overline{G}$	Y
X	H	Z
L	L	L
H	L	H

TRUTH TABLE (HC126)

A	G	Y
X	L	Z
L	H	L
H	H	H

PIN DESCRIPTION (HC125)

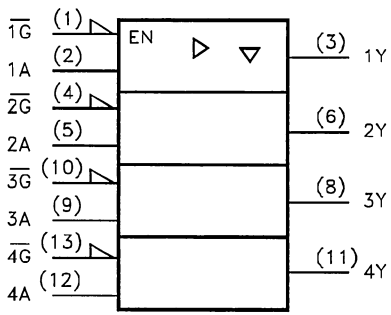
PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	$\overline{G1}$ to $\overline{G4}$	Output Enable Input
2, 5, 9, 12	A1 to A4	Data Inputs
3, 6, 8, 11	Y1 to Y4	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

PIN DESCRIPTION (HC126)

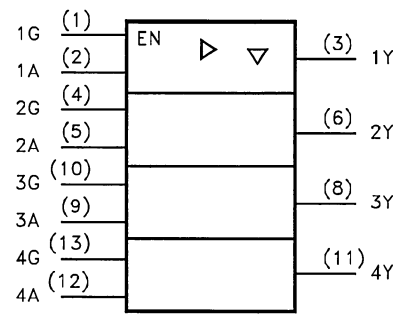
PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	G1 to G4	Output Enable Input
2, 5, 9, 12	A1 to A4	Data Inputs
3, 6, 8, 11	Y1 to Y4	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS

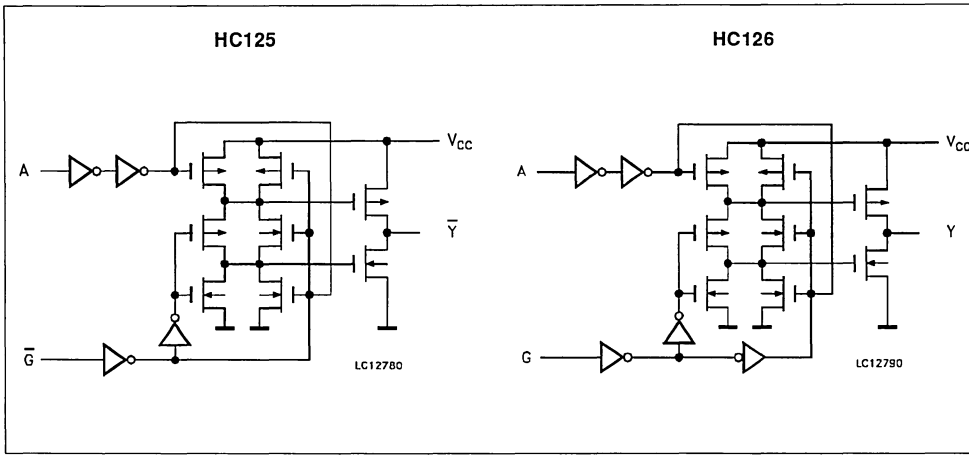
HC125



HC126



CIRCUIT DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

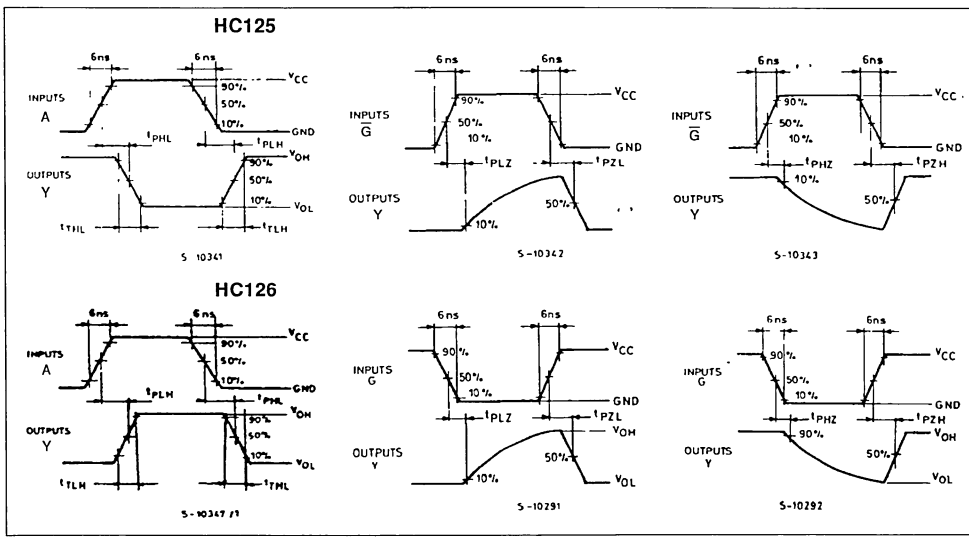
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off-state Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			20	60		75		90	ns
		4.5				6	12		15		18	
		6.0				5	10		13		15	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0	50			36	75		95		110	ns
		4.5				9	15		19		22	
		6.0				8	13		16		19	
		2.0	150			52	105		130		160	ns
		4.5				13	21		26		32	
		6.0				11	18		22		27	
t_{PZL} t_{PZH}	3 State Output Enable Time	2.0	50	R_L = 1 KΩ		36	75		95		110	ns
		4.5				9	15		19		22	
		6.0				8	13		16		19	
		2.0	150	R_L = 1 KΩ		52	105		130		160	ns
		4.5				13	21		26		32	
		6.0				11	18		22		27	
t_{PLZ} t_{PHZ}	3 State Output Disable Time	2.0	50	R_L = 1 KΩ		48	80		100		120	ns
		4.5				12	16		20		24	
		6.0				10	14		17		20	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance					35						pF

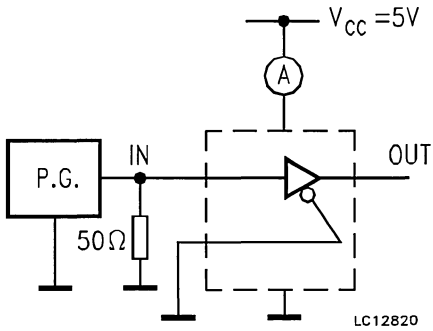
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

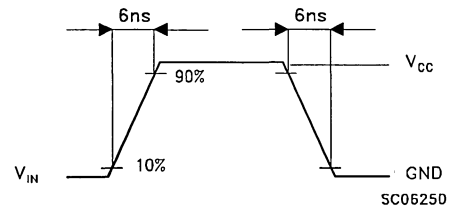
SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)

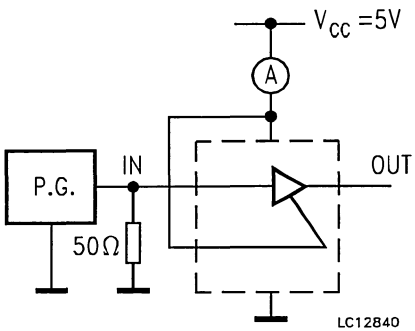
HC125

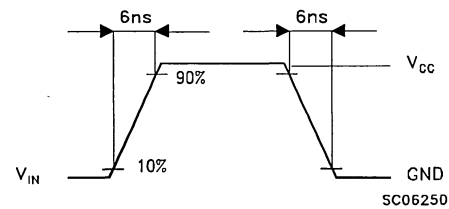




THE OTHER INPUTS ARE CONNECTED TO V_{CC} LINE OR GND LINE

HC126



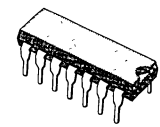


THE OTHER INPUTS ARE CONNECTED TO V_{CC} LINE OR GND LINE

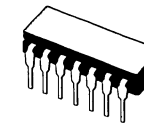
M54/74HCT125
M54/74HCT126

QUAD BUS BUFFERS (3-STATE)

- HIGH SPEED
  t_{PD} = 12 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT 25 °C
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- SYMMETRICAL OUTPUT IMPEDANCE
  $I_{OL} = |I_{OH}|$ = 6 mA (MIN.)
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS125/126



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

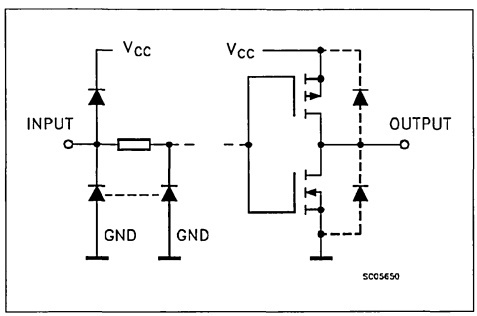
ORDER CODES :

M54HCTXXXF1R M74HCTXXXM1R
M74HCTXXXB1R M74HCTXXXC1R

DESCRIPTION

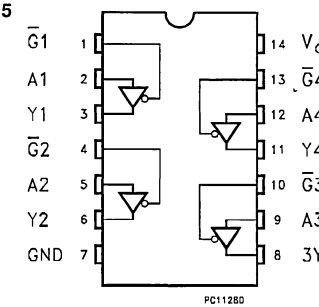
The M54/74HCT125/126 are high speed CMOS QUAD BUS BUFFER (3-STATE) FABRICATED IN SILICON GATE C^2MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. These devices require the same 3-STATE control input G to be taken high to make the output go into the high impedance state.This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT

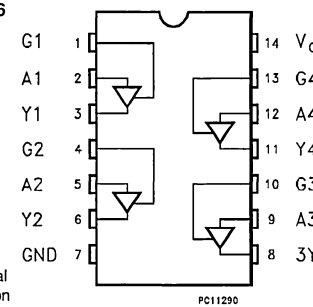


PIN CONNECTIONS (top view)

HCT125



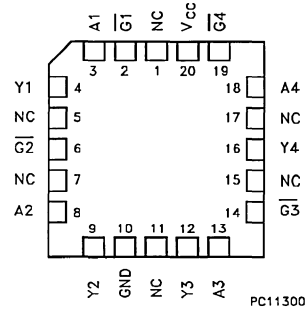
HCT126



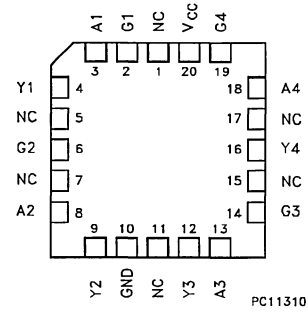
NC = No Internal Connection

CHIP CARRIER

HCT125



HCT126



TRUTH TABLE (HCT125)

A	$\overline{G}$	Y
X	H	Z
L	L	L
H	L	H

TRUTH TABLE (HCT126)

A	G	Y
X	L	Z
L	H	L
H	H	H

PIN DESCRIPTION (HCT125)

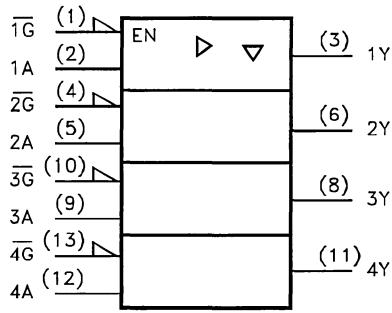
PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	$\overline{G1}$ to $\overline{G4}$	Output Enable Input
2, 5, 9, 12	A1 to A4	Data Inputs
3, 6, 8, 11	Y1 to Y4	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

PIN DESCRIPTION (HCT126)

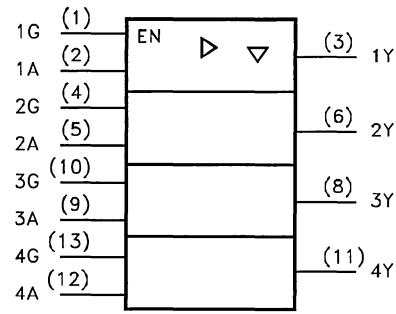
PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	G1 to G4	Output Enable Input
2, 5, 9, 12	A1 to A4	Data Inputs
3, 6, 8, 11	Y1 to Y4	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS

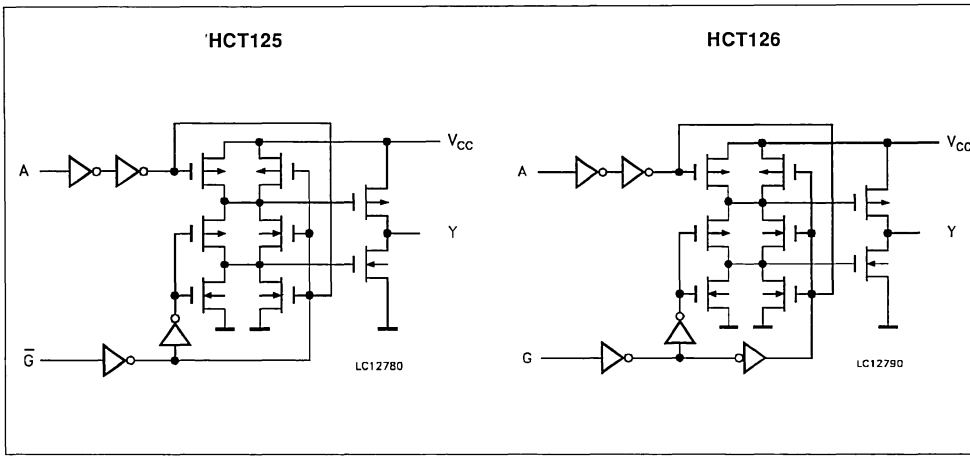
HCT125



HCT126



CIRCUIT DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

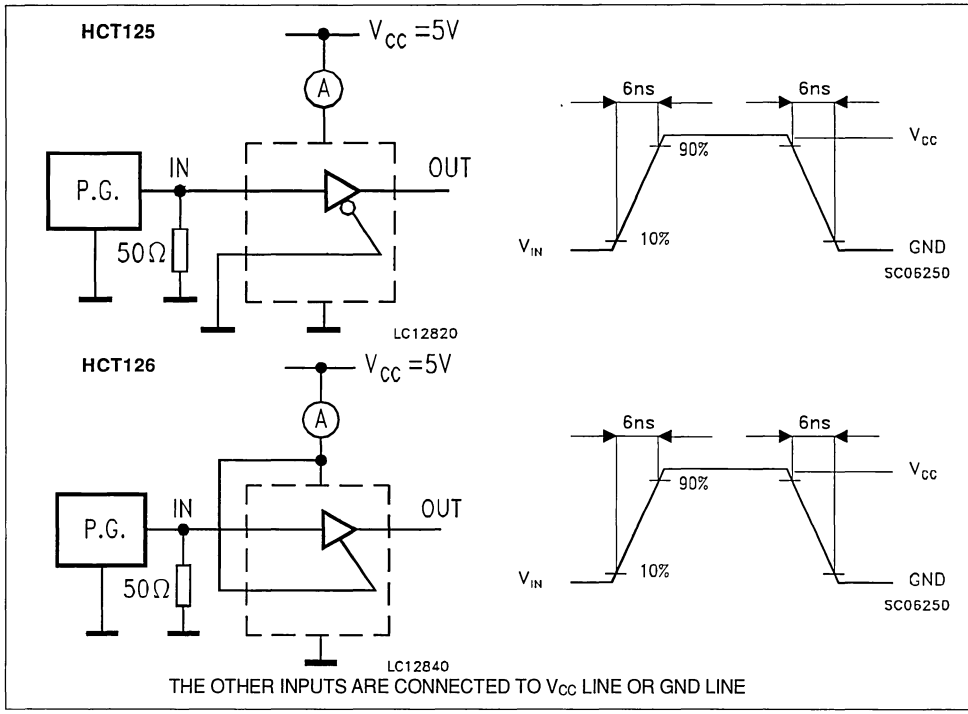
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-6.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 6.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				4		40		80	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5		±10	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9		3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5	50			7	12		15		18	ns
t_{PLH} t_{PHL}	Propagation Delay Time	4.5	50			13	21		26		32	ns
		4.5	150			17	27		34		41	ns
t_{PZL} t_{PZH}	3 State Output Enable Time	4.5	50	R_L = 1 KΩ		15	24		30		36	ns
		4.5	150	R_L = 1 KΩ		19	30		38		45	ns
t_{PLZ} t_{PHZ}	3 State Output Disable Time	4.5	50	R_L = 1 KΩ		17	24		30		36	ns
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance					56						pF

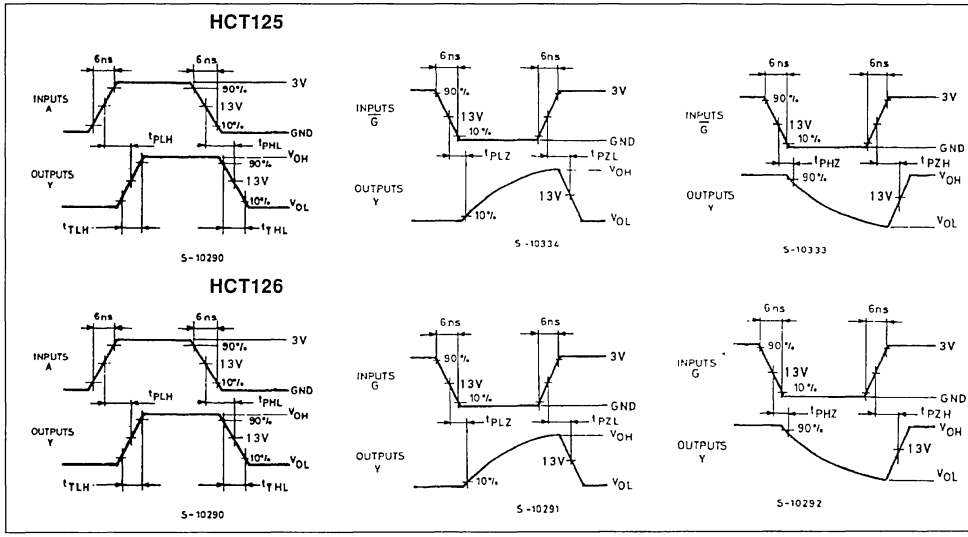
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

TEST CIRCUIT I_{CC} (Opr.)



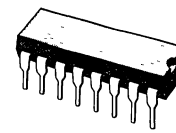
THE OTHER INPUTS ARE CONNECTED TO V_{CC} LINE OR GND LINE

SWITCHING CHARACTERISTICS TEST WAVEFORM

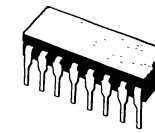


3 TO 8 LINE DECODER/LATCH

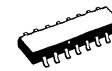
- HIGH SPEED
  t_{PD} = 22 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY
  VNIH = VNIL = 28 % VCC (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC}(OPR) = 2 V to 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS131



B1R
(Plastic Package)



F1R
(Ceramic Package)



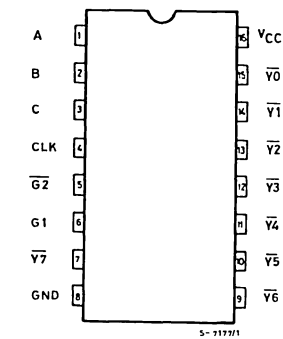
M1R
(Micro Package)

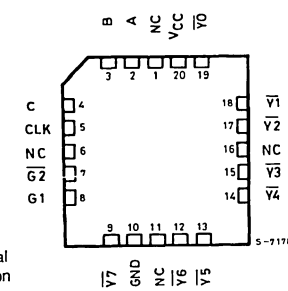
C1R
(Chip Carrier)

ORDER CODES :

M54HC131F1R M74HC131M1R
M74HC131B1R M74HC131C1R

PIN CONNECTIONS (top view)





NC =
No Internal
Connection

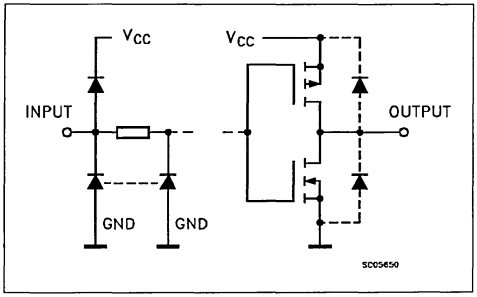
DESCRIPTION

The M54/74HC131 is a high speed CMOS 3 TO 8 LINE DECODER/LATCH fabricated in silicon gate C2MOS technology.

It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This device is a DECODER/LATCH capable of selecting arbitrarily one of eight outputs by three binary inputs A, B, and C, in this case, the selected output is at logic "low".

Also, when ENABLE input G1 is set low or ENABLE input $\overline{G2}$ is set high, selection is inhibited regardless of other input signals and all the outputs are at high. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

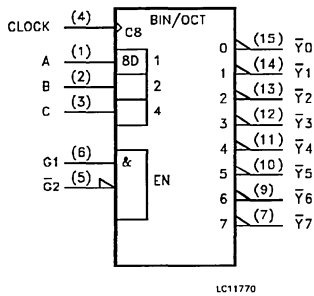
INPUT AND OUTPUT EQUIVALENT CIRCUIT

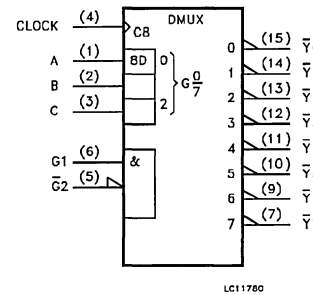


PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3	A, B, C	Data Inputs
4	CLK	Clock Input (LOW to HIGH, Edge-triggered)
5	$\overline{G2}$	Enable (Active LOW)
6	G1	Enable (Active HIGH)
9, 10, 11, 12, 13, 14, 15, 7	$\overline{Y0}$, $\overline{Y1}$, $\overline{Y2}$, $\overline{Y3}$, $\overline{Y4}$, $\overline{Y5}$, $\overline{Y6}$, $\overline{Y7}$	Data Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL

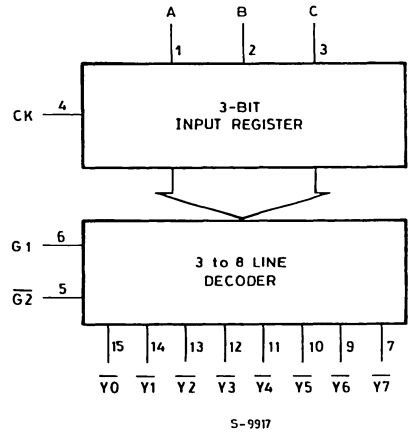




TRUTH TABLE

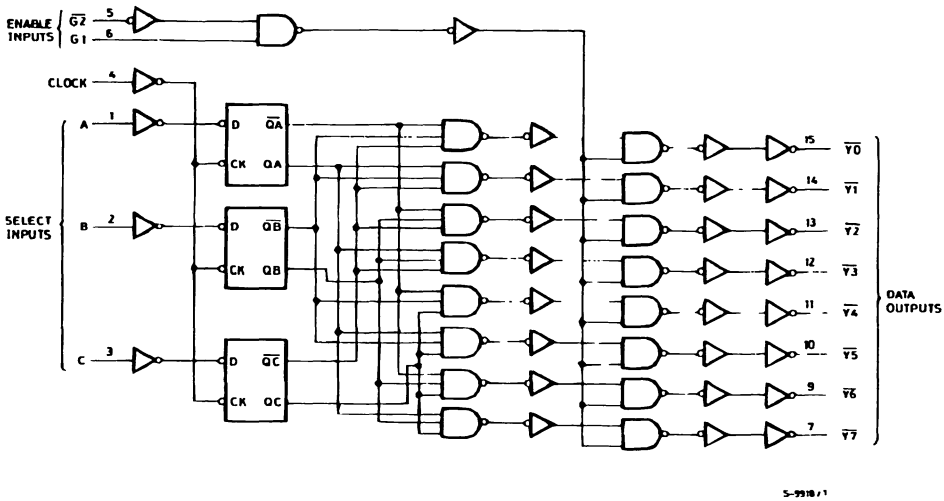
INPUTS						OUTPUTS							
CLK	ENABLE		SELECT										
	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
⎍	H	L	L	L	L	L	H	H	H	H	H	H	H
⎍	H	L	L	L	H	H	L	H	H	H	H	H	H
⎍	H	L	L	H	L	H	H	L	H	H	H	H	H
⎍	H	L	L	H	H	H	H	H	L	H	H	H	H
⎍	H	L	H	L	L	H	H	H	H	L	H	H	H
⎍	H	L	H	L	H	H	H	H	H	H	L	H	H
⎍	H	L	H	H	L	H	H	H	H	H	H	L	H
⎍	H	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	X	X	X	Outputs corresponding to stored address L: all others H							

BLOCK DIAGRAM



V_{CC} = 16
GND = 8

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

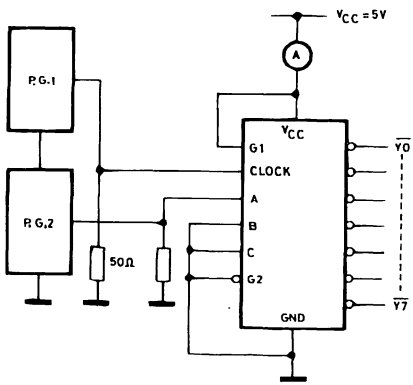
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

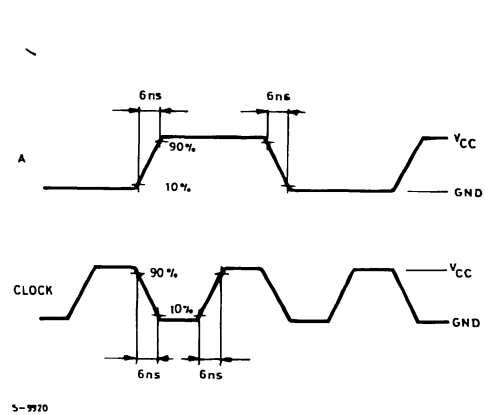
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - $\overline{Yn}$)	2.0			78	200		250		300	ns
		4.5			26	40		50		60	
		6.0			22	34		43		51	
t_{PLH} t_{PHL}	Propagation Delay Time (G - $\overline{Yn}$)	2.0			60	140		175		210	ns
		4.5			15	28		35		42	
		6.0			13	24		30		36	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0			20	75		95		110	ns
		4.5			6	15		19		22	
		6.0			6	13		16		19	
t_s	Minimum Set-up Time	2.0			25	50		65		75	ns
		4.5			5	10		13		15	
		6.0			5	9		11		13	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				37						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

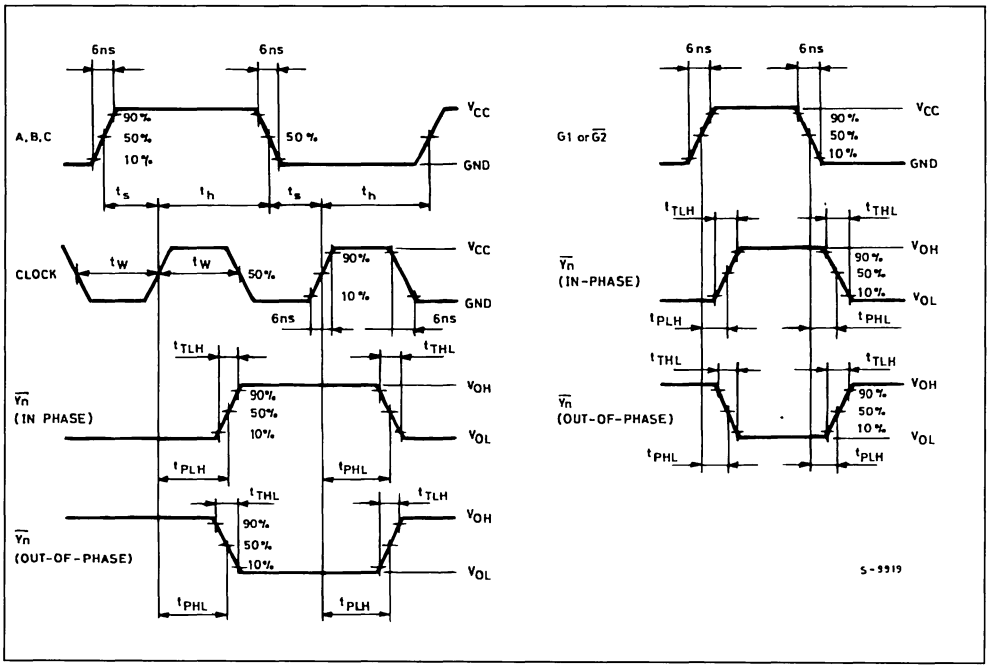
SWITCHING CHARACTERISTICS TEST CIRCUIT



INPUT WAVEFORM

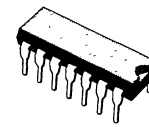


SWITCHING CHARACTERISTICS TEST WAVEFORM

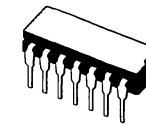


QUAD 2-INPUT SCHMITT NAND GATE

- HIGH SPEED
  t_{PD} = 11 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1μA (MAX.) AT T_A = 25 °C
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- HIGH NOISE IMMUNITY
  V_H (TYP.) = 0.9 V AT V_{CC} = 5 V
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS132



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

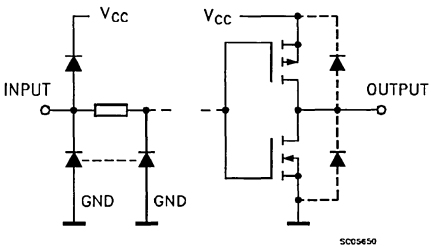
M54HC132F1R M74HC132M1R
M74HC132B1R M74HC132C1R

DESCRIPTION

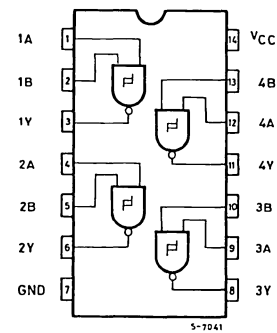
The M54/74HC132 is a high speed CMOS QUAD 2-INPUT SCHMITT NAND GATE fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. Pin configuration and function are identical to those of the M54/74HC00.

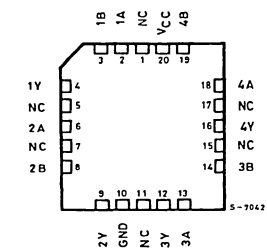
The hysterisis characteristics (around 20 % V_{CC}) of all inputs allow slowly changing input signals to be transformed into sharply defined jitter-free output signals. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



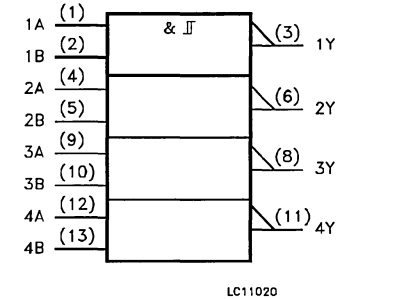


NC =
No Internal
Connection

TRUTH TABLE

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

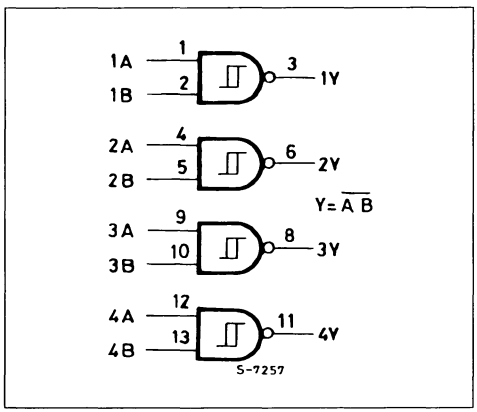
IEC LOGIC SYMBOL



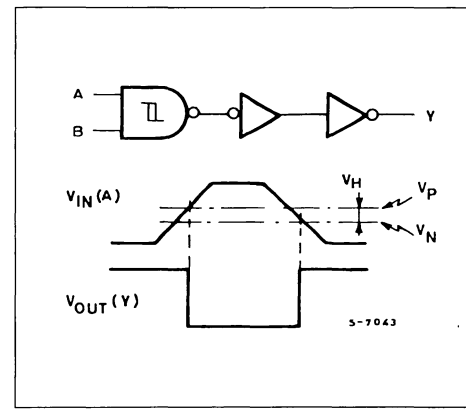
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data Inputs
2, 5, 10, 13	1B to 4B	Data Inputs
3, 6, 8, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

BLOCK DIAGRAM



LOGIC DIAGRAM/WAVEFORM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	No Limits	

DC SPECIFICATIONS

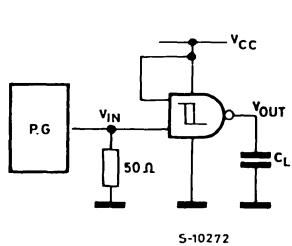
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_P	High Level Threshold Voltage	2.0			1.0	1.25	1.5	1.0	1.5	1.0	1.5	V
		4.5			2.3	2.7	3.15	2.3	3.15	2.3	3.15	
		6.0			3.0	3.5	4.2	3.0	4.2	3.0	4.2	
V_N	Low Level Threshold Voltage	2.0			0.3	0.65	0.9	0.3	0.9	0.3	0.9	V
		4.5			1.13	1.6	2.0	1.13	2.0	1.13	2.0	
		6.0			1.5	2.3	2.6	1.5	2.6	1.5	2.6	
V_H	Hysteresis Voltage	2.0			0.3	0.6	1.0	0.3	1.0	0.3	1.0	V
		4.5			0.6	1.1	1.4	0.6	1.4	0.6	1.4	
		6.0			0.8	1.2	1.4	0.8	1.7	0.8	1.7	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 μA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 μA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	μA

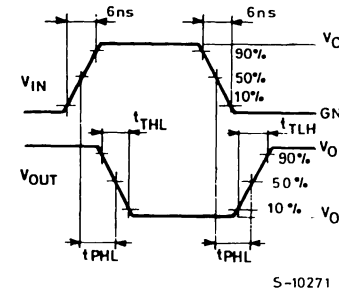
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			52	105		130		160	ns
		4.5			13	21		26		32	
		6.0			11	18		22		27	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				29						pF

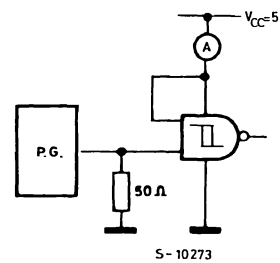
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



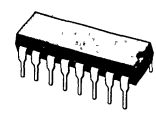


TEST CIRCUIT I_{CC} (Opr.)

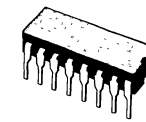


13 INPUT NAND GATE

- HIGH SPEED
  t_{PD} = 13 ns (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) at T_A = 25° C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OutpuT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V to 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS133



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

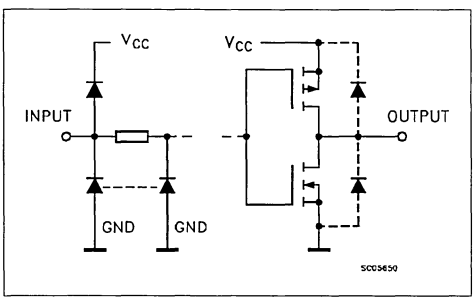
M54HC133F1R M74HC133M1R
M74HC133B1R M74HC133C1R

DESCRIPTION

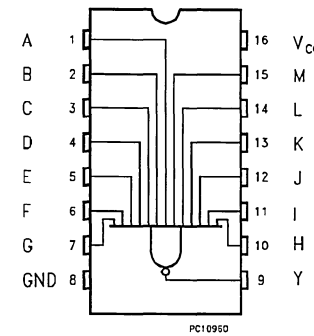
The M54/74HC133 is a high speed CMOS 13-INPUT NAND GATE fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

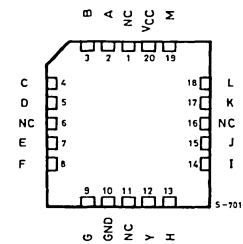
The internal circuit is composed of 7 stages including buffer output, which gives high noise immunity and stable output. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





NC =
No Internal
Connection

TRUTH TABLE

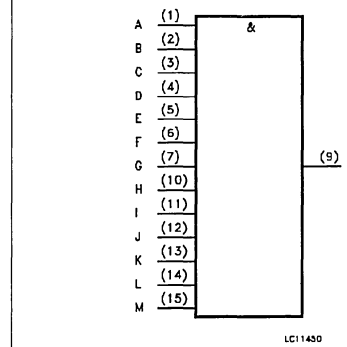
A	B	C	D	E	F	G	H	I	J	K	L	M	Y
L	X	X	X	X	X	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	X	X	X	X	X	H
X	X	X	L	X	X	X	X	X	X	X	X	X	H
X	X	X	X	L	X	X	X	X	X	X	X	X	H
X	X	X	X	X	L	X	X	X	X	X	X	X	H
X	X	X	X	X	X	L	X	X	X	X	X	X	H
X	X	X	X	X	X	X	L	X	X	X	X	X	H
X	X	X	X	X	X	X	X	L	X	X	X	X	H
X	X	X	X	X	X	X	X	X	L	X	X	X	H
X	X	X	X	X	X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	H	H	H	H	H	L

X: Don't Care

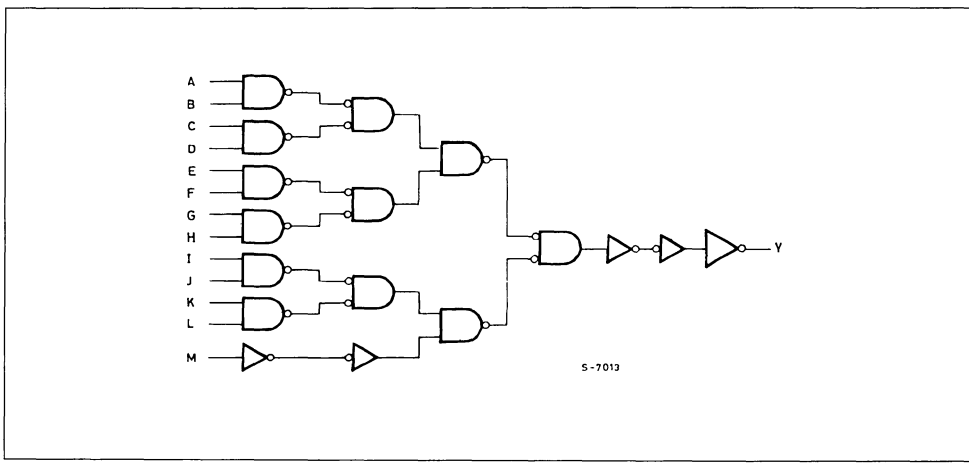
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1 to 7, 10 to 15	A to G, H to M	Data Inputs
9	Y	Data Output
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



LOGIC DIAGRAM (1/2 Package)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series		-55 to +125	°C
	M74HC Series		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

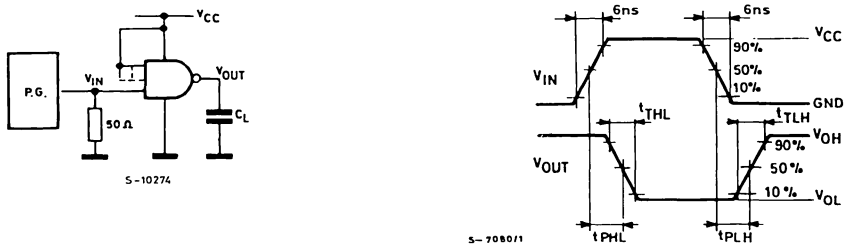
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

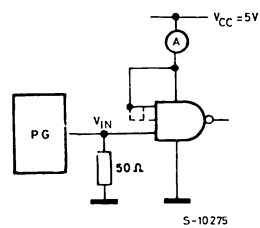
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			42	130		165		195	ns
		4.5			16	26		33		39	
		6.0			14	22		28		33	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				29						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST CIRCUIT



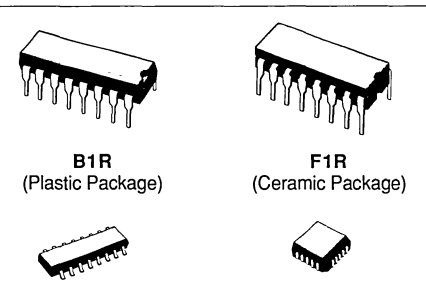
TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

3 TO 8 LINE DECODER/LATCH (INVERTING)

- HIGH SPEED
  t_{PD} = 11 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS137



B1R
(Plastic Package)

F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

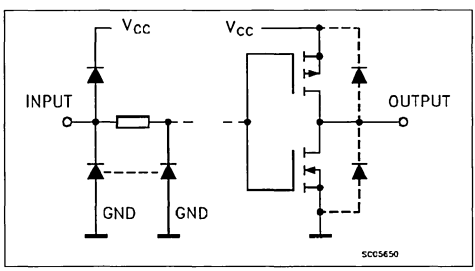
ORDER CODES :

M54HC137F1R M74HC137M1R
M74HC137B1R M74HC137C1R

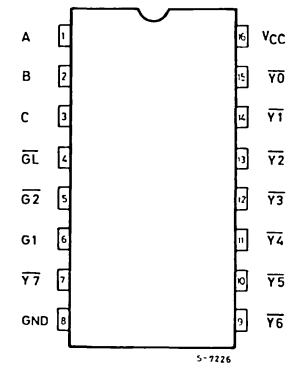
DESCRIPTION

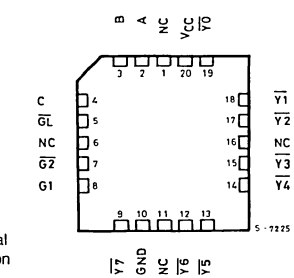
The M54/74HC137 is a high speed CMOS 3 TO 8 LINE DECODER/LATCH (INVERTING) fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This device is a 3 to 8 line decoder with latches on the three address inputs. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B and C) is stored in the latches. As long as $\overline{GL}$ remains high no address changes will be recognized. Output enable pins G1 and $\overline{G2}$, control the state of the outputs independently of the select or latch-enable inputs. All the outputs are high unless G1 is high and $\overline{G2}$ is low. The HC137 is ideally suited for the implementation of glitch-free decoders in stored-address applications in bus oriented systems. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



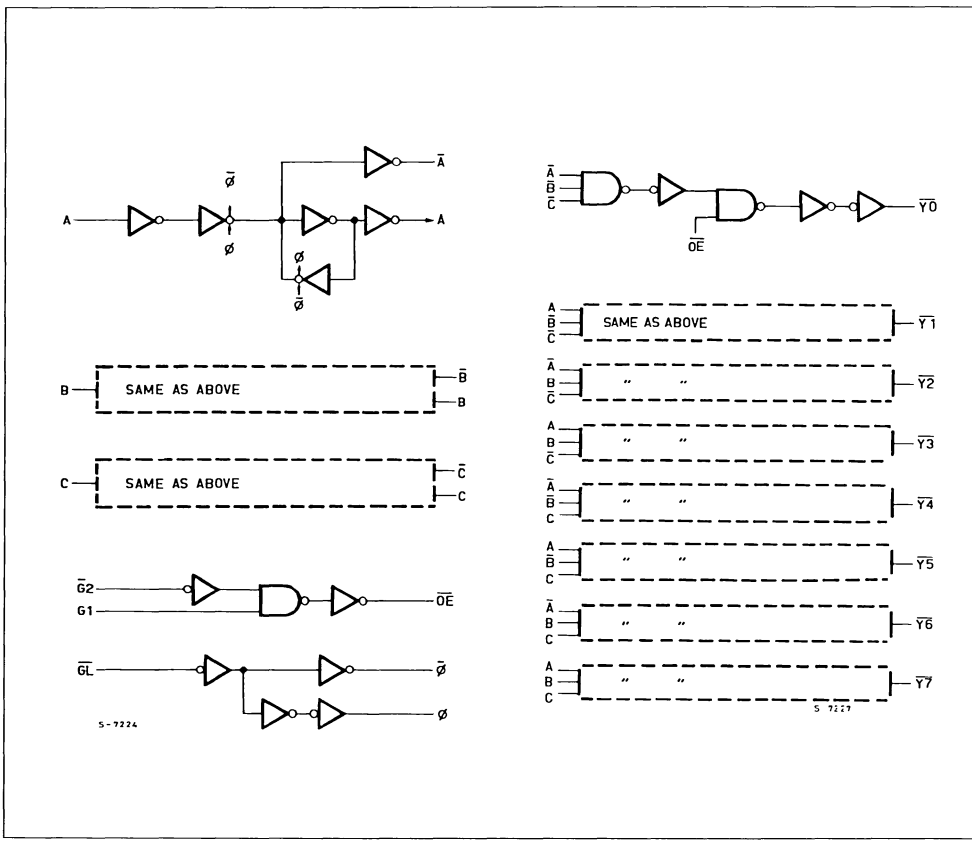


NC =
No Internal
Connection

TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Outputs corresponding to stored address L: all others H							

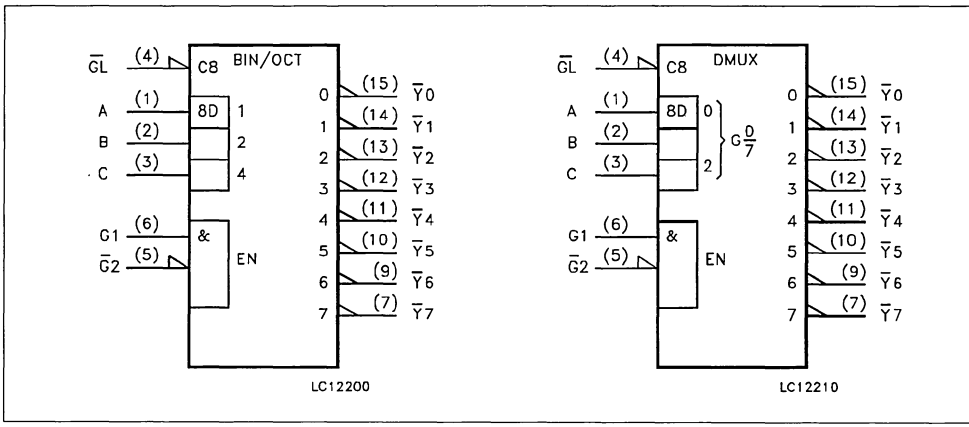
LOGIC DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3	A to C	Data Inputs
4	$\overline{GL}$	Latch Enable Input (Active LOW)
5	$\overline{G2}$	Data Enable Input (Active LOW)
6	G1	Data Enable Input (Active HIGH)
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y0}$ to $\overline{Y7}$	Multiplexer Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

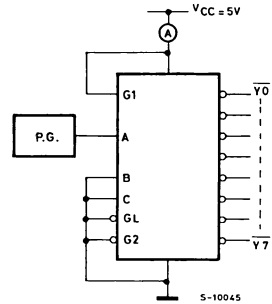
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				2		20		40	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (G1 - $\overline{Y}$)	2.0			45	115		145		175	ns
		4.5			14	23		29		35	
		6.0			12	20		25		30	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{G2}$ - $\overline{Y}$)	2.0			50	115		145		175	ns
		4.5			15	23		29		35	
		6.0			13	20		25		30	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{GL}$ - $\overline{Y}$)	2.0			70	170		215		250	ns
		4.5			22	34		43		50	
		6.0			19	29		37		43	
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C - $\overline{Y}$)	2.0			70	165		205		110	ns
		4.5			21	33		41		22	
		6.0			18	28		35		19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{GL}$)	2.0			12	50		65		75	ns
		4.5			3	10		13		15	
		6.0			3	9		11		13	
t_s	Minimum Set-up Time (A, B, C - $\overline{GL}$)	2.0			8	50		60		75	ns
		4.5			2	10		12		15	
		6.0			2	9		10		13	
t_h	Minimum Hold Time (A, B, C - $\overline{GL}$)	2.0				5		5		5	ns
		4.5				5		5		5	
		6.0				5		5		5	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				55						pF

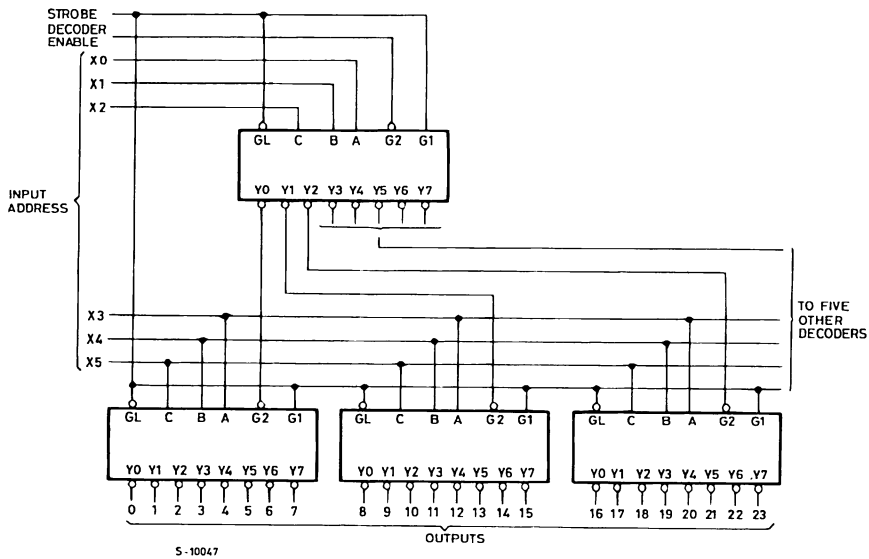
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

TEST CIRCUIT I_{CC} (Opr.)



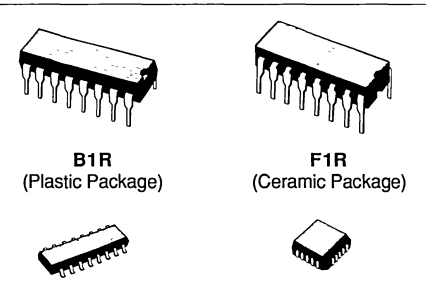
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TYPICAL APPLICATION



3 TO 8 LINE DECODER/LATCH (INVERTING)

- HIGH SPEED
  t_{PD} = 17 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS137



B1R
(Plastic Package)

F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

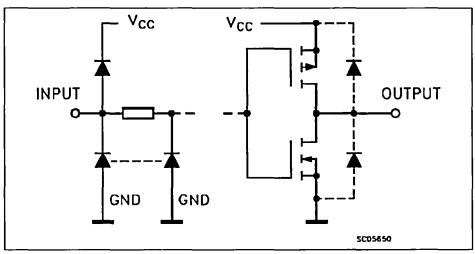
ORDER CODES :

M54HCT137F1R M74HCT137M1R
M74HCT137B1R M74HCT137C1R

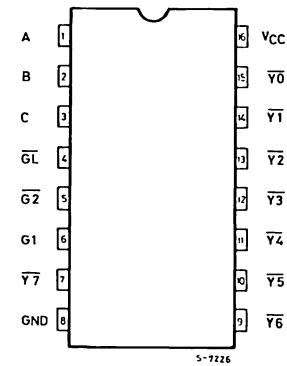
DESCRIPTION

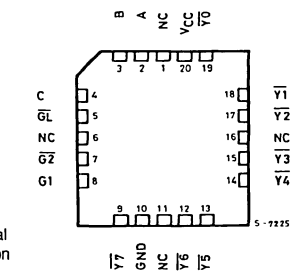
The M54/74HCT137 is a high speed CMOS 3 TO 8 LINE DECODER/LATCH (INVERTING) fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This device is a 3 to 8 line decoder with latches on the three address inputs. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B and C) is stored in the latches. As long as $\overline{GL}$ remains high no address changes will be recognized. Output enable pins G1 and $\overline{G2}$, control the state of the outputs independently of the select or latch-enable inputs. All the outputs are high unless G1 is high and $\overline{G2}$ is low. The HC137 is ideally suited for the implementation of glitch-free decoders in stored-address applications in bus oriented systems. All inputs are equipped with protection circuits against static discharge and transient excess voltage. This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



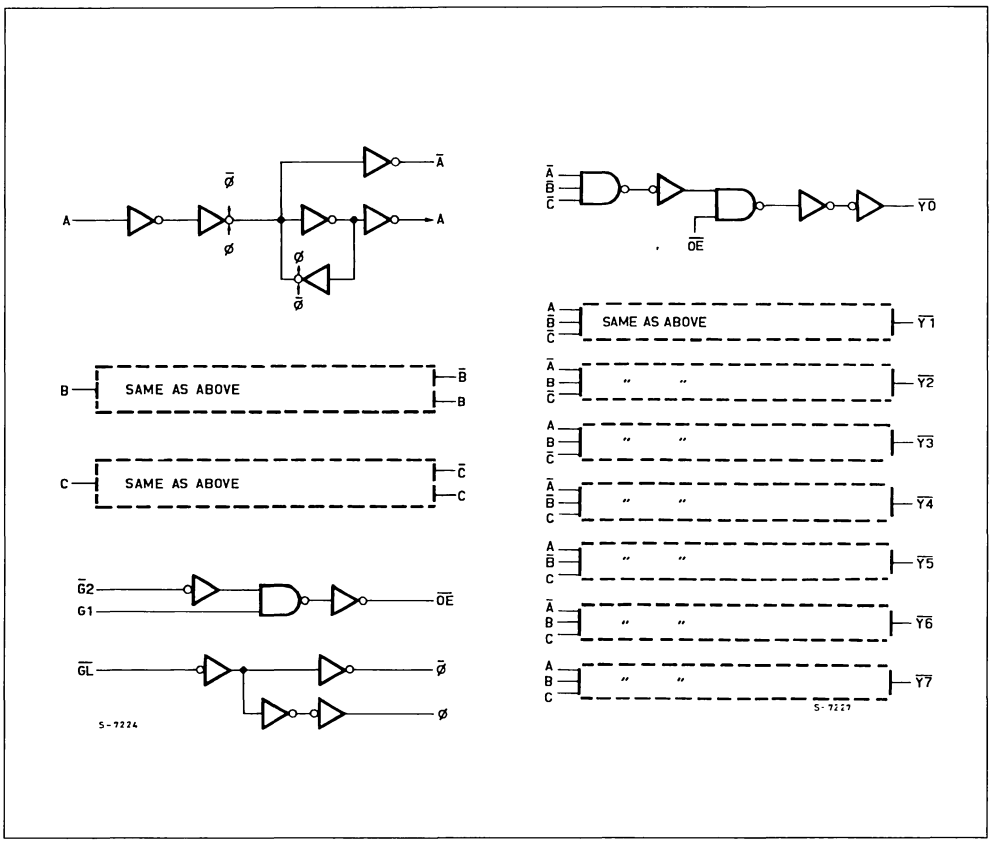


NC =
No Internal
Connection

TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	L	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Outputs corresponding to stored address L: all others H							

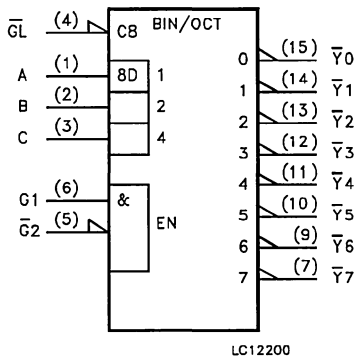
LOGIC DIAGRAM



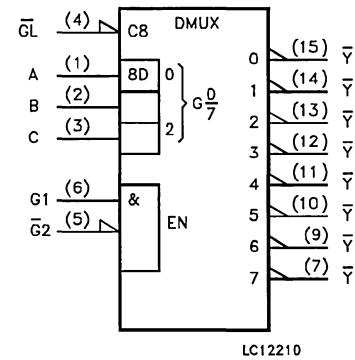
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3	A to C	Data Inputs
4	$\overline{GL}$	Latch Enable Input (Active LOW)
5	$\overline{G2}$	Data Enable Input (Active LOW)
6	G1	Data Enable Input (Active HIGH)
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y0}$ to $\overline{Y7}$	Multiplexer Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS



LC12200



LC12210

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

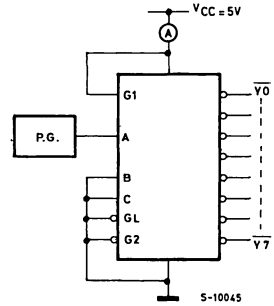
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				4		40		80	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9		3.0	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			8	15		19		22	ns
t_{PLH} t_{PHL}	Propagation Delay Time (G1 - $\overline{Y}$)	4.5			17	27		34		41	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{G2}$ - $\overline{Y}$)	4.5			18	28		35		42	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{GL}$ - $\overline{Y}$)	4.5			25	39		49		59	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C - $\overline{Y}$)	4.5			24	37		46		56	ns
$t_{W(L)}$	Minimum Pulse Width ($\overline{GL}$)	4.5			8	15		19		22	ns
t_s	Minimum Set-up Time (A, B, C - $\overline{GL}$)	4.5				5		6		8	ns
t_h	Minimum Hold Time (A, B, C - $\overline{GL}$)	4.5				5		6		8	ns
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				58						pF

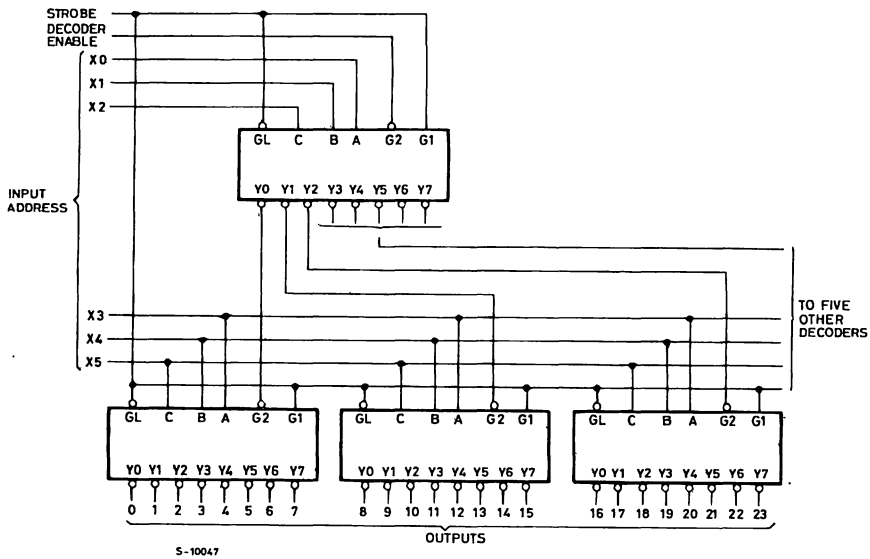
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

TEST CIRCUIT I_{CC} (Opr.)

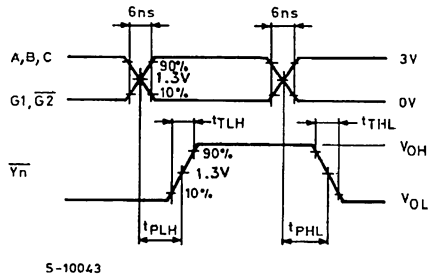


INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

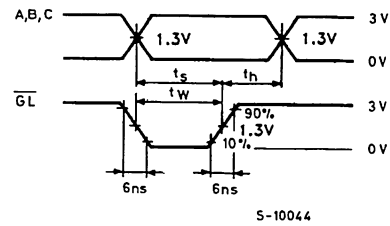
TYPICAL APPLICATION



SWITCHING CHARACTERISTICS TEST WAVEFORM



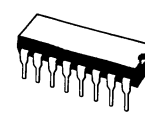
S-10043



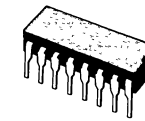
S-10044

3 TO 8 LINE DECODER (INVERTING)

- HIGH SPEED
  t_{PD} = 16 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA AT T_A = 25 °C
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS138



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HC138F1R M74HC138M1R
M74HC138B1R M74HC138C1R

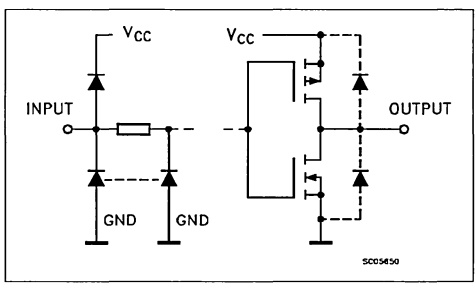
DESCRIPTION

The M54/74HC138 is a high speed CMOS 3 TO 8 LINE DECODER fabricated in silicon gate C^2MOS technology.

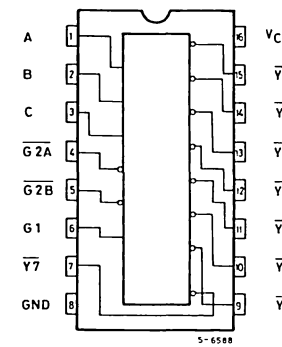
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. If the device is enabled, 3 binary select inputs (A, B and C) determine which one of the outputs will go low. If enable input G1 is held low or either $\overline{G2A}$ or $\overline{G2B}$ is held high, the decoding function is inhibited and all the 8 outputs go high.

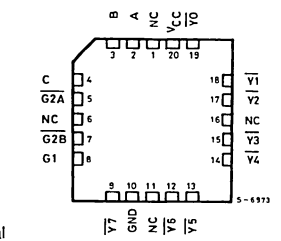
Three enable inputs are provided to ease cascade connection and application of address decoders for memory systems. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





NC =
No Internal
Connection

TRUTH TABLE

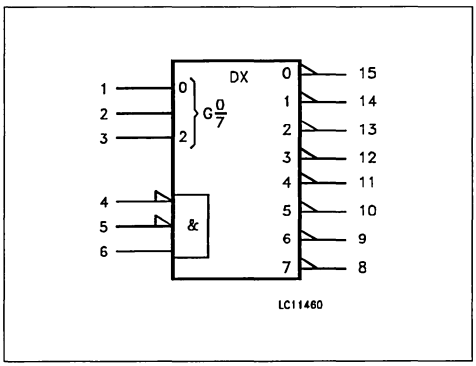
INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{G2B}$	$\overline{G2A}$	G1	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	L	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	X	X	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

X: Don't Care

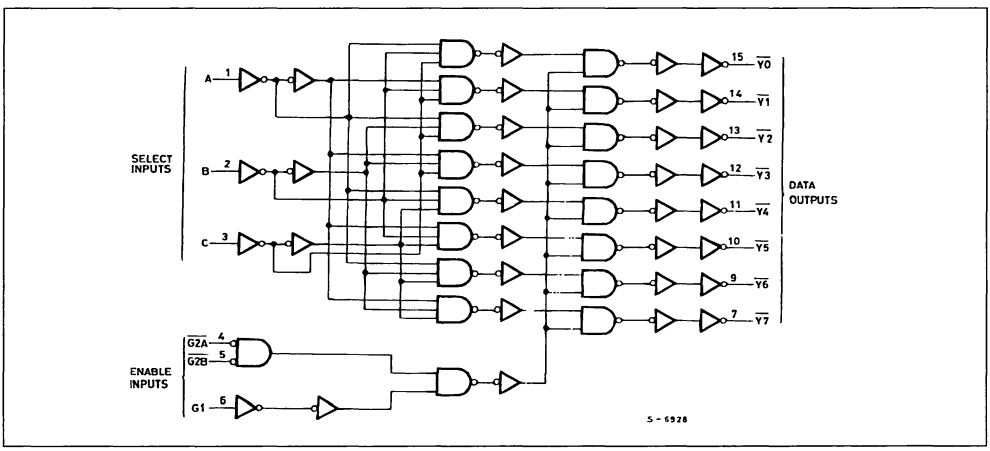
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3	A, B, C	Address Inputs
4, 5	$\overline{G2A}$, $\overline{G2B}$	Enable Inputs
6	G1	Enable Input
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y0}$ to $\overline{Y7}$	Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

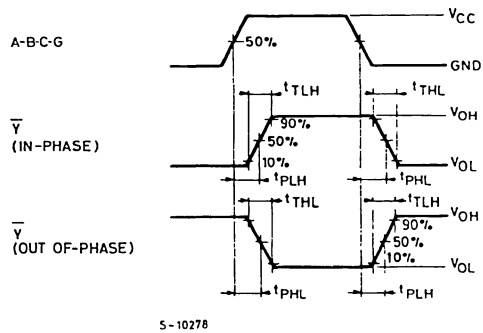
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

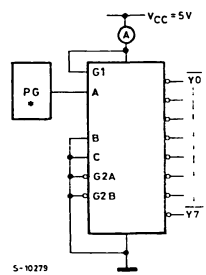
Symbol	Parameter	Test Conditions		Value						Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC	
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C - $\overline{Y}$)	2.0			60	125		155		190	ns
		4.5			15	25		31		38	
		6.0			13	21		26		32	
t_{PLH} t_{PHL}	Propagation Delay Time (G, $\overline{G}$ - $\overline{Y}$)	2.0			56	120		150		180	ns
		4.5			14	24		30		36	
		6.0			12	20		26		31	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				47						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



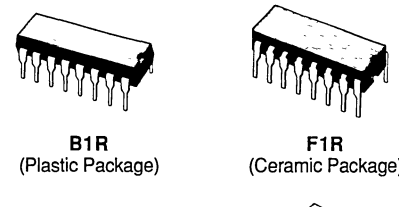
TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

3 TO 8 LINE DECODER (INVERTING)

- HIGH SPEED
  t_{PD} = 16 ns (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA AT T_A = 25 °C
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS138



B1R (Plastic Package)

F1R (Ceramic Package)

M1R (Micro Package)

C1R (Chip Carrier)

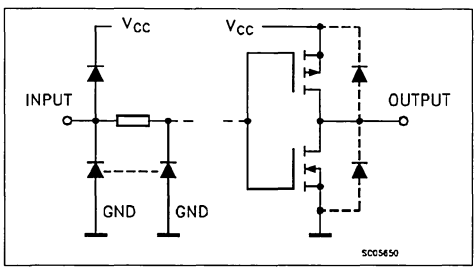
ORDER CODES :

M54HCT138F1R M74HCT138M1R
M74HCT138B1R M74HCT138C1R

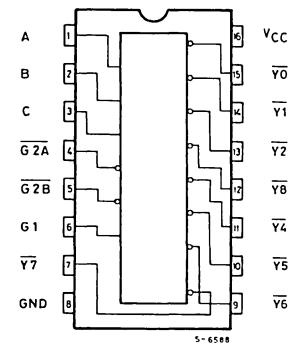
DESCRIPTION

The M54/74HC138 is a high speed CMOS 3 TO 8 LINE DECODER fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. If the device is enabled, 3 binary select inputs (A, B and C) determine which one of the outputs will go low. If enable input G1 is held low or either $\overline{G2A}$ or $\overline{G2B}$ is held high, the decoding function is inhibited and all the 8 outputs go high. Three enable inputs are provided to ease cascade connection and application of address decoders for memory systems. All inputs are equipped with protection circuits against static discharge and tran- sient excess voltage.This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



NC = No Internal Connection

TRUTH TABLE

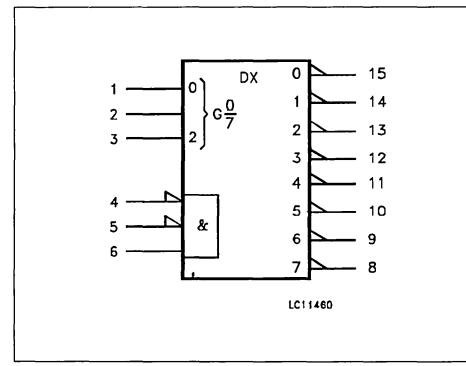
INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{G2B}$	$\overline{G2A}$	G1	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	L	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	X	X	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

X: Don't Care

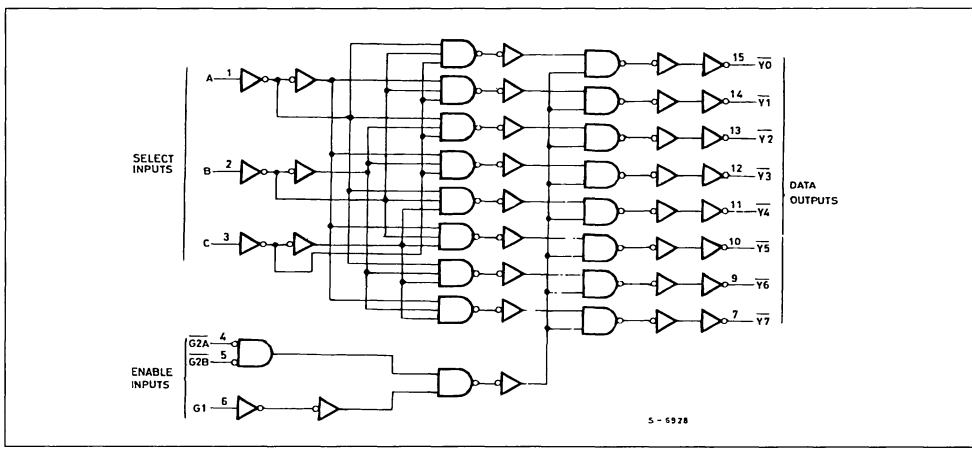
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3	A, B, C	Address Inputs
4, 5	$\overline{G2A}$, $\overline{G2B}$	Enable Inputs
6	G1	Enable Input
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y0}$ to $\overline{Y7}$	Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

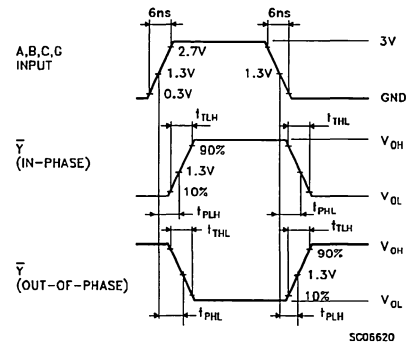
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				4		40		80	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND				2.0		2.9		3.0	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			8	15		19		22	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C - $\overline{Y}$)	4.5			17	30		38		45	ns
t_{PLH} t_{PHL}	Propagation Delay Time (G1 - $\overline{Y}$)	4.5			16	30		38		45	ns
t_{PLH} t_{PHL}	Propagation Delay Time (G2 - $\overline{Y}$)	4.5			19	30		38		45	ns
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				52						pF

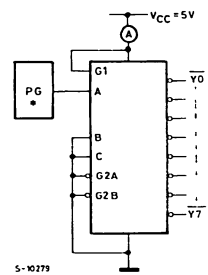
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



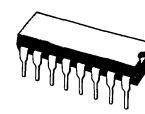
TEST CIRCUIT I_{CC} (Opr.)

INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

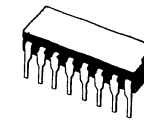


DUAL 2 TO 4 DECODER/DEMULTIPLEXER

- HIGH SPEED
  t_{PD} = 12 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS139



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

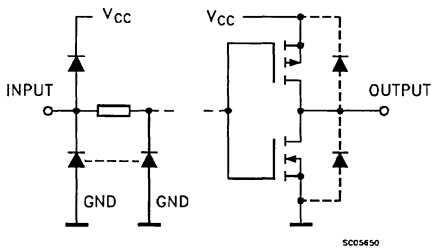
ORDER CODES :

M54HC139F1R M74HC139M1R
M74HC139B1R M74HC139C1R

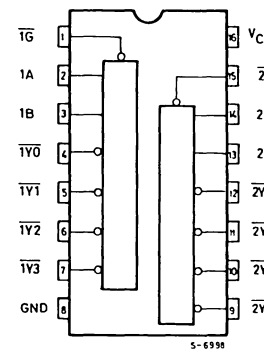
DESCRIPTION

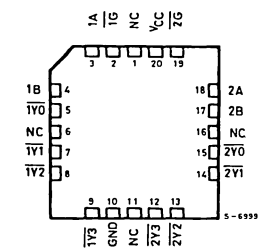
The M54/74HC139 is a high speed CMOS DUAL TWO LINE TO FOUR LINE DECODER/DEMULTIPLEXER fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The active low enable input can be used for gating or as a data input for demultiplexing applications. While the enable input is held high, all four outputs are high independently of the other inputs. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



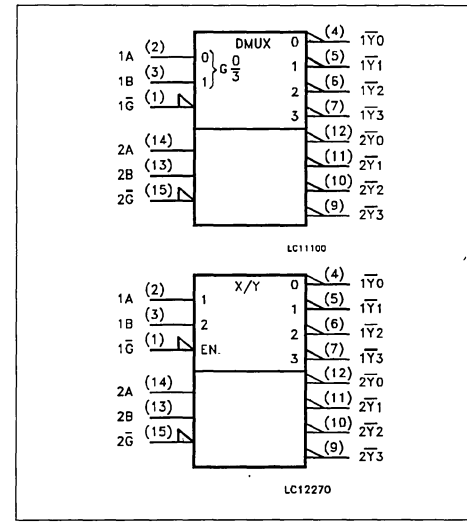


NC =
No Internal
Connection

TRUTH TABLE

INPUTS			OUTPUTS				SELECTED OUTPUT
ENABLE	SELECT						
$\overline{G}$	B	A	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	
H	X	X	H	H	H	H	NONE
L	L	L	L	H	H	H	$\overline{Y}_0$
L	L	H	H	L	H	H	$\overline{Y}_1$
L	H	L	H	H	L	H	$\overline{Y}_2$
L	H	H	H	H	H	L	$\overline{Y}_3$

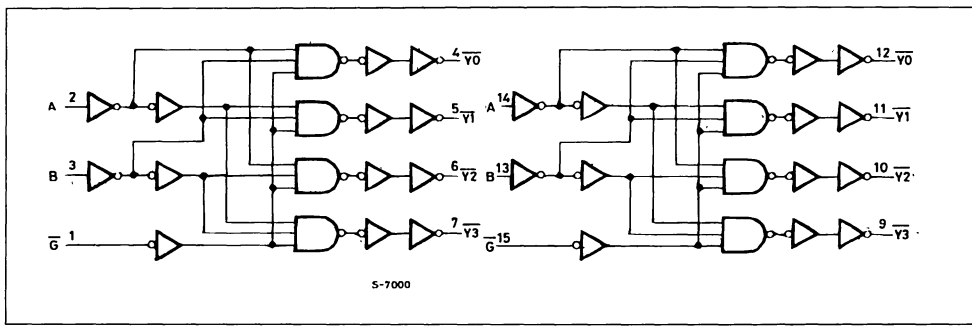
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{G}$, $2\overline{G}$	Enable Inputs
2, 3	1A, 1B	Address Inputs
4, 5, 6, 7	$1\overline{Y}_0$ to $1\overline{Y}_3$	Outputs
12, 11, 10, 9	$2\overline{Y}_0$ to $2\overline{Y}_3$	Outputs
14, 13	2A, 2B	Address Inputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

SCHEMATIC CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

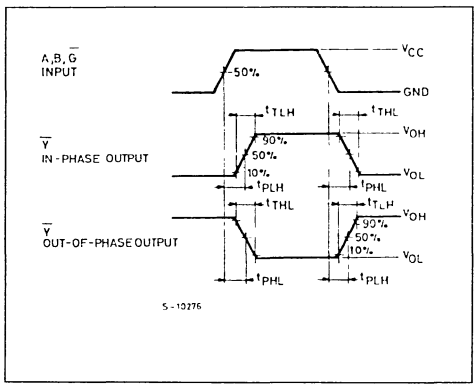
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

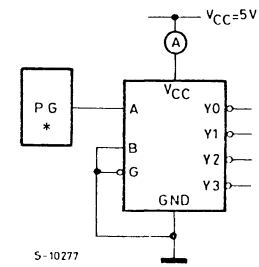
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (A, B - Y)	2.0			45	130		165		195	ns
		4.5			15	26		33		39	
		6.0			13	22		28		33	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{G}$ - Y)	2.0			39	110		140		165	ns
		4.5			13	22		28		33	
		6.0			11	19		24		28	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				46						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST CIRCUIT



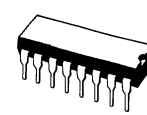
TEST CIRCUIT I_{CC} (Opr.)



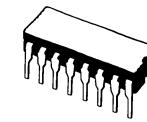
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

DUAL 2 TO 4 DECODER/DEMULTIPLEXER

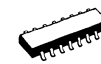
- HIGH SPEED
  t_{PD} = 17 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS139



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

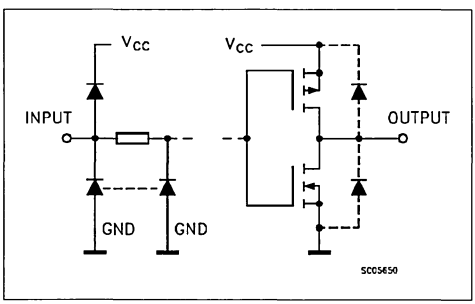
ORDER CODES :

M54HCT139F1R M74HCT139M1R
M74HCT139B1R M74HCT139C1R

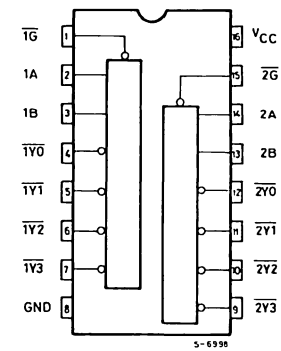
DESCRIPTION

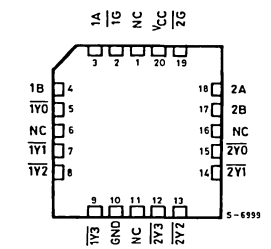
The M54/74HCT139 is a high speed CMOS DUAL TWO LINE TO FOUR LINE DECODER/DEMULTIPLEXER fabricated in silicon gate C2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The active low enable input can be used for gating or as a data input for demultiplexing applications. While the enable input is held high, all four outputs are high independently of the other inputs. All inputs are equipped with protection circuits against static discharge and transient excess volt-age. This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^{2}MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



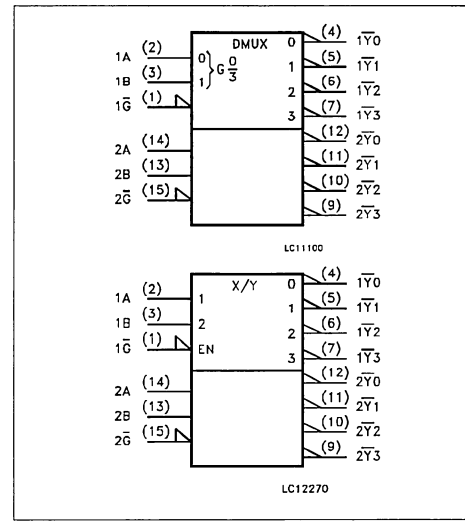


NC =
No Internal
Connection

TRUTH TABLE

INPUTS			OUTPUTS				SELECTED OUTPUT
ENABLE	SELECT						
$\overline{G}$	B	A	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	
H	X	X	H	H	H	H	NONE
L	L	L	L	H	H	H	$\overline{Y}_0$
L	L	H	H	L	H	H	$\overline{Y}_1$
L	H	L	H	H	L	H	$\overline{Y}_2$
L	H	H	H	H	H	L	$\overline{Y}_3$

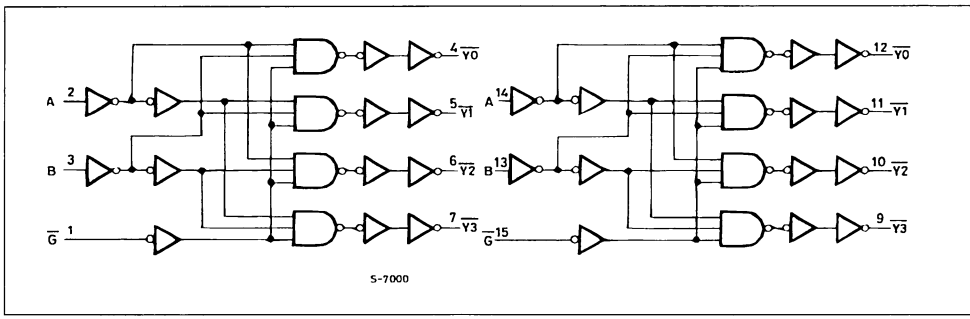
IEC LOGIC SYMBOLS



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{G}$, $2\overline{G}$	Enable Inputs
2, 3	1A, 1B	Address Inputs
4, 5, 6, 7	$1\overline{Y}_0$ to $1\overline{Y}_3$	Outputs
12, 11, 10, 9	$2\overline{Y}_0$ to $2\overline{Y}_3$	Outputs
14, 13	2A, 2B	Address Inputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

SCHEMATIC CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

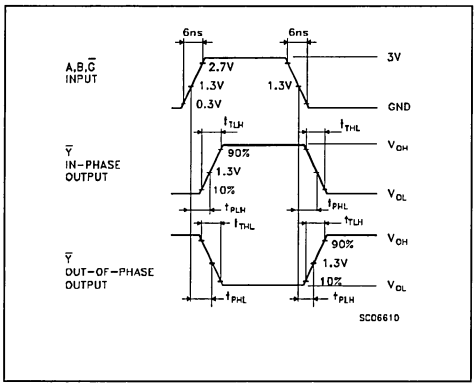
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				4		40		80	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9		3.0	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

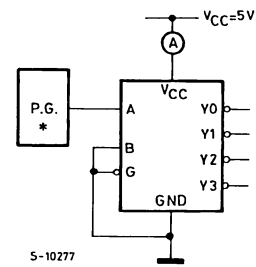
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			8	15		19		22	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A, B - Y)	4.5			19	30		38		45	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{G}$ - Y)	4.5			17	27		34		41	ns
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				40						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per decoder)

SWITCHING CHARACTERISTICS TEST CIRCUIT



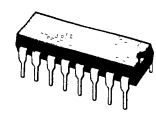
TEST CIRCUIT I_{CC} (Opr.)



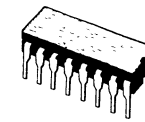
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

10 TO 4 LINE PRIORITY ENCODER

- HIGH SPEED
  t_{PD} = 15 ns (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V to 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS147



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

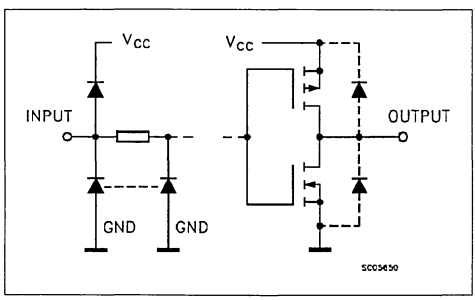
M54HC147F1R M74HC147M1R
M74HC147B1R M74HC147C1R

DESCRIPTION

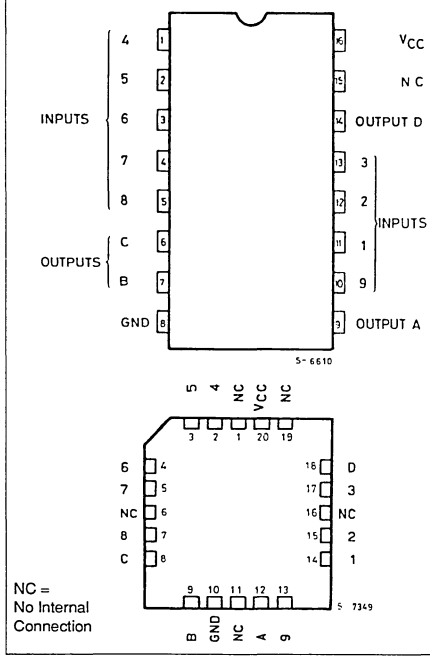
The M54/74HC147 is a high speed CMOS 10 TO 4 LINE PRIORITY ENCODER fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

This device features priority encoding of the inputs to ensure that only the highest order data line is encoded. Nine input lines are encoded to a four line BCD output. The implied decimal zero condition requires no input condition as zero is encoded when all nine data lines are at high logic level. All data input and outputs are active at the low logic level. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



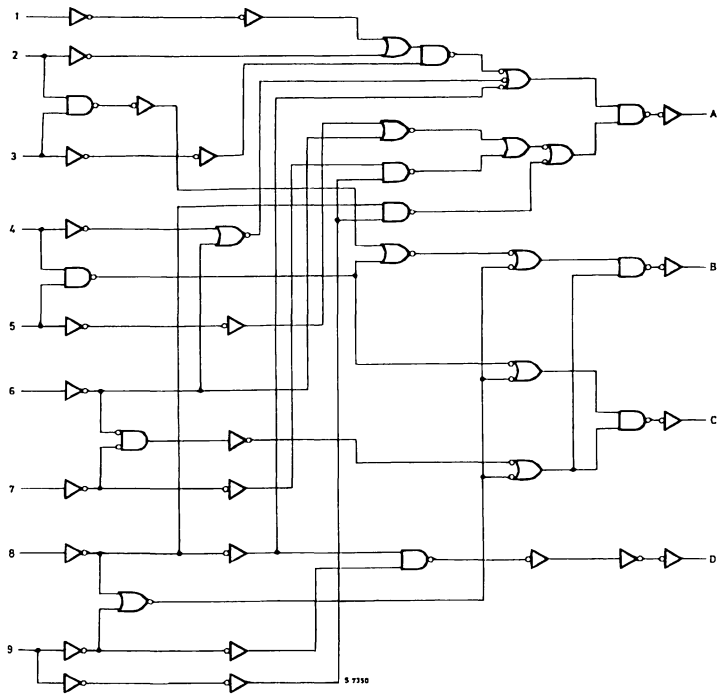
NC = No Internal Connection

TRUTH TABLE

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

X: Don't Care

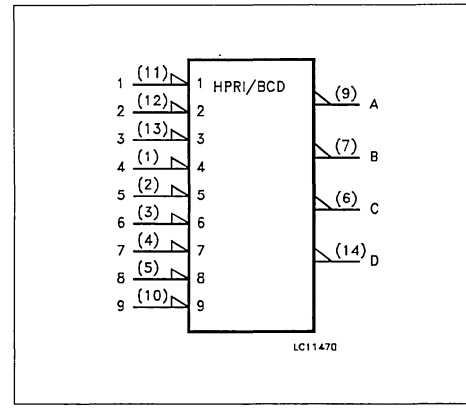
LOGIC DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
9, 7, 6, 14	A to D	BCD Address Outputs (Active LOW)
11, 12, 13, 1, 2, 3, 4, 5, 10	1 to 9	Decimal Data Inputs (Active LOW)
15	NC	Not Connected
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW. ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

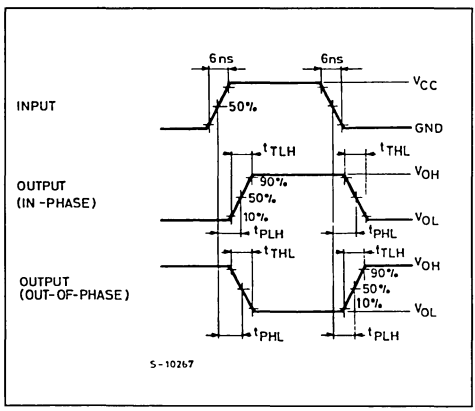
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

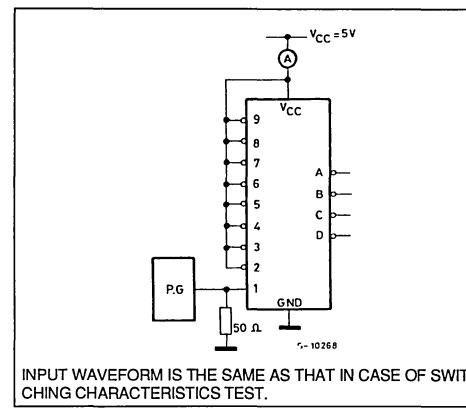
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			60	125		190		225	ns
		4.5			18	30		38		45	
		6.0			15	26		32		38	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				24						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST CIRCUIT



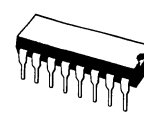
TEST CIRCUIT I_{CC} (Opr.)



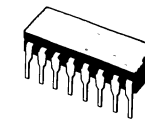
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

8 TO 3 LINE PRIORITY ENCODER

- HIGH SPEED
  t_{PD} = 15 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS148



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HC148F1R M74HC148M1R
M74HC148B1R M74HC148C1R

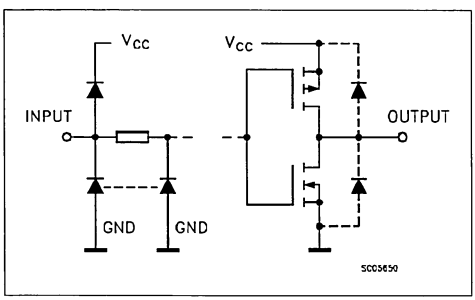
DESCRIPTION

The M54/74HC148 is a high speed CMOS 8-TO-3 LINE PRIORITY ENCODER fabricated in silicon gate C^2MOS technology.

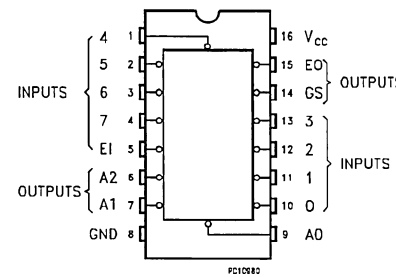
It has the same high speed performance for LSTTL combined with true CMOS low power consumption. The M54/74HC148 encodes eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion without the need for external circuitry. Data inputs are active at the low logic level.

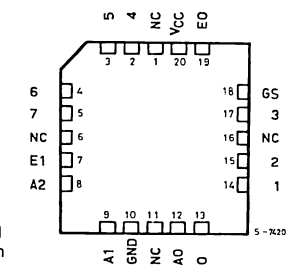
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





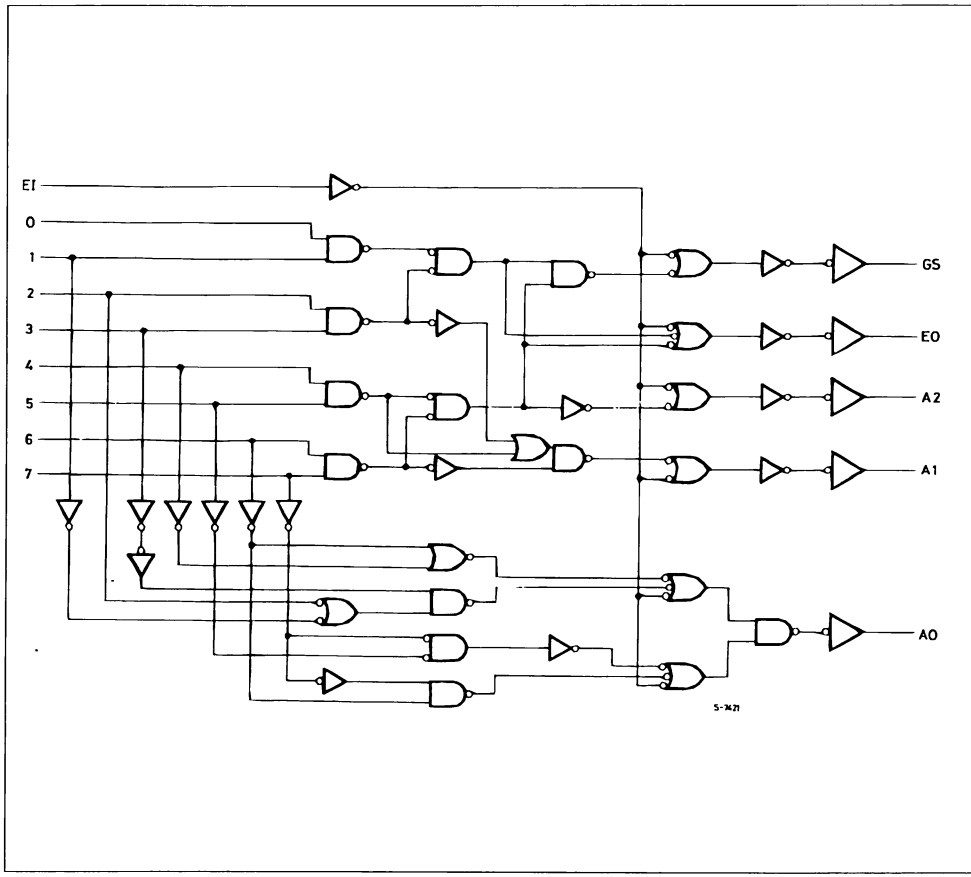
NC =
No Internal
Connection

TRUTH TABLE

INPUTS									OUTPUTS				
E1	0	1	2	3	4	5	6	7	A2	A1	A0	GS	E0
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	LL	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

X: Don't Care

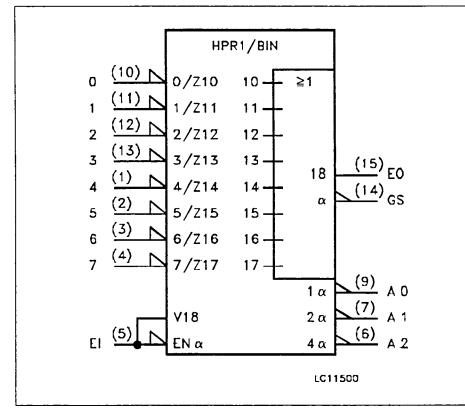
LOGIC DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
9, 7, 6	A0 to A2	Data Outputs
11, 12, 13, 1, 2, 3, 4, 10	0 to 7	Data Inputs
15	EO	Enable Output
5	EI	Enable Input
14	GS	Priority Flag Output
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C. 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

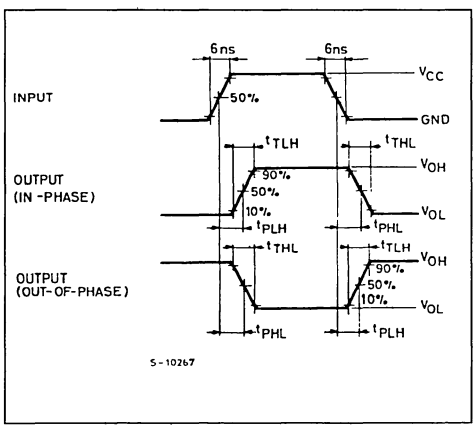
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

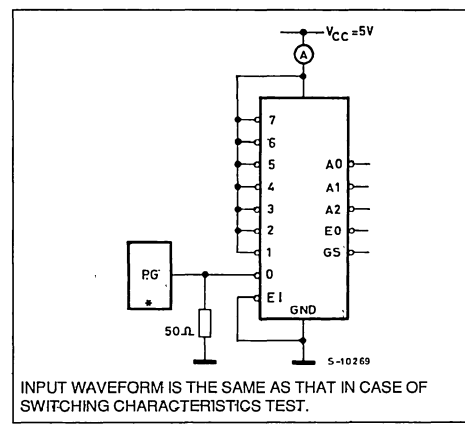
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (In - A0, A1, A2)	2.0			60	150		190		225	ns
		4.5			19	30		38		45	
		6.0			16	26		32		38	
t_{PLH} t_{PHL}	Propagation Delay Time (In - EO, GS)	2.0			60	150		190		225	ns
		4.5			19	30		38		45	
		6.0			16	26		32		38	
t_{PLH} t_{PHL}	Propagation Delay Time (EI - EO)	2.0			40	115		145		175	ns
		4.5			14	23		29		35	
		6.0			12	20		25		30	
t_{PLH} t_{PHL}	Propagation Delay Time (EI - GS)	2.0			40	115		145		175	ns
		4.5			14	23		29		35	
		6.0			12	20		25		30	
t_{PLH} t_{PHL}	Propagation Delay Time (EI - A0, A1, A2)	2.0			40	115		145		175	ns
		4.5			14	23		29		35	
		6.0			12	20		25		30	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				60						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST CIRCUIT



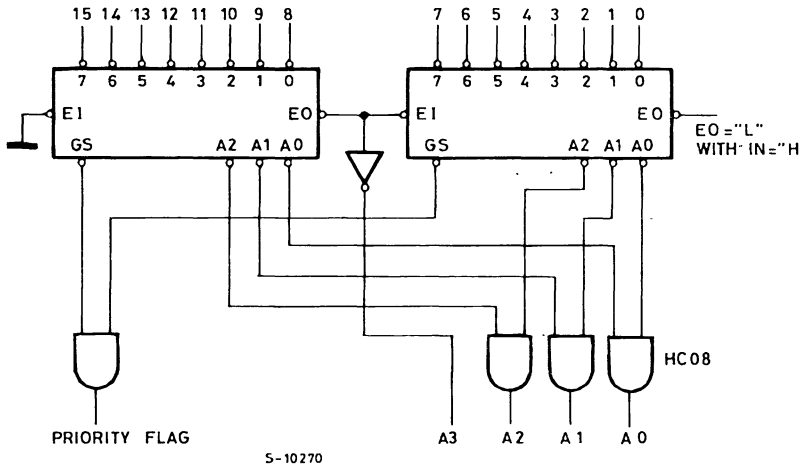
TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

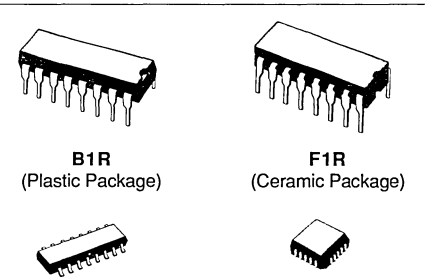
TYPICAL APPLICATION

4-BIT CASCADE CONNECTION



8 CHANNEL MULTIPLEXER

- HIGH SPEED
  t_{PD} = 15 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS151



B1R
(Plastic Package)

F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

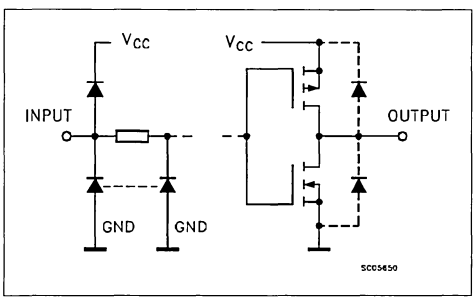
ORDER CODES :

M54HC151F1R M74HC151M1R
M74HC151B1R M74HC151C1R

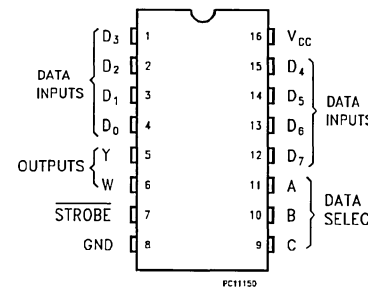
DESCRIPTION

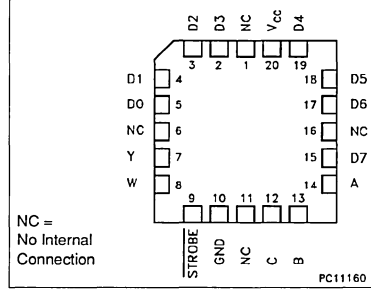
The M54/74HC151 is a high speed CMOS 8 CHANNEL MULTIPLEXER fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. It provides, in one package, the ability to select one bit of data from up to eight sources. The HC151 can be used as a universal function generator to generate any logic function of four variables. Outputs Y and W are complementary selection depends on the address inputs A, B and C. The strobe input must be taken low to enable this device, when the strobe is high W output is forced high and consequently Y output goes low. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





NC = No Internal Connection

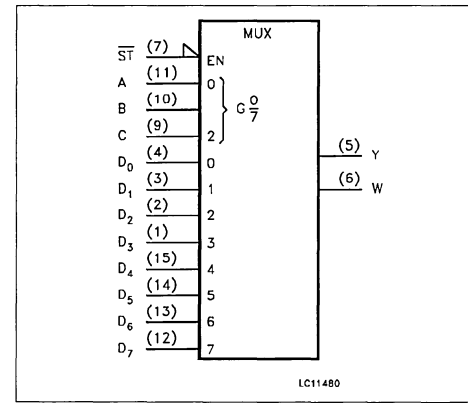
TRUTH TABLE

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	$\overline{S}$		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

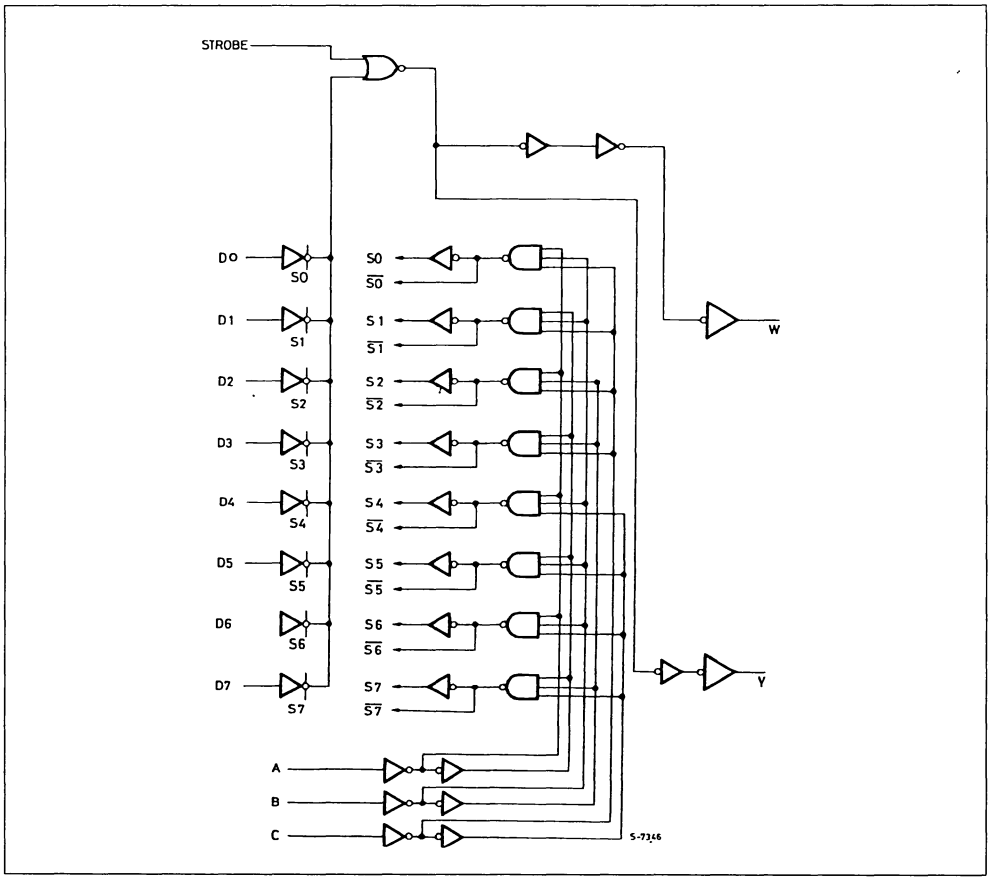
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
4, 3, 2, 1, 15, 14, 13, 12	D0 to D7	Multiplexer Inputs
5	y	Multiplexer Output
6	w	Complementary Multiplexer Output
7	$\overline{\text{STROBE}}$	Strobe Input
11, 10, 9	A, B, C	Select Inputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

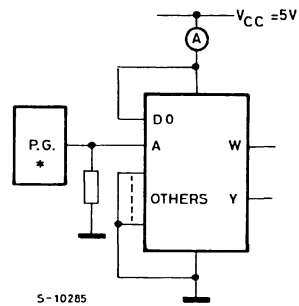
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to,85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (D - W)	2.0			56	130		165		190	ns
		4.5			16	26		33		38	
		6.0			14	22		28		32	
t_{PLH} t_{PHL}	Propagation Delay Time (D - Y)	2.0			56	130		165		190	ns
		4.5			16	26		33		38	
		6.0			14	22		28		32	
t_{PLH} t_{PHL}	Propagation Delay Time (STROBE - W)	2.0			30	85		105		125	ns
		4.5			10	17		21		25	
		6.0			9	14		18		21	
t_{PLH} t_{PHL}	Propagation Delay Time (STROBE - Y)	2.0			30	85		105		125	ns
		4.5			10	17		21		25	
		6.0			9	14		18		21	
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C - W)	2.0			72	160		200		235	ns
		4.5			20	32		40		47	
		6.0			17	27		34		40	
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C - Y)	2.0			72	160		200		235	ns
		4.5			20	32		40		47	
		6.0			17	27		34		40	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				63						pF

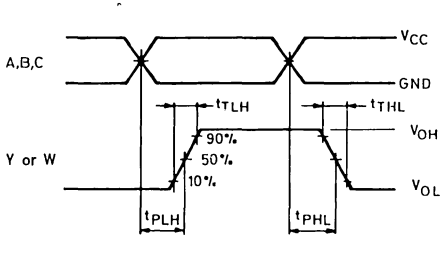
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit) Average operting current can be obtained by the following equation $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

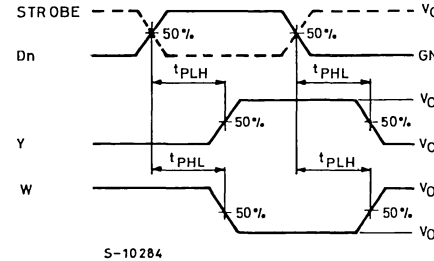
TEST CIRCUIT I_{CC} (Opr.)



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

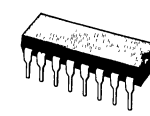
SWITCHING CHARACTERISTICS TEST WAVEFORM



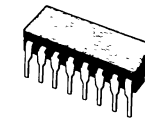


HC153 DUAL 4 CHANNEL MULTIPLEXER
HC253 DUAL 4 CHANNEL MULTIPLEXER 3 STATE OUTPUT

- HIGH SPEED
  t_{PD} = 12 ns (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V to 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS153/253



B1R
(Plastic Package)



F1R
(Ceramic Package)

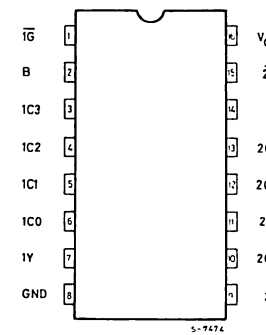
M1R
(Micro Package)

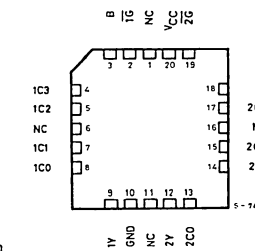
C1R
(Chip Carrier)

ORDER CODES :

M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

PIN CONNECTIONS (top view)





NC =
No Internal
Connection

DESCRIPTION

The M54/74HC153 and M54/74HC253 are high speed CMOS DUAL 4-CHANNEL MULTIPLEXERS fabricated with silicon gate C^2MOS technology. Both achieve high speed operation, similar to equivalent LSTTL, while maintaining the CMOS low power dissipation.

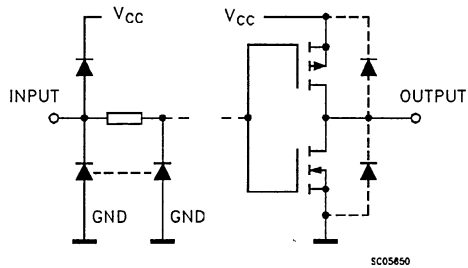
The designer has a choice of complementary output (HC153) and 3-state output (HC253).

Each of these data (1C0-1C3, 2C0-2C3) is selected by the two address inputs A and B.

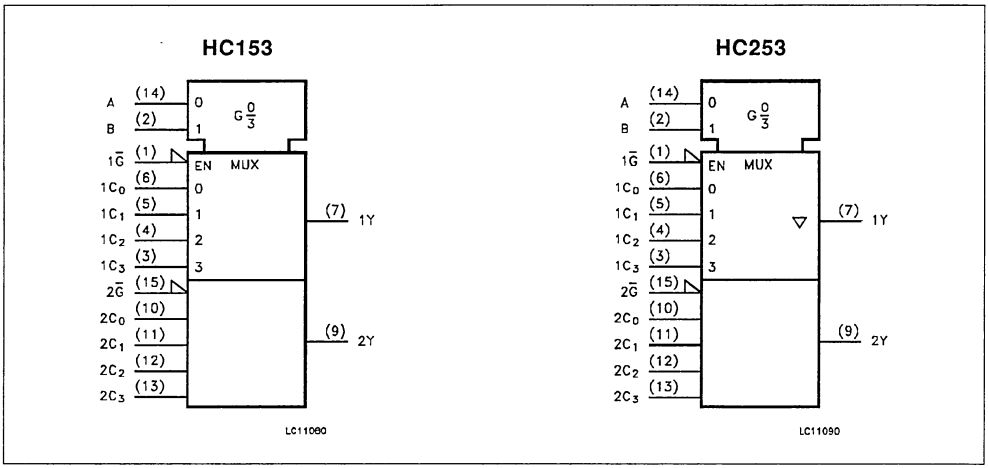
Separate strobe inputs ($1\overline{G}$, $2\overline{G}$) are provided for each of the two four-line sections. The strobe input ($\overline{G}$) can be used to inhibit the data output ; the output of HC 153 is fixed at a low level and the output of HC253 is a high impedance, while the strobe input is held low.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



IEC LOGIC SYMBOLS



PIN DESCRIPTION (for HC153)

PIN No	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{G}$, $2\overline{G}$	Output Enable Inputs
14, 2	A, B	Common Data Select Inputs
6, 5, 4, 3	1C0 to 1C3	Data Inputs From Source 1
7	1Y	Multiplexer Output From Source 1
9	2Y	Multiplexer Output From Source 2
10, 11, 12, 13	2C0 to 2C3	Data Inputs From Source 2
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

PIN DESCRIPTION (for HC253)

PIN No	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{G}$, $2\overline{G}$	Output Enable Inputs
14, 2	A, B	Common Data Select Inputs
6, 5, 4, 3	1C0 to 1C3	Data Inputs From Source 1
7, 9	1Y, 2Y	3 State Multiplexer Outputs
10, 11, 12, 13	2C0 to 2C3	Data Inputs From Source 2
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

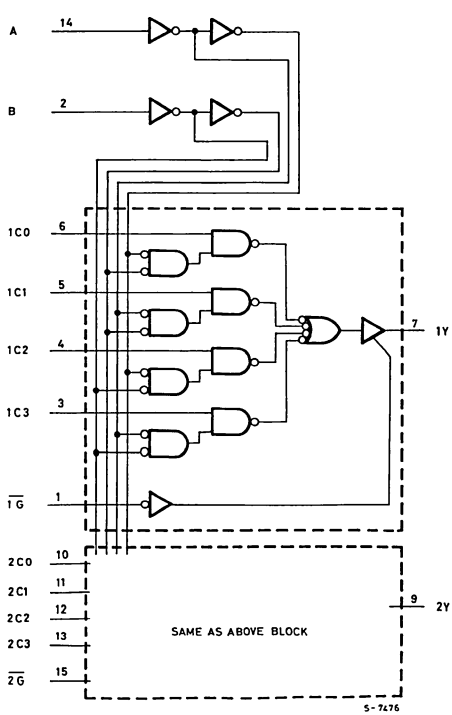
TRUTH TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT Y	
B	A	C_0	C_1	C_2	C_3	$\overline{G}$	HC153	HC253
X	X	X	X	X	X	H	L	Z
L	L	L	X	X	X	L	L	L
L	L	H	X	X	X	L	H	H
L	H	X	L	X	X	L	L	L
L	H	X	H	X	X	L	H	H
H	L	X	X	L	X	L	L	L
H	L	X	X	H	X	L	H	H
H	H	X	X	X	L	L	L	L
H	H	X	X	X	H	L	H	H

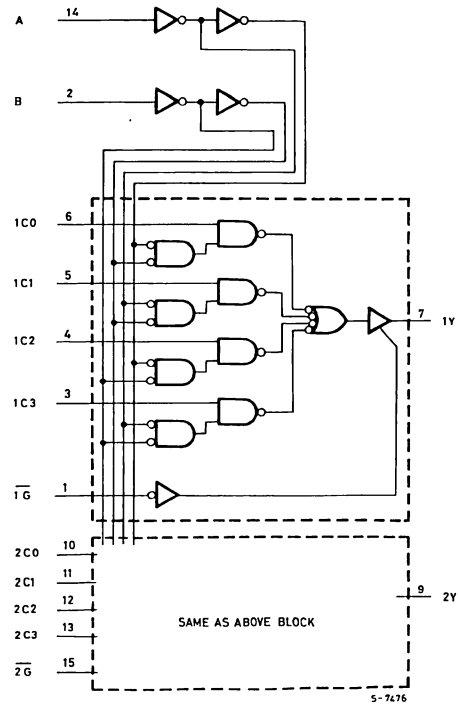
X: DON'T CARE - Z: HIGH IMPEDANCE

LOGIC DIAGRAM

HC153



HC253



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ} (1)	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	mA

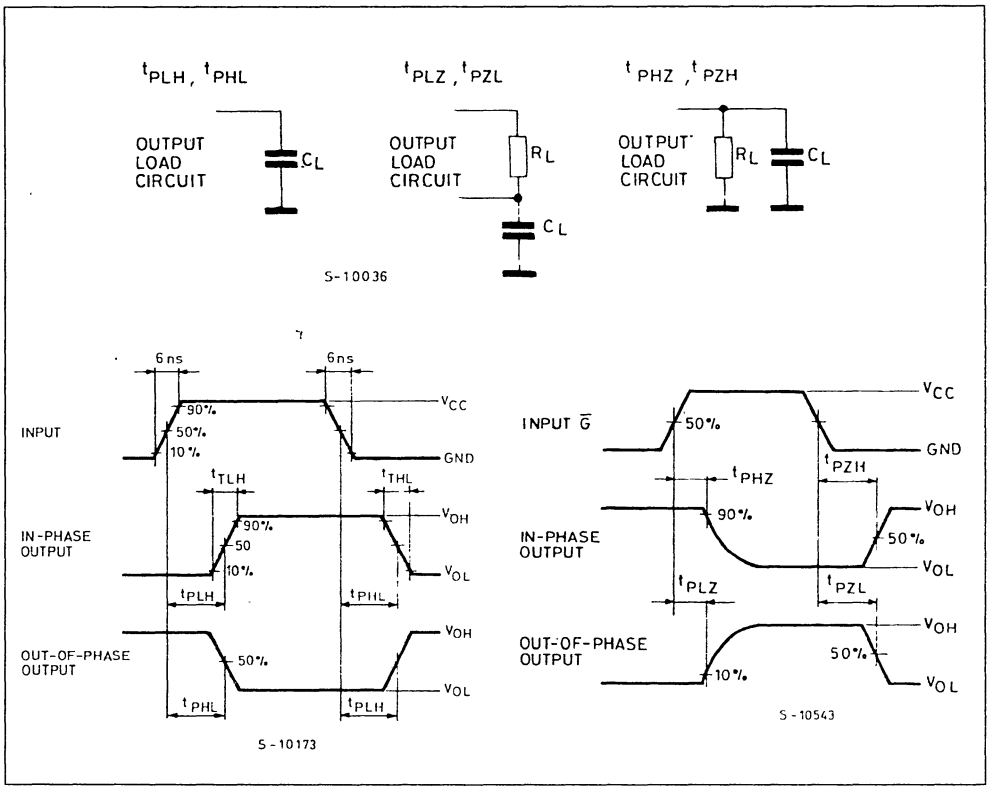
Note: 1. Applied only for M54/M74HC253

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

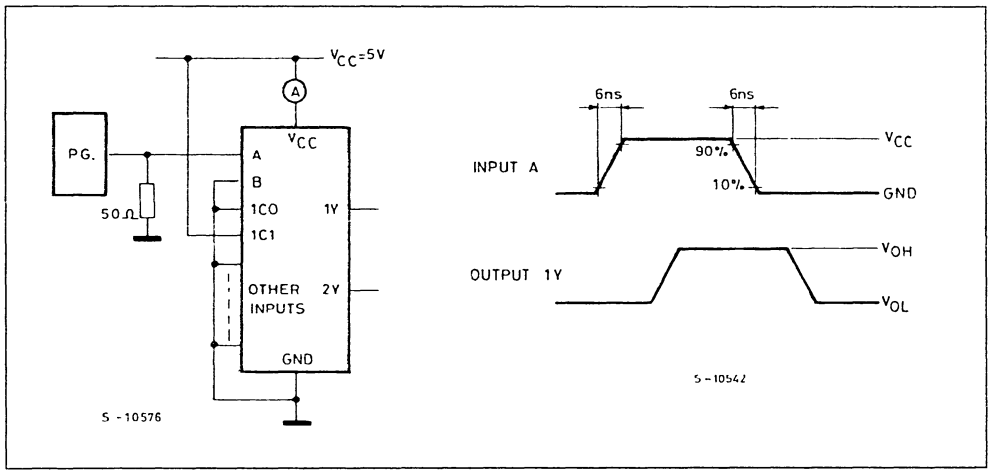
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (Cn - Y)	2.0			48	115		145		175	ns
		4.5			15	23		29		35	
		6.0			12	20		25		30	
t_{PLH} t_{PHL}	Propagation Delay Time (A, B - Y)	2.0			68	150		190		225	ns
		4.5			20	30		38		45	
		6.0			16	26		32		38	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{G}$ - Y)	2.0			30	85		105		130	ns
		4.5			10	17		21		26	
		6.0			9	14		18		22	
t_{PZL} t_{PZH}	Propagation Delay Time (for HC253) ($\overline{G}$ - Y)	2.0	R_L = 1KΩ		36	100		125		150	ns
		4.5			12	20		25		30	
		6.0			9	17		21		26	
t_{PLZ} t_{PHZ}	Propagation Delay Time (for HC253) ($\overline{G}$ - Y)	2.0	R_L = 1KΩ		22	100		125		150	ns
		4.5			11	20		25		30	
		6.0			9	17		21		26	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				58						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per circuit)

SWITCHING CHARACTERISTICS TEST WAVEFORM

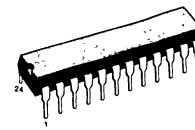


TEST CIRCUIT Icc (Opr.)

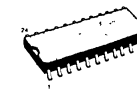


4 TO 16 LINE DECODER/DEMULTIPLEXER

- HIGH SPEED
- t_{PD} = 15 ns (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V to 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS154



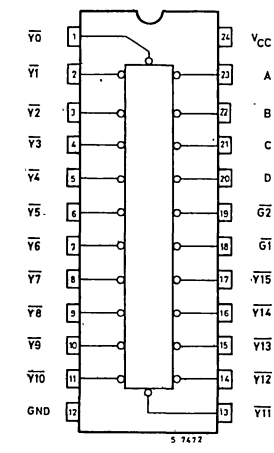
B1R
(Plastic Package)



M1R
(Micro Package)

ORDER CODES :
M74HC154B1R M74HC154M1R

PIN CONNECTIONS (top view)



NC = No Internal Connection

DESCRIPTION

The 74HC154 is a high speed CMOS 4 TO 16-LINE DECODER/DEMULTIPLEXER fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

A binary code applied to the four inputs (A to D) provides a low level at the selected one of sixteen outputs excluding the other fifteen outputs, when both the strobe inputs, $\overline{G1}$ and $\overline{G2}$, are held low. When either strobe input is held high, the decording function is inhibited to keep all outputs high. The strobe function makes it easy to expand the decoding lines through cascading, and simplifies the design of address decoding circuits in memory control systems.

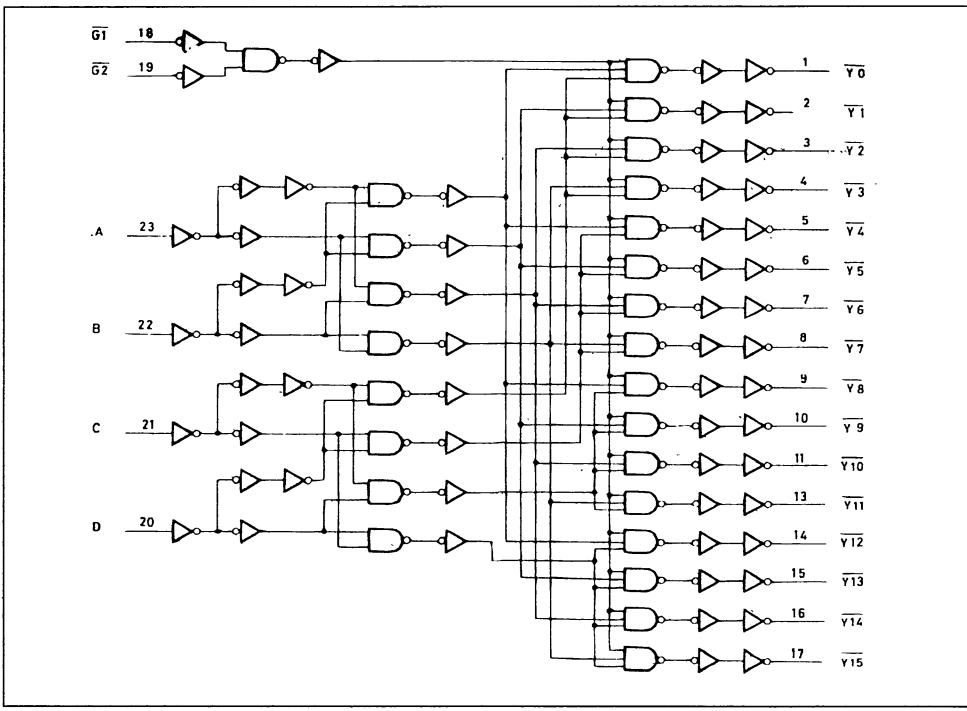
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

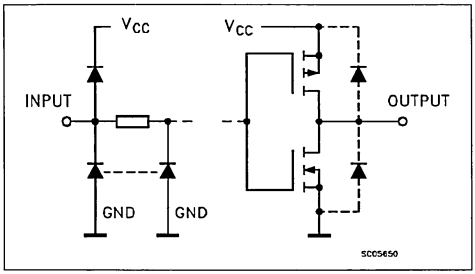
INPUTS						SELECTED OUTPUT (L)
$\overline{G1}$	$\overline{G2}$	D	C	B	A	
L	L	L	L	L	L	$\overline{Y0}$
L	L	L	L	L	H	$\overline{Y1}$
L	L	L	L	H	L	$\overline{Y2}$
L	L	L	L	H	H	$\overline{Y3}$
L	L	L	H	L	L	$\overline{Y4}$
L	L	L	H	L	H	$\overline{Y5}$
L	L	L	H	H	L	$\overline{Y6}$
L	L	L	H	H	H	$\overline{Y7}$
L	L	H	L	L	L	$\overline{Y8}$
L	L	H	L	L	H	$\overline{Y9}$
L	L	H	L	H	L	$\overline{Y10}$
L	L	H	L	H	H	$\overline{Y11}$
L	L	H	H	L	L	$\overline{Y12}$
L	L	H	H	L	H	$\overline{Y13}$
L	L	H	H	H	L	$\overline{Y14}$
L	L	H	H	H	H	$\overline{Y15}$
X	H	X	X	X	X	NONE
H	X	X	X	X	X	NONE

X: Don't Care

LOGIC DIAGRAM



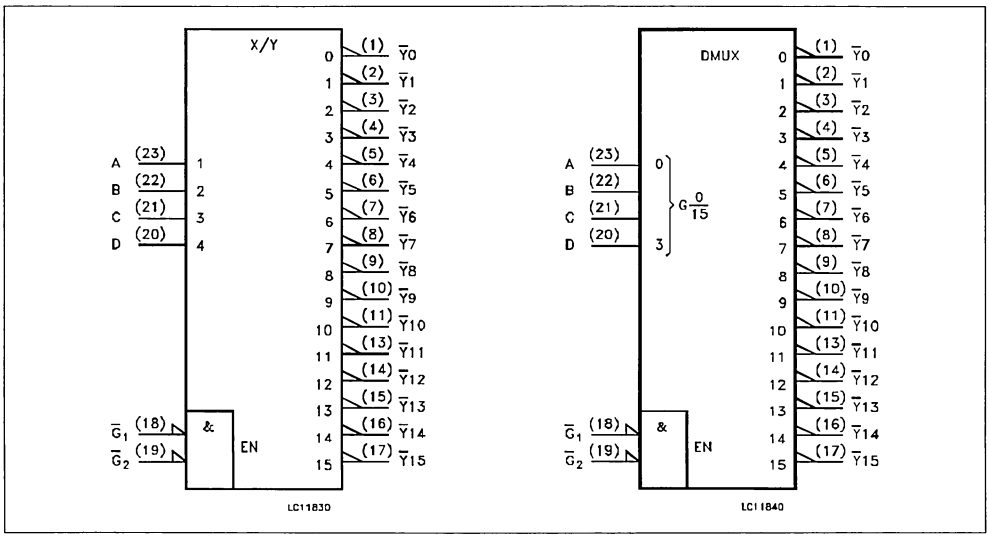
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 13, 14, 15, 16, 17	$\overline{Y0}$ to $\overline{Y15}$	Outputs (Active LOW)
18, 19	$\overline{G1}$, $\overline{G2}$	Enable Inputs (Active LOW)
23, 22, 21, 20	A to D	Address Inputs
12	GND	Ground (0V)
24	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature:		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

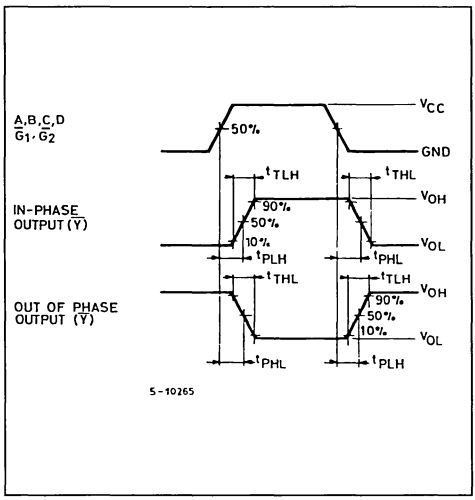
Symbol	Parameter	Test Conditions			Value					Unit
		V_{CC} (V)			T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		V
		4.5			3.15			3.15		
		6.0			4.2			4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5	V
		4.5					1.35		1.35	
		6.0					1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 μA	1.9	2.0		1.9		V
		4.5			4.4	4.5		4.4		
		6.0			5.9	6.0		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 μA		0.0	0.1		0.1	V
		4.5				0.0	0.1		0.1	
		6.0				0.0	0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40	μA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

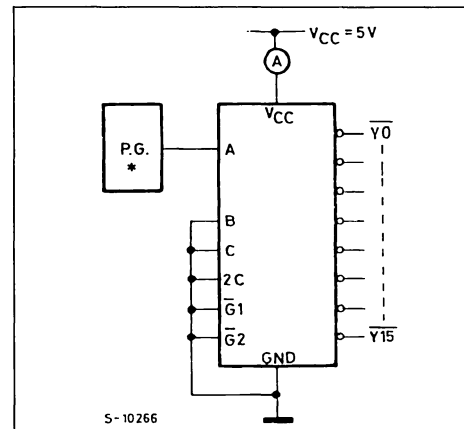
Symbol	Parameter	Test Conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C, D - $\overline{Y}$)	2.0			65	175		220	ns
		4.5			19	35		44	
		6.0			16	30		37	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{G1}$, $\overline{G2}$ - Y)	2.0			55	160		200	ns
		4.5			17	32		40	
		6.0			15	27		34	
C_{IN}	Input Capacitance				5	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				57				pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST CIRCUIT



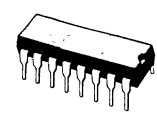
TEST CIRCUIT I_{CC} (Opr.)



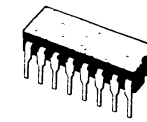
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

DUAL 2 TO 4 LINE DECODER 3 TO 8 LINE DECODER

- HIGH SPEED
  t_{PD} = 12 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS155



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HC155F1R M74HC155M1R
M74HC155B1R M74HC155C1R

DESCRIPTION

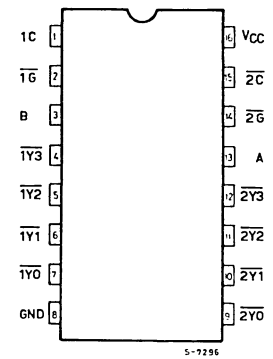
The M54/74HC155 is a high speed CMOS DUAL 2-TO-4 LINE DECODER fabricated in silicon gate C^2MOS technology.

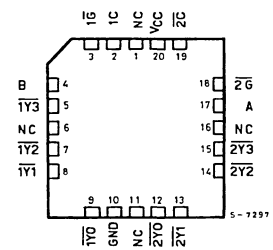
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. It features dual 1-TO-4 line demultiplexers with individual strobe inputs (1G and 2G), individual data inputs (1C and $\overline{2C}$) and common binary address inputs (A and B).

When both decoders are enabled by the strobes, the inverted output of 1C data and non-inverted output of $\overline{2C}$ data will be brought to the select output pins of each sections. A 1-TO-8 line demultiplexer can also be easily built up by providing a data signal to both 1C and $\overline{2C}$ inputs ; the output order from the msb is 1Y3, 1Y2, 1Y1, 1Y0, 2Y3, 2Y2, 2Y1, 2Y0. This device can be used as a 2-to-4 line decoder or a 3-to-8 line decoder when 1C is held high and $\overline{2C}$ is held low.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

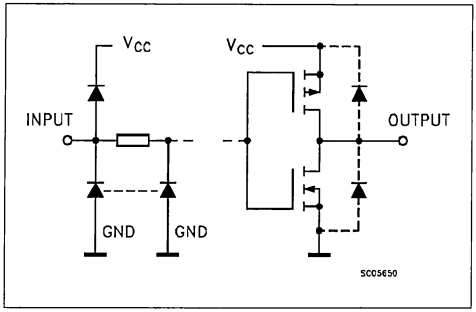
PIN CONNECTIONS (top view)



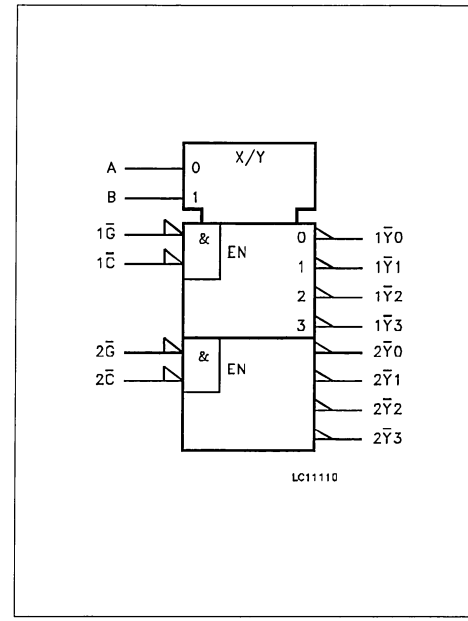


NC =
No Internal
Connection

INPUT AND OUTPUT EQUIVALENT CIRCUIT



IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 15	1C, 2C	Data Inputs
2, 14	1G, 2G	Strobe Inputs
3, 13	B, A	Common Data Inputs
7, 6, 5, 4	1Y0 to 1Y3	Outputs
9, 10, 11, 12	2Y0 to 2Y3	Outputs
8	GND	Ground (0V)
16	VCC	Positive Supply Voltage

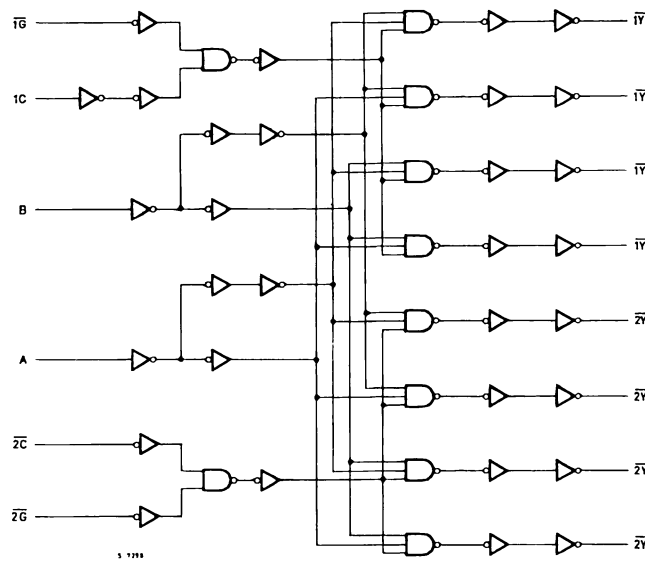
TRUTH TABLE

INPUTS				OUTPUTS			
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

TRUTH TABLE

INPUTS				OUTPUTS			
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

LOGIC CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

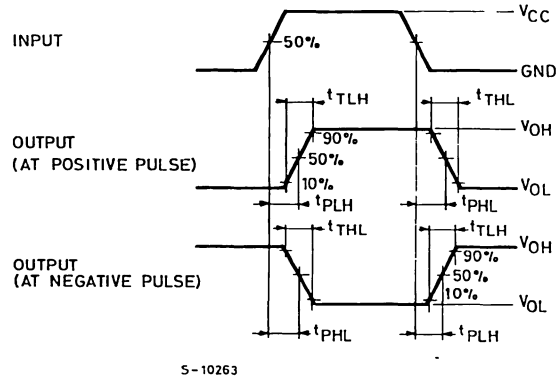
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

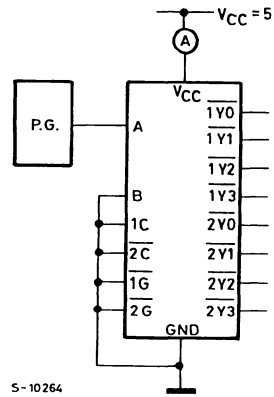
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			45	130		165		195	ns
		4.5			15	26		33		39	
		6.0			13	22		28		33	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				53						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST WAVEFORM I_{CC} (Opr.)



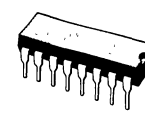
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

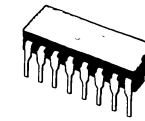
M54HC157/158
M74HC157/158

HC157 QUAD 2 CHANNEL MULTIPLEXER
HC158 QUAD 2 CHANNEL MULTIPLEXER (INV.)

- HIGH SPEED
  t_{PD} = 10 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS157/158



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

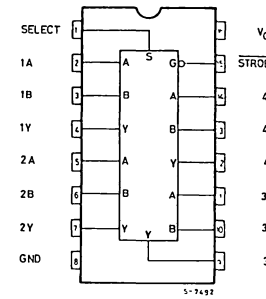
C1R
(Chip Carrier)

ORDER CODES :

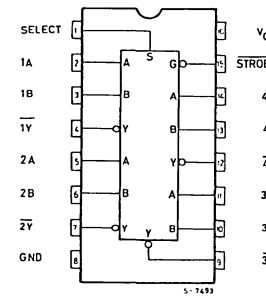
M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

PIN CONNECTIONS (top view)

HC157



HC158



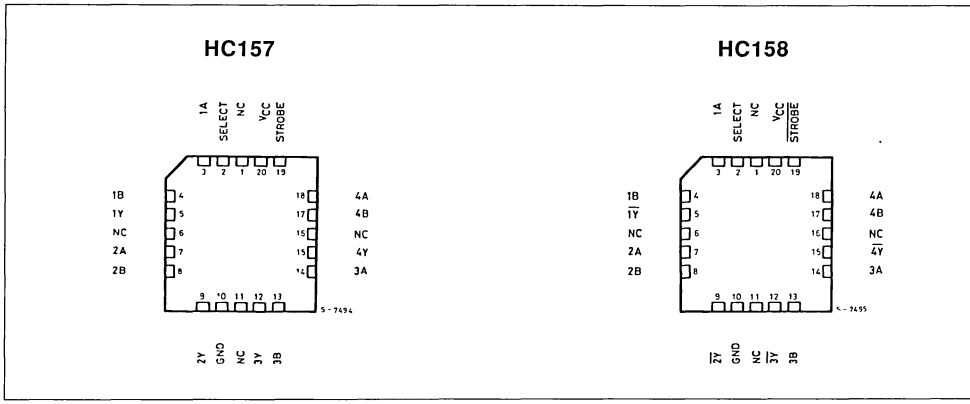
NC =
No Internal
Connection

DESCRIPTION

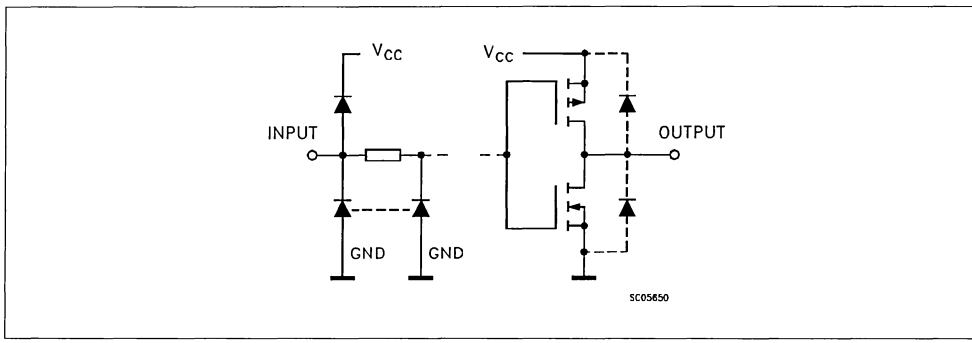
The M54/74HC157 and the M54/74HC158 are high speed CMOS QUAD 2-CHANNEL MULTIPLEXER's fabricated with silicon gate C^2MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These devices consist of four 2-input digital multiplexers with common select and strobe inputs. The HC158 is an inverting multiplexer while the HC157 is a non-inverting multiplexer. When the $\overline{\text{STROBE}}$ input is held High, selection of data is inhibited and all the outputs become Low in the M74HC157 and High in the M74HC158. The SELECT decoding determines whether the A or B inputs get routed to their corresponding Y outputs. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

CHIP CARRIER



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION (for HC157)

PIN No	SYMBOL	NAME AND FUNCTION
1	SELECT	Common Data Select Input
2, 5, 11, 14	1A to 4A	Data Inputs From Source A
3, 6, 10, 13	1B to 4B	Data Inputs From Source B
4, 7, 9, 12	1Y to 4Y	Multiplexer Output
15	$\overline{\text{STROBE}}$	Strobe Input
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

PIN DESCRIPTION (for HC158)

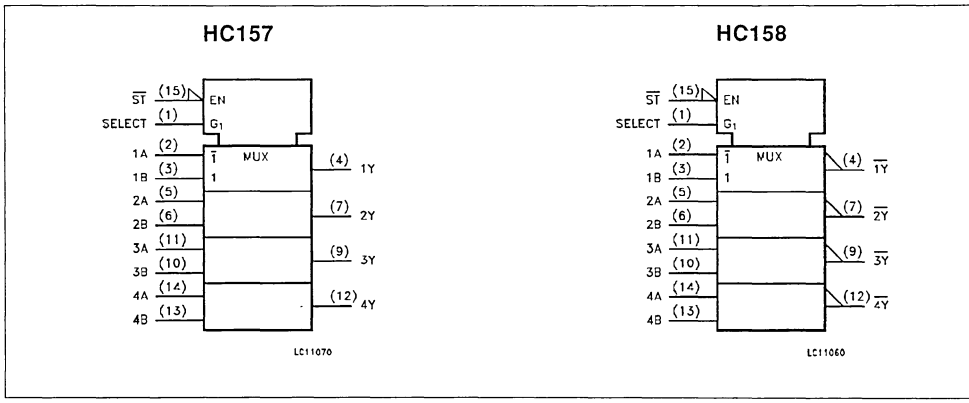
PIN No	SYMBOL	NAME AND FUNCTION
1	SELECT	Common Data Select Input
2, 5, 11, 14	1A to 4A	Data Inputs From Source A
3, 6, 10, 13	1B to 4B	Data Inputs From Source B
4, 7, 9, 12	$\overline{1Y}$ to $\overline{4Y}$	Multiplexer Output
15	$\overline{\text{STROBE}}$	Strobe Input
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

TRUTH TABLE

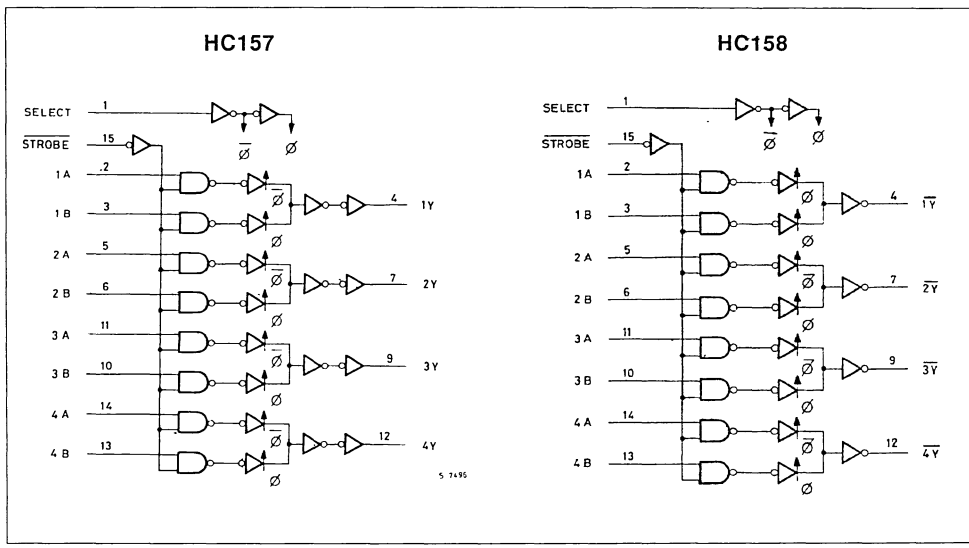
INPUTS				OUTPUTS	
$\overline{STROBE}$	SELECT	A	B	Y (HC157)	$\overline{Y}$ (HC158)
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

X: DON'T CARE

IEC LOGIC SYMBOL



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied

(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C· 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series·		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I *	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND I_O =0				4		40		80	µA

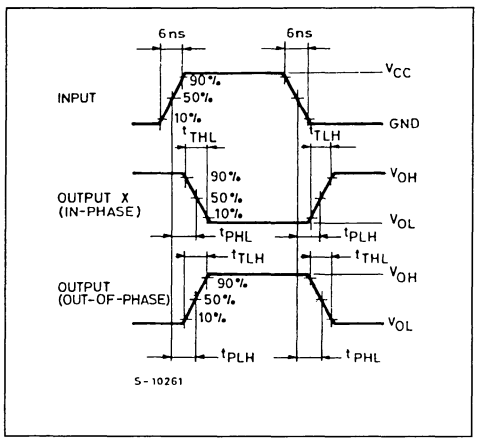
* Applicable only to DIR, G, $\overline{G}$ input

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

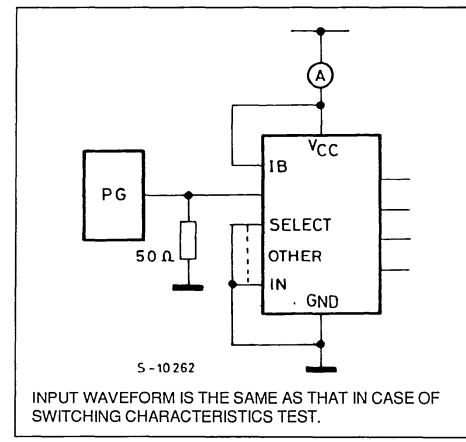
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (A, B - Y)	2.0			30	100		125		150	ns
		4.5			12	20		25		30	
		6.0			10	17		21		26	
t_{PLH} t_{PHL}	Propagation Delay Time (SELECT - Y)	2.0			50	125		155		190	ns
		4.5			16	25		31		38	
		6.0			14	21		26		32	
t_{PLH} t_{PHL}	Propagation Delay Time (STROBE - Y)	2.0			36	115		145		175	ns
		4.5			12	23		29		35	
		6.0			10	20		25		30	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				47						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit) Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per channel)

SWITCHING CHARACTERISTICS TEST CIRCUIT



TEST CIRCUIT I_{CC} (Opr.)



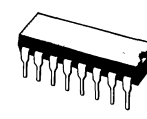
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

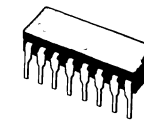
M54HCT157/158
M74HCT157/158

HCT157 QUAD 2 CHANNEL MULTIPLEXER
HCT158 QUAD 2 CHANNEL MULTIPLEXER (INV.)

- HIGH SPEED
  t_{PD} = 21 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS157/158



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

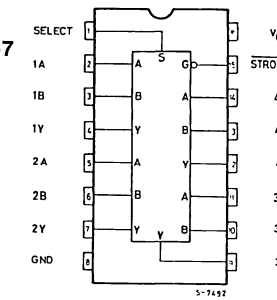
C1R
(Chip Carrier)

ORDER CODES :

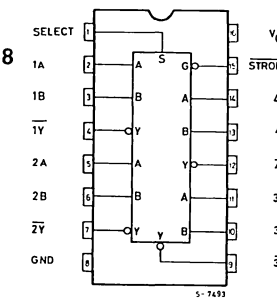
M54HCTXXXF1R M74HCTXXXM1R
M74HCTXXXB1R M74HCTXXXC1R

PIN CONNECTIONS (top view)

HCT157



HCT158



NC =
No Internal
Connection

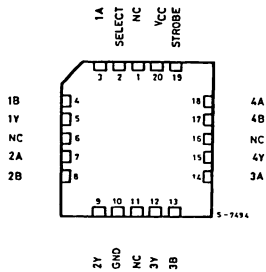
DESCRIPTION

The M54/74HCT157 and the M54/74HCT158 are high speed CMOS QUAD 2-CHANNEL MULTIPLEXERs fabricated with silicon gate C^2MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

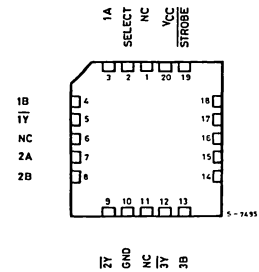
These devices consist of four 2-input digital multiplexers with common select and strobe inputs. The HCT158 is an inverting multiplexer while the HCT157 is a non-inverting multiplexer. When the $\overline{\text{STROBE}}$ input is held High, selection of data is inhibited and all the outputs become Low in the M74HCT157 and High in the M74HCT158. The SELECT decoding determines whether the A or B inputs get routed to their corresponding Y outputs. All inputs are equipped with protection circuits against static discharge and transient excess voltage. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

CHIP CARRIER

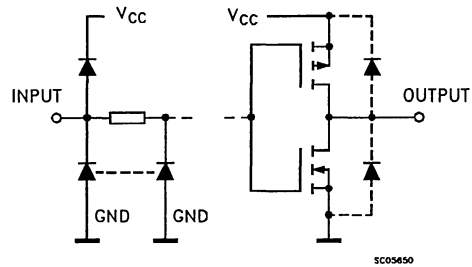
HCT157



HCT158



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION (for HCT157)

PIN No	SYMBOL	NAME AND FUNCTION
1	SELECT	Common Data Select Input
2, 5, 11, 14	1A to 4A	Data Inputs From Source A
3, 6, 10, 13	1B to 4B	Data Inputs From Source B
4, 7, 9, 12	1Y to 4Y	Multiplexer Output
15	$\overline{\text{STROBE}}$	Strobe Input
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

PIN DESCRIPTION (for HCT158)

PIN No	SYMBOL	NAME AND FUNCTION
1	SELECT	Common Data Select Input
2, 5, 11, 14	1A to 4A	Data Inputs From Source A
3, 6, 10, 13	1B to 4B	Data Inputs From Source B
4, 7, 9, 12	$\overline{1Y}$ to $\overline{4Y}$	Multiplexer Output
15	$\overline{\text{STROBE}}$	Strobe Input
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

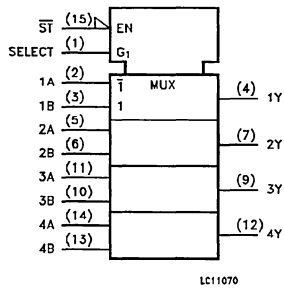
TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{STROBE}$	SELECT	A	B	Y (HCT157)	$\overline{Y}$ (HCT158)
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

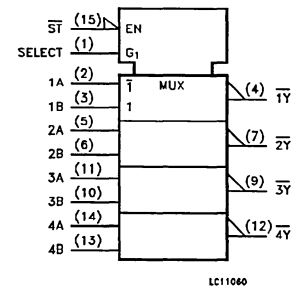
X: DON'T CARE

IEC LOGIC SYMBOL

HCT157

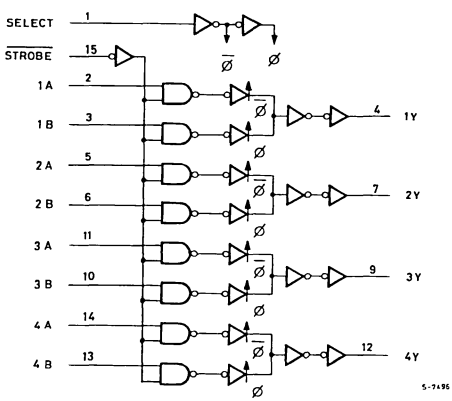


HCT158



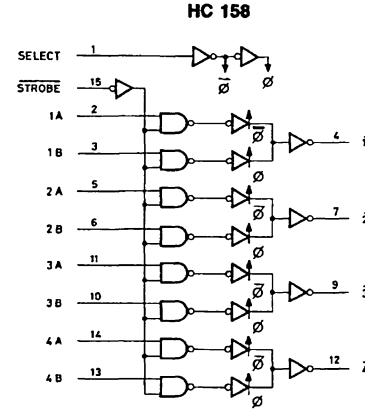
LOGIC DIAGRAM

HCT157



HCT158

HC 158



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

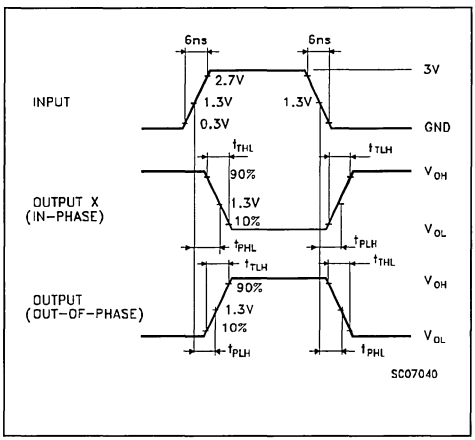
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				4		40		80	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9		3.0	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

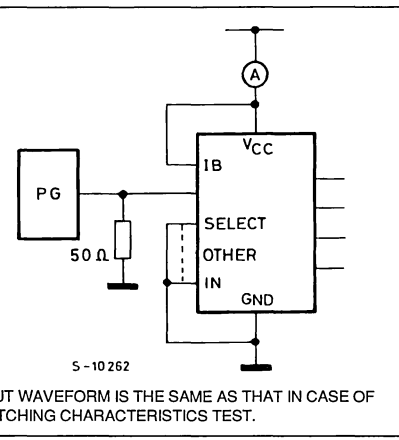
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			8	15		19		22	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A, B - Y)	4.5			16	25		31		38	ns
t_{PLH} t_{PHL}	Propagation Delay Time (SELECT - Y)	4.5			19	30		38		45	ns
t_{PLH} t_{PHL}	Propagation Delay Time (STROBE - Y)	4.5			17	27		34		41	ns
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance		HCT157		50						pF
			HCT158		60						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per channel)

SWITCHING CHARACTERISTICS TEST CIRCUIT



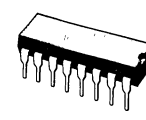
TEST CIRCUIT I_{CC} (Opr.)



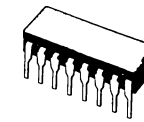
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SYNCHRONOUS PRESETTABLE 4-BIT COUNTER

- HIGH SPEED
  f_{MAX} = 63 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT 25 °C
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS160 ~ 163



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

DESCRIPTION

M54/74HC160 Decade, Asynchronous Clear
M54/74HC161 Binary, Asynchronous Clear
M54/74HC162 Decade, Synchronous Clear
M54/74HC163 Binary, Synchronous Clear

The M54/74HC160, 161, 162 and 163 are high speed CMOS SYNCHRONOUS PRESETTABLE COUNTERS fabricated with silicon gate C^2MOS technology.

They have the same the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The M54/74HC160/162 are BCD Decade counters and the M54/74HC161/163 are 4 bit binary counters.

The CLOCK input is active on the rising edge. Both $\overline{LOAD}$ and $\overline{CLEAR}$ inputs are active Low.

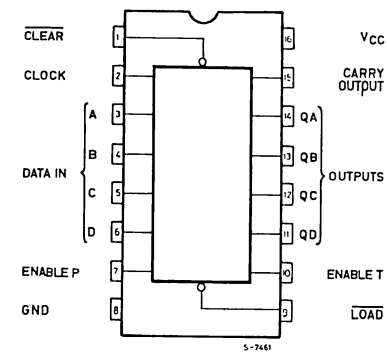
Presetting of all four IC's is synchronous on the rising edge of the CLOCK.

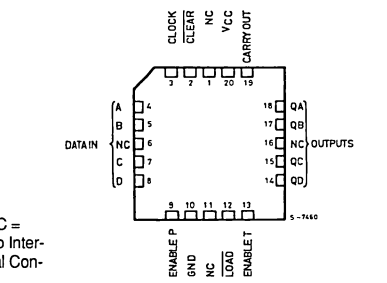
The function on the M54/74HC162/163 is synchronous to CLOCK, while the M54/74HC160/161 counters are cleared asynchronously.

Two enable inputs (TE and PE) and CARRY output are provided to easily cascading of counters, which facilities easy implementation of N-bit counters without using external gates.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

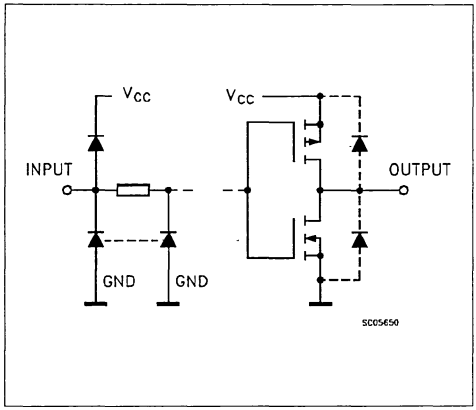
PIN CONNECTIONS (top view)





NC = No Internal Con-

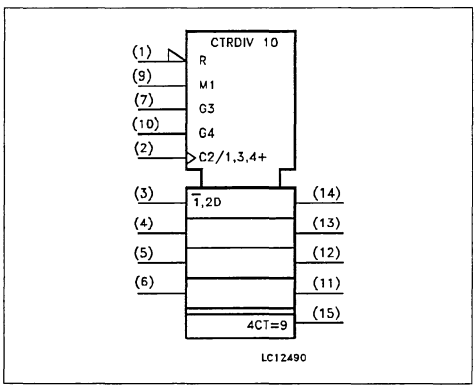
INPUT AND OUTPUT EQUIVALENT CIRCUIT



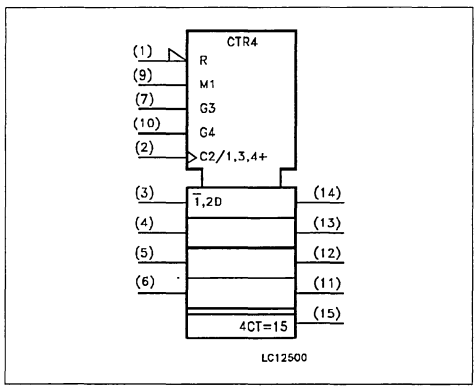
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	CLEAR	Asynchronous Master reset
2	CLOCK	Clock Input (LOW to HIGH, Edge-triggered)
3, 4, 5, 6	A, B, C, D	Data Inputs
7	ENABLE P	Count Enable Input
10	ENABLET	Count Enable Carry Input
9	$\overline{LOAD}$	Parallel Enable Input
14, 13, 12, 11	QA to QD	Flip Flop Outputs
15	CARRY OUTPUT	Terminal Count Output
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

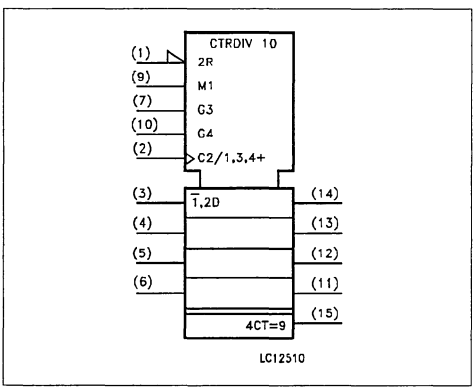
IEC LOGIC SYMBOL (HC160)



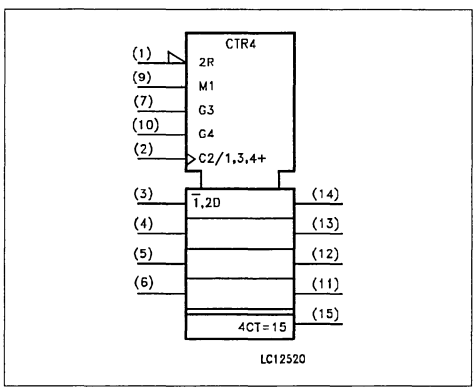
IEC LOGIC SYMBOL (HC161)



IEC LOGIC SYMBOL (HC162)



IEC LOGIC SYMBOL (HC163)

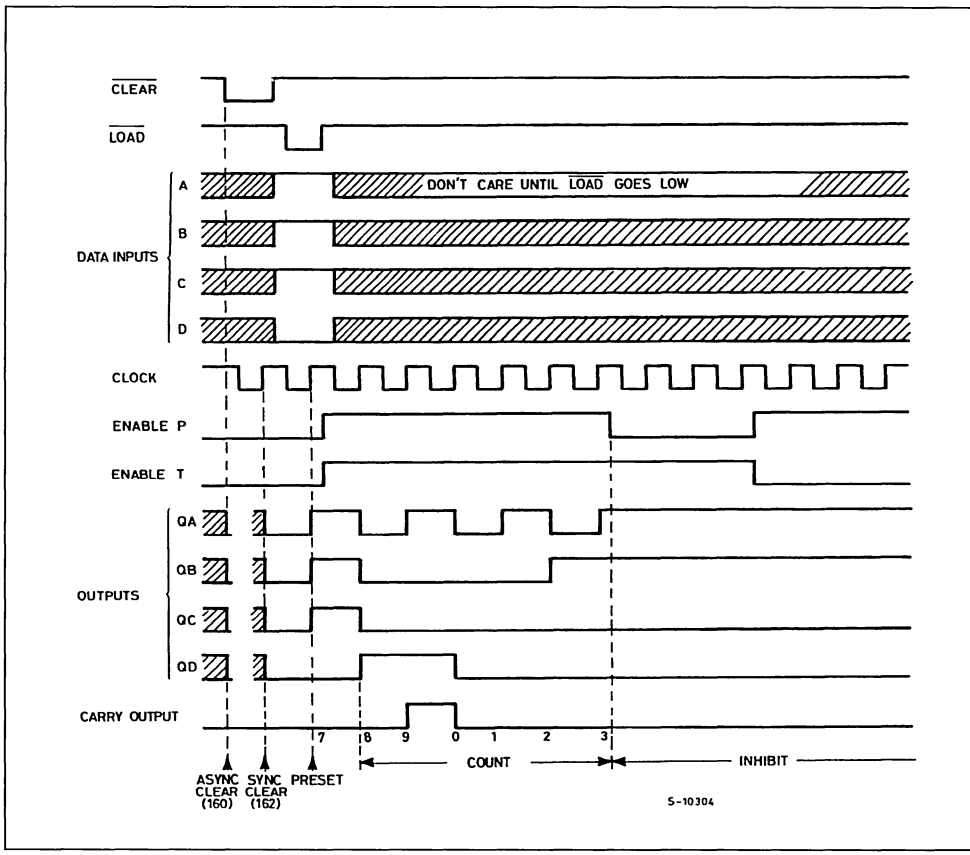


TRUTH TABLE

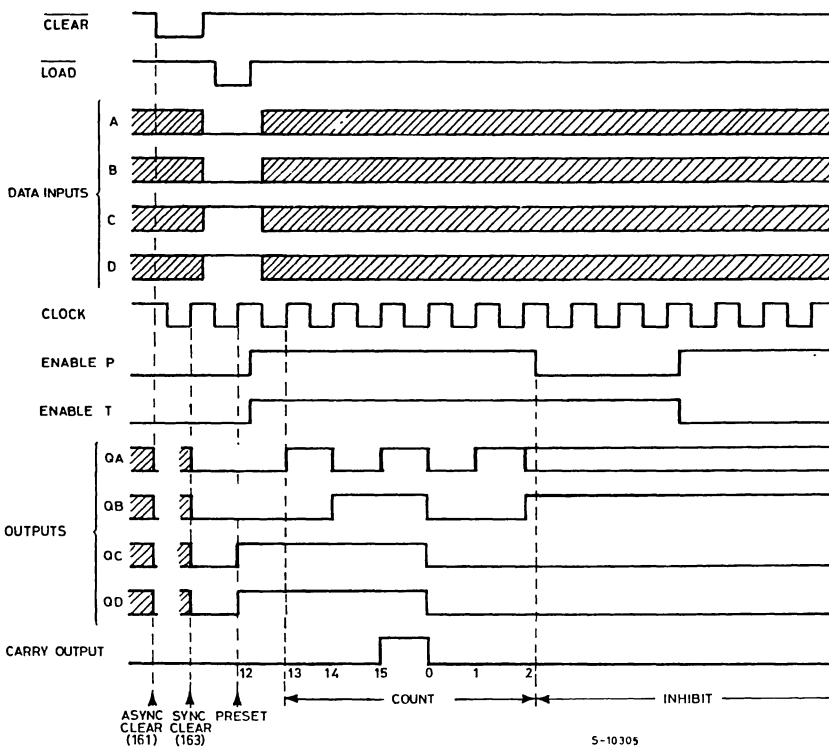
M54/74HC160/161 INPUTS					M54/74HC162/163 INPUTS					OUTPUTS				FUNCTION
$\overline{CLR}$	$\overline{LD}$	PE	TE	CK	$\overline{CLR}$	$\overline{LD}$	PE	TE	CK	QA	QB	QC	QD	
L	X	X	X	X	L	X	X	X	↑	L	L	L	L	RESET TO "0"
H	L	X	X	↑	H	L	X	X	↑	A	B	C	D	PRESET DATA
H	H	X	L	↑	H	H	X	L	↑	NO CHANGE				NO COUNT
H	H	L	X	↑	H	H	L	X	↑	NO CHANGE				NO COUNT
H	H	H	H	↑	H	H	H	H	↑	COUNT UP				COUNT
H	X	X	X	↓	X	X	X	X	↓	NO CHANGE				NO COUNT

Note: X : Don't Care
A, B, C, D : Logi level of data inputs
Carry : CARRY = TE • Q_A • $\overline{Q_B}$ • $\overline{Q_C}$ • Q_D ..... (M54/74HC160/162)
: CARRY = TE • Q_A • Q_B • Q_C • Q_D ..... (M54/74HC161/163)

TIMING CHART (HC160/162 : decade counter)

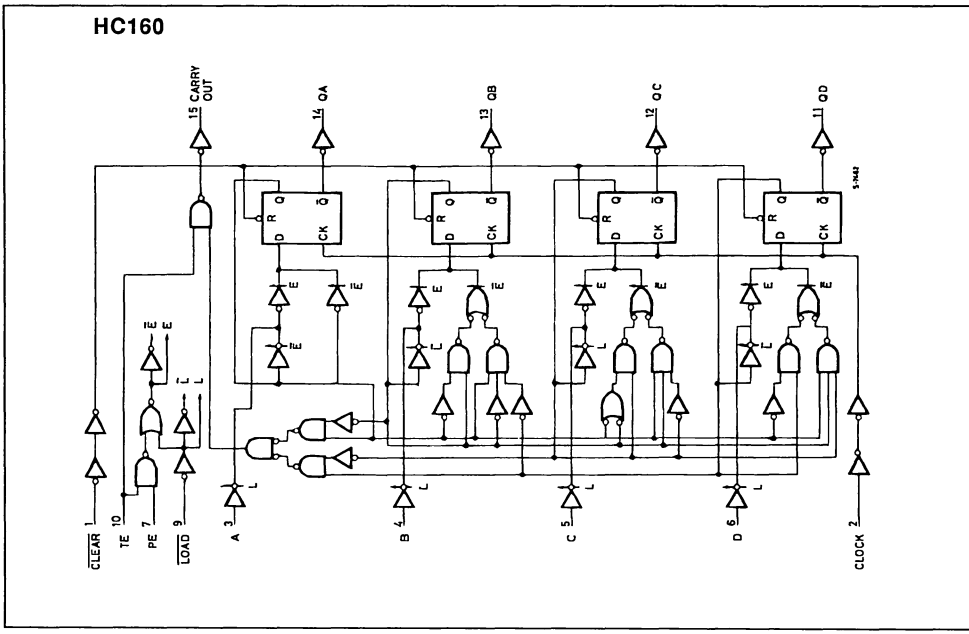


TIMING CHART (HC161/163 : binary counter)



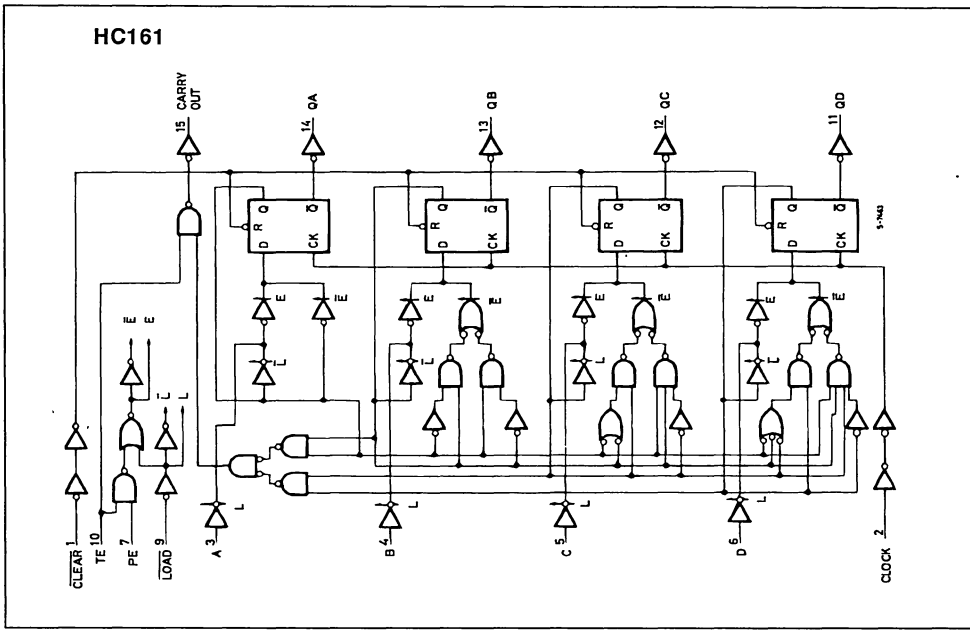
LOGIC DIAGRAM

HC160

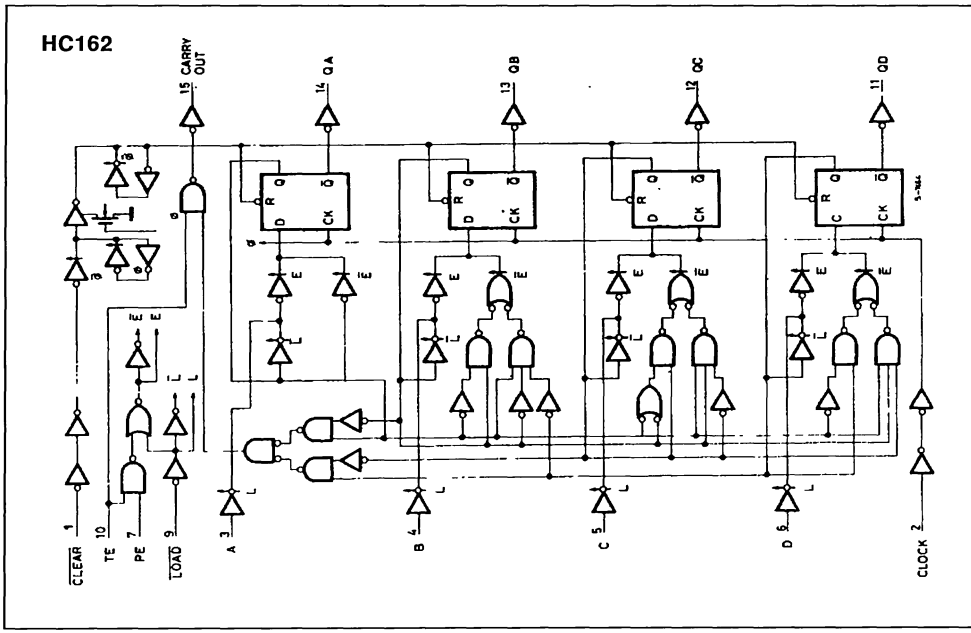


LOGIC DIAGRAM

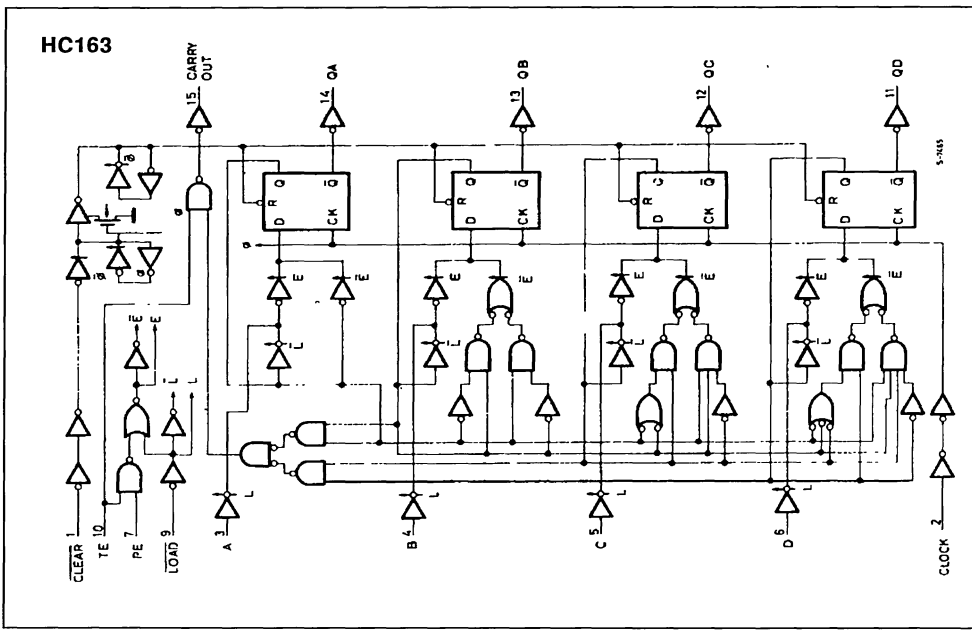
HC161



LOGIC DIAGRAM



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied

(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			25	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q)	2.0			48	125		155		190	ns
		4.5			16	25		31		38	
		6.0			14	21		26		32	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-CARRY)	2.0	COUNT MODE		57	150		190		225	ns
		4.5			19	30		38		45	
		6.0			16	26		32		38	
t_{PLH}	Propagation Delay Time (CLOCK-CARRY)	2.0	PRESET MODE		66	175		220		265	ns
		4.5			22	35		44		53	
		6.0			19	30		37		45	
t_{PHL}	Propagation Delay Time (CLOCK-CARRY)	2.0	PRESET MODE		72	200		250		300	ns
		4.5			24	40		50		60	
		6.0			20	34		43		51	
t_{PLH} t_{PHL}	Propagation Delay Time (ENT-CARRY)	2.0			39	100		125		150	ns
		4.5			13	20		25		30	
		6.0			11	17		21		26	
t_{PLH}	Propagation Delay Time (CLEAR - Q)	2.0	for HC160/161 only		60	150		190		225	ns
		4.5			20	30		38		45	
		6.0			17	26		32		38	
t_{PHL}	Propagation Delay Time (CLEAR-CARRY)	2.0	for HC160/161 only		72	200		250		300	ns
		4.5			24	40		50		60	
		6.0			20	34		43		51	
f_{MAX}	Maximum Clock Frequency	2.0		6.2	18		5		4.2		MHz
		4.5		31	53		25		21		
		6.0		37	62		30		25		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0			18	75		95		110	ns
		4.5			6	15		19		22	
		6.0			6	13		16		19	
$t_{W(L)}$	Minimum Pulse Width (CLEAR)	2.0	for HC160/161 only		24	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
t_s	Minimum Set-up Time (LOAD, PE, TE)	2.0			40	100		125		150	ns
		4.5			10	20		25		30	
		6.0			8	17		21		26	
t_s	Minimum Set-up Time (A, B, C, D)	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			3	13		16		19	
t_s	Minimum Set-up Time (CLEAR)	2.0	for HC162/163 only		20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			3	13		16		19	

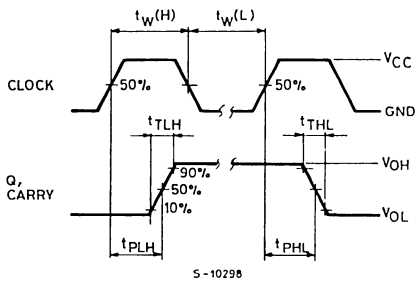
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_h	Minimum Hold Time (A, B - CK)	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Minimum Removal Time	2.0			18	50		65		75	ns
		4.5			4	10		13		15	
		6.0			3	9		11		13	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				50						pF

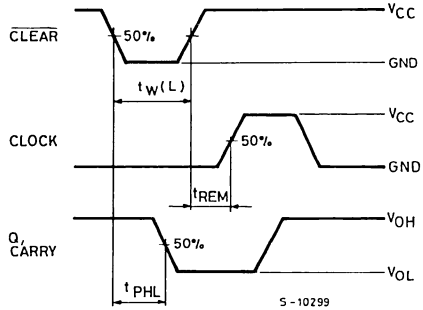
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

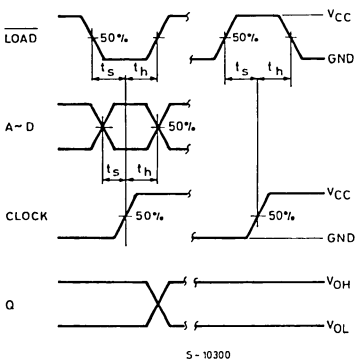
COUNT MODE



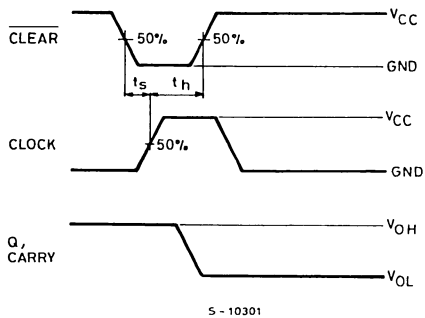
CLEAR MODE (HC160/161)



PRESET MODE

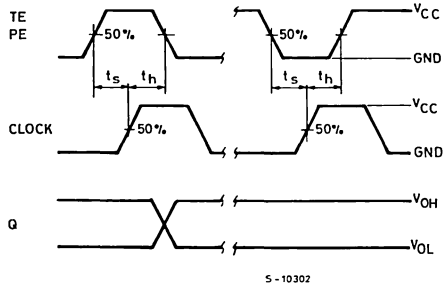


CLEAR MODE (HC162/163)



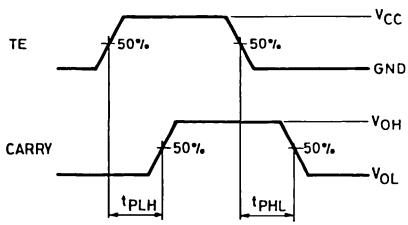
SWITCHING CHARACTERISTICS TEST WAVEFORM (continued)

COUNTENABLE MODE



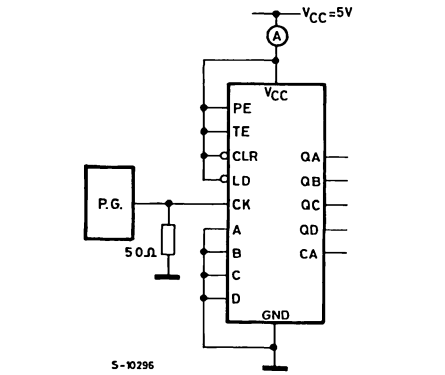
S-10302

CASCADE MODE
(fix maximum count)



S-10303

TEST CIRCUIT I_{CC} (Opr.)



S-10296

TOTAL OPERATING CURRENT WHEN USING A CAPACITIVE LOAD

When the outputs drive a capacitive load, the total current can be calculated as follows :

For M74HC160/162 :

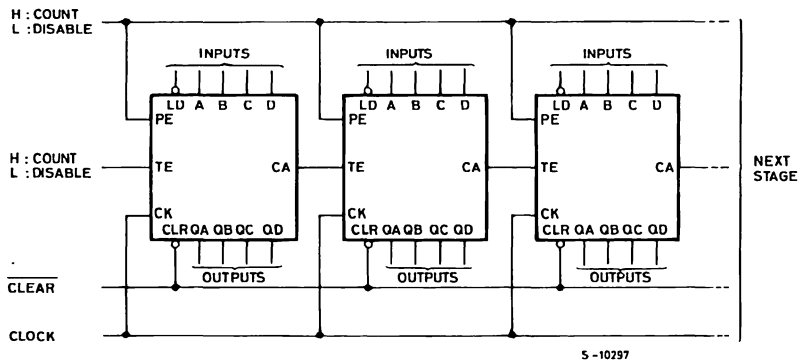
$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \cdot \left(\frac{C_a}{2} + \frac{C_b}{5} + \frac{C_c}{10} + \frac{C_d}{10} + \frac{C_{ca}}{10} \right)$$

For M74HC161/163 :

$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \cdot \left(\frac{C_a}{2} + \frac{C_b}{4} + \frac{C_c}{8} + \frac{C_d}{16} + \frac{C_{ca}}{16} \right)$$

C_a to C_{ca} are the capacitors loading the outputs.

TYPICAL APPLICATION

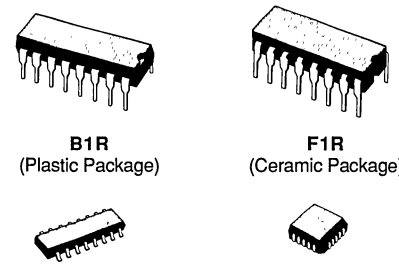


S-10297

M54/74HCT160/161
M54/74HCT162/163

SYNCHRONOUS PRESETTABLE 4-BIT COUNTER

- HIGH SPEED
  f_{MAX} = 50 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT 25 °C
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- SYMMETRICAL OUTPUT IMPEDANCE
  $I_{OH} = I_{OL}$ = 4 mA (MIN.)
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.); V_{IL} = 0.8V (MAX.)
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS160 ~ 163



B1R (Plastic Package)

F1R (Ceramic Package)

M1R (Micro Package)

C1R (Chip Carrier)

ORDER CODES :

M54HCTXXXF1R M74HCTXXXM1R
M74HCTXXXB1R M74HCTXXXC1R

DESCRIPTION

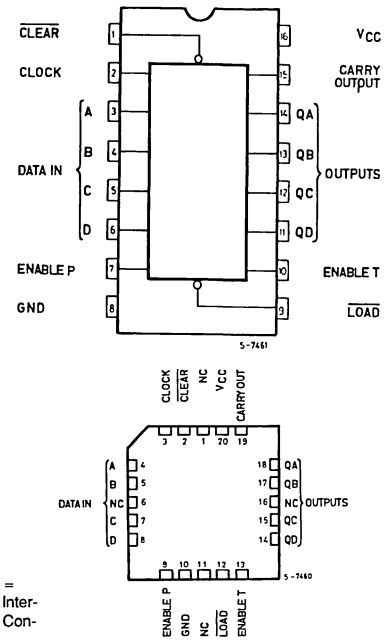
M54/74HCT160 Decade, Asynchronous Clear
M54/74HCT161 Binary, Asynchronous Clear
M54/74HCT162 Decade, Synchronous Clear
M54/74HCT163 Binary, Synchronous Clear

The M54/74HCT160, 161, 162 and 163 are high speed CMOS SYNCHRONOUS PRESETTABLE COUNTERS fabricated with silicon gate C^2MOS technology. They have the same high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The M54/74HCT160/162 are BCD Decade counters and the M54/74HCT161/163 are 4 bit binary counters. The CLOCK input is active on the rising edge. Both $\overline{LOAD}$ and $\overline{CLEAR}$ inputs are active Low.

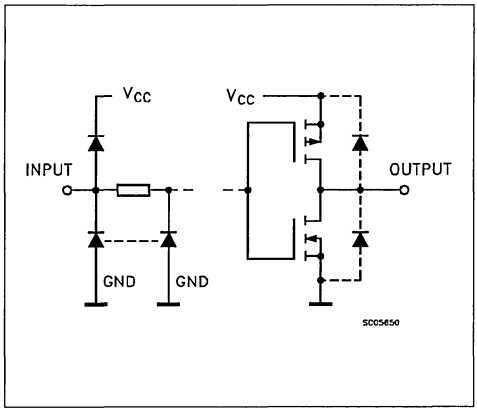
Presetting of all four IC's is synchronous on the rising edge of the CLOCK. The function on the M54/74HCT162/163 is synchronous to CLOCK, while the M54/74HCT160/161 counters are cleared asynchronously. Two enable inputs (TE and PE) and CARRY output are provided to enable easy cascading of counters, which facilities easy implementation of N-bit counters without using external gates. This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption. All inputs are equipped with

PIN CONNECTIONS (top view)



NC = No Internal Con-

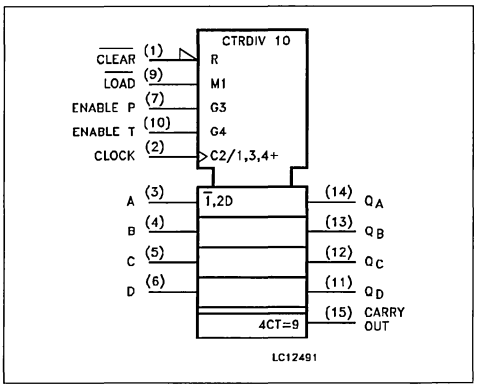
INPUT AND OUTPUT EQUIVALENT CIRCUIT



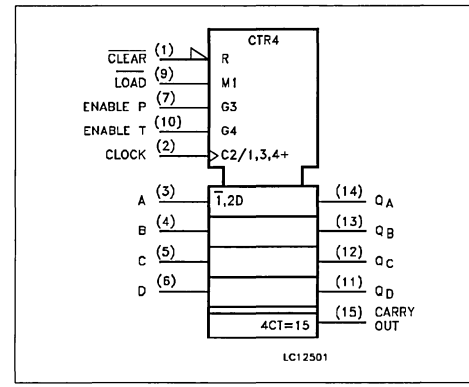
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{\text{CLEAR}}$	Master Reset
2	CLOCK	Clock Input (LOW to HIGH, Edge-triggered)
3, 4, 5, 6	A, B, C, D	Data Inputs
7	ENABLE P	Count Enable Input
10	ENABLET	Count Enable Carry Input
9	$\overline{\text{LOAD}}$	Parallel Enable Input
14, 13, 12, 11	QA to QD	Flip Flop Outputs
15	CARRY OUTPUT	Terminal Count Output
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

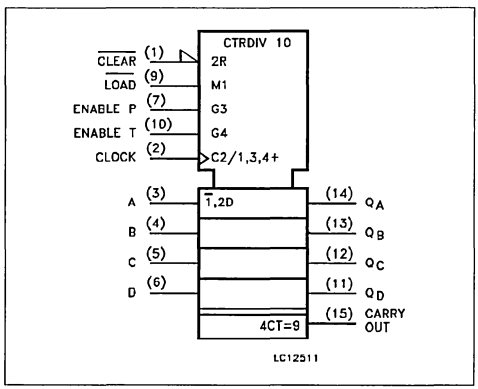
IEC LOGIC SYMBOL (HCT160)



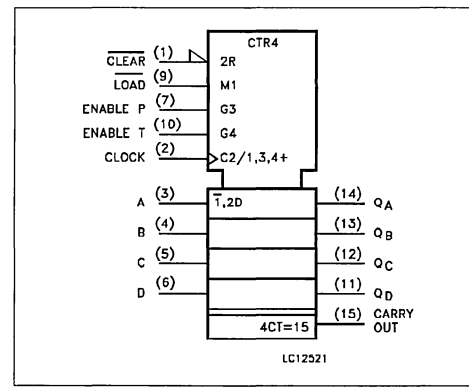
IEC LOGIC SYMBOL (HCT161)



IEC LOGIC SYMBOL (HCT162)



IEC LOGIC SYMBOL (HCT163)

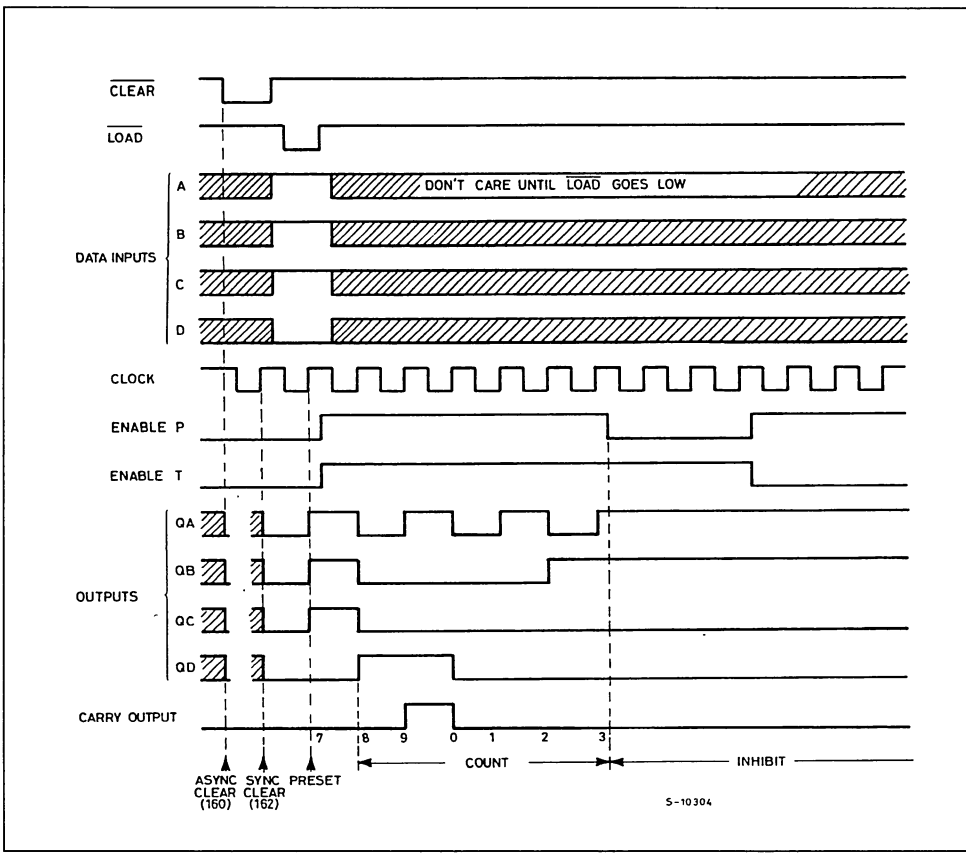


TRUTH TABLE

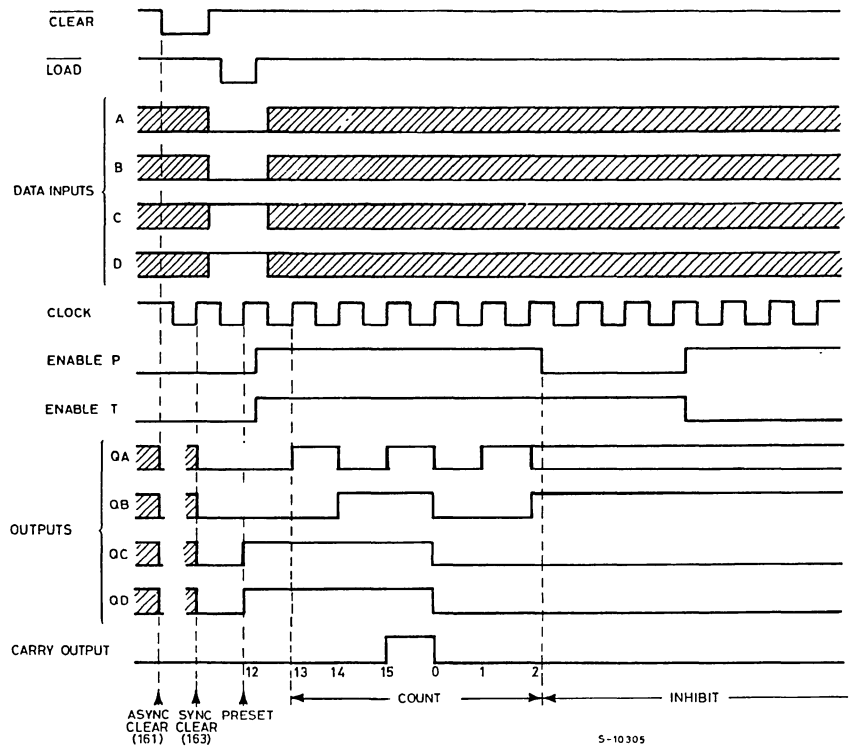
M54/74HCT160/161 INPUTS					M54/74HCT162/163 INPUTS					OUTPUTS				FUNCTION
$\overline{CLR}$	$\overline{LD}$	PE	TE	CK	$\overline{CLR}$	$\overline{LD}$	PE	TE	CK	QA	QB	QC	QD	
L	X	X	X	X	L	X	X	X	⌐	L	L	L	L	RESET TO "0"
H	L	X	X	⌐	H	L	X	X	⌐	A	B	C	D	PRESET DATA
H	H	X	L	⌐	H	H	X	L	⌐	NO CHANGE				NO COUNT
H	H	L	X	⌐	H	H	L	X	⌐	NO CHANGE				NO COUNT
H	H	H	H	⌐	H	H	H	H	⌐	COUNT UP				COUNT
H	X	X	X	⌙	X	X	X	X	⌙	NO CHANGE				NO COUNT

Note: X : Don't Care
A, B, C, D : Logi level of data inputs
Carry : CARRY = TE • Q_A • Q_B • $\overline{Q_C}$ • Q_D ..... (M54/74HCT160/162)
: CARRY = TE • Q_A • Q_B • Q_C • Q_D ..... (M54/74HCT161/163)

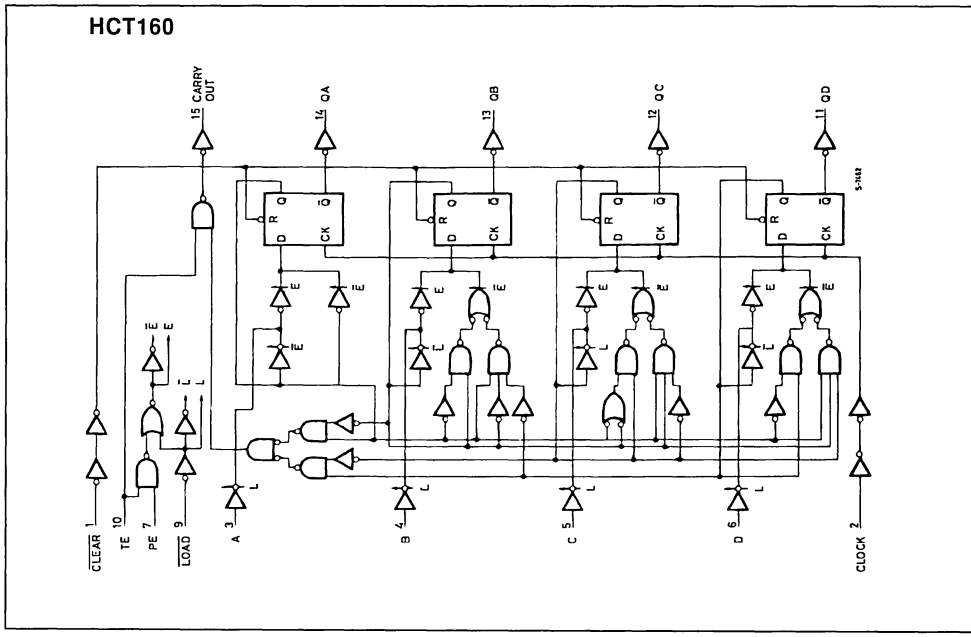
TIMING CHART (HCT160/162 : decade counter)



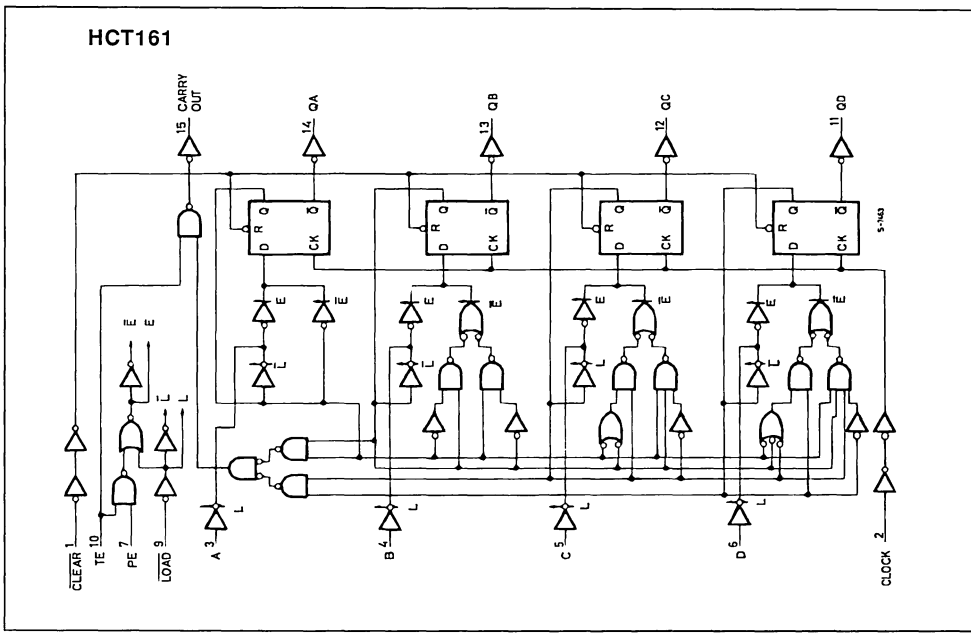
TIMING CHART (HCT161/163 : binary counter)



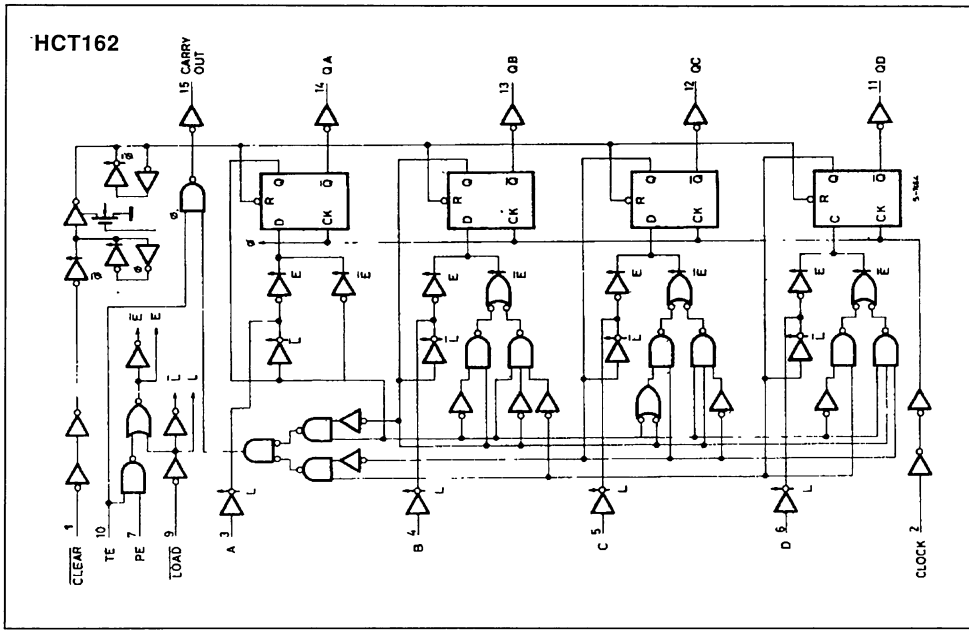
LOGIC DIAGRAM



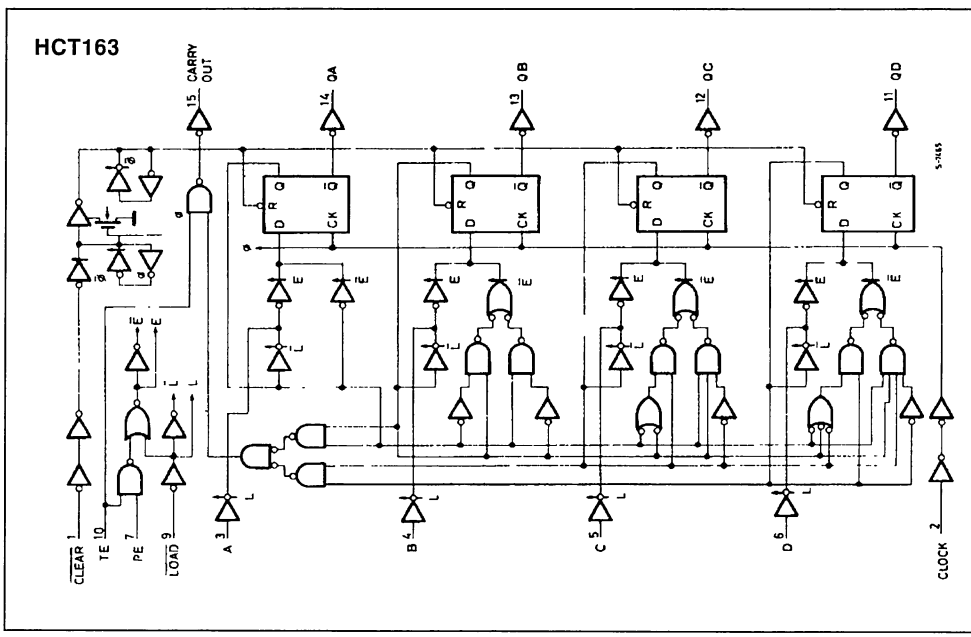
LOGIC DIAGRAM



LOGIC DIAGRAM



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				4		40		80	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND				2.0		2.9		3.0	mA

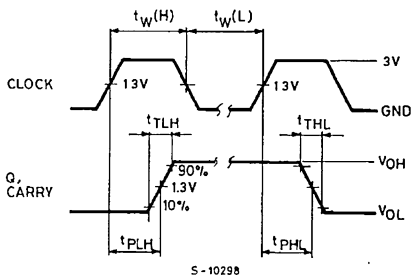
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			8	15		19		22	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CK - Q)	4.5			23	36		45		54	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CK-CO)	4.5			27	42		53		63	ns
t_{PLH}	Propagation Delay Time (TE-CO)	4.5			21	33		41		50	ns
t_{PLH}	Propagation Delay Time (CLEAR - Q)	4.5	for HCT160/161 only		26	40		50		60	ns
t_{PHL}	Propagation Delay Time (CLEAR-CO)	4.5	for HCT160/161 only		28	43		54		65	ns
f_{MAX}	Maximum Clock Frequency	4.5		31	49		25		21		MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CK)	4.5			8	15		19		22	ns
$t_{W(L)}$	Minimum Pulse Width (CLEAR)	4.5	for HCT160/161 only		8	15		19		22	ns
t_s	Minimum Set-up Time (LOAD, PE, TE)	4.5			11	20		25		30	ns
t_s	Minimum Set-up Time (A, B, C, D)	4.5			5	15		19		22	ns
t_s	Minimum Set-up Time (CLEAR)	4.5	for HCT162/163 only		5	15		19		22	ns
t_h	Minimum Hold Time	4.5				5		5		8	ns
t_{REM}	Minimum Removal Time (CLEAR)	4.5	for HCT160/161 only		5	15		19		22	ns
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				33						pF

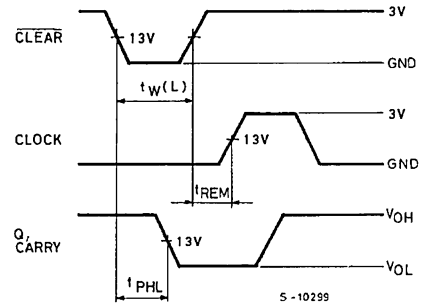
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

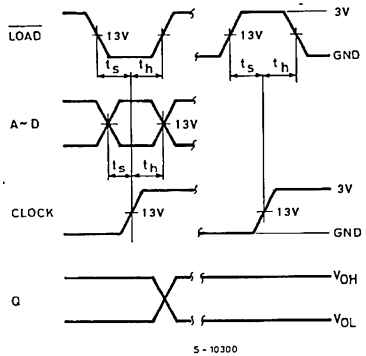
COUNT MODE



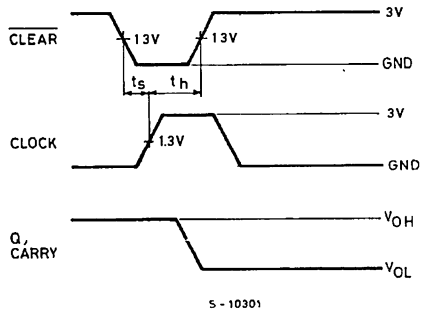
CLEAR MODE (HCT160/161)



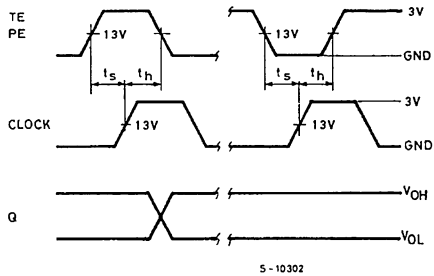
PRESET MODE



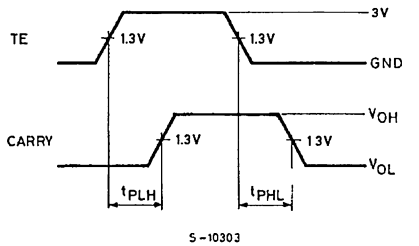
CLEAR MODE (HCT162/163)



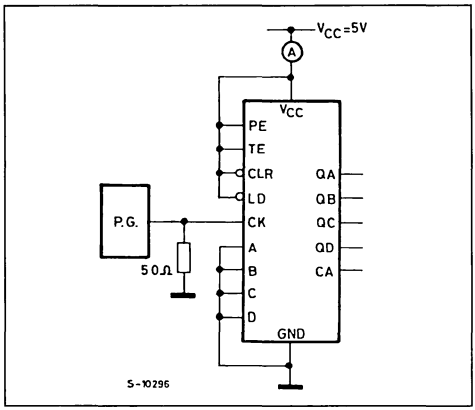
COUNTENABLE MODE



CASCADE MODE (fix maximum count)



TEST CIRCUIT I_{CC} (Opr.)



TOTAL OPERATING CURRENT WHEN USING A CAPACITIVE LOAD

When the outputs drive a capacitive load, the total current can be calculated as follows :

For M74HCT160/162 :

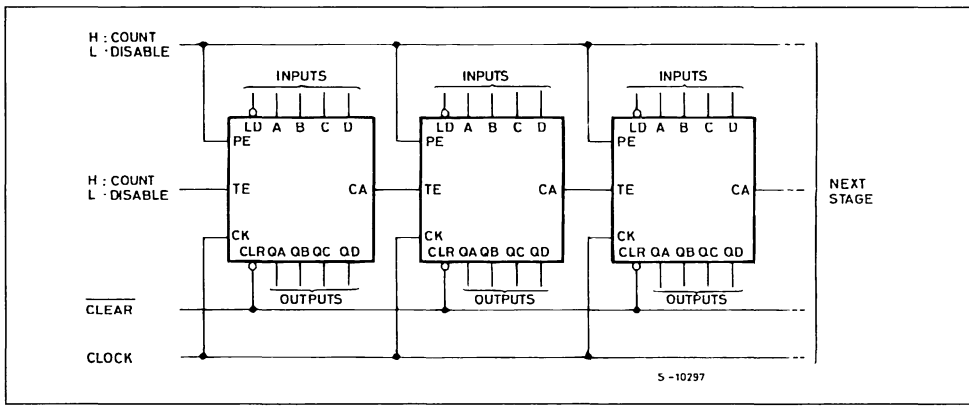
$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \cdot \left(\frac{C_a}{2} + \frac{C_b}{5} + \frac{C_c}{10} + \frac{C_d}{10} + \frac{C_{ca}}{10} \right)$$

For M74HCT161/163 :

$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \cdot \left(\frac{C_a}{2} + \frac{C_b}{4} + \frac{C_c}{8} + \frac{C_d}{16} + \frac{C_{ca}}{16} \right)$$

C_a to C_{ca} are the capacitors loading the outputs.

TYPICAL APPLICATION

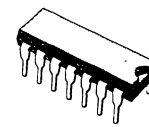


SGS-THOMSON MICROELECTRONICS

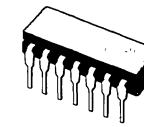
M54HC164
M74HC164

8 BIT SIPO SHIFT REGISTER

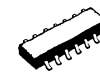
- HIGH SPEED
  t_{PD} = 15 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- SYMMETRICAL OUTPUT IMPEDANCE
  $I_{OL} = |I_{OH}|$ = 4 mA (MIN.)
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS164



B1R
(Plastic Package)



F1R
(Ceramic Package)



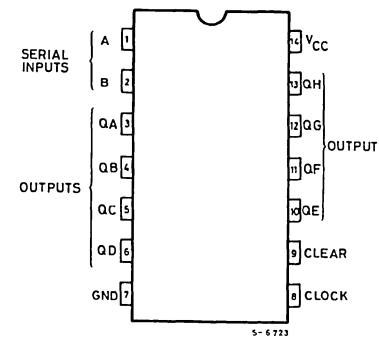
M1R
(Micro Package)

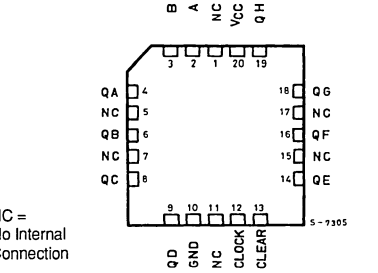
C1R
(Chip Carrier)

ORDER CODES :

M54HC164F1R M74HC164M1R
M74HC164B1R M74HC164C1R

PIN CONNECTIONS (top view)





NC =
No Internal
Connection

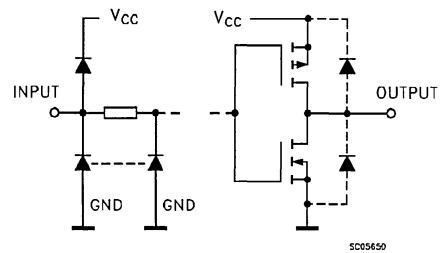
DESCRIPTION

The M54/74HC164 is a high speed CMOS 8 BIT SIPO SHIFT REGISTER fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

The HC164 is an 8 bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B), either of these inputs can be used as an active high enable for data entry through the other input. An unused input must be high, or both inputs connected together. Each low-to-high transition on the clock input shifts data one place to the right and enters into QA, the logic NAND of the two data inputs $(\overline{A \cdot B})$, the data that existed before the rising clock edge. A low level on the clear input overrides all other inputs and clears the register asynchronously, forcing all Q outputs low.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



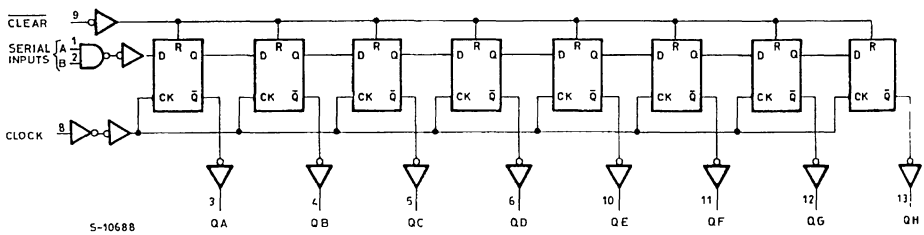
TRUTH TABLE

INPUTS				OUTPUS			
$\overline{CLEAR}$	CLOCK	SERIAL IN		QA	QB	.....	QH
		A	B				
L	X	X	X	L	L	.....	L
H	⊓	X	X	NO CHANGE			
H	⊔	L	X	L	QAn	.....	QGn
H	⊔	X	L	L	QAn	.....	QGn
H	⊔	H	H	H	QAn	.....	QGn

X: Don't Care

QAn - QGn : The level of QA -QG, respectively. before the most-recent transition of th clock.

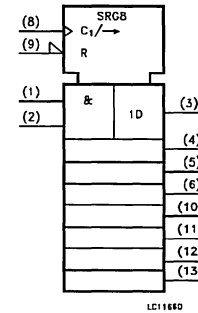
LOGIC DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2	A, B	Data Inputs
3, 4, 5, 6, 10, 11, 12, 13	QA to QH	Outputs
8	CLOCK	Clock Input (LOW to HIGH, Edge-triggered)
9	$\overline{CLEAR}$	Master Reset Input
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

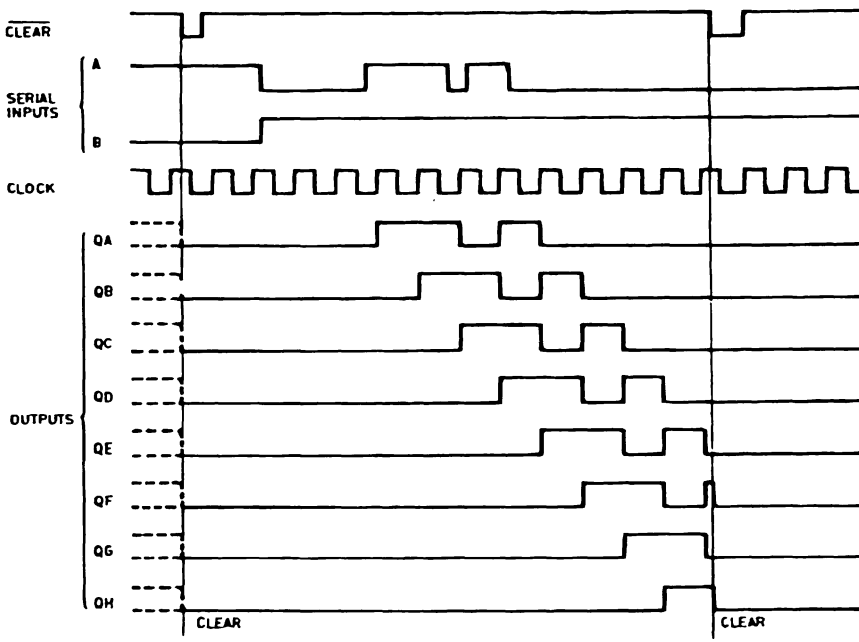
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q)	2.0			57	160		200		240	ns
		4.5			19	32		40		48	
		6.0			16	27		34		41	
t_{PHL}	Propagation Delay Time (CLEAR - Q)	2.0			60	175		220		265	ns
		4.5			20	35		44		53	
		6.0			17	30		37		45	
f_{MAX}	Maximum Clock Frequency	2.0		6.2	18		5.0		4.2		MHz
		4.5		31	53		25		21		
		6.0		37	62		30		25		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0			24	75		95		110	ns
		4.5			6	15		19		22	
		6.0			5	13		16		19	
$t_{W(L)}$	Minimum Pulse Width (CLEAR)	2.0			40	75		95		110	ns
		4.5			10	15		19		22	
		6.0			9	13		16		19	
t_s	Minimum Set-up Time (A, B - CK)	2.0			16	50		65		75	ns
		4.5			4	10		13		15	
		6.0			3	9		11		13	
t_h	Minimum Hold Time (A, B - CK)	2.0				5		5		5	ns
		4.5				5		5		5	
		6.0				5		5		5	
t_{REM}	Minimum Removal Time	2.0				5		5		5	ns
		4.5				5		5		5	
		6.0				5		5		5	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				99						pF

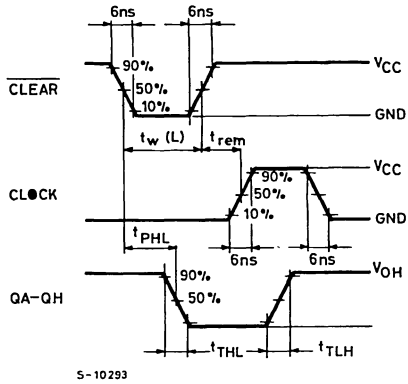
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

TIMING CHART

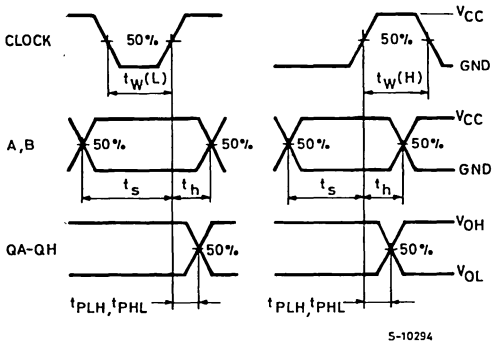


SWITCHING CHARACTERISTICS TEST WAVEFORM

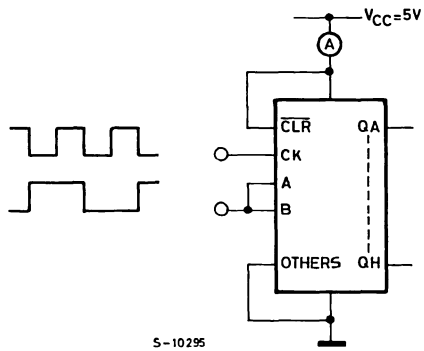
CLEAR MODE



SERIAL MODE



TEST CIRCUIT I_{CC} (Opr.)



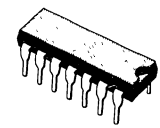
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

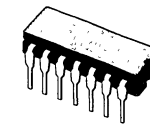
M54HCT164
M74HCT164

8 BIT SIPO SHIFT REGISTER

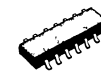
- HIGH SPEED
  t_{PD} = 20 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$ = 4 mA (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE
  $I_{OL} = |I_{OH}|$ = 4 mA (MIN)
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS164



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HCT164F1R M74HCT164M1R
M74HCT164B1R M74HCT164C1R

DESCRIPTION

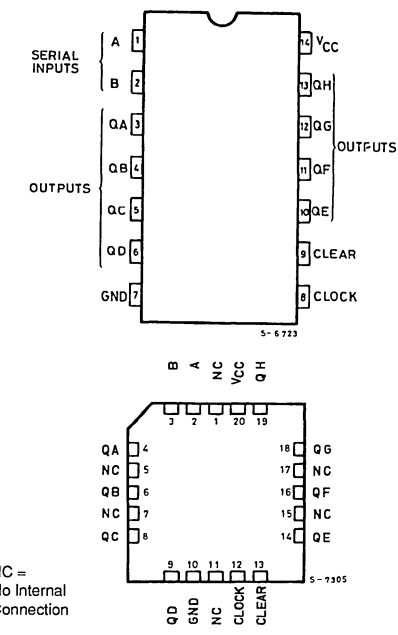
The M54/74HCT164 is a high speed CMOS 8 BIT SIPO SHIFT REGISTER fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

The HCT164 is an 8 bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B), either of these inputs can be used as an active high enable for data entry through the other input. An unused input must be high, or both inputs connected together. Each low-to-high transition on the clock input shifts data one place to the right and enters into QA, the logic NAND of the two data inputs ($\overline{A \bullet B}$), the data that existed before the rising clock edge. A low level on the clear input overrides all other inputs and clears the register asynchronously, forcing all Q outputs low.

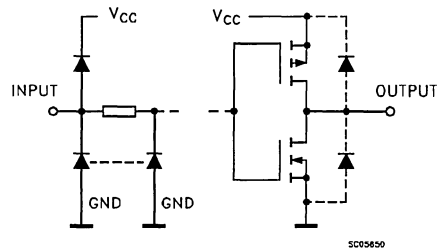
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

PIN CONNECTIONS (top view)



INPUT AND OUTPUT EQUIVALENT CIRCUIT



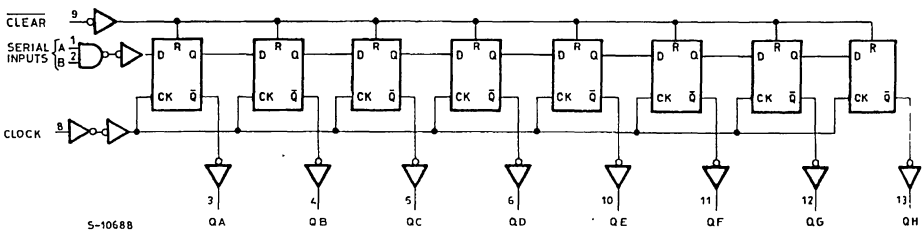
TRUTH TABLE

INPUTS				OUTPUS			
$\overline{CLEAR}$	CLOCK	SERIAL IN		QA	QB	.....	QH
		A	B				
L	X	X	X	L	L	.....	L
H	⌐_	X	X	NO CHANGE			
H	_⌐	L	X	L	QAn	.....	QGn
H	_⌐	X	L	L	QAn	.....	QGn
H	_⌐	H	H	H	QAn	.....	QGn

X: Don't Care

QAn - QGn : The level of QA -QG, respectively. before the most-recent transition of th clock.

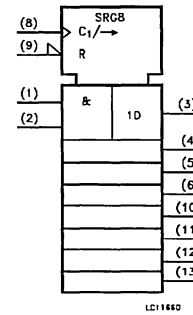
LOGIC DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2	A, B	Data Inputs
3, 4, 5, 6, 10, 11, 12, 13	QA to QH	Outputs
8	CLOCK	Clock Input (LOW to HIGH, Edge-triggered)
9	$\overline{CLEAR}$	Master Reset Input
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

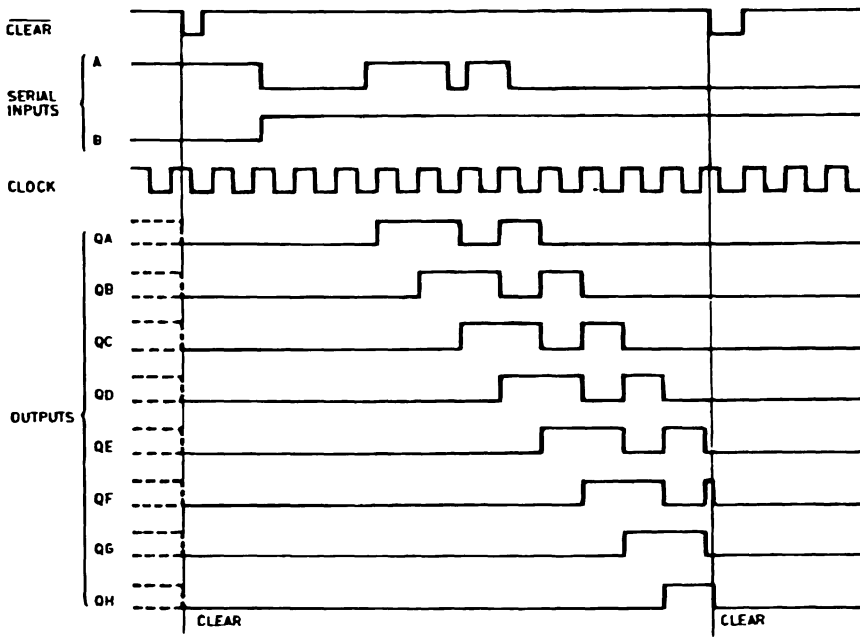
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				4		40		80	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9		3.0	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			8	15		19		22	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q)	4.5			23	36		45		54	ns
t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$ - Q)	4.5			24	37		46		56	ns
f_{MAX}	Maximum Clock Frequency	4.5		30	50		24		20		MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	4.5			8	15		19		22	ns
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLEAR}$)	4.5			8	15		19		22	ns
t_s	Minimum Set-up Time (A, B - CK)	4.5			4	10		13		15	ns
t_h	Minimum Hold Time (A, B - CK)	4.5				0		0		0	ns
t_{REM}	Minimum Removal Time					5		6		8	ns
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				137						pF

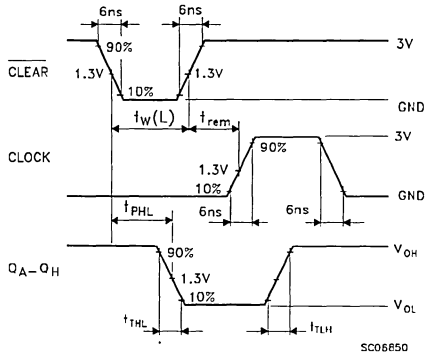
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

TIMING CHART

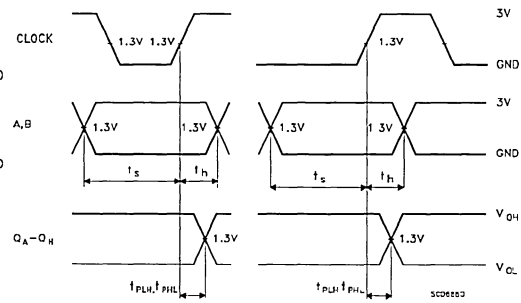


SWITCHING CHARACTERISTICS TEST WAVEFORM

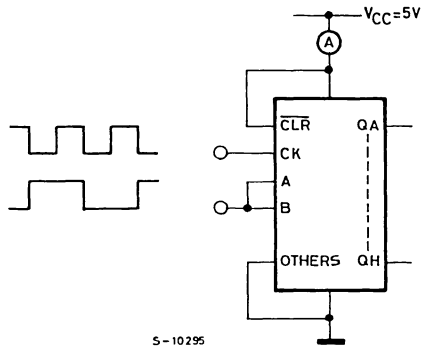
CLEAR MODE



SERIAL MODE



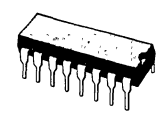
TEST CIRCUIT I_{CC} (Opr.)



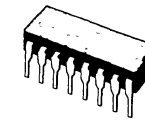
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

8 BIT PISO SHIFT REGISTER

- HIGH SPEED
  t_{PD} = 15 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- SYMMETRICAL OUTPUT IMPEDANCE
  $I_{OL} = |I_{OH}|$ = 4 mA (MIN.)
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS165



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HC165F1R	M74HC165M1R
M74HC165B1R	M74HC165C1R

DESCRIPTION

The M54/74HC165 is a high speed CMOS 8 BIT PISO SHIFT REGISTER fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

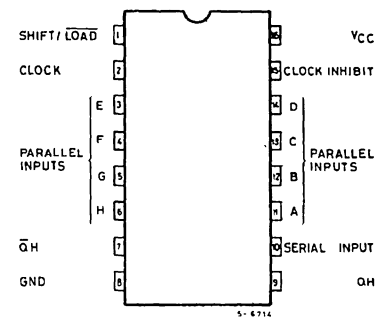
It achives the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

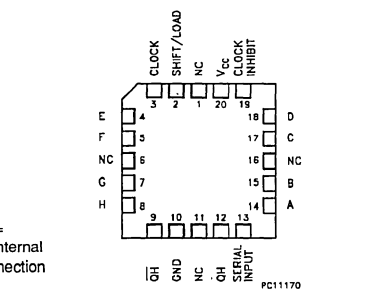
This device contains eight clocked master slave RS flip-flops connected as a shift register, with auxiliary gating to provide over-riding asynchronous parallel entry. Parallel data entres when the shift/load input is low. The parallel data can change while shift/load is low, provided that the recommended set-up and hold times are observed. For clocked operation, shift/load must be high. The two clock input perform identically; one can be used as a clock inhibit by applying a high signal; to permit this operation clocking is accomplished through a 2 input nor gate.

To avoid double clocking, however, the inhibit signal should only go high while the clock is high. Otherwise the rising inhibit signal will cause the same response as rising clock edge.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

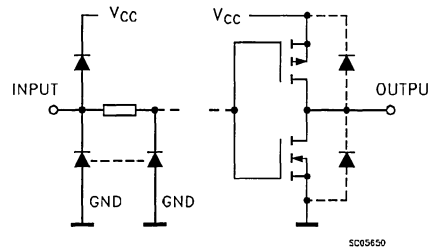
PIN CONNECTIONS (top view)





NC =
No Internal
Connection

INPUT AND OUTPUT EQUIVALENT CIRCUIT

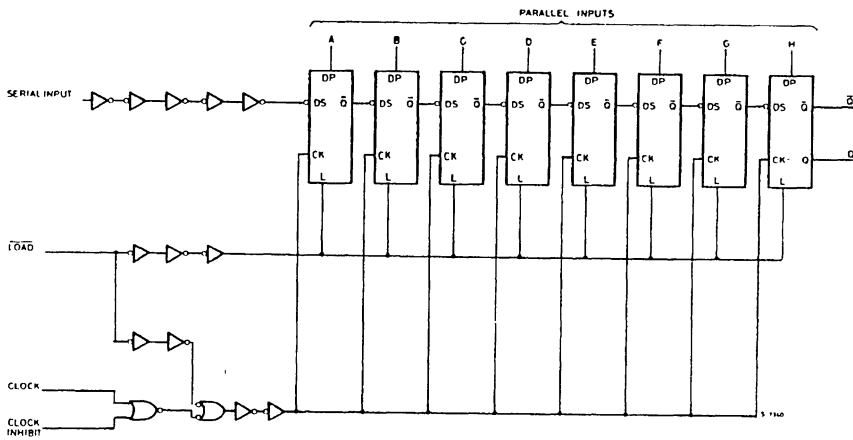


TRUTH TABLE

INPUTS					INTERNAL OUTPUTS		OUTPUS
SHIFT/ CLEAR	CLOCK INHIBIT	CLOCK	SERIAL IN	A .....H	QA	QB	QH
L	X	X	X	a.....h	a	b	h
H	L	⎍	H	X	H	QAn	QGn
H	L	⎍	L	X	L	QAn	QGn
H	⎍	L	H	X	H	QAn	QGn
H	⎍	L	L	X	L	QAn	QGn
H	X	H	X	X	NO CHANGE		
H	H	X	X	X	NO CHANGE		

a .... .h. The level of steady input voltage at inputs a through respectively
QAn - QGn : The level of QA -QG, respectively. before the most-recent transition of the clock.

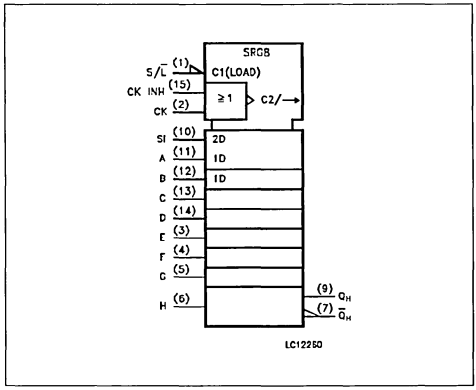
LOGIC DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{S/L}$	Asynchronous Parallel Load Input
2	$\overline{QH}$	Complementary Output
7	QH	Serial Output
9	CLOCK	Clock Input (LOW to HIGH edge triggered)
10	SI	Serial Data Input
11, 12, 13, 14, 3, 4, 5, 6	A to H	Parallel Data Inputs
15	CLOCK INH	CLock Inhibit
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

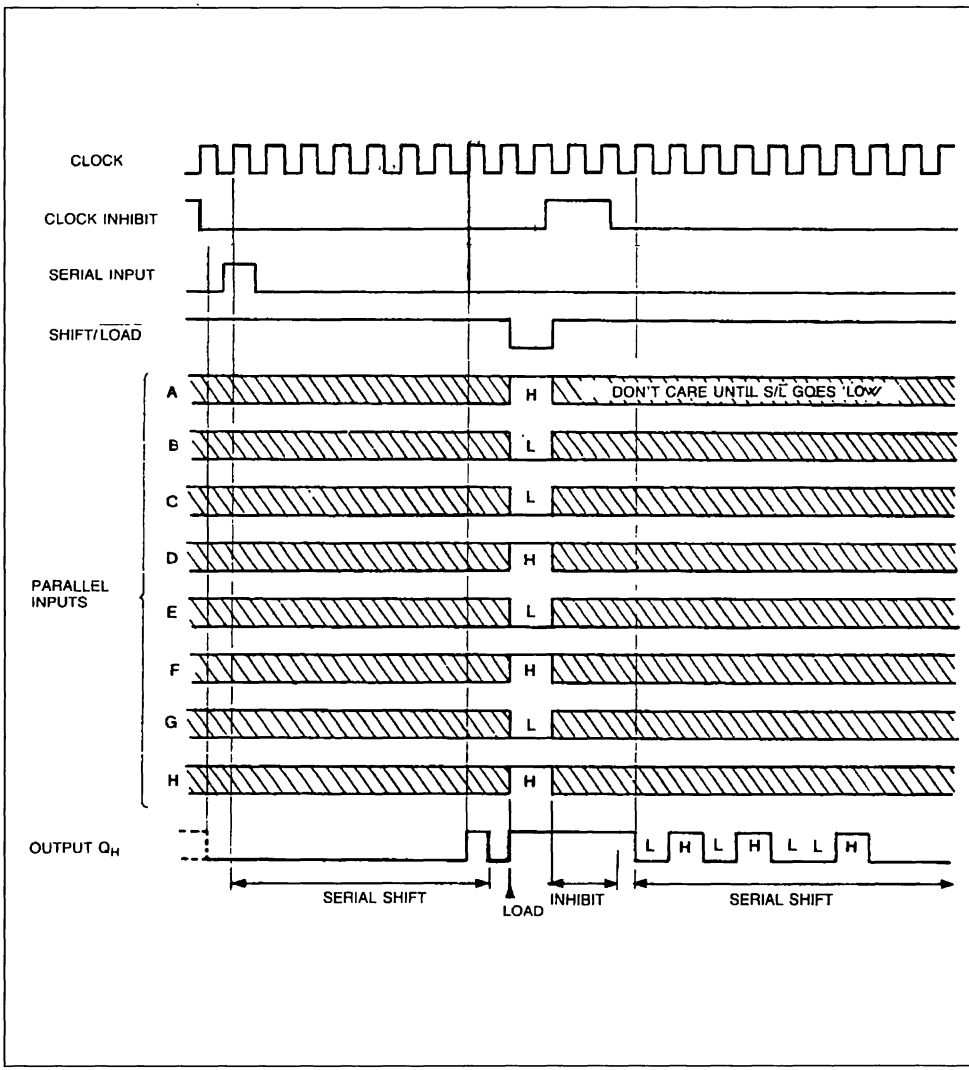
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CK - QH, $\overline{QH}$)	2.0			55	150		190		225	ns
		4.5			18	30		38		45	
		6.0			15	26		33		38	
t_{PLH} t_{PHL}	Propagation Delay Time (S/$\overline{L}$ - QH, $\overline{QH}$)	2.0			65	165		205		250	ns
		4.5			21	33		41		50	
		6.0			18	28		35		43	
t_{PLH} t_{PHL}	Propagation Delay Time (H - QH, $\overline{QH}$)	2.0			52	135		170		205	ns
		4.5			17	27		34		41	
		6.0			14	23		29		35	
f_{MAX}	Maximum Clock Frequency	2.0		7.4	15		6.0		4.8		MHz
		4.5		37	60		30		24		
		6.0		44	71		35		28		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CK)	2.0			24	75		95		110	ns
		4.5			6	15		19		22	
		6.0			5	13		16		19	
$t_{W(L)}$	Minimum Pulse Width (S/$\overline{L}$)	2.0			32	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_s	Minimum Set-up Time (PI - S/$\overline{L}$) (SI - CK) (S/$\overline{L}$ -CK)	2.0			24	75		95		110	ns
		4.5			6	15		19		22	
		6.0			5	13		16		19	
t_h	Minimum Hold Time (S/$\overline{L}$ - PI) (CK - SI) (CK - S/$\overline{L}$)	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Minimum Removal Time (CK - CKINH)	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				55						pF

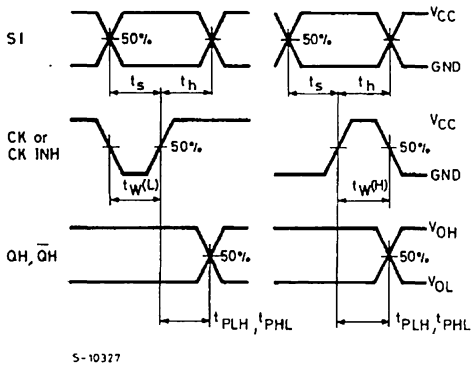
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

TIMING CHART

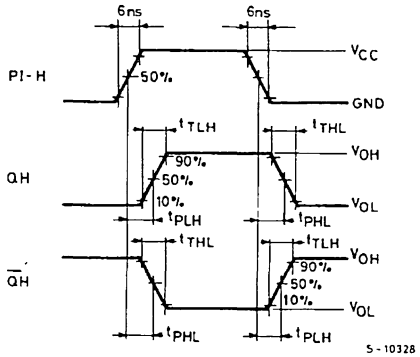


SWITCHING CHARACTERISTICS TEST WAVEFORM

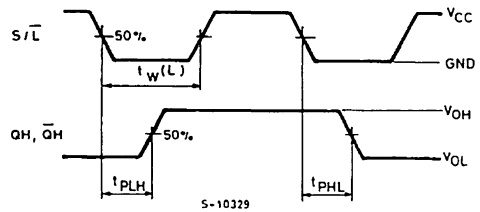
SERIAL MODE



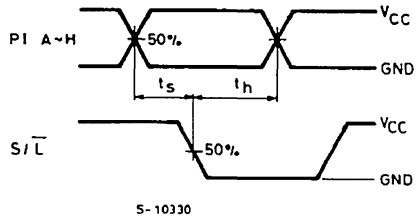
PARALLEL MODE



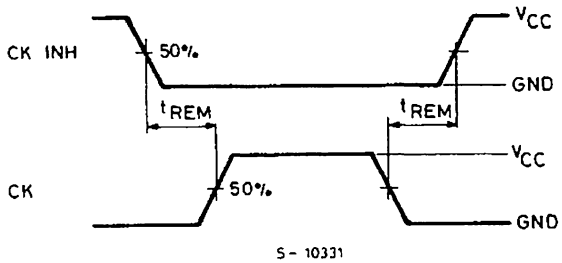
PARALLEL MODE



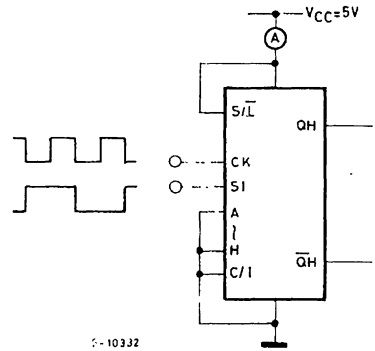
PARALLEL MODE



PARALLEL MODE



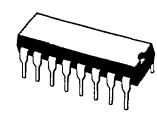
TEST CIRCUIT I_{CC} (Opr.)



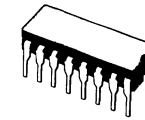
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

8 BIT PISO SHIFT REGISTER

- HIGH SPEED
  t_{PD} = 17 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- SYMMETRICAL OUTPUT IMPEDANCE
  $I_{OL} = |I_{OH}|$ = 4 mA (MIN.)
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2 V (MIN.) V_{IL} = 0.8 V (MAX.)
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS165



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HCT165F1R M74HCT165M1R
M74HCT165B1R M74HCT165C1R

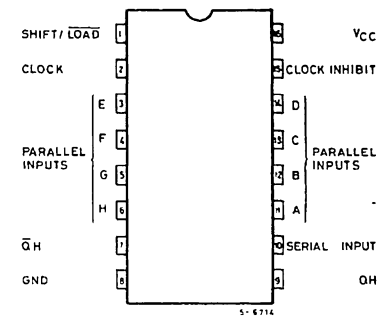
DESCRIPTION

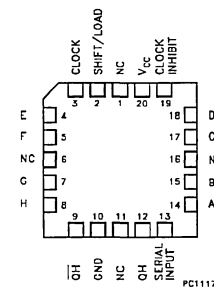
The M54/74HCT165 is a high speed CMOS 8 BIT PISO SHIFT REGISTER fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. It achives the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

This device contains eight clocked master slave RS flip-flops connected as a shift register, with auxiliary gating to provide over-riding asynchronous parallel entry. Parallel data entrens when the shift/load input is low. The parallel data can change while shift/load is low, provided that the recommended set-up and hold times are observed. For clocked operation, shift/load must be high. The two clock input perform identically; one can be used as a clock inhibit by applying a high signal; to permit this operation clocking is accomplished through a 2 input nor gates.

To avoid double clocking, however, the inhibit signal should only go high while the clock is high. Otherwise the rising inhibit signal will cause the same response as rising clock edge. This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSCMOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

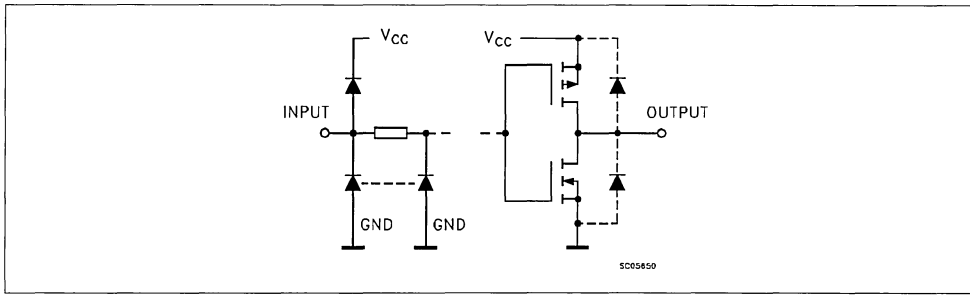
PIN CONNECTIONS (top view)





NC =
No Internal
Connection

INPUT AND OUTPUT EQUIVALENT CIRCUIT

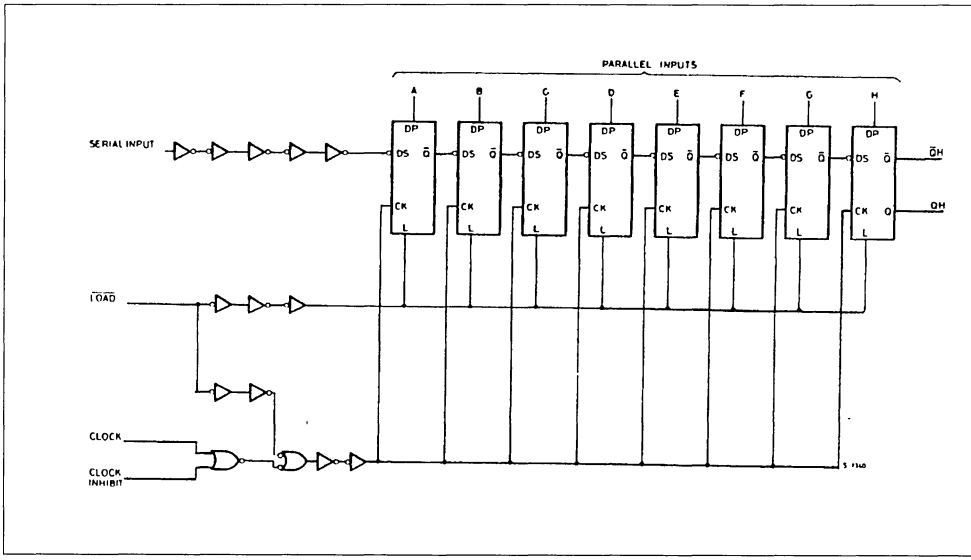


TRUTH TABLE

INPUTS					INTERNAL OUTPUTS		OUTPUS	OUTPUS
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL IN	A .....H	QA	QB	QH	$\overline{QH}$
L	X	X	X	a.....h	a	b	h	$\overline{h}$
H	L	⎍	H	X	H	QAn	QGn	$\overline{QGn}$
H	L	⎍	L	X	L	QAn	QGn	$\overline{QGn}$
H	⎍	L	H	X	H	QAn	QGn	$\overline{QGn}$
H	⎍	L	L	X	L	QAn	QGn	$\overline{QGn}$
H	X	H	X	X	NO CHANGE			
H	H	X	X	X	NO CHANGE			

a..... h: The level of steady input voltage at inputs A through H respectively
QAn - QGn : The level of QA -QG, respectively, before the most-recent transition of the clock.

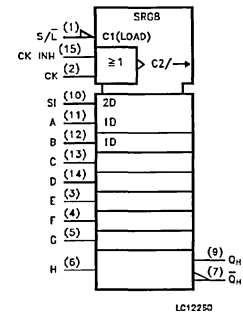
LOGIC DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	$S/\overline{L}$	Asynchronous Parallel Load Input
2	$\overline{QH}$	Complementary Output
7	QH	Serial Output
9	CLOCK	Clock Input (LOW to HIGH edge triggered)
10	SI	Serial Data Input
11, 12, 13, 14, 3, 4, 5, 6	A to H	Parallel Data Inputs
15	CLOCK INH	CLock Inhibit
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

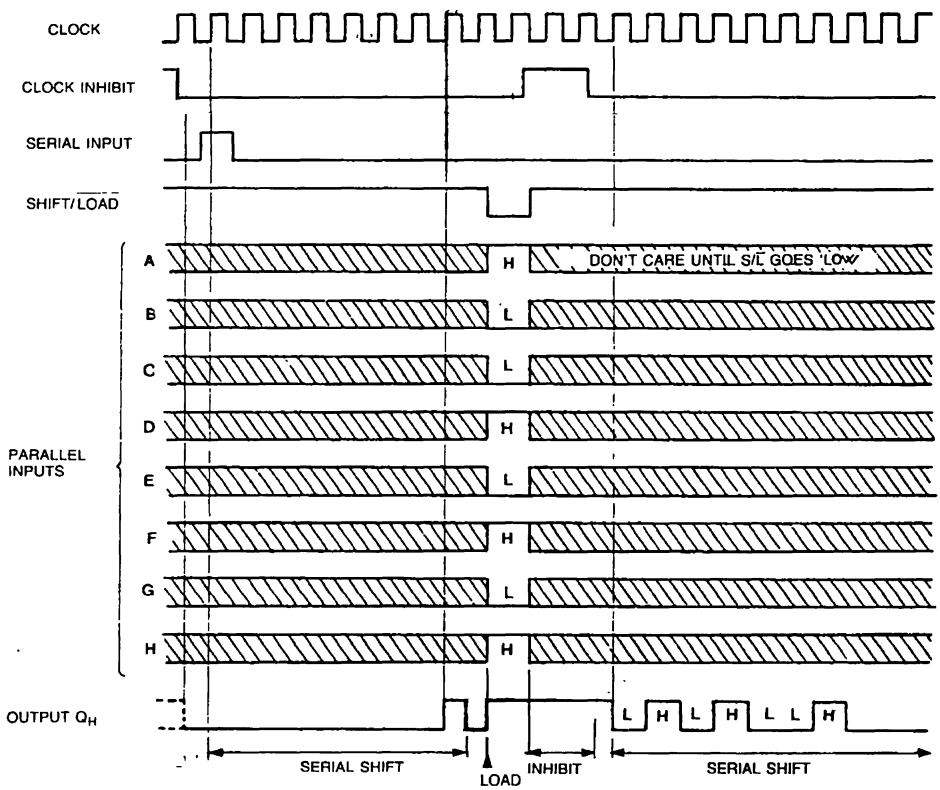
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				4		40		80	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9		3.0	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			8	15		19		22	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CK - QH, $\overline{QH}$)	4.5			24	37		46		56	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CKINH - QH, $\overline{QH}$)	4.5			24	37		46		56	ns
t_{PLH} t_{PHL}	Propagation Delay Time (S/L - QH, $\overline{QH}$)	4.5			26	40		50		60	ns
t_{PLH} t_{PHL}	Propagation Delay Time (H - QH, $\overline{QH}$)	4.5			22	34		43		51	ns
f_{MAX}	Maximum Clock Frequency	4.5		30	46		24				MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CK, CKINH)	4.5			8	15		19		22	ns
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width ($S/\overline{L}$)	4.5			8	15		19			ns
t_s	Minimum Set-up Time (PI - $S/\overline{L}$)	4.5			7	15		19		22	ns
t_s	Minimum Set-up Time (S/L -CK, CHINH)	4.5			7	15		19		22	ns
t_s	Minimum Set-up Time (S -CK, CHINH)	4.5			7	15		19		22	ns
t_h	Minimum Hold Time (PI - $S/\overline{L}$) (S/L -CK, CHINH)	4.5				0		0		0	ns
t_{REM}	Minimum Removal Time (CK - CKINH) (CKINH - CK)	4.5			5	15		19		22	ns
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				96						pF

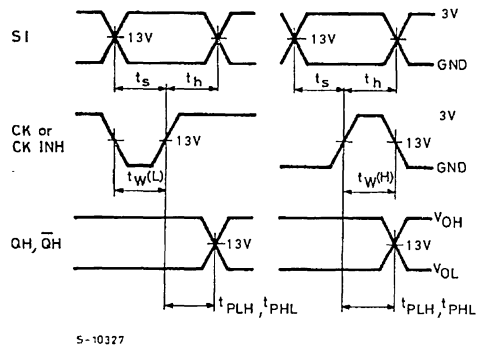
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

TIMING CHART

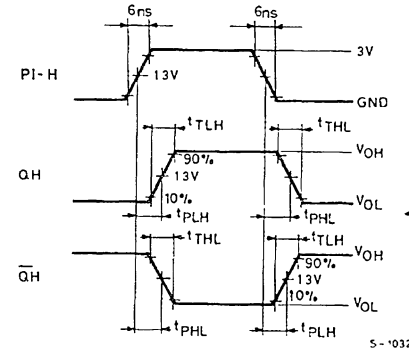


SWITCHING CHARACTERISTICS TEST WAVEFORM

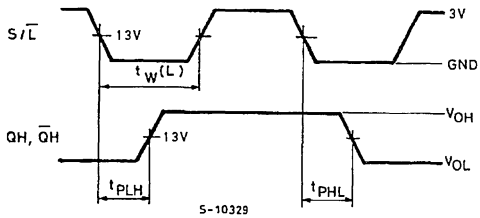
SERIAL MODE



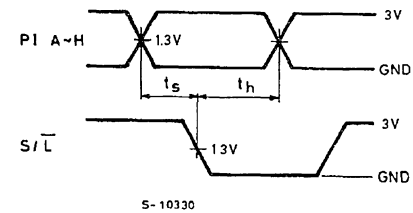
PARALLEL MODE



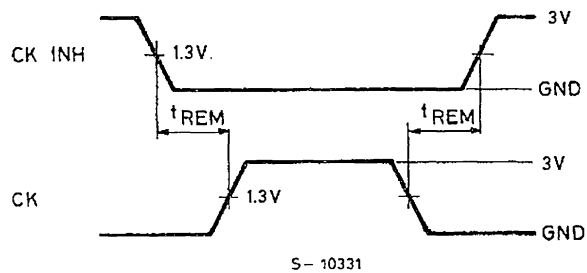
PARALLEL MODE



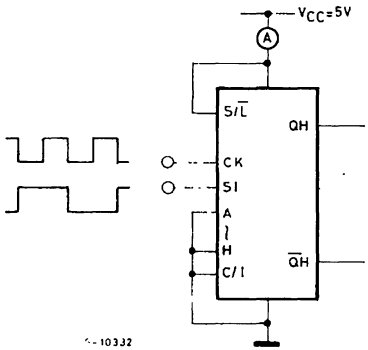
PARALLEL MODE



PARALLEL MODE



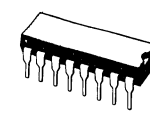
TEST CIRCUIT I_{CC} (Opr.)



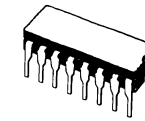
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

8 BIT PISO SHIFT REGISTER

- HIGH SPEED
  f_{MAX} = 57 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS166



B1R
(Plastic Package)



F1R
(Ceramic Package)

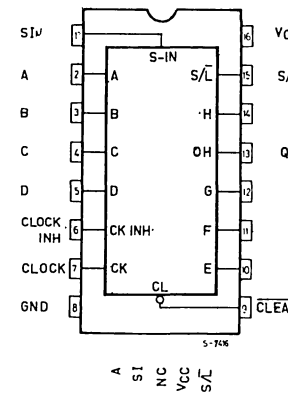
M1R
(Micro Package)

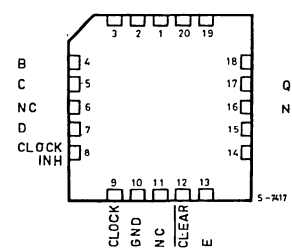
C1R
(Chip Carrier)

ORDER CODES :

M54HC166F1R	M74HC166M1R
M74HC166B1R	M74HC166C1R

PIN CONNECTIONS (top view)





NC = No Internal Con-

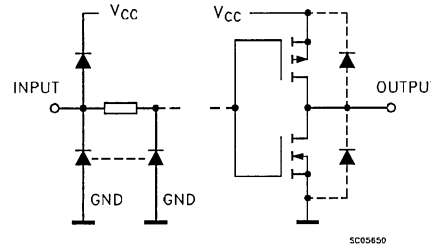
DESCRIPTION

The M54/74HC166 is a high speed C^2MOS 8 BIT PISO SHIFT REGISTER fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

It consists of parallel or serial inputs and a serial-out 8-bit shift register with gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are controlled by the SHIFT/$\overline{LOAD}$ input. When the SHIFT/$\overline{LOAD}$ input is held high, the serial data input is enabled and the eight flip-flops perform serial shifting with each clock pulse. When held low, the parallel data inputs are enabled and synchronous loading occurs on the next clock pulse. Clocking is accomplished on the low-to-high level edge of the clock pulse. The CLOCK-INHIBIT input should be changed to the high only while the CLOCK input is held high. A direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero. Functional details are shown in the truth table and the timing chart.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

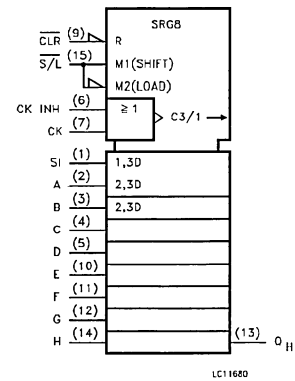
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	SI	Serial Data Inputs
2, 3, 4, 5, 10, 11, 12, 14	A to H	Parallel Data Inputs
6	CK INH	Clock Enable Input (Active LOW)
7	CK	Clock Input (LOW to HIGH edge-triggered)
9	$\overline{CLEAR}$	Asyncronous Master reset Input (Active LOW)
13	Q_H	Serial Output from the Last Stage
15	$S/\overline{L}$	Parallel Enable Input (Active LOW)
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL

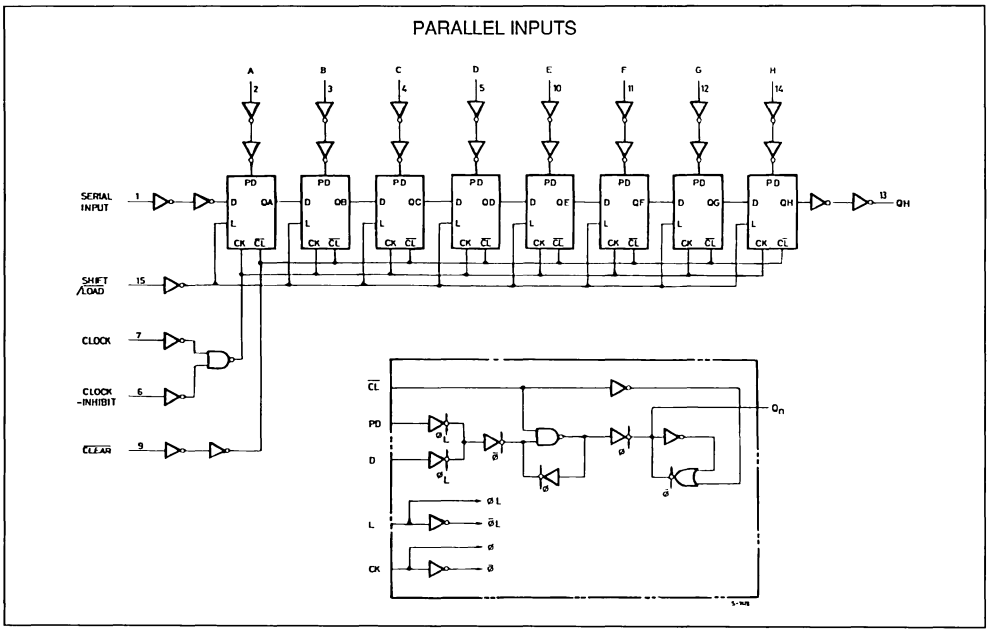


TRUTH TABLE

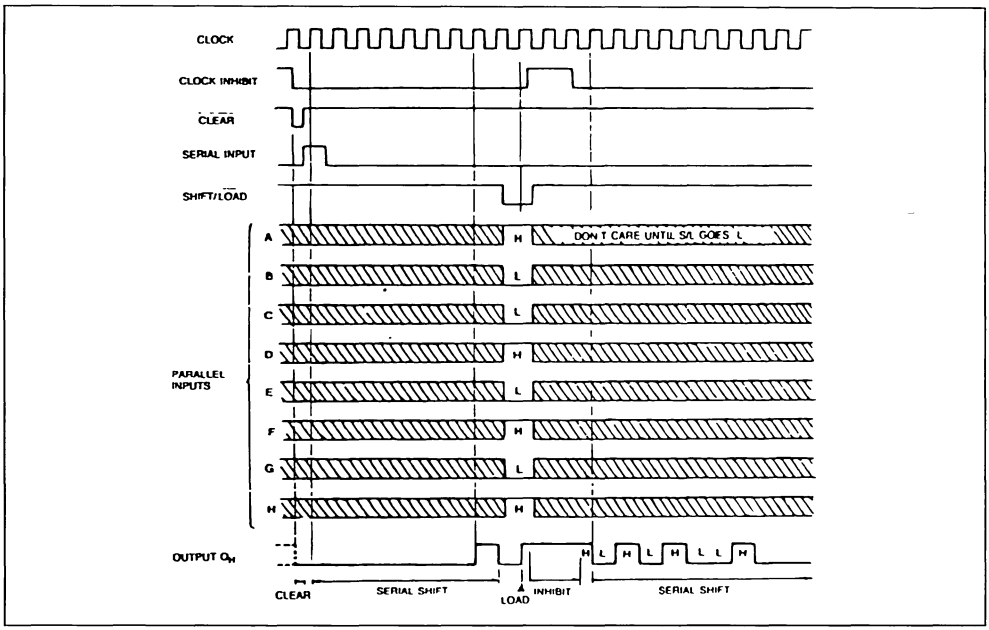
INPUTS						INTERNAL OUTPUTS		OUTPUTS
$\overline{CLEAR}$	SHIFT/$\overline{LOAD}$	CLOCK INH	CLOCK	SERIAL IN	PARALLEL A·····H	QA	QB	QH
L	X	X	X	X	X	L	L	L
L	X	X	⌜	X	X	NO CHANGE		
H	L	L	⌟	X	a·····h	a	b	h
H	H	L	⌟	H	X	H	QAn	QGn
H	H	L	⌟	L	X	L	QAn	QGn
H	X	H	X	X	X	NO CHANGE		

X. Don't Care
a····· h The level of steady state input voltage at inputs a trough H respectively

LOGIC DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

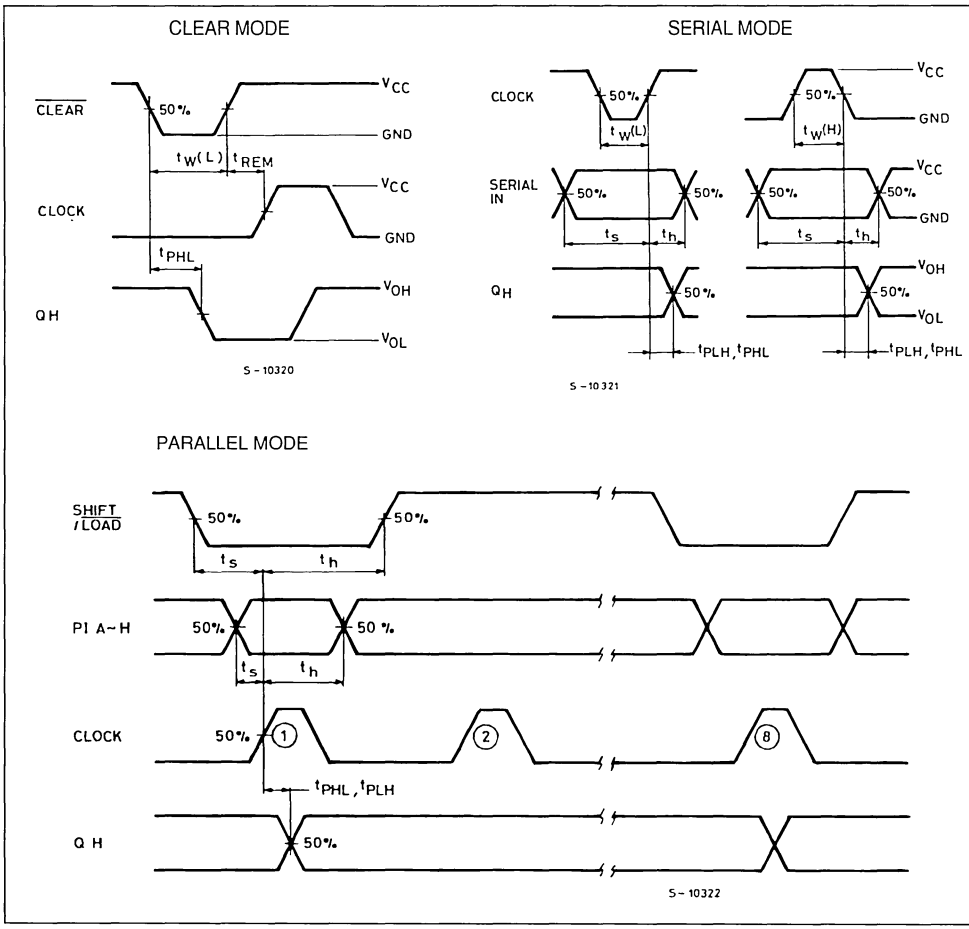
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

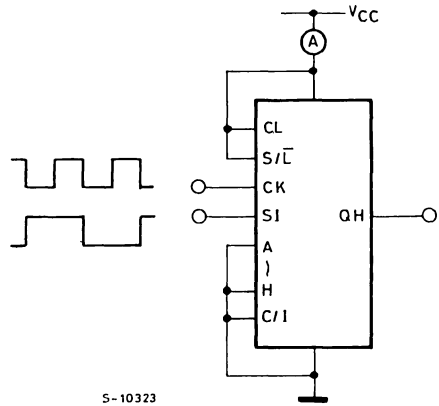
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - QH)	2.0			70	150		190		225	ns
		4.5			20	30		38		45	
		6.0			16	26		32		38	
t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$ - QH)	2.0			60	135		170		205	ns
		4.5			18	27		34		41	
		6.0			14	23		29		35	
f_{MAX}	Maximum Clock Frequency	2.0		6.2	14		5.0		4.2		MHz
		4.5		31	50		25		21		
		6.0		37	63		30		25		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0			28	75		95		110	ns
		4.5			6	15		19		22	
		6.0			5	13		16		19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLEAR}$)	2.0			28	75		95		110	ns
		4.5			6	15		19		22	
		6.0			5	13		16		19	
t_s	Minimum Set-up Time (SI, PI)	2.0			20	75		95		110	ns
		4.5			4	15		19		22	
		6.0			3	13		16		19	
t_s	Minimum Set-up Time ($\overline{S/L}$)	2.0			25	75		95		110	ns
		4.5			5	15		19		22	
		6.0			3	13		16		19	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Minimum Removal Time	2.0			12	50		65		75	ns
		4.5			3	10		13		15	
		6.0			3	9		11		13	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				60						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



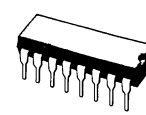
TEST CIRCUIT I_{CC} (Opr.)



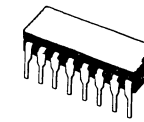
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

QUAD D-TYPE REGISTER (3-STATE)

- HIGH SPEED
  f_{MAX} = 73 MHz (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V to 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS 173



B1R
(Plastic Package)



F1R
(Ceramic Package)

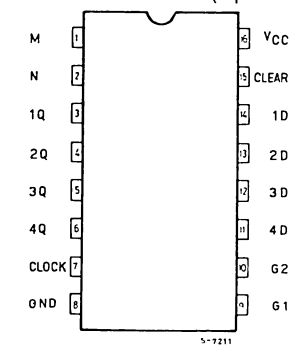
M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HC173F1R M74HC173M1R
M74HC173B1R M74HC173C1R

PIN CONNECTIONS (top view)



NC =
No Internal
Connection

DESCRIPTION

The M54/74HC173 is a high speed CMOS QUAD D-TYPE REGISTER (3-STATE) fabricated in silicon gate C^2MOS technology.

It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This device is composed of a four-bit register including D-type flip-flops and 3-state buffers. The four flip-flops are controlled by a common clock input (CLOCK) and a common reset input (CLEAR). Signals applied to the data inputs (D_1-D_4) are stored at the respective flip-flops on the positive going transition of the clock input, only when both clock control inputs (G_1 and G_2) are held low.

The reset feature is asynchronous and active high. The stored data are provided on each output only when both output control inputs (M and N) are held low, otherwise the outputs go to the high-impedance state.

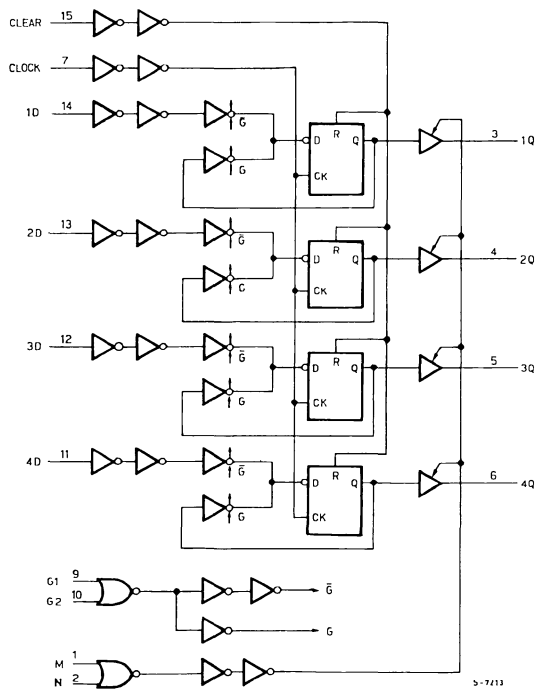
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

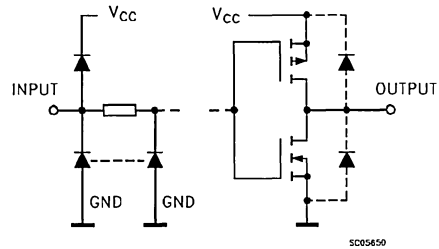
CLEAR	CLOCK	DATA ENABLE		Dn	OUTPUT CONTROL		Qn
		G1	G2		M	N	
X	X	X	X	X	H	X	Z
X	X	X	X	X	X	H	Z
H	X	X	X	X	L	L	L
L	⊓	X	X	X	L	L	Q0
L	⊔	H	X	X	L	L	Q0
L	⊔	X	H	X	L	L	Q0
L	⊔	L	L	H	L	L	H
L	⊔	L	L	L	L	L	L

X Don't Care Z High Impedance

LOGIC DIAGRAM



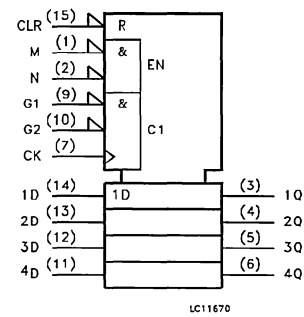
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2	M, N	Output Enable Input (Active LOW)
3, 4, 5, 6	1Q to 4Q	3-State Flip-flop Outputs
7	CLOCK	Clock Input (LOW to HIGH, Edge-triggered)
9, 10	G1, G2	Data Enable Inputs (Active LOW)
14, 13, 12, 11	1D to 4D	Data Inputs
15	CLEAR	Asynchronous Master Reset (Active HIGH)
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series		-55 to +125	°C
	M74HC Series		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 μA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 μA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.37		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.37		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	μA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5.0		±10	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	μA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

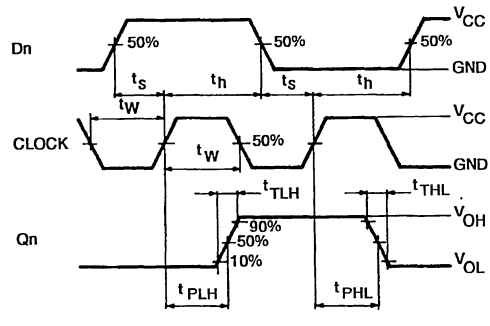
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q)	2.0	50			50	115		145		175	ns
		4.5				14	23		29		35	
		6.0				12	20		25		30	
		2.0	150			65	145		180		220	ns
		4.5				18	29		36		44	
		6.0				15	25		31		37	
t_{PLH} t_{PHL}	Propagation Delay Time (CLEAR - Q)	2.0	50			50	115		145		175	ns
		4.5				14	23		29		35	
		6.0				12	20		25		30	
		2.0	150			65	145		180		220	ns
		4.5				18	29		36		44	
		6.0				15	25		31		37	
f_{MAX}	Maximum Clock Frequency	2.0	50		8.6	20		6.8		5.8		MHz
		4.5			43	67		34		29		
		6.0			51	84		40		34		
t_{PZL} t_{PZH}	Output Enable Time	2.0	50	R_L = 1KΩ		50	115		145		175	ns
		4.5				14	23		29		35	
		6.0				12	20		25		30	
		2.0	150	R_L = 1KΩ		65	145		180		220	ns
		4.5				18	29		36		44	
		6.0				15	25		31		37	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0	50	R_L = 1KΩ		36	105		130		160	ns
		4.5				15	21		26		32	
		6.0				13	18		22		27	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0	50			16	75		95		110	ns
		4.5				4	15		19		22	
		6.0				3	13		16		19	
$t_{W(L)}$	Minimum Pulse Width (CLEAR)	2.0	50			16	75		95		110	ns
		4.5				4	15		19		22	
		6.0				3	13		16		19	
t_s	Minimum Set-up Time (G1, G2)	2.0	50			40	100		125		150	ns
		4.5				10	20		25		30	
		6.0				9	17		21		26	
t_s	Minimum Set-up Time (D)	2.0	50			24	75		95		110	ns
		4.5				6	15		19		22	
		6.0				5	13		16		19	
t_h	Minimum Hold Time (G1, G2, D)	2.0	50				0		0		0	ns
		4.5					0		0		0	
		6.0					0		0		0	

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{REM}	Minimum Removal Time	2.0	50				5		5		5	ns
		4.5					5		5		5	
		6.0					5		5		5	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance					50						pF

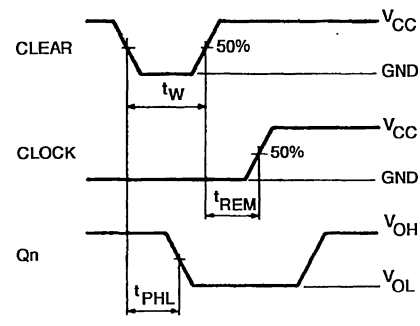
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per circuit)

SWITCHING CHARACTERISTICS TEST WAVEFORM

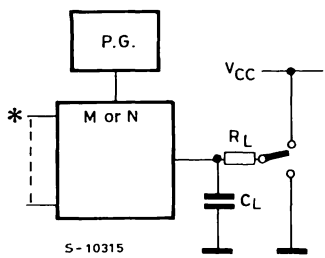


S-10668

CLEAR = "H"

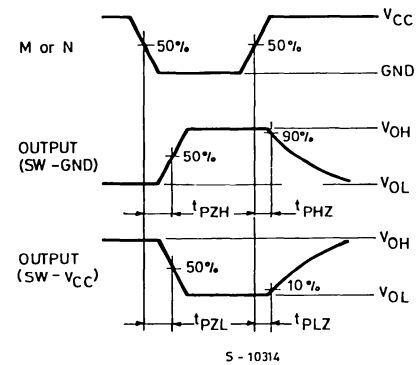


S-10669



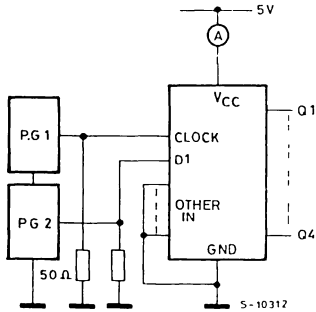
S-10315

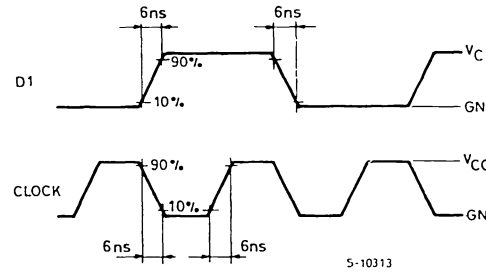
EACH FLIP-FLOP SHALL BE SET HIGH WHEN SWITCH IS CONNECTED TO GND LINE AND IT SHALL BE SET LOW WHEN SWITCH IS



S - 10314

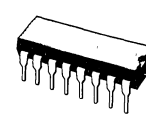
TEST CIRCUIT I_{CC} (Opr.)



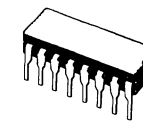


HEX D-TYPE FLIP FLOP WITH CLEAR

- HIGH SPEED
  f_{MAX} = 71 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS174



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

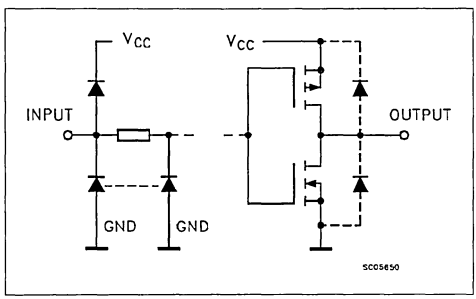
M54HC174F1R M74HC174M1R
M74HC174B1R M74HC174C1R

DESCRIPTION

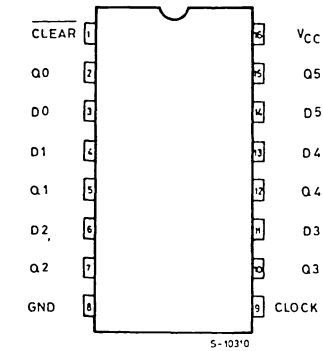
The M54/74HC174 is a high speed CMOS HEX D-TYPE FLIP-FLOP WITH CLEAR fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

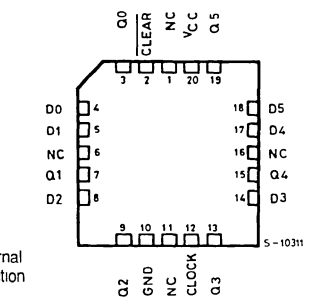
Information signals applied to D inputs are transfered to the Q output on the positive going edge of the clock pulse. When the $\overline{CLEAR}$ input is held low, the Q outputs are held low independently of the other inputs. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





NC =
No Internal
Connection

TRUTH TABLE

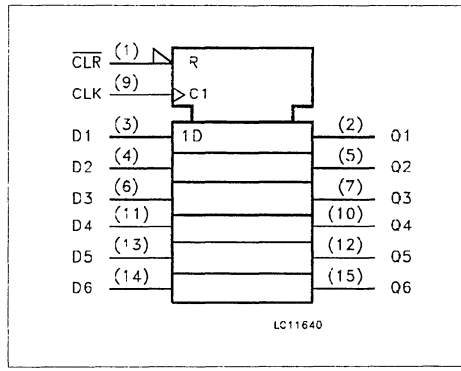
INPUTS			OUTPUTS	FUNCTION
$\overline{CLEAR}$	D	CK	Q	
L	X	X	L	CLEAR
H	L	⌐	L	
H	H	⌐	H	
H	X	¬	Q_n	NO CHANGE

X Don't Care

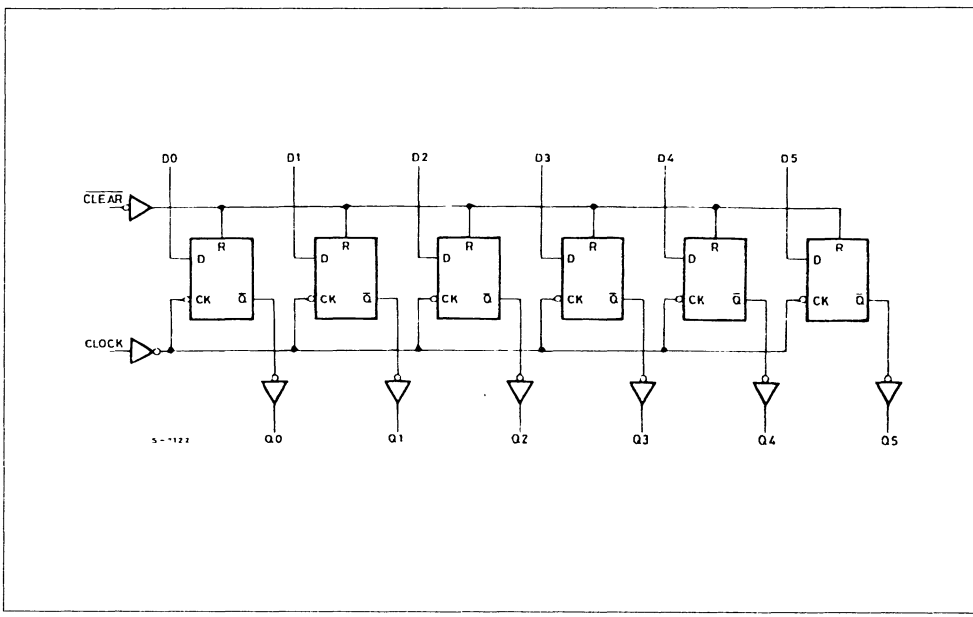
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{CLEAR}$	Asynchronous Master Reset (Active LOW)
2, 5, 7, 10, 12, 15	Q0 to Q5	Flip-flop Outputs
3, 4, 6, 11, 13, 14	D0 to D5	Data Inputs
9	CLOCK	Clock Input (LOW to HIGH, edge triggered)
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

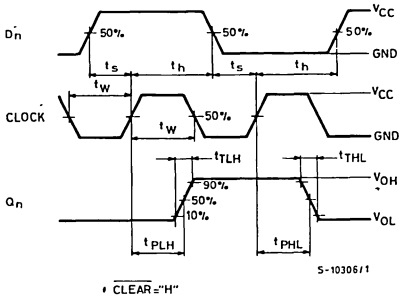
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 μA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 μA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	μA

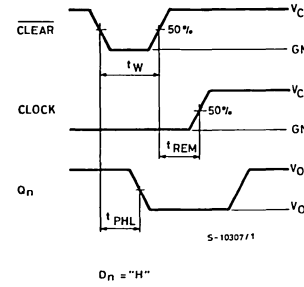
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value						Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CK - Q)	2.0			68	135		170		205	ns
		4.5			17	27		34		41	
		6.0			14	23		29		35	
t_{PHL}	Propagation Delay Time ($\overline{CLR}$ - Q)	2.0			72	145		180		220	ns
		4.5			18	29		36		44	
		6.0			15	25		31		37	
f_{MAX}	Maximum Clock Frequency	2.0		7.2	14		5.8		4.8		MHz
		4.5		36	56		29		24		
		6.0		42	66		34		28		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0			24	75		95		110	ns
		4.5			6	15		19		22	
		6.0			5	13		16		19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLR}$)	2.0			24	75		95		110	ns
		4.5			6	15		19		22	
		6.0			5	13		16		19	
t_s	Minimum Set-up Time	2.0			28	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Minimum Removal Time	2.0			5	5		5		5	ns
		4.5			5	5		5		5	
		6.0			5	5		5		5	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				40						pF

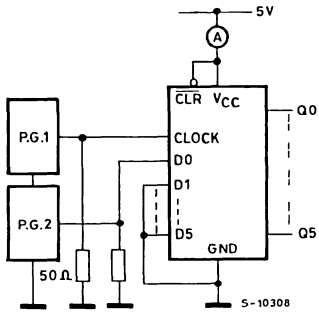
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$ (per FLIP/FLOP)
And the total CPD when N pcs of FLIP FLOP operate can be gained by the following equation: CPD (total)= 38 + 15 x n

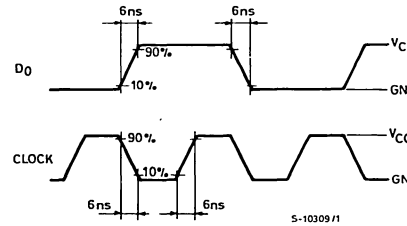
SWITCHING CHARACTERISTICS TEST WAVEFORM





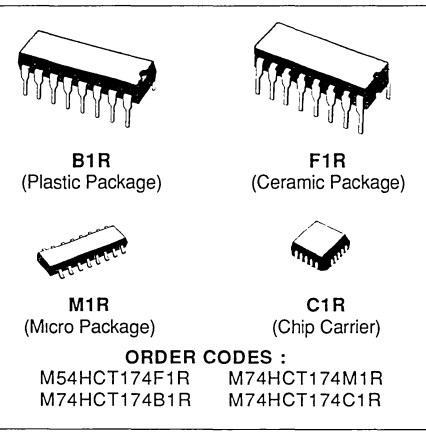
TEST CIRCUIT Icc (Opr.)





HEX D-TYPE FLIP FLOP WITH CLEAR

- HIGH SPEED
  f_{MAX} = 56 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS174



B1R
(Plastic Package)

F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HCT174F1R M74HCT174M1R
M74HCT174B1R M74HCT174C1R

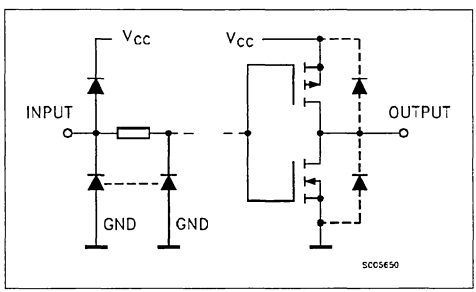
DESCRIPTION

The M54/74HCT174 is a high speed CMOS HEX D-TYPE FLIP-FLOP WITH CLEAR fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

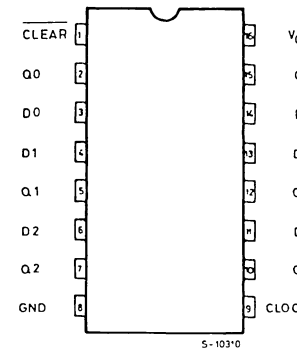
Information signals applied to D inputs are transfered to the Q output on the positive going edge of the clock pulse. When the $\overline{CLEAR}$ input is held low, the Q outputs are held low independently of the other inputs.

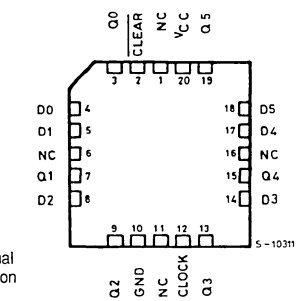
This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





NC =
No Internal
Connection

TRUTH TABLE

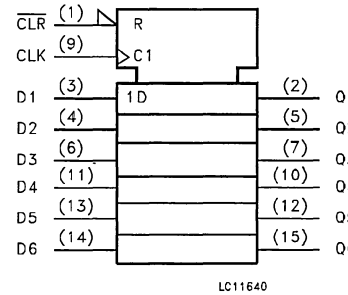
INPUTS			OUTPUTS	FUNCTION
$\overline{CLEAR}$	D	$\overline{CK}$	Q	
L	X	X	L	CLEAR
H	L	⎍	L	
H	H	⎍	H	
H	X	⎏	Q_n	NO CHANGE

X. Don't Care

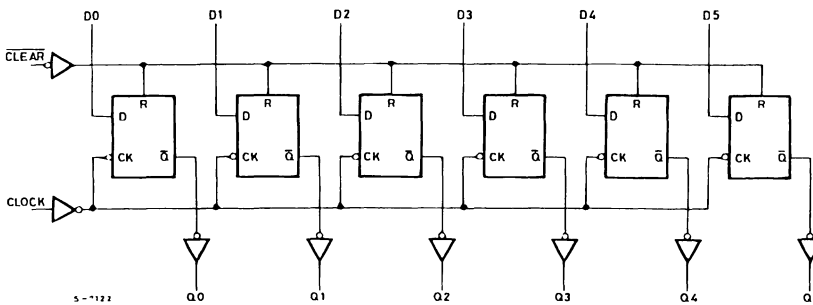
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{CLEAR}$	Asynchronous Master Reset (Active LOW)
2, 5, 7, 10, 12, 15	Q0 to Q5	Flip-flop Outputs
3, 4, 6, 11, 13, 14	D0 to D5	Data Inputs
9	CLOCK	Clock Input (LOW to HIGH, edge triggered)
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW. ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

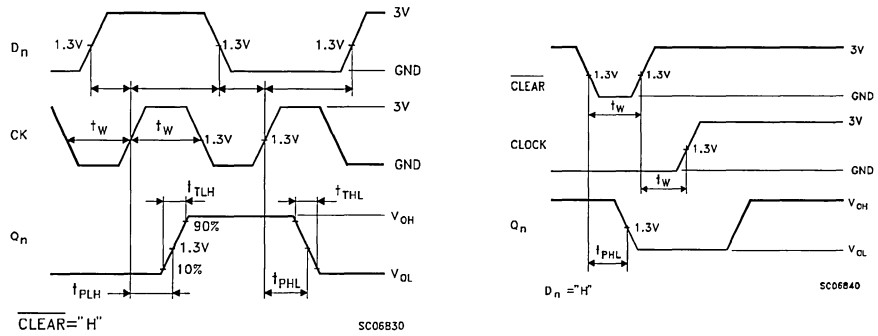
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				4		40		80	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND				2.0		2.9		3.0	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

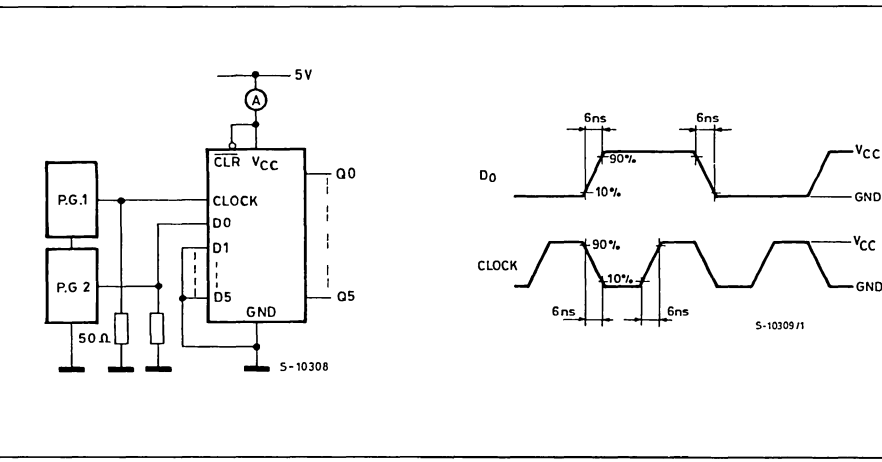
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			8	15		19		22	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CK - Q)	4.5			18	28		35			ns
t_{PHL}	Propagation Delay Time ($\overline{CLR}$ - Q)	4.5			18	28		35		42	ns
f_{MAX}	Maximum Clock Frequency	4.5		30	54		24				MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width ($\overline{CLOCK}$)	4.5			8	15		19		22	ns
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLR}$)	4.5			8	15		19		22	ns
t_s	Minimum Set-up Time	4.5			2	10		13		15	ns
t_h	Minimum Hold Time	4.5				5		6		8	ns
t_{REM}	Minimum Removal Time	4.5			5	5		5		5	ns
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				68						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$ (per FLIP/FLOP)
And the total CPD when N pcs of FLIP FLOP operate can be gained by the following equation: CPD (total)= 38 + 15 x n

SWITCHING CHARACTERISTICS TEST WAVEFORM

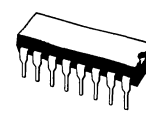


TEST CIRCUIT Icc (Opr.)

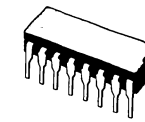


QUAD D-TYPE FLIP-FLOP WITH CLEAR

- HIGH SPEED
  t_{PD} = 13 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS175



B1R
(Plastic Package)



F1R
(Ceramic Package)

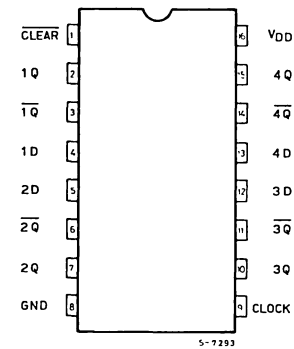
M1R
(Micro Package)

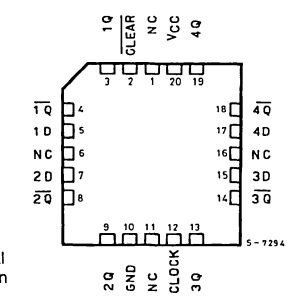
C1R
(Chip Carrier)

ORDER CODES :

M54HC175F1R M74HC175M1R
M74HC175B1R M74HC175C1R

PIN CONNECTIONS (top view)





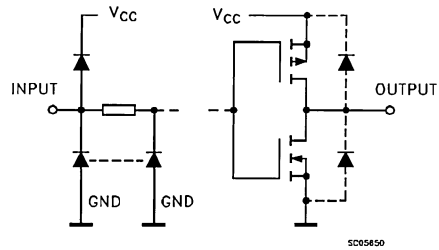
NC =
No Internal
Connection

DESCRIPTION

The M54/74HC175 is a high speed CMOS QUAD D-TYPE FLIP-FLOP WITH CLEAR fabricated in silicon gate CMOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

These four flip-flops are controlled by a clock input (CLOCK) and a clear input (CLEAR). The information data applied to the D inputs (1D to 4D) are transfered to the outputs (1Q to 4Q and $\overline{1Q}$ to $\overline{4Q}$) on the positive-going edge of the clock pulse. The reset function is accomplished when the clear input is taken low and all Q outputs are kept low regardless of other input conditions. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT

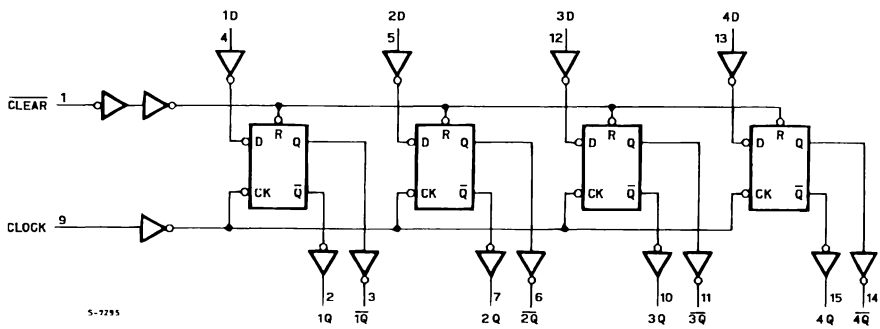


TRUTH TABLE

INPUTS			OUTPUS		FUNCTION
$\overline{CLEAR}$	D	CLOCK	Q	$\overline{Q}$	
L	X	X	L	H	
H	L	⌐	L	H	
H	H	⌐	H	L	
H	X	⌙	Qn	$\overline{Q}$n	NO CHANGE

X: Don't Care

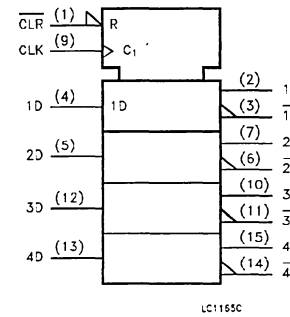
LOGIC DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{CLEAR}$	Master Reset Input (Active LOW)
2, 7, 10, 15	1Q to 4 Q	Flip Flop Outputs
3, 6, 11, 14	$1\overline{Q}$ to $4\overline{Q}$	Complementary Flip Flop Outputs
4, 5, 12, 13	1D to 4D	Data Inputs
9	CLOCK	Clock Input (LOW to HIGH, Edge-triggered)
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur Functional operation under these condition is not implied
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

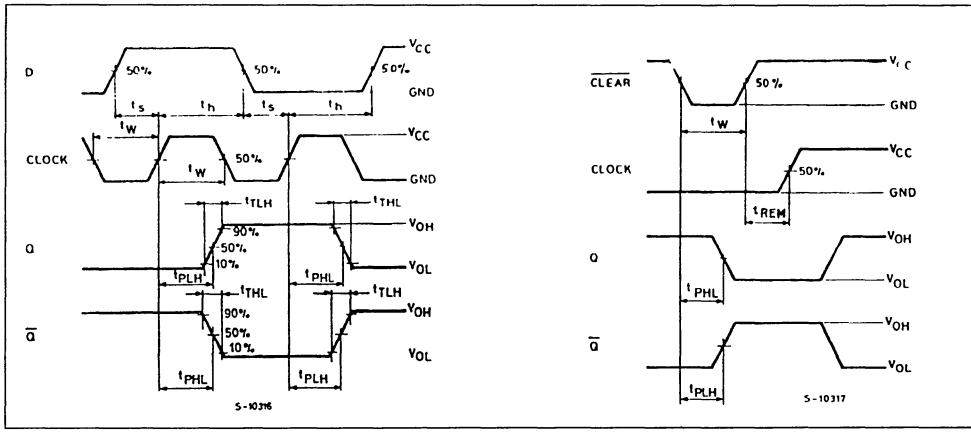
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

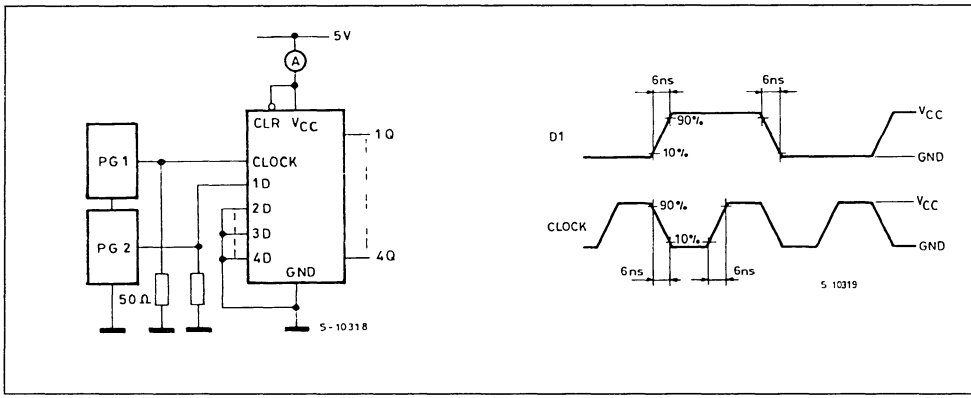
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q, $\overline{Q}$)	2.0			60	150		190		225	ns
		4.5			19	30		38		45	
		6.0			16	26		32		38	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$ - Q, $\overline{Q}$)	2.0			50	125		155		190	ns
		4.5			16	25		31		38	
		6.0			14	21		26		32	
f_{MAX}	Maximum Clock Frequency	2.0		6.2	13		5		4.2		MHz
		4.5		31	52		25		21		
		6.0		37	61		30		25		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width ($\overline{CLOCK}$)	2.0			28	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLEAR}$)	2.0			28	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
t_s	Minimum Set-up Time	2.0			28	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Minimum Removal Time ($\overline{CLEAR}$)	2.0				5		5		5	ns
		4.5				5		5		5	
		6.0				5		5		5	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				47						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Flip Flop)

SWITCHING CHARACTERISTICS TEST WAVEFORM

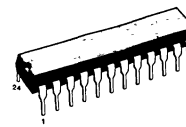


TEST CIRCUIT I_{CC} (Opr.)



ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

- HIGH SPEED
  t_{PD} = 13 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V to 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS181



B1R
(Plastic Package)

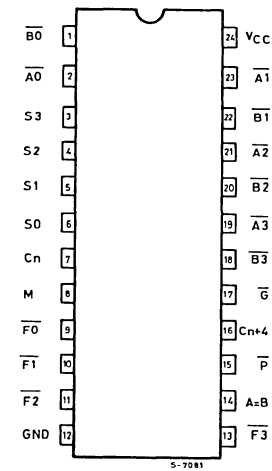
M1R
(Micro Package)

ORDER CODES :
M74HC181M1R M74HC181B1R

DESCRIPTION

The 74HC181 is a high speed CMOS ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR fabricated with silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the M54HC182 or M74HC182, full carry look-ahead circuits, high-speed arithmetic operations can be performed. These circuits will accomodate active-high or active-low data, if the pin designations are interpreted as shown below. Subtraction is accomplished by 1,s complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is 1–B–1, which requires an end-around or forced carry to produce A–B. The 181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs ($\overline{F0}$, $\overline{F1}$, $\overline{F2}$, $\overline{F3}$) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicated equality (A = B). The ALU should be

PIN CONNECTIONS (top view)

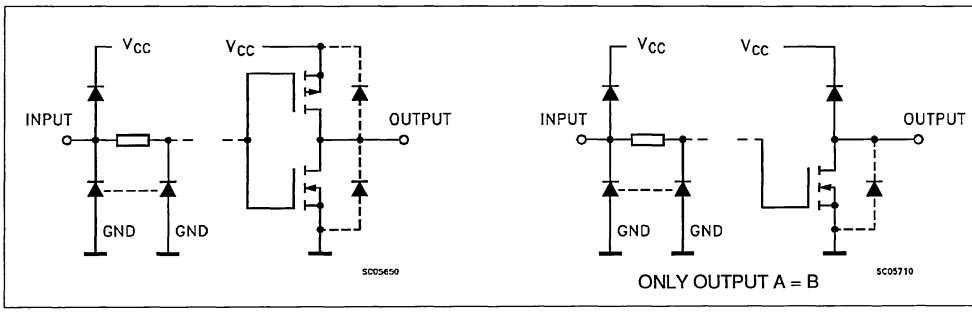


* Open drain Output Structure

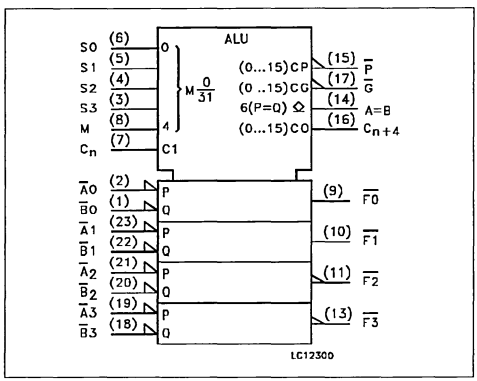
DESCRIPTION (continued)

in the subtract mode with C_n = H when performing this comparison. The A = B output is open-drain so that it can be wire-AND connected to give a comparison for more that four bits. The carry output (Cn + 4) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively. These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUITS



IEC LOGIC SYMBOLS



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
2, 23, 21, 19	$\overline{A0}$ to $\overline{A3}$	Word A Inputs
1, 22, 20, 18	$\overline{B0}$ to $\overline{B3}$	Word B Inputs
6, 5, 4, 3	S0 to S3	Function Select Inputs
7	Cn	Inv. Carry Input
8	M	Mode Control Input
9, 10, 11, 13	$\overline{F0}$ to $\overline{F3}$	Function Outputs
14	A = B	Comparator Output
15	$\overline{P}$	Carry Propagate Output
16	Cn + 4	Inv. Carry Output
17	$\overline{G}$	Carry Generate Output
12	GND	Ground (0V)
24	V_{CC}	Positive Supply Voltage

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
ACTIVE LOW DATA (Table 1)	$\overline{A0}$	$\overline{B0}$	$\overline{A1}$	$\overline{B1}$	$\overline{A2}$	$\overline{B2}$	$\overline{A3}$	$\overline{B3}$	$\overline{F0}$	$\overline{F1}$	$\overline{F2}$	$\overline{F3}$	Cn	Cn + 4	$\overline{P}$	$\overline{G}$
ACTIVE HIGH DATA (Table 1)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	Cn	Cn + 4	X	Y

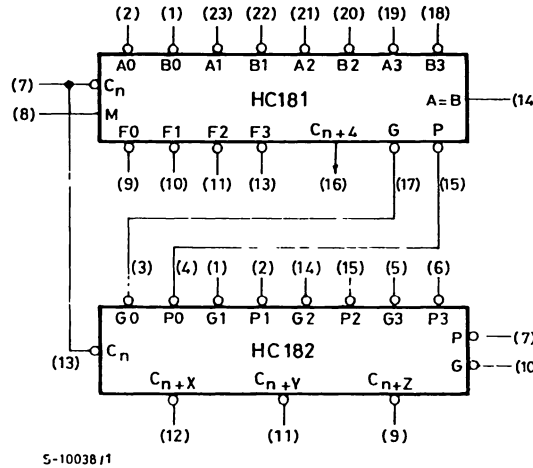
Input Cn	Output Cn + 4	Active LOW Data (Figure 1)	Active HIGH Data (Figure 2)
H	H	A ≥ B	A ≤ B
H	L	A < B	A > B
L	H	A > B	A < B
L	L	A ≤ B	A ≥ B

TRUTH TABLE 1

Selection				ACTIVE LOW DATA		
				M = H Logic Functions	M = L: Arithmetic Operations	
S3	S2	S1	S0		Cn = L (no carry)	Cn = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A Minus 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB Minus 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ Minus 1	F = (A$\overline{B}$)
L	L	H	H	F = 1	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	F = $\overline{A + B}$	F = A Plus (A + $\overline{B}$)	F = A Plus (A + $\overline{B}$) Plus 1
L	H	L	H	F = $\overline{B}$	F = AB Plus (A + B)	F = AB Plus (A + $\overline{B}$) Plus 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
H	L	L	L	F = $\overline{AB}$	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H	L	L	H	F = A $\oplus$ B	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = A$\overline{B}$ Plus (A + B)	F = A$\overline{B}$ Plus (A + B) Plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) Plus 1
H	H	L	L	F = 0	F = A Plus A *	F = A Plus A Plus 1
H	H	L	H	F = A$\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = AB	F = A$\overline{B}$ Plus A	F = A$\overline{B}$ Plus A Plus 1
H	H	H	H	F = A	F = A	F = A Plus 1

* Each bit is shifted to the next more significant position.

FIGURE 1

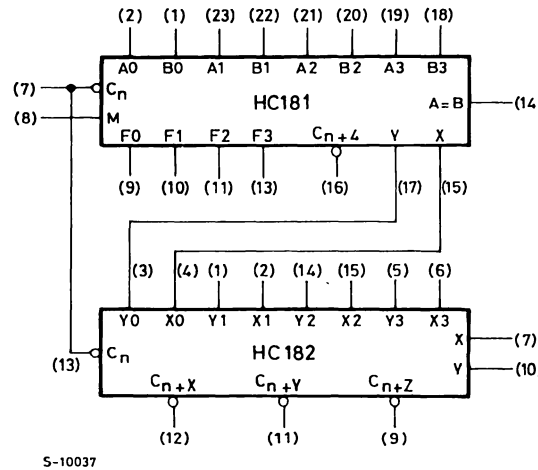


TRUTH TABLE 2

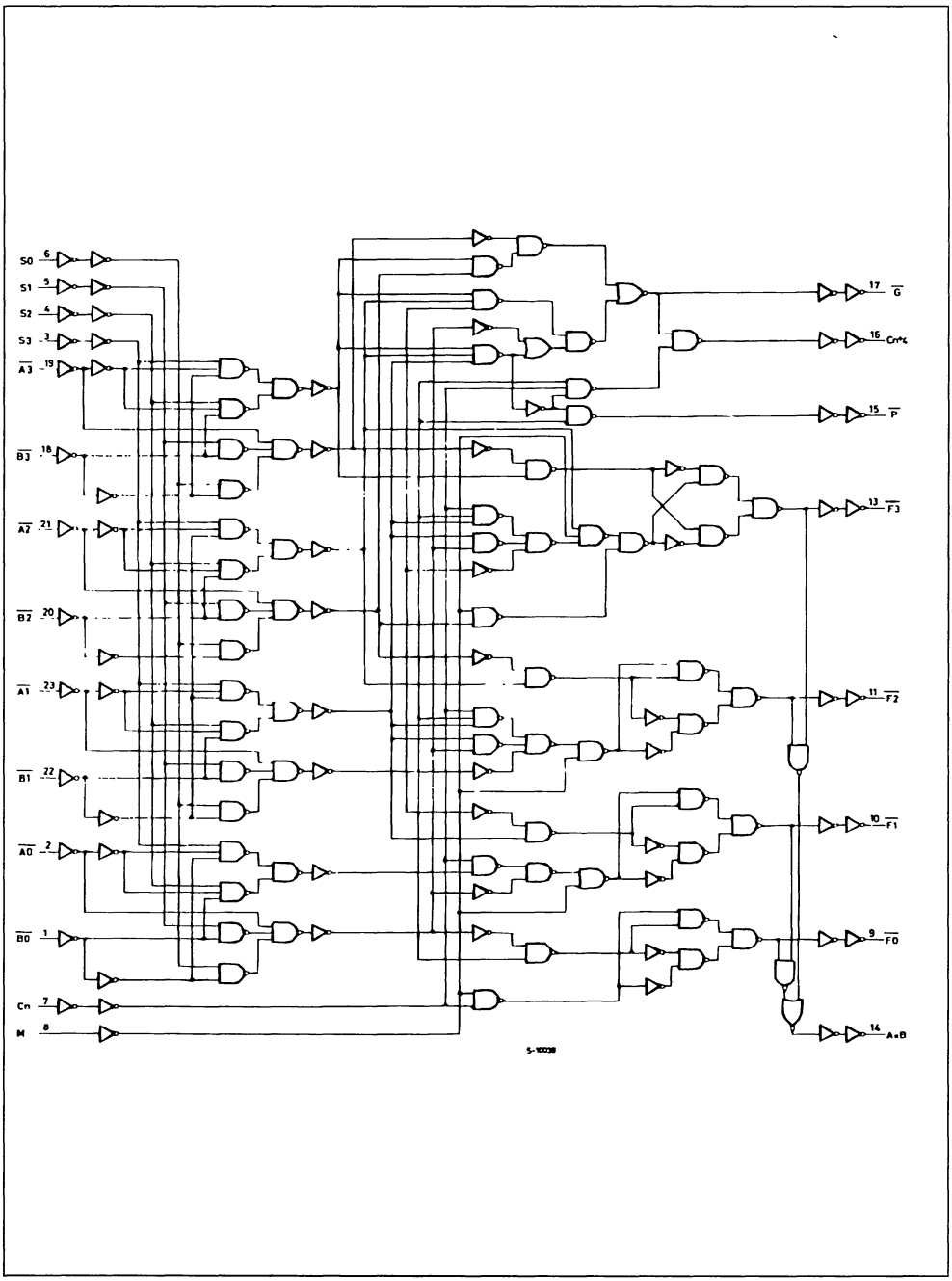
Selection				ACTIVE HIGH DATA		
				M = H Logic Functions	M = L: Arithmetic Operations	
S3	S2	S1	S0		Cn = H (no carry)	Cn = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A Plus 1
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A + B) Plus 1
L	L	H	L	F = $\overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
L	L	H	H	F = 0	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	F = $\overline{AB}$	F = A Plus (A$\overline{B}$)	F = A Plus A$\overline{B}$ Plus 1
L	H	L	H	F = $\overline{B}$	F = (A + B) Plus A$\overline{B}$	F = (A + B) Plus (A$\overline{B}$) Plus 1
L	H	H	L	F = A ⊕ B	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A Plus AB	F = A Plus AB Plus 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) Plus AB	F = (A + $\overline{B}$) Plus AB Plus 1
H	L	H	H	F = AB	F = AB Minus 1	F = AB
H	H	L	L	F = 1	F = A Plus A *	F = A Plus A Plus 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) Plus A	F = (A + B) Plus A Plus 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) Plus A	F = (A + $\overline{B}$) Plus A Plus 1
H	H	H	H	F = A	F = A Minus 1	F = A

* Each bit is shifted to the next more significant position.

FIGURE 2



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value					Unit
		V_{CC} (V)			T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		V
		4.5			3.15			3.15		
		6.0			4.2			4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5	V
		4.5					1.35		1.35	
		6.0					1.8		1.8	
V_{OH}	High Level Output Voltage (except A = B output)	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		V
		4.5			4.4	4.5		4.4		
		6.0			5.9	6.0		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1	V
		4.5				0.0	0.1		0.1	
		6.0				0.0	0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

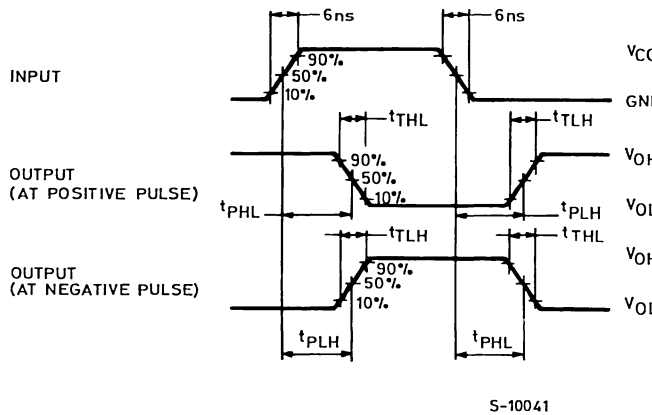
Symbol	Parameter	Test Conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		
				Min.	Typ.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
t_{PLH} t_{PHL}	Propagation Delay Time (1)	2.0			54	120		150	ns
		4.5			16	24		30	
		6.0			13	20		26	
t_{PLH} t_{PHL}	Propagation Delay Time (2)	2.0			90	215		270	ns
		4.5			26	43		54	
		6.0			20	37		46	
t_{PLH} t_{PHL}	Propagation Delay Time (3)	2.0			97	215		270	ns
		4.5			27	43		54	
		6.0			21	37		46	
t_{PLH} t_{PHL}	Propagation Delay Time (4)	2.0			80	180		225	ns
		4.5			23	36		45	
		6.0			18	31		38	
t_{PLH} t_{PHL}	Propagation Delay Time (5)	2.0			81	190		240	ns
		4.5			24	38		48	
		6.0			19	32		41	
t_{PLH} t_{PHL}	Propagation Delay Time (6)	2.0			80	180		225	ns
		4.5			23	36		45	
		6.0			18	31		38	
t_{PLH} t_{PHL}	Propagation Delay Time (7)	2.0			80	170		215	ns
		4.5			23	34		43	
		6.0			18	29		37	
t_{PLH} t_{PHL}	Propagation Delay Time (8)	2.0			80	170		215	ns
		4.5			23	34		43	
		6.0			18	29		37	
t_{PLH} t_{PHL}	Propagation Delay Time (9)	2.0			95	220		275	ns
		4.5			27	44		55	
		6.0			21	37		47	
t_{PLH} t_{PHL}	Propagation Delay Time (10)	2.0			95	220		275	ns
		4.5			27	44		55	
		6.0			21	37		47	
t_{PLH} t_{PHL}	Propagation Delay Time (11)	2.0			86	200		250	ns
		4.5			24	40		50	
		6.0			18	34		43	
t_{PLZ} t_{PZL}	Propagation Delay Time (12)	2.0	R_L = 1kΩ		92	210		265	ns
		4.5			27	42		53	
		6.0			27	36		45	
C_{IN}	Input Capacitance				5	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				195				pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

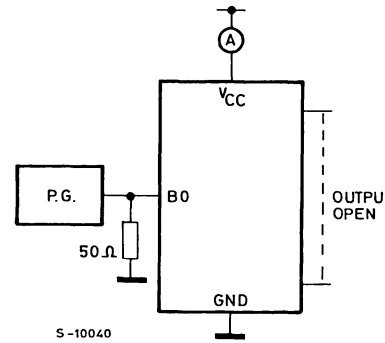
PROPAGATION DELAY TIME TEST CONDITIONS

Test No	INPUT	OUTPUT	Test Conditions
(1)	Cn	Cn + 4	
(2)	Any $\overline{A}$ or $\overline{B}$	Cn + 4	M = GND, S0 = S3 = V_{CC}, S1 = S2 GND ($\overline{SUM}$ mode)
(3)	Any $\overline{A}$ or $\overline{B}$	Cn + 4	M = GND, S0 = S3 = GND, S1 = S2 V_{CC} ($\overline{DIFF}$ mode)
(4)	$\overline{Cn}$	Any $\overline{F}$	M = GND ($\overline{SUM}$ or $\overline{DIFF}$ mode)
(5)	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = GND, S0 = S3 = V_{CC}, S1 = S2 GND ($\overline{SUM}$ mode)
(6)	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = GND, S0 = S3 = GND, S1 = S2 V_{CC} ($\overline{DIFF}$ mode)
(7)	Any $\overline{A}$ or $\overline{B}$	$\overline{F}$	M = GND, S0 = S3 = V_{CC}, S1 = S2 GND ($\overline{SUM}$ mode)
(8)	Any $\overline{A}$ or $\overline{B}$	$\overline{F}$	M = GND, S0 = S3 = GND, S1 = S2 V_{CC} ($\overline{DIFF}$ mode)
(9)	$\overline{Ai}$ or $\overline{Bi}$	$\overline{Fi}$	M = GND, S0 = S3 = V_{CC}, S1 = S2 GND ($\overline{SUM}$ mode)
(10)	$\overline{Ai}$ or $\overline{Bi}$	$\overline{Fi}$	M = GND, S0 = S3 = GND, S1 = S2 V_{CC} ($\overline{DIFF}$ mode)
(11)	$\overline{Ai}$ or $\overline{Bi}$	Fi	M = V_{CC} (Logic mode)
(12)	Any $\overline{A}$ or $\overline{B}$	A = B	M = GND, S0 = S3 = GND, S1 = S2 V_{CC} ($\overline{DIFF}$ mode)

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



Input Condition :

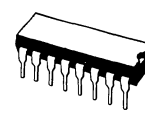
$\overline{A0}$, $\overline{A1}$, $\overline{A2}$, $\overline{A3}$, S0, S3, Cn = V_{DD}

$\overline{B1}$, $\overline{B2}$, $\overline{B3}$, S1, S2, M = GND

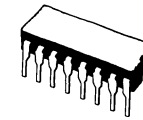
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

FUNCTION LOOK AHEAD CARRY GENERATOR

- HIGH SPEED
  t_{PD} = 14 ns (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V to 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS182



B1R
(Plastic Package)



F1R
(Ceramic Package)

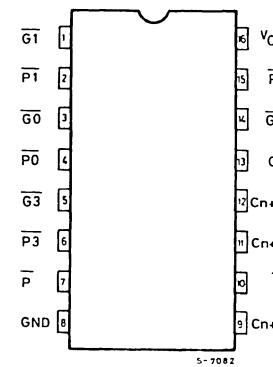
M1R
(Micro Package)

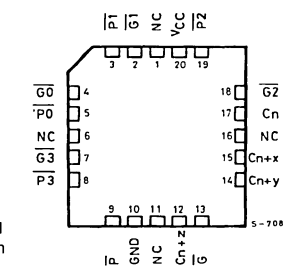
C1R
(Chip Carrier)

ORDER CODES :

M54HC182F1R M74HC182M1R
M74HC182B1R M74HC182C1R

PIN CONNECTIONS (top view)





NC =
No Internal
Connection

DESCRIPTION

The M54/74HC182 is a high speed CMOS FUNCTION LOOK AHEAD CARRY GENERATOR fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. These circuit are capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin connection table. When used in conjunction with the HC181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each HC182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALUs are in their true form, and the carry propagate (P) and carry generate (G) are in negated form ; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretation of carry functions as explained on the HC181 data sheet are also applicable to and compatible with the look-ahead generator. All inputs are equipped with

FUNCTION TABLES

FOR $\overline{G}$ OUTPUT

INPUTS							OUTPUT
$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
ALL OTHER COMBINATIONS							H

FOR $\overline{P}$ OUTPUT

INPUTS				OUTPUT
$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	$\overline{P}$
L	L	L	L	L
ALL OTHER COMBINATIONS				H

FOR Cn+x OUTPUT

INPUTS			OUTPUT
$\overline{G0}$	$\overline{P0}$	Cn	Cn+x
L	X	X	H
X	L	H	H
ALL OTHER COMBINATIONS			L

FOR Cn+y OUTPUT

INPUTS					OUTPUT
$\overline{G1}$	$\overline{G0}$	$\overline{P1}$	$\overline{P0}$	Cn	Cn+y
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
ALL OTHER COMBINATIONS					L

FOR Cn+z OUTPUT

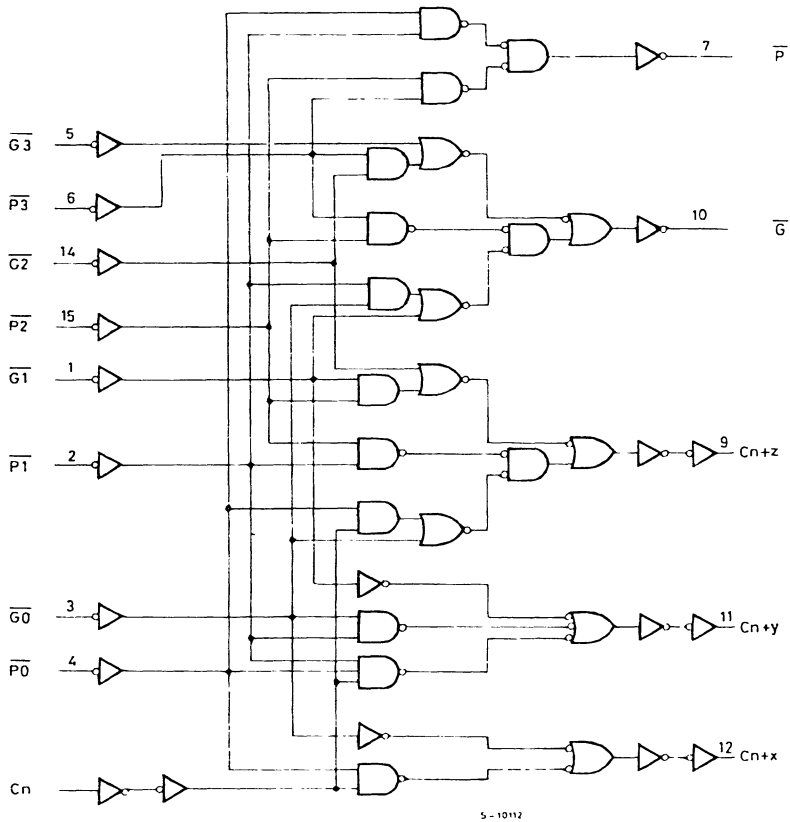
INPUTS							OUTPUT
$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	Cn	Cn+z
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
ALL OTHER COMBINATIONS							L

$Cn+x = G0 + P0Cn$
$Cn+y = G1 + P1G0 + P1P0Cn$
$Cn+z = G2 + P2G1 + P2P1G0 + P2P1P0Cn$
$G = \overline{G3 + G3 + P3G2 + P3P2G1 + P3P2P1G0}$
$P = P3P2P1P0$

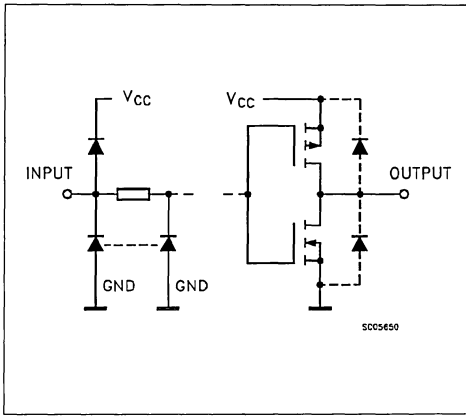
or

$\overline{Cn+x} = \overline{Y0 + (X0 + Cn)}$
$\overline{Cn+y} = \overline{Y1 + [X1 + Y0(X0 + Cn)]}$
$\overline{Cn+z} = \overline{Y2 + \{X2 + Y1[X1 + Y0(X0 + Cn)]\}}$
$G = Y3 + (X3 + Y2)(X3 + X2 + Y1)(X3 + X2 + X1 + Y0)$
$P = X3 + X2 + X1 + X0$

LOGIC DIAGRAM



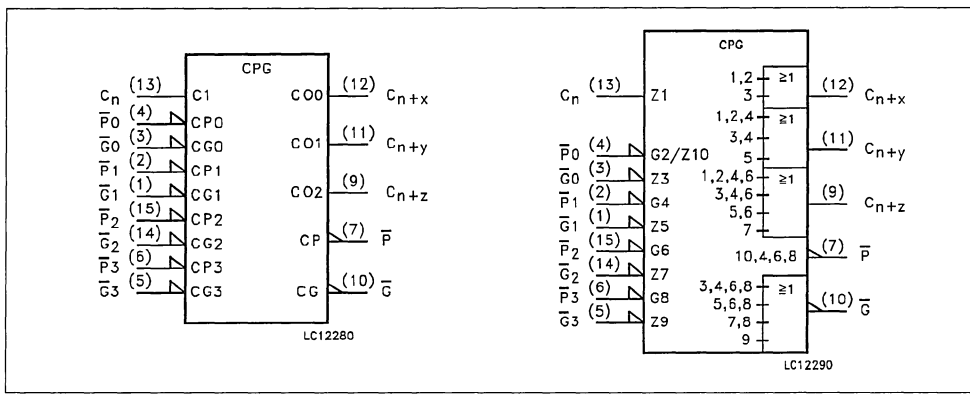
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
3, 1, 14, 5	G0 to G3	Carry Generate Inputs (Active LOW)
4, 2, 15, 6	P0 to P3	Carry Propagate Inputs (Active LOW)
7	P	Carry Propagate Output (Active LOW)
9	Cn+z	Function Output
10	G	Carry Generate Output (Active LOW)
11	Cn+y	Function Output
12	Cn+x	Function Output
13	Cn	
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

IEC LOGIC SYMBOLS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series		-55 to +125	°C
	M74HC Series		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

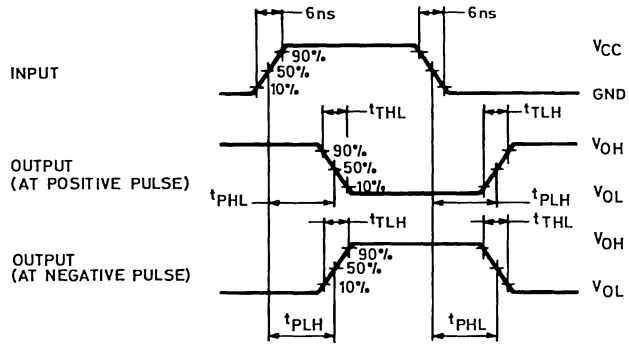
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.37		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.37		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5.0		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

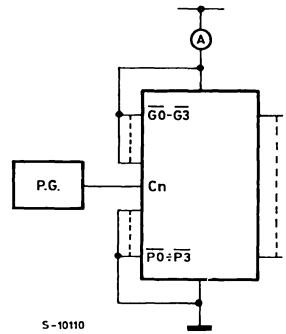
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{Gn}$, $\overline{Pn}$ - Cn+xyz)	2.0			62	135		170		205	ns
		4.5			17	27		34		41	
		6.0			13	23		29		35	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{Gn}$, $\overline{Pn}$ - G)	2.0			72	150		190		225	ns
		4.5			19	30		38		45	
		6.0			14	26		32		38	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{Pn}$ - P)	2.0			62	135		170		205	ns
		4.5			17	27		34		41	
		6.0			13	23		29		35	
t_{PLH} t_{PHL}	Propagation Delay Time (Cn - Cn+xyz)	2.0			62	135		170		205	ns
		4.5			17	27		34		41	
		6.0			13	23		29		35	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				61						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit) Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per FLIP/FLOP)

SWITCHING CHARACTERISTICS TEST WAVEFORM

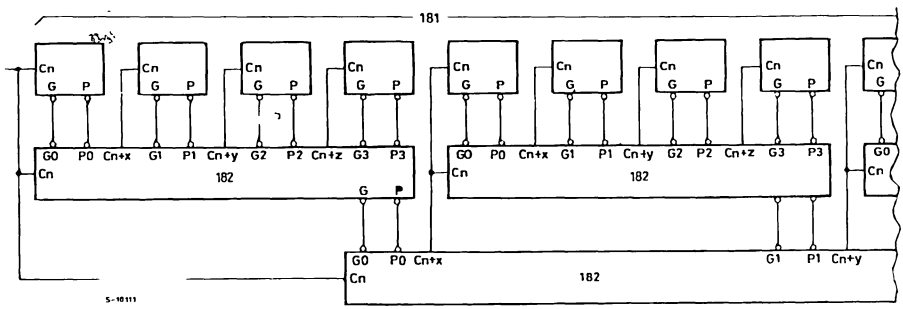


TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TYPICAL APPLICATION

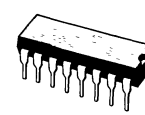


64-BIT ALU, FULL-CARRY LOOK-AHEAD IN THREE LEVELS.

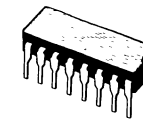
M54/M74HC190
M54/M74HC191

4 BIT SYNCHRONOUS UP/DOWN COUNTERS

- HIGH SPEED
  f_{MAX} = 48 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS190/191



B1R
(Plastic Package)



F1R
(Ceramic Package)

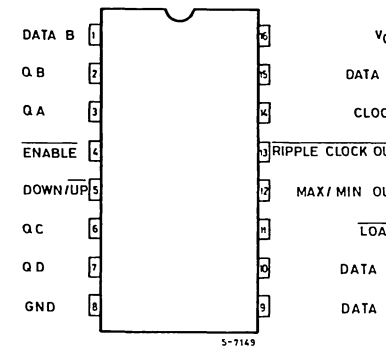
M1R
(Micro Package)

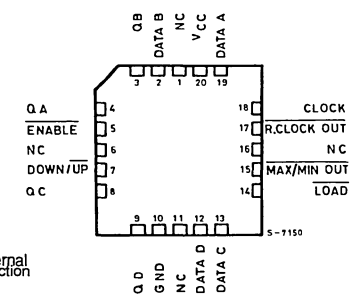
C1R
(Chip Carrier)

ORDER CODES :

M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

PIN CONNECTIONS (top view)





DESCRIPTION

The M54/74HC190/191 are high speed CMOS 4-BIT SYNCHRONOUS UP/DOWN COUNTERS fabricated in silicon gate C^2MOS technology.

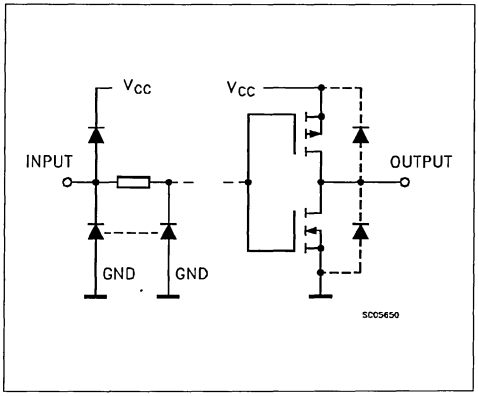
They have the same high speed performance of LSTTL combined with true CMOS low power consumption.

State changes of the counter are synchronous with the LOW-to-HIGH transition of the Clock Pulse input.

An asynchronous parallel load input overrides counting and loads the data present on the DATA inputs into the flip-flops, which makes it possible to use the circuits as programmable counters. A count enable input serves as the carry/borrow input in multi-stage counters. Control input, Down/Up, determines whether a circuit counts up or down. A MAX/MIN output and a Ripple Clock output provide overflow/underflow indication and make possible a variety of methods for generating carry/borrow signals in multi-stage counter applications.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

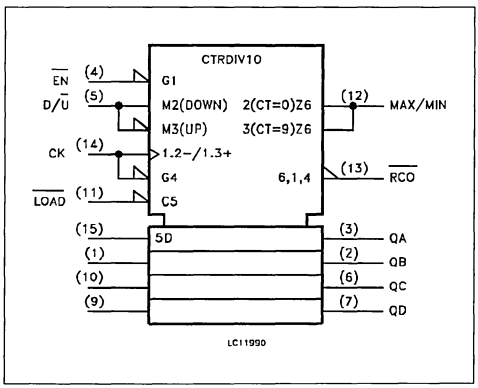
INPUT AND OUTPUT EQUIVALENT CIRCUIT



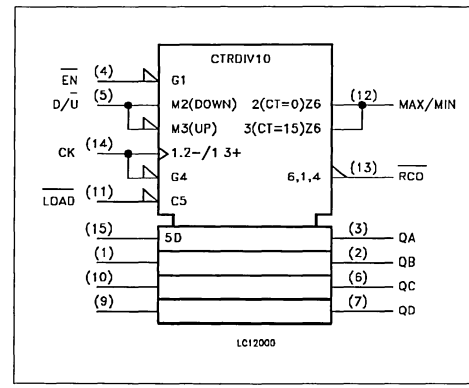
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	QA to QD	Flip-Flop Outputs
4	$\overline{ENABLE}$	Count Enable Input (Active LOW)
5	$\overline{U}$/D	Parallel Data Input
11	LOAD	Load Input (Active LOW)
12	MA/MI OUT	Terminal Count Output
13	$\overline{RC}$	Ripple Clock Output (Active LOW)
14	CLOCK	Cloack Input (LOW to HIGH, Edge-triggered)
15, 1, 10, 9	DA to DD	Data Inputs
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

IEC LOGIC SYMBOL (HC190)



IEC LOGIC SYMBOL (HC191)

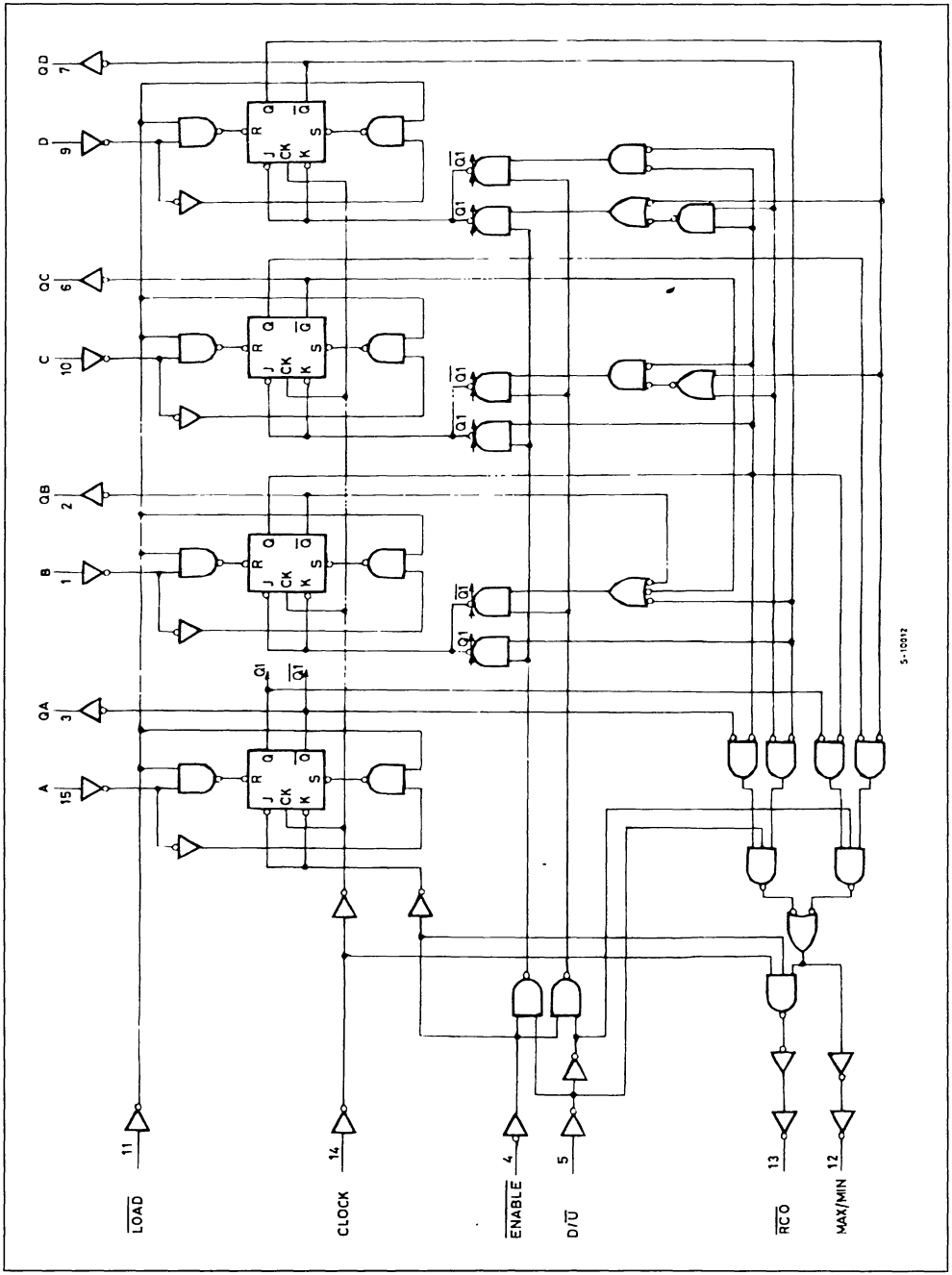


TRUTH TABLE

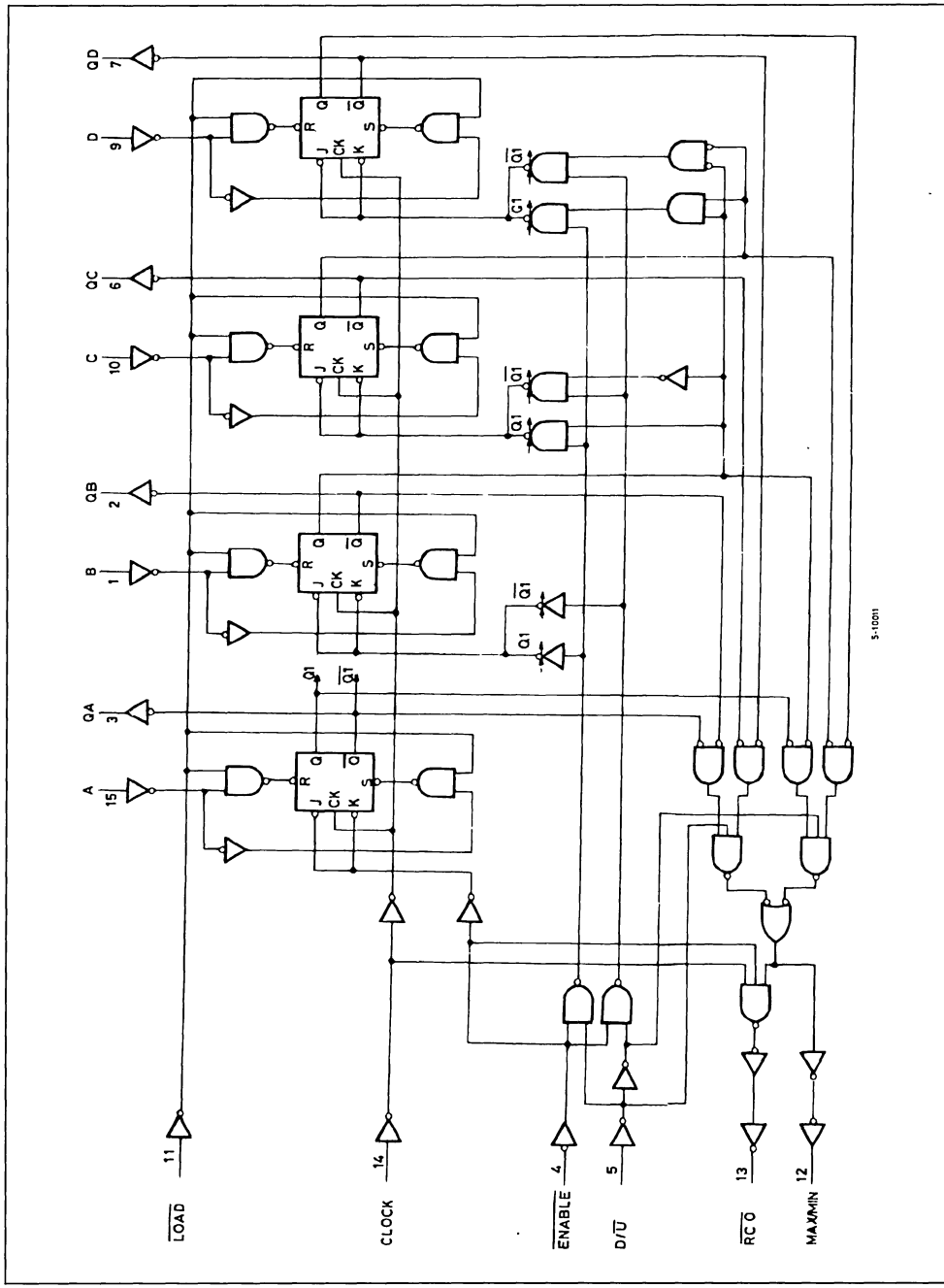
INPUTS				OUTPUS				FUNCTION
$\overline{LOAD}$	$\overline{ENABLE}$	D/$\overline{U}$	CLOCK	QA	QB	QC	QD	
L	X	X	X	a	b	c	d	PRESET DATA
H	L	L	⎍	UP COUNT				UP COUNT
H	L	H	⎍	DOWN COUNT				DOWN COUNT
H	H	X	⎍	NO CHANGE				NO COUNT
H	X	X	⎏	NO CHANGE				NO COUNT

X: Don't Care
a - d: The level of steady state inputs at inputs a through D respectively

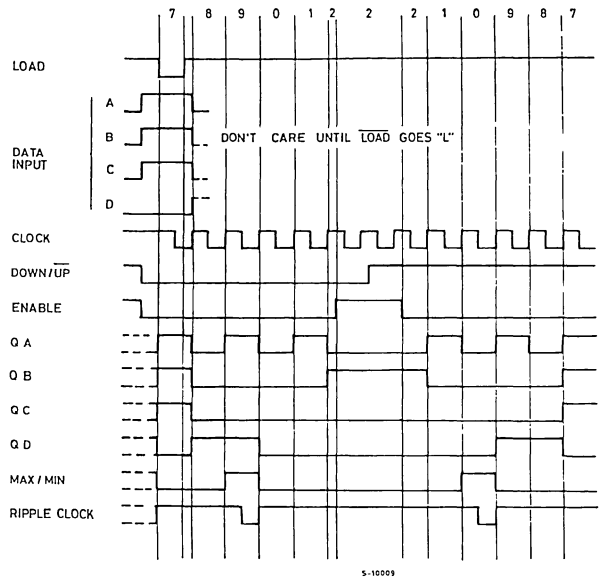
LOGIC DIAGRAM (HC190)



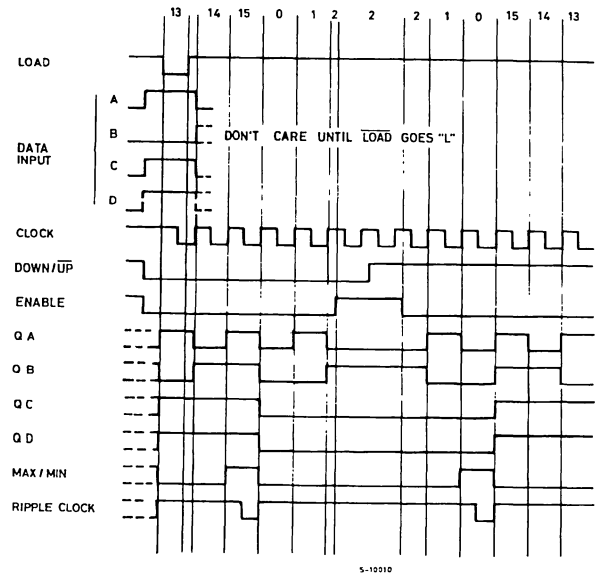
LOGIC DIAGRAM (HC191)



TIMING CHART (HC190)



TIMING CHART (HC191)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur Functional operation under these condition is not implied

(*) 500 mW. ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

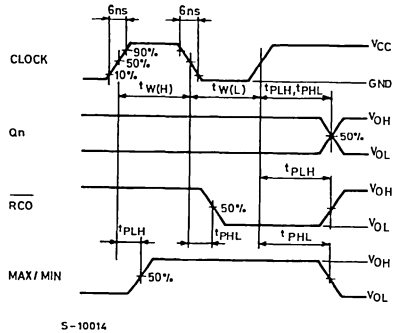
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q)	2.0			92	180		225		270	ns
		4.5			23	36		45		54	
		6.0			20	31		38		46	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - $\overline{RCO}$)	2.0			39	120		150		180	ns
		4.5			13	24		30		36	
		6.0			11	20		26		31	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - MAX/MIN)	2.0			120	240		300		360	ns
		4.5			30	48		60		72	
		6.0			26	41		51		61	
t_{PLH} t_{PHL}	Propagation Delay Time (LOAD - Q)	2.0			108	205		255		310	ns
		4.5			27	41		51		62	
		6.0			23	35		43		53	

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

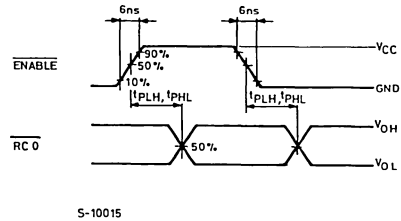
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time (DATA - Q)	2.0			84	175		220		265	ns
		4.5			21	35		44		53	
		6.0			18	30		37		45	
t_{PLH} t_{PHL}	Propagation Delay Time (ENABLE - RCO)	2.0			39	105		130		160	ns
		4.5			13	21		26		32	
		6.0			11	18		22		27	
t_{PLH} t_{PHL}	Propagation Delay Time (D/U - RCO)	2.0			63	180		225		270	ns
		4.5			21	36		45		54	
		6.0			18	31		38		46	
t_{PLH} t_{PHL}	Propagation Delay Time (D/U - MAX/MIN)	2.0			64	160		200		240	ns
		4.5			18	32		40		48	
		6.0			15	27		34		41	
f_{MAX}	Maximum Clock Frequency	2.0		5	9		4		3.4		MHz
		4.5		25	37		20		17		
		6.0		30	44		24		20		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0			40	100		125		150	ns
		4.5			10	20		25		30	
		6.0			9	17		21		26	
$t_{W(L)}$	Minimum Pulse Width (LOAD)	2.0			36	75		95		110	ns
		4.5			9	15		19		22	
		6.0			8	13		16		19	
t_s	Minimum Set-up Time (SI, PI - CK)	2.0			80	175		220		265	ns
		4.5			20	35		44		53	
		6.0			17	30		37		45	
t_s	Minimum Set-up Time (S0, S1 - CK)	2.0			16	50		60		75	ns
		4.5			4	10		12		15	
		6.0			3	9		11		13	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Minimum Removal Time	2.0			12	50		60		5	ns
		4.5			3	10		12		15	
		6.0			3	9		11		13	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance		for HC190 for HC191		111 112						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

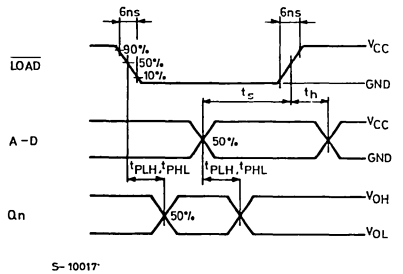
SWITCHING CHARACTERISTICS TEST WAVEFORM



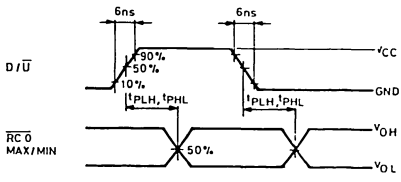
S-10014



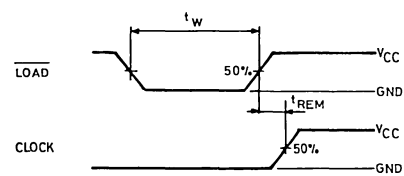
S-10015



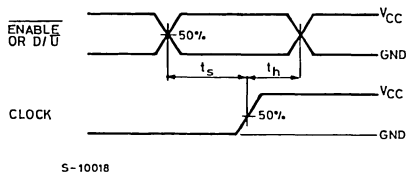
S-10017



S-10016

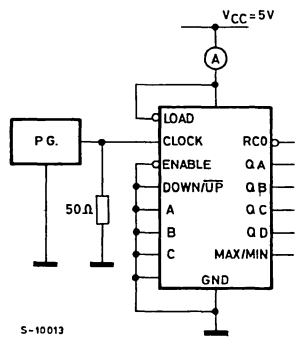


S-10019



S-10018

TEST CIRCUIT Icc (Opr.)

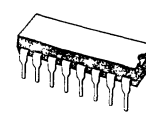


S-10013

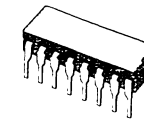
INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

HC192 - SYNCHRONOUS UP/DOWN DECADE COUNTER
HC193 - SYNCHRONOUS UP/DOWN BINARY COUNTER

- HIGH SPEED
  f_{MAX} = 54 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS192-193



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

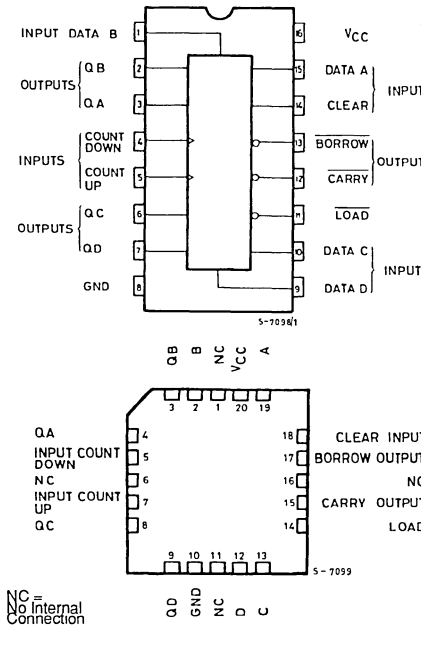
ORDER CODES :

M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

DESCRIPTION

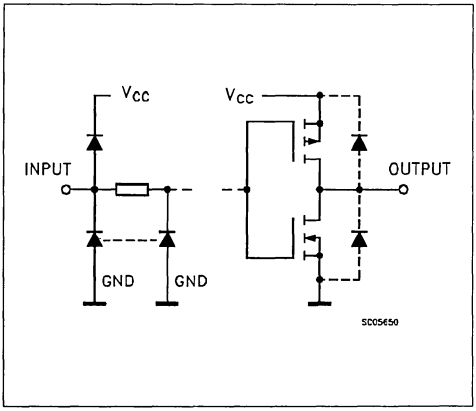
The M54/74HC192/193 are a high speed CMOS SYNCHRONOUS UP/DOWN DECADE COUNTERS fabricated in silicon gate C^2MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. The counter has two separate clock inputs, an UP COUNT input and a DOWN COUNT input. All outputs of the flip-flop are simultaneously triggered on the low to high transition of either clock while the other input is held high. The direction of counting is determined by which input is clocked. This counter may be preset by entering the desired data on the DATA A, DATA B, DATA C, and DATA D input. When the LOAD input is taken low the data is loaded independently of either clock input. This feature allows the counters to be used as divide-by-n counters by modifying the count length with the preset inputs. In addition the counter can also be cleared. This is accomplished by inputting a high on the CLEAR input. All 4 internal stages are set to low independently of either COUNT input. Both a BORROW and CARRY output are provided to enable cascading of both up and down counting functions. The BORROW output produces a negative going pulse when the counter underflows and the CARRY outputs a pulse when the counter overflows. The counter can be cascaded by connecting the CARRY and BORROW outputs of one device to the COUNT UP and COUNT DOWN inputs, respectively, of the next device. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)



NC = No Internal Connection

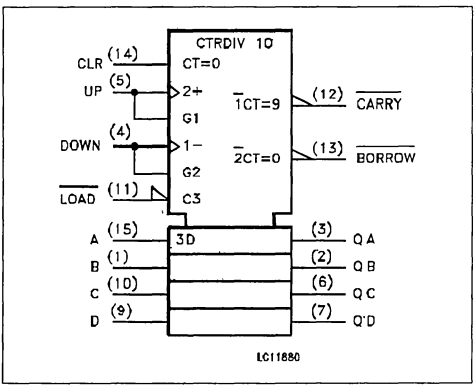
INPUT AND OUTPUT EQUIVALENT CIRCUIT



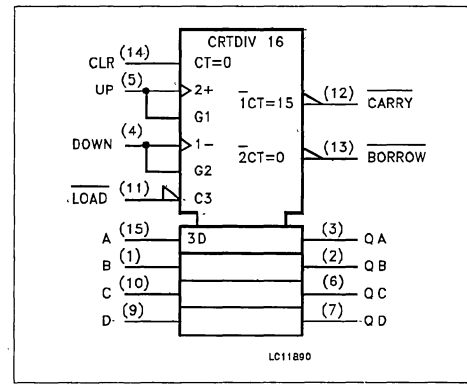
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	QA to QD	Flip-Flop Outputs
4	CP_D	Count Down Clock Input
5	CP_U	Count Up Clock Input
11	$\overline{LOAD}$	Asynchronous Parallel Load Input (Active LOW)
12	$\overline{CARRY}$	Count Up (Carry) Output (Active LOW)
13	$\overline{BORROW}$	Count Down (Borrow) Output (Active LOW)
14	CLEAR	Asynchronous Reset Input (Active HIGH)
15, 1, 10, 9	DA to DD	Data Inputs
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

IEC LOGIC SYMBOL (HC191)



IEC LOGIC SYMBOL (HC193)

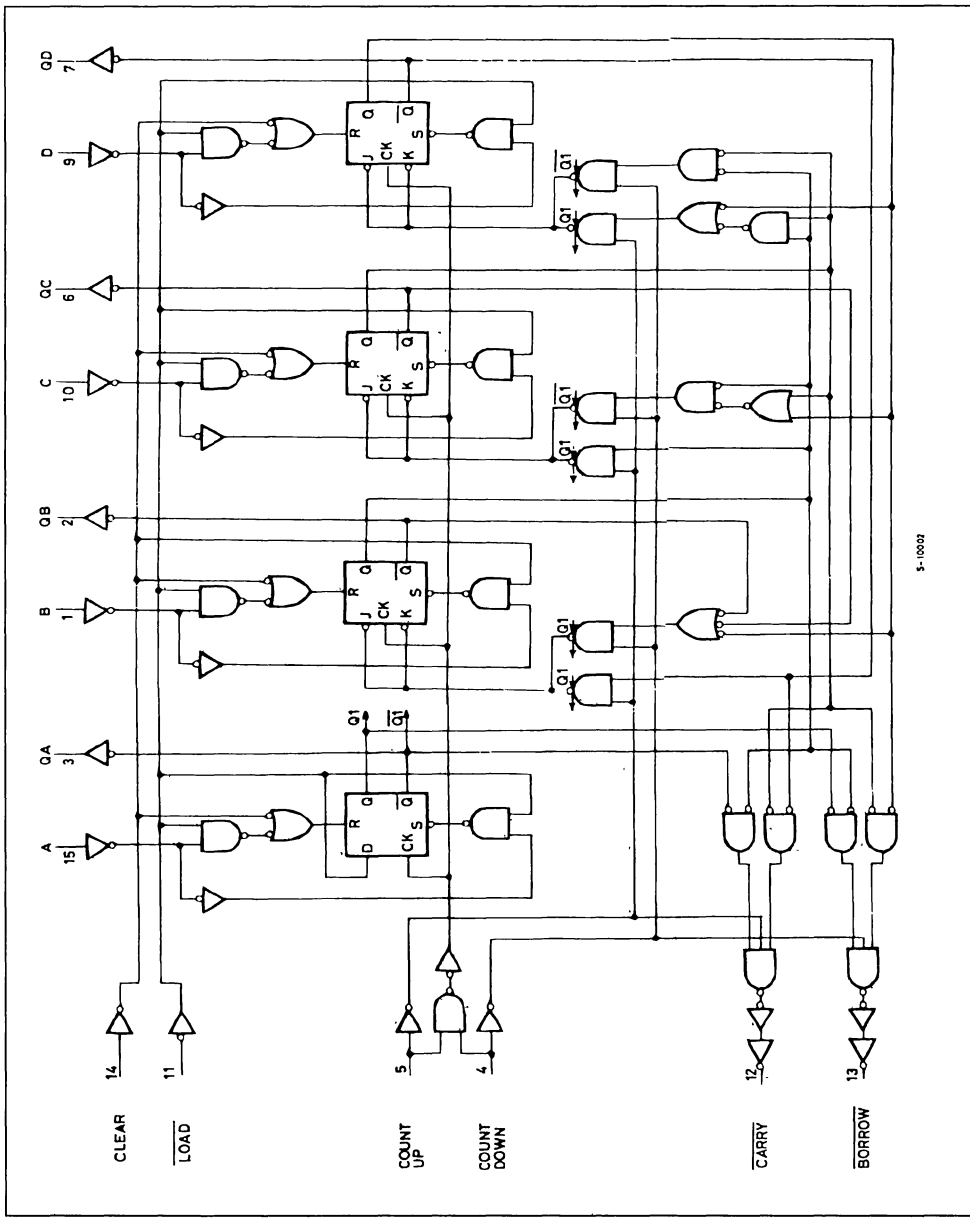


TRUTH TABLE

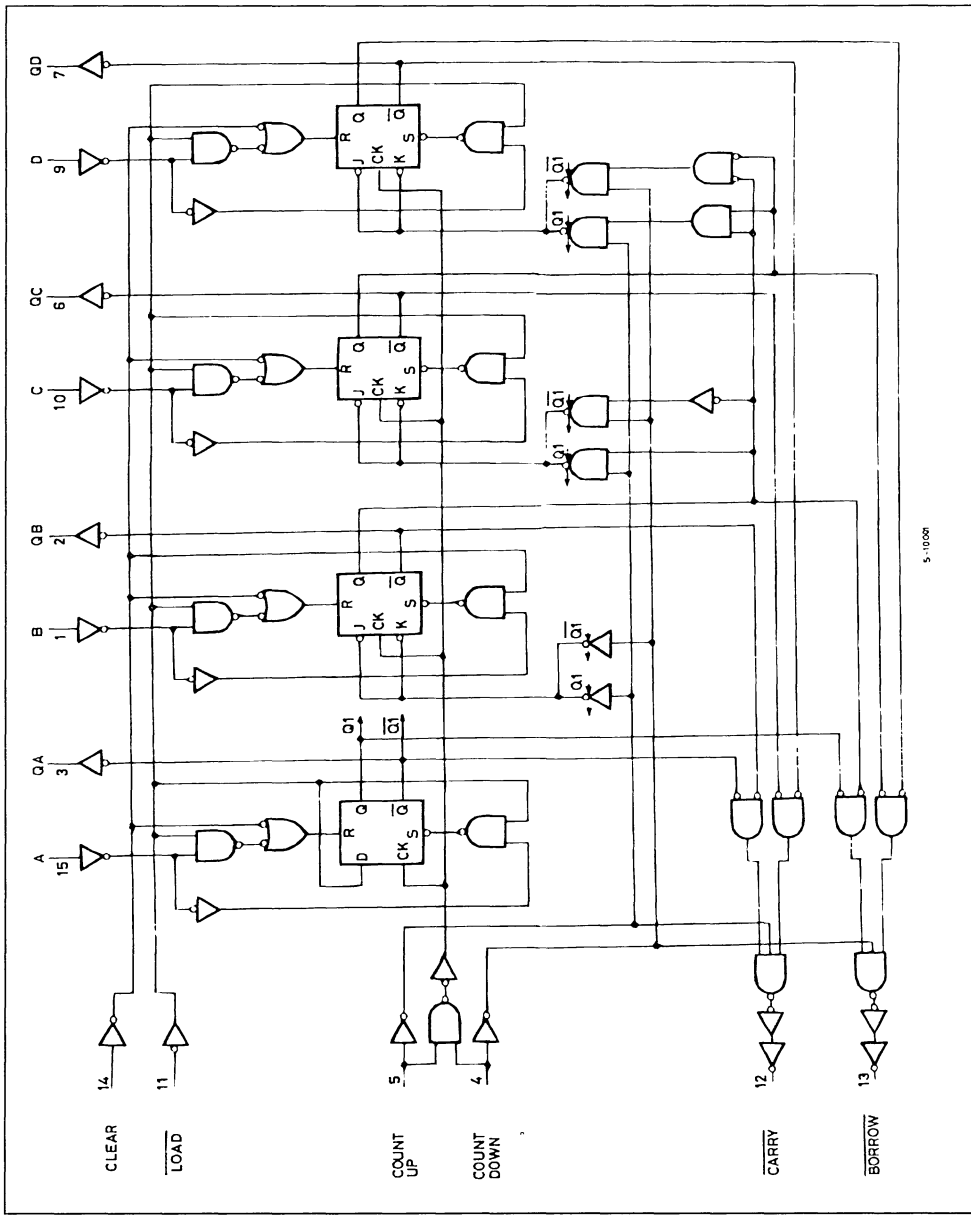
COUNT UP	COUNT DOWN	$\overline{LOAD}$	CLEAR	FUNCTION
⌐	H	H	L	COUNT UP
¬	H	H	L	NO COUNT
H	⌐	H	L	COUNT DOWN
H	¬	H	L	NO COUNT
X	X	L	L	PRESET
X	X	X	H	RESET

X: Don't Care

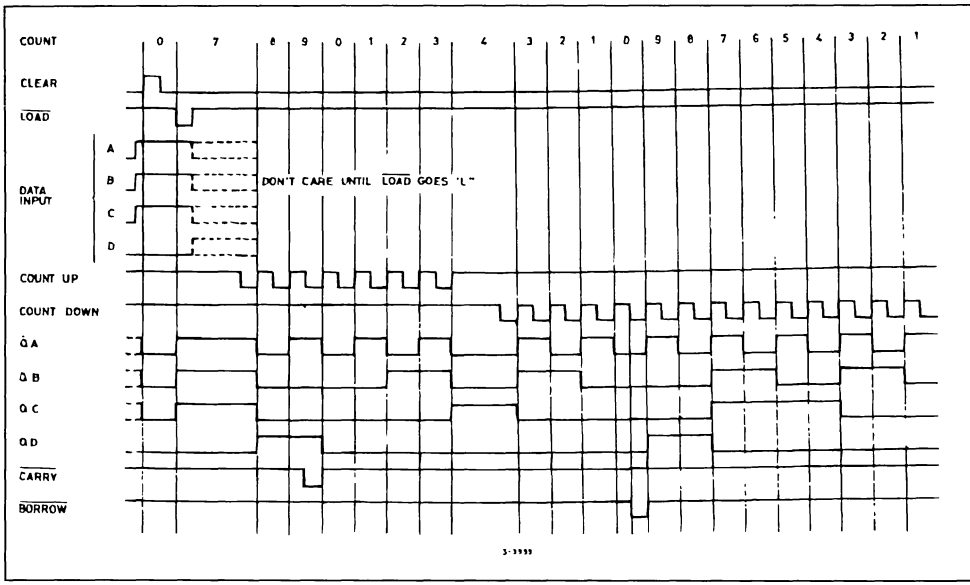
LOGIC DIAGAM (HC192)



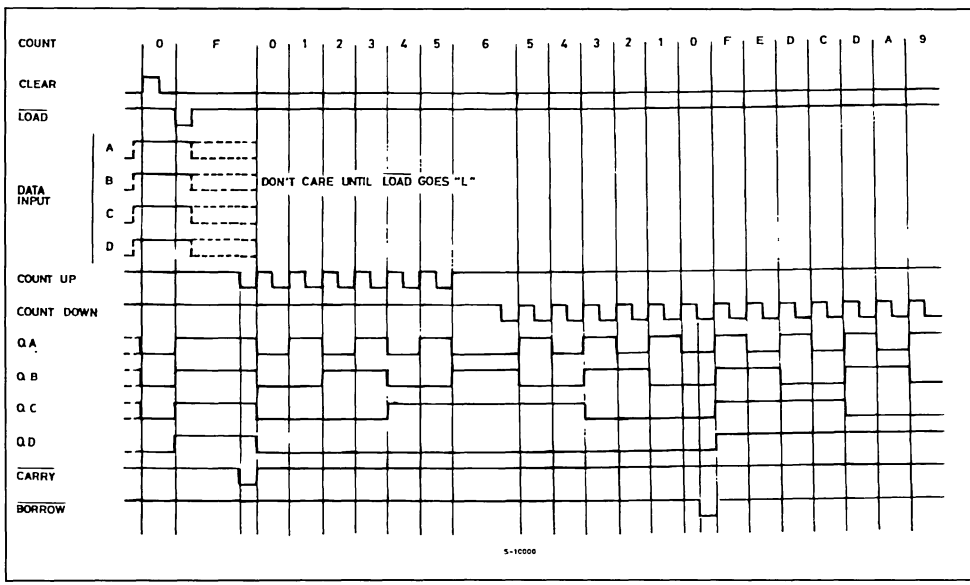
LOGIC DIAGAM (HC193)



TIMING DIAGRAM (HC192)



TIMING DIAGRAM (HC193)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

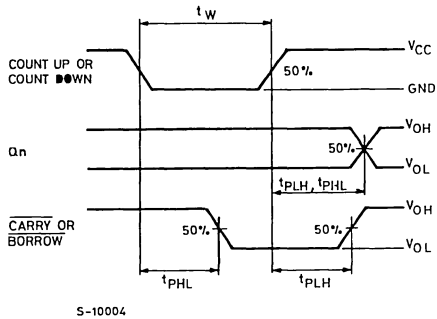
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (UP, DOWN - Q)	2.0			65	190		240		285	ns
		4.5			20	38		48		57	
		6.0			16	32		41		48	
t_{PLH} t_{PHL}	Propagation Delay Time (UP - $\overline{CARRY}$)	2.0			40	130		165		195	ns
		4.5			13	26		33		39	
		6.0			11	22		28		33	
t_{PLH} t_{PHL}	Propagation Delay Time (DOWN - BORROW)	2.0			40	130		165		195	ns
		4.5			13	26		33		39	
		6.0			11	22		28		33	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{LOAD}$ - Q)	2.0			85	220		275		330	ns
		4.5			25	44		55		66	
		6.0			20	37		47		56	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{LOAD}$ - $\overline{CARRY}$)	2.0			110	250		315		375	ns
		4.5			30	50		63		75	
		6.0			25	43		54		64	
t_{PLH} t_{PHL}	Propagation Delay Time (LOAD - BORROW)	2.0			110	250		315		375	ns
		4.5			31	50		63		75	
		6.0			25	43		54		64	
t_{PLH} t_{PHL}	Propagation Delay Time (DATA - Q)	2.0			80	190		240		285	ns
		4.5			25	38		48		57	
		6.0			20	32		41		48	
t_{PLH} t_{PHL}	Propagation Delay Time (DATA - $\overline{CARRY}$)	2.0			120	250		315		375	ns
		4.5			34	50		63		75	
		6.0			28	43		54		64	
t_{PLH} t_{PHL}	Propagation Delay Time (DATA - $\overline{BORROW}$)	2.0			110	250		315		375	ns
		4.5			30	50		63		75	
		6.0			25	43		54		64	
t_{PHL}	Propagation Delay Time (CLEAR - Q)	2.0			100	225		280		340	ns
		4.5			30	45		56		68	
		6.0			25	38		48		58	
t_{PLH}	Propagation Delay Time (CLEAR - $\overline{CARRY}$)	2.0			120	250		315		375	ns
		4.5			35	50		63		75	
		6.0			29	43		54		64	
t_{PHL}	Propagation Delay Time (CLEAR - $\overline{BORROW}$)	2.0			120	250		315		375	ns
		4.5			35	50		63		75	
		6.0			29	43		54		64	
f_{MAX}	Maximum Clock Frequency	2.0		5	12		4		3.4		MHz
		4.5		25	48		20		17		
		6.0		30	55		24		20		

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

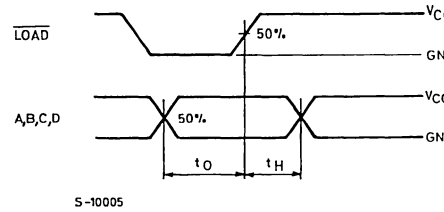
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (COUNT UP/DOWN)	2.0			34	100		125		150	ns
		4.5			9	20		25		30	
		6.0			7	17		21		26	
$t_{W(L)}$	Minimum Pulse Width $\overline{(LOAD)}$	2.0			34	75		95		110	ns
		4.5			9	15		19		22	
		6.0			7	13		16		19	
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	2.0			40	100		125		150	ns
		4.5			12	20		25		30	
		6.0			10	17		21		26	
t_s	Minimum Set-up Time (DATA - $\overline{LOAD}$)	2.0			30	75		95		110	ns
		4.5			9	15		19		22	
		6.0			7	13		16		19	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Minimum Removal Time $\overline{(LOAD)}$	2.0			6	50		65		75	ns
		4.5			2	10		13		15	
		6.0			2	9		11		13	
t_{REM}	Minimum Removal Time (CLEAR)	2.0			14	50		65		75	ns
		4.5			4	10		13		15	
		6.0			3	9		11		13	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance		for HC192		68						pF
			for HC193		67						

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

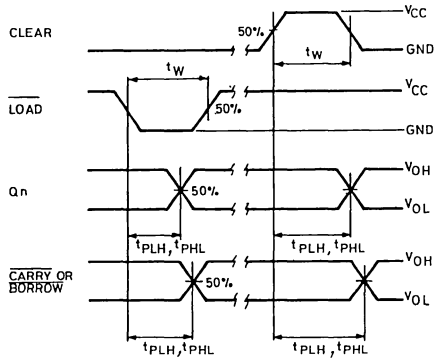
SWITCHING CHARACTERISTICS TEST WAVEFORM



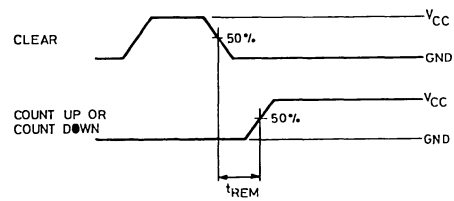
S-10004



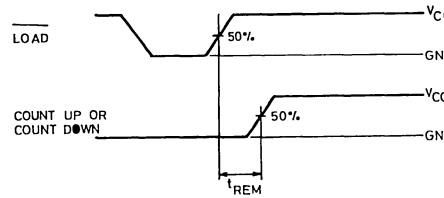
S-10005



S-10006

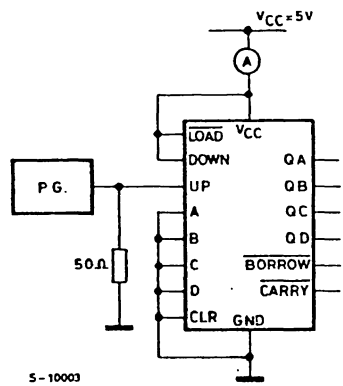


S-10008



S-10007

TEST CIRCUIT Icc (Opr.)



S-10003

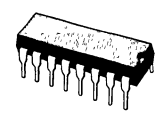
TRANSITION TIME OF INPUT WAVEFORMS IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

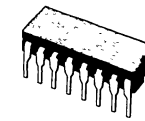
M54HC194
M74HC194

4 BIT PIPO SHIFT REGISTER

- HIGH SPEED
  t_{PD} = 12 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS194



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

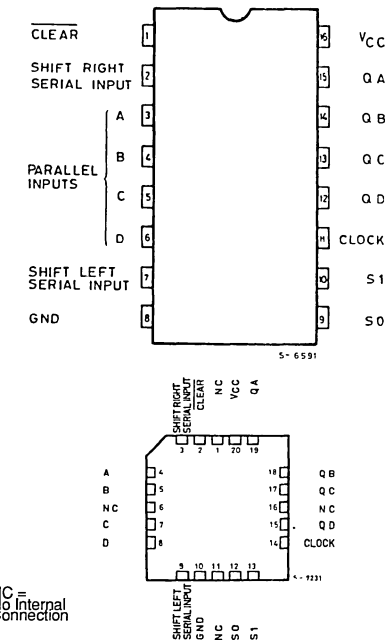
ORDER CODES :

M54HC194F1R M74HC194M1R
M74HC194B1R M74HC194C1R

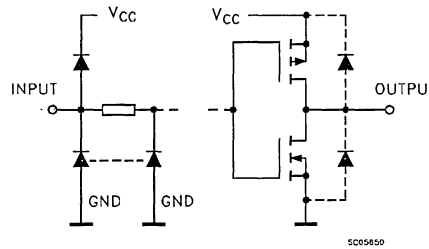
DESCRIPTION

The M54/74HC194 is a high speed CMOS 4 BIT PIPO SHIFT REGISTER fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This SHIFT REGISTER is designed to incorporate virtually all of the features a system designer may want in a shift register. It features parallel inputs, parallel outputs, right shift and left shift serial inputs, clear line. The register has four distinct modes of operation : PARALLEL (broadside) LOAD ; SHIFT RIGHT (in the direction Q_A Q_D); SHIFT LEFT ; INHIBIT CLOCK (do nothing). Synchronous parallel loading is accomplished by applying the four data bits and taking both mode control inputs, S0 and S1 high. The data are loaded into their respective flip-flops and appear at the outputs after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the SHIFT RIGHT data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the SHIFT LEFT serial input. Clocking of the flip flops is inhibited when both mode control inputs are low. The mode control inputs should be changed only when the CLOCK input is high. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)



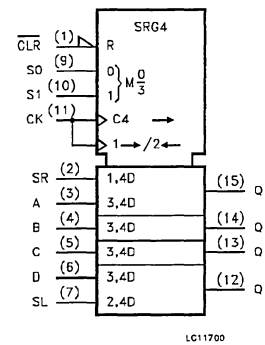
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{CLEAR}$	Asynchronous Reset Input (Active LOW)
2	SR	Serial Data Input (Shift Right)
3, 4, 5, 6	A to D	Parallel Data Input
7	SL	Serial Data Input (Shift Left)
9, 10	S0, S1	Mode Control Inputs
11	CLOCK	Clock Input (LOW to HIGH Edge-triggered)
15, 14, 13, 12	QA to QD	Paralle Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL

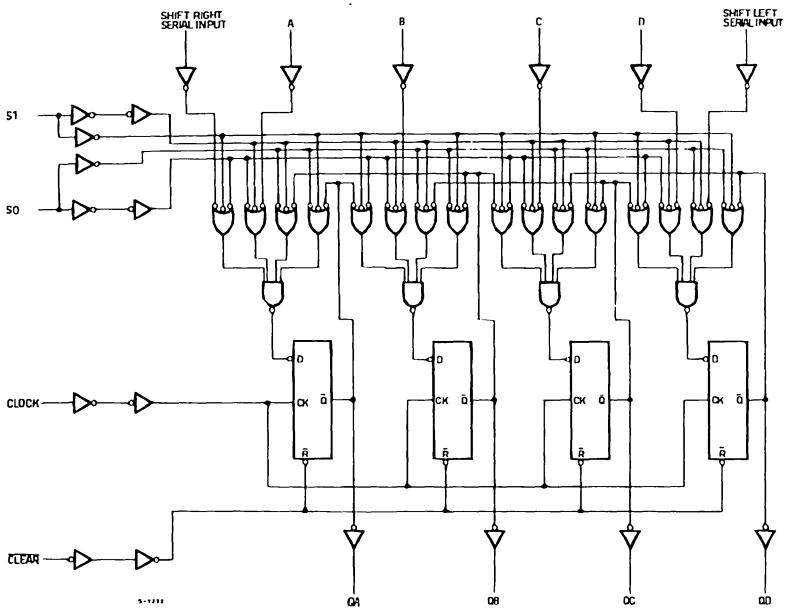


TRUTH TABLE

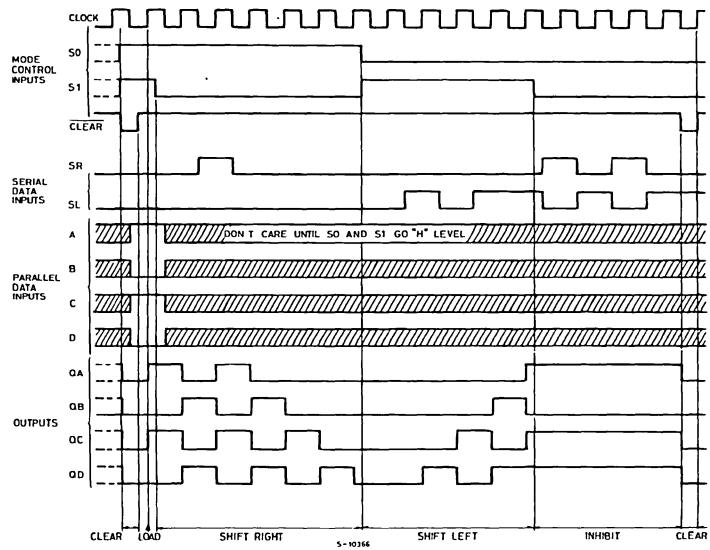
INPUTS										OUTPUS			
$\overline{CLEAR}$	MODE		CLOCK	SERIAL		PARALLEL				QA	QB	QC	QD
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	⌐	X	X	X	X	X	X	QA0	QB0	QC0	QD0
H	H	H	⌐	X	X	a	b	c	d	a	b	c	d
H	L	H	⌐	X	H	X	X	X	X	H	QAn	QBn	QCn
H	L	H	⌐	X	L	X	X	X	X	L	QAn	QBn	QCn
H	H	L	⌐	H	X	X	X	X	X	QBn	QCn	QDn	H
H	H	L	⌐	L	X	X	X	X	X	QBn	QCn	QDn	L
H	L	L	X	X	X	X	X	X	X	QA0	QB0	QC0	QD0

X: Don't Care : Don't Care
a ~ d : The level of steady state input voltage at input A ~ D respactıvely
QA0 ~ QD0 : No change
QAn ~ QDn : The level of QA, QB, QC, respectively, before the mst recent positive transition of the clock

LOGIC DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

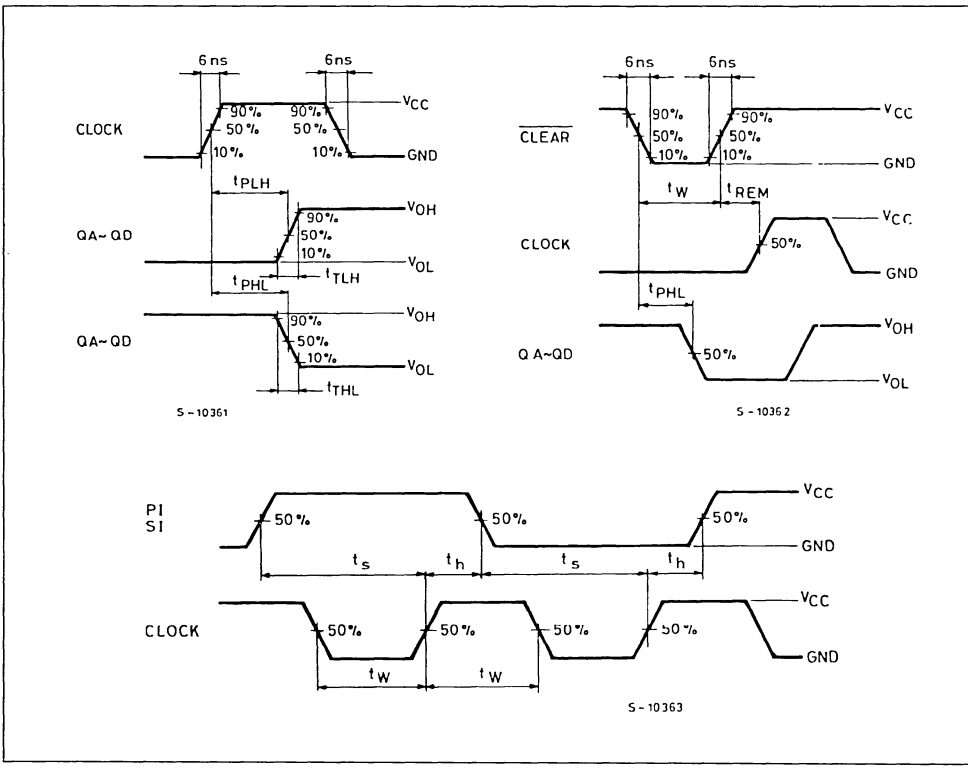
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

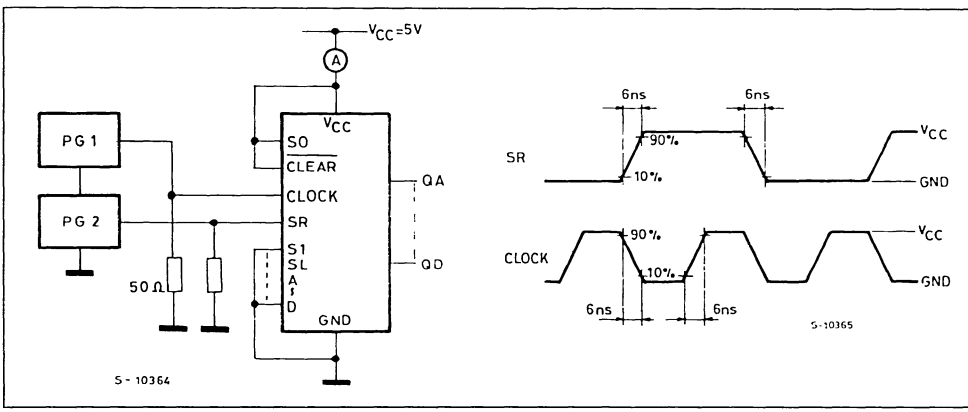
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		115	ns
		4.5			8	15		19		23	
		6.0			7	13		16		20	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q)	2.0			48	115		145		175	ns
		4.5			15	23		29		35	
		6.0			13	20		25		30	
t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$ - Q)	2.0			52	125		155		190	ns
		4.5			17	25		31		38	
		6.0			15	21		26		32	
f_{MAX}	Maximum Clock Frequency	2.0		6.2	13		5.0		4.2		MHz
		4.5		31	50		25		21		
		6.0		37	59		30		25		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLEAR}$)	2.0			24	75		95		110	ns
		4.5			6	15		19		22	
		6.0			5	13		16		19	
t_s	Minimum Set-up Time (SI, PI - CK)	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		20	
t_s	Minimum Set-up Time (S0, S1 - CK)	2.0			28	75		95		110	ns
		4.5			7	15		19		23	
		6.0			6	13		16		20	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Minimum Removal Time	2.0				5		5		5	ns
		4.5				5		5		5	
		6.0				5		5		5	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				85						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

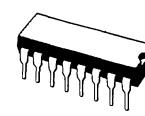


TEST CIRCUIT I_{CC} (Opr.)

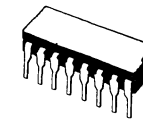


8 BIT PIPO SHIFT REGISTER

- HIGH SPEED
  t_{PD} = 13 ns (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25 °C 6 V
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V to 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS195



B1R
(Plastic Package)



F1R
(Ceramic Package)

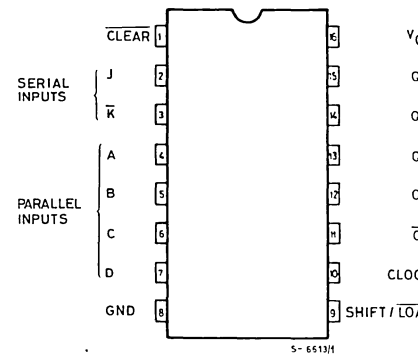
M1R
(Micro Package)

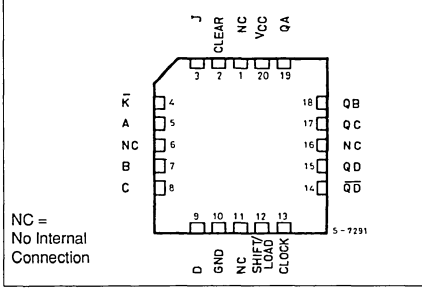
C1R
(Chip Carrier)

ORDER CODES :

M54HC195F1R M74HC195M1R
M74HC195B1R M74HC195C1R

PIN CONNECTIONS (top view)





NC =
No Internal
Connection

DESCRIPTION

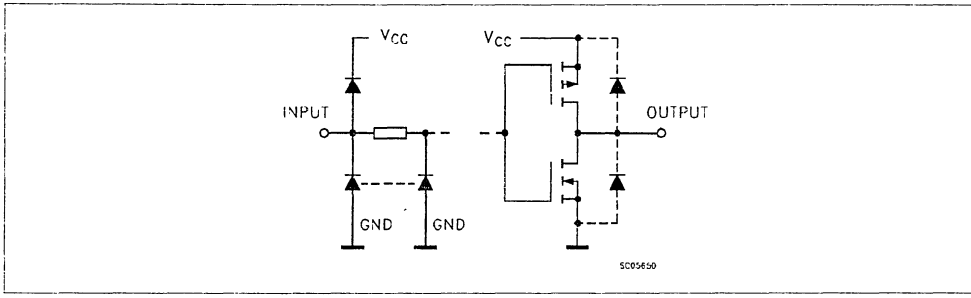
The M54/74HC195 is a high speed CMOS 4 BIT PIPO SHIFT REGISTER fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

This shift register features parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, a SHIFT/$\overline{LOAD}$ control input, and a direct overriding $\overline{CLEAR}$. This shift register can operate in two modes : Parallel Load ; Shift from QA towards QD.

Parallel loading is accomplished by applying the four bits of data, and taking the SHIFT/$\overline{LOAD}$ control input low. The data is loaded into the associated flip flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited. Serial shifting occurs synchronously when the SHIFT/$\overline{LOAD}$ control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs allow the first stage to perform as a J-$\overline{K}$ or TOGGLE flip flop as shown in the truthtable.

All inputs are equipped with protection circuits against static discharge transient excess voltage.

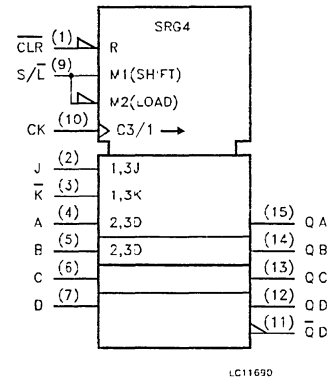
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{CLEAR}$	Reset Input (Active LOW)
2	J	First Stage J Input (Active LOW)
3	$\overline{K}$	First Stage $\overline{K}$ Input (Active LOW)
4, 5, 6, 7	A to D	Parallel Data Input
9	SHIFT/$\overline{LOAD}$	Control Input
10	CLOCK	Clock Input (LOW to HIGH Edge-triggered)
11	$\overline{QD}$	Inverted Output From The Last Stage
15, 14, 13, 12	QA to QD	Paralle Outputs
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

IEC LOGIC SYMBOL

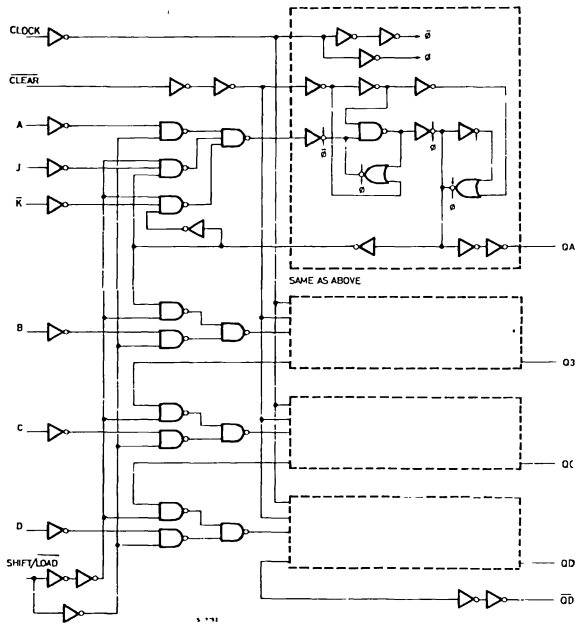


TRUTH TABLE

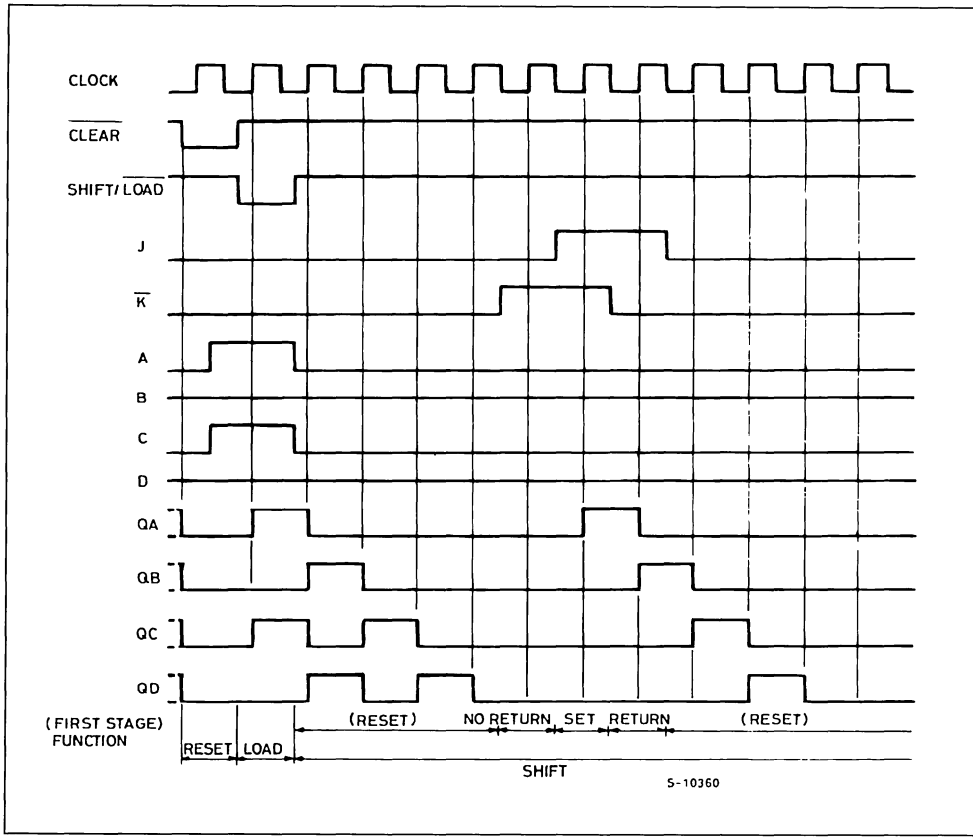
INPUTS									OUTPUS				
$\overline{CLEAR}$	SHIFT/$\overline{LOAD}$	CLOCK	SERIAL		PARALLEL				QA	QB	QC	QD	$\overline{QD}$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	L
H	L	⌐	X	X	a	b	c	d	a	b	c	d	d
H	H	⌐	X	X	X	X	X	X	QA0	QB0	QC0	QD0	$\overline{QD0}$
H	H	⌐	L	H	X	X	X	X	QA0	QA0	QBn	QCn	$\overline{QCn}$
H	H	⌐	L	L	X	X	X	X	L	QAn	QBn	QCn	$\overline{QCn}$
H	H	⌐	H	H	X	X	X	X	H	QAn	QBn	QCn	$\overline{QCn}$
H	H	⌐	H	L	X	X	X	X	$\overline{QAn}$	QAn	QBn	QCn	$\overline{QCn}$

X Don't Care The level of QA QB QC, respectively, before the mst recent positive transition of the clock

LOGIC DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

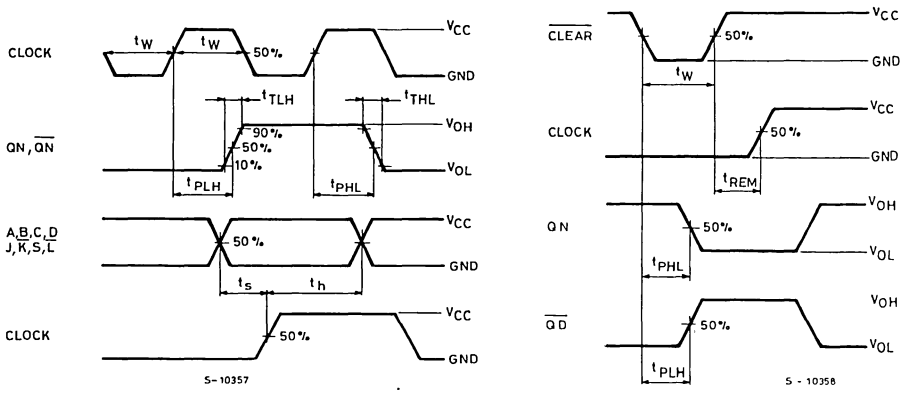
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

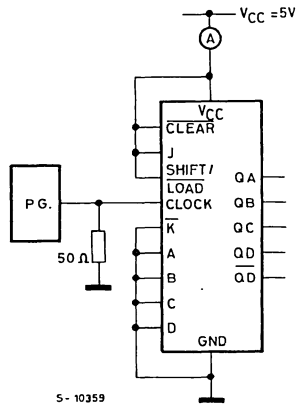
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		115	ns
		4.5			8	15		19		23	
		6.0			7	13		16		20	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK- Qn, $\overline{QD}$)	2.0			48	125		155		190	ns
		4.5			16	25		31		38	
		6.0			14	21		26		32	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$- Qn, $\overline{QD}$)	2.0			45	120		150		180	ns
		4.5			15	24		30		36	
		6.0			13	20		26		31	
f_{MAX}	Maximum Clock Frequency	2.0		7.6	15		6		5		MHz
		4.5		38	60		30		25		
		6.0		45	71		35		30		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0			20	75		95		115	ns
		4.5			5	15		19		23	
		6.0			4	13		16		20	
$t_{W(L)}$	Minimum Pulse Width (CLEAR)	2.0			20	75		95		115	ns
		4.5			5	15		19		23	
		6.0			4	13		16		20	
t_s	Minimum Set-up Time (PI)	2.0			28	75		95		115	ns
		4.5			7	15		19		23	
		6.0			6	13		16		20	
t_s	Minimum Set-up Time (J, $\overline{K}$, $\overline{S/L}$)	2.0			28	75		95		115	ns
		4.5			7	15		19		23	
		6.0			6	13		16		20	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Minimum Removal Time	2.0				5		5		5	ns
		4.5				5		5		5	
		6.0				5		5		5	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				72						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT Icc (Opr.)

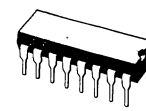


TRANSITION TIME OF INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

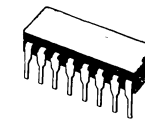
M54HC221/221A
M74HC221/221A

DUAL MONOSTABLE MULTIVIBRATOR

- HIGH SPEED
  t_{PD} = 25 ns (TYP) at V_{CC} = 5V
- LOW POWER DISSIPATION
  STANDBY STATE I_{CC}=4 µA (MAX.) AT T_A=25°C
  ACTIVE STATE I_{CC} = 700 µA (MAX.) AT V_{CC}=5V
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $I_{OH} = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- WIDE OUTPUT PULSE WIDTH RANGE
  t_{WOUT} = 150 ns ~ 60 s OVER AT V_{CC} = 4.5 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS221



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

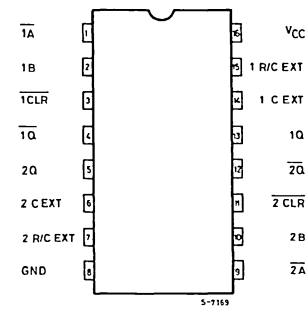
ORDER CODES :

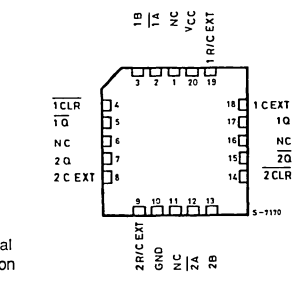
M54HCXXXF1R M74HCXXXXM1R
M74HCXXXB1R M74HCXXXC1R

DESCRIPTION

The M54/74HC221/221A are high speed CMOS MONOSTABLE multivibrators fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. There are two trigger inputs, $\overline{A}$ INPUT (negative edge) and B INPUT (positive edge). Triggering on the B input occurs at a particular voltage threshold and is not related to the rise and fall time of the applied pulse. The device may also be triggered by using the $\overline{CLR}$ input (positive-edge) because of the Schmitt-trigger input ; after triggering the output maintains the MONOSTABLE state for the time period determined by the external resistor Rx and capacitor Cx.Taking $\overline{CLR}$ low breaks this MONOSTABLE STATE. If the next trigger pulse occurs during the MONOSTABLE period it makes the MONOSTABLE period longer.
Limit for values of Cx and Rx :
Cx : NO LIMIT
Rx : V_{CC} < 3.0 V 5 K Ω to 1 M Ω
$V_{CC} \geq$ 3.0 V 1 K Ω to 1 M Ω
Two different pulse width constants are available:
K ≅ 0.7 for HC221
K ≅ 1 for HC221A
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

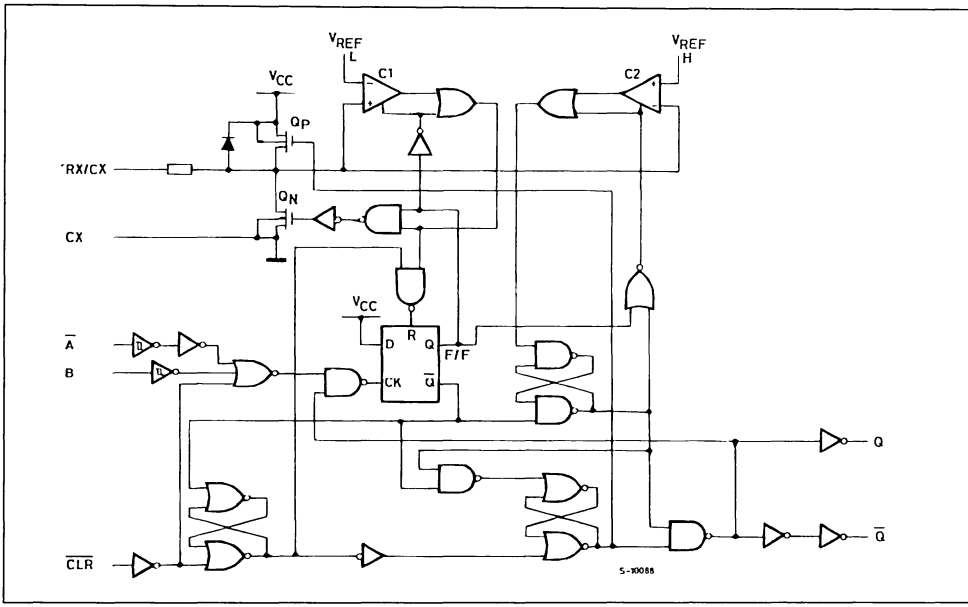
PIN CONNECTIONS (top view)



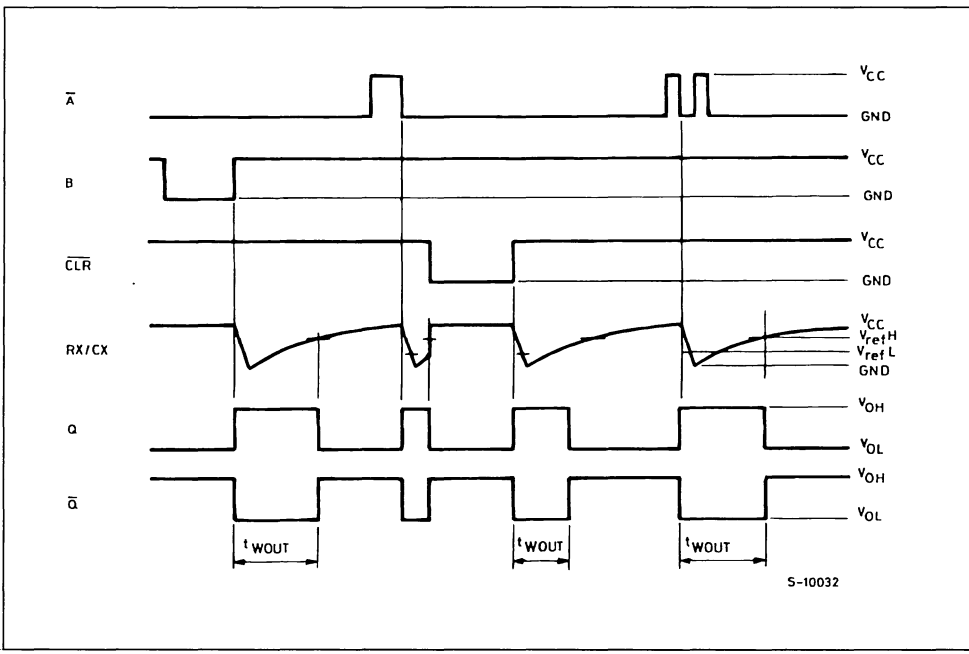


NC =
No Internal
Connection

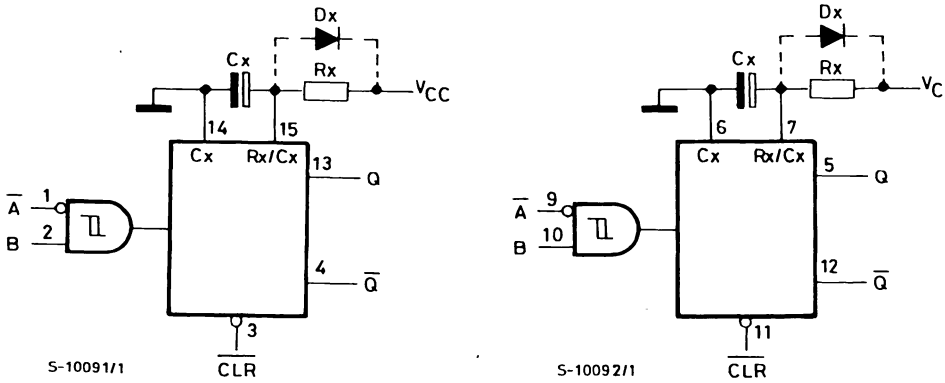
SYSTEM DIAGRAM



TIMING CHART



BLOCK DIAGRAM



Note :

(1) Cx, Rx, Dx are external components.

(2) Dx is a clamping diode.

The external capacitor is charged to V_{CC} in the stand-by state, i.e. no trigger. When the supply voltage is turned off Cx is discharged mainly through an internal parasitic diode (see figures). If Cx is sufficiently large and V_{CC} decreases rapidy, there will be some possibility of damaging the I.C. with a surge current or latch-up. If the voltage supply filter capacitor is large enough and V_{CC} decrease slowly, the surge current is automatically limited and damage the I.C. is avoided. The maximum forward current of the parasitic diode is approximately 20 mA. In cases where Cx is large the time taken for the supply voltage to fall to 0.4 V_{CC} can be calculated as follows :

$t_f \geq (V_{CC} - 0.7)\ Cx/20mA$

In cases where t_f is too short an external clamping diode is required to protect the I.C. from the surge current.

FUNCTIONAL DESCRIPTION

STAND-BY STATE

The external capacitor, Cx, is fully charged to V_{CC} in the stand-by state. Hence, before triggering, transistor Qp and Qn (connected to the Rx/Cx node) are both turned-off. The two comparators that control the timing and the two reference voltage sources stop operating. The total supply current is therefore only leakage current.

TRIGGER OPERATION

Triggering occurs when :

1st) A is "low" and B has a falling edge ;
2nd) B is "high" and A has a rising edge ;
3rd) A is low and B is high and C1 has a rising edge.

After the multivibrator has been retriggered comparator C1 and C2 start operating and Qn is turned on. Cx then discharges through Qn. The voltage at the node R/C external falls.

When it reaches V_{REFL} the output of comparator C1 becomes low. This in turn resets the flip-flop and Qn is turned off.

At this point C1 stops functioning but C2 continues to operate.

The voltage at R/C external begins to rise with a time constant set by the external components Rx, Cx.

Triggering the multivibrator causes Q to go high after internal delay due to the flip-flop and the gate. Q remains high until the voltage at R/C external rises again to V_{REFH}. At this point C2 output goes low and O goes low. C2 stop operating. That means that after triggering when the voltage R/C external returns to V_{REFH} the multivibrator has returned to its MONOSTABLE STATE. In the case where Rx · Cx are large enough and the discharge time of the capacitor and the delay time in the I.C. can be ignored, the width of the output pulse tw (out) is as follows :

$$t_{W(OUT)} = 0.70\ Cx \cdot Rx\ (HC221)$$
$$t_{W(OUT)} = Cx \cdot Rx\ (HC221A)$$

RESET OPERATION

CL is normally high. If CL is low, the trigger is not effective because Q output goes low and trigger control flip-flop is reset.

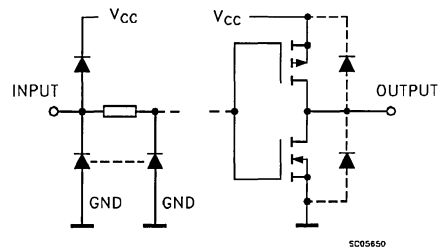
Also transistor Op is turned on and Cx is charged quicky to V_{CC}. This means if CL input goes low, the IC becomes waiting state both in operating and non operating state.

TRUTH TABLE

INPUTS			OUTPUTS		NOTE
$\overline{A}$	B	$\overline{CLR}$	Q	$\overline{Q}$	
⌐	H	H	⌐¬	¬⌐	OUTPUT ENABLE
X	L	H	L (*)	H (*)	INHIBIT
H	X	H	L (*)	H (*)	INHIBIT
L	⌐	H	⌐¬	¬⌐	OUTPUT ENABLE
L	H	⌐	⌐¬	¬⌐	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X: Don't Care (*): Except for monostble period

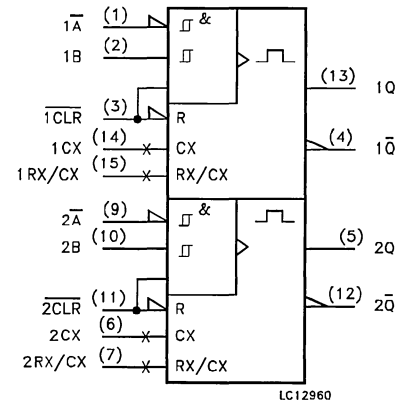
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 9	$1\overline{A}$, $2\overline{A}$	Trigger Inputs (Negative Edge Triggered)
2, 10	1B, 2B	Trigger Inputs (Positive Edge Triggered)
3, 11	$1\overline{CLR}$, $2\overline{CLR}$	Direct Reset LOW and Trigger Action at Positive Edge
4, 12	$1\overline{Q}$, $2\overline{Q}$	Outputs (Active LOW)
7	$2R_{EXT}/C_{EXT}$	External Resistor Capacitor Connection
13, 5	1Q, 2Q	Outputs (Active HIGH)
14, 6	$1C_{EXT}$ $2C_{EXT}$	External Capacitor Connection
15	$1R_{EXT}/C_{EXT}$	External Resistor Capacitor Connection
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time ($\overline{CLR}$ and $\overline{A}$ only)	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	
C_X	External Capacitor		> 100 (*)	pF
R_X	External Resistor	V_{CC} < 3 V	5K to 1M (*)	Ω
		V_{CC} ≥ 3 V	1K to 1M (*)	

(*)The maximum allowable values of Cx and Rx are a function of leackage of capacitor Cx, the leackage of HC221/A, and leackage due to the board layout and surface resistance. Susceptibility to externally induced noise signals may occur for Rx > 1MΩ

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage (Q, $\overline{Q}$ Output)	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage (Q, $\overline{Q}$ Output)	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_I	R/C Terminal Off State Current	6.0	V_I = V_{CC} or GND				±0.5		±5		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA
I_{CC}'	Active State Supply Current (1)	2.0	V_I = V_{CC} or GND V_{IN} = V_{CC}/2			45	250		260		350	µA
		4.5				400	530		650		850	µA
		6.0				0.7	1		1.3		1.7	mA

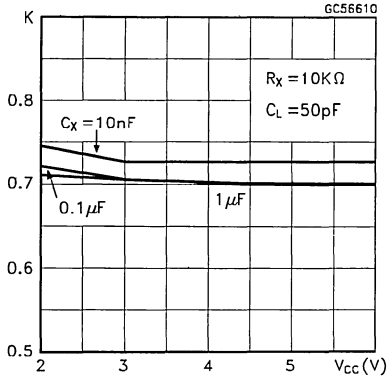
(1): Per Circuit

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

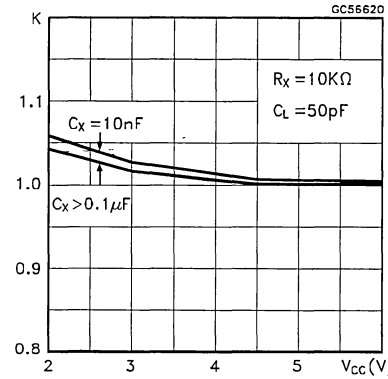
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{A}$, B - Q, $\overline{Q}$)	2.0			102	210		265		315	ns
		4.5			30	42		53		63	
		6.0			24	36		45		54	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$ TRIGGER - Q, $\overline{Q}$)	2.0			102	235		295		355	ns
		4.5			30	47		59		71	
		6.0			24	40		50		60	
t_{PLH} t_{PHL}	Propagation Delay Time (CLR - Q, $\overline{Q}$)	2.0			67	160		200		240	ns
		4.5			20	32		40		48	
		6.0			16	27		34		41	
t_{WOUT}	Output Pulse Width (for HC221)	2.0	C_X = 100 pF R_X = 10 KΩ		1.5						µs
		4.5			1.3						
		6.0			1.2						
		2.0	C_X = 0.1 µF R_X = 100 KΩ		7						ms
		4.5			6.9						
		6.0			6.9						
t_{WOUT}	Output Pulse Width (for HC221A)	2.0	C_X = 100 pF R_X = 10 KΩ		1.8						µs
		4.5			1.5						
		6.0			1.4						
		2.0	C_X = 0.1 µF R_X = 100 KΩ		10						ms
		4.5			9.7						
		6.0			9.6						
Δt_{WOUT}	Output Pulse Width Error Between Circuits in Same Package				±1						%
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width	2.0				75		95		110	ns
		4.5				15		19		22	
		6.0				13		16		20	
$t_{W(L)}$	Minimum Pulse Width	2.0				75		95		110	ns
		4.5				15		19		22	
		6.0				13		16		20	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				174						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$' Duty/100 + $I_{CC}/2$ (per monostable) (I_{CC}': Active Supply Current) (Duty %)

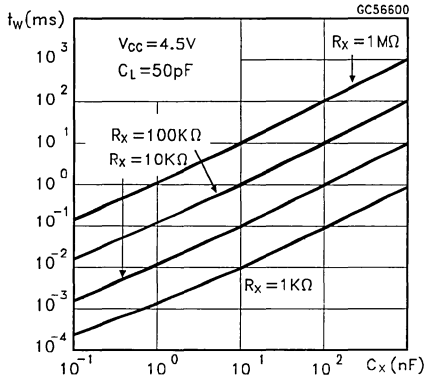
Output Pulse Width Constant Characteristics (for HC221)



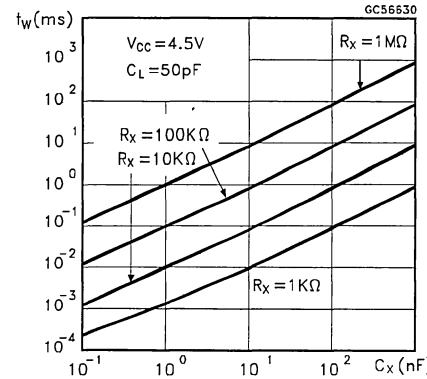
Output Pulse Width Constant Characteristics (for HC221A)



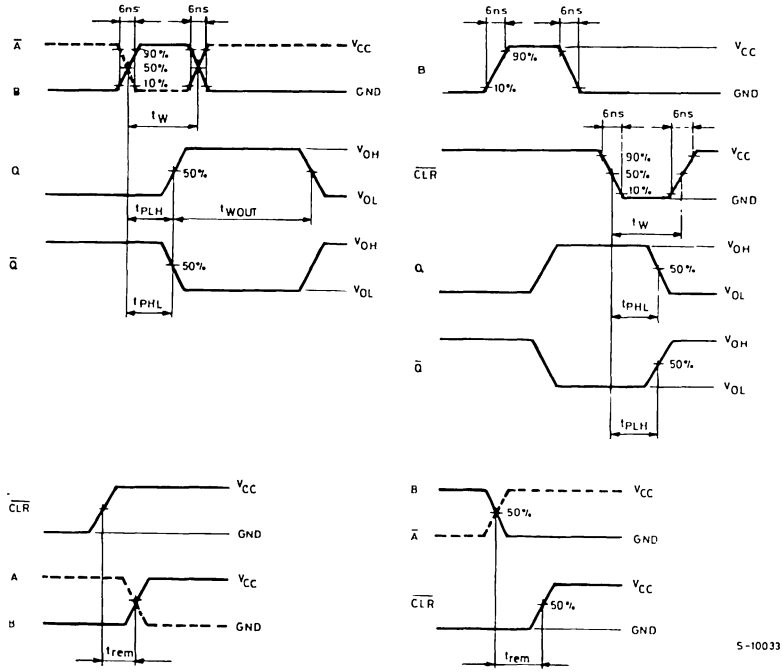
Output Pulse Width Characteristics (for HC221)



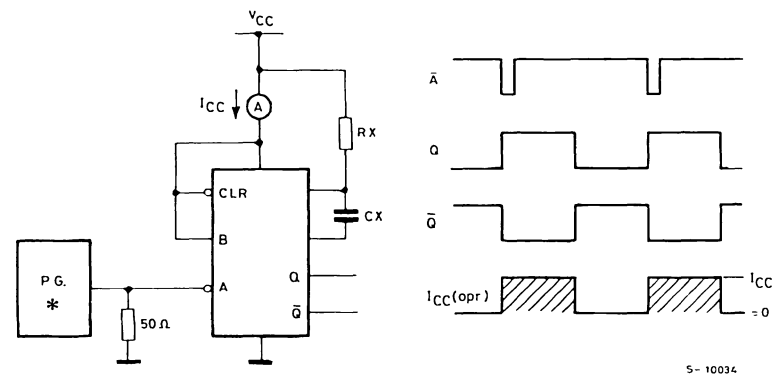
Output Pulse Width Characteristics (for HC221A)



SWITCHING CHARACTERISTICS TEST WAVEFORM



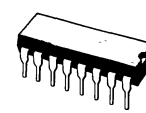
TEST WAVEFORM



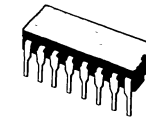
Input Transition Time : 6ns
$V_{IH} = V_{CC}$, $V_{IL} = GND$

3 TO 8 LINE DECODER LATCH

- HIGH SPEED
  t_{PD} = 12 ns (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS237



B1R
(Plastic Package)



F1R
(Ceramic Package)

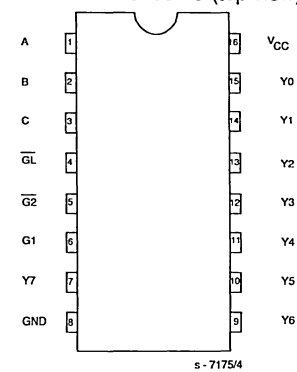
M1R
(Micro Package)

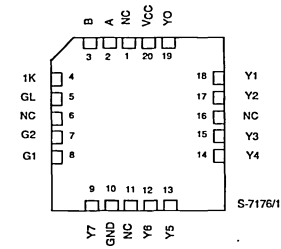
C1R
(Chip Carrier)

ORDER CODES :

M54HC237F1R M74HC237M1R
M74HC237B1R M74HC237C1R

PIN CONNECTIONS (top view)



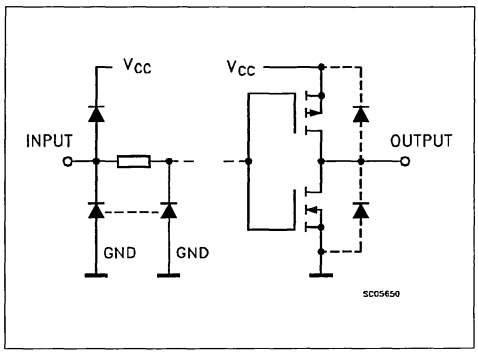


DESCRIPTION

The M54/74HC237 is a high speed CMOS 3 TO 8 LINE DECODER LATCH fabricated in silicon gate C^2MOS technology.

It has the same high speed performance of LSTTL combined with true CMOS low power consumption. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B, C) is stored in the latches. As long as $\overline{GL}$ remains high no address changes will be recognized. Output enable controls, G1 and $\overline{G2}$ control the state of the outputs independantly of the select or latch-enable inputs. All of the outputs are low unless G1 is high and $\overline{G2}$ is low. The 'HC237 is ideally suited for the implementation of glitch-free decoders in stored-address applications in bus oriented systems. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

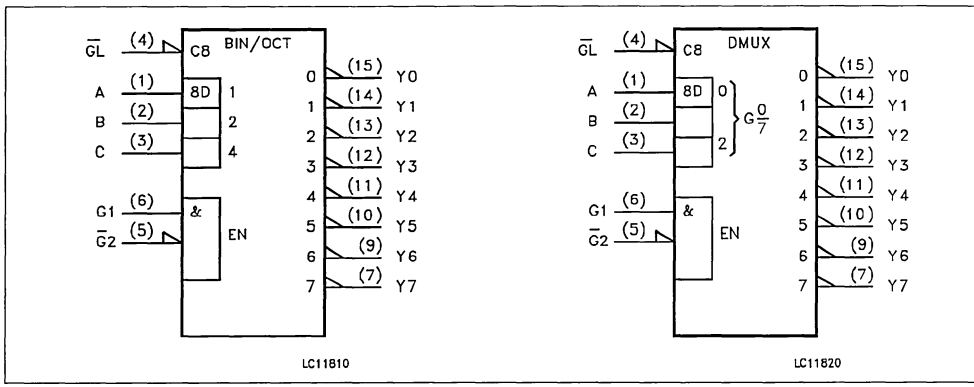
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3	A, B, C	Data Inputs
4	$\overline{GL}$	Latch Enable Input (Active LOW)
5	$\overline{G2}$	Data Enable Input (Active LOW)
6	G1	Data Enable Input (Active HIGH)
15, 14, 13, 12, 11, 10, 9, 7	Y0 to Y7	Decoder Outputs
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

IEC LOGIC SYMBOLS

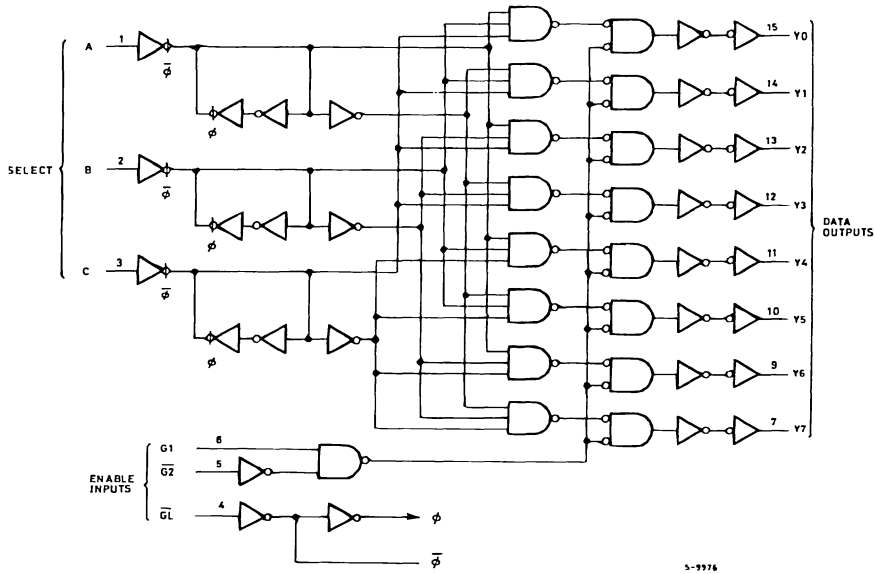


TRUTH TABLE

INPUTS						OUTPUS							
ENABLE			SELECT										
$\overline{GL}$	$\overline{G2}$	G1	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	L	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	L	L	H	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	L	H	H	L	L	L	H	L	L	L	L
L	L	H	H	L	L	L	L	L	L	H	L	L	L
L	L	H	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H
H	L	H	X	X	X	OUTPUT CORRESPONDING TO STORED ADDRESS, H: ALL OTHERS, L							

X: Don't Care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

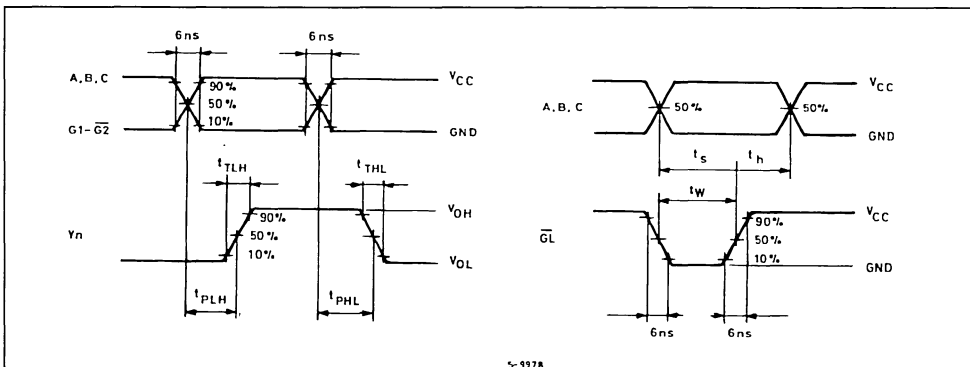
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

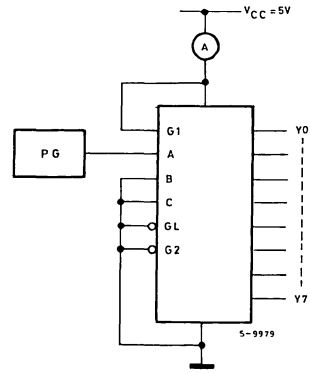
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		115	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C - Y)	2.0			60	180		225		270	ns
		4.5			19	36		45		54	
		6.0			16	31		38		46	
t_{PLH} t_{PHL}	Propagation Delay Time (G1 - Y)	2.0			45	140		175		210	ns
		4.5			15	28		35		42	
		6.0			13	24		30		36	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{G2}$ - Y)	2.0			45	140		175		210	ns
		4.5			15	28		35		42	
		6.0			13	24		30		36	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{GL}$ - Y)	2.0			65	190		240		285	ns
		4.5			21	38		48		57	
		6.0			18	32		41		48	
$t_{W(L)}$	Minimum Pulse Width ($\overline{GL}$)	2.0			10	75		95		110	ns
		4.5			6	15		19		22	
		6.0			6	13		16		19	
t_s	Minimum Set-up Time (A, B, C - $\overline{GL}$)	2.0			12	50		65		75	ns
		4.5			3	10		13		15	
		6.0			2	9		11		13	
t_h	Minimum Hold Time (A, B, C - $\overline{GL}$)	2.0				25		30		40	ns
		4.5				5		6		8	
		6.0				5		5		7	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				52						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

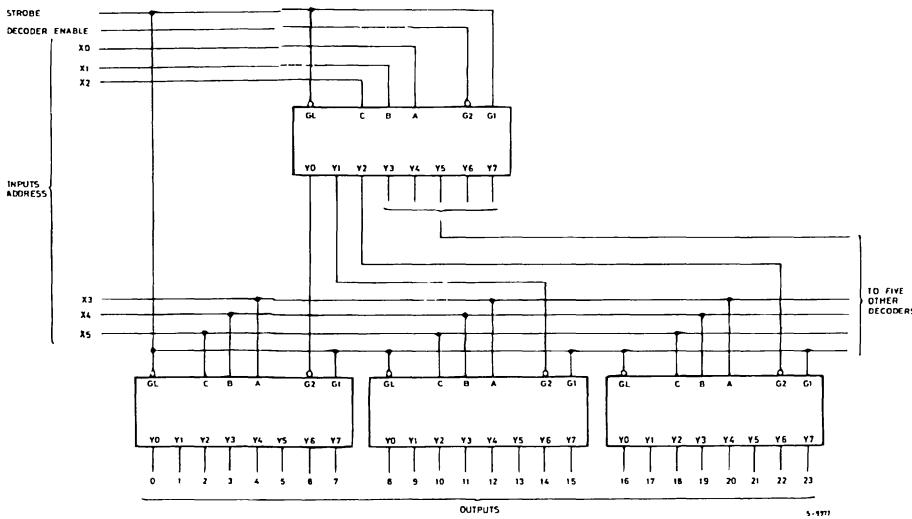
SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.



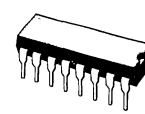
6 Line to 64 Line Decoder with Input Address Storage.

SGS-THOMSON MICROELECTRONICS

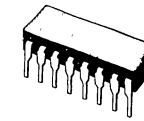
M54HC238
M74HC238

3 TO 8 LINE DECODER

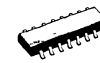
- HIGH SPEED
  t_{PD} = 14 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS238



B1R
(Plastic Package)



F1R
(Ceramic Package)



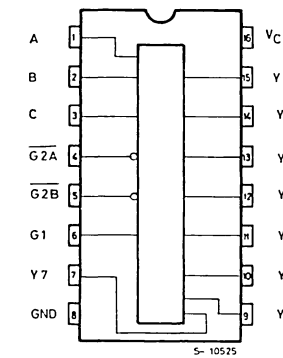
M1R
(Micro Package)

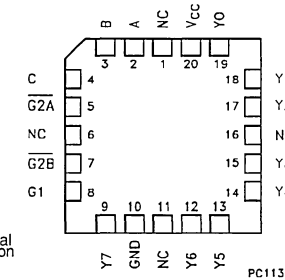
C1R
(Chip Carrier)

ORDER CODES :

M54HC238F1R	M74HC238M1R
M74HC238B1R	M74HC238C1R

PIN CONNECTIONS (top view)





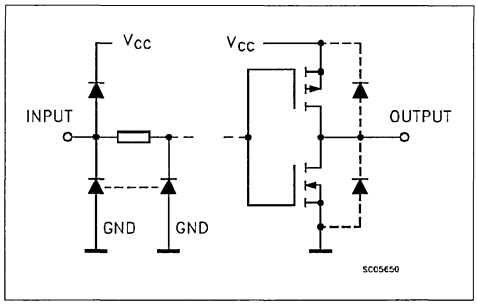
NC = No Internal Connection

DESCRIPTION

The M54/74HC238 is a high speed CMOS 3 to 8 line decoder fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. If the device is enabled, 3 binary select inputs (A, B and C) determine which one of outputs will go high. Enable input G1 is held "Low" or either $\overline{G2A}$ or $\overline{G2B}$ is held "High" decoding function is inhibited and all the 8 outputs go low. Three enable inputs are provided to ease cascade connection and application of this address decoder in memory systems.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

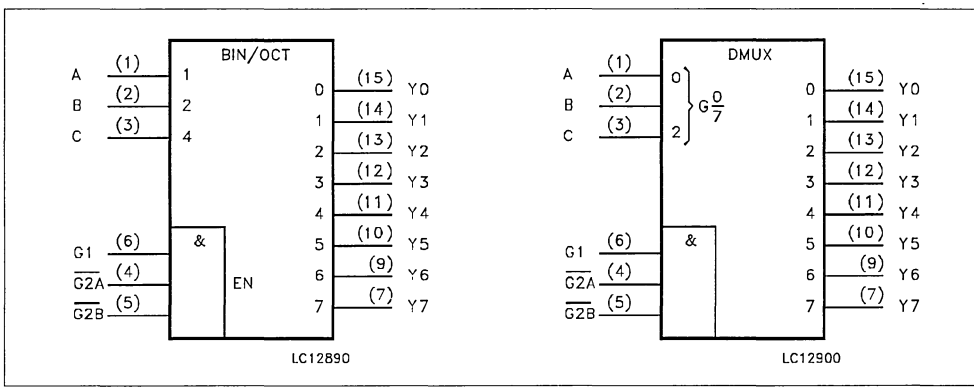
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3	A, B, C	Data Inputs
4, 5	$\overline{G2A}$ $\overline{G2B}$	Enable Input (Active LOW)
6	G1	Data Enable Input (Active HIGH)
15, 14, 13, 12, 11, 10, 9, 7	Y0 to Y7	Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS

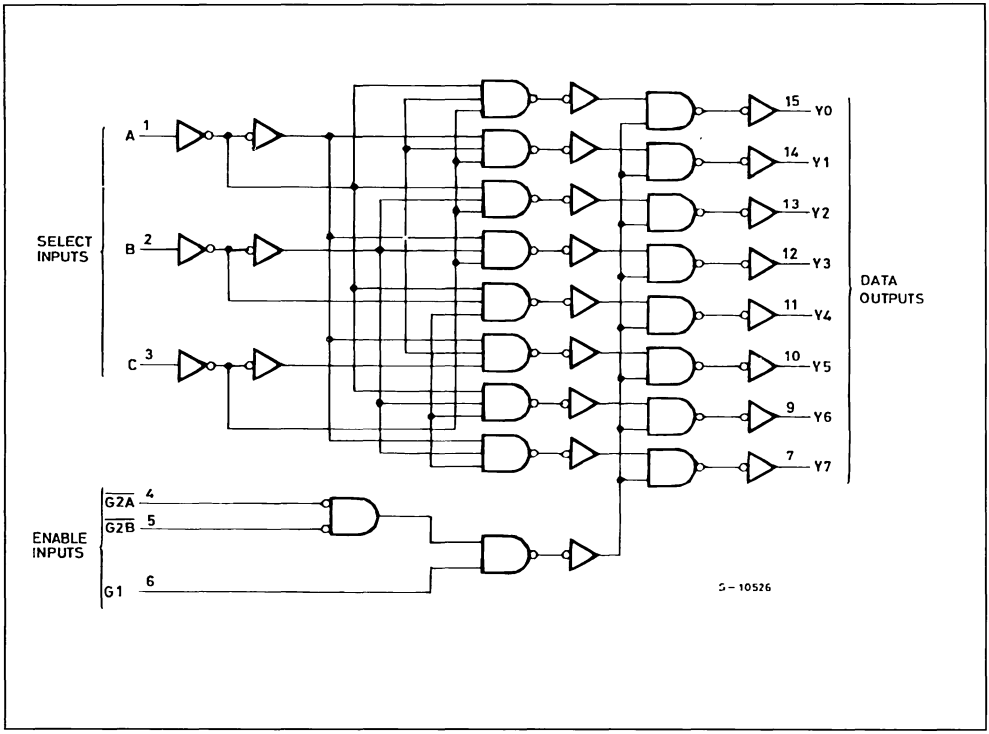


TRUTH TABLE

INPUTS						OUTPUS								SELECTED OUTPUT
ENABLE			SELECT											
$\overline{G2B}$	$\overline{G2A}$	G1	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	
X	X	L	X	X	X	L	L	L	L	L	L	L	L	NONE
X	H	X	X	X	X	L	L	L	L	L	L	L	L	NONE
H	X	X	X	X	X	L	L	L	L	L	L	L	L	NONE
L	L	H	L	L	L	H	L	L	L	L	L	L	L	Y0
L	L	H	L	L	H	L	H	L	L	L	L	L	L	Y1
L	L	H	L	H	L	L	L	H	L	L	L	L	L	Y2
L	L	H	L	H	H	L	L	L	H	L	L	L	L	Y3
L	L	H	H	L	L	L	L	L	L	H	L	L	L	Y4
L	L	H	H	L	H	L	L	L	L	L	H	L	L	Y5
L	L	H	H	H	L	L	L	L	L	L	L	H	L	Y6
L	L	H	H	H	H	L	L	L	L	L	L	L	H	Y7

X: Don't Care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

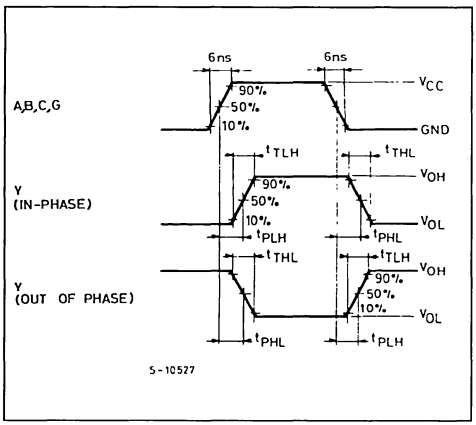
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

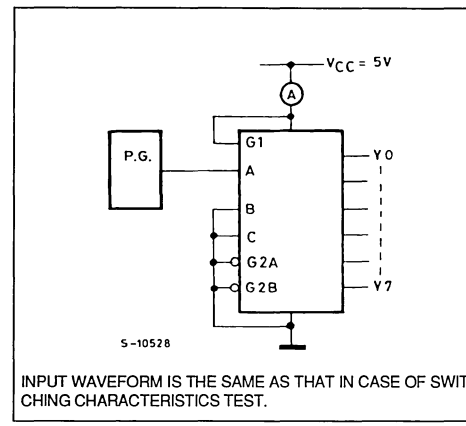
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C - Y)	2.0			50	150		190		225	ns
		4.5			17	30		38		45	
		6.0			15	26		32		38	
t_{PLH} t_{PHL}	Propagation Delay Time (G1 - Y)	2.0			50	150		190		225	ns
		4.5			17	30		38		45	
		6.0			15	26		32		38	
t_{PLH} t_{PHL}	Propagation Delay Time (G2 - Y)	2.0			50	150		190		225	ns
		4.5			17	30		38		45	
		6.0			15	26		32		38	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				53						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



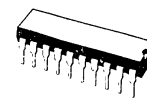
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

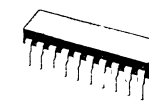
M54HC240/241/244
M74HC240/241/244

OCTAL BUS BUFFER WITH 3 STATE OUTPUTS
HC240: INVERTED - HC241/244 NON INVERTED

- HIGH SPEED
  t_{PD} = 10 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{INL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS240/241/244



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

DESCRIPTION

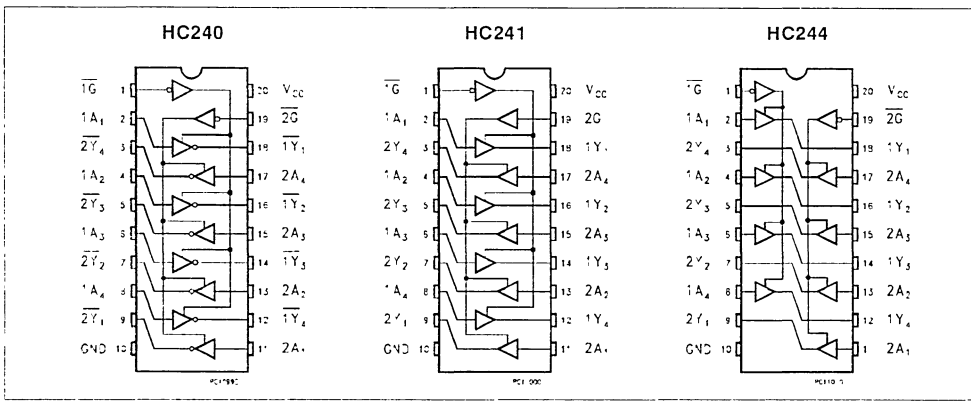
The M54/74HC240, HC241 and HC244 are high speed CMOS OCTAL BUS BUFFERs fabricated in silicon gate C^2MOS technology.

They have the same high speed performance of LSTTL combined with true CMOS low power consumption.

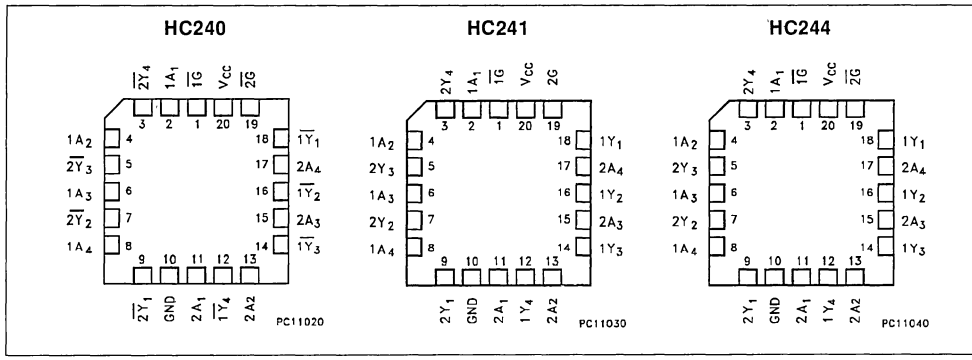
The designer has a choise of select combination of inverting and non-inverting outputs, symmetrical $\overline{G}$ (active low output control) input, and complementary G and $\overline{G}$ inputs. Each control input governs four BUS BUFFERs.

These devices are designed to be used with 3 state memory address drivers, etc. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

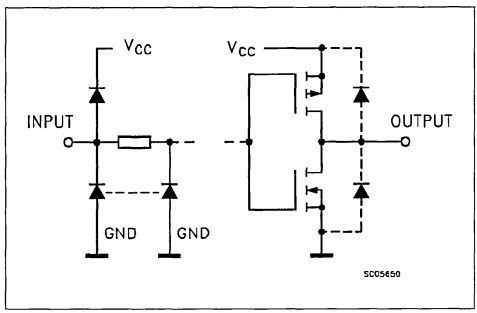
PIN CONNECTION (top view)



CHIP CARRIER



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION (HC240)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{1G}$	Output Enable Input
2, 4, 6, 8	1A1 to 1A4	Data Inputs
9, 7, 5, 3	$\overline{2Y1}$ to $\overline{2Y4}$	Data Outputs
11, 13, 15, 17	2A1 to 2A4	Data Inputs
18, 16, 14, 12	$\overline{1Y1}$ to $\overline{1Y4}$	Data Outputs
19	$\overline{2G}$	Output Enabel Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

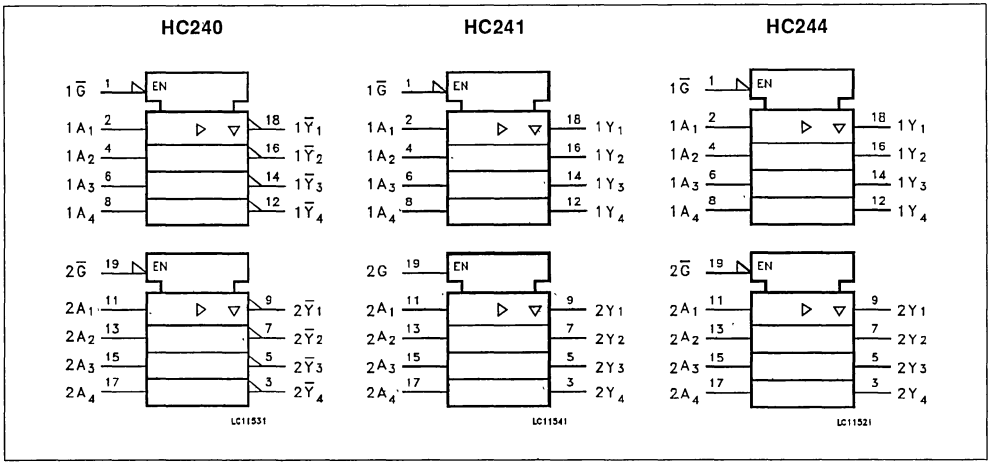
PIN DESCRIPTION (HC241)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{1G}$	Output Enable Input
2, 4, 6, 8	1A1 to 1A4	Data Inputs
9, 7, 5, 3	2Y1 to 2Y4	Data Outputs
11, 13, 15, 17	2A1 to 2A4	Data Inputs
18, 16, 14, 12	1Y1 to 1Y4	Data Outputs
19	2G	Output Enabel Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

PIN DESCRIPTION (HC244)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{1G}$	Output Enable Input
2, 4, 6, 8	1A1 to 1A4	Data Inputs
9, 7, 5, 3	2Y1 to 2Y4	Data Outputs
11, 13, 15, 17	2A1 to 2A4	Data Inputs
18, 16, 14, 12	1Y1 to 1Y4	Data Outputs
19	$\overline{2G}$	Output Enabel Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS

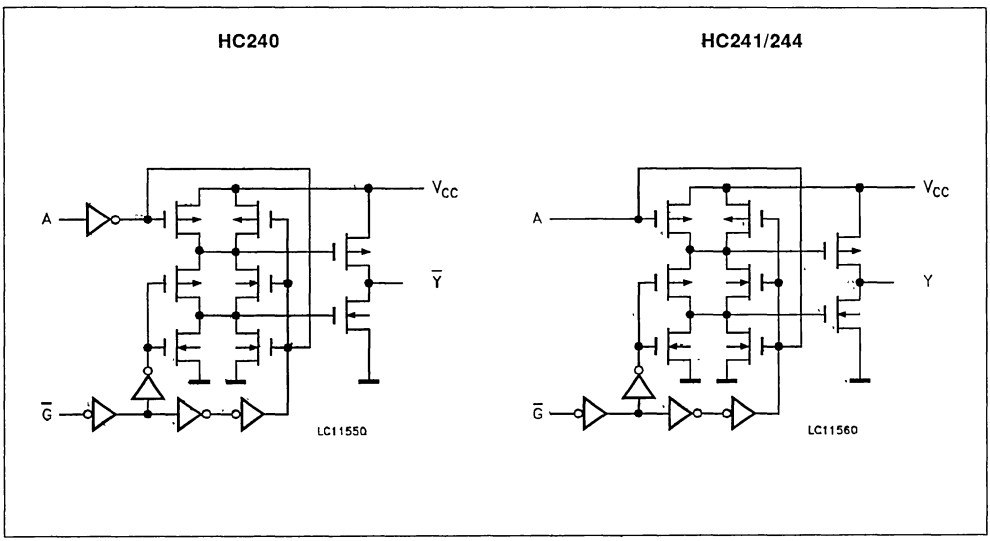


TRUTH TABLE

INPUT			OUTPUT		
$\overline{G}$	G (HC241)	An	$\overline{Yn}$ (HC240)	Yn (HC241)	Yn (HC244)
L	H	L	H	L	L
L	H	H	L	H	H
H	L	X	Z	Z	Z

X: "H" or "L"
Z: High impedance

CIRCUIT SCHEMATIC (1/8 PACKAGE)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied

(*) 500 mW ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series		-55 to +125	°C
	M74HC Series		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

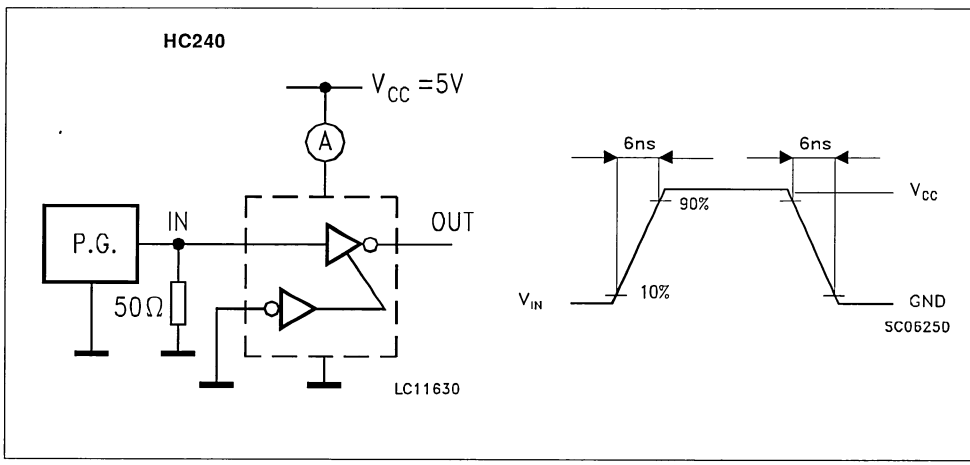
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75		90	ns
		4.5				7	12		19		18	
		6.0				6	10		13		15	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0	50			36	90		115		135	ns
		4.5				12	18		23		27	
		6.0				10	15		20		23	
		2.0	150			51	130		165		195	ns
		4.5				17	26		33		39	
		6.0				14	22		28		33	
t_{PZL} t_{PZH}	Output Enable Time	2.0	50	R_L = 1KΩ		48	125		155		190	ns
		4.5				16	25		31		38	
		6.0				14	21		26		32	
		2.0	150	R_L = 1KΩ		63	165		205		250	ns
		4.5				21	33		41		50	
		6.0				18	28		35		43	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0	50	R_L = 1KΩ		32	125		155		190	ns
		4.5				15	25		31		38	
		6.0				14	21		26		32	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{OUT}	Output Capacitance					10						pF
C_{PD} (*)	Power Dissipation Capacitance		HC240 HC241/244			31 33						pF

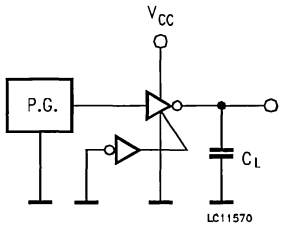
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per circuit)

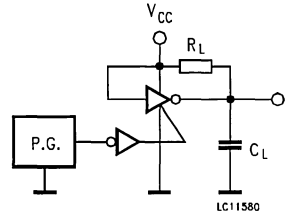
TEST CIRCUIT I_{CC} (Opr.)

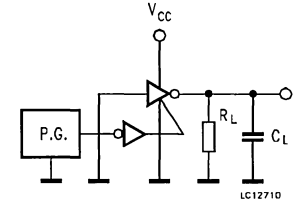


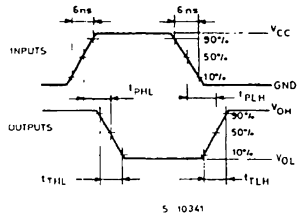
SWITCHING CHARACTERISTICS TEST CIRCUIT

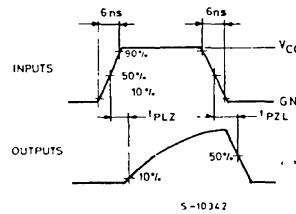
HC240

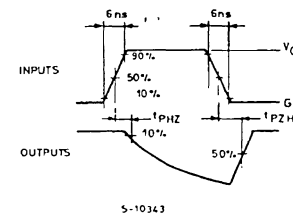




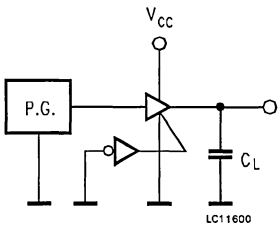


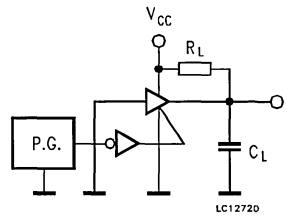


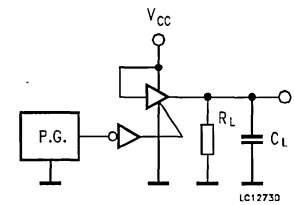


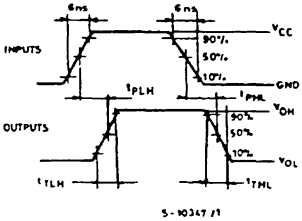


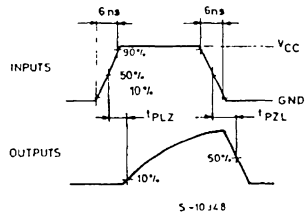
HC241/HC244

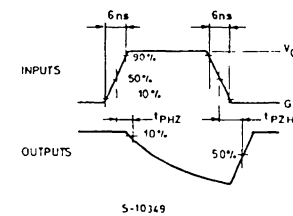






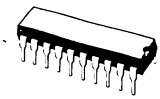




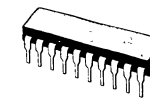


OCTAL BUS BUFFER WITH 3 STATE OUTPUTS
HC240HV: INVERTED - HC241HV NON INVERTED

- HIGH SPEED
  t_{PD} = 12 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{INL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- SAME FUNCTION OF HC240/241 PLUS HIGH TO LOW LEVEL LOGIC CONVERSION CAPABILITY
- LATCH UP FREE OPERATION ALSO WHEN V_{IH} IS HIGHER THAN V_{CC}



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

ORDER CODES :
M54HCXXXHVF1R M74HCXXXHVM1R
M74HCXXXHVB1R

DESCRIPTION

The M54/74HC240HV and HC241HV are high speed CMOS OCTAL BUS BUFFERs fabricated in silicon gate C^2MOS technology.

They have the same high speed performance of LSTTL combined with true CMOS low power consumption.

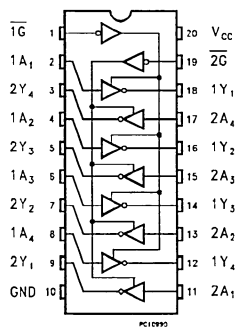
Performing the same function of their non HV counterpart, they have a particularl input configuration which allows all inputs to be driven by logic levels exceeding the supply voltage.

This makes them particularly suitable in systems where mixed 3V/5V logic devices need to be interfaced.

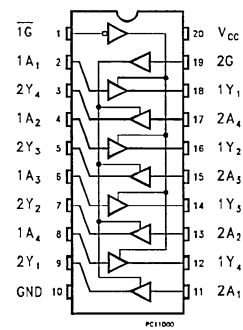
All inputs are equipped with protection circuits against static discharge and transient excess voltage.
NOTE: BOTH DEVICES DO NOT MEET 2KV ESD RATING

PIN CONNECTION (top view)

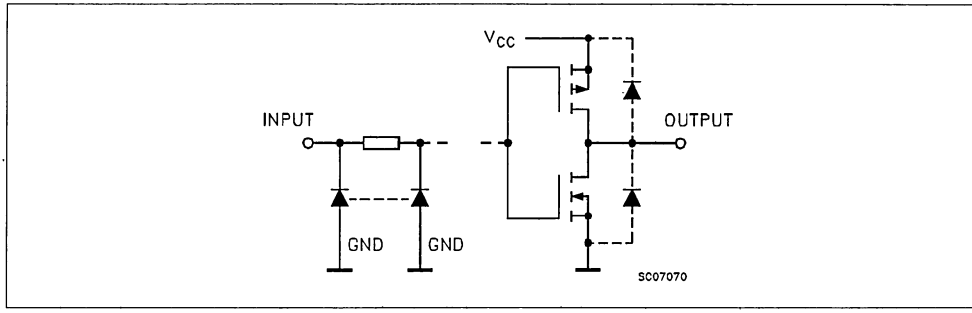
HC240HV



HC241HV



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION (HC240HV)

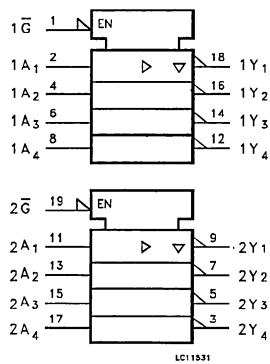
PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{1G}$	Output Enable Input
2, 4, 6, 8	1A1 to 1A4	Data Inputs
9, 7, 5, 3	2Y1 to 2Y4	Data Outputs
11, 13, 15, 17	2A1 to 2A4	Data Inputs
18, 16, 14, 12	1Y1 to 1Y4	Data Outputs
19	$\overline{2G}$	Output Enabel Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

PIN DESCRIPTION (HC241HV)

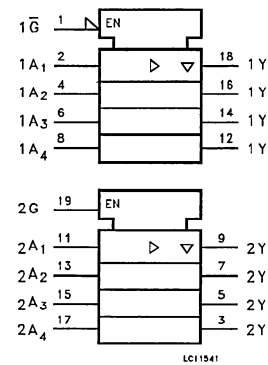
PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{1G}$	Output Enable Input
2, 4, 6, 8	1A1 to 1A4	Data Inputs
9, 7, 5, 3	2Y1 to 2Y4	Data Outputs
11, 13, 15, 17	2A1 to 2A4	Data Inputs
18, 16, 14, 12	1Y1 to 1Y4	Data Outputs
19	2G	Output Enabel Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS

HC240HV



HC241HV



TRUTH TABLE

INPUT			OUTPUT	
$\overline{G}$	G (HC241)	An	$\overline{Yn}$ (HC240HV)	Yn (HC241HV)
L	H	L	H	L
L	H	H	L	H
H	L	X	Z	Z

X: "H" or "L"
Z. High impedance

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to 13	V
V_I	DC Input Voltage	-0.5 to 13	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	- 20	mA
I_{OK}	DC Output Diode Current	± 100	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 100	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to 12	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

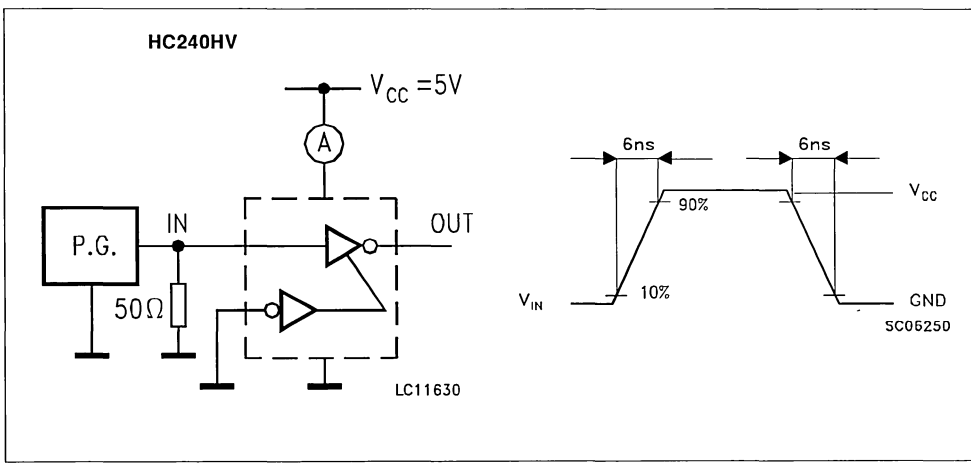
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	12.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{IH}	Input Leakage Current	2.0	V_I = 12 V				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	12.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5		±10	µA
I_{CC}	Quiescent Supply Current	12.0	V_I = V_{CC} or GND				8		80		160	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75		90	ns
		4.5				7	12		19		18	
		6.0				6	10		13		15	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0	50			40	110		140		165	ns
		4.5				13	22		28		33	
		6.0				11	19		24		28	
		2.0	150			52	135		170		205	ns
		4.5				17	27		34		41	
		6.0				14	23		29		35	
t_{PZL} t_{PZH}	Output Enable Time	2.0	50	R_L = 1KΩ		52	135		170		205	ns
		4.5				17	27		34		41	
		6.0				14	23		29		35	
		2.0	150	R_L = 1KΩ		63	165		205		250	ns
		4.5				21	33		41		50	
		6.0				18	28		35		43	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0	50	R_L = 1KΩ		40	135		170		205	ns
		4.5				19	27		34		41	
		6.0				15	23		29		35	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{OUT}	Output Capacitance					10						pF
C_{PD} (*)	Power Dissipation Capacitance					33						pF

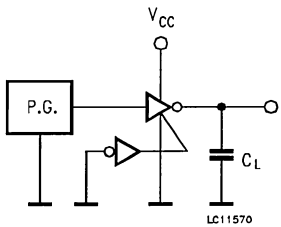
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per circuit)

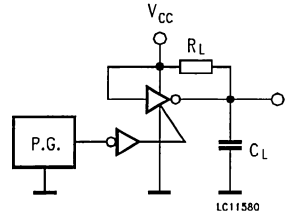
TEST CIRCUIT I_{CC} (Opr.)

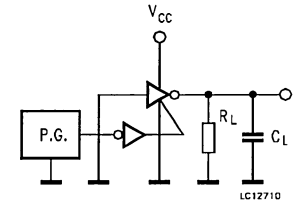


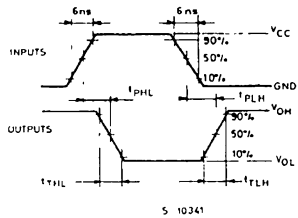
SWITCHING CHARACTERISTICS TEST CIRCUIT

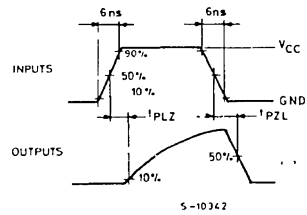
HC240HV

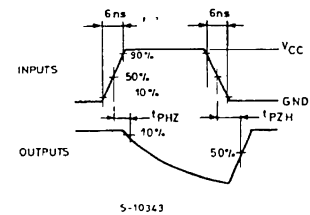




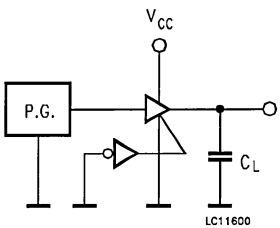


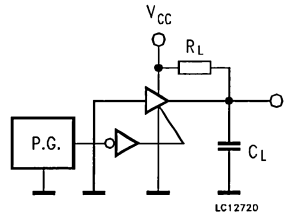


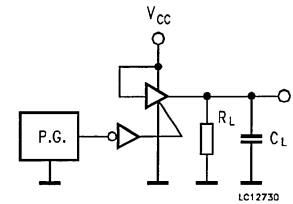


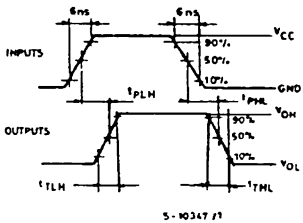


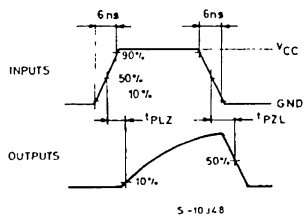
HC241HV

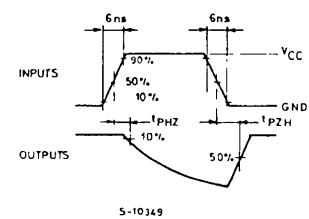








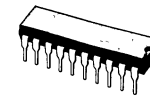




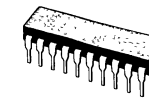
M54HCT240/241/244
M74HCT240/241/244

OCTAL BUS BUFFER WITH 3 STATE OUTPUTS
HCT240: INVERTED - HCT241/244 NON INVERTED

- HIGH SPEED
  t_{PD} = 13 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) at T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS240/241/244



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

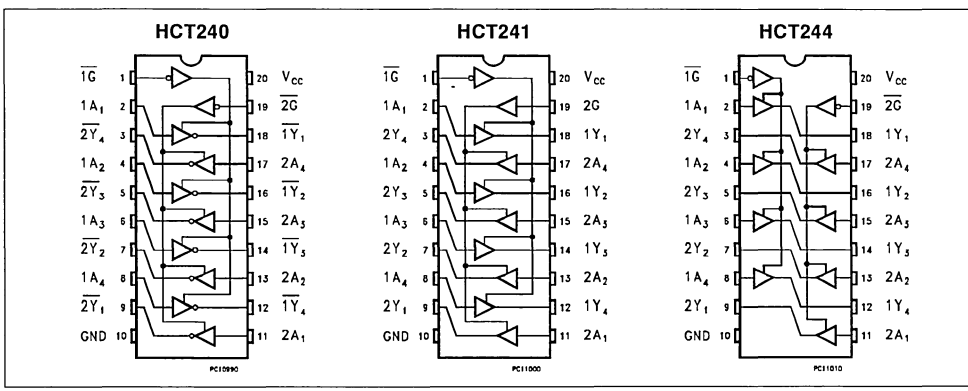
ORDER CODES :

M54HCTXXXF1R M74HCTXXXM1R
M74HCTXXXB1R M74HCTXXXC1R

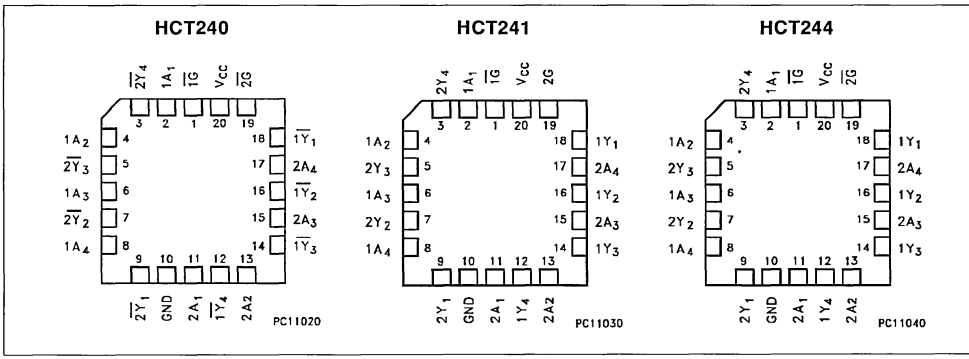
DESCRIPTION

The M54/74HCT240, HCT241 and HCT244 are high speed CMOS OCTAL BUS BUFFERs fabricated in silicon gate C^2MOS technology.
They have the same high speed performance of LSTTL combined with true CMOS low power consumption. The designer has a choise of select combination of inverting and non-inverting outputs, symmetrical $\overline{G}$ (active low output control) input, and complementary G and $\overline{G}$ inputs. Each control input governs four BUS BUFFERs.
This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components.
They are also plug in replacements for LSTTL devices giving a reduction of power consumption. These devices are designed to be used with 3 state memory address drivers, etc.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

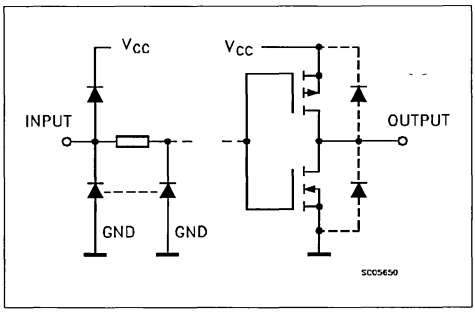
PIN CONNECTION (top view)



CHIP CARRIER



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION (HCT240)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{1G}$	Output Enable Input
2, 4, 6, 8	1A1 to 1A4	Data Inputs
9, 7, 5, 3	2Y1 to 2Y4	Data Outputs
11, 13, 15, 17	2A1 to 2A4	Data Inputs
18, 16, 14, 12	1Y1 to 1Y4	Data Outputs
19	$\overline{2G}$	Output Enabel Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

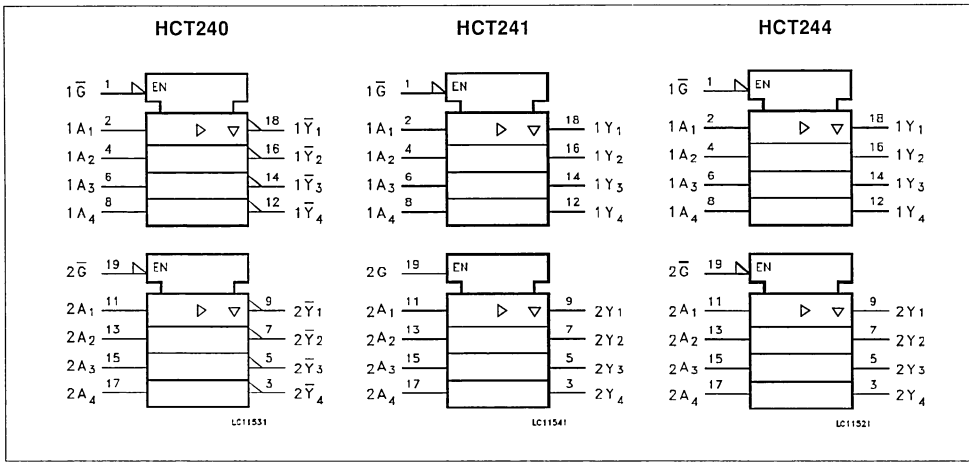
PIN DESCRIPTION (HCT241)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{1G}$	Output Enable Input
2, 4, 6, 8	1A1 to 1A4	Data Inputs
9, 7, 5, 3	2Y1 to 2Y4	Data Outputs
11, 13, 15, 17	2A1 to 2A4	Data Inputs
18, 16, 14, 12	1Y1 to 1Y4	Data Outputs
19	2G	Output Enabel Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

PIN DESCRIPTION (HCT244)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{1G}$	Output Enable Input
2, 4, 6, 8	1A1 to 1A4	Data Inputs
9, 7, 5, 3	$\overline{2Y1}$ to $\overline{2Y4}$	Data Outputs
11, 13, 15, 17	2A1 to 2A4	Data Inputs
18, 16, 14, 12	$\overline{1Y1}$ to $\overline{1Y4}$	Data Outputs
19	$\overline{2G}$	Output Enabel Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS

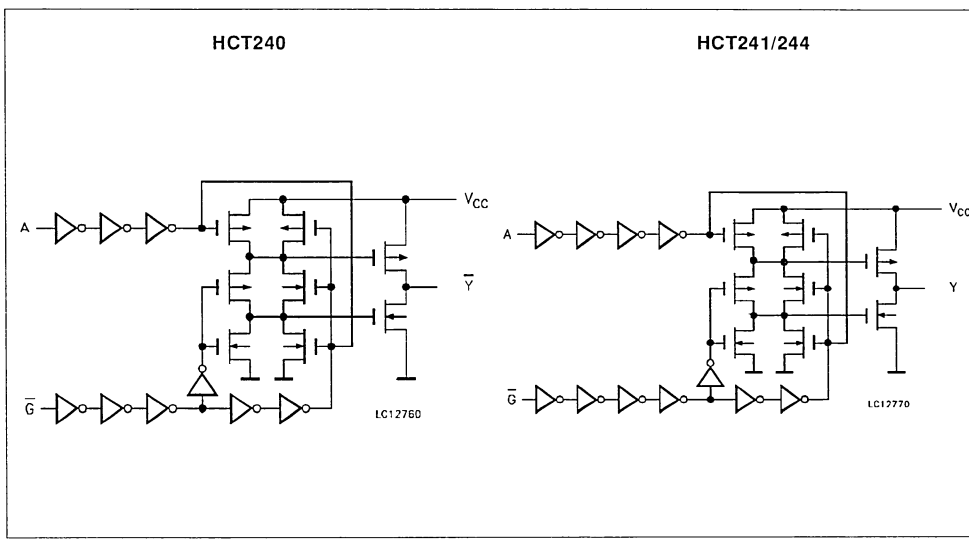


TRUTH TABLE

INPUT			OUTPUT		
$\overline{G}$	G (HCT241)	An	$\overline{Yn}$ (HCT240)	Yn (HCT241)	Yn (HCT244)
L	H	L	H	L	L
L	H	H	L	H	H
H	L	X	Z	Z	Z

X: "H" or "L"
Z: High impedance

CIRCUIT SCHEMATIC (1/8 PACKAGE)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

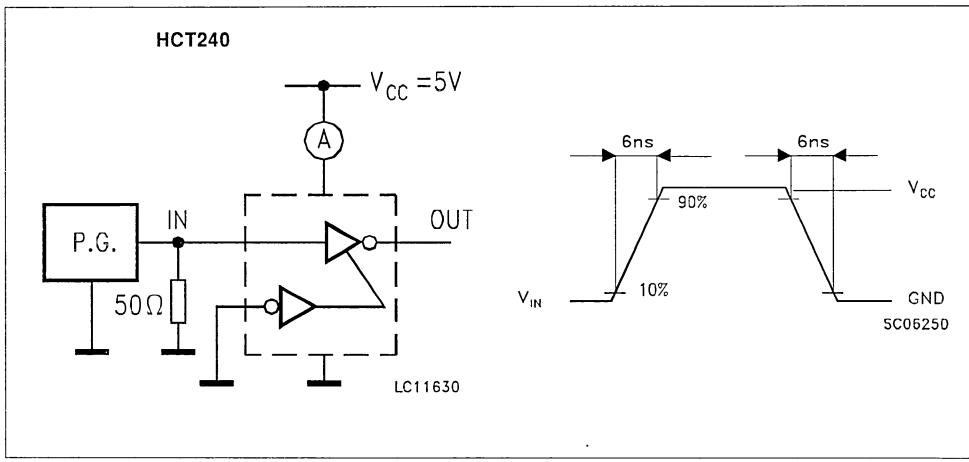
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-6.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 6.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				4		40		80	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or 2.4V Other Inputs at V_{CC} or GND				2.0		2.9		3.0	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

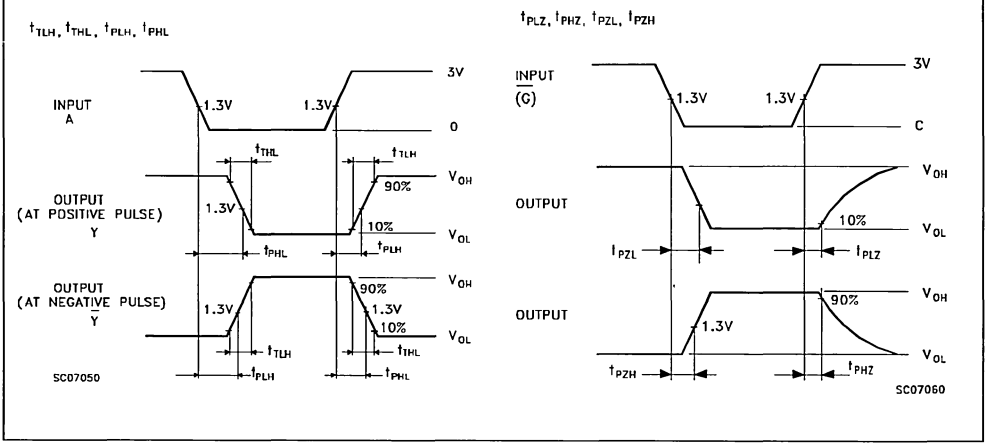
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5	50			7	12		15		18	ns
t_{PLH} t_{PHL}	Propagation Delay Time	4.5	50			15	22		28		33	ns
		4.5	150			21	30		38		45	ns
t_{PLH} t_{PHL}	Propagation Delay Time	4.5	50			15	25		31		38	ns
		4.5	150			21	33		41		50	ns
t_{PZL} t_{PZH}	Output Enable Time	4.5	50	R_L = 1KΩ		17	30		38		45	ns
		4.5	150	R_L = 1KΩ		23	38		48		57	ns
t_{PLZ} t_{PHZ}	Output Disable Time	4.5	50	R_L = 1KΩ		16	30		38		45	ns
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{OUT}	Output Capacitance					10						pF
C_{PD} (*)	Power Dissipation Capacitance		HCT240 HCT241/244			33 31						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit) Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per circuit)

TEST CIRCUIT I_{CC} (Opr.)

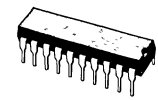


SWITCHING CHARACTERISTICS TEST WAVEFORM

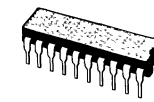


OCTAL BUS BUFFERS WITH PULL-UP INPUT NETWORK

- HIGH SPEED
  t_{PD} = 14 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CCH} = 200 µA (TYP.) at T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- CURRENT SOURCES ON DATA INPUTS ELIMINATE THE NEED OF EXTERNAL PULL-UP RESISTORS
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS240/241/244



B1R
(Plastic Package)



F1R
(Ceramic Package)

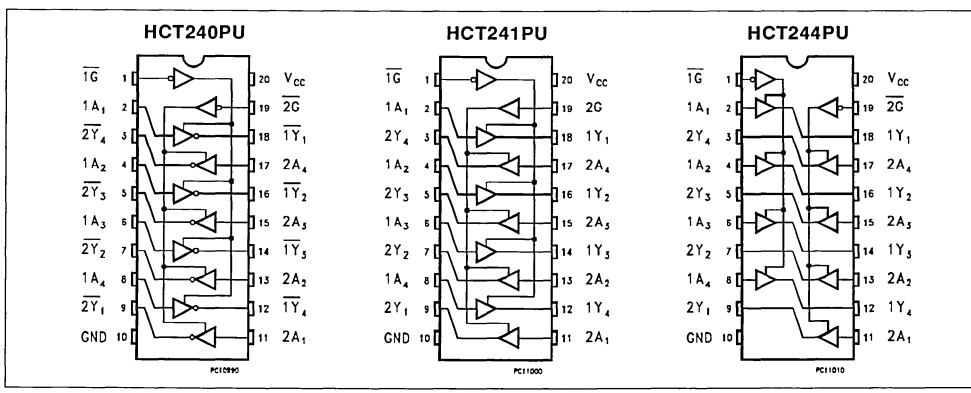
M1R
(Micro Package)

ORDER CODES :
M54HCTXXXPUF1R M74HCTXXXPUM1R
M74HCTXXXPUB1R

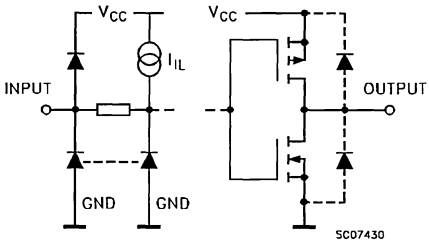
DESCRIPTION

The M54/74HCT240, HCT241 and HCT244 are high speed CMOS OCTAL BUS BUFFERs fabricated in silicon gate C^2MOS technology.
They have the same high speed performance of their non-PU counterpart, plus a unique input topology which incorporates a constant current source for each data input. This results is a small IIL (-150 µA Typ.) wich can fix any data input in the HIGH Logic Level when it is left floating, thus eliminating the need of external pull-up resistor network.
This features makes these devices particularly suitable in all applications where a data bus needs to be interfaced to manual controls like: rotary selectors, keyboards, dip-switches, etc. The inputs are compatible with TTL, NMOS and CMOS output voltage levels. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. All

PIN CONNECTION (top view)



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION (HCT240PU)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{1G}$	Output Enable Input
2, 4, 6, 8	1A1 to 1A4	Data Inputs
9, 7, 5, 3	2Y1 to 2Y4	Data Outputs
11, 13, 15, 17	2A1 to 2A4	Data Inputs
18, 16, 14, 12	1Y1 to 1Y4	Data Outputs
19	$\overline{2G}$	Output Enabel Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

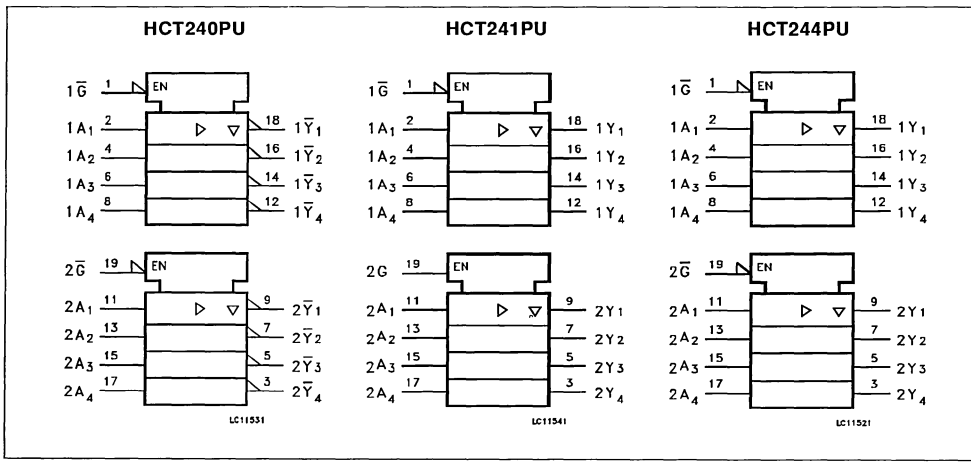
PIN DESCRIPTION (HCT241PU)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{1G}$	Output Enable Input
2, 4, 6, 8	1A1 to 1A4	Data Inputs
9, 7, 5, 3	2Y1 to 2Y4	Data Outputs
11, 13, 15, 17	2A1 to 2A4	Data Inputs
18, 16, 14, 12	1Y1 to 1Y4	Data Outputs
19	2G	Output Enabel Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

PIN DESCRIPTION (HCT244PU)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{1G}$	Output Enable Input
2, 4, 6, 8	1A1 to 1A4	Data Inputs
9, 7, 5, 3	$\overline{2Y1}$ to $\overline{2Y4}$	Data Outputs
11, 13, 15, 17	2A1 to 2A4	Data Inputs
18, 16, 14, 12	$\overline{1Y1}$ to $\overline{1Y4}$	Data Outputs
19	$\overline{2G}$	Output Enabel Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS

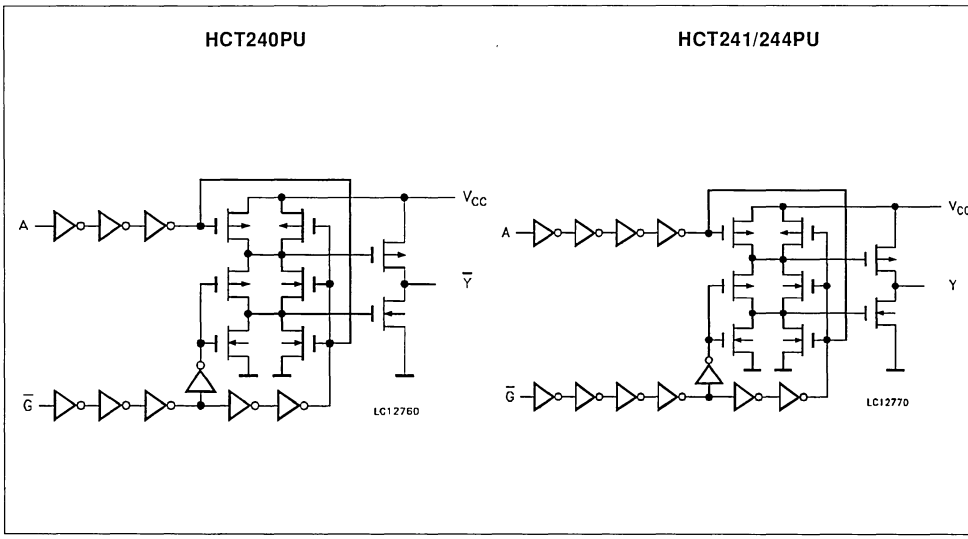


TRUTH TABLE

INPUT			OUTPUT		
$\overline{G}$	G (HCT241)	An	$\overline{Yn}$ (HCT240)	Yn (HCT241)	Yn (HCT244)
L	H	L	H	L	L
L	H	H	L	H	H
H	L	X	Z	Z	Z

X "H" or "L"
Z· High impedance

CIRCUIT SCHEMATIC (1/8 PACKAGE)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

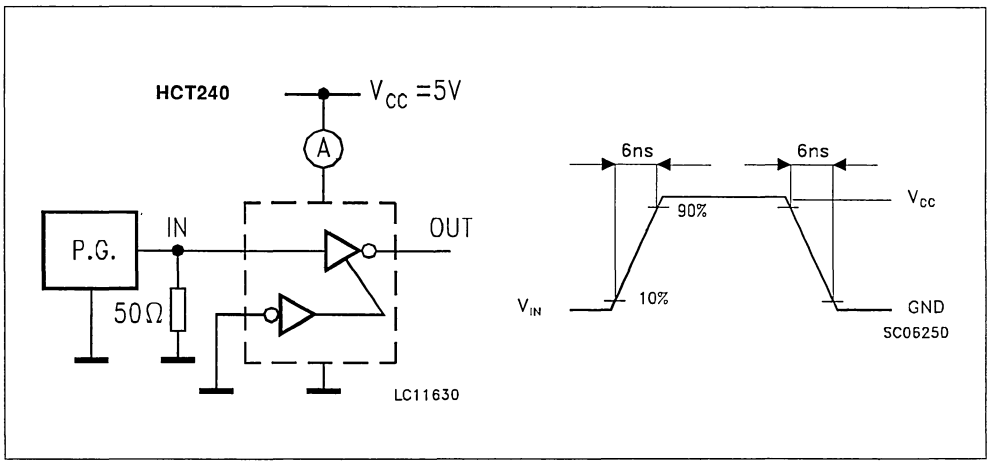
DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC.		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage.	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-6.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 6.0 mA		0.17	0.26		0.33		0.4	
I_{IL}	Input Low Current	4.5	V_I = 0.4 V		-50	-130	-250	-30	-350	-20	-400	mA
		5.5			-50	-180	-300	-30	-400	-20	-450	
I_{IN}	input Leakage Current (EN inp.)	5.5	V_{IN} = V_{CC} or GND				±0.1		±1.0		±1.0	µA
I_{OZ}	3 State Output Off State Current	5.5	V_{IN} = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5.0		±10	µA
I_{CCH}	Quiescent Supply Current	5.5	V_I = V_{CC}			200	600		800		1000	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or 2.4V Other Inputs at V_{CC} or GND				3.0		3.9		4.0	mA

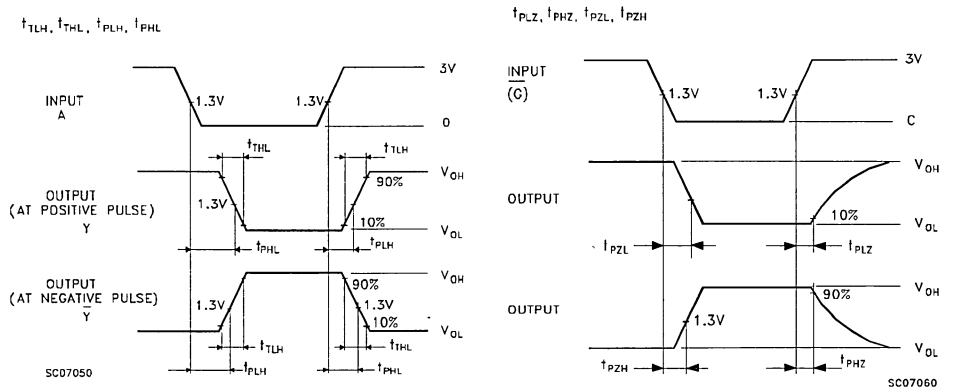
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5	50			7	12		15		18	ns
t_{PLH} t_{PHL}	Propagation Delay Time (for 240)	4.5	50			18	28		35		42	ns
		4.5	150			22	34		43		51	ns
t_{PLH} t_{PHL}	Propagation Delay Time (for 241/244)	4.5	50			20	31		39		47	ns
		4.5	150			24	37		46		56	ns
t_{PZL} t_{PZH}	Output Enable Time	4.5	50	R_L = 1KΩ		22	34		43		51	ns
		4.5	150	R_L = 1KΩ		26	40		50		60	ns
t_{PLZ} t_{PHZ}	Output Disable Time	4.5	50	R_L = 1KΩ		25	36		45		54	ns
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance					100						pF

TEST CIRCUIT I_{CC} (Opr.)

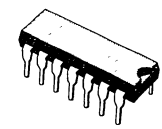


SWITCHING CHARACTERISTICS TEST WAVEFORM

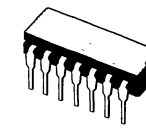


QUAD BUS TRANSCEIVER (3-STATE)

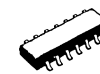
- HIGH SPEED
  t_{PD} = 9 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT 25 °C
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- SYMMETRICAL OUTPUT IMPEDANCE
  $I_{OL} = |I_{OH}|$ = 6 mA (MIN.)
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS242/243



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

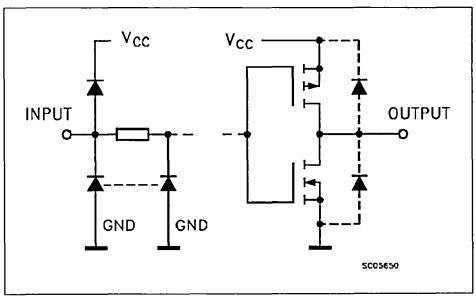
ORDER CODES :

M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

DESCRIPTION

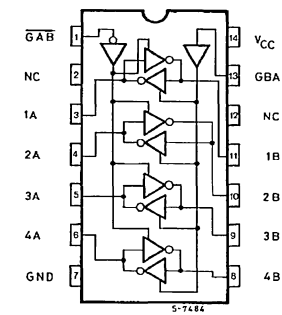
The M54/74HC242/243 are high speed CMOS QUAD BUS TRANSCEIVER (3-STATE) FABRICATED IN SILICON GATE C^2MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. The HC242/243 are 3 STATE bi-directional inverting and non-inverting buffers and are intended for two-way asynchronous communication between data buses. They are high drive current outputs which enable high speed operation when driving large bus capacitances. Each device has one active high enable (GBA), and one active low enable ($\overline{GAB}$). GBA enables the A outputs and $\overline{GAB}$ enables the B outputs. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT

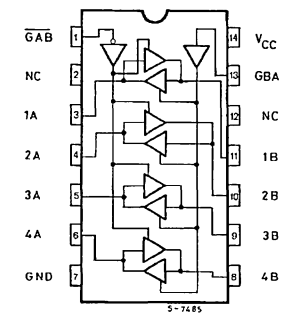


PIN CONNECTIONS (top view)

HC242

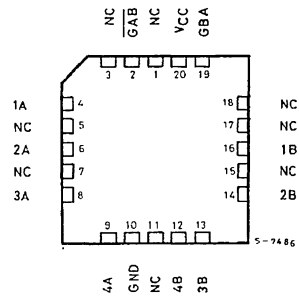


HC243



NC =
No Internal
Connection

CHIP CARRIER



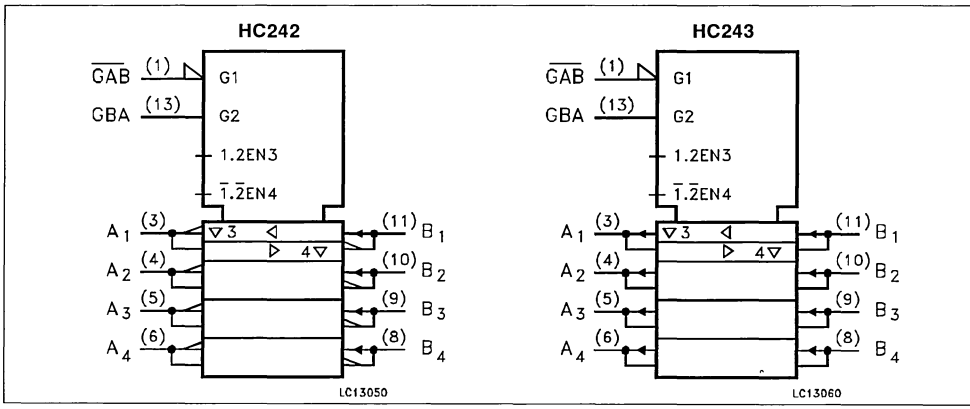
TRUTH TABLE

INPUTS		FUNCTION		OUTPUTS	
$\overline{GAB}$	GBA	A BUS	B BUS	HC242	HC243
H	H	OUTPUT	INPUT	$A = \overline{B}$	A = B
L	L	INPUT	OUTPUT	$B = \overline{A}$	B = A
H	L	HIGH IMPEDANCE		Z	Z
L	H	HIGH IMPEDANCE		Z	Z

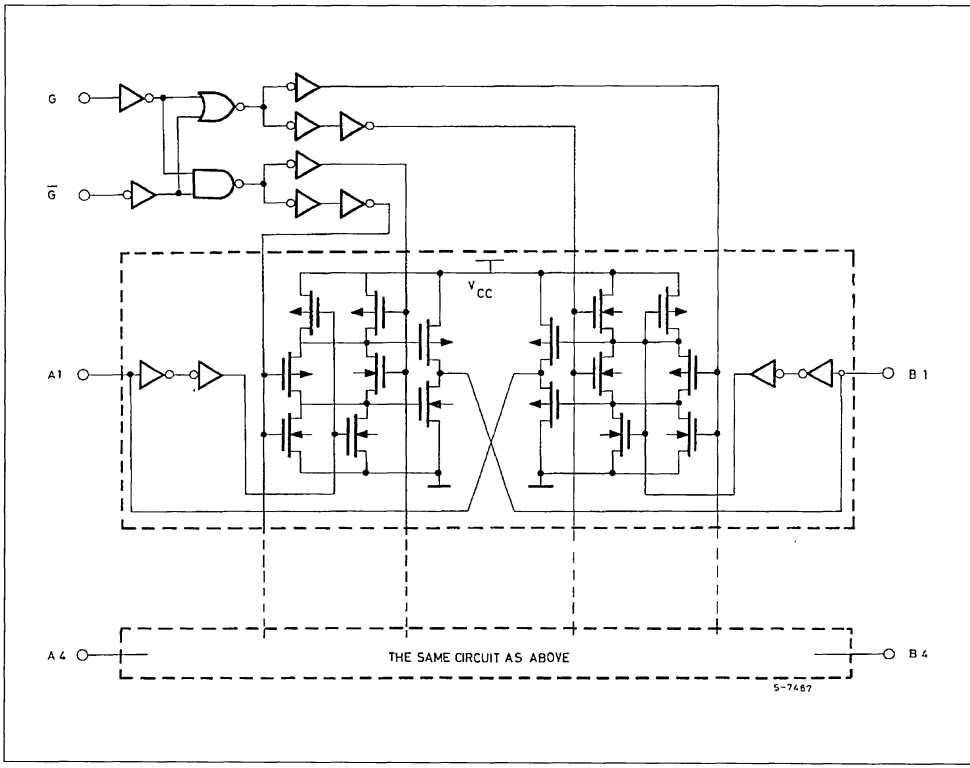
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{GAB}$	Output Enable Input (active LOW)
2, 12	NC	Not connected
3, 4, 5, 6	1A to 4A	Data Inputs/Outputs
11, 10, 9, 8	1B to 4B	Data Inputs/Outputs
13	GBA	Output Enable Input
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS



CIRCUIT DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series		-55 to +125	°C
	M74HC Series		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

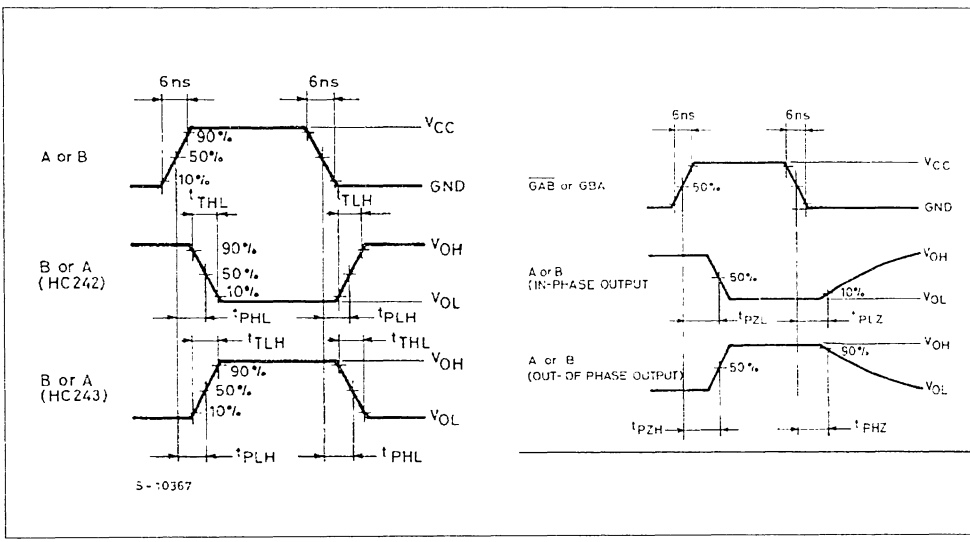
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off-state Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6$ ns)

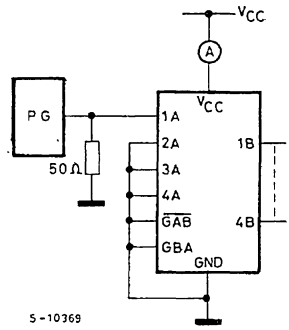
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0	50			39	90		115		135	ns
		4.5				13	18		23		27	
		6.0				11	15		20		23	
		2.0	150			51	145		180		220	ns
		4.5				17	29		36		44	
		6.0				14	25		31		37	
t_{PZL} t_{PZH}	3 State Output Enable Time	2.0	50	R_L = 1 KΩ		57	145		180		220	ns
		4.5				18	29		36		44	
		6.0				15	25		31		37	
		2.0	150	R_L = 1 KΩ		70	175		220		265	ns
		4.5				22	35		44		53	
		6.0				19	30		37		45	
t_{PLZ} t_{PHZ}	3 State Output Disable Time	2.0	50	R_L = 1 KΩ		45	150		190		225	ns
		4.5				20	30		38		45	
		6.0				17	26		32		38	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance		for HC242 for HC243			30 35						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit) Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



C_{CP} CALCULATION

C_{PD} is to be calculated with the following formula by using the measured value of ICC (Opr.) in the test circuit opposite

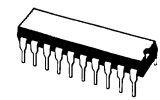
$$C_{PD} = \frac{I_{CC}\,(Opr.)}{f_{IN} \times V_{CC}}$$

In determining the typical value of CPD, a relatively high frequency of 1MHz was applied to fIN, in order to eliminate any error caused by the quiescent supply current.

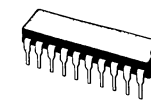
M54/74HC245/640/643

OCTAL BUS TRANSCEIVER (3-STATE): HC245 NON INVERTING HC640 INVERTING, HC643 INVERTING/NON INVERTING

- HIGH SPEED
  t_{PD} = 10 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{INL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS245/640/643



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

DESCRIPTION

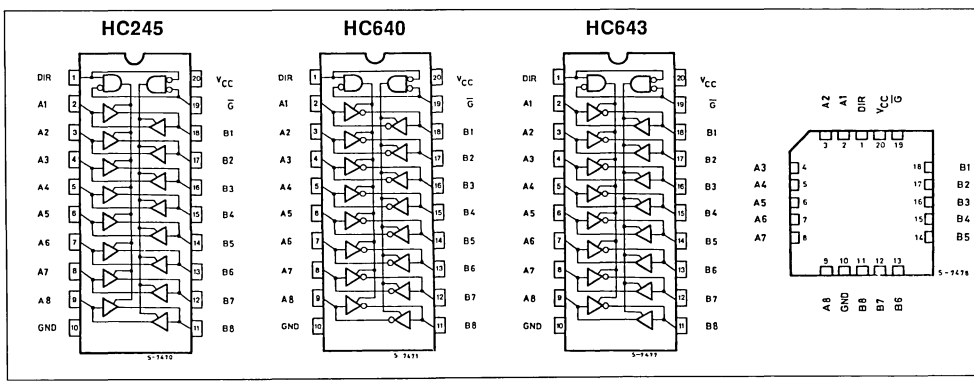
The M54/74HC245, HC640 and HC643 utilise silicon gate C2MOS technology to achive operating speeds equivalent to LSTTL devices.

Along with the low power dissipation and high noise immunity of standards C^2MOS integrated circuit, it possesses the capability to drive 15 LSTTL loads. These IC's are intended for two-way asynchronous communication between data buses, and the direction of data trasmission is determined by DIR input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

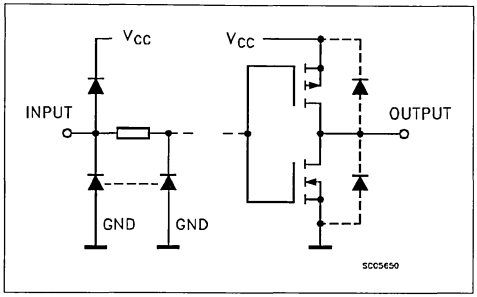
All input are equipped with protection circuits against static discharge and transient discharge and transient excess voltage.

IT IS PROHIBITED TO APPLY A SIGNAL TO A BUS TERMINAL WHEN IT IS IN OUTPUT MODE AND WHEN A BUS THERMINAL IS FLOATING (HIGH IMPEDANCE STATE), IT IS REQUESTED TO FIX THE INPUT LEVEL BY MEANS OF EXTERNAL PULL DOWN OR PULL UP RESISTOR.

PIN CONNECTION (top view)



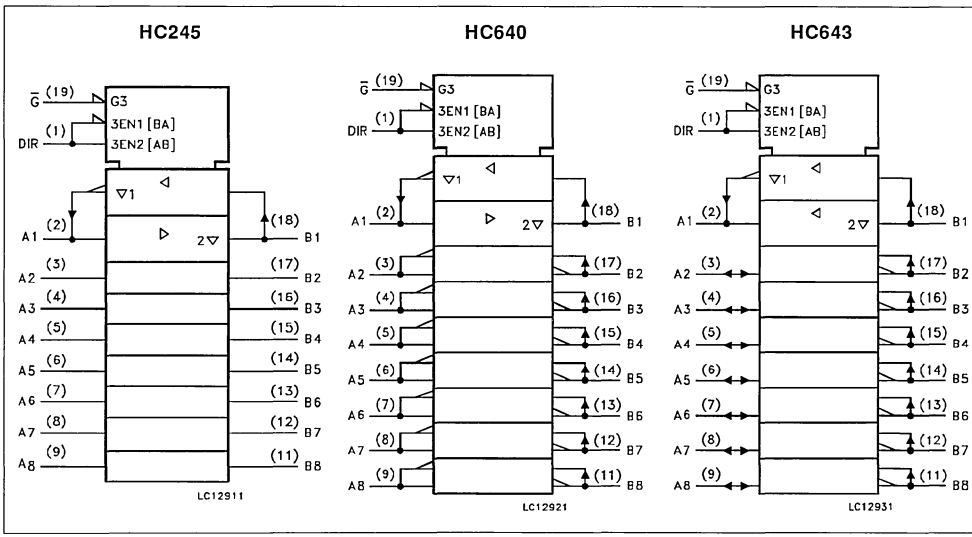
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	DIR	Directional Control
2, 3, 4, 5, 6, 7, 8, 9	A1 to A8	Data Inputs/Outputs
18, 17, 16, 15, 14, 13, 12, 11	B1 to B8	Data Inputs/Outputs
19	$\overline{G}$	Output Enabel Input (Active LOW)
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS

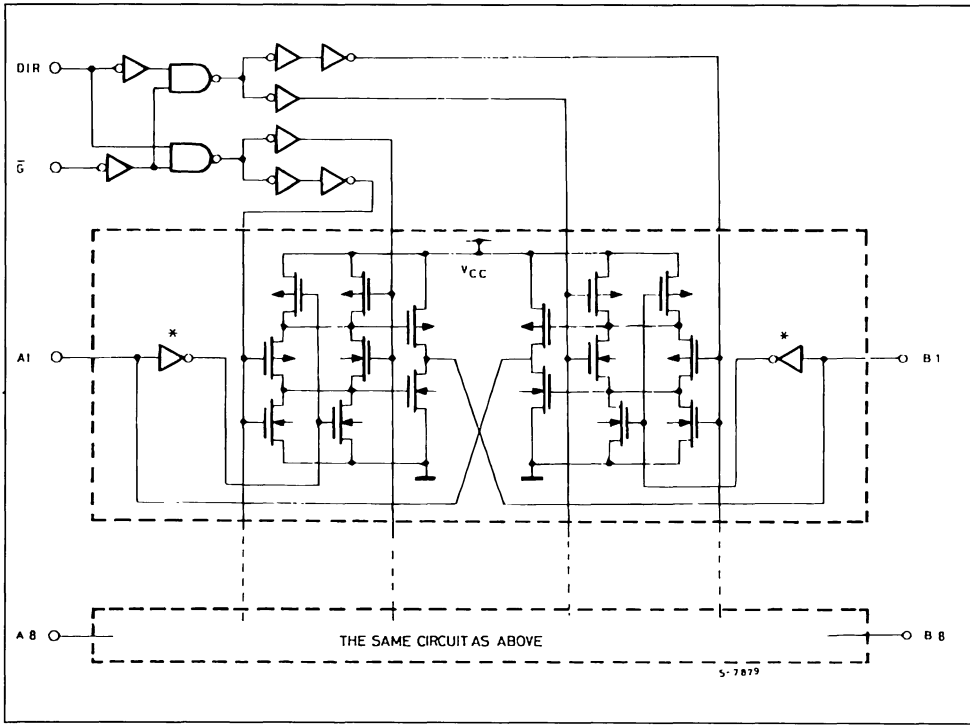


TRUTH TABLE

INPUT		FUNCTION		OUTPUT		
$\overline{G}$	DIR	A BUS	B BUS	HC245	HC640	HC643
L	L	OUTPUT	INPUT	A = B	A = $\overline{B}$	A = B
L	H	INPUT	OUTPUT	B = A	B = $\overline{A}$	B = $\overline{A}$
H	X	Z	Z	Z	Z	Z

X: "H" or "L"
Z: High impedance

LOGIC DIAGRAM (HC640)



NOTE: IN CASE OF HC245 OR HC643, INPUT INVERTERS MARKED* AT A BUS AND B BUS ARE ELIMINATED RESPECTIVELY

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series		-55 to +125	°C
	M74HC Series		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

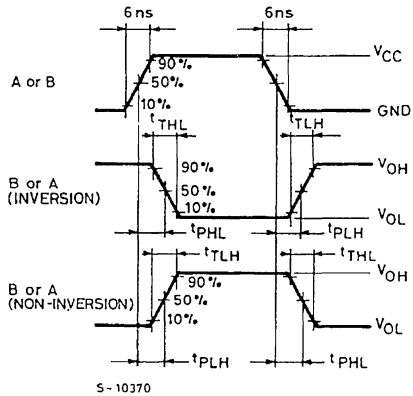
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5.0	µA		
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

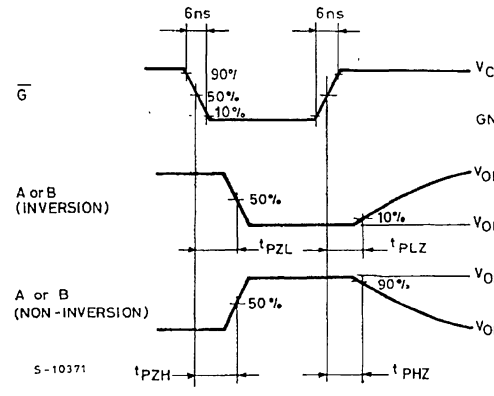
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75		90	ns
		4.5				7	12		19		18	
		6.0				6	10		13		15	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0	50			33	90		115		135	ns
		4.5				12	18		23		27	
		6.0				10	15		20		23	
		2.0	150			48	120		150		180	ns
		4.5				16	24		30		36	
		6.0				14	20		26		31	
t_{PZL} t_{PZH}	Output Enable Time	2.0	50	R_L = 1KΩ		48	150		190		225	ns
		4.5				16	30		38		45	
		6.0				14	26		32		38	
		2.0	150	R_L = 1KΩ		63	180		225		270	ns
		4.5				21	36		45		54	
		6.0				18	31		38		46	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0	50	R_L = 1KΩ		37	150		190		225	ns
		4.5				17	30		38		45	
		6.0				15	26		32		38	
C_{IN}	Input Capacitance		DIR, $\overline{G}$			5	10		10		10	pF
$C_{I/OUT}$	Output Capacitance		An, Bn			13						pF
C_{PD} (*)	Power Dissipation Capacitance		HC245 HC640/643			39 37						pF

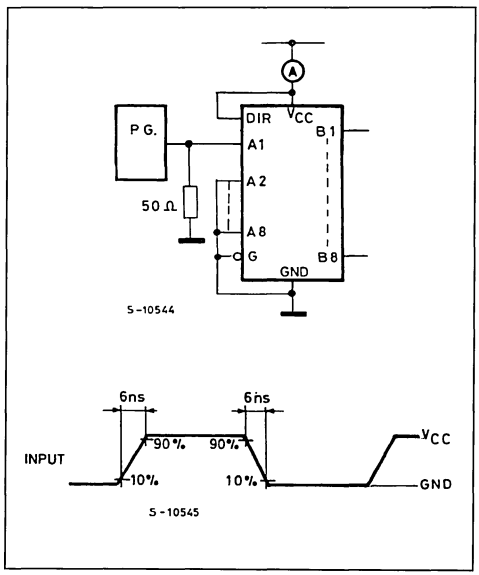
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per circuit)

SWITCHING CHARACTERISTICS TEST WAVEFORM





TEST CIRCUIT I_{CC} (Opr.)



C_{PD} CALCULATION

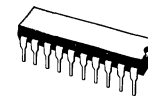
C_{PD} is to be calculated with the following formula by using the measured value of I_{CC} (Opr.) in the test circuit opposite.

$$C_{PD} = \frac{I_{CC}\,(Opr.)}{f_{IN} \times V_{CC}}$$

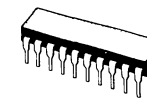
M54/74HCT245/640/643

OCTAL BUS TRANSCEIVER (3-STATE): HCT245 NON INVERTING HCT640 INVERTING, HCT643 INVERTING/NON INVERTING

- HIGH SPEED
  t_{PD} = 10 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) at T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS245/640/643



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

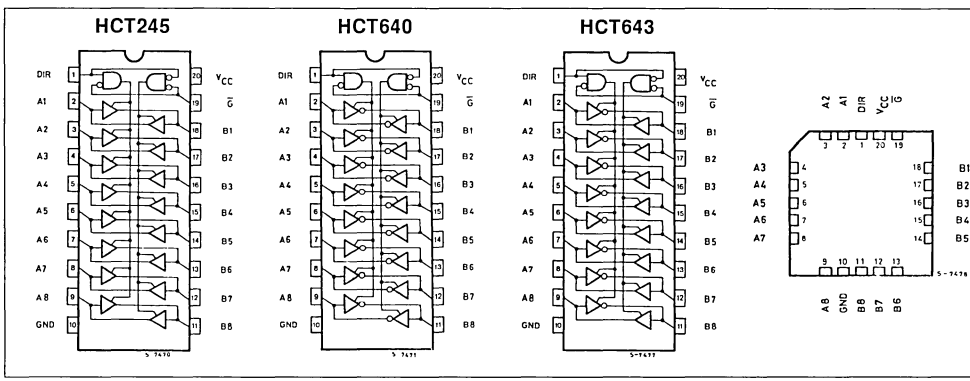
ORDER CODES :

M54HCTXXXF1R M74HCTXXXM1R
M74HCTXXXB1R M74HCTXXXC1R

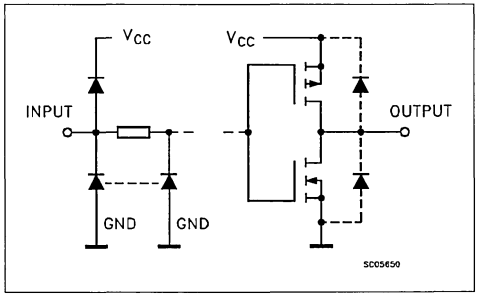
DESCRIPTION

The M54/74HCT245, HCT640 and HCT643 utilise silicon gate C²MOS technology to achive operating speeds eqivalent to LSTTL devices.
Along with the low power dissipation and high noise immunity of standad CMOS integrated circuit, it possesses the capability to drive 15 LSTTL loads. These IC's are intended for two-way asynchronous communication between data buses, and the direction of data trasmission is determined by DIR input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated. All input are equipped with protection circuits against static discharge and transient discharge. These integrated circuits have input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC²MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.
IT IS PROHIBITED TO APPLY A SIGNAL TO A BUS TERMINAL WHEN IT IS IN OUTPUT MODE AND WHEN A BUS THERMINAL IS FLOATING (HIGH IMPEDANCE STATE), IT IS REQUESTED TO FIX THE INPUT LEVEL BY MEANS OF EXTERNAL PULL DOWN OR PULL UP RESISTOR.

PIN CONNECTION (top view)



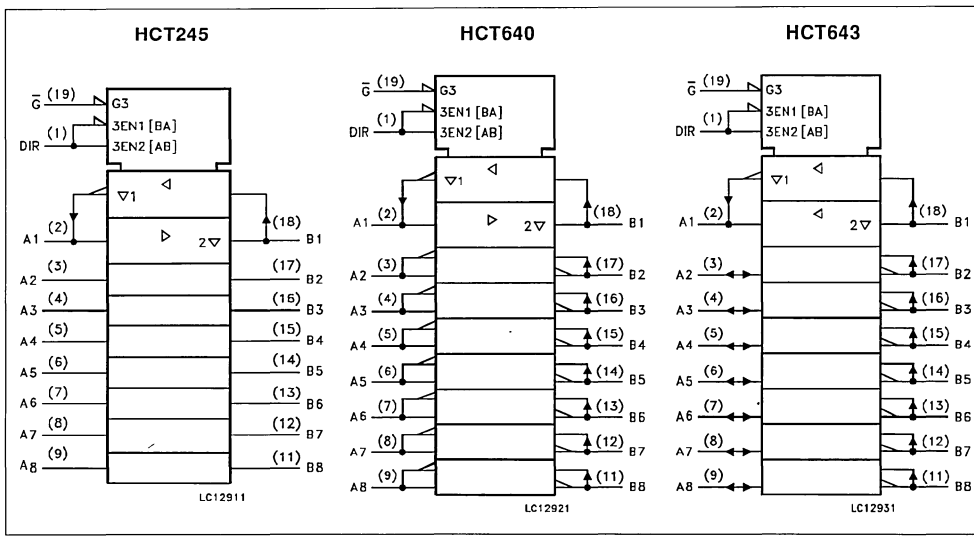
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	DIR	Directional Control
2, 3, 4, 5, 6, 7, 8, 9	A1 to A8	Data Inputs/Outputs
18, 17, 16, 15, 14, 13, 12, 11	B1 to B8	Data Inputs/Outputs
19	$\overline{G}$	Output Enabel Input (Active LOW)
10	GND	Ground (0V)
20	Vcc	Positive Supply Voltage

IEC LOGIC SYMBOLS

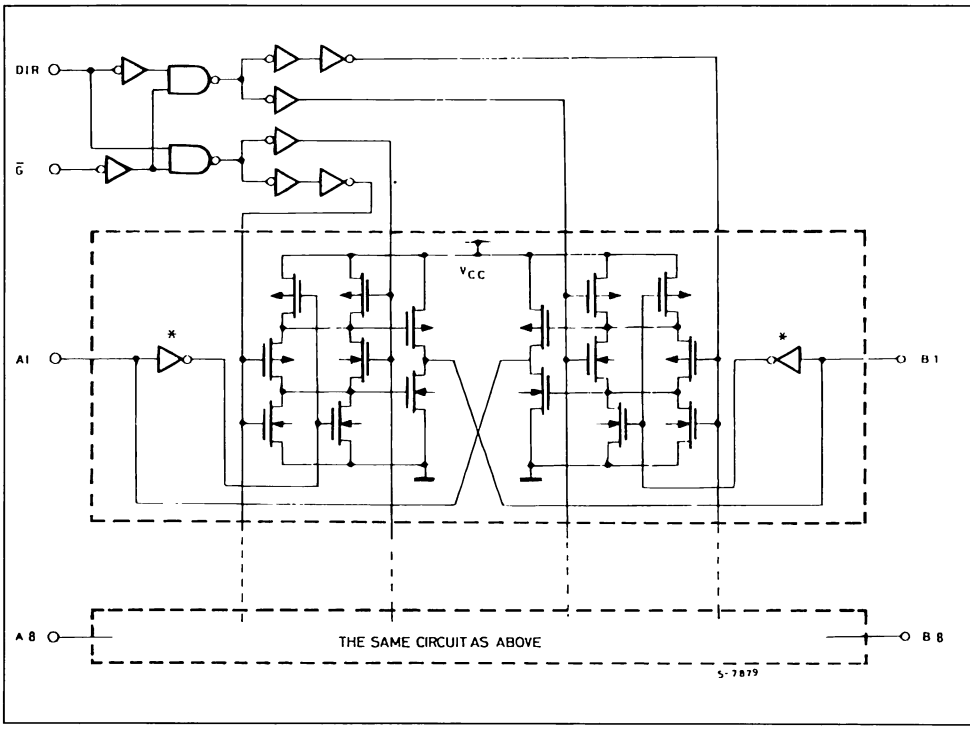


TRUTH TABLE

INPUT		FUNCTION		OUTPUT		
$\overline{G}$	DIR	A BUS	B BUS	HCT245	HCT640	HCT643
L	L	OUTPUT	INPUT	A = B	A = $\overline{B}$	A = B
L	H	INPUT	OUTPUT	B = A	B = $\overline{A}$	B = $\overline{A}$
H	X	Z	Z	Z	Z	Z

X: "H" or "L"
Z: High impedance

LOGIC DIAGRAM (HCT640)



NOTE: IN CASE OF HCT245 OR HCT643, INPUT INVERTERS MARKED* AT A BUS AND B BUS ARE ELIMINATED RESPECTIVELY

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

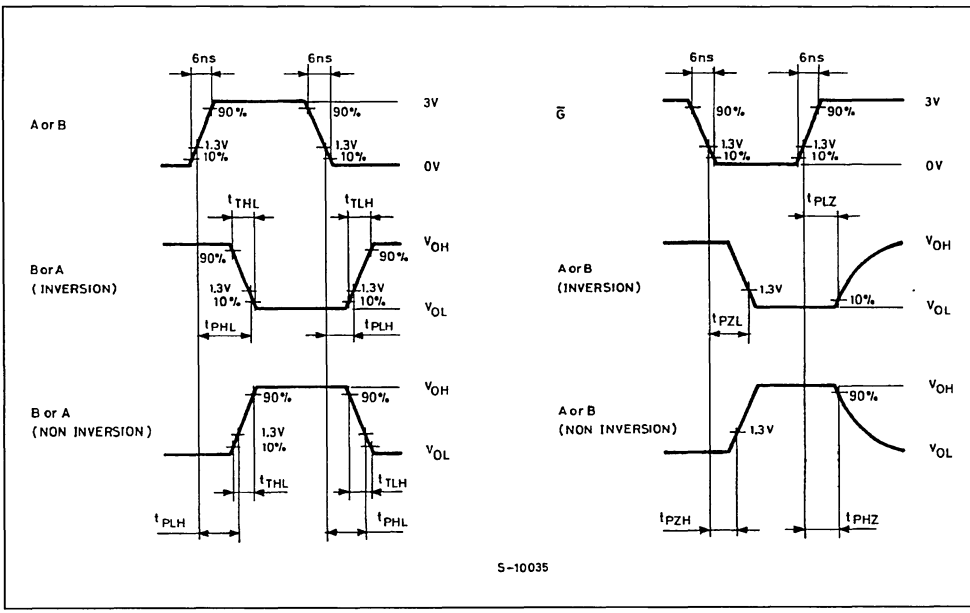
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-6.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 6.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	5.5	V_I = V_{CC} or GND				±0.5		±5.0		±10	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				4		40		80	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9		3.0	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

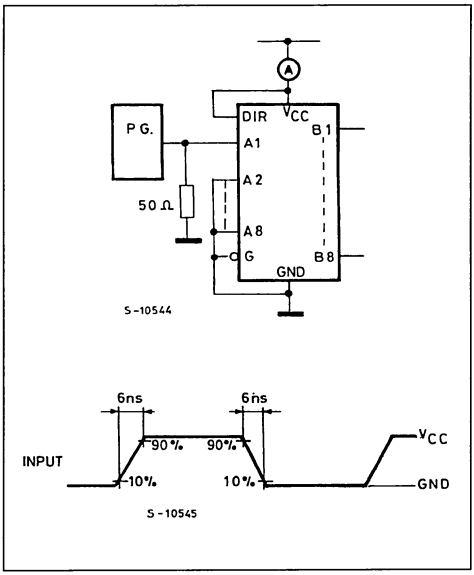
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5	50			7	12		15		18	ns
t_{PLH} t_{PHL}	Propagation Delay Time	4.5	50			13	22		28		33	ns
		4.5	150			18	30		38		45	ns
t_{PZL} t_{PZH}	Output Enable Time	4.5	50	R_L = 1KΩ		19	30		38		45	ns
		4.5	150	R_L = 1KΩ		24	38		48		57	ns
t_{PLZ} t_{PHZ}	Output Disable Time	4.5	50	R_L = 1KΩ		17	30		38		45	ns
C_{IN}	Input Capacitance		DIR, $\overline{G}$			5	10		10		10	pF
$C_{I/OUT}$	Output Capacitance		An, Bn			13						pF
C_{PD} (*)	Power Dissipation Capacitance		HCT245 HCT640/643			41 39						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per circuit)

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



C_{PD} CALCULATION

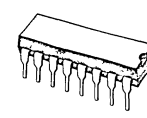
C_{PD} is to be calculated with the following formula by using the measured value of I_{CC} (Opr.) in the test circuit opposite.

$$C_{PD} = \frac{I_{CC}\,(Opr.)}{f_{IN} \times V_{CC}}$$

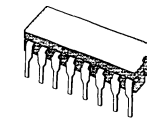
In determining the value of C_{PD}, a relatively high frequency of 1 MHz was applied to f_{IN}, in orther to eliminate any error caused by the quiescent supply current.

8 BIT SIPO SHIFT REGISTER

- HIGH SPEED
  t_{PD} = 14 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C 6 V
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS251



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

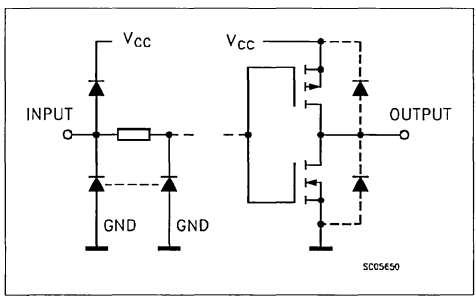
ORDER CODES :

M54HC251F1R M74HC251M1R
M74HC251B1R M74HC251C1R

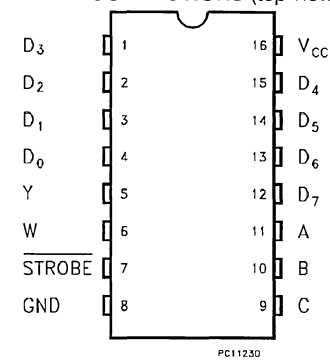
DESCRIPTION

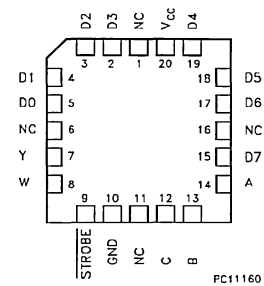
The M54/74HC251 is a high speed CMOS 8-CHANNEL MULTIPLEXER (3-STATE) fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This multiplexer features both true (Y) and complement (W) outputs as well as $\overline{\text{STROBE}}$ input. The $\overline{\text{STROBE}}$ must be a low logic level to enable this device. When the $\overline{\text{STROBE}}$ input is high, both outputs are in the high impedance state. When enabled, address information on the data select inputs determines which data input is routed to Y and W. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)





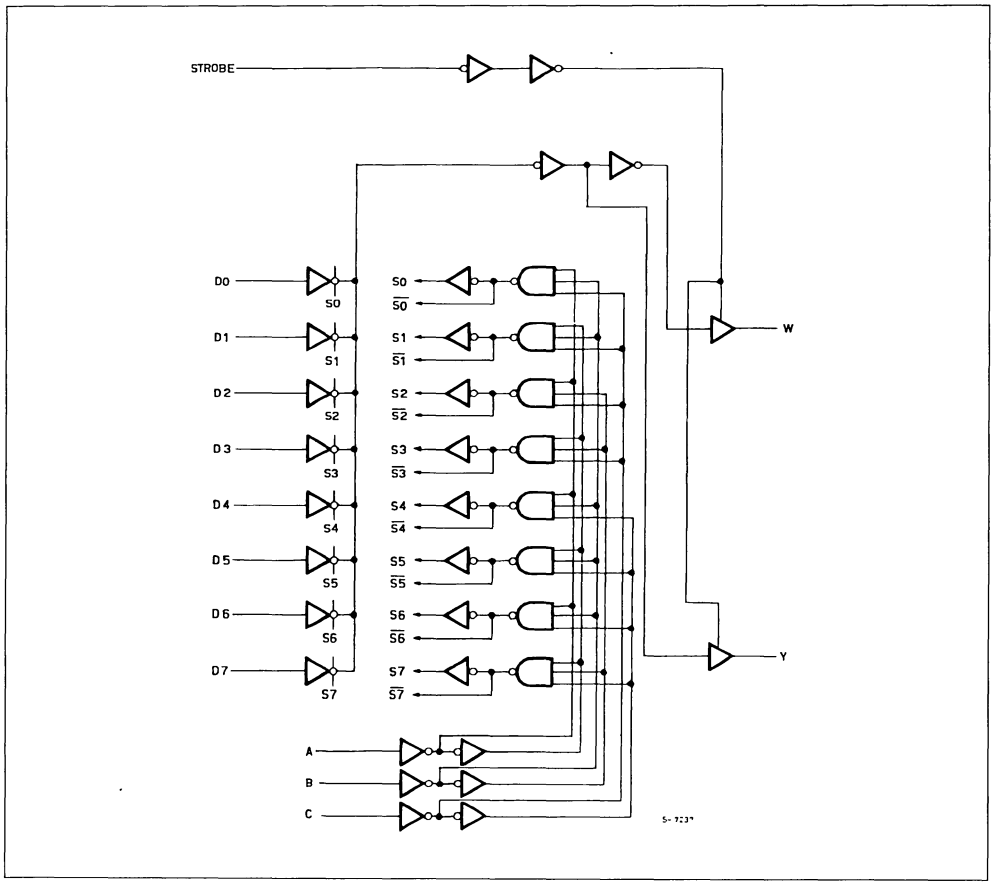
NC =
No Internal
Connection

TRUTH TABLE

INPUTS				OUTPUS	
			$\overline{STROBE}$	Y	W
C	B	A	$\overline{S}$		
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

X: Don't Care Z: HIGH Impedance

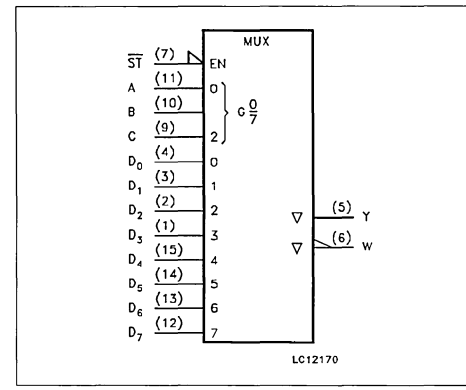
LOGIC DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
4, 3, 2, 1, 15, 14, 13, 12	D0 to D7	Multiplexer Inputs
5	Y	Multiplexer Output
6	W	Complementary Multiplexer Output
7	$\overline{\text{STROBE}}$	3 State Output Enable Input
11, 10, 9	A, B, C	Select Inputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied

(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C. 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

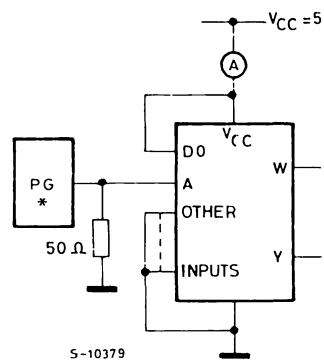
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5.0		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (D - Y, W)	2.0			64	130		165		195	ns
		4.5			16	26		33		39	
		6.0			14	22		28		33	
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C - Y, W)	2.0			80	160		200		240	ns
		4.5			20	32		40		48	
		6.0			17	27		34		41	
t_{PZL} t_{PZH}	Output Enable Time	2.0	R_L = 1 KΩ		36	90		115		135	ns
		4.5			11	18		23		27	
		6.0			9	15		20		23	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0	R_L = 1 KΩ		26	85		105		130	ns
		4.5			13	17		21		26	
		6.0			11	14		18		22	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				62						pF

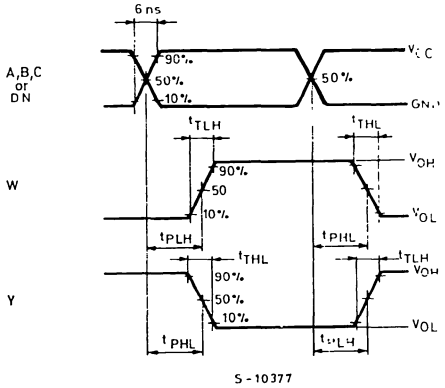
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit) Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

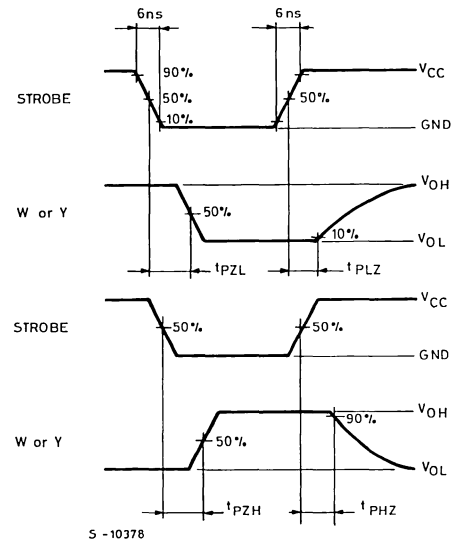
TEST WAVEFORM I_{CC} (Opr.)



* INPUT WAVEFORM TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SWITCHING CHARACTERISTICS TEST WAVEFORM

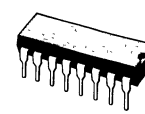




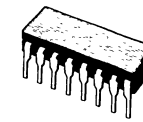
M54/M74HC257
M54/M74HC258

HC257 QUAD 2 CHANNEL MULTIPLEXER (3-STATE)
HC258 QUAD 2 CHANNEL MULTIPLEXER (3-STATE, INVERTING)

- HIGH SPEED
  t_{PD} = 10 ns (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V to 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS257/258



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

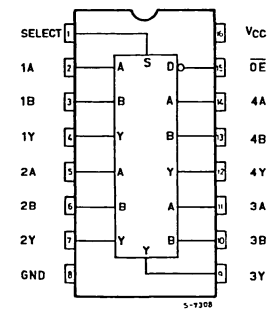
C1R
(Chip Carrier)

ORDER CODES :

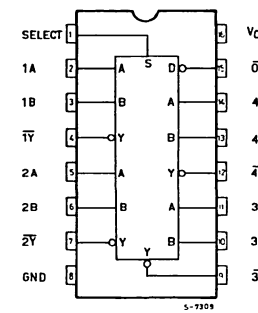
M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

PIN CONNECTIONS (top view)

HC257



HC258



DESCRIPTION

The M54/74HC257 and the M54/74HC258 are high speed CMOS MULTIPLEXERs fabricated with silicon gate C^2MOS technology.

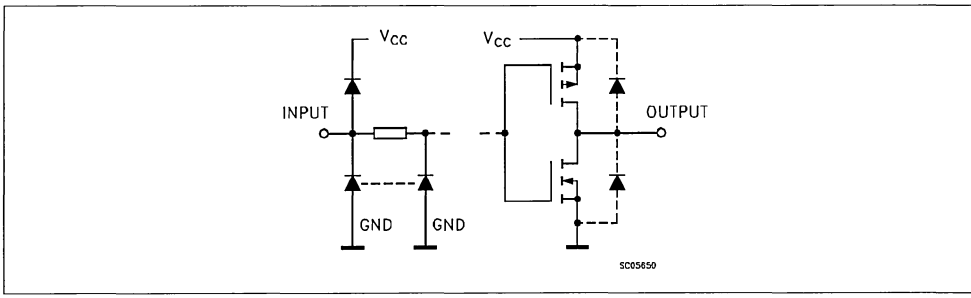
They have the same high speed performance of LSTTL combined with true CMOS low power consumption.

These IC's are composed of an independent 2-channel multiplexer with common SELECT and ENABLE INPUT.

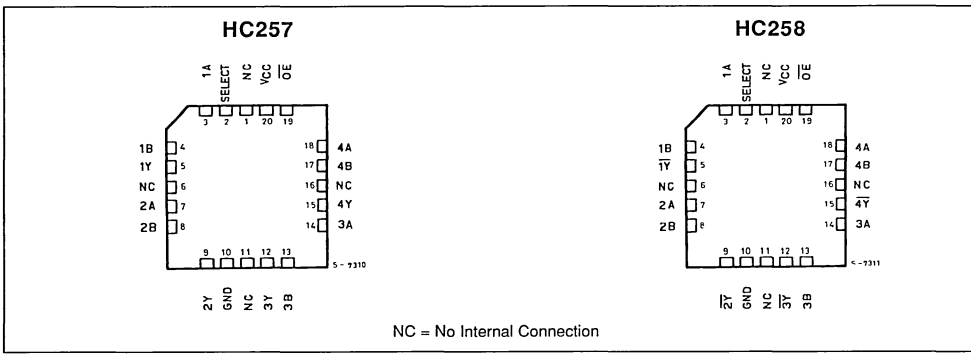
The M54/74HC258 is an inverting multiplexer while the M54/74HC257 is a non-inverting multiplexer. When the ENABLE INPUT is held "High", outputs of both IC's become high-impedance state. If SELECT INPUT is held "Low", "A" data is selected, when SELECT INPUT is high "H", "B" data is chosen.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



CHIP CARRIER



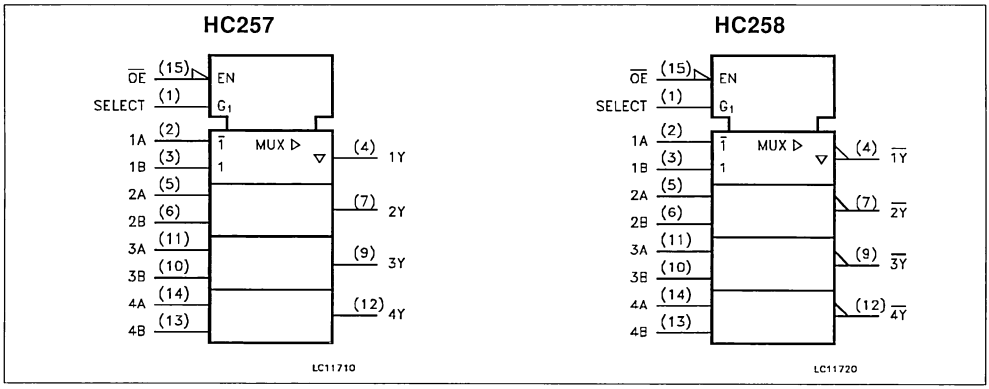
PIN DESCRIPTION (HC257)

PIN No	SYMBOL	NAME AND FUNCTION
1	SELECT	Common Data Select Input
2, 5, 14, 11	1A to 4A	Data Input From Source A
3, 6, 13, 10	1B to 4B	Data Inputs from Source B
4, 7, 12, 9	1Y to 4Y	3 State Multiplexer Outputs
15	$\overline{OE}$	3 State Output Enable Inputs (Active LOW)
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

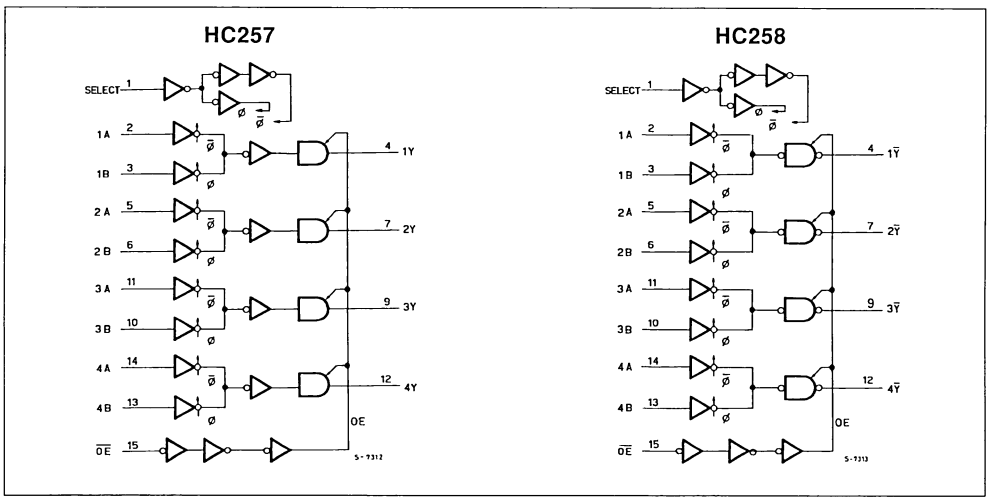
PIN DESCRIPTION (HC258)

PIN No	SYMBOL	NAME AND FUNCTION
1	SELECT	Common Data Select Input
2, 5, 14, 11	1A to 4A	Data Input From Source A
3, 6, 13, 10	1B to 4B	Data Inputs from Source B
4, 7, 12, 9	$1\overline{Y}$ to $4\overline{Y}$	3 State Multiplexer Outputs
15	$\overline{OE}$	3 State Output Enable Inputs (Active LOW)
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



LOGIC DIAGRAM



TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{OE}$	SELECT	A	B	Y (257)	$\overline{Y}$ (258)
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

X = DON'T CARE Z = HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series		-55 to +125	°C
	M74HC Series		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

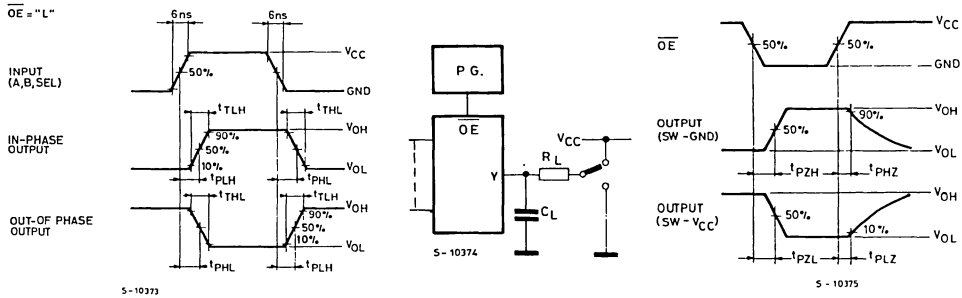
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	Output Leakage Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

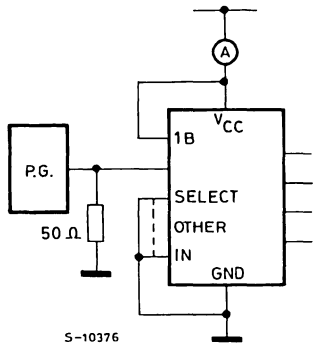
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75		90	ns
		4.5				7	12		15		19	
		6.0				6	10		13		15	
t_{PLH} t_{PHL}	Propagation Delay Time (A, B - Y)	2.0	50			45	100		125		150	ns
		4.5				13	20		25		30	
		6.0				11	17		21		26	
		2.0	150			62	140		175		210	ns
		4.5				18	28		35		42	
		6.0				15	24		30		36	
t_{PLH} t_{PHL}	Propagation Delay Time (SELECT - Y)	2.0	50			45	100		125		150	ns
		4.5				13	20		25		30	
		6.0				11	17		21		26	
		2.0	150			62	140		175		210	ns
		4.5				18	28		35		42	
		6.0				15	24		30		36	
t_{PZL} t_{PZH}	Output Enable Time	2.0	50	R_L = 1 KΩ		40	110		140		165	ns
		4.5				12	22		28		33	
		6.0				10	19		24		28	
		2.0	150	R_L = 1 KΩ		57	150		190		225	ns
		4.5				17	30		38		45	
		6.0				14	26		32		38	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0	50	R_L = 1 KΩ		28	140		175		210	ns
		4.5				14	28		35		42	
		6.0				13	24		30		36	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{OUT}	Output Capacitance					10						pF
C_{PD} (*)	Power Dissipation Capacitance					47						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit) Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Channel)

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERSISTICS TESt.

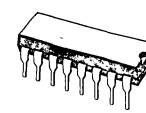
C_{PD} CALCULATION

C_{PD} is to be calculated with the following formula by using the measured value of ICC (opr.) in the test circuit opposite.

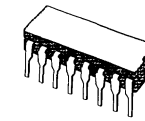
$$C_{PD} = \frac{I_{CC}\,(opr)}{f_{IN} \times V_{CC}}$$

HCT257 QUAD 2 CHANNEL MULTIPLEXER (3-STATE)
HCT258 QUAD 2 CHANNEL MULTIPLEXER (3-STATE, INVERTING)

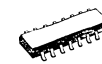
- HIGH SPEED
  t_{PD} = 16 ns (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) at T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS257/258



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HCTXXXF1R M74HCTXXXM1R
M74HCTXXXB1R M74HCTXXXC1R

DESCRIPTION

The M54/74HCT257 and the M54/74HCT258 are high speed CMOS MULTIPLEXERs fabricated with silicon gate C^2MOS technology.

They have the same high speed performance of LSTTL combined with true CMOS low power consumption.

These IC's are composed of an independent 2-channel multiplexer with common SELECT and ENABLE INPUT.

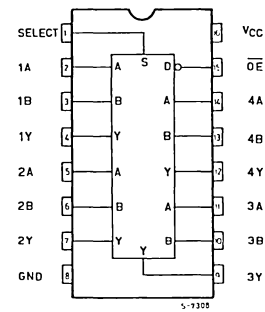
The M54/74HCT258 is an inverting multiplexer while the M54/74HCT257 is a non-inverting multiplexer. When the ENABLE INPUT is held "High", outputs of both IC's become high-impedance state. If SELECT INPUT is held "Low", "A" data is selected, when SELECT INPUT is high "H", "B" data is chosen.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

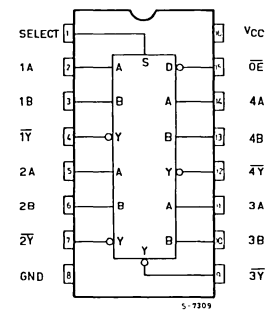
This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

PIN CONNECTIONS (top view)

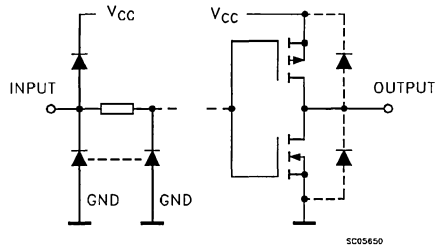
HCT257



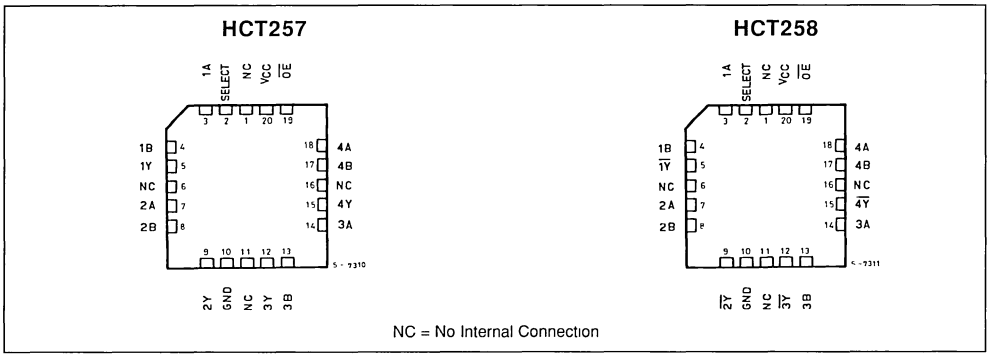
HCT258



INPUT AND OUTPUT EQUIVALENT CIRCUIT



CHIP CARRIER



NC = No Internal Connection

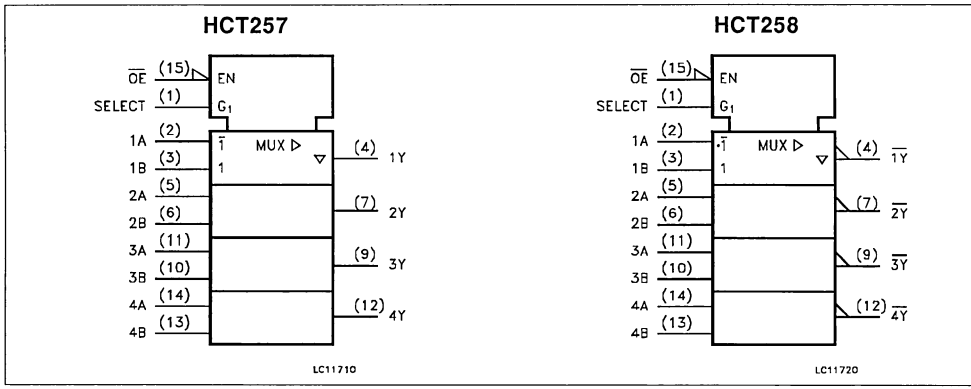
PIN DESCRIPTION (HCT257)

PIN No	SYMBOL	NAME AND FUNCTION
1	SELECT	Common Data Select Input
2, 5, 14, 11	1A to 4A	Data Input From Source A
3, 6, 13, 10	1B to 4B	Data Inputs from Source B
4, 7, 12, 9	1Y to 4Y	3 State Multiplexer Outputs
15	$\overline{OE}$	3 State Output Enable Inputs (Active LOW)
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

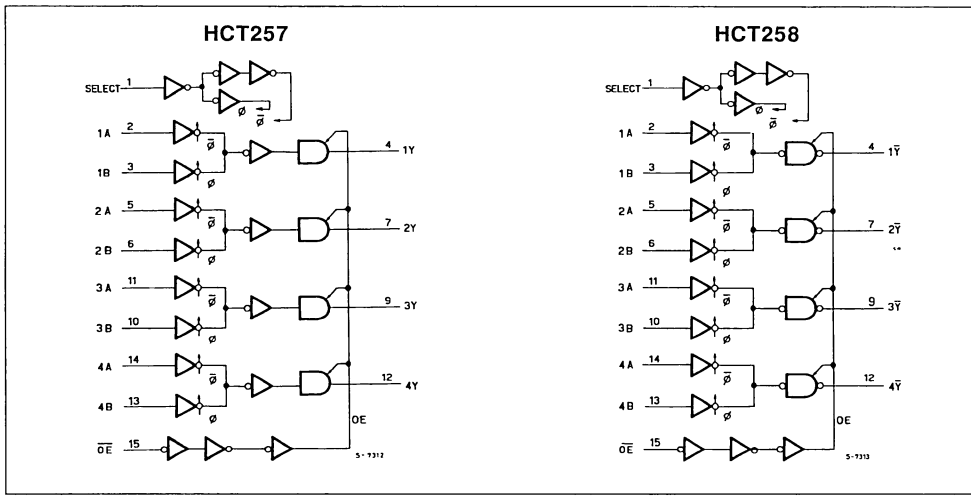
PIN DESCRIPTION (HCT258)

PIN No	SYMBOL	NAME AND FUNCTION
1	SELECT	Common Data Select Input
2, 5, 14, 11	1A to 4A	Data Input From Source A
3, 6, 13, 10	1B to 4B	Data Inputs from Source B
4, 7, 12, 9	$1\overline{Y}$ to $4\overline{Y}$	3 State Multiplexer Outputs
15	$\overline{OE}$	3 State Output Enable Inputs (Active LOW)
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



LOGIC DIAGRAM



TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{OE}$	SELECT	A	B	Y (257)	$\overline{Y}$ (258)
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

X = DON'T CARE Z = HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

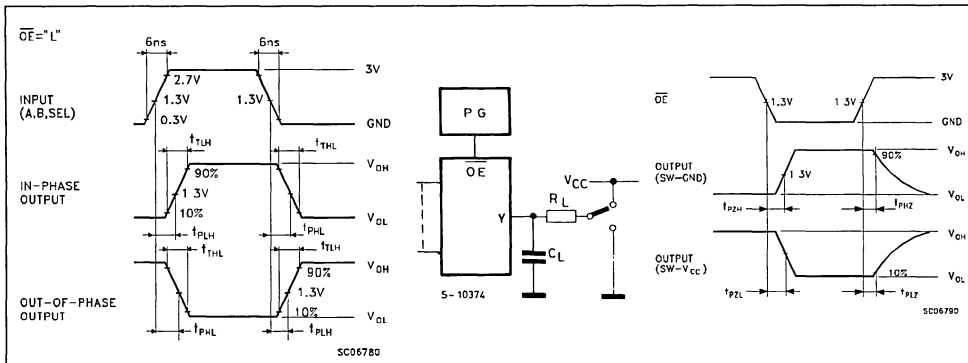
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.4	
I_{OZ}	3-State Output Off State Current	5.5	V_I = V_{CC} or GND				±0.5		±5		±10	µA
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				1		10		20	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND				2.0		2.9		3.0	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

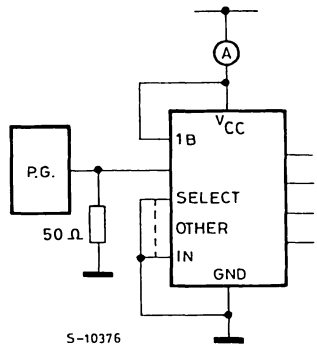
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			7	12		15		18	ns
t_{PLH} t_{PHL}	Propagation Delay Time (A, B - Y)	4.5	HCT257		19	30		38		45	ns
			HCT258		17	27		34		41	
t_{PLH} t_{PHL}	Propagation Delay Time (SELECT - Y)	4.5			20	30		38		45	ns
t_{PZL} t_{PZH}	Output Enable Time	4.5	R_L = 1 KΩ		18	30		38		45	ns
t_{PLZ} t_{PHZ}	Output Disable Time	4.5	R_L = 1 KΩ		16	30		38		45	ns
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{OUT}	Output Capacitance				10						pF
C_{PD} (*)	Power Dissipation Capacitance		HCT257 HCT258		34 33						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit) Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Channel)

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERSISTICS TESt

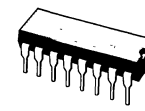
C_{PD} CALCULATION

C_{PD} is to be calculated with the following formula by using the measured value of ICC (opr.) in the test circuit opposite.

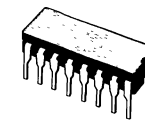
$$C_{PD} = \frac{I_{CC}\,(opr)}{f_{IN} \times V_{CC}}$$

8 BIT ADDRESSABLE LATCH

- HIGH SPEED
  t_{PD} = 15 ns (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL PROPAGATION DELAYS
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PRORAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V to 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS259



B1R
(Plastic Package)



F1R
(Ceramic Package)

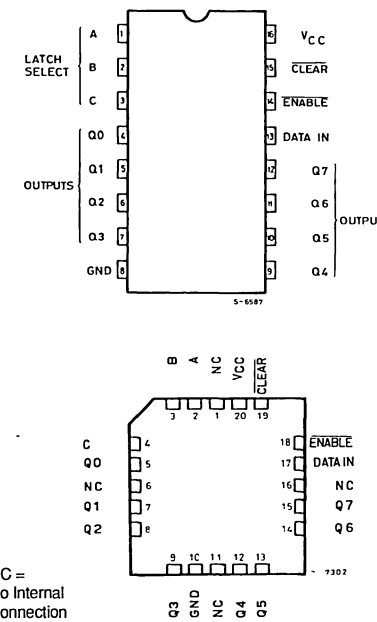
M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HC259F1R M74HC259M1R
M74HC259B1R M74HC259C1R

PIN CONNECTIONS (top view)



NC =
No Internal
Connection

DESCRIPTION

The M54/74HC259 is a high speed CMOS 8 BIT ADDRESSABLE LATCH fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

The M54HC259/M74HC259 has single data input (D) 8 latch outputs (Q0-Q7), 3 address inputs (A, B, and C), common enable input (E), and a common $\overline{CLEAR}$ input. To operate this device as an addressable latch, data is held on the D input, and the address of the latch into which the data is to be entered is held on the A, B, and C inputs. When $\overline{ENABLE}$ is taken low the data flows through to the addresses output. The data is stored on the positive-going edge of the $\overline{ENABLE}$ pulse. All unaddressed latches will remain unaffected. With $\overline{ENABLE}$ in the high state the device is deselected and all latches remain in their previous state, unaffected by changes on the data or address inputs. To eliminate the possibility of entering erroneous data into the latches, the $\overline{ENABLE}$ should be held high (inactive) while the address lines are changing. If $\overline{ENABLE}$ is held high and $\overline{CLEAR}$ is taken low all eight latches are cleared to the low state. If $\overline{ENABLE}$ is low all latches except the addressed latch will be cleared. The addressed latch will instead follow the D input, effectively implementing a 3-to 8 line decoder.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

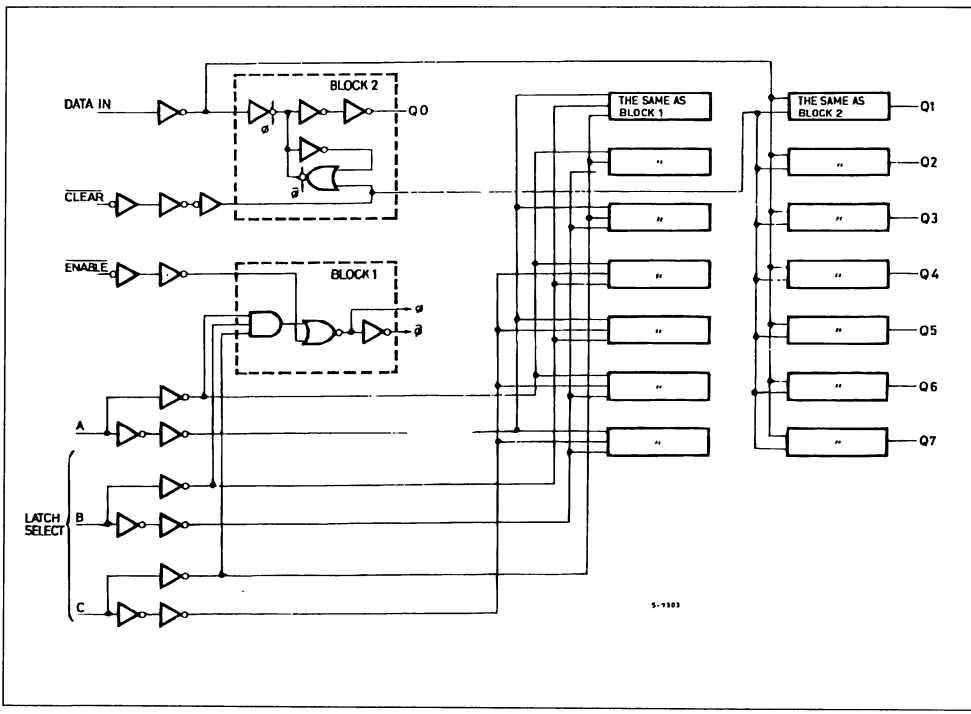
TRUTH TABLE

INPUTS		OUTPUTS OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
$\overline{\text{CLEAR}}$	$\overline{\text{ENABLE}}$			
H	L	D	Qi0	ADDRESSABLE LATCH
H	H	Qi0	Qi0	MEMORY
L	L	D	L	8 LINE DEMULTIPLEXER
L	H	L	L	CLEAR ALL BITS TO 'L'

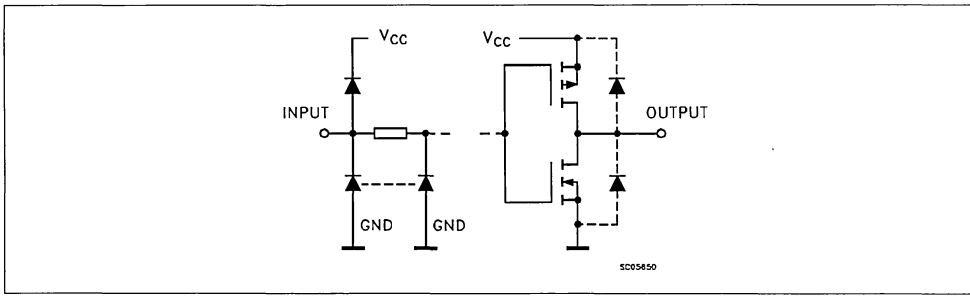
D: The level at the data input
Qi0: The level before the indicated steady state input conditions were established, (i = 0, 1, ...,7).

SELECT INPUTS			LATCH ADDRESSED
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

LOGIC DIAGRAM



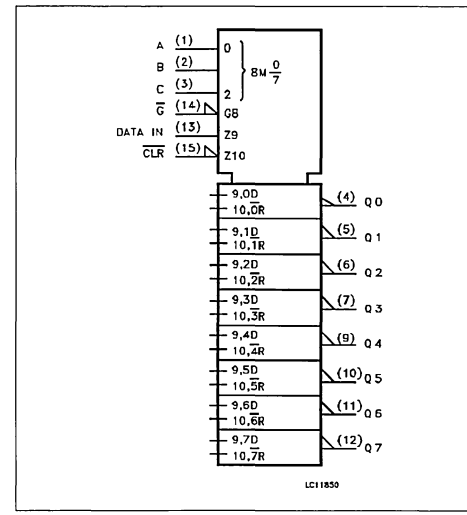
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3	A, B, C	Address Inputs
4, 5, 6, 7, 9, 10, 11, 12	Q0 to Q7	Latch Outputs
13	D	Data Input
14	$\overline{ENABLE}$	Latch Enable Input (Active LOW)
15	$\overline{CLEAR}$	Conditional Reset Input (Active LOW)
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied

(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

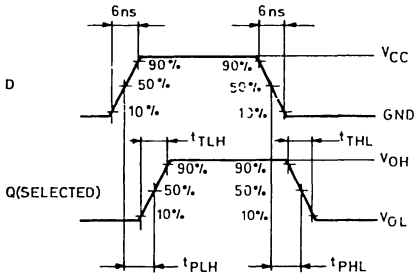
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (DATA - Q)	2.0			56	140		175		210	ns
		4.5			18	28		35		42	
		6.0			15	24		30		36	
t_{PLH} t_{PHL}	Propagation Delay Time (A, B, C - Q)	2.0			76	190		240		285	ns
		4.5			24	38		48		57	
		6.0			20	32		41		48	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{G}$ - Q)	2.0			57	150		190		225	ns
		4.5			19	30		38		45	
		6.0			16	26		32		38	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$ - Q)	2.0			45	115		145		175	ns
		4.5			15	23		29		35	
		6.0			13	20		25		30	
$t_{W(L)}$	Minimum Pulse Width ($\overline{ENABLE}$)	2.0			28	75		90		115	ns
		4.5			7	15		19		23	
		6.0			6	13		16		20	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLEAR}$)	2.0			24	75		90		115	ns
		4.5			6	15		19		23	
		6.0			5	13		16		20	
t_s	Minimum Set-up Time (DATA)	2.0			12	50		60		75	ns
		4.5			3	10		12		15	
		6.0			3	9		11		13	
t_s	Minimum Set-up Time (A, B, C)	2.0				25		30		40	ns
		4.5				5		6		8	
		6.0				5		5		7	
t_h	Minimum Hold Time (DATA)	2.0				5		5		5	ns
		4.5				5		5		5	
		6.0				5		5		5	
t_h	Minimum Hold Time (A, B, C)	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				66						pF

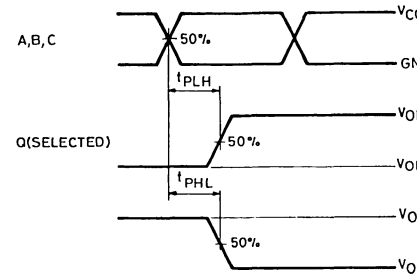
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

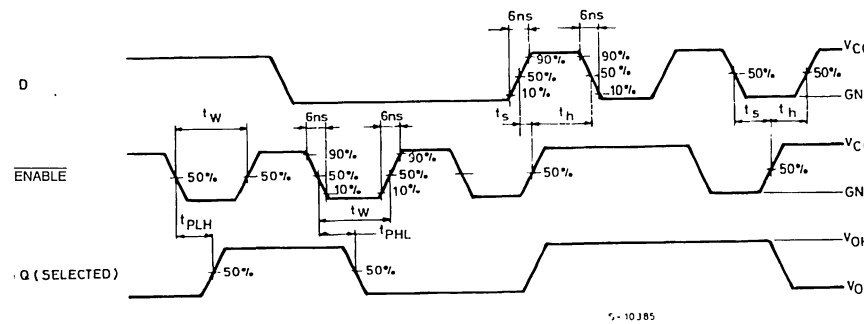
WAVEFORM 1. ($\overline{ENABLE}$ = L, $\overline{CLR}$ = H, A ~ C =



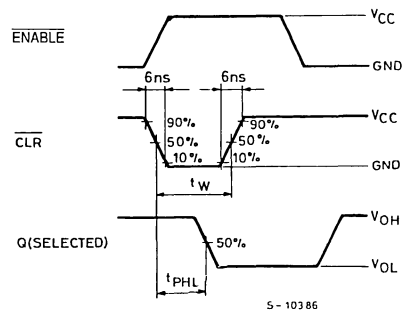
WAVEFORM 2. ($\overline{G}$ = L)



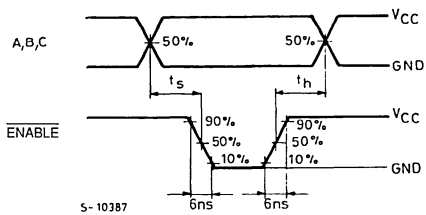
WAVEFORM 3. ($\overline{CLR}$ = H, A ~ C = Stable)



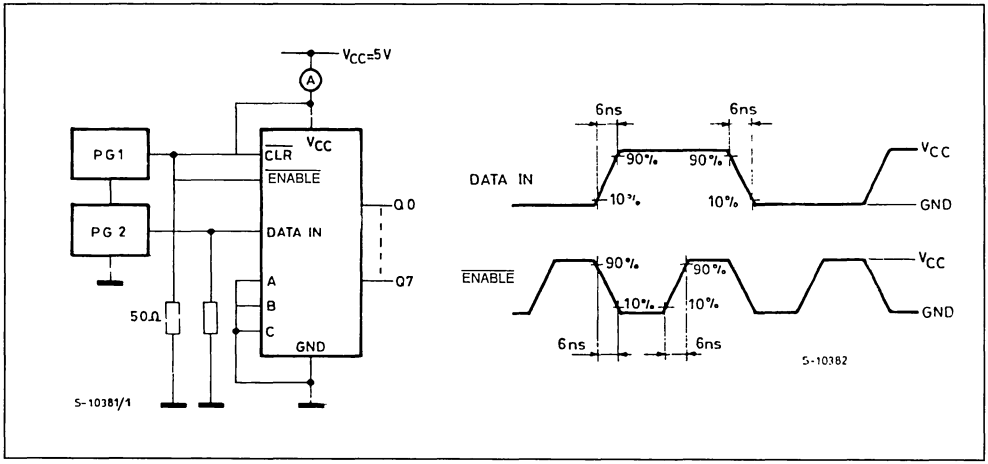
WAVEFORM 4. (D = H, A ~ C - Stable)



WAVEFORM 5. ($\overline{CLR}$ = H)

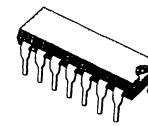


TEST CIRCUIT I_{CC} (Opr.)

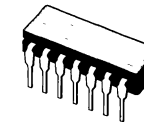


HC266 QUAD EXCLUSIVE NOR GATE WITH OPEN DRAIN
HC7266 QUAD EXCLUSIVE NOR GATE

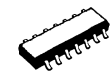
- HIGH SPEED
  t_{PD} = 10 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE (7266)
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS (7266)
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS7266



B1R
(Plastic Package)



F1R
(Ceramic Package)



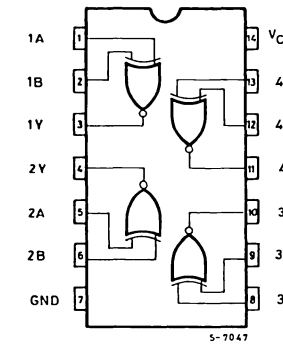
M1R
(Micro Package)

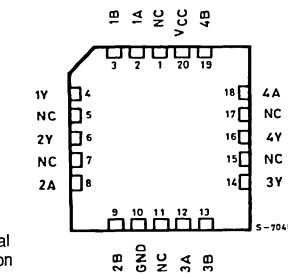
C1R
(Chip Carrier)

ORDER CODES :

M54HCXXXF1R M74HCXXX1R
M74HCXXXB1R M74HCXXXC1R

PIN CONNECTIONS (top view)





NC =
No Internal
Connection

DESCRIPTION

The M54/74HC266/7266 are high speed CMOS QUAD EXCLUSIVE NOR GATES, fabricated in silicon gate C^2MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption.

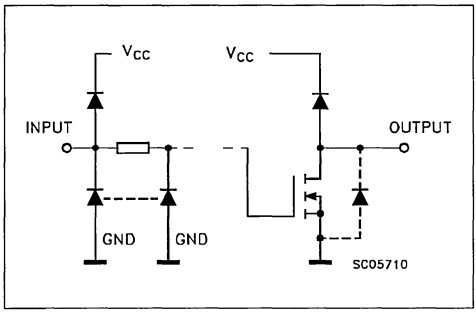
The HC266 has a high performance N-channel MOS transistor (OPEN DRAIN output).

The HC7266 has an output buffer which is CMOS structure.

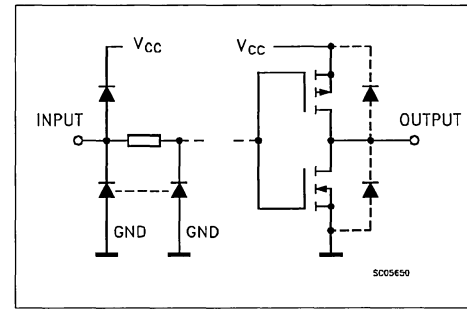
Input and output buffers ensure high noise immunity and stable outputs.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT (HC266)



INPUT AND OUTPUT EQUIVALENT CIRCUIT (HC7266)



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 5, 8, 12	1A to 4A	Data Inputs
2, 6, 9, 13	1B to 4B	Data Inputs
3, 4, 10, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	Vcc	Positive Supply Voltage

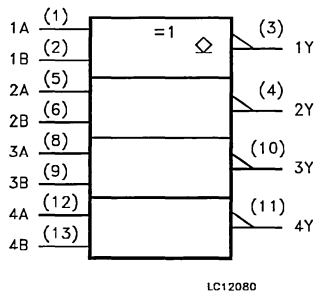
TRUTH TABLE

A	B	Y	
		7266	266
L	L	H	Z
L	H	L	L
H	L	L	L
H	H	H	Z

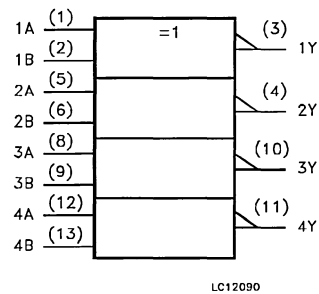
Z: High Impedance

IEC LOGIC SYMBOLS

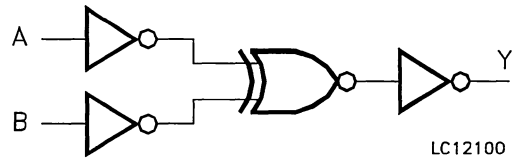
HC266



HC7266



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{DD} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

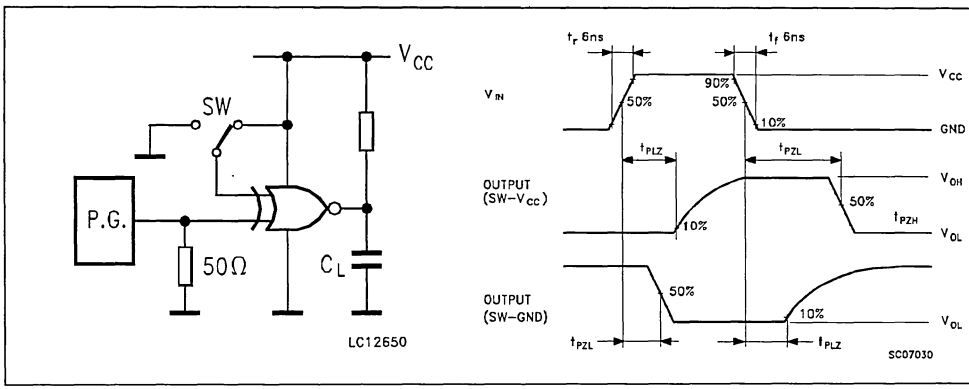
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage (HC7266)	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	Output Leakage Current (HC266)	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

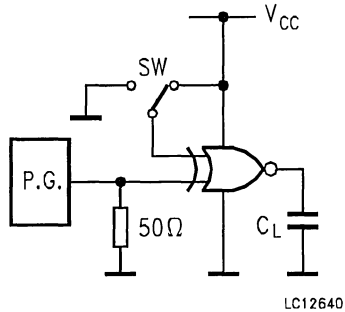
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{THL}	Output Transition Time (HC266)	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{TLH} t_{THL}	Output Transition Time (HC7266)	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLZ} t_{PZL}	Propagation Delay Time (HC266)	2.0	R_L = 1KΩ		48	90		115		135	ns
		4.5			12	18		23		27	
		6.0			10	15		20		23	
t_{PLH} t_{PHL}	Propagation Delay Time (HC7266)	2.0			36	90		115		135	ns
		4.5			11	18		23		27	
		6.0			9	15		20		23	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				20						pF

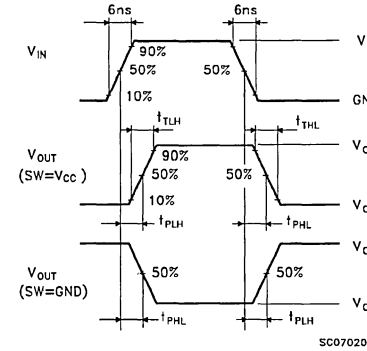
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT (HC266)

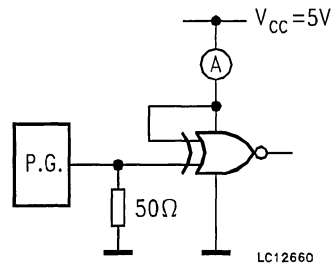


SWITCHING CHARACTERISTICS TEST CIRCUIT (HC7266)





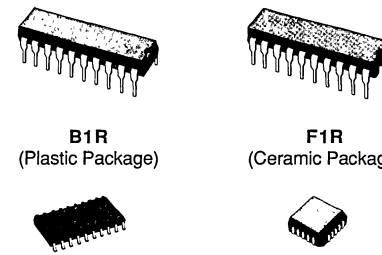
TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

OCTAL D TYPE FLIP FLOP WITH CLEAR

- HIGH SPEED
  f_{MAX} = 67 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS273



B1R (Plastic Package)

F1R (Ceramic Package)

M1R (Micro Package)

C1R (Chip Carrier)

ORDER CODES :

M54HC273F1R M74HC273M1R
M74HC273B1R M74HC273C1R

DESCRIPTION

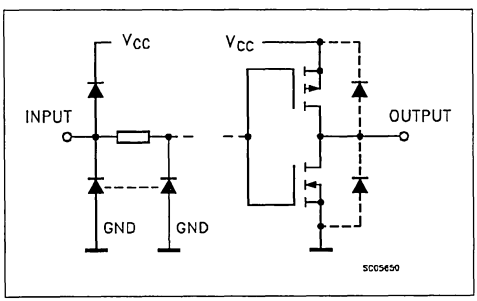
The M54/74HC273 is a high speed CMOS OCTAL D-TYPE FLIP FLOP WITH CLEAR fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

Information signals applied to D inputs are transferred to the Q outputs on the positive-going edge of the clock pulse.

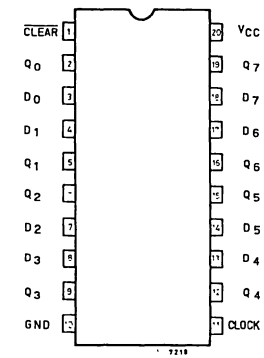
When the $\overline{CLEAR}$ input is held low, the Q output are in the low logic level independent of the other inputs.

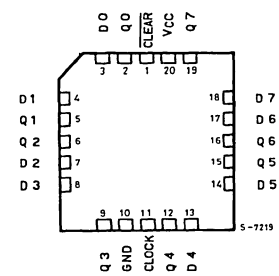
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



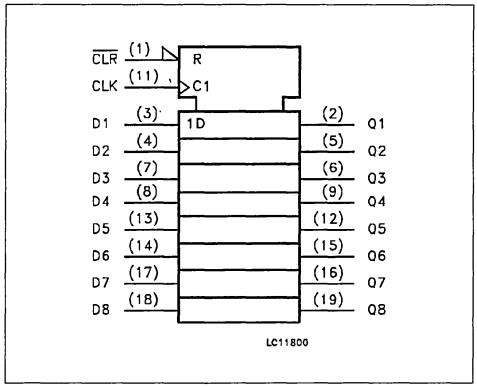


NC = No Internal Connection

PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{CLEAR}$	Master Reset Input (Active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0 to Q7	Flip Flop Outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data Inputs
11	CLOCK	Clock Input (LOW to HIGH, Edge Triggered)
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL

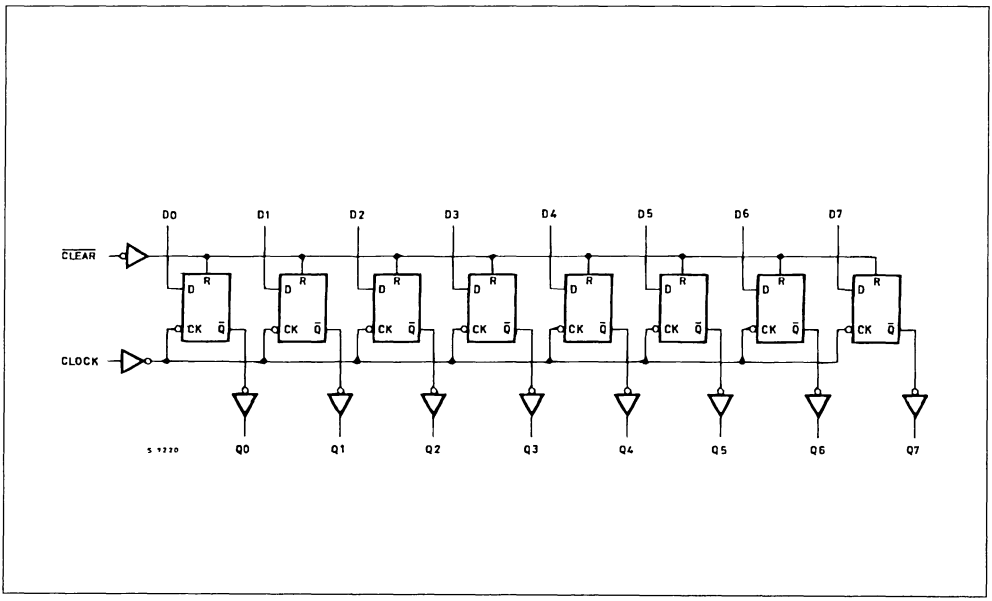


TRUTH TABLE

INPUTS			OUTPUS	FUNCTION
$\overline{CLEAR}$	CLOCK	D	Q	
L	X	X	L	CLEAR
H	⎍	L	L	
H	⎍	H	H	
H	⎎	X	Qn	NO CHANGE

X: Don't Care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied

(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

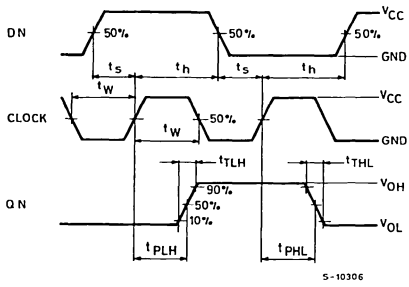
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

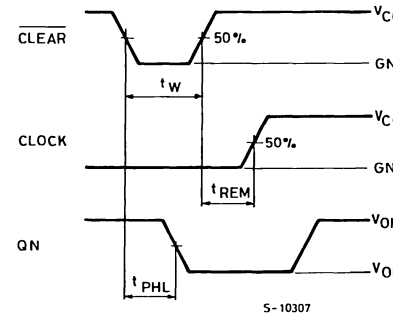
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			25	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q)	2.0			54	145		180		220	ns
		4.5			18	29		36		44	
		6.0			15	25		31		37	
t_{PLH} t_{PHL}	Propagation Delay Time (CLEAR - Q)	2.0			60	160		200		240	ns
		4.5			20	32		40		48	
		6.0			17	27		34		41	
f_{MAX}	Maximum Clock Frequency	2.0		6	18		4.8		4		MHz
		4.5		30	56		24		20		
		6.0		35	66		28		24		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0			28	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
$t_{W(L)}$	Minimum Pulse Width (CLEAR)	2.0			28	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
t_s	Minimum Set-up Time	2.0			20	75		95		110	ns
		4.5			4	15		19		22	
		6.0			3	13		16		19	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Minimum Removal Time (CLEAR)	2.0			16	50		65		75	ns
		4.5			4	10		13		15	
		6.0			3	9		11		13	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				43						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Flip FLop), and the total CPD when n pcs of Flip Flop operate can be gained by the following equations: CPD (total) = 32 + 11 x n

SWITCHING CHARACTERISTICS TEST WAVEFORM

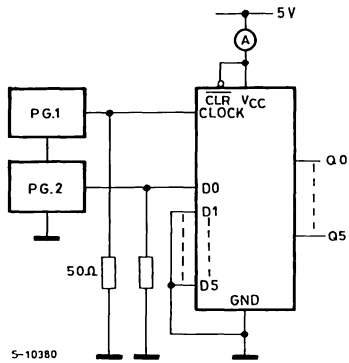


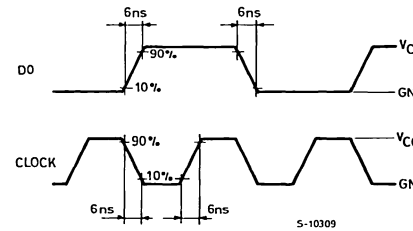
$\overline{CLEAR}$ = "H"



DN = "H"

TEST CIRCUIT I_{CC} (Opr.)



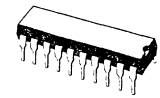


SGS-THOMSON MICROELECTRONICS

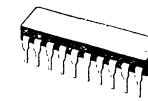
M54HCT273
M74HCT273

OCTAL D TYPE FLIP FLOP WITH CLEAR

- HIGH SPEED
  f_{MAX} = 80 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS273



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

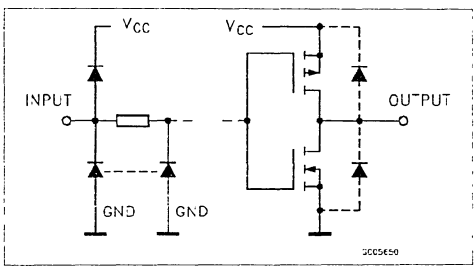
ORDER CODES :

M54HCT273F1R M74HCT273M1R
M74HCT273B1R M74HCT273C1R

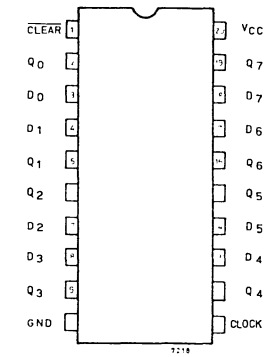
DESCRIPTION

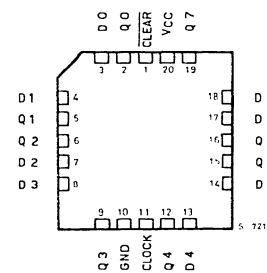
The M54/74HCT273 is a high speed CMOS OCTAL D-TYPE FLIP FLOP WITH CLEAR fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. Information signals applied to D inputs are transferred to the Q outputs on the positive-going edge of the clock pulse.
When the CLEAR input is held low, the Q output are in the low logic level independent of the other inputs. All inputs are equipped with protection circuits against static discharge and transient excess voltage. This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



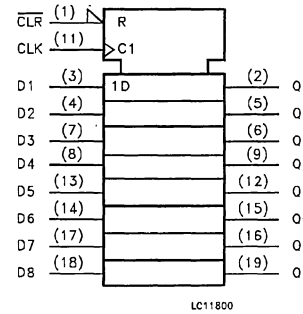


NC =
No Internal
Connection

PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{CLEAR}$	Master Reset Input (Active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0 to Q7	Flip Flop Outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data Inputs
11	CLOCK	Clock Input (LOW to HIGH, Edge Triggered)
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL

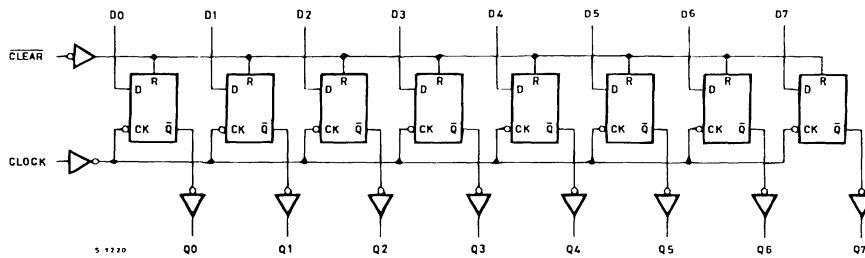


TRUTH TABLE

INPUTS			OUTPUS	FUNCTION
$\overline{CLEAR}$	CLOCK	D	QA	
L	X	X	L	CLEAR
H	⎍	L	L	
H	⎍	H	H	
H	⎎	X	Qn	NO CHANGE

X. Don't Care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C· 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

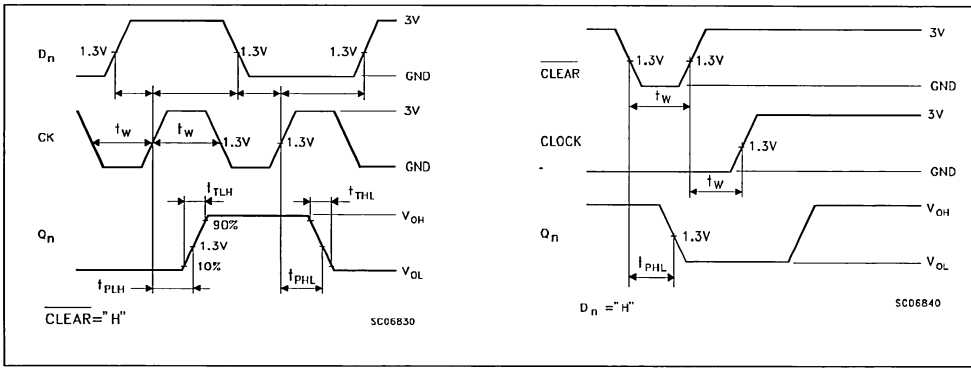
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0 1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				4		40		80	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9		3.0	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

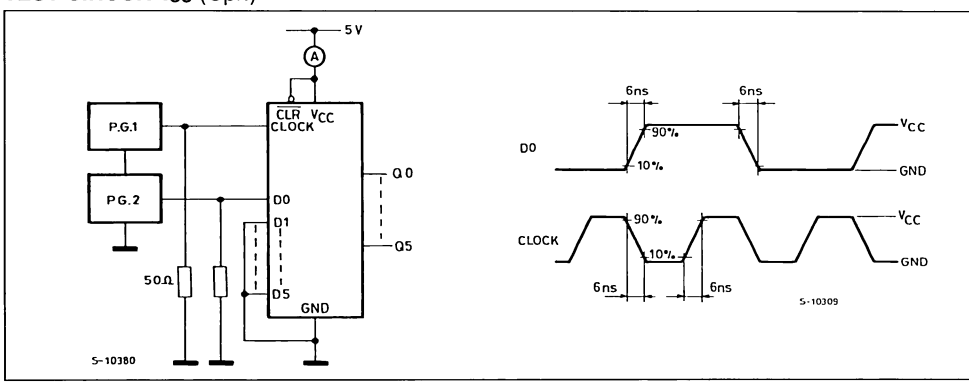
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			9	15		19		22	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q)	4.5			19	30		38		45	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$ - Q)	4.5			22	32		40		48	ns
f_{MAX}	Maximum Clock Frequency	4.5		30	71		24				MHz
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				29						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Flip FLop), and the total CPD when n pcs of Flip Flop operate can be gained by the following equations: CPD (total) = 32 + 11 x n

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)

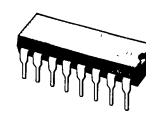


SGS-THOMSON MICROELECTRONICS

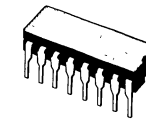
M54HC279
M74HC279

QUAD $\overline{S}$ - $\overline{R}$ LATCH

- HIGH SPEED
  t_{PD} = 12 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 2 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS279



B1R
(Plastic Package)



F1R
(Ceramic Package)

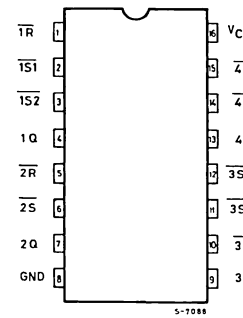
M1R
(Micro Package)

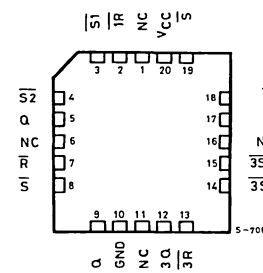
C1R
(Chip Carrier)

ORDER CODES :

M54HC279F1R M74HC279M1R
M74HC279B1R M74HC279C1R

PIN CONNECTIONS (top view)





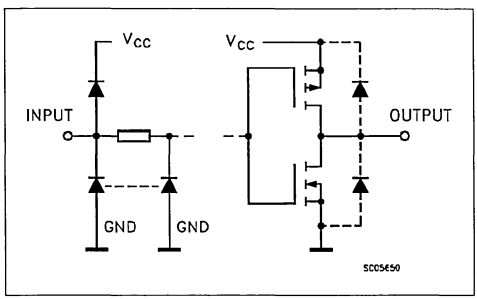
NC =
No Internal
Connection

DESCRIPTION

The M54/74HC279 is a high speed CMOS QUAD $\overline{S}$ - $\overline{R}$ LATCH fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

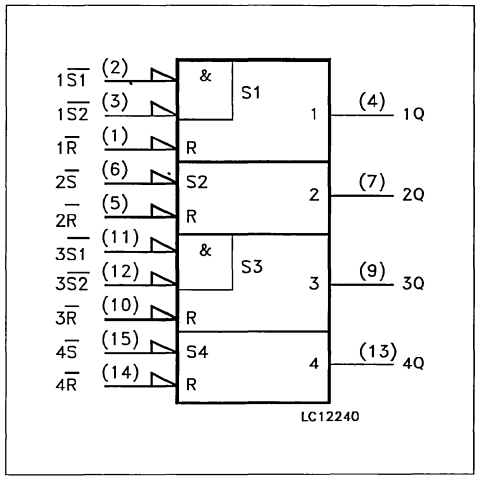
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 5, 10. 14	$1\overline{R}$ to $4\overline{R}$	Reset Inputs (Active LOW)
2, 3, 6, 11, 12, 15	$1\overline{S1}$, $1\overline{S2}$, 2S, $3\overline{S1}$, $3\overline{S2}$, 4S	Set Inputs (Active LOW)
4, 7, 9, 13	1Q to 4Q	Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



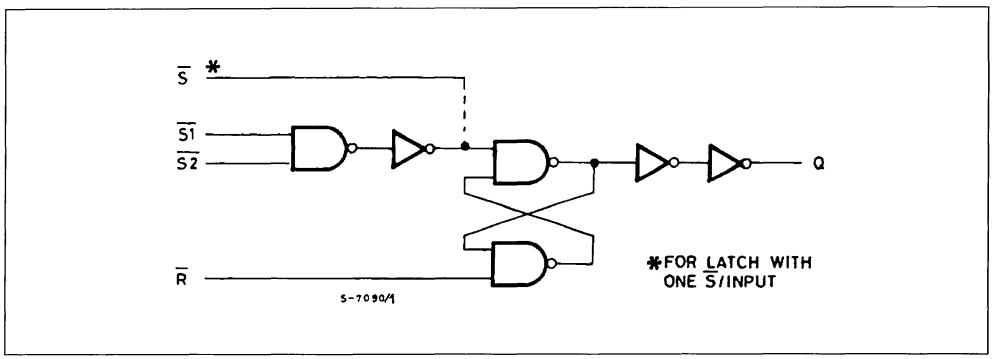
TRUTH TABLE

$\overline{S}$ #	$\overline{R}$	Q
H	H	Q0
L	H	H
H	L	L
L	L	H

NOTE: Q0 = THE LEVEL OF Q BEFORE THE INDICRTED INPUT CONDITION WAS ESTABLISHED.

\# FOR LATCHES WITH DOUBLE S INPUT:
H = BOTH S INPUTS HIGH
L = ONE OF BOTH INPUTS LOW

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

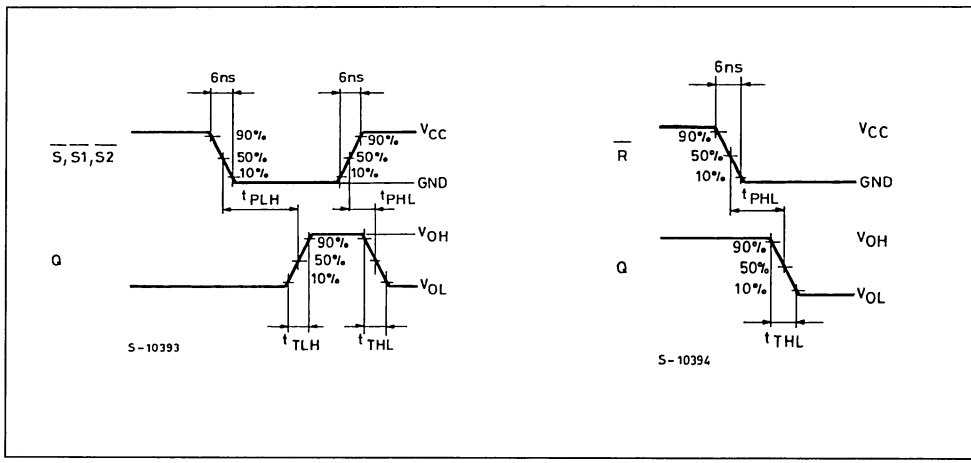
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				2		20		40	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

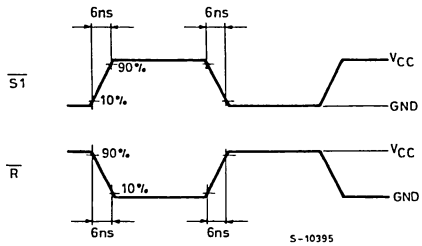
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (S1, S2 - Q)	2.0			45	130		165		195	ns
		4.5			15	26		33		39	
		6.0			13	22		28		33	
t_{PLH} t_{PHL}	Propagation Delay Time (S - Q)	2.0			38	100		125		150	ns
		4.5			12	20		25		30	
		6.0			10	17		21		26	
t_{PHL}	Propagation Delay Time ($\overline{R}$ - Q)	2.0			42	120		150		180	ns
		4.5			14	24		30		36	
		6.0			12	20		26		31	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				18						pF

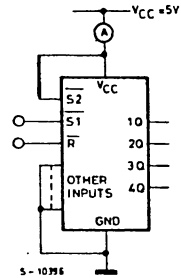
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



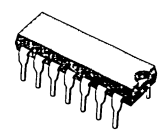
TEST CIRCUIT I_{CC} (Opr.)



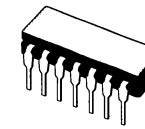


9 BIT PARITY GENERATOR

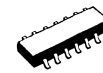
- HIGH SPEED
  t_{PD} = 22 ns (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) at T_A = 25 °C 6 V
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V to 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS280



B1R
(Plastic Package)



F1R
(Ceramic Package)



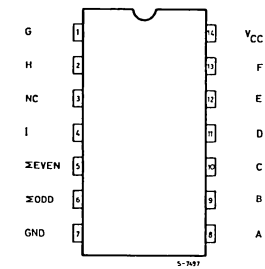
M1R
(Micro Package)

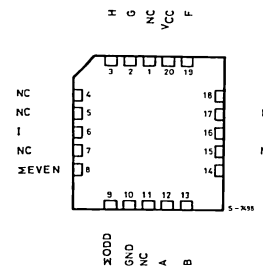
C1R
(Chip Carrier)

ORDER CODES :

M54HC280F1R M74HC280M1R
M74HC280B1R M74HC280C1R

PIN CONNECTIONS (top view)





NC =
No Internal
Connection

DESCRIPTION

The M54/74HC280 is a high speed CMOS 9-BIT PARITY GENERATOR fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low consumption.

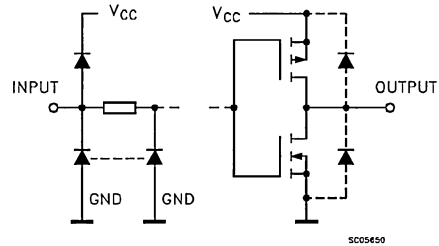
It is composed of nine data inputs (A to I) and odd/even parity outputs (Σ ODD and Σ EVEN). The nine data inputs contro! the output conditions. When the number of high level inputs is odd, ΣODD output is kept high and ΣEVEN output low. Conversely, when the number is even , ΣEVEN output is kept high and ΣODD low.

This IC generates either odd or even parity making it flexible application.

The word-length capability is easily expanded by cascading.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

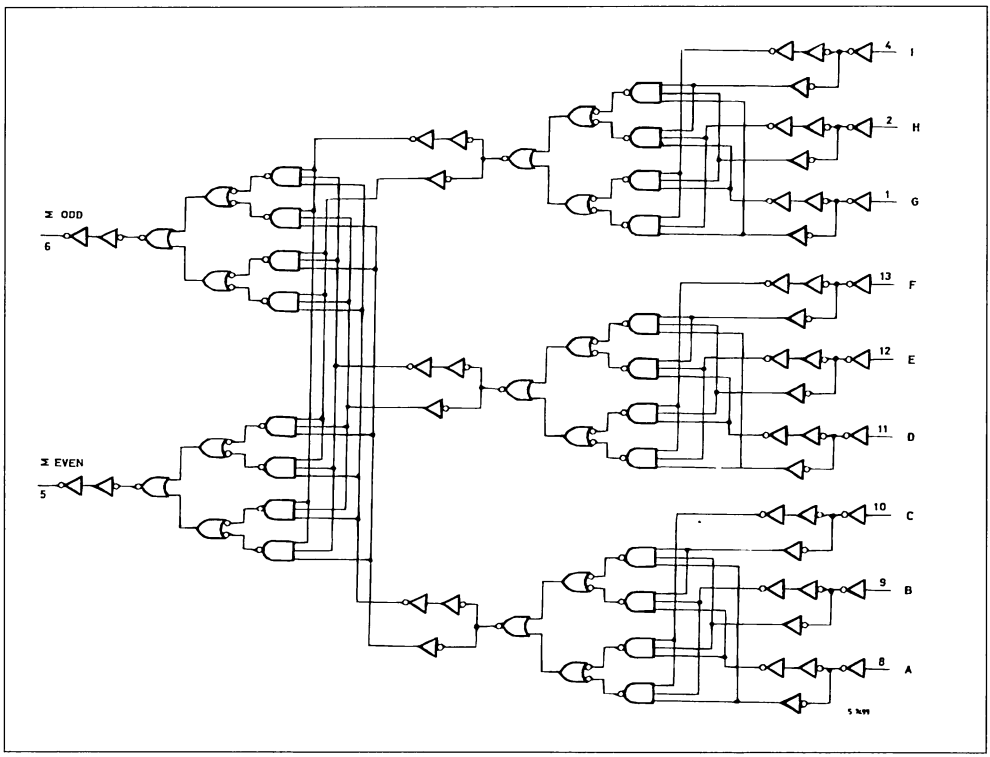
INPUT AND OUTPUT EQUIVALENT CIRCUIT



TRUTH TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUT	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

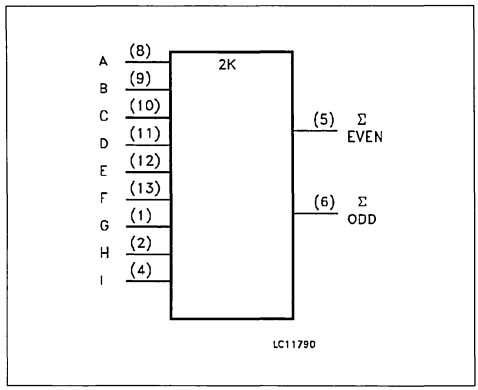
LOGIC DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
5, 6	Σ EVEN, Σ ODD	Parity Outputs
8, 9, 10, 11, 12, 13, 1, 2, 4	A to I	Data Inputs
3	NC	No Connection
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

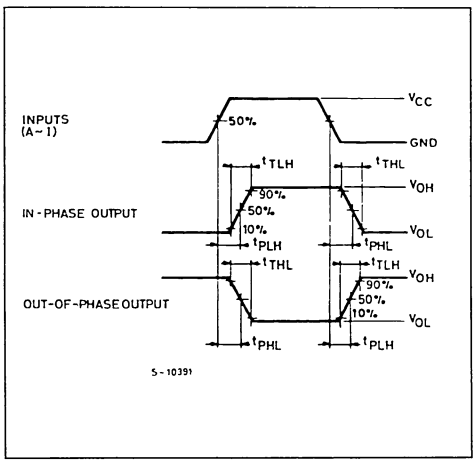
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

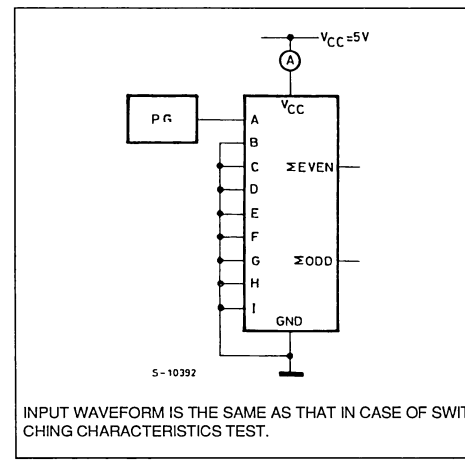
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q)	2.0			80	200		250		290	ns
		4.5			26	40		50		58	
		6.0			22	34		43		49	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				61						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



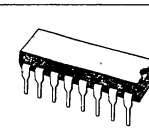
TEST CIRCUIT I_{CC} (Opr.)



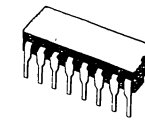
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

4 BIT BINARY FULL ADDER

- HIGH SPEED
  t_{PD} = 17 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- FULL-CARRY LOOK-AHEAD ACROSS THE FOUR BITS
- PARTIAL LOOK-AHEAD WITH THE ECONOMY OF RIPPLY CARRY
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS283



B1R
(Plastic Package)



F1R
(Ceramic Package)

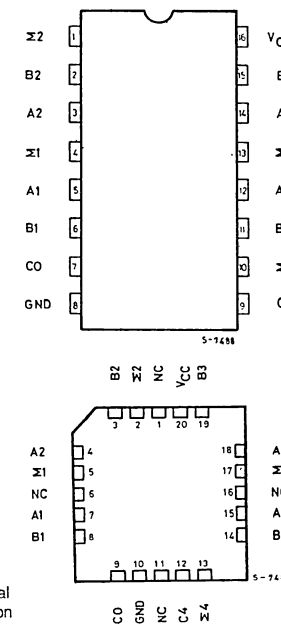
M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HC283F1R M74HC283M1R
M74HC283B1R M74HC283C1R

PIN CONNECTIONS (top view)



NC =
No Internal
Connection

DESCRIPTION

The M54/74HC283 is a high-speed CMOS 4-BIT BINARY FULL ADDER fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

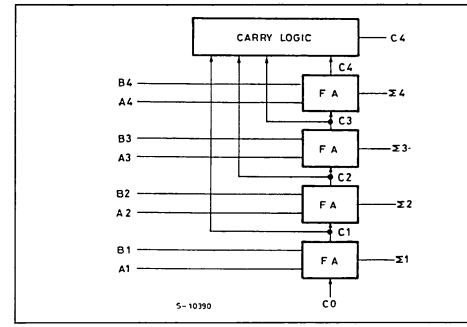
Sum (Σ) outputs are provided for each bit and a resultant carry (C4) is obtained from the fourth bit. This adder features full internal look ahead across all four bits. A 4 x n binary adder is easily built up by cascading without any additional logic.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

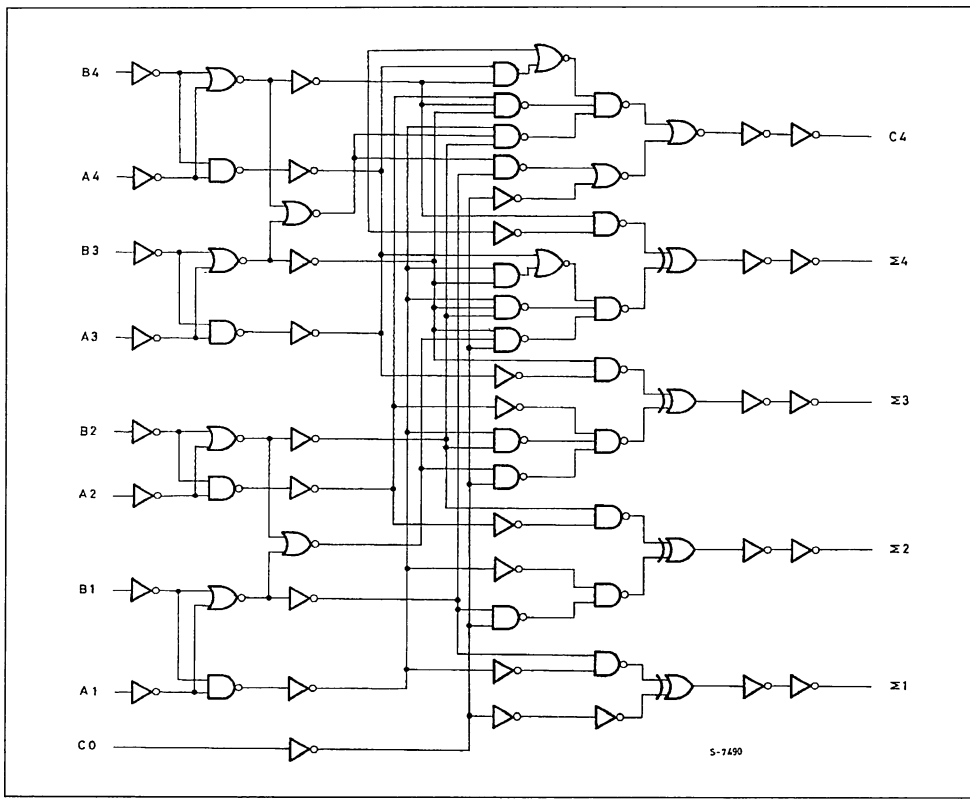
TRUTH TABLE (1 bit)

INPUTS			OUTPUTS	
Bn	An	Cn-1	Σn	Cn
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

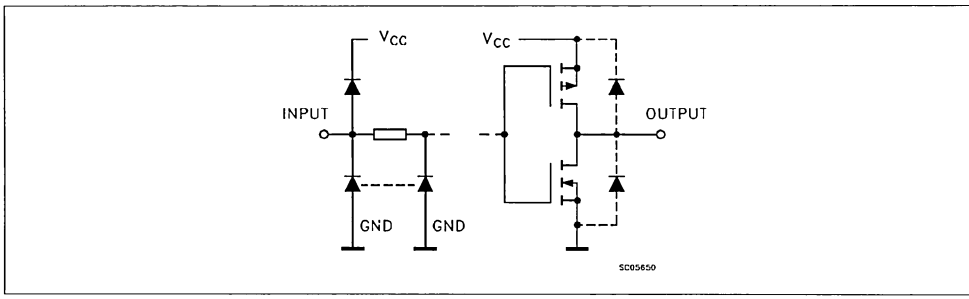
BLOCK DIAGRAM



LOGIC DIAGRAM



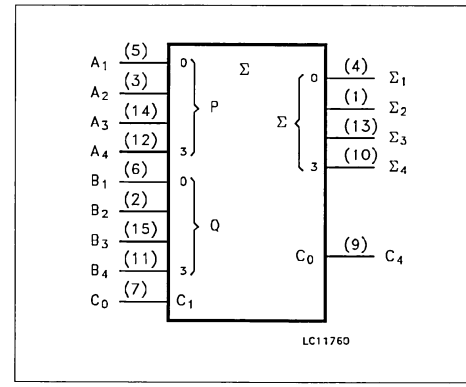
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
4, 1, 13, 10	Σ1 to Σ4	Sum Outputs
5, 3, 14, 12	A1 to A4	A Operand Inputs
6, 2, 15, 11	B1 to B4	B Operand Inputs
7	C0	Carry Input
9	C4	Carry Output
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series		-55 to +125	°C
	M74HC Series		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

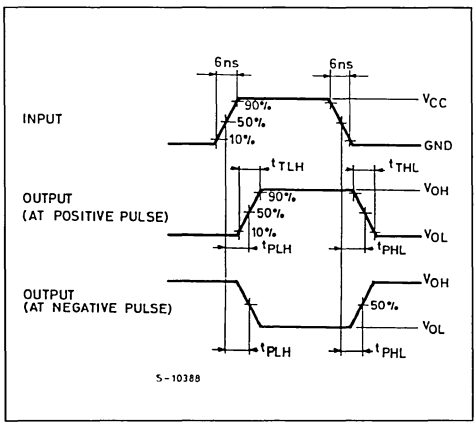
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

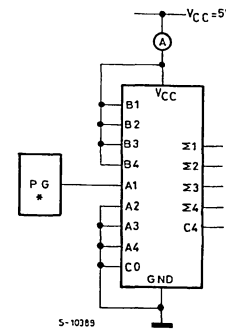
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (An, Bn - Σn)	2.0			95	210		265		315	ns
		4.5			27	42		53		63	
		6.0			22	36		45		54	
t_{PLH} t_{PHL}	Propagation Delay Time (An, Bn - C4)	2.0			80	195		245		295	ns
		4.5			25	39		49		59	
		6.0			20	33		42		50	
t_{PLH} t_{PHL}	Propagation Delay Time (C0 - Σn)	2.0			60	150		190		225	ns
		4.5			20	30		38		45	
		6.0			17	26		32		38	
t_{PLH} t_{PHL}	Propagation Delay Time (C0 - C4)	2.0			60	150		190		225	ns
		4.5			20	30		38		45	
		6.0			17	26		32		38	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				126						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)

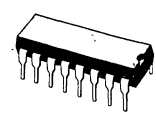


INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

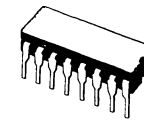
M54/74HC292/7292
M54/74HC294/7294

PROGRAMMABLE DIVIDER/TIMER

- HIGH SPEED
  f_{MAX} = 70 MHz (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 mA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS292/294



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

DESCRIPTION

The 54/74HC292/7292 and HC294/7294 are high speed CMOS PROGRAMMABLE DIVIDER/TIMER fabricated with silicon C^2MOS technology.

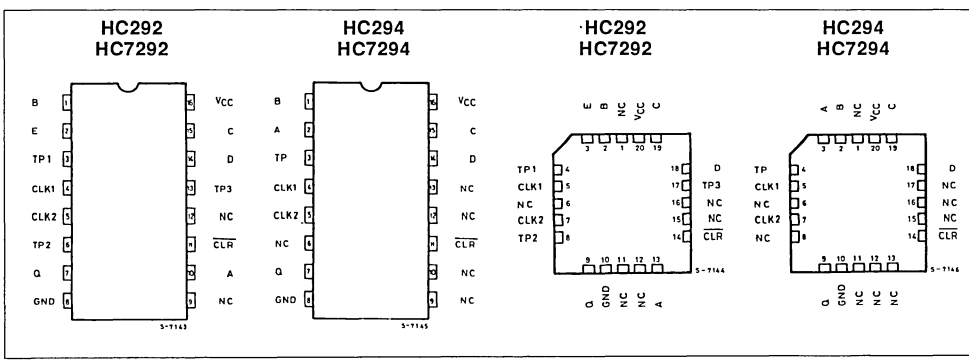
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These devices are programmable frequency dividers. The types have two clock inputs, either one may be used for clock gating. (see the function table). The HC292/7292 can divide from 2^2 to 2^{31}, and the HC294/7294 can divide from 2^2 to 2^{15}. The types feature an active-low clear input to initialize the state of all flip-flops. To facilitate incoming inspection, test points are provided. (TP1, TP2 and TP3 on the HC292/7292 and TP on the HC294/7294). All inputs are equipped with protection circuits against static discharge and transient excess voltage.

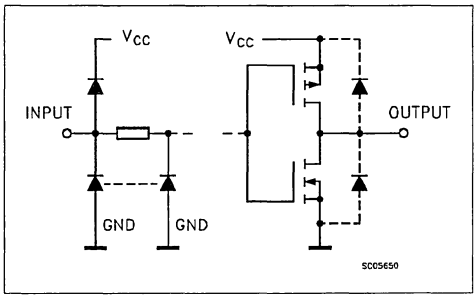
HC292/294 have Q output with "Totem pole" configuration and test point TP with "Open Drain" output configuration.

HC7292/7294 have all outputs "Totem Pole".

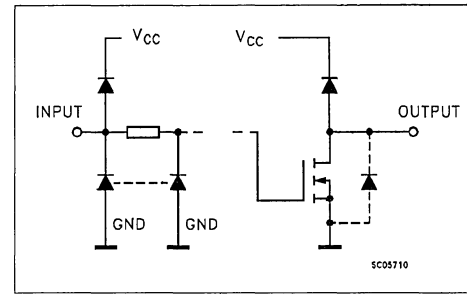
PIN CONNECTION (top view)



INPUT AND OUTPUT EQUIVALENT CIRCUIT (TOTEM POLE OUTPUT)



INPUT AND OUTPUT EQUIVALENT CIRCUIT (OPEN DRAIN OUTPUT, HC292/294)



PIN DESCRIPTION (HC292/7292)

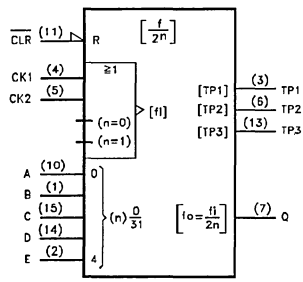
PIN No	SYMBOL	NAME AND FUNCTION
4, 5	CLK1, CLK2	input Clock
1, 2, 10, 14, 15	A to E	Program Inputs
3, 6, 13	TP1, TP2, TP3	Test Point Outputs
11	$\overline{CLR}$	Clear (Active LOW)
7	Q	Output
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

PIN DESCRIPTION (HC294/7294)

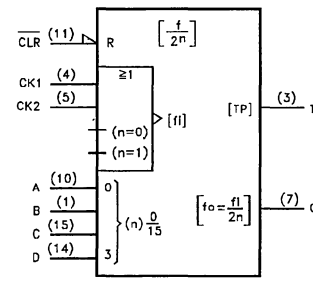
PIN No	SYMBOL	NAME AND FUNCTION
4, 5	CLK1, CLK2	input Clock
1, 2, 14, 15	A to D	Program Inputs
3	TP1	Test Point Output
11	$\overline{CLR}$	Clear (Active LOW)
7	Q	Output
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS

HC292/HC7292



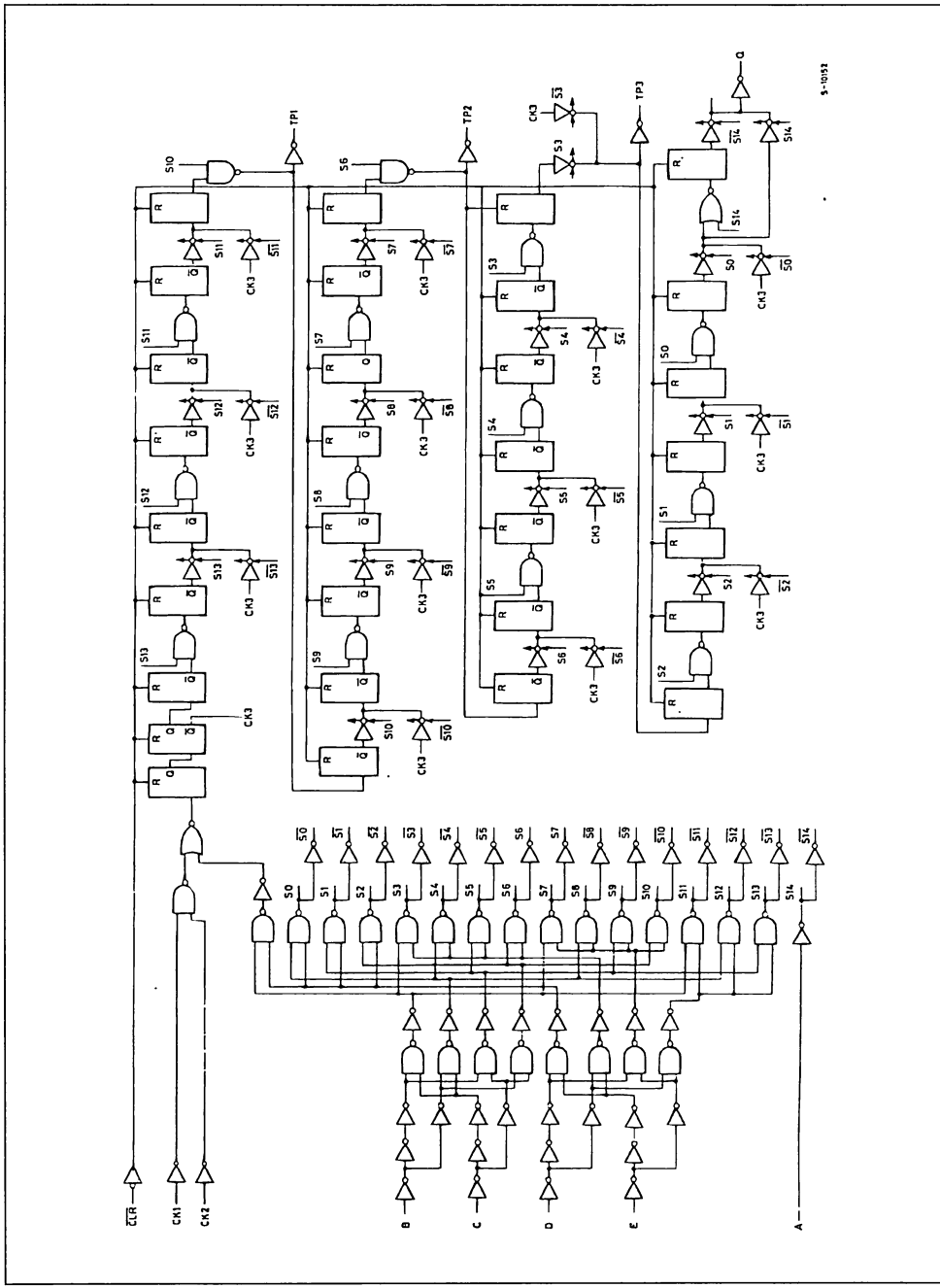
HC294/HC7294



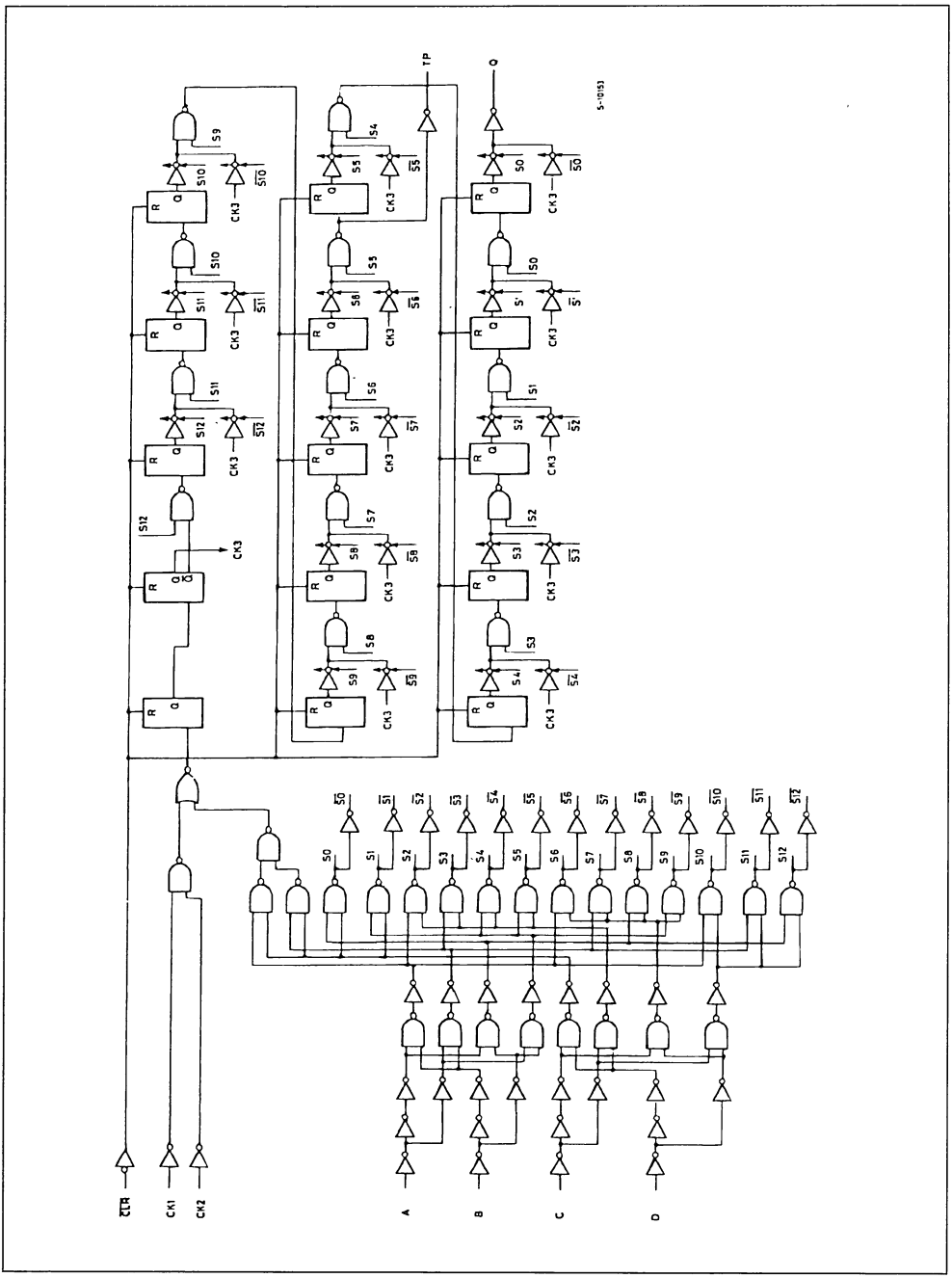
TRUTH TABLE

$\overline{CLEAR}$	CLOCK1	CLOCK2	Q OUTPUT MODE
L	X	X	CLEARED TO L
H	⎍	L	UP COUNT
H	L	⎍	
H	H	X	NO CHANGE
H	X	H	

LOGIC DIAGRAM (HC292/7292)



LOGIC DIAGRAM (HC294/7294)



FUNCTION TABLE (HC292/7292)

PROGRAMMING INPUTS					FREQUENCY DIVISION							
					Q		TP1		TP2		TP3	
E	D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	L	2^2	4	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	L	H	H	2^3	8	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	L	L	2^4	16	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	L	H	2^5	32	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	H	L	2^6	64	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	H	H	2^7	128	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	H	L	L	L	2^8	256	2^9	512	2^{17}	131,072	2^2	4
L	H	L	L	H	2^9	512	2^9	512	2^{17}	131,072	2^2	4
L	H	L	H	L	2^{10}	1,024	2^9	512	2^{17}	131,072	2^4	16
L	H	L	H	H	2^{11}	2,048	2^9	512	2^{17}	131,072	2^4	16
L	H	H	L	L	2^{12}	4,096	2^9	512	2^{17}	131,072	2^6	64
L	H	H	L	H	2^{13}	8,192	2^9	512	2^{17}	131,072	2^6	64
L	H	H	H	L	2^{14}	16,384	2^9	512	Disabled Low		2^8	256
H	H	H	H	H	2^{15}	32,768	2^9	512	Disabled Low		2^8	256
H	L	L	L	L	2^{16}	65,536	2^9	512	2^3	8	2^{10}	1,024
H	L	L	L	H	2^{17}	131,072	2^9	512	2^3	8	2^{10}	1,024
H	L	L	H	L	2^{18}	262,144	2^9	512	2^5	32	2^{12}	4,096
H	L	L	H	H	2^{19}	524,288	2^9	512	2^5	32	2^{12}	4,096
H	L	H	L	L	2^{20}	1,048,576	2^9	512	2^7	128	2^{14}	16,384
H	L	H	L	H	2^{21}	2,097,152	2^9	512	2^7	128	2^{14}	16,384
H	L	H	H	L	2^{22}	4,194,304	Disabled Low		2^9	512	2^{16}	65,536
H	L	H	H	H	2^{23}	8,388,608	Disabled Low		2^9	512	2^{16}	65,536
H	H	L	L	L	2^{24}	16,777,216	2^3	8	2^{11}	2,048	2^{18}	262,144
H	H	L	L	H	2^{25}	33,554,432	2^3	8	2^{11}	2,048	2^{18}	262,144
H	H	L	H	L	2^{26}	67,108,864	2^5	32	2^{13}	8,192	2^{20}	1,048,576
H	H	L	H	H	2^{27}	134,217,728	2^5	32	2^{13}	8,192	2^{20}	1,048,576
H	H	H	L	L	2^{28}	268,435,456	2^7	128	2^{15}	32,768	2^{22}	4,194,304
H	H	H	L	H	2^{29}	536,870,912	2^7	128	2^{15}	32,768	2^{22}	4,194,304
H	H	H	H	L	2^{30}	1,073,741,824	2^9	512	2^{17}	131,072	2^{24}	16,777,216
H	H	H	H	H	2^{31}	2,147,483,648	2^9	512	2^{17}	131,072	2^{24}	16,777,216

FUNCTION TABLE (HC294/7294)

PROGRAMMING INPUTS				FREQUENCY DIVISION			
				Q		TP	
D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit
L	L	H	L	2^2	4	2^9	512
L	L	H	H	2^3	8	2^9	512
L	H	L	L	2^4	16	2^9	512
L	H	L	H	2^5	32	2^9	512
L	H	H	L	2^6	64	2^9	512
L	H	H	H	2^7	128	Disabled Low	
H	L	L	L	2^8	256	2^2	4
H	L	L	H	2^9	512	2^3	8
H	L	H	L	2^{10}	1,024	2^4	16
H	L	H	H	2^{11}	2,048	2^5	32
H	H	L	L	2^{12}	4,096	2^6	64
H	H	L	H	2^{13}	8,192	2^7	128
H	H	H	L	2^{14}	16,384	2^8	256
H	H	H	H	2^{15}	32,768	2^9	512

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

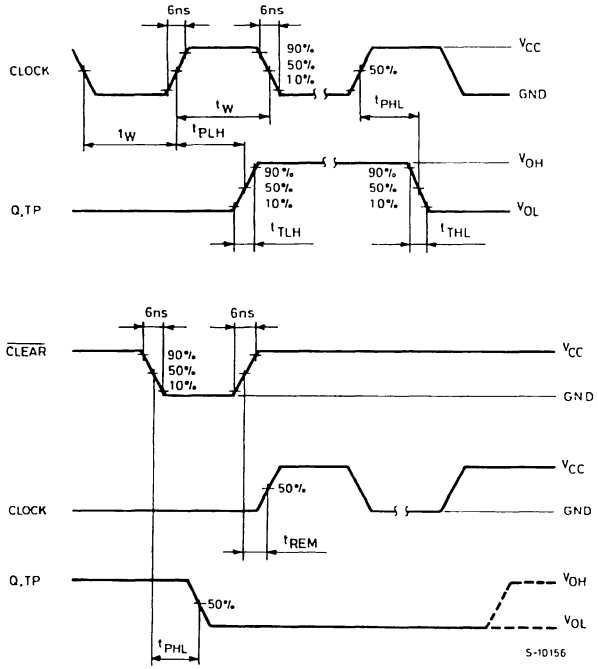
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage (Q)	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OH}	High Level Output Voltage (TP) (for HC7292 HC7294 only)	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-1.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-1.3 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage (Q)	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
V_{OL}	Low Level Output Voltage (TP)	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 1.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 1.3 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time (Q)	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{TLH} t_{THL}	Output Transition Time (TP)	2.0			116	225		280		340	ns
		4.5			29	45		56		68	
		6.0			25	38		48		57	
t_{PLH} t_{PHL}	Propagation Delay Time (CK - Q)	2.0	for HC292/7292		160	350		440		ns	
		4.5			46	70		88		105	
		6.0			39	60		75		90	
t_{PLH} t_{PHL}	Propagation Delay Time (CK - Q)	2.0	for HC294/7294		145	330		415			ns
		4.5			43	66		83		15	
		6.0			37	56		71		84	
t_{PHL}	Propagation Delay Time (CLR - Q)	2.0	for HC292/7292		130	320		400		210	ns
		4.5			42	64		80		100	
		6.0			36	54		68		81	
t_{PHL}	Propagation Delay Time (CLR - Q)	2.0	for HC294/7294		110	260		325		390	ns
		4.5			34	52		65		78	
		6.0			29	44		55		66	
f_{MAX}	Maximum Clock Frequency	2.0	for HC292/7292	5.0	21		4		3.4		MHz
		4.5		27	64		22		18		
		6.0		32	75		26		21		
f_{MAX}	Maximum Clock Frequency	2.0	for HC294/7294	6.0	20		5		4		MHz
		4.5		32	64		26		21		
		6.0		38	75		31		25		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0			40	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		20	
$t_{W(L)}$	Minimum Pulse Width (CLEAR)	2.0	for HC292/7292		48	125		155		190	ns
		4.5			12	25		31		38	
		6.0			10	21		26		32	
$t_{W(L)}$	Minimum Pulse Width (CLEAR)	2.0	for HC294/7294		40	100		125		150	ns
		4.5			10	20		25		30	
		6.0			9	17		21		26	
t_{REM}	Minimum Removal Time	2.0	for HC292/7292			5		5		5	ns
		4.5				5		5		5	
		6.0				5		5		5	
t_{REM}	Minimum Removal Time	2.0	for HC294/7294			0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
C_{IN}	Input Capacitance				5	10		10			pF
C_{PD} (*)	Power Dissipation Capacitance		for HC292/7292 for HC294/7294		21 23						pF

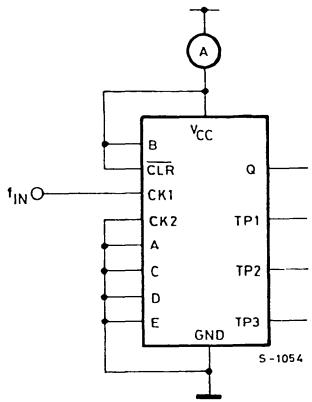
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

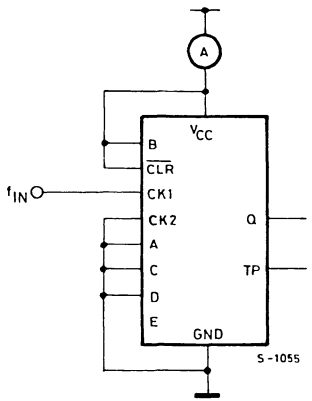


TEST CIRCUIT I_{CC} (Opr.)

HC292/HC7292



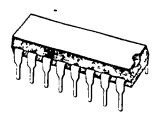
HC294/HC7294



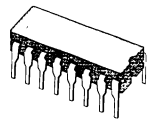
INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

QUAD 2 CHANNEL MULTIPLEXER/REGISTER

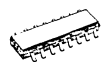
- HIGH SPEED
  f_{MAX} = 73 MHz (typ.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS298



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

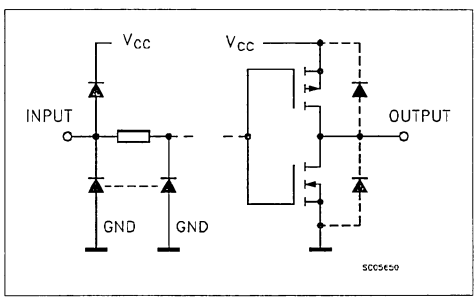
M54HC298F1R M74HC298M1R
M74HC298B1R M74HC298C1R

DESCRIPTION

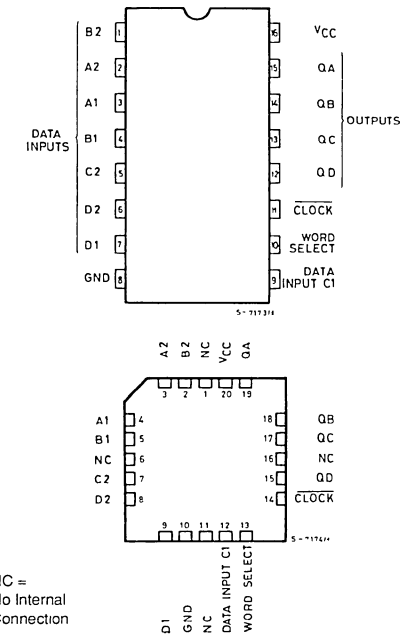
The M54/74HC298 is a high speed CMOS QUAD 2-CHANNEL MULTIPLEXER/REGISTER fabricated in silicon gate C^2MOS technology.

It has the same high speed performance of LSTTL combined with true CMOS low power consumption. These circuits are controlled by the signals WORD SELECT and $\overline{\text{CLOCK}}$. When the WORD SELECT input is taken low Word 1 (A1, B1, C1 and D1) is presented to the input of the flip-flops, and when WORD SELECT is high Word 2 (A2, B2, C2 and D2) is presented to the inputs of the flip-flops. The select word is clocked to the output terminals on the negative edge of the clock pulse. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



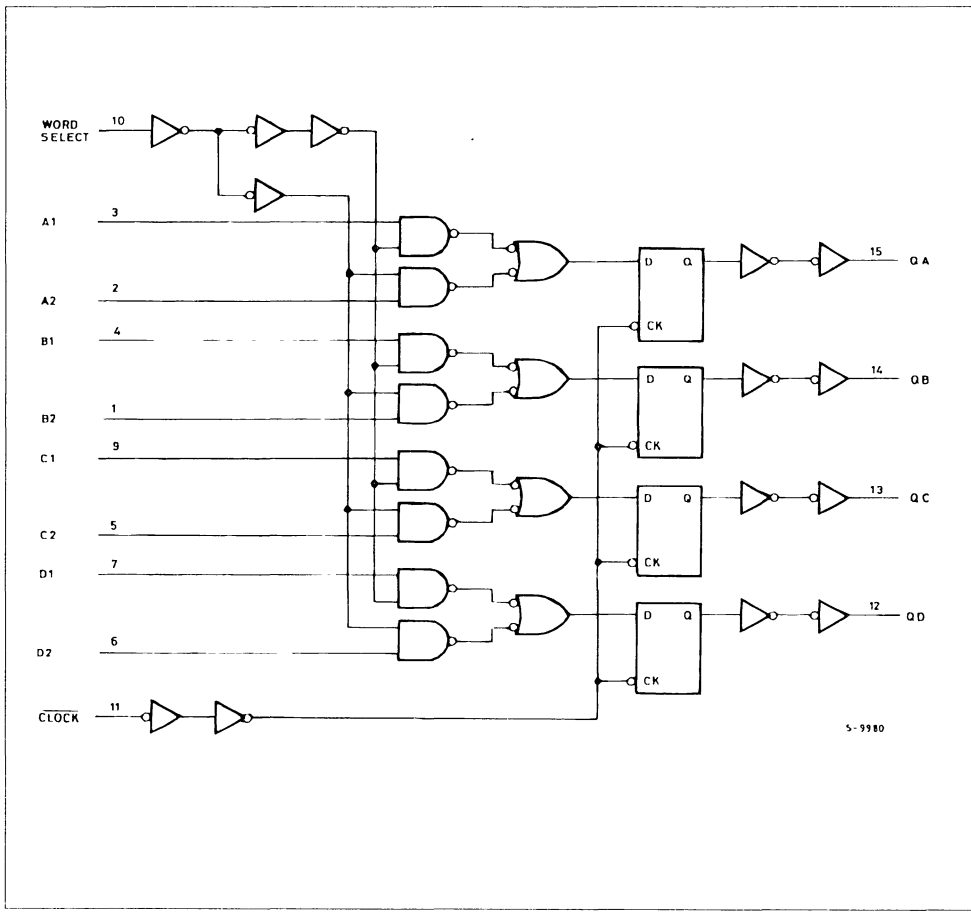
NC =
No Internal
Connection

TRUTH TABLE

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	QA	QB	QC	QD
L	⊓⊔	a1	b1	c1	d1
H	⊓⊔	a2	b2	c2	d2
X	⊔⊓	QA0	QB0	QC0	QD0

X DON'T CARE (INCLUDING TRANSITION)
a1, a2, ETC · THE LEVEL OF STEAY STATE INPUT AT a1, a2, etc
QA0, QB0, ETC THE LEVEL OF QA, QB, ETC ENTERED ON THE MOST RECENT NEGATIVE TRANSITION OF THE CLOCK INPUT

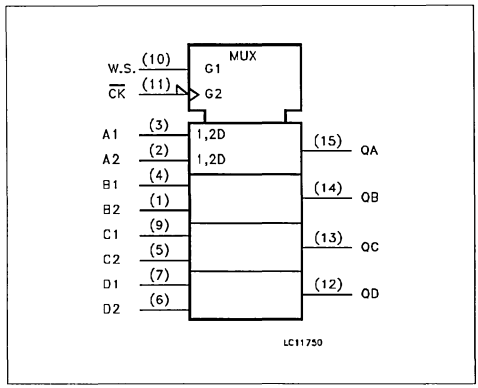
LOGIC DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 5, 6	A2, B2, C2, D2	Word 2 Data Inputs
3, 4, 7, 9	A1, B1, C1, D1	Word 1 Data Inputs
12 to 15	QA to QD	Outputs
10	WORD SELECT	Word Select Input
11	$\overline{CLOCK}$	Clock Input (HIGH to LOW, Edge-triggered)
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied

(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C. 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

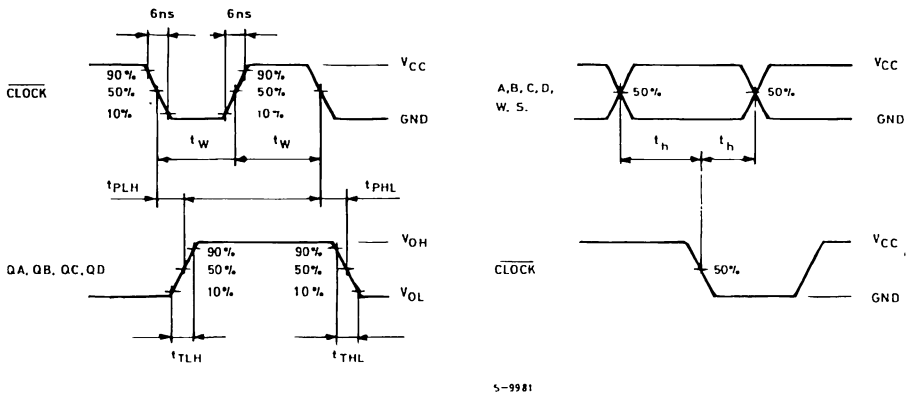
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

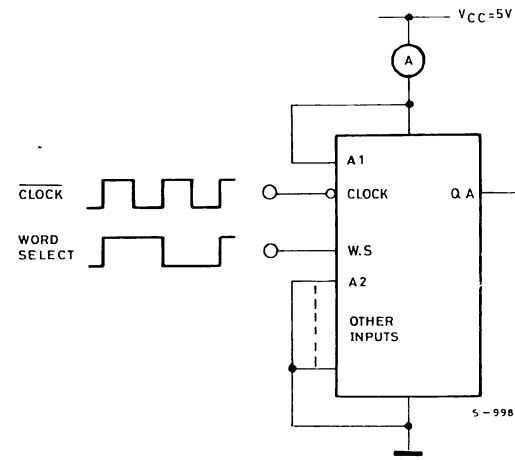
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q)	2.0			45	125		155		190	ns
		4.5			15	25		31		38	
		6.0			13	21		26		32	
f_{MAX}	Maximum Clock Frequency	2.0		7	22		5.6		4 6		MHz
		4.5		35	67		28		23		
		6.0		41	79		33		25		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0			18	75		95		110	ns
		4.5			6	15		19		22	
		6.0			6	13		16		19	
t_s	Minimum Set-up Time (A, B, C, D)	2.0			12	50		65		75	ns
		4.5			3	10		13		15	
		6.0			2	9		11		13	
t_s	Minimum Set-up Time (W. S.)	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			6	13		16		19	
t_h	Minimum Hold Time (A, B, C, D)	2.0				25		30		40	ns
		4.5				5		6		8	
		6.0				4		5		7	
t_h	Minimum Hold Time (W. S.)	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				39						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per bit), and the CPD for operating current can be obtained by the following equation CPD = 27 + 12 x n

SWITCHING CHARACTERISTICS TEST WAVEFORM



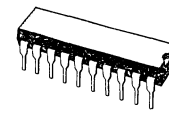
TEST CIRCUIT



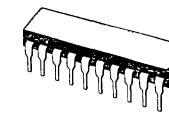
TRANSITION TIME AND V_{IH}, V_{IL} OF INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

HC299 8 BIT PIPO SHIFT REGISTER WITH ASYNCHRONOUS CLEAR
HC323 8 BIT PIPO SHIFT REGISTER WITH SYNCHRONOUS CLEAR

- HIGH SPEED
  f_{MAX} = 42 MHz (TYP.) AT V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS FOR QA' TO QH'
  15 LSTTL LOADS FOR QA TO QH
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.) FOR Q_A, TO Q_H,
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.) FOR Q_A, TO Q_H
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS299



B1R
(Plastic Package)



F1R
(Ceramic Package)

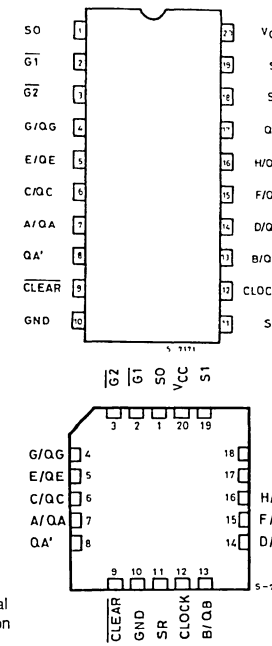
M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

PIN CONNECTIONS (top view)



NC =
No Internal
Connection

DESCRIPTION

The M54/74HC299/323 are high speed CMOS 8-BIT PIPO SHIFT REGISTERS (3-STATE) fabricated with silicon gate C^2MOS technology.

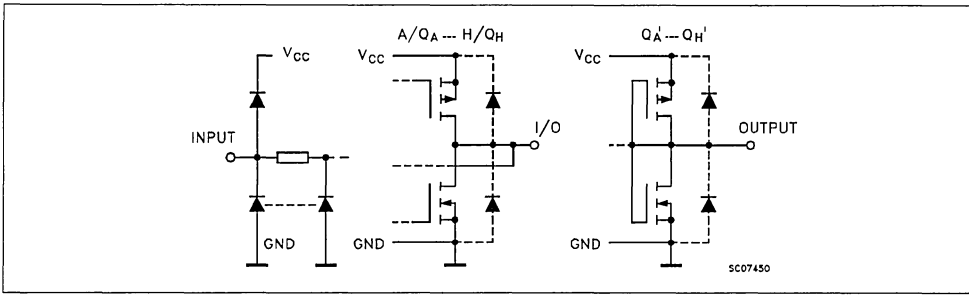
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power consumption.

These devices have four modes (HOLD, SHIFT LEFT, SHIFT RIGHT and LOAD DATA). Each mode is chosen by two function select inputs (S0, S1). When one or both enable inputs, ($\overline{G1}$, $\overline{G2}$) are high, the eight input/output terminals are in the high-impedance state ; however sequential operation or clearing of the register is not affected.

Clear function on the HC299 is asynchronous to CLOCK, while the HC323 is cleared synchronous to clock.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



TRUTH TABLE

MODE	INPUTS							INPUTS/OUTPUTS				OUTPUTS	
	$\overline{CLEAR}$	FUNCTION SELECTED		OUTPUT CONTROL		CLOCK		SERIAL		A/QA	H/QH	QA'	QH'
		S1	S0	$\overline{G1}$ *	$\overline{G2}$ *	(299)	(323)	SL	SR				
Z	L	H	H	X	X	X		X	X	Z	Z	L	L
CLEAR	L	L	X	L	L	X	⎍	X	X	L	L	L	L
	L	X	L	L	L	X	⎍	X	X	L	L	L	L
HOLD	H	L	L	L	L	X		X	X	QA0	QH0	QA0	QH0
SHIFT RIGHT	H	L	H	L	L	⎍		X	H	H	QGn	H	QGn
	H	L	H	L	L	⎍		X	L	L	QGn	L	QGn
SHIFT LEFT	H	H	L	L	L	⎍		H	X	QBn	H	QBn	H
	H	H	L	L	L	⎍		L	X	QBn	L	QBn	L
LOAD	H	H	H	X	X	⎍		X	X	a	h	a	h

* When one or both output controls are high, the eight, input/output terminals are in the high impedance state: however sequential operation or clearing of the register is not affected.

Z : HIGH IMPEDANCE

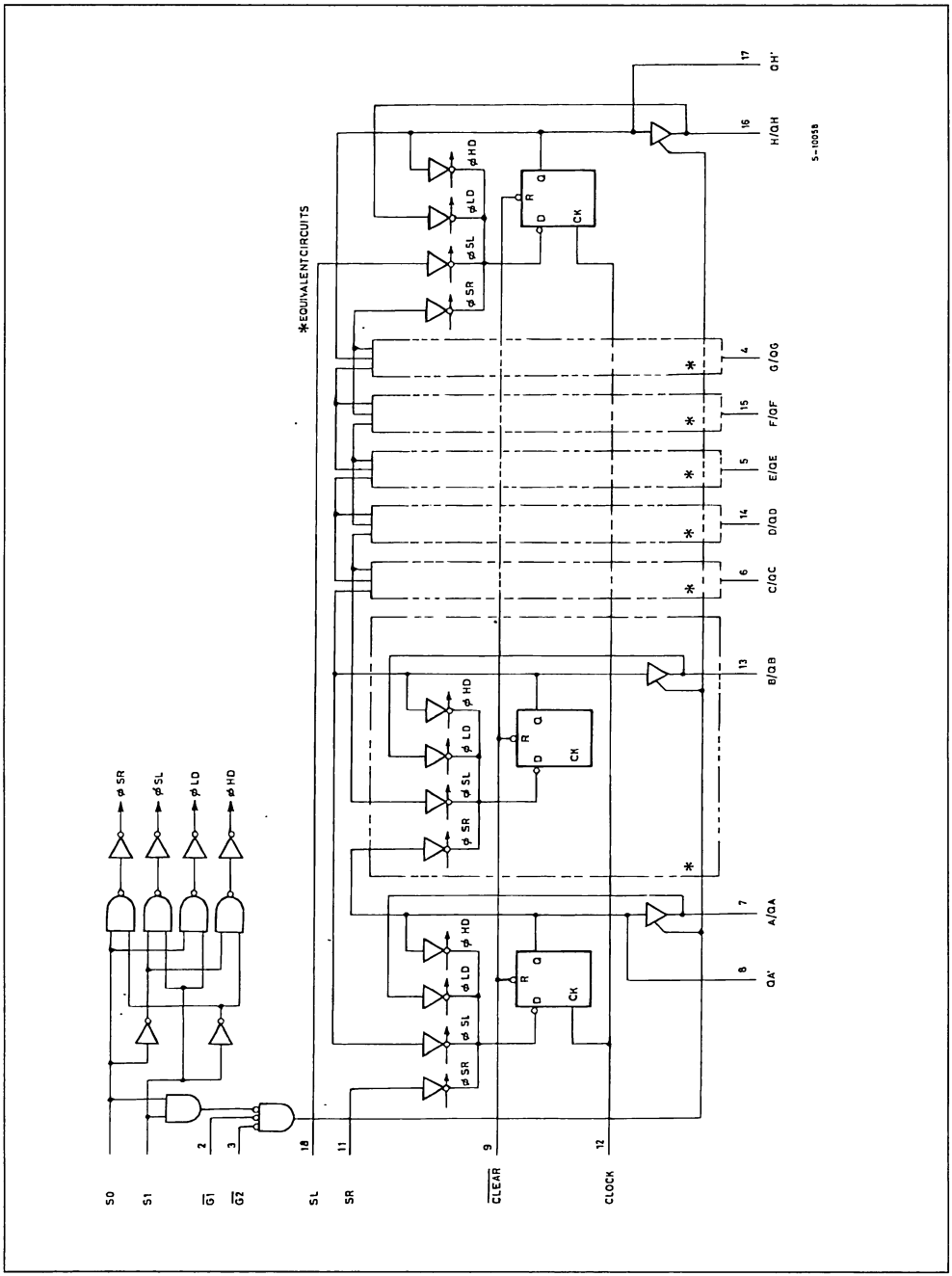
Qn0 : THE LEVEL OF An BEFORE THE INDICATED STEADY STATE INPUT CONDITIONS WERE ESTABLISHED

Qnn : THE LEVEL ON Qn BEFORE THE MOST RECENT ACTIVE TRANSITION INDICATED BY ⎍ OR ⎍

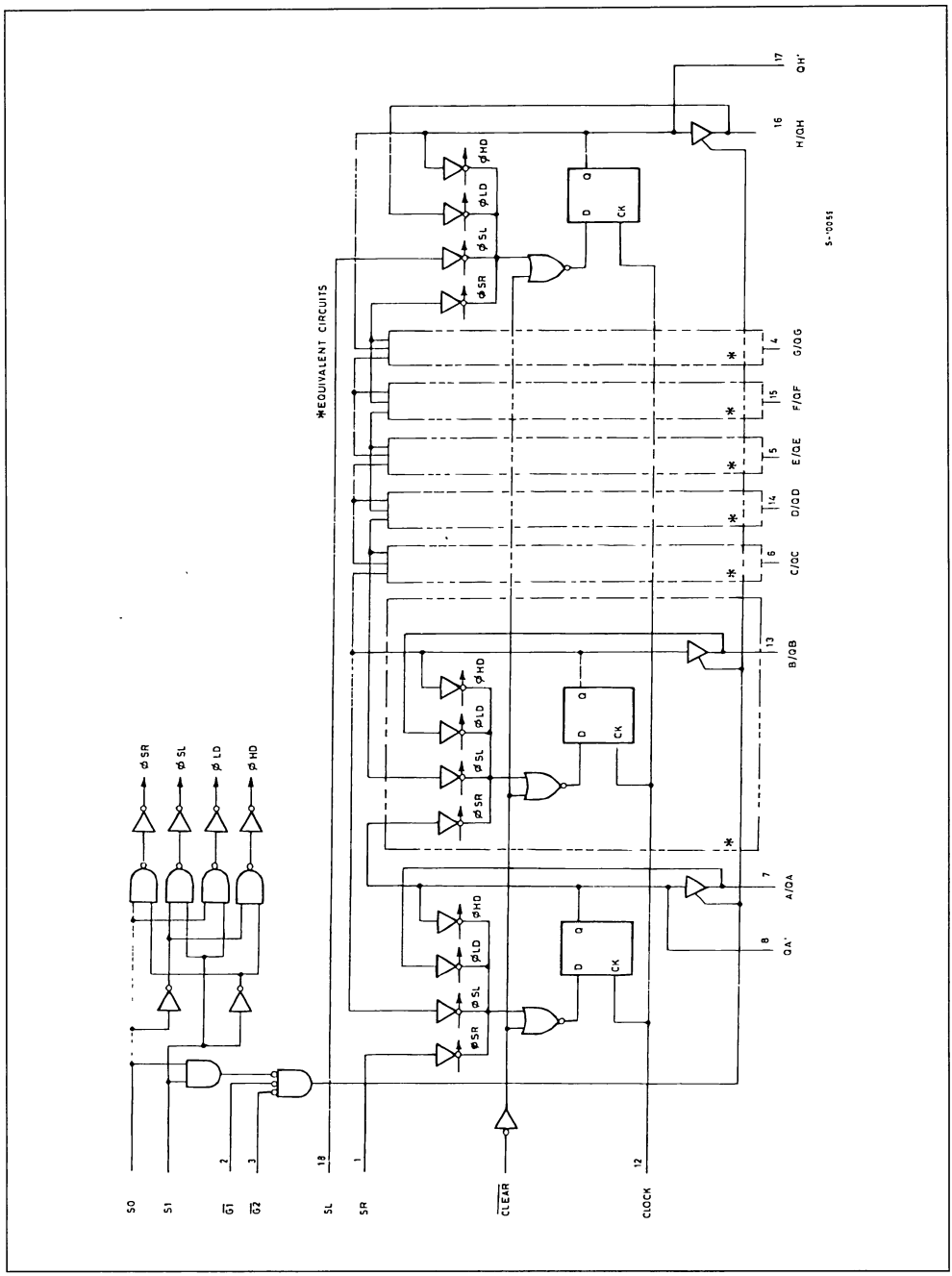
a, h : THE LEVEL OF THE STEADY STATE INPUTS A, H, RESPECTIVELY

X : DON'T CARE

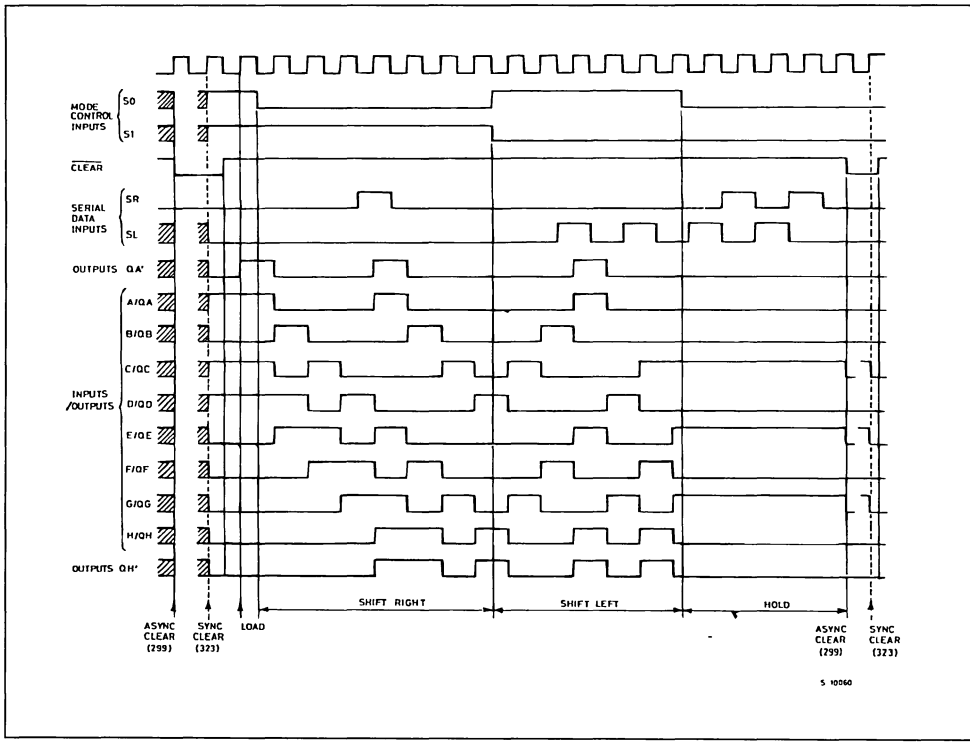
LOGIC DIAGRAM (HC299)



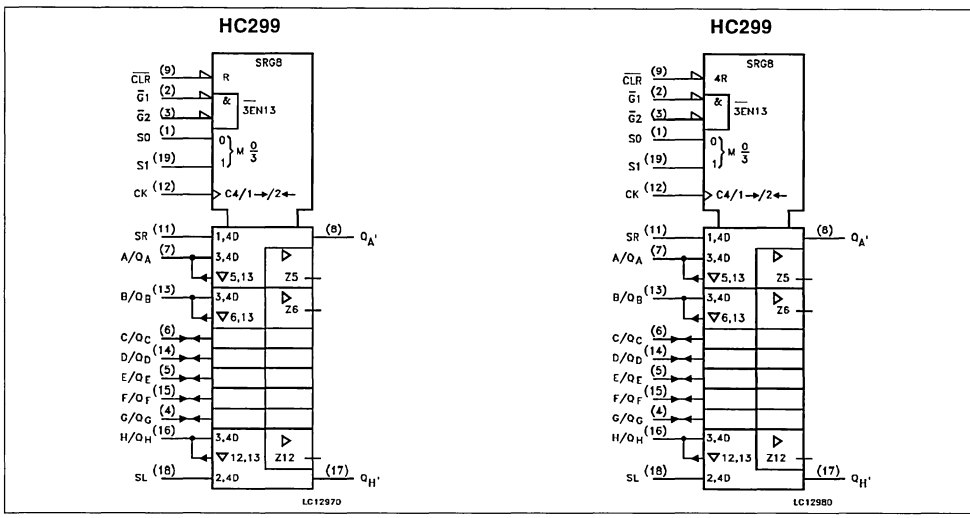
LOGIC DIAGRAM (HC323)



TIMING CHART



IEC LOGIC SYMBOLS



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 19	S0, S1	Mode Select Inputs
2, 3	$\overline{G1}$, $\overline{G2}$	3 State Output Enable Inputs (Active LOW)
7, 13, 6, 14, 5, 15, 4, 16	A/QA to H/QH	Parallel Data Inputs or 3 State Parallel Outputs (Bus Driver)
8, 17	QA' to QH'	Serial Outputs (Standard Output)
9	$\overline{CLEAR}$	Asynchronous Master Reset Input (Active LOW)
11	SR	Serial Data Shift Right Input
12	CLOCK	Clock Input (LOW to HIGH, Edge-triggered)
18	SL	Serial Data Shift Left Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin (QA -QH)	± 35	mA
I_O	DC Output Source Sink Current Per Output Pin (QA' -QH')	±235	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW. ≅ 65 °C derate to 300 mW by 10mW/°C· 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
	QA TO QH	4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
	QA' TO QH'	4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
	QA TO QH	4.5		I_O= 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.33		0.40	
	QA' TO QH'	4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off-state Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

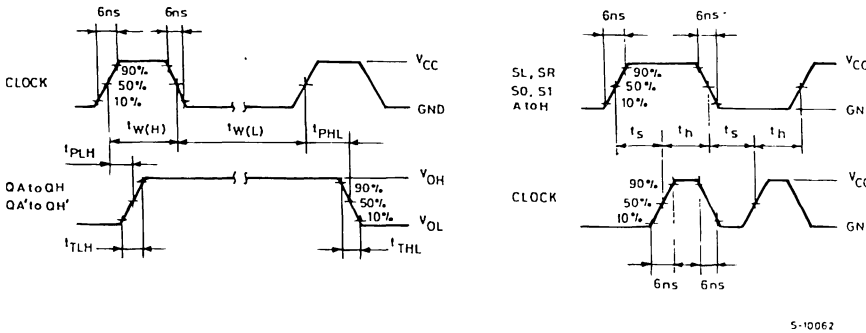
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time (QA, QH)	2.0	50			25	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t_{TLH} t_{THL}	Output Transition Time (QA', QH')	2.0	50			30	75		95		110	ns
		4.5				8	15		19		22	
		6.0				7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CK - QA', QH')	2.0	50			85	170		215		255	ns
		4.5				23	34		43		51	
		6.0				18	29		37		43	
t_{PHL}	Propagation Delay Time (CLR - QA', QH')	2.0	50	for HC299		85	175		220		265	ns
		4.5				24	35		44		53	
		6.0				18	30		37		45	

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

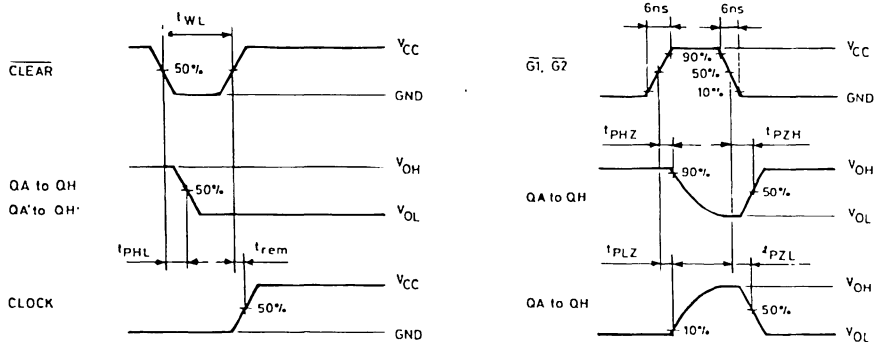
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time (CK - QA, QH)	2.0	50			80	160		200		240	ns
		4.5				21	32		40		48	
		6.0				17	27		34		41	
		2.0	150			100	200		250		300	ns
		4.5				26	40		50		60	
		6.0				21	34		43		51	
t_{PHL}	Propagation Delay Time ($\overline{CLR}$ - QA, QH)	2.0	50	for HC323		85	190		240		285	ns
		4.5				24	38		48		57	
		6.0				18	32		41		48	
		2.0	150	for HC323		105	230		290		345	ns
		4.5				29	46		58		69	
		6.0				22	39		49		59	
t_{PZL} t_{PZH}	3 State Output Enable Time	2.0	50	R_L = 1 KΩ		60	130		165		195	ns
		4.5				17	26		33		39	
		6.0				13	22		28		33	
		2.0	150	R_L = 1 KΩ		78	170		15		255	ns
		4.5				23	34		43		51	
		6.0				17	29		37		43	
t_{PLZ} t_{PHZ}	3 State Output Disable Time	2.0	50	R_L = 1 KΩ		54	150		190		225	ns
		4.5				19	30		38		45	
		6.0				16	26		32		38	
f_{MAX}	Maximum Clock Frequency	2.0	50		6	12		4.8		4		ns
		4.5			30	58		24		20		
		6.0			35	80		28		24		
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CLOCK)	2.0	50				75		95		110	ns
		4.5					15		19		22	
		6.0					13		16		19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLEAR}$)	2.0	50	for HC299			75		95		110	ns
		4.5					15		19		22	
		6.0					13		16		19	
t_s	Minimum Set-up Time (S0, S1) ($\overline{SL}$, $\overline{SR}$, A H) (CLEAR for 323)	2.0	50				100		125		150	ns
		4.5					20		25		30	
		6.0					17		21		26	
t_h	Minimum Hold Time (S0, S1) ($\overline{SL}$, $\overline{SR}$, A H) (CLEAR for 323)	2.0	50				0		0		0	ns
		4.5					0		0		0	
		6.0					0		0		0	
t_{REM}	Minimum Removal Time ($\overline{CLEAR}$)	2.0	50	for HC299			50		65		75	ns
		4.5					10		13		15	
		6.0					9		11		13	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance					170						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

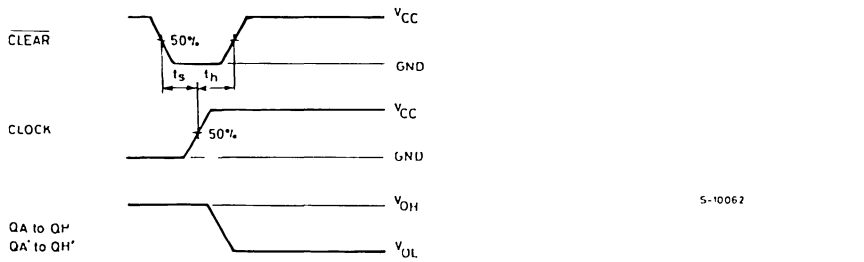
SWITCHING CHARACTERISTICS TEST WAVEFORM



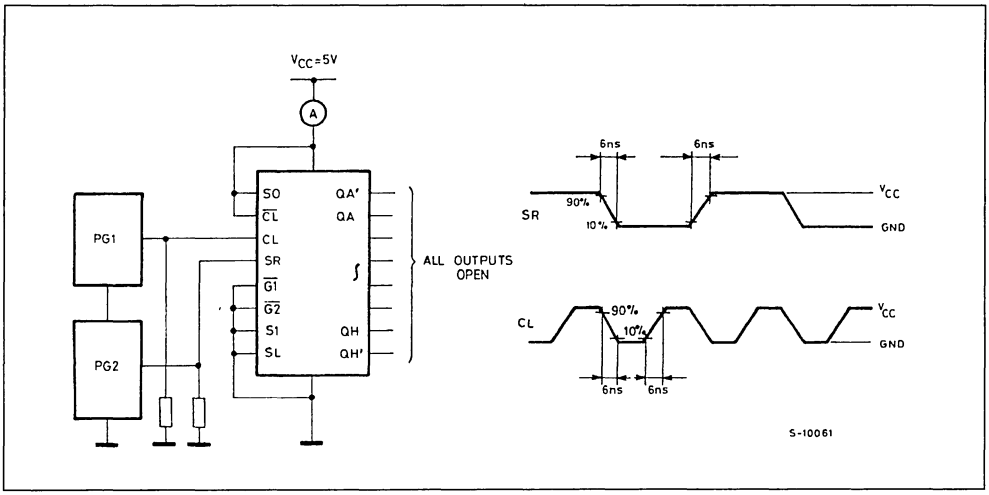
HC299



HC323

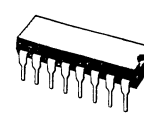


TEST CIRCUIT I_{CC} (Opr.)

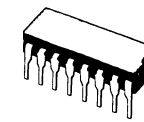


HC352: DUAL 4 CHANNEL MULTIPLEXER(INV.)
HC353: DUAL 4 CHANNEL MULTIPLEXER 3 STATE OUTPUT(INV.)

- HIGH SPEED
  t_{PD} = 12 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- SYMMETRICAL OUTPUT IMPEDANCE
  $I_{OL} = |I_{OH}| = 4$ mA (MIN.)
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL} = 28\ \% V_{CC}$ (MIN.)
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS352/353



B1R
(Plastic Package)



F1R
(Ceramic Package)

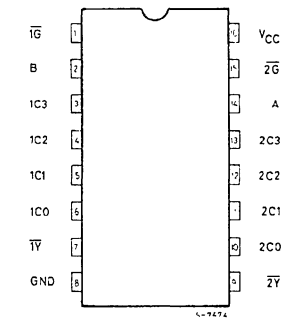
M1R
(Micro Package)

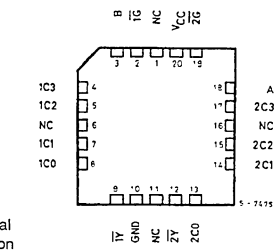
C1R
(Chip Carrier)

ORDER CODES :

M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

PIN CONNECTIONS (top view)





NC =
No Internal
Connection

DESCRIPTION

The M54/74HC352 and M54/74HC353 are high speed CMOS DUAL 4 CHANNEL MULTIPLEXERS INVERTING fabricated with silicon gate C^2MOS technology.

Both achieve high speed operation, similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The designer has a choice of complementary output (HC352) and 3 state output (HC353). Each of these data (1C0-1C3, 2C0-2C3) is selected by the two address inputs A and B.

Separate strobe inputs ($1\overline{G}$, $2\overline{G}$) are provided for each of the two four line sections. Taking the strobe input ($1\overline{G}$, $2\overline{G}$) high inhibits the outputs. The output of HC352 is fixed at logic low level and the output of HC353 has a high impedance, unconditionally.

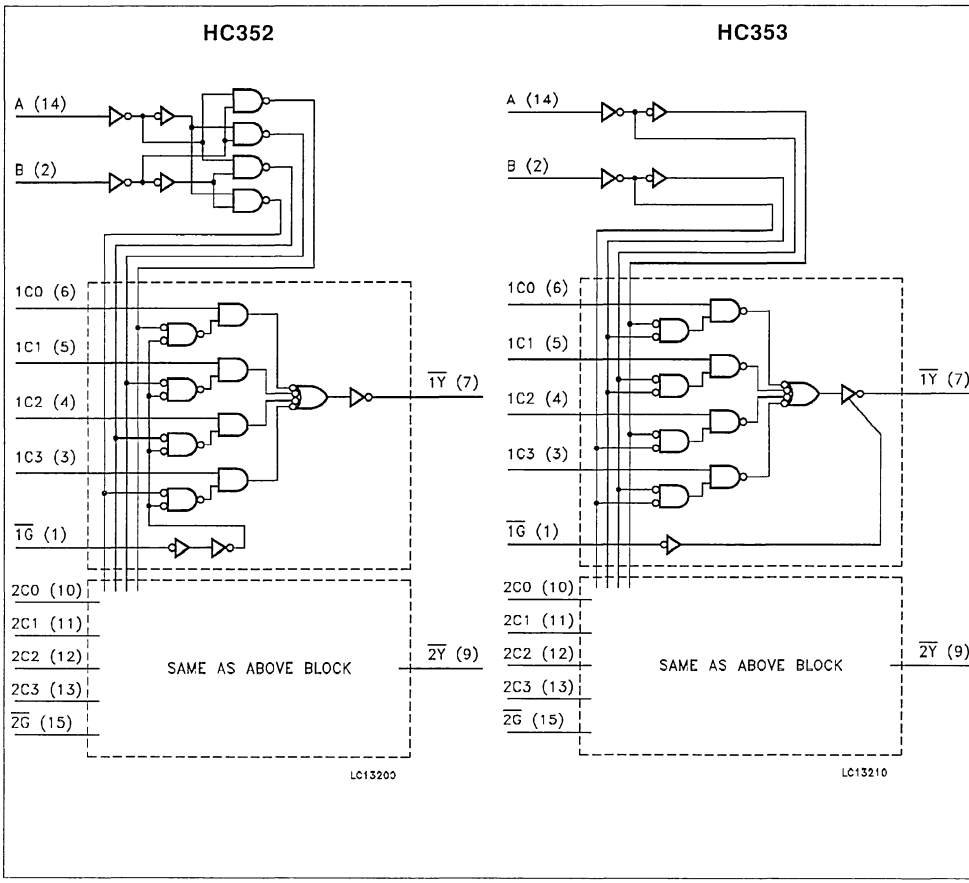
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

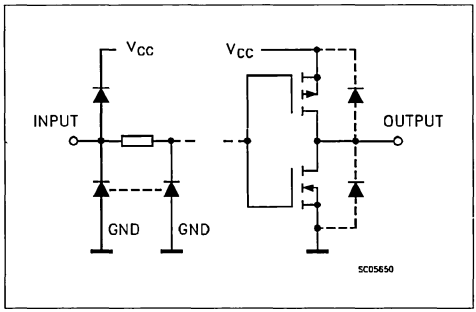
SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT $\overline{Y}$	
B	A	C_0	C_1	C_2	C_3	$\overline{G}$	HC352	HC353
X	X	X	X	X	X	H	H	Z
L	L	L	X	X	X	L	H	H
L	L	H	X	X	X	L	L	L
L	H	X	L	X	X	L	H	H
L	H	X	H	X	X	L	L	L
H	L	X	X	L	X	L	H	H
H	L	X	X	H	X	L	L	L
H	H	X	X	X	L	L	H	H
H	H	X	X	X	H	L	L	L

X: Don't Care
Z: High Impedance

LOGIC DIAGRAM



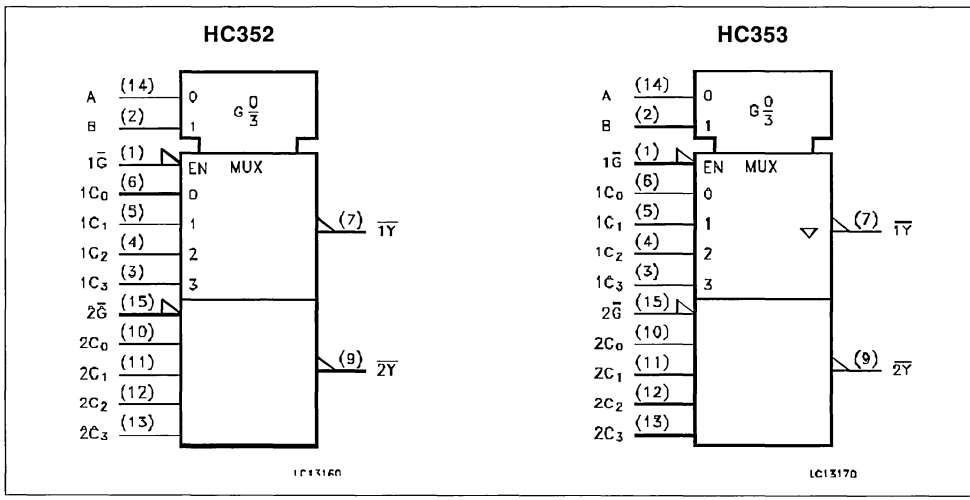
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{1G}$, $\overline{2G}$	Output Enable Inputs
6, 5, 4, 3	$1C_0$ to $1C_3$	Data Input from Source 1
7	$\overline{1Y}$	Data Outputs from Source 1
9	$\overline{2Y}$	Data Outputs from Source 2
10, 11, 12, 13	$2C_0$ to $2C_3$	Data Input from Source 2
14, 2	A, B	Common Data Select Inputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

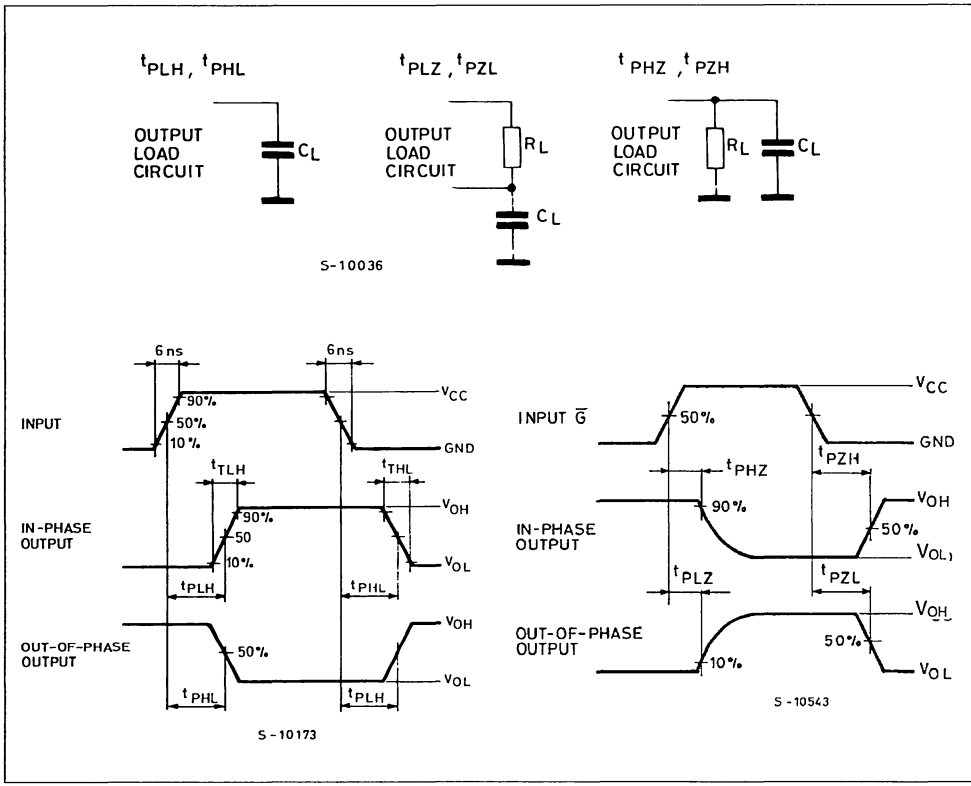
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current (for HC353)	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

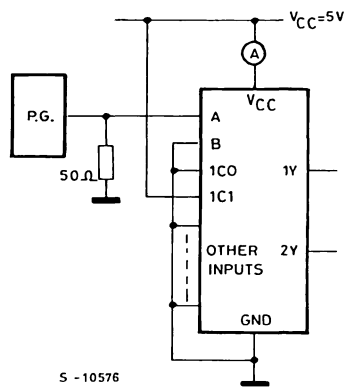
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (Cn - $\overline{Y}$) for HC352	2.0			56	115		145		175	ns
		4.5			14	23		29		35	
		6.0			12	20		25		30	
t_{PLH} t_{PHL}	Propagation Delay Time (A, B - $\overline{Y}$) for HC352	2.0			80	150		190		225	ns
		4.5			20	30		38		45	
		6.0			17	26		33		38	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{G}$ - $\overline{Y}$) for HC352	2.0			40	85		105		130	ns
		4.5			10	17		21		26	
		6.0			9	14		18		22	
t_{PLH} t_{PHL}	Propagation Delay Time (Cn - $\overline{Y}$) for HC353	2.0			64	125		155		95	ns
		4.5			16	25		31		38	
		6.0			14	21		26		32	
t_{PLH} t_{PHL}	Propagation Delay Time (A, B - $\overline{Y}$) for HC353	2.0			84	150		190		225	ns
		4.5			21	30		38		45	
		6.0			18	26		33		38	
t_{PZL} t_{PZH}	Output Enable Time ($\overline{G}$ - $\overline{Y}$) for HC353	2.0	R_L = 1 KΩ		64	115		145		175	ns
		4.5			16	23		29		35	
		6.0			14	20		25		30	
t_{PLZ} t_{PHZ}	Output Disable Time ($\overline{G}$ - $\overline{Y}$) for HC353	2.0	R_L = 1 KΩ		44	100		125		150	ns
		4.5			11	20		25		30	
		6.0			9	17		21		26	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance		for HC352 for HC353		63 61						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORMS

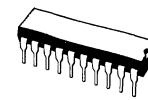


TEST CIRCUIT Icc (Opr.)

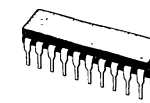


8 CHANNEL MULTIPLEXER/REGISTER (3 STATE)

- HIGH SPEED
  t_{PD} = 24 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS354



B1R
(Plastic Package)



F1R
(Ceramic Package)

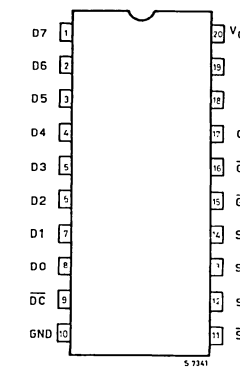
M1R
(Micro Package)

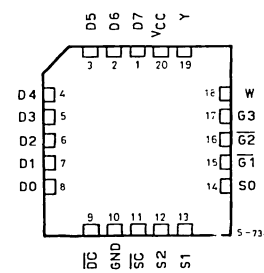
C1R
(Chip Carrier)

ORDER CODES :

M54HC354F1R M74HC354M1R
M74HC354B1R M74HC354C1R

PIN CONNECTIONS (top view)





NC =
No Internal
Connection

DESCRIPTION

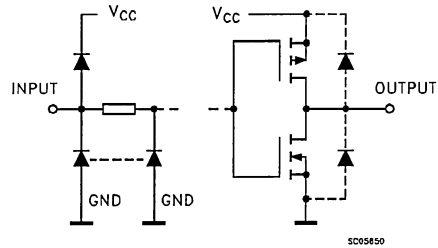
The M54/74HC354 is a high speed CMOS 8-CHANNEL MULTIPLEXER/REGISTER (3-state) fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low consumption.

This device contains an 8 channel digital multiplexer with an 8-bit input data register and a 3-bit address input register with 3-state outputs. The one of eight input data will be provided on the Y output pin (non-inverted output) and W output pin (inverted output) determined by the address data.

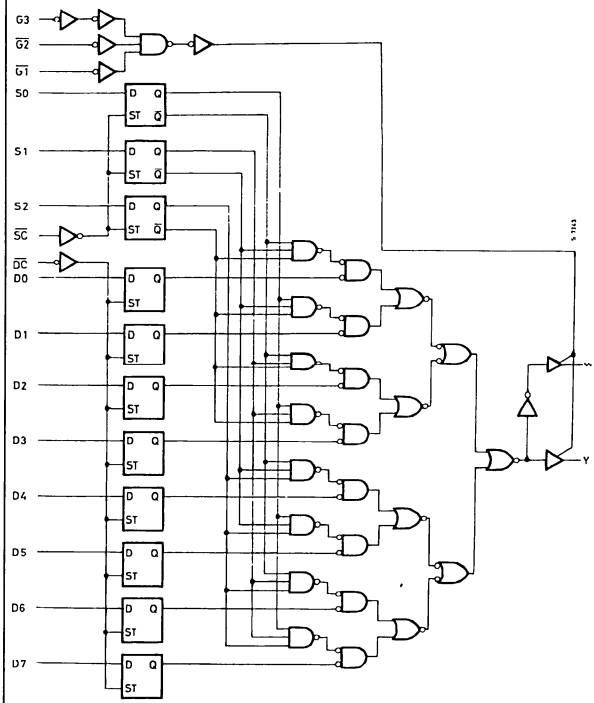
The information at the data inputs (D0 to D7) is stored in the 8-bit latch at the negative pulse on $\overline{DC}$ input. The information at the address inputs (S0 to S2) is stored in the 3-bit latch at the negative pulse on $\overline{SC}$ input. These outputs are disabled to be high-impedance when input $\overline{G1}$ is held high, input $\overline{G2}$ is held high or input G3 is held low. This device is suitable for interfacing with bus lines in a bus organized system.

The M54/74HC354 is similar in function to the M54/74HC356, which has an 8-bit flip-flop as the data register instead of an 8-bit latch. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



LOGIC DIAGRAM



TRUTH TABLE OF INTERNAL LATCH

INPUTS		OUTPUTS	
D	ST	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Qn	$\overline{Qn}$

X: DON'T CARE

Qn: DATA STORED AT THE TRAILING EDGE OF THE MOST RECENT ST PULSE.

TRUTH TABLE

INPUTS							OUTPUTS	
SELECT *			$\overline{DC}$	OUTPUT ENABLES			W	Y
S2	S1	S0		G1	$\overline{G2}$	G3		
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	L	L	L	H	$\overline{D0}$	D0
L	L	L	H	L	L	H	$\overline{D0n}$	D0n
L	L	H	L	L	L	H	$\overline{D1}$	D1
L	L	H	H	L	L	H	$\overline{D1n}$	D1n
L	H	L	L	L	L	H	$\overline{D2}$	D2
L	H	L	H	L	L	H	$\overline{D2n}$	D2n
L	H	H	L	L	L	H	$\overline{D3}$	D3
L	H	H	H	L	L	H	$\overline{D3n}$	D3n
H	L	L	L	L	L	H	$\overline{D4}$	D4
H	L	L	H	L	L	H	$\overline{D4n}$	D4n
H	L	H	L	L	L	H	$\overline{D5}$	D5
H	L	H	H	L	L	H	$\overline{D5n}$	D5n
H	H	L	L	L	L	H	$\overline{D6}$	D6
H	H	L	H	L	L	H	$\overline{D6n}$	D6n
H	H	H	L	L	L	H	$\overline{D7}$	D7
H	H	H	H	L	L	H	$\overline{D7n}$	D7n

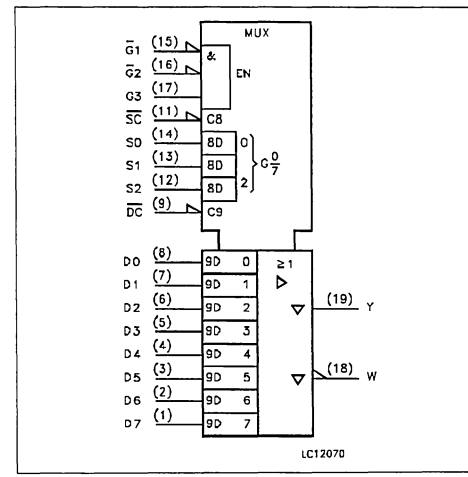
X: DON'T CARE Z: HIGH IMPEDANCE *. THISCOLUMN SHOWS THE INPUT ADDRESS SETUP WITH $\overline{SC}$ LOW

D0n ....D7n: THE LEVEL OF STEADY-STATE INPUTS AT INPUT DO THROUGH D7, RESPECTIVELY, BEFORE THE MOST RECENT LOW TO HIGH TRANSITION OF DATA CONTROL.

PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
8, 7, 6, 5, 4, 3, 2, 1	D0 to D7	Data Inputs
9	$\overline{DC}$	Data Enable Input (Active LOW)
11	$\overline{SC}$	Latch Enable Input (Active LOW)
14, 13, 12	SO, S1, S2	Select Inputs
15, 16	$\overline{G1}$, $\overline{G2}$	Output Enable Inputs (Active LOW)
17	G3	Output Enable Input (Active HIGH)
18	W	3 State Multiplexer Output (Active LOW)
19	Y	3 State Multiplexer Output (Active HIGH)
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

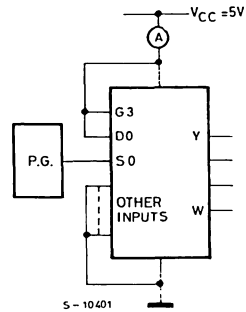
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5.0		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t_{PLH} t_{PHL}	Propagation Delay Time (Dn, $\overline{DC}$ - Y, W)	2.0	50			83	210		265		315	ns
		4.5				26	42		53		63	
		6.0				21	36		45		54	
		2.0	150			99	250		315		375	ns
		4.5				31	50		63		75	
		6.0				25	43		54		64	
t_{PLH} t_{PHL}	Propagation Delay Time (Sn - Y, W)	2.0	50			98	260		325		390	ns
		4.5				30	52		65		78	
		6.0				25	44		55		66	
		2.0	150			114	300		375		450	ns
		4.5				35	60		75		90	
		6.0				29	51		64		77	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{SC}$ - Y, W)	2.0	50			102	270		340		405	ns
		4.5				31	54		68		81	
		6.0				27	46		58		69	
		2.0	150			118	310		390		465	ns
		4.5				36	62		78		93	
		6.0				31	53		66		79	
t_{PZL} t_{PZH}	3 State Output Enable Time	2.0	50	R_L = 1 KΩ		44	125		155		190	ns
		4.5				14	25		31		38	
		6.0				12	21		26		32	
		2.0	150	R_L = 1 KΩ		60	165		205		250	ns
		4.5				19	33		41		50	
		6.0				16	28		35		43	
t_{PLZ} t_{PHZ}	3 State Output Disable Time	2.0	50	R_L = 1 KΩ		42	155		195		235	ns
		4.5				20	31		39		47	
		6.0				17	26		33		40	
$t_{W(L)}$	Minimum Pulse Width ($\overline{DC}$) ($\overline{SC}$)	2.0	50			18	75		95		110	ns
		4.5				6	15		19		22	
		6.0				6	13		16		19	
t_s	Minimum Set-up Time (Dn) (Sn)	2.0	50			10	50		65		75	ns
		4.5				3	10		13		15	
		6.0				3	9		11		13	
t_h	Minimum Hold Time (Dn) (Sn)	2.0	50				5		5		5	ns
		4.5					5		5		5	
		6.0					5		5		5	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance					77						pF

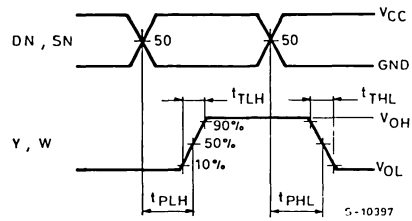
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

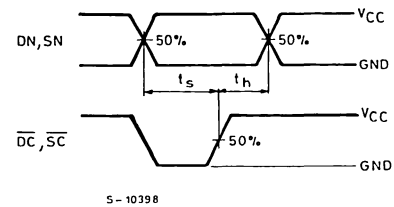
TEST CIRCUIT I_{CC} (Opr.)

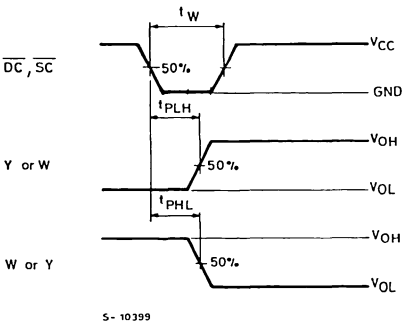


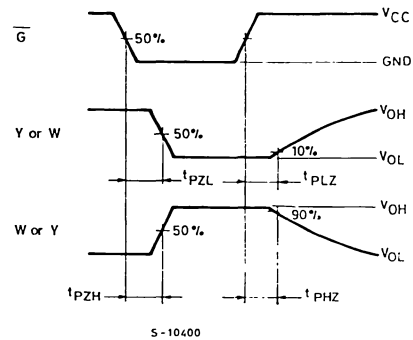
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SWITCHING CHARACTERISTICS TEST WAVEFORM







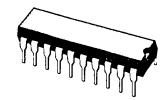


SGS-THOMSON MICROELECTRONICS

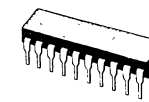
M54HC356
M74HC356

8 CHANNEL MULTIPLEXER/REGISTER WITH LATCHES (3-STATE)

- HIGH SPEED
  t_{PD} = 25 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS356



B1R
(Plastic Package)



F1R
(Ceramic Package)

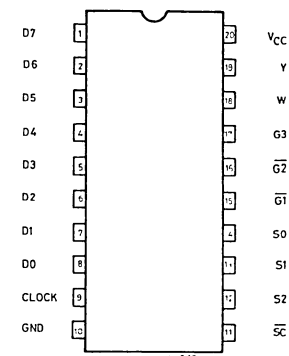
M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HC356F1R M74HC356M1R
M74HC356B1R M74HC356C1R

PIN CONNECTIONS (top view)



NC =
No Internal
Connection

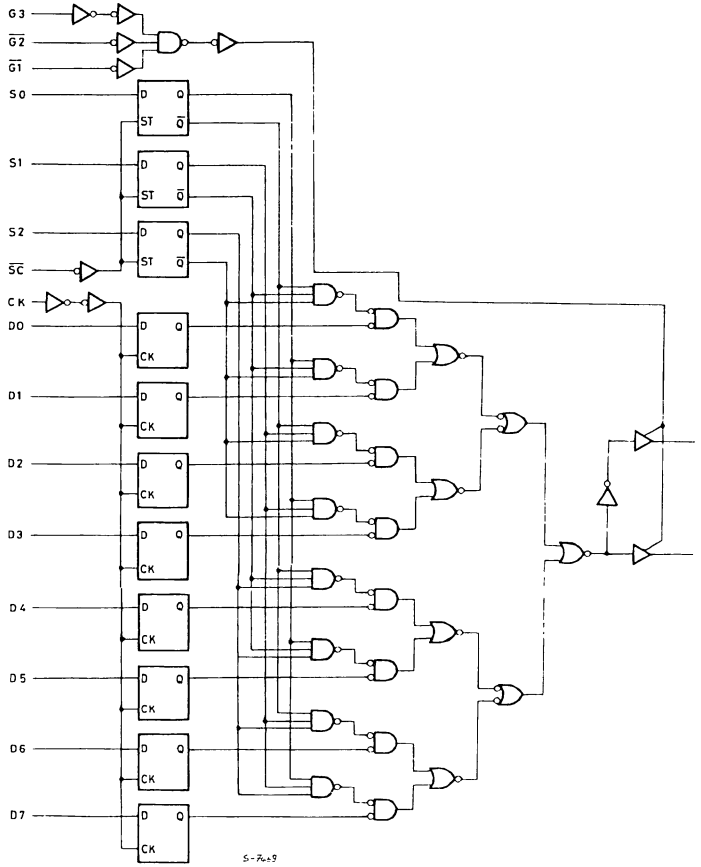
DESCRIPTION

The M54/74HC356 is a high speed CMOS 8-CHANNEL MULTIPLEXER/REGISTER (3-State) fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low consumption.

This device contains an 8 channel digital multiplexer with an 8-bit input data register and a 3-bit address input register with 3-state outputs. The one of eight input data will be provided on the Y output pin (non-inverted output) and W output pin (inverted output) is determineted by the address data.

The information at the data inputs (D0 to D7) is stored in the 8-bit flip-flop at the positive going edge of clock input (CLOCK). The information at the address inputs (S0 to S2) is stored in the 3-bit latch at the negative pulse on $\overline{SC}$ input. These outputs are disabled to be high-impedance when input $\overline{G1}$ is held high, input $\overline{G2}$ is held high or input G3 is held low. This device is suitable for interfacing with bus lines in a bus organized system. The M54/74HC356 is similar in function to the M54/74HC354, which has an 8-bit latch as the data register instead of an 8-bit flip-flop. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

LOGIC DIAGRAM



TRUTH TABLE OF INTERNAL LATCH

INPUTS		OUTPUTS	
D	ST	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Qn	$\overline{Qn}$

X: DON'T CARE

Qn. DATA STORED AT THE TRAILING EDGE OF THE MOST RECENT ST PULSE

TRUTH TABLE OF INTERNAL LATCH (FLIP FLOP)

D	CK	Q
L	⌐¯	L
H	⌐¯	H
X	¯⌐	Qn

X: DON'T CARE

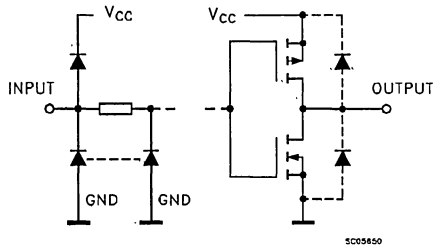
Qn· NO CHANGE

TRUTH TABLE

INPUTS								
SELECT *			CLOCK	OUTPUT ENABLES			W	Y
S2	S1	S0		$\overline{G1}$	$\overline{G2}$	G3		
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	⌐	L	L	H	$\overline{D0}$	D0
L	L	L	¬	L	L	H	$\overline{D0n}$	D0n
L	L	H	⌐	L	L	H	$\overline{D1}$	D1
L	L	H	¬	L	L	H	$\overline{D1n}$	D1n
L	H	L	⌐	L	L	H	$\overline{D2}$	D2
L	H	L	¬	L	L	H	$\overline{D2n}$	D2n
L	H	H	⌐	L	L	H	$\overline{D3}$	D3
L	H	H	¬	L	L	H	$\overline{D3n}$	D3n
H	L	L	⌐	L	L	H	$\overline{D4}$	D4
H	L	L	¬	L	L	H	$\overline{D4n}$	D4n
H	L	H	⌐	L	L	H	$\overline{D5}$	D5
H	L	H	¬	L	L	H	$\overline{D5n}$	D5n
H	H	L	⌐	L	L	H	$\overline{D6}$	D6
H	H	L	¬	L	L	H	$\overline{D6n}$	D6n
H	H	H	⌐	L	L	H	$\overline{D7}$	D7
H	H	H	¬	L	L	H	$\overline{D7n}$	D7n

X: DON'T CARE Z: HIGH IMPEDANCE *: This column shows the input adress setup with SC LOW.
D1 ..... D7: The level of steady state inputs at input D1 througth D7, respectively, at the time of the LOW to HIGH transition of the clock.

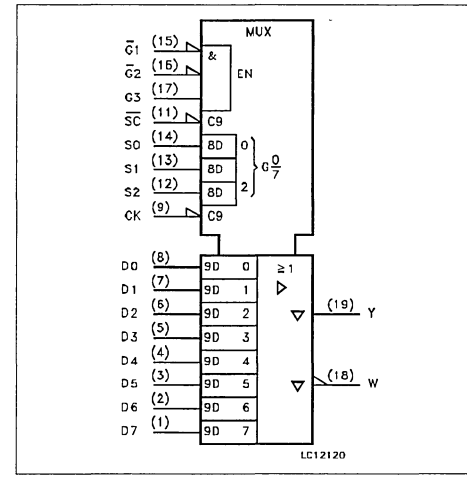
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
8, 7,, 6, 5, 4, 3, 2, 1	D0 to D7	Data Inputs
9	CLOCK	Clock Input (LOW to HIGH, Edge-triggered)
11	$\overline{SC}$	Latch Enable Input (Active LOW)
14, 13, 12	S0, S1, S2	Select Inputs
15, 16	$\overline{G1}$, $\overline{G2}$	Output Enable Inputs (Active LOW)
17	G3	Output Enable Inputs (Active HIGH)
18	W	3 State Multiplexer Output (Active LOW)
19	Y	3 State Multiplexer Output (Active HIGH)
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur Functional operation under these condition is not implied
(*) 500 mW. ≡ 65 °C derate to 300 mW by 10mW/°C· 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5.0		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

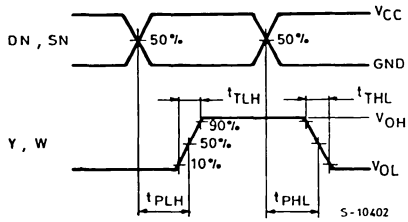
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Y, W)	2.0	50			99	240		300		360	ns
		4.5				28	48		60		72	
		6.0				22	41		51		61	
		2.0	150			117	280		350		420	ns
		4.5				33	56		70		84	
		6.0				26	48		60		71	

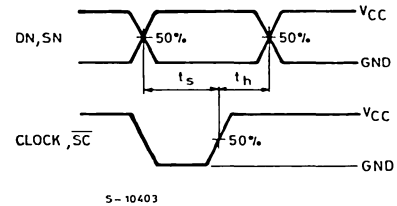
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

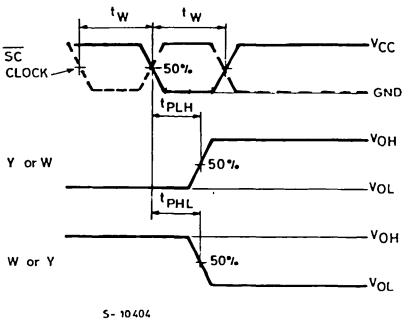
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time (Sn - Y, W)	2.0	50			111	260		325		390	ns
		4.5				32	52		65		78	
		6.0				24	44		55		66	
		2.0	150			128	300		375		450	ns
		4.5				37	60		75		90	
		6.0				28	51		64		77	
t_{PLH} t_{PHL}	Propagation Delay Time (SC - Y, W)	2.0	50			115	270		340		405	ns
		4.5				33	54		68		81	
		6.0				25	46		58		69	
		2.0	150			132	310		390		465	ns
		4.5				38	62		78		93	
		6.0				29	53		66		79	
t_{PZL} t_{PZH}	3 State Output Enable Time	2.0	50	R_L = 1 KΩ		48	125		155		190	ns
		4.5				14	25		31		38	
		6.0				11	21		26		32	
		2.0	150	R_L = 1 KΩ		65	165		205		250	ns
		4.5				19	33		41		50	
		6.0				15	28		35		43	
t_{PLZ} t_{PHZ}	3 State Output Disable Time	2.0	50	R_L = 1 KΩ		43	155		195		235	ns
		4.5				18	31		39		47	
		6.0				16	26		33		40	
f_{MAX}	Maximum Clock Frequency	2.0	50		6.2	20		5		4.2		ns
		4.5			31	80		25		21		
		6.0			37	82		30		25		
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CLOCK)	2.0	50			25	75		95		110	ns
		4.5				6	15		19		22	
		6.0				6	13		16		19	
$t_{W(L)}$	Minimum Pulse Width (SC)	2.0	50			13	75		95		110	ns
		4.5				6	15		19		22	
		6.0				6	13		16		19	
t_s	Minimum Set-up Time (Dn)	2.0	50			21	50		65		75	ns
		4.5				4	10		113		15	
		6.0				3	9		11		13	
t_s	Minimum Set-up Time (Sn)	2.0	50			9	50		65		75	ns
		4.5				2	10		13		15	
		6.0				2	9		11		13	
t_h	Minimum Hold Time (Dn) (Sn)	2.0	50				5		5		5	ns
		4.5					5		5		5	
		6.0					5		5		5	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance					59						pF

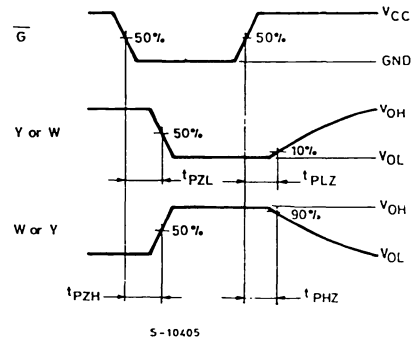
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

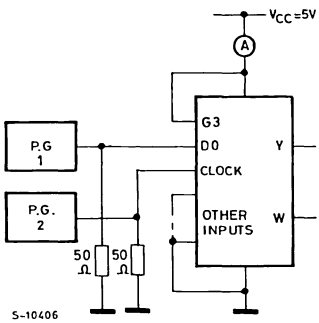


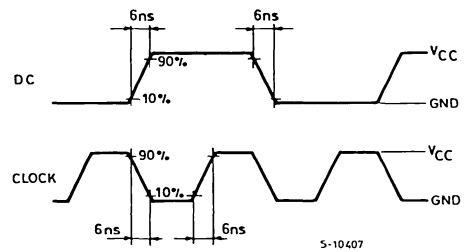






TEST CIRCUIT WAVEFORM Icc (Opr.)



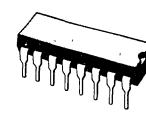


SGS-THOMSON MICROELECTRONICS

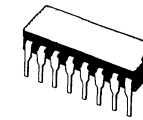
M54/M74HC365
M54/M74HC366

HEX BUS BUFFER (3-STATE)
HC365 NON INVERTING - HC366 INVERTING

- HIGH SPEED
  t_{PD} = 9 ns (TYP) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS365/366



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

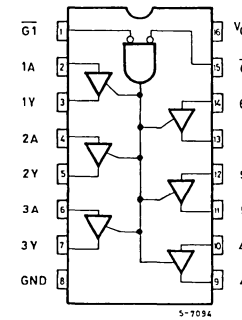
C1R
(Chip Carrier)

ORDER CODES :

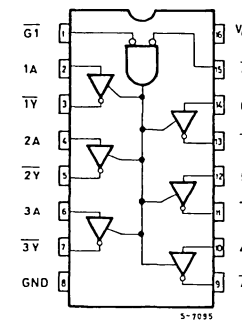
M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

PIN CONNECTIONS (top view)

HC365



HC366



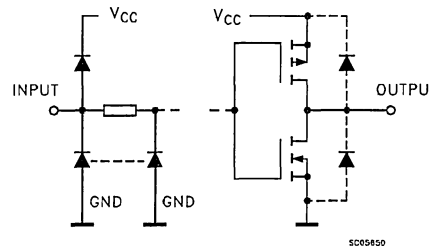
DESCRIPTION

The M54/74HC365 and the M54/74HC366 are high speed CMOS HEX BUS BUFFER fabricated in silicon gate C^2MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption.

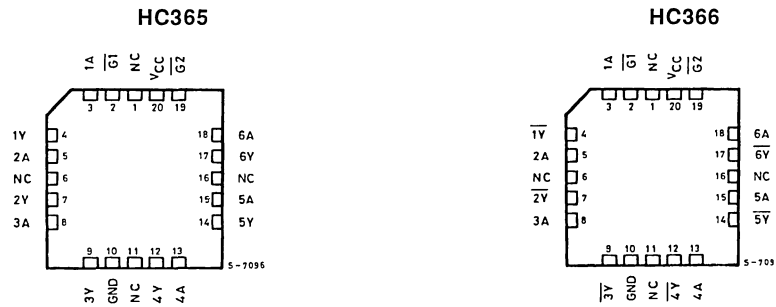
All six buffers are controlled by the combination of two enable inputs ($\overline{G1}$ and $\overline{G2}$) ; all outputs of these buffers are enabled only when both $\overline{G1}$ and $\overline{G2}$ inputs are held low, under all other conditions these output are disabled to be high-impedance.

These outputs are capable of driving up to 15 LSTTL loads. The designer has a choice of non-inverting outputs (HC365) and inverting outputs (HC366). All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



CHIP CARRIER



NC = No Internal Connection

TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{G1}$	$\overline{G2}$	An	Y (365)	$\overline{Y}$ (366)
L	L	L	L	H
L	L	H	H	L
H	X	X	Z	Z
X	H	X	Z	Z

X = DON'T CARE Z = HIGH IMPEDANCE

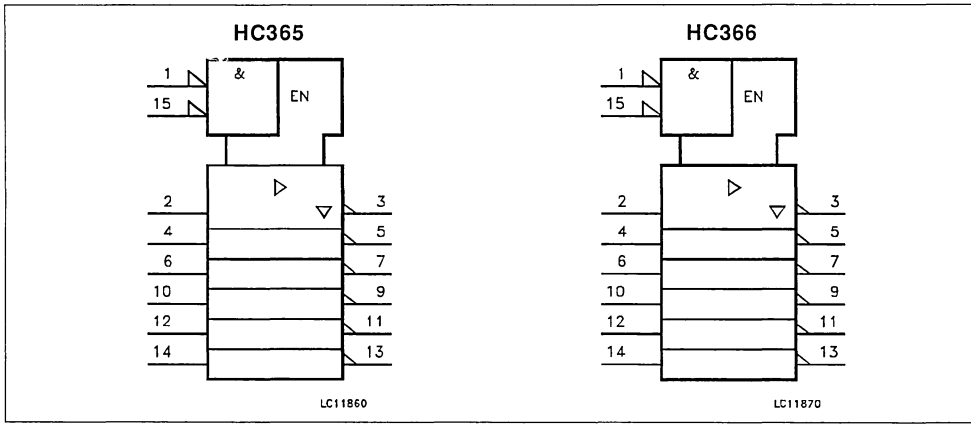
PIN DESCRIPTION (HC365)

PIN No	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{G1}$, $\overline{G2}$	Output Enable Inputs
2, 4, 6, 10, 12, 14	1A to 6A	Data Inputs
3, 5, 7, 9, 11, 13	1Y to 6Y	Data Outputs
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

PIN DESCRIPTION (HC366)

PIN No	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{G1}$, $\overline{G2}$	Output Enable Inputs
2, 4, 6, 10, 12, 14	1A to 6A	Data Inputs
3, 5, 7, 9, 11, 13	$\overline{1Y}$ to $\overline{6Y}$	Data Outputs
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

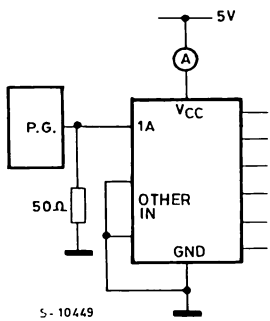
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0	50			38	90		115		135	ns
		4.5				12	18		23		27	
		6.0				10	15		20		23	
		2.0	150			51	130		165		195	ns
		4.5				17	26		33		39	
		6.0				14	22		28		33	
t_{PZL} t_{PZH}	Output Enable Time	2.0	50	R_L = 1 KΩ		64	130		165		195	ns
		4.5				16	26		33		39	
		6.0				14	22		28		33	
		2.0	150	R_L = 1 KΩ		76	150		190		225	ns
		4.5				19	30		38		45	
		6.0				16	26		32		38	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0	50	R_L = 1 KΩ		42	130		165		195	ns
		4.5				18	26		33		39	
		6.0				15	22		28		33	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance		for HC365 for HC366			27 25						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$ (per Gate)

TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

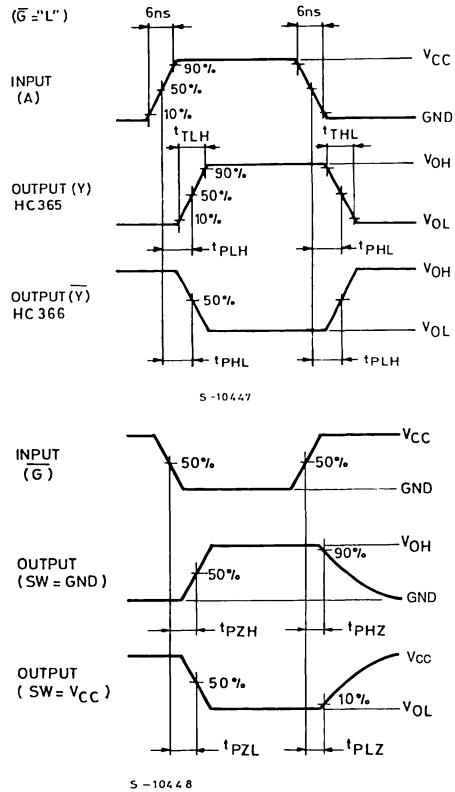
C_{PD} CALCULATION

C_{PD} is to be calculated with the following formula by using the measured value of ICC (opr.) in the test circuit opposite.

$$C_{PD} = \frac{I_{CC}(opr)}{f_{IN} \times V_{CC}}$$

In determining the typical value of CPD a relatvely high frequency of 1 MHz was applied to fIN, in order to eliminate any error caused by the quiescent supply current.

SWITCHING CHARACTERISTICS TEST WAVEFORM



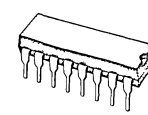
Note : Such a logic level shall be applied to each input that the output voltage stays in the apposite side to the switch connection level, when the output is enable.

SGS-THOMSON MICROELECTRONICS

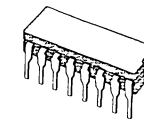
M54/M74HC367
M54/M74HC368

HEX BUS BUFFER (3-STATE)
HC367 NON INVERTING, HC368 INVERTING

- HIGH SPEED
  t_{PD} = 11 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS367/368



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

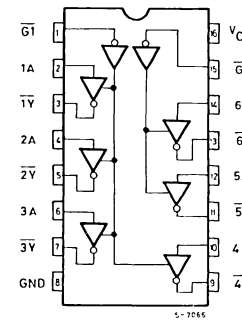
C1R
(Chip Carrier)

ORDER CODES :

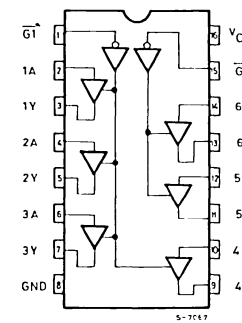
M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

PIN CONNECTIONS (top view)

HC368



HC367



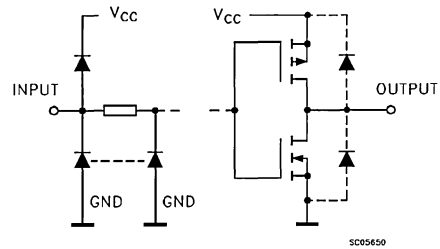
DESCRIPTION

The M54/74HC367 and the M54/74HC368 are high speed CMOS HEX BUS BUFFER (3-STATE) fabricated in silicon gate C^2MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. These devices contain six buffers, four buffers are controlled by an enable input ($\overline{G1}$) and the other two buffers are controlled by the other enable input ($\overline{G2}$) ; the outputs of each buffer group are enabled when $\overline{G1}$ and/or $\overline{G2}$ inputs are held low, and when held high these outputs are disabled to be high-impedance.

These outputs are capable of driving up to 15 LSTTL loads. The designer has a choice of non-inverting outputs (HC367) and inverting outputs (HC368).

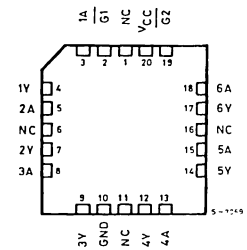
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT

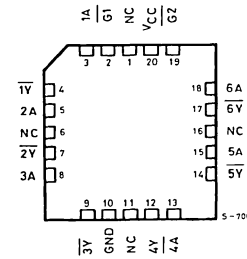


CHIP CARRIER

HC367



HC368



NC = No Internal Connection

TRUTH TABLE

INPUTS		OUTPUTS	
$\overline{G}$	An	Y n (367)	$\overline{Yn}$ (368)
L	L	L	H
L	H	H	L
H	X	Z	Z

X = DON'T CARE Z = HIGH IMPEDANCE

PIN DESCRIPTION (HC367)

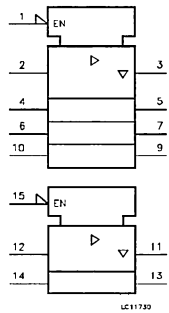
PIN No	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{G1}$, $\overline{G2}$	Output Enable Inputs
2, 4, 6, 10, 12, 14	1A to 6A	Data Inputs
3, 5, 7, 9, 11, 13	1Y to 6Y	Data Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

PIN DESCRIPTION (HC368)

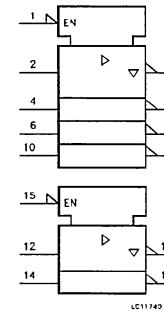
PIN No	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{G1}$, $\overline{G2}$	Output Enable Inputs
2, 4, 6, 10, 12, 14	1A to 6A	Data Inputs
3, 5, 7, 9, 11, 13	$\overline{1Y}$ to $\overline{6Y}$	Data Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL

HC367



HC368



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW ≡ 65 °C derate to 300 mW by 10mW/°C 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

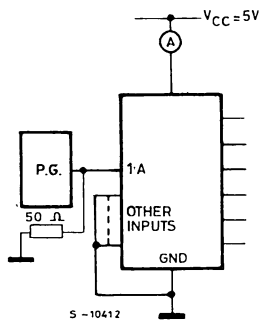
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6 0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0	50			30	85		105		130	ns
		4.5				10	17		21		26	
		6.0				9	14		18		22	
		2.0	150			42	105		130		160	ns
		4.5				14	21		26		32	
		6.0				12	18		22		27	
t_{PZL} t_{PZH}	Output Enable Time	2.0	50	R_L = 1 KΩ		36	90		115		135	ns
		4.5				11	18		23		27	
		6.0				9	15		20		23	
		2.0	150	R_L = 1 KΩ		49	110		140		165	ns
		4.5				15	22		28		33	
		6.0				13	19		24		28	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0	50	R_L = 1 KΩ		32	95		120		145	ns
		4.5				14	19		24		29	
		6.0				12	16		20		25	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance					33						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit) Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$ (per Channel)

TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

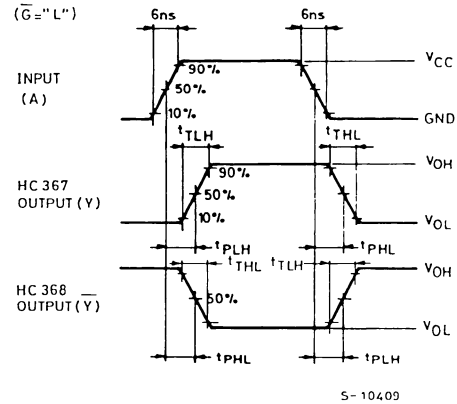
C_{PD} CALCULATION

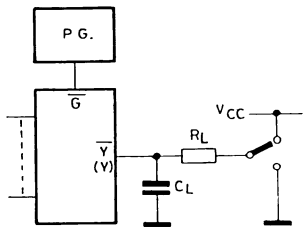
C_{PD} is to be calculated with the following formula by using the measured value of I_{CC} (opr.) in the test circuit opposite.

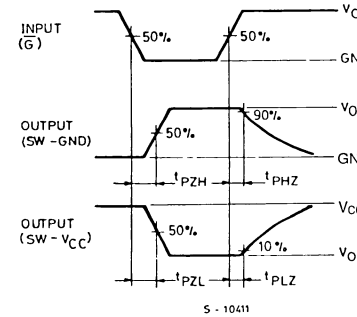
$$C_{PD} = \frac{I_{CC}(opr)}{f_{IN} \times V_{CC}}$$

In determining the typical value of C_{PD}, a relatively high frequency of 1 MHz was applied to f_{IN}, in order to eliminate any error caused by the quiescent supply current.

SWITCHING CHARACTERISTICS TEST WAVEFORM







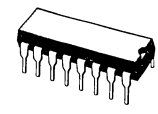
Note Such a logic level shall be applied to each input that the output voltage stays in the apposite side to the switch connection level, when the output is enable

SGS-THOMSON MICROELECTRONICS

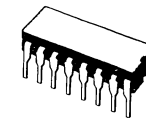
M54/M74HCT367
M54/M74HCT368

HEX BUS BUFFER (3-STATE)
HCT367 NON INVERTING, HCT368 INVERTING

- HIGH SPEED
  t_{PD} = 11 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS367/368



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HCTXXXF1R M74HCTXXXM1R
M74HCTXXXB1R M74HCTXXXC1R

DESCRIPTION

The M54/74HCT367 and the M54/74HCT368 are high speed CMOS HEX BUS BUFFER (3-STATE) fabricated in silicon gate C^2MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. These devices contain six buffers, four buffers are controlled by an enable input ($\overline{G1}$) and the other two buffers are controlled by the other enable input ($\overline{G2}$) ; the outputs of each buffer group are enabled when $\overline{G1}$ and/or $\overline{G2}$ inputs are held low, and when held high these outputs are disabled to be high-impedance.

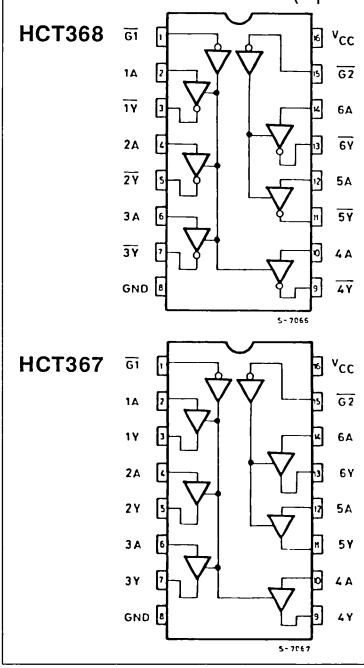
These outputs are capable of driving up to 15 LSTTL loads. The designer has a choice of non-inverting outputs (HCT367) and inverting outputs (HCT368).

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

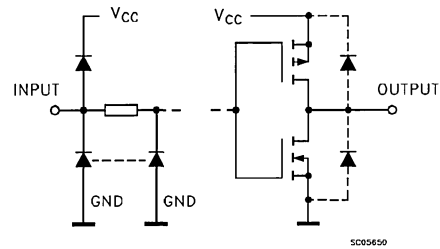
This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

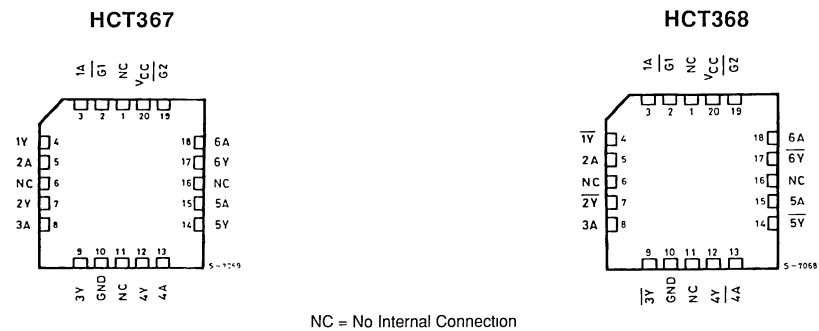
PIN CONNECTIONS (top view)



INPUT AND OUTPUT EQUIVALENT CIRCUIT



CHIP CARRIER



NC = No Internal Connection

TRUTH TABLE

INPUTS		OUTPUTS	
$\overline{G}$	An	Y n (367)	$\overline{Yn}$ (368)
L	L	L	H
L	H	H	L
H	X	Z	Z

X = DON'T CARE Z = HIGH IMPEDANCE

PIN DESCRIPTION (HCT367)

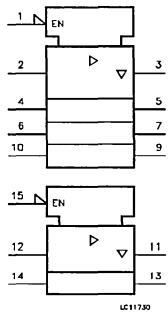
PIN No	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{G1}$, $\overline{G2}$	Output Enable Inputs
2, 4, 6, 10, 12, 14	1A to 6A	Data Inputs
3, 5, 7, 9, 11, 13	1Y to 6Y	Data Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

PIN DESCRIPTION (HCT368)

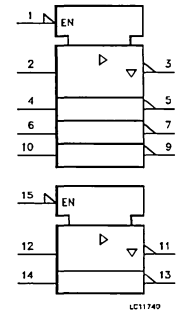
PIN No	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{G1}$, $\overline{G2}$	Output Enable Inputs
2, 4, 6, 10, 12, 14	1A to 6A	Data Inputs
3, 5, 7, 9, 11, 13	$\overline{1Y}$ to $\overline{6Y}$	Data Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL

HCT367



HCT368



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

RECOMMENDED OPERATING CONDITIONS

DC SPECIFICATIONS

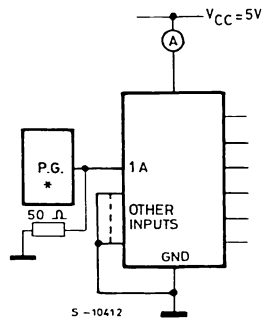
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-6.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 6.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				4		40		80	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9		3.0	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			7	12		15		18	ns
t_{PLH} t_{PHL}	Propagation Delay Time (for HCT367 only)	2.0	50			14	22		28		33	ns
		2.0	150			18	28		35		42	
t_{PLH} t_{PHL}	Propagation Delay Time (for HCT368 only)	2.0	50			15	24		30		36	ns
		2.0	150			19	30		38		45	
t_{PZL} t_{PZH}	Output Enable Time	2.0	50			16	25		31		38	ns
		2.0	150			20	31		39		47	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0	50			18	25		31		38	ns
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance		fot HCT367 for HCT368			47 55						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit) Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$ (per Channel)

TEST CIRCUIT I_{CC} (Opr.)



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

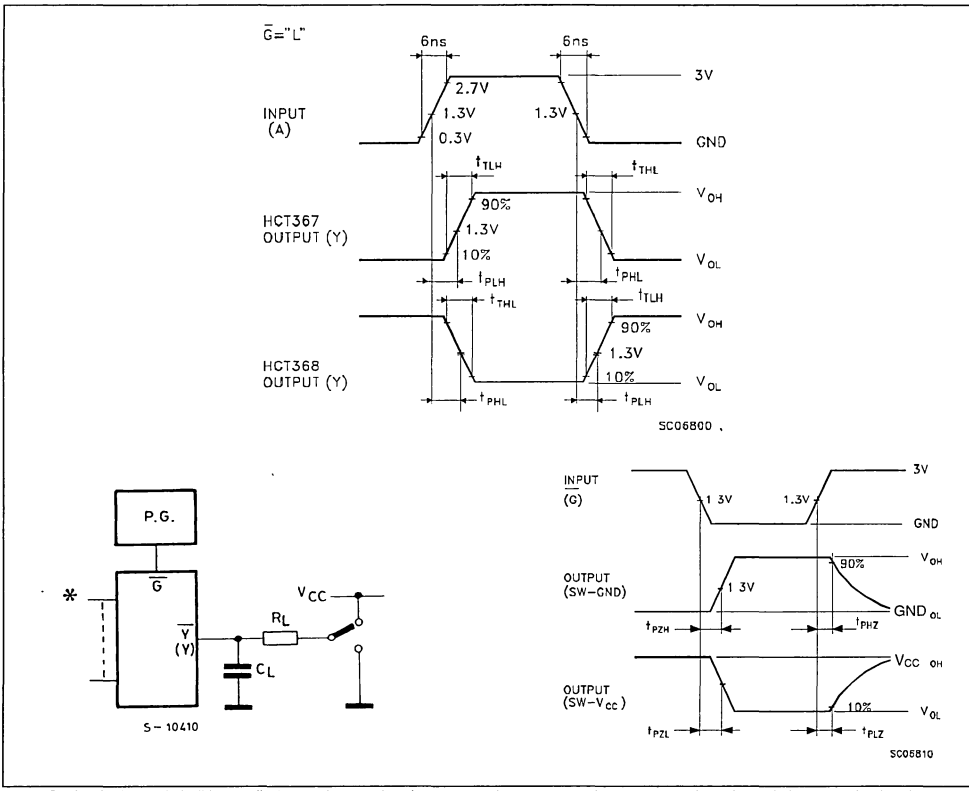
C_{PD} CALCULATION

C_{PD} is to be calculated with the following formula by using the measured value of I_{CC} (opr.) in the test circuit opposite.

$$C_{PD} = \frac{I_{CC}(opr)}{f_{IN} \times V_{CC}}$$

In determining the typical value of C_{PD}, a relatively high frequency of 1 MHz was applied to f_{IN}, in order to eliminate any error caused by the quiescent supply current.

SWITCHING CHARACTERISTICS TEST WAVEFORM



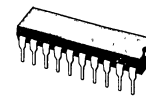
Note . Such a logic level shall be applied to each input that the output voltage stays in the apposite side to the switch connection level, when the output is enabled.

SGS-THOMSON MICROELECTRONICS

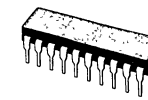
M54/74HC373
M54/74HC533

OCTAL D-TYPE LATCH WITH 3 STATE OUTPUT
HC373 NON INVERTING - HC533 INVERTING

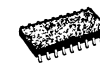
- HIGH SPEED
  t_{PD} = 11 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $I_{OL} = |I_{OH}|$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS373/533



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HCXXXF1R	M74HCXXXM1R
M74HCXXXB1R	M74HCXXXC1R

DESCRIPTION

The M54/74HC373/533 are high speed CMOS OCTAL LATCH WITH 3-STATE OUTPUTS fabricated with in silicon gate C^2MOS technology.

These ICs achive the high speed operation similar to equivalent LSTTL while maintaning the CMOS low power dissipation.

These 8 bit D-Type latches are controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$).

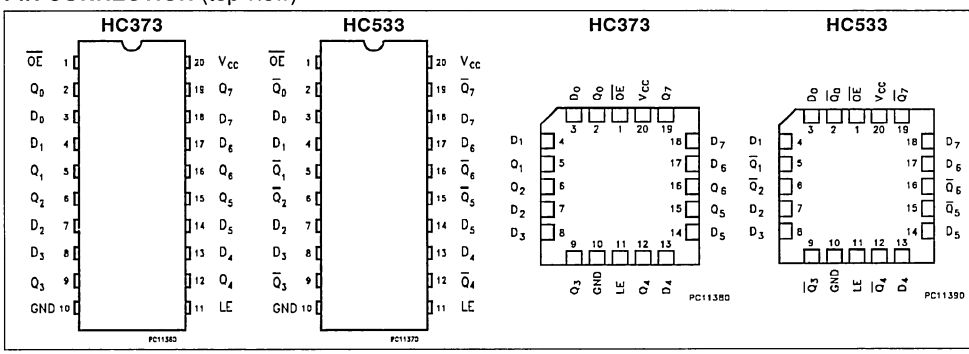
While the LE input is held at a high level, the Q outputs will follow the data input precisely or inversely. When the LE is taken low, the Q outputs will be latched precisely or inversely at the logic level of D input data. While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level) and while high level the outpts will be in a high impedance state.

The application designer has a choise of combination of inverting and non inverting outputs.

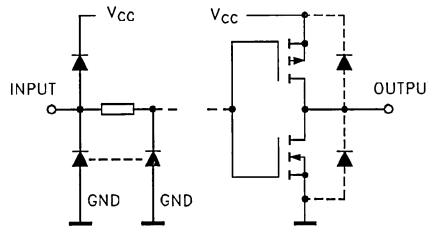
The three state output configuration and the wide choise of outline make bus organized system simple.

All inputs are equipped with protection circuits against discharge and transient excess voltage.

PIN CONNECTION (top view)



INPUT AND OUTPUT EQUIVALENT CIRCUIT



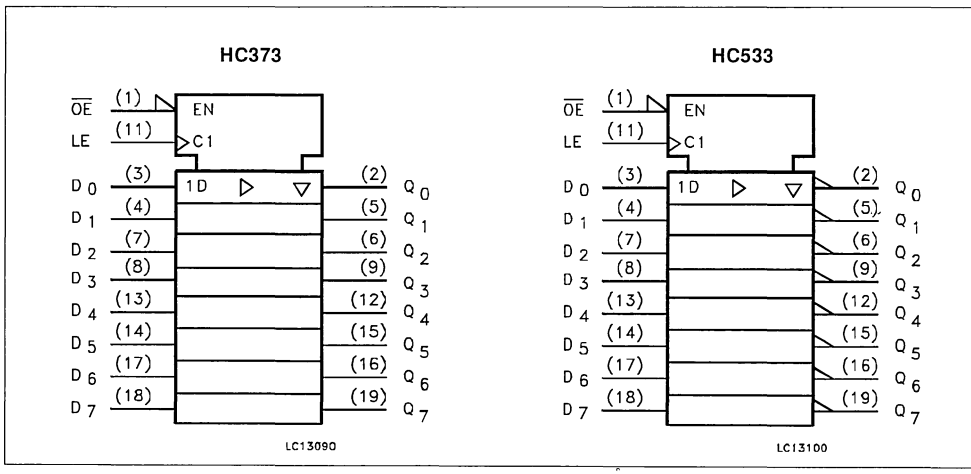
PIN DESCRIPTION (HC373)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State output Enable Input (Active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0 to Q7	3 State outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data Inputs
11	LE	Latch Enable Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

PIN DESCRIPTION (HC533)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State output Enable Input (Active LOW)
2, 5, 6, 9, 12, 15, 16, 19	$\overline{Q0}$ to $\overline{Q7}$	3 State outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data Inputs
11	LE	Latch Enable Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS



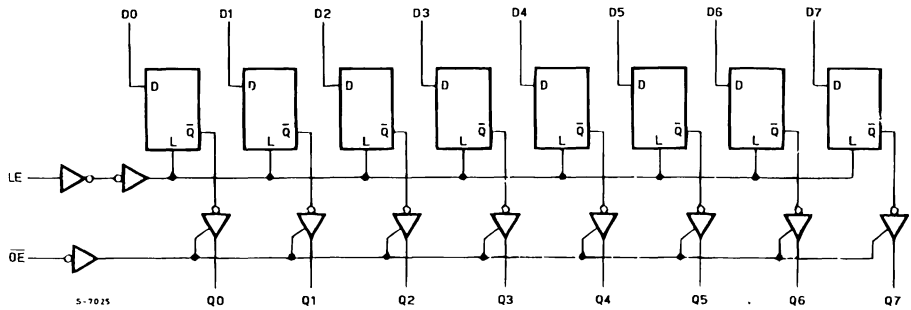
TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q (HC373)	$\overline{Q}$ (HC533)
H	X	X	Z	Z
L	L	X	NO CHANGE *	NO CHANGE *
L	H	L	L	H
L	H	H	H	L

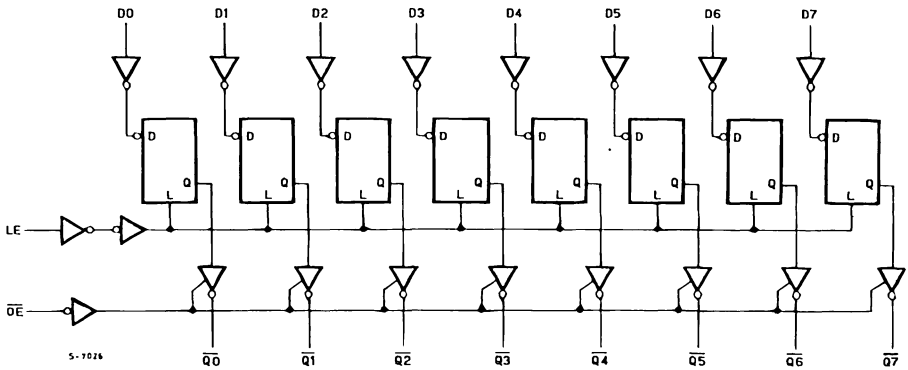
X: DON'T CARE
Z: HIGH IMPEDANCE
*: Q/$\overline{Q}$ OUTPUTS ARE LATCHED AT THE TIME WHEN THE LE INPUT IS TAKEN LOW LOGIC LEVEL.

LOGIC DIAGRAMS

HC373



HC533



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5.0		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

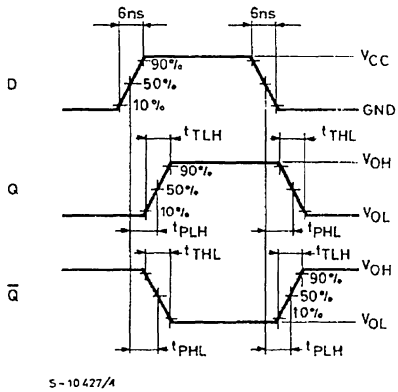
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t_{PLH} t_{PHL}	Propagation Delay Time (LE, D - Q, $\overline{Q}$)	2.0	50			42	125		155		190	ns
		4.5				14	25		31		38	
		6.0				12	21		26		32	
		2.0	150			57	175		220		265	ns
		4.5				19	35		44		53	
		6.0				16	30		37		45	
t_{PZL} t_{PZH}	3 State Output Enable Time	2.0	50	R_L = 1 KΩ		39	125		155		190	ns
		4.5				13	25		31		38	
		6.0				11	21		26		32	
		2.0	150	R_L = 1 KΩ		54	175		220		265	ns
		4.5				18	35		44		53	
		6.0				15	30		37		45	
t_{PLZ} t_{PHZ}	3 State Output Disable Time	2.0	50	R_L = 1 KΩ		30	125		155		190	ns
		4.5				14	25		31		38	
		6.0				13	21		26		32	
$t_{W(H)}$	Minimum Pulse Width (LE)	2.0	50			15	75		95		110	ns
		4.5				6	15		19		22	
		6.0				6	13		16		19	
t_s	Minimum Set-up Time	2.0	50			16	50		65		75	ns
		4.5				4	10		13		15	
		6.0				3	9		11		13	
t_h	Minimum Hold Time	2.0	50				5		5		5	ns
		4.5					5		5		5	
		6.0					5		5		5	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{OUT}	Out put Capacitance					10						pF
C_{PD} (*)	Power Dissipation Capacitance					38						pF

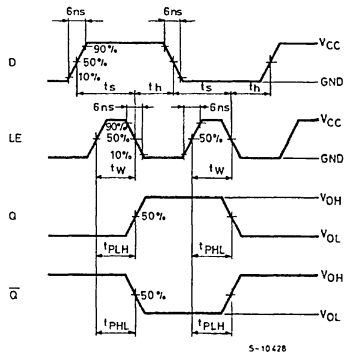
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Flip Flop) and the CPD when n pcs of Flip Flop operate, can be gained by following equation: CPD (TOTAL) = 22 + 16 x n [pF]

SWITCHING CHARACTERISTICS TEST WAVEFORM

t_{PLH}, t_{PHL}, (D - Q, $\overline{Q}$)



t_{PLH}, t_{PHL} (LE - Q, $\overline{Q}$), t_s, t_h, t_W

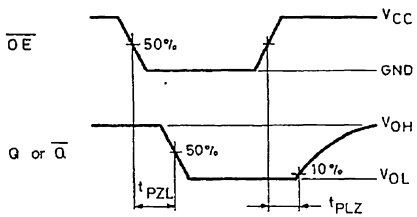


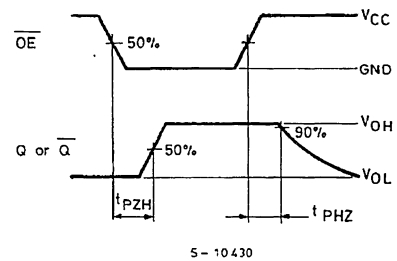
t_{PLZ}, t_{PZL}

The 1KΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputsand GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{OE}$ input is held low.

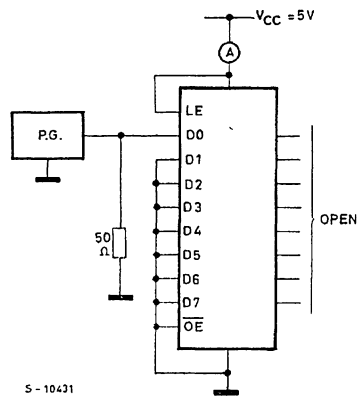
t_{PHZ}, t_{PZH}

The 1KΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{OE}$ input is held low.





TEST CIRCUIT I_{CC} (Opr.)

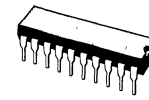


INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

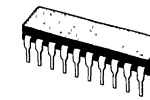
M54/74HCT373
M54/74HCT533

OCTAL D-TYPE LATCH WITH 3 STATE OUTPUT
HCT373 NON INVERTING - HCT533 INVERTING

- HIGH SPEED
  t_{PD} = 17 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8 V (MAX.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $I_{OL} = |I_{OH}| = 6$ mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS373/533



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

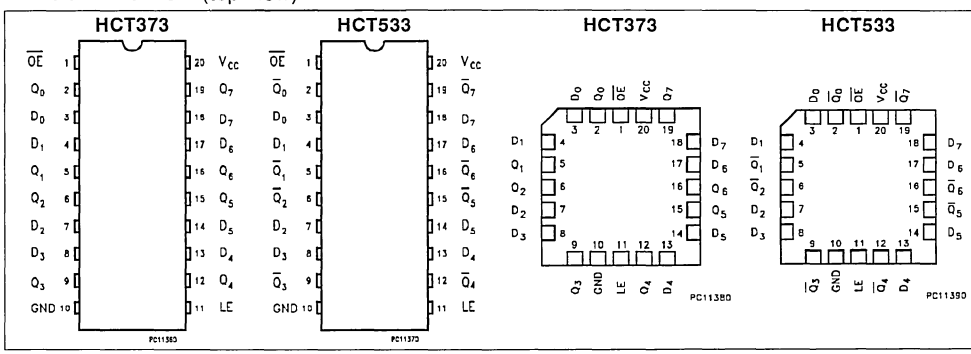
ORDER CODES :

M54HCTXXXF1R M74HCTXXXM1R
M74HCTXXXB1R M74HCTXXXC1R

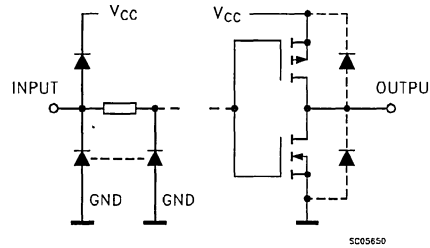
DESCRIPTION

The M54/74HCT373 and M54HCT533 are high speed CMOS OCTAL LATCH WITH 3-STATE OUTPUTS fabricated with in silicon gate C^2MOS technology.
These ICs achive the high speed operation similar to equivalent LSTTL while maintaning the CMOS low power dissipation.
These 8 bit D-Type latches are controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$).
While the LE input is held at a high level, the Q outputs will follow the data input precisely or inversely. When the LE is taken low, the Q outputs will be latched precisely or inversely at the logic level of D input data. While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level) and while high level the outpts will be in a high impedance state. The application designer has a choise of combination of inverting and non inverting outputs. The three state output configuration and the wide choise of outline make bus organized system simple.
These integrated circuits have input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption. All inputs are equipped with protection circuits against discharge and transient excess voltage.

PIN CONNECTION (top view)



INPUT AND OUTPUT EQUIVALENT CIRCUIT



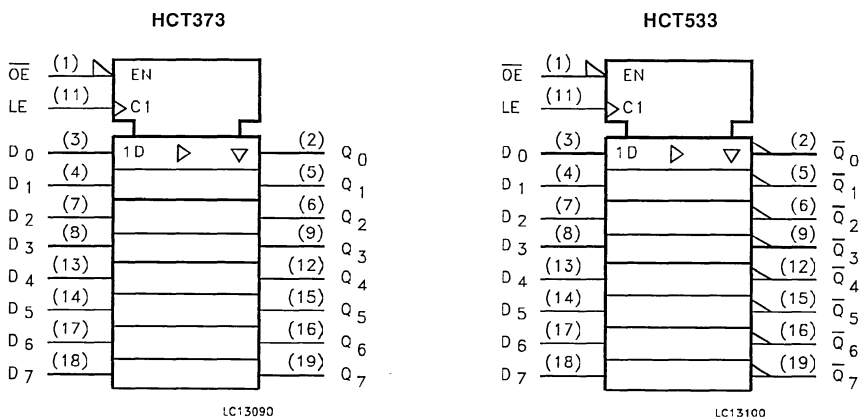
PIN DESCRIPTION (HCT373)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State output Enable Input (Active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0 to Q7	3 State outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data Inputs
11	LE	Latch Enable Input
10	GND	Ground (0V)
20	Vcc	Positive Supply Voltage

PIN DESCRIPTION (HCT533)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State output Enable Input (Active LOW)
2, 5, 6, 9, 12, 15, 16, 19	$\overline{Q0}$ to $\overline{Q7}$	3 State outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data Inputs
11	LE	Latch Enable Input
10	GND	Ground (0V)
20	Vcc	Positive Supply Voltage

IEC LOGIC SYMBOLS



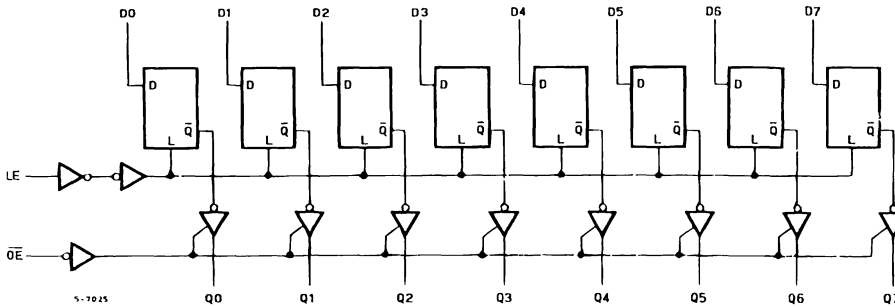
TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q (HCT373)	$\overline{Q}$ (HCT533)
H	X	X	Z	Z
L	L	X	NO CHANGE *	NO CHANGE *
L	H	L	L	H
L	H	H	H	L

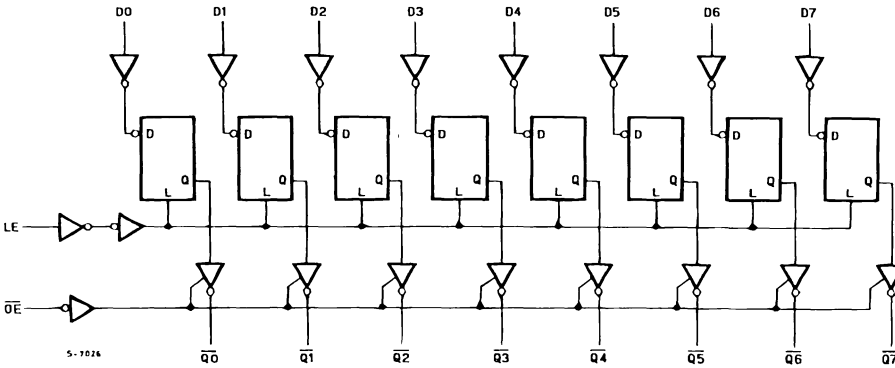
X: DON'T CARE
Z: HIGH IMPEDANCE
*: Q/$\overline{Q}$ OUTPUTS ARE LATCHED AT THE TIME WHEN THE LE INPUT IS TAKEN LOW LOGIC LEVEL.

LOGIC DIAGRAMS

HCT373



HCT533



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied

(*) 500 mW. ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-6.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 6.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5.0		±10	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				4		40		80	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND				2.0		2.9		3.0	mA

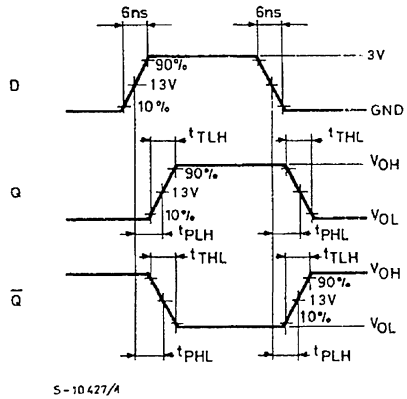
AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5	50			7	12		15		18	ns
t_{PLH} t_{PHL}	Propagation Delay Time (LE - Q)	4.5	50			20	30		38		45	ns
		4.5	150			24	37		46		56	ns
t_{PLH} t_{PHL}	Propagation Delay Time (D - Q)	4.5	50			19	30		38		45	ns
		4.5	150			23	36		45		54	ns
t_{PZL} t_{PZH}	3 State Output Enable Time ($\overline{OE}$ - Q)	4.5	50	R_L = 1 KΩ		20	30		38		45	ns
		4.5	150	R_L = 1 KΩ		24	37		46		56	ns
t_{PLZ} t_{PHZ}	3 State Output Disable Time ($\overline{OE}$ - Q)	4.5	50	R_L = 1 KΩ		20	30		38		45	ns
$t_{W(H)}$	Minimum Pulse Width (LE)	4.5	50			8	15		19		22	ns
t_s	Minimum Set-up Time	4.5	50			4	10		13		15	ns
t_h	Minimum Hold Time	4.5	50				5		5		8	ns
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance		HCT373 HCT533			66 52						pF

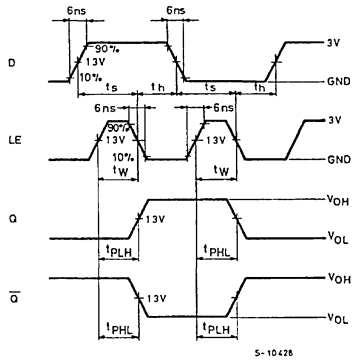
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Flip Flop) and the CPD when N pcs of Flip Flop operate, can be gained by following equation:
CPD (TOTAL) = 32 + 34 x n [pF] (for HCT373); 30 + 22 x n [pF] (for HCT533)

SWITCHING CHARACTERISTICS TEST WAVEFORM

t_{PLH}, t_{PHL}, t_s, t_h, t_w



f_{MAX}

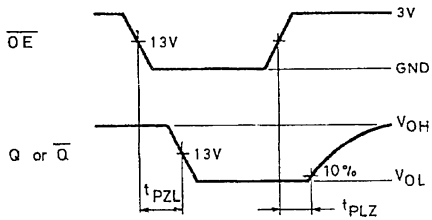


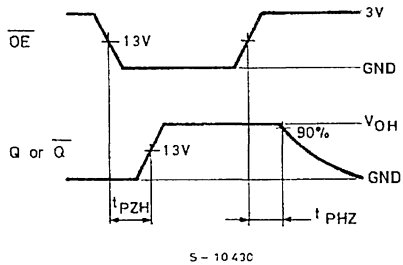
t_{PLZ}, t_{PZL}

The 1KΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputsand GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{OE}$ input is held low.

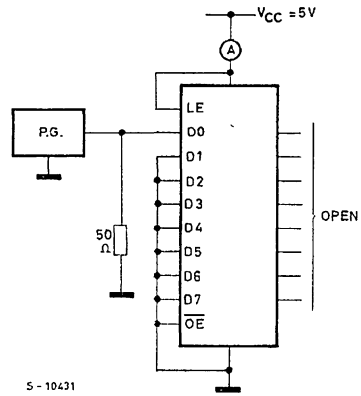
t_{PHZ}, t_{PZH}

The 1KΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{OE}$ input is held low.



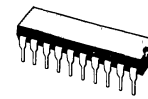


TEST CIRCUIT I_{CC} (Opr.)

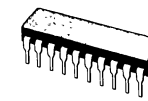


OCTAL D-TYPE FLIP FLOP WITH 3 STATE OUTPUT
HC374 NON INVERTING - HC534 INVERTING

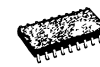
- HIGH SPEED
  f_{MAX} = 77 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $I_{OL} = |I_{OH}|$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS374/534



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

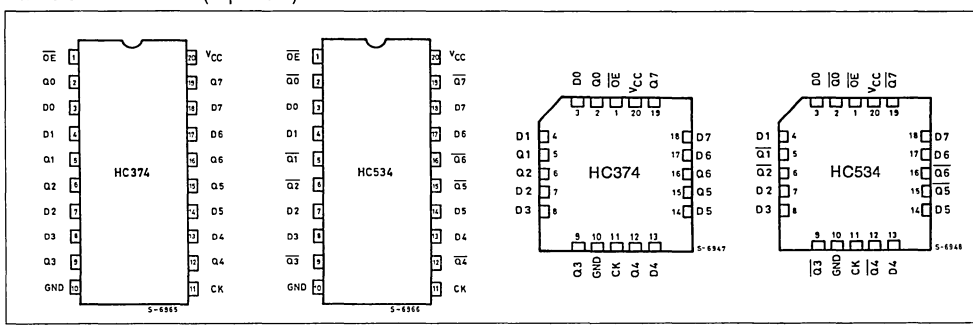
M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

DESCRIPTION

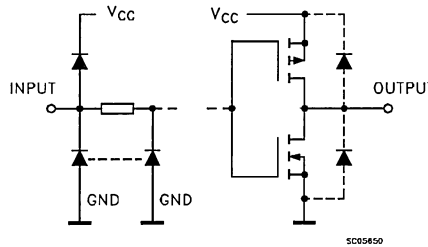
The M54/74HC374, M54/74HC534, are high speed CMOS OCTAL D-TYPE FLIP FLOP WITH 3-STATE OUTPUTS fabricated with in silicon gate C^2MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power comsuption. These8-bit D-type flip-flops are controlled by a clock input (CK) and an ouput enable input ($\overline{OE}$). On the positive transition of the clock, the Q outputs will be set to the logic state that were setup at the D inputs (HC374) or their complements (HC534).

While the $\overline{OE}$ input is low, the eight outputs will be in a normal logic state (high or low logic level), and while high level, the outputs will be in a high impedance state. The output control does not affect the internal operation of flip-flops. That is, the old data can be retained or the new data can be entered even while the outputs are off. The application engineer has a choice of combination of inverting and non-inverting outputs. The HC374 and HC574 are identical, apart from pin layout. The 3-state output configuration and the wide choice of outline make bus-organized systems simple. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION (top view)



INPUT AND OUTPUT EQUIVALENT CIRCUIT



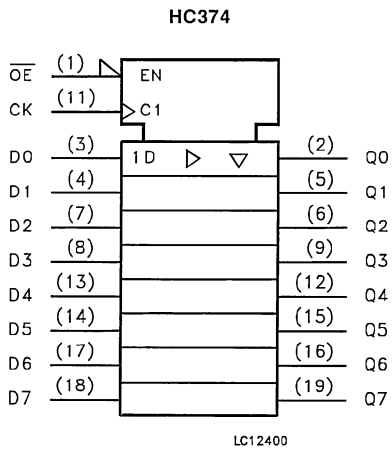
PIN DESCRIPTION (HC374)

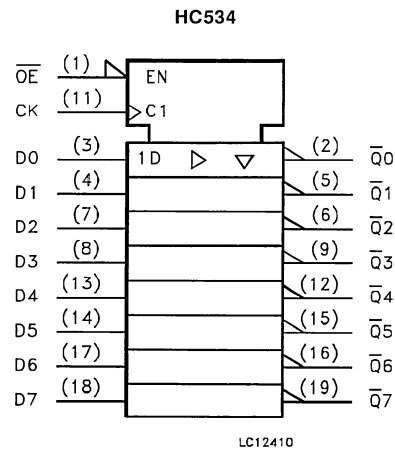
PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State output Enable Input (Active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0 to Q7	3 State outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data Inputs
11	CLOCK	Clock Input (LOW to HIGH, edge triggered)
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

PIN DESCRIPTION (HC534)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State output Enable Input (Active LOW)
2, 5, 6, 9, 12, 15, 16, 19	$\overline{Q0}$ to $\overline{Q7}$	3 State outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data Inputs
11	CLOCK	Clock Input (LOW to HIGH, edge triggered)
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS

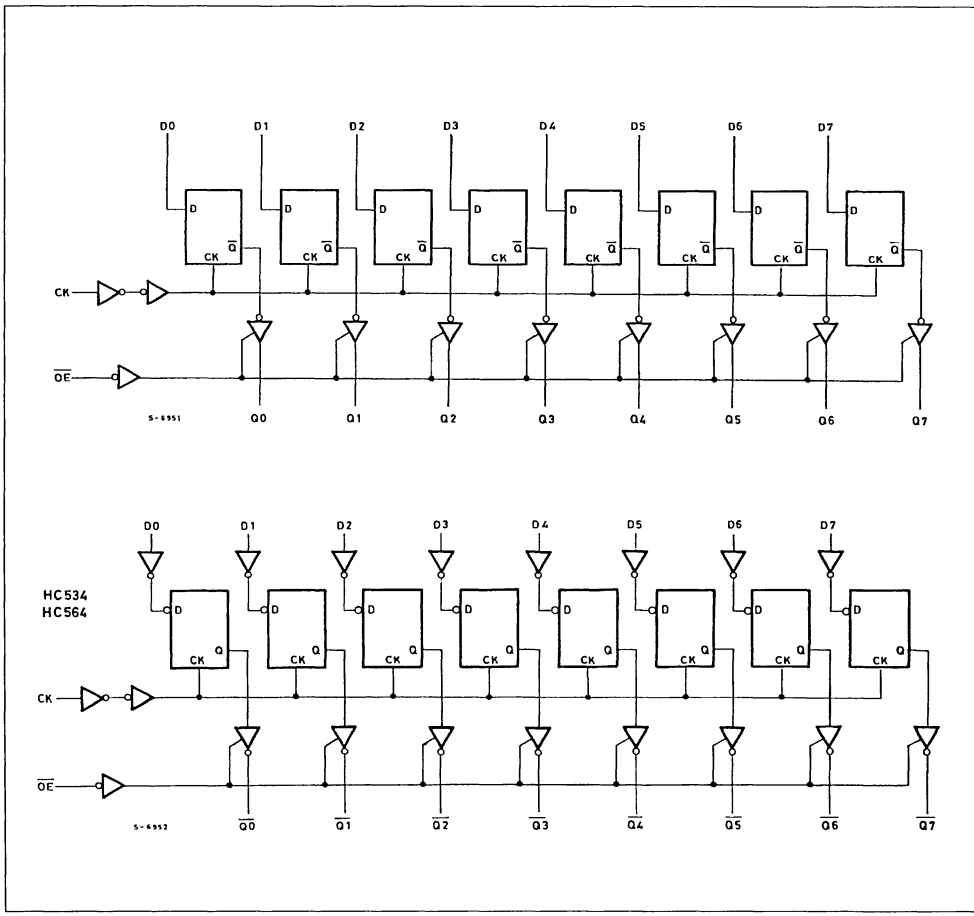




TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q (HC374)	$\overline{Q}$ (HC534)
H	X	X	Z	Z
L	⌐⌙	X	NO CHANGE	NO CHANGE
L	⌙⌐	L	L	H
L	⌙⌐	H	H	L

LOGIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series		-55 to +125	°C
	M74HC Series		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5.0		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

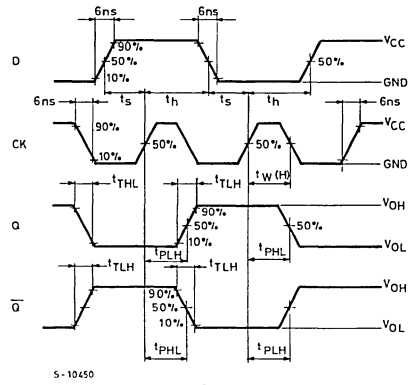
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q, $\overline{Q}$)	2.0	50			45	140		175		210	ns
		4.5				15	28		35		42	
		6.0				13	24		30		36	
		2.0	150			60	190		240		285	ns
		4.5				20	38		48		57	
		6.0				17	32		41		48	
t_{PLZ} t_{PHZ}	3 State Output Enable Time	2.0	50	R_L = 1 KΩ		39	135		170		205	ns
		4.5				13	27		34		41	
		6.0				11	23		29		35	
		2.0	150	R_L = 1 KΩ		54	185		230		280	ns
		4.5				18	37		46		56	
		6.0				15	31		39		48	
f_{MAX}	Maximum CLock Frequency	2.0	50		6.2	18		5		4.2		ns
		4.5			31	75		25		21		
		6.0			37	90		30		25		
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CLOCK)	2.0	50			15	75		95		110	ns
		4.5				6	15		19		22	
		6.0				6	13		16		19	
t_s	Minimum Set-up Time	2.0	50			25	75		95		110	ns
		4.5				6	15		19		22	
		6.0				4	13		16		19	
t_h	Minimum Hold Time	2.0	50				0		0		0	ns
		4.5					0		0		0	
		6.0					0		0		0	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{OUT}	Out put Capacitance					10						pF
C_{PD} (*)	Power Dissipation Capacitance					47						pF

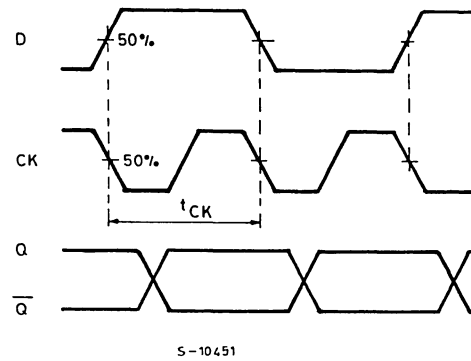
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per FLIP-FLOP) and C_{PD} when N pcs of FLIP-FLOP operate, can be gained by following equation: C_{PD} (TOTAL) = 30 + 17 x N (pF)

SWITCHING CHARACTERISTICS TEST WAVEFORM

t_{PLH}, t_{PHL}, t_s, t_h, t_w



f_{MAX}

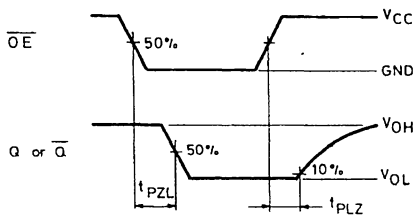


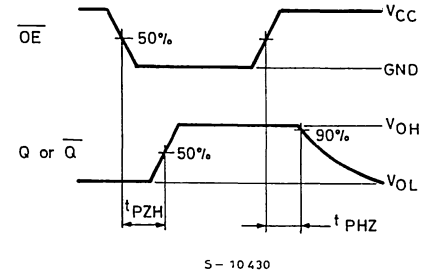
t_{PLZ}, t_{PZL}

The 1KΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputsand GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{OE}$ input is held low.

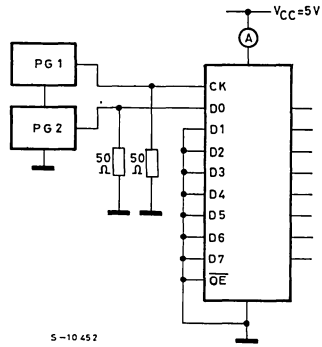
t_{PHZ}, t_{PZH}

The 1KΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{OE}$ input is held low.





TEST CIRCUIT I_{CC} (Opr.)



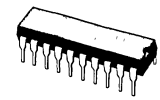
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

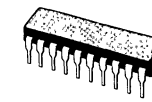
M54/74HCT374
M54/74HCT534

OCTAL D-TYPE FLIP FLOP WITH 3 STATE OUTPUT
HCT374 NON INVERTING - HCT534 INVERTING

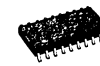
- HIGH SPEED
  f_{MAX} = 62 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $I_{OL} = |I_{OH}|$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS374/534



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

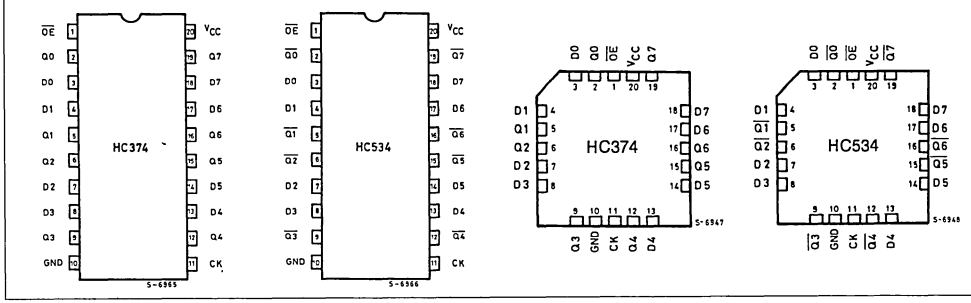
ORDER CODES :

M54HCTXXXF1R M74HCTXXXM1R
M74HCTXXXB1R M74HCTXXXC1R

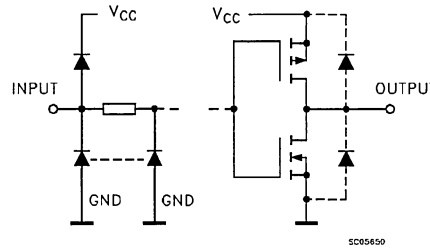
DESCRIPTION

The M54/74HCT374, M54/74HCT534, are high speed CMOS OCTAL D-TYPE FLIP FLOP WITH 3-STATE OUTPUTS fabricated with in silicon gate C^2MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power comsuption. These8-bit D-type flip-flops are controlled by a clock input (CK) and an ouput enable input ($\overline{OE}$). On the positive transition of the clock, the Q outputs will be set to the logic state that were setup at the D inputs (HCT374) or their complements (HCT534).
While the $\overline{OE}$ input is low, the eight outputs will be in a normal logic state (high or low logic level), and while high level, the outputs will be in a high impedance state. The output control does not affect the internal operation of flip-flops. That is, the old data can be retained or the new data can be entered even while the outputs are off. The application engineer has a choice of combination of inverting and non-inverting outputs. The 3-state output configuration and the wide choice of outline make bus-organized systems simple. All inputs are equipped with protection circuits against static discharge and transient excess voltage. This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

PIN CONNECTION (top view)



INPUT AND OUTPUT EQUIVALENT CIRCUIT



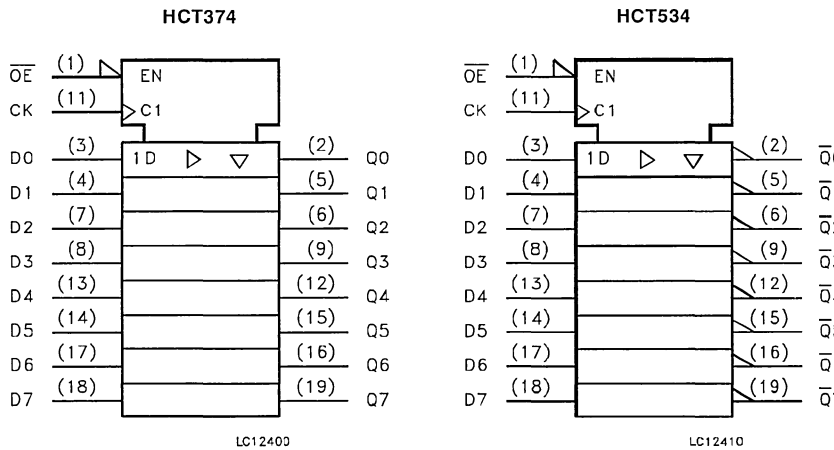
PIN DESCRIPTION (HCT374)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State output Enable Input (Active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0 to Q7	3 State outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data Inputs
11	CLOCK	Clock Input (LOW to HIGH, edge triggered)
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

PIN DESCRIPTION (HCT534)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State output Enable Input (Active LOW)
2, 5, 6, 9, 12, 15, 16, 19	$\overline{Q0}$ to $\overline{Q7}$	3 State outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data Inputs
11	CLOCK	Clock Input (LOW to HIGH, edge triggered)
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

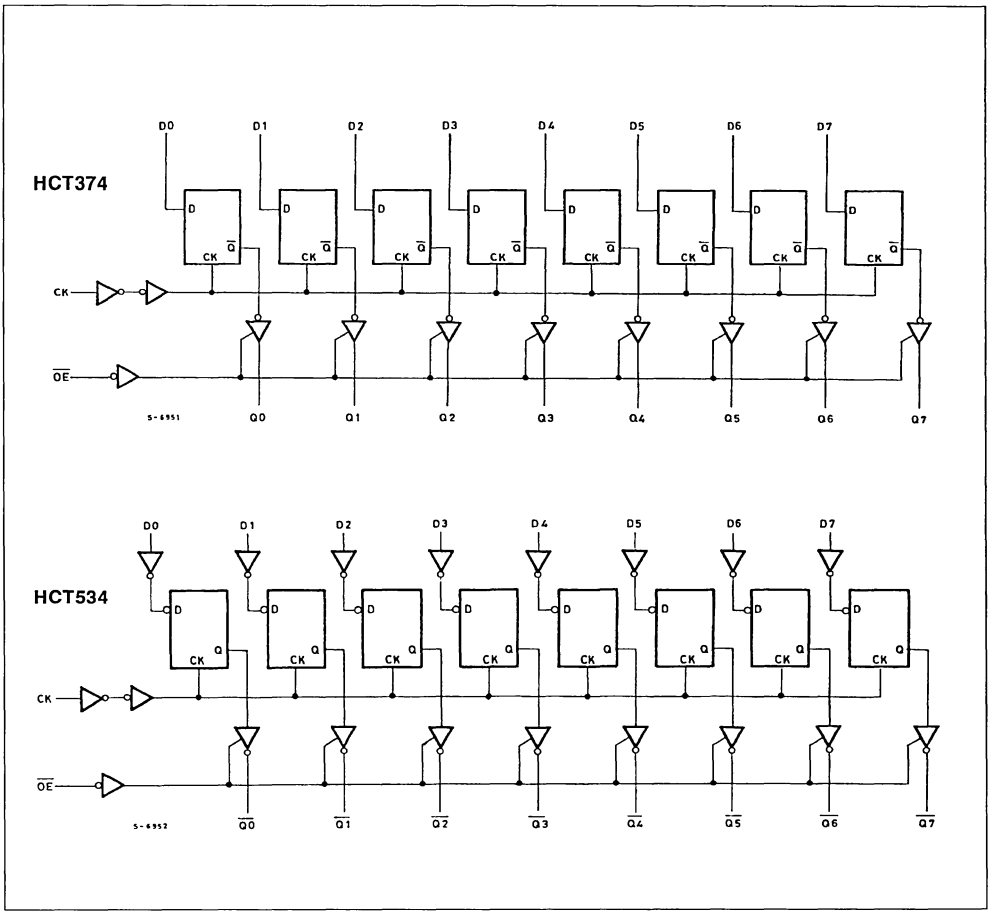
IEC LOGIC SYMBOLS



TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q (HC374)	$\overline{Q}$ (HC534)
H	X	X	Z	Z
L	↓	X	NO CHANGE	NO CHANGE
L	↑	L	L	H
L	↑	H	H	L

LOGIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-6.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 6.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				4		40		80	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9		3.0	mA

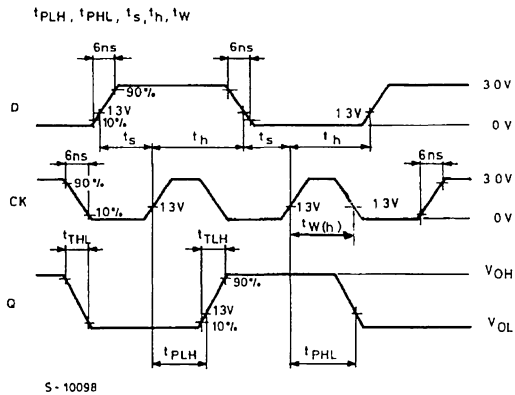
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5	50			7	12		15		18	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q, $\overline{Q}$)	4.5	50			20	30		38		45	ns
		4.5	150			25	38		48		57	ns
t_{PZL} t_{PZH}	Output Enable Time	4.5	50	R_L = 1 KΩ		17	30		38		45	ns
		4.5	150	R_L = 1 KΩ		25	38		48		57	ns
t_{PZL} t_{PZH}	Output Disable Time	4.5	50	R_L = 1 KΩ		16	28		35		42	ns
f_{MAX}	Maximum CLock Frequency	4.5	50		31	50		25		21		ns
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CLOCK)	4.5	50				15		19		23	ns
t_s	Minimum Set-up Time	4.5	50				15		19		23	ns
t_h	Minimum Hold Time	4.5	50				0		0		0	ns
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{OUT}	Out put Capacitance					10						pF
C_{PD} (*)	Power Dissipation Capacitance					48						pF

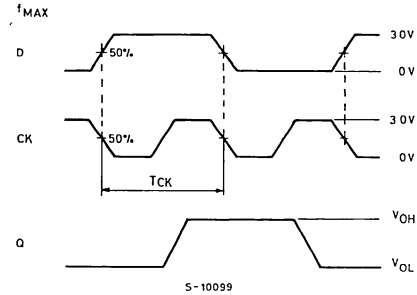
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per FLIP-FLOP) and C_{PD} when N pcs of FLIP-FLOP operate, can be gained by following equation: C_{PD} (TOTAL) = 38 + 18 x N (pF)

SWITCHING CHARACTERISTICS TEST WAVEFORM

t_{PLH}, t_{PHL}, t_s, t_h, t_w



f_{MAX}

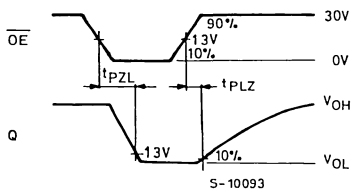


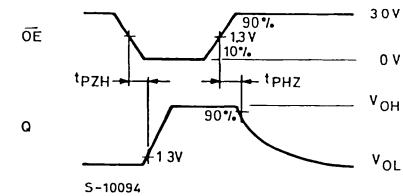
t_{PLZ}, t_{PZL}

The 1KΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputsand GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{OE}$ input is held low.

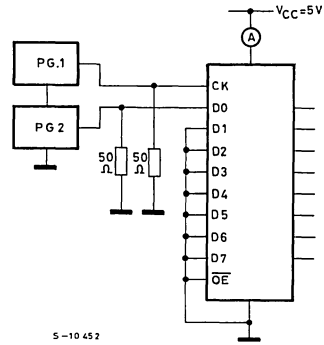
t_{PHZ}, t_{PZH}

The 1KΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{OE}$ input is held low.





TEST CIRCUIT I_{CC} (Opr.)



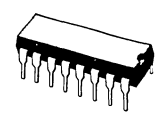
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

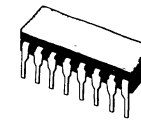
M54HC375
M74HC375

QUAD D TYPE LATCH

- HIGH SPEED
  t_{PD} = 14 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS375



B1R
(Plastic Package)



F1R
(Ceramic Package)

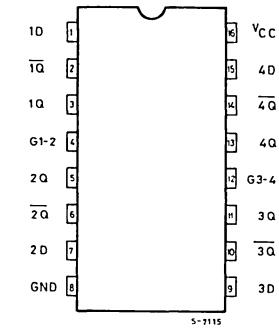
M1R
(Micro Package)

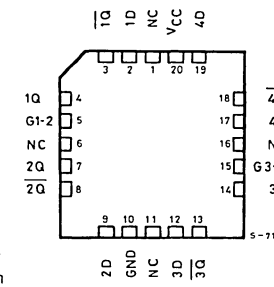
C1R
(Chip Carrier)

ORDER CODES :

M54HC375F1R M74HC375M1R
M74HC375B1R M74HC375C1R

PIN CONNECTIONS (top view)





NC =
No Internal
Connection

DESCRIPTION

The M54/74HC375 is a high speed CMOS QUAD D TYPE LATCH fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. It contains two groups of 2-bit latches controlled by an enable input (G1 · 2 or G3 · 4).

These two latch groups can be used in the different circuits. Each latch has Q and $\overline{Q}$ outputs (1Q to 4Q and $1\overline{Q}$ to $4\overline{Q}$). The data applied to the data input is transferred to the Q and $\overline{Q}$ outputs when the enable input is taken high and the outputs will follow the data input as long as the enable input is kept high. When the enable input is taken low, the information data applied to the data input at that time is retained at the outputs.

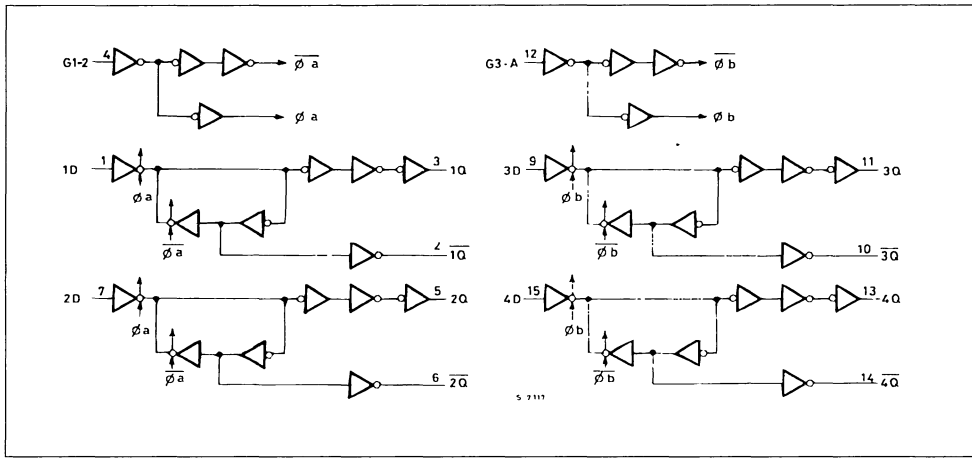
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

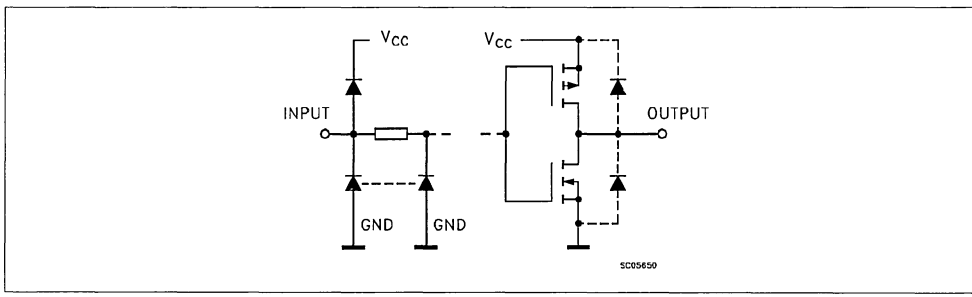
INPUTS		OUTPUTS		FUNCTION
D	G	Q	$\overline{Q}$	
L	H	L	H	
H	H	H	L	
X	L	Qn	$\overline{Qn}$	LATCH

X: DON'T CARE

LOGIC DIAGRAM



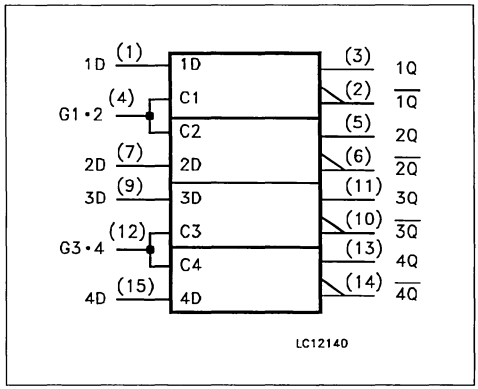
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 7, 9, 15	1D to 4D	Data Inputs
3, 5, 11, 13, 2, 6, 10, 14	1Q to 4Q $\overline{1Q}$ to $\overline{4Q}$	Outputs
4	G1- 2	Enable Input
12	G3 - 4	Enable Input
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

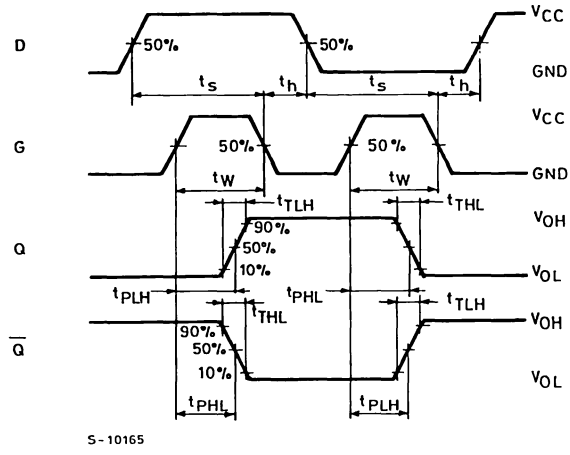
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				2		20		40	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

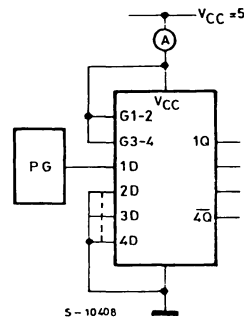
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (DATA - Q, $\overline{Q}$)	2.0			56	115		145		175	ns
		4.5			14	23		29		35	
		6.0			12	20		25		30	
t_{PLH} t_{PHL}	Propagation Delay Time (G - Q, $\overline{Q}$)	2.0			52	105		130		160	ns
		4.5			13	21		26		32	
		6.0			11	18		22		27	
$t_{(W)H}$	Minimum Enable Pulse Width (G)	2.0			12	75		95		115	ns
		4.5			3	15		19		23	
		6.0			3	13		16		20	
t_s	Minimum Set-up Time (DATA - G)	2.0			20	75		95		115	ns
		4.5			5	15		19		23	
		6.0			4	13		16		20	
t_h	Minimum Hold Time (DATA - G)	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				52						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



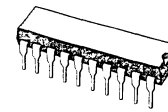
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

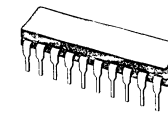
M54HC377
M74HC377

OCTAL D TYPE FLIP FLOP

- HIGH SPEED
  f_{MAX} = 73 MHz (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) at 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V to 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS377



B1R
(Plastic Package)



F1R
(Ceramic Package)

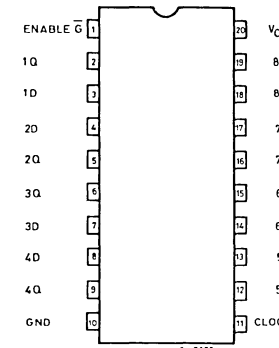
M1R
(Micro Package)

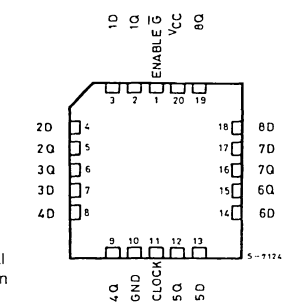
C1R
(Chip Carrier)

ORDER CODES :

M54HC377F1R M74HC377M1R
M74HC377B1R M74HC377C1R

PIN CONNECTIONS (top view)





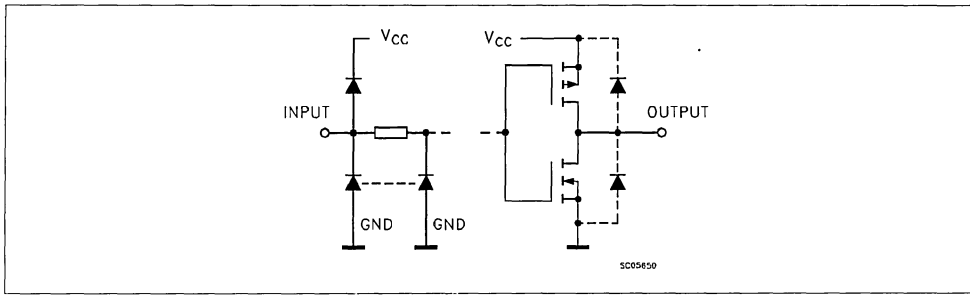
NC =
No Internal
Connection

DESCRIPTION

The M54/74HC377 is a high speed CMOS OCTAL-D-TYPE FLIP FLOP fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if the enable input $\overline{G}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT

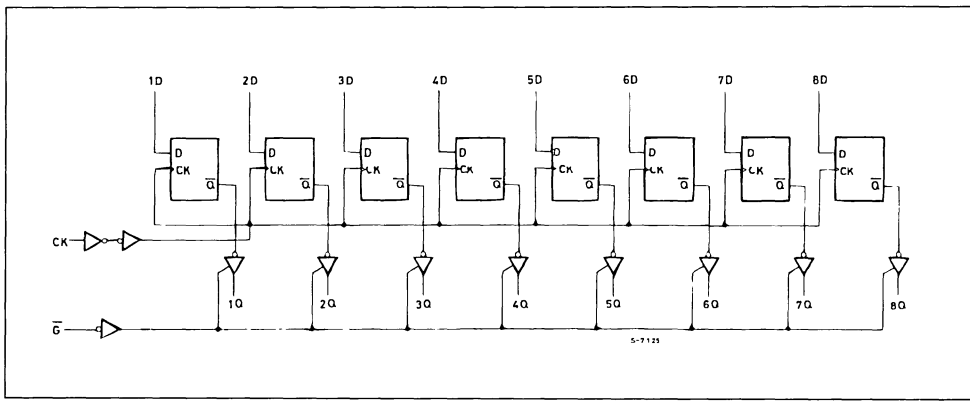


TRUTH TABLE

INPUTS			OUTPUT
$\overline{G}$	CLOCK	DATA	Q
H	X	X	NO CHANGE
L	⌐	L	L
L	⌐	H	H
X	⌙	X	NO CHANGE

X: DON'T CARE

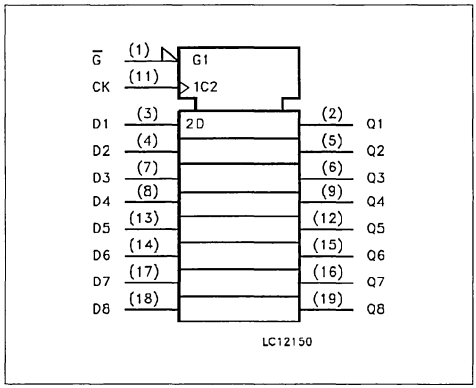
LOGIC DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	ENABLE $\overline{G}$	Data Enable Input (Active LOW)
2, 5, 6, 9, 12, 15, 16, 19	1Q to 8Q	Flip Flop Outputs
3, 4, 7, 8, 13, 14, 17, 18	1D to 8D	Data Inputs
11	CLOCK	Clock Input (LOW to HIGH, Edge-triggered)
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C. 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

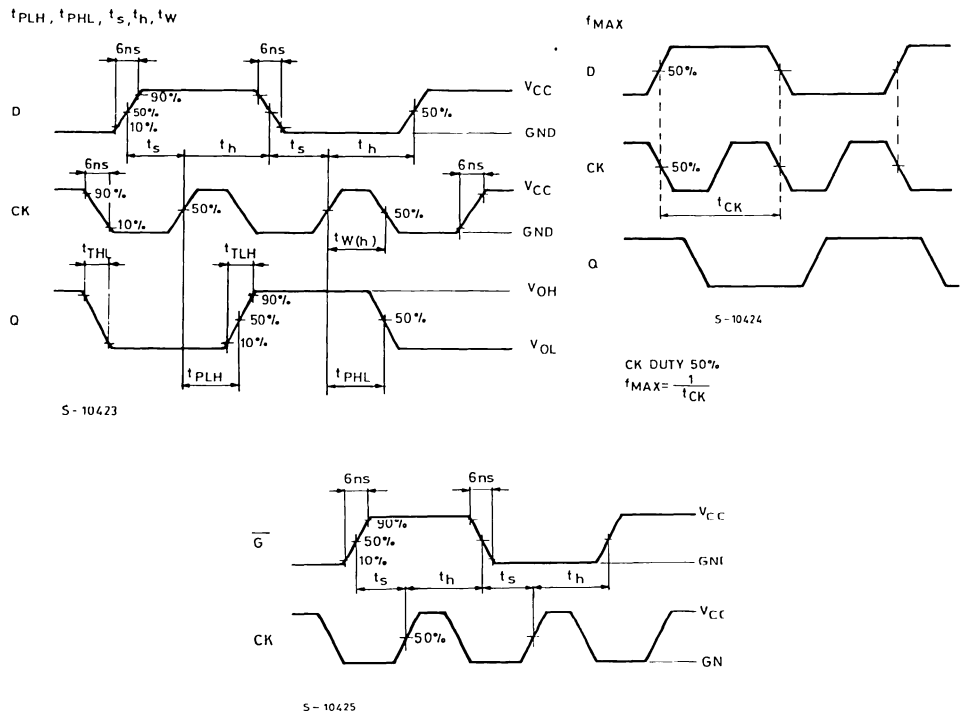
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4 13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

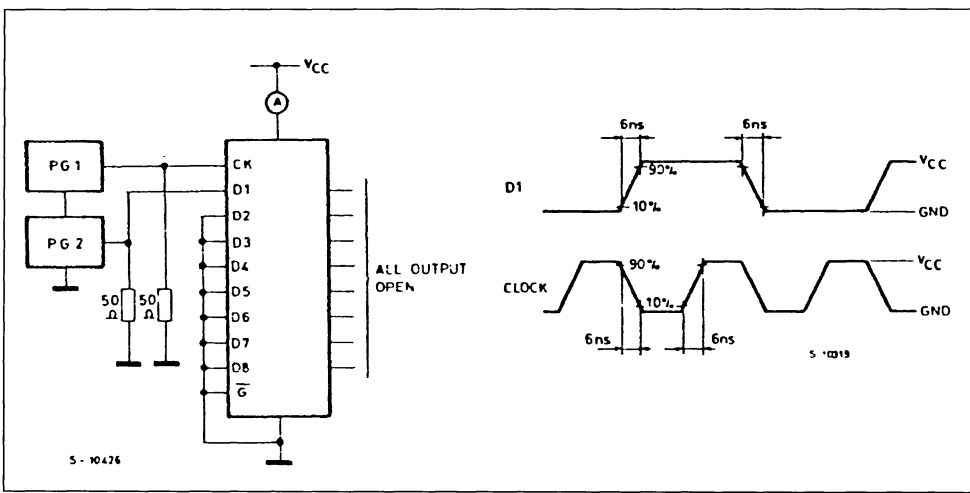
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q)	2.0			57	140		175		210	ns
		4.5			17	28		35		42	
		6.0			13	24		30		36	
f_{MAX}	Maximum Clock Frequency	2.0		7.2	14		5.8		4.8		MHz
		4.5		36	56		29		24		
		6.0		42	66		34		28		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0			24	75		95		115	ns
		4.5			6	15		19		23	
		6.0			5	13		16		20	
t_s	Minimum Set-up Time (D - CK)	2.0			24	75		95		115	ns
		4.5			6	15		19		23	
		6.0			5	13		16		20	
t_s	Minimum Set-up Time ($\overline{G}$ - CK)	2.0			30	75		95		115	ns
		4.5			8	15		19		23	
		6.0			6	13		16		20	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				34						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

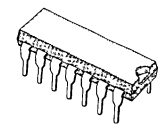


TEST CIRCUIT I_{CC} (Opr.)

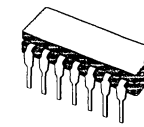


QUAD EXCLUSIVE OR GATE

- HIGH SPEED
  t_{PD} = 10 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS386



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HC386F1R M74HC386M1R
M74HC386B1R M74HC386C1R

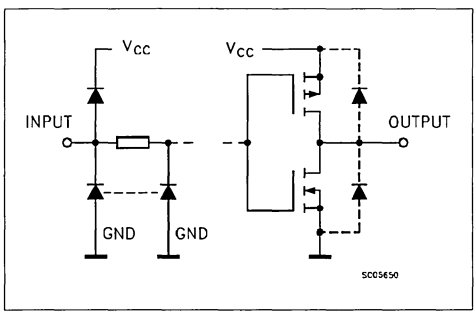
DESCRIPTION

The M54/74HC386 is a high speed CMOS QUAD EXCLUSIVE-OR GATE fabricated in silicon gate C^2MOS technology.

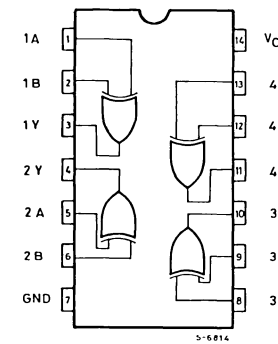
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. An output buffer provides high noise immunity and a stable output.

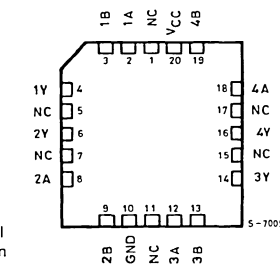
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



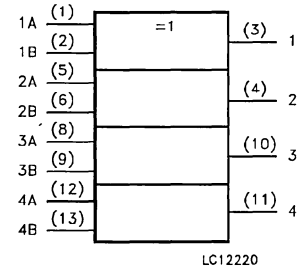


NC =
No Internal
Connection

TRUTH TABLE

A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

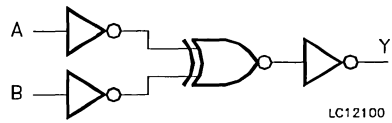
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 5, 6, 8, 9, 12, 13	1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B	Data Inputs
3, 4, 10, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

SCHEMATIC CIRCUIT (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

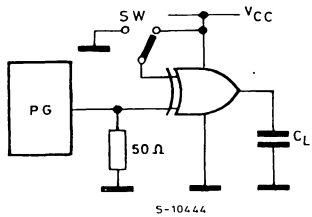
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 μA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 μA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	μA

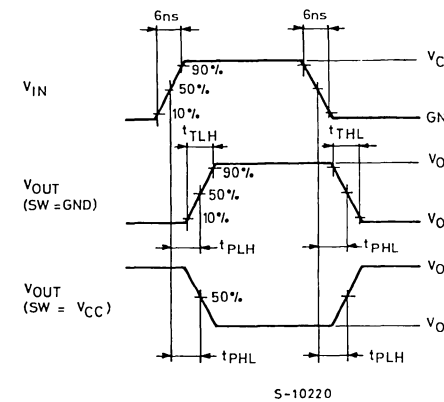
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			48	100		125		145	ns
		4.5			12	20		25		29	
		6.0			10	17		21		25	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				31						pF

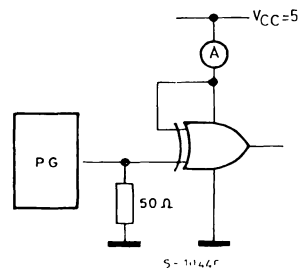
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit) Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT





TEST CIRCUIT I_{CC} (Opr.)



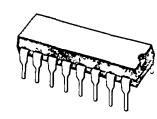
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

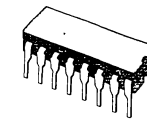
M54HC390
M74HC390

DUAL DECADE COUNTER

- HIGH SPEED
  f_{MAX} = 84 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS390



B1R
(Plastic Package)



F1R
(Ceramic Package)

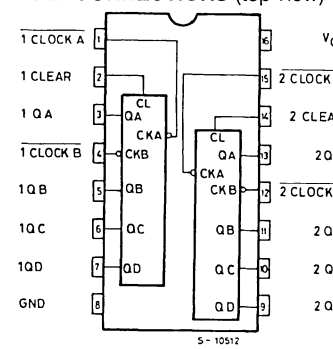
M1R
(Micro Package)

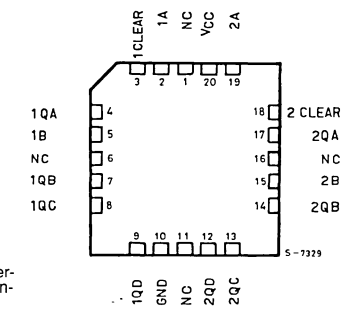
C1R
(Chip Carrier)

ORDER CODES :

M54HC390F1R M74HC390M1R
M74HC390B1R M74HC390C1R

PIN CONNECTIONS (top view)





NC = No Internal Connection

DESCRIPTION

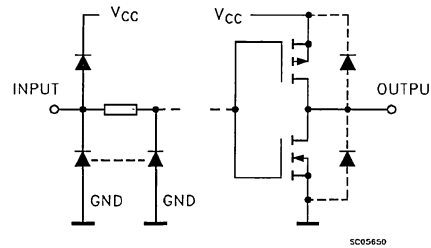
The M54/74HC390 is a high speed CMOS DUAL DECADE COUNTER fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

This dual decade counter contains two independent ripple carry counters. Each counter is composed of a divide-by-two and divide-by-five counter. The divide-by-two and divide-by-five counters can be cascaded to form dual decade, dual biquinary, or various combinations up to a single divide-by-100 counter.

Each 4-bit counter is incremented on the high to low transition (negative edge) of the clock input, and each has an independent clear input. When clear is set low all four bits of each counter are set to low. This enables count truncation and allows the implementation of divide-by-N counter configurations.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



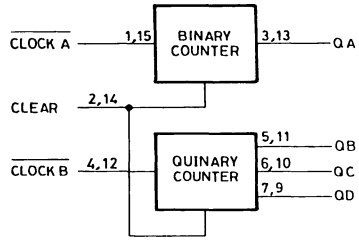
TRUTH TABLE

COUNT	OUTPUTS							
	BCD COUNT *				BI-QUINARY **			
	QD	QC	QB	QA	QA	QD	QC	QB
0	L	L	L	L	L	L	L	L
1	L	L	L	H	L	L	L	H
2	L	L	H	L	L	L	H	L
3	L	L	H	H	L	L	H	H
4	L	H	L	L	L	H	L	L
5	L	H	L	H	H	L	L	L
6	L	H	H	L	H	L	L	H
7	L	H	H	H	H	L	H	L
8	H	L	L	L	H	L	H	H
9	H	L	L	H	H	H	L	L

INPUTS			OUTPUTS			
$\overline{\text{CLOCK A}}$	$\overline{\text{CLOCK B}}$	CLEAR	QA	QB	QC	QD
X	X	H	L	L	L	L
⌐	X	L	BINARY COUNT UP			
X	⌐	L	QUINARY COUNT UP			

Note: * Output QA is connected to input $\overline{\text{CLOCK B}}$ for BCD count
** Output QD is connected to input $\overline{\text{CLOCK A}}$ for bi-quinary count

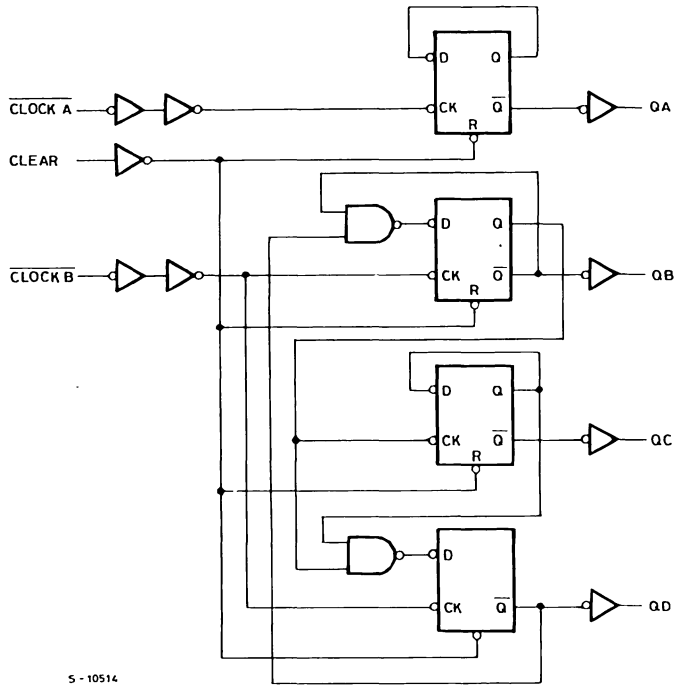
BLOCK DIAGRAM



V_{CC} = 16, GND = 8

S - 10513

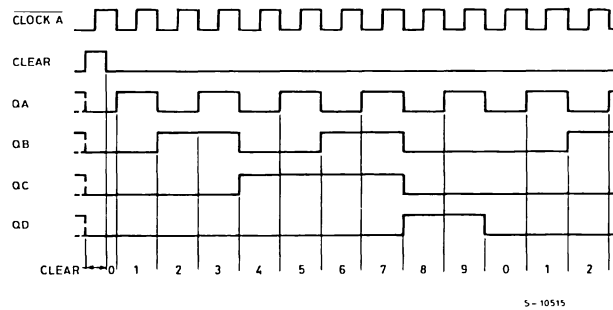
LOGIC DIAGRAM



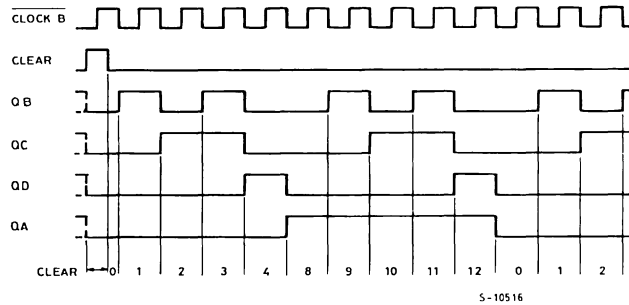
S - 10514

TIMING CHART

(1) BCD COUNT SEQUENCE *



(2) BI-QUINARY COUNT SEQUENCE **

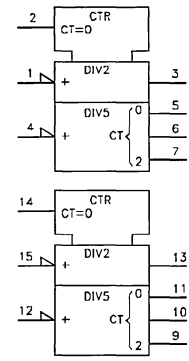


*OUTPUT QA IS CONNECTED TO INPUT $\overline{\text{CLOCK B}}$

PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{1\ CLOCK\ A}$ $\overline{2\ CLOCK\ B}$	Clock Input Divide by 2 Section (HIGH to LOW Edge-triggered)
2, 14	1 CLEAR 2 CLEAR	Asynchronous Master Reset Inputs
3, 5, 6, 7	1QA to 1QD	Flip Flop Outputs
4, 12	$\overline{1\ CLOCK\ B}$ $\overline{2\ CLOCK\ B}$	Clock Input Divide by 5 Section (HIGH to LOW Edge-triggered)
13, 11, 10, 9	2QA to 2QD	Flip Flop Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

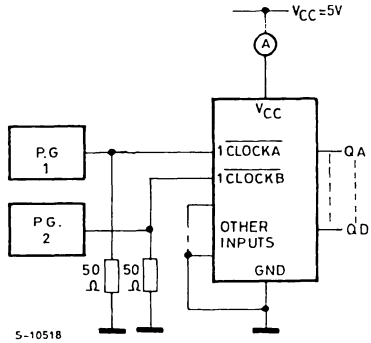
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

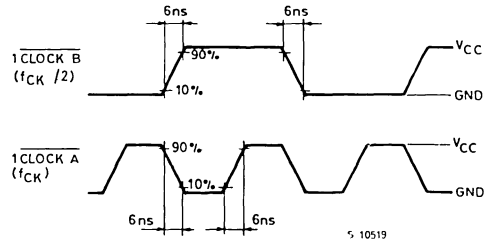
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK A - QA)	2.0			42	120		150		180	ns
		4.5			14	24		30		36	
		6.0			12	20		26		31	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK A - QB, QD)	2.0			45	120		150		180	ns
		4.5			15	24		30		36	
		6.0			13	20		26		31	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK A - QC)	2.0	QA Connected to CKB		108	280		350		420	ns
		4.5			36	56		70		84	
		6.0			31	48		60		71	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK B - QC)	2.0			72	185		230		280	ns
		4.5			24	37		46		56	
		6.0			20	31		39		48	
t_{PHL}	Propagation Delay Time (CLEAR - Qn	2.0			45	125		155		190	ns
		4.5			15	25		31		38	
		6.0			13	21		26		32	
f_{MAX}	Maximum Clock Frequency (CLOCK A - QA)	2.0		8.4	17		6.8		5.6		ns
		4 5		42	65		34		28		
		6.0		50	79		40		33		
f_{MAX}	Maximum Clock Frequency (CLOCK B - QB)	2.0		8.4	17		6.8		5.6		ns
		4.5		42	67		34		28		
		6.0		50	79		40		33		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Wisth (CLOCK)	2.0			24	75		95		110	ns
		4.5			6	15		19		22	
		6.0			5	13		16		19	
$t_{(W)H}$	Minimum Pulse Wisth (CLEAR)	2.0			24	75		95		110	ns
		4.5			6	15		19 -		22	
		6.0			5	13		16		19	
t_{REM}	Propagation Delay Time	2.0				25		30		35	ns
		4.5				5		6		7	
		6.0				5		5		6	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				84						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit) Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

TEST CIRCUIT I_{CC} (Opr.)



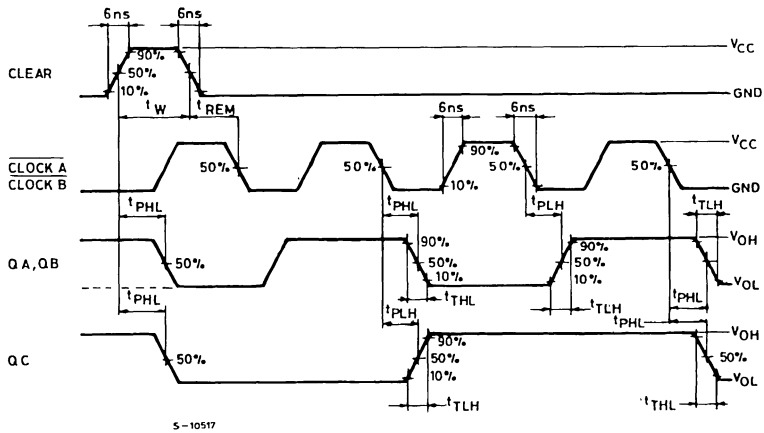


WHEN THE OUTPUTS DRIVE CAPACITIVE LOAD, TOTAL CURRENT CONSUMPTION IS TO BE A SUM OF THE VALUE CALCULATED FROM C_{PD} AND ΔI_{CC} OBTAINED FROM THE FOLLOWING FORMULA.

$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \cdot \frac{Ca}{2} + \frac{f_{CK}}{2} \cdot V_{CC} \cdot \left(\frac{2Cb}{5} + \frac{Cc}{5} + \frac{Cd}{5}\right)$$

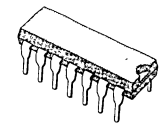
Ca – Cd ARE THE CAPACITANCE AT QA ~ QD OUTPUT

SWITCHING CHARACTERISTICS TEST WAVEFORM

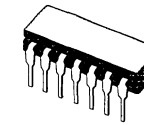


DUAL BINARY COUNTER

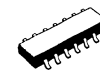
- HIGH SPEED
  f_{MAX} = 72 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS393



B1R
(Plastic Package)



F1R
(Ceramic Package)



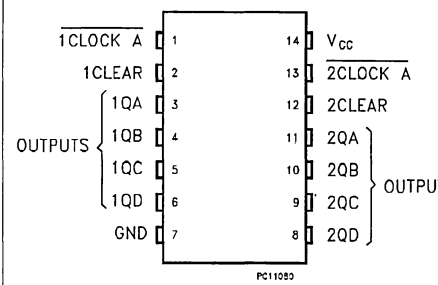
M1R
(Micro Package)

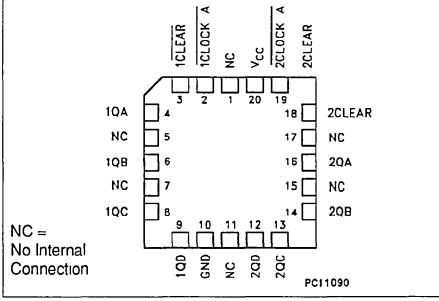
C1R
(Chip Carrier)

ORDER CODES :

M54HC393F1R M74HC393M1R
M74HC393B1R M74HC393C1R

PIN CONNECTIONS (top view)





DESCRIPTION

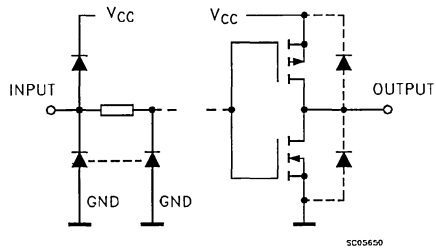
The M54/74HC393 is a high speed CMOS DUAL BINARY COUNTER fabricated in silicon gate C2MOS technology. It has the same high speed performance of LSTTL combined with true COMS low power consumption.

This counter circuit contains independent ripple carry counters and two 4-bit ripple carry binary counters, which can be cascated to create a single divide by 256 counter.

Each 4-bit counter is incremented on the high to low transition (negative edge) of the clock input,and each has an independent clear input. When clear is set to low all four bits of each counter are set to a low level. This enables count truncation and allows the implementation od divide by N counter configurations.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



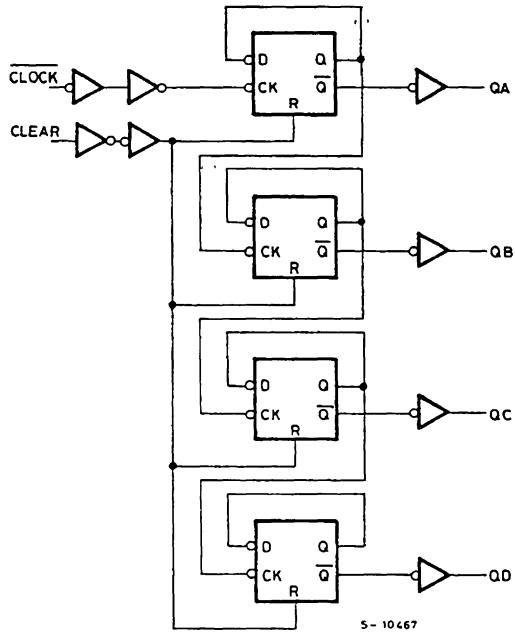
TRUTH TABLE

INPUTS		OUTPUS			
$\overline{\text{CLOCK}}$	CLEAR	QD	QC	QB	QA
X	H	L	L	L	L
⊓	L	COUNT UP			
⊔	L	NO CHANGE			

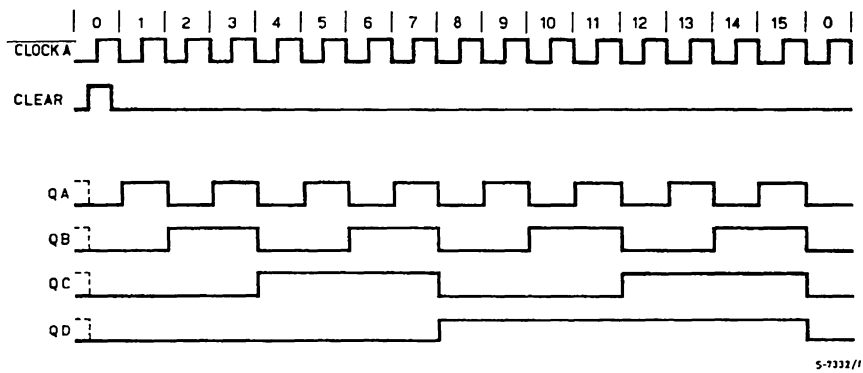
X: Don't Care

COUNT	OUTPUT			
	QD	QC	QB	QA
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

LOGIC DIAGRAM



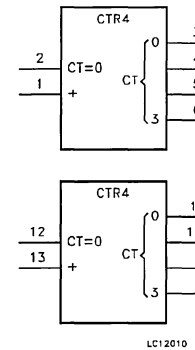
TIMING CHART



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 13	$\overline{1 \text{ CLOCK A}}$ $\overline{2 \text{ CLOCK A}}$	Clocck Input (HIGH to LOW Edge triggered)
2, 12	1 CLEAR 2 CLEAR	Asynchronouns Master Reset Inputs
3, 4, 5, 6	1QA to 1QD	Flip Flop Outputs
11, 10, 9, 8	2QA to 2QD	Flip Flop Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur Functional operation under these condition is not implied

(*) 500 mW. ≡ 65 °C derate to 300 mW by 10mW/°C. 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

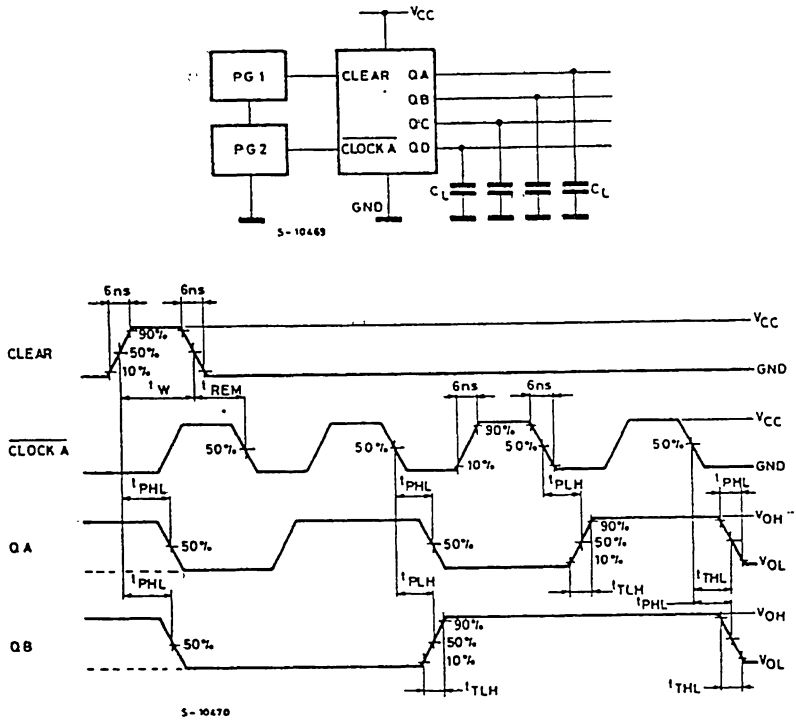
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

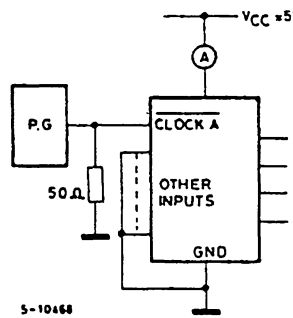
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLOCK}$ - QA)	2.0			50	120		150		180	ns
		4.5			15	24		30		36	
		6.0			13	20		26		31	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLOCK}$ - QB)	2.0			70	160		200		240	ns
		4.5			20	32		40		48	
		6.0			17	27		34		41	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLOCK}$ - QC)	2.0			90	195		245		295	ns
		4.5			25	39		49		59	
		6.0			21	33		42		50	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLOCK}$ - QD)	2.0			120	230		290		345	ns
		4.5			30	46		58		69	
		6.0			26	39		49		59	
t_{PLH} t_{PHL}	Propagation Delay Time (CLEAR - Qn)	2.0			55	150		190		225	ns
		4.5			18	30		38		45	
		6.0			15	26		32		38	
f_{MAX}	Maximum Clock Frequency	2.0		8.4	17		6.8		5.6		MHz
		4.5		42	67		34		28		
		6.0		50	79		40		33		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width ($\overline{CLOCK}$)	2.0			28	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	2.0			28	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
t_{REM}	Minimum Removal Time	2.0				25		30		35	ns
		4.5				5		6		7	
		6.0				5		5		6	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				35						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Flip Flop)

SWITCHING CHARACTERISTICS TEST WAVEFORM



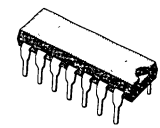
TEST CIRCUIT I_{CC} (Opr.)



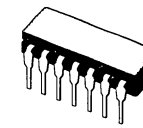
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

DUAL BINARY COUNTER

- HIGH SPEED
  f_{MAX} = 80 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS393



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HCT393F1R M74HCT393M1R
M74HCT393B1R M74HCT393C1R

DESCRIPTION

The M54/74HCT393 is a high speed CMOS DUAL BINARY COUNTER fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true COMS low power consumption.

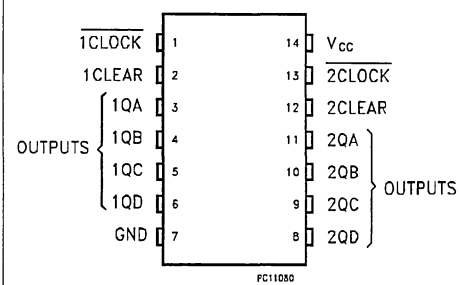
This counter circuit contains independent ripple carry counters and two 4-bit ripple carry binary counters, which can be cascated to create a single divide by 256 counter.

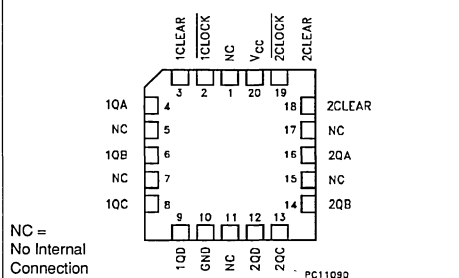
Each 4-bit counter is incremented on the high to low transition (negative edge) of the clock input,and each has an independent clear input. When clear is set to high all four bits of each counter are set to a low level. This enables count truncation and allows the implementation of divide by N counter configurations.

This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

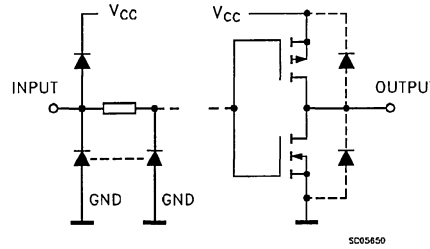
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)





INPUT AND OUTPUT EQUIVALENT CIRCUIT



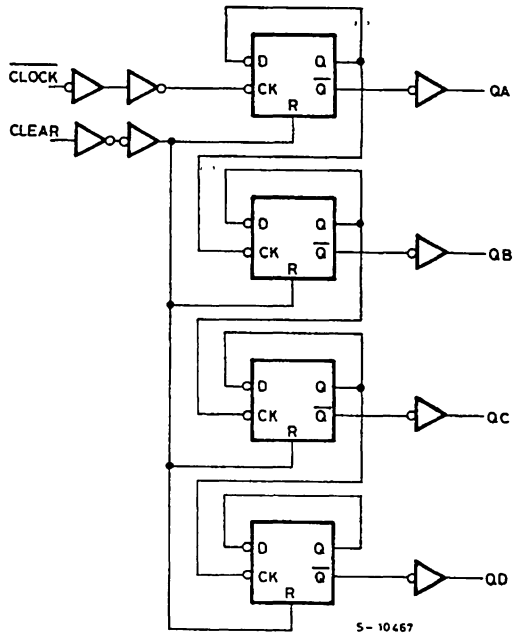
TRUTH TABLE

INPUTS		OUTPUS			
$\overline{\text{CLOCK}}$	CLEAR	QD	QC	QB	QA
X	H	L	L	L	L
⊓	L	COUNT UP			
⊔	L	NO CHANGE			

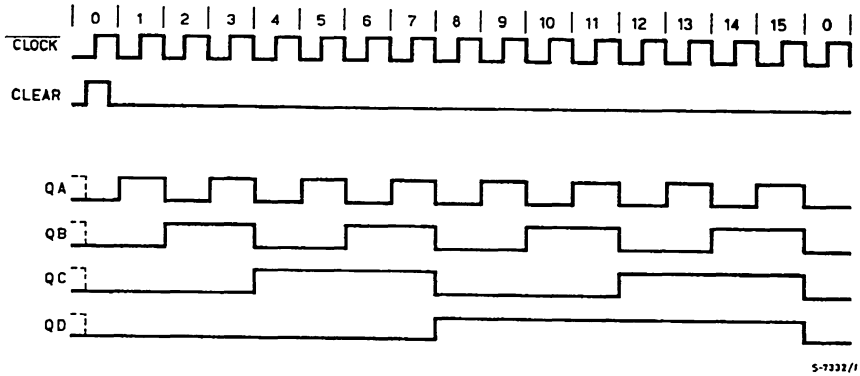
X: Don't Care

COUNT	OUTPUT			
	QD	QC	QB	QA
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

LOGIC DIAGRAM



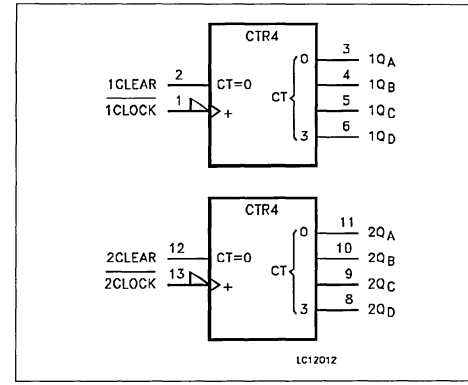
TIMING CHART



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 13	$\overline{1\ CLOCK}$ $\overline{2\ CLOCK}$	Clock Input (HIGH to LOW Edge triggered)
2, 12	1 CLEAR 2 CLEAR	Asynchronouns Master Reset Inputs
3, 4, 5, 6	1QA to 1QD	Flip Flop Outputs
11, 10, 9, 8	2QA to 2QD	Flip Flop Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW. ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

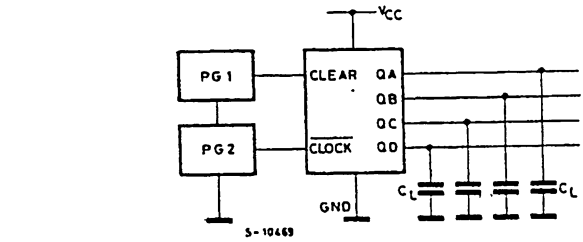
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				4		40		80	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND				2.0		2.9		3.0	mA

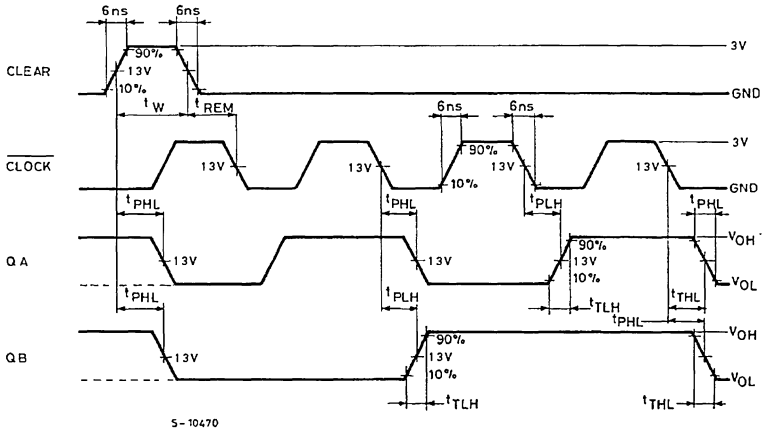
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			8	15		19		22	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - QA)	4.5			19	30		38		45	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - QB)	4.5			24	37		46		56	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - QC)	4.5			28	43		54		65	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - QD)	4.5			33	51		64		77	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLEAR - Qn)	4.5			20	31		39		47	ns
f_{MAX}	Maximum Clock Frequency	4.5		4.2	80		34				MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	4.5			8	15		19		22	ns
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	4.5			8	15		19		22	ns
t_{REM}	Minimum Removal Time	4.5				5		6		8	ns
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				66						pF

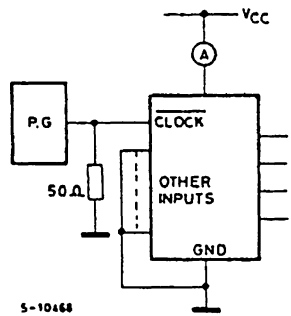
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Flip Flop)

SWITCHING CHARACTERISTICS TEST WAVEFORM





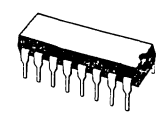
TEST CIRCUIT Icc (Opr.)



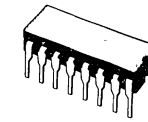
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

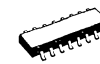
- HIGH SPEED
  t_{PD} = 25 ns (TYP) at V_{CC} = 5V
- LOW POWER DISSIPATION
  STANDBY STATE I_{CC}=4 µA (MAX.) AT T_A=25°C
  ACTIVE STATE I_{CC} = 700 µA (MAX.) AT V_{CC}=5V
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $I_{OH} = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- WIDE OUTPUT PULSE WIDTH RANGE
  t_{WOUT} = 120 ns ~ 60 s OVER AT V_{CC} = 4.5 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS423



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

DESCRIPTION

The M54/74HC423/423A are high speed CMOS MONOSTABLE multivibrators fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. There are two trigger inputs, $\overline{A}$ INPUT (negative edge) and B INPUT (positive edge). These inputs are valid for rising/falling signals, ($t_r - t_f$ – 1 sec). After triggering the output maintains the MONOSTABLE state for the time period determined by the external resistor Rx and capacitor Cx.

Two different pulse width constant are available:
K ≡ 0.46 for HC423 K ≡ 1 for HC423A.

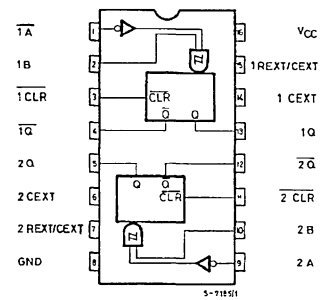
Taking $\overline{CLR}$ low breaks this MONOSTABLE STATE. If the next trigger pulse occurs during the MONOSTABLE period it makes the MONOSTABLE period longer. Limit for values of Cx and Rx :

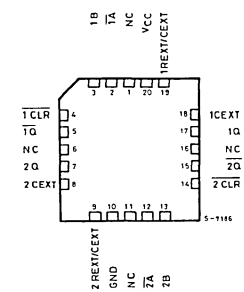
Cx : NO LIMIT

Rx : V_{CC} < 3.0 V 5 K Ω to 1 M Ω
$V_{CC} \geq$ 3.0 V 1 K Ω to 1 M Ω

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

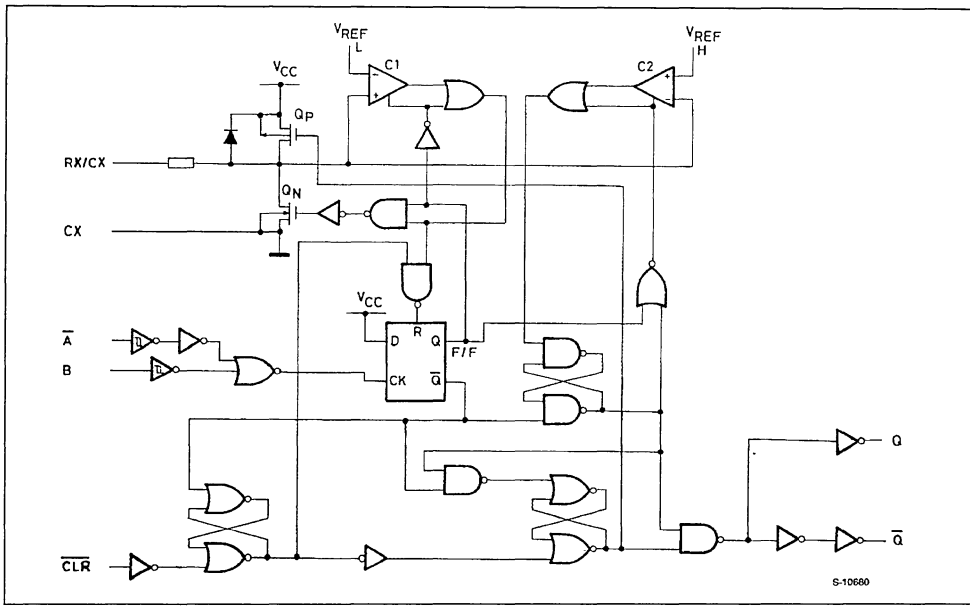
PIN CONNECTIONS (top view)



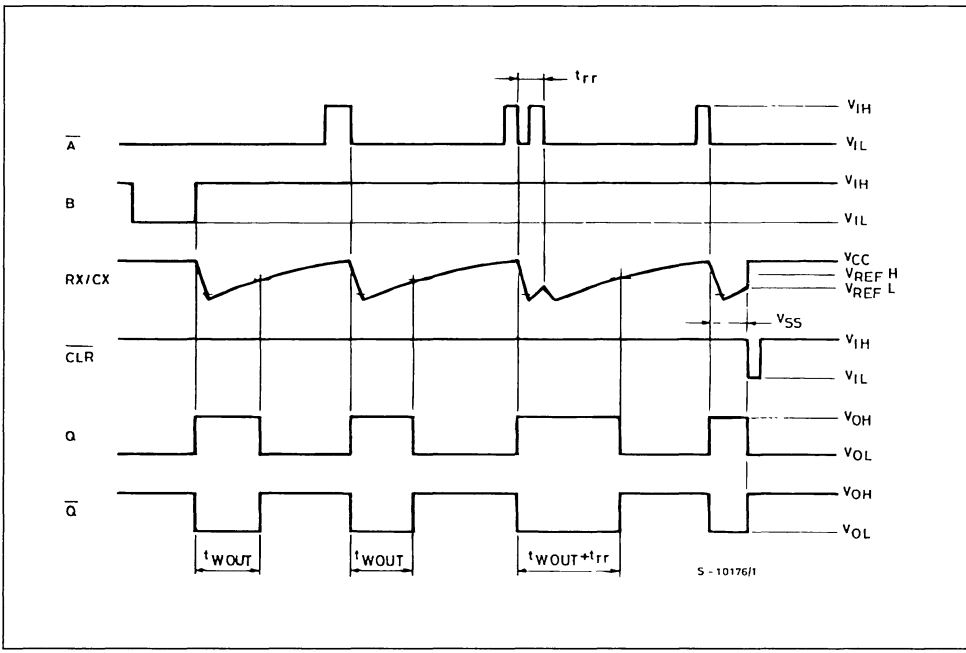


NC =
No Internal
Connection

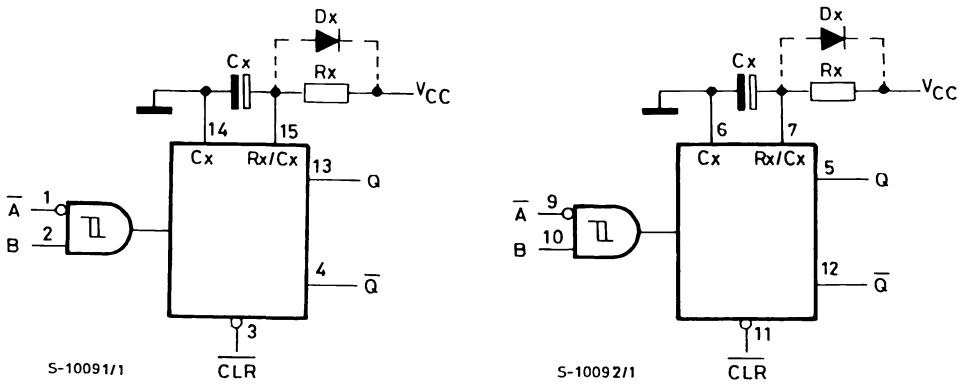
SYSTEM DIAGRAM



TIMING CHART



BLOCK DIAGRAM



Note :

(1) Cx, Rx, Dx are external components.

(2) Dx is a clamping diode.

The external capacitor is charged to V_{CC} in the stand-by state, i e. no trigger. When the supply voltage is turned off Cx is discharged mainly through an internal parasitic diode (see figures). If Cx is sufficiently large and V_{CC} decreases rapidy, there will be some possibility of damaging the I.C. with a surge current or latch-up. If the voltage supply filter capacitor is large enough and V_{CC} decrease slowly, the surge current is automatically limited and damage the I.C. is avoided. The maximum forward current of the parasitc diode is approximately 20 mA. In cases where Cx is large the time taken for the supply voltage to fall to 0.4 V_{CC} can be calculated as follows :

$t_f \geq (V_{CC} - 0.7) \cdot Cx/20mA$

In cases where t_f is too short an external clamping diode is required to protect the I.C. from the surge current.

FUNCTIONAL DESCRIPTION

STAND-BY STATE

The external capacitor, Cx, is fully charged to V_{CC} in the stand-by state. Hence, before triggering, transistor Qp and Qn (connected to the Rx/Cx node) are both turned-off. The two comparators that control the timing and the two reference voltage sources stop operating. The total supply current is therefore only leakage current.

TRIGGER OPERATION

Triggering occurs when :

1 st) A is "low" and B has a falling edge ;
2 nd) B is "high" and A has a rising edge ;
3 rd) A is low and B is high and C1 has a rising edge.

After the multivibrator has been retriggered comparator C1 and C2 start operating and Qn is turned on. Cx then discharges through Qn. The voltage at the node R/C external falls.

When it reaches V_{REFL} the output of comparator C1 becomes low. This in turn resets the flip-flop and Qn is turned off.

At this point C1 stops functioning but C2 continues to operate.

The voltage at R/C external begins to rise with a time constant set by the external components Rx, Cx.

Triggering the multivibrator causes Q to go high after internal delay due to the flip-flop and the gate. Q remains high until the voltage at R/C external rises again to V_{REFH}. At this point C2 output goes low and O goes low. C2 stop operating. That means that after triggering when the voltage R/C external returns to V_{REFH} the multivibrator has returned to its MONOSTABLE STATE. In the case where Rx · Cx are large enough and the discharge time of the capacitor and the delay time in the I.C. can be ignored, the width of the output pulse tw (out) is as follows :

$$t_{W(OUT)} = 0.46\ Cx \cdot Rx\ (HC423)$$
$$t_{W(OUT)} = Cx \cdot Rx\ (HC423A)$$

FUNCTIONAL DESCRIPTION (continued)

RE-TRIGGERED OPERATION

When a second trigger pulse follows the first its effect will depend on the state of the multivibrator. If the capacitor Cx is being charged the voltage level of R/C external falls to Vrefl again and Q remains high i.e. the retrigger pulse arrives in a time shorter than the period Rx · Cx seconds, the capacitor charging time constant. If the second trigger pulse is very close to the initial trigger pulse it is ineffective ; i.e. the second trigger must arrive in the capacitor discharge cycle to be ineffective; Hence the minimum time for a second trigger to be effective depends on V_{CC} and Cx.

RESET OPERATION

CL is normally high. If CL is low, the trigger is not effective because Q output goes low and trigger control flip-flop is reset.

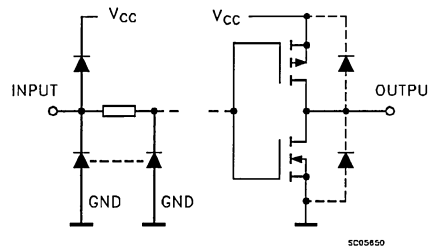
Also transistor Op is turned on and Cx is charged quicky to V_{CC}. This means if CL input goes low, the IC becomes waiting state both in operating and non operating state.

TRUTH TABLE

INPUTS			OUTPUTS		NOTE
$\overline{A}$	B	$\overline{CL}$	Q	$\overline{Q}$	
⌐	H	H	⌐¬	¬⌐	OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L	⌐	H	⌐¬	¬⌐	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X: Don't Care Z: High Impedance

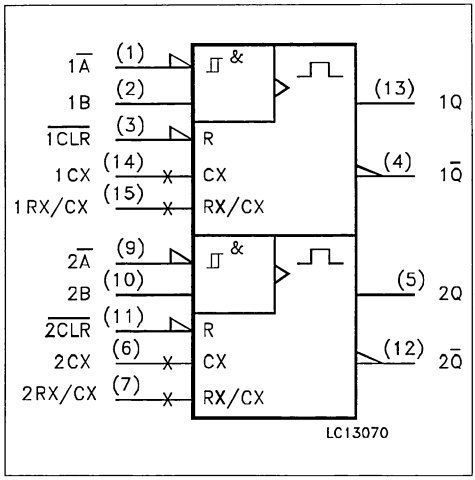
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 9	$1\overline{A}$, $2\overline{A}$	Trigger Inputs (Negative Edge Triggered)
2, 10	1B, 2B	Trigger Inputs (Positive Edge Triggered)
3, 11	$1\overline{CLR}$, $2\overline{CLR}$	Direct Reset (Active LOW)
4, 12	$1\overline{Q}$, $2\overline{Q}$	Outputs (Active LOW)
7	$2R_{EXT}/C_{EXT}$	External Resistor Capacitor Connection
13, 5	1Q, 2Q	Outputs (Active HIGH)
14, 6	$1C_{EXT}$ $2C_{EXT}$	External Capacitor Connection
15	$1R_{EXT}/C_{EXT}$	External Resistor Capacitor Connection
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time		0 to 1000	ns
			0 to 500	
			0 to 400	
C_X	External Capacitor		NO LIMITATION	
R_X	External Resistor	V_{CC} < 2 V	5K to 1M (*)	Ω
		V_{CC} ≥ 3 V	1K to 1M (*)	

(*) The maximum allowable values of Cx and Rx are a function of leakage of capacitor Cx, the leakage of device and leakage due to the board layout and surface resistance. Susceptibility to externally induced noise may occur for Rx > 1MΩ

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 μA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 μA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	μA
I_I	R/C Terminal Off State Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	μA
I_{CC}	Active State Supply Current (1)	2.0	V_I = V_{CC} or GND Pin 7 or 15 V_{IN} = V_{CC}/2			45	200		260		325	μA
		4.5				400	500		650		810	μA
		6.0				0.7	1.0		1.3		1.6	mA

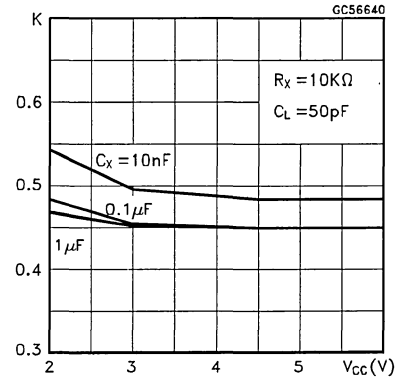
(1): Per Circuit

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

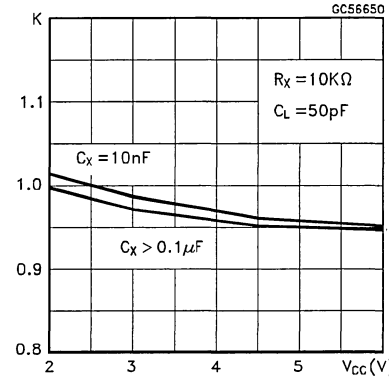
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95			ns
		4.5			8	15		19			
		6.0			7	13		16			
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{A}$, B - Q, $\overline{Q}$)	2.0			102	210		265			ns
		4.5			29	42		53			
		6.0			22	36		45			
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$ - Q, $\overline{Q}$)	2.0			68	160		200			ns
		4.5			20	32		40			
		6.0			16	27		34			
t_{WOUT}	Output Pulse Width (for HC423)	2.0	C_X = 100 pF R_X = 10 KΩ		1.3						µs
		4.5			1.1						
		6.0			1						
		2.0	C_X = 0.1 µF R_X = 100 KΩ		4.8						ms
		4.5			4.6						
		6.0			4.5						
t_{WOUT}	Output Pulse Width (for HC423A)	2.0	C_X = 100 pF R_X = 10 KΩ		1.7						µs
		4.5			1.4						
		6.0			1.3						
		2.0	C_X = 0.1 µF R_X = 100 KΩ		10						ms
		4.5			9.5						
		6.0			9.5						
Δt_{WOUT}	Output Pulse Width Error Between Circuits in Same Package				±1						%
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width	2.0				75		95			ns
		4.5				15		19			
		6.0				13		16			
$t_{W(L)}$	Minimum Pulse Width	2.0				75		95			ns
		4.5				15		19			
		6.0				13		16			
t_{rr}	Minimum Retrigger Time	2.0	C_X = 100 pF R_X = 1 KΩ		325						ns
		4.5			108						
		6.0			78						
		2.0	C_X = 0.1 µF R_X = 100 KΩ		5						µs
		4.5			1.4						
		6.0			1.2						
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				160						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$' Duty/100 + I_C/2 (per monostable) (I_{CC}': Active Supply Current) (Duty:%)

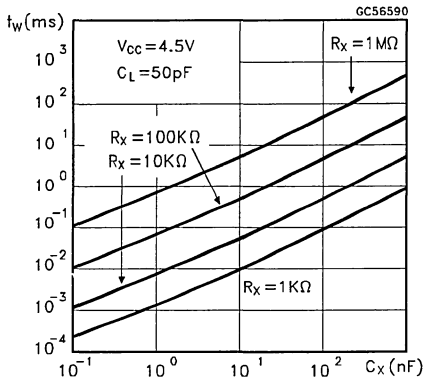
Output Pulse Width Constant Characteristics (for HC423)



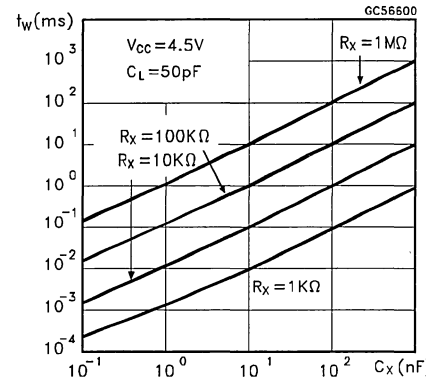
Output Pulse Width Constant Characteristics (for HC423A)



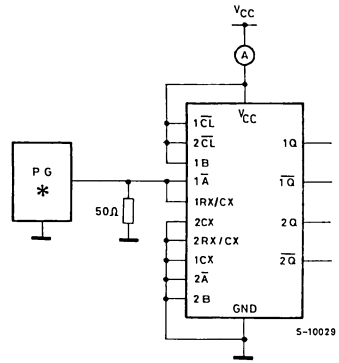
Output Pulse Width Characteristics (for HC423)



Output Pulse Width Characteristics (for HC423A)

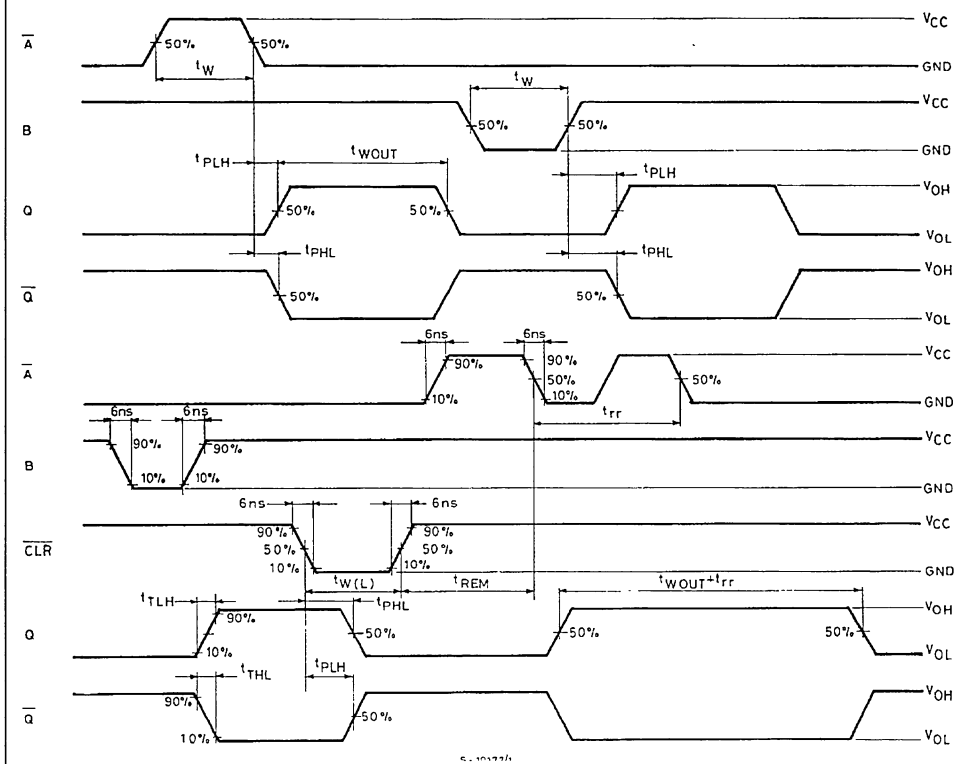


TEST CIRCUIT Icc (Opr)



* TRANSITION TIME OF INPUT WAVEFORM IS THE SAME AS THAT IN SASE OF SWITCHING CHARACTERISTICS TESTS.

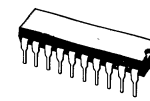
SWITCHING CHARACTERISTICS TEST WAVEFORM



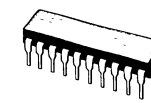
M54HC540/541
M74HC540/541

OCTAL BUS BUFFER WITH 3 STATE OUTPUTS
HC540: INVERTED - HC541 NON INVERTED

- HIGH SPEED
  t_{PD} = 10 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{INL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS540/541



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

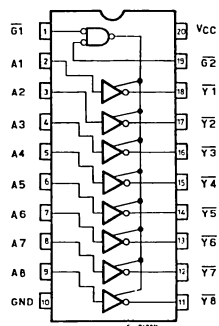
M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

DESCRIPTION

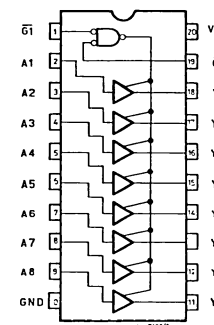
The M54/74HC540 and HC541 are high speed CMOS OCTAL BUS BUFFERS (3-STATE) fabricated in silicon gate C^2MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. The HC540 is an inverting buffer and HC541 is a non inverting buffer.
The 3 STATE control gate operates as a two input AND such that if either $\overline{G1}$ and $\overline{G2}$ are high, all eight output are in the high impedance state. In order to enhance PC board layout, the HC540 and HC541 offers a pinout having inputs and outputs on opposite sides of the package.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION (top view)

HC540

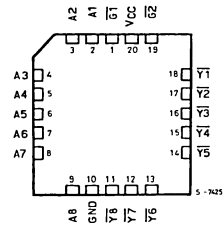


HC541

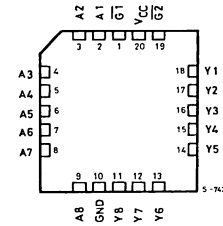


CHIP CARRIER

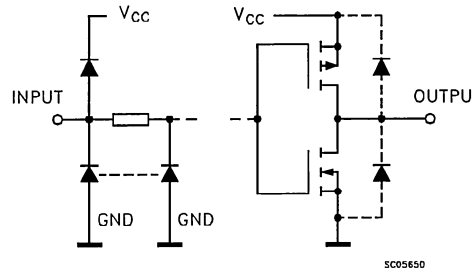
HC540



HC541



INPUT AND OUTPUT EQUIVALENT CIRCUIT



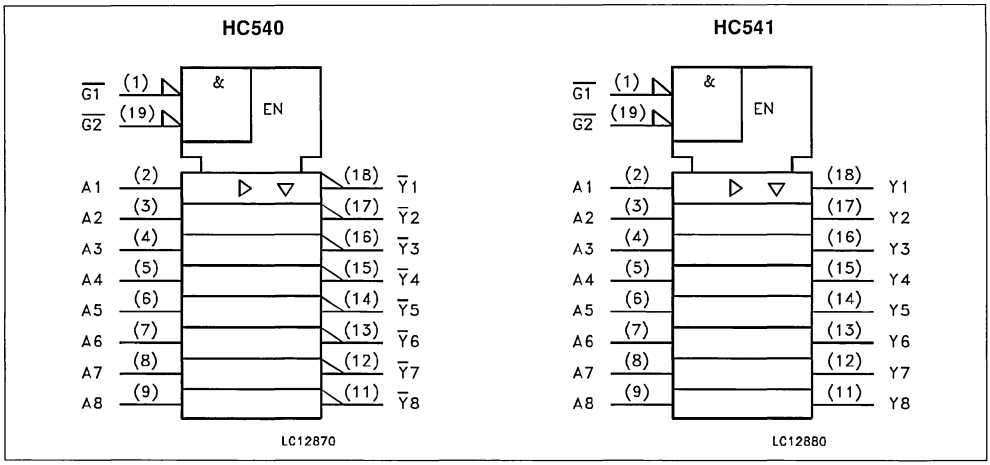
PIN DESCRIPTION (HC540)

PIN No	SYMBOL	NAME AND FUNCTION
1, 19	$\overline{1G}$, $\overline{G2}$	Output Enable Inputs
2, 3, 4, 5, 6, 7, 8, 9	A1 to A8	Data Inputs
18, 17, 16, 15, 14, 13, 12, 11	$\overline{Y1}$ to $\overline{Y8}$	Bus Outputs
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

PIN DESCRIPTION (HC541)

PIN No	SYMBOL	NAME AND FUNCTION
1, 19	$\overline{1G}$, $\overline{G2}$	Output Enable Inputs
2, 3, 4, 5, 6, 7, 8, 9	A1 to A8	Data Inputs
18, 17, 16, 15, 14, 13, 12, 11	Y1 to Y8	Bus Outputs
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS

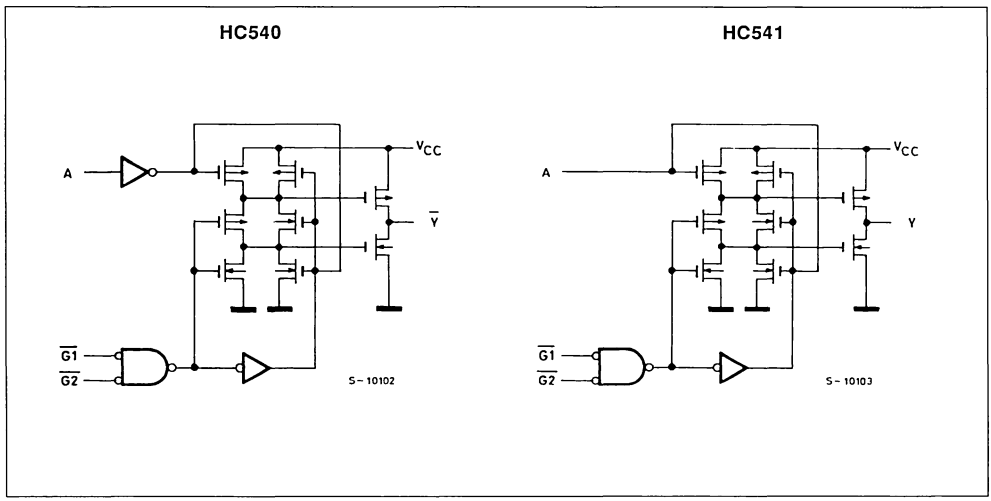


TRUTH TABLE

INPUT			OUTPUT	
$\overline{G1}$	$\overline{G2}$	An	$\overline{Yn}$ (HC540)	Yn (HC541)
H	X	X	Z	Z
X	H	X	Z	Z
L	L	H	L	H
L	L	L	H	L

X: "H" or "L"
Z: High impedance

CIRCUIT SCHEMATIC (Per Circuit)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
(*) 500 mW. ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series		-55 to +125	°C
	M74HC Series		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

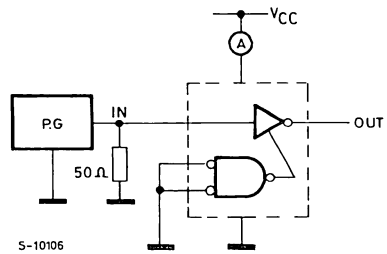
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

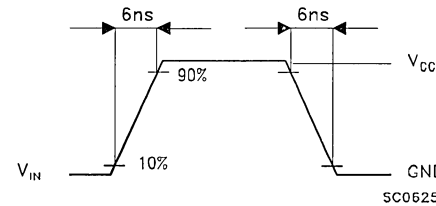
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75		90	ns
		4.5				7	12		19		18	
		6.0				6	10		13		15	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0	50			40	85		105		130	ns
		4.5				10	17		21		26	
		6.0				9	14		18		22	
		2.0	150			56	115		145		175	ns
		4.5				14	23		29		35	
		6.0				12	20		25		30	
t_{PZL} t_{PZH}	Output Enable Time	2.0	50	R_L = 1KΩ		47	110		140		165	ns
		4.5				13	22		28		33	
		6.0				11	19		24		28	
		2.0	150	R_L = 1KΩ		61	135		170		205	ns
		4.5				17	27		34		41	
		6.0				14	23		29		35	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0	50	R_L = 1KΩ		52	110		140		165	ns
		4.5				15	22		28		33	
		6.0				13	19		24		28	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance					31						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per gate)

TEST CIRCUIT I_{CC} (Opr.)

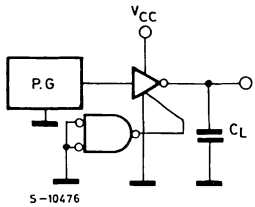
HC540



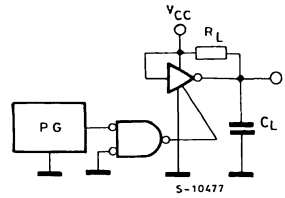


SWITCHING CHARACTERISTICS TEST CIRCUIT

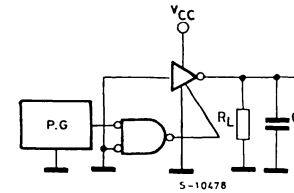
HC540



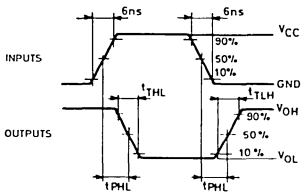
S-10476



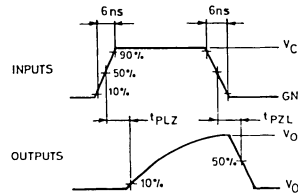
S-10477



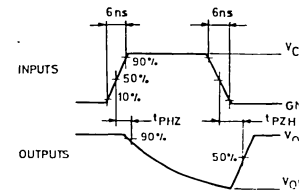
S-10478



S-10480

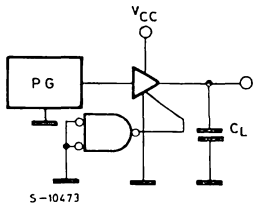


S-10471

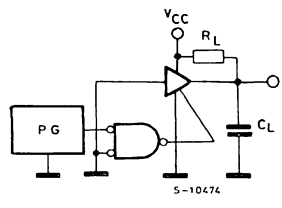


S-10472

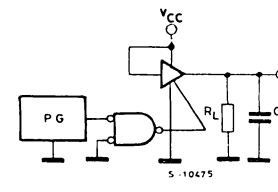
HC541



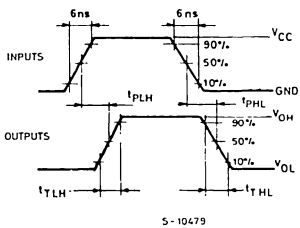
S-10473



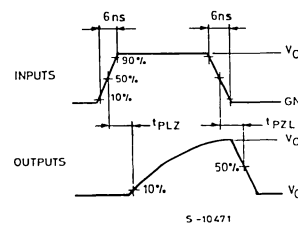
S-10474



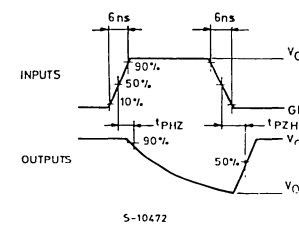
S-10475



S-10479



S-10471

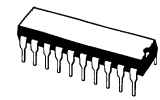


S-10472

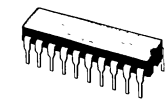
M54HCT540/541
M74HCT540/541

OCTAL BUS BUFFER WITH 3 STATE OUTPUTS
HCT540: INVERTED - HCT541 NON INVERTED

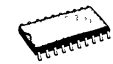
- HIGH SPEED
  t_{PD} = 10 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS540/541



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

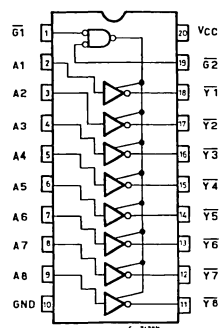
M54HCTXXXF1R M74HCTXXXM1R
M74HCTXXXB1R M74HCTXXXC1R

DESCRIPTION

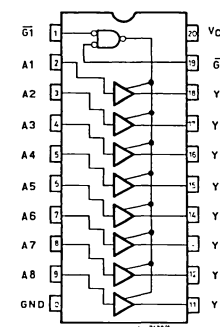
The M54/74HCT540 and HCT541 are high speed CMOS OCTAL BUS BUFFERS (3-STATE) fabricated in silicon gate C^2MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. The HCT540 is an inverting buffer and HCT541 is a non inverting buffer.
The 3 STATE control gate operates as a two input AND such that if either $\overline{G1}$ and $\overline{G2}$ are high, all eight outputs are in the high impedance state. In order to enhance PC board layout, the HCT540 and HCT541 offers a pinout having inputs and outputs on opposite sides of the package. All inputs are equipped with protection circuits against static discharge and transient excess voltage.
This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.
IT IS PROHIBITED TO APPLY A SIGNAL TO BUS TERMINAL WHEN IT IS IN OUTPUT MODE. WHEN A BUS TERMINAL IS FLOATING (HIGH IMPEDANCE STATE) IT IS REQUESTED TO FIX THE INPUT LEVEL BY MEANS OF EXTERNAL PULL DOWN OR PULL UP RESISTOR.

PIN CONNECTION (top view)

HCT540

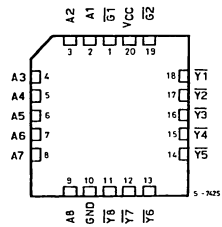


HCT541

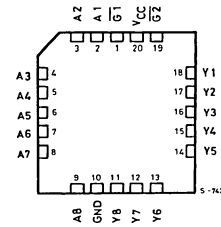


CHIP CARRIER

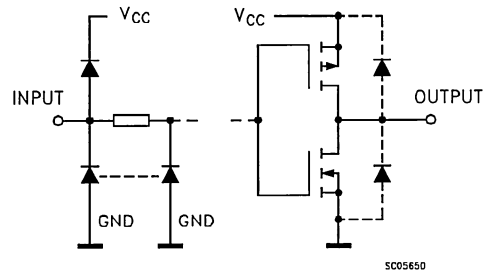
HCT540



HCT541



INPUT AND OUTPUT EQUIVALENT CIRCUIT



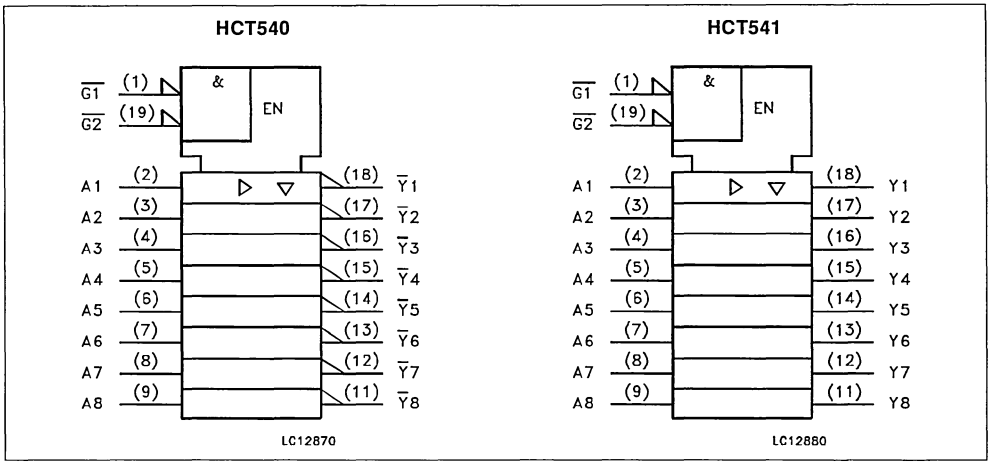
PIN DESCRIPTION (HCT540)

PIN No	SYMBOL	NAME AND FUNCTION
1, 19	$\overline{G1}$, $\overline{G2}$	Output Enable Inputs
2, 3, 4, 5, 6, 7, 8, 9	A1 to A8	Data Inputs
18, 17, 16, 15, 14, 13, 11, 12	$\overline{Y1}$ to $\overline{Y8}$	Bus Outputs
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

PIN DESCRIPTION (HCT541)

PIN No	SYMBOL	NAME AND FUNCTION
1, 19	$\overline{G1}$, $\overline{G2}$	Output Enable Inputs
2, 3, 4, 5, 6, 7, 8, 9	A1 to A8	Data Inputs
18, 17, 16, 15, 14, 13, 11, 12	Y1 to Y8	Bus Outputs
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS

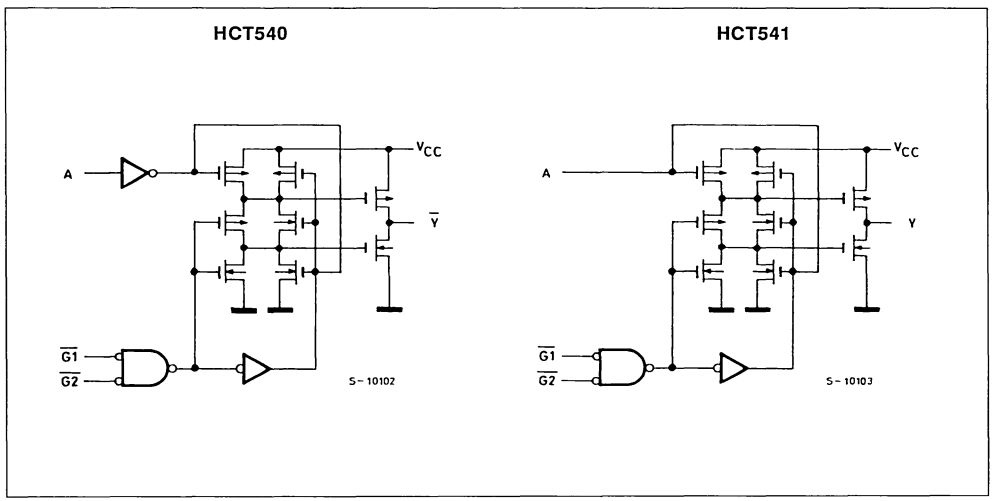


TRUTH TABLE

INPUT			OUTPUT	
$\overline{G1}$	$\overline{G2}$	An	$\overline{Yn}$ (HCT540)	Yn (HCT541)
H	X	X	Z	Z
X	H	X	Z	Z
L	L	H	L	H
L	L	L	H	L

X: "H" or "L"
Z: High impedance

CIRCUIT SCHEMATIC (Per Circuit)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-6.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 6.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	5.5	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5		±10	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				4		40		80	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND				2.0		2.9		3.0	mA

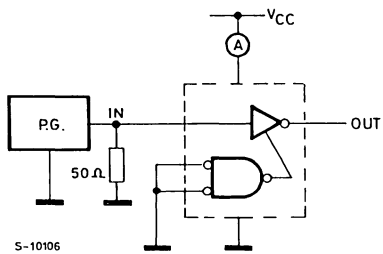
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

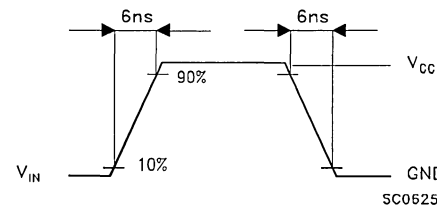
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5	50			6	12		15		18	ns
t_{PLH} t_{PHL}	Propagation Delay Time (for HCT540)	4.5	50			12	20		25		30	ns
		4.5	150			16	25		31		38	ns
t_{PLH} t_{PHL}	Propagation Delay Time (for HCT541)	4.5	50			14	23		29		35	ns
		4.5	150			18	28		35		42	ns
t_{PZL} t_{PZH}	Output Enable Time	4.5	50	R_L = 1KΩ		18	30		38		45	ns
		4.5	150	R_L = 1KΩ		22	34		43		51	ns
t_{PLZ} t_{PHZ}	Output Disable Time	4.5	50	R_L = 1KΩ		19	27		34		41	ns
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance					34						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per gate)

TEST CIRCUIT I_{CC} (Opr.)

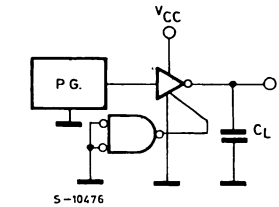
HCT540

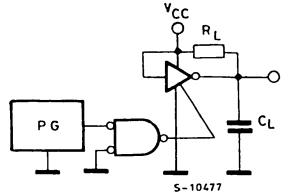


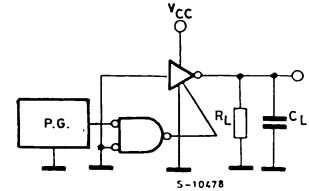


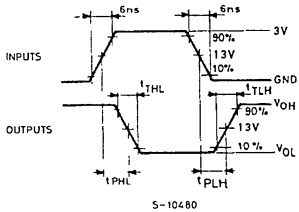
SWITCHING CHARACTERISTICS TEST CIRCUIT

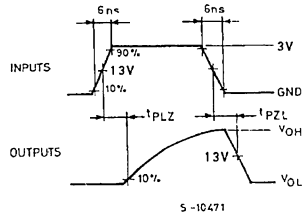
HCT540

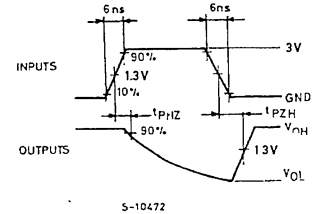




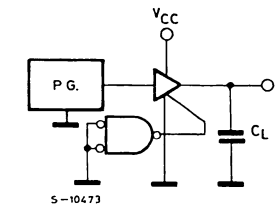


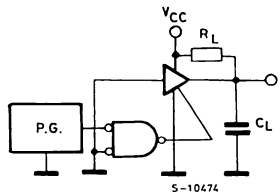


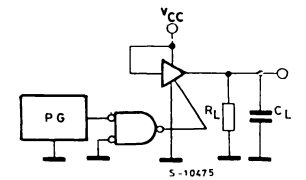


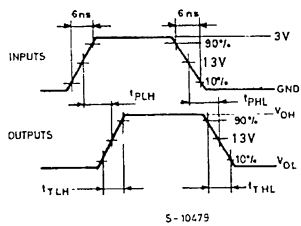


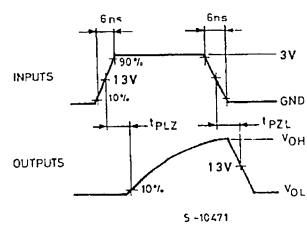
HCT541

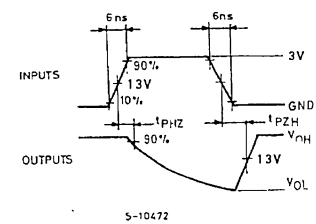










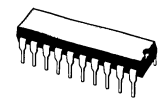


SGS-THOMSON MICROELECTRONICS

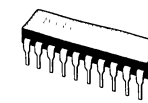
M54/74HC563
M54/74HC573

OCTAL D-TYPE LATCH WITH 3 STATE OUTPUT
HC563 INVERTING - HC573 NON INVERTING

- HIGH SPEED
  t_{PD} = 13 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $I_{OL} = |I_{OH}|$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS563/573



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

DESCRIPTION

The M54/74HC563 and M54HC573 are high speed CMOS OCTAL LATCH WITH 3-STATE OUTPUTS fabricated with in silicon gate C^2MOS technology.

These ICs archive the high speed operation similar to equivalent LSTTL while maintaning the CMOS low power dissipation.

These 8 bit D-Type latches are controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$).

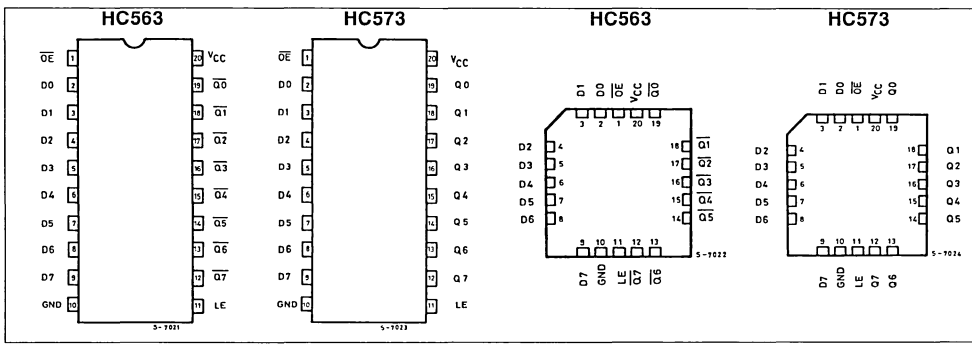
While the LE input is held at a high level, the Q outputs will follow the data input precisely or inversely. When the LE is taken low, the Q outputs will be latched precisely or inversely at the logic level of D input data. While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level) and while high level the outpts will be in a high impedance state.

The application designer has a choise of combination of inverting and non inverting outputs.

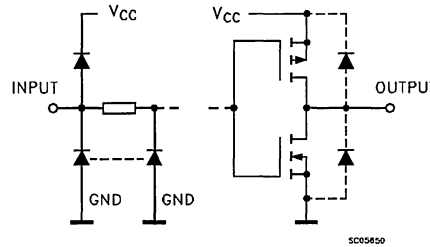
The three state output configuration and the wide choise of outline make bus organized system simple.

All inputs are equipped with protection circuits against discharge and transient excess voltage.

PIN CONNECTION (top view)



INPUT AND OUTPUT EQUIVALENT CIRCUIT



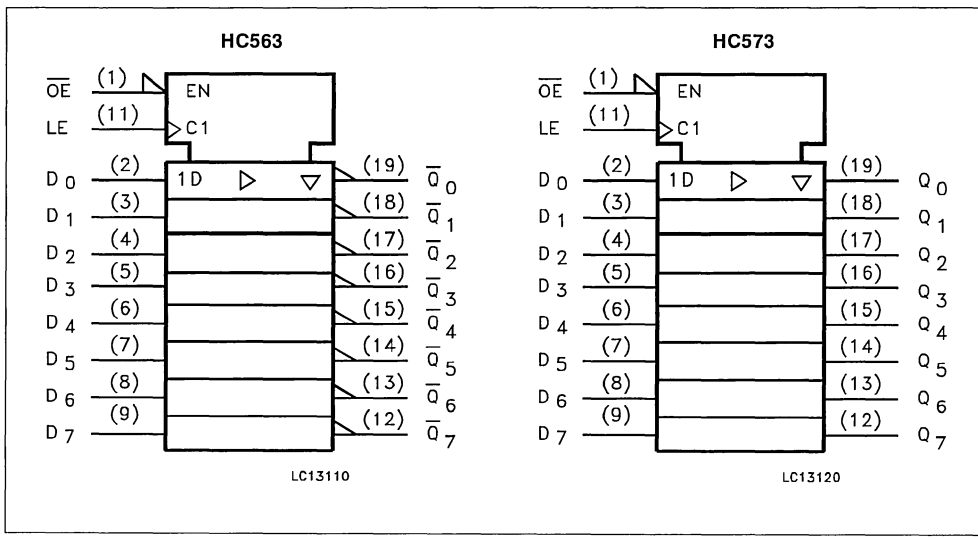
PIN DESCRIPTION (HC563)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State output Enable Input (Active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0 to D7	Data Inputs
12, 13, 14, 15, 16, 17, 18, 19	$\overline{Q0}$ to $\overline{Q7}$	3 State Latch Outputs
11	LE	Latch Enable Input
10	GND	Ground (0V)
20	Vcc	Positive Supply Voltage

PIN DESCRIPTION (HC573)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State output Enable Input (Active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0 to D7	Data Inputs
12, 13, 14, 15, 16, 17, 18, 19	Q0 to Q7	3 State Latch Outputs
11	LE	Latch Enable Input
10	GND	Ground (0V)
20	Vcc	Positive Supply Voltage

IEC LOGIC SYMBOLS



SGS-THOMSON MICROELECTRONICS

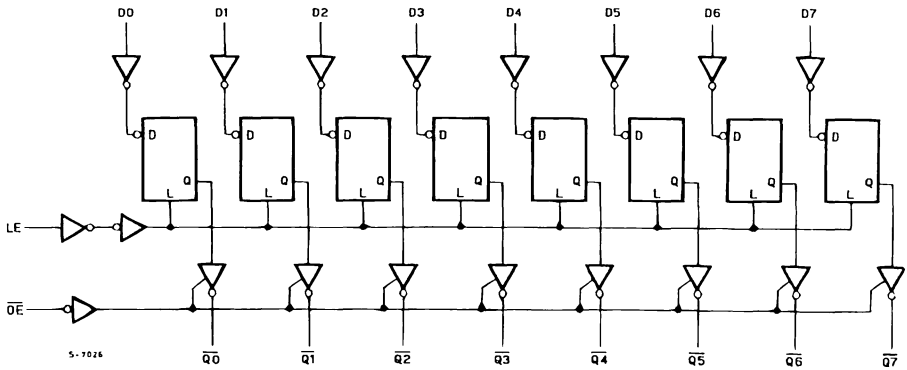
TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q (HC573)	$\overline{Q}$ (HC563)
H	X	X	Z	Z
L	L	X	NO CHANGE *	NO CHANGE *
L	H	L	L	H
L	H	H	H	L

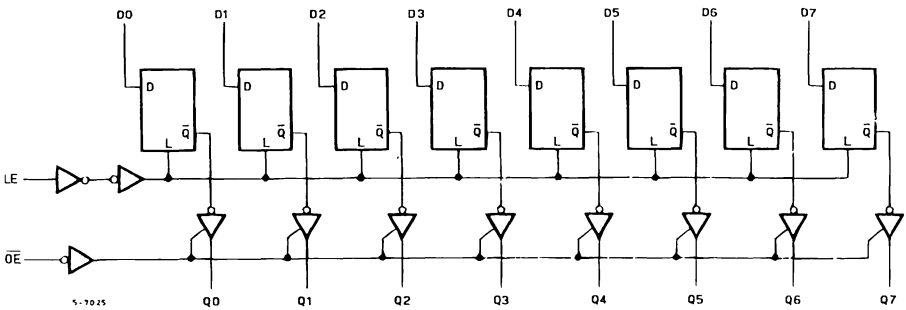
X: DON'T CARE
Z: HIGH IMPEDANCE
*: Q/$\overline{Q}$ OUTPUTS ARE LATCHED AT THE TIME WHEN THE LE INPUT IS TAKEN LOW LOGIC LEVEL.

LOGIC DIAGRAMS

HC563



HC573



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5.0		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t_{PLH} t_{PHL}	Propagation Delay Time (LE - Q, $\overline{Q}$)	2.0	50			50	115		145		175	ns
		4.5				15	23		29		35	
		6.0				13	20		25		30	
		2.0	150			60	155		195		235	ns
		4.5				20	31		39		47	
		6.0				17	26		33		40	
t_{PLH} t_{PHL}	Propagation Delay Time (D - Q, $\overline{Q}$)	2.0	50			42	110		140		165	ns
		4.5				14	22		28		33	
		6.0				12	19		24		28	
		2.0	150			57	150		190		225	ns
		4.5				19	30		38		45	
		6.0				16	26		32		38	
t_{PZL} t_{PZH}	3 State Output Enable Time	2.0	50	R_L = 1 KΩ		55	140		175		210	ns
		4.5				17	28		35		42	
		6.0				14	24		30		36	
		2.0	150	R_L = 1 KΩ		66	180		225		270	ns
		4.5				22	36		45		54	
		6.0				19	31		38		46	
t_{PLZ} t_{PHZ}	3 State Output Disable Time	2.0	50	R_L = 1 KΩ		40	125		155		190	ns
		4.5				17	25		31		38	
		6.0				15	21		26		32	
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width	2.0	50			40	75		95		110	ns
		4.5				8	15		19		22	
		6.0				7	13		16		19	
t_s	Minimum Set-up Time	2.0	50			16	50		65		75	ns
		4.5				5	10		13		15	
		6.0				3	9		11		13	
t_h	Minimum Hold Time	2.0	50				5		5		5	ns
		4.5					5		5		5	
		6.0					5		5		5	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{OUT}	Output Capacitance					10						pF
C_{PD} (*)	Power Dissipation Capacitance		for HC563 for HC573			49 51						pF

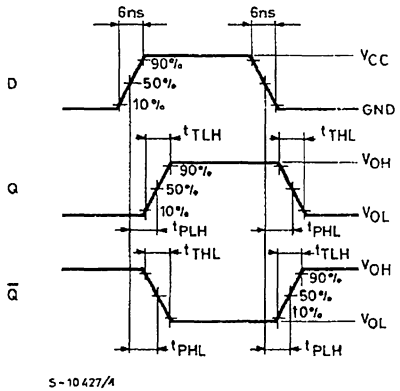
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Gate)

The CPD when n pcs of FLIP-FLOP operate, can be gained by following equations:

for HC563 CPD (TOTAL) = 33 + 16 x n [pF], for HC573 CPD (TOTAL) = 33 + 18 x n [pF]

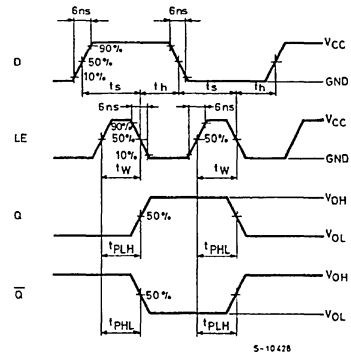
SWITCHING CHARACTERISTICS TEST WAVEFORM

t_{PLH}, t_{PHL}, (D - Q, $\overline{Q}$)



S-10427/A

t_{PLH}, t_{PHL}, (LE - Q, $\overline{Q}$) t_s, t_h, t_w



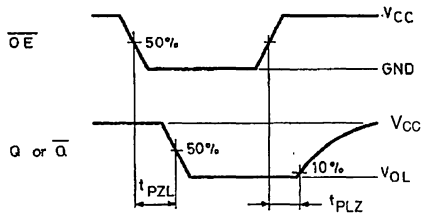
S-10428

t_{PLZ}, t_{PZL}

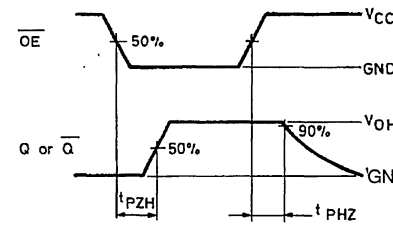
The 1KΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputsand GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{OE}$ input is held low.

t_{PHZ}, t_{PZH}

The 1KΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{OE}$ input is held low.

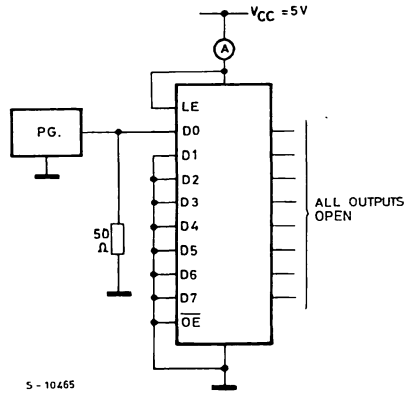


S-10429



S-10430

TEST CIRCUIT I_{CC} (Opr.)



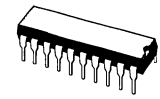
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

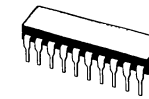
M54/74HCT563
M54/74HCT573

OCTAL D-TYPE LATCH WITH 3 STATE OUTPUT
HCT563 INVERTING - HCT573 NON INVERTING

- HIGH SPEED
  t_{PD} = 18 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $I_{OL} = |I_{OH}|$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS563/573



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

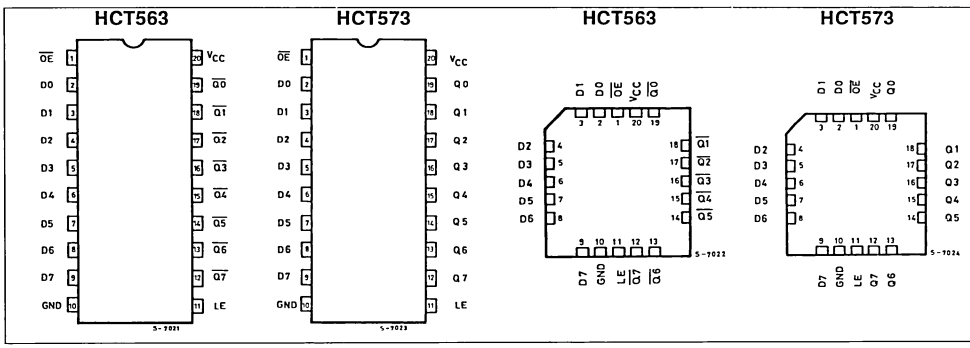
ORDER CODES :

M54HCTXXXF1R M74HCTXXXM1R
M74HCTXXXB1R M74HCTXXXC1R

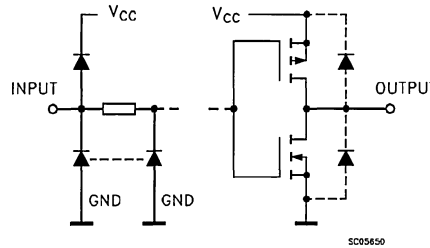
DESCRIPTION

The M54/74HCT563 and M54HCT573 are high speed CMOS OCTAL LATCH WITH 3-STATE OUTPUTS fabricated with silicon gate C^2MOS technology.
These ICs achive the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
These 8 bit D-Type latches are controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$).
While the LE input is held at a high level, the Q outputs will follow the data input precisely or inversely. When the LE is taken low, the Q outputs will be latched precisely or inversely at the logic level of D input data. While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level) and while high level the outpts will be in a high impedance state.
The application designer has a choise of combination of inverting and non inverting outputs.
This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.
All inputs are equipped with protection circuits against discharge and transient excess voltage.

PIN CONNECTION (top view)



INPUT AND OUTPUT EQUIVALENT CIRCUIT



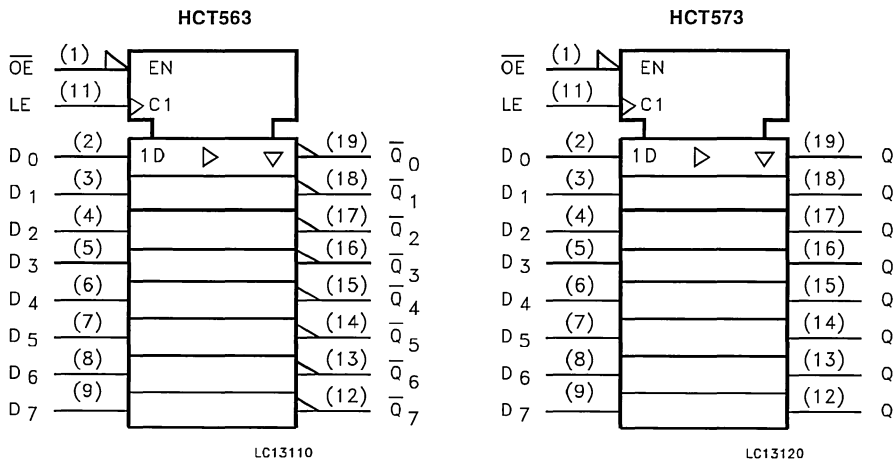
PIN DESCRIPTION (HCT563)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State output Enable Input (Active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0 to D7	Data Inputs
12, 13, 14, 15, 16, 17, 18, 19	$\overline{Q0}$ to $\overline{Q7}$	3 State Latch Outputs
11	LE	Latch Enable Input
10	GND	Ground (0V)
20	Vcc	Positive Supply Voltage

PIN DESCRIPTION (HCT573)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State output Enable Input (Active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0 to D7	Data Inputs
12, 13, 14, 15, 16, 17, 18, 19	Q0 to Q7	3 State Latch Outputs
11	LE	Latch Enable Input
10	GND	Ground (0V)
20	Vcc	Positive Supply Voltage

IEC LOGIC SYMBOLS



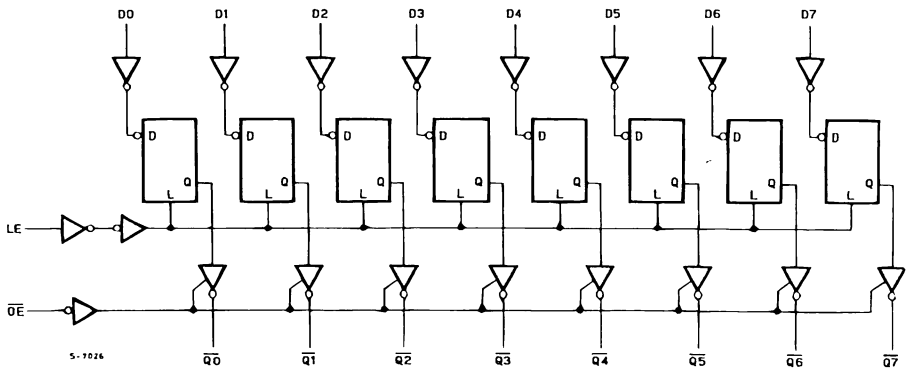
TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q (HCT573)	$\overline{Q}$ (HCT563)
H	X	X	Z	Z
L	L	X	NO CHANGE *	NO CHANGE *
L	H	L	L	H
L	H	H	H	L

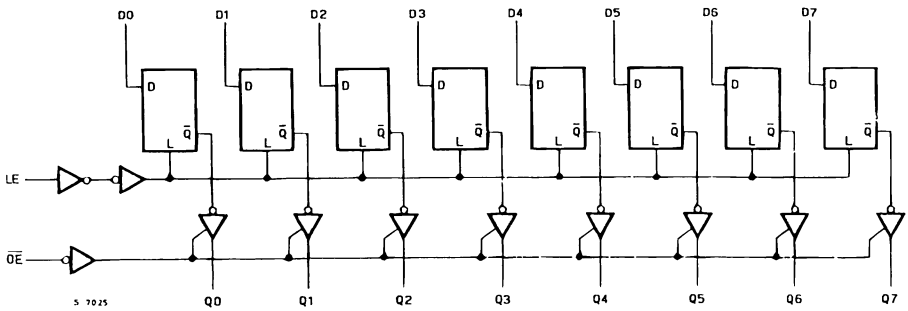
X: DON'T CARE
Z: HIGH IMPEDANCE
*: Q/$\overline{Q}$ OUTPUTS ARE LATCHED AT THE TIME WHEN THE LE INPUT IS TAKEN LOW LOGIC LEVEL.

LOGIC DIAGRAMS

HCT563



HCT573



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-6.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 6.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	5.5	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5.0		±10	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				4		40		80	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND				2.0		2.9		3.0	mA

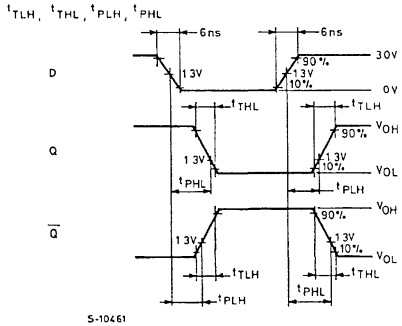
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5	50			7	12		15		18	ns
t_{PLH} t_{PHL}	Propagation Delay Time (LE - Q, $\overline{Q}$)	4.5	50			21	33		41		50	ns
		4.5	150			25	39		49		59	ns
t_{PLH} t_{PHL}	Propagation Delay Time (D - Q, $\overline{Q}$)	4.5	50			19	30		38		45	ns
		4.5	150			23	36		45		54	ns
t_{PZL} t_{PZH}	3 State Output Enable Time	4.5	50	R_L = 1 KΩ		19	30		38		45	ns
		4.5	150	R_L = 1 KΩ		23	36		45		54	ns
t_{PZL} t_{PZH}	3 State Output Disable Time	4.5	50	R_L = 1 KΩ		18	25		31		38	ns
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (LE)	4.5	50			7	15		19		22	ns
t_s	Minimum Set-up Time	4.5	50			4	10		13		15	ns
t_h	Minimum Hold Time	4.5	50				5		5		5	ns
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{OUT}	Output Capacitance					10						pF
C_{PD} (*)	Power Dissipation Capacitance					51						pF

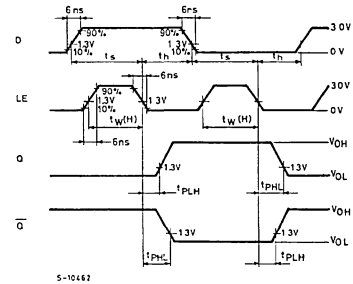
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Flip-Flop)

SWITCHING CHARACTERISTICS TEST WAVEFORM

t_{PLH}, t_{PHL} (D - Q)



t_{PLH}, t_{PHL} (LE - Q, $\overline{Q}$)
t_s, t_h, t_w

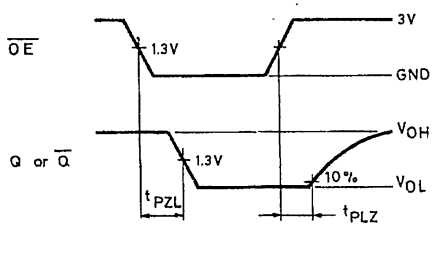


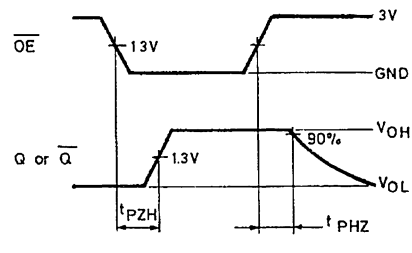
t_{PLZ}, t_{PZL}

The 1KΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputsand GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{OE}$ input is held low.

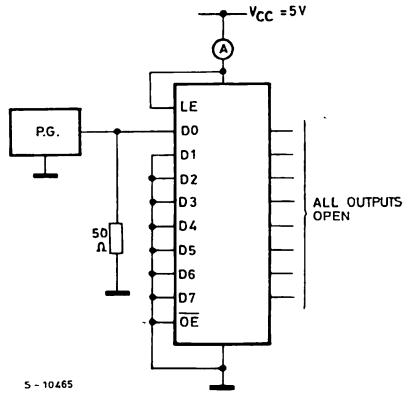
t_{PHZ}, t_{PZH}

The 1KΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{OE}$ input is held low.





TEST CIRCUIT I_{CC} (Opr.)



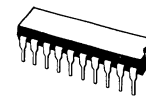
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

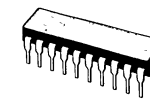
M54/74HC564
M54/74HC574

OCTAL D-TYPE FLIP FLOP WITH 3 STATE OUTPUT
HC564 INVERTING - HC574 NON INVERTING

- HIGH SPEED
  f_{MAX} = 62 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $I_{OL} = |I_{OH}|$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS564/574



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

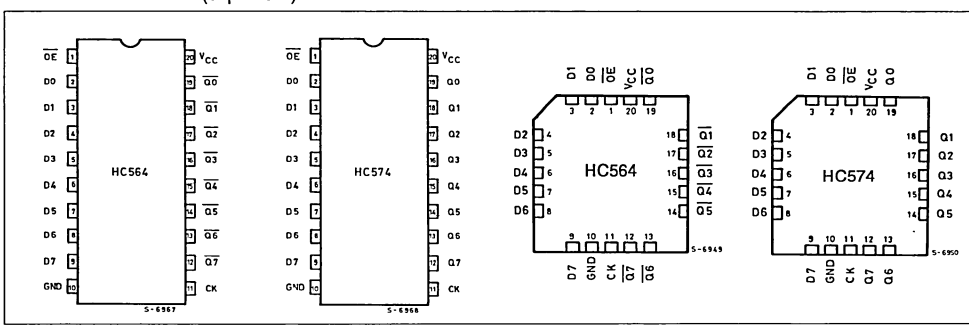
M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

DESCRIPTION

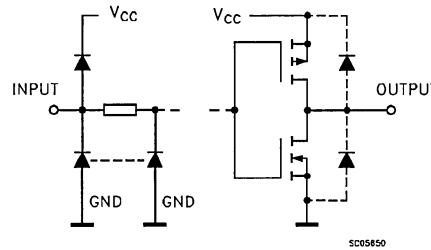
The M54/74HC564 and M54HC574 are high speed CMOS OCTAL D-TYPE FLIP FLOP WITH 3-STATE OUTPUTS fabricated with in silicon gate C^2MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power comsuption. These8-bit D-type flip-flops are controlled by a clock input (CK) and an ouput enable input ($\overline{OE}$). On the positive transition of the clock, the Q outputs will be set to the logic state that were setup at the D inputs (HC574) or their complements (HC564).

While the $\overline{OE}$ input is low, the eight outputs will be in a normal logic state (high or low logic level), and while high level, the outputs will be in a high impedance state. The output control does not affect the internal operation of flip-flops. That is, the old data can be retained or the new data can be entered even while the outputs are off. The application engineer has a choice of combination of inverting and non-inverting outputs. The 3-state output configuration and the wide choice of outline make bus-organized systems simple. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION (top view)



INPUT AND OUTPUT EQUIVALENT CIRCUIT



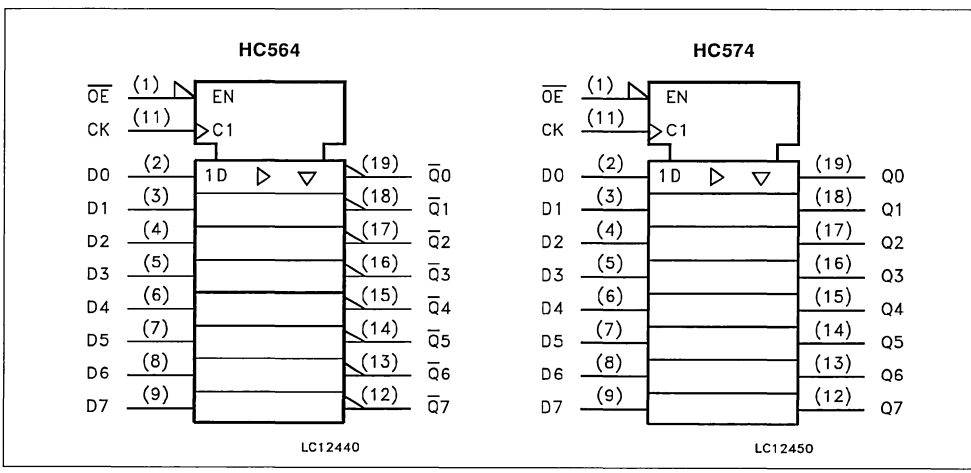
PIN DESCRIPTION (HC564)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State output Enable Input (Active LOW)
2, 3, 4, 5, 6, 7, 8, 9, 10	D0 to D7	Data Inputs
12, 13, 14, 15, 16, 17, 18, 19	$\overline{Q0}$ to $\overline{Q7}$	3 State outputs
11	CLOCK	Clock Input (LOW to HIGH, edge triggered)
10	GND	Ground (0V)
20	Vcc	Positive Supply Voltage

PIN DESCRIPTION (HC574)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State output Enable Input (Active LOW)
2, 3, 4, 5, 6, 7, 8, 9, 10	D0 to D7	Data Inputs
12, 13, 14, 15, 16, 17, 18, 19	Q0 to Q7	3 State outputs
11	CLOCK	Clock Input (LOW to HIGH, edge triggered)
10	GND	Ground (0V)
20	Vcc	Positive Supply Voltage

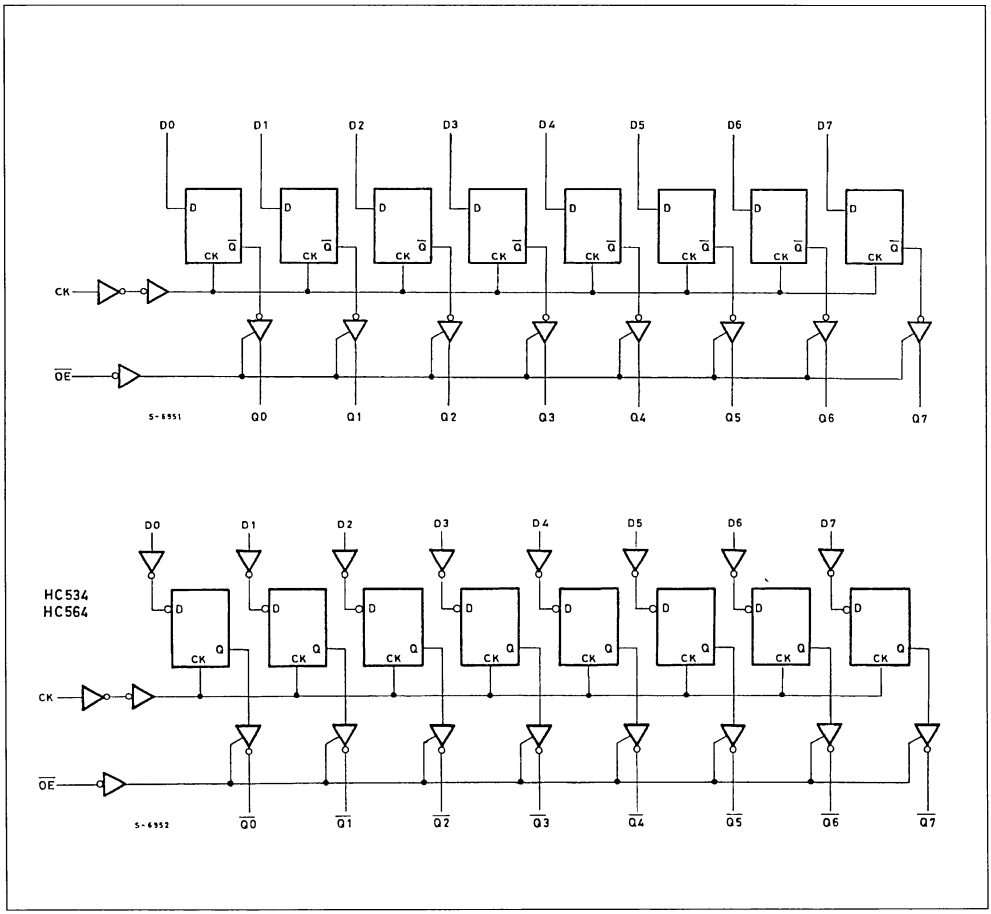
IEC LOGIC SYMBOLS



TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q (HC574)	$\overline{Q}$ (HC564)
H	X	X	Z	Z
L	⌐	X	NO CHANGE	NO CHANGE
L	⌐	L	L	H
L	⌐	H	H	L

LOGIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series		-55 to +125	°C
	M74HC Series		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5.0		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

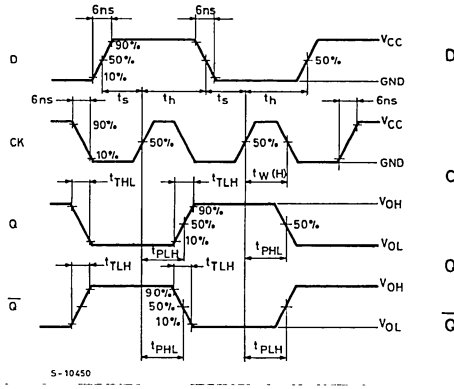
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q, $\overline{Q}$)	2.0	50			70	150		190		225	ns
		4.5				20	30		38		45	
		6.0				15	26		32		38	
		2.0	150			88	190		240		285	ns
		4.5				25	38		48		57	
		6.0				19	32		41		48	
t_{PZL} t_{PZH}	3 State Output Enable Time	2.0	50	R_L = 1 KΩ		48	125		155		190	ns
		4.5				15	25		31		38	
		6.0				12	21		26		32	
		2.0	150	R_L = 1 KΩ		60	165		205		250	ns
		4.5				20	33		41		50	
		6.0				16	28		35		43	
t_{PLZ} t_{PHZ}	3 State Output Disable Time	2.0	50	R_L = 1 KΩ		34	125		155		190	ns
		4.5				17	25		31		38	
		6.0				15	21		26		32	
f_{MAX}	Maximum CLock Frequency	2.0	50		6.2	18		5		4.2		ns
		4.5			31	75		25		21		
		6.0			37	90		30		25		
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CLOCK)	2.0	50			15	75		95		110	ns
		4.5				6	15		19		22	
		6.0				6	13		16		19	
t_s	Minimum Set-up Time	2.0	50			25	75		95		110	ns
		4.5				6	15		19		22	
		6.0				4	13		16		19	
t_h	Minimum Hold Time	2.0	50				0		0		0	ns
		4.5					0		0		0	
		6.0					0		0		0	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{OUT}	Out put Capacitance					10						pF
C_{PD} (*)	Power Dissipation Capacitance					54						pF

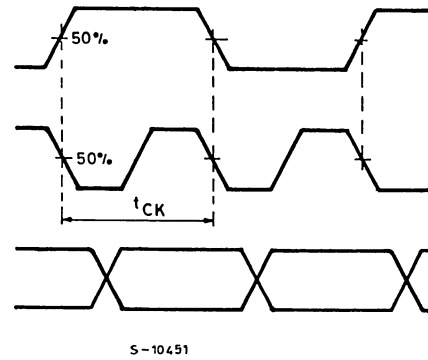
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

t_{PLH}, t_{PHL}, t_S, t_h, t_W



f_{MAX}

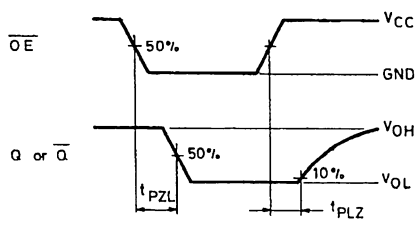


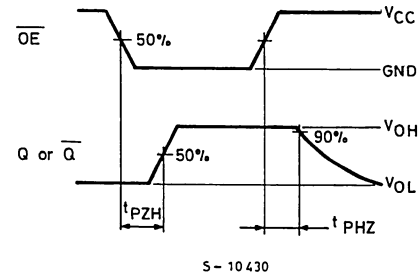
t_{PLZ}, t_{PZL}

The 1KΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputsand GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{OE}$ input is held low.

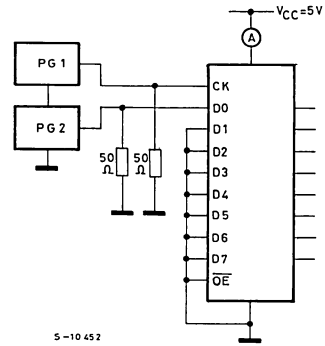
t_{PHZ}, t_{PZH}

The 1KΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{OE}$ input is held low.





TEST CIRCUIT I_{CC} (Opr.)

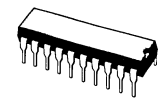


INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

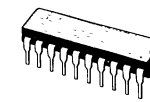
M54/74HCT564
M54/74HCT574

OCTAL D-TYPE FLIP FLOP WITH 3 STATE OUTPUT
HCT564 INVERTING - HCT574 NON INVERTING

- HIGH SPEED
  f_{MAX} = 62 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $I_{OL} = |I_{OH}|$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS564/574



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

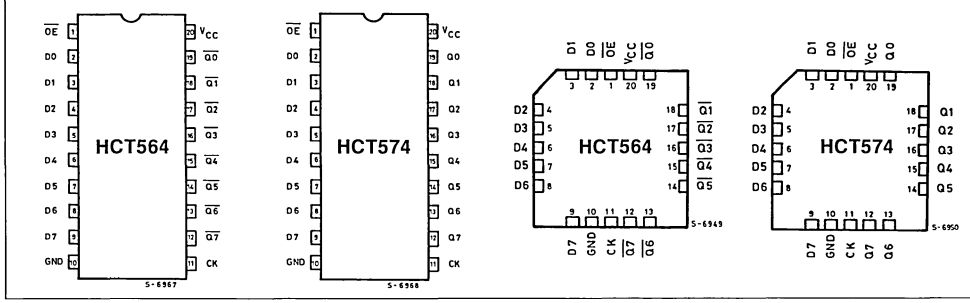
M54HCTXXXF1R M74HCTXXXM1R
M74HCTXXXB1R M74HCTXXXC1R

DESCRIPTION

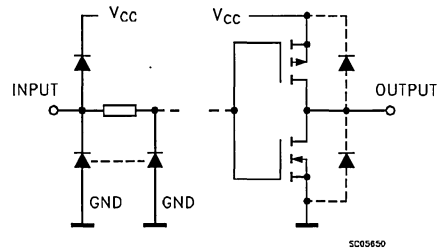
The M54/74HCT564 and M54HCT574 are high speed CMOS OCTAL D-TYPE FLIP FLOP WITH 3-STATE OUTPUTS fabricated in silicon gate C^2MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power comsuption. These 8-bit D-type flip-flops are controlled by a clock input (CK) and an ouput enable input ($\overline{OE}$). On the positive transition of the clock, the Q outputs will be set to the logic state that were setup at the D inputs (HCT574) or their complements (HCT564).

While the $\overline{OE}$ input is low, the eight outputs will be in a normal logic state (high or low logic level), and while high level, the outputs will be in a high impedance state. The output control does not affect the internal operation of flip-flops. That is, the old data can be retained or the new data can be entered even while the outputs are off. The application engineer has a choice of combination of inverting and non-inverting outputs. The 3-state output configuration and the wide choice of outline make bus-organized systems simple. All inputs are equipped with protection circuits against static discharge and transient excess voltage. This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

PIN CONNECTION (top view)



INPUT AND OUTPUT EQUIVALENT CIRCUIT



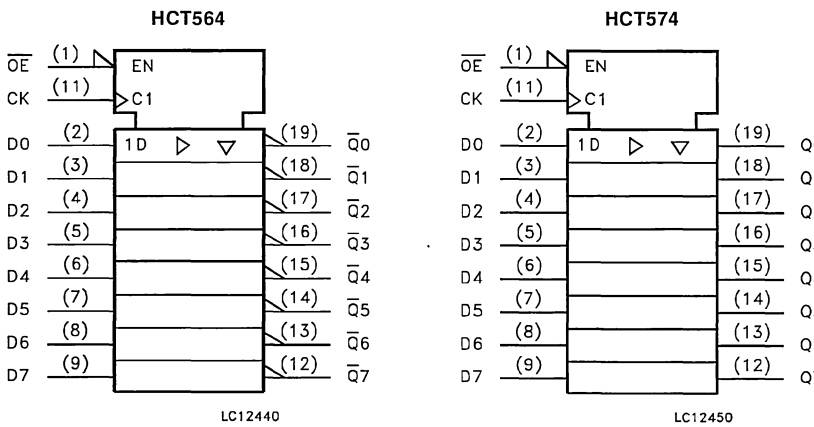
PIN DESCRIPTION (HCT564)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State output Enable Input (Active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0 to D7	Data Inputs
12, 13, 14, 15, 16, 17, 18, 19	$\overline{Q0}$ to $\overline{Q7}$	3 State outputs
11	CLOCK	Clock Input (LOW to HIGH, edge triggered)
10	GND	Ground (0V)
20	Vcc	Positive Supply Voltage

PIN DESCRIPTION (HCT574)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State output Enable Input (Active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0 to D7	Data Inputs
12, 13, 14, 15, 16, 17, 18, 19	Q0 to Q7	3 State outputs
11	CLOCK	Clock Input (LOW to HIGH, edge triggered)
10	GND	Ground (0V)
20	Vcc	Positive Supply Voltage

IEC LOGIC SYMBOLS

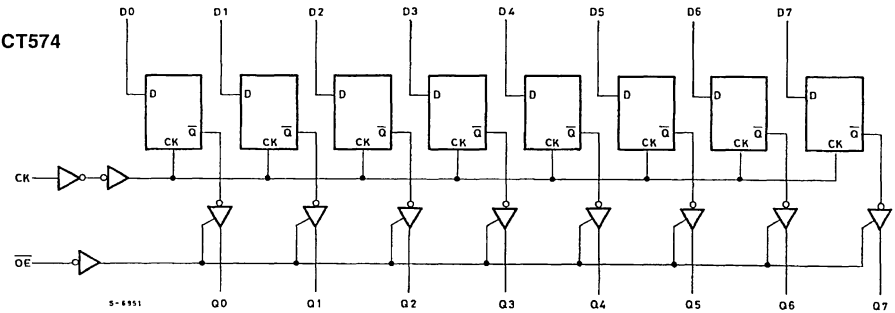


TRUTH TABLE

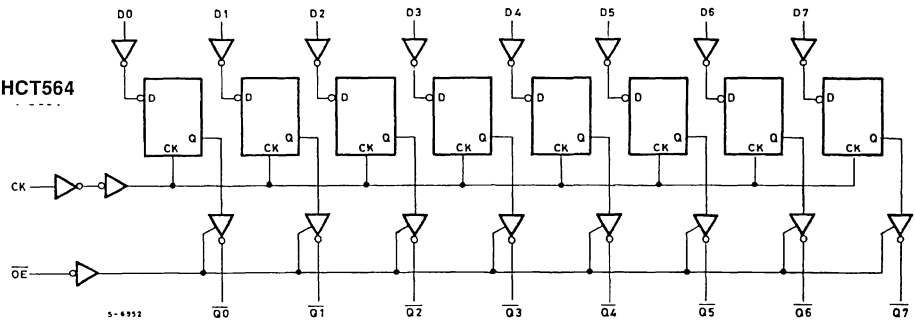
INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q (HCT574)	$\overline{Q}$ (HCT564)
H	X	X	Z	Z
L	⌐	X	NO CHANGE	NO CHANGE
L	⌐	L	L	H
L	⌐	H	H	L

LOGIC DIAGRAMS

HCT574



HCT564



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

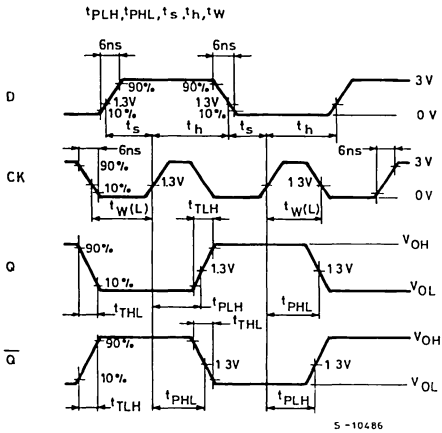
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-6.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 6.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				4		40		80	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9		3.0	mA

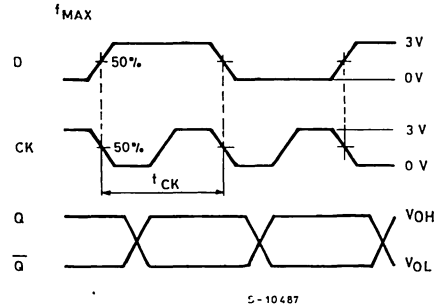
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5	50			7	12		15		18	ns
t_{PLH} t_{PHL}	Propagation Delay Time	4.5	50			20	30		38		45	ns
		4.5	150			24	36		45		54	
t_{PZL} t_{PZH}	3 State Output Enable Time	4.5	50	R_L = 1 KΩ		19	30		38		45	ns
		4.5	150	R_L = 1 KΩ		23	36		45		54	
t_{PLZ} t_{PHZ}	3 State Output Disable Time	4.5	50	R_L = 1 KΩ		19	30		38		45	ns
f_{MAX}	Maximum CLock Frequency	4.5	50		31	50		25		21		ns
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CLOCK)	4.5	50			8	15		19		22	ns
t_s	Minimum Set-up Time	4.5	50			7	15		19		22	ns
t_h	Minimum Hold Time	4.5	50				0		0		0	ns
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{OUT}	Out put Capacitance					10						pF
C_{PD} (*)	Power Dissipation Capacitance		HCT564 HCT574			67 63						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$ (per Flip-Flop)

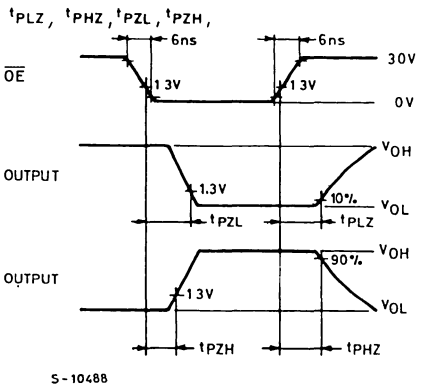
SWITCHING CHARACTERISTICS TEST WAVEFORM

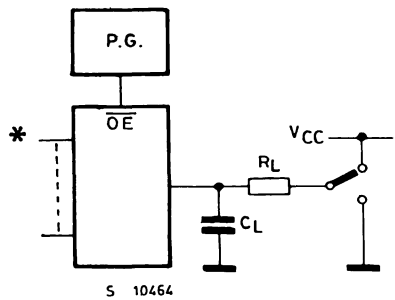




CLOCK DUTY : 50%

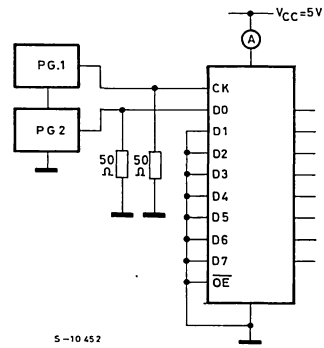
$$f_{MAX} = \frac{1}{T_{CK}}$$





EACH FLIP-FLOP SHALL BE SET HIGH WHEN SWITCH IS CONNECTED TO GND LINE AND IT SHALL BE SET LOW WHEN SWITCH IS CONNECTED TO V_{CC} LINE.

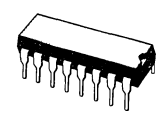
TEST CIRCUIT I_{CC} (Opr.)



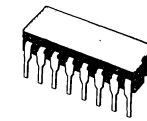
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

8 BIT BINARY COUNTER REGISTER (3 STATE)

- HIGH SPEED
  f_{MAX} = 62 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS (for RCO)
  15 LSTTL LOADS (for QA ~ QH)
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.) FOR QA ~ QH OUTPUT
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.) FOR RCO OUTPUT
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS590



B1R
(Plastic Package)



F1R
(Ceramic Package)

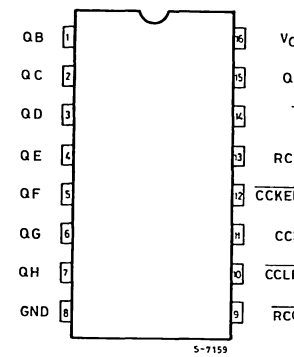
M1R
(Micro Package)

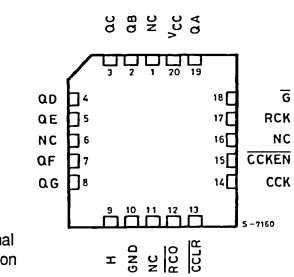
C1R
(Chip Carrier)

ORDER CODES :

M54HC590F1R M74HC590M1R
M74HC590B1R M74HC590C1R

PIN CONNECTIONS (top view)





NC =
No Internal
Connection

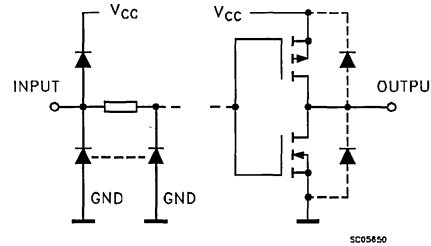
DESCRIPTION

The M54/74HC590 is a high speed CMOS 8-BIT BINARY COUNTER REGISTER (3-STATE) fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

These devices each contain an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features a direct clear input $\overline{CCLR}$ and a count enable input $\overline{CCKEN}$. For cascading, a ripple carry output $\overline{RCO}$ is provided. Expansion is easily accomplished by tying $\overline{RCO}$ of the first stage to $\overline{CCKEN}$ of the second stage, etc. Both the counter and register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the counter state will always be one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



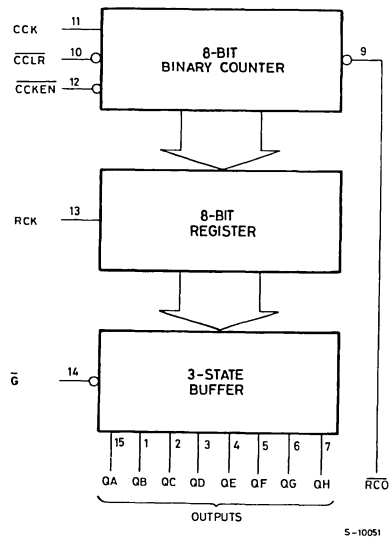
TRUTH TABLE

INPUTS					OUTPUT
$\overline{G}$	RCK	$\overline{CCLR}$	$\overline{CCKEN}$	CCK	
H	X	X	X	X	Q OUTPUTS DISABLE
L	X	X	X	X	Q OUTPUTS ENABLE
X	⌐	X	X	X	COUNTER DATA IS STORED INTO REGISTER
X	⌐	X	X	X	REGISTER STATE IS NOT CHANGED
X	X	L	X	X	COUNTER CLEAR
X	X	H	L	⌐	ADVANCE ONE COUNT
X	X	H	L	⌐	NO COUNT
X	X	H	H	X	NO COUNT

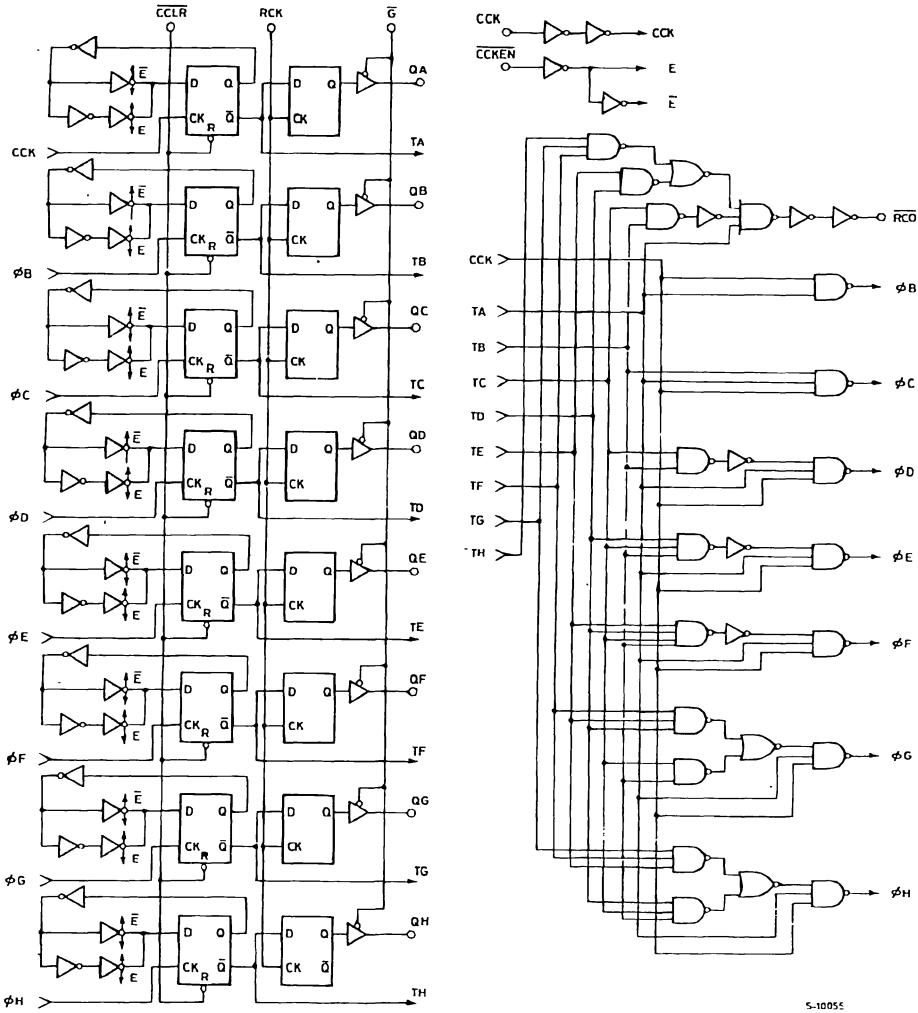
X: DON'T CARE

$\overline{RCO} = \overline{QA' \bullet QB' \bullet QC' \bullet QD' \bullet QE' \bullet QF' \bullet QG' \bullet QH'}$ (QA' to QH': INTERNAL OUTPUTS OF THE COUNTER)

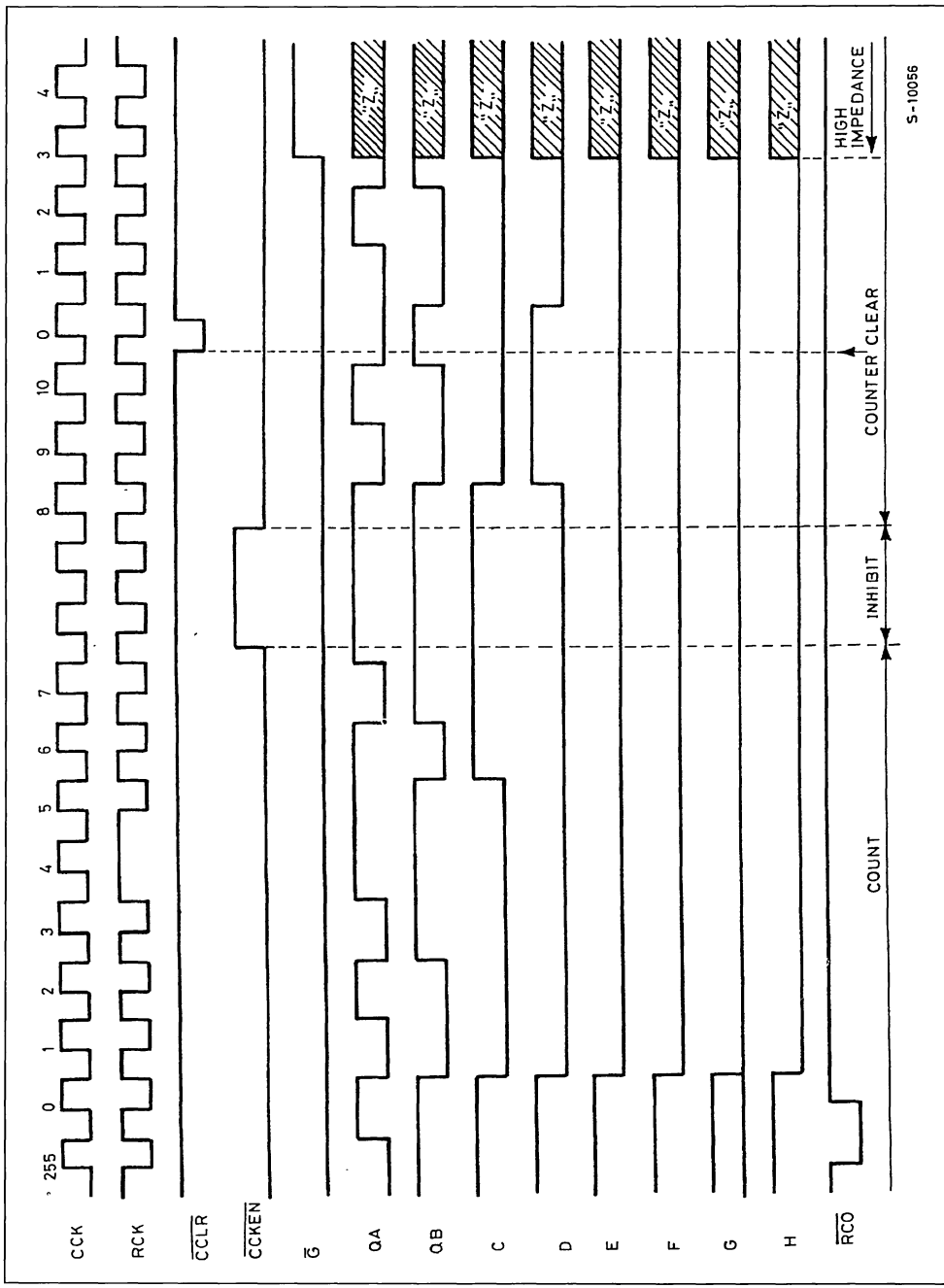
LOGIC DIAGRAM



LOGIC DIAGRAM



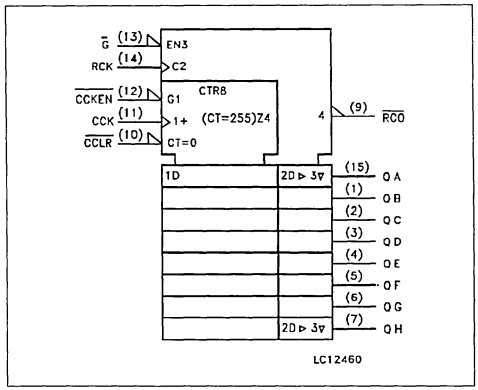
TIMING CHART



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 15	QA to QH	Outputs
11	CCK	Counter Clock Input
12	$\overline{CCKEN}$	Counter Clock Enable Input
13	RCK	Register Clock Input
9	$\overline{RCO}$	Ripple Carry Output
14	G	Output Enable Input
10	$\overline{CCLR}$	Counter Clear Input
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin (RCO) (Q_A - Q_H)	± 25 ± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage.		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage (for RCO output)	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OH}	High Level Output Voltage (for QA to QH outputs)	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage (for RCO output)	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
V_{OL}	Low Level Output Voltage (for QA to QH outputs)	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_O = V_{CC} or GND				±0.5		±5		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

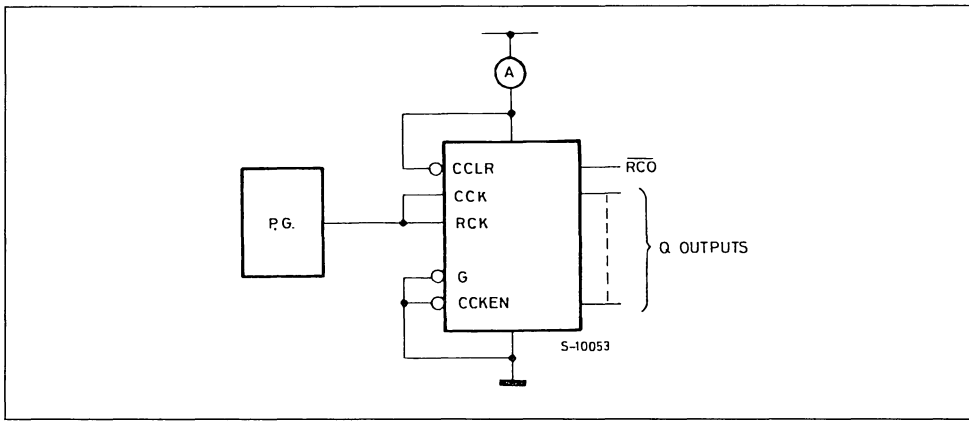
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time (Qn)	2.0	50			25	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t_{TLH} t_{THL}	Output Transition Time ($\overline{RCO}$)	2.0	50			30	75		95		115	ns
		4.5				8	15		19		23	
		6.0				7	13		16		20	
t_{PLH} t_{PHL}	Propagation Delay Time (CCK - $\overline{RCO}$)	2.0	50			56	165		205		250	ns
		4.5				19	33		41		50	
		6.0				16	28		35		43	
t_{PLH}	Propagation Delay Time ($\overline{CCLR}$ - $\overline{RCO}$)	2.0	50			53	175		220		265	ns
		4.5				21	35		44		53	
		6.0				18	30		37		45	
t_{PLH} t_{PHL}	Propagation Delay Time (RCK - Q)	2.0	50			48	145		180		220	ns
		4.5				17	29		36		44	
		6.0				14	25		31		37	
		2.0	150			60	185		230		280	ns
		4.5				21	37		46		56	
		6.0				18	31		39		48	
t_{PZL} t_{PZH}	Output Enable Time	2.0	50	R_L = 1 KΩ		39	105		130		160	ns
		4.5				13	21		26		32	
		6.0				11	18		22		27	
		2.0	150	R_L = 1 KΩ		51	135		170		205	ns
		4.5				17	27		34		41	
		0				14	23		29		35	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0	50	R_L = 1 KΩ		28	105		130		160	ns
		4.5				14	21		26		32	
		6.0				12	18		22		27	
f_{MAX}	Maximum Clock Frequency	2.0	50		6.6	13		5.2		4.4		ns
		4.5			33	52		26		22		
		6.0			39	61		31		26		
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CCK, RCK)	2.0	50			36	100		125		145	ns
		4.5				9	20		25		29	
		6.0				8	17		21		25	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CCLR}$)	2.0	50			32	75		95		110	ns
		4.5				8	15		19		22	
		6.0				7	13		16		19	
t_s	Minimum Set-up Time ($\overline{CCKEN}$ - CCK)	2.0	50			44	100		125		150	ns
		4.5				11	20		25		30	
		6.0				9	17		21		26	

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

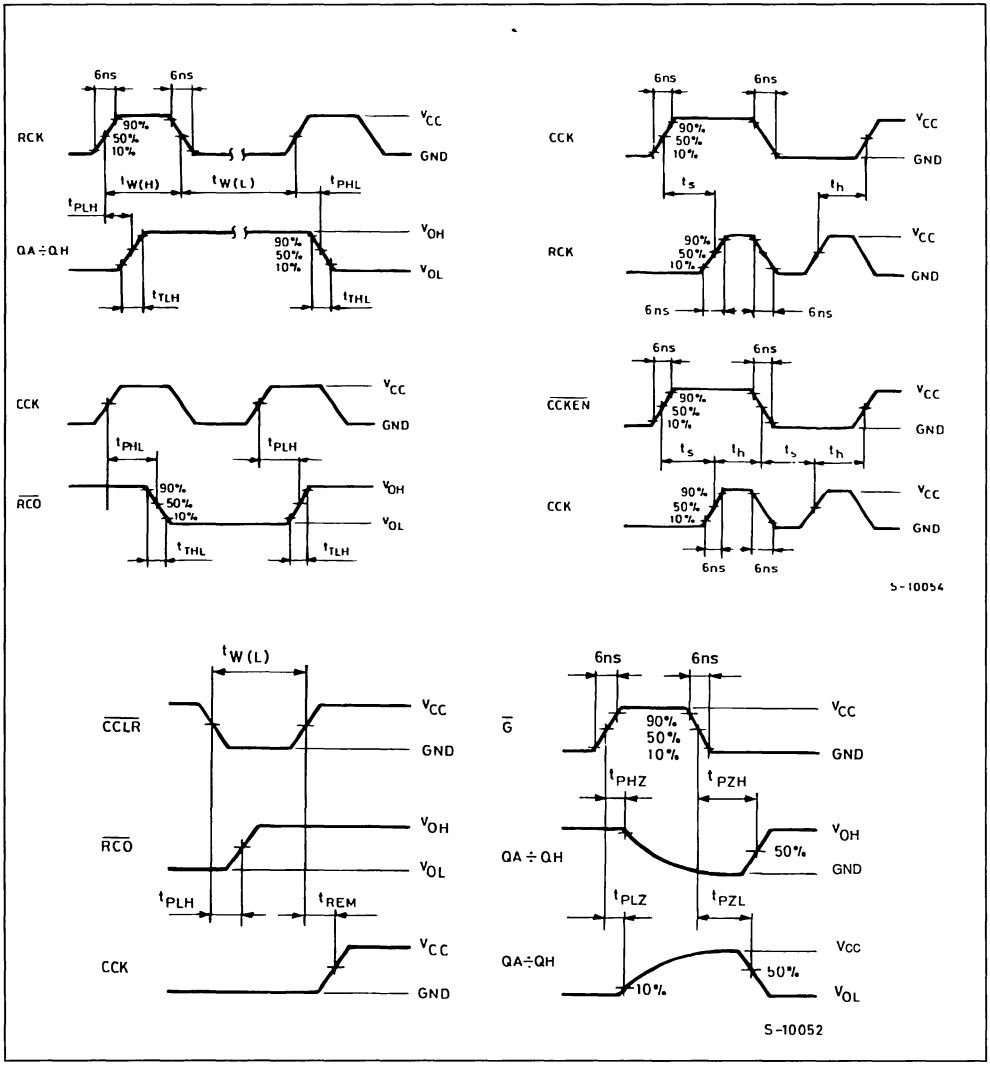
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$t_{s(H)}$	Minimum Set-up Time (CCK - RCK)	2.0	50			76	175		220		255	ns
		4.5				19	35		44		51	
		6.0				16	30		37		43	
t_h	Minimum Hold Time	2.0	50				0		0		0	ns
		4.5					0		0		0	
		6.0					0		0		0	
t_{REM}	Minimum Hold Time (CCLR)	2.0	50			28	75		95		110	ns
		4.5				7	15		19		22	
		6.0				6	13		16		19	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance					40						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit) Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

TEST WAVEFORM I_{CC} (Opr.)

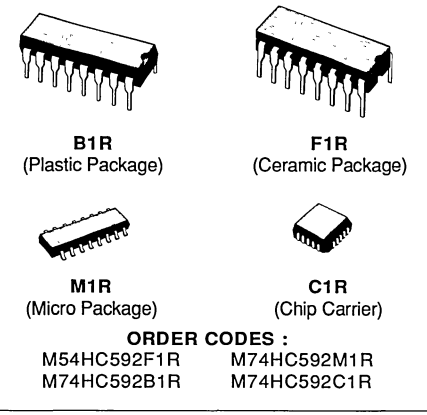


SWITCHING CHARACTERISTICS TEST WAVEFORM



8 BIT REGISTER BINARY COUNTER

- HIGH SPEED
  f_{MAX} = 35 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- SYMMETRICAL OUTPUT IMPEDANCE
  $I_{OL} = |I_{OH}| = 4$ mA (MIN.)
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL} = 28\ \% V_{CC}$ (MIN.)
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS592



B1R
(Plastic Package)

F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

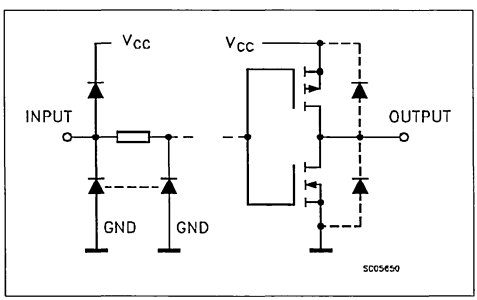
ORDER CODES :

M54HC592F1R M74HC592M1R
M74HC592B1R M74HC592C1R

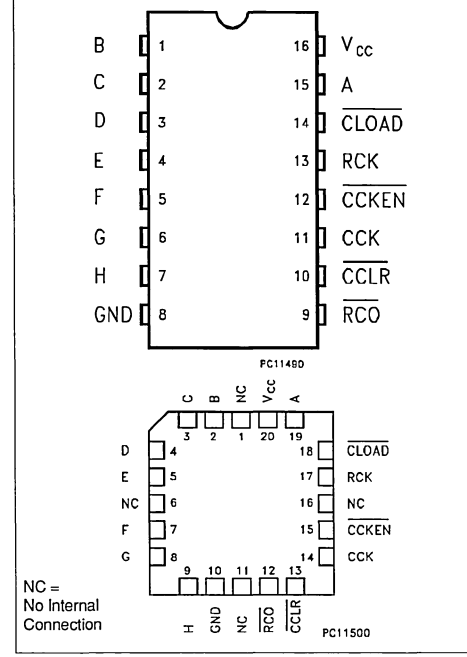
DESCRIPTION

The M54/74HC592 is a high speed CMOS 8 BIT REGISTER COUNTER fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
The M54/74HC592 is a parallel input, 8 bit storage register feeding an 8 bit binary counter. Both the register and the counter have individual positive edge triggered clock. In addition, the counter has direct load and clear functions. Expansion is easily accomplished by connecting $\overline{RCO}$ af the first stage to the count enable of the second stage. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



NC = No Internal Connection

TRUTH TABLE

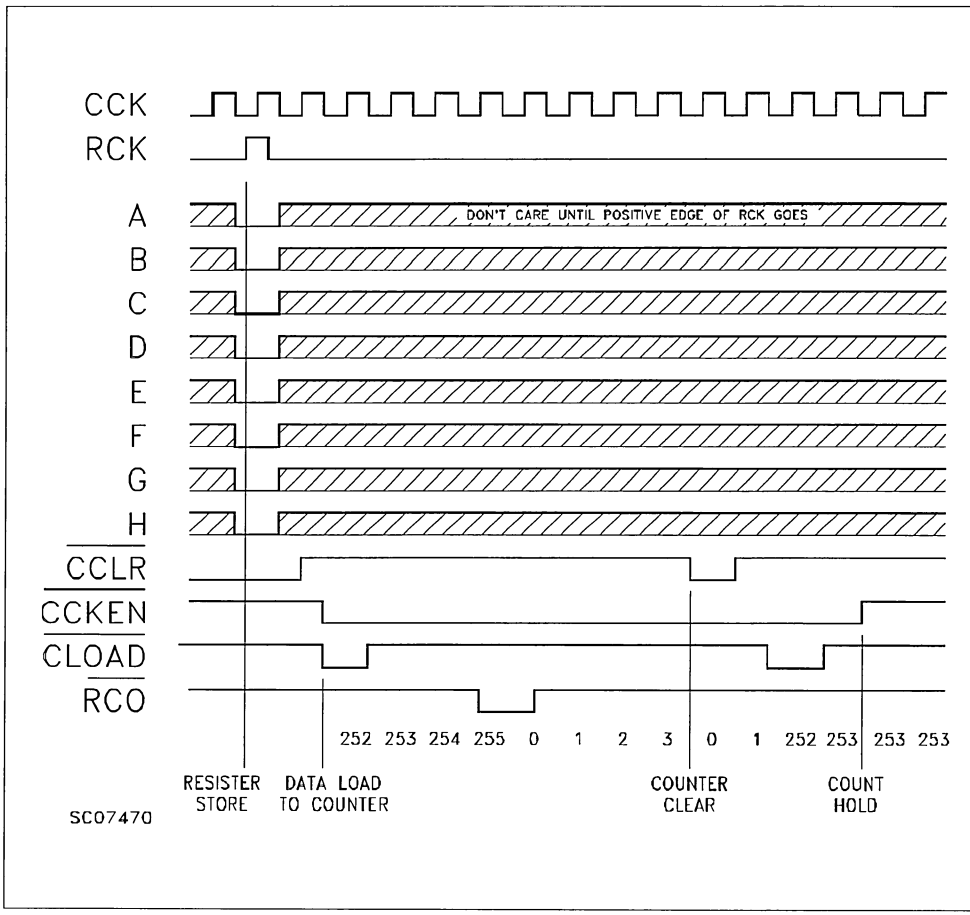
INPUTS					FUNCTION
RCK	$\overline{CLOAD}$	$\overline{CCLR}$	$\overline{CCKEN}$	CCK	
X	L	H	X	X	REGISTER DATA IS LOADED INTO COUNTER
X	H	L	X	X	COUNTER CLEAR
⎍	H	H	X	X	THE DATA OF A THRU H INPUTS IS STORED INTO REGISTER
⎎	H	H	X	X	REGISTER STATE IS NOT CHANGED
X	H	H	L	⎍	COUNTER ADVANCES THE COUNT
X	H	H	L	⎎	NO COUNT
X	H	H	H	X	NO COUNT

X: Don't Care

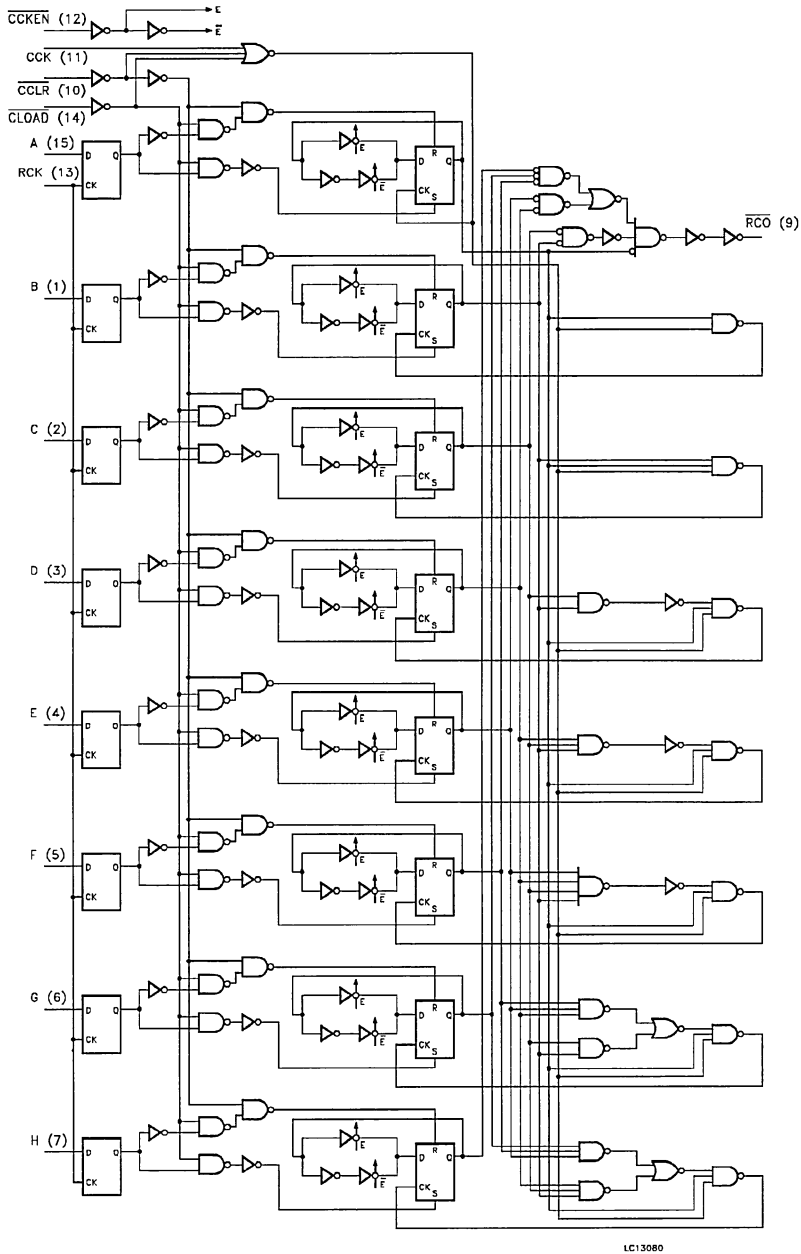
$RCO = \overline{QA' \bullet QB' \bullet QC' \bullet QD' \bullet QE' \bullet QF' \bullet QG' \bullet QH'}$

(QA' to QH': Internal outputs of the counter)

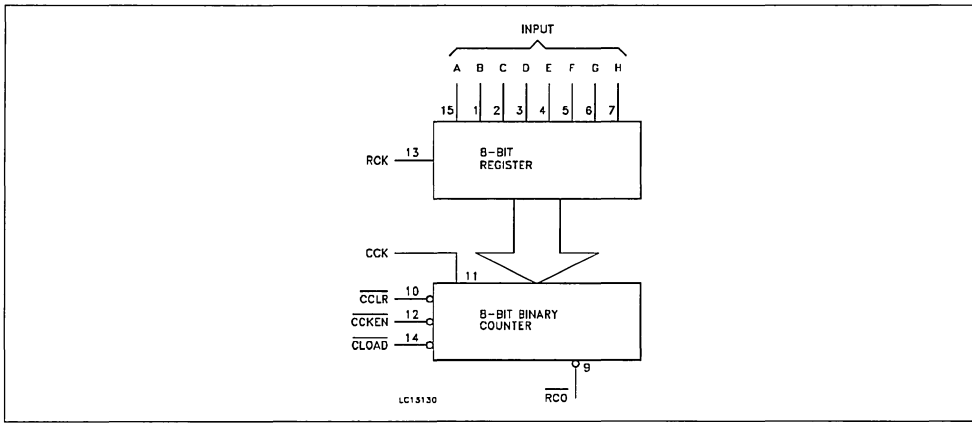
TIMING CHART



LOGIC DIAGRAM



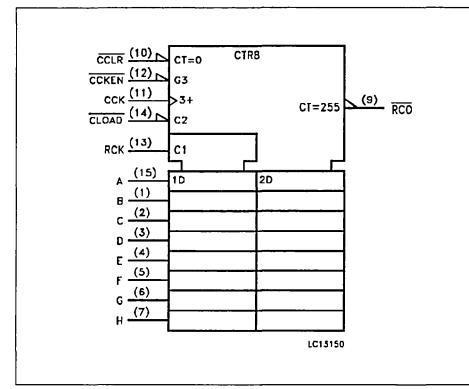
BLOCK DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1 to 7, 15	A to H	Data Inputs
9	$\overline{RCO}$	Ripple Counter Output
10	$\overline{CCLR}$	Counter Clear Input
11	CCK	Counter Clock Input
12	$\overline{CCKEN}$	Counter Clock Enable Input
13	RCK	Register Clock Input
14	$\overline{CLOAD}$	Counter Load Input
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

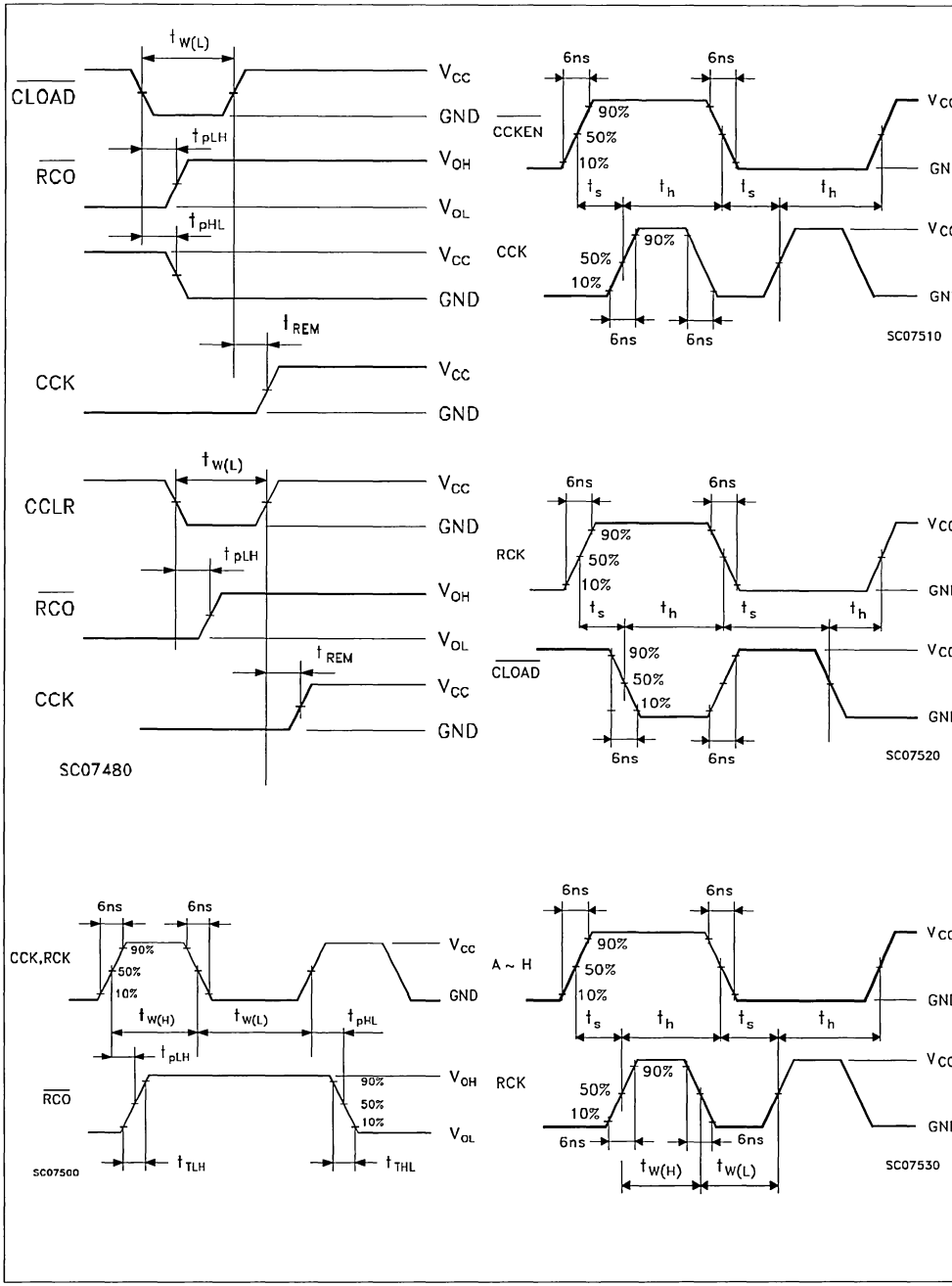
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

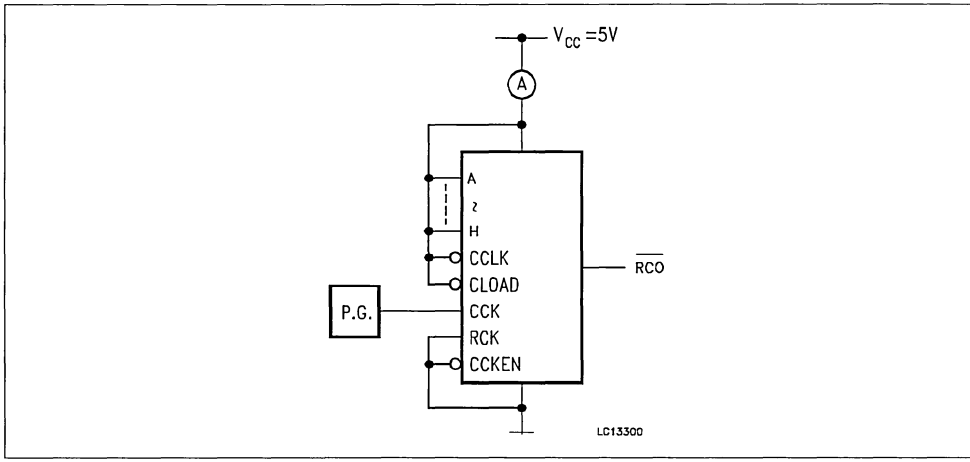
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CCK - $\overline{RCO}$)	2.0			63	165		205		250	ns
		4.5			21	33		41		50	
		6.0			18	28		35		43	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLOAD}$ - $\overline{RCO}$)	2.0			110	235		295		355	ns
		4.5			30	47		59		71	
		6.0			26	40		50		60	
t_{PHL}	Propagation Delay Time ($\overline{CCLR}$ - $\overline{RCO}$)	2.0			70	160		200		240	ns
		4.5			20	32		40		48	
		6.0			17	27		34		41	
t_{PLH} t_{PHL}	Propagation Delay Time (RCK - $\overline{RCO}$)	2.0			120	260		325		390	ns
		4.5			34	52		65		78	
		6.0			29	44		55		66	
f_{MAX}	Maximum Clock Frequency	2.0		5.4	11		4.4		3.6		MHz
		4.5		27	45		22		18		
		6.0		32	53		26		21		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width	2.0			40	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CCLR}$, $\overline{CLOAD}$)	2.0			40	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_s	Minimum Set-up Time ($\overline{CCKEN}$ - $\overline{CCK}$)	2.0			28	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
t_s	Minimum Set-up Time ($\overline{RCK}$ - $\overline{CLOAD}$) (A ... H - RCK)	2.0			40	100		125		145	ns
		4.5			10	20		25		29	
		6.0			9	17		21		25	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Minimum Removal Time	2.0			28	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				30						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit) Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

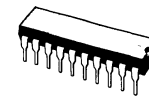


I_{CC} (Opr.) TEST CIRCUIT

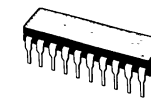


8 BIT BINARY COUNTER WITH INPUT REGISTER (3-STATE)

- HIGH SPEED
  f_{MAX} = 80 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS FOR $\overline{RCO}$
  15 LSTTL LOADS FOR Qn
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- SYMMETRICAL OUTPUT IMPEDANCE
  $I_{OL} = |I_{OH}|$ = 6 mA (MIN.) for Qn
  $I_{OL} = |I_{OH}|$ = 4 mA (MIN.) for $\overline{RCO}$
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS593



B1R
(Plastic Package)



F1R
(Ceramic Package)

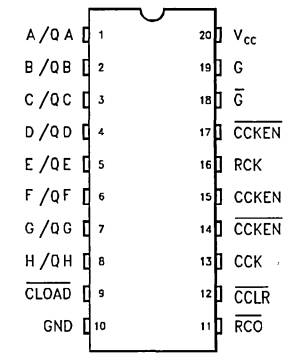
M1R
(Micro Package)

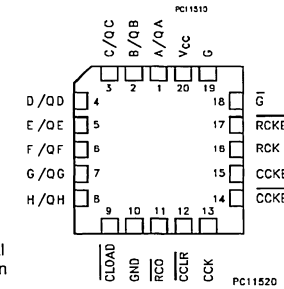
C1R
(Chip Carrier)

ORDER CODES :

M54HC593F1R M74HC593M1R
M74HC593B1R M74HC593C1R

PIN CONNECTIONS (top view)





NC = No Internal Connection

DESCRIPTION

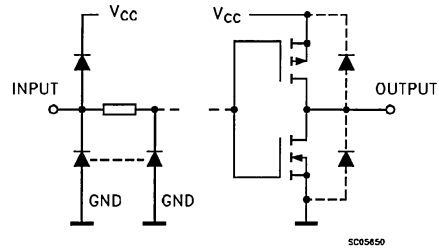
The M54/74HC593 is a high speed CMOS 8 BIT REGISTER COUNTER (3 STATE) fabricated with silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

The M54/74HC593 consists of a parallel input, 8 bit storage register feeding an 8 bit binary counter. Both the register and the counter have individual positive edge-triggered clock. In addition, the counter has direct load and clear functions. Expansion is easily accomplished by connecting $\overline{RCO}$ of first stage to the count enable $\overline{CCKEN}$, of the second stage etc.

The M54/74HC593 comes in a 20 pin package and has 3 state I/O, which provides parallel counter outputs.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



TRUTH TABLE

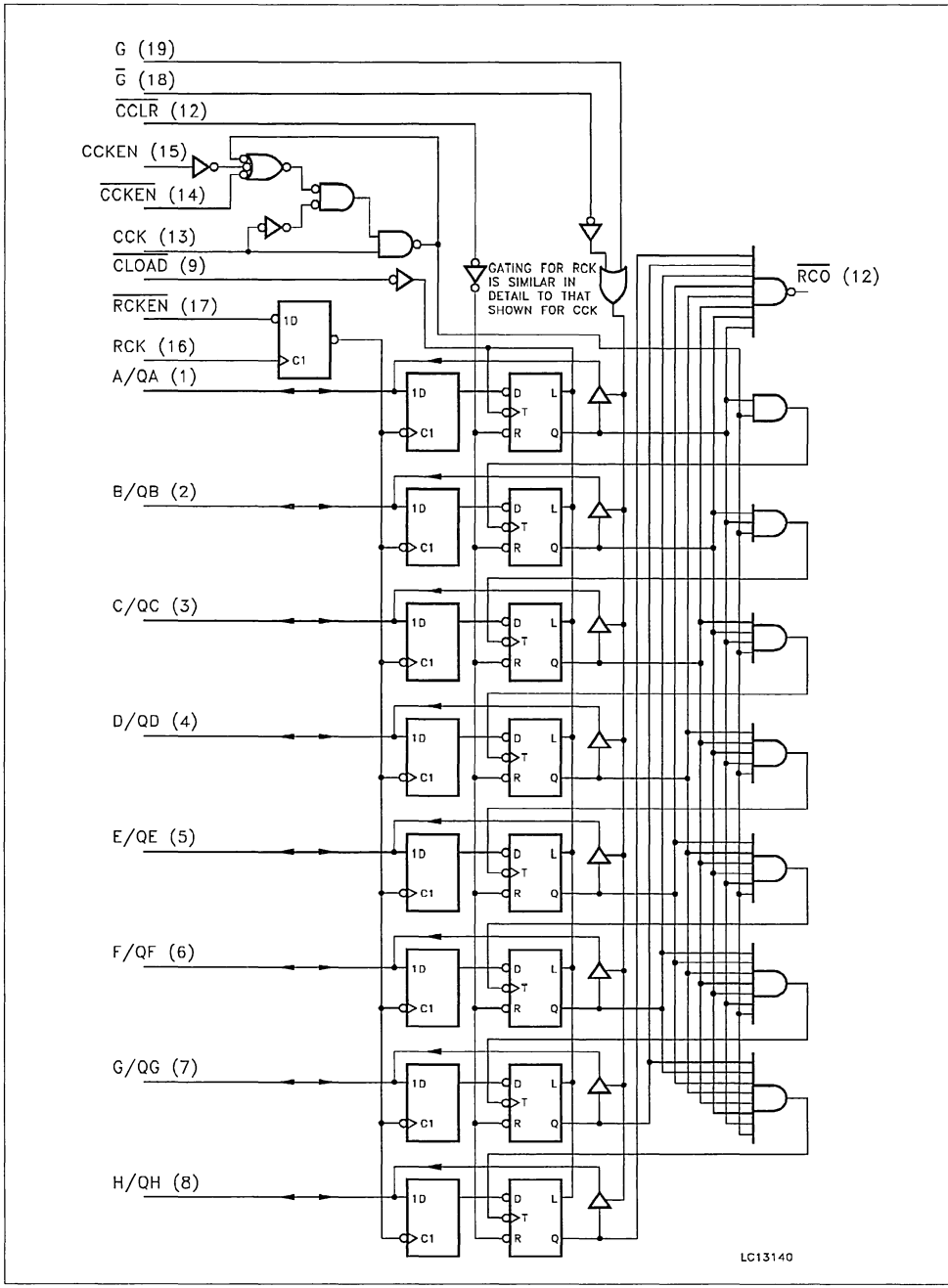
INPUTS									FUNCTION
G	$\overline{G}$	$\overline{CCLR}$	CCKEN	$\overline{CCKEN}$	CCK	$\overline{CLOAD}$	$\overline{RCKEN}$	RCK	
L	H	X	X	X	X	X	X	X	ALL Q BUS BECOME HIGH Z AND CAN BE APPLIED ANY DATA
H	X	X	X	X	X	X	X	X	THE OUTPUT DATA OF THE COUNTER IS ENABLE ON QA THRU QH
X	L	X	X	X	X	X	X	X	
X	X	L	X	X	X	H	X	X	COUNTER IS CLEARED TO ZERO
X	X	H	X	X	X	L	X	X	THE DATA OF Q BUS IS LOADED INTO COUNTER
X	X	H	H	X	⌐¬	H	X	X	COUNTER ADVANCES THE COUNT
X	X	H	X	L	⌐¬	H	X	X	
X	X	H	H	X	¬⌐	H	X	X	NO COUNT
X	X	H	X	L	¬⌐	H	X	X	
X	X	H	L	H	X	H	X	X	NO COUNT
X	X	X	X	X	X	X	H	X	REGISTER DATA IS NOT CHANGED
X	X	X	X	X	X	X	L	¬⌐ ⌐¬	REGISTER DATA IS NOT CHANGED
X	X	X	X	X	X	X	L		THE DATA OF Q BUS IS STORED INTO REGISTER

X: Don't Care

$\overline{RCO} = \overline{QA' \bullet QB' \bullet QC' \bullet QD' \bullet QE' \bullet QF' \bullet QG' \bullet QH'}$

(QA' to QH': Internal outputs of the counter)

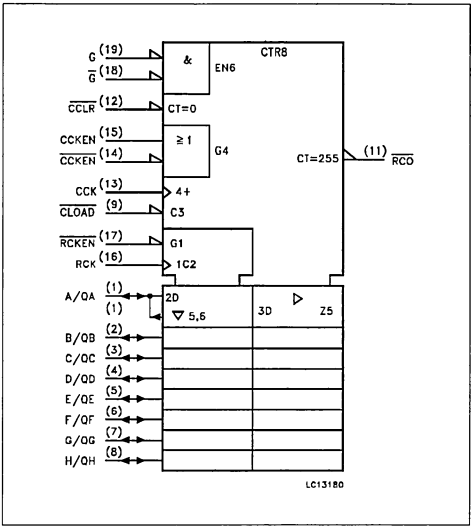
LOGIC DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 8	A/QA to H/QH	Binary Outputs
9	$\overline{CLOAD}$	Counter Clock Load Input
11	$\overline{RCO}$	Ripple Carry Output
12	$\overline{CCLR}$	Counter Clear Input
13	CCK	Counter Clock Input
14, 15	$\overline{CCKEN}$, CCKEN	Counter Clock Enable Inputs
16	RCK	Register Clock Input
17	$\overline{RCKEN}$	Register Clock Enable Input
18, 19	$\overline{G}$, G	Output Enable
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin ($\overline{RCO}$) (QA - QH)	± 20 ± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage (RCO)	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OH}	High Level Output Voltage (QA - QH)	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage (RCO)	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
V_{OL}	Low Level Output Voltage (QA - QH)	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5.0		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time (RCO)	2.0	50			30	75		95		110	ns
		4.5				8	15		19		22	
		6.0				7	13		16		19	
t_{TLH} t_{THL}	Output Transition Time (Qn)	2.0	50			20	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t_{PLH} t_{PHL}	Propagation Delay Time (CCK - Qn)	2.0	50			108	210		265		315	ns
		4.5				27	42		53		63	
		6.0				23	36		45		54	
		2.0	150			124	240		300		360	ns
		4.5				31	48		60		72	
		6.0				26	41		51		61	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLOAD}$ - Qn)	2.0	50			108	210		265		315	ns
		4.5				27	42		53		63	
		6.0				23	36		45		54	
		2.0	150			124	240		300		360	ns
		4.5				31	48		60		72	
		6.0				26	41		51		61	
t_{PHL}	Propagation Delay Time ($\overline{CCLR}$ - Qn)	2.0	50			112	220		275		330	ns
		4.5				28	44		55		66	
		6.0				24	37		47		56	
		2.0	150			128	250		315		375	ns
		4.5				32	50		63		75	
		6.0				27	43		54		64	
t_{PLH} t_{PHL}	Propagation Delay Time (CCK - $\overline{RCO}$)	2.0	50			144	250		315		375	ns
		4.5				36	50		63		75	
		6.0				31	10		54		64	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLOAD}$ - $\overline{RCO}$)	2.0	50			152	295		370		445	ns
		4.5				38	59		74		89	
		6.0				32	50		63		76	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CCLR}$ - $\overline{RCO}$)	2.0	50			116	225		280		340	ns
		4.5				29	45		56		68	
		6.0				25	38		48		58	
t_{PLH} t_{PHL}	Propagation Delay Time (RCK - $\overline{RCO}$)	2.0	50			188	360		450		540	ns
		4.5				47	72		90		108	
		6.0				40	61		77		93	
t_{PZL} t_{PZH}	3 State Output Enable Time	2.0	50	R_L = 1 KΩ		72	145		180		220	ns
		4.5				18	29		36		44	
		6.0				15	25		31		38	
		2.0	150	R_L = 1 KΩ		88	175		220		265	ns
		4.5				22	35		44		53	
		6.0				19	30		37		45	

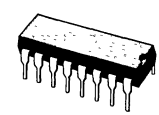
AC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLZ} t_{PHZ}	3 State Output Disable Time	2.0	50	R_L = 1 KΩ		80	140		175		210	ns
		4.5				22	28		35		42	
		6.0				17	24		30		36	
f_{MAX}	Maximum Clock Frequency	2.0	50		5.4	4		4.4		3.6		MHz
		4.5			27	17		22		18		
		6.0			32	20		26		21		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CCK, RCK)	2.0	50			44	100		125		150	ns
		4.5				11	20		25		30	
		6.0				9	17		21		26	
$t_{W(L)}$	Minimum Pulse Width $\overline{(CCLR, CLOAD)}$	2.0	50			40	100		125		150	ns
		4.5				10	20		25		30	
		6.0				9	17		21		26	
t_S	Minimum Set-up Time ($\overline{CCKEN}$, $\overline{CCKEN}$, CCK)	2.0	50			56	125		160		195	ns
		4.5				14	25		32		39	
		6.0				12	21		27		33	
t_S	Minimum Set-up Time $\overline{(RCKEN - RCK)}$	2.0	50			32	75		95		110	ns
		4.5				8	15		19		22	
		6.0				7	13		16		19	
$t_{S(H)}$	Minimum Set-up Time $\overline{(RCK - CLOAD)}$	2.0	50			56	125		160		195	ns
		4.5				14	25		32		39	
		6.0				12	21		27		33	
t_S	Minimum Set-up Time (A to H - RCK)	2.0	50			16	50		60		70	ns
		4.5				4	10		12		14	
		6.0				3	9		11		12	
t_h	Minimum Hold Time	2.0	50			0	0		0		0	ns
		4.5				0	0		0		0	
		6.0				0	0		0		0	
t_{REM}	Minimum Clear Remuval Time $\overline{(CCLR, CLOAD)}$	2.0	50				5				5	ns
		4.5					5		5		5	
		6.0					5		5		5	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance					19						pF

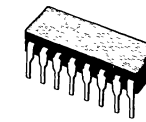
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

8 BIT SHIFT REGISTER WITH OUTPUT LATCHES (3 STATE)

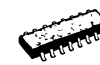
- HIGH SPEED
  f_{MAX} = 55 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS FOR QA TO QH
  10 LSTTL LOADS FOR QH'
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.) FOR QA TO QH
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.) FOR QH'
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH LSTTL 54/74LS595



B1R
(Plastic Package)



F1R
(Ceramic Package)



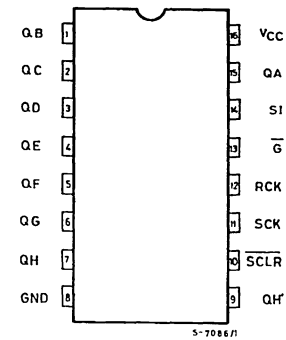
M1R
(Micro Package)

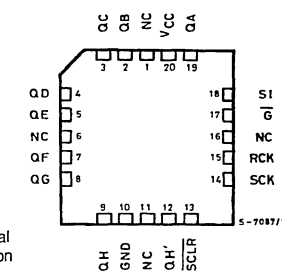
C1R
(Chip Carrier)

ORDER CODES :

M54HC595F1R M74HC595M1R
M74HC595B1R M74HC595C1R

PIN CONNECTIONS (top view)





NC = No Internal Connection

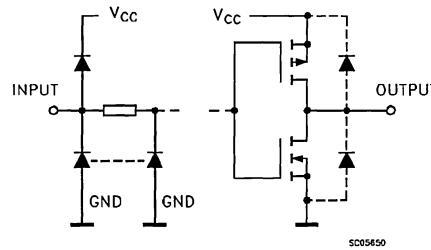
DESCRIPTION

The M54/74HC595 is a high speed CMOS 8-BIT SHIFT REGISTERS/OUTPUT LATCHES (3-STATE) fabricated in silicon C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has 8 3-STATE outputs. Separate clocks are provided for both the shift register and the storage register.

The shift register has a direct-overriding clear, serial input, and serial output (standard) pins for cascading. Both the shift register and storage register use positive-edge triggered clocks. If both clocks are connected together, the shift register state will always be one clock pulse ahead of the storage register.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT

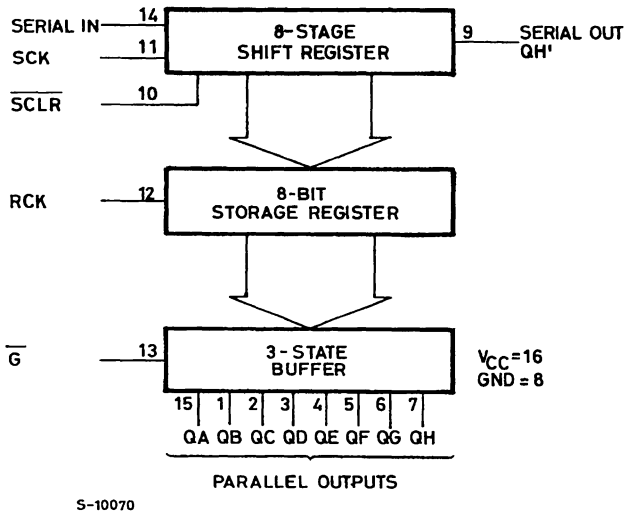


TRUTH TABLE

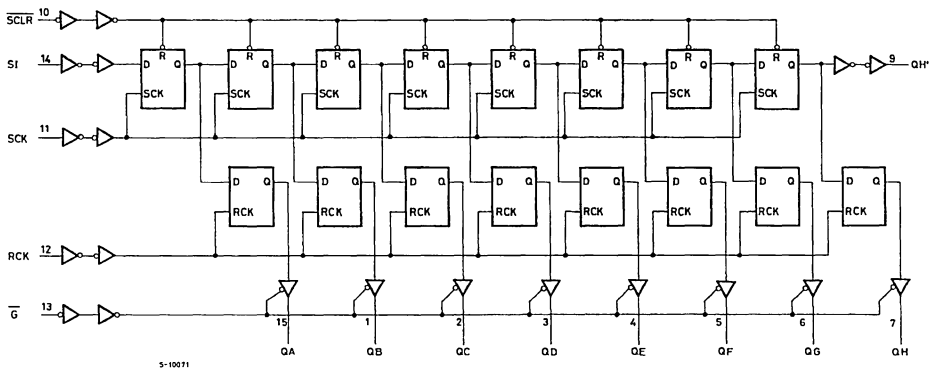
INPUTS					OUTPUT
SI	SCK	$\overline{SCLR}$	RCK	$\overline{G}$	
X	X	X	X	H	QA THRU QH OUTPUTS DISABLE
X	X	X	X	L	QA THRU QH OUTPUTS ENABLE
X	X	L	X	X	SHIFT REGISTER IS CLEARED
L	⌐	H	X	X	FIRST STAGE OF S.R. BECOMES "L" OTHER STAGES STORE THE DATA OF PREVIOUS STAGE, RESPECTIVELY
H	⌐	H	X	X	FIRST STAGE OF S.R. BECOMES "H" OTHER STAGES STORE THE DATA OF PREVIOUS STAGE, RESPECTIVELY
X	¬	H	X	X	STATE OF S.R IS NOT CHANGED
X	X	X	⌐	X	S.R. DATA IS STORED INTO STORAGE REGISTER
X	X	X	¬	X	STORAGE REGISTER STATE IS NOT CHANGED

X: DON'T CARE

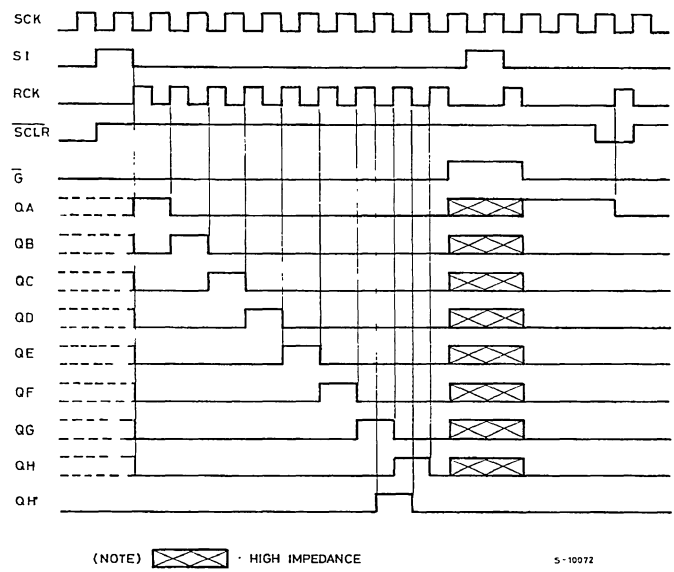
LOGIC DIAGRAM



LOGIC DIAGRAM



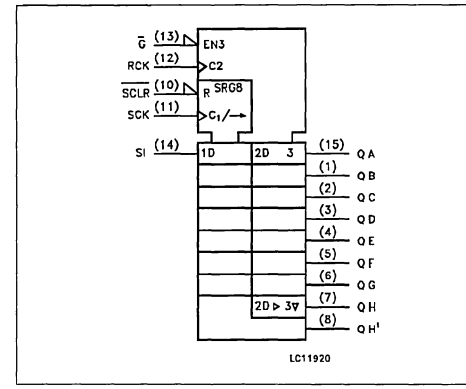
TIMING CHART



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 15	QA to QH	Data Outputs
9	QH'	Serial Data Outputs
10	$\overline{SCLR}$	Shift Register Clear Input
11	SCK	Shift Register Clock Input
13	$\overline{G}$	Output Enable Input
14	SI	Serial Data Input
12	RCK	Storage Register Clock Input
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current Per Output Pin QA-QH	± 35	mA
I_O	DC Output Current Per Output Pin QH'	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage (for QH' output)	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OH}	High Level Output Voltage (for QA to QH outputs)	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage (for QH' output)	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
V_{OL}	Low Level Output Voltage (for QA to QH outputs)	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

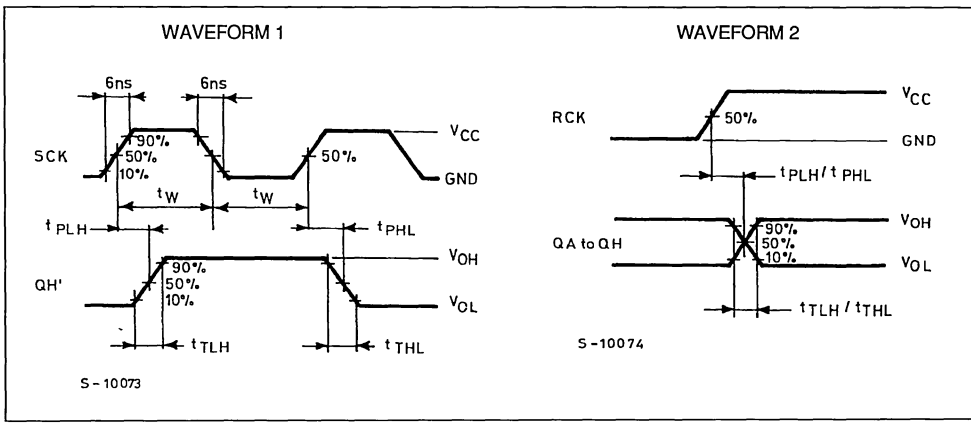
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time (Qn)	2.0	50			25	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t_{TLH} t_{THL}	Output Transition Time (QH')	2.0	50			30	75		95		115	ns
		4.5				8	15		19		23	
		6.0				7	13		16		20	
t_{PLH} t_{PHL}	Propagation Delay Time (SCK - QH')	2.0	50			45	125		155		190	ns
		4.5				15	25		31		38	
		6.0				13	21		26		32	
t_{PLH} t_{PHL}	Propagation Delay Time (SCLR - QH')	2.0	50			60	175		220		265	ns
		4.5				18	35		44		53	
		6.0				15	30		37		45	
t_{PLH} t_{PHL}	Propagation Delay Time (RCK - Qn)	2.0	50			60	150		190		225	ns
		4.5				20	30		38		45	
		6.0				17	26		32		38	
		2.0	150			75	190		240		285	ns
		4.5				25	38		48		57	
		6.0				22	32		41		48	
t_{PZL} t_{PZH}	3 State Output Enable Time	2.0	50	R_L = 1 KΩ		45	135		170		205	ns
		4.5				15	27		34		41	
		6.0				13	23		29		35	
		2.0	150	R_L = 1 KΩ		60	175		220		265	ns
		4.5				20	35		44		53	
		6.0				17	30		37		45	
t_{PLZ} t_{PHZ}	3 State Output Disable Time	2.0	50	R_L = 1 KΩ		30	150		190		225	ns
		4.5				15	30		38		45	
		6.0				14	26		32		38	
f_{MAX}	Maximum Clock Frequency	2.0	50		6.0	17		4.8		4		ns
		4.5			30	50		24		20		
		6.0			35	59		28		24		
		2.0	150		5.2	14		4.2		3.4		ns
		4.5			26	40		21		17		
		6.0			31	45		25		20		
$t_{W(H)}$	Minimum Pulse Width (SCK, RCK)	2.0	50			17	75		95		110	ns
		4.5				6	15		19		22	
		6.0				6	13		16		19	
$t_{W(L)}$	Minimum Pulse Width (SCLR)	2.0	50			20	75		95		110	ns
		4.5				6	15		19		22	
		6.0				6	13		16		19	
t_s	Minimum Set-up Time (SI - CCK)	2.0	50			25	50		65		75	ns
		4.5				5	10		13		15	
		6.0				4	9		11		13	

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

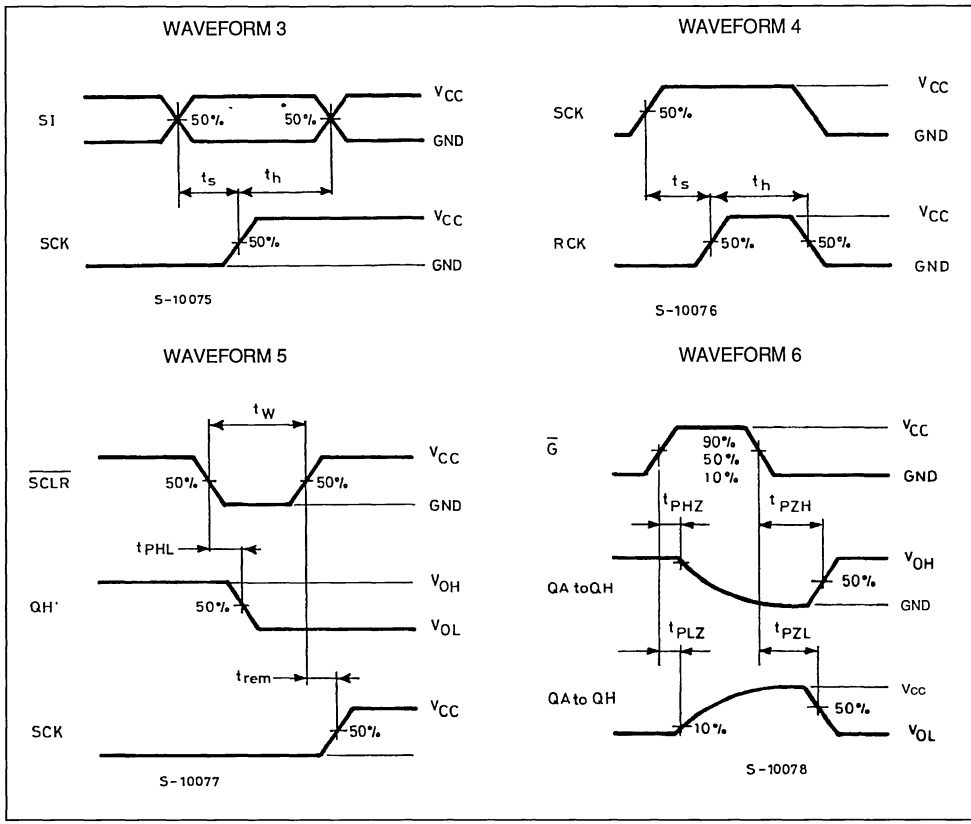
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_s	Minimum Set-up Time (SCK - RCK)	2.0	50			35	75		95		110	ns
		4.5				8	15		19		22	
		6.0				6	13		16		19	
t_s	Minimum Set-up Time (SCRL - RCK)	2.0	50			40	100		125		145	ns
		4.5				10	20		25		29	
		6.0				7	17		21		25	
t_h	Minimum Hold Time	2.0	50				0		0		0	ns
		4.5					0		0		0	
		6.0					0		0		0	
t_{REM}	Minimum Clear Remuval Time	2.0	50			15	50		65		75	ns
		4.5				3	10		13		15	
		6.0				3	9		11		13	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance					184						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

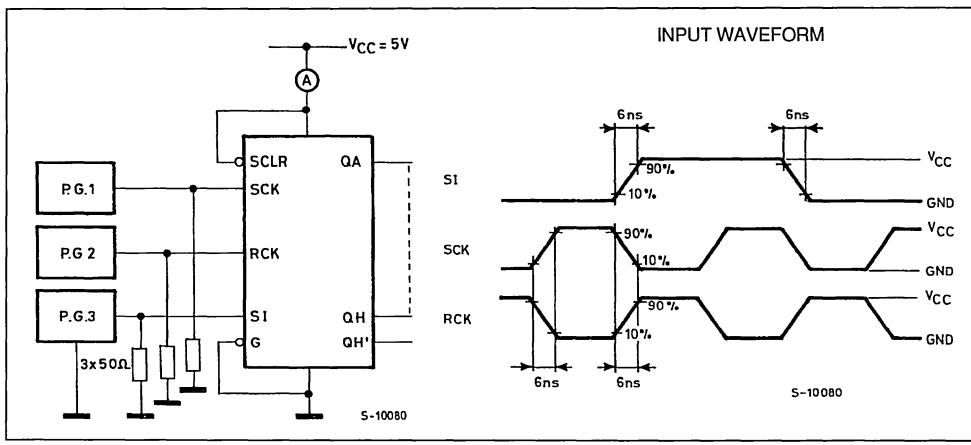
SWITCHING CHARACTERISTICS TEST WAVEFORM



SWITCHING CHARACTERISTICS TEST WAVEFORM (continued)

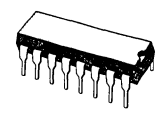


TEST CIRCUIT I_{CC} (Opr.)

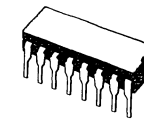


8 BIT LATCH/SHIFT REGISTER

- HIGH SPEED
  f_{MAX} = 60 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS597



B1R
(Plastic Package)



F1R
(Ceramic Package)

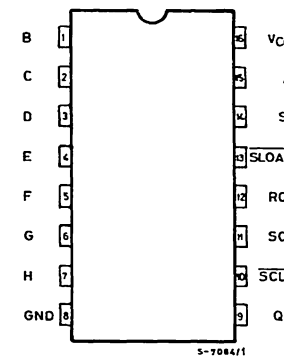
M1R
(Micro Package)

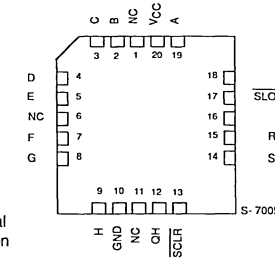
C1R
(Chip Carrier)

ORDER CODES :

M54HC597F1R M74HC597M1R
M74HC597B1R M74HC597C1R

PIN CONNECTIONS (top view)





NC =
No Internal
Connection

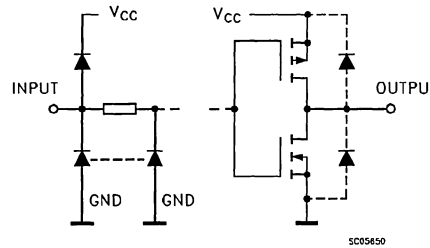
DESCRIPTION

The M54/74HC597 is a high speed CMOS 8-BIT LATCH/SHIFT REGISTER fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

This devices comes in a 16-pin package and consist of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.

All inputs are equipped with protection circuits against static discharge and transient voltage excess.

INPUT AND OUTPUT EQUIVALENT CIRCUIT

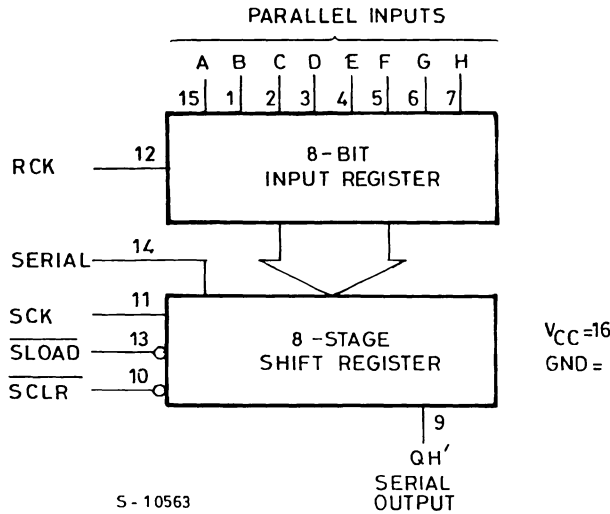


TRUTH TABLE

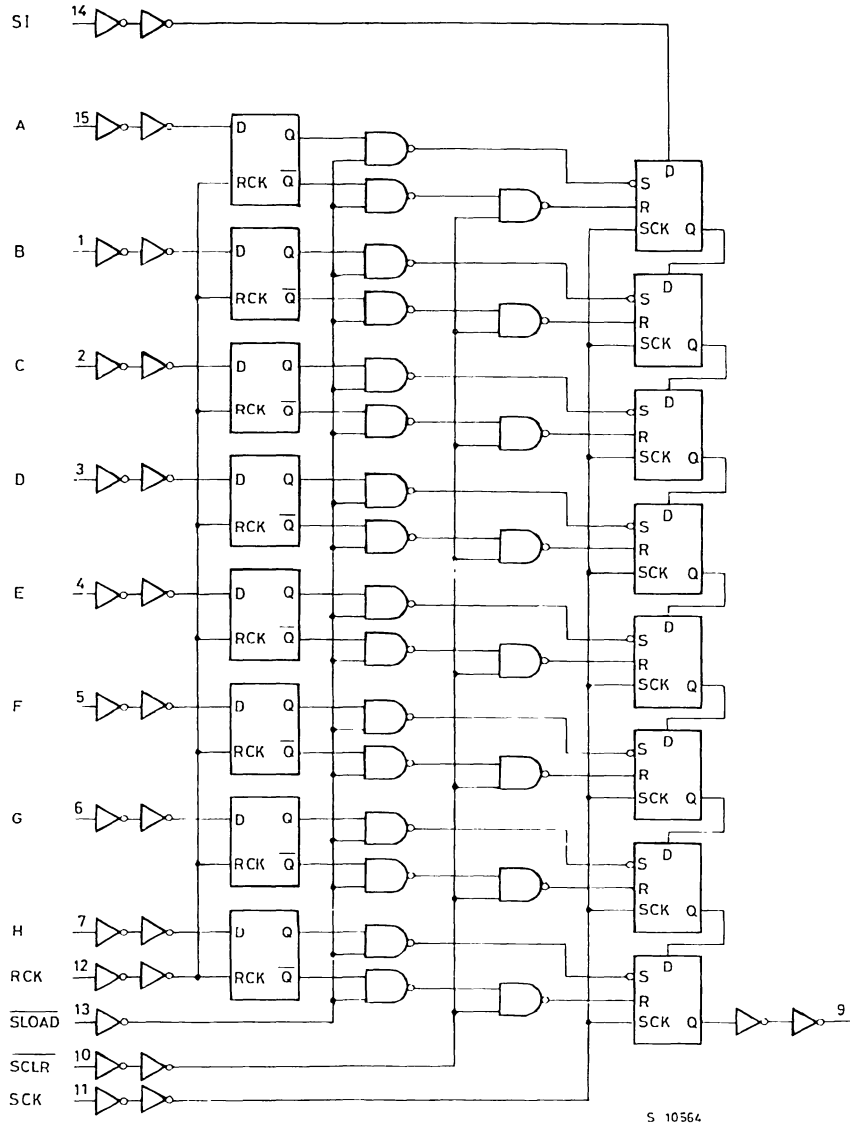
INPUTS					OUTPUT
SI	SCK	$\overline{SCLR}$	$\overline{SLOAD}$	RCK	
X	X	L	H	X	S.R. IS CLEARED TO "L"
X	X	H	L	X	INPTU REGISTER DATA IS STORED INTO S.R.
L	⌐	H	H	X	FIRST STAGE OF S.R. BECOMES "L" OTHER STAGES STORE THE DATA OF PREVIOUS STAGE, RESPECTIVELY
H	⌐	H	H	X	FIRST STAGE OF S.R. BECOMES "H" OTHER STAGES STORE THE DATA OF PREVIOUS STAGE, RESPECTIVELY
X	¬	H	H	X	STATE OF S.R IS NOT CHANGED
X	X	X	X	⌐	INPUT DATA ON A ~ H LINE IS STORED INTO INPUT REGISTER
X	X	X	X	¬	STORAGE REGISTER STATE IS NOT CHANGED

X: DON'T CARE

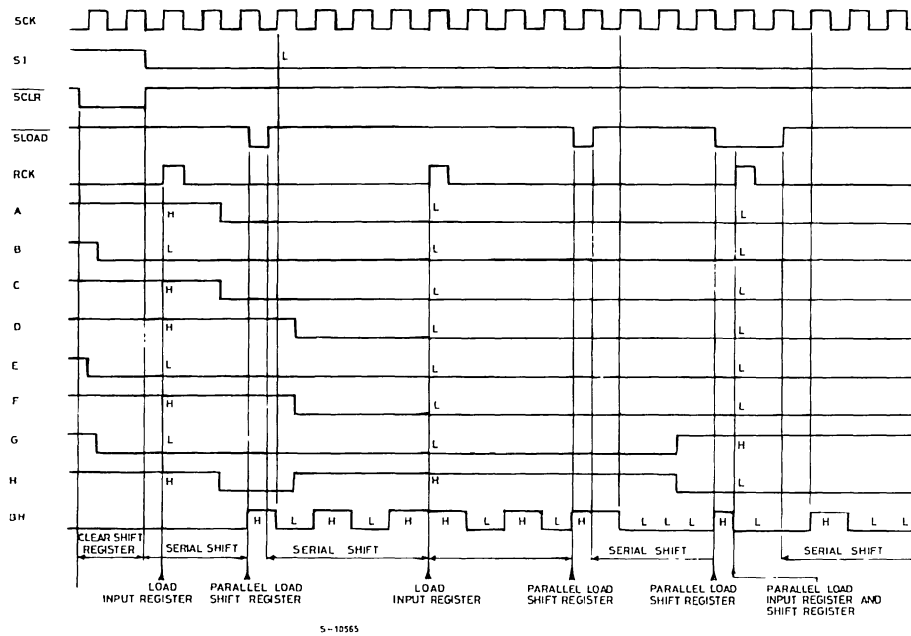
LOGIC DIAGRAM



LOGIC DIAGRAM



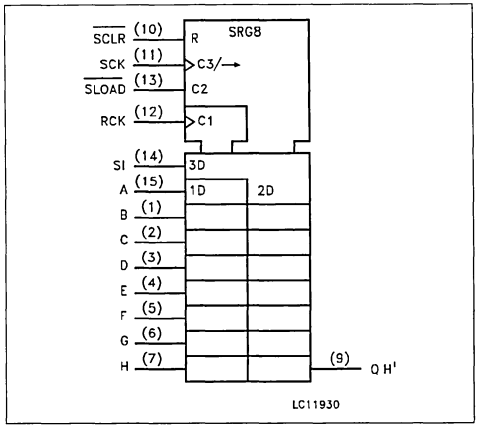
TIMING CHART



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
9	QH'	Serial Data Outputs
10	$\overline{SCLR}$	Asynchronous Reset Input (Active LOW)
11	SCK	Shift Clock Input (LOW to HIGH Edge-triggered)
12	RCK	Storage Clock Input (LOW to HIGH Edge-triggered)
13	$\overline{SLOAD}$	Parallel Data Input (Active LOW)
10	SI	Serial Data Input
15, 1, 2, 3, 4, 5, 6, 7	A to H	Parallel Data Inputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

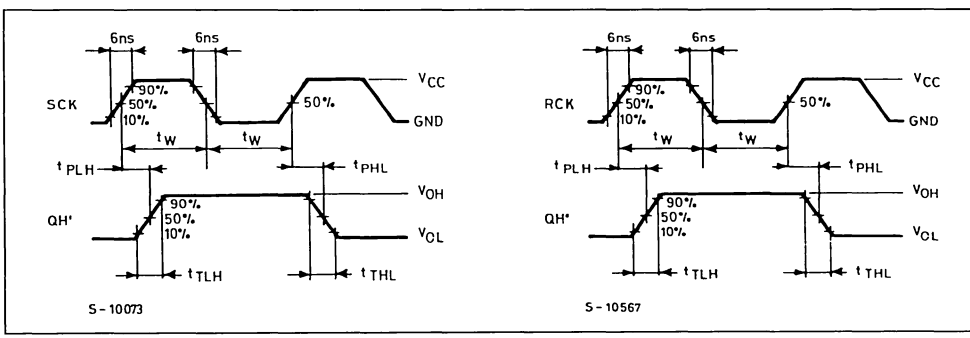
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		115	ns
		4.5			8	15		19		23	
		6.0			7	13		16		20	
t_{PLH} t_{PHL}	Propagation Delay Time (SCK - QH')	2.0			78	145		180		220	ns
		4.5			20	29		36		44	
		6.0			16	25		31		37	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{SCLR}$ - QH')	2.0			90	175		220		265	ns
		4.5			24	35		44		53	
		6.0			20	30		37		45	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{SLOAD}$ - QH')	2.0			80	175		220		265	ns
		4.5			22	35		44		53	
		6.0			18	30		37		45	
t_{PLH} t_{PHL}	Propagation Delay Time (RCK - QH')	2.0	$\overline{SLOAD}$ = "L"		112	210		265		315	ns
		4.5			30	42		53		63	
		6.0			24	36		45		54	

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

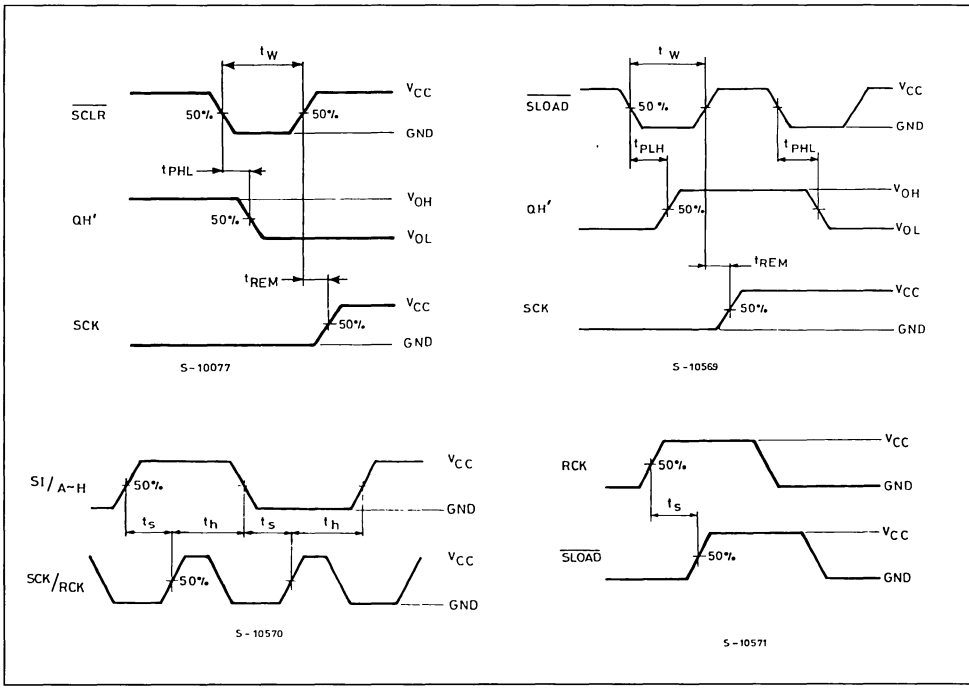
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}	Maximum Clock Frequency	2.0		6.0	12		4.8		4.0		ns
		4.5		30	48		24		20		
		6.0		35	50		28		24		
$t_{W(H)}$ $t_{W(L)}$	Propagation Delay Time (SCK, RCK)	2.0			20	75		95		110	ns
		4.5			7	15		19		22	
		6.0			4	13		16		19	
$t_{W(L)}$	Propagation Delay Time ($\overline{SCLR}$, $\overline{SLOAD}$)	2.0			25	75		95		110	ns
		4.5			7	15		19		22	
		6.0			5	13		16		19	
t_S	Minimum Set-up Time ($\overline{RCK}$ - $\overline{SLOAD}$)	2.0			48	100		125		150	ns
		4.5			12	20		25		30	
		6.0			10	17		21		26	
t_S	Minimum Set-up Time (SI, SCK)	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	
t_S	Minimum Set-up Time (PI - RCK)	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	
t_f	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Propagation Delay Time ($\overline{SCLR}$, $\overline{SLOAD}$)	2.0			12	75		95		115	ns
		4.5			4	15		19		23	
		6.0			3	13		16		20	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				60						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

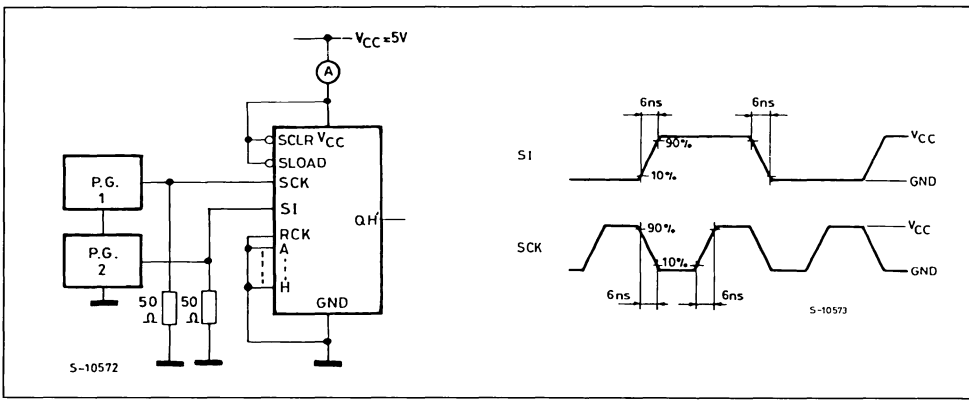
SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST WAVEFORM (continued)



TEST CIRCUIT Icc (Opr.)

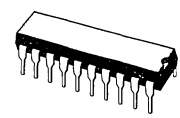


SGS-THOMSON MICROELECTRONICS

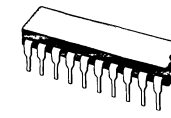
M54/74HC620
M54/74HC623

OCTAL BUS TRANSCEIVER
HC620 3 STATE INVERTING HC623 3 STATE NON INVERTING

- HIGH SPEED
  t_{PD} = 10 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V to 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH LS620/623



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

DESCRIPTION

The M54/74HC620/623 are high speed CMOS OCTAL BUS TRANSCEIVERS fabricated in silicon gate C^2MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption.

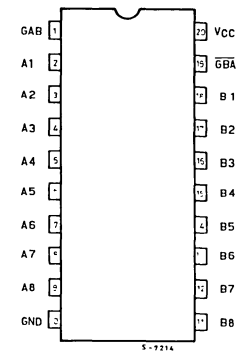
These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows maximum flexibility in timing.

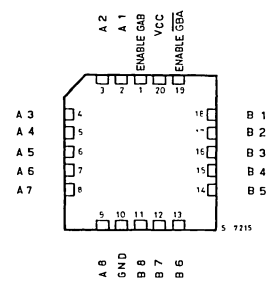
These devices allow data transmission from the A bus to B bus or from the B to the A bus depending upon the logic levels at the enable inputs ($\overline{GBA}$ and GAB). The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives these devices the capability to store data by simultaneous enabling of $\overline{GBA}$ and GAB.

Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 'HC623 or complementary for the 'HC620. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

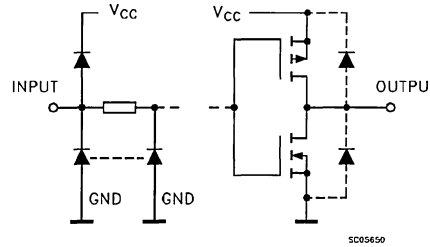
PIN CONNECTIONS (top view)





NC =
No Internal
Connection

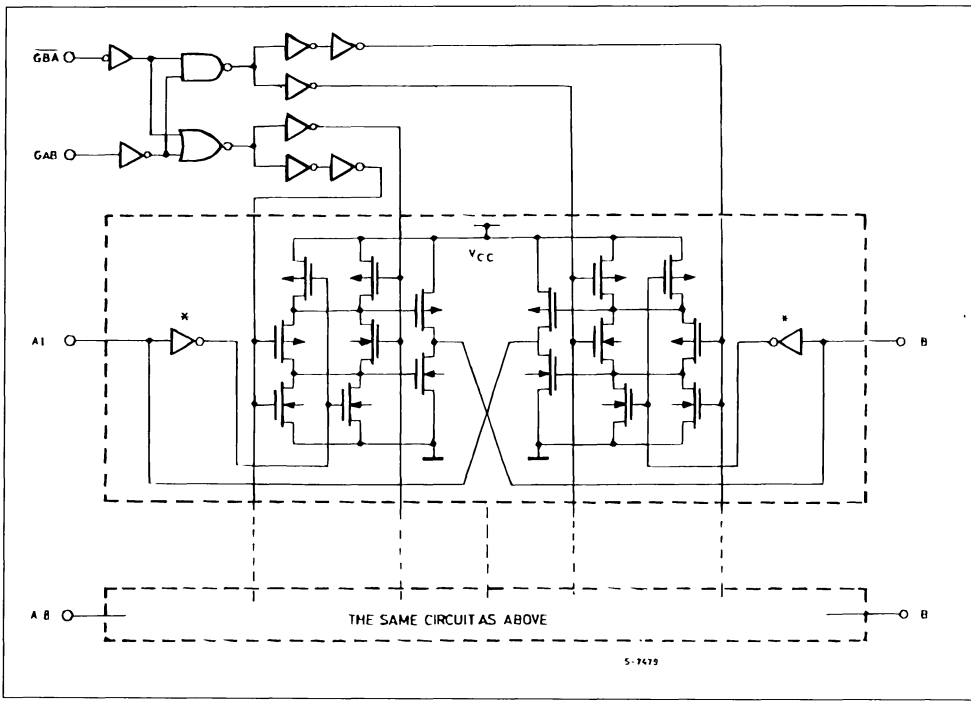
INPUT AND OUTPUT EQUIVALENT CIRCUIT



TRUTH TABLE

INPUTS		FUNCTION		OUTPUS	
GAB	$\overline{GBA}$	A Bus	B Bus	HC620	HC623
L	L	Output	Input	A = $\overline{B}$	A = B
H	H	Input	Output	B = $\overline{A}$	B = A
L	H	High Impedance		Z	Z
H	L	High Impedance		Z	Z

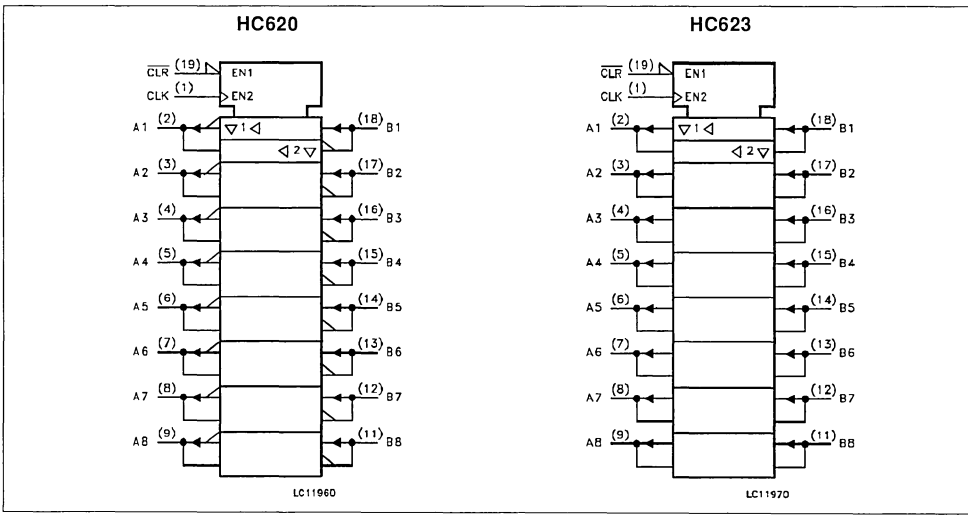
LOGIC DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 19	$\overline{GBA}$, GAB	Direction Controls
2, 3, 4, 5, 6, 7, 8, 9	A1 to A8	Data Inputs/Outputs
11, 12, 13, 14, 15, 16, 17, 18	B1 to B8	Data Inputs/Outputs
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur Functional operation under these condition is not implied
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C· 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

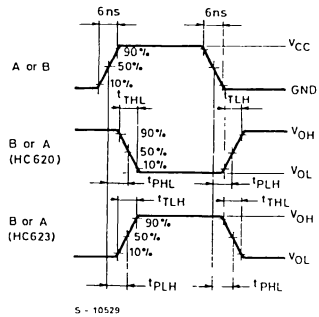
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

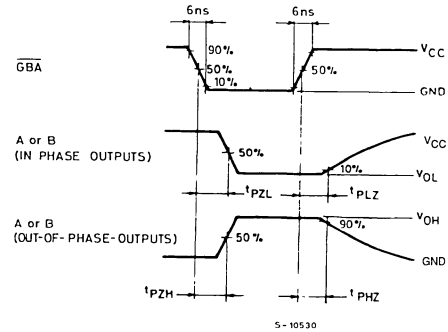
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t_{PLH} t_{PHL}	Propagation Delay Time (for HC620)	2.0	50			41	100		125		150	ns
		4.5				12	20		25		30	
		6.0				10	17		21		26	
		2.0	150			55	130		165		195	ns
		4.5				16	26		33		39	
		6.0				14	22		28		33	
t_{PLH} t_{PHL}	Propagation Delay Time (for HC623)	2.0	50			38	85		105		130	ns
		4.5				12	17		21		26	
		6.0				10	14		18		22	
		2.0	150			51	130		165		195	ns
		4.5				16	26		33		39	
		6.0				14	22		28		33	
t_{PZL} t_{PZH}	Output Enable Time	2.0	50	R_L = 1 KΩ		57	150		190		225	ns
		4.5				19	30		38		45	
		6.0				16	26		32		38	
		2.0	150	R_L = 1 KΩ		69	180		225		270	ns
		4.5				23	36		45		54	
		0				20	31		38		46	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0	50	R_L = 1 KΩ		43	125		155		190	ns
		4.5				18	25		31		38	
		6.0				15	21		26		32	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance		for HC620 for HC623			32 34						pF

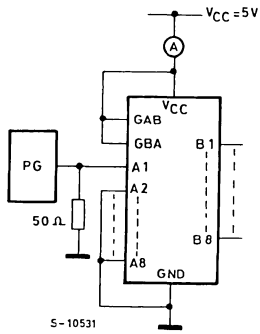
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM





TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

C_{PD} CALCULATION

C_{PD} is to be calculated with the following formula by using the measured value of I_{CC} (Opr.) in the test circuit opposite.

$$C_{PD} = \frac{I_{CC}\,(Opr.)}{f_{IN} \times V_{CC}}$$

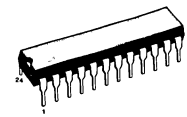
In determining the typical value of C_{PD}, a relatively high frequency of 1 MHz was applied to f_{IN}, in order to eliminate any error caused by the quiescent supply current.

SGS-THOMSON MICROELECTRONICS

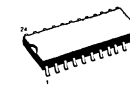
M74HC646
M74HC648

HC646 OCTAL BUS TRANSCEIVER/REGISTER (3-STATE)
HC648 OCTAL BUS TRANSCEIVER/REGISTER (3-STATE, INV.)

- HIGH SPEED
  f_{MAX} = 73 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS646/648



B1R
(Plastic Package)



M1R
(Micro Package)

ORDER CODES :
M74HCXXXM1R M74HCXXXB1R

DESCRIPTION

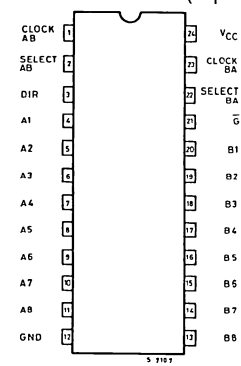
The M74HC646/648 are high speed CMOS OCTAL BUS TRANSCEIVERS AND REGISTERS, (3-STATE) fabricated in silicon gate C^2MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption.

These devices consist of bus transceiver circuits with 3-state output, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (Clock AB - or Clock BA). Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

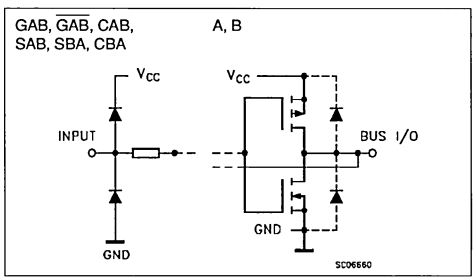
The select controls (Select AB select BA) can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when enable $\overline{G}$ is active (low).

In the isolation mode (enable $\overline{G}$ high), "A" data may be stored in one register and/or "B" data may be stored in the other register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

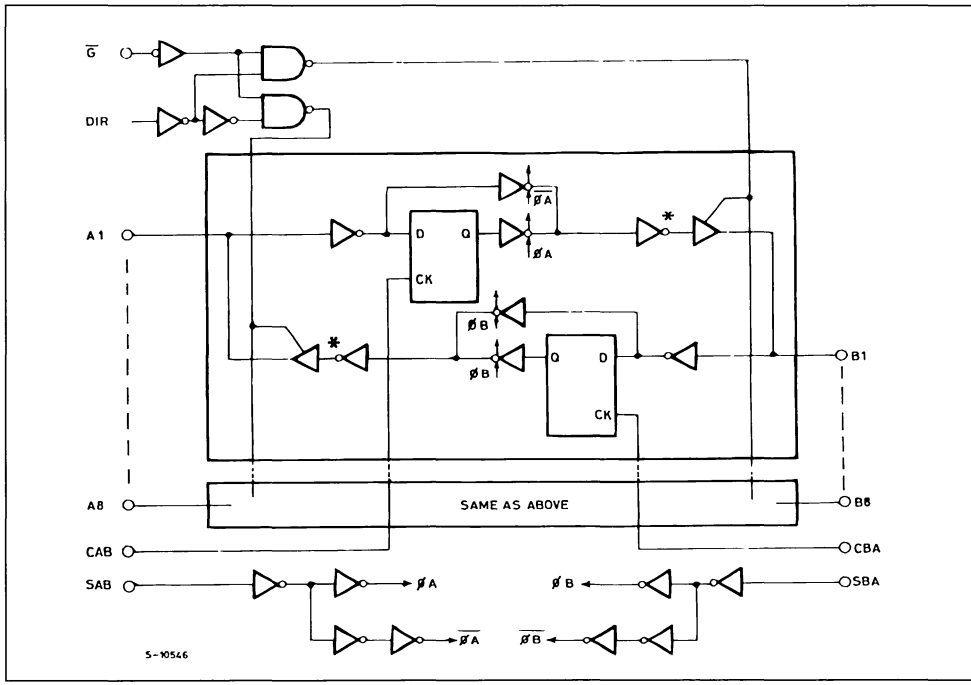
PIN CONNECTIONS (top view)



INPUT AND OUTPUT EQUIVALENT CIRCUIT

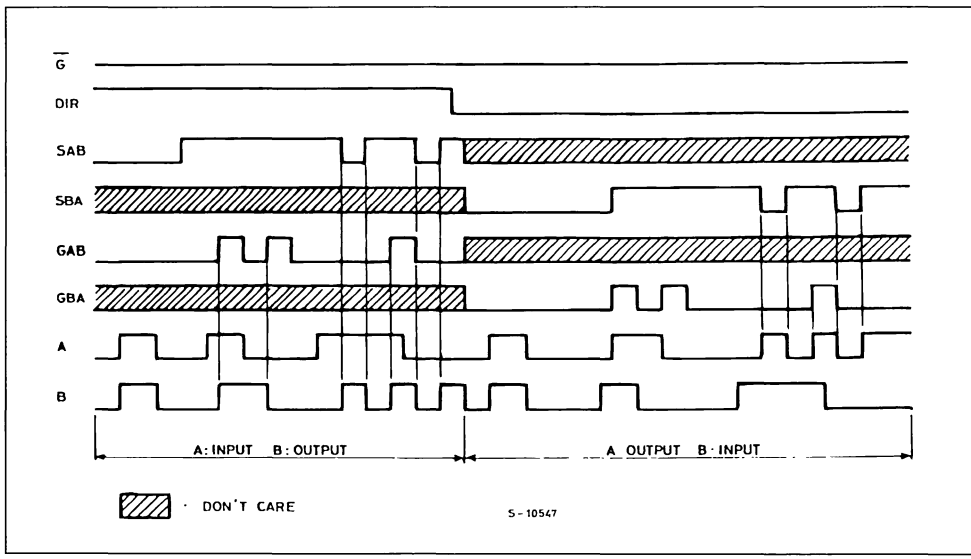


LOGIC DIAGRAM (HC648)



Note : In case of M54/74HC646 output inverter marked * at A bus and B bus are eliminated

TIMING CHART



TRUTH TABLE

HC646 (The truth table for HC648 is the same as this, but with the outputs inverted)

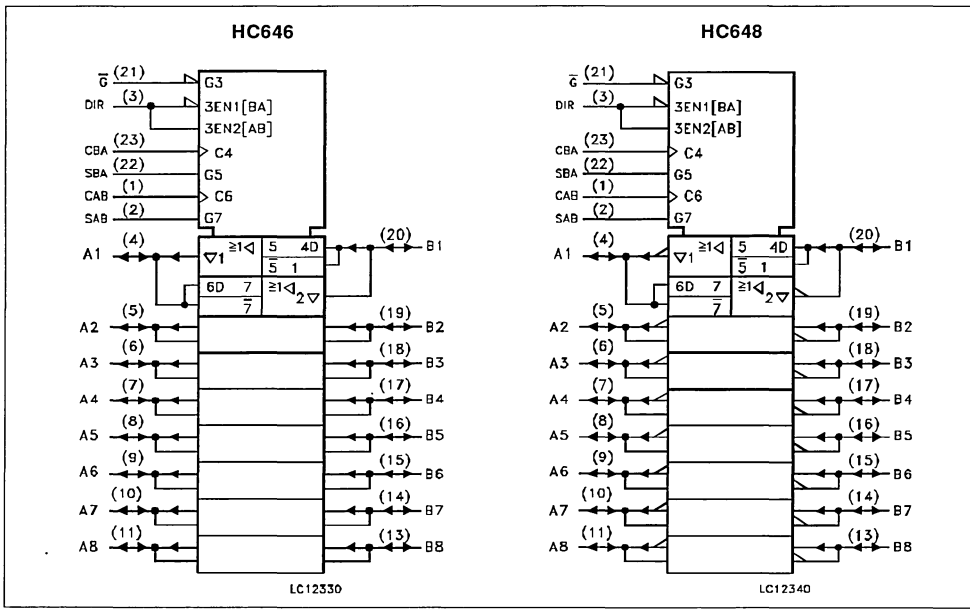
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A	B	FUNCTION
H	X					INPUTS	INPUTS	Both the A bus and the B bus are inputs
		X	X	X	X	Z	Z	The output functions of the A and B bus are disabled
		↑	↑	X	X	INPUTS	INPUTS	Both the A and B bus are used for inputs to the internal flip-flops. Data at the bus will be stored on low to high transition of the clock inputs
L	H					INPUTS	OUTPUTS	The A bus are inputs and the B bus are outputs
		X	X*	L	X	L	L	The data at the A bus are displayed at the B bus
						H	H	
		↑	X*	L	X	L	L	The data at the A bus are displayed at the B bus. The data of the A bus are stored to the internal flip-flop on low to high transition of th clock pulse.
						H	H	
		X	X*	H	X	X	Qn	The data stored to the internal flip-flop are dispayed at the B bus
		↑	X*	H	X	L	L	The data at the A bus are stored to the internal flip-flop on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the B bus
						H	H	
L	L					OUTPUTS	INPUTS	The B bus are inputs and the A bus are outputs
		X*	X	X	L	L	L	The data at the B bus are displayed at the A bus
						H	H	
		X*	↑	X	L	L	L	The data at the B bus are displayed at the A bus. The data of the B bus are stored to the internal flip-flop on low to high transition of the clock pulse
						H	H	
		X*	X	X	H	Qn	X	The data stored to the internal flip-flops are displayed at the A bus
		x*	↑	X	H	L	L	the data at the B bus are stored to the internal flip-flop on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the A bus
						H	H	

X : DON'T CARE
Z : HIGH IMPEDANCE
Qn : THE DATA STORED TO THE INTERNAL FLIP-FLOPS BY MOST RECENT LOW TO HIGH TRANSITION OF THE CLOCK INPUTS
* : THE DATA AT THE A AND B BUS WILL BE STORED TO THE INTERNAL FLIP-FLOPS ON EVERY LOW TO HIGH TRANSITION OF THE CLOCK INPUTS

PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	CLOCK AB	A to B Clock Input (LOW to HIGH, Edge-Trigged)
2	SELECT AB	Select A to B Source Input
3	GAB	Direction Control Input
4, 5, 6, 7, 8, 9, 10, 11	A1 to A8	A data Inputs/Outputs
20, 19, 18, 17, 16, 15, 14, 13	B1 to B8	B Data Inputs/Outputs
21	$\overline{G}$	Output Enable Input (Active LOW)
22	SELECT BA	Select B to A Source Input
23	CLOCK BA	B to A Clock Input (LOW to HIGH, Edge-Triggered)
12	GND	Ground (0V)
24	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value					Unit
		V_{CC} (V)			T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		V
		4.5			3.15			3.15		
		6.0			4.2			4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5	V
		4.5					1.35		1.35	
		6.0					1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 μA	1.9	2.0		1.9		V
		4.5			4.4	4.5		4.4		
		6.0			5.9	6.0		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 μA		0.0	0.1		0.1	V
		4.5				0.0	0.1		0.1	
		6.0				0.0	0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.37	
		6.0		I_O= 7.8 mA		0.18	0.26		0.37	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1	μA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5.0	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40	μA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	Test Conditions			Value					Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75	ns
		4.5				7	12		15	
		6.0				6	10		13	
t_{PLH} t_{PHL}	Propagation Delay Time (BUS - BUS)	2.0	50			74	150		190	ns
		4.5				21	30		38	
		6.0				18	26		32	
		2.0	150			91	190		240	ns
		4.5				26	38		48	
		6.0				22	32		41	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - BUS)	2.0	50			98	210		265	ns
		4.5				28	42		53	
		6.0				24	36		45	
		2.0	150			116	250		315	ns
		4.5				33	50		63	
		6.0				28	43		54	

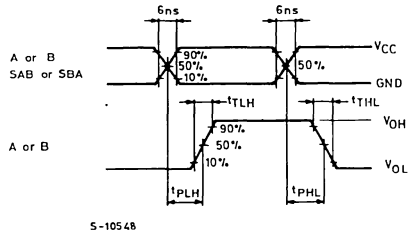
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value					Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time (SELECT - BUS)	2.0	50			81	170		215	ns
		4.5				23	34		43	
		6.0				20	29		37	
		2.0	150			98	210		265	ns
		4.5				28	42		53	
		6.0				24	36		45	
t_{PZL} t_{PZH}	3-State Output Enable Time ($\overline{G}$, DIR)	2.0	50	R_L = 1 KΩ		84	175		220	ns
		4.5				24	35		44	
		6.0				20	30		37	
		2.0	150	R_L = 1 KΩ		102	215		270	ns
		4.5				29	43		54	
		6.0				25	37		46	
t_{PLZ} t_{PHZ}	Output Disable Time ($\overline{G}$, DIR)	2.0	50	R_L = 1 KΩ		60	175		220	ns
		4.5				23	35		44	
		6.0				20	30		37	
f_{MAX}	Maximum Clock Frequency	2.0	50		6	19		4.8		MHz
		4.5			30	67		24		
		6.0			35	79		28		
$t_{W(H)}$ $t_{W(L)}$	Minimum Clock Pulse Width	2.0	50			30	75		95	ns
		4.5				7	15		19	
		6.0				6	13		16	
t_s	Minimum Set-up Time	2.0	50			16	50		65	ns
		4.5				4	10		13	
		6.0				3	9		11	
t_h	Minimum Hold Time	2.0	50				5		5	ns
		4.5					5		5	
		6.0					5		5	
C_{IN}	Input Capacitance					5	10		10	pF
$C_{I/O}$	Bus Terminal Capacitance					10				pF
C_{PD} (*)	Power Dissipation Capacitance		for HC646 for HC648			39 38				pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per bit)

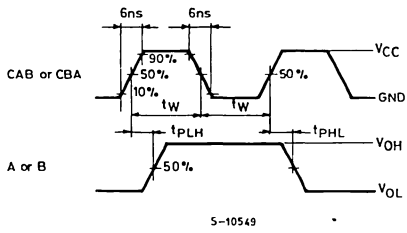
SWITCHING CHARACTERISTICS TEST CIRCUIT AND WAVEFORM

WAVEFORM 1



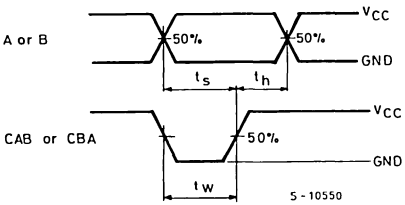
S-10548

WAVEFORM 2



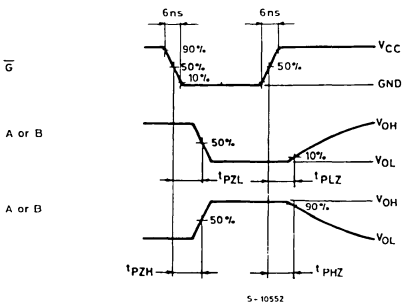
S-10549

WAVEFORM 3



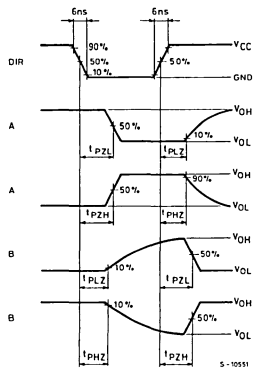
S-10550

WAVEFORM 4



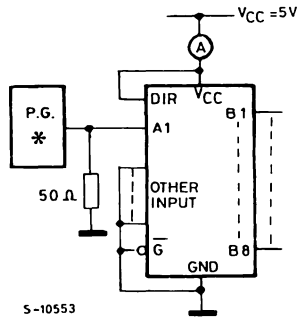
S-10552

WAVEFORM 5



S-10551

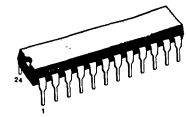
TEST WAVEFORM I_{CC} (Opr.)



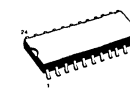
* INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

HCT646 OCTAL BUS TRANSCEIVER/REGISTER (3-STATE)
HCT648 OCTAL BUS TRANSCEIVER/REGISTER (3-STATE, INV.)

- HIGH SPEED
  f_{MAX} = 60 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS646/648



B1R
(Plastic Package)



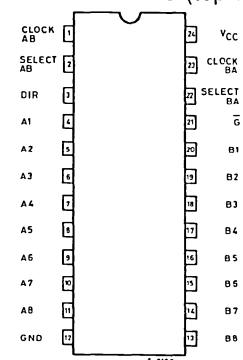
M1R
(Micro Package)

ORDER CODES :
M74HCTXXXM1R M74HCTXXXB1R

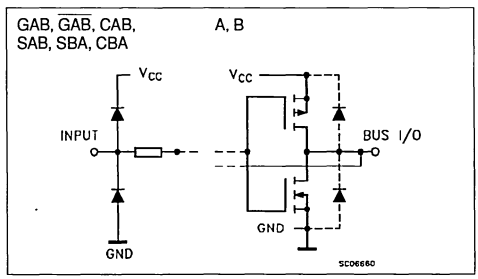
DESCRIPTION

The M74HCT646/648 are high speed CMOS OCTAL BUS TRANSCEIVERS AND REGISTERS, (3-STATE) fabricated in silicon gate C^2MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. These devices consist of bus transceiver circuits with 3-state output, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (Clock AB - or Clock BA). Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (Select AB select BA) can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when enable $\overline{G}$ is active (low). In the isolation mode (enable $\overline{G}$ high), "A" data may be stored in one register and/or "B" data may be stored in the other register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time. All inputs are equipped with protection circuits against static discharge and transient excess voltage.This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

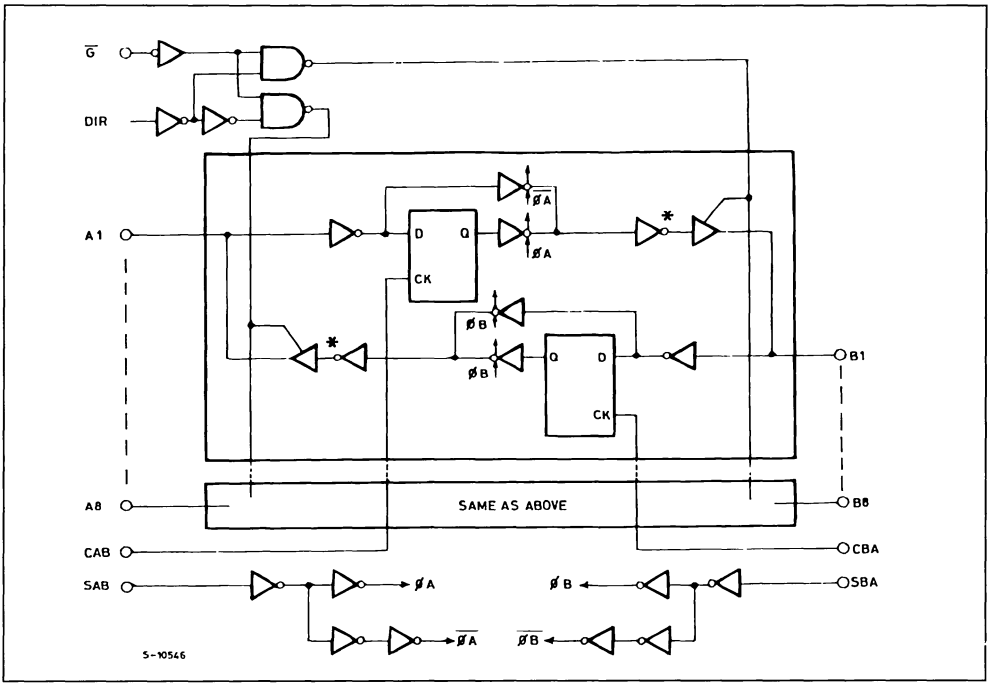
PIN CONNECTIONS (top view)



INPUT AND OUTPUT EQUIVALENT CIRCUIT

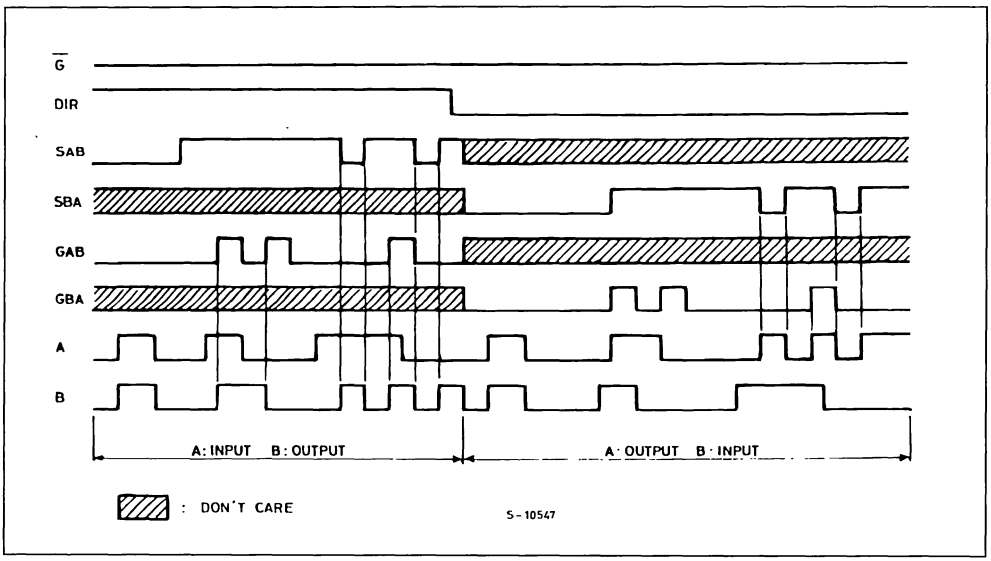


LOGIC DIAGRAM (HCT648)



Note : In case of M54/74HCT646 output inverter marked * at A bus and B bus are eliminated.

TIMING CHART



TRUTH TABLE

HCT646 (The truth table for HCT648 is the same as this, but with the outputs inverted)

$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A	B	FUNCTION
						INPUTS	INPUTS	Both the A bus and the B bus are inputs
H	X	X	X	X	X	Z	Z	The output functions of the A and B bus are disabled
		↓	↓	X	X	INPUTS	INPUTS	Both the A and B bus are used for inputs to the internal flip-flops. Data at the bus will be stored on low to high transition of the clock inputs
						INPUTS	OUTPUTS	The A bus are inputs and the B bus are outputs
		X	X*	L	X	L	L	The data at the A bus are displayed at the B bus
						H	H	
		↓	X*	L	X	L	L	The data at the A bus are displayed at the B bus. The data of the A bus are stored to the internal flip-flop on low to high transition of th clock pulse.
L	H					H	H	
		X	X*	H	X	X	Qn	The data stored to the internal flip-flop are dispayed at the B bus
		↓	X*	H	X	L	L	The data at the A bus are stored to the internal flip-flop on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the B bus
						H	H	
						OUTPUTS	INPUTS	The A bus are outputs and the B bus are inputs
		X*	X	X	L	L	L	The data at the B bus are displayed at the A bus
						H	H	
		X*	↓	X	L	L	L	The data at the B bus are displayed at the A bus. The data of the B bus are stored to the internal flip-flop on low to high transition of the clock pulse
L	L					H	H	
		X*	X	X	H	Qn	X	The data stored to the internal flip-flops are displayed at the B bus
		x*	↓	X	H	L	L	the data at the B bus are stored to the internal flip-flop on low.to high transition of the clock pulse. The states of the internal flip-flops output directly to the A bus
						H	H	

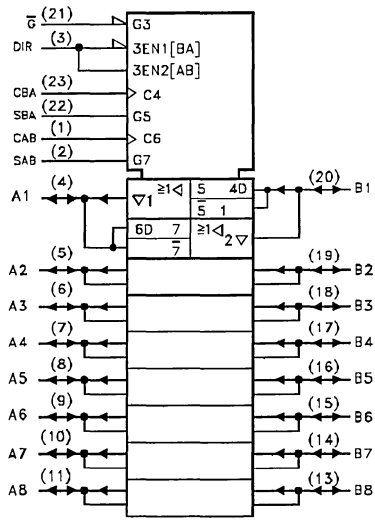
X : DON'T CARE
Z : HIGH IMPEDANCE
Qn : THE DATA STORED TO THE INTERNAL FLIP-FLOPS BY MOST RECENT LOW TO HIGH TRANSITION OF THE CLOCK INPUTS
* : THE DATA AT THE A AND B BUS WILL BE STORED TO THE INTERNAL FLIP-FLOPS ON EVERY LOW TO HIGH TRANSITION OF THE CLOCK INPUTS

PIN DESCRIPTION

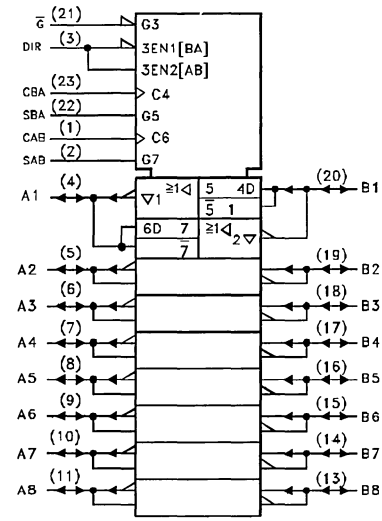
PIN No	SYMBOL	NAME AND FUNCTION
1	CLOCK AB	A to B Clock Input (LOW to HIGH, Edge-Trigged)
2	SELECT AB	Select A to B Source Input
3	DIR	Direction Control Input
4, 5, 6, 7, 8, 9, 10, 11	A1 to A8	A data Inputs/Outputs
20, 19, 18, 17, 16, 15, 14, 13	B1 to B8	B Data Inputs/Outputs
21	$\overline{G}$	Output Enable Input (Active LOW)
22	SELECT BA	Select B to A Source Input
23	CLOCK BA	B to A Clock Input (LOW to HIGH, Edge-Triggered)
12	GND	Ground (0V)
24	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS

HCT646



HCT648



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-40 to +85	°C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value					Unit
		V_{CC} (V)			T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		V
				I_O=-6.0 mA	4.18	4.31		4.13		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1	V
				I_O= 6.0 mA		0.17	0.26		0.33	
I_I	Input Leakage Current (*)	5.5	V_I = V_{CC} or GND				±0.1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				4		40	µA
I_{OZ}	Output Off-state Current	5.5	V_O = V_{CC} or GND V_I = V_{IH} or V_{IL}				æ0.5		±5	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9	mA

(*): Applicable only to DIR, $\overline{G}$, CAB, CBA, SBA input.

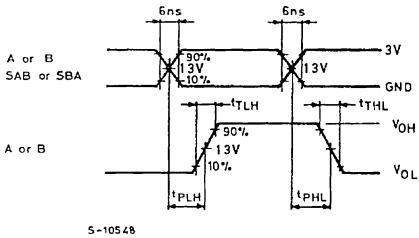
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value					Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		
					Min.	Typ.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5	50			7	12		15	ns
t_{PLH} t_{PHL}	Propagation Delay Time (BUS - BUS)	4.5	50			20	30		38	ns
		4.5	150			25	38		48	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - BUS)	4.5	50			29	44		55	ns
		4.5	150			34	52		65	ns
t_{PLH} t_{PHL}	Propagation Delay Time (SELECT - BUS)	4.5	50			24	34		43	ns
		4.5	150			29	42		53	ns
t_{PZL} t_{PZH}	3-State Output Enable Time ($\overline{G}$, DIR - BUS)	4.5	50	R_L = 1 KΩ		26	38		48	ns
		4.5	150	R_L = 1 KΩ		31	46		58	ns
t_{PLZ} t_{PHZ}	3-State Output Disable Time ($\overline{G}$, DIR - BUS)	4.5	50	R_L = 1 KΩ		26	35		44	ns
f_{MAX}	Maximum Clock Frequency	4.5	50		31	55		25		MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width	4.5	50			8	15		19	ns
t_s	Minimum Set-up Time	4.5	50			3	10		13	ns
t_h	Minimum Hold Time	4.5	50				5		5	ns
C_{IN}	Input Capacitance					5	10		10	pF
$C_{I/O}$	Bus Terminal Capacitance					13				pF
C_{PD} (*)	Power Dissipation Capacitance		for HCT646 for HCT648			40 39				pF

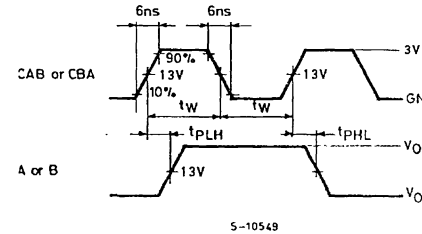
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per bit)

SWITCHING CHARACTERISTICS TEST CIRCUIT AND WAVEFORM

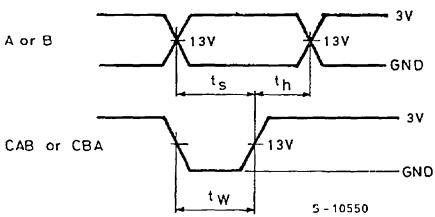
WAVEFORM 1



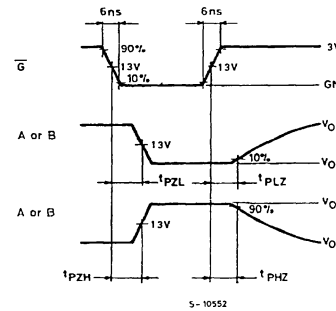
WAVEFORM 2



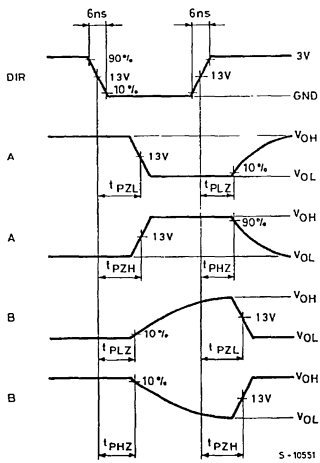
WAVEFORM 3



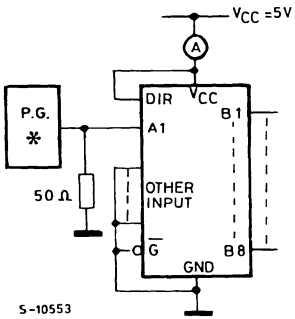
WAVEFORM 4



WAVEFORM 5



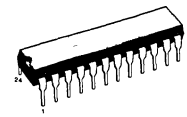
TEST WAVEFORM I_{CC} (Opr.)



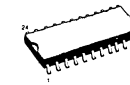
* INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

HC651 OCTAL BUS TRANSCEIVER/REGISTER (3-STATE, INV.)
HC652 OCTAL BUS TRANSCEIVER/REGISTER (3-STATE)

- HIGH SPEED
  f_{MAX} = 73 MHz (TYP.) AT V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS651/652



B1R
(Plastic Package)



M1R
(Micro Package)

ORDER CODES :
M74HCXXXM1R M74HCXXXB1R

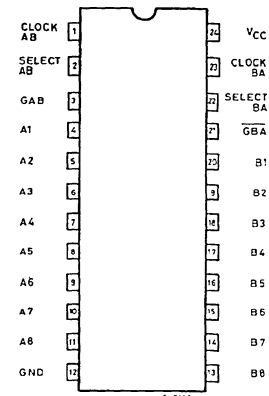
DESCRIPTION

M74HC651/652 are high speed CMOS OCTAL BUS TRANSCEIVERS AND REGISTERS (3-STATE), fabricated in silicon gate C^2MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal storage registers. Enable GAB and $\overline{GBA}$ are provided to control the transceiver functions.

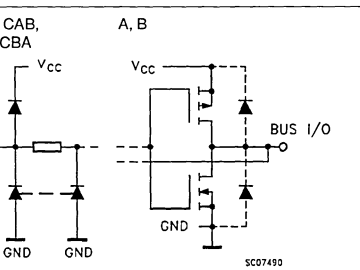
Select AB and Select BA control pins are provided to select whether real-time or stored data is transfered. A low input level selects real-time data, and a high selects stored data.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CLOCK AB or CLOCK BA) regardless of the select or enable control pins. When select AB and select BA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and GBA. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

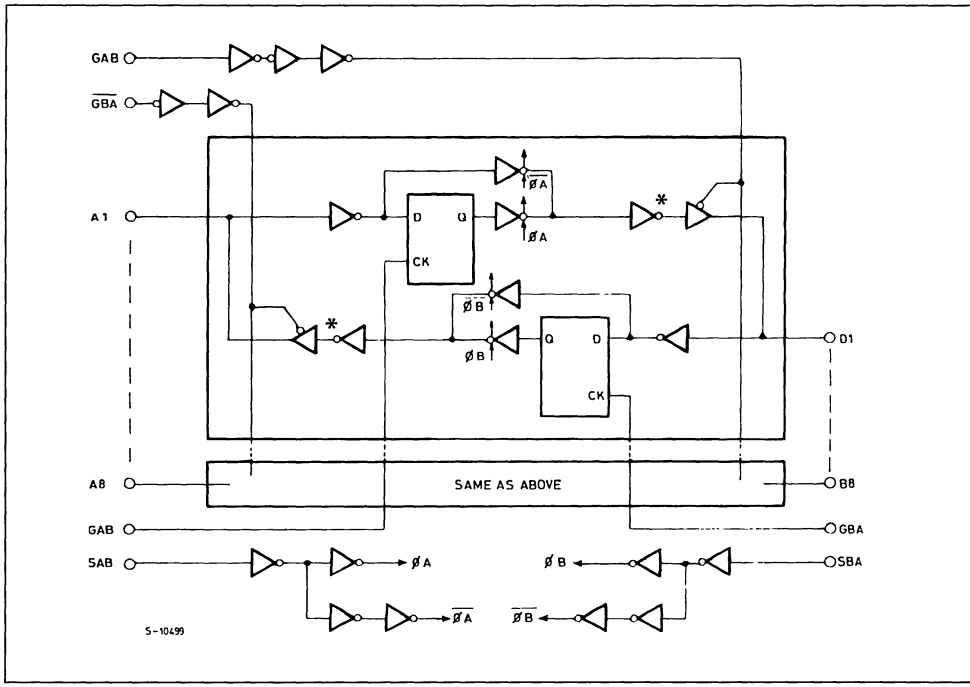
PIN CONNECTIONS (top view)



INPUT AND OUTPUT EQUIVALENT CIRCUIT

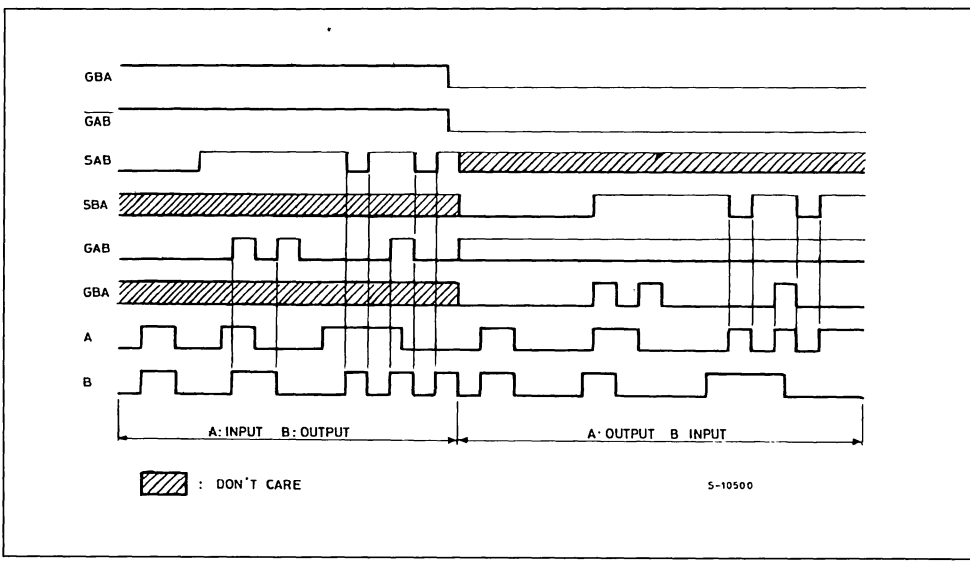


LOGIC DIAGRAM (HC652)



Note : In case of M74HC652 output inverter marked * at A bus and B bus are eliminated.

TIMING CHART



TRUTH TABLE

HC652 (The truth table for HC651 is the same as this, but with the outputs inverted)

GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A	B	FUNCTION
L	H					INPUTS	INPUTS	Both the A bus and the B bus are inputs
		X	X	X	X	Z	Z	The output functions of the A and B bus are disabled
		⌐	⌐	X	X	INPUTS	INPUTS	Both the A and B buz are used for inputs to the internal flip-flops. Data at the bus will be stored on low to high transition of the clock inputs
L	L					OUTPUTS	INPUTS	The A bus are outputs and the B bus are inputs
		X*	X	X	L	L	L	The data at the B bus are displayed at the A bus
						H	H	
		X*	⌐	X	L	L	L	The data at the B bus ar displayed at the A bus. The data of the B bus are stored to the internal flip-flop on low to high transition of th clock pulse
						H	H	
		X*	X	X	H	Qn	X	The data stored to the internal flip-flop are dispayed at the A bus
		X*	⌐	X	H	L	L	The data at the B bus are stored to the internal flip-flop on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the A bus
						H	H	
H	H					INPUTS	OUTPUTS	The A bus are inputs and the B bus are outputs
		X	X*	L	X	L	L	The data at the A bus are displayed at the B bus
						H	H	
		⌐	X*	L	X	L	L	The data at the A bus are displayed at the B bus. The data of the A bus are stored to the internal flip-flop on low to high transition of the clock pulse
						H	H	
		X	X*	H	X	X	Qn	The data stored to the internal flip-flops are displayed at the B bus
		⌐	X*	H	X	L	L	the data at the A bus are stored to the internal flip-flop on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the B bus
						H	H	
H	L					OUTPUTS	OUTPUTS	Both the A bus and the B bus are outputs
		X	X	H	H	Qn	Qn	The data stored to the internal flip-flops are displayed at the A and B bus respectively
		⌐	⌐	H	H	Qn	Qn	The output at the A bus are displayed at the B bus, the output at the B bus are displayed at the A bus respectively

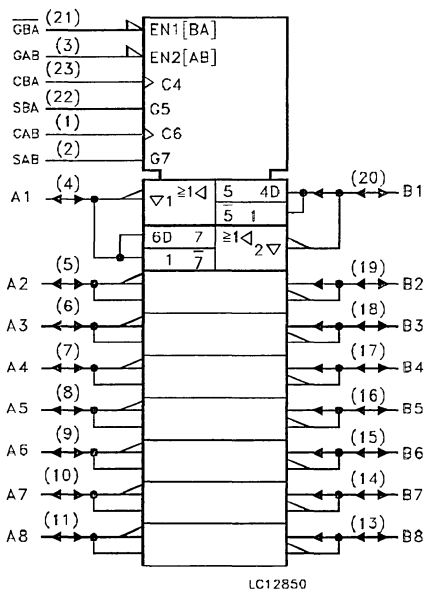
X : DON'T CARE
Z : HIGH IMPEDANCE
Qn : THE DATA STORED TO THE INTERNAL FLIP-FLOPS BY MOST RECENT LOW TO HIGH TRANSITION OF THE CLOCK INPUTS
* : THE DATA AT THE A AND B BUS WILL BE STORED TO THE INTERNAL FLIP-FLOPS ON EVERY LOW TO HIGH TRANSITION OF THE CLOCK INPUTS

PIN DESCRIPTION

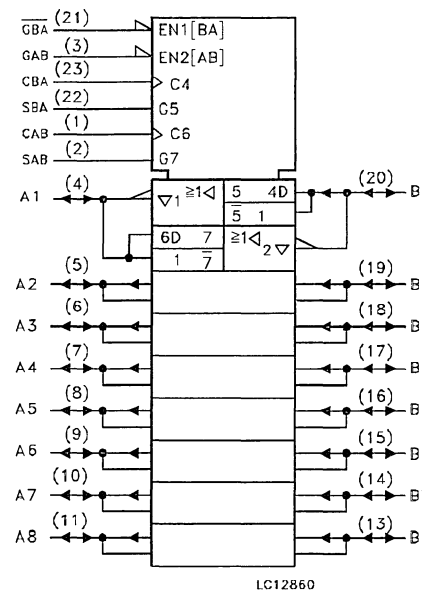
PIN No	SYMBOL	NAME AND FUNCTION
1	CLOCK AB	A to B Clock Input (LOW to HIGH, Edge-Trigged)
2	SELECT AB	Select A to B Source Input
3	GAB	Direction Control Input
4, 5, 6, 7, 8, 9, 10, 11	A1 to A8	A data Inputs/Outputs
20, 19, 18, 17, 16, 15, 14, 13	B1 to B8	B Data Inputs/Outputs
21	$\overline{GBA}$	Output Enable Input (Active LOW)
22	SELECT BA	Select B to A Source Input
23	CLOCK BA	B to A Clock Input (LOW to HIGH, Edge-Triggered)
12	GND	Ground (0V)
24	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS

HC651



HC652



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature:		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value					Unit
		V_{CC} (V)			T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		V
		4.5			3.15			3.15		
		6.0			4.2			4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5	V
		4.5					1.35		1.35	
		6.0					1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		V
		4.5			4.4	4.5		4.4		
		6.0			5.9	6.0		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1	V
		4.5				0.0	0.1		0.1	
		6.0				0.0	0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.37	
		6.0		I_O= 7.8 mA		0.18	0.26		0.37	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5.0	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40	µA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 6 ns)

Symbol	Parameter	Test Conditions			Value					Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75	ns
		4.5				7	12		15	
		6.0				6	10		13	
t_{PLH} t_{PHL}	Propagation Delay Time (BUS - BUS)	2.0	50			74	150		190	ns
		4.5				21	30		38	
		6.0				18	26		32	
		2.0	150			91	190		240	ns
		4.5				26	38		48	
		6.0				22	32		41	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - BUS)	2.0	50			98	210		265	ns
		4.5				28	42		53	
		6.0				24	36		45	
		2.0	150			116	250		315	ns
		4.5				33	50		63	
		6.0				28	43		54	

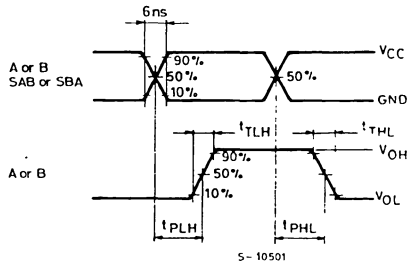
AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions			Value					Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time (SELECT - BUS)	2.0	50			81	170		215	ns
		4.5				23	34		43	
		6.0				20	29		37	
		2.0	150			98	210		265	ns
		4.5				28	42		53	
		6.0				24	36		45	
t_{PZL} t_{PZH}	3-State Output Enable Time	2.0	50	R_L = 1 KΩ		74	175		220	ns
		4.5				21	35		44	
		6.0				18	30		37	
		2.0	150	R_L = 1 KΩ		91	215		270	ns
		4.5				26	43		54	
		6.0				22	37		46	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0	50	R_L = 1 KΩ		50	175		220	ns
		4.5				21	35		44	
		6.0				18	30		37	
f_{MAX}	Maximum Clock Frequency	2.0	50		6	19		4.8		MHz
		4.5			30	67		24		
		6.0			35	79		28		
$t_{W(H)}$ $t_{W(L)}$	Minimum Clock Pulse Width	2.0	50			30	75		95	ns
		4.5				7	15		19	
		6.0				6	13		16	
t_s	Minimum Set-up Time	2.0	50			16	50		65	ns
		4.5				4	10		13	
		6.0				3	9		11	
t_h	Minimum Hold Time	2.0	50				5		5	ns
		4.5					5		5	
		6.0					5		5	
C_{IN}	Input Capacitance					5	10		10	pF
$C_{I/O}$	Bus Terminal Capacitance					10				pF
C_{PD} (*)	Power Dissipation Capacitance		for HC651 for HC652			39 38				pF

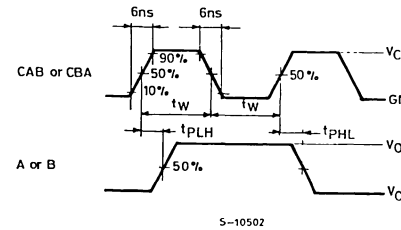
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Channel)

SWITCHING CHARACTERISTICS TEST CIRCUIT AND WAVEFORM

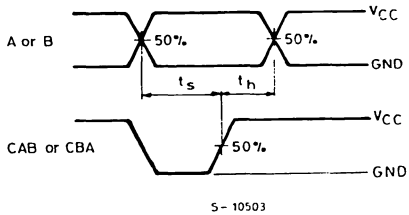
WAVEFORM 1



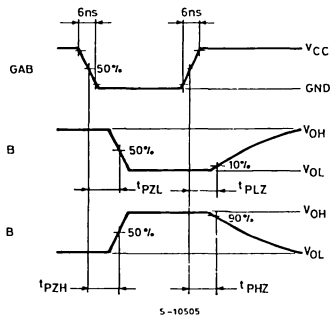
WAVEFORM 2



WAVEFORM 3

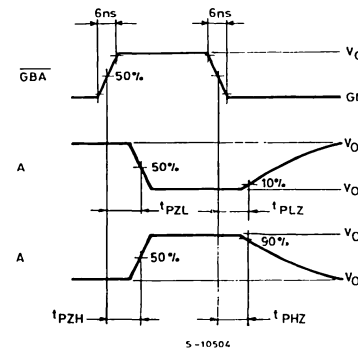


WAVEFORM 4



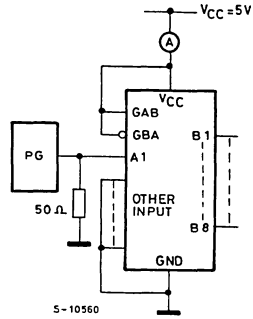
$\overline{GBA}$ = "H"

WAVEFORM 5



GAB = "L"

TEST WAVEFORM I_{CC} (Opr.)



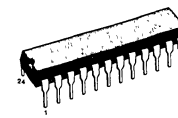
INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

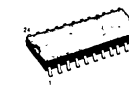
M74HCT651
M74HCT652

HCT651 OCTAL BUS TRANSCEIVER/REGISTER (3-STATE, INV.)
HCT652 OCTAL BUS TRANSCEIVER/REGISTER (3-STATE)

- HIGH SPEED
  f_{MAX} = 60 MHz (TYP.) AT V_{CC} = 5V
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2 V (MIN.) AT V_{IL} = 0.8V (MAX)
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX) AT T_A = 25 °C
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (mIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS651/652



B1R
(Plastic Package)



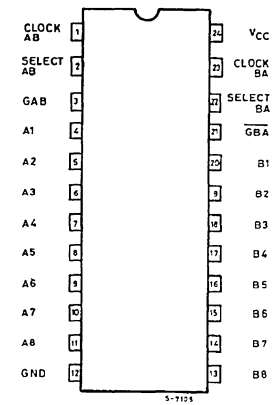
M1R
(Micro Package)

ORDER CODES :
M74HCXXXM1R M74HCXXXB1R

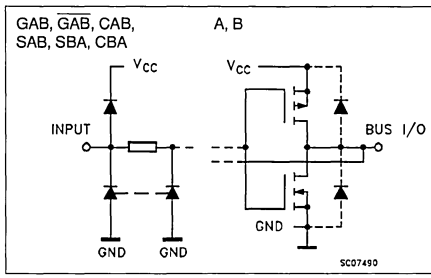
DESCRIPTION

M74HCT651/652 are high speed CMOS OCTAL BUS TRANSCEIVERS AND REGISTERS (3-STATE), fabricated in silicon gate C^2MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal storage registers. Enable GAB and $\overline{GBA}$ are provided to control the transceiver functions. Select AB and Select BA control pins are provided to select whether real-time or stored data is transfered. A low input level selects real-time data, and a high selects stored data. Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CLOCK AB or CLOCK BA) regardless of the select or enable control pins. When select AB and select BA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{GBA}$. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state. All inputs are equipped with protection circuits against static discharge and transient excess voltage.This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSCMOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

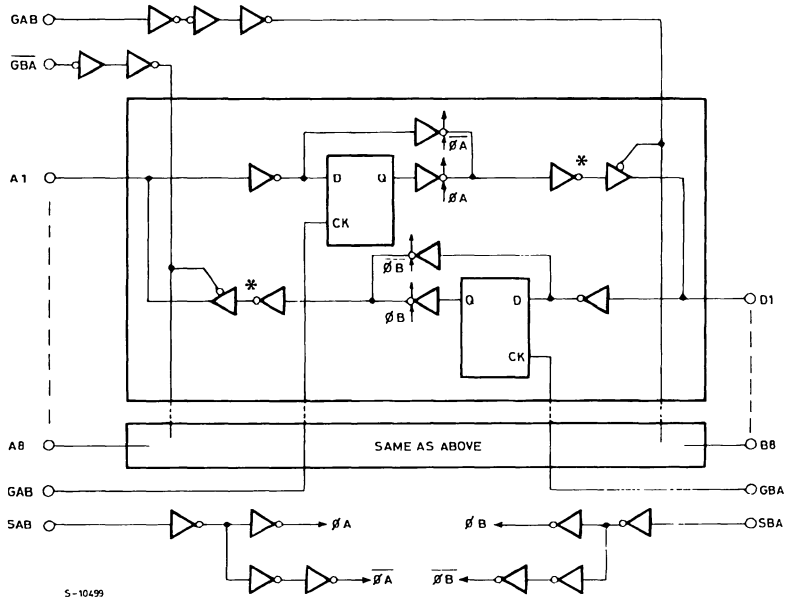
PIN CONNECTIONS (top view)



INPUT AND OUTPUT EQUIVALENT CIRCUIT

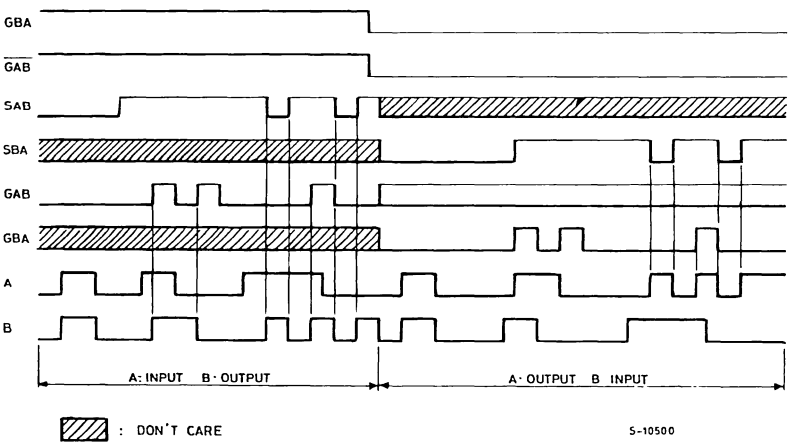


LOGIC DIAGRAM (HCT651)



Note : In case of 74HCT652 output inverter marked * at A bus and B bus are eliminated.

TIMING CHART



TRUTH TABLE

HCT652 (The truth table for HCT651 is the same as this, but with the outputs inverted)

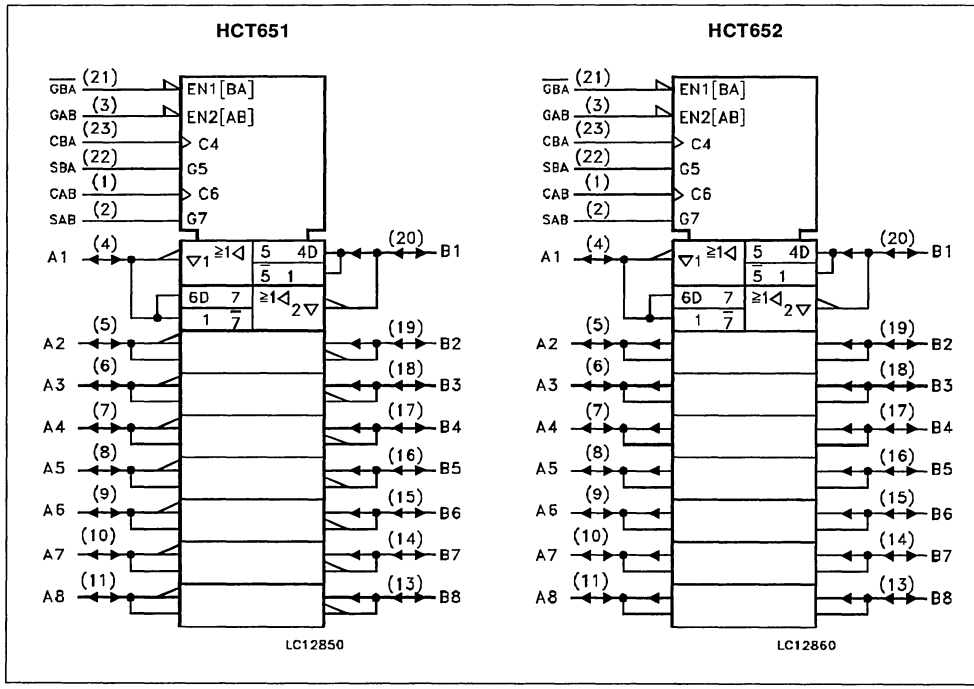
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A	B	FUNCTION
						INPUTS	INPUTS	Both the A bus and the B bus are inputs
L	H	X	X	X	X	Z	Z	The output functions of the A and B bus are disabled
		⌐	⌐	X	X	INPUTS	INPUTS	Both the A and B bus are used for inputs to the internal flip-flops. Data at the bus will be stored on low to high transition of the clock inputs
						OUTPUTS	INPUTS	The A bus are outputs and the B bus are inputs
		X*	X	X	L	L	L	The data at the B bus are displayed at the A bus
						H	H	
		X*	⌐	X	L	L	L	The data at the B bus ar displayed at the A bus. The data of the B bus are stored to the internal flip-flop on low to high transition of th clock pulse
L	L					H	H	
		X*	X	X	H	Qn	X	The data stored to the internal flip-flop are dispayed at the A bus
		X*	⌐	X	H	L	L	The data at the B bus are stored to the internal flip-flop on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the A bus
						H	H	
						INPUTS	OUTPUTS	The A bus are inputs and the B bus are outputs
		X	X*	L	X	L	L	The data at the A bus are displayed at the B bus
						H	H	
		⌐	X*	L	X	L	L	The data at the A bus are displayed at the B bus. The data of the A bus are stored to the internal flip-flop on low to high transition of the clock pulse
H	H					H	H	
		X	X*	H	X	X	Qn	The data stored to the internal flip-flops are displayed at the B bus
		⌐	X*	H	X	L	L	the data at the A bus are stored to the internal flip-flop on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the B bus
						H	H	
						OUTPUTS	OUTPUTS	Both the A bus and the B bus are outputs
H	L	X	X	H	H	Qn	Qn	The data stored to the internal flip-flops are displayed at the A and B bus respactively
		⌐	⌐	H	H	Qn	Qn	The output at the A bus are displayed at the B bus, the output at the B bus are displayed at the A bus respectively

X : DON'T CARE
Z : HIGH IMPEDANCE
Qn : THE DATA STORED TO THE INTERNAL FLIP-FLOPS BY MOST RECENT LOW TO HIGH TRANSITION OF THE CLOCK INPUTS
* : THE DATA AT THE A AND B BUS WILL BE STORED TO THE INTERNAL FLIP-FLOPS ON EVERY LOW TO HIGH TRANSITION OF THE CLOCK INPUTS

PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	CLOCK AB	A to B Clock Input (LOW to HIGH, Edge-Trigged)
2	SELECT AB	Select A to B Source Input
3	GAB	Direction Control Input
4, 5, 6, 7, 8, 9, 10, 11	A1 to A8	A data Inputs/Outputs
20, 19, 18, 17, 16, 15, 14, 13	B1 to B8	B Data Inputs/Outputs
21	$\overline{GBA}$	Output Enable Input (Active LOW)
22	SELECT BA	Select B to A Source Input
23	CLOCK BA	B to A Clock Input (LOW to HIGH, Edge-Triggered)
12	GND	Ground (0V)
24	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature:	-40 to +85	°C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value					Unit
		V_{CC} (V)			T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		V
				I_O=-6.0 mA	4.18	4.31		4.13		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1	V
				I_O= 6.0 mA		0.17	0.26		0.33	
I_I	Input Leakage Current (*)	5.5	V_I = V_{CC} or GND				±0.1		±1	µA
I_{OZ}	3 State Output Off State Current	5.5	V_I = V_{CC} or GND				±0.5		±5.0	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				1		10	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND				2.0		2.9	mA

(*): Applicable only to GAB, $\overline{GBA}$, CAB, CBA, SAB, SBA input

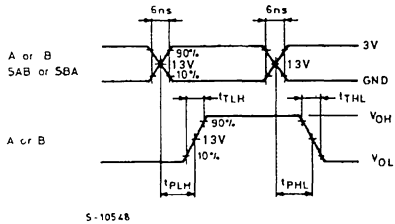
AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	Test Conditions			Value					Unit
		V_{CC} (V)	C_L (pF)		$T_A = 25$ °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5	50			7	12		15	ns
t_{PLH} t_{PHL}	Propagation Delay Time (BUS - BUS)	4.5	50			20	30		38	ns
		4.5	150			25	38		48	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - BUS)	4.5	50			29	44		55	ns
		4.5	150			34	52		65	ns
t_{PLH} t_{PHL}	Propagation Delay Time (SELECT - BUS)	4.5	50			24	34		43	ns
		4.5	150			29	42		53	ns
t_{PZL} t_{PZH}	3-State Output Enable Time (GAB, GBA - BUS)	4.5	50	$R_L = 1$ KΩ		22	33		41	ns
		4.5	150	$R_L = 1$ KΩ		27	41		51	ns
t_{PLZ} t_{PHZ}	Output Disable Time (GAB, GBA - BUS)	4.5	50	$R_L = 1$ KΩ		24	35		44	ns
f_{MAX}	Maximum Clock Frequency	4.5	50		31	55		25		MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Clock Pulse Width	4.5	50			8	15		19	ns
t_s	Minimum Set-up Time	4.5	50			3	10		13	ns
t_h	Minimum Hold Time	4.5	50				5		5	ns
C_{IN}	Input Capacitance					5	10		10	pF
$C_{I/O}$	Bus Terminal Capacitance					13				pF
C_{PD} (*)	Power Dissipation Capacitance		for HCT651 for HCT652			38 39				pF

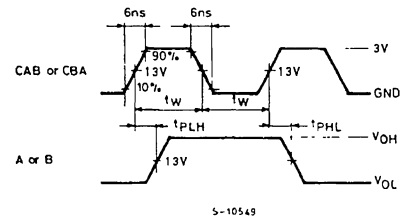
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Channel)

SWITCHING CHARACTERISTICS TEST CIRCUIT AND WAVEFORM

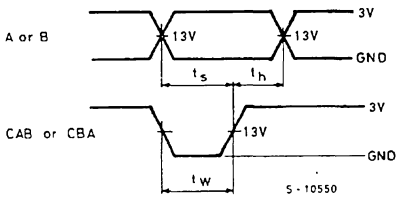
WAVEFORM 1



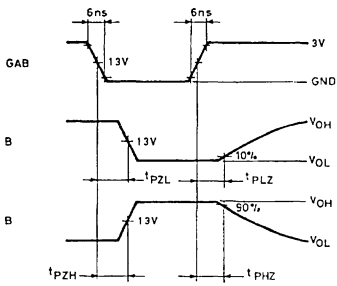
WAVEFORM 2



WAVEFORM 3

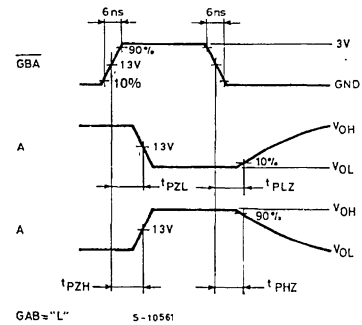


WAVEFORM 4



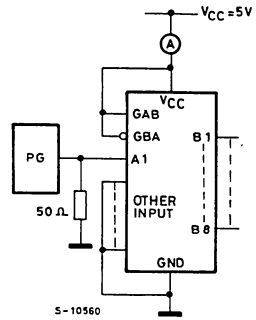
GBA = "H"

WAVEFORM 5



GAB = "L"

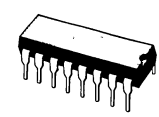
TEST WAVEFORM I_{CC} (Opr.)



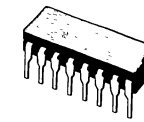
INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

4 WORD X 4 BIT REGISTER FILE (3 STATE)

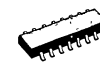
- HIGH SPEED
  t_{PD} = 23 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS670



B1R
(Plastic Package)



F1R
(Ceramic Package)



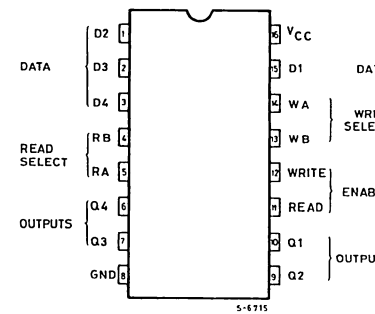
M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HC670F1R M74HC670M1R
M74HC670B1R M74HC670C1R

PIN CONNECTIONS (top view)



NC =
No Internal
Connection

DESCRIPTION

The M54/74HC670 is a high speed CMOS 4 WORD X 4 BIT REGISTER FILE (3-STATE) fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The M54HC/74HC670 is a 4 x 4 Register File organized as four words by four bits. Separate read and write inputs, both address and enable, allow simultaneous read and write operation. The 3-state outputs make it possible to connect up to 128 outputs to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

WRITE FUNCTION TABLE

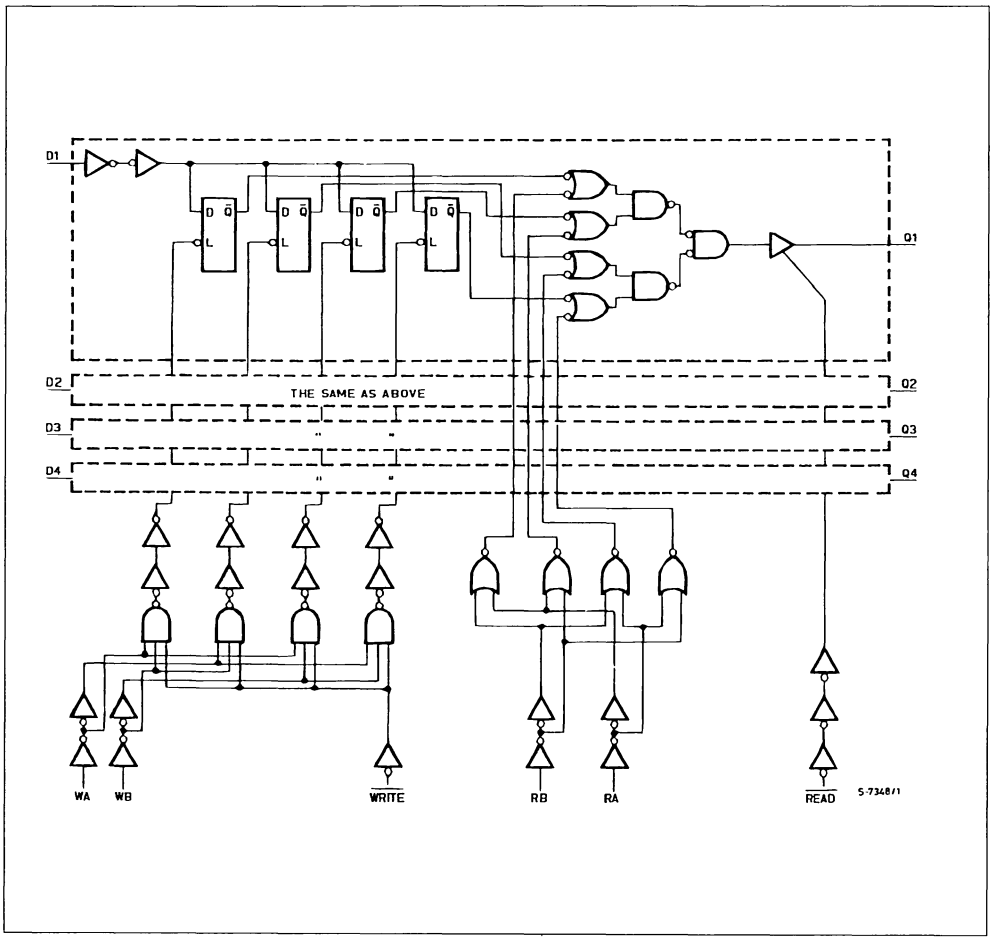
WRITE INPUTS			WORDS			
WB	WA	$\overline{WE}$	0	1	2	3
L	L	L	Q = D	Q0	Q0	Q0
L	H	L	Q0	Q = D	Q0	Q0
H	L	L	Q0	Q0	Q = D	Q0
H	H	L	Q0	Q0	Q0	Q = D
X	X	H	Q0	Q0	Q0	Q0

READ FUNCTION TABLE

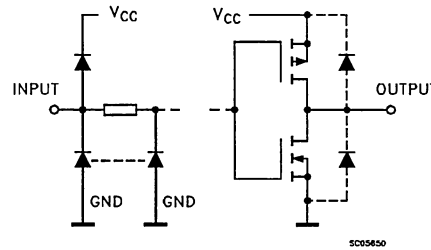
READ INPUTS			OUTPUTS			
RB	RA	$\overline{RE}$	Q0	Q1	Q2	Q3
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

Notes: 1 *. DON'T CARE Z: HIGH IMPEDANCE
2 (Q = D) = THE FOUR SELECT INTERNAL FLIP FLOP OUTPUTS WILL ASSUME THE STATES APPLIED TO THE FOUR EXTERNAL DATA INPUTS.
3 Q0 = THE LEVEL OF Q BEFORE THE INDICATED INPUT CONDITIONS WERE ESTABLISHED.
4 W0B1 = THE FIRST BIT OF WORD 0, ETC.

LOGIC DIAGRAM



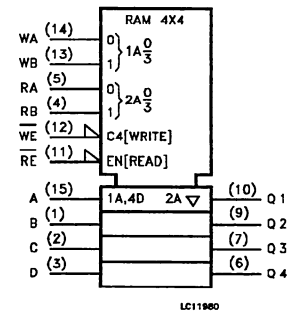
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
5, 4	RA, RB	Read Address Inputs
10, 9, 7, 6	Q1 to Q4	Data Outputs
11	$\overline{RE}$	3 State Output Read Enable Input (Active LOW)
12	$\overline{WE}$	Write Enable Input (Active LOW)
14, 13	WA, WB	Write Address Inputs
15, 1, 2, 3	D1 to D4	Data Inputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

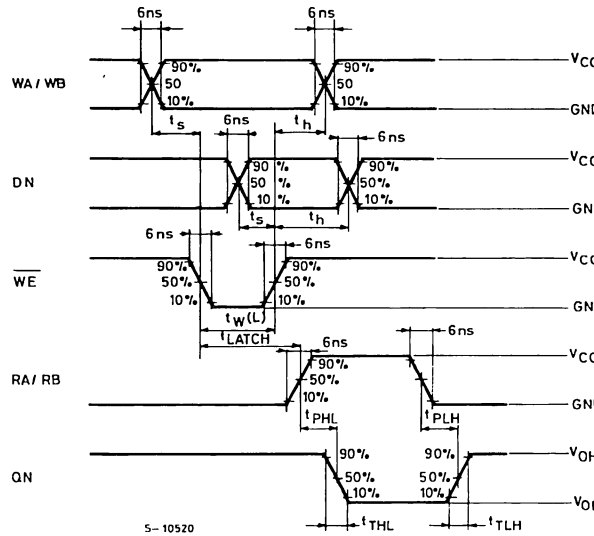
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5		±5	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

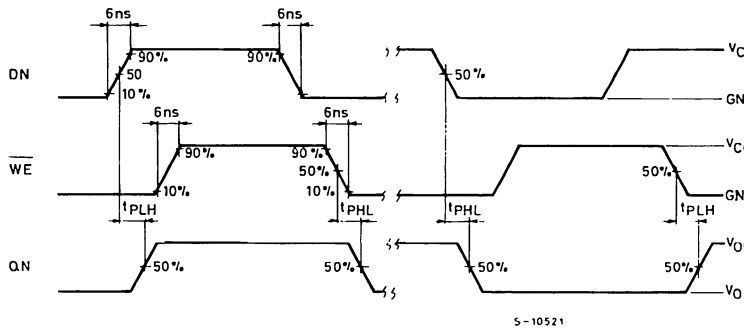
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (RA, RB - Qn)	2.0			96	185		230		280	ns
		4.5			24	37		46		56	
		6.0			20	31		39		48	
t_{PLH} t_{PHL}	Propagation Delay Time (WE - Qn)	2.0			108	220		275		330	ns
		4.5			27	44		55		66	
		6.0			23	37		47		56	
t_{PLH} t_{PHL}	Propagation Delay Time (Dn - Qn)	2.0			104	185		230		280	ns
		4.5			26	37		46		56	
		6.0			22	31		39		48	
t_{PZL} t_{PZH}	Output Disable Time	2.0	R_L = 1 KΩ		42	110		140		165	ns
		4.5			13	22		28		33	
		6.0			11	19		24		28	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0	R_L = 1 KΩ		25	95		120		145	ns
		4.5			13	19		24		29	
		6.0			11	16		20		25	
$t_{W(L)}$	Minimum Pulse Width (WE)	2.0			16	75		95		110	ns
		4.5			4	15		19		22	
		6.0			3	13		16		19	
t_s	Minimum Set-up Time (Dn - WE) (WA, WB - WE)	2.0			12	50		65		75	ns
		4.5			3	10		13		15	
		6.0			3	9		11		13	
t_h	Minimum Hold Time (Dn - WE)	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_h	Minimum Hold Time (WA, WB - WE)	2.0				5		5		5	ns
		4.5				5		5		5	
		6.0				5		5		5	
t_{latch}	Minimum Latch Time (WE - RA, RB)	2.0				5		5		5	ns
		4.5				5		5		5	
		6.0				5		5		5	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				96						pF

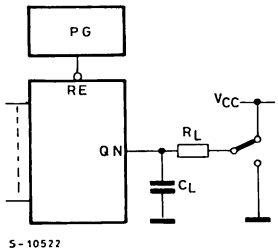
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

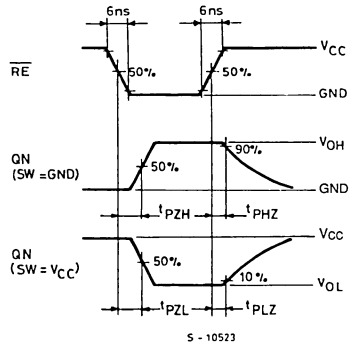
SWITCHING CHARACTERISTICS TEST WAVEFORM





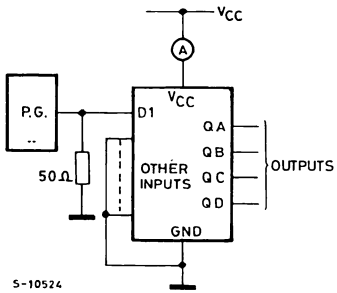
SWITCHING CHARACTERISTICS TEST WAVEFORM (continued)





SUCH A LOGIC LEVEL, SHALL BE APPLIED TO EACH INPUT THAT THE OUTPUT VOLTAGE STAYS IN THE APPOSITE SIDE TO THE SWITCH CONNECTION LEVEL. WHEN THE OUTPUT IS ENABLED.

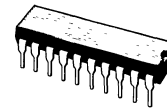
TEST CIRCUIT I_{CC} (Opr.)



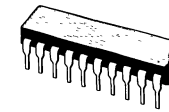
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

8 BIT EQUALITY COMPARATOR

- HIGH SPEED
  t_{PD} = 17 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS688



B1R
(Plastic Package)



F1R
(Ceramic Package)

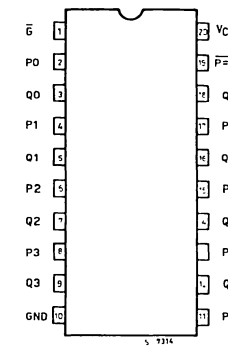
M1R
(Micro Package)

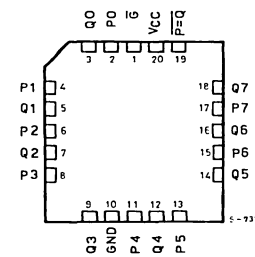
C1R
(Chip Carrier)

ORDER CODES :

M54HC688F1R M74HC688M1R
M74HC688B1R M74HC688C1R

PIN CONNECTIONS (top view)



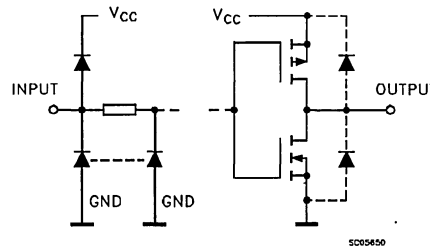


NC =
No Internal
Connection

DESCRIPTION

The M54/74HC688 utilizes silicon gate C^2MOS technology to achieve operating speeds equivalent to LSTTL devices. Along with the low power dissipation and high noise immunity of standard C^2MOS integrated circuit, it possesses the driving capability of 10 LSTTL load. The M54/74HC688 compares bit for bit two 8-bit words applied on inputs P0 - P7 and inputs Q0 - Q7 and indicates whether or not they are equal. A single active low enable is provided to facilitate cascading several packages to enable comparison of words greater than 8 bits. All inputs are equipped with protection circuit against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT

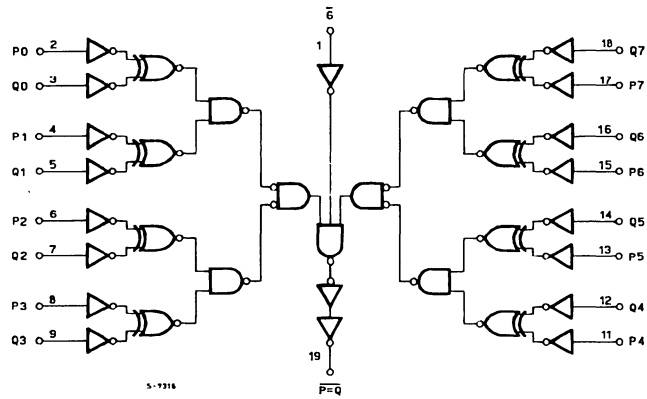


TRUTH TABLE

INPUT		OUTPUT
P, Q	$\overline{G}$	$\overline{P = Q}$
P = Q	L	L
P ≠ Q	L	H
X	H	H

X: DON'T CARE

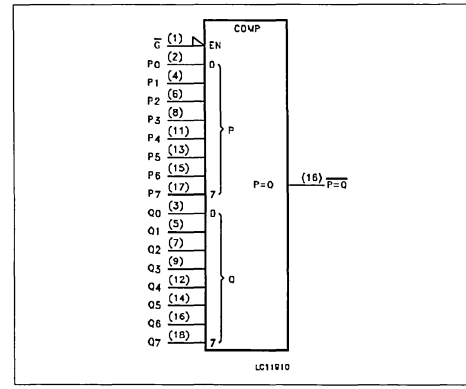
LOGIC DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{G}$	Enable Input (Active LOW)
2, 4, 6, 8, 11, 13, 15, 17	P0 to P7	Word Inputs
3, 5, 7, 9, 12, 14, 16, 18	Q0 to Q7	Word Outputs
19	$\overline{P = Q}$	Equal to Output
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

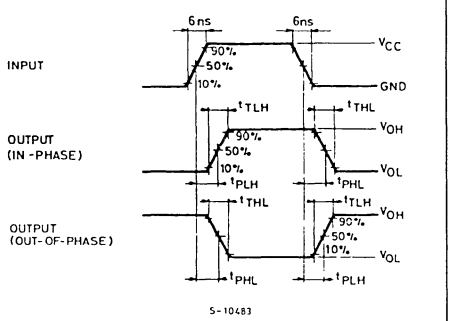
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

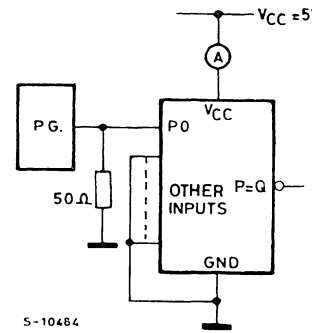
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (Pn, Qn - $\overline{P}$ = Q)	2.0			60	170		215		255	ns
		4.5			21	34		43		51	
		6.0			17	29		37		43	
t_{PLH} t_{PHL}	Propagation Delay Time (G - P = Q)	2.0			40	110		140		165	ns
		4.5			13	22		28		33	
		6.0			10	19		24		28	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				32						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit) Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT ICC (Opr.)



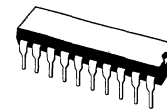
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

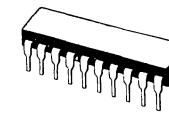
M54HCT688
M74HCT688

8 BIT EQUALITY COMPARATOR

- HIGH SPEED
  t_{PD} = 17 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS688



B1R
(Plastic Package)



F1R
(Ceramic Package)

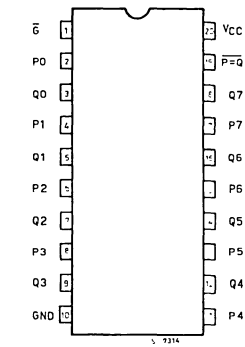
M1R
(Micro Package)

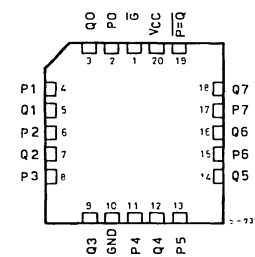
C1R
(Chip Carrier)

ORDER CODES :

M54HCT688F1R M74HCT688M1R
M74HCT688B1R M74HCT688C1R

PIN CONNECTIONS (top view)





NC =
No Internal
Connection

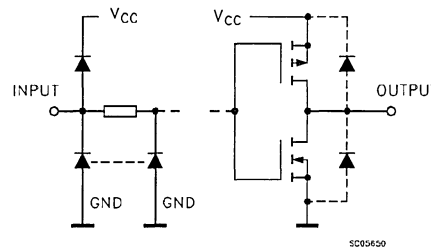
DESCRIPTION

The M54/74HCT688 utilizes silicon gate C^2MOS technology to achieve operating speeds equivalent to LSTTL devices. Along with the low power dissipation and high noise immunity of standard C^2MOS integrated circuit, it possesses the driving capability of 10 LSTTL load. The M54/74HCT688 compares bit for bit two 8-bit words applied on inputs P0 - P7 and inputs Q0 - Q7 and indicates whether or not they are equal. A single active low enable is provided to facilitate cascading several packages to enable comparison of words greater than 8 bits.

This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

All inputs are equipped with protection circuit against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT

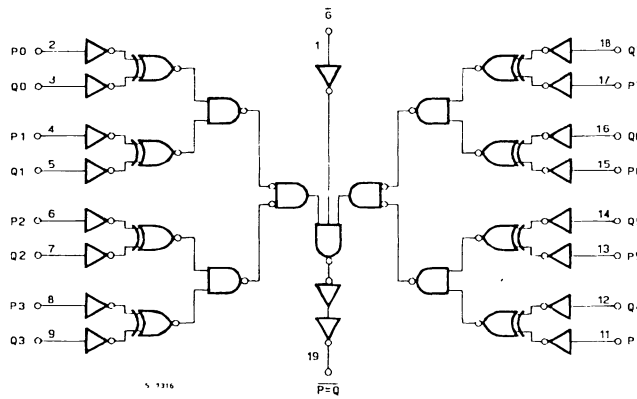


TRUTH TABLE

INPUT		OUTPUT
P, Q	$\overline{G}$	$\overline{P = Q}$
P = Q	L	L
P ≠ Q	L	H
X	H	H

X. DON'T CARE

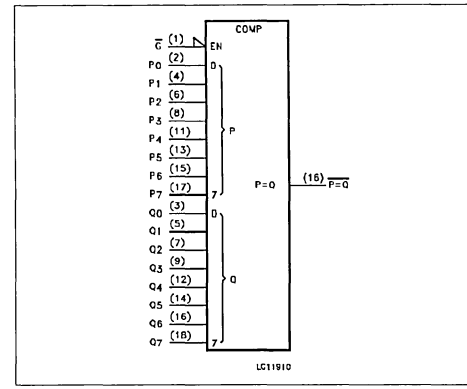
LOGIC DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{G}$	Enable Input (Active LOW)
2, 4, 6, 8, 11, 13, 15, 17	P0 to P7	Word Inputs
3, 5, 7, 9, 12, 14, 16, 18	Q0 to Q7	Word Outputs
19	$\overline{P = Q}$	Equal to Output
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied

(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

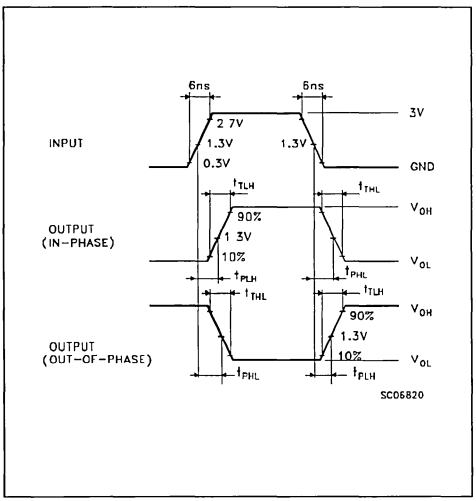
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				4		40		80	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND				2.0		2.9		3.0	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

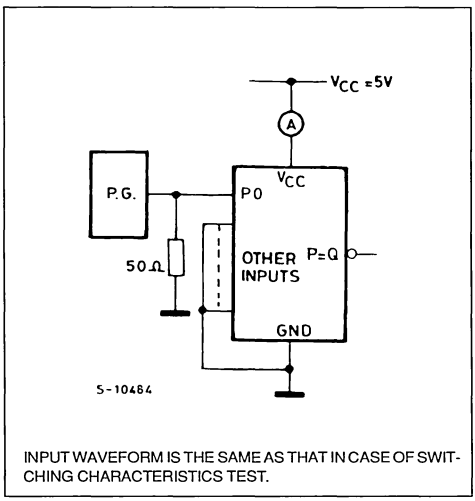
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			8	15		19		22	ns
t_{PLH} t_{PHL}	Propagation Delay Time (Pn, Qn - $\overline{P}$ = Q)	4.5			21	32		40		48	ns
t_{PLH} t_{PHL}	Propagation Delay Time (G - $\overline{P}$ = Q)	4.5			15	23		29		35	ns
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				32						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT ICC (Opr.)

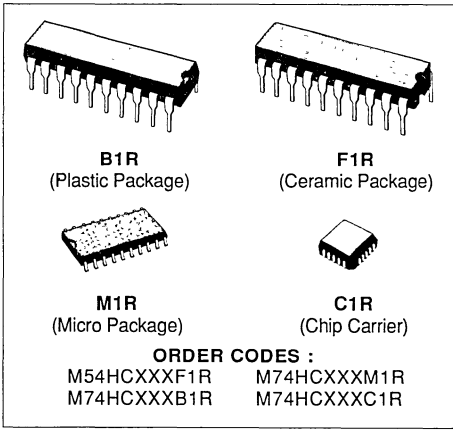


INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

M54/74HC690/691 M54/74HC692/693

HC690/692 DECADE COUNTER/REGISTER (3-STATE) HC691/693 4 BIT BINARY COUNTER/REGISTER (3-STATE)

- HIGH SPEED
  f_{MAX} = 50 MHz (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS (for Q_A to Q_D)
  10 LSTTL LOADS (for RCO)
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.) (for Q_A to Q_D)
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.) (for RCO)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V to 6 V
- PIN AND FUNCTION COMPATIBLE WITH LSTTL 54/74LS690/691



B1R (Plastic Package)

F1R (Ceramic Package)

M1R (Micro Package)

C1R (Chip Carrier)

ORDER CODES :

M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

DESCRIPTION

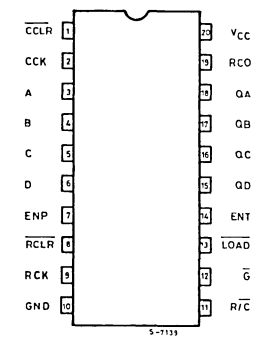
The HC690/691/692/693 are high speed CMOS COUNTER/REGISTER fabricated in silicon gate C^2MOS technology.

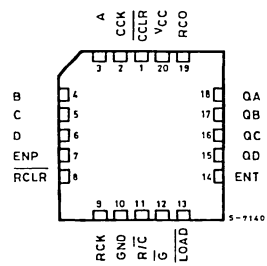
They have the same high speed performance of LSTTL combined with true CMOS low power consumption.

The internal circuit is composed of 3 stages including buffer output, which offers high noise immunity and stable output. These devices incorporate a synchronous counter, four-bit D-type register, and quadruple two-line to one-line multiplexers with three-state outputs in a single 20-pin package. The counter can be programmed from the data inputs and have enable P and enable T inputs and a ripple-carry output for easy expansion. The register/counter select input, R/$\overline{C}$, selects the counter when low or the register when high for the three-state outputs, QA, QB, QC, and QD.

If the LOAD input ($\overline{LOAD}$) is held "L" DATA input (A-D) are loaded in to the internal counter at positive edge of counter clock input ($\overline{CCK}$). In the counter mode, internal counter counts up at the positive of the counter clock. If the counter clear input ($\overline{CCLR}$) is held "L", the internal counter is cleared (synchronously to the counter clock for HC692/HC693, and asynchronously for HC690/HC691). The internal

PIN CONNECTIONS (top view)

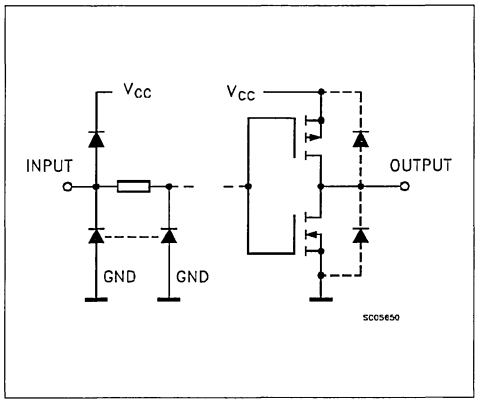




NC = No Internal Connection

counter's outputs are stored in the output register at the positive edge of the register clock (RCK). If the register clear input (RCLR) is held "L" the register is cleared (synchronously to register clock for HC692/HC693 and asynchronously for HC690/HC691). All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT

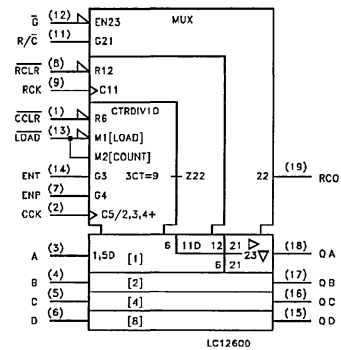


PIN DESCRIPTION

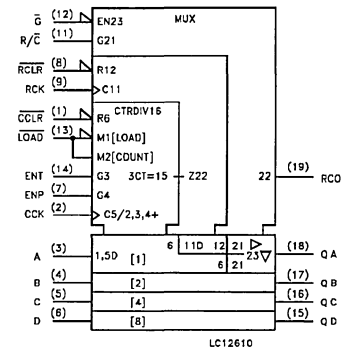
PIN No	SYMBOL	NAME AND FUNCTION
3 to 6	A to D	Data Inputs
7, 14	ENT, ENP	Enable Inputs
15 to 18	QA to QD	Data Outputs
1	$\overline{CCLR}$	Counter Clear (Active LOW)
2	CCK	Counter Clock
11	R/$\overline{C}$	Counter/ Register Select
8	$\overline{RCLR}$	Register Clear (Active LOW)
9	RCK	Register Clear
19	RCO	Ripple Counter Output
10	GND	Ground (0V)
20	Vcc	Positive Supply Voltage

IEC LOGIC SYMBOLS

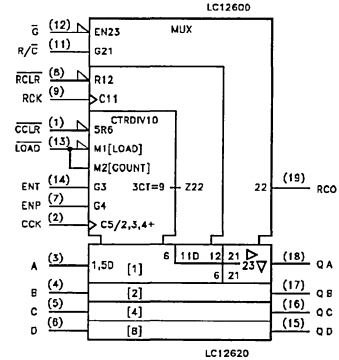
HC690



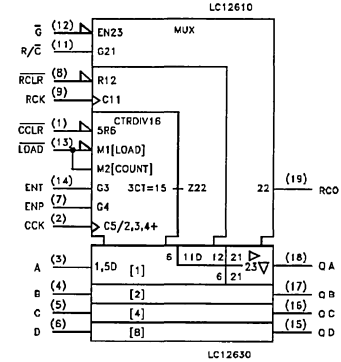
HC691



HC692



HC693

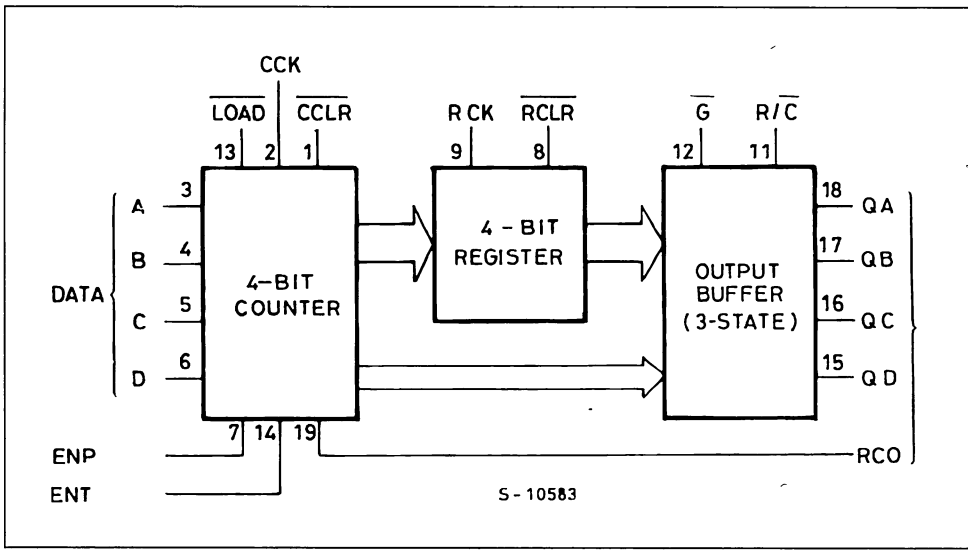


TRUTH TABLE

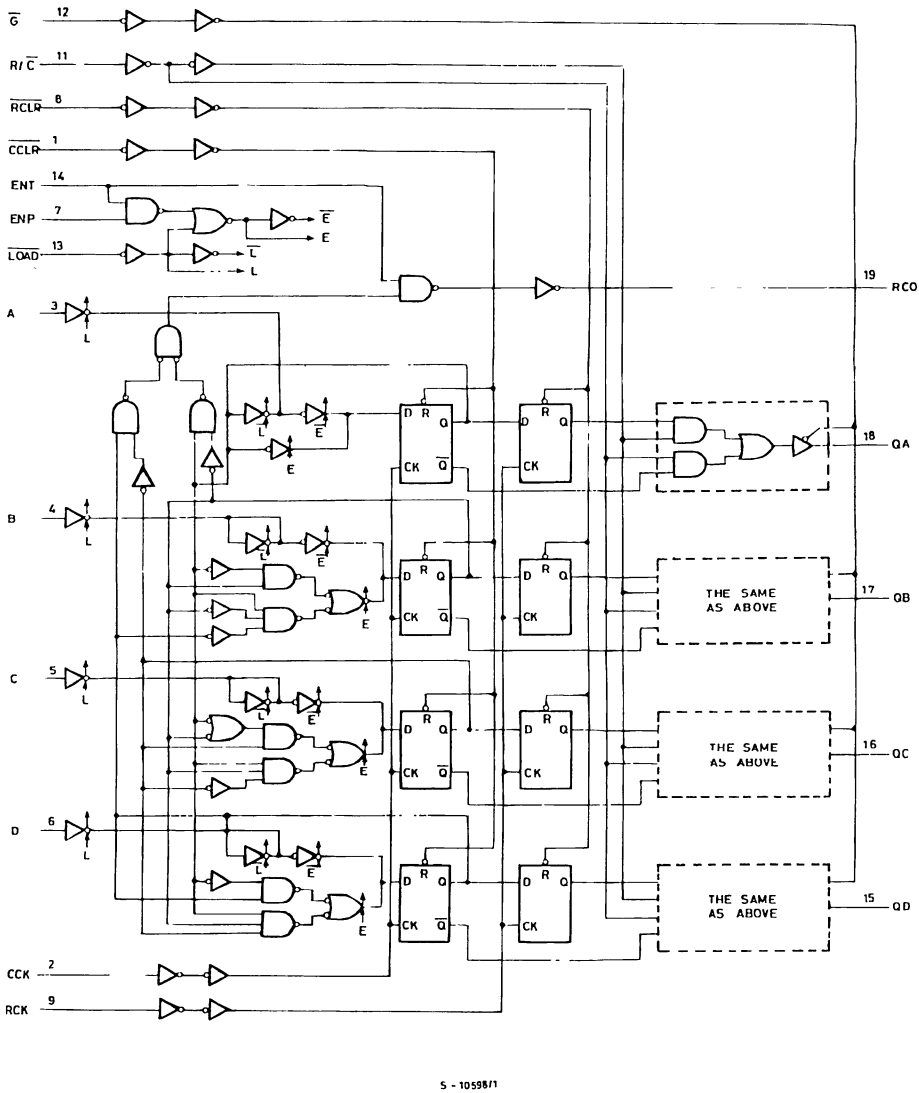
INPUTS									OUTPUS				FUNCTION
$\overline{CCLR}$	$\overline{LOAD}$	ENP	ENT	CCK	$\overline{RCLR}$	RCK	R/$\overline{C}$	$\overline{G}$	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	(*)	X	X	L	L	L	L	L	L	CLEAR COUNTER
H	L	X	X	⌐	X	X	L	L	a	b	c	d	LOAD COUNTER
H	H	L	X	⌐	X	X	L	L	NO CHANGE				NO COUNT
H	H	X	L	⌐	X	X	L	L	NO CHANGE				NO COUNT
H	H	H	H	⌐	X	X	L	L	COUNT UP				COUNT UP
H	X	X	X	⌐	X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	L	(*)	H	L	L	L	L	L	CLEAR REGISTER
X	X	X	X	X	H	⌐	H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	H	⌐	H	L	NO CHANGE				NO LOAD

(*) : X for HC690/691 ⌐ for HC692/693
X : DON'T CARE
Z : HIGH IMPEDANCE
a-d : THE LEVEL OF STEADY STATE INPUTS AT INPUTS A THROUGHT D RESPECTIVELY.
a'-d' : THE LEVEL OF STEADY STATE OUTPUTS AT INTERNAL COUNTER OUTPUTS a' through qd' respectively
HC690/692 RCO = QA • QD • ENT
HC691/693 RCO = QA • QB • QC • QD • ENT

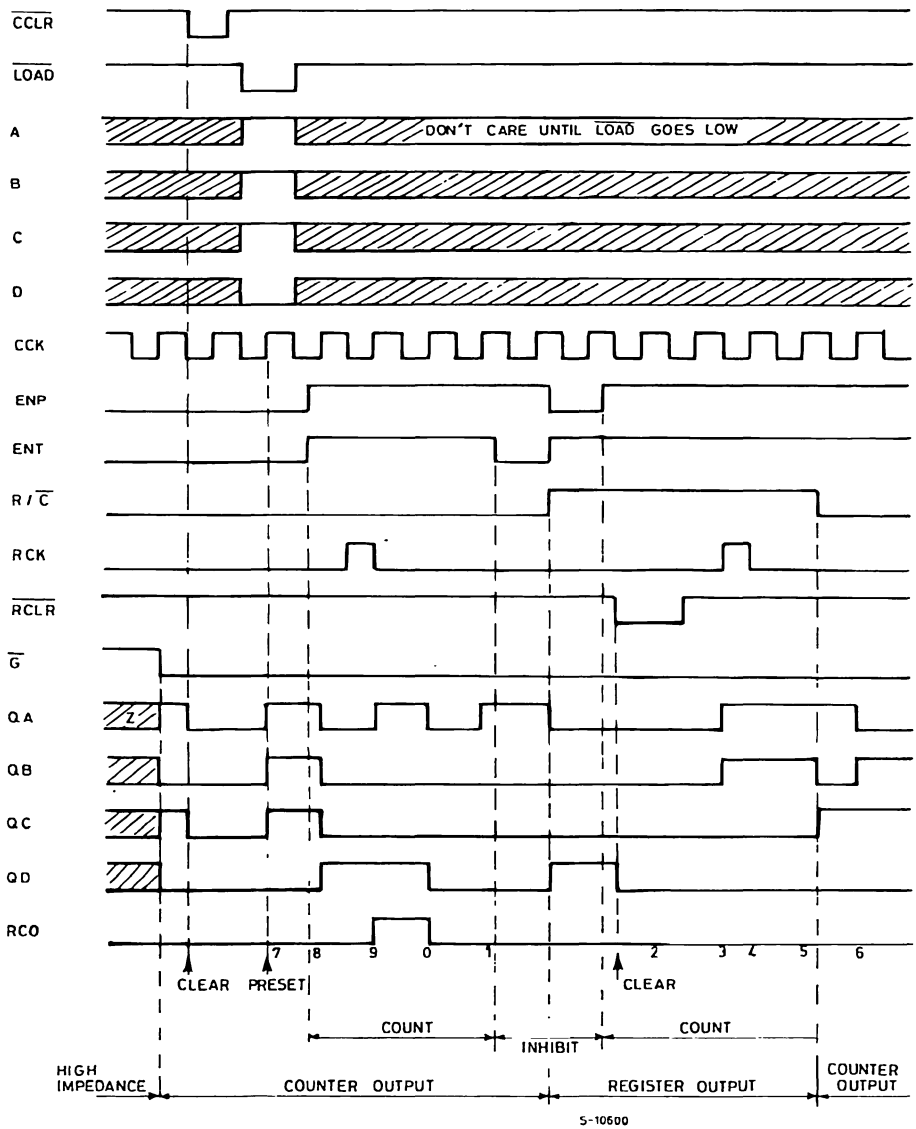
BLOCK DIAGRAM



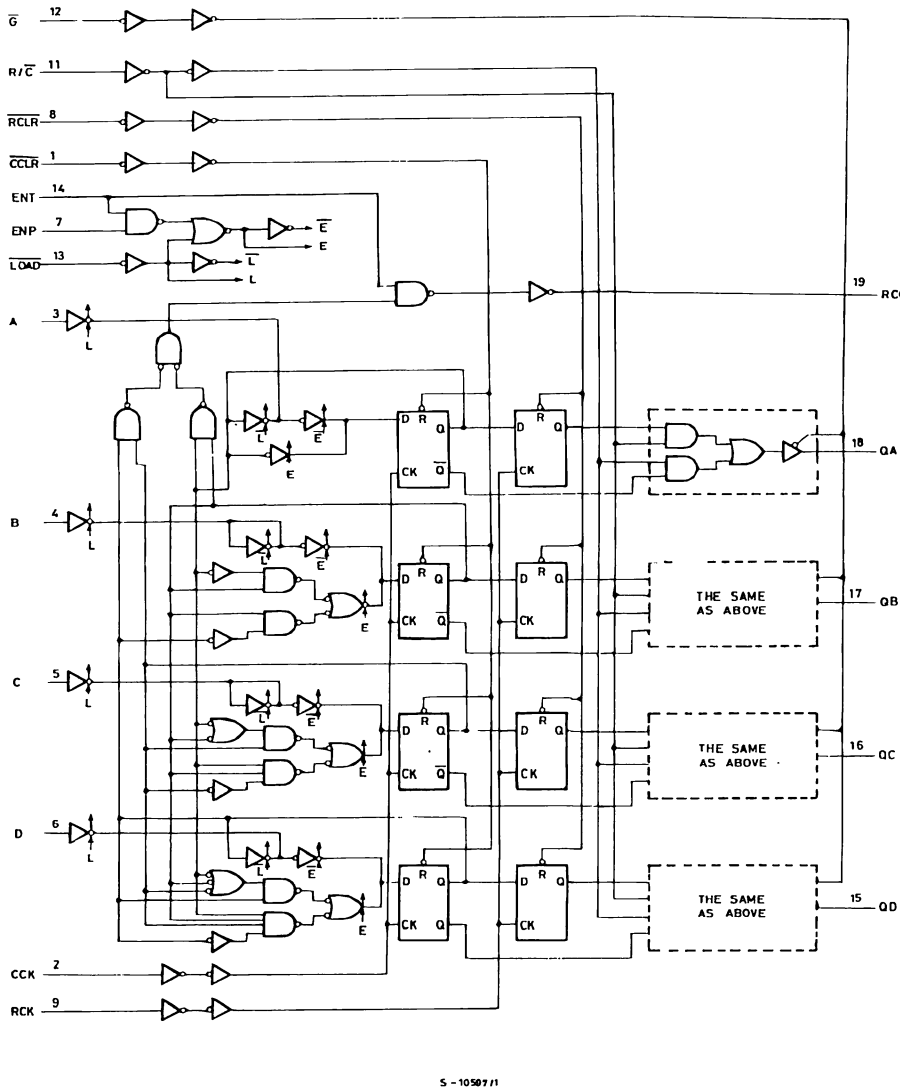
LOGIC DIAGRAM (HC690)



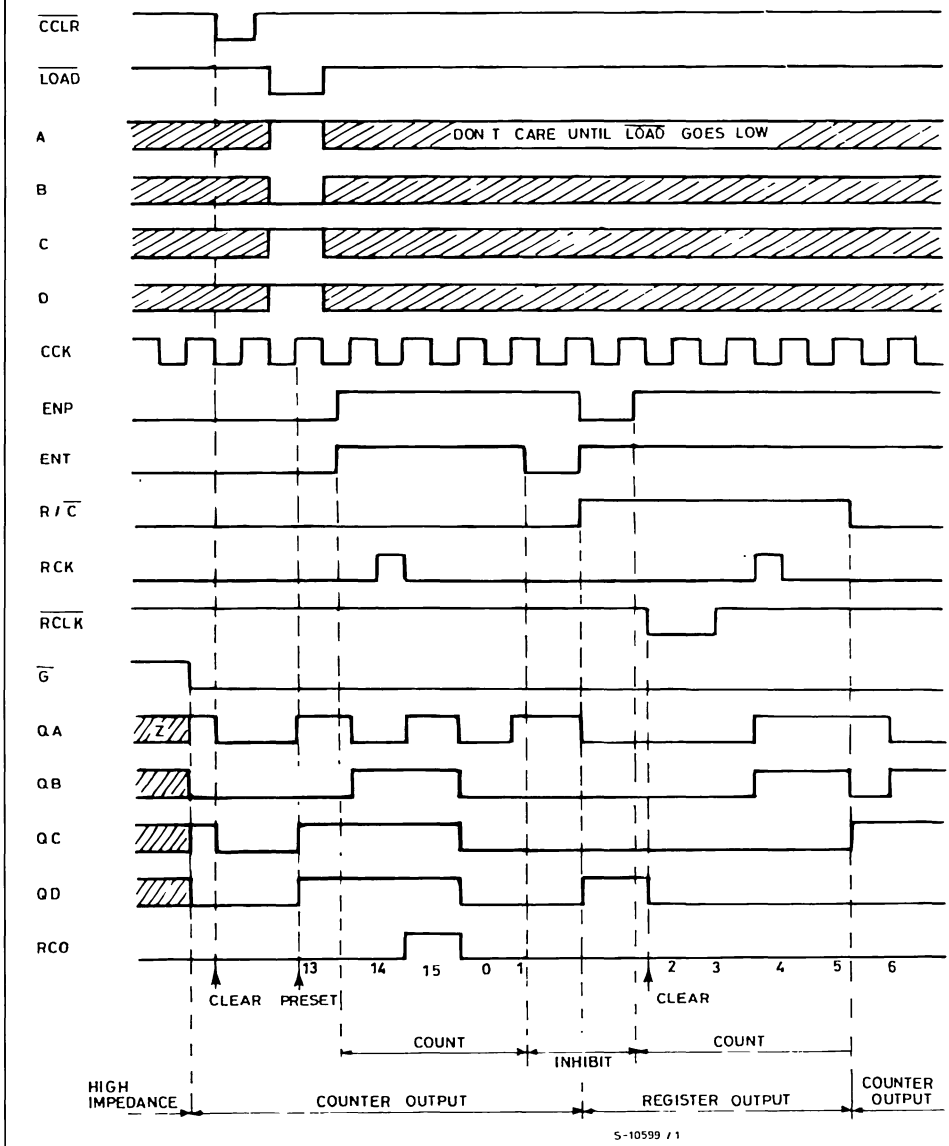
TIMING CHART (HC690)



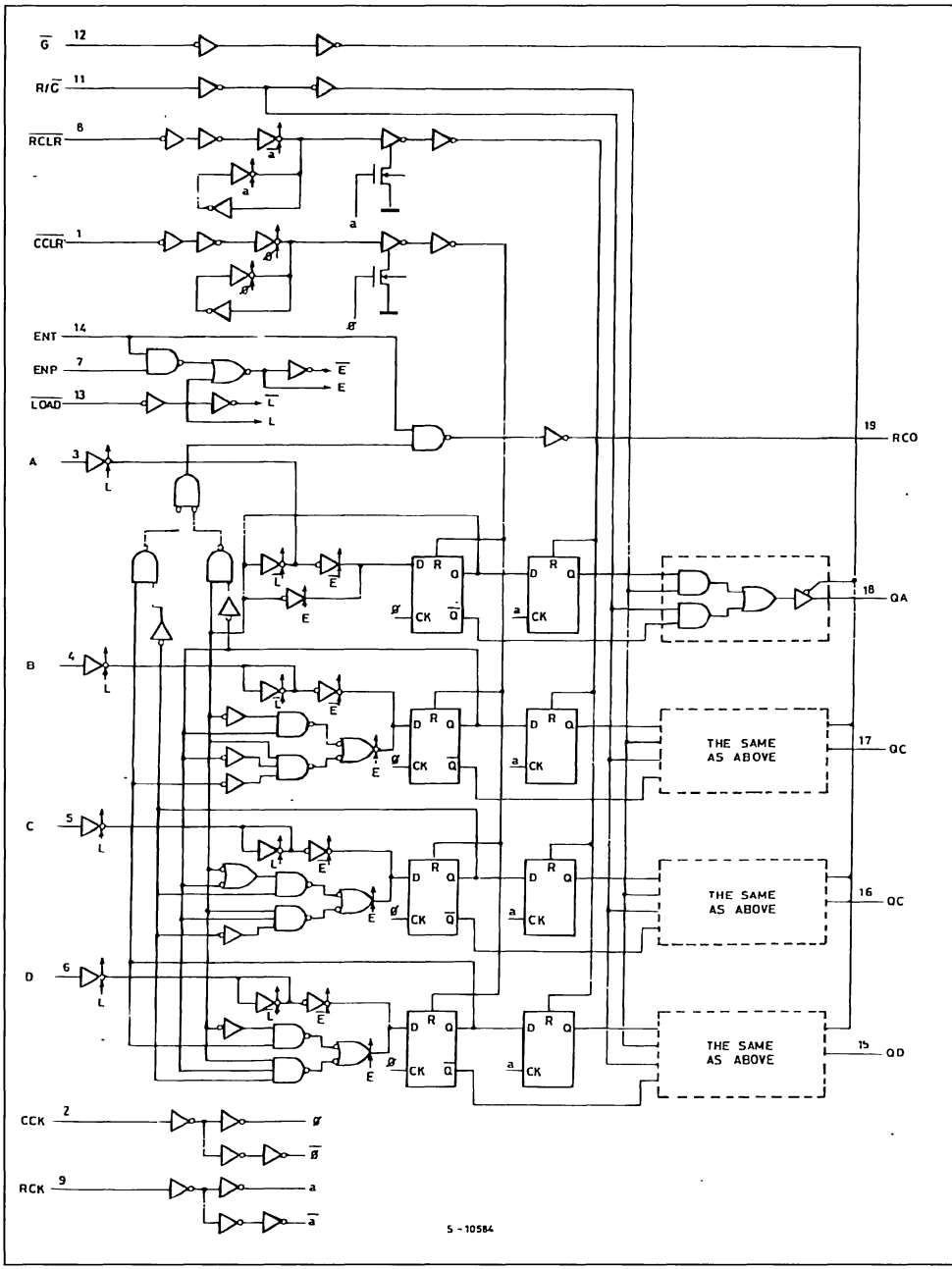
LOGIC DIAGRAM (HC691)



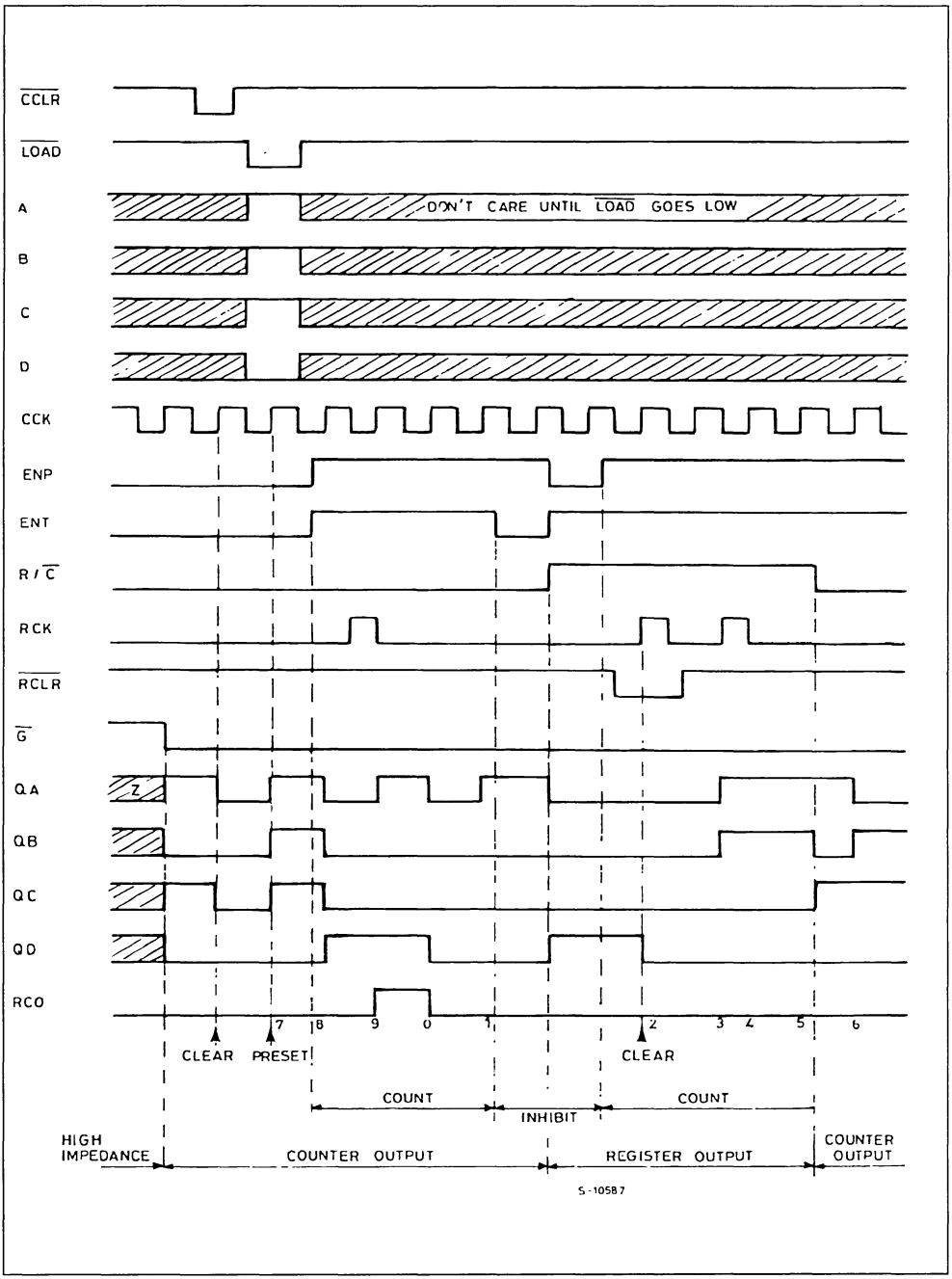
TIMING CHART (HC691)



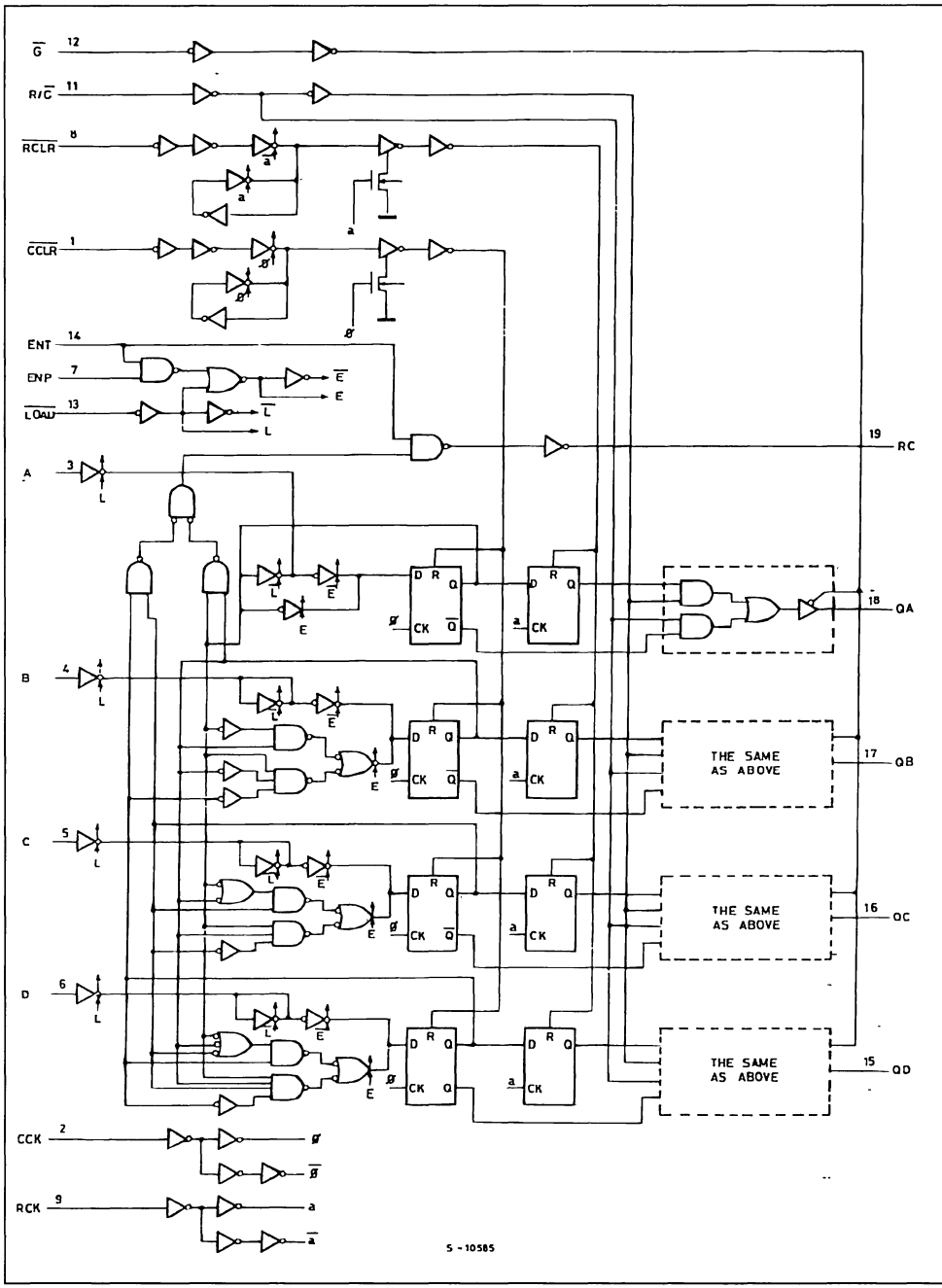
LOGIC DIAGRAM (HC692)



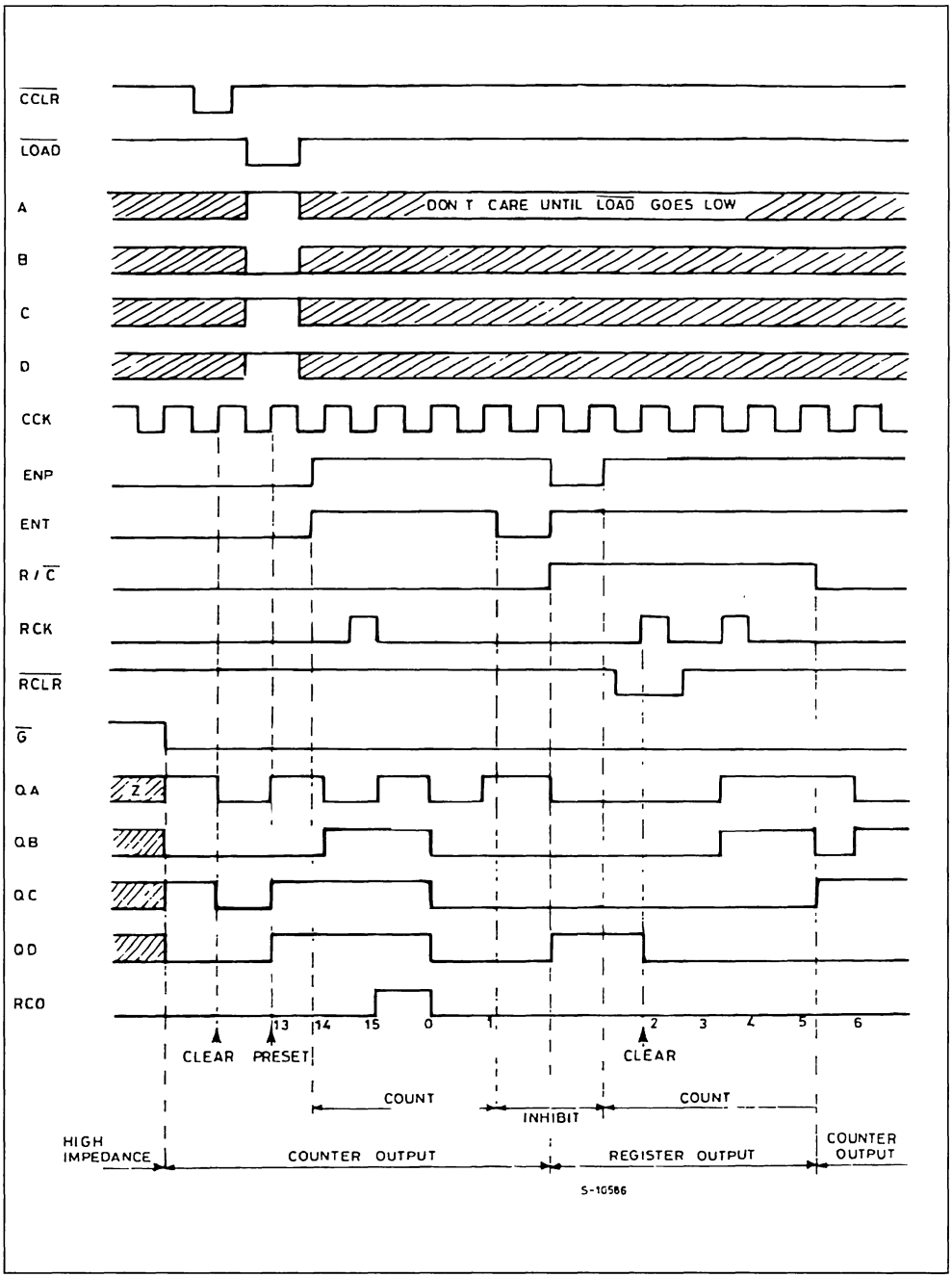
TIMING CHART (HC692)



LOGIC DIAGRAM (HC693)



TIMING CHART (HC693)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		-0.5 to +7	V
V_I	DC Input Voltage		-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage		-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current		± 20	mA
I_{OK}	DC Output Diode Current		± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	RCO	± 25	mA
		QA to QD	± 35	
I_{CC} or I_{GND}	DC V_{CC} or Ground Current		± 70	mA
P_D	Power Dissipation		500 (*)	mW
T_{stg}	Storage Temperature		-65 to +150	°C
T_L	Lead Temperature (10 sec)		300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied

(*) 500 mW. ≡ 65 °C derate to 300 mW by 10mW/°C. 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series		-55 to +125	°C
	M74HC Series		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage (QA - QD)	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OH}	High Level Output Voltage (RCO)	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage (QA - QD)	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.37		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.37		0.40	
V_{OL}	Low Level Output Voltage (RCO)	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.37		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.37		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5.0		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

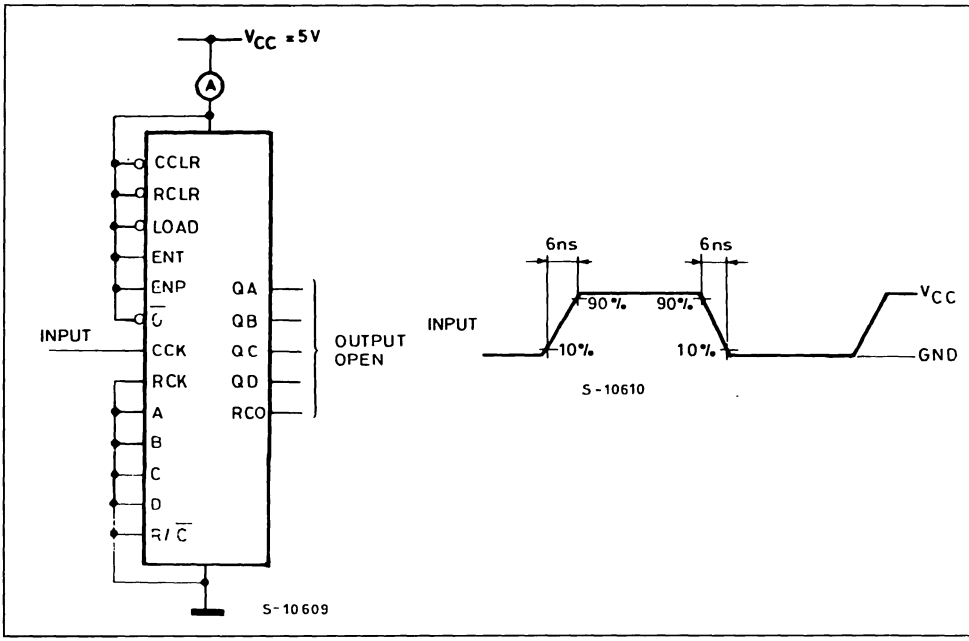
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time (Q)	2.0	50			25	60		75		90	ns
		4.5				7	12		15		19	
		6.0				6	10		13		15	
t_{TLH} t_{THL}	Output Transition Time (RCO)	2.0	50			30	75		95		115	ns
		4.5				8	15		19		23	
		6.0				7	13		16		20	
t_{PLH} t_{PHL}	Propagation Delay Time (CCK - Q)	2.0	50			82	205		255		310	ns
		4.5				26	41		51		62	
		6.0				22	35		43		53	
		2.0	150			95	235		295		255	ns
		4.5				30	47		59		71	
		6.0				26	40		50		60	
t_{PLH} t_{PHL}	Propagation Delay Time (RCK - Q)	2.0	50			86	210		265		315	ns
		4.5				27	42		53		63	
		6.0				23	36		45		54	
		2.0	150			99	240		300		360	ns
		4.5				31	48		60		72	
		6.0				26	41		51		61	
t_{PLH} t_{PHL}	Propagation Delay Time (CCK - RCO)	2.0	50			65	165		205		250	ns
		4.5				21	33		41		50	
		6.0				18	28		35		43	
t_{PLH} t_{PHL}	Propagation Delay Time (R/C - Q)	2.0	50			59	145		180		220	ns
		4.5				18	29		36		44	
		6.0				15	25		31		37	
		2.0	150			72	175		220		265	ns
		4.5				22	35		44		53	
		6.0				19	30		37		45	
t_{PLH} t_{PHL}	Propagation Delay Time (ENT - RCO)	2.0	50			36	100		125		150	ns
		4.5				12	20		25		30	
		6.0				10	17		21		26	
t_{PHL}	Propagation Delay Time ($\overline{CCLR}$ - Q) (for HC690/691)	2.0	50			91	225		280		340	ns
		4.5				29	45		56		68	
		6.0				25	38		48		58	
		2.0	150			104	255		320		385	ns
		4.5				33	51		64		77	
		6.0				28	43		54		65	
t_{PHL}	Propagation Delay Time ($\overline{RCLR}$ - Q) (for HC690/691)	2.0	50			86	210		265		315	ns
		4.5				27	42		53		63	
		6.0				23	36		45		54	
		2.0	150			100	240		300		360	ns
		4.5				31	48		60		72	
		6.0				26	41		51		61	
t_{PHL}	Propagation Delay Time ($\overline{CCLR}$ - RCO) (for HC690/691)	2.0	50			70	175		220		265	ns
		4.5				22	35		44		53	
		6.0				19	30		37		45	

AC ELECTRICAL CHARACTERISTICS (Continued)

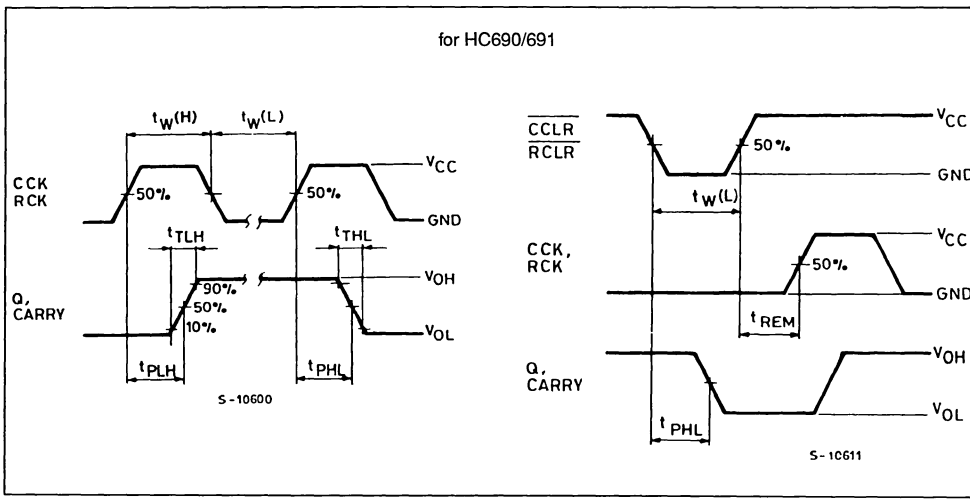
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}	Maximum Clock Frequency	2.0	50		4.4	12		3.6		3		MHz
		4.5			22	45		18		15		
		6.0			26	53		21		18		
t_{PZL} t_{PZH}	Output Enable Time	2.0	50	R_L = 1 KΩ		48	120		150		180	ns
		4.5				15	24		30		36	
		6.0				13	20		26		31	
		2.0	150	R_L = 1 KΩ		61	150		190		225	ns
		4.5				19	30		38		45	
		6.0				17	26		32		38	
t_{PLH} t_{PHL}	Output Disable Time	2.0	50	R_L = 1 KΩ		32	145		180		220	ns
		4.5				15	29		36		44	
		6.0				13	25		31		37	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CCK - RCK)	2.0	50			28	75		95		110	ns
		4.5				7	15		19		22	
		6.0				6	13		16		19	
$t_{W(L)}$	Minimum Pulse Width $\overline{(CCLR - RCLR)}$ (for HC690/691)	2.0	50			40	75		95		110	ns
		4.5				8	15		19		22	
		6.0				7	13		16		19	
t_s	Minimum Set-up Time (LOAD, ENT, ENP)	2.0	50			68	150		190		220	ns
		4.5				17	30		38		44	
		6.0				14	26		32		37	
t_s	Minimum Set-up Time (A, B, C, D)	2.0	50			44	100		125		145	ns
		4.5				11	20		25		29	
		6.0				9	17		21		25	
t_s	Minimum Set-up Time $\overline{(CCLR, RCLR)}$ (for HC692/693)	2.0	50			44	100		125		145	ns
		4.5				11	20		25		29	
		6.0				9	17		21		25	
t_s	Minimum Set-up Time (CCK, RCK)	2.0	50			48	125		155		180	ns
		4.5				12	25		31		36	
		6.0				10	21		26		31	
t_h	Minimum Hold Time	2.0	50				0		0		0	ns
		4.5					0		0		0	
		6.0					0		0		0	
t_{REM}	Minimum Removal Time (for HC690/691)	2.0	50				25		30		40	ns
		4.5					5		6		8	
		6.0					5		5		7	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance		for HC690/691 for HC692/693			70 80						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

TEST CIRCUIT I_{CC} (Opr.)

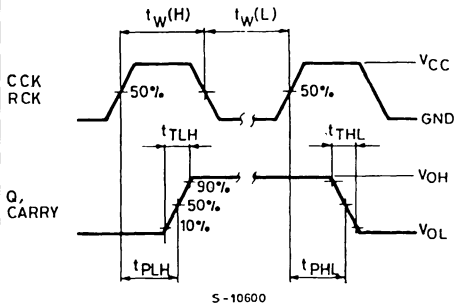


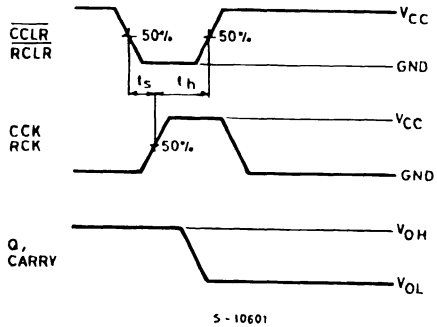
SWITCHING CHARACTERISTICS TEST WAVEFORM



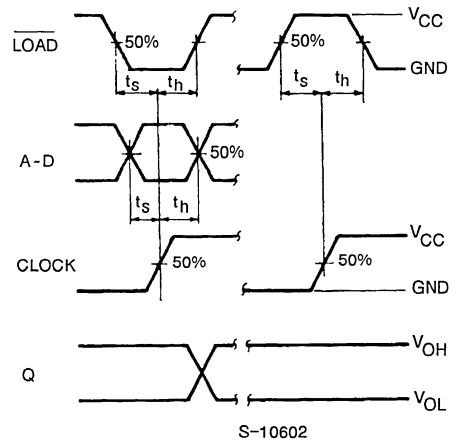
SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)

for HC692/693

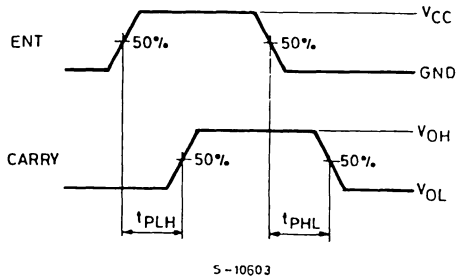


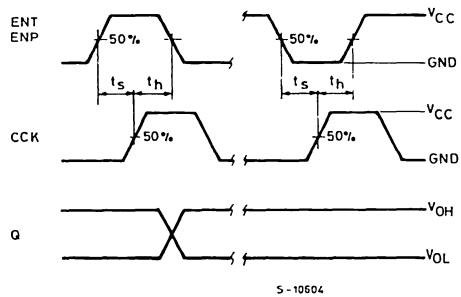


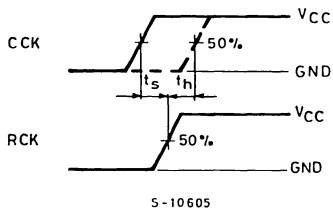
for ALL TYPES



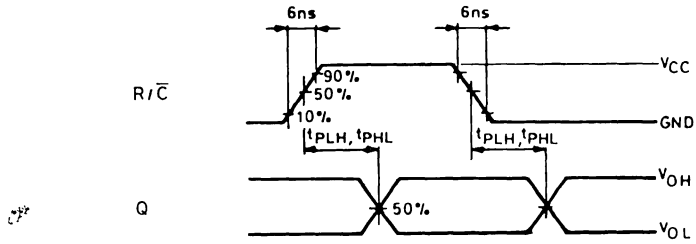
(Fix Maximum Count)







SWITCHING CHARACTERISTICS (continued)



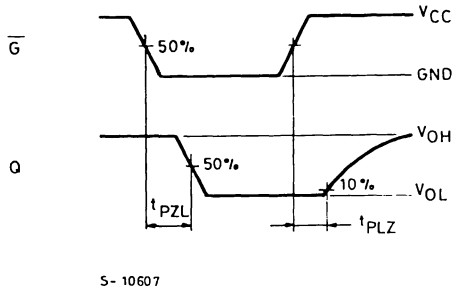
S-10606

t_{PLZ}, t_{PZL}

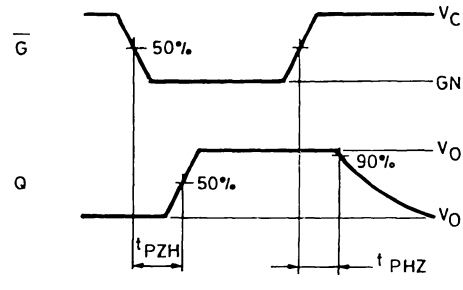
The 1 kΩ load resistors should be connected between outputs and V_{CC} line and the 50 pF load capacitors should be connected between outputs and GND line. All inputs except $\overline{G}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{G}$ input is held low.

t_{PHZ}, t_{PZH}

The 1 kΩ load resistors and the 50 pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{G}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{G}$ input is held low.



S-10607



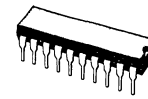
S-10608

SGS-THOMSON MICROELECTRONICS

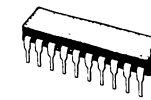
M54/74HC696/697
M54/74HC698/699

HC696/698 U/D DECADE COUNTER/REGISTER (3-STATE)
HC697/699 U/D 4 BIT BINARY COUNTER/REGISTER (3-STATE)

- HIGH SPEED
  f_{MAX} = 50 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS (for Q_A to Q_D)
  10 LSTTL LOADS (for RCO)
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.) FOR Q_A TO Q_D
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.) FOR RCO OUTPUT
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH LSTTL 54/74LS696/697/698/699



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HCXXXF1R	M74HCXXXM1R
M74HCXXXB1R	M74HCXXXC1R

DESCRIPTION

The HC696/697 are high speed CMOS up/down counters fabricated with silicon gate C^2MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The HC696/698 are BCD DECADE COUNTER, and the HC697/699 are 4-BIT BINARY COUNTER. Both devices have register.

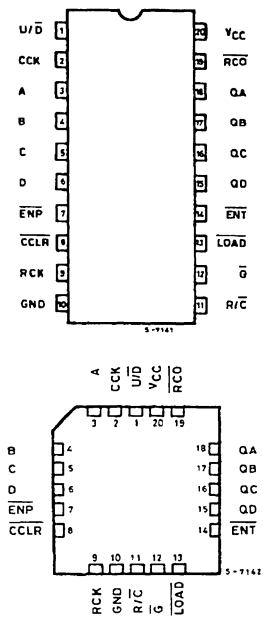
They count on the positive edge of the counter clock input (CCK) when selected by the "Counter Mode". If the input U/$\overline{D}$ is held "H", the internal counter counts up, and held "L", counts down. The internal counter's outputs are stored in the output register at the positive edge of register clock (RCK).

The counter features enable P and enable T and a ripple-carry output for easy expansion. the register/counter select input, R/C, selects the counter when low or the register when high for the three state outputs, QA, QB, Qc and QD.

Both the counter clock CCK and register clock RCK are positive-edge triggered. The counter clear CCLR is active low and is synchronous for HC698/699, and asynchronous for HC696/697.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)

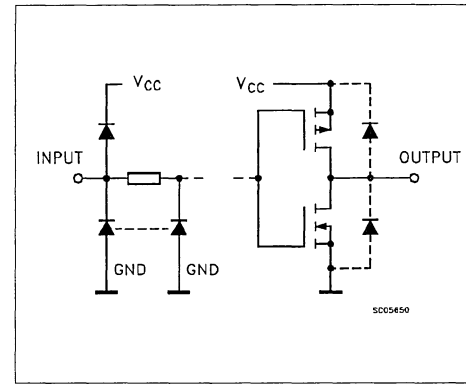


NC =
No Internal
Connection

PIN DESCRIPTION

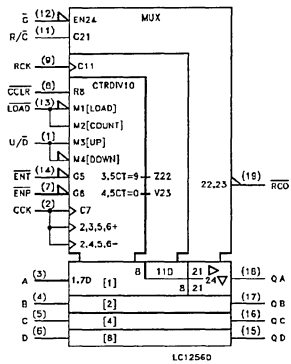
PIN No	SYMBOL	NAME AND FUNCTION
1	U/$\overline{D}$	Up Down Counter Selector
2	CCK	Counter Clock
3, 4, 5, 6	A to D	Data Inputs
7, 14	$\overline{EMP}$/$\overline{ENT}$	Enable $\overline{P}$ and $\overline{T}$
8	$\overline{CCLR}$	Counter Clear (Active LOW)
9	RCK	Register Clock
11	R/$\overline{C}$	Register Counter Selector
12	$\overline{G}$	Enable Input
13	LOAD	Load Counter (Active LOW)
15, 16, 17, 18	QA to QD	Data Outputs
19	$\overline{RCO}$	Load Counter (Active HIGH)
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

INPUT AND OUTPUT EQUIVALENT CIRCUIT

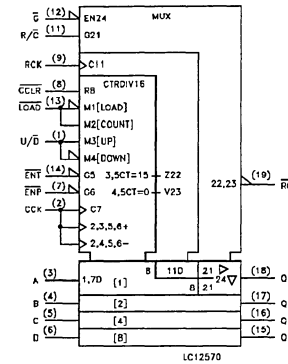


IEC LOGIC SYMBOL

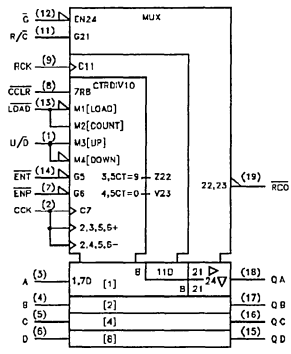
HC696



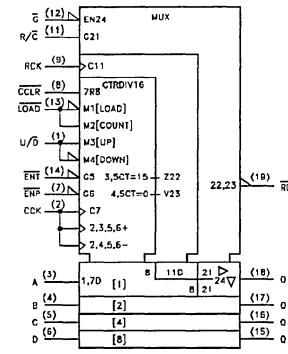
HC697



HC698



HC699



TRUTH TABLE

INPUTS									OUTPUTS				FUNCTION
$\overline{CCLR}$	$\overline{LOAD}$	$\overline{ENP}$	$\overline{ENT}$	CCK	U/$\overline{D}$	RCK	R/$\overline{C}$	$\overline{G}$	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	X (*)	X	X	L	L	L	L	L	L	CLEAR COUNTER
H	L	X	X	⎍	X	X	L	L	a	b	c	d	LOAD COUNTER
H	H	H	X	⎍	X	X	L	L	NO CHANGE				NO COUNT
H	H	X	H	⎍	X	X	L	L	NO CHANGE				NO COUNT
H	H	L	L	⎍	H	X	L	L	COUNT UP				COUNT UP
H	H	L	L	⎍	L	X	L	L	COUNT DOWN				COUNT DOWN
H	X	X	X	⎎	X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	X	⎍	H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	X	⎎	H	L	NO CHANGE				NO LOAD

(*) : ⎍ For HC698/699

X : Don't care

Z : High impedance

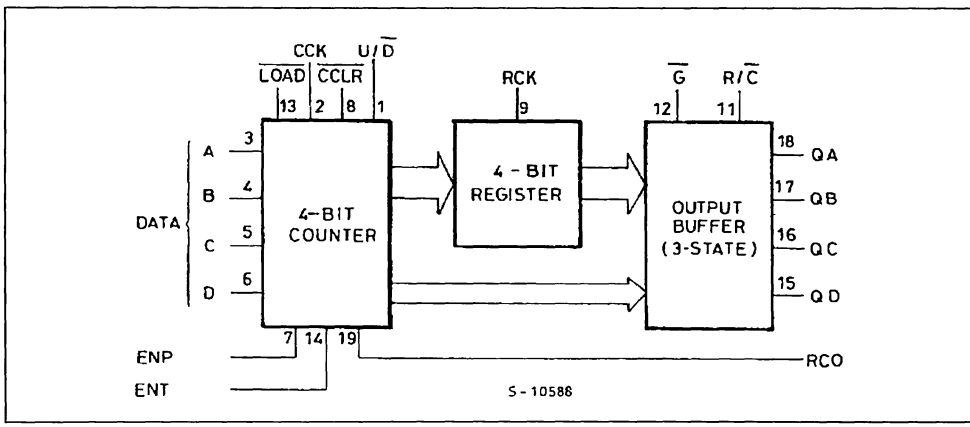
a-d : The level of steady state input at inputs a through D respectively

a'-d' : The level of steady state outputs at internal counter outputs QA' through QD' respectively

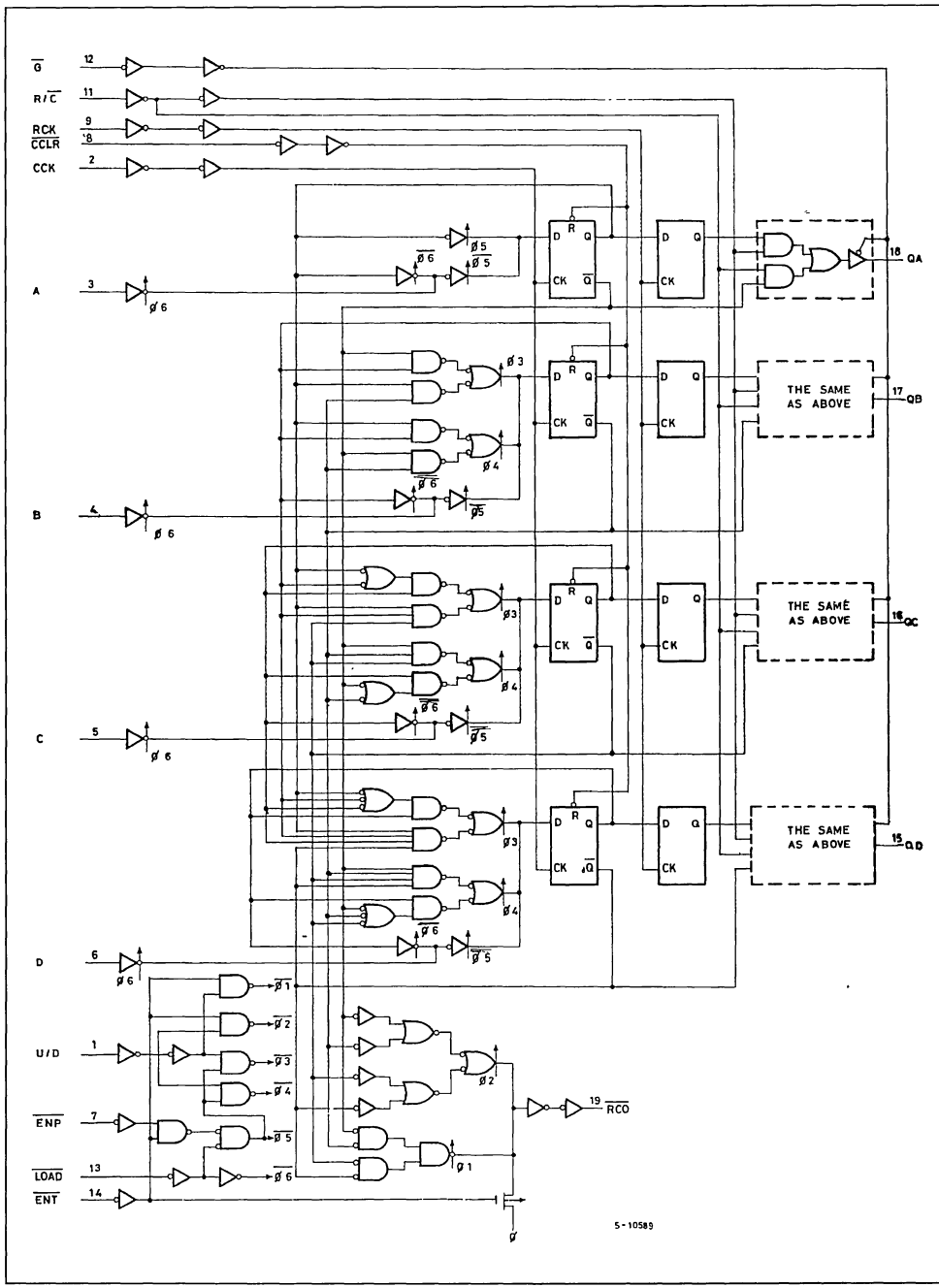
$\overline{RCO}$ function : HC696/8 - $\overline{RCO} = \overline{(UP \bullet QA \bullet QD \bullet ENT + \overline{UP} \bullet \overline{QA} \bullet \overline{QD} \bullet ENT)}$

HC697/9 - $\overline{RCO} = \overline{(UP \bullet QA \bullet QB \bullet QC \bullet QD \bullet ENT + \overline{UP} \bullet \overline{QA} \bullet \overline{QB} \bullet \overline{QC} \bullet \overline{QD} \bullet ENT)}$

BLOCK DIAGRAM

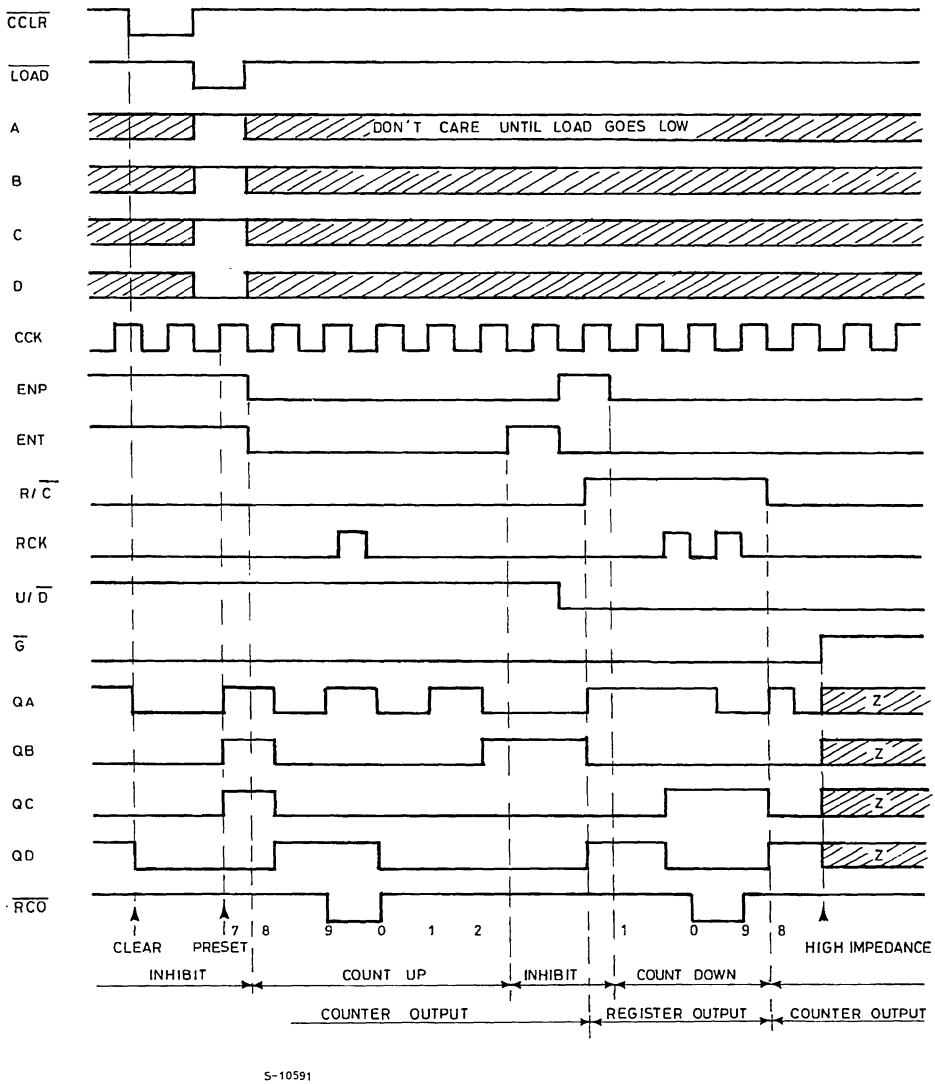


LOGIC DIAGRAM (HC696)

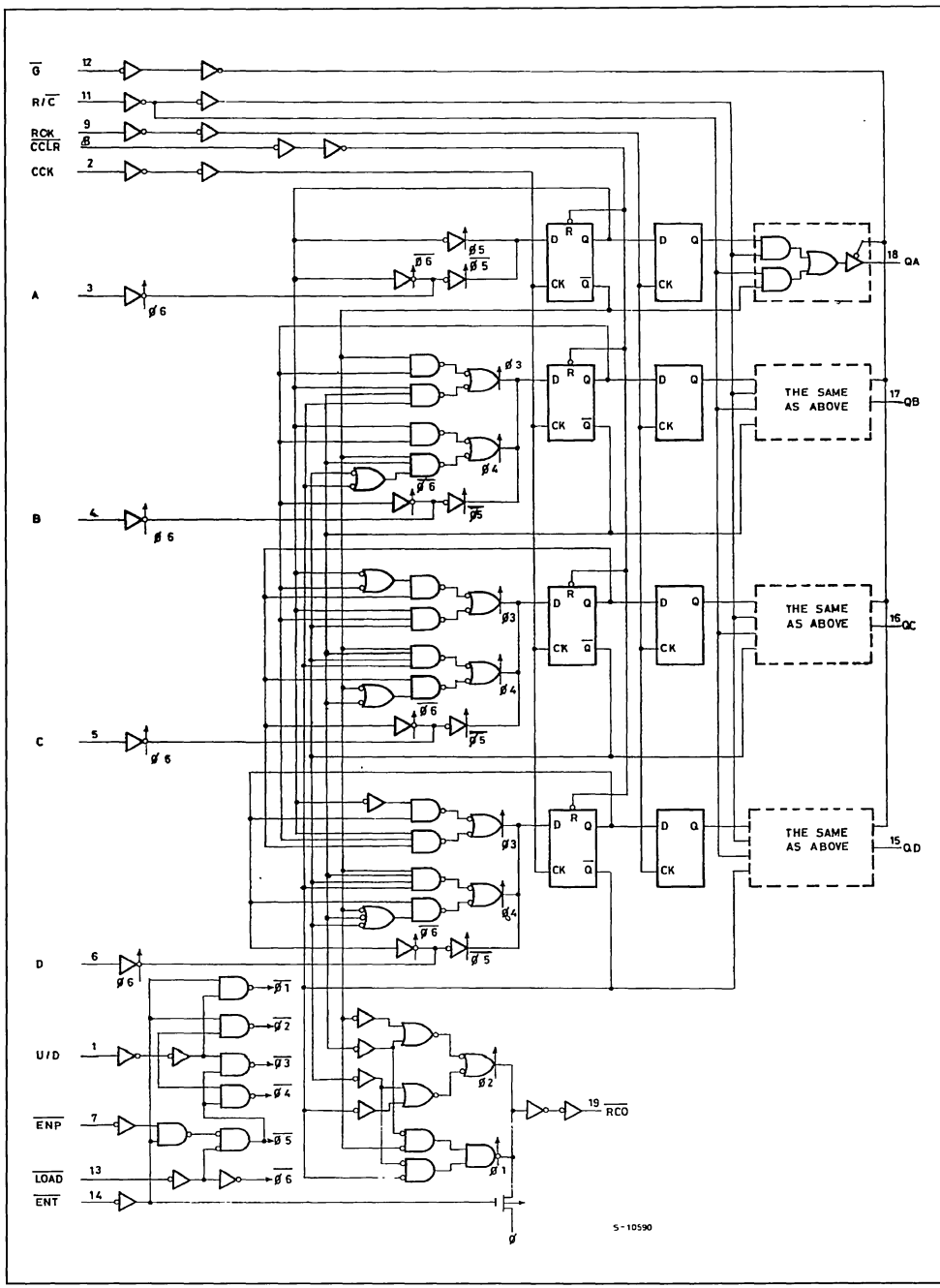


SGS-THOMSON MICROELECTRONICS

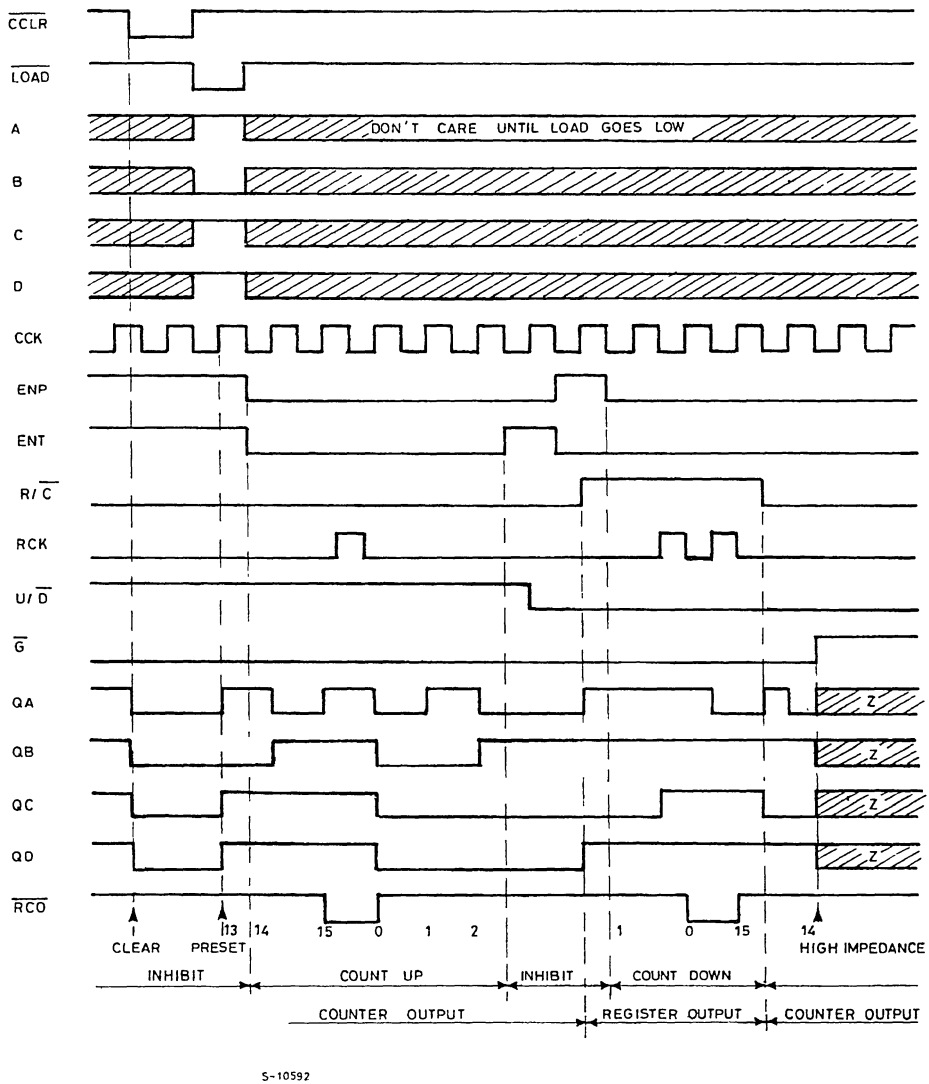
TIMING CHART (HC696)



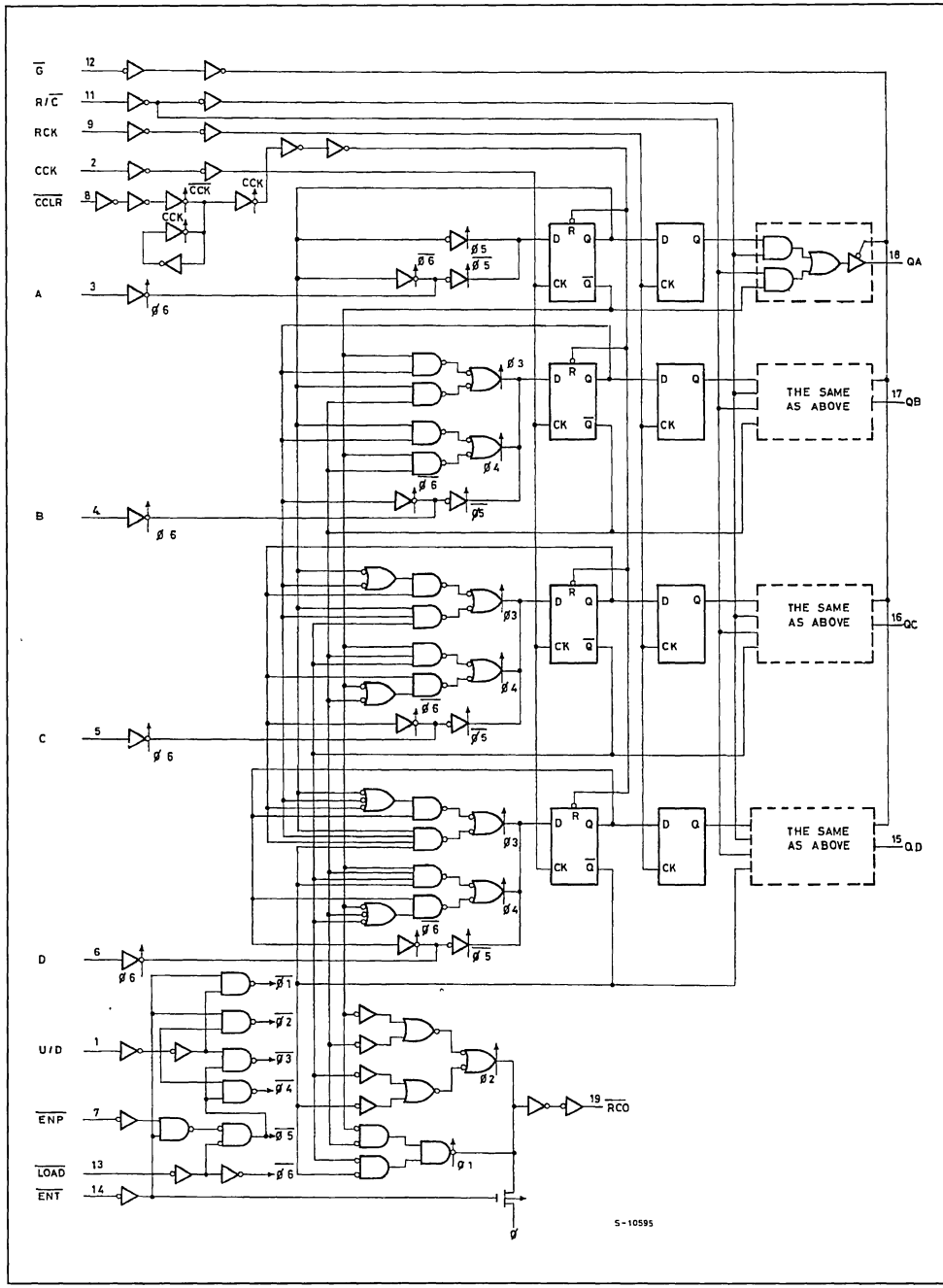
LOGIC DIAGRAM (HC697)



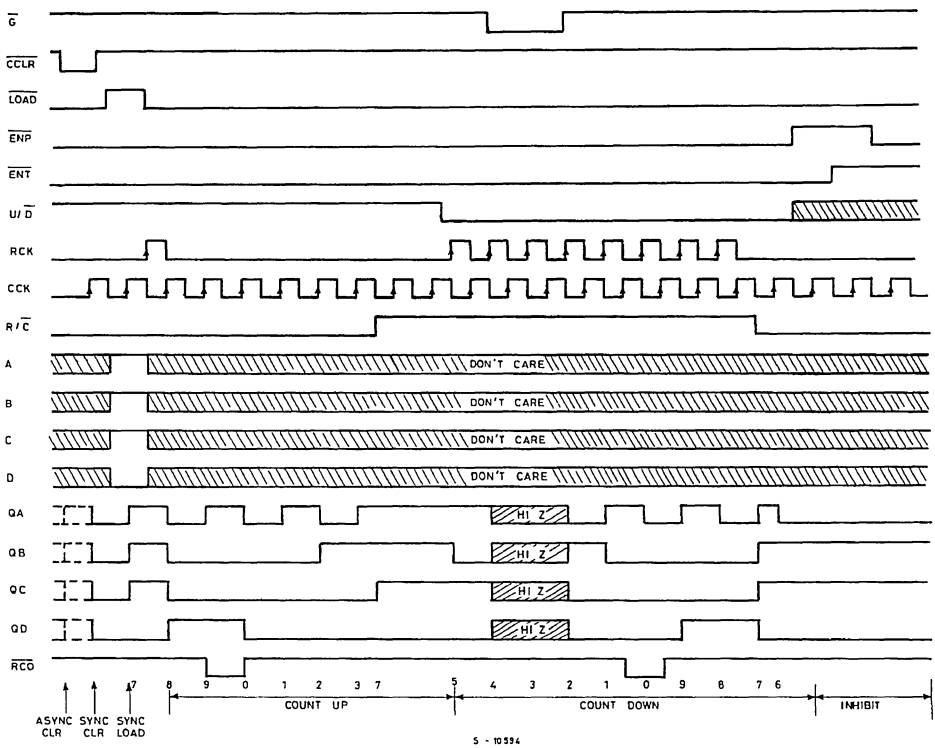
TIMING CHART (HC697)



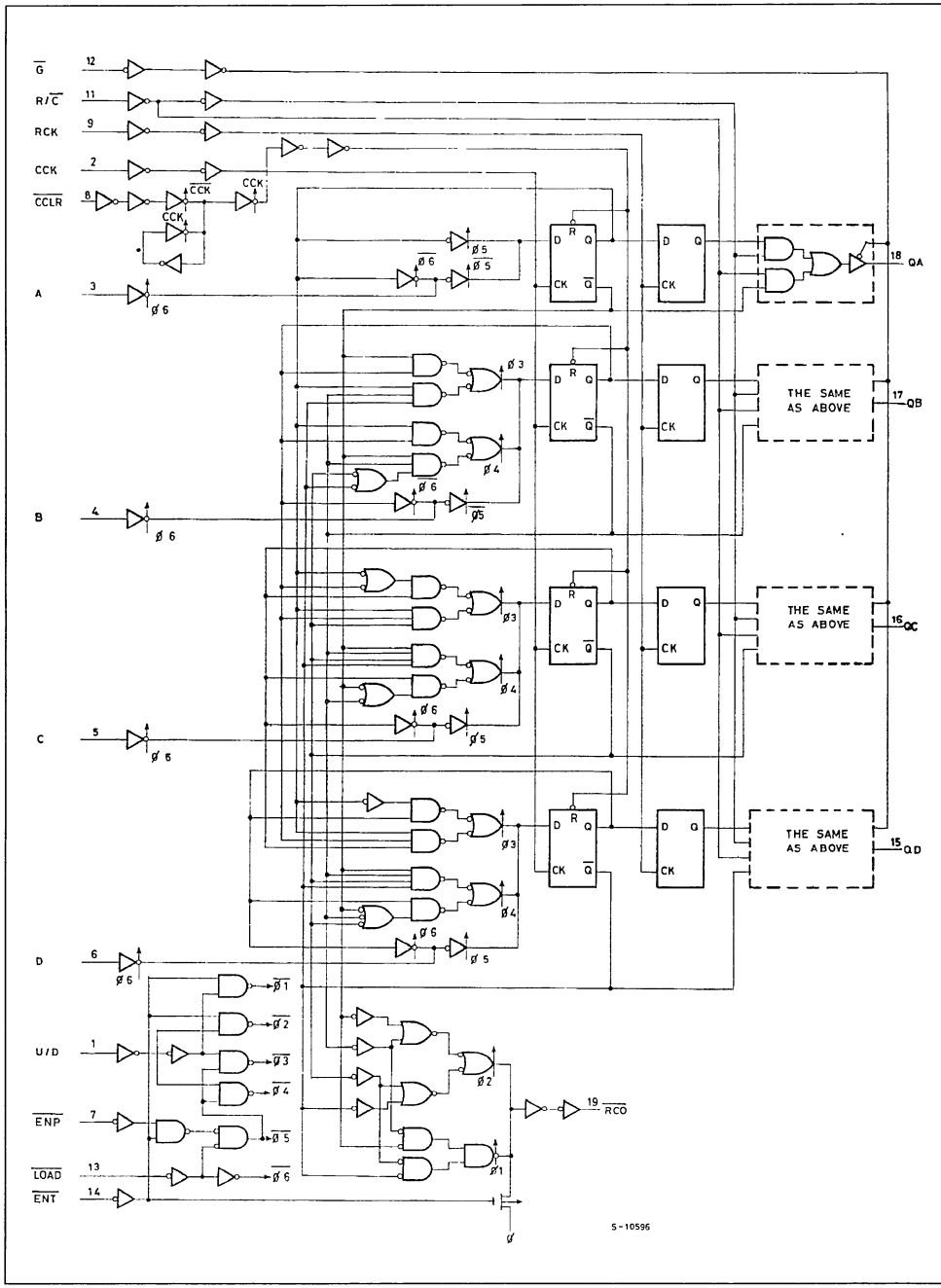
LOGIC DIAGRAM (HC698)



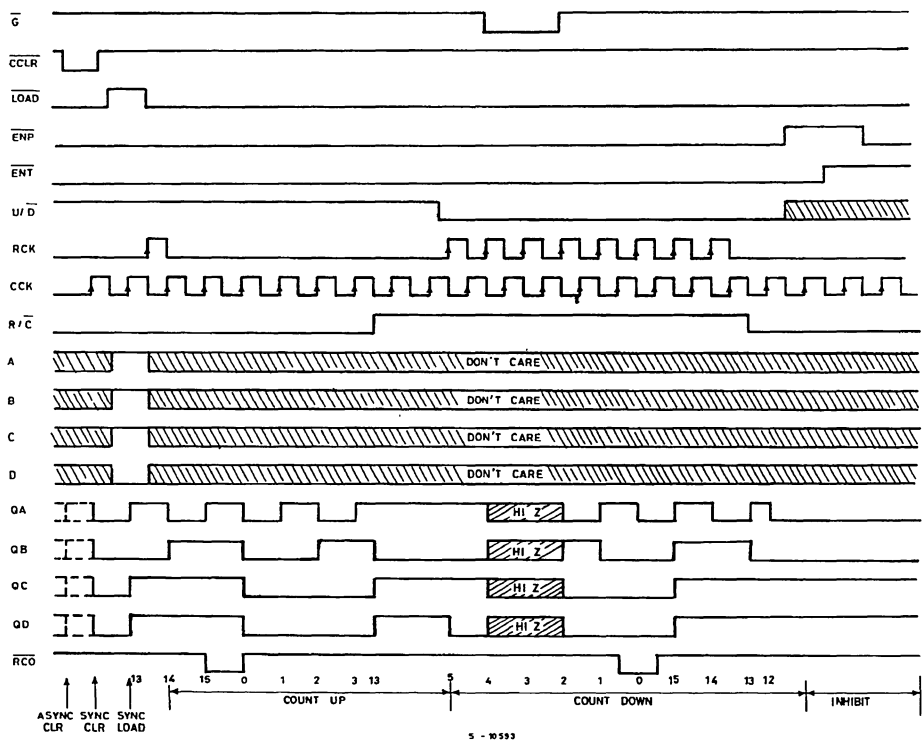
DECADE COUNTER, SYNCHRONOUS CLEAR (HC698)



LOGIC DIAGRAM (HC699)



BINARY COUNTER, SYNCHRONOUS CLEAR (HC699)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin (RCO) (QA to QD)	± 25 ± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied

(*) 500 mW. ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage (RCO)	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OH}	High Level Output Voltage (QA - QD)	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage (RCO)	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
V_{OL}	Low Level Output Voltage (QA - QD)	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6$ ns)

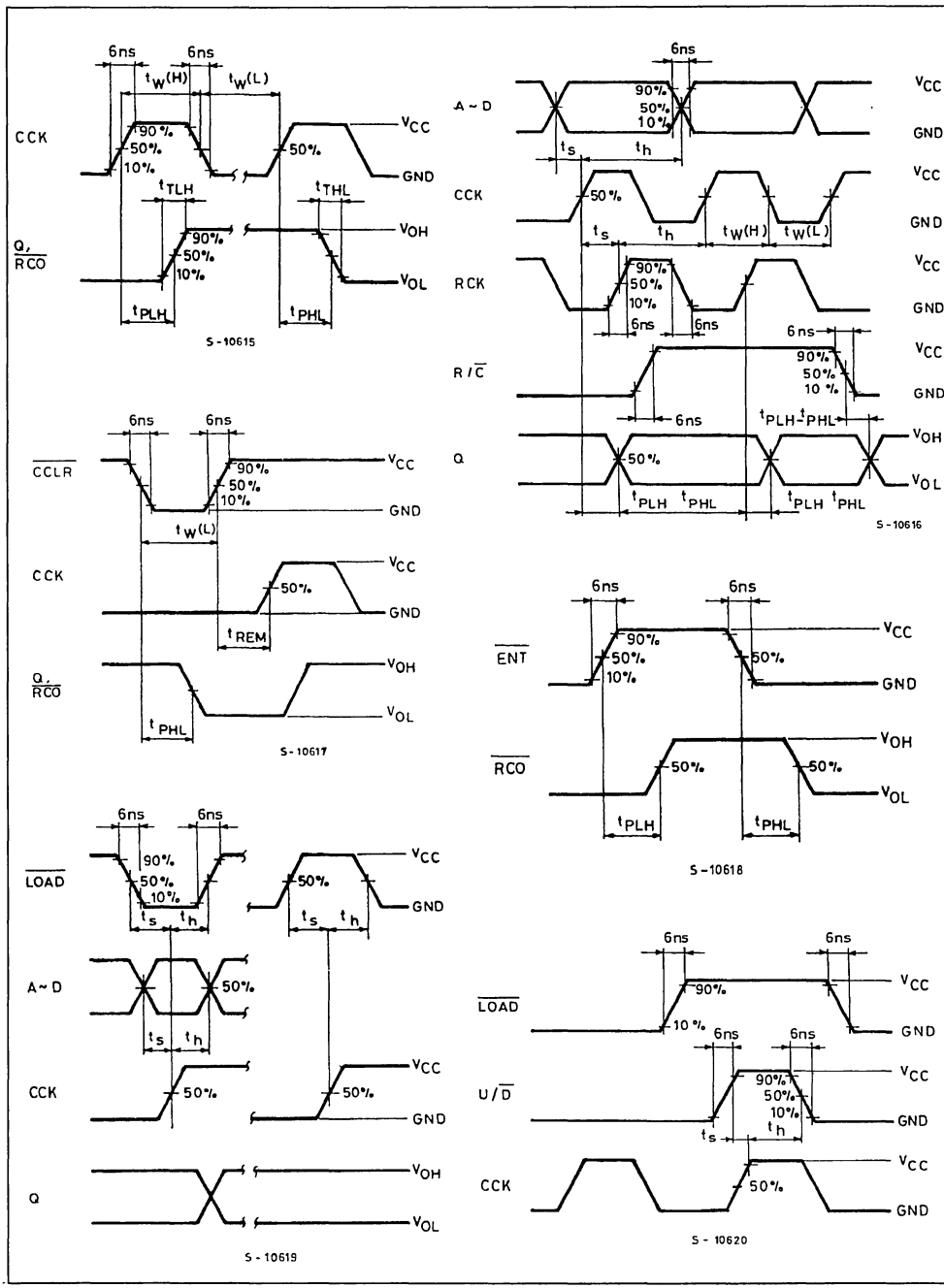
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time (Qn)	2.0	50			25	60		75		90	ns
		4.5				7	12		19		18	
		6.0				6	10		13		15	
t_{TLH} t_{THL}	Output Transition Time ($\overline{RCO}$)	2.0	50			30	75		95		115	ns
		4.5				8	15		19		23	
		6.0				7	13		16		20	
t_{PLH} t_{PHL}	Propagation Delay Time (CCK - Q)	2.0	50			90	215		270		325	ns
		4.5				28	43		54		65	
		6.0				24	37		46		55	
		2.0	150			103	245		305		370	ns
		4.5				32	49		61		74	
		6.0				27	42		52		63	
t_{PLH} t_{PHL}	Propagation Delay Time (RCK - Q)	2.0	50			82	185		230		280	ns
		4.5				24	37		46		56	
		6.0				20	31		39		48	
		2.0	150			95	215		270		325	ns
		4.5				28	43		54		65	
		6.0				24	37		46		55	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CCK}$ - $\overline{RCO}$)	2.0	50			109	245		305		370	ns
		4.5				32	49		61		74	
		6.0				27	42		52		63	
t_{PLH} t_{PHL}	Propagation Delay Time (R/$\overline{C}$ - Q)	2.0	50			61	155		195		235	ns
		4.5				20	31		39		47	
		6.0				17	26		33		40	
		2.0	150			73	185		230		280	ns
		4.5				24	37		46		56	
		6.0				20	31		39		48	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{ENT}$ - $\overline{RCO}$)	2.0	50			63	140		175		210	ns
		4.5				18	28		35		42	
		6.0				15	24		30		36	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CCLR}$ - Q)	2.0	50	for HC696 HC697		78	195		245		295	ns
		4.5				26	39		49		59	
		6.0				22	33		42		50	
		2.0	150			90	235		295		355	ns
		4.5				30	47		59		71	
		6.0				26	40		50		60	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CCLR}$ - $\overline{RCO}$)	2.0	50	for HC696 HC697		98	220		275		330	ns
		4.5				29	44		55		66	
		6.0				25	37		47		56	
f_{MAX}	Maximum Clock Frequency	2.0	50		5	12		4		3.4		MHz
		4.5			25	45		20		17		
		6.0			30	53		24		20		

AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PZL} t_{PZH}	Output Enable Time	2.0	50	R_L = 1KΩ		45	120		150		180	ns
		4.5				15	24		30		36	
		6.0				13	20		26		31	
		2.0	150	R_L = 1KΩ		57	150		190		225	ns
		4.5				19	30		38		45	
		6.0				16	26		32		38	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0	50	R_L = 1KΩ		32	115		145		175	ns
		4.5				17	23		29		35	
		6.0				14	20		25		30	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CCK, RCK)	2.0	50			40	75		95		110	ns
		4.5				8	15		19		22	
		6.0				7	13		16		19	
$t_{W(L)}$	Minimum Pulse Width (CCLR)	2.0	50	for HC696 HC697		40	75		95		110	ns
		4.5				8	15		19		22	
		6.0				7	13		16		19	
t_s	Minimum Set-up Time (CCLR)	2.0	50	for HC698 HC699		16	50		65		75	ns
		4.5				4	10		13		15	
		6.0				3	9		11		13	
t_s	Minimum Set-up Time (LOAD, ENT, ENP)	2.0	50			64	150		190		220	ns
		4.5				16	30		38		44	
		6.0				14	26		32		37	
t_s	Minimum Set-up Time (A, B, C, D)	2.0	50			16	50		65		75	ns
		4.5				4	10		13		15	
		6.0				3	9		11		13	
t_s	Minimum Set-up Time (CCK, RCK)	2.0	50			44	100		125		150	ns
		4.5				11	20		25		30	
		6.0				9	17		21		26	
t_s	Minimum Set-up Time (U/$\overline{D}$)	2.0	50			44	100		125		145	ns
		4.5				11	20		25		29	
		6.0				9	17		21		25	
t_h	Minimum Hold Time	2.0	50				5		5		5	ns
		4.5					5		5		5	
		6.0					5		5		5	
t_{REM}	Minimum Removal Time	2.0	50	for HC696 HC697			5		5		5	ns
		4.5					5		5		5	
		6.0					5		5		5	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance		HC696/697/699 HC698			71 77						pF

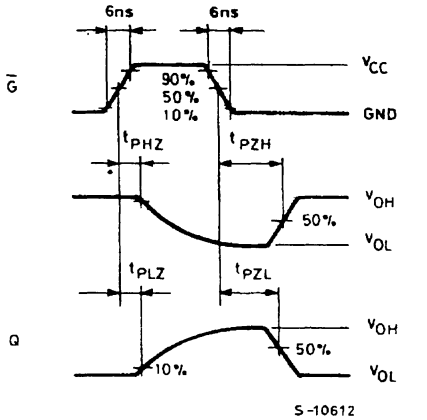
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per circuit)

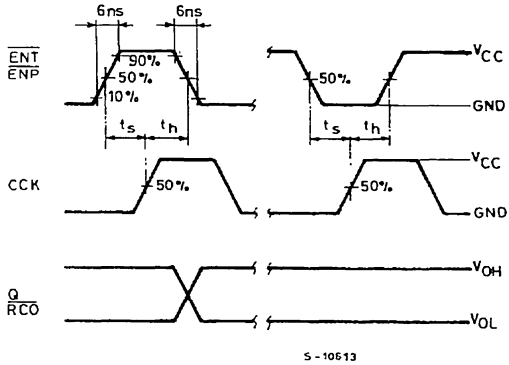
SWITCHING CHARACTERISTICS TEST WAVEFORM (HC696/697)



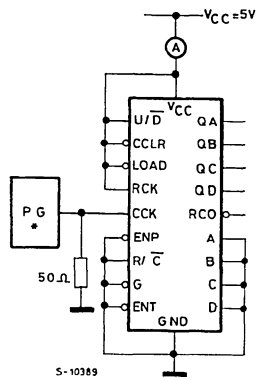
SWITCHING CHARACTERISTICS TEST WAVEFORM (continued)

OUTPUT DISABLE, ENABLE





TEST CIRCUIT I_{CC} (Opr.)

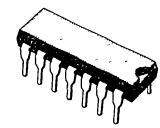


SGS-THOMSON MICROELECTRONICS

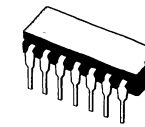
M54HC4002
M74HC4002

DUAL 4 INPUT NOR GATE

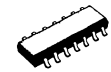
- HIGH SPEED
  t_{PD} = 10 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) AT T_A = 25° C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 4002B



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HC4002F1R M74HC4002M1R
M74HC4002B1R M74HC4002C1R

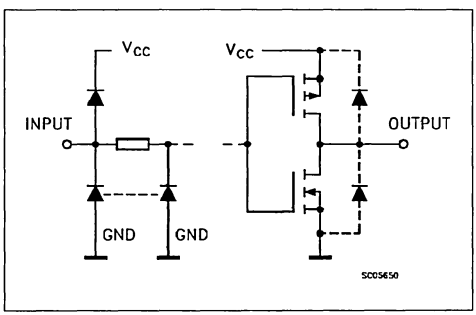
DESCRIPTION

The M54/74HC4002 is a high speed CMOS DUAL 4-INPUT NOR GATE fabricated in silicon gate C^2MOS technology.

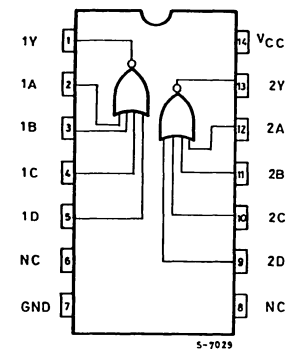
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The internal circuit is composed of 3 stages including buffer output, which ensures high noise immunity and stable output.

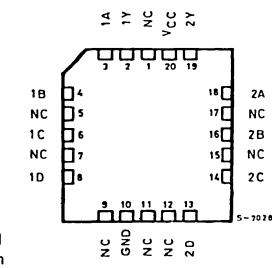
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



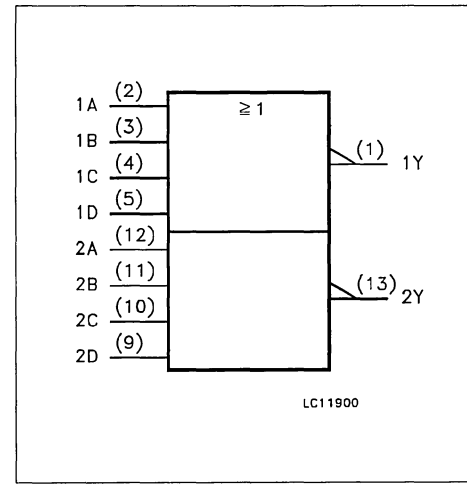


NC =
No Internal
Connection

TRUTH TABLE

nA	nB	nC	nD	nY
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

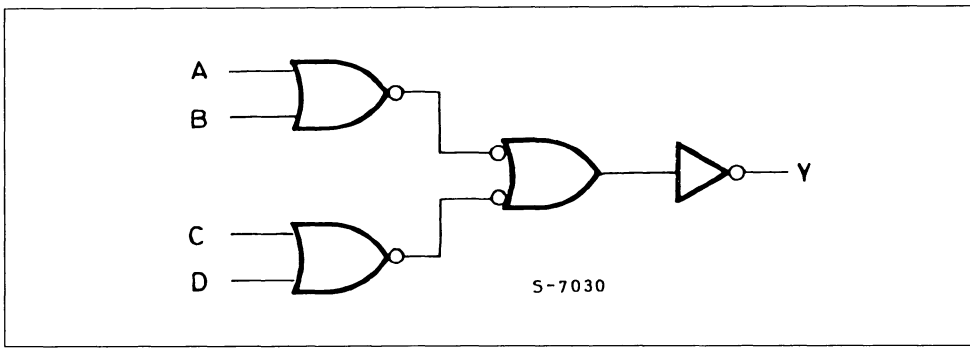
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 13	1Y to 2Y	Data Outputs
2, 9	1A to 2A	Data Inputs
3, 10	1B to 2B	Data Inputs
4, 11	1C to 2C	Data Inputs
5, 12	1D to 4D	Data Inputs
6, 8	NC	Not Connected
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

SCHEMATIC CIRCUIT (Per Gate)



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW. ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

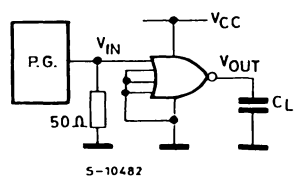
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	µA

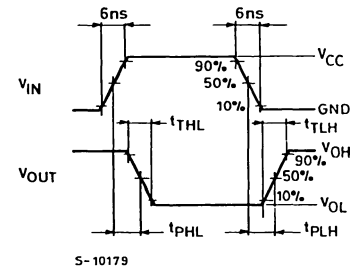
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			48	100		125		150	ns
		4.5			12	20		25		30	
		6.0			10	17		21		26	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				20						pF

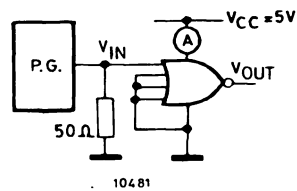
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT





TEST CIRCUIT I_{CC} (Opr.)



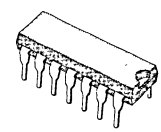
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

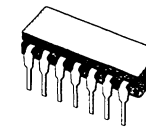
M54HC4016
M74HC4016

QUAD BILATERAL SWITCH

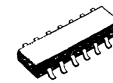
- HIGH SPEED
  t_{PD} = 9 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- LOW "ON" RESISTANCE
  R_{ON} = 60 Ω (TYP.) AT V_{CC} = 9 V, $I_{I/O}$ = 100 µA
- SINE WAVE DISTORSION
  0.042 % (TYP.) AT V_{CC} = 9 V_{PP}, f = 1KHz
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 12 V
- PIN AND FUNCTION COMPATIBLE WITH 4016B



B1R
(Plastic Package)



F1R
(Ceramic Package)



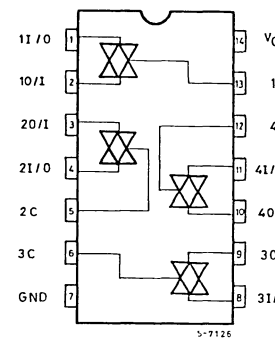
M1R
(Micro Package)

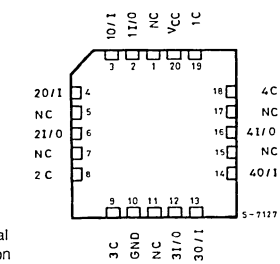
C1R
(Chip Carrier)

ORDER CODES :

M54HC4016F1R M74HC4016M1R
M74HC4016B1R M74HC4016C1R

PIN CONNECTIONS (top view)





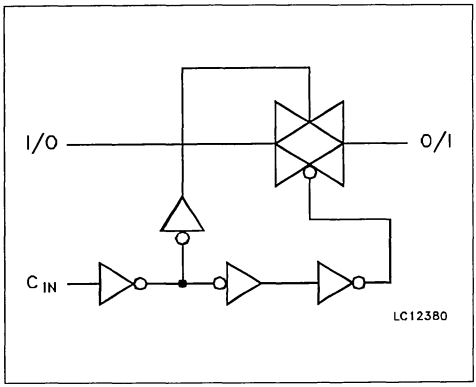
NC =
No Internal
Connection

DESCRIPTION

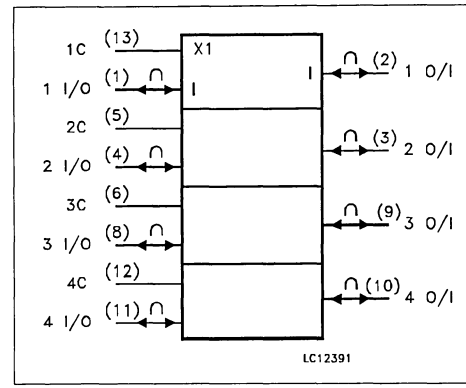
The M54/74HC4016 is a high speed CMOS QUAD BILATERAL SWITCH fabricated in silicon gate C^2MOS technology. It has high speed performance combined with true CMOS low power consumption.

The C input is provided to control the switch ; the switch is ON when the C input is held high and off when C is held low.

LOGIC DIAGRAM



IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 8, 11	1 to 4 I/O	Independent Inputs/Outputs
2, 3, 9, 10	1 to 4 O/I	Independent Outputs/Inputs
13, 5, 6, 12	1C to 4C	Enable Inputs (Active HIGH)
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

TRUTH TABLE

CONTROL	SWITCH FUNCTION
H	ON
L	OFF

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +13	V
V_{IN}	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
$V_{I/O}$	DC Input/Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{OK}	Control Input DC Diode Current	± 20	mA
$I_{I/OK}$	I/O DC Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 12	V
V_I	Input Voltage (Control)		0 to V_{CC}	V
$V_{I/O}$	Input/Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series		-55 to +125	°C
	M74HC Series		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	
		V_{CC} = 10 V	0 to 250	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IHC}	High Level Control Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		9.0		6.3			6.3		6.3		
		12.0		8.4			8.4		8.4		
V_{ILC}	Low Level Control Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		9.0				2.5		2.5		2.5	
		12.0				3.6		3.6		3.6	
R_{ON}	ON Resistance	4.5	V_{IN} = V_{IHC} $V_{I/O}$ = V_{CC} to GND $I_{I/O}$ = 100 µA		160	320		400		450	Ω
		9.0			85	170		213		260	
		12.0			60	120		150		180	
		4.5	V_{IN} = V_{IHC} $V_{I/O}$ = V_{CC} or GND $I_{I/O}$ = 100 µA		80	160		200		250	
		9.0			60	120		150		200	
		12.0			50	100		125		150	
ΔR_{ON}	Difference of ON Resistance Between Switches	4.5	V_{IN} = V_{IHC} $V_{I/O}$ = V_{CC} or GND $I_{I/O} \leq$ 100 µA		16						Ω
		9.0			9						
		12.0			6						
I_{OFF}	Input/Output Leakage Current (SWITCH OFF)	12.0	V_{OS} = V_{CC} or GND V_{IS} = V_{CC} or GND V_{IN} = V_{ILC}			±0.1		±1		±2	µA
I_{IZ}	Switch Input Leakage Current (SWITCH ON, OUTPUT OPEN)	12.0	V_{OS} = V_{CC} or GND V_{IN} = V_{IHC}			±0.1		±1		±2	µA
I_{IN}	Control Input Current	6.0	V_{IN} = V_{CC} or GND			±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_{IN} = V_{CC} or GND			1		10		20	µA
		9.0				4		40		80	
		12.0				8		80		160	

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$ø_{I/O}$	Phase Difference Between Input and Output	2.0			20	50		65		75	ns
		4.5			5	10		13		15	
		9.0			4	8		10		12	
		12.0			3	7		9		11	
t_{PZL} t_{PZH}	Output Enable Time	2.0	R_L = 1KΩ		40	100		125		150	ns
		4.5			10	20		25		30	
		9.0			8	15		20		24	
		12.0			7	14		18		21	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0	R_L = 1KΩ		60	150		190		225	ns
		4.5			15	30		38		45	
		9.0			10	26		33		36	
		12.0			8	24		30		32	
C_{IN}	Input Capacitance				5	10		10		10	pF
$C_{I/O}$	Switch Terminal Capacitance	9.0			5						pF
C_{IOS}	Feed Through Capacitance	9.0			1						pF
C_{PD} (*)	Power Dissipation Capacitance	5.0			15						pF

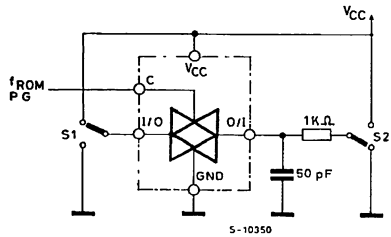
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

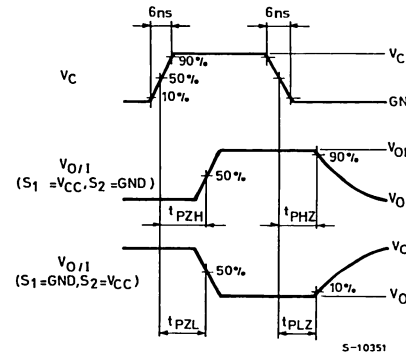
ANALOG SWITCH CHARACTERISTICS (GND = 0 V T_A = 25 °C)

Symbol	Parameter	Test Conditions			Value	Unit
		V_{CC} (V)	VIN (Vp-p)		Typ.	
	Sine Wave Distortion (THD)	4.5	4.5	f_{IN} = 1 KHz R_L = 10 KΩ C_L = 50 pF	0.118	%
		9.0	9.0		0.042	
		12.0	12.0		0.032	
f_{MAX}	Frequency Response (Switch ON)	4.5	Adjust f_{IN} voltage to Obtain 0 dBm at V_{OS}. Increase f_{IN} Frequency until dB Meter reads -3dB R_L = 50 Ω C_L = 50 pF		23	MHz
		9.0			38	
		12.0			42	
	Feedthrough Attenuation (Switch OFF)	4.5	V_{IN} is centered at VCC/2. Adjust input for 0 dBm R_L = 600 Ω C_L = 50 pF f_{IN} = 1 MHz sine wave		-50	dB
		9.0			-50	
		12.0			-50	
	Crosstalk (Control Input to Signal Output)	4.5	R_L = 600 Ω C_L = 50 pF f_{IN} = 1 MHz square wave ($t_r = t_f$ = 6ns)		8	mV
		9.0			23	
		12.0			40	
	Crosstalk (Between Any Switches)	4.5	Adjust V_{IN} to Obtain 0 dBm at input R_L = 600 Ω C_L = 50 pF f_{IN} = 1 MHz sine wave		-50	dB
		9.0			-50	
		12.0			-50	

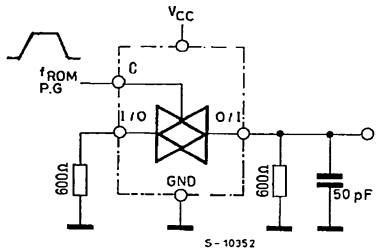
SWITCHING CHARACTERISTICS TEST CIRCUIT

t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}.

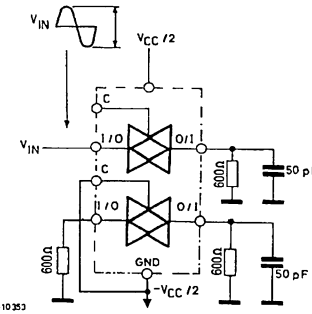




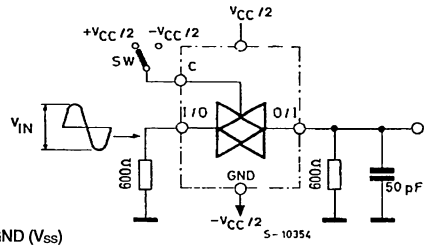
CROSSTALK (control to output)



CROSSTALK BETWEEN ANY TWO SWITCHES

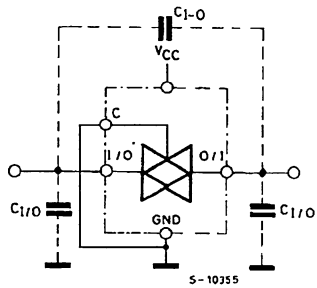


BANDWIDTH AND FEEDTHROUGH ATTENUATION



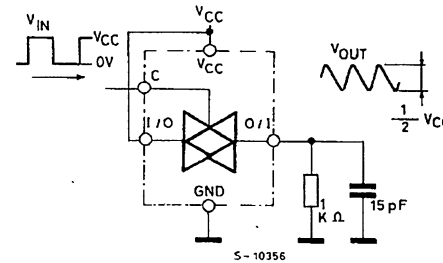
GND (V_{SS})

C_{I-O} $C_{I/O}$

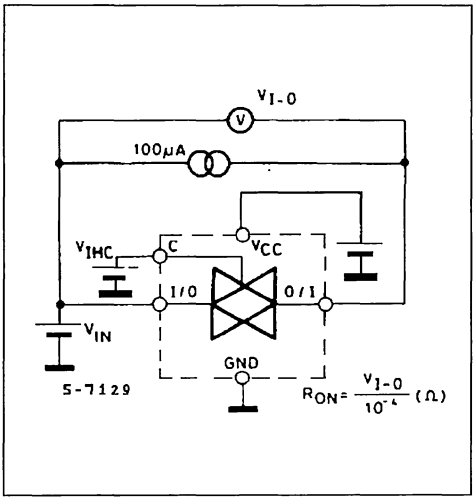


GND (V_{SS})

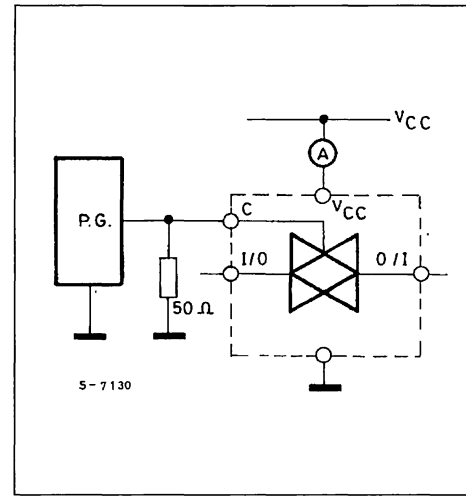
MAXIMUM CONTROL FREQUENCY



CHANNEL RESISTANCE (R_{ON})

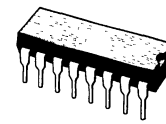


I_{CC} (Opr.)

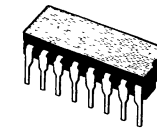


DECADE COUNTER/DIVIDER

- HIGH SPEED
  t_{PD} = 21 ns (typ.) AT V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLEWITH 4017B



B1R
(Plastic Package)



F1R
(Ceramic Package)

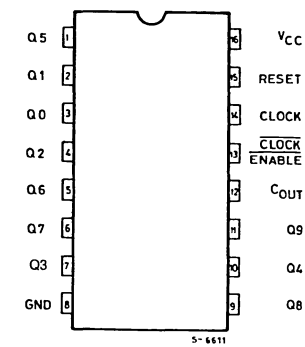
M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HC4017F1R M74HC4017M1R
M74HC4017B1R M74HC4017C1R

PIN CONNECTIONS (top view)



NC =
No Internal
Connection

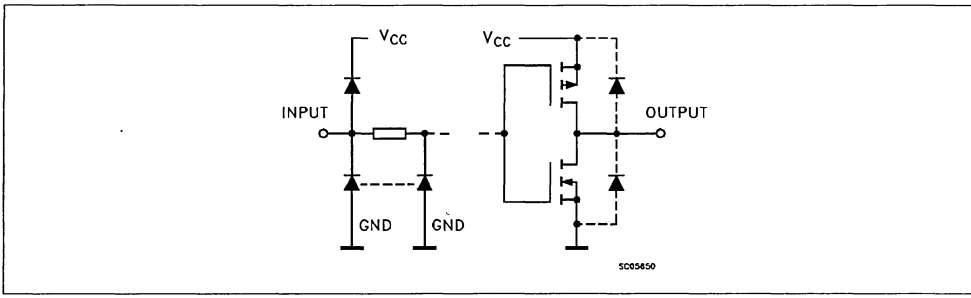
DESCRIPTION

The M54/74HC4017 is a high speed CMOS DECADE COUNTER/DIVIDER fabricated in silicon gate C2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

The M54/74HC4017 is a 5-stage Johnson counter with 10 decoded outputs. Each of the decoded outputs is normally low and sequentially goes high on the low to high transition of the clock input. Each output stays high for one clock period of the 10 clock period cycle. The CARRY output goes low to high after OUTPUT 10 goes low, and can be used in conjunction with the CLOCK ENABLE to cascade several stages.

The CLOCK ENABLE input disables counting when in the high state. A RESET input is also provided which when taken high sets all the decoded outputs low.

INPUT AND OUTPUT EQUIVALENT CIRCUIT

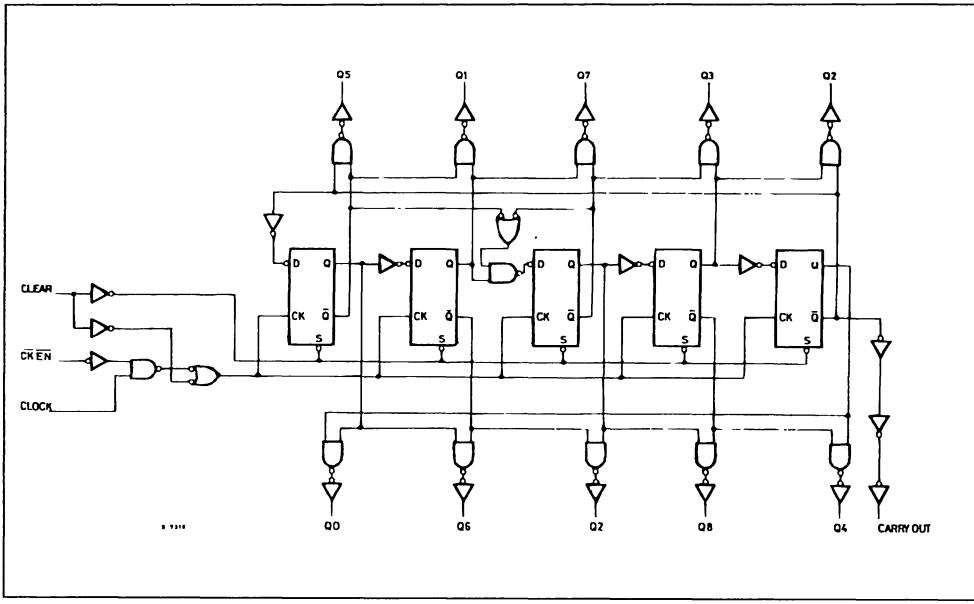


TRUTH TABLE

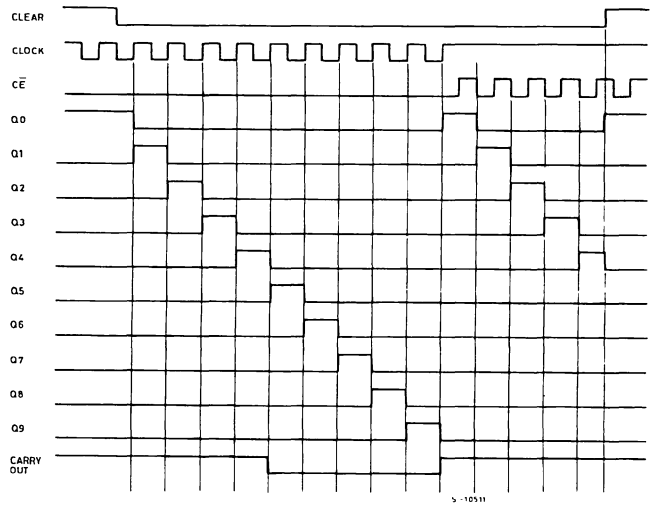
CLOCK	CLOCK ENABLE	CLEAR	DECODE OUTPUT (H)
X	X	H	QO
L	X	L	Qn
X	H	L	Qn
⌐¯	L	L	Qn + 1
¯⌐	L	L	Qn
H	⌐¯	L	Qn
H	¯⌐	L	Qn + 1

X: DON'T CARE
Qn : NO CHANGE

LOGIC DIAGRAM



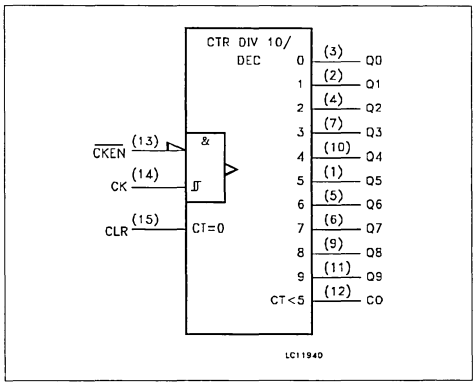
TIMING DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
3, 2, 4, 7, 10, 1, 5, 6, 9, 11	Q0 to Q9	Decoded Outputs
12	C_{OUT}	Carry Output (Active LOW)
13	$\overline{CKEN}$	Clock Enable Input (Active LOW)
14	CLOCK	Clock Input (LOW to HIGH, Edge-triggered)
15	RESET	Master Reset Input (Active HIGH)
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

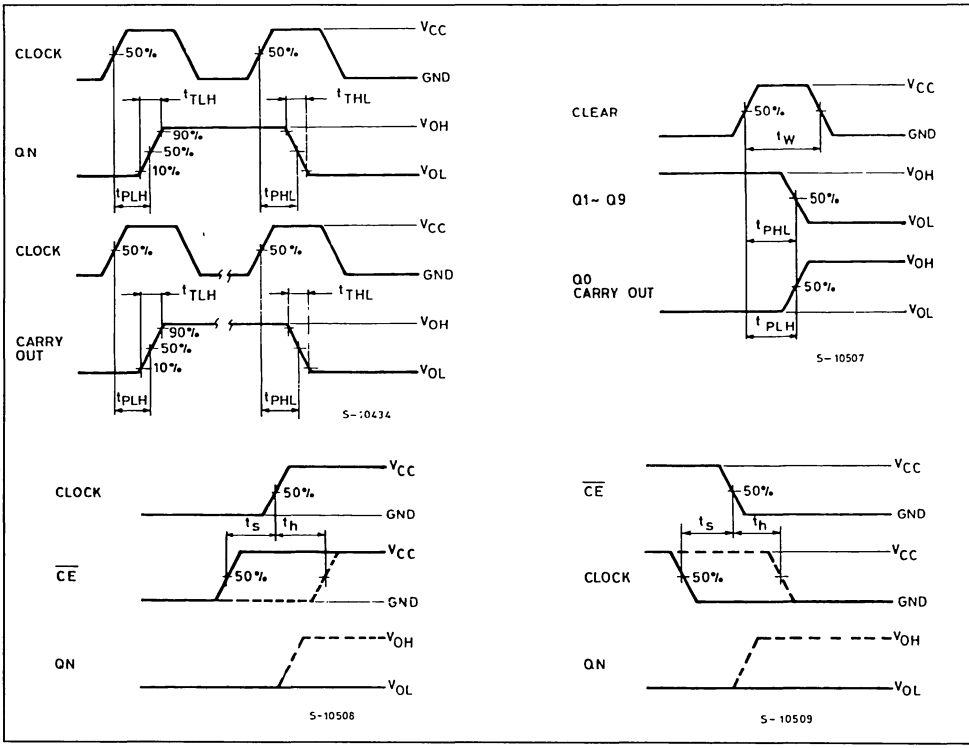
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

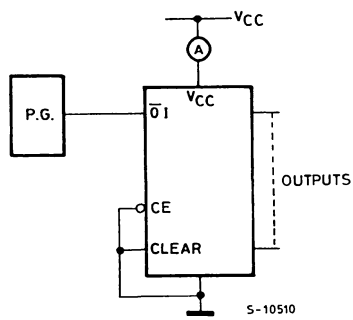
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CK, CE - Q, C_{OUT})	2.0			100	195		245		295	ns
		4.5			25	39		49		59	
		6.0			21	33		42		50	
t_{PLH} t_{PHL}	Propagation Delay Time (CLEAR- Q, C_{OUT})	2.0			100	195		245		295	ns
		4.5			25	39		49		59	
		6.0			21	33		42		50	
f_{MAX}	Maximum Clock Frequency	2.0		5	10		4		3.4		ns
		4.5		25	41		20		17		
		6.0		29	48		24		20		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0			35	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	2.0			35	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
t_s	Minimum Set-up Time	2.0			12	50		65		75	ns
		4.5			3	10		13		15	
		6.0			3	9		11		13	
t_h	Minimum Hold Time	2.0			32	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{REM}	Minimum Removal Time	2.0			28	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				41						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



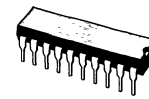
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

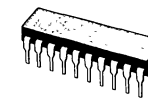
M54/74HC4020
M54/74HC4040

HC4020 14 STAGE BINARY COUNTER
HC4040 12 STAGE BINARY COUNTER

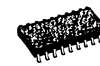
- HIGH SPEED
  f_{MAX} = 73 MHz (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V to 6 V
- PIN AND FUNCTION COMPATIBLE WITH 4020B/4040B



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HCXXXF1R M74HCXXXM1R
M74HCXXXB1R M74HCXXXC1R

DESCRIPTION

The M54/74HC4020/HC4040 are high speed CMOS 14/12-STAGE BINARY COUNTER fabricated in silicon gate C^2MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low consumption.

A clear input is used to reset the counter to the all low level state. A high level on CLEAR accomplishes the reset function. A negative transition on the CLOCK input increments the counter by one.

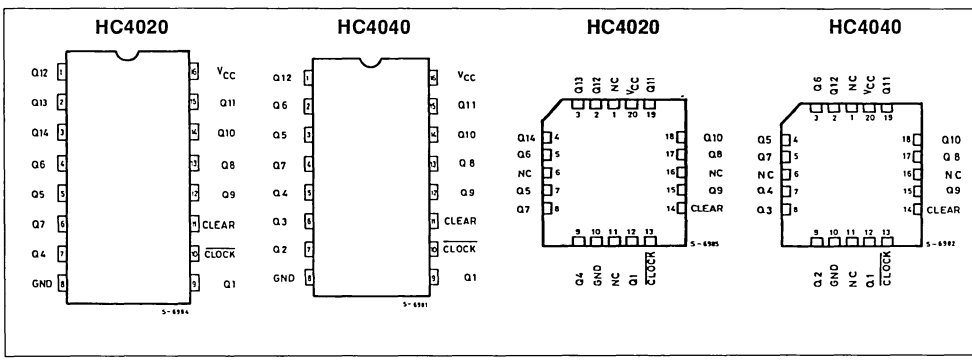
For HC4020 twelve kind od divided output are provided; 1st and 4th stage to 14th stage.

The maximum division available at last stage is 1/16384 x f_{IN} at clock.

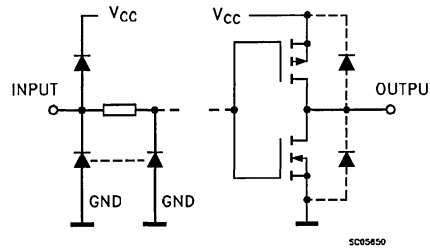
For HC4040 each division stage has an output; the final frequency is 1/4096 x f_{IN}.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION (top view)



INPUT AND OUTPUT EQUIVALENT CIRCUIT



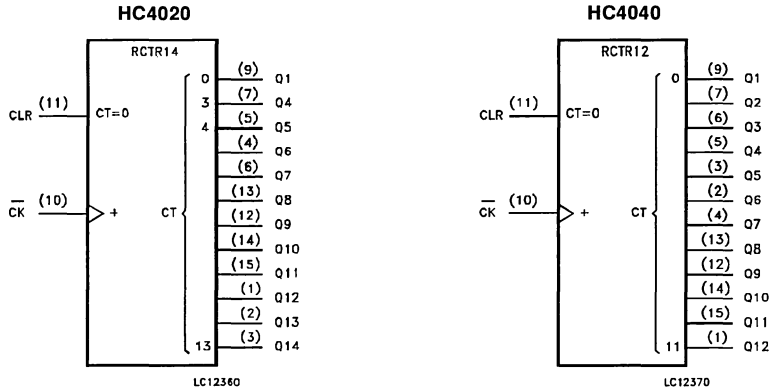
PIN DESCRIPTION (HC4020)

PIN No	SYMBOL	NAME AND FUNCTION
9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1	Q1, Q4 to Q14	Parallel Outputs
10	$\overline{CLOCK}$	Clock Input (LOW to HIGH, edge triggered)
11	CLEAR	Reset Inputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

PIN DESCRIPTION (HC4040)

PIN No	SYMBOL	NAME AND FUNCTION
9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1	Q1 to Q12	Parallel Outputs
10	$\overline{CLOCK}$	Clock Input (LOW to HIGH, edge triggered)
11	CLEAR	Reset Inputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

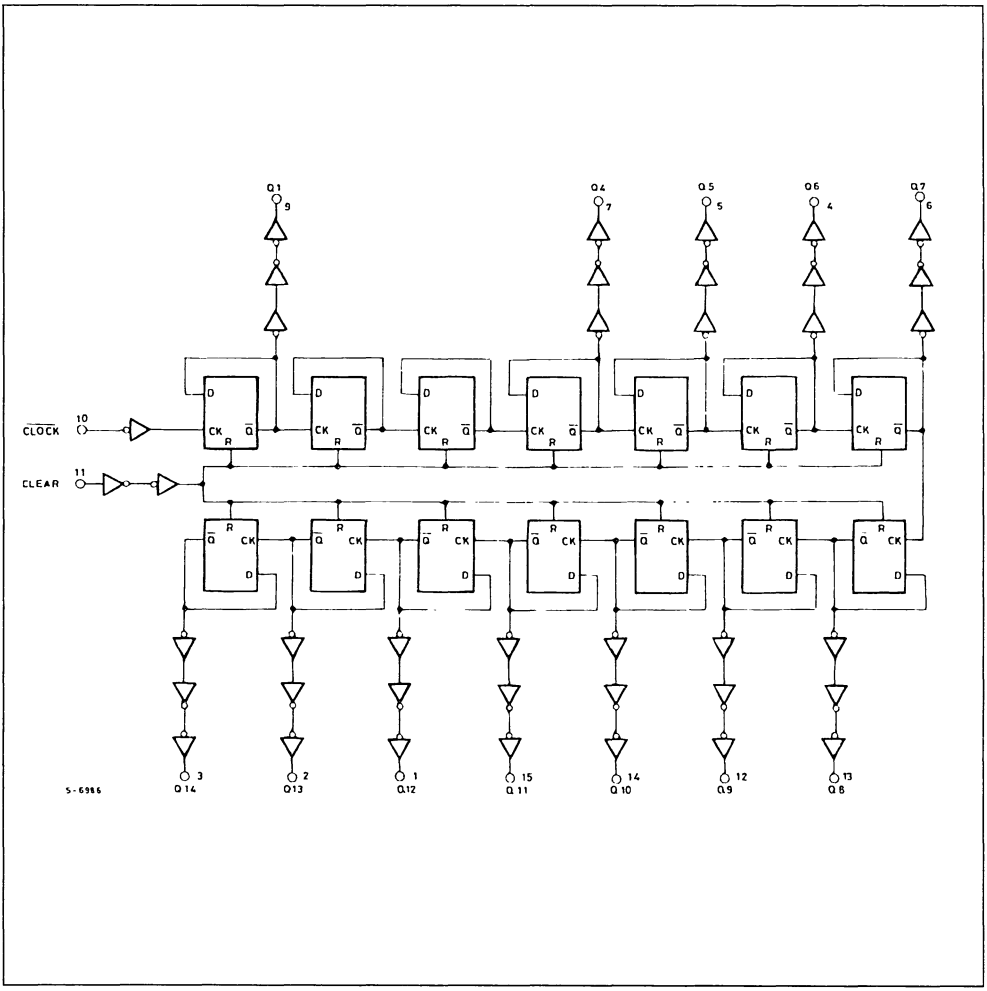
IEC LOGIC SYMBOLS



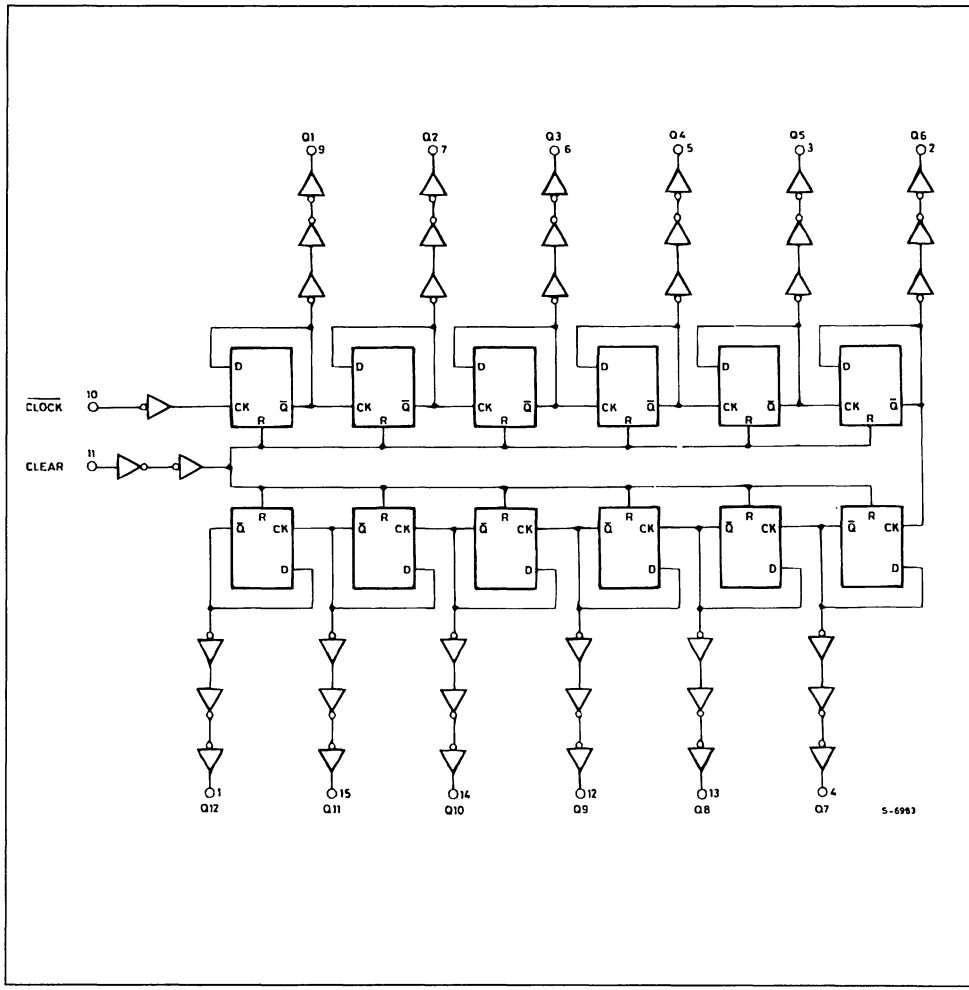
TRUTH TABLE

$\overline{CLOCK}$	CLEAR	OUTPUT STATE
X	H	ALL OUTPUTS = "L"
⌐	L	NO CHANGE
¬	L	ADVANCE TO NEXT STATE

LOGIC DIAGRAM (HC4020)



LOGIC DIAGRAM (HC4040)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series		-55 to +125	°C
	M74HC Series		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

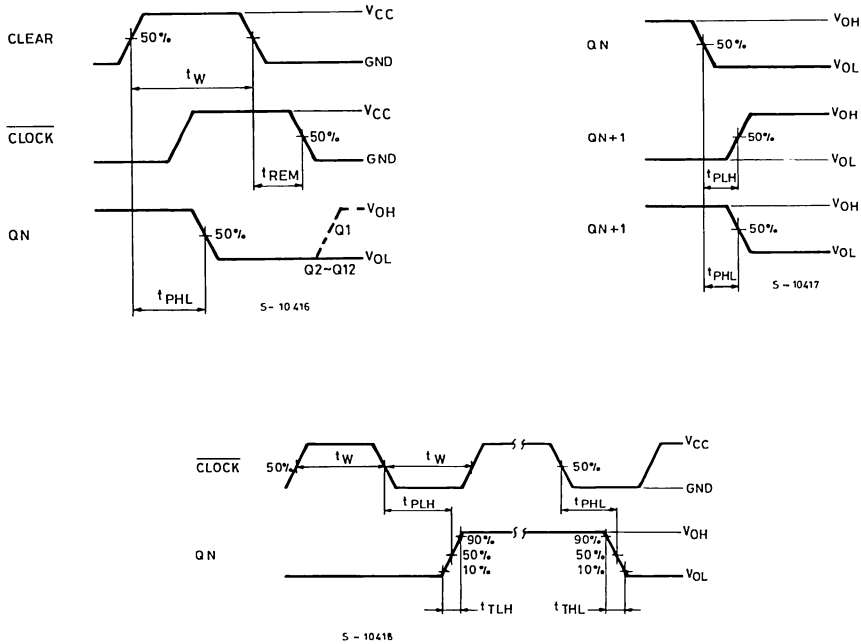
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

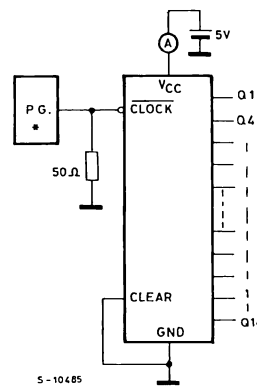
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (Qn - Qn+1)	2.0			20	50		65		75	ns
		4.5			5	10		13		15	
		6.0			4	9		11		13	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK Q1)	2.0	for HC4020		76	145		180		220	ns
		4.5			21	29		36		44	
		6.0			18	25		31		38	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK Q1)	2.0	for HC4040		48	145		180		220	ns
		4.5			17	29		36		44	
		6.0			13	25		31		38	
t_{PHL}	Propagation Delay Time (CLEAR - Qn)	2.0	for HC4020		60	140		175		210	ns
		4.5			18	28		35		42	
		6.0			15	24		30		36	
t_{PHL}	Propagation Delay Time (CLEAR - Qn)	2.0	for HC4040		56	140		175		210	ns
		4.5			18	28		35		42	
		6.0			15	24		30		36	
f_{MAX}	Maximum Clock Frequency	2.0		6.0	15		4.8		4		MHz
		4.5		30	65		24		20		
		6.0		35	70		28		24		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0			40	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	2.0	for HC4020		32	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	2.0	for HC4040		70	175		220		265	ns
		4.5			19	35		44		53	
		6.0			16	30		37		45	
t_{REM}	Minimum Removal Time	2.0	for HC4020			0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Minimum Removal Time	2.0	for HC4040			25		30		40	ns
		4.5				5		6		8	
		6.0				5		5		7	
C_{IN}	Input Capacitance				5	10		10			pF
C_{PD} (*)	Power Dissipation Capacitance				34						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per FLIP/FLOP)

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



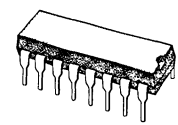
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

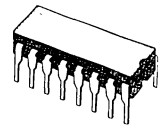
M54HC4022
M74HC4022

OCTAL COUNTER/DIVIDER

- HIGH SPEED
  f_{MAX} = 57 MHz (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} 4 µA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V to 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 4022B



B1R
(Plastic Package)



F1R
(Ceramic Package)

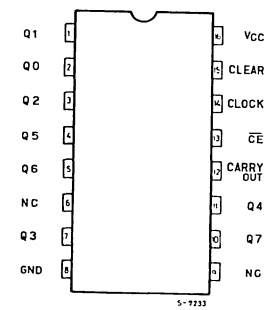
M1R
(Micro Package)

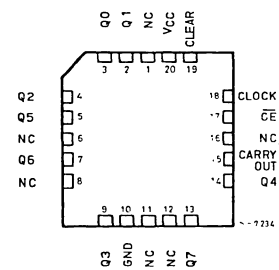
C1R
(Chip Carrier)

ORDER CODES :

M54HC4022F1R M74HC4022M1R
M74HC4022B1R M74HC4022C1R

PIN CONNECTIONS (top view)





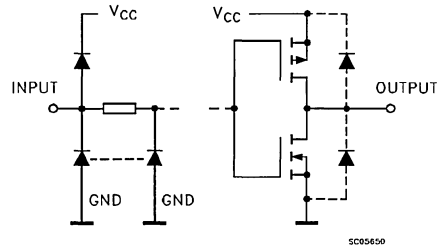
NC =
No Internal
Connection

DESCRIPTION

The M54/74HC4022 is a high speed CMOS OCTAL COUNTER/DIVIDER fabricated in silicon gate C^2MOS technology.

It has the same high speed performance of LSTTL combined with true CMOS low power consumption. It contains a 4-stage divide-by-8 Johnson counter with 8 decoded outputs (Q0-Q7) and a Carry-out bit. This counter is advanced on the positive edge of the clock signal when CLOCK ENABLE input is held low, or is advanced on the negative edge of clock enable signal when CLOCK input is held high, and the selected one of eight outputs goes high. Holding the CLEAR input high clears the counter to zero regardless of the other input conditions. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT

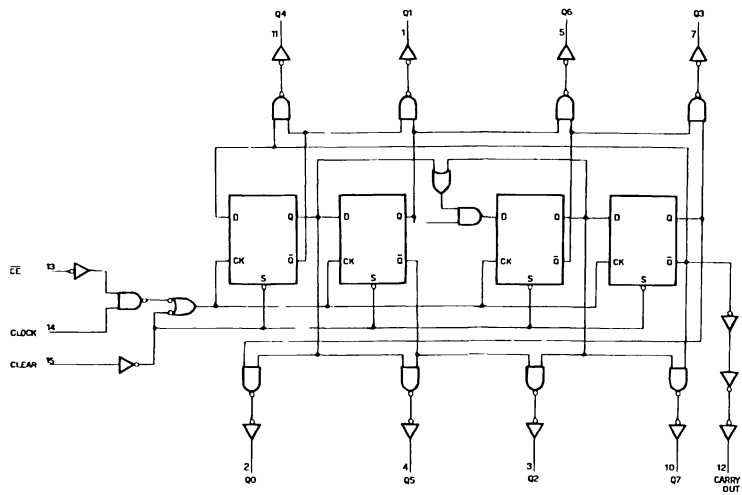


TRUTH TABLE

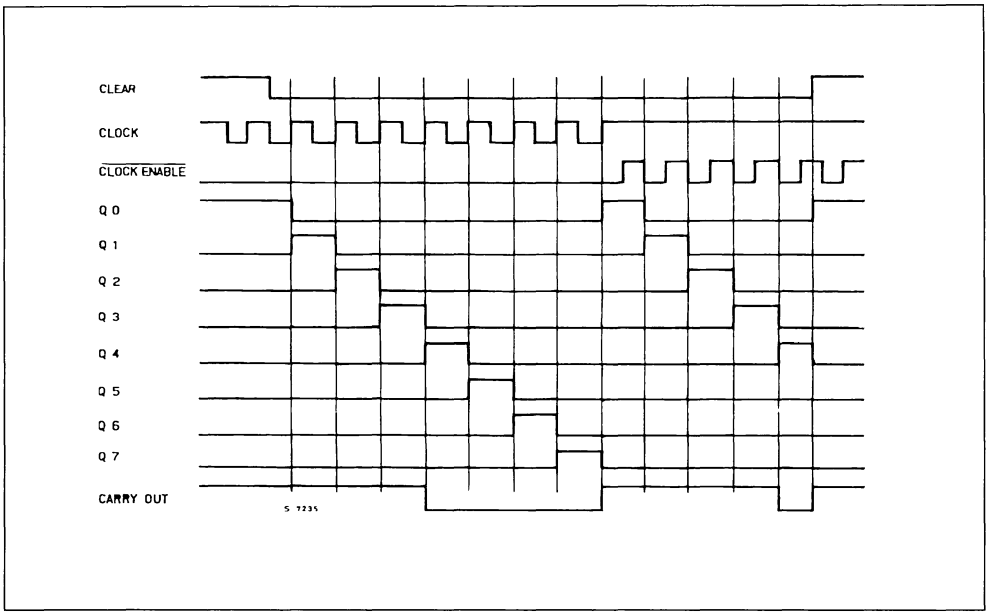
CLOCK	$\overline{CE}$	CLEAR	DECODER OUTPUT (H)
X	X	H	Q0
L	X	L	NO CHANGE
X	H	L	NO CHANGE
⌐	L	L	NO CHANGE + 1
¬	L	L	NO CHANGE
H	⌐	L	NO CHANGE
H	¬	L	NO CHANGE + 1

X: DON'T CARE

LOGIC DIAGRAM



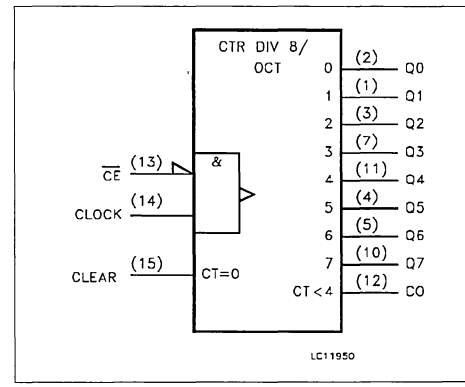
TIMING CHART



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
3, 2, 4, 7, 10, 1, 5, 11	Q0 to Q7	Decoded Outputs
6, 9	NC	Not Connected
12	CARRY OUT	Carry Output (Active LOW)
13	$\overline{CE}$	Clock Input (HIGH to LOW, Edge-triggered)
14	CLOCK	Clock Input (LOW to HIGH, Edge-triggered)
15	CLEAR	Master reset Input (Active HIGH)
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

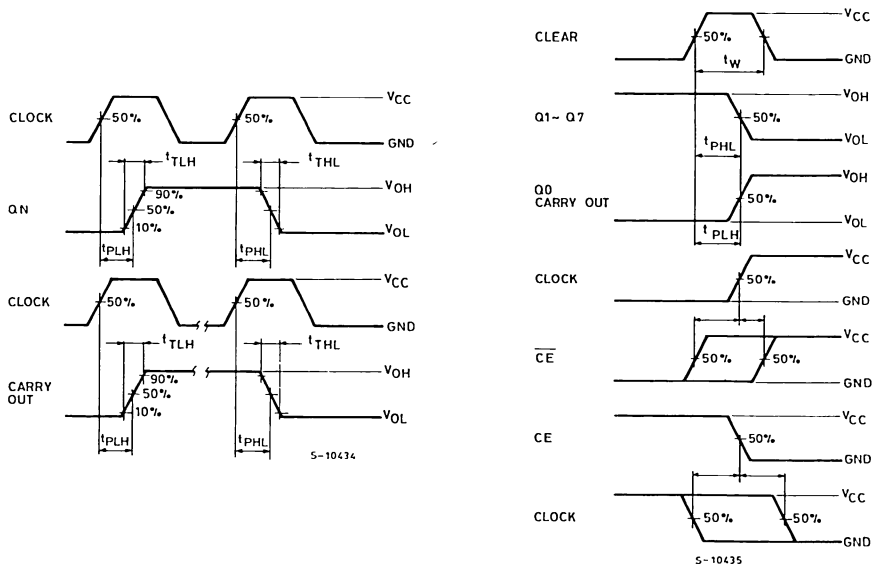
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

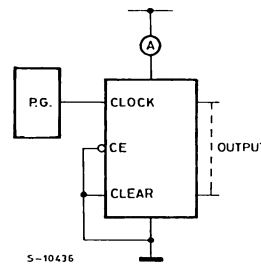
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Qn, CARRY)	2.0			71	160		200		240	ns
		4.5			21	32		40		48	
		6.0			16	27		34		41	
t_{PLH} t_{PHL}	Propagation Delay Time (CLEAR - Qn, CARRY)	2.0			69	145		180		220	ns
		4.5			19	29		36		44	
		6.0			15	25		31		38	
f_{MAX}	Maximum Clock Frequency	2.0		6	11		5		4.2		ns
		4.5		31	51		25		21		
		6.0		36	63		29		25		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0			20	75		95		110	ns
		4.5			7	15		19		22	
		6.0			4	13		16		19	
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	2.0			19	75		95		110	ns
		4.5			7	15		19		22	
		6.0			3	13		16		198	
t_s	Minimum Set-Up Time	2.0			9	0		0		0	ns
		4.5			3	0		0		0	
		6.0			2.5	0		0		0	
t_h	Minimum Hold Time	2.0			13	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	
t_{REM}	Minimum Removal Time	2.0			13	50		65		75	ns
		4.5			3	10		13		15	
		6.0			2	9		11		13	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				53						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



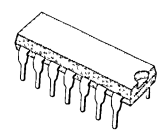
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

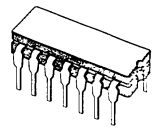
M54HC4024
M74HC4024

7 STAGE BINARY COUNTER

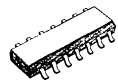
- HIGH SPEED
  t_{PD} = 13 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25° C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 4024B



B1R
(Plastic Package)



F1R
(Ceramic Package)



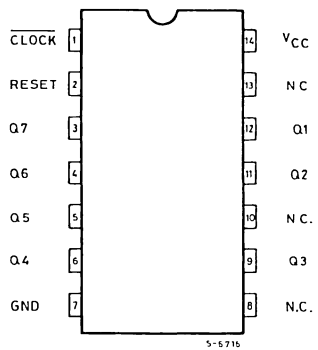
M1R
(Micro Package)

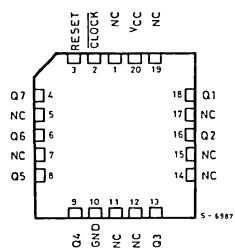
C1R
(Chip Carrier)

ORDER CODES :

M54HC4024F1R M74HC4024M1R
M74HC4024B1R M74HC4024C1R

PIN CONNECTIONS (top view)



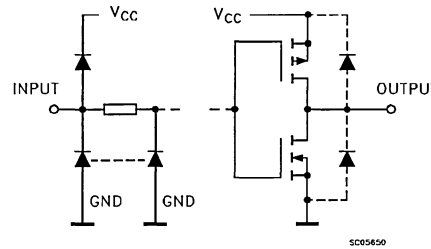


NC =
No Internal
Connection

DESCRIPTION

The M54/74HC4024 is a high speed CMOS 7-STAGE BINARY COUNTER fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The HC4024 is a 7 stage Counter. This devices is incremented on the falling edge (negative transition) of the input clock, and all its outputs are reset to a low level by applying a logical high on their reset input. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT

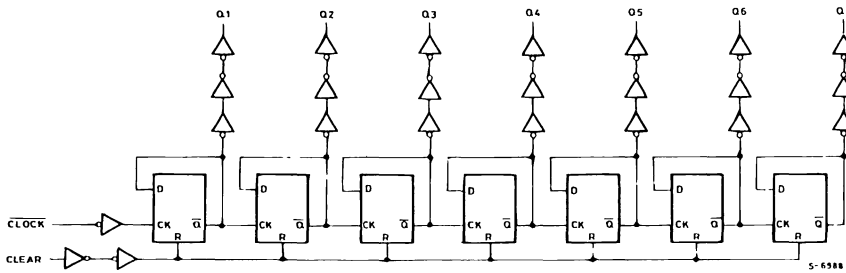


TRUTH TABLE

CLOCK	CLEAR	OUTPUT STATE
X	H	ALL OUTPUTS = "L"
⎍	L	NO CHANGE
⎎	L	ADVANCE TO NEXT STATE

X: DON'T CARE

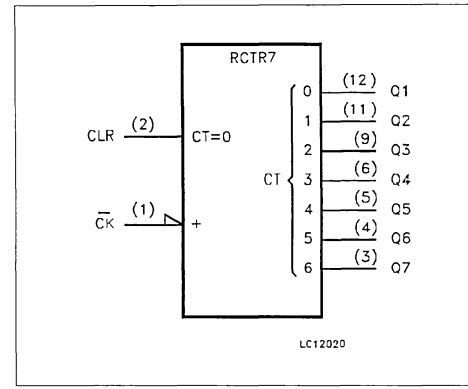
LOGIC DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{CLOCK}$	Clock Input (HIGH to LOW, Edge-triggered)
2	RESET	Reset Input (Active HIGH)
12, 11, 9, 6, 5, 4, 3	Q1 to Q7	Parallel Outputs
8, 10, 13	NC	Not Connected
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied
(*) 500 mW. ≅ 65 °C derate to 300 mW by 10mW/°C. 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

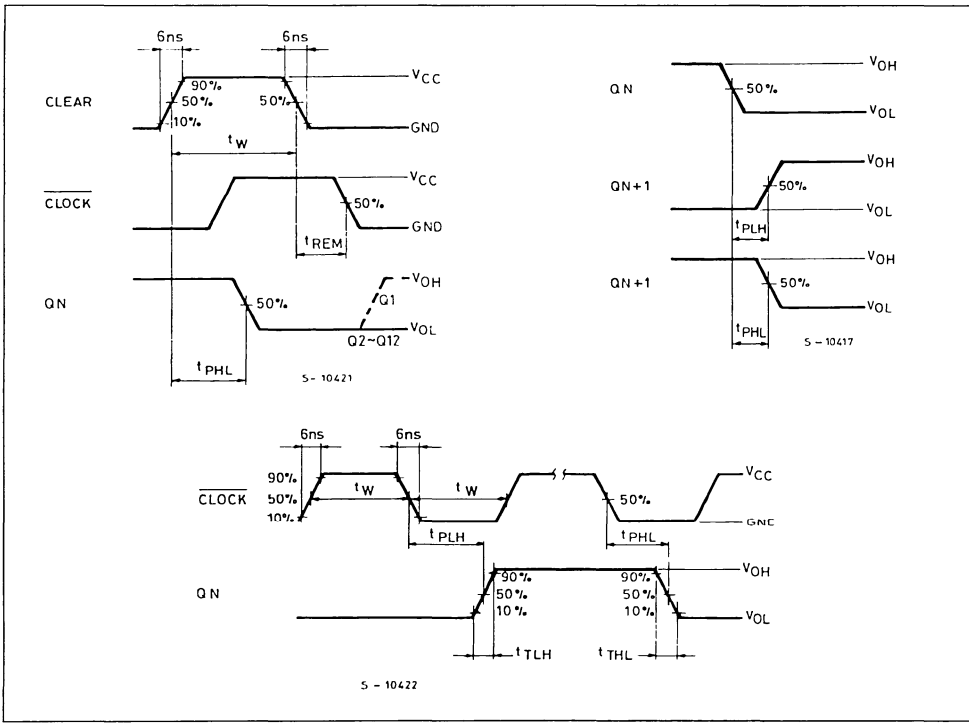
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

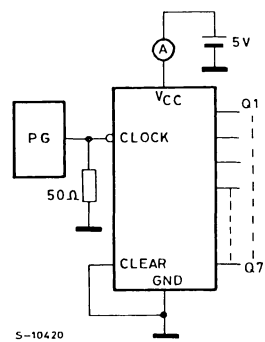
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (Qn - Qn + 1)	2.0			24	60		75		90	ns
		4.5			6	12		15		18	
		6.0			5	10		13		15	
t_{PLH} t_{PHL}	Propagation Delay Time Clock - Q1	2.0			60	120		150		180	ns
		4.5			15	24		30		36	
		6.0			13	20		26		31	
t_{PHL}	Propagation Delay Time (CLEAR - Qn)	2.0			60	120		150		180	ns
		4.5			15	24		30		36	
		6.0			13	20		26		31	
f_{MAX}	Maximum Clock Frequency	2.0		8	17		7		5.6		ns
		4.5		42	67		34		28		
		6.0		49	79		40		34		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0			24	75		95		110	ns
		4.5			6	15		19		22	
		6.0			5	13		16		19	
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	2.0			32	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{REM}	Minimum Removal Time	2.0				25		30		40	ns
		4.5				5		6		8	
		6.0				5		5		7	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				34						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



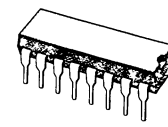
TEST CIRCUIT Icc (Opr.)



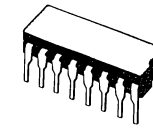
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

BCD TO DECIMAL DECODER

- HIGH SPEED
  t_{PD} = 18 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 4028B



B1R
(Plastic Package)



F1R
(Ceramic Package)

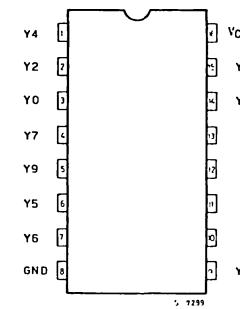
M1R
(Micro Package)

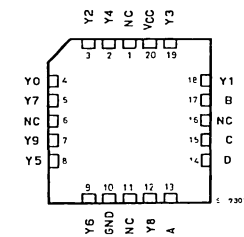
C1R
(Chip Carrier)

ORDER CODES :

M54HC4028F1R M74HC4028M1R
M74HC4028B1R M74HC4028C1R

PIN CONNECTIONS (top view)





NC =
No Internal
Connection

DESCRIPTION

The M54/74HC4028 is a high speed CMOS BCD-TO-DECIMAL DECODER fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. A BCD code applied to the four inputs (A to D) provides a high level at the selected one of the decimal decoded outputs. An illegal BCD code such as eleven to fifteen gives a low level at all outputs. The device also can be used as 3-TO-8-LINE DECODER, when D input is assigned as a disable input. The device is useful for code conversion, address decoding, memory selection, demultiplexing, or read out decoding.

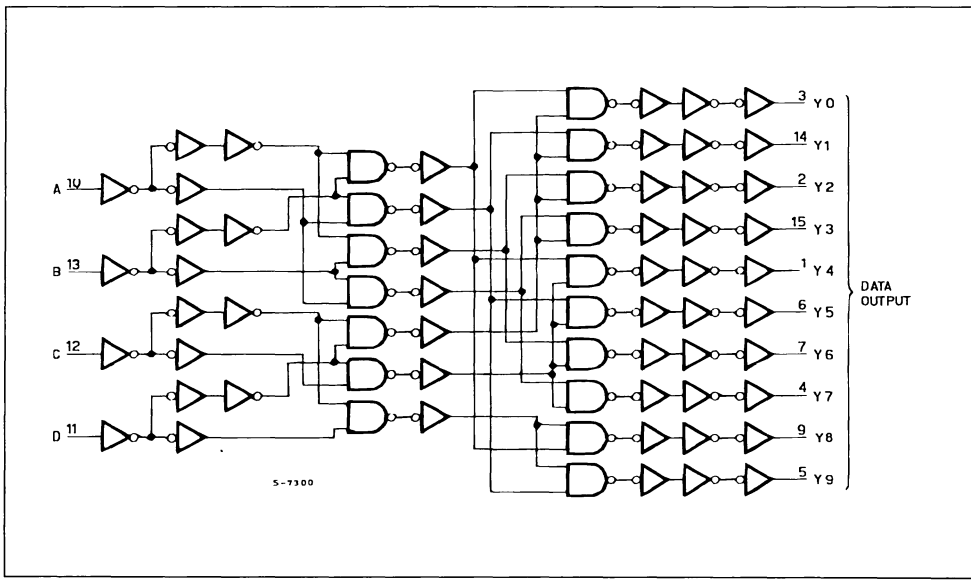
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

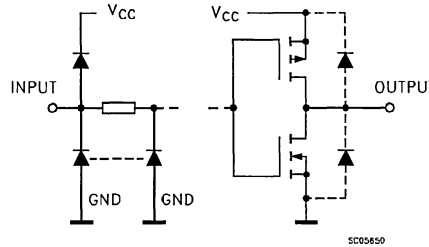
INPUTS				OUTPUTS										SELECTED OUTPUTT
D	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	
L	L	L	L	H	L	L	L	L	L	L	L	L	L	Y0
L	L	L	H	L	H	L	L	L	L	L	L	L	L	Y1
L	L	H	L	L	L	H	L	L	L	L	L	L	L	Y2
L	L	H	H	L	L	L	H	L	L	L	L	L	L	Y3
L	H	L	L	L	L	L	L	H	L	L	L	L	L	Y4
L	H	L	H	L	L	L	L	L	H	L	L	L	L	Y5
L	H	H	L	L	L	L	L	L	L	H	L	L	L	Y6
L	H	H	H	L	L	L	L	L	L	L	H	L	L	Y7
H	L	L	L	L	L	L	L	L	L	L	L	H	L	Y8
H	L	L	H	L	L	L	L	L	L	L	L	L	H	Y9
H	X	H	X	L	L	L	L	L	L	L	L	L	L	NOTE
H	H	X	X	L	L	L	L	L	L	L	L	L	L	NOTE

X DON'T CARE

LOGIC DIAGRAM



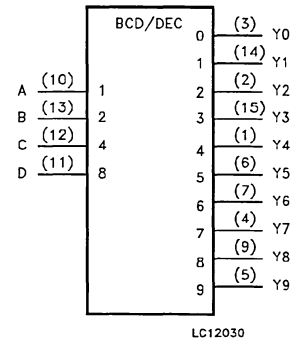
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 9, 14, 15	Y0 to Y9	Decoder Outputs
10, 11, 13, 12	A to D	Data Inputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied

(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series		-55 to +125	°C
	M74HC Series		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

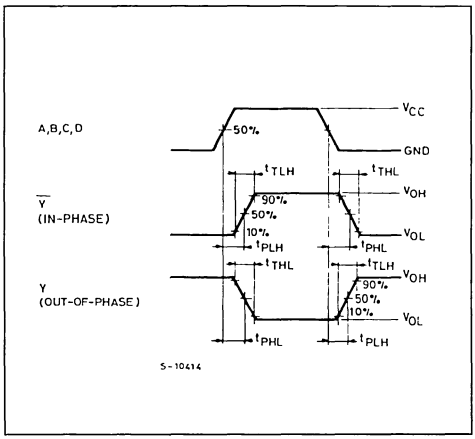
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

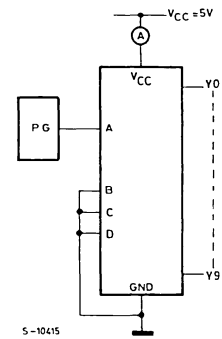
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			96	185		230		280	ns
		4.5			24	37		46		56	
		6.0			20	31		39		48	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				39						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)

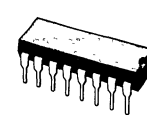


INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

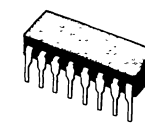
M54/74HC4049
M54/74HC4050

HC4049 HEX BUFFER/CONVERTER (INVERTER)
HC4050 HEX BUFFER/CONVERTER

- HIGH SPEED
  t_{PD} = 9 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 4049B/4050B



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

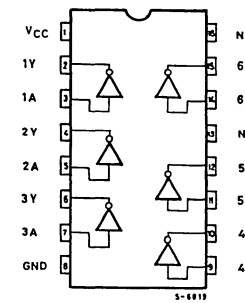
C1R
(Chip Carrier)

ORDER CODES :

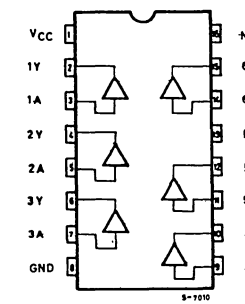
M54HCXXXXF1R M74HCXXXXM1R
M74HCXXXXB1R M74HCXXXXC1R

PIN CONNECTIONS (top view)

HC4049



HC4050



NC =
No Internal
Connection

DESCRIPTION

The M54/74HC4049 and the M54/74HC4050 are high speed CMOS HEX BUFFER fabricated in silicon gate C^2MOS technology.

They have the same high speed performance of LSTTL combined with true CMOS low power consumption.

The M54/75HC4049 is an inverting buffer, while the M54/74HC4050 is a non-inverting buffer.

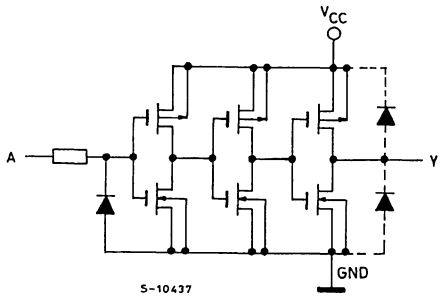
The internal circuit is composed of 3 stage or 2-stage inverters, which provides high noise immunity and a stable output.

Input protection circuits are different from those of the high speed CMOS IC's.

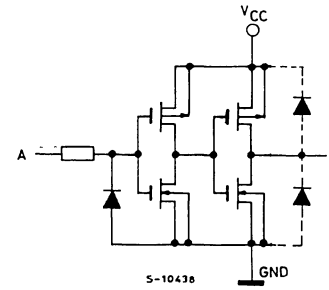
The VCC side diodes are designed to allow logic-level convertion from high-level voltages (up to 15 V) to low-level voltages.

CIRCUIT SCHEMATIC (Per Gate)

HC4049

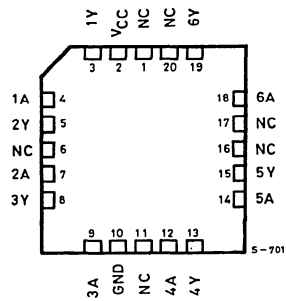


HC4050

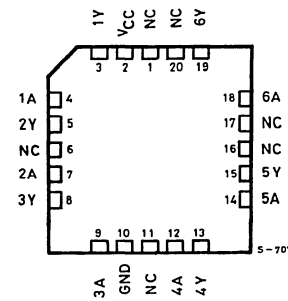


CHIP CARRIER

HC4049



HC4050



NC =No Internal Connection

TRUTH TABLE (HC4049)

INPUT	OUTPUT
nA	$n\overline{Y}$
L	H
H	L

TRUTH TABLE (HC4050)

INPUT	OUTPUT
nA	nY
L	L
H	H

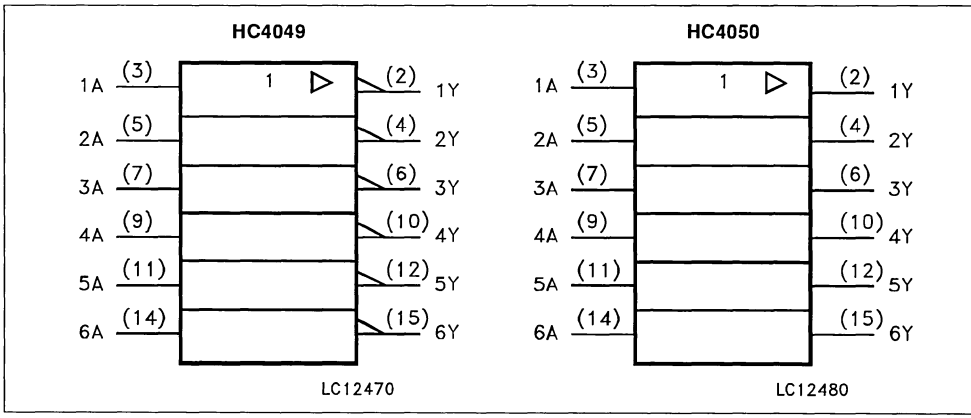
PIN DESCRIPTION (HC4049)

PIN No	SYMBOL	NAME AND FUNCTION
2, 4, 6, 10, 12, 15	$1\overline{Y}$ to $6\overline{Y}$	Data Outputs
3, 5, 7, 9, 11, 14	1A to 6A	Data Inputs
13, 16	NC	Not Connected
8	GND	Ground (0V)
1	V_{CC}	Positive Supply Voltage

PIN DESCRIPTION (HC4050)

PIN No	SYMBOL	NAME AND FUNCTION
2, 4, 6, 10, 12, 15	1Y to 6Y	Data Outputs
3, 5, 7, 9, 11, 14	1A to 6A	Data Inputs
13, 16	NC	Not Connected
8	GND	Ground (0V)
1	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND V_I = 15 V				±0.1 ±0.5		±1 ±5		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	µA

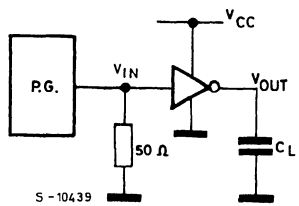
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0	50			30	75		95		115	ns
		4.5				9	15		19		23	
		6.0				8	13		16		20	
		2.0	150			45	100		125		150	ns
		4.5				14	20		25		30	
		6.0				12	17		21		26	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance					26						pF

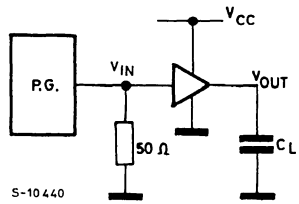
C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$ (per Gate)

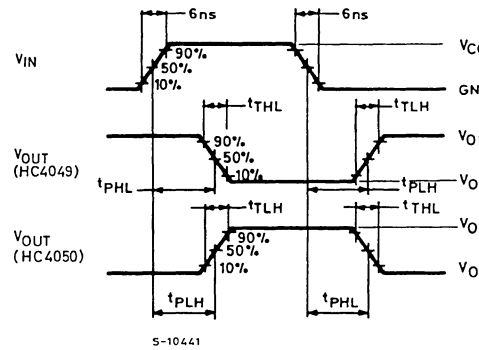
SWITCHING CHARACTERISTICS TEST WAVEFORM

HC4049



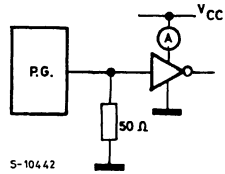
HC4050



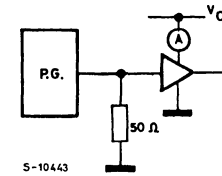


TEST CIRCUIT I_{CC} (Opr.)

HC4049



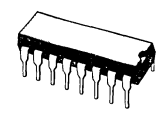
HC4050



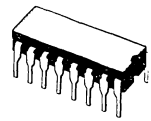
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

ANALOG MULTIPLEXER/DEMULTIPLEXER: SINGLE 8 CHANNEL, DUAL 4 CHANNEL, TRIPLE 2 CHANNEL

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- LOGIC LEVEL TRANSLATION TO ENABLE 5V LOGIC SIGNAL TO COMMUNICATE WITH ±5V ANALOG SIGNAL
- LOW "ON" RESISTANCE:
  70Ω TYP. (V_{CC} - V_{EE} = 4.5 V)
  50Ω TYP. (V_{CC} - V_{EE} = 9 V)
- WIDE ANALOG INPUT VOLTAGE RANGE: ±6V
- FAST SWITCHING:
  t_{pd} = 15 ns (TYP.) AT T_A = 25 °C
- LOW CROSSTALK BETWEEN SWITCHES
- HIGH ON/OFF OUTPUT VOLTAGE RATIO
- WIDE OPERATING VOLTAGE RANGE
  (V_{CC} - V_{EE}) = 2V TO 12V
- LOW SINE WAVE DISTORTION
  0.02% AT V_{CC} - V_{EE} = 9V
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28 % V_{CC} (MIN.)
- PIN AND FUNCTION COMPATIBLE WITH HCC/HCF4051/4052/4053B



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

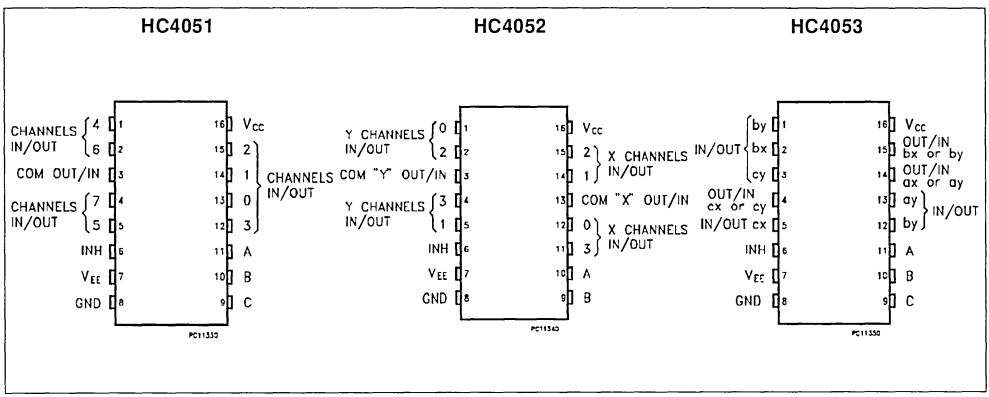
ORDER CODES :

M54HCXXXXF1R M74HCXXXXM1R
M74HCXXXXB1R M74HCXXXXC1R

DESCRIPTION

These devices are analog multiplexer demultiplexers in high speed silicon gate C²MOS technology and they are pin compatible with the equivalent metal gate CMOS "4000B" series. These analog switches are bidirectional and digitally controlled.
A built-in level shifting is included to allow them an input range of up to ± 6V (peak) for an analog signal with digital control signal of 0 to 6V.
V_{EE} supply pin is provided for analog input signals. They have an inhibit (INH) input terminal to disable all the switches when high. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND.

PIN CONNECTION (top view)



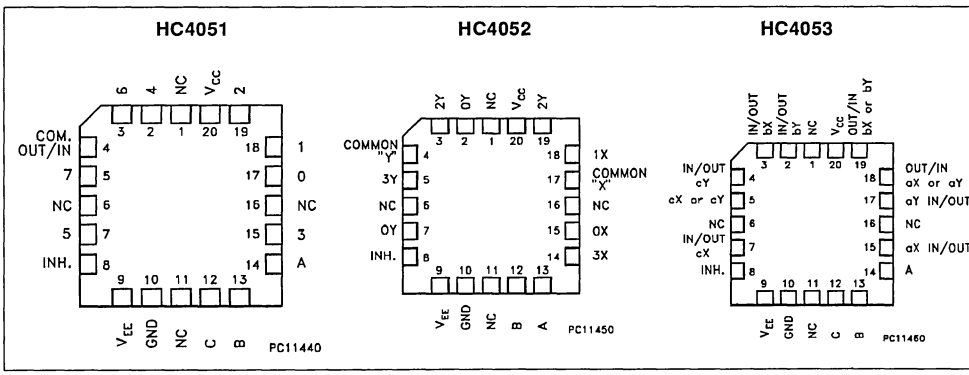
DESCRIPTION

The HC4051 is a single 8 channel multiplexer demultiplexer having three binary control inputs A, B and C to select 1 of 8 to be turned on, and connected to the output.

The HC4052 has a pair of four channel multiplexer demultiplexer having two control inputs A and B that select one of four channels of the two sections.

The HC4053 is a triple two channel multiplexer demultiplexer having three separate digital control inputs A, B and C to select independently one of a pair of channles.

CHIP CARRIER



TRUTH TABLE (HC4051)

INPUT STATES				"ON" CHANNEL
INHIBIT	C	B	A	
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	X	X	X	NONE

X: DON'T CARE

TRUTH TABLE (HC4052)

INPUT STATES			"ON" CHANNELS
INHIBIT	B	A	
L	L	L	0X, 0Y
L	L	H	1X, 1Y
L	H	L	2X, 2Y
L	H	H	3X, 3Y
H	X	X	NONE

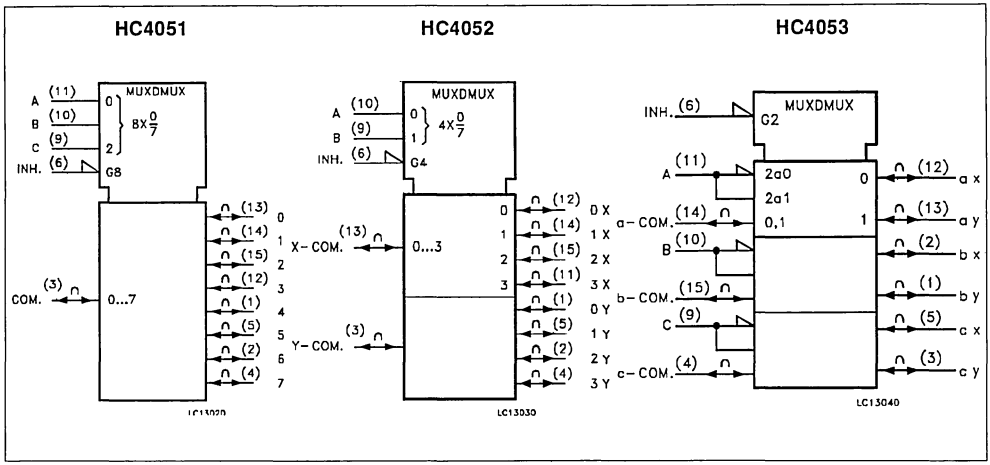
X: DON'T CARE

TRUTH TABLE (HC4053)

INPUT STATES		"ON" CHANNELS
INHIBIT	A or B or C	
L	L	ax or bx or cx
L	H	ay or by or cy
H	X	NONE

X: DON'T CARE

IEC LOGIC SYMBOLS



PIN DESCRIPTION (HC4051)

PIN No	SYMBOL	NAME AND FUNCTION
3	COM OUT/IN	Common Output/input
6	INH	INHIBIT Input
7	V_{EE}	Negative Supply Voltage
11, 10, 9	A, B, C	Select Inputs
13, 14, 15, 12, 1, 5, 2, 4	0 TO 7	Independent Input/Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

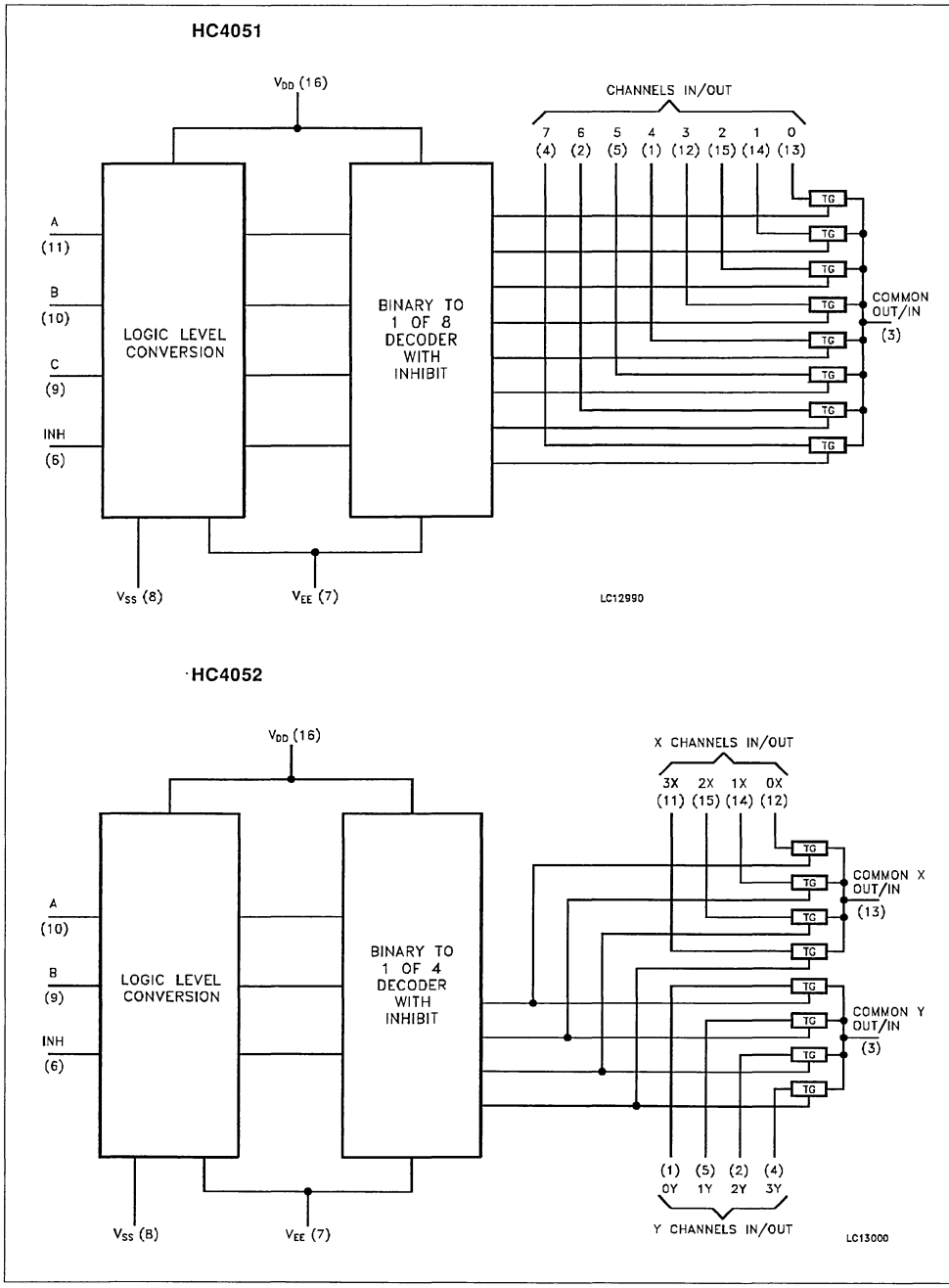
PIN DESCRIPTION (HC4052)

PIN No	SYMBOL	NAME AND FUNCTION
1, 5, 2, 4	0Y TO 3Y	Independent Input/Outputs
6	INH	INHIBIT Input
7	V_{EE}	Negative Supply Voltage
10, 9	A, B	Select Inputs
12, 14, 15, 11	0X TO 3X	Independent Input/Outputs
3	COM Y OUT/IN	Common X Output/input
13	COM X OUT/IN	Common Y Output/input
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

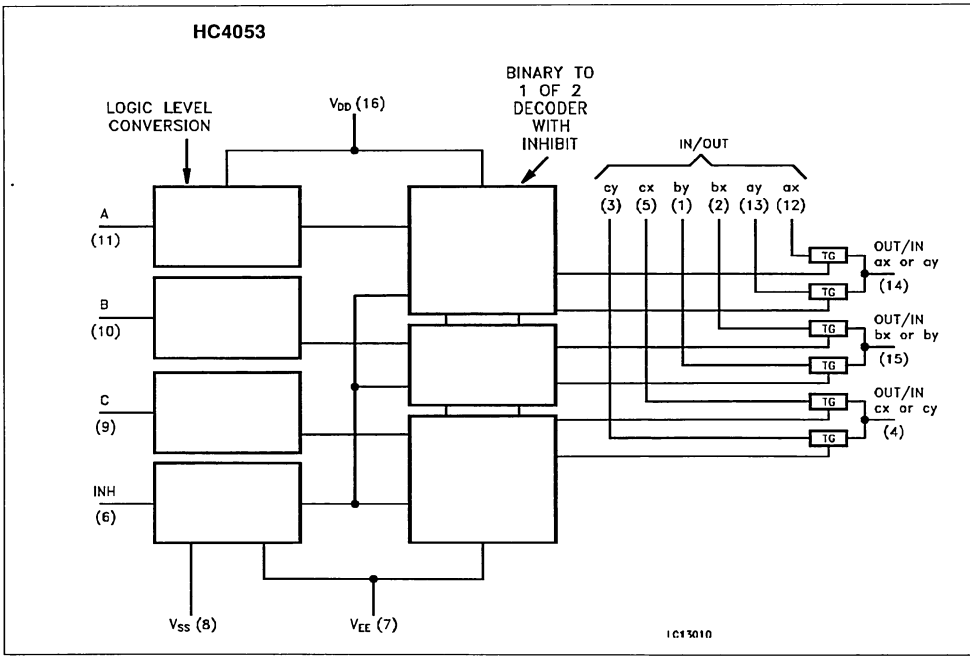
PIN DESCRIPTION (HC4053)

PIN No	SYMBOL	NAME AND FUNCTION
2, 1	bx, by	Independent Input/Outputs
5, 3	cx, cy	Independent Input/Outputs
6	INH	INHIBIT Input
7	V_{EE}	Negative Supply Voltage
11, 10, 9	A, B, C	Select Inputs
12, 13	ax, ay	Independent Input/Outputs
14, 15, 4	ax TO cy	Common Output/input
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

FUNCTIONAL DIAGRAM



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage Range	-0.5 to +7	V
V_{CC} - V_{EE}	Supply Voltage Range	-0.5 to 13	V
V_{IN}	Control Input Voltage	-0.5 to V_{CC} + 0.5	V
$V_{I/O}$	Switch I/O Voltage	V_{EE} - 0.5 to V_{CC} + 0.5	V
I_{CK}	Control Input Diode Current	± 20	mA
I_{IOK}	I/O Diode Current	± 20	mA
I_T	Switch Through Current	± 25	mA
I_{CC}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_{EE}	Supply Voltage		-6 to 0	V
V_{CC} - V_{EE}	Supply Voltage		2 to 12	V
V_{IN}	Input Voltage		0 to V_{CC}	V
$V_{I/O}$	Input/Output Voltage		V_{EE} to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	V_{EE} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IHC}	High Level Control Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{ILC}	Low Level Control Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
R_{ON}	ON Resistance	4.5	GND	V_{IN} = V_{IHC} or V_{ILC} $V_{I/O}$ = V_{CC} to V_{EE} $I_{I/O} \leq$ 2 mA		85	180		225		270	Ω
		4.5	-4.5			55	120		150		180	
		6.0	-6.0			50	100		125		150	
		2.0	GND	V_{IN} = V_{IHC} or V_{ILC} $V_{I/O}$ = V_{CC} or V_{EE} $I_{I/O} \leq$ 2 mA		150						
		4.5	GND			70	150		190		230	
		4.5	-4.5			50	100		125		150	
		6.0	-6.0			45	80		100		120	
ΔR_{ON}	Difference of ON Resistance Between Switches	4.5	GND	V_{IN} = V_{IHC} or V_{ILC} $V_{I/O}$ = V_{CC} or V_{EE} $I_{I/O} \leq$ 2 mA		10	30		35		45	Ω
		4.5	-4.5			5	12		15		18	
		6.0	-6.0			5	10		12		15	
I_{OFF}	Input/Output Leakage Current (SWITCH OFF)	6.0	GND	V_{OS} = V_{CC} or GND V_{IS} = GND or V_{CC} V_{IN} = V_{ILC} or V_{IHC}			±0.06		±0.6		±1.2	µA
		6.0	-6.0				±0.1		±1		±2	
I_{IZ}	Switch Input Leakage Current (SWITCH ON, OUTPUT OPEN)	6.0	GND	V_{OS} = V_{CC} or GND V_{IN} = V_{IHC} or V_{ILC}			±0.06		±0.6		±1.2	µA
		6.0	-6.0				±0.1		±1		±2	
I_{IN}	Control Input Current	6.0	GND	V_{IN} = V_{CC} or GND			±0.1		±0.1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	GND	V_{IN} = V_{CC} or GND			4		40		80	µA
		6.0	-6.0				8		80		160	

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	V_{EE} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$\Phi_{I/O}$	Phase Difference Between Input and Output	2.0	GND			25	60		75		90	ns
		4.5	GND			6	12		15		18	
		6.0	GND			5	10		13		15	
		4.5	-4.5			4						
t_{PZL} t_{PZH}	Output Enable Time (for 4051/4052)	2.0	GND	R_L = 1KΩ		64	225		280		340	ns
		4.5	GND			18	45		56		68	
		6.0	GND			15	38		48		58	
		4.5	-4.5			18						
t_{PZL} t_{PZH}	Output Enable Time (for 4053)	2.0	GND	R_L = 1KΩ		50	225		280		340	ns
		4.5	GND			14	45		56		68	
		6.0	GND			12	38		48		58	
		4.5	-4.5			14						
t_{PLZ} t_{PHZ}	Output Disable Time (for 4051/4052)	2.0	GND	R_L = 1KΩ		100	250		315		375	ns
		4.5	GND			33	50		63		7	
		6.0	GND			28	43		54		64	
		4.5	-4.5			29						
t_{PLZ} t_{PHZ}	Output Disable Time (for 4053)	2.0	GND	R_L = 1KΩ		95	225		280		340	ns
		4.5	GND			30	45		56		68	
		6.0	GND			26	38		48		58	
		4.5	-4.5			26						
C_{IN}	Input Capacitance					5	10		10		10	pF
$C_{I/O}$	Common Terminal Capacitance	5.0	-5.0	HC4051		36	70		70		70	pF
				HC4052		19	40		40		40	
				HC4053		11	20		20		20	
$C_{I/O}$	Switch Terminal Capacitance	5.0	-5.0	HC4051		7	15		15		15	pF
				HC4052		7	15		15		15	
				HC4053		7	15		15		15	
C_{IOS}	Feed Through Capacitance	5.0	-5.0	HC4051		0.95	2		2		2	pF
				HC4052		0.85	2		2		2	
				HC4053		0.75	2		2		2	
C_{PD} (*)	Power Dissipation Capacitance	5.0	GND	HC4051		70						pF
				HC4052		71						
				HC4053		67						

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

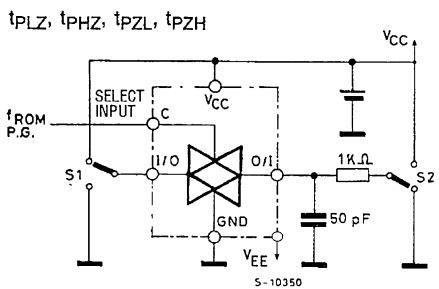
ANALOG SWITCH CHARACTERISTICS (GND = 0 V T_A = 25 °C)

Symbol	Parameter	Test Conditions					Value	Unit
		V_{CC} (V)	V_{EE} (V)	VIN (Vp-p)			Typ.	
	Sine Wave Distortion	2.25	2.25	4	f_{IN} = 1 KHz R_L = 10 KΩ C_L = 50 pF		0.025	%
		4.5	-4.5	8			0.020	
		6.0	-6.0	11			0.018	
f_{MAX}	Frequency Response (Switch ON)	2.25	-2.25	Adjust f_{IN} voltage to Obtain 0 dBm at V_{OS}. Increase f_{IN} Frequency until dB Meter Reads -3dB R_L = 50 Ω C_L = 10 pF f_{IN} = 1 KHz sine wave	ALL (*)		120	MHz
					HC4051 (**)		45	
					HC4052 (**)		70	
					HC4053 (**)		95	
		4.5	-4.5		ALL (*)		190	
					HC4051 (**)		70	
					HC4052 (**)		110	
					HC4053 (**)		150	
		6.0	-6.0		ALL (*)		200	
					HC4051 (**)		85	
					HC4052 (**)		140	
					HC4053 (**)		190	
	Feedthrough Attenuation (Switch OFF)	2.25	-2.25	V_{IN} is centered at (V_{CC} - V_{EE})/2. Adjust input for 0 dBm R_L = 600 Ω C_L = 50 pF f_{IN} = 1 KHz sine wave			-50	dB
		4.5	-4.5				-50	
		6.0	-6.0				-50	
	Crosstalk (Control Input to Signal Output)	2.25	-2.25	Adjust RL at set up so that I_S = 0A R_L = 600 Ω C_L = 50 pF f_{IN} = 1 MHz square wave			60	mV
		4.5	-4.5				140	
		6.0	-6.0				200	
	Crosstalk (Between Any Switches)	2.25	-2.25	Adjust V_{IN} to Obtain 0 dBm at Input R_L = 600 Ω C_L = 50 pF f_{IN} = 1 MHz sine wave			-50	dB
		4.5	-4.5				-50	
		6.0	-6.0				-50	

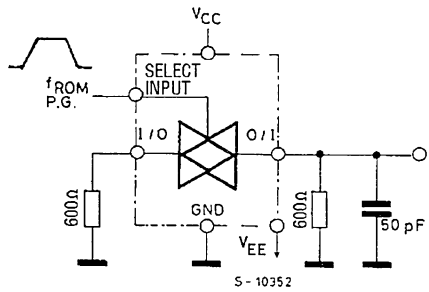
(*): Input COMMON Terminal, and measured at SWITCH Terminal.
(**): Input SWITCH Terminal, and measured at COMMON Terminal.
NOTE: These characteristics are determined by design of devices.

SWITCHING CHARACTERISTICS TEST CIRCUIT

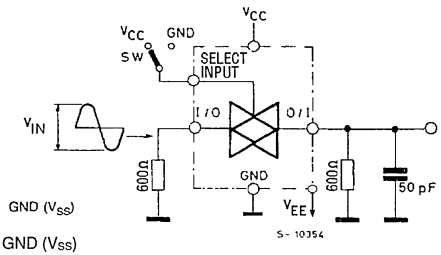
t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}.



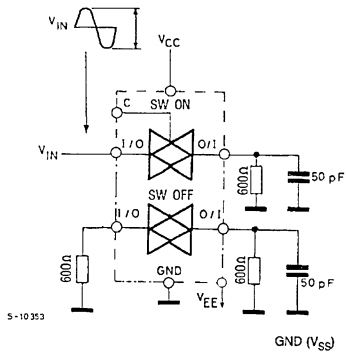
CROSSTALK (control to output)



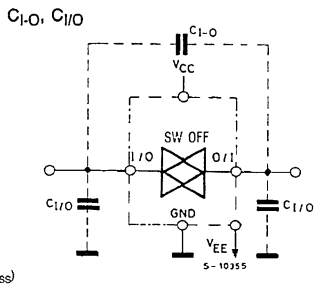
BANDWIDTH AND FEEDTHROUGH ATTENUATION



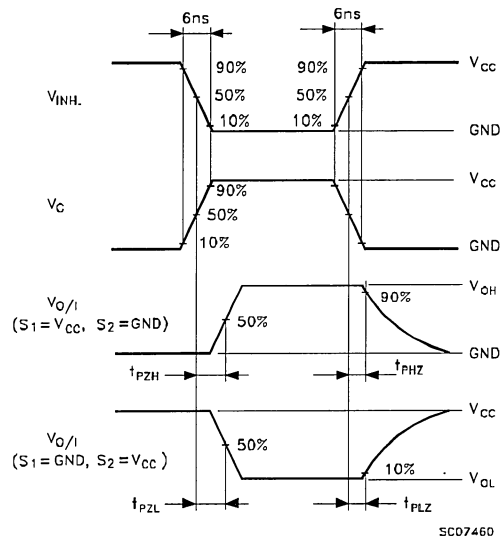
CROSSTALK BETWEEN ANY TWO SWITCHES



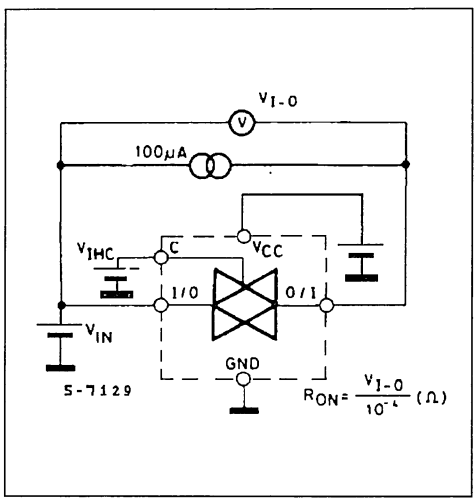
C_{I-O} $C_{I/O}$



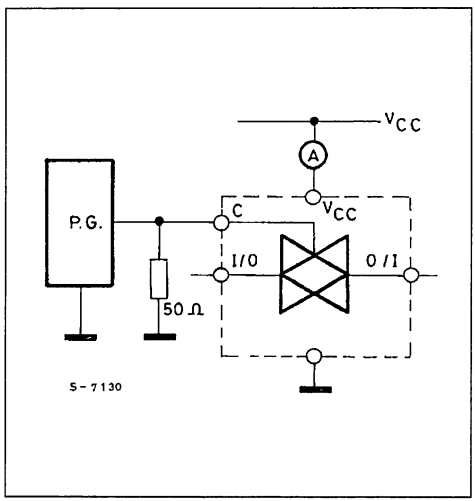
SWITCHING CHARACTERISTICS TEST WAVEFORM



CHANNEL RESISTANCE (R_{ON})

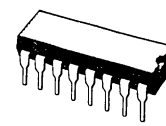


I_{CC} (Opr.)

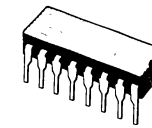


14 STAGE BINARY COUNTER/OSCILLATOR

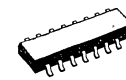
- HIGH SPEED
  f_{MAX} = 58 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 4060B



B1R
(Plastic Package)



F1R
(Ceramic Package)



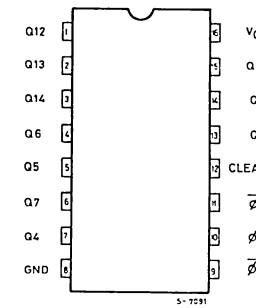
M1R
(Micro Package)

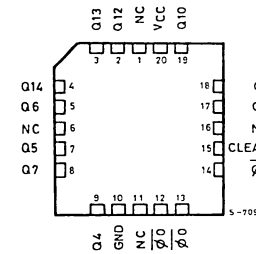
C1R
(Chip Carrier)

ORDER CODES :

M54HC4060F1R M74HC4060M1R
M74HC4060B1R M74HC4060C1R

PIN CONNECTIONS (top view)





NC =
No Internal
Connection

DESCRIPTION

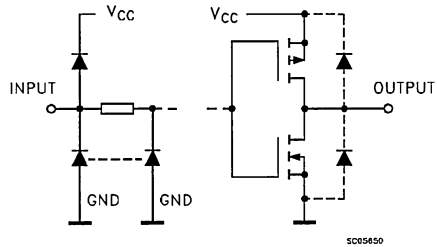
The M54/74HC4060 is a high speed CMOS 14-STAGE BINARY COUNTER/OSCILLATOR fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. It operates ten times faster than metal-gate C^2MOS IC (4060B) with the same power dissipation.

The oscillator configuration allows design of either RC or crystal oscillator circuits. A high level on the CLEAR accomplishes the reset function, i.e. all counter outputs are made low and the oscillator is disabled.

A negative transition on the clock input increments the counter. Ten kinds of divided output are provided ; 4 to 10 and 12 to 14 stage inclusive. The maximum division available at Q12 is 1/16384 f oscillator.

The $\overline{\varnothing_1}$ input and the CLEAR input are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT

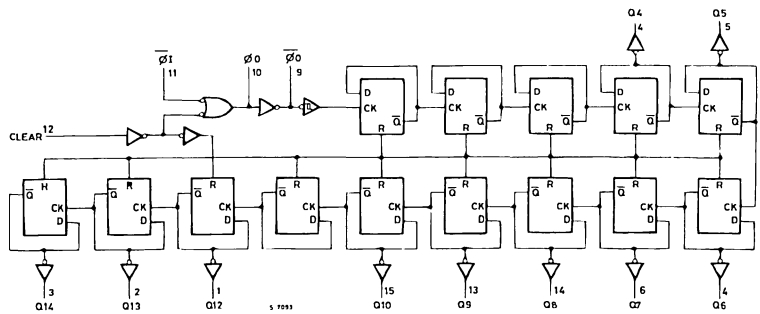


TRUTH TABLE

$\overline{øi}$	CLEAR	FUNCTION
X	H	COUNTER IS RESET TO ZERO STATE ø0 OUTPUT GOES TO HIGH LEVEL $\overline{ø0}$ OUTPUT GOES TO LOW LEVEL
⌐	L	COUNT UP ONE STEP
⌐	L	NO CHANGE

X: DON'T CARE

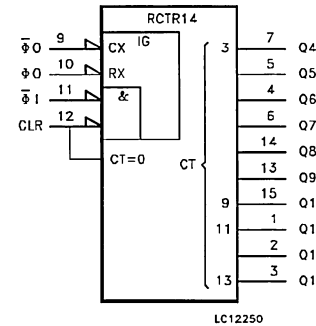
LOGIC DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3	Q12 to Q14	Counter Outputs
7, 5, 4, 6, 14, 13, 15	Q4 to Q10	Counter Outputs
9	$\overline{\text{ø}}\text{O}$	External Capacitor Connection
10	øO	External Resistor Connection
11	$\overline{\text{ø}}\text{I}$	Clock Input/Oscillator Pin
12	CLEAR	Master Reset
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

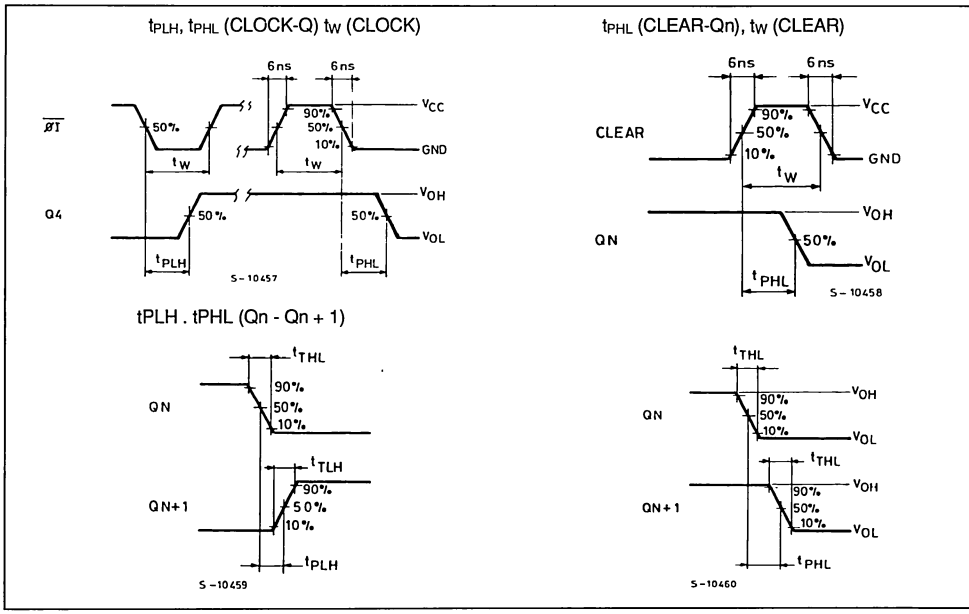
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage (Q Outputs)	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage (Q Outputs)	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
V_{OH}	High Level Output Voltage (øO, ø$\overline{O}$ Output)	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.8	2.0		1.8		1.8		V
		4.5			4.4	4.5		4.0		4.0		
		6.0			5.5	5.9		5.5		5.5		
V_{OL}	Low Level Output Voltage (øO, ø$\overline{O}$ Output)	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.2		0.2		0.2	V
		4.5				0.0	0.5		0.5		0.5	
		6.0				0.1	0.5		0.5		0.5	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

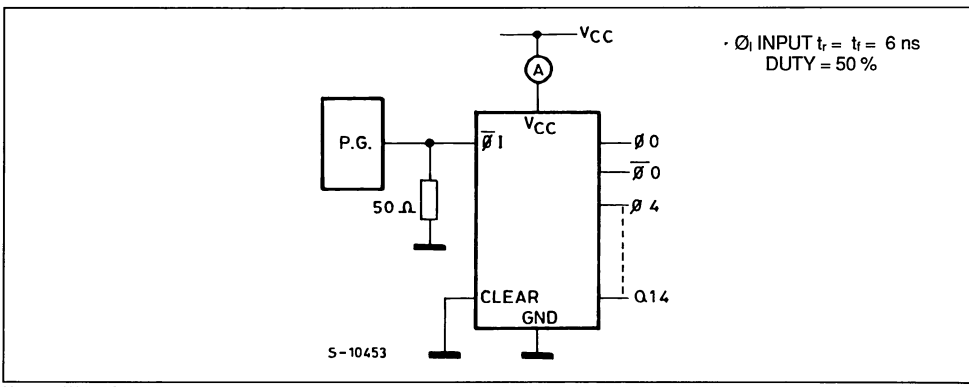
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (øI - Q4)	2.0			170	300		375		450	ns
		4.5			41	60		75		90	
		6.0			30	51		64		76	
t_{PD}	Propagation Delay Time Difference (Qn- Qn+1)	2.0			32	75		95		110	ns
		4.5			7	15		19		22	
		6.0			5	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLEAR - Qn)	2.0			85	195		245		295	ns
		4.5			23	39		49		59	
		6.0			17	33		42		50	
f_{MAX}	Maximum Clock Frequency	2.0		6	12		5		4		ns
		4.5		30	50		24		20		
		6.0		35	65		28		24		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (øI)	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
$t_{W(H)}$	Minimum Pulse Width (CLEAR)	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{REM}	Minimum Removal Time	2.0			40	100		125		150	ns
		4.5			10	20		25		30	
		6.0			9	17		21		26	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				27						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit) Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST CIRCUIT



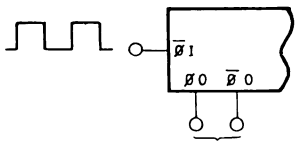
TEST CIRCUIT Icc (Opr.)



Note : When CR or crystal oscillation circuit is adopted, the dynamic power dissipation will be greater than the measured value from the test circuit shown left, because these oscillion circuits spend much supply current.

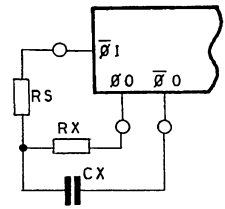
TYPICAL CLOCK DRIVE CIRCUITS

EXTERNAL CLOCK DRIVE



S-10454

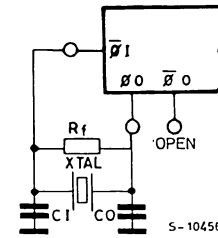
TYPICAL CIRCUIT



R 8 : 2RX ~ 10RX

S-10455

TYPICAL CRYSTAL CIRCUIT



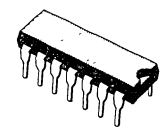
S-10456

SGS-THOMSON MICROELECTRONICS

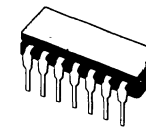
M54HC4066
M74HC4066

QUAD BILATERAL SWITCH

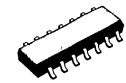
- HIGH SPEED
  t_{PD} = 7 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28 % V_{CC} (MIN.)
- LOW "ON" RESISTANCE
  R_{ON} = 50 Ω (TYP.) AT V_{CC} = 9 V, $I_{I/O}$ = 100 µA
- SINE WAVE DISTORTION
- 0.042% (TYP.) AT V_{CC} = 4V f = 1KHz
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 12 V
- PIN AND FUNCTION COMPATIBLE
  WITH 4066B



B1R
(Plastic Package)



F1R
(Ceramic Package)



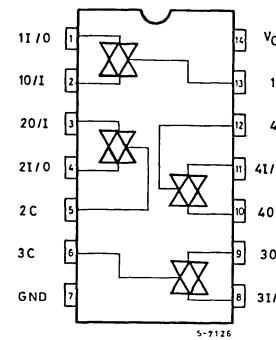
M1R
(Micro Package)

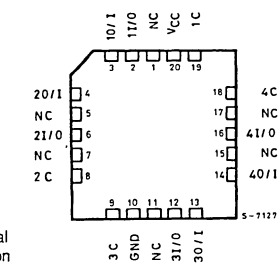
C1R
(Chip Carrier)

ORDER CODES :

M54HC4066F1R M74HC4066M1R
M74HC4066B1R M74HC4066C1R

PIN CONNECTIONS (top view)





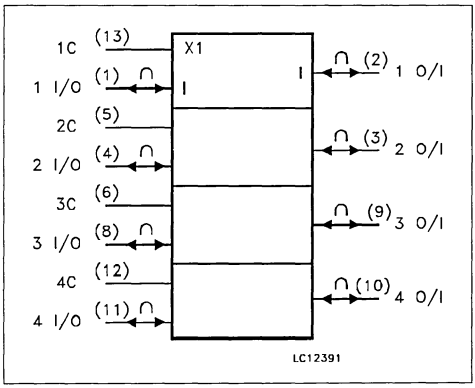
NC =
No Internal
Connection

DESCRIPTION

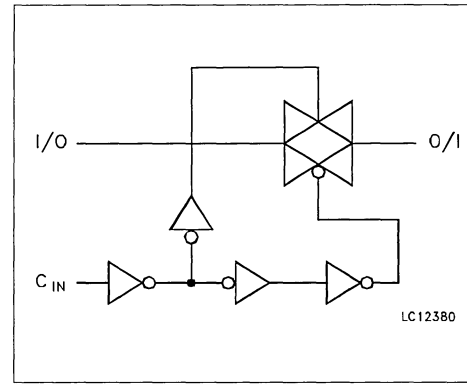
The M54/74HC4066 is a high speed CMOS QUAD BILATERAL SWITCH fabricated in silicon gate C^2MOS technology. It has high speed performance combined with true CMOS low power consumption.

The C input is provided to control the switch ; the switch is ON when the C input is held high and off when C is held low.

IEC LOGIC SYMBOL



LOGIC DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 8, 11	1 to 4 I/O	Independent Inputs/Outputs
2, 3, 9, 10	1 to 4 O/I	Independent Outputs/Inputs
13, 5, 6, 12	1C to 4C	Enable Inputs (Active HIGH)
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

TRUTH TABLE

CONTROL	SWITCH FUNCTION
H	ON
L	OFF

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +13	V
V_{IN}	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
$V_{I/O}$	DC Input/Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{OK}	Control Input DC Diode Current	± 20	mA
I_{IOK}	I/O DC Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 12	V
V_{IN}	Input Voltage (Control)		0 to V_{CC}	V
$V_{I/O}$	Input/Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	
		V_{CC} = 10 V	0 to 250	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IHC}	High Level Control Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		9.0		6.3			6.3		6.3		
		12.0		8.4			8.4		8.4		
V_{ILC}	Low Level Control Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		9.0				2.7		2.7		2.7	
		12.0				3.6		3.6		3.6	
R_{ON}	ON Resistance	4.5	V_{IN} = V_{IHC} V_{IO} = V_{CC} to GND $I_{IO} \leq$ 1 mA		96	170		200		250	Ω
		9.0			55	85		100		150	
		12.0			45	80		90		120	
		4.5	V_{IN} = V_{IHC} V_{IO} = V_{CC} or GND $I_{IO} \leq$ 1 mA		70	100		130		160	
		9.0			50	75		95		115	
		12.0			45	70		90		110	
ΔR_{ON}	Difference of ON Resistance Between Switches	4.5	V_{IN} = V_{IHC} V_{IO} = V_{CC} or GND $I_{IO} \leq$ 1 mA		10						Ω
		9.0			5						
		12.0			5						
I_{OFF}	Input/Output Leakage Current (SWITCH OFF)	12.0	V_{OS} = V_{CC} or GND V_{IS} = V_{CC} or GND V_{IN} = V_{ILC}			±0.1		±1		±2	µA
I_{IZ}	Switch Input Leakage Current (SWITCH ON, OUTPUT OPEN)	12.0	V_{OS} = V_{CC} or GND V_{IN} = V_{IHC}			±0.1		±1		±2	µA
I_{IN}	Control Input Current	6.0	V_{IN} = V_{CC} or GND			±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_{IN} = V_{CC} or GND			1		10		20	µA
		9.0				4		40		80	
		12.0				8		80		160	

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$\emptyset_{I/O}$	Phase Difference Between Input and Output	2.0			10	50		65		75	ns
		4.5			4	10		13		15	
		9.0			3	8		10		13	
		12.0			3	7		9		10	
t_{PZL} t_{PZH}	Output Enable Time	2.0	R_L = 1KΩ		18	100		125		150	ns
		4.5			8	20		25		30	
		9.0			6	12		22		27	
		12.0			6	12		18		25	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0	R_L = 1KΩ		20	115		145		175	ns
		4.5			10	23		29		35	
		9.0			8	20		25		30	
		12.0			8	18		22		27	
	Maximum Control Input Frequency	2.0	R_L = 1KΩ C_L = 15 pF V_{OUT} = 1/2 V_{CC}		30						MHz
		4.5			30						
		9.0			30						
		12.0			30						
C_{IN}	Input Capacitance				5	10		10		10	pF
$C_{I/O}$	Switch Terminal Capacitance				6						pF
C_{IOS}	Feed Through Capacitance				0.5						pF
C_{PD} (*)	Power Dissipation Capacitance				15						pF

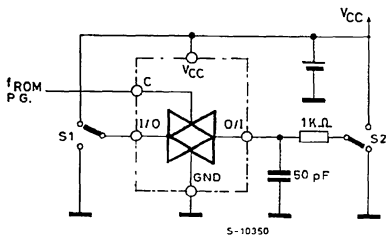
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

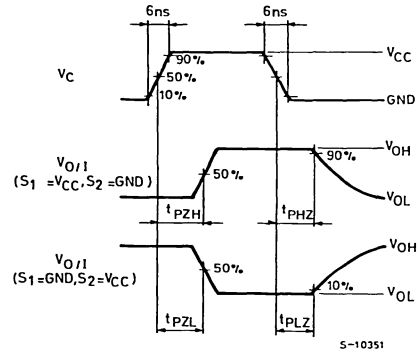
ANALOG SWITCH CHARACTERISTICS (GND = 0 V T_A = 25 °C)

Symbol	Parameter	Test Conditions			Value	Unit
		V_{CC} (V)	VIN (Vp-p)		Typ.	
	Sine Wave Distortion (THD)	4.5	4	f_{IN} = 1 KHz R_L = 10 KΩ C_L = 50 pF	0.05	%
		9.0	8		0.04	
f_{MAX}	Frequency Response (Switch ON)	4.5	Adjust f_{IN} voltage to Obtain 0 dBm at V_{OS}. Increase f_{IN} Frequency until dB Meter reads -3dB R_L = 50 Ω C_L = 10 pF		200	MHz
		9.0			200	
	Feedthrough Attenuation (Switch OFF)	4.5	V_{IN} is centered at VCC/2. Adjust input for 0 dBm R_L = 600 Ω C_L = 50 pF f_{IN} = 1 MHz sine wave		-60	dB
		9.0			-60	
	Crosstalk (Control Input to Signal Output)	4.5	R_L = 600 Ω C_L = 50 pF f_{IN} = 1 MHz square wave ($t_r = t_f$ = 6ns)		60	mV
		9.0			100	
	Crosstalk (Between Any Switches)	4.5	Adjust V_{IN} to Obtain 0 dBm at input R_L = 600 Ω C_L = 50 pF f_{IN} = 1 MHz sine wave		-60	dB
		9.0			-60	

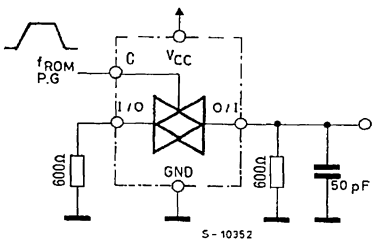
SWITCHING CHARACTERISTICS TEST CIRCUIT

t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}.

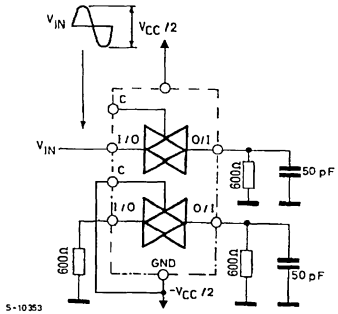




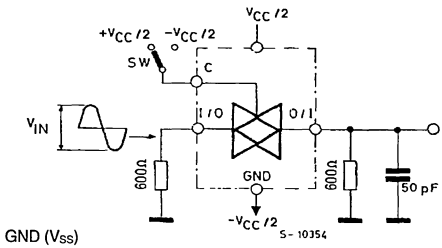
CROSSTALK (control to output)



CROSSTALK BETWEEN ANY TWO SWITCHES

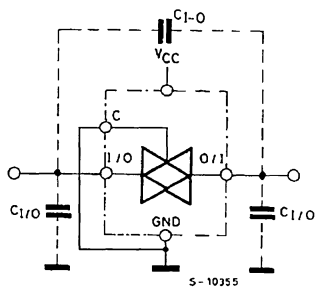


BANDWIDTH AND FEEDTHROUGH ATTENUATION



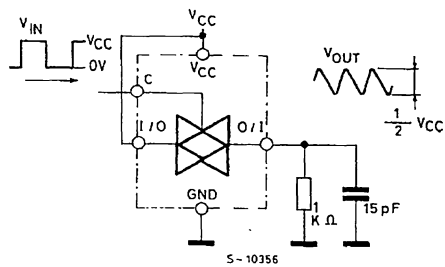
GND (V_{SS})

C_{I-O} $C_{I/O}$

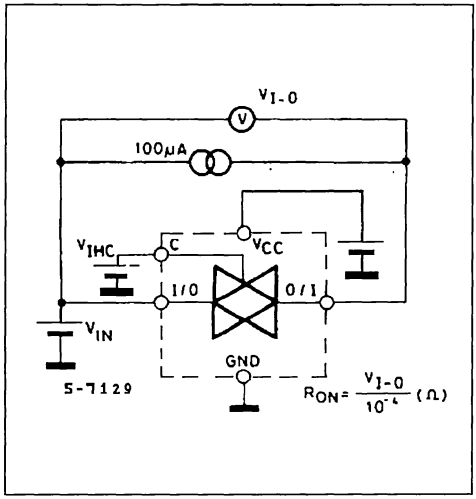


GND (V_{SS})

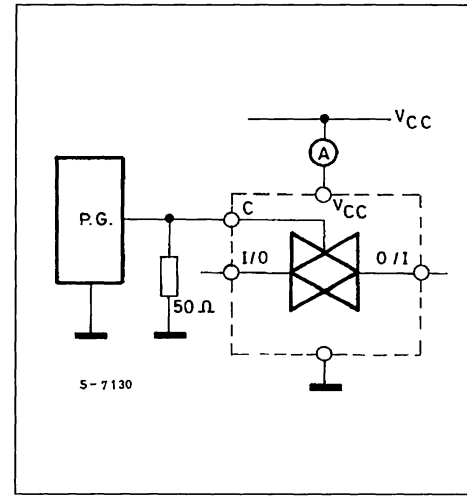
MAXIMUM CONTROL FREQUENCY



CHANNEL RESISTANCE (R_{ON})

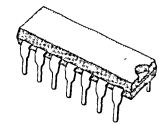


I_{CC} (Opr.)

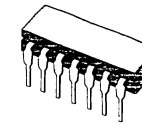


DUAL 4 INPUT OR GATE

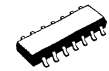
- HIGH SPEED
  t_{PD} = 9 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 4072B



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

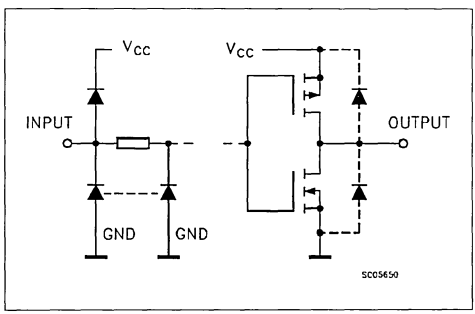
M54HC4072F1R M74HC4072M1R
M74HC4072B1R M74HC4072C1R

DESCRIPTION

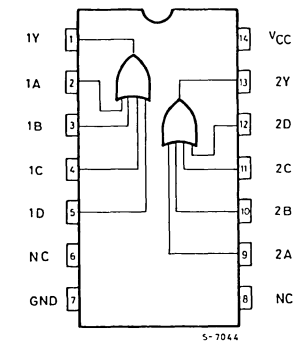
The M54/74HC4072 is a high speed CMOS DUAL 4-INPUT OR GATE fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

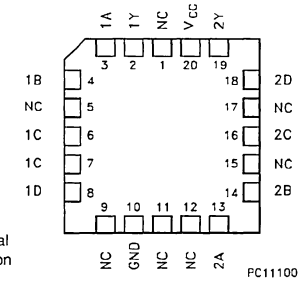
The internal circuit is composed of 3 stages including buffer output, which gives high noise immunity and stable output. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



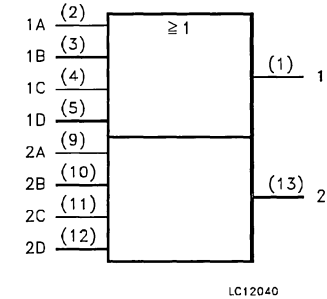


NC =
No Internal
Connection

TRUTH TABLE

A	B	C	D	Y
L	L	L	L	L
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
X	X	X	H	H

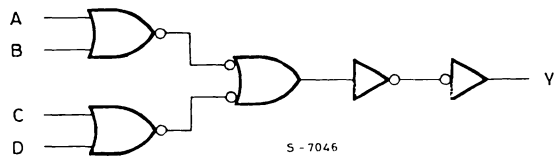
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5	1A to 1D	Data Inputs
9, 10, 11, 12	2A to 2D	Data Inputs
1, 13	1Y to 2Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

SCHEMATIC CIRCUIT (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied

(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

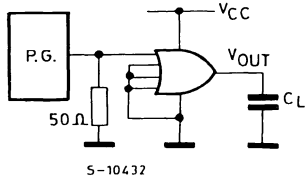
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	µA

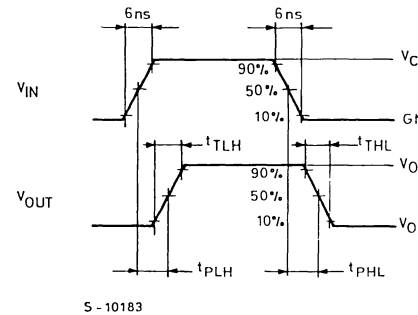
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			36	100		125		150	ns
		4.5			12	20		25		30	
		6.0			10	17		21		26	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				22						pF

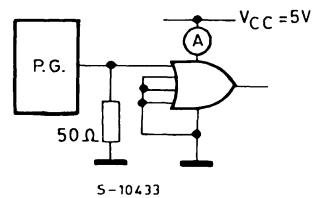
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT





TEST CIRCUIT I_{CC} (Opr.)



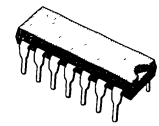
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

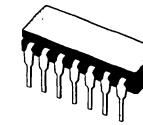
M54HC4075
M74HC4075

TRIPLE 3 INPUT OR GATE

- HIGH SPEED
  t_{PD} = 8 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 4075B



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HC4075F1R M74HC4075M1R
M74HC4075B1R M74HC4075C1R

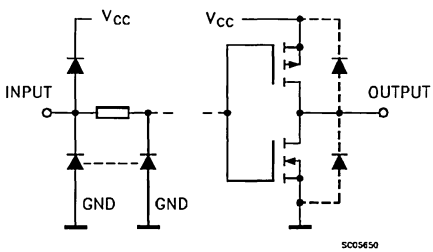
DESCRIPTION

The M54/74HC4075 is a high speed CMOS TRIPLE 3-INPUT OR GATE fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

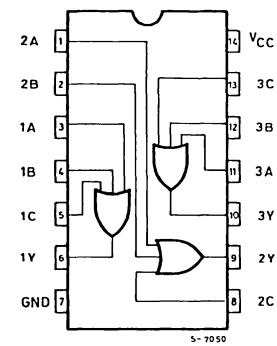
The internal circuit is composed of 4 stages including buffered output, which gives high noise immunity and a stable output.

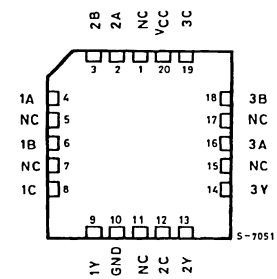
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



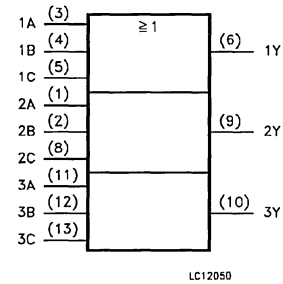


NC = No Internal Connection

TRUTH TABLE

A	B	C	Y
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

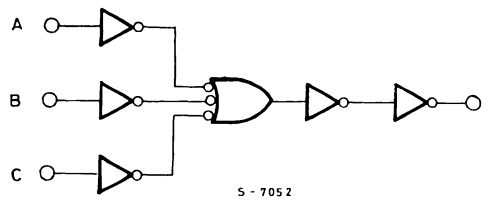
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
3, 1, 11	1A to 3A	Data Inputs
4, 2, 12	1B to 3B	Data Inputs
5, 8, 13	1C to 3C	Data Inputs
6, 9, 10	1Y to 3Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

SCHEMATIC CIRCUIT (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

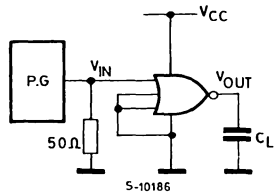
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	µA

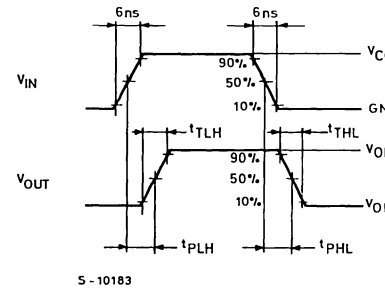
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			40	80		100		120	ns
		4.5			10	16		20		24	
		6.0			9	14		17		20	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				24						pF

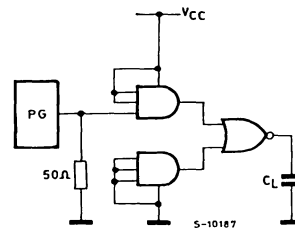
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/3$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT





TEST CIRCUIT I_{CC} (Opr.)



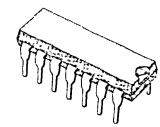
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

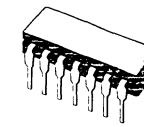
M54HC4078
M74HC4078

8 INPUT NOR/OR GATE

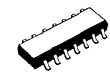
- HIGH SPEED
  t_{PD} = 13 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 4078B



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

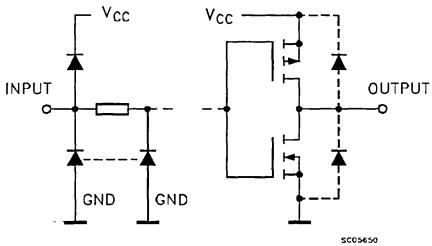
M54HC4078F1R M74HC4078M1R
M74HC4078B1R M74HC4078C1R

DESCRIPTION

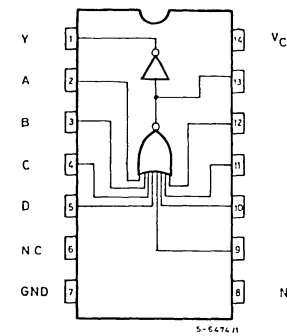
The M54/74HC4078 is a high speed CMOS 8 INPUT NOR/OR GATE fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

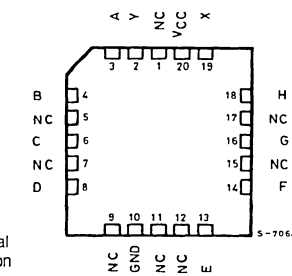
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



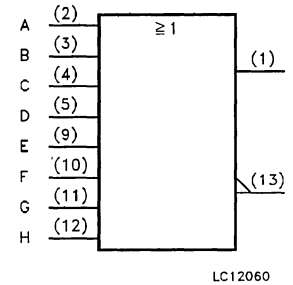


NC =
No Internal
Connection

TRUTH TABLE

INPUTS	OUTPUTS	
	X	Y
ALL INPUTS "L"	H	L
OTHER POSSIBILITIES	L	H

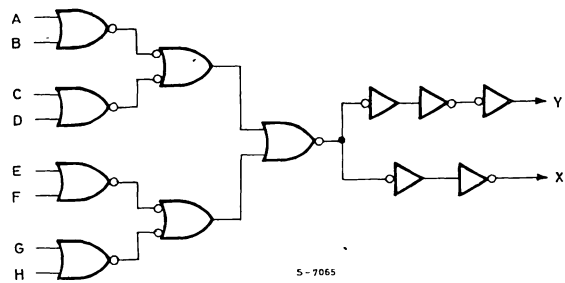
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5, 9, 10, 11, 12	A to H	Data Inputs
1, 13	Y, X	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

SCHEMATIC CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur Functional operation under these condition is not implied

(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

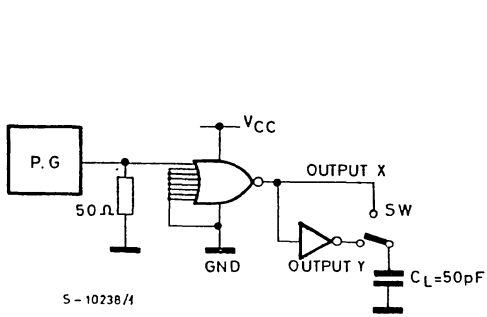
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	µA

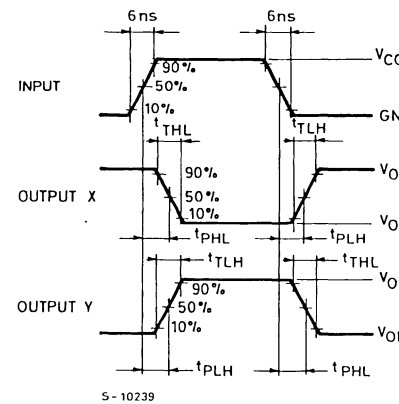
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value						Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC	
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			48	95		120		145	ns
		4.5			12	19		24		29	
		6.0			10	16		20		25	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				37						pF

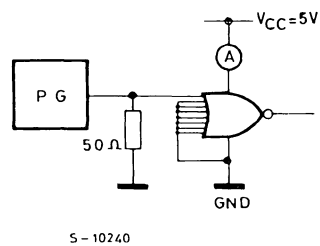
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit) Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST CIRCUIT





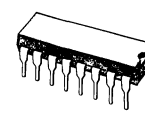
TEST CIRCUIT I_{CC} (Opr.)



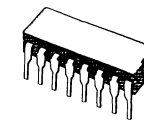
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

8 BIT SIPO SHIFT LATCH REGISTER (3-STATE)

- HIGH SPEED
  f_{MAX} = 73 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 4094B



B1R
(Plastic Package)



F1R
(Ceramic Package)

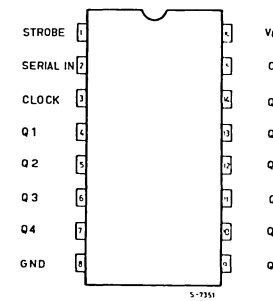
M1R
(Micro Package)

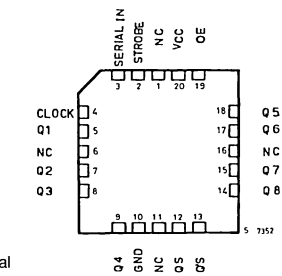
C1R
(Chip Carrier)

ORDER CODES :

M54HC4094F1R M74HC4094M1R
M74HC4094B1R M74HC4094C1R

PIN CONNECTIONS (top view)





NC =
No Internal
Connection

DESCRIPTION

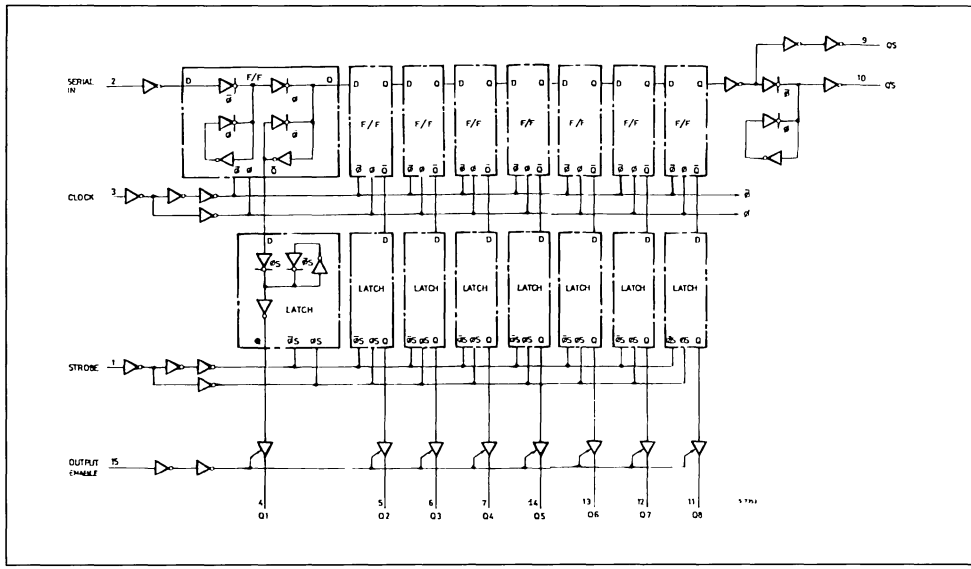
The M54/74HC4094 is a high speed CMOS 8 BIT SIPO SHIFT LATCH REGISTER fabricated with silicon gate C^2MOS technology.

It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This device consists of an 8-bit shift register and an 8-bit latch with 3-state output buffer. Data is shifted serially through the shift register on the positive going transition of the clock input signal. The output of the last stage (Qs) can be used to cascade several devices.

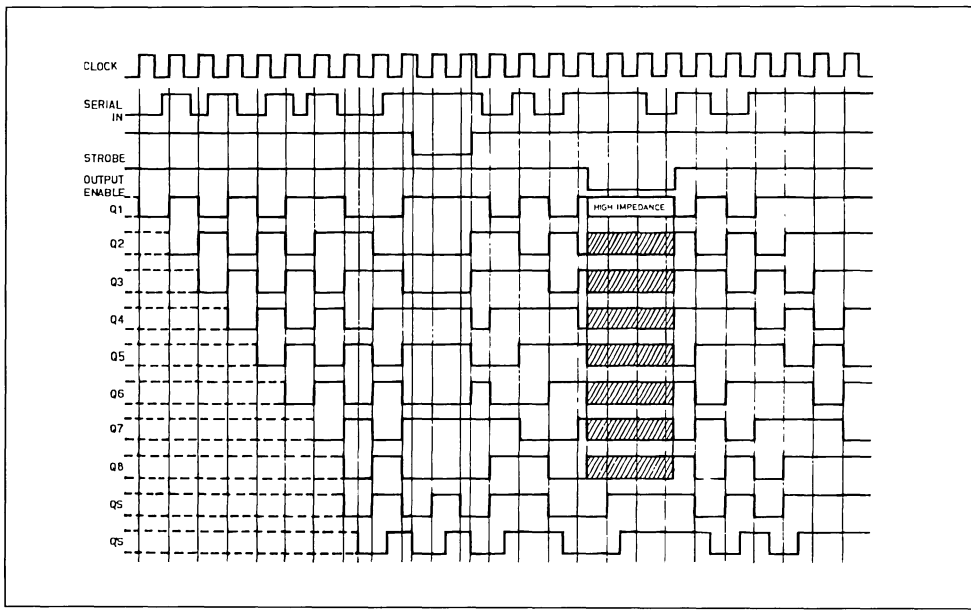
Data on the Qs output is transferred to a second output (Qs') on the following negative transition of the clock input signal. The data of each stage of the shift register is provided with a latch, which latches data on the negative going transition of the STROBE input signal. When the STROBE input is held high, data propagates through the latch to a 3-state output buffer.

This buffer is enabled when OUTPUT ENABLE input is taken high. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

LOGIC DIAGRAM



LOGIC DIAGRAM

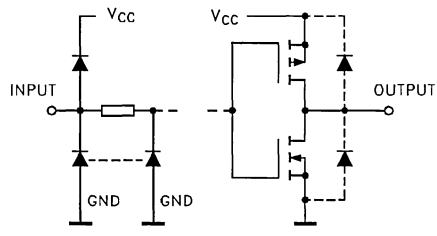


TRUTH TABLE

CK	OE	ST	SI	PARALLEL OUTPUT		SERIAL OUTPUT	
				Q1	Qn	Qs	Qs'
⌐	H	H	L	L	Qn-1	Q7	NC
⌐	H	H	H	H	Qn-1	Q7	NC
⌐	H	L	X	NC	NC	Q7	NC
⌐	L	X	X	Z	Z	Q7	NC
⌐	H	X	X	NC	NC	NC	Qs
⌐	L	X	X	Z	Z	NC	Qs

X. Don't Care Z. High Impedance NC. No Change

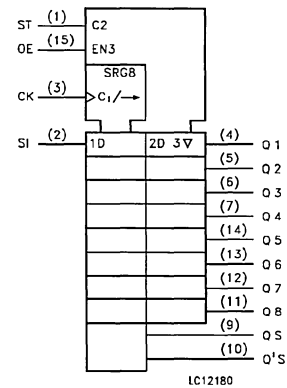
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	STROBE	Strobe Input
2	SERIAL IN	Serial Input
3	CLOCK	Clock Input
4, 5, 6, 7, 14, 13, 12, 11	Q1 to Q7	Parallel Outputs
9, 10	QS Q'S	Serial Outputs
15	OE	Output Enable Input
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series		-55 to +125	°C
	M74HC Series		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

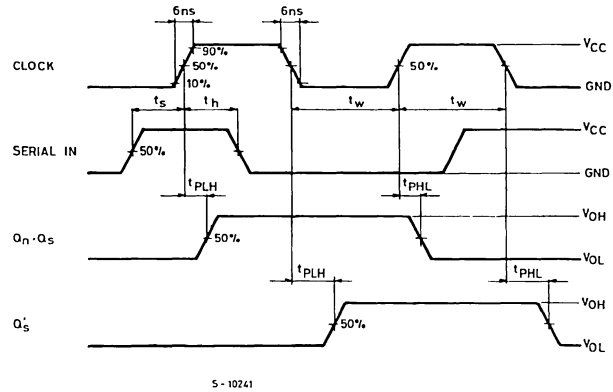
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	.Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.37		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.37		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5.0		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

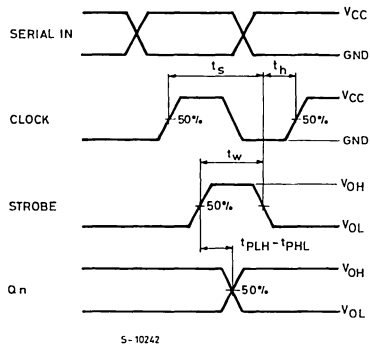
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

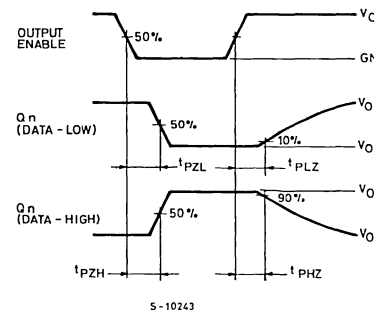
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Qn)	2.0			92	200		250		300	ns
		4.5			26	40		50		60	
		6.0			20	34		43		51	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - QS, QS)	2.0			65	150		190		225	ns
		4.5			19	30		38		45	
		6.0			15	26		32		38	
t_{PLH} t_{PHL}	Propagation Delay Time (STROBE - Qn)	2.0			75	160		200		240	ns
		4.5			20	32		40		48	
		6.0			16	27		34		41	
t_{PZL} t_{PZH}	3 State Output Enable Time	2.0			58	150		190		225	ns
		4.5			16	30		38		45	
		6.0			13	26		32		38	
t_{PHZ} t_{PLZ}	3 State Output Disable Time	2.0			35	150		190		225	ns
		4.5			16	30		38		45	
		6.0			13	26		32		38	
f_{MAX}	Maximum Clock Frequency	2.0		6	16		4.8		4		MHz
		4.5		30	66		24		20		
		6.0		35	80		28		24		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width	2.0			17	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
$t_{W(L)}$	Minimum Pulse Width	2.0			28	75		95		110	ns
		4.5			6	15		19		22	
		6.0			6	13		16		19	
t_s	Minimum Set-up Time (SI)	2.0			30	75		95		110	ns
		4.5			7	15		19		22	
		6.0			5	13		16		19	
t_s	Minimum Set-up Time (ST)	2.0			45	100		125		145	ns
		4.5			10	20		25		29	
		6.0			8	17		21		25	
t_h	Minimum Hold Time (SI, ST)	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				140						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per FLIP/FLOP)

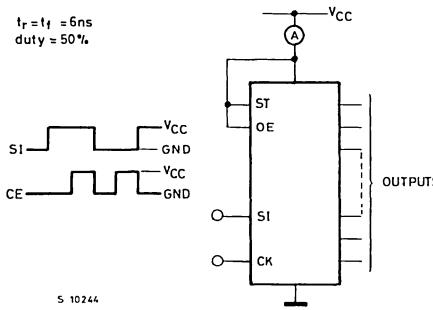
SWITCHING CHARACTERISTICS TEST WAVEFORM







TEST WAVEFORM I_{CC} (Opr.)



C_{PD} CALCULATION

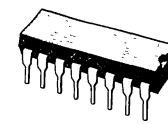
C_{PD} is to be calculated with the following formula by using the measured value of I_{CC} (Opr.) in the test circuit opposite.

$$C_{PD} = \frac{I_{CC}\,(Opr)}{f_{IN} \times V_{CC}}$$

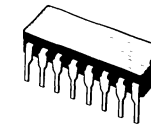
In determining the typical value of C_{PD}, a relatively high frequency of 1 MHz was applied to f_{IN}, in order to eliminate any error caused by the quiescent supply current.

QUAD BILATERAL SWITCH

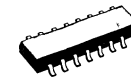
- HIGH SPEED
  t_{PD} = 13 ns (TYP.) AT V_{CC} = 5V
- LOW "ON" RESISTANCE:
  120 Ω TYP. (V_{CC} - V_{EE} = 2 V)
  50 Ω TYP. (V_{CC} - V_{EE} = 4.5 V)
  35 Ω TYP. (V_{CC} - V_{EE} = 9 V)
- WIDE ANALOG INPUT VOLTAGE RANGE: ±6V
- LOW CROSSTALK BETWEEN SWITCHES
- FAST SWITCHING
- SINE WAVE DISTORTION
  0.020 (TYP.) AT V_{CC} - V_{EE} = 9V
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28 % V_{CC} (MIN.)
- LOW POWER DISSIPATION
  I_{CC} = 1μA (MAX.) AT V_{CC} 5V
- PIN AND FUNCTION COMPATIBLE
  WITH 4316B



B1R
(Plastic Package)



F1R
(Ceramic Package)



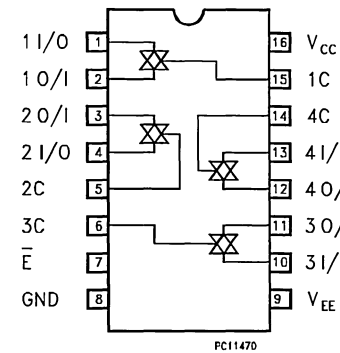
M1R
(Micro Package)

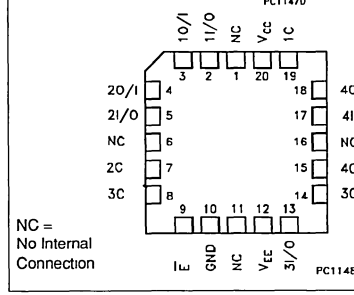
C1R
(Chip Carrier)

ORDER CODES :

M54HC4316F1R M74HC4316M1R
M74HC4316B1R M74HC4316C1R

PIN CONNECTIONS (top view)



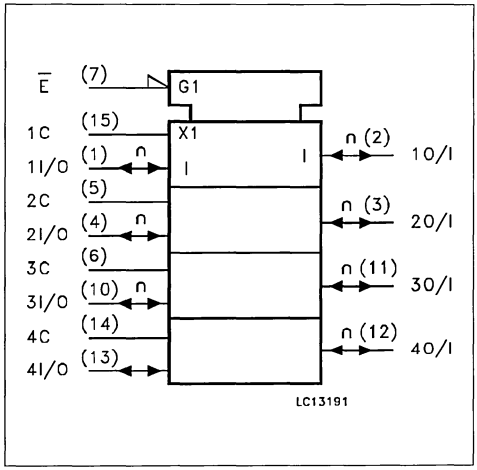


NC =
No Internal
Connection

DESCRIPTION

The M54/74HC4316 is a high speed CMOS QUAD BILATERAL SWITCH fabricated in silicon gate C^2MOS technology. It has high speed performance combined with true CMOS low power consumption. HC4316 has four independent analogue switches. Each switch has two input/output terminals (nI/O, nO/I and an active high select input (nC).
When the enable input is high all four analog switches are off. The supply voltage for the digital signals applied to V_{CC} and GND must be within the range 0 to 6 V. The voltage swing on the analogue Input/Outputs can be between VCC (Positive Limit) and V_{EE} (Negative Limit). The voltage between V_{CC} and V_{EE} must not exceed 12 V.
All input are equipped with protection circuits against static discharge and transient excess voltage.

IEC LOGIC SYMBOL



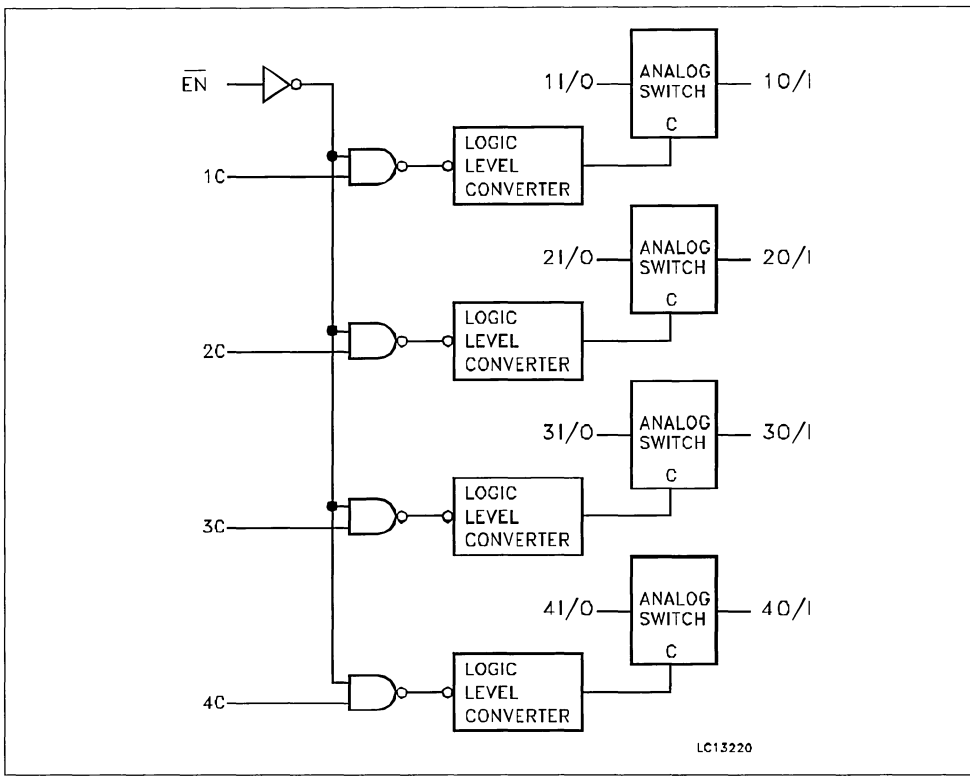
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1 to 4 I/O	Independent Inputs/Outputs
2, 3, 11, 12	1 to 4 O/I	Independent Outputs/Inputs
7	$\overline{E}$	Enable Inputs (Active LOW)
15, 5, 6, 14	1C to 4C	Enable Inputs (Active HIGH)
9	V_{EE}	Negative Supply Voltage
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

TRUTH TABLE

		SWITCH FUNCTION
$\overline{ENABLE}$	CONTROL	
L	H	ON
L	L	OFF
H	X	OFF

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_{CC} - V_{EE}	Supply Voltage	-0.5 to +13	V
V_I	COntrol Input Voltage	-0.5 to V_{CC} + 0.5	V
$V_{I/O}$	Switch I/O Voltage	V_{EE} -0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C· 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_{EE}	Supply Voltage		-6 to 0	V
V_{CC} - V_{EE}	Supply Voltage		2 to 12	V
V_I	Input Voltage		0 to V_{CC}	V
$V_{I/O}$	Switch I/O Voltage		V_{EE} to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	V_{EE} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IHC}	High Level Control Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{ILC}	Low Level Control Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
R_{ON}	ON Resistance	4.5	GND	$V_{IN} = V_{IHC}$ $V_{I/O} = V_{CC}$ to V_{EE} $I_{I/O}$ = 0.1 mA		70	170		200			Ω
		4.5	-4.5			50	85		105			
		6.0	-6.0			30	70		85			
		2.0	GND	$V_{IN} = V_{IHC}$ $V_{I/O} = V_{CC}$ or V_{EE} $I_{I/O}$ = 0.1 mA		120	180		215			
		4.5	GND			50	80		100			
		4.5	-4.5			35	60		75			
		6.0	-6.0			20	40		60			
ΔR_{ON}	Difference of ON Resistance Between Switches	4.5	GND	$V_{IN} = V_{IHC}$ or V_{ILC} $V_{I/O} = V_{CC}$ to V_{EE} $I_{I/O}$ = 0.1 mA		10	15		20			Ω
		4.5	-4.5			5	10		15			
		6.0	-6.0			5	10		15			
I_{OFF}	Input/Output Leakage Current (SWITCH OFF)	6.0	GND	$V_{OS} = V_{CC}$ or GND $V_{IS} = V_{CC}$ or GND $V_{IN} = V_{IHC}$ or V_{ILC}			±0.06		±0.6		±2	µA
		6.0	-6.0				±0.1		±1		±2	
I_{IZ}	Switch Input Leakage Current (SWITCH ON, OUTPUT OPEN)	6.0	GND	$V_{OS} = V_{CC}$ or GND $V_{IN} = V_{ILC}$ or V_{IHC}			±0.06		±0.6		±2	µA
		6.0	-6.0				±0.1		±1		±2	
I_{IN}	Control Input Current	6.0	$V_I = V_{CC}$ or GND			10^{-5}	±0.1		±1		±1	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$\varnothing_{I/O}$	Phase Difference Between Input and Output	2.0	GND			12	30		40			ns
		4.5	GND			3	6		8			
		6.0	GND			3	5		7			
		4.5	-4.5			2	4		5			
		6.0	-6.0			2	4		5			
t_{PZL} t_{PZH}	Output Enable Time ($\overline{E}$, C-OUT)	2.0	GND	R_L = 1KΩ		56	115		145			ns
		4.5	GND			14	23		29			
		6.0	GND			12	20		25			
		4.5	-4.5			13	21		26			
		6.0	-6.0			11	18		23			
t_{PLZ} t_{PHZ}	Output Disable Time ($\overline{E}$, C-OUT)	2.0	GND	R_L = 1KΩ		112	205		255			ns
		4.5	GND			28	41		51			
		6.0	GND			24	35		43			
		4.5	-4.5			24	34		43			
		6.0	-6.0			21	29		36			
	Maximum Control Input Frequency	2.0	GND	R_L = 1KΩ C_L = 15 pF V_{OUT} = 1/2 V_{CC}		2						MHz
		4.5	GND			9						
		6.0	GND			11						
C_{IN}	Input Capacitance					5	10		10		10	pF
$C_{I/O}$	Switch Terminal Capacitance	4.5	-4.5			5						pF
C_{IOS}	Feed Through Capacitance	4.5	-4.5			1						pF
C_{PD} (*)	Power Dissipation Capacitance	5.0	GND			16						pF

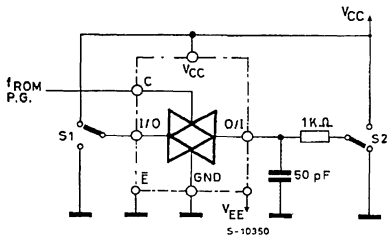
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit) Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

ANALOG SWITCH CHARACTERISTICS (GND = 0 V T_A = 25 °C)

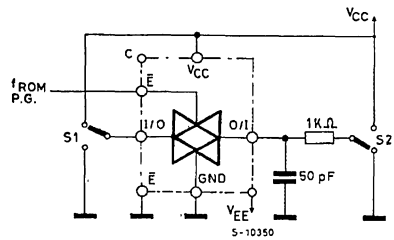
Symbol	Parameter	Test Conditions				Value	Unit
		V_{CC} (V)	V_{EE} (V)	VIN (Vp-p)		Typ.	
	Sine Wave Distortion (THD)	2.25	2.25	4	f_{IN} = 1 KHz R_L = 10 Ω C_L = 50 pF	0.025	%
		4.5	4.5	8		0.020	
		6.0	6.0	11		0.018	
f_{MAX}	Frequency Response (Switch ON)	2.25	2.25	Adjust f_{IN} voltage to Obtain 0 dBm at V_{OS}. Increase f_{IN} Frequency until dB Meter reads -3dB R_L = 50 Ω C_L = 10 pF f_{IN} = 1 KHz sine wave		28	MHz
		4.5	4.5			42	
		6.0	6.0			43	
	Feedthrough Attenuation (Switch OFF)	2.25	2.25	V_{IN} is centered at V_{CC}/2. Adjust input for 0 dBm R_L = 600 Ω C_L = 50 pF f_{IN} = 1 MHz sine wave		-50	dB
		4.5	4.5			-50	
		6.0	6.0			-50	
	Crosstalk (Control Input to Signal Output)	2.25	2.25	R_L = 600 Ω C_L = 50 pF f_{IN} = 1 KHz square wave (t_r = t_f = 6ns)			mV
		4.5	4.5			5	
		6.0	6.0				
	Crosstalk (Between Any Switches)	2.25	2.25	Adjust V_{IN} to Obtain 0 dBm at input R_L = 600 Ω C_L = 50 pF f_{IN} = 1 MHz sine wave		-50	dB
		4.5	4.5			-50	
		6.0	6.0			-50	

SWITCHING CHARACTERISTICS TEST CIRCUIT

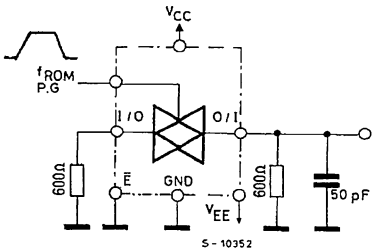
CONTROL
t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}.



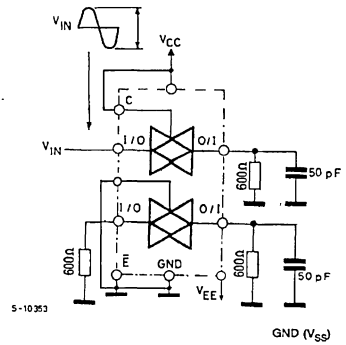
ENABLE
t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}.



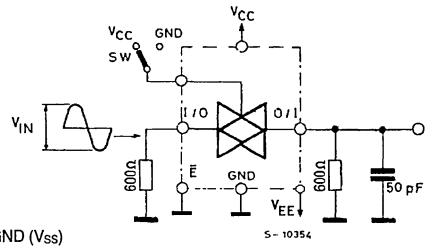
CROSSTALK (control to output)



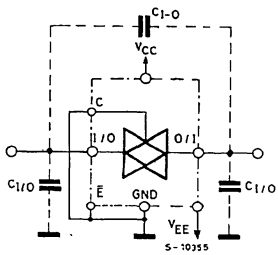
CROSSTALK BETWEEN ANY TWO SWITCHES



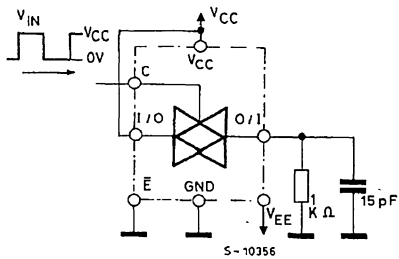
BANDWIDTH AND FEEDTHROUGH ATTENUATION



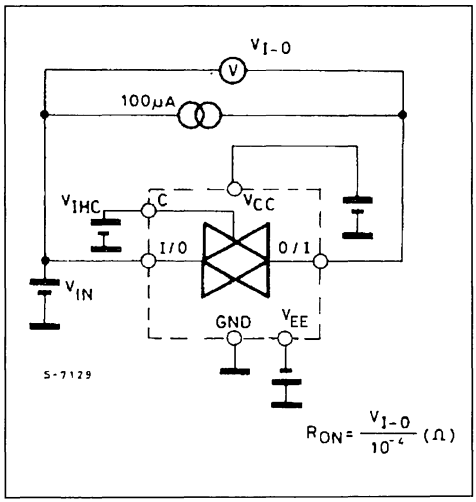
C_{I-O} $C_{I/O}$



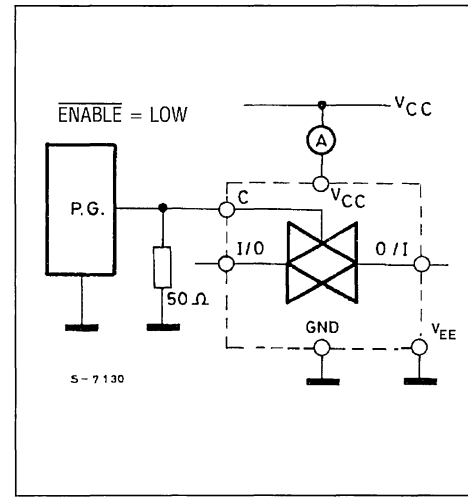
MAXIMUM CONTROL FREQUENCY



CHANNEL RESISTANCE (R_{ON})



I_{CC} (Opr.)

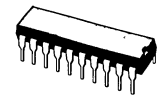


SGS-THOMSON MICROELECTRONICS

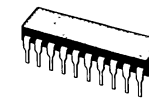
M54HC4351/52/53
M74HC4351/52/53

ANALOG MULTIPLEXER/DEMULTIPLEXER WITH ADDRESS LATCH: SINGLE 8 CHANNEL, DUAL 4 CHANNEL, TRIPLE 2 CHANNEL

- LOGIC LEVEL TRANSLATION TO ENABLE 5V LOGIC SIGNAL TO COMMUNICATE WITH ±5V ANALOG SIGNAL
- WIDE OPERATING VOLTAGE RANGE (V_{CC} - V_{EE}) 2V TO 12V
- LOW "ON" RESISTANCE: 70Ω TYP. (V_{CC} - V_{EE} = 4.5 V) 50Ω TYP. (V_{CC} - V_{EE} = 9 V)
- WIDE ANALOG INPUT VOLTAGE RANGE: ±6V
- FAST SWITCHING
- LOW CROSSTALK BETWEEN SWITCHES
- HIGH ON/OFF OUTPUT VOLTAGE RATIO
- LOW SINE WAVE DISTORTION: 0.02% (TYP.) AT V_{CC} - V_{EE} = 9 V
- HIGH NOISE IMMUNITY V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- LOW POWER DISSIPATION I_{CC} = 4 μA (MAX) AT T_A = 25 °C



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HCXXXXF1R M74HCXXXXM1R
M74HCXXXXB1R M74HCXXXXC1R

DESCRIPTION

These devices are analog multiplexer demultiplexers in high speed silicon gate C^2MOS technology. These analog switches are bidirectional and digitally controlled. A built-in level shifting is included to allow them a control input range of up to ± 6V (peak) for an analog signal with digital control signal of 0 to 6V.

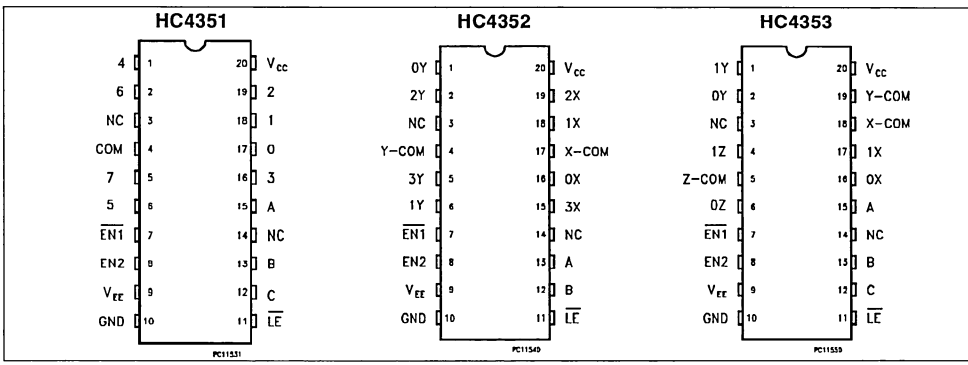
V_{EE} supply pin is provided for analog input signals. They have two enable inputs to enable all the switches when high (EN2) or low ($\overline{EN1}$). For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND.

The HC4351 is a single 8 channel multiplexer demultiplexer having three binary control inputs A, B and C to select 1 of 8 to be turned on, and connected to the output.

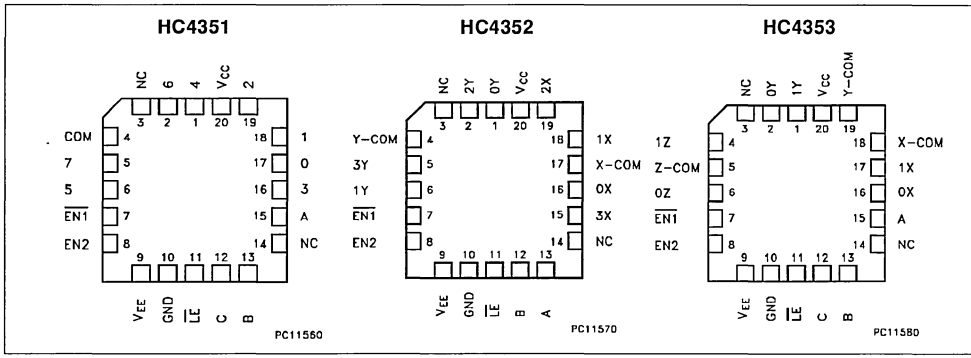
The HC4352 has a pair of four channel multiplexer demultiplexer having two control inputs A and B that select one of four channel of the two sections.

The HC4353 is a triple two channel multiplexer demultiplexer having three separate digital control inputs A, B and C to select independently one of a pair of channles.

PIN CONNECTION (top view)



CHIP CARRIER



PIN DESCRIPTION (HC4351)

PIN No	SYMBOL	NAME AND FUNCTION
4	COM	Common
3, 14	NC	Not Connected
7	$\overline{EN1}$	Enable Input (Active LOW)
8	EN2	Enable Input (Active HIGH)
9	V_{EE}	Negative Supply Voltage
11	$\overline{LE}$	Latch Enable Input (Active LOW)
15, 13, 12	A, B, C	Select Inputs
17, 18, 19, 16, 1, 6, 2, 5	0 to 7	Independent Input/Outputs
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

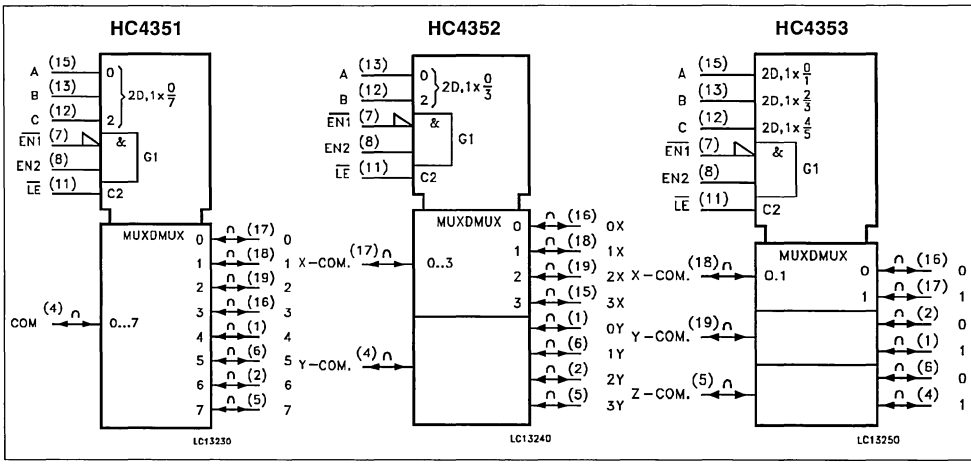
PIN DESCRIPTION (HC4352)

PIN No	SYMBOL	NAME AND FUNCTION
1, 6, 2, 5	0Y to 3Y	Independent Input/Outputs
3, 14	NC	Not Connected
7	$\overline{EN1}$	Enable Input (Active LOW)
8	EN2	Enable Input (Active HIGH)
9	V_{EE}	Negative Supply Voltage
11	$\overline{LE}$	Latch Enable Input (Active LOW)
13, 12	A, B	Select Inputs
16, 18, 19, 15	0X to 3X	Independent Input/Outputs
17, 4	X COM Y COM	Common Output/Inputs
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

PIN DESCRIPTION (HC4353)

PIN No	SYMBOL	NAME AND FUNCTION
1, 2	0Y 1Y	Independent Input/Outputs
5	Z COM	Common Output/Inputs
6, 4	0Z, 1Z	Independent Input/Outputs
3, 14	NC	Not Connected
7	$\overline{EN1}$	Enable Input (Active LOW)
8	EN2	Enable Input (Active HIGH)
9	V_{EE}	Negative Supply Voltage
11	$\overline{LE}$	Latch Enable Input (Active LOW)
15, 13, 12	A, B, C	Select Inputs
16, 17	0X, 1X	Independent Input/Outputs
18	X COM	Common Output/Inputs
19	Y COM	Common Output/Inputs
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS



TRUTH TABLE

CONTROL INPUTS					"ON" CHANNEL ($\overline{LE}$ = H) **		
$\overline{EN1}$	EN2	C *	B	A	HC4351	HC4352	HC4353
L	H	L	L	L	0	0X, 0Y	0X, 0Y, 0Z
L	H	L	L	H	1	1X, 1Y	1X, 0Y, 0Z
L	H	L	H	L	2	2X, 2Y	0X, 1Y, 0Z
L	H	L	H	H	3	3X, 3Y	1X, 1Y, 0Z
L	H	H	L	L	4	- -	0X, 0Y, 1Z
L	H	H	L	H	5	- -	1X, 0Y, 1Z
L	H	H	H	L	6	- -	0X, 1Y, 1Z
L	H	H	H	H	7	- -	1X, 1Y, 1Z
H	X	X	X	X	NONE	NONE	NONE
X	L	X	X	X	NONE	NONE	NONE

X: DON'T CARE *: HC4351/3 only
** When latch Enable is low, the Channel Selection is latched and the Channel Address Latch does not change state.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage Range	-0.5 to +7	V
V_{CC} - V_{EE}	Supply Voltage Range	-0.5 to 13	V
V_{IN}	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
$V_{I/O}$	DC Switch I/O Voltage	V_{EE} - 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	± 20	mA
I_{OK}	I/O Diode Current	± 20	mA
I_{OUT}	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied

(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_{EE}	Supply Voltage		-6 to 0	V
V_{CC} - V_{EE}	Supply Voltage		2 to 12	V
V_{IN}	Input Voltage		0 to V_{CC}	V
$V_{I/O}$	DC Switch I/O Voltage		V_{EE} to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	V_{EE} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IHC}	High Level Control Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{ILC}	Low Level Control Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
R_{ON}	ON Resistance	4.5	GND	V_{IN} = V_{IHC} or V_{ILC} $V_{I/O}$ = V_{CC} to V_{EE} $I_{I/O} \leq 2$ mA		85	180		225			Ω
		4.5	-4.5			55	120		150			
		6.0	-6.0			50	100		125			
		2.0	GND	V_{IN} = V_{IHC} or V_{ILC} $V_{I/O}$ = V_{CC} or V_{EE} $I_{I/O} \leq 2$ mA		150						
		4.5	GND			70	150		190			
		4.5	-4.5			50	100		125			
		6.0	-6.0			45	80		100			
ΔR_{ON}	Difference of ON Resistance Between Switches	4.5	GND	V_{IN} = V_{IHC} or V_{ILC} $V_{I/O}$ = V_{CC} to V_{EE} $I_{I/O} \leq 2$ mA		10	30		35			Ω
		4.5	-4.5			5	12		15			
		6.0	-6.0			5	10		12			
I_{OFF}	Input/Output Leakage Current (SWITCH OFF)	6.0	-6.0	V_{OS} = V_{CC} or GND V_{IS} = GND or V_{CC} V_{IN} = V_{ILC}			±100		±1000		±	nA
I_{IZ}	Switch Input Leakage Current (SWITCH ON)	6.0	-6.0	V_{OS} = V_{CC} or GND V_{INH} = V_{IHC}			±100		±1000		±	nA
I_{IN}	Control Input Current	6.0	GND	V_{IN} = V_{CC} or GND			±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	GND	V_{IN} = V_{CC} or GND			4		40		80	µA
		6.0	-6.0				8		80		160	

AC ELECTRICAL CHARACTERISTICS for HC4351 (C_L = 50 pF, Input $t_r = t_f$ = 6 ns, GND=0V)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	V_{EE} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$\Phi_{I/O}$	Phase Difference Between Input and Output	2.0	GND			25	60		75			ns
		4.5	GND			6	12		15			
		6.0	GND			5	10		13			
		4.5	-4.5			4						
t_{PZL} t_{PZH}	Output Enable Time ($\overline{E1}$, E2 - O)	2.0	GND	R_L = 1KΩ		80	200		250		300	ns
		4.5	GND			20	40		50		60	
		6.0	GND			16	34		43		51	
		4.5	-4.5			18						
t_{PZL} t_{PZH}	Output Enable Time ($\overline{LE}$ - I/O)	2.0	GND	R_L = 1KΩ		80	225		280		340	ns
		4.5	GND			22	45		56		68	
		6.0	GND			17	38		48		57	
		4.5	-4.5			18						
t_{PZL} t_{PZH}	Output Enable Time (A, B, C - I/O)	2.0	GND	R_L = 1KΩ		75	225		280		340	ns
		4.5	GND			22	45		56		68	
		6.0	GND			16	38		48		57	
		4.5	-4.5			17						
t_{PLZ} t_{PHZ}	Output Disable Time ($\overline{E1}$, E2 - O)	2.0	GND	R_L = 1KΩ		120	275		344		415	ns
		4.5	GND			38	55		69		83	
		6.0	GND			33	47		59		71	
		4.5	-4.5			30						
t_{PLZ} t_{PHZ}	Output Disable Time ($\overline{LE}$ - I/O)	2.0	GND	R_L = 1KΩ		120	275		344		415	ns
		4.5	GND			40	55		69		83	
		6.0	GND			35	47		59		71	
		4.5	-4.5			34						
t_{PLZ} t_{PHZ}	Output Disable Time (A, B, C - I/O)	2.0	GND	R_L = 1KΩ		120	290		363		433	ns
		4.5	GND			40	58		73		87	
		6.0	GND			35	49		61		74	
		4.5	-4.5			35						
$t_{W(H)}$	Minimum Pulse Width (LE)	2.0					75		95		110	ns
		4.5					15		19		22	
		6.0					13		16		19	
t_s	Minimum Set Up Time	2.0					50		60		75	ns
		4.5					10		12		15	
		6.0					9		11		13	
t_h	Minimum Hold Time	2.0					5		5		5	ns
		4.5					5		5		5	
		6.0					5		5		5	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{IS}	Common Terminal Capacitance	5.0	-5.0			36	70		70		70	pF
C_{OS}	Switch Terminal Capacitance	5.0	-5.0			7	15		15		15	pF
C_{IOS}	Feed Through Capacitance	5.0	-5.0			0.95	2		2		2	pF
C_{PD} (*)	Power Dissipation Capacitance	5.0	GND			23						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

AC ELECTRICAL CHARACTERISTICS for HC4352 (C_L = 50 pF, Input $t_r = t_f$ = 6 ns, GND=0V)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	V_{EE} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$\Phi_{I/O}$	Phase Difference Between Input and Output	2.0	GND			25	60		75			ns
		4.5	GND			6	12		15			
		6.0	GND			5	10		13			
		4.5	-4.5			4						
t_{PZL} t_{PZH}	Output Enable Time ($\overline{E1}$, E2 - O)	2.0	GND	R_L = 1KΩ		80	200		250		300	ns
		4.5	GND			20	40		50		60	
		6.0	GND			16	34		43		51	
		4.5	-4.5			18						
t_{PZL} t_{PZH}	Output Enable Time ($\overline{LE}$ - I/O)	2.0	GND	R_L = 1KΩ		80	225		280		340	ns
		4.5	GND			22	45		56		68	
		6.0	GND			17	38		48		57	
		4.5	-4.5			18						
t_{PZL} t_{PZH}	Output Enable Time (A, B, C - I/O)	2.0	GND	R_L = 1KΩ		80	225		280		340	ns
		4.5	GND			22	45		56		68	
		6.0	GND			16	38		48		57	
		4.5	-4.5			17						
t_{PLZ} t_{PHZ}	Output Disable Time ($\overline{E1}$, E2 - O)	2.0	GND	R_L = 1KΩ		120	275		344		415	ns
		4.5	GND			38	55		69		83	
		6.0	GND			33	47		59		71	
		4.5	-4.5			36						
t_{PLZ} t_{PHZ}	Output Disable Time ($\overline{LE}$ - I/O)	2.0	GND	R_L = 1KΩ		160	275		344		415	ns
		4.5	GND			40	55		69		83	
		6.0	GND			34	47		59		71	
		4.5	-4.5			32						
t_{PLZ} t_{PHZ}	Output Disable Time (A, B, C - I/O)	2.0	GND	R_L = 1KΩ		120	275		344		415	ns
		4.5	GND			40	55		69		83	
		6.0	GND			35	47		59		71	
		4.5	-4.5			31						
$t_{W(H)}$	Minimum Pulse Width (LE)	2.0					75		95		110	ns
		4.5					15		19		22	
		6.0					13		16		19	
t_s	Minimum Set Up Time	2.0					50		60		75	ns
		4.5					10		12		15	
		6.0					9		11		13	
t_h	Minimum Hold Time	2.0					5		5		5	ns
		4.5					5		5		5	
		6.0					5		5		5	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{IS}	Common Terminal Capacitance	5.0	-5.0			19	40		40		40	pF
C_{OS}	Switch Terminal Capacitance	5.0	-5.0			7	15		15		15	pF
C_{IOS}	Feed Through Capacitance	5.0	-5.0			0.85	2		2		2	pF
C_{PD} (*)	Power Dissipation Capacitance	5.0	GND			34						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

AC ELECTRICAL CHARACTERISTICS for HC4353 (C_L = 50 pF, Input $t_r = t_f$ = 6 ns, GND=0V)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	V_{EE} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$\Phi_{I/O}$	Phase Difference Between Input and Output	2.0	GND			25	60		75			ns
		4.5	GND			6	12		15			
		6.0	GND			5	10		13			
		4.5	-4.5			4						
t_{PZL} t_{PZH}	Output Enable Time ($\overline{E1}$, E2 - O)	2.0	GND	R_L = 1KΩ		100	200		250		300	ns
		4.5	GND			22	40		50		60	
		6.0	GND			18	34		43		51	
		4.5	-4.5			19						
t_{PZL} t_{PZH}	Output Enable Time ($\overline{LE}$ - I/O)	2.0	GND	R_L = 1KΩ		110	225		280		340	ns
		4.5	GND			24	45		56		68	
		6.0	GND			20	38		48		57	
		4.5	-4.5			18						
t_{PZL} t_{PZH}	Output Enable Time (A, B, C - I/O)	2.0	GND	R_L = 1KΩ		100	225		280		340	ns
		4.5	GND			22	45		56		68	
		6.0	GND			18	38		48		57	
		4.5	-4.5			19						
t_{PLZ} t_{PHZ}	Output Disable Time ($\overline{E1}$, E2 - O)	2.0	GND	R_L = 1KΩ		130	290		363		435	ns
		4.5	GND			38	58		72		87	
		6.0	GND			32	49		61		74	
		4.5	-4.5			30						
t_{PLZ} t_{PHZ}	Output Disable Time ($\overline{LE}$ - I/O)	2.0	GND	R_L = 1KΩ		140	300		375		450	ns
		4.5	GND			41	60		75		90	
		6.0	GND			34	51		64		77	
		4.5	-4.5			37						
t_{PLZ} t_{PHZ}	Output Disable Time (A, B, C - I/O)	2.0	GND	R_L = 1KΩ		135	325		406			ns
		4.5	GND			42	65		81		100	
		6.0	GND			32	55		69		85	
		4.5	-4.5			35						
$t_{W(H)}$	Minimum Pulse Width (LE)	2.0					75		95		110	ns
		4.5					15		19		22	
		6.0					13		16		19	
t_s	Minimum Set Up Time	2.0					50		60		75	ns
		4.5					10		12		15	
		6.0					9		11		13	
t_h	Minimum Hold Time	2.0					5		5		5	ns
		4.5					5		5		5	
		6.0					5		5		5	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{IS}	Common Terminal Capacitance	5.0	-5.0			11	20		20		20	pF
C_{OS}	Switch Terminal Capacitance	5.0	-5.0			7	15		15		15	pF
C_{IOS}	Feed Through Capacitance	5.0	-5.0			0.75	2		2		2	pF
C_{PD} (*)	Power Dissipation Capacitance	5.0	GND			10						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

ANALOG SWITCH CHARACTERISTICS (GND = 0 V T_A = 25 °C)

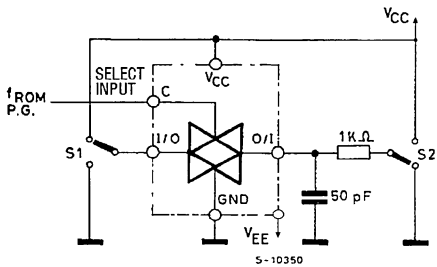
Symbol	Parameter	Test Conditions				Value	Unit
		V_{CC} (V)	V_{EE} (V)	VIN (Vp-p)		Typ.	
	Sine Wave Distortion	2.25	-2.25	4	f_{IN} = 1 KHz R_L = 10 Ω C_L = 50 pF	0.025	%
		4.5	-4.5	8		0.02	
f_{MAX}	Frequency Response (Switch ON)	4.5	-4.5	Adjust f_{IN} voltage to Obtain 0 dBm at V_{OS}. Increase f_{IN} Frequency until dB Meter Reads -3dB R_L = 50 Ω C_L = 10 pF (*)		200	MHz
	Feedthrough Attenuation (Switch OFF)	2.25	-2.25	V_{IN} is centered at (V_{CC} - V_{EE})/2. Adjust input for 0 dBm R_L = 600 Ω C_L = 50 pF f_{IN} = 1 MHz sine wave		-50	dB
		4.5	-4.5			-50	
		6	-6			-50	
	Crosstalk Control to switch	2.25	-2.25	$t_r = t_f$ = 6ns R_L = 600 Ω C_L = 50 pF f_{IN} = 1 MHz square wave		110	mV
		4.5	-4.5			225	
		6.0	-6.0			310	
	Crosstalk Between any two switches	2.25	-2.25	Adjust V_{IN} to obtain 0dBm at input R_L = 600 Ω C_L = 50 pF f_{IN} = 1 MHz sine wave		-50	dB
		4.5	-4.5			-50	
		6	-6			-50	

(*): Input COMMON Terminal, and measured at SWITCH Terminal.

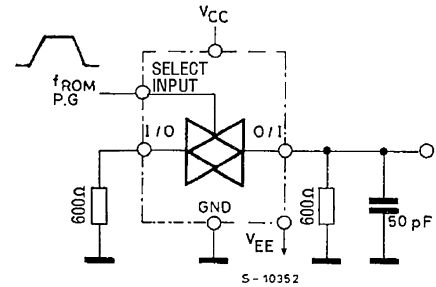
NOTE: These characteristics are determined by design of devices.

SWITCHING CHARACTERISTICS TEST CIRCUIT

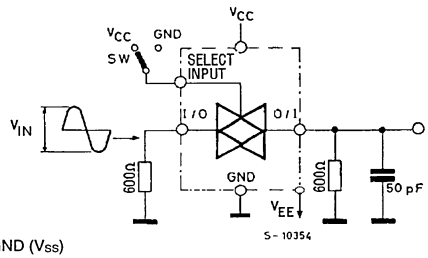
t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}.



CROSSTALK (control to output)

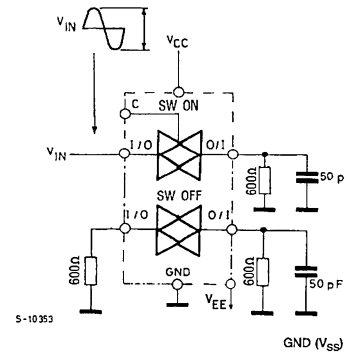


BANDWIDTH AND FEEDTHROUGH ATTENUATION



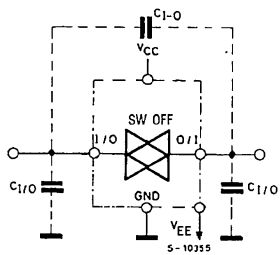
GND (V_{SS})

CROSSTALK BETWEEN ANY TWO SWITCHES



GND (V_{SS})

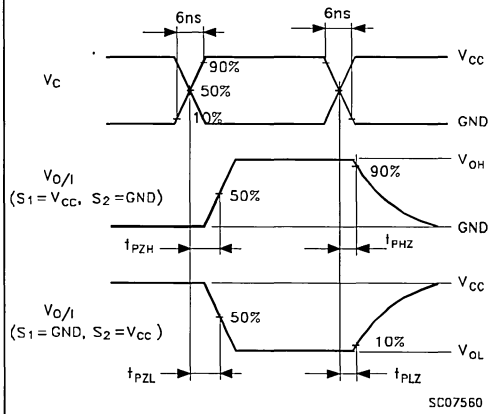
C_{I-O} $C_{I/O}$



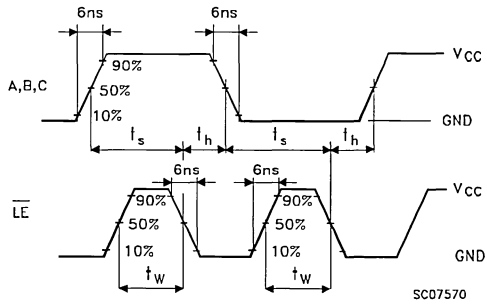
GND (V_{SS})

SWITCHING CHARACTERISTICS TEST WAVEFORM

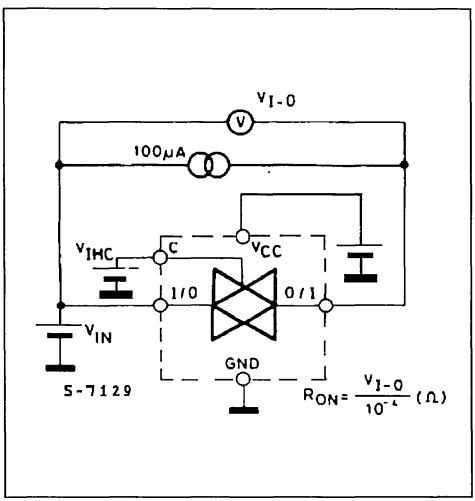
t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}.



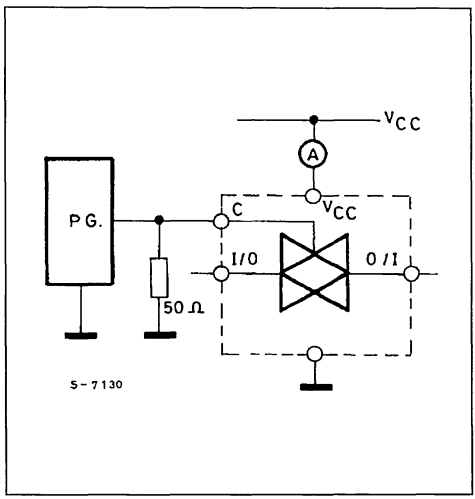
t_s, t_h, t_w



CHANNEL RESISTANCE (R_{ON})

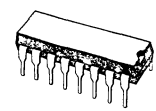


Icc (Opr.)

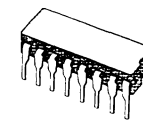


BCD TO 7 SEGMENT LATCH/DECODER DRIVER

- HIGH SPEED
  t_{PD} = 28 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- HIGH SOURGE CURRENT
  $|I_{OH}|$ = 20 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 4511B



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HC4011F1R M74HC4011M1R
M74HC4011B1R M74HC4011C1R

DESCRIPTION

The M54/74HC4511 is a high speed CMOS BCD-TO-7 SEGMENT LATCH/DECODER/DRIVER fabricated with silicon gate C^2MOS technology. It enables high speed latch and decode operation with identical pin connection and function to standard CMOS 4511B.

The segment output driver, which is CMOS fabricated in silicon gate C^2MOS technology, has large I_{OH} capability which enables common cathode Leds to be directly driven.

When lamp test ($\overline{LT}$) is taken "L", all segment outputs will go to "H", and when blanking ($\overline{BI}$) is taken "L" and $\overline{LT}$ is taken "H" all segment outputs will go to "L".

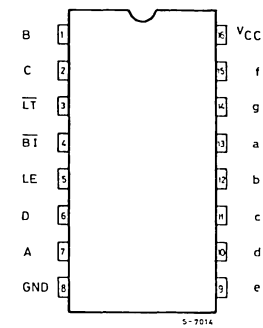
These functions operate regardless of other inputs and are used to test the display.

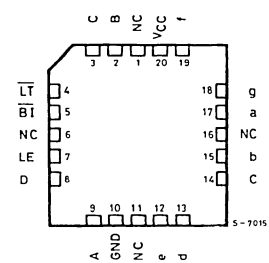
Input BI is used to pulse-modulate the brightness of the display.

When an error input code (over 10) is applied to the BCD input, all segment outputs will go "L" (turn off).

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)





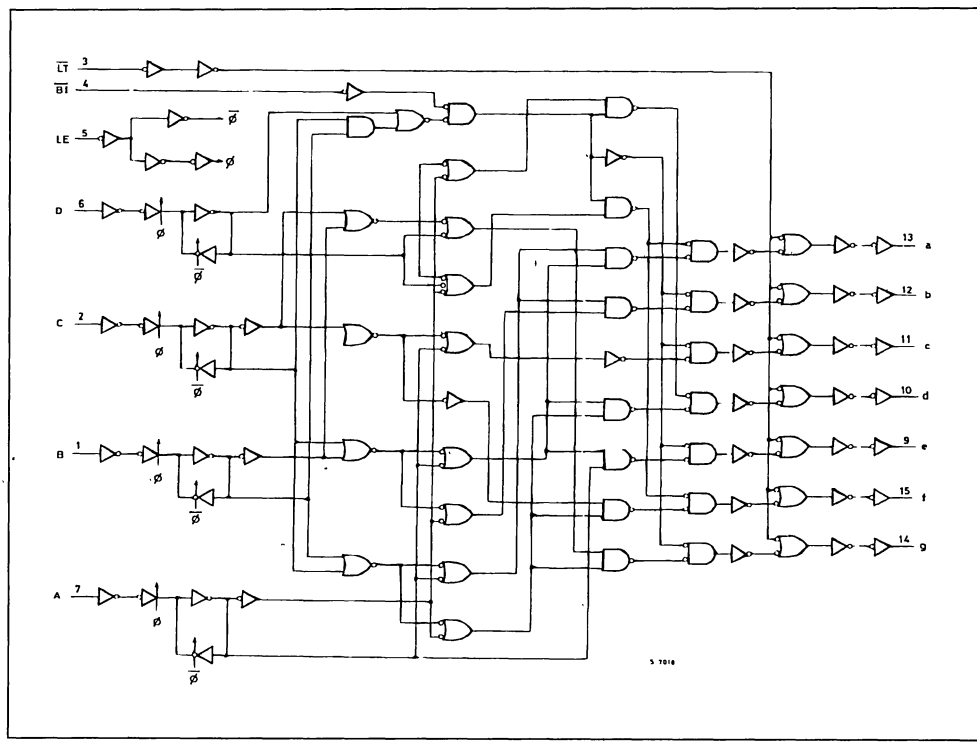
NC =
No Internal
Connection

TRUTH TABLE

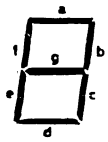
INPUTS							OUTPUTD							DISPLAY MODE
$\overline{LE}$	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	BLANK
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	L	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	X	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	X	X	L	L	L	L	L	L	L	BLANK
H	H	H	X	X	X	X	Hold the stage at the leading edge of LE							

X: Don't Care

LOGIC DIAGRAM

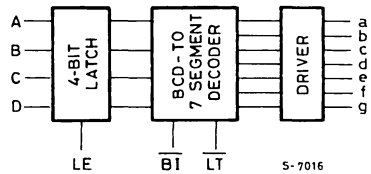


DISPLAY MODE

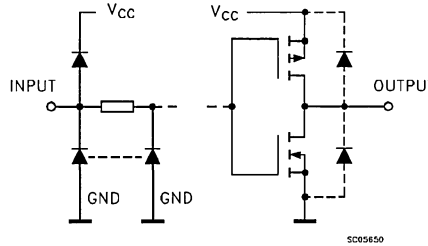


INPUT CODE										
	A	L	H	L	H	L	H	L	H	L	H
	B	L	L	H	H	L	L	H	H	L	L
	C	L	L	L	L	H	H	H	H	L	L
	D	L	L	L	L	L	L	L	L	H	H
DISPLAY		0	1	2	3	4	5	6	7	8	9

BLOCK DIAGRAM



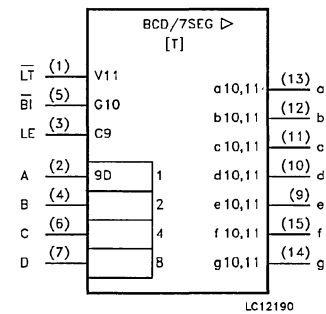
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
3	LT	Lamp Test Input (Active LOW)
4	BI	Ripple Blanking Input (Active LOW)
5	LE	Latch Enable Input
7, 1, 2, 6	A to D	BCD Address Inputs
13, 12, 11, 10, 9 , 15, 14	a to g	Segment Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	-35/25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	+150/-50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	3.2	3.8		2.9				
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.37		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.37		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

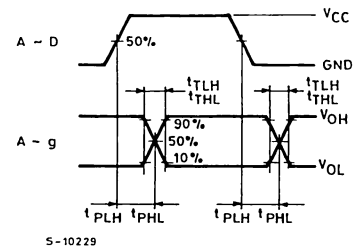
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH}	Output Transition Time	2.0			25	60		75		90	ns
		4.5			7	12		15		18	
		6.0			6	11		13		15	
t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (BCD - Seg.)	2.0			125	255		320		385	ns
		4.5			33	51		64		77	
		6.0			23	43		54		65	
t_{PLH} t_{PHL}	Propagation Delay Time (BI - Seg.)	2.0			70	175		220		265	ns
		4.5			22	35		44		53	
		6.0			17	30		37		45	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{LT}$ - Seg.)	2.0			60	120		150		180	ns
		4.5			15	24		30		36	
		6.0			12	20		26		31	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{LE}$ - Seg.)	2.0			95	240		300		360	ns
		4.5			32	48		60		72	
		6.0			23	41		51		61	
$t_{W(L)}$	Minimum Pulse Width	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_s	Minimum Set-up Time	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				95						pF

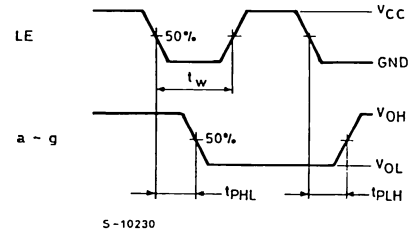
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per FLIP/FLOP)

SWITCHING CHARACTERISTICS TEST WAVEFORM

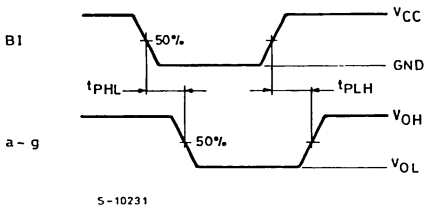
Data Segment Delay Time



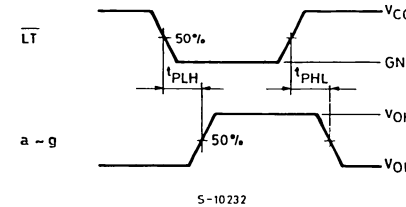
LE-Segment Delay Time



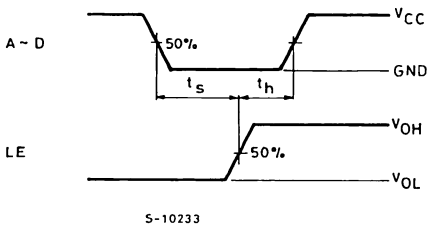
$\overline{BI}$-Segment Delay Time



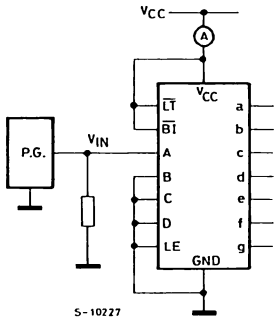
$\overline{LT}$-Segment Delay Time

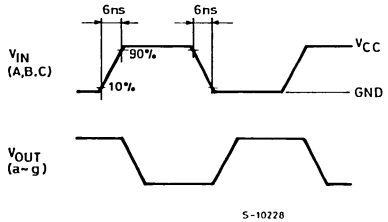


Data Set-up/Hold Time



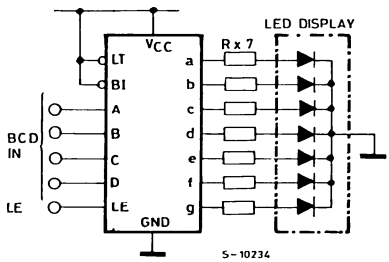
TEST CIRCUIT I_{CC} (Opr.)





APPLICATION CIRCUIT

Static Display Circuit

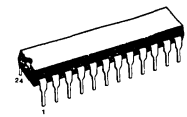


SGS-THOMSON MICROELECTRONICS

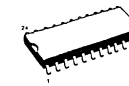
M74HC4514
M74HC4515

HC4514: 4 TO 16 LINE DECODER/LATCH
HC4515: 4 TO 16 LINE DECODER LATCH (INV.)

- HIGH SPEED
  t_{PD} = 18 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC}(OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 4514B/4515B



B1R
(Plastic Package)

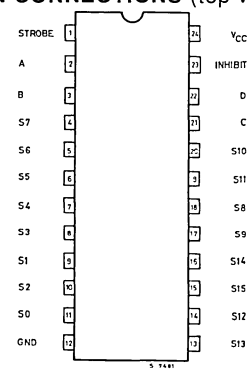


M1R
(Micro Package)

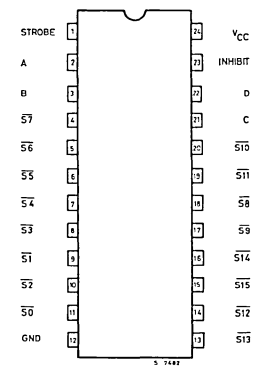
ORDER CODES :
M74HCXXXXM1R M74HCXXXXB1R

PIN CONNECTIONS (top view)

HC4514



HC4515

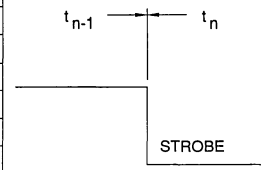


DESCRIPTION

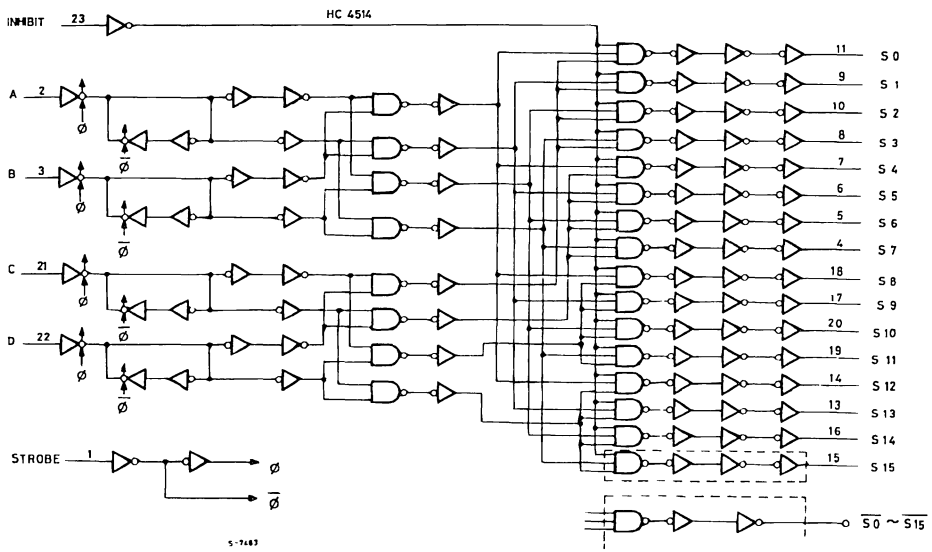
The 74HC4514 and the 74HC4515 are high speed CMOS 4-LINE TO 16-LINE DECODERS WITH LATCHED INPUTS fabricated in silicon gate C^2MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption.

A binary code stored in the four input latches (A to D) provides a high level (HC4514) or a low level (HC4515) at the selected one of sixteen outputs excluding the other fifteen outputs, when the inhibit input (INHIBIT) is held low. When the inhibit input is held high, all outputs are kept low level (HC4514) or high level (HC4515), while the latch function is available. The data applied to the data inputs are transfered to the Q outputs of latches when the strobe input is held high. When the strobe input is taken low, the information data applied to the data input at a time is retained at the output of the latches. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

INPUTS					STROBE	SELECT OUTPUT HC4514 - 'H' (HC4515 - 'L')
INHIBIT	A	B	C	D		
L	L	L	L	L	STROBE = 'H' Refer to truth table STROBE = 'L' Data at the negative going transition of strobe shall be provided on the each output while strobe is held low. 	S0 ($\overline{S0}$)
L	H	L	L	L		S1 ($\overline{S1}$)
L	L	H	L	L		S2 ($\overline{S2}$)
L	H	H	L	L		S3 ($\overline{S3}$)
L	L	L	H	L		S4 ($\overline{S4}$)
L	H	L	H	L		S5 ($\overline{S5}$)
L	L	H	H	L		S6 ($\overline{S6}$)
L	H	H	H	L		S7 ($\overline{S7}$)
L	L	L	L	H		S8 ($\overline{S8}$)
L	H	L	L	H		S9 ($\overline{S9}$)
L	L	H	L	H		S10 ($\overline{S10}$)
L	H	H	L	H		S11 ($\overline{S11}$)
L	L	L	H	H		S12 ($\overline{S12}$)
L	H	L	H	H		S13 ($\overline{S13}$)
L	L	H	H	H		S14 ($\overline{S14}$)
L	H	H	H	H		S15 ($\overline{S15}$)
H	X	X	X	X		HC4514 - ALL OUTPUTS 'L' (HC4515 - ALL OUTPUTS 'H')

LOGIC DIAGRAM (HC4514)



FOR HC4515 DEVICE LOGIC DIAGRAM SHOWN AT THE BOTTOM SHALL TAKE THE PLACE OF OUTPUT CIRCUITS.

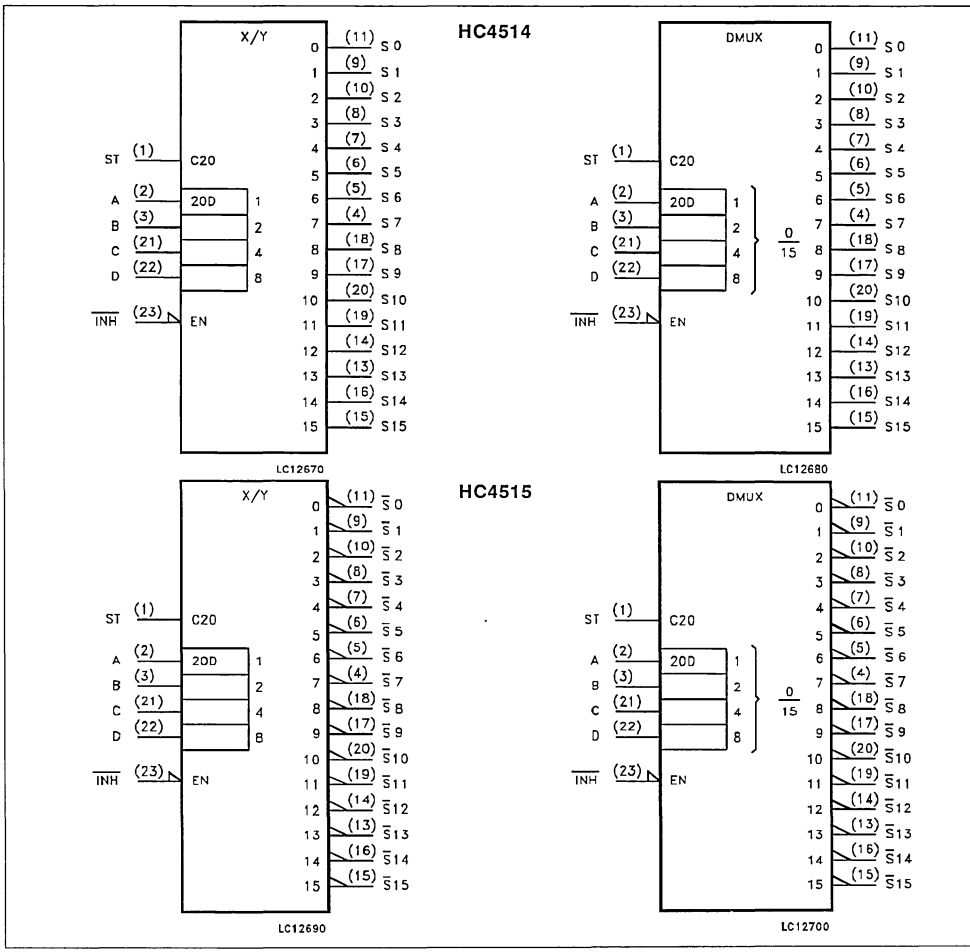
PIN DESCRIPTION (HC4514)

PIN No	SYMBOL	NAME AND FUNCTION
1	STROBE	Strobe Input
2, 3, 21, 22	A to D	Address Inputs
11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19, 14, 13, 16, 15	S0 to S15	Multiplexer Outputs (Active HIGH)
23	INHIBIT	Enable Input
12	GND	Ground (0V)
24	V_{CC}	Positive Supply Voltage

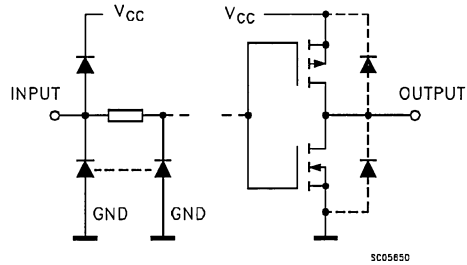
PIN DESCRIPTION (HC4515)

PIN No	SYMBOL	NAME AND FUNCTION
1	STROBE	Strobe Input
2, 3, 21, 22	A to D	Address Inputs
11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19, 14, 13, 16, 15	$\overline{S0}$ to $\overline{S15}$	Multiplexer Outputs (Active LOW)
23	INHIBIT	Enable Input
12	GND	Ground (0V)
24	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied

(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

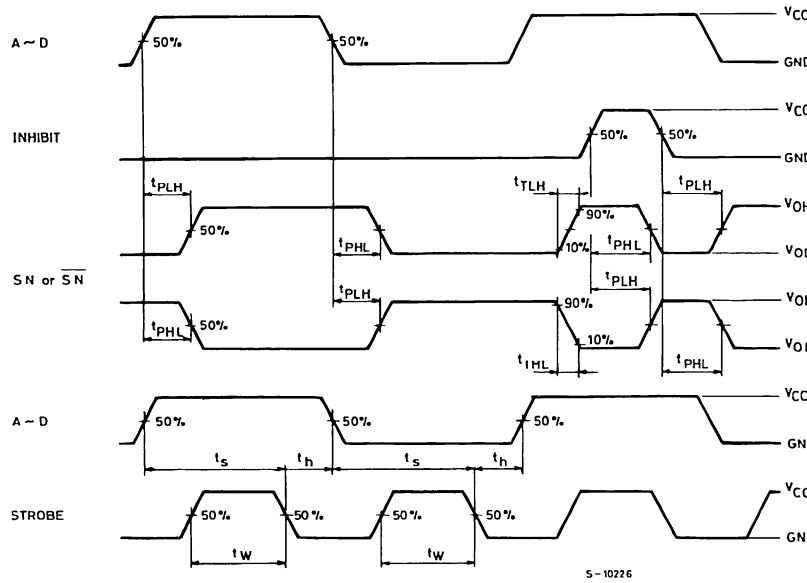
Symbol	Parameter	Test Conditions			Value					Unit
		V_{CC} (V)			T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		V
		4.5			3.15			3.15		
		6.0			4.2			4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5	V
		4.5					1.35		1.35	
		6.0					1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		V
		4.5			4.4	4.5		4.4		
		6.0			5.9	6.0		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1	V
		4.5				0.0	0.1		0.1	
		6.0				0.0	0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.5		±5.0	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

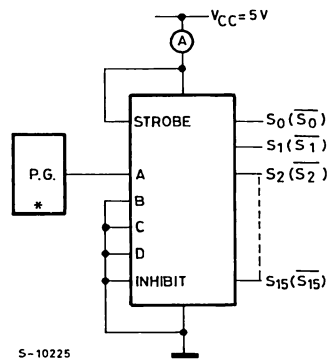
Symbol	Parameter	Test Conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
t_{PLH} t_{PHL}	Propagation Delay Time (DATA - Sn, $\overline{Sn}$)	2.0			65	175		220	ns
		4.5			22	35		44	
		6.0			19	30		37	
t_{PHL} t_{PLH}	Propagation Delay Time (STROBE - Sn, $\overline{Sn}$)	2.0			75	175		220	ns
		4.5			24	35		44	
		6.0			20	30		37	
t_{PHL} t_{PLH}	Propagation Delay Time (INHIBIT - Sn, $\overline{Sn}$)	2.0			60	175		220	ns
		4.5			20	35		44	
		6.0			17	30		37	
$t_{W(L)}$	Minimum Pulse Width (STROBE)	2.0			14	75		95	ns
		4.5			6	15		19	
		6.0			6	13		16	
t_s	Minimum Set-up Time (DATA)	2.0			10	50		65	ns
		4.5			2	10		13	
		6.0			2	9		11	
t_h	Minimum Hold Time (DATA)	2.0				5		5	ns
		4.5				5		5	
		6.0				5		5	
C_{IN}	Input Capacitance				5	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				61				pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



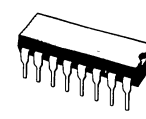
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SGS-THOMSON MICROELECTRONICS

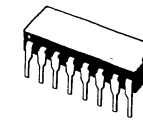
M54/M74HC4518
M54/M74HC4520

HC4518 DUAL DECADE COUNTER
HC4520 DUAL 4 BIT BINARY COUNTER

- HIGH SPEED
  f_{MAX} = 55 MHz (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 4520B/4518B



B1R
(Plastic Package)



F1R
(Ceramic Package)

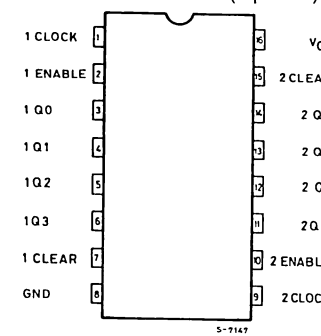
M1R
(Micro Package)

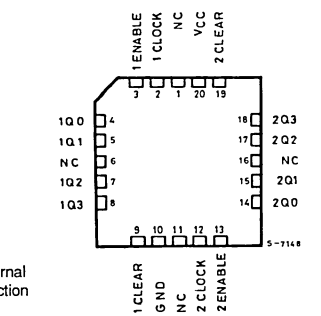
C1R
(Chip Carrier)

ORDER CODES :

M54HCXXXXF1R M74HCXXXXM1R
M74HCXXXXB1R M74HCXXXXC1R

PIN CONNECTIONS (top view)





NC =
No Internal
Connection

DESCRIPTION

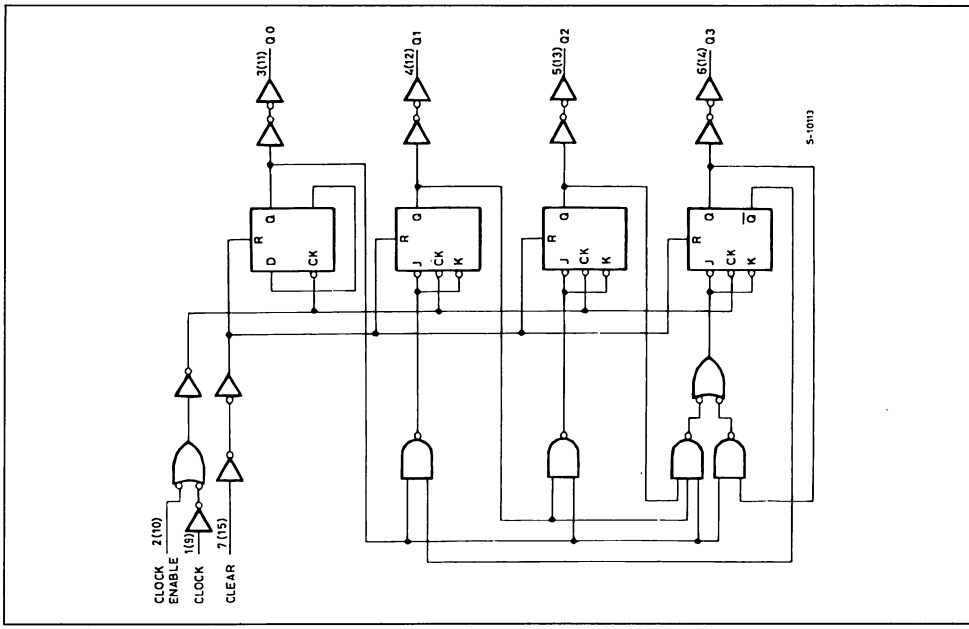
The M54/74HC4518/4520 are high speed CMOS DUAL 4 BIT BINARY COUNTERS fabricated in silicon gate C^2MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption.

They consists of two identical internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable Clock and ENABLE inputs for incrementing on either the positive-going or negative-going transition.

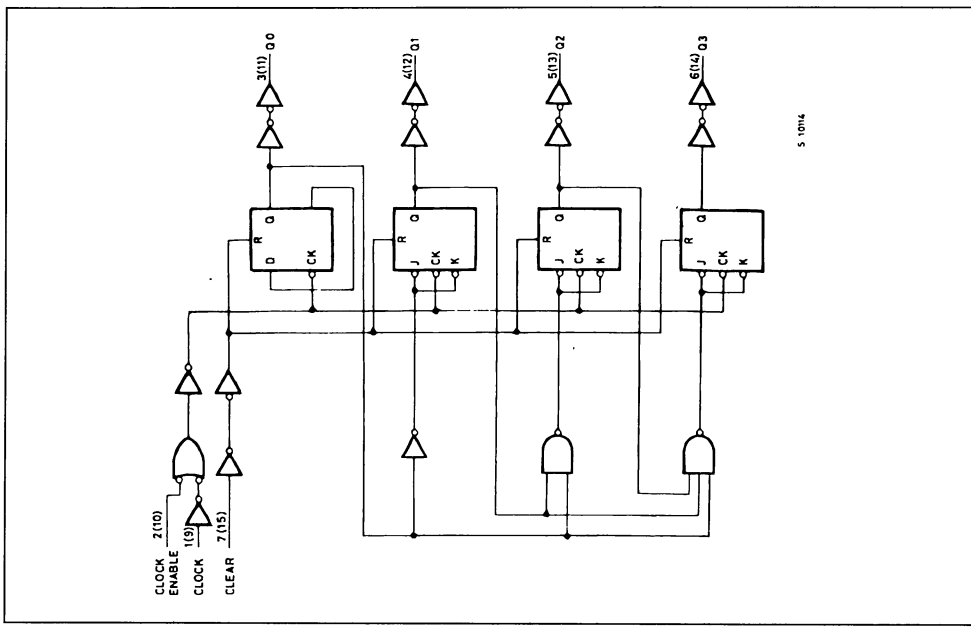
For single-unit operation the ENABLE input is maintained "high" and the counter advances on each positive-going transition of the CLOCK. The counters are cleared by high levels on their clear lines. The counter can be cascaded in the ripple mode by connecting Q4 to the enable input of the subsequent counter while the clock input of the latter is held permanently low.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

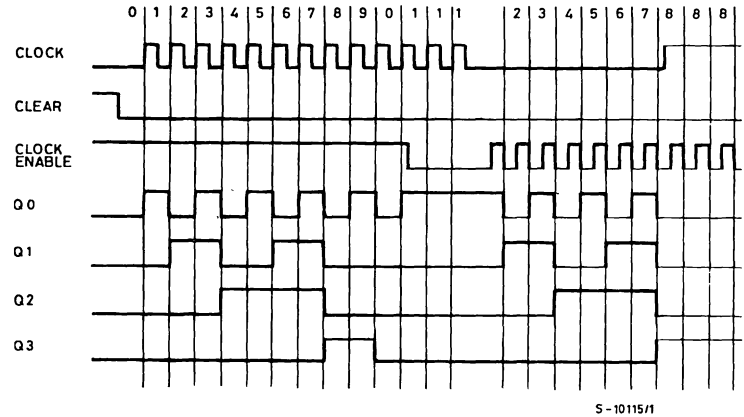
LOGIC DIAGRAM (1/2 HC4518)



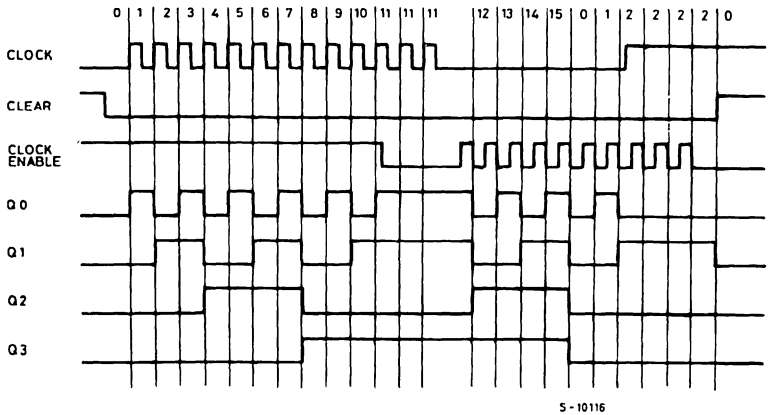
LOGIC DIAGRAM (1/2 HC4520)



TIMING CHART (HC4518)



TIMING CHART (HC4520)



TRUTH TABLE

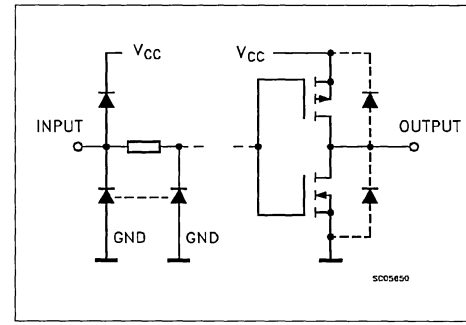
INPUTS			FUNCTION
CLOCK	ENABLE	CLEAR	
⎍	H	L	INCREMENT COUNTER
L	⎏	L	INCREMENT COUNTER
⎏	X	L	NO CHANGE
X	⎍	L	NO CHANGE
⎍	L	L	NO CHANGE
H	⎏	L	NO CHANGE
X	X	H	Q0 THRU Q3 = L

X: Don't Care Z: High Impedance

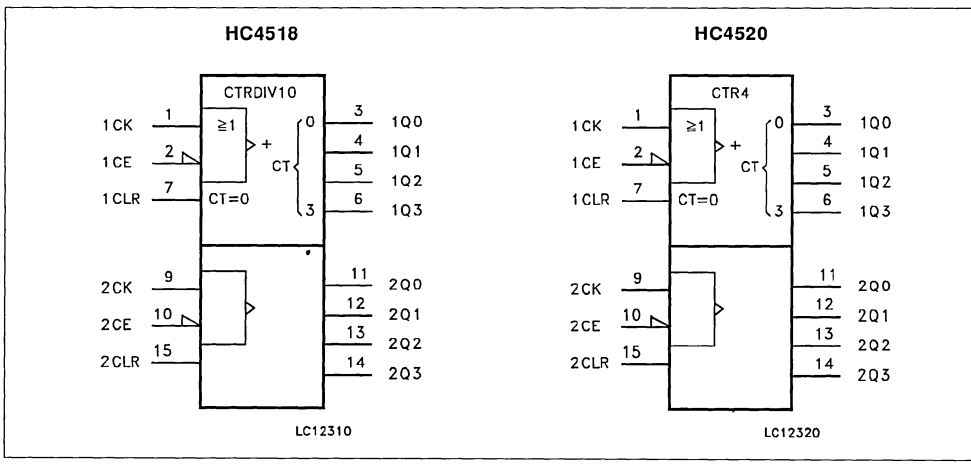
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 9	1CLOCK, 2CLOCK	Clock Inputs (LOW to HIGH, Edge-triggered)
2, 10	1ENABLE, 2ENABLE	Clock Enable Inputs
3, 4, 5, 6	1Q0 to 1Q3	Data Outputs
7, 15	1CLEAR, 2CLEAR	Asynchronous Reset Inputs (Active LOW)
11, 12, 13, 14	2Q0 to 2Q3	Data Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

INPUT AND OUTPUT EQUIVALENT CIRCUIT



IEC LOGIC SYMBOLS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

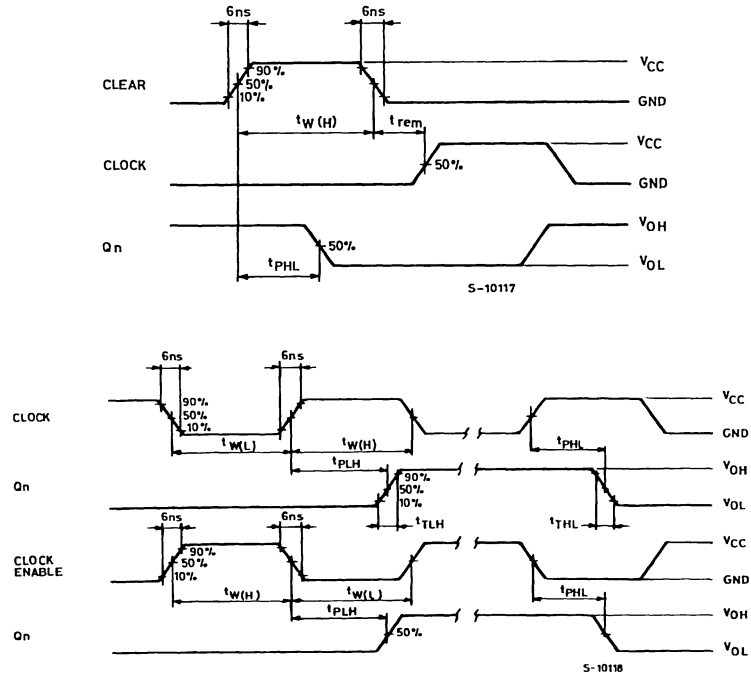
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.37		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.37		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

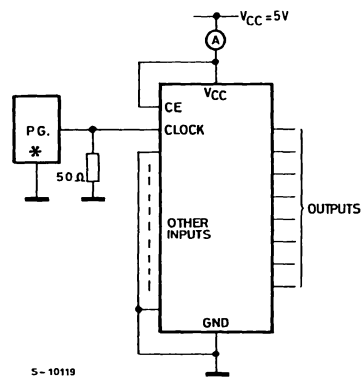
Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CK, CE - Qn)	2.0			72	160		200		240	ns
		4.5			22	32		40		48	
		6.0			18	27		34		41	
t_{PHL}	Propagation Delay Time (CLR - Qn)	2.0			65	150		190		225	ns
		4.5			20	30		38		45	
		6.0			16	26		33		38	
f_{MAX}	Maximum Clock Frequency	2.0		6	23		4.8		4		MHz
		4.5		30	51		24		20		
		6.0		35	60		28		24		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CK, CE)	2.0			25	75		95			ns
		4.5			6	15		19			
		6.0			5	13		16			
$t_{W(L)}$	Minimum Pulse Width (CLR)	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	
t_{REM}	Minimum Removal Time (CLR)	2.0			21	50		60		75	ns
		4.5			3	10		12		15	
		6.0			3	9		11		13	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance		for HC4518 for HC4520		38 32						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per COUNTER)

SWITCHING CHARACTERISTICS TEST WAVEFORMS



TEST CIRCUIT Icc (Opr.)



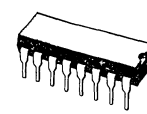
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TESTS.

SGS-THOMSON MICROELECTRONICS

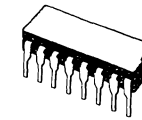
M54HC4538
M74HC4538

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

- HIGH SPEED
  t_{PD} = 25 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  STANDBY STATE I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
  ACTIVE STATE I_{CC} = 200 µA (TYP.) AT V_{CC} = 5 V
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OUTPUT PULSE WIDTH RANGE
  t_{WOUT} = 120 ns ~ 60 s OVER AT V_{CC} = 4.5 V
- OUTPUT PULSE WIDTH INDEPENDENT FROM TRIGGER INPUT PULSE WIDTH
- PIN AND FUNCTION COMPATIBLE WITH 4538B



B1R
(Plastic Package)



F1R
(Ceramic Package)

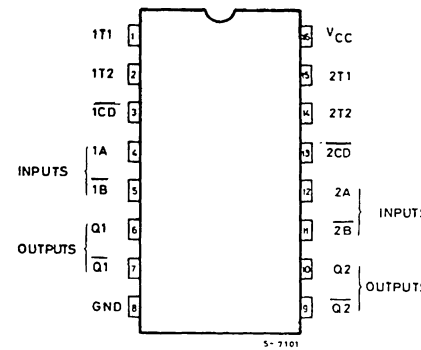
M1R
(Micro Package)

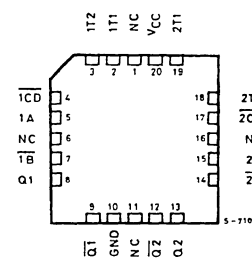
C1R
(Chip Carrier)

ORDER CODES :

M54HC4538F1R M74HC4538M1R
M74HC4538B1R M74HC4538C1R

PIN CONNECTIONS (top view)





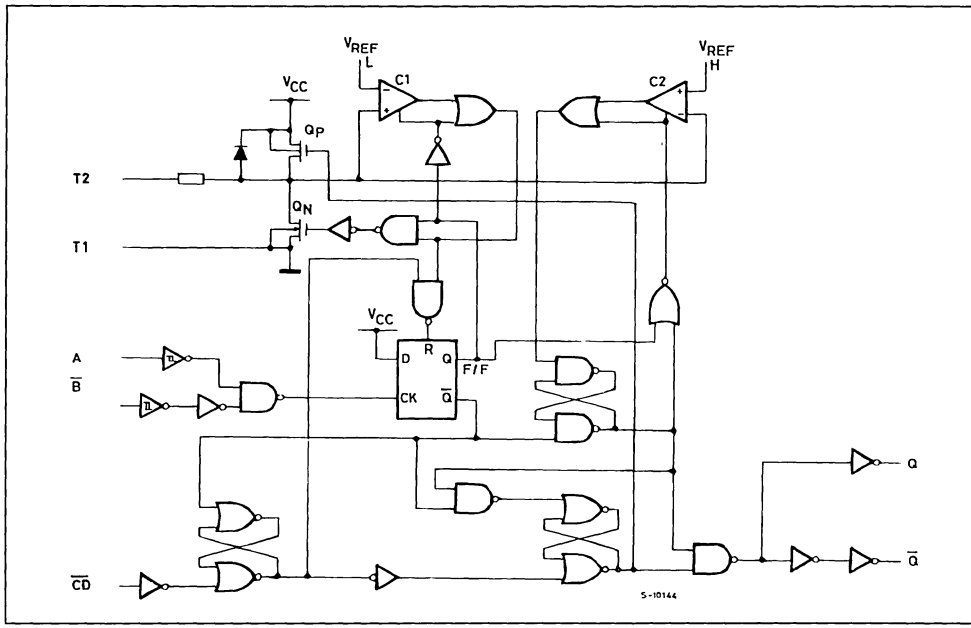
NC =
No Internal
Connection

DESCRIPTION

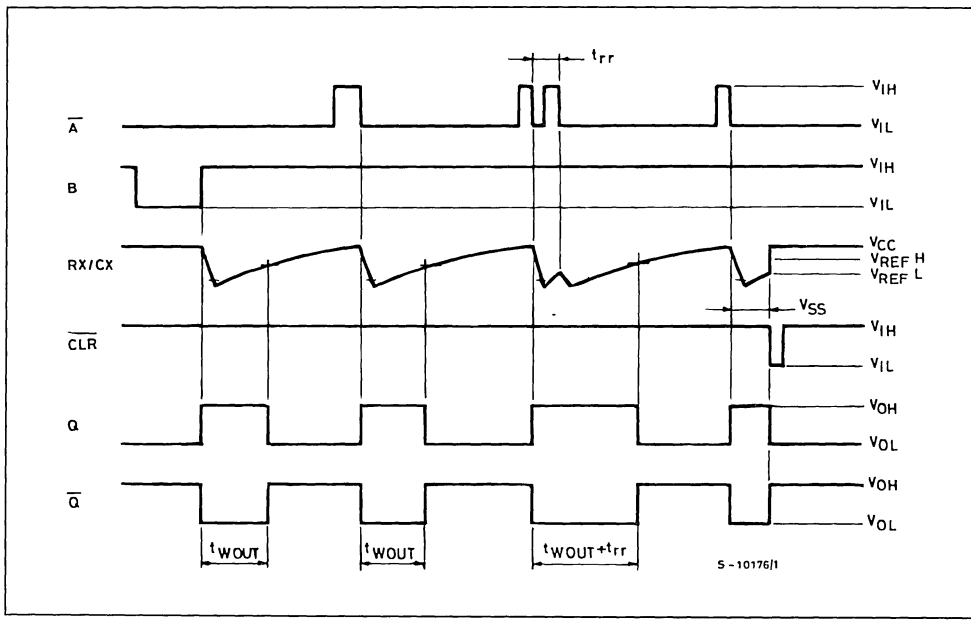
The M54/74HC4538 is a high speed CMOS DUAL MONOSTABLE MULTIVIBRATOR fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. Each multivibrator features both a negative, A, and a positive, B, edge triggered input, either of which can be used as an inhibit input. Also included is a clear input that when taken low resets the one shot. The monostable multivibrators are retriggerable. That is, they may be triggered reapeatedly while their outputs are generating a pulse and the pulse will be extended. Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques. The output pulse equation is simply : PW = 0.7 (R)(C) where PW is in seconds, R in Ohms, and C is in Farads.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

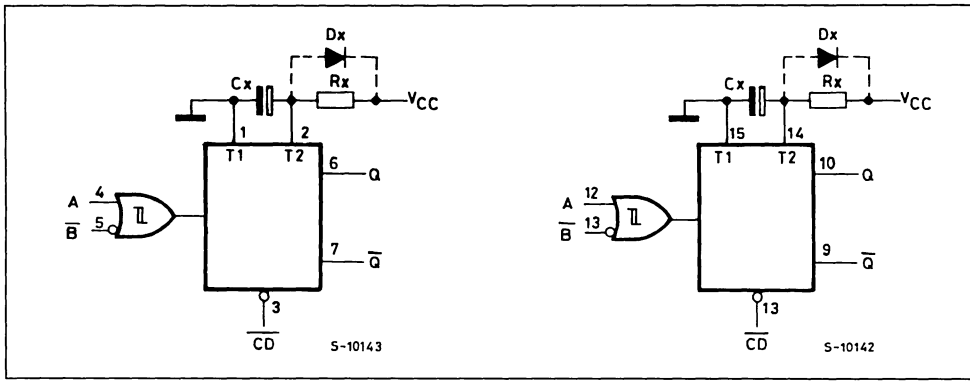
SYSTEM DIAGRAM



TIMING CHART



BLOCK DIAGRAM



Notes : 1. Cx, Rx, Dx are external components.
2. Dx is a clamping diode.
3. The external capacitor is charged to V_{CC} in the stand-by state, i.e. no trigger. When the supply voltage is turned off Cx is discharged mainly through an internal parasitic diode (see figures). If Cx is sufficiently large and V_{CC} decreases rapidy, there will be some possibility of damaging the I.C. with a surge current or latch-up. If the voltage supply filter capacitor is large enough and V_{CC} decrease slowly, the surge current is automatically limited and damage the I.C. is avoided. The maximum forward current of the parasitic diode is approximately 20 mA. In cases where Cx is large the time taken for the supply voltage to fall to 0.4 V_{CC} can be calculated as follows . $t_f \geq (V_{CC} - 0.7) \cdot Cx/20\ mA$
In cases where t_f is too short an external champing diode is required to protect the I.C. from the surge current.

FUNCTIONAL DESCRIPTION

STAND-BY STATE

The external capacitor, Cx, is fully charged to V_{CC} in the stand-by state. Hence, before triggering, transistor Qp and Qn (connected to the Rx/Cx node) are both turned off. The two comparators that control the timing and the two reference voltage sources stop operating. The total supply current is therefore only leakage current.

TRIGGER OPERATION

Triggering occurs when :

1 st) A is "low" and $\overline{B}$ has a falling edge ;

2 nd) $\overline{B}$ is "high" and A has a rising edge ;

After the multivibrator has been retriggered comparator C1 and C2 start operating and Qn is turned on. Cx then discharges through Qn. The voltage at the node Rx/Cx external falls.

When it reaches V_{REFL} the output of comparator C1 becomes low. This in turn resets the flip-flop and Qn is turned off.

At this point C1 stops functioning but C2 continues to operate. The voltage at R/C external begins to rise with a time constant set by the external components Rx, Cx.

Triggering the multivibrator causes Q to go high after internal delay due to the flip-flop and the gate. Q remains high until the voltage at R/C external rises again to V_{REFH}. At this point C2 output goes low and G goes low. C2 stops operating. That means that after triggering when the voltage at R/C external returns to V_{REFH} the multivibrator has returned to its MONOSTABLE STATE. In the case where Rx • Cx are large enough and the discharge time of the capacitor and the delay time in the I.C. can be ignored, the width of the output pulse tw (out) is as follows :

$$t_{W(OUT)} = 0.72\ Cx \bullet Rx$$

RE-TRIGGER OPERATION

When a second trigger pulse follows the first its effect will depend on the state of the multivibrator. If the capacitor Cx is being charged the voltage level of Rx/Cx external falls to V_{REFL} again and Q remains high i.e. the retrigger pulse arrives in a time shorter than the period Rx • Cx seconds, the capacitor charging time constant. If the second trigger pulse is very close to the initial trigger pulse it is ineffective ; i.e., the second trigger must arrive in the capacitor discharge cycle to be ineffective.

Hence the minimum time for a second trigger to be effective, trr (Min.) depends on V_{CC} and Cx.

FUNCTIONAL DESCRIPTION (continued)

RESET OPERATION

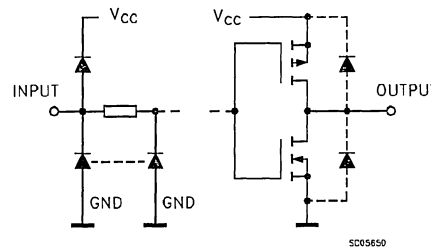
$\overline{CD}$ is normally high. If $\overline{CD}$ is low, the trigger is not effective because Q output goes low and trigger control flip-flop is reset.

Also transistor Op is turned on and Cx is charged quicky to V_{CC}. This means if $\overline{CD}$ input goes low, the IC becomes waiting state both in operating and non operating state.

TRUTH TABLE

INPUTS			OUTPUTS		NOTE
A	$\overline{B}$	$\overline{CD}$	Q	$\overline{Q}$	
⎍	H	H	⎍	⎍	OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L	⎎	H	⎍	⎍	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

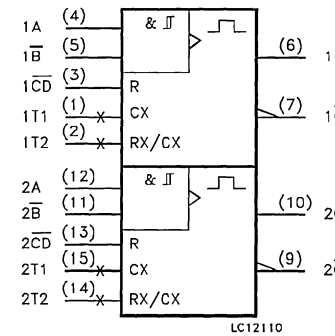
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 15	1T1, 2T1	External Capacitor Connections
2, 14	1T2, 2T2	External Resistor/Capacitor Connections
3, 13	$\overline{1CD}$, $\overline{2CD}$	Direct Reset Inputs (Active LOW)
4, 12	1A, 2A	Trigger Inputs (LOW to HIGH, Edge-Triggered)
5, 11	$1\overline{B}$, $2\overline{B}$	Trigger Inputs (HIGH to LOW, Edge-Triggered)
6, 10	Q1, Q2	Pulse Outputs
7, 9	$\overline{Q1}$, $\overline{Q2}$	Complementary Pulse Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time ($\overline{CLR}$ only)	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	
C_X	External Capacitor		NO LIMITATION (*)	
R_X	External Resistor	$V_{CC} \leq 3$ V	5K to 1M (*)	Ω
		$V_{CC} > 3$ V	1K to 1M (*)	

(*) The maximum allowable values of Cx and Rx are a function of leakage of capacitor Cx, the leakage of device and leakage due to the board layout and surface resistance. Susceptibility to externally induced noise may occur for Rx > 1MΩ

DC SPECIFICATIONS

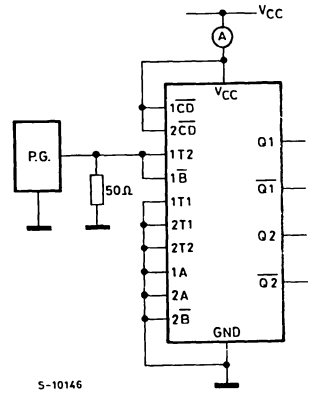
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.37		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.37		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND Rext/Cext				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA
I_{CC}	Quiescent Supply Current	2.0	V_I = V_{CC} or GND pins 2, 14 V_I = V_{CC}/2			40	120		160			µA
		4.5				0.2	0.3		0.4			mA
		6.0				0.3	0.6		0.8			mA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0				30	75		95		110	ns
		4.5				8	15		19		22	
		6.0				7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (A, B - Q, $\overline{Q}$)	2.0				120	250		315		375	ns
		4.5				30	50		63		75	
		6.0				25	43		54		64	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CD}$ - Q, $\overline{Q}$)	2.0				100	195		245		295	ns
		4.5				25	39		49		59	
		6.0				20	33		42		50	
t_{WOUT}	Output Pulse Width	2.0	C_X = 0	R_X = 5KΩ		540	1200		1500		1800	ns
		4.5	C_X = 0	R_X = 1KΩ		180	250		320		375	
		6.0	C_X = 0	R_X = 1KΩ		150	200		260		320	
		2.0	C_X = 0.01 µF R_X = 10KΩ		70	83	96	70	96	70	96	µs
		4.5	C_X = 0.01 µF R_X = 10KΩ		69	77	85	69	85	69	85	
		6.0	C_X = 0.01 µF R_X = 10KΩ		69	77	85	69	85	69	85	
		2.0	C_X = 0.1 µF R_X = 10KΩ		0.67	0.75	0.83	0.67	0.83	0.67	0.9	ms
		4.5	C_X = 0.1 µF R_X = 10KΩ		0.67	0.73	0.77	0.67	0.77	0.67	0.8	
		6.0	C_X = 0.1 µF R_X = 10KΩ		0.67	0.73	0.77	0.67	0.77	0.67	0.8	
Δt_{WOUT}	Output Pulse Width Error Between Circuits (In same pack)					±1						%
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0				30	75		95		110	ns
		4.5				8	15		19		22	
		6.0				7	13		16		19	
$t_{W(L)}$	Minimum Pulse Width (CLEAR)	2.0				30	75		95		110	ns
		4.5				8	15		19		22	
		6.0				7	13		16		19	
t_{REM}	Minimum Clear Removal Time	2.0				0	15		15		20	ns
		4.5				0	5		5		7	
		6.0				0	5		5			
t_S	Minimum Retrigger Time	2.0	C_X = 0.1 µF R_X = 1KΩ			380					6	ns
		4.5	C_X = 0.1 µF R_X = 1KΩ			92						
		6.0	C_X = 0.1 µF R_X = 1KΩ			72						
		2.0	C_X = 0.01 µF R_X = 1KΩ			6						µs
		4.5	C_X = 0.01 µF R_X = 1KΩ			1.4						
		6.0	C_X = 0.01 µF R_X = 1KΩ			1.2						
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance					70						pF

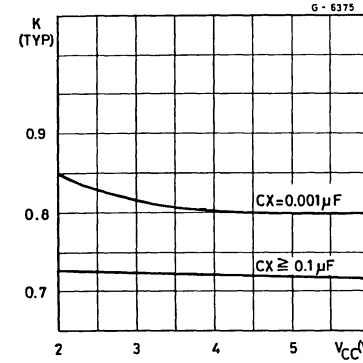
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}' \cdot Duty/100 + I_{CC}/2$ (per circuit)
(I_{CC}' = Active Supply Current)
(Duty = %))

TEST CIRCUIT I_{CC} (Opr.)

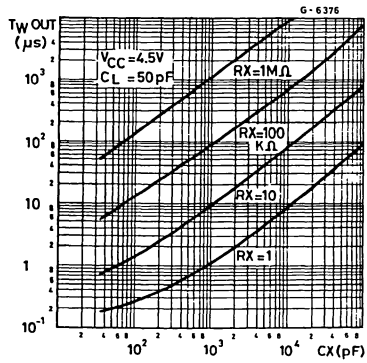


INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

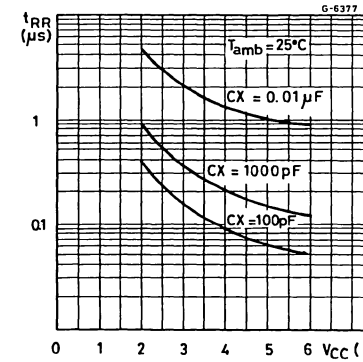
Output Pulse Width Constant K = Supply Voltage.



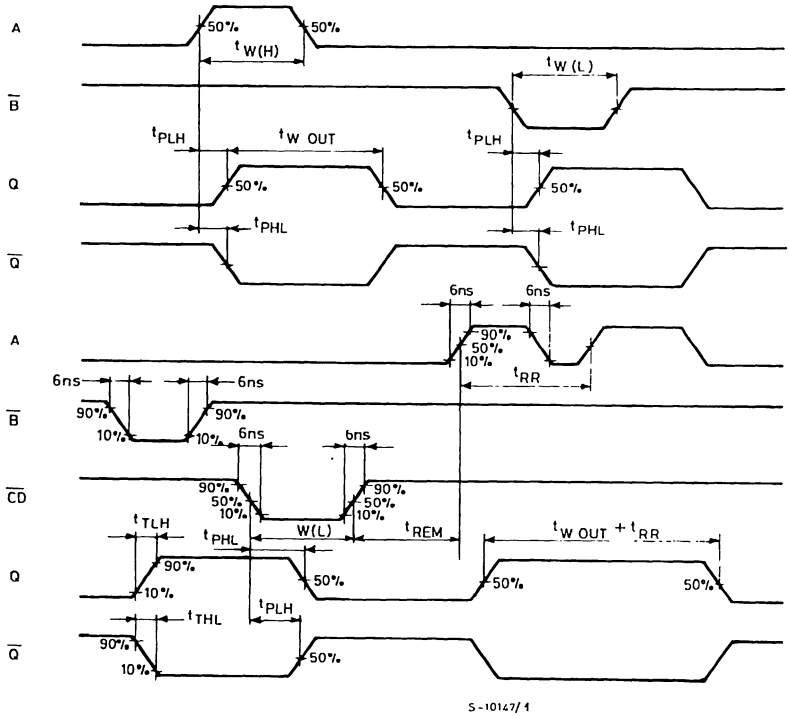
t_{WOUT} - Cx Characteristics (Typ).



t_{rr} - V_{CC} Characteristics (Typ).



SWITCHING CHARACTERISTICS TEST WAVEFORM

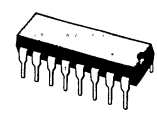


SGS-THOMSON MICROELECTRONICS

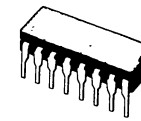
M54HC4543
M74HC4543

BCD TO 7 SEGMENT LATCH/DECODER/LCD DRIVER

- HIGH SPEED
  t_W = 7 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 4543B



B1R
(Plastic Package)



F1R
(Ceramic Package)

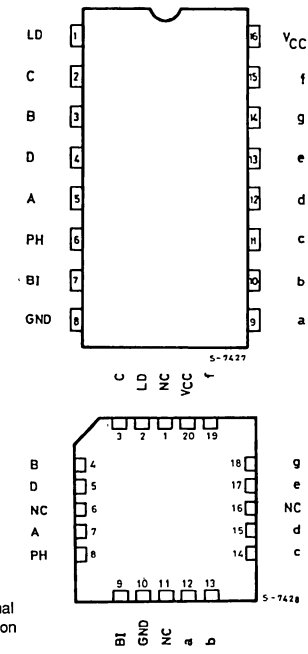
M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HC4543F1R M74HC4543M1R
M74HC4543B1R M74HC4543C1R

PIN CONNECTIONS (top view)



NC =
No Internal
Connection

DESCRIPTION

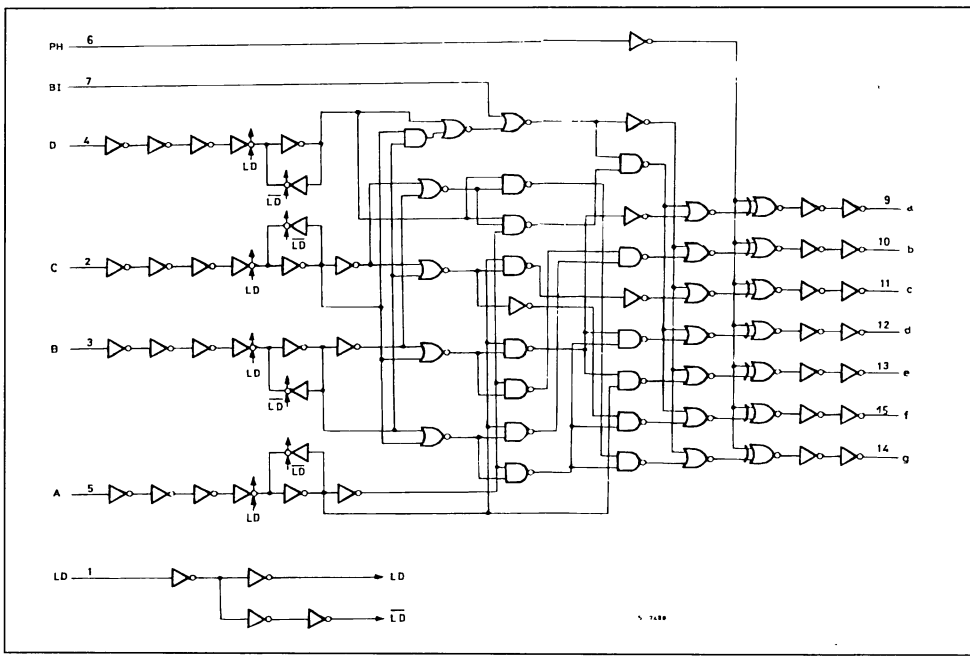
The M54/74HC4543 is a high speed CMOS BCD-TO-7 SEGMENT DECODER WITH LCD DRIVER fabricated in silicon gate C^2MOS technology. High speed latch and decode operation 120 times as fast as standard CMOS 4511B while CMOS low power consumption in maintained. This device consist of BCD-TO-7 segment decoder with a BCD input latch and a 7-segment driver for a liquid crystal display (LCD). When any illegal BCD input signal is applied or input BI is held high, the display is blanked. When driving LCDs, a common square wave signal should be applied not only to the PH input of this device but also to the electrically common backplane of the display. For other types of readouts, such as light-emitting diode (LED), some additional drivers, such as a transistor array is required. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

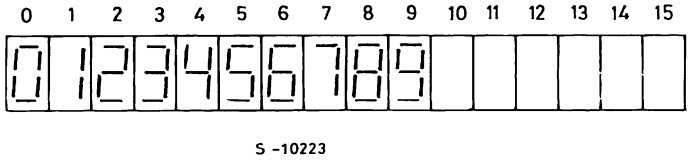
INPUTS							OUTPUTD							DISPLAY MODE
LD	BI	PH	D	C	B	A	a	b	c	d	e	f	g	
X	H	L	X	X	X	X	L	L	L	L	L	L	L	BLANK
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	X	L	L	L	L	L	L	L	BLANK
H	L	L	H	H	X	X	L	L	L	L	L	L	L	BLANK
L	L	L	X	X	X	X	# # #							# # #
↑	↑	H	↑				INVERSE OF ABOVE OUTPUT LEVEL							DISPLAY AS ABOVE

X: Don't Care
↑: SAME AS ABOVE COMBINATIONS
: DEPENDS UPON THE BCD CODE PREVIOUSLY APPLIED WHEN LD = 'H'

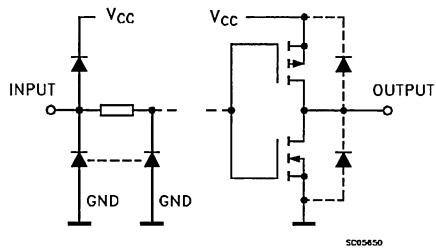
LOGIC DIAGRAM



DISPLAY MODE



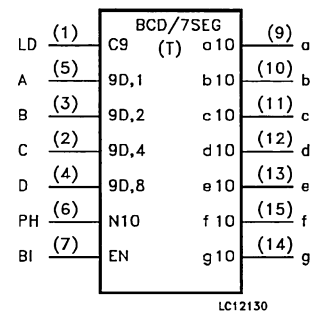
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
12	LD	Latch Disable Input (Active HIGH)
5, 3, 2, 4	A to D	Address (Data) Inputs
6	PH	Phase Input (Active HIGH)
7	BI	Blanking Input (Active HIGH)
9, 10, 11, 12, 13, 15, 14	a to g	Segment Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur Functional operation under these condition is not implied

(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

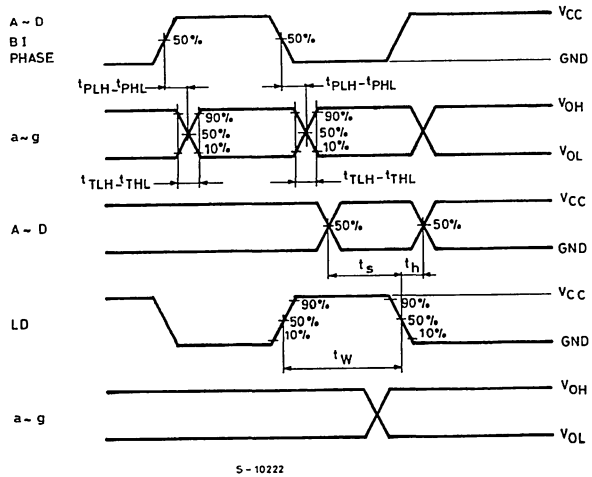
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.37		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.37		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (BCD - OUT)	2.0			160	300		375		450	ns
		4.5			40	60		75		90	
		6.0			30	51		64		76	
t_{PLH} t_{PHL}	Propagation Delay Time (BI - OUT)	2.0			80	175		220		265	ns
		4.5			23	35		44		53	
		6.0			17	30		37		45	
t_{PLH} t_{PHL}	Propagation Delay Time (PH - OUT)	2.0			58	130		165		195	ns
		4.5			17	26		33		39	
		6.0			14	22		28		33	
t_{PLH} t_{PHL}	Propagation Delay Time (LD - OUT)	2.0			130	265		335		400	ns
		4.5			35	53		66		80	
		6.0			16	45		56		68	
$t_{W(H)}$	Minimum Pulse Width (LD)	2.0			30	75		95		110	ns
		4.5			8	15		29		22	
		6.0			7	13		26		19	
t_s	Minimum Set-up Time	2.0			15	75		95		110	ns
		4.5			4	15		19		22	
		6.0			3	13		16		19	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				115						pF

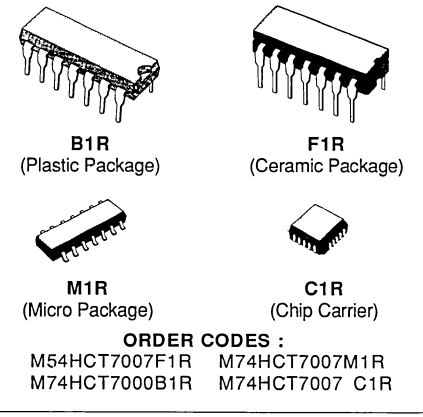
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per FLIP/FLOP)

SWITCHING CHARACTERISTICS TEST WAVEFORM



HEX BUFFER

- HIGH SPEED
  t_{pd} = 11 ns (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS07



B1R
(Plastic Package)

F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HCT7007F1R M74HCT7007M1R
M74HCT7000B1R M74HCT7007 C1R

DESCRIPTION

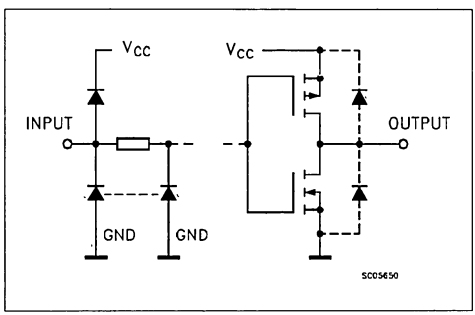
The M54/74HCT7007 is a high speed CMOS HEX BUFFER fabricated in silicon gate C^2MOS technology.

It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

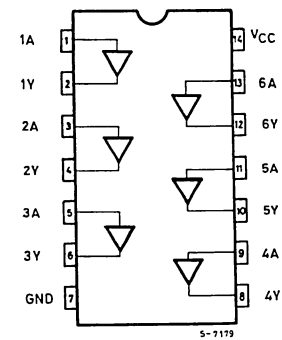
All inputs are equipped with protection circuits against static discharge and transient excess voltage. The integrated circuit has totally compatible, input and output characteristic, with standard 54/74 LSTTL logic families.

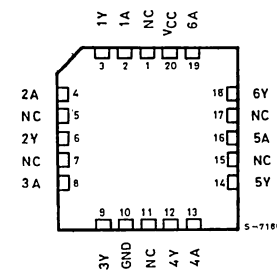
M54HCT/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. These devices are also plug in replacement for LSTTL devices giving a reduction of power consumption.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



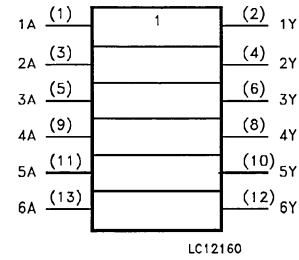


NC =
No Internal
Connection

TRUTH TABLE

A	Y
L	L
H	H

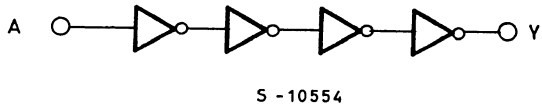
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	Data Inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	Data Outputs
7	GND	Ground (0V)

SCHEMATIC CIRCUIT (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

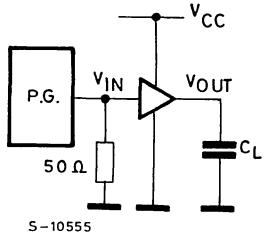
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				1		10		20	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9		3.0	mA

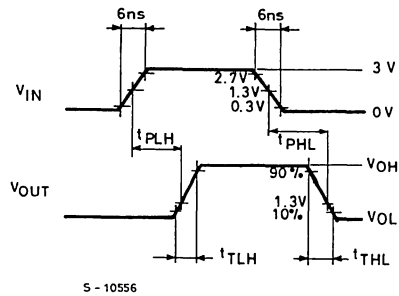
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			8	15		19		23	ns
t_{PLH} t_{PHL}	Propagation Delay Time	4.5			14	23		29		35	ns
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				22						pF

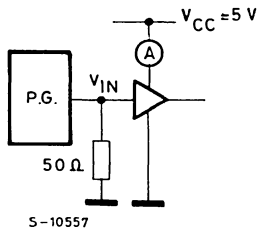
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$ (per BUFFER)

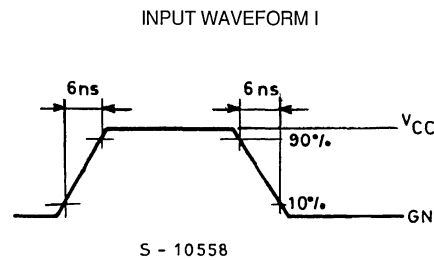
SWITCHING CHARACTERISTICS TEST CIRCUIT





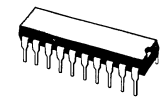
TEST CIRCUIT I_{CC} (Opr.)



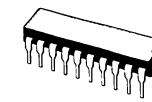


OCTAL BUS BUFFER WITH 3 STATE OUTPUTS
HC7240: INVERTED - HC7241/7244 NON INVERTED

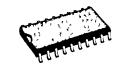
- HIGH SPEED
  t_{PD} = 15 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY
  V_H = 1.1 V(TYP.) at V_{CC} = 5V
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS240/241/244



B1R
(Plastic Package)



F1R
(Ceramic Package)



M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HCXXXXF1R M74HCXXXXM1R
M74HCXXXXB1R M74HCXXXXC1R

DESCRIPTION

The M54/74HC7240, HC7241 and HC7244 are high speed CMOS OCTAL BUS BUFFERs fabricated in silicon gate C^2MOS technology.

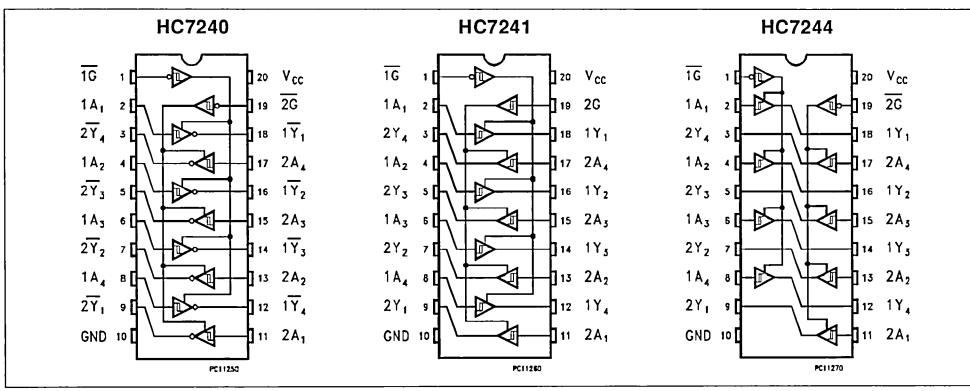
They have the same high speed performance of LSTTL combined with true CMOS low power consumption.

The designer has a choise of select combination of inverting and non-inverting outputs, symmetrical $\overline{G}$ (active low output control) input, and complementary G and $\overline{G}$ inputs. Each control input governs four BUS BUFFERs.

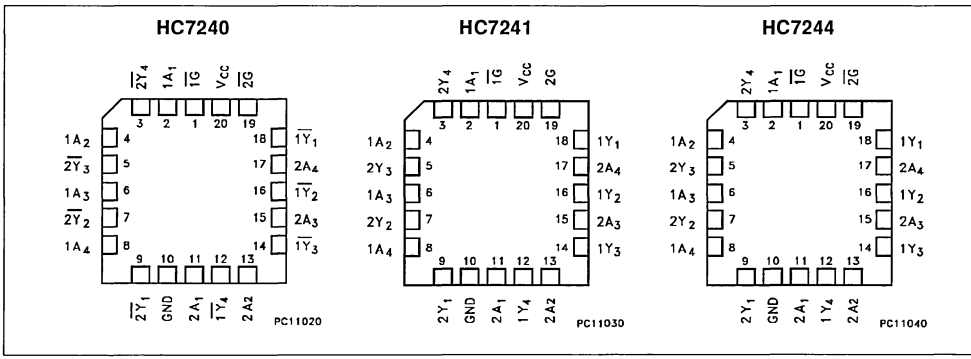
The HC7240, HC7241 and HC7244 have the same pin configuration and function as the HC240, HC241 and HC244 and they have a hysteresis characteristics with each input so can be used as a line receiver, etc.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

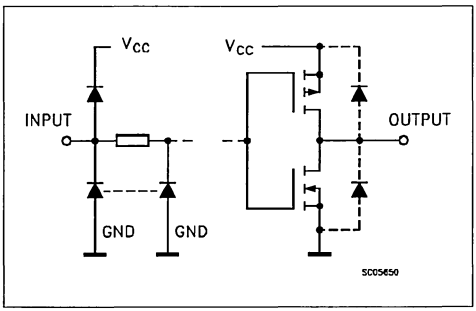
PIN CONNECTION (top view)



CHIP CARRIER



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION (HC7240)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{1G}$	Output Enable Input
2, 4, 6, 8	1A1 to 1A4	Data Inputs
9, 7, 5, 3	$\overline{2Y1}$ to $\overline{2Y4}$	Data Outputs
11, 13, 15, 17	2A1 to 2A4	Data Inputs
18, 16, 14, 12	$\overline{1Y1}$ to $\overline{1Y4}$	Data Outputs
19	$\overline{2G}$	Output Enabel Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

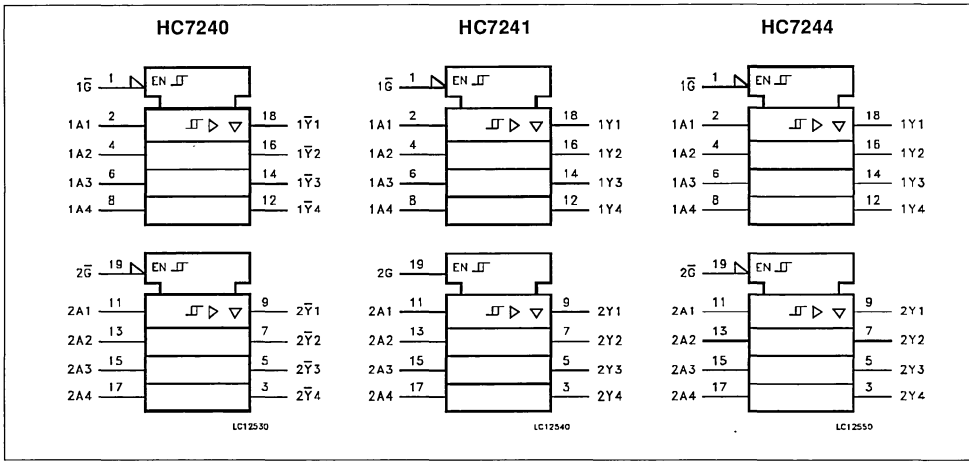
PIN DESCRIPTION (HC7241)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{1G}$	Output Enable Input
2, 4, 6, 8	1A1 to 1A4	Data Inputs
9, 7, 5, 3	2Y1 to 2Y4	Data Outputs
11, 13, 15, 17	2A1 to 2A4	Data Inputs
18, 16, 14, 12	1Y1 to 1Y4	Data Outputs
19	2G	Output Enabel Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

PIN DESCRIPTION (HC7244)

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{1G}$	Output Enable Input
2, 4, 6, 8	1A1 to 1A4	Data Inputs
9, 7, 5, 3	2Y1 to 2Y4	Data Outputs
11, 13, 15, 17	2A1 to 2A4	Data Inputs
18, 16, 14, 12	1Y1 to 1Y4	Data Outputs
19	$\overline{2G}$	Output Enabel Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS

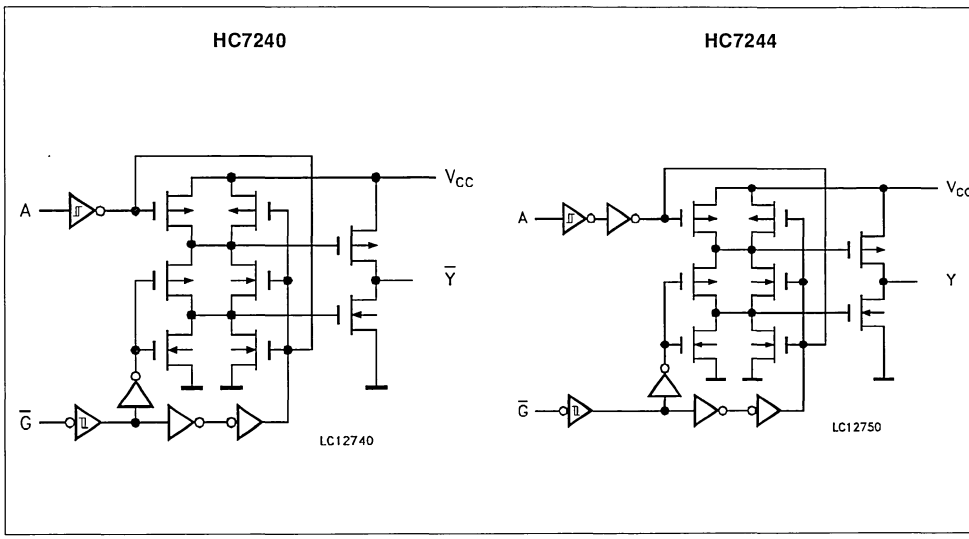


TRUTH TABLE

INPUT			OUTPUT		
$\overline{G}$	G (HC7241)	An	$\overline{Yn}$ (HC7240)	Yn (HC7241)	Yn (HC7244)
L	H	L	H	L	L
L	H	H	L	H	H
H	L	X	Z	Z	Z

X: "H" or "L"
Z: High impedance

CIRCUIT SCHEMATIC (1/8 PACKAGE)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C

DC SPECIFICATIONS

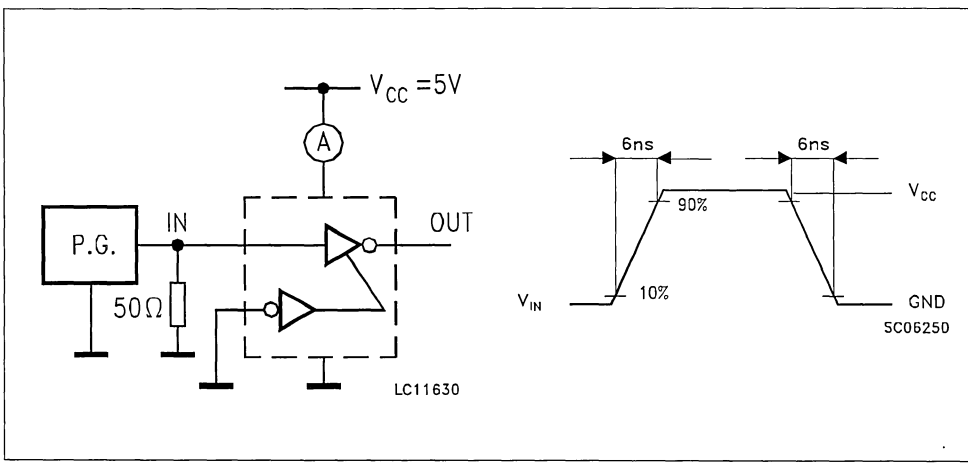
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_P	High Level Threshold Voltage	2.0			1.0	1.25	1.5	1.0	1.5	1.0	1.5	V
		4.5			2.3	2.7	3.15	2.3	3.15	2.3	3.15	
		6.0			3.0	3.5	4.2	3.0	4.2	3.0	4.2	
V_N	Low Level Threshold Voltage	2.0			0.3	0.65	0.9	0.3	0.9	0.3	0.9	V
		4.5			1.13	1.6	2.0	1.13	2.0	1.13	2.0	
		6.0			1.5	2.3	2.6	1.5	2.6	1.5	2.6	
V_H	Hysteresis Voltage	2.0			0.3	0.6	1.0	0.3	1.0	0.3	1.0	V
		4.5			0.6	1.1	1.4	0.6	1.4	0.6	1.4	
		6.0			0.8	1.2	1.7	0.8	1.7	0.8	1.7	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0		I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	3 State Output Off State Current	6.0	V_I = V_{CC} or GND				±0.5		±5		±10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75			ns
		4.5				7	12		19			
		6.0				6	10		13			
t_{PLH} t_{PHL}	Propagation Delay Time	2.0	50			50	125		155			ns
		4.5				15	25		31			
		6.0				13	21		26			
t_{PZL} t_{PZH}	Output Enable Time	2.0	50	R_L = 1KΩ		68	150		190			ns
		4.5				21	30		38			
		6.0				16	26		32			
t_{PLZ} t_{PHZ}	Output Disable Time	2.0	50	R_L = 1KΩ		48	150		190			ns
		4.5				21	30		38			
		6.0				19	26		32			
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{OUT}	Output Capacitance					10						pF
C_{PD} (*)	Power Dissipation Capacitance		HC7240 HC7241/7244			33 34						pF

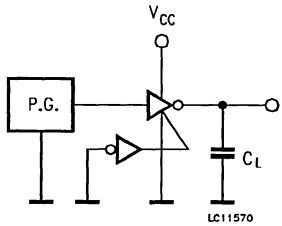
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per channel)

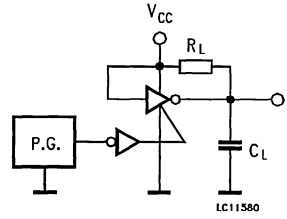
TEST CIRCUIT I_{CC} (Opr.)

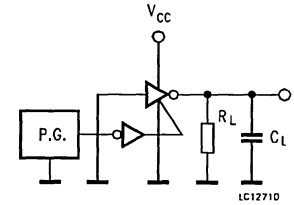


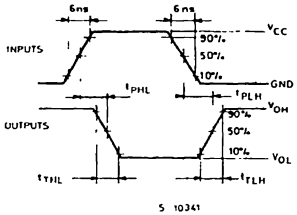
SWITCHING CHARACTERISTICS TEST CIRCUIT

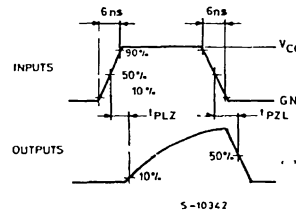
HC7240

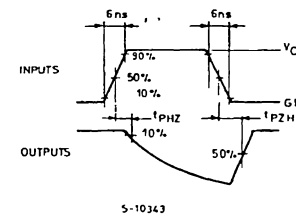




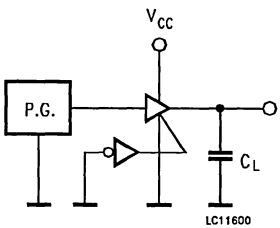


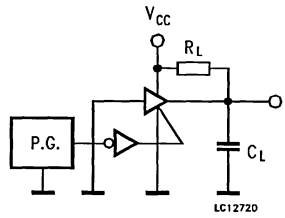


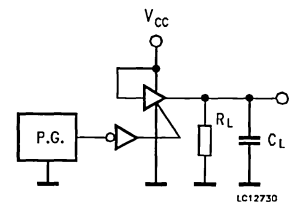


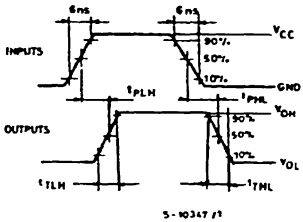


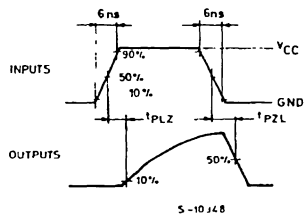
HC7241/HC7244

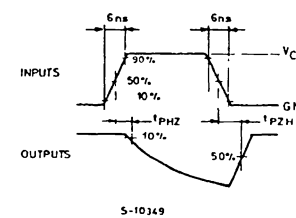






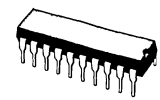




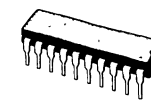


OCTAL BUS TRANSCEIVER (3-STATE): HC7645 NON INVERTING HC7640 INVERTING , HC7643 INVERTING/NON INVERTING

- HIGH SPEED
  t_{PD} = 12 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY
  V_H = 1.1 (TYP.) at V_{CC} = 5V
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS245/640/643



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

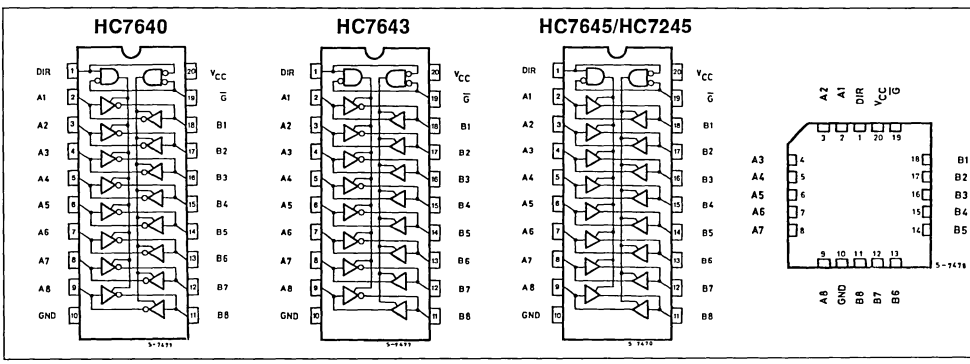
ORDER CODES :

M54HCXXXXF1R M74HCXXXXM1R
M74HCXXXXB1R M74HCXXXXC1R

DESCRIPTION

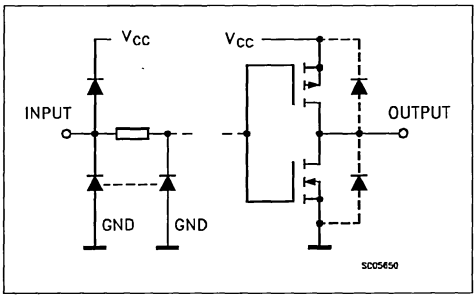
The M54/74HC7245 HC7640, HC7643 and HC7645 utilise silicon gate C^2MOS technology to achive operating speeds equivalent to LSTTL devices.
Along with the low power dissipation and high noise immunity of standads C^2MOS integrated circuit, it possesses the capability to drive 15 LSTTL loads. These IC's are intended for two-way asynchronous communication between data buses, and the direction of data trasmission is determined by DIR input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.
The HC7245/640/7643/7645 have the same pin configuration and function as the HC245/640/643 and they have a hysteresis characteristics with each input, so HC7245/7640/7643/7645 can be used as a line receiver, etc. All input are equipped with protection circuits against static discharge and transient excess voltage.
IT IS PROHIBITED TO APPLY A SIGNAL TO A BUS TERMINAL WHEN IT IS IN OUTPUT MODE AND WHEN A BUS THERMINAL IS FLOATING (HIGH IMPEDANCE STATE), IT IS REQUESTED TO FIX THE INPUT LEVEL BY MEANS OF EXTERNAL PULL DOWN OR PULL UP RESISTOR.

PIN CONNECTION (top view)



HC7245 is electrically and funcutionally the same as the HC7645

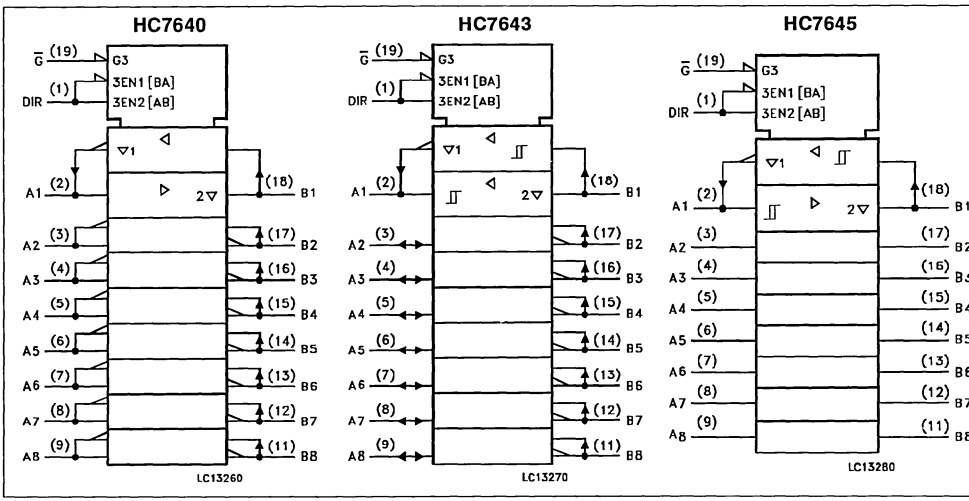
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	DIR	Directional Control
2, 3, 4, 5, 6, 7, 8, 9	A1 to A8	Data Inputs/Outputs
18, 17, 16, 15, 14, 13, 12, 11	B1 to B8	Data Inputs/Outputs
19	$\overline{G}$	Output Enabel Input (Active LOW)
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS



TRUTH TABLE

INPUT		FUNCTION		OUTPUT		
$\overline{G}$	DIR	A BUS	B BUS	HC7640	HC7643	HC7645/7245
L	L	OUTPUT	INPUT	$A = \overline{B}$	A = B	A = B
L	H	INPUT	OUTPUT	$B = \overline{A}$	$B = \overline{A}$	B = A
H	X	Z	Z	Z	Z	Z

X: "H" or "L"
Z: High impedance

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C

DC SPECIFICATIONS

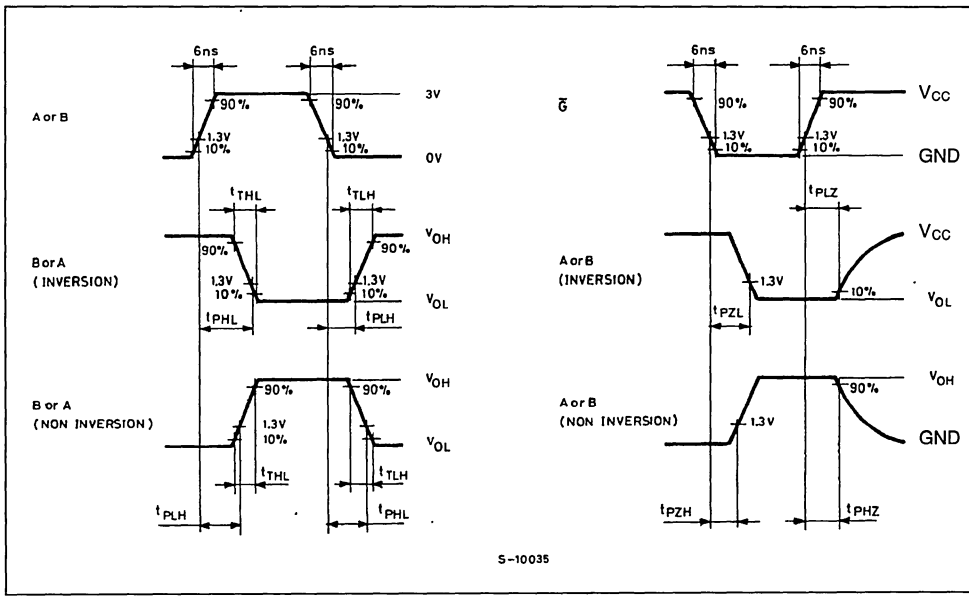
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_P	Positive Threshold Voltage (An, Bn inputs)	2.0			1	1.25	1.5	1	1.5	1	1.5	V
		4.5			2.3	2.7	3.15	2.3	3.15	2.3	3.15	
		6.0			3	3.5	4.2	3	4.2	3	4.2	
V_N	Negative Threshold Voltage (An, Bn inputs)	2.0			0.3	0.65	0.9	0.3	0.9	0.3	0.9	V
		4.5			1.13	1.6	2	1.13	2	1.13	2	
		6.0			1.5	2.3	2.6	1.5	2.6	1.5	2.6	
V_H	Hysteresiis Voltage (An, Bn inputs)	2.0			0.3	0.6	1	0.3	1	0.3	1	V
		4.5			0.6	1.1	1.4	0.6	1.4	0.6	1.4	
		6.0			0.8	1.2	1.7	0.8	1.7	0.8	1.7	
V_{IH}	High Level Input Voltage (DIR, $\overline{G}$ inputs)	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage (DIR, $\overline{G}$ inputs)	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 6.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{OZ}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				æ0.5		±5		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			25	60		75		90	ns
		4.5			7	12		15		18	
		6.0			6	10		13		15	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0			61	125		156		190	ns
		4.5			15	25		31		38	
		6.0			13	21		27		32	
t_{PZL} t_{PZH}	Output Enable Time	2.0			77	150		188		225	ns
		4.5	R_L = 1 KΩ		19	30		38		45	
		6.0			16	26		32		38	
t_{PLZ} t_{PHZ}	Output Disable Time	2.0			84	150		188		225	ns
		4.5	R_L = 1 KΩ		21	30		38		45	
		6.0			18	26		32		38	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{OUT}	Output Capacitance										pF
C_{PD} (*)	Power Dissipation Capacitance										pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST WAVEFORM

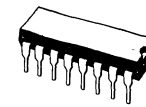


SGS-THOMSON MICROELECTRONICS

M74HCT7259

8 BIT ADDRESSABLE LATCH/DECODER/RELAIS DRIVER (OPEN DRAIN, INVERTING OUTPUT)

- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  90 LSTTL LOADS
- HIGH CURRENT OPEN DRAIN OUTPUT UP TO 80 mA



B1R
(Plastic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :
M74HCT7259B1R M74HCT7259M1R
M74HCT7259C1R

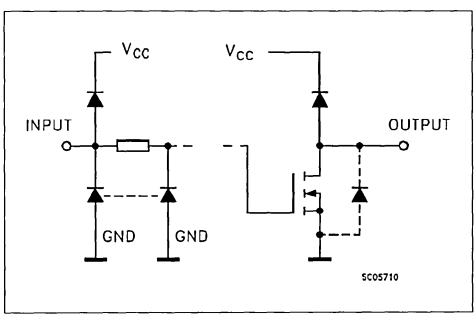
DESCRIPTION

The **M74HCT7259** is a high speed CMOS 8 BIT ADDRESSABLE LATCH/DECODER fabricated in silicon gate C2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

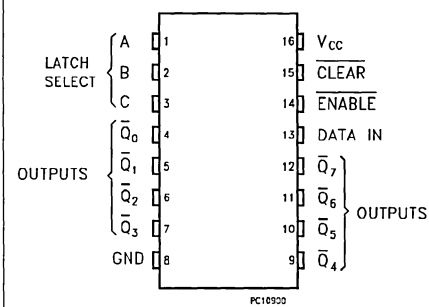
The **M74HCT7259** has single data input (D) 8 LATCH inverted OUTPUTS ($\overline{Q0}$-$\overline{Q7}$), 3 address inputs (A, B and C), common enable input ($\overline{ENABLE}$) and a common $\overline{CLEAR}$ input. To operate this device as an addressable latch, data is held on the D input, and the address of the latch into which the data is to be entered is held on the A, B and C inputs.

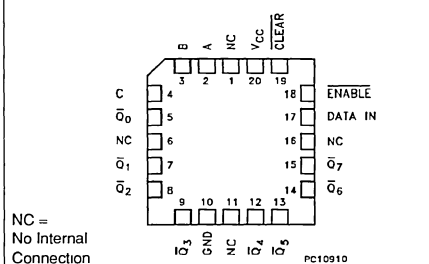
When $\overline{ENABLE}$ is taken low the data flows through to the address output. The data is stored on the positive-going edge of the $\overline{ENABLE}$ pulse. All unadressed latches will remain unaffected. With $\overline{ENABLE}$ in the high state the device is deselected and all latches remain in their previous state, unaffected by changes on the data or address inputs. To eliminate the possibility of entering erroneous data into the latches, the $\overline{ENABLE}$ should be held high (inactive)

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)

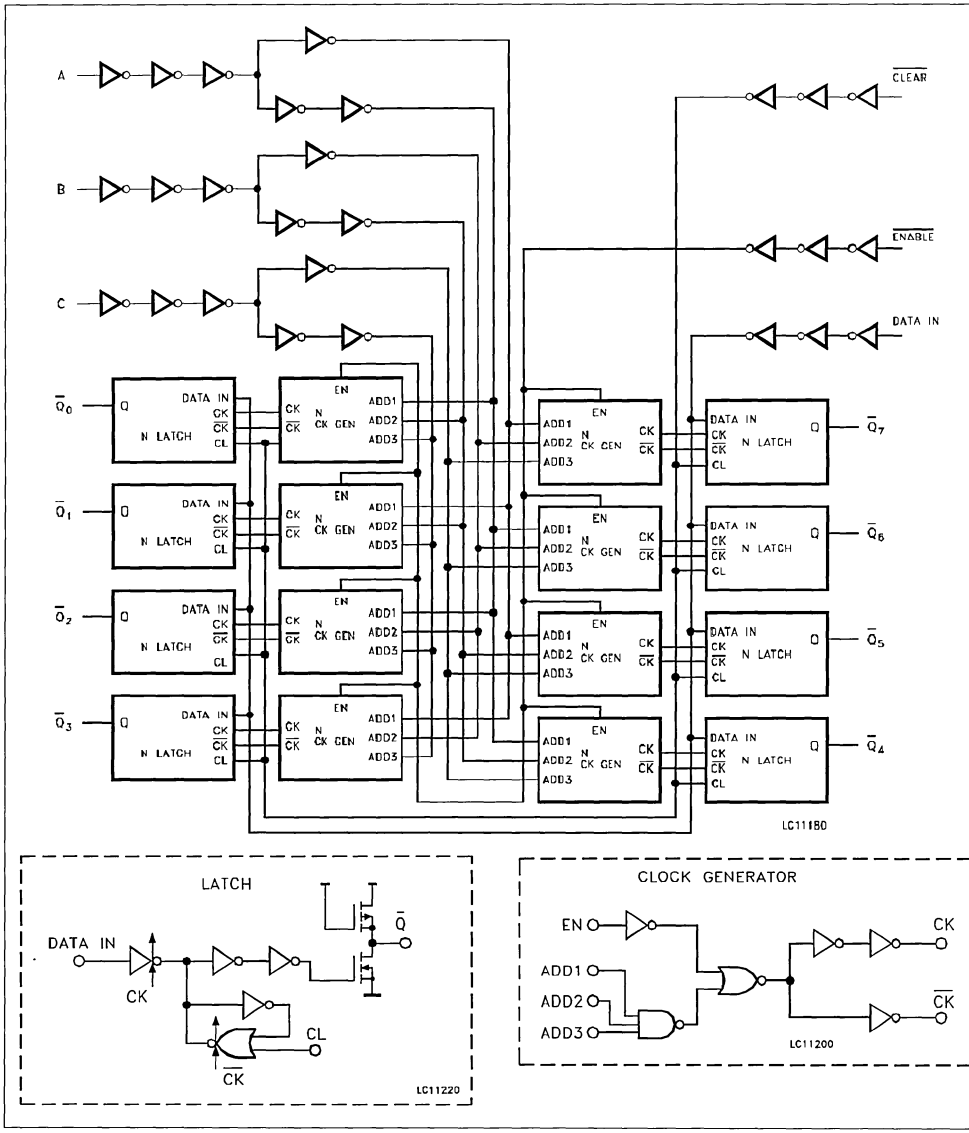




while the address lines are changing. If $\overline{\text{ENABLE}}$ is held high and $\overline{\text{CLEAR}}$ is taken low all eight latches are cleared to the HIGH (OFF) state. If $\overline{\text{ENABLE}}$ is low all latches except the addressed latch will be cleared. The address latch will instead be the complement of the D input,effectively implementing a 3 to 8 line decoder. Internal clamp diodes protect the open drain outputs against over voltages due to inductive loads.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

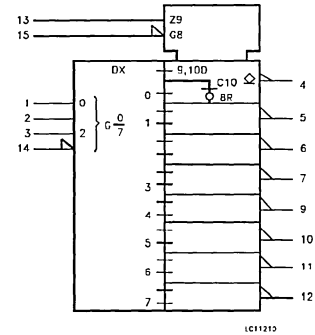
LOGIC DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3	A, B, C	Latch Select
4, 5, 6, 7, 9, 10, 11, 12	$\overline{Q0}$ to $\overline{Q7}$	latch Outputs
13	DATA IN	Data Inputs
14	$\overline{ENABLE}$	Latch Enable Input
15	$\overline{CLEAR}$	Conditional Reset Input
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS		OUTPUTS OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
$\overline{CLEAR}$	$\overline{ENABLE}$			
H	L	$\overline{D}$	QI0	ADDRESSABLE LATCH
H	H	Qi0	Qi0	MEMORY
L	L	$\overline{D}$	H	8-LINE DEMULTIPLEXER
L	H	H	H	CLEAR ALL BITS TO "H"

SELECT INPUTS			LATCH ADDRESSED
C	B	A	
L	L	L	$\overline{Q0}$
L	L	H	$\overline{Q1}$
L	H	L	$\overline{Q2}$
L	H	H	$\overline{Q3}$
H	L	L	$\overline{Q4}$
H	L	H	$\overline{Q5}$
H	H	L	$\overline{Q6}$
H	H	H	$\overline{Q7}$

D: The level at the data input

Qi0 The level before the indicated steady state input conditions were established, (i = 0,1,. ..,7).

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{DD} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current Per Pin	100	mA
I_{GND}	DC Ground Current	- 800	mA
I_{CC}	DC V_{CC} Current	50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature 10 sec	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied

(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C. 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-40 to +85	°C
t_r, t_f	Input Rise and Fall Time	0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5		2.0			2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5				0.8		0.8	V
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}; I_O= 20 µA		0.0	0.1		0.1	V
			V_I = V_{IH} or V_{IL}; I_O= 36 mA		0.17	0.26		0.33	
			V_I = V_{IH} or V_{IL}; I_O= 80 mA		0.32	0.40		0.50	
I_{OZ}	Output Leackage Current	5.5	V_I = V_{IH} or V_{IL}; V_{OUT} = V_{CC} or GND			±5		±50	µA
I_{IN}	Input Leakage Current	5.5	V_I = V_{CC} or GND			±0.1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND			4		40	µA
			Each Input in Turn: V_{IN} = 0.5 V or 2.4 V All Other Inputs: V_{CC} or GND			3.0		3.9	mA

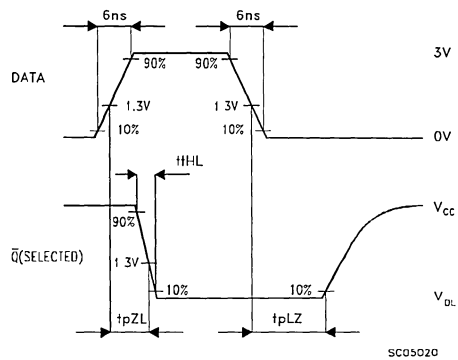
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value					Unit
		V_{CC} (V)	C_L (pF)	R_L (KΩ)	T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
t_{TLH}	Output Transition Time	4.5	50	1		3	6		9	ns
t_{PLZ} t_{PZL}	Propagation Delay Time (DATA - Q)	4.5	50	1		20	31		39	ns
		4.5	150	1		24	37		46	
t_{PLZ} t_{PZL}	Propagation Delay Time (A, B, C - Q)	4.5	50	1		25	39		49	ns
		4.5	150	1		29	45		56	
t_{PLZ} t_{PZL}	Propagation Delay Time (ENABLE - Q)	4.5	50	1		21	33		41	ns
		4.5	150	1		25	39		49	
t_{PLZ} t_{PZL}	Propagation Delay Time ($\overline{CLEAR}$ - Q)	4.5	50	1		19	30		38	ns
		4.5	150	1		23	36		45	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLEAR}$)	4.5	50	1		7	15		19	ns
$t_{W(L)}$	Minimum Pulse Width ($\overline{ENABLE}$)	4.5	50	1		7	15		19	ns
t_s	Minimum Set-Up Time	4.5	50	1		4	10		13	ns
t_h	Minimum Hold Time	4.5	50	1			5		5	ns
C_{IN}	Input Capacitance					5	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance					96				pF

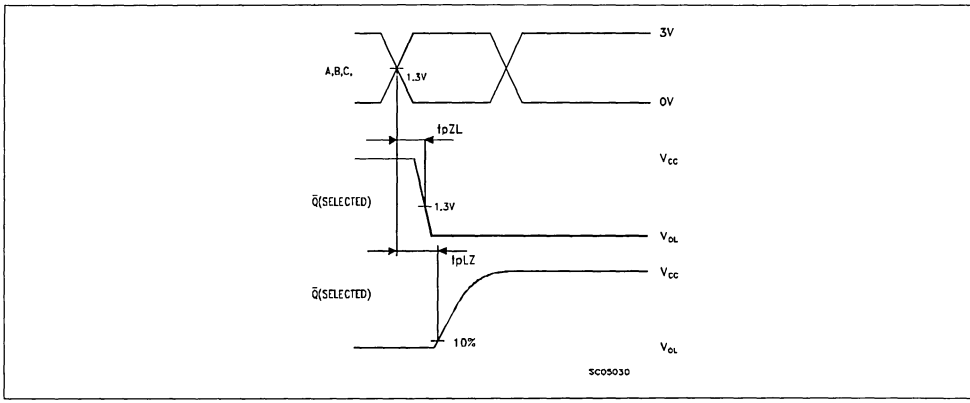
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (Refer to Test Circuit) Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORMS

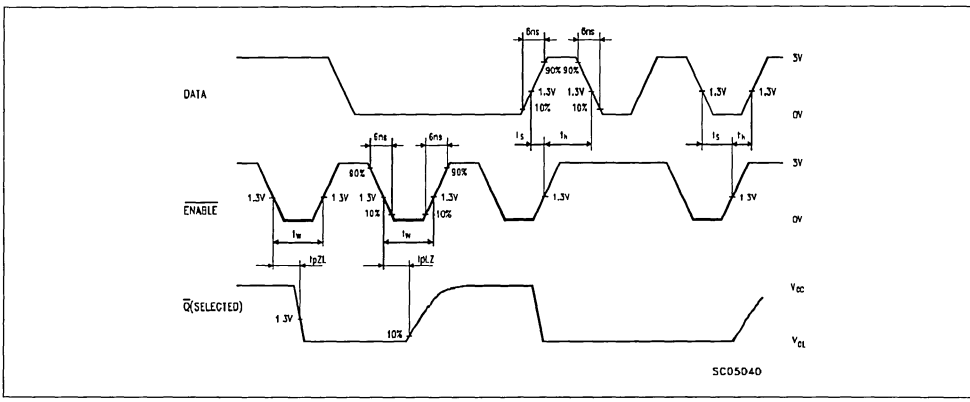
WAVEFORM 1: ($\overline{ENABLE}$ = L, $\overline{CLR}$ = H, A-C= STABLE)



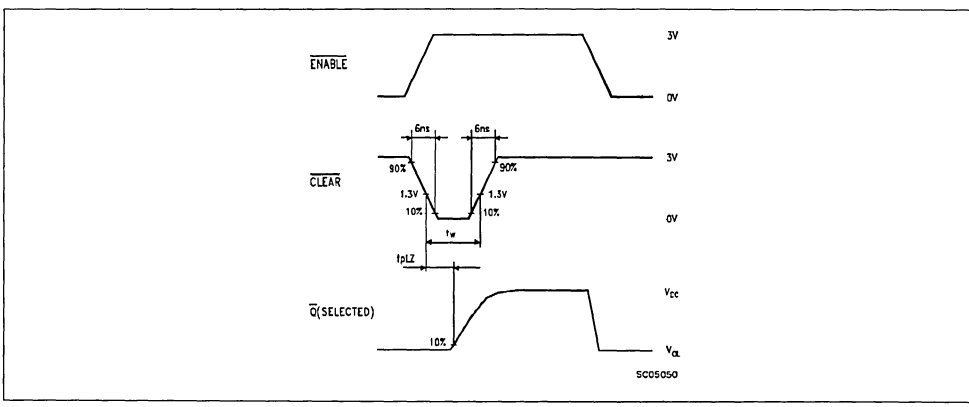
WAVEFORM 2: ($\overline{ENABLE}$ = L)



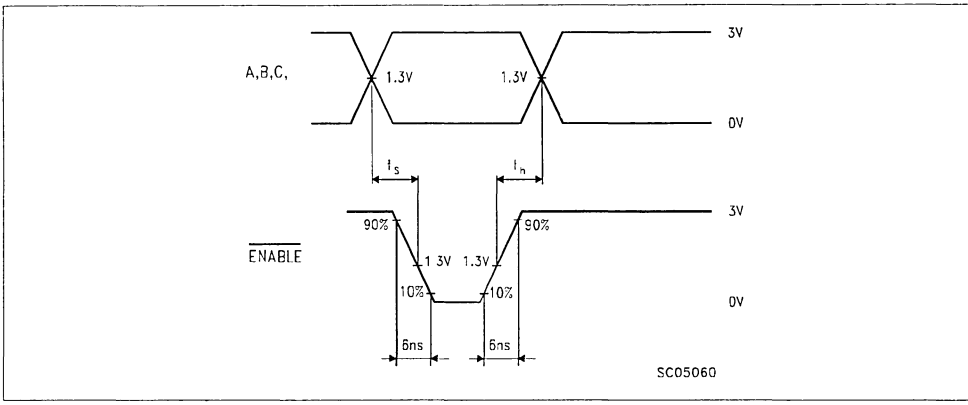
WAVEFORM 3: ($\overline{CLR}$ = H, A-C = STABLE)



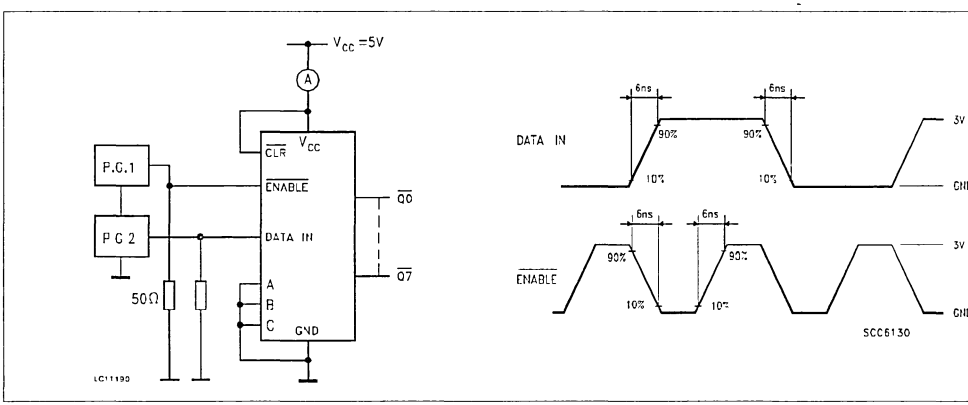
WAVEFORM 4: (D = H, A-C = STABLE)



WAVEFORM 5: ($\overline{CLR}$ = H)

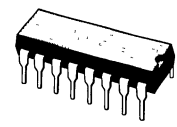


TEST CIRCUIT I_{CC} (Opr.)

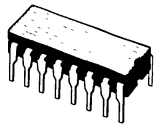


8 STAGE PRESETTABLE SYNCHRONOUS DOWN COUNTERS

- HIGH SPEED
  f_{MAX} = 40 MHz (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V to 6 V
- PIN AND FUNCTION COMPATIBLE WITH 40102B/40103B



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

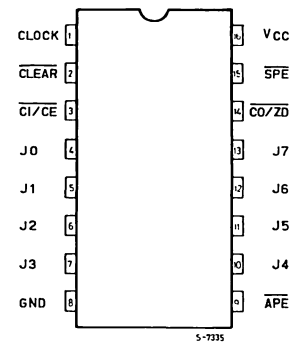
M54HCXXXXXF1R M74HCXXXXXM1R
M74HCXXXXXB1R M74HCXXXXX C1R

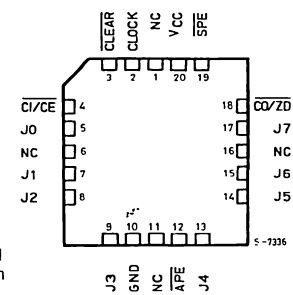
DESCRIPTION

The M54/74HC40102/40103 are high speed CMOS 8-STAGE PRESETTABLE SYNCHRONOUS DOWN COUNTERS fabricated with silicon gate C^2MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The HC40102, and HC40103 consist of an 8-stage synchronous down counter with a single output which is active when the internal count is zero. The HC40102 is configured as two cascaded 4-bit BCD counters, and the HC40103 contains a single 8-bit binary counter. Each type has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the CARRY-OUT/ZERO-DETECT output are active-low logic. In normal operation, the counter is decremented by one count on each positive transition of the CLOCK. Counting is inhibited when the CARRY-IN/COUNTER ENABLE ($\overline{CI/CE}$) input is high. The CARRY-OUT/ZERO-DETECT ($\overline{CO/ZD}$) output goes low when the count reaches zero if the $\overline{CI/CE}$ input is low, and remains low for one full clock period. When the SYNCHRONOUS PRESET-ENABLE ($\overline{SPE}$) input is low, data at the J input is clocked into the counter on the next positive clock transition regardless of the state of the $\overline{CI/CE}$ input.

PIN CONNECTIONS (top view)





NC =
No Internal
Connection

DESCRIPTION (Continued)

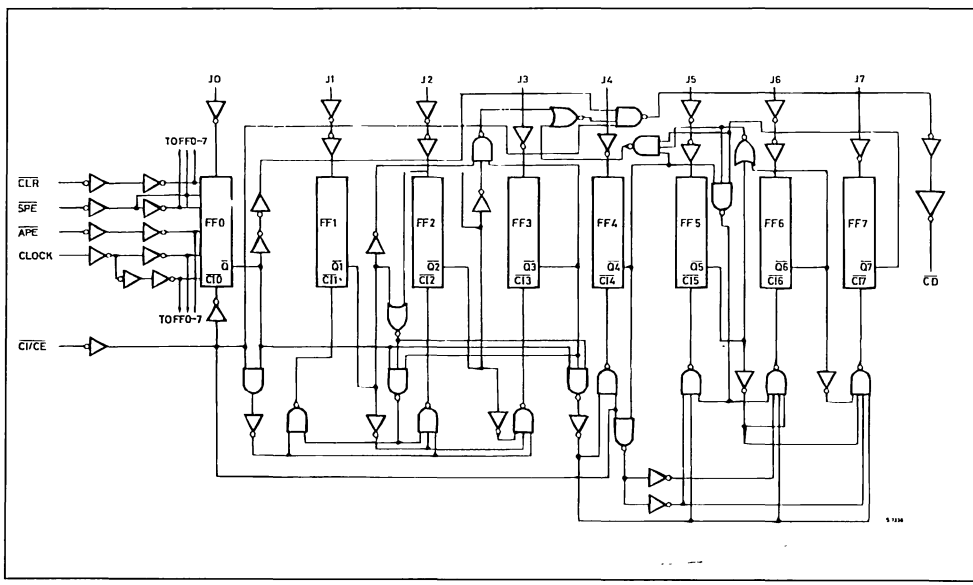
When the ASYNCHRONOUS PRESET-ENABLE ($\overline{APE}$) input is low, data at the J inputs is asynchronously forced into the counter regardless of the state of the $\overline{SPE}$, $\overline{CI/CE}$, or CLOCK inputs. J Inputs J0-J7 represent two 4-bit BCD words for the HC40102 and a single 8-bit binary word for the HC40103. When the CLEAR ($\overline{CLR}$ input is low, the counter is asynchronously cleared to its maximum count (99_{10} for the HC40102 and 255_{10} for the HC40103 regardless of the state of any other input. The precedence relationship between control input is indicated in the truth table. If all control inputs are high at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 100 pr 256 clock pulses long. The HC40102 and HC40103 may be cascaded using the $\overline{CI/CE}$ input and the $\overline{CO/ZD}$ output, in either a synchronous or ripple mode. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

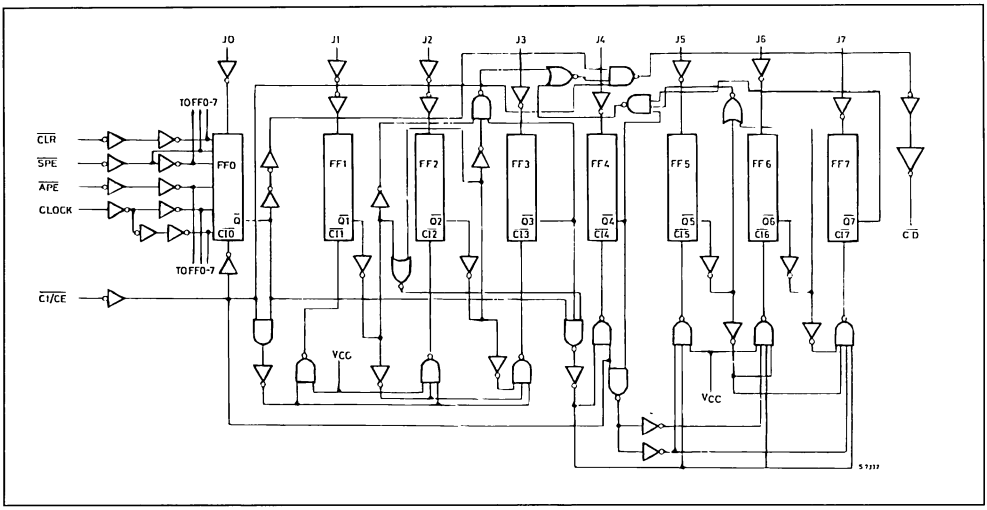
CONTROL INPUTS				MODE	FUNCTIONAL DESCRIPTION
$\overline{CLEAR}$	$\overline{APE}$	$\overline{SPE}$	$\overline{CI/CE}$		
H	H	H	H	COUNT INHIBIT	EVEN IF CLOCK IS GIVEN, NO COUNT IS MADE
H	H	H	L	REGULAR COUNT	DOWN COUNT AT RISING EDGE OF CLOCK
H	H	L	X	SYNCHRONOUS PRESET	DATA OF PI TERMINAL IS PRESET AT RISING EDGE OF CLOCK
H	L	X	X	ASYNCRONOUS PRESET	DATA PF PI TERMINAL IS ASYNCHRONOUSLY PRESET TO CLOCK
L	X	X	X	CLEAR	COUNTER IS SET TO MAXIMUM COUNT

X: DON'T CARE - MAXIMUM COUNT: "99" FOR HC40102 AND "255" FOR HC40103

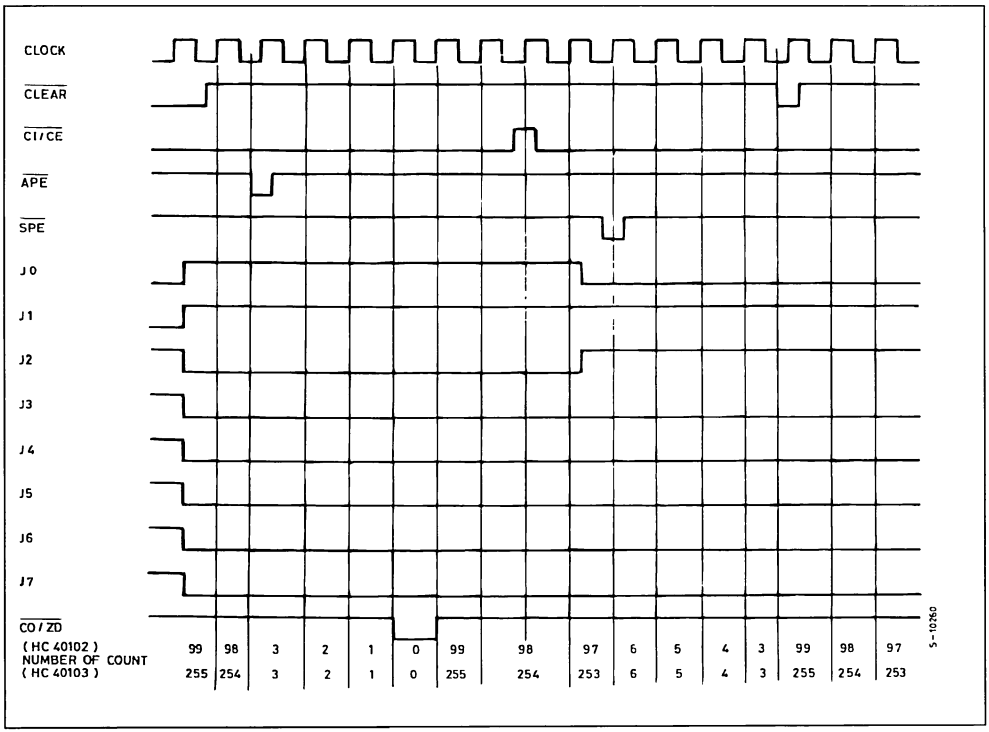
LOGIC DIAGRAM (HC40102)



LOGIC DIAGRAM (HC40103)



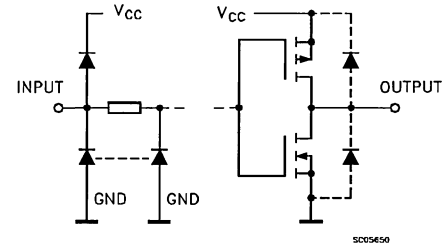
TIMING CHART



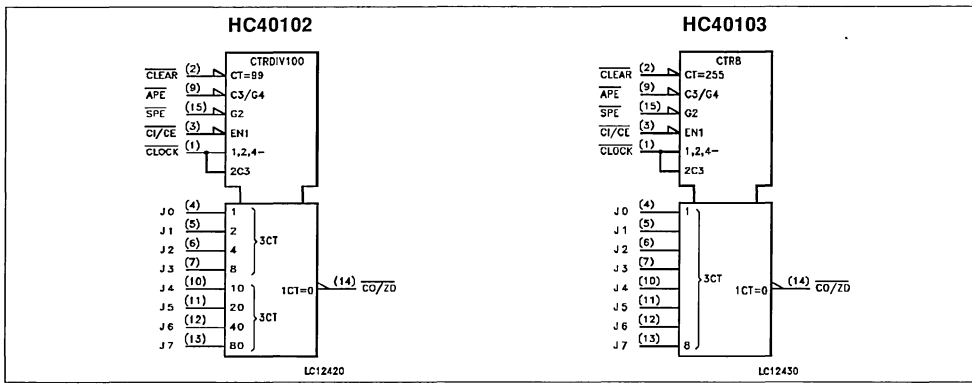
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	CLOCK	CLock Input (LOW to HIGH edge triggered)
2	$\overline{CLEAR}$	Asynchronous Master Reset Input (Active LOW)
3	$\overline{CI/CE}$	Terminal Enable Input
4, 5, 6, 7, 10, 11, 12, 13	J0 to J9	Jam Inputs
9	$\overline{APE}$	Asynchronous Preset Enable Input (Active LOW)
14	$\overline{CO/ZD}$	Terminal Count Output (Active LOW)
15	$\overline{SPE}$	Synchronous Preset Enable Input (Active LOW)
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

INPUT AND OUTPUT EQUIVALENT CIRCUIT



IEC LOGIC SYMBOLS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

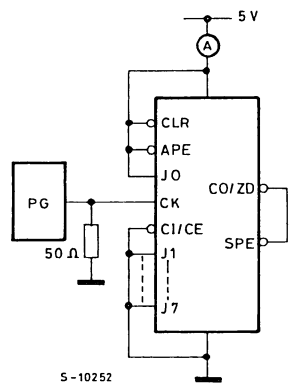
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CK - CO/ZD)	2.0			96	185		230		280	ns
		4.5			24	37		46		56	
		6.0			20	31		39		47	
t_{PLH} t_{PHL}	Propagation Delay Time (APE - CO/ZD)	2.0			116	225		280		340	ns
		4.5			29	45		56		68	
		6.0			25	38		48		57	
t_{PLH} t_{PHL}	Propagation Delay Time (CL - CO/ZD)	2.0			104	200		250		300	ns
		4.5			26	40		50		60	
		6.0			22	34		43		51	
t_{PLH} t_{PHL}	Propagation Delay Time (CI/CE - CO/ZD)	2.0			48	95		120		145	ns
		4.5			12	19		24		29	
		6.0			10	16		20		24	
f_{MAX}	Propagation Delay Time	2.0		4	8		3		2.6		pF
		4.5		20	32		16		13		
		6.0		24	38		19		15		
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				60						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

TEST CIRCUIT I_{CC} (Opr.)



INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

FUNCTIONAL DESCRIPTION

The HC40102 and HC40103 are 8-stage presettable synchronous down counters. Carry Out/Zero Detect ($\overline{CO/ZD}$) is output at the "L" level for the period of 1 bit when the readout becomes "0". The HC40102 adopts binary coded decimal notation, making setting up to 99 counts possible. While the HC40103 adopts 8-bit binary counter and can set up to 255 counts.

COUNT OPERATION

At the "H" level of control input of $\overline{CLEAR}$, $\overline{SPE}$ and $\overline{APE}$, the counter carriers out down count operation one by one at the rise of pulse given to CLOCK input. Count operation can be inhibited by setting Carry Input/Clock Enable $\overline{CI/CE}$ to the "H" level.

$\overline{CO/ZD}$ is output at the "L" level when the readout becomes "0" but is not output even if the readout becomes "0" when $\overline{CI/CE}$ is at the "H" level, thus maintaining the "H" level.

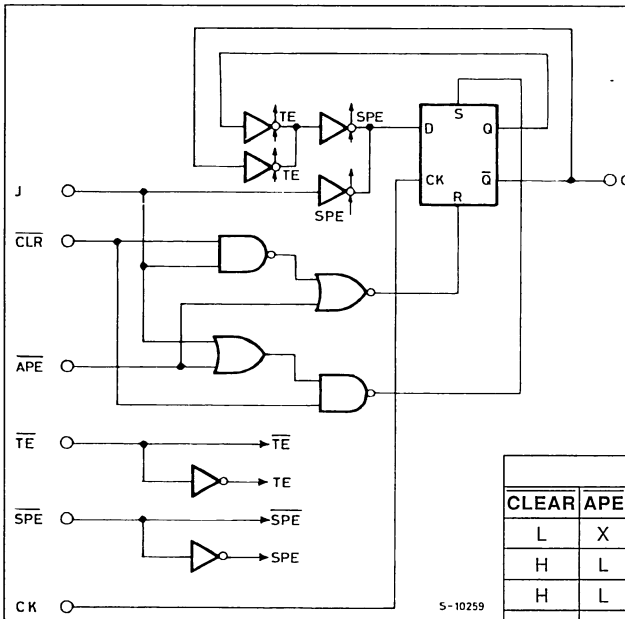
Synchronous cascade operation can be carried out by using $\overline{CI/CE}$ input and $\overline{CO/ZD}$ output.

The contents of count jump to maximum count (99 for the HC40102 and 225 for the HC40103) if clock is given when the readout is "0". Therefore, operation of 100-frequency division and that of 256-frequency division are carried out for the HC40102 and HC40103, respectively, when clock input alone is given without various kinds of preset operation.

PRESET OPERATION AND RESET OPERATION

When Clear ($\overline{CLEAR}$) input is set to the "L" level, the readout is set to the maximum count independetly of other inputs. When Asynchronous Preset Enable ($\overline{APE}$) input is set to the "L" level, readouts given on J0 to J7 can be preset asynchronously to counter independently of inputs other than $\overline{CLEAR}$ input. When Synchronous Preset Enable ($\overline{SPE}$) is set to the "L" level, the readouts given on J0 to J7 can be preset to counter synchronously with the rise of clock.

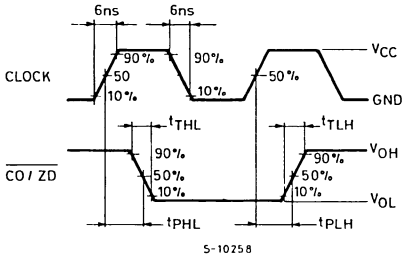
As to these operation modes, refer to the truth table.



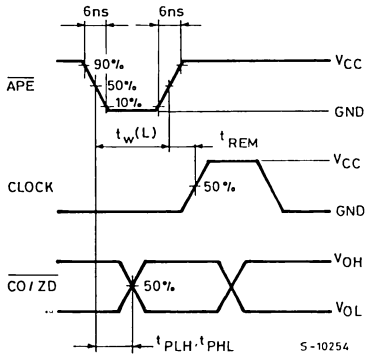
Input						Output
$\overline{CLEAR}$	$\overline{APE}$	$\overline{SPE}$	J	$\overline{TE}$	CLOCK	$\overline{Q_n + 1}$
L	X	X	X	X	X	L
H	L	X	L	X	X	L
H	L	X	H	X	X	H
H	H	L	L	X	↑	L
H	H	L	H	X	↑	H
H	H	L	X	X	↓	$\overline{Q_n}$
H	H	H	X	L	↑	Qn
H	H	H	X	H	X	$\overline{Q_n}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

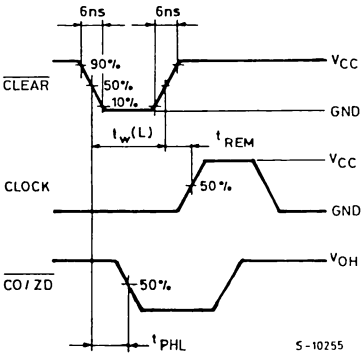
WAVEFORM 1



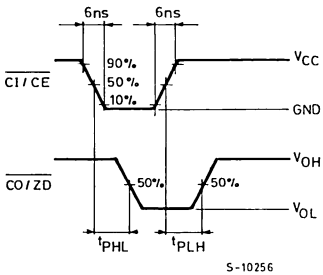
WAVEFORM 2



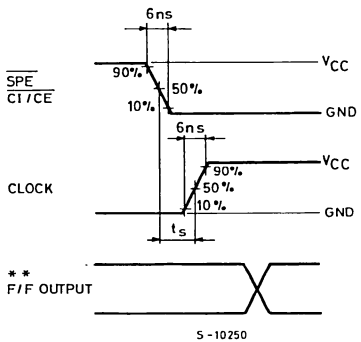
WAVEFORM 3



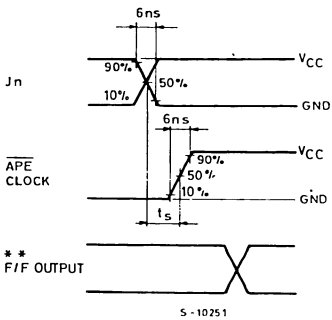
WAVEFORM 4



WAVEFORM 5



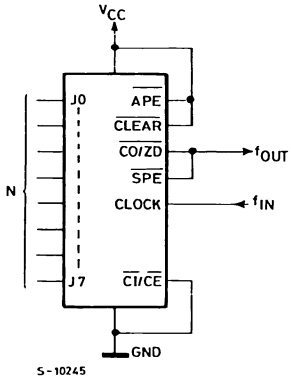
WAVEFORM 6



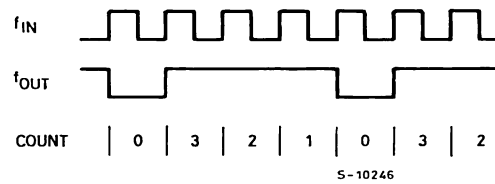
(** F/F output is internal signal of IC)

EXAMPLE OF TYPICAL APPLICATION

PROGRAMMABLE DIVIDE-BY-N COUNTER

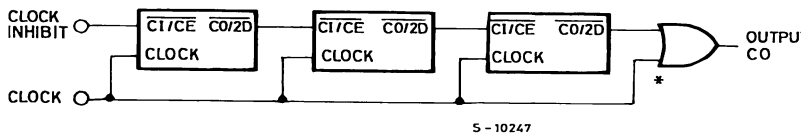


- $f_{OUT} = \frac{f_{IN}}{N+1}$
- Timing chart when N = "3" (J0, J1 = V_{CC}, J2 – J7 = GND)



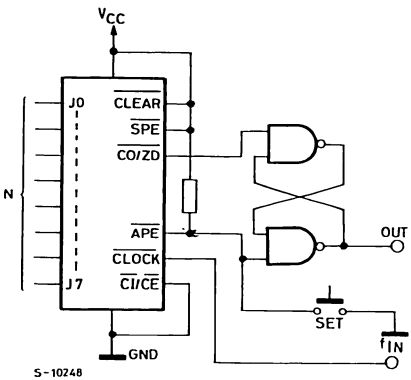
- HC40102... 1/2 to 1/100 are dividable
- HC40103... 1/2 to 1/256 are dividable

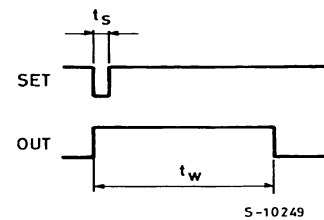
PARALLEL CARRY CASCADING



* At synchronous cascade connection, huzzerd occurs at C0 output after its second stage when digit place changes, due to delay arrival. Therefore, take gate from HC32 or the like, not from C0 output at the rear stage directly.

PROGRAMMABLE TIMER





$$t_W = \left(\frac{N}{f_{IN}} + t_S\right)$$

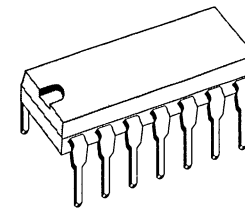
Note : The above formula does not take into account the phase of clock input. Therefore, the real pulse width is the distance between the above formula-1/fIN ~ the above formula.

PACKAGES

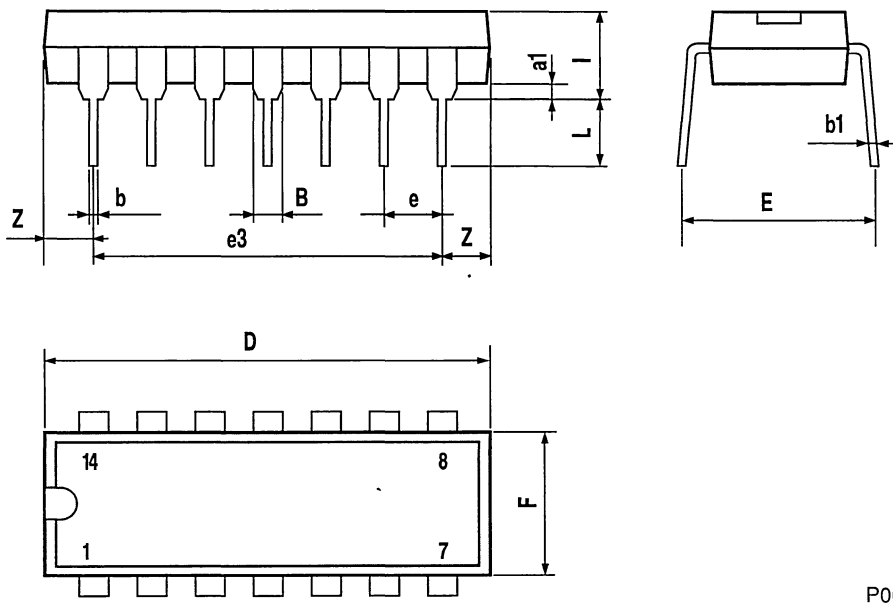
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Plastic DIP14

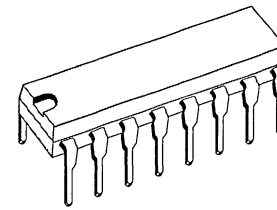


P001A

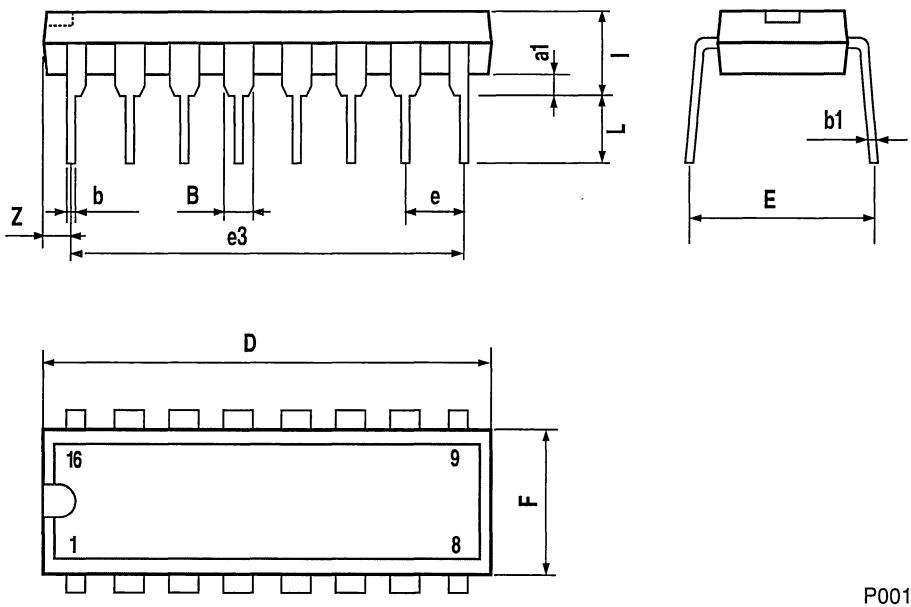
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Plastic DIP16 (0.25)

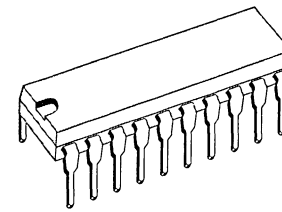


P001C

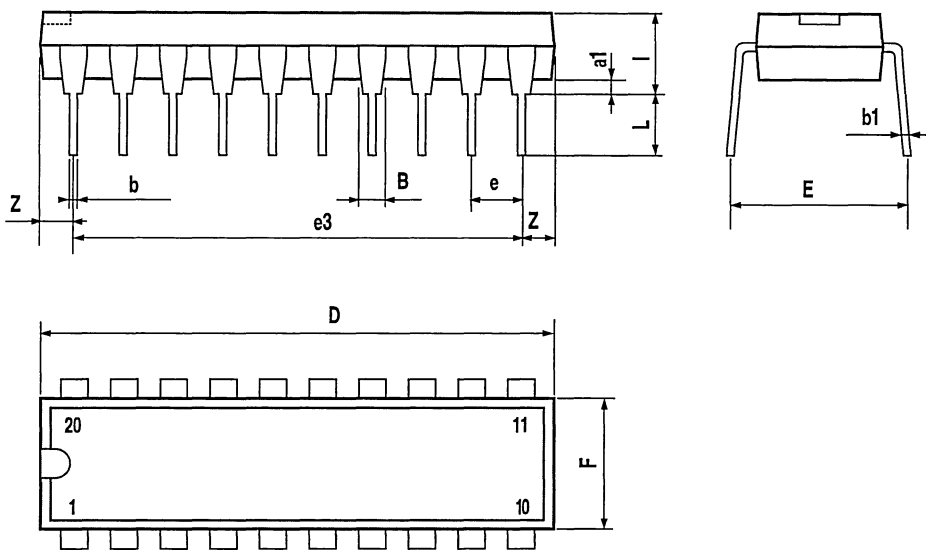
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Plastic DIP20 (0.25)

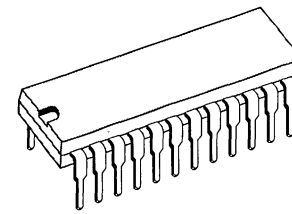


P001J

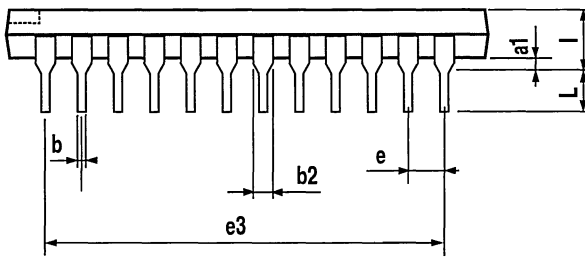
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			32.2			1.268
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		27.94			1.100	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	

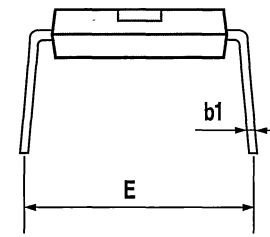
SGS-THOMSON MICROELECTRONICS

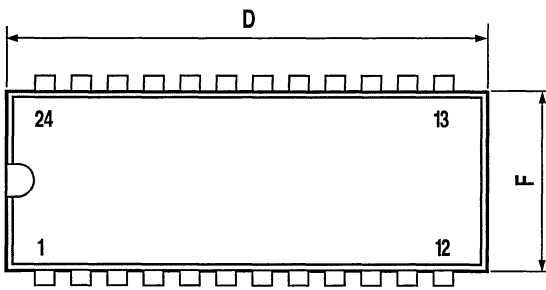
OUTLINE AND MECHANICAL DATA



Plastic DIP24 (0.25)





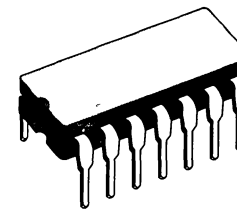


P043A

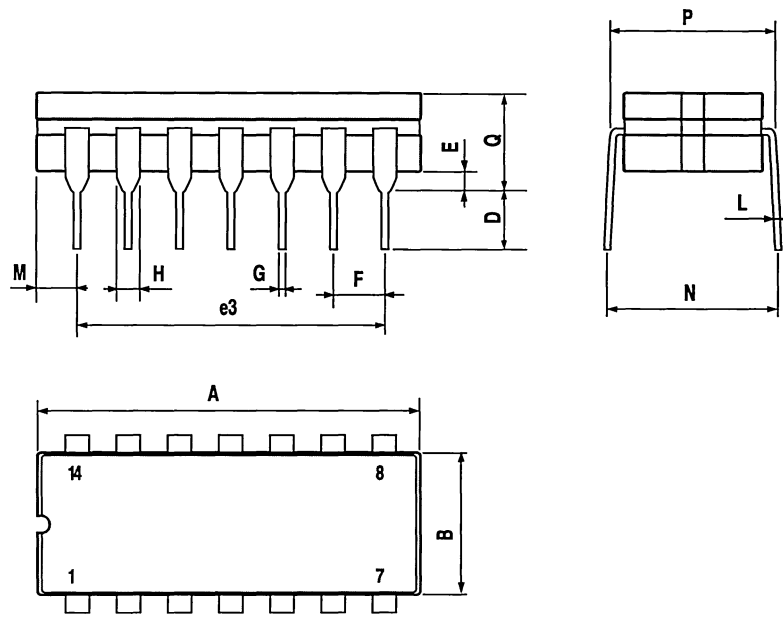
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7.0			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		15.24			0.600	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.54	0.060		0.100
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Ceramic DIP14/1

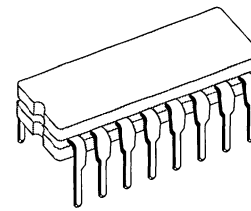


P053C

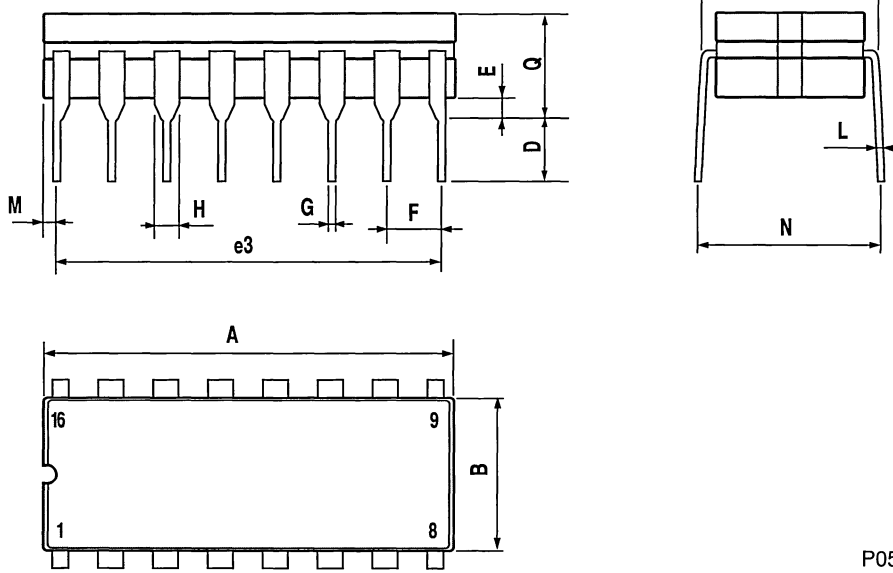
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		17.78			0.700	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Ceramic DIP16/1

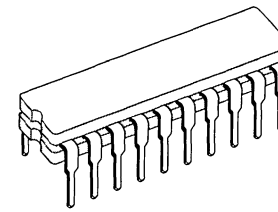


P053D

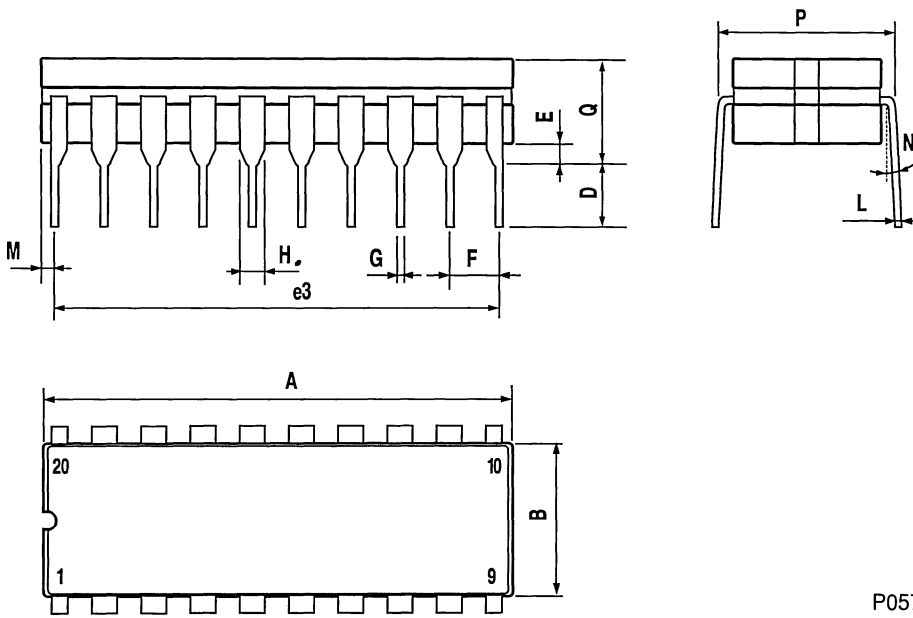
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			25			0.984
B			7.8			0.307
D		3.3			0.130	
E	0.5		1.78	0.020		0.070
e3		22.86			0.900	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
I	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N1	4° (min.), 15° (max.)					
P	7.9		8.13	0.311		0.320
Q			5.71			0.225

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Ceramic DIP20

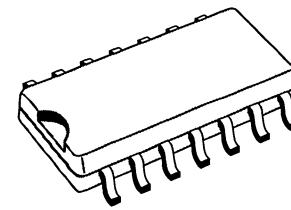


P057H

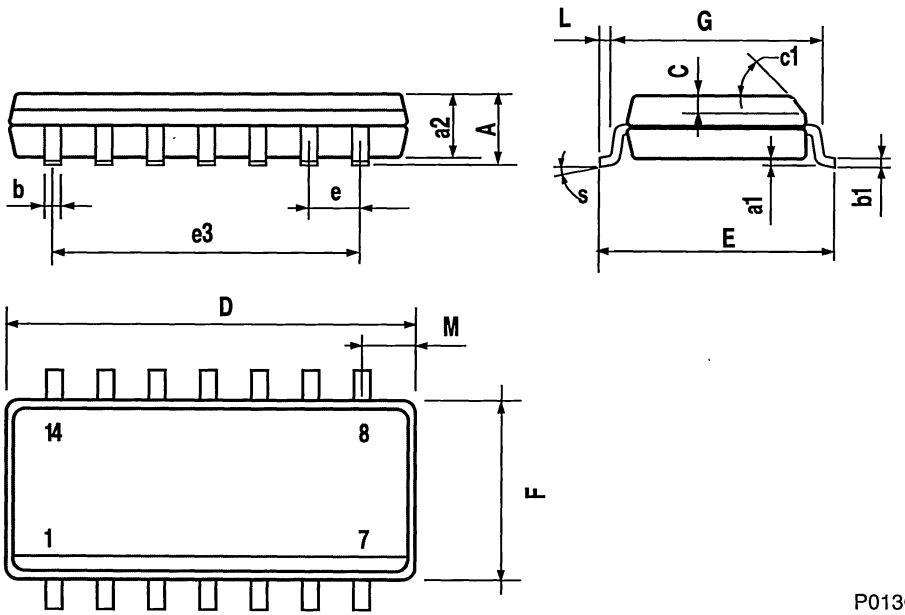
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.2	0.004		0.008
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.15		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.020		0.050
M			0.68			0.027
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



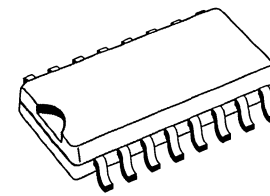
SO14



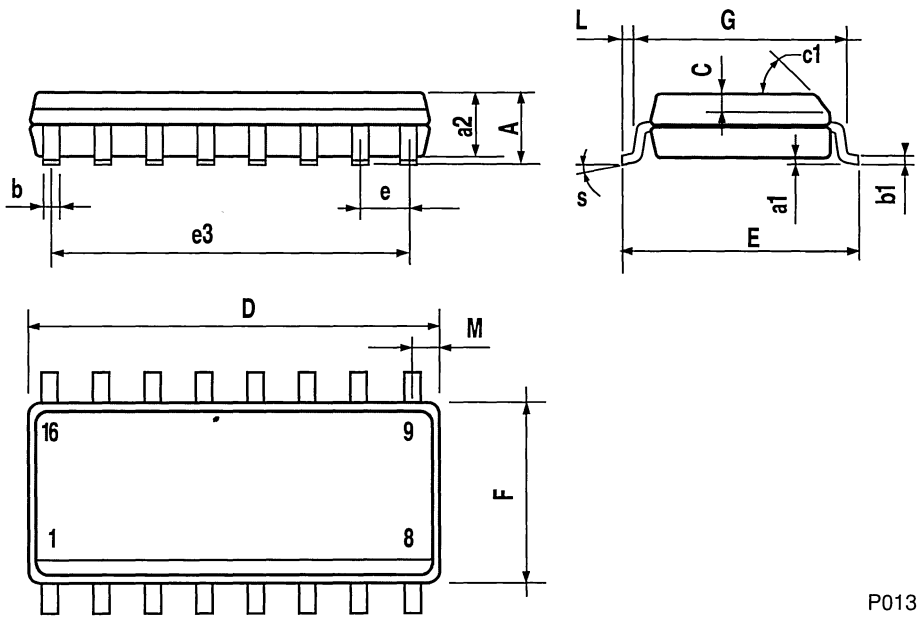
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.2	0.004		0.008
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.150		0.157
G	4.6		5.3	0.181		0.209
L	0.5		1.27	0.020		0.050
M			0.62			0.024
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO16

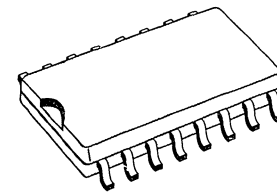


P013H

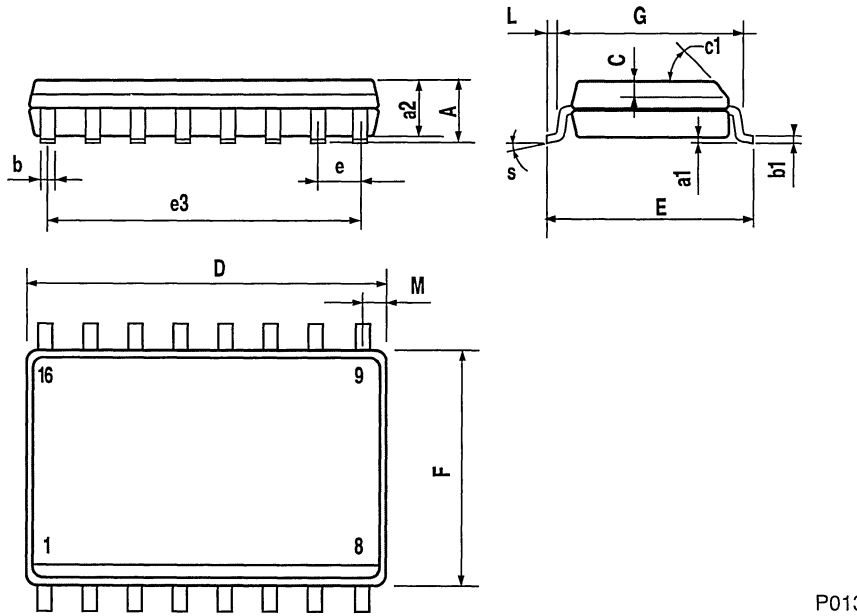
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	10.1		10.5	0.397		0.413
E	10.0		10.65	0.393		0.419
e		1.27			0.050	
e3		8.89			0.350	
F	7.4		7.6	0.291		0.300
G	8.8		9.15	0.346		0.360
L	0.5		1.27	0.020		0.050
M			0.75			0.029
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO16L

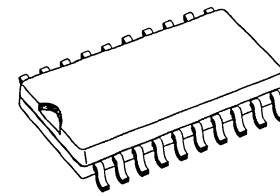


P013I

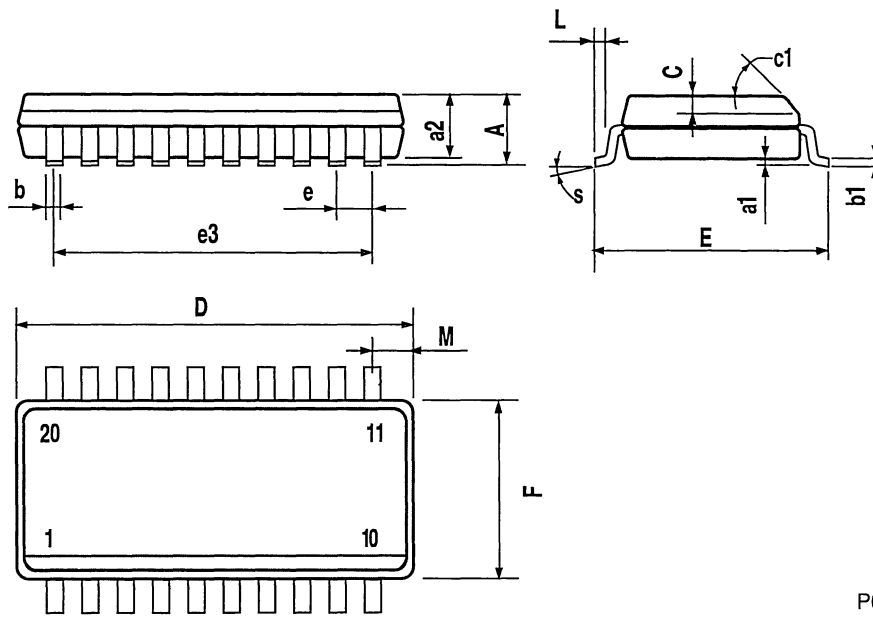
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	12.6		13.0	0.496		0.510
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.300
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO20

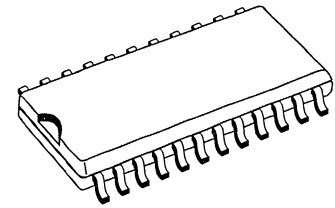


P013L

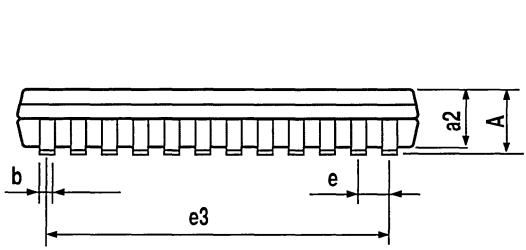
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	15.2		15.6	0.598		0.614
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		13.97			0.550	
F	7.4		7.6	0.291		0.300
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8° (max.)					

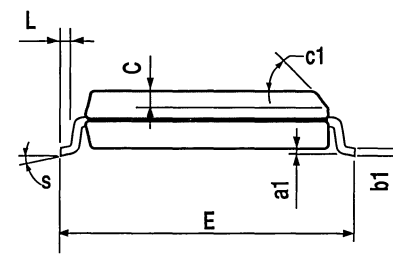
SGS-THOMSON MICROELECTRONICS

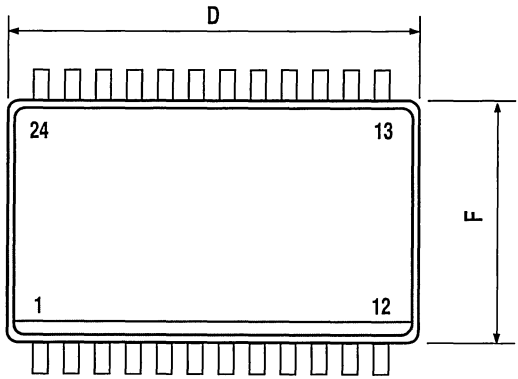
OUTLINE AND MECHANICAL DATA



SO24







EUROPE

DENMARK

2730 HERLEV
Herlev Torv, 4
Tel. (45-44) 94.85.33
Telex: 35411
Telefax. (45-44) 948694

FINLAND

LOHJA SF-08150
Ratakatu, 26
Tel (358-12) 155.11
Telefax. (358-12) 155 66

FRANCE

94253 GENTILLY Cedex
7 - avenue Gallieni - BP. 93
Tel.: (33-1) 47 40 75.75
Telex: 632570 STMHQ
Telefax. (33-1) 47.40.79.10

67000 STRASBOURG
20, Place des Halles
Tel. (33-88) 75.50.66
Telefax: (33-88) 22.29.32

GERMANY

85630 GRASBRUNN
Bretonischer Ring 4
Postfach 1122
Tel.: (49-89) 460060
Telefax: (49-89) 4605454
Teletex· 897107=STDISTR

60327 FRANKFURT
Gutleutstrasse 322
Tel. (49-69) 237492-3
Telefax. (49-69) 231957
Teletex: 6997689=STVBF

30695 HANNOVER 51
Rotenburger Strasse 28A
Tel. (49-511) 615960-3
Teletex: 5118418 CSFBEH
Telefax· (49-511) 6151243

90441 NÜRNBERG 20
Erlenstegenstrasse, 72
Tel.· (49-911) 59893-0
Telefax: (49-911) 5980701

70499 STUTTGART 31
Mittlerer Pfad 2-4
Tel. (49-711) 13968-0
Telefax: (49-711) 8661427

ITALY

20090 ASSAGO (MI)
V.le Milanofiori - Strada 4 - Palazzo A/4/A
Tel. (39-2) 57546.1 (10 linee)
Telex: 330131 - 330141 SGSAGR
Telefax: (39-2) 8250449

40033 CASALECCHIO DI RENO (BO)
Via R. Fucini, 12
Tel. (39-51) 593029
Telex. 512442
Telefax. (39-51) 591305

00161 ROMA
Via A. Torlonia, 15
Tel. (39-6) 8443341
Telex: 620653 SGSATE I
Telefax: (39-6) 8444474

NETHERLANDS

5652 AR EINDHOVEN
Meerenakkerweg 1
Tel.: (31-40) 550015
Telex: 51186
Telefax: (31-40) 528835

SPAIN

08004 BARCELONA
Calle Gran Via Corts Catalanes, 322
6th Floor, 2th Door
Tel. (34-3) 4251800
Telefax. (34-3) 4253674

28027 MADRID
Calle Albacete, 5
Tel. (34-1) 4051615
Telex: 46033 TCCEE
Telefax: (34-1) 4031134

SWEDEN

S-16421 KISTA
Borgarfjordsgatan, 13 - Box 1094
Tel.. (46-8) 7939220
Telex: 12078 THSWS
Telefax· (46-8) 7504950

SWITZERLAND

1218 GRAND-SACONNEX (GENEVA)
Chemin Francois-Lehmann, 18/A
Tel. (41-22) 7986462
Telex. 415493 STM CH
Telefax (41-22) 7984869

UNITED KINGDOM and EIRE

MARLOW, BUCKS
Planar House, Parkway
Globe Park
Tel · (44-628) 890800
Telex· 847458
Telefax (44-628) 890391

AMERICAS

BRAZIL

05413 SÃO PAULO
R Henrique Schaumann 286-CJ33
Tel (55-11) 883-5455
Telex (391)11-37988 "UMBR BR"
Telefax (55-11) 282-2367

CANADA

NEPEAN ONTARIO K2H 9C4
301 Moodie Drive Suite 307
Tel (613) 829-9944
Telefax (613) 829-8998

U.S.A.

NORTH & SOUTH AMERICAN
MARKETING HEADQUARTERS
55 Old Bedford Road
Lincoln, MA 01773
Tel (617) 259-0300
Telefax (617) 259-4421

SALES COVERAGE BY STATE

ALABAMA
Huntsville - Tel (205) 533-5995
Fax (205) 533-9320

ARIZONA
Phoenix - Tel (602) 867-6217
Fax (602) 867-6200

CALIFORNIA
Santa Ana - Tel (714) 957-6018
Fax (714) 957-3281
San Jose - Tel (408) 452-8585
Fax (452) 1549

COLORADO
Boulder - Tel (303) 449-9000
Fax (303) 449-9505

FLORIDA
Boca Raton - Tel (407) 997-7233
Fax (407) 997-7554

GEORGIA
Norcross - Tel (404) 242-7444
Fax (404) 368-9439

ILLINOIS
Schaumburg - Tel (708) 517-1890
Fax (708) 517-1899

INDIANA
Kokomo - Tel (317) 455-3500
Fax (317) 455-3400
Indianapolis - Tel (317) 575-5520
Fax (317) 575-8211

MICHIGAN
Livonia - Tel : (313) 953-1700
Fax (313) 462-4071

MINNESOTA
Bloomington - Tel (612) 944-0098
Fax (612) 944-0133

NORTH CAROLINA
Cary - Tel (919) 469-1311
Fax (919) 469-4515

NEW JERSEY
Voorhees - Tel (609) 772-6222
Fax (609) 772-6037

NEW YORK
Poughkeepsie - Tel : (914) 454-8813
Fax: (914) 454-1320

OREGON
Lake Oswego - Tel (503) 635-7650

TENNESSEE
Knoxville - Tel (615) 524-6239

TEXAS
Austin - Tel (512) 502-3020
Fax (512) 346-6260
Carrollton - Tel (214) 466-8844
Fax (214) 466-8130
Houston - Tel (713) 376-9936
Fax (713) 376-9948

FOR RF AND MICROWAVE
POWER TRANSISTORS CON-
TACT
THE FOLLOWING REGIONAL
OFFICE IN THE U.S A.

PENNSYLVANIA
Montgomeryville - Tel (215) 361-6400
Fax (215) 361-1293

ASIA / PACIFIC

AUSTRALIA

NSW 2220 HURTSVILLE
Suite 3, Level 7, Otis House
43 Bridge Street
Tel (61-2) 5803811
Telefax (61-2) 5806440

HONG KONG

WANCHAI
22nd Floor - Hopewell centre
183 Queen's Road East
Tel (852) 8615788
Telex 60955 ESGIES HX
Telefax (852) 8656589

INDIA

NEW DELHI 110019
Liaison Office
3rd Floor, F-Block
International Trade Tower
Nehru Place
Tel (91-11) 644-5928/647-9415
Telex 031-70193 STMI IN
Telefax (91-11) 6424615

MALAYSIA

SELANGOR, PETALING JAYA 46200
Unit BM-10
PJ Industrial Park
Jalan Kemajuan 12/18
Tel (03) 758 1189
Telefax (03) 758 1179

PULAU PINANG 10400
4th Floor - Suite 4-03
Bangunan FOP-123D Jalan Anson
Tel (04) 379735
Telefax (04) 379816

KOREA

SEOUL 121
8th floor Shinwon Building
823-14, Yuksam-Dong
Kang-Nam-Gu
Tel (82-2) 553-0399
Telex SGSKOR K29998
Telefax (82-2) 552-1051

SINGAPORE

SINGAPORE 2056
28 Ang Mo Kio - Industrial Park 2
Tel (65) 4821411
Telex RS 55201 ESGIES
Telefax (65) 4820240

TAIWAN

TAIPEI
11th Floor
105, Section 2 Tun Hua South Road
Tel (886-2) 755-4111
Telex 10310 ESGIE TW
Telefax (886-2) 755-4008

THAILAND

BANGKOK 10110
54 Asoke Road
Sukhumvit 21
Tel (662) 260 7870
Telefax (662) 260 7871

JAPAN

TOKYO 108
Nisseki - Takanawa Bld 4F
2-18-10 Takanawa
Minato-Ku
Tel (81-3) 3280-4121
Telefax (81-3) 3280-4131

Information furnished is believed to be accurate and reliable However, SGS-THOMSON Microelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of SGS-THOMSON Microelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. SGS-THOMSON Microelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of SGS-THOMSON Microelectronics

© 1994 SGS-THOMSON Microelectronics – Printed in Italy – All Rights Reserved

SGS-THOMSON Microelectronics GROUP OF COMPANIES
Australia - Brazil - France - Germany - Hong Kong - Italy - Japan - Korea - Malaysia - Malta - Morocco - The Netherlands - Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S A.

Recycled and chlorine free paper

Eurodis Texim Electronics B.V.
Postbus 172
7480 AD Haaksbergen
Tel.: 05427 33333
Fax: 05427 33888