TELECOM NETWORK ICs

DATABOOK

2nd EDITION

SGS-THOMSON MICROELECTRONICS

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DATABOOK

MARCH 1995

USE IN LIFE SUPPORT DEVICES OR SYSTEMS MUST BE EXPRESSLY AUTHORIZED 542

SGS-THOMSON PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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INTRODUCTION

According to market research company Dataquest, SGS-THOMSON Microelectronics is the world's leading supplier of dedicated integrated ciruits for Telecom applications. This leading position is due in large measure to the company's strength in network applications, such as central office and PABX line cards, analog & digital trunks and ISDN.

Thanks to long experience and a global customer portfolio, today SGS-THOMSON can offer solutions to suit a very wide variety of application needs, satisfying international and local standards, plus the specific needs of telecom markets throughout the world. This broad portfolio also includes solutions that provide alternative trade-offs between performance and price, and choices in the approach to system partitioning.

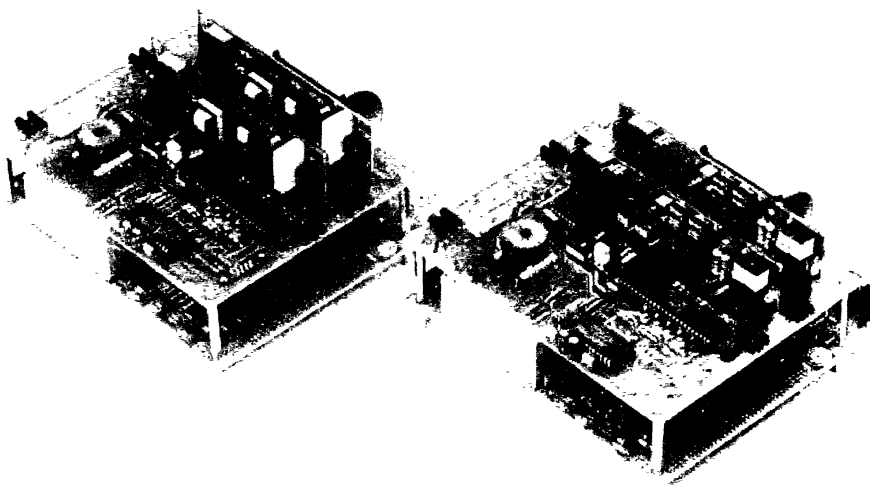
Underlying these products is the solid base of leading edge technologies, fruit of years of intensive investment in research and development. In CMOS technology SGS-THOMSON's submicron 8" capability is comparable with the leading edge technology of the industry, while in mixed bipolar-CMOS and bipolar-CMOS- DMOS the company is unmatched.

To simplify system design, SGS-THOMSON offers comprehensive application support, including evaluation boards, software, on-line assistance, courses and detailed technical documentation.

All of this reflects the importance that SGS-THOMSON Microelectronics attaches to the telecom market, a committment that guarantees continued support at the highest levels offered in the industry, and continued leadership of this key market.

In addition to dedicated products, specially designed for telecom network application, SGS-THOMSON Microelectronics manufactures many general purpose discrete semiconductors, integrated circuits and modules which are useful in this field. Datasheets for these products are included in this book.

Pair-Gain System Demo-Tool Developed by SGS-THOMSON



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ETC5064/7(-X)	Serial Interface Codec/Filter with Receive Power Amplifier	DIP20 / PLCC20 / SO20	33
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SLIC

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L3000N/L3092	SLIC Kit Optimized for applications with both First and Second Generation COMBOS	DIP28 / PLCC28 PowerSO20 / FLEXIWATT15	109
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ISDN

Device	Description	Package	Page Number
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STLC5460	Line Card Interface Controller	DIP40 / PLCC44	413
STU2071	4B3T U Interface Circuit	DIP28 / PLCC28	421

OTHER

Device	Description	Package	Page Number
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SPECIAL OP-AMPs and COMPARATORS

Device	Description	Package	Page Number
LS204	High Performance Dual Bipolar Op-Amps	DIP8 / SO8 / TO99	637
LS404	High Performance Quad Bipolar Op-Amps	DIP14 / SO14	649
TSH150	150MHz Bandwidth Bipolar Inputs Single Op-Amps	DIP8 / SO8	661
TSH151	150MHz Bandwidth MOS Inputs Single Op-Amps	DIP8 / SO8	667
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TS3V339	3V Micropower Quad Voltage Comparators	DIP14 / SO14	677
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TS3V902	Input/Output Rail to Rail Dual Op-Amps	DIP14 / SO14	701
TS3V912	Input/Output Rail to Rail Dual Op-Amps	DIP8 / SO8	709

PROTECTION DEVICES

TRISIL

I_{PP} (A)	V_{BR} (V)	Types	Case	Page
MONO FUNCTION				
100/8-20 µs	62 to 270	TPA Series	F126	607
150/8-20 µs	62 to 270	TPB Series	CB429	613
250/8-20 µs	17 to 120	LS5018B/LS5060B/LS5120B,B1	MINIDIP	523
75/10-1000 µs	200	SMTHBT200	SOD15	563
DUAL FUNCTION				
150/8-20 µs	200	THBT200S	SIP3	583
150/8-20 µs	58	THDT58S	SIP3	599
30/10-1000 µs	51 to 65	THDT51/65	SO8 / DIL8	591
TRIGGERED FUNCTION UNIDIRECTIONAL				
250/8-20 µs	255	L3100B1	MINIDIP	495
TRIGGERED FUNCTION BIDIRECTION				
250/8-20 µs	100	L3121B	SIP4	503
30/10-1000 µs	Programmable	LCP1511/12	SO8 / DIL8	515
50/10-1000 µs	Programmable	LCP150S	SIP4	509
PRIMARY PROTECTION*				
100/10-1000 µs	200 to 265	SA100 Series	Button Cell	537
100/10-1000 µs	200 to 265	SMA100 Series	SOD15	559
100/10-1000 µs	200 to 265	TPB200S/245S/265S	CB429	619
TRISIL+BRIDGE RECTIFIER*				
30/10-1000 µs	62 to 270	TSIxxxB5	SO16	631

* New

PROTECTION DEVICES (cont'd)

PROTECTION OF ISDN LINES*

I_{PP} (A)	V_{BR} (V)	V_{RM} (V)	Type	Case	Page
30/10-1000 µs	80 to 120		TPI80xxN/TPI120xxN	SO8 / DIL8	623
12/8-20 µs		18	DA108S1	SO8	489

SURFACE MOUNT TRANSIL

P_P (W)	V_{RM} (V)	Type		Case	Page
		Unidirectional	Bidirectional		
400/1 ms	5.8 to 188	SM4T..., A	–	SOD6	541
	5.8 to 188	–	SM4T...C, A	SOD6	541
600/1 ms	5.8 to 188	SM6T..., A	–	SOD6	547
	5.8 to 188	–	SM6T...C, A	SOD6	547
1500/1 ms	5.8 to 188	SM15T..., A	–	SOD15	553
	5.8 to 188	–	SM15T...C, A	SOD15	553

SURFACE MOUNT TRISIL*

I_{PP} (A)	V_{BR} (V)	Type	Case	Page
50/100-1000 µs	62 to 270	SMTPA Series	SOD6	571
90/10-1000 µs	62 to 270	SMTPB Series	SOD15	577

* New

TRANSIL

P_P (W)	V_{RM} (V)	Type		Case	Page
		Unidirectional	Bidirectional		
400/1 ms	5.8 to 376	BZW04../BZW04P..	BZW04..B/BZW04P..B	F126	475
600/1 ms	5.8 to 376	P6KE.. P,A	P6KE..CP, CA	CB417	529
1500/1 ms	5.8 to 376	1.5KE...P,A	1.5KE...CP, CA	CB429	467
5000/1 ms	10 to 180	BZW50...	BZW50...B	AG	483

DC / DC CONVERTERS

TELECOM (48 V_{DC} INPUT)

Single Output Type	Output Power (W)	Input Voltage Range (V_{DC})	Output Volt / mA (A)	Dimensions L • W • H (mm)	Page Number
GS4T48-5	4	38 to 60	5 / 50 to 800	33 • 33 • 16.5	737
GS5T48-5	5	40 to 60	5 / 50 to 1000	50.8 • 50.8 • 14.7	739
GS5T48-12	5	38 to 60	12 / 50 to 420	33 • 33 • 16.5	741
GS5T48-15	5	38 to 60	15 / 50 to 330	33 • 33 • 16.5	743
GS15T48-5	15	40 to 60	5 / 3000	50.8 • 50.8 • 14.7	745
GS24T48-12	24	36 to 72	12 / 2000	50.8 • 50.8 • 12.5	747
GS25T48-5	25	36 to 72	5 / 5000	116 • 65 • 21.1	749
GS30T48-5	30	36 to 72	5 / 50 to 6000	50.8 • 50.8 • 12.5	753
GS30T48-12	30	36 to 72	12 / 2500	116 • 65 • 21.1	749
GS30T48-15	30	36 to 72	15 / 2000	116 • 65 • 21.1	749
GS120T48-3.3	120	38 to 60	3.35 / 35 A	125 • 66.5 • 19	765
GS175T48-5	175	38 to 60	5.075 / 35 A	125 • 66.5 • 19	765
GS175T48-12	175	38 to 60	12 / 15 A	125 • 66.5 • 19	765
GS175T48-15	175	38 to 60	15 / 12 A	125 • 66.5 • 19	765
GS300T48-5	300	38 to 60	5.075 / 60 A	125 • 66.5 • 20	775
Double Output Type	**Output Power (W)**	**Input Voltage Range (V_{DC})**	**Output Volt / mA**	**Dimensions L • W • H (mm)**	**Page Number**
GS2T48-D12	2	38 to 60	± 12 / 100	50 • 38 • 19	735

ISDN

Type Number	Output Power (W)	Input Voltage Range (V_{DC})	Output Volt / mA	Dimensions L • W • H (mm)	Page Number
GS1T70-D540	1	25 to 99	5 / 2 to 90 40 / 10.5	50.8 • 50.8 • 18	727
GS1T70-D540F	1	25 to 115	5 / 2 to 90 40 / 10.5	56 • 56 • 18	731

HIGH INPUT VOLTAGE (UL AND TUV APPROVED)

Type Number	Output Power (W)	Input Voltage Range (V_{DC})	Output Volt (*) / A	Dimensions L • W • H (mm)	Page Number
GS100T300-48	100	200 to 400	48.0 / 2.0	50.8 • 101.6 • 20	755

(*) Output voltage can be adjusted from about 1/2 V_{out} to 1.1 V_{out}. See data sheet for more details

SWITCHING VOLTAGE REGULATORS

Type Number	Description	Dimensions L • W • H (mm)	Page Number
GS-R4840N	40V / 1 A Negative Output Regulator	85.5 • 67.0 • 21.3	781
GS-R4840NV	Digital Adjust. 0.6 A / -22 to -60V Negative Output Regulator	109 • 65 • 21	783

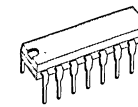
DEDICATED ICs
DATASHEETS

SGS-THOMSON MICROELECTRONICS

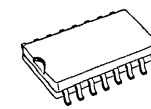
ETC5054/54-X
ETC5057/57-X

SERIAL INTERFACE CODEC/FILTER

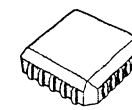
- COMPLETE CODEC AND FILTERING SYSTEM (DEVICE) INCLUDING:
  - Transmit high-pass and low-pass filtering.
  - Receive low-pass filter with sin x/x correction.
  - Active RC noise filters
  - μ-law or A-law compatible COder and DECoder.
  - Internal precision voltage reference.
  - Serial I/O interface.
  - Internal auto-zero circuitry.
- A-LAW 16 PINS (ETC5057FN, 20 PINS)
- μ-LAW WITHOUT SIGNALING, 16 PINS (ETC5054FN, 20 PINS)
- MEETS OR EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS
- ±5V OPERATION
- LOW OPERATING POWER - TYPICALLY 60 mW
- POWER-DOWN STANDBY MODE - TYPICALLY 3 mW
- AUTOMATIC POWER-DOWN
- TTL OR CMOS COMPATIBLE DIGITAL INTERFACES
- MAXIMIZES LINE INTERFACE CARD CIRCUIT DENSITY
- 0 to 70°C OPERATION: ETC5057/54
- –40 to +85°C OPERATION: ETC5057-X/54-X



DIP16 (Plastic)
ORDERING NUMBERS:
ETC5057N
ETC5054N
ETC5057N-X
ETC5054N-X



SO16 (Wide)
ORDERING NUMBERS:
ETC5057D
ETC5054D
ETC5057D-X
ETC5054D-X

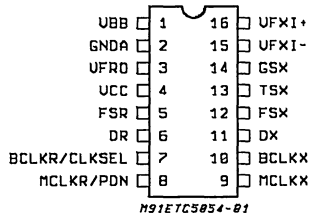


PLCC20
ORDERING NUMBERS:
ETC5057FN
ETC5054FN
ETC5057FN-X
ETC5054FN-X

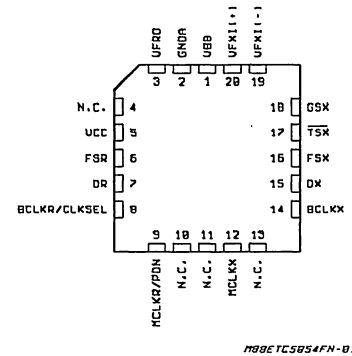
DESCRIPTION

The ETC5057/ETC5054 family consists of A-law and μ–law monolithic PCM CODEC/filters utilizing the A/D and D/A conversion architecture shown in the block diagram below, and a serial PCM interface. The devices are fabricated using double-poly CMOS process. The encode portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded A-law or μ–law PCM format. The decode portion of each device consists of an expanding decoder, which reconstructs the analog signal from the companded A-law or μ–law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz and is followed by a single-ended power amplifier capable of driving low impedance loads. The devices require 1.536 MHz, 1.544 MHz, or 2.048 MHz transmit and receive master clocks, which may be asynchronous, transmit and receive bit clocks which may vary from 64 kHz to 2.048 MHz, and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.

PIN CONNECTIONS (Top view)

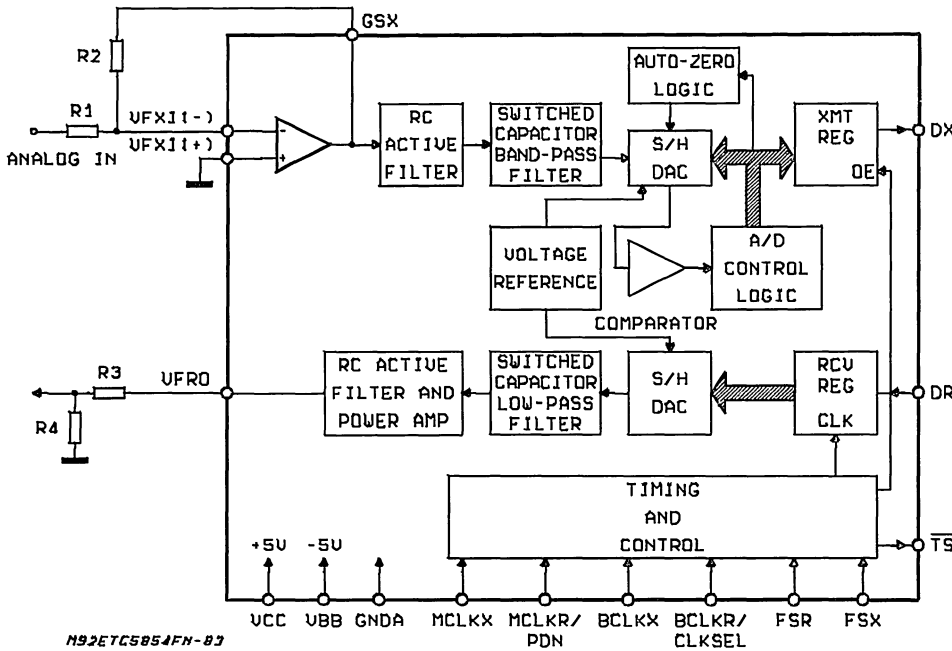


DIP and SO



PLCC

BLOCK DIAGRAM



PIN DESCRIPTION

Name	Pin Type *	N° DIP and SO	N° PLCC (**)	Function	Description
V_{BB}	S	1	1	Negative Power Supply	$V_{BB} = -5\ V \pm 5\ \%$.
GNDA	GND	2	2	Analog Ground	All signals are referenced to this pin.
VF_RO	O	3	3	Receive Filter Output	Analog Output of the Receive Filter
V_{CC}	S	4	5	Positive Power Supply	$V_{CC} = +5\ V \pm 5\ \%$.
FS_R	I	5	6	Receive Frame Sync Pulse	Enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8kHz pulse train. See figures 1, 2 and 3 for timing details.
D_R	I	6	7	Receive Data Input	PCM data is shifted into D_R following the FS_R leading edge.
$BCLK_R$/CLKSEL	I	7	8	Shift-in Clock	Shifts data into D_R after the FS_R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see table 1). This input has an internal pull-up.
$MCLK_R$/PDN	I	8	9	Receive Master Clock	Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
$MCLK_X$	I	9	12	Transmit Master Clock	Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$.
$BCLK_X$	I	10	14	Shift-out Clock	Shifts out the PCM data on DX. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
D_X	O	11	15	Transmit Data Output	The TRI-STATE® PCM data output which is enabled by FS_X.
FS_X	I	12	16	Transmit Frame Sync Pulse	Enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8 kHz pulse train. See figures 1, 2 and 3 for timing details.
$\overline{TS_X}$	O	13	17	Transmit Time Slot	Open drain output which pulses low during the encoder time slot. Recommended to be grounded if not used.
GS_X	O	14	18	Gain Set	Analog output of the transmit input amplifier. Used to set gain externally.
VF_XI^-	I	15	19	Inverting Amplifier Input	Inverting Input of the Transmit Input Amplifier.
VF_XI^+	I	16	20	Non-inverting Amplifier Input	Non-inverting Input of the Transmit Input Amplifier.

(*) I: Input, O: Output, S: Power Supply
(**) Pins 4,10,11 and 13 are not connected
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FUNCTIONAL DESCRIPTION

POWER-UP

When power is first applied, power-on reset circuitry initializes the device and places it into the power-down mode. All non-essential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin and FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high ; the alternative is to hold both FS_X and FS_R inputs continuously low. The device will power-down approximately 2 ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R$/CKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. With a fixed level on the $BCLK_R$/CLKSEL pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R$/CLKSEL. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With and FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or $BCLK_R$ if running). FS_X and FS_R must be synchronous with $MCLK_{X/R}$.

Table 1: Selection of Master Clock Frequencies.

$BCLK_R$/CLKSEL	Master Clock Frequency Selected	
	ETC5057/57-X	ETC5054/54-X
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or open circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied, $MCLK_X$ and $MCLK_R$ must be 2.048 MHz for the ETC5057, or 1.536 MHz, 1.544 MHz for the ETC5054, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see pin description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in table 1 are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64 kHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The device can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R, must be one bit clock period long, with timing relationships specified in figure 2. With FS_X high during a falling edge of $BCLK_X$ the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. Both devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in figure 3. Based on the transmit frame sync, FS_X, the device will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns (see fig. 1). The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising

edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, which-ever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$ ($BCLK_X$ in synchronous mode). Both devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see figure 6. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unitygain filter consisting of RD active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to A-law (ETC5057) or μ–law (ETC5054) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5V peak (see table of transmission characteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 μs (due to the transmit filter) plus 125μs (due to encoding delay), which totals 290μs. Any offset vol-tage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (ETC5057) or μ–law (ETC5054) and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample and hold. The filter is then followed by a 2nd order RC active post-filter and power amplifier capable of driving a 600Ω load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10μs later the decoder DAC output is updated. The total decoder delay is ~ 10μs (decoder update) plus 110μs (filter delay) plus 62.5μs (1/2 frame), which gives approximately 180μs. A mute circuitry is a active during 10ms when power up.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GNDA	7	V
V_{BB}	V_{BB} to GNDA	– 7	V
V_{IN}, V_{OUT}	Voltage at any Analog Input or Output	V_{CC} + 0.3 to V_{BB} – 0.3	V
	Voltage at Any Digital Input or Output	V_{CC} + 0.3 to GNDA – 0.3	V
T_{oper}	Operating Temperature Range: for **ETC5054/57** for **ETC5054-X/57-X**	– 25 to + 125 – 40 to + 125	°C °C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
	Lead Temperature (soldering, 10 seconds)	300	°C

ELECTRICAL OPERATING CHARACTERISTICS V_{CC} = 5.0 V ± 5 %, V_{BB} = – 5.0 V ± 5%GNDA = 0 V, T_A = 0 °C to 70 °C (ETC5054-X/57-X T_A = -40°C to +85°C); Typical Characteristics Specified at V_{CC} = 5.0 V, V_{BB} = – 5.0 V, T_A = 25 °C ; all signals are referenced to GNDA.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage			0.6	V
V_{IH}	Input High Voltage	2.2			V
V_{OL}	Output Low Voltage I_L = 3.2mA D_X I_L = 3.2mA, Open Drain TS_X			 0.4 0.4	 V V
V_{OH}	Output High Voltage I_H = 3.2mA D_X	 2.4			 V
I_{IL}	Input Low Current (GNDA ≤ V_{IN} ≤ V_{IL}, all digital inputs)	–10		10	μA
I_{IH}	Input High Current (V_{IH} ≤ V_{IN} ≤ V_{CC}) except $BCLK_R$/BCLKSEL	–10		10	μA
I_{OZ}	Output Current in HIGH Impedance State (TRI-STATE) (GNDA ≤ V_O ≤ V_{CC}) D_X	 –10		 10	 μA

ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_IXA	Input Leakage Current (VF_XI^+ or VF_XI^-) ($-2.5V \le V \le +2.5V$)	– 200		200	nA
R_IXA	Input Resistance (VF_XI^+ or VF_XI^-) ($-2.5V \le V \le +2.5V$)	10			MΩ
R_OXA	Output Resistance (closed loop, unity gain)		1	3	Ω
R_LXA	Load Resistance (GS_X)	10			kΩ
C_LXA	Load Capacitance (GS_X)			50	pF
V_OXA	Output Dynamic Range ($R_L \ge 10K\Omega$) (GS_X)	±2.8			V
AV_XA	Voltage Gain (VF_XI^+ to GS_X)	5000			V/V
F_UXA	Unity Gain Bandwidth	1	2		MHz
$V_{OS}XA$	Offset Voltage	– 20		20	mV
$V_{CM}XA$	Common-mode Voltage	– 2.5		2.5	V
CMRRXA	Common-mode Rejection Ratio	60			dB
PSRRXA	Power Supply Rejection Ratio	60			dB

ANALOG INTERFACE WITH RECEIVE FILTER (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
R_ORF	Output Resistance (VF_RO)		1	3	Ω
R_LRF	Load Resistance ($VF_RO = \pm 2.5V$)	600			Ω
C_LRF	Load Capacitance			500	pF
VOS_RO	Output DC Offset Voltage	– 200		200	mV

POWER DISSIPATION (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}0$	Power-down Current for **ETC5054/57** **ETC5054-X/57-X**		0.5 0.5	1.5	mA mA
$I_{BB}0$	Power-down Current for **ETC5054/57** **ETC5054-X/57-X**		0.05 0.05	0.3 0.4	mA mA
$I_{CC}1$	Active Current for **ETC5054/57** **ETC5054-X/57-X**		6.0 6.0	9.0 11	mA mA
$I_{BB}1$	Active Current for **ETC5054/57** **ETC5054-X/57-X**		6.0 6.0	9.0 11	mA mA

TIMING SPECIFICATIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
$1/t_{PM}$	Frequency of master clocks Depends on the device used and the $BCLK_R$/CLKSEL Pin $MCLK_X$ and $MCLK_R$		1.536 1.544 2.048		MHz MHz MHz
t_{WMH}	Width of Master Clock High $MCLK_X$ and $MCLK_R$	160			ns
t_{WML}	Width of Master Clock Low $MCLK_X$ and $MCLK_R$	160			ns
t_{RM}	Rise Time of Master Clock $MCLK_X$ and $MCLK_R$			50	ns
t_{FM}	Fall Time of Master Clock $MCLK_X$ and $MCLK_R$			50	ns
t_{PB}	Period of Bit Clock	485	488	15.725	ns
t_{WBH}	Width of Bit Clock High (V_{IH} = 2.2V)	160			ns
t_{WBL}	Width of Bit Clock Low (V_{IL} = 0.6V)	160			ns
t_{RB}	Rise Time of Bit Clock (t_{PB} = 488ns)			50	ns
t_{FB}	Fall Time of Bit Clock (t_{PB} = 488ns)			50	ns
t_{SBFM}	Set-up time from $BCLK_X$ high to $MCLK_X$ falling edge. (first bit clock after the leading edge of FS_X)	100			ns
t_{HBF}	Holding Time from Bit Clock Low to the Frame Sync (long frame only)	0			ns
t_{SFB}	Set-up Time from Frame Sync to Bit Clock (long frame only)	80			ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock FS_X or FS_R Low to Frame Sync (long frame only)	100			ns
t_{DZF}	Delay time to valid data from FS_X or $BCLK_X$, whichever comes later and delay time from FS_X to data output disabled. (C_L = 0pF to 150pF)	20		165	ns
t_{DBD}	Delay time from $BCLK_X$ high to data valid. (load = 150pF plus 2 LSTTL loads)	0		180	ns
t_{DZC}	Delay time from $BCLK_X$ low to data output disabled.	50		165	ns
t_{SDB}	Set-up time from D_R valid to $BCLK_{R/X}$ low.	50			ns
t_{HBD}	Hold time from $BCLK_{R/X}$ low to D_R invalid.	50			ns
t_{HOLD}	Holding Time from Bit Clock High to Frame Sync (short frame only)	0			ns
t_{SF}	Set-up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low (short frame sync pulse) - Note 1	80			ns
t_{HF}	Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low (short frame sync pulse) - Note 1	100			ns
t_{XDP}	Delay Time to TS_Xlow (load = 150pF plus 2 LSTTL loads)			140	ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (low level) 64kbit/s operating mode)	160			ns

Note 1: For short frame sync timing FS_X and FS_R must go high while their respective bit clocks are high.

Figure 1: 64kbits/s TIMING DIAGRAM (see next page for complete timing).

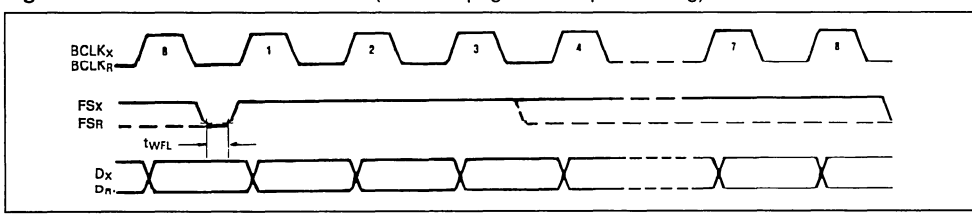


Figure 2: Short Frame Sync Timing

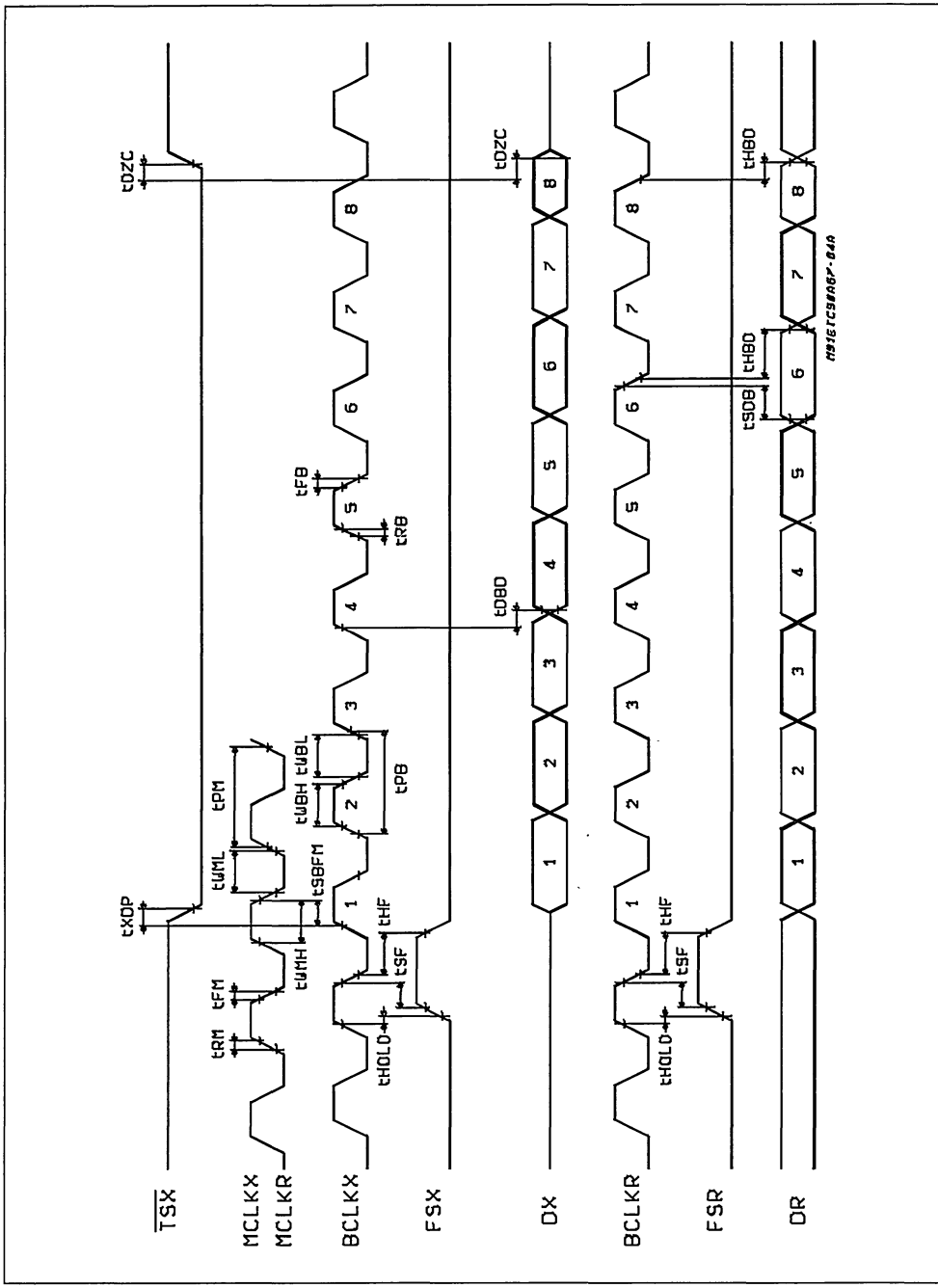
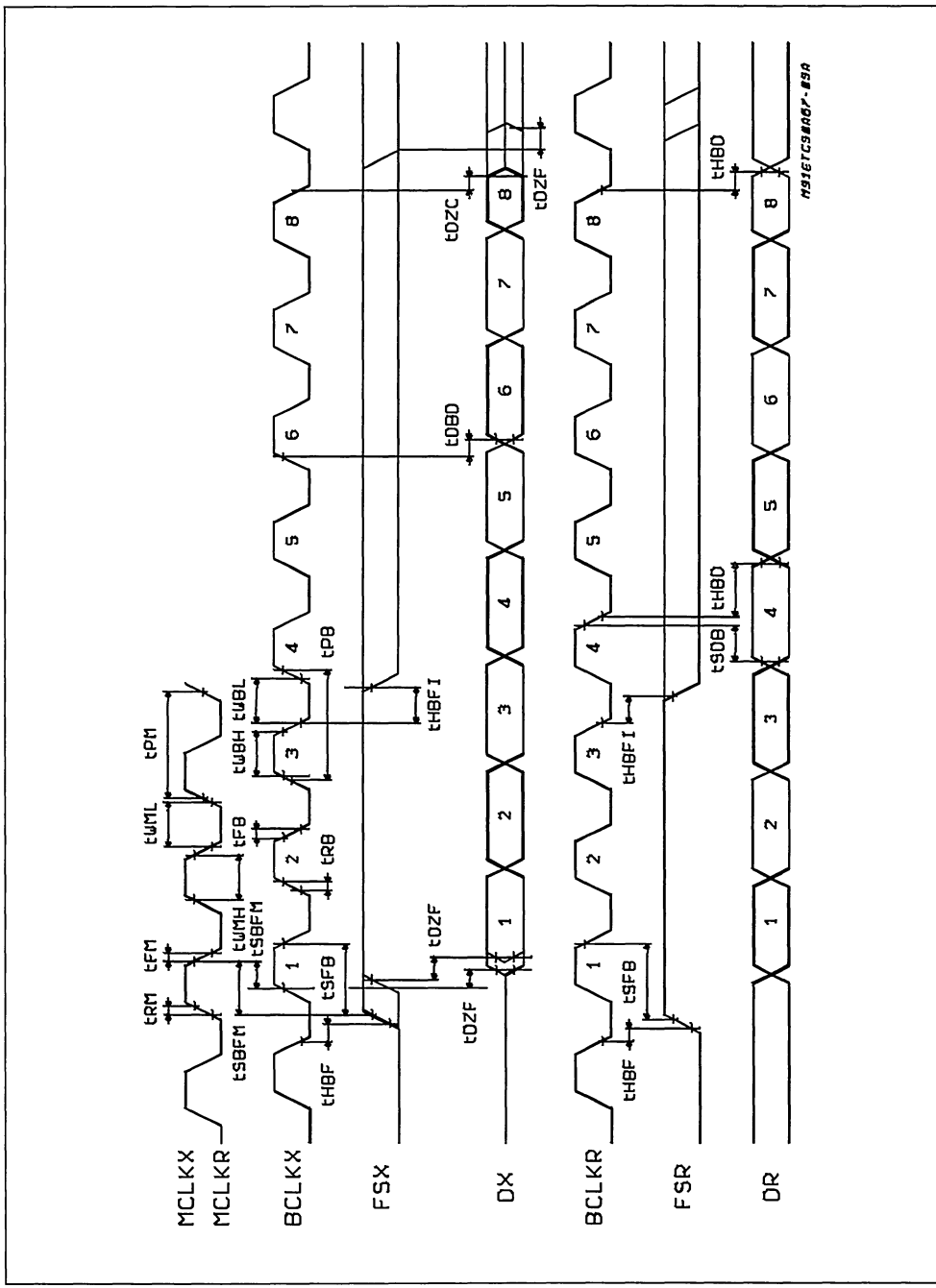


Figure 3: Long Frame Sync Timing



TRANSMISSION CHARACTERISTICS

T_A = 0 to 70°C (ETC5054-X/57-X T_A = -40°C to +85°C), V_{CC} = +5V ±5%, V_{BB} = –5V ±5%, GNDA = 0V, f = 1.0KHz, V_{IN} = 0dBm0 transmit input amplifier connected for unity-gain non-inverting (unless otherwise specified).

AMPLITUDE RESPONSE

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Absolute levels - nominal 0 dBm0 level is 4 dBm (600 Ω) 0 dBm0		1.2276		Vrms
t_{MAX}	Max Overload Level 3.14 dBm0 (A LAW) 3.17 dBm0 (U LAW)		 2.492 2.501		 V_{PK} V_{PK}
G_{XA}	Transmit Gain, Absolute (TA = 25 °C, V_{CC} = 5 V, V_{BB} = – 5 V) Input at GS_X = 0 dBm0 at 1020 Hz	– 0.15		0.15	dB
G_{XR}	Transmit Gain, Relative to GXA f = 16 Hz f = 50 Hz f = 60 Hz f = 180 Hz f = 200 Hz f = 300 Hz - 3000 Hz f = 3200Hz (ETC5054-X/57-X) f = 3300 Hz f = 3400 Hz f = 4000 Hz f = 4600 Hz and up, Measure Response from 0 Hz to 4000 Hz	 – 2.8 – 1.8 – 0.15 – 0.35 – 0.35 – 0.7		 – 40 – 30 – 26 – 0.2 – 0.1 0.15 0.20 0.05 0 – 14 – 32	 dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature TA = 0 to +70°C T_A = –40 to +85°C (ETC5054-X/57-X)	 – 0.1 –0.15		 0.1 0.15	 dB dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage (V_{CC} = 5 V ± 5 %, V_{BB} = – 5 V ± 5 %)	– 0.05		0.05	dB
G_{XRL}	Transmit Gain Variations with Level Sinusoidal Test Method Reference Level = – 10 dBm0 VFXI+ = – 40 dBm0 to + 3 dBm0 VF_XI+ = – 50 dBm0 to – 40 dBm0 VF_XI+ = – 55 dBm0 to – 50 dBm0	 – 0.2 – 0.4 – 1.2		 0.2 0.4 1.2	 dB dB dB
G_{RA}	Receive Gain, Absolute (T_A = 25°C, V_{CC} = 5V, V_{BB} = –5V) Input = Digital Code Sequence for 0dBm0 Signal at 1020Hz	– 0.15		0.15	dB
G_{RR}	Receive Gain, Relative to GRA f = 0Hz to 3000Hz f = 3200Hz (ETC5054-X/57-X) f = 3300Hz f = 3400Hz f = 4000Hz	 – 0.15 – 0.35 – 0.35 – 0.7		 0.15 0.20 0.05 0 – 14	 dB dB dB dB dB
G_{RAT}	Absolute Transmit Gain Variation with Temperature T_A = 0 to +70°C T_A = –40 to +85°C (ETC5054-X/57-X)	 – 0.1 –0.15		 0.1 0.15	 dB dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage (V_{CC} = 5 V ± 5 %, V_{BB} = – 5 V ± 5 %)	– 0.05		0.05	dB
G_{RRL}	Receive Gain Variations with Level Sinusoidal Test Method; Reference input PCM code corresponds to an ideally encoded – 10 dBm0 signal PCM level = – 40 dBm0 to + 3 dBm0 PCM level = – 50 dBm0 to – 40 dBm0 PCM level = – 55 dBm0 to – 50 dBm0	 – 0.2 – 0.4 – 1.2		 0.2 0.4 1.2	 dB dB dB
V_{RO}	Receive Output Drive Level (R_L = 600Ω)	– 2.5		2.5	V

TRANSMISSION (continued)

ENVELOPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Min.	Typ.	Max.	Unit
D_{XA}	Transmit Delay, Absolute (f = 1600Hz)		290	315	µs
D_{XR}	Transmit Delay, Relative to D_{XA}				
	f = 500Hz - 600Hz		195	220	
	f = 600Hz - 800Hz		120	145	
	f = 800Hz - 1000Hz		50	75	µs
	f = 1000Hz - 1600Hz		20	40	
	f = 1600Hz - 2600Hz		55	75	
	f = 2600Hz - 2800Hz		80	105	
	f = 2800Hz - 3000Hz		130	155	
D_{RA}	Receive Delay, Absolute (f = 1600Hz)		180	200	µs
D_{RR}	Receive Delay, Relative to D_{RA}				
	f = 500Hz - 1000Hz	– 40	– 25		
	f = 1000Hz - 1600Hz	– 30	– 20		µs
	f = 1600Hz - 2600Hz		70	90	
	f = 2600Hz - 2800Hz		100	125	
	f = 2800Hz - 3000Hz		145	175	

NOISE

Symbol	Parameter	Min.	Typ.	Max.	Unit
N_{XP}	Transmit Noise, P Message Weighted (A LAW, $VFXI^+$ = 0 V) 1)				
	ETC5057		– 74	– 69	dBm0p
	ETC5057-X		– 74	– 67	dBm0p
N_{RP}	Receive Noise, P Message Weighted (A LAW, PCM code equals positive zero)		– 82	– 79	dBm0p
N_{XC}	Transmit Noise, C Message Weighted µ LAW ($VFXI^+$ = 0 V)				
	ETC5054		12	15	dBmC0
	ETC5054-X		12	16	dBmC0
N_{RC}	Receive Noise, C Message Weighted (µ LAW, PCM Code Equals Alternating Positive and Negative Zero)		8	11	dBmC0
N_{RS}	Noise, Single Frequency f = 0 kHz to 100 kHz, Loop around Measurement, $VFXI^+$ = 0 Vrms			– 53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit (note 2) V_{CC} = 5.0 V_{DC} + 100 mVrms, f = 0 kHz-50 kHz	40			dBp
$NPSR_X$	Negative Power Supply Rejection, Transmit (note 2) V_{BB} = – 5.0 V_{DC} + 100 mVrms, f = 0 kHz-50 kHz	40			dBp
$PPSR_R$	Positive Power Supply Rejection, Receive (PCM code equals positive zero, V_{CC} = 5.0 VD_C + 100mVrms)				
	f = 0Hz to 4000Hz	40			dBp
	f = 4KHz to 25KHz	40			dB
	f = 25KHz to 50KHz	36			dB
$NPSR_R$	Negative Power Supply Rejection, Receive (PCM code equals positive zero, VBB = 5.0 VD_C + 100mVrms)				
	f = 0Hz to 4000Hz	40			dBp
	f = 4KHz to 25KHz	40			dB
	f = 25KHz to 50KHz	36			dB

TRANSMISSION CHARACTERISTICS (continued)

NOISE (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SOS	Spurius out-of-band Signals at the Channel Output Loop around measurement, 0dBm0, 300Hz - 3400Hz input applied to DR, measure individual image signals at DX 4600Hz - 7600Hz 7600Hz - 8400Hz 8400Hz - 100,000Hz			 – 32 – 40 – 32	 dB dB dB

DISTORTION

Symbol	Parameter		Min.	Typ.	Max.	Unit
STD_X or STD_R	Signal to Total Distortion (sinusoidal test method) Transmit or Receive Half-channel					
	Level = 3.0dBm0		33			
	Level = 0dBm0 to –30dBm0		36			
	Level = –40dBm0	XMT	29			dBp
		RCV	30			
	Level = –55dBm0	XMT	14			
		RCV	15			
SFD_X	Single Frequency Distortion, Transmit (T_A = 25°C)				–46	dB
SFD_R	Single Frequency Distortion, Receive (T_A = 25°C)				–46	dB
IMD	Intermodulation Distortion Loop Around Measurement, VFXI+ = –4dBm0 to –21dBm0, two Frequencies in the Range 300Hz - 3400Hz				–41	dB

CROSSTALK

Symbol	Parameter	Min.	Typ.	Max.	Unit
CT_{X-R}	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level f = 300Hz to 3400Hz, D_R = Steady PCM Mode for **ETC5054/57** **ETC5054-X/57-X**		– 90	– 75 – 65	dB dB
CT_{R-X}	Receive to Transmit Crosstalk, 0 dBm0 Receive Level f = 300Hz to 3400Hz, (note 2) for **ETC5054/57** **ETC5054-X/57-X**		– 90	– 70 – 65	dB dB

Notes:
1) Measured by extrapolation from distortion test results.
2) $PPSR_X$, $NPSR_X$, CT_{R-X} is measured with a –50dBm0 activating signal applied at $VFXI^+$.

ENCODING FORMAT AT D_X OUTPUT

	A-Law (including even bit inversion)								μLaw							
V_{IN} (at GS_X) = +Full-scale	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0
V_{IN} (at GS_X) = 0V	1 0	1 1	0 0	1 1	0 0	1 1	0 0	1 1	1 0	1 1	1 1	1 1	1 1	1 1	1 1	1 1
V_{IN} (at GS_X) = – Full-scale	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0

APPLICATION INFORMATION

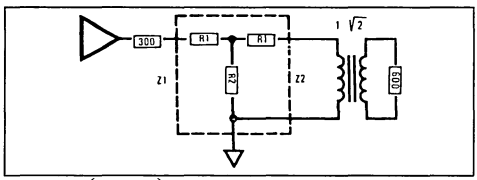
POWER SUPPLIES

While the pins at the ETC505X family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any-other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1µF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB} as close to the device as possible.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10µF capacitors.

Figure 4: T-PAD Attenuator



$$R1 = Z1\left(\frac{N^2+1}{N^2-1}\right) - 2\sqrt{Z1 \cdot Z2}\left(\frac{N}{N^2-1}\right)$$

$$R2 = 2\sqrt{Z1.Z2}\left(\frac{N}{N^2-1}\right)$$

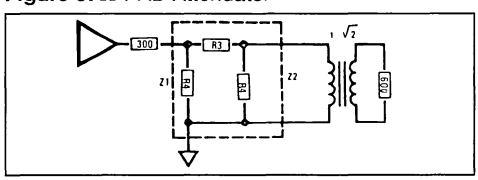
Where: $N = \sqrt{\frac{POWERIN}{POWEROUT}}$

and: $S = \sqrt{\frac{Z1}{Z2}}$

Also : $Z = \sqrt{Z_{SC} \cdot Z_{OC}}$

Where Z_{SC} = impedance with short circuit termination and Z_{OC} = impedance with open circuit termination.

Figure 5: Π-PAD Attenuator



$$R3 = \sqrt{\frac{Z1 \cdot Z2}{2}}\left(\frac{N^2-1}{N}\right)$$

$$R3 = Z1\left(\frac{N^2-1}{N^2-2NS+1}\right)$$

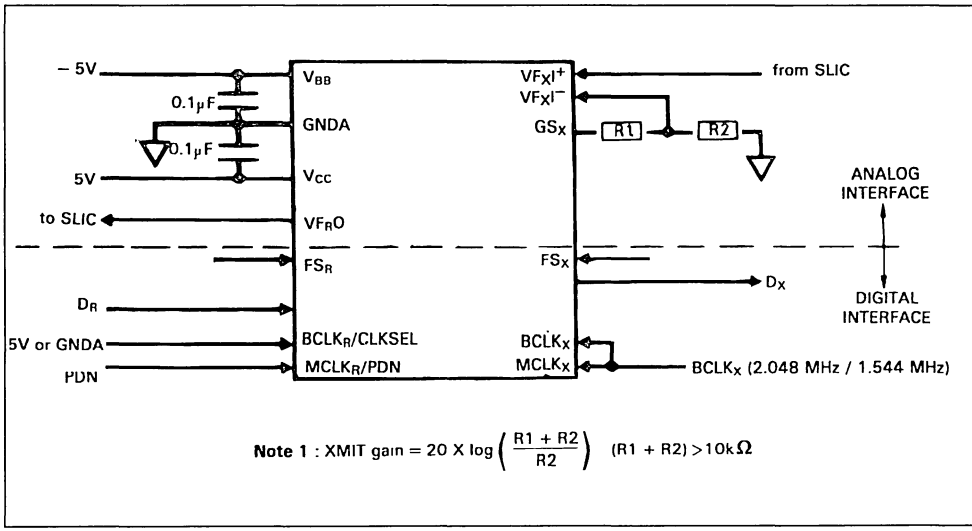
RECEIVE GAIN ADJUSTMENT

For applications where a ETC505X family CODEC/filter receive output must drive a 600Ω load, but a peak swing lower then ± 2.5V is required, the receive gain can be easily adjusted by inserting a matched T-pad or π –pad at the output. Table II lists the required resistor values for 600Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest pratical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30dB return loss against 600Ω is obtained if the output impedance of the attenuator is in the range 282Ω to 319Ω (assuming a perfect transformer).

Table 2 : Attenuator Tables For Z1 = Z2 = 300 Ω (all values in Ω).

dB	R1	R2	R3	R4
0.1	1.7	26k	3.5	52k
0.2	3.5	13k	6.9	26k
0.3	5.2	8.7k	10.4	17.4k
0.4	6.9	6.5k	13.8	13k
0.5	8.5	5.2k	17.3	10.5k
0.6	10.4	4.4k	21.3	8.7k
0.7	12.1	3.7k	24.2	7.5k
0.8	13.8	3.3k	27.7	6.5k
0.9	15.5	2.9k	31.1	5.8k
1.0	17.3	2.6k	34.6	5.2k
2	34.4	1.3k	70	2.6k
3	51.3	850	107	1.8k
4	68	650	144	1.3k
5	84	494	183	1.1k
6	100	402	224	900
7	115	380	269	785
8	129	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17k	386
20	246	61	1.5k	366

Figure 6: Typical Synchronous Application.



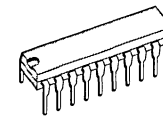
Note 1 : XMIT gain = 20 X log $\left(\frac{R1 + R2}{R2}\right)$ (R1 + R2) >10kΩ

SGS-THOMSON MICROELECTRONICS

ETC5064/64-X
ETC5067/67-X

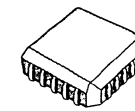
SERIAL INTERFACE CODEC/FILTER WITH RECEIVE POWER AMPLIFIER

- COMPLETE CODEC AND FILTERING SYSTEM INCLUDING :
  - Transmit high-pass and low-pass filtering.
  - Receive low-pass filter with sin x/x correction.
  - Active RC noise filter.
  - μ-law or A-law compatible CODER and DECODER.
  - Internal precision voltage reference.
  - Serial I/O interface.
  - Internal auto-zero circuitry.
  - Receive push-pull power amplifiers.
- μ-LAW ETC5064
- A-LAW ETC5067
- MEETS OR EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS.
- ± 5 V OPERATION.
- LOW OPERATING POWER-TYPICALLY 70 mW
- POWER-DOWN STANDBY MODE-TYPICALLY 3 mW
- AUTOMATIC POWER DOWN
- TTL OR CMOS COMPATIBLE DIGITAL INTERFACES
- MAXIMIZES LINE INTERFACE CARD CIRCUIT DENSITY
- 0°C TO 70°C OPERATION: ETC5064/67
- –40°C TO 85°C OPERATION: ETC5064-X/67-X



DIP20
(Plastic) N

ORDERING NUMBERS:
ETC5064N
ETC5064N-X
ETC5067N
ETC5067N-X



PLCC20
FN

ORDERING NUMBERS:
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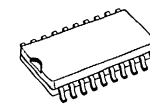
ETC5064FN-X
ETC5067FN
ETC5067FN-X



SO20
D

ORDERING NUMBERS:
ETC5064D
ETC5064D-X
ETC5067D
ETC5067D-X

DESCRIPTION

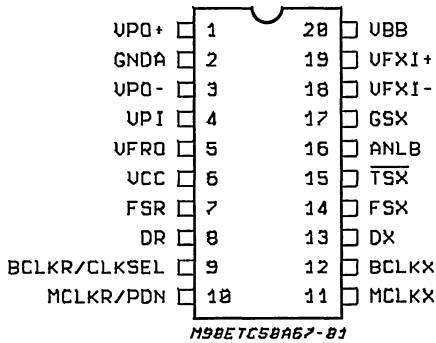
The ETC5064 (μ-law), ETC5067 (A-law) are monolithic PCM CODEC/FILTERS utilizing the A/D and D/A conversion architecture shown in the Block Diagrams and a serial PCM interface. The devices are fabricated using double-poly CMOS process.

Similar to the ETC505X family, these devices feature an additional Receive Power Amplifier to provide push-pull balanced output drive capability. The receive gain can be adjusted by means of two external resistors for an output level of up to ± 6.6 V across a balanced 600Ω load.

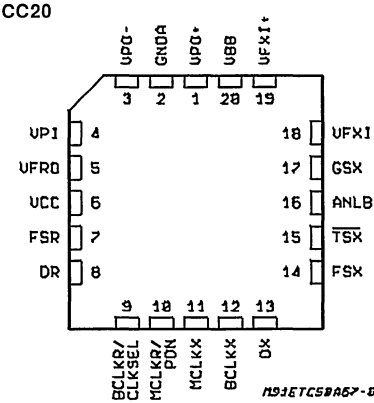
Also included is an Analog Loopback switch and $\overline{TS}_X$ output.

PIN CONNECTIONS (Top views)

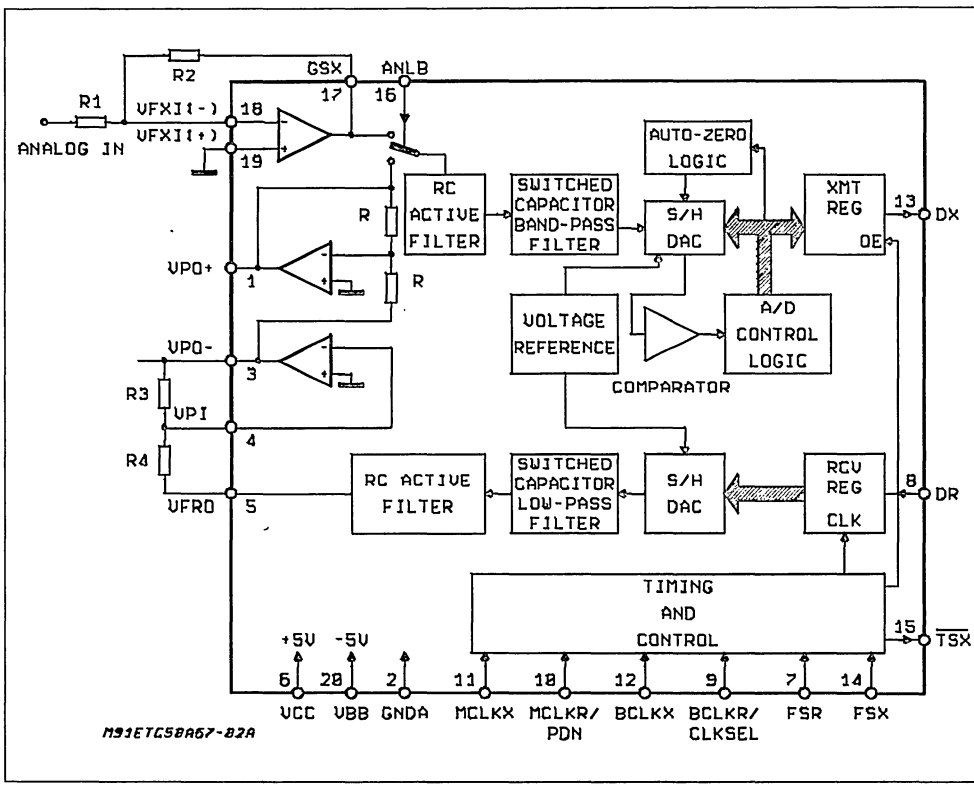
DIP20 & SO20



PLCC20



BLOCK DIAGRAM (ETC5064 - ETC5064-X - ETC5067 - ETC5067-X)



PIN DESCRIPTION

Name	Pin Type (*)	N	Description
VPO^+	O	1	The Non-inverting Output of the Receive Power Amplifier
GNDA	GND	2	Analog Ground. All signals are referenced to this pin.
VPO^-	O	3	The Inverting Output of the Receive Power Amplifier
VPI	I	4	Inverting Input to the Receive Power Amplifier. Also powers down both amplifiers when connected to V_{BB}.
VF_RO	O	5	Analog Output of the Receive Filter.
V_{CC}	S	6	Positive Power Supply Pin. V_{CC} = +5V ±5%
FS_R	I	7	Receive Frame Sync Pulse which enable $BCLK_R$ to shift PCM data into D_R. FS_R is an 8KHz pulse train. See figures 1 and 2 for timing details.
D_R	I	8	Receive Data Input. PCM data is shifted into D_R following the FS_R leading edge
$BCLK_R$/CLKSEL	I	9	The bit Clock which shifts data into D_R after the FS_R leading edge. May vary from 64KHz to 2.048MHz. Alternatively, may be a logic input which selects either 1.536MHz/1.544MHz or 2.048MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see table 1). This input has an internal pull-up.
$MCKL_R$/PDN	I	10	Receive Master Clock. Must be 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
$MCLK_X$	I	11	Transmit Master Clock. Must be 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with $MCLK_R$.
$BCLK_X$	I	12	The bit clock which shifts out the PCM data on D_X. May vary from 64KHz to 2.048MHz, but must be synchronous with $MCLK_X$.
D_X	O	13	The TRI-STATE®PCM data output which is enabled by FS_X.
FS_X	I	14	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8KHz pulse train. See figures 1 and 2 for timing details.
$\overline{TS_X}$	O	15	Open drain output which pulses low during the encoder time slot. Must to be grounded if not used.
ANLB	I	16	Analog Loopback Control Input. Must be set to logic '0' for normal operation. When pulled to logic '1', the transmit filter input is disconnected from the output of the transmit preamplifier and connected to the VPO^+ output of the receive power amplifier.
GS_X	O	17	Analog output of the transmit input amplifier. Used to set gain externally.
$VFxI^-$	I	18	Inverting input of the transmit input amplifier.
$VFxI^+$	I	19	Non-inverting input of the transmit input amplifier.
V_{BB}	S	20	Negative Power Supply Pin. V_{BB} = -5V ±5%

(*) I: Input, O: Output, S: Power Supply.
TRI-STATE® is a trademark of National Semiconductor Corp.

FUNCTIONAL DESCRIPTION

POWER-UP

When power is first applied, power-on reset circuitry initializes the device and places it into the power-down mode. All non-essential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin and FS_X and/or FS_R pulses must be present. Thus 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high; the alternative is to hold both FS_X and FS_R inputs continuously low. The device will power-down approximately 2 ms after the last FS_X pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, MCLKX will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the BCL_R/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193 rd clock pulse each frame.

With a fixed level on the $BCLK_R$/CKSEL pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R$/CLKSEL. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

Table 1: Selection of Master Clock Frequencies.

BCLKR/CLKSEL	Master Clock Frequency Selected	
	ETC5067 ETC5067-X	ETC5064 ETC5064-X
Clocked	2.048MHz	1.536MHz or 1.544MHz
0	1.536MHz or 1.544MHz	2.048MHz
1 (or open circuit)	2.048MHz	1.536MHz or 1.544MHz

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shift out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRISTATE D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or on $BCKL_R$ if running). FS_X and FS_R must be synchronous with MCLKX/R.

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 2.048 MHz for the ETC5067 or 1.536 MHz, 1.544 MHz for the ETC5064, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see pin description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in Table 1 are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64kHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The device can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses. FS_X and FS_R, must be one bit clock period long, with timing relationships specified in figure 2. With FS_X high during a falling edge of $BCLK_R$, the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. Both devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in figure 3. Based on the transmit frame sync FS_X, the device will sense whether short or long frame sync

pulses are being used. For 64 kHz operation, the frame sync pulses must be kept low for a minimum of 160 ns (see Fig 1). The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$ ($BCLK_x$ in synchronous mode). Both devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see figure 4. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to A-law (ETC5067 and ETC5067-X) or μ-law (ETC5064 and ETC5064-X) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input over load (t_{MAX}) of nominally 2.5V peak (see table of Transmission Characteristics). The FS_X frame sync pulse controls the sampling of the filer output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. the total encoding delay will be approximately 165 μs (due to the transmit filter) plus 125μs (due to encoding delay), which totals 290μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consist of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256kHz. The decoder is A-law (ETC5067 and ETC5067-X) or μ–law (ETC5064 and ETC5064-X) and the 5 th order low pass filter corrects for the sin x/x attenuation due to the 8kHz sample and hold. The filter is then followed by a 2 nd order RC active post-filter and power amplifier capable of driving a 600Ω load to a level of 7.2dBm. The receive section is unity-gain. Upon the occurence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCKL_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10μs later the decoder DAC output is updated. The total decoder delay is about10μs (decoder up-date) plus 110μs (filter delay) plus 62.5μs (1/2 frame), which gives approximately 180μs.

RECEIVE POWER AMPLIFIERS

Two inverting mode power amplifiers are provided for directly driving a matched line interface transformer. The gain of the first power amplifier can be adjusted to boost the ± 2.5V peak output signal from the receive filter up ± 3.3V peak into an unbalanced 300Ω load, or ±4.0V into an unbalanced 15kΩ load. The second power amplifier is internally connected in unity-gain inverting mode to give 6dB of signal gain for balanced loads. Maximum power transfer to a 600Ω subscriber line termination is obtained by differentially driving a balanced transformer with a $\sqrt{2}$: 1 turns ratio, as shown in figure 4. A total peak power of 15.6dBm can be delivered to the load plus termination. Both power amplifier can be powered down independently from the PDN input by connecting the VPI input to V_{BB} saving approximately 12 mW of power.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GNDA	7	V
V_{BB}	V_{BB} to GNDA	-7	V
V_{IN}, V_{OUT}	Voltage at any Analog Input or Output	V_{CC} +0.3 to V_{BB} -0.3	V
	Voltage at any Digital Input or Output	V_{CC} +0.3 to GNDA -0.3	V
T_{oper}	Operating Temperature Range: **ETC5064/67** **ETC5064-X/67-X**	-25 to +125 -40 to +125	°C °C
T_{stg}	Storage Temperature Range	-65 to +150	°C
	Lead Temperature (soldering, 10 seconds)	300	°C

ELECTRICAL OPERATING CHARACTERISTICS

V_{CC} = 5.0V ±5%, V_{BB} = -5V ±5%, GNDA = 0V, T_A = 0°C to 70°C (ETC5064-X/67-X: T_A = –40°C to 85°), unless otherwise noted; typical characteristics specified at V_{CC} = 5.0V, V_{BB} =-5.0V, T_A = 25°C; all signals are referenced to GNDA.

DIGITAL INTERFACE (All devices)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage					
	I_L = 3.2 mA	D_X			0.4	V
	I_L = 3.2 mA, Open Drain	$\overline{TS_X}$			0.4	V
V_{OH}	Output High Voltage					
	IH = 3.2 mA	D_X	2.4			V
I_{IL}	Input Low Current (GNDA ≤ V_{IN} ≤ V_{IL})all digital inputs Except $BCLK_R$		– 10		10	µA
I_{IH}	Input High Current (V_{IH} ≤ V_{IN} ≤ V_{CC}) Except ANLB		– 10		10	µA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)					
	(GNDA ≤ V_O ≤ V_{CC})	D_X	– 10		10	µA

ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (all devices)

Symbol	Parameter		Min.	Typ.	Max.	Unit
I_IXA	Input Leakage Current (– 2.5 V ≤ V ≤ + 2.5 V)	$VFxI^+$ or $VFxI^-$	– 200		200	nA
R_IXA	Input Resistance (– 2.5 V ≤ V ≤ + 2.5 V)	VF_XI^+ or VF_XI^-	10			MΩ
R_OXA	Output Resistance (closed loop, unity gain)			1	3	Ω
R_LXA	Load Resistance	GS_X	10			kΩ
C_LXA	Load Capacitance	GS_X			50	pF
V_OXA	Output Dynamic Range (R_L ≥ 10 kΩ)	GS_X	– 2.8		+2.8	V
A_VXA	Voltage Gain ($VFxI^+$ to GS_X)		5000			V/V
F_UXA	Unity Gain Bandwidth		1	2		MHz
$V_{OS}XA$	Offset Voltage		– 20		20	mV
$V_{CM}XA$	Common-mode Voltage		– 2.5		2.5	V
CMRRXA	Common-mode Rejection Ratio		60			dB
PSRRXA	Power Supply Rejection Ratio		60			dB

ANALOG INTERFACE WITH RECEIVE FILTER (all devices)

Symbol	Parameter		Min.	Typ.	Max.	Unit
R_ORF	Output Resistance	VF_RO		1	3	Ω
R_LRF	Load Resistance (VF_RO = ± 2.5 V)		10			kΩ
C_LRF	Load Capacitance				25	pF
VOS_RO	Output DC Offset Voltage		– 200		200	mV

ELECTRICAL OPERATING CHARACTERISTICS (Continued)

ANALOG INTERFACE WITH POWER AMPLIFIERS (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
IPI	Input Leakage Current (– 1.0 V ≤ VPI ≤ 1.0 V)	– 100		100	nA
RIPI	Input Resistance (– 1.0 ≤ VPI ≤ 1.0 V)	10			MΩ
VIOS	Input Offset Voltage	– 25		25	mV
ROP	Output Resistance (inverting unity–gain at VPO^+ or VPO^-)		1		Ω
Fc	Unity–gain Bandwidth, Open Loop (VPO^-)		400		kHz
C_LP	Load Capacitance (VPO^+ or VPO^- to GNDA) $R_L \geq 1500\ \Omega$ $R_L = 600\ \Omega$ $R_L = 300\ \Omega$			 100 500 1000	pF
GAp^+	Gain VPO^- to VPO^+ to GNDA, Level at VPO^- = 1. 77 Vrms (+ 3 dBmO)		– 1		V/V
PSRRp	Power Supply Rejection of V_{CC} or V_{BB} (VPO^- connected to VPI) 0 kHz – 4 kHz 0 kHz – 50 kHz	 60 36			dB

POWER DISSIPATION (all devices)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}0$	Power-down Current at **ETC6064/67** **ETC5064-X/67-X**		0.5 0.5	1.5	mA mA
$I_{BB}0$	Power-down Current at **ETC6064/67** **ETC5064-X/67-X**		0.05 0.05	0.3 0.4	mA mA
$I_{CC}1$	Active Current at **ETC6064/67** **ETC5064-X/67-X**		7.0 7.0	10.0 12.0	mA mA
$I_{BB}1$	Active Current at **ETC6064/67** **ETC5064-X/67-X**		7.0 7.0	10.0 12.0	mA mA

All TIMING SPECIFICATIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
$1/t_{PM}$	Frequency of master clocks $MCLK_X$ and $MCLK_R$ Depends on the device used and the $BCLK_R$/CLKSEL Pin		1.536 2.048 1.544		MHz
t_{WMH}	Width of Master Clock High $MCLK_X$ and $MCLK_R$	160			ns
t_{WML}	Width of Master Clock Low $MCLK_X$ and $MCLK_R$	160			ns
t_{RM}	Rise Time of Master Clock $MCLK_X$ and $MCLK_R$			50	ns
t_{FM}	Fall Time of Master Clock $MCLK_X$ and $MCLK_R$			50	ns
t_{PB}	Period of Bit Clock	485	488	15.725	ns
t_{WBH}	Width of Bit Clock High (V_{IH} = 2.2 V)	160			ns
t_{WBL}	Width of Bit Clock Low (V_{IL} = 0.6 V)	160			ns
t_{RB}	Rise Time of Bit Clock (t_{PB} = 488 ns)			50	ns
t_{FB}	Fall Time of Bit Clock (t_{PB} = 488 ns)			50	ns
t_{SBFM}	Set-up time from $BCLK_X$ high to $MCLK_X$ falling edge. (first bit clock after the leading edge of FS_X)	100			ns
t_{HBF}	Holding Time from Bit Clock Low to the Frame Sync (long frame only)	0			ns
t_{SFB}	Set-up Time from Frame Sync to Bit Clock (long frame only)	80			ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (long frame only) FS_X or FS_R	100			ns
t_{DZF}	Delay Time to valid data from FS_X or $BCLK_X$, whichever comes later and delay time from FSX to data output disabled (C_L = 0 pF to 150 pF)	20		165	ns
t_{DBD}	Delay Time from $BCLK_X$ high to data valid (load = 150 pF plus 2 LSTTL loads)	0		150	ns
t_{DZC}	Delay Time from $BCLK_X$ low to data output disabled	50		165	ns
t_{SDB}	Set-up Time from D_R valid to $BCLK_{R/X}$ low	50			ns
t_{HBD}	Hold Time from $BCLK_{R/X}$ low to D_R invalid	50			ns
t_{HOLD}	Holding Time from Bit Clock High to Frame Sync (short frame only)	0			ns
t_{SF}	Set-up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low (short frame sync pulse) - Note 1	80			ns
t_{HF}	Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low (short frame sync pulse) - Note 1	100			ns
t_{XDP}	Delay Time to TS_X low (load = 150 pF plus 2 LSTTl loads)			140	ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (low level) (64 bit/s operating mode)	160			ns

Note : 1.For short frame sync timing. FS_X and FS_R must go high while their respective bit clocks are high.

Figure 1 : 64 k bits/s TIMING DIAGRAM. (see next page for complete timing)

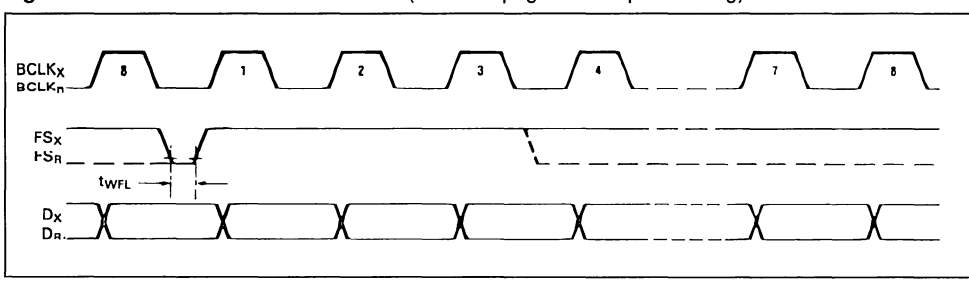


Figure 2 : Short Frame Sync Timing.

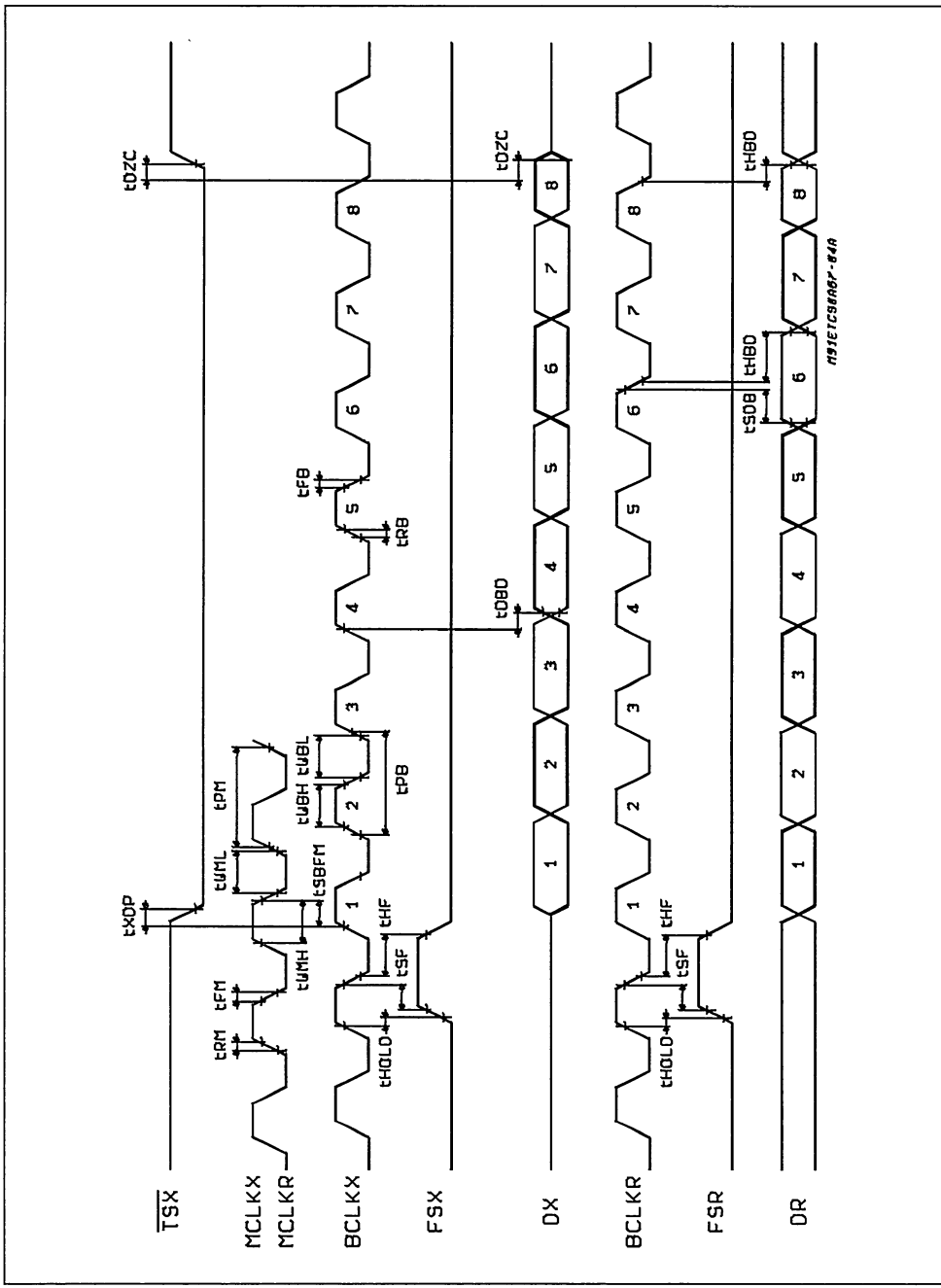
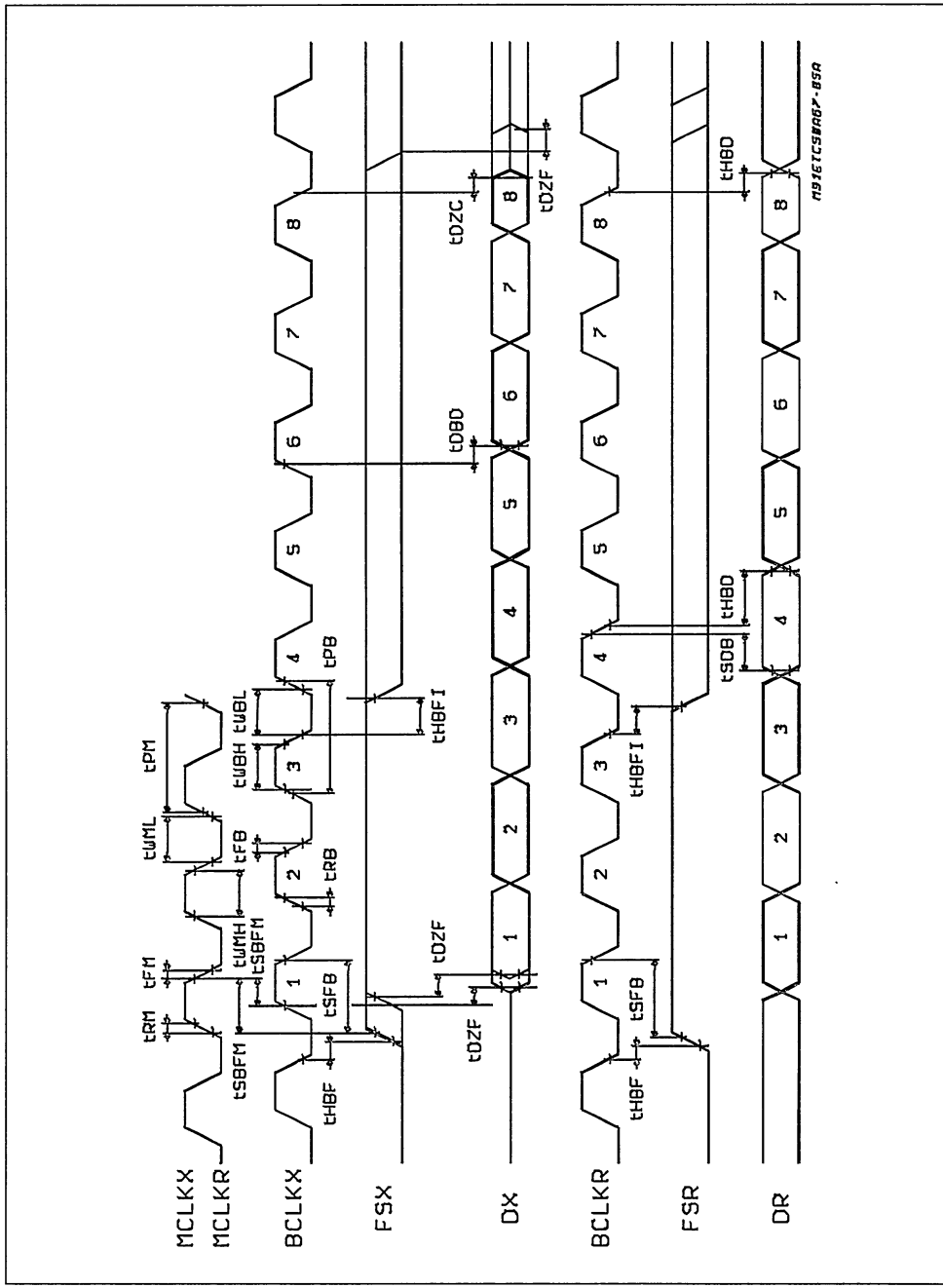


Figure 3 : Long Frame Sync Timing.



TRANSMISSION CHARACTERISTICS

(all devices) T_A = 0°C to 70°C (ETC5064-X/67-X: T_A = –40°C to 85°), V_{CC} = 5V ± 5%, V_{BB} = – 5V ± 5%, GNDA = 0V, f = 1.02kHz, V_{IN} = 0dBm0 transmit input amplifier connected for unity–gain non–inverting. (unless otherwise specified).

AMPLITUDE RESPONSE

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Absolute Levels - Nominal 0 dBm0 is 4 dBm (600Ω). 0 dBm0		1.2276		Vrms
t_{MAX}	Max Overload Level 3.14 dBm0 **ETC5067** 3.17 dBm0 **ETC5064**		2.492 2.501		VPK
G_{XA}	Transmit Gain, Absolute (T_A = 25°C, V_{CC} = 5V, V_{BB} = -5V) Input at GS_X = 0dBm0 at 1020Hz	-0.15		0.15	dB
GXR	Transmit Gain, Relative to GXA f = 16Hz f = 50Hz f = 60Hz f = 180Hz f = 200Hz f = 300Hz -3000Hz f = 3200Hz (ETC5064-X/67-X) f = 3300Hz f = 3400Hz f = 4000Hz f = 4600Hz and up, measure response from oHz to 4000Hz	 - - - -2.8 -1.8 -0.15 -0.35 -0.35 -0.7		 -40 -30 -26 -0.2 -0.1 0.15 0.20 0.05 0 -14 -32	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature T_A = 0°C to +70°C T_A = –40°C to +85°C (ETC5064-X/67-X)	 -0.1 -0.15		 0.1 0.15	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage (V_{CC} = 5V ±5%, V_{BB} = -5V ±5%)	-0.05		0.05	dB
G_{XRL}	Transmit Gain Variation with Level Sinusolidal Test Method Reference Level = -10dBm0 VF_XI^+ = -40dBm0 to +3dBm0 VF_XI^+ = -50dBm0 to -40dBm0 VF_XI^+ = -55dBm0 to -50dBm0	 -0.2 -0.4 -1.2		 0.2 0.4 1.2	dB
G_{RA}	Receive Gain, Absolute (T_A = 25°C, V_{CC} = 5V, V_{BB} = -5V) Input = Digital Code Sequence for 0dBm0 Signal at 1020Hz	-0.15		0.15	dB
G_{RR}	Receive Gain, Relative to G_{RA} f = 0Hz to 3000Hz f = 3200Hz (ETC5064-X/67-X) f = 3300Hz f = 3400Hz f = 4000Hz	 -0.15 -0.35 -0.35 -0.7		 0.15 0.20 0.05 0 -14	dB
G_{RAT}	Absolute Receive Gain Variation with Temeperature T_A = 0°C to +70°C T_A = –40°C to +85°C (ETC5064-X/67-X)	 -0.1 -0.15		 0.1 0.15	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage (V_{CC} = 5V ±5%, V_{BB} = -5V ±5%)	-0.05		0.05	dB
G_{RRL}	Receive Gain Variation with Level Sinusoidal Test Method; Reference Input PCM code corresponds to an ideally encoded -10dBm0 signal PCM level = -40dBm0 to +3dBm0 PCM level = -50dBm0 to -40dBm0 PCM level = -55dBm0 to -50dBm0	 -0.2 -0.4 -1.2		 0.2 0.4 1.2	dB
V_{RO}	Receive Filter Output at VF_RO R_L = 10KΩ	-2.5		2.5	V

TRANSMISSION CHARACTERISTICS (continued).
ENVELOPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Min.	Typ.	Max.	Unit
D_{XA}	Transmit Delay, Absolute (f = 1600 Hz)		290	315	µs
D_{XR}	Transmit Delay, Relative to D_{XA}				
	f = 500 Hz-600 Hz		195	220	
	f = 600 Hz-800 Hz		120	145	
	f = 800 Hz-1000 Hz		50	75	µs
	f = 1000 Hz-1600 Hz		20	40	
	f = 1600 Hz-2600Hz		55	75	
	f = 2600 Hz-2800 Hz		80	105	
	f = 2800 Hz-3000 Hz		130	155	
D_{RA}	Receive Delay, Absolute (f = 1600 Hz)		180	200	µs
D_{RR}	Receive Delay, Relative to D_{RA}				
	f = 500 Hz-1000 Hz	– 40	– 25		
	f = 1000 Hz-1600 Hz	– 30	– 20		µs
	f = 1600 Hz-2600 Hz		70	90	
	f = 2600 Hz-2800 Hz		100	125	
	f = 2800 Hz-3000 Hz		145	175	

NOISE

Symbol	Parameter	Min.	Typ.	Max.	Unit
N_{XP}	Transmit Noise, P Message (A-LAW, $VFxI^+$ = 0 V) Weighted 1)				
	ETC5064		– 74	– 69	dBm0p
	ETC5064-X		– 74	– 67	dBm0p
N_{RP}	Receive Noise, P Message Weighted (A-LAW, PCM Code Equals Positive Zero)		– 82	– 79	dBm0p
N_{XC}	Transmit Noise, C Message Weighted				
	(µ-LAW, $VFxI^+$ = 0 V) **ETC5064**		12	15	dBrnC0
	ETC5064-X		12	16	dBrnC0
N_{RC}	Receive Noise, C Message Weighted (µ-LAW, PCM Code Equals Alternating Positive and Negative Zero)		8	11	dBrnC0
N_{RS}	Noise, Single Frequency f = 0 kHz to 100 kHz, Loop around Measurement, $VFxI^+$ = 0 V			– 53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit (note 2) V_{CC} = 5.0 V_{DC} + 100 mVrms, f = 0 kHz-50 kHz	40			dBp
$NPSR_X$	Negative Power Supply Rejection, Transmit (note 2) V_{BB} = 5.0 V_{DC} + 100 mVrms, f = 0 kHz-50 kHz	40			dBp
$PPSR_R$	Positive Power Supply Rejection, Receive (PCM code equals positive zero, V_{CC} = 5.0 V_{DC} + 100 mVrms)				
	f = 0 Hz-4000Hz A LAW	40			dBp
	µ LAW	40			dBc
	f = 4 kHz-25 kHz	40			dB
	f = 25 kHz-50 kHz	36			dB
$NPSR_R$	Negative Power Supply Rejection, Receive (PCM code equals positive zero, V_{BB} = – 5.0 V_{DC} + 100 mVrms)				
	f = 0 Hz-4000Hz A LAW	40			dBp
	µ LAW	40			dBc
	f = 4 kHz-25 kHz	40			dB
	f = 25 kHz-50 kHz	36			dB
SOS	Spurious out-of-band Signals at the Channel Output 0 dBm0, 300 Hz-3400 Hz input PCM applied at D_R				
	4600 Hz-7600 Hz			–32	dB
	7600 Hz-8400 Hz			–40	dB
	8400 Hz-100,000 Hz			–32	dB

TRANSMISSION CHARACTERISTICS (continued).

DISTORTION

Symbol	Parameter		Min.	Typ.	Max.	Unit
STD_X or STD_R	Signal to Total Distortion (sinusoidal test method) Transmit or Receive Half-channel					dBp
	Level = 3.0 dBm0		33			(ALAW)
	= 0 dBm0 to – 30 dBm0		36			
	= – 40 dBm0	XMT	29			dBc
		RCV	30			(μLAW)
	= – 55 dBm0	XMT	14			
		RCV	15			
SFD_X	Single Frequency Distortion, Transmit (T_A = 25°C)				– 46	dB
SFD_R	Single Frequency Distortion, Receive (T_A = 25°C)				– 46	dB
IMD	Intermodulation Distortion Loop Around Measurement, VF_XI^+ = – 4 dBm0 to – 21 dBm0, two Frequencies in the Range 300 Hz-3400 Hz				– 41	dB

CROSSTALK

Symbol	Parameter		Min.	Typ.	Max.	Unit
CT_{X-R}	Transmit to Receive Crosstalk, 0dBm0 Transmit f = 300 Hz-3400 Hz, D_R = Steady PCM Code	**ETC5064/67**		– 90	– 75	dB
		ETC5064-X/67-X			– 65	dB
CT_{R-X}	Receive to Transmit Crosstalk, 0dBm0 Receive Level (note 2) f = 300 Hz-3400 Hz, VF_XI = 0 V	**ETC5064/67**		– 90	– 70	dB
		ETC5064-X/67-X			– 65	dB

POWER AMPLIFIERS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	Maximum 0 dBm0 Level for Better than ± 0.1 dB Linearity Over the Range 10 dBm0 to + 3 dBm0 (balanced load, R_L connected between VPO^+ and VPO^-)				Vrms
	R_L = 600 Ω	33			
	R_L = 1200 Ω	3.5			
	R_L = 30 kΩ	4.0			
S/D_P	Signal/Distortion R_L = 600 Ω, 0 dBm0	50			dB

Notes : 1. Measured by extrapolation from the distortion test results.
2. PPSRX, NPSRX, CTR–X measured with a –50dBm0 activating signal applied at VF_XI^+

ENCODING FORMAT AT D_X OUTPUT

	A-Law (Including even bit inversion)	μLaw
V_{IN} (at GS_X) = + Full-scale	1 0 1 0 1 0 1 0	1 0 0 0 0 0 0 0
V_{IN} (at GS_X) = 0 V	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1
V_{IN} (at GS_X) = – Full-scale	0 0 1 0 1 0 1 0	0 0 0 0 0 0 0 0

APPLICATION INFORMATION

POWER SUPPLIES

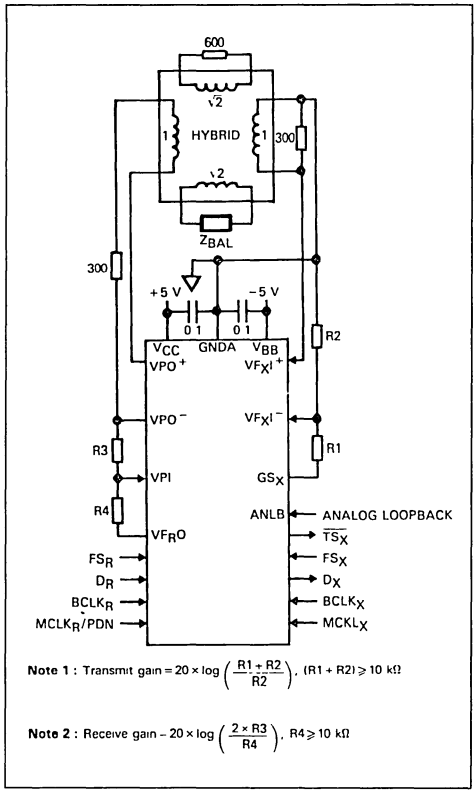
While the pins at the ETC506X family are well protected against electrical misure, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1µF supply decoupling capacitors should be connected from this common ground point to VCC and VBB as close to the device as possible.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to VCC and VBB with 10µF capacitors.

For best performance, $\overline{TSx}$ should be grounded if not used.

Figure 4 : Typical Asynchronous Application.



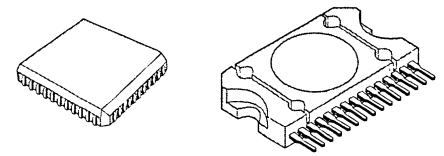
Note 1 : Transmit gain = $20 \times \log \left(\frac{R1 + R2}{R2} \right)$, (R1 + R2) ≥ 10 kΩ

Note 2 : Receive gain = $20 \times \log \left(\frac{2 \times R3}{R4} \right)$, R4 ≥ 10 kΩ

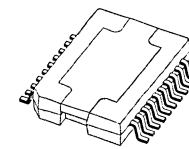
SUBSCRIBER LINE INTERFACE KIT

PRELIMINARY DATA

- PROGRAMMABLE DC FEEDING RESIS-TANCE AND LIMITING CURRENT (four values available)
- THREE OPERATING MODES : STAND-BY, CONVERSATION, RINGING
- NORMAL/BOOST BATTERY, DIRECT/REVERSE POLARITY
- SIGNALLING FUNCTION (off-hook/GND-key)
- FILTERED OFF-HOOK DETECTION IN STAND-BY (10ms)
- QUICK OFF-HOOK DETECTION IN CONVERSATION (< 1ms) FOR LOW DIAL PULSE DETECTION DISTORTION
- HYBRID FUNCTION
- RINGING GENERATION WITH QUASI ZERO OUTPUT IMPEDANCE, ZERO CROSSING INJECTION (no ext. relay needed) AND RING TRIP DETECTION
- AUTOMATIC RINGING STOP WHEN OFF-HOOK IS DETECTED
- PARALLEL AND SERIAL DIGITAL INTERFACES
- TELETAXE SIGNAL INJECTION ($2V_{RMS}/5V_{RMS}$)
- LOW NUMBER OF EXTERNAL COMPONENTS
- GOOD REJECTION OF THE NOISE ON BATTERY VOLTAGE (20dB at 10Hz and 35dB at 1kHz)
- POSSIBILITY TO WORK ALSO WITH HIGH COMMON MODE CURRENTS
- INTEGRATED THERMAL PROTECTION WITH THERMAL OVERLOAD INDICATION
- SURFACE MOUNT PACKAGE (PLCC44 + PowerSO-20)



PLCC44 FLEXIWATT15



PowerSO-20

ORDERING NUMBERS :
L3030 (PLCC44)
L3000N (FLEXIWATT15)
L3000NSO (PowerSO-20)

DESCRIPTION

The ST SLIC KIT (L3000N/L3030) is a set of solid state devices designed to integrate main of the functions needed to interface a telephone line. It consists of 2 integrated devices : the L3000N line interface circuit and the L3030 control unit.

This kit performs the main features of the BORSHT functions :

- Battery feed
- Ringing
- Signalling
- Hybrid

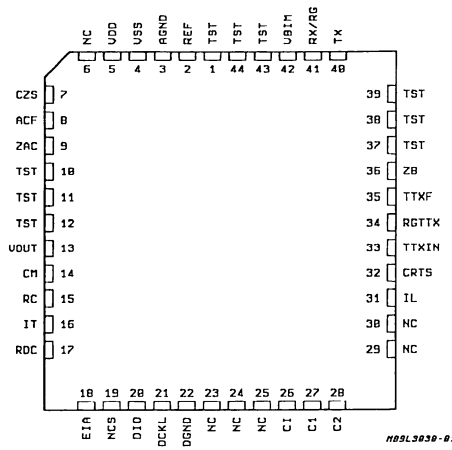
Additional functions, such as battery reversal, extra battery use, line overvoltage sensing and metering-pulse injection are also featured ; most external characteristics, as AC and DC impedances, are programmable with external components. The SLIC injects ringing in balanced mode and for that, as well as for the operation in battery boosted, a positive battery voltage shall be available on the subscriber card. As the right ringing signal amplification both in voltage and in current is provided by SLIC, the ring signal generator shall only provide a low level signal (0.285Vrms).

This kit is fabricated using a 140V Bipolar technology for L3000N and a 12V Bipolar I^2L technology for L3030.

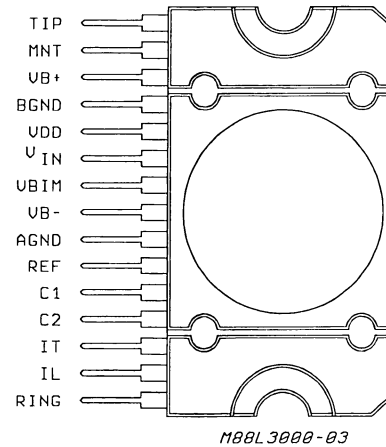
L3030 is available PLCC44 and L3000N in both FLEXIWATT15 and PowerSO-20 for surface mount application.

This kit is suitable for all the following applications: C.O. (Central Office), DLC (Digital Loop Carrier) and high range PABX (Private Automatic Branch Exchange).

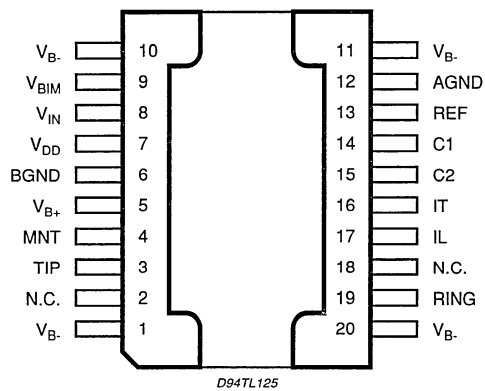
PIN CONNECTIONS (top view)



PLCC44



FLEXIWATT15



PowerSO-20

PIN DESCRIPTION (L3000N)

FLEX. N°	PSO N°	Name	Description
1	3	TIP	A line termination output with current capability up to 100mA (I_a is the current sourced from this pin).
2	4	MNT	Positive Supply Voltage Monitor
3	5	V_{B+}	Positive Battery Supply Voltage
4	6	BGND	Battery ground relative to the V_{B+} and the V_{B-} supply voltages. It is also the reference ground for TIP and RING signals.
5	7	V_{DD}	Positive Power Supply + 5V
6	8	VIN	2 wire unbalanced voltage input.
7	9	VBIM	Output voltage without current capability, with the following functions : - give an image of the total battery voltage scaled by 40 to the low voltage part. - filter by an external capacitor the noise on V_{B-}.
8	1, 10 11, 20	V_{B-}	Negative Battery Supply Voltage
9	12	AGND	Analog Ground. All input signals and the V_{DD} supply voltage must be referred to this pin.
10	13	REF	Voltage reference output with very low temperature coefficient. The connected resistor sets internal circuit bias current.
11	14	C1	Digital signal input (3 levels) that defines device status with pin 12.
12	15	C2	Digital signal input (3 levels) that defines device status with pin 11.
13	16	I_T	High precision scaled transversal line current signal. $I_T = \frac{I_a + I_b}{100}$
14	17	I_L	Scaled longitudinal line current signal. $I_L = \frac{I_b - I_a}{100}$
15	19	RING	B line termination output with current capability up to 100mA (I_b is the current sunk into this pin).
–	2, 18	N.C.	Not connected

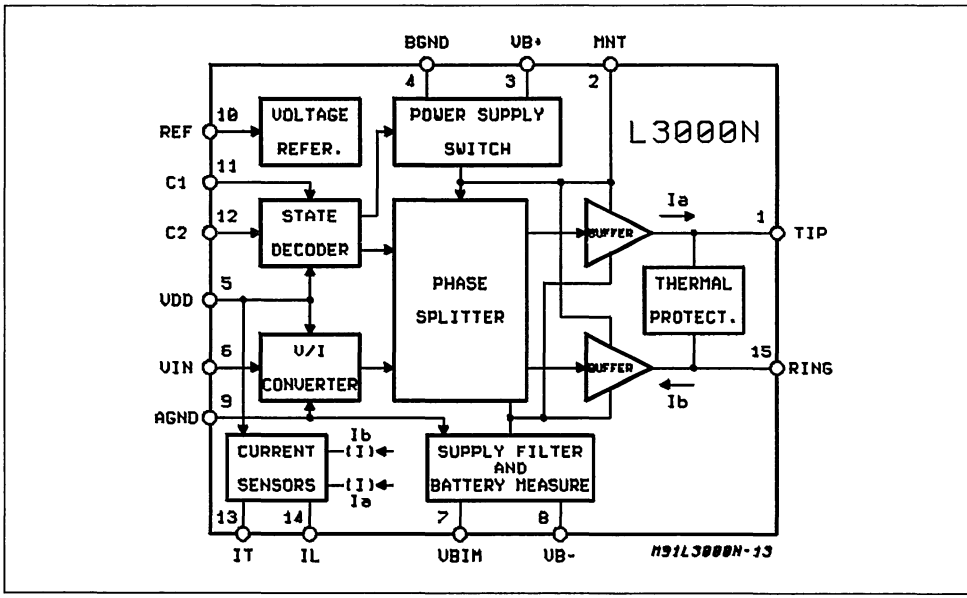
Notes: 1) Unless otherwise specified all the diagrams in this datasheet refers to the FLEXIWATT15 pin connection

2) All informations relative to the PowerSO-20 package option should be considered as advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice.

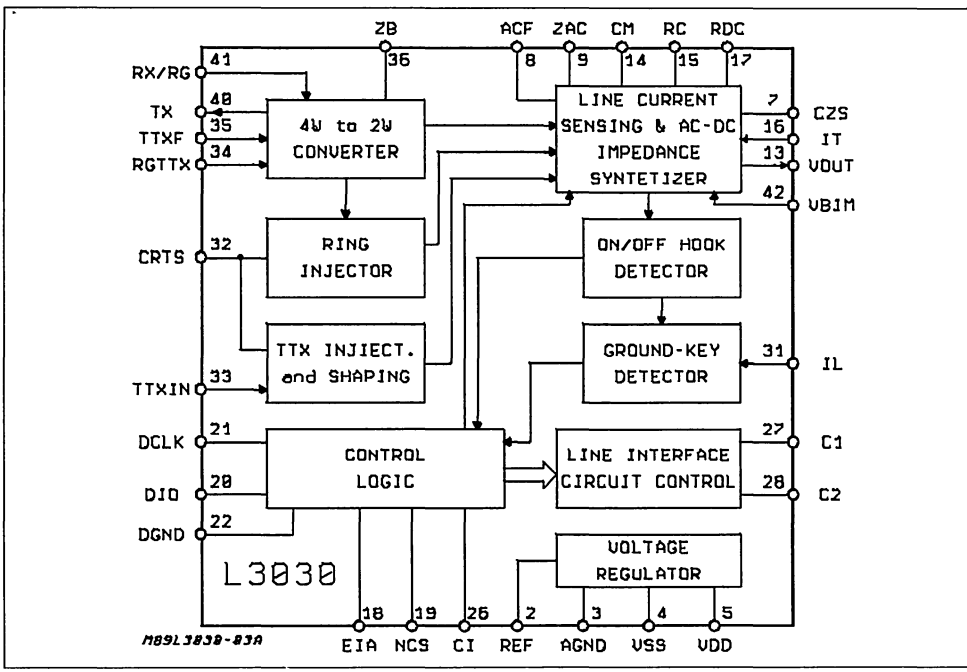
PIN DESCRIPTION (L3030)

Pin	Symbol	Function
1	TST	This pin is connected internally for test purpose. It should not be used as a tie point for external components.
2	REF	Bias Set
3	AGND	Analog Ground
4	VSS	– 5V
5	VDD	+ 5V
6	N.C.	Not connected.
7	CZS	AC Feedback Input
8	ACF	AC Line Impedance Synthesis
9	ZAC	AC Impedance Adjustement
10 11 12	TST	These pins are connected internally for test purpose. It should not be used as a tie point for external components.
13	VOUT	Two wire unbalanced output.
14	CM	Capacitor Multiplier Input
15	RC	DC Feedback Input
16	IT	Transversal Line Current
17	RDC	DC Feeding System
18	EIA	Read/write Command
19	NCS	Chip Select Command
20	DIO	Data Input/output
21	DCKL	Clock Signal
22	DGND	Digital Ground
23	N.C.	Not connected.
24	N.C.	Not connected.
25	N.C.	Not connected.
26	CI	Input/output Changing Command
27	C1	State Control Signal 1
28	C2	State Control Signal 2
29	N.C.	Not connected.
30	N.C.	Not connected.
31	IL	Longitudinal Line Current
32	CRTS	Ringtrip Det. & TTX Shaping
33	TTXIN	Teletaxe Signal Input
34	RGTTX	TTX Filter Level Compensation
35	TTXF	TTX Filter Input
36	ZB	Balancing Network
37 38 39	TST	These pins are connected internally for test purpose. It should not be used as a tie point for external components.
40	TX	4W Sending Output
41	RX/RG	4W Receiving and Ring Input
42	VBIM	Battery Image Input
43 44	TST	These pins are connected internally for test purpose. It should not be used as a tie point for external components.

L3000N BLOCK DIAGRAM



L3030 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{b-}	Negative Battery Voltage	– 80	V
V_{b+}	Positive Battery Voltage	80	V
$\|V_{b-}\| + \|V_{b+}\|$	Total Battery Voltage	140	V
V_{dd}	Positive Supply Voltage	+ 6	V
V_{ss}	Negative Supply Voltage	– 6	V
$V_{agnd} - V_{bgnd}$	Max. Voltage between Analog Ground and Battery Ground	5	V
T_j	Max. Junction Temperature	+ 150	°C
T_{stg}	Storage Temperature	– 55 to + 150	°C

THERMAL DATA

Symbol	Parameter	Value		Unit
L3000N HIGH VOLTAGE		**Flexiwatt**	**PWSO20**	
$R_{th\ j\text{-}case}$	Thermal Resistance Junction to Case	Max. 4	Typ. 2	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient	Max. 50	Max. 60	°C/W
L3030 LOW VOLTAGE				
$R_{th\ j\text{-}amb}$	Max. Resistance Junction to Ambient	80		°C/W

OPERATING RANGE

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{oper}	Operating Temperature Range	0		70	°C
V_{b-}	Negative Battery Voltage	– 70	– 48	– 24	V
V_{b+}	Positive Battery Voltage	0	+ 72	+ 75	V
$V_{b-} + V_{b+}$	Total Battery Voltage		120	130	V
V_{dd}	Positive Supply Voltage	+ 4.5		+ 5.5	V
V_{ss}	Negative Supply Voltage	– 5.5		– 4.5	V
I_{max}	Total Line Current (IL + IT)			85	mA

FUNCTIONAL DESCRIPTION

L3000N - High Voltage Circuit

The L3000N line interface provides a battery feeding for telephone lines and ringing injection. The IC contains a state decoder that under external control can force the following operational modes : standby, conversation and ringing.

In addition Power down mode can be forced connecting the bias current resistor to V_{DD} or leaving it open.

Two pins, I_L and I_T, carry out the information concerning line status which is detected by sensing the line current into the output stage.

The L3000N amplifies both the AC and DC signals entering at pin 6 (VIN) by a factor equal to 40.

Separate grounds are provided :
- Analog ground as a reference for analog signals
- Battery ground as a reference for the output stages

The two ground should be shorted together at a low impedance point.

L3030 - Control Unit

The L3030 low voltage control unit controls L3000N line interface module, giving the proper information to set line feed characteristic, to inject ringing and TTX signal and synthetizes the line and balance impedances. An on chip digital interface allows a microprocessor to control all the operations. L3030 defines working states of line interface and also informs the card controller about line status.

L3000N - Working States

In order to carry out the different possible operations, the L3000N has several different working states. Each state is defined by the voltage respectively applied by pins 27 and 28 of L3030 to the pins 11 and 12 of L3000N.

Three different voltage levels (– 3, 0, + 3) are available at each connection, so defining nine possible

Table 1.

		Pin 28 of L3030 / Pin 12 of L3000N (C2)		
		+ 3	0	– 3
Pin 27 of L3030 / Pin 11 of L3000	+ 3	Stand-by	Conversation in Normal Battery Direct Polarity	Conversation in Normal Battery Reverse Polar
	0	Not allowed.	Conversation in Boost Battery Direct Polarity	Conversation in Boost Battery Reverse Polar
	– 3	Not allowed.	Ringing with Direct Polarity	Not allowed.

states as listed in Table. 1.

Appropriate combinations of two pins define the three modes of the ST SLIC, that are :

a) Stand-by (SBY)
b) Conversation (CVS), Normal and Reverse polarity
c) Ringing (RING)
d) Boost Battery (BB), Normal and Reverse polarity

A fifth status, Power down (PD), can be set disconnecting the bias resistor (RH) from pin 10 of L3000N by means of an external transistor.

The main difference between Stand-by and Power down is that in SBY the power consumption on the voltage battery VB– (– 48V) is reduced but the L3000N DC feeding and monitoring circuits are still active. In PD the power consumption on VB- is reduced to zero, and the L3000N is completely switched off.

The SBY status should be used when the telephone is in On hook and PD status only in emergency condition when it is mandatory to cut any possible dissipation but no operation are requested.

OPERATING MODES

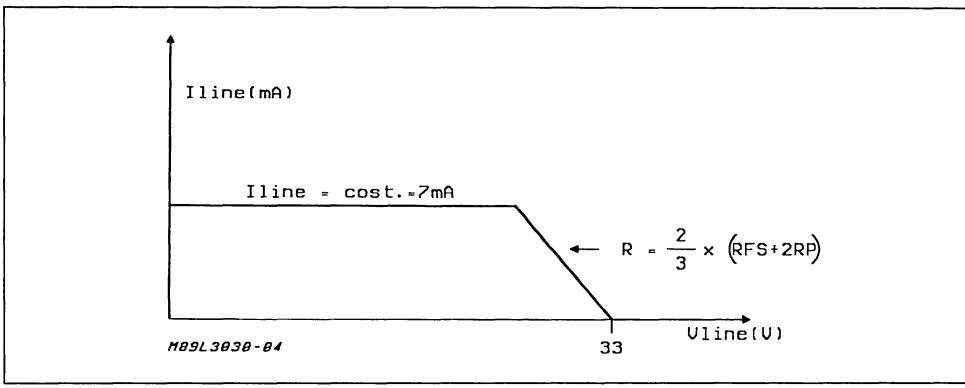
Stand-by (SBY) Mode

In this mode, the bias currents of both L3000N and L3030 are reduced as only some parts of the two circuits are completely active, control interface and current sensors among them. The current supplied to the line is limited at 7mA, and the slope of the DC characteristic corresponds to :

$$R = \frac{2}{3} \times (RFS + 2RP)$$

The Line voltage in on Hook condition is just the battery voltage minus the voltage drop (approx. 15V) of the output stage amplifiers (see Fig. 1).

Figure 1 : DC Characteristics in Stand-by Mode.



The AC characteristic is just the resistance of the two serial resistors RP.

In Stand-by mode the battery polarity is just in direct condition, that is the TIP wire more positive than the RING one ; boost battery is not achievable. There are two possible line conditions where the SLIC is expected to be in stand-by mode :

1) ON-HOOK (I_{line} < 5mA). Normal on-hook condition.
2) OFF-HOOK (I_{line} > 7mA). Handset is unhooked, the SLIC is waiting for command to activate conversation.

When the SLIC is in stand-by mode, the power dissipation of L3000N does not exceed 120mW (from -48V) eventually increased of a certain amount if some current is flowing into the line.

The power dissipation of L3030 in the same condition, is typically 120mW.

The Stand-by Mode is set when the byte sent to the L3030 Serial Digital Interface has the first two bits (BIT0R and BIT1R) equal to "0".

Setting to 0 all the 8 bits of the command sent to the digital interface of L3030, the bias currents of both L3000N and L3030 are reduced and only some parts of the two circuits are active similarly to the stand-by mode ; in this situation, named power-down denial, the line sensors are disabled (ON/OFF-HOOK line conditions cannot be recognized) and the current supplied to the line is limited at 0.25mA.

Conversation (CVS) or Active Mode

In conversation mode it is possible to select between two different DC Characteristics by the BIT5R of the Serial Interface.

1) Normal Battery (NB)
2) Boost Battery (BB)

It is also possible to select (BIT4R) the polarity of the DC line voltage and (BIT6R-BIT7R) one of the four values of limiting current (25mA or 30mA or 45mA or 70mA).

Battery reverse can take place either before or during conversation.

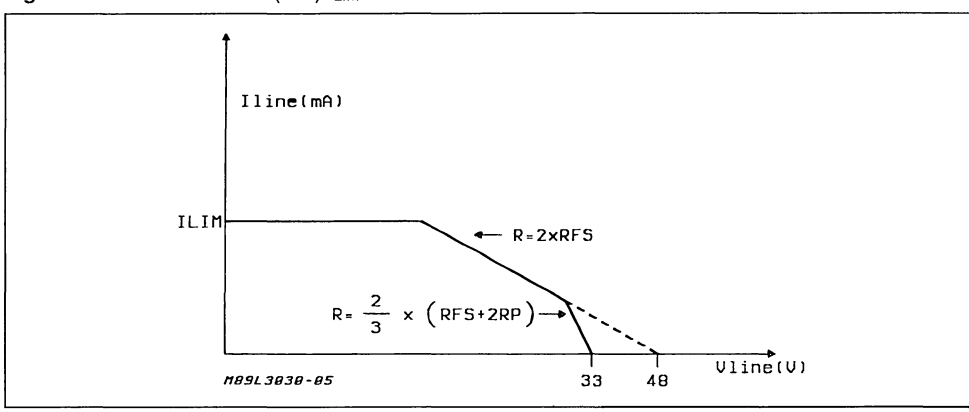
As far as the DC characteristic in Normal Battery is concerned, three different feeding conditions are present :

a) current limiting region ; the DC impedance of the SLIC is very high (> 20 Kohm) and therefore the system works like a current generator, the current value being set through the digital interface (25/30/45/70mA).
b) standard feeding system region ; the characteristic is equal to a – 48V (– 60V) battery (note 1), in series with two resistors, whose value is set by external components (see external component list of L3030).
c) low impedance region ; the battery value is reduced to 33V (45V) and the serial resistance is reduced to the value specified in stand by mode, that is : $\frac{2}{3} \times (RFS + 2RP)$

Switching between the three region is automatic without discontinuity, and depends on the loop resistance. Fig. 2 shows the DC characteristic in normal battery condition.

When the boost battery condition is activated the low impedance region can never be reached by the sy-

Figure 2 : DC Characteristic (n.b.) I_{LIM} = 25/30/45/70 mA.



Note : 1. This value of voltage battery, named apparent battery, is fixed internally by the control unit and is independent of the actual battery value. So, the voltage drop in the low impedance region is 15V. It is also possible to increase up to 25V this value setting BIT3R to 1.

stem ; in this case the internal dropout voltage is equal to 30V.

Fig. 3 shows the DC characteristic in boost battery condition.

In conversation mode, on request of control processor, whatever condition is set (normal or boost battery, direct or reverse polarity), you can inject the 12kHz (or 16kHz) signal (permanently applied at the pin 33 with 950mVrms typ. amplitude), as metering pulses. A patented automatic control system adjust the level of the metering signal, across the line, to 2Vrms setting BIT3 = 0, or to 5Vrms setting BIT3 = 1 ; this, regardless of the line impedance. Moreover the metering signal is ramped at the beginning and at the end of each pulse to prevent undesirable clicking noise ; the slope is determined by the value of CINT (see the external component list of L3030). The SLIC also provides, in the transmit direction (from line to 4-wire side), an amplifier to insert an external notch filter (series resonator) for suppressing the 12/16kHz residual signal.
Fig. 4 shows a suggested notch Filter configuration.

The metering pulses can be injected with a DC line current equal to zero (ON-HOOK Operation).

If teletax is not used the notch filter can be replaced by a 1KΩ resistor.

In conversation mode the AC impedance at the line terminals, ZML, is synthetized by the external components ZAC and RP, according to the following formula :

$$ZML = ZAC + (RP1 + RP2)$$

Depending on the characteristic of the ZAC network, ZML can be either a pure resistance or a complex impedance, so allowing ST SLIC to meet different standards as far as the return loss is concerned. The capacitor CCOMP guarantees stability to the system.

The two-to-four wire conversion is achieved by means of a Wheatstone bridge configuration, the sides of which being :

1) the line impedance (Zline),
2) the SLIC impedance at line terminals (ZML),
3) the network ZA connected between pin 36 and 41 of L3030 (see external component list of L3030),
4) the network ZB between pin 36 and ground that shall copy the line impedance.

For a perfect balancing, the following equation shall be verified :

$$\frac{ZA}{ZB} = \frac{ZML}{Zline}$$

It is important to underline that ZA and ZB are not obliged to be equal to ZML and to Zline, but they both may be multiplied by a factor (up to ten) so allowing use of smaller capacitors.

In conversation, the L3000N dissipates about 250mW for its own operation ; the dissipation depending on the current supplied to the line shall be added.

The fig 5 and fig 6 show the DC characteristic for two different Feeding resistance.
2 x 200 Ohm and 2 x 400 respectively.

Figure 3 : DC Characteristic (b.b.)
I_{LIM} = 25/30/45/70 mA.

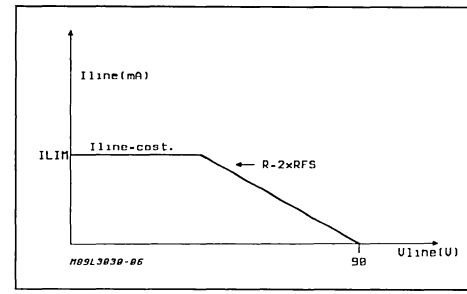
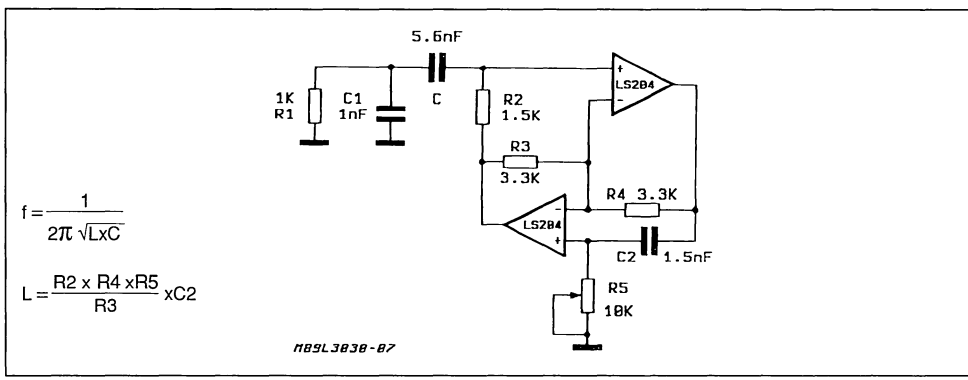


Figure 4 : External Teletaxe Filter.



$$f = \frac{1}{2\pi\sqrt{LxC}}$$

$$L = \frac{R2 \times R4 \times R5}{R3} \times C2$$

Figure 5 : DC Characteristic for 2 x 200 ohm Feeding System.

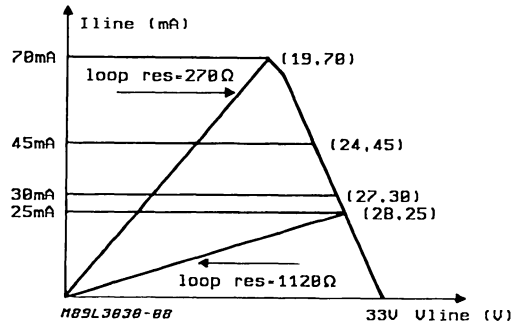


Figure 6 : DC Characteristic for 2 x 400 ohm Feeding System.

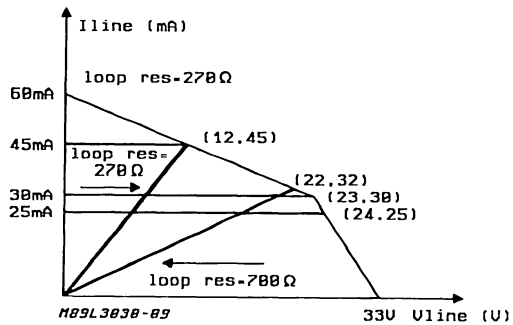
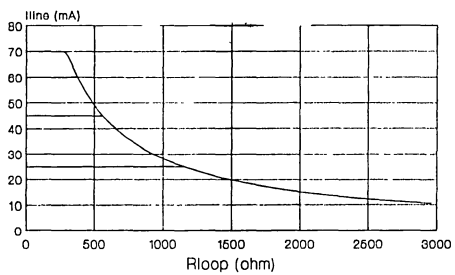


Figure 7 : Line Current Versus Loop Resistance, RFS = 200Ω, R_P = 30Ω, V_{B-} = −48V.



Ringing Mode

When ringing is selected (BIT2R = 1, BIT0R = 0), the control unit L3030 presets the L3000N to operate between – 48V (– 60V) and + 72V (+ 60V) battery. Then, setting BIT1 = 1, a low level signal (0.285Vrms with frequency range 16-66Hz) applied to pin 41, is amplified and injected in balanced mode to the line through L3000N with a superimposed DC voltage of 24V. The impedance to the line is given by the two external resistors and the 24V DC polarity can only be direct.

The first and the last ringing cycles are synchronized by L3030 so that ringing always starts and stops at zero crossing. Ring trip detection is performed autonomously by the SLIC, without any particular command, using a patented system ; when handset is lifted, SLIC suspends the ringing signal just remaining in the ringing mode. In this condition, the control unit L3030 checks that the loop is closed for a time equal to two periods of the ringing signal ; if the closure is confirmed, a flag (BIT0T = 1) is set and the SLIC waits the new command from the control processor. Whereas the loop closure is not confirmed, the ringing signal is newly applied to the line, without setting BIT0T.

DIGITAL INTERFACE

Functional Description

The L3030 states and functions are controlled by central processor through five wires defining a digital interface. It is possible to select the interface working mode between SERIAL or PARALLEL (pin 33 tied to a voltage between 4 and 5V).

1) Serial Mode

The five wires of the digital interface have the following functions :

- clock (DCLK), entering at pin 21
- data in/data out (DIO), exchanged at pin 20
- input/output select (EIA), entering at pin 18
- chip select (NCS), entering at pin 19
- change NCS from in to out (CI), entering at pin 26 (note 1)

The maximum clock frequency is 600Khz.

When EIA signal is low data are transferred from the card controller into I/O registers of the L3030 selected by NCS signal tied at low level ; then data are latched for execution. In this phase a complete 8 bit word is loaded into internal register and consequently NCS signal must remain low for the corresponding 8 clock pulses (DCLK). The EIA signal must remain at low level at least for the time in which NCS signal remain low. The device load data in input register during the positive edge of clock signal (DCLK) and store the contents of the register on the positive edge of NCS signal.

When EIA signal is high data are transferred from the L3030 selected by NCS tied to low level to the card controller. The L3030 status is described by five bits contained in the output register ; the NCS signal can remain low for five or less clock pulses depending if the card controller want to read the complete L3030 status or only a part of it.

Fig. 8, 9 show the complete write and read operation timing. Table 1 shows the meaning of each bit of an I/O data.

Table 1 : Serial Mode.

Meaning	Value			
Data in (note 2)				
BIT0R = Impedance (note 3)	0 - Stand-by/ringing			
	1 - Conversation			
BIT1R = TTX & Ring Timing (note 4)	0 - Timing off			
	1 - Timing on			
BIT2R = Ring (note 5)	0 - TTX Signal Injection			
	1 - Ring Signal Injection			
BIT3R = TTX Level	0 - Low Amplitude ($2V_{RMS}$)			
	1 - High Amplitude ($5V_{RMS}$)			
BIT4R = Battery Polarity	0 - Normal Polarity			
	1 - Reverse Polarity			
BIT5R = Extra Feeding	0 - Normal Battery			
	1 - Boosted Battery			
BIT6R / BIT7R Current Limiting	0 25mA 0	0 30mA 1	1 45mA 1	1 70mA 0
Data Out (note 6)				
BIT0T = Line Supervision	0 - On Hook			
	1 - Off Hook			
BIT1T = Ground Key	1 - Long. Line Current < 17mA			
	0 - Long. Line Current > 17mA			
BIT2T = Internal Line Current Limiter (note7)	0 - Off			
	1 - On			
BIT3T = Line Voltage	0 - Normal			
	1 - Minus of Half Battery			
BIT4T = Thermal Overload (note 8)	1 - Off			
	0 - On			

Notes : 1. When CI signal is tied to low level, NCS signal is the chip select input ; with CI signal at high level, the NCS signal becomes an output that carry out the logical sum of the following bits : BIT0T, BIT1T.
2. The description of the commands is referred to the system L3030 + LINE INTERFACE module.
3. To set SBY mode with I_{lim} = 7mA : BIT0R = 0 and at least one of the two last bits (BIT6R ; BIT7R) must be set to 1.
4. TTX and RING signals are injected into the line interface module with BIT1R to "1".
5 To set RING mode at least one of the three last bits (BIT5R, BIT6R, BIT7R) must be set to 1, in addition BIT0R must be set to 0.
6. The description of the commands is referred to the system L3030 + LINE INTERFACE module.
7. The bit BIT2T is set to 1 when the SLIC is operating in Conversation Mode and into the limiting current region (short loop).
8. The bit BIT4T is set to 1 when the junction temperature of L3000N is about 140°C.

Figure 8 : Writing Operation Timing (serial mode).

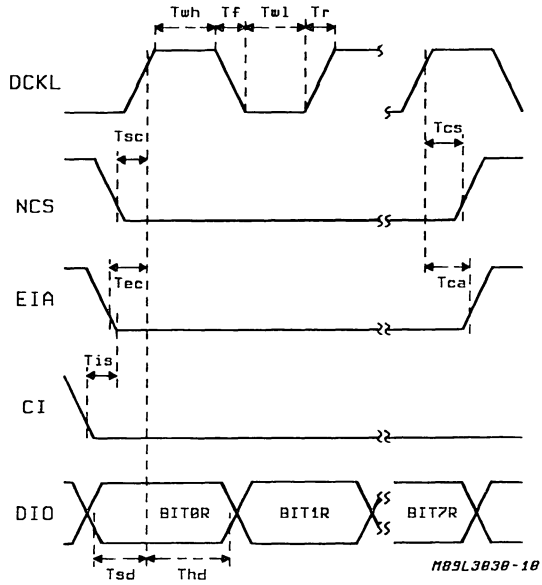
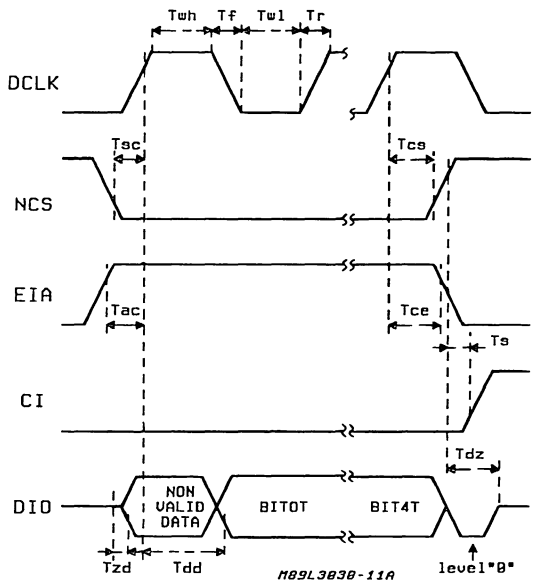


Figure 9 : Reading Operation Timing (serial mode).



2) Parallel Mode

This operating mode is enabled connecting pin 33 to a voltage in the range from 4V to 5V. The five wire have the following functions :
- power down/feeding (EIA), entering at pin 18
- timing (CI), entering at pin 26
- ring (DCLK), entering at pin 21
- on-hook/off-hook (NCS), outgoing at pin 19
- ground-key (DIO), outgoing at pin 20

In this operating mode the signals at the inputs are immediately executed, without any external clock timing ; all the internal registers are bypassed. The informations sent back on pins 19 and 20, display in real time the setting of internal circuits, that means line status. In the table 2 the correspondence between the interface wires in the parallel mode and equivalent bit in serial mode is pointed out ; where there isn't this correspondence, the internal setting is shown.

Table 2 : Parallel Mode.

Pin	Rif.	Meaning (note 1)	Eq. Bit of Ser. Interf.	Value
18	EIA	PD/feeding	BIT0R	0 : High Impedance
				1 : Low Impedance
26	CI	Timing	BIT1R	0 : Ring Timing Off
				1 : Ring Timing On
21	DCKL	Ring	BIT2R	0 : No Ring
				1 : Ring Injection
			BIT3R	0 : Low Amplitude
			BIT4R	0 : Normal Polarity
			BIT5R	0 : Normal Battery
			BIT6R	0 : 1 : Line Curr. = 30mA
			BIT7R	
19	NCS	On-hook/off-hook	BIT0T	0 : On-hook
				1 : Off-hook
20	DIO	Ground Key	BIT1T	1 : Long. Curr. < 17mA
				0 : Long. Curr. > 17mA
			BIT2T	
			BIT3T	
			BIT4T	

Note : 1. The description of the commands is referred to the system L3030 + LINE INTERFACE module.

DIGITAL INTERFACE ELECTRICAL CHARACTERISTICS

(V_{DD} = + 5V, V_{SS} = – 5V, $T_{amb.}$ = 25°C) (refer to PLCC44 package)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
STATIC ELECTRICAL CHARACTERISTICS						
Vil	Input Voltage at Logical "0"	Pins 18, 19, 20, 21, 26	0		0.8	V
Vih	Input Voltage at Logical "1"		2.0		5	V
Iil	Input Current at Logical "0"	Vil = 0V			200	µA
Iih	Input Current at Logical "1"	Vih = 5V			10	µA
Vol	Output Voltage at Logical "0"	Pins 19, 20 Iout = – 1mA			0.4	V
Voh	Output Voltage at Logical "1"	Pins 19, 20 Iout = 1mA	2.4			V
Ilk	Tristate Leak. Current	Pin 20 NCS = "1"			10	µA

DIGITAL INTERFACE ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DYNAMIC ELECTRICAL CHARACTERISTICS						
fclk	Clock Frequency		1		600	kHz
Tr, Tf	Clock Rise and Fall Time				50	ns
Twh, Twl	Clock Impulse Width		750			ns
Tis	CI to NCS Set up Time		300			ns
Tec	"0" EIA to DCKL Set up Time		300			ns
Tsc	DCKL to NCS Delay (+ edge)		300			ns
Tsd	Data in Set up Time		0			ns
Thd	Data in Hold Time		800			ns
Tcs	NCS to DCKL Hold Time		800			ns
Tca	"0" EIA to DCKL Hold Time		900			ns
Tac	"1" EIA to DCKL Set up Time		400			ns
Tzd	Data out to "0" NCS Delay		0		600	ns
Tce	"1" EIA to DCKL Hold Time		900			ns
Tdz	Data out to "1" NCS Delay				500	ns
Tdd	Data out to DCKL Delay				1500	ns
Tsi	"0" CI to NCS Hold Time		300			ns

OPERATION DESCRIPTION

To set SLIC in operation the following parameters have to be defined :

- the DC feeding resistance RFS, defined as the resistance of each side of the traditional feeding system (most common values are 200, 400 or 500 ohm).
- the AC impedance at line terminals, ZML, to which the return loss measurement references. It can be real (typically 600 ohm) or complex.
- the equivalent AC impedance of the line Zline, when evaluating the trans hybrid loss (2/4 wire conversion). It is usually a complex impedance.
- the ringing signal frequency Fr (ST SLIC allows frequency ranging from 16 to 66Hz).
- the metering pulse frequency Ft (two values are possible : 12kHz or 16kHz).
- the value of the two resistors RP1/RP2 in series with the line terminals ; main purpose of the a.m. resistors is to allow primary protection to fire. ST suggest the minimum value of 50 ohm for each side.

On this assumptions, the following component list is defined.

EXTERNAL COMPONENT LIST FOR THE LINE INTERFACE

Pin	Component		Involved Parameter or Function
	Ref.	Value	
L3000N			
10	RREF	24.9kΩ ± 1%	Bias Resistance
1,15	RP	30 to 100Ω	Line Series Resistor
7	CDVB	47µF – 20V	Battery Voltage Rejection
3	CVB+	0.1µF – 100V (1)	Positive Battery Filter
8	CVB–	0.1µF – 100V (2)	Negative Battery Filter
8	D1	BAT 49X	Protective Shottky Diode
L3030 (PLCC44)			
4-3	CVSS	0.1µF – 15V	Negative Supply Voltage Filter
5-3	CVDD	0.1µF – 15V	Positive Supply Voltage Filter
7-8	RR	16KΩ (range: 10 to 50KΩ)	Capacitor Multiplier Gain (8)
15-17	RDC	2 x (RFS – RP1)	DC Feeding Resistor (RDC > 270Ω)
7-15	CAC1 (3)	$\frac{1}{6.28 \times 250 \times (ZAC + RDC)}$	AC Path decoupling
14-15	CAC2	CAC1	
8-9	ZAC	ZML – (RP1 + RP2)	2 Wire AC impedance
8-9	CCOMP	1/(6.28 x 150000 x (RPC))	AC loop compensation
9-14	RPC	RP1 + RP2	Rp insertion loss compensation
2-3	RREF	24.9KΩ 1%	Bias Resistance
36-3	ZB	K x Zline (note 4)	Line Impedance Balancing Network
36-41	ZL	K x RPC in Series with K x ZAC // (CCOMP/K)	SLIC Impedance Balancing Network (note 5)
32-3	CINT	(note 6)	Ring trip detection time constant
15-16	Ccon	0.15µF (note 7)	Interface Time Constant
35	TTx FILT.	Z_{TTX} = 1kΩ 1% in speech band Z_{TTX} ≈ 0Ω at TTX freq. (note 9)	Teletax filter.
34	R_{GTTX}	10kΩ 1%	Teletax filter.

Notes :

1. In case line cards with less than 7 subscribers are implemented CVB– capacitor should be equal to 680nF/N where N is the number of subscriber per card.
2. This shottky diode or equivalent is necessary to avoid to damage to the device during hot insertion or in all those cases when a proper power up sequence cannot be guaranteed.
   In case the shottky diode is not implemented the power sequence should guarantee that VB+ is always the last supply applied at power on and the first removed at power off.
   In case an other shottky diode type is adopted it must fulfill the following characteristics:
   V_F < 450mV @ I_F = n 15mA, T_{amb} = 25°C
   V_F < 350mV @ I_F = n · 15mA, T_{amb} = 50°C (T_{jL3000} = 90°C)
   V_F < 245mV @ I_F = n · 15mA, T_{amb} = 85°C (T_{jL3000} = 120°C)
   Where n is the number of line sharing the same diode.
3. If the internal capacity multiplier stage is not used, pin 7 must be connected with pin 14 without mounting RR and CAC2. In this case CAC1 = 1/(6.28 x 30 x RDC).
4. The structure of this network shall copy the line impedance, in case multiplied by a factor K = 1....10
5. K as fixed at note 4.
6. CINT can have the following values :

Fr. (Hz)	16/18	18/21	21/26	26/31	31/38	38/46	46/57	57/66
CINT (nF)	560	470	390	330	270	220	180	150

7. Ccon is necessary to work "without on/off hook detection-errors" during TTX-pulses.
8. RR is used by a capacitor multiplier circuit to synthetize an higher AC/DC splitting capacitor starting from CAC1 and CAC2. Supposing CAC1 = CAC2 = CAC the synthetized capacitor value will be equal $\frac{RR + ZML}{ZML} \cdot CAC$.
9. If Teletax is not used the TTX FILT. can be replaced by a 1kΩ resistor.

Figure 10 : Typical Application Schematic Diagram.

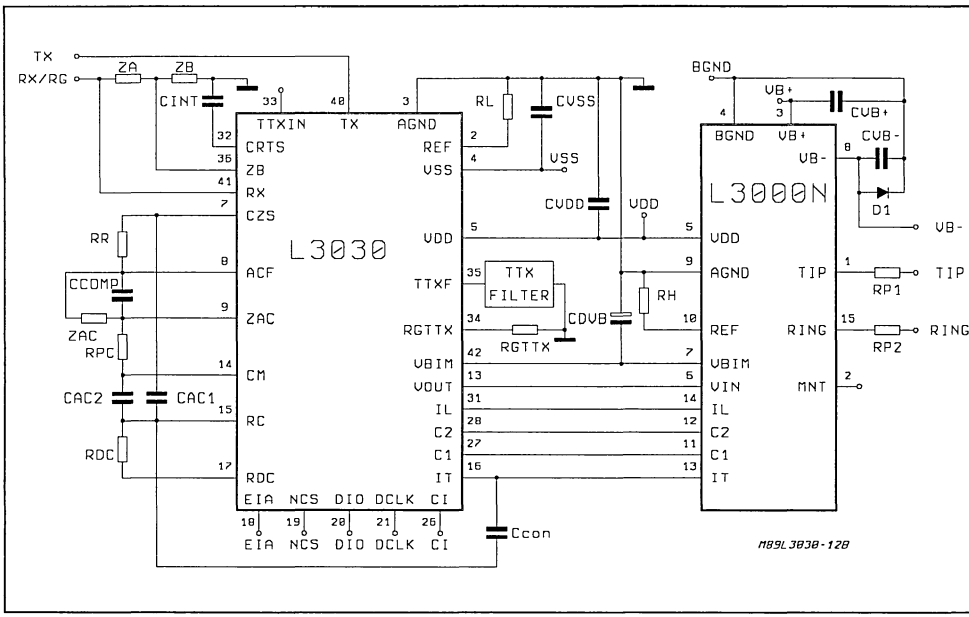
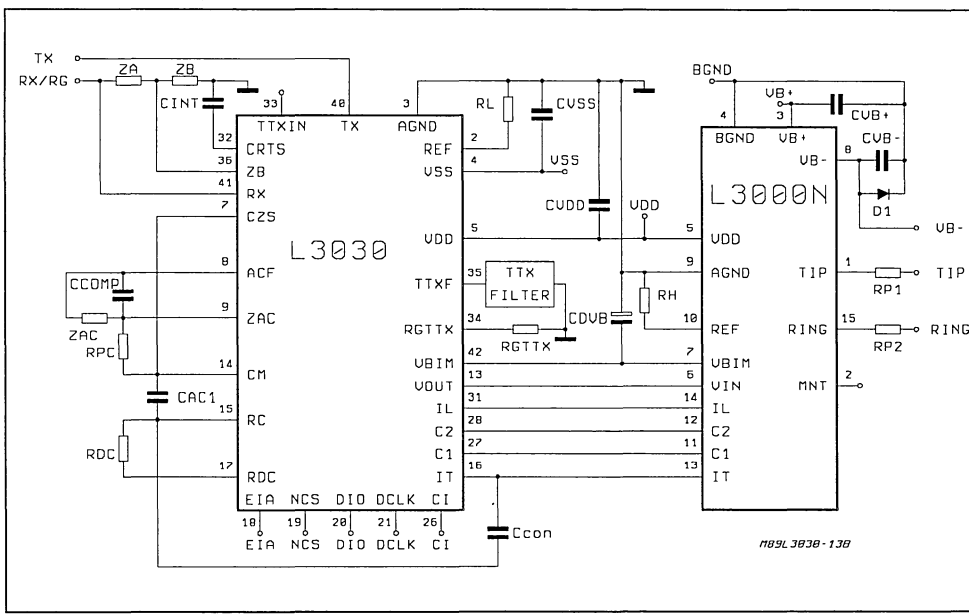


Figure 11 : Typical Application Schematic Diagram without Capacitor Multiplier.



ELECTRICAL CHARACTERISTICS (refer to the test circuits of the Figure 12, V_{DD} = + 5V, V_{SS} = - 5V, V_{B+} = + 72V, V_{B-} = – 48V, T_{amb} = + 25°C, TTX FILT = 1kΩ)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
STAND-BY						
Vls	Output Voltage at L3000N Terminals	Iline = 0mA Iline = 5mA	30.0 28.2		40.0 38.5	V V
Ilcc	Short Circuit Current	DATA IN (note 1) 000X00X1	5		8.5	mA
Iot	On/off-hook Detection Threshold		5		8.5	mA
Vls	Symmetry to Ground	Iline = 0mA			.75	V
STAND BY DENIAL						
Ilcc	Short Circuit Current	DATA IN 000X00X0			2	mA
DC OPERATION - NORMAL BATTERY (V_{TTX} = 2V_{RMS}, low level)						
Vlo	Output Voltage at L3000N Terminals Ilim = 70mA Data in 1000X010	Iline = 0mA Iline = 20mA Iline = 50mA	31.0 24.0 2.5		35.0 28.8 17.5	V V V
Ilim	Current Programmed Through the Digital Inter.		– 10%	Ilim	+ 15%	mA
Io	On-hook Detection Threshold				8	mA
If	Off-hook Detection Threshold		12			mA
Ilgk	Longitudinal Line Current with GK Detect		10	17	26	mA
DC OPERATION - BOOST BATTERY						
Vlo	Output Voltage at L3000N Terminals	Iline = 0mA Iline = 20mA	86 68.6		95.6 81	V V
AC OPERATION						
Ztx	Sending Output Impedance 4 Wire Side				10	Ω
Zrx	Receiving Input Impedance 4 Wire Side		100			kΩ
THD	Signal Distorsion at 2W and 4W Terminals				0.5	%
R1	2W Return Loss	f = 300 to 3400Hz	22			dB
Thl	Trans Hybrid Loss	f = 300 to 3400Hz	24			dB
Gs	Sending Gain	Vso = 0dBm f = 1020Hz Norm. Polarity	– 0.25		+ 0.25	dB
Gsf	Sending Gain Flatness versus Frequency	f = 300 to 3400Hz Respect to 1020Hz	– 0.1		+ 0.1	dB
Gsl	Sending Gain Linearity	fr = 1020Hz, Vsoref = –10dBm Vso = + 4 /– 40dBm	– 0.1		+ 0.1	dB
Gr	Receiving Gain	Vri = 0dBm f = 1020Hz Norm. Polarity	– 0.25	0	+ 0.25	dB
Grf	Receiving Gain Flatness	f = 300 to 3400Hz Respect to 1020	– 0.1		+ 0.1	dB

Notes : 1. The data into the digital interface of L3030 are send in serial mode. The format of data is the following :
a) DATA IN : the bit at left side is BIT 0 of the writing word, while the bit at the right side is BIT 7.
b) DATA OUT : the bit at the left side is BIT0 of the reading word, while the bit at the right is BIT4.
When appear a symbol X, the value of the bit don't care.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
AC OPERATION (continued)						
Grl	Receiving Gain Linearity	fr = 1020Hz, Vriref = – 10dBm Vri = + 4 /– 40dBm	– 0.1		+ 0.1	dB
Np4W	Psophometric Noise at 4W-Tx Terminals			– 75	– 70	dBmp
Np2W	Psophometric Noise at Line Terminals			– 75	– 70	dBmp
SVRR	Supply Voltage Rejection Ratio Relative to VB–	f = 3400Hz			– 30	dB
SVRR	Relative to V_{DD}	f = 3400Hz Vs = 100mVrms		– 30	– 26	dB
SVRR	Relative to V_{SS}			– 32	– 30	dB
Ltc	Longitudinal to Transversal Conversion	f = 300 to 3400Hz Iline = 30mA, ZML = 600Ω	49 (1)	60		dB
Tlc	Transversal to Longitudinal Conversion		48	51		dB
Td	Propagation Time	Both Direction			40	µs
Tdd	Propag. Time Distortion				25	µs
Vttx	Line Voltage of Teletaxe Signal	V_{TTXin} = 950mVrms Note 2 Note 3	1.7 4.5		2.3 5.5	V V
THD	Teletaxe Signal Harmonic	Dist. ttx Filt = 0Ω @ 16kHz Note 4			5	%
Zitt	Teletaxe Amplif. Input Impedance	Pin 33 of L3030	100			kΩ
AC OPERATION BOOST BATTERY						
Gs	Sending Gain	Vso = 0dBm f = 1020Hz Norm. Polarity	– 0.66	– 0.16	+ 0.34	dB
Gr	Receiving Gain	Vri = 0dBm f = 1020Hz Norm. Polarity	– 0.27	+ 0.08	+ 0.43	dB
Np4W	Psophometric Noise at 4W-Tx Terminals			– 73	– 68	dBmp
Np2W	Psophometric Noise at line Terminals			– 73	– 68	dB
SVRR	Relative to Vdd	f = 3400Hz Vs = 100mVrms			– 23	dB
SVRR	Relative to Vss				– 23	dB
RINGING PHASE						
Vlr	Superimposed DC Voltage	Rloop > 100kΩ Rloop = 1kΩ	19 17	23 21	27 25	V V
Vacr	Ringing Signal at Line Termin.	Rloop = 1kΩ/1µF	56			Vrms
If	DC Off-hook Det. Threshold		1.5		3.5	mA
Ilim	Current Limit.		85		130	mA
Vrs	Ringing Simmetry				2	Vrms
THDr	Ringing Signal Distortion	V_{AC} = 0.285V_{RMS} f_{RING} = 30Hz			5	%

Notes : 1. Up to 52dB using selected L3000N.
2. The configuration of data sent to device change, every 100mS, from - 1100X010 - to - 1000X010 -
3. The configuration of data sent to device change, every 100mS, from - 1101X010 - to - 1001X010 -
4. Error generated by ttx filt ≠ 0 ohm, on the output teletax amplitude is err% = 100 x (1 + A) x B/C where A = 10 Kohm/RGTTX[Kohm], B = TTXFILT[Kohm], C = (TTXFILT[Kohm] + 1 Kohm), for example 10 ohm means err% = 2%.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
RINGING PHASE						
Zir	Ringing Amplif. Input Impedance	Pin 41 of L3030	100			kΩ
Vrr	Residual of Ringing Signal at TX Output				600	mV
Trt	Ring Trip Detection Time	fring = 16Hz T = 1/fring	(1T)		125 (2T)	ms
Toh	Off-hook Status Delay after the Ringing Stop				125 (2T)	ms
Trs	Cut off of Ringing	Ring Trip not Confirmed			188 (3T)	ms
SUPPLY CURRENT						
IDD	Positive Supply Current CS = 1	Stand-by Conversation (NB/BB) Ringing		16.0 26.0 16.5	20.0 31.0 21.0	mA mA mA
ISS	Negative Supply Current CS = 1	Stand-by Conversation (NB/BB) Ringing		9 19 9	12 23 12	mA mA mA
I_{BAT-}	Negative Battery Supply Current Line Current = 0mA	Stand-by Conversation NB Conversation BB Ringing		2 5 6.6 14	2.5 6.5 8.0 17	mA mA mA mA
I_{BAT+}	Positive Battery Supply Current Line Current = 0mA	Stand by Conversation NB Conversation BB Ringing		10 10 8 12	15 15 10 13.5	µA µA mA mA

NB = Normal Battery
BB = Boosted Battery

Figure 12 : Slic Test Circuit Schematic.

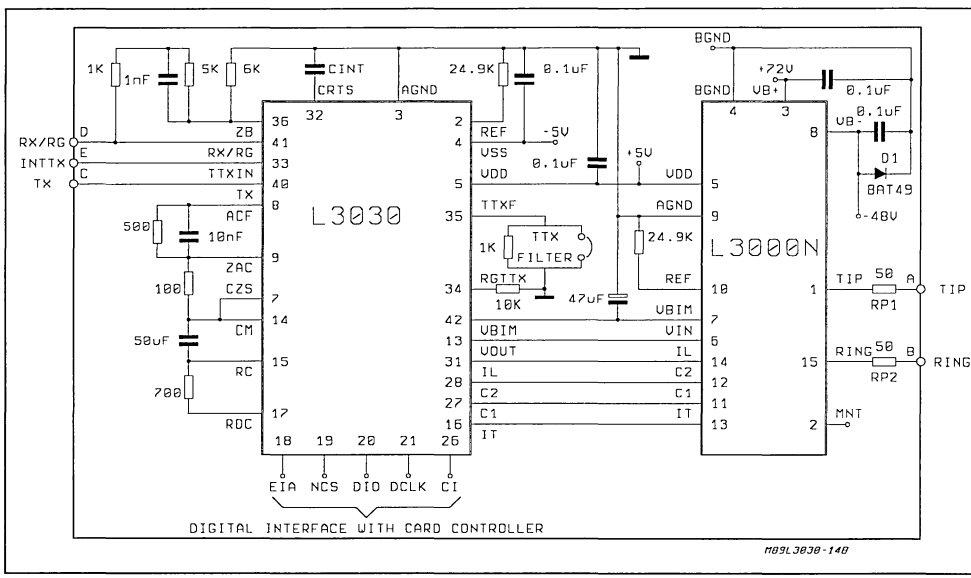


Figure 13: Typical application schematic with 2nd generation COMBO.

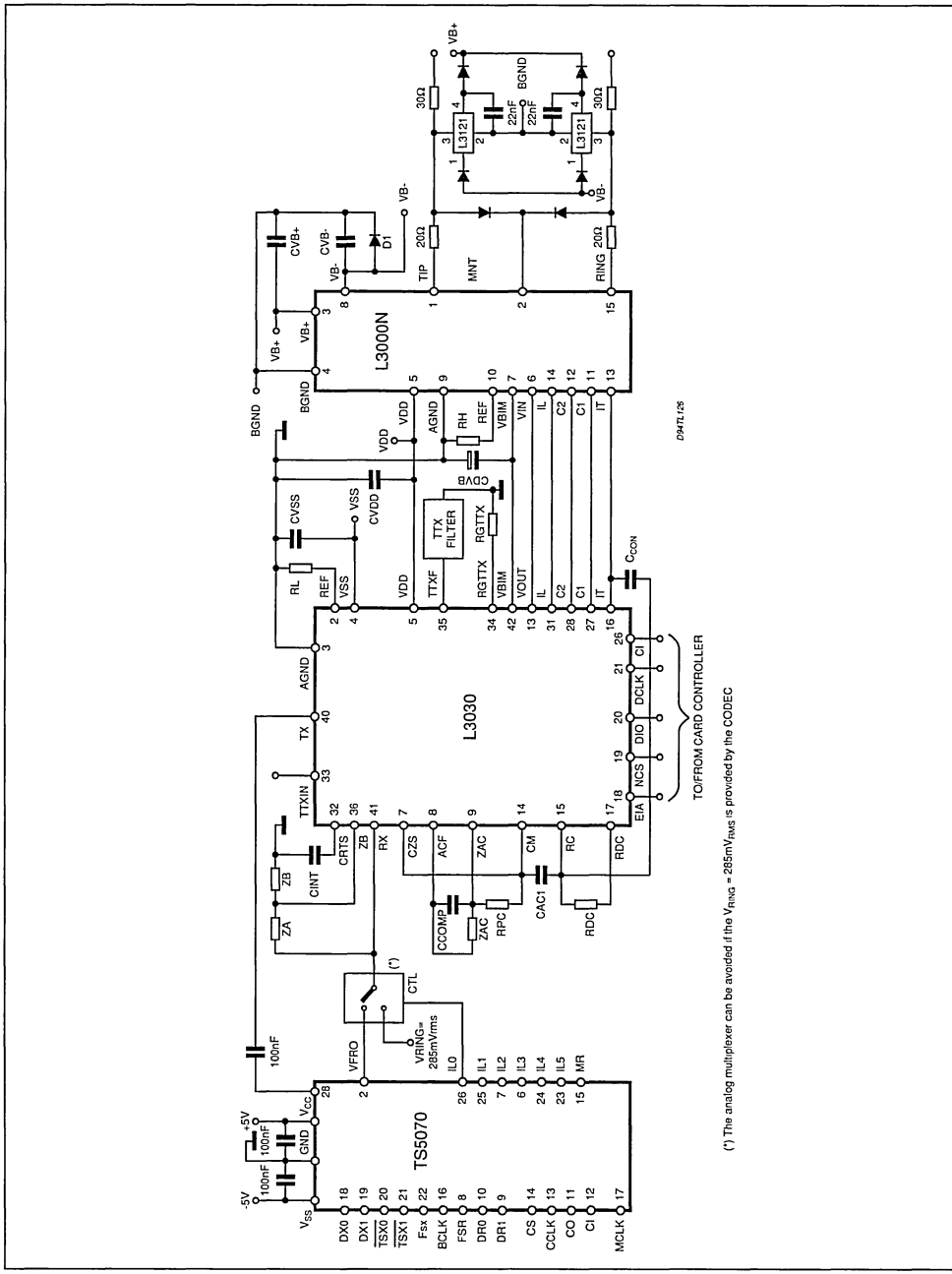
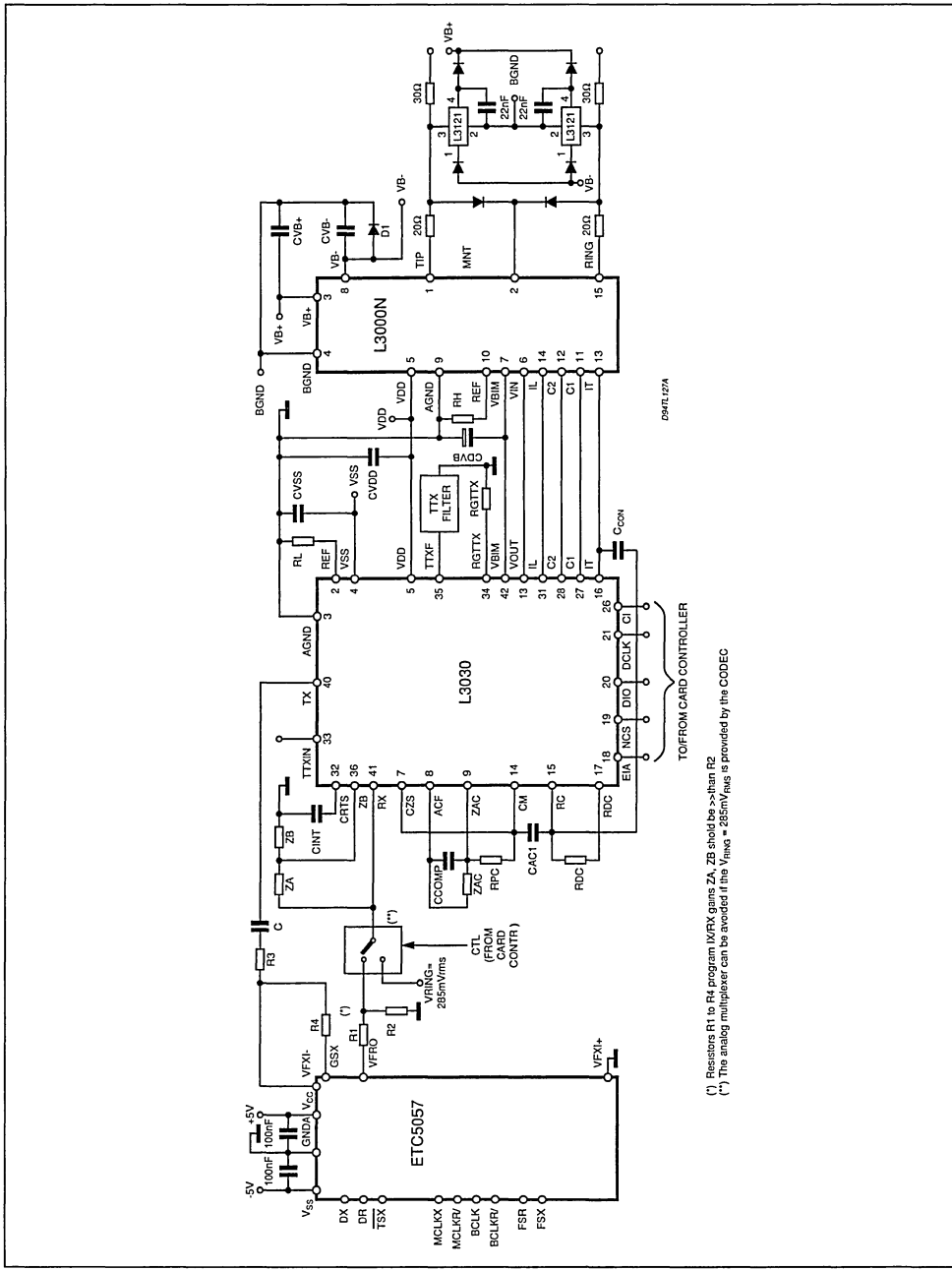


Figure 14: Typical application schematic with 1st generation COMBO.



APPENDIX

SLIC TEST CIRCUITS

Referring to the test circuit reported at the end of each SLIC data sheet here below you can find the proper configuration for each measurement.

In particular : A-B : Line terminals

C : TX sending output on 4W side

D : RX receiving input on 4W side

E : TTX teletaxe signal input

R_{GIN} : low level ringing signal input.

TEST CIRCUITS

Figure 1 : Symmetry to Ground.

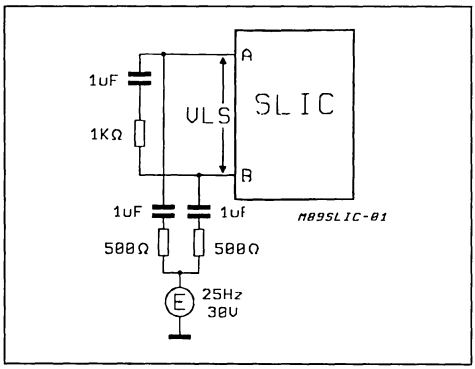
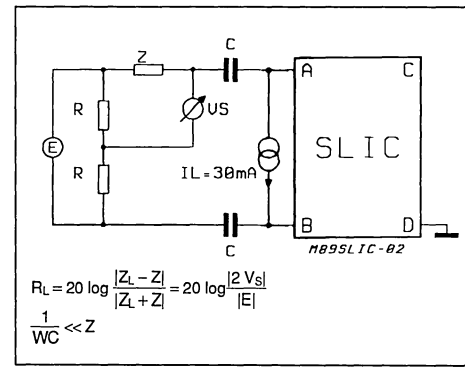


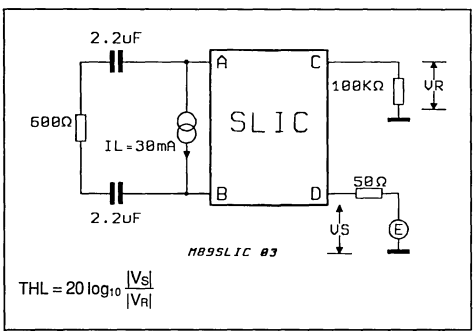
Figure 2 : 2W Return Loss.



$$R_L = 20 \log \frac{|Z_L - Z|}{|Z_L + Z|} = 20 \log \frac{|2\,V_S|}{|E|}$$

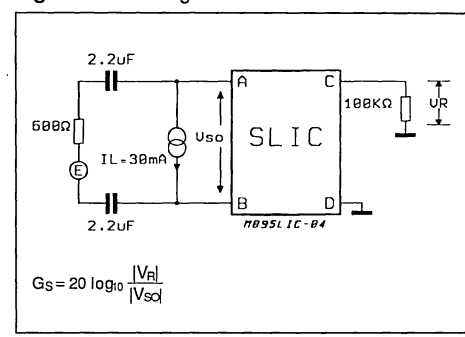
$$\frac{1}{WC} \ll Z$$

Figure 3 : Trans-hybrid Loss.



$$THL = 20 \log_{10} \frac{|V_S|}{|V_R|}$$

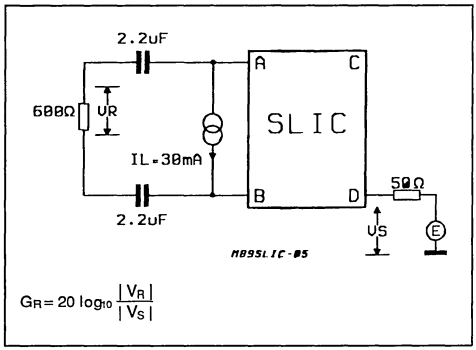
Figure 4 : Sending Gain.



$$G_S = 20 \log_{10} \frac{|V_R|}{|V_{SO}|}$$

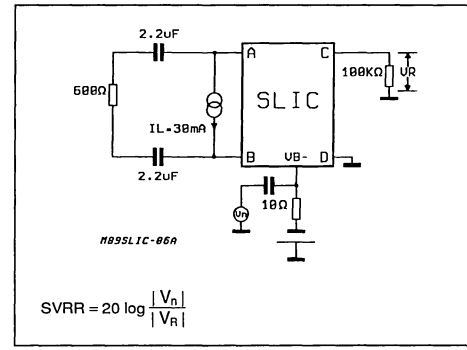
TEST CIRCUITS (continued)

Figure 5 : Receiving Gain.



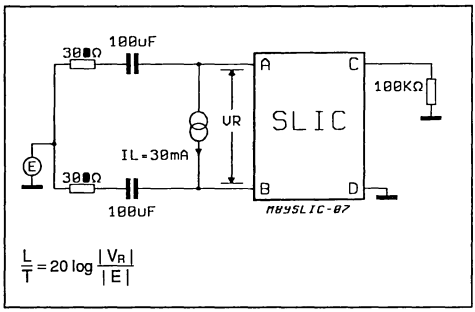
$$G_R = 20 \log_{10} \frac{|V_R|}{|V_S|}$$

Figure 6 : SVRR Relative to Battery Voltage VB–.



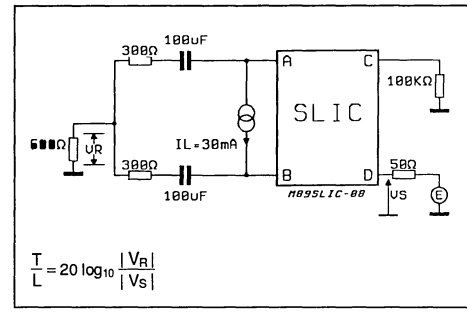
$$SVRR = 20 \log \frac{|V_n|}{|V_R|}$$

Figure 7 : Longitudinal to Transversal Conversion.



$$\frac{L}{T} = 20 \log \frac{|V_R|}{|E|}$$

Figure 8 : Transversal to Longitudinal Conversion.



$$\frac{T}{L} = 20 \log_{10} \frac{|V_R|}{|V_S|}$$

Figure 9 : TTX Level at Line Terminals.

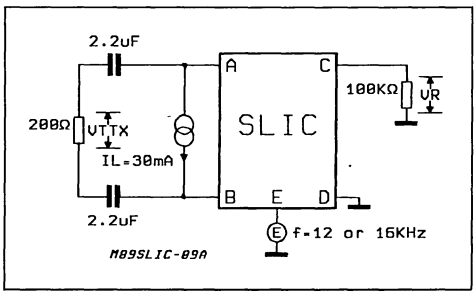
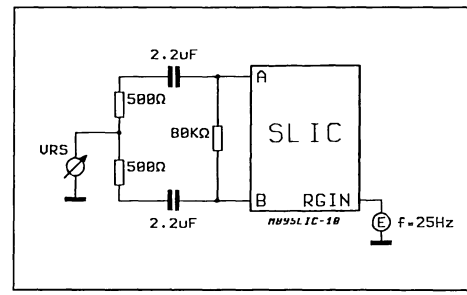


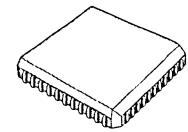
Figure 10 : Ringing Simmetry.

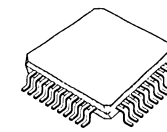


SUBSCRIBER LINE INTERFACE CIRCUIT

PRELIMINARY DATA

- MONOCHIP SILICON SLIC SUITABLE FOR PUBLIC/PRIVATE APPLICATIONS
- IMPLEMENTS ALL KEY FEATURES OF THE BORSCHT FUNCTION
- METERING PULSE INJECTION AND FILTERING WITH MINIMAL COMPONENTS COUNT (NO TRIMMING REQUIRED).
- PROTECTION RESISTOR MISMATCH COMPENSATION
- ON HOOK TRANSMISSION
- LOOP START/GROUND START FEATURE
- IND TEMP. RANGE (-40°C to +85°C)
- LOW POWER DISSIPATION IN ALL OPERATING MODES
- INTEGRATED ZERO CROSSING RELAY DRIVER
- INTEGRATED (NOISE-LESS) RING TRIP DETECTION
- VERY LOW NO. of STD TOLERANCE EXTERNAL COMPONENTS
- OPTIMIZED FOR U.S. APPLICATIONS (63dB TYP. LONG. BALANCE WITH L3035).
- SURFACE MOUNT PACKAGE (PLCC44 or PQFP44)





PLCC44 **PQFP44 (10x10)**

ORDERING NUMBERS:

L3035 L3036Q
L3036

- INTEGRATED THERMAL PROTECTION

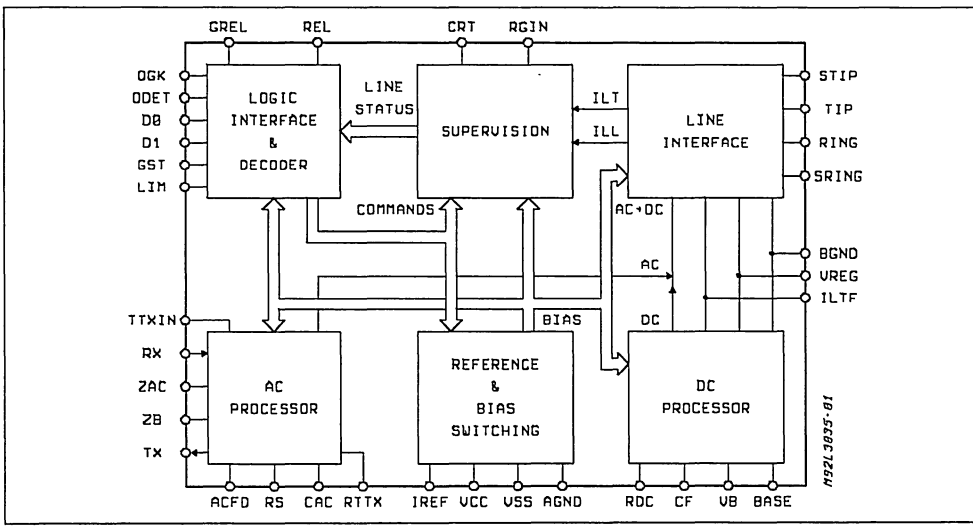
DESCRIPTION

The L3035/6 subscriber line interface circuit is a bipolar device in 70V technology developed for central office / loop carrier and private applications.

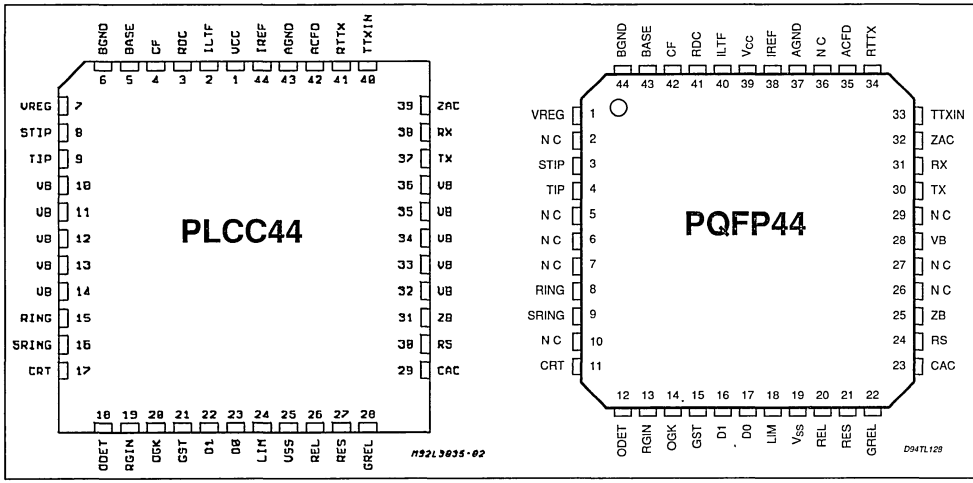
The only difference between L3035 and L3036 is that the L3035 has a better longitudinal balance performance allowing it to meet the United States BELLCORE requirements for central office/loop carrier and private applications

The SLIC integrates loop start, ground start, ground key on/off-hook, automatic ring-trip as well as zero crossing ring relay driver.

BLOCK DIAGRAM



PIN CONNECTIONs (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{bat}	Battery Voltage	-64 to V_{SS}+0.5	V
V_{CC}	Positive Supply Voltage (0 to 1ms) (continuous)	-0.4 to +7 -0.4 to +5.5	V V
V_{SS}	Negative Supply Voltage (0 to 1ms) (continuous)	-7 to +0.4 -5.5 to +0.4	V V
V_{agnd} - V_{bgnd}	Agnd Respect Bgnd (continuous)	-2 to +2	V
V_{REL}	Ring Relay Supply Voltage	14	V
V_{dig}	Digital I/O D0, D1, GST, LIM, ODET, OGK	-0.4 to +5.5	V
I_{dig}	Digital I/O D0, D1, GST, LIM, ODET, OGK	-3 to +3	mA
T_j	Maximum Junction Temperature	+150	°C
T_{stg}	Storage Temperature	-55 to +150	°C
Hu	Humidity	5 to 95	%

Note: In case of power on, power failure or hot insertion with V_{DD}, V_{SS} present and V_{bat} floating the Absolute Maximum Ratings can be exceeded with Vbat > V_{SS} +0.5V. In this case the power consumption of the device increases and the logic output state including relay driver are not controlled. This effect can be prevented ensuring that Vbat is always present before V_{DD} and V_{SS} or connecting one shottky diode (e.g. BAT49X or equivalent) between Vbat and V_{SS}. One diode can be shared between all the SLICs of the same line card.

OPERATING RANGE

T_{op}	Operating Temperature Range	-40 to +85	°C
V_{agnd} - V_{bgnd}	Difference between Agnd and Bgnd	-2 to +2	V
V_{CC}	Positive Supply voltage	+4.5 to +5.5	V
V_{SS}	Negative Supply Voltage	-5.5 to -4.5	V
V_{bat}	Battery Voltage	-62 to -24	V
V_{REL}	Ring Relay Supply Voltage	4 to 13	V

THERMAL DATA

Symbol	Parameter		PQFP44	PLCC44	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	75	45	°C/W

PIN DESCRIPTION

Unless otherwise specified all the diagrams in this datasheet refers to the PLCC44 Pin Connection.

PQFP44 No.	PLCC44 No.	Pin	Description
39	1	V_{CC}	Positive Power Supply (+5V)
40	2	I_{LTF}	Transversal Line Current Image ((I_A + I_B) / 200)
41	3	RDC	DC feedback input (the RDC resistor is connected from this node to I_{LTF})
42	4	CF	Battery voltage ripple rejection (C_{SVR} capacitor is connected from this node to BGND).
43	5	BASE	Driver for external transistor base
44	6	BGND	Battery ground
1	7	VREG	Regulated Voltage. Provides negative power supply for the power amplifier. (connected to emitter of the external transistor.)
3	8	STIP	Input of A power amplifier (when no compensation of ext. ptc resistor mismatch is requested it must be shorted to the TIP lead).
4	9	TIP	A line termination output (I_A is the current sourced from this pin).
28	10 to 14 32 to 36	VB	Battery Supply (All pins are internally connected together)
8	15	RING	B line termination output (I_B is the current sunk into this pin).
9	16	SRING	Input of B power amplifier (when no compensation of ext. ptc resistor mismatch is requested it must be shorted to the RING lead).
11	17	CRT	Ring trip and ground key capacitor
12	18	ODET	ON/OFF hook and RING TRIP output (when disable is internally pulled up)
13	19	RGIN	Ring input signal. (when open is internally pulled to GND)
14	20	OGK	Ground key output (when disable is internally pulled up)
15	21	GST	A open command (when open is internally pulled down)
16	22	D1	Bit 1
17	23	D0	Bit 0
18	24	LIM	Current Limitation Program. (when open is internally forced to 44mA current limitation)
19	25	V_{SS}	Negative Power Supply (-5V)
20	26	REL	Ring relay driver output
21	27	RES	Reserved should be connected to AGND.
22	28	GREL	Ground reference for ring relay driver
23	29	C_{AC}	AC feedback input (ACDC split capacitor is connected from this node to ILTF)
24	30	R_S	Protection resistors image (the image resistor is connected from this node to ACFD)
25	31	Z_B	Balance network for 2 to 4 wire conversion (the balance impedance Z_B is connecetd from this node to AGND. The Z_A impedance is connected from this node to Z_{AC})
30	37	Tx	4 wire output port (Tx output)
31	38	Rx	4 wire receiving port. (Rx input)
32	39	Z_{AC}	Rx buffer output (the AC impedance is connected from this node to ACFD)
33	40	TTXIN	Metering input port/V_{drop} programming. If not used should be connected to AGND.
34	41	RTTX	Metering cancellation network. If not used should be left open.
35	42	ACFD	AC impedance synthesis
37	43	AGND	DC and AC signal ground
38	44	I_{REF}	Voltage Reference Output
2,5 to 7, 10,26, 27, 29,36	–	N.C.	Not connected

DESCRIPTION (continued)

L3036 is available in two different package options: PLCC44 and PQFP44(10 x 10).

Two to four wire conversion is implemented by the SLIC for applications with first generation COMBO. In case of application with second generation (programmable) COMBO this function can be implemented outside saving external components.

The L3035/6 offers programmable current limitation (3 ranges), on hook transmission and low power in all operating modes, power management is controlled by a simple external low cost transistor.

Metering pulses are injected on the line via a summing node through TTXIN pin.
Metering pulse filtering is performed by means of a simple RC network with standard tolerance components. When TTX function is not used this pin must be connected to AGND. It is also possible to use this pin to modify the DC voltage drop between TIP/RING terminals and battery voltage for appications where it is important to optimize the battery voltage supply versus the signal swing.
Effects of protection resistor mismatch are compensated by a feedback loop on the final stage, allowing good longitudinal balance performance even with large tolerance protection resistors (ex: PTC).

This function allows L3035 to fully conform to BELLCORE power cross and surge tests and also meet the Longitudinal Balance Specification without using matched PTC resistors.

An integrated thermal protection circuit forces the L3035/6 into POWER DOWN (PD) mode when the junction temperature exceeds 150°C Typ.

L3035/6 is specified over a -40°C to +85°C ambient temperature range.
L3035/6 package is a surface mount 44PLCC.

FUNCTIONAL DESCRIPTION

L3035/36 is designed in 70V bipolar technology and performs the telephone line interface functions required in both C.O. and PABX environments. The full range of signal transmission, battery feed, loop supervision are performed.

Signal transmission performance is compatible with European and North American Standards and with CCITT recommendations.
Ringing, overvoltage and power cross protection are performed by means of external networks.

The signal transmission function includes both 2 to 4 wire and 4 to 2 wire conversion. The 2W termination impedance is set by means of an external impedance which may be complex. The 2 to 4 wire conversion is provided by means of an external network.

Such a network can be avoided in case of applications with COMBOII, in this case the 2 to 4 wire conversion is implemented inside the COMBOII by means of the programmable Hybal filter.

An additional input allows a metering pulse signal to be added on the line.

The DC feed resistance is programmable with one external resistor. Three different values of current limitation (25, 43, 56mA)can be selected by software through the parallel digital interface.

One external transistor reduces the power dissipation inside the L3035/6 in the presence of a short loop (limiting current region).

An additional supervisory function sets the TIP lead into high impedance state in order to allow application in ground start configurations.

The different L3035/6 operating modes are controlled by a 4bit logic interface, two additional detector outputs provide ground key detection and either hook state or ring trip detection.

SLIC OPERATING MODES

Through the L3035/6 digital interface it is possible to select 5 different SLIC operating modes:

1) Active Mode (ACT)
2) Standby Mode (SBY)
3) Tip Open Mode (TO)
4) Power Down Mode (PD)
5) Ringing Mode (RNG)

ACTIVE MODE (ACT)

This operating mode is set by the card controller when the Off-Hook condition has been recognized.

When this operating mode is selected the two output buffers (TIP/RING) can sink or source up to 100mA each. In case of Ground key or line terminals to GND the output current is limited to 15mA for the Tip wire and 30mA for the Ring wire.

As far as the DC characteristic is concerned three different feeding conditions are present:

a) Current limiting region: the DC impedance of the SLIC is very high (20Kohm) and therefore the system works like a current source. Using the L3035/6 digital interface it is possible to select the value of the limiting current:

25mA, 43mA, or 56mA.

When the device is in limiting current region the negative supply for the output buffer is fixed by the ext. transistor to a proper value higher than the real negative battery in order to reduce the power dissipated by the L3035/6 itself.

b) Resistive feed region: the characteristic is equal to a battery voltage (Vbat) in series with a resistor (typ 400ohm or 800ohm) whose value is set by one ext. resistor (see ext. components list).

c) Constant voltage region: the characteristic is equal to the battery voltage - 12V in series with the ext. protection resistors (typ 80ohm).

This voltage drop between battery and line termi-

nals for II=0 allows on-hook transmission.

Fig. 1 shows the DC characteristic in active mode. Fig. 2 shows the line current versus loop resistance

Figure 1: DC Characteristic in active mode

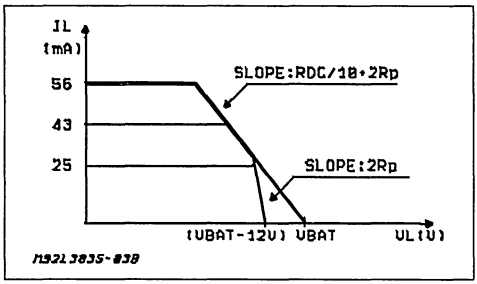
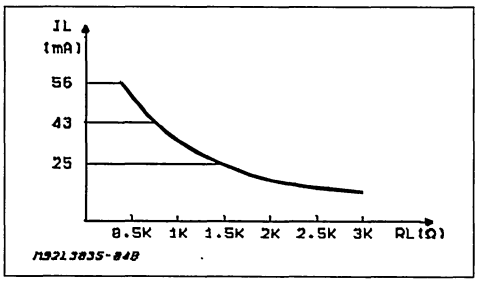


Figure 2: Current vs. Loop Resistance.
Rfeed = 2 x 200ohm,
Lim. currents: 25, 43, 56mA



In active mode the AC impedance at the line terminals is sinthetized by the external components ZAC and Rp according to the following formula:

$$Zs = ZAC/50 + 2*Rp$$

Depending on the characteristic of the ZAC network, Zs can be either a pure resistance or a complex impedance. This allows L3035/6 to meet different standards as far as return loss is concerned. The capacitor CCOMP guarantees stability to the system.

The two to four wire conversion is achieved by means of a circuit that can be represented as a Wheastone bridge, the branches of which are:

1) The line impedance (Zline)
2) The SLIC impedance at line terminals (Zs)
3) The balancing network ZA+RA connected between pin ZAC and ZB of L3035/6.
4) The network ZB between pin ZB and GND that shall copy the line impedance.

When L3035/6 is used with a second generation combo (eg TS5070FN) which is able to perform the two to four wire conversion, the two impedances ZA and ZB can be removed and the ZB pin connected to GND. The -6dB TX gain of the L3035/6 allows the echo signal to remain always within the COMBOII Hybrid balance filter dynamic range.

The injection of high frequency metering pulses is carried out through the SLIC. An unbalanced 12 or 16KHz sinusoidal signal with shaping is, when necessary, applied at the TTXIN input of the SLIC.
A fixed transfer gain is provided for the metering signal. To avoid saturation in the 4-wire side a cancellation is provided in the 4-wire transmission path.

Cancellation is obtained via an external RC network without the need for trimmed components.

When the TTX function is not used TTXIN input should be connected to GND. Since this pin is directly connected to a summing node inside the SLIC any signal applied to the TTXIN is transferred to the line with a fixed transfer gain.
In special applications, this pin can be used to modify the voltage drop (constant voltage region of DC characteristic) simply by applying a proper DC level on the TTXIN pin, allowing optimization of the battery voltage versus the maximum needed AC signal swing.

In active mode, with a -48V battery voltage, the L3035/6 dissipates 150mW for its own operation (including the power dissipation from +5/-5 supply), the dissipation related to the current supplied to the line should be added in order to get the total dissipation.

STAND-BY MODE (SBY)

In this mode the bias current of the L3035/6 is reduced and only some part of the circuit are completely active. The transversal current supplied to the line is limited at 12mA. Common mode current rejection is performed and the total current capability of the output stages (TIP and RING) is limited to 30mA. The open circuit voltage is |Vbat|-7V.

CONTROL INTERFACE

INPUTS				OPERATING MODE	OUTPUTS	
D0	D1	GST	LIM		ODET	OGK
0	0	0	X	POWER DOWN	DISABLE	DISABLE
1	1	0	X	STANDBY	OFF/HK	GDKEY
1	0	0	0	ACTIVE (25mA)	OFF/HK	GDKEY
1	0	0	HI	ACTIVE (43mA)	OFF/HK	GDKEY
1	0	0	1	ACTIVE (56mA)	OFF/HK	GDKEY
0	1	0	X	RING	RING-TRIP	DISABLE
0	0	1	X	A OPEN	OFF/HK	GDKEY

Both Off/Hook and Ground key detectors are active. Signal transmission is not operating.

In stand-by mode, with a -48V battery voltage, the L3035/6 dissipates 90mW typ. (including the power dissipation from a +5/-5V supply).
Stand-by mode is usually selected when the telephone is in on-hook condition. It allows a proper off-hook detection, even in the presence of high common mode currents, or with telephone sets sinking a few milliamperes of line current in on-hook condition.

TIP OPEN MODE (TO)

This mode is selected when the SLIC is adopted in a system using the Ground start feature. In this mode the TIP termination is set in High Impedance (100Kohm) while the RING termination is active and fixed at Vbat + 4.5V. In the case of connection of RING termination to GND the sinked current is limited to 30mA. When RING is connected to GND both off-hook and ground-key detectors become active.

Power dissipation in this mode with a -48V battery voltage is 100mW (including the power dissipation from +5/-5V supply).

POWER DOWN MODE (PD)

In this mode, both TIP and RING terminations are open and no current is fed into the line.

The power dissipation is very low.

This mode is usually selected in emergency conditions or when the connected line is disabled.

This is also the mode into which the SLIC is automatically forced, in the case of thermal overload $T_j > 150°C$ typ.

RINGING MODE (RNG)

When this mode is selected the ringing signal is injected on the line via the ext relay activated by the L3035/6 relay driver.

When the ringing signal phase is provided at the RGIN pin, the relay command is also synchronized with the ringing signal zero crossing.

The TIP and RING termination of the L3035/6 also senses the line current which is then integrated on the CRT capacitor.

TIP pin voltage is fixed at – 2.5V, RING pin voltage is fixed at V_{BAT} + 4.5V, TIP, RING buffer current capability is limited to 100mA.

When off-hook occurs during ringing burst the voltage on CRT increase above a proper threshold and ring trip is detected.

Once ring trip is detected the ringing signal is automatically disconnected at the first zero crossing. When the ringing signal phase is not provided at the RGIN pin the ringing signal is disconnected immediately after ring trip detection.

EXTERNAL COMPONENTS LIST

To set the SLIC into operation the following parameters have to be defined:

- The DC feeding resistance "Rfeed" defined as the resistance of the traditional feeding system (most common Rfeed values are: 400, 800, 1000 ohm).
- The AC SLIC impedance at line terminals "Zs" to which the return loss measurements is referred. It can be real (typ. 600ohm) or complex.
- The equivalent AC impedance of the line "Zl" used for evaluation of the trans-hybrid loss performance (2/4wire conversion). It is usually a complex impedance.
- The value of the two protection resistors Rp in series with the line termination.
- The line impedance at the TTX freq. Zlttx.

Once, the above parameters are defined, it is possible to calculate all the external components using the following table.
The typical values has been obtained supposing:

- Rfeed = 400Ω
- Zs = 600Ω
- Zl = 600Ω
- Rp = 40Ω
- Zlttx = 216Ω + 120nF @ 12KHz
- Re[Zlttx] = 216Ω
- Im[Zlttx] = -110Ω @12KHz

EXTERNAL COMPONENTS

Name	Function	Formula	Typ. Value
CVB	Battery Filter		330nF 20% 63VI
CVDD	Positive Supply Filter		100nF 20%
CVSS	Negative Supply Filter		100nF 20%
RREF	Internal Current Reference		23.7K 1%
CSVR	Battery Ripple Rejection	CSVR = 1/(6.28 * fp * 150K) @ fp = 1.6Hz	680nF 20% 60VI
CRT	Ring Trip & Ground-key Capacitor	CRT = (25/f_{RING}) · 390nF	390nF 20% 6VI
RDC	DC Feeding Resistance	RDC = 10 * (Rfeed - 2Rp)	3.2K 1%
CAC	AC/DC Splitter	CAC = 1 / (6.28 * fsp * RDC) @ fsp = 10Hz	4.7µF 20% 15VI
RS	Protection Resistor Image	RS = 50 * 2RP	4K 1%
ZAC	2 Wire AC Impedance	ZAC = 50 * (Zs-2Rp)	26K 1%
ZA (1)	SLIC Impedance Balancing Network	ZA = 50 * (Zs-2Rp)	26K 1%
RA (1)	SLIC Impedance Balancing Network	RA = 50 * 2Rp	4K 1%
ZB (1)	Line Impedance Balancing Network	ZB = 50 * Zl	30K 1%
CCOMP	AC Feedback Compensation	CCOMP = 1 / [2ΠIfo (100 Rp)] @ fo = 250KHz	220pF 20%
CH (1)	Trans-hybrid Loss Frequency Compensation	CH = CCOMP	220pF 20%
RF	Feeding Resistance for Ring Inj.	≥ 200Ω (7)	200Ω 2W
RT	Feeding Resistance for Ring Inj.	≥ 200Ω (7)	200Ω 2W
RRG	Ring Input Resistor	RRG = (V_{RING}/25µA)cos[-2·f_{RING} · T · 180] (4)	4MΩ 5%
CRG	Ring Input Capacitor	CRG = 25µA/(V_{RING} · sin[2 · f_{RING}·T · 180] · 2Πf_{RING}) (4)	3.9nF 20% 100V
PTC (2)	Positive Temp. Coeff. Resistor	< 15Ω	10Ω
RST (2)	Tip Buffer Sensing Resistor	10 to 50KΩ	33K 1W 5% (6)
RSR (2)	Ring Buffer Sensing Resistor	10 to 50KΩ	33K 1W 5% (6)
QEXT	External Transistor (3)		(*)
Rp	Protection Resistor	30 to 80Ω (8)	40Ω
RTTX	Teletax Cancellation Resistor	RTTX = 21.5 · [Re (Zlttx) +2Rp] (5)	6.34K 1%
CTTX	Teletax Cancellation Capacitor	CTTX = 1/(21.5 · [-Im(Zlttx) · fttx · 6.28]) (5)	5.6nF 20%
D1	Relay Kickback Clamp Diode		1N4148

Notes:

(1) These components can be removed and ZB pin shorted to GND when 2/4wire conversion is implemented with 2nd generation COMBO (EG. TS5070FN)

(2) In case there is no necessity to recover the unbalance introduced by PTC tolerance pins TIP and STIP can be shorted togheter as pins RING and SRING. In this case also the R_P Resistor should be splitted in two parts keeping at least 20Ω between TIP/RING terminals and protection connection. In this case PTC or fuse resistor (if used) can be placed in series to Rp

(3) Transistor characteristic.
P_{DISS} = 1W (typ. depending on application)
$h_{FE} \geq 25$; $I_C \geq 100mA$; $V_{CEO} \geq 60V$; $f_T \geq 15MHz$.

(4) V_{RING}: Max Ring Generator Voltage, f_{RING}: Ring Frequency, T: relay response time.
Typical value obtained for V_{RING} = 100Vrms, f_{RING} = 25Hz; T = 2.5ms.

(5) Defining RTTX + CTTX = ZTTX, RTTX and CTTX can also be calculated from the following formula: $Z_{FTTX} = 21.5$ [Zlttx + 2Rp].

(6) RST and RSR wattage should be calculated according to the power cross test specification (When PTC become open circuit the entire power cross voltage will appear across RSR and RST).

(7) In order to optimize the component count it is also possible to use only one resistor in series to the ringing generator. In this case RT = 0Ω, RF≥ 400Ω (RF typ. value = 400Ω).

(8) Suggested Rp type are 2W wire wound resistors or thick film resistors on ceramic substrate.
Fuse function should be included if PTC are not used.

(*) ex: BD140; MJE172;MJE350....(SOT32 or SOT82 package available also for surface mount).
For low power application (reduced battery voltage) BCP53 (SOT223 surface mount package) can be used

Figure 3: Typical Application Circuit including all features.

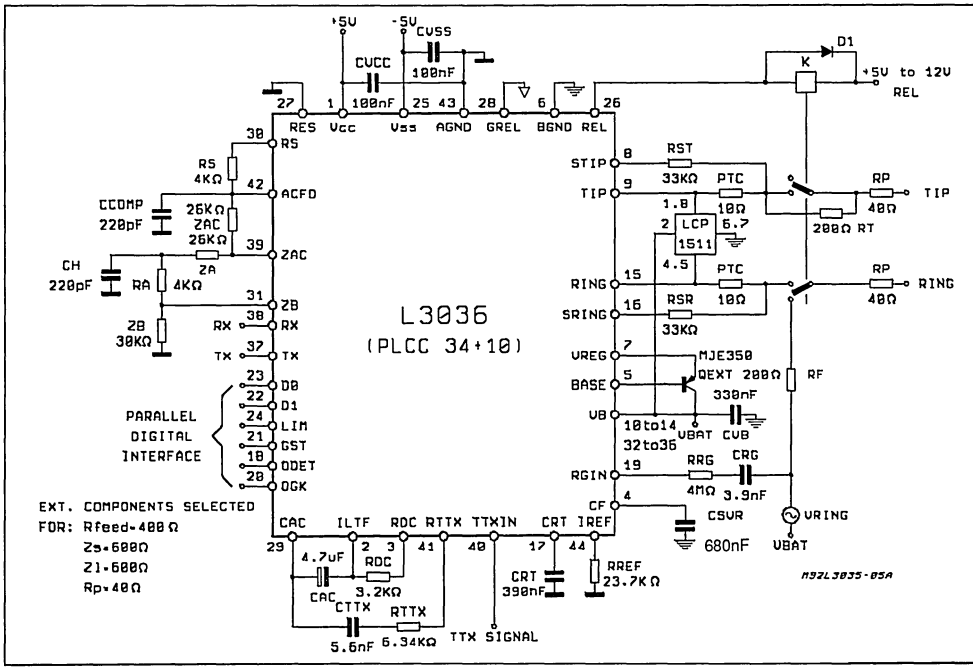
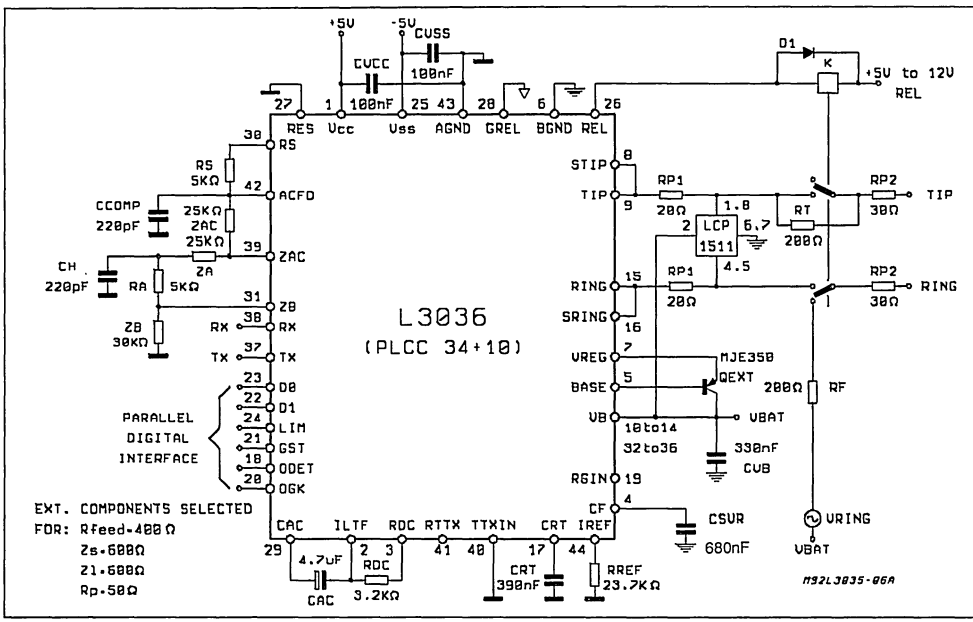


Figure 4: Typical Application circuit with minimum components count (NoTTX/No zero crossing sync/no PTC mismatch compensation).



In case of U.S. application based on L3035 the external components can be calculated supposing:

- Rfeed = 400Ω
- Zs = 900Ω + 2.12µF
- ZI = 1650Ω// (100Ω + 5nF) Loaded Line
- ZI = 800Ω// (100Ω + 50nF) Not Loaded Line
- Rp = 62Ω

EXTERNAL COMPONENTS (for US. Application)

Name	Function	Formula	Typ. Value
CVB	Battery Filter		330nF 20% 63VI
CVDD	Positive Supply Filter		100nF 20%
CVSS	Negative Supply Filter		100nF 20%
RREF	Internal Current Reference		23.7K 1%
CSVR	Battery Ripple Rejection	CSVR = 1/(6.28 * fp * 150K) @ fp = 1.6Hz	680nF 20% 60VI
CRT	Ring Trip & Ground-key Capacitor	CRT = (25/f_{RING}) · 390nF	390nF 20% 6VI
RDC	DC Feeding Resistance	RDC = 10 * (Rfeed - 2Rp)	2.76K 1%
CAC	AC/DC Splitter	CAC = 1 / (6.28 * fsp * RDC) @ fsp = 10Hz	4.7µF 20% 15VI
RS	Protection Resistor Image	RS = 50 * 2RP	6.2K 1%
ZAC	2 Wire AC Impedance	ZAC = 50 * (Zs-2Rp) (7)	39K + (180K//55nF)
ZA (1)	SLIC Impedance Balancing Network	ZA = 50 * (Zs-2Rp) (7)	39K + (180K//55nF)
RA (1)	SLIC Impedance Balancing Network	RA = 50 * 2Rp	6.2K 1%
ZB (1)	Line Impedance Balancing Network	ZB = 50 * ZI	82.5K + (5K + 100pF) (3) 40K + (5K + 1nF) (4)
CCOMP	AC Feedback Compensation	CCOMP = 1 / [2Πfo (100 Rp)] @ fo = 250KHz	100pF 20%
CH (1)	Trans-hybrid Loss Frequency Compensation	CH = CCOMP	100pF 20%
RF	Feeding Resistance for Ring Inj.	≤ 200Ω (9)	200Ω 2W
RT	Feeding Resistance for Ring Inj.	≤ 200Ω (9)	200Ω 2W
RRG	Ring Input Resistor	RRG = (V_{RING}/25µA)cos[-2·f_{RING} · T · 180] (6)	4MΩ 5%
CRG	Ring Input Capacitor	CRG = 25µA/(V_{RING} · sin[2 · f_{RING}·T · 180] · 2Πf_{RING} (6)	3.9nF 20% 100V
PTC (2)	Positive Temp. Coeff. Resistor	< 15Ω	10Ω
RST (2)	Tip Buffer Sensing Resistor	10 to 50KΩ	33K 1W 5% (8)
RSR (2)	Ring Buffer Sensing Resistor	10 to 50KΩ	33K 1W 5% (8)
QEXT	External Transistor (5)		(*)
Rp	Protection Resistor	30 to 80Ω (10)	62Ω
D1	Relay Kickback Clamp Diode		1N4148

Notes:

(1) These components can be removed and ZB pin shorted to GND when 2/4wire conversion is implemented with 2nd generation COMBO (EG. TS5070FN)

(2) In case there is no necessity to recover the unbalance introduced by PTC tolerance pins TIP and STIP can be shorted togheter as pins RING and SRING. In this case also the R_P Resistor should be splitted in two parts keeping at least 20Ω between TIP/RING terminals and protection connection In this case PTC or fuse resistor (if used) can be placed in series to Rp.

(3) Loaded Line.

(4) Not Loaded Line.

(5) Transistor characteristic: P_{DISS} = 1W (typ. depending on application); h_{FE} ≥ 25; I_C ≥ 100mA; V_{CEO} ≥ 60V; f_T ≥ 15MHz.

(6) V_{RING}: Max Ring Generator Voltage, f_{RING}: Ring Frequency, T: relay response time. Typical value obtained for V_{RING} = 100Vrms, f_{RING} = 25Hz; T = 2.5ms.

(7) For details see AN496.

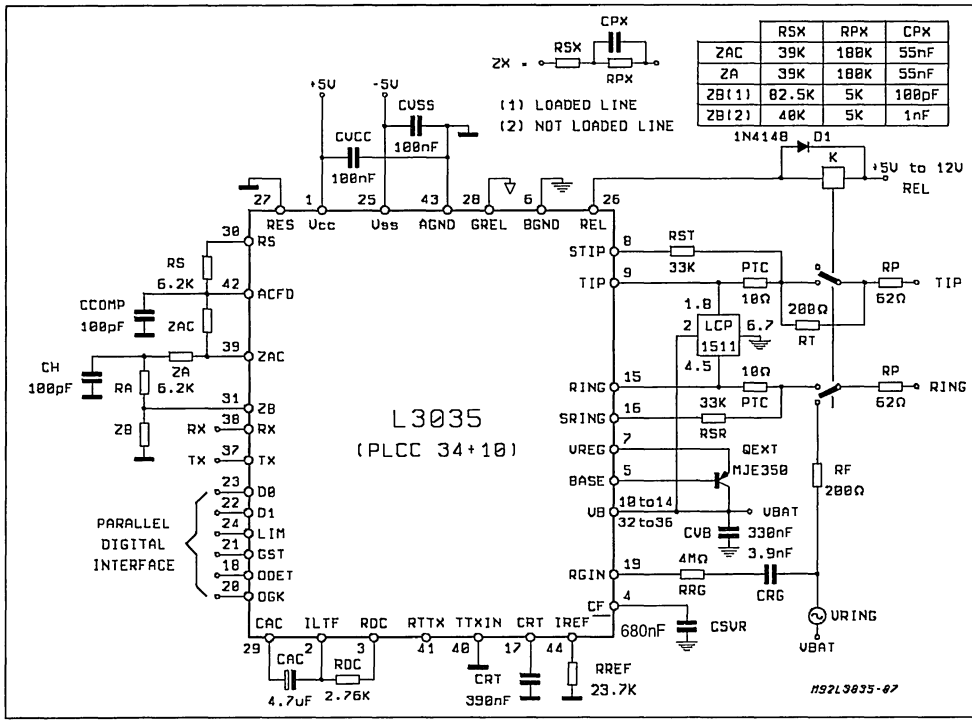
(8) RST and RSR wattage should be calculated according to the power cross test specification. (When PTC become open circuit the entire power cross voltage will appear across RSR and RST).

(9) In order to optimize the component count it is also possible to use only one resistor in series to the ringing generator. In this case RT = 0Ω; RF≥ 400Ω (RF typ. value = 400Ω).

(10) Suggested Rp type are 2W wire wound resistors or thick film resistors on ceramic substrate. Fuse function should be included if PTC are not used

(*) ex: BD140; MJE172;MJE350....(SOT32 or SOT82 package available also for surface mount).
For low power application (reduced battery voltage) BCP53 (SOT223 surface mount package) can be used.

Figure 5: Typical Application Circuit for U.S. Application.



	RSX	RPX	CPX
ZAC	39K	100K	55nF
ZA	39K	100K	55nF
ZB(1)	82.5K	5K	100pF
ZB(2)	40K	5K	1nF

ELECTRICAL CHARACTERISTICS TEST CONDITION, unless otherwise specified: V_{CC} = 5V; V_{SS} = -5V; V_{BAT} = -48V; AGND = BGND; T_A = 25°C.

Note: Testing of all parameter is performed at 25°C. Characterization as well as the design rules used allow correlation of tested performances at other temperatures. All parameters listed here are met in the range 0°C to +70°C. Additional selection (on request ordering part #: L3035/6T) can be performed so that the functionality between -40°C and 85°C is verified.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
INTERFACE REQUIREMENTS 2 WIRE PORT						
V_{ab}	Overload Level Voice Signal	Rp +PTC = 50Ω 300Hz to 3.4KHz (*)	4.1			Vpk
Z_{II}	Long Input Impedance	at SLIC terminals per wire			10	Ω
I_{II}	Long Current Capab. ac	standby per wire (on HOOK)	17			mApk
		active per wire (on HOOK)	17			mApk
I_{II}	Longitudinal Current Capability	active per wire off HOOK (IT = Transversal current)	75-I_T			mApk
4 WIRE TRANS PORT						
V_{tx}	Overload Level		1.8			Vpk
V_{toff}	Output Offset Voltage		-350		350	mV
Z_{tx}	Output Impedance				10	Ω

(*) At TIP/RING line connection with Z_{LINE} (AC) = 600Ω. For any DC Loop current from 0mA to I_{LIM}

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
4 WIRE RECEIVE PORT						
Z_{RX}	Input Impedance		100			KΩ
V_{RX}	Overload Level		3.2			Vpk
METERING INPUT PORT						
Z_{MIN}	Input Impedance		100			KΩ
LOGIC CONTROL PORT INPUT D0, D1, GST						
V_{ih}	Input High Voltage		2			V
V_{il}	Input Low Voltage				0.8	V
I_{ih}	Input High Current		-10		90	µA
I_{il}	Input Low Current		-10		10	µA
C_{in}	Input Capacitance				10	pF
INPUT LIM						
V_{ih}	Input High Voltage		2.4			V
V_{il}	Input Low Voltage				0.4	V
I_{ih}	Input high Current		-10		30	µA
I_{il}	Input Low Current		-30		10	µA
C_{in}	Input Capacitance				10	pF
OUTPUT DET						
V_{ol}	Output Low Voltage	I_o = 1.5mA			0.4	V
V_{oh}	Output High Voltage	I_o = 30µA I_o ≤10µA	2.4 3.8			V V
C_{ld}	Load Capacitance				150	pF
RINGING INPUT PORT						
	Overload Level		-0.5		0.5	V
	Input Impedance		50		90	KΩ
	Offset Voltage Allowed		-15		15	mV

TRANSMISSION PERFORMANCE

Arl	Return Loss (2-wire)	300Hz to 3.4KHz	22			dB
Thl	Transhibrid Loss	300Hz to 3.4KHz $20\log_{10} \lvert \frac{V_{RX}}{V_{TX}} \rvert$	30			dB
Longitudinal balance (CCITT Rec.0.121)						
L-T	Longit to Transversal	300Hz to 3.4KHz Zs = 600Ω Rp = 40Ω, 1% tolerance	52			dB
L-4	Long Sign Rejection		58			dB
T-L	Transvers to Longit		49			dB
4-L	Long Sign Generation		49			dB
L3035 Longitudinal balance (IEEE Std 455-1976)						
L – T	Longitudinal to Transversal	300Hz to 3.4KHz Z_S = 900Ω + 2.12µF R_P = 62Ω, 1% match	58	63		dB
L – 4	Longitudinal Signal Rejection			70		dB

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
INSERTION LOSS						
G_t	Transmit V Gain	0dBm, 1KHz	-6.25		-5.79	dB
G_r	Receive V Gain		-0.2		0.2	dB
INSERTION LOSS vs. FREQUENCY (rel 1KHz / 0dBm)						
G_t	Transmit V Gain	0.3 to 3.4KHz	-0.1		0.1	dB
G_r	Receive V Gain		-0.1		0.1	dB
METERING INJECTION						
G_{TTX}	Transfer Gain	V_{TTXIN} = 0.66Vrms Z_L =200Ω; $2 \cdot R_P = 80\Omega$; $V_{moff} = 0$	3.18		3.51	
THD	Harmonic Distortion				3	%
GAIN LINEARITY (rel 1KHz, -4dBm)						
G_t	Transmit V Gain	-55dBm to 7dBm (1)	-0.1		0.1	dB
G_r	Receive V Gain		-0.1		0.1	dB
GROUP DELAY (2-4, 4-2) 0DbM						
T_{gABS}	Absolute	3KHz		5		µs
T_{gDIS}	4 to 2-wire	0.5 to 3,4KHz		5		µs
TOT HARMONIC DISTORTION						
Thd4	2 to 4-wire	7dBm, 0.3 to 3.4KHz			-46	dB
Thd2	4 to 2-wire				-46	dB
IDLE CHANNEL NOISE						
Vabp	2-wire port	psophometric		-78	-72	dBmP
Vtxp	4-wire transmit	psophometric		-82	-76	dBmP
Vabc	2-wire port	c message		12	18	dBrnC
Vtxc	4-wire transmit	c message		8	14	dBrnC

RINGING FUNCTION

0 cross	Zero Crossing Threshold Level	f_{RING} = 16 to 66Hz R_{GIN} = 3Vrms	-70		70	mV
I_{RT}	Ring Trip Threshold			7.5		mA DC
T_{RTD}	Ring Trip Detection Time	R_L = 1.8k, f_{RING} = 25Hz			150	ms

BATTERY FEED CHARACTERISTIC

POWER DOWN STATE						
I_{LGND}	Loop Current	TIP or RING to BGND			0.5	mA
I_{LBAT}	Loop Current	TIP or RING to V_{bat}			0.5	mA
I_L	Loop Current	R_L = 0			1	mA
STAND BY STATE						
I_l	Iloop Accuracy	constant region	11		15	mA
V_{LOS}	Line Voltage	@ I_L = 0	40		42	V
ACTIVE STATE						
V_{LO}	Line Voltage	@ I_L = 0	34.5		37.5	V
R_{feed}	Feeding Resistance Accuracy		-10		10	%
I_{lim}	Loop Current Limit Accuracy	I_{lim} = 25mA, 43mA, 56mA	-8	I_{lim}	8	%
GROUND START STATE						
Z_{TIP}	Tip Lead Impedance		100			KΩ
I_{GS}	Ring Lead Current	RING to GND		30		mA

(1): For level lower than -40dBm guaranteed by correlation.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DETECTORS						
OFF HOOK DETECTOR						
I_{det}	Off-hook Current Threshold	stand by state	9		12	mA
I_{det}	Off-hook Current Threshold	active state	9		12	mA
Hys	Off-hook / On-hook Hysteresys	Both stand by and active state	1		1.6	mA
Td	Dialling Distortion	active state	-1		1	ms
GROUND KEY DETECTOR						
I_{LL}	Ground Key Current Threshold $I_{LL} = (I_B - I_A) / 2$	TIP to RING to GND or RING to GND		4		mA
POWER DISSIPATION ON L3035/36 at V_{BAT} = 48V						
P_d	Power Down	any line lenght			38	mW
P_d	Stand-by	2-wire open R_L = 0 to 2K		95	136 220	mW mW
P_d	Active, R_{feed} = 800Ω I_{LIM} = 25mA I_{LIM} = 43mA I_{LIM} = 56mA	2-wire open R_L = 0 to 2K R_L = 0 to 2K R_L = 0 to 2K		155	224 710 1690 2710	mW mW mW mW
P_d	Active, Rfeed = 400Ω I_{LIM} = 25mA I_{LIM} = 43mA I_{LIM} = 56mA	2-wire open R_L = 0 to 2K R_L = 0 to 2K R_L = 0 to 2K		155	224 510 850 1300	mW mW mW mW
P_d	Active	Ground Key		1500		mW
POWER DISSIPATION ON QEXT AT V_{bat} = 48V						
P_{dq}	Active, R_{feed} = 800Ω I_{LIM} = 25mA I_{LIM} = 43mA I_{LIM} = 56mA	 R_L = 0 to 2K R_L = 0 to 2K R_L = 0 to 2K			 880 790 430	 mW mW mW
P_{dq}	Active, Rfeed = 400Ω I_{LIM} = 25mA I_{LIM} = 43mA I_{LIM} = 56mA	 R_L = 0 to 2K R_L = 0 to 2K R_L = 0 to 2K			 1080 1580 1700	 mW mW mW
SUPPLY CURRENTS						
ANALOG SUPPLY						
I_{CC}	V_{CC}	Power Down		1.5	2.2	mA
I_{SS}	V_{SS}	Power Down		0.1	0.5	mA
I_{CC}	V_{CC}	Stand-by/ A open		4	5	mA
I_{SS}	V_{SS}	Stand-by/ A open		1.5	3	mA
I_{CC}	V_{CC}	Active		6	10	mA
I_{SS}	V_{SS}	Active		3	6	mA
BATTERY SUPPLY						
I_{bat}	Power down	a or b to BGND		120	500	µA
I_{bat}	Stand-by/ A open	2-wire open		1.4	2	mA
I_{bat}	Active	2-wire open 2-wire R_L = 400Ω		2.3	3 I_{l}+5	mA mA

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
POWER SUPPLY REJECTION (V_{RIPPLE} = 100mVrms)						
LINE TERMINALS						
PSRR	V_{CC} ref to AGND	50Hz to 3.4KHz	20			dB
PSRR	V_{SS} ref to AGND		20			dB
PSRR	V_{bat} ref to AGND		30			dB
PSRR	BGND ref to AGND		20			dB
RELE DRIVER						
i_{RD}	Current Capability		40			mA
V	Voltage Drop	@I_{RD} = 40mA			1.25	V
i_{LK}	Off Leakage Current				100	µA

Figure 6: Test Circuit

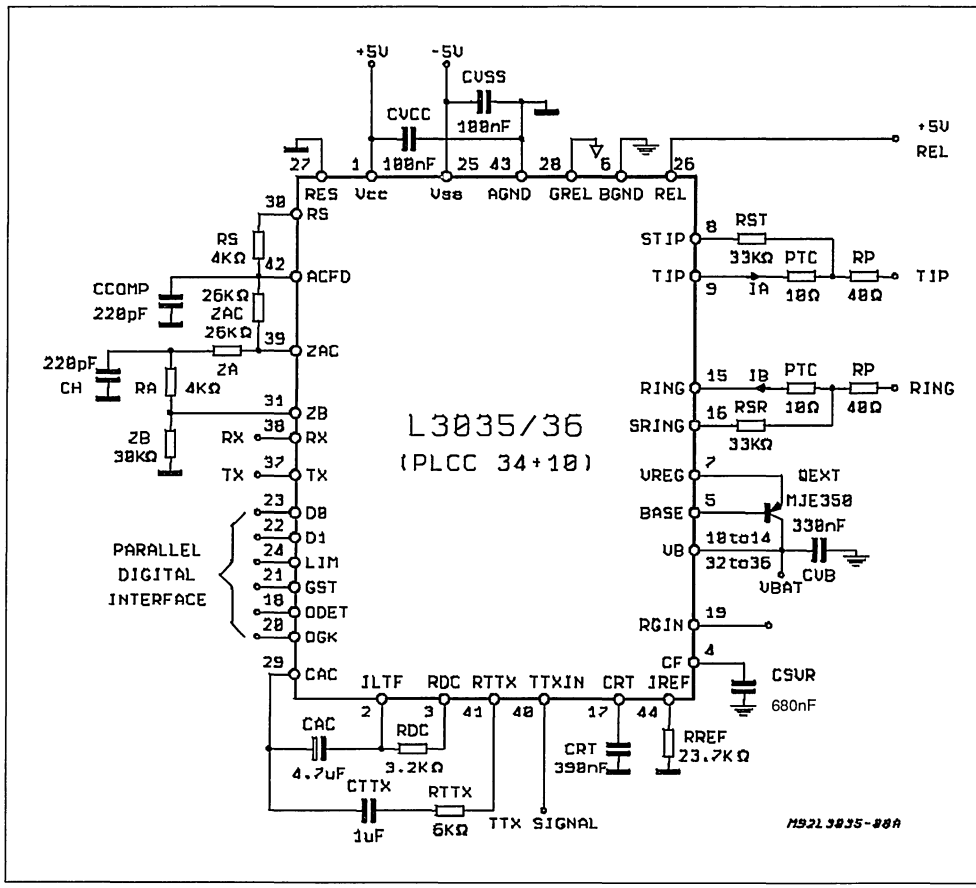


Figure 7: Typical Application with 2nd Generation COMBO (600Ω Application)

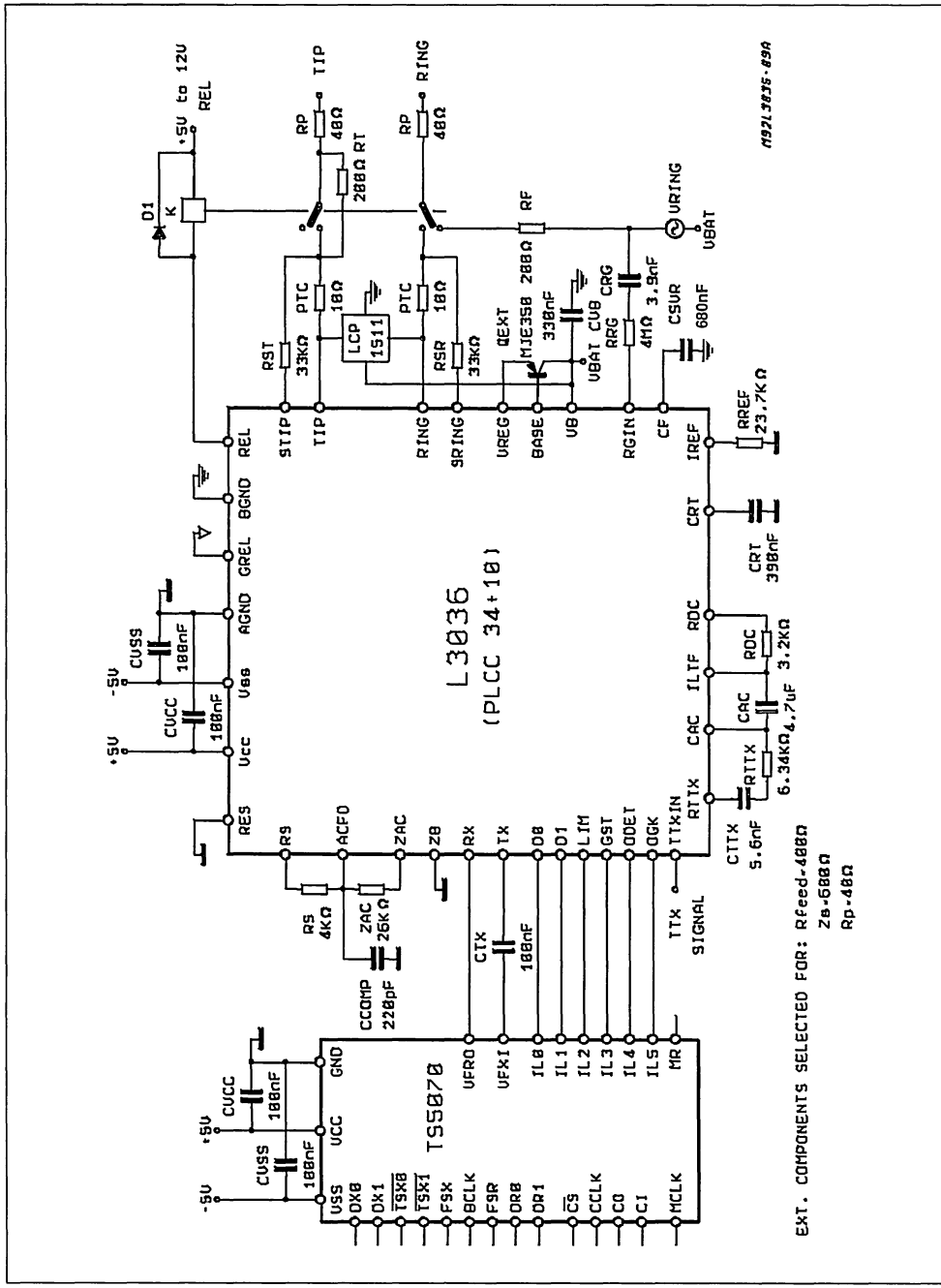


Figure 8: Typical Application with 1st Generation COMBO (600Ω Application)

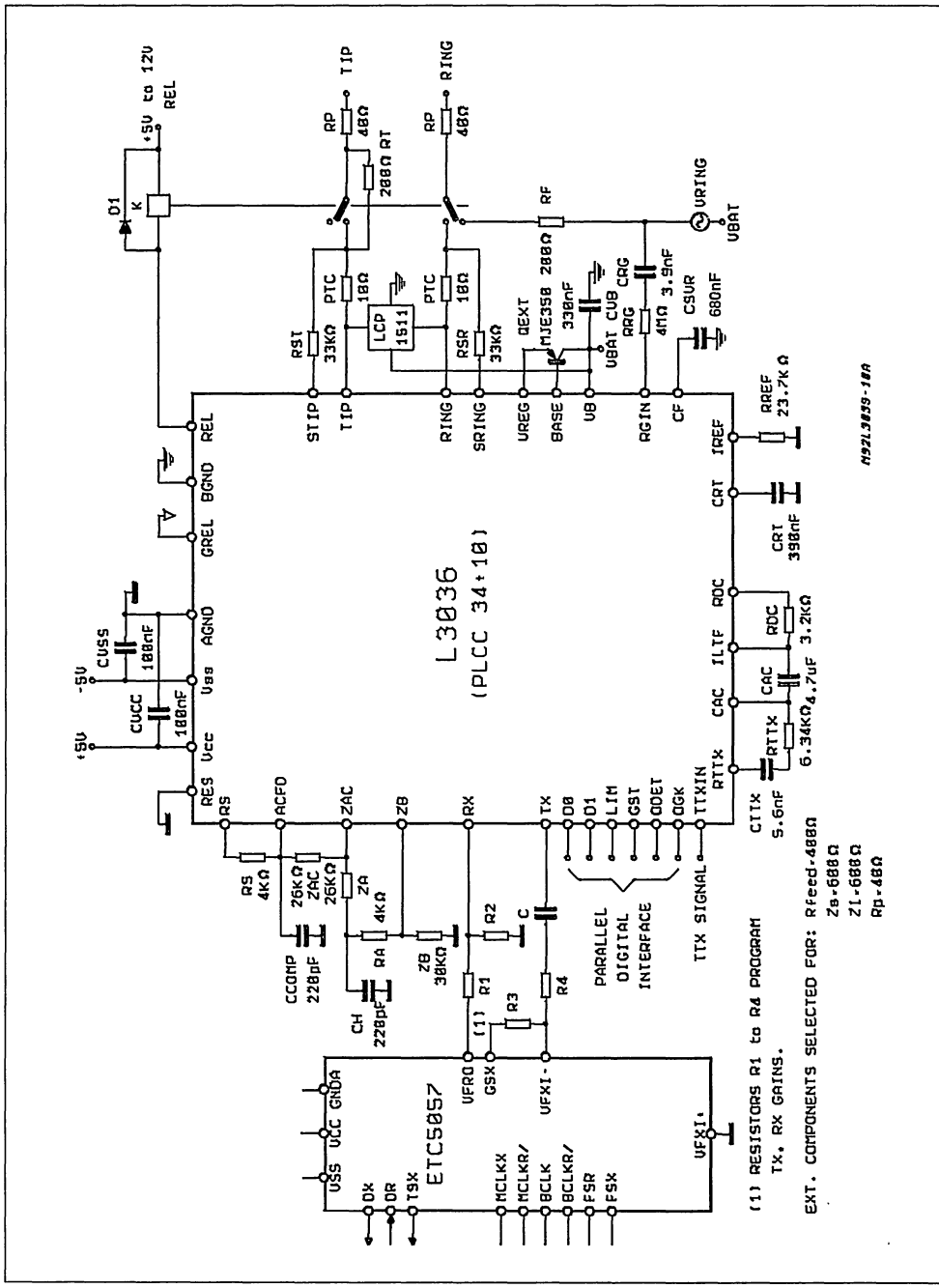


Figure 9: Typical Application with 2nd Generation COMBO (U.S. Application)

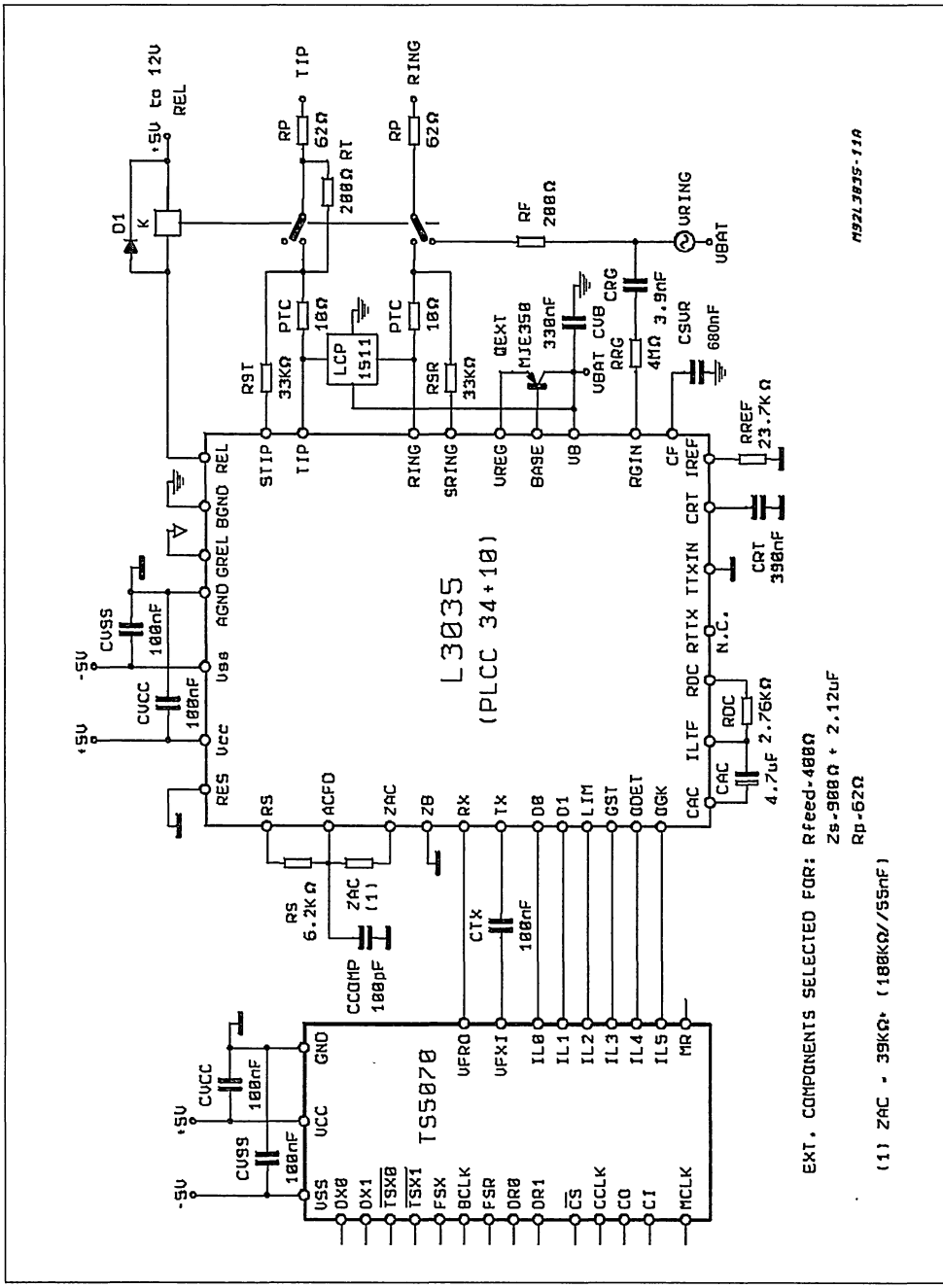
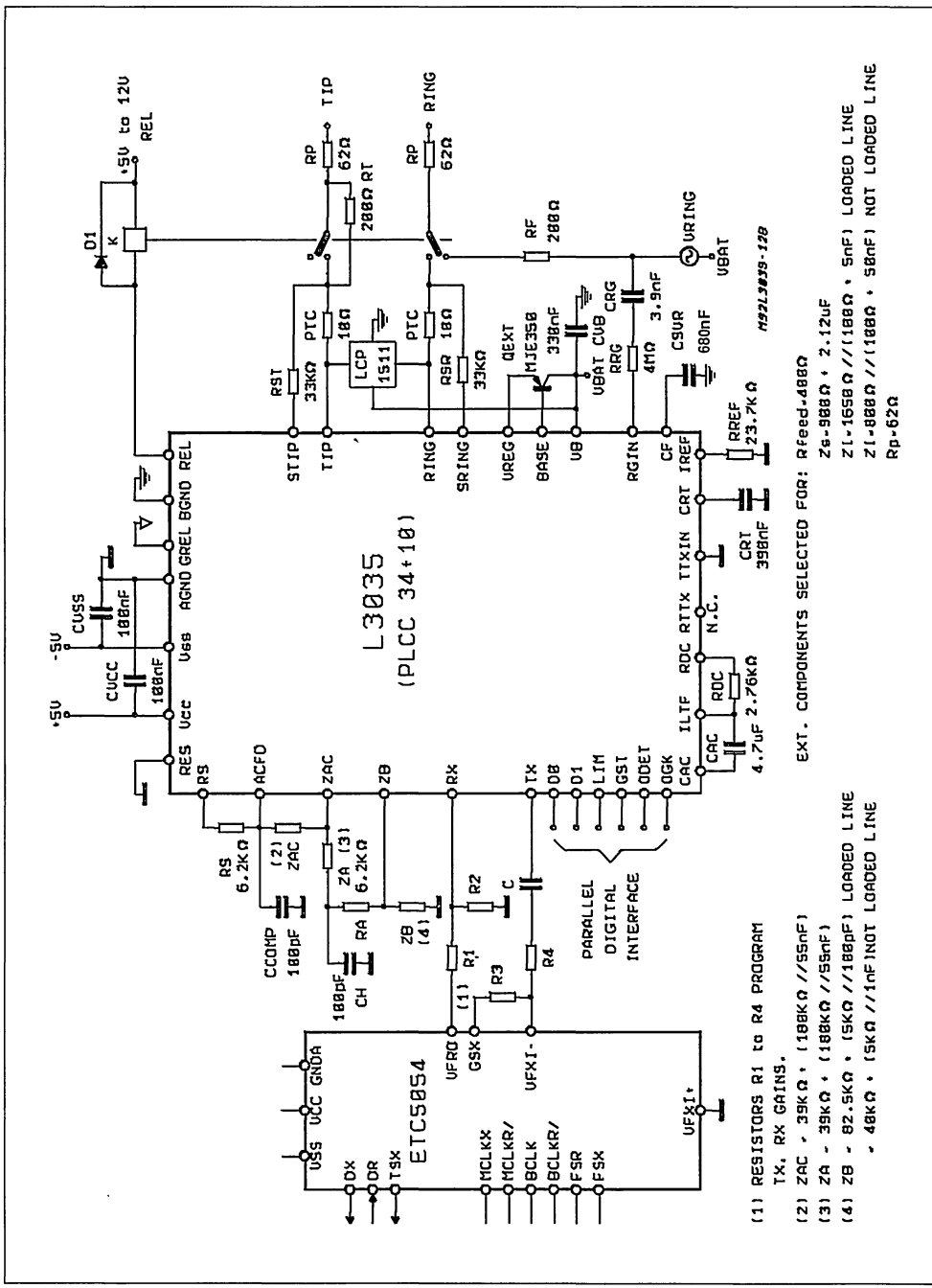


Figure 10: Typical application with 1st Generation COMBO (U.S. Application)



SUBSCRIBER LINE INTERFACE CIRCUIT

PRELIMINARY DATA

- MONOCHIP SILICON SLIC SUITABLE FOR PUBLIC/PRIVATE APPLICATIONS
- IMPLEMENTS ALL KEY FEATURES OF THE BORSCHT FUNCTION
- SOFT BATTERY REVERSAL WITH PROGRAMMABLE TRANSITION TIME (3 to 100ms)
- METERING PULSE INJECTION AND FILTERING WITH MINIMAL COMPONENTS COUNT (NO TRIMMING REQUIRED).
- PROTECTION RESISTOR MISMATCH COMPENSATION
- ON HOOK TRANSMISSION
- LOOP START/GROUND START FEATURE
- IND TEMP. RANGE:
  – L3037 0°C TO 70°C
  – L3037T -40°C to +85°C
- LOW POWER DISSIPATION IN ALL OPERATING MODES
- INTEGRATED ZERO CROSSING RELAY DRIVER
- INTEGRATED (NOISE-LESS) RING TRIP DETECTION
- VERY LOW NO. of STD TOLERANCE EXTERNAL COMPONENTS
- SELECT PART FOR U.S. APPLICATIONS (63dB TYP. LONG. BALANCE)

PLCC44 **PQFP44(10 x 10)**

ORDERING NUMBERS:

L3037FN L3037QN

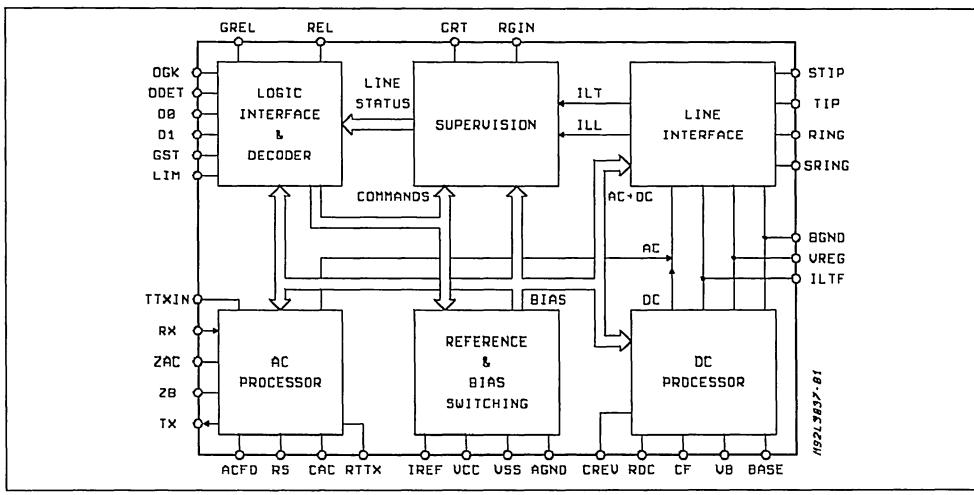
- SURFACE MOUNT PACKAGE (PLCC44 or PQFP44)
- INTEGRATED THERMAL PROTECTION
- PIN TO PIN COMPATIBLE WITH L3035/36

DESCRIPTION

The L3037 subscriber line interface circuit is a bipolar device in 70V technology developed for central office / loop carrier and private applications.

The L3037 is pin to pin and function compatible with L3035/36. One particular pin (reserved in L3035/36) is now used for reverse polarity transition time programming. The line polarity transition is not affecting the AC signal transmission that can continue also during the line voltage transition.L3037 is available in two different package options: PLCC44 and PQFP44 (10 x 10mm).

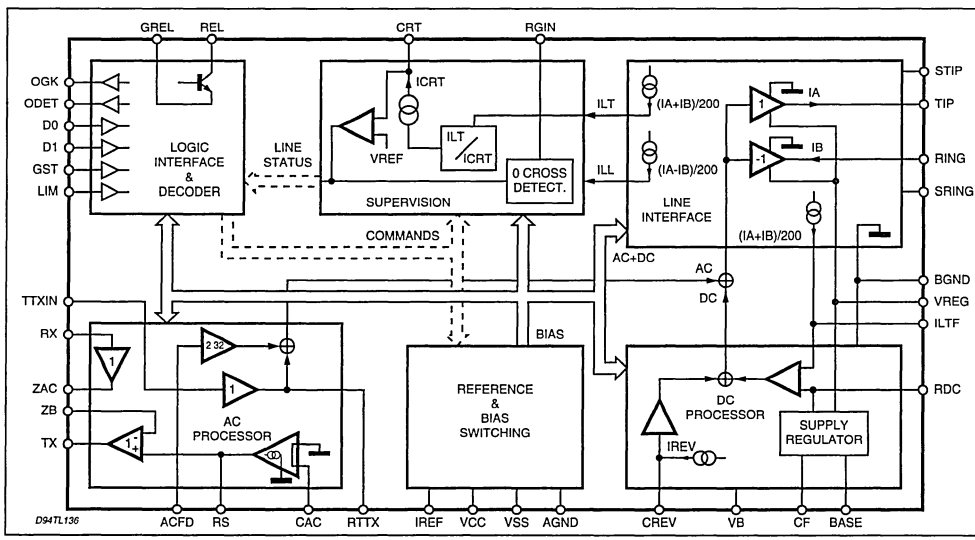
BLOCK DIAGRAM



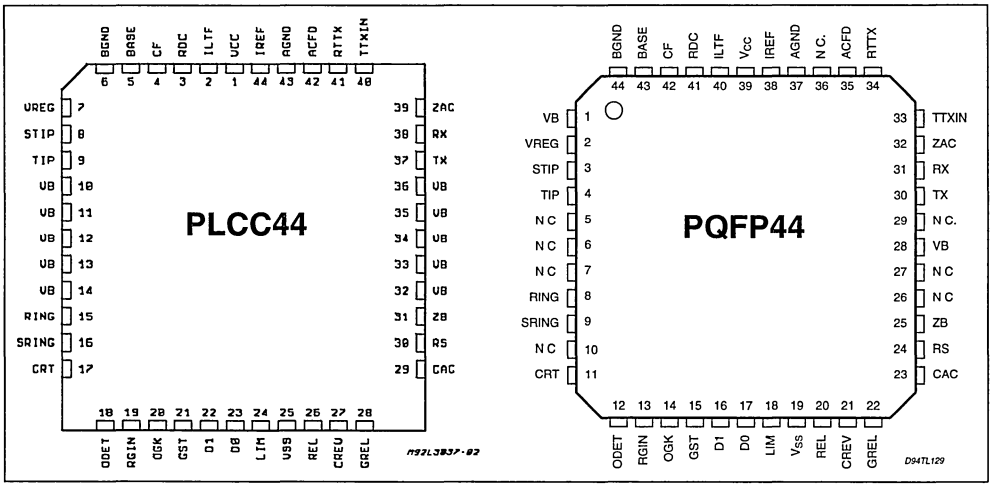
L3037 PIN FUNCTIONALITY (PLCC44)

No.	Name	Function
1	V_{CC}	Supply input (+5V)
2	I_{LTF}	Analog output (current source)
3	RDC	Analog input (current input)
4	CF	Analog input (voltage input)
5	BASE	Analog output (voltage source)
6	BGND	Ground input (0V)
7	VREG	Supply input (VREG)
8	STIP	Analog input (voltage input)
9	TIP	Analog output (voltage output)
10 to14	VB	Supply input (-V_{BAT})
15	RING	Analog output (voltage output)
16	SRING	Analog input (voltage input)
17	CRT	Analog input/output (voltage input / current output)
18	ODET	Digital output (voltage output with internal pull up)
19	RGIN	Analog input (current input)
20	OGK	Digital output (voltage output with internal pull up)
21	GST	Digital input (voltage input, internal pull down)
22	D1	Digital input (voltage input)
23	D0	Digital input (voltage input)
24	LIM	Digital input (voltage input 3 levels: 0, +5, open)
25	V_{SS}	Supply input (-5V)
26	REL	Digital output (voltage output open drain)
27	CREV	Analog input/output (voltage input/current output)
28	GREL	Ground input (0V)
29	CAC	Analog input (current input)
30	RS	Analog input/output (current output/voltage input)
31	ZB	Analog input (voltage input)
32 to 36	VB	Supply input (-V_{BAT})
37	Tx	Analog output (voltage output)
38	Rx	Analog input (voltage input)
39	Z_{AC}	Analog output (voltage output)
40	TTXIN	Analog input (voltage input)
41	RTTX	Analog output (voltage output)
42	ACFD	Analog input (voltage input)
43	AGND	Ground input (0V)
44	I_{REF}	Analog input/output (voltage output/current input)

L3037 FUNCTIONAL DIAGRAM



PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{bat}	Battery Voltage	-64 to V_{SS}+0.5	V
V_{CC}	Positive Supply Voltage (0 to 1ms) (continuous)	-0.4 to +7 -0.4 to +5.5	V V
V_{SS}	Negative Supply Voltage (0 to 1ms) (continuous)	-7 to +0.4 -5.5 to +0.4	V V
V_{agnd} - V_{bgnd}	Agnd Respect Bgnd (continuous)	-2 to +2	V
V_{REL}	Ring Relay Supply Voltage	14	V
V_{dig}	Digital I/O D0, D1, GST, LIM, ODET, OGK	-0.4 to +5.5	V
I_{dig}	Digital I/O D0, D1, GST, LIM, ODET, OGK	-3 to +3	mA
T_j	Maximum Junction Temperature	+150	°C
T_{stg}	Storage Temperature	-55 to +150	°C
Hu	Humidity	5 to 95	%

Note: In case of power on, power failure or hot insertion with V_{DD}, V_{SS} present and V_{bat} floating the Absolute Maximum Ratings can be exceeded with Vbat > V_{SS} +0.5V. In this case the power consumption of the device increases and the logic output state including relay driver are not controlled. This effect can be prevented ensuring that Vbat is always present before V_{DD} and V_{SS} or connecting one shottky diode (e.g. BAT49X or equivalent) between Vbat and V_{SS}. One diode can be shared between all the SLICs of the same line card.

OPERATING RANGE

Symbol	Parameter		Value	Unit
T_{op}	Operating Temperature Range	**L3037** **L3037T**	0 to +70 -40 to +85	°C °C
V_{agnd} - V_{bgnd}	Difference between Agnd and Bgnd		-2 to +2	V
V_{CC}	Positive Supply voltage		+4.5 to +5.5	V
V_{SS}	Negative Supply Voltage		-5.5 to -4.5	V
V_{bat}	Battery Voltage		-62 to -24	V
V_{REL}	Ring Relay Supply Voltage		4 to 13	V

THERMAL DATA

Symbol	Parameter		PLCC44	PQFP44	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	45	75	°C/W

PIN DESCRIPTION

Unless otherwise specified all the diagrams in this datasheet refers to the PLCC44 Pin Connection.

PQFP44 No.	PLCC44 No.	Pin	Description
39	1	V_{CC}	Positive Power Supply (+5V)
40	2	I_{LTF}	Transversal Line Current Image ((I_A + I_B) / 200)
41	3	RDC	DC feedback input (the RDC resistor is connected from this node to I_{LTF})
42	4	CF	Battery voltage ripple rejection (C_{SVR} capacitor is connected from this node to BGND).
43	5	BASE	Driver for external transistor base
44	6	BGND	Battery ground
2	7	VREG	Regulated Voltage. Provides negative power supply for the power amplifier. (connected to emitter of the external transistor.)
3	8	STIP	Input of A power amplifier (when no compensation of ext. ptc resistor mismatch is requested it must be shorted to the TIP lead).
4	9	TIP	A line termination output (I_A is the current sourced from this pin).
1, 28	10 to 14 32 to 36	VB	Battery Supply **PLCC44**: All pins are internally connected together. **PQFP44**: It is mandatory to short pin 1 and pin 28 as closed as possible to the device.
8	15	RING	B line termination output (I_B is the current sunk into this pin).
9	16	SRING	Input of B power amplifier (when no compensation of ext. ptc resistor mismatch is requested it must be shorted to the RING lead).
11	17	CRT	Ring trip and ground key capacitor
12	18	ODET	ON/OFF hook and RING TRIP output (when disable is internally pulled up)
13	19	RGIN	Ring input signal. (when open is internally pulled to GND)
14	20	OGK	Ground key output (when disable is internally pulled up)
15	21	GST	A open command (when open is internally pulled down)
16	22	D1	Bit 1
17	23	D0	Bit 0
18	24	LIM	Current Limitation Program. (when open is internally forced to 44mA current limitation)
19	25	V_{SS}	Negative Power Supply (-5V)
20	26	REL	Ring relay driver output
21	27	CREV	Reverse polarity transition time control. One proper capacitor connected between this pin and AGND is setting the reverse polarity transition time. If reverse polarity feature is not used must be shorted to AGND.
22	28	GREL	Ground reference for ring relay driver
23	29	C_{AC}	AC feedback input (ACDC split capacitor is connected from this node to ILTF)
24	30	R_S	Protection resistors image (the image resistor is connected from this node to ACFD)
25	31	Z_B	Balance network for 2 to 4 wire conversion (the balance impedance Z_B is connecetd from this node to AGND. The Z_A impedance is connected from this node to Z_{AC})
30	37	Tx	4 wire output port (Tx output)
31	38	Rx	4 wire receiving port. (Rx input)
32	39	Z_{AC}	Rx buffer output (the AC impedance is connected from this node to ACFD)
33	40	TTXIN	Metering input port/V_{drop} programming. If not used should be connected to AGND.
34	41	RTTX	Metering cancellation network. If not used should be left open.
35	42	ACFD	AC impedance synthesis
37	43	AGND	DC and AC signal ground
38	44	I_{REF}	Voltage Reference Output
2,5 to 7, 10,26, 27, 29,36	–	N.C.	Not connected

DESCRIPTION (continued)

One special selection with high longitudinal balance performances allows to meet the United States BELLCORE requirements for central office/loop carrier and private applications.

The SLIC integrates loop start, ground start, ground key on/off-hook, automatic ring-trip as well as zero crossing ring relay driver.

Two to four wire conversion is implemented by the SLIC for application with first generation COMBO. In case of application with second generation (programmable) COMBO this function can be implemented outside saving external components.

The L3037 offers programmable current limitation (3 ranges), on hook transmission and low power in all operating modes, power management is controlled by a simple external low cost transistor.

Metering pulses are injected on the line via a summing node through TTXIN pin.
Metering pulse filtering is performed by means of a simple RC network with standard tolerance components. In case TTX function is not used this pin must be connected to AGND. It is also possible to use this pin to modify the DC voltage drop between TIP/RING terminals and battery voltage for appications where it is important to optimize the battery voltage supply versus the signal swing.
Effect of protection resistors mismatch are compensated by a feedback loop on the final stage allowing good long balance performances also with large tolerance protection resistors (ex: PTC).

This function allow the L3037 to be fully conform to BELLCORE power cross and surge test and meet also the Longitudinal Balance Specification without using matched PTC resistors.

An integrated thermal protection circuit forces the L3037 in POWER DOWN (PD) mode when the junction temperature exceeds 150°C Typ.

The L3037 is specified over -40°C to +85°C ambient temperature range.
The L3037 package is a surface mount PLCC44 or PQFP44.

FUNCTIONAL DESCRIPTION

L3037 is designed in 70V bipolar technology and performs the telephone line interface functions required in both C.O. and PABX environments. The full range of signal transmission, battery feed, loop supervision are performed.

Signal transmission performance is compatible with European and North American Standards and with CCITT recommendations.
Ringing, overvoltage and power cross protection are performed by means of external networks.

The signal transmission function includes both 2 to 4 wire and 4 to 2 wire conversion. The 2W termination impedance is set by means of an external impedance which may be complex. The 2 to 4 wire conversion is provided by means of an external network.

Such a network can be avoided in case of applications with COMBOII, in this case the 2 to 4 wire conversion is implemented inside the COMBOII by means of the programmable Hybal filter.

An additional input allows a metering pulse signal to be added on the line.

The DC feed resistance is programmable with one external resistor. Three different values of current limitation (25, 44, 55mA)can be selected by software through the parallel digital interface.

One external transistor reduces the power dissipation inside the L3037 in the presence of a short loop (limiting current region).

An additional supervisory function sets the TIP lead into high impedance state in order to allow application in ground start configurations.

The different L3037 operating modes are controlled by a 4bit logic interface, two additional detector outputs provide ground key detection and either hook state or ring trip detection.

SLIC OPERATING MODES

Through the L3037 digital interface it is possible to select 5 different SLIC operating modes:

1) Active Mode (ACT)

2) Standby Mode (SBY)

3) Tip Open Mode (TO)

4) Power Down Mode (PD)

5) Ringing Mode (RNG)

In both ACT and SBY modes it is possible to select the reverse polarity (see control interface).
Transition from direct to reverse polarity is soft and the transition time is defined by the external capacitor CREV.

ACTIVE MODE (ACT)

This operating mode is set by the card controller when the Off-Hook condition has been recognized.

When this operating mode is selected the two output buffers (TIP/RING) can sink or source up to 100mA each. In case of Ground key or line terminals to GND the output current is limited to 15mA for the Tip wire and 30mA for the Ring wire.

As far as the DC characteristic is concerned three different feeding conditions are present:

a) Current limiting region: the DC impedance of the SLIC is very high (20Kohm) and therefore the system works like a current source. Using the L3037 digital interface it is possible to select the value of the limiting current:

25mA, 44mA, or 55mA.

When the device is in limiting current region the negative supply for the output buffer is fixed by

the ext. transistor to a proper value higher than the real negative battery in order to reduce the power dissipated by the L3037 itself.

b) Resistive feed region: the characteristic is equal to a battery voltage (Vbat) in series with a resistor (typ 400ohm or 800ohm) whose value is set by one ext. resistor (see ext. components list).

c) Constant voltage region: the characteristic is equal to the battery voltage - 12V in series with the ext. protection resistors (typ 80ohm).

This voltage drop between battery and line terminals for Il=0 allows on-hook transmission.

Fig. 1 shows the DC characteristic in active mode. Fig. 2 shows the line current versus loop resistance

Figure 1: DC Characteristic in active mode

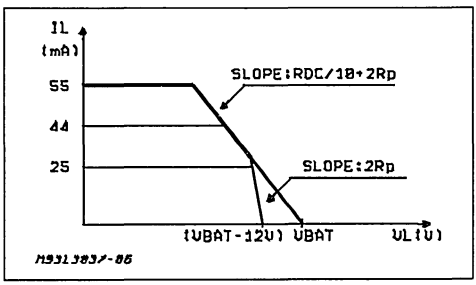
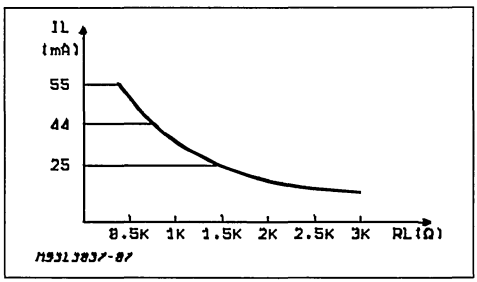


Figure 2: Current vs. Loop Resistance.
Rfeed = 2 x 200ohm,
Lim. currents: 25, 43, 55mA



In active mode the AC impedance at the line terminals is sinthetized by the external components ZAC and Rp according to the following formula:

$$Zs = ZAC/50 + 2*Rp$$

Depending on the characteristic of the ZAC network Zs can be either a pure resistance or a complex impedance. This allows L3037 to meet different standard as far as return loss is concerned. The capacitor CCOMP guarantees stability to the system.

The two to four wire conversion is achieved by means of a circuit that can be represented as a Wheastone bridge, the branches of which are:

1) The line impedance (Zline)
2) The SLIC impedance at line terminals (Zs)
3) The balancing network ZA+RA connected between pin ZAC and ZB of L3037.
4) The network ZB between pin ZB and GND that shall copy the line impedance.

When L3037 is used with a second generation combo (eg TS5070FN) which is able to perform the two to four wire conversion, the two impedances ZA and ZB can be removed and the ZB pin connected to GND. The -6dB TX gain of the L3037 allows the echo signal to remain always within the COMBOII Hybrid balance filter dynamic range.

The injection of high frequency metering pulses is carried out through the SLIC. An unbalanced 12 or 16KHz sinusoidal signal with shaping is, when necessary, applied at the TTXIN input of the SLIC.
A fixed transfer gain is provided for the metering signal. To avoid saturation in the 4-wire side a cancellation is provided in the 4-wire transmission path.

Cancellation is obtained via an external RC network without the need for trimmed components.

When the TTX function is not used TTXIN input should be connected to GND. Since this pin is directly connected to a summing node inside the SLIC any signal applied to the TTXIN is transferred to the line with a fixed transfer gain.
In special applications, this pin can be used to modify the voltage drop (constant voltage region of DC characteristic) simply by applying a proper DC level on the TTXIN pin, allowing optimization of the battery voltage versus the maximum needed AC signal swing.

In active mode, with a -48V battery voltage, the L3037 dissipate 150mW for its own operation (including the power dissipation from +5/-5 supply), the dissipation related to the current supplied to the line should be added in order to get the total dissipation.

STAND-BY MODE (SBY)

In this mode the bias current of the L3037 is reduced and only some part of the circuit are completely active. The transversal current supplied to the line is limited at 14mA. Common mode current rejection is performed and the total current capability of the output stages (TIP and RING) is limited to 30mA. The open circuit voltage is |Vbat|-7V.

Both Off/Hook and Ground key detectors are active. Signal transmission is not operating.

In stand-by mode, with a -48V battery voltage, the L3037 dissipates 90mW typ. (including the power dissipation from a +5/-5V supply).
Stand-by mode is usually selected when the telephone is in on-hook condition. It allows a proper off-hook detection, even in the presence of high common mode currents, or with telephone sets sinking a few milliamperes of line current in on-hook condition.

CONTROL INTERFACE

INPUTS				OPERATING MODE	OUTPUTS	
D0	D1	GST	LIM		ODET	OGK
0	0	0	X	POWER DOWN	DISABLE	DISABLE
1	1	0	X	STANDBY D. P.	OFF/HK	GDKEY
1	1	1	X	STANDBY R. P.	OFF/HK	GDKEY
1	0	0	X (*)	ACTIVE D. P.	OFF/HK	GDKEY
1	0	1	X (*)	ACTIVE R. P.	OFF/HK	GDKEY
0	1	0	X	RING	RING-TRIP	DISABLE
0	0	1	X	A. OPEN	OFF/HK	GDKEY
0	1	1	X	RESERVED	–	–

(*) LIM = 0 → I_{lim} = 25mA; LIM = H. I. (open) → I_{lim} = 44mA; LIM = 1 → I_{lim} = 55mA.

TIP OPEN MODE (TO)

This mode is selected when the SLIC is adopted in a system using the Ground start feature. In this mode the TIP termination is set in High Impedance (100Kohm) while the RING termination is active and fixed at Vbat + 4.5V. In the case of connection of RING termination to GND the sinked current is limited to 30mA. When RING is connected to GND both off-hook and ground-key detectors become active.

Power dissipation in this mode with a -48V battery voltage is 100mW (including the power dissipation from +5/-5V supply).

POWER DOWN MODE (PD)

In this mode, both TIP and RING terminations are open and no current is fed into the line.

The power dissipation is very low.

This mode is usually selected in emergency condition or when the connected line is disabled.

This is also the mode into which the SLIC is automatically forced, in the case of thermal overload T_j > 150°C typ.

RINGING MODE (RNG)

When this mode is selected the ringing signal is injected on the line via the ext relay activated by the L3037 relay driver.

When the ringing signal phase is provided at the RGIN pin, the relay command is also synchronized with the ringing signal zero crossing.

The TIP and RING termination of the L3037 are senses the line current which is then integrated on the CRT capacitor.

TIP pin voltage is fixed at – 2.5V, RING pin voltage is fixed at V_{BAT} + 4.5V, TIP, RING buffer current capability is limited to 100mA.

When off-hook occurs during ringing burst the voltage on CRT increase above a proper threshold and ring trip is detected.

Once ring trip is detected the ringing signal is automatically disconnected at the first zero crossing. When the ringing signal phase is not provided at the RGIN pin the ringing signal is disconnected immediately after ring trip detection.

EXTERNAL COMPONENTS LIST

To set the SLIC into operation the following parameters have to be defined:

- The DC feeding resistance "Rfeed" defined as the resistance of the traditional feeding system (most common Rfeed values are: 400, 800, 1000 ohm).
- The AC SLIC impedance at line terminals "Zs" to which the return loss measurements is referred. It can be real (typ. 600ohm) or complex.
- The equivalent AC impedance of the line "Zl" used for evaluation of the trans-hybrid loss performance (2/4wire conversion). It is usually a complex impedance.
- The value of the two protection resistors Rp in series with the line termination.
- The line impedance at the TTX freq. Zlttx.
- The reverse polarity transition time defined as "$\Delta V_{TR}/\Delta T$".

Once, the above parameters are defined, it is possible to calculate all the external components using the following table.
The typical values has been obtained supposing:

- Rfeed = 400Ω
- Zs = 600Ω
- Zl = 600Ω
- Rp = 40Ω
- Zlttx = 216Ω + 120nF @ 12KHz
- Re[Zlttx] = 216Ω
- Im[Zlttx] = -110Ω @12KHz
- $\Delta V_{TR}/\Delta T$ = 4250[V/s]

EXTERNAL COMPONENTS

Name	Function	Formula	Typ. Value
CVB	Battery Filter		330nF 20% 63VI
CVDD	Positive Supply Filter		100nF 20%
CVSS	Negative Supply Filter		100nF 20%
RREF	Internal Current Reference		23.7K 1%
CSVR	Battery Ripple Rejection	CSVR = 1/(6.28 * fp * 150K) @ fp = 1.6Hz	680nF 20% 60VI
CRT	Ring Trip & Ground-key Capacitor	CRT = (25/f_{RING}) · 390nF	390nF 20% 6VI
RDC	DC Feeding Resistance	RDC = 10 * (Rfeed - 2Rp)	3.2K 1%
CAC	AC/DC Splitter	CAC = 1 / (6.28 * fsp * RDC) @ fsp = 10Hz	4.7µF 20% 15VI
RS	Protection Resistor Image	RS = 50 * 2RP	4K 1%
ZAC	2 Wire AC Impedance	ZAC = 50 * (Zs-2Rp)	26K 1%
ZA (1)	SLIC Impedance Balancing Network	ZA = 50 * (Zs-2Rp)	26K 1%
RA (1)	SLIC Impedance Balancing Network	RA = 50 * 2Rp	4K 1%
ZB (1)	Line Impedance Balancing Network	ZB = 50 * Zl	30K 1%
CCOMP	AC Feedback Compensation	CCOMP = 1 / [2Πfo (100 Rp)] @ fo = 250KHz	220pF 20%
CH (1)	Trans-hybrid Loss Frequency Compensation	CH = CCOMP	220pF 20%
RF	Feeding Resistance for Ring Inj.	≥ 200Ω (7)	200Ω 2W
RT	Feeding Resistance for Ring Inj.	≥ 200Ω (7)	200Ω 2W
RRG	Ring Input Resistor	RRG = (V_{RING}/25µA)cos[-2·f_{RING} · T · 180] (4)	4MΩ 5%
CRG	Ring Input Capacitor	CRG = 25µA/(V_{RING} · sin[2 · f_{RING}·T · 180] · 2Πf_{RING}) (4)	3.9nF 20% 100V
PTC (2)	Positive Temp. Coeff. Resistor	< 15Ω	10Ω
RST (2)	Tip Buffer Sensing Resistor	10 to 50KΩ	33K 1W 5% (6)
RSR (2)	Ring Buffer Sensing Resistor	10 to 50KΩ	33K 1W 5% (6)
QEXT	External Transistor (3)		(*)
Rp	Protection Resistor	30 to 80Ω (8)	40Ω
RTTX	Teletax Cancellation Resistor	RTTX = 21.5 · [Re (Zlttx) +2Rp] (5)	6.34K 1%
CTTX	Teletax Cancellation Capacitor	CTTX = 1/(21.5 · [-Im(Zlttx) · fttx · 6.28]) (5)	5.6nF 20%
D1	Relay Kickback Clamp Diode		1N4148
CREV	Polarity Reversal Transition Time Programming	$CREV = \frac{K}{\Delta V_{TR}/\Delta T}$; $K = 2 \cdot 10^{-4}$	47nF

Notes:

(1) These components can be removed and ZB pin shorted to GND when 2/4wire conversion is implemented with 2nd generation COMBO (EG. TS5070FN)

(2) In case there is no necessity to recover the unbalance introduced by PTC tolerance pins TIP and STIP can be shorted togheter as pins RING and SRING. In this case also the R_P Resistor should be splitted in two parts keeping at least 20Ω between TIP/RING terminals and protection connection. In this case PTC or fuse resistor (if used) can be placed in series to Rp.

(3) Transistor characteristic: P_{DISS} = 1W (typ. depending on application); $h_{FE} \geq 25$; $I_C \geq 100mA$; $V_{CEO} \geq 60V$; $f_T \geq 15MHz$.

(4) V_{RING}: Max Ring Generator Voltage, f_{RING}: Ring Frequency, T: relay response time.
Typical value obtained for V_{RING} = 100Vrms, f_{RING} = 25Hz; T = 2.5ms.

(5) Defining RTTX + CTTX = ZTTX, RTTX and CTTX can also be calculated from the following formula: Z_{FTTX} = 21.5 [Zlttx + 2Rp].

(6) RST and RSR wattage should be calculated according to the power cross test specification. (When PTC become open circuit the entire power cross voltage will appear across RSR and RST).

(7) In order to optimize the component count it is also possible to use only one resistor in series to the ringing generator. In this case RT = 0Ω; RF≥ 400Ω (RF typ. value = 400Ω).

(8) Suggested Rp type are 2W wire wound resistors or thick film resistors on ceramic substrate.
Fuse function should be included if PTC are not used.

(*) ex: BD140; MJE172;MJE350....(ST32 or SOT82 package available also for surface mount).
For low power application (reduced battery voltage) BCP53 (SOT223 surface mount package) can be used.

Figure 3: Typical Application Circuit including all features.

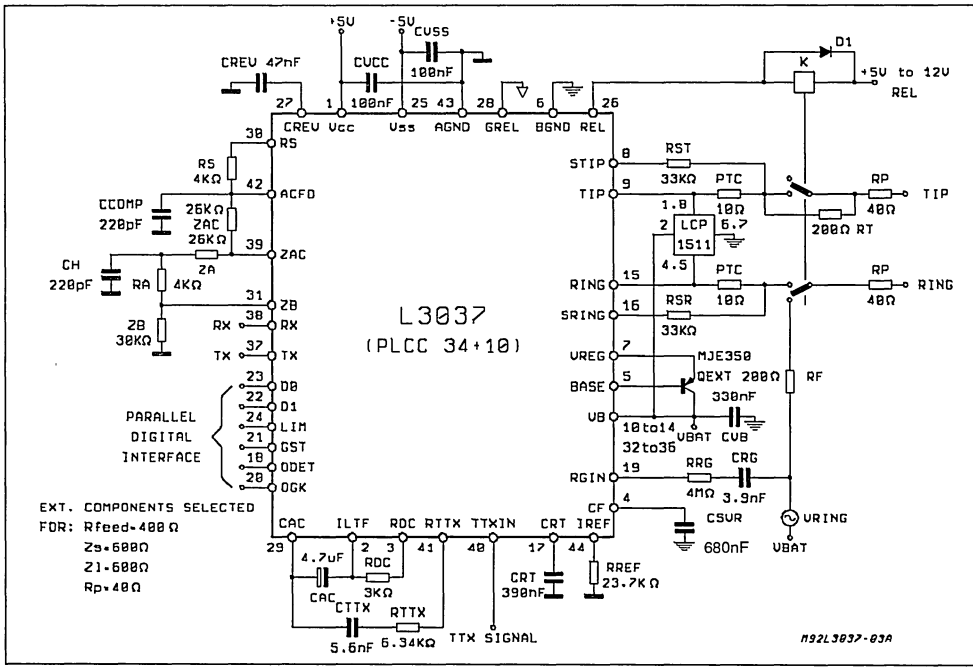
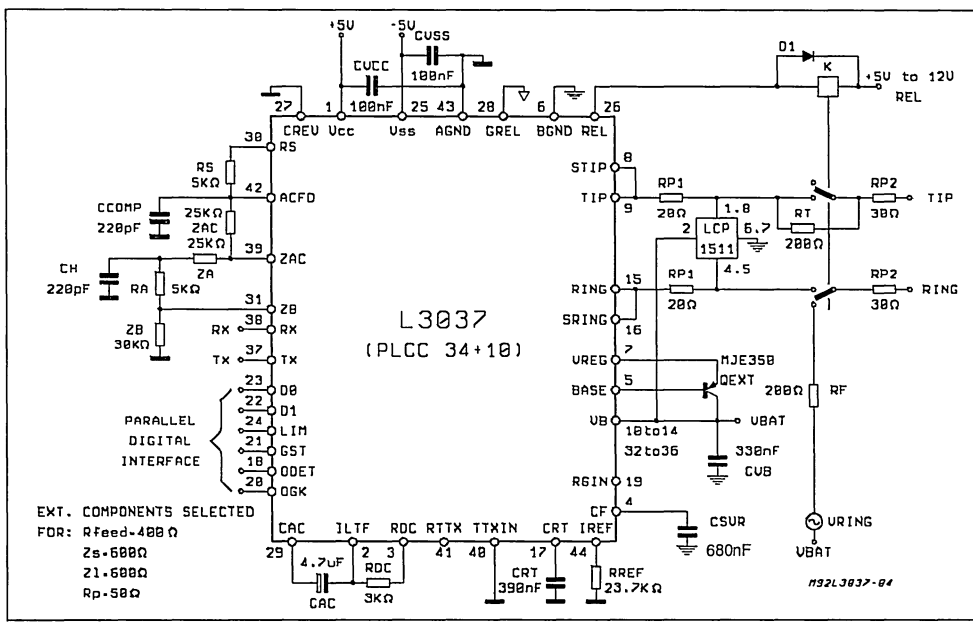


Figure 4: Typical Application circuit with minimum components count (No Rev. polarity NoTTX/No zero crossing sync/no PTC mismatch compensation).



In case of U.S. application based on L3035 the external components can be calculated supposing:

- Rfeed = 400Ω
- Zs = 900Ω + 2.12µF
- ZI = 1650Ω// (100Ω + 5nF) Loaded Line
- ZI = 800Ω// (100Ω + 50nF) Not Loaded Line
- Rp = 62Ω

EXTERNAL COMPONENTS (for US. Application)

Name	Function	Formula	Typ. Value
CVB	Battery Filter		330nF 20% 63VI
CVDD	Positive Supply Filter		100nF 20%
CVSS	Negative Supply Filter		100nF 20%
RREF	Internal Current Reference		23.7K 1%
CSVR	Battery Ripple Rejection	CSVR = 1/(6.28 * fp * 150K) @ fp = 1.6Hz	680nF 20% 60VI
CRT	Ring Trip & Ground-key Capacitor	CRT = (25/f_{RING}) · 390nF	390nF 20% 6VI
RDC	DC Feeding Resistance	RDC = 10 * (Rfeed - 2Rp)	2.76K 1%
CAC	AC/DC Splitter	CAC = 1 / (6.28 * fsp * RDC) @ fsp = 10Hz	4.7µF 20% 15VI
RS	Protection Resistor Image	RS = 50 * 2RP	6.2K 1%
ZAC	2 Wire AC Impedance	ZAC = 50 * (Zs-2Rp) (7)	39K + (180K//55nF)
ZA (1)	SLIC Impedance Balancing Network	ZA = 50 * (Zs-2Rp) (7)	39K + (180K//55nF)
RA (1)	SLIC Impedance Balancing Network	RA = 50 * 2Rp	6.2K 1%
ZB (1)	Line Impedance Balancing Network	ZB = 50 * ZI	82.5K + (5K + 100pF) (3) 40K + (5K + 1nF) (4)
CCOMP	AC Feedback Compensation	CCOMP = 1 / [2ΠIfo (100 Rp)] @ fo = 250KHz	100pF 20%
CH (1)	Trans-hybrid Loss Freq. Comp.	CH = CCOMP	100pF 20%
RF	Feeding Resistance for Ring Inj.	≥ 200Ω (9)	200Ω 2W
RT	Feeding Resistance for Ring Inj.	≥ 200Ω (9)	200Ω 2W
RRG	Ring Input Resistor	RRG = (V_{RING}/25µA)cos[-2·f_{RING} · T · 180] (6)	4MΩ 5%
CRG	Ring Input Capacitor	CRG = 25µA/(V_{RING} · sin[2 · f_{RING}·T · 180] · 2Πf_{RING} (6)	3.9nF 20% 100V
PTC (2)	Positive Temp. Coeff. Resistor	< 15Ω	10Ω
RST (2)	Tip Buffer Sensing Resistor	10 to 50KΩ	33K 1W 5% (8)
RSR (2)	Ring Buffer Sensing Resistor	10 to 50KΩ	33K 1W 5% (8)
QEXT	External Transistor (5)		(*)
Rp	Protection Resistor	30 to 80Ω (10)	62Ω
D1	Relay Kickback Clamp Diode		1N4148

Notes:

(1) These components can be removed and ZB pin shorted to GND when 2/4wire conversion is implemented with 2nd generation COMBO (EG. TS5070FN)

(2) In case there is no necessity to recover the unbalance introduced by PTC tolerance pins TIP and STIP can be shorted togheter as pins RING and SRING. In this case also the R_P Resistor should be splitted in two parts keeping at least 20Ω between TIP/RING terminals and protection connection. In this case PTC or fuse resistor (if used) can be placed in series to Rp.

(3) Loaded Line.

(4) Not Loaded Line.

(5) Transistor characteristic: P_{DISS} = 1W (typ. depending on application); $h_{FE} \geq 25$; $I_C \geq 100mA$; $V_{CEO} \geq 60V$; $f_T \geq 15MHz$.

(6) V_{RING}: Max Ring Generator Voltage, f_{RING}: Ring Frequency, T: relay response time. Typical value obtained for V_{RING} = 100Vrms, f_{RING} = 25Hz; T = 2.5ms.

(7) For details see AN496.

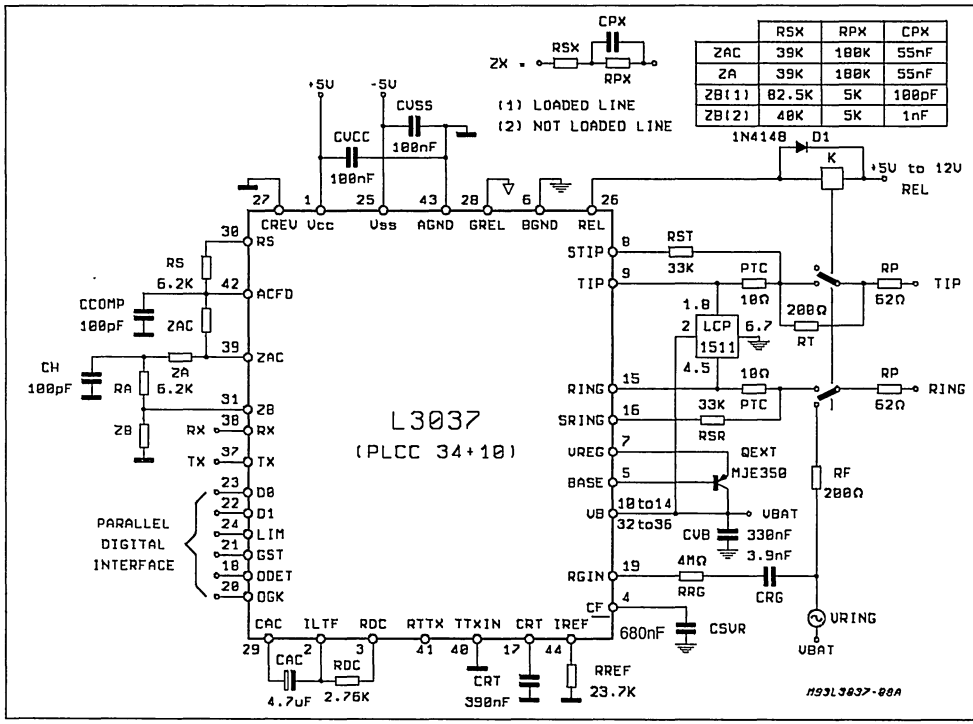
(8) RST and RSR wattage should be calculated according to the power cross test specification. (When PTC become open circuit the entire power cross voltage will appear across RSR and RST).

(9) In order to optimize the component count it is also possible to use only one resistor in series to the ringing generator. In this case RT = 0Ω; RF≥ 400Ω (RF typ. value = 400Ω).

(10) Suggested Rp type are 2W wire wound resistors or thick film resistors on ceramic substrate. Fuse function should be included if PTC are not used.

(*) ex: BD140; MJE172;MJE350....(SOT32 or SOT82 package available also for surface mount). For low power application (reduced battery voltage) BCP53 (SOT223 surface mount package) can be used.

Figure 5: Typical Application Circuit for U.S. Application.



	RSX	RPX	CPX
ZAC	39K	100K	55nF
ZA	39K	100K	55nF
ZB(1)	82.5K	5K	100pF
ZB(2)	40K	5K	1nF

ELECTRICAL CHARACTERISTICS TEST CONDITION, unless otherwise specified: V_{CC} = 5V; V_{SS} = -5V; V_{BAT} = -48V; AGND = BGND; Direct Polarity; T_A = 25°C.

Note: Testing of all parameter is performed at 25°C. Characterization as well as the design rules used allow correlation of tested performances at other temperatures. All parameters listed here are met in the range 0°C to +70°C. Additional selection (on request ordering part #: L3037T) can be performed so that the functionality between -40°C and 85°C is verified.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
INTERFACE REQUIREMENTS 2 WIRE PORT						
V_{ab}	Overload Level Voice Signal	Rp +PTC = 50Ω 300Hz to 3.4KHz (*)	4.1			Vpk
Z_{ll}	Long Input Impedance	at SLIC terminals per wire			10	Ω
I_{ll}	Long Current Capab. ac	standby per wire (on HOOK)	17			mApk
		active per wire (on HOOK)	17			mApk
I_{ll}	Longitudinal Current Capability	active per wire off HOOK (IT = Transversal current)	75-I_T			mApk
4 WIRE TRANS PORT						
V_{tx}	Overload Level		1.8			Vpk
V_{toff}	Output Offset Voltage		-350		+350	mV
Z_{tx}	Output Impedance				10	Ω

(*) At TIP/RING line connection with Z_{LINE} (AC) = 600Ω. For any DC Loop current from 0mA to I_{LIM}

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
4 WIRE RECEIVE PORT						
Z_{RX}	Input Impedance		100			KΩ
V_{RX}	Overload Level		3.2			Vpk
METERING INPUT PORT						
Z_{MIN}	Input Impedance		100			KΩ
LOGIC CONTROL PORT INPUT D0, D1, GST						
V_{ih}	Input High Voltage		2			V
V_{il}	Input Low Voltage				0.8	V
I_{ih}	Input High Current		-10		90	µA
I_{il}	Input Low Current		-10		10	µA
C_{in}	Input Capacitance				10	pF
INPUT LIM						
V_{ih}	Input High Voltage		2.4			V
V_{il}	Input Low Voltage				0.4	V
I_{ih}	Input high Current		-10		30	µA
I_{il}	Input Low Current		-30		10	µA
C_{in}	Input Capacitance				10	pF
OUTPUT DET						
V_{ol}	Output Low Voltage	I_o = 2mA			0.4	V
V_{oh}	Output High Voltage	I_o = 30µA I_o ≤10µA	2.4 3.8			V V
C_{ld}	Load Capacitance				150	pF
RINGING INPUT PORT						
	Overload Level		-0.5		0.5	V
	Input Impedance		50		90	KΩ
	Offset Voltage Allowed		-15		15	mV

TRANSMISSION PERFORMANCE

Arl	Return Loss (2-wire)	300Hz to 3.4KHz	22			dB
Thl	Transhibrid Loss	300Hz to 3.4KHz $20\log_{10} \lvert \frac{V_{RX}}{V_{TX}} \rvert$	30			dB
Longitudinal balance (CCITT Rec.0.121)						
L-T	Longit to Transversal	300Hz to 3.4KHz Z_S = 600Ω R_P = 40Ω, 1% tolerance	52			dB
L-4	Long Sign Rejection		58			dB
T-L	Transvers to Longit		49			dB
4-L	Long Sign Generation		49			dB
Selected L3037 Longitudinal balance (IEEE Std 455-1976)						
L – T	Longitudinal to Transversal	300Hz to 3.4KHz Z_S = 900Ω + 2.12µF R_P = 62Ω, 1% match	58	63		dB
L – 4	Longitudinal Signal Rejection			70		dB

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
INSERTION LOSS						
G_t	Transmit V Gain	0dBm, 1KHz	-6.22		-5.82	dB
G_r	Receive V Gain		-0.2		0.2	dB
INSERTION LOSS vs. FREQUENCY (rel 1KHz / 0dBm)						
G_t	Transmit V Gain	0.3 to 3.4KHz	-0.1		0.1	dB
G_r	Receive V Gain		-0.1		0.1	dB
METERING INJECTION						
G_{TTX}	Transfer Gain	V_{TTXIN} = 0.66Vrms Z_L =200Ω;	3.18		3.51	
THD	Harmonic Distortion	$2 \cdot R_P$ = 80Ω; V_{moff} = 0			5	%
GAIN LINEARITY (rel 1KHz, -4dBm)						
G_t	Transmit V Gain	-55dBm to 7dBm (1)	-0.1		0.1	dB
G_r	Receive V Gain		-0.1		0.1	dB
GROUP DELAY (2-4, 4-2) 0DbM						
T_{gABS}	Absolute	3KHz		5		µs
T_{gDIS}	4 to 2-wire	0.5 to 3,4KHz		5		µs
TOT HARMONIC DISTORTION						
Thd4	2 to 4-wire	7dBm, 0.3 to 3.4KHz			-46	dB
Thd2	4 to 2-wire				-46	dB
IDLE CHANNEL NOISE						
Vabp	2-wire port	psophometric		-78	-72	dBmP
Vtxp	4-wire transmit	psophometric		-82	-76	dBmP
Vabc	2-wire port	c message		12	18	dBrnC
Vtxc	4-wire transmit	c message		8	14	dBrnC

RINGING FUNCTION

0 cross	Zero Crossing Threshold Level	f_{RING} = 16 to 66Hz R_{GIN} = 3Vrms	-70		70	mV
I_{RT}	Ring Trip Threshold			7.5		mA DC
T_{RTD}	Ring Trip Detection Time	R_L = 1.8k, f_{RING} = 25Hz			150	ms

BATTERY FEED CHARACTERISTIC

POWER DOWN STATE						
I_{LGND}	Loop Current	TIP or RING to BGND			0.5	mA
I_{LBAT}	Loop Current	TIP or RING to V_{bat}			0.5	mA
I_L	Loop Current	R_L = 0			1	mA
STAND BY STATE						
I_l	Iloop Accuracy	constant region	13		16	mA
V_{LOS}	Line Voltage	@ I_L = 0	40		42	V
ACTIVE STATE						
V_{LO}	Line Voltage	@ I_L = 0	34.5		37.5	V
R_{feed}	Feeding Resistance Accuracy		-10		+10	%
I_{lim}	Loop Current Limit Accuracy	I_{lim} = 25mA, 44mA, 55mA	-8	I_{lim}	+8	%
GROUND START STATE						
Z_{TIP}	Tip Lead Impedance		100			KΩ
I_{GS}	Ring Lead Current	RING to GND		30		mA

(1) For level lower than -40dB guaranteed by correlation.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DETECTORS						
OFF HOOK DETECTOR						
I_{det}	Off-hook Current Threshold	stand by state	9		12	mA
I_{det}	Off-hook Current Threshold	active state	9		12	mA
Hys	Off-hook / On-hook Hysteresys	Both stand by and active state	1		1.6	mA
Td	Dialling Distortion	active state	-1		1	ms
GROUND KEY DETECTOR						
I_{LL}	Ground Key Current Threshold $I_{LL} = (I_B - I_A) / 2$	TIP to RING to GND or RING to GND		4		mA
POWER DISSIPATION ON L3037 at V_{BAT} = 48V						
P_d	Power Down	any line lenght			38	mW
P_d	Stand-by	2-wire open R_L = 0 to 2K		95	136 250	mW mW
P_d	Active, R_{feed} = 800Ω I_{LIM} = 25mA I_{LIM} = 44mA I_{LIM} = 55mA	2-wire open R_L = 0 to 2K R_L = 0 to 2K R_L = 0 to 2K		155	224 710 1730 2660	mW mW mW mW
P_d	Active, Rfeed = 400Ω I_{LIM} = 25mA I_{LIM} = 44mA I_{LIM} = 55mA	2-wire open R_L = 0 to 2K R_L = 0 to 2K R_L = 0 to 2K		155	224 510 870 1280	mW mW mW mW
P_d	Active	Ground Key		1500		mW
POWER DISSIPATION ON QEXT AT V_{bat} = 48V						
P_{dq}	Active, R_{feed} = 800Ω I_{LIM} = 25mA I_{LIM} = 44mA I_{LIM} = 55mA	 R_L = 0 to 2K R_L = 0 to 2K R_L = 0 to 2K			 880 810 420	 mW mW mW
P_{dq}	Active, Rfeed = 400Ω I_{LIM} = 25mA I_{LIM} = 44mA I_{LIM} = 55mA	 R_L = 0 to 2K R_L = 0 to 2K R_L = 0 to 2K			 1080 1610 1670	 mW mW mW
SUPPLY CURRENTS						
ANALOG SUPPLY						
I_{CC}	V_{CC}	Power Down		1.5	2.2	mA
I_{SS}	V_{SS}	Power Down		0.1	0.5	mA
I_{CC}	V_{CC}	Stand-by / A open		4	5	mA
I_{SS}	V_{SS}	Stand-by / A open		1.5	3	mA
I_{CC}	V_{CC}	Active		6	10	mA
I_{SS}	V_{SS}	Active		3	6	mA
BATTERY SUPPLY						
I_{bat}	Power down	a or b to BGND		120	500	µA
I_{bat}	Stand-by	2-wire open		1.4	2	mA
I_{bat}	Active	2-wire open 2-wire R_L = 400Ω		2.3	3 I_{LOOP}+5	mA mA

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
POWER SUPPLY REJECTION (V_{RIPPLE} = 100mVrms)						
LINE TERMINALS						
PSRR	V_{CC} ref to AGND	50Hz to 3.4KHz	20			dB
PSRR	V_{SS} ref to AGND		20			dB
PSRR	V_{bat} ref to AGND		30			dB
PSRR	BGND ref to AGND		20			dB
RELAY DRIVER						
i_{RD}	Current Capability		40			mA
V	Voltage Drop	@I_{RD} = 40mA			1.25	V
i_{LK}	Off Leakage Current				100	µA

Figure 6: Test Circuit

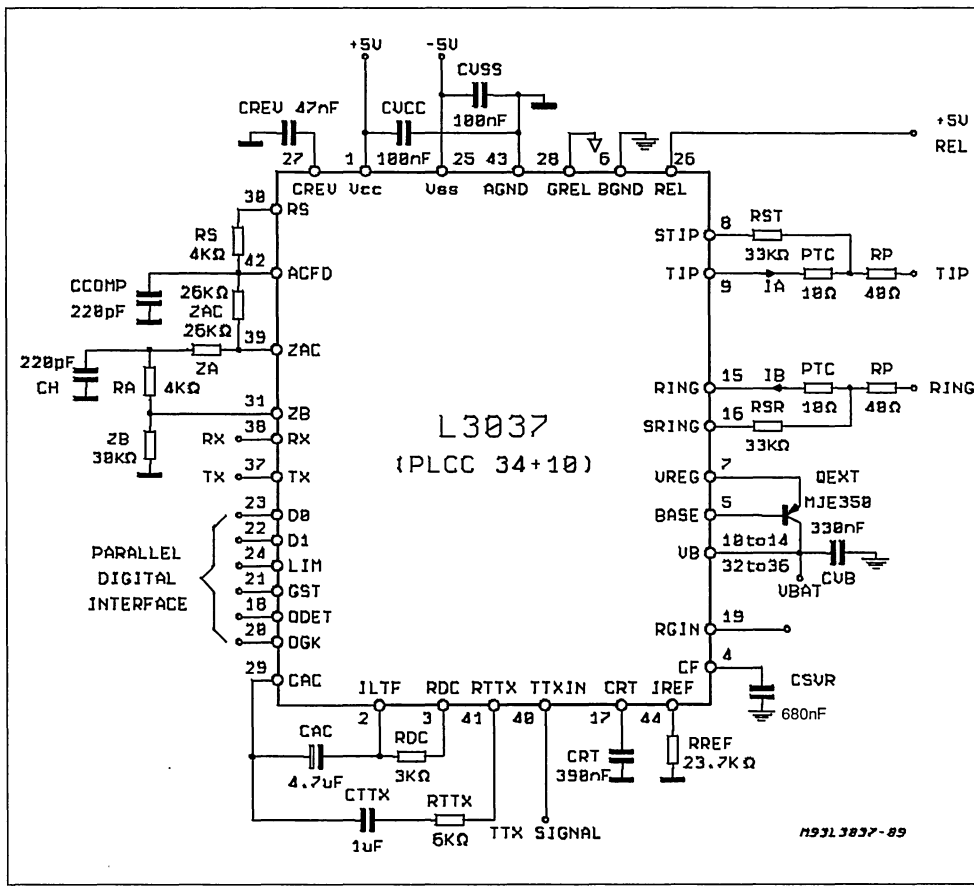


Figure 7: Typical Application with 2nd Generation COMBO (600Ω Application)

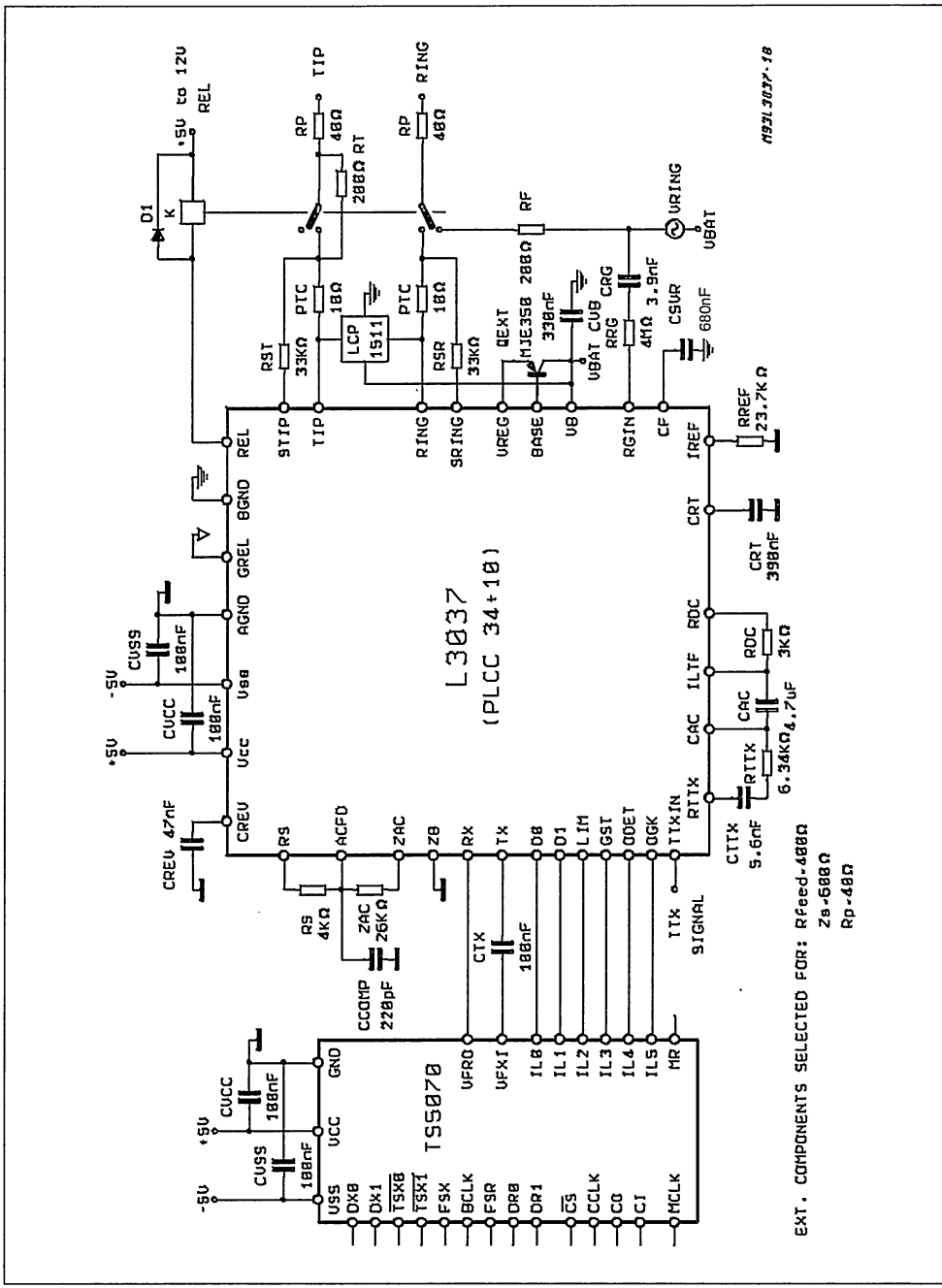


Figure 8: Typical Application with 1st Generation COMBO (600Ω Application)

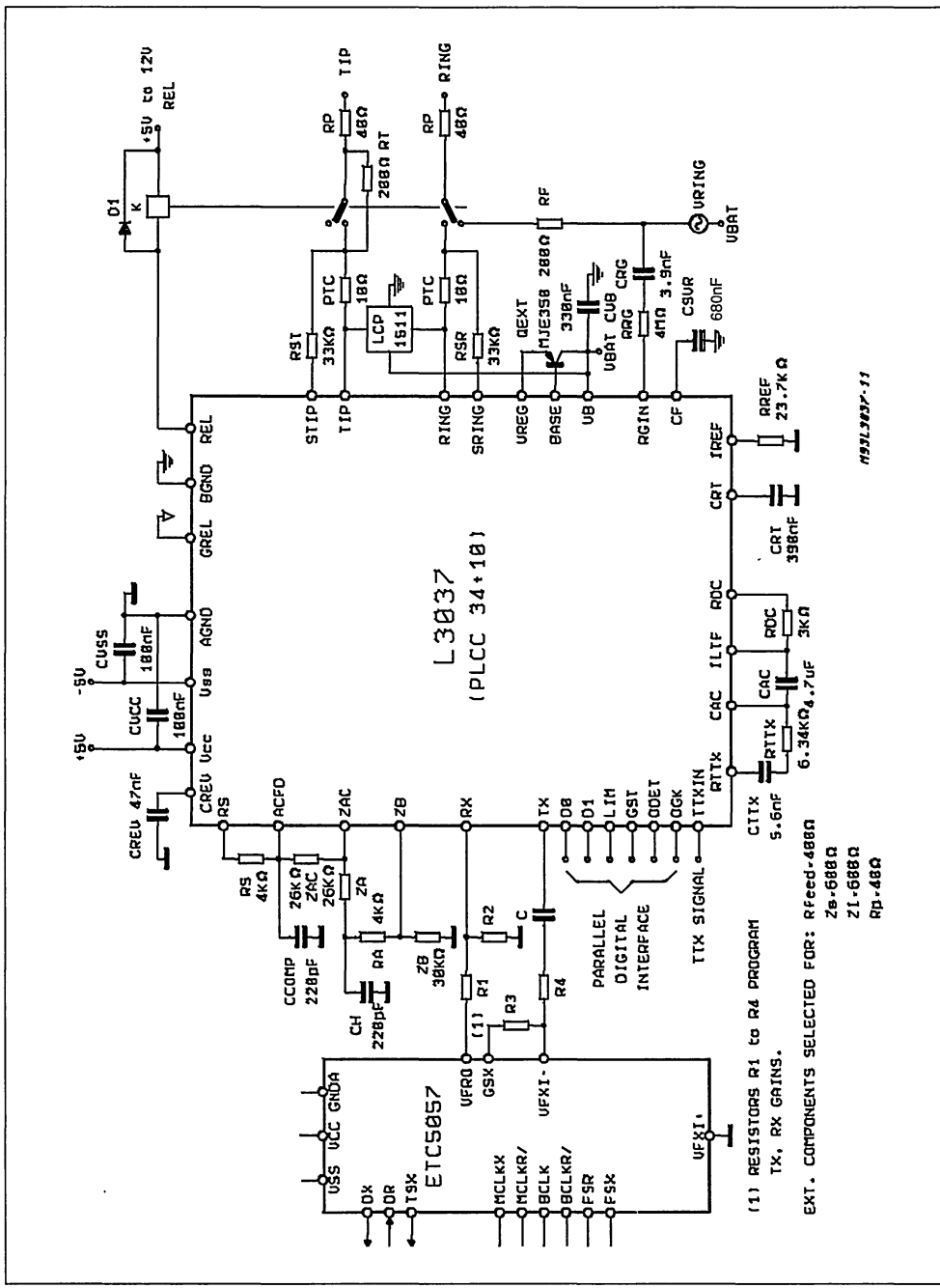


Figure 9: Typical Application with 2nd Generation COMBO (U.S. Application)

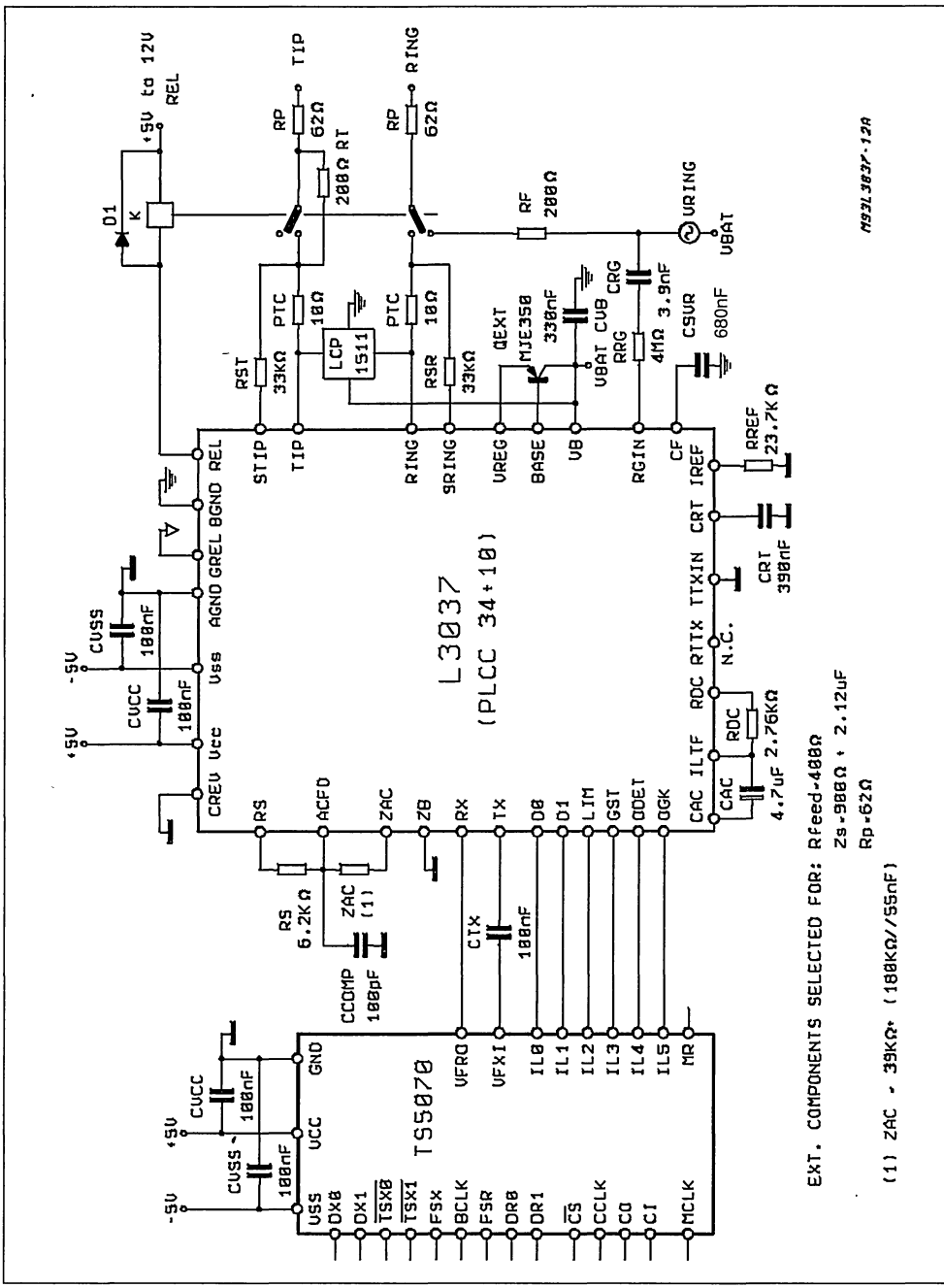
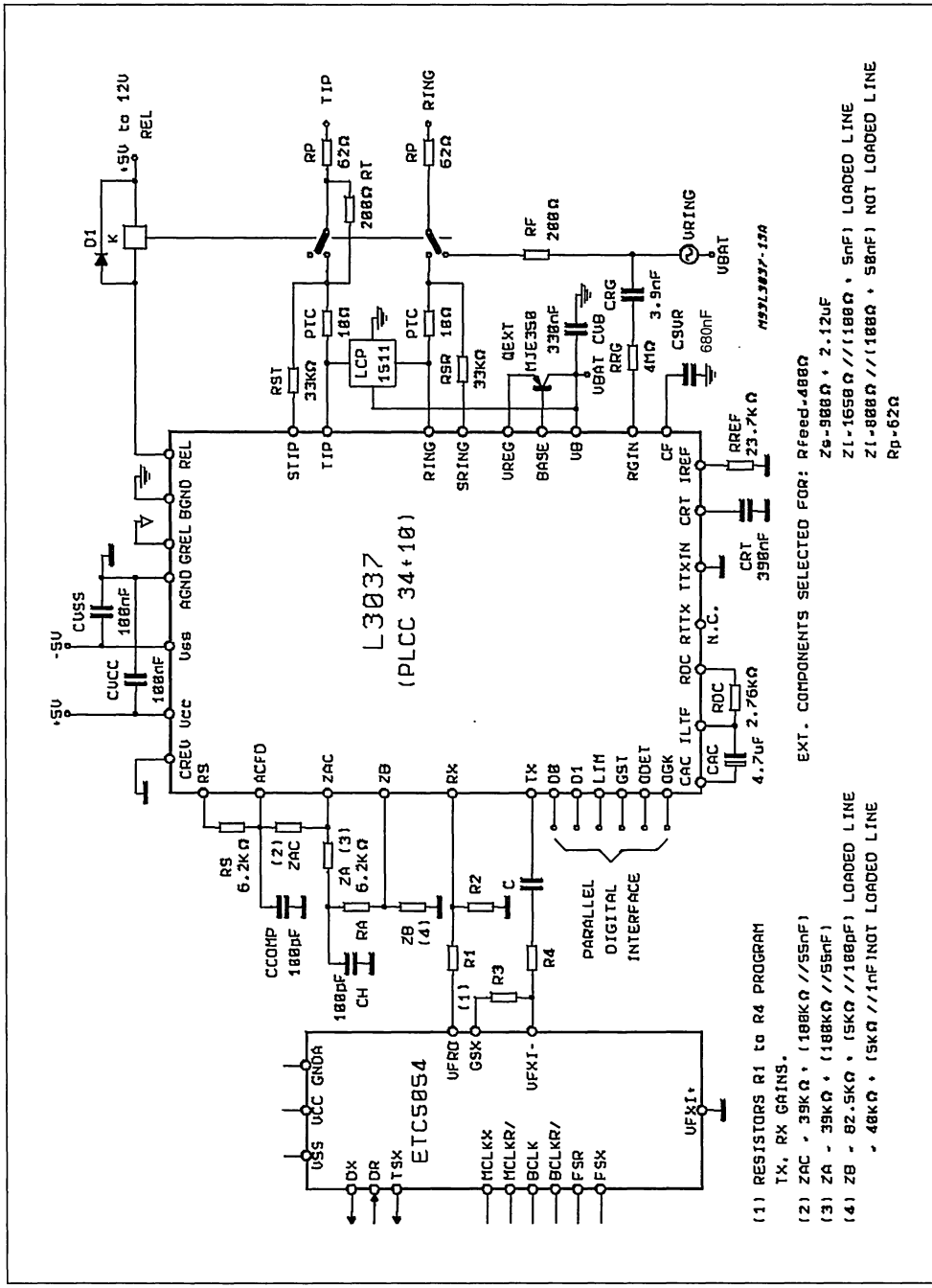


Figure 10: Typical application with 1st Generation COMBO (U.S. Application)



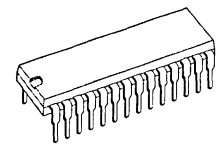
SGS-THOMSON MICROELECTRONICS

L3000N
L3092

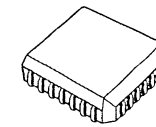
SLIC KIT OPTIMIZED FOR APPLICATIONS WITH BOTH FIRST AND SECOND GENERATION COMBOS

PRELIMINARY DATA

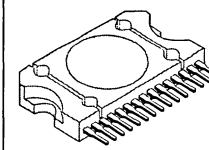
- PROGRAMMABLE DC FEED RESISTANCE AND LIMITING CURRENT (25/40/60mA)
- LOW ON-HOOK POWER DISSIPATION (50mW typ)
- SIGNALLING FUNCTION (off-hook/GND-Key)
- QUICK OFF-HOOK DETECTION IN CVS FOR LOW DISTORTION (< 1 %) DIAL PULSE DETECTION
- HYBRID FUNCTION
- RINGING GENERATION WITH QUASI ZERO OUTPUT IMPEDANCE, ZERO CROSSING INJECTION (no ext. relay needed) AND RING TRIP DETECTION
- ABSOLUTELY NO NOISE INJECTED ON ADIACENT LINES DURING RINGING SEQUENCE
- AUTOMATIC RINGING STOP WHEN OFF-HOOK IS DETECTED
- TEST MODE ALLOWS LINE LENGHT MEASUREMENT
- PARALLEL LATCHED DIGITAL INTERFACE
- LOW NUMBER OF EXTERNAL COMPONENTS WITH STANDARD TOLERANCE ONLY : 9 1% RESISTORS AND 5 10-20% CAPACITORS (for 600 ohm appl.)
- POSSIBILITY TO WORK ALSO WITH HIGH COMMON MODE CURRENTS
- GOOD REJECTION OF THE NOISE ON BATTERY VOLTAGE (20dB at 10Hz ; 35dB at 1KHz)
- INTEGRATED THERMAL PROTECTION
- SURFACE MOUNT PACKAGE (PLCC28 + PowerSO-20)
- 0°C TO 70°C: L3000N/L3092
- -40°C TO +85°C: L3000NT/L3092T



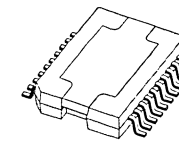
DIP28
ORDERING NUMBER:
L3092N



PLCC28
ORDERING NUMBER:
L3092FN



FLEXIWATT15
ORDERING NUMBER:
L3000N



PowerSO-20
ORDERING NUMBER:
L3000NSO

DESCRIPTION

The SLIC KIT (L3000N/L3092) is a set of solid state devices designed to integrate many of the functions needed to interface a telephone line. It consists of 2 integrated devices ; the L3000N line interface circuit and the L3092 control unit.

The kit implements the main features of the BORSHT functions:

- Battery feed (balance mode)
- Ringing Injection
- Signalling Detection
- Hybrid Function

The SLIC KIT injects the ringing signal in balanced mode and requires a positive supply voltage of typically + 72V to be available on the subscriber card.

The L3000N/L3092 kit generates the ringing signal internally, avoiding the requirement for expensive external circuitry. A low level 1.5Vrms input is required. (This can be provided by the combo).

A special operating mode limits the SLIC KIT power dissipation to 50mW in on-hook condition keeping the on/off hook detection circuit active.

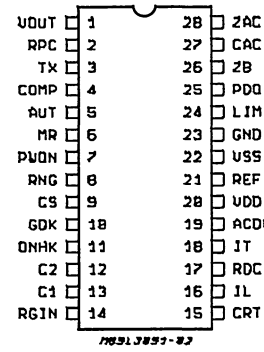
Through the Digital Interface it is also possible to set an operating mode that allows measurements of loop resistance and therefore of line lenght.

This kit is fabricated using a 140V Bipolar technology for L3000N and a 12V Bipolar I^2L technology for L3092.

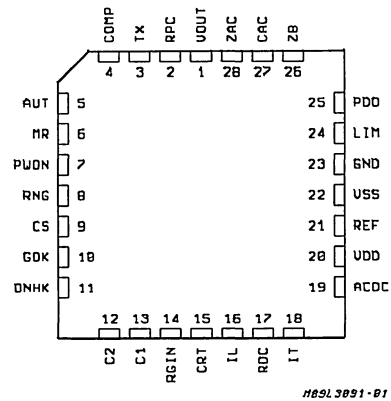
Both devices are available PTH application (FLEXIWATT15 and DIP28) or SMD application (PowerSO-20 and PLCC28).

This kit is specially suitable to Private Automatic Branch Exchange (PABX) and Low Range C.O. Applications.

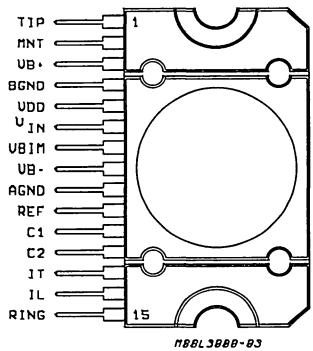
PIN CONNECTIONS



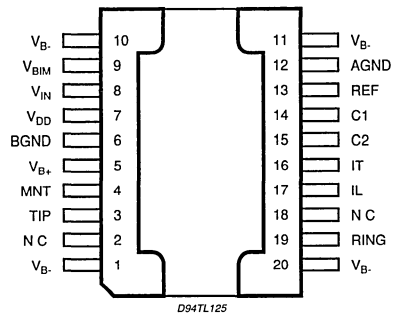
DIP-28



PLCC-28



FLEXIWATT15



PowerSO-20

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{b-}	Negative Battery Voltage	–80	V
V_{b+}	Positive Battery Voltage	80	V
$\|V_{b-}\|+\|V_{b+}\|$	Total Battery Voltage	140	V
V_{dd}	Positive Supply Voltage	+6	V
V_{ss}	Negative Supply Voltage	–6	V
$V_{agnd}-V_{bgnd}$	Max. Voltage between Analog Ground and Battery Ground	5	V
T_j	Max. Junction Temperature	+150	°C
T_{stg}	Storage Temperature	–55 to +150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
L3000N HIGH VOLTAGE				
$R_{th\ j\text{-}case}$	Thermal Resistance Junction to case (FLEXIWATT15)	Max.	4	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to ambient (FLEXIWATT15)	Max.	50	°C/W
$R_{th\ j\text{-}case}$	Thermal Resistance Junction to case (PowerSO-20)	Typ.	2	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to ambient (PowerSO-20)	Max.	60	°C/W
L3092 LOW VOLTAGE				
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to ambient	Max.	80	°C/W

OPERATING RANGE

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{oper}	Operating Temperature Range for **L3000N/L3092** **L3000NT/L3092T**	0 -40		70 +85	°C °C
V_b-	Negative Battery Voltage	–70	–48	–20	V
V_b+	Positive Battery Voltage	0	+72	+75	V
$\|V_b-\|+\|V_b+\|$	Total Battery Voltage		120	130	V
V_{dd}	Positive Supply Voltage	+4.5		+5.5	V
V_{ss}	Negative Supply Voltage	–5.5		–4.5	V

PIN DESCRIPTION (L3000N)

FLEX. N°	SO-P. N°	Name	Description
1	3	TIP	A line termination output with current capability up to 100mA (I_s is the current sourced from this pin).
2	4	MNT	Positive Supply Voltage Monitor.
3	5	V_{B+}	Positive Battery Supply Voltage.
4	6	BGND	Battery ground relative to the V_{S+} and the V_{B-} supply voltages. It is also the reference ground for TIP and RING signals.
5	7	V_{DD}	Positive Power Supply +5V.
6	8	V_{IN}	2 wire unbalanced voltage input.
7	9	VBIM	Output voltage without current capability, with the following functions: - give an image of the total battery voltage scaled by 40 to the low voltage part. - filter by an external capacitor the noise on .
8	1,10,11, 20	V_{B-}	Negative Battery Supply Voltage.
9	12	AGND	Analog Ground. All input signals and the V_{DD} supply voltage must be referred to this pin.
10	13	REF	Voltage reference output with very low temperature coefficient. The connected resistor sets Internal circuit bias current.
11	14	C1	Digital signal input (3 levels) that defines device status with pin 12.
12	15	C2	Digital signal input (3 levels) that defines device status with pin 11.
13	16	I_T	High precision scaled transversal line current signal. $I_T = \frac{I_a + I_b}{100}$
14	17	I_L	Scaled longitudinal line current signal. $I_L = \frac{I_a - I_b}{100}$
15	19	RING	B line termination output with current capability up to 100mA (I_b is the current sunk into this pin).
–	2, 18	N.C.	Not connected.

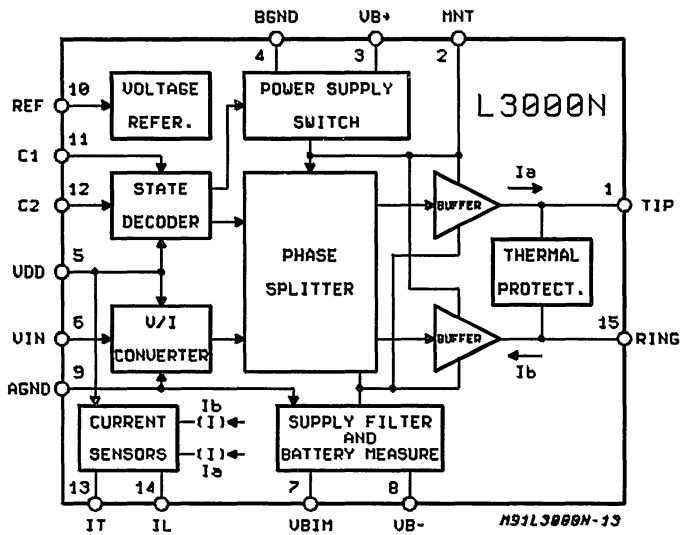
Notes: 1) Unless otherwise specified all the diagrams in this datasheet refers to the FLEXIWATT15 pin connection.
2) All information relative to the PowerSO-20 package option should be considered as advanced information on a new product now in developement or undergoing evaluation. Details are subject to change without notice.

PIN DESCRIPTION (L3092)

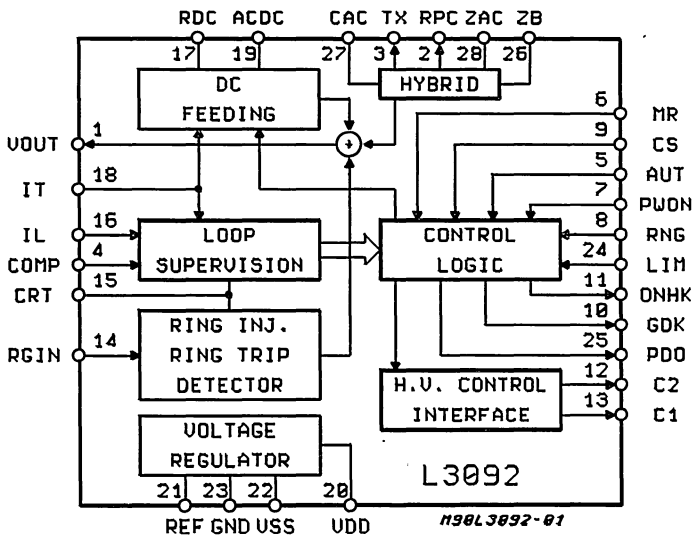
N°	Name	Description
1	VOUT	Two wire unbalanced output carryng out the following signals reduced by 40: 1) DC voltage to perform the proper DC characteristic. 2) Ringing Signal 3) Voice Signal
2	RPC	AC line Impedance Adjustment Protection Resistances Compensation
3	TX	Transmit Amplifier Output
4	COMP	Comparator Input. This is the input comparator that senses the line voltage in power down and in automatic stand-by, allowing off hook detection in this mode.
5	AUT	Aut. Input. It is a part of the digital interface. Loaded when CS is low.
6	MR	Master Reset Input. When it is connected to ground the SLIC is forced in power down. It has an internal pull-up. (typ. 200KΩ) (*)
7	PWON	Power on/power off input. This input is part of digital interface. Loaded when CS is low.
8	RING	Ring Enable Input. This input is part of the digital interface. Loaded when CS is low.
9	CS	Chip Select Input.
10	GDK	Ground Key Output Enabled by CS Low.
11	ONHK	On Hook/off Hook Output Enabled by CS Low.
12	C2	State control Signal 2.
13	C1	State Control Signal 1. Combination of C1 and C2 define operating mode of the high voltage part.
14	RGIN	Low Level Ringing Signal Input.
15	CRT	Ring Trip Detection
16	IL	Longitudinal Line Current Input $IL = \frac{I_b - I_a}{100}$
17	RDC	DC Feeding System
18	IT	Transversal Line Current Input $IT = \frac{I_a + I_b}{100}$
19	ACDC	AC - DC Feedback Input.
20	VDD	Positive Supply Voltage, +5V.
21	REF	Bias Setting Pin.
22	VSS	Negative Supply Voltage, -5V.
23	GND	Analog and Digital Ground.
24	LIM	Limiting Current Selection Input. Loaded when CS is low.
25	PDO	Power Down Output. Driving the high voltage part L3000N through the bias resistor RH.
26	ZB	TX Amplifier Negative Input performig the two to four wire conversion. In case of application with 2nd Generation COMBO performing also the echo cancellation (ex TS5070/5071), this pin must be connected to GND.
27	CAC	AC Feedback Input.
28	ZAC	AC Line Impedance Synthesis.

(*) Must be connected to a proper capacitor for power on reset or to V_{DD} if not used. Should not be left open.

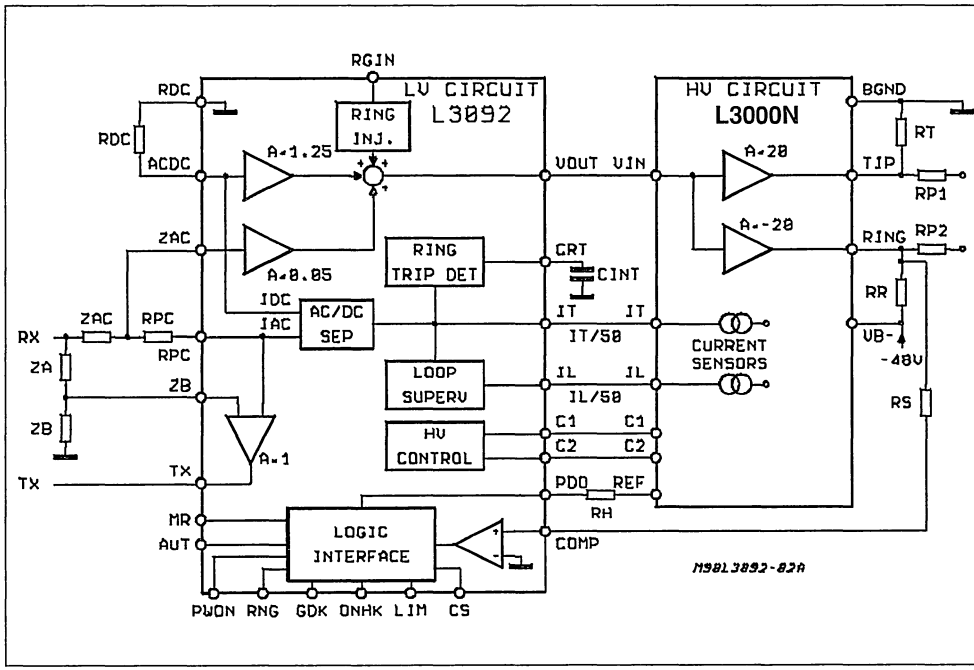
L3000N BLOCK DIAGRAM



L3092 BLOCK DIAGRAM



FUNCTIONAL DIAGRAM



FUNCTIONAL DESCRIPTION

L3000N - HIGH VOLTAGE CIRCUIT

The L3000N line interface provides battery feed for telephone lines and ringing injection. Both these operations are done in Balance Mode. This is very important in order to avoid the generation of common mode signals in particular during the pulse dialling operation of the telephone set connected to the SLIC. The IC contains a state decoder that under external control can force the following operational modes : stand-by, conversation and ringing.

In addition Power down mode can be forced connecting the bias current resistor to V_{DD} or leaving it open.

Two pins, I_L and I_T, carry out the information concerning line status which is detected by sensing the line current into the output stage.

The L3000N amplifies both the AC and DC signals entering at pin 6 (VIN) by a factor equal to 40.

Separate grounds are provided :

- Analog ground as reference for analog signals
- Battery ground as a reference for the output stages

The two ground should be shorted together at a low impedance point.

L3092 - LOW VOLTAGE CIRCUIT

The L3092 Low Voltage Control Unit controls the L3000N line interface module providing set up data to set line feed characteristics and to inject ringing. An on chip digital parallel interface allows a microprocessor or a second generation COMBO as the TS5070 to control all the operations.

L3092 defines working states of Line Interface Circuit and also informs the card controller about line status.

L3000N WORKING STATES

In order to carry out the different possible operations, the L3000N has several different working states. Each state is defined by the voltage respectively applied by pin 12 and 13 of L3092 to the pins 12 and 11 of L3000N.

Three different voltage levels (–3, 0, +3) are available at each connection, so defining nine possible states as listed in tab. 1.

Appropriate combinations of two pins define four of the five possible L3000N working states that are:

a) Stand-by (SBY)
b) Conversation (CVS)

Table 1.

		Pin 12 of L3092 Pin 12 of L3000N (C2)		
		+3	0	–3
Pin 13 of L3092	+3	Stand-by	Conversation	Not Used
(C1)	0	Not Used	B.B	Not Used
Pin 11 of L3000N	–3	Not Used	Ringing	Not Used

c) Ringing (RING)

d) Boost Battery (BB),(see Appendix B).

The fifth status, Power down (PD), is set by the output pin PDO of the L3092 that disconnect the Bias Resistor, RH, of L3000N from ground.

The main difference between Stand-by and Power down is that in SBY the power consumption on the voltage battery VB– (– 48V) is reduced but the L3000N DC Feeding and monitoring circuits are still active, in PD the power consumption on VB- is reduced to zero, and the L3000N is completely switched off.

SLIC OPERATING MODES

Through the L3092 Digital Interface it is possible to select six different SLIC OPERATING MODES :

1) Conversation or Active Mode (CVS)

2) Stand - By Mode (SBY)

3) Power - Down Mode (PD)

4) Automatic Stand - By Mode (ASBY)

5) Test Mode (TS)

6) Ringing Mode (RNG)

1) CONVERSATION (CVS) OR ACTIVE MODE

This operating mode is set by the control processor when the Off hook condition has been recognized,

As far as the DC Characteristic is concerned two different feeding conditions are present :

a) Current limiting region : the DC impedance of the SLIC is very high (> 20KΩ) and therefore the system works like a current generator. By the L3092 Digital Interface it is possible to selects the value of the limiting current.:

60mA, 40mA or 25mA.

b) A standard resistive feeding mode : the characteristic is equal to a battery voltage (VB-) minus 5V, in series with a resistor, whose value is set by external components (see external component list of L3092).

Switching between the two regions is automatic without discontinuity, and depends on the loop resistance. The SLIC AC characteristics are guaranteed in both regions.

Fig. 1 shows the DC characteristic in conversation mode.

Fig. 2 shows the line current versus loop resistance for two different battery values and RFS = 200Ω.

The allowed maximum loop resistance depends on the values of the battery voltage (VB), on the RFS and on the value of the longitudinal current (I_{GDK}). With a battery voltage of 48V, RFS = 200Ω and I_{GDK} = 0mA, the maximum loop resistance is over 3000Ω and with I_{GDK} = 20mA is about 2000Ω (see Application Note on maximum loop resistance for L3000N/L3092 SLIC KIT).

In conversation mode the AC impedance at the line terminals is synthetized by the external components ZAC and RP, according to the following formula :

$$ZML = \frac{ZAC}{25} + 2 \cdot RP$$

Depending the characteristic of the ZAC network, ZML can be either a pure resistance or a complex impedance. This allows for ST SLIC to meet different standards as far as the return loss is concerned. The capacitor CCOMP guarantees stability to the system.

The two to four wire conversion is achieved by means of a circuit that can be represented as a Wheatstone bridge, the branches of which being:

1) The line impedance (Zline).

2) The SLIC impedance at line terminals (ZML).

3) The balancing network ZA connected between RX input and ZB pin of L3092.

4) The network ZB between ZB pin and ground that shall copy the line impedance.

It is important to underline that ZA and ZB are not equal to ZML and to Zline. They both must be multiplied by a factor in the range of 10 to 25, allowing use of smaller capacitors.

In case the L3000N/L3092 kit is used with a second generation programmable COMBO (EG TS5070FN) which is able to perform the two to four wire conversion, the two impedances ZA and ZB can be removed and the ZB pin connected to GND.

The -6dB Tx gain of the L3000N/L3092 SLIC kit in fact allows to keep the echo signal always within the COMBO Hybrid Balance Filter dynamic range.

In conversation mode, the L3000N dissipates about 250mW for its own operation. The dissipation related to the current supplied to the line shall be added, in order to get the total dissipation.

In the same condition the power dissipation of L3092 is typically 100mW.

Figure 1: DC Characteristics in Conversation Mode

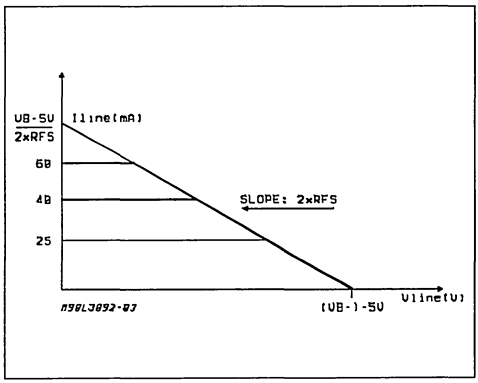
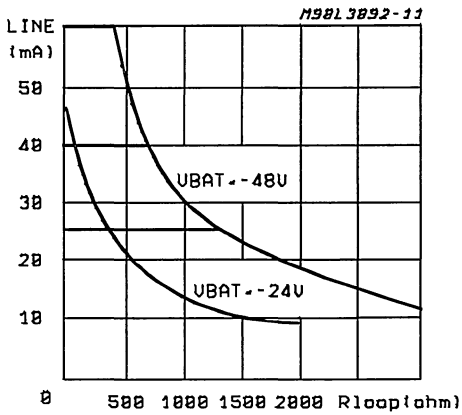


Figure 2: Line Current versus Loop Resistance - RFS = 200Ω; Limiting Currents: 25/40/60mA



2) STAND-BY (SBY) MODE

In this mode the bias currents of both L3000N and L3092 are reduced as only some parts of the two circuits are completely active, control interface and current sensors among them. The current supplied to the line is limited at 10mA, and the slope of the DC characteristic corresponds to 2 x RFS.

The AC characteristic in Stand-by corresponds to a low impedance (2 x RP)

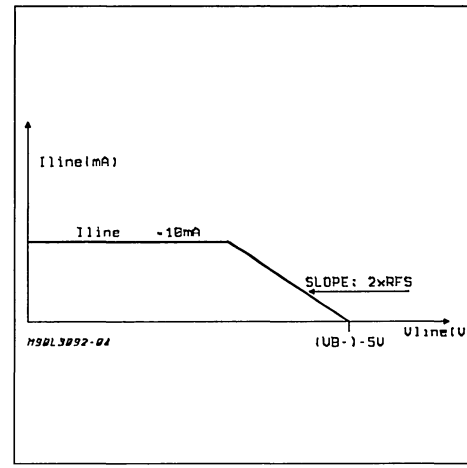
In Stand-by mode the line voltage polarity is just in direct condition, that is the TIP wire more positive than the RING one as in Conversation Mode.

When the SLIC is in Stand-by mode, the power dissipation of L3000N does not exceed 120mW from – 48V) eventually increased of a certain amount if some current is flowing into the line.

The power dissipation of the L3092 in the same condition is typically 50mW.

SBY Mode is usually selected when the telephone is in on-hook. It allows a proper off-hook detection also in presence of high common mode line current or with telephone set sinking few milliAmpere of line current in on hook condition.

Figure 3: DC Characteristics in Stand-by Mode



3) POWER DOWN (PD) MODE

In this mode the L3000N present a high impedance (> 1 Mohm) to the line and cannot feed any line current.

The L3092 forces L3000N in Power Down disconnecting its bias Resistor, RH, from the ground through the output pin PD0.

The power dissipation from the battery voltage (– VB) is almost equal to zero and the power dissipation of L3092 is typically 50mW.

The PD mode is normally used in emergency condition but can be used also in normal on-hook condition.

In this case the off-hook detection is performed using the line sense comparator integrated in the L3092.

The fig. 4 shows the functional circuit to perform the off hook detection in Power down mode.

The resistor RR and RT feed the line current. The voltage at the terminal of the resistor RS connected to RING wire is normally – 48V.

When there is a loop resistor between TIP and

RING wires the voltage will increases to – 24V.

The comparator C1 will change its output voltage from low to high level.

If the Chip Select input (CS) is low the ONHK output pin will be set to low level (+ 0V) indicating that the off hook condition is present.

This off-hook detection circuit can be influenced by common mode signal present on RING Terminal. The capacitor Cs is used to filter this common mode signal.

In the case of very high common mode signal after the detection of a low level on the ONHK output pin, it is suggested to set the SLIC in Stand-by. In this operating mode the off-hook detection circuit is not sensitive to the line common mode signal.

If in Stand-by Mode the off-hook detection is not confirmed (ONHK output set to high level) we suggest after few second to set the SLIC again in Power Down Mode.

Total operation is managed by line card controller.

Figure 4: Off-hook Detection Circuit in Power Down Mode

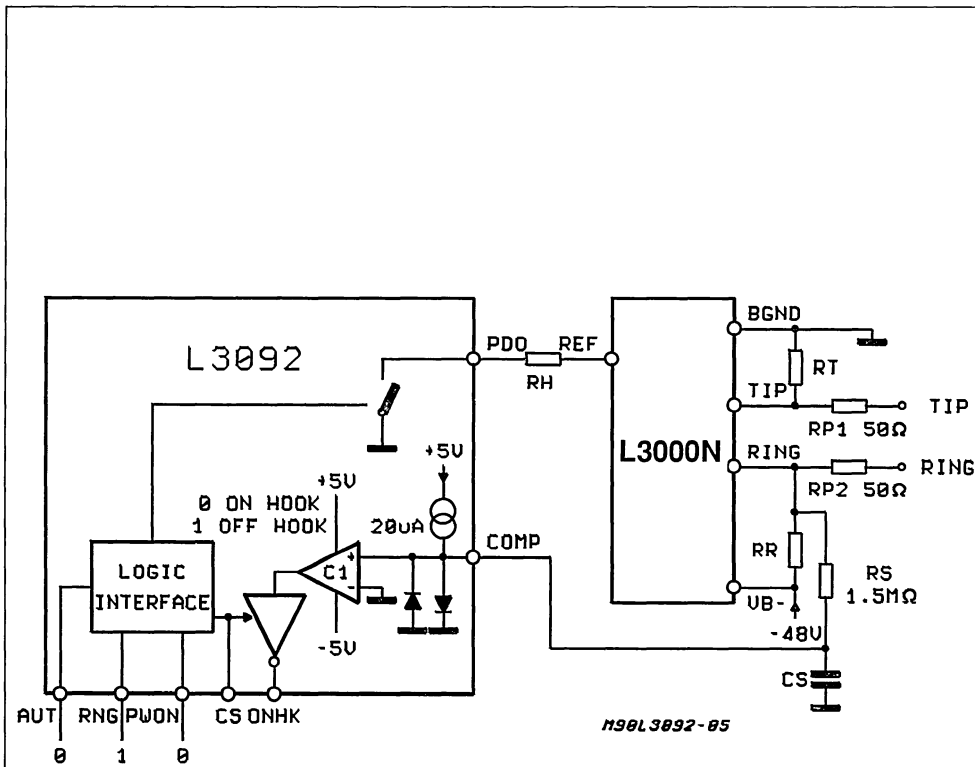
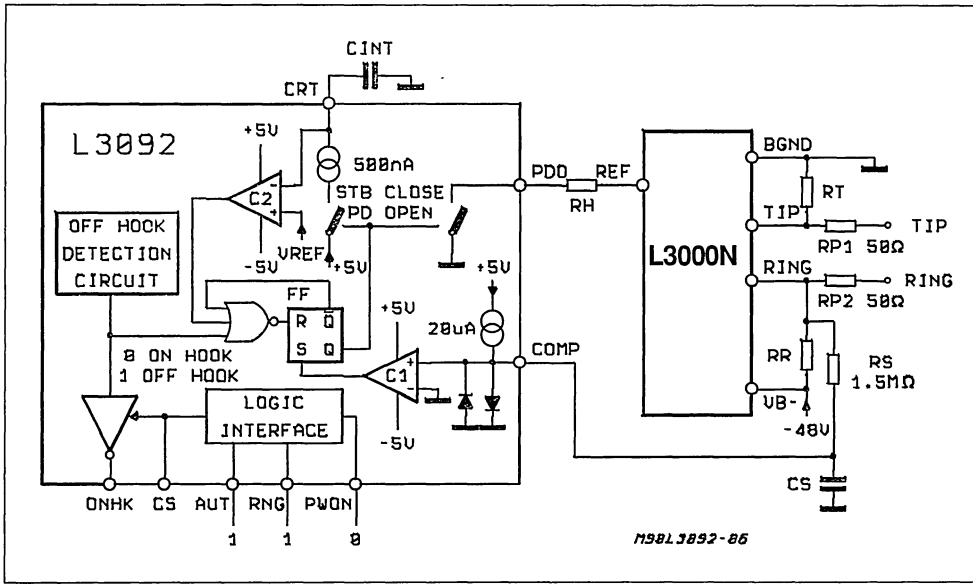


Figure 5: Off-hook Detection Circuit in Automatic Standby Mode



4) AUTOMATIC STAND - BY (ASB) MODE

This is an operating mode similar to the Power Down Mode, but with the software procedure to detect off-hook condition integrated in hardware on chip.

Fig. 5 shows the functional circuit activated in this mode.

When the off-hook condition occurs RING wire voltage goes high (from - 48V to - 24V).

The output of the comparator C1 will go high setting the output of the flip - flop FF high.

Therefore L3092 will set L3000N in Stand-by providing a ground signal at pin PDO.

At the same time the external capacitor CINT will be slowly charged.

In Stand-by the internal off-hook Detection circuit will be activated and will check if the off-hook condition detected by the comparator C1 was true or not true.

If the off-hook condition is confirmed the SLIC will be kept in Stand-by Mode and the output ONHK will go low when CS is low.

If the off-hook condition is not confirmed the SLIC will be kept in Stand - By only for a few seconds. (typ. 5sec). When the voltage at CRT out put will reach the V_{REF} value the C2 comparator will reset the FF Flip - Flop and therefore the SLIC will be set again in Power Down.

The Automatic Stand-by (ASBY) Mode combine the key characteristics of Power Down (PD) and Stand-by (SBY) Modes in particular it is characterized by a very low power consumption (as the Power Down mode) and a sophisticated off hook detection circuit (as the Stand-By mode).

The card controller will receive the off-hook information from the pin ONHK only after that it is checked and confirmed by the internal off-hook detector that is not sensitive to spikes and common mode line signal. Therefore the software required to manage the SLIC will be very simple.

5) TEST (TS) MODE

When this mode is activated the SLIC will be set in conversation mode keeping the initial value of limiting current.

The GDK output pin of L3092 Digital Interface will be set to "0" if the SLIC is operating in the limiting current region of the DC characteristic, see fig. 1 and 2. GDK output will be set to 1 if the SLIC is operating in the resistive region.

The SLIC will work in one of the two region depending on the loop resistance and the programmed limiting current value.

By changing the liming current value selected in conversation mode it is possible to measure the Loop Resistance and therefore the line lenght connected to the SLIC.

The following table shows the ranges of the loop resistance that set the GDK output pin to high and low level in correspondance of all the possible limiting current values (25/40/60mA) with RFS = 200Ω.

Limiting Current	GDK = 0	GDK = 1
60mA	(0 – 300) ohm	>300 ohm
40mA	(0 – 650) ohm	>650 ohm
25mA	(0 – 1300) ohm	>1300 ohm

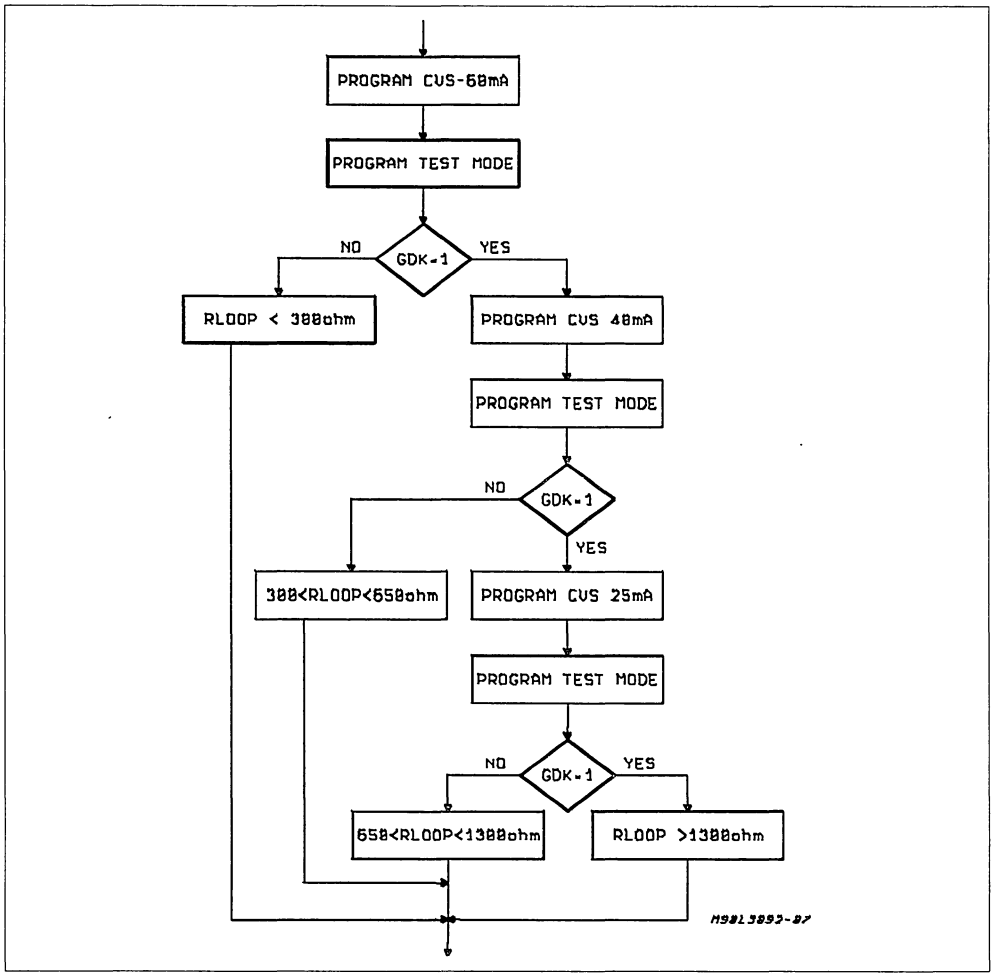
If, for example, the loop resistance is 400Ω the GDK output will be 0 only when the limiting current value is 40 or 25mA.

The card controller can program consecutive Test Mode and Conversation Mode with different limiting current in order to individuate the range of loop resistance as shown in the flow chart of fig. 6.

The information of the Loop Resistance Range can be very useful to optimize the transmission characteristics of the Line Card to each line.

For example, if a second generation COMBO like TS5070 is used the Card Controller can use this information to change the Tx, RX Gains and echo cancellation characteristics into the programmable COMBO improving the quality of the system.

Figure 6: Procedure for Loop Resistance Evaluation.



6) RINGING MODE

When the ringing function is selected by the control processor a low level signal (1.5Vrms) with a frequency in the range from 16 to 70Hz, permanently applied to the L3092 (pin RGIN), is amplified and injected in balanced mode into the line through the L3000N with a super imposed DC voltage of 24V typ.

This low level sinewave can be obtained also from COMBO connecting RGIN pin to RX COMBO output with a decoupling capacitor.

The first and the last ringing cycles are synchronized by the L3092 so that the ringing signal always starts and stops when the line voltage crosses zero.

When this mode is activated, the L3000N operates between the negative and the positive battery voltages typically - 48V and + 72V. The impedance to the line is just equal to the two external resistors (typ. 100Ω).

Ring trip detection is performed autonomously by the SLIC, without waiting for a command from the control processor, using a patented system which allows detection during a ringing burst ; when the off-hook condition is detected, the SLIC stops the ringing signal and forces the Conversation Mode.

In this condition, if CS = 0V, the output pin ONHK goes to 0V.

After the detection of the ONHK = 0, the Card Controller must set the SLIC in Conversation Mode to remove the internal latching of the On/Off hook information.

CONTROL INTERFACE BETWEEN THE SLIC AND THE CARD CONTROLLER

The SLIC states and functions are controlled by microprocessor or interface latches of a second generation combo through seven wires that define a parallel digital interface.

The seven pins of the digital interface have the following functions :

- Chip select input (CS)
- Power on/off input (PWON)
- Ring enable input (RNG)
- Automatic SBY input (AUT)
- Limiting current input (LIM)
- On hook/Off hook detection output (ONHK)
- Ground Key detection output (GDK)

The four input pins PWON, RNG, AUT and LIM, set the status of the SLIC as shown in the following table.

The output pin ONHK is equals to 0V when the line is in OFF hook condition (I_{line} > 7,5mA) and is equal to + 5V when the line is in On hook condition (I_{line} < 5,5mA).

The output pin GDK monitors the ground key function when the SLIC is in Conversation (CVS) Mode and the DC operating region (limiting or resistive) in Test (TS) Mode. When the SLIC is in Conversation (CVS) Mode and I_{GDK} (longitudinal current) > 12mA, pin GDK is set to 0V ;

Operating Mode	Input Pin				Output Pin	
	RNG	PWON	AUT	LIM	ONHK	GDK
Conversation 25mA	0	1	1	X	1 on-hook	1 Ground key not detected.
Conversation 40mA	0	1	0	1	0 off-hook	0 Ground key detected.
Conversation 60mA	0	1	0	0		
Stand-by	0	0	0	X		Disable
Automatic Stand-by	1	0	1	X		
Power-down	1	0	0	X	C1 Comparator Output	Disable
Test Mode	0	0	1	X	1 on-hook	0 Limiting Region
Ringing (CVS 25mA)	1	1	1	X	0 off-hook	1 Resistive Region
Ringing (CVS 40mA)	1	1	0	1		Disable
Ringing (CVS 60mA)	1	1	0	0		

N.B. : When Ringing Mode is selected, you must choose also which of the three possible Conversation Modes The SLIC will automatically select if Off-Hook condition will be detected during ringing

When I_{GDK} < 8mA, pin GDK set to + 5V

The longitudinal current (I_{GDK}) is defined as follows :

$$I_{GDK} = \frac{I_b - I_a}{2}$$

Where I_a is the current sourced from pin TIP and I_b is the current sunk into pin RING.

The CS input pin allows to connect the I/O pins of the digital interfaces of many SLIC together.

It is possible to do it because :

When the CS = + 5V the output pins (ONHK, GDK) are in high impedance condition (> 100KΩ). The signals present at the input pins are not transfered into the SLIC.

When the CS = 0V the output pins change in function of the values of the line current (I_{line}) and the longitudinal current (I_{GDK}). The operating status of the SLIC are set by the voltage applied to the input pins.

The rising edge of the CS signal latches the signal applied to the input pins. The status of the SLIC will not change until the CS signal will be again equal to zero.

See timings fig 7 & 8.

An additional input pin MR (Master Reset) can be useful during the system start up phase or in emergency condition.

In fact when this pin is set to "0" the SLIC will be set in POWER DOWN MODE. This pin has an internal pull-up resistor of about 200KΩ

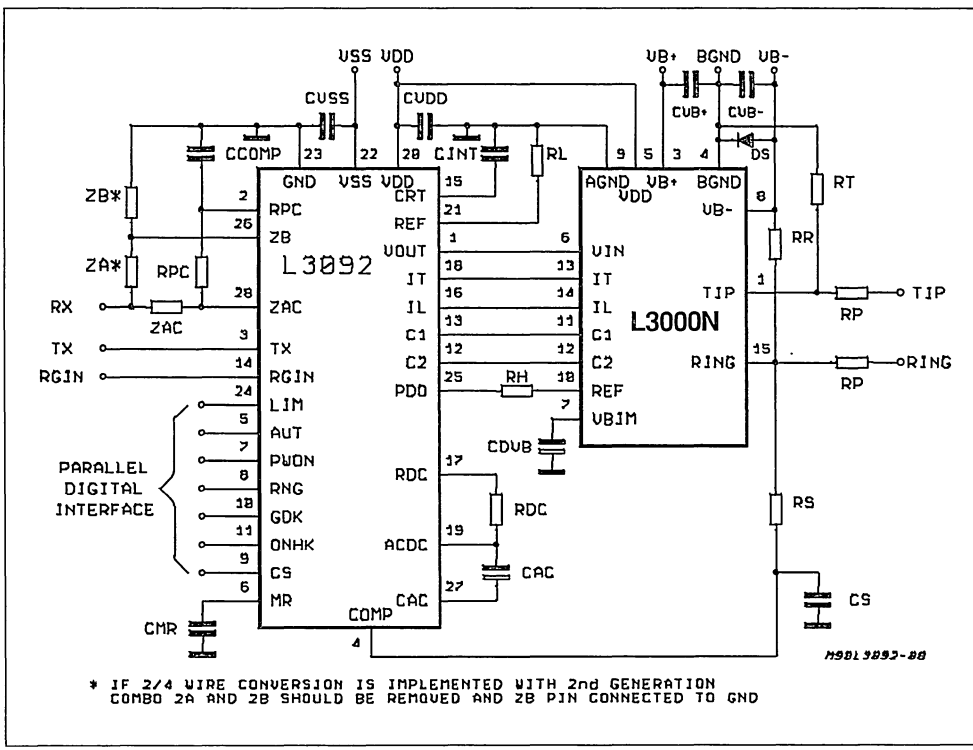
EXTERNAL COMPONENTS LIST

To set up the SLIC kit into operation, the following parameters have to be defined :

- The DC feeding resistance RFS, defined as the resistance of each side of the traditional feeding system (most common value for RFS are 200, 400 or 500).
- The AC input/output SLIC impedance at line terminals, ZML, to which the return loss measurement is refered. It can be real (typically 600Ω) or complex.
- The equivalent AC impedance of the line Zline used for evaluation of the trans-hybrid loss (2/4 wire conversion). It is usually a complex impedance.
- The frequency of the ringing signal Fr (SLIC can work with this frequency ranging from 16 to 68Hz).
- The value of the two resistors RP in series with the line terminals ; main purpose of the a.m. resistors is to allow primary protection to fire..

With these assumptions the following components list is defined :

Figure 7: Typical Application Circuit



EXTERNAL COMPONENT LIST FOR THE L3000N

Component		Involved Parameter or Function
Ref	Value	
RH	22.5KΩ ±2%	Bias Resistor
RP	30 to 100Ω	Lines Series Resistor
CDVB	47µF - 20V ±20%	Battery Voltage Rejection
CVB+	0.1µF - 100V ±20%	Positive Battery Filter
CVB-	0.1µF - 100V ±20% (note 1)	Negative Battery Filter
DS	BAT49X (note 2)	Protective Shottky Diode

EXTERNAL COMPONENT LIST FOR THE L3092

CVSS	0.1µF - 15V	Negative Supply Voltage Filter
CVDD	0.1µF - 15V	Positive Supply Voltage Filter
CAC	47µF - 10V ±20%	AC Path Decoupling
ZAC	25 x (ZML - 2xRP)	2 Wire AC Impedance
CCOMP	$\frac{1}{2\Pi f_o (50 R_P)}$ with f_o = 200KHz	AC Loop Compensation
RPC	25 x (2xRP)	R_P Insertion Loss Compensation
RDC	2 x (RFS - RP)	DC Feeding Resistor (RDC > 200Ω)
RL	63.4KΩ ±1%	Bias Resistor
ZA	K x Z_{ML} (note 3)	SLIC Impedance Balancing Network
ZB	(K x Zline)//($\frac{25}{K}$ x CCOMP) (note 4)	Line Impedance Balancing Network
CINT	see Table 2 (note 5)	Ring Trip Detection Time Constant
RT	47KΩ	Resistors used only in the automatic stand-by mode.
RR	47KΩ	
RS	1.5MΩ (note 6)	
CS	47nF	To be used only if high common mode rejection in Aut. SBY mode and in Power Down mode is requested (note 7)
CMR	100nF	To be used only if Power on reset requested. The capacitor value depends on V_{DD} rise time.

Notes:

1) In case line cards with less than 7 subscribers are implemented CVB- capacitor should be equal to 680nF/N where N is the number of subscriber per card.
2) This shottky diode or equivalent is necessary to avoid damage to the device during hot insertion or in all those cases when a proper power up sequence cannot be guaranteed. In case the Shottky diode is not implemented the power sequence should guarantee that VB+ is always the last supply applied at power on and the first removed at power off.
   In case an other shottky diode type is adopted it must fulfill the following characteristics:
   V_F < 450mV @ I_F = n 15mA, T_{amb} = 25°C
   V_F < 350mV @ I_F = n 15mA, T_{amb} = 50°C (T_{j3000} = 90°C)
   V_F < 245mV @ I_F = n · 15mA, T_{amb} = 85°C (T_{j3000} = 120°C)
   Where n is the number of line sharing the same diode.
3) The structure of this network shall copy the SLIC output impedance multiplexed by a factor K = 10 to 25. This network must be removed when 2/4 wire conversion is implemented with 2nd generation COMBO (EG. TS5070).
4) The structure of this network shall copy the line impedance, Zline, multiplexed by a factor K = 10 to 25 and compensate the effect of CCOMP on transhybrid rejection. This network must be removed when 2/4 wire conversion is implemented with 2nd generation COMBO (EG TS5070).
5) The CINT value depends on the ringing frequency F_R.
6) Value related to Vb = 48V application, for application with different battery voltages should be properly dimensioned (see Fig 4).
7) Ex.: For line leakage resistance to GND equal to 500KΩ, the common mode rejection is 5V_P without CS and about 10Vp with CS -

Table 2

Fr (Hz)	16/18	19/21	22/27	28/32	33/38	39/46	47/55	56/68
CINT (nF)	680	580	470	390	330	270	220	180

The CINT value can be optimized experimentally for each application choosing the lower value that in correspondance of the lower ringing frequency, the minimum line lenght and the higher number of ringers doesn't produce false off-hook detection.

ELECTRICAL CHARACTERISTICS (V_{DD} = +5V; V_{SS} = -5V; V_{B+} = +72V; V_{B-} = −48V; T_{amb} = +25°C [1])

STANDBY

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{LS}	Output Voltage at L3000N Terminals	I Line = 0mA		43		V
I_{LCC}	Short Circuit Current		8.8		12.5	mA
Iot	Off-hook Detection Threshold		5.3		8.8	mA
Hys	Off-hook/on-hook Hysteresis		1.5		2.5	mA
Vls	Simmetry to Ground				.75	V

CONVERSATION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{LO}	Output Voltage at L3000N Terminals	I Line = 0mA		43		V
Ilim	Current Programmed Through the LIM and AUT Inputs		Ilim −10%		Ilim +10%	mA
Iot	Off-hook Detection Threshold		5.6		9.8	mA
Hys	Off-hook/on-hook Hysteresis		1.5		2.5	mA
Ilgk	Longitudinal Line Current with GDK Detect		6.5		15	mA

POWER-DOWN

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CN}	Input Voltage at Pin COMP to Set the Output Pin ONHK = 1				−100	mV
V_{CF}	Input Voltage at Pin COMP to Set the Output Pin ONHK = 0		100			mV
I_{COM}	Output Current at Pin COMP	COMP = GND		20		µA

SUPPLY CURRENT

Symbol	Parameter		Min.	Typ.	Max.	Unit
I_{DD}	Positive Supply Current	Power Down/aut. Stand-by		5.7		mA
	CS = 1	Stand-by		7.5		mA
		Conversation		11.7		mA
		Ringing		11.3		mA
I_{SS}	Negative Supply Current	Power Down/aut. Stand-by		4.2		mA
	CS = 1	Stand-by		4.2		mA
		Conversation		8.2		mA
		Ringing		8.2		mA
I_{BAT-}	Negative Battery Supply Current	Power Down/aut. Stand-by		0		mA
	Line Current = 0mA	Stand-by		2	2.5	mA
		Conversation		5	6.5	mA
		Ringing		14	17	mA
I_{BAT+}	Positive Battery Supply Current	Power Down/aut. Stand-by		0		µA
	Line Current = 0mA	Stand-by		10	15	µA
		Conversation		10	15	µA
		Ringing		12	13.5	mA

AC OPERATION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Zlx	Sending Output Impedance on TX				15	Ω
THD	Signal Distortion at 2W and 4W Terminals	Vtx = 0dBm @ 1020Hz			0.3	%
Rl	2W Return Loss	f = 300 to 3400Hz	22			dB
Thl	Transhybrid Loss	f = 300 to 3400Hz $20\log_{10}\left\|\frac{V_R}{V_S}\right\|$	30			dB
Gs	Sending Gain (2)	Vso = 0dBm; f = 1020Hz	–6.27	–6.02	–5.77	dB
Gsf	Sending Gain Flatness vs. Frequency	f = 300 to 3400Hz Respect to 1020Hz	–0.1		+0.1	dB
Gl	Sending Gain Linearity	fr = 1020Hz Vsoref = –10dBm Vso = +4 / –40dBm	–0.1		+0.1	dB
Gr	Receiving Gain	Vrl = 0dBm; f = 1020Hz	–0.25		+0.25	dB
Grf	Receiving Gain Flatness	f = 300 to 3400Hz Respect to 1020Hz	–0.1		+0.1	dB
Grf	Receiving Gain Linearity	fr = 1020Hz Vrlref = –10dBm Vrl = +4 / –40dBm	–0.1		+0.1	dB
Np4W	Psophomet. Noise 4W - Tx Terminals			–79	–74	dBmp
Np4W	Psophomet. at Line Terminals			–75	–70	dBmp
SVRR	Supply Voltage Rejection Ratio Relative to VB–	f = 10Hz Vn = 100mVrms		–20		dB
		f = 1KHz Vn = 100mVrms			–35	dB
		f =3.4KHz Vn = 100mVrms			–30	dB
Ltc	Longitudinal to Transversal Conversion	f = 300 to 3400Hz I line = 30mA ZML = 600Ω				
Tlc	Transversal to Longitudinal Conversion		48	51		dB

Notes:
(*) 52dB using selected L3000N
(1) The datasheet certifies the electrical characteristics at 25°C. For applications requiring operations in the standard temperature range (0°C to 70°C) use L3000N/L3092 If operations are required in the extended temperature range (-40°C to +85°C), use the kit L3000NT/L3092T.
(2) value optimized for programmable COMBO Hybrid Balance Filter

RINGING PHASE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Vir	Superimposed DC Voltage	Rloop > 100KΩ	19		27	V
		Rloop = 1KΩ	17		25	V
Vacr	Ringing Siganl at Line Terminal	Rloop > 100kΩ V_{RGN} = 1.5Vrms/30Hz	56.0			Vrms
		Rloop = 1KΩ + 1µF V_{RGN} = 1.5Vrms/30Hz	56.0			Vrms
If	DC Off-hook Del Threshold			5.5		mA
Ilim	Output Current Capability		85		130	mA
Vrs	Ringing Symmetry				2	Vrms
THDr	Ringing Signal Distortion				5	%
Zir	Ringing Amplicat. Input Impedance	L3092's Pin RGIN	50			KΩ
Vrr	Residual of Ringing Signal at Tx Output				100	mVrms
Trt	Ring Trip Detection Time	fring = 25Hz (T = 1/fring) CINT = 470nF		80(3T)		ms
Toh	Off-hook Status Delay after the Ringing Stop				50	µs

DIGITAL INTERFACE ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V; V_{SS} = -5V; T_{amb} = 25°C (1))

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Vil	Input Voltage at Logical "0"	Pins CS PWON LIM	0		0.8	V
Vih	Input Voltage at Logical "1"		2		5	V
Vil	Input Voltage at Logical "0"	Pins RNG-AUT	0		0.5	V
Vih	Input Voltage at Logical "1"		2.3		5	V
Iil	Input Current at Logical "0"	All logic pins Vil = 0V Vih = 5V			15	µA
Iih	Input Current at Logical "1"				25	µA
Vol	Output Voltage at Logical "0"	Pins ONHK GDK Iout = -1mA Iout = 1mA			0.4	V
Voh	Output Volatge at Logical "1"		2.4			V
Ilk	Tristate Leak Current	CS = "1"			10	µA
I_{MR}	Pull-up MR Output Current	MR = "0"		50		µA

DYNAMIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Tsd	PWON, RING, AUT, LIM		1500			ns
Thd	PWON, RING, AUT, LIM		0			ns
Tww	CS Impulse Width (writing op.)		1500			ns
Thv	ONHK, GDK Data Out to "0" CS Delay				600	ns
Tvh	ONHK, GDK High Imped. to "1 "CS Delay				600	ns
Twr	CS Impulse Width (writing op.)		800			ns

(1) The datasheet certifies the electrical characteristics at 25°C. For applications requiring operations in the standard temperature range (0°C to 70°C) use L3000N/L3092. If operations are required in the extended temperature range (-40°C to +85°C), use the kit L3000NT/L3092T.

Figure 8: Writing Operating Timing (controller to SLIC).

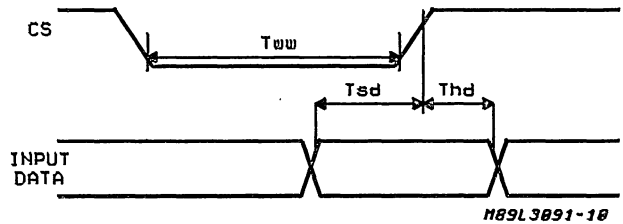


Figure 9: Reading Operating Timing (from SLIC to controller).

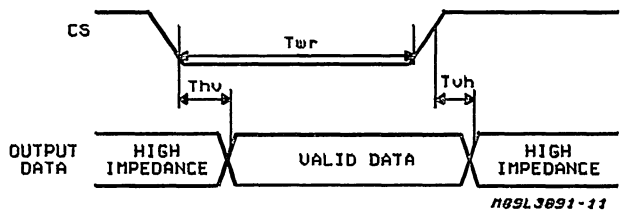
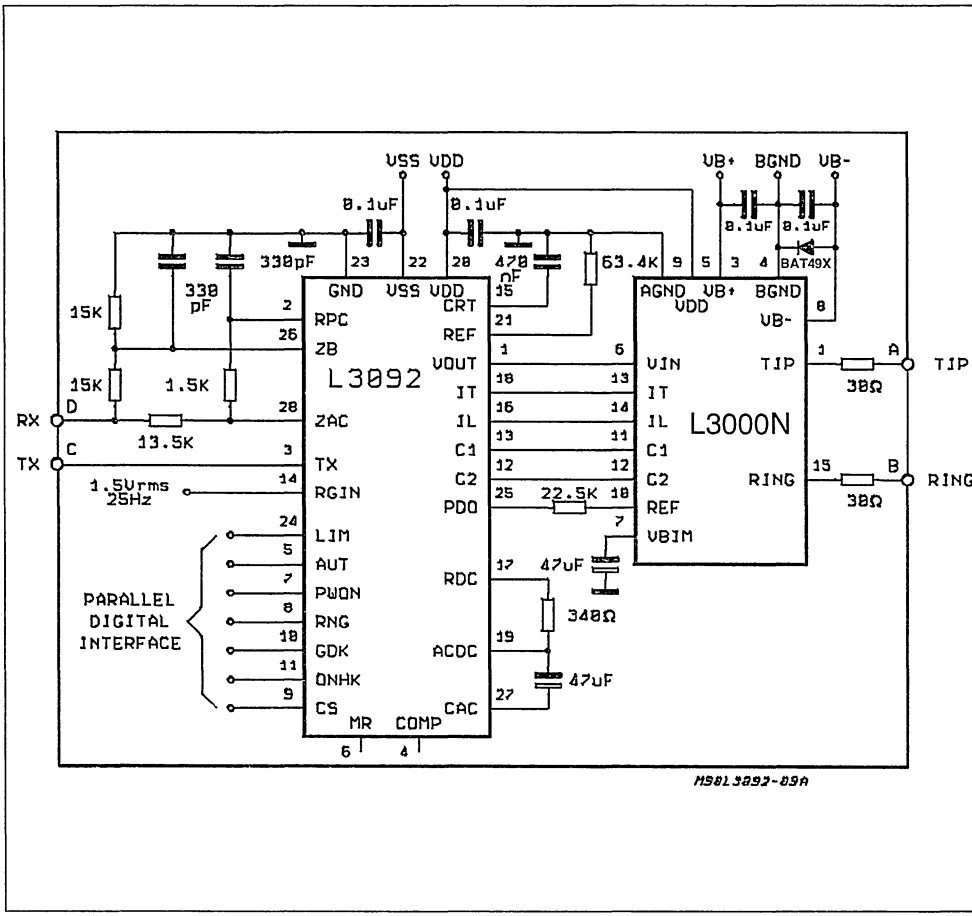


Figure 10: Test Circuit



A, B, C, D are test reference points used during testing.

Figure 11: Typical Application Circuit with 2nd Generation COMBO for Complete Subscriber Circuit (Protection - SLIC - COMBO).

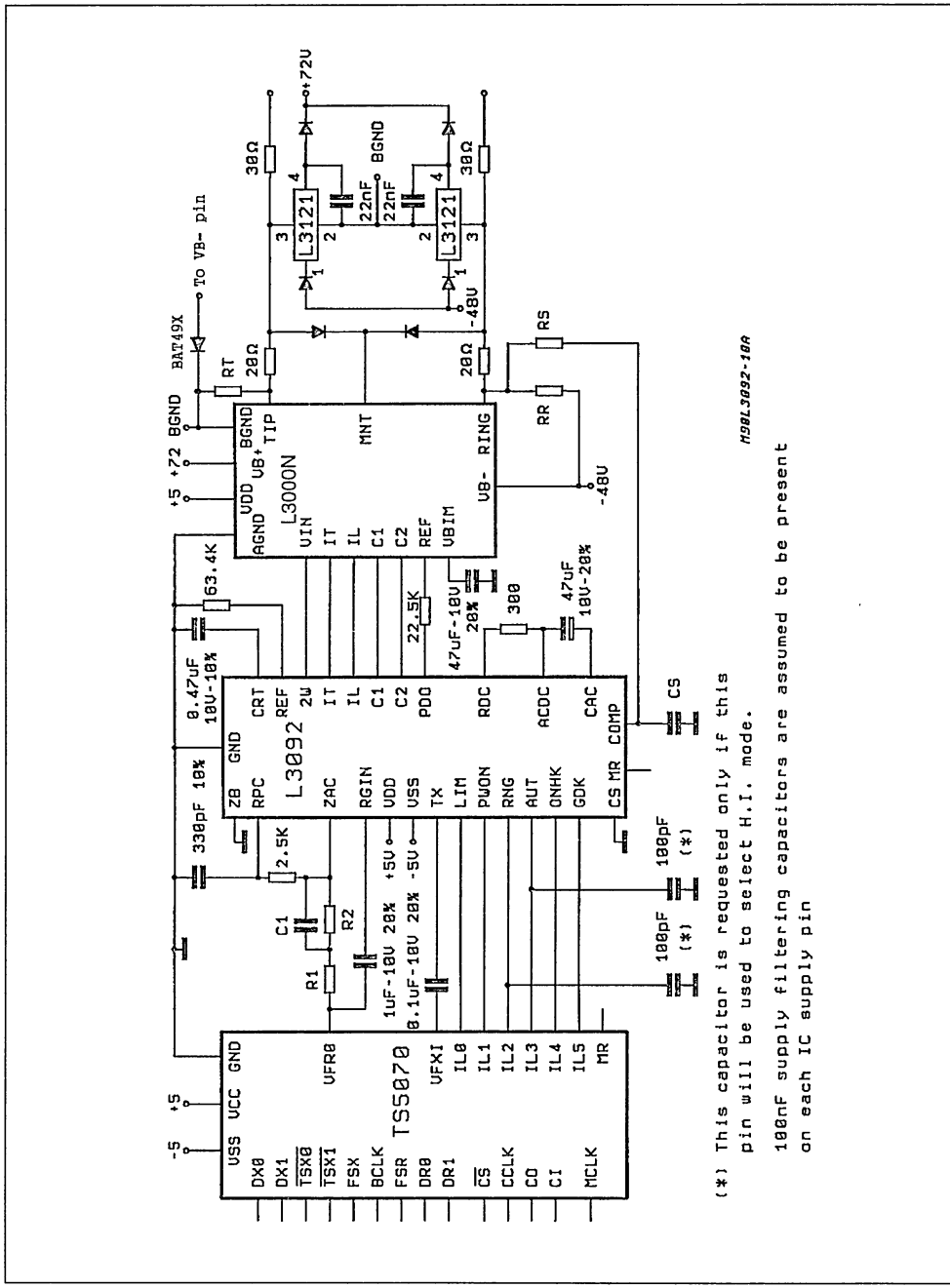
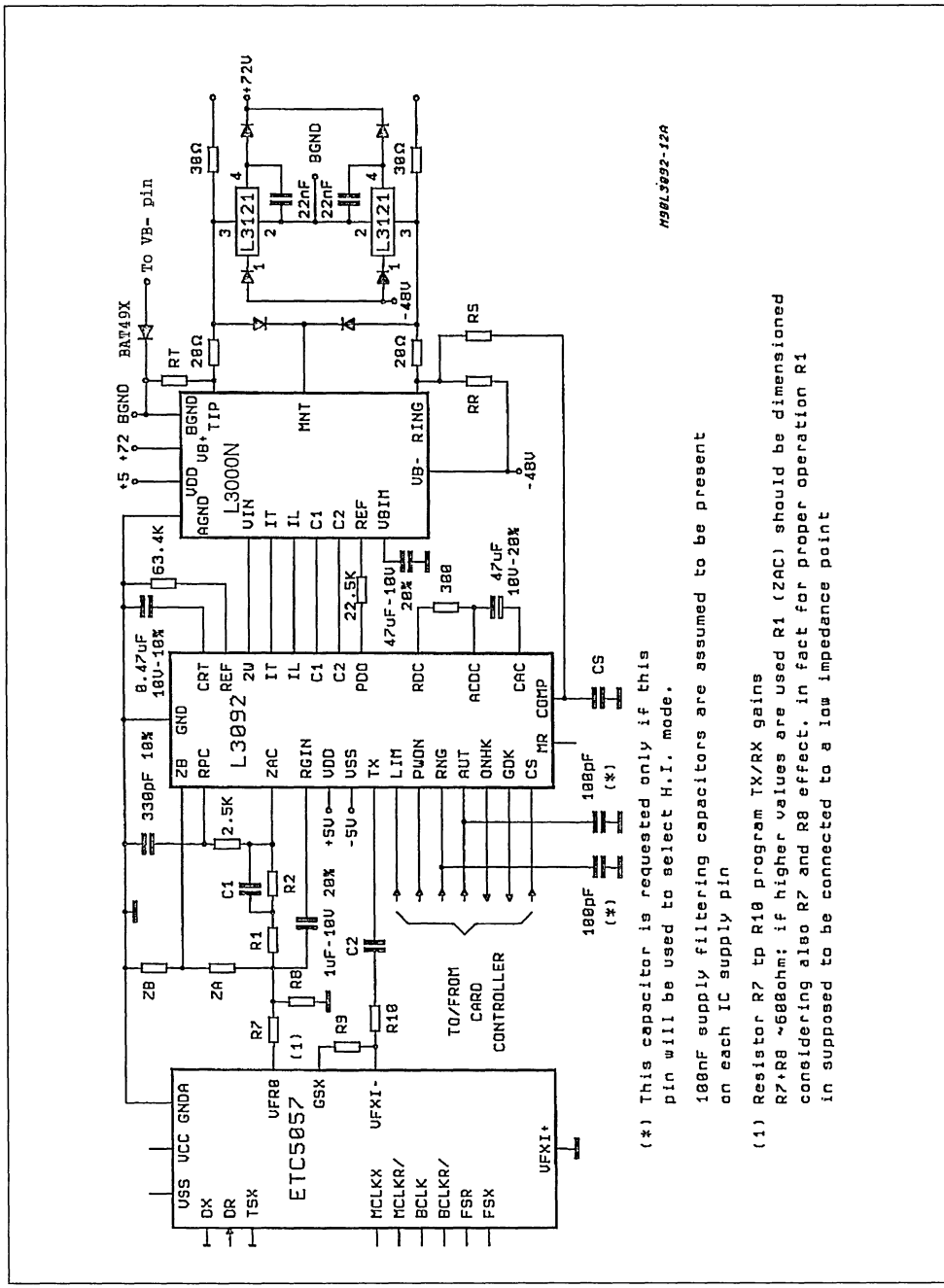


Figure 12: Typical Application Circuit with 1st Generation COMBO for Complete Subscriber Circuit (Protection - SLIC - COMBO).



APPENDIX A

SLIC TEST CIRCUITS

Referring to the test circuit reported at the end of each SLIC data sheet here below you can find the proper configuration for each measurement.
In particular:

A-B: Line terminals
C: Tx sending output on 4W side
D: Rx receiving input on 4W Side
E: TTx teletaxe signal input
R_{GIN}: low level ringing signal input.

TEST CIRCUITS

Figure A1: Symmetry to Ground

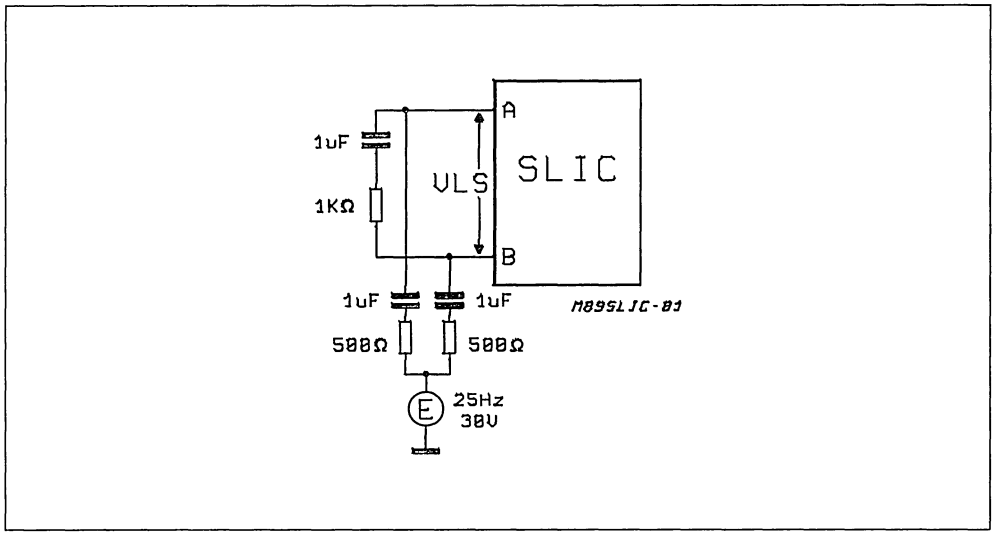
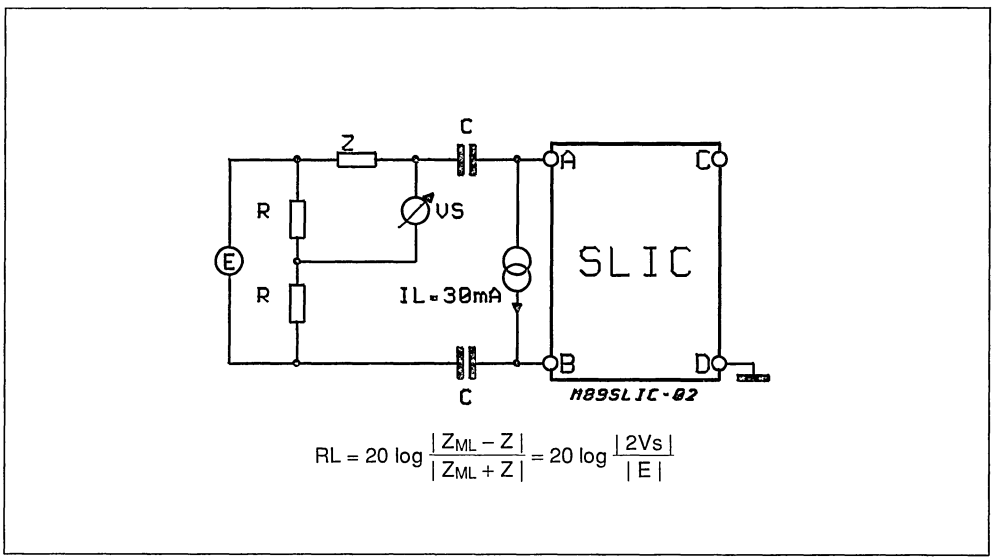


Figure A2: 2W Returns Loss



$$RL = 20 \log \frac{|Z_{ML} - Z|}{|Z_{ML} + Z|} = 20 \log \frac{|2Vs|}{|E|}$$

TEST CIRCUITS (continued)
Figure A3: Trans-hybrid Loss.

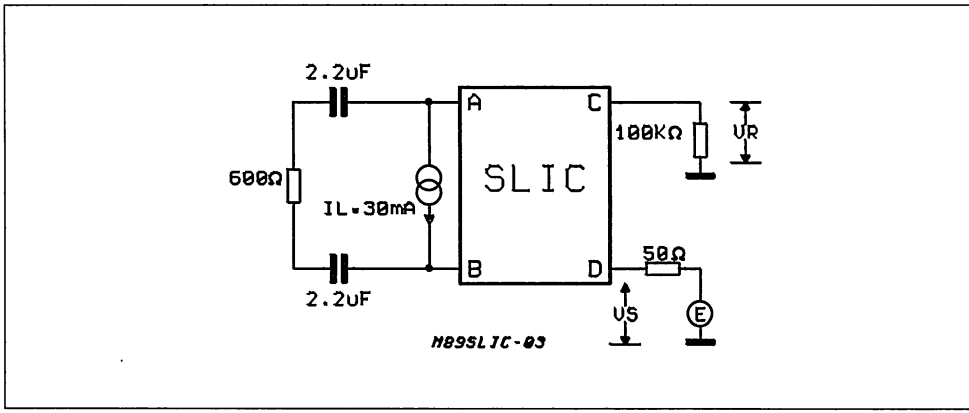


Figure A4: Sending Gain

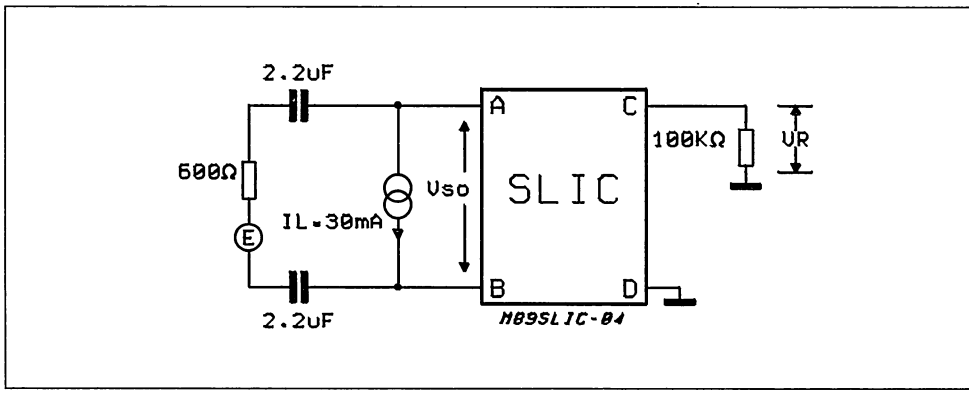
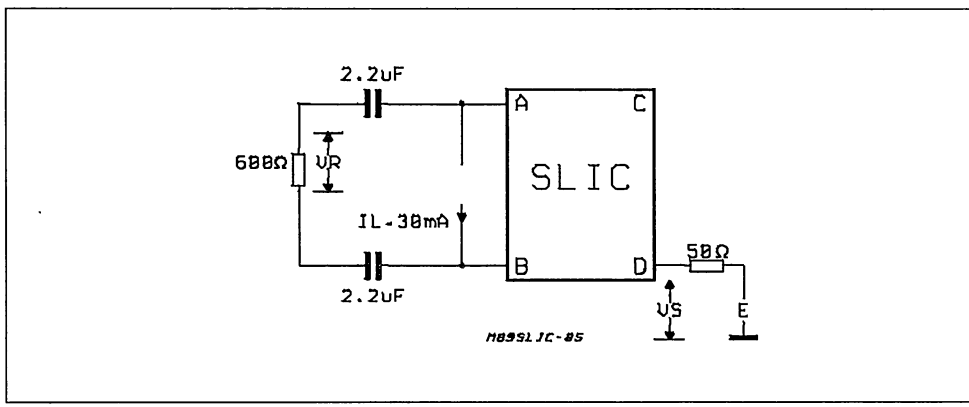


Figure A5: Receiving Gain



TEST CIRCUITS (continued)
Figure A6: PSRR Relative to Battery Voltage VB-

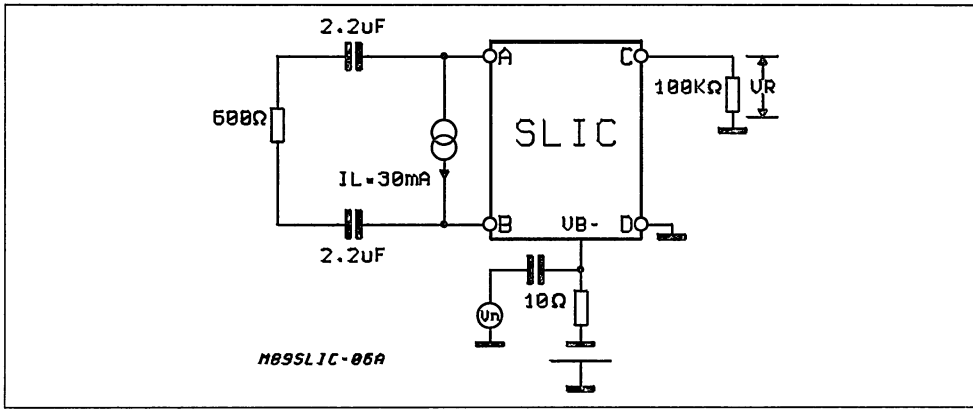


Figure A7: Longitudinal to Transversal Conversion

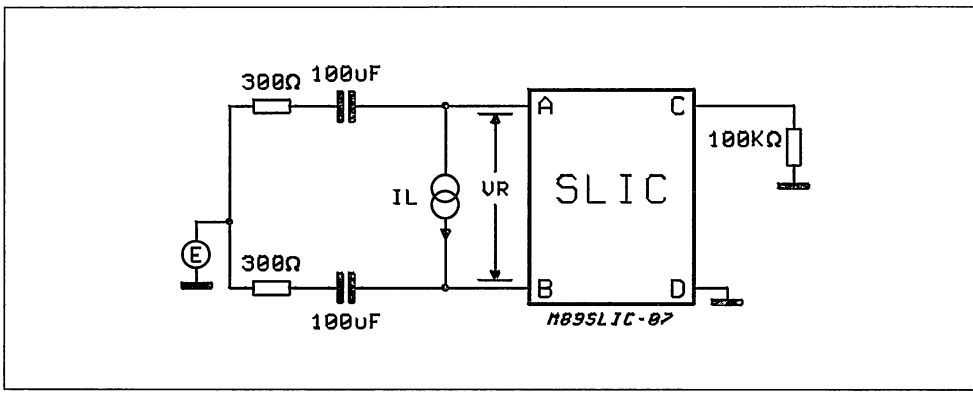
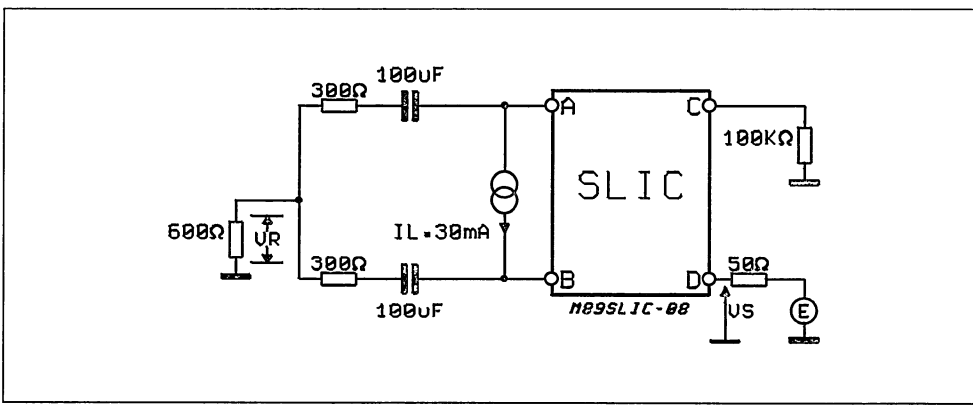


Figure A8: Longitudinal to Transversal Conversion



TEST CIRCUITS (continued)
Figure A9: TTX Level at Line Terminals

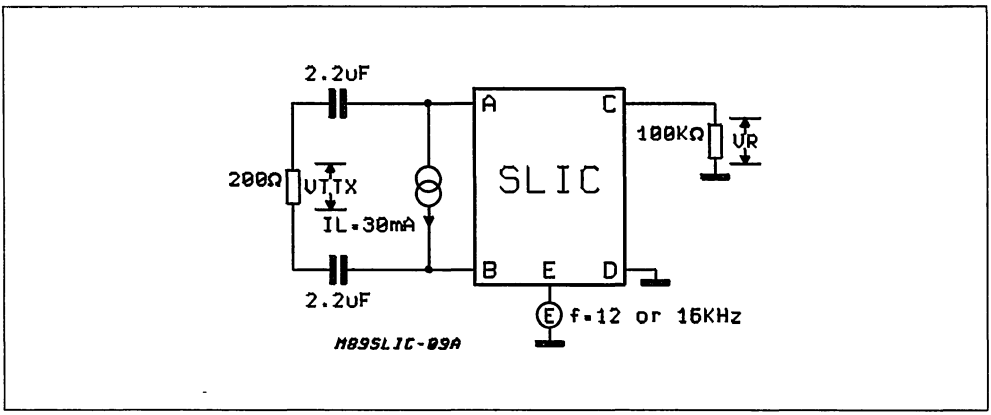
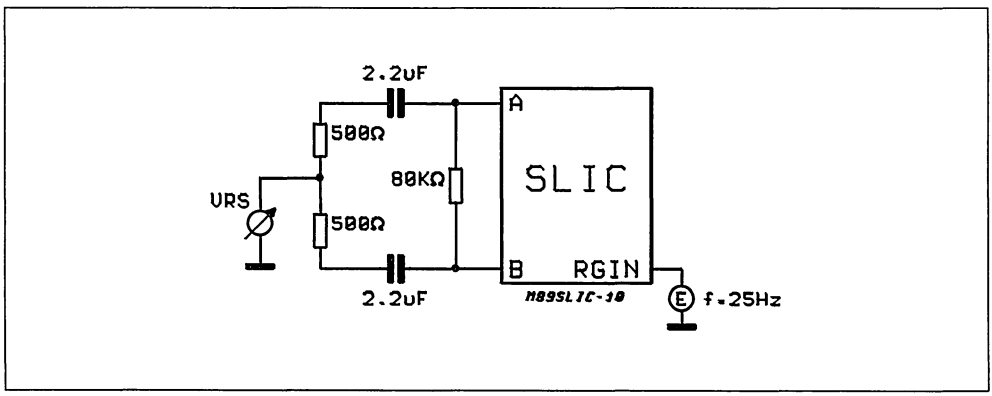


Figure A10: Ringing Simmetry



APPENDIX B

ADDITIONAL OPERATING FEATURES

Two further operating modes are provided on the L3092, boosted battery and ring pause. Both of these Modes are accessed by appllying a high impedance on inputs AUT and or RING of the digital interface.

1.Boosted Battery (BB)

This operating mode is equivalent to conversation mode with respect to AC and signaling functions but with the following changes to the DC characteristics:

a) Current limiting value fixed at 25mA.

b) Characteristic in the resistive feeding region corresponds to a battery voltage equal to (-5 + $|VB_-|$ + VB_+)Volt in series with the same feeding resistor utilized in the DC characteristic of conversation mode.

BB mode is typically used to feed long lines (20mA/4Kohm) and to implement special functions such as message waiting where high voltage signals are required.

Further information about this opersating mode may be found by referring to the L3000/L3030 datasheet.

2.Ringing Pause Mode

During Ring Pause - Mode the SLIC is always in ringing mode but the AC ringing signal is not injected into the line. This mode allows to avoid any common mode voltage variation of TIP and RING wire during the transition bteween Ringing Burst and Ringing Pause. This feature is used in application where it is mandatory to avoid perturbations on adjacent lines during ringing injection. For example when in the same system analog lines are used both for speech and modem transmission.

The following table shows all operating modes of L3000/L3092 SLIC KIT. Boosted Battery or Ringing Pause Modes are selected by applying a high impedance (HI) to input pins RNG and/or AUT.

Included also in this table are the operating modes to which the SLIC defaults automatically during ringing mode when OFF HOOK is detected.

CONTROL INTERFACE BETWEEN THE SLIC AND THE CARD CONTROLLER

Operating Mode	Input Pin				Output Pin	
	RNG	PWON	AUT	LIM	ONHK	GDK
Conversation 25mA Conversation 40mA Conversation 60mA	0 0 0	1 1 1	1 0 0	X 1 0	1 on-hook 0 off-hook	1 Ground key not detected 0 Ground key detected
Boosted Battery 25mA	0	1	HI	X		
Stand-by	0	0	0	X		Disable
Automatic Stand-by	1	0	1	X		
Power Down	1	0	0	X	C1 Comparator Output	Disable
Test Mode	0	0	1	X	1 on-hook 0 off-hook	0 Limiting Region 1 Resistive Region
Ringing Inj. (CVS 25mA) Ringing Inj. (CVS 40mA) Ringing Inj. (CVS 60mA)	1 1 1	1 1 1	1 0 0	x 1 0		
Ringing Inj. (BB 25mA)	1	1	HI	X		
Ringing Pause (CVS 25mA) Ringing Pause (CVS 40mA) Ringing Pause (CVS 60mA)	HI HI HI	1 1 1	1 0 0	X 1 0	1 on-hook 0 off-hook	Disable
Ringing Pause (BB 25mA)	HI	1	HI	X		

NB:
HI = High Impedance
BB = Boosted Battery

APPENDIX C

LAYOUT SUGGESTIONS

Standard layout rules should be followewd in order to get the best system performances:

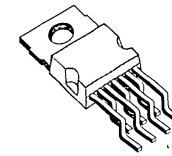
1) Use always 100nF filtering capacitor close to the supply pins of each I.C.
2) Connect together BGND and AGND at a low impedance point. (e.g. on a ground plane common to the line card).
3) The L3092 bias resistor (RL) should be connected close to the corresponding pins of L3092 (REF and GND).
   Avoid any digital line to pass close to REF pin.
   Eventually screen REF pin with a GND track.

SGS-THOMSON MICROELECTRONICS

L3234
L3235

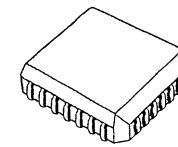
HIGHLY INTEGRATED SLIC KIT TARGETED TO PABX AND KEY SYSTEM APPLICATIONS

- HIGHLY INTEGRATED SUBSCRIBER LINE INTERFACE KIT FOR PABX AND KEY SYSTEM APPLICATIONS
- IMPLEMENTS ALL KEY ELEMENTS OF THE BORSCHT FUNCTION
- INTEGRATED ZERO CROSSING BALANCED RINGING INJECTION ELIMINATES EXTERNAL RELAY AND CENTRALISED RINGING GENERATOR
- ZERO NOISE INJECTED ON ADJACENT LINES DURING RINGING SEQUENCE
- LOW POWER IN STANDBY AND ACTIVE MODES
- BATTERY FEED WITH PROGRAMMABLE LIMITING CURRENT
- PARALLEL LATCHED DIGITAL INTERFACE
- SIGNALLING FUNCTIONS (OFF HOOK, GND-KEY)
- LOW NUMBER OF EXTERNAL COMPONENTS
- INTEGRATED THERMAL PROTECTION
- INTEGRATED OVER CURRENT PROTECTION
- 0°C TO 70°C: L3234/L3235
- -40°C TO 85°C: L3234T/L3235T



HEPTAWATT

ORDERING NUMBER: L3234



PLCC28

ORDERING NUMBER: L3235

DESCRIPTION

The L3234/L3235 is a highly integrated SLIC KIT targeted to PABX and key system applications

The kit integrates the majority of functions required to interface a telephone line. The L3234/L3235 implements the main features of the broths function:

- Battery Feed (Balanced Mode)
- Ringing Injection
- Signalling Detection
- Hybrid Function

The Kit comprises 2 devices, the L3234 ringing injector fabricated in Bipolar in 140V Technology.

Its function is to amplify and inject in balanced mode with zero crossing the ringing signal. The device requires an external positive supply of 100V and a low level sinusoid of approx. 950mVrms. The L3235 Line Feeder is integrated in 60V Bipolar Technology. The L3235 provides battery feed to the line with programmable current limitation. The two to four wire voice frequency signal conversion is implemented by the L3235 and line terminating and balance impedances are externally programmable. The L3234/L3235 kit is designed for low power dissipation. In a short loop condition the extra power is dissipated on an external transistor. The Kit is controlled by five wire parallel bus and interfaces easily to all first and programmable second generation COMBOS. (see figg. 1 and 2)

Figure 1: Typical Application Circuit with Second Generation COMBO for Complete Subscriber Circuit (Protection-SLIC-COMBO)

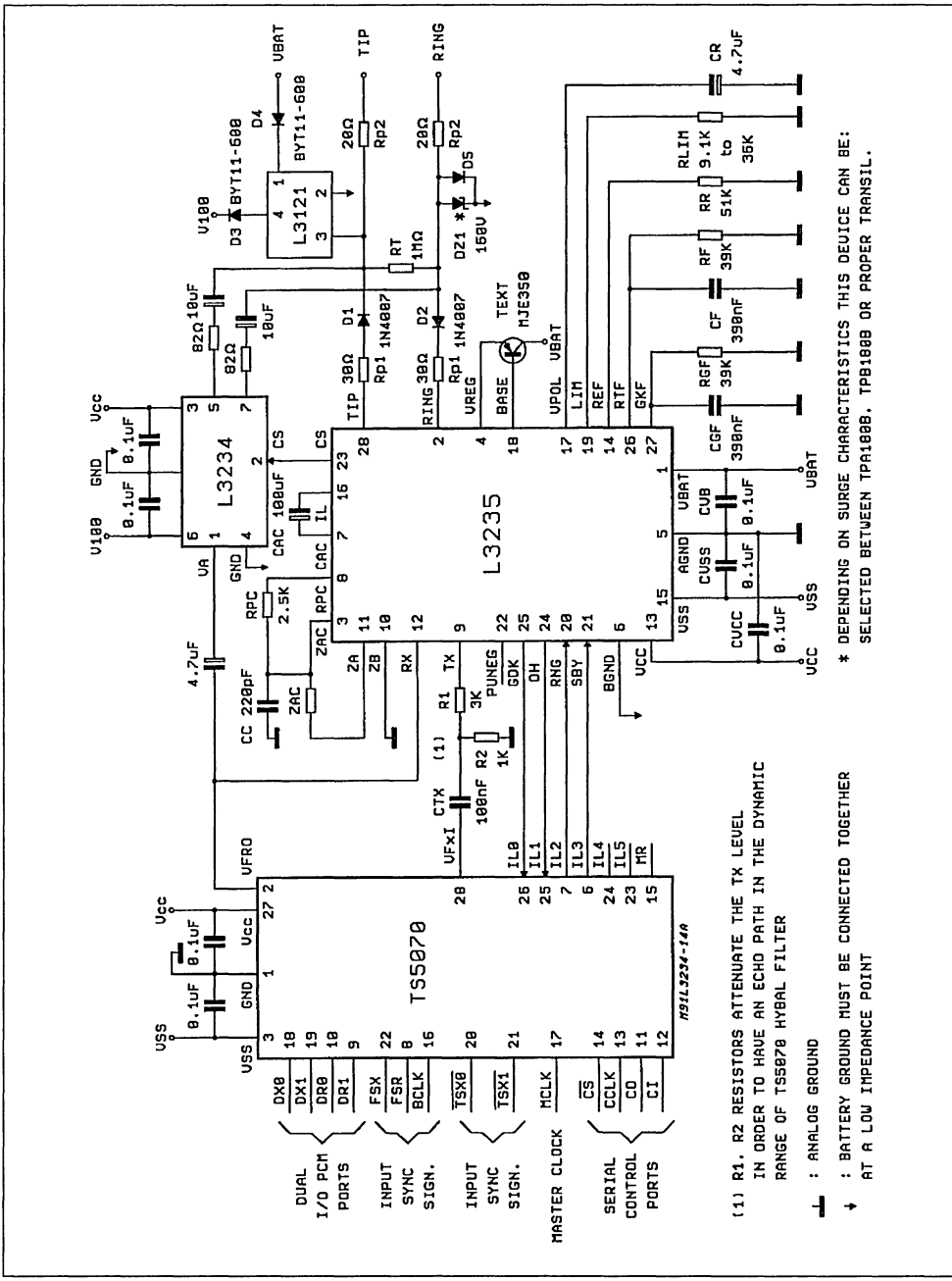
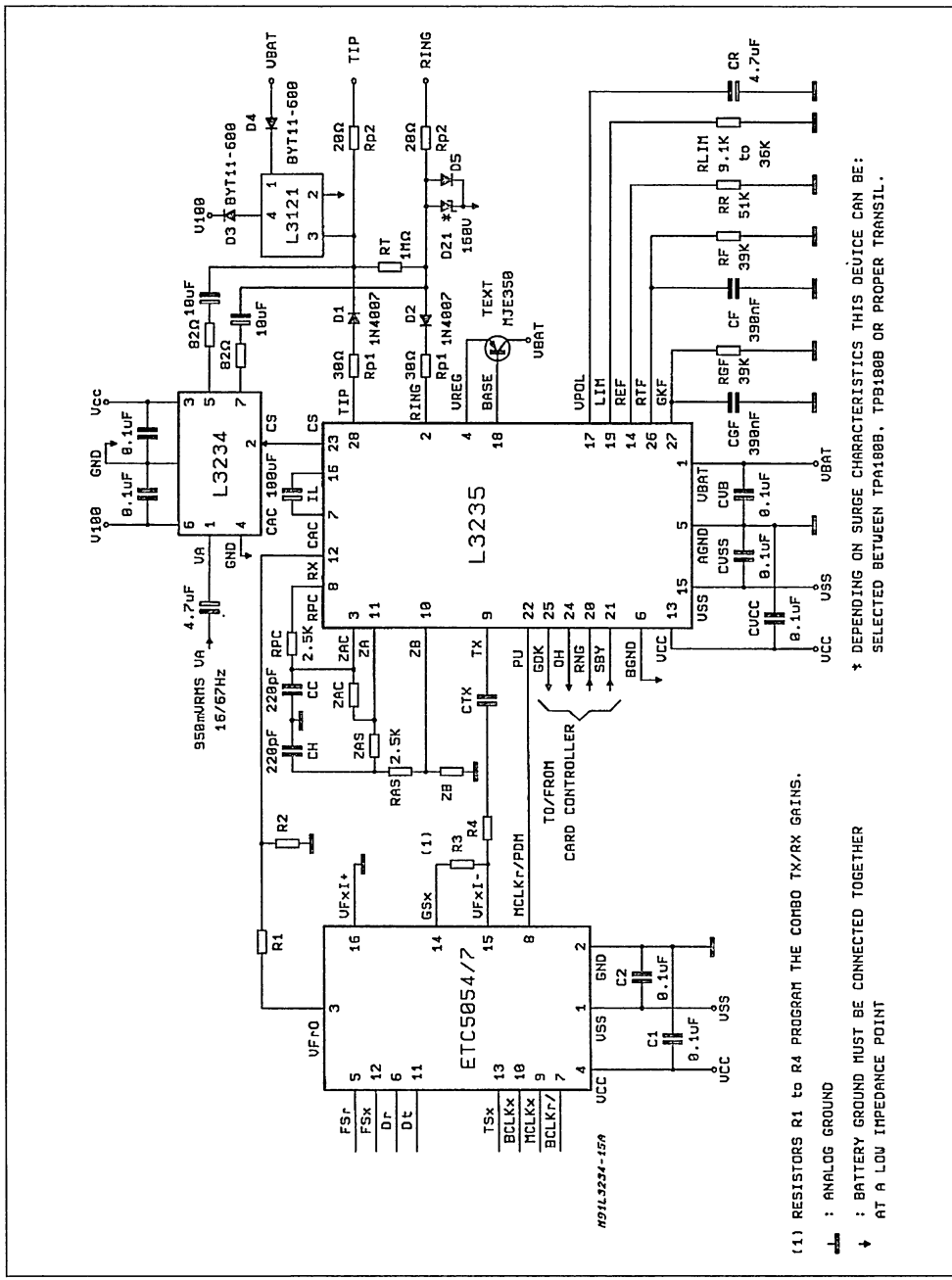


Figure 2: Typical Application Circuit with First Generation COMBO for Complete Subscriber Circuit (Protection-SLIC-COMBO)



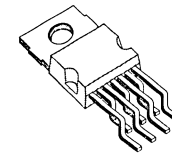
L3234
Solid State Ringing Injector

DESCRIPTION

The L3234 is a monolithic integrated circuit which is part of a kit of solid state devices for the subscriber line interface. The L3234 sends a ringing signal into a two wires analog telephone line in balanced mode. The AC ringing signal amplitude is up to 60Vrms, and for that purpose a positive supply voltage of +100V shall be available on the subscriber card.

The L3234 receives a low amplitude ringing signal (950mVrms) and provide the voltage/current amplification (60Vrms/70mA) when the enable input is active (CS $\geq$ 2V). In disable mode (CS $\leq$ 0.8V) the power consumption of the chip is very low (<14mW).

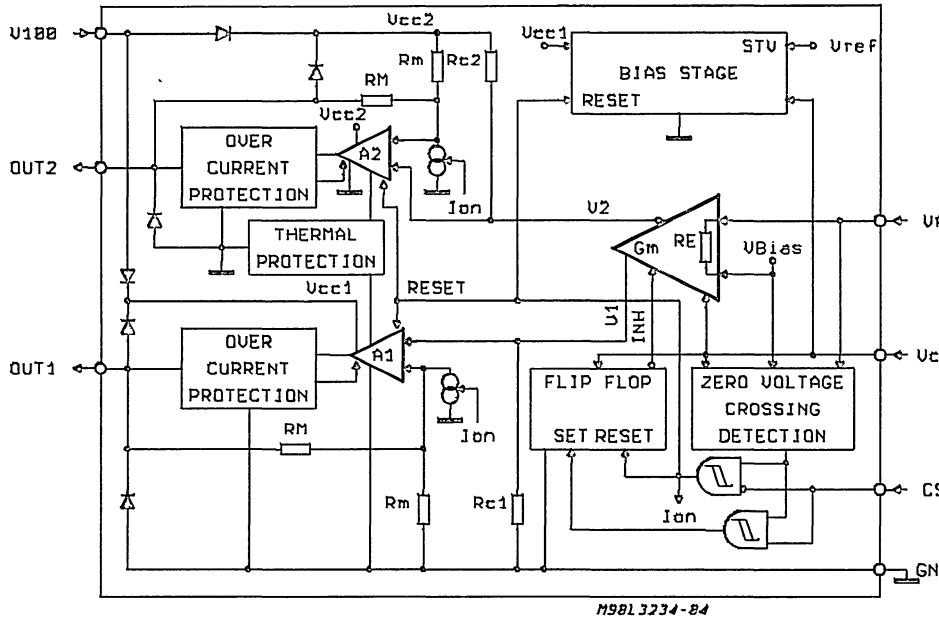
The circuit is designed with a high voltage bipolar technology (V_{CEO} > 140V / V_{CBO} > 250V).



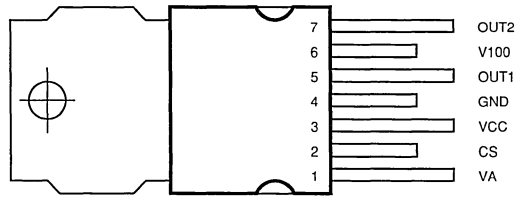
HEPTAWATT

The package is a moulded plastic power package (Heptawatt) suitable also for surface mounting.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V100	Positive Power Supply Voltage	+120	V
V_{CC}	5V Power Supply Voltage	5.5	V
V_A	Low Voltage Ringing Signal (with V100 = 120Vdc)	1.4	Vrms
CS	Logical Ring Drive Input	V_{CC}	
T_j	Max. Junction Temperature	150	°C
T_{stg}	Storage Temperature	-55 to +150	°C

OPERATING RANGE

Symbol	Parameter	Value	Unit
V100	High Power Supply Voltage	95 to 105	V
V_{CC}	Low Power Supply Voltage	5 ±5%	V
V_A	Low Voltage Ringing Signal	600 to 950 within 10Hz - 100Hz	Vrms
T_{op}	Operating Temperature for **L3234** **L3234T**	0 to 70 -40 to 85	°C °C
T_{jop}	Max. Junction Operating Temperature (due to thermal protection)	130	°C

Note: Operating ranges define those limits between which the functionality of the device is guaranteed

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max.	4	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	50	°C/W

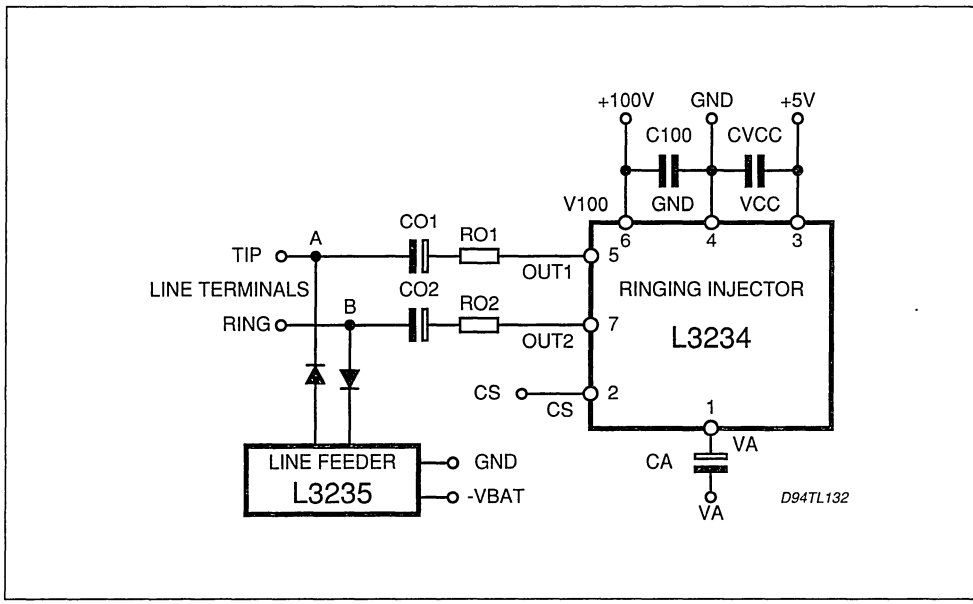
PIN DESCRIPTION

Pin	Name	Description
1	VA	Low Voltage Ringing Signal Input
2	CS	Logical Ring Drive Input
3	V_{CC}	+5V Low Power Supply
4	GND	Common Analog-Digital Ground
5	OUT1	Ringing Signal Output
6	V100	+100V High Power Supply

OPERATION DESCRIPTION

The Fig. 3 show the simplified circuit configuration of the L3234 Solid State Ringing injector when used with the L3235 Line Feeder.

Figure 3: L3234/L3235 Circuit Configuration



EXTERNAL COMPONENTS LIST

In the following table are shown the recommended external components values for L3234.

Ref.	Value	Involved Parameter or Function
R01, R02	82Ω	Ringing Feeding Series Resistors
C01, C02	10μF - 160V	Ringing Feeding De coupling Capacitors
CA	4.7μF - 10V	Low Level Ringing Signal De coupling Capacitor
C100	100nF - 100V	Positive Battery Filter
CV_{CC}	100nF	+5V Supply Filter

When the ringing function is selected by the subscriber card, a low level signal is continuously applied to pin 1 through a de coupling capacitor. Then the logical ring drive signal CS provided by L3235 is applied to pin 2 with a cadenced mode.

The ringing cycles are synchronised by the L3234 in such a way that the ringing starts and stops always when the analog input signal crosses zero.

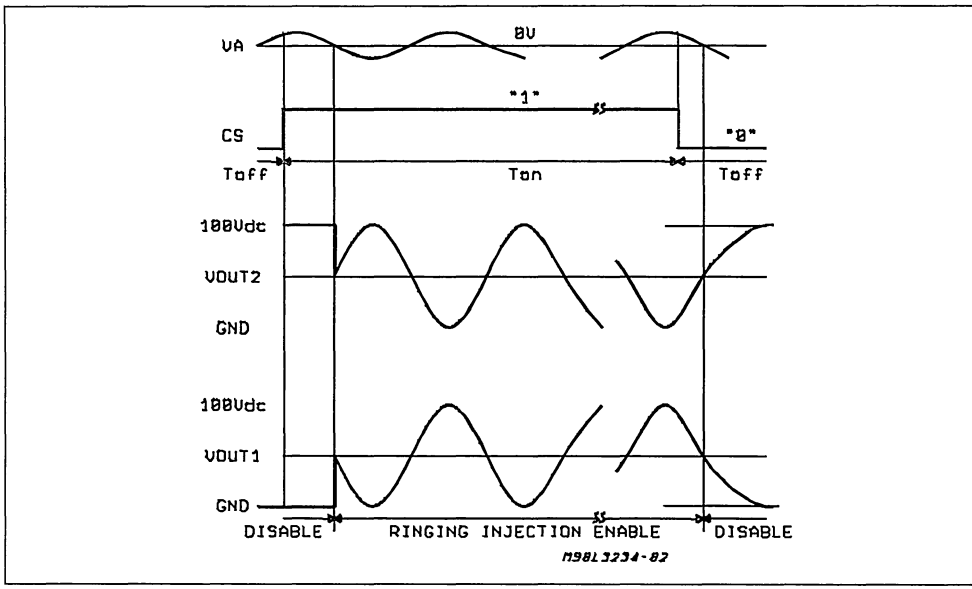
When the ringing injection is enabled (CS = "1"), an AC ringing signal is injected in a balanced mode into the telephone line.

When the ringing injection is disabled (CS = "0"), the output voltage on OUT2 raises to the high power supply, whereas on OUT1, it falls down to ground.

The L3234 has a low output impedance when sending the signal, and high output impedance when the ringing signal is disabled

In fig. 4 the dynamic features of L3234 are shown.

Figure 4: Dynamic Features of L3234



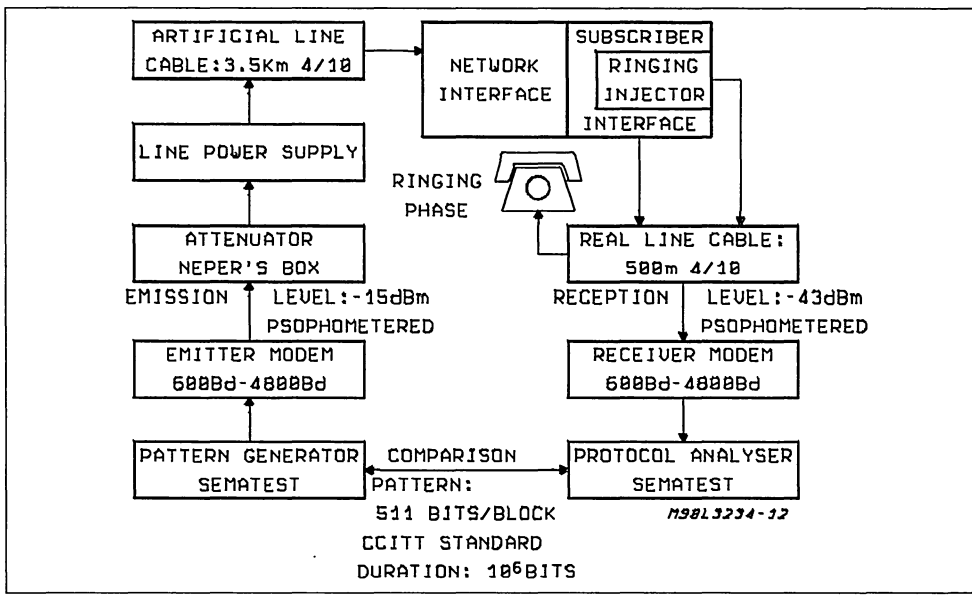
DATA TRANSMISSION INTERFERENCE TEST

The L3234 meet the requirements of the technical specification ST/PAA/TPA/STP/1063 from the CNET. The test circuit used is indicated below.

The measured error rate for data transmission is lower than 10^{-6} during the ringing phase.

This test measures if during the ringing phase the circuit induce any noise to the closer lines.

Figure 5: Test Circuit Data Transmission Interference Test

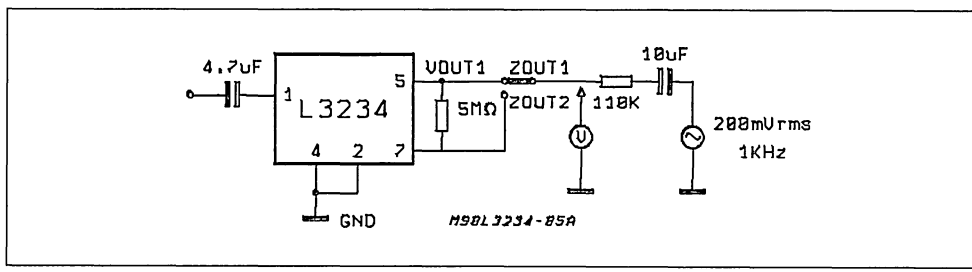


ELECTRICAL CHARACTERISTICS (Test conditions: V100 = +100V, V_{CC} = +5V, T_{amb} = 25°C, unless otherwise specified)

Note: Testing of all parameter is performed at 25°C. Characterisation, as well as the design rule used allow correlation of tested performance with actual performances at other temperatures. All parameters listed here are met in the range 0°C to +70°C. For applications requiring operations in the standard temperature range (0°C to 70°C) use L3234. If operations are required in the extended temperature range (-40°C to 85°C), use the L3234T.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig
STAND BY MODE: CS = "0"							
I_S (V100) I_S (V_{CC})	Consumption	VA = 950mVrms; 50Hz		45 560	100 800	µA µA	
V_{SOUT1} V_{SOUT2}	DC Output Voltage	VA = 950mVrms; 50Hz	 92		6	V V	
Z_{SOUT1} Z_{SOUT2}	Output Impedance		70 70			kΩ kΩ	6
	Z_{OUT} Matching				15	%	
THD	Harmonic Distortion During Emission	$V_{LINE} \leq$ 6dBm; f = 1kHz		-46	-40	dB	7
RINGING PHASE: CS = "1" DC OPERATION							
I_R (V100) I_R (V_{CC})	Consumption	$Z_{LINE} = \infty$ VA = 950mVrms; 50Hz		2.5 2.2	5 3	mA mA	
V_{ROUT1} V_{ROUT2}	DC Output Voltage	VA = 0V	44 44		56 56	V V	
V_{IH} I_{IH} (CS = 0)	Threshold Voltage on the Logical Input CS	VA = 950mVrms; 50Hz	2.0		 1	V µA	8
V_{IL} I_{IL} (CS = 0)					0.8 1	V µA	
I_{lim}	DC Line Current Limitation	VA = 0V	70		150	mA	12
AC OPERATION							
V_{OUT1}/VA V_{OUT2}/VA	Ringing Gain	Z_{LINE} = 2.2µF + 1kΩ VA = 0dBm	29.5 29.5	30 30		dB dB	9
V_{OUT1} -V_{OUT1}	Ringing Signal	ZLINE = 2.2µF + 1kΩ VA = 950mVrms; 50Hz	57	60		Vrms	9
THD V_{LINE}	Harmonic Distortion	VA = 950mVrms; 50Hz			5	%	
Z_{IN} (VA)	Input Impedance	VA = 950mVrms; 50Hz	40			kΩ	10
Z_{OUT}	Differential Output Impedance	I_{LINE} < 50mArms			20	Ω	11

TEST CIRCUITS
Figure 6.



TEST CIRCUITS (continued)
Figure 7.

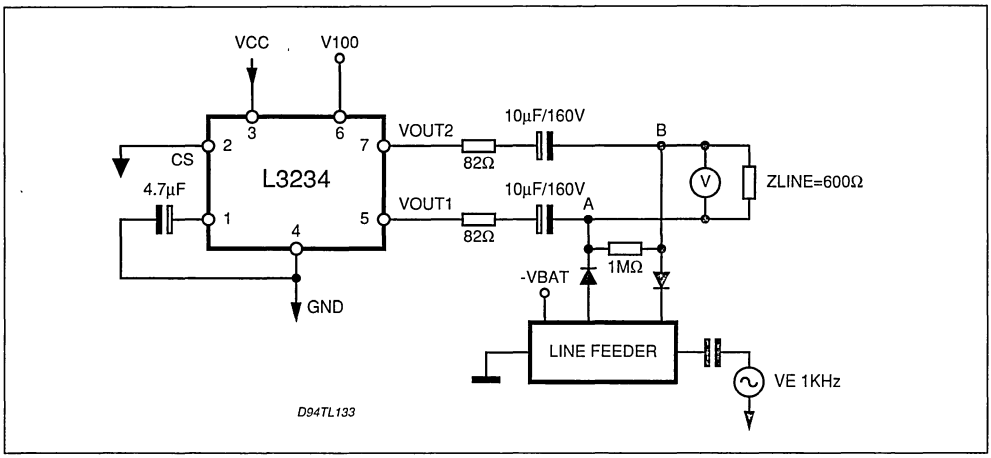


Figure 8.

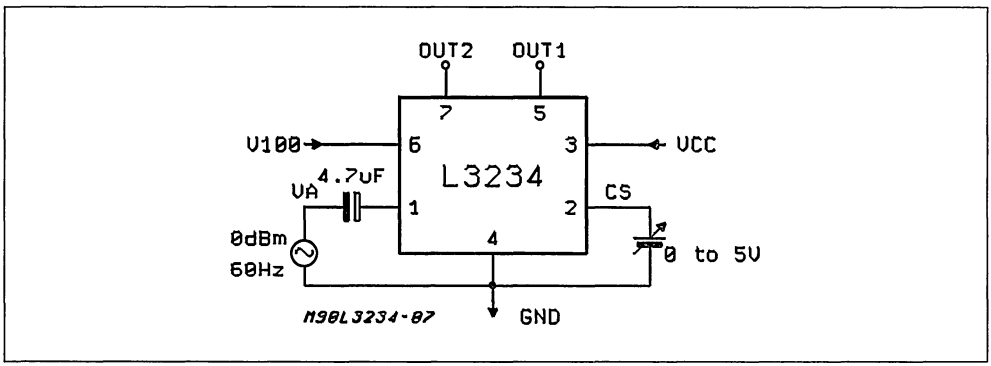
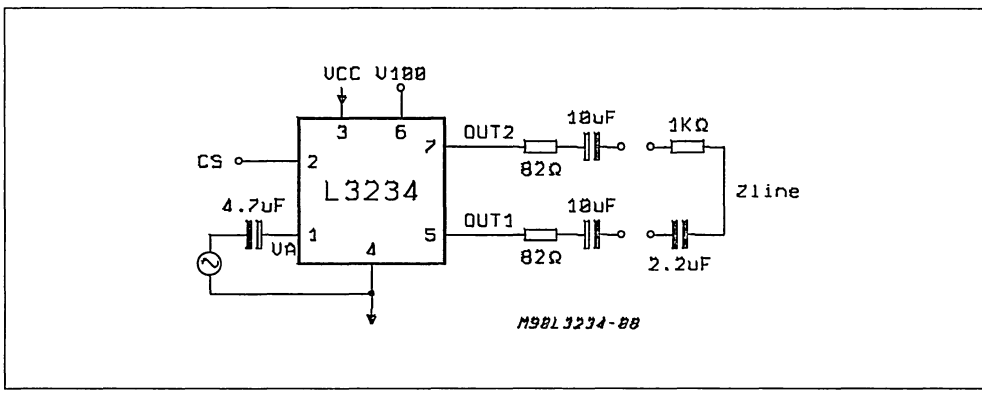


Figure 9.



TEST CIRCUITS (continued)
Figure 10.

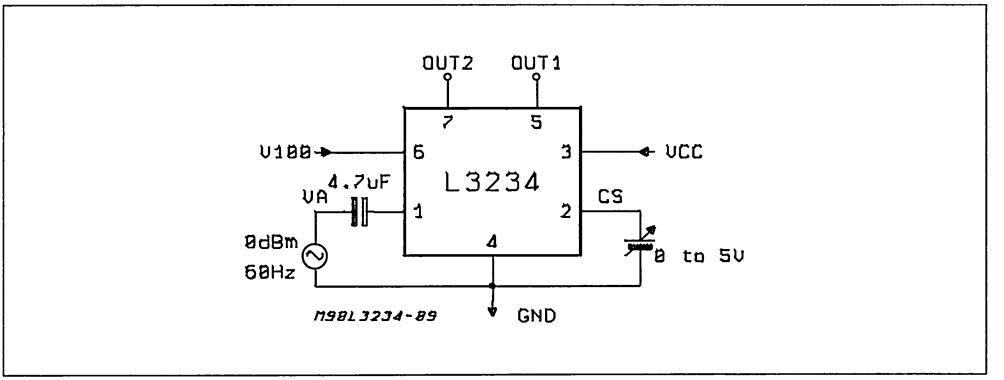


Figure 11.

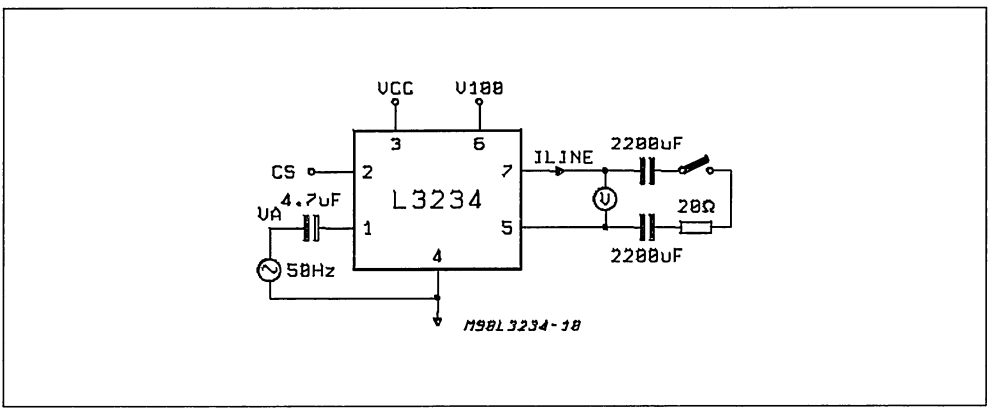
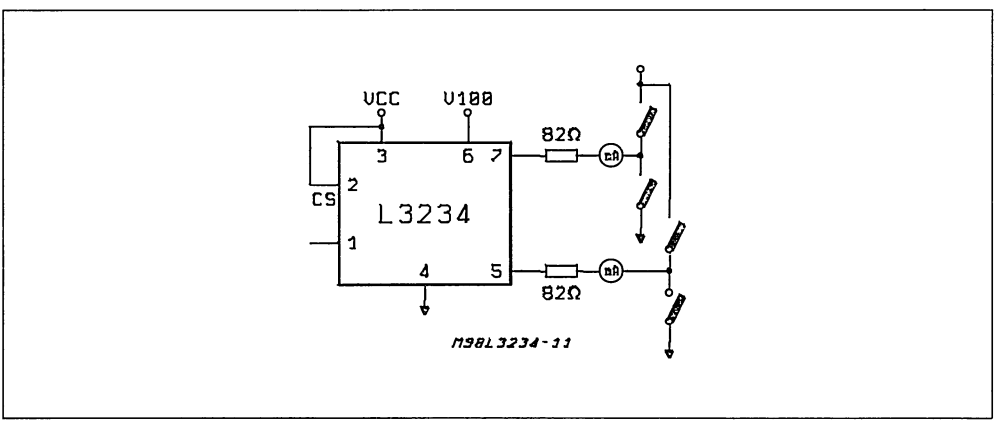


Figure 12.



L3235
Subscriber Line Interface Circuit

DESCRIPTION

Circuit description

The L3235 Subscriber Line Interface Circuit (SLIC) is a bipolar integrated circuit in 60V technology optimized for PABX application.

The L3235 supplies a line feed voltage with a current limitation which can be modified by an external resistor (RLIM).

The SLIC incorporates loop currents, ground key detection functions with an externally programmable constant time.

The two to four wires and four to two wires voice frequency signal conversion is performed by the L3235 and the line terminating and the balancing impedances are externally programmable.

The device integrates an automatic power limitation circuit. In short loop condition the extra power is dissipated on one external transistor (Text).

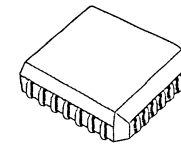
This aproach allows to assembly the L3235 in a low cost standard plastic PLCC28 package.

The chip is protected by thermal protection at Tj = 150°C.

The SLIC is able to give a power up command for Combo in off hook condition and an enable logic for solid state ringing injector L3234.

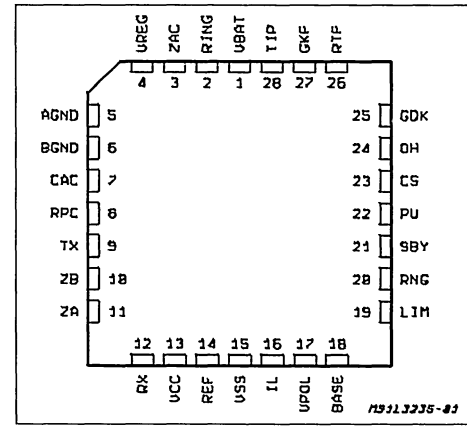
The L3235 package is 28 pin plastic PLCC.

The L3235 has been designed to operate togheter with L3234 performing complete BORSHT function without any electromechanical ringing relay (see the application circuit fig. 16).



PLCC28

PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{BAT}	Battery Voltage	-54	V
V_{CC}	Positive Supply Voltage	5.5	V
V_{SS}	Negative Supply Voltage	-5.5	V
T_j	Max. Junction Temperature	150	°C
T_{stg}	Storage Temperature	-55 to +150	°C

OPERATING RANGE

Symbol	Parameter	Min.	Max.	Unit
V_{BAT}	Battery Voltage	-52	-24	V
V_{CC}	Positive Supply Voltage	4.75	5.25	V
V_{SS}	Negative Supply Voltage	-5.25	-4.75	V
T_{op}	Operating Temperature for **L3235** **L3235T**	0 -40	70 85	°C °C
T_j	Max Junction Operating Temperature		130	°C

Note: Operating ranges define those limits between which the functionality of the device is guaranteed.

THERMAL DATA

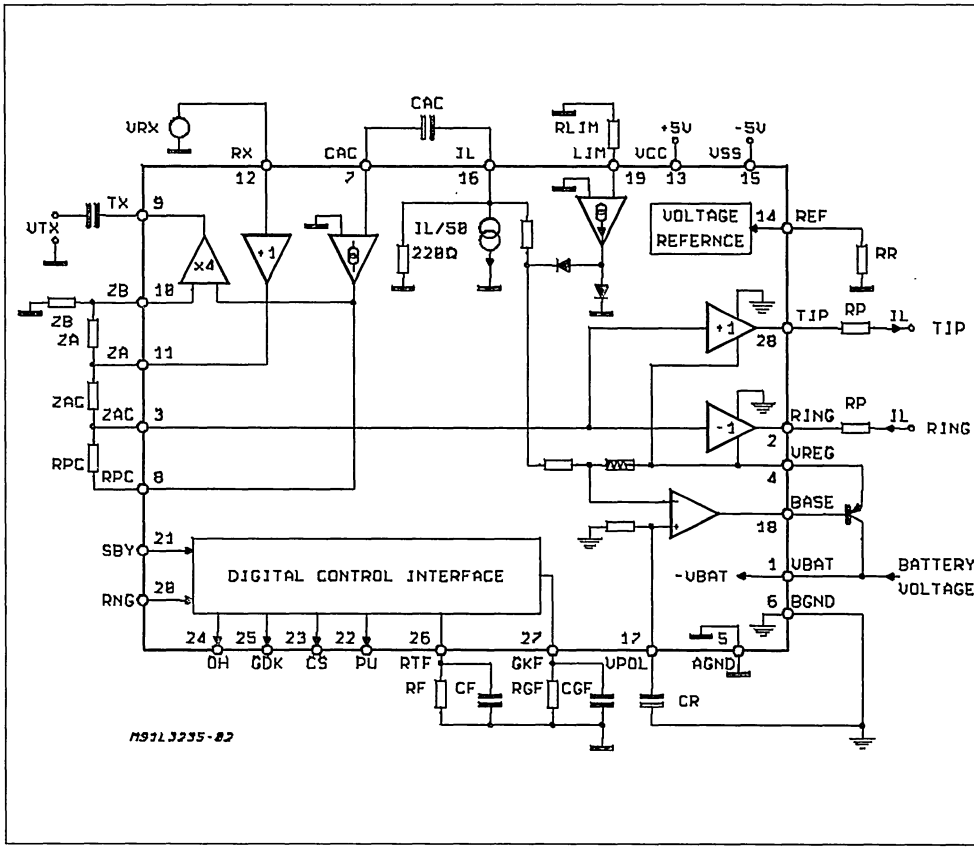
Symbol	Description		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

PIN DESCRIPTION

Pin	Name	Description
1	V_{bat}	Negative Battery Supply Input.
2	RING	RING wire of 2 Wire Line Interface.
3	ZAC	Non Inverting Input of the AC Impedance Synthesis Circuit.
4	VREG	Emitter Connection for the External Transistor.
5	AGND	Analog/Digital Ground.
6	BGND	Battery Ground. This is the Reference for the Battery Voltage (note 1).
7	CAC	AC Current Feedback Input.
8	RPC	External Protection Resistors AC Transmission Compensation.
9	TX	Four Wire Transmitting Amplifier Output.
10	ZB	Non Inverting Operational Input Inserted in the Hybrid Circuit for 2W to 4W Conversion. The Network Connected from this Pin to Ground shall be a copy of the Line Impedance.
11	ZA	VRX Output Buffer 2W to 4W Conversion.
12	RX	High Impedance Four Wire Receiving Input.
13	V_{CC}	Positive 5V Supply Voltage.
14	REF	Voltage Reference Output; a Resistor Connected to this pin sets the Internal Bias Current.
15	V_{SS}	Negative 5V Supply Voltage.
16	IL	Transversal Line Current Feedback Divided by 50.
17	VPOL	Non Inverting Operational Input to Implement DC Character.
18	BASE	Driver for External Transistor Base.
19	LIM	Voltage Reference Output; a Resistor Connected to this Pin Sets the Value of Line Current Limitation.
20	RNG	Ringing Logic Input from Line Card Controller.
21	SBY	Stand by Logic Input (SBY = 1 Set Line Current Limitation at 3mA).
22	PU	Power u.p Logic Output for the Codec Filter. (PU = 0 means Codec Filter Activated)
23	CS	Ring Injector Enable for L3234 Output. (CS = 1 means L3234 Ringing Injection Enable).
24	OH	Hook Status Logic Output (OH = 0 means off hook).
25	GDK	Ground Key Status Logic Output (GDK = 0 means Ground Key on).
26	RTF	Time Constant Hook Detector Filter Input.
27	GKF	Time Constant GK Detector Filter Input.
28	TIP	Tip Wire of 2 Wire Line Interface.

Note 1:
AGND and BGND pins must be tied together at a low impedance point (e.g at card connector level).

L3235 FUNCTIONAL DIAGRAM



FUNCTIONAL DESCRIPTION

DIGITAL INTERFACE

The different operating modes of the L3235 are programmed through a digital interface based on two input pins:

1)SBY input programs the stand-by or Active/Ringing modes.
2)RNG input programs the ringing ON/OFF activation condition for the L3234.

The L3235 digital interface has four output pins :

1)OH provides the on hook/off hook or ring trip informations (active low).
2)GDK provides the ground key on/off information (active low).
3)PU must be connected to the enable input pin of CODEC/FILTER devices like ETC 5054/57 and automatically activates this device when in active mode off-hook is detected or when ringing mode is selected.
4)CS output must be connected to the CS enable input of the solid state ringing injector L3234.

In this way the L3234 will be enabled when ringing mode is programmed and will be automatically disabled when the ring trip condition will be detected reducing the ringing signal disconnection time after ring trip.

The table 1 here below resumes the different operation modes and the relative logic output signals.

The two current detection (hook and GND key) have internal fixed threshold. Externally it is possible to program their time costant through two R-C components connected respectively to pin 26 (RTF) and pin 27 (GKF).

Table 1.

OPERATING MODE	INPUT PIN		LINE STATUS		OUTPUT PIN			
	SBY	RNG	0: ON HOOK 1: OFF HOOK	0: NO GND KEY 1: GND KEY ON	OH	GDK	PU	CS
ACTIVE	0	0	0	0	1	1	1	0
	0	0	0	1	0	0	0	0
	0	0	1	0	0	1	0	0
	0	0	1	1	0	0	0	0
RINGING	0	1	0	0	1	1	0	1
	0	1	0	1	0	0	0	0(*)
	0	1	1	0	0	1	0	0(*)
	0	1	1	1	0	0	0	0(*)
STAND-BY	1	0	X	X	1	1	1	0
	1	1	X	X	1	1	0	1

(*)This status is latched and doesn't change until RNG turn to 0

OPERATING MODES

Stand-By (SBY = 1 and RNG = 0)

In Stand-By mode the L3235 limits the DC Loop current to 3 mA.

In this mode all the AC circuits are active and all the AC characteristics are the same as in Active Mode.

Also the two Line Current detectors (hook and GND key) are active but due to the loop current limited to 3 mA they will not be activated.

This mode is useful in emergency condition when it is very important to limits the system power dissipation.

Ringing Mode (SBY = 0 and RNG = 1)

When ringing mode is selected "CS" pin is set to 1 in order to activate the L3234 ringing injector.

See L3234 for detailed description.

Ring trip is detected by means of the same internal circuitry used for off-hook detection.

An off-hook delay time lower than ½ F_{RING} should be selected. (see ext. components list).

When ring trip is detected "CS" is automatically set to "0" allowing in this way a quick ringing disconnection.

After Ring trip detection the Card Controller must set the L3235 in active mode to remove the internal latching of the "CS" information.

Active mode (SBY = 0 and CS1 = 0)

In Active mode the L3235 has the DC characteristic show in Fig.13

The DC characteristics of L3235 has two different feeding conditions:

1)Current Limiting Region : (short loop) the DC impedance of the SLIC is very high (>20 Kohm) therefore the system works as a current generator. By the ext. resistor RLIM connected at pin 19 it is possible to program limiting current values from 20 mA to 70 mA.

2) Voltage source region (long loop).
The DC impedance of the L3235 is almost equal to zero therefore the system works like a voltage generator with in series the two external protection resistors Rp.

When a limiting current value higher than 40 mA is programmed the device will automatically reduce to 40 mA the loop current for very short loop.

This is done in order to limit the maximum power dissipation in very short loop to values lower than 2W for the external transistor and lower than 0.5W for the L3235 itself.

This improve the system reliability reducing the L3235 power dissipation and therefore the internal junction temperature.

Figure 13: DC characteristic in Active Mode with two different values of limiting current (30mA and 70 mA).

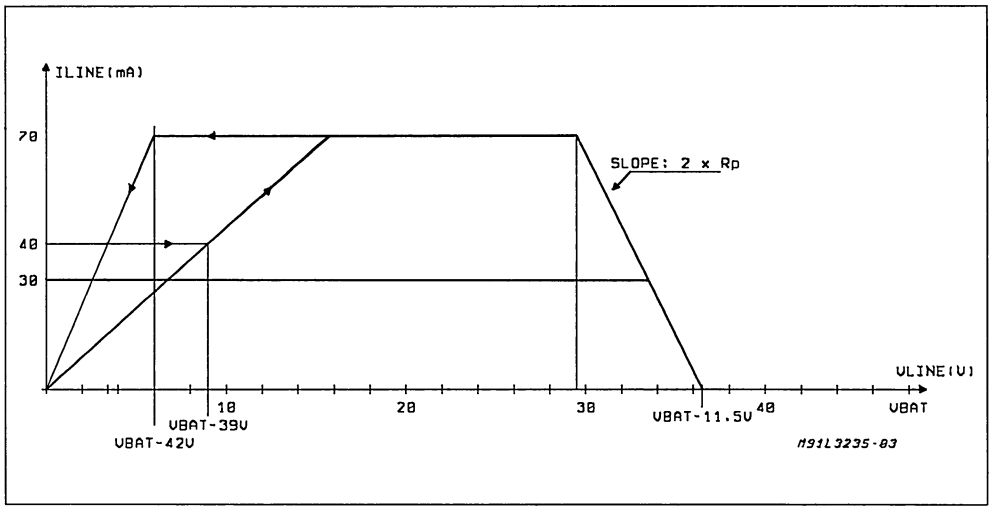
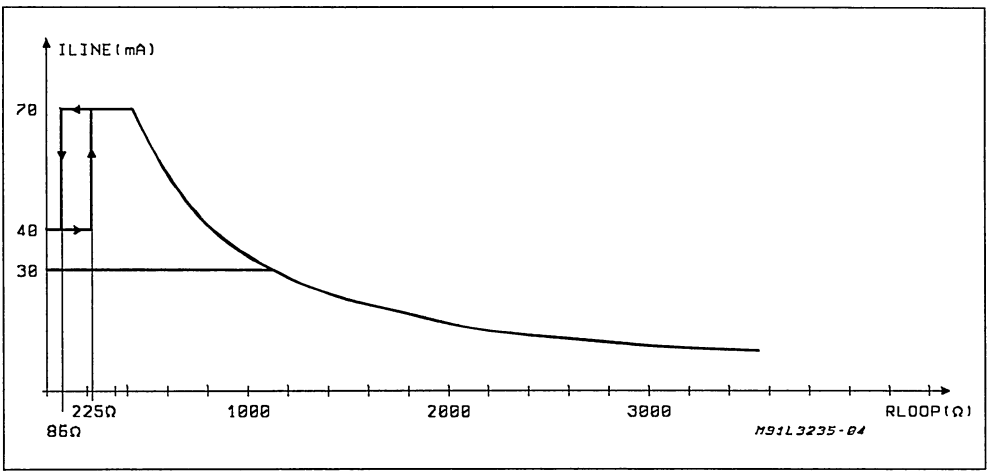


Figure 14: Line current versus loop resistance with two different values of limiting current (30mA and 70mA)



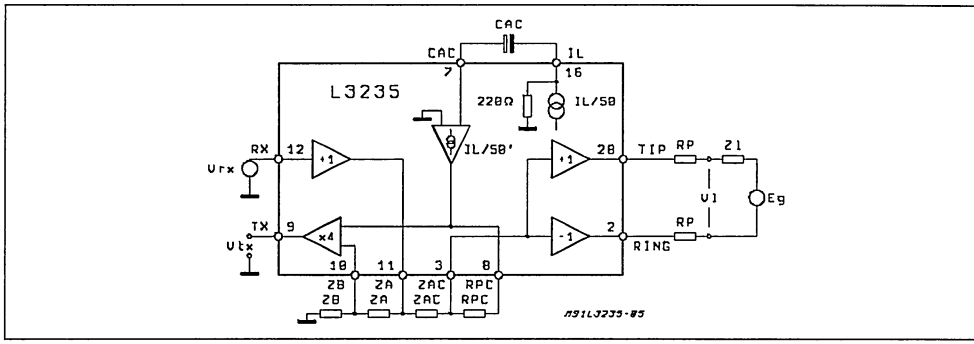
AC characteristic

A simplified AC model of the transmission circuits is shown in figure 15.

Where :

- V_{rx} is the received signal
- V_{tx} is the transmitted signal
- V_l is the AC transversal voltage at line terminations.
- E_g is the line open circuit AC voltage
- Z_l is the line impedance
- R_p are the protection resistors
- Z_B is the line impedance balancing network
- Z_A is the SLIC impedance balancing network
- Z_{AC} program the AC line termination impedance
- R_{PC} used for external protection resistors insertion loss compensation
- $I_l/50$ is the AC transversal current divided by 50
- CAC AC feedback current decoupling

Figure 15: Simplified AC Circuits



Two wire impedance

To calculate the impedance presented to the two wire line by the SLIC including the protection resistors R_p and defined as Z_S let:

$V_{rx} = 0$

II/50' = II/50 (in first approximation)

Rp = 50Ω

$Z_S = Z_{AC}/25 + 2R_P$

Z_{AC} to make $Z_S = 600\Omega$

$Z_{AC} = 25 \bullet (Z_S - 2R_P)$

$Z_{AC} = 25 \cdot (600 - 100)$

$Z_{AC} = 12.5K\Omega$

Two wire to four wire gain (Tx gain)

Let $V_{rx} = 0$

$$G_{tx} = \frac{V_{tx}}{V_I}$$

$$\frac{V_{tx}}{V_I} = 2 \cdot \frac{Z_{AC} + R_{PC}}{Z_{AC} + 50R_P}$$

Example: Calculate Gtx making $R_{PC} = 50 \cdot R_P$

$$G_{tx} = 2 \cdot \frac{Z_{AC} + 50 \cdot R_P}{Z_{AC} + 50 \cdot R_P} = 2$$

As you can see the RPC resistor is providing the compensation of the insertion loss introduced by the two external protection resistors R_P.

Four wire to two wire gain (Rx gain)

Let Eg = 0

$$G_{rx} = \frac{V_I}{V_{rx}} = \frac{50 \cdot Z_I}{25 \cdot (Z_I + 2R_P) + Z_{AC}}$$

Example:
Calculate G_{rx} making $Z_{AC} = 25 \cdot (Z_{ML} - 2 \cdot R_P)$

$$G_{rx} = \frac{50 \cdot Z_I}{25 \cdot (Z_I + 2R_P - 2R_P + Z_{ML})}$$

$$G_{rx} = \frac{2 \cdot Z_I}{Z_I + Z_{ML}}$$

In particular for $Z_S = Z_I$: $G_{rx} = 1$

Hybrid function

To calculated the transhybrid loss (Thl) let: Eg = 0
Thl =

$$= \frac{VT_x}{VR_x} = 4 \left(\frac{Z_B}{Z_B} + Z_A - \frac{50 \cdot (2 \cdot R_P + Z_I) - 2R_{PC}}{50 \cdot (2 \cdot R_P + Z_I) - 2R_{AC}} \right)$$

Example:
Calculating Thl making $R_S = 50 \cdot R_P$, $Z_S = 25 \cdot (ZSlic - 2 \cdot R_P)$

$$Thl = 4 \cdot \left(\frac{Z_B}{Z_B + Z_A} - \frac{Z_I}{Z_I + Z_{ML}} \right)$$

In particular if $\frac{Z_A}{Z_B} = \frac{Z_S}{Z_I}$

Thl = 0

From the above relation it is evident that if Z_S is equal to the Z_I used in Thl test, the two Z_A, Z_B impedances can be two resistor of the same value.

AC transmission circuit stability

To ensure stability of the feedback loop shown in block diagram form in figure 15 two capacitors are required. Figure 16 includes these capacitors Cc and Ch.

AC - DC separation

The high pass filter capacitor C_{AC} provides the separation between DC circuits and AC circuits. A CAC value of 100mF will position the low end frequency response 3dB break point at 7Hz,

$$fsp = \frac{1}{2\pi \cdot 220\Omega \cdot C_{AC}}$$

External components list for L3235

To set the SLIC into operation the following parameters have to be defined:
- The AC SLIC impedance at line terminals "Zs" to which the return loss measurements is referred. It can be real (typ. 600Ω) or complex.
- The equivalent AC impedance of the line "Zl" used for evaluation of the trans-hybrid loss performance (2/4 wire conversion). It is usually a complex impedance.
- The value of the two protection resistors Rp in series with the line termination.

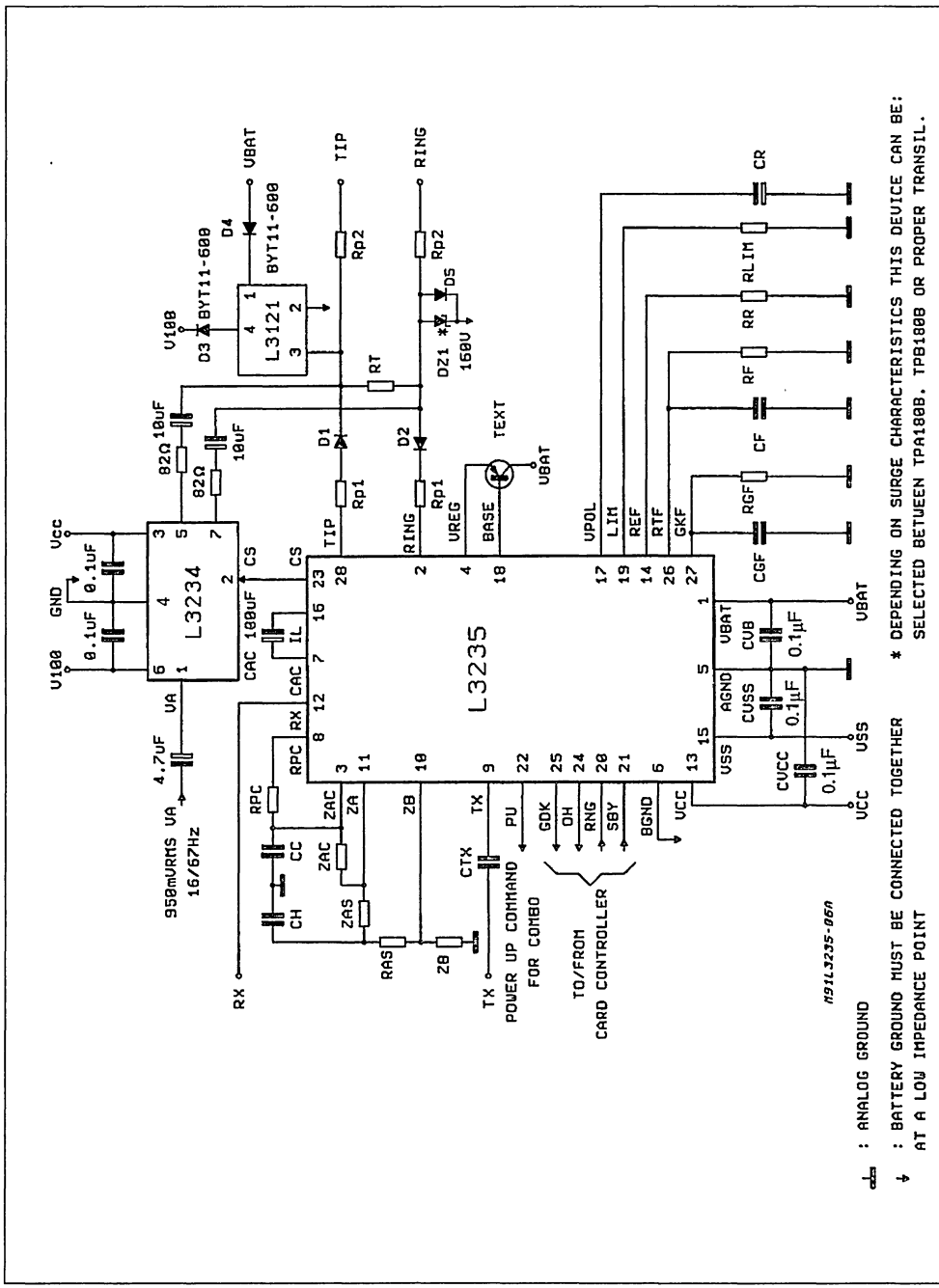
Once, the above parameters are defined, it is possible to calculate all the external components using the following table. The typical values has been obtained supposing: Zs = 600Ω; Zl = 600Ω; Rp = 50Ω

Name	Suggested Value	Function	Formula
R_F C_F	39KΩ 390nF	Delay Time On-hook Off-hook	$\tau = 0.69 \cdot C_F \cdot 39K\Omega$ (1)
R_{GF} C_{GF}	39KΩ 390nF	Delay Time GK Detector	$\tau = 0.69 \cdot C_{GF} \cdot 39K\Omega$
R_R	51KΩ	Bias Set	
R_{LIM}	8.4KΩ to 33KΩ	Ext. Current Limit. Progr.	$R_{LIM} = \frac{564}{I_{LIM} - 3mA}$
CR	4.7µF 6.3 V 30%	Negative Battery Filter	$C_{AC} = \frac{1}{2\pi \cdot 16K\Omega \cdot fp}$
R_P	50	Protection Resistors	$47 \leq R_P \leq 100\Omega$ (2)
R_T	1MΩ 20%	Termination Resistor	
C_{AC}	100µF 6.3V 20%	DC/AC current feedback splitting	$C_{AC} = \frac{1}{2\pi \cdot 220\Omega \cdot f_{sp}}$
R_{PC}	2500Ω 1%	R_P insertion loss compensation	$R_{PC} = 25 \cdot (2R_P)$
Z_{AC}	12500Ω 1%	2W AC Impedance programmation	$Z_{AC} = 25 \cdot (Z_S - 2R_P)$
C_C	220pF 20%	AC Feedback compensation	f1 = 300KHz $C_C = \frac{1}{2\pi f1 \cdot 50R_P}$
Z_{AS}	12500Ω 1%	Slic Impedance Balancing Net.	$Z_{AS} = 25 \ (Z_S - 2R_P)$
R_{AS}	2500Ω 1%		$RAS = 25 \cdot (2R_P)$
ZB	15KΩ 1%	Line impedance Balancing Net.	$Z_B = 25 \cdot Zl$
C_H	220pF 20%	C_C Transybrid loss Compensation	$C_H = C_C \cdot \frac{Z_{AC}}{Z_{AS}}$
C_{TX}	4.7µF 30%	DC Decoupling Tx Output	$C_{TX} = \frac{1}{6.28 \cdot fp \cdot Z_{load}}$
D1, D2	1N4007	Line Rectifier	
Text	(3)	External Transistor	$P_{Diss} \geq 2W$, $V_{CEO} \geq 60V$ $H_{FE} \geq 40$, $I_C \geq 100mA$ $V_{BE} < 0.8V$ @ 100mA
CV_{SS}; CV_{DD}	100nF	±5V supply filter	
C_{VB}	100nF/100V	V_{BAT} supply filter	

Notes:

1) For proper operation Cf should be selected in order to verify the following conditions.
   A) cf > 150nF
   B) $\tau < 1/2 \bullet f_{RING}$
   f_{RING}: Ringing signal frequency
2) For protection purposes the RP resistor is usually splitted in two part R_{P1} and R_{P2}, with $R_{P1} \geq 30\Omega$.
3) ex: BD140; MJE172, MJE350.... (SOT32 or SOT82 package available also for surface mount). For low power application (reduced battery voltage) BCP53 (SOT223 surface mount package) can be used Depending on application enviroment an heatsink could be necessary.

Figure 16: Typical Appication Circuit Including L3234 and Protection



ELECTRICAL CHARACTERISTICS (Test condition: refer to the test circuit of the fig. 17; V_{CC} = 5V, V_{SS} = -5V, V_{bat} = -48V, T_{amb} = 25°C, unless otherwise specified)

Note: Testing of all parameters is performed at 25°C. Characterization, as well as the design rules used allow correlation of tested performance with actual performance at other temperatures. All parameters listed here are met in the range 0°C to +70°C. For applications requiring operations in the standard temperature range (0°C to 70°C) use L3234. If operations are required in the extended temperature range (-40°C to 85°C), use the L3234T.

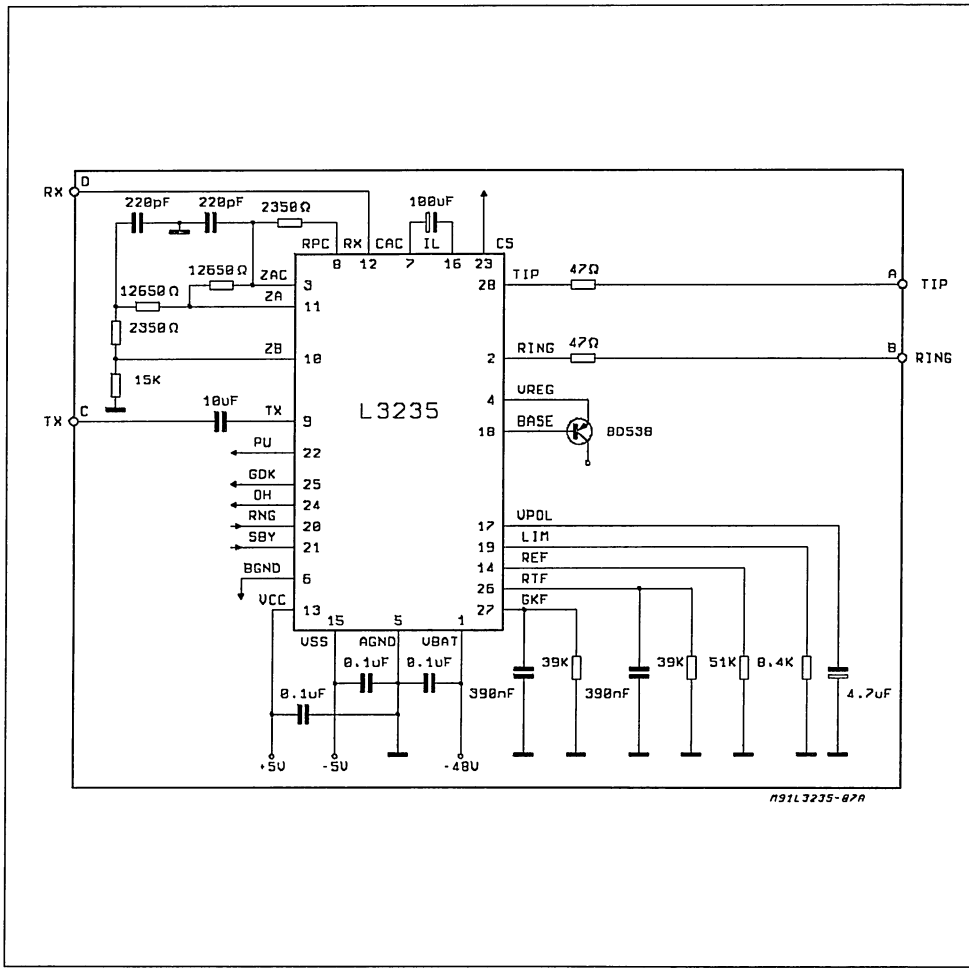
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
STAND-BY							
V_{ls}	Output Voltage at TIP/RING pins	I_{LINE} = 0	35.7		39	V	
I_{LCC}	Short Circuit Current	Stand-by, SBY = 1	2	3	4	mA	
DC OPERATION							
V_{IP}	Output Voltage at TIP/RING pins	I_{LINE} = 0 I_{LINE} = 50mA	35.7 35.2		39 39	V V	
I_{lim}	Current Progr.	I_{lim} Prog. = 70mA	63	70	77	mA	
I_{lim}	Current Progr.	8.4KΩ < R_{LIM} < 33KΩ	20		70	mA	
I_O	On-hook Threshold				5		
I_f	Off-hook Threshold		10				
I_{lgk}	GK Detector Threshold		10		17		
Gklim	Ground Key Current Limitation	RING to BGND	13		22	mA	
Gkov	Ground Key Threshold Overloap	Gklim-Ilgk	1			mA	
I_{max}	Max. Output Current at TIP/RING	I_{lim} = 70mA	90		140	mA	
IV_{CC}	Supply Current from V_{CC}	I_{line} = 0		6.2	8	mA	
IV_{SS}	Supply Current from V_{SS}	Iline = 0		1.6	2.1	mA	
IV_{bat}	Supply Current from V_{bat}	Iline = 0		2.8	3.6	mA	
AC OPERATION							
Z_{tx}	Sending Output Impedance	pin 9 (Tx)			10	Ω	
Z_{rx}	Receiving Input Impedance	pin 12 (Rx)	1			MΩ	
R_l	2W Return Loss	f = 300 to 3400Hz	20	36		dB	A1
Thl	Trans Hybrid Loos	f = 300 to 3400Hz	20	36		dB	A2
G_s	Sending Gain	f = 1020Hz I_l = 20mA	5.82	6.02	6.22	dB	A3
G_{sf}	Flatness	f = 300 to 3400Hz	-0.2		0.2	dB	
G_{sl}	Linearity	-20dB to 10dBm	-0.2		0.2	dB	
G_r	Receiving Gain	f = 1020Hz I_l = 20mA	0.2	0	0.2	dB	A4
G_{rf}	Flatness	f = 300 to 3400Hz	-0.2		0.2	dB	
G_{rl}	Linearity	-20dBm to +4dBm	-0.2		0.2	dB	
Np4W	Psoph. Noise at Tx			-69	-62	dBmp	
Np2W	Psoph. Noise at Line			-75	-68	dBmp	
S_{vrr}	Relative to V_{bat} versus Line Terminal versus Tx Terminal	f = 1020Hz V_S = 100mVpp			-30 -24	dB dB	A5
S_{vrr}	Relative to V_{cc} and V_{ss} versus Line Terminal versus Tx Terminal	f = 1020Hz V_S = 100mVpp			-20 -14	dB dB	
L_{tc}	L/T Conversion measured at line Terminals	f = 300 to 3400 I_{line} = 20mA	49 53(*)			dB dB	A6
T_{lc}	T/L Conversion Measured at Line Terminals	f = 300 to 3400 I_{line} = 20mA	46(*)			dB	A7

(*) Selected parts L3235C

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
DIGITAL STATIC INTERFACE							
V_{il}	Input Voltage at Logical "0"	Input SBY, CS1	0		0.8	V	
V_{ih}	Input Voltage at Logical "1"	Input SBY, CS1	2		5	V	
I_{il}	Input Current at Logical "0"	Input SBY, CS1			10	µA	
I_{ih}	Input Current at Logical "1"	Input SBY, CS1			10	µA	
V_{ol}	Output Voltage at Logical "0"	I_{out} = 1mA I_{out} = 10µA			0.5 0.4	V V	
V_{oh}	Output Voltage at Logical "1"	I_{out} = 10µA I_{out} = 1mA	4 2.7			V V	

Figure 17: Test Circuit



APPENDIX A

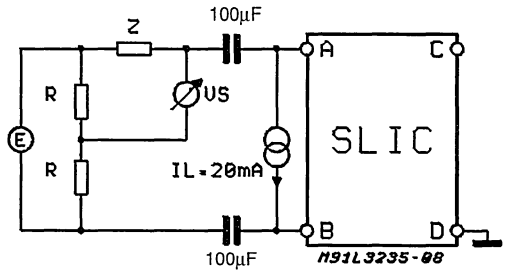
L3235 TEST CIRCUITS

Referring to the test circuit reported in fig 17 you can find the proper configuration for the main measurements.

In particular:

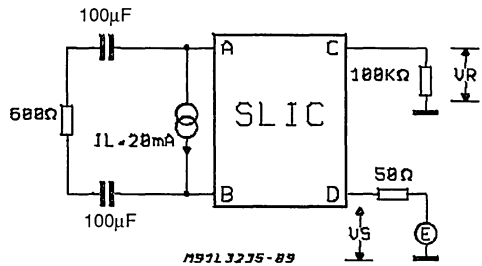
A-B: Line terminals
C: Tx sending output on 4W side
D: Rx receiving input on 4W Side

Figure A1: 2W Return Loss



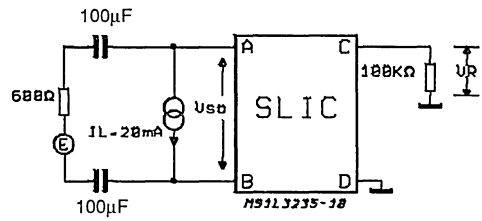
$$R_L = 20 \log \frac{|Z_{ML} - Z|}{|Z_{ML} + Z|} = 20 \log \frac{|2V_S|}{|E|}$$

Figure A2: Trans-hybrid Loss



$$T_{HL} = 20 \log \frac{V_S}{V_R}$$

Figure A3: Sending Gain



TEST CIRCUITS (continued)
Figure A4: Receiving Gain

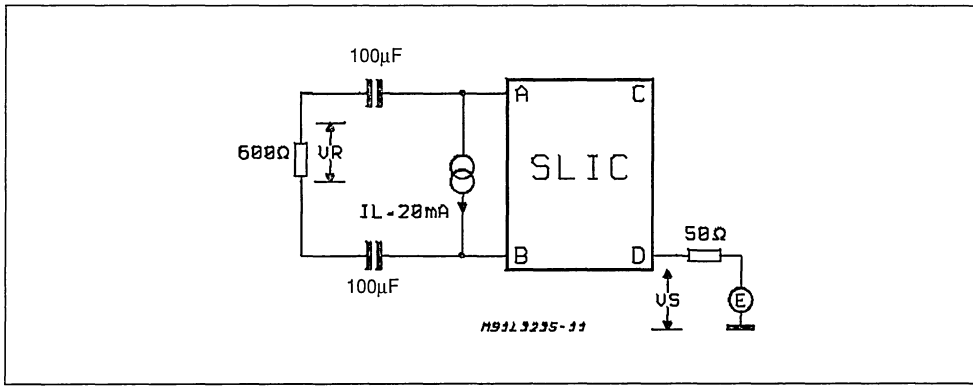


Figure A5: SVRR Relative to Battery Voltage VB

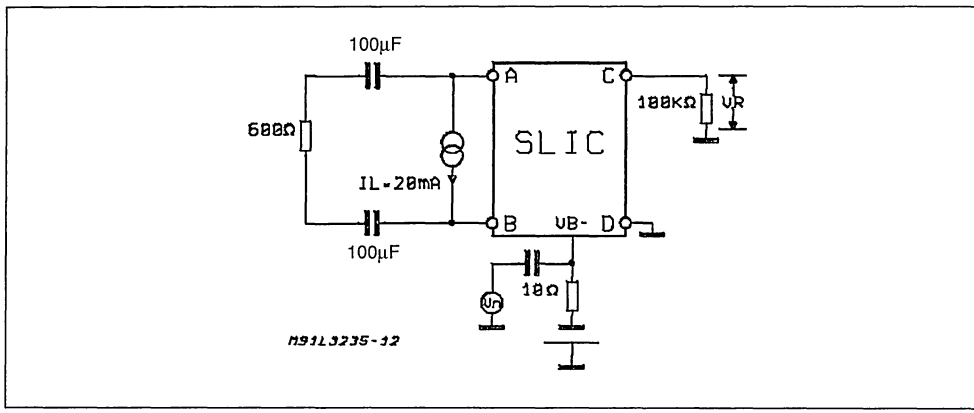
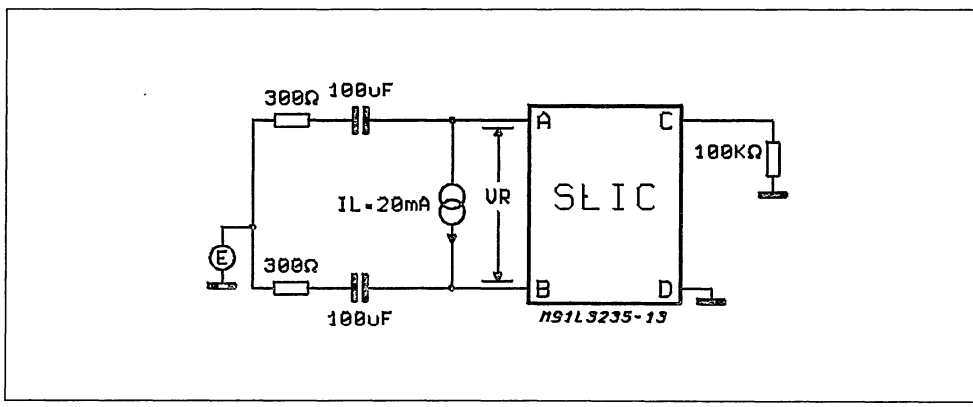


Figure A6: Longitudinal to Transversal Conversion



APPENDIX B

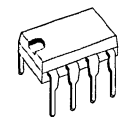
LAYOUT SUGGESTIONS

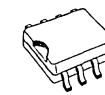
Standard layout rules should be followed in order to get the best system performances:

1) Use always 100nF filtering capacitor close to the supply pins of each IC.
2) The L3235 bias resistor (RR) should be connected close to the corresponding pins of L3235 (REF and AGND).

TRUNK INTERFACE

- ON CHIP POLARITY GUARD
- MEETS DC LINE CHARACTERISTICS OF EITHER CCITT AND EIA RS 464 SPECS
- PULSE FUNCTION
- HIGH AC IMPEDANCE
- OFF HOOK-STATUS DETECTION OUTPUT
- LOW EXTERNAL COMPONENT COUNT





Minidip **SO8**

ORDERING NUMBERS:

L3845B L3845D

DESCRIPTION

The circuit provides DC loop termination for analog trunk lines.

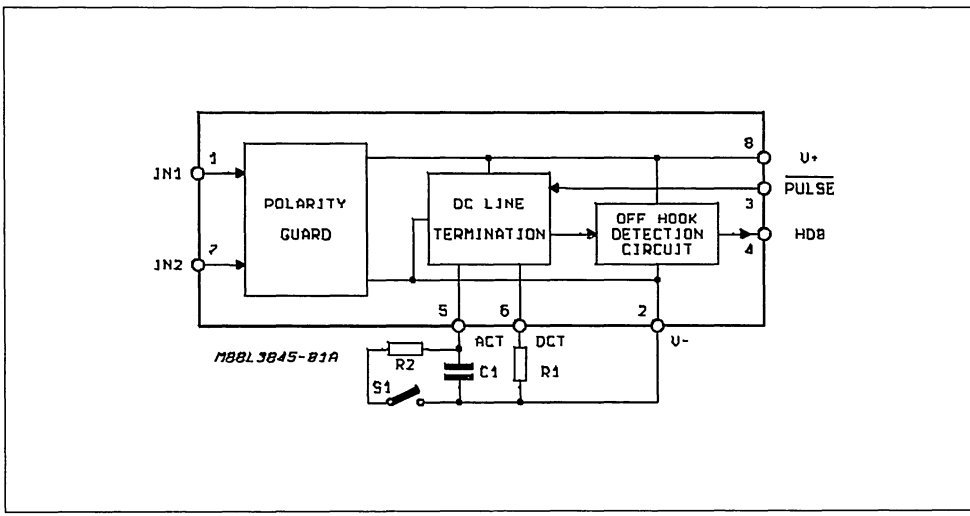
The V-I characteristics is equivalent to a fixed voltage drop (zener like characteristic) in series with an external resistance that determines the slope of the DC characteristic.

An external low voltage electrolytic capacitor causes the circuit to exhibit a very high impedance to all AC signal above a minimum frequency that is determined by the capacitor itself and by a 20 K nominal resistor integrated on the chip.

The Off-Hook status is detected all the time a typic of 8 mA is flowing into the circuit. In this condition a constant current generator is activated to supply an external device (typically an optocoupler) without affecting the AC characteristic of the circuit.

When Pulse Dialing is required the $\overline{\text{PULSE}}$ input (pin 3) connected to V- causes the device to reduce the fixed DC voltage drop and to exhibit a pure resistive impedance equal to the external resistor.

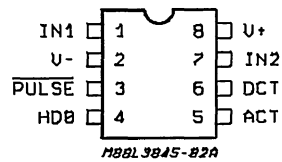
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_L	Max Line Voltage (pulse duration 10 ms max)	20	V
I_L	Max Line Current	150	mA
P_{tot}	Total Power Dissipation at Tamb = 70 °C	800	mW
T_{op}	Operating Temperature	– 40 to + 70	°C
T_{srg}, T_j	Storage and Junction Temperature	– 55 to + 150	°C

PIN CONNECTION (Top view)



THERMAL DATA

Symbol	Parameter		Minidip	SO8	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient (*)	Max.	80	140 to 180	°C/W

(*) Mounted on FR4 Boards

DC ELECTRICAL CHARACTERISTICS (I_L = 10 mA to 100 mA, R_1 = 56 Ω, S_1 = Open, T_{amb} = + 25 °C, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_L	Line Voltage (normal mode)	PULSE = Open IL = 10 mA I_L = 20 mA I_L = 100 mA			 5 6 12	 V V V
V_{LP}	Line Voltage (pulse mode)	PULSE = V^- I_L = 20 mA I_L = 35 mA I_L = 80 mA			 4 5.5 9.5	 V V V
I_{hn}	ON/OFF-Hook Line Current Detection Threshold		6.5		9.5	mA
I_{hf}	OFF/ON-Hook Line Current Detection Threshold		5		9.2	mA
I_{OUT}	OFF-Hook Output Drive Current at Pin HDO	IL = 10 mA $I_L \geq$ 20 mA	1.5 2			mA mA
V_{PM}	Pulse Input Low Voltage				0.8	V
I_{PM}	Pull-up Input Current at Pin PULSE (pulse mode)	IL = 100 mA Pulse = V^-			20	µA
I_{NM}	Imput Current at Pin Pulse (normal mode)				3	µA

AC ELECTRICAL CHARACTERISTICS (I_L = 10 mA to 100 mA, R_1 = 56 Ω, R_2 = 470 KΩ, S_1 = Open, T_{amb} = + 25 °C, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Z_L	AC Line Impedance	C_1 = 2.2mF f = 1KHz		 20		 KΩ
	Sending/Receiving Distortion	f = 1KHz V_S = 775mVrms I_L = 15 to 100mA			 2	 %
	Sending/Receiving Distortion	S_1 = Closed; V_S = 1.3Vrms		 2		 %

APPLICATION INFORMATION

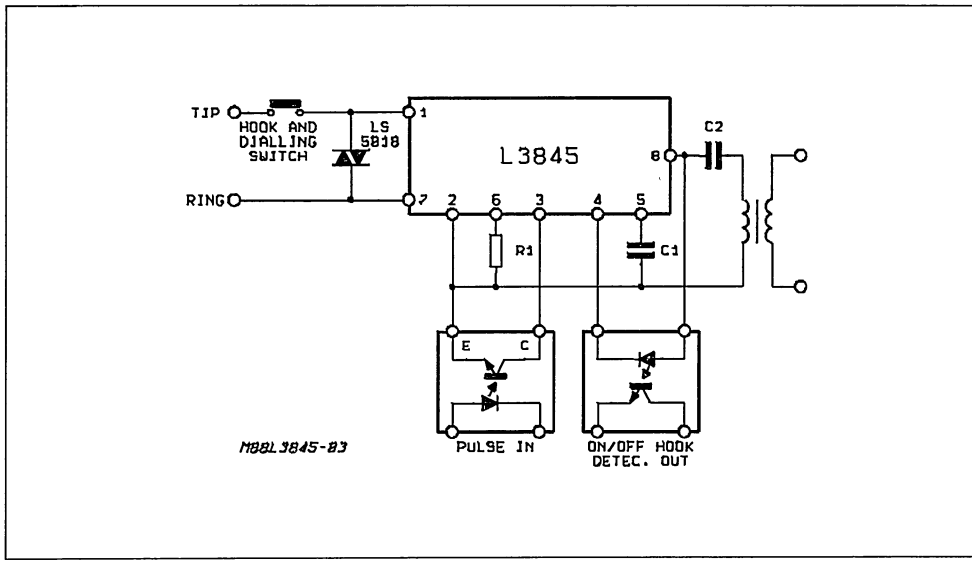
With the use of this circuit it is possible to terminate an analog trunk so that all the DC current component is flowing in the TRUNK TERMINATION CIRCUIT while the AC component is decoupled with a low voltage capacitor and can be used with a small and low cost audio coupler transformer to provide the AC balancing termination and two to four wire conversion.

Therefore it is usefull both for MODEM and PABX systems.

Figure 1 gives the typical application circuit ; it is worth to note that the TRUNK TERMINATION CIRCUIT, together with the LS5018 transient suppressor provides a compact and low cost module fully protected against lightning or overvoltages frequently present on telephone lines.

The $\overline{\text{PULSE}}$ input when connected to V- allows the device to reduce the Line Voltage and to show a resistive impedance equal to R1 to the line. When $\overline{\text{PULSE}}$ input is left open, this function is disable.

Figure 1: Typical Application.



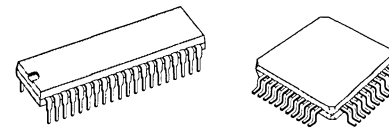
SGS-THOMSON MICROELECTRONICS

M3488

256 x 256 DIGITAL SWITCHING MATRIX

PRELIMINARY DATA

- 256 INPUT AND 256 OUTPUT CHANNEL CMOS DIGITAL SWITCHING MATRIX COMPATIBLE WITH M088
- BUILDING BLOCK DESIGNED FOR LARGE CAPACITY ELECTRONIC EXCHANGES, SUBSYSTEMS AND PABX
- NO EXTRA PIN NEEDED FOR NOT-BLOCKING SINGLE STAGE AND HIGHER CAPACITY SYNTHESIS BLOCKS (512 or 1024 channels)
- EUROPEAN TELEPHONE STANDARD COMPATIBLE (32 serial channels per frame)
- PCM INPUTS AND OUTPUTS MUTUALLY COMPATIBLE
- ACTUAL INPUT-OUTPUT CHANNEL CONNECTIONS STORED AND MODIFIED VIA AN ON CHIP 8-BIT PARALLEL MICROPROCESSOR INTERFACE
- TYPICAL BIT RATE : 2Mbit/s
- TYPICAL SYNCHRONIZATION RATE : 8KHz (time frame is 125µs)
- 5V POWER SUPPLY
- CMOS & TTL INPUT/OUTPUT LEVELS COMPATIBLE
- HIGH DENSITY ADVANCED 1.2µm HCMOS3 PROCESS



DIP40 **PQFP44**

ORDERING NUMBERS:

M3488B1 M3488Q1

Main instructions controlled by the microprocessor interface

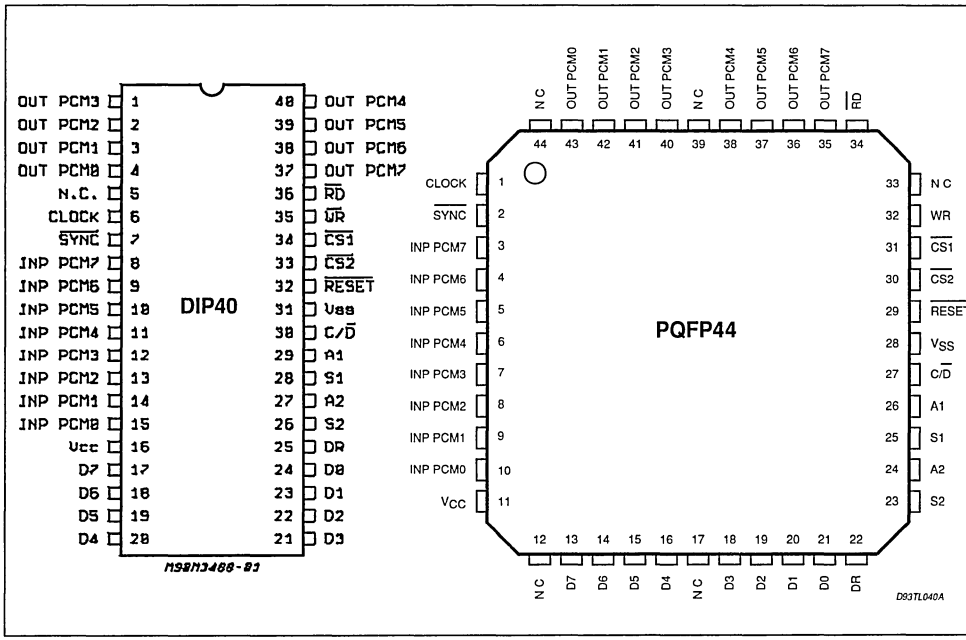
- CHANNEL CONNECTION/DISCONNECTION
- OUTPUT CHANNEL DISCONNECTION
- INSERTION OF A BYTE ON A PCM OUTPUT CHANNEL/DISCONNECTION
- TRANSFER TO THE MICROPROCESSOR OF A SINGLE PCM OUTPUT CHANNEL SAMPLE
- TRANSFER TO THE MICROPROCESSOR OF A SINGLE OUTPUT CHANNEL CONTROL WORD
- TRANSFER TO THE MICROPROCESSOR OF A SELECTED 0 CHANNEL PCM INPUT DATA

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_{CC}	Supply Voltage	-0.3 to 7	V
V_I	Input Voltage	-0.3 to V_{CC}+0.3	V
V_O	Off State Output Voltage	-0.3 to V_{CC}+0.3	V
I_O	Current at Digital Outputs	30	mA
P_{tot}	Total Package Power Dissipation	1.5	W
T_{stg}	Storage Temperature Range	-65 to 150	°C
T_{op}	Operating Temperature Range	0 to 70	°C

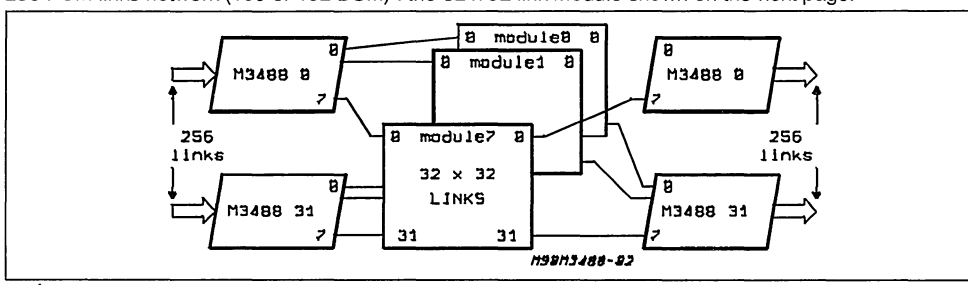
Stresses above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operating conditions of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONNECTIONS (Top views)

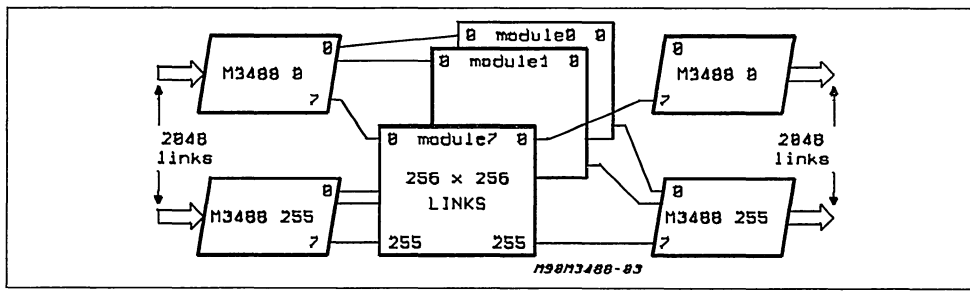


EXCHANGE NETWORKS APPLICATIONS

256 PCM links network (160 or 192 DSM) : the 32 x 32 link module shown on the next page.

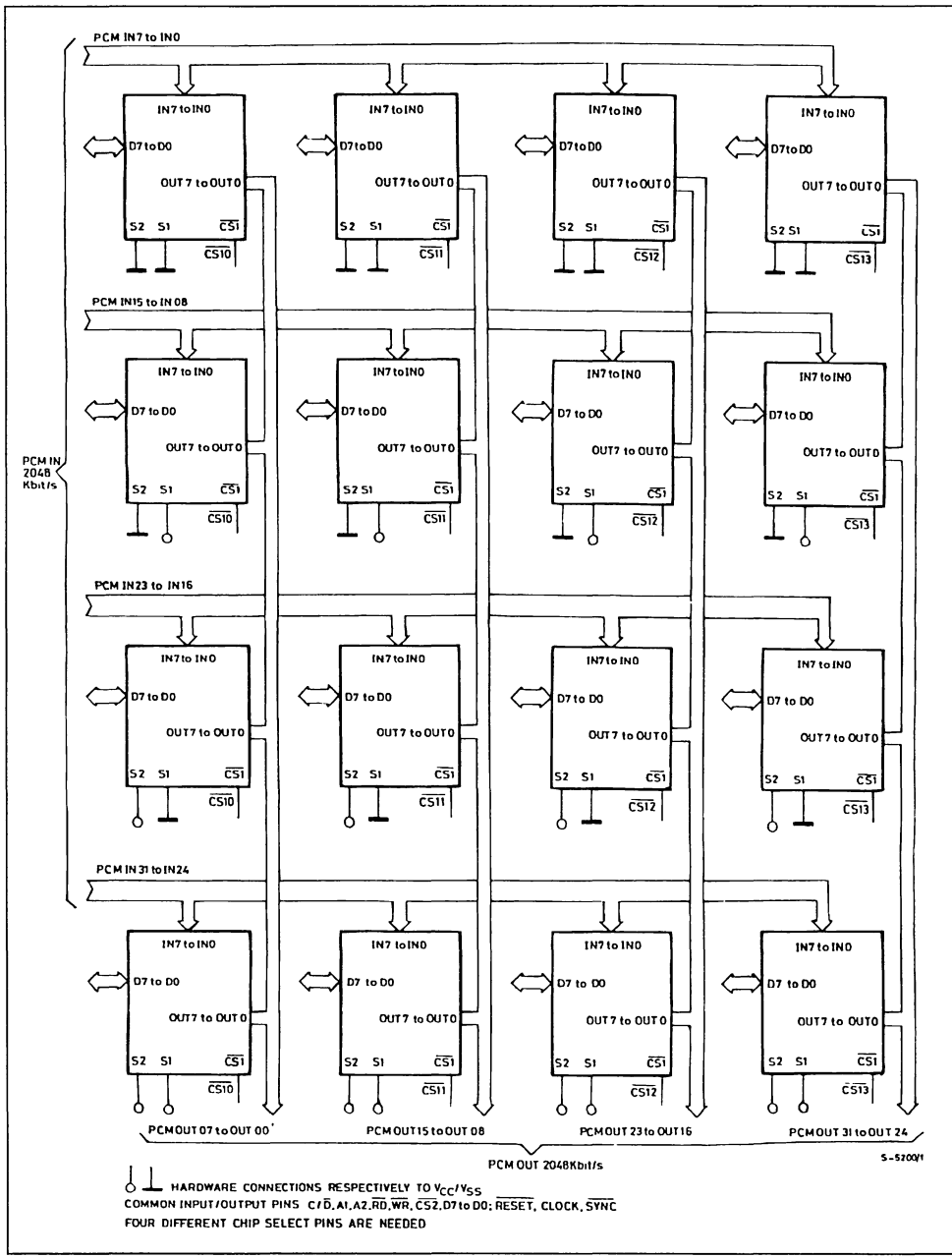


2048 PCM links network (1792 or 2048 DSM) : the 256 x 256 link network is shown above.

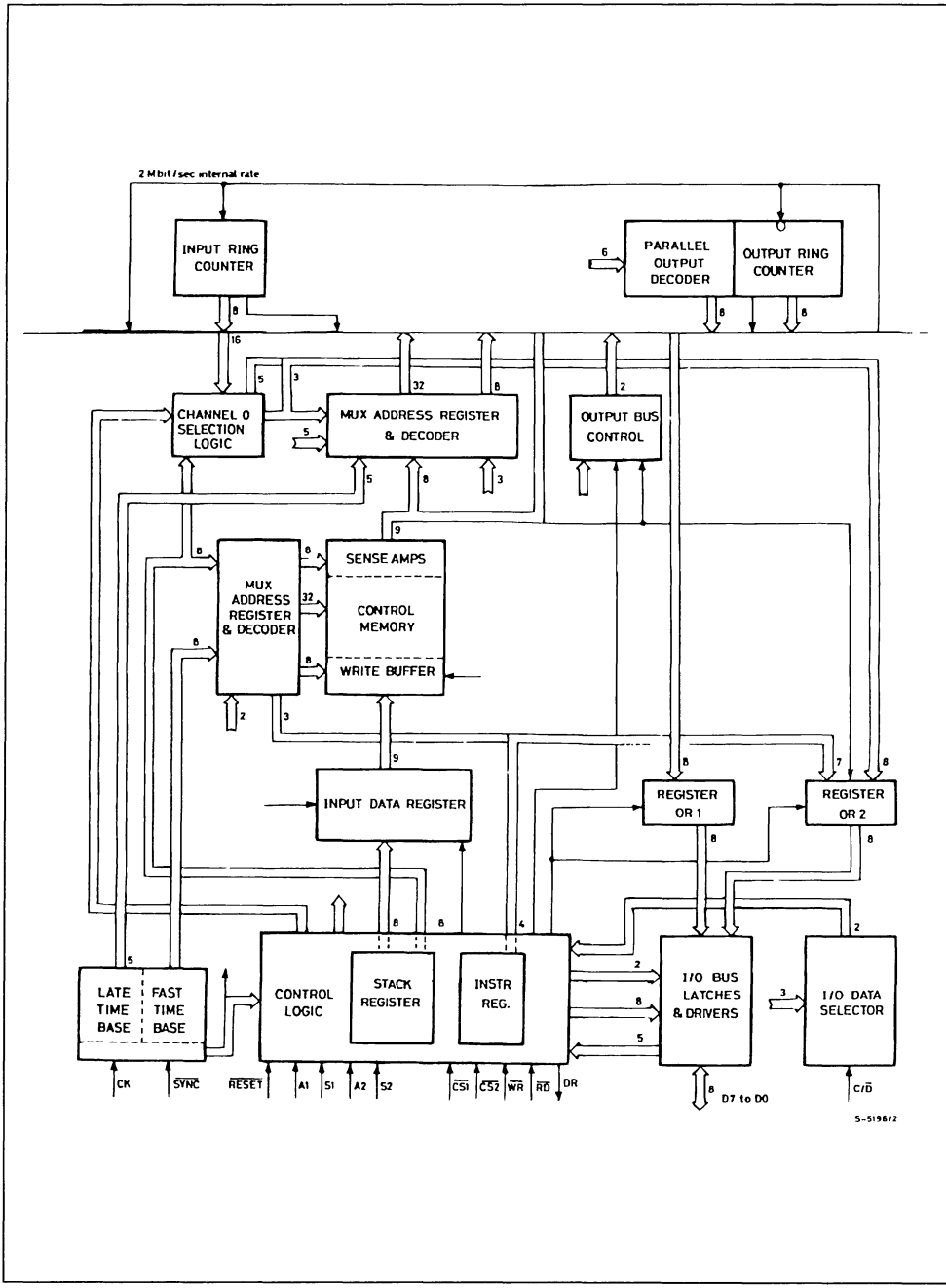


EXCHANGE NETWORKS APPLICATIONS (continued)

Single Stage/Sixteen Devices Configuration (32 by 32 links or 1024 channels).



BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.75 to 5.25	V
V_I	Input Voltage	0 to 5.25	V
V_O	Off State Input Voltage	0 to 5.25	V
CLOCK Freq.	Input Clock Frequency	4.096	MHz
SYNC Freq.	Input Synchronization Frequency	8	KHz
T_{op}	Operating Temperature	0 to 70	°C

CAPACITANCES (measurement freq. = 1MHz; T_{op} = 0 to 70°C; unused pins tied to V_{SS})

Symbol	Parameter	Pins (*)	Min.	Typ.	Max.	Unit
C_I	Input Capacitance	6 to 15; 26 to 30; 32 to 36			5	pF
$C_{I/O}$	I/O Capacitance	20 to 24			15	pF
C_O	Output Capacitance	1 to 4; 17 to 19; 25; 37 to 40			10	pF

D.C. ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C, V_{CC} = 5V ±5%)
All D.C. characteristics are valid 250µs after V_{CC} and clock have been applied.

Symbol	Parameter	Pins (*)	Test Condition	Min.	Typ.	Max.	Unit
V_{ILC}	Clock Input Low Level	6		-0.3		0.8	V
V_{IHC}	Clock Input High Level	6		2.4		V_{CC}	V
V_{IL}	Input Low Level	7 to 15 20 to 24 26 to 30 32 to 36		-0.3		0.8	V
V_{IH}	Input High Level	7 to 15 20 to 24 26 to 30 32 to 36		2		V_{CC}	V
V_{OH}	Output High Voltage (Level)	17 to 25	I_{OH} = 5mA	2.4			V
I_{OH}	Output High Current		V_{OH} = 2.4V	5			mA
V_{OL}	Output Low Voltage (Level)	1 to 4	I_{OL} = 5mA			0.4	V
I_{OL}	Output Low Current	37 to 40 17 to 25	V_{OL} = 0.4V	5			mA
I_{IL}	Input Leakage Current	6 to 15 26 to 30 32 to 36	V_{IN} = 0 to V_{CC}			5	µA
I_{DL}	Data Bus Leakage Current	17 to 24	V_{IN} = 0 to V_{CC} V_{CC} applied; Pins 35 and 36 tied to V_{CC}, after Device Initialization			±5	µA
I_{CC}	Supply Current	16	Clock Freq. = 4.096MHz		15	30	mA

(*) The pin number is referred to the DIP40 version.

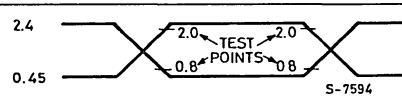
A.C. ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C, V_{CC} = 5V ±5%)
All A.C. characteristics are valid 250µs after V_{CC} and clock have been applied. C_L is the max. capacitive load.

Signal	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
CK (clock)	t_{CK}	Clock Period		230	244		ns
	t_{WL}	Clock Low Level Width		100			ns
	t_{WH}	Clock High Level Width		100			ns
	t_R	Rise Time				25	ns
	t_F	Fall Time				25	ns
SYNC (frame pulse)	t_{SL}	Low Level Setup Time		60			ns
	t_{HL}	Low Level Hold Time		30			ns
	t_{SH}	High Level Setup Time		80			ns
	t_{WH}	High Level Width		t_{CK}			ns
PCM Input Busses	t_S	Setup Time		5			ns
	t_H	Hold Time		+40			ns
PCM Output Busses Open Drain	$t_{PD\ min}$	Propagation time referred to CK low level	C_L = 150pF R_L = 1K	45	110		ns
	$t_{PD\ max}$	Propagation time referred to CK high level			110	140	ns
RESET	t_{SL}	Low Level Setup Time		60			ns
	t_{HL}	Low Level Hold Time		30			ns
	t_{SH}	High Level Setup Time		80			ns
	t_{WH}	High level Width		t_{CK}			ns
$\overline{WR}$, $\overline{RD}$	t_{WL}	Low Lvel Width		100			ns
	t_{WH}	High Level Width		t_{CK}			ns
	t_{REP}	Repetition Interval between Active Pulses		see formula			ns
	t_{SH}	High Level Setup Time to Active Read Strobe	t_{REP} 40 + 2 t_{CK} + $t_{WL(CK)}$ + + $t_{R(CK)}$	0			ns
	t_{HH}	High Level Hold Time from Active Write Strobe		15			ns
	t_R	Rise Time				60	ns
	t_F	Fall Time				60	ns

A.C. ELECTRICAL CHARACTERISTICS (continued)

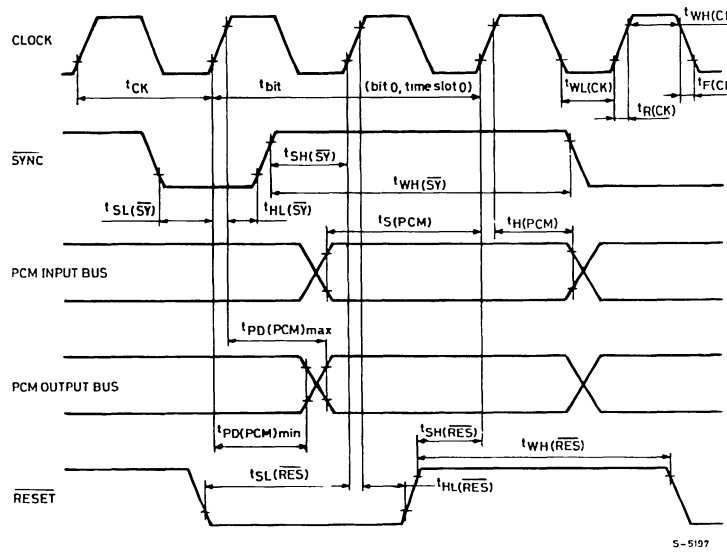
Signal	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
CS1, $\overline{CS2}$	$t_{SL(\overline{CS}\text{-}\overline{WR})}$	Low level setup time to WR falling edge	Active Case	0			ns
	$t_{HL(\overline{CS}\text{-}\overline{WR})}$	Low Level hold time from WR rising edge	Active Case	0			ns
	$t_{SH(\overline{CS}\text{-}WR)}$	High Level setup time to WR falling edge	Inactive Case	0			ns
	$t_{HH(\overline{CS}\text{-}WR)}$	High level hold time from WR rising edge	Inactive Case	0			ns
	$t_{SL(\overline{CS}\text{-}RD)}$	Low level setup time to RD falling edge	Active Case	0			ns
	$t_{HL(\overline{CS}\text{-}RD)}$	Low level hold time from RD rising edge	Active Case	0			ns
	$t_{SH(\overline{CS}\text{-}RD)}$	High level setup time RD falling edge	Inactive Case	0			ns
	$t_{HH(\overline{CS}\text{-}RD)}$	High level hold time from RD	Inactive Case	0			ns
C/$\overline{D}$	$t_{S(\overline{C/D}\text{-}WR)}$	Setup time to write strobe end		130			ns
	$t_{H(\overline{C/D}\text{-}WR)}$	Hold time from write strobe end		15			ns
	$t_{S(\overline{C/D})\text{-}RD)}$	Setup time to read strobe start		20			ns
	$t_{H(\overline{C/D}\text{-}RD)}$	Hold time from read strobe end		20			ns
A1, S1, A2, S2 (match inputs)	$t_{S(match\text{-}\overline{WR})}$	Setup time to write strobe end		130			ns
	$t_{H(match\text{-}\overline{WR})}$	Hold time from strobe end		15			ns
	$t_{S(match\text{-}\overline{RD})}$	Setup time to read strobe start		20			ns
	$t_{H(match\text{-}\overline{RD})}$	Hold time from read strobe end		20			ns
DR (data ready)	t_W	Low state width	Instructions 5 and 6			2.t_{CK}	ns
	t_{PD}	DR output delay from write strobe end (active command)	Instruction 5, C_L = 150pF	4.t_{CK}		7.t_{CK}	ns
D0 to D7 (interface bus)	$t_{S(\overline{BUS}\text{-}WR)}$	Input setup time to write strobe end		130			ns
	$t_{H(\overline{BUS}\text{-}WR)}$	Input hold time from write strobe end		15			ns
	$t_{PD(BUS)}$	Propagation time from (active) falling Edge of read strobe	C_L = 200pF			120	ns
	$t_{HZ(BUS)}$	Propagation time from (active) rising Edge of read strobe to high impedance state	C_L = 200pF			80	ns

A.C. TESTING, OUTPUT WAVEFORM

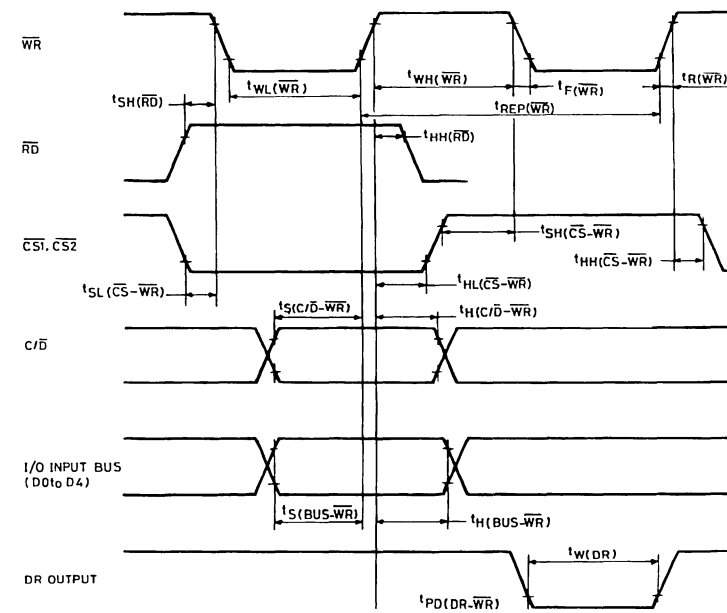


A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0", timing measurement are made at 2.0V for a logic "1"and 0.8V for a logic "0".

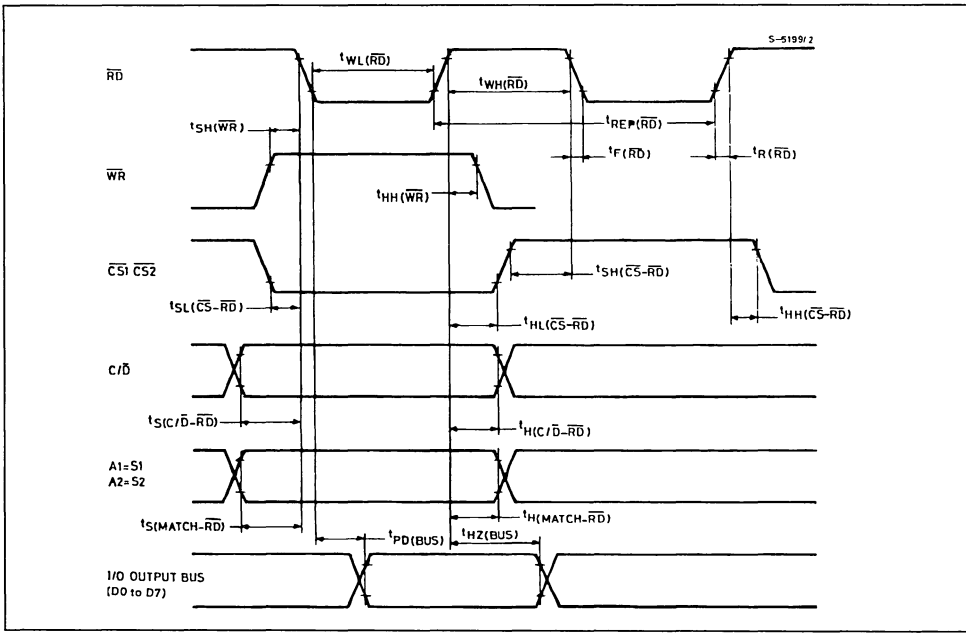
PCM TIMING, $\overline{RESET}$, $\overline{SYNC}$



WRITE OPERATION TIMING



READ OPERATION TIMING



GENERAL DESCRIPTION

The M3488 is intended for large telephone switching systems, mainly central exchanges, digital line concentrators and private branch exchanges where a distributed microcomputer control approach is extensively used. It consists of a speech memory (SM), a control memory (CM), a serial/parallel and a parallel/serial converter, an internal parallel bus, an interface (8 data lines, 11 control signals) and dedicated control logic.

By means of repeated clock division two timebases are generated. These are preset from an external synchronization signal to two specific count numbers so that sequential scanning of the bases give synchronous addresses to the memories and I/O channel controls. Different preset count numbers are needed because of processing delays and data path direction. The timebase for the input channels is delayed and the timebase for output channels is advanced with respect to the actual time.

Each serial PCM input channel is converted to parallel data and stored in the speech memory at the beginning of any new time slot (according to first timebase) in the location determined by input pin number and time slot number. The control memory CM maintains the correspondences between input and output channels. More exactly, for any output pin/output channel combination the control memory gives either the full address of the speech memory location involved in the PCM transfer or an 8-bit word to be supplied to the parallel/serial output converter. A 9th bit at each CM location defines the data source for output links, low for SM, high for CM.

The late timebase is used to scan the output channels and to determine the pins to be serviced within each channel ; enough idle cycles are left to the microprocessor for asynchronous instruction processing.

Two 8-bit registers OR1 and OR2 supply feedback data for control or diagnostic purposes ; OR1 comes from internal bus i.e. from memories, OR2 gives an opcode copy and additional data to the microcomputer. A four byte-five bit stack register and an instruction register, under microcomputer control, store input data available at the interface.

Dedicated logic, under control of the microprocessor interface, extracts the 0 channel content of any selected PCM input bus, using spare cycles of SM.

PINS FUNCTION

Symbol	Name	Pin Assignement	
		DIP40	PQFP44
D7 to D0	Data bus	17 to 24	13 to 21
C/$\overline{D}$	Input control	30	27
A1, S1, A2, S2	Address select or match	26 to 29	23 to 26
$\overline{CS1}$, $\overline{CS2}$	Chip select	33, 34	30, 31
$\overline{WR}$	Data transfer enable	35	32
$\overline{RD}$	Read enable	36	34
DR	Data ready	25	22
$\overline{RESET}$	$\overline{RESET}$ control	32	29
CLOCK	Input master clock	6	1
$\overline{SYNC}$	Input synchronization	7	2
IN PCM 7 to 0	PCM input bus	8 to 15	3 to 10
OUT PCM 7 to 0	PCM output bus	37 to 40 and 1 to 4	35 to 38 and 40 to 43

PIN DESCRIPTION

D7 to D0

Data bus pins. The bidirectional bus is used to transfer data and instructions to/from the microprocessor. D0 is the least significant digit. The output bus is 8 bits wide ; input is only 5 bits wide. (D4 to D0)

The bus is tristate and cannot be used while $\overline{\text{RESET}}$ is held low.

The meaning of input data, such as bus or channel numbers, and of expected output data is specified in detail by the instruction description. (Pagg. 12-14)

C/$\overline{\text{D}}$ (pin 30)

Input control pin, select pin. In a write operation C/$\overline{\text{D}}$ = 0 qualifies any bus content as data, while C/$\overline{\text{D}}$ = 1 qualifies it as an opcode. In a read operation OR1 is selected by C/$\overline{\text{D}}$ = 0, OR2 by C/$\overline{\text{D}}$ = 1.

A1, S1, A2, S2

Address select or match pins. In a multi-chip configuration (e.g. a single stage matrix expansion), using the same $\overline{\text{CS}}$ pins, the match condition (A1 = S1 and A2 = S2) leaves the command instruction as defined; on the contrary the mismatch condition modifies the execution as follows : instructions 1 and 3 are reversed to channel disconnection, instruction 5 is unaffected, instructions 2-4-6 are cancelled (not executed).

Bus reading takes place only on match condition, instruction flow is in any case affected.

Each pins couple is commutative : in a multichip configuration pins S1 and S2 give a hard-wired address selection for individual matrixes, while in single configuration S1 and A1 or S2 and A2 are normally tied together.

$\overline{\text{CS1}}$, $\overline{\text{CS2}}$

Commutative chip select pins. They enable the device to perform valid read/write operations (active low). Two pins allow row/column selection with different types of microprocessors ; normally one is tied to ground.

$\overline{\text{WR}}$

Pin $\overline{\text{WR}}$, when $\overline{\text{CS1}}$ and $\overline{\text{CS2}}$ are low, enables data transfer from microprocessor to the device. Data or opcode and controls are latched on $\overline{\text{WR}}$ rising edge. Because of internal clock resynchronization one single additional requirement is recommended in order to produce a simultaneous instruction execution in a multichip configuration : $\overline{\text{WR}}$ rising edge has to be 20 to 20 + $t_{WL(CK)}$ nsec late relative to clock falling edge.

$\overline{\text{RD}}$

When CS1 and CS2 are low and match condition exists, a low level on $\overline{\text{RD}}$ enables a register OR1 or OR2 read operation, through the bidirectional bus.

In addition, the rising edge of $\overline{\text{RD}}$ latches C/$\overline{\text{D}}$ and the match condition pins in order to direct the internal flow of operations. Because of internal clock resynchronization, one single additional requirement is recommended in order to produce a simultaneous instruction flow in a multichip configuration: the $\overline{\text{RD}}$ rising edge has to be 20 to 20 + $t_{WL(CK)}$ nsec late relative to clock falling edge.

DR

Data ready. Normally high, DR output pin goes low to tell the microprocessor that :

a) the instruction code was found to be invalid ;

b) executing instruction 5 an active output channel was found in the whole matrix array, that is a CM word not all "ones" was found in a configuration of devices sharing the same CS pins ;

c) executing instruction 6 "0 channel extraction" took place and OR2 was loaded with total number of messages inserted on 0 time slot.

DR is active low about two clock cycles in case **b** and **c** ; in case a it is left low until a valid instruction code is supplied.

$\overline{\text{RESET}}$

$\overline{\text{RESET}}$ control pin is normally used at the very beginning to initialize the device or the network. Any logical status is reset and CM is set to all "ones" after $\overline{\text{RESET}}$ going low.

The internal initialization routine takes one time frame whatever the $\overline{\text{RESET}}$ width on low level (minimum one cycle roughly), but it is repeated an integer number of time frames as long as $\overline{\text{RESET}}$ is found low during 0 time slot.

Initialization pulls the interface bus immediately to a high impedance state. After the CM has been set to all "ones" the PCM output channels are also set to high impedance state.

CLOCK

Input master clock. Typical frequency is 4.096MHz. First division gives an internal clock controlling the input and output channels bit rate.

$\overline{\text{SYNC}}$

Input synchronization signal is active low. Typical frequency is 8kHz.

Internal time bases are forced by synchronism to an assigned count number in order to restore channels and bit sequential addressing to a known state. Count difference between the bases is 32, corresponding to two time slots, that is the minimum PCM propagation time, or latency time.

INP PCM 7 to INP PCM 0

PCM input busses or pins ; they accept a standard 2Mbit/s rate. Bit 1 (sign bit) is the first of the serial sequence ; in a parallel conversion it is left adjusted as the most significant digit.

OUT PCM 7 to OUT PCM 0

PCM output busses or pins ; bit rate and organization are the same as input pins.

Output buffers are open drain CMOS .

The device drives the output channels theoretically one bit time before they can be exploited as logical input channels (bit and slot compatibility is preserved): this feature allows inputs and outputs to be tied together cancelling any analog delay of digital outputs up to

$t_{DEL\,max} = t_{bit} - t_{PD(PCM)max} + t_{PD(PCM)min}$

MIXED $\overline{RD}$ and $\overline{WR}$ OPERATIONS

In principle $\overline{RD}$ and $\overline{WR}$ operations are allowed in any order within specification constraints.

In practive, only one control pin is low at any given time when CS1 and CS2 are enabled.

If by mistake or hardware failure both $\overline{RD}$ and $\overline{WR}$ pins are low, the interface bus is internally pushed to tristate condition as long as $\overline{WR}$ is held low and input registers are protected.

Registers OR1 and OR2 can be read in any order with a single $\overline{RD}$ strobe using C/$\overline{D}$ as multiplexing control ; never the less this procedure is not recommended because the device is directed for instruction flow only according to data latched by $\overline{RD}$ rising edge.

Multiple $\overline{RD}$ operations of the same kind are allowed without affecting the instruction flow : only "new" OR1 or OR2 read operations step the flow.

Input and output registers are held for sure in the previous state for the first 3 cycles following an opcode or an OR2 read.

FUNCTIONAL DESCRIPTION OF SPECIFIC MICROPROCESSOR OPERATIONS

The device, under microprocessor control, performs the following instructions :

1 CHANNEL CONNECTION

2 CHANNEL DISCONNECTION

3 LOADING OF A BYTE ON A PCM OUTPUT CHANNEL

4 TRANSFER OF A SINGLE PCM OUTPUT CHANNEL SAMPLE

5 TRANSFER OF A SINGLE OUTPUT CHANNEL CONTROL WORD

6 TRANSFER OF A SELECTED 0 CHANNEL PCM INPUT DATA ACCORDING TO AN 8-BIT MASK PREVIOUSLY STORED IN THE "EXPECTED MESSAGES" REGISTER

The instruction flow is as follows.

Any input protocol is started by the microprocessor interface loading the internal stack register with 2 bytes (4 bytes for instructions 1 and 3) qualified as data bytes by C/$\overline{D}$ = 0 and a specific opcode qualified by C/$\overline{D}$ = 1 (match condition is normally needed).

After the code is loaded in the instruction register it is immediately checked to see whether it is acceptable and if not it is rejected. If accepted the instruction is also processed as regards match condition and is appended for execution during the memories' spare cycles.

Four cases are possible :

a) the code is not valid ; execution cannot take place, the DR output pin is reset to indicate the error ; all registers are saved ;

b) the code is valid for types 2, 4 and 6 but it is unmatched ; execution cannot take place, DR is not affected.

c) the code is valid for types 1 and 3 and it is unmatched ; the instruction is interpreted as a channel disconnection.

d) the code is valid and is either matched or of type 5 ; the instruction is processed as received.

Validation control takes only two cycles out of a total execution time of 4 to 7 cycles ; the last operation is updating of the content of registers OR1 and OR2, according to the following instruction tables.

During a very long internal operation (device initialization after RESET going high or execution of instruction 6) a new set of data bytes with a valid opcode is accepted while a wrong code is rejected. At the end of the current routine execution takes place in the same way as described before.

At the end of an instruction it is normally recommended to read one or both registers. To exploit instruction 6, however, it is mandatory to read register OR2. This is because instruction 6, used between other short instructions of type 1 to 5, must have priority and can be enabled only after the short instructions have been completed. Instruction 6 normally has a long process and a special flow which is described below.

First a not-all-zero mask is stored in the "expected messages" register and in another "background" register. This operation starts the second phase of instruction 6 which is called "channel 0 extraction" and is repeated at the beginning of any new time frame. At the beginning of the time frame a new copy of activated channels to be extracted is made from the "background register" and put in the "expected messages" register. In addition the latter register is modified to indicate the exact number of messages that have arrived. The term messages covers any input 0 channel data with starting sequence different from the label 01. So using this label the number of expected messages can be reduced to correspond to the number of effective messages. If and only if the residual number is different from zero will the device start the extraction protocol at the end of the current routine.

The procedure is as follows : the DR output is pulsed low as a two cycle interrupt request and OR2 is loaded with the total number of active channels to be extracted.

The transfer of OR2 content to the microprocessor continues the extraction which consists of repeated steps of OR1 and OR2 loading, indicating respectively the message and the incoming bus number. Reading the registers in the order OR1, OR2 must be continued until completion or until the time frame runs out.

With a new time frame a new extraction process begins, resuming the copy operation from the background register.

During extraction the active channels are scanned from the highest to the lowest number (from 7 to 0). While extraction is being carried out the time interval requirements between active rising edges of $\overline{RD}$ are minimum 4 to 7 t_{CK} for sequence OR2 - OR1 and minimum 2 times t_{CK} for sequence OR1 - OR2. More details are given in the following tables.

INSTRUCTION TABLES

The most significant digits of OR2 A7, A6, A5 are a copy of the PCM selected output bus ; the least significant digits of OR2 are the opcode, C8 is the control bit. In any case parentheses () define actual register content.

INSTRUCTION 1: CHANNEL CONNECTION

Control Signals					Data Bus								Notes
Match	C/$\overline{D}$	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	Bi2	Bi1	Bi0	1st Data Byte: selected input bus.
X	0	0	0	1	X	X	X	Ci4	Ci3	Ci2	Ci1	Ci0	2nd Data Byte: selected input channel.
x	0	0	0	1	X	X	X	X	X	Bo2	Bo1	Bo0	3rd Data Byte: selected output bus.
X	0	0	0	1	X	X	X	Co4	Co3	Co2	Co1	Co0	4th Data Byte: selected output channel.
yes/no	1	0	0	1	X	X	X	X	0	0	0	1	Instruction Opcode
yes	0	0	1	0	C7 (1 (Bi2	C6 1 Bi1	C5 1 Bi0	C4 1 Ci4	C3 1 Ci3	C2 1 Ci2	C1 1 Ci1	C0 1) Ci0)	OR1: CM content copy, that is, for mismatch condition, for match condition
yes	1	0	1	0	A7 (Bo2 (Bo2	A6 Bo1 Bo1	A5 Bo0 Bo0	C8 1 0	0 0 0	0 0 0	0 0 0	1 1) 1)	OR2: that is, for mismatch condition for match condition

INSTRUCTION2: OUTPUT CHANNEL DISCONNECTION

Control Signals					Data Bus								Notes
Match	C/D	CS	WR	RD	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	Bo2	Bo1	Bo0	1st Data Byte: selected output bus.
X	0	0	0	1	X	X	X	Co4	Co3	Co2	Co1	Co0	2nd Data Byte: selected output channel.
Yes	1	0	0	1	X	X	X	X	0	0	1	0	Instruction Opcode
Yes	0	0	1	0	1	1	1	1	1	1	1	1	OR1: CM Content Copy (output channel is inactive)
Yes	1	0	1	0	A7 (Bo2	A6 Bo1	A5 Bo0	1 1	0 0	1 1	1 1	1 1)	OR2: that is.

INSTRUCTION3: LOADING ON A PCM OUTPUT CHANNEL FROM A MICROPROCESSOR BYTE

Control Signals					Data Bus								Notes
Match	C/D	CS	WR	RD	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	Ci7	Ci6	Ci5	1st Data Byte: most significant digits to be inserted.
X	0	0	0	1	X	X	X	Ci4	Ci3	Ci2	Ci1	Ci0	2nd Data Byte: least significant digits to be inserted.
X	0	0	0	1	X	X	X	X	X	Bo2	Bo1	Bo0	3rd Data Byte: selected output bus.
X	0	0	0	1	X	X	X	Co4	Co3	Co2	Co1	Co0	4th Data Byte: selected output channel..
Yes/no	1	0	0	1	X	X	X	X	0	1	0	0	Instruction Opcode
Yes	0	0	1	0	C7 (1 (Ci7	C6 1 Ci6	C5 1 Ci5	C4 1 Ci4	C3 1 Ci3	C2 1 Ci2	C1 1 Ci1	C0 1) Ci0)	OR1: CM content copy, that is, for mismatch condition, for match condition
Yes	1	0	1	0	A7 (Bo2	A6 Bo1	A5 Bo0	1 1	0 0	1 1	1 1	1 1)	OR2: that is.

INSTRUCTION4: TRANSFER OF A SINGLE PCM SAMPLE

Control Signals					Data Bus								Notes
Match	C/D	CS	WR	RD	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	Bo2	Bo1	Bo0	1st Data Byte: selected output bus.
X	0	0	0	1	X	X	X	Co4	Co3	Co2	Co1	Co0	2nd Data Byte: selected output channel.
Yes	1	0	0	1	X	X	X	X	1	0	1	1	Instruction Opcode
Yes	0	0	1	0	C7 S7	C6 S6	C5 S5	C4 S4	C3 S3	C2 S2	C1 S1	C0 S0	OR1: CM Content Copy if C8 = 1; or SM Content Sample if C8 = 0
Yes	1	0	1	0	A7 (Bo2	A6 Bo1	A5 Bo0	1 1	0 0	1 1	1 1	1 1)	OR2: that is.

Notes : S7...S0 is a parallel copy of a PCM data, S7 is the most significant digit and the first of the sequence.

INSTRUCTION5: TRANSFER OF AN OUTPUT CHANNEL CONTROL WORD

Control Signals					Data Bus								Notes
Match	C/D	CS	WR	RD	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	Bo2	Bo1	Bo0	1st Data Byte: selected output bus.
X	0	0	0	1	X	X	X	Co4	Co3	Co2	Co1	Co0	2nd Data Byte: selected output channel.
Yes	1	0	0	1	X	X	X	X	1	0	0	0	Instruction Opcode
Yes	0	0	1	0	C7	C6	C5	C4	C3	C2	C1	C0	OR1: CM selected CM word copy.
Yes	1	0	1	0	A7 (Bo2	A6 Bo1	A5 Bo0	C8 C8	1 1	0 0	0 0	0 0)	OR2: that is.

INSTRUCTION6: CHANNEL 0 SELECTION MASK STORE/DATA TRANSFER

Control Signals					Data Bus								Notes
Match	C/D	CS	WR	RD	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	1	X	X	X	X	X	Mi7	Mi6	Mi5	1st Data Byte: most sign. digits of selection mask.
X	0	0	0	1	X	X	X	Mi4	Mi3	Mi2	Mi1	Mi0	2nd Data Byte: least sign. digits of selection mask.
Yes	1	0	0	1	X	X	X	X	1	1	1	0	Instruction Opcode
Mask store control													
Yes	0	0	1	0	(previous content)								OR1: register is not affected.
Yes	1	0	1	0	N2	N1	N0	Tn	1	1	1	0	OR2: see below.
First Data Transfer (after DR going low)													
Yes	0	0	1	0	(previous content)								OR1: register is not affected.
Yes	1	0	1	0	N2	N1	N0	Tn	1	1	1	0	OR2: see below.
Repeated Data Transfer (after first OR2 transfer)													
Yes	0	0	1	0	S7	S6	S5	S4	S3	S2	S1	S0	OR1: expected message stored in SM.
Yes	1	0	1	0	P2	P1	P0	Fn	1	1	1	0	OR2: see below.

Notes :
1. About mask bits Mi0 to Mi7 a logic "0" level means disabling condition, a logic "1" level means enabling condition.
2. A null mask or a RESET pulse clear the mask and the deep background mask registers and disable channel 0 extraction function.
3. Reading of OR2 is optional after mask store or redefinition, because function is activated only by not-null mask writing.
4. After mask store (N2 N1 N0) is the sum of activated channels, after DR is the sum of active channels ; Tn = 1/0 means activation/suppression of the function after store while after DR only Tn = 1 can appear to tell a not-null configuration to be extracted
5. Reading of OR2 is imperative after DR in order to step the data transfer ; reading of OR1 is also needed to scan in descending order the priority register. Relevant messages only are considered, that means only messages with a MSD label different from 0 1.
6. (P2 P1 P0) is the PCM bus on which the message copied in OR1 was found ; Fn is a continuation bit telling respectively on level 1/0 for any more/no more extraction step to be performed.

M3488 WITH LESS PCM LINKS THAN 32 CHANNELS

It is also possible to use M3488 when the PCM frames are made up of a number of channels other than 32.

Suppose that the PCM frames are made up of N-Channels, which will be numbered from 0 to (N-1).

Each PCM frame will thus be made up of a number of bits multiplied by 8 ; this exactly equal to (N · 8).

Also, in this case, it is necessary to respect the timing relationship between the different signals shown on the data sheet ; in particular, a relation-ship is always carefully made between the rising edge of SYNC and the first clock (CK) bit contained in the slot time for bit 0 of channel 0.

In order to use M3488 with these frames, it is sufficient, using the data bytes sent by the microprocessor, to modify the numbering of a few channels.

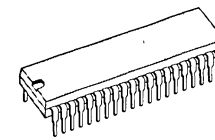
In particular :

a) in all instructions in which reference is made to the input channel (N-1), the number 31 should be substituted for the number (N-1) ;

b) in all instructions in which reference is made to the output channel 0, the number N should be substituted for the number 0.

CMOS 12 X 8 CROSSPOINT WITH CONTROL MEMORY

- LOW ON RESISTANCE (typ. 60 Ω at V_{DD} = 10 V)
- INTERNAL CONTROL LATCHES
- ANALOG SIGNAL SWING CAPABILITY EQUAL TO POWER SUPPLY VOLTAGE APPLIED
- LESS THAN 1 % TOTAL DISTORT. AT 0 dBm
- LESS THAN – 95 dB CROSS-TALK AT 1 KHz 1 V_{PP}
- VERY LOW POWER CONSUMPTION
- PIN-TO-PIN COMPATIBLE WITH M093



DIP40

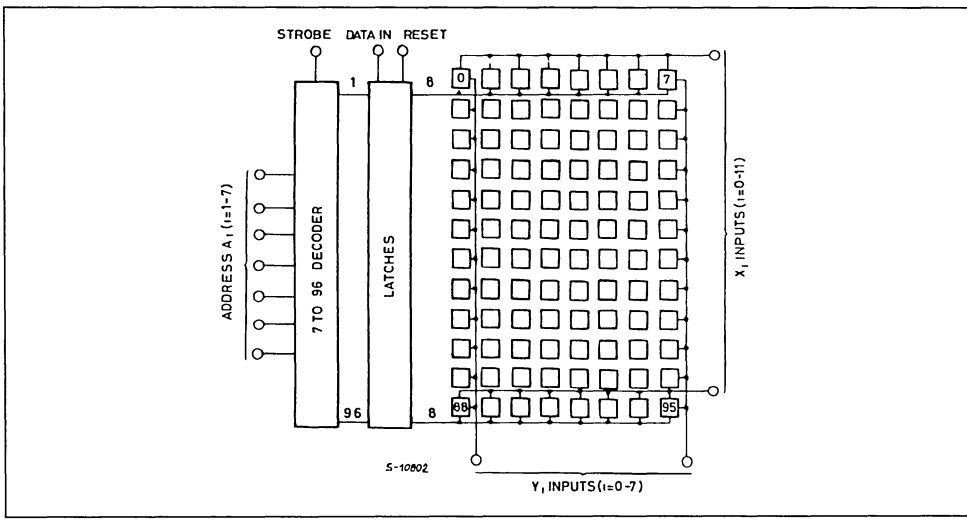
ORDERING NUMBER : M3493B1

DESCRIPTION

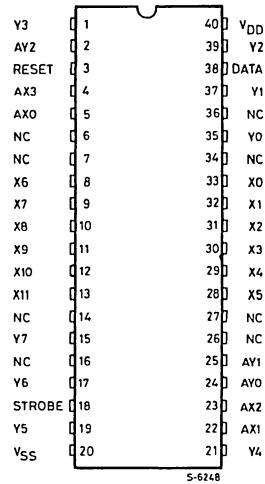
The M3493 contains a 12 x 8 array of crosspoint together with a 7 to 96 line decoder and latch circuits. Anyone of the 96 switches can be addressed by selecting the appropriate 7 input bits. The selected switch can be turned on or off by applying a logical one or zero to the data in and the strobe input at logical one. A reset signal can be used to turn off all the switches together when is switched at logical one.

M3493 is available in 40 lead dual in-line plastic package.

BLOCK DIAGRAM



PIN CONNECTION (top view)



INPUT/OUTPUT DESCRIPTION

I/O	Symbol	Pin	Description
POWER			
I	V_{DD}	40	Positive Power Supply
I	V_{SS}	20	Negative Power Supply
ADDRESS			
I	AX0-AX3	4, 5, 22, 23	X Address Lines. These 4 pins are used to select one of the 12 rows of switches. Refer to the truth table for legal address.
I	AY0-AY2	2, 24, 25	Y Address Lines. These 3 pins are used to select one of the 8 columns of switches. Refer to the truth table for legal address.
CONTROL			
I	DATA	38	This input determines if the selected switch will be turned on (closed) or off (opened). If the pin is held high, the selected switch will be closed. If the pin is held low, the switch will be opened.
I	STROBE	18	This pin enables whatever action is selected by the ADDRESS and DATA pins. When the STROBE pin is held low, no switch openings or closings take place. When the STROBE pin is held high, the switch addressed by the select lines will be opened or closed (depending upon the state of the DATA pin)
I	RESET	3	Master Reset. This pin turns off (opens) all 96 switches. The states of the above control lines are irreleant. This pin is active high.
DATA			
I/O	X0-X11	8-13, 28-33	Analog Input/Outputs. These pins are connected to the Y0-Y7 pins in according to the truth table.
I/O	Y0-Y7	1,15,17,19,21 35,37,39	Analog Input/Outputs. These pins are connected to the X0-X15 pins in according to the truth table.

TRUTH TABLE

Address							Connections
AX0	AX1	AX2	AX3	AY0	AY1	AY2	
0	0	0	0	0	0	0	X0 - Y0
1	0	0	0	0	0	0	X1 - Y0
0	1	0	0	0	0	0	X2 - Y0
1	1	0	0	0	0	0	X3 - Y0
0	0	1	0	0	0	0	X4 - Y0
1	0	1	0	0	0	0	X5 - Y0
0*	1	1	0	0	0	0	No connection
1*	1	1	0	0	0	0	No connection
0	0	0	1	0	0	0	X6 - Y0
1	0	0	1	0	0	0	X7 - Y0
0	1	0	1	0	0	0	X8 - Y0
1	1	0	1	0	0	0	X9 - Y0
0	0	1	1	0	0	0	X10 - Y0
1	0	1	1	0	0	0	X11 - Y0
0*	1	1	1	0	0	0	No connection
1*	1	1	1	0	0	0	No connection
0	0	0	0	1	0	0	X0 - Y1
↓	↓	↓	↓	↓	↓	↓	↓ <0> ↓
1	0	1	1	1	0	0	X11 - Y1
0	0	0	0	0	1	0	X0 - Y2
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	0	1	0	X11 - Y2
0	0	0	0	1	1	0	X0 - Y3
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	1	1	0	X11 - Y3
0	0	0	0	0	0	1	X0 - Y4
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	0	0	1	X11 - Y4
0	0	0	0	1	0	1	X0 - Y5
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	1	0	1	X11 - Y5
0	0	0	0	0	1	1	X0 - Y6
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	0	1	1	X11 - Y6
0	0	0	0	1	1	1	X0 - Y7
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	1	1	1	X11 - Y7

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	DC supply Voltage	- 0.5, 14	V
V_{IN}	Input Voltage Range	- 0.5, V_{DD} + 0.5	V
P_{tot}	Power Dissipation	1	W
T_{oper}	Operating Temperature Range	0, + 70	°C
T_{stg}	Storage Temperature Range	- 50, + 125	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	10	V
T_{oper}	Operating Temperature	0, + 70	°C
V_{IN}	(Logic Signal)	0, V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C, V_{DD} = 10V, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_S	Supply Current	Reset = V_{DD}			1	mA
CROSSPOINT						
	On Resistance	V_{IDC} = 4.75V, V_{ODC} = 4.5V, See Figure 1		60	100	Ω
	On Resistance Variation			10	20	Ω
	Off-leakage *	All switches off V_{OS} = V_{IS} = 0 to V_{DD}			± 3	µA
CONTROLS						
V_{IL}					0.8	V
V_{IH}			2.4			V
	Input Leakage *	V_{IN} = 0 to V_{DD}			± 3	µA

* The device is guaranteed with such limits up to 70°C. At 25°C these limits become ± 100nA.

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_{amb} = 25°C, C_L = 50pF all input square wave rise and fall times = 10ns, V_{DD} = 10V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
CROSSPOINT							
t_{PHL}, t_{PLH}	Propagation Delay Time (switch on) Signal Input to Output	R_H = 1kΩ, V_{IS} = $2V_{PP}$		30	100	ns	2
	Frequency Response (any switch on) 20 log (V_{OS}/V_{IS}) = -3dB	R_H = 81Ω, V_{IS} = $2V_{PP}$, C_L = 3pF		50		MHz	
	Sine Wave Distortion	f_q = 1kHz, R_H = 0.6kΩ, V_{IS} = $8V_{PP}$			1	%	
	Feed Through (any switches off)	f_q = 10kHz, R_H = 1kΩ, V_{IS} = $2V_{PP}$	-80			dB	3
	Frequency for Signal Crosstalk Attenuation of 40dB Attenuation of 110dB	R_H = 1kΩ, V_{IS} = $2V_{PP}$	 1 5			 MHz kHz	4
C	Capacitance Xn to Ground Vn to Ground Feed Through	f_q = 1MHz, V_{IS} = $0.1V_{PP}$		 15 15 0.4		pF	
C	Capacitance Logic Input to Ground	f_q = 1MHz, V_{IS} = $0.1V_{PP}$		5		pF	
CONTROLS (t_r, t_f = 10ns)							
t_{PSN}	Propagation Delay Time Strobe to Output (switch turn-on to high level)	R_L = 1kΩ, C_L = 50pF		150	200	ns	5
t_{PZH}	Data-in to Output (turn-on to high level)			150	200	ns	6
t_{PAN}	Address to Output (turn-on to high level)			150	200	ns	7
t_{PSF}	Propagation Delay Time Strobe to Output (switch turn-off)			150	200	ns	5
t_{PZL}	Data-in to Output (turn-on to low level)			150	200	ns	6
t_{PAF}	Address to Output (turn-off)			150	200	ns	7
t_S	Set-up Time Data-in to Strobe		40			ns	5 10
t_H	Hold Time Data-in to Strobe		120			ns	5 10
t_O	Switching Frequency			1		MHz	
t_W	Strobe Pulse Width		100			ns	10
t_{WR}	Reset Pulse Width		150			ns	9
t_{PHZ}	Reset Turn-off to Output Delay			150	200	ns	9
t_{AS}	Address Set-up Time Address to Strobe		120			ns	10
t_{AH}	Address Hold Time Address to Strobe		120			ns	10
	Control Crosstalk Data-in, Address or Strobe to Output	Square wave input, V_{IN} = 3V, R_L = 10kΩ		75		mV	8

TEST CIRCUITS

Figure 1 : R_{ON} Measurement.

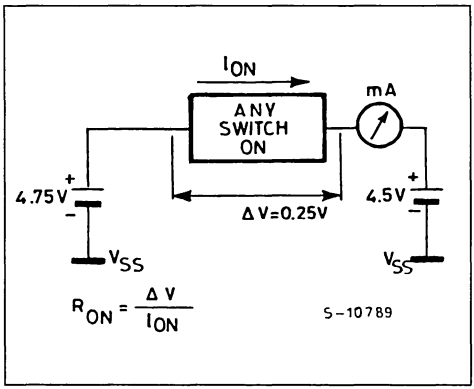


Figure 2 : Propagation Delay Time and Waveforms (signal input to signal output switch ON).

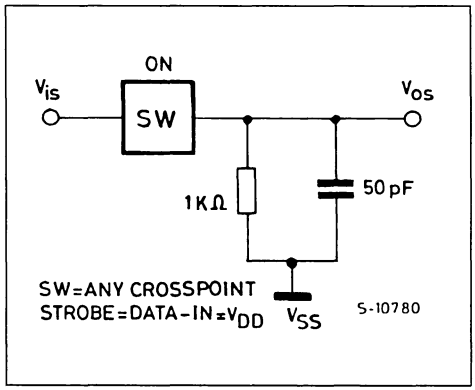
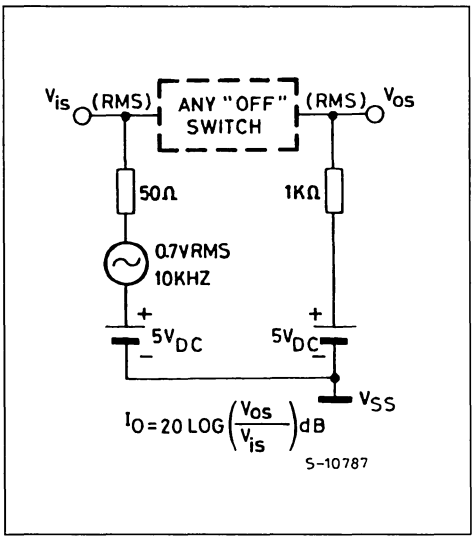


Figure 3 : Off Isolation Measurement (Feed through).



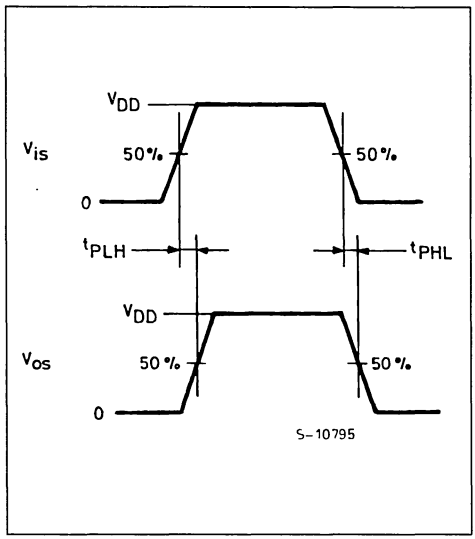


Figure 4 : Crosstalk Measurements.

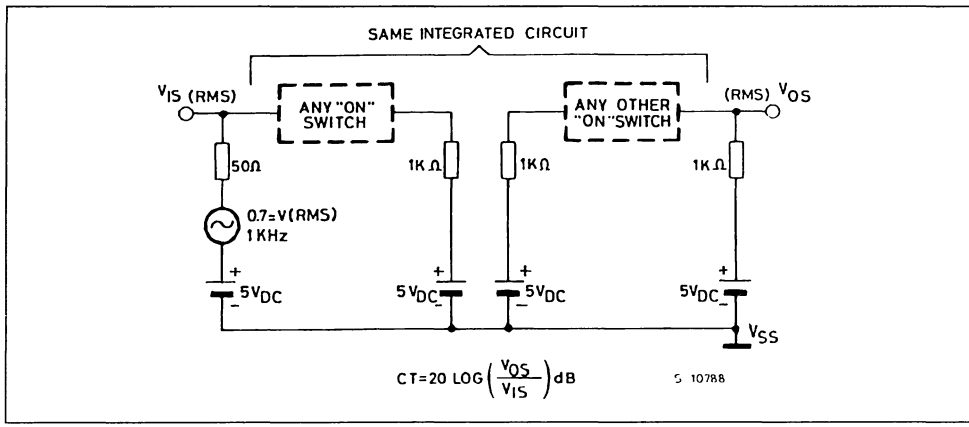


Figure 5 : Propagation Delay Time and Waveforms (strobe to signal output switch Turn-ON or Turn-OFF).

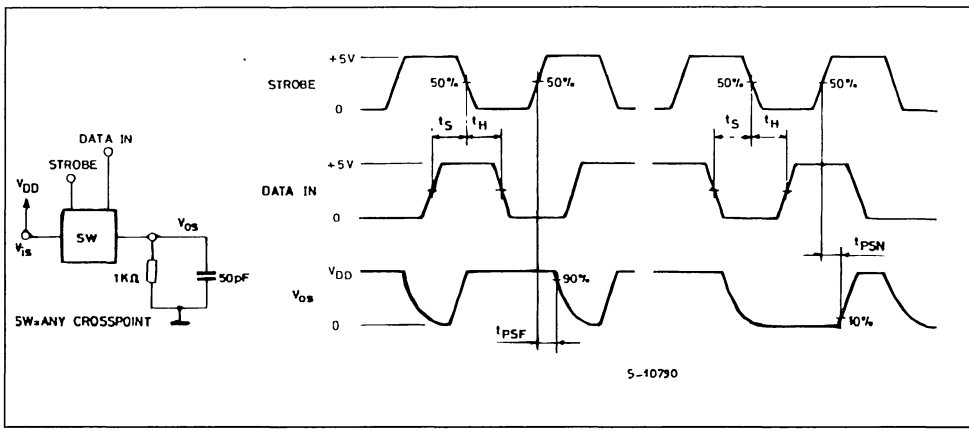


Figure 6 : Propagation Delay Time and Waveforms (data-in signal output, switch Turn-ON to high or low level).

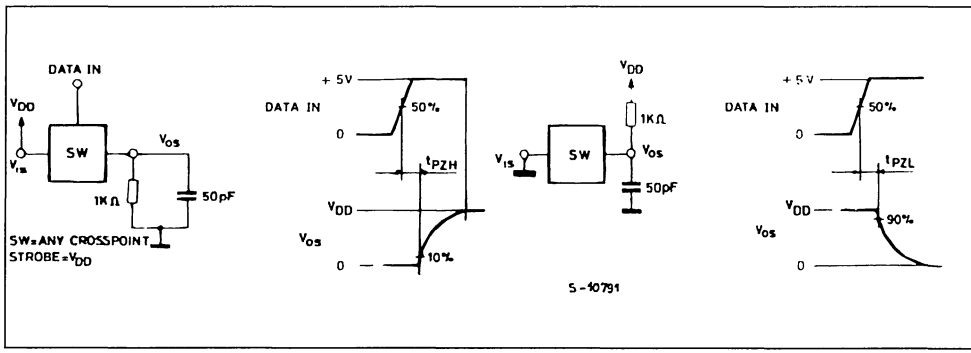


Figure 7 : Propagation Delay Time and Waveforms (address to signal output switch Turn-ON or Turn-OFF).

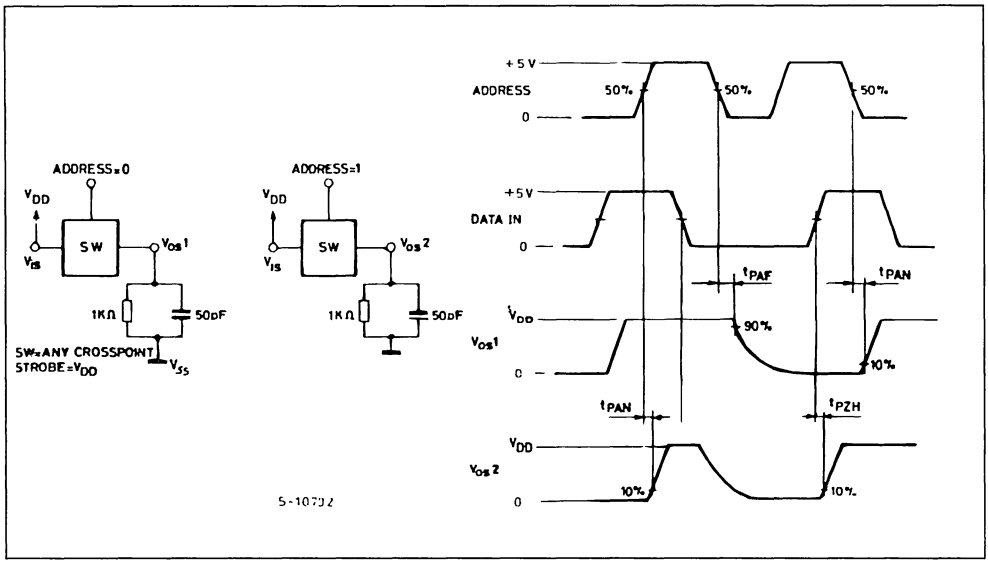


Figure 8 : Waveforms for Crosstalk (control input to signal output).

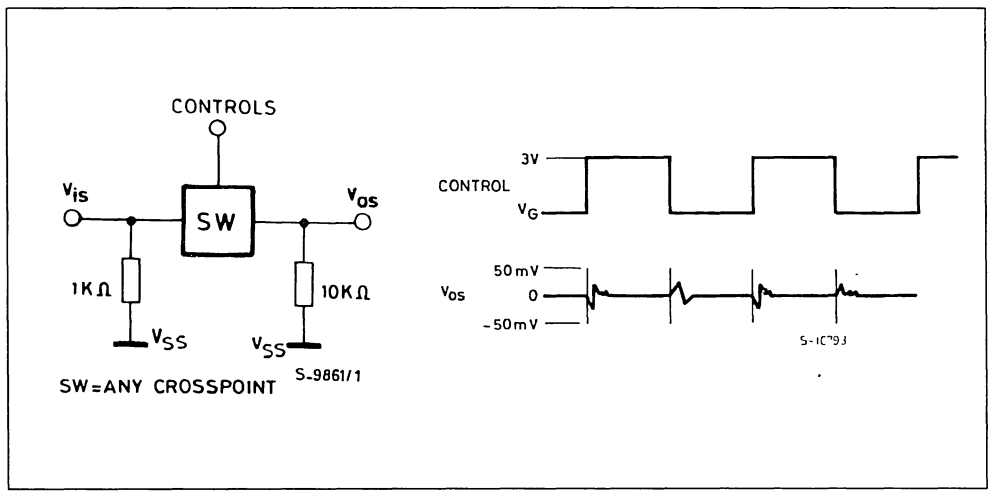


Figure 9 : Propagation Delay Time and Waveforms (reset to output delay).

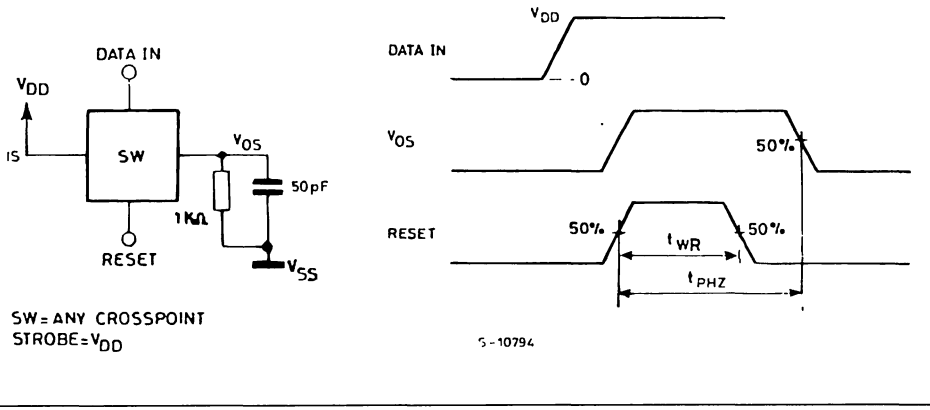


Figure 10 : Propagation Delay Time and Waveforms (Strobe and C/S to signal output switch).

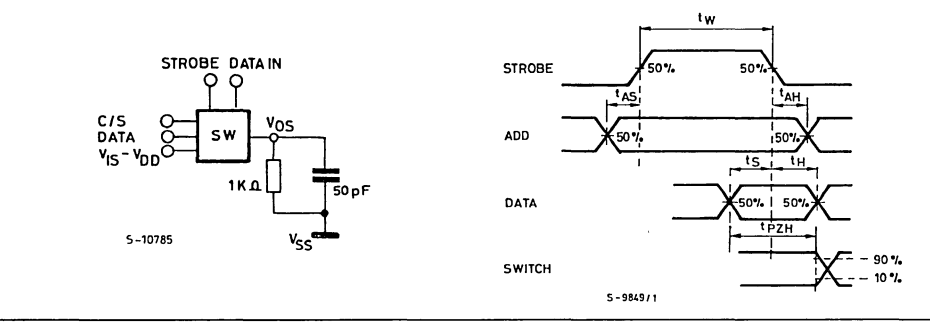


Figure 11 : Typical R_{ON} versus V_{is}.

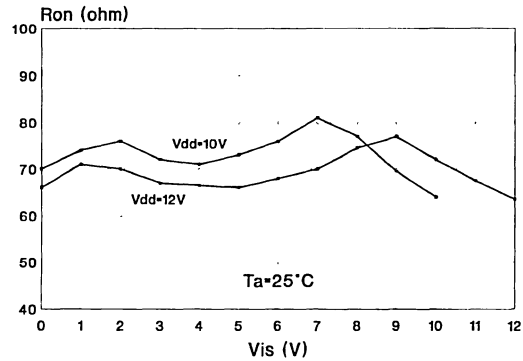


Figure 12 : Peak to Peak Voltage Capability versus Total Harmonic Distortion.

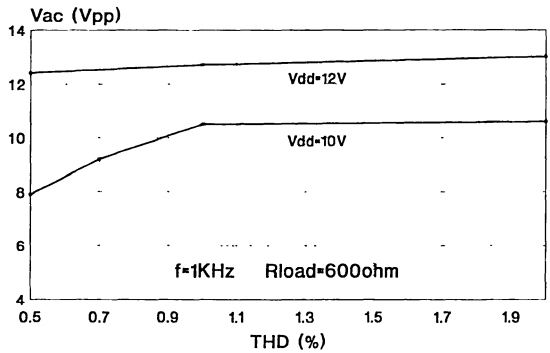
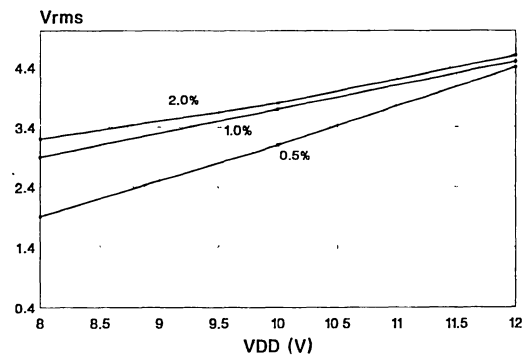


Figure 13 : V_{RMS} Capability versus V_{DD}.



TYPICAL APPLICATIONS

The figures 14, 15 and 16 show the system configuration for expanded matrices (16 x 16, 8 x 64, 32 x 32).

Figure 14 : (16 x 16 non blocking matrix).

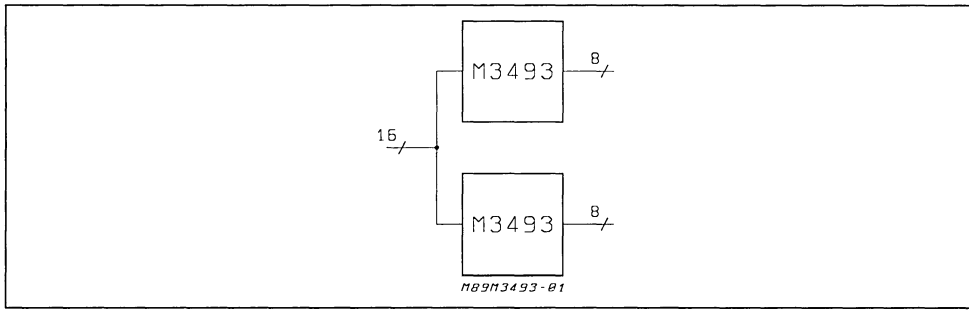


Figure 15 : (8 x 64 matrix).

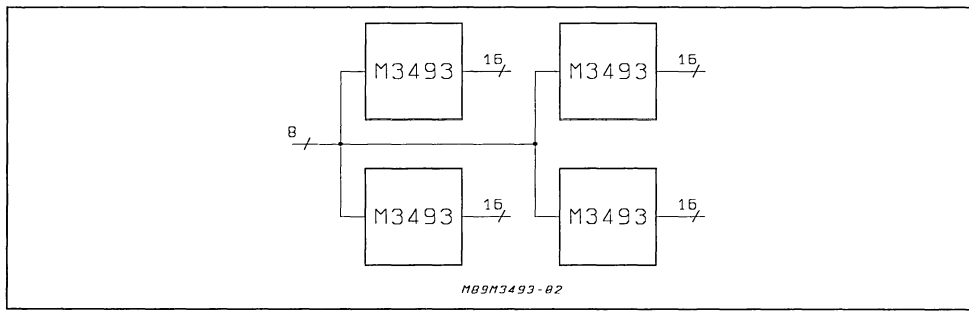
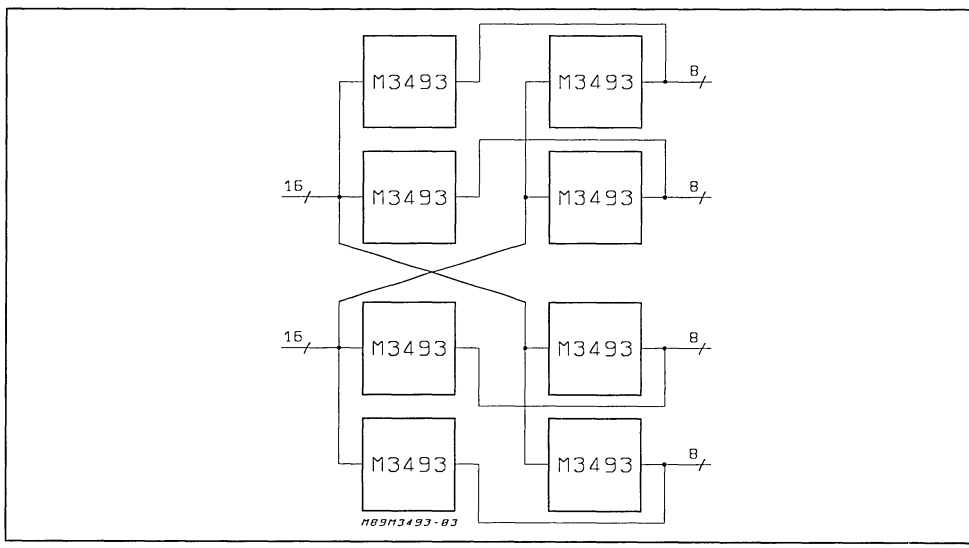
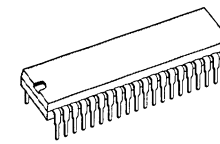


Figure 16 : (32 x 32 non blocking matrix).



CMOS 16 X 8 CROSSPOINT WITH CONTROL MEMORY

- LOW ON RESISTANCE (typ. 60 Ω at V_{DD} = 10 V)
- INTERNAL CONTROL LATCHES
- ANALOG SIGNAL SWING CAPABILITY EQUAL TO POWER SUPPLY VOLTAGE APPLIED
- LESS THAN 1 % TOTAL DISTORT. AT 0 dBm
- LESS THAN – 95 dB CROSS-TALK AT 1 KHz 1 V_{pp}
- VERY LOW POWER CONSUMPTION



DIP40

ORDERING NUMBER : M3494 B1

DESCRIPTION

The M3494 contains a 16 x 8 array of crosspoint together with a 7 to 128 line decoder and latch circuits. Anyone of the 128 switches can be addressed by selecting the appropriate 7 input bits. The selected switch can be turned on or off by applying a logical one or zero to the data in and the strobe input at logical one. A reset signal can be used to turn off all the switches together when is set at logical one.

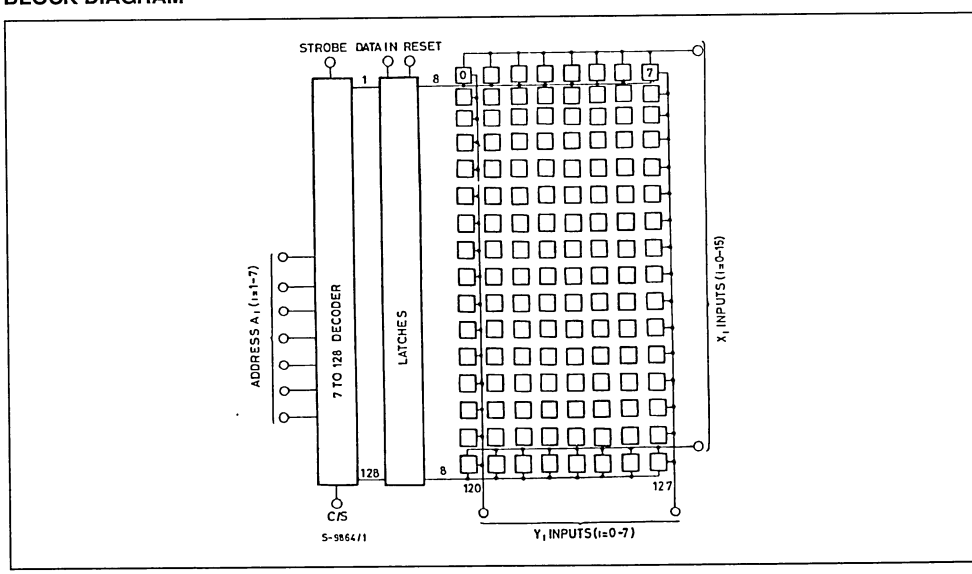
The input pin V_G shifts the logic level of the digital inputs. It allows one M3494 supplied between V_{BB} and V_{DD} to have input logic levels equal to V_G and V_{DD}.

M3494 can handle analog signals with an amplitude equal to the voltage power supply.

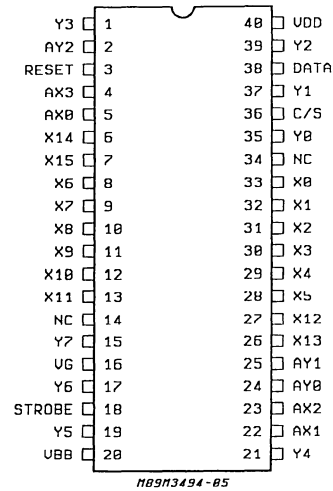
The C/S allows the control inputs of different devices to be connected in parallel in multiple chip system. Each device is selected when its own C/S input pin is high level.

M3494 is available in 40 lead dual in-line plastic.

BLOCK DIAGRAM



PIN CONNECTION (top view)



INPUT/OUTPUT DESCRIPTION

I/O	Symbol	Pin	Description
POWER			
I	V_{DD}	40	Positive Power Supply
I	V_{SS}	20	Negative Power Supply
I	V_G	16	Digital Signal Ground
ADDRESS			
I	AX0-AX3	4, 5, 22, 23	X Address Lines. These 4 pins are used to select one of the 16 rows of switches. Refer to the truth table for legal address.
I	AY0-AY2	2, 24, 25	Y Address Lines. These 3 pins are used to select one of the 8 columns of switches. Refer to the truth table for legal address.
CONTROL			
I	DATA	38	This input determines if the selected switch will be turned on (closed) or off (opened). If the pin is held high, the selected switch will be closed. If the pin is held low, the switch will be opened.
I	STROBE	18	This pin enables whatever action is selected by the ADDRESS and DATA pins. When the STROBE pin is held low, no switch openings or closings take place. When the STROBE pin is held high, the switch addressed by the select lines will be opened or closed (depending upon the state of the DATA pin)
I	RESET	3	Master Reset. This pin turns off (opens) all 128 switches. The states of the above control lines are irreleant. This pin is active high.
I	C/S	36	Chip Select. This pin allow the input control lines of different M3494's to be connected in parallel in multiple chip system. This pin is active high. Each device is selected by its own C/S input pin.
DATA			
I/O	X0-X11	6-13, 26-33	Analog Input/Outputs. These pins are connected to the Y0-Y7 pins in according to the truth table.
I/O	Y0-Y7	1,15,17,19,21 35,37,39	Analog Input/Outputs. These pins are connected to the X0-X15 pins in according to the truth table.

TRUTH TABLE

Address							Connections
AX0	AX1	AX2	AX3	AY0	AY1	AY2	
0	0	0	0	0	0	0	X0<0> -<0>Y0
1	0	0	0	0	0	0	X1<0> -<0>Y0
0	1	0	0	0	0	0	X2 <0>-<0>Y0
1	1	0	0	0	0	0	X3 <0>-<0>Y0
0	0	1	0	0	0	0	X4 <0>-<0>Y0
1	0	1	0	0	0	0	X5 <0>-<0>Y0
0	1	1	0	0	0	0	X12 -<0>Y0
1	1	1	0	0	0	0	X13 -<0>Y0
0	0	0	1	0	0	0	X6 <0>-<0>Y0
1	0	0	1	0	0	0	X7 <0>-<0>Y0
0	1	0	1	0	0	0	X8 <0>-<0>Y0
1	1	0	1	0	0	0	X9<0> -<0>Y0
0	0	1	1	0	0	0	X10 -<0>Y0
1	0	1	1	0	0	0	X11 -<0>Y0
0	1	1	1	0	0	0	X14 -<0>Y0
1	1	1	1	0	0	0	X15 -<0>Y0
0	0	0	0	1	0	0	X0 - Y1
↓	↓	↓	↓	↓	↓	↓	↓ <0> ↓
1	1	1	1	1	0	0	X15 - Y1
0	0	0	0	0	1	0	X0 - Y2
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	0	1	0	X15 - Y2
0	0	0	0	1	1	0	X0 - Y3
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	1	1	0	X15 - Y3
0	0	0	0	0	0	1	X0 - Y4
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	0	0	1	X15 - Y4
0	0	0	0	1	0	1	X0 - Y5
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	1	0	1	X15 - Y5
0	0	0	0	0	1	1	X0 - Y6
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	0	1	1	X15 - Y6
0	0	0	0	1	1	1	X0 - Y7
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	1	1	1	X15 - Y7

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (V_{BB} = 0)	– 0.5 to 14	V
V_{IN}	Input Voltage Range	V_G – 0.5 to V_{DD} + 0.5	V
P_{tot}	Power Dissipation	1	W
T_{op}	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	– 50 to 125	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD} V_{BB}	Supply Voltages	V_G = 0+ 5 ± 10 % – 5 ± 10 %	V V
T_{op}	Operating Temperature	0, + 70	°C
V_{IN}	(logic signal)	V_G, V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C, V_{DD} = +5V, V_G = 0V, V_{BB} = -5V unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_S	Supply Current	Reset = V_{DD}			1	mA
CROSSPOINT						
	On Resistance	V_{IDC} = 0.75V, V_{ODC} = 0.5V, See Figure 1		60	100	Ω
	On Resistance Variation			6	10	Ω
	Off-leakage *	All switches off V_{OS} = V_{IS} = V_{BB} to V_{DD}			± 3	µA
CONTROLS						
V_{IL}					0.8	V
V_{IH}			2.4			V
	Input Leakage *	V_{IN} = V_G to V_{DD}			± 3	µA

* The device is guaranteed with such limits up to 70°C. At 25°C these limits become ± 100nA

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_{amb} = 25°C, C_L = 50pF all input square wave rise and fall times = 10ns, V_{DD} = 10V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
CROSSPOINT							
t_{PHL}, t_{PLH}	Propagation Delay Time (switch on) Signal Input to Output	R_L = 1kΩ		30	100	ns	2
	Frequency Response (any switch on) 20 log (V_{OS}/V_{IS}) = -3dB	R_L = 91Ω, V_{IS} = 2V_{PP}, C_L = 3pF		50		MHz	
	Sine Wave Distortion	f_i = 1kHz, R_L = 0.6kΩ, V_{IS} = 8V_{PP}			1	%	
	Feedthrough (any switches off)	f_i = 10kHz, R_L = 1kΩ, V_{IS} = 2V_{PP}	-80			dB	3
	Frequency for Signal Crosstalk Attenuation of 40dB Attenuation of 110dB	V_{IS} = 1V_{PP}	 1 5			 MHz kHz	4
C	Capacitance Xn to V_{BB} Yn to V_{BB} Feedthrough	 f_i = 1MHz, V_{IS} = 0.1V_{PP}	 15		 15 0.4	pF	
C	Capacitance Logic Input to V_G	f_i = 1MHz, V_{IS} = 0.1V_{PP}	5			pF	
CONTROLS (t_r, t_f = 10ns) (V_{DD} = +5V, V_G = 0V, V_{BB} = -5V)							
t_{PSN}	Propagation Delay Time Strobe to Output (switch turn-on to high level)	R_L = 1kΩ, C_L = 50pF		150	200	ns	5
t_{PZH}	Data-in to Output (turn-on to high level)			150	200	ns	6
t_{PAN}	Address to Output (turn-on to high level)			150	200	ns	7
t_{PSF}	Propagation Delay Time Strobe to Output (switch turn-off)			150	200	ns	5
t_{PZL}	Data-in to Output (turn-on to low level)			150	200	ns	6
t_{PAF}	Address to Output (turn-off)			150	200	ns	7
t_S	Set-up Time Data-in to Strobe or C/S		40			ns	5 10
t_H	Hold Time Data-in to Strobe or C/S		120			ns	5 10
t_O	Switching Frequency			1		MHz	
t_W	Strobe Pulse Width C/S Pulse Width		100			ns	10
t_{WR}	Reset Pulse Width		150			ns	9
t_{PHZ}	Reset Turn-off to Output Delay			150	200	ns	9
t_{AS}	Address Set-up Time Address to Strobe or C/S		120			ns	10
t_{AH}	Address Hold Time Address to Strobe or C/S		120			ns	10
	Control Crosstalk Data-in, Address or Strobe to Output	Square wave input, V_{IN} = 3V, R_L = 10kΩ		75		mV	8

TEST CIRCUITS

Figure 1 : RON Measurement.

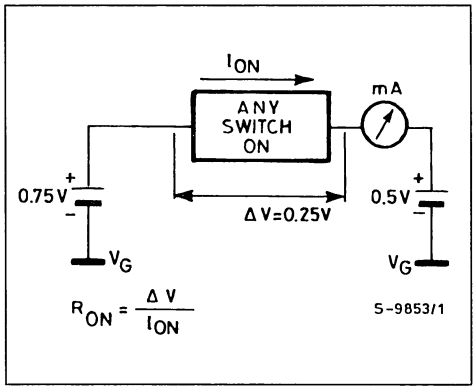


Figure 2 : Propagation Delay Time and Waveforms (signal input to signal output switch ON).

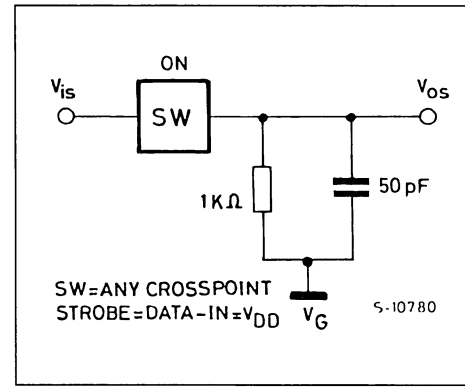
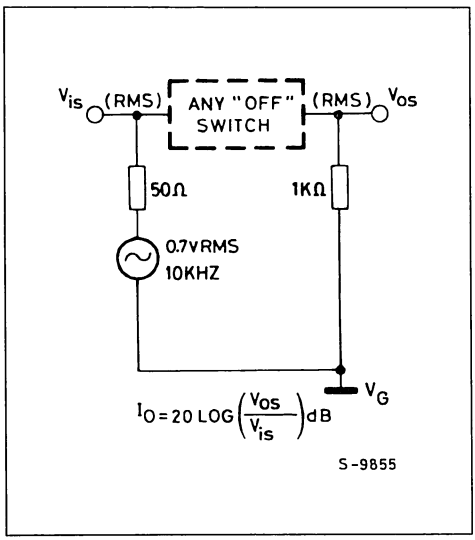


Figure 3 : Off Isolation Measurement (Feed through).



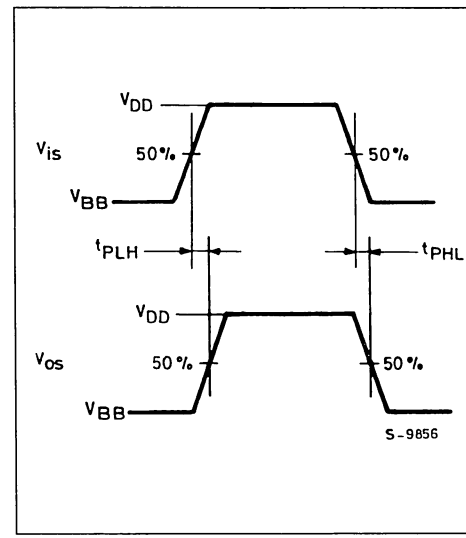


Figure 4 : Crosstalk Measurements.

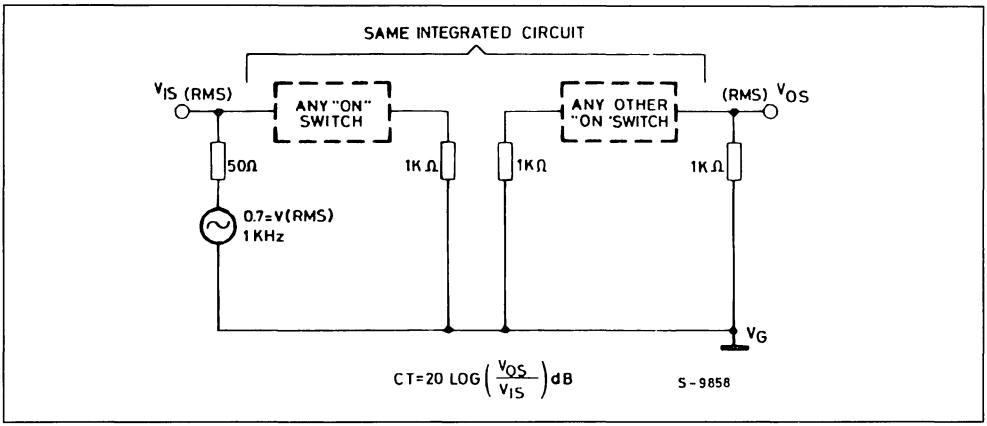


Figure 5 : Propagation Delay Time and Waveforms (strobe to signal output switch Turn-ON or Turn-OFF).

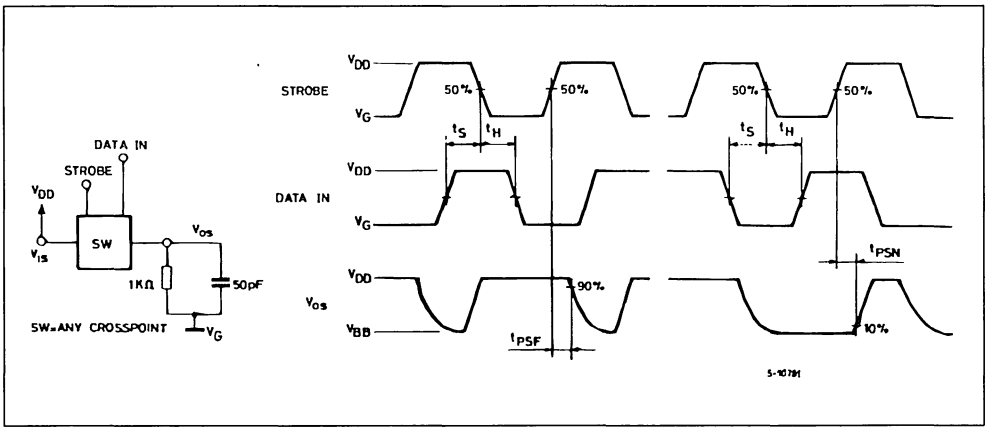


Figure 6 : Propagation Delay Time and Waveforms (data-in signal output, switch Turn-ON to high or low level).

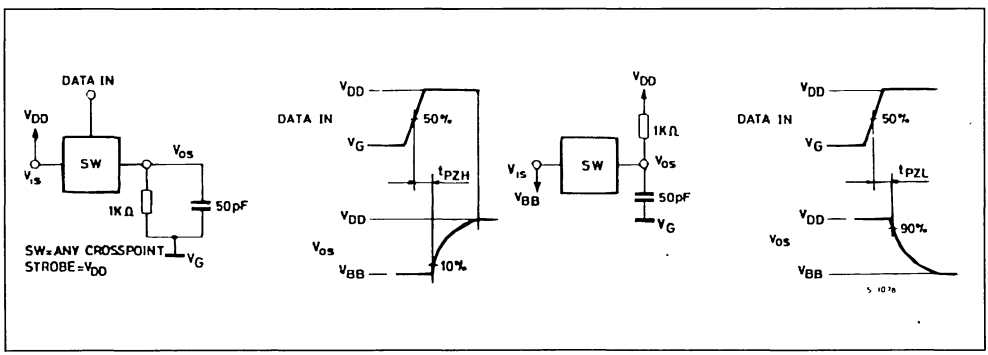


Figure 7 : Propagation Delay Time and Waveforms (address to signal output switch Turn-ON or Turn-OFF).

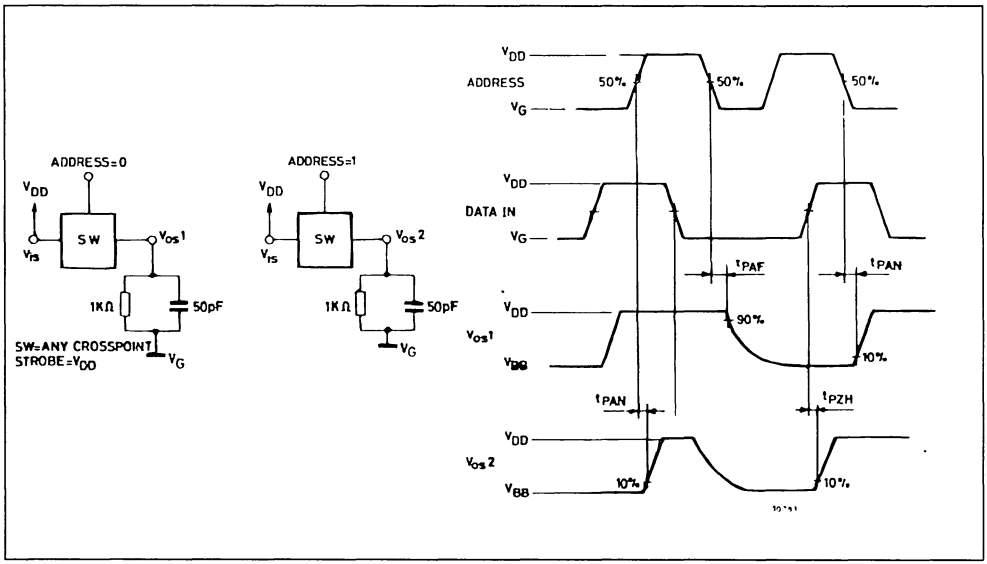


Figure 8 : Waveforms for Crosstalk (control input to signal output).

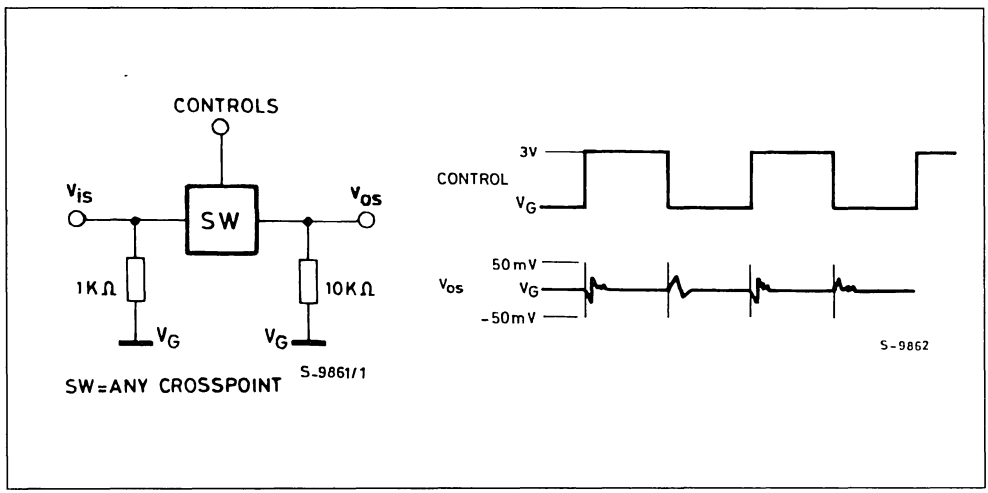


Figure 9 : Propagation Delay Time and Waveforms (reset to output delay).

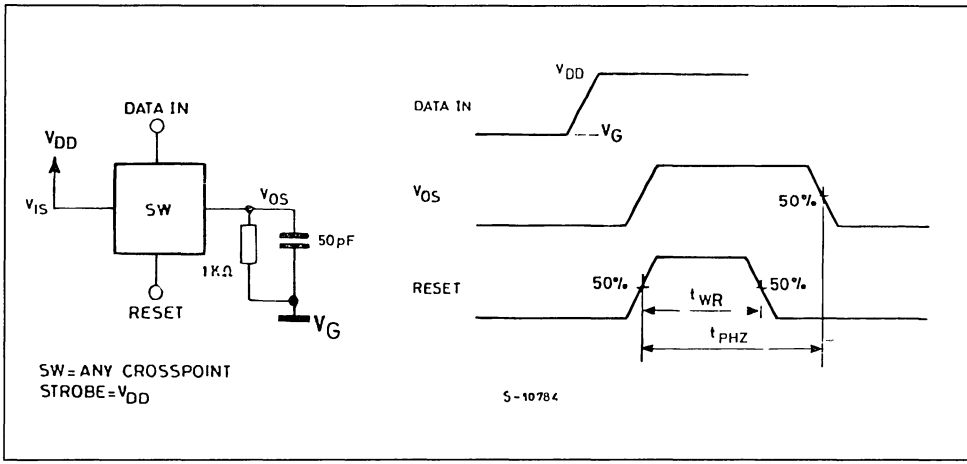


Figure 10 : Propagation Delay Time and Waveforms (Strobe and C/S to signal output switch).

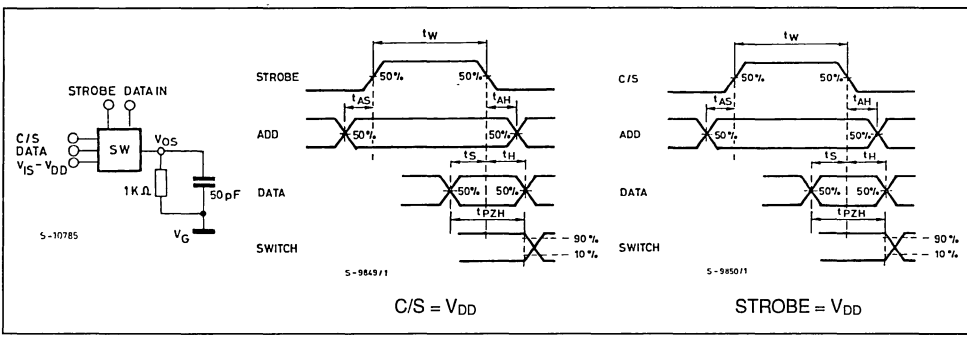


Figure 11 : Typical R_{ON} versus V_{is}.

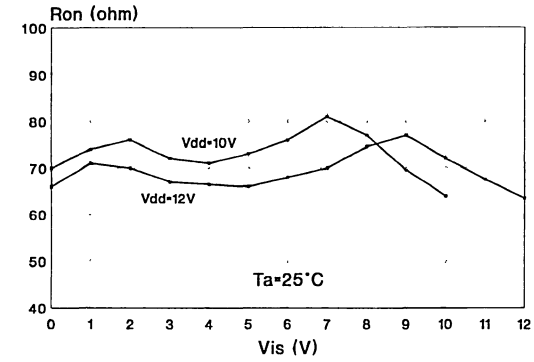


Figure 12 : Peak to Peak Voltage Capability versus Total Harmonic Distortion.

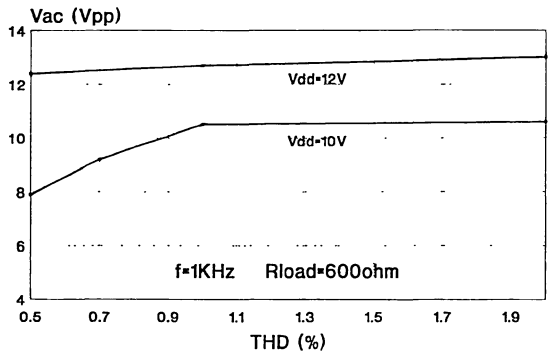
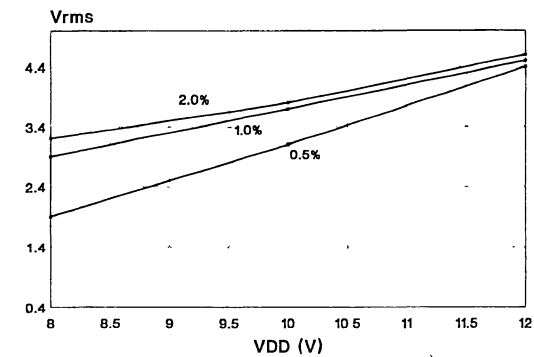


Figure 13 : V_{RMS} Capability versus V_{DD}.



TYPICAL APPLICATIONS

The figures 14, 15 and 16 show the system configuration for expanded matrices (16 x 16, 8 x 64, 32 x 32).

Figure 14 : (16 x 16 non blocking matrix).

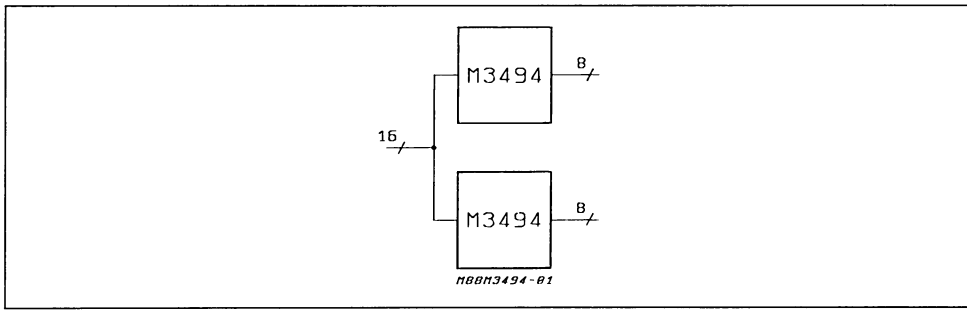


Figure 15 : (8 x 64 matrix).

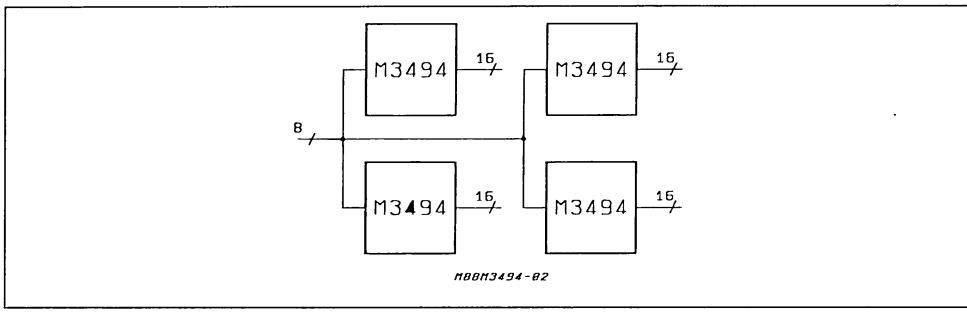
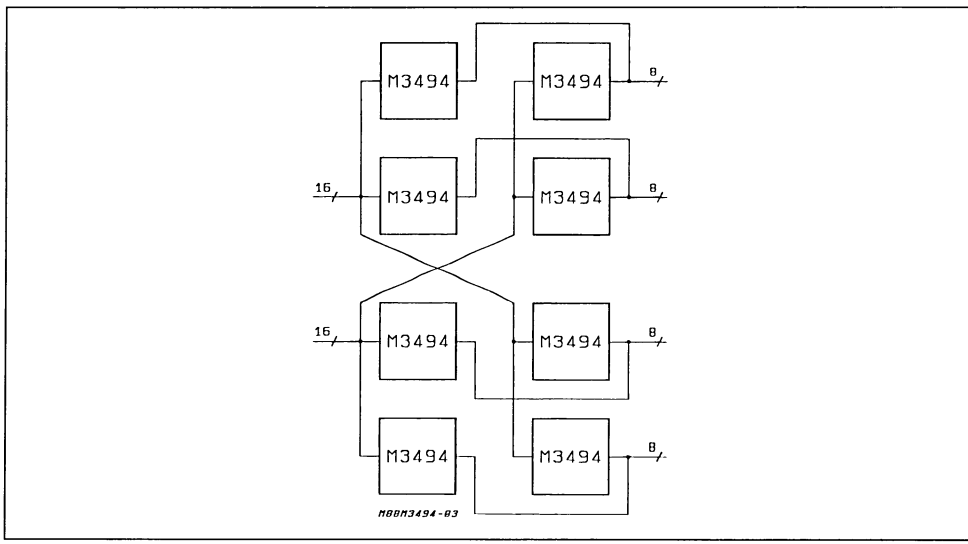


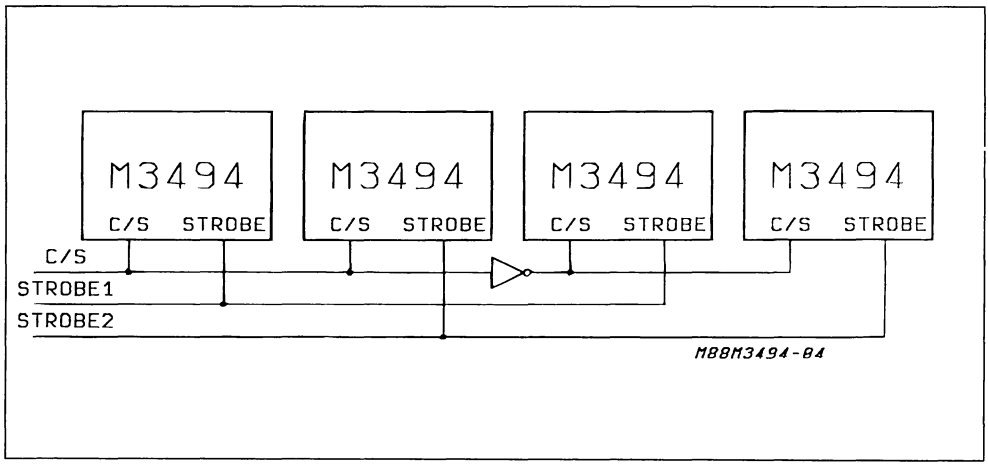
Figure 16 : (32 x 32 non blocking matrix).



The availability of the C/S input in addition of the STROBE input aids the addressing circuit for expanded matrices.

Fig. 17 shows an example, the selection circuit for a matrix with 4 x M3494 that implement this function with only one extenal inverter.

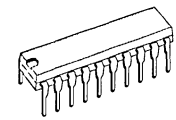
Figure 17.



Note : The Reset, Data and Address inputs are connected in parallel.

COMBINED SINGLE CHIP PCM CODEC AND FILTER

- SYNCHRONOUS CLOCKS ONLY
- AT&T D3/D4 AND CCITT COMPATIBLE
- TWO TIMING MODES:
  FIXED DATA RATE MODE 1.536MHz, 1.544MHz, 2.048MHz
  VARIABLE DATA MODE: 64KHz - 4.096MHz
- PIN SELECTABLE μ-LAW OR A-LAW OPERATION
- NO EXTERNAL COMPONENTS FOR SAMPLE-AND-HOLD AND AUTO ZERO FUNCTIONS
- LOW POWER DISSIPATION:
  0.5mW POWER DOWN
  70mW OPERATING
- EXCELLENT POWER SUPPLY REJECTION



DIP 20
ORDERING NUMBER: M5913B1

DESCRIPTION

The M5913 is fully integrated PCM (pulse code modulation) codecs and transmit/receive filter using CMOS silicon gate technology.

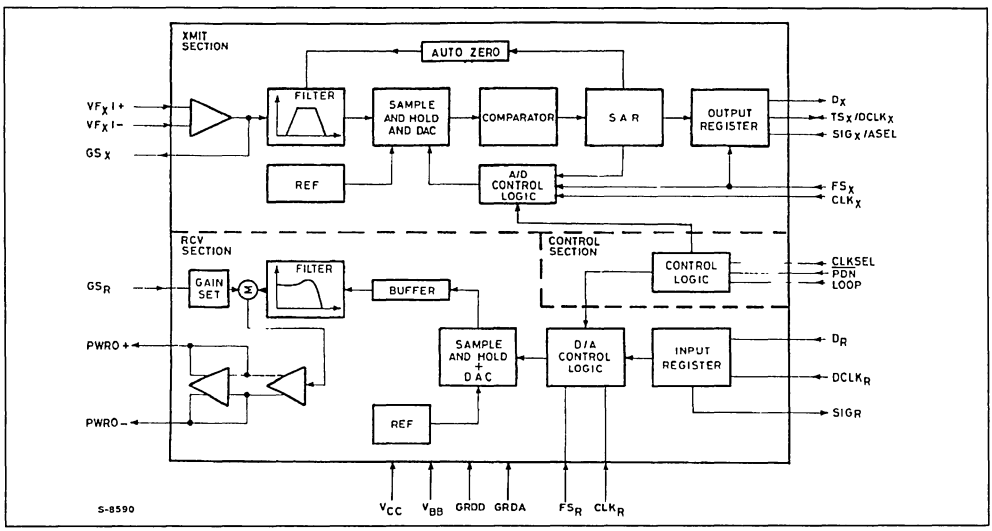
The primary applications for the M5913 are telephone systems :

- Switching - M5913-Digital PBX's and Central Office Switching Systems
- Concentration - M5913 Subscriber Carrier and Concentrators.

The wide dynamic range (78dB) and the minimal conversion time make it ideal products for other applications such as:

- Voice Store and Forward
- Secure Communications Systems
- Digital Echo Cancellers
- Satellite Earth Stations.

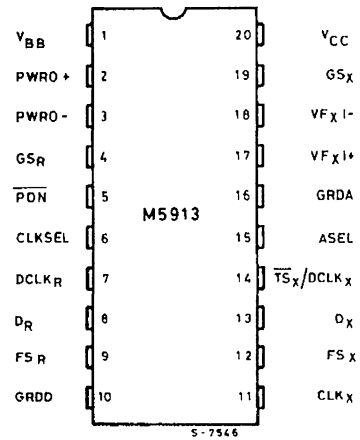
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	With Respect GRDD, GRDA = 0V	– 0.6 to 7	V
V_{BB}	With Respect GRDD, GRDA = 0V	- 0.6 to – 7	V
GRDD, GRDA	In Such Case : $0 \leq V_{CC} \leq +7V$, $-7V \leq V_{BB} \leq 0V$	± 0.3	V
$V_{I/O}$	Analog Inputs, Analog Outputs and Digital Inputs	$VBB - 0.3 \leq V_{IN}/V_{OUT} \leq V_{CC} + 0.3$	V
$V_{O\,DIG}$	Digital Outputs	$GRDD - 0.3 \leq V_{OUT} \leq V_{CC} + 0.3$	V
P_{tot}	Total Power Dissipation	1	W
T_{stg}	Storage Temperature Range	-65 to 150	°C

PIN CONNECTION (Top view)



PIN NAMES

Symbol	Parameter	Symbol	Parameter
V_{BB}	Power (-5V)	GS_X	Gain Control
PWRO+, PWRO-	Power Amplifier Outputs	VF_XI-, VF_XI+	Analog Inputs
GS_R	Gain Setting Input for receive Channel	GRDA	Analog Ground
$\overline{PDN}$	Power Pown Select	$\overline{NC}$	No Connected
CLKSEL	Master Clock Select	SIG_X	Transmit Digital Signaling Input
LOOP	Analog Loop Back	ASEL	μ or A-law Select
SIG_R	Signaling Bit Output	TS_X	Digital Output - Timeslot Strobe
$DCLK_R$	Receive Data Rate Clock	$DCLK_X$	Transmit Data Rate Clock
D_R	Receive Channel Input	D_X	Transmit (Digital) Output
FS_R	Receive Frame Synchronization Clock	FS_X	Transmit Frame Synchronization Clock
GRDD	Digital Ground	CLK_X	Transmit Master Clock
V_{CC}	Power (+5V)	CLK_R	Receive Master Clock

PIN DESCRIPTION

Symbol	Function
V_{BB}	Most Negative Supply. Input voltage is -5 volts ±5%.
PWRO+	Non-inverting Output of Power Amplifier. Can drive transformer hybrids or high impedance loads directly in either a differential or single ended configuration.
PWRO -	Inverting Output of Power Amplifier. Functionally identical and complementary to PWRO+.
GS_R	Input to the gain Setting Network on the Output Power Amplifier, Transmission level can be adjusted over a 12dB range depending on the voltage at GS_R.
$\overline{PDN}$	Power Down Select. When PDN is TTL high, the device is active.When low, the device is powered down.
CLKSEL	input which must be pinstrapped to reflect the master clock frequency at CLK_X, CLK_R. CLKSEL = V_{BB} 2.048MHz CLKSEL = GRDD 1.544MHz CLKSEL = V_{CC} 1.536MHz
LOOP	Analog Loopback. When this pin is TTL high, the receive output (PWRO+) is internally connected to VF_XI+, GS_R is internally connected to PWRO-, and VF_XI- is internally connected to GS_X. A 0dBm0 digital signal input at D_R is returned as a +3dBm0 digital signal output at D_X.
SIG_R	Signalling Bit Output, Receive Channel. In fixed data rate mode. SIG_R outputs the logical state of the eighth bit of the PCM word in the most recent signaling frame.
$DCLK_R$	Selects the fixed or variable data rate mode. When DCLKR is connected to V_{BB}, the fixed data rate mode is selected. When $DCLK_R$ is not connected to V_{BB}, the device operates in the variable data rate mode. In this mode $DCLK_R$ becomes the receive data clock wich operates at TTL levels from 64kB to 4.096MB data rates
D_R	Receive PCM Input. PCM data is clocked in on this lead on eight consecutive negative transitions of the receive data clock: CLKR in the fixed data rate mode and $DCLK_R$ in variable data rate mode.
FS_R	8kHz frame synchronization clock input/timeslot enable, receive channel. A multifunction input which in fixed data rate mode distinguishes between signaling and non-signaling frames by means of a double or single wide pulse respectively. In variable data rate mode this signal must remain high for the entire length of the timeslot. The receive channel enters the standby state whenever FSR is TTL low for 30 miliseconds
GRDD	Digital Ground for all Internal Logic Circuits. Not internally tied to GRDA.
CLK_R	Receive master and data clock for the fixed data rate mode; receive master clock only in variable data rate mode.
CLK_X	Transmit master and data clock for the fixed data rate mode; transmit master clock only in variable data rate mode.
FS_X	8kHz frame synchronization clock input/timeslot enable, transmit channel. Operates independently but in an analogous manner to FSR. The transmit channel enters the standby state whenever FS_X is TTL low for 30 milliseconds.
D_X	Transmit PCM Output. PCM data is clocked out on this lead on eight consecutive positive transitions of the transmit data clock : CLK in fixed data rate mode and $DCLK_X$ in variable data rate mode.
$\overline{TS_X}/DCLK_X$	Transmit channel timeslot strobe (output) or data clock (input) for the transmit channel. In fixed data rate mode, this pin becomes the transmit data clock which operates at TTL levels from 64kB to 4.096MB data rates.
SIG_X/ASEL	A dual purpose selects μ-law and pin. When connected to V_{BB}. A law operation is selected. When it is not connected to V_{BB} pin is a TTL level input for signaling operation. This input is transmitted as the eighth bit of the PCM word during signaling frames on the D_X lead.
NC	Not Connected.
GRDA	Analog ground return for all internal voice circuits. Not internally connected to GRDD.
VF_XI+	Non inverting analog input to uncommitted transmit operational amplifier.
VF_XI-	Inverting analog input to uncommitted transmit operational amplifier.
GS_X	Output terminal of on-chip uncommitted op amp. Internally, this is the voice signal input to the transmit filter.
V_{CC}	Most positive supply ; input voltage is + 5 volts ±5%

FUNCTIONAL DESCRIPTION

The M5913 provides the analog-to-digital and the digital-to-analog conversion and the transmit and receive filtering necessary to interface a full duplex (4 wires) voice telephone circuit with the PCM highway of a time division multiplexed (TDM) system. It is intended to be used at the analog termination of a PCM line.

The following major functions are provided :

- Bandpass filtering of the analog signals prior to encoding and after decoding
- Encoding and decoding of voice and call progress information
- Encoding and decoding of the signaling and supervision information

GENERAL OPERATION

System Reliability Features

The combo-chip can be powered up by pulsing FS_X and/or FS_R while a TTL high voltage is applied to $\overline{PDN}$, provided that all clocks and supplies are connected. The M5913 has internal resets on power up (or when V_{BB} or V_{CC} are re-applied) in order to ensure validity of the digital outputs and thereby maintain integrity of the PCM highway.

On the transmit channel, digital outputs D_X and $\overline{TS}_X$ are held in a high impedance state for approximately four frames (500µs) after power up or application of V_{BB} or V_{CC}. After this delay, D_X and $\overline{TS}_X$ will be functional and will occur in the proper timeslot. The analog circuits on the transmit side require approximately 40 milliseconds to reach their equilibrium value due to the autozero circuit setting time. Thus, valid digital information, such as for on/off hook detection, is available almost immediately, while analog information is available after some delay.

On the receive channel, the digital output SIG_R is also held low for a maximum of four frames after power up or application of V_{BB} or V_{CC}, SIG_R will remain low thereafter until it is updated by a signaling frame.

To further enhance system reliability, $\overline{TS}_X$ and $\overline{D_X}$ will be placed in a high impedance state approximately 20µs after an interruption of CLK_X. Similarly SIG_R will be held low approximately 20µs after an interruption of CLK_R. These interruptions could possibly occur with some kind of fault condition.

Power Down And Standby Modes

To minimize power consumption, two power down modes are provided in which most M5913 functions are disabled. Only the power down, clock, and frame sync buffers, which are required to power up the device, are enabled in these modes. As shown in table 1, the digital outputs on the appropriate channels are placed in a high impedance state until the device returns to the active mode.

The Power Down mode utilizes an external control signal to the $\overline{PDN}$ pin. In this mode, power consumption is reduced to an average of 0.5mW. The device is active when the signal is high and inactive when it is low. In the absence of any signal, the $\overline{PDN}$ pin floats to TTL high allowing the device to remain active continuously.

The Standby mode leaves the user an option of powering either channel down separately or powering the entire down by selectively removing FS_X and/or FS_R. With both channels in the standby state, power consumption is reduced to an average of 1mW. If transmit only operation is desired, FS_X should be applied to the device while FS_R is held low. Similarly, if receive only operation is desired, FS_R should be applied while FS_X is held low.

Fixed Data Rate Mode

Fixed data rate timing, is selected by connecting $DCLK_R$ to V_{BB}. It employs master clock CLK_X, and CLK_R, frame synchronization clocks FS_X and FS_R, and output $\overline{TS}_X$.

CLK_X, and CLK_R, serve both as the master clock to operate the codec and filter sections and bit clocks to clock the data in and out from the PCM highway. FS_X and FS_R are 8kHz inputs which set the sampling frequency and distinguish between signaling and non-signaling frames by thir pulse width. A frame synchronization pulse which is one master clock wide designates a non-signaling frame, while a double wide sync pulse enables

Table 1: Power Down Methods

Device Status	Power Down Methods	Digital Outputs Status
Power Down Mode	$\overline{PDN}$ = TTL low	$\overline{TS}_X$ and D_X are placed in a high impedance state and SIG_R is placed in a TTL low state within 10µs.
Stand-by Mode	FS_X and FS_R are TTL low	$\overline{TS}_X$ and D_X are placed in a high impedance state and SIG_R is placed in a TTL low state 30ms after FS_X and FS_R are removed.
Only transmit is on stand-by	FS_X is TTL low	$\overline{TS}_X$ and D_X are placed in a high impedance state within 30ms.
Only receive is on stand-by	FS_R is TTL low	SIG_R is placed in a TTL low state within 30ms.

the signaling function. TS_X is a timeslot strobe/buffer enable output which gates the PCM word onto the PCM highway when an external buffer is used to drive the line.

Data is transmitted on the highway at D_X on the first eight positive transitions of CLK_X following the rising edge of FS_X. Similarly, on the receive side, data is received on the first eight falling edges of CLK_R. The frequency of CLK_X and CLK_R is selected by the CLKSEL pin to be either 1.536, 1.544 or 2.048MHz. No other frequency of operation is allowed in the fixed data rate mode.

Variable Data Rate Mode

Variable data rate timing is selected by connecting $DCLK_R$ to the bit clock for the receive PCM highway rather than to V_{BB}. It employes master clocks CLK_X and CLK_R, bit clocks $DCLK_R$ and $DCLK_X$ and frame synchronization clocks FS_R and FS_X.

Variable data rate timing allows for a flexible data frequency. It provides the ability to vary the frequency of the bit clocks, from 64kHz to 4096MHz. Master clocks inputs are still restricted to 1.536, 1.544, or 2.048MHz.

In this mode, $DCLK_R$ and $DCLK_X$ become the data clocks for the receive and transmit PCM highways. While FS_X is high, PCM data from D_X is transmitted onto the highway on the next eight consecutive positive transitions of $DCLK_X$. Similarly, while FS_R is high, each PCM bit from the highway is received by D_R on the next eight consecutive negative transitions of $DCLK_R$.

On the transmit side, the PCM word will be repeated in all remaining timeslots in the 125µs frame as long as $DCLK_X$ is pulsed and FS_X is held high. This feature allows the PCM word to be transmitted to the PCM highway more than once per frame, if desired, and is only available in the variable data rate mode. Conversely, signaling is only allowed in the fixed data rate mode since the variable mode provides no means with which to specify a signaling frame.

Precision Voltage References

No external components are required with the combochip to provide the voltage reference function. Voltage references are generated on-chip and are calibrated during the manufacturing process. The technique use the bandgap principle to derive a temperature and bias stable reference voltage. These references determine the gain and dynamic range characteristics of the device.

Separate references are supplied to the transmit and receive sections. Transmit and receive section are trimmed independently in the filter stages to a final precision value. With this method the combochip can achieve manufacturing tolerances of typically ± 0.04dB in absolute gain for each half channel, providing the user a significant margin for error in other board components.

Conversion Laws

The M5913 is designed to operate in both µ-law and A-law systems. The user can select either conversion law according to the voltage present on the SIG_X/ASEL pin . In each case the coder and decoder process a companded 8-bit PCM word following CCITT recommandation G.711 for µ-law and A-law conversion. If A-law operation is desired, SIG_X should be tied to V_{BB}. Thus, signaling is not allowed during A-law operation. If µ = 255-law operation is selected, then SIG_X is a TTL level input which modifies the LSB on the PCM output in signaling frames

TRANSMIT OPERATION

Transmit Filter

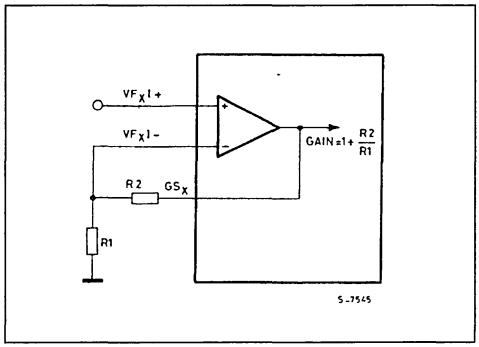
The input section provides gain adjustment in the passband by means of an on-chip uncommitted operational amplifier. This operational amplifier has a common mode range of 2.17V, a maximum DC offset of 25mV, a minimum voltage gain of 5000, and a unity gain bandwidth of typically 1MHz. Gain of up to 20dB can be set without degrading the performance of the filter. The load impedance to ground (GRDA) at the amplifier output (GS_X) must be greater than 10kΩ in parallel high less than 50pF. The input signal on lead VF_XI+ can be either AC or DC coupled. The input op amp can also be used in the inverting mode or differential amplifier mode (see figure 3).

A low pass anti-aliasing section is included on-chip. This section typically provides 35dB attenuation at the sampling frequency. No external components are required to provide the necessary anti-aliasing function for the switched capacitor section of the transmit filter.

The passband section provides flatness and stopband attenuation which fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.712.
The M5913 specifications meet or exceed digital class 5 central office switching systems requirements. The transmit filter transfer characteristics and specifications will be within the limits shown the relative table.

A high pass section configuration was chosen to reject low frequency noise from 50 and 60Hz power lines, 17Hz European electric railroads, ringing frequencies and their harmonics, and other low frequency noise.
Even though there is high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200Hz. This feature allows the use of low-cost transformer hybrids without external components.

Figure 3: Transmit Filter Gain Adjustment.



Encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample and hold capacitor.
The encoder then performs an analog to digital conversion on a switched capacitor array. Digital data representing the sample is transmitted on the first eight data clock bits of the next frame.

An on-chip autozero circuit corrects for DC-offset on the input signal to the encoder. This autozero circuit uses the sign bit averaging technique. In this way, all DC offset is removed from the encoder input waveform.

RECEIVE OPERATION

Decoding

The PCM word at the D_R lead is serially fetched on the first eight data clock bits of the frame.
A D/A conversion is performed on the digital word and the corresponding analog sample is held on an internal sample and hold capacitor. This sample is then transferred to the receive filter.

Receive Filter

The receive section of the filter provides passband flatness and stopband rejection which fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin X)/X response of such decoders. The receive filter characteristics and specifications are shown in the relative table.

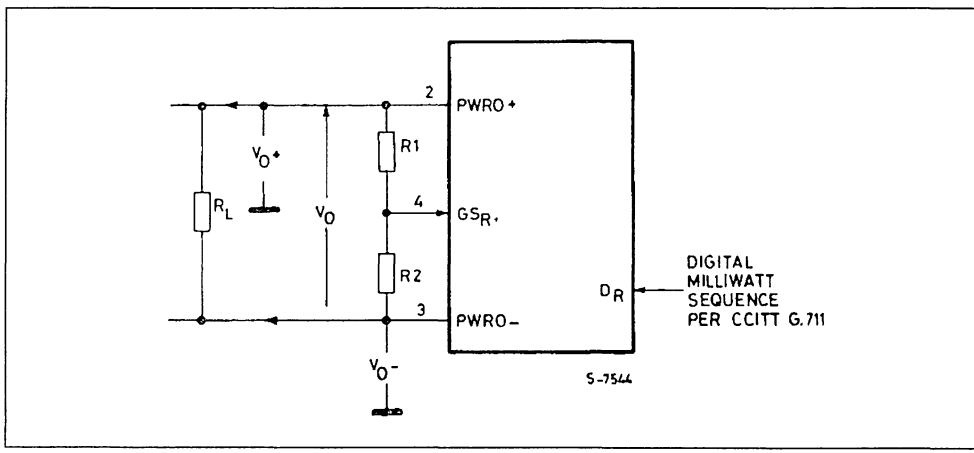
Receive Output Power Amplifiers

A balanced output amplifier is provided in order to allow maximum flexibility in output configuration. Either of the two outputs can be used single ended (referenced to GRDA) to drive single ended loads. Alternatively, the differential output will drive a bridged load directly. The output stage is capable of driving loads as low as 300 ohms single ended to a level of 12dBm or 600 ohms differentially to a level of 15dBm.

The receive channel transmission level may be adjusted between specified limits by manipulation of the GS_R input. GS_R is internally connected to an analog gain setting network. When GS_R is strapped to PWRO–, the receive level is minimized; when it is tied to PWRO+, the level is minimized. The output transmission level interpolates between 0 and -12dB as GSR is interpolated (with potentiometer) between PWRO- and PWRO+. The use of the output gain set is illustrated in figure 4.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions, that is, when the digital input at D_R is the eight-code sequence specified in CCITT recommendation G.711.

Figure 4: Gain Setting Configuration.



OUTPUT GAIN SET: DESIGN CONSIDERATIONS (refer to figure 4)

PWRO+ and PWRO– are low impedance complementary outputs. The voltages at the nodes are:

V_O at PWRO+

V_O at PWRO

$V_O = V_{O+} V_{O-}$ (total differential response)

R1 and R2 are a gain setting resistor network with the center tap connected to the GS_R input. A value greater than 10KΩ and less than 100KΩ for R1 + R2 is recommended because:

a) The parallel combination of R1 + R2 and RL sets the total loading.

b) The total capacitance at the GS_R input and the parallel combination of R1 and R2 define a time constant which has to be minimized to avoid inaccuracies.

If VA represents the output voltage without any gain setting network connected, you can have:

$$V_O = AV_A$$

$$\text{where } A = \frac{1 + (R_1 / R_2)}{4 + (R_1 / R_2)}$$

For design purposes, a useful form is R1/R2 as a function of A.

$$R1 / R2 = \frac{4A - 1}{1 - A}$$

(allowable values for A are those which make R1/R2 positive)

Examples are:

If A = 1 (maximum output), then
R1/R2 = ∞ or $V(GS_R) = V_O$;
i.e., GS_R is tied to PWRO+

If A = 1/2. then
R1/R2 = 2

If A = 1/4 (minimum output) then
R1/R2 = 0 or $V(GS_R) = V_{O+}$;
i.e., GSR is tied to PWRO+

DC CHARACTERISTICS (T_{amb} = 0 to 70°C, V_{CC} = +5V ± 5%, V_{BB} = – 5V ± 5%, GRDA = 0V,unless otherwise specified) Typical values are for T_{amb} = 25°C and nominal power supply values.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DIGITAL INTERFACE						
I_{IL}	Low Level Input Current	GRDD ≤ V_{IN} ≤ V_{IL} (note 1)			10	µA
I_{IH}	High Level Input Current	V_{IH} ≤ V_{IN} ≤ V_{CC}			10	µA
V_{IL}	Input Low Voltage, Except CLKSEL				0.8	V
V_{IH}	Input High Voltage, Except CLKSEL		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 3.2mA at D_X, $\overline{TS_X}$ and SIG_R			0.4	V
V_{OH}	Output High Voltage	I_{OH} = 9.6mA at D_X I_{OH} = 1.2mA at SIG_R	2.4			V
V_{ILO}	Input Low Voltage, CLKSEL (note 2)		V_{BB}		V_{BB} + 0.5	V
V_{IIO}	Input Intermediate Voltage, CLKSEL		GRDD -0.5		0.5	V
V_{IHO}	Input High Voltage, CLKSEL		V_{CC} - 0.5		VCC	V
C_{OX}	Digital Output Capacitance (note 3)			5		pF
C_{IN}	Digital Input Capacitance			5	10	pF

Notes:

1. V_{IN} is the voltage on any digital pin.

2. SIG_X and $DCLK_R$ are TTL level inputs between GRDD and V_{CC}; they are also pinstraps for mode selection when tied to V_{BB}. Under these conditions V_{ILO} is the input low voltage requirement.

3. Timing parameters are guaranteed based on a 100pF load capacitance. Up to eight digital outputs may be connected to a common PCM highway without buffering, assuming a board capacitance of 60pF.

DC CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max	Unit
POWER DISSIPATION All measurements made at f_{DCLK} = 2.048MHz, outputs unloaded						
I_{CC1}	V_{CC} Operating Current			6	10	mA
I_{BB1}	V_{BB} Operating Current			6	9	mA
I_{CC0}	V_{CC} Power Down Current	PDN ≤ V_{IL} ; after 10µs		40	300	µA
I_{BB0}	V_{BB} Power Down Current	PDN ≤ V_{IL} ; after 10µs		40	300	µA
I_{CCS}	V_{CC} Standby Current	FS_X, FS_R ≤ V_{IL} ; after 30ms		300	600	µA
I_{BBS}	V_{BB} Standby Current	FS_X, FS_R ≤ V_{IL} ; after 30ms		40	300	µA
P_{D1}	Operating Power Dissipation			60	100	mW
P_{D0}	Power Down Dissipation	PDN ≤ V_{IL} ; after 10µs		0.4	3	mW
P_{ST}	Standby Power Dissipation	FSX, FS_R ≤ V_{IL} ; after 30ms		1.7	5	mW
ANALOG INTERFACE, RECEIVE FILTER DRIVER AMPLIFIER STAGE						
I_{BX1}	Input Leakage Current, VF_XI+, VF_XI-	-2.17V ≤ V_{IN} ≤ 2.17V			100	nA
R_{IXI}	Input Resistance, VF_XI+, VF_XI-		10			MΩ
V_{OSXI}	Input Offset Voltage, VF_XI+, VF_XI-				25	mV
CMRR	Common Mode Rejection, VF_XI+, VF_XI-	-2.17V ≤ V_{IN} ≤ 2.17V	55			dB
A_{VOL}	DC Open Loop Voltage Gain, GS_X	R_L = 10K	5000	20.000		
f_C	Open Loop Unity Gain Bandwidth, GS_X			1		MHz
V_{OXI}	Output Voltage Swing GS_X	R_L ≥ 10kΩ	– 2.17		2.17	V
C_{LXI}	Load Capacitance, GS_X				50	pF
R_{LXI}	Minimum Load Resistance, GS_X		10			kΩ
ANALOG INTERFACE, RECEIVE FILTER DRIVER AMPLIFIER STAGE						
R_{ORA}	Output Resistance, PWRO+, PWRO-			1		Ω
V_{OSRA}	Single-ended Output DC Offset, PWRO+, PWRO-	Relative to GRDA	-150	75	150	mV
C_{LRA}	Load Capacitance, PWRO+, PWRO-				100	pF

AC CHARACTERISTICS - TRANSMISSION PARAMETERS

Unless otherwie noted, the analog input is a 0dBm0, 1020Hz sine wave[1]. Input amplifier is set for unity gain, noninverting. The digital inputs is a PCM bit stream generated by passing a 0dBm0, 1020Hz sine wave through an ideal encoder. Receive output is measured single ended, maximum gain configuration[2]. All output levels are (sin X)/X corrected.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
GAIN AND DYNAMIC RANGE						
EmW	Encoder Milliwatt Response (transmit gain tolerance)	T_{amb} = 25°C, V_{BB} = – 5V, V_{CC} = + 5V	-0.15	± 0.04	+0.15	dBm0
EmW_{TS}	EmW Variation with Temperature and Supplies	± 5% Supplies, 0 to 70°C Relative to Nominal Conditions	-0.12		+0.12	dB
DmW	Digital Milliwatt Response (receive gain tolerance)	T_{amb} = 25°C ; V_{BB} = – 5V, V_{CC} = + 5V	-0.15	± 0.04	+0.15	dBm0
DmW_{TS}	DmW Variation with Temperature and Supplies	± 5%, 0 to 70°C	-0.08		+0.08	dB
$0TLP_{1X}$	Zero Transmission Level Point Transmit Channel (0dBm0) µ-law	Referenced to 600Ω Referenced to 900Ω		+ 2.76 + 1.00		dBm dBm
$0TLP_{2X}$	Zero Transmission Level Point Transmit Channel (0dBm0) A-law	Referenced to 600Ω Referenced to 900Ω		+ 2.79 + 1.03		dBm dBm
$0TLP_{1R}$	Zero Receive Level Point Receive Channel (0dBm0) µ-law	Referenced to 600Ω Referenced to 900Ω		+ 5.76 + 4.00		dBm dBm
$0TLP_{2R}$	Zero Transmission Level Point Transmit Channel (0dBm0)) A-law	Referenced to 600Ω Referenced to 900Ω		+ 5.79 + 4.03		dBm dBm

AC CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
GAIN TRACKING Reference Level = – 10dBm0						
$GT1_X$	Transmit Gain Tracking Error Sinusoidal Input; μ-law	+ 3 to – 40dBm0 – 40 to – 50dBm0 – 50 to – 55dBm0			± 0.2 ± 0.4 ± 1.0	dB dB dB
$GT2_X$	Transmit Gain Tracking Error Sinusoidal Input; A-law	+ 3 to – 40dBm0 – 40 to – 50dBm0 – 50 to – 55dBm0			± 0.2 ± 0.4 ± 1.0	dB dB dB
$GT1_R$	Receive Gain Tracking Error Sinusoidal Input; μ-law	+ 3 to – 40dBm0 – 40 to – 50dBm0 – 50 to – 55dBm0			± 0.2 ± 0.4 ± 1.0	dB dB dB
$GT2_R$	Receive Gain Tracking Error Sinusoidal Input; A-law	+ 3 to – 40dBm0 – 40 to – 50dBm0 – 50 to – 55dBm0			± 0.2 ± 0.4 ± 1.0	dB dB dB
NOISE						
N_{XC1}	Transmit Noise, C-message Weighted	VF_XI+ = GRDA, VF_XI- = GS_X		0	13	dBrnc0
N_{XC2}	Transmit Noise, C-message Weighted with Eighth Bit Signaling	VF_XI+ = GRDA, VF_XI- = GS_X 6 th Frame Signaling		13	18	dBrnc0
N_{XP}	Transmit Noise, Psophometrically Weighted	VF_XI+ = GRDA, VF_XI- = GS_X		(note 3)	– 80	dBrnc0
N_{RC1}	Receive Noise, C-message Weighted: Quiet Code	D_R = 11111111 Measure at PWRO+		1	9	dBrnc0
N_{RC2}	Receive Noise, C-message Weighted: Sign Bit Toggle	Input to D_R is 0 code with Sign Bit Toggle at 1KHz Rate		1	10	dBm0p
N_{RP}	Receive Noise, Psophometrically Weighted	D_R = Lowest Positive Decode Level		-90	– 81	dB0p
N_{SF}	Single Frequency NOISE End to End Measurement	CCITT G.712.4.2			– 50	dBm0
$PSRR_1$	V_{CC} Power Supply Rejection, Transmit Channel	Idle Channel ; 200mV P-P Signal on Supply ; 0 to 50kHz, Measure at D_X		– 40		dB
$PSRR_2$	V_{BB} Power Supply Rejection, Transmit Channel	Idle Channel ; 200mV P-P Signal on Supply ; 0 to 50kHz, Measure at D_X		– 40		dB
$PSRR_3$	V_{CC} Power Supply Rejection, Receive Channel	Idle Channel ; 200mV P-P Signal on Supply ; Measure Narrow Band at PWRO+ Single Ended, 0 to 50kHz		– 40		dB
$PSRR_4$	V_{BB} Power Supply, Rejection Receive Channel	Idle Channel ; 200mV P-P Signal on Supply ; Measure Narrow Band at PWRO+ Single Ended, 0 to 50kHz		– 40		dB
CT_{TR}	Crosstalk, Transmit to Receive, Single Ended Outputs	VF_XI+ = 0dBm0, 1.02kHz, D_R = Lowest Positive Decode Level, Measure at PWRO+			– 80	dB
CT_{RT}	Crosstalk, Receive to Transmit, Single Ended Outputs	D_B = 0dBm0, 1.02kHz, VF_XI+ = GRDA, Measure at D_X			– 80	dB

Notes:

1. 0dBm0 is defined as the zero reference point of the channel under test (0TLP). This corresponds to an analog signal input of 1.064 V_{rms} or an output of 1.503 V_{rms} (μLaw) dual 1.068 V_{rms} or a output 1.516 V_{rms} (A-Law)

2. Unity gain input amplifier : GS_X is connected to VF_XI, Signal input VF_XI+; Maximum gain output amplifier: GS_R is connected to PWRO, output to PWRO+.

3. Noise free: DX PCM Code stable at 01010101.

A.C. CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DISTORTION						
$SD1_X$	Transmit Signal to Distortion, μ-law Sinusoidal Input; CCITT G.712-method 2	$0 \leq VF_XI+ \leq -30dBm0$ −40dBm0 −45dBm0	36 30 25			dB dB dB
$SD2_X$	Transmit Signal to Distortion, A-law Sinusoidal Input, CCITT G.712-method 2	$0 \leq VF_XI+ \leq -30dBm0$ −40dBm0 −45dBm0	36 30 25			dB dB dB
$SD1_R$	Transmit Signal to Distortion, μ-law Sinusoidal Input , CCITT G.712-method 2	$0 \leq VF_XI+ \leq -30dBm0$ −40dBm0 −45dBm0	36 30 25			dB dB dB
$SD2_R$	Receive Signal to Distortion, A-law Sinusoidal Input; CCITT G.712-method 2	$0 \leq VF_XI+ \leq -30dBm0$ −40dBm0 −45dBm0	36 30 25			dB dB dB
DP_{X1}	Transmit Single Frequency Distortion Products	AT & T Adivisory # 64 (3.8) 0dBm0 Input Signal			−46	dB
DP_{R1}	Receive Single Frequency Distortion Products	AT & T Adivisory # 64 (3.8) 0dBm0 Input Signal			−46	dB
IMD_1	Intermodulation Distortion, End to End Measurement	CCITT G.712 (7.1)			−35	dB
IMD_2	Intermodulation Distortion, End to End Measurement	CCITT G.712 (7.2)			−49	dB
SOS	Spurious Out of Band Signals, End to End Measurement	CCITT G.712 (6.1)			−30	dBm0
SIS	Spurious in Band Signals, End to End Measurement	CCITT G.712 (9)			−40	dBm0
D_{AX}	Transmit Absolute Delay	Fixed Data Rate CLK_X = 2.048MHz, 0dBm0, 1.02kHz Signal at VF_XI+ Measure at D_X		300		μs
D_{DX}	Transmit Differential Envelope Delay Relative to D_{AX}	f = 500 − 600Hz f = 600 − 1000Hz f = 1000 − 2600Hz f = 2600 − 2800Hz		170 95 45 80		μs μs μs μs
D_{AR}	Receive Absolute Delay	Fixed data rate, CLK_R = 2.048MHz; Digital input is DMW codes. Measure at PWRO+			190	μs
D_{DR}	Receive Differential Envelope Delay Relative to D_{AR}	f = 500 − 600Hz f = 600 − 1000Hz f = 1000 − 2600Hz f = 2600 − 2800Hz		10 10 85 110		μs μs μs μs

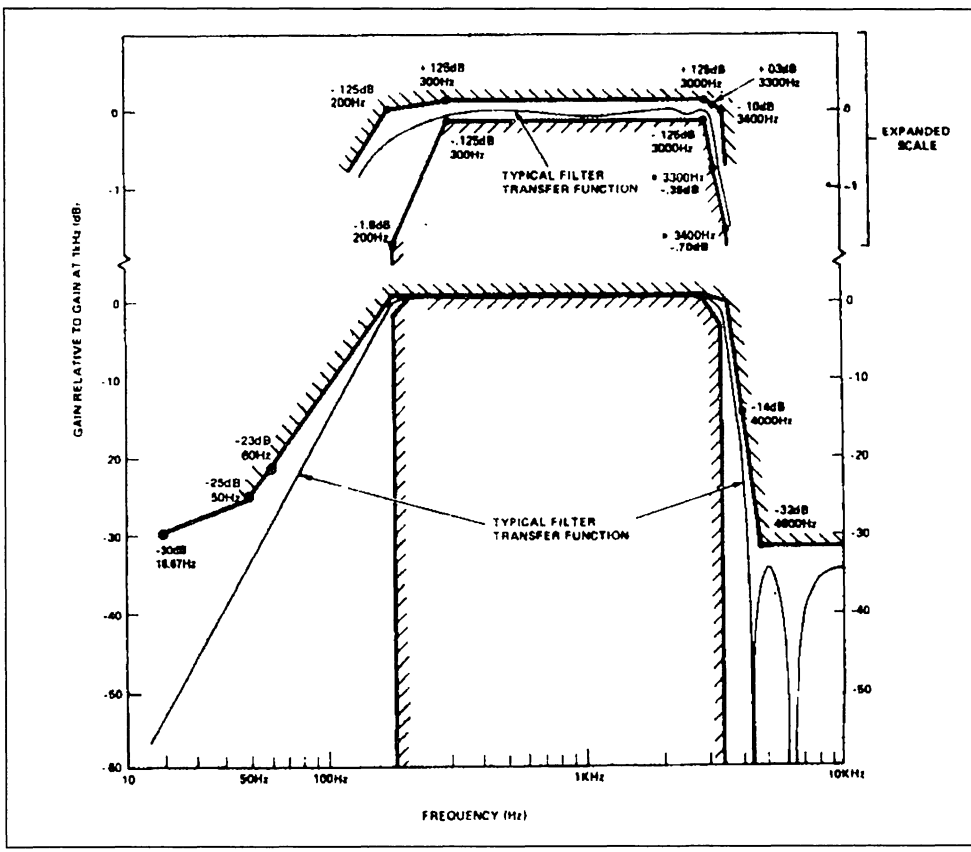
A.C. CHARACTERISTICS (continued)

TRANSMIT CHANNEL TRANSFER CHARACTERISTICS

(Input amplifier is set for unity gain, noninverting; maximum gain output.)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
G_{RX}	Gain Relative to Gain at 1.02 kHz	0 dBm0 Signal Input at VF_XI+				
	16.67Hz				− 30	dB
	50Hz				− 25	dB
	60Hz				− 23	dB
	200Hz		− 1.8		− 0.125	dB
	300 to 3000Hz		− 0.125		+ 0.125	dB
	3300Hz		− 0.35		+ 0.03	dB
	3400Hz		− 0.7		− 0.10	dB
	4000Hz				− 14	dB
	4600Hz and Above				− 32	dB

Figure 5: Transmit Filter

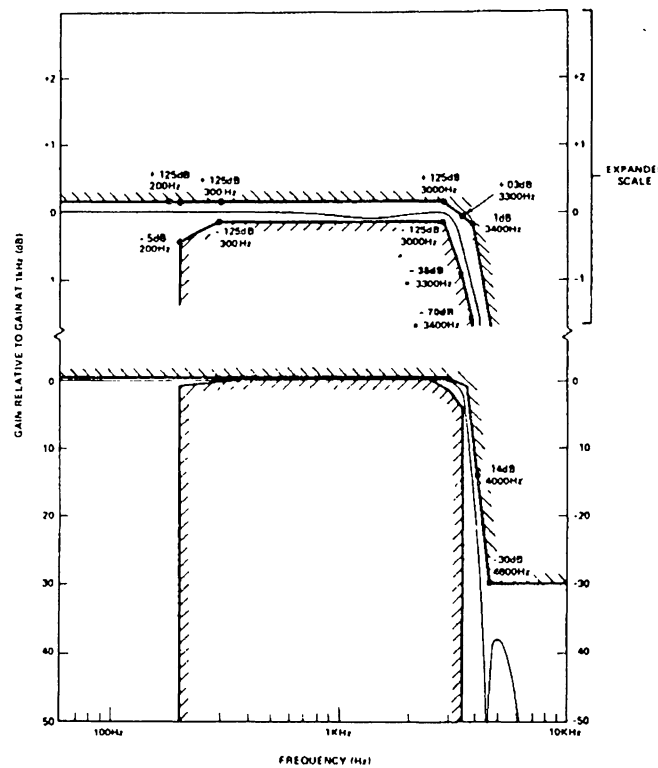


A.C. CHARACTERISTICS (continued)

RECEIVE CHANNEL TRANSFER CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
G_{RR}	Gain Relative to Gainat 1.02kHz	0dBm0 Signal Input at D_R				
	below 200Hz				+ 0.125	dB
	200Hz		– 0.5		+ 0.125	dB
	300 to 3000Hz		– 0.125		+ 0.125	dB
	3300Hz		– 0.35		+ 0.03	dB
	3400Hz		– 0.7		– 0.1	dB
	4000Hz				– 14	dB
	4600Hz and Above				– 30	dB

Figure 6: Receive Filter



AC CHARACTERISTICS - TIMING PARAMETERS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CLOCK SECTION						
t_{CY}	Clock Period, CLK_X, CLK_R	$f_{CLKX} = f_{CLKR} = 2.048MHz$	488			ns
t_{CLK}	Clock Pulse Width	CLK_X, CLK_R	195			ns
t_{DCLK}	Data Clock Pulse Width[1]	$64kHz \leq f_{DCLK} \leq 2.048MHz$	195			ns
t_{CDC}	Clock Duty Cycle	CLK_X, CLK_R	40	50	60	%
t_r, t_f	Clock Rise and Fall Time		5		30	ns
TRANSMIT SECTION, FIXED DATA RATE MODE[2]						
t_{DZX}	Data Enabled on TS Entry	$0 < C_{LOAD} < 100pF$	0		145	ns
t_{DDX}	Data Delay from CLK_X	$0 < C_{LOAD} < 100pF$	0		145	ns
t_{HZX}	Data Float on TS Exit	$C_{LOAD} = 0$	60		190	ns
t_{SON}	Timeslot X to Enable	$0 < C_{LOAD} < 100pF$	0		145	ns
t_{SOFF}	Timeslot X to Disable	$C_{LOAD} = 0$	50		190	ns
t_{FSD}	Frame Sync Delay		0		120	ns
t_{SS}	Signal Setup Time		0			ns
t_{SH}	Signal Setup Time		0			ns
RECEIVE SECTION, FIXED DATA RATE MODE						
t_{DSR}	Receive Data Setup		10			ns
t_{DHR}	Receive Data Hold		60			ns
t_{FSD}	Frame Sync Delay		0		120	ns
t_{SIGR}	SIG_R Update		0		2	µs
TRANSMIT SECTION, FIXED DATA RATE MODE[2]						
t_{TSDX}	Timeslot Delay from $DCLK_X$		-80		80	ns
t_{FSD}	Frame Sync Delay		0		120	ns
t_{DDX}	Data Delay from $DCLK_X$	0 < CLOAD < 100pF	0		100	ns
t_{DON}	Timeslot to D_X Active	$0 < C_{LOAD} < 100pF$	0		50	ns
t_{DOFF}	Timeslot to D_X Inactive	$0 < C_{LOAD} < 100pF$	0		80	ns
f_{DX}	Data Clock Frequency		64		2048[1]	KHz
t_{DFSX}	Data Delay from FS_X	$t_{TSDX} = 80ns$	0		140	ns
RECEIVE SECTION, FIXED DATA RATE MODE						
t_{TSDR}	Timeslot Delay from $DCLK_R$		-80		80	ns
t_{FSD}	Frame Sync Delay		0		120	ns
t_{DSR}	Receive Data Setup Time		10			ns
t_{DHR}	Receive Data Hold Time		60			ns
t_{DR}	Data Clock Frequency		64		2048[1]	kHz
t_{SER}	Timeslot End Receive Time		0			ns
64KB OPERATION, VARIABLE DATA RATE MODE						
t_{FSLX}	Transmit Frame Sync Minimum Downtime	FS_X is TTL high for remainder of frame	488			ns
t_{FSLR}	Receive Frame Sync Miniumum Downtime	FS_R is TTL high for remainder of frame	1952			ns
t_{DCLK}	Data Clock Pulse Width		10			µs

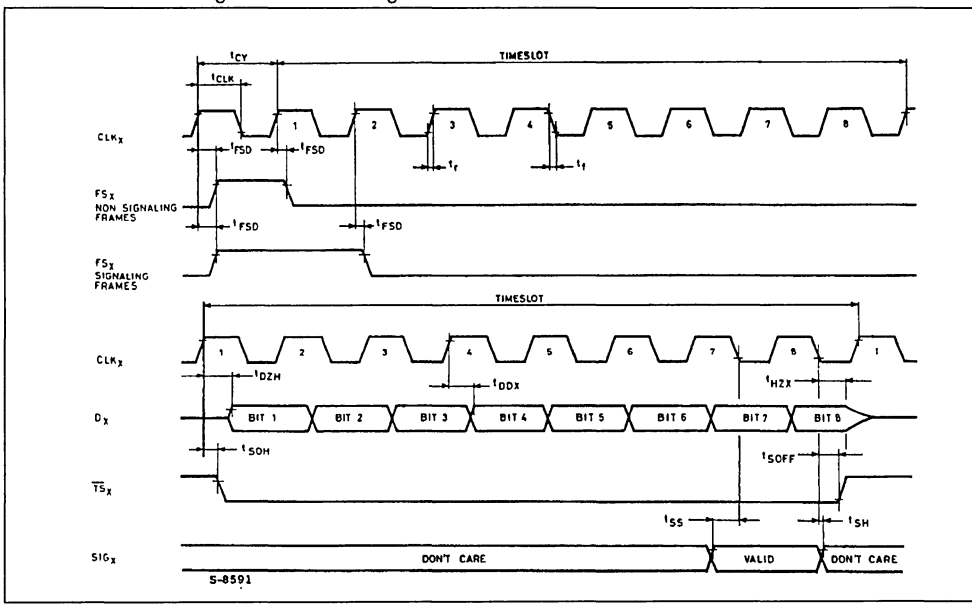
Notes:

1. Devices are available wich operate at data rates up to 4.096MHz; the minimum data clock pulse width for these devices is 110ns

2. Timing parameters t_{DZX}, t_{HZX}, and t_{SOFF} are referenced to a high impedance state.

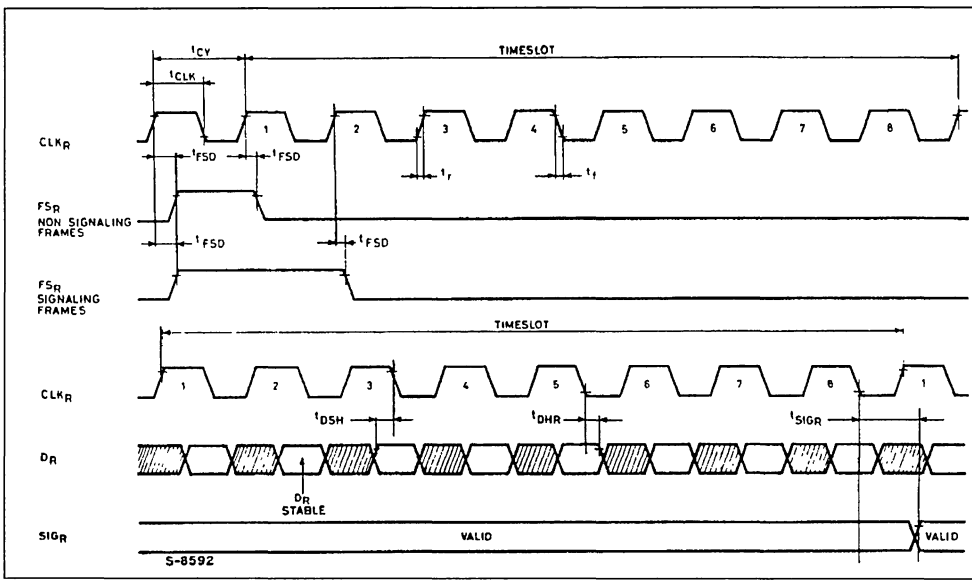
WAVEFORMS:

Fixed Data Rate Timing - Transmit Timing



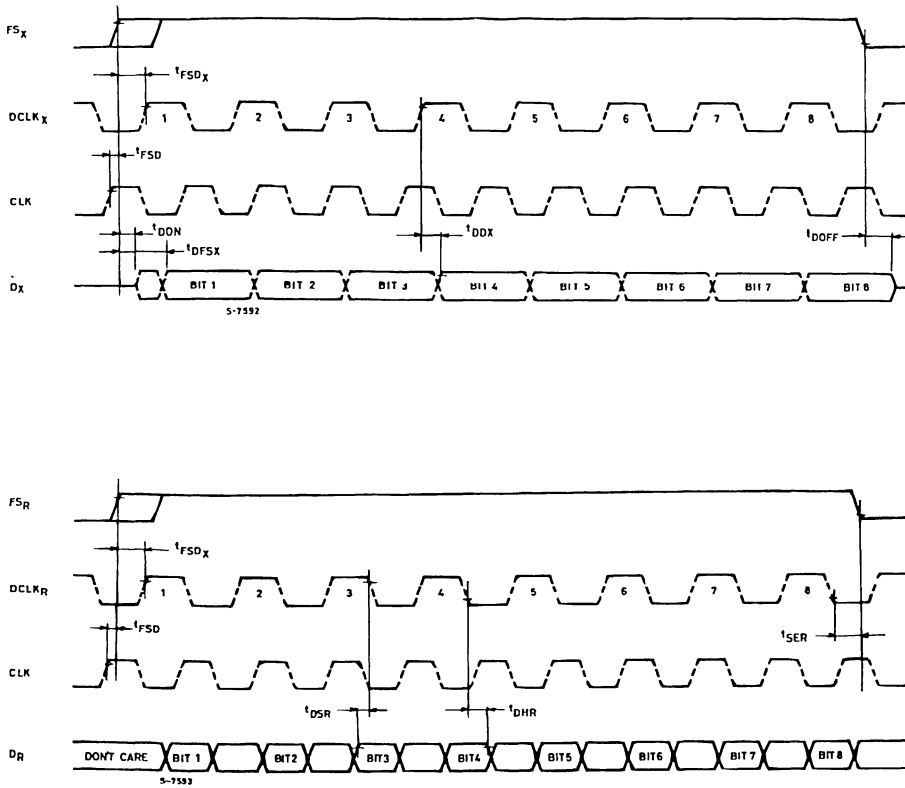
NOTE: All timing parameters referenced to V_{IH} and V_{IL} except t_{DZX}, t_{SOFF} and t_{HZX} which reference a high impedance state.

Receive Timing

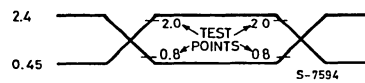


NOTE: All timing parameters referenced to V_{IH} and V_{IL}

VARIABLE DATA RATE TIMING



AC Timing Input, Output Waveform



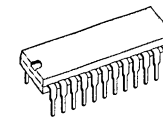
SGS-THOMSON MICROELECTRONICS

M34116

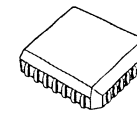
PCM CONFERENCE CALL AND TONE GENERATION CIRCUIT

PRELIMINARY DATA

- HW AND SW COMPATIBLE WITH M116
- 1 TO 64 SERIAL CHANNELS PER FRAME (CONTROLLED BY SYNC SIGNAL PERIOD)
- 29 MAXIMUM CONFERENCES
- 1 TO 64 SERIAL CHANNELS PER CONFERENCES
- 3 SIMULTANEOUS OPERATION MODES AVAILABLE:
  CONFERENCE, TRANSPARENT AND TONE GENERATION
- TYPICAL BIT RATES:
  1536/1544/2048/4096 Kbits/s
- COMPATIBLE WITH ALL KINDS OF PCM FORMAT
- μ AND A LAW (PIN PROGRAMMABLE)
- EQUAL PRIORITY TO EVERY CHANNEL
- ONE FRAME AND ONE CHANNEL DELAY FROM SENDING TO RECEIVING
- OVERFLOW INFORMATION FOR EACH CONFERENCE BY PIN $\overline{OS}$ (OVERFLOW SIGNALLING) AND ON DATA BUS ON MPU REQUEST
- INSTRUCTION SET COMPATIBLE WITH M3488
- PROGRAMMABLE INPUT AND OUTPUT ATTENUATION OR GAIN FROM 0 TO 15dB WITH STEP OF 1dB FOR EACH CHANNEL
- TONE GENERATION FROM 3.9Hz TO 3938Hz WITH MIN. STEP OF 3.9Hz
- TOTAL OF 7 DIFFERENT TONE OUTPUTS IN PARALLEL PROGRAMMABLE VIA MPU (MAXIMUM 4 DIFFERENT FREQUENCIES AND DURATIONS)
- 1 MELODY OF MAXIMUM 32 PROGRAMMABLE FREQUENCIES AND DURATIONS
- 5V POWER SUPPLY
- TTL COMPATIBLE INPUT LEVELS, CMOS/TTL COMPATIBLE OUTPUT LEVELS
- MAIN INSTRUCTIONS CONTROLLED BY MICROPROCESSOR INTERFACE:
  - Channel connection to a conference
  - Channel attenuation or gain
  - Channel disconnection from both conference and transparent modes
  - Tone and melody generation
  - Overflow status
  - Operating mode
  - Channel status



DIP24
ORDERING NUMBER: M34116B1



PLCC28
ORDERING NUMBER: M34116C1

DESCRIPTION

The M34116 is a product specifically designed for applications in PCM digital exchanges. It is able to handle up to 64 channels in any conferences combination from 1 to 29 conferences in parallel and to generate seven different tones and one melody.

The parties in a conference must previously be allocated through the Digital Switching Matrix (M3488) in a single serial wire at M34116 PCM input (IN PCM pin).

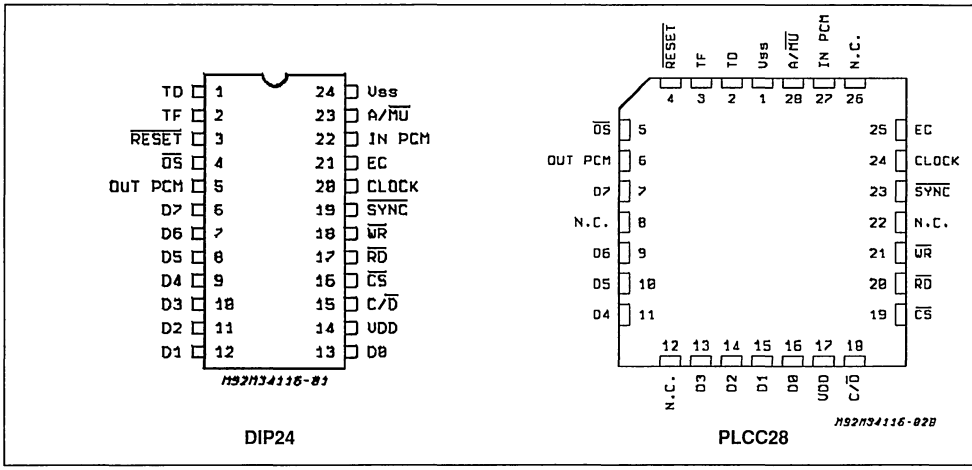
The M34116 is full pin and function compatible with the M116. In addition, it has the capability to generate tone directly coded in PCM.

For the conference function, each channel is converted inside the chip from PCM law to linear law (14 bits). Then it is added to its conference, and the sample of the previous frame is subtracted from the conference.
In this way a new conference sum signal is generated.
The channel output signal will contain the information of all the other channels in its conference except its own.

After the PCM encoding, the data is serialized by the M34116 in the same sequence as the PCM input frame, with one frame (plus one channel) delay and will be reallocated by the DSM (M3488) at the final channel and bus position.

A programmable attenuation or gain can be set on each channel and for every function: conference, tone generation and transparent mode.

PIN CONNECTIONS (Top view)



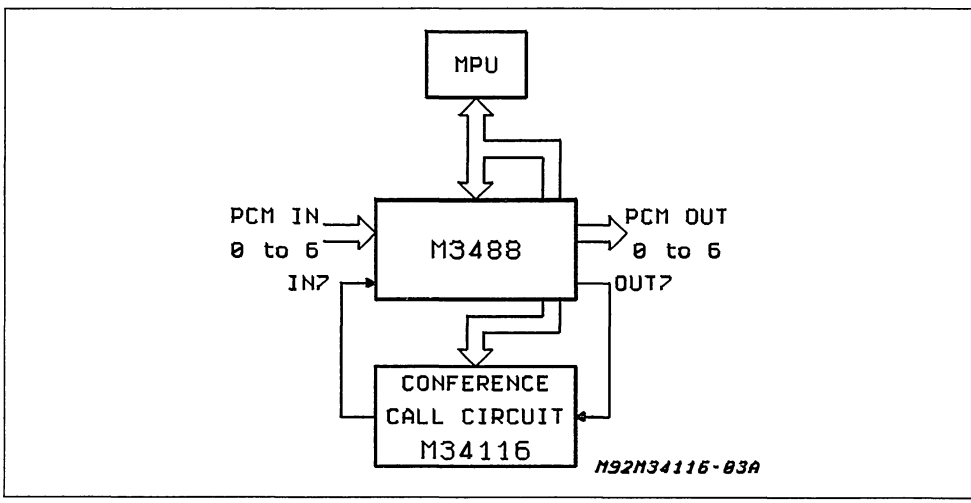
DIP24 PLCC28

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD} (*)	Supply Voltage	– 0.3 to 7	V
V_I	Input Voltage	– 0.3 to V_{DD}	
$V_{O\ (off)}$	Off State Output Voltage	– 0.3 to 7	V
P_{tot}	Total Power Dissipation	500	mW
T_{stg}	Storage Temperature	– 65 to 150	°C
T_{op}	Operating Temperature	0 to 70	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1: PCM Conference Call Insertion Scheme



PIN DESCRIPTION

DIP N°	PLCC N°	Pin	Function
1	2	TD	M116 operating mode only. Tone Duration input pin. When TD = 1, a PCM coded tone (instead of PCM data) is sent out to all channels enabled by the IT bit. TD is latched by the SYNC signal so that all channels have the same tone during the same number of frames. TD = 0 for normal operation.
2	3	TF	M116 operating mode only. Tone Frequency input pin. When TF = 1, the tone amplitude is high. When TF = 0, the tone amplitude is low. TF is latched by SYNC. The PCM coded tone level corresponds to 1/10 of the full scale. For M34116 operating mode: Melody waveform select input pin. When TF = 1, the PCM output of the melody represents a square wave. When TF = 0, it represents a sine wave. In both cases, the rms level is the same and is equal to – 6 dBm0 if no attenuation or gain is programmed.
3	4	$\overline{\text{RESET}}$	Master reset input pin. This pin is active low and must be used at the very beginning after power up to initialize the device or when switching from A law to Mu law. The Internal initialization routine takes 2 time frames starting from the rising edge of $\overline{\text{RESET}}$. During this initialization time, all data bus and PCM output are pulled to a high impedance state.
4	5	$\overline{\text{OS}}$	Overflow Signalling output pin. When $\overline{\text{OS}}$ = 0 one conference is in overflow. This signal is anticipated over half time slot with respect to the output channel involved in the conference in overflow. Example: if output channel 4 is one of the parties of one conference in overflow, $\overline{\text{OS}}$ = 0 during the second half of the time slot corresponding to output channel 3 and during the first half of the time slot corresponding to output channel 4.
5	6	OUT PCM	PCM output pin. The bit rate is 4096Kbits/s max. The sign bit is the first bit of the serial sequence. The first bit of the first channel is found at the rising edge of the CLOCK signal preceding the rising edge of the $\overline{\text{SYNC}}$ signal. The output buffer is open drain to allow for multiple connections.
6 to 13	7, 9 to 11, 13 to 16	D0 to D7	Bidirectional Data bus pins. Data and instructions are transferred to or from the microprocessor. D0 is the Least Significant Bit. The bus is tristate when RESET is low and/or $\overline{\text{CS}}$ is high.
14	17	VDD	+5V Supply input. 100nF decoupling capacitor recommended.
15	18	C/$\overline{\text{D}}$	Control Data input pin. In a write operation C/$\overline{\text{D}}$ = 0 qualifies any bus content as data while C/$\overline{\text{D}}$ = 1 qualifies it as an opcode. For M116 operating mode only: in a read operation, the overflow information of the first eight conferences is selected by C/$\overline{\text{D}}$ = 0, the overflow of the last two conferences and the status by C/$\overline{\text{D}}$ = 1.
16	19	$\overline{\text{CS}}$	Chip Select input pin. When $\overline{\text{CS}}$ = 0, data and instructions can be transferred to or from the external microprocessor and when $\overline{\text{CS}}$ = 1 the data bus is in tristate.
17	20	$\overline{\text{RD}}$	Read control input pin. When $\overline{\text{RD}}$ = 0, read operation is performed. When match conditions for the opcode exists, data is transferred to the external microprocessor on the falling edge of $\overline{\text{RD}}$.
18	21	$\overline{\text{WR}}$	Write control input pin. Instructions and opcode from the external microprocessor are latched on the rising edge of $\overline{\text{WR}}$.
19	23	$\overline{\text{SYNC}}$	Synchronization input pin. The rising edge of CLOCK preceding the rising edge of $\overline{\text{SYNC}}$ corresponds to the first bit of the first channel except for PCM frame of 1544Kbits/s. In this case, it corresponds to the Extra bit (193th).
20	24	CLOCK	Master Clock input pin. Typ. operating Frequencies are: 3.072MHz for 24 PCM channels frame (192 bit/frame) 3.088MHz for 24 PCM channels frame with extra bit (193 bit/frame) 4.096MHz for 32 PCM channels frame (256 bit/frame) 8.192MHz for 64 PCM channels frame (512 bit/frame) Both M34116 an M116 operating modes are possible up to 4.096MHz. At 8.192MHz only M34116 operating mode is possible.
21	25	EC	External Clock output pin. This pin provides the master clock for the Digital Switching Matrix (M3488). Normally it is the same signal as applied to the CLOCK input (pin 20). When the Extra bit is selected with the instruction 5, the first two periods of the master clock are canceled in order to allow the operation of the M34116 and the DSM with PCM frame with Extra bit (e.g. 193 bit/frame with PCM I/O of 1544Kbits/s).
22	27	IN PCM	PCM input pin. The max bit rate is 4096Kbits/s. The first bit of the first cahnnel is found at the second rising edge of the CLOCK signal following the rising edge of the SYNC signal. If Extra bit is selected, then the first bit is shifted by two CLOCK periods.
23	28	A/$\overline{\text{MU}}$	A Law or MU Law select pin. When A/$\overline{\text{MU}}$ = 1, A Law is selected. When A/$\overline{\text{MU}}$ = 0, MU Law is selected. The law selection must be done before initializing the device using the RESET pin.
24	1	Vss	Ground.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.75 to 5.25	V
V_I	Input Voltage	0 to 5.25	V
V_O	Off State Output Voltage	0 to 5.25	V
CLOCK Freq.	Input Clock Frequency	3.072/3.088 4.096 / 8.192 (*)	MHz MHz
$\overline{SYNC}$ Freq.	Input Synchronization Frequency	8	KHz
T_{op}	Operating Temperature	0 to 70	°C

CAPACITANCES (measurements frequency = 1MHz; 0 to 70°C; unused pins tied to V_{SS})

Symbol	Parameter	Pin (**)	Min.	Typ.	Max.	Unit
C_I	Input Capacitance	1 to 3; 15 to 20; 22 to 23			5	pF
$C_{I/O}$	I/O Capacitance	6 to 13			15	pF
C_O	Output Capacitance	4, 5, 21			10	pF

ELECTRICAL CHARACTERISTICS (Tamb = 0 to 70°C, V_{CC} = 5V ± 5%)
All DC characteristic are valid 250µs after V_{CC} and clock have been applied.

Symbol	Parameter	Pins (**)	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level	1 to 3 15 to 20 22 to 23		– 0.3		+0.8	V
V_{IH}	Input High Level	1 to 3 15 to 20 22 to 23		2.0		V_{CC}	V
V_{T-}	Negative Threshold Voltage	6 to 13 (***)	V_{CC} = 5V	0.6	0.9	1.1	V
V_{T+}	Positive Threshold Voltage	6 to 13 (***)	V_{CC} = 5V	1.5	1.7	2	V
V_{HY}	Hysteresis	6 to 13 (***)	V_{CC} = 5V	0.4	0.8		V
V_{OL}	Output Low Level	4,6 to 13,21	I_{OL} = 2mA			0.4	V
V_{OH}	Output High Level	4 to 13, 21	I_{OH} = 1mA	V_{CC}-0.4			V
V_{OL}	Output Low Level	5	I_{OL} = 4.1mA			0.4	V
I_{IL}	Input Leakage Current	1 to 3 6 to 13 15 to 20 22 to 23	V_{IN} = 0 to V_{CC}			10	µA
I_{OL}	Data Bus Leakage Current	6 to 13	$\overline{V_{IN}}$ = 0 to V_{CC} $\overline{CS}$ = V_{CC}			±10	µA
I_{CC}	Supply Current	14	Clock Freq. = 4.096MHz			50	mA

(*) Only in M34116 Operating Mode.
(**) Pin numbers referred to the DIP24.
(***) Schimitt-trigger inputs.

ELECTRICAL CHARACTERISTICS (Tamb = 0 to 70°C, V_{CC} = 5V ± 5%)
All DC characteristic are valid 250µs after V_{CC} and clock have been applied. C_L is the max. capacitive load and R_L the test pull up resistor.

Signal	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
CK	t_{CK}	Clock Period		230			ns
Up to	t_{WL}	Clock Low Level Width		100			ns
4.096MHz	t_{WH}	Clock High Level Width		100			ns
	t_R	Rise Time				25	ns
	t_F	Fall Time				25	ns
CK	t_{CK}	Clock Period		120			ns
8.192MHz	t_{WL}	Clock Low Level Width		50			ns
	t_{WH}	Clock High Level Width		50			ns
	t_R	Rise Time				10	ns
	t_F	Fall Time				10	ns
$\overline{SYNC}$	t_{SL}	Low Level Set-up Time	See note 1	30			ns
	t_{HL}	Low Level Hold Time		30			ns
	t_{SH}	High Level Set-up Time		30			ns
	t_{WH}	High Level Width		t_{CK}			ns
PCM	t_S	Set-up Time		35			ns
Input	t_H	Hold Time		35			ns
PCM Output (Open drain)	$t_{PD\ min}$	Propagation Time Low Level referred to CK	C_L = 50pF R_L = 1KΩ	40			ns
	$t_{PD\ max}$	Propagation Time High level Referred to CK				180	ns
$\overline{RESET}$	t_{SL}	Low Level Set-up Time	note 6	50			ns
	t_{HL}	Low Level Hold Time		30			ns
	t_{SH}	High Level Set-up Time		30			ns
	t_{WH}	High Level Width		t_{CK}			ns
$\overline{WR}$	t_{WL}	Low Level Width		150			ns
	t_{WH}	High Level Width		200			ns
	t_{REP}	Repetition interval between active pulses.	note 3 and 4	500			ns
	t_{SH}	High Level st-up time to active read strobe.		0			ns
	t_{HH}	High Level hold time to active read strobe.		20			ns
	t_R	Rise Time				60	ns
	t_F	Fall Time				60	ns
RD	t_{WL}	Low Level Width		180			ns
	t_{WH}	High Level Width		200			ns
	t_{REP}	Repetition interval between active pulses.	note 5	4 t_{CK}			ns
	t_{SH}	High Level st-up time to active read strobe.		0			ns
	t_{HH}	High Level hold time to active read strobe.		20			ns
	t_R	Rise Time				60	ns
	t_F	Fall Time				60	ns

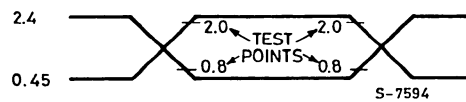
Notes:

1. With Extra Bit operating mode insert this time becomes 3 t_{CK}.
2. With Extra Bit operating mode insert these times are 80ns longer.
3. With OPCODE (C/D = l), this time becomes 4tck (6tck if E = 1). E: extra bit indication in "operating mode" instruction.
4. For tone generation instruction, this time becomes 4tck (6tck if E = 1) E: extra bit indication in "operating mode" instruction.
5. With extra bit operating mode insert, this time becomes 6tck
6. The initialization routine takes 2 frames time starting from the rising edge of $\overline{RESET}$ - Any access to the device should take place after the initialization routine is completed. (2 frames time)

ELECTRICAL CHARACTERISTICS (continued)

Signal	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$\overline{CS}$	$t_{SL\ (\overline{CS}\text{-}\overline{WR})}$	Low level set-up time to $\overline{WR}$ falling edge.	Active Case	0			ns
	$t_{HL\ (\overline{CS}\text{-}\overline{WR})}$	Low Level hold time from $\overline{WR}$ rising edge.	Active Case	20			ns
	$t_{SH\ (\overline{CS}\text{-}\overline{WR})}$	High level set-up time to $\overline{WR}$ falling edge.	Inactive Case	0			ns
	$t_{HH\ (\overline{CS}\text{-}\overline{WR})}$	High level hold time from $\overline{WR}$ rising edge.	Inactive Case	20			ns
	$t_{SL\ (\overline{CS}\text{-}\overline{RD})}$	Low level set-up time to $\overline{RD}$ falling edge.	Active Case	0			ns
	$t_{HL\ (\overline{CS}\text{-}\overline{RD})}$	Low Level hold time from $\overline{RD}$ rising edge.	Active Case	0			ns
	$t_{SH\ (\overline{CS}\text{-}\overline{RD})}$	High level set-up time to $\overline{RD}$ falling edge.	Inactive Case	0			ns
	$t_{HH\ (\overline{CS}\text{-}\overline{RD})}$	High level hold time from $\overline{RD}$ rising edge.	Inactive Case	0			ns
$\overline{CD}$	$t_{S(\overline{C/D}\text{-}\overline{WR})}$	Set-up time to write strobe end.		130			ns
	$t_{H(\overline{C/D}\text{-}\overline{WR})}$	Hold time from write strobe end.		25			ns
	$t_{S(\overline{C/D}\text{-}\overline{RD})}$	Set-up time to read strobe start.		20			ns
	$t_{H(\overline{C/D}\text{-}\overline{RD})}$	Hold time from read strobe end.		25			ns
$\overline{OS}$	$t_{PD(\overline{OS})}$	Propagation time from rising edge of CK.	C_L = 50pF			100	ns
EC	$t_{PD(EC)}$	Propagation time referred to CK edges.	C_L = 50pF			30	ns
TD/TF	t_S	Set-up		80			ns
	t_H	Hold Time		40			ns
D0 to D7 (interface bus)	$t_{S(BUS\text{-}WR)}$	Input set-up time to write strobe end.		130			ns
	$t_{H(BUS\text{-}WR)}$	Input hold time from write strobe end.		25			ns
	$t_{PD(BUS)}$	Propagation time from (active) falling edge of read strobe.	CL = 200pF			120	ns
	$t_{HZ(BUS)}$	Propagation time from (active) rising edge of read strobe to high impedance state.				80	ns

A.C. TESTING, OUTPUT WAVEFORM



A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0", timing measurement are made at 2.0V for a logic "1" and 0.8V for a logic "0".

Figure 2: Insertion Schema of M34116 in a 480 x 480 Non-Blocking Digital Switching Matrix

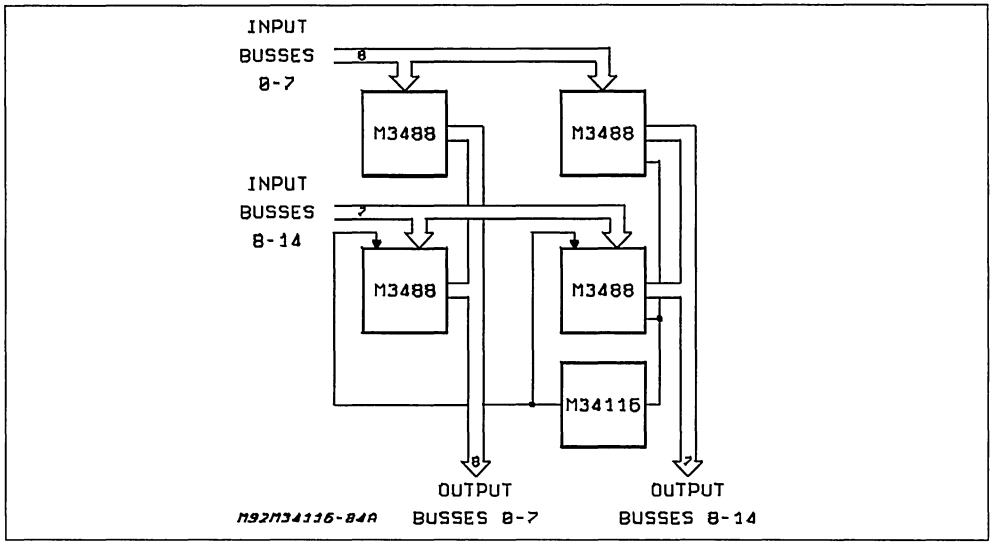
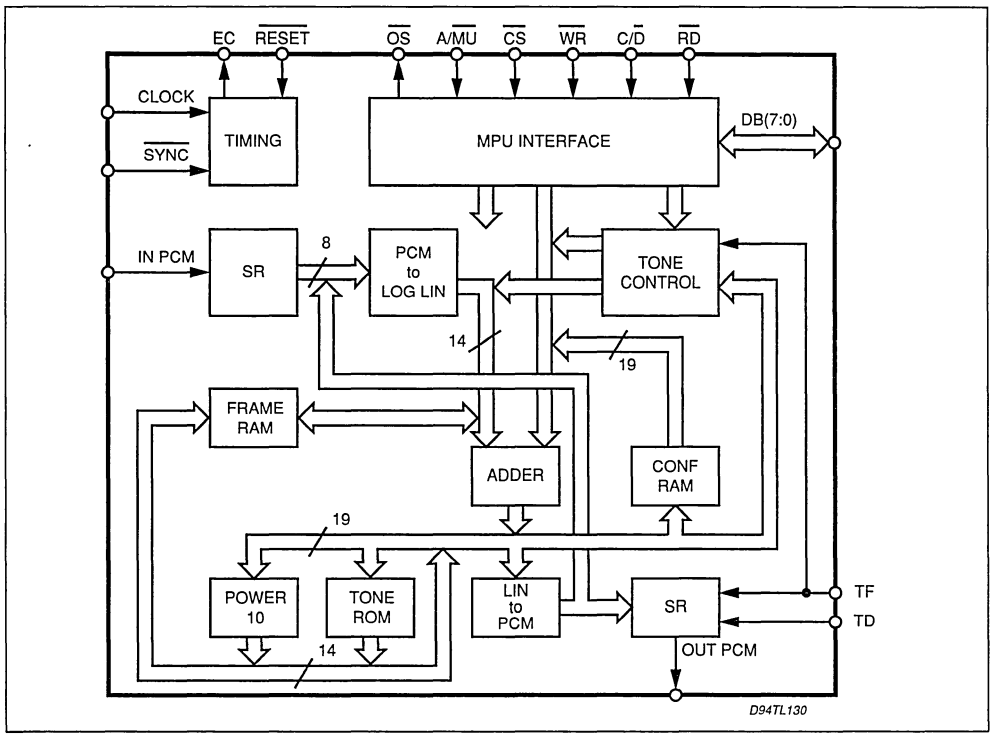


Figure 3: Block Diagram



CIRCUIT DESCRIPTION

ALGORITHMS

- Conference. For each channel, the PCM signal coming in is added to its conference and the PCM signal of the previous frame is subtracted to its conference before being sent out. The output signal contains only the data of all the other channels in its conference except its own.
- Tone. A fourth of a sine wave equivalent to 3.9Hz (8KHz/2048) is stored in a ROM which is read at multiple of the step (modulus 512) equivalent to the specified frequency. This step is used until the duration is reached then a new step will be used according to the specified sequence.
- Attenuation gain. The PCM signal is converted to logarithmic of the equivalent linear and then added or subtracted to the specified level. It is then raised to the power of 10 to be converted back to linear.

ARCHITECTURE

The basic time slot (16 periods of the master clock) is divided in four different parts that perform four different operations (also refer to Fig. 2 block diagram):

input processing: attenuation or gain of input PCM according to the algorithm mentioned earlier. The serial PCM signal coming in is loaded as 8 bits parallel and converted to logarithmic of the linear (through the PCM to LOG LIN block). It is then added to the attenuation or gain levels (also in logarithmic) stored in the MPU interface, the result is raised to the power of 10 (through the POWER 10 block) to be converted back to linear and written in the FRAME RAM.

conference addition: the above PCM signal, amplified or attenuated and converted in linear, is added to the conference and the result is stored in the conference RAM (block CONF RAM).

conference subtraction: the signal stored in the FRAME RAM during the previous frame is subtracted to the conference and the result is stored in the conference RAM.

output processing: attenuation or gain of the PCM to be sent out. The result of the above substraction is converted to PCM (through the block LIN to PCM) and to logarithmic (through the block PCM to LOG LIN), added to the attenuation or gain level stored in the MPU interface, converted to linear (through the block POWER 10) and then to PCM (through the block LIN to PCM). The resulting 8 bits are then shifted out serially.

If a channel is in conference, then all the four above operations are applied. If it is in transparent mode, then only the first and last operations are applied. For tone generation, the two first operations are not used. During the third part, the tone ROM is read. Since the ROM data is in linear it can therefore be applied to the fourth operation for output processing.

By default, after reset, the M34116 has the functionality and the instruction set of the M116. With a new operating mode instruction, the user can select the functionality of the M34116 with its new instruction set. The instruction set includes:

◊ operating mode: the user can choose either the M116 mode or the M34116 mode, the PCM byte format (no bit inverted, even bit inverted, odd bit inverted or all bit inverted) and the presence or not of the extra bit.

◊ conference connection: the user specifies which channel to be connected to which conference with the attenuation or gain levels to be applied to the PCM signal coming in and/or sent out.

◊ transparent connection: the user specifies which channel to be connected in transparent mode (bypass mode) with the attenuation or gain levels to be applied to the PCM signal coming in and/or sent out.

◊ tone generation: the user specifies to which channel the tone must be sent out with the attenuation or gain levels and the tone sequence. The sequence is composed of maximum 4 pairs of frequency-duration for tone and maximum 32 pairs of frequency-duration for melody. The frequency range is 3.9Hz to 3938Hz and the duration range is from 32ms to 8610ms. The user can specify either all of the pairs or finish the sequence with the byte hex FF. The M34116 will loop the specified sequence endlessly or until the channel is disconnected. The melody could be either a sine or square wave (pin programmable).

◊ channel disconnection: the user specifies which channel to be disconnected. A disconnected channel can be reconnected only after a minimum of one frame time.

◊ overflow status. The user specifies which of the 4 banks of 8 conferences to be monitored and the M34116 will send the status byte at the read operation.

◊ channel status. The user specifies the channel number and the M34116 will send out the status bytes at the read operation. These bytes include: conference number or transparent mode or tone or no connection, input attenuation or gain levels, output attenuation or gain levels. If the channel is in the tone mode, the tone sequence of frequency and duration will also be sent out.

INSTRUCTION SET

OPERATING MODES

Two different operating mode istructions are available:

M116 Operating Mode:
Sending this operating mode instruction, the device functionality is the same as M116 and M116 instruction set is selected (refer to the following M116 instruction set for further details).

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	X	E	F1	F0	0	1	0	1

- E = 1 extra bit
- F1– F0 = 00 no bit inverted
  01 even bit inverted
  10 odd bit inverted
  11 all bit inverted

Default values after reset:

E = 0 F1– F0 = 11 if MU Law
F1– F0 = 01 if A Law

M34116 Operating Mode:
Sending this operating mode instruction, the M34116 instruction set and functionality are selected

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	X	E	F1	F0	1	0	0	1

- E = 1 extra bit
- F1– F0 = 00 no bit inverted
  01 even bit inverted
  10 odd bit inverted
  11 all bit inverted

Note:
Upon reset M116 instruction set is automatically selected. To switch from the M116 instruction set the above M34116 operating mode instruction is necessary. The operating mode instruction, when necessary, must be sent just after reset.

M34116 INSTRUCTION SET.

INSTRUCTION 1: M34116 CHANNEL CONNECTION IN CONFERENCE MODE
Five bytes are needed:

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	X	X	S	P4	P3	P2	P1	P0
0	1	0	0	X	X	X	AI4	AI3	AI2	AI1	AI0
0	1	0	0	X	X	X	AO4	AO3	AO2	AO1	AO0
0	1	0	0	X	PT	C5	C4	C3	C2	C1	C0
0	1	1	0	X	X	X	X	0	1	1	1

- S: Start bit
- AI4–AI0: Input attenuation or gain (±15dB)
  AI4 = 1 gain
  AI4 = 0 attenuation
  AI3–AI0 value in dB (0–15)
- OI4–AO0: output attenuation or gain (±15dB)
  AO4 = 1 gain
  AO4 = 0 attenuation
  AO3–AO0 value in dB (0–15)
- PT: Phase toggle conference
- P4–P0: Conference number (1–29)
- C5–C0: Channel number (0–63)

When S = 1 the conference register is cleared. S = 1 can be used only when connecting the first channel to a new conference.

When PT = 1 the sign of the PCM samples is changed before they are put in conference. This corresponds to a phase shift of 180° and may be used to reduce the electrical echo.

Note: Unspecified Data Bus can be either 0's or 1's

M34116 INSTRUCTION SET (continued)

INSTRUCTION 2: M34116 CHANNEL CONNECTION IN TRANSPARENT MODE
Four bytes are needed:

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	X	X	X	AI4	AI3	AI2	AI1	AI0
0	1	0	0	X	X	X	AO4	AO3	AO2	AO1	AO0
0	1	0	0	X	X	C5	C4	C3	C2	C1	C0
0	1	1	0	X	X	X	X	0	0	1	1

- ❖ AI4–AI0: Input attenuation or gain (±15dB)
  AI4 = 1 gain
  AI4 = 0 attenuation
  AI3–AI0 value in dB (0–15)
- ❖ AO4–AO0: output attenuation or gain (±15dB)
  AO4 = 1 gain
  AO4 = 0 attenuation
  AO3–AO0 value in dB (0–15)
- ❖ C5–C0: Channel number (0–63)

INSTRUCTION 3: M34116 CHANNEL DISCONNECTION
This instruction is necessary to disconnect a party from a conference, to end a transparent mode connection or to end a tone generation.
Two bytes are needed (same format as M116):

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	X	X	C5	C4	C3	C2	C1	C0
0	1	1	0	X	X	X	X	1	1	1	1

C5–C0: Channel number (0–63)

One time frame must exist between disconnection and connection of the same channel.

INSTRUCTION 4: M34116 OVERFLOW INFORMATION
Single byte instruction:

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	X	X	B1	B0	1	0	1	0

❖ B1–B0: Bank Selection (0–3)

Conference overflow information is sent out, after this instruction, in the data bus (D7–D0) when $\overline{RD}$ goes low according to the Bank selection value:

Control Signal				Bank Selection		Conference Number							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	B1	B0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	7	6	5	4	3	2	1	X
0	0	0	1	0	1	15	14	13	12	11	10	9	8
0	0	0	1	1	0	23	22	21	20	19	18	17	16
0	0	0	1	1	1	X	X	29	28	27	26	25	24

M34116 INSTRUCTION SET (continued)
INSTRUCTION 5: M34116 TONE GENERATION

Up to 7 Tone and 1 Melody channels may be active simultaneously. The instruction format for Tone and Melody is the same. For each Tone channel from 1 up to 4 couples of Step/Time may be specified while for the Melody channel from 1 up to 32 couples of Step/Time may be specified.
Note:
The Melody channel can be channel 0 or 8 or 16 or 24 etc. according to the following formula:

Melody channel number = 0 + 8 x n (n = 0, 1, 2, 3, 4, 5, 6, 7)

The Tone channel assignment follows the same rule:

Tone 1 channel number = 1 + 8 x n (n = 0, 1, 2, 3, 4, 5, 6, 7)
Tone 2 channel number = 2 + 8 x n (n = 0, 1, 2, 3, 4, 5, 6, 7)
. . . . . .
Tone 7 channel number = 7 + 8 x n (n = 0, 1, 2, 3, 4, 5, 6, 7)

This means that, selecting the tone 1 on the channel 9 (or and other one of its series), the channels 1, 17, 25.... can not be used for tones (or melody). The same is occuring for the tones 2...7 or the melody.

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/D	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0				AO4	AO3	AO2	AO1	AO0
0	1	0	0				C4	C3	C2	C1	C0
0	1	1	0					1	1	0	0
0	1	0	0	S17	S16	S15	S14	S13	S12	S11	S10
0	1	0	0	T17	T16	T15	T14	T13	T12	T11	T10
0	1	0	0	S27	S26	S25	S24	S23	S22	S21	S20
0	1	0	0	T27	T26	T25	T24	T23	T22	T21	T20
:	:	:	:	:	:	:	:	:	:	:	:

optional end code:

0	1	0	0	1	1	1	1	1	1	1	1

opcode:

0	1	1	0					1	1	0	0

- AO4–AO0: Output attenuation or gain (±15dB) AO4 = 1 gain, AO4 = 0 attenuation, AO3–AO0 value in dB (0–15)
  0dB attenuation or gain correspond to -6dBm0 level.
- C5–C0: Channel number (0–63)
- Sn7–Sn0: Frequency Step for the n–th note in the tone sequence (n = 1–4 for tone n = 1–32 for melody). Step is a compressed coding of the frequency value. Given a frequency value f the value of S7–S0 can be calculated as follow:

1) calculate the linear step $SL = \text{round}\ (f \times \frac{32}{125})$
2) apply the following table to get S7–S0 value from SL value (see also Appendix 1A and 1B).

S7	S6	Linear Step SL value (10 bit)										(SL decimal)	STEP (Hz)
0	0	0	0	0	0	S5	S4	S3	S2	S1	S0	(1→64) (*)	3.9
0	0	0	0	0	1	S5	S4	S3	S2	S1	S0	(65–>127) (**)	3.9
0	1	0	0	1	S5	S4	S3	S2	S1	S0	0	(128–>254)	7.8
1	0	0	1	S5	S4	S3	S2	S1	S0	0	0	(256–>508)	15.6
1	1	1	S5	S4	S3	S2	S1	S0	0	0	0	(512–>1008)	31.2

(*) For tone 7 only; (**) For melody and tone 1-6

Note: to obtain a Pause (Silence) –> S7–S0 must be all 0's

- End code: if Less than 4 couples of Step/Time for tone or less than 32 for melody are to be specified then after the last couple of Step/Time a Step of all 1's (optional end code) must be sent before the opcode. Otherwise it must be skipped.
- Tn7–Tn0: Specify the duration of the n'th note or pause. The time increment is 32ms. To get T7–T0 value, divide the wanted duration in ms by 32 and round to integer.

Note: The minimum time between rising edges of successive $\overline{WR}$ for tone generation instruction is 4ck periods (6ck periods if EC = 1).

M34116 INSTRUCTION SET (continued)

INSTRUCTION 6: M34116 STATUS

The Status instruction can be used to read the contents of the instruction register and of the tone and melody registers.

Two byte are needed:

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0			C5	C4	C3	C2	C1	C0
0	1	1	0					0	1	1	0

❖ C5–C0: Channel number (0–63)

After sending this instruction a variable number of Read can be sent depending on the type of operation that performs the channel (conference, transparent, tone, or melody). The first 3 Read, common to all type of operation, will send on the Data Bus the following data relative to the channel (C5–C0):

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	IT	PT		P4	P3	P2	P1	P0
0	0	0	1				AI4	AI3	AI2	AI1	AI0
0	0	0	1				AO4	AO3	AO2	AO1	AO0

Note:
P4–P0 = 0 means that the channel is disconnected so any following data read is meaningless.
P4–P0 = 1 to 29 is the conference number.
P4–P0 = 30 means that the channel operation is Tone or Melody.
P4–P0 = 31 means that the channel operation is transparent connection.

If the channel operation is Tone or Melody (P4 – P0 = 30) then the subsequent Read will send on the Data Bus the couples of Step/Time:

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	S17	S16	S15	S14	S13	S12	S11	S10
0	0	0	1	T17	T16	T15	T14	T13	T12	T11	T10
0	0	0	1	S27	S26	S25	S24	S23	S22	S21	S20
0	0	0	1	T27	T26	T25	T24	T23	T22	T21	T20
:	:	:	:	:	:	:	:	:	:	:	:

Notes:
–Tone and Melody status reading ends if an all 1's Step value is found, otherwise the reading is cyclic.

–The minimum time from the rising edge of the $\overline{WR}$ (with opcode) to the falling edge of first $\overline{RD}$ is 4clock periods (6clock periods if E = 1) unless the selected channel has been disconnected. In this case, one time frame must exist between the disconnect command and the read status command. The RD period is minimum 4clock periods (6clock periods if E = 1).

– for both modes (M34116 and M116) the minimum time between two successive rising edges of the WR with opcode (C/D = 1) is 4clock periods (6clock periods if E = 1).
E: Extra bit indication in "Operating mode" instruction.

M116 INSTRUCTION SET

INSTRUCTION 1: CHANNEL CONNECTION IN CONFERENCE MODE

Three byte are needed:

1)The first byte contains the conference number (bits D0–D3) and the Start bit S (bit D4). When S = 1, all registers of the conference will be cleared. S = 1 is only required in the instruction 1 set of the first channel connected to a new conference.

2)The second byte contains in the bits (D0–D4) the number of the channel to be connected and the Insert Tone Enable bit IT (D5). When bit IT = 1 all the channels belonging to that conference are enabled using insert tone function if it's active (TD = 1).

3) The third byte contains information about the attenuation level to be applied to that channel and the opcode (0111).

Instruction 1 Format

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	X	X	X	S	P3	P2	P1	P0
0	1	0	0	X	X	IT	C4	C3	C2	C1	C0
0	1	1	0	A1	A0	X	X	0	1	1	1

S: Conference Start bit
P3–P0: Conference number (1–10)
IT: Insertion Tone function enable (IT = 1)
C4–C0: Channel number (0–31)
A1–A0: Channel attenuation
00 = – 0dB
01 = – 3dB
10 = – 6dB

INSTRUCTION 2: CHANNEL CONNECTION IN TRANSPARENT MODE

Two bytes are needed:

1) The first byte contains the number of the channel.

2) The second byte contains information about the attenuation level to be applied to that channel and the opcode (0011).

PCM data of this channel is not added to any conference and it is transferred to the PCM output. It is not affected by the tone control pins.

Instruction 2 Format

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	X	X	X	C4	C3	C2	C1	C0
0	1	1	0	A1	A0	X	X	0	0	1	1

INSTRUCTION 3: CHANNEL DISCONNECTION

Two bytes are needed:

1) The first word contains the number of the channel to be disconnected.
2) The second word contains the opcode (1111).
One time frame must exist between disconnection and connection of the same channel.

Instruction 3 Format

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	X	X	X	C4	C3	C2	C1	C0
0	1	1	0	X	X	X	X	1	1	1	1

M116 INSTRUCTION SET (continued)

INSTRUCTION 4: OVERFLOW INFORMATION

Two bytes are needed to know the status of all 10 conferences: C/$\overline{D}$ = 0 reads the first byte (first 8 conferences) and C/$\overline{D}$ = 1 reads the second byte (the last 2 conferences). A conference is in overflow when the corresponding bit is high.

Instruction 4 Format

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1
0	0	1	1	X	X	X	X	X	X	CF10	CF9

CF10 – CF1: Conference in overflow when high.
nb: as long as $\overline{RD}$ remains low, the overflow status of the conference selected by C/$\overline{D}$ can be monitored in real time.

INSTRUCTION 5: OPERATING MODE

The single byte needed contains the Extra bit (D6), the format bits F1–F0 (D5–D4) and the opcode (0101).
The E bit must be E = 1 when the PCM frame contains a number of bit multiple of eight plus on bit (ex. PCM frame at 1544Kbit/s). Normally E = 0. The bits F1–F0 select the kinds of PCM format byte according table 1. After Reset the default values corresponds to F1 = 0, F0 = 1 if A–law is selected and F1 = 1, F0 = 1 if Mu–law is selected. All channels must be disconnected when the Operating Mode Instruction is sent. They must remain disconnected for at least two time frames after the instruction was sent.
We recommende to use this instruction right after the RESET (see pin $\overline{RESET}$ decription).

Instruction 5 Format

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	X	E	F1	F0	0	1	0	1

E: Extra bit insertion (active when E = 1)
F1 – F0: PCM byte Format selection (see also table 1)
00 = no bit inverted
01 = even bit (B0–B2–B4–B6) inverted
10 = odd bit (B1–B3–B5) inverted
11 = all bit (B0–B1–B2–B3–B4–B5–B6) inverted

INSTRUCTION 6: STATUS

Three bytes are needed:

1) The first byte contains the number of the channel;
2) The second byte contains the opcode (0110);
3) By a reding cycle you extract from the third byte the information about the operating mode of the channel (no connection or transparent mode or number of the conference, bits D4–D7); the attenuation (D2–D3) and noise suppression values (D0–D1) eventually inserted.
This reading cycle must be executed at least one frame after the end of the opcode writing cycle.

Instruction 6 Format

Control Signal				Data Bus							
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	X	X	X	C4	C3	C2	C1	C0
0	1	1	0	X	X	X	X	0	1	1	0
0	0	1	1	P3	P2	P1	P0	A1	A0	T1	T0

P3–P0: channel mode operation information
0000 = no connection
1111 = transparent mode
1010 – 0001 = conference mode

P3–P0 give the number of the conferenc

nb: the instruction 6 enables the dat bus to read the status until reset by C/D = 0 and WR = 1.

Table 1 : PCM Byte Format. B7 (sign–bit) is the MSB and B0 is the LSB. F1–F0 corresponds to D5–D4 in the byte of the Operating Mode Instruction (instruction 5).

F1	F0		B7	B6	B5	B4	B3	B2	B1	B0
0	0	+FULL SCALE	1	1	1	1	1	1	1	1
		MIN LEVELS	1	0	0	0	0	0	0	0
			0	0	0	0	0	0	0	0
		–FULL SCALE	0	1	1	1	1	1	1	1
0	0	+FULL SCALE	1	0	1	0	1	0	1	0
		MIN LEVELS	1	1	0	1	0	1	0	1
			0	1	0	1	0	1	0	1
		–FULL SCALE	0	0	1	0	1	0	1	0
1	0	+FULL SCALE	1	1	0	1	0	0	0	0
		MIN LEVELS	1	0	1	0	1	1	1	1
			0	0	1	0	1	1	1	1
		–FULL SCALE	0	1	0	1	0	0	0	0

Figure 11: Overflow Control with µP Interactive Procedure

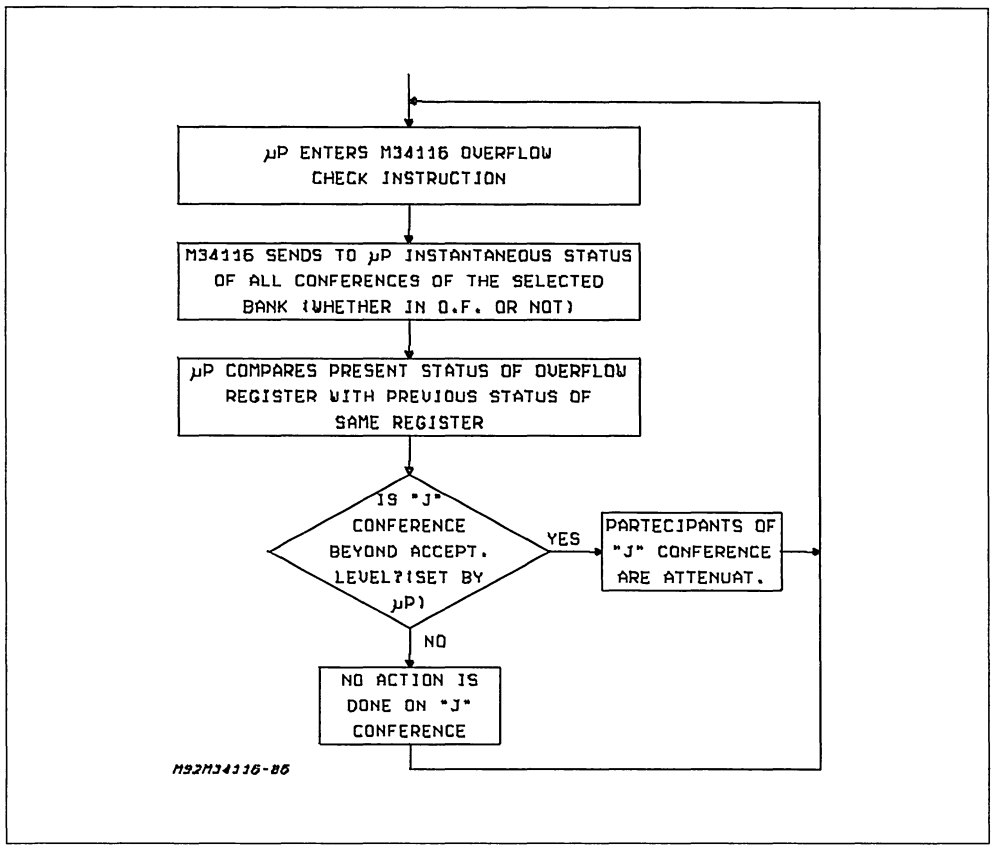
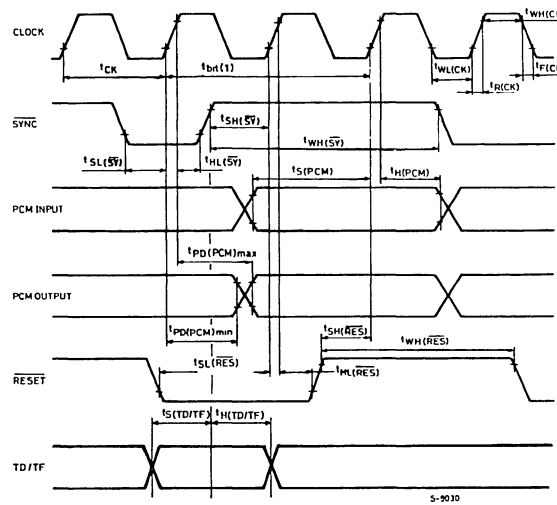


Figure 12: $\overline{\text{SYNC}}$, PCM I/O, $\overline{\text{RESET}}$, TD/TF Timings



(1) t_{bit} corresponds to bit 0, channel 0 or Extra Bit.

Figure 13: WRITE Operating Timing.

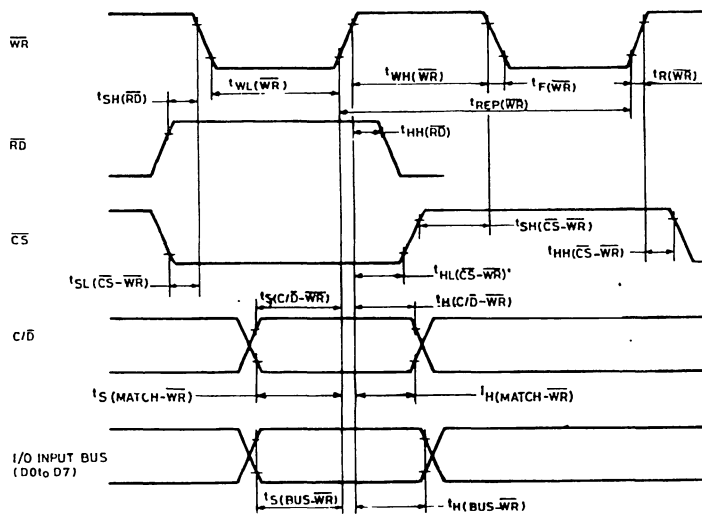


Figure 14: READ Operating Timing.

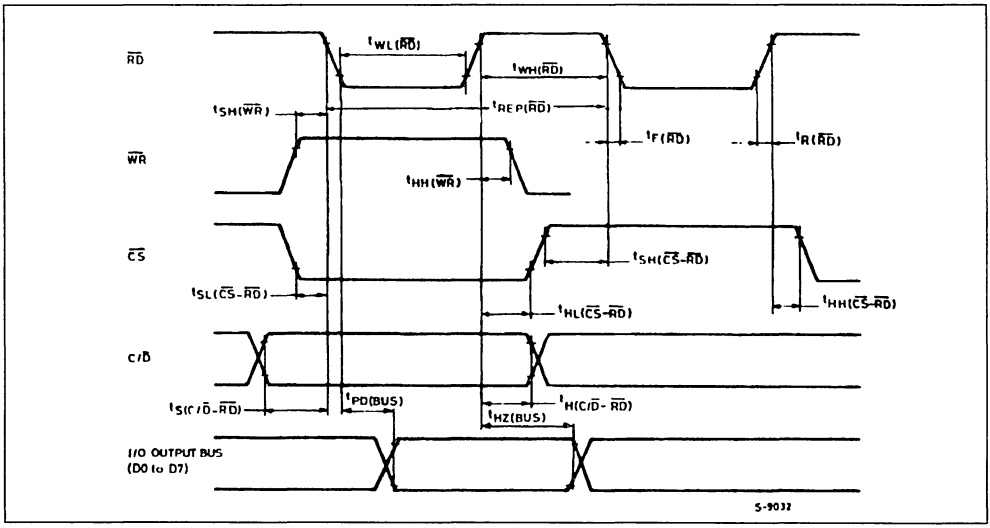


Figure 15: RC (External Clock) and $\overline{OS}$ (Overflow Signalling) Timings.

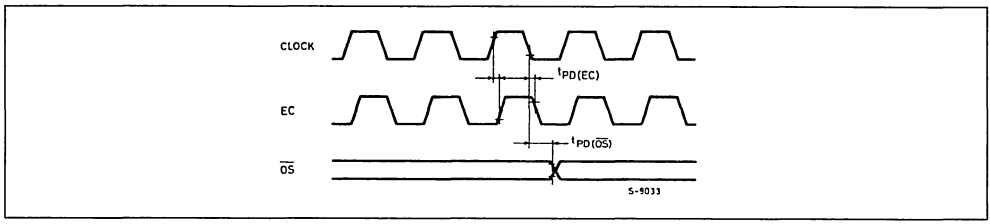


Figure 16: EC Timing with Extra Bit Operating Mode Insert.

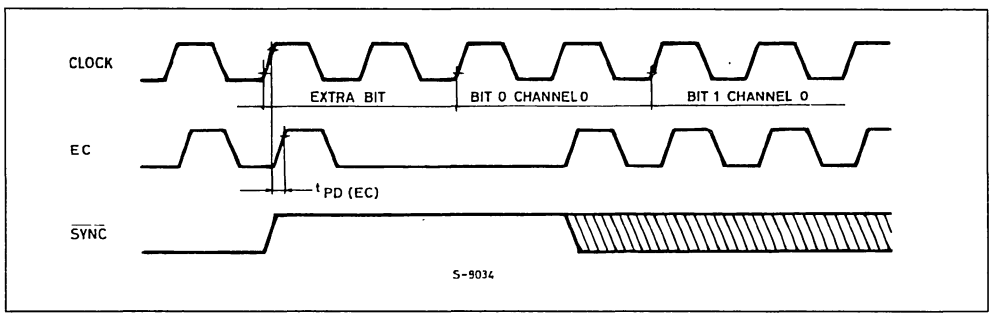
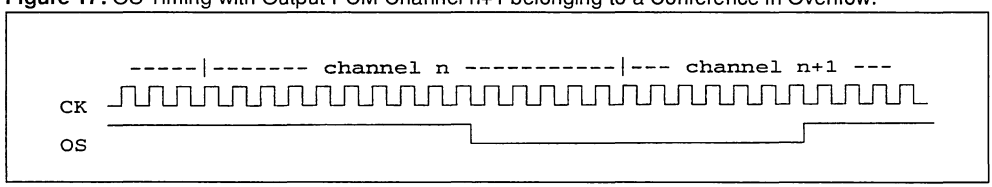


Figure 17: $\overline{OS}$ Timing with Output PCM Channel n+1 belonging to a Conference in Overflow.



APPENDIX 1A - Correspondance between S7-S0 values (HEX) and synthetized frequency for melody and tone 1-6:

00	SILENCE	40	500.00	80	1000.00	C0	2000.00
01	253.91	41	507.81	81	1015.62	C1	2031.25
02	257.81	42	515.62	82	1031.25	C2	2062.50
03	261.72	43	523.44	83	1046.88	C3	2093.75
04	265.62	44	531.25	84	1062.50	C4	2125.00
05	269.53	45	539.06	85	1078.12	C5	2156.25
06	273.44	46	546.88	86	1093.75	C6	2187.50
07	277.34	47	554.69	87	1109.38	C7	2218.75
08	281.25	48	562.50	88	1125.00	C8	2250.00
09	285.16	49	570.31	89	1140.62	C9	2281.25
0A	289.06	4A	578.12	8A	1156.25	CA	2312.50
0B	292.97	4B	585.94	8B	1171.88	CB	2343.75
0C	296.88	4C	593.75	8C	1187.50	CC	2375.00
0D	300.78	4D	601.56	8D	1203.12	CD	2406.25
0E	304.69	4E	609.38	8E	1218.75	CE	2437.50
0F	308.59	4F	617.19	8F	1234.38	CF	2468.75
10	312.50	50	625.00	90	1250.00	D0	2500.00
11	316.41	51	632.81	91	1265.62	D1	2531.25
12	320.31	52	640.62	92	1281.25	D2	2562.50
13	324.22	53	648.44	93	1296.88	D3	2593.75
14	328.12	54	656.25	94	1312.50	D4	2625.00
15	332.03	55	664.06	95	1328.12	D5	2656.25
16	335.94	56	671.88	96	1343.75	D6	2687.50
17	339.84	57	679.69	97	1359.38	D7	2718.75
18	343.75	58	687.50	98	1375.00	D8	2750.00
19	347.66	59	695.31	99	1390.62	D9	2781.25
1A	351.56	5A	703.12	9A	1406.25	DA	2812.50
1B	355.47	5B	710.94	9B	1421.88	DB	2843.75
1C	359.38	5C	718.75	9C	1437.50	DC	2875.00
1D	363.28	5D	726.56	9D	1453.12	DD	2906.25
1E	367.19	5E	734.38	9E	1468.75	DE	2937.50
1F	371.09	5F	742.19	9F	1484.38	DF	2968.75
20	375.00	60	750.00	A0	1500.00	E0	3000.00
21	378.91	61	757.81	A1	1515.62	E1	3031.25
22	382.81	62	765.62	A2	1531.25	E2	3062.50
23	386.72	63	773.44	A3	1546.88	E3	3093.75
24	390.62	64	781.25	A4	1562.50	E4	3125.00
25	394.53	65	789.06	A5	1578.12	E5	3156.25
26	398.44	66	796.88	A6	1593.75	E6	3187.50
27	402.34	67	804.69	A7	1609.38	E7	3218.75
28	406.25	68	812.50	A8	1625.00	E8	3250.00
29	410.16	69	820.31	A9	1640.62	E9	3281.25
2A	414.06	6A	828.12	AA	1656.25	EA	3312.50
2B	417.97	6B	835.94	AB	1671.88	EB	3343.75
2C	421.88	6C	843.75	AC	1687.50	EC	3375.00
2D	425.78	6D	851.56	AD	1703.12	ED	3406.25
2E	429.69	6E	859.38	AE	1718.75	EE	3437.50
2F	433.59	6F	867.19	AF	1734.38	EF	3468.75
30	437.50	70	875.00	B0	1750.00	F0	3500.00
31	441.41	71	882.81	B1	1765.62	F1	3531.25
32	445.31	72	890.62	B2	1781.25	F2	3562.50
33	449.22	73	898.44	B3	1796.88	F3	3593.75
34	453.12	74	906.25	B4	1812.50	F4	3625.00
35	457.03	75	914.06	B5	1828.12	F5	3656.25
36	460.94	76	921.88	B6	1843.75	F6	3687.50
37	464.84	77	929.69	B7	1859.38	F7	3718.75
38	468.75	78	937.50	B8	1875.00	F8	3750.00
39	472.66	79	945.31	B9	1890.62	F9	3781.25
3A	476.56	7A	953.12	BA	1906.25	FA	3812.50
3B	480.47	7B	960.94	BB	1921.88	FB	3843.75
3C	484.38	7C	968.75	BC	1937.50	FC	3875.00
3D	488.28	7D	976.56	BD	1953.12	FD	3906.25
3E	492.19	7E	984.38	BE	1968.75	FE	3937.50
3F	496.09	7F	992.19	BF	1984.38	FF	3968.75

APPENDIX 1B - Correspondence between S7-S0 values (HEX) and synthetized frequency for tone 7:

0	SILENCE	40	500.00	80	1000.00	c0	2000.00
1	3.91	41	507.81	81	1015.62	c1	2031.25
2	7.81	42	515.62	82	1031.25	c2	2062.50
3	11.72	43	523.44	83	1046.88	c3	2093.75
4	15.62	44	531.25	84	1062.50	c4	2125.00
5	19.53	45	539.06	85	1078.12	c5	2156.25
6	23.44	46	546.88	86	1093.75	c6	2187.50
7	27.34	47	554.69	87	1109.38	c7	2218.75
8	31.25	48	562.50	88	1125.00	c8	2250.00
9	35.16	49	570.31	89	1140.62	c9	2281.25
a	39.06	4a	578.12	8a	1156.25	ca	2312.50
b	42.97	4b	585.94	8b	1171.88	cb	2343.75
c	46.88	4c	593.75	8c	1187.50	cc	2375.00
d	50.78	4d	601.56	8d	1203.12	cd	2406.25
e	54.69	4e	609.38	8e	1218.75	ce	2437.50
f	58.59	4f	617.19	8f	1234.38	cf	2468.75
10	62.50	50	625.00	90	1250.00	d0	2500.00
11	66.41	51	632.81	91	1265.62	d1	2531.25
12	70.31	52	640.62	92	1281.25	d2	2562.50
13	74.22	53	648.44	93	1296.88	d3	2593.75
14	78.12	54	656.25	94	1312.50	d4	2625.00
15	82.03	55	664.06	95	1328.12	d5	2656.25
16	85.94	56	671.88	96	1343.75	d6	2687.50
17	89.84	57	679.69	97	1359.38	d7	2718.75
18	93.75	58	687.50	98	1375.00	d8	2750.00
19	97.66	59	695.31	99	1390.62	d9	2781.25
1a	101.56	5a	703.12	9a	1406.25	da	2812.50
1b	105.47	5b	710.94	9b	1421.88	db	2843.75
1c	109.38	5c	718.75	9c	1437.50	dc	2875.00
1d	113.28	5d	726.56	9d	1453.12	dd	2906.25
1e	117.19	5e	734.38	9e	1468.75	de	2937.50
1f	121.09	5f	742.19	9f	1484.38	df	2968.75
20	125.00	60	750.00	a0	1500.00	e0	3000.00
21	128.91	61	757.81	a1	1515.62	e1	3031.25
22	132.81	62	765.62	a2	1531.25	e2	3062.50
23	136.72	63	773.44	a3	1546.88	e3	3093.75
24	140.62	64	781.25	a4	1562.50	e4	3125.00
25	144.53	65	789.06	a5	1578.12	e5	3156.25
26	148.44	66	796.88	a6	1593.75	e6	3187.50
27	152.34	67	804.69	a7	1609.38	e7	3218.75
28	156.25	68	812.50	a8	1625.00	e8	3250.00
29	160.16	69	820.31	a9	1640.62	e9	3281.25
2a	164.06	6a	828.12	aa	1656.25	ea	3312.50
2b	167.97	6b	835.94	ab	1671.88	eb	3343.75
2c	171.88	6c	843.75	ac	1687.50	ec	3375.00
2d	175.78	6d	851.56	ad	1703.12	ed	3406.25
2e	179.69	6e	859.38	ae	1718.75	ee	3437.50
2f	183.59	6f	867.19	af	1734.38	ef	3468.75
30	187.50	70	875.00	b0	1750.00	f0	3500.00
31	191.41	71	882.81	b1	1765.62	f1	3531.25
32	195.31	72	890.62	b2	1781.25	f2	3562.50
33	199.22	73	898.44	b3	1796.88	f3	3593.75
34	203.12	74	906.25	b4	1812.50	f4	3625.00
35	207.03	75	914.06	b5	1828.12	f5	3656.25
36	210.94	76	921.88	b6	1843.75	f6	3687.50
37	214.84	77	929.69	b7	1859.38	f7	3718.75
38	218.75	78	937.50	b8	1875.00	f8	3750.00
39	222.66	79	945.31	b9	1890.62	f9	3781.25
3a	226.56	7a	953.12	ba	1906.25	fa	3812.50
3b	230.47	7b	960.94	bb	1921.88	fb	3843.75
3c	234.38	7c	968.75	bc	1937.50	fc	3875.00
3d	238.28	7d	976.56	bd	1953.12	fd	3906.25
3e	242.19	7e	984.38	be	1968.75	fe	3937.50
3f	246.09	7f	992.19	bf	1984.38	ff	3968.75

APPENDIX 2

TONE GENERATION PROGRAMMING

Example 1:

f = 425Hz

Duration 200ms ON, 200ms OFF, 600ms ON, 1000ms OFF

Attenuation 10dB

Channel #0.

Programming sequence:

Control Signal				Data
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7 . . . . D0
0	1	0	0	0AH
0	1	0	0	00H
0	1	1	0	0CH
0	1	0	0	2DH
0	1	0	0	06H
0	1	0	0	00H
0	1	0	0	06H
0	1	0	0	2DH
0	1	0	0	12H
0	1	0	0	00H
0	1	0	0	1FH
0	1	1	0	0CH

Example 2:

f = 400Hz

Duration: 375ms ON, 375ms OFF

Attenuation 5dB

Channel #3

Programming sequence:

Control Signal				Data
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7 . . . . D0
0	1	0	0	05H
0	1	0	0	03H
0	1	1	0	0CH
0	1	0	0	26H
0	1	0	0	0CH
0	1	0	0	00H
0	1	0	0	0CH
0	1	0	0	FFH
0	1	1	0	0CH

SGS-THOMSON MICROELECTRONICS

ST5410

2B1Q U INTERFACE DEVICE

ADVANCE DATA

GENERAL FEATURES

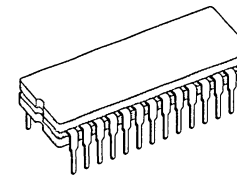
- SINGLE CHIP 2B1Q LINE CODE TRANSCEIVER
- SUITABLE FOR BOTH ISDN AND PAIR GAIN APPLICATIONS
- MEETS OR EXCEEDS ANSI T1.601-1988 U.S. STANDARD
- MEETS OR EXCEEDS ST/LAA/ELR/822 FRENCH SPECIFICATIONS
- SINGLE 5V SUPPLY
- 28 PINS PACKAGE
- 300mW ACTIVE AND 10mW INACTIVE POWER DISSIPATION
- HCMOS3A SGS-THOMSON ADVANCED DOUBLE-METAL SINGLE-POLY CMOS PROCESS

TRANSMISSION FEATURES

- 160 KBIT/S FULL DUPLEX TRANSCEIVER
- 2B1Q LINE CODING WITH SCRAMBLER/DESCRAMBLER
- 18KFT (5.5KM) ON 26AWG/24AWG TWISTED PAIR CABLES
- SUPPORTS BRIDGE TAPS, SPLICES AND MIXED GAUGES
- >70DB ADAPTIVE ECHO-CANCELLATION
- DIGITAL FEEDBACK EQUALIZATION
- ON CHIP TIMING RECOVERY WITHOUT EXTERNAL PRECISION COMPONENTS
- DIRECT CONNECTION TO SMALL LINE TRANSFORMER

SYSTEM FEATURES

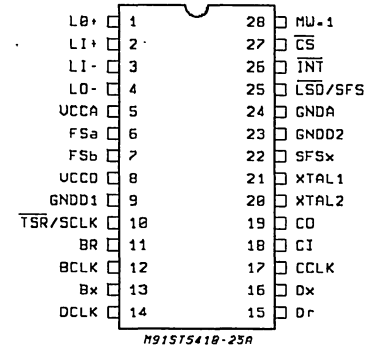
- ACTIVATION/DEACTIVATION CONTROLLER
- ON CHIP CRC CALCULATION AND VERIFICATION INCLUDING PROGRAMMABLE BLOCK ERROR COUNTER
- EOC CHANNEL AND OVERHEAD-BITS TRANSMISSION WITH AUTOMATIC MESSAGE CHECKING
- GCI AND MW/DSI MODULE INTERFACES COMPATIBLE
- DIGITAL LOOPBACKS
- ELASTIC DATA BUFFERS AND BACKPLANE CLOCK DE-JITTERIZER



Ceramic DIP28

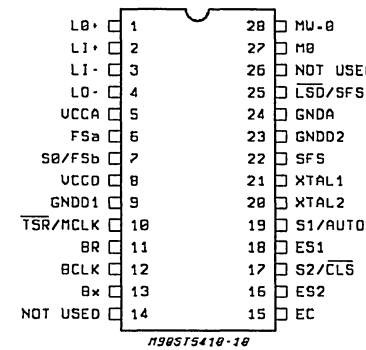
PIN CONNECTIONS (Top views)

MICROWIRE MODE



M91ST5410-25A

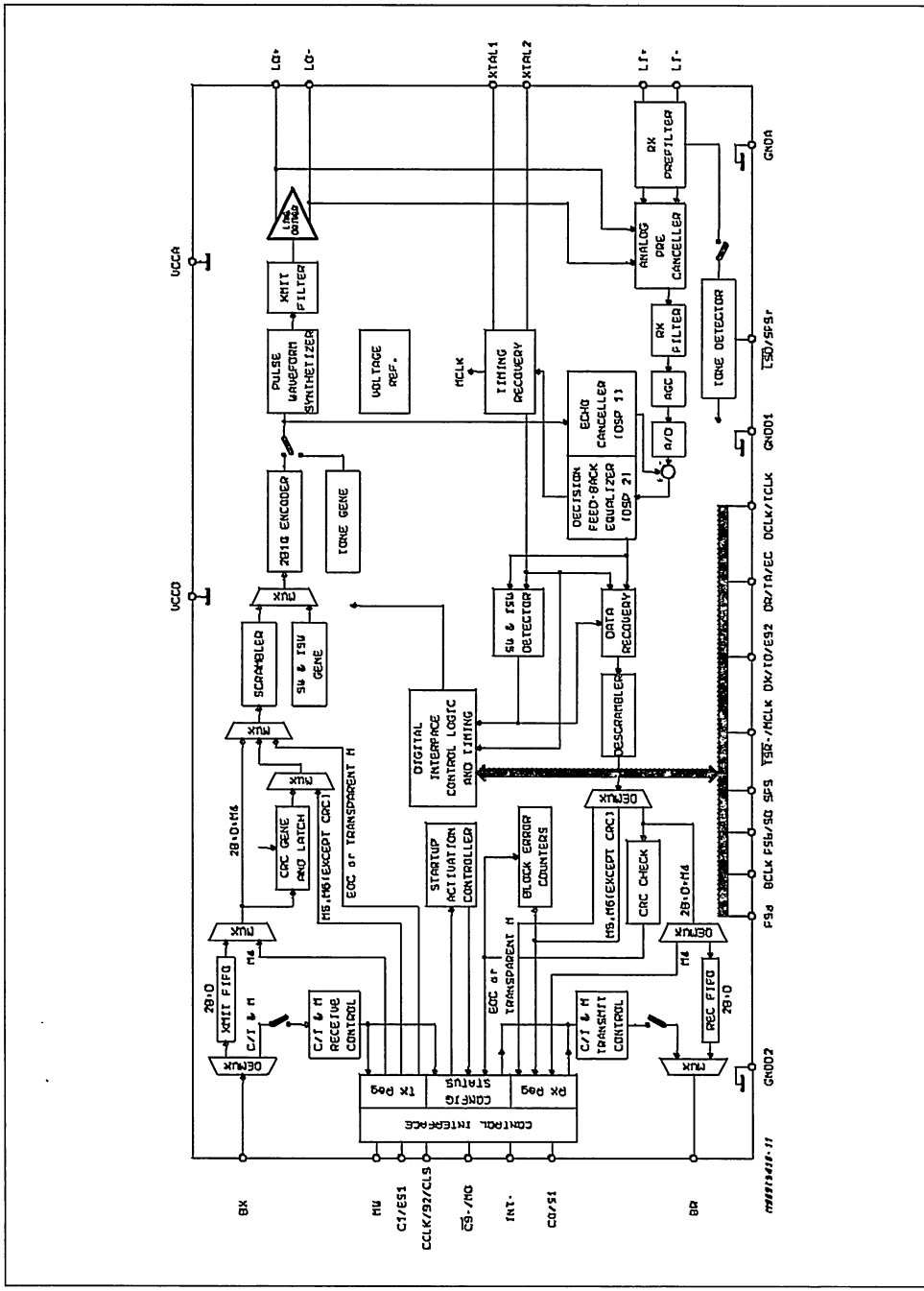
GCI MODE



M90ST5410-10

INDEX

Figure 1: ST5410 Block Diagram.



GENERAL DESCRIPTION

ST5410 is a complete monolithic transceiver for ISDN Basic access data transmission on twisted pair subscriber loops typical of public switched telephone networks. The device is fully compatible with both ANSIT1.601-1988 U.S. and ST/LAA/ELR/822 French specifications.

The equivalent of 160 kbit/s full-duplex transmission on a single twisted pair is provided, according to the formats defined in the a.m. spec. Frames include two B channels, each of 64 kbit/s, one D channel of 16 kbit/s plus an additional 4 kbit/s M channel fcr loop maintenance and other user functions. 12 kbit/s bandwidth is reserved for framing. 2B1Q Line coding is used, where pairs of bits are coded into one of 4 quantum levels. This technique results in a low frequency spectrum (160 kbit/s turn into 80 kband), thereby reducing both line attenuation and crosstalk and achieving long range with low Bit Error Rates.

The system is designed to operate on any of the standard types of cable pairs including mixed gauges (26AWG, 24 AWG and 22 AWG) linking the loop by means of one simple transformer. Good noise margins are achieved even when bridged taps are present. On 26AWG cable, the transmission range is in excess of 5.5 km (18 kft) in presence of crosstalk and noise as specified by ANSI standard. ST 5410 is designed to operate with Bit Error Rate less than 10^{-6} on 45 dB loss loops with near-end Crosstalk (NEXT) of 52 dB as specified in european ETSI recommendation.

To meet these very demanding specifications, the device includes two Digital Signal Processors, one configured as an adaptive Echo-Canceller to cancel the near end echoes resulting from the transmit/recive hybrid interface, the other as an adaptive line equalizer. A Digital Phase-Locked Loop (DPLL) timing recovery circuit is also included that provides in NT1 a 15.36 MHz synchronized clock to the rest of the system. Scrambling and descrambling are performed as specified in the US and French specifications.

On the system side, ST5410 can be linked to two bus configuration simply by pin MW bias.

MICROWIRE(μW)/DSI mode (MW= 5V): 144 kbit/s 2B+D basic access data is transferred on a multiplex Digital System Interface with 4 different interface formats (see fig. 2 and 3) providing maximum flexibility with a limited pin count (BCLK, Bx, Br, FSa, FSb). Three pre-defined 2B+D formats plus an internal time slot assigner allows direct connection of the UID to the most common multiplexed digital interfaces (TDM/IDL). Bit and Frame Synchronisation signals are inputs or outputs depending on the configuration selected. Data buffers allow any phase shift between the line and the digital interface. That permits building of slave-slave configurations e.g. in NT12 trunk-cards.

It is possible to separate the D from the B channels and to transfer it on a separate digital interface (Dx, Dr) using the same bit and frame clocks as for the B channels or in a continuous mode using an internally generated 16 kHz bit clock output (DCLK).

All the Control, Status and Interrupt registers are handled via a control channel on a separate serial interface MICROWIRE compatible (CI, CO, $\overline{CS}$, CCLK, $\overline{INT}$) supported by a number of microcontroller including the ST6, ST9 and COPS families from SGS-THOMSON

GCI mode (MW= 0V). Control/maintenance channels are multiplexed with 2B+D basic access data in a GCI compatible interface format (see fig. 4a) requiring only 4 pins (BCLK, Bx, Br, FSa). On chip GCI channel assignement allows to multiplex on the same bus up to 8 GCI channels, each supporting data and controls of one device. Bit and Frame Synchronisation signals can be inputs or ouputs depending on the configuration selected. Data buffers, again, allow to have any phase between the line interface and the digital interface.

Through the M channel and its protocol allowing to check both direction exchanges, internals register can be configurated, the EOC channel and the Overhead-bits can be monitored. Associated to the M channel, there are A and E channels for enabling the exchanged messages and to insure the flow control. The C/I channel allows the primitive exchanges following the standard protocol.

In both mode (μW and GCI) CRC is calculated and checked in both directions internally.

In LT mode, the superframe can be synchronized by an external signal (SFS) or be self running. In NT mode the SFS is always output synchronized by the transmit superframe.

Line side or Digital Interface side loopbacks can be selected for each B1, B2 or D channel independently without restriction in transparent or in non-transparent mode.

Activation and deactivation procedures, which are automatically processed by UID, require only the exchange of simple commands as Activation Request, Deactivation Request, Activation Indication. Cold and Warm start up procedures are operated automatically without any special instruction.

PIN FUNCTIONS

Pin	Name	Description
1, 4	LO+, LO-	Transmit 2B1Q signal differential outputs to the line transformer. When used with an appropriate 1:1.5 step-up transformer and the proper line interface circuit the line signal conforms to the output specifications in ANSI standard with a nominal pulse amplitude of 2.5 Volts.
2, 3	LI+, LI-	Receive 2B1Q signal differential inputs from the line transformer.
5, 8	VCCD, VCCA	Positive power supply input for the analog and digital sections, which must be +5 Volts +/-5% and must be directly connected together.
6	FSa	When the Digital Interface clocks are selected as inputs, this signal must be a 8 kHz clock input which indicates the start of the frame on the Digital Interface data input pin Bx. In microwire mode two phases between the rising edge of FSa and the first slot of the frame can be selected by means of bit DDM in CR1: Delayed timing mode or non Delayed timing mode. When GCI Format is selected, FSa defines the frame begining for both Tx and Rx directions and non delayed timing mode is automatically selected. When the Digital Interface clocks are selected as outputs, FSa is a 8KHz output pulse conforming with the selected Interface format.
9, 23, 24	GNDD1, GNDD2, GNDA	Negative power supply pins, which must be connected together close to the device. All digital and analog signals are referred to these pins, which are normally at the system Ground.
10	$\overline{\text{TSR}}$	(LT configuration only) This pin is an open drain output normally in the high impedance state which pulls low when B1 and B2 time-slots are active. It can be used to enable the Tristate control of a backplane line-driver.
	MCLK	(NT mode only) 15.36 MHz clock output which is frequency locked to the received line signal (unlike the XTAL pins, it is not freerunning) .
11	Br	Data output: 2B+D basic access data received from the line can be shifted out from the TRISTATE output Br at the BCLK frequency on the rising edges during the assigned time slots. Elsewhere, Br is in the high impedance state. When the D channel port is enabled, only Bl & B2 data is shifted out from Br on the rising edges of BCLK. In Format 4 and GCI mode, data is shifted out at half the BCLK frequency on the transmit rising edges. When GCI mode is selected, 2B+D data is combined with the GCI Control channels and output Br becomes open drain. There is 1.5 period delay between the rising transmit edge and the receive falling edge of BCLK.

PIN FUNCTIONS (Continued)

in	Name	Description
12	BCLK	Bit Clock: This signal determines the data shift rate on the Digital Interface.When slave mode is selected,,BCLK is an input which may be any multiple of 8 kHz from 256 kHz to 6176 kHz. When master mode is selected , BCLK is an output at 256 kHz, 512 kHz, 1536 kHz, 2048 kHz or 2560 kHz depending on the selection in Command Register 1. BLCK is synchronous with FSa/b Frame syncsignals and phase locked to the recovered clock received from the line. In formats 1-3, data is shifted in and out at the BCLK frequency. In format 4 and in GCI mode, data is shifted in and out at half the BCLK frequency.
1 3	Bx	Data input: 2B+D basic access data to transmit to the line can be shifted in at the BCLK frequency on the falling edges during the assigned time-slots. When D channel port is enabled, only B1 & B2 data is shifted in at the BCLK frequency on the falling edges during the assigned time slots. In format 4 and in GCI mode, data is shifted in at half the BCLK frequency on the receive falling edges. When GCI mode is selected, 2B+D data is combined with the GCI Control channels.
20	XTAL2	The output of the crystal oscillator, which should be connected to one end of the crystal, if used. Otherwise, this pin must be left no connected.
21	XTAL1	The master clock input, which requires either a parallel resonance crystal to be tied between this pin and XTAL2, or a logic level clock input from a stable source. This clock does not need to be synchronized to the digital interface clocks (FSa, BCLK).Crystal specifications: 15.36 MHz +/-50ppm parallel resonant; Rs ≤ 20 ohms; load with 33pF to GND each side.
22	SFS	Super Frame synchronization I/O: When LT configuration is selected, the rising edge of SFS indicates the beginning of the Transmit Super Frame on the line. Two modes can be selected. In the first mode, SFS is an input that synchronizes the Transmit Frame counter of the UID core. SFS must be synchronous with FSa but with any phase . In the second mode, SFS is a square wave output issued from the free-running Transmit Frame counter. When NT configuration is selected, SFS is always a square wave output which indicates the beginning of the Transmit Superframe. There is no direct phase-relation between the data on the line and the data on the digital interface.
25	$\overline{\text{LSD}}$	Line Signal Detect output (default conf.): This pin is an open drain output which is normally in the high impedance state but pulls low when the device previously in the power down state receives a wake-up by Tone from the line. This signal is intended to be used to wake-up a micro-controller from a low power idle mode. The $\overline{\text{LSD}}$ output goes back in the high impedance state when the device is powered up.
	SFSr	Super Frame Synchronization output. When LT configuration is selected, it is possible to configurate pin 25 as SFSr that provides a square wave output indicating the beginning of the received Super Frame from the line. As for SFSx, there is no direct phase-relation between the data on the line and the data on the digital interface.
28	MW	MICROWIRE selection: When set high, MICROWIRE control interface is selected. All the internal registers can be accessed through it. When set low, GCI interface is selected. All the internal registers can be accessed through the GCI Monitor and Command/Indicate Control channels.

PIN FUNCTIONS (Specific to MICROWIRE MODE ONLY (MW = 1))

Pin	Name	Description
7	FSb	This is a 8 kHz clock input which define the start of the frame on the Digital Interface data ouput pin Br. Two phases between the rising edge of FSb and the first slot of the frame can be selected with the same command as for FSa; Delayed timing mode or non Delayed timing mode. When the Digital Interface clocks are selected as outputs, FSb is a 8 kHz output pulse conforming with the selected format.
14	DCLK	(D channel port enabled, continuous mode selected) D channel Clock output: when the D channel port is enabled in continuous mode, data are shifted in and out at 16 kHz on the falling and rising edges of DCLK respectively. DCLK is synchronous with the BCLK frequency. When DCLK is disabled, it must be tied to GNDD.
15	Dr	(D channel port enabled) D channel data output: when the D channel port is enabled, D channel data is shifted out from the UID on this pin in two selectable modes: In multiplexed mode, data is shifted out at the BCLK frequency on the rising edges when the assigned time slot is active. In continuous mode, data is shifted out at the DCLK frequency on the rising edge continuously.
16	Dx	(D channel port enabled) D channel data input: When the channel port is enabled, D channel data is shifted in the UID on this pin in two selectable modes: In multiplexed mode, data is shifted in at the BCLK frequency on the falling edges when the selected receive time slots are active. In continuous mode, data is shifted in at the DCLK frequency on the falling edge continuously. When the D channel port is disabled, Dx must be tied to GNDD.
17	CCLK	Clock input for the MICROWIRE control channel: data is shifted in and out on the rising and falling edges of CCLK respectively. CCLK may be asynchronous with the digital interface clock.
18	CI	MICROWIRE control channel serial input: two bytes data is shifted into the UID on this pin on the rising edges of CCLK.
19	CO	MICROWIRE control channel serial output: two bytes data is shifted out from the UID on the falling edges of CCLK. When not enabled by $\overline{CS}$, CO is high-impedance.
26	$\overline{INT}$	Interrupt output: Latched open-drain output signal which is normally high impedance and goes low to request a read cycle. Pending interrupt data is shifted out from CO at the following read-write cycle. Several pending interrupts may be queued internally and may provide several interrupt requests. $\overline{INT}$ is freed upon receiving of $\overline{CS}$ low and can goes low again when $\overline{CS}$ is freed.
27	$\overline{CS}$	Chip Select input: When this pin is pulled low, data can be shifted in and out from the UID through CI & CO pins. When high, this pin inhibits the MICROWIRE interface. For normal read or write operation, $\overline{CS}$ has to be pulled low for 16 CCLK periods of time.

PIN FUNCTIONS (Specific to GCI MODE ONLY (MW = 0))

Pin	Name	Description
15	EC	External Control Output: controlled by the bit LEC in the TxM56 register.
18, 16	ES1,ES2	External Status inputs: during full synchronization the status of ES1, ES2 is loaded in the LES1, LES2 bits of the RxM56 register at each status change and an interrupt is issued. In NT mode, with AUTOE = 1, ES1/ES2 status are automatically sent on the line as ps1/ps2.
27	M0	GCI clocks I/O selection: when M0 is set low, BCLK and FSa clocks are inputs. BCLK can have any value between 512 kHz and 6176 kHz. GCI is selected in slave mode. When M0 is set high, BCLK and FSa clocks are outputs. FSa is a 8 kHz clock signal while BCLK is a 512 kHz or a 1536 kHz depending on CLS pin polarization. GCI channel 0 is automatically selected.In addition, when M0 is set high, NT configuration is also selected. When M0 is set low, NT or LT configuration must be selected through Configuration Register 2.
7,19,17	S0/FSb, S1/AUTOE, S2/CLS	(M0 = 0: slave mode) GCI number selection: these 3 pins S0, S1, S2 are significant when GCI is selected in slave mode only. A GCI channel constituted of 32 bits and relative to one basic access can be multiplexed on Bx and Br links used as a serial bus for several devices. The channel number selection among 8 available GCI channels is made by programming the S0-S2 pins. (M0 = 1: master mode) S0 becomes FSb (output pulse indicating 2nd 64Kbit time slot.) S1 becomes AUTOE (input) S2 becomes $\overline{CLS}$ (input) GCI Clock Selection: while M0 is set high, $\overline{CLS}$ high selects the 1536 kHz frequency on BCLK and $\overline{CLS}$ low selects the 512 kHz frequency on BCLK.

FUNCTIONAL DESCRIPTION

Digital Interfaces

ST5410 provides a choice between two types of digital interface for both control data and (2 B + D) basic access data.

These are:
a) General Circuit Interface: GCI.
b) Microwire/Digital System Interface: µW/DSI

The device will automatically switch to one of them by sensing the MW input pin at the Power up.

µW/DSI MODE

Microwire control interface

The MICROWIRE interface is enabled when pin MW equal one. Internal registers can be written or read through that control interface.
It is constituted of 5 pins:

CI: data in
CO: data ouput
CCLK:data clock input
$\overline{CS}$: Chip Select input
$\overline{INT}$: Interruption output

Transmission of data onto CI & CO is enabled when $\overline{CS}$ input is low.

A Write cycle or a Read cycle is always constituted of two bytes. CCLK must be pulsed 16 times while $\overline{CS}$ is low. Data on the CI input is shifted into the serial Receive input register on the rising edge of each CCLK pulse. At the same time, data from the Transmit output register is shifted out onto the CO ouput on the falling edge of each CCLK pulse. The bit 7 (the first) is available as soon as $\overline{CS}$ goes low.

You can write in the UID on CI while the UID send back a register content to the microprocessor. If the UID has no message to send, it forces the CO output to all zero's.

If the UID is to be read (status change has occured in the UID or a read-back cycle has been requested by the controller), it pulls the $\overline{INT}$ output low until $\overline{CS}$ is provided. $\overline{INT}$ high to low transition is not allowed when $\overline{CS}$ is low (the UID waits for $\overline{CS}$ high if a pending interrupt occurs while $\overline{CS}$ is low) .

When $\overline{CS}$ is high, the CO pin is in the high impedance state.

Note: Special format is used for EOC channels.

Write cycle

The format to write a message into the UID is:

A7	A6	A5	A4	A3	A2	A1	A0

1st byte

D7	D6	D5	D4	D3	D2	D1	D0

2nd byte

A7-A1: Register Adress
A0: Write/Read Indicator
D7-D0: Register Content

After the first byte is shifted in, Register address is decoded. A0 set low indicates a write cycle: the content of the following received byte has to be loaded into the adressed register.
A0 set high indicates a read-back cycle request and the byte following is not significant. The UID will respond to the request with an interrupt cycle. It is than possible for the micro to receive the required register content after several other pending interrupts.

Read cycle

When UID has a register content to send to the microprocessor, it pulls low the $\overline{INT}$ output to request $\overline{CS}$ and CCLK signals. Note that the data to send can be the content of a Register previously requested by the microprocessor by means of a read-back request.

The format of the message sent by the UID is:

A7	A6	A5	A4	A3	A2	A1	A0

1st byte

D7	D6	D5	D4	D3	D2	D1	D0

2nd byte

A7-A1: Register Adress
A0: forced to 1 if read back
forced to 0 if spontaneous
D7-D0: Register Content

Digital System Interface

Two B channels, each at 64 kbit/s and one D channel at 16 kbit/s form the Basic access data. Basic access data is transferred on the Digital System Interface with several different formats selectable by means of the configuration register CRI.
The DSI is basically constituted of 5 wires (see fig.2 and 3):

BCLK bit clock
Bx data input to transmit to the line
Br data output received from the line
FSa Transmit Frame sync
FSb Receive Frame sync

It is possible to separate the D channel from the B channels and to transfer it on a separate Digital Interface constituted of 2 pins:

Dx D channel data input
Dr D channel data ouput

The multiplexed mode uses the same bit and frame clocks as for the B channels. The continuous mode

uses an internally generated 16 kHz bit clock output:

DCLK D channel clock output.

ST5410 provides a choice of four multiplexed formats for the B and D channels data as shown in fig.2 and 3.

Format 1: the 2B+D data transfer is assigned to the first 18 bits of the frame on Br and Bx I/0 pins. Channels are assigned as follows: B1(8 bits), B2(8 bits), D(2 bits), with the remaining bits ignored until the next Frame sync pulse.

Format 2: the 2B+D data transfer is assigned to the first 19 bits of the frame on Br and Bx I/O pins. Channels are assigned as follows: B1(8 bits), D(1 bit), 1 bit ignored, B2(8 bits), D(1 bit), with the remaining bits ignored until the next frame sync pulse.

Format 3: B1 and B2 Channels can be independently assigned to any 8 bits wide time slot among 64 (or less) on the Bx and Br pins. The transmit and receive directions are also independent. When multiplexed mode is selected, the D channel can be assigned to any 2 bits wide time slot among 256 on the Bx and Br pins or on the Dx and Dr pins (D port disabled or enabled in multiplexed mode continuous respectively).

Format 4: is a GCI like format excluding Monitor channel and C/I channel. The 2B+D data transfer is assigned to the first 26 bits of the frame on Br and Bx I/O pins. Channels are assigned as follows. B1(8 bits) B2(8 bits), 8 bits ignored, D(2 bits), with remaining bits ignored up to the next frame sync pulse.

For all formats when D channel part is enabled "continuous mode" is possible. When the D channel port is enabled in multiplexed mode, only the 2 B channels use the Bx and Br pins. D bits are assigned according to the related format.

When the Digital Interface clocks are selected as inputs, FSa must be a 8 kHz clock input which indicates the start of the frame on the data input pin Bx. When the Digital Interface clocks are selected ae outputs, FSa is an 8 kHz output pulse conforming to the selected format which indicates the frame beginning for both Tx and Rx directions.

When the Digital Interface clocks are selected as inputs, FSb is a 8 kHz clock input which defines the start of the frame on the data ouput pin Br. When the Digital Interface clocks are selected as outputs, FSb is a 8 kHz output pulse indicating the second 64Kbit slot.

Two phase-relations between the rising edge of FSa/FSb and the first (or second for FSb as output) slot of the frame can be selected depending on format selected: Delayed timing mode or non Delayed timing mode.

Non delayed data mode is similar to long frame timing on the COMBOI/II series of devices: The first bit of the frame begins nominally coincident with the rising edge of FSa/b. When output, FSa is coincident with the first 8 bits wide time-slot while FSb is coincident with the second 8 bits wide time-slot. Non delayed mode is not available in format 2.

Delayed timing mode, which is similar to short frame sync timing on COMBO I/II, in which the FSa/b input must be set high at least a half cycle of BCLK earlier the frame beginning. When output, Fsa (1bit wide pulse) indicates the first 8 bits time-slot beginning while FSb indicates the second. Delayed mode is not available in format 4.

2B+D basic access data to transmit to the line can be shifted in at the BCLX frequency on the falling edges during the assigned time-slots. When D channel port is enabled, only B1 & B2 data is shifted in during the assigned time slots. In format 4, data is shifted in at half the BCLK frequency on the receive falling edges.

2B+ D basic access data received from the line can be shifted out from the Br output at the BCLK frequency on the rising edges during the assigned time-slots. Elsewhere, Br is in the high impedance state. When the D channel port is enabled, only B1 & B2 data is shifted out from Br. In Format 4, data is shifted out at half the BCLK frequency on the transmit rising edges; there is 1.5 period delay between the rising transmit edge and the receive falling edge of BCLK.

Bit Clock BCLK determines the data shift rate on the Digital Interface. Depending on mode selected, BCLK is an input which may be any multiple of 8 kHz from 256 kHz to 6176 kHz or an output at a frequency depending on the format and the frequency selected. Possible frequencies are:

256 KHz, 512 KHz, 1536 KHz,
2048 KHz, 2560 KHz.

In format 4 the use of 256kHz is forbidden.

BCLK is synchronous with FSa/b frame sync signal. When output, BCLK is phased locked to the recovered clock received from the line.

Figure 2: DSI interface formats: MASTER mode.

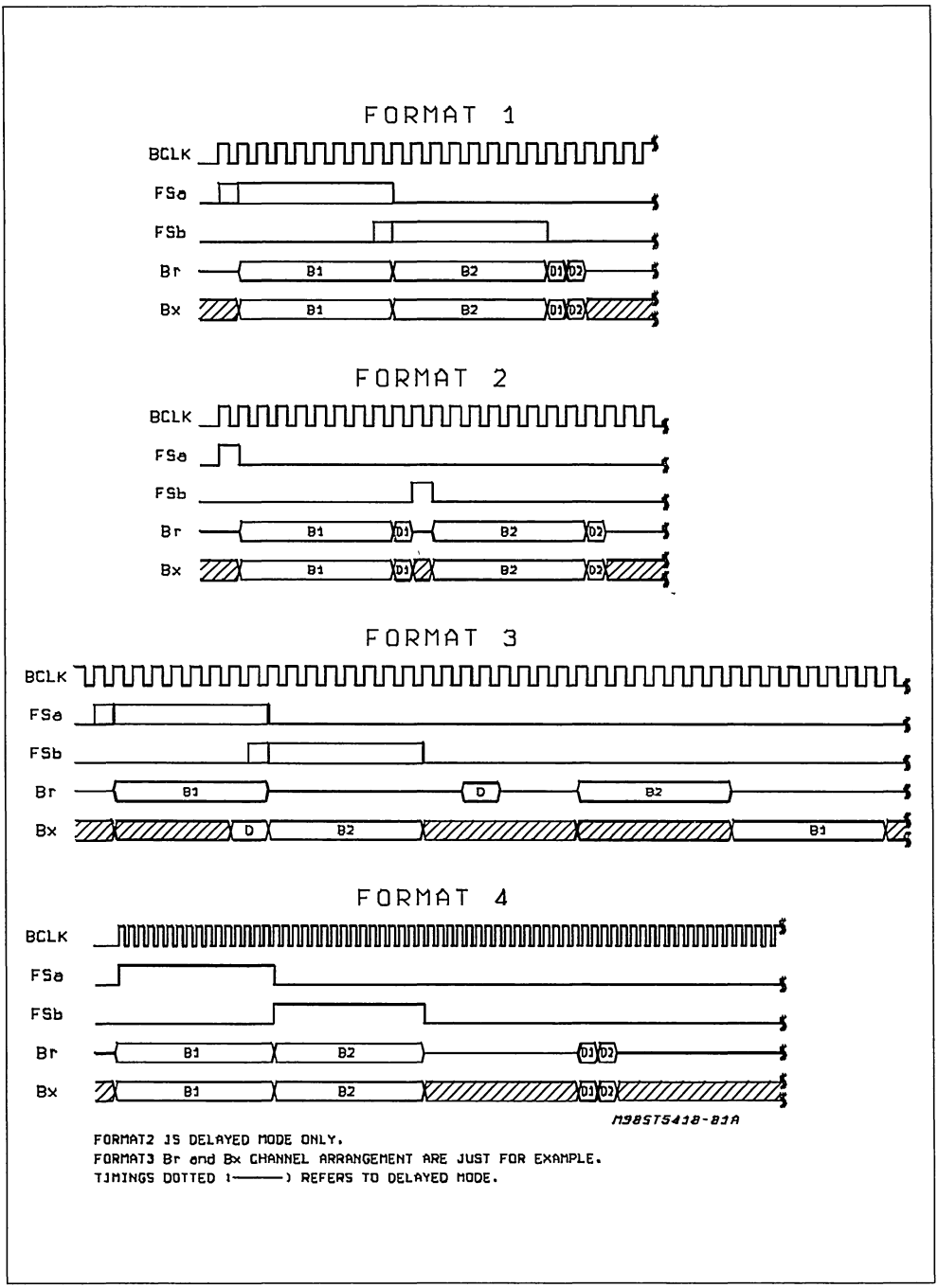
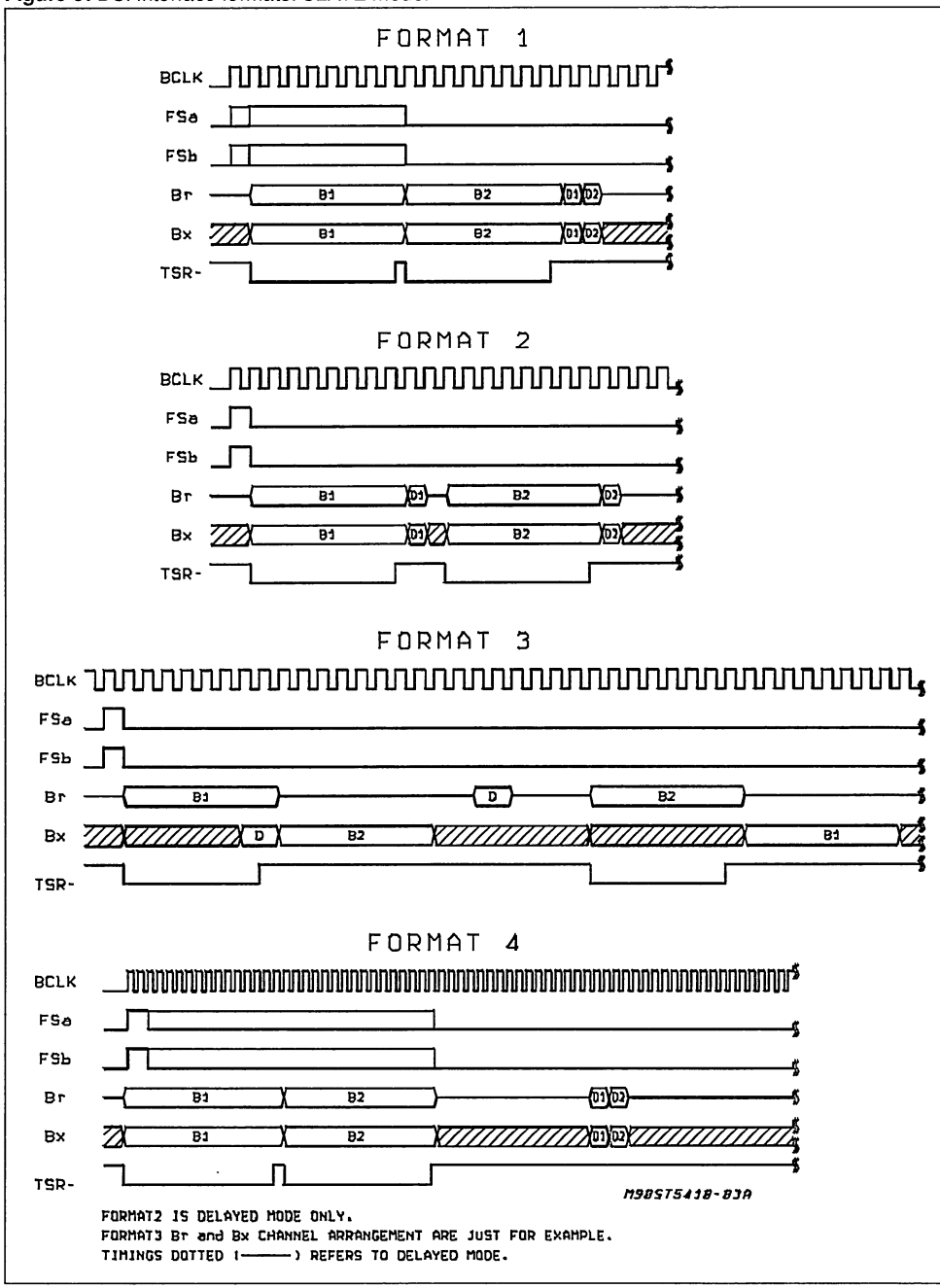


Figure 3: DSI interface formats: SLAVE mode.



GCI MODE

The GCI is a standard interface for the interconnection of dedicated ISDN components in the different equipments of the subscriber loop :
In a Terminal, GCI interlinks the S interface transceiver, the ISDN layer 2 (LAPD) controller and the voice/data processing components as an audio-processor or a Terminal Adaptor module.

In NT1-2, PABX subscriber line card, or central office line card (LT), GCI interlinks the UID, the ISDN Layer 2 (LAPD) controllers and eventually the backplane where the channels are multiplexed.

Frame Structure

2B+D data and control interface is transferred in a time-division multiplexed mode based on 8 kHz frame structure and assigned to four octets per frame and direction.(see fig.4a).
The 64 kbit/s channels B1 and B2 are conveyed in the first two octets; the third octet (M: Monitor) is used for transferring most of the control and status registers; the fourth octet (SC: Signalling & Control) contains the two D channel bits, the four C/I (command/Indicate) bits controlling the activation/deactivation procedures, and the E & A bits which support the handling of the Monitor channel.
These four octets per frame serving one ISDN

Figure 4a: GCI interface format.

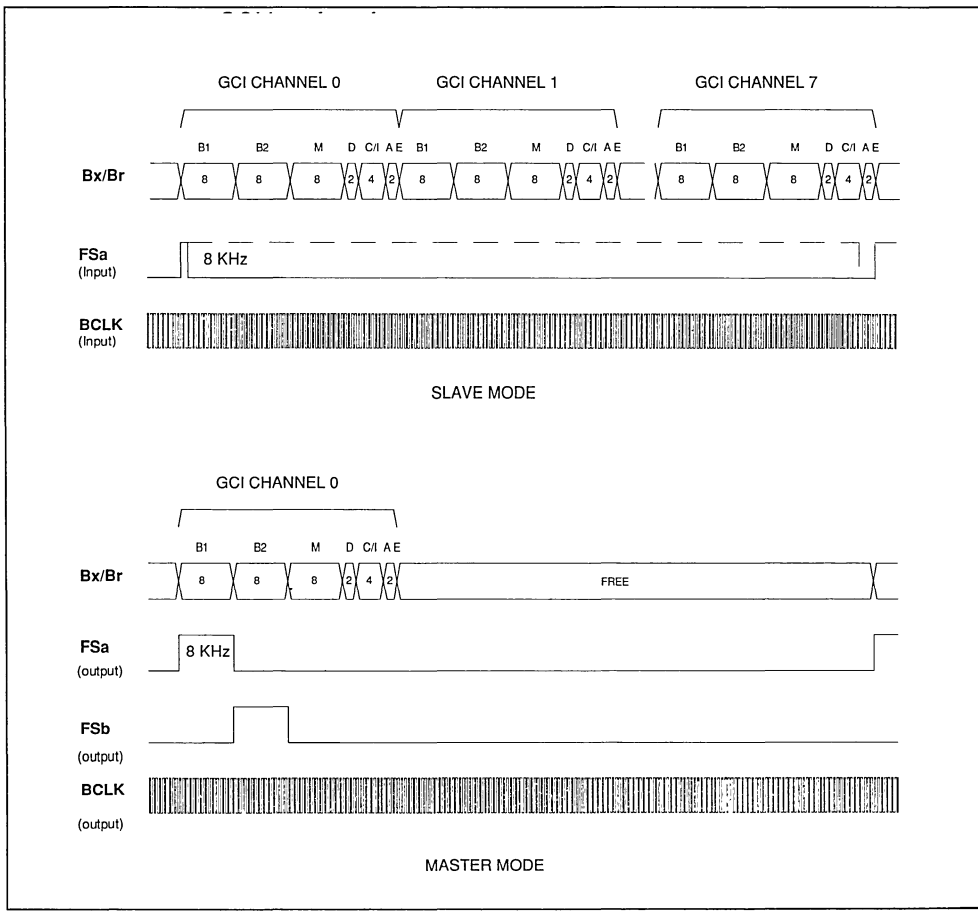
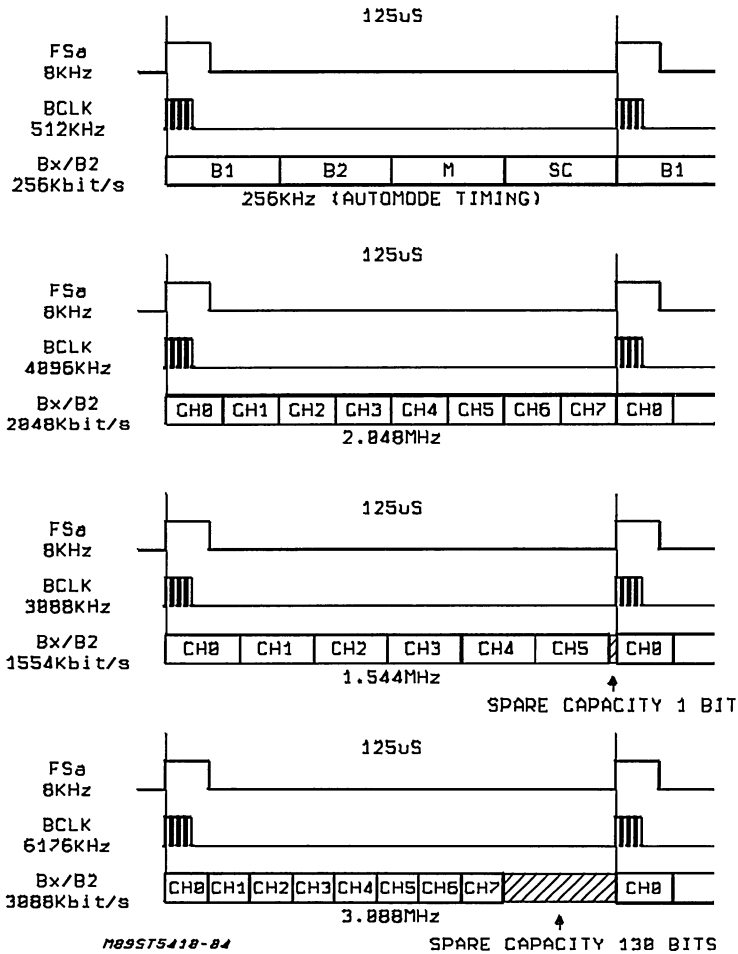


Figure 4b: GCI Multiplex Examples.



subscribers line form a GCI Channel. One GCI channel calls for a bit rate of 256 kbit/s.

In NT1-2s or subscriber Line Cards up to 8 GCI channels may be carried in a frame of a GCI multiplex. The bit rate of a GCI multiplex may be from 256 kbit/s and up to 3088 kbit/s. Adjacent 4-octet slots from the frame start are numbered 0 to 7. The GCI channel takes the number of the slot it occupies. Spare bits in the frame beyond 256 bits from the frame start will be ignored by GCI compatible devices but may be used for other purposes if required (see Fig.4b). GCI channel number is selected by biasing pins S0,S1,S2.

Physical Links.

Four physical links are used in the GCI.

Transmitted data to the line: Bx
Received data from the line: Br
Data clock: BCLK
Frame Synchronization clock: FSa

GCI is always synchronized by frame and data clocks derived by any master clock source. These two clock signals are provided to each component linked by GCI.

A device used in NT mode can deliver clock sources able to synchronize GCI, either directly, or via a local Clock Generator synchronized on the line by means of the MCLK 15.36 MHz output clock.Frame clock and data clock could be independent of the internal devices clocks. Logical one on the Br output is the high impedance state while logical zero is low voltage. For E and A bits, active state is voltage Low while inactive state is high impedance state.

Data is transmitted in both directions at half the data clock rate. The information is clocked by the transmitter on the front edge of the data clock and can be accepted by the receiver after 1 to 1.5 period of the data clock.

The data clock (BCLK) is a square wave signal at twice the data transmission frequency on Bx and Br with a 1 to 1 duty cycle. The frequency can be choosen from 512 to 4096 kHz with 16 kHz modularity. Data transmission rate depends only on the data clock rate.

The Frame Clock is a 8 kHz signal for synchronization of data transmission. The front edge of this signal gives the time reference of the first bit in the first GCI input and output channel, and reset the slot counter at the start of each frame

When some GCI channels are not selected on devices connected to the same GCI link, these time slots are free for alternative uses.

GCI configuration select is done by bias of input pins according to TABLE 1.

Table 1: GCI Configuration selection.

Pin name	TE/NT1	NT12/LT*
MW	0	0
M0	1	0
S2/CLS	CLS = 0: 512 KHz CLS = 1: 1536 KHz	S2
S0/FSb	FSb	S0
S1/AUTOE	AUTOE	S1

* Differentiation between NT and LT mode is done by configuration register 2 (NTS bit)

Monitor channel

The Monitor channel is used to write and read all ST5410 internal registers. Protocol on the Monitor channel allows a bidirectional transfer of bytes between UID and a control unit with acknowledgement at each received byte. Bytes are transmitted on the Br output and received on the Bx input in the Monitor channel slot.
A write or read cycle is always constituted of two bytes.(see fig. 5)

Note: Special format is used for EOC channel.

Write cycle

The format to write a message into the UID is:

A7	A6	A5	A4	A3	A2	A1	A0

1st byte

D7	D6	D5	D4	D3	D2	D1	D0

2nd byte

A7-A1: Register Address
A0: Write/Read Indicator set low
D7-D0: Register Content

After the first byte is shifted in, Register address is decoded. A0 set low indicates a write cycle: the content of the following received byte has to be loaded into the addressed register.

A0 set high indicates a read-back cycle request. the second byte content is not significative. ST5410 will respond to the request by sending back a message with the register content associated with its own address. It is than possible for the micro to receive the required register content after several other pending messages.

Read cycle

When UID has a register content to send to the controller, it send it on the monitor channel directly. Note that the data to send can be the content of a Register previously requested by the controller by means of a read-back request.

The format of the message sent by the UID is:

A7	A6	A5	A4	A3	A2	A1	A0

1st byte

D7	D6	D5	D4	D3	D2	D1	D0

2nd byte

A7-A1: Register Adress
A0: forced to 1
D7-D0: Register Content

Exchange Protocol

ST5410 validates a received byte if it is detected two consecutive times identical. (see fig. 5)

The exchange protocol is identical for both directions. The sender uses the E bit to indicate that it is sending a Monitor byte while the receiver uses A bit to acknowledge the received byte.When no message is transferred, E bit and A bit are forced to inactive state.

A transmission is started by the sender (Transmit section of the Monitor channel protocol handler) by putting the E bit from inactive to active state and by sending the first byte on Monitor channel in the same frame. Transmission of a message is allowed only if A bit sent from the receiver has been set inactive for at least two consecutive frames.

When the receiver is ready, it validates the incoming byte when received identical in two consecutive frames. Then, the receiver set A bit from the inactive to the active state (preacknowledgement) and maintain active at least in the following frame (acknowledgement).

If validation is not possible (two last bytes received are not identical) the receiver aborts the message by setting the A bit active for only a single frame.

The second byte can be transmitted by the sender putting the E bit from the active to the inactive state and sending the second byte on the Monitor chanel in the same frame . The E bit is set inactive for only one frame.

If it remains inactive more than one frame, it is an end of message.

The second byte may be transmitted only after receiving of the pre-acknowledgement of the previous byte . Each byte has to be transmitted at least in two consecutive frames.

The receiver validates the current received byte as for the first one and then set the A bit in the next two frames first from the active state to the inactive state (pre-acknowledgement) and back to the active (acknowledgement). If the receiver cannot validates the received current byte (two bytes received not identical)it pre-acknowledges normally but let the A bit in the inactive state in the next frame which indicates an abort request .

If a message sent by the UID is aborted, the UID will send again the complete message until receiving of an acknowledgement .

A message received by the UID can be acknowledged or aborted with flow Control.

The most significant bit (MSB) of Monitor byte is sent first on the Monitor channel. E & A bits are active low and inactive state on DOUT is 5 V. When no byte is transmitted, Monitor channel slot on Br is in the high impedance state.

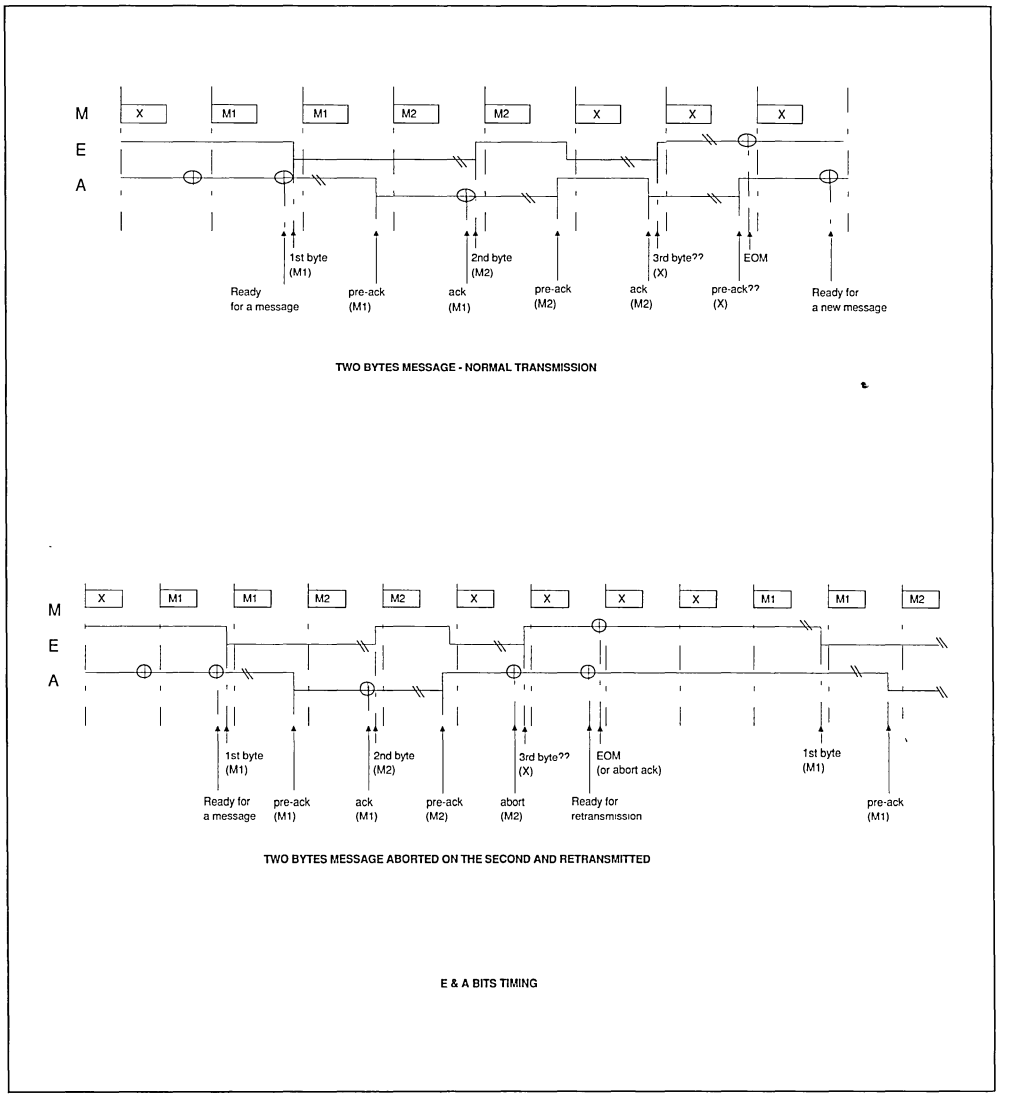
C/I channel

The C/I channel is used to load the Activation Control Register and to read the Activation Indication Register.

A four bits code (C1, C2, C3, C4) is transmitted on the Br output in the C/I channel of the GCI channel. The code is sent permanently at a 8 kHz frequency as long as the content the transmitted register remains unchanged. C1 bit is transmitted first.

A four bits code (C1, C2, C3, C4) is received on the Bx input in the C/I channel of the GCI channel . A change in the receive C/I channel code is validated if it has been received identical in two consecutive frames.

Figure 5: GCI Monitor channel messaging examples.



TURNING ON AND OFF THE DEVICE

ST5410 contains an automatic sequencer for the complete control of the start-up activation sequences specified by the ANSI and French specifications. Interactions with an external control unit requires only Activate Request and Deactivate Request commands, with the option of inserting breakpoints. Automatic control of act and dea bits in the M4 bit positions is provided, along with the specified 40 ms, 480 ms and 15 s timers used during the sequencing.

By default, during ACT procedure, the 15s timer is enabled, to force the device to abandon the sequence where the time limit is reached.

Except the Power up and Power down control that is slightly different, the Activation/Deactivation procedures are identical in GCI and Microwire modes. Same command codes or indication codes are used. In Microwire mode, Activation Control is done by writing in the Activation Control Register ACT. In GCI mode, these registers are accessed directly by the Command/Indicate channels.

Power on initialization

Following the initial application of power, ST5410 enters the power down deactivated state in MICROWIRE mode or in GCI mode depending on the polarization of the MW input.
All the internal circuits including the master oscillator are inactive and in a low power state except for the 10 kHz Tone signal detector. The line outputs LO+/LO- are low impedance and all digital outputs are high impedance. All programmable registers and the activation controller are reset to their default value.

In µW/DSI mode, configuration programming has to be completed before a power up instruction.

In GCI mode, GCI configuration is done by means of pins polarization and register programming.
In NT1 and TE equipments, GCI configuration is defined fully by means of the configuration pins M0, and CLS at Power On Reset.
For LT and NT1-2 equipments, GCI configuration is first defined by means of the configuration pins M0, S2, S1, S0 and must be completed by means of Control Register Programming prior the Power Up instruction.

Power up control

µW/DSI: control instruction PUP in ACT register is required to power up the UID.

GCI: when in TE/NT1 mode (M0=1), the UID provides the GCI clocks needed for control channel transfer; PUP control instruction is provided to the UID by pulling low the Bx data input; ST5410 then reacts sending GCI clocks. It is possible to operate an automatic power up of the UID when a wake up tone is detected from the line by connecting the $\overline{LSD}$ output directly to the Bx input.

GCI: when in LT/NT12 mode (M0=0), the UID powers up after that PUP code (0000) on C/I Control Channel has been sent.

When UID is in the power down state and a 10 kHz tone TN or TL is detected from the line, $\overline{LSD}$ and $\overline{INT}$(µW/DSI only) open drain outputs are forced to zero.

In NT configuration, code LSD (0000) is loaded in the activation indication register RXACT.

In LT configuration, code AP (1000) is loaded in the activation indication register.
In µW/DSI these indications are sent onto CO at the following access even if the UID is still in power down mode.
In GCI, these indications are sent onto the C/I channel as soon as GCI clocks are available.

$\overline{LSD}$ open drain output is set back in the high impedance state as soon as the UID is powered up.

$\overline{INT}$ open drain output is set back in the high impedance state when the $\overline{CS}$ input is detected at zero.

Power up transition enables all analog and digital circuitry, starts the Crystal oscillator and internal clocks. The LSD output is in the high impedance state even if a tone is detected from the line. As for the PDN instruction, PUP has no influence on the content of the internal registers.

Power down control

A control instruction PDN in ACT register is required to power down the device after a period of activity. PDN forces directly the device to the low power state. It should therefore only be used after the UID has been put in the line deactivated state. PDN has no influence on the content of the internal registers, but immediately stops the output clocks when UID is in master mode.

When line is fully deactivated DI code put UID in power down. UID waits for 2 frames (250µs) before entering power down state. During this time on GCI bus the code DI (1111) is sent an C/I. The clocks are stopped as soon as UID is in power down. The DI command is recommended in GCI mode.

Configuration Registers remain in their current state and can be changed either by the µW control interface or the CGI Monitor channel (if M0 = 0 only) depending on mode selected. It is then possible, for instance, after a normal deactivation procedure followed by a power down command, to power up again the device in order to operate directly a Warm Start procedure. In Power Down mode low impedance (with Typical value of 12Ω) between Li+ and Li- is ensured to maintain adaptation to the line impedance.

Software Reset

When the device is either powered-up or down, a control instruction RES resets the activation controller ready for a cold start. That feature can be used if the far-end equipment fails to warm start, for example if the line card or NT has been replaced or if in a regenerator, the loss of synchronisation of the second section imply the reset of the first section for a further cold start. The configuration registers remain in their selected value.

COMMAND/INDICATION (C/I) CODING

The Command/Indication codes are given in Table 2. For each mode a list of recognized Control codes and generated Indicate codes is given. Here after you have a detailed description depending on mode selected.

The C/I codes can be used:

a) in GCI mode, according to the already described rules.

b) in µW/DSI, using the register ACT described in chapter 'Internal register description'

NT mode: Control.

0000 (PUP) Power Up Request.
In GCI configuration with clocks selected as outputs, when UID is in Power down state, Power Up request is done by pulling low the Bx data input; UID reacts sending GCI clocks; code PUP enters no other change. In the other configurations, the PUP instruction powers up the device.

0001 (RES) RESET.
This code resets UID for a cold start. Configuration registers remain in their current value. Can be operated with the device either powered up or down.

0100 (EI) Error Indication.
EI code indicates that a transmission error has been detected on the TE side of the loop relative to UID. act bit is forced to 0 in the SN3 signal transmitted to the line.

0101 (PDN) Power Down Request.
PDN instruction forces the device to Power down state. It should normally only be used in µW/DSI mode after the ST5410 has been put in a known state, e.g. in an NT after a DI status indication has been reported.

1000 (AR) Activation Request.
Being in inactive Power Up state, AR instruction forces UID through the appropriate sequence to activate the line by sending TN and SN1.

1100 (AI) Activation Indication.
The AI code indicates that TE side of the loop relative to UID has been activated. act bit is sent equal 1 in the SN3 signal transmitted to the line.

1111 (DI) Deactivation Indication. (GCI only)
The DI instruction allows the UID to automatically enter the Power down state if the line is deactivated. When the line is not deactivated, DI has no effect.

NT mode : Indication.

0000 (DR/LSD) Deactivation Request.
When in the deactivated state either powered up or down, the LSD code is sent if a 10 kHz wake-up tone is detected. If the device is powered down, the $\overline{LSD}$ pin is also pulled low.
When in activated state, DR code indicates that network has decided to deactivate the line. dea bit has been received equal 0. UID enters the normal deactivate state waiting for a further Warm Start.

0100 (EI) Error Indication.
The EI code indicates that a transmission error has been detected on the loop for more than 480 ms (loss of synchro or loss of signal). UID enters the receive RESET state. EI also indicate that act bit has been received equal 0, or that 15sec timer has expired.

TABLE 2: C/I channel codes.

CODE	TE/NT1/NT12		LT	
C1C2C3C4	Ind	Com	Ind	Com
0000	DR/LSD	PUP	TIM*	PUP/DR
0001	--	RES	--	RES
0100	EI	EI	EI	FAO
0101	--	PDN	--	PDN
0110	--	--	SYNC	--
1000	AP	AR	AP	AR
1100	AI	AI	AI	AI
1111	DI	DI	DI	DI

(*) GCI code only for power up/power down control.

1000 (AP) Activation Pending.
Indicates that the network has decided to activate the loop. SL2/SL3 signal is received with the act bit set to 0.

1100 (AI) Activation Indication.
AI code indicates that network side of the loop relative to UID is activated. SL3 signal is received with the act bit equal 1.

1111 (DI) Deactivation Indication.The DI code indicates that the UID has entered the deactivated state H1.

LT mode: Control.

0000 (PUP/DR) Power Up Request/Deactivation Request.
When in the Power down state, the PUP code powers up the UID. When in the Power Up state, the DR code forces the UID through the appropriate deactivation sequence where the dea bit is set to 0 in four consecutive superframes before ceasing transmission.

0001 (RES) RESET.
This code resets the UID ready for a cold start. Configuration registers remain in their current value. Can be operated with the device either powered up or down.

0100 (FAO) Force act bit to 0.
The act bit is forced to 0 in the SL3 signal transmitted to the line. Is intended to reflect either a transmission error detected on the network side of the loop relative to UID or to acknowledge receiving of an act bit set to 0 from the line.

0101 (PDN) Power Down Request.
PDN instruction forces ST5410 to Power down state. It should normally only be used in µW/DSI mode after the ST5410 has been put in a known state, e.g. in an LT after a DI status indication has been reported.

1000 (AR) Activation Request.
Being in inactive Power Up state, AR instruction forces UID through the appropriate sequence to activate the line.

1100 (AI) Activation Indication.
The AI code is an optional command recognised only when the second break point BP2 is enabled giving the authorization to set the act bit equal one

1111 (DI) Deactivation Indication.
When line is fully deactivated the DI command allows UID to enter power down state. DI is recommended in GCI mode.

LT mode: Indication.

0000 (TIM) Timing required (GCI only)
The TIM code acnowledges PUP command in the case where the UID was previously in the Power Down state.

0100 (EI) Error Indication.
EI code indicates that a transmission error or a act bit equal zero has been received on the loop. In the first case, UID will enter automatically RESET state waiting for a further Cold Start and a DI primitive will be sent. EI also indicate that act bit has been received equal 0, UID being in the activate state.

0110 (SYNC) Synchronization Indication.
SYNC code is sent to indicate that ST5410 is superframe synchronized.

1000 (AP) Activation Pending.
AP code indicates that TE side is attempting to activate the loop. UID waits AR command to send SL1.

1100 (AI) Activation Indication.
The AI code indicates that the UID has received SN3 signal with act bit set to one. That means that the TE side of the loop relative to the UID is activated.

1111 (DI) Deactivation Indication.
The DI code indicates that the UID has entered the Deactivated state .

Activation/deactivation sequencing
Activation/deactivation signals onto the line are in accordance with the activation/deactivation state matrix given in Appendix A.
The startup procedures are in accordance with the T1.601-1988 and ST/LAA/ELR/822 procedures. All the timers defined in the standard are on chip. It is possible in any case to disable the 15sec timer replacing it with an external soft timing.
Refer to T1.601-1988 document for standard procedures description.

Table 3.

INTERNAL REGISTERS																	
COMMAND REGISTERS																	
FUNCTION		**BYTE 1**								**BYTE 2**							
		7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
No Operation (NOP)		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OPR	W	0	0	1	0	0	0	0	0	CIE	EIE	FIE	OB1	OB0	OC1	OC0	0
	R	0	0	1	0	0	0	0	1	X	X	X	X	X	X	X	X
CR1	W	0	0	1	0	0	0	1	0	FF1	FF0	CK2	CK1	CK0	DDM	CMS	BEX
	R	0	0	1	0	0	0	1	1	X	X	X	X	X	X	X	X
CR2	W	0	0	1	0	0	1	0	0	SFS	NTS	DMO	DEN	DD	0	BP2	0
	R	0	0	1	0	0	1	0	1	X	X	X	X	X	X	X	X
CR3	W	0	0	1	0	0	1	1	0	LB1	LB2	LBD	DB1	DB2	DBD	TLB	0
	R	0	0	1	0	0	1	1	1	X	X	X	X	X	X	X	X
TXB1 TSA	W	0	0	1	1	0	0	0	0	0	0	TS5	TS4	TS3	TS2	TS1	TS0
	R	0	0	1	1	0	0	0	1	X	X	X	X	X	X	X	X
TXB2 TSA	W	0	0	1	1	0	0	1	0	0	0	TS5	TS4	TS3	TS2	TS1	TS0
	R	0	0	1	1	0	0	1	1	X	X	X	X	X	X	X	X
RXB1 TSA	W	0	0	1	1	0	1	0	0	EB1	ED	TS5	TS4	TS3	TS2	TS1	TS0
	R	0	0	1	1	0	1	0	1	X	X	X	X	X	X	X	X
RXB2 TSA	W	0	0	1	1	0	1	1	0	EB2	0	TS5	TS4	TS3	TS2	TS1	TS0
	R	0	0	1	1	0	1	1	1	X	X	X	X	X	X	X	X
TXD	W	0	0	1	1	1	0	0	0	DX5	DX4	DX3	DX2	DX1	DX0	SX1	SX0
	R	0	0	1	1	1	0	0	1	X	X	X	X	X	X	X	X
RXD	W	0	0	1	1	1	0	1	0	DR5	DR4	DR3	DR2	DR1	DR0	SR1	SR0
	R	0	0	1	1	1	0	1	1	X	X	X	X	X	X	X	X
TXM4	W	0	1	0	0	0	0	0	0	ACT	M42	M43	M44	M45	M46	M47	M48
TXM56	W	0	1	0	0	0	0	1	0	0	0	LEC	M51	M61	M52	FEB	CTC
ACT Register	W	0	1	0	0	0	1	0	0	0	0	0	0	C4	C3	C2	C1
EC01	W	0	1	0	0	0	1	1	0	07	06	05	04	03	02	01	00
BEC1	R	0	1	0	0	0	1	1	1	X	X	X	X	X	X	X	X
Tx EOC Register	W	0	1	0	1	E	F	G	H	ei1	ei2	ei3	ei4	ei5	ei6	ei7	ei8

Note 1 bit 7 of byte 1 is always the first bit clocked into the device.
Note 2: In the Tx EOC Register:
E = ea1, the msb of the EOC destination address;
F = ea2, bit 2 of the EOC destination address;
G = ea3, the lsb of the EOC destination address,
H = dm, the EOC data/message mode indicator.

Note 3: X= don't care (it is recommended that these bits be set = 0).

Note 4: M42 in TXM4 only significant in LT mode

Table 3: (continued)

STATUS REGISTERS										
FUNCTION	**BYTE 1**	**BYTE 2**								
	7 6 5 4 3 2 1 0	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
READABLE CONFIGURATION REGISTERS										
Default (No Change on a Write cycle)	0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0
OPR Contents	0 0 1 0 0 0 0 0	NBE	ECE	FBE	OB1	OB0	OC1	OC0	0
CR1 Contents	0 0 1 0 0 0 1 0	FF1	FF0	CK2	CK1	CK0	DDM	CLK	BEX
CR2 Contents	0 0 1 0 0 1 0 0	SFS	NTS	DMO	DEN	DD	BP1	BP2	0
CR3 Contents	0 0 1 0 0 1 1 0	LB1	LB2	LBD	DB1	DB2	DBD	TLB	0
TXB1 Contents	0 0 1 1 0 0 0 0	EB1	ED	TS5	TS4	TS3	TS2	TS1	TS0
TXB2 Contents	0 0 1 1 0 0 1 0	EB2	0	TS5	TS4	TS3	TS2	TS1	TS0
RXB1 Contents	0 0 1 1 0 1 0 0	0	0	TS5	TS4	TS3	TS2	TS1	TS0
RXB2 Contents	0 0 1 1 0 1 1 0	0	0	TS5	TS4	TS3	TS2	TS1	TS0
TXD Contents	0 0 1 1 1 0 0 0	DX5	DX4	DX3	DX2	DX1	DX0	SX1	SX0
RXD Contents	0 0 1 1 1 0 1 0	DR5	DR4	DR3	DR2	DR1	DR0	SR1	SR0
REGISTERS WHICH GENERATE SPONTANEOUS INTERRUPTS (NOTE 2)										
RXM4	0 1 0 0 0 0 0 0	M41	M42	M43	M44	M45	M46	M47	M48
RXM56 Spare Bits	0 1 0 0 0 0 1 0	0	ES2	ES1	M51	M61	M52	feb	neb
ACT Indication Reg	0 1 0 0 0 1 0 0	0	0	0	0	C4	C3	C2	C1
BEC1 (Note 3)	0 1 0 0 0 1 1 0	ec7	ec6	ec5	ec4	ec3	ec2	ec1	ec0
Rx EOC Register (Note 4)	0 1 0 1 E F G H	ei1	ei2	ei3	ei4	ei5	ei6	ei7	ei8

Note 1: bit 7 of byte 1 is always the first bit clocked out from the device.

Note 2: All these Registers, with the exception of the EOC Register, set bit 0 of byte 1 as follows: bit 0=0 when the register is read in response to an Interrupt; bit 0=1 when reading back the register in response to a readback command.

Note 3: BEC1 may be polled, via the appropriate read command (see Table 1), at any time to read the current error count. When reading in response to a spontaneous interrupt, the data byte is always X'00.

Note 4: In the Rx EOC Register:
E = ea1, the msb of the EOC destination address;
F = ea2, bit 2 of the EOC destination address;
G = ea3, the lsb of the EOC destination address;

Note 5: ES1, ES2 (RXM56) not significant in µW mode.

INTERNAL REGISTERS DESCRIPTION.

Here following a detailed description of ST5410 internal registers.

Internal registers can be accessed:

a) In GCI mode, according to the monitor channel exchange rules.

b) in µW/DSI mode, using the MICROWIRE interface according to the rules described in section "µW control interface".

By default:
1) When not stated the registers are read-write.
2) Superframe formats (according to AN51 Std) are reported in table 2 and 3.

Overhead bits programmable register (OPR)

After reset: 00H

CIE	EIE	FIE	OB1	OB0	OC1	OC0	0

CIE Near-End CRC Interrupt Enable:

CIE = 1: the RXM56 register is queued in the interrupt register stack with nebe bit set to zero each time the CRC result is not identical to the corresponding CRC received from the line. If in two or more consecutive superframes, an error is detected, two or more interrupt cycles are issued.

CIE = 0: no interrupt is issued but the error detection remains active for instance for on chip error counting.

EIE Error counting Interrupt Enable:

EIE = 1: an interrupt is provided for the counter which goes in overflow (FF).

EIE= 0: no interrupt is issued. It is feasible to read the counters even if no relevant interrupt has been provided.

FIE FEBE Interrupt Enable:

FIE = 1: the RXM56 register is queued into the interrupt register stack each time the febe bit is received at zero in a superframe. If in two or more consecutive superframes, febe bit is received equal zero, two or more interrupt cycles are issued.

FIE = 0: no interrupt is issued but the receive febe bit remains active for on chip error counting

OB1, OB0 Overhead Bit processing:
select how each spare overhead bit received from the line is validated and transmitted to the system. RXM4 and RXM56 registers are independently provided onto the system interface as for the eoc channel. Spare overhead bits are validated independently.

OB1	OB0	
0	0	each super frame, a signal is generated for the RXM4 or the RXM56 register. Spare bits are transparently transmited to the system.
0	1	a signal is set at each new spare overhead Bits received.
1	0	a signal is set at each new spare overhead Bits received and confirmed once. (two times identical).
1	1	a signal is set at each new spare overhead Bits received and confirmed twice. (three times identical).

If new bits are received at the same time in M4 and M56, both registers RXM4 and RXM56 are queued in the interrupt register stack.
Bits act, dea are dedicated to the activation procedure. Validation is always done in accordance with the ANSI rule: validation at each new activation bit received and confirmed twice independently from the above rules. These bits are taken into account directly by the activation decoder. An interrupt is not generated for the RM4 Register when one of these bits changes.

OC1, OC0 eoc channel processing:
select how a received eoc message is validated and transmitted to the system.
The eoc message is signaled:
- in µW/DSI mode: on the control interface by an interrupt
- in GCI mode: on the Monitor channel.

OC1	OC0	
0	0	every half a super frame, a signal is generated for the RXEOC register. eoc channel is transparently transmitted to the system.
0	1	a signal is set at each new eoc message received.
1	0	a signal is set at each new eoc message received and confirmed once. (two times identical)
1	1	a signal is set at each new eoc message received and confirmed twice. (three times identical).

Configuration register 1 (CR1)

FF1	FF0	CK2	CK1	CK0	DDM	CMS	BEX

FF1, FF0 Frame Format Selection:
Refer to fig.1.

FF1	FF0	
0	0	Format 1
0	1	Format 2
1	0	Format 3
1	1	Format 4

CK0-CK2 Digital Interface Clock select:
CK0-CK2 bits select the BCLK output frequency when DSI clocks are outputs.

CK2	CK1	CK0	BCLK frequency:
0	0	0	256KHz
0	0	1	512KHz
0	1	0	1536KHz
0	1	1	2048KHz
1	X	X	2560KHz

DDM Delayed Data Mode select:
Two different phase-relations may be establish between the Frame Sync input and the first bit of the frame on the Digital Interface:

DDM = 0: Non delayed data mode (not available in Format 2) is similar to long frame timing on the COMBOI/II series of devices: The first bit of the frame begins nominally coincident with the rising edge of FSa/b. When output, FSa starts with the first 8 bits wide time-slot while FSb with the second 8 bits wide time-slot.

DDM = 1: delayed data mode (not available in Format 4): which is similar to short frame sync timing on COMBO I/II, in which the FSa/b input must be set high at least a half cycle of BCLK earlier the frame beginning. When output, FSa pulse indicates the first 8 bits wide time-slot while FSb indicates the second.

CMS Clocks Master Select:

CMS = 0: BCLK, FSa and FSb are inputs; BCLK can have in Format 1, 2 and 3 value between 256KHz to 4048KHz, value in Format 4: 512KHz to 6176KHz.

CMS = 1: BCLK, FSa and FSb are outputs; FSa is a 8 kHz clock pulse indicating the frame beginning, FSb is a 8 kHz clock pulse is indicating the second time-slot. BCLK is a bit clock signal whose frequency bits CK2-CK0.

BEX B channels Exchange:

BEX = 0: B1 and B2 Tx/Rx channels are associatedwith B1 and B2 registers respectively.

BEX = 1: B1 and B2 channels are exchanged.

Configuration register 2 (CR2)

SFS	NTS	DMO	DEN	DD	0	BP2	-

SFS Super Frame Synchronization Select:
Significant in LT mode only.

SFS = 0: SFS is an input that synchronizes the transmit frame counter of ths GSC board (timing to be precised).

SFS = 1: SFS is an output issued from the free-running Transmit Frame counter of the GSC board. in NT mode SFS is always an output.

NTS LT / NT mode Select.

NTS = 0: LT mode selected

NTS = 1: NT (NT1, NT2, TE) mode selected

DMO D channel Transfer mode Select.
Significant only when DEN=1.

DMO = 1: D channel data is shifted in and out on Dx and Dr pins in continuous mode at 16 kbit/s on the falling and rising edges of DCLK respectively.

DMO = 0: D channel data is shifted in and out on Dx and Dr pins in a multiplexed mode at the BCLK frequency on the falling and rising edges of BCLK respectively when the assigned time-slots are active.

DEN D channel port Enable.

DEN = 0: D channel port disabled. D bits are transferred on Br and Bx; Multiplexed mode is selected automatically. Test port (TA, TD, TCLK) is selected and may be activated by a Test instruction.

DEN = 1: The D channel port (DX, DR, DCLK) is selected. D bits are transferred on Dr and Dxin a mode depending on DMO bit setting. Test port is disabled.

DD 2B+D Data channel Disable.

DD = 0: 2B+D channel transfer is enabled as soon as the line is completly synchronized.

DD = 1:

2B+D channel transfer is idle; 2B+D bits transmitted to the line are ones or zero depending on configuration respectively selected. 2B+D bits on the Digital Interface are in

the high impedance state. A second level of transparency control is provided for each channel independently from the others when format 3 is selected. See bits EB1, ED and EB2 in TXB1 and TXB2 configuration registers.

BP2 Break Points.
Significant only when NTS=0 (LT selected).

BP2 = 1: a break point in the activation sequencer is enabled after the UID has detected that NT was activatsd avoiding automatic response by act bit = 1.

BP2 = 0: the break point is disabled allowing automatic activation sequencing.

Configuration register 3 (CR3)
After reset: 00H

LB1	LB2	LBD	DB1	DB2	DBD	TLB	-

LB1, LB2, LBD Line side Loopback select.
When set high they turn each individual B1, B2, or D channel from the Line receive input to the Line transmit output. They may be set separately or together. The loopback is operated close to Bx and Br (or Dx and Dr if the D port is selected).

DB1, DB2, DBD Digital side Channel Loopback select.
When set high they turn each individual B1, B2, or D channel from the Digital Interface receive input to the Digital Interface transmit output. They may be set separately or together. The loopback is operated close to Bx and Br (or Dx and Dr if D port selected).

TLB Transparent Loopback select

TLB = 0: loopback are non transparent when line side loopback is set, data transmitted onto the digital interface is forced to one. When digital side loopback is set data transmitted onto the line is forced to one or zero depending on NT or LT configuration respectively.

TLB = 1: 2B+D is transparently transferred through the UID.

Configuration register TXB1

Significant only when format 3 selected.
After reset: 00H

-	-	TS5	TS4	TS3	TS2	TS1	TS0

TS5-TS0 Transmit B1 Time Slot Assignment
Those bits define the binary number of the transmit B1 channel time-slot on Bx input. Time slot are numbered from 0 to 63. The register content is taken into account at each frame beginning.

Configuration register TXB2
Register significant only when format 3 selected.
After reset: 01H

-	-	TS5	TS4	TS3	TS2	TS1	TS0

TS5-TS0 Transmit B2 Time Slot Assignment
Those bits define the binary number of the transmit B2 channel time-slot on Bx input. Time slots are numbered from 0 to 63. The register content is taken into account at each frame beginning.

Configuration register RXB1
Register significant only when format 3 selected.
After reset: 00H

EB1	ED	TS5	TS4	TS3	TS2	TS1	TS0

EB1 B1 channel transparency

EB1= 1: B1 channel transparency enabled.

EB1= 0: B1 channel transmitted forced to one or zero depending on NT or LT configuration and forced the selected B1 channel time slot on Br output in the high impedance state.

ED D channel transparency enabling

ED = 1: enables the D channel transparency.

ED = 0: forces the D channel transmitted onto the line to one or zero depending on NT or LT configuration respectively and forces the selected D channel time slot on Br or Dr output in the high impedance state

TS5-TS0 Receive B1 Time Slot Assignment
TS5-TS0 bits define the binary number of the receive B1 channel time-slot on BR output. Time slot are numbered from 0 to 63. The register content is taken into account at each frame beginning.

Configuration register RXB2
Register significant only when format 3 selected.
After reset: 01H

EB2	-	TS5	TS4	TS3	TS2	TS1	TS0

EB2 B2 channel transparency
EB2 = 1: enables the B2 channel transparency.
EB2 = 0: forces the B2 channel transmitted onto the line to one or zero depending on NT or LT configuration respectively and forces the selected B2 channel time slot on Br output in the high impedance state.

TS5-TS0 Receive B2 Time Slot Assignment
Those bits define the binary number of the receive B2 channel time-slot on BR output. Time slot are numbered from 0 to 63. The register content is taken into account at each frame beginning.

Configuration register TXD
Significant only when format 3 is selected with the D channel Digital interface selected in the multiplexed mode:
After reset: 0CH in GCI
08H in µW/DSI

DX5	DX4	DX3	DX2	DX1	DX0	SX1	SX0

DX5-SX0 Transmit D channel Time Slot Assignment
DX5-DX0 and SX1-SX0 bits define the binary number of the transmit D channel time-slot. DX5-DX0 bits define the binary number of the 8 bits wide timeslot. Time slot are numbered from 0 to 63. Within this selected time slot, SX1,SX0 bits define the binary numbar of the 2 bits wide time-slot. Sub time-slots are numbered 0 to 3. The register content is taken into account at each frame beginning.

Configuration register RXD
Significant only when format 3 is selected with the D channel Digital interface selected in multiplexed mode.
After reset: 0CH in GCI
08H in µW/DSI

DR5	DR4	DR3	DR3	DR2	DR1	SR1	SR0

DR5-SR0 Receive D channel Time Slot Assignment
DR5-DR0 and SR1-SR0 bits define the binary number of the receive D channel time-slot. DR5-DR0 bits define the binary number of the 8 bits wide timeslot. Time slot are numbered from 0 to 63. Within this selected time slot., SR1,SR0 bits define the binary number of the 2 bits wide time-slot. Sub time-slots are numbered 0 to 3. The register content is taken into account at each frame beginning.

Transmit M4 channel register (TXM4)
(write only)
After reset: 7FH

-	m42	m43	m44	m45	m46	m47	m48

The TXM4 Register is constituted of 7 bits: m42, m43, m44, m45, m46, m47, m48. When the line is fully activated (super framing synchronized), the UID shall continuously send in the M4 channel field the register content to the line once per superframe. Register content is loaded in the transmit register at each superframe.
m41 is the act bit. m42 in LT mode in the LT to NT direction is the dea bit. These activation bits are controlled directly by the on chip activation encoder-decoder. The corresponding bits in the TXM4 register are not significant.

Transmit M5 and M6 channels register (TXM56)
(write only)
After reset: 3EH

-	-	LEC	m51	m61	m52	feb	CTC

LEC External Control pin
The logical level of the output EC is directly controlled by the bit LEC (GCI mode only).

m51, m61, m52 M5 and M6 spare over-head bits
Those spare overhead bits are normally equal to 1. Default value can be changed by setting the respective bits.

feb Transmit febe bit control
The febe bit which is normally at logical 1 and automatically set low in the following superframe when a CRC checking error has been detected in the previous received superframe may be forced to 0 by writing 0 in bit position feb. The febe bit set to zero is sent once to the line in the following available superframe.

CTC Corrupted Transmit CRC Control
CTC = 0: allows the normal calculation of the CRC for the transmitted data to the Line
CTC = 1: CRC result is transmitted inverted starting from next superframe. That ensure transmission of a corrupted CRC.

Activation control register (ACT)
(write only, µW only)
After reset XFH

-	-	-	-	C4	C3	C2	C1

This register is constituted of four bits: (C1, C2, C3, C4). In GCI mode, this register is directly adressed by means of the C/I channel. Activation Control instructions are coded on 4 bits.

Transmit EOC register (TXEOC)
(write only)
After reset: FFFH

ea1	ea2	ea3	dm	ei1	ei2	ei3	ei4	ei5	ei6	ei7	ei8

TXEOC Register is constituted of 12 bits. When the line is fully activated (super framing synchronized), ST5410 shall continuously send into the EOC channel field the eoc bits twice per superframe. TXEOC register is loaded in the transmit register at each half a superframe.
The address of this register is composed only of 4 bits. The W/R indicator is not needed.

Receive spare M4 overhead bits register (RXM4)
(read only)
After reset: 7FH

-	m42	m43	m44	m45	m46	m47	m48

RXM4 Register is constituted of 8 bits. When the line is fully activated (super frame synchronized), ST5410 extracts the M4 channel bits. m41 is the act bit; m42 in NT mode is the dea bit these bits are under the control of the activation sequencer. No interrupt cycle is provided for the RXM4 register when a change on one of the activation bits is detected.
When one of the remaining received spare bits is validated following the criteria selected in the Configuration Register OPR, the RXM4 register content is queued in the interrupt register stack. Activation bits status are also delivered.

Receive m5, m6 overhead bits register (RXM56)
(read only)
After reset: FFH

-	ES2	ES1	m51	m61	m52	feb	neb

When the line is fully activated (super frame synchronized), ST5410 extracts the overhead bits.
When one of the received spare bits m51, m61, m52 is validated following the criterias selected in the Configuration Register OPR, the RXM56 register content is queued in the interrupt register stack.If the FIE bit in OPR register is set high, the RXM56 register content is queued in the interrupt register stack each time the febe bit is received equal zero with bit feb equal 0.
The CRC received from the far-end is compared at the end of the superframe with the CRC calculated by the UID during that superframe. If an error is detected, the febe bit in the transmit direction is forced equal zero in the next superframe. If the CIE bit in the OPR register is set high, the RXM56 register is queued in the interrupt register stack at each CRC error detected with bit neb equal zero. ES1,ES2 bits indicates the status of the inputs pins ES1,ES2 respectively. At each status change, the RXM56 register is queued in the interrupt register stack.

Activation indication register (RXACT)
(read only)
Afterr reset: XHF

-	-	-	-	C4	C3	C2	C1

This Register is constituted of four bits: (C1, C2, C3, C4). In GCI mode, this register is directly connected to the C/I channel. At each activation status change, an interrupt request is queued in the interrupt register stack. In GCI mode, the C1-C4 bits are directly sent on the C/I channel. Activation Indication instructions are coded on 4 bits according to activation description.

Block Error counter 1 (EC1)
(read only)
After reset: 00H

ec7	ec6	ec5	ec4	ec3	ec2	ec1	ec0

This Register indicates the binary value of the Error up-counter 1. The register accounts for the febe and mebe errors. When counter goes in overflow (FF), an interrupt is provided for the EC1 register with value FF.

Offset Block error control counter 1 register (EC1) read only
(write only)
After reset: 00H

o7	o6	o5	o4	o3	o2	o1	o0

Block Error Counter 1 can be preset at a value given by Offset register EC1 Error. The counter is preset at that value each time the counter is read or when the preset value is loaded. o7-o0 is the binary value of the error up-counter 1 offset.

Receive EOC register (RXEOC)
(read only)

ea1	ea2	ea3	dm	ei1	ei2	ei3	ei4	ei5	ei6	ei7	ei8

The RX EOC Register is constituted of 12 bits. When the line is fully activated (super frame synchronized) and when a eoc message is received and validated in accordance with the criteria selected in the Configuration Register OPR, the RX EOC Register is queued in the interrupt register stack. The address of this register is composed only of 4 bits. The W/R indicator is not needed.
After each activation process, this register generates an interrupt giving the first received EOC channel content, even if it is a FFFH.

Table 4: Network-to-NT 2B1Q Superframe Technique and Overhead Bit Assignments.

		FRAMING	2B+D	Overhead Bits (M_1-M_6)					
	Quat Positions	1-9	10-117	118s	118m	119s	119m	120s	120m
	Bit Positions	1-18	19-234	235	236	237	238	239	240
Super Frame #	Basic Frame #	Sync Word	2B+D	M_1	M_2	M_3	M_4	M_5	M_6
A	1	ISW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	act	1	1
	2	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	dea	1	febe
	3	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	1	crc_1	crc_2
	4	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	1	crc_3	crc_4
	5	SW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	1	crc_5	crc_6
	6	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	1	crc_7	crc_8
	7	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	uoa	crc_9	crc_{10}
	8	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	1	crc_{11}	crc_{12}
B,C,...									

NT-to-Network superframe delay offset from Network-to-NT superframe by 60 ± 2 quats (about 0.75 ms).
All bits than the Sync Word are scrambled.

Symbols & Abbreviations:

"1" = reserve = reserved bit for future standard; set = 1
eoc = embedded operations channel
a = address bit
dm = data/message indicator
i = information (data/message)
SW = synchronization word
ISW = inverted synchronization word
s = sign bit (first) in quat
m = magnitude bit (second) in quat
act = activation bit (set = 1 during activation)
crc = cyclic redundancy check· covers 2B+D & M4
1 = most significant bit
2 = next most significant bit
etc.
febe = far end block error bit (set = 0 for errored superframe)
dea = deactivation bit (set = 0 to announce deactivation)
uoa = (not used in this version)

Note: 8 x 1.5 msec Basic Frames 12 msec Superframe

Table 5: NT-to-Network 2B1Q Superframe Technique and Overhead Bit Assignments.

		FRAMING	2B+D	Overhead Bits (M_1-M_6)					
	Quat Positions	1-9	10-117	118s	118m	119s	119m	120s	120m
	Bit Positions	1-18	19-234	235	236	237	238	239	240
Super Frame #	Basic Frame #	Sync Word	2B+D	M_1	M_2	M_3	M_4	M_5	M_6
1	1	ISW .	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	act	1	1
	2	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	ps_1	1	febe
	3	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	ps_2	crc_1	crc_2
	4	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	ntm	crc_3	crc_4
	5	SW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	cso	crc_5	crc_6
	6	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	1	crc_7	crc_8
	7	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	sai	crc_9	crc_{10}
	8	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	1	crc_{11}	crc_{12}
2,3,...									

NT-to-Network superframe delay offset from Network-to-NT superframe by 602 quats (about 0.75 ms). All bits than the Sync Word are scrambled.

Symbols & Abbreviations:

"1" = reserve = reserved bit for future standard, set = 1
eoc = embedded operations channel
a = address bit
dm = data/message indicator
i = information (data/message)
SW = synchronization word
ISW = inverted synchronization word
s = sign bit (first) in quat
m = magnitude bit (second) in quat

act = activation bit (set = 1 during activation)
ps_1, ps_2 = power status bits (set = 0 to indicate power problems)
ntm = NT in Test Mode bit (set = 0 to indicate test mode)
cso = cold-start-only bit (set = 1 to indicate cold-start-only)
crc = cyclic redundancy check: covers 2B+D & M4
1 = most significant bit
2 = next most significant bit
etc.
febe = far end block error bit (set = 0 for errored superframe)
sai = S/T interface activation bit. Used in restricted activation only (not used in this version)

Note: 8 x 1.5 msec Basic Frames 12 msec Superframe

LINE CODING AND FRAME FORMAT

2B1Q coding rule requires that binary data bits are grouped in pairs so called quats (see Tab.6). Each quat is transmitted as a symbol, the magnitude of which may be 1 out 4 equally spaced voltage levels (see Fig. 6). No redundancy is included and in the limit there is no bound to the Running Digital Sum (RDS), although scrambling controls the RDS in the pratical sense +3 quat referers to the nominal pulse wavwform specified in the ANSI standard. Other quats are deduced directly with respect of the ratio and keeping of the waveform.

The frame format used in UID follows ANSI and French specifications (see Tab. 4 and 5). Each complete frame cosists of 120 quats, with a line baud rate of 80 kbaud/s, giving a frame duration of 1.5ms. A9 quats sync-word defines the framing boundary. Furthermore, a Multiframe consisting of 8 frames is defined in order to provide sub-channels within the spare bits M1 to M6. Inversion of the syncword defines the multiframe boundary. Prior to transmisssion, all data, with the exception of the sync-word,is scrambled using a self-synchronizing scrambler to perform the specified 23rd-order polynomial. Descrambling is included in the receiver. Polynomial is different depending on the direction TE to NT or NT to TE.

Maintenance functions

M channel
In each frame there are 6 "overhead" bits assigned to various control and maintenance functions. Some programmable processing of these bits is provided on chip while interaction with an external controller provides the flexibility to take full advantage of the maintenance channels. See OPR, TXM4, TXM56, TXEOC, RXM4, RXM56, RXEOC register description fo details. New data written to any of the Overhead bit Transmit Registers is resynchronized internally to the next available complete superframe or half superframe, as appropriate.

Embedded Operatione Channel (EOC)
The EOC channel consists of two complete 12 bits messages per superframe, distributed through the M1, M2 and M3 bits of each frame. Each message is composed of 3 fields; a 3 bit address identifying the message destination/origin, a 1 bit indicator for the data mode i.e. encoded message or raw data, and an 8 bits information field. The Control Interface (Microwire or Monitor channel in GCI) provides access to the complete 12 bits of every message in TX and RX EOC registers.

UID does not recognize the received and encoded messages e. g. send corrupted CRC, then the apprpriate command register instruction must be written to the device to invoke the relevant function.

It is possible to select a transparent transmission mode in which the EOC channel can be considered as a transparent 2 kbit/s channel. See OPR register description for details.

M4 channel
M4 bit positions of every frame is a channel in which are trasmitted data bits loaded from the TXM4 transmit register and from the on-chip activation sequencer once the superframe. On the receive side, M4 bits from one complete superframe are first valitated and then stored in the RXM4 Receive Register or transmitted to on-chip activation sequencer. See OPR, TXM4 and RXM4 registers description for details.

Spare M5 and M6 bits
The spare bit positions in the M5 and M6 field form a channel in which are transmitted data bits loaded from the TXM56 transmit register. On the receive side, the spare bits in the M5 and M6 field are first validated and then stored in the RXM56 receive register. See OPR, TXM56 and RXM56 registers description for details.

CRC calculation/checking
In transmit direction, an on-chip CRC calculation circuit automatically generates a checksum of the 2B+D+M4 bits using the specified 12th order polynomial. Once per superframe, the CRC is transmitted in the M5 and M6 bit positions. In receive direction, a checksum is again calculated on the same bits as they are received and, at the end of the superframe compared with the received CRC. The result of this comparison generates a "Far End Block Error" bit (febe) which is transmitted back towards the other end of the Line in the next bute-one superframe and an indication of Near End Block Error is sent to the system by means of Register RXM56. If there is no error in superframe, febe is set = 1, and if there is one or more errors, febe is set = 0.

UID also includes an 8 bits Block Error Counter associated with the febe bits transmitted and received. Block error counting is always enabled but it is possible to disabled the overflow interrupt and/or to enabled/disabled the interrupt issued at each received or transmitted block error detection. See OPR register for details.

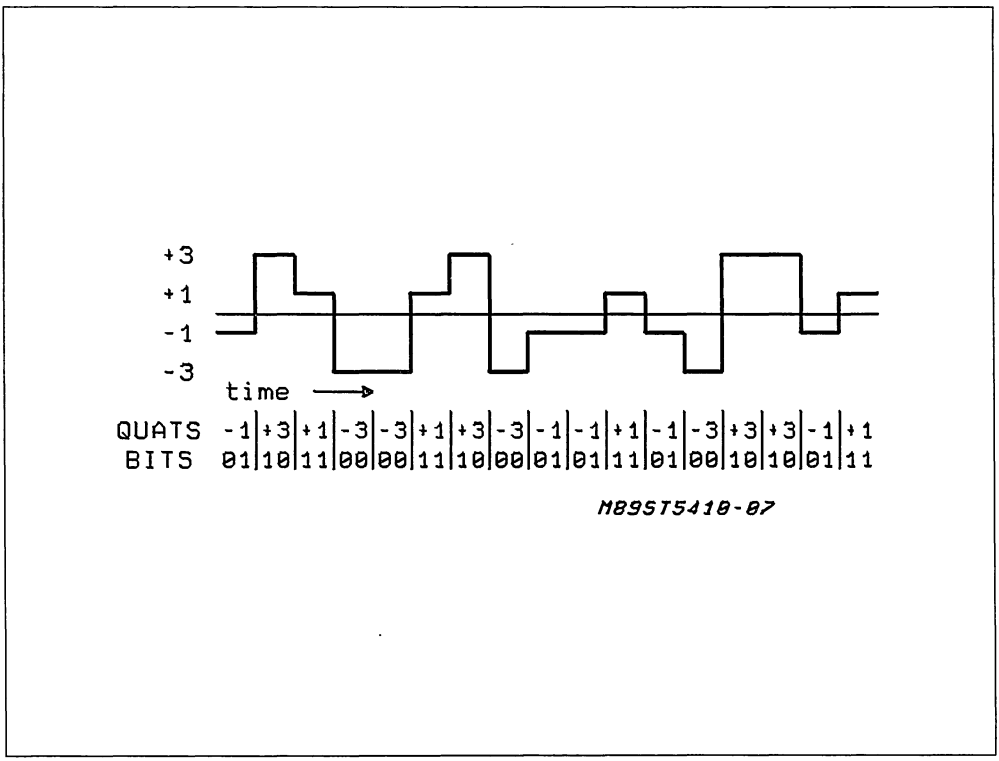
Table 6: 2B1Q Encoding of 2B+ D Fields.

Data	Time → B_I				B_g				D
Bit Pairt	$b_{11}b_{12}$	$b_{13}b_{14}$	$b_{15}b_{16}$	$b_{17}b_{18}$	$b_{21}b_{22}$	$b_{23}b_{24}$	$b_{25}b_{26}$	$b_{27}b_{28}$	d_1d_2
Quat # (relative)	q_1	q_2	q_3	q_4	q5	q_6	q_7	q_8	q_9
# Bits	8				8				2
# Quats	4				4				1

Where: b_{11} = first bit of B_1 octet as received at the S/T interface
b_{18} = last bit of B_I octet as received at the S/T interface
b_{21} = first bit of B_2 octet as received at the S/T interface
b_{28} = last bit of B_2 octet as received at the S/T interface
d_1 d_2 = consecutive D-channel bits (d_1 is first bit of pair as received at the S/T interface)
q_i = ith quat relative to start of given 18-bit 2B+D data field.

NOTE: There are 12 2B+D 18-bit fields per 1.5 msec basic frame.

Figure 6: Example of 2B1Q Quaternary Symbols.



LINE SECTION

Data transmitted to the line consists of the 2B+D channel data received from the Digital Interface through an elastic data buffer allowing any phase deviation with the line, the activation/deactivation bits (M4) from the on-chip activation sequencer, the CRC code plus maintenance data (eoc channels) and other spare bits in the overhead channels (M4, M5, M6). Data are multiplexed and scrambled prior to addition of the sync-word, whiich generated within the device. A pulse waveform synthesizer then drives the transmit filter, which in turn passes the line signal to the line driver. The differential line-driver Outputs, LO+, LO- are designed to drive a transformer through an external termination circuit. A 1:1.5 transformer designed as shown in the Application section, results in a signal amplitude of normally 2.5V pk on the line for single quats of the +3 level. However, because of the RDS accumulation of the 2B1Q line code, continuous random data will produce signal swings considerably greater than this on the line. Short-circuit protection is included in the output stage; over-voltage protection must be provided externally.

In LT applications, the Network reference clock given by the FSa 8kHz clock input synchronizes the transmitted data to the line. The Digital Interface normally accepts BCLK and Fsa signals from the network, requiring the selection of Slave Mode in CRI. Retiming circuitry on chip allow the 15.36MHz crystal oscillator (or the logic level clock input on XTAL1) to be plesiochronous with respect to the network clock provided the sum of frequency inaccuracies, expressed in ppm deviation from nominal, of the network clock plus the XTAL1 one does not exceed 150ppm.

In NT applications, data is transmitted to the line with a phase deviation of half a frame relative to the received data as specified in the ANSI standard.

The receive input signal should be derived from the transformer by a coupling circuit aa shown in the Application section. At the front end of the receive section is a continuous filter which limits the noise bandwidth to approximately 200kHz. Then, a precanceller provides a degree of analog echo cancellation in order to limit the dynamic range of the composite signal which noise bandwidth limited by a 4th order butterworth switched capacitor low pass filter. After an automatic gain control, a 13bits A/D converter then samples the composite received signal before the echo cancellation from local transmitter by means of an adaptive digital transversal filter. The attenuation and distortion of the received signal from the far-end, caused by the line, is equalized by a second adaptive digital filter configured as a Decision Feedback Equlizer (DFE), that restores a flat channel response with maximum received eye opening over a wide spread of cable attenuation characteristics.

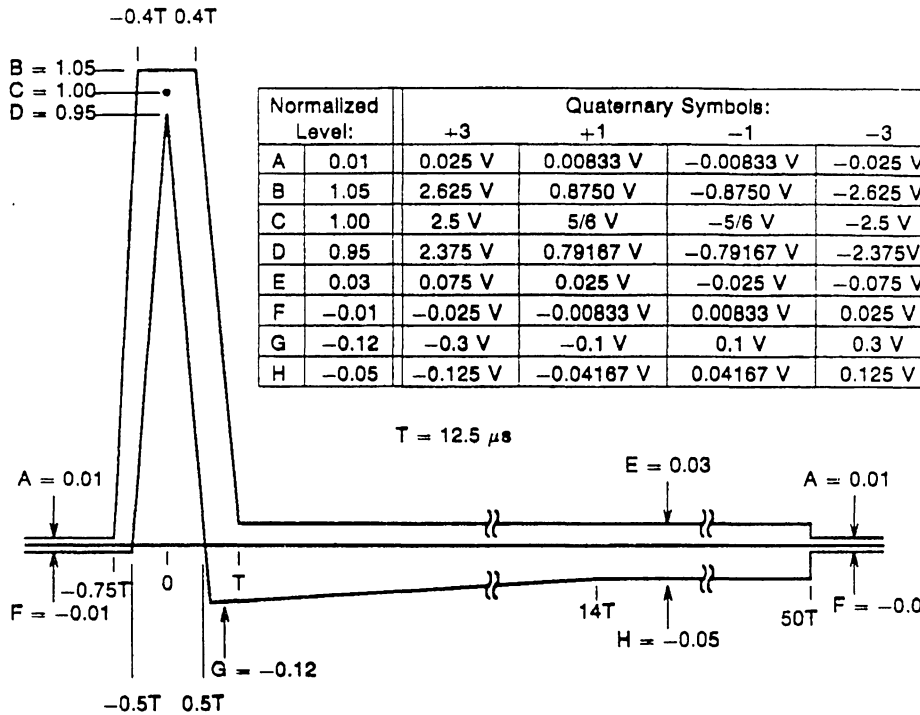
A timing recovery circuit based on a DPLL (Digital Phase-Locked Loop) recovers a very low-jitter clock for optimum sampling of the received symbols. The 15.36MHz crystal oscillator (or the logic level clock input) provides the reference clock for DPLL. In NT configuration, MCLK output provides a very low jitterized 15.36MHz clock to the system.

Received data is then detected and flywheel synchronization circuit searches for and locks onto the frame and superframe syncwords. ST5410 is frame-synchronized when two consecutive synchwords have been consecutively detected. Frame lock will be maintained until six consecutive errored sync-words are detected, which will cause the flywheel to attempt to re-synchronize. If a loss of frame sync condition persists for 480ms the device will cease searching, cease transmitting and go automatically into the RESET state, ready for a further cold start. When UID is frame-synchronized, it is superframe-locked upon the first superframe-locked upon the first superframe sync-word detection. No loss of superframe sync-word is provided.

While the receiver is synchronized, data is descrambled using the specified polynomial, and individual channels demultiplexed and passed to their respective processing circuits: user's 2B+D channel data is transmitted to the Digital Interface through an elastic data buffer allowing any phase deviation with the Line; the activation/deactivation bits (M4) are transmitted to the on-chip cativation sequencer; CRC is transmitted to CRC checking section while maintenance data (eoc) and other spare bits in the overhead channels (M4, M5, N6) are stored in their respective Rx registers.

In NT applications, if the Digital Interface is selected in master mode (see CR1) BCLK and FSa clock outputs are phase-locked to the recovered clock. If it is selected in Slave mode ie for NT1-2 application, the on-chip elastic buffers allow BCLX and FSa to be input from an external source, which must be frequency locked to the received line signal ie using the XTA1 output but with arbitrary phase.

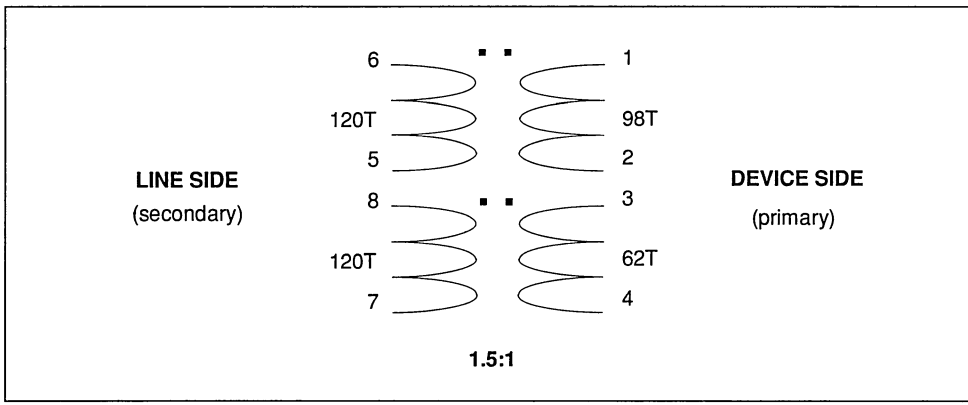
Figure 7: Normalized Output Pulse From NT1 or LT..



Normalized Level:		Quaternary Symbols: +3	+1	−1	−3
A	0.01	0.025 V	0.00833 V	−0.00833 V	−0.025 V
B	1.05	2.625 V	0.8750 V	−0.8750 V	−2.625 V
C	1.00	2.5 V	5/6 V	−5/6 V	−2.5 V
D	0.95	2.375 V	0.79167 V	−0.79167 V	−2.375V
E	0.03	0.075 V	0.025 V	−0.025 V	−0.075 V
F	−0.01	−0.025 V	−0.00833 V	0.00833 V	0.025 V
G	−0.12	−0.3 V	−0.1 V	0.1 V	0.3 V
H	−0.05	−0.125 V	−0.04167 V	0.04167 V	0.125 V

Line Interface Circuit
It is very important, for compliance with the ANSI and French standard, that the recommended line interface circuit should be strictly adhered to. The channel response and dynamic range of this circuit have been carefully designed as an integral part of the overall signal processing system to ensure the performance requirements are met under all the specified loop conditions. Deviations from this design are likely to result in sub-optimal performance or even total failure of the system on some types of loops.

Figure 8: Transformer Design.



Turns Ratio: Np:Ns = 1:1.5.
Secondary Inductance: Lp 27mH.
Winding Resistances: 30 ohms > (2.25Rp + Rs) > 10 ohms.
Return Loss at: 40 kHz against 135 ohms 26 dB.
Saturation characteristics: THD –70dB when tested with 50mA d.c. through the secondary and a 40kHz sine-wave injected into the primary at a level which generates 5V p-p into 135 ohms at the secondary.

List of suppliers:

SHOTT
PULSE ENGINEERING
AIE

Table 7.

WINDING	NUMBER OF TURNS	WIRE GAUCE
1-2	98 Single	#34 AWG
6-5, 8-7	120+120 Bifilar	#36 AWG
3-4	62 Single	#34 AWG
WINDING	**INDUCTANCE**	**RESISTANCE**
1-2 + 3-4	12 mH	less than 5 ohms
5-6 + 7-8	27 mH	less than 10 ohms

Note: the split primary winding is designed to minimize leakage inductance.

Board Layout

While the pins of the UID are well protected against electrical misuse, it is recommended that the standard CMOS practise of applayng GND to the device before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used. Great care must be taken in the layout of the printed circuit board in order to preserve the high transmission performance of the ST5410. To maximize performance, do not use the philosophy of separating analog and digital grounds for chip. The 3 GND pins should be connected together as close as possible to the pins, and the 2 VCC pins should be strapped together. All ground connections to each device should meet at a common point as close as possible to the 3 GND pins order to prevent the interaction of ground return currents flowing through a common bus impedance. A decoupling capacitor of 1.5µF should be connected from this common point to VCC pins as close as possible to the chip. Taking care with the board layout in the following ways will also help prevent noise injection into the receiver frontend and maximize the transmission performances. Keep the crystal oscillator components away from the receiver inputs and use a shielded ground plane around these components. Keep the device, the components connected to LI+/LI- and the transformer as close as possible. Simmetrical layout for the line interface is suggested.

Figure 9: Recommended Connections.

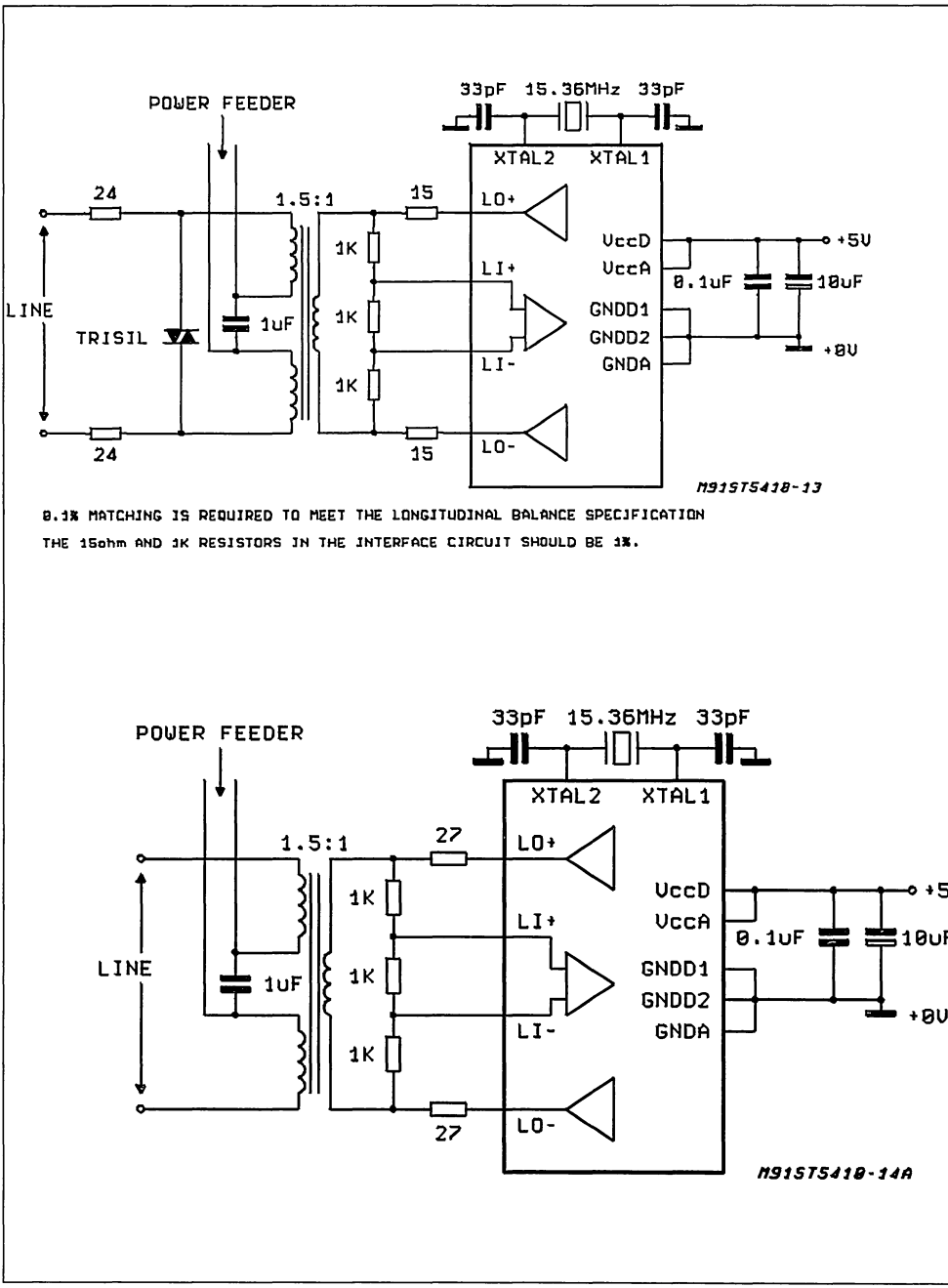
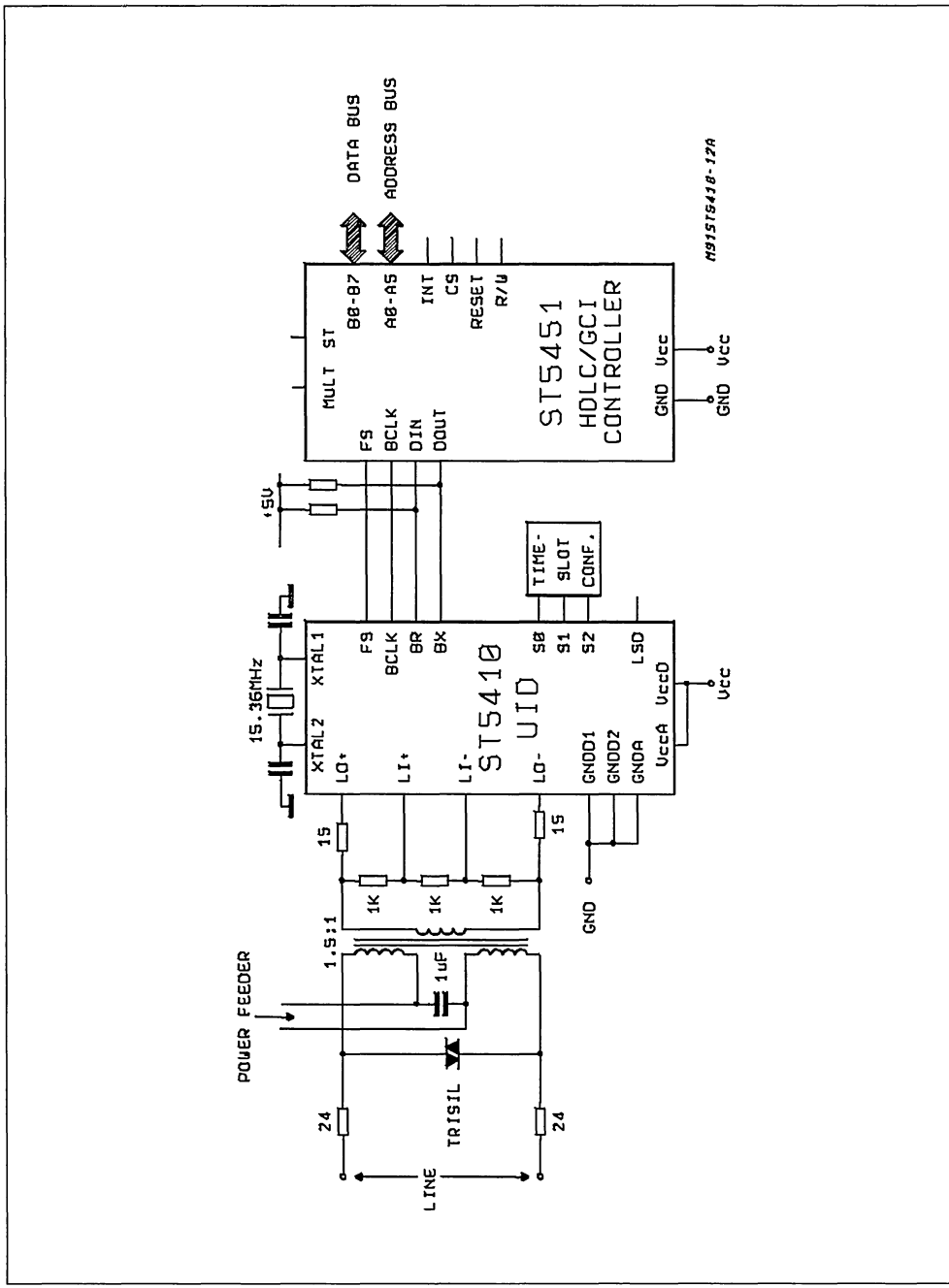


Figure 10: LT Application



APPENDIX A
State Matrix

EVENT	STATE NAME	Power Off	Full Reset	Alertg	Awake	EC Training	WAIT SN2	CHECK SN2	EC Covrg'd	SW Sync	ISW Sync	Active	Deact'n Alert'n	Tear Down	Pending Deact'n	Recv Reset
	STATE CODE	J0	J1	J2	J3	J4	J4. 1	J4 2	J5	J6	J7	J8	J9	J10	J11	J12
	TX	SL0	SL0	TL	SL0	SL1	SL2 dea = 1 act = 0	SL2 dea = 1 act = 0	SL2 dea = 1 act = 0	SL2 dea = 1 act = 0	SL3 dea = 1 no change (*)	SL3 dea = 1 act = 1	SL3 dea = 0 act = 0	SL0	SL0	SL0
POWERON		J1	-	-	-	-	-	-	-	-	-	-	-	-	-	-
LOSS OF POWER		-	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0
ACTIVATION REQUEST (AR)		/	ST T5 J2	-	-	-	-	-	-	-	-	-	-	-	-	-
DEACTIVATION REQUEST (DR)		/	-	-	-	-	-	-	-	-	J9	J9	-	-	-	-
END OF TONE TL (3 ms)		/	/	J3	-	/	/	/	/	/	/	/	/	/	/	/
RECEIVED TONE TN and ACTIVATION REQUEST (AR)		/	ST T5 J3 AP	-	-	/	/	/	/	/	/	/	/	/	/	ST T5 STP T7 J3 AP
LOSS OF SIGNAL ENERGY		/	-	-	J4	-	-	J4.1	/	/	/	/	/	/	/	/
ECHO CANCELLER CONVERGED		/	-	-	-	J4.1	-	-	-	-	-	-	-	-	-	-
B-ASIC FRAME SYNC (SW)		/	/	/	/	/	/	/	J6	-	-	-	-	-	-	-
SUPERFRAME SYNC (ISW)		/	/	/	/	/	/	/	/	STP T5 J7 SYNC	-	-	-	-	-	-
RECEIVED act = 0		/	/	/	/	/	/	/	/	/	-	J7 EI	-	-	-	-
RECEIVED act = 1		/	/	/	/	/		/	/	/	J8 AI	-	-	-	-	-
LOSS OF SYNC (> 480 ms)		/	/	/	/	/	/	/	/	/	J10 EI	J10 EI	-	-	-	-
LOSS OF SIGNAL (> 480 ms)		/	/	/	/	/	/	/	/	ST T7 J12 EI	ST T7 J12 EI	ST T7 J12 EI	-	/	/	/
END OF THE LAST SUPERFRAME WITH dea = 0 (4th)		/	/	/	/	/	/	/	/	/	/	/	J11	/	/	/
EXPIRY OF TIMER (**) T5 (15 seconds)		/	-	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	/	-	/	-	/	/
LOSS OF SIGNAL (< 40 ms)		/	-	/	/	/	/	/	/	/	/	/	/	ST T7 J12	J1 D1	-
EXPIRY OF TIMER (**) T7 (40 ms)		/	/	/	/	/	/	/	/	/	/	/	/	/	/	J1 D1
DETECTION OF SIGNAL ENERGY		/	-	-	-	-	J4 2	J5	-	-	-	-	-	-	-	-
RESET COMAND (RES)		/	-	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	-	-	-	-	-	-

(*) FAO command is needed to send act = 0
(**) When timer is enabled (default)

ACTIVATION/DEACTIVATION FINITE STATE MATRIX IN LT MODE

EVENT	STATE NAME	Power Off	Full Reset	Alertg	EC Training	WAIT SL	CHECK SL	EC Covrg'd	SW Sync	ISW Sync	Pending Active	Active	Pending Deact'n	Tear Down	TE Inactive	Recv Reset
	STATE CODE	H0	H1	H2	H3	H3 1	H3 2	H4	H5	H6	H7	H8	H9	H10	H11	H12
	TX	SN0 INFO0	SN0 INFO0	TN INFO0	SN1 INFO0	SN0 INFO0	SN0 INFO0	SN0 INFO0	SN2 INFO0	SL3 act = 0 INFO2	SN3 act = 1 INFO2	SN3 act = 1 INFO4	SN3 no change	SN0 INFO0	SN3 act = 0 INFO2	SN0 INFO0
POWERON		H1	-	-	-	-	-	-	-	-	-	-	-	-	-	-
LOSS OF POWER		-	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0
RECEIVED S/T INFO 1 SIGNAL (Received AR)		/	ST T4 H2	-	-	-	-	-	-	-	-	/	/	-	/	-
RECEIVED S/T INFO 3 SIGNAL (Received AI)		/	/	/	/	/	/	/	/	H7	-	-	-	-	H7	/
RECEIVED S/T INFO 0 SIGNAL (Received EI)		/	-	-	-	-	-	-	-	-	H11	H11	-	-	-	-
END OF TONE TN (9 ms)		/	/	H3	-	-	-	/	/	/	/	/	/	/	-	/
RECEIVED TONE TL and ACTIVATION REQUEST (AR)		/	ST T4 H2 LSD	-	/	/	/	/	/	/	/	/	/	/	-	ST T4 STP T6 H2 LSD
ECHO CANCELLER CONVERGED		/	-	-	H3 1	-	-	-	-	-	-	-	-	-	-	-
BASIC FRAME SYNC (SW)		/	/	/	/	/	/	H5	-	-	-	-	-	-	-	-
SUPERFRAME SYNC (ISW)		/	/	/	/	/	/	/	STP T4 H6 AP	-	-	-	-	-	-	-
RECEIVED dea = 0		/	/	/	/	/	/	/	/	H9 DP	H9 DP	H9 DP	-	-	H9 DP	-
RECEIVED act = 0 and dea = 1		/	/	/	/	/	/	/	/	/	-	H7 EI	-	-	-	-
RECEIVED act = 1 and dea = 1		/	/	/	/	/	/	/	/	/	H8 AI	-	-	-	-	-
LOSS OF SYNC (> 480 ms)		/	/	/	/	/	/	/	/	H10 EI	H10 EI	H10 EI	-	-	H10 EI	-
LOSS OF SIGNAL (> 480 ms)		/	/	/	/	ST T6 H12 EI	/	ST T6 H12 EI	ST T6 H12 EI	ST T6 H12 EI	ST T6 H12 EI	ST T6 H12 EI	/	/	ST T6 H12 EI	-
EXPIRY OF TIMER (*) T4 (15 seconds)		/	-	H10 EI	H10 EI	H10 EI	H10 EI	H10 EI	H10 EI	/	/	/	/	-	/	-
LOSS OF SIGNAL (< 40 ms)		/	-	/	/	/	H3 1	/	/	/	/	/	ST T6 H12	ST T7 J12	/	/
EXPIRY OF TIMER T6 (40 ms)		/	/	/	/	/	/	/	/	/	/	/	/	/	/	H1 DI
DETECTION OF SIGNAL ENERGY		/	-	-	-	H3 2	H4	-	-	-	-	-	-	-	-	-
RESET COMAND (RES)		/	-	H10 EI	H10 EI	H10 EI	H10 EI	H10 EI	H10 EI	-	-	-	-	-	-	-

(*) When timer is enabled (default)

ACTIVATION/DEACTIVATION FINITE STATE MATRIX IN NT MODE

APPENDIX B
Electrical Parameters

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.3 to 7.0	V
V_{IN}	Input Voltage	– 0.3 to 7.0	V
T_A	Operting Temperature Range	0 to 70	°C
T_{stg}	Storage TemperatureRange	– 55 to 150	°C

TRANSMISSION ELECTRICAL PARAMETERS

Parameter	Min.	Typ.	Max.	Unit
LINE INTERFACE FEATURES				
Differential Input Resistance		140		KΩ
Line Driver Load			1000	pF
Differential Output Offset at LO+ / LO–	– 30	0	30	mV
Power up Output Differential Impedance (20KHz Bandwidth)		1		Ω
Power Down Output Diffrential Impedance	8	12	16	Ω
POWER CONSUMPTION				
I_{CCO}		2		mA
I_{CC1}		55		mA
TRANSMISSION PERFORMANCES				
Transmit Pulse Amplifier		3.2		V
Transmit Pulse Linearity	36	50		dB
Input Pulse Amplitude Differential Between LI+ and LI	±4		±800	mVpk

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	All Dig Inputs			0.7	V
V_{IH}	Input High Voltage	All Dig Inputs	2.2			V
V_{ILX}	Input Low Voltage	MCLK/XTAL Inputs			0.5	V
V_{IHX}	Input High Voltage	MCLK/XTAL Inputs	V_{CC}–0.5		0.7	V
V_{OL}	Output Low Voltage	Br, I_O = +7mA All other Dig Outputs, IO = 1mA			0.4	V
V_{OH}	Output High Voltage	Br, I_O = –7mA All other Dig Outputs, I_O = –1mA All Outputs, I_O = –100µA	2.4 2.4 V_{CC}–0.5			V V V
I_L	Input Current	Any Dig Input, GND < V_{IN} < V_{CC}	–10		10	µA
I_{OZ}	Output Current in High Impedance State (TRISTATE)	Br, INT, LSD, CO, DR GND, V_{OUT} < V_{CC}	–10		10	µA

TIMING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
MASTER CLOCK (timing diagram 15)						
FMCLK	Frequency of MCLK Tolerance	Including Temperature, Aging, Etc...	 –100	15.36	 +100	MHz ppm
	MCLK/XTAL Input Clock Jitter	External Clock Source			50	ns pk-pk
tWMH	Clock Pulse Width, MCLK High Level	$V_{IH} = V_{CC} - 0.5V$	20			ns
tWML	Clock Pulse Width, MCLK Low Level	$V_{IL} = 0.5V$	20			ns
tRM tFM	Rise Time of MCLK Fall Time of MCLK	Used as a Logic Input			10 10	ns ns
DIGITAL INTERFACE (timing diagrams 1 to 12)						
FBCLK	Frequency of BCLK	Formats 1, 2 and 3 Format 4 and GCI Mode	256 512		4095 6144	KHz KHz
tWBH	Clock Pulse Width, BCLK High Level	Measured from V_{IH} to V_{IH}	30			ns
tWBL	Clock Pulse Width, BCLK Low Level	Measured from V_{IL} to V_{IL}	30			ns
tRB	Risae Time of BCLK	Measured from V_{IL} to V_{IH}			15	ns
tFB	Fall Time of BCLK	Measured from V_{IH} to V_{IL}			15	ns
tSFB	Setup Time, FS High or Low to BCLK Low	DSI or GCI Slave Mode only	30			ns
tHBF	Hold Time, BCLK Low to FS High or Low	DSI or GCI Slave Mode only	20			ns
tDBF	Delay Time, BCLK High to FS High or Low	DSI or GCI Master Mode only	–20		20	ns
tDBD	Delay Time, BCLK High to Data Valid	Load = 150pF + 2 LSTTL Loads			80	ns
tDBDZ	Delay Time, BCLK High to Data HZ				50	ns
tDFD	Delay Time, FS High to Data Valid	Load = 150pF + 2 LSTTL Loads See Timing Diagram 9			80	ns
tSDB	Setup Time, Data Valid to BCLK Low		0			ns
tHBD	Hold time, BCLK to Data Invalid		20			ns
tDBT	Delay Time, BCLK High to TSR Low	Load = 100pF + 2 LSTTL Loads			80	ns
tDBTZ	Delay Time, BCLK Low to TSR HZ				50	ns
tDFT	Delay Tie, FS High to TSR Low	Load = 100pF + 2 LSTTL Loads See Timing Diagram 12			80	ns
D PORT IN CONTINUOUS MODE: 16KBITS/SEC (timing diagram 13)						
tSDD	Setup Time, DCLK Low to DX High or Low		50			ns
tHDD	Hold Time, DCLK Low to DX High or Low		50			ns
tDDD	Delay Time, DCLK High to DR High or Low	Load = 50pF + 2 LSTTL Loads			80	ns
MICROWIRE CONTROL INTERFACE (timing diagram 14)						
FCCLK	Frequency of CCLK				5	MHz
tWCH	Clock Pulse Width, CCLK High Level	Measured from V_{IH} to V_{IH}	85			ns
tWCL	Clock Pulse Width, CCLK Low Level	Measured from V_{IL} to V_{IL}	85			ns
tRC	Rise Time of CCLK	Measured from V_{IL} to V_{IH}			15	ns
tFC	Fall Time of CCLK	Measured from V_{IH} to V_{IL}			15	ns
tSSC	Setup Time, CSB Low to CCLK High		60			ns
tHCS	Hold Time, CCLK Low to CSB High		10			ns
tWSH	Duration of CSB High		200			ns
tSIC	Setup Time, CI Valid to CCLK High		25			ns
tHCI	Hold Time, CCLK High to CI Invalid		25			ns
tDSO	Delay Time, CSB Low to CO Valid	Out First Bit on CO			50	ns
tDCO	Delay Time CCLK Low to CO Valid	Load = 50 pF + 2LSTTL Loads			50	ns
tDCOZ	Delay Time, CCLK Low to CO HZ				50	ns
tDCI	Delay Time, CCLK Low to INTB Low or HZ	Load = 80pF + 2LSTTL Loads			50	ns

Figure 11: BCLK, FSA, FSB, SLAVE MODE, DELAYED MODE, FORMATS 1 2 3 (MW ONLY)

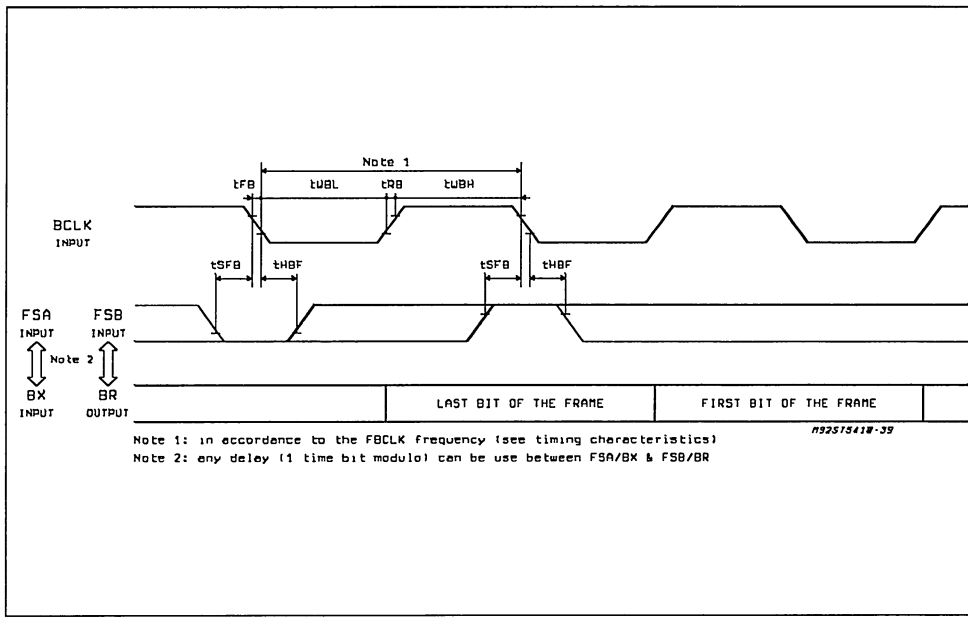


Figure 12: BCLK, FSA, FSB, SLAVE MODE, NON DELAYED MODE, FORMATS 1 3 (MW ONLY)

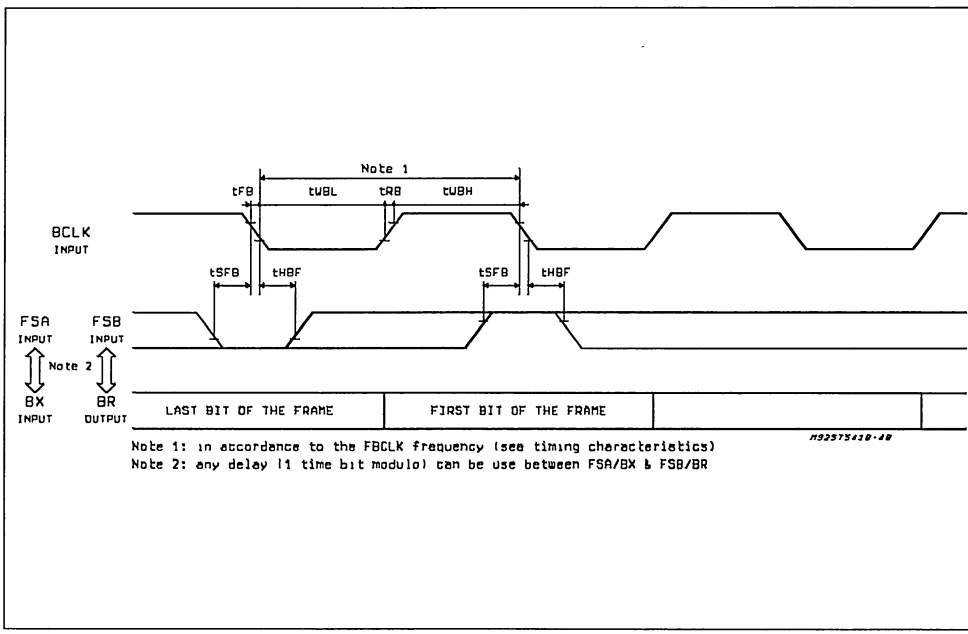


Figure 13: BCLK, FSA, FSB, SLAVE MODE, FORMAT 4 ALWAYS NON DELAYED MODE, (MW and GCI MODE)

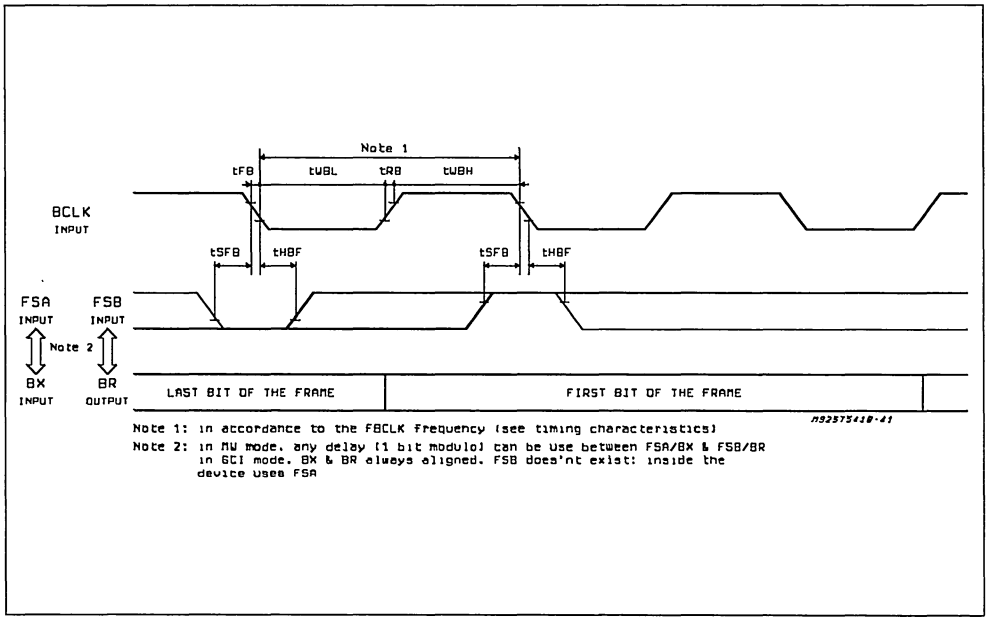


Figure 14: BCLK, FSA, FSB, MASTER MODE, DELAYED MODE, FORMATS 1 2 3 (MW ONLY)

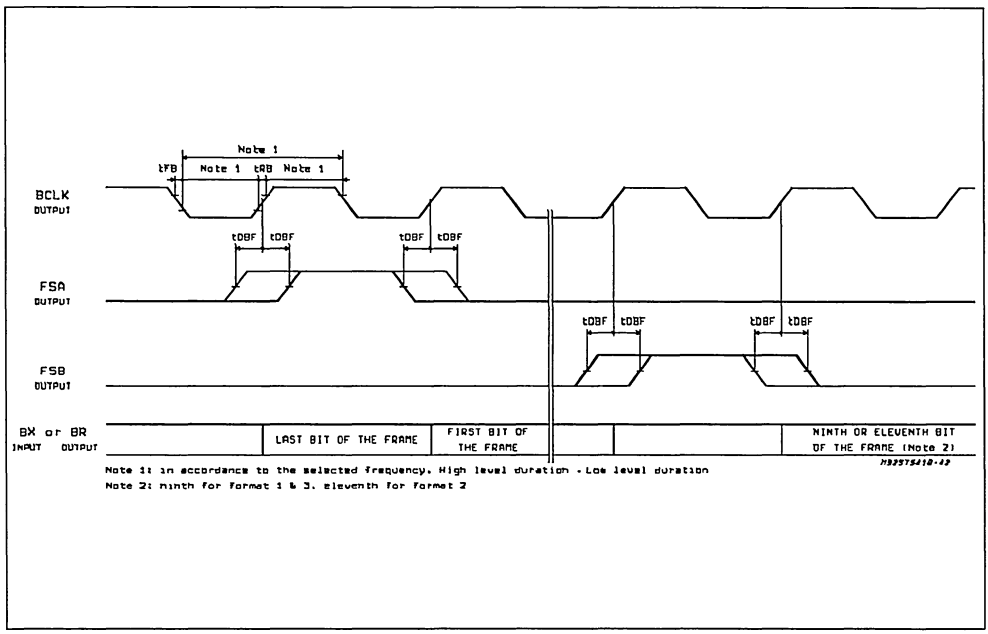


Figure 15: BCLK, FSA, FSB, MASTER MODE, NON DELAYED MODE, FORMATS 1 3 (MW ONLY)

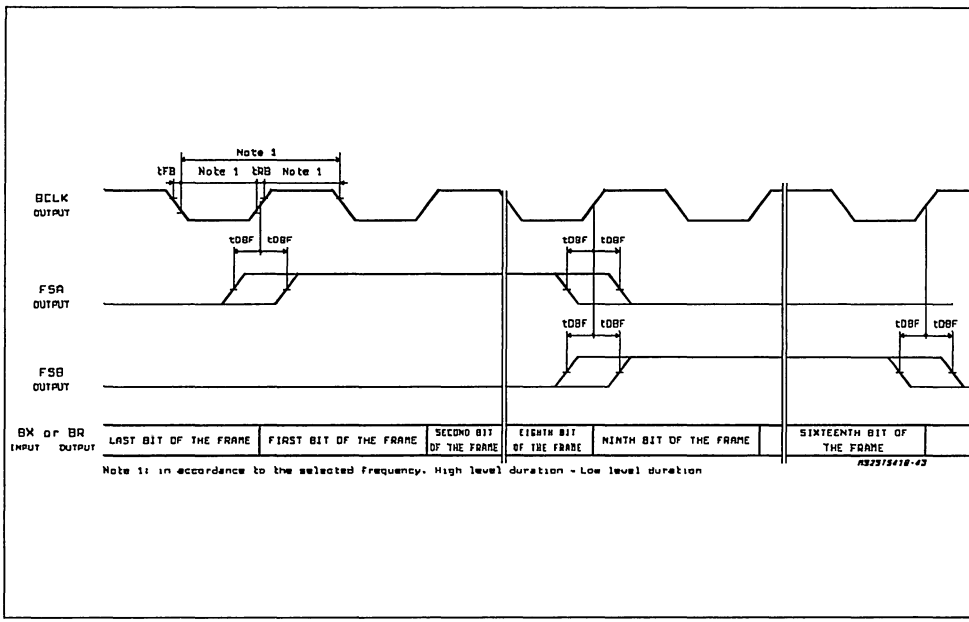


Figure 16: BCLK, FSA, FSB, SLAVE MODE, FORMAT 4 ALWAYS NON DELAYED MODE, (MW and GCI MODE)

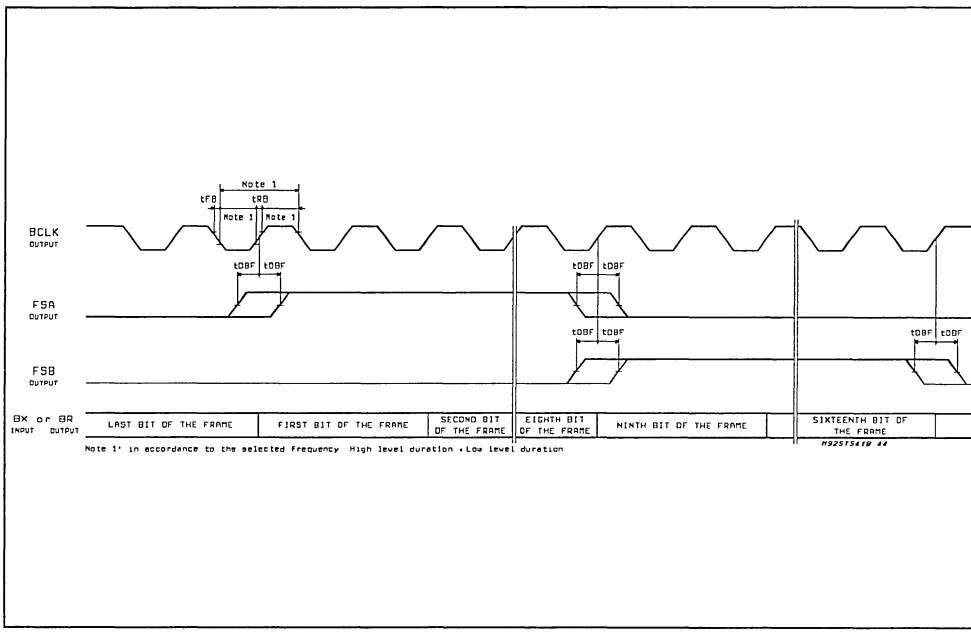


Figure 17: BX, DX, BR, DR, SLAVE & MASTER, DELAYED & NON DELAYED, FORMATS 1 2 3 (MW ONLY)

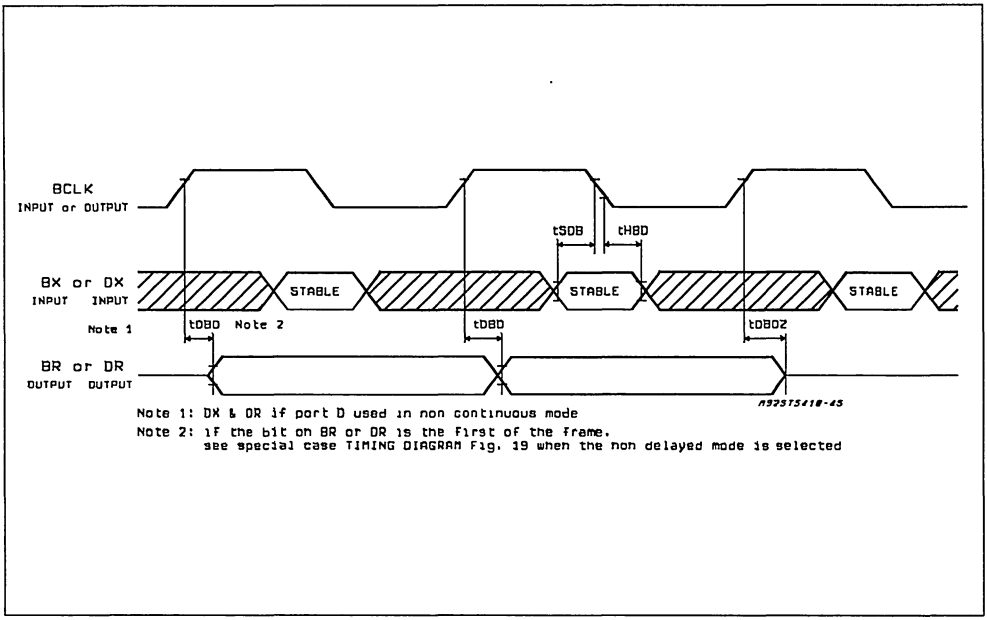


Figure 18: BX, DX, BR, DR, SLAVE & MASTER, FORMAT 4 ALWAYS NON DELAYED, FORMATS 1 2 3 (MW & GCI MODE)

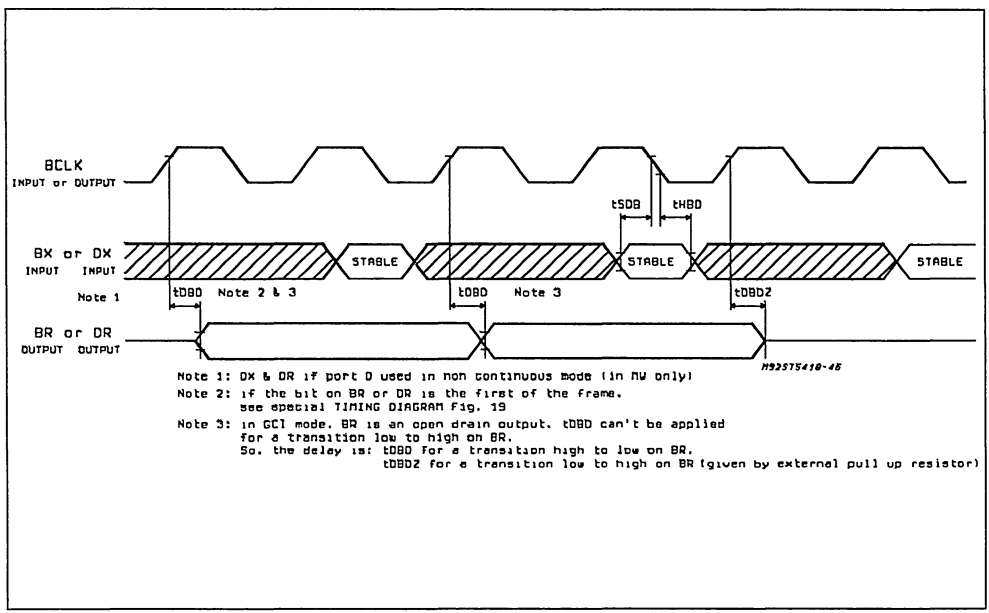


Figure 19: SPECIAL CASE BR, DR, ONLY FIRST BIT OF THE FRAME, IN SLAVE AND NON DELAYED MODES FORMATS 1 3 (MW MODE), FORMAT 4 (MW & GCI MODE)

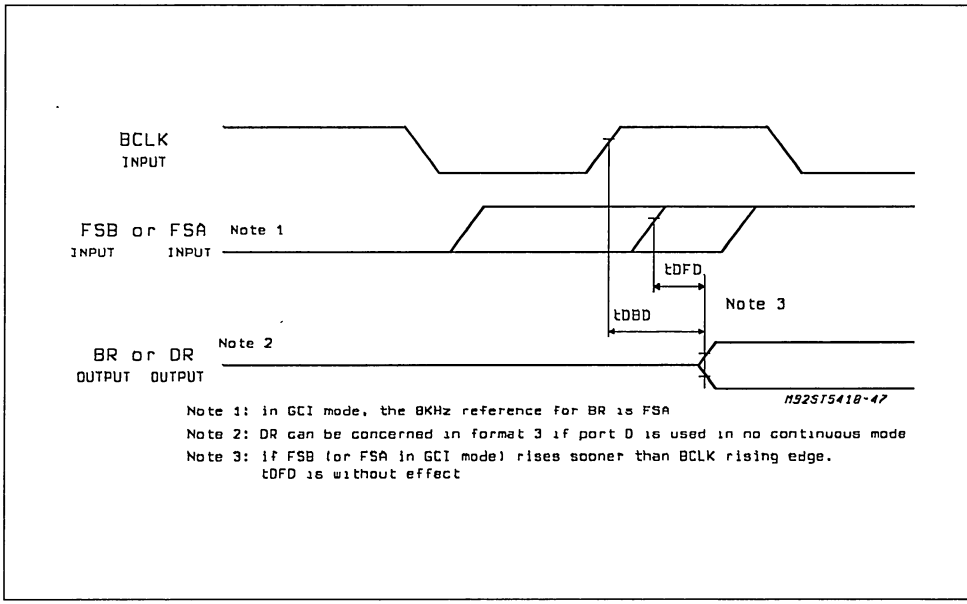


Figure 20: TSRB, SLAVE & MASTER, DELAYED & NON DELAYED, FORMATS 1 2 3 (MW ONLY)

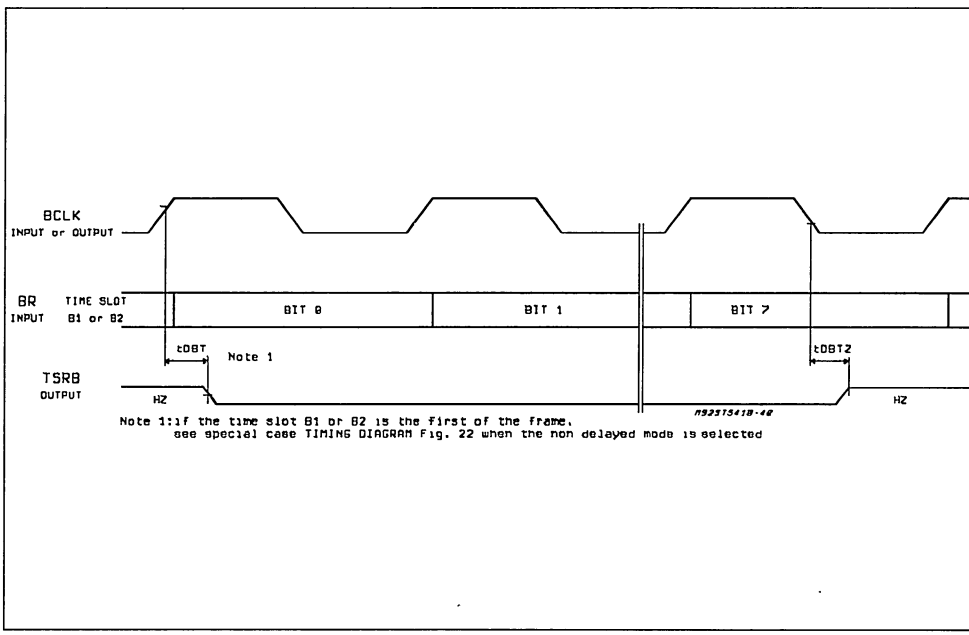


Figure 21: TSRB, SLAVE & MASTER, FORMAT 4 ALWAYS NON DELAYED MODE (MW & GCI)

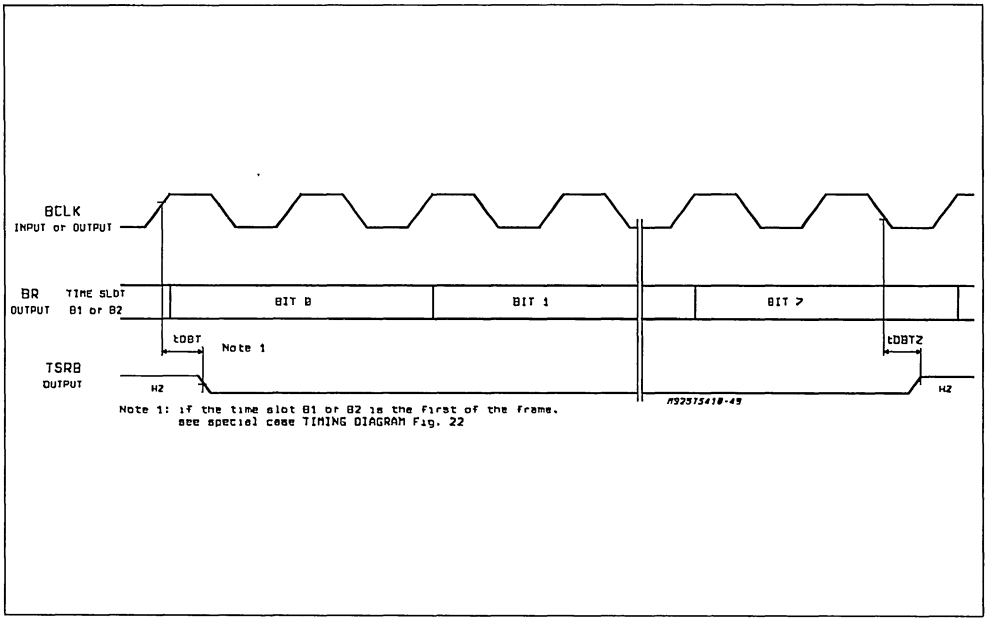


Figure 22: SPECIAL CASE TSRB, B1 OR B2 FIRST CHANNEL OF THE FRAME, IN SLAVE & NON DELAYED MODE, FORMATS 1 3 (MW MODE), FORMAT 4 (MW & GCI MODE)

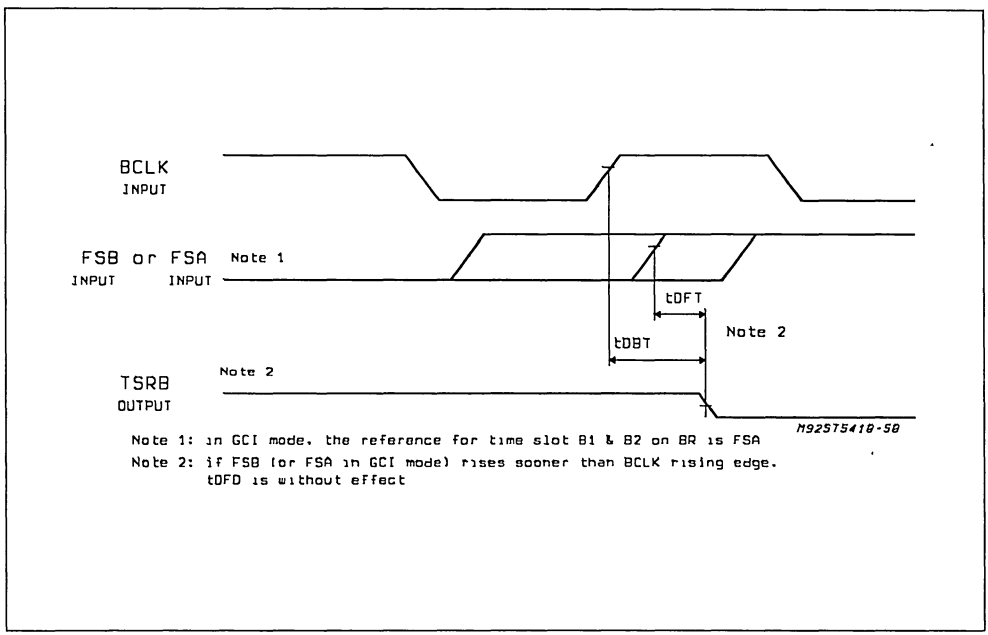


Figure 23: DCLK, DX, DR IN CONTINUOUS MODE SLAVE & MASTER, DELAYED & NON DELAYED MODES ALL FORMATS IN MW MODE ONLY

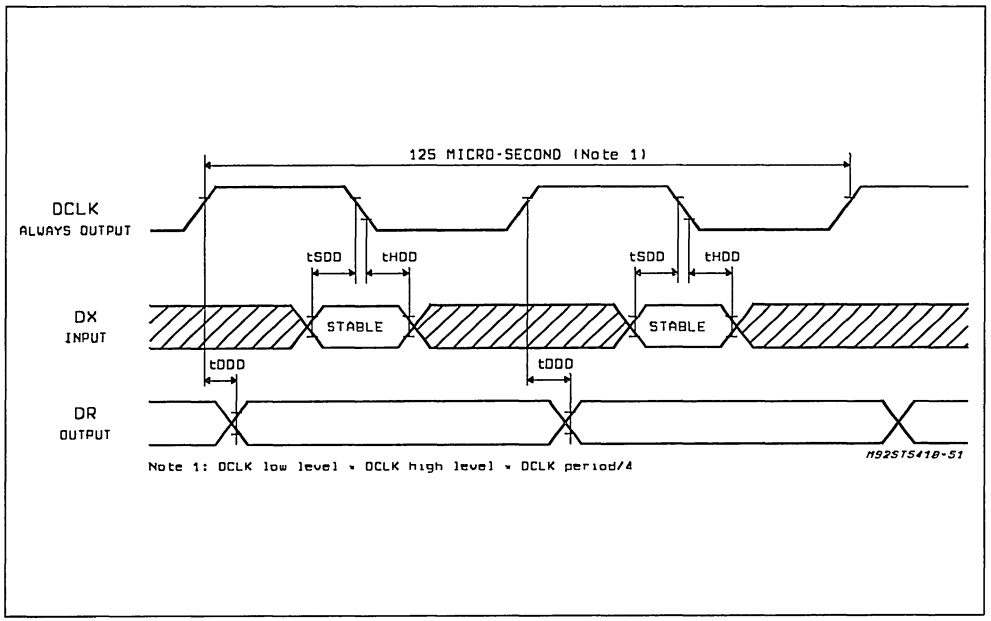


Figure 24: MW PORT

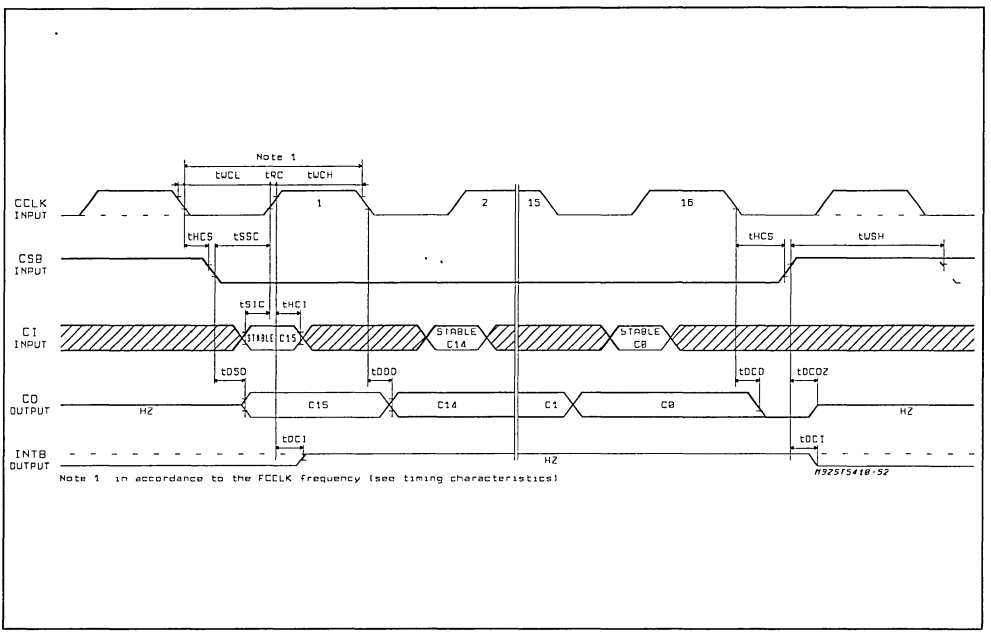
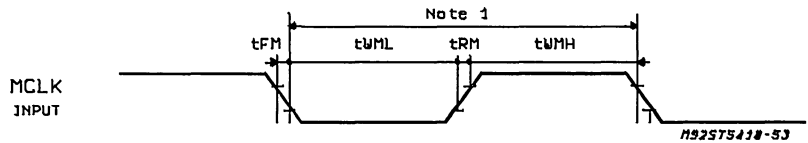


Figure 25: MCLK ALL MODES

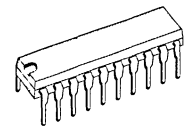


Note 1: In accordance to the FMCLK frequency (see timing characteristics)

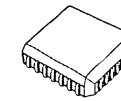
SID-GCI : S/T INTERFACE DEVICE WITH GCI

PRELIMINARY DATA

- SINGLE CHIP 4 WIRES 192kb/s TRANSCEIVER FULLY COMPLYING WITH CCITT I.430
- ISDN BASIC ACCESS HANDLING 144kb/s 2B + D TRANSMISSION
- GCI COMPATIBLE INTERCHIP INTERFACE
- ADAPTIVE AND FIXED TIMING OPTIONS FOR NT
- CLOCK RESYNCHRONIZER AND DATA BUFFERS FOR NT2
- PROGRAMMABLE S1 AND Q CHANNELS HANDLING ACCORDING TO US ANSI STANDARD FOR LAYER 1 MAINTENANCE
- EASILY INTERFACEABLE WITH ST5451 HDLC & GCI CONTROLLER AND ANY OTHER GCI COMPATIBLE DEVICE



DIP20



PLCC28

ORDERING NUMBERS:

ST5421CP ST5421CFN

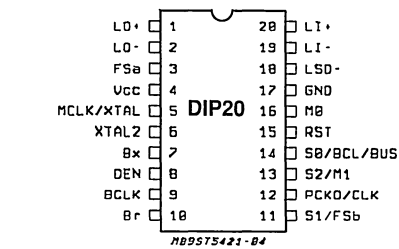
DESCRIPTION

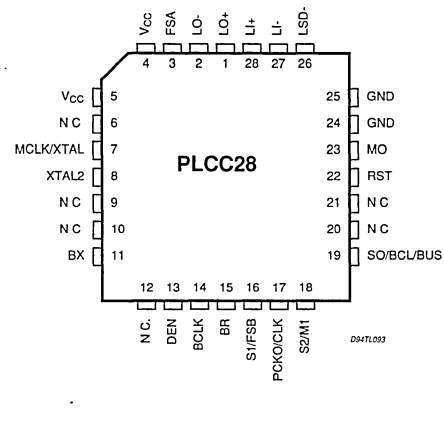
The ST5421 (SID-GCI) is a complete monolithic transceiver for data transmission on twisted pair subscriber loops. It is built on SGS-THOMSON HCMOS 3A double metal advanced process, and requires only a single + 5V supply. All functions specified in CCITT recommendation I.430 for ISDN basic access at the 'S' and 'T' interfaces are provided, and the device can be configured to operate either in TE (Terminal Equipment), in NT1 or NT2 (Network Termination) or in PABX line-card device.

GCI interchip interface highly enhances device connection efficiency by multiplexing controls and data on the same bus and requiring only 4 pins. ST5421 implements all the GCI standard functions for Monitor and Control/Indicate channels, supporting up to 8 GCI peripherals in multiplexed mode.

As specified in I.430, full-duplex transmission at 192kb/s is provided on separate transmit and receive twisted wire pairs using inverted Alternate Mark Inversion (AMI) line coding. Various channels are combined to form the 192kb/s aggregate rate, including 2 'B' channels, each of 64kb/s, and 1 'D' channel at 16kb/s. In addition, multiframe transmission is provided in a switchable processing mode based on United State ANSI standard for Layer 1 maintenance. 800 bit/s message oriented data transmission is supported by S1 and Q channels.

PIN CONNECTIONS (Top views)



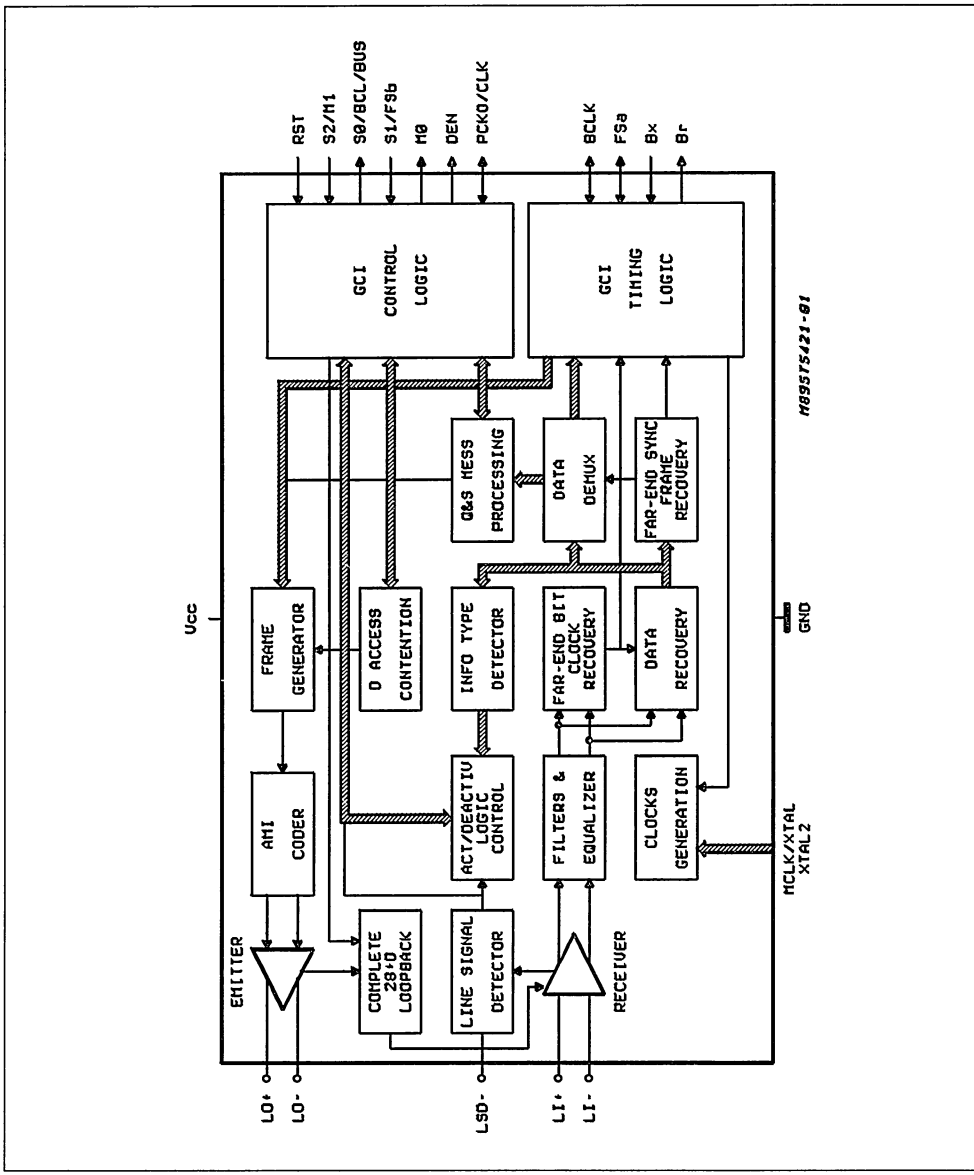


DESCRIPTION (Continued)

All I.430 wiring configurations are supported by ST5421 including passive bus for TE's distributed point-to-point and point-to-multipoint extended. Adaptive receive signal processing enables the device to operate with low bit error rate on any of the standard types of cable pairs commonly found in premise wiring installations when tested with the noise sources specified in I.430.

Far-end Clock Resynchronizer automatically selected, data buffer and slave-slave mode allow design of NT2 trunk-card connected to several T interfaces.

BLOCK DIAGRAM



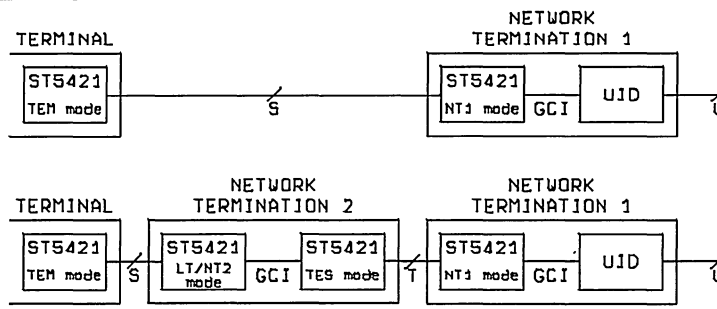
PIN DESCRIPTION

Name	DIP	PLCC	Description
GND	17	24,25	Ground Reference Voltage: all analog and digital signals are referenced to this pin.
V_{CC}	4	4,5	Positive Power Supply Input 5V (± 5%) relative to GND
MCLK/XTAL	5	7	Master Clock or Crystal Oscillator Input: this pin requires either a 15.36MHz crystal (parallel resonant with R_S < 100 Ω) to be tied between this pin and XTAL2 or a logic CMOS level 15.36MHz clock from a stable source. When using a 20pF crystal, a total of 33pF load capacitance to GND must also be connected. In NT configurations. MCLK clock input doesn't need to be synchronous with the Network Reference Clock (FSa).
XTAL2	6	8	Crystal Oscillator Output. This pin should be connected to one end of the 15.36MHz crystal, otherwise is not connected. (see MCLK/XTAL).
BCLK	9	14	Bit Clock: this signal determines the data shift rate at GCI. Data is shifted-in on Bx and shifted-out on Br at half the BCLK frequency. When NT/TES mode is selected, BCLK is an input which does not need to be synchronous with the Master Clock input (MCLK). When TEM is selected, BCLK is an output at frequency of 1536kHz. This clock is phase locked to the receive line signal and synchronous with FSa output.
FSa	3	3	Frame Synchronization Clock: 8kHz clock which defines the start of the frame. In GCI slave (NT/TES) FSa is an input used as a network reference clock for S/T line. In GCI master (TEM) is an output applicable as a validation strobe for the first B channel.
S1/FSb	11	16	S1 if M0 = 1; is GCI channel number selection (input). FSb if M0 = 0 and M1 = 0 (TEM): is a data strobe indicating the active slot for the second B channel on the GCI (output). In NT1 mode, M0 = 0; M1 = 1, this pin is not used and must be left floating.
Bx	7	11	Digital Input for GCI Channels: data to be transmitted to S line is shifted-in at half the BCLK frequency on the 2nd falling edge.
Br	10	15	Digital Output for GCI Channel (OPENDRAIN): data is shifted-out at half the BCLK frequency on the transmit rising edges of BCLK. An external pull-up resistor is needed.
DEN	8	13	In TEM mode DEN is an output, normally low, that pulses high to indicate the active time slot for D channel data at the Bx input. It is intended to be gated with BCLK to control the D channel shifting from a layer 2 device (i.e. ST5451) to ST5421 transmit buffer. Using ST5451 HDCL/GCI controller, no external circuitry is needed. In NT/TES mode this pin is not used and must be kept floating.
Not Connected	–	6,9,10, 12,20,21	Leave open on the board.
PCK0/CLK	12	17	PCK0 IN TEM, LT/NT2, NT1 mode: 32 kHz clock output synchronized to GCI clocks. It is intended to synchronize DC/DC converter in TEM mode. CLK in TES mode: is a clock signal open drain output phased-locked to the receive S line signal and applicable as far-end clock reference. Its frequency is 1536kHz compatible with 768kbit/s GCI data rate. An external pull-up resistor is needed.
M0	16	23	M0 = 0: GCI mode selection; Time slot Assigner is selected on GCI channel 0. M0 = 1: GCI in a multiplex mode; S0, S1, S2 pins define the GCI channel number allocated to ST5421. TES/NT2 selection is done with the configuration registers (input).

PIN DESCRIPTION (continued)

Name	DIP	PLCC	Description
S2/M1	13	18	S2 if M0 = 1: GCI channel number selection (input). When M0 = 0 M1 select TEM or NT1 mode: M1 = 0 selects TEM, M1 = 1 selects NT1.
S0/BCL/BUS	14	19	S0 if M0 = 1; GCI channel number selection (input). BCL in TEM; bit clock output at 768kHz compatible with COMBO families ETC5054/57. BUS in NT1; S Bus Configuration Selection: low for fixed timing recovery and high for adaptive timing recovery (input).
RST	15	22	Reset Pin: must be low at Power On Reset; after, a high pulse on this pin reset ST5421 in a state depending on the other configuration pins (input).
LSD-	18	26	Line Signal Detect: open drain output, normally high impedance, pulling low when SID-GCI is powered down and an S line signal is detected. It is applicable to wake up a microprocessor from a low power idle mode. LSD$^-$ output goes back to high impedance when ST5421 is powered up.
LO+, LO-	1,2	1,2	Transmit AMI signal differential outputs to the S/T line transformer; when used with an appropriate 2:1 step down transformer, the line signal conforms to the output pulse masks in CCITT I.430.
LI$^-$,LI$^+$	19,20	27,28	Receive AMI signal inputs from the S/T line transformer. They should be connected to an appropriate 1:2 or 1:1 transformer through a line coupling circuit to conform I.430 recommendation. LI$^-$ pin is also the internal voltage reference pin.

Table 1: Pin configurations



	TEM	LT/NT2(1)	TES (1)	NT1
M0	i=0	i=1	i=1	i=0
DEN	o=DEN			
S2/M1	i=M1=0	i=S2	i=S2	i=M1=1
S1/FSb	o=FSb	i=S1	i=S1	Not used
S0/BCL/BUS	o=BCL	i=S0	i=S0	i=BUS
PCKO/CLK	o=PCKO	o=PCKO	o=CLK	o=PCKO

M89ST5421-86

(1) differentiation between TES and LT/NT2 is done by register programming.
Default value after reset is LT/NT2 in adaptive timing recovery configuration.

FUNCTIONAL DESCRIPTION

POWER ON INITIALIZATION

Following initial application of power, SID-GCI enters the power down de-activated state.
RST input must be tied low during power-on.

After Power on reset, all the internal I.430 circuits including the master oscillator are inactive and in a low power state except for the line signal detection circuit.

After any period of activity a high pulse on RST reset completely SID-GCI.

Configuration mode programming of SID-GCI is done by means of pins polarization and register programming.

NT1 and TEM modes are defined only by means of 2 configuration pins M0, M1 at Power On Reset.

For NT2 and TES modes (M0=1), configuration has to be completed by means of a Control Instruction on Monitor channel prior a Power Up instruction.

POWER UP/DOWN CONTROL

When TEM configuration is selected, ST5421 provides GCI Clocks needed for control channel transfer. Power Up instruction is directly provided by pulling low the Bx data input. SID-GCI then reacts sending GCI clocks. LSD- output pin can be directly connected to Bx data input for providing an automatic Power up when far-end attempts to activate.
After a period of activity, Power down state is normally re-entered by C/I control code DC (1111) while ST5421 is sending C/I indication code DP (0000); then ST5421 send twice C/I indication code DI(1111) before to power down.
It is possible to force immediately power down state by using PDN (0001) C/I control code.

When NT1 configuration is selected, ST5421 is powered up directly by receiving GCI clocks on BCLK and FSa input from the "U" device. The only way to power down ST5421 is to stop BCLK or FSa clock signal inputs.
For example PDN (0001) C/I control code has no effect.

When NT2 or TES configuration is selected, SID-GCI is powered up by the PUP code (0000) on C/I Control Channel. After a period of activity, Power down state is normally reentred by C/I control code DC (1111) while ST5421 is sending C/I indication DI(1111).
It is possible to force immediately Power down state by using PDN (0001) C/I control code. In NT1, NT2 or TES mode, loss of GCI clocks automatically forces the power down state.

POWER UP/DOWN STATE

Following a period of activity in the power up state, power down state may be re-entered as described above. Configuration Registers remain in their current state. They can be changed by the GCI Monitor channel.

The power down transition disables analog and I.430 circuitry, stops the Crystal Oscillator and all the clocks internally generated. Line Signal Detector Circuit remains active allowing LSD-pin to pull low if a receive signal is detected.

Power up transition enables all analog and I.430 circuitry, starts the Crystal oscillator and reset the state machine to the de-activated state. It also inhibits LSD-output.

LINE CODING AND FRAME FORMAT

For both directions of transmission, Alternate Mark Inversion (AMI) coding with inverted binary is used, as illustrated in figure 1.

This coding rule requires that a binary ONE is represented by a 0 current high impedance output, whereas a binary ZERO is represented by a positive or negative-going 100% duty cycle pulse. Normally, binary ZEROs alternate in polarity to maintain a d.c. balanced line signal.

The frame format used in SID-GCI follows CCITT reccommendation in I.430 and illustrated in figure 2. Each complete frame consists of 48 bits, with a line bit rate of 192kbit/s, giving a frame repetition rate of 4kHz. A violation of the AMI coding rule is used to indicate a frame boundary, by using a 0+ bit followed by a 0- balance bit to indicate the start of a frame, and by forcing the first binary zero following the balance bit to be of the same polarity as the balance bit.

In the Network Termination (NT) to Terminal Equipment (TE) transmission direction, the frame contains in addition to the 2B+D basic access data, an echo channel, the E bit, which is used to retransmit the D bits that are received from the TE (s), and three extra channels: FA, M and S bit.

In the TE to NT direction, the frame contains in addition to the 2B + D data, an extra channel, the FA bit.

FA, M and S bits are used to set up a Q multiframe channel in the TE or NT direction, and a S1 multiframe channel from NT to TE. These 800bit/s message oriented channels are structured on the base of the United States ANSI standard specification for layer 1 maintenance.

Figure 1: Inverted AMI Line-coding Rule.

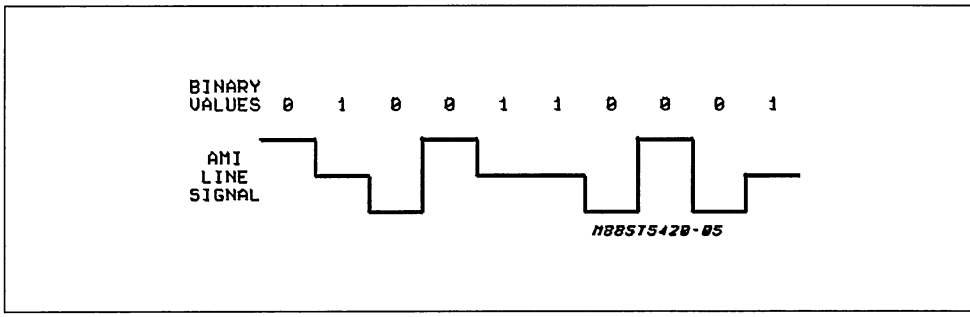
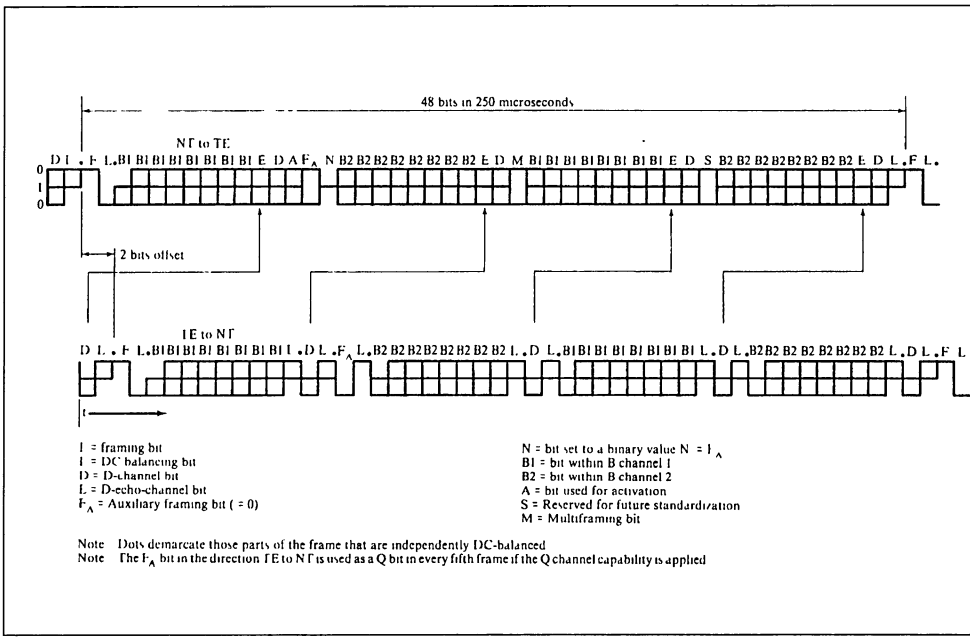


Figure 2: Frame Format



LINE TRANSMIT SECTION

The differential line driver outputs LO+ and LO- are designed to drive a suitable transformer with an external termination resistor. A 2:1 transformer, results in a signal amplitude of 750mV on the line which meets the I.430 pulse shape for all the loads specified.

When driving a binary 1 symbol, the output presents a high impedance in accordance with I.430. When driving a 0+ or 0- symbol, the voltage limited current source is turned on.

Short protection is included in the output stage.

Overvoltage protection is required externally.

Depending on TE or NT selected configuration, 192kbit/s data is transmitted on LO+,LO- by means of clocks respectively locked on the far-end received bit and frame clocks recovered from the line with two bit delay between transmit and receive frame, or locked with a fixed delay on the Frame Sync signal received from FSa input.

LINE RECEIVE SECTION

The receive input signal should be derived via a 1:1 a or 1:2 transformer of the same type used for

the transmit direction. At the front end of the receive section is a continuous filter which limits the noise bandwith. To improve the protection of the line interface and to comply with the receive input impedance specification even if power is lost, it is necessary to add 3 external resistors between the receive transformer and the LI+/LI- pins.

To correct pulse attenuation and distorsion caused by the transmission line in point-to-point and extended passive bus applications, an adaptive equalizer enhances the received pulse shape, thereby restoring a "flat" channel response with maximum eye opening over a wide spread of cable attenuation characteristics.

This equalizer is always enabled when either TE or NT mode adaptive sampling is selected, but is disabled for NT short passive bus applications, when NT mode fixed sampling is selected.

An adaptive threshold circuit maximizes Signal to Noise ratio in the eye at the detector for all loop conditions.

A DPLL (Digital Phase-Locked Loop) recovers a low-jitter clock for optimum sampling of the received symbols.

The MCLK input provides the reference clock for the DPLL at 15.36MHz.

When the device is powered down, a Line Signal Detect circuit, able to discriminate a valid line signal from noise, is enabled to detect the presence of incoming data. LSD-output pulls low to wake up the equipment.

GCI INTERFACE

General Description

GCI interface is an European standardized interface to connect ISDN dedicated components in the different configurations of equipment as Terminals, Network Terminations, PBX, etc...

In Terminal Equipments, this interface allows connection between SID-GCI and an associated ST5451 HDLC&GCI Controller used for 16kbit/s D channel processing and SID-GCI control. 64kbit/s B1 and B2 channels are transferred on GCI interface providing direct connection for B channel processing peripherals like Programmable ISDN COMBO ST5080 or extra ST5451 controllers.

In NT2 or PBX line card, GCI interface permits connection of up to 8 SID-GCI onto a common serial multiplexed bus. Each SID-GCI is assigned to one GCI channel selected by hardware configuration.

Figure 3 shows the Frame structure of a GCI channel. One GCI channel is structured in four subchannels:

- B1 channel 8 bits
- B2 channel 8 bits
- Monitor (M) channel 8 bits
- SC channel which is structured as follows:
  - D channel 2 bits
  - C/I channel 4 bits
  - A bit associated with M channel
  - E bit associated with M channel

B1,B2 and D channels are used to transfer 2B + D basic access data.

M channel is used to read and write multiframe S1 and Q channel messages and to configurate SID-GCI. Protocol for byte exchange on the M channel uses the E and A bits.

C/I (Control/Indicate) channel is used to exchange "real time" primitives between the SID-GCI and the Controller as Activation/Deactivation codes.

Physical Description

The interface consists of 4 wires:

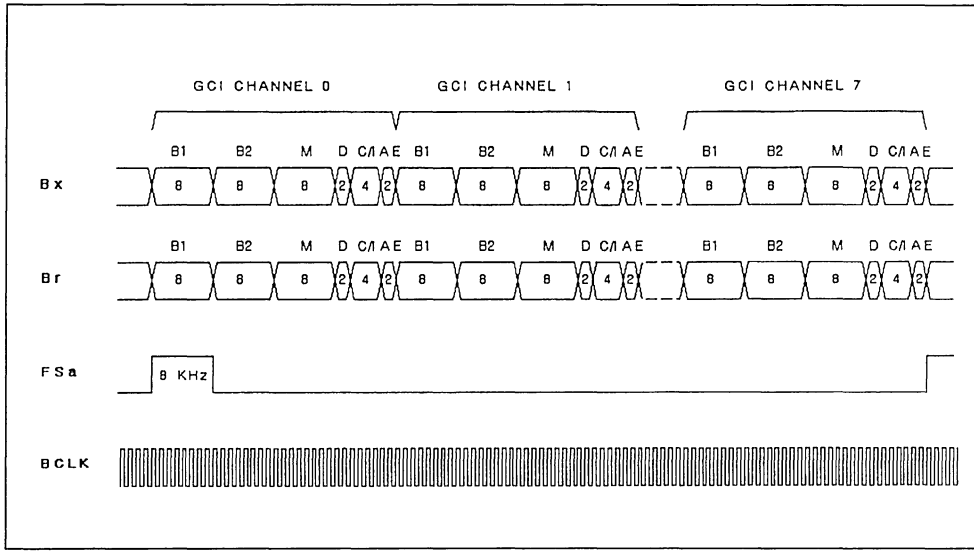
- Input Data: Bx
- Output Data: Br
- Bit Clock: BCLK
- Frame Synchronization: FSa

Data is synchronized by BCLK and FSa signals. The latter insures reinitialization of a time slot counter at each frame beginning. Its rising edge is the reference for the first bit of the first GCI channel. Data is transmitted in both directions at half the BCLK frequency, on the rising edge of BCLK and is sampled 1.5 period after the transmit rising edge. Unused channels are high impedance.

In NT2 or PABX equipments, up to 8 GCI channels (32 bits each) may be multiplexed on Bx and Br links used as a serial bus for several devices. The channel number selection is made by programming pins S0,S1 and S2 according to the following rules:

S2	S1	S0	Channel Number	Timeslots
0	0	0	0	0 -3
0	0	1	1	4 - 7
0	1	0	2	8 - 11
0	1	1	3	12 - 15
1	0	0	4	16 - 19
1	0	1	5	20 - 23
1	1	0	6	24 - 27
1	1	1	7	28 - 31

Figure 3: GCI Interface Structure



BCLK frequency may be any value between 512 and 6176kHz.

In TEM and NT1 configurations, the first GCI channels is automatically selected.

In TEM configuration, due to SID-GCI recovery circuitry, a low jitter should be provided on FSa and BCLK clocks. FSa and BCLK are always in phase. The maximum value of jitter amplitude is a step of 65ns at each GCI frame (125µs). The maximum high frequency jitter amplitude is 130ns pk-pk.

For applications such as the network side of an NT2, eg, a PABX trunk card, TES mode allows the transmission side of SID-GCI to be a slave to the received frame timing while GCI is also in slave mode Elastic buffers which allow any phase relationship between FSa and I.430 frames and a clock resynchroniser circuit absorb jitter and low frequency wander up to at least 18µs pk-pk at frequencies below 10Hz.

Exchange Protocol on the C/I channel

Exchange of information in the C/I channel runs as follows:

Two devices connected on a GCI channel send each other a permanent four bit command code in the C/I field. The same code is sent at a 8kHz frequency as long as the content of the internal C/I register remains unchanged.

When a change of C/I the command is initiated that is recognized by SID-GCI if detected in two consecutive frames.

ST5421 will interpret the new code and send the corresponding control instructions on the S line or switch a local function as long as the corresponding action is required.

An information change received from the S line or a local status change of SID-GCI set a new indication code on the C/I channel. The code is sent at least in 2 consecutive frames.

Table 2 gives the C/I codes meaning. C1 bit is first transmitted.

Here after for each mode a list of recognized Control and Indicate codes is given.

TEM mode: Control

0000 (DR) : Deactivation Request
In the Power Up state, DR instruction can be used as a Deactivation Request instruction to force transmission of INFO0 on the S line.

0001 (PDN) : Power Down Request.
PDN instruction forces the device to the Power Down state after that DI (1111) has been sent in two consecutive frames.

1000 (AR8) : Activate Request Class 8.
AR8 instruction combines an Activation Request, which initiates the Activation Sequence on the line, and a request to attempt to access the transmit D channel in the high priority class at the S interface after its complete activation. After activation of the S interface, AI8 indication is sent by ST5421. D channel access attempt is

Table 2: C/I Channel Coding

Code	TEM		LT/NT2		TES		NT1	
C1 C2 C3 C4	Ind.	Com.	Ind.	Com.	Ind.	Com.	Ind.	Com.
0000	DP	DR	TIM	PUP/DR	DP	PUP/DR	TIM	DR
0001	X	PDN	X	PDN	X	PDN	X	X
0010	X	X	X	X	X	X	X	X
0011	EOM	X	X	X	X	X	X	X
0100	EI	X	EI	X	EI	X	EI	FI2
0101	X	X	X	X	X	X	X	X
0110	X	X	X	X	X	X	X	X
0111	X	X	X	X	X	X	X	X
1000	AP	AR8	AP	AR	AP	AR	AP	AR
1001	CON	AR10	X	X	X	X	X	X
1010	X	ARL	X	ARL	X	ARL	X	ARL
1011	X	X	X	X	X	X	X	X
1100	AI8	X	AI	FI4	AI	X	AI	FI4
1101	AI10	X	X	X	X	X	X	X
1110	AIL	X	AIL	X	AIL	X	AIL	X
1111	DI	DC	DI	DC	DI	DC	DI	DC

(x) codes reserved

automatically processed for each HDLC frame to be transmitted without need for new Control Instruction.
Except for code EOM, any further indication change on C/I as CON or EI deactivates D channel access attempt at the S interface. A new AR8 instruction is needed to restart the procedure.
Note : A new AR8 instruction means that if the controller was already sending AR8, it has to change first the code sent to ie DC (1111) and after change again to AR8.

1001 (AR10) : Activate Request Class 10.
Same meaning as AR8 command but requesting access to transmit D channel with low priority class.
After activation of the S interface has been completed, AI10 indication is sent by SID-GCI.

1010 (ARL) : Activate Request Loopback.
ARL instruction operates a loopback of 2B + D channels from Bx input to Br output. It may be set when the device is either activated, in which case it is transparent (the composite signal is also transmitted to the line), or when it is deactivated in which case it is non transparent.
Any change from ARL to another C/I command clears the loopback.
When the complete loopback is activated, (AIL) code is sent by SID-GCI.

1111 (DC) : Deactivation Control.
DC instruction allows ST5421 to enter automatically the Power Down state if the S line is deactivated (DP sent by SID-GCI). When S line is not deactivated, DC has no effect.

TEM mode : Indication

0000 (DP) : Deactivation Pending Indication.
DP code indicates ST5421 is powered up and that no identified signal has been detected on the S line. DP indication is sent when one of the following events occur :
- Power Up has been completed and no signal is identified on the line,
- after a period of activity, INFO0 is detected on the S line,
- the device being in status F4, F5, F6, F7 or, F8, a DR instruction is issued.

0011 (EOM) : End of Message.
EOM indicates that the closing flag of a D channel message has been transmitted on S line indicating successfull completion of a packet sending. EOM is sent continuously until receiving of a new AR8 or AR10 command or line status change.
EOM code sending can be disabled via a Monitor channel instruction EID : (see table 3).

0100 (EI) : Error Indication.
EI indicates that a frame loss of has been detected on S line ; is sent when one of the following events occur :
- being in the F6 or F7 states, detection of a loss of frame, (jump to F8).

- being in the F7 state, receiving of INFO2, (jump to F6).

1000 (AP) : Activation Pending.
AP indicates that INFO2 (or INFO4) frames have been identified on the line.
AP indication is sent when one of the following events occur:
- being in F2 deactivated state, detection of INFO2 or INFO4.
- being in the loss framing state F8, detection of INFO2

1001 (CON) : Contention Indication
CON is sent when, during transmission of a packet in the D channel, a received E bit does not match the last transmitted D bit, indicating a lost collision.
D channel access attempt is deactivated at the S interface. A new AR8 or AR10 instruction is needed to restart the procedure.

1100 (AI8) : Activation Indication Class 8.
AI8 is sent when, following an AR8 instruction, the S line is completely activated (state F7). The D channel access procedure is set in the high priority class 8 (or 9).

1101 (AI10) : Activation Indication Class 10.
AI10 is sent when, following an AR10 instruction, the S line is completely activated. The D channel access procedure is set in the low priority class 10 (or 11).

1110 (AIL) : Activation Indication Loopback.
AIL indicates that the complete loopback requested by the instruction ARL is completed.

1111 (DI) : Deactivation Indication.
DI is sent at least in two consecutive frames when, being in the S line deactivated state (DP indication sent by SID-GCI) DC control instruction is received on C/I control channel.
After that, SID-GCI is automatically powered down.

TES mode : Control.

0000 (PUP/DR) : Power Up Request/Deactivation Request.
When in Power Down, Power Up instruction powers up the device in the configuration previously set. When in Power Up, PUP/DR can be used as a Deactivation Request instruction to force the transmission of INFO0 on the line.

0001 (PDN) : Power Down Request.
PDN instruction forces the device to the Power Down state.

1000 (AR) : Activate Request.
AR instruction initiates the Activation Sequence on the line. It is recommended that an AR be delayed at least 2ms after the PUP instruction.

1010 (ARL) : Activate Request Loopback.
Identical to TEM mode.

1111 (DC) : Deactivation Control.
DC instruction allows ST5421 to enter automatically the Power Down state if the S line is deactivated (DI sent by SID-GCI). When S line is not deactivated, DC has no effect.

TES mode : Indication.

0000 (DP) : Deactivation Pending.
DP code indicates ST5421 has been just powered up and no signal has been identified on the line.

0100 (EI) : Error Indication.
Identical to TEM mode.

1000 (AP) : Activation Pending.
Identical to TEM mode.

1100 (AI) : Activation Indication.
AI is sent when, following an AR instruction, the S line is completely activated in state F7.

1110 (AIL) : Activation Indication Loopback.
Identical to TEM mode.

1111 (DI) : Deactivation indication.
DI indication is sent when one of the following events occur:
- After a period of activity, INFO0 is detected on the S line,
- the device beeing in status F4, F5, F6, F7 or F8, DR instructions is issued.

NT1 mode : Control.

0000 (DR) : Deactivation Request.
DR command forces ST5421 through the appropriate deactivation sequence where INFO0 is sent on the line. The device remains in the Power Up state. DI indication is sent.

0100 (FI2) : Force Info 2
Being in the activated state G3, FI2 instruction forces the appropriate sequence to send INFO2 on the line. If the S line is not completely activated, FI2 instruction has no effect.

1000 (AR) : Activation Request.
Being in the inactive Power Up state, sending INFO0, AR instruction forces SID-GCI through the appropriate sequence to send INFO2 on the line. It is recommended that an AR instruction be delayed at least 2ms after setting the GCI clocks.

1010 (ARL): Activate Request Loopback.
Identical to TEM mode.

1100 (FI4) : Force Info 4.
An activation Request being in progress, FI4 instruction allows SID-GCI through the appropriate sequence to send INFO4 on the line.

1111 (DC) : Deactivation Control.
DC instruction has no effect on SID-GCI.

NT1 mode : Indication.

0000 (TIM) : Timing Requested.
Being in Power down state, the LSD- output is pulled low to indicate that the far-end is attempting to activate the S interface. The device requests GCI clock signals. Receiving of GCI clocks powers up the SID-GCI, LSD- is freed, and TIM code is sent on the C/I channel.

0100 (EI) : Error Indication.
EI code indicates that a loss of frame has been detected on the S line, ST5421 being previously activated.

1000 (AP) : Activation Pending.
AP code indicates that INFO1 frames have been identified of the line. The device is waiting for an activate request to send INFO2.

1100 (AI) : Activation Indication.
AI code indicates that the S line is activated. That means it is receiving INFO3.

1111 (DI) : Deactivation Indication.
DI code indicates S line is completely deactivated: the device can be powered down switching off GCI clocks.

1110 (AIL) : Activation Indication Loopback.
Identical to TEM mode.

NT2 mode : Control.

0000 (PUP/DR) Power Up Request/Deactivation Request.
When in Power Down state, PUP code powers up the device in the NT2 configuration previously selected. When in Power Up state DR code forces the appropriate deactivation sequence where INFO0 is sent on the line. SID-GCI remains in Power Up state.

0001 (PDN) : Power Down Request.
Identical to TES mode.

1000 (AR) : Activation Request.
After a PUP instruction, AR forces the appropriate sequence to send INFO2 on the line. It is recommended that AR instruction is sent after receiving TIM indication..

1010 (ARL) : Activation Request Loopback.
Identical to TEM mode.

1100 (FI4) : Force Info 4.
An Activation Request being in progress, FI4 instruction puts ST5421 through the appropriate sequence to send INFO4 on the line.

1111 (DC) : Deactivation Control.
The DC instruction allows to enter the power down state if the S line is deactivated.
DC control has no effect if SID-GCI not sending DI indication.

NT2 mode : Indication.

0000 (TIM) : Timing Requested.
Being in Power down state, LSD- output is pulled low to indicate that far-end is attempting to activate the interface. SID-GCI requests GCI clocks followed by a PUP instruction. After receiving, LSD- is freed and TIM is sent on C/I channel.

0100 (EI) : Error Indication.
Identical to NT1 mode.

1000 (AP) : Activation Pending.
Identical to NT1 mode.

1101 (AI) : Activation Indication.
Identical to NT1 mode.

1110 (AIL) : Activation Indication Loopback.
Identical to TEM mode.

1111 (DI) : Deactivation Indication.
The DI code indicates that the S line is completely deactivated.

EXCHANGE PROTOCOL ON M CHANNEL

Protocol allows a bidirectional transfer of bytes between SID-GCI and a Controller (for example ST5451) with an acknowledgement at each received byte.

Write cycle.
The Controller sends to ST5421 control instruction(s) coded on a single byte. It is possible but optional to write several control instructions in a single message. Control instruction bytes are structured as defined in Table 3.

Read cycle.
When a new validated S1 or Q message is received from the line, the device send a single byte message as defined in table 4. If a new message is received from the S line before the previous is acknowledged by the controller end, this new message is lost.

Exchange protocol.
The exchange protocol is identical for both directions.

The sender uses E bit to indicate that it is sending a M byte while the receiver uses A bit to acknowledge the received byte.

When no message is transferred, E bit and A bit are forced to inactive state (i.e. high impedance).

A transmission is initialized by the sender setting E bit in active state and sending the first byte on M channel in the same frame. Transmission of a message is allowed only if A bit received has been detected inactive in the last two frames.

When the receiver is ready, it validates the received byte internally when it has been detected identical in two consecutive frames. Then, the receiver set first A bit from inactive to active state; it is the pre-acknowledgement, and maintain A bit active at least in the following frame, it is the acknowledgement.
If validation is not possible, the two last bytes received not identical, the receiver abort the message by setting A bit active for one frame only.

A second M byte may be transmitted by the sender turning E bit from active to inactive state and sending the byte in the same frame. The E bit is set inactive for one frame only. If it remains inactive more than one frame, it is an end of message. The second byte may be transmitted only after receiving the pre-acknowledgement of the previous byte (see timing diagram).

The receiver validates the current received byte as for the first one and then set A bit in the next two frames first from active to inactive state (pre-acknowledgement) and from inactive to active (acknowledgement). If the receiver cannot validate (the two bytes received are not identical) it pre-acknowledges normally but let A bit in the inactive state in the next frame which indicates an abort request.

If a message is aborted, ST5421 sends again the complete message until receiving acknowledgement.
A received message is acknowledged or aborted without flow Control.
Figure 4 gives the timing of a write cycle. The most significant bit of a Monitor byte is sent first of the M channel. E & A bits are active low and inactive state on Br is high impedance.

Figure 4: Monitor messaging

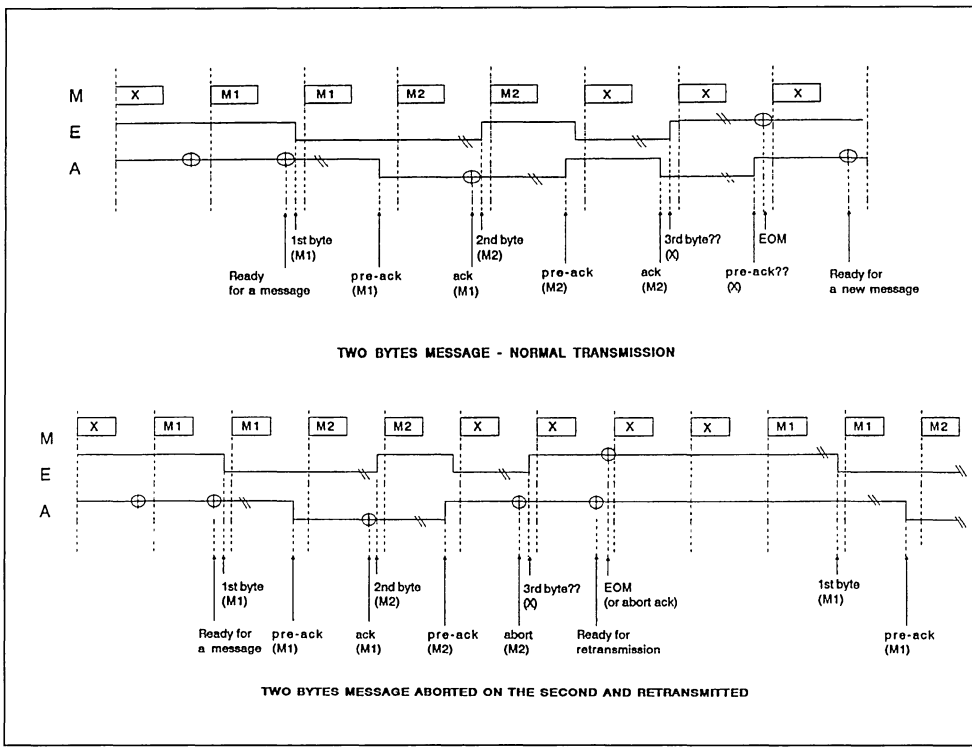


Table 3: Monitor Channel Instruction

Functions	Mnemonic	Bit Number							
		7	6	5	4	3	2	1	0
Device Mode:									
NT Mode Adaptive Sampling (*)	NTA	0	0	0	0	0	1	0	0
NT Mode Fixed Sampling	NTF	0	0	0	0	0	1	0	1
TE Slave Mode (slave-slave)	TES	0	0	0	0	0	1	1	0
Monitoring Mode Activation	MMA	0	0	0	1	1	1	1	1
TE Master Mode	TEM	0	0	0	0	0	1	1	1
B Channel Configuration:									
B Channel Mapped Direct (*)	BDIR	0	0	0	0	1	1	0	0
B Channel Exchanged	BEX	0	0	0	0	1	1	0	1
B1 Channel Enabled (*)	B1E	0	0	0	1	0	1	0	0
B1 Channel Disabled	B1D	0	0	0	1	0	1	0	1
B2 Channel Enabled (*)	B2E	0	0	0	1	0	1	1	0
B2 Channel Disabled	B2D	0	0	0	1	0	1	1	1
End of Messages Indication:									
EOM Indication Enabled (*)	EIE	0	0	0	1	0	0	0	1
EOM Indication Disabled	EID	0	0	0	1	0	0	0	0
Multiframe Processing:									
Multiframe Disabled (*)	MID	0	0	0	1	0	0	1	1
Multiframe Enabled	MIE	0	0	0	1	0	0	1	0
Disable Three Time Checking	DIS3X	0	0	1	0	1	0	0	1
Enable Three Time Checking (*)	EN3X	0	0	1	0	1	0	0	0
Write Multiframe Message	MFT	0	0	1	1	M1	M2	M3	M4
Loopback Test Mode:									
Clear All loopbacks (*)	CAL	0	0	0	1	1	0	1	1
Loopback B1 on Line Enabled	LB1E	0	0	0	1	1	0	0	0
Loopback B2 on Line Enabled	LB2E	0	0	0	1	1	0	0	1
Loopback 2B+D Enabled (1)	LBS	0	0	0	1	1	0	1	0
Loopback B1 on GCI Enabled	LBB1E	0	0	0	1	1	1	0	0
Loopback B2 on GCI Enabled	LBB2E	0	0	0	1	1	1	0	1

(1) alternate command instruction to ARL (C/I code); but without any status indication pending
(*) initial state following Power on initialization

Table 4: Monitor Status Messages

Functions	Mnemonic	Bit Number							
		7	6	5	4	3	2	1	0
Multiframe Receive Register	MFR	0	0	1	1	M1	M2	M3	M4

Monitor channel code description:
Monitor channel code list is given in table 3 and 4.

Device mode.

NTA : NT mode Adaptive sampling.
In NT mode, adaptive sampling should be selected when the device is an NT equipment connected on any wiring configuration up to the maximum specified length for operation. Multiple Terminals, if required, must be grouped within approximately 50 meters one from each other (depending on cable capacitance as indicated in I.430). Transmit section of SID-GCI is phased locked to GCI FSa source.

NTF : NT mode fixed sampling.
In NT mode, fixed sampling should be selected when the device is in a NT equipment connected on a passive bus wiring configuration up to approximately 200 meters in length depending on cable type. In this mode the receiver DPLL is disabled and sampling of the received symbols is fixed to enable multiple Terminals (nominally up to 8) to be connected anywhere along the passive bus. Transmit and Receive section is phased locked to GCI FSa source.

TES : TE mode connected on the T interface.
This mode should be selected when the device is used on the T interface side of an NT2 equipment. I.430 circuitry operates as in TE mode but GCI interface is driven by BCLK and FSa sources providing a slave-slave configuration.

Data buffers and a clock resynchronizer enable

the GCI to function with FSa and BCLK jittering sources. No phase relationship is needed between the line recovered clocks and GCI.

A 1536kHz clock signal output phased locked to the Recevied line signal is delivered on CLK.

CLK output signal is generated only when ST5421 if fully activated (state F7) and no clock signal is detected on that pin by the device during his own selected GCI channel.
Otherwise CLK output remains high impedance.

Note: CLK output is activated immediately on the first bit of the B2 channel (GCI side) and is deactivated immediately if SID-GCI leaves F7 state.

D channel access Control circuitry is disabled. i.e. D channel data at Bx input is continuously transmitted to the line; there is no monitoring of the D echo channel from the network direction.

MMA : Monitoring mode activation.
When ST5421 is configured in TE mode by means of pins M0, M1, the MMA instruction allows to receive and activate on INFO3 frames, while remaining the master of GCI. That configuration can be used for applications such as monitoring the outputs of TEs on a passive bus.
The received 2B+D can then be passively monitored (the line transmit LO+,LO- would not be connected).

TEM : TE Master Mode.
When ST5421 is in TE configuration by means of pins M0, M1, and in the Monitoring Mode Activation by means of the instruction MMA, the TEM instruction set back SID-GCI in the normal TE Master mode.

B channels configuration.

BDIR/BEX B1E/B1D B2E/B2D
BDIR and BEX instructions provide for the exchange of data between the B1 and B2 channels.
(Note: when enabling a B channel in conjuction with the BEX command, channels is referenced at the CGI).
When either or both B channels are disabled by means of the B1D or B2D instruction, binary 1 are transmitted on the line regardless of Bx input while Br output is in high impedance state. When enabled by means of B1E and B2E instructions, B channel are transparently transmitted.

End of message indication.

EID/EIE
C/I channel End Of Message code sending can be enabled with instruction EIE and disabled by means of EID.

Multiframe processing.

MFT/MFR/MIE/MID
In the Transmit direction, with the device in TEM or TES mode, data entered in bit positions M1, M2, M3 and M4 of instruction MFT is transmitted to the NT in multiframe bit positions Q1, Q2, Q3 and Q4 respectively. With the device in NT mode, data entered in the M bit positions is transmitted to the TE in multiframe bit positions S11, S12, S13 and S14 respectively. In the Receive direction, when the Multiframe receive data buffer requires servicing, the MFR (see table 4) status message is autonomously sent with M1, M2, M3 and M4 bits representing Q1, Q2, Q3 and Q4 or S11, S12, S13 and S14 bits received from the multiframe respectively.

Multiframe Structure and transmission protocol on the line comply with the ANSI US Standard T1.605.1989. "Basic Access Interface for S and T Reference points - Layer 1 specification".

Multiframe message exchange can be supported by SID-GCI when the line is synchronized : states F6 & F7 in TEM or TES modes and state G3 in NT modes.

The multiframe channel processing must be enabled by an MIE instruction to use these channels.

DIS3X/EN3X
When EN3X is set, a new Multiframe message received from the line is checked and transferred on the M channel when received three times identical.
When DIS3X is set, Multiframe messages are transferred tranparently every superframe.

Loopback test modes

CAL/LBS/LB1E/LB2E/LBB1E/LBB2E
LB1E and LB2E instructions turn each individual B channel from the line receive input back to the line transmit output. They may be set separately or together.
LBB1E and LBB2E instructions turn each individual B channel from GCI input to the GCI output. They may be set separately or together.
CAL instruction clears both loopbacks.
It is not allowed to set or clear a LB1, LB2, LBB1 or LBB2 loopback while a complete loopback is set by means of the C/I instruction ARL. LBS can be used as an alternate command to ARL.

Activation/Deactivation

In NT configuration :

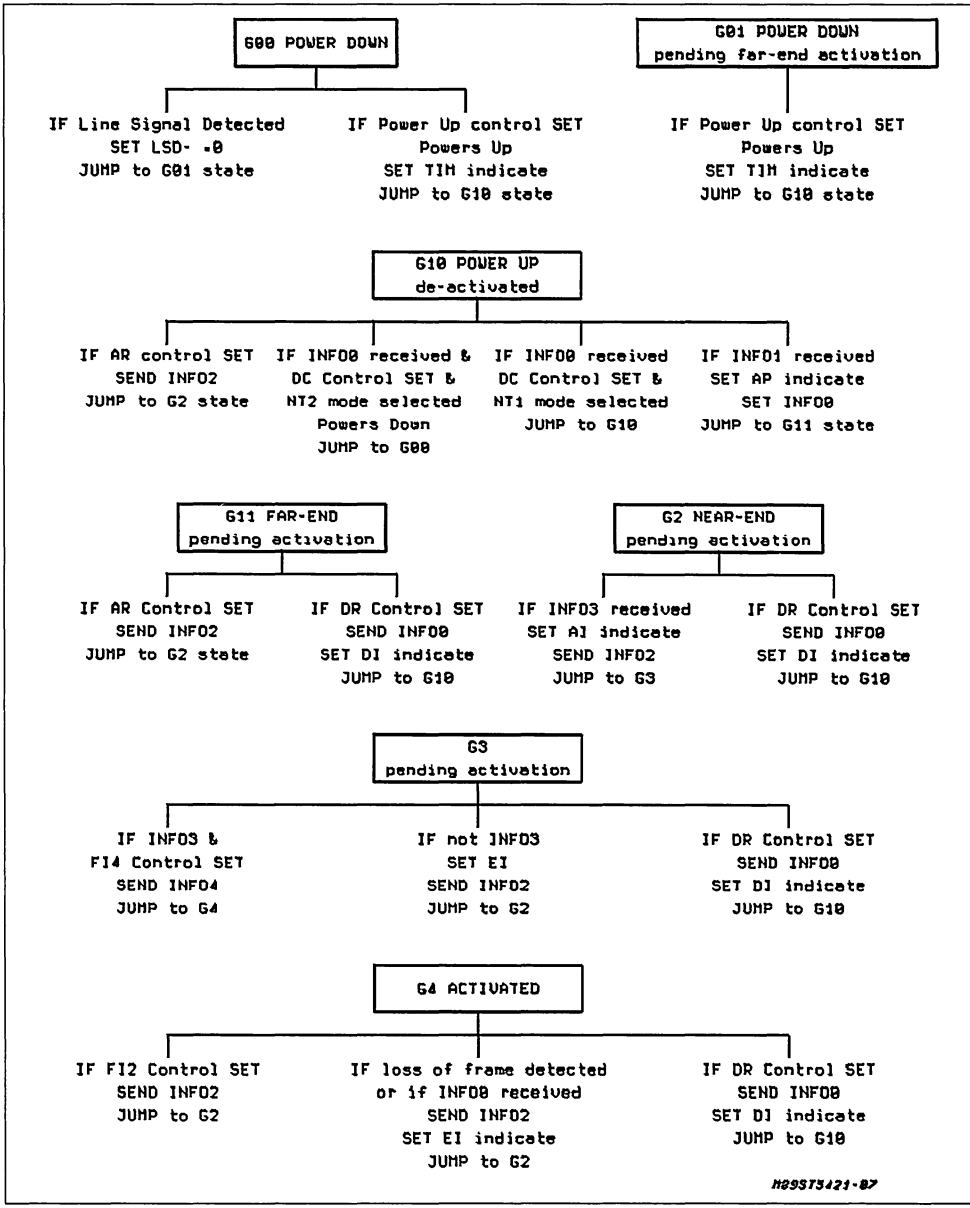
After Power on initialization, ST5421 can be con-

figured in NT1 or NT2 mode, by means of pins and register programming. In NT1, SID-GCI is powered up directly by receiving the GCI clocks on BCLK and FSa inputs. In NT2 mode, the device is powered up by means of PUP code on the C/I Control channel.

Activation may be initiated from either end of the loop.

To operate an activation from the Network, ST5421 must be first powered up by the appropriate procedure followed at least 2ms later by an AR instruction on the C/I channel. Network timing,

Figure 5: Activation Procedure in GCI mode, NT Selected.



FSa, BCLK and MCLK must be present at this time. When activation is initiated by the far-end, SID-GCI being in the Power Down state, a Line Signal Detector circuit pulls low LSD- pin, which can be used to wake up the system. A power Up procedure must be then be issued allowing identification of received signal ie, INFO1 or INFO2. The appropriate procedure is then followed according to I.430.

I.430 recommends that 2 Timers should be available in an NT. An Activation Request should be associated with the start of an external Timer 1 if required. Timer 1 should be stopped when the AI indication is generated following successful activation. If Timer 1 expires before AI is generated, however, Control instruction DR should be written to the device to force deactivation. Timer 2 which is specified to prevent unintentional re-activation, is not required since ST5421 can uniquely recognize INFO1 frames.
Two extra codes are needed for NT1 application: FI4 indicates to the SID-GCI that the U line is activated and allows completion of activation by sending INFO4. FI2 indicates to SID-GCI that the U line has lost synchronization and requests sending of INFO2.

In TEM or TES configuration :
After Power on initialization, ST5421 can be configured in TE or TES power down mode, depending on pins and register configuration setting. In TEM mode, SID-GCI is powered up by pulling low the Bx input. SID-GCI reacts by sending GCI free-running clocks. In TES mode, the SID-GCI is powered up by means of the PUP code on the C/I Control channel.

Activation may be initiated from either end of the loop. To operate an activation from the Terminal, the device must be first powered up by the appropriate procedure followed at least 2ms later by an AR instruction on the C/I channel. When activation is initiated by the far-end, SID-GCI being in the Power Down state, a Line Signal Detector Circuit pulls low the LSD- pin, which can be used to wake up the system. A Power Up procedure must then be issued allowing identification of received signal ie, INFO2. The appropriate procedure is then followed according to I.430.

Figure 6: Activation Procedure in GCI mode, TE Selected

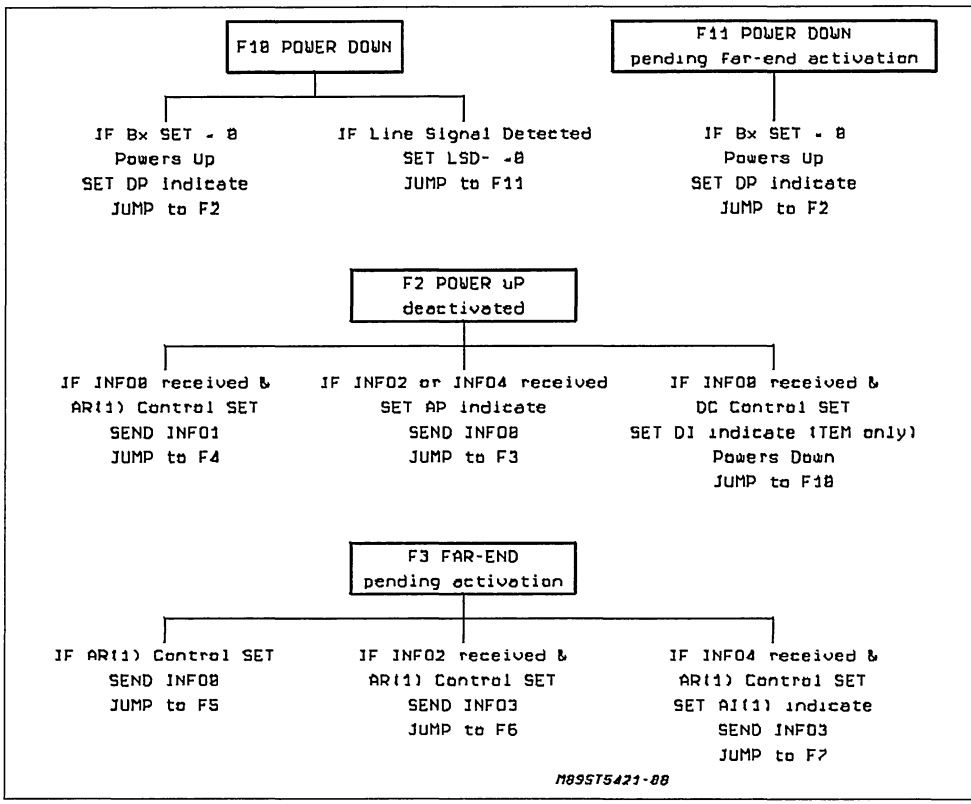
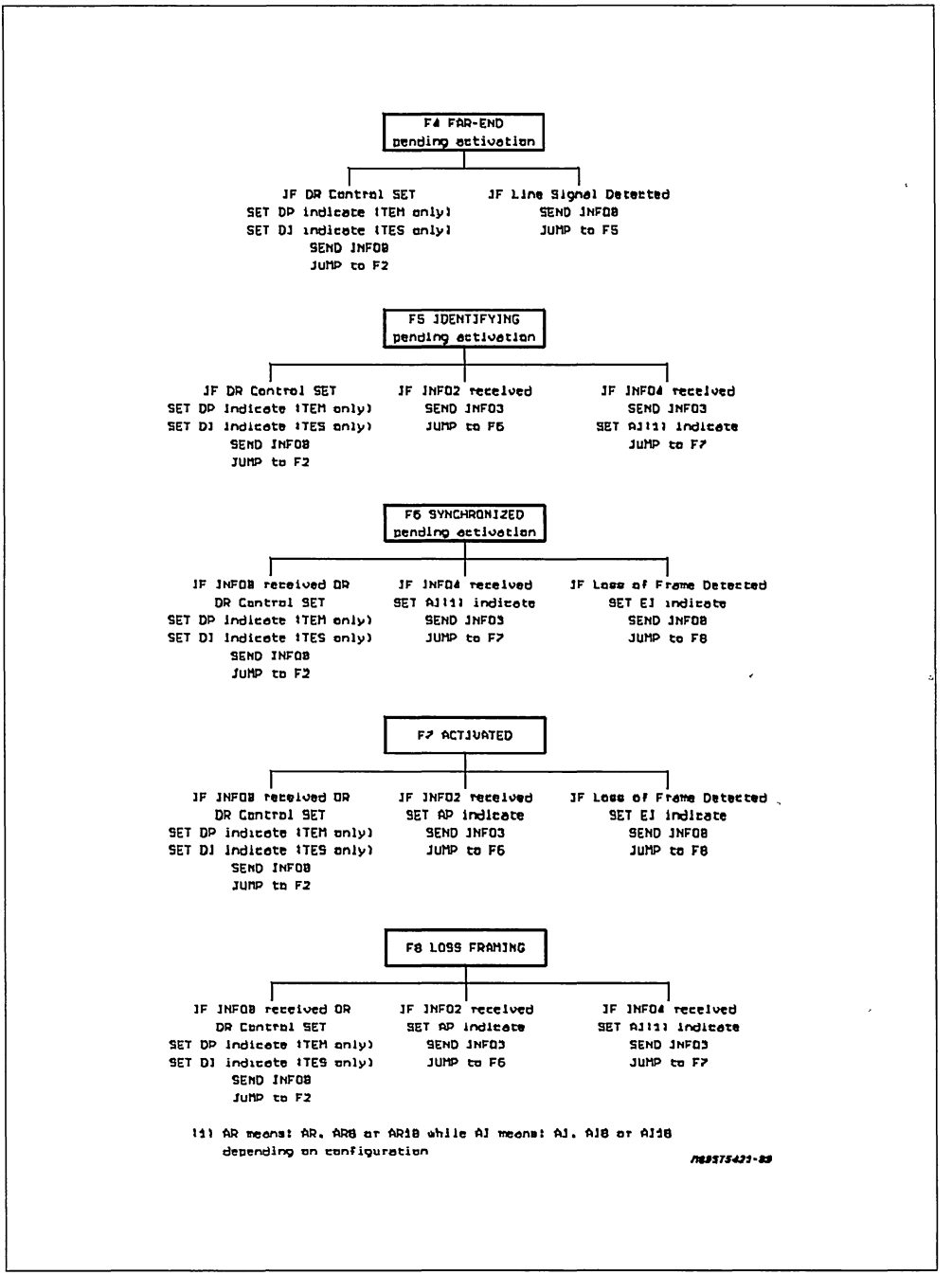


Figure 6: Continued



I.430 recommends that a Timer should be available in a TE. An Activation Request to the SID-GCI should be associated with the start of an external Timer 3 if required.Timer 3 should be stopped when the AI indication is generated following successful activation. Timer 3 expires before AI, AI8 or AI10 is generated, however, Control instruction DR should be written to the device to force de-activation.

D CHANNEL ACCESS IN TEM MODE

A controller device requiring to start transmission of a packet on the line should first prepare the complete message such that the opening Flag is ready to be shifted accross GCI. A Control Instruction AR8 or AR10 will initiate first the Activation Sequence on the line until activation has been completed and then the D channel access sequence according to Priority Class 1 (signalling) or Priority Class 2 (Data packet) respectively.

After line activation, AI8 (or AI10) indication is sent from SID-GCI. Then, DEN output immediately enables to prefetch the opening flag from the controller device into the SID-GCI D channel buffer. Meanwhile, the Priority Counter checks that no other TE connected to the S interface is transmitting in the D channel. This is assured by counting consecutive "1"s in the E bit position of frames received from the NT and comparing the value with the current priority level as specified by I.430. If another TE is active in the D channel, DEN pulses are inhibited once the Opening Flag is in the Transmit buffer to prevent further fetching of Transmit data from the Controller until D channel access is achieved.

As soon as the required number of consecutive E bit "1"s has been counted, the leading 0 of the opening flag is transmitted in the next D bit position to the NT. Then, DEN pulses are re-enabled in order to get new D channel bits. No other instructions are necessary for local flow control between controller and ST5421.

During transmission in the D channel, SID-GCI continues to compare each E bit with the D bit previously transmitted before proceeding to send the next. In case of mis-match, a contention for the previous D bit is assumed to have been won by another TE. Transmission of the current packet therefore ceases and "1"s are transmitted in all following D bit positions. Status indication CON is sent to the controller on C/I channel. DEN output pulses are again inhibited, and D channel access sequence is disabled.

In order to retransmit the lost frame, the controller must begin as before sending a new AR8 (or AR10) ; it has to change first the code sent (ie DI) and after change again to AR8. Successful sending of a transmit frame is detected when the closing Flag is transmitted in the D channel. "1"s are then transmitted in the following D bit positions.

If enabled by the Control Instruction EIE, indication EOM is sent to indicate the End of message.

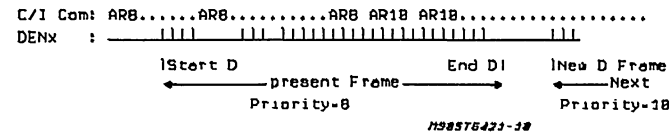
After sending of a transmit frame successfull, SID GCI will automatically perform a new D access sequence if it's still receiving AR8 or AR10 command on C/I channel, otherwise no D access sequence will be done until reception of AR8 or AR10 command.

Any indication change on the C/I channel except EOM indicates deactivation of the D channel access sequence and a new AR8 (or AR10) is needed to restart the procedure.

Note: Users willing to control the D channel access, can use this procedure:
Send AR8 or AR10 until receiving DENx, then remove ARx command code and replace it by an another command (ie DI that is equivalent to a NOP operation if the device is full_activated). At the end of a D frame EOM Indication is received (if EIE is set); when a new D message is prepared an ask for a new D channel access by AR8 or AR10 can be sent.

Users that want to discriminate consecutive D channel access with EOM Indication, are suggested to remove EOM Indication, between 2 D frames, to be able to separate the 2 messages EOM: With the following method: send AR8 (AR10) continuously, until receiving EOM Indication, then send ONCE AR8~ [0111] (AR10~ [0110]) on C/I channel and continue to send the previous code AR8 (AR10); this AR8~ (AR10~) is a kind of EOM aknowledge: the device detect a 'new' primitive AR8 (AR10), stop EOM Indication and replace it by AI8 or AI10 if ST5421 is still full activated.

For application with automatic D channel access and wanting to change the priority class (8 or 10) for D channel, they can use the following procedure:
Assuming that the present D frame is priority class 8 and that the next D frame will be priority class 10, users can change AR8 code to AR10 as soon as they are sure that the present D frame is started, by controlling DENx, anticipating the next D messages before the closing flag of the present D frame. When the automatic D channel access will be performed for next D message, the D channel request will be done with the desired priority class. (see figure below).



MULTIFRAME MAINTENANCE CHANNELS (S1 AND Q WORDS)

Each direction of transmission across the S interface includes a low-speed (800 b/s) channel for loop maintenance accessed via the monitor channel of ST5421. A multiframe structure, consisting of 20 frames on the S interface, is used to synchronize these channels and convey messages coded into 4-bit words, see Table 5. One word is transmitted downstream (NT-to-TE) in the S1 channel, and one word is transmitted upstream (TE-to-NT) in the Q channel every multiframe.

When the device is in NT mode, the MIE command enables both the transmission of the multiframe identification algorithm (reversal of the FA/N bits every 5th frame and M bit set = 1 every 20th frame) and enables the MFR message. The algorithm is present during INFO2 and INFO4 frames. In TE modes this command only enables the MFR message since the device will always search for and synchronize to the multiframing identification bits if NT is sending them. In all modes, at the end of each multiframe the received 4-bit word is decoded to determine if it should generate an MFR interrupt immediately, or be stored until 3 consecutive multiframes have contained the same 4-bit word before a MFR message is generated. Table 5 lists the codes which are 3-times checked. Note, however, that no other action is taken by the ST5421 in response to received codes (e.g. loop-backs are not automotically implemented); the external controller must take the necessary action. This provides the freedom to implement maintenance functions without constrains from the device, and to utilise the unassigned codes for other functions.
It is possible to disable the checking algorithm by setting DIS3X instruction on M channel. There, Multiframe words are transferred transparently on M channel.

The MID command disables the transmission of the Multiframe identification algorithm in NT mode and disables the MFR message in both NT and TE modes. Both the MIE and MID commands can only be written to the device when it is deactivated (either powered-up or powered-down). The Multiframe Transmit Register should also be loaded with the appropriate "idle" messages, by means of an MFT instruction, prior to activation.

Table 5: Codes for Q and S1 channel messages

Message (1)	NT to TE					TE to NT				
	Received at TE				Number of Repetitions Before MFR message (EN3X set)	Received at NT				Number of Repetitions Before MFR message (EN3X set)
	S11	S12	S13	S14		Q1	Q2	Q3	Q4	
Idle (Normal)	0	0	0	0	3	1	1	1	1	3
Loss-of-Power Indication	1	1	1	1	1	0	0	0	0	1
STP Pass	0	0	1	0	3	--	--	--	--	--
STF Fail	0	0	0	1	3	--	--	--	--	--
ST Request (3)	--	--	--	--	--	0	0	0	1	3
STI Indication	0	1	1	1	3	--	--	--	--	--
DTSE-IN	1	0	0	0	1	--	--	--	--	--
DTSE-OUT	0	1	0	0	1	--	--	--	--	--
DTSE-IN & OUT	1	1	0	0	1	--	--	--	--	--
LB1 Request	--	--	--	--	--	0	1	1	1	3
LB1/Indication	1	1	0	1	3	--	--	--	--	--
LB2 Request	--	--	--	--	--	1	0	1	1	3
LB2/Indication	1	0	1	1	3	--	--	--	--	--
LB1/2Request (2)	--	--	--	--	--	0	0	1	1	3
LB1/2Indication	1	0	0	1	3	--	--	--	--	--
Loss-of-Received Signal Indication	1	0	1	0	3	--	--	--	--	--
Unassigned	All other codes				1	All other codes				1

Notes:
(1) No autonomous action is taken by ST5421 in response to received messages. Where appropriate, the external controller must respond with a command or other action.
(2) The code "0011" will be received by an NT1 when the LB1 and LB2 requests are transmitted by two different TEs (NT2s) on a Passive Bus.
(3) The code "0001" will be received by an NT1 when ST Request and any other code (except LP) is sent simultaneously by two or more TEs on a Passive Bus.

Figure 7: ISDN Telephone Set Application (non isolated)

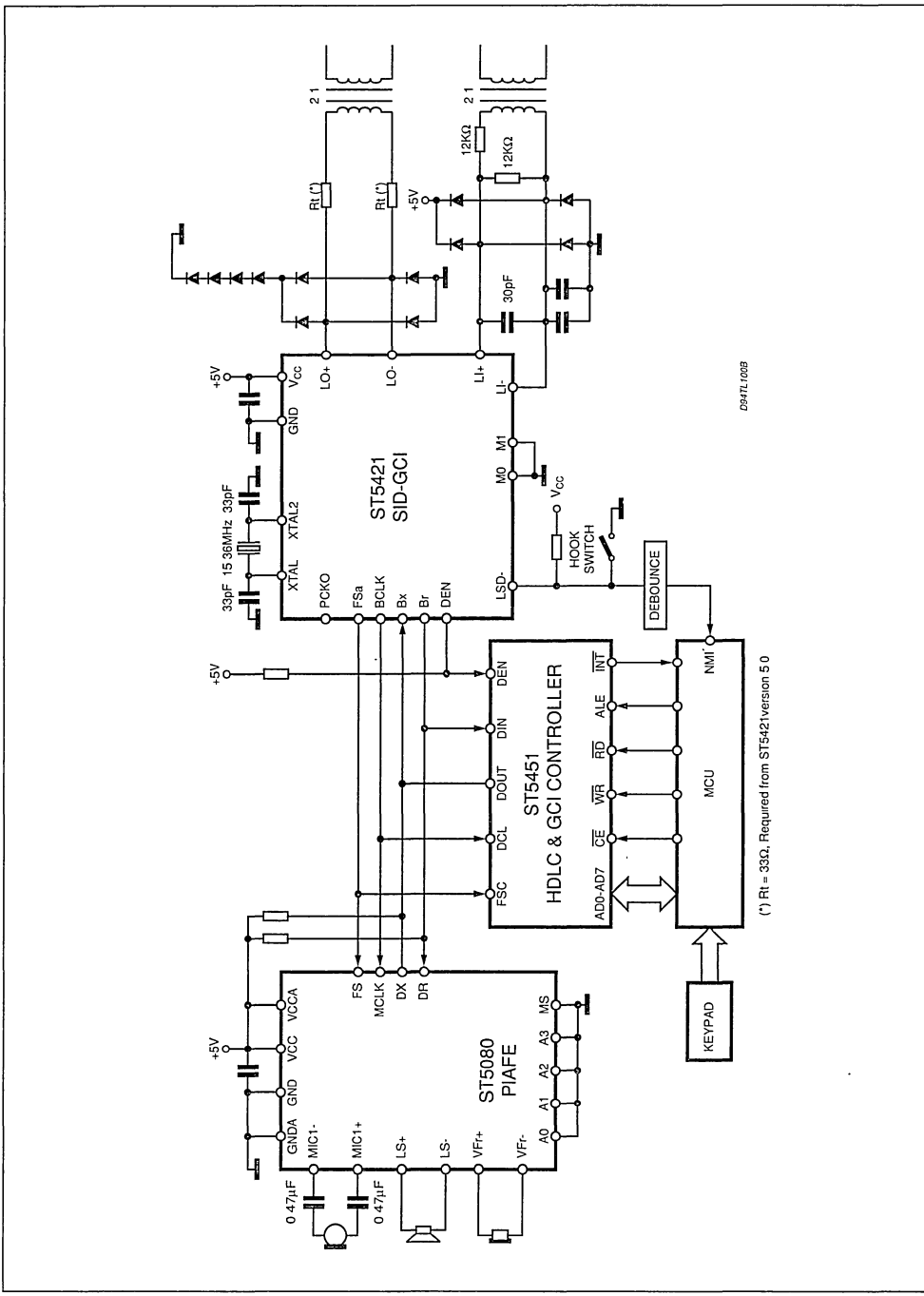
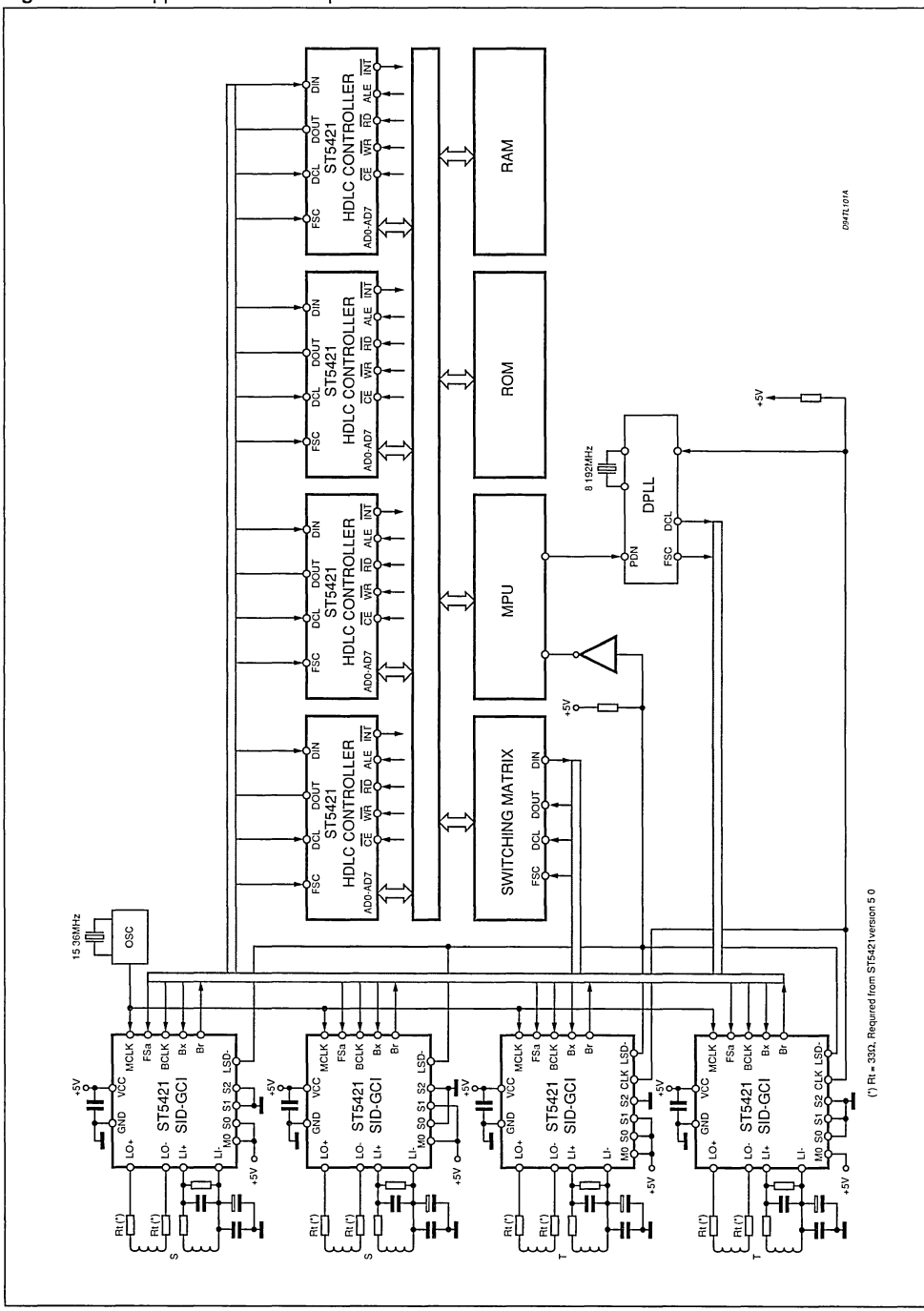


Figure 8: NT2 Application GCI Compatible



ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
V_{CC} to GND	7	V
Voltage at Bx, Br	V_{CC} + 1 to GND - 1	V
Voltage at any Digital Input (except Bx)	V_{CC} + 1 to GND - 1	V
Current at any Digital Input (except Br)	± 50	mA
Current at Lo	± 100	mA
Storage Temperature Range	-65 to +150	°C
Lead Temperature (soldering 10s)	300	°C

ELECTRICAL CHARACTERISTICS (unless specified otherwise: V_{CC} = 5V ±5%, T_A = 0 °C to 70°C; typical characteristics are specified at V_{CC} = 5V, T_A = 25°C. All signals are referenced to GND).

DIGITAL INTERFACE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	All Digital Inputs			0.8	V
V_{IH}	Input High Voltage	All Digital Inputs	2.2			V
V_{ILX}	Input Low Voltage	MCLK/XTAL input			0.5	V
V_{IHX}	Input High Voltage	MCLK/XTAL input	V_{CC}-0.5			V
V_{OL}	Output Low Voltage	Br: I_L = 3.2 mA All other Digital Outputs: I_L = ±1mA			0.4	V
V_{OH}	Output High Voltage	Br: I_L = 3.2 mA All other Digital Outputs: I_L = ±1mA	2.4 2.4			V V
I_{IL}	Input Low Current	Any Digital Input, GND < VIN < V_{IL}	-10		+10	µA
I_{IH}	Input High Current	Any Digital Input, VIH < V_{IN} < V_{CC}	-10		+10	µA
I_{OZ}	Output Current in HIGH Impedance (tri-state)	All Digital Tri-state I/Os	-10		+10	µA

LINE INTERFACE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
R_{LI}	Differential Input Resistance	GND < LI_+, LI- < V_{CC}	200			kΩ
C_{LLO}	Load Capacitance	From LO+ to LO-			200	pF
	Transmit Pullse Amplitude	R1 = 212Ω between LO+ and LO- (1)	1.484	1.585	1.696	Vpk
	Transmite Pulse Unbalance	O+ relative to O-			5	%
	Input Amplitude	Differential Between LI+ and LI-	±175			mV
V_{OS}	Differential Offset Voltage at L_{O+}, L_{O-}	Driving Binary 1s, 220Ω between LO+ and LO-	-20		20	mV

POWER DISSIPATION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{cc0}	Power Down Current	All Outputs Open-circuit			900	µA
I_{ccnt}	Active Current (2)	NT/TES not transmitting		12	13	mA
I_{ccntt}	Active Current (3)	NT/TES transmitting			21	mA
I_{ccte}	Active Current (2)	TEM not transmitting		17	18	mA
I_{cctet}	Active Current (3)	TEM transmitting			26	mA

(1) This specification garanties compliance with CCITT1430 recommendation concerning the pulse templates. Winding resistors for the transformer is assumed to be represented by an extra 12Ω load added to the 200Ω corresponding to the 50Ω load reflected back through the 1.2 transformer.

(2) Measured with an external 15.36MHz clock applied on pin XTAL1, XTAL2 being left unconnected.

(3) Same condition as in (2) assuming worst case line current on 50Ω.

ELECTRICAL CHARACTERISTICS (continued)

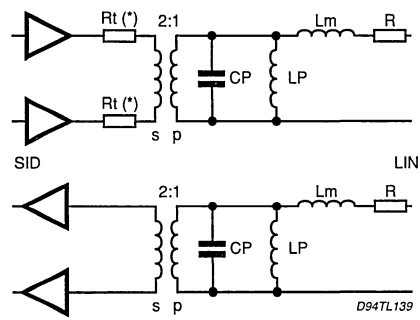
MASTERCLOCK

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	MCLK Frequency			15.36		MHz
	MCLK Frequency Tolerance		-100		100	ppm
	MCLK Input Clock Jitter				50	ns pk-pk
	Timing Recovery Jitter	BCLK Output Relative to MCLK at TE	-130		130	ns
t_{MH}, t_{ML}	Clock Pulse width High and Low of MCLK	$V_{IH} = V_{CC}$-0.5V, V_{IL} = 0.5V	20			ns
t_{MR}, t_{MF}	Rise Time and Fall Time of MCLK	Used as a logical input			10	ns

TRANSFORMER MODEL (all values are to be measured at 10kHz)

		Min.	Typ.	Max.	Unit
1:N	Primary to Secondary Turn Ratio	1.98	2	2.02	%
Rp	Primary Winding Resistance		2		W
Rs	Secondary Winding Resistance		4		Ω
R	Primary Total Resistance		3		Ω
Lp	Primary Inductance	22	30	37.5	mH
Lm	Primary Inductance with Secondary Shorted		16	20	mH
Cp	Primary Capacitance with Secondary Open			25	pF

Figure 9: Transmit & Receive Transformer Model

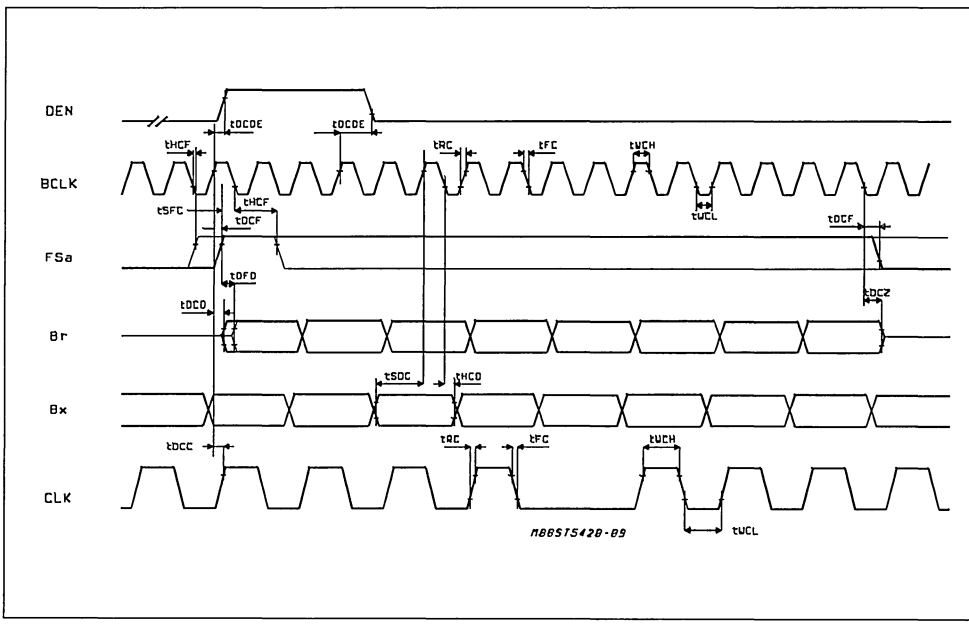


(*) Rt = 33Ω, Required from ST5421version 5.0

TIMING SPECIFICATIONS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{DCDE}	Delay Time BCLK High to DEN Transition	TE Mode only			30	ns
t_{HCF}	Hold Time BCLK Trans. to FSa Transition		0			ns
t_{RC}, t_{FC}	Rise & Fall Time BCLK				15	ns
t_{WCH}, t_{WCL}	BCLK width High & Low		60			ns
t_{SFC}	Setup Time FSa High to BCLK Low		70		BCLK -50	ns
t_{DCF}	Delay Time BCLK High to FSa HIGH	TE Mode only			30	ns
t_{DCD}	Delay Time BCLK High to DATA Valid		20		80	ns
t_{DFD}	Delay Time FSa High to Data Valid	Load 100pF. Apply only if FSa rises later than BCLK rising edge			80	ns
t_{DCZ}	Delay Time BCLK Low Data Invalid		50		120	ns
t_{SDC}	Setup Time Data Valid to BCLK Low		30			ns
t_{HDC}	Hold Time BCLK Low to Data Invalid		20			ns
t_{DCC}	Delay Time BCLK High to CLK High	TE and TES side modes only	0		30	ns

Figure 10: GCI Mode



APPLICATIONS INFORMATION

While the pins of ST5421 SID-GCI device are well protected against electrical misuse, it is recommended that the standard CMOS practise of applying GND to the device before any other connections, should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used.

To minimize noise sources, all ground connections to each device should meet at a common point as close as possible to the GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. A power supply decoupling capacitor of 0.15F should be connected from this common point to V_{CC} as close as possible to the device pins.

CRYSTAL OSCILLATOR

The clock source for ST5421 may be provided with a commercially available crystal or an external clock source meeting the frequency requirements as explained in the following sections.

CRYSTAL SPECIFICATION

ST5421 SID-GCI clock source may be either a quartz crystal operating in parallel mode or an external signal source at 15.36MHz. The complete oscillator (crystal plus the oscillator circuit) must meet a frequency tolerance specification of ±50ppm total to comply with the CCITT I.430 specification for TE applications.The frequency tolerance limits span the conditions of full operating temeprature range (commercial or industrial) and effects due to aging and part parameter variations.

The crystal is connected between pin 5 (MCLK/XTAL) and pin 6 (XTAL2), with a 33pF total capacitance from each pin to ground. The external capacitors must be mica or high-Q ceramic type. The use of NPO (Negative Positive Zero coefficient) capacitors is highly recommended to ensure tight tolerance over the operating temperature range. The 33pF capacitance includes the external capacitor plus any trace and lead capacitance on the board. Nominal frequency of 15.360MHz, frequency tolerance (accuracy, temperature and aging) less than 1.60ppm, with Rs = 150, CL= 20pF, parallel mode, C0 (shunt capacitance) 7pF.An external circuit may be driven directly from the pin XTAL2 (pin 6) provided that the load presented is greater than 50K shunted by a total of 33pF of capacitance. Crystal oscillator board layout is critical and should be designed with short traces that do not run parallel when in close proximity (to minimize coupling between adjacent pins). On multi-layered boards a ground layer should be used to prevent coupling from signals on adjacent board layers. Ground traces on either side of the high frequency trace also helps isolate the noise pickup.

EXTERNAL OSCILLATOR CONFIGURATION

An external 5V drive clock sourcxed may be connected to the MCLK (pin 5) input pin of ST5421. The nominal frequency should be 15.36MHz with a tolerance of 1 80ppm. The ST5421 SID provides a load of about 7pF at the MCLK input pin.

LINE TRANSFORMER REQUIREMENTS

The electrical characteristics of the pulse transformer for the ISDN "S" interface are defined to meet the output and input signal and the line isolation and characteristics as defined in CCITT reccommednation I.430. The transformer provides isolation for the line card or terminal from the line it lasi provides a means to transfer power to the terminalb over the S-loop via the "phantom" circuit created by center-tapping the line side windings. A transformer is used both at the transmit and the receive end of the loop. These notes specify the tolerances of a transformer that is employed with ST5421 to meet the CCITT recommendation on output pulse mask and impedance requirements.

LINE TRANSFORMER RATIO

The transmit and th receive transformers can be the same (with a winding ratio of 1:2) or optionally, the receive transformer could have a transformer ratio of 1:1. The primary of the transformer is connected to the S loop while the secondary is connected to the device.

EXTERNAL PROTECTION CIRCUITRY

Precautions are to be taken to ensure that ST5421 SID-GCI is protected against electrical surges and other interferences due to electromagnetic fields, power line faults and lightening discharge that may occur in the transmission medium. Protection circuits that are external to the device are recommended on both the primary and secondary sides of the line transformer.

DC BIAS CAPACITORS FOR ANALOG REFERENCE

Two decoupling capacitors (0.1µF mica) and 10µF (electrolytic) are connected between pin 19 of the device and its ground connection. These capacitors decouple the midpoint of a two-resistor potential divider (inside the device) and provide an internally buffered reference for the analog circuitry.

ST5421 EXCEEDING I.430 TRANSMISSION REQUIREMENTS

This ST5421 is designed with the goal of substantially exceeding the transmission performance requirements as specified in the I.430. This is made possible in the ST5421 SID design by employing superior analog front end designs. For example, in the receive path, an analog prefiter removes <200kHz noise signals, which is then followed by an adaptive line equalizer to accomodate varying line conditions with superior performance. A continuously tracking adaptive threshold circuit provides the slicing levels for the detection circuits for correct interpretation of transmission bits even on long lossy loops. This implementation results in longer ranges of S interface cables compared to I.430 requirements.

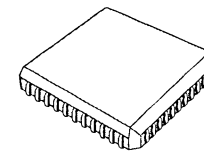
SGS-THOMSON MICROELECTRONICS

L3000N STLC3040

THIRD GENERATION SUBSCRIBER LINE INTERFACE

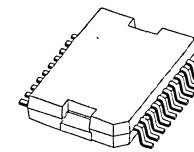
PRODUCT PREVIEW

- TWO CHIP SET + OVERVOLTAGE PROTECTION PROVIDE THE COMPLETE BORSCHT FUNCTIONS.
- PROGRAMMABLE DC FEEDING RESISTANCE AND CURRENT LIMITING 0 TO 70mA (1.1mA STEPS).
- PROGRAMMABLE VOLTAGE DROP ACCORDING TO TTX/ON HOOK TRANSMISSION NEEDS.
- INTEGRATED RING GENERATOR WITH ZERO CROSSING AND PROGRAMMABLE FREQ/LEVEL.
- SUPPORT NORMAL LOOP START LINES, GROUND START PABX LINES, EXTENDED LOOPS AND PAY-PHONES.
- GENERATION, SHAPING AND FILTERING OF 12KHz/16kHz PROGRAMMABLE LEVELS TELETAX METERING SIGNALS.
- REVERSE POLARITY HARD OR SOFT SWITCHING.
- SIGNALLING FUNCTIONS HOOK, GDKEY WITH PROGRAMMABLE PERSISTANCE CHECK.
- ON HOOK TRANSMISSION CAPABILITY.
- CCITT AND LSSGR CODEC/FILTER STD. A/μ LAW.
- 2 WIRE IMPEDANCE SYNTHESIS SOFTWARE PROGRAMMABLE.
- HYBRID FUNCTION SOFTWARE PROGRAMMABLE.
- PROGRAMMABLE GAIN CONTROL AND FREQUENCY RESPONSE CORRECTION.
- SUPERVISION AND TEST OF LINE CONDITIONS, LEAKAGE, CAPACITANCE AND CIRCUIT SIGNALLING TEST FOR TTX AND RINGING.
- TEST TONE GENERATION FOR CIRCUIT TEST, LOOPBACKS POSSIBILITY.
- GCI COMPATIBLE CONTROL INTERFACE.
- SELECTABLE 2/4MHZ BACKPLANE CLOCK.
- MINIMUM EXTERNAL COMPONENTS COUNT.
- ADVANCED 12V BJT-5V CMOS 0.8μmTECHNOLOGY GUARANTEES RELIABILITY AND LOW POWER CONSUMPTION (50MW TOTAL IN ON-HOOK CONDITION).
- INTEGRATED THERMAL PROTECTION WITH THERMAL OVERLOAD INDICATION.



PLCC44

ORDERING NUMBER: STLC3040



PowerSO-20

ORDERING NUMBER: L3000NSO

DESCRIPTION

The subscriber line interface kit (L3000N/STLC3040) is a set of solid state devices designed to integrate all the classical BORSCHT functions (overvoltage protection external) and several additional features needed to interface a telephone line.

The L3000N device is fabricated in B140II (140V Bipolar) technology and is basically an analog front end that drives the line via two output buffers properly amplifying signal applied at its input by the STLC3040. At the same time it provides back to the STLC3040 an accurate image of the loop current.

The STLC3040 device is fabricated in BiCMOS (12V bipolar / 5V CMOS) technology. This device interfaces the L3000N via a dedicated interface and the C.O. backplane via a GCI compatible interface.

The STLC3040 processes the line current image provided by the L3000N generating the transmit signal and the proper voltage signal that will be sent back to the L3000N in order to synthetize the desired AC/DC impedances on the 2-wire side.
At the same time also the received signal on the digital side is transferred into the line.

The signal processing inside the STLC3040 is both analog and digital merging the best available analog and digital processing performances of the BiCMOS technology.

The L3000N/STLC3040 kit is fully programmable and needs only 5 ext. resistors (including the two protection resistors) and 3 capacitors. These components are always the same; all the parameters related to different applications are software programmed. Considering the DC characteristic, by proper programming it is possible to select several limiting currents (from 0 to 70mA with 1.1mA steps, different DC feeding resistance (from 0 to 2 x 400Ω with 100Ω steps) and different drop voltages (on-hook transmission, metering pulse injection).

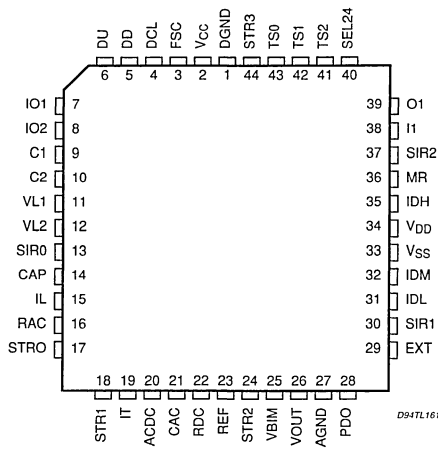
Considering AC performances all possible 2-wire impedances are software programmable, the same for the two to four wire conversion, where all the possible balance impedances can be software programmed. Both Tx and Rx gain are programmable (12 dB range, 0.1dB step) with proper frequency equalization that will guarantee a complete flat response in the speech band.

Ringing signal is also generated on chip with programmable frequency and amplitude. For this purpose the L3000N device in addition to the negative battery (VB-) requires also a positive one (VB+). VB- can vary between -70V to -24V depending on the application. The VB+ is usually selected in order to have a total battery voltage |VB+|+|VB-| = 120V.

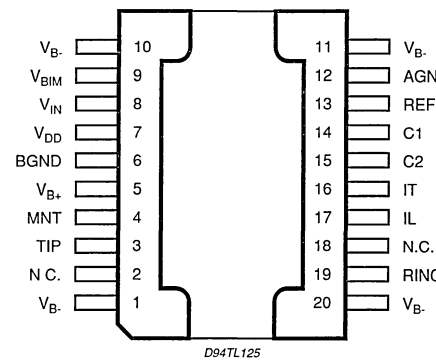
Ring injection and disconnection is always performed in correspondance of zero crossing. In addition when ring trip is detected the ring signal is automatically disconnected again at the first zero crossing. The kit is also able to generate metering pulse signals (12 or 16kHz) with programmable amplitudes up to 5Vrms. Polarity reversal is supported.

Finally several testing features are provided by the kit. This means that the kit is able both to test itself and also the line parameters (leakage, capacitance ..) saving the testing relays and the equipment needed to perform the test.

PIN CONNECTIONS (Top views)



PLCC44



PowerSO-20

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{B-}	Negative Battery Voltage	-80	V
V_{B+}	Positive Battery Voltage	+80	V
$\|V_{B-}\|+\|V_{B+}\|$	Total Battery Voltage	140	V
V_{DD}	Positive Supply Voltage	+5.5	V
V_{SS}	Negative Supply Voltage	-5.5	V
|Vagnd-Vbgnd|	Maximum Voltage Between AGND/BGND	5	V
T_j	Maximum Junction Temperature	150	°C
T_{stg}	Storage Temperature	-55 to +150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
L3000N				
$R_{Th\ j\text{-}case}$	Thermal Resistance Junction to Case	Typ.	2	°C/W
$R_{Th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient	Max.	60	°C/W
STLC3040				
$R_{Th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient	Max.	80	°C/W

OPERATING RANGE (Refer to the test circuit, unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
T_{oper}	Operating Temperature Range		0		70	°C
V_{B-}	Negative Battery Voltage		-70	-48	-24	V
V_{B+}	Positive Battery Voltage		0	72	75	V
$\|V_{B-}\|+\|V_{B+}\|$	Total Battery Voltage			120	130	V
V_{DD}	Positive Supply Voltage		+4.5		+5.5	V
V_{SS}	Negative Supply Voltage		-5.5		-4.5	V
I_{max}	Total Line Current (IL+IT)				85	mA

PIN DESCRIPTION (L3000N)

PowerSO-20 N°	Name	Description
3	TIP	A line termination output with current capability up to 100mA (I_a is the current sourced from this pin).
4	MNT	Positive Supply Voltage Monitor.
5	V_{B+}	Positive Battery Supply Voltage.
6	BGND	Battery ground relative to the V_{B+} and the V_{B-} supply voltages. It is also the reference ground for TIP and RING signals.
7	V_{DD}	Positive Power Supply +5V.
8	V_{IN}	2 wire unbalanced voltage input.
9	VBIM	Output voltage without current capability, with the following functions: - give an image of the total battery voltage scaled by 40 to the low voltage part. - filter by an external capacitor the noise on V_{B+} and V_{B-}.
1,10,11,20	V_{B-}	Negative Battery Supply Voltage.
12	AGND	Analog Ground. All input signals and the V_{DD} supply voltage must be referred to this pin.
13	REF	Voltage reference output with very low temperature coefficient. The connected resistor sets Internal circuit bias current.
14	C1	Digital signal input (3 levels) that defines device status with pin 12. In thermal overload condition a 240mA typical current is sunk by this pin.
15	C2	Digital signal input (3 levels) that defines device status with pin 11.
16	I_T	High precision scaled transversal line current signal. $I_T = \frac{I_a + I_b}{100}$
17	I_L	Scaled longitudinal line current signal. $I_L = \frac{I_a - I_b}{100}$
19	RING	B line termination output with current capability up to 100mA (I_b is the current sunk into this pin).
2, 18	N.C.	Not connected.

Notes: 1) All information relative to the PowerSO-20 package option should be considered as advanced information on a new product now in developement or undergoing evaluation. Details are subject to change without notice.

PIN DESCRIPTION (STLC3040)

PLCC44 N°	Symbol	Type	Description
1	DGND	ID	Digital Ground.
2	V_{CC}	ID	+5V Digital Supply.
3	FSC	ID	Frame sinc. 8KHz GCI Interface.
4	DCL	ID	Master data Clock GCI Interface.
5	DD	ID	Data Down link GCI Interface
6	DU	OD	Data Up link GCI Interface
7,8	IO1,IO2	I/OD	Programmable I/O GCI controlled
9	C1	OD	State control signal 1. Combination of C1 and C2 define L3000N operating mode.
10	C2	OD	State control signal 2.
11,12	VL1,VL2	IA	Comparator inputs. These are inputs of the comparator that senses the line voltage in Loop Open Mode allowing OFF/Hook detection in this mode.
13	SIR0	I/OD	Dedicated, leave open.
14	CAP	I/OA	Reversal. Proper Capacitor should be connected to this pin when soft battery reversal is needed.
15	IL	IA	Longitudinal Line Current input $I_L = \frac{I_a - I_b}{100}$
16	RAC	I/OA	AC Synthesis Reference Resistor.
17,18	STR0,STR1	I/OD	Dedicated, leave open.
19	IT	IA	Transversal Line Current input $I_T = \frac{I_a + I_b}{100}$
20	ACDC	I/OA	AC/DC Line split. Scaled line current output, DC feedback input.
21	CAC	I/OA	Split Capacitor. AC scaled line current input.
22	RDC	I/OA	DC Synthesis Reference Resistor.
23	REF	I/OA	Reference voltage output. A resistor connected to this pin is setting the internal reference current.
24	STR2	I/OD	Dedicated, leave open
25	VBIM	IA	Battery image monitor.
26	VOUT	OA	Two wire unbalanced output feeding the line voltage signals (DC, AC, RING, TTX) scaled by 40.
27	AGND	IA	Analog Ground.
28	PDO	OA	Power Down output. Proper bias current is provided to L3000N by this pin. When the current is 0 the L3000N goes in Power Down (high impedance).
29	EXT	ID	External Ring Sync. Input.
30	SIR1	I/OD	Dedicated, leave open.
31,32	IDL,IDM	IA	Line-card Identification, least valued bit.
33	V_S	IA	-5V Analog Supply.
34	V_{DD}	IA	+5V Analog Supply.
35	IDH	IA	Line-card Id, serial ID signature input.
36	MR	ID	Master reset Input. When connected to VCC the STLC3040 is forced in power down, all internal registers resetted.
37	SIR2	I/OD	Dedicated, leave open.
38	I1	ID	Digital input read via GCI
39	O1	OD	Digital output written via GCI.
40	SEL24	ID	Select Clock Frequency for GCI Interface 2MHz/4MHz, not affecting the data rate.
41,42,43	TS2,TS1,TS0	ID	GCI Select Time Slot Identifier Pins.
44	STR3	I/OD	Dedicated, leave open.

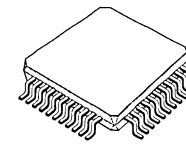
SGS-THOMSON MICROELECTRONICS

STLC5048

PROGRAMMABLE FOUR CHANNEL CODEC AND FILTER

PRODUCT PREVIEW

- PROGRAMMABLE MONOLITHIC 4 CHANNEL CODEC/FILTER
- SINGLE +5V SUPPLY
- PIN STRAP / MCU CONTROL MODE
- A/μ LAW PROGRAMMABLE
- PCM HIGHWAY FORMAT:
  - 1.536 or 1.544 MHz
  - 2.048 MHz, 4.096 MHz
- TX GAIN PROGRAMMING:
  - 15dB RANGE; 0.5dB STEP
- RX GAIN PROGRAMMING: 15dB RANGE; 0.5dB STEP
- PROGRAMMABLE TIME SLOT ASSIGNMENT
- DIGITAL LOOPBACK
- AUXILIARY INPUT MODE (ALLOW DC ENCODING)
- POWER DOWN MODE
- 44 PQFP PACKAGE



PQFP44

ORDERING NUMBER: STLC5048

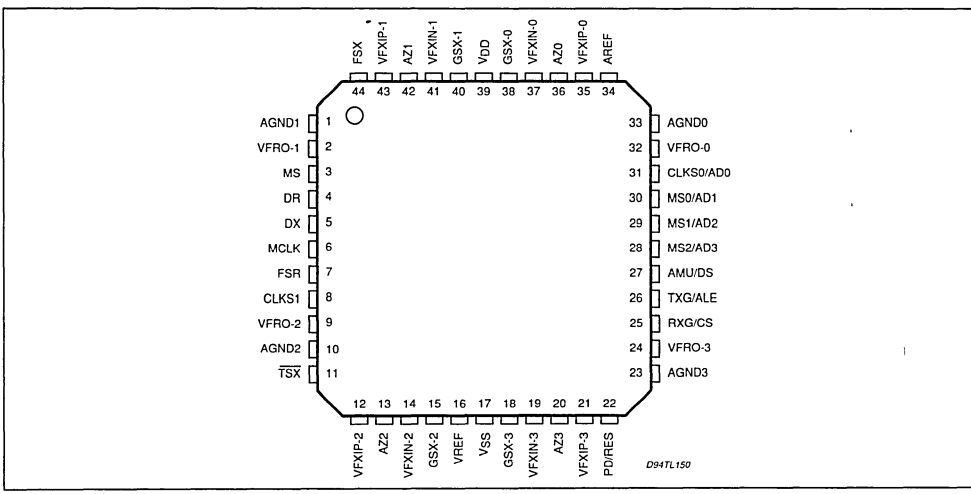
DESCRIPTION

The STLC5048 is a monolithic programmable 4 channel codec and filter. It operates with a single +5V supply. The analog interface is compatible with the first generation codec / filter standard: 600Ω load driving capability on the receive output and operational amplifier input stage. A midsupply reference level of 2.5V is generated by the device and provided to each analog port.

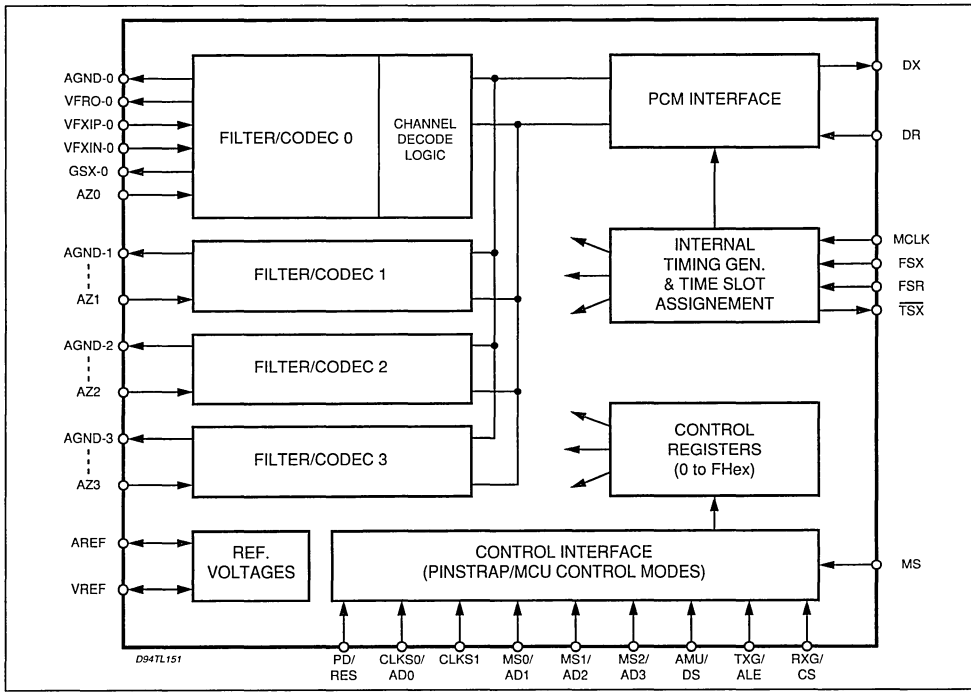
The PCM interface allows the use of independent 8KHz frame sync. pulses for the transmit and receive direction. The MCLK clock can be selected from three standards: 1.563/1.544MHz, 2.048MHz, 4.096MHz.

Device programmability is achieved by means of 16 registers used to set parameters such as TX/RX gains, encoding law (A/μ), time slot assignment, channel enable/disable, TX filter disable, loopback and mute. The pinstrap option is used to set the most significant of these parameters by hw. Connection of the proper pins allow the device to operate without MCU control.

PIN CONNECTION (Top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to V_{SS}	-0.5 to 7	V
V_{IN}	Input Pin Voltage	GND-0.3 to V_{CC}+0.3	V
I_{IN}	Input Pin Current	+/-1	mA
I_{OUT}	Output Pin Current	±10	mA
P_{DISS}	Power dissipation	800	mW
T_{stg}	Storage Temperature Range	-60 to +150	°C
S_{DIS}	Static discharge (100pF; 1.5KΩ) (1)	1000 (Target 2000)	V
T_{LEAD}	Lead Temperature (soldering, 10s)	300	°C

(1): Latch up current will exceed 100mA (Target 200mA).

OPERATING RANGE

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.75 to 5.25	V
T_{OP}	Operating Resistance Junction to Ambient	-40 to +85	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient	75	°C/W

PIN DESCRIPTION

I/O DEFINITION

Type	Definition
AI	Analog Input
AO	Analog Output
AI/O	Analog Input/Output
DI	Digital Input
PS	Chip Power/Ground
DO	Digital Output
OD	Open Drain Output

ANALOG PIN DESCRIPTION

No.	Name	Type	Description
32	VFRO-0	AO	Analog output of the Receive Filter - 0
2	VFRO-1	AO	Analog output of the Receive Filter - 1
9	VFRO-2	AO	Analog output of the Receive Filter - 2
24	VFRO-3	AO	Analog output of the Receive Filter - 3
35	VFXIP-0	AI	Non-inverting input of theTX Input Amplifier - 0
37	VFXIN-0	AI	Inverting input TX Input Amplifier - 0
38	GSX-0	AO	Analog output of the TX Input Amplifier - 0. Used to set gain externally.
43	VFXIP-1	AI	Non-inverting input of theTX Input Amplifier - 1
41	VFXIN-1	AI	Inverting input TX Input Amplifier - 1
40	GSX-1	AO	Analog output of the TX Input Amplifier - 1. Used to set gain externally.
12	VFXIP-2	AI	Non-inverting input of theTX Input Amplifier - 2
14	VFXIN-2	AI	Inverting input TX Input Amplifier - 2
15	GSX-2	AO	Analog output of the TX Input Amplifier - 2. Used to set gain externally.
21	VFXIP-3	AI	Non-inverting input of theTX Input Amplifier - 3
19	VFXIN-3	AI	Inverting input TX Input Amplifier - 3
18	GSX-3	AO	Analog output of the TX Input Amplifier - 3. Used to set gain externally.
36	AZ0	AIO	Auto-Zero pin for Ch. 0, A 0.1uF capacitor should be connected beween this pin and VSS. (1)
42	AZ1	AIO	Auto-Zero pin for Ch. 1, A 0.1uF capacitor should be connected beween this pin and VSS. (1)
13	AZ2	AIO	Auto-Zero pin for Ch. 2, A 0.1uF capacitor should be connected beween this pin and VSS. (1)
20	AZ3	AIO	Auto-Zero pin for Ch. 3, A 0.1uF capacitor should be connected beween this pin and VSS. (1)
34	AREF	AIO	High impedance ground pin (common for all four channels). A 0.1uF capacitor should be connected between this pin and VSS. (1)
33	AGND0	AIO	Low impedance Ground pin for channel 0. It is a 2.5V midsupply level with 10uA current capability. A 0.1uF capacitor should be connected between this pin and VSS.
1	AGND1	AIO	Low impedance Ground pin for channel 1. It is a 2.5V midsupply level with 10uA current capability. A 0.1uF capacitor should be connected between this pin and VSS.
10	AGND2	AIO	Low impedance Ground pin for channel 2. It is a 2.5V midsupply level with 10uA current capability. A 0.1uF capacitor should be connected between this pin and VSS.
23	AGND3	AIO	Low impedance Ground pin for channel 3. It is a 2.5V midsupply level with 10uA current capability. A 0.1uF capacitor should be connected between this pin and VSS.

(1): Low leakage capacitors should be used (I_{leak} < 10nA)

POWER AND REFERENCE PIN DESCRIPTION

No.	Name	Type	Description
17	VSS	PS	Digital ground.
39	VDD	PS	5V Power Supply
16	VREF	AIO	CODEC 4.0V Voltage Reference Output for Decoupling. A 0.1µF capacitor should be connected between this pin and VSS (1)

(1): Low leakage capacitors should be used (I_{leak} < 10nA)

DIGITAL PIN DESCRIPTION

No.	Name	Type	PAD	Description
3	MS	DI	CMOS	Mode Select. 1: MCU control mode. 0: Pin-strap control mode.
14	FSX	DI	TTL	Transmit Frame Sync. Pulse.
7	FSR	DI	TTL	Receive Frame Sync. Pulse.
6	MCLK	DI	TT L	Master Clock Input. Three possible frequencies can be used: 1.536/1.544 MHz; 2.048 MHz; 4.096 MHz. Depending on the MCLK freq. CLKS0 and CLKS1 should be properly set.
11	$\overline{TSX}$	OD		Transmit Time Slot (open drain output, 3.2mA). Normally it is floating in high impedance state except when a time slot is active on the DX output. In this case TSX output pulls low to enable the backplane line driver. Should be strapped to VSS when not used.
5	DX	DO	CMOS/TTL	Transmit PCM interface. It remains in high impedance state except during the assigned time slots during which the PCM data byte is shifted out on the rising edge of MCLK.
4	DR	DI	TTL	Receive PCM interface. It remains inactive except during the assigned receive time slots during which the PCM data byte is shifted in on the falling edge of MCLK.

DIGITAL PIN (DUAL MODE) DESCRIPTION (continued)

No.	Name	Type	PAD	Description
22	PD/RES	DI	CMOS	MS=0 (pin strap mode): Power down mode when PD=1. MS=1 (MCU control mode) System Reset when RES=1.
31	CLKS0/AD0	DI	CMOS/TTL	MS=0 (pin strap mode): Together with CLKS1 define MCLK frequency. MS=1 (MCU control mode): Address/Data Bit 0.
8	CLKS1	DI	CMOS/TTL	MS=0 (pin strap mode): Together with CLKS0 define MCLK frequency. MS=1 (MCU control mode): Not used should be connected to GND
30	MS0/AD1	DI	CMOS/TTL	MS=0 (pin strap mode): Together with MS1, MS2 define time slot group for DX and DR. When operating at 4.096MHz CLKS0 is used for timeslot definition. MS=1 (MCU control mode): Address/Data Bit 1.
29	MS1/AD2	DI	CMOS/TTL	MS=0 (pin strap mode): Together with MS0, MS2 define time slot group for DX and DR. When operating at 4.096MHz, CLKS0 is used for timeslot definition. MS=1 (MCU control mode): Address/Data Bit 2.
28	MS2/AD3	DI	CMOS/TTL	MS=0 (pin strap mode): Together with MS0, MS1 define time slot group for DX and DR. When operating at 4.096MHz also CLKS0 is used for timeslot definition. MS=1 (MCU control mode): Address/Data Bit 3.
27	AMU/DS	DI	CMOS/TTL	MS=0 (pin strap mode): A/µ Law sel.: AMU=0: µ law all bit inv. AMU=1: A law even bit inv. MS=1 (MCU control mode): Data Write Strobe (active low).
26	TXG/ALE	DI	CMOS/TTL	MS=0 (pin strap mode): TX gain set: TXG=0: 0.0dB TXG=1: 3.5dB MS=1 (MCU control mode): Address Latch Enable.
25	RXG/CS	DI	CMOS/TTL	MS=0 (pin strap mode): RX gain set: RXG=0: -0.5dB RXG=1: 3.0dB MS=1 (MCU control mode): Chip Select Enable.

SGS-THOMSON MICROELECTRONICS

STLC5411

2B1Q U INTERFACE DEVICE

ADVANCE DATA

GENERAL FEATURES

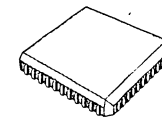
- SINGLE CHIP 2B1Q LINE CODE TRANSCEIVER
- SUITABLE FOR BOTH ISDN AND PAIR GAIN APPLICATIONS
- MEETS OR EXCEEDS ANSI U.S. AND ETSI EUROPEAN STANDARD
- SINGLE 5V SUPPLY
- 28 PIN AND PLCC44 PACKAGE
- 350mW MAX ACTIVE AND 10mW INACTIVE POWER DISSIPATION
- HCMOS3A SGS-THOMSON ADVANCED 1.2µm DOUBLE-METAL CMOS PROCESS

TRANSMISSION FEATURES

- 160 KBIT/S FULL DUPLEX TRANSCEIVER
- 2B1Q LINE CODING WITH SCRAMBLER/DESCRAMBLER
- 18KFT (5.5KM) ON 26AWG/24AWG TWISTED PAIR CABLES
- SUPPORTS BRIDGE TAPS, SPLICES AND MIXED GAUGES
- >70DB ADAPTIVE ECHO-CANCELLATION
- ON CHIP HYBRID CIRCUIT
- DECISION FEEDBACK EQUALIZATION
- ON CHIP ANALOG VCO SYSTEM
- DIRECT CONNECTION TO SMALL LINE TRANSFORMER

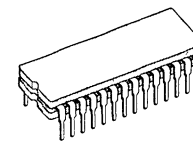
SYSTEM FEATURES

- ACTIVATION/DEACTIVATION CONTROLLER
- ON CHIP CRC CALCULATION AND VERIFICATION INCLUDING TWO PROGRAMMABLE BLOCK ERROR COUNTERS
- EOC CHANNEL AND OVERHEAD-BITS TRANSMISSION WITH AUTOMATIC MESSAGE CHECKING
- GCI AND MW/DSI MODULE INTERFACES COMPATIBLE
- DIGITAL LOOPBACKS
- COMPLETE (2B+D) ANALOG LOOPBACK IN LT
- ELASTIC DATA BUFFERS AND BACKPLANE CLOCK DE-JITTERIZER
- AUTOMODE NT1 AND REPEATER
- "U ACTIVATION ONLY" IN NT1



PLCC44

ORDERING NUMBER: STLC5411FN



Ceramic DIP28

ORDERING NUMBER: STLC5411CJ

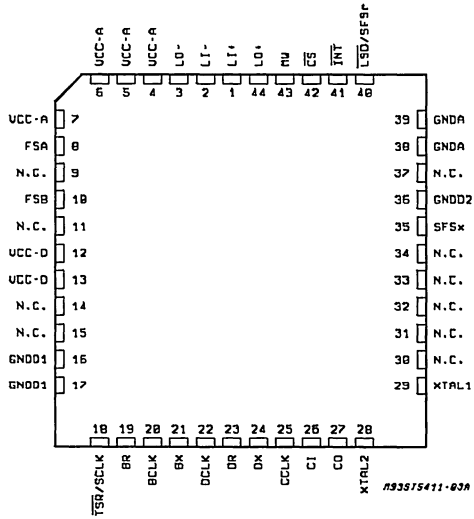
- IDENTIFICATION CODE AS PER GCI STANDARD
- EASILY INTERFACEABLE WITH ST5451 (HDLC & GCI CONTROLLER), ST5421 SID-GCI TRANSCEIVER AND ANY OTHER GCI, IDL or TDM COMPATIBLE DEVICES

INDEX

PIN CONNECTIONS (Top view)

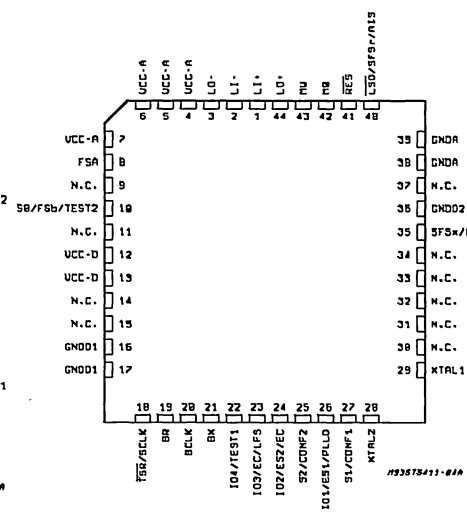
PLCC44

MICROWIRE MODE



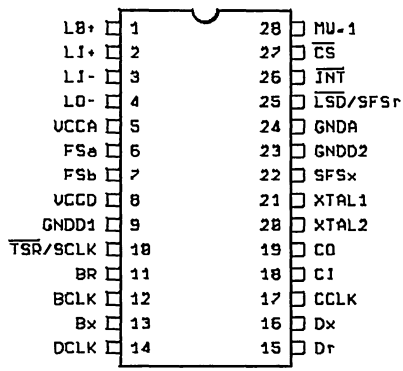
PLCC44

GCI MODE



DIP28

MICROWIRE MODE



DIP28

GCI MODE

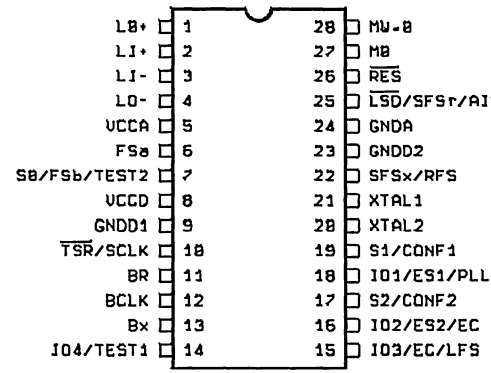
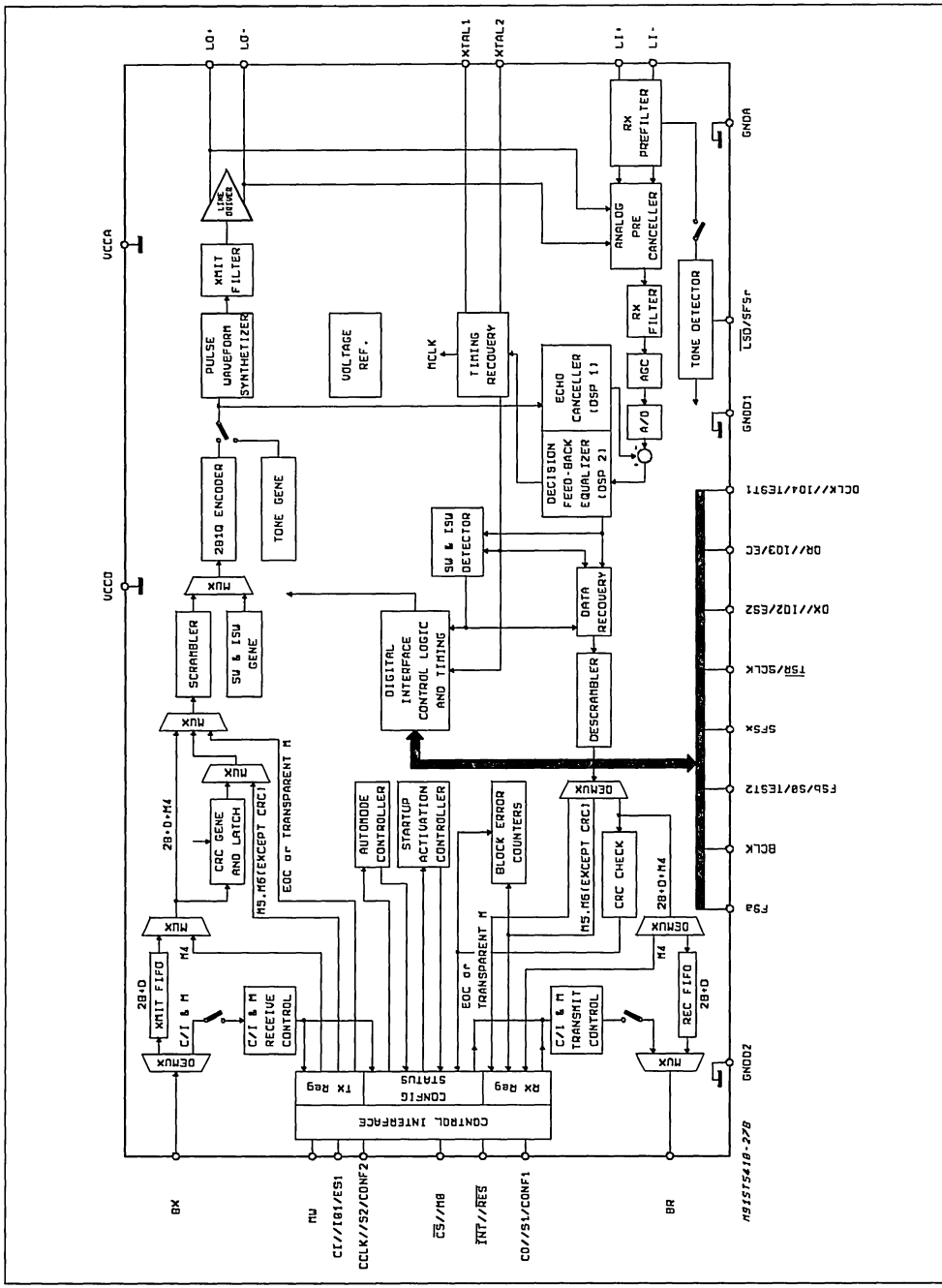


Figure 1: Block Diagram.



GENERAL DESCRIPTION

STLC5411 is a complete monolithic transceiver for ISDN Basic access data transmission on twisted pair subscriber loops typical of public switched telephone networks. The device is fully compatible with both ANSI T1.601-1988 U.S. and CSE (C32-11) French specifications. It is intended also to comply with ETSI specification both in term of transmission performances and requested features.

The equivalent of 160 kbit/s full-duplex transmission on a single twisted pair is provided, according to the formats defined in the a.m. spec. Frames include two B channels, each of 64 kbit/s, one D channel of 16 kbit/s plus an additional 4 kbit/s M channel fcr loop maintenance and other user functions. 12 kbit/s bandwidth is reserved for framing. 2B1Q Line coding is used, where pairs of bits are coded into one of 4 quantum levels. This technique results in a low frequency spectrum (160 kbit/s turn into 80 kband), thereby reducing both line attenuation and crosstalk and achieving long range with low Bit Error Rates.

The system is designed to operate on standard types of cable pairs including mixed gauges (26AWG, 24 AWG and 22 AWG) including the 15 loops configuration specified by ANSI. Good noise margins are achieved even when bridged taps are present. On 26AWG cable, the transmission range is in excess of 5.5 km (18 kft) in presence of crosstalk and noise as specified by ANSI standard. STLC5411 is designed to operate with Bit Error Rate near-end Crosstalk (NEXT) as specified in european ETSI recommendation.
To meet these very demanding specifications, the device includes two Digital Signal Processors, one configured as an adaptive Echo-Canceller to cancel the near end echoes resulting from the transmit/receive hybrid interface, the other as an adaptive line equalizer. A Digital Phase-Locked Loop (DPLL) timing recovery circuit is also included that provides in NT modes a 15.36 MHz synchronized clock to the rest of the system. Scrambling and descrambling are performed as specified in the US and French specifications.

On the system side, STLC5411 can be linked to two bus configuration simply by pin MW bias.

MICROWIRE(μW/DSI) mode (MWpin = 5V): 144 kbit/s 2B+D basic access data is transferred on a multiplex Digital System Interface with 4 different interface formats (see fig. 2 and 3) providing maximum flexibility with a limited pin count (BCLK, Bx, Br, FSa, FSb). Three pre-defined 2B+D formats plus an internal time slot assigner allows direct connection of the UID to the most common multiplexed digital interfaces (TDM/IDL). Bit and Frame Synchronisation signals are inputs or outputs depending on the configuration selected. Data buffers allow any phase between the line and the digital interface. That permits building of slave-slave configurations e.g. in NT12 trunk-cards.

It is possible to separate the D from the B channels and to transfer it on a separate digital interface (Dx, Dr) using the same bit and frame clocks as for the B channels or in a continuous mode using an internally generated 16 kHz bit clock output (DCLK).

All the Control, Status and Interrupt registers are handled via a control channel on a separate serial interface MICROWIRE compatible (CI, CO, $\overline{CS}$, CCLK, $\overline{INT}$) supported by a number of microcontroller including the MCU families from SGS-THOMSON

GCI mode (MWpin = 0V). Control/maintenance channels are multiplexed with 2B+D basic access data in a GCI compatible interface format (see fig. 4a) requiring only 4 pins (BCLK, Bx, Br, FSa). On chip GCI channel assignement allows to multiplex on the same bus up to 8 GCI channels, each supporting data and controls of one device. Bit and Frame Synchronisation signals can be inputs or ouputs depending on the configuration selected. Data buffers, again, allow to have any phase between the line interface and the digital interface.

Through the M channel and its protocol allowing to check both direction exchanges, internal registers can be configured, the EOC channel and the Overhead-bits can be monitored. Associated to the M channel, there are A and E channels for enabling the exchanged messages and to insure the flow control. The C/I channel allows the primitive exchanges following the standard protocol.

In both mode (μW and GCI) CRC is calculated and checked in both directions internally.
In LT mode, the transmit superframe can be synchronized by an external signal (SFSx) or be self running. In NT mode, the SFSx is always output synchronized by the transmit superframe.

Line side or Digital Interface side loopbacks can be selected for each B1, B2 or D channel independently without restriction in transparent or in non-transparent mode. A transparent complete analog loopback allowing the test of the transmission path is also selectable.

Activation and deactivation procedures, which are automatically processed by UID, require only the exchange of simple commands as Activation Request, Deactivation Request, Activation Indication. Cold and Warm start up procedures are operated automatically without any special instruction.

Four programmable I/Os are provided in GCI for external device control.

PIN FUNCTIONS (no Specific Microwire / GCI Mode)

Pin	Name	In/Out	Description
1, 4	LO+, LO-	Out, Out	Transmit 2B1Q signal differential outputs to the line transformer. When used with an appropriate 1:1.5 step-up transformer and the proper line interface circuit the line signal conforms to the output specifications in ANSI standard with a nominal pulse amplitude of 2.5 Volts.
2, 3	LI+, LI-	In, In	Receive 2B1Q signal differential inputs from the line transformer.
5, 8	VCCA, VCCD	In, In	Positive power supply input for the analog and digital sections, which must be +5 Volts +/-5% and must be directly connected together.
24, 9 23	GNDA,GNDD1 GNDD2	In, In In	Negative power supply pins, which must be connected together close to the device. All digital and analog signals are referred to these pins, which are normally at the system Ground.
10	TSRb	Out	(LT configuration only) This pin is an open drain output normally in the high impedance state which pulls low when B1 and B2 time-slots are active. It can be used to enable the Tristate control of a backplane line-driver.
	SCLK	Out	(NT configuration only) 15.36 MHz clock output which is frequency locked to the received line signal active as soon as UID is powered up except in NT1 Auto configuration (active only if S line activation is requested)
20	XTAL2	Out	The output of the crystal oscillator, which should be connected to one end of the crystal, if used. Otherwise, this pin must be left not connected.
21	XTAL1	In	The master clock input, which requires either a parallel resonance crystal to be tied between this pin and XTAL2, or a logic level clock input from a stable source. This clock does not need to be synchronized to the digital interface clocks (FSa, BCLK).Crystal specifications: 15.36 MHz +/-50ppm parallel resonant; Rs ≤ 20 ohms; load with 33pF to GND each side.
28	MW	In	MICROWIRE selection: When set high, MICROWIRE control interface is selected. When set low, GCI interface is selected.

PIN FUNCTIONS (specific Micro Wire mode)

Pin	Name	In/Out	Description
6	FSA	In Out	Input or Output depending of the CMS bit in CR1 register, FSA is a 8 KHz clock which indicates the start of the frame on Bx when FSA is input, or Bx and Br when FSA is output. Input or Output, the location of FSA relative to the frame on Bx or Bx and Br depens of DDM bit in CR1 register, also the selected format.
7	FSB	In Out	Input or Output depending of the CMS bit in CR1 register, FSB is a 8 KHz clock which indicates the start of the frame on Br when it is an input. When it is an output, FSB is a 8 KHz pulse conforming with the selected format and always indicating the second 64Kbit/sec channel of the frame on Br. Input or Output, the location of FSB relative to the frame on Br depends of DDM bit in CR1 register, also the selected format.
11	Br	Out	2B+D datas tristate output. Datas received from the line can be shifted out on the rising edge (at the BCLK frequency or the half BCLK frequency if format 4 is selected) during the assigned time slot. Br is in high impedance state outside the assigned time slot and during the assigned time slot of the channel if it is disabled. When D channel port is enabled, only B1 B2 are on Br.

PIN FUNCTIONS (specific Micro Wire mode)

Pin	Name	In/Out	Description
12	BCLK	In Out	Bit clock input or output depending of the CMS bit in CMR register. When BCLK is an input, its frequency may be any multiple of 8 KHz from 256 KHz to 4096 KHz in formats 1 2 3, 512 KHz to 6176 KHz in format 4. When BCLK is an output, its frequency is 256 KHz, 512 KHz, 1536 KHz, 2048 KHz or 2560 KHz depending of the selection in CR1 register; In this case, BCLK is locked to the recovered clock received from the line. Input or Output BCLK is synchronous with FSA/FSB. Datas are shifted in and out (on Bx and Br) at the BCLK frequency in formats 1 2 3. In format 4 datas are shifted out at half the BCLK frequency.
13	Bx	In	2B+D input. Basic access data to transmit to the line can be shifted in on the falling edges (at the BCLK frequency or the half BCLK frequency if format 4 is selected) during the assigned time-slots. When D channel port is enabled, only B1 & B2 sampled on Bx.
14	DCLK	Out	D channel clock output when the D channel port is enabled in continuous mode. Datas are shifted in and out (on Dx and Dr) at 16 KHz on the falling and rising edges of DCLK respectively. In master mode, DCLK is synchronous with BCLK.
15	Dr	Out	D channel data output when the D channel port is enabled D channel data is shifted out from the UID on this pin in 2 selectable modes: in TDM mode data is shifted out at the BCLK frequency (or half BCLK frequency in format 4) on the ridsing edges when the assigned time slot is active. In continuous mode data is shifted out at the DCLK frequency on the rising edge continuouly.
16	Dx	In	D channel data input when the D channel port is enabled. D channel data is shifted in from the UID on this pin in 2 selectable modes: in TDM mode data is shifted in at the BCLK frequency (or half BCLK frequency in format 4) on the falling edges when the assigned time slot is active. In continuous mode data is shifted out at the DCLK frequency on the falling edge continuously.
17	CCLK	In	Clock input for the MICROWIRE control channel: data is shifted in and out on CI and CO pins with CCLK frequency following 2 modes. For each mode the CCLK polarity is indifferent. CCLK may be asynchronous with all the others UID clocks.
18	CI	In	MICROWIRE control channel serial input: Two bytes data is shifted out the UID on this pin on the rising or the falling edge of CCLK depending of the working mode.
19	CO	Out	MICROWIRE control channel: serial output: two bytes data is shifted out the UID on this pin on the rising or the falling edge of CCLK depending of the working mode. When not enabled by CSb low, CO is high impedance.
22	SFSx	In Out	Tx Super frame synchronization. The rising edge of SFSx indicates the beginning of the transmit superframe on the line. In NT mode SFSx is always an output. In LT mode SFSx is an input or an output depending of the SFS bit in CR2 register. When SFSx is input, it must be synchronous of FSA.
25	SFSr	Out	Rx Super frame synchronization. The rising edge of SFSr indicates the begenning of the received superframe on the line. UID provides this output only when ESFR bit in CR4 register is to 1.
	LSDb	Out	Line Signal Detect output (default conf.): This pin is an open drain output which is normally in the high impedance state but pulls low when the device previously in the power down state receives a wake-up by Tone from the line. This signal is intended to be used to wake-up a micro-controller from a low power idle mode. The LSD output goes back in the high impedance state when the device is powered up.
26	INTb	Out	Interrupt output: Latched open-drain output signal which is normally high impedance and goes low to request a read cycle. Pending interrupt data is shifted out from CO at the following read-write cycle. Several pending interrupts may be queued internally and may provide several interrupt requests. INT is freed upon receiving of CS low and can goes low again when CS is freed.
27	CSb	In	Chip Select input: When this pin is pulled low, data can be shifted in and out from the UID through CI & CO pins. When high, this pin inhibits the MICROWIRE interface. For normal read or write operation, CS has to be pulled low for 16 CCLK periods of time.

PIN FUNCTIONS (specific GCI mode)

Pin	Name	In/Out	Description
6	FSA	In Out	Input or Output depending of the configuration. FSA is a 8 KHz clock which indicates the start of the frame on Bx and Br.
7	FSB	Out	In NT/TE non auto-mode configuration, FSB is a 8 KHz pulse always indicating the second 64Kbit/sec channel of the frame on Br.
	S0	In	When MO = 0 (LT/NT12 configuration): S0 associated with S1 and S2 selects a GCI channel number on Bx/Br.
	TEST2	In	Input pin to select a transmission test in all auto mode configurations. TEST2 is associated with TEST1.
11	Br	Out	2B+D and GCI control channel open drain output. Data is shifted out (at the half BCLK frequency) on the first rising edge of BCLK during the assigned channels slot. Br is in high impedance state outside the assigned time slot and during the assigned time slot of a channel if it is desabled.
12	BCLK	In Out	Bit clock input or output depending of the configuration. When BCLK is an input, its frequency may be any multiple of 16 KHz from 512 KHz to 6176 KHz.. When BCLK is an output, its frequence is 512 KHz in NT1 auto and NTRR auto configurations, 1536 KHz in NT/TE configuration; In this case, BCLK is locked to the recovered clock received from the line. Input or Output BCLK is synchronous with FSA. Datas are shifted in and out (on Bx and Br) at the half the BCLK frequency.
13	Bx	In	2B+D and GCI control channel input. Data is sampled by the UID on the second falling edge of BCLK within the period of the bit, during the assigned channels time slot.
14	IO4	In Out	General purpose programmable I/O configured by CR5 register in all non auto mode configurations.
	TEST1	In	Input pin to select a transmission test in all auto mode configurations. TEST1 is associated with TEST2.
15	IO3	In Out	General purpose programmable I/O configured by CR5 register in all non auto mode configurations.
	EC	Out	External control output pin in NT1 auto configuration. Normaly high, this pin is pulled low when an eoc message "öperate 2B+D loopback" is recognized from the line.
	LFS	In	Local febe select: When tied to 1 the febe is locally looped back. See figure 10.
16	IO2	In, Out	General purpose programmable I/O configured by CR5 register in all non auto mode configurations.
	EC	Out	External control output pin in LTRR auto configuration. Normaly high, this pin is pulled low when an ARL command is received by the UID.
	ES2	In	External status input pin. In NT1 auto and NTRR auto configurations, this status is sent on the line through the ps2 bit.
17	S2	In	When MO = 0 (LT/NT12 configuration): S2 associated with S0 and S1 selects a GCI channel number on Bx/Br.
	CONF2	In	When MO = 1: Configuration input pin. Is used associated with CONF1 to select configuration NT/TE (non auto), NT1 auto, LTRR auto and NTRR auto.
18	IO1	In Out	General purpose programmable I/O configured by CR5 register in all non auto mode configurations.
	ES1	In	External status input pin. In NT1 auto and NTRR auto configurations, this status is sent on the line through the ps1 bit.
	PLLD	In	PLL1 can be disabled in LTRR onto configuration with this pin.
19	S1	In	When MO = 0 (LT/NT12 configuration): S1 associated with S0 and S2 selects a GCI channel number on Bx/Br.
	CONF1	In	When MO = 1: Configuration input pin. Is used associated with CONF2 to select configuration NT/TE (non auto), NT1 auto, LTRR auto and NTRR auto.

PIN FUNCTIONS (specific GCI mode)

Pin	Name	In/Out	Description
22	RFS	In	Remote febe select: When tied to 0 the remote febe is not transferred. When tied to 1 febe is transparently reported. See figure 10.
25	AIS	In	Analog interface select for all auto mode configurations
	SFSr	Out	Rx Super frame synchronization. The rising edge of SFSr indicates the beginning of the received superframe on the line. UID provides this output only when ESFR bit in CR4 register is to 1 and LT/NT12 or NT/TE configuration is done.
	LSDb	Out	Line Signal Detect output (default conf.): This pin is an open drain output which is normally in the high impedance state but pulls low when the device previously in the power down state receives a wake-up by Tone from the line. This signal is intended to be used to wake-up a micro-controller from a low power idle mode. The LSD output goes back in the high impedance state when the device is powered up.
26	RESb	In	Reset input pin with internal pull-up resistor. When pulled low, all registers of the UID are reset to their default values. UID is configured according to configuration inputs bias excluding MW input which must be maintained at the 0 volt. minimum recommended pulse lenght is 200µs.
27	M0	In	Configuration input pin. When pulled low, GCI channel assigner is selected (channel number defined by inputs S0, S1, S2). When pulled high, UID is configured by pins CONF1 and CONF2.

MULTIPLE FUNCTION PIN DESCRIPTION

Pin 1: LO+ always

Pin 2: LI+ always

Pin 3: LI- always

Pin 4: LO- always

Pin 5: VCCA always

Pin 6: FSA

Function or In/Out conditions (*)				Function	In/Out
MW(pin) = 1		CMS(cr1) = 1		FSA	Out
		CMS(cr1) = 0		FSA	In
MW(pin) = 0	MO(pin) = 1	CONF2(pin) = 1	CONF1(pin) = 1	FSA	Out
			CONF1(pin) = 0	FSA	Out
		CONF2(pin) = 0	CONF1(pin) = 1	FSA	In
			CONF1(pin) = 0	FSA	Out
	MO(pin) = 0			FSA	In

(*) Only true if ANATST (internal test signal) = 0

MULTIPLE FUNCTION PIN DESCRIPTION

Pin 7: FSA

Function or In/Out conditions (*)				Function	In/Out
MW(pin) = 1		CMS(cr1) = 1		FSB	Out
		CMS(cr1) = 0		FSB	In
MW(pin) = 0	MO(pin) = 1	CONF2(pin) = 1	CONF1(pin) = 1	TEST2	In
			CONF1(pin) = 0	FSB	Out
		CONF2(pin) = 0	CONF1(pin) = 1	TEST2	In
			CONF1(pin) = 0	TEST2	Out
	MO(pin) = 0			SO	In

(*) Only true if ANATST (internal test signal) = 0

Pin 8: VCCD

Pin 9: GNDD1

Pin 10: TSR~/SCLK/TCLK

Function or In/Out conditions (*)				Function	In/Out
MW(pin) = 1		NTS(cr2) = 1		SCLK	Out
		NTS(cr2) = 0		TSR~	Out OD
MW(pin) = 0	MO(pin) = 1	CONF2(pin) = 1	CONF1(pin) = 1	SCLK	Out
			CONF1(pin) = 0	SCLK	Out
		CONF2(pin) = 0	CONF1(pin) = 1	TSR~	Out OD
			CONF1(pin) = 0	SCLK	Out
	MO(pin) = 0	NTS(cr2) = 1		SCLK	Out
		NTS(cr2) = 0		TSR~	Out OD

(*) Only true if TDSPANA (internal test signal) = 0

Pin 11: Br

Function or In/Out conditions (*)				Function	In/Out
MW(pin) = 1				Br	Out
MW(pin) = 0				Br	Out

(*) Only true if TSTDX (internal test signal) = 0

Pin 12: BCLK

Function or In/Out conditions				Function	In/Out
MW(pin) = 1		CMS(cr1) = 1		BCLK	Out
		CMS(cr1) = 0		BCLK	In
MW(pin) = 0	MO(pin) = 1	CONF2(pin) = 1	CONF1(pin) = 1	BCLK	Out
			CONF1(pin) = 0	BCLK	Out
		CONF2(pin) = 0	CONF1(pin) = 1	BCLK	In
			CONF1(pin) = 0	BCLK	Out
	MO(pin) = 0			BCLK	In

MULTIPLE FUNCTION PIN DESCRIPTION

Pin 13: Bx

Function or In/Out conditions				Function	In/Out
				Bx	In

Pin 14: DCLK/IO4/TEST1/TSYNC [R+]

Function or In/Out conditions					Function	In/Out
MW(pin) = 1		DEN(cr2) = 1	DMO(cr2) = 1		DCLK	Out
			DMO(cr2) = 0		TSYNC	Out
		DEN(cr2) = 0			TSYNC	Out
MW(pin) = 0	MO(pin) = 1	CONF2(pin) = 1	CONF1(pin) = 1		TEST1	In
			CONF1(pin) = 0	IO4(cr5) = 1	I4	In
				IO4(cr5) = 0	O4	Out
		CONF2(pin) = 0			TEST1	In
	MO(pin) = 0			IO4(cr5) = 1	I4	In
				IO4(cr5) = 0	O4	Out

Pin 15: Dr/IO3/EC/LFS/TDOUT [R+]

Function or In/Out conditions (*)					Function	In/Out
MW(pin) = 1		DEN(cr2) = 1			Dr	Out
		DEN(cr2) = 0			TDOUT	Out
MW(pin) = 0	MO(pin) = 1	CONF2(pin) = 1	CONF1(pin) = 1		EC	Out
			CONF1(pin) = 0	IO3(cr5) = 1	I3	In
				IO3(cr5) = 0	O3	Out
		CONF2(pin) = 0			LFS	In
	MO(pin) = 0			IO3(cr5) = 1	I3	In
				IO3(cr5) = 0	O3	Out

(*) Only true if TDSPANA (internal test signal) = 0

Pin 16: Dx/IO2/EC/ES2/TDIN [R+]

Function or In/Out conditions (*)					Function	In/Out
MW(pin) = 1		DEN(cr2) = 1			Dx	In
		DEN(cr2) = 0			TDIN	In
MW(pin) = 0	MO(pin) = 1	CONF2(pin) = 1	CONF1(pin) = 1		ES2	In
			CONF1(pin) = 0	IO2(cr5) = 1	I2	In
				IO2(cr5) = 0	O2	Out
		CONF2(pin) = 0	CONF1(pin) = 1		EC	Out
			CONF1(pin) = 0		ES2	In
	MO(pin) = 0			IO2(cr5) = 1	I2	In
				IO2(cr5) = 0	O2	Out

(*) Only true if TGSCEN (internal test signal) = 0

MULTIPLE FUNCTION PIN DESCRIPTION

Pin 17: CCLK/S2/CONF2

Function or In/Out conditions					Function	In/Out
MW(pin) = 1					CCLK	In
MW(pin) = 0	MO(pin) = 1				CONF2	In
	MO(pin) = 0				S2	In

Pin 18: CI/IO1/ES1/PLLD [R+]

Function or In/Out conditions					Function	In/Out
MW(pin) = 1					CI	In
MW(pin) = 0	MO(pin) = 1	CONF2(pin) = 1	CONF1(pin) = 1		ES	In
			CONF1(pin) = 0	IO1(cr5) = 1	I1	In
				IO1(cr5) = 0	O1	Out
		CONF2(pin) = 0	CONF1(pin) = 1		PLLD	In
			CONF1(pin) = 0		ES1	In
	MO(pin) = 0			IO1(cr5) = 1	I1	In
				IO1(cr5) = 0	O1	Out

Pin 19: CO/S1/CONF1

Function or In/Out conditions					Function	In/Out
MW(pin) = 1					CO	Out
MW(pin) = 0	MO(pin) = 1				CONF1	In
	MO(pin) = 0				S2	In

Pin 20: XTAL2

Pin 21: XTAL1

Pin 22: SFSx/RFS [R+]

Function or In/Out conditions					Function	In/Out
MW(pin) = 1		NTS(cr2) = 1			SFSx	Out
		NTS(cr2) = 0	SFS(cr2) = 1		SFSx	Out
			SFS(cr2) = 0		SFSx	In
MW(pin) = 0	MO(pin) = 1	CONF2(pin) = 1			SFSx	Out
		CONF2(pin) = 0			RFS	In
	MO(pin) = 0	NTS(cr2) = 1			SFSx	Out
		NTS(cr2) = 0	SFS(cr2) = 1		SFSx	Out
			SFS(cr2) = 0		SFSx	In

Pin 23: GNDD2

Pin 24: GNDA

MULTIPLE FUNCTION PIN DESCRIPTION

Pin 25: LSD~/SFSr/AIS

Function or In/Out conditions					Function	In/Out
MW(pin) = 1				ESFR(cr4) = 1	SFSr	Out OD
				ESFR(cr4) = 0	LSD~	Out OD
MW(pin) = 0	MO(pin) = 1	CONF2(pin) = 1	CONF1(pin) = 1		AIS	In
			CONF1(pin) = 0	ESFR(cr4) = 1	SFSr	Out OD
				ESFR(cr4) = 0	LSD~	Out OD
		CONF2(pin) = 0			AIS	In
	MO(pin) = 0			ESFR(cr4) = 1	SFSr	Out OD
				ESFR(cr4) = 0	LSD~	Out OD

Pin 26: INT~/RES~ [R+]

Function or In/Out conditions					Function	In/Out
MW(pin) = 1					INT~	Out OD
MW(pin) = 0					MO	In

Pin 27: CS~/MO

Function or In/Out conditions					Function	In/Out
MW(pin) = 1					CS~	In
MW(pin) = 0					MO	In

PIN28: MW

Notes: ~ = complement
: [R+] = Pull up Resistor
: Out OD = Open Drain Output

FUNCTIONAL DESCRIPTION

Digital Interfaces

STLC5411 provides a choice between two types of digital interface for both control data and (2 B+D) basic access data.

These are:

a) General Circuit Interface: GCI.

b) Microwire/Digital System Interface: µW/DSI

The device will automatically switch to one of them by sensing the MW input pin at the Power up.

µW/DSI MODE

Microwire control interface

The MICROWIRE interface is enabled when pin MW equal one. Internal registers can be written or read through that control interface.
It is constituted of 5 pins:

CI:	data in
CO:	data output
CCLK:	data clock input
CS:	Chip Select input
INT:	Interruption output

Transmission of data onto CI & CO is enabled when CS input is low.

A Write cycle or a Read cycle is always constituted of two bytes. CCLK must be pulsed 16 times while CS is low.

Transmission of data onto CI & CO is enabled following 2 modes.

- MODE A: the CCLK first edge after CSb falling edge (and fifteen others odd CCLK edges) are used to shift in the CI data, the even edges being used to shift out the CO data.
- MODE B: the CCLK first edge after CSb falling edge (and the fifteen others odd CCLK loss) are used to shift out the CO data, the even edges being used to shift in the CI data.

For each modes the first CCLK edge after CSb falling edge can be positive or negative: the UID automaticaly detects the CCLK polarity.
Mode A is the default value. To select the mode B, write MWPS register.

You can write in the UID on CI while the UID send back a register content to the microprocessor. If the UID has no message to send, it forces the CO output to all zero's.

If the UID is to be read (status change has occured in the UID or a read-back cycle has been requested by the controller), it pulls the INT output low until CS is provided. INT high to low transition is not allowed when CS is low (the UID waits for CS high if a pending interrupt occurs while CS is low) .

When CS is high, the CO pin is in the high impedance state.

Write cycle

The format to write a 8 bits message into the UID is:

A7	A6	A5	A4	A3	A2	A1	A0

1st byte

D7	D6	D5	D4	D3	D2	D1	D0

2nd byte

A7-A1: Register Address
A0: Write/Read back Indicator
D7-D0: Register Content

After the first byte is shifted in, Register address is decoded. A0 set low indicates a write cycle: the content of the following received byte has to be loaded into the adressed register.
A0 set high indicates a read-back cycle request and the byte following is not significant. The UID will respond to the request with an interrupt cycle. It is then possible for the microprocessor to receive the required register content after several other pending interrupts.

To write a 12bits message, the difference is:
limited address field: A7 - A4
extended data field (D11 - D8): A3 - A0.
The Write/Read back indicator doesn't apply; to read and write a 12 bits register two addresses are necessary.

Read cycle

When UID has a register content to send to the microprocessor, it pulls low the INT output to request CS and CCLK signals. Note that the data to send can be the content of a Register previously requested by the microprocessor by means of a read-back request.

The format of the 8 bits message sent by the UID is:

A7	A6	A5	A4	A3	A2	A1	A0

1st byte

D7	D6	D5	D4	D3	D2	D1	D0

2nd byte

A7-A1: Register Address
A0: forced to 1 if read back
forced to 0 if spontaneous
D7-D0: Register Content

To read a 12 bits message, the difference is:
limited address field: A7 - A4
extended data field (D11 - D8): A3 - A0.
The Write/Read back indicator doesn't exit.

DIGITAL SYSTEM INTERFACE

Two B channels, each at 64 kbit/s and one D channel at 16 kbit/s form the Basic access data. Basic access data is transferred on the Digital System Interface with several different formats selectable by means of the configuration register CR1.
The DSI is basically constituted of 5 wires (see fig.2 and 3):

BCLK	bit clock
Bx	data input to transmit to the line
Br	data output received from the line
FSA	Transmit Frame sync
FSB	Receive Frame sync

It is possible to separate the D channel from the B channels and to transfer it on a separate Digital Interface constituted of 2 pins:

Dx	D channel data input
Dr	D channel data ouput

The TDM (Time Division Multiplex) mode uses the same bit and frame clocks as for the B channels. The continuous mode uses an internally generated 16 kHz bit clock output:

DCLK	D channel clock output

For all formats when D channel port is enabled "continuous mode" is possible. When the D channel port is enabled in TDM mode, D bits are assigned according to the related format on Dx and Dr .

ST5410 provides a choice of four multiplexed formats for the B and D channels data as shown in fig.2 and 3.

Format 1: the 2B+D data transfer is assigned to the first 18 bits of the frame on Br and Bx I/0 pins. Channels are assigned as follows: B1(8 bits), B2(8 bits), D(2 bits), with the remaining bits ignored until the next Frame sync pulse.

Format 2: the 2B+D data transfer is assigned to the first 19 bits of the frame on Br and Bx I/O pins. Channels are assigned as follows: B1(8 bits), D(1 bit), 1 bit ignored, B2(8 bits), D(1 bit), with the remaining bits ignored until the next frame sync pulse.

Format 3: B1 and B2 Channels can be independently assigned to any 8 bits wide time slot among 64 (or less) on the Bx and Br pins. The transmit and receive directions are also independent. When TDM mode is selected, the D channel can be assigned to any 2 bits wide time slot among 256 on the Bx and Br pins or on the Dx and Dr pins (D port disabled or enabled in TDM mode respectively).

Format 4: is a GCI like format excluding Monitor channel and C/I channel. The 2B+D data transfer is assigned to the first 26 bits of the frame on Br and Bx I/O pins. Channels are assigned as follows. B1(8 bits) B2(8 bits), 8 bits ignored, D(2 bits), with remaining bits ignored up to the next frame sync pulse.

When the Digital Interface clocks are selected as inputs, FSA must be a 8 kHz clock input which indicates the start of the frame on the data input pin Bx. When the Digital Interface clocks are selected as outputs, FSA is an 8 kHz output pulse conforming to the selected format which indicates the frame beginning for both Tx and Rx directions.

When the Digital Interface clocks are selected as inputs, FSB is a 8 kHz clock input which defines the start of the frame on the data ouput pin Br. When the Digital Interface clocks are selected as outputs, FSB is a 8 kHz output pulse indicating the second 64kbit/s slot.

Two phase-relations between the rising edge of FSA/FSB and the first (or second for FSB as output) slot of the frame can be selected depending on format selected: Delayed timing mode or non Delayed timing mode.

Non delayed data mode is similar to long frame timing on the COMBOI/II series of devices: The first bit of the frame begins nominally coincident with the rising edge of FSA/B. When output, FSa is coincident with the first 8 bits wide time-slot while FSB is coincident with the second 8 bits wide time-slot. Non delayed mode is not available in format 2.

Delayed timing mode, which is similar to short frame sync timing on COMBO I/II, in which the FSA/B input must be set high at least a half cycle of BCLK earlier the frame beginning. When output, FSA 1bit wide pulse indicates the first 8 bits wide time-slot while FSB indicates the second. Delayed mode is not available in format 4.

2B+D basic access data to transmit to the line can be shifted in at the BCLK frequency on the falling edges during the assigned time-slots. When D channel port is enabled, only B1 & B2 data is shifted in during the assigned time slots. In format 4, data is shifted in at half the BCLK frequency on the receive falling edges.

2B+ D basic access data received from the line can be shifted out from the Br output at the BCLK frequency on the rising edges during the assigned time-slots. Elsewhere, Br is in the high impedance state. When the D channel port is enabled, only B1 & B2 data is shifted out from Br. In Format 4, data is shifted out at half the BCLK frequency on the transmit rising edges; there is 1.5 period delay between the rising transmit edge and the receive falling edge of BCLK.

Bit Clock BCLK determines the data shift rate on the Digital Interface. Depending on mode selected, BCLK is an input which may be any multiple of 8 kHz from 256 kHz to 6176 kHz or an output at a frequency depending on the format and the frequency selected. Possible frequencies are:
256 KHz, 512 KHz, 1536 KHz,
2048 KHz, 2560 KHz.

In format 4 the use of 256kHz is forbidden.

BCLK is synchronous with FSA/B frame sync signal. When output, BCLK is phased locked to the recovered clock received from the line.

Figure 2: DSI Interface formats: MASTER mode.

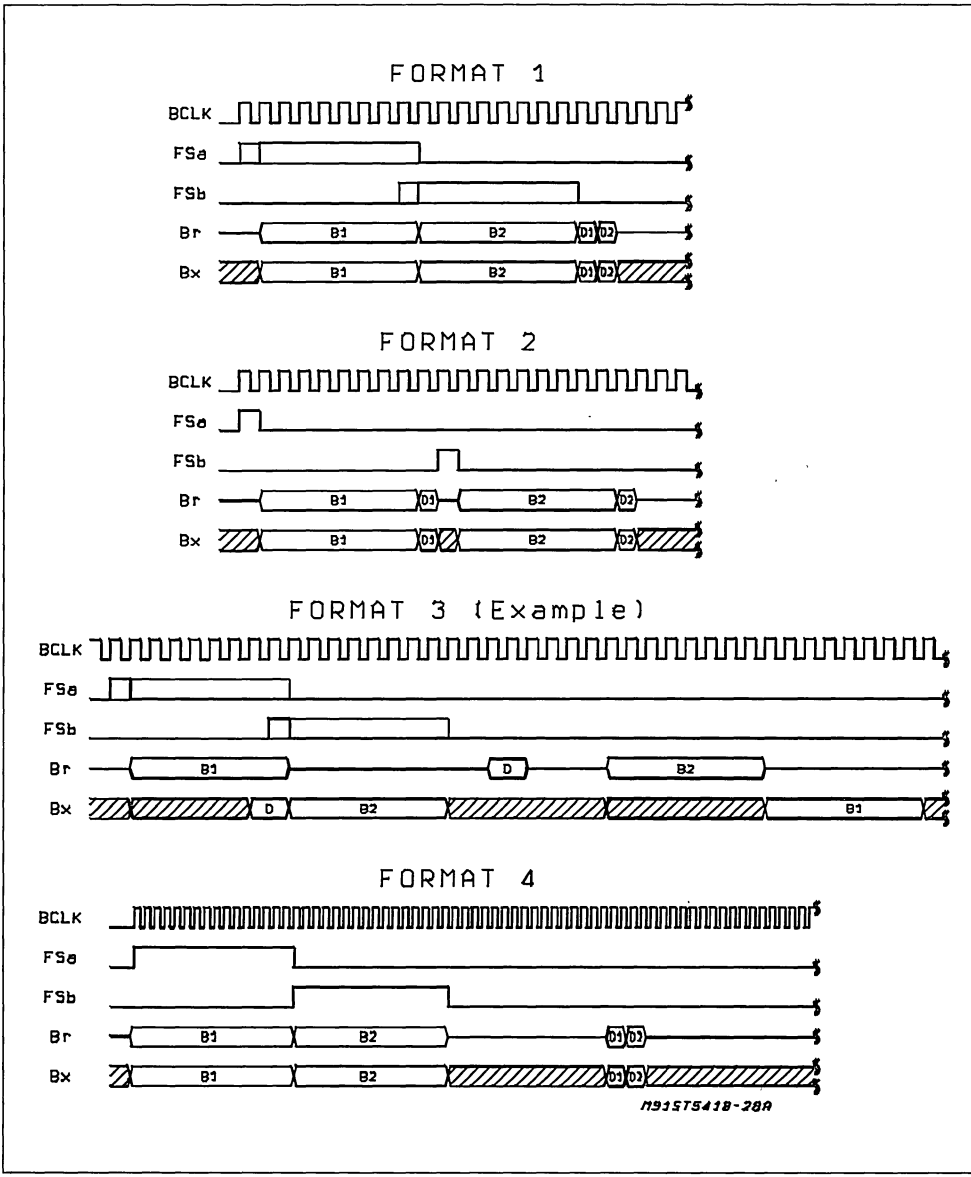
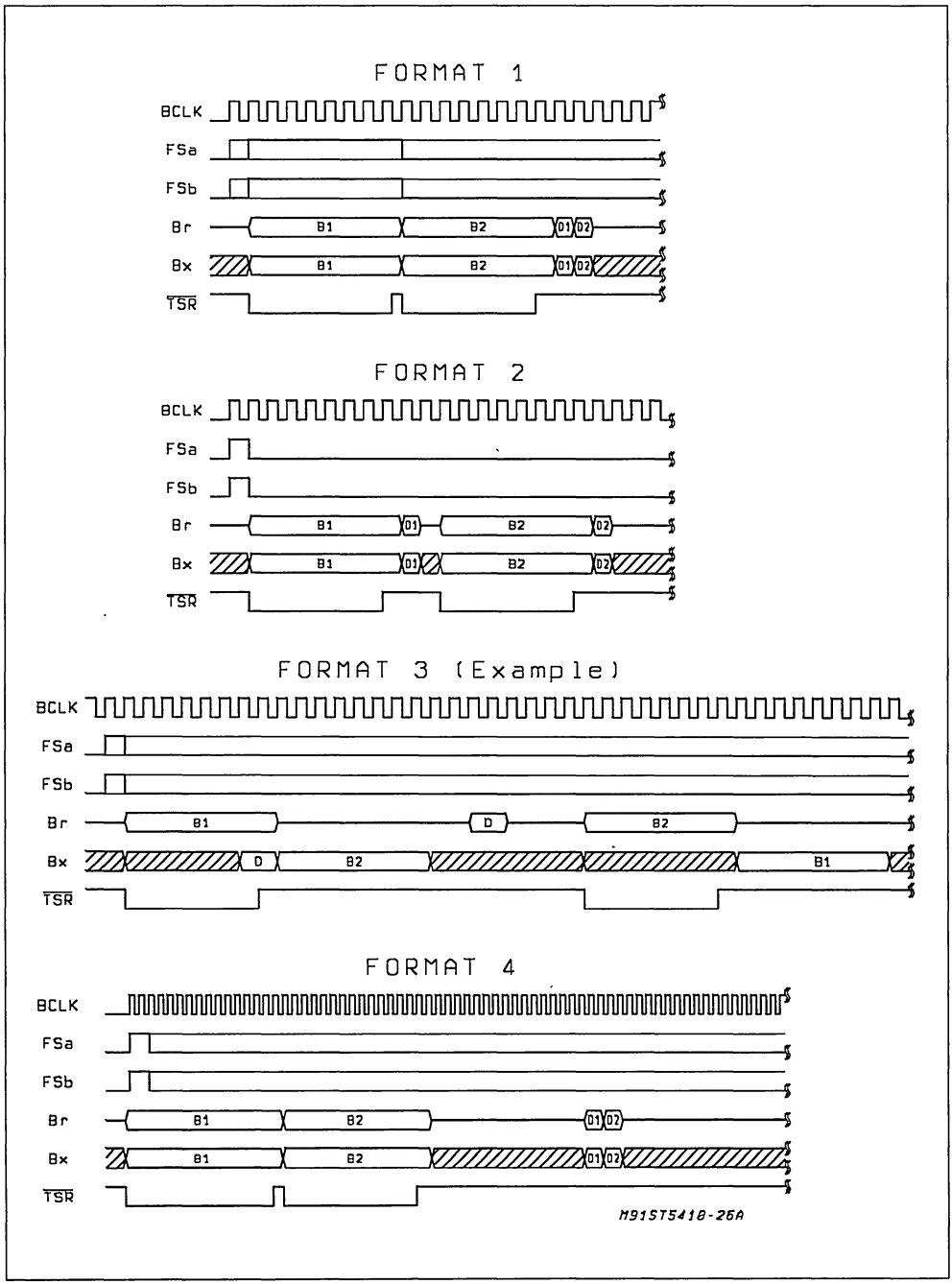


Figure 3: DSI Interface formats: SLAVE mode.



GCI MODE

The GCI is a standard interface for the interconnection of dedicated ISDN components in the different equipments of the subscriber loop :
In a Terminal, GCI interlinks the ST5410, the ISDN layer 2 (LAPD) controller and the voice/data processing components as an audio-processor or a Terminal Adaptor module.

In NT1-2, PABX subscriber line card, or central office line card (LT), GCI interlinks the UID, the ISDN Layer 2 (LAPD) controllers and eventually the backplane where the channels are multiplexed.

In NT1, GCI interlinks ST5421 (SID-GCI) and ST5410, via automode (NT1-auto). In Regenerators, GCI links both ST5410 UID in automode (NT-RR-auto, LT-RR-auto). (See Fig. 4a)

Frame Structure

2B+D data and control interface is transferred in a time-division multiplexed mode based on 8 kHz frame structure and assigned to four octets per frame and direction.(see fig.4b).

The 64 kbit/s channels B1 and B2 are conveyed in the first two octets; the third octet (M: Monitor) is used for transferring most of the control and status registers; the fourth octet (SC: Signalling & Control) contains the two D channel bits, the four C/I (command/Indicate) bits controlling the activation/deactivation procedures, and the E & A bits which support the handling of the Monitor channel.

These four octets per frame serving one ISDN subscribers line form a GCI Channel. One GCI channel calls for a bit rate of 256 kbit/s.

In NT1-2s or subscriber Line Cards up to 8 GCI channels may be carried in a frame of a GCI multiplex. The bit rate of a GCI multiplex may be from 256 kbit/s and up to 3088 kbit/s. Adjacent 4-octet slots from the frame start are numbered 0 to 7. The GCI channel takes the number of the slot it occupies. Spare bits in the frame beyond 256 bits from the frame start will be ignored by GCI compatible devices but may be used for other purposes if required (see Fig.4c). GCI channel number is selected by biasing pins S0,S1,S2.

Physical Links

Four physical links are used in the GCI.

Transmitted data to the line: Bx
Received data from the line: Br
Data clock: BCLK
Frame Synchronization clock: FSA

GCI is always synchronized by frame and data clocks derived by any master clock source.

A device used in NT mode can deliver clock sources able to synchronize GCI, either directly, or via a local Clock Generator synchronized on the line by means of the SCLK 15.36 MHz output clock. Frame clock and data clock could be independent of the internal devices clocks. Logical one on the Br output is the high impedance state while logical zero is low voltage. For E and A bits, active state is voltage Low while inactive state is high impedance state.

Figure 4a: GCI configurations of the UID.

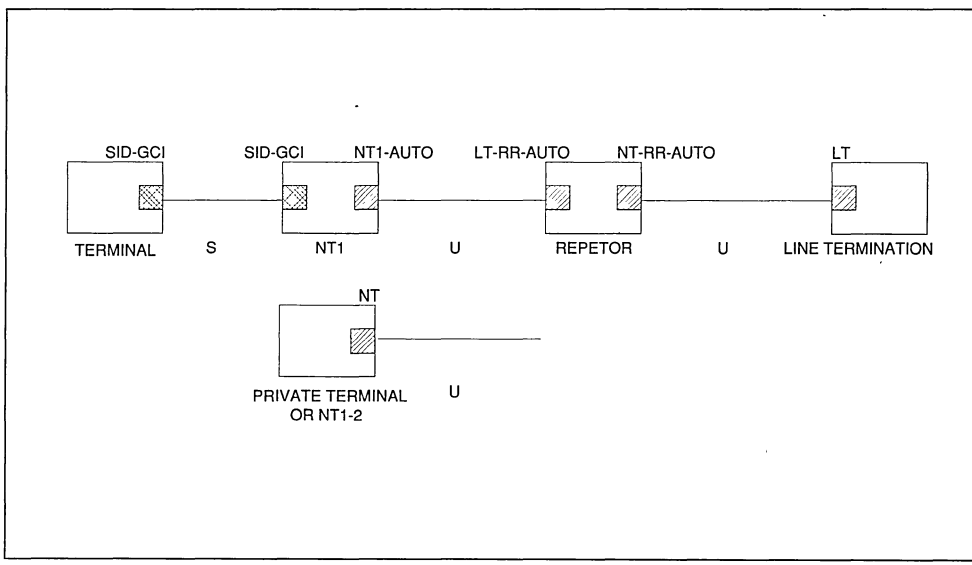


Figure 4b: GCI interface format.

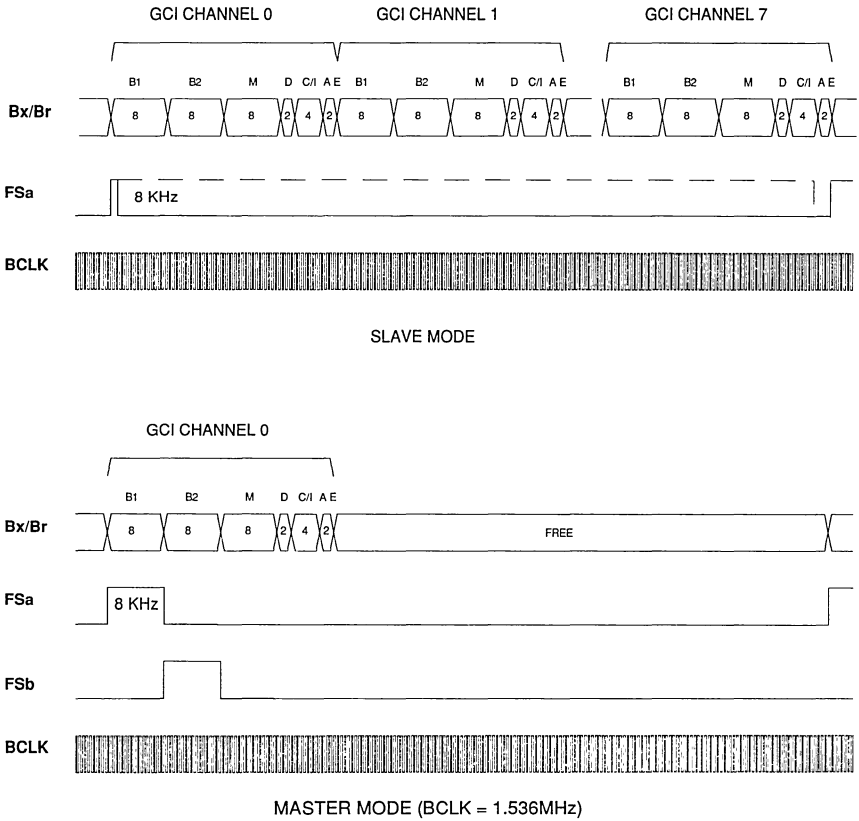
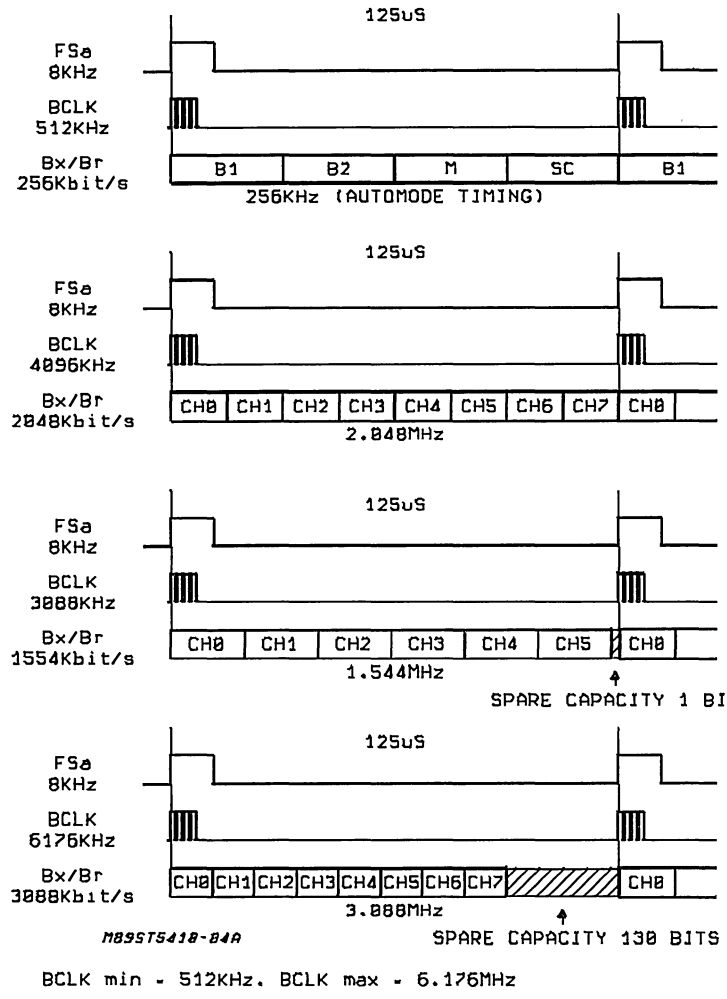


Figure 4c: GCI multiplex examples, (slave mode).



Data is transmitted in both directions at half the data clock rate. The information is clocked by the transmitter on the front edge of the data clock and can be accepted by the receiver after 1 to 1.5 period of the data clock.

The data clock (BCLK) is a square wave signal at twice the data transmission frequency on Bx and Br with a 1 to 1 duty cycle. The frequency can be choosen from 512 to 6176 kHz with 16 kHz modularity. Data transmission rate depends only on the data clock rate.

The Frame Clock FSa is a 8 kHz signal for synchronization of data transmission. The front edge of this signal gives the time reference of the first bit in the first GCI input and output channel, and reset the slot counter at the start of each frame

When some GCI channels are not selected on devices connected to the same GCI link, these time slots are free for alternative uses.

GCI configuration selection is done by biasing of input pins MW, M0, CONF1, CONF2 according to TABLE1.

Table 1: GCI Configuration selection.

Pin Number	Pin name	Configuration				
		LT/NT12*	NT/TE	NT1-AUTO	LT-RR-AUTO	NT-RR-AUTO
28	MW	0	0	0	0	0
27	M0	0	1	1	1	1
19	S1/CONF1	S1	0	1	1	0
17	S2/CONF2	S2	1	1	0	0
7	S0/FSb/TEST2	S0	FSb	TEST2	TEST2	TEST2
18	IO1/ES1	IO1	IO1	ES1	PLDD	ES1
16	IO2/ES2	IO2	IO2	ES2	EC	ES2
15	IO3/EC	IO3	IO3	EC	LFS	LFS
14	IO4/TEST1	IO4	IO4	TEST1	TEST1	TEST1
22	SFSx/RFS	SFSx	SFSx	SFSx	RFS	RFS

* Differentation between LT and NT configuration done by bit NTS in CR2 register; GCI in slave mode.

When NT1-AUTO or NT-RR-AUTO configuration is selected, BCLK bit clock frequency of 512 kHz is automatically selected

When NT configuration is selected, BCLK bit clock frequency of 1536 kHz is automatically selected.

* * Connected to V_{CC} through internal pull-up resistors.

Monitor channel

The Monitor channel is used to write and read all STLC5411 internal registers. Protocol on the Monitor channel allows a bidirectional transfer of bytes between UID and a control unit with acknowledgement at each received byte. Bytes are transmitted on the Br output and received on the Bx input in the Monitor channel time slot.
A write or read cycle is always constituted of two bytes.(see fig. 5). It is possible to operate several write or read cycles within a single monitor message.

Note: Special format is used for EOC channel.

Write cycle

The format to write a message into the UID is:

A7	A6	A5	A4	A3	A2	A1	A0

1st byte

D7	D6	D5	D4	D3	D2	D1	D0

2nd byte

A7-A1: Register Address
A0: Write/Read back Indicator
D7-D0: Register Content

After the first byte is shifted in, Register address is decoded. A0 set low indicates a write cycle: the content of the following received byte has to be loaded into the addressed register.

A0 set high indicates a read-back cycle request. the second byte content is not significative. ST5410 will respond to the request by sending back a message with the register content associated with its own address. It is then possible for the microprocessor to receive the required register content after several other pending messages. To avoid any loss of data, it is recommended to operate only one read-back request at a time.

Note: Special format is used for EOC channel.

Read cycle

When UID has a register content to send to the controller, it send it on the monitor channel directly. Note that the data to send can be the content of a Register previously requested by the controller by means of a read-back request.

The format of the message sent by the UID is:

A7	A6	A5	A4	A3	A2	A1	A0

1st byte

D7	D6	D5	D4	D3	D2	D1	D0

2nd byte

A7-A1: Register Address
A0: forced to 0 is spontaneous interrupt
D7-D0: forced to 1 if read-back Register Content

Exchange Protocol

STLC5411 validates a received byte if it is detected two consecutive times identical. (see fig. 5)

The exchange protocol is identical for both directions. The sender uses the E bit to indicate that it is sending a Monitor byte while the receiver uses A bit to acknowledge the received byte.When no message is transferred, E bit and A bit are forced to inactive state.

A transmission is started by the sender (Transmit section of the Monitor channel protocol handler) by putting the E bit from inactive to active state and by sending the first byte on Monitor channel in the same frame. Transmission of a message is allowed only if A bit sent from the receiver has been set inactive for at least two consecutive frames. When the receiver is ready, it validates the incoming byte when received identical in two consecutive frames. Then, the receiver set A bit from the inactive to the active state (preacknowledgement) and maintain active at least in the following frame (acknowledgement).

If validation is not possible (two last bytes received are not identical) the receiver aborts the message by setting the A bit active for only a single frame.The second byte can be transmitted by the sender putting the E bit from the active to the inactive state and sending the second byte on the Monitor channel in the same frame . The E bit is set inactive for only one frame. If it remains inactive more than one frame, it is an end of message. The second byte may be transmitted only after receiving of the pre-acknowledgement of the previous byte . Each byte has to be transmitted at least in two consecutive frames.

The receiver validates the current received byte as for the first one and then set the A bit in the next two frames first from the active state to the inactive state (pre-acknowledgement) and back to the active (acknowledgement). If the receiver cannot validates the received current byte (two bytes received not identical)it pre-acknowledges normally but let the A bit in the inactive state in the next frame which indicates an abort request . If a message sent by the UID is aborted, the UID will send again the complete message until receiving of an acknowledgement . A message received by the UID can be acknowledged or aborted with flow Control.

The most significant bit (MSB) of Monitor byte is sent first on the Monitor channel. E & A bits are active low and inactive state on Br is 5 V. When no byte is transmitted, Monitor channel time slot on Br is in the high impedance state.

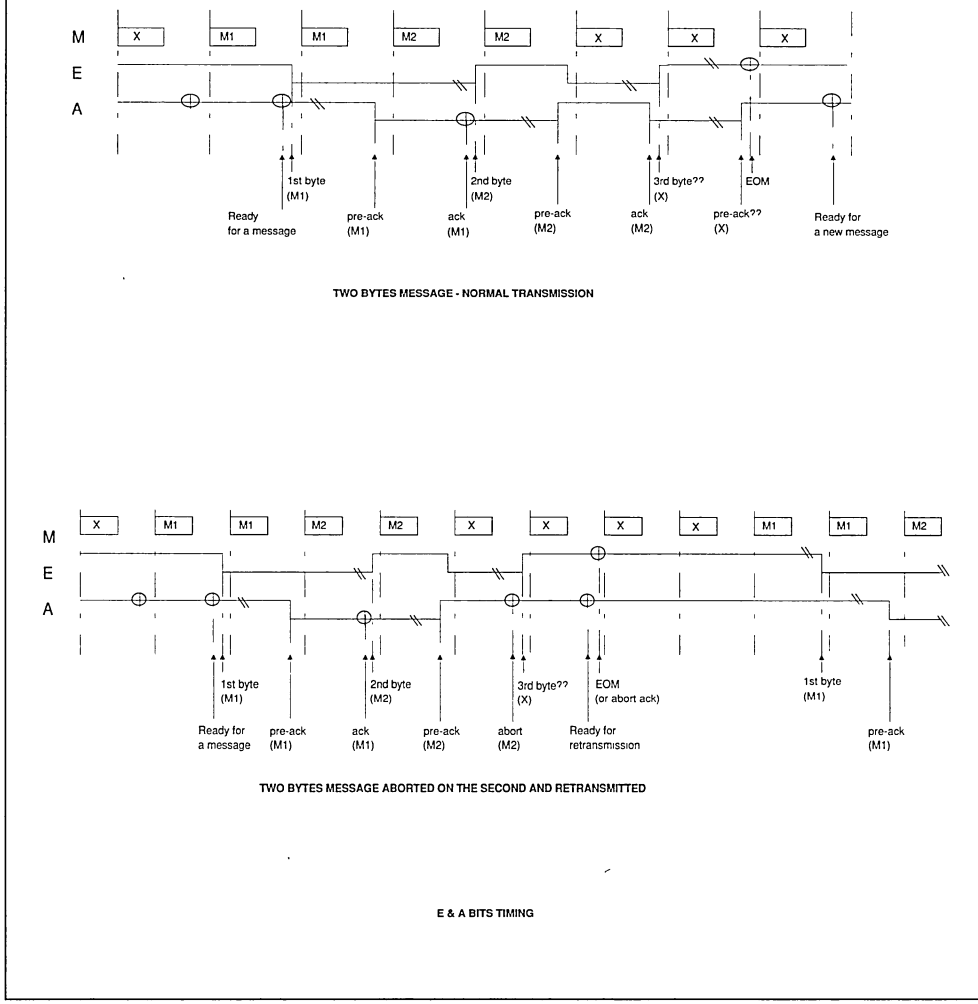
A 24 ms timer is implemented in the UID. This timer (when enabled) starts each time the sender starts a byte sending and waits for a pre acknowledgement.

C/I channel

The C/I channel is used for TXACT and RXACT registers write and read operation. However, it is possible to access to ACT registers by monitor channel: this access is controled by the CID bit in CR2 register.

The four bits code (C1,C2,C3,C4) of TXACT register can be loaded in the UID by writing permanently this code in the C/I channel time-slot on Bx input every GCI frames. The UID takes into account the received code when it has been received two consecutive times identical. When a status change occurs in the RXACT register, the new (C1,C2,C3,C4) code is sent in the C/I channel time-slot on Br output every GCI frames. This code is sent permanently by the UID until a new

Figure 5: GCI Monitor channel messaging examples.



status change occurs in RXACT register.
C1 bit is sent first to the line.

LINE CODING AND FRAME FORMAT

2B1Q coding rule requires that binary data bits are grouped in pairs so called quats (see Tab.2). Each quat is transmitted as a symbol, the magnitude of which may be 1 out 4 equally spaced voltage levels (see Fig. 6). +3 quat refers to the nominal pulse waveform specified in the ANSI standard. Other quats are deduced directly with respect of the ratio and keeping of the waveform.

The frame format used in UID follows ANSI specification (see Tab. 3 and 4). Each complete frame consists of 120 quats, with a line baud rate of 80 kbaud, giving a frame duration of 1.5ms. A nine quats lenght sync-word defines the framing boundary. Furthermore, a Multiframe consisting of 8 frames is defined in order to provide sub-channels within the spare bits M1 to M6. Inversion of the syncword defines the multiframe boundary. In LT, the transmit multiframe starting time may be synchronized by means of a 12 ms period of time pulse on the SFSx pin selected as an input (bit SFS in CR2); If SFSx is selected as an output, SFSx provides a square wave signal with the rising edge indicating the multiframe starting time. In NT, the transmit multiframe starting time is provided on SFSx output by the rising edge of a 12 ms period of time square wave signal. LT or NT, when pin 25 is selected as SFSr by mean of bit ESFr in CR4, SFSr is a square wave open drain output indicating the received superframe on the line. (see figure 7). Prior to transmisssion, all data, with the exception of the sync-word,is scrambled using a self-synchronizing scrambler to perform the specified 23rd-order polynomial. Descrambling is included in the receiver. Polynomial is different depending on the direction LT to NT or vice versa.

TRANSMIT SECTION

Data transmitted to the line consists of the 2B+D channel data received from the Digital Interface through an elastic data buffer allowing any phase deviation with the line, the activation/deactivation bits (M4) from the on-chip activation sequencer, the CRC code plus maintenance data (eoc channels) and other spare bits in the overhead channels (M4, M5, M6). Data is multiplexed and scrambled prior to addition of the sync-word, which is generated within the device. A pulse waveform synthesizer then drives the transmit filter, which in turn passes the line signal to the line driver. The differential line-driver Outputs, LO+, LO- are designed to drive a transformer through an external termination circuit. A 1:1.5 transformer designed as shown in the Application section, results in a signal amplitude of 2.5V pk nomince on the line for single quats of the +3 level. (see output pulse template fig.8). Short-circuit protection is included in the output stage; over-voltage protection must be provided externally.

In LT applications, the Network reference clock given by the FSa 8kHz clock input synchronizes the transmitted data to the line. The Digital Interface normally accepts BCLK and Fsa signals from the network, requiring the selection of Slave Mode in CR1. A Digital Phase-Locked Loop (DPLL#1) on the UID allows the SCLK frequency to be plesiochronous with respect to the network reference clock (8 kHz FSa input). With a tolerance on the XTAL1 oscillator of 15.36 MHz +/- 100 ppm, the lock-in range of DPLL1 allows the network clock frequency to deviate up to +/- 50ppm from nominal.

In LT, if DSI is selected in Master mode, (Microwire only, bit CMS = 1 in CR1), BCLK and FSa signals are outputs frequency synchronized to XTAL1 input, DPLL#1 is disabled.

In NT applications, data is transmitted to the line with a phase deviation of half a frame relative to the received data as specified in the ANSI standard.

RECEIVE SECTION

The receive input signal should be derived from the transformer by a coupling circuit as shown in the Application section. At the front end of the receive section is a continuous filter which limits the noise bandwidth to approximately 100kHz. Then, an analog pre-canceller provides a degree of echo cancellation in order to limit the dynamic range of the composite signal which noise bandwidth limited by a 4th order Butterworth switched capacitor low pass filter. After an automatic gain control, a 13bits A/D converter then samples the composite received signal before the echo cancellation from local transmitter by means of an adaptive digital transversal filter. The attenuation and distortion of the received signal from the far-end, caused by the line, is equalized by a second adaptive digital filter configured as a Decision Feedback Equalizer (DFE), that restores a flat channel response with maximum received eye opening over a wide spread of cable attenuation characteristics.

A timing recovery circuit based on a DPLL (Digital Phase-Locked Loop) recovers a very low-jitter clock for optimum sampling of the received symbols. The 15.36MHz crystal oscillator (or the logic level clock input) provides the reference clock for the DPLL. In NT configuration, SCLK output provides a very low jitterized 15.36MHz clock synchronized from the line.

Received data is then detected and flywheel synchronization circuit searches for and locks onto the frame and superframe syncwords. ST5410 is

Table 2: 2B1Q Encoding of 2B+ D Fields.

Data	Time →								
	B_I				B_Q				D
Bit Pairt	$b_{11}b_{12}$	$b_{13}b_{14}$	$b_{15}b_{16}$	$b_{17}b_{18}$	$b_{21}b_{22}$	$b_{23}b_{24}$	$b_{25}b_{26}$	$b_{27}b_{28}$	d_1d_2
Quat # (relative)	q_1	q_2	q_3	q_4	q5	q_6	q_7	q_8	q_9
# Bits	8				8				2
# Quats	4				4				1

Where:
b_{11} = first bit of B_1 octet as received at the S/T interface

b_{18} = last bit of B_I octet as received at the S/T interface

b_{21} = first bit of B_2 octet as received at the S/T interface

b_{28} = last bit of B_2 octet as received at the S/T interface

d_1 d_2 = consecutive D-channel bits (d_1 is first bit of pair as received at the S/T interface)

q_i = ith quat relative to start of given 18-bit 2B+D data field.

NOTE. There are 12 2B+D 18-bit fields per 1.5 msec basic frame.

Table 3: Network-to-NT 2B1Q Superframe Technique and Overhead Bit Assignments.

		FRAMING	2B+D	Overhead Bits (M_1-M_6)					
	Quat Positions	1-9	10-117	118s	118m	119s	119m	120s	120m
	Bit Positions	1-18	19-234	235	236	237	238	239	240
Super Frame #	Basic Frame #	Sync Word	2B+D	M_1	M_2	M_3	M_4	M_5	M_6
A	1	ISW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	act	1	1
	2	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	dea	1	febe
	3	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	1	crc_1	crc_2
	4	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	1	crc_3	crc_4
	5	SW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	1	crc_5	crc_6
	6	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	1	crc_7	crc_8
	7	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	uoa	crc_9	crc_{10}
	8	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	aib	crc_{11}	crc_{12}
B,C,...									

NT-to-Network superframe delay offset from Network-to-NT superframe by 60 ± 2 quats (about 0.75 ms). All bits than the Sync Word are scrambled.

Symbols & Abbreviations:

"1" reserve = reserved bit for future standard; set = 1

eoc embedded operations channel
a = address bit
dm = data/message indicator
i = information (data/message)

SW synchronization word

ISW inverted synchronization word

s sign bit (first) in quat

m magnitude bit (second) in quat

act activation bit

crc cyclic redundancy check: covers 2B+D & M4
1 = most significant bit
2 = next most significant bit
etc

febe far end block error bit (set = 0 for errored superframe)

dea deactivation bit (set = 0 to announce deactivation)

uoa u only activation bit (set = 1 to activate S/T)

aib alarm indication bit (set = 0 to indicate interruption)

Table 4: NT-to-Network 2B1Q Superframe Technique and Overhead Bit Assignments.

		FRAMING	2B+D	Overhead Bits (M_1-M_6)					
	Quat Positions	1-9	10-117	118s	118m	119s	119m	120s	120m
	Bit Positions	1-18	19-234	235	236	237	238	239	240
Super Frame #	Basic Frame #	Sync Word	2B+D	M_1	M_2	M_3	M_4	M_5	M_6
1	1	ISW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	act	1	1
	2	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	ps_1	1	febe
	3	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	ps_2	crc_1	crc_2
	4	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	ntm	crc_3	crc_4
	5	SW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	cso	crc_5	crc_6
	6	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	1	crc_7	crc_8
	7	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	sai	crc_9	crc_{10}
	8	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	1	crc_{11}	crc_{12}
2,3,...									

NT-to-Network superframe delay offset from Network-to-NT superframe by 60 ± 2 quats (about 0.75 ms). All bits than the Sync Word are scrambled.

Symbols & Abbreviations:

"1" reserve = reserved bit for future standard; set = 1

eoc embedded operations channel
a = address bit
dm = data/message indicator
i = information (data/message)

SW synchronization word

ISW inverted synchronization word

s sign bit (first) in quat

m magnitude bit (second) in quat

act activation bit

ps_1, ps_2 power status bits (set = 0 to indicate power problems)

ntm NT in Test Mode bit (set = 0 to indicate test mode

cso cold-start-only bit (set = 1 to indicate cold-start-only

crc cyclic redundancy check: covers 2B+D & M4
1 = most significant bit
2 = next most significant bit
etc

febe far end block error bit (set = 0 for errored superframe)

sai S/T interface activation indication bit.

Figure 6: Example of 2B1Q Quaternary Symbols.

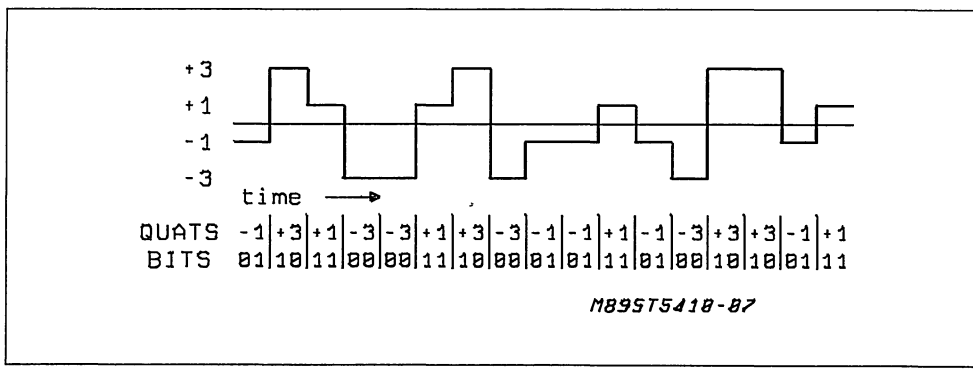


Figure 7: Superframe I/O pin SFS

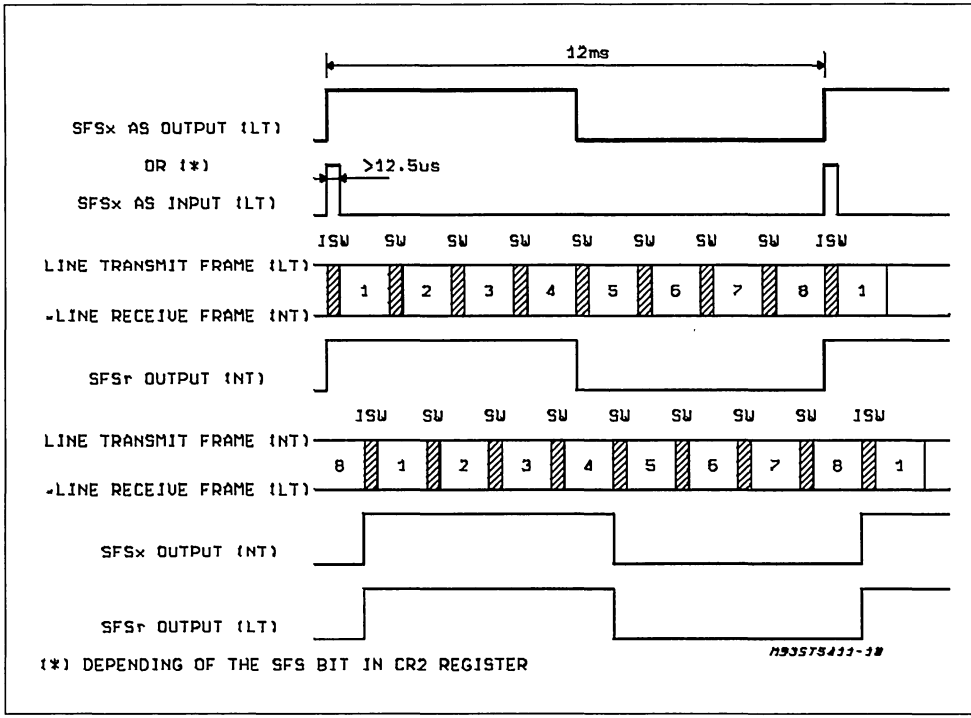
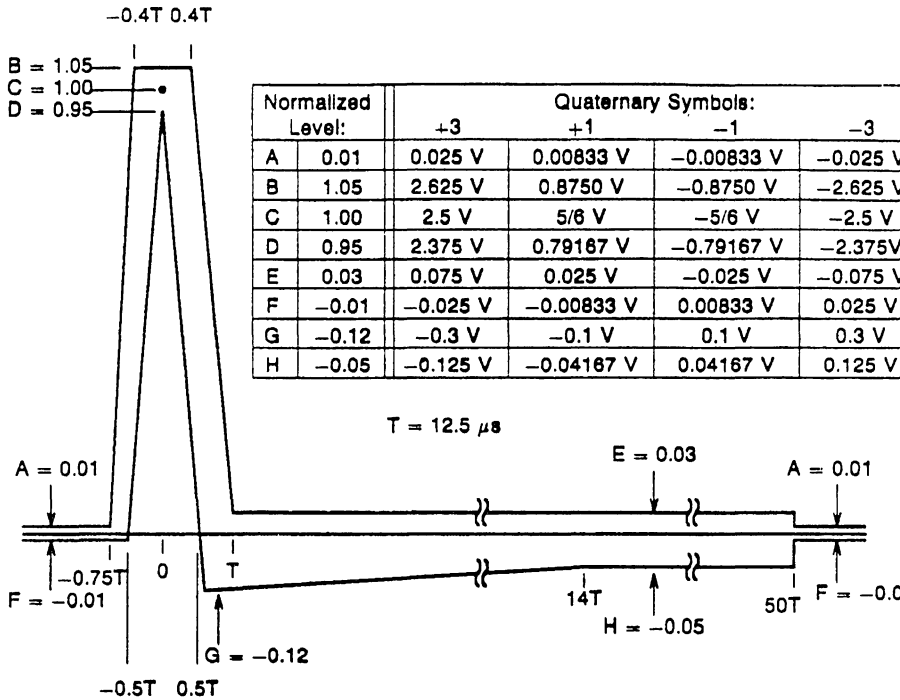


Figure 8: Normalized output pulse from



Normalized Level:		Quaternary Symbols: +3	+1	−1	−3
A	0.01	0.025 V	0.00833 V	−0.00833 V	−0.025 V
B	1.05	2.625 V	0.8750 V	−0.8750 V	−2.625 V
C	1.00	2.5 V	5/6 V	−5/6 V	−2.5 V
D	0.95	2.375 V	0.79167 V	−0.79167 V	−2.375V
E	0.03	0.075 V	0.025 V	−0.025 V	−0.075 V
F	−0.01	−0.025 V	−0.00833 V	0.00833 V	0.025 V
G	−0.12	−0.3 V	−0.1 V	0.1 V	0.3 V
H	−0.05	−0.125 V	−0.04167 V	0.04167 V	0.125 V

frame-synchronized when two consecutive synchwords have been consecutively detected. Frame lock will be maintained until six consecutive errored sync-words are detected, which will cause the flywheel to attempt to re-synchronize. If a loss of frame sync condition persists for 480ms the device will cease searching, cease transmitting and go automatically into the RESET state, ready for a further cold start. When UID is frame-synchronized, it is superframe-locked upon the first superframe sync-word detection. No loss of superframe sync-word is provided.

While the receiver is synchronized, data is descrambled using the specified polynomial, and individual channels demultiplexed and passed to their respective processing circuits: user's 2B+D channel data is transmitted to the Digital Interface through an elastic data buffer allowing any phase deviation with the line; the activation/deactivation bits (M4) are transmitted to the on-chip activation sequencer; CRC is transmitted to CRC checking section while maintenance data (eoc) and other spare bits in the overhead channels (M4, M5, M6) are stored in their respective Rx registers.

In NT applications, if the Digital Interface is selected in master mode (see CR1) BCLK and FSa clock outputs are phase-locked to the recovered clock. If it is selected in Slave mode ie for NT1-2 application, the on-chip elastic buffers allow BCLK and FSa to be input from an external source, which must be frequency locked to the received line signal ie using the SCLK output but with arbitrary phase.

ELASTIC BUFFERS

The UID buffers the 2B+D data in elastic fifos which are 3 line-frames deep in each direction. When the Digital Interface is a timing slave, these FIFOs compensate for relative jitter and wander between the Digital Interface and the line. Each buffer can absorb wander up to 18µs at 80 KHz max without "slip". This is particulary convenient for NT1-2 or PABX application in case the local reference clock is jitterized and wandered relative to the incoming signal from the line.

MAINTENANCE FUNCTIONS

M channel

In each frame there are 6 "overhead" bits assigned to various control and maintenance functions. Some programmable processing of these bits is provided on chip while interaction with an external controller provides the flexibility to take full advantage of the maintenance channels. See OPR, TXM4, TXM56, TXEOC, RXM4, RXM56, RXEOC registers description fo details. New data written to any of the Overhead bit Transmit Registers is resynchronized internally to the next available complete superframe or half superframe, as appropriate.

Embedded Operation Channel (EOC)

The EOC channel consists of two complete 12 bits messages per superframe, distributed through the M1, M2 and M3 bits of each frame. Each message is composed of 3 fields; a 3 bit address identifying the message destination/origin, a 1 bit indicator for the data mode i.e. encoded message or raw data, and an 8 bits information field. The Control Interface (Microwire or Monitor channel in GCI) provides access to the complete 12 bits of every message in TX and RX EOC registers.

When non-auto mode is selected, UID does not interpret the received eoc messages e.g. "send corrupted CRC"; therefore the appropriate command instruction must be written to the device e.g. "set to one bit CTC in register CR4". It is possible to select a transparent transmission mode in which the EOC channel can be considered as a transparent 2 kbit/s channel. See OPR register description for details.

When auto-mode is selected in GCI configuration, UID performs automatic recognition/acknowlegment of the EOC messages sent by the network according to processing defined in ANSI standard and illustrated in figure 9. When UID recognizes a message with the appropriate address and a known command, it performs automatically the relevant action inside the device and send a message at the digital interface as appropriate. Table 5 gives the list of recognized eoc messages and associated actions.

When NT-RR-AUTO configuration is selected, eoc addressing is processed according to appendix E of T1E1.601 standard:

- If address of the eoc message received from LT is in the range of 2 to 6, UID decrements address and pass the message onto GCI.
- If address of the eoc message received from GCI is in the range of 1 to 5, UID increments address and pass the message onto the line toward LT.
- If data/msg indicator is set to 0, UID pass data on transparently with eoc address as described above.

M4 channel

M4 bit positions of every frame is a channel in which are transmitted data bits loaded from the TXM4 transmit register and from the on-chip activation sequencer once the superframe. On the receive side, M4 bits from one complete superframe are first validated and then stored in the RXM4 Receive Register or transmitted to on-chip activation sequencer. See OPR, TXM4 and RXM4 registers description for details.

When NT1-AUTO or NT-RR-AUTO mode is selected, bits ps1 and ps2 in M4 channel are controlled directly by biasing input pins ES1 and ES2 respectively. e.g. ps1 is sent continuously to the line equal 0 when ES1 input is forced at 0 Volt.

Spare M5 and M6 bits
The spare bit positions in the M5 and M6 field form a channel in which are transmitted data bits loaded from the TXM56 transmit register. On the receive side, the spare bits in the M5 and M6 field are first validated and then stored in the RXM56 receive register. See OPR, TXM56 and RXM56 registers description for details.

CRC calculation/checking
In transmit direction, an on-chip CRC calculation circuit automatically generates a checksum of the 2B+D+M4 bits using the specified 12th order polynomial. Once per superframe, the CRC is transmitted in the M5 and M6 bit positions. In receive direction, a checksum is again calculated on the same bits as they are received and, at the end of the superframe compared with the received CRC. The result of this comparison generates a "Far End Block Error" bit (febe) which is transmitted back towards the other end of the Line in the next but one superframe and an indication of Near End Block Error is sent to the system by means of Register RXM56. If there is no error in superframe, febe is set = 1, and if there is one or more errors, febe is set = 0.

UID also includes two 8 bits Block Error Counters associated with the febe bits transmitted and received. It is then possible to select one Error Counter per direction or to select only one counter for both by means of bit 2CE in OPR register. Block error counting is always enabled but it is possible to disabled the threshold interrupt and/or to enable/disable the interrupt issued at each received or transmitted block error detection. See OPR register for details.

Loopbacks
Six transparent or non transparent channel loopbacks are provided by UID. It is therefore possible to operate any loopback on B1, B2 and D channels line to line or DSI/GCI to DSI/GCI. Command are grouped in CR3 register.

In addition to the channel loopbacks in LT modes, a complete transparent loopback operated at the transmission side of UID allows the device to activate through an appropriate sequence with the complete data stream looped-back to the receiver. Therefore, most of analog/digital clock and data recovery circuits are tested. After activation completed, an AI status indication is reported. Complete loopback is enabled with ARL command in TXACT register.

Figure 9: EOC message processing mode.

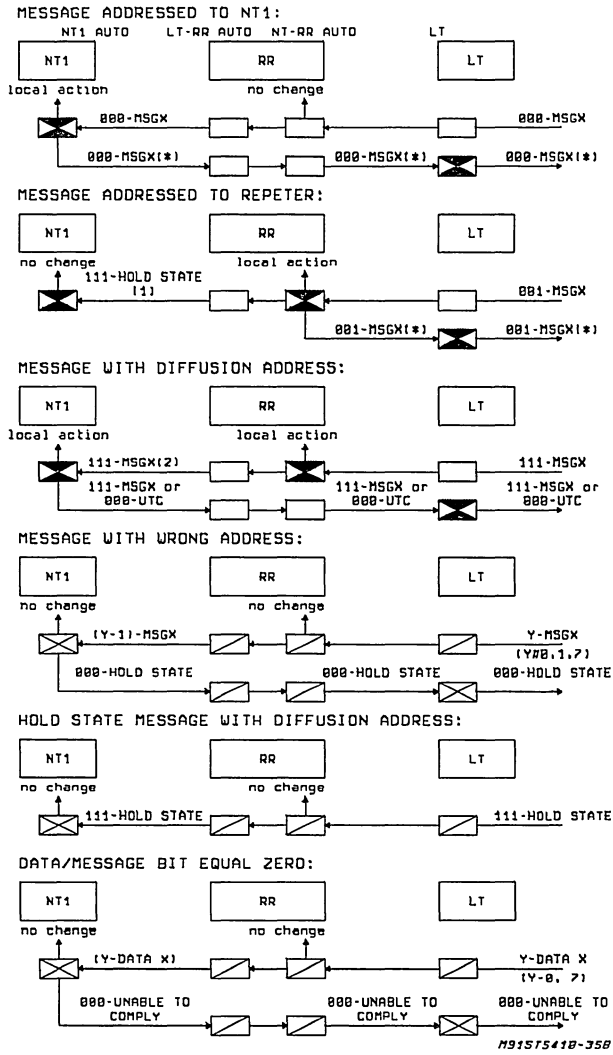


Figure 10: CRC Errors Processing (auto-mode)

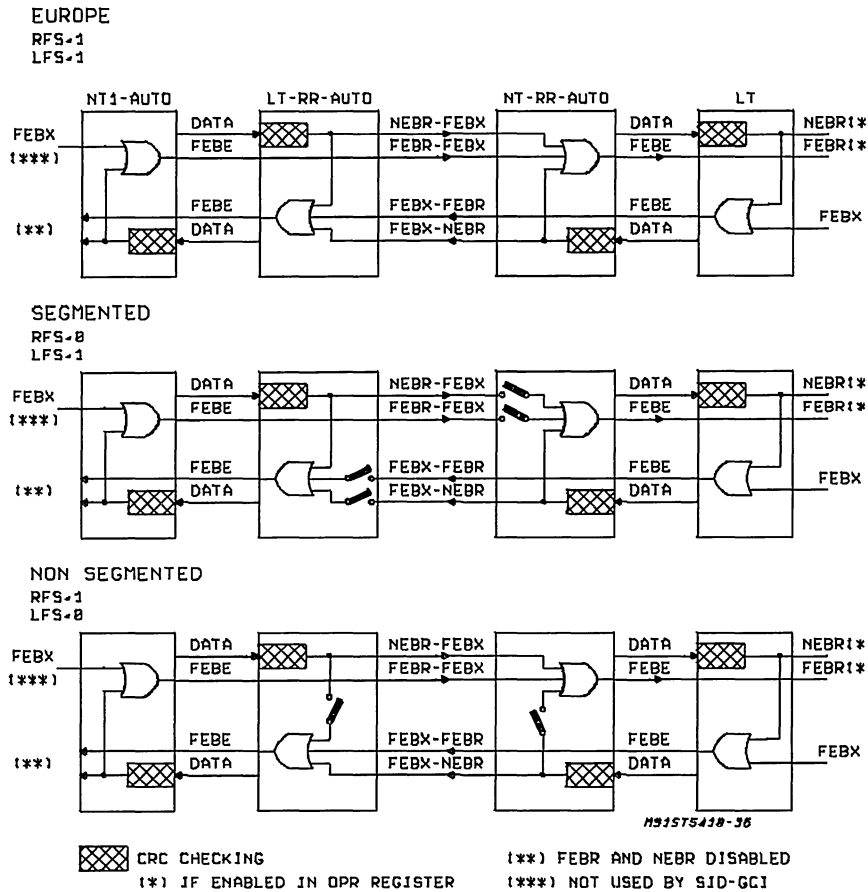


Table 5: EOC message processing: local actions.

NT1-AUTO: (eoc address 000 or 111)

Message	Code	Local action
Operate 2B+D loopback	0101 0000	Send ARL code on C/I channel to operate Loopback 2 in SID-GCI. Forces EC output low
Operate B1channel Loopback	0101 0001	Performs transparent loopback on B1 channel identical to LB1 command in CR3
Operate B2 channel Loopback	0101 0010	Performs transparent loopback on B2 channel identical to LB2 command in CR3
Request Corrupted CRC	0101 0011	Performs corruption of the transmit CRC identical to CTC command in CR4.
Notify of Corrupted CRC	0101 0100	No action taken. Send back to the Network unable to comply message.
Return to Normal	1111 1111	All outstanding EOC operations are reset.
Hold state	0000 0000	All outstanding EOC operations maintained in their present state
Unable to comply	1010 1010	Sent by UID to indicate that the message is not in its menu

NT-RR-AUTO: (eoc address 001 or 111)

Message	Code	Local action
Operate 2B+D loopback	0101 0000	Send ARL code on C/I channel to operate Loopback 1A in UID configured in LT-RR-AUTO. Forces EC output low.
Operate B1channel Loopback	0101 0001	Performs transparent loopback on B1 channel identical to LB1 command in CR3
Operate B2 channel Loopback	0101 0010	Performs transparent loopback on B2 channel identical to LB2 command in CR3
Request Corrupted CRC	0101 0011	Performs corruption of the transmit CRC identical to CTC command in CR4.
Notify of Corrupted CRC	0101 0100	No action taken. Send back to the Network unable to comply message.
Return to Normal	1111 1111	All outstanding EOC operations are reset.
Hold state	0000 0000	All outstanding EOC operations maintained in their present state
Unable to comply	1010 1010	Sent by UID to indicate that the message is not in its menu

IDENTIFICATION CODE (GCI)

In GCI configuration, a read-only register IDR contains a reference code agreed by the GCI standard and refering to SGS-THOMSON STLC5411 device.

STLC5411 device reference code is 08 H. This code is sent on Monitor channel of GCI interface upon read-back request.

GENERAL PURPOSE I/Os (GCI)

When GCI non-auto mode is selected, (NT or LT), four programmable I/Os (IO1, IO2, IO3, IO4) are provided and associated with CR5 register. Each I/O is internally pulled-up with a 50kΩ resistor. Input or output can be selected for each pin independently from the others by means of bits IO1, IO2, IO3, IO4 in CR5. D1, D2, D3, D4 bits give the logical value of the I/O pins respectively. When a status change occurs on one of the input pins, CR5 is sent on the monitor channel of the GCI interface.

When GCI auto-mode is selected, two inputs (ES1, ES2) and one output (EC) are provided in NT1-AUTO and NT-RRAUTO configurations only. ES1 and ES2 inputs drive the logical values of ps1 and ps2 bits in the M4 channel on the line while EC ouput normally high is driven low using the eoc message "operate 2B+D loopback. This intends to provide power supply testing command occuring simultaneously with the loopback command.

TEST FUNCTIONS

Various test functions are provided for transmitted pulse waveform checking, power spectral density measurement and transmitter linearity.

Three commands in TXACT register are provided. The associated test function is enabled as long as the command is not disabled by any other command.

SP1: (0010) Send Single Pulses+1, -1:
+1, -1, pulses are transmitted consecutively onto the line, one pulse per frame.

SP3: (1011) Send Single Pulses+3, -3:
+3, -3, pulses are transmitted consecutively onto the line, one pulse per frame.

RDT: (0011) Random Data Transmitted:

Random data can be transmitted onto the line continously. B1, B2 and D channel transparency between the digital interface and the line is enabled.

When auto-mode is selected, two test inputs (TEST1, TEST2) are provided allowing the same test functions as described above but without the need of a microcontroller. See Table 6 for Test pins biasing.

Table 6: Test Pins

TEST1	TEST2	FUNCTIONS
1	1	Normal operation
1	0	Send Single Pulse ± 1
0	1	Random Data Transmitted
0	0	Send Single Pulse ± 3

TURNING ON AND OFF THE DEVICE

STLC5411 contains an automatic sequencer for the complete control of the start-up activation sequences. Interactions with an external control unit requires only Activate Request and Deactivate Request commands, with the option of inserting break-points in the sequence for additional external control allowing for instance easy building of a repetor application. Automatic control of act, uoa/sai and dea bits in the M4 bit positions is provided, along with the specified 40 ms, 480 ms and 15 s timers used during the sequencing.

Except the Power up and Power down control that is slightly different, the Activation/Deactivation procedures are identical in GCI and Microwire/DSI modes. Same command codes or indication codes are used. In Microwire and GCI mode, activation control is done by writing in the Activation Control Register TXACT and by reading the Activation Indication Register RXACT. For TXACT and RXACT access, MICROWIRE port is used in MICROWIRE mode and C/I channel (or MONITOR channel depending of CID bit in CR2 register) is used in GCI mode.
In MICROWIRE mode, a primitive indication generates first an interrupt requesting an action from the Microprocessor, in GCI mode the primitive Indication is directly transmitted via C/I (or MONITOR channel).

Power on initialization

Following the initial application of power, STLC5411 enters the power down deactivated state in MICROWIRE mode or in GCI mode depending on the polarization of the MW input.
All the internal circuits including the master oscillator are inactive and in a low power state except for the 10 kHz Tone signal detector. The line outputs LO+/LO- are low impedance and all digital outputs are high impedance. All programmable registers and the activation controller are reset to their default value.

GCI configuration is defined by means of the configuration pins M0, CONF1 and CONF2 when Power supply is turned on.
For LT and NT1-2 equipments, GCI configuration should be completed by means of Control Register Programming. See Table 1 for configuration pins bias.

Line activation request

When UID is in the power down state and a 10kHz tone TN or TL is detected from the line. $\overline{\text{LSD}}$ and $\overline{\text{INT}}$ (MICROWIRE/DSI only) open drain outputs are forced to zero.

In NT configuration , code LSD (0000) is loaded in the activation indication register RXACT.

In LT configuration, code AP (1000) is loaded in the activation indication register RXACT.

In Microwire/DSI these indications are sent onto CO at the following access even if the UID is still in power down mode.

In GCI these indications are sent onto the C/I channel as soon as GCI clocks are available.

$\overline{\text{LSD}}$ open drain output is set back in the high impedance state as soon as the UID is powered up.

$\overline{\text{INT}}$ open drain output is set back in the high impedance state when $\overline{\text{CS}}$ input is detected at zero.

Depending of the ACTAUT and PUPAUT bits in CR6 register, UID can powered up itself, also automatically to start the activation.
For all auto mode configurations, on 10KHz tone reception, power up and activation procedure are full automatic, but in NT1 auto, UID waits the uoa bit from the line before to provide (or not) the cloks and primitives to the S device.

Power up control

Microwire/DSI: control instruction PUP in ACT

register is required to power up the UID.

GCI: when GCI "NT master of the clocks"configuration is selected, UID provides the GCI clocks needed for control channel transfer; PUP control instruction is provided to the UID by pulling low the Bx data input; STLC5411 then reacts sending GCI clocks. It is possible to operate an automatic power up of the UID when a wake up tone is detected from the line by connecting the $\overline{LSD}$ output directly to the Bx input.

GCI: when NT1-2 or LT configuration is selected (M0 = 0), the UID is powered up after configuration setting by the PUP code (0000) on C/I Channel.

Power down control

A control instruction PDN in ACT register is required to power down the device after a period of activity. PDN forces directly the device to the low power state without sequencing through any of the de-activation states. It should therefore only be used after the UID has been put in the line deactivated state. PDN has no influence on the content of the internal registers, but immediately stops the output clocks when UID is in master mode and in µW/DSI mode.

In GCI mode, UID send first two times code DI(1111) on C/I channel before powering down at the end of the assigned GCI channel.

The DI code purpose is similar to PDN code but power down state is entered only when the line is entirely deactivated (state H1 or J1). The DI command is recommended in GCI mode and in µW/DSI mode.

Power up state

Power up transition enables all analog and digital circuitry, starts the crystal oscillator and internal clocks. The $\overline{LSD}$ output is in the high impedance state even if a tone is detected from the line. As for PDN, PUP has no influence on the content of the internal registers

Power down state

Following a period of activity in the power up state, the power down state may be re-entered as described above. Configuration Registers remain in their current state. PDN and DI have no influence on the content of the internal registers: it is then possible, for instance, after a normal deactivation procedure followed by a power down command, to power up again the device in order to operate directly a Warm Start procedure.

ACTIVATION/DEACTIVATION SEQUENCING

Activation/deactivation signals onto the line are in accordance with the activation/deactivation state matrix given in Appendix A.

CASE OF RESTRICTED ACTIVATION

The standard specifies a mode where the U interface can be turned on without the need to activate the S/T interface provided this function is supported at both ends of the loop. In this condition Maintenance channel is available, typically for setting loop-backs in the NT for error rate testing and other diagnostics.

When this mode is enabled, bit M47 on the line in LT to NT direction becomes the uoa bit. Setting UAR activation command in the LT chip will set uoa bit equal zero on the line. Detection of uoa bit equal zero by the NT will inhibit activation of the S/T interface. This results in SN3 signal in the NT to LT direction, which causes generation of UAI indication by the LT U device when superframe synchronized.

If during restricted activation operation, a TE starts to try activate the S/T interface by sending info 1, the NT can pass this request to the LT via M47 bit, the sai bit. This bit is set equal one by writing AR command to the Activation Control Register. sai bit received equal one causes generation of an AP indication by the LT U device.

RESET OF ACTIVATION/DEACTIVATION STATE MACHINE

When the device is either powered-up or down, a control instruction RES resets the activation controller ready for a cold start. That feature can be used if the far-end equipment fails to warm start, for example if the line card or NT has been replaced or if in a regenerator, the loss of synchronisation of the second section imply the reset of the first section for a further cold start. The configuration registers remain in their selected value.

HARDWARE RESET

When GCI configuration is selected, pin 26 acts as a logical hardware Reset. The device is entirely reset including activation/deactivation state machine and configuration registers. Configuration pins bias excluding MW define the eventual new configuration. Pin MW must be maintained at the 0 Volt for GCI configuration setting.

It is possible to operate a similar "complete reset" of UID by setting high bit RST in the RXOH command register. In this last case the Control interface remains enabled.

QUIET MODE

It is possible to force the device in a quiet mode in which UID does not react to any line wake-up tone; LSD pin will remain high. There are two

ways to enter quiet mode: QM bit in CR6 register and QM primitive command to write in TXACT register; in this last case, any further primitive will clear quiet mode.

AUTOMODE

For all auto mode configurations, AIS pin allows a choice of line interface: 27 or 15mh for the transformer and resistors line or device side.

In NT1, the activation/deactivation state machine and the automatic power-up / power-down capabilities of the UID provide for a direct connection through GCI between UID and SID-GCI (ST 5421) without the need of an extra microcontroller (see figure 13b). LSD- pin of SID-GCI must be connected together to the Bx input pin of UID to ensure autonomous power-up/down control. Activation/Deactivation commands and indications are transferred from one device to the other by means of the C/I channel. Maintenance functions are automatically processed in UID. Therefore, there is not transfer of messages on the Monitor channel between UID and SID-GCI. Please note that the 2B+D loop-back request at the S interface is provided using the C/I channel code ARL and that there is not automatic processing of S and Q messages in SID-GCI.

In Repetor, the same advantages provide for a direct connection through GCI between both UID without the need of an extra microcontroller (see figure 13c). As for NT1, C/I channel transfers activation/deactivation commands and indications. Maintenance functions are automatically processed in UIDs, needing the transfer of eoc messages, overhead bits and CRC fault detections. This is performed autonomously on the Monitor channel by sending when required messages in a regular format as already described.EOC messages are transmitted according to Table 5; overhead bits in the M4 channel excluding (act, dea, uoa and sai) transferred transparently; spare overhead bits in M5 or M6 bit positions are also transferred transparently; febe and nebe bits are transmitted according to Figure10.

COMMAND INDICATION (C/I) CODES

Activation, deactivation and some special test functions can be initiated by the system by writing in TXACT register. Any status change of the on-chip state machine is indicated to the system by the UID by setting a new code in the RXACT register. When GCI is selected, TXACT and RXACT registers are normally associated with the C/I channel (it is possible to associate them with the MONITOR channel thank to the CID bit in CR2 register). All commands and indications are coded on four bits: C1, C2, C3, C4. Codes are listed in Table 7. For each mode, a list of recognized commands and generated indications is given. Hereafter, you have a detailed description of the codes depending on mode selected.

NT mode: Command

0000 (PUP): Power Up
When in the power down state, PUP command powers up the device ready for a cold or a warm start. When GCI is selected with clocks as outputs, PUP command is replaced by pulling low Bx input pin.

0001 (RES): Reset
RES command resets UID ready for a cold start. Configuration registers are not changed. RES can be operated when the device is either powered up or down.

If RES command is applied when the line is not fully deactivated, UID properly ends the activation before to come back in H1 state; In this case DP or EIU indication is returned (Auto mode configuration or not respectively).

0010 (SP1): Send Single Pulse +1 and -1
SP1 test command forces UID to send +1, -1, pulses to the line, one pulse per frame.

0011 (RDT): Random Data Transmitted
RDT test command forces UID to send data with random equiprobable levels at 80 kbaud.

0100 (EIS): Error Indicate S Interface
EIS command reports on the U line, a default on the S interface.

0101 (PDN): Power Down
PDN command forces UID to power down state. It should normally be used after UID has been set in a known deactivated state, e.g. in an NT after a DI status indication has been reported. In GCI, C/I indication (DI) is sent twice on Br output before UID powers down.

0110 (UAI): U interface Activation Indicate
UAI command is significant only when RR bit is set equal one in CR2 register or if NT-RR-AUTO auto-mode is selected. After the receiver has been super-frame synchronized, UAI command allows UID to send SN3 signal to the line.

0111 (QM): Quiet Mode
In this mode, UID does not react to any line status change. UID can be powered up or down and ready for a cold start or a warm start. All configuration registers and .coefficients remain unchanged. Quiet Mode is disabled by any other command.
Note: Inside UID, an logical or is implemented with this QM primitive and the QM bit in CR6 register.

1000 (AR): Activation Request
Beeing in the Power Up and deactivated state

Table 7a: RXACT (indication) and TXACT (command) codes

	CODES				NT (GCI or MW, NON AUTO-MODE)		LT (GCI or MW, NON AUTO-MODE)	
	C1	C2	C3	C4	RXACT (indications)	TXACT (commands)	RXACT (indications)	TXACT (commands)
0	0	0	0	0	DP/LSD	PUP (1)	–	PUP/DR
1	0	0	0	1	EIU	RES	EIU	RES
2	0	0	1	0	–	SP1	–	SP1
3	0	0	1	1	–	RDT	–	RDT
4	0	1	0	0	EIS	EIS	EIS	FA0
5	0	1	0	1	–	PDN	–	PDN
6	0	1	1	0	–	–	UAI	UAR
7	0	1	1	1	–	QM	–	QM
8	1	0	0	0	AP	AR	AP	AR
9	1	0	0	1	–	–	–	–
A	1	0	1	0	–	–	–	ARL
B	1	0	1	1	–	SP3	–	SP3
C	1	1	0	0	AI	AI	AI	AI
D	1	1	0	1	–	–	–	–
E	1	1	1	0	–	AIL	–	–
F	1	1	1	1	DI	DI	DI	DI

Note:
(1) ONLY IN SLAVE MODE IN MASTER. MODE, SET BXpin TO '0' TO HAVE THE SAME EFFECT THAN PUP.

	CODES				NTRR (GCI or MW, NON AUTO-MODE)		LTRR (GCI or MW, NON AUTO-MODE)	
	C1	C2	C3	C4	RXACT (indications)	TXACT (commands)	RXACT (indications)	TXACT (commands)
0	0	0	0	0	DP/LSD	PUP (1)	–	PUP/DR
1	0	0	0	1	EIU	RES	EIU	RES
2	0	0	1	0	–	SP1	–	SP1
3	0	0	1	1	–	RDT	–	RDT
4	0	1	0	0	EIS	EIS	EIS	FA0
5	0	1	0	1	–	PDN	–	PDN
6	0	1	1	0	UAP	UAI	UAI	UAR
7	0	1	1	1	–	QM	–	QM
8	1	0	0	0	AP	AR	AP	AR
9	1	0	0	1	–	–	–	–
A	1	0	1	0	–	–	–	ARL
B	1	0	1	1	–	SP3	–	SP3
C	1	1	0	0	AI	AI	AI	AI
D	1	1	0	1	–	–	–	–
E	1	1	1	0	–	–	–	–
F	1	1	1	1	DI	DI	DI	DI

(1) ONLY IN SLAVE MODE.

Table 7b: RXACT (indication) and TXACT (command) codes.

	CODES	NT1 (GCI ONLY, AUTO-MODE)	
	C1 C2 C3 C4	**RXACT** (indications)	**TXACT** (commands)
0	0 0 0 0	DP/LSD	(1)
1	0 0 0 1	–	RES
2	0 0 1 0	–	SP1
3	0 0 1 1	–	RDT
4	0 1 0 0	EIS	EIS
5	0 1 0 1	–	PDN
6	0 1 1 0	–	–
7	0 1 1 1	–	QM
8	1 0 0 0	AP	AR
9	1 0 0 1	–	–
A	1 0 1 0	ARL	–
B	1 0 1 1	–	SP3
C	1 1 0 0	AI	AI
D	1 1 0 1	–	–
E	1 1 1 0	–	AIL
F	1 1 1 1	DI	DI

(1) SET Bx PIN TO '0' IS EQUIVALENT TO A PUP COMMANDE

	CODES	NTRR (GCI ONLY, AUTO-MODE)		LTRR (GCI ONLY, AUTO-MODE)	
	C1 C2 C3 C4	**RXACT** (indications)	**TXACT** (commands)	**RXACT** (indications)	**TXACT** (commands)
0	0 0 0 0	DP/LSD	(1)	(2)	PUP/DR
1	0 0 0 1	EIU	RES	EIU	RES
2	0 0 1 0	–	–	–	–
3	0 0 1 1	–	–	–	–
4	0 1 0 0	EIS	EIS	EIS	FA0
5	0 1 0 1	–	–	–	–
6	0 1 1 0	UAP	UAI	UAI	UAR
7	0 1 1 1	–	–	–	–
8	1 0 0 0	AP	AR	AP	AR
9	1 0 0 1	–	–	–	–
A	1 0 1 0	ARL	–	–	ARL
B	1 0 1 1	–	–	–	–
C	1 1 0 0	AI	AI	AI	AI
D	1 1 0 1	–	–	–	–
E	1 1 1 0	–	–	–	–
F	1 1 1 1	DI	DI	DI	DI

(1) SET Bx PIN TO '0' IS EQUIVALENT TO A PUP COMMANDE

(H1), AR instruction forces UID through the appropriate sequence to activate the line by sending TN followed by SN1. Beeing in the U-only-active state (H8A), AR command forces the sai bit equal 1 to the line. Is intended to transfer to the network an activation attempt at the S/T interface.

1011 (SP3): Send Single Pulse +3 and -3
SP3 test command forces UID to send +3, -3 pulses to the line, one pulse per frame.

1100 (AI): Activation Indicate
AI command forces act bit equal one in SN3 signal transmitted to the line. Is intended to reflect an activate state at the S/T interface.

1110 (AIL): Activation Indicate Loopback
Identical to AI command. Ensure direct compatibility with status indications of SID-GCI.

1111 (DI): Deactivation Indicate
The DI command allows the UID to automatically enter the power down state if the line is deactivated. DI command has no effect as long as the line is not deactivated (DI status indication reported).

NT mode: Status indication

0000 (DP/LSD): Deactivation pending / Line signal detected
When in the deactivated state (H1) either powered up or down, LSD status indication is reported if TN wake-up tone is detected except if NT1 AUTO is selected; in this configuration, UID must check uoa bit before to send (or not) LSD. When in the superframe-synchronized states, DP status indication reports that the dea bit has been received equal zero from the line. UID enters in the receive reset state. When NT1-AUTO mode is selected, DP status indication is reported also when a transmission error has been detected on the loop. This is intended to ensure immediate deactivation of the S/T interface.

0001 (EIU): Error Indication User
EIU status indication is reported to acknowledge RES command. UID is deactivated, ready for a cold start. When NT1-AUTO is selected, EIU is replaced by DP.

0010 (EIL): Error Indication Loss of signal
EIL status indication reports a Loss of signal for more than 480ms on the line. When NT1-AUTO is selected, EIL is replaced by (DP).

0011 (EIS): Error Indication Loss of Sync
EIS status indication reports a Loss of synchronization for more than 480ms on the line. When NT1-AUTO is selected, EIS is replaced by (DP). When NT-RR-AUTO is selected, EIS is replaced by RES.

0100 (EI): Error Indication
EI status indication reports that act bit has been detected equal zero.

0101 (EIT): Error Indication Expiry of Timer 4
EIT status indication reports that an expiry of Timer 4 interrupt has reset UID ready for a cold start. When NT1-AUTO is selected, EIT is replaced by (DP). When NT-RR-AUTO is selected, EIT is replaced by RES.

0110 (UAP): U interface Activation pending
Is significant only when RR bit in CR2 has been set equal one or if NT-RR-AUTO mode is selected. UAP reports that the receiver is superframe synchronized with uoa bit received equal zero.

1000 (AP): Activation Pending
AP reports that the receiver is superframe synchronized with uoa bit received equal one .

1010 (ARL): Activation Request Loopback
Is significant only when NT1-AUTO or NT-RR-AUTO mode is selected. ARL reports that an eoc message has been received requiring to operate a local 2B+D loopback. When connected to SID-GCI in a NT1 or to UID in LT-RR-AUTO mode in a regenerator, 2B+D loopback command is therefore automatically provided.

1100 (AI): Activation Indication
AI reports that UID is superframe synchronized with act and uoa bits received equal one.

1111 (DI): Deactivation Indication
DI reports that UID has entered the deactivated state (H1).

LT mode: Command

0000 (PUP/DR): Power Up / Deactivation Request When in the power down state, PUP command powers up the device ready for a cold or a warm start. When in one of the superframe synchronized states, DR command forces dea bit on the line equal zero for four consecutive superframes before ceasing transmission.

0001 (RES): Reset
RES command resets UID ready for a cold start. Configuration registers are not changed. RES can be operated when the device is either powered up or down. If RES command is applied when the line is not fully deactivated, UID returns EIU indication and goes in J1 state (Receive Reset).
If RES command is applied when the line is not fully deactivated, UID properly ends the activation before to come back in J1 state; in this case EIU indication is returned.

0010 (SP1): Send Single Pulse +1 and-1
SP1 test command forces UID to send +1, -1, pulses to the line, one pulse per frame.

0011 (RDT): Random Data Transmitted
RDT test command forces UID to send data with random equiprobable levels at 80 kbaud.

0100 (FA0): Force act bit to Zero
FA0 command forces the act bit to 0 in the SL3 signal transmitted to the line. Is intended to reflect a transmission failure detected on the network side of the loop relative to UID.

0101 (PDN): Power Down
PDN command forces UID to power down state. It should normally be used after UID has been set in a known deactivated state, e.g. in an LT after a DI status indication has been reported. In GCI, C/I indication DI is sent twice on Br output before UID powers down.

0110 (UAR): U-interface-only Activation Request
Being Power Up and deactivated , UAR command forces UID through the appropriate sequence to activate the loop without activating the S/T interface. SL2/SL3 signal is sent with uoa bit set to zero. With the line already active, UAR command forces bit uoa equal zero: this is intended to deactivate the S/T interface.

0111 (QM): Quiet Mode
This command has the same effect as in NT mode.

1000 (AR): Activation Request
Being Power Up and deactivated, AR instruction forces UID through the appropriate sequence to activate the line by sending TL followed by SL1. SL2/SL3 signal is sent with uoa bit equal one.
Beeing in the U-only-active states, AR command forces the uoa bit equal 1 to the line. Is intended to activate the S/T interface.

1010 (ARL): Activation Request with Loopback
ARL test command forces UID through the appropriate sequence to activate with the complete transmit data stream looped-back to the receiver. When this loop-back is disabled by DR command, UID is ready to operate a warm start if a new ARL command is issued.

1011 (SP3): Send Single Pulse +3, -3
SP3 test command forces UID to send +3, -3 pulses to the line, one pulse per frame.

1100 (AI): Activation Indicate
AI is an optional command recognized only when BP2 bit in CR2 register is set equal one or LT-RR-AUTO mode is selected. Beeing in the superframe-synchronized state with act bit received from the line equal one, AI command allows UID to send act bit equal one to the line.

1111 (DI): Deactivation Indicate
The DI command allows the UID to automatically enter the power down state if the line is deactivated. DI command has no effect as long as the line is not deactivated (DI status indication reported).

LT mode: Status indication

0001 (EIU): Error Indication Interface U
EIU status indication reports an error at U interface. It can be a 'loss at signal' a 'loss of sync','expiry of Timer 4 lias reset UID for cold-start' and 'UID put in receive reset state by RES command'.

0100 (EIS): Error Indication
EIS status indication reports that act bit has been detected equal zero.

0110 (UAI): U interface Activation Indication
UAI reports that the line is superframe synchronized.

1000 (AP): Activation Pending
Being in one of the deactivated states, AP reports that a wake up tone has been detected from the line. Beeing in the U-only-activated state, AP reports that sai bit has been detected equal one from the line. Is intended to reflect an activation attempt at the S/T interface.

1100 (AI): Activation Indication
AI reports that UID is superframe synchronized with act bit received equal one. TE side of the loop relative to the UID is active

1111 (DI): Deactivation Indication DI reports that UID has entered the deactivated state (J1).

B1, B2 and D channels transparency
UID is able to control automatically transparency of B1, B2 and D channels. Nevertheless, when ETC bit in CR2 register is set equal 1, transparency is forced as soon as the line is synchronized.
It is also possible to control each data channel B1, B2, D enabling at the DSI/GCI interface independently by means of bits EB1, EB2 and ED in CR4 register; Set equal 1, B1, B2 or D channel on the DSI/GCI interface is enabled; In this case, out of the transparency state (s), ones are forced on thee relevant time slot of the DSI/GCI, and ones or zeros are transmitted on the line conforming T1E1 recommendations. Set equal 0, relevant time slot on DSI/GCI is always in high impedance state and ones or zeros are transmitted on the line. In this last case, as soon as transparency is enabled, ones are transmitted to the line.

When RDT test command is applied, transparency on 2B+D is forced. This intend to permit the user, if required, to send a random sequence of bits to the line. Please note that the on-chip scrambler normally ensures transmission of equiprobable levels to the line, even if logical one only is provided to the DSI/GCI system interface.

INTERNAL REGISTERS DESCRIPTION.

Here following a detailed description of STLC5411 internal registers.

Internal registers can be accessed:

a) In GCI mode, according to the monitor channel exchange rules. For RXACT and TXACT also through C/I channel.

b) in µW/DSI mode, using the MICROWIRE interface according to the rules described in section "µW control interface".

Table 8 gives the list of all the STLC5411 internal registers can be used in MICROWIRE mode.
Table 9 gives the list of all the STLC5411 internal registers can be used in GCI mode.
Registers are grouped by types and address ar-

eas:

area 00/0FH: NOP operations.

area 10/1FH: the test registers: reserved.

area 20/2FH: the configuration registers.
OPR CR1 CR2 CR3 CR4 CR5 CR6
Read Write access. CR5 only usefull in GCI mode

area 30/3FH: the B1 B2 D time slot registers.
TXB1 TXB2 RXB1 RXB2 TXD RXD STATUS
Read Write access except STATUS: Read only.
Usefull only in MW mode except STATUS: MW & GCI modes.

area 40/4FH: the transmit and receive registers (except EOC).
TXM4 RXM4 TXM56 RXM56 TXACT RXACT BEC1 BEC2 ECT1 ECT2 RXOH
Read Write access for the transmit registers:
TXM4 TXM56 TXACT
Read access only for the receive registers:
RXM4 RXM56 RXACT
Read Write access for the control registers:
ECT1 ECT2
Read access only for the error registers:
BEC1 BEC2
Write access only for the command registers:
RXOH

area 5x to 9x: for 12 bits registers.
5x: to write TXEOC register, to read RXEOC register.
6x: to read TXEOC register.
7x: reserved
8x & 9x: to read IDR register.

area Ax to Ex: reserved.

area Fx: reserved except FF address: special register MWPS.

Overhead bits programmable register (OPR)
After reset: 1EH

CIE	EIE	FIE	OB1	OB0	OC1	OC0	C2E

CIE Near-End CRC Interrupt Enable:

CIE = 1: the RXM56 register is queued in the interrupt register stack with nebe bit set to zero each time the CRC result is not identical to the corresponding CRC received from the line.

CIE = 0: no interrupt is issued but the error detection remains active for instance for on chip error counting.

EIE Error counting Interrupt Enable:

EIE = 1: an interrupt is provided for the counter when the threshold (ETC1 or ETC2) is reached.

EIE= 0: no interrupt is issued. It is feasible to read the counters even if no relevant interrupt has been provided.

FIE FEBE Interrupt Enable:

FIE = 1: the RXM56 register is queued into the interrupt register stack each time the febe bit is received at zero in a superframe.

FIE = 0: no interrupt is issued but the receive febe bit remains active for on chip error counting.

OB1, OB0 Overhead Bit processing:

select how each spare overhead bit received from the line is validated and transmitted to the system. RXM4 and RXM56 registers are independently provided onto the system interface as for the eoc channel. Each spare overhead bit is validated independently from the others.

OB1	OB0	
0	0	each super frame, an interrupt is generated for the RXM4 or the RXM56 register. Spare bits are transparently transmited to the system.
0	1	an interrupt is set at each new spare overhead bit(s) received.
1	0	an interrupt is set at each new spare overhead bit(s) received and confirmed once. (two times identical).
1	1	an interrupt is set at each new spare overhead bit(s) received and confirmed twice. (three times identical).

If new bits are received at the same time in M4

and M56, both registers RXM4 and RXM56 are queued in the interrupt register stack.
Bits act, dea, uoa, sai are dedicated to the activation procedure. Validation is always done in accordance with the ANSI rule: validation at each new activation bit received and confirmed twice independently from the above rules. These bits are taken into account directly by the activation decoder. An interrupt is not generated for the RXM4 Register when one of these bits changes, but they are provided for test to the RXM4 Register.

OC1, OC0 eoc channel processing:

select how a received eoc message is validated and transmitted to the system.

OC1	OC0	
0	0	every half a super frame, an interrupt is generated for the RXEOC register. eoc channel is transparently transmitted to the system.
0	1	an interrupt is set at each new eoc message received.
1	0	an interrupt is set at each new eoc message received and confirmed once. (two times identical)
1	1	an interrupt is set at each new eoc message received and confirmed twice. (three times identical).

C2E Counter 2 enable:

C2E = 0: Only counter BEC1 is used for both febe and nebe counting.

C2E = 1: Counter BEC1 is used for nebe. Counter BEC2 is used for febe.

Configuration register 1 (CR1)
After reset:
µW mode 00H
GCI: MO = 0 (LT/NT12) = C0H
GCI: MO = 1 (NT/TE) = D2H

FF1	FF0	CK2	CK1	CK0	DDM	CMS	BEX

FF1, FF0 Frame Format Selection: (µW/DSI only)
Refer to fig. 2 and 3.

FF1	FF2	
0	0	Format 1
0	1	Format 2
1	0	Format 3
1	1	Format 4

CK0-CK2 Digital Interface Clock select: (mW/DSI only)
CK0-CK2 bits select the BCLK output frequency when DSI clocks are outputs.

CK2	CK1	CK0	BCLK frequency:
0	0	0	256KHz
0	0	1	512KHz
0	1	0	1536KHz
0	1	1	2048KHz
1	0	0	2560KHz

DDM Delayed Data Mode select:(µW/DSI only)
Two different phase-relations may be established between the Frame Sync signals and the first bit of the frame on the Digital Interface:

DDM = 0: Non delayed data mode The first bit of the frame begins nominally coincident with the rising edge of FSA/B.

DDM = 1: delayed data mode: FSA/B input must be set high at least a half cycle of BCLK earlier the frame beginning.

CMS Clocks Master Select:(µW/DSI only)

CMS = 0: BCLK, FSA and FSB are inputs; BCLK can have in Format 1, 2 and 3 value between 256KHz to 4096KHz, value in Format 4: 512KHz to 6176KHz.

CMS = 1: BCLK, FSA and FSB are outputs; FSA is a 8 kHz clock pulse indicating the frame beginning, FSB is a 8 kHz clock pulse is indicating the second 8 bits wide time-slot. BCLK is a bit clock signal whose frequency bits CK2-CK0.

BEX B channels Exchange:

BEX = 0: B1 and B2 Tx/Rx channels are associated with TXB1/RXB1 and TXB2/RXB2 registers respectively.

BEX = 1: B1 and B2 channels are exchanged.

Configuration register 2 (CR2)
After reset:
µW mode 00H
GCI: MO = 0 (LT/NT12) = 00H
GCI: MO = 1 (NT/TE) = 80H

µW (LT,NT):

SFS	NTS	DMO	DEN	ETC	BP1 EIF	BP2 BFH9D	RR

GCI (LT,NT):

SFS	NTS	T24D	CID	ETC	BP1 EIF	BP2 BFH9D	RR

SFS Super Frame Synchronization Select:
Significant in LT mode only.

SFS = 0: SFSx is an input that synchronizes the transmit superframe.

SFS = 1: SFSx is an output indicating the Transmit Superframe. In NT mode SFSx is always an output.

NTS LT / NT mode Select.

NTS = 0: LT mode selected

NTS = 1: NT mode selected

DMO D channel Transfer mode Select.(µW/DSI only)
Significant only when DEN=1.

DMO = 1: D channel data is shifted in and out on Dx and Dr pins in continuous mode at 16 kbit/s on the falling and rising edges of DCLK respectively.

DMO = 0: D channel data is shifted in and out on Dx and Dr pins in a TDM mode at the BCLK frequency on the falling and rising edges of BCLK respectively when the assigned time-slots are active.

T24D: 24ms timer desable (GCI only).

T24D = 1: The timer watches at the exchange on MONITOR channel every time the UID sends new byte. If it expires before pre-acknoledgement, an abort message is generated; In this last case, the aborted message is lost.

T24D = 0: The timer is desable. This means for instance that UID may wait an pre-acknoledgement for ever.

DEN D channel port Enable. (µW/DSI only)

DEN = 0: D channel port disabled. D bits are transferred on Br and Bx; Multiplexed mode is selected automatically.

DEN = 1: D channel port (DX, DR, and DCLK when DMO bit equal 1) is selected. D bits are transferred on Dr and Dx in a mode depending on DMO bit setting.

CID: C/I channel desable (GCI only).

CID = 0: TXACT and RXACT registers only accessible via the C/I channel.
Others registers only accessible via MONITOR channel.

CID = 1: All registers only accessible via the MONITOR channel.

ETC 2B+D Data Extended Transparency channel.

ETC = 1: 2B+D channel transparency is enabled as soon as the line is superframe synchronized.

ETC = 0: 2B+D channel transparency is under control of the on-chip state machine: act bit equal one both directions.

BP1 Break Point 1 during activation(significative only when NTS = 0: LT mode) .

BP1 = 1: During an activation attempt from the loop, (before SL2 sending) UID waits for an AR command to pursue activation. It is recommended to set BP1 equal 1 for repetor application.

BP1 = 0: The activation procedure is automatically processed without the need of an AR command.

EIF Error Indication Filter.
Significant in NT mode only

EIF = 0: act bit is set to zero in the transmit superframe in case of EI command, even if EI is sent sporadically.

EIF = 1: act bit may be not set to zero in the transmit superframe in case of EI command with a duration of less than 36ms.

BP2 Break Point 2 during activation. Significant only when NTS=0 (LT selected)

BP2 = 1: During a full activation procedure, UID receiving act bit set to one in the received SN3 signal, UID waits for an AI command to send act bit equal one in SL3 signal. It is recommended to set BP2 equal 1 for repetor application.

BP2 = 0: The activation procedure described above is automatically processed without the need of an AI command.

BFH9D: Back from H9 disabled. (Significant in NT mode only)

BFH9D = 0: UID is in H9 state (pending deactivation) after reception of dea bit = 0. It is waiting a loss of signal to return in H1 state via H12.

BFH9D = 1: UID is H9 state (pending deactivation) after reception of dea bit = 0. It is waiting a loss of signal to return in H1 state via H12, or dea bit = 1; In this last case UID returns in the previous state.

RR Repetor mode.

RR = 0: UID activation/deactivation complies with the standard requirements for NT1 or LT equipment depending on NTS bit select. See state matrix for the detailed behaviour of UID.

RR = 1: UID activation/deactivation complies with the requirements for repetor equipment. "LT" or "NT" behaviour is selected by means of bit NTS. BP1 and BP2 break-points should be set equal one too. See state matrix for the detailed behaviour of UID in this mode of operation.

Configuration register 3 (CR3)
After reset: 00H

LB1	LB2	LBD	DB1	DB2	DBD	TLB	T15D

LB1, LB2, LBD Line side Loopback select.

When set high they turn each individual B1, B2, or D channel from the Line receive input to the Line transmit output. They may be set separately or together. The loopback is operated close to Bx and Br (or Dx and Dr if the D port is selected). These loop backs ensures channels integrity.

DB1, DB2, DBD Digital side Channel Loopback select.

When set high they turn each individual B1, B2, or D channel from the Digital Interface receive input to the Digital Interface transmit output. They may be set separately or together. The loopback is operated close to Bx and Br (or Dx and Dr if D port selected). These loop backs ensures channels integrity whatever the selected format or assigned channels time slot.

TLB Transparent Loopback select

TLB = 0: Digital loopbacks are non transparent. When line side loopback is set, data transmitted onto the digital interface is forced to one. When digital side loopback is set, data transmitted onto the line is forced to 1 in NT mode and to 0 in LT mode.

TLB = 1: 2B+D is transparently transferred through the UID.

T15D Timer 15 second disabled

T15D = 0: On-chip 15 second timer (timer 4 or 5 of ANSI standard) is enabled and ensure full reset of the activation procedure in case of non synchronization of the line within 15 second.

T15D = 1: On-chip 15 second timer is disabled. This means for instance that UID may attempt to synchronize for ever.

Configuration register 4 (CR4)
After reset: E0H

EB1	EB2	ED	FFIT	ESFr	CTLIO	MOB	CTC

EB1 B1 channel Enabling

EB1 = 1: Selected B1 channel time-slot on the DSI/GCI interface is enabled. Note that transparency of B1 channel remains under control of the activation state machine and the ETC bit in CR2.

EB1 = 0: Selected B1 channel time-slot on the DSI/GCI interface is disabled: Br output remains in high impedance state and data on Bx input is ignored. Ones (NT) or zeroes (LT) are transmitted on the line.

EB2 B2 channel Enabling Identical to EB1 bit but for B2 channel.

ED D channel enabling identical to EB1 but for D channel on Bx/Br pin or DX/Dr pin depending on DEN bit in CR2 register.

FFIT FIFOs interrupt.

FFIT = 1: overflow or underflow of the TXFIFO and RXFIFO are reported in STATUS register. An interrupt is generated in MW mode, a MONITOR message is automatically sends in GCI mode.

FFIT = 0: No interrupt or message is generated when FIFOs overflow or underflow.

ESFr Enable SFSr on pin25

ESFr = 0: LSD open drain output is selected on pin 25.

ESFr = 1: SFSr output is selected on pin 25.

CTLIO Control IO (significant in GCI mode only)

CTLIO = 1: The input pins configurated via CR5 register generate a message on every change even if the UID is powered down in master mode; that is to say UID is able to wake up itself, to provide the clocks, to sends the message. After that UID is automatically powered down except if a PUP command is sent to it.

CTLIO = 0: In master mode and powered down, the UID does not react to a input pin change.

MOB Mask Overhead Bits.

MOB = 0: No Mask on overhead bit interrupts.

MOB = 1: All interrupts issued from RXM4, RXM56 RXEOC and CR5 are masked. It is still possible to read these registers via RXOH.

CTC Corrupted Transmit CRC Control

CTC = 0: Allows the normal calculation of the CRC for the transmitted data to the line.

CTC = 1: The CRC result transmitted to the line in the next Superframe is inverted. This ensure transmission of corrupted CRC as long as CTC equal 1.

Configuration Register 5 (CR5)
Significant in GCI only.

After reset: FFH

IO4	IO3	IO2	IO1	D4	D3	D2	D1

IO4, IO3, IO2, IO1 Input/Output select for I/O pins (14, 15, 16, 18)

IOi = 1: IOi pin is selected as an input. An on-chip pull up resistor ensures a stable logical 1 at power-on reset or if IOi pin is not connected to stable source.

IOi = 0: IOi pin is selected as an output. Each I/O pin can be selected independently from the others.

D4, D3, D2, D1 I/O pin logical level command/status.

D4, D3, D2, D1 bits are associated with IO4, IO3, IO2, IO1 pins respectively. When IOi pin is selected as an output, the associated Di bit can be written to control the logical level of the output; Di equals 1 commands a high level on IOi. When IOi pin is selected as an input, the associated Di bit indicates the status of the input; Di equals one indicates a high level on IOi. CR5 register is buffered in the interrupt stack each time a status change is detected on an input. It is also possible to read-back at any time CR5.

Configuration register 6 (CR6)

After reset: 0FH

T15E	ACTAUT	PUPAUT	QM	AIS	TFB0	RFS	LFS

T15E Timer 15 seconds extension

T15E = 0: The on chip T4 or T6 timer is done for the ANSI standard: 15 seconds.

T15E = 1: The on chip T4 or T5 timer is extended to 20 seconds.

Note: the T15D bit in CR3 register enables or desables the T4/T5 timer independently of theT15E bit.

ACTAUT: Activation Automatic

ACTAUT = 1: If UID is powered up, a 10KHz tone from the line starts the activation without need of extra commands (like AR), except when QM (Quiet mode) is enterred.

ACTAUT = 0 A detection of a 10KHz tone from the line does not start the activation: UID waits a primitive command (normaly AR).

PUPAUT PUP Automatic

PUPAUT = 1: If UID is powered up, a 10KHz tone from the line allows an automatic power up of the UID.

Notes if ACTAUT is set to 1, from a power down state a 10KHz tone automatically starts the activation.

PUPAUT = 0: A detection of a 10KHz tone from the line does not power up the device: UID waits a PUP primitive command.

QM Quiet mode.

QM = 1: has the same effect of the QM primitive command enterred in TXACT register. An or logic is done with the QM bit and the QM primitive. The goal of this bit is to allow a quiet mode for an UID in power down state in some applications.

QM = 0: no effect.

AIS Analog Interface Select.

AIS = 1: selects an analog interface using 27mh transformer.

AIS = 0: selects an analog interface using 15mh transformer

TFB0 Transmit febe equal 0

TFB0 = 0: A permanent febe bit = 0 is sent on the line as long as TFB0 = 0

TFB0 = 1: The febe bit sent on the line is normaly computed.

RFS Remote febe select.

Please report to the figure 10. RFS is usefull in report application to transfert or not the anomalies

second line section to the first line section and viceversa.

RFS = 1: Transfert anomalies second section first section and viceversa allowed.

RFS = 0: Transfert anomalies second section first section and viceversa not allowed.

LFS Local febe select.

Please report to the figure 10. LFS is usefull in report application to transfert or not the crc anomalies (nebe) of a line section to the febe bit of the same line section.

RFS = 0: The computing febe takes in account the local nebe.

RFS = 1: The computing febe does not take in account the local nebe.

Configuration register TXB1
Significant only when format 3 selected.
(µW/DSI Only)

After reset: 00H Time slot 0 selected.

-	-	B1X5	B1X4	B1X3	B1X2	B1X1	B1X0

B1X5-B1X0 Transmit B1 Time Slot Assignment

Those bits define the binary number of the transmit B1 channel time-slot on Bx input. Time slot are numbered from 0 to 63. The register content is taken into account at each frame beginning.

Configuration register RXB1
Significant only when format 3 selected.
(µW/DSI Only)

After reset: 00h Time slot 0 selected.

–	–	B1R5	B2R4	B2R3	B2R2	B2R1	B2R0

B1R5-B1R0 Receive B1 Time Slot Assignment

B1R5-B1R0 bits define the binary number of the receive B1 channel time-slot on BR output. Time slot are numbered from 0 to 63. The register content is taken into account at each frame beginning.

Configuration register TXB2
Significant only when format 3 selected.
(µW/DSI Only)

After reset: 01H Time slot 1 selected.

-	-	B2X5	B2X4	B2X3	B2X2	B2X1	B2X0

B2X5-B2X0 Transmit B2 Time Slot Assignment

Those bits define the binary number of the transmit B2 channel time-slot on Bx input. Time slots are numbered from 0 to 63. The register content is taken into account at each frame beginning.

Configuration register RXB2
Significant only when format 3 selected. (µW/DSI Only)
After reset: 01H Time slot 1 selected.

-	-	B2R5	B2R4	B2R3	B2R2	B2R1	B2R0

B2R5-B2R0 Receive B2 Time Slot Assignment

Those bits define the binary number of the receive B2 channel time-slot on BR output. Time slot are numbered from 0 to 63. The register content is taken into account at each frame beginning.

Configuration register TXD
After reset:
µW mode 08H (sub time slot 0, time slot 2 selected)
Significant only when format 3 is selected with the D channel selected in the multiplexed mode:

DX5	DX4	DX3	DX2	DX1	DX0	SX1	SX0

DX5-SX0 Transmit D channel Time Slot Assignment

DX5-DX0 and SX1-SX0 bits define the binary number of the transmit D channel time-slot. DX5-DX0 bits define the binary number of the 8 bits wide timeslot. Time slot are numbered from 0 to 63. Within this selected time slot, SX1,SX0 bits define the binary number of the 2 bits wide time-slot. Sub time-slots are numbered 0 to 3. The register content is taken into account at each frame beginning.

Configuration register RXD
After reset:
µW mode 08H (sub time slot 0, time slot 2 selected)
Significant only when format 3 is selected with the D channel selected in multiplexed mode.

DR5	DR4	DR3	DR3	DR2	DR1	SR1	SR0

DR5-SR0 Receive D channel Time Slot Assignment

DR5-DR0 and SR1-SR0 bits define the binary number of the receive D channel time-slot. DR5-DR0 bits define the binary number of the 8 bits wide timeslot. Time slot are numbered from 0 to 63. Within this selected time slot., SR1,SR0 bits define the binary number of the 2 bits wide time-slot. Sub time-slots are numbered 0 to 3. The register content is taken into account at each frame beginning.

Status Register (STATUS)

(Read only)

After reset: 85H

PWDN	X	X	X	RXFFU	RXFFO	TXFFU	TXFFO

PWDN Power down

PWDN = 1: UID is in power down state

PWDN = 0: UID is in power up state

RXFFU RX FIFO underflow

RXFFU = 1: The bits rate on Br pin is higher than the bits rate side line.

RXFFU = 0: The bits rate on Br is in accordance with the bits rate side line

RXFFO: RX FIFO overflow

RXFFO = 1: The bits rate on Br pin is lower than the bits rate side line.

RXFFO = 0: The bits rate on Br pin is in accordance with the bits rate side line.

TXFFU TX FIFO underflow

TXFFU = 1: The bits rate on Bx pin is lower than the bits rate side line.

TXFFU = 0: The bits rate on Bx pin is in accordance with the bits rate side line.

TXFFO Tx FIFO overflow

TXFFO = 1: The bits rate on Bx pin is higher than the bits rate side line.

TXFFO The bits rate on Bx pin is in accordance with the bits rate side line.

When one of these four bits is set to 1, Tx FIFO and/or Rx FIFO is re-adjusted and data is lost. Un interrupt or message is generated if FFIT bit in CR4 register is set to 1. It is always possible to read this register by writting STATUS bit = 1 in RXOH register.

Transmit M4 channel register (TXM4)

After reset: 7DH

-	m42x	m43x	m44x	m45x	m46x	-	m48x

When transmitting SL2/SL3 or SN3, the UID shall continuously send in the M4 channel field the register content to the line once per superframe. Register content is transmitted to the line at each superframe.

m41x, m42x in LT, m47x are activation bits. These bits are controlled directly by the on chip activation encoder-decoder. The corresponding bits in the TXM4 register are not significant.

m45x in NT mode is CS0 bit: this is normally 0 (UID performing warm start). Nevertheless, user can force CSO to 1 by setting m45x to 1.

When a read back is operated on TXM4, m41x, m42x in LT, m47x are indicating the current value of act, dea in LT and uoa/sai bits transmitted to the line.

Receive spare M4 overhead bits register (RXM4) (read only)

After reset: 75H

m41r	m42r	m43r	m44r	m45r	m46r	m47r	m48r

RXM4 Register is constituted of 8 bits. When the line is fully activated (super frame synchronized), STLC5411 extracts the M4 channel bits. m41 is the act bit; m42 in NT mode is the dea bit; in NT m47 is the uoa bit; in LT m47 is the sai bit. These bits are under the control of the activation sequencer. No interrupt cycle is provided for the RXM4 register when a change on one of the activation bits is detected; never the less, they are available in RXM4.

When one of the remaining received spare bits is validated following the criteria selected in the Configuration Register OPR, the RXM4 register content is queued in the interrupt register stack, if no mask overhead bits is set (see MOB bit in CR4 register). It is always possible to read this register by writting RXM4 bit = 1 in RXOH register.

Transmit M5 and M6 channels register (TXM56)

After reset: 1FH

-	-	-	m51x	m61x	m52x	febx	febx

m51x, m61x, m52x spare over-head bits are normally equal to 1. Default value can be changed by setting the respective bits. These bits are transmitted to the line in SL2/SL3 or SN3 signal.

febx Transmit febe bit control

The febe can be forced to 0 by writing 0 in one of febx if RFS bit in CR6 register is set to 1. The febe bit set to zero is sent once to the line in the following available superframe. After febe transmission, febx bit returns to 1; the two bits positions are identical and allow direct compatibility between UIDs set in auto-mode (repeter).

Note: the febx bits in TXM56 register are not the only way to force febe = 0 to the line.

First, the febx action is controlled by RFS bit in CR6 register.

Second, the nebe = 0 (local crc cmputing result) forces also febe = 0 to the line and this action is controlled by LFS bit in CR6 register.

Third, TFB0 = 0 in CR6 register forces permanentely febe = 0 to the line.

Receive M5 and M6 overhead bits register (RXM56) (read only)

After reset: 1FH

-	-	-	m51r	m61r	m52r	febr	nebr

When the line is fully activated (super frame synchronized), STLC5411 extracts the overhead bits. When one of the received spare bits m51, m61, m52 is validated following the criterias selected in the Configuration Register OPR. The RXM56 register content is queued in the interrupt register stack, if no mask overhead bits is set (see MOB bit in CR4 register). If the FIE bit in OPR register is set high, the RXM56 register content is queued in the interrupt register stack each time the febe bit is received equal zero with bit feb equal 0.
The CRC received from the far-end is compared at the end of the superframe with the CRC calculated by the UID during that superframe. If an error is detected, the febe bit in the transmit direction is forced equal zero in the next superframe. If the CIE bit in the OPR register is set high, the RXM56 register is queued in the interrupt register stack at each CRC error detected with bit neb equal zero. It is always possible to read this register by writing RXM56 bit = 1 in RXOH register.

Activation control register (TXACT)

After reset: 0FH

-	-	-	-	C4	C3	C2	C1

This register is constituted of four bits: (C1, C2, C3, C4). In GCI mode, this register is normaly addressed by means of the C/I channel, but it is possible to address it by means of the MONITOR channel (see CID bit in CR2 register).

Activation indication register (RXACT)

(read only)

After reset: 0FH

-	-	-	-	C4r	C3r	C2r	C1r

This Register is constituted of four bits: (C1r, C2r, C3r, C4r). At each activation status change, RXACT is queued in the interrupt register stack. In GCI mode, the C1-C4 bits are directly sent on the C/I channel or monitor channel depending on the CID bit in CR2 register. Activation Indication instructions are coded on 4 bits according to activation control description. It is always possible to read this register by writting RXACT bit = 1 in RXOH register.

Block Error counter 1 (BEC1)

(read only)

After reset: 00H

ec7	ec6	ec5	ec4	ec3	ec2	ec1	ec0

This Register indicates the binary value of the Block Error up-counter 1. Error are counted according to C2E bit setting in register OPR (nebe + febe or nebe only). When counter one reachs the threshold ECT1, BEC1 register is queued in the interrupt stack. BEC1 is reset to zero when it is read.

Block Error counter 2 (BEC2)

(read only)

After reset: 00H

ec7	ec6	ec5	ec4	ec3	ec2	ec1	ec0

This Register indicates the binary value of the Block Error up-counter 2. Febe errors are always counted. According to C2E bit setting in register OPR, when counter one reachs the threshold ECT2, BEC2 register is queued in the interrupt stack. BEC2 is reset to zero when it is read.

Threshold Block Error Counter 1 register (ECT1)

After reset: FFH

ect17	ect16	ect15	ect14	ect13	ect12	ect11

It is possible to load in this register the binary value of a threshold for the Block Error counter 1.When Block error counter reachs this value, an Interrupt relative to BEC1 register is loaded in the interrupt stack. This can be used as an early alarm in case of degraded transmission.

Threshold Block Error Counter 2 register (ECT2)

After reset: FFH

ect27	ect26	ect25	ect24	ect23	ect22	ect21

It is possible to load in this register the binary value of a threshold for the Block Error counter 2.When Block error counter reachs this value, an interrupt relative to BEC2 register is loaded in the interrupt stack. This can be used as an early alarm in case of degraded transmission.

Receive status register - read command (RXOH) (Write only)

EOC	M4	M56	ACT	0	STATUS	0	RST

Reset to zero of all the RXOH bits is automatic.

EOC Receive EOC status register read.

When EOC bit is set equal one, UID automatically loads the current value of RXEOC register in the interrupt stack independently of any status change.

M4 Receive M4 overhead bits status register read.

When M4 bit is set equal one, UID automatically loads the current value of RXM4 register in the interrupt stack independently of any status change.

M56 Receive M5 and M6 overhead bits status register read.

When M56 bit is set equal one, UID automatically loads the current value of RXM56 register in the interrupt stack independently of any status change.

ACT Activation indication status.

When ACT bit is set equal one, UID automatically loads the current value of RXACT register in the interrupt stack independently of any status change.
In GCI mode, the RXACT read back always uses the monitor channel.

STATUS

When STATUS bit is set egal one, UID automatically loads the current value of STATUS register in the interrupt stack independently of any status change.

RST RESET (MICROWIRE/DSI configuration only).

When RST bit is set equal one, UID is fully reset including configuration registers, state machine and all coefficients and reset to their default value. UID enters in the power-down state.

Transmit EOC register (TXEOC)

After reset: FFFH

XEOC1	XEOC2	XEOC3	XEOC4	XEOC5	XEOC6	XEOC7	XEOC8

TXEOC Register is constituted of 12 bits. When transmitting SL2/SL3 or SN3 signal. STLC5411 shall continuously send into the EOC channel field the eoc bits twice per superframe. TXEOC register is loaded in the transmit register at each half a superframe.

The address of this register is composed only of 4 bits. Read-back can be performed by means of a read-back command 6100H.

Receive EOC register (RXEOC)

(read only)
After reset: FFFH

REOC1	REOC2	REOC3	REOC4	REOC5	REOC6	REOC7	REOC8

The RX EOC Register is constituted of 12 bits. When the line is fully activated (super frame synchronized) and when a new eoc message is received and validated in accordance with the criteria selected in the Configuration Register OPR, the RX EOC Register is queued in the interrupt register stack. The address of this register is composed only of 4 bits.
It is always possible to read this register by writing RXEOC = 1 in RXOH register

Identification Register (IDR)
Fixed value: 08H
(read only)

When a read-back operation of IDR register is entered, UID loads the Identification Register in the interrupt stack. This register provides a reserved identification code agreed by GCI standard: 08H.

IDR register is accessible via two addresses.

MWPS Micro Wire Port Select register (Significant in microwire mode only).
(write only)

Default value: Mode A (5410 compatible)

- Writting FFH value select the mode B to exchange data onto CI & CO
- Writing 00H value select the mode A (See Microwire control interface paragraph for more details Mode A, Mode B).

Note: Soft Reset has no effect on the select mode.

Table 8: Register Content.

REGISTER ACCESS MESSAGES												
FUNCTION		BYTE 1			BYTE 2							
		AD7/4	AD3/1	AD0	7	6	5	4	3	2	1	0
NOP		0000	000	0	0	0	0	0	0	0	0	0
RESERVED		0001	XXX	X	0	0	0	0	0	0	0	0
OPR	W	0010	000	0	CIE	EIE	FIE	OB1	OB0	0C1	0C0	C2E
OPR	R	0010	000	1	0	0	0	0	0	0	0	0
CR1	W	0010	001	0	FF1	FF0	CK2	CK1	CK0	DDM	CMS	BEX
CR1	R	0010	001	1	0	0	0	0	0	0	0	0
CR2	W	0010	010	0	SFS	NTS	DMO	DEN	DD	BP1	BP2	RR
CR2	R	0010	010	1	0	0	0	0	0	0	0	0
CR3	W	0010	011	0	LB1	LB2	LBD	DB1	DB2	DBD	TLB	T15D
CR3	R	0010	011	1	0	0	0	0	0	0	0	0
CR4	W	0010	100	0	EB1	EB2	ED	0	ESFr	EIF	MOB	CTC
CR4	R	0010	100	1	0	0	0	0	0	0	0	0
CR5	W	0010	101	0	IO4	IO3	IO2	IO1	D4	D3	D2	D1
CR5	R	0010	101	1	0	0	0	0	0	0	0	0
CR6	W	0010	110	0	T15E	ACTAUT	PUPAUT	QM	AIS	TFB0	RFS	LFS
CR6	R	0010	110	1	0	0	0	0	0	0	0	0
RESERVED		0010	111	X	0	0	0	0	0	0	0	0
TXB1	W	0011	000	0	0	0	B1X5	B1X4	B1X3	B1X2	B1X1	B1X0
TXB1	R	0011	000	1	0	0	0	0	0	0	0	0
TXB2	W	0011	001	0	0	0	B2X5	B2X4	B2X3	B2X2	B2X1	B2X0
TXB2	R	0011	001	1	0	0	0	0	0	0	0	0
RXB1	W	0011	010	0	0	0	B1R5	B1R4	B1R3	B1R2	B1R1	B1R0
RXB1	R	0011	010	1	0	0	0	0	0	0	0	0
RXB2	W	0011	011	0	0	0	B2R5	B2R4	B2R3	B2R2	B2R1	B2R0
RXB2	R	0011	011	1	0	0	0	0	0	0	0	0
TXD	W	0011	100	0	DX5	DX4	DX3	DX2	DX1	DX0	SX1	SX0
TXD	R	0011	100	1	0	0	0	0	0	0	0	0
RXD	W	0011	101	0	DR5	DR4	DR3	DR2	DR1	DR0	SR1	SR0
RXD	R	0011	101	1	0	0	0	0	0	0	0	0
RESERVED		0011	11X	X	0	0	0	0	0	0	0	0

Notes:

1. Bit 7 of byte 1 is the first bit clocked into the UID.
2. All configuration registers can be read-back by setting bit 7 of BYTE 1 equal 1
3. RXOH is a Write only register to force RXEOC, RXM4, RXM56, RXACT status register sending. RST reset the device
4. It is recommended not to access all RESERVED adresses. X means 1 or 0

W refers to a write operation.
R refers to a request for read-back.

Table 8: Register Content (Continued)

REGISTER ACCESS MESSAGES												
FUNCTION		BYTE 1			BYTE 2							
		AD7/4	AD3/1	AD0	7	6	5	4	3	2	1	0
TXM4	W	0100	000	0	0	M42x	M43x	M44x	M45x	M46x	0	M48x
TXM4	R	0100	000	1	0	0	0	0	0	0	0	0
TXM56	W	0100	001	0	0	0	0	M51x	M61x	M52x	FEBx	FEBx
TXM56	R	0100	001	1	0	0	0	0	0	0	0	0
TXACT	W	0100	010	0	0	0	0	0	C4x	C3x	C2x	C1x
TXACT	R	0100	010	1	0	0	0	0	0	0	0	0
BEC1	R	0100	011	1	0	0	0	0	0	0	0	0
BEC2	R	0100	100	1	0	0	0	0	0	0	0	0
ECT1	W	0100	101	0	ECT17	ECT16	ECT15	ECT14	ECT13	ECT12	ECT11	ECT10
ECT1	R	0100	101	1	0	0	0	0	0	0	0	0
ECT2	W	0100	110	0	ECT27	ECT26	ECT25	ECT24	ECT23	ECT22	ECT21	ECT20
ECT2	R	0100	110	1	0	0	0	0	0	0	0	0
RXOH	W	0100	111	0	EOC	M4	M56	ACT	0	STATUS	0	RST
RESERVED		0100	111	0	0	0	0	0	0	0	0	0
TXEOC	W	0101	EFG	H	XEOC1	XEOC2	XEOC3	XEOC4	XEOC5	XEOC6	XEOC7	XEOC8
TXEOC	R	0110	000	1	0	0	0	0	0	0	0	0
RESERVED		0111	XXX	X	0	0	0	0	0	0	0	0
IDR	R	1000	000	0	0	0	0	0	0	0	0	0
DR	R	1001	XXX	X	0	0	0	0	0	0	0	0
FREE		101X	XXX	X	0	0	0	0	0	0	0	0
FREE		11XX	XXX	X	0	0	0	0	0	0	0	0
MPWS	W	1111	111	0	FF = Mode B					00 = Mode A		

Notes:

1. All transmit registers can be read-back by setting bit 7 of BYTE 1 equal 1 except for TXEOC register To read-back TXEOC, use the command 61-00 H.

2. BEC1, BEC2 and IDR are read-only registers

3. FREE adresses are ignored by the device.

4. In the TXEOC register:
   E = ea1, the msb of the EOC destination address
   F = ea2
   G = ea3
   H = dm, the EOC data/message mode indicator

5 M42x is significant in NT mode only

Table 8: Register Content (Continued).

READ BACK MESSAGES											
FUNCTION	BYTE 1			BYTE 2							
	AD7/4	AD3/1	AD0	7	6	5	4	3	2	1	0
OPR	0010	000	1	CIE	EIE	FIE	OB1	OB0	0C1	0C0	C2E
CR1	0010	001	1	FF1	FF0	CK2	CK1	CK0	DDM	CMS	BEX
CR2	0010	010	1	SFS	NTS	DMO	DEN	DD	BP1	BP2	RR
CR3	0010	011	1	LB1	LB2	LBD	DB1	DB2	DBD	TLB	T15D
CR4	0010	100	1	EB1	EB2	ED	0	ESFr	EIF	UOB	CTC
CR5	0010	101	1	I04	I03	I02	I01	D4	D3	D2	D1
CR6	0010	110		T1SE	ACTUAT	PUPAUT	QM	AIS	TFB0	RFS	LFS
TXB1	0011	000	1	0	0	B1X5	B1X4	B1X3	B1X2	B1X1	B1X0
TXB2	0011	001	1	0	0	B2X5	B2X4	B2X3	B2X2	B2X1	B2X0
RXB1	0011	010	1	0	0	B1R5	B1R4	B1R3	B1R2	B1R1	B1R0
RXB2	0011	011	1	0	0	B2R5	B2R4	B2R3	B2R2	B2R1	B2R0
TXD	0011	100	1	DX5	DX4	DX3	DX2	DX1	DX0	SX1	SX0
RXD	0011	101	1	DR5	DR4	DR3	DR2	DR1	DR0	SR1	SR0
TXM4	0100	000	1	0	M42x	M43x	M44x	M45x	M46x	0	M48x
TXM56	0100	001	1	0	0	0	M51x	M61x	M52x	FEBx	FEBx
TXACT	0100	010	1	0	0	0	0	C4x	C3x	C2x	C1x
BEC1	0100	011	1	c7	c6	c5	c4	c3	c2	c1	c0
BEC2	0100	100	1	c7	c6	c5	c4	c3	c2	c1	c0
ECT1	0100	101	1	ECT17	ECT16	ECT15	ECT14	ECT13	ECT12	ECT11	ECT10
ECT2	0100	110	1	ECT27	ECT26	ECT25	ECT24	ECT23	ECT22	ECT21	ECT20
TXEOC	0110	EFG	H	XEOC1	XEOC2	XEOC3	XEOC4	XEOC5	XEOC6	XEOC7	XEOC8
IDR	1000	000	0	0	0	0	0	1	0	0	0

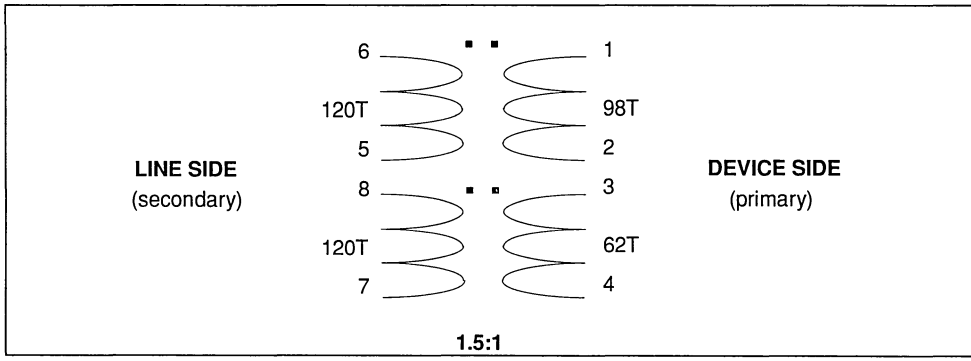
Notes:
1. For all these registers with the exception of TXEOC, bit 0 of BYTE 1 is set to 1 to indicate read-back message.
2. CR5 configuration/status register is listed with status registers.
3. Bit 7 of BYTE 1 is the first clocked out from the UID.
4. M42x is significant in NT mode only

SPONTANEOUS OR DRIVEN MESSAGES											
FUNCTION	BYTE 1			BYTE 2							
	AD7/4	AD3/1	AD0	7	6	5	4	3	2	1	0
CR5	0010	101	0	IO4	IO3	IO2	IO1	D4	D3	D2	D1
RXM4	0100	000	0	M41R	M42R	M43R	M44R	M45R	M46R	M47R	M48R
RXM56	0100	001	0	0	0	0	M51R	M61R	M52R	FEBR	NEBR
RXACT	0100	010	0	0	0	0	0	C4R	C3R	C2R	C1R
BEC1	0100	011	0	c7	c6	c5	c4	c3	c2	c1	c0
BEC2	0100	100	0	c7	c6	c5	c4	c3	c2	c1	c0
RXEOC	0101	EFG	H	REOC1	REOC2	REOC3	REOC4	REOC5	REOC6	REOC7	REOC8

Notes:

1. All status registers can be read by setting first the appropriate command. At any status change, an interrupt cycle is issued
2. In the RXEOC register:
   E = ea1
   F = ea2
   G = ea3
   H = d=0/m = 1
3. For all These registers with the exception of RXEOC, bit 0 of BYTE 1 is set to 0 to indicate a status register.

Figure 11: Transformer Design.



Line Interface Circuit

It is very important, compliance with the ANSI and French standard, that the recommended line interface circuit should be strictly adhered to. The channel response and dynamic range of this circuit have been carefully designed as an integral part of the overall signal processing system to ensure the the performance requirements are met under all the specified loop conditions. Deviatons from this design are likely to result in sub-optimal performance or even total failure of the system on some types of loops.

Turns Ratio: Np:Ns = 1:1.5.
Secondary Inductance: Lp 27mH.
Max leakage inductance: 100µH
Winding Resistances: 30 ohms (2.25Rp + Rs) > 10 ohms.
Return Loss at: 40 kHz against 135 ohms 26 dB.
Saturation characteristics: THD –70dB when tested with 50mA d.c. through the secondary and a 40kHz sine-wave injected into the primary at a level which generates 5V p-p into 135 ohms at the secondary.

List of suppliers:

SHOTT
PULSE ENGINEERING
AIE

Table 10.

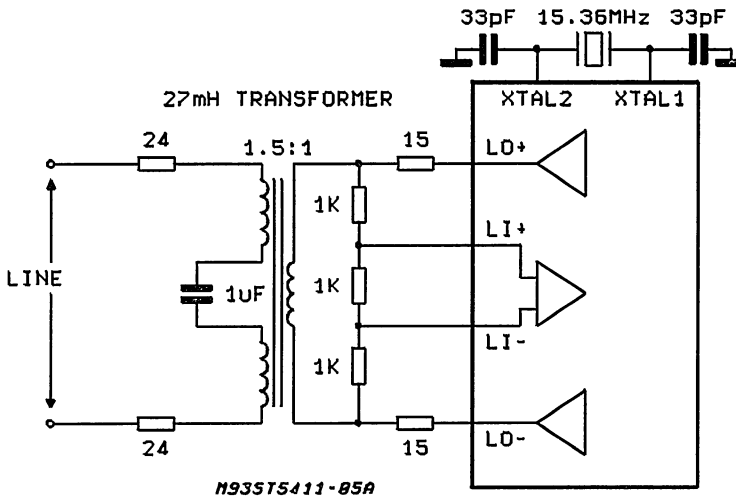
WINDING	NUMBER OF TURNS	WIRE GAUDGE
1-2	98 Single	#34 AWG
6-5, 8-7	120+120 Bifilar	#36 AWG
3-4	62 Single	#34 AWG

WINDING	INDUCTANCE	RESISTANCE
1-2 + 3-4	12 mH	less than 5Ω
5-6 + 7-8	27 mH	less than 10 Ω

Board Layout

While the pins of the UID are well protected against electrical misuse, it is recommended that the standard CMOS practise of applying GND to the device before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used. Great care must be taken in the layout of the printed circuit board in order to preserve the high transmission performance of the ST5410. To maximize performance, do not use the philosophy of separating analog and digital grounds for chip. The 3 GND pins should be connected together as close as possible to the pins, and the 2 VCC pins should be strapped together. All ground connections to each device should meet at a common point as close as possible to the 3 GND pins order to prevent the interaction of ground return currents flowing through a common bus impedance. Two decoupling capacitors of 10µF and 0.1µF should be connected from this common point to VCC pins as close as possible to the chip. Taking care with the board layout in the following ways will also help prevent noise injection into the receiver frontend and maximize the transmission performances. Keep the crystal oscillator components away from the receiver inputs and use a shielded ground plane around these components. Keep the device, the components connected to LI+/LI- and the transformer as close possible. Simmetrical layout for the line interface is suggested.

Figure 12: Recommended connections.



0.1% MATCHING IS REQUIRED TO MEET THE LONGITUDINAL BALANCE SPECIFICATION
THE 15ohm AND 1K RESISTORS IN THE INTERFACE CIRCUIT SHOULD BE 1%.

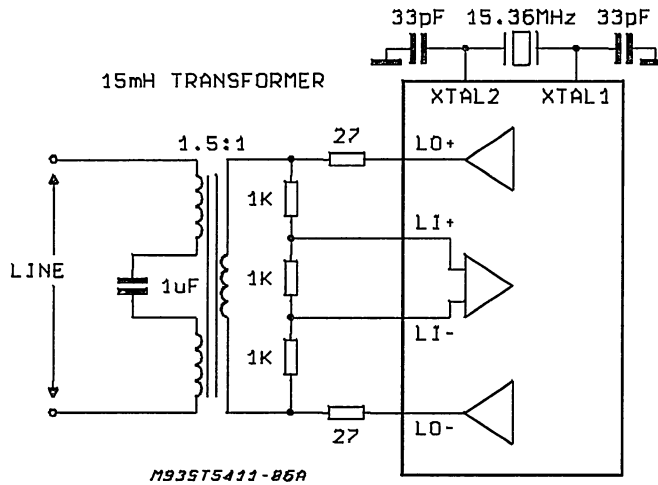


Figure 13a: LT Application.

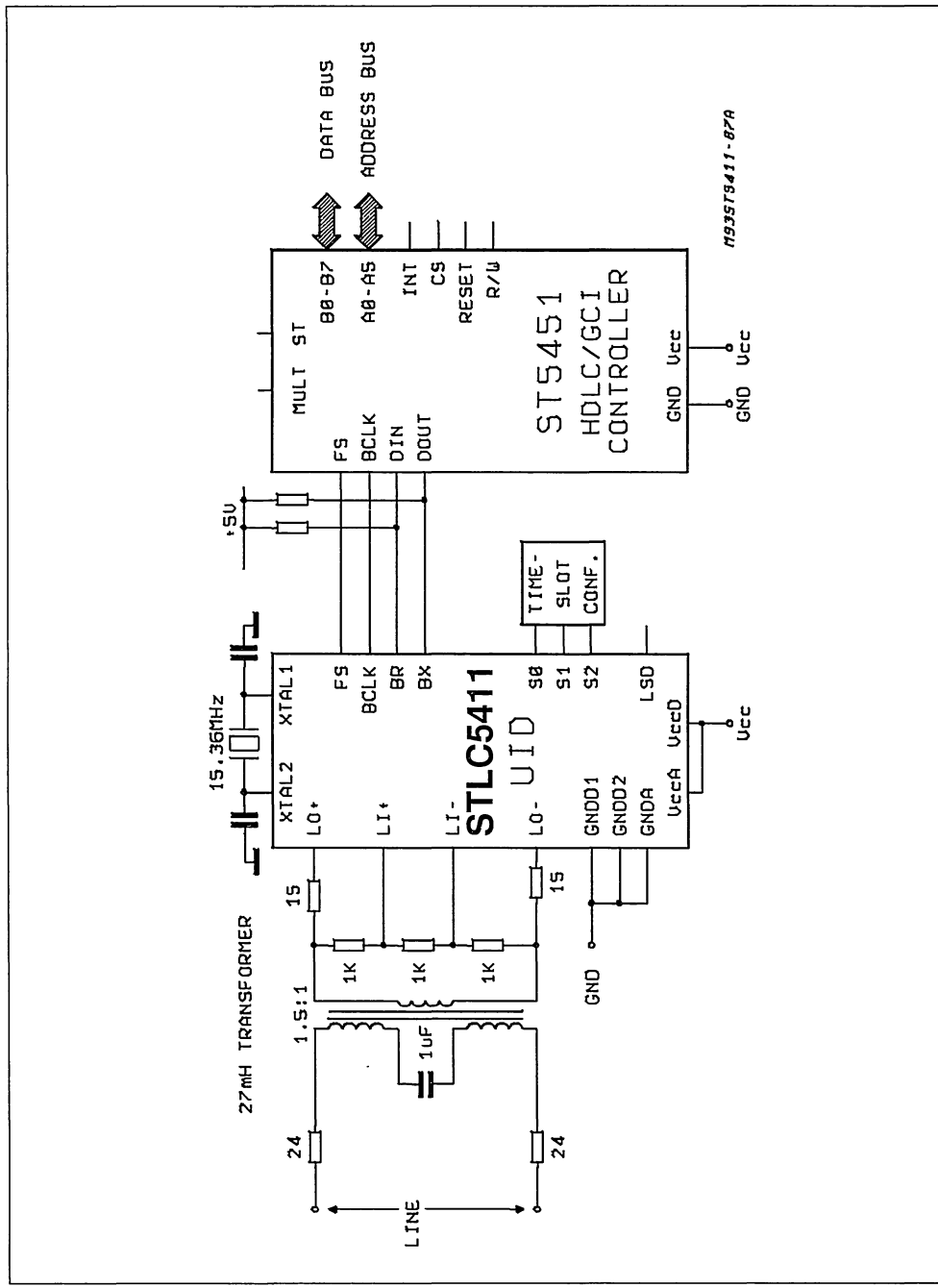


Figure 13b: NT Application.

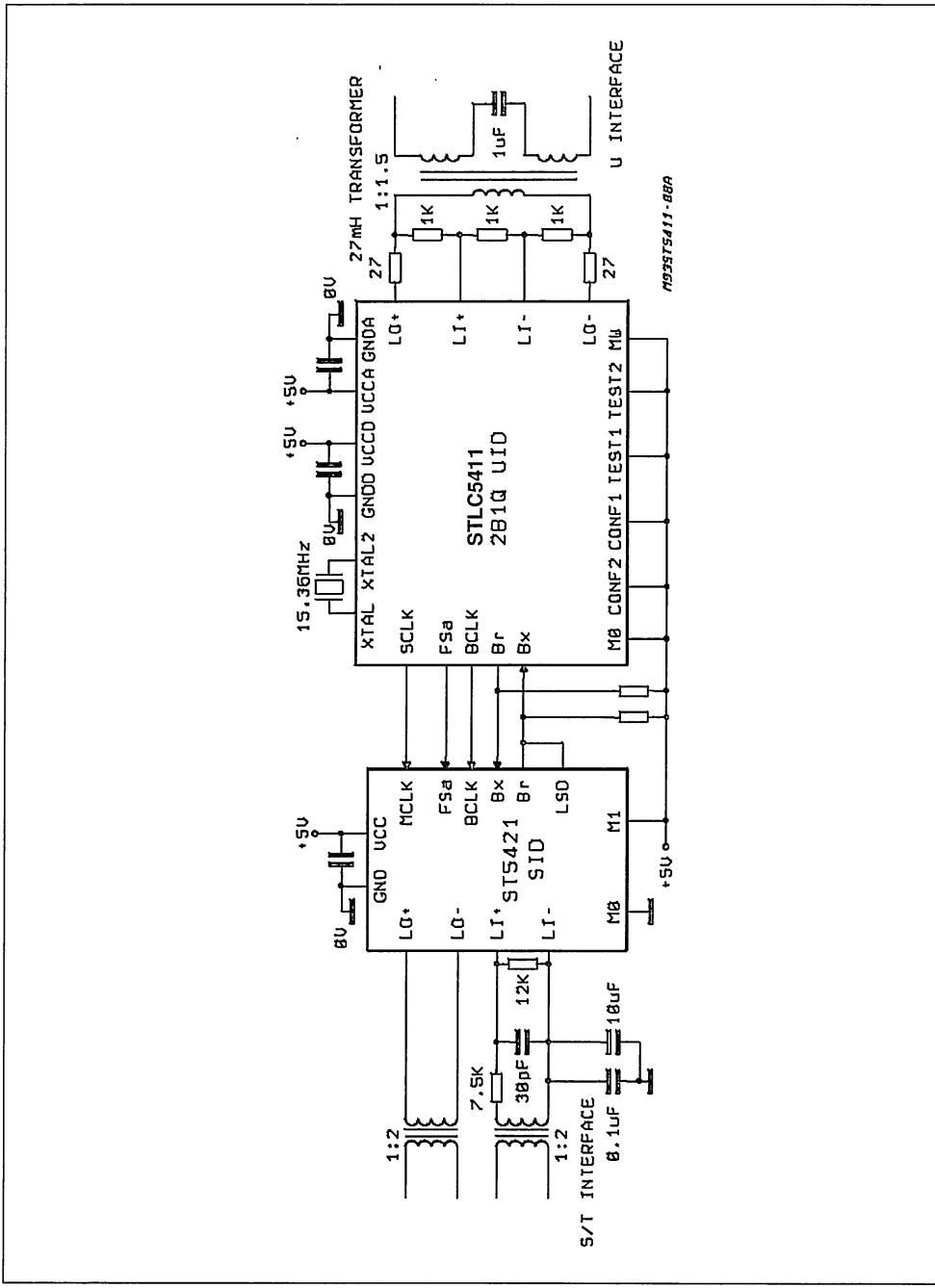
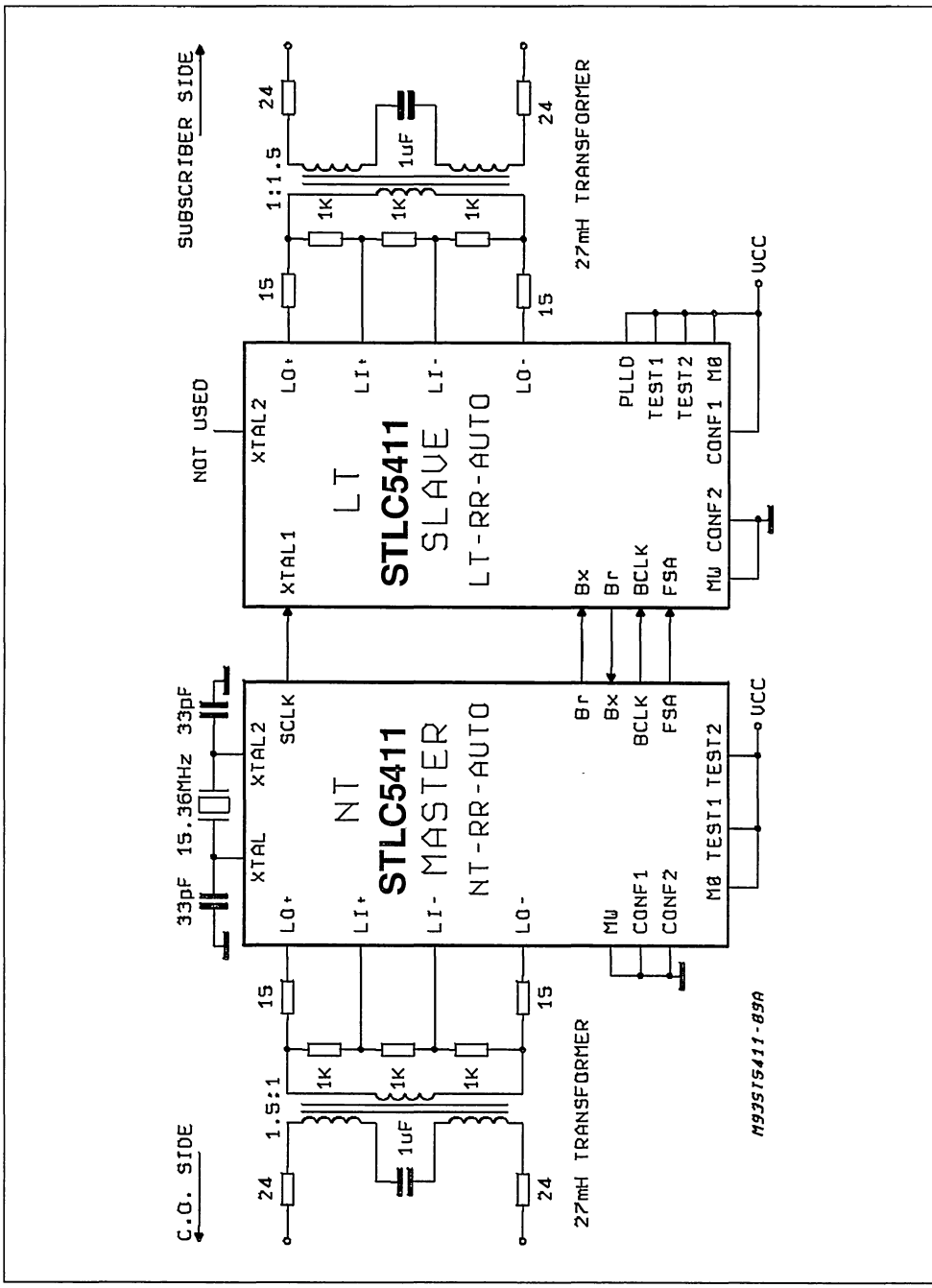
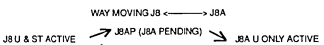


Figure 13c: RR Application.



				← START UP STATES →										← ACTIVATION STATES →							← END STATES →		← ERROR STATES →	
														← U & S →				← U ONLY →							
	EVENTS	STATE NAME	Power Off	Full Reset	Alting	Awake	EC TRming	WAIT SN2	CHECK SN2	EC CVGED	EC CVG UAO	SW SYNC	SW SYN UAO	ISW SYNC	TRANSIT BP2/FAO	TRANSIT RR	U & ST ACTIVE	Pending $DEACT_{ST}$	U only ACTIVE	Pding $ACTIVE_{ST}$	DEACT Alertn	Pding DEACT	TEAR DOWN	RECV RESET
		STATE CODE	J0	J1	J2	J3	J4	J41	J42	J5	J5A	J6	J6A	J7	J78	J78R	J8	J8AP	J8A	J8P	J9	J11	J10	J12
		U LINE TX	SL0	SL0	TL	SL0	SL1	SL2 act = 0 dea = 1 uoa (4)	SL2 act = 0 dea = 1 uoa = *	SL2 act = 0 dea = 1 uoa = 1	SL2 act = 0 dea = 1 uoa = 0	SL2 act = 0 dea = 1 uoa = 1	SL2 act = 0 dea = 1 uoa = 0	SL3 act (3) dea = 1 uoa = 1	SL3 act (3) dea = 1 uoa = 1	SL3 act = 1 dea = 1 uoa = 1	SL3 act = 1 dea = 1 uoa = 1	SL3 act = * dea = 1 uoa = 1	SL3 act = 0 dea = 1 uoa = 0	SL3 act = 0 dea = 1 uoa = 0	SL3 act = * dea = 0 uoa = *	SL0	SL0	SL0
↑ MOST	POWER ON # GCI only		J1 DI#	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
	LOSS OF POWER		/	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0
	RES COMMAND		/	J1	sp T5 J10 EIU (1)	sp T5 J10 EIU (1)	sp T5 J10 EIU (1)	sp T5 J10 EIU (1)	sp T5 J10 EIU (1)	sp T5 J10 EIU (1)	sp T5 J10 EIU (1)	sp T5 J10 EIU (1)	sp T5 J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	/	/	/	/
	EXPIRY OF TIMER 5 (15 seconds)		/	/	/	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	/	/	/	/	/	/	/	/	/	/	/
	LOSS OF SIGNAL (>480ms)		/	/	/	/	/	/	/	/	/	/	/	st T7 J12 EIU (1)	st T7 J12 EIU (1)	st T7 J12 EIU (1)	st T7 J12 EIU (1)	st T7 J12 EIU (1)	st T7 J12 EIU (1)	st T7 J12 EIU (1)	st T7 J12 EIU (1)	/	/	/
	LOSS OF SYNC (>480ms)		/	/	/	/	/	/	/	/	/	/	/	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	J10 EIU (1)	/	/	/
	not CM COMMAND & RECEIVED TONE TN		/	st T5 J3 AP	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	sp T7 J1 D1
	ARL COMMAND		/	st T5 J2	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
	END TONE TL (3ms)		/	/	J3	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
EVENTS PRIORITY	EC	not BP1 or ARL	/	/	/	/	J41	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
	CVC	BP1 &(AR or UAR)	/	/	/	/	J41	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
	DETCT SIGN ENERGY	not UAR	/	/	/	/	/	J42	J5	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
		UAR	/	/	/	/	/	J42	J5A	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
	BASIC FRAME SYNC		/	/	/	/	/	/	/	J6	J6A	/	/	/	/	/	/	/	/	/	/	/	-	/
	SUPER FRAME SYNC (ISW)		/	/	/	/	/	/	/	/	/	spT5 J7 UAI	spT5 J8A UAI	/	/	/	/	/	/	/	/	/	/	/
	DR COMMAND		/	/	/	/	/	/	/	/	/	/	/	J9	J9	J9	J9	J9	J9	J9	/	/	/	/
	AR COMMAND		/	st T5 J2	/	/	/	/	/	/	/	/	/	/	/	/	/	/	J7	J7	/	/	/	/
	UAR COMMAND		/	st T5 J2	/	/	/	/	/	/	/	/	/	J8AP	J8AP	J8AP	J8AP	/	/	/	/	/	/	/
	AI COMMAND		/	/	/	/	/	/	/	/	/	/	/	/	J8	/	/	/	/	/	/	/	/	/
	FAO COMMAND		/	/	/	/	/	/	/	/	/	/	/	/	/	J7	J78	/	/	/	/	/	/	/
	Receved act=1	not BP2	/	/	/	/	/	/	/	/	/	/	/	J8 AI	/	J8 AI	/	/	/	/	/	/	/	/
		BP2	/	/	/	/	/	/	/	/	/	/	/	J78 AI	/	J8 AI	/	/	/	/	/	/	/	/
	Receved act=0	not RR or ARL	/	/	/	/	/	/	/	/	/	/	/	/	J7 EI	/	J7 EI	/	/	/	/	/	/	/
		RR & not ARL	/	/	/	/	/	/	/	/	/	/	/	/	J7 EI	/	J78R EI	/	/	/	/	/	/	/
	Receved sai = 1		/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	J8P AP	/	/	/	/	/
	Receved sai = 0 and act = 0		/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	J8A UAI	/	/	/	/	/	/
	ABSCENCE OF SIGNAL (<40ms)		/	/	/	J4	/	/	J41	/	/	/	/	/	/	/	/	/	/	/	/	J1 D1	st T7 J12	/
	END 4 SUPER FRAMES		/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	J11	/	/	/
↓ LEAST	EXPIRY OF TIMER 7 (40ms)		/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	J1 D1

(1) IN AUTO MODE, THE EIU INDICATION BECOMES RES (EIU & RES HAVE THE SAME CODE)
(2) IN J7/J78 STATES, IF ARL COMMAND THEN act BIT IS AUTOMATICALLY SET TO "1", ELSE act BIT = "0"
(3) uoa BIT = "1" WHEN THE ACTVATION PROCEDURE HAS BEEN INITIATED BY TE SIDE OR LT SIDE BY AR COMMAND, ELSE uoa BIT = "0"
(*) NO CHANGE

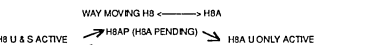


ACTIVATION/DEACTIVATION FINITE STATE MATRIX IN LT MODE

				START UP STATES									ACTIVATION STATES								END STATES		
													U & S				U ONLY				ERROR STATES		
	EVENTS	STATE NAME	POWER OFF	FULL RESET	ALTING	EC TRning	WAIT SL	CHECK SL	EC CVGED	SW SYNC	ISW SYN Chk uoa	Pding ACTIV$_{nt}$	ISW SYNC	Pding ACTIVE	U & ST ACTIVE	TE INACTIV	Pding DAECT$_{ST}$	U only ACTIVE	Pding ACTIVE$_{ST}$	Pding DEACT	RECEIV RESET	TEAR DOWN
		STATE CODE	H0	H1	H2	H3	H31	H32	H4	H5	H5A	H5B	H6	H7	H8	H11	H8AP	H8A	H8P	H9	H12	H10
		U LINE TX	SN0	SN0	TN	SN1	SN0	SN0	SN0	SN2	SN2	SN2	SN3 act = 0 sai = *	SN3 act = 1 sai = 1	SN3 act = 1 sai = 1	SN3 act = 0 sai = 0	SN3 act = * sai = *	SN3 act = 0 sai = 0	SN3 act = 0 sai = 1	SN3 act = * sai = *	SN0	SN0
↑ MOST	POWER ON # GCI only		H1 DI#	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
	LOSS OF POWER		/	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0
	RES COMMAND		/	H1	sp T4 H10 EIU (1)	sp T4 H10 EIU (1)	sp T4 H10 EIU (1)	sp T4 H10 EIU (1)	sp T4 H10 EIU (1)	sp T4 H10 EIU (1)	H10 EIU	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	/	/
	EXPIRY OF TIMER 4 (15 seconds)		/	/	/	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	J10 EIU (1)	/	/	/	/	/	/	/	/	/	/	/	/
	LOSS OF SIGNAL (>480ms)		/	/	/	/	sp T4 st T6 H12 EIU (1)	/	/	/	st T6 H12 EIU (1)	st T6 H12 EIU (1)	st T6 H12 EIU (1)	st T6 H12 EIU (1)	st T6 - H12 EIU (1)	st T6 H12 EIU (1)	st T6 H12 EIU (1)	st T6 H12 EIU (1)	st T6 H12 EIU (1)	/	/	/
	LOSS OF SYNC (>480ms)		/	/	/	/	/	/	/	/	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	H10 EIU (1)	/	/
	not OM COMMAND & RECEIVED TONE TL (2)		/	st T4 H2(6) LSD	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	sp T6 H1 D1	/
	AR COMMAND & not RECEIVED TONE TL		/	st T4 H2	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
	END TONE TN (3ms)		/	/	H3	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
	EC CONVERGED		/	/	/	H31	/	/	/	/	/	/		/	/	/	/	/	/	/	/	/
	DETECT SIGN ENERGY		/	/	/	/	H32	H4	/	/	/	/		/	/	/	/	/	/	/	/	/
	BASIC FRAME SYNC		/	/	/	/	/	/	H5	/	/	/	/	/	/	/	/	/	/	/	/	/
	SUPER FRAME SYNC (ISW)		/	/	/	/	/	/	/	spT4 H5A	/	/	/	/	/	/	/	/	/	/	/	/
	RECEIVED dea = 0		/	/	/	/	/	/	/	/	H9 SAVE ST	H9 SAVE ST	H9 SAVE ST	H9 SAVE ST	H9 SAVE ST	H9 SAVE ST	H9 SAVE ST	H9 SAVE ST	H9 SAVE ST	/	/	/
	RECEIVED dea = 1		/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	RETURN SAVd ST	/	/
	When not RR	RECEIVED uoa = 0	/	/	/	/	/	/	/	/	H8A	/	H8AP DP (4)	H8AP DP (4)	H8AP DP (4)	/	/	/	/	/	/	/
		RECEIVED uoa = 1	/	/	/	/	/	/	/	/	H6 AP (3)	/	/	/	/	/	/	H6 AP (4)	H6 AP (4)	/	/	/
	When RR	RECEIVED uoa = 0	/	/	/	/	/	/	/	/	H5B UAP (3)	/	H8AP UAP (4)	H8AP UAP (4)	H8AP UAP (4)	/	/	/	/	/	/	/
		RECEIVED uoa = 1	/	/	/	/	/	/	/	/	H5B AP (3)	/	/	/	/	/	/	H6 AP (4)	H6 AP (4)	/	/	/
		UAI COMMAND & RECEIVED uoa = 0	/	/	/	/	/	/	/	/	/	H8A	/	/	/	/	H8A	/	/	/	/	/
		UAI COMMAND & RECEIVED uoa = 1	/	/	/	/	/	/	/	/	/	H6	/	/	/	/	H8A	/	/	/	/	/
	DI COMMAND		/	/	/	/	/	/	/	/	/	/	/	/	/	/	H8A	/	/	/	/	/
	AR COMMAND		/	/	/	/	/	/	/	/	/	/	/	/	/	/	H8A	/	/	/	/	/
	AI or AILCOMMAND		/	/	/	/	/	/	/	/	/	/	H7	/	/	H7 (5)	/	/	/	/	/	/
	EI COMMAND		/	/	/	/	/	/	/	/	/	/	/	H11 EI (5)	H11 EI (5)	/	/	/	/	/	/	/
	RECEIVED ad=0		/	/	/	/	/	/	/	/	/	/	/	/	H7 EI (4)	H6 EI (4,5)	/	/	/	/	/	/
↓ LESS	RECEIVED ad=1		/	/	/	/	/	/	/	/	/	/	/	H6 AI (4)	/	/	/	/	/	/	/	/
	ABSCENCE OF SIGNAL (<40ms)		/	/	/	/	/	H31	/	/	/	/	/	/	/	/	/	/	/	st T6 H12 DP	/	st T6 H12
	EXPIRY OF TIMER 6 (40ms)		/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	H1 D1	/

(1) IN AUTO-MODE, THE EIU PRIMITIVE BECOMES DP WHEN NOT RR MODE OR RES WHEN NOT RR MODE
(2) WHEN BP1 = '1', THE JUMP H2 FROM H1 WAITS FOR AN AR COMMAND
(3) IN AUTO-MODE, THESE PRIMITIVES INDICATION ARE REPLACED BY ARL WHEN A MESSAGE ANALOG LOOP BACK IS DETECTED
(4) IN AUTO-MODE, THESE PRIMITIVES INDICATION ARE REMOVED WHEN ARL INDICATION IS ALREADY SET
(5) IN NON AUTO-MODE, EI PRIMITIVE INDICATION IS SENT FROM H7/H8 TO H11 AND REMOVED FROM H11 TO H6 WHEN EI FILTER IS SET
THE JUMP FROM H11 TO H7 WITH AIOR AIL COMMAND IS POSSIBLE ONLY WHEN EI-FILTER IS SET
(6) IF BP1 = 1 AR REQUIRED TO JUMP TO H2

* no change



ACTIVATION/DEACTIVATION FINITE MACHINE IN NT MODE

APPENDIX B - ELECTRICAL PARAMETERS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.3 to 7.0	V
V_{IN}	Input Voltage	– 0.3 to 7.0	V
T_A	Operting Temperature Range	0 to 70	°C
T_{stg}	Storage TemperatureRange	– 55 to 150	°C

TRANSMISSION ELECTRICAL PARAMETERS

Parameter	Min.	Typ.	Max.	Unit
LINE INTERFACE FEATURES				
Differential Input Resistance between LI+/LI- (0–20KHz Bandwidth)	to be characterized			KΩ
Common Mode Input Resistance	to be characterized			KΩ
Power up Output Differential Impedance (0–20KHz) between LO+/LO-		1		Ω
Power Down Output Diffrential Impedance (0–20KHz) between LO+/LO-	8	12	16	Ω
POWER CONSUMPTION				
I_{CC} in Power Down		4		mA
I_{CC} in Power Up Transmitting (2)		55		mA
TRANSMISSION PERFORMANCES				
Transmit Pulse Amplitude on 120Ω load (1)	3.27		3.61	V
Transmit Pulse Linearity (1:3 ratio accurancy)	36	50		dB

(1) This specification garanties the ANSI specification, concerning the pulse amplitude using the line interface recommended schematics, of 2,5 æ 5% Volts peak amplitude for 2B1Q pulse.

(2) Test condition: VDD = 5V, 2B1Q random signal transmitted with recommended 27mH line interface (fig 12) terminated with 135Ω.

STATIC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{CC}	DC Supply Voltage		4.75		5.25	V
V_{IL}	Input Low Voltage	All Dig Inputs except XTAL1			0.7	V
V_{IH}	Input High Voltage	All Dig Inputs except XTAL1	2.2			V
V_{ILX}	Input Low Voltage	XTAL1 Input			0.5	V
V_{IHX}	Input High Voltage	XTAL1 Input	V_{DD}–0.5		0.7	V
V_{OL}	Output Low Voltage	Br, I_O = +7mA All other Digital Outputs, I_{ol} = +1mA			0.4 0.4	V V
V_{OH}	Output High Voltage	Br, I_O = –7mA All other Digital Outputs I_O = –1mA All Outputs (3), I_O = –100µA	2.4 2.4 V_{DD}–0.5			V V V
I_{LH}	Input Current	Any Digital V_{in} = V_{DD}	0		10	µA
I_{LL}	Input Current	Input pin numbers: 14,15,16, 22,26,18, V_{in} = GND	–10		0	µA
I_{LLR}	Input Current with Internal Pull Up Resistor	Input pin numbers: 6,7,12,13 17,19,25,27,28 Vin = GND	–100		0	µA
I_{LLX}	Input Current on XTAL1	GND < V_{in} < V_{DD}	–200		200	µA
I_{LLI}	Input Current on LI+/LI-	LI+ and LI- to GND	to be characterized			µA
IOZ	Output Current in High Impedance State (TRISTATE)	GND < Vout < V_{DD} ; All Digital Outputs except XTAL2	–10		10	µA

TIMING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
MASTER CLOCK						
FMCLK	Frequency of MCLK Tolerance	Including Temperature, Aging, Etc...	 –100	15.36	 +100	MHz ppm
	MCLK/XTAL Input Clock Jitter	External Clock Source			50	ns pk-pk
tWMH	Clock Pulse Width, MCLK High Level	$V_{IH} = V_{CC} - 0.5V$ $V_{IL} = 0.5V$	20			ns
tWML	Clock Pulse Width, MCLK Low Level		20			ns
tRM tFM	Rise Time of MCLK Fall Time of MCLK	Used as a Logic Input			10 10	ns ns
DIGITAL INTERFACE						
FBCLK	Frequency of BCLK	Formats 1, 2 and 3 Format 4 and GCI Mode	256 512		4095 6144	KHz KHz
tWBH	Clock Pulse Width, BCLK High Level	Measured from V_{IH} to V_{IH}	30			ns
tWBL	Clock Pulse Width, BCLK Low Level	Measured from V_{IL} to V_{IL}	30			ns
tRB	Risae Time of BCLK	Measured from V_{IL} to V_{IH}			15	ns
tFB	Fall Time of BCLK	Measured from V_{IH} to V_{IL}			15	ns
tSFB	Setup Time, FS High or Low to BCLK Low	DSI or GCI Slave Mode only	30			ns
tHBF	Hold Time, BCLK Low to FS High or Low	DSI or GCI Slave Mode only	20			ns
tDBF	Delay Time, BCLK High to FS High or Low	DSI or GCI Master Mode only	–20		20	ns
tDBD	Delay Time, BCLK High to Data Valid	Load = 150pF + 2 LSTTL Loads (*			80	ns
tDBDZ	Delay Time, BCLK High to Data HZ				50	ns
tDFD	Delay Time, FS High to Data Valid	Load = 150pF + 2 LSTTL Loads			80	ns
tSDB	Setup Time, Data Valid to BCLK Low		0			ns
tHBD	Hold time, BCLK to Data Invalid		20			ns
tDBT	Delay Time, BCLK High to TSR Low	Load = 100pF + 2 LSTTL Loads			80	ns
tDBTZ	Delay Time, BCLK Low to TSR HZ				50	ns
tDFT	Delay Tie, FS High to TSR Low	Load = 100pF + 2 LSTTL Loads			80	ns
D PORT IN CONTINUOUS MODE: 16KBITS/SEC						
tSDD	Setup Time, DCLK Low to DX High or Low		50			ns
tHDD	Hold Time, DCLK Low to DX High or Low		50			ns
tDDD	Delay Time, DCLK High to DR High or Low	Load = 50pF + 2 LSTTL Loads			80	ns
MICROWIRE CONTROL INTERFACE						
FCCLK	Frequency of CCLK				5	MHz
tWCH	Clock Pulse Width, CCLK High Level	Measured from V_{IH} to V_{IH}	85			ns
tWCL	Clock Pulse Width, CCLK Low Level	Measured from V_{IL} to V_{IL}	85			ns
tRC	Rise Time of CCLK	Measured from V_{IL} to V_{IH}			15	ns
tFC	Fall Time of CCLK	Measured from V_{IH} to V_{IL}			15	ns
tSSC	Setup Time, CSB Low to CCLK High		60			ns
tHCS	Hold Time, CCLK Low to CSB High		10			ns
tWSH	Duration of CSB High		200			ns
tSIC	Setup Time, CI Valid to CCLK High		25			ns
tHCI	Hold Time, CCLK High to CI Invalid		25			ns
tDSO	Delay Time, CSB Low to CO Valid	Out First Bit on CO			50	ns
tDCO	Delay Time CCLK Low to CO Valid	Load = 50 pF + 2LSTTL Loads			50	ns
tDCOZ	Delay Time, CCLK Low to CO HZ				50	ns
tDCI	Delay Time, CCLK Low to INTB Low or HZ	Load = 80pF + 2LSTTL Loads			50	ns

(* In GCI mode: Load Res.

Figure 14: BCLK, FSA, FSB, SLAVE MODE, DELAYED MODE, FORMATS 1 2 3 (MW ONLY).

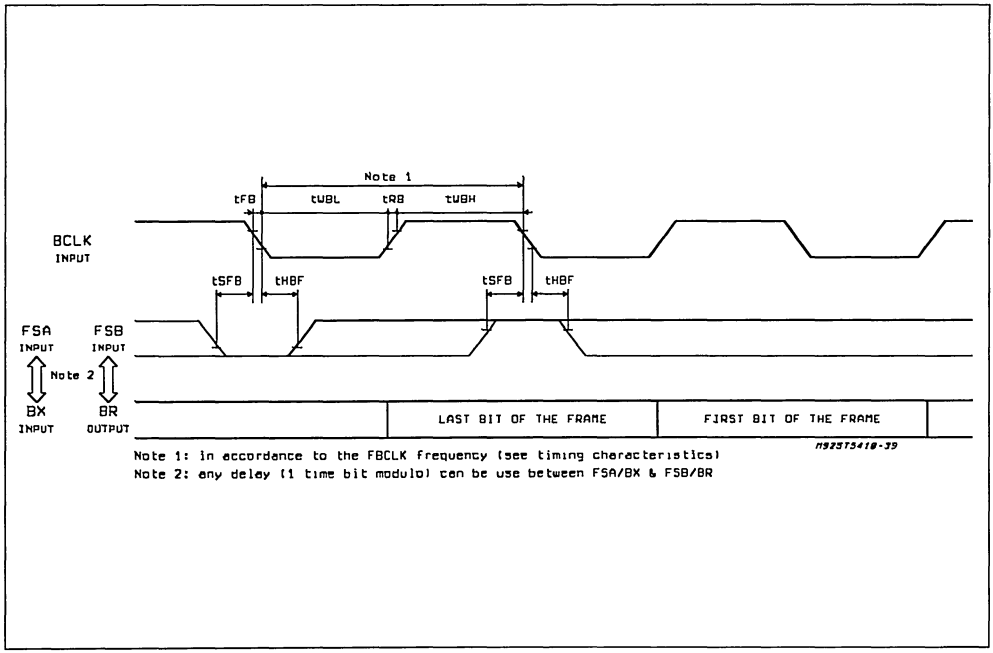


Figure 15: BCLK, FSA, FSB, SLAVE MODE, NON DELAYED MODE, FORMATS 1 2 3 (MW ONLY).

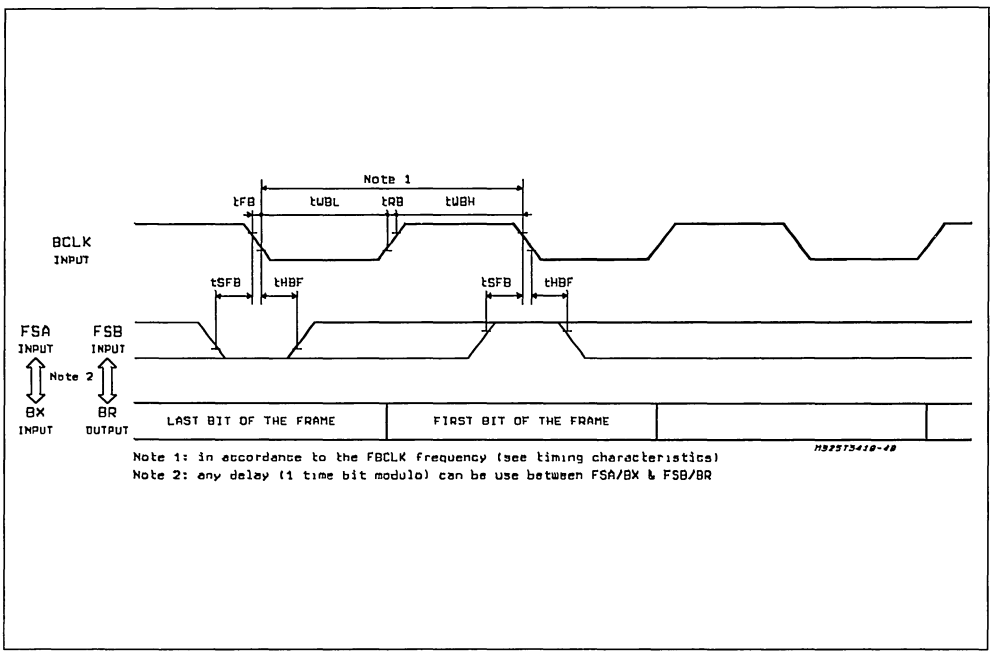


Figure 16: BCLK, FSA, FSB, SLAVE MODE, FORMAT 4 ALWAYS NON DELAYED MODE, (MW AND GCI MODE).

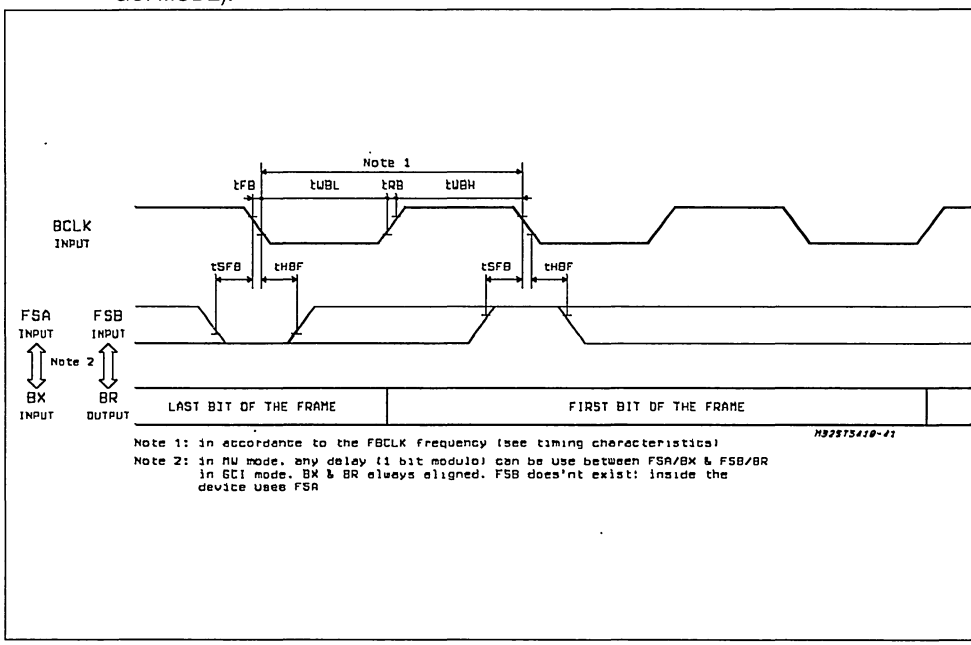


Figure 17: BCLK, FSA, FSB, MASTER MODE, DELAYED MODE, FORMATS 1 2 3 (MW ONLY).

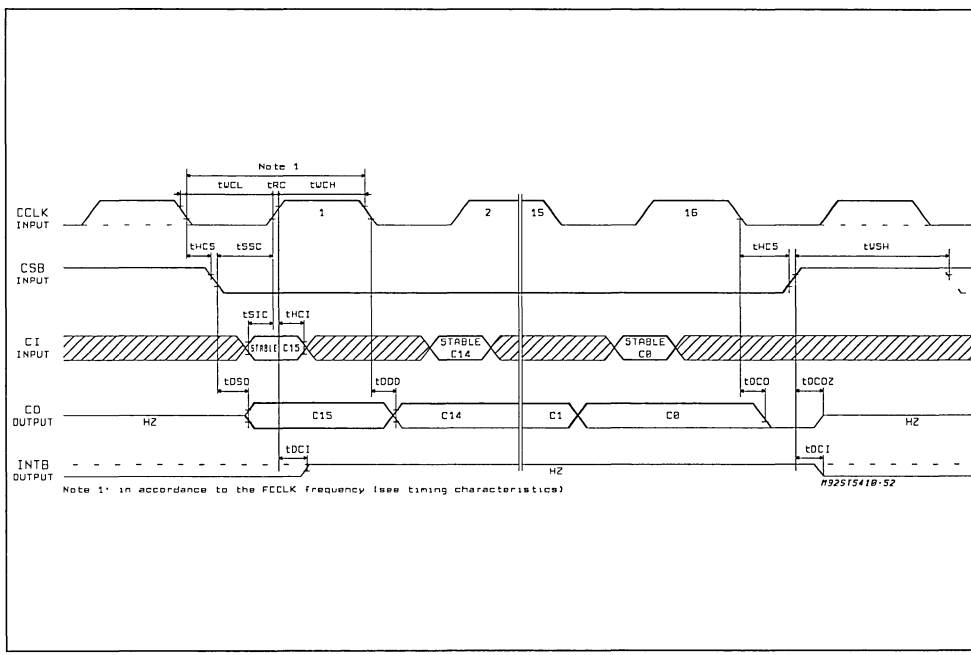


Figure 18: BCLK, FSA, FSB, MASTER MODE, NON DELAYED MODE, FORMATS 1 3 (MW ONLY).

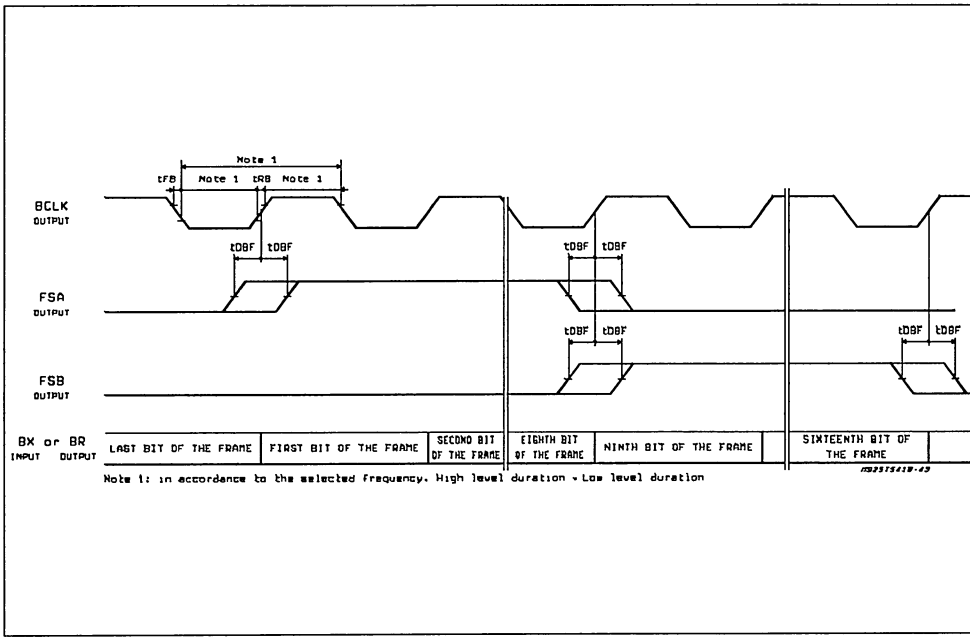


Figure 19: BCLK, FSA, FSB, MASTER MODE, FORMAT 4 ALWAYS NON DELAYED MODE, (MW AND GCI MODE).

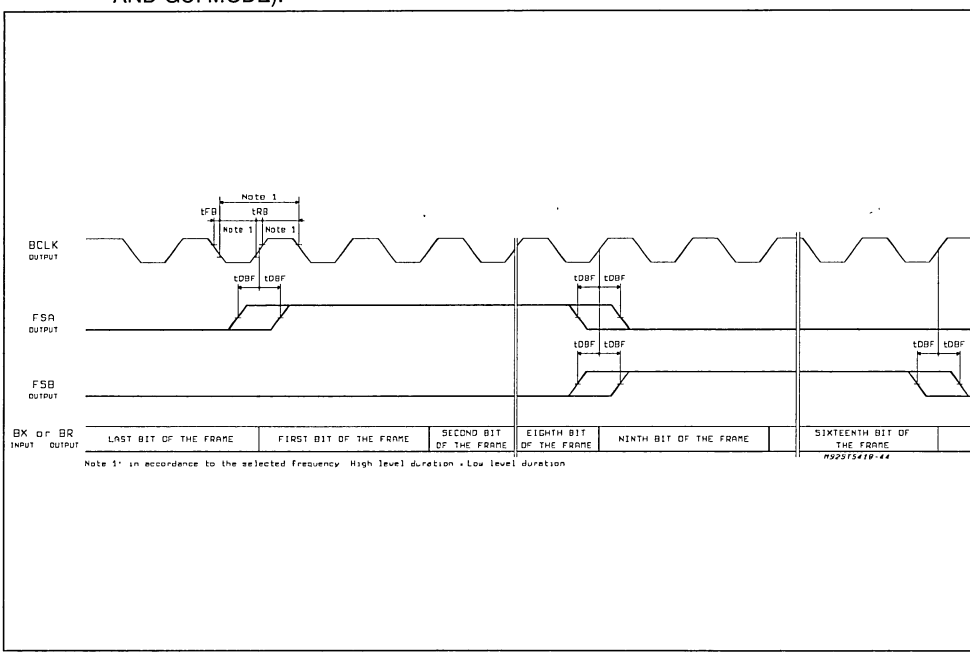


Figure 20: BX, DX, BR, DR, SLAVE & MASTER, DELAYED & NON DELAYED, FORMATS 1 2 3 (MW ONLY)

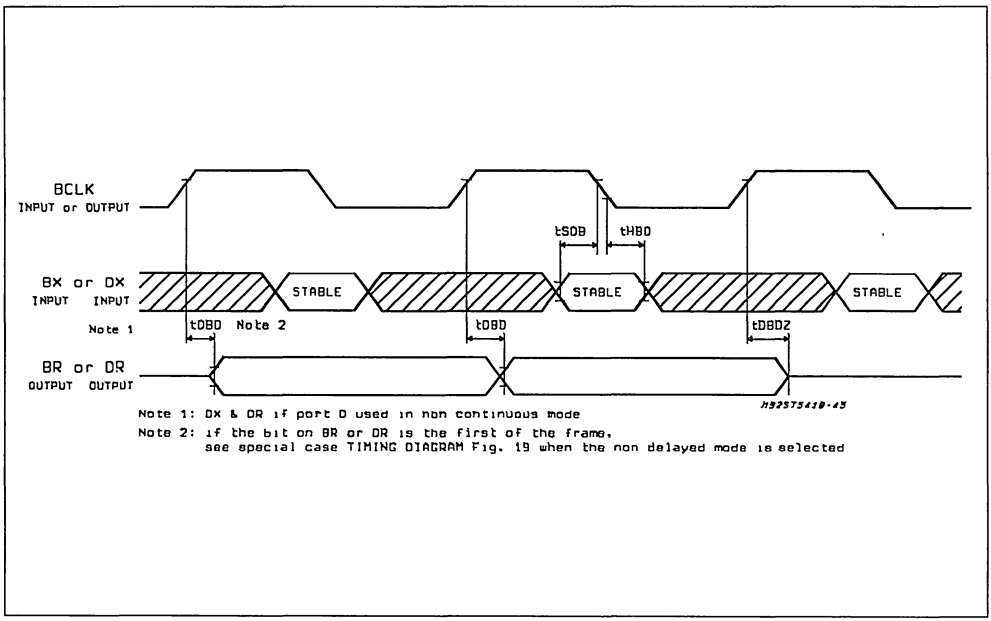


Figure 21: BX, DX, BR, DR, SLAVE & MASTER, FORMAT 4 ALWAYS NON DELAYED, (MW & GCI MODE)

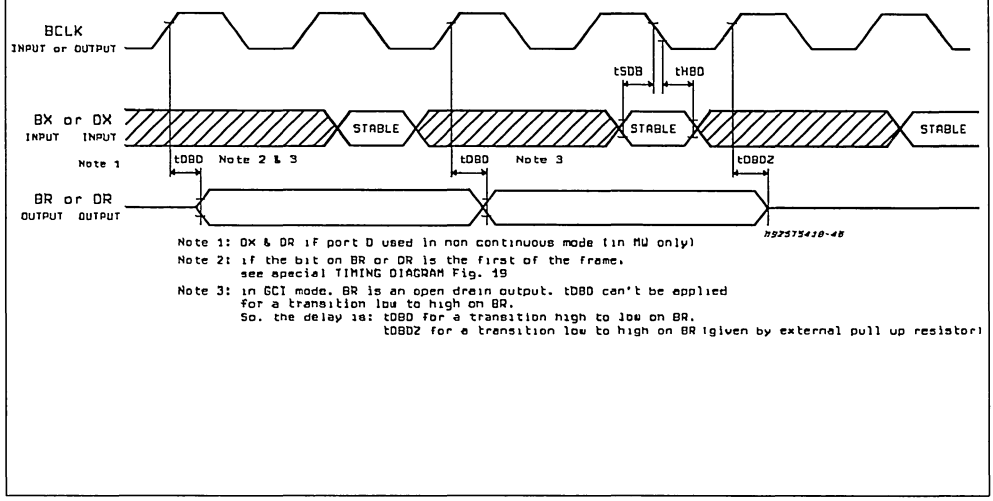
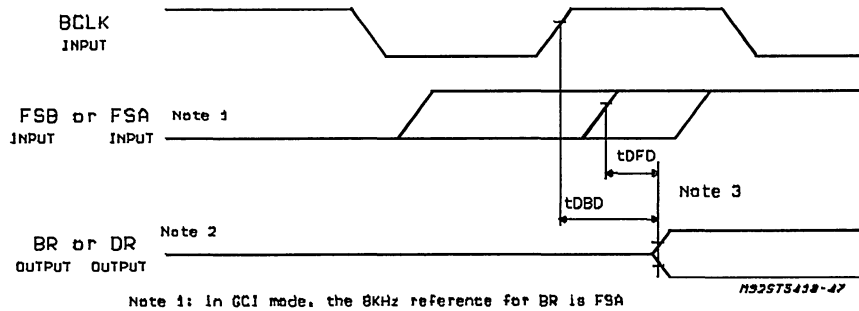


Figure 22: SPECIAL CASE BR, DR, ONLY FIRST BIT OF THE FRAME, IN SLAVE AND NON DELAYED MODES FORMATS 1 3 (MW MODE), FORMAT 4 (MW & GCI MODE)

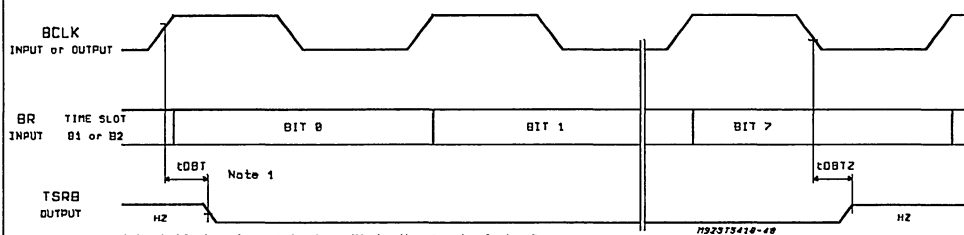


Note 1: in GCI mode, the 8KHz reference for BR is FSA

Note 2: DR can be concerned in format 3 if port D is used in no continuous mode

Note 3: if FSB (or FSA in GCI mode) rises sooner than BCLK rising edge. tDFD is without effect

Figure 23: TSRB, SLAVE & MASTER, DELAYED & NON DELAYED, FORMATS 1 2 3 (MW ONLY)



Note 1: if the time slot B1 or B2 is the first of the Frame, see speciel case TIMING DIAGRAM Fig. 22 when the non delayed mode is selected

Figure 24: TSRB, SLAVE & MASTER, FORMAT 4 ALWAYS NON DELAYED MODE (MW & GCI)

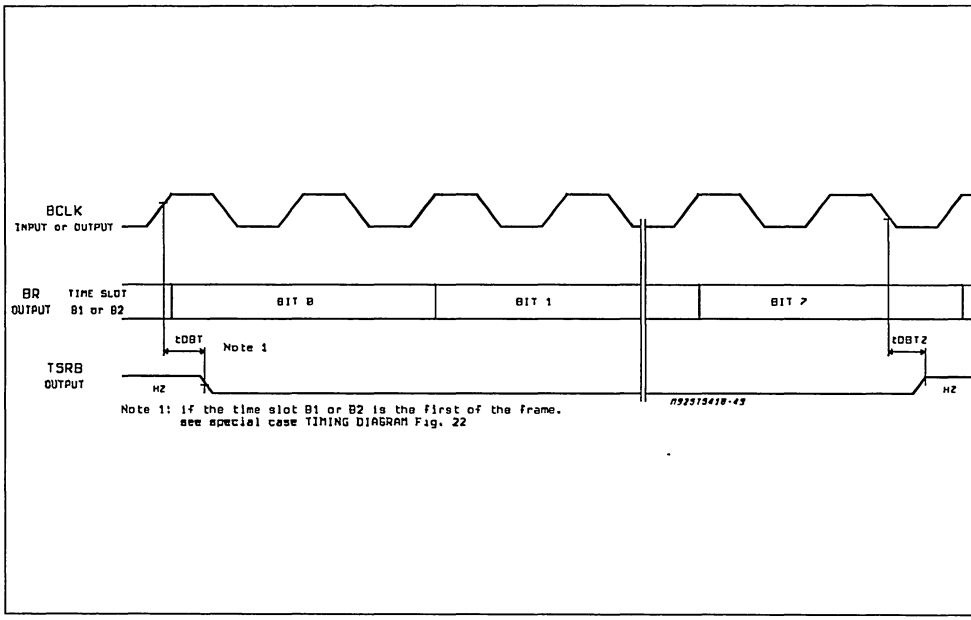


Figure 25: SPECIAL CASE TSRB, B1 OR B2 FIRST CHANNEL OF THE FRAME, IN SLAVE & NON DELAYED MODE, FORMATS 1 3 (MW MODE), FORMAT 4 (MW & GCI MODE)

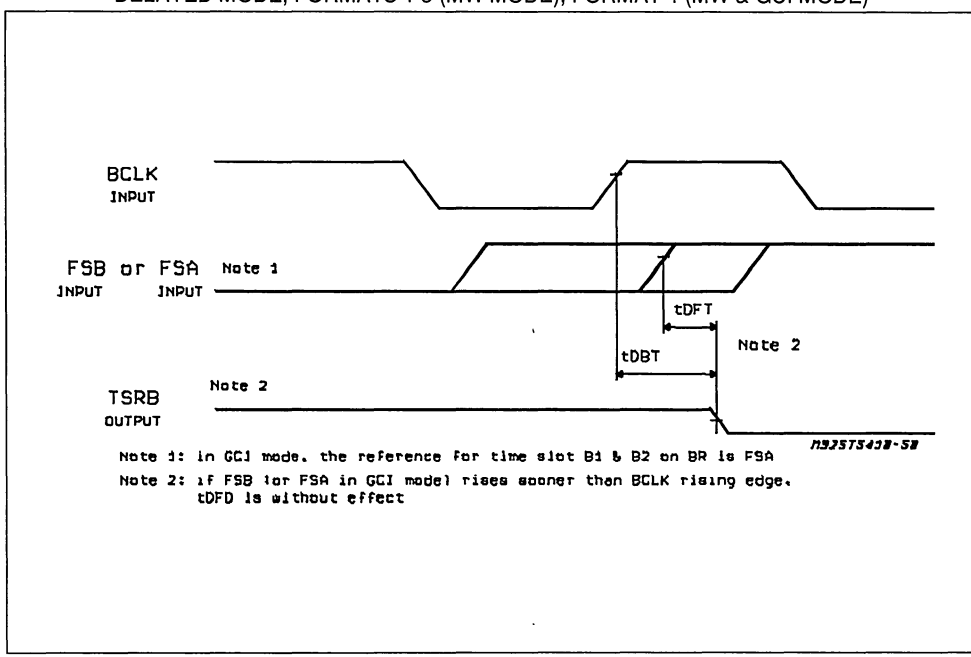


Figure 26: DCLK, DX, DR IN CONTINUOUS MODE SLAVE & MASTER, DELAYED & NON DELAYED MODES ALL FORMATS IN MW MODE ONLY

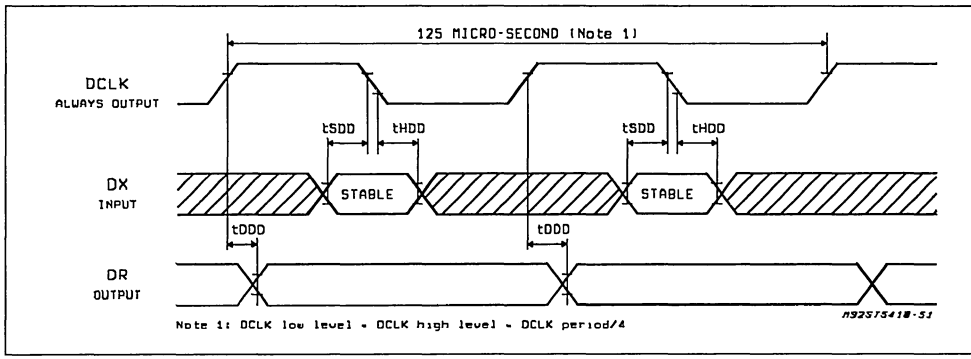


Figure 24: MCLK ALL MODES

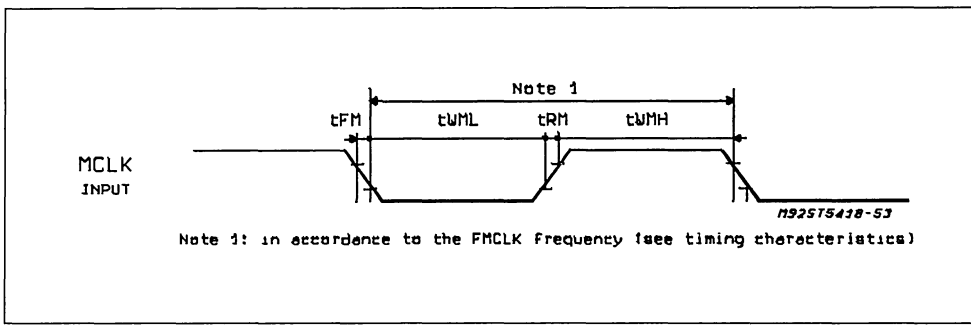


Figure 25: MW PORT Mode A

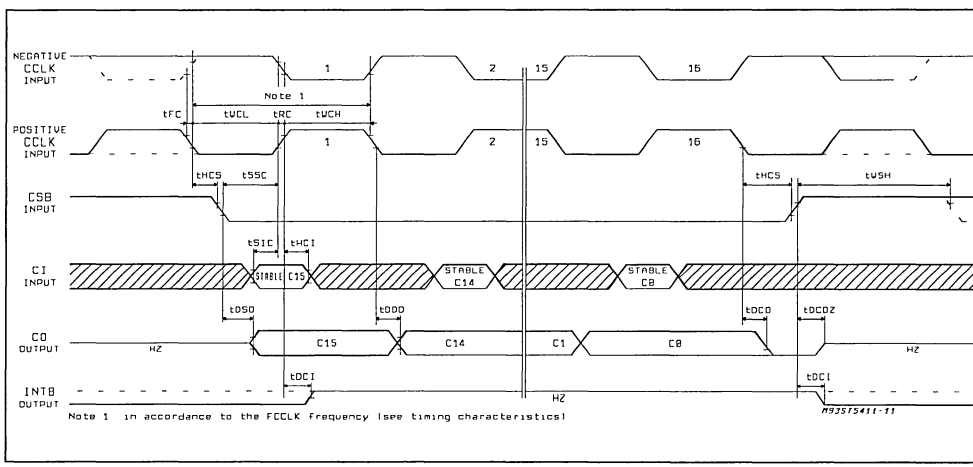
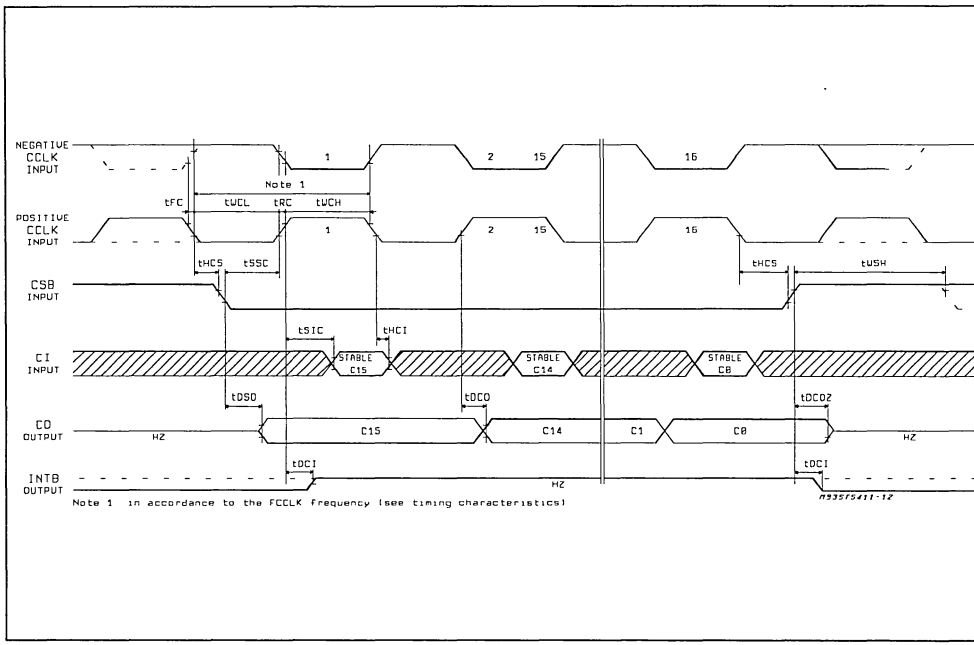


Figure 26: MW PORT Mode B



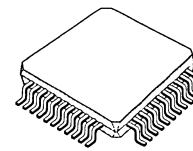
SGS-THOMSON MICROELECTRONICS

STLC5432

2Mbit CEPT & PRIMARY RATE CONTROLLER DEVICE

PRODUCT PREVIEW

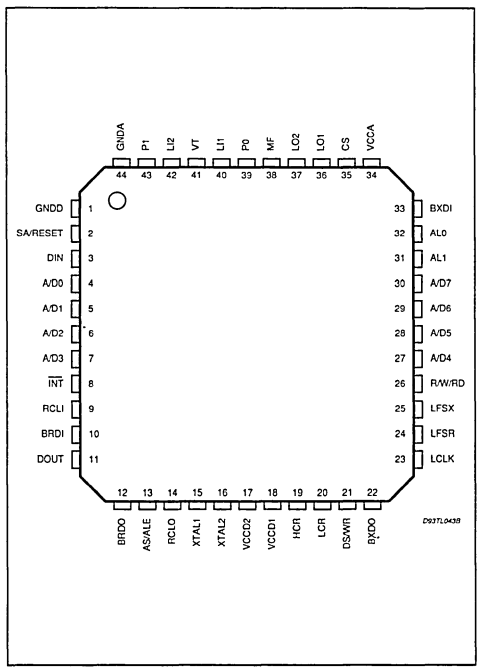
- ONE CHIP SOLUTION FROM PCM BUS TO TRANSFORMER (CEPT STANDARD)
- ISDN PRIMARY ACCESS CONTROLLER (COMPATIBLE WITH ETSI, OPTION 1 AND 2)
- HDB3/BIN ENCODER AND DECODER ON CHIP
- MULTIFRAME STRUCTURE HANDLING
- BUILT IN CRC4
- EASY LINK TO ST5451/MK50H25/MK5027 LINK CONTROLLER.
- REFRAME TIME LESS THAN 0.5ms
- REMULTIFRAME TIME LESS THAN 6ms
- DATA RATE: 2048, 4096 AND 8192 Kb/s FOR MULTIPLEXED APPLICATIONS
- FOUR LOOPBACK MODES FOR TESTING
- PSEUDO RANDOM SEQUENCE GENERATOR AND ANALYZER FOR ON-LINE, OFF-LINE AND AUTOTEST
- RECOVERY CLOCK CIRCUITRY ON CHIP
- 64 BYTE ELASTIC MEMORY FOR TIME COMPENSATION AND AUTOMATIC FRAME AND SUPERFRAME ALIGNMENT
- 25 ON CHIP REGISTERS FOR CONFIGURATIONS, TESTING, ALARMS, FAULT AND ERROR RATE CONTROL.
- AUTO ADAPTATIVE DETECTION THRESHOLD
- AUTOMATIC EQUALIZER OPTION
- 5V POWER SUPPLY



PQFP44 (10 x 10)

ORDERING NUMBER: STLC5432Q

PIN CONNECTION (top view)



DESCRIPTION

STLC5432, CMOS device, interfaces the multiplex system to the physical CEPT Transmission link at 2048Kb/s. Furthermore, thanks to its flexibility, it is the optimum solution also for the ISDN application as PRIMARY RATE CONTROLLER. The receive circuit performances exceeds CCITT Recommendation and the line driver outputs meets the G.703 specifications.
STLC5432 is the real single chip solution that allows the best system flexibility and easy design. STLC5432 can work either in 2048 or 4096 or 8192 Kbit/s systems programming the CR4 register (when parallel micro interface selected).

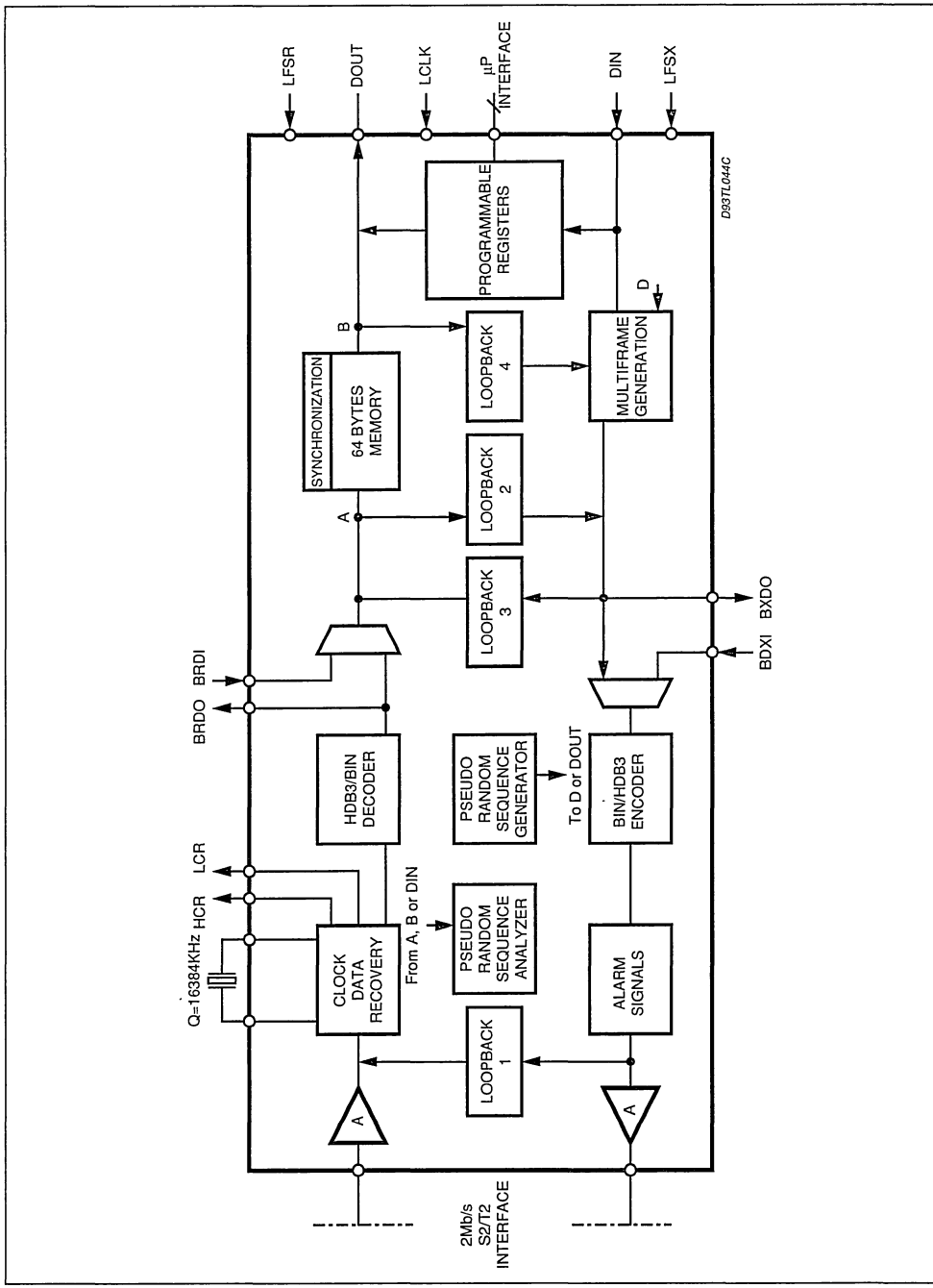
PIN DESCRIPTION

Name	Pin	Type	Function
VCCD1 VCCD2 VCCA	18 17 34	I I I	Positive power supply inputs for the digital (V_{CCD1}) and analog (V_{CCA}) sections and for microprocessor interface signals (V_{CCD2}). They must be +5 Volts and must be directly connected together.
GNDD GNDA	1 44	I I	Negative power supply pins which must be connected together close to the device. All digital and analog signals are referred to these pins, which are normally at the system ground.
LI1 LI2	40 42	I I	Receive HDB3 signal differential inputs from the line transformer.
VT	41	O	Positive power supply output for fixing reference voltage to the receive transformer. Typical value is 2.375V.
L01 L02	36 37	O O	Transmit HDB3 signal differential outputs to the line transformer.When used with an appropriate transformer, the line signal conforms to the output specifications in CCITT with a nominal pulse amplitude of 3 volts for a 120Ω load on line side.
XTAL1	15	I	The master clock input which requires either a parallel resonance crystal to be tied between this pin and XTAL2, or a clock input from a stable source. This clock does not need to be synchronized to the system clock. Crystal specifications = 16 384 kHz ± 50 ppm parallel resonant; RS ≤ 20Ω loaded with 33pF to GND each side.
XTAL2	16	O	The output of the crystal oscillator, which should be connected to one end of the crystal if used.
HCR	19	O	High clock received. When the device has recovered the clock from the HDB3 signal, HCR signal is synchronized to the remote circuit. The HCR frequency is either 8 192 kHz if 8MCR bit of CR1 Register is put to 1 or 4 096 kHz if 8MCR is set to 0.
LCR	20	O	Low clock received. When the device has recovered the clock from the HDB3 signal, LCR signal is synchronized to the remote entity. The LCR frequency is 8 kHz if 8KCR bit is set to 1, or 4 kHz if 8KCR bit is set to 0. When the remote clock is not recovered, HCR and LCR frequency are synchronized to master clock (16 384 kHz). HCR and LCR can be used by the system in Terminal Mode.These two clocks can be used by the transmit function of the device.
BRDO RCLO	12 14	O O	Binary Receive Data Output. 2 048 kbit/s Receive Clock output. 2 048 kHz. After decoding, Binary Data and clock associated are provided for different applications.
BRDI RCLI	10 9	I I	Binary Receive Data Input. 2 048 kbit/s. Receive Clock Input 2 048 kHz.
BXDO	22	O	Binary Transmit Data Output. 2 048 kbit/s. Before encoding Binary Data is provided to different applications (Optical Interface for instance). Local clock is associated to this data.
BXDI	33	I	This binary signal can replace BXD internal signal to be encoded if SELEX bit (CR1 Register) is set to 1.
DOUT	11	O	Data Output. 30 B+D primary access data received from the line.Data can be shifted out from the tristate output DOUT at the LCLK frequency on the rising edges during all the time slots,except Time Slot Zero in accordance with TSOE bit (CR1Register). NB : If parallel micro-interface is selected, DOUT is at high impedance after Reset. DOUT is at low impedance after writing CR4 register.
DIN	3	I	Data Input : 30B+D primary access data to transmit to the line.Data can be shifted in at the LCLK frequency on the falling edges during all the time slots, except Time Slot Zero, in accordance with TSOE bit (CR1 Register).

PIN DESCRIPTION (continued)

Name	Pin	Type	Function
LCLK	23	I	Local Clock : this clock input determines the data shift rate on the two digital multiplexes. This clock frequency can be indifferently 2 048, 4096, 8 192 or 16 384 kHz. Data Out and Data In rate is always 2 048 kbit/s when Serial Interface microprocessor: an internal automatic mechanism divides by two the frequency if 4 096 kHz.
LFSR	24	I	Local Frame Synchronization for the Receiver. This clock input defines the start of the frame on the digital multiplex Data (pin DOUT). This clock frequency can be indifferently 8 kHz or a submultiple of 8 kHz.
LFSX	25	I	Local Frame Synchronization for the Transmitter. This clock input defines the start of the frame on the digital multiplex Data (pin DIN). This clock frequency can be indifferently 8 kHz or a submultiple of 8 kHz. If submultiple of 8 kHz, LFSX defines the start of even frame on DIN. The TSO of this even frame will contain the Frame Alignment Signal (FAS) on the line.
AL0, AL1	32 31	O O	Alarm 0 Output, alarm 1 Output. These pins are open drain outputs which are normally in high impedance state. **AL1** **AL0** **Alarm definitions** Z Z Frame or Multiframe recovered, A bit received is 0. 0Volt Z Frame or Multiframe recovered, A bit received is 1 Z 0Volt Frame and Multiframe lost, AIS Alarm Indication Signal is detected. 0Volt 0Volt Frame and Multiframe lost, AIS Alarm Indication Signal is not detected.
MF	38	I	Multiframe. This pin is an input, connected to 0 Volt, the frame (FAS) is transmitted, the multiframe (MFAS) is not transmitted. If 5 Volt Frame (FAS) and multiframe (MFAS) are transmitted on to the line in accordance with G.704. Receiver is not concerned by this pin.
SA/RESET	2	I	**Stand Alone** : When this pin is connected to 5 Volts, the device works without microprocessor. The configuration is given by the values per default of programmable registers. BRDI and BXDI must not be used. **RESET**: When this pin is put to 5 Volts during 100 ns at least every programmable register is reset (value per default). When this pin is set at zero Volt, the type of microprocessor is selected by P0, P1 pins.
P0, P1	39,43	I	Processor interface. These two input pins define the microprocessor interface chosen. P1 P0 Microprocessor Interface 0 0 Serial Microprocessor Interface 0 1 ST9 Microprocessor Interface 1 0 Multiplexed Motorola processor interface 1 1 Multiplexed Intel processor interface
AS/ALE	13	I	Address Strobe/Address Latch Enable. Input
CS	35	I	Chip Select. A high level on this input selects the PRCD for a read write operation.
R/W/RD	26	I	Read/Write/Read Data. Input.
DS/WR	21	I	Data Strobe/Write Read. Input.
A/D0 to A/D7	4 to 7; 27 to 30	I/O	Address/Data 0 to 7. Input-Output.
$\overline{INT}$	8	O	Interrupt Request. The signal is activated low when the PRCD requests an interrupt. It is an open drain output.

BLOCK DIAGRAM



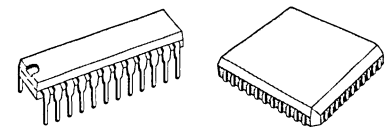
SGS-THOMSON MICROELECTRONICS

STLC5444

QUAD FEEDER POWER SUPPLY

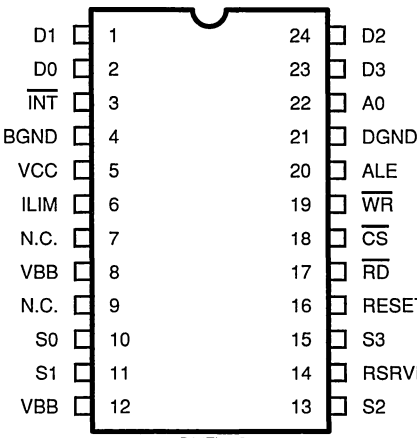
PRODUCT PREVIEW

- SUPPLIES POWER FOR UP TO FOUR DIGITAL TELEPHONE LINES
- CONFORMS TO THE CCITT RECOMMENDATIONS FOR POWER FEED AT THE S OR T REFERENCE POINTS
- SUPPORTS POINT-TO-POINT AND POINT TO MULTIPOINT CONFIGURATIONS
- OPTIONAL USE FOR U-LINE FEEDING (PUBLIC & PRIVATE)
- EACH OF THE FOUR LINES IS INDIVIDUALLY CONTROLLED
- HIGH-VOLTAGE BCD TECHNOLOGY SUPPORTING UP TO -130V
- AUTOMATIC THERMAL SHUTDOWN
- STATUS CONDITION DETECTION (BY MICROPROCESSOR) FOR EACH LINE:
  - Low output voltage
  - Openloop
  - Current overload
  - Thermal overload
  - Normal line condition
- PROGRAMMABLE CURRENT LIMITING
- OUTPUT CURRENT UP TO 120mA



DIP24 PLCC44

DIP24 PIN CONNECTION (Top view)



D94TL102

DESCRIPTION

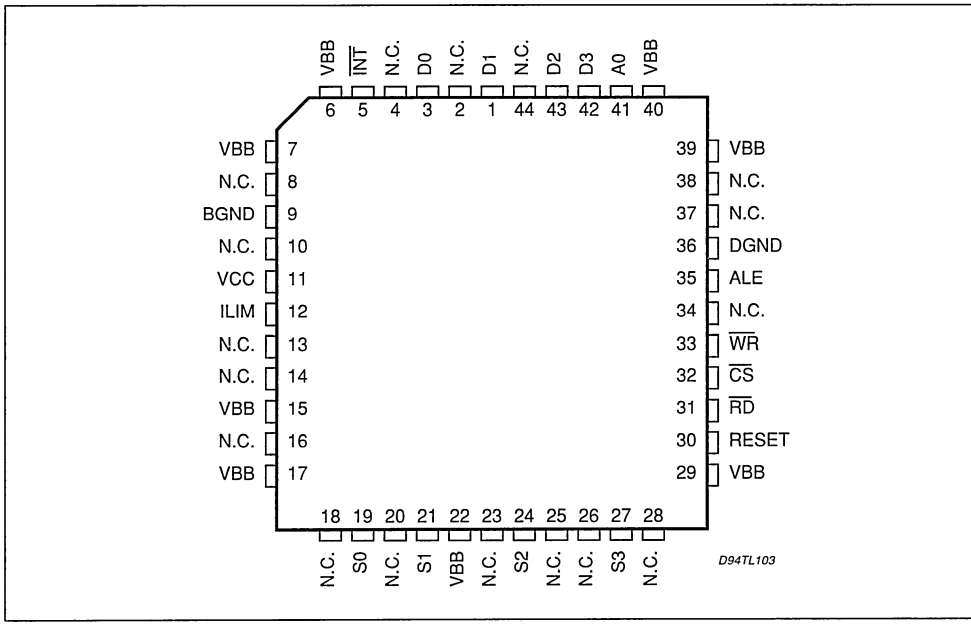
The ISDN Quad Feeder Power Supply (IQFPS) provides a power source for up to four line interfaces. The power source to the device is a local battery or a centralized regulated power supply.
It can operate in point-to-point and point-to-multipoint configurations as far as S interface is concerned.
By the device microprocessor interface, each powered line is individually controlled and monitored.
Therefore, overloads and faults are easy to detect and localize even in a large system.

The status conditions detected by the device on each line that may be read by the microprocessor are :

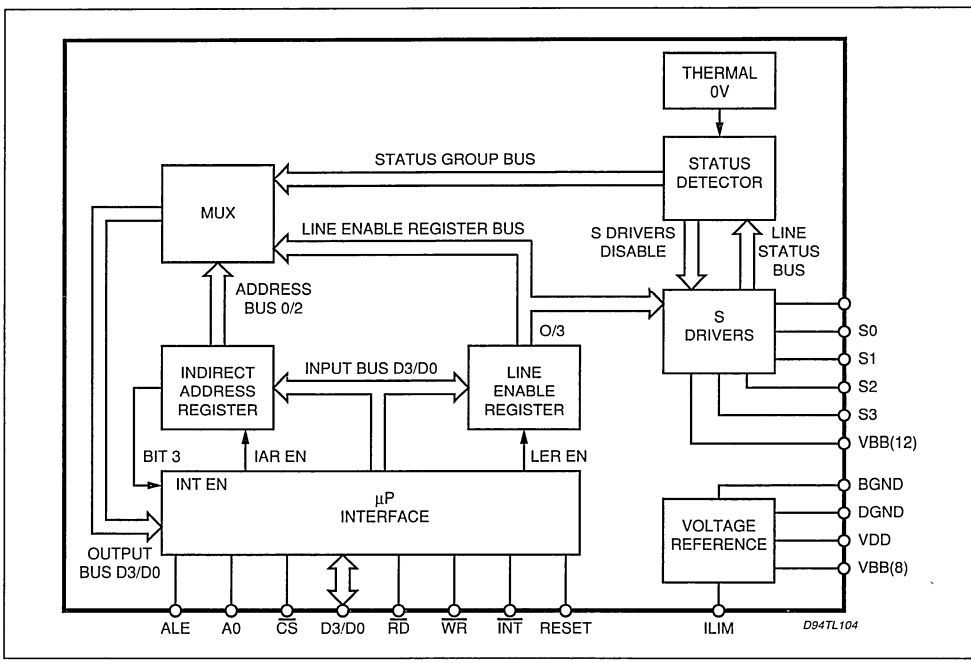
- low output voltage
- openloop
- current overload
- thermal overload
- normal line conditions

A hardware current limiting programmable feature is available.

PLCC44 PIN CONNECTION (Top view)



BLOCK DIAGRAM



PIN DESCRIPTION

Name	N° PLCC	N° DIP	Function
D1	1	1	Bit 1 of the tri state I/O data bus
NC	2,4,8,10, 13,14, 16,18, 20,23, 25,26, 28,34, 37,38,44	7,9	No connection
D0	3	2	Bit 0 of the tri state I/O data bus
$\overline{INT}$	5	3	Active low interrupt output for the µP (open drain)
VBB	6,7 15,17 22,29, 39,40	8,12	Battery supply line (negative battery's terminal)
BGND	9	4	Battery ground line
VCC	11	5	+5V supply line
ILIM	12	6	Current limit programming
S0	19	10	Output of the power switch controller 0
S1	21	11	Output of the power switch controller 1
S2	24	13	Output of the power switch controller 2
RSRVD	–	14	Reserved pin: it must be left floating
S3	27	15	Output of the power switch controller 3
RESET	30	16	Active high reset input
$\overline{RD}$	31	17	Active low read input
$\overline{CS}$	32	18	Active low chip select input
$\overline{WR}$	33	19	Active low write input
ALE	35	20	Active high address latch enable
DGND	36	21	Digital ground
A0	41	22	Address bit for R/W operations on the data bus
D3	42	23	Bit 3 of the I/O tri state data bus
D2	43	24	Bit 2 of the I/O tri state data bus

FUNCTIONAL DESCRIPTION

ADDRESS LINE (Input)

A0 selects source and destination locations for read and write operations on the data bus. A0 must be valid on the falling edge of ALE or during RD and WR if ALE is tied High.

ALE - Address Latch Enable (Input; Active High)

ALE is an input control pulse used to strobe the address on the A0 line into the address latch. This signal is active High to admit the input address. The address is latched on the High-Low transition of ALE. While ALE is High, the address latch is transparent. For an unmultiplexed microprocessor bus, ALE must be tied High.

BGND - Ground Battery

CS - Chip Select (Input; Active Low)

CS must be Low to enable the read or write operations of the device. Data transfer occurs over the D3-D0 lines.

D3-D0 - DATA BUS (Input/Output; Three-State, Active Low)

The four bidirectional data bus lines are to exchange information with a microprocessor. D0 is the least significant bit and D3 is the most significant bit. A High on the data bus corresponds to a logical 1. These lines act as input when WR and CS are active and as output when RD and CS are active. When CS is inactive, the D3-D0 pins are placed in a high-impedance state.

DGND - Ground Digital

ILIM - Current Limit Programming (Input)

ILIM programs the current limit of the Output drivers using an external resistor connected between ILIM and VBB. The ILIM pin is 1.25V more positive than VBB. The current limit is 5mA plus 1000 times the current in the external resistor. The programmed current limit applies to each driver.

INT - Interrupt (Output; Open-Collector, Active Low)

INT augments the Microprocessor Interface by generating an interrupt when a Current Overload Detector (COD) occurs. INT is active whenever any bits in the COD register are active. INT is not latched; when the COD register is zero, INT goes inactive (High). INT will also go inactive if the IQFPS automatically disables the S-output driver that caused the interrupt (due to Thermal Overload), or if the microprocessor disables that line via the Line Enable Register (LER). COD interrupts can be masked via the Indirect Address Register (IAR); RESET always disables the INT pin.

RD - Read (Input; Active Low)

The active Low read signal is conditioned by CS and transfers internal information to the data bus. If A0 is a logical 0, logic levels of the Indirect Address Register (IAR) and Thermal Shutdown Status bit will be transferred to D3-D0. If A0 is a logical 1, the data addressed by the IAR will be transferred to D3-D0.

RESET - Reset (Input; Active High)

RESET initialize the registers in the device, leaving the drivers switched off.

S3-S0 - Drivers (Output)

S3-S0 each supply power to one line. The outputs can sink up to 120 mA each. The voltage at the line is connected to VBB through a DMOS switch.

VBB - Battery Voltage (input)

VBB is the internal negative supply voltage. VBB must always be connected to the most negative supply voltage. The MPI Registers will not function properly when the battery power is disconnected, that is, when VBB is floating or grounded. The IQFPS should also be reset if a drastic transient is applied to VBB.

VCC - +5V Power Supply (Input)

WR - Write (Input; Active Low)

The active Low write signal is conditioned by CS and transfers information from the data bus to an internal register selected by A0. If A0 is a logical 1, D3-D0 is written into the Line Enable Register (LER). If A0 is a logical 0, D3-D0 is written into the IAR. LER and IAR are the only two writable registers in the device.

DC CHARACTERISTICS (T_{amb} = 25°C; V_{BB} = -54V; V_{CC} = 5V; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input Voltage High Level		2			V
V_{IL}	Input Voltage Low Level				0.8	V
I_{OH}	High Level Output Current	V_{OH} = 2.4V	400			µA
I_{OL}	Low Level Output Current	V_{OL} = 0.4V	2			mA
I_{IH}	High Level Input Current	V_{IH} = 2V			10	µA
I_{IL}	Low Level Input Current	V_{IL} = 0.8V			60	µA
I_{OZH}	Z High Level Output Current	2.4V < V_{OZ} < V_{CC}			10	µA
I_{OZL}	Z Low Level Output Current	0V < V_{OZ} < 0.4V			10	µA
I_{CC}	V_{CC} supply Current		1.6		5	mA
C_L	Logic I/O Capacitance			10		pF
V_{SAT}	Saturation Voltage	I_S = 80mA			2	V
I_{BB}	V_{BB} Supply Current	V_{BB} = -54V, R_{LIM} = 31.2KΩ	1.4		4	mA
I_{SLIM}	Limit Current	R_{LIM} = 31.2KΩ, V_{BB} = -96V R_{LIM} = 10.9KΩ, V_{BB} = -54V	40.5 102	45 120	49.5 138	mA mA
V_{LVD}	Low Voltage Detector Threshold (relative to V_{BB})	S3 - S0 output active	2.7	3	3.3	V
I_{SOL}	Current Overload Detector Threshold (as % of I_{SLIM})		75	85	95	%
I_{SOC}	Open Loop Detector Threshold		2	3	4	mA
I_{SZ}	Si Leakage Current to ground @ Si disabled	V_{BB} = -110V			100	µA
H_{LVD}	Low Voltage Detector Hysteresis			18		mV
H_{OLD}	Open Loop Detector Hysteresis			0.6		mA
H_{COD}	Current Overload Detector Hysteresis			2.4		mA
H1	130°C Thermal Detector Hysteresis			10		°C
H2	160°C Thermal Detector Hysteresis			10		°C
T_{H1}	Thermal Overload Recovery Time H1			80		µs

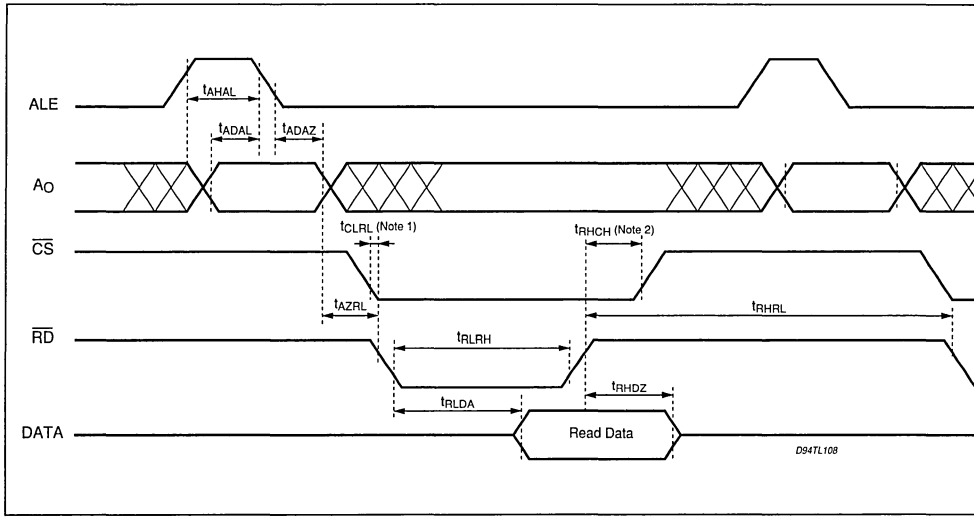
SWITCHING CHARACTERISTICS (T_{amb} = 25°C; V_{BB} = -54V; V_{CC} = 5V; unless otherwise specified)

MICROPROCESSOR READ/WRITE TIMING (for references see figure 1 and 2).

Symbol	Parameter	Min.	Max.	Unit
t_{RLRH}	RD, CS pulse width	200		ns
t_{RHRL}	RD, recovery time	200		ns
t_{RLDA}	RD, CS low to data available		200	ns
t_{RHDZ}	RD or CS high to data Z		110	ns
t_{AHAL}	ALE pulse width	60		ns
t_{ADAL}	Address setup time	60		ns
t_{ADAZ}	Address hold time	30		ns
t_{AZRL}	Address Z to RD low	0		ns
t_{WLWH}	WR or CS pulse width	200		ns
t_{WHWL}	Write recovery time	200		ns
t_{DAWH}	Data setup time	100		ns
t_{WHDZ}	Data hold time	20		ns
t_{RES}	Reset Pulse with	200		ns

Note: AC timings are tested at 0.8V and 2V with input levels of 0.4V and 2.4V.

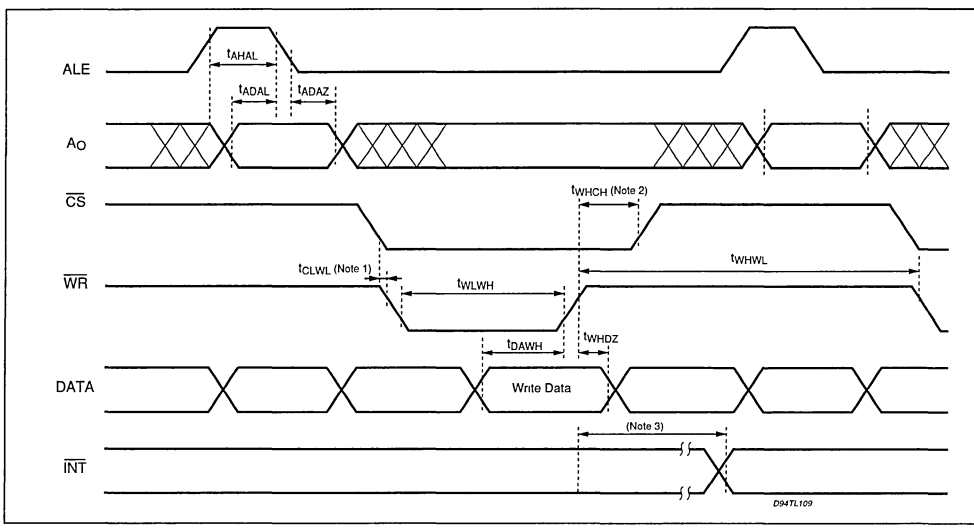
Figure 1: Microprocessor Read Timing.



Notes:
1 - If t_{CLRL} is negative, t_{RHRL}, t_{RLRH}, t_{AZRL}, and t_{RLDA} are measured from $\overline{CS}$ rathar than $\overline{RD}$.
2 - If t_{RHCH} is negative, t_{RHRL}, t_{RLRH} and t_{RHDZ} are measured from $\overline{CS}$ rather than $\overline{RD}$

When a read from the LER immediately follows a write to the LER a minimum of 1 µs is required between these operations

Figure 2: Microprocessor Write Timing.



Notes:
1 - If t_{CLWL} is negative t_{WHWL} and t_{WLWH} are measured from $\overline{CS}$ rathar than $\overline{WR}$.
2 - If t_{WHCH} is negative, t_{WHWL}, t_{WLWH}, t_{DAWH} and t_{WHDZ} are measured from $\overline{CS}$ rather than $\overline{WR}$.

The propagation delay from the writing of the T/I bit to the effect on the $\overline{INT}$ pin is approximately 1µs for both mask and enable operations.

OPERATIVE DESCRIPTION.

Initialization

The device is initialized by the RESET pin. In this state the analog drivers are switched off, the Indirect Address Register (IAR) is cleared, and the internally latched address A0 is cleared.

Power at Output drivers

The voltage at the Output drivers is approximately VBB (less VSAT).

Analog Section

The analog section consists of four line drivers, which are saturated DMOS transistor switches capable of sinking up to 120 mA each. The power to the drivers is derived from the negative supply voltage (VBB). The output voltage to each line is slaved to VBB, and the voltage drop in each driver is approximately 1.5V.

Line driver protection is provided through the integration of current limit and over-temperature shut-off. The current limit is hardware-programmable via an external resistor (RLIM) connected between ILIM and VBB.

The output limit is : 5mA + 1000 x 1.25V/RLIM.

This 1000 x gain makes the ILIM pin susceptible to external noise, care should be taken to connect RLIM as close as possible to the component.

The thermal shut-off is internally set at approximately 160°C.

At this temperature all the drivers are unconditionally switched off. However, at approximately 130°C, only the drivers that are in the current-overload condition will be turned off.

Status detectors, associated with each of the line drivers, monitor the load conditions on each line by comparing an electrical parameter (e.g., current and voltage at the line) with reference level. The output of each detector can be read by the microprocessor. In addition to these status detectors, the temperature of the device is monitored via integrated temperature detectors. The detectors respond at approximately 130°C and 160°C, as defined above, and the 160°C detector can be monitored by the microprocessor via the MPI. The status detectors provide the following information from each of the lines (all detectors have built-in hysteresis) :

*) Low Output Voltage Detection

The low-output-voltage status bit becomes active when the output DMOS transistor is pulled out of its linear region.

*) Open Loop Detection

The open-loop status bit becomes active when the current on the line drops below a minimum value.

*) Current Overload Detection

The current-overload status bits become active when the current on the line nears the current limit. These bits active the INT output if COD interrupts are enabled via the IAR Register.

*) Thermal Overload Detection

If the device temperature reaches 130°C, then all the line drivers in the current-overload condition will be switched off and the corresponding bits in the Thermal Overload Register will be cleared. If the device temperature increases to 160°C, all the line drivers will be turned off, and all the bits in the Thermal Overload Register will be cleared.

The T-bit will also be set, and it can be read along with the Indirect Address Register (IAR) to indicate that all the drivers have been turned off. To initialize any of the bits in the Thermal Overload Register, the microprocessor must first turn off the line drivers that must not be reactivated until the T-bit in the address register is cleared by the temperature detector in the device.

MPI Section

The MPI allows the user to access the detectors defined in the analog section. The line driver's status bits are grouped by function. Bits 3-0 of the detectors correspond to lines 3-0, respectively.

The status group are :

- Low Voltage Detector (LVD)
- Open Loop Detector (OLD)
- Current Overload Detector (COD)
- Thermal Overload Register (TOR)

The data is not latched in these status groups except in the TOR.

Thus, the user should filter (multiple samples) the received data to ensure its integrity. There are two other registers in the MPI: the indirect Address Register (IAR), and Line Enable Register (LER).

The IAR contains 3 bits that address the desired status group or the LER. The IAR is read along with the T-bit defined in the analog section. The microprocessor can read the IAR to check the validity of the address. A 1us delay is required between a write to the LER register, followed by a Read of the same register. Subsequent reads of the LER do not have this constraint.

The LER is used to enable or disable the individual line drivers. The line drivers will only become active if the corresponding bit in the TOR is inactive. The LER is a read/write register.

The MPI is the interface containing the following pins :

D3-D0	Bidirectional	Data Bus
A0	Input	Address Line
ALE	Input	Address Latch Enable
$\overline{RD}$	Input	Read Enable
$\overline{WR}$	Input	Write Enable
$\overline{CS}$	Input	Chip Select
$\overline{INT}$	Output	COD Interrupt
RESET	Input	Reset pin

The 4-bit bidirectional data bus (D3-D0) is used to communicate with the registers. Access to the registers is controlled by CS, RD, WR, ALE, and A0 as shown below. A read or write cycle must be preceded by a valid A0. A0 is latched internally in a transparent latch by ALE. The selection of the status group or the LER is determined by the content of the IAR.

The truth table for the MPI control is shown below :

CS	RD	WR	A0	
0	1	0	0	Write IAR (T bit is read only)
0	0	1	0	Read IAR and T bit
0	1	0	1	Write LER
0	0	1	1	Read status groups or LER
1	X	X	X	No access

Indirect Address Register (IAR) and T/I Bit

The IAR is 3 bits wide and accessible through the data port, D2-D0. The content of the Indirect Address Register (IAR2-IAR0) determines the selection of the status groups or the LER. The thermal overload bit T/I is read and written at the same time as IAR and occupies D3.

This register has the following format :

Bit	Symbol	
0	IARO	Bit 0 of the IAR
1	IAR1	Bit 1 of the IAR
2	IAR2	Bit 2 of the IAR
3	T/I	T bit: (Read only) Logical 0: temperature normal (default value) Logical 1: temperature above 160°C (all drivers shut off) I bit : (write only) Logical 0: INT pin disabled Logical 1: COD interrupts enabled via INT pin

IAR2-IAR0 address the status groups and the LER as shown below:

IAR2	IAR1	IAR0	Select
0	0	0	LVD
0	0	1	OLD
0	1	0	COD
0	1	1	LEC
1	0	0	RESERVED
1	0	1	RESERVED
1	1	0	LER
1	1	1	TOR

The contents and format of the status groups and the LER are as follows :

LVD:

Bit	Logical 1	Logical 0 (default value)
0	O0 low voltage	O0 voltage normal
1	O1 low voltage	O1 voltage normal
2	O2 low voltage	O2 voltage normal
3	O3 low voltage	O3 voltage normal

LEC:

Bit	Logical 1	Logical 0
0	SWITCH ON	SWITCH OFF
1	SWITCH ON	SWITCH OFF
2	SWITCH ON	SWITCH OFF
3	SWITCH ON	SWITCH OFF

The Line Enable Command (LEC) indicates the status of the DMOS SWITCH OUTPUT.

The Low Voltage Detector (LVD) indicates the voltage level on the output lines, even when the lines are disabled. The low-voltage condition becomes active (logical 1) if the output reaches the Low Voltage Threshold (VLVD).

OLD:

Bit	Logical 1	Logical 0 (default value)
0	O0 open loop	O0 current normal
1	O1 open loop	O1 current normal
2	O2 open loop	O2 current normal
3	O3 open loop	O3 current normal

The Open Loop Detector (OLD) indicates the open-loop condition on the output lines. The open-loop condition becomes active (logical 1) if the current on the line drops below the threshold value ISOC.

COD:

Bit	Logical 1	Logical 0 (default value)
0	O0 current overload	O0 current normal
1	O1 current overload	O1 current normal
2	O2 current overload	O2 current normal
3	O3 current overload	O3 current normal

The Current Overload Detector (COD) indicates the current-overload condition on the output lines. The overload condition becomes active (logical 1) if the output current approaches the value programmed by an external resistor between ILIM and VBB.

TOR :

Bit	Logical 1 (default value)	Logical 0
0	O0 operational	O0 off
1	O1 operational	O1 off
2	O2 operational	O2 off
3	O3 operational	O3 off

The Thermal Overload Register (TOR) contains the overload status of the output line drivers. If the device temperature reaches 130°C, then the output line drivers that are in the current-overload condition will be switched off. The corresponding bits in the TOR will be set to a logical 0. To initialize any of the bits in the TOR, the microprocessor must first turn off the output line drivers via the LER. However, the TOR bits cannot be deactivated if the 160°C detector is active. The Up may re-enable the output drivers via the LER after the TOR condition is removed. The TOR is a read-only register.

LER :

Bit	Logical 1	Logical 0 (default value)
0	O0 on	O0 off
1	O1 on	O1 off
2	O2 on	O2 off
3	O3 on	O3 off

The Line Enable Register (LER) is used to enable or disable the individual output line drivers. The output line will only become active if the corresponding bit in the TOR is set to a logical 1. The LER can be written directly and read indirectly.

ABSOLUTE MAXIMUM RATINGS (T_A = 0°C to 70°C)

Parameter	Value
Voltage from Digital Input to DGND	-0.4V to V_{CC}
Voltage from V_{CC} to DGND	-0.4V to +7V
Voltage from V_{BB} to DGND	-110V to +0.4V
100ns Pulse voltage from Si to DGND (See Notes)	-130V to +2V
Voltage from BGND to DGND	+0.5V, -3V
Storage Temperature	T = -60°C to +150°C

Note : Si stands for O0, O1, O2 or O3 outputs.

RECOMMENDED OPERATING CONDITIONS

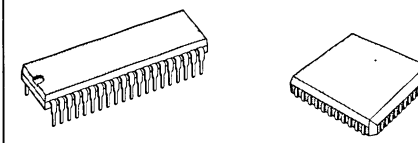
Parameter	Symbol1	Min.	Max.	Units
Ambient Temperature	T_A	0	70	°C
Supply Voltage	V_{CC}	4.75	5.25	V
	V_{BB}	-110	-38	V
	DGND	0	0	V
	BGND	-3	+0.5	V

Note: The test condition is specified with a diode in series with V_{BB}.

LINE CARD INTERFACE CONTROLLER

PRODUCT PREVIEW

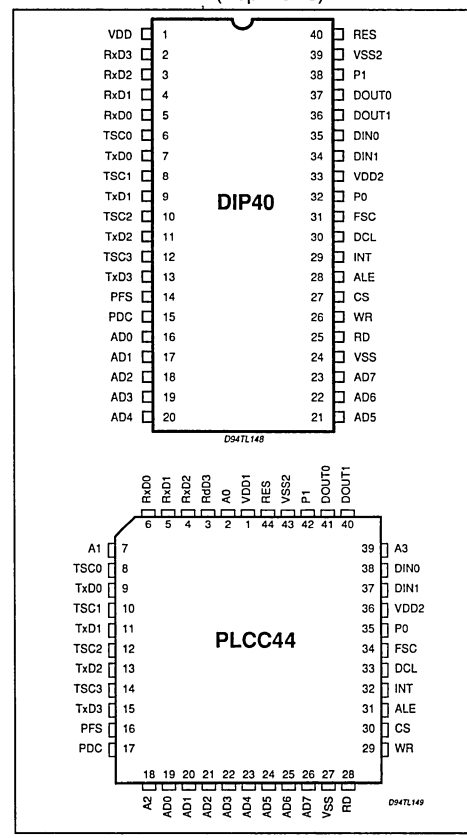
- BOARD CONTROLLER FOR UP TO 16 ISDN LINES OR 16 VOICE SUBSCRIBERS.
- TWO SERIAL INTERFACES :
  -PCM Four bidirectional multiplexes
  -GCI One (or two) at 2 Mb/s.
- NON BLOCKING SWITCH FOR 128 CHANNELS (16, 32 OR 64 KB/S BANDWIDTH).
- N CONSECUTIVE 64 kb/s CHANNELS FROM AN INPUT MULTIPLEX CAN BE SWITCHED AS A SINGLE N X 64 kbit/s CHANNEL TO AN OUTPUT MULTIPLEX AT 2048 kb/s.
- TIME SLOT ASSIGNMENT FREELY PROGRAMMABLE FOR EVERY CONNECTED SUBSCRIBER.
- PROGRAMMABLE PCM DATA RATES UP TO 8192 kb/s.CONSTANT DATA RATE AT 2 Mb/s ON GCI SIDE.
- PCM interface :
  - Simple and double clock frequency selectable;.
  - Programmable clock shift
  - Tristate mode control signals for external drivers.
- GCI interface :
  - Six bits or four bits Command/indicate channel selectable for analog or digital equipment
  - Command/Indicate Monitor channels validated or not
- Microprocessor access to two selected bidirectional channels of GCI and/or PCM.
- Multicontrollers for layer 1 functions :
  - C/I protocol controller for up to 16 C/I channels
  - Monitor protocol controller for up to 16 Monitor channels.
- Standard microprocessor interface with multiplexed address/data bus or separate address data buses.
- DIP40 PINS & PLCC44 pins PACKAGES



DIP40 **PLCC44**

ORDERING NUMBER: STLC5460

PIN CONNECTIONS (Top views)



DESCRIPTION

The Line Card Interface Controller, STLC5460, is a monolithic switching device for the path control of up to 128 channels of 16, 32, 64 kbps bandwidth. Two consecutive 64 kbps channels may also be handled as a quasi single 128 kbps channel. For these channels, the LCIC performs non-blocking space time switching between two serial interfaces, the system interface (or PCM interface) and the general component interface (GCI).

PCM interface can be programmed to operate at different data rates between 2048 and 8192 kbps. The PCM interface consists of up to four duplex ports with a tristate indication signal for each output line. The GCI interface can be selected to be PCM interface at 2Mbit/s.

The LCIC can be programmed to communicate with GCI compatible devices such as STLC3040 (SLIC), STLC5411 (U interface), ST5421 (S interface) and others. The device manages the layer 1 protocol buffering the Command/Indicate and Monitor channels for GCI compatible devices.

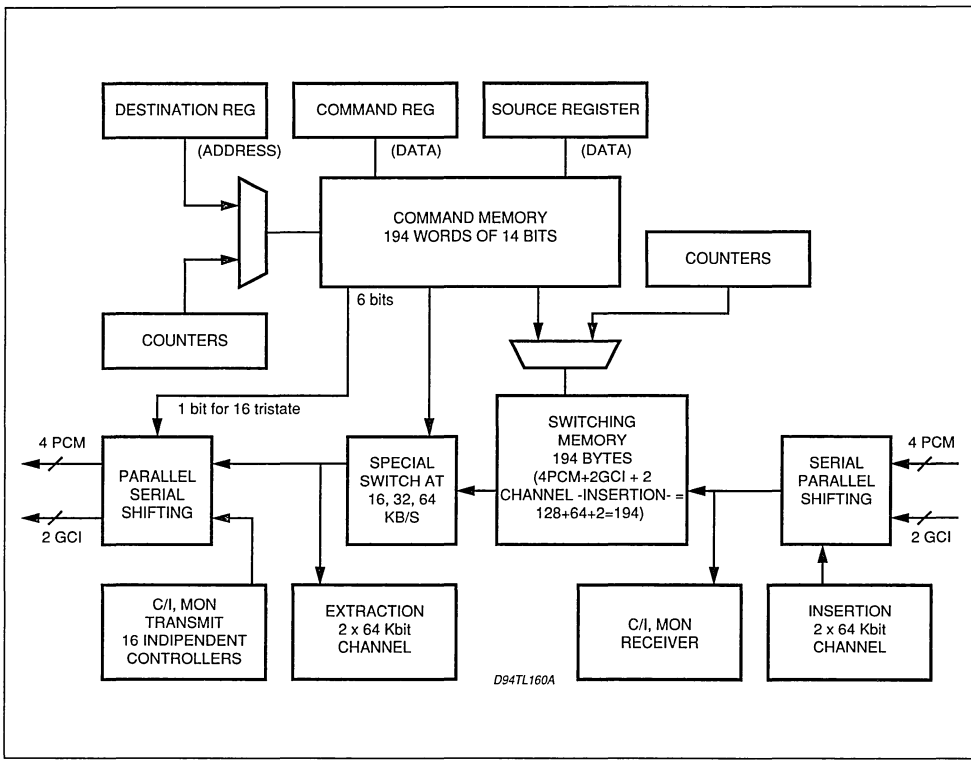
Due to its capability to switch channels of different bandwidths, the STLC5460 can handle up to 16 ISDN subscribers with their 2B+D channel structure in GCI configuration, or up to 16 analog subscribers. Since its interfaces can operate at different data rates, the LCIC is an ideal device for data rate adaption between PCM interface up to 8Mb/s and GCI at 2Mb/s.

Moreover, STLC5460 is one of the key building blocks for networks either with central, decentral or mixed signaling and packet data handling architectures associated with ST5451 (HDLC controller).

STLC5460 is available in a DIP40 or a PLCC44 package.

The DIP40 version is controlled by a standard 8 bit parallel microprocessor interface with a multiplexed address-data bus. In the PLCC 44 package, the device may optionally be controlled by separate address and data buses.

BLOCK DIAGRAM



PIN DEFINITIONS AND FUNCTIONS

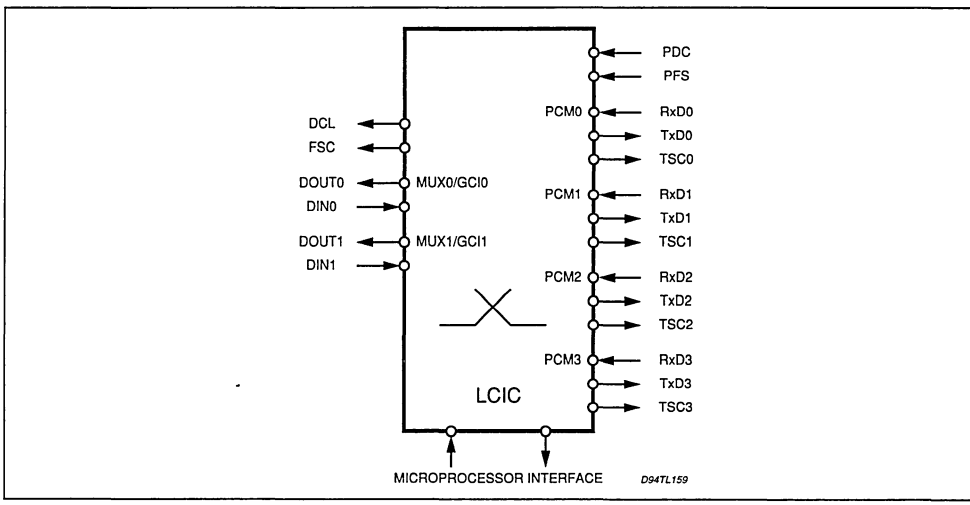
Symbol	Pin N DIP	Pin n PLCC	Type (*)	Function
VDD1	1	1	I	Supply Voltage 5V, ±5% .
A0	-	2	I	Address Bus Bit 0 : internal register address bus, bit 0.
RxD3 RxD2 RxD1 RxD0	2 3 4 5	3 4 5 6	I	Receive PCM interface Data : Serial data is received at these lines at standard TTL or CMOS levels.
A1	-	7	I	Address Bus Bit 1 : internal register address bus, bit 1.
TSC0 TSC1 TSC2 TSC3	6 8 10 12	8 10 12 14	OD	Tristate control for the PCM interface. These lines are low when the corresponding TxD outputs are valid.
TxD0 TxD1 TxD2 TxD3	7 9 11 13	9 11 13 15	O	Transmit PCM interface Data : Serial data is sent by these lines at standard TTL or CMOS levels. These pins can be tristated.
PFS	14	16	I	PCM interface frame synchronization pulse.
PDC	15	17	I	PCM interface data clock, single or double rate.
A2	-	18	I	Address Bus Bit 2 : internal register address bus, bit 2.
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	16 17 18 19 20 21 22 23	19 20 21 22 23 24 25 26	I/O	Address Data Bus. If the multiplexed address/data P interface bus mode is selected these pins transfer data and commands between the P and the STLC5460. If a demultiplexed mode is used, these bits interface with the system data bus.
VSS1	24	27	I	Ground : 0V
RD	25	28	I	Read : The signal indicates a read operation, active low.
WR	26	29	I	Write : This signal indicates a write operatin, active low.
CS	27	30	I	Chip select. A low on this line selects the STLC5460 for a read/write operation.

(*): (I) Input
(O) Output
(IO) In/Output
(OD) Open Drain

PIN DEFINITIONS AND FUNCTIONS (continued)

Symbol	Pin N DIP	Pin n PLCC	Type	Function
ALE	28	31	I	Address latch enable. In the Intel type multiplexed P interface mode a logical high on this line indicates an address of a STLC5460 internal register on the external address/data bus. In the Intel type demultiplexed P interface mode, this line is hardwired to VSS, in the demultiplexed Motorola type P interface mode it should be connected to VDD.
INT	29	32	OD	Interrupt line, active low.
DCL	30	33	0	Data clock output.
FSC	31	34	O	Frame synchronization output.
PO	32	35	I	P0 associated to P1 selects the microprocessor interface (Motorola, Intel, ST9)
VDD2	33	36	I	Power supply : 5V
DIN1	34	37	I	GCI Data input 1
DIN0	35	38	I	GCI Data input 0
DOUT1	36	40	O	GCI Data Output 1
DOUT0	37	41	O	GCI Data Output 0
A3	-	39	I	Address Bus Bit 3 : Internal register address bus, bit 3..
P1	38	42	I	P1 associated to P selects the microprocessor interface (Motorola, Intel or ST9).
VSS2	39	43	I	Ground.
RES	40	44	I	Reset. A logical high on this input forces the STLC5460 into the reset state

Figure 1: GCI and PCM Interfaces.



LINE CARD APPLICATIONS

STLC5460 is designed both for digital and analog line card architectures.

It supports up to 16 ISDN subscribers or 16 voice subscribers. The level 1 devices are connected to ST5451 circuits to perform the D channel handling.

Analog Line Card

In analog line cards STLC5460 controls the signalling voice and data path of 64 kb/s channels.

In combination with STLC3040 and ST5451, it allows to perform an optimized line card architecture.

STLC5460 controls configuration of STLC3040 and transmits/receives signalling from the STLC3040.

Digital Line Card

In digital line cards STLC5460 controls configuration of Level 1 circuits (U or S Interface) by means MON channel configuration and performs activation/deactivation by means of Command/Indicate protocol. STLC5460 switches the B channels and can switch the D channels if the channel processing is centralized.

FUNCTIONNAL DESCRIPTION

PCM INTERFACE

The PCM Interface Registers configurate the data transmitted or received at the PCM port for:

- one PCM, the maximum data rate is 2048kb/s with four PCM ports (PCM Mode 0).
- one PCM, the maximum data rate is 4096kb/s with two PCM ports (PCM Mode 1).
- one PCM, the maximum data rate is 8192kb/s with one PCM port (PCM Mode 2).

The clock frequency of PDC is equal to or twice the data rate.

The rising edge of PFS signal is evaluated to determine the first bit of the first time slot of the frame. The length of PFS pulse is one bit-time at least and the length between two pulses is also one bit time.

After reset, STLC5460 is synchronized after two consecutive correct PFS pulses. Synchronization is lost by the device if the PFS signal is not repeated with the correct repetiton rate which has been stored by the circuit at the beginning of synchronization reserch.

LSYNC bit (interrupt register) at "1" indicates the synchronous state, a logical 0 shows that the synchronism has been lost.

Without programming the bit shift function of the PCM interface, the rising edge of the PFS signal marks the first bit of input and output PCM frame.

The Time Slot structure may be shifted using IPOF, OPOF and CPOF registers. The relation between the framing signal PFS and the bit stream is controlled by the contents of these registers. These registers denote the number of bit times, the PCM frame is shifted.

GCI INTERFACE

The Monitor Channel and the Command/Indicate channel may be validated or not. If not validated, the B3 and B4 channels become standard channels at 64 kb/s.

Command/Indicate channel if validated may be configurated with four bits for digital cards or six bits for analog cards.

The clocks (Bit clock and frame clock) are delivered by the device with double rate clocking or simple rate clocking

GCI		PCM			
Double clock DCL kHz	Data kb/s	PDC Clock (kHz)		Data rate kb/s	Mode
		Simple	Double		
4.096	2.048	2.048		2.048	Mode 0
4.096	2.048		4.096	2.048	Mode 0
4.096	2.048	4.096		4.096	Mode1
4.096	2.048		8.192	4.096	Mode 1
4.096	2.048	8.192		8.192	Mode 2
4.096	2.048		16.384	8.192	Mode 2

FSC and DCL are output signals derived from PFS and PDC which are input signals.

MEMORY STRUCTURE AND SWITCHING

The STLC5460 contains two memories, the Control Memory (CM) and Data Memory (DM).

Data Memory buffers the data input from the PCM interface and the data input from the GCI interface. Data Memory has a capacity of 128 + 64 time slots to buffer 4 PCM frame of 32 time slots and two GCI interfaces. It is written periodically once every 125µs controlled by the input counter associated to PCM interface and by the input counter associated to GCI interface. Data Memory is also used to perform the switching function and loopbacks.

The Control Memory has a capacity of 128 + 64 locations of 8 bits of control memory data and 6 bits of control memory code. The 14 bits are written via microprocessor interface and read cyclically under the control of the output counter associated to PCM interface and under the control of the output counter associated to GCI interface. The description of command register describes the different capabilities: switching at 64kb/s, 32kb/s, 16kb/s, loopback and also extraction/insertion from the microprocessor interface.

MICROPROCESSOR INTERFACE

The STLC5460 provides interface signals for Motorola type, Intel type and ST9 microprocessors. In the Intel type P interface mode either a multiplexed or a demultiplexed bus structure may be chosen.

For a demultiplexed bus structure the PLCC 44 package needs to be used, since only this package provides the additional lines of a separate 4 line address bus.

The ALE line of STLC5460 is used to control the bus structure and interface type. ALE is fixed to +5V for the Motorola type P interface and it is switching to signal an address or data transfer in the multiplexed Intel type P interface mode. Pins 28 and 29 of the PLCC package are interpreted as RD and WR for an Intel type interface or DS and R/W for a Motorola type interface.

For memory access, three registers are provided.

The destination register contains the address of a specific location of control memory; the source register contains the data (to be written or read) of the control memory. The control register contains the code (6 bits to be written or read) of the control memory.

A memory access using the actual command register and source register is performed upon every destination register write access. The processing of the memory access takes at most 488 ns.2.5.

EXTRA CHANNELS C/I AND MON CHANNELS

The Command/indicate and Monitor channels can be validated or not.

If validated, the C/I and MON protocol controllers operate and it is not possible to use this channels for switching.

If not validated, the protocols are inhibited and the channels can be used for switching.

COMMAND/INDICATE PROTOCOL

One configuration bit indicates the number of bits of the primitive (four or six bits) for all the channels. Eight (or sixteen) C/I channels are implemented.

To transmit a primitive into one of 16 channels, the primitive (4 or 6 bits) is loaded into source register and the C/I channel number is loaded into destination register with W/R bit of command register at "1".

With the same content in the destination register, the reading of the source register contains 4 (Or 6) last significant bits of the primitive which has not been transmitted yet, transmitted once, twice or more (two more significant bits).

To receive one primitive from sixteen channels, the process is the following :

An interrupt is generated when a new primitive has been received twice identical. Receive Number C/I Register contains the number of C/I channels (4 bits) and Auxiliary Memory contains the primitive received.

Moreover, the microprocessor can read directly the 16 primitives which have been received and stored into the Receive C/I Memory. To read this memory, Source Register contains the number of Receive C/I channel and destination register contains the primitive (4 or 6 bits) with a seventh bit which indicates whether the primitive has been received one or twice identical.

MONITOR CHANNEL PROTOCOL

Sixteen Monitor channels are implemented. To transmit message of one (or more) words, the first (and the next) is loaded into source register and the number of MON channels into destination register with W/R bit of Command Register at 1.

This byte is transmitted if BYTE Bit of Command Register is at 1.

To receive Message from sixteen Monitor channels, the process is the following : an interrupt is generated when a new byte has been received twice identical.

Receive Number Register contains the number of MON channels (4 bits) and receive data Monitor Channel Memory contains the last word received. The remote transmitter will transmit the next word after this register is read by the local microprocessor.

INSERTION - EXTRACTION

This capability allows to insert data to GCI interface and to PCM interface and to extract data from GCI interface and from PCM interface. This data is provided either by the microprocessor or by an internal Pseudo Random Sequence Generator.

INSERTION

Two programmable registers (Insert A and B) contain the data to insert into two outputs time slots continuously. To perform an insertion, four registers are programmed by the microprocessor.

- Insert A and/or B Registers for the data to insert.
- The Destination Register to indicate the output PCM or GCI interface and the number of Time Slot selected.
- If necessary, the Command Register to insert into 64 kb/s, 32 kb/s or 16 kb/s channel.

if two insertions are validated with two consecu-

tive time slots, a 128 kb/s channel is performed. When the data is inserted, status bit (INS) is put at logical 1. An interrupt is also generated.

EXTRACTION

Two programmable registers (Extract A and B) contain the data extracted from two input time slots. To perform an extraction, three registers are programmed by the microprocessor :

- Extract A and/or B Registers for the data extracted.
- The Source register to indicate the input PCM or GCI interface and the number of Time Slot selected. if two insertions are validated with two consecutive time slots, data at 128 kb/s is extracted. When the data is loaded in Extract A or Extract B Register, Status Bit (EXT) is put at logical 1. An interrupt is also generated.

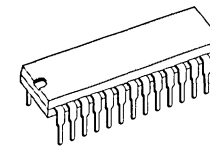
SGS-THOMSON MICROELECTRONICS

STU2071

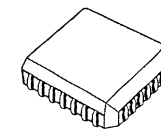
4B3T U INTERFACE CIRCUIT

PRELIMINARY DATA

- 4B3T TWO-WIRE U INTERFACE CIRCUIT FOR LT AND NT APPLICATION
- 120 kbaud LINE SYMBOL RATE (120 SYMBOLS PER FRAME)
- SCRAMBLER AND DESCRAMBLER ACCORDING TO CCITT REC V.29
- BARKER CODE (11 SYMBOLS) SYNCHRONIZATION WORD
- UNSCRAMBLED 1 KBIT/S HOUSEKEEPING CHANNEL
- ADAPTIVE ECHO CANCELLATION WITH TRANSVERSAL FILTERING
- ADAPTIVE DECISION FEEDBACK EQUALIZATION
- AUTOMATIC GAIN CONTROL
- PDM AD CONVERTER
- AUTOMATIC ACTIVATION AND DEACTIVATION WITH POLARITY ADAPTION
- AUTOMATIC CODE VIOLATION DETECTION
- POWER FEED UNIT CONTROL
- ADVANCED CL3 1.5µm CMOS PROCESS
- 28 PIN DUAL-IN-LINE PLASTIC PACKAGE
- V* DIGITAL INTERFACE



DIP28
ORDERING NUMBER: STU2071B1



PLCC28
ORDERING NUMBER: STU2071FN

SYSTEM OVERVIEW

STU2071 (UIC) provides two transparent 64 kbit/s B channels, a transparent 16 kbit/s D channel, a transparent 1 kbit/s service channel and a 1 kbit/s maintenance channel for loop and error messages on subscriber lines.

UIC enables full duplex continuous data transmission via the standard twisted pair telephone cable. Adaptive Echo cancellation is used to restore the received data. An equalizer, done with an adaptive filter, restores the data which are distorted by the transmission line.

The coefficient of the equalizer and echo canceller are conserved during a power down. An all digital PLL performs both bit and frame synchronization.

The analog front end consists of receive path RX and transmit path TX, providing a full duplex analog interfacing to the twisted pair telephone cable. Before data are converted to analog signals, they pass through a digital filter (TX-filter) to reduce the high frequency components. After D/A conversion the signal is amplified and sent to the hybrid.

The received signal is converted back to digital data and passed through the RX matching filter to restore the line signal. The A/D convertor is a second order sigma/delta modulator which operates with a clock of 15.36 MHz. After timing recovery, achieved by a digital PLL, the received signal is equalized, in an adaptive digital filter, to correct for the frequency and group delay distortion of the line.

Power supply status can be read via PFOFF. The UIC can disable its power supply (DISS), and two relay drivers outputs are provided (accessible via B2*) to control the power feed unit (RD1,RD2).

PIN CONNECTION (Top view)

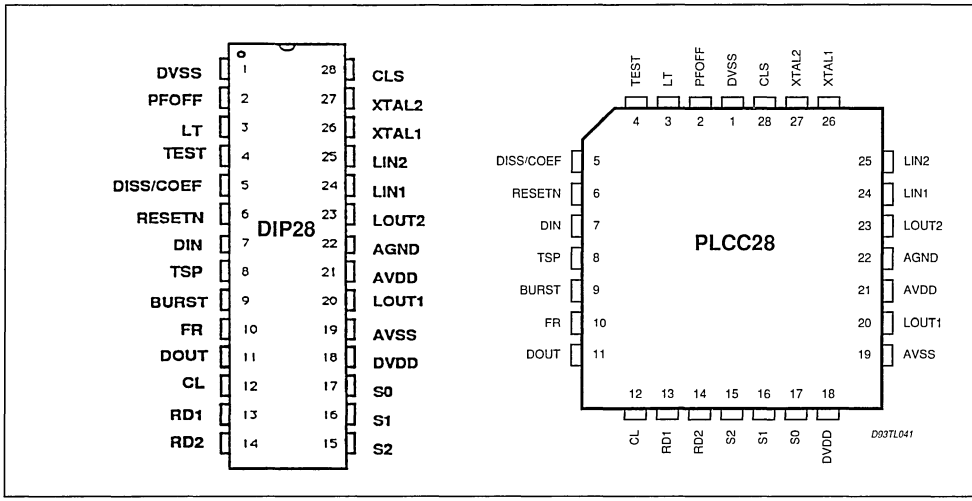
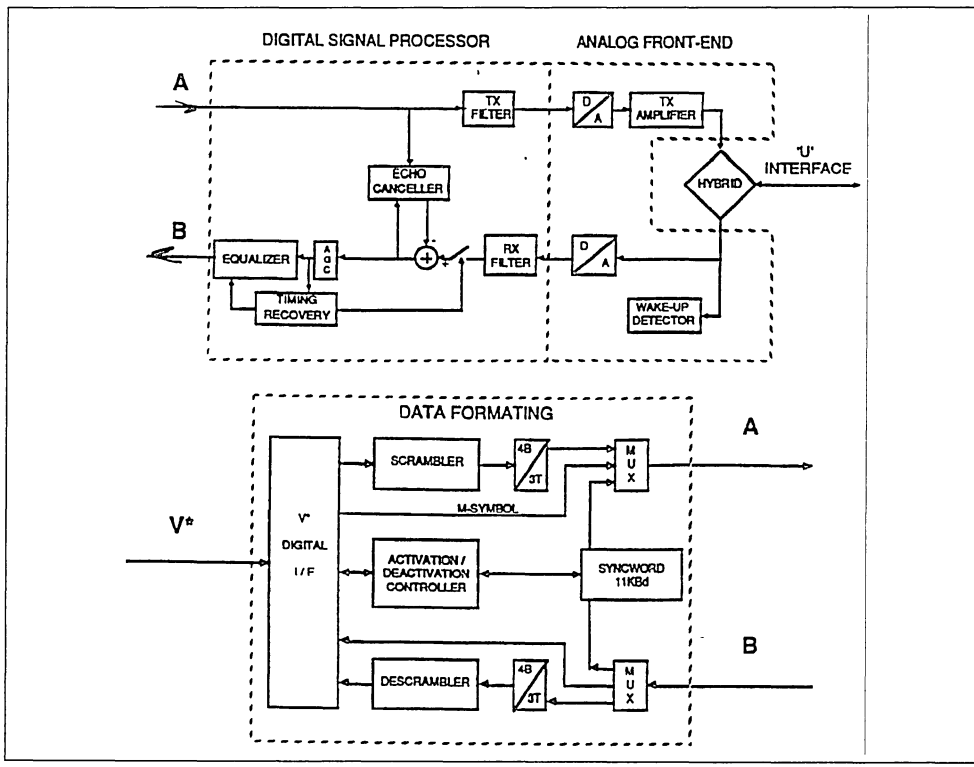


Figure 1: UIC Schematic Block Diagram



PIN DESCRIPTION

Pin	Name	Function
1	DVSS(input)	Digital Ground.
2	PFOFF(input)	Power feed off. PFOFF=HIGH is coded by the A-bit indication HI accessible on DOUT. Active in LT mode only.
3	LT(input)	LT/NT mode selection.
4	TEST(input)	Test Mode.
5	DISS(output)	A bit channel driven pin. Active in LT mode only.
6	RESETN(input)	Hardware Reset.
7	DIN(input)	Digital interface input.
8	TSP(input)	Transmit single pulse. 1 KHz single pulse alternating positive and negative polarity is transmitted.
9	BURST(input)	Burst mode selection. Active in LT mode only.
10	FR(in/out)	8KHz Digital interface frame clock; input in LT and output in NT mode.
11	DOUT(output)	Digital interface output.
12	CL(in/out)	Digital interface bit clock; input in LT and output in NT mode.
13	RD1(output)	Power feeder relay driver.
14	RD2(output)	Power feeder relay driver.
15, 16, 17	S2,S1,S0	Time slot pin strap (. Active in LT mode only.
18	DVDD(input)	5V +/-5% positive digital power supply.
19	AVSS(input)	Analog Ground.
20	LOUT1(output)	Output to the line.
21	AVDD(input)	5V +/-5% positive analog power supply.
22	AGND(input)	Analog Ground.
23	LOUT2(output)	Output to the line.
24,25	LIN1,LIN2(input)	Inputs from the line (UK0).
26, 27	XTAL1,XTAL2(inputs)	System clock input;nominal frequency is 15.36MHz.
28	CLS(output)	Clock output synchronous to the line receive clock at 7.68MHz.

APPLICATION AND MODES

The UIC can be used in LT, LT-burst and in NT mode.

Hereafter a list of the pin bias to set up the desired mode is given.

In LT mode:

Pins	Value
LT	1
BURST	0
S0	0
S1	0
S2	0

In LT burst:

Pins	Value
LT	1
BURST	1
S0	time slot
S1	time slot
S2	time slot

In NT:

Pins	Value
LT	0
BURST	0
S0	0
S1	0
S2	1

Test pins should always be tied to GND

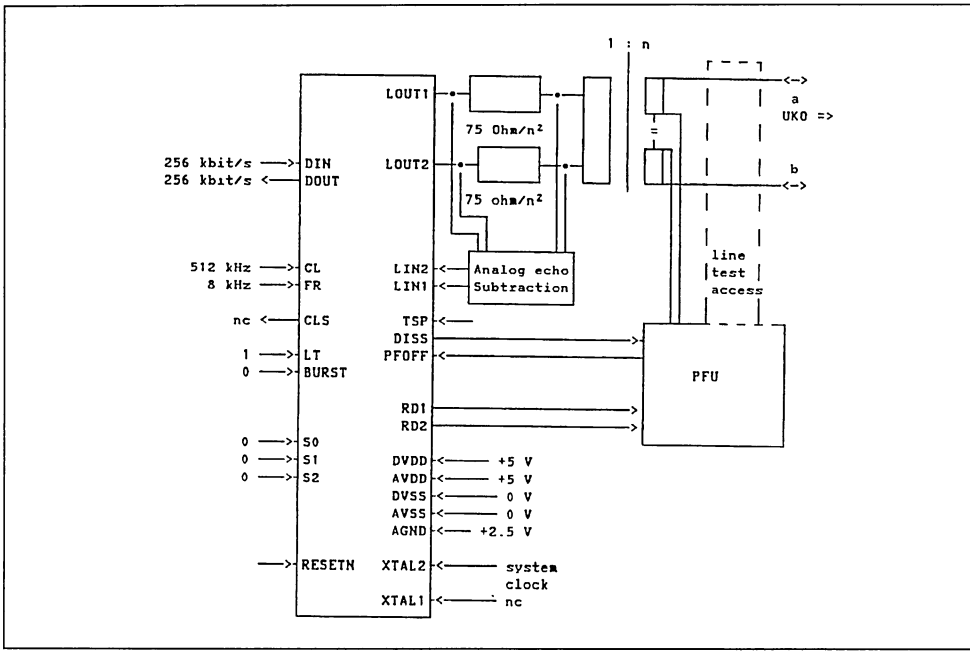
MODE DEPENDENT FUNCTIONS

PIN		MODE				
		LT burst	NT	LT	LTRP	NTRP
LT	input	1	0	1	0	0
BURST	input	1	0	0	0	0
S2, S1, S0	input	static	1 0 0	0 0 0	0 0 1	0 1 0
DIN DOUT	input output	2048 kbit/s	256 kbit/s	256 kbit/s	256 kbit/s	256 kbit/s
CLS (MHz)	output	7.68	7.68	7.68	–	7.68
CL (KHz)	input output	4096 –	– 512	512 –	512 –	– 512
FR (KHz)	input output	8 –	– 8	8 –	8 –	– 8

RECOMMENDED APPLICATIONS

LT mode

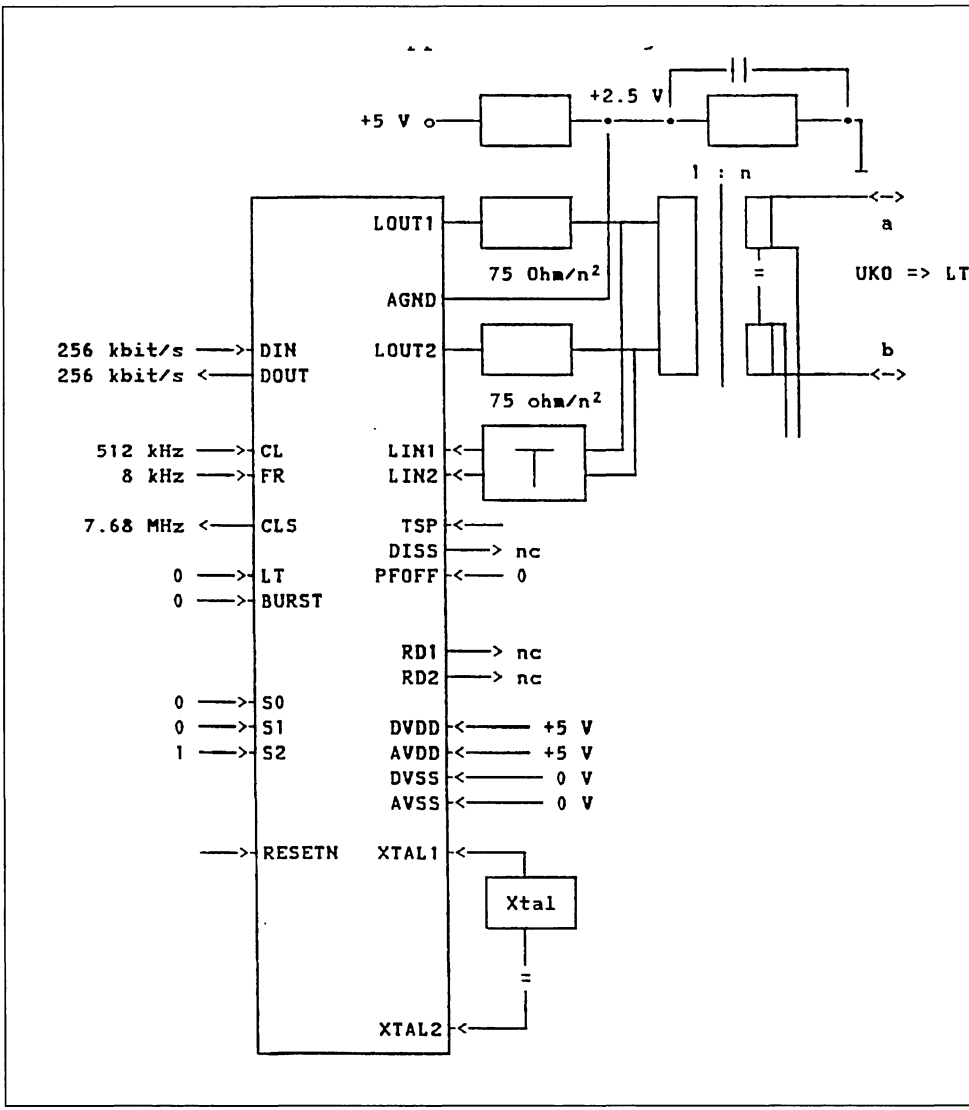
Figure 2: LT Schematic Application Diagram



DIN:	Data input, datarate = 256 kbit/s, continuous
DOUT:	Data output, datarate = 256 kbit/s, continuous
CL:	Data clock input, f = 512 KHz
FR:	Frame clock input, f = 8 KHz (1:1)
XTAL2:	System clock input, f = 15.36 MHz (Tx clock synchronous to system clock)
CLS:	Clock output, 7.68 MHz

NT mode

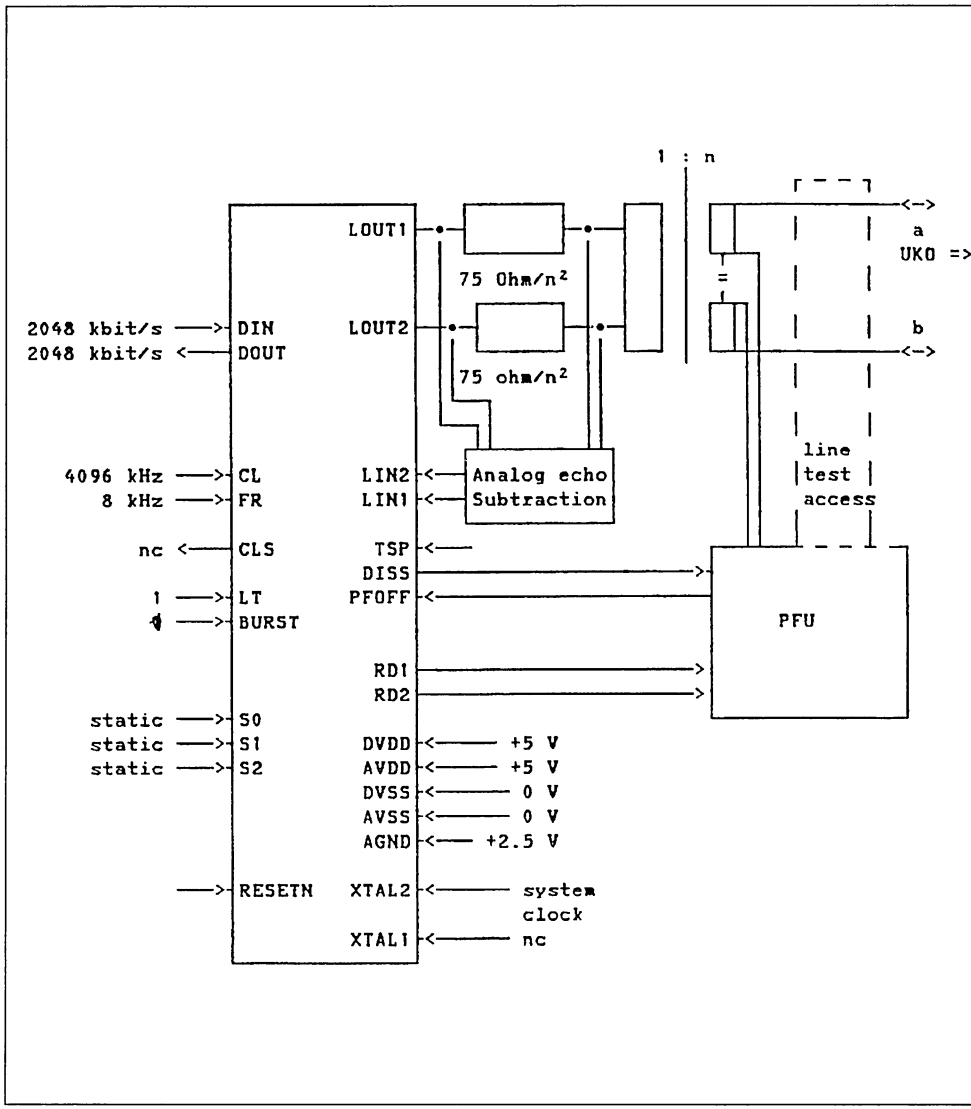
Figure 3: LT Schematic Application Diagram



DIN:	Data input, datarate = 256 kbit/s, continuous
DOUT:	Data output, datarate = 256 kbit/s, continuous
CL:	Data clock input, f = 512 KHz
FR:	Frame clock input, f = 8 KHz (1:1)
XTAL1/2:	15.36 MHz Xtal connection (Clock not synchronous to system clock)
CLS:	Clock output, 7.68 MHz (used to synch S interface)

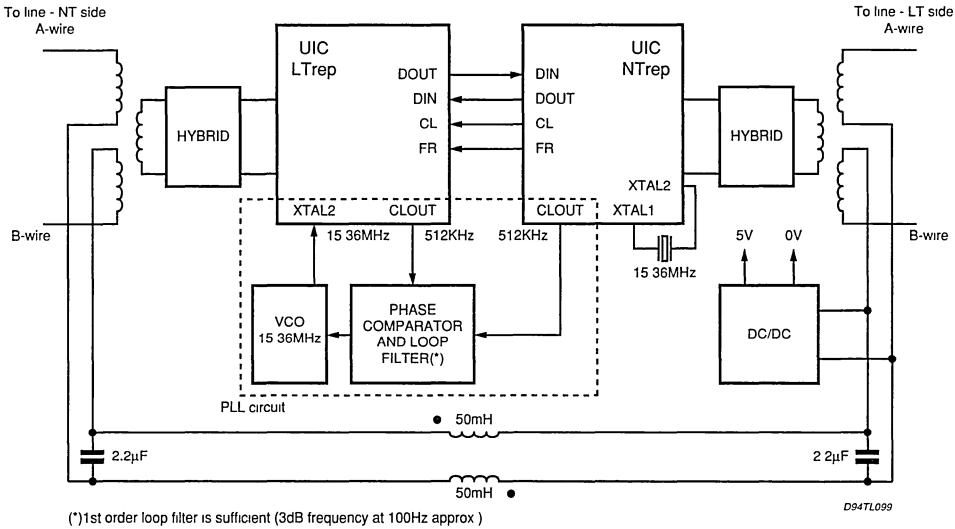
LT burst mode

Figure 4: LT Burst Mode Schematic Application Diagram.



DIN:	Data input, datarate = 2048 kbit/s, continuous
DOUT:	Data output, datarate = 2048 kbit/s, continuous
CL:	Data clock input, f = 4096 KHz
FR:	Frame clock input, f = 8 KHz (1:1)
XTAL2:	System clock input, f = 15.36 MHz (Tx clock synchronous to system clock)
CLS:	Clock output, 7.68 MHz

Figure 5: Repeater Block Diagram.



DIGITAL INTERFACE

UIC is provided with a digital serial interface, named V*, which operates in two modes.

In Fig. 6 the frame format for both modes is shown.

The base frame consists of:

B1 : 64 kbit/s transparent data channel
B2 : 64 kbit/s transparent data channel
B2* : Monitor channel
B1* : 8 bits so set
D1/D2 : 16 kbit/s D channel
A1..A4 : Command/Indicate channel
T : Transparent service channel
E : Extension bit

In Fig. 7 and 8 the timings in Continuous and in Burst mode are given.

B2* available messages (do not use in REPETER modes):

Code	Function
74H	Set RD1 to HIGH
75H	Set RD2 to HIGH
76H	Set RD1 and RD2 to HIGH
77H	Reset RD1 and RD2 to LOW
EFH	Reset frame error counter
(F0-FF)H	NOD
All others	Not defined

In Fig. 7 and 8 the timings in Continuous and in Burst mode are given.

Figure 6: V* Frame Format.

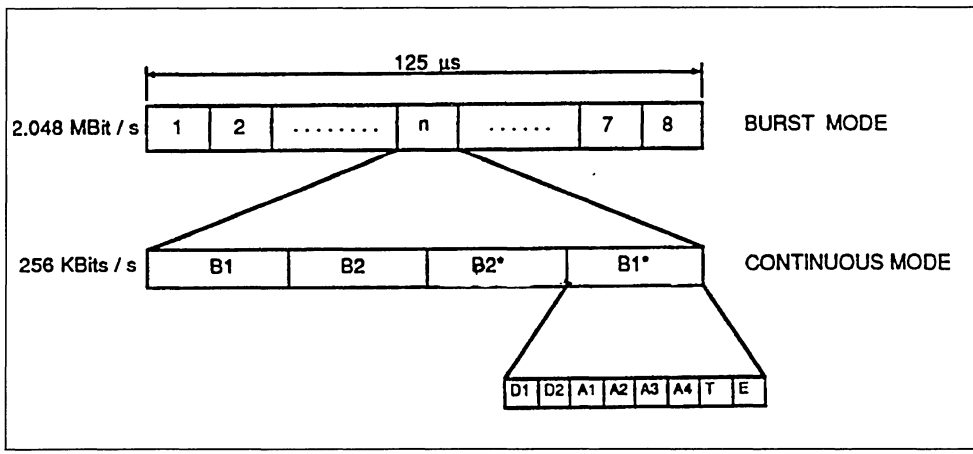


Figure 7: Continuous Mode.

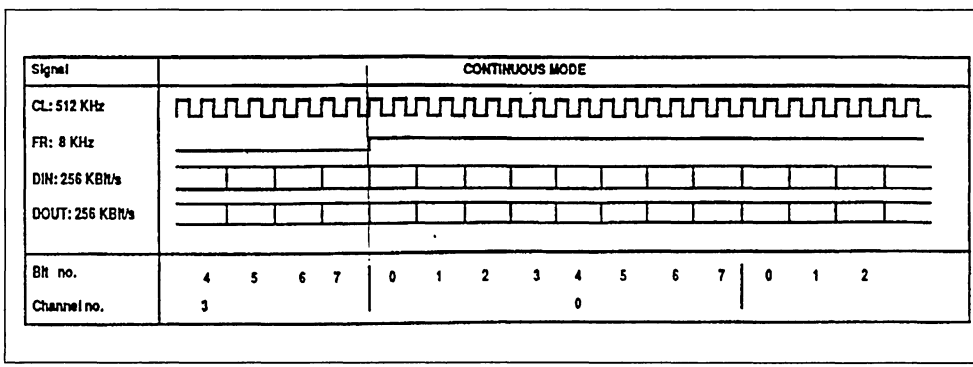
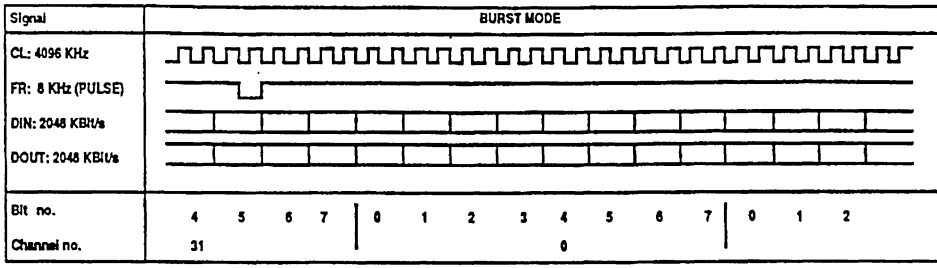


Figure 8: Burst Mode.



LINE FRAME STRUCTURE.

The information flow across the subscriber line uses the frame structure here below. The length of one frame corresponds to 120 ternary symbols being transmitted within 1 ms.

1	2	3	4	5	6	7	8	9	10	11	12		
T1	T1	T1	T1	T1	T1	T1	T1	T1	T1	T1	T1		
T1	T1	T1	T1	T1	T1	T1	T1	T1	T1	T1	T1	24	
T1	T1	T1	T2	T2	T2	T2	T2	T2	T2	T2	T2	36	
T2	T2	T2	T2	T2	T2	T2	T2	T2	T2	T2	T2	48	
T2	T2	T2	T2	T2	T2	T3	T3	T3	T3	T3	T3	60	LT ⇒ NT
T3	T3	T3	T3	T3	T3	T3	T3	T3	T3	T3	T3	72	
T3	T3	T3	T3	T3	T3	T3	T3	T3	T4	T4	T4	84	
T4	T4	T4	T4	T4	T4	T4	T4	T4	T4	T4	T4	96	
T4	T4	T4	T4	T4	T4	T4	T4	T4	T4	T4	T4	108	
T4	SW1											120	

1	2	3	4	5	6	7	8	9	19	11	12		
T5	T5	T5	T5	T5	T5	T5	T5	T5	T5	T5	T5		
T5	T5	T5	T5	T5	T5	T5	T5	T5	T5	T5	T5	24	
M2	T5	T5	T5	T6	T6	T6	T6	T6	T6	T6	T6	36	
T6	T6	T6	T6	T6	T6	T6	T6	T6	T6	T6	T6	48	
T6	SW2											60	NT ⇒ LT
T6	T6	T6	T6	T6	T6	T7	T7	T7	T7	T7	T7	72	
T7	T7	T7	T7	T7	T7	T7	T7	T7	T7	T7	T7	84	
T7	T7	T7	T7	T7	T7	T7	T7	T7	T8	T8	T8	96	
T8	T8	T8	T8	T8	T8	T8	T8	T8	T8	T8	T8	108	
T8	T8	T8	T8	T8	T8	T8	T8	T8	T8	T8	T8	120	

Agenda:

T1. . . . . T8 B + B + D - Data (ternary)

M1, M2 Service Data (ternary)

SW1, SW2 Synchronizing Word

Maintenance and service channel.

The ternary symbols M1 and M2 represent non-scrambled data that can be transmitted at a rate of 1 kBaud. Those symbols are used for various purposes:

- Maintenance Channel (control test loops (LT → NT) and frame errors (LT → NT)
- Service channel (transparent user data and transmit messages from NT to LT)

Encoding.

The encoding of a binary bit stream is made such that 4 binary bits correspond to 3 symbols of ternary symbol stream. The encoding follows the rules of modified monitoring state 43 (MMS43).

COMMAND / INDICATE CHANNEL (A bits)

Command/Indicate codes are define depending on the mode selected (LT or NT).

NT mode COMMANDS (DIN)

ACT	1 0 0 0	Activate. Layer 1 is activated at the UK0 interface starting with a 'wake-up' signal INFO U1W, followed by INFO U1A during synchronization and closed by INFO U1 when synch is gained.
AW	0 0 0 0	Awake. Set the module interface from the power-down to the power-up state. No signal is emitted at UK0 interface. Even DIN pin pulled LOW can have the same effect.
DC	1 1 1 1	Deactivation confirmation. The module interface is deactivated. The transmitter is disabled but the receiver is still enabled to recognize an awake signal. THe UIC is set in power down state.
RES	1 1 0 1	Reset. Reset the UIC to the initial state.
SY	1 1 0 0	Synchronize. Drive the UIC in connect through from module interface to line interface.

Remark: Executing the command RES (1101) is functionally equivalent to pulling the RESETN pin (6) LOW, with one exception:

a) RES command set pin DISS to HIGH (+5V)
b) pulling RESETN LOW set pin DISS to LOW (0V).

NT mode INDICATION (DOUT)

ACT	1 0 0 0	Activate. The synchronous state of the receiver is reached.
DC	1 1 1 1	Deactivation confirmation. The transmitter is disabled but the receiver remains enabled to detect awake signals at UK0 UIC is set in power down state.
DEAC	0 0 0 0	Deactivate. A request to deactivate INFO U0 has been detected.
CT	1 1 0 0	Connection Through. The UIC is fully activated.
CTL2	1 1 1 0	Connection through with loop 2. A loop 2 command has been detected at UK0.
L2	1 0 1 0	Loop 2. Synchronization has been reached during a Loop 2 activation procedure.
RSYN	0 1 0 0	Resynchronization. The receiver has lost framing and is attempting to resynchronize.

LT mode COMMANDS (DIN)

ACT	1 0 0 0	Activate. UIC is set in power-up state, executing the complete activation of Layer 1. The transparent channel transmission is enabled.
AL	1 0 0 1	Analog Loop. The analog transmitter output is looped back to the receiver input which is disconnected from UK0 interface. A pseudo wake-up procedure is executed.
L2	1 0 1 0	Loop 2. Command to close Loop 2 in NT.
LTD	0 0 1 1	Line Transmission Disabled. UIC stops transmitting signals on the line and is powered down.
DEAC	0 0 0 0	Deactivate. Request to deactivate UK0.
RES	1 1 0 1	Reset. Reset the UIC to the initial state.
SSP	0 1 0 1	Send Single Pulse. The UIC transmits single pulse at 1 ms time intervals with alternate polarity.
L4	1 0 1 1	Repeter loop

LT mode INDICATION (DOUT)

ACT	1 0 0 0	Activation running. UIC is powered-up and the activation procedure is running.
RDS	0 1 1 1	Running Digital Sum. Given during activation procedure. The receiver has reached synchronization.
CT	1 1 0 0	Connection Through. Layer 1 activation procedure has been completed. B and D channels are transparently connected.
DEAC	0 0 0 1	Deactivation running. UIC is deactivating in response of a DEAC, RES or LTD command.
DC	1 1 1 1	Deactivation confirmation. UIC has completed the deactivation procedure.
RSYN	0 1 0 0	Resynchronization. The receiver has lost framing and is attempting to resynchronize.
HI	0 0 1 1	High Impedance. When pin PFOFF is HIGH indication HI is output and UIC starts transmitting INFO U0. Normally used to indicate that remote feeding has been switched off.

POWER DOWN STATE

Power consumption of most functions is reduced; module interface is not active; C/I messages cannot be exchanged.

ACTIVATION DEACTIVATION

The ACTIVATION procedure consists of three steps: AWAKE, SYNCHRONIZE and CONNECT THROUGH.

Activation times are (max):

COLDSTART 1 sec

WARMSTART 170 msec

The DEACTIVATION procedure consists of two steps: line DEACTIVATION and POWER DOWN.

Deactivation time is (typ) 4 ms.

OSCILLATOR

Oscillators of 15.36 MHz are required. When in NT a tollerances of +/-30 ppm is allowed, it is advisable to use in LT a tollerances of +/-20 ppm.

LINE RANGE

The LINE RANGE depends on the cable section. Typically:

up to 4.2Km with 0.4mm cable

- 5.5Km - 0.5mm -
- 8.0Km - 0.6mm -

Assumed noise level for such performances is 10uV/SQRT(Hz) on a 200KHz bandwidth.

LT CLOCK JITTER

The phase jitter between Master Clock (15.36MHz) and interface clock (4.096MHz) should not exceed 50ns.

ELECTRICAL CHARACTERISTICS

Supply Voltages:

DVDD = 5V +/- 5%

AVDD = 5V +/- 5%

AGND = 2.5V +/- 5% (max curr 0.25mA)

Power consumption

Active = max 280mW (line loaded at 150Ohm)

Power down = Typ. 30mW
= Max. 50mW

DIGITAL INTERFACE STATIC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IH}	High Level Input Voltage		3.5			V
V_{IL}	Low Level Input Voltage				1.0	V
V_{OH1}	High Level Output Voltage all outputs except DOUT	I_{OH1} = 0.4mA	V_{DD}-0.66			V
V_{OH2}	High Level Output Voltage DOUT, (Open Drain)	R to DV_{DD} R = 1KΩ	4			V
V_{OL1}	Low Level Output Voltage all outputs except DOUT	I_{OL1} = 0.4mA			0.33	V
V_{OL2}	Low Level Output Voltage DOUT, (Open Drain)	I_{OL1} = 0.7mA			0.4	V
C_{IN}	Inputs Capacitance, all inputs at DOUT if output is off				10 10	pF pF
C_{OUT}	Load Capacitance at all outputs except at DOUT				25	pF
C_{OUT}	Load Capacitance at DOUT				150	pF
I_{IN}	Input Leakage Current				1	µA

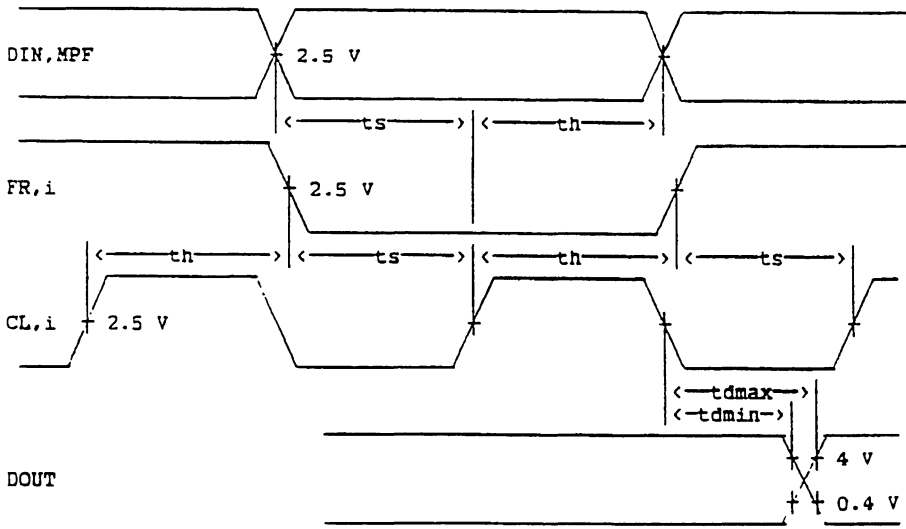
DIGITAL INTERFACE DYNAMIC CHARACTERISTICS

Burst mode.

Parameter	Port	from	to	Conditions		Min.	Max.
				C	R to DVDD		
				pF	KΩ	ns	ns
Rise Time tr	FR, CL	1.0V	3.5V	10			30
Fall Time tf	FR, CL	3.5V	1.0V	10			30
Setup Time ts	FR	FR, i –	CL, i +			30	
Setup Time ts	FR	FR, i +	CL, i +			30	
Setup Time ts	DIN	DIN +/–	CL, i +			50	
Setup Time ts	MPF	MPF +/–	CL, i +			50	
Hold Time th	FR	CL, i +	FR, i –			50	
Hold Time th	FR	CL, i +	FR, i +			50	
Hold Time th	DIN	CL, i +	DIN +/–			60	
Hold Time th	MPF	CL, i +	MPF +/–			60	
Delay Time td	DOUT	CL, i –	DOUT +/–	50	1	0	150
Delay Time td	DOUT	CL, i –	DOUT +/–	150	1	0	200
Clock Width tc	CL, i	CL +/–	CL +/–			239	249
Clock Width tc	CL, i	CL +/–	CL –/+			100	144

+ = rising edge

– = falling edge



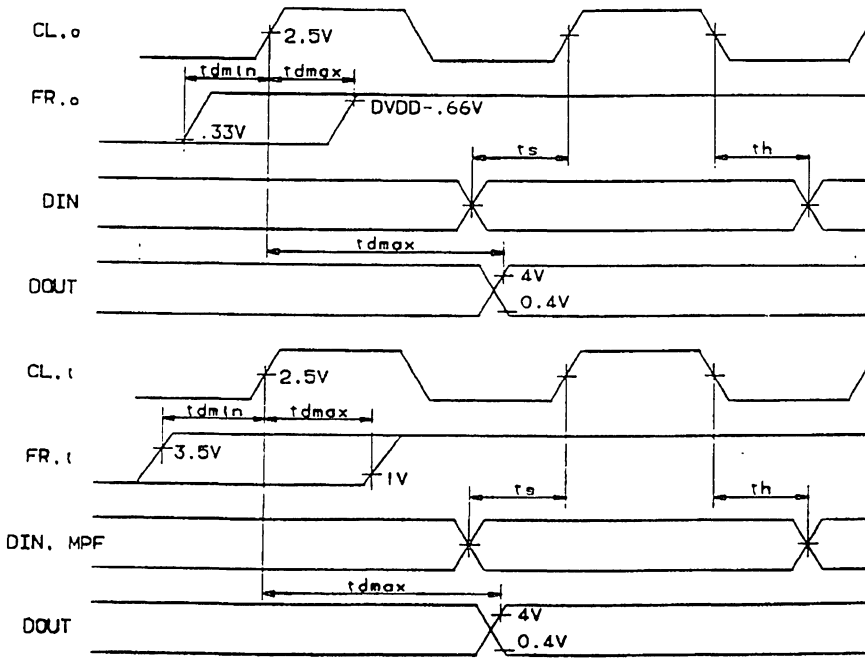
DIGITAL INTERFACE DYNAMIC CHARACTERISTICS (continued)

Continuous mode.

Parameter	Port	from	to	Conditions		Min.	Max.
				C	R to DVDD		
				pF	KΩ	ns	ns
Rise Time tr	FR, CL, i	1.0V	3.5V	10			30
Fall Time tf	FR, CL, i	3.5V	1.0V	10			30
Rise Time tr	FR, CL, o	10%	90%	25			30
Fall Time tf	FR, CL, o	90%	10%	25			30
Setup Time ts	DIN	DIN +/–	CL, i +			50	
Setup Time ts	MPF	MPF +/–	CL, i +			50	
Delay Time td	FR	CL, i +	FR, i +			-200	200
Hold Time th	DIN	CL, i –	DIN +/–			100	
Hold Time th	MPF	CL, i –	DIN +/–			100	
Delay Time td	DOUT	CL, i +	DOUT +/–	25	10		500
Setup Time ts	DIN	DIN +/–1	CL, o +			50	
Setup Time th	DIN	CL, o –	DIN +/–			100	
Delay Time td	DOUT	CL. o +	DOUT +/–	25	10		500
Delay Time td	FR	CL, o +	FR,o +	25		-150	150
Clock Width tc	CL, i	CL +/–	CL +/–			1830	2080
Clock Width tp	CL, i	CL +/–	CL +/–	25		1830	2080
Pulse Width tp	CL, i	CL +/–	CL –/+			850	1100
Pulse Width tp	CL, i	CL +/–	CL –/+	25		850	1100

+ = rising edge

– = falling edge



DIGITAL INTERFACE DYNAMIC CHARACTERISTICS (continued)

Master clock.

Parameter	Port	from	to	Conditions		Min.	Max.
				C			
				pF		ns	ns
Rise Time tr	XTAL2	1.0V	3.5V	10			15
Fall Time tf	XTAL2	3.5V	1.0V	10			15
Rise Time tr	CLS	10%	90%	25			15
Fall Time tf	CLS	90%	10%	25			15
Pulse Width	CLS	CLS +/–	CLS –/+	25		20	

+ = rising edge

– = falling edge

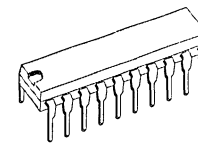
Setup Time ts	DIN, FR, i +/–	2.5V	CL, i +	2.5V
Hold Time th	CL, i +	2.5V	DIN, FR, i +/–	2.5V
Delay min. td	CL, i + CL, i –	2.5V	DOUT +/–	0.4 / 4V
Delay max. td	CL, i + CL, i –	2.5V	DOUT +/–	4 / 0.4V
Delay min. td (negative)	CL, i +	2.5V	FR, i +	3.5V
Delay max. td	CL, i +	2.5V	FR, i +	1V
Setup Time ts	DIN, +/–	2.5V	CL, o +	2.5V
Hold Time ts	CL, o +	2.5V	DIN +/–	2.5V
Delay max. td	CL, o +	2.5V	DOUT +/–	4 / 0.4V
Delay min. td (negative)	CL, o +	2.5V	FR, o +	0.33V
Delay max. td	CL, o +	2.5V	FR, o +	VDD - 0.66V
Pulse Width tp	CL, o +/–	2.5V	CL, o –/+	2.5V
Clock Width tc	CL, o +/–	2.5V	CL, o +/–	2.5V
Pulse Width tp	CLS, MXCL +/–	2.5V	CL, o –/+	2.5V
Clock Width tc	CLS, MXCL +/–	2.5V	CL, o +/–	2.5V

SGS-THOMSON MICROELECTRONICS

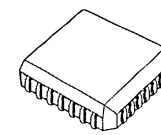
TS5070
TS5071

PROGRAMMABLE CODEC/FILTER COMBO 2ND GENERATION

- COMPLETE CODEC AND FILTER SYSTEM INCLUDING :
  - TRANSMIT AND RECEIVE PCM CHANNEL FILTERS
  - μ-LAW OR A-LAW COMPANDING CODER AND DECODER
  - RECEIVE POWER AMPLIFIER DRIVES 300 Ω
  - 4.096 MHz SERIAL PCM DATA (max)
- PROGRAMMABLE FUNCTIONS :
  - TRANSMIT GAIN : 25.4 dB RANGE, 0.1 dB STEPS
  - RECEIVE GAIN : 25.4 dB RANGE, 0.1 dB STEPS
  - HYBRID BALANCE CANCELLATION FILTER
  - TIME-SLOT ASSIGNMENT: UP TO 64 SLOTS/FRAME
  - 2 PORT ASSIGNMENT (TS5070)
  - 6 INTERFACE LATCHES (TS5070)
  - A OR μ-LAW
  - ANALOG LOOPBACK
  - DIGITAL LOOPBACK
- DIRECT INTERFACE TO SOLID-STATE SLICs
- SIMPLIFIES TRANSFORMER SLIC, SINGLE WINDING SECONDARY
- STANDARD SERIAL CONTROL INTERFACE
- 80 mW OPERATING POWER (typ)
- 1.5mW STANDBY POWER (typ)
- MEETS OR EXCEEDS ALL CCITT AND LSSGR SPECIFICATIONS
- TTL AND CMOS COMPATIBLE DIGITAL INTERFACES



DIP20 (Plastic)
ORDERING NUMBER:TS5071N



PLCC28
ORDERING NUMBER: TS5070FN

DESCRIPTION

The TS5070 series are the second generation combined PCM CODEC and Filter devices optimized for digital switching applications on subscriber and trunk line cards.

Using advanced switched capacitor techniques the TS5070 and TS5071 combine transmit bandpass and receive lowpass channel filters with a companding PCM encoder and decoder. The devices are A-law and μ-law selectable and employ a conventional serial PCM interface capable of being clocked up to 4.096 MHz. A number of programmable functions may be controlled via a serial control port.

Channel gains are programmable over a 25.4 dB range in each direction, and a programmable filter is included to enable Hybrid Balancing to be adjusted to suit a wide range of loop impedance conditions.

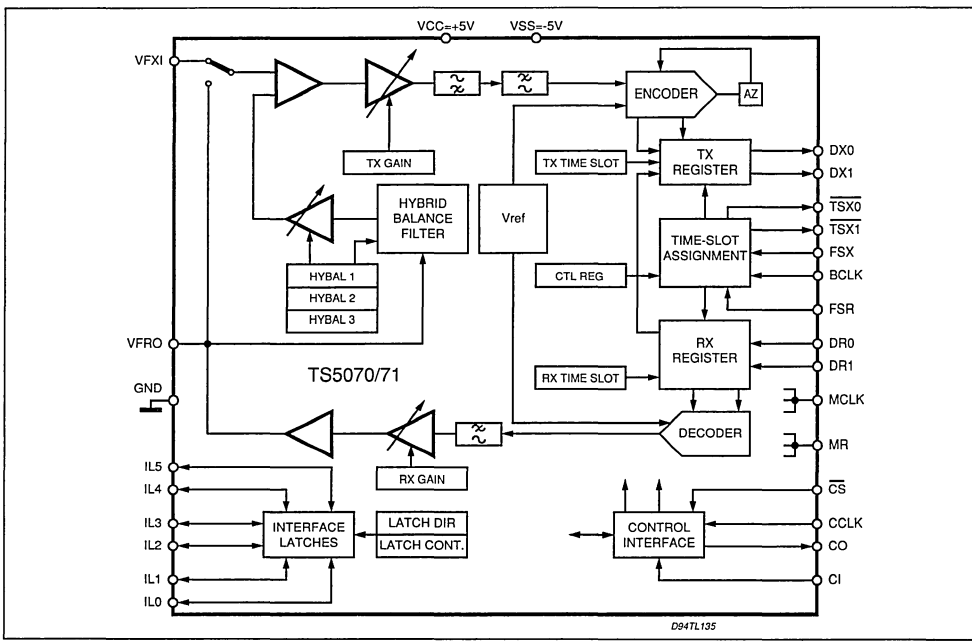
Both transformer and active SLIC interface circuits with real or complex termination impedances can be balanced by this filter, with cancellation in excess of 30 dB being readily achievable when measured across the passband against standard test termination networks.

To enable COMBO IIG to interface to the SLIC control leads, a number of programmable latches are included ; each may be configured as either an input or an output. The TS5070 provides 6 latches and the TS5071 5 latches.

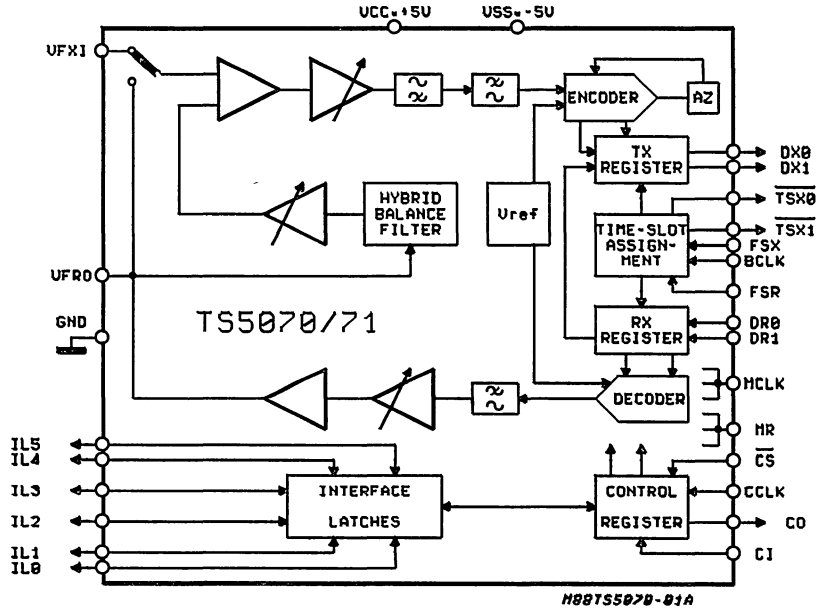
TS5070 PIN FUNCTIONALITY (PLCC28)

No.	Name	Function
1	GND	Ground Input (+0V)
2	VF_R0	Analog Output
3	V_{SS}	Supply Input (-5V)
4	NC	Not Connected
5	NC	Not Connected
6	IL3	Digital Input or Output defined by LDR register content
7	IL2	Digital Input or Output defined by LDR register content
8	FS_R	Digital input
9	D_R1	Digital input sampled by BCLK falling edge
10	D_R0	Digital input sampled by BCLK falling edge
11	CO	Digital output (shifted out on CCLK rising edge)
12	CI	Digital input (sampled on CCLK falling edge)
13	CCLK	Digital input (clock)
14	$\overline{CS}$	Digital input (chip select for CI/CO)
15	MR	Digital Input
16	BCLK	Digital input (clock)
17	MCLK	Digital input
18	D_X0	Digital output clocked by BCLK rising edge
19	D_X1	Digital output clocked by BCLK rising edge
20	$\overline{TS_X0}$	Open drain output (pulled low by active DX0 time slot)
21	$\overline{TS_X1}$	Open drain output (pulled low by active DX1 time slot)
22	FS_X	Digital input
23	IL5	Digital input or output defined by LDR register content
24	IL4	Digital input or output defined by LDR register content
25	IL1	Digital input or output defined by LDR register content
26	IL0	Digital input or output defined by LDR register content
27	V_{CC}	Supply input (+5V)
28	VF_XI	Analog input

TS5070 FUNCTIONAL DIAGRAM



BLOCK DIAGRAM

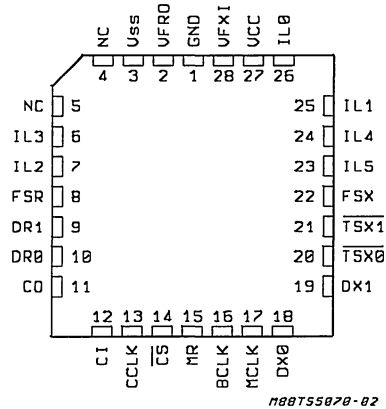


ABSOLUTE MAXIMUM RATINGS

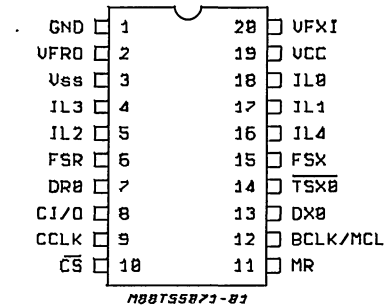
Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GND	7	V
V_{SS}	V_{SS} to GND	– 7	V
	Voltage at VFXI	V_{CC} + 0.5 to V_{SS} – 0.5	V
V_{IN}	Voltage at Any Digital Input	V_{CC} + 0.5 to GND – 0.5	V
	Current at VFRO	± 100	mA
I_O	Current at Any Digital Output	± 50	mA
T_{stg}	Storage Temperature Range	– 65, + 150	°C
T_{lead}	Lead Temperature Range (soldering, 10 seconds)	300	°C

PIN CONNECTIONS

PLCC28
TS5070FN



DIP20
TS5071N



POWER SUPPLY, CLOCK

Name	Pin Type	TS5070 FN	TS5071 N	Function	Description
V_{CC}	S	27	19	Positive Power Supply	+ 5 V ± 5 %
V_{SS}	S	3	3	Negative Power Supply	– 5 V ± 5 %
GND	S	1	1	Ground	All analog and digital signals are referenced to this pin.
BCLK	I	16	12	Bit Clock	Bit clock input used to shift PCM data into and out of the D_R and D_X pins. BCLK may vary from 64 kHz to 4.096 MHz in 8 kHz increments, and must be synchronous with MCLK (TS5071 only).
MCLK	I	17	12	Master Clock	Master clock input used by the switched capacitor filters and the encoder and decoder sequencing logic. Must be 512 kHz, 1. 536/1. 544 MHz, 2.048 MHz or 4.096 MHz and synchronous with BCLK. BCLK and MCLK are wired together in the TS5071.

TRANSMIT SECTION

Name	Pin Type	TS5070 FN	TS5071 N	Function	Description
FS_X	I	22	15	Transmit Frame Sync.	Normally a pulse or squarewave waveform with an 8 kHz repetition rate is applied to this input to define the start of the transmit time-slot assigned to this device (non-delayed data mode) or the start of the transmit frame (delayed data mode using the internal time-slot assignment counter).
VF_XI	I	28	20	Transmit Analog	This is a high–impedance input. Voice frequency signals present on this input are encoded as an A–law or μ–law PCM bit stream and shifted out on the selected D_X pin.
D_X0 D_X1	0 0	18 19	13 –	Transmit Data	D_X1 is available on the TS5070 only, D_X0 is available on all devices. These transmit data TRI–STATE® outputs remain in the high impedance state except during the assigned transmit time–slot on the assigned port, during which the transmit PCM data byte is shifted out on the rising edges of BCLK.
$\overline{TS_X0}$ $\overline{TS_X1}$	0 0	20 21	14 –	Transmit Time–slot	$\overline{TS_X1}$ is available on the TS5070 only. $\overline{TS_X0}$ is available on all devices. Normally these opendrain outputs are floating in a high impedance state except when a time–slot is active on one of the D_X outputs, when the apppropriate $\overline{TS_X}$ output pulls low to enable a backplane line–driver. Should be strapped to ground (GND) when not used.

RECEIVE SECTION

Name	Pin Type	TS5070 FN	TS5071 N	Function	Description
FS_R	I	8	6	Receive Frame Sync.	Normally a pulse or squarewave waveform with an 8 kHz repetition rate is applied to this input to define the start of the receive time–slot assigned to this device (non-delayed frame mode) or the start of the receive frame (delayed frame mode using the internal time-slot assignment counter.
VF_R0	0	2	2	Receive Analog	The receive analog power amplifier output, capable of driving load impedances as low as 300 Ω (depending on the peak overload level required). PCM data received on the assigned D_R pin is decoded and appears at this output as voice frequency signals.
D_R0 D_R1	I I	10 9	7 –	Receive Data	D_R1 is available on the TS5070 only, D_R0 is available on all devices. These receive data input(s) are inactive except during the assigned receive time–slot of the assigned port when the receive PCM data is shifted in on the falling edges of BCLK.

INTERFACE, CONTROL, RESET

Name	Pin Type	TS5070 FN	TS5071 N	Function	Description
IL5 IL4 IL3 IL2 IL1 IL0	I/O I/O I/O I/O I/O I/O	23 24 6 7 25 26	– 16 4 5 17 18	Interface Latches	IL5 through IL0 are available on the TS5070, IL4 through IL0 are available on the TS5071. Each interface Latch I/O pin may be individually programmed as an input or an output determined by the state of the corresponding bit in the Latch Direction Register (LDR) . For pins configured as inputs, the logic state sensed on each input is latched into the interface Latch Register (ILR) whenever control data is written to COMBO IIG, while CS is low, and the information is shifted out on the CO (or CI/O) pin. When configured as outputs, control data written into the ILR appears at the corresponding IL pins.
CCLK	I	13	9	Control Clock	This clock shifts serial control information into or out of CI or CO (or CI/O) when the $\overline{CS}$ input is low depending on the current instruction. CCLK may be asynchronous with the other system clocks.
CI/O	I/O	–	8	Control Data Input/output	This is Control Data I/O pin wich is provided on the TS5071. Serial control information is shifted into or out of COMBO IIG on this pin when $\overline{CS}$ is low. The direction of the data is determined by the current instruction as defined in Table 1.
CI CO	I O	12 11	– –	Control Data Input Control Data Output	These are separate controls, availables only on the TS5070. They can be wired together if required.
$\overline{CS}$	I	14	10	Chip Select	When this pins is low, control information can be written to or read from the COMBO IIG via the CI and CO pins (or CI/O).
MR	I	15	11	Master Reset	This logic input must be pulled low for normal operation of COMBO IIG. When pulled momentarily high, all programmable registers in the device are reset to the states specified under "Power–on Initialization".

FUNCTIONAL DESCRIPTION

POWER-ON INITIALIZATION

When power is first applied, power-on reset circuitry initializes COMBO IIG and puts it into the power-down state. The gain control registers for the transmit and receive gain sections are programmed for no output, the hybrid balance circuit is turned off, the power amp is disabled and the device is in the non-delayed timing mode. The Latch Direction Register (LDR) is pre-set with all IL pins programmed as inputs, placing the SLIC interface pins in a high impedance state. The CI/O pin is set as an input ready for the first control byte of the initialization sequence. Other initial states in the Control Register are indicated in Table 2.

A reset to these same initial conditions may also be forced by driving the MR pin momentarily high. This may be done either when powered-up or down. For normal operation this pin must be pulled low. If not used, MR should be hard-wired to ground.

The desired modes for all programmable functions may be initialized via the control port prior to a Power-up command.

POWER-DOWN STATE

Following a period of activity in the powered-up state the power-down state may be re-entered by writing any of the control instructions into the serial control port with the "P" bit set to "1" It is recommended that the chip be powered down before writing any additional instructions. In the power-down state, all non-essential circuitry is de-activated and the D_X0 and D_X1 outputs are in the high impedance TRI-STATE condition.

The coefficients stored in the Hybrid Balance circuit and the Gain Control registers, the data in the LDR and ILR, and all control bits remain unchanged in the power-down state unless changed by writing new data via the serial control port, which remains operational. The outputs of the Interface Latches also remain active, maintaining the ability to monitor and control a SLIC.

TRANSMIT FILTER AND ENCODER

The Transmit section input, VF_XI, is a high impedance summing input which is used as the differencing point for the internal hybrid balance cancellation signal. No external components are needed to set the gain. Following this circuit is a programmable gain/attenuation amplifier which is controlled by the contents of the Transmit Gain Register (see Programmable Functions section). An active prefilter then precedes the 3rd order high-pass and 5th order low-pass switched capacitor filters. The A/D converter has a compressing characteristic according to the standard CCITT A or µ255 coding laws, which must be selected by a control instruction during initialization (see table 1 and 2). A precision on-chip voltage reference ensures accurate and highly stable transmission levels. Any offset voltage arising in the gain-set amplifier, the filters or the comparator is cancelled by an internal auto-zero circuit.

Each encode cycle begins immediately following the assigned Transmit time-slot. The total signal delay referenced to the start of the time-slot is approximately 165 µs (due to the Transmit Filter) plus 125 µs (due to encoding delay), which totals 290 µs. Data is shifted out on D_X0 or D_X1 during the selected time slot on eight rising edges of BCLK.

DECODER AND RECEIVE FILTER

PCM data is shifted into the Decoder's Receive PCM Register via the D_R0 or D_R1 pin during the selected time-slot on the 8 falling edges of BCLK. The Decoder consists of an expanding DAC with either A or µ255 law decoding characteristic, which is selected by the same control instruction used to select the Encode law during initialization. Following the Decoder is a 5th order low-pass switched capacitor filter with integral Sin x/x correction for the 8 kHz sample and hold. A programmable gain amplifier, which must be set by writing to the Receive Gain Register, is included, and finally a Post-Filter/Power Amplifier capable of driving a 300 Ω load to ± 3.5 V, a 600 Ω load to ± 3.8 V or 15 kΩ load to ± 4.0 V at peak overload.

A decode cycle begins immediately after each receive time-slot, and 10 µs later the Decoder DAC output is updated. The total signal delay is 10 µs plus 120 µs (filter delay) plus 62.5 µs (1/2 frame) which gives approximately 190 µs.

PCM INTERFACE

The FS_X and FS_R frame sync inputs determine the beginning of the 8-bit transmit and receive time-slots respectively. They may have any duration from a single cycle of BCLK to one MCLK period LOW. Two different relationships may be established between the frame sync inputs and the actual time-slots on the PCM busses by setting bit 3 in the Control Register (see table 2). Non delayed data mode is similar to long-frame timing on the ETC5050/60 series of devices : time-slots being nominally coincident with the rising edge of the appropriate FS input. The alternative is to use Delayed Data mode which is similar to short-frame sync timing, in which each FS input must be high at least a half-cycle of BCLK earlier than the time-slot.

The Time-Slot Assignment circuit on the device can only be used with Delayed Data timing. When using Time-Slot Assignment, the beginning of the first time-slot in a frame is identified by the appropriate FS input. The actual transmit and receive time-slots are then determined by the internal Time-Slot Assignment counters. Transmit and Receive frames and time-slots may be skewed from each other by any number of BCLK cycles.

During each assigned transmit time-slot, the selected $D_X0/1$ output shifts data out from the PCM register on the rising edges of BCLK. TS_X0 (or TS_X1 as appropriate) also pulls low for the first 7 1/2 bit times of the time-slot to control the TRI-STATE Enable of a backplane line driver. Serial PCM data is shifted into the selected $D_R0/1$ input during each assigned Receive time slot on the falling edges of BCLK. D_X0 or D_X1 and D_R0 or D_R1 are selectable on the TS5070 only.

SERIAL CONTROL PORT

Control information and data are written into or readback from COMBO IIG via the serial control port consisting of the control clock CCLK ; the serial data input/output CI/O (or separate input CI, and output CO on the TS5070 only) ; and the Chip Select input $\overline{CS}$. All control instructions require 2 bytes, as listed in table 1, with the exception of a single byte power-up/down command. The byte 1 bits are used as follows: bit 7 specifies power-up or power-down; bits 6, 5, 4 and 3 specify the register address; bit 2 specifies whether the instructions is read or write; bit 1 specifies a one or two byte in-

struction; and bit 0 is not used. To shift control data into COMBO IIG, CCLK must be pulsed high 8 times while $\overline{CS}$ is low. Data on the CI or CI/O input is shifted into the serial input register on the falling edge of each CCLK pulse. After all data is shifted in, the contents of the input shift register are decoded, and may indicate that a 2nd byte of control data will follow. This second byte may either be defined by a second byte-wide $\overline{CS}$ pulse or may follow the first continuously, i.e. it is not mandatory for $\overline{CS}$ to return high in between the first and second control bytes. On the falling edge of the 8th CCLK clock pulse in the 2nd control byte the data is loaded into the appropriate programmable register. $\overline{CS}$ may remain low continuously when programming successive registers, if desired. However $\overline{CS}$ should be set high when no data transfers are in progress.

To readback interface Latch data or status information from COMBO IIG, the first byte of the appropriate instruction is strobed in during the first $\overline{CS}$ pulse, as defined in table 1. $\overline{CS}$ must then be taken low for a further 8 CCLK cycles, during which the data is shifted onto the $\overline{CO}$ or CI/O pin on the rising edges of CCLK. When $\overline{CS}$ is high the CO or CI/O pin is in the high-impedance TRI-STATE, enabling the CI/O pins of many devices to be multiplexed together. Thus, to summarize, 2-byte READ and WRITE instructions may use either two 8-bit wide $\overline{CS}$ pulses or a single 16-bit wide $\overline{CS}$ pulse.

Table 1: Programmable Register Instructions

Function	Byte 1								Byte 2
	7	6	5	4	3	2	1	0	
Single Byte Power–up/down	P	X	X	X	X	X	0	X	None
Write Control Register	P	0	0	0	0	0	1	X	See Table 2
Read–back Control Register	P	0	0	0	0	1	1	X	See Table 2
Write Latch Direction Register (LDR)	P	0	0	1	0	0	1	X	See Table 4
Read Latch Direction Register	P	0	0	1	0	1	1	X	See Table 4
Write Latch Content Register (ILR)	P	0	0	0	1	0	1	X	See Table 5
Read Latch Content Register	P	0	0	0	1	1	1	X	See Table 5
Write Transmit Time–slot/port	P	1	0	1	0	0	1	X	See Table 6
Read–back Transmit Time–slot/port	P	1	0	1	0	1	1	X	See Table 6
Write Receive Time–slot/port	P	1	0	0	1	0	1	X	See Table 6
Read–back Receive Time–slot/port	P	1	0	0	1	1	1	X	See Table 6
Write Transmit Gain Register	P	0	1	0	1	0	1	X	See Table 7
Read Transmit Gain Register	P	0	1	0	1	1	1	X	See Table 7
Write Receive Gain Register	P	0	1	0	0	0	1	X	See Table 8
Read Receive Gain Register	P	0	1	0	0	1	1	X	See Table 8
Write Hybrid Balance Register ≠ 1	P	0	1	1	0	0	1	X	See Table 9
Read Hybrid Balance Register ≠ 1	P	0	1	1	0	1	1	X	See Table 9
Write Hybrid Balance Register ≠ 2	P	0	1	1	1	0	1	X	See Table 10
Read Hybrid Balance Register ≠ 2	P	0	1	1	1	1	1	X	See Table 10
Write Hybrid Balance Register ≠ 3	P	1	0	0	0	0	1	X	
Read Hybrid Balance Register ≠ 3	P	1	0	0	0	1	1	X	

Notes: 1. Bit 7 of bytes 1 and 2 is always the first bit clocked into or out of the CI, CO or CI/CO pin.
2. "P" is the power-up/down control bit, see "Power-up" section ("0" = Power Up "1" = Power Down).

PROGRAMMABLE FUNCTIONS

POWER-UP/DOWN CONTROL

Following power-on initialization, power-up and power-down control may be accomplished by writing any of the control instructions listed in table 1 into COMBO IIG with the "P" bit set to "0" for power-up or "1" for power-down. Normally it is recommended that all programmable functions be initially programmed while the device is powered down. Power state control can then be included with the last programming instruction or the separate single-byte instruction. Any of the programmable registers may also be modified while the device is powered-up or down be setting the "P" bit as indicated. When the power up or down control is entered as a single byte instruction, bit one (1) must be set to a 0.

When a power-up command is given, all de-activated circuits are activated, but the TRI-STATE PCM output(s), D_X0 (and D_X1), will remain in the high impedance state until the second FS_X pulse after power-up.

CONTROL REGISTER INSTRUCTION

The first byte of a READ or WRITE instruction to the Control Register is as shown in table 1. The second byte functions are detailed in table 2.

MASTER CLOCK FREQUENCY SELECTION

A Master clock must be provided to COMBO IIG for operation of the filter and coding/decoding functions. The MCLK frequency must be either 512 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz, or 4.096 MHz and must be synchronous with BCLK. Bits F1 and F0 (see table 2) must be set during initialization to select the correct internal divider.

CODING LAW SELECTION

Bits "MA" and "IA" in table 2 permit the selection of μ255 coding or A-law coding with or without even-bit inversion.

ANALOG LOOPBACK

Analog Loopback mode is entered by setting the "AL" and "DL" bits in the Control Register as shown in table 2. In the analog loopback mode, the Transmit input VF_XI is isolated from the input pin and internally connected to the VF_RO output, forming a loop from the Receive PCM Register back to the Transmit PCM Register. The VF_RO pin remains active, and the programmed settings of the Transmit and Receive gains remain unchanged, thus care must be taken to ensure that overload levels are not exceeded anywhere in the loop.

Hybrid balancing must be disabled for meaning ful analog loopback Function.

DIGITAL LOOPBACK

Digital Loopback mode is entered by setting the "DL" bit in the Control Register as shown in table 2.

Table 2: Control Register Byte 2 Functions

Bit Number								Function
7	6	5	4	3	2	1	0	
F1	F0	MA	IA	DN	DL	AL	PP	
0 0 1 1	0 1 0 1							MCLK = 512 kHz MCLK = 1. 536 or 1. 544 MHz MCLK = 2. 048 MHz MCLK = 4. 096 MHz
		0 1 1	X 0 1					Select μ. 255 Law (*) A–law, Including Even Bit Inversion A–Law, No Even Bit Inversion
				0 1				Delayed Data Timing Non–delayed Data Timing (*)
					0 1 0	0 X 1		Normal Operation (*) Digital Loopback Analog Loopback
							0 1	Power Amp Enabled in PDN (*) Power Amp Disabled in PDN

(*) State at power-on initialization (bit 4 = 0)

Table 3: Coding Law Conventions.

	m255 Law MSB LSB								True A-law with even bit inversion MSB LSB								A-law without even bit inversion MSB LSB							
V_{IN} = +Full Scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1	1
V_{IN} = 0V	1 0	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 0	1 1	0 0	1 1	0 0	1 1	0 0	1 1	1 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0
V_{IN} = -Full Scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	1	1	1	1	1	1

Note: The MSB is always the first PCM bit shifted in or out of COMBO IIG.

This mode provides another stage of path verification by enabling data written into the Receive PCM Register to be read back from that register in any Transmit time-slot at D_X0 or D_X1.

For Analog Loopback as well as for Digital Loopback PCM decoding continues and analog output appears at VF_RO. The output can be disabled by pro gramming "No Output" in the Receive Gain Register (see table 8).

INTERFACE LATCH DIRECTIONS

Immediately following power-on, all Interface Latches assume they are inputs, and therefore all IL pins are in a high impedance state. Each IL pin may be individually programmed as a logic input or output by writing the appropriate instruction to the LDR, see table 1 and 4. Bits L_5-L_0 must be set by writing the specific instruction to the LDR with the L bits in the second byte set as specified in table 4. Unused interface latches should be programmed as outputs. For the TS5071, L5 should always be programmed as an output.

Table 4: Byte 2 Function of Latch Direction Register

Bit Number							
7	6	5	4	3	2	1	0
L0	L1	L2	L3	L4	L5	X	X

L_N Bit	IL Direction
0	Input *
1	Output

(*) State at power-on initilization.
Note: L5 should be programmed as an output for the TS5071.

INTERFACE LATCH STATES

Interface Latches configured as outputs assume the state determined by the appropriate data bit in the 2-byte instruction written to the Latch Content Register (ILR) as shown in tables 1 and 5. Latches configured as inputs will sense the state applied by an external source, such as the Off-Hook detect output of a SLIC. All bits of the ILR, i.e. sensed inputs and the programmed state of outputs, can be read back in the 2nd byte of a READ from the ILR. It is recommended that, during initialization, the state of IL pins to be configured as outputs should first be programmed, followed immediately by the Latch Direction Register.

Table 5: Interface Latch Data Bit Order

Bit Number							
7	6	5	4	3	2	1	0
D0	D1	D2	D3	D4	D5	X	X

TIME-SLOT ASSIGNMENT

COMBO IIG can operate in either fixed time-slot or time-slot assignment mode for selecting the Transmit and Receive PCM time-slots. Following power-on, the device is automatically in Non-Delayed Timing mode, in which the time-slot always begins with the leading (rising) edge of frame sync inputs FS_X and FS_R. Time-Slot Assignment may only be used with Delayed Data timing : see figure 6. FS_X and FS_R may have any phase relationship with each other in BCLK period increments.

Table 6: Byte 2 of Time-slot and Port Assignment Instructions

Bit Number								Function
7 EN	6 PS (note 1)	5 T5 (note 2)	4 T4	3 T3	2 T2	1 T1	0 T0	
0	X	X	X	X	X	X	X	Disable D_X Outputs (transmit instruction) * Disable D_R Inputs (receive instruction) *
1	0	Assign One Binary Coded Time-slot from 0–63 Assign One Binary Coded Time-slot from 0–63						Enable D_X0 Output, Disable D_X1 Output (Transmit instruction) Enable D_R0 Input, Disable D_R1 Input (Receive Instruction)
1	1	Assign One Binary Coded Time-slot from 0–63 Assign One Binary Coded Time-slot from 0–63						Enable D_X1 Output, Disable D_X0 Output (Transmit instruction) Enable D_R1 Input, Disable D_R0 Input (Receive Instruction)

Notes:
1. The "PS" bit MUST always be set to 0 for the TS5071.
2. T5 is the MSB of the time-slot assignment.
(*) State at power-on initialization

Alternatively, the internal time-slot assignment counters and comparators can be used to access any time-slot in a frame, using the frame sync inputs as marker pulses for the beginning of transmit and receive time-slot 0. In this mode, a frame may consist of up to 64 time-slots of 8 bits each. A time-slot is assigned by a 2-byte instruction as shown in table 1 and 6. The last 6 bits of the second byte indicate the selected time-slot from 0-63 using straight binary notation. A new assignment becomes active on the second frame following the end of the Chip Select for the second control byte. The "EN" bit allows the PCM inputs $D_R0/1$ or outputs $D_X0/1$ as appropriate, to be enabled or disabled.

Time-Slot Assignment mode requires that the FS_X and FS_R pulses must conform to the delayed timing format shown in figure 6.

PORT SELECTION

On the TS5070 only, an additional capability is available : 2 Transmit serial PCM ports, D_X0 and D_X1, and 2 receive serial PCM ports, D_R0 and D_R1, are provided to enable two-way space switching to be implemented. Port selections for transmit and receive are made within the appropriate time-slot assignment instruction using the "PS" bit in the second byte.

On the TS5071, only ports D_X0 and D_R0 are available, therefore the "PS" bit MUST always be set to 0 for these devices.

Table 6 shows the format for the second byte of both transmit and receive time-slot and port assignment instructions.

TRANSMIT GAIN INSTRUCTION BYTE 2

The transmit gain can be programmed in 0.1 dB steps by writing to the Transmit Gain Register as defined in tables 1 and 7. This corresponds to a range of 0 dBm0 levels at VF_XI between 1.619 Vrms and 0.087 Vrms (equivalent to + 6.4 dBm to – 19.0 dBm in 600 Ω).
To calculate the binary code for byte 2 of this instruction for any desired input 0 dBm0 level in Vrms, take the nearest integer to the decimal number given by :

$$200 \times \log_{10}(V/\sqrt{6}) + 191$$

and convert to the binary equivalent. Some examples are given in table 7.

Table 7: Byte 2 of Transmit Gain Instructions.

Bit Number								0dBm0 Test Leve at VF_XI	
7	6	5	4	3	2	1	0	In dBm (Into 600Ω)	In Vrms (approx.)
0	0	0	0	0	0	0	0	No Output	
0	0	0	0	0	0	0	1	– 19	0.087
0	0	0	0	0	0	1	0	– 18.9	0.088
1	0	1	1	1	1	1	1	0	0.775
1	1	1	1	1	1	1	0	+6.3	1.60
1	1	1	1	1	1	1	1	+6.4	1.62

(*) State at power initialization

RECEIVE GAIN INSTRUCTION BYTE 2

The receive gain can be programmed in 0.1 dB steps by writing to the Receive Gain Register as defined in table 1 and 8. Note the following restriction on output drive capability :

a) 0 dBm0 levels ≤ 8.1dBm at VF_RO may be driven into a load of ≥ 15 kΩ to GND,

b) 0 dBm0 levels ≤ 7.6dBm at VF_RO may be driven into a load of ≥ 600 Ω to GND,

c) 0 dBm levels ≤ 6.9dBm at VF_RO may be driven into a load of ≥ 300 Ω to GND.

To calculate the binary code for byte 2 of this instruction for any desired output 0 dBm0 level in Vrms, take the nearest integer to the decimal number given by :

$$200 \times \log_{10}(V/\sqrt{6}) + 174$$

and convert to the binary equivalent. Some examples are given in table 8.

Table 8: Byte 2 of Receive Gain Instructions.

Bit Number								0dBm0 Test Leve at VF_R0	
7	6	5	4	3	2	1	0	In dBm (Into 600Ω)	In Vrms (approx.)
0	0	0	0	0	0	0	0	No Output	
0 0	0 0	0 0	0 0	0 0	0 0	0 1	1 0	– 17.3 – 17.2	0.106 0.107
1	0	1	0	1	1	1	0	0	0.775
1	1	1	1	0	0	1	1	+ 6.9 (note 1)	1.71
1	1	1	1	1	0	1	0	+ 7.6 (note 2)	1.86
1	1	1	1	1	1	1	1	+ 8.1 (note 3)	1.07

Notes:
1. Maximum level into 300Ω ; 2. Maximum level into 600Ω; 3. $R_L \geq 15K\Omega$ (*) State at power on initialization

HYBRID BALANCE FILTER

The Hybrid Balance Filter on COMBO IIG is a programmable filter consisting of a second-order Bi-Quad section, Hybal1, followed by a first-order section, Hybal2, and a programmable attenuator. Either of the filter sections can be bypassed if only one is required to achieve good cancellation. A selectable 180 degree inverting stage is included to compensate for interface circuits which also invert the transmit input relative to the receive output signal. The Bi-Quad is intended mainly to balance low frequency signals across a transformer SLIC, and the first order section to balance midrange to higher audio frequency signals. The attenuator can be programmed to compensate for VF_RO to VF_XI echos in the range of -2.5 to – 8.5 dB.

As a Bi-Quad, Hybal1 has a pair of low frequency zeroes and a pair of complex conjugate poles. When configuring the Bi-Quad, matching the phase of the hybrid at low to midband frequencies is most critical. Once the echo path is correctly balanced in phase, the magnitude of the cancellation signal can be corrected by the programmable attenuator.

The Bi-Quad mode of Hybal1 is most suitable for balancing interfaces with transformers having high inductance of 1.5 Henries or more. An alternative configuration for smaller transformers is available by converting Hybal1 to a simple first-order section with a single real low frequency pole and 0 Hz zero. In this mode, the pole/zero frequency may be programmed.

Many line interfaces can be adequately balanced by use of the Hybal1 section only, in which case the Hybal2 filter should be de-selected to bypass it.

Hybal2, the higher frequency first-order section, is provided for balancing an electronic SLIC, and is also helpful with a transformer SLIC in providing additional phase correction for mid and high-band frequencies, typically 1 kHz to 3.4 kHz. Such a correction is particularly useful if the test balance impedance includes a capacitor of 100 nF or less, such as the loaded and non-loaded loop test networks in the United States. Independent placement of the pole and zero location is provided.

Table 9: Hybrid Balance Register 1 Byte 2 Instruction.

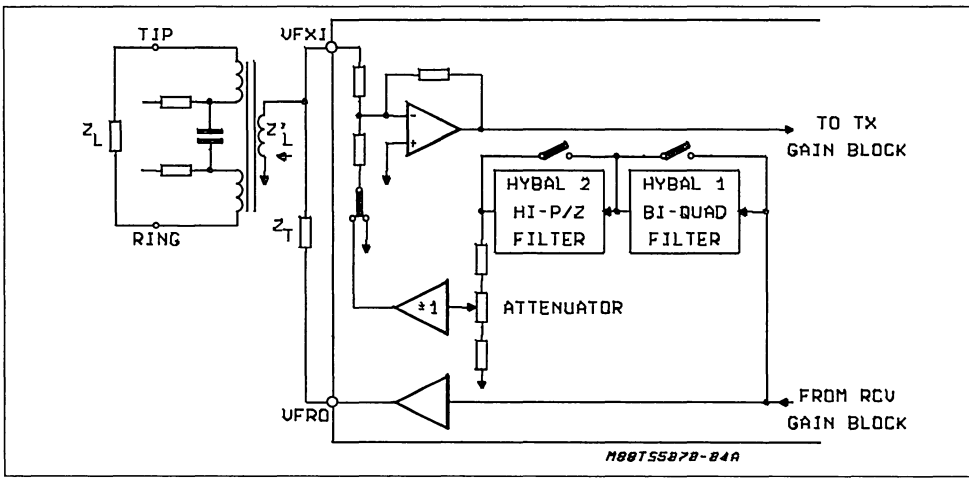
Bit	State	Function
7	0	Disable Hybrid Balance Circuit Completely. No internal cancellation is provided.
	1	Enable Hybrid Balance Cancellation Path
6	0	Phase of the internal cancellation signal assumes inverted phase of the echo path from VF_RO to VF_XI.
	1	Phase of the internal cancellation signal assumes no phase inversion in the line interface.
5	0	Bypass Hybal 2 Filter Section
	1	Enable Hybal 2 Filter Section
G4–G0		Attenuation Adjustment for the Magnitude of the Cancellation Signal. Range is – 2.5 dB (00000) to – 8.5 dB (11000)

(*) State at power on initialization
Setting = Please refer to software TS5077 2

Figure 1 shows a simplified diagram of the local echo path for a typical application with a transformer interface. The magnitude and phase of the local echo signal, measured at VF_XI, are a function of the termination impedance Z_T, the line transformer and the impedance of the 2 W loop, Z_L. If the impedance reflected back into the transformer primary is expressed as Z_L' then the echo path transfer function from VF_RO to VF_XI is :

$$H(W) = Z_L' / (Z_T + Z_L') \quad (1)$$

Figure 1: Simplified Diagram of Hybrid Balance Circuit



PROGRAMMING THE FILTER

On initial power-up the Hybrid Balance filter is disabled. Before the hybrid balance filter can be programmed it is necessary to design the transformer and termination impedance in order to meet system 2 W input return loss specifications, which are normally measured against a fixed test impedance (600 or 900 Ω in most countries). Only then can the echo path be modeled and the hybrid balance filter programmed. Hybrid balancing is also measured against a fixed test impedance, specified by each national Telecom administration to provide adequate control of talker and listener echo over the majority of their network connections. This test impedance is Z_L in figure 1. The echo signal and the degree of transhybrid loss obtained by the programmable filter must be measured from the PCM digital input D_R0, to the PCM digital output D_X0, either by digital test signal analysis or by conversion back to analog by a PCM CODEC/Filter.

Three registers must be programmed in COMBO IIG to fully configure the Hybrid Balance Filter as follows :

Register 1: select/de-select Hybrid Balance Filter; invert/non-invert cancellation signal; select/de-select Hybal2 filter section; attenuator setting.

Register 2: select/de-select Hybal1 filter; set Hybal1 to Bi-Quad or 1st order; program pole and zero frequency.

Table 10: Hybrid Balance Register 2 Byte 2 instructions

Bit Number								Function
7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	By Pass Hybal 1 Filter
X	X	X	X	X	X	X	X	Pole/zero Setting

Register 3 : program pole frequency in Hybal2 filter; program zero frequency in Hybal2 filter; settings = Please refer to software TS5077-2.

Standard filter design techniques may be used to model the echo path (see equation (1)) and design a matching hybrid balance filter configuration. Alternatively, the frequency response of the echo path can be measured and the hybrid balance filter programmed to replicate it.

An Hybrid Balance filter design guide and software optimization program are available under license from SGS-THOMSON Microelectronics (order TS5077-2).

APPLICATION INFORMATION

Figure 2 shows a typical application of the TS5070 together with a transformer SLIC.

The design of the transformer is greatly simplified due to the on-chip hybrid balance cancellation filter. Only one single secondary winding is required (see application note AN.091 - Designing a subscriber line card module using the TS5070/COMBO IIG). Figures 3 and 4 show an arrangement with SGS-Thomson monolithic SLICS.

POWER SUPPLIES

While the pins of the TS5070 and TS5071/COMBO IIG devices are well protected against electrical misuse, it is recommended that the standard CMOS practice of applying GND to the device before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used and a Schottky diode connected between V_{SS} and GND. To minimize noise sources all ground connections to each device should meet at a common point as close as possible to the GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. Power supply decoupling capacitors of 0.1 µF should be connected from this common device ground point to V_{CC} and V_{SS} as close to the device pins as possible. V_{CC} and V_{SS} should also be decoupled with low effective series resis-tance capacitors of at least 10 µF located near the card edge connector.

Figure 2: Transformer SLIC + COMBO IIG.

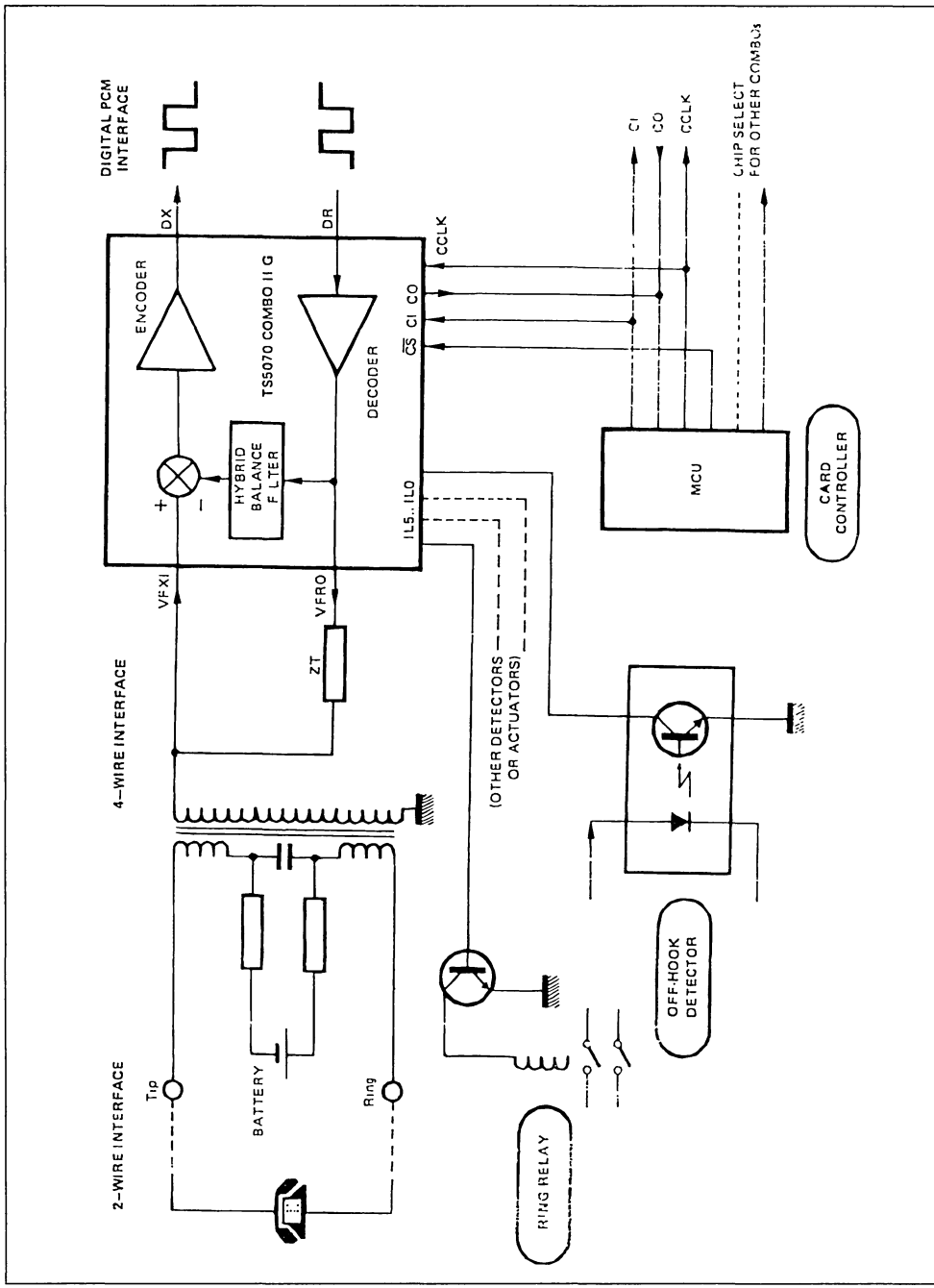
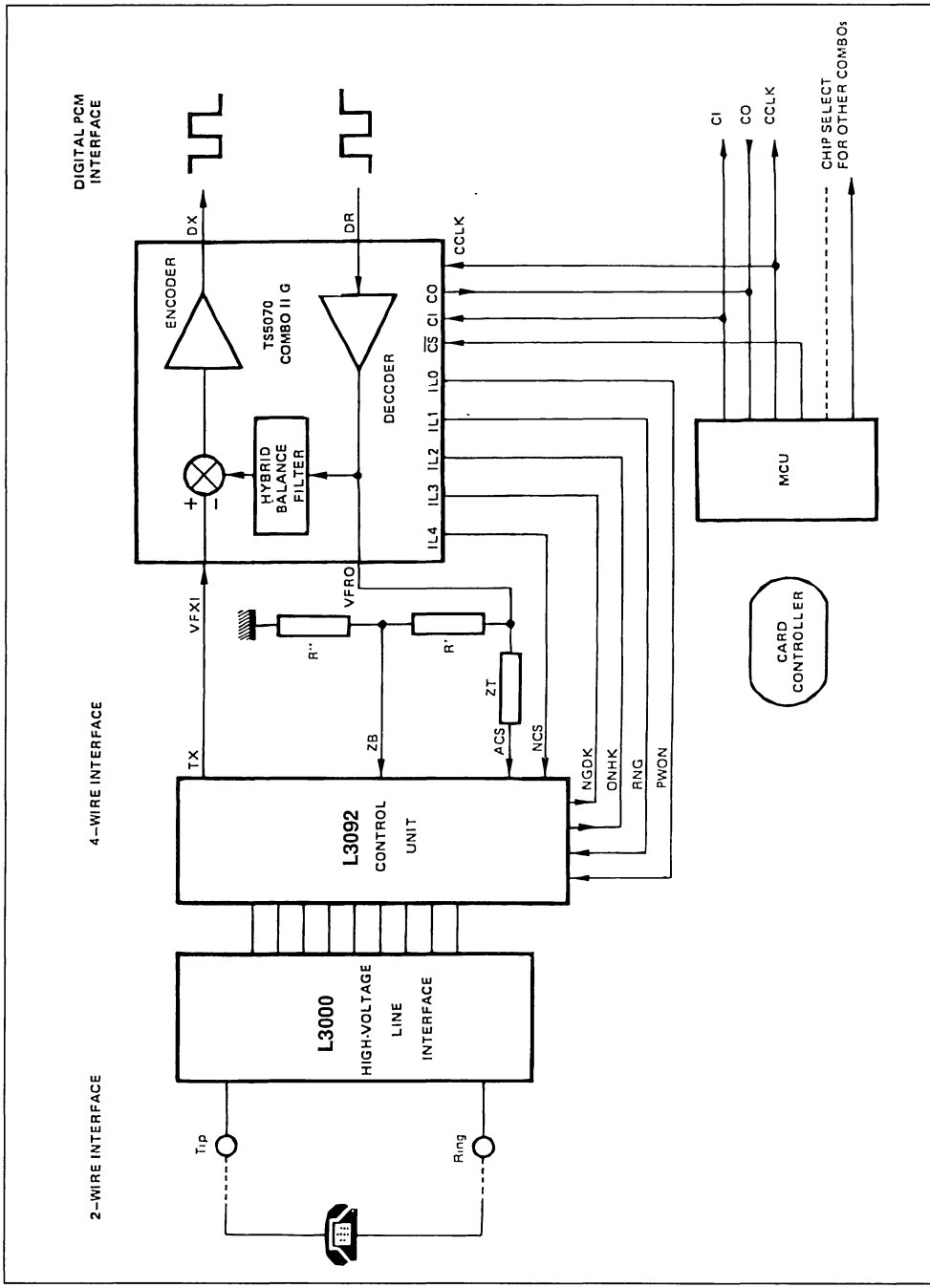


Figure 4: Interface with L3092 + L3000 Silicon SLIC.



ELECTRICAL OPERATING CHARACTERISTICS

Unless otherwise noted, limits in **BOLD** characters are guaranteed for V_{CC} = + 5 V ± 5 % ; V_{SS} = − 5 V ± 5 %. T_A = 0 °C to 70 °C by correlation with 100% electrical testing at T_A = 25 °C. All other limits are assured by correlation with other production tests and/or product design and characterisation. All signals referenced to GND. Typicals specified at V_{CC} = + 5 V, V_{SS} = − 5 V, T_A = 25 °C.

DIGITAL INTERFACE

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage All Digital Inputs (DC measurement)			**0.7**	V
V_{IH}	Input High Voltage All Digital Inputs (DC measurement)	**2.0**			V
V_{OL}	Output Low Voltage D_X0 and D_X1, TS_X0, TS_X1 and CO, I_L = 3.2mA All Other Digital Outputs, I_L = 1mA			 **0.4**	 V
V_{OH}	Output High Voltage DX0 and DX1 and CO, I_L = -3.2mA All other digital outputs except TS_X, I_L = -1mA All Digital Outputs, I_L = -100µA	 **2.4** V_{CC}-0.5			 V V
I_{IL}	Input Low Current all Digital Inputs (GND < V_{IN} < V_{IL})	**-10**		**10**	µA
I_{IH}	Input High Current all Digital Inputs Except MR (V_{IH} < V_{IN} < V_{CC})	**-10**		**10**	µA
I_{IH}	Input High Current on MR	**-10**		**100**	µA
I_{OZ}	Output Current in High Impedance State (TRI-STATE) DX0 and DX1, CO and CI/O (as an input) IL5-IL0 as inputs (GND < V_O < V_{CC})	**-10**		**10**	µA

ANALOG INTERFACE

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{VFXI}	Input Current VF_XI (-3.3V < VF_XI < 3.3V)	**-10**		**10**	µA
R_{VFXI}	Input Resistance VF_XI (-3.3V < VF_XI < 3.3V)	**390**	**620**		kΩ
VOS_X	Input offset voltage at VF_XI 0dBm0 = -19dBm 0dBm0 = +6.4dBm			 10 200	 mV mV
RL_{VFRO}	Load Resistance at VF_RO 0dBm0 = 8.1dBm 0dBm0 = 7.6dBm 0dBm0 = 6.9dBm	 **15** **600** **300**			 kΩ Ω Ω
CL_{VFRO}	Load Capacitance CLVFRO from VFRO to GND			**200**	pF
RO_{VFRO}	Output Resistance VFRO (steady zero PCM code applied to DR0 or D_R1)		**1**	**3**	Ω
V_{OSR}	Output Offset Voltage at VF_RO (alternating ±zero PCM code applied to D_R0 or D_R1, 0dBm0 = 8.1dBm)	**-200**		**200**	mV

ELECTRICAL OPERATING CHARACTERISTICS (continued)

POWER DISSIPATION

Symbol	Parameter	Min.	Typ.	Max.	Unit
ICC0	Power Down Current (CCLK, CI/O, CI = 0.4V, $\overline{CS}$ = 2.4V) Interface Latches set as Outputs with no load All over Inputs active, Power Amp Disabled		0.3	**1.5**	mA
-ISS0	Power Down Current (as above)		0.1	**0.3**	mA
ICC1	Power Up Current (CCLK, CI/O, CI = 0.4V, $\overline{CS}$ = 2.4V) No Load on Power Amp Interface Latches set as Outputs with no Load		7	**11**	mA
-ISS1	Power Up Current (as above)		7	**11**	mA
ICC2	Power Down Current with Power Amp Enabled		2	**3**	mA
-ISS2	Power Down Current with Power Amp Enabled		2	**3**	mA

TIMING SPECIFICATIONS

Unless otherwise noted, limits in BOLD characters are guaranteed for V_{CC} = + 5 V ± 5 %; V_{SS} = -5V ± 5 %. T_A = 0 °C to 70 °C by correlation with 100 % electrical testing at T_A = 25 °C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = + 5 V, V_{SS} = -5 V, T_A = 25 °C. All timing parameters are measured at V_{OH} = 2.0 V and V_{OL} = 0.7 V.

See Definitions and Timing Conventions section for test methods information.

MASTER CLOCK TIMING

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{MCLK}	Frequency of MCLK (selection of frequency is programmable, see table 2)		512 1.536 1.544 2.048 **4.096**		kHz MHz MHz MHz MHz
t_{WMH}	Period of MCLK High (measured from V_{IH} to V_{IH}, see note 1)	**80**			ns
t_{WML}	Period of MCLK Low (measured from V_{IL} to V_{IL}, see note 1)	**80**			ns
t_{RM}	Rise Time of MCLK (measured from V_{IL} or V_{IH})			30	ns
t_{FM}	Fall Time of MCLK (measured from V_{IH} to V_{IL})			30	
t_{HBM}	Hold Time, BCLK Low to MCLK High (TS5070 only)	**50**			ns
t_{WFL}	Period of FS_X or FS_R Low (Measured from V_{IL} to V_{IL})	1			(*)

(*) MCLK period

TIMING SPECIFICATIONS (continued)

PCM INTERFACE TIMING

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{BCLK}	Frequency of BCLK (may vary from 64KHz to 4.096MHz in 8KHz increments, TS5070 only)	**64**		**4096**	kHz
t_{WBH}	Period of BCLK High (measured from V_{IH} to V_{IH})	**80**			ns
t_{WBL}	Period of BCLK Low (measured from V_{IL} to V_{IL})	**80**			ns
t_{RB}	Rise Time of BCLK (measured from V_{IL} to V_{IH})			30	ns
t_{FB}	Fall Time of BCLK (measured from V_{IH} to V_{IL})			30	ns
t_{HBF}	Hold Time, BCLK Low to $FS_{X/R}$ High or Low	**30**			ns
t_{SFB}	Setup Time $FS_{X/R}$ High to BCLK Low	**30**			ns
t_{DBD}	Delay Time, BCLK High to Data Valid (load = 100pF plus 2 LSTTL loads)			**80**	ns
t_{DBZ}	Delay Time from BCLK8 Low to Dx Disabled (if FSx already low); FSx Low to Dx Disabled (if BCLK8 low); BCLK9 High to Dx Disabled (if FSx still high)	**15**		80	ns
t_{DBT}	Delay Time from BCLK and FSx Both High to $\overline{TSx}$ Low (Load = 100pF plus 2 LSTTL loads)			**60**	ns
t_{ZBT}	Delay Time from BCLK8 low to $\overline{TSx}$ Disabled (if FSx already low); FSx Low to $\overline{TSx}$ Disabled (if BCLK8 low); BCLK9 High to TSx Disabled (if FSx still high);	15		60	ns
t_{DFD}	Delay Time, FSx High to Data Valid (load = 100pF plus 2 LSTTL loads, applies if FSx rises later than BCLK rising edge in non-delayed data mode only)			**80**	ns
t_{SDB}	Setup Time, D_R 0/1 Valid to BCLK Low	**30**			ns
t_{HBD}	Hold Time, BCLK Low to DR0/1 Invalid	**20**			ns

Figure 5: Non Delayed Data Timing (short frame mode)

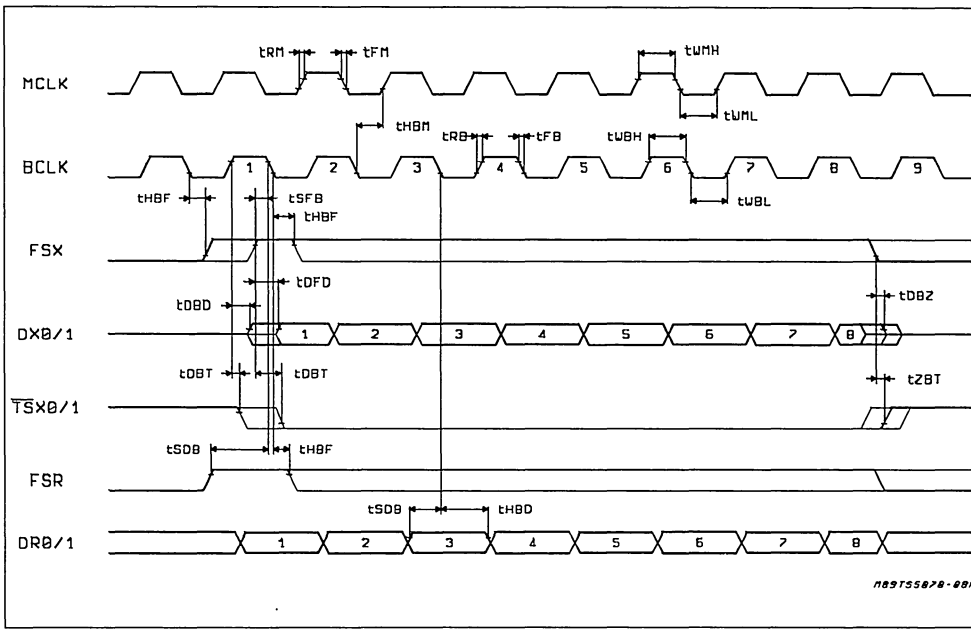
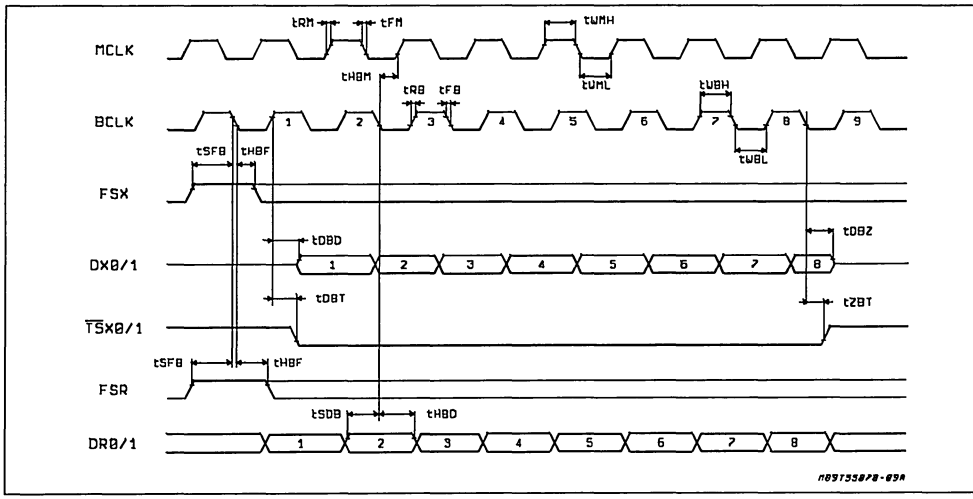


Figure 6: Delayed Data Timing (short frame mode)



SERIAL CONTROL PORT TIMING

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{CCLK}	Frequency of CCLK			**2.048**	MHz
t_{WCH}	Period of CCLK High (measured from V_{IH} to V_{IH})	**160**			ns
t_{WCL}	Period of CCLK Low (measured from V_{IL} to V_{IL})	**160**			ns
t_{RC}	Rise Time of CCLK (measured from V_{IL} to V_{IH})			50	ns
t_{FC}	Fall Time of CCLK (measured from V_{IH} to V_{IL})			50	ns
t_{HCS}	Hold Time, CCLK Low to $\overline{CS}$ Low (CCLK1)	**10**			ns
t_{HSC}	Hold Time, CCLK Low to $\overline{CS}$ High (CCLK8)	**100**			ns
t_{SSC}	Setup Time, $\overline{CS}$ Transition to CCLK Low	**70**			ns
t_{SSCO}	Setup Time, $\overline{CS}$ Transition to CCLK High (to insure CO is not enabled for single byte)	**50**			ns
t_{SDC}	Setup Time, CI (CI/O) Data in to CCLK low	**50**			ns
t_{HCD}	Hold Time, CCLK Low to CI (CI/O) Invalid	50			ns
t_{DCD}	Delay Time, CCLK High to CO (CI/O) Data Out Valid (load = 100 pF plus 2 LSTTL loads)			**50**	ns
t_{DSD}	Delay Time, $\overline{CS}$ Low to CO (CI/O) Valid (applies only if separate $\overline{CS}$ used for byte 2)			**50**	ns
t_{DDZ}	Delay Time, $\overline{CS}$ or CCLK9 High to CO (CI/O) High Impedance (applies to earlier of $\overline{CS}$ high or CCLK9 high)	15		80	ns

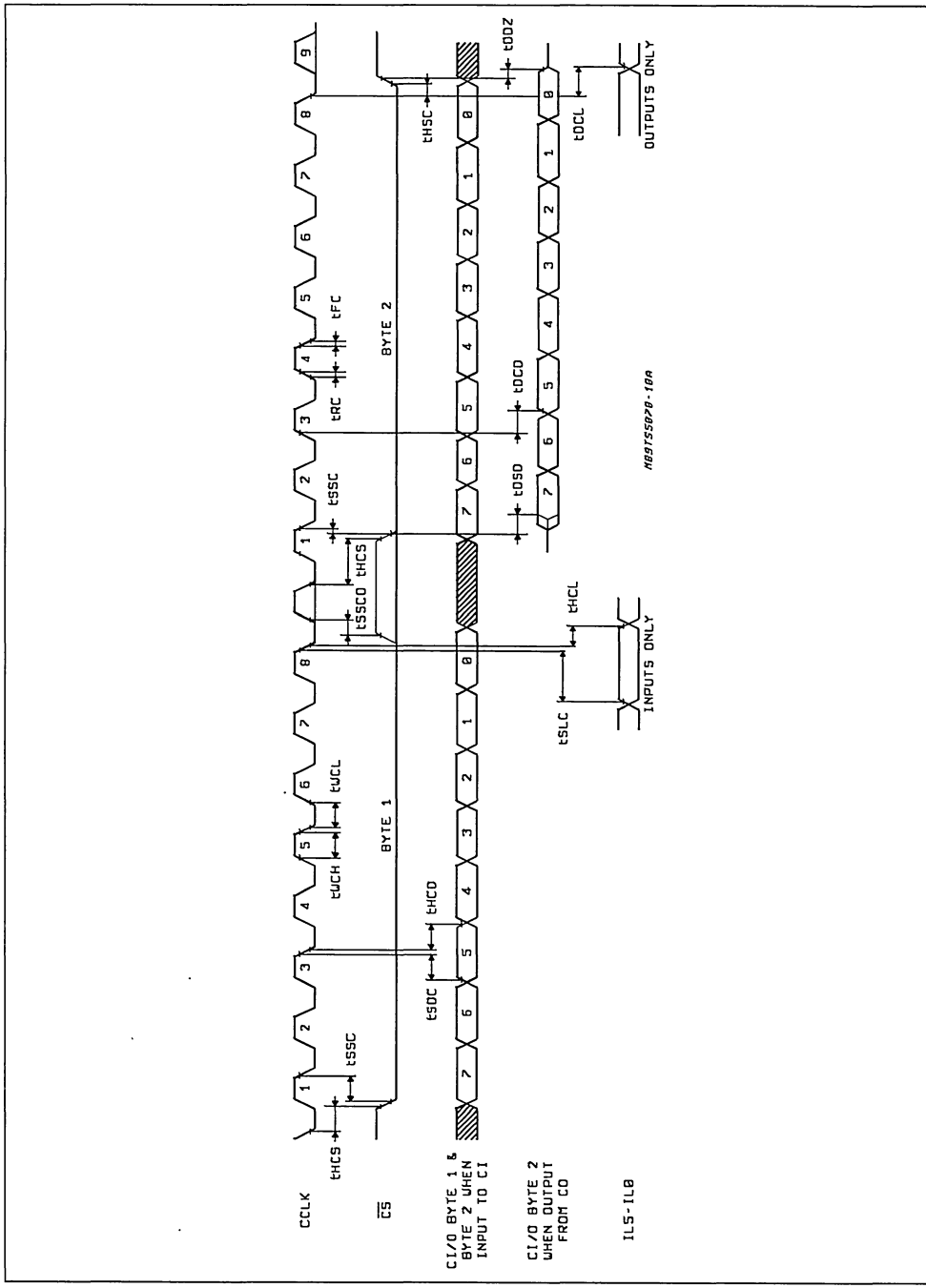
INTERFACE LATCH TIMING

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SLC}	Setup Time, I_L Valid to CCLK 8 of Byte 1 Low. I_L as Input	**100**			ns
t_{HCL}	Hold Time, I_L Valid from CCLK 8 of Byte 1 Low. I_L as Input	50			ns
t_{DCL}	Delay Time, CCLK 8 of Byte 2 Low to I_L. C_L = 50 pF. I_L as Output			200	ns

MASTER RESET PIN

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WMR}	Duration of Master Reset High	1			µs

Figure 7: Control Port Timing



TRANSMISSION CHARACTERISTICS

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = + 5 V ± 5 % ; V_{SS} = – 5 V ± 5 %, T_A = 0 °C to 70 °C by correlation with 100 % electrical testing at T_A = 25 °C (-40°C to 85°C for TS5070-X and TS5071-X).

f = 1031.25 Hz, VF_XI = 0 dBm0, D_R0 or D_R1 = 0 dBm0 PCM code, Hybrid Balance filter disabled. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. dBm levels are into 600 ohms. Typicals specified at V_{CC} = + 5 V, V_{SS} = -5 V, T_A = 25 °C.

AMPLITUDE RESPONSE

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Absolute levels				
	The nominal 0 dBm 0 levels are :				
	VF_XI 0 dB Tx Gain		1.618		Vrms
	25.4 dB Tx Gain		86.9		mVrms
	VF_RO 0 dB Rx Attenuation (RL ≥ 15 kΩ)		1.968		Vrms
	0.5 dB Rx Attenuation (RL ≥ 600 Ω)		1.858		Vrms
	1.2 dB Rx Attenuation (RL ≥ 300 Ω)		1.714		Vrms
	25.4 dB Rx Attenuation		105.7		mVrms
	Maximum Overload				
	The nominal overload levels are :				
	A-law				
	VF_XI 0 dB Tx Gain		2.323		Vrms
	25.4 dB Tx Gain		124.8		mVrms
	VF_RO 0 dB Rx Attenuation (R_L ≥ 15 kΩ)		2.825		Vrms
	0.5 dB Rx Attenuation (R_L ≥ 300 Ω)		2.667		Vrms
	1.2 dB Rx Attenuation (R_L ≥ 300 Ω)		2.461		Vrms
	25.4 dB Rx Attenuation		151.7		mVrms
	μ-law				
	VF_XI 0 dB Tx Gain		2.332		Vrms
	25.4 dB Tx Gain		125.2		mVrms
	VF_RO 0 dB Rx Attenuation (R_L ≥ 15 kΩ)		2.836		Vrms
	0.5 dB Rx Attenuation (R_L ≥ 600 Ω)		2.677		Vrms
	1.2 dB Rx Attenuation (R_L ≥ 300 Ω)		2.470		Vrms
	25.4 dB Rx Attenuation		152.3		mVrms
	Transmit Gain Absolute Accurary				
GXA	Transmit Gain Programmed for 0 dBm0 = 6.4 dBm, A-law Measure Deviation of Digital Code from Ideal 0 dBm0 PCM Code at $D_X0/1$, f = 1031.25 Hz T_A = 25 °C, V_{CC} = 5 V, V_{SS} = – 5 V	**– 0.15**		**0.15**	dB
	Transmit gain Variation with Programmed Gain				
GXAG	– 19 dBm ≤ 0 dBm0 ≤ 6.4 dBm Calculate the Deviation from the Programmed Gain Relative to GXA i.e., GXAG = Gactual – Gprog – GXA T_A = 25 °C, V_{CC} = 5 V, V_{SS} = – 5 V	**– 0.1**		**0.1**	dB

AMPLITUDE RESPONSE (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
GXAF	**Transmit Gain Variation with Frequency**				
	Relative to 1031.25 Hz (note 2)				
	-19 dBm ≤ o dBm0 ≤ 6.4 dBm				
	D_R0 (or D_R1) = 0 dBm0 Code				
	f = 60Hz			-26	dB
	f = 200 Hz	-1.8		-0.1	dB
	f = 300 Hz to 3000 Hz	-0.15		0.15	dB
	f = 3400 Hz	-0.7		0	dB
	f = 4000 Hz			-14	dB
	f > 4600 Hz Measure Response at Alias Frequency from 0 kHz to 4 kHz			-32	dB
	0 dBm0 = 6.4 dBm				
	VFXI = -4 dBm0 (note2)				
	f = 62.5 Hz			**-24.9**	dB
	f = 203.125 Hz	**-1.7**		**-0.1**	dB
	f = 2093.750 Hz	**-0.15**		**0.15**	dB
	f = 2984.375 Hz	**-0.15**		**0.15**	dB
	f = 3296.875 Hz	**-0.15**		**0.15**	dB
	f = 3406.250 Hz	**-0.74**		**0**	dB
	f = 3984.375 Hz			**-13.5**	dB
	f = 5250 Hz, Measure 2750 Hz			**-32**	dB
	f = 11750Hz, Measure 3750 Hz			**-32**	dB
	f = 49750 Hz, Measure 1750 Hz			**-32**	dB
GXAT	**Transmit Gain Variation with Temperature**				
	Measured Relative to GXA, VCC = 5V, VSS = -5V -19dBm < 0dBm < 6.4dBm	-0.1		0.1	dB
GXAV	**Transmit Gain Variation with Supply**				
	V_{CC} = 5V ± 5%, V_{SS} = -5V ± 5%				
	Measured Relative to GXA				
	T_A = 25 °C, o dBm0 = 6.4dBm	**-0.05**		**0.05**	dB
GXAL	**Transmit Gain Variation with Signal Level**				
	Sinusoidal Test Method, Reference Level = 0 dBm0				
	VF_XI = -40 dBm0 to + 3 dBm0	**-0.2**		**0.2**	dB
	VF_XI = -50 dBm0 to -40 dBm0	**-0.4**		**0.4**	dB
	VF_XI = -55 dBm0 to -50 dBm0	**-1.2**		**1.2**	dB
GRA	**Receive Gain Absolute Accuracy**				
	0 dBm0 = 8 1 dBm, A-law				
	Apply 0 dBm0 PCM Code to D_R0 or D_R1 Measure VF_RO, f =1015.625Hz	**-0.15**		**0.15**	dB
	T_A = 25 °C, V_{CC} = 5V, V_{SS} = -5V				
GRAG	**Receive Gain Variation with Programmed Gain**				
	-17.3 dBm ≤ 0 dBm0 ≤ 8.1 dBm				
	Calculate the Deviation from the Programmed Gain Relative to GRA	**-0.1**		**0.1**	dB
	I.e. GRAG = Gactual - Gprog - GRA T_A = 25°C, V_{CC} = 5V, V_{SS} = -5V				

AMPLITUDE RESPONSE (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
GRAT	**Receive Gain Variation with Temperature**				
	Measure Relative to GRA				
	V_{CC} = 5V, V_{SS} = -5V -17dBm ≤ 0dBm0 ≤ 8.1dBm	-0.1		0.1	dB
GRAV	**Receive Gain Variation with Supply**				
	Measured Relative to GRA				
	V_{CC} = 5V ± 5%, V_{SS} = -5V ± 5%	**-0.05**		**0.05**	dB
	T_A = 25°C, 0dBm 0 = 8.1 dBm				
GRAF	**Receive Gain Variation with Frequency**				
	Relative to 1015.625 Hz, (note 2)				
	D_R0 or D_R1 = 0 dBm0 Code				
	-17.3dBm ≤ 0 dBm0 ≤ 8.1dBm				
	f = 200Hz	-0.25		0.15	dB
	f = 300Hz to 3000Hz	-0.15		0.15	dB
	f = 3400Hz	-0.7		0	dB
	f = 4000Hz			-14	dB
	GR = 0dBm0 = 8.1dBm				
	D_R0 = -4dBm0				
	Relative to 1015.625 (note 2)				
	f = 296.875 Hz	**-0.15**		**0.15**	dB
	f = 1906.250Hz	**-0.15**		**0.15**	dB
	f = 2812.500Hz	**-0.15**		**0.15**	dB
	f = 2984.375Hz	**-0.15**		**0.15**	dB
	f = 3406.250Hz	**-0.74**		**0**	dB
	f = 3984.375Hz			**-13.5**	dB
GRAL	**Receive Gain Variation with Signal Level**				
	Sinusoidal Test Method Reference Level = 0dBm0				
	D_R0 = -40dBm0 to +3dBm0	**-0.2**		**0.2**	dB
	D_R0 = -50dBm0 to -40dBm0	**-0.4**		**0.4**	dB
	D_R0 = -55dBm0 to -50dBm0	**-1.2**		**1.2**	dB
	DR0 = 3.1dBm0				
	R_L = 600Ω, 0dBm0 = 7.6dBm	-0.2		0.2	dB
	R_L = 300Ω, 0dBm0 = 6.9dBm	-0.2		0.2	dB

ENVELOPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Min.	Typ.	Max.	Unit
DXA	**Tx Delay Absolute**				
	f = 1600 Hz			315	µs
DXR	**Tx Delay, Relative to DXA**				
	f = 500 – 600 Hz			220	µs
	f = 600 – 800 Hz			145	µs
	f = 800 – 1000 Hz			75	µs
	f = 1000 – 1600 Hz			40	µs
	f = 1600 – 2600 Hz			75	µs
	f = 2600 – 2800 Hz			105	µs
	f = 2800 – 3000 Hz			155	µs
DRA	**Rx Delay, Absolute**				
	f = 1600 Hz			200	µs
DRR	**Rx Delay, Relative to DRA**				
	f = 500 – 1000 Hz	– 40			µs
	f = 1000 – 1600 Hz	– 30			µs
	f = 1600 – 2600 Hz			90	µs
	f = 2600 – 2800 Hz			125	µs
	f = 2800 – 3000 Hz			175	µs

NOISE

Symbol	Parameter	Min.	Typ.	Max.	Unit
NXC	**Transmit Noise, C Message Weighted** μ-law Selected (note 3) 0 dBm0 = 6.4dBm		12	15	dBrnC0
NXP	**Transmit Noise, Psophometric Weighted** A-law Selected (note 3) 0 dBm0 = 6.4dBm		-74	**-67**	dBm0p
NRC	**Receive Noise, C Message Weighted** μ-law Selected PCM code is alternating positive and negative zero		8	11	dBrnC0
NRP	**Receive Noise, Psophometric Weighted** A-law Selected PCM Code Equals Positive Zero		-82	**-79**	dBm0p
NRS	**Noise, Single Frequency** f = 0Hz to 100kHz, Loop Around Measurement VF_XI = 0Vrms			-53	dBm0
PPSRX	**Positive Power Supply Rejection Transmit** V_{CC} = $5V_{DC}$ + 100mVrms f = 0Hz to 4000Hz (note 4) f = 4kHz to 50kHz	 **30** 30			 dBp dBp
NPSRX	**Negative Power Supply Rejection Transmit** V_{SS} = $-5V_{DC}$ + 100mVrms f = 0Hz to 4000Hz (note 4) f = 4kHz to 50kHz	 **30** 30			 dBp dBp
PPSRR	**Positive Power Supply Rejection Receive** PCM Code Equals Positive Zero V_{CC} = $5V_{DC}$ + 100mVrms Measure VFR0 f = 0Hz to 4000Hz f = 4kHz to 25kHz f = 25kHz to 50kHz	 **30** 40 36			 dBp dB dB
NPSRR	**Negative Power Supply Rejection Receive** PCM Code Equals Positive Zero V_{SS} = $-5V_{DC}$ + 100mVrms Measure VFR0 f = 0Hz to 4000Hz f = 4kHz to 25kHz f = 25kHz to 50kHz	 **30** 40 36			 dBp dB dB
SOS	**Spurious Out-of Band Signals at the Channel Output** 0dBm0 300Hz to 3400Hz input PCM code applied at D_R0 (D_R1) Relative to f = 1062.5Hz 4600Hz to 7600Hz 7600Hz to 8400Hz 8400Hz to 50000Hz			 -30 -40 -30	 dB dB dB

DISTORTION

Symbol	Parameter	Min.	Typ.	Max.	Unit
STDX	**Signal to Total Distortion Transmit** Sinusoidal Test Method Half Channel				
	Level = 3dBm0	**33**			dBp
	Level = -30dBm0 to 0dBm0	**36**			dBp
	Level = -40dBm0	**30**			dBp
	Level = -45dBm0	**25**			dBp
STDR	**Signal to Total Distortion Receive** Sinusoidal Test Method Half Channel				
	Level = 3dBm0	**33**			dBp
	Level = -30dBm0 to 0dBm0	**36**			dBp
	Level = -40dBm0	**30**			dBp
	Level = -45dBm0	**25**			dBp
SFDX	**Single Frequency Distortion Transmit**			**-46**	dB
SFDR	**Single Frequency Distortion Receive**			**-46**	dB
IMD	**Intermodulation Distortion Transmit or Receive** Two Frequencies in the Range 300Hz to 3400Hz			**-41**	dB

CROSSTALK

Symbol	Parameter	Min.	Typ.	Max.	Unit
CTX-R	**Transmit to Receive Crosstalk,** 0dBm0 Transmit Level f = 300 to 3400Hz DR = Idle PCM Code		-90	**-75**	dB
CTR-X	**Receive to Transmit Crosstalk,** 0dBm0 Receive Level f = 300 to 3400Hz (note 4)		-90	**-70**	dB

Notes:
1. Applies only to MCLK frequencies ≥ 1.536 MHz. At 512 kHz A 50:50 ± 2 % duty cycle must be used.

2. A multi-tone test technique is used (peak/rms ≤ 9.5 dB).

3. Measured by grounded input at VF_XI.

4. PPSRX, NPSRX and CTR-X are measured with a – 50 dBm0 activation signal applied to VF_XI.

A signal is Valid if it is above V_{IH} or below V_{IL} and invalid if it is between V_{IL} and V_{IH} For the purpose of the specification the following conditions apply :

a) All input signals are defined as V_{IL} = 0.4 V, V_{IH} = 2.7 V, t_R < 10 ns, t_F 10 ns

b) t_R is measured from V_{IL} to V_{IH}, t_F is measured from V_{IH} to V_{IL}

c) Delay Times are measured from the input signal Valid to the clock input invalid

d) Setup Times are measured from the data input Valid to the clock input invalid

e) Hold Times are measured from the clock signal Valid to the data input invalid

f) Pulse widths are measured from V_{IL} to V_{IL} or from V_{IH} to V_{IH}

DEFINITIONS AND TIMING CONVENTIONS

DEFINITIONS

V_{IH}	VIH is the D.C. input level above which an input level is guaranteed to appear as a logical one. This parameter is to be measured by performing a functional test at reduced clock speeds and nominal timing (i.e. not minimum setup and hold times or output strobes), with the high level of all driving signals set to V_{IH} and maximum supply voltages applied to the device.
V_{IL}	VIL is the D.C. input level below which an input level is guaranteed to appear as a logical zero the device. This parameter is measured in the same manner as V_{IH} but with all driving signal low levels set to V_{IL} and minimum supply voltage applied to the device.
V_{OH}	VOH is the minimmum D.C. output level to which an output placed in a logical one state will converge when loaded at the maximum specified load current.
V_{OL}	VOL is the maximum D.C. output level to which an output placed in a logical zero state will converge when loaded at the maximum specified load current.
Threshold Region Valid Signal	The threshold region is the range of input voltages between V_{IL} and V_{IH}. A signal is Valid if it is in one of the valid logic states. (i.e. above V_{IH} or below V_{IL}). In timing specifications, a signal is deemed valid at the instant it enters a valid state.
Invalid signal	A signal is invalid if it is not in a valid logic state, i.e., when it is in the threshold region between V_{IL} and V_{IH}. In timing specifications, a signal is deemed Invalid at the instant it enters the threshold region.

TIMING CONVENTIONS

For the purpose of this timing specifications the following conventions apply :

Input Signals	All input signals may be characterized as : V_L = 0.4 V, V_H = 2.4 V, tR < 10 ns, tF < 10 ns.
Period	The period of the clock signal is designated as tPxx where xx represents the mnemonic of the clock signal being specified.
Rise Time	Rise times are designated as tRyy, where yy represents a mnemonic of the signal whose rise time is being specified, tRyy is measured from V_{IL} to V_{IH}.
Fall Time	Fall times are designated as tFyy, where yy represents a mnemonic of the signal whose fall time is being specified, tFyy is measured from V_{IH} to V_{IL}.
Pulse Width High	The high pulse width is designated as tWzzH, where zz represents the mnemonic of the input or output signal whose pulse width is being specified. High pulse width are measured from V_{IH} to V_{IH}.
Pulse Width Low	The low pulse is designated as tWzzL' where zz represents the mnemonic of the input or output signal whose pulse width is being specified. Low pulse width are measured from V_{IL} to V_{IL}.
Setup Time	Setup times are designated as tSwwxx where ww represents the mnemonic of the input signal whose setup time is being specified relative to a clock or strobe input represented by mnemonic xx. Setup times are measured from the ww Valid to xx Invalid.
Hold Time	Hold times are designated as THwwxx where ww represents the mnemonic of the input signal whose hold time is being specified relative to a clock or strobe input represented by the mnemonic xx. Hold times are measured from xx Valid to ww Invalid
Delay Time	Delay times are designated as TDxxyy [H/L], where xx represents the mnemonic of the input reference signal and yy represents the mnemonic of the output signal whose timing is being specified relative to xx. The mnemonic may optionally be terminated by an H or L to specify the high going or low going transition of the output signal. Maximum delay times are measured from xx Valid to yy Valid. Minimum delay times are measured from xx Valid to yy Invalid. This parameter is tested under the load conditions specified in the Conditions column of the Timing Specifications section of this datasheet.

PROTECTION DEVICES DATASHEETS

SGS-THOMSON MICROELECTRONICS

1.5KE6V8P,A/440P,A
1.5KE6V8CP,CA/440CP,CA

TRANSIL

FEATURES

- PEAK PULSE POWER= 1500 W @ 1ms.
- BREAKDOWN VOLTAGE RANGE : From 6V8 to 440 V.
- UNI AND BIDIRECTIONAL TYPES.
- LOW CLAMPING FACTOR.
- FAST RESPONSE TIME: Tclamping : 1ps (0 V to VBR).
- UL RECOGNIZED.

CB429
(Plastic)

DESCRIPTION

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous reponse to transients makes them particularly suited to protect voltage sensitive devices such as MOS Technology and low voltage supplied IC's.

MECHANICAL CHARACTERISTICS

- Body marked with : Logo, Date Code, Type Code, and Cathode Band (for unidirectional types only).
- Tinned copper leads.
- High temperature soldering.

ABSOLUTE RATINGS (limiting values)

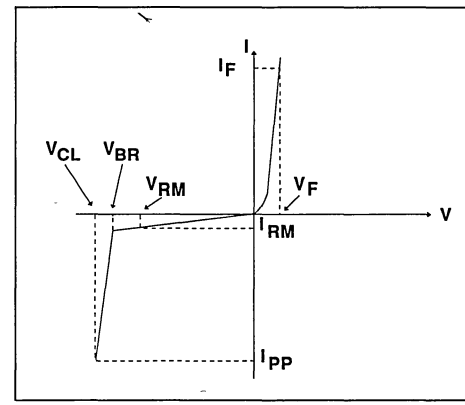
Symbol	Parameter		Value	Unit
P_p	Peak pulse power dissipation See note 1 and derating curve Fig 1.	Tamb = 25°C	1500	W
P	Power dissipation on infinite heatsink See note 1 and derating curve Fig 1.	Tlead = 75°C	5	W
I_{FSM}	Non repetitive surge peak forward current For Unidirectional types.	Tamb = 25°C t =10 ms	250	A
T_{stg} T_j	Storage and junction temperature range		- 65 to + 175 175	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		230	°C

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction-leads on infinite heatsink	20	°C/W
R_{th} (j-a)	Junction to ambient. on printed circuit. L_{lead} = 10 mm	75	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage.
V_{BR}	Breakdown voltage.
V_{CL}	Clamping voltage.
I_{RM}	Leakage current @ VRM.
I_{PP}	Surge current.
αT	Voltage temperature coefficient.
V_F	Forward Voltage drop V_F < 3.5V @ I_F = 100 A.



TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min	nom	max note2		V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Unidirectional	Bidirectional	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
P 1.5KE6V8P	P 1.5KE6V8CP	1000	5.8	6.45	6.8	7.48	10	10.5	143	13.4	746	5.7	9500
P 1.5KE6V8A	P 1.5KE6V8CA	1000	5.8	6.45	6.8	7.14	10	10.5	143	13.4	746	5.7	9500
P 1.5KE7V5P	1.5KE7V5CP	500	6.4	7.13	7.5	8.25	10	11.3	132	14.5	690	6.1	8500
1.5KE7V5A	P 1.5KE7V5CA	500	6.4	7.13	7.5	7.88	10	11.3	132	14.5	690	6.1	8500
1.5KE8V2P	1.5KE8V2CP	200	7.02	7.79	8.2	9.02	10	12.1	124	15.5	645	6.5	8000
P 1.5KE8V2A	P 1.5KE8V2CA	200	7.02	7.79	8.2	8.61	10	12.1	124	15.5	645	6.5	8000
1.5KE9V1P	1.5KE9V1CP	50	7.78	8.65	9.1	10	1	13.4	112	17.1	585	6.8	7500
1.5KE9V1A	1.5KE9V1CA	50	7.78	8.65	9.1	9.55	1	13.4	112	17.1	585	6.8	7500
1.5KE10P	1.5KE10CP	10	8.55	9.5	10	11	1	14.5	103	18.6	538	7.3	7000
P 1.5KE10A	P 1.5KE10CA	10	8.55	9.5	10	10.5	1	14.5	103	18.6	538	7.3	7000
1.5KE11P	1.5KE11CP	5	9.4	10.5	11	12.1	1	15.6	96	20.3	493	7.5	6400
1.5KE11A	1.5KE11CA	5	9.4	10.5	11	11.6	1	15.6	96	20.3	493	7.5	6400
1.5KE12P	P 1.5KE12CP	5	10.2	11.4	12	13.2	1	16.7	90	21.7	461	7.8	6000
P 1.5KE12A	P 1.5KE12CA	5	10.2	11.4	12	12.6	1	16.7	90	21.7	461	7.8	6000
1.5KE13P	1.5KE13CP	5	11.1	12.4	13	14.3	1	18.2	82	23.6	423	8.1	5500
P 1.5KE13A	P 1.5KE13CA	5	11.1	12.4	13	13.7	1	18.2	82	23.6	423	8.1	5500
P 1.5KE15P	P 1.5KE15CP	5	12.8	14.3	15	16.5	1	21.2	71	27.2	368	8.4	5000
P 1.5KE15A	P 1.5KE15CA	5	12.8	14.3	15	15.8	1	21.2	71	27.2	368	8.4	5000
1.5KE16P	1.5KE16CP	5	13.6	15.2	16	17.6	1	22.5	67	28.9	346	8.6	4700
1.5KE16A	1.5KE16CA	5	13.6	15.2	16	16.8	1	22.5	67	28.9	346	8.6	4700
P 1.5KE18P	P 1.5KE18CP	5	15.3	17.1	18	19.8	1	25.2	59.5	32.5	308	8.8	4300
P 1.5KE18A	P 1.5KE18CA	5	15.3	17.1	18	18.9	1	25.2	59.5	32.5	308	8.8	4300
P 1.5KE20P	P 1.5KE20CP	5	17.1	19	20	22	1	27.7	54	36.1	277	9.0	4000
P 1.5KE20A	1.5KE20CA	5	17.1	19	20	21	1	27.7	54	36.1	277	9.0	4000
1.5KE22P	1.5KE22CP	5	18.8	20.9	22	24.2	1	30.6	49	39.3	254	9.2	3700

P = Prefered device

TYPES		I_{RM} @ V_{RM}		V_{BR} @ I_R				V_{CL} @ I_{PP}		V_{CL} @ I_{PP}		αT	C
		max		min	nom	max		max		max		max	typ
						note2		10/1000µs		8/20µs		note3	note4
Unidirectional	Bidirectional	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
1.5KE22A	1.5KE22CA	5	18.8	20.9	22	23.1	1	30.6	49	39.3	254	9.2	3700
1.5KE24P	1.5KE24CP	5	20.5	22.8	24	26.4	1	33.2	45	42.8	234	9.4	3500
P 1.5KE24A	1.5KE24CA	5	20.5	22.8	24	25.2	1	33.2	45	42.8	234	9.4	3500
P 1.5KE27P	1.5KE27CP	5	23.1	25.7	27	29.7	1	37.5	40	48.3	207	9.6	3200
1.5KE27A	1.5KE27CA	5	23.1	25.7	27	28.4	1	37.5	40	48.3	207	9.6	3200
1.5KE30P	P 1.5KE30CP	5	25.6	28.5	30	33	1	41.5	36	53.5	187	9.7	2900
P 1.5KE30A	P 1.5KE30CA	5	25.6	28.5	30	31.5	1	41.5	36	53.5	187	9.7	2900
P 1.5KE33P	P 1.5KE33CP	5	28.2	31.4	33	36.3	1	45.7	33	59.0	169	9.8	2700
P 1.5KE33A	1.5KE33CA	5	28.2	31.4	33	34.7	1	45.7	33	59.0	169	9.8	2700
P 1.5KE36P	P 1.5KE36CP	5	30.8	34.2	36	39.6	1	49.9	30	64.3	156	9.9	2500
P 1.5KE36A	P 1.5KE36CA	5	30.8	34.2	36	37.8	1	49.9	30	64.3	156	9.9	2500
P 1.5KE39P	P 1.5KE39CP	5	33.3	37.1	39	42.9	1	53.9	28	69.7	143	10.0	2400
P 1.5KE39A	P 1.5KE39CA	5	33.3	37.1	39	41.0	1	53.9	28	69.7	143	10.0	2400
1.5KE43P	1.5KE43CP	5	36.8	40.9	43	47.3	1	59.3	25.3	76.8	130	10.1	2200
P 1.5KE43A	P 1.5KE43CA	5	36.8	40.9	43	45.2	1	59.3	25.3	76.8	130	10.1	2200
1.5KE47P	1.5KE47CP	5	40.2	44.7	47	51.7	1	64.8	23.2	84	119	10.1	2050
P 1.5KE47A	P 1.5KE47CA	5	40.2	44.7	47	49.4	1	64.8	23.2	84	119	10.1	2050
1.5KE51P	1.5KE51CP	5	43.6	48.5	51	56.1	1	70.1	21.4	91	110	10.2	1950
P 1.5KE51A	1.5KE51CA	5	43.6	48.5	51	53.6	1	70.1	21.4	91	110	10.2	1950
1.5KE56P	1.5KE56CP	5	47.8	53.2	56	61.6	1	77	19.5	100	100	10.3	1800
P 1.5KE56A	1.5KE56CA	5	47.8	53.2	56	58.8	1	77	19.5	100	100	10.3	1800
1.5KE62P	1.5KE62CP	5	53.0	58.9	62	68.2	1	85	17.7	111	90	10.4	1700
P 1.5KE62A	P 1.5KE62CA	5	53.0	58.9	62	65.1	1	85	17.7	111	90	10.4	1700
P 1.5KE68P	P 1.5KE68CP	5	58.1	64.6	68	74.8	1	92	16.3	121	83	10.4	1550
P 1.5KE68A	P 1.5KE68CA	5	58.1	64.6	68	71.4	1	92	16.3	121	83	10.4	1550
1.5KE75P	1.5KE75CP	5	64.1	71.3	75	82.5	1	103	14.6	134	75	10.5	1450
P 1.5KE75A	P 1.5KE75CA	5	64.1	71.3	75	78.8	1	103	14.6	134	75	10.5	1450
P 1.5KE82P	P 1.5KE82CP	5	70.1	77.9	82	90.2	1	113	13.3	146	69	10.5	1350
P 1.5KE82A	P 1.5KE82CA	5	70.1	77.9	82	86.1	1	113	13.3	146	69	10.5	1350
1.5KE91P	1.5KE91CP	5	77.8	86.5	91	100	1	125	12	162	62	10.6	1250
P 1.5KE91A	P 1.5KE91CA	5	77.8	86.5	91	95.5	1	125	12	162	62	10.6	1250
1.5KE100P	1.5KE100CP	5	85.5	95.0	100	110	1	137	11	178	56	10.6	1150
P 1.5KE100A	1.5KE100CA	5	85.5	95.0	100	105	1	137	11	178	56	10.6	1150
1.5KE110P	P 1.5KE110CP	5	94.0	105	110	121	1	152	9.9	195	51	10.7	1050
1.5KE110A	1.5KE110CA	5	94.0	105	110	116	1	152	9.9	195	51	10.7	1050
1.5KE120P	1.5KE120CP	5	102	114	120	132	1	165	9.1	212	47	10.7	1000
P 1.5KE120A	P 1.5KE120CA	5	102	114	120	126	1	165	9.1	212	47	10.7	1000
1.5KE130P	P 1.5KE130CP	5	111	124	130	143	1	179	8.4	230	43	10.7	950
P 1.5KE130A	P 1.5KE130CA	5	111	124	130	137	1	179	8.4	230	43	10.7	950
1.5KE150P	1.5KE150CP	5	128	143	150	165	1	207	7.2	265	38	10.8	850
P 1.5KE150A	P 1.5KE150CA	5	128	143	150	158	1	207	7.2	265	38	10.8	850
P 1.5KE160P	P 1.5KE160CP	5	136	152	160	176	1	219	6.8	282	35	10.8	800
P 1.5KE160A	P 1.5KE160CA	5	136	152	160	168	1	219	6.8	282	35	10.8	800
1.5KE170P	1.5KE170CP	5	145	161	170	187	1	234	6.4	301	33	10.8	750
P 1.5KE170A	1.5KE170CA	5	145	161	170	179	1	234	6.4	301	33	10.8	750
1.5KE180P	P 1.5KE180CP	5	154	171	180	198	1	246	6.1	317	31.5	10.8	725
P 1.5KE180A	P 1.5KE180CA	5	154	171	180	189	1	246	6.1	317	31.5	10.8	725
P 1.5KE200P	P 1.5KE200CP	5	171	190	200	220	1	274	5.5	353	28	10.8	675
P 1.5KE200A	P 1.5KE200CA	5	171	190	200	210	1	274	5.5	353	28	10.8	675
1.5KE220P	P 1.5KE220CP	5	188	209	220	242	1	328	4.6	388	26	10.8	625
P 1.5KE220A	P 1.5KE220CA	5	188	209	220	231	1	328	4.6	388	26	10.8	625
P 1.5KE250P	P 1.5KE250CP	5	213	237	250	275	1	344	5.0	442	23	11	560
P 1.5KE250A	P 1.5KE250CA	5	213	237	250	263	1	344	5.0	442	23	11	560
1.5KE280P	1.5KE280CP	5	239	266	280	308	1	384	5.0	494	20	11	520
1.5KE280A	1.5KE280CA	5	239	266	280	294	1	384	5.0	494	20	11	520

P = Prefered device

TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Unidirectional	Bidirectional	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
1.5KE300P	P 1.5KE300CP	5	256	285	300	330	1	414	5.0	529	19	11	500
P 1.5KE300A	1.5KE300CA	5	256	285	300	315	1	414	5.0	529	19	11	500
1.5KE320P	1.5KE320CP	5	273	304	320	352	1	438	4.5	564	18	11	460
P 1.5KE320A	1.5KE320CA	5	273	304	320	336	1	438	4.5	564	18	11	460
P 1.5KE350P	P 1.5KE350CP	5	299	332	350	385	1	482	4.0	618	16	11	430
1.5KE350A	1.5KE350CA	5	299	332	350	368	1	482	4.0	618	16	11	430
P 1.5KE400P	P 1.5KE400CP	5	342	380	400	440	1	548	4.0	706	14	11	390
1.5KE400A	1.5KE400CA	5	342	380	400	420	1	548	4.0	706	14	11	390
P 1.5KE440P	P 1.5KE440CP	5	376	418	440	484	1	603	3.5	776	13	11	360
1.5KE440A	1.5KE440CA	5	376	418	440	462	1	603	3.5	776	13	11	360

All parameters tested at 25 °C, except where indicated.

P = Prefered device

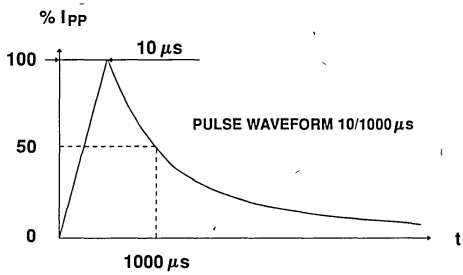
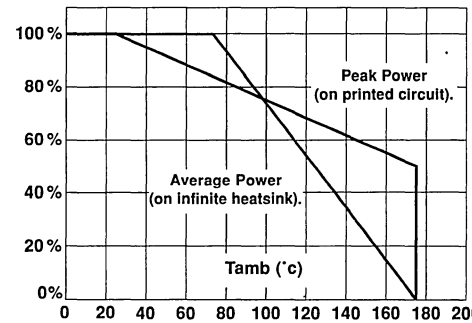


Figure 1: Power dissipation derating versus ambient temperature



Note 1 : For surges greater than the maximum values, the diode will present a short-circuit Anode - Cathode.

Note 2 : Pulse test: $T_P < 50$ ms.

Note 3 : $\Delta V_{BR} = \alpha T \cdot (Ta - 25) \cdot V_{BR(25°C)}$.

Note 4 : VR = 0 V, F = 1 MHz. For bidirectional types, capacitance value is divided by 2.

Figure 2 : Peak pulse power versus exponential pulse duration.

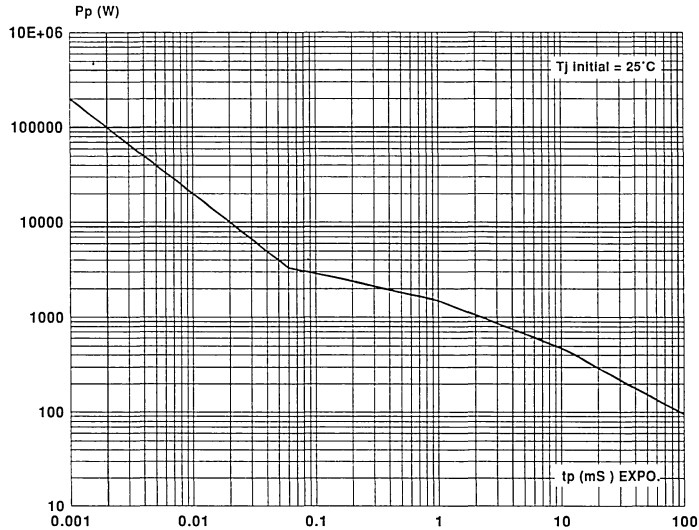
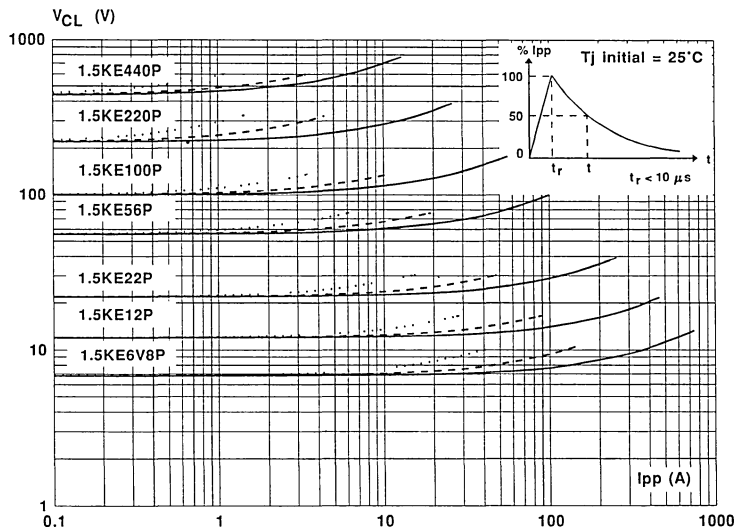


Figure 3 : Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs _____
t = 1 ms ----------
t =10 ms .....



Note : The curves of the figure 3 are specified for a junction temperature of 25 °C before surge.
The given results may be extrapolated for other junction temperatures by using the following formula :
$\Delta V_{(BR)} = \alpha T_{(V(BR))} \cdot [T_a - 25] \cdot V_{(BR)}$.
For intermediate voltages, extrapolate the given results.

Figure 4a : Capacitance versus reverse applied voltage for unidirectional types (typical values).

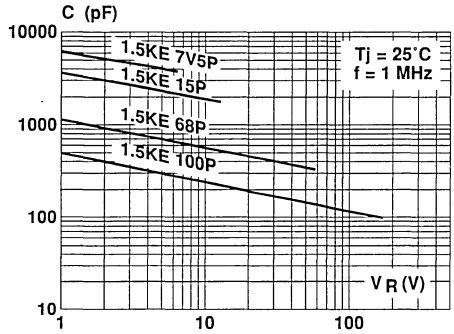


Figure 4b : Capacitance versus reverse applied voltage for bidirectional types (typical values)

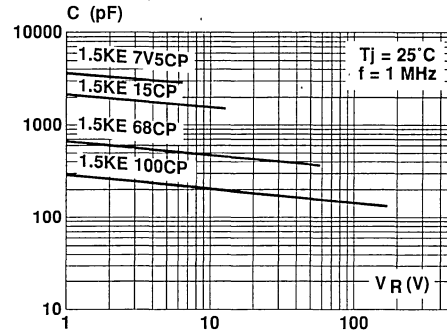


Figure 5 : Peak forward voltage drop versus peak forward current (typical values for unidirectional types).

Note : For units with $V_{BR} > 200$ V V_F is twice than shown.

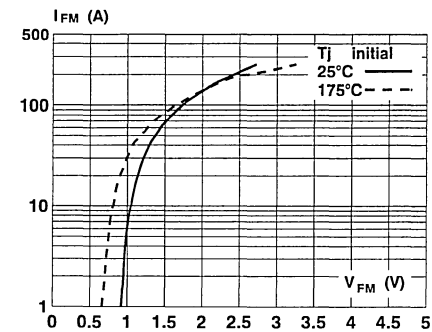
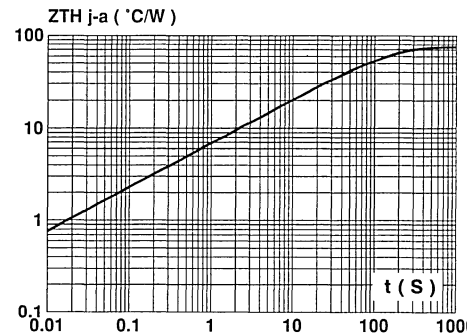


Figure 6 : Transient thermal impedance junction-ambient versus pulse duration. For a mounting on PC Board with L_{lead} = 10mm.



ORDER CODE

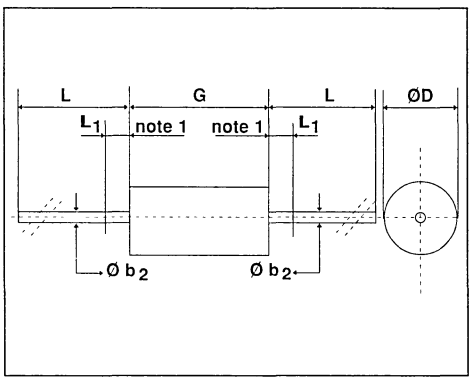
1.5 KE 100 C A RL

- 1.5 : 1500 W
- KE : BREAKDOWN VOLTAGE
- 100 : BREAKDOWN VOLTAGE
- C : BIDIRECTIONAL
- A : TOLERANCE : A = +/- 5%, P = -5%, +10%.
- RL : PACKAGING: = Ammopack, RL = Tape and reel.

MARKING : Logo, Date Code, Type Code, Cathode Band (for unidirectional types only).

PACKAGE MECHANICAL DATA

CB429



Ref.	Millimeters		Inches	
	min	max	min	max
Ø b_2	-	1.06	-	0.042
Ø D	-	5.1	-	0.20
G	-	9.8	-	0.386
L	26	-	1.024	-
L_1	-	1.27	-	0.050

note1:The diameter Ø b_2 is not controlled over zone L_1

Weight = 0.85 g.

Packaging : standard packaging is in tape and reel.

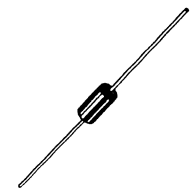
SGS-THOMSON MICROELECTRONICS

BZW04-5V8,B/376,B
BZW04P5V8,B/376,B

TRANSIL

FEATURES

- PEAK PULSE POWER= 400 W @ 1ms.
- STAND-OFF VOLTAGE RANGE : From 5V8 to 376 V.
- UNI AND BIDIRECTIONAL TYPES.
- LOW CLAMPING FACTOR.
- FAST RESPONSE TIME: Tclamping : 1ps (0 V to VBR).
- UL RECOGNIZED



F126
(Plastic)

DESCRIPTION

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous reponse to transients makes them particularly suited to protect voltage sensitive devices such as MOS Technology and low voltage supplied IC's.

MECHANICAL CHARACTERISTICS

- Body marked with : Logo, Date Code, Type Code and Cathode Band (for unidirectional types only).
- Tinned copper leads.
- High temperature soldering.

ABSOLUTE RATINGS (limiting values)

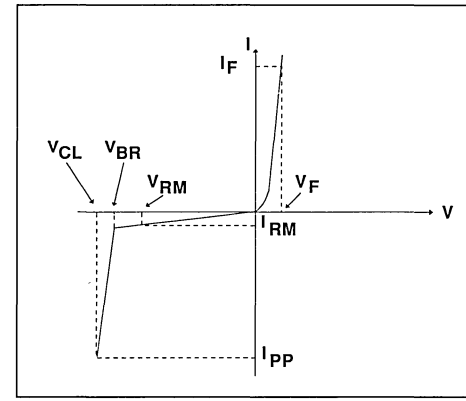
Symbol	Parameter		Value	Unit
P_p	Peak pulse power dissipation See note 1 and derating curve Fig 1.	Tamb = 25°C	400	W
P	Power dissipation on infinite heatsink See note 1 and derating curve Fig 1.	Tlead = 75°C	1.7	W
I_{FSM}	Non repetitive surge peak forward current For Unidirectional types	Tamb = 25°C t =10 ms	50	A
T_{stg} T_j	Storage and junction temperature range		- 65 to + 175 175	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		230	°C

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction-leads on infinite heatsink	60	°C/W
R_{th} (j-a)	Junction to ambiant. on printed circuit. L_{lead} = 10 mm	100	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage.
V_{BR}	Breakdown voltage.
V_{CL}	Clamping voltage.
I_{RM}	Leakage current @ VRM.
I_{PP}	Surge current.
αT	Voltage temperature coefficient.
V_F	Forward Voltage drop V_F < 3.5V @ I_F = 25 A.



TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Unidirectional	Bidirectional	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
P BZW04P5V8	P BZW04P5V8B	1000	5.8	6.45	6.8	7.48	10	10.5	38	13.4	174	5.7	3500
BZW04-5V8	BZW04-5V8B	1000	5.8	6.45	6.8	7.14	10	10.5	38	13.4	174	5.7	3500
BZW04P6V4	P BZW04P6V4B	500	6.4	7.13	7.5	8.25	10	11.3	35.4	14.5	160	6.1	3100
BZW04-6V4	BZW04-6V4B	500	6.4	7.13	7.5	7.88	10	11.3	35.4	14.5	160	6.1	3100
BZW04P7V0	BZW04P7V0B	200	7.02	7.79	8.2	9.02	10	12.1	33	15.5	148	6.5	2700
BZW04-7V0	BZW04-7V0B	200	7.02	7.79	8.2	8.61	10	12.1	33	15.5	148	6.5	2700
BZW04P7V8	BZW04P7V8B	50	7.78	8.65	9.1	10	1	13.4	30	17.1	134	6.8	2300
BZW04-7V8	BZW04-7V8B	50	7.78	8.65	9.1	9.55	1	13.4	30	17.1	134	6.8	2300
BZW04P8V5	BZW04P8V5B	10	8.55	9.5	10	11	1	14.5	27.6	18.6	124	7.3	2000
BZW04-8V5	BZW04-8V5B	10	8.55	9.5	10	10.5	1	14.5	27.6	18.6	124	7.3	2000
P BZW04P9V4	BZW04P9V4B	5	9.4	10.5	11	12.1	1	15.6	25.7	20.3	113	7.5	1750
BZW04-9V4	BZW04-9V4B	5	9.4	10.5	11	11.6	1	15.6	25.7	20.3	113	7.5	1750
P BZW04P10	P BZW04P10B	5	10.2	11.4	12	13.2	1	16.7	24	21.7	106	7.8	1550
BZW04-10	BZW04-10B	5	10.2	11.4	12	12.6	1	16.7	24	21.7	106	7.8	1550
P BZW04P11	P BZW04P11B	5	11.1	12.4	13	14.3	1	18.2	22	23.6	97	8.1	1450
BZW04-11	BZW04-11B	5	11.1	12.4	13	13.7	1	18.2	22	23.6	97	8.1	1450
P BZW04P13	P BZW04P13B	5	12.8	14.3	15	16.5	1	21.2	19	27.2	85	8.4	1200
P BZW04-13	P BZW04-13B	5	12.8	14.3	15	15.8	1	21.2	19	27.2	85	8.4	1200
P BZW04P14	BZW04P14B	5	13.6	15.2	16	17.6	1	22.5	17.8	28.9	80	8.6	1100
BZW04-14	BZW04-14B	5	13.6	15.2	16	16.8	1	22.5	17.8	28.9	80	8.6	1100
P BZW04P15	P BZW04P15B	5	15.3	17.1	18	19.8	1	25.2	16	32.5	71	8.8	975
P BZW04-15	P BZW04-15B	5	15.3	17.1	18	18.9	1	25.2	16	32.5	71	8.8	975
BZW04P17	BZW04P17B	5	17.1	19	20	22	1	27.7	14.5	36.1	64	9.0	850
BZW04-17	BZW04-17B	5	17.1	19	20	21	1	27.7	14.5	36.1	64	9.0	850
BZW04P19	P BZW04P19B	5	18.8	20.9	22	24.2	1	30.6	13	39.3	59	9.2	800

P = Prevered device

TYPES		I_{RM} @ V_{RM}		V_{BR} @ I_R				V_{CL} @ I_{PP}		V_{CL} @ I_{PP}		αT	C
		max		min	nom	max		max		max		max	typ
					note2			10/1000µs		8/20µs		note3	note4
Unidirectional	Bidirectional	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
BZW04-19	BZW04-19B	5	18.8	20.9	22	23.1	1	30.6	13	39.3	59	9.2	800
BZW04P20	P BZW04P20B	5	20.5	22.8	24	26.4	1	33.2	12	42.8	54	9.4	725
BZW04-20	BZW04-20B	5	20.5	22.8	24	25.2	1	33.2	12	42.8	54	9.4	725
BZW04P23	P BZW04P23B	5	23.1	25.7	27	29.7	1	37.5	10.7	48.3	48	9.6	625
BZW04-23	BZW04-23B	5	23.1	25.7	27	28.4	1	37.5	10.7	48.3	48	9.6	625
P BZW04P26	BZW04P26B	5	25.6	28.5	30	33	1	41.5	9.6	53.5	43	9.7	575
BZW04-26	BZW04-26B	5	25.6	28.5	30	31.5	1	41.5	9.6	53.5	43	9.7	575
P BZW04P28	P BZW04P28B	5	28.2	31.4	33	36.3	1	45.7	8.8	59.0	39	9.8	510
BZW04-28	BZW04-28B	5	28.2	31.4	33	34.7	1	45.7	8.8	59.0	39	9.8	510
BZW04P31	BZW04P31B	5	30.8	34.2	36	39.6	1	49.9	8	64.3	36	9.9	480
P BZW04-31	BZW04-31B	5	30.8	34.2	36	37.8	1	49.9	8	64.3	36	9.9	480
P BZW04P33	P BZW04P33B	5	33.3	37.1	39	42.9	1	53.9	7.4	69.7	33	10.0	450
P BZW04-33	BZW04-33B	5	33.3	37.1	39	41.0	1	53.9	7.4	69.7	33	10.0	450
BZW04P37	BZW04P37B	5	36.8	40.9	43	47.3	1	59.3	6.7	76.8	30	10.1	400
BZW04-37	P BZW04-37B	5	36.8	40.9	43	45.2	1	59.3	6.7	76.8	30	10.1	400
BZW04P40	BZW04P40B	5	40.2	44.7	47	51.7	1	64.8	6.2	84	27	10.1	370
BZW04-40	BZW04-40B	5	40.2	44.7	47	49.4	1	64.8	6.2	84	27	10.1	370
BZW04P44	BZW04P44B	5	43.6	48.5	51	56.1	1	70.1	5.7	91	25	10.2	350
BZW04-44	BZW04-44B	5	43.6	48.5	51	53.6	1	70.1	5.7	91	25	10.2	350
BZW04P48	P BZW04P48B	5	47.8	53.2	56	61.6	1	77	5.2	100	23	10.3	320
P BZW04-48	P BZW04-48B	5	47.8	53.2	56	58.8	1	77	5.2	100	23	10.3	320
BZW04P53	BZW04P53B	5	53.0	58.9	62	68.2	1	85	4.7	111	21	10.4	290
BZW04-53	BZW04-53B	5	53.0	58.9	62	65.1	1	85	4.7	111	21	10.4	290
P BZW04P58	P BZW04P58B	5	58.1	64.6	68	74.8	1	92	4.3	121	19	10.4	270
BZW04-58	BZW04-58B	5	58.1	64.6	68	71.4	1	92	4.3	121	19	10.4	270
BZW04P64	BZW04P64B	5	64.1	71.3	75	82.5	1	103	3.9	134	17	10.5	250
P BZW04-64	BZW04-64B	5	64.1	71.3	75	78.8	1	103	3.9	134	17	10.5	250
BZW04P70	BZW04P70B	5	70.1	77.9	82	90.2	1	113	3.5	146	16	10.5	230
BZW04-70	P BZW04-70B	5	70.1	77.9	82	86.1	1	113	3.5	146	16	10.5	230
BZW04P78	BZW04P78B	5	77.8	86.5	91	100	1	125	3.2	162	14	10.6	210
BZW04-78	BZW04-78B	5	77.8	86.5	91	95.5	1	125	3.2	162	14	10.6	210
P BZW04P85	P BZW04P85B	5	85.5	95.0	100	110	1	137	2.9	178	13	10.6	200
BZW04-85	BZW04-85B	5	85.5	95.0	100	105	1	137	2.9	178	13	10.6	200
BZW04P94	BZW04P94B	5	94.0	105	110	121	1	152	2.6	195	12	10.7	185
BZW04-94	BZW04-94B	5	94.0	105	110	116	1	152	2.6	195	12	10.7	185
BZW04P102	BZW04P102B	5	102	114	120	132	1	165	2.4	212	11	10.7	170
BZW04-102	BZW04-102B	5	102	114	120	126	1	165	2.4	212	11	10.7	170
BZW04P111	P BZW04P111B	5	111	124	130	143	1	179	2.2	230	10	10.7	165
BZW04-111	BZW04-111B	5	111	124	130	137	1	179	2.2	230	10	10.7	165
P BZW04P128	P BZW04P128B	5	128	143	150	165	1	207	2.0	265	9	10.8	145
BZW04-128	BZW04-128B	5	128	143	150	158	1	207	2.0	265	9	10.8	145
P BZW04P136	P BZW04P136B	5	136	152	160	176	1	219	1.8	282	8	10.8	140
P BZW04-136	P BZW04-136B	5	136	152	160	168	1	219	1.8	282	8	10.8	140
P BZW04P145	P BZW04P145B	5	145	161	170	187	1	234	1.7	301	7.5	10.8	135
BZW04-145	BZW04-145B	5	145	161	170	179	1	234	1.7	301	7.5	10.8	135
BZW04P154	BZW04P154B	5	154	171	180	198	1	246	1.6	317	7	10.8	125
BZW04-154	BZW04-154B	5	154	171	180	189	1	246	1.6	317	7	10.8	125
BZW04P171	BZW04P171B	5	171	190	200	220	1	274	1.5	353	6.5	10.8	120
BZW04-171	BZW04-171B	5	171	190	200	210	1	274	1.5	353	6.5	10.8	120
BZW04P188	P BZW04P188B	5	188	209	220	242	1	328	1.4	388	6	10.8	110
BZW04-188	BZW04-188B	5	188	209	220	231	1	328	1.4	388	6	10.8	110
BZW04P213	P BZW04P213B	5	213	237	250	275	1	344	1.5	442	5.2	11	100
BZW04-213	BZW04-213B	5	213	237	250	263	1	344	1.5	442	5.2	11	100
P BZW04P239	P BZW04P239B	5	239	266	280	308	1	384	1.5	494	4.6	11	95
BZW04-239	BZW04-239B	5	239	266	280	294	1	384	1.5	494	4.6	11	95

P = Prevered device

TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Unidirectional	**Bidirectional**	**µA**	**V**	**V**	**V**	**V**	**mA**	**V**	**A**	**V**	**A**	**10^{-4}/°C**	**(pF)**
BZW04P256	BZW04P256B	5	256	285	300	330	1	414	1.2	529	4.3	11	90
BZW04-256	BZW04-256B	5	256	285	300	315	1	414	1.2	529	4.3	11	90
BZW04P273	BZW04P273B	5	273	304	320	352	1	438	1.2	564	4	11	85
BZW04-273	BZW04-273B	5	273	304	320	336	1	438	1.2	564	4	11	85
BZW04P299	P BZW04P299B	5	299	332	350	385	1	482	0.9	618	3.7	11	80
P BZW04-299	P BZW04-299B	5	299	332	350	368	1	482	0.9	618	3.7	11	80
BZW04P342	P BZW04P342B	5	342	380	400	440	1	548	0.9	706	3.2	11	75
BZW04-342	P BZW04-342B	5	342	380	400	420	1	548	0.9	706	3.2	11	75
P BZW04P376	P BZW04P376B	5	376	418	440	484	1	603	0.8	776	3	11	70
BZW04-376	P BZW04-376B	5	376	418	440	462	1	603	0.8	776	3	11	70

All parameters tested at 25 °C, except where indicated.

P = Prefered device

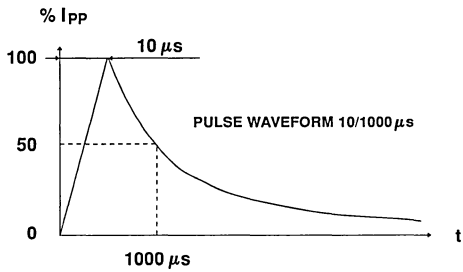
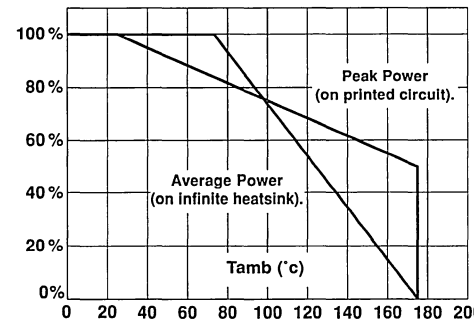


Figure 1: Power dissipation derating versus ambient temperature



Note 1 : For surges greater than the maximum values, the diode will present a short-circuit Anode - Cathode.

Note 2 : Pulse test: $T_P < 50$ ms.

Note 3 : $\Delta V_{BR} = \alpha T \cdot (Ta - 25) \cdot V_{BR(25°C)}$.

Note 4 : VR = 0 V, F = 1 MHz. For bidirectional types, capacitance value is divided by 2.

Figure 2 : Peak pulse power versus exponential pulse duration.

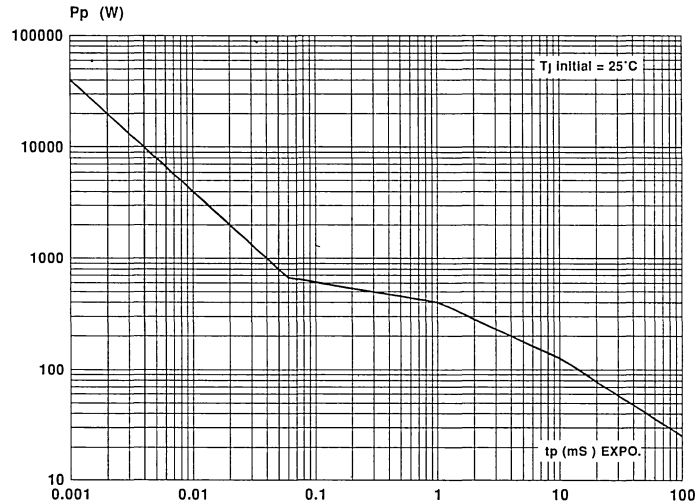
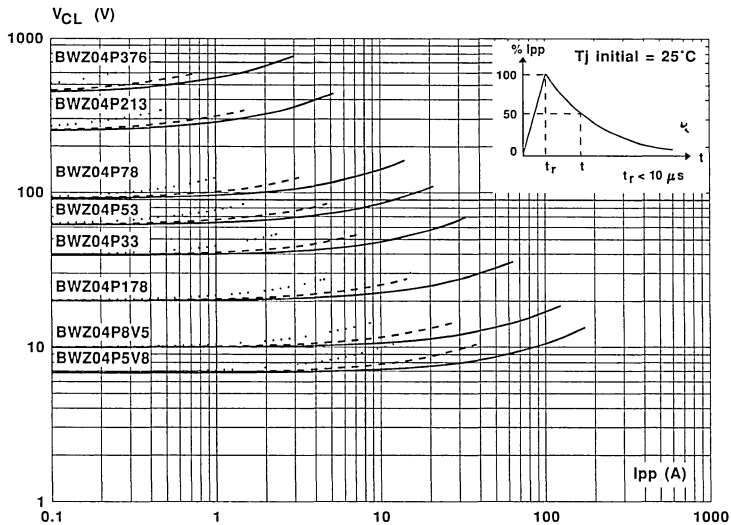


Figure 3 : Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs _____
t = 1 ms ----------
t =10 ms .....



Note : The curves of the figure 3 are specified for a junction temperature of 25 °C before surge.
The given results may be extrapolated for other junction temperatures by using the following formula :
$\Delta V_{(BR)} = \alpha T_{(V(BR))} * [T_a - 25] * V_{(BR)}$.
For intermediate voltages, extrapolate the given results.

Figure 4a : Capacitance versus reverse applied voltage for unidirectional types (typical values).

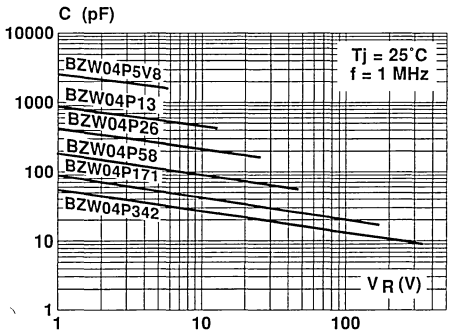


Figure 4b : Capacitance versus reverse applied voltage for bidirectional types (typical values)

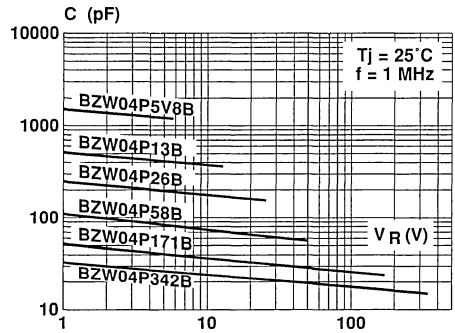


Figure 5 : Peak forward voltage drop versus peak forward current (typical values for unidirectional types).

Note : For units with V_{BR} > 200 V
V_F is twice than shown

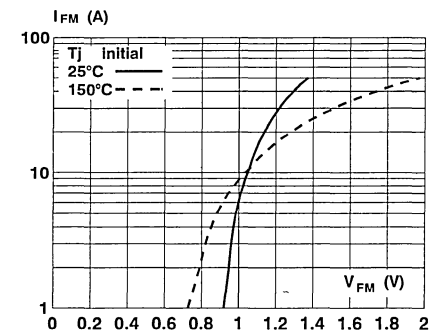
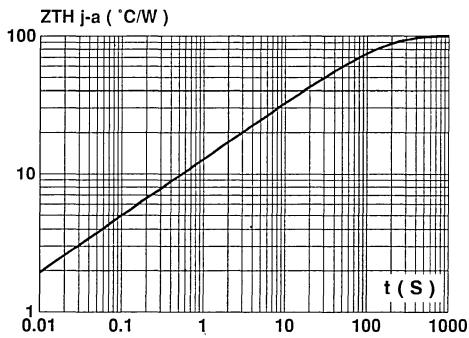


Figure 6 : Transient thermal impedance junction-ambient versus pulse duration. For a mounting on PC Board with L_{lead} = 10mm.



ORDER CODE

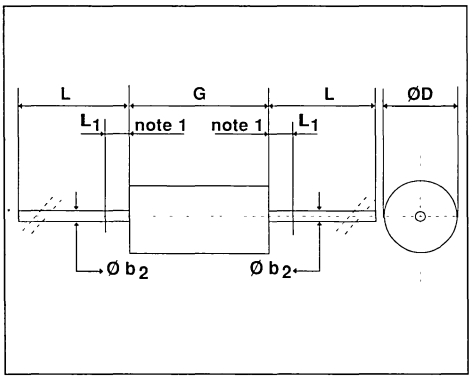
BZW 04 - 10 B RL

- 400 W
- TOLERANCE : - = +/- 5%, P = -5%, +10%.
- STAND-OFF VOLTAGE
- BIDIRECTIONAL
- PACKAGING: = Ammopack, RL = Tape and reel.

MARKING : Logo, Date Code, Type Code, Cathode Band (for unidirectional types only).

PACKAGE MECHANICAL DATA

F 126 (Plastic).



Ref	Millimeters		Inches	
	min	max	min	max
Ø b_2	0.76	0.86	0.029	0.034
Ø D	2.95	3.05	0.116	0.120
G	6.05	6.35	0.238	0.250
L	26	-	1.024	-
L_1	-	1.27	-	0.050

note1:The diameter Ø b_2 is not controlled over zone L_1

Weight = 0.4 g.

Packaging : standard packaging is in tape and reel.

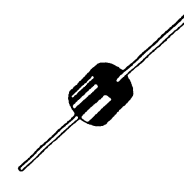
SGS-THOMSON MICROELECTRONICS

BZW50-10,B/180,B

TRANSIL

FEATURES

- PEAK PULSE POWER= 5000 W @ 1ms.
- STAND-OFF VOLTAGE RANGE : From 10V to 180 V.
- UNI AND BIDIRECTIONAL TYPES.
- LOW CLAMPING FACTOR.
- FAST RESPONSE TIME: Tclamping : 1ps (0 V to VBR).



AG
(Plastic)

DESCRIPTION

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous reponse to transients makes them particularly suited to protect voltage sensitive devices such as MOS Technology and low voltage supplied IC's.

MECHANICAL CHARACTERISTICS

- Body marked with : Logo, Date Code, Type Code and Cathode Band (for unidirectional types only).
- Tinned copper leads.
- High temperature soldering.

ABSOLUTE RATINGS (limiting values)

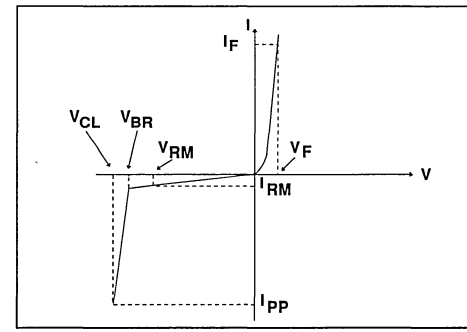
Symbol	Parameter		Value	Unit
P_p	Peak pulse power dissipation See note 1 and derating curve Fig 1.	Tamb = 25°C	5000	W
P	Power dissipation on infinite heatsink See note 1 and derating curve Fig 1.	Tlead = 75°C	6.5	W
I_{FSM}	Non repetitive surge peak forward current For Unidirectional types.	Tamb = 25°C t =10 ms	500	A
T_{stg} T_j	Storage and junction temperature range		- 65 to + 175 175	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		230	°C

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction-leads on infinite heatsink	15	°C/W
R_{th} (j-a)	Junction to ambient. on printed circuit. L_{lead} = 10 mm	65	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage.
V_{BR}	Breakdown voltage.
V_{CL}	Clamping voltage.
I_{RM}	Leakage current @ VRM.
I_{PP}	Surge current.
αT	Voltage temperature coefficient.



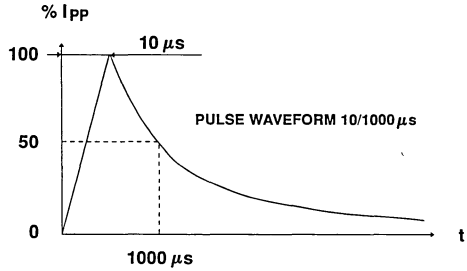
TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min	nom	max note2		V_{CL}@ I_{PP} max 10/1000µs		V_{CL}@ I_{PP} max 8/20µs		αT max note3	C typ note4
Unidirectional	**Bidirectional**	**µA**	**V**	**V**	**V**	**V**	**mA**	**V**	**A**	**V**	**A**	**10^{-4}/°C**	**(pF)**
BZW50-10	BZW50-10B	5	10	11.1	12.4	13.6	1	18.8	266	23.4	2564	7.8	24000
BZW50-12	BZW50-12B	5	12	13.3	14.8	16.3	1	22	227	28	2143	8.4	18500
BZW50-15	BZW50-15B	5	15	16.6	18.5	20.4	1	26.9	186	35	1714	8.8	13500
BZW50-18	BZW50-18B	5	18	20	22.2	24.4	1	32.2	155	41.5	1446	9.2	11500
BZW50-22	BZW50-22B	5	22	24.4	27.1	29.8	1	39.4	127	51	1177	9.6	8500
BZW50-27	BZW50-27B	5	27	30	33.3	36.6	1	48.3	103	62	968	9.8	7000
BZW50-33	BZW50-33B	5	33	36.6	40.7	44.7	1	59	85	76	789	1.0	5750
BZW50-39	BZW50-39B	5	39	43.3	48.1	53	1	69.4	72	90	667	10.1	4800
BZW50-47	BZW50-47B	5	47	52	57.8	63.6	1	83.2	60.1	108	556	10.3	4100
BZW50-56	BZW50-56B	5	56	62.2	69.1	76	1	99.6	50	129	465	10.4	3400
BZW50-68	BZW50-68B	5	68	75.6	84	92.4	1	121	41	157	382	10.5	3000
BZW50-82	BZW50-82B	5	82	91	101.2	111	1	145	34	189	317	10.6	2600
BZW50-100	BZW50-100B	5	100	111	123.5	136	1	179	28	228	263	10.7	2300
BZW50-120	BZW50-120B	5	120	133	148.1	163	1	215	23	274	219	10.8	1900
BZW50-150	BZW50-150B	5	150	166	185.2	204	1	269	19	343	175	10.8	1700
BZW50-180	BZW50-180B	5	180	200	222	244	1	322	16	410	146	10.8	1500

All parameters tested at 25 °C, except where indicated.

Note 2 : Pulse test: $T_P < 50$ ms.

Note 3 : $\Delta V_{BR} = \alpha T \cdot (Ta - 25) \cdot V_{BR(25°C)}$.

Note 4 : VR = 0 V, F = 1 MHz. For bidirectional types, capacitance value is divided by 2.



Note 1 : For surges greater than the maximum values, the diode will present a short-circuit Anode - Cathode.

Figure 1: Power dissipation derating versus ambient temperature

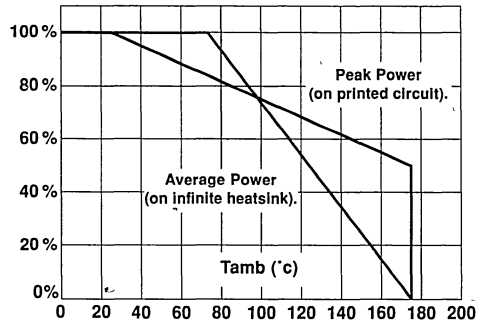


Figure 2 : Peak pulse power versus exponential pulse duration.

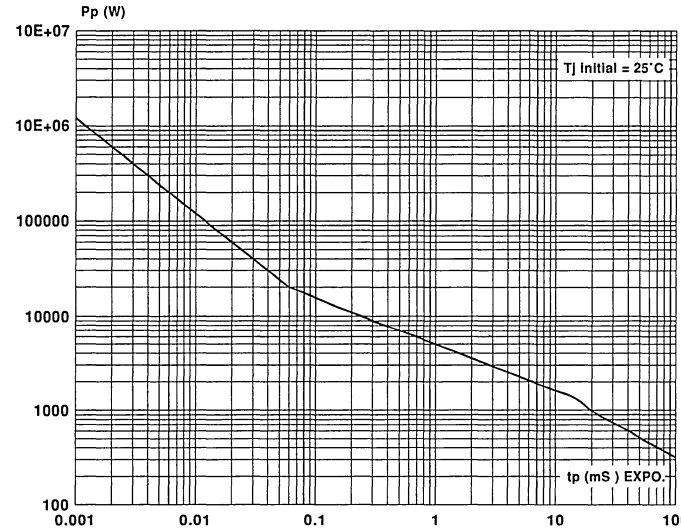
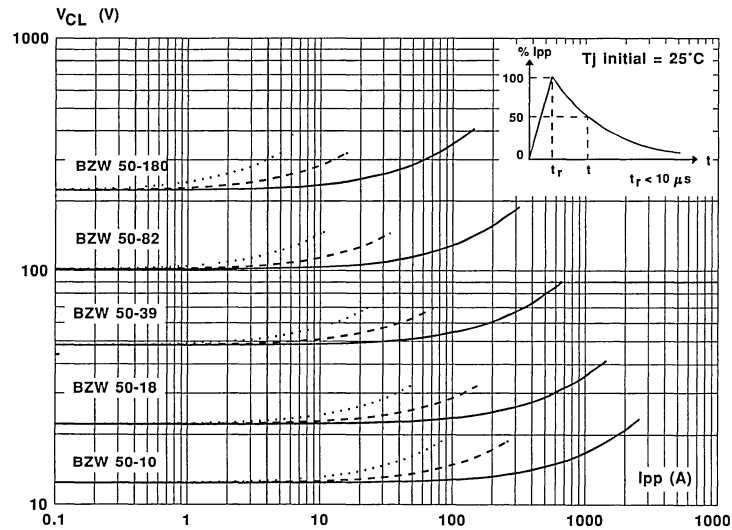


Figure 3 : Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs _____
t = 1 ms ----------
t =10 ms .....



Note : The curves of the figure 3 are specified for a junction temperature of 25 °C before surge.
The given results may be extrapolated for other junction temperatures by using the following formula :
$\Delta V_{(BR)} = \alpha T_{(V(BR))} * [T_a - 25] * V_{(BR)}$.
For intermediate voltages, extrapolate the given results.

Figure 4a : Capacitance versus reverse applied voltage for unidirectional types (typical values).

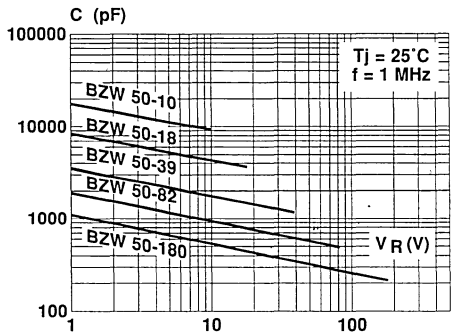


Figure 4b : Capacitance versus reverse applied voltage for bidirectional types (typical values)

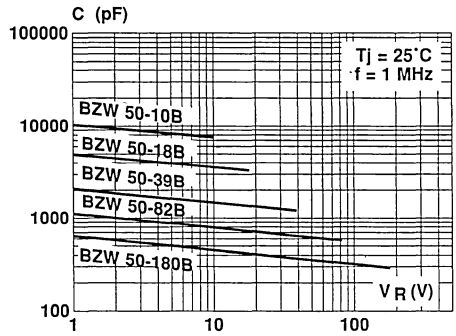


Figure 5 : Peak forward voltage drop versus peak forward current (typical values for unidirectional types).

Note : For units with V_{BR} > 200 V
V_F is twice than shown.

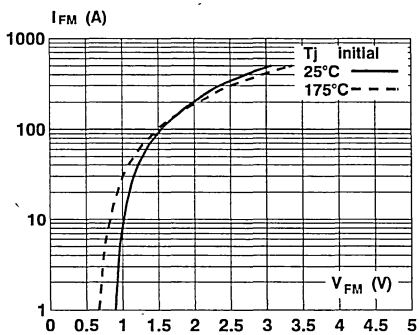
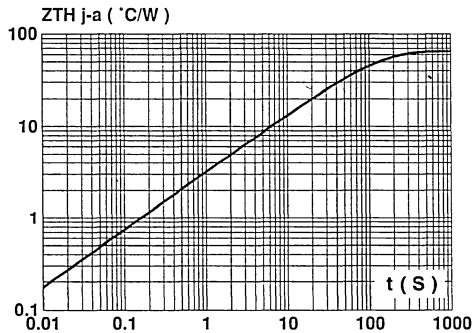
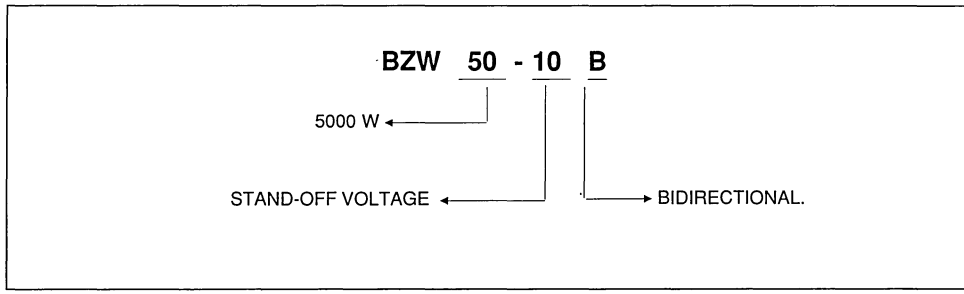


Figure 6 : Transient thermal impedance junction-ambient versus pulse duration. For a mounting on PC Board with L_{lead} = 10mm.



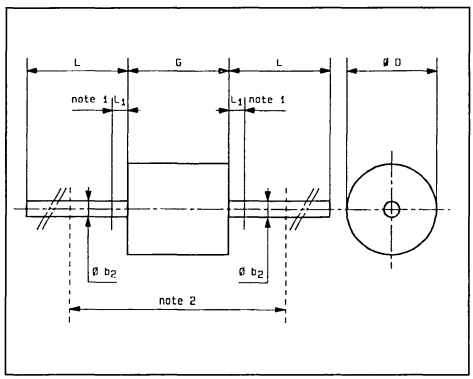
ORDER CODE



MARKING : Logo, Date Code, Type Code, Cathode Band (for unidirectional types only).

PACKAGE MECHANICAL DATA

AG plastic.



Ref	Millimeters		Inches	
	min	max	min	max
Ø b_2	1.35	1.45	0.053	0.057
Ø D	-	8	-	0.315
G	-	9.8	-	0.354
L	20	-	0.787	-
L_1	-	1.27	-	0.050

note 1 : The lead diameter Ø b_2 is not controlled over zone L_1
note 2 : 20mm minimum between bendings

Weight = 1.6 g.

Packaging : standard packaging is in bulk.

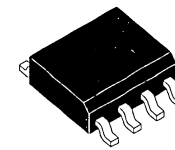
SGS-THOMSON MICROELECTRONICS

DA108S1

DIODE ARRAY

FEATURES

- ARRAY OF EIGHT DIODES
- IDEAL FOR CLAMPING SIGNALS TO SUPPLY RAILS
- SUITABLE FOR ISDN PROTECTION APPLICATIONS
- SURFACE-MOUNT SO8 PACKAGE



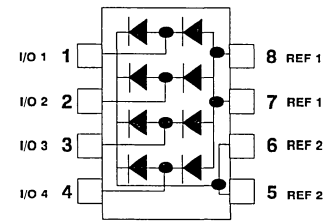
SO8
(plastic)

DESCRIPTION

Array of diodes configured to clamp four signals to a fixed reference so as to prevent damage caused by overvoltages. The reference can be either the supply rails or a Transil™ clamping device.

The diode array can be used for protecting the low-voltage side of an ISDN S interface. Other applications include microcontroller input port protection and signal conditioning.

PINOUT



ABSOLUTE MAXIMUM RATINGS ($0°C \leq T_{amb} \leq 70°C$)

Symbol	Parameter		Value	Unit
V_{RRM}	Repetitive peak reverse voltage (for one single diode)		18	V
I_{PP}	Repetitive peak forward current *	8/20 µs	12	A
P_{tot}	Power dissipation	Tamb = 25°C	0.73	W
Tstg Tj	Storage temperature range Maximum operating junction temperature		- 55 to + 150 150	°C °C

(* The surge is repeated after the device returns to its initial conditions)

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
Rth (j-l)	Junction - Leads thermal resistance	60	°C/W
Rth (j-a)	Junction - Ambient thermal resistance	170	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter		Min.	Max.	Unit
V_{FP}	Peak voltage	I_{PP} = 12A, 8/20 µs		9	V
V_F	Formard voltage	I_F = 50 mA		1.2	V
I_R	Reverse leakage current	V_R = 15V		2	µA
C	Typical input capacitance	(see fig.1)			

Fig.1 : I/O pin capacitance

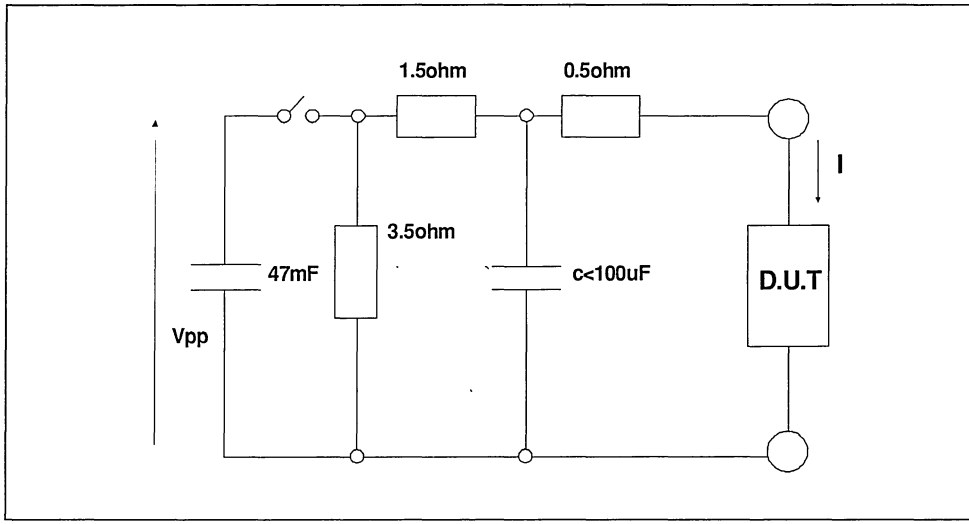
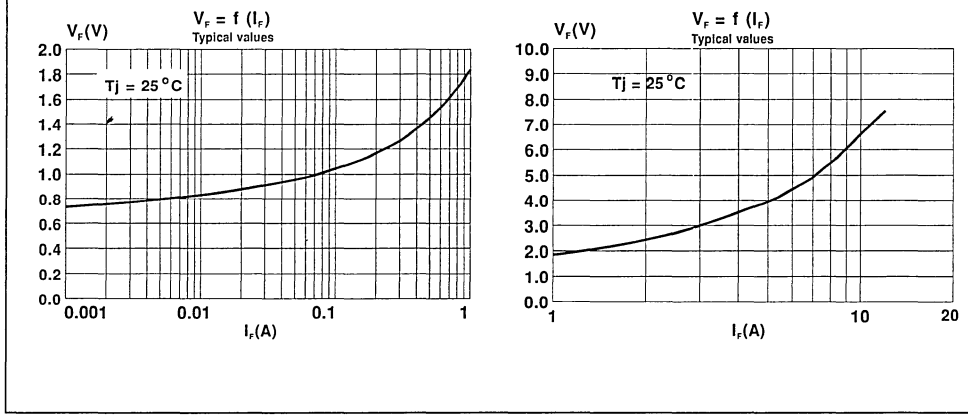
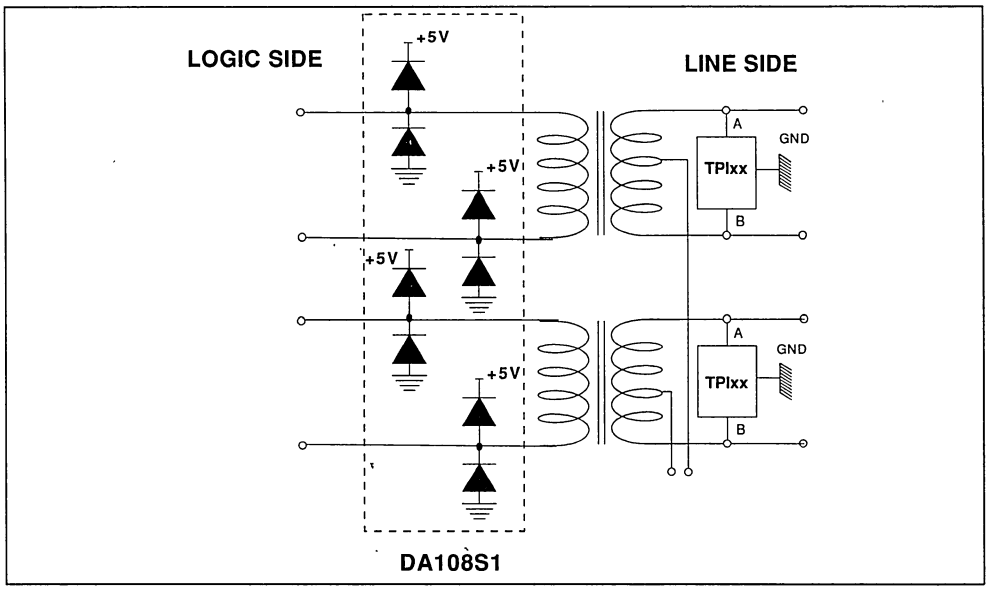


Fig.2 : Typical peak forward voltage characteristics (8/20µs pulse)

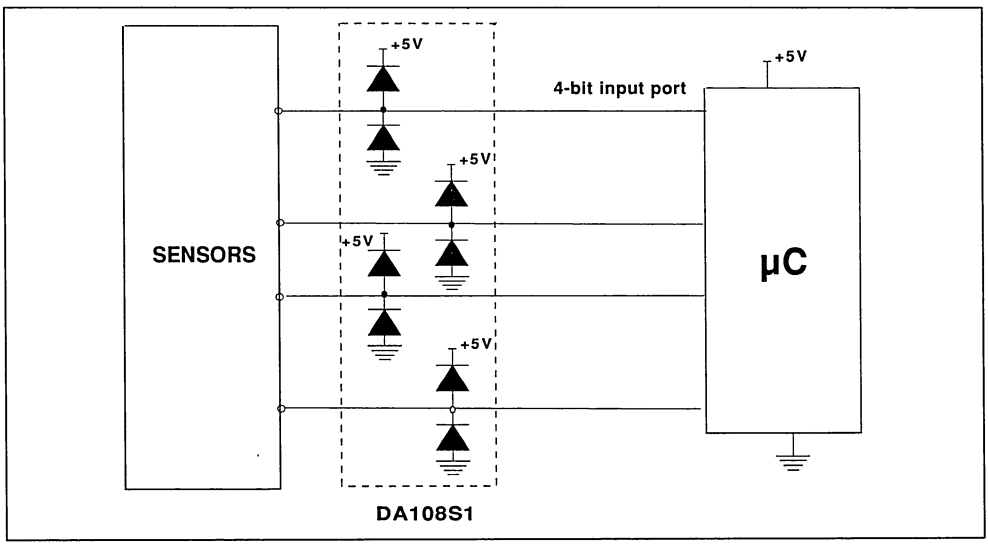


APPLICATION 1 : ISDN Interface Protection



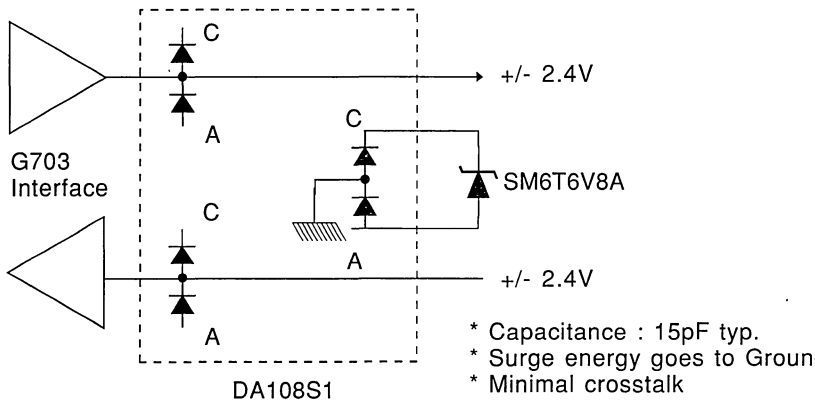
Residual lightning surges at transformer secondary are suppressed by DA108S1.

APPLICATION 2 : Microcontroller Input Signal Conditioning

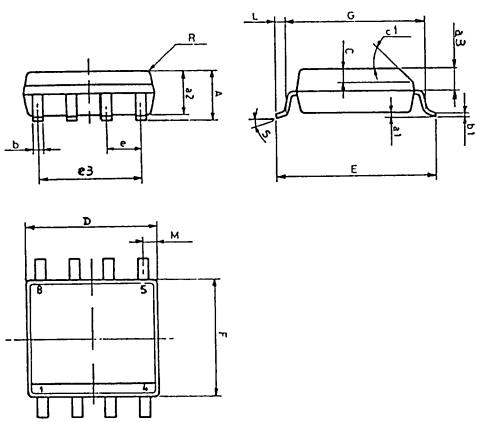


Sensor output voltage is clamped to within microcontroller supply range.

APPLICATION 3 : High-speed transmission protection



PACKAGE MECHANICAL DATA (in millimeters)
SO8 (plastic)



REF.	DIMENSIONS					
	Millimetres			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max)					

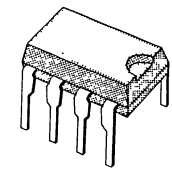
Packaging : Products supplied in antistatic tubes.

MARKING : Logo, Data Code, DA108S

PROGRAMMABLE TRANSIENT VOLTAGE SUPPRESSOR AND CURRENT LIMITER

FEATURES

- UNIDIRECTIONAL FUNCTION
- PROGRAMMABLE BREAKDOWN VOLTAGE UP TO 265 V
- PROGRAMMABLE CURRENT LIMITATION FROM 50 mA TO 550 mA
- HIGH SURGE CURRENT CAPABILITY
  I_{PP} = 100A 10/1000 µs



DIL 8
(Plastic)

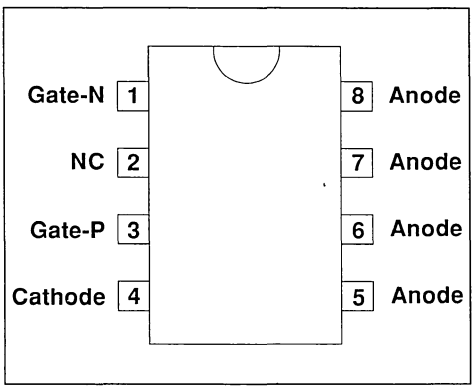
DESCRIPTION

Dedicated to sensitive telecom equipment protection, this device can provide both voltage protection and current limitation with a very tight tolerance.
Its high surge current capability makes the L3100B a reliable protection device for very exposed equipment, or when series resistors are very low.
The breakdown voltage can be easily programmed by using an external zener diode.
A multiple protection mode can also be performed when using several zener diodes, providing each line interface with an optimized protection level.
The current limiting function is achieved with the use of a resistor between the gate and the cathode. The value of the resistor will determine the level of the desired current.

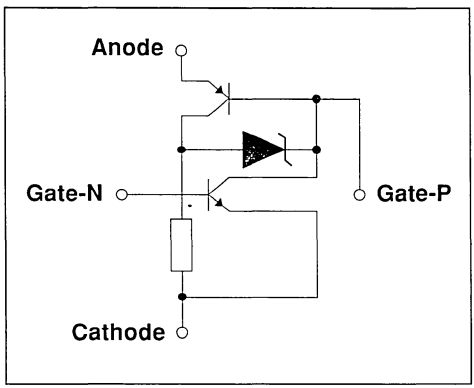
IN ACCORDANCE WITH FOLLOWING STANDARDS :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

CONNECTION DIAGRAM

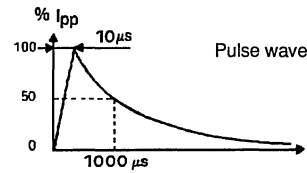


SCHEMATIC DIAGRAM



ABSOLUTE RATINGS (limiting values) (- 40°C ≤ T_{amb} ≤ +85°C)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current	10/1000 µs 8/20 µs	100 250	A
I_{TSM}	Non repetitive surge peak on-state current	tp = 10 ms	50	A
di/dt	Critical rate of rise of on-state current	Non repetitive	100	A/µs
dv/dt	Critical rate of rise of off-state voltage	67% V_{BR}	5	KV/µs
T_{stg} T_j	Storage and operating junction temperature range		- 40 to + 150 + 150	°C °C



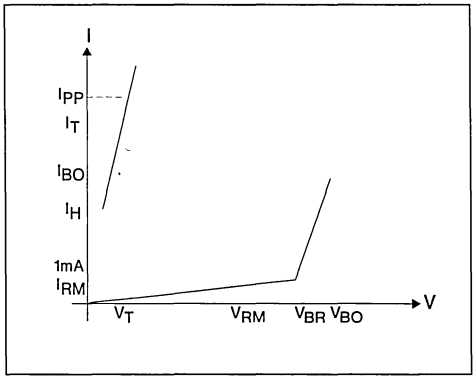
Pulse waveform 10/1000µs

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
R_{th} (j-a)	Junction-to-ambient	80	°C/W

ELECTRICAL CHARACTERISTICS.

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{BO}	Breakover voltage
I_H	Holding current
V_T	On-state voltage @ I_T
I_{BO}	Breakover current
I_{PP}	Peak pulse current
V_G	Gate voltage
I_G	Firing gate current



OPERATION WITHOUT GATE.

Type	I_{RM} @ V_{RM} max		V_{BR} @ I_R min		V_{BO} max	@ min note 1	I_{BO} max	I_H min note 1	V_T max note 2	C max note 3
	µA	V	V	mA	V	mA	mA	mA	V	pF
L3100B	6 40	60 250	265	1	350	200	500	280	2	100
L3100B1	6 40	60 250	255	1	350	200	500	210	2	100

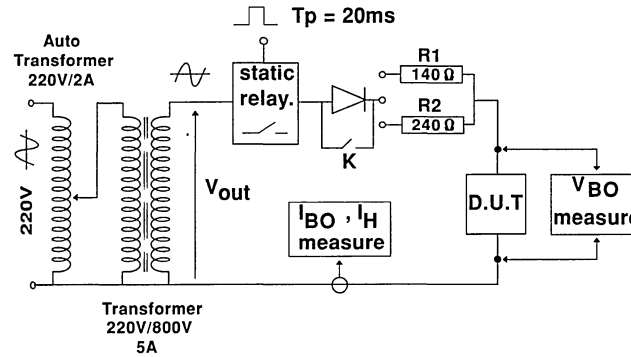
OPERATION WITH GATES.

Type	V_{GN} @ I_{GN} = 200 mA min	max	IGN @ V_{AC} = 100V min	max	V_{RGN} @ I_G = 1mA min	I_{GP} @ V_{AC} = 100V max
	V	V	mA	mA	V	mA
L3100B/B1	0.6	1.8	30	200	0.7	150

All parameters tested at 25°C, except where indicated otherwise.

Note 1 : See the reference test circuit for I_H, I_{BO} and V_{BO} parameters.
Note 2 : Square pulse T_P= 500µs - I_T = 1A.
Note 3 : V_R = 5 V, f = 1MHz.

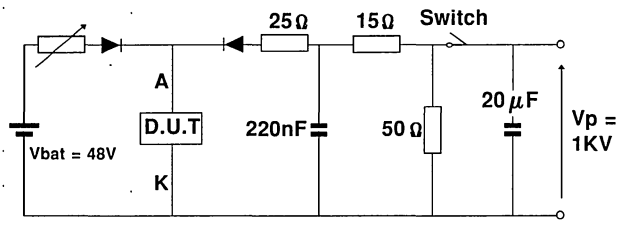
REFERENCE TEST CIRCUIT FOR I_H, I_{BO} and V_{BO} parameters :



TEST PROCEDURE :

- Pulse Test duration (Tp = 20ms):
  - For Bidirectional devices = Switch K is closed
  - For Unidirectional devices = Switch K is open.
- V_{OUT} Selection
  - Device with $V_{BR} \leq 150$ Volt
    - $V_{OUT} = 250\ V_{RMS}$, $R_1 = 140\ \Omega$.
  - Device with $V_{BR} \geq 150$ Volt
    - $V_{OUT} = 480\ V_{RMS}$, $R_2 = 240\ \Omega$.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT = GO - NOGO TEST.



Surge Generator
10/700 µsec
Vp =1KV / Ipp = 25A

This is a GO-NOGO Test which allows to confirm the holding current (I_H) level in a functional test circuit. This test can be performed if the reference test circuit can't be implemented.

TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.
2) Fire the D.U.T with a surge Current : Ipp = 25A , 10/700 µs.
3) The D.U.T will come back to the OFF-State within a duration of 50 ms max.

Figure 1 : Non-repetitive surge peak on state current versus number of cycles. (with sinusoïdal pulse: F = 50 Hz).

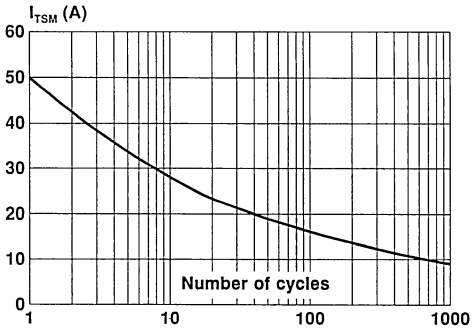


Figure 2 : Relative variation of holding current versus junction temperature.

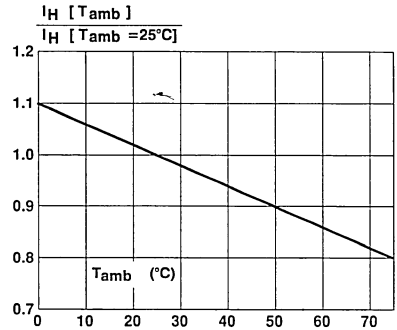


Figure 3 : Relative variation of breakdown voltage versus ambient temperature.

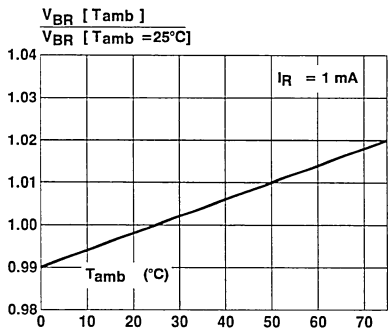
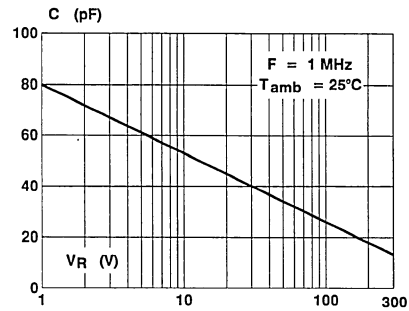


Figure 4 : Junction capacitance versus reverse applied voltage.



APPLICATION CIRCUIT

Overvoltage Protection and Current limitation

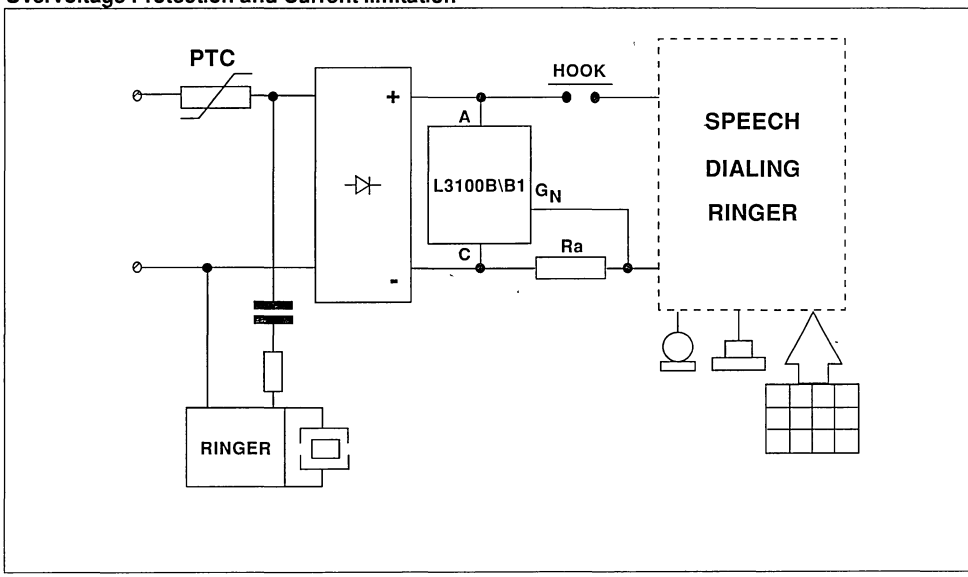
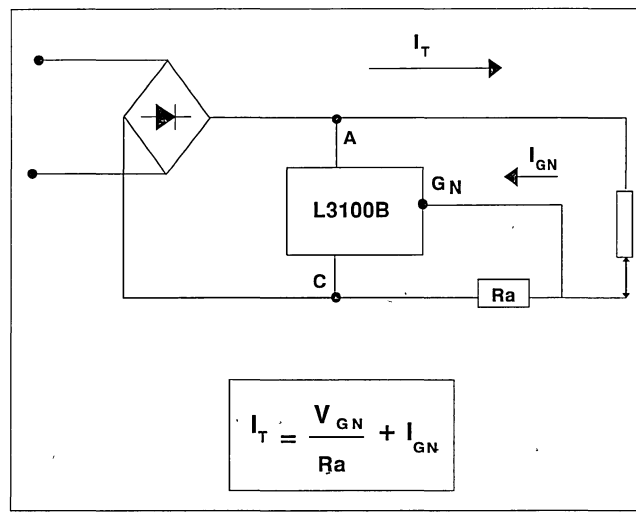


Table below gives the tolerance of the limited current I_T for each standardized resistor value. The formula (1) has been used with V_{GN} values specified at the typical gate current level I_{GN}.

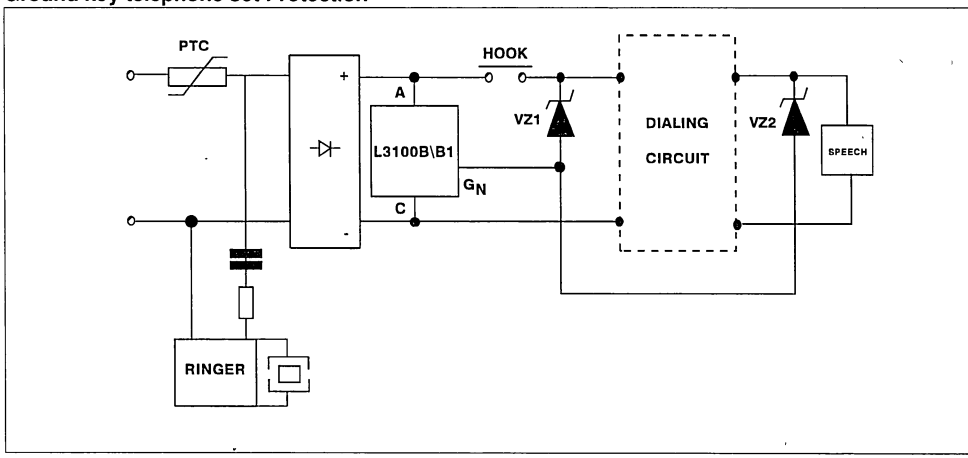
CURRENT TOLERANCE		
R Ω (± 5%)	I_T mA min	I_T mA max
3.00	268	533
3.30	246	503
3.60	228	478
3.90	213	456
4.30	196	433
4.70	181	413
5.10	170	396
5.60	158	379
6.20	145	361
6.80	135	347
7.50	152	333
8.20	117	322
9.10	108	310
10.10	101	299
11.00	95	291
12.00	90	283
13.00	85	277
15.00	78	266
16.00	75	263
18.00	70	256
20.00	66	250
22.00	62	245
24.00	60	242
27.00	56	237
30.00	54	233



$$I_T = \frac{V_{GN}}{Ra} + I_{GN}$$

V_{GN} @ I_{GN}		
Min	Max	Typ.
V	V	mA
0.75	0.95	100

Ground key telephone set Protection



PROTECTION MODES :

OFF HOOK = Ringer circuit protection is ensured with breakdown voltage at 265 V.

ON HOOK = In dialing mode and in conversation mode, the breakdown voltage of L3100B can be adapted to different levels with two zener diodes.

ORDER CODE

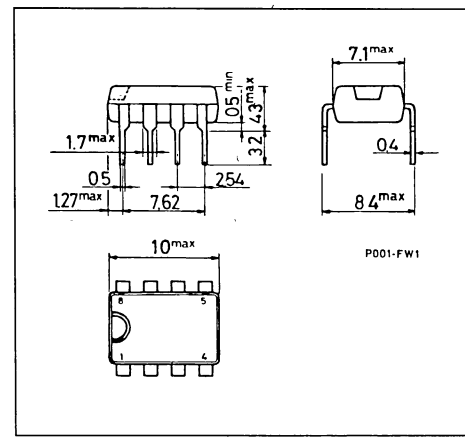
L3100 B 1

VERSION.
= VBR = 265 V
1 = VBR = 255 V

MARKING : Logo, Date Code,part Number.

PACKAGING : Products supplied in antistatic tubes.

PACKAGE MECHANICAL DATA (in millimeters)
DIL 8 Plastic



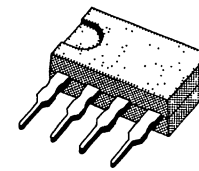
SGS-THOMSON MICROELECTRONICS

L3121B

PROGRAMMABLE TRANSIENT VOLTAGE SUPPRESSOR

FEATURES

- BIDIRECTIONAL FUNCTION WITH VOLTAGE PROGRAMMABILITY IN BOTH POSITIVE AND NEGATIVE POLARITIES.
- PROGRAMMABLE BREAKDOWN VOLTAGE UP TO 100 V.
- HOLDING CURRENT = 150 mA min.
- HIGH SURGE CURRENT CAPABILITY.
  I_{PP} = 100A , 10/1000 µs



SIP 4
(Plastic)

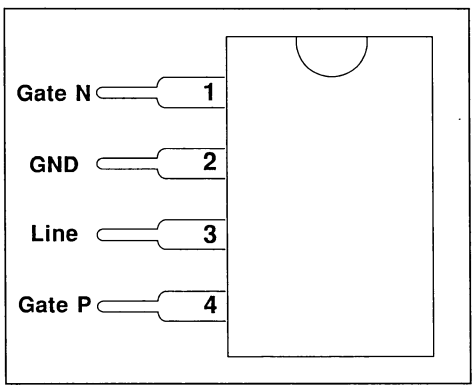
DESCRIPTION

This device has been especially designed to protect a subscriber line card interface (SLIC) with a integrated ring generator.
Used with the recommended application circuit, each line (TIP and RING) is protected against positive and negative surges. In the positive polarity, the breakdown voltage is referenced to the + VB , and in the negative polarity, the breakdown voltage is referenced to the -Vbat .
Its high surge current capability makes the L3121B a reliable protection device for very exposed equipment, or when series resistors are very low.

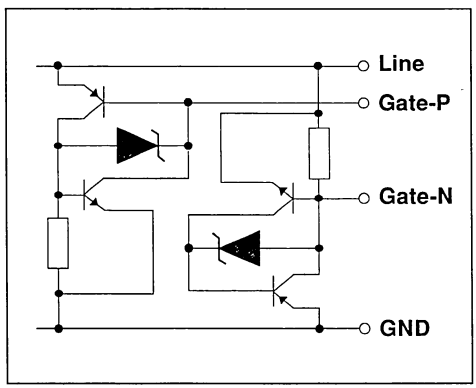
IN ACCORDANCE WITH FOLLOWING STANDARDS :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

CONNECTION DIAGRAM

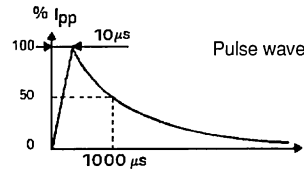


SCHEMATIC DIAGRAM



ABSOLUTE RATINGS (limiting values) (- 40°C ≤ T_{amb} ≤ +85°C)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current	10/1000 µs 8/20 µs	100 250	A
I_{TSM}	Non repetitive surge peak on-state current	tp = 10 ms	50	A
di/dt	Critical rate of rise of on-state current	Non repetitive	100	A/µs
V_{MLG} V_{MGL}	Maximum voltage LINE/GND. Maximum voltage GATE/LINE.		100 80	V V
T_{stg} T_j	Storage and operating junction temperature range		- 40 to + 150 150	°C °C



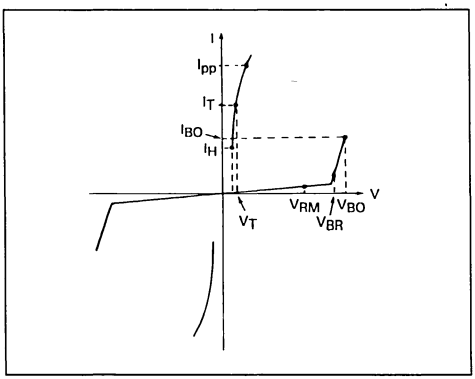
Pulse waveform 10/1000µs

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
R_{th} (j-a)	Junction-to-ambient	80	°C/W

ELECTRICAL CHARACTERISTICS.

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{BO}	Breakover voltage
I_H	Holding current
V_T	On-state voltage @ I_T
I_{BO}	Breakover current
I_{PP}	Peak pulse current
V_G	Gate voltage
I_G	Firing gate current



OPERATION WITHOUT GATE.

Type	I_{RM} @ V_{RM} max		V_{BR} @ I_R min		V_{BO} max	@ Typ note 1	I_{BO} max	I_H min note 1	V_T max note 2	C max note 3
	µA	V	V	mA	V	mA	mA	mA	V	pF
L3121B	5 8	60 90	100	1	180	200	500	150	2	200

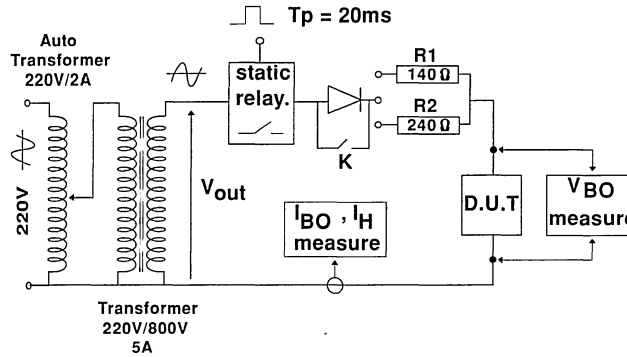
OPERATION WITH GATES.

Type	V_{GN} @ I_{GN} = 200mA		I_{GN} @ V_{AC} = 60V		I_{GP} @ V_{AC} = 60V
	min	max	min	max	max
	V	V	mA	mA	mA
L3121B	0.6	1.8	80	200	180

All parameters tested at 25°C, except where indicated.

Note 1 : See the reference test circuit for I_H, I_{BO} and V_{BO} parameters.
Note 2 : Square pulse T_P= 500µs - I_T = 1A.
Note 3 : V_R = 5 V, F = 1MHz.

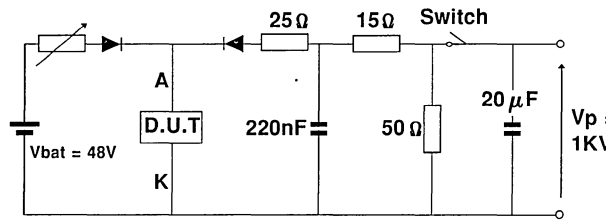
REFERENCE TEST CIRCUIT FOR I_H, I_{BO} and V_{BO} parameters :



TEST PROCEDURE :

- Pulse Test duration (Tp = 20ms):
  - For Bidirectional devices = Switch K is closed
  - For Unidirectional devices = Switch K is open.
- V_{OUT} Selection
  - Device with $V_{BR} \leq 150$ Volt
    - $V_{OUT} = 250\ V_{RMS}$, $R_1 = 140\ \Omega$.
  - Device with $V_{BR} \geq 150$ Volt
    - $V_{OUT} = 480\ V_{RMS}$, $R_2 = 240\ \Omega$.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT = GO - NOGO TEST.



Surge Generator
10/700 μsec
Vp =1KV / Ipp = 25A

This is a GO-NOGO Test which allows to confirm the holding current (I_H) level in a functional test circuit. This test can be performed if the reference test circuit can't be implemented.

TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.
2) Fire the D.U.T with a surge Current : Ipp = 25A , 10/700 μs.
3) The D.U.T will come back to the OFF-State within a duration of 50 ms max.

Figure 1 : Non-repetitive surge peak on state current versus number of cycles. (with sinusoïdal pluse: F = 50 Hz).

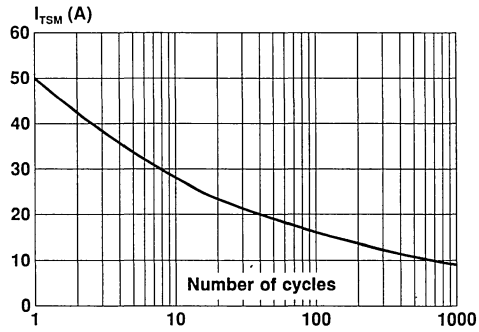


Figure 2 : Relative variation of holding current versus junction temperature.

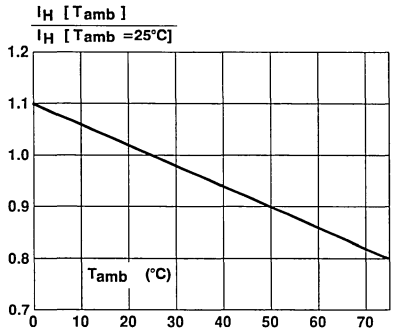


Figure 3 : Relative variation of breakdown voltage versus ambient temperature.

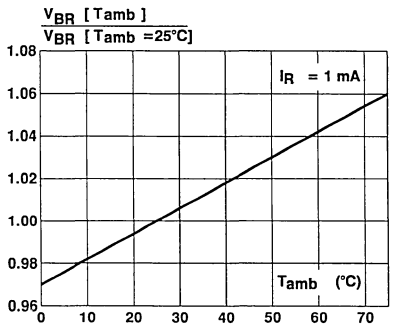
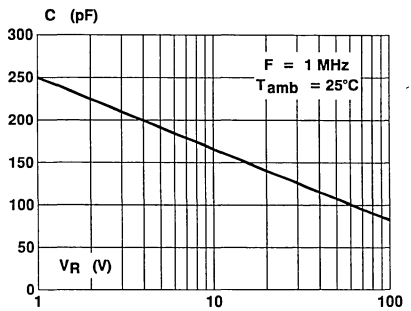
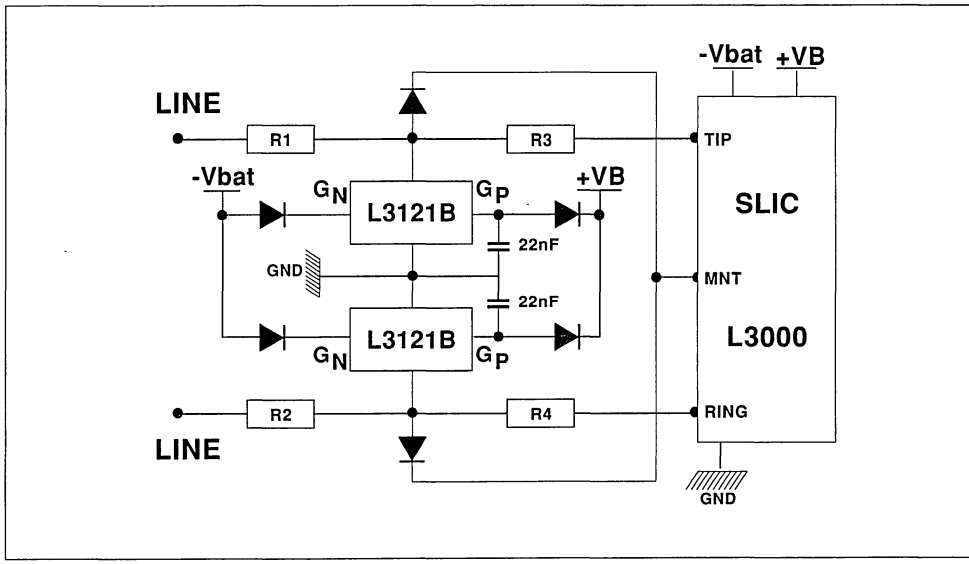


Figure 4 : Junction capacitance versus reverse applied voltage.



APPLICATION CIRCUIT

Typical Slic Protection Concept.

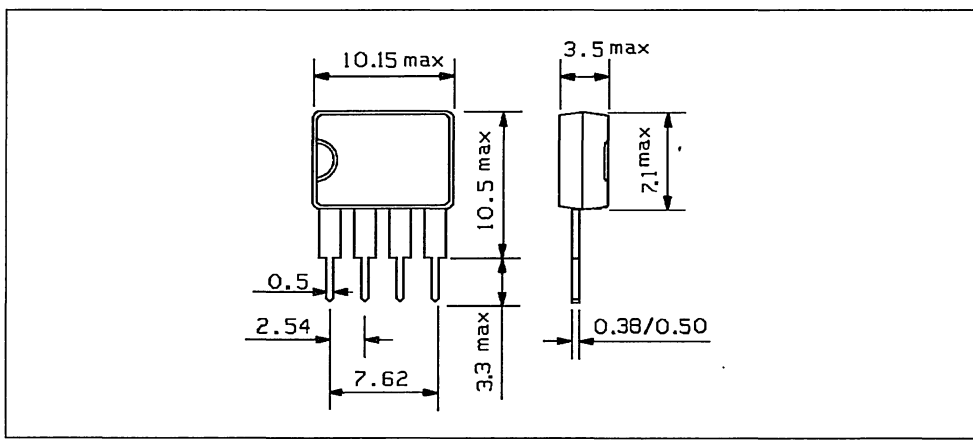


MARKING : Logo, Date Code,part Number.

PACKAGING : Products supplied in antistatic tubes.

PACKAGE MECHANICAL DATA (in millimeters)

SIP 4 Plastic



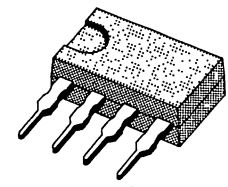
SGS-THOMSON MICROELECTRONICS

LCP150S

PROGRAMMABLE TRANSIENT VOLTAGE SUPPRESSOR FOR SLIC PROTECTION

FEATURES

- DUAL PROGRAMMABLE TRANSIENT SUPPRESSOR.
- HIGH SURGE CURRENT CAPABILITY
  - I_{PP} = 50 A, 10/1000 µs.
  - I_{PP} = 60 A, 5/320 µs.
  - I_{PP} = 150 A, 2/10 µs.
- WIDE NEGATIVE FIRING VOLTAGE RANGE: V_{MGL} = -80 V max
- HOLDING CURRENT = 150 mA min.
- LOW GATE TRIGGERING CURRENT: I_{GT} = 15 mA max.



SIP 4
(Plastic)

DESCRIPTION

This device has been especially designed to protect subscriber line card interfaces (SLIC) against transient overvoltages.

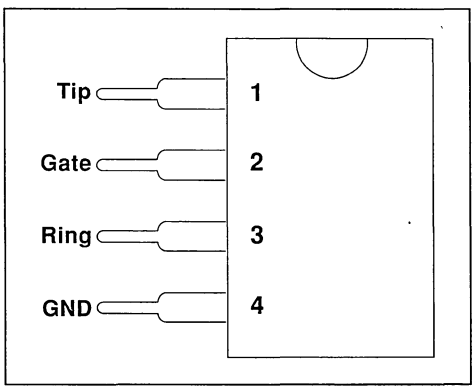
Positive overloads are clipped with two diodes. When negative surges are suppressed by two protection thyristors, the breakdown voltage of which is referenced to the -Vbat.

This component presents a very low gate triggering current (I_{GT}) in order to reduce the current comsumption on PC board during the firing phase.

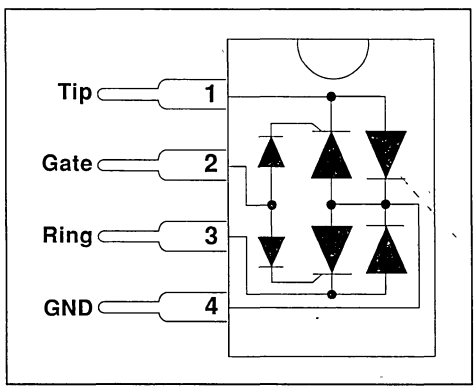
IN ACCORDANCE WITH FOLLOWING STANDARDS :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

CONNECTION DIAGRAM



SCHEMATIC DIAGRAM

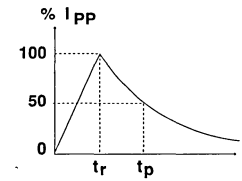


ABSOLUTE RATINGS (limiting values) ($-40°C \leq T_{amb} \leq +85°C$)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current see note 1.	10/1000 µs 5/320 µs 2/10 µs	50 60 150	A
I_{TSM}	Non repetitive surge peak on-state current F = 50 Hz	tp = 10 ms tp = 1 s	25 8	A
I_{GSM}	Maximum gate current (hall sine wave 10 ms)		2	A
V_{MLG} V_{MGL}	Maximum Voltage LINE/GND Maximum Voltage GATE/LINE		- 100 - 80	V
T_{stg} T_j	Storage and operating junction temperature range		- 55 to + 150 150	°C °C

Note 1: Pulse waveform

10/1000 µs	tr = 10 µs	tp = 1000 µs
5/320 µs	tr = 5 µs	tp = 320 µs
2/10 µs	tr = 2 µs,	tp = 10 µs

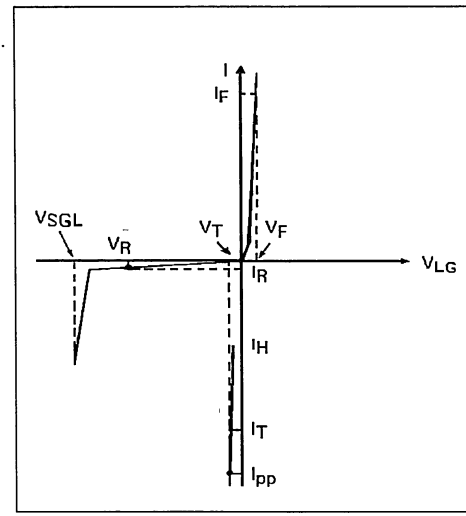


THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
R_{th} (j-a)	Junction-to-ambient	80	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
I_{GT}	Gate Trigger Current
I_H	Holding Current
I_R	Reverse Leakage Current LINE/GND
I_{RG}	Reverse Leakage Current GATE/LINE
V_R	Reverse Voltage LINE/GND
V_F	Forward Voltage LINE/GND
V_{GT}	Gate Trigger Voltage
V_{FP}	Peak Forward Voltage LINE/GND
V_{SGL}	Dynamic Switching Voltage GND/LINE
V_{gate}	GATE/GND Voltage
V_{LG}	LINE/GND Voltage
dv/dt	Critical Rate of rise of off State Voltage
V_T	On State Voltage
C_{off}	Off State Capacitance LINE/GND



PARAMETERS RELATED TO THE DIODE LINE/GND

Symbol	Test Conditions	Max.	Unit
V_F	Square pulse, Tp = 500 µs, I_F = 5 A	3	V
V_{FP}	Ipp = 40 A, 10/1000 µs.	15	V

PARAMETERS RELATED TO PROTECTION THYRISTOR

Symbol	Tests Conditions		Min.	Max.	Unit
I_{GT}	$V_{GND/LINE}$ = -48 V		0.2	15	mA
I_H	V_{GATE}= -48 V	Note 2.	150		mA
V_{GT}	at I_{GT}			2.5	V
I_{RG}	Tc = 25°C Tc = 70°C	V_{RG} = -75 V V_{RG} = -75 V		5 50	µA µA
V_{SGL}	V_{GATE}= -48 V	Note 2.		- 63	V
V_T	Square pulse, Tp = 500 µs, I_T = 0.5 A Square pulse, Tp = 500 µs, I_T = 3 A			3 4	V V

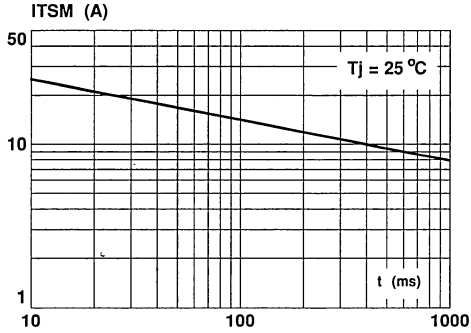
PARAMETERS RELATIVE TO DIODE AND PROTECTION THYRISTOR

Symbol	Tests Conditions			Min.	Max.	Unit
I_R	Tc = 25°C Tc = 70°C	-1 < V_{GL} < -Vbat -1 < V_{GL} < -Vbat	V_R = - 85 V V_R = - 85 V		5 50	µA µA
C_{off}	V_R = - 3 V V_R = - 48 V		F < 1MHz F < 1MHz		150 80	pF pF

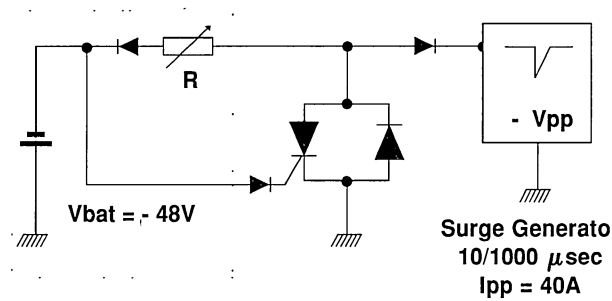
All Parameters Tested at 25 °C except when indicated.

Note 2 : See test circuit for I_H and V_{SGL}.

Figure 1 : Non repetitive surge peak on-state current. (with sinusoidal pulse : f =50Hz)



TEST CIRCUIT FOR I_H AND V_{SGL} PARAMETERS.



This is a GO-NOGO Test which allows to confirm the holding current (I_H) level, and to measure the dynamic switching voltage (V_{SGL}).

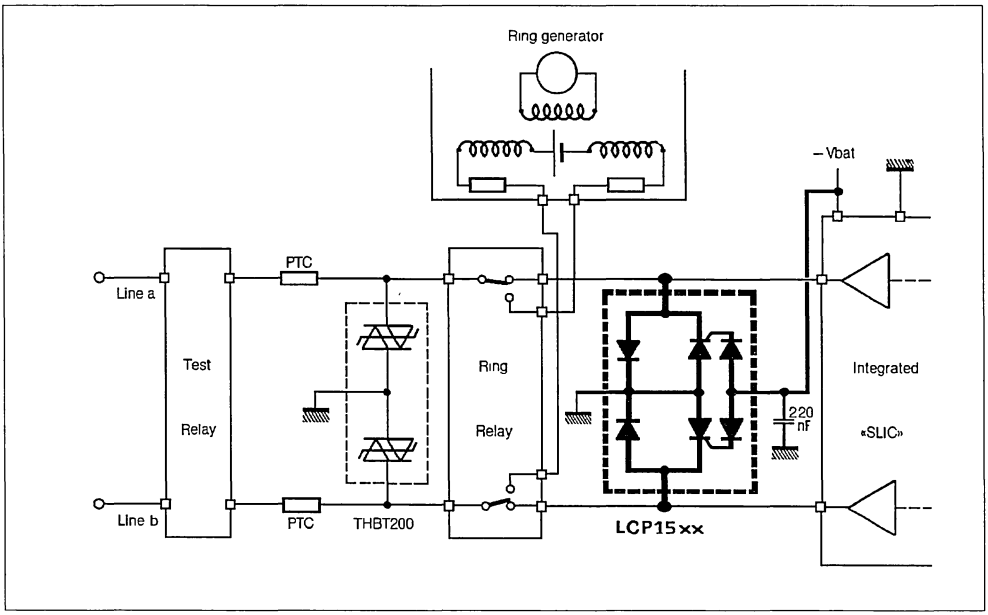
TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.
2) Fire the D.U.T with a surge Current : Ipp = 40A , 10/1000 µs.
3) The D.U.T will come back to the OFF-State within a duration of 50 ms max.

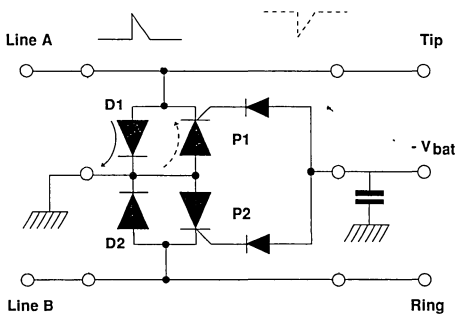
- The V_{SGL} is measured just before firing.

APPLICATION CIRCUIT

Typical slic protection concept



FUNCTIONAL DESCRIPTION



LINE A PROTECTION:

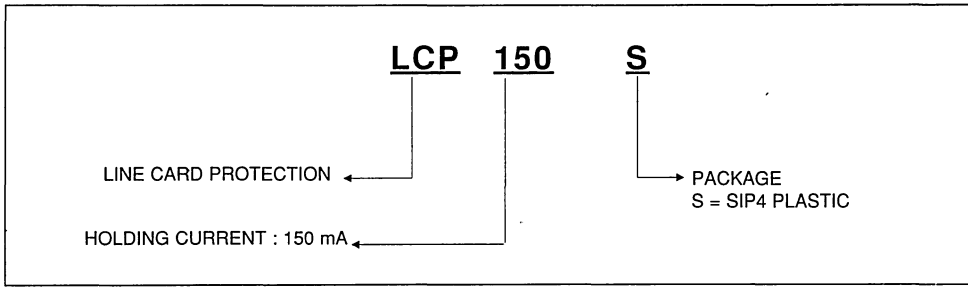
- For positive surges versus GND, the diode D1 will conduct.
- For negative surges versus GND, the protection device P1 will trigger at a voltage fixed by the -VBAT reference.

LINE B PROTECTION:

- For surges on Line B, the operating mode is the same , D2 or P2 is activated.

- A capacitor (C = 220nF) can be added close to the gate of the LCP15xx, in order to speed up the triggering.

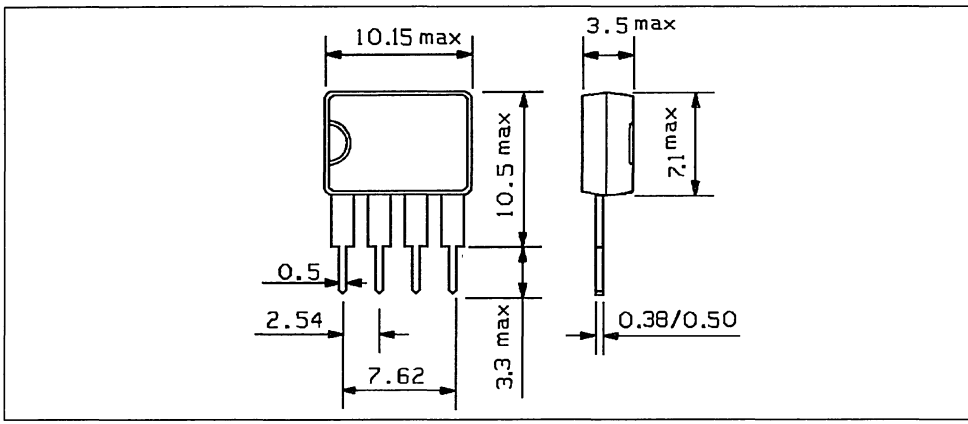
ORDER CODE



MARKING = Logo, date code, LCP150S.

PACKAGE MECHANICAL DATA (in millimeters)

SIP 4 Plastic



Packaging : Products supplied in antistatic tubes.

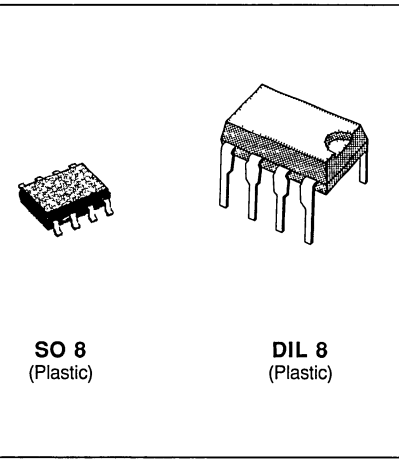
SGS-THOMSON MICROELECTRONICS

LCP1511
LCP1512

PROGRAMMABLE TRANSIENT VOLTAGE SUPPRESSOR FOR SLIC PROTECTION

FEATURES

- DUAL PROGRAMMABLE TRANSIENT SUPPRESSOR.
- WIDE NEGATIVE FIRING VOLTAGE RANGE: V_{MGL} = -80 V max
- HOLDING CURRENT = 150 mA.
- LOW GATE TRIGGERING CURRENT: I_{GT} = 15 mA max.
- PEAK PULSE CURRENT : I_{PP} = 30 A , 10/1000 µs
- AVAILABLE IN SO 8 AND DIP 8.



SO 8 (Plastic)

DIL 8 (Plastic)

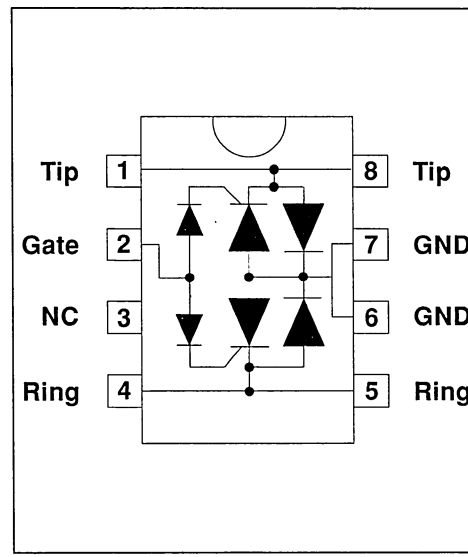
DESCRIPTION

This device has been especially designed to protect subscriber line card interfaces (SLIC) against transient overvoltages.

Positive overloads are clipped with two diodes. When negative surges are suppressed by two protection thyristors, the breakdown voltage of which is referenced to the -Vbat.

This component presents a very low gate triggering current (I_{GT}) in order to reduce the current comsumption on PC board during the firing phase .
A particular attention has been given to the internal wire bonding . A "4-points configuration" ensures a reliable protection, eliminating the overvoltage introduced by the parasitic inductances of the wiring (Ldi/dt) especially for very fast transients.

SCHEMATIC DIAGRAM



IN ACCORDANCE WITH FOLLOWING STANDARDS :

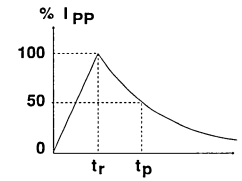
CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

ABSOLUTE RATINGS (limiting values) (-40°C ≤ Tamb ≤ +85°C)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current see note 1.	10/1000 µs 5/320 µs 2/10 µs	30 40 90	A
I_{TSM}	Non repetitive surge peak on-state current f = 50 Hz	tp = 10 ms tp = 1 s	5 3.5	A
I_{GSM}	Maximum gate current (hall sine wave 10 ms)		2	A
V_{MLG} V_{MGL}	Maximum Voltage LINE/GND Maximum Voltage GATE/LINE		- 100 - 80	V
T_{stg} T_j	Storage and operating junction temperature range		- 55 to + 150 150	°C °C

Note 1: **Pulse waveform**

10/1000 µs	tr = 10 µs	tp = 1000 µs
5/320 µs	tr = 5 µs	tp = 320 µs
2/10 µs	tr = 2 µs,	tp = 10 µs

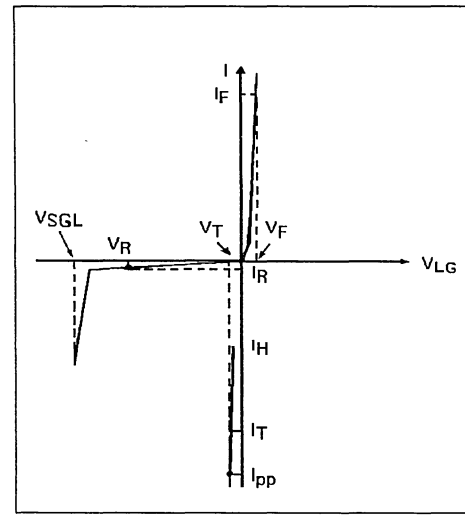


THERMAL RESISTANCES

Symbol	Parameter		Value	Unit
R_{th} (j-a)	Junction-to-ambient	DIL 8 SO 8	125 171	°C/W °C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
I_{GT}	Gate Trigger Current
I_H	Holding Current
I_R	Reverse Leakage Current LINE/GND
I_{RG}	Reverse Leakage Current GATE/LINE
V_R	Reverse Voltage LINE/GND
V_F	Forward Voltage LINE/GND
V_{GT}	Gate Trigger Voltage
V_{FP}	Peak Forward Voltage LINE/GND
V_{SGL}	Dynamic Switching Voltage GND/LINE
V_{gate}	GATE/GND Voltage
V_{LG}	LINE/GND Voltage
dv/dt	Critical Rate of rise of off State Voltage
V_T	On State Voltage
C_{off}	Off State Capacitance LINE/GND



PARAMETERS RELATED TO THE DIODE LINE/GND

Symbol	Test Conditions	Max.	Unit
V_F	Square pulse, tp = 500 µs, I_F = 5 A	3	V
V_{FP}	Ipp = 30 A, 10/1000 µs.	15	V

PARAMETERS RELATED TO PROTECTION THYRISTOR

Symbol	Tests Conditions		Min.	Max.	Unit
I_{GT}	$V_{GND/LINE}$ = -48 V		0.2	15	mA
I_H	V_{GATE}= -48 V	Note 2.	150		mA
V_{GT}	at I_{GT}			2.5	V
I_{RG}	Tc = 25°C Tc = 70°C	V_{RG} = -75 V V_{RG} = -75 V		5 50	µA µA
V_{SGL}	V_{GATE}= -48 V	Note 2.		- 63	V
V_T	Square pulse, Tp = 500 µs, I_T = 0.5 A Square pulse, Tp = 500 µs, I_T = 3 A			3 4	V V

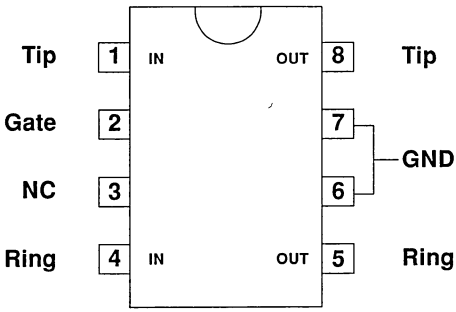
PARAMETERS RELATIVE TO DIODE AND PROTECTION THYRISTOR

Symbol	Tests Conditions			Min.	Max.	Unit
I_R	Tc = 25°C Tc = 70°C	-1 < V_{GL} < -Vbat -1 < V_{GL} < -Vbat	V_R = - 85 V V_R = - 85 V		5 50	µA µA
C_{off}	V_R = - 3 V V_R = - 48 V		F < 1MHz F < 1MHz		100 50	pF pF

All Parameters Tested at 25 °C except when indicated.

Note 2 : See test circuit for I_H and V_{SGL}.

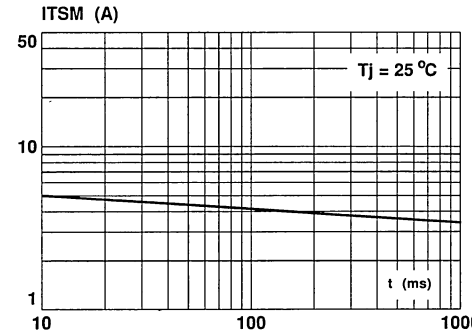
APPLICATION NOTE



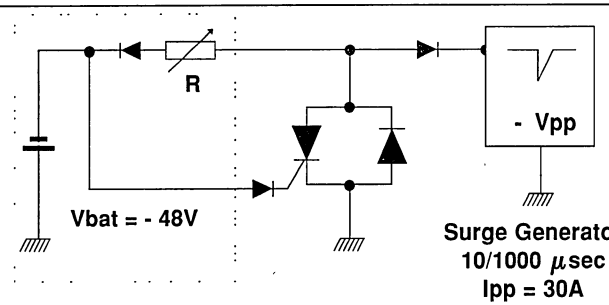
4- points structure lay-out.

In order to take advantage of the "4-points structure" of the LCPxxxx, the tip and Ring lines have to cross through the device. In this case, the device will eliminate the overvoltages generated by the parasitic inductances of the wiring (Ldi/dt), especially for very fast Transients.

Figure 1 : Non repetitive surge peak on-state current. (with sinusoidal pulse : F =50Hz)



TEST CIRCUIT FOR I_H AND V_{SGL} PARAMETERS



This is a GO-NOGO Test which allows to confirm the holding current (I_H) level, and to measure the dynamic switching voltage (V_{SGL}).

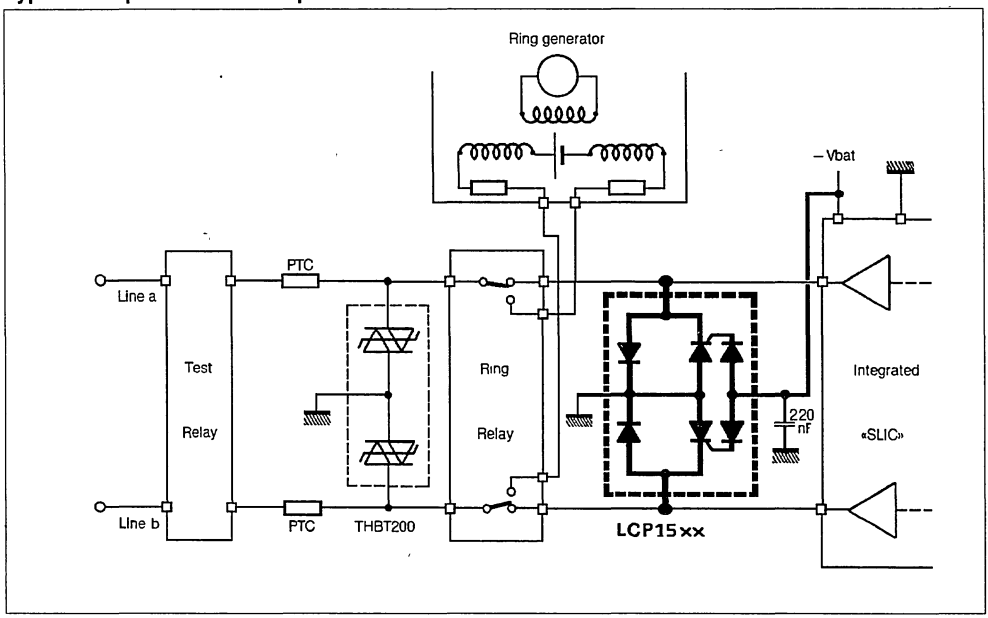
TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.
2) Fire the D.U.T with a surge Current : Ipp = 30A , 10/1000 µs.
3) The D.U.T will come back to the OFF-State within a duration of 50 ms max.

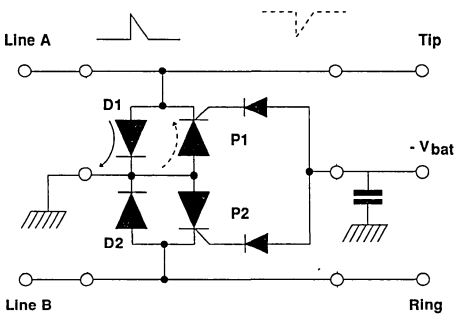
- The V_{SGL} is measured just before firing.

APPLICATION CIRCUIT

Typical slic protection concept



FUNCTIONAL DESCRIPTION



LINE A PROTECTION:

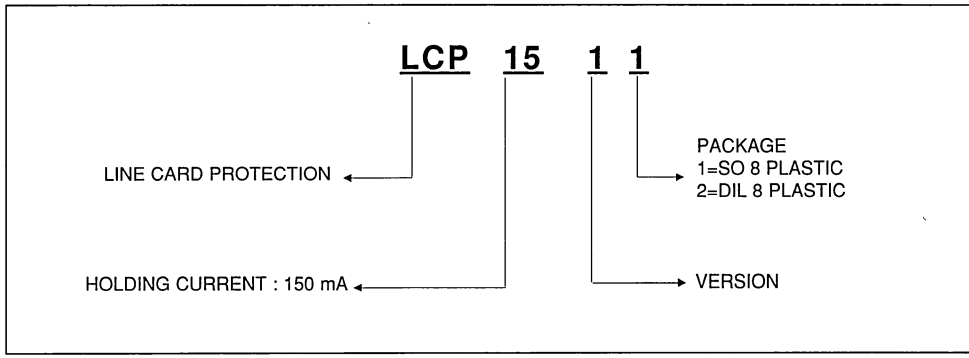
- For positive surges versus GND, the diode D1 will conduct.
- For negative surges versus GND, the protection device P1 will trigger at a voltage fixed by the -VBAT reference.

LINE B PROTECTION:

- For surges on Line B, the operating mode is the same , D2 or P2 is activated.

- A capacitor (C = 220nF) can be added close to the gate of the LCP15xx, in order to speed up the triggering.

ORDER CODE



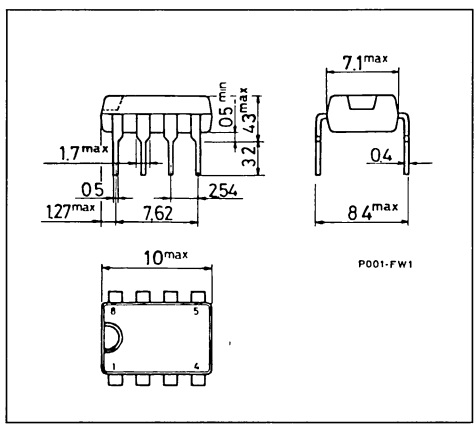
MARKING

Package	Type	Marking
SO8	LCP1511	CP1511
DIL8	LCP1512	CP1512

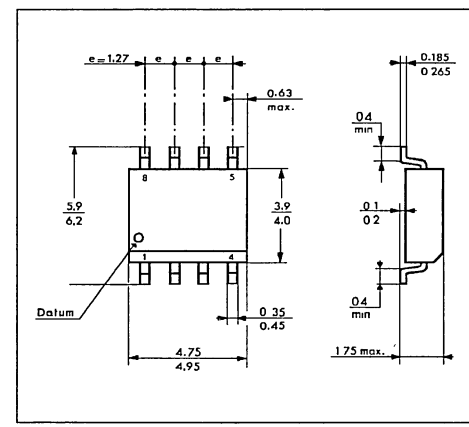
Packaging : Products supplied in antistatic tubes.

PACKAGE MECHANICAL DATA (in millimeters)

DIL 8 Plastic

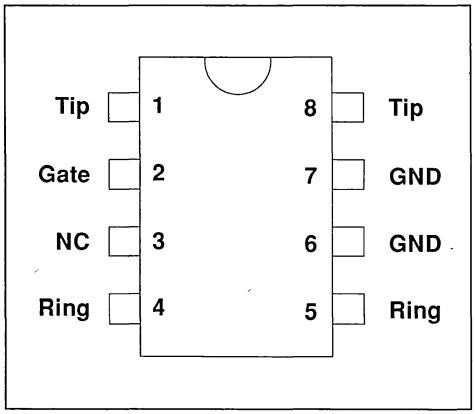


SO 8 Plastic

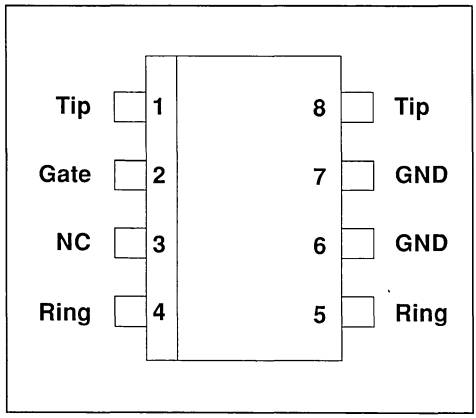


CONNECTION DIAGRAMS

DIL 8 Plastic



SO 8 Plastic

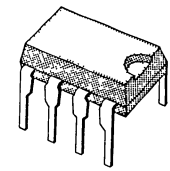


LS5018B
LS5060B/LS5120B

TRISIL

FEATURES

- BIDIRECTIONAL CROWBAR PROTECTION.
- BREAKDOWN VOLTAGE RANGE: FROM 18 V To 120 V.
- HOLDING CURRENT = 200 mA min.
- HIGH SURGE CURRENT CAPABILITY I_{PP} = 100A 10/1000 µs

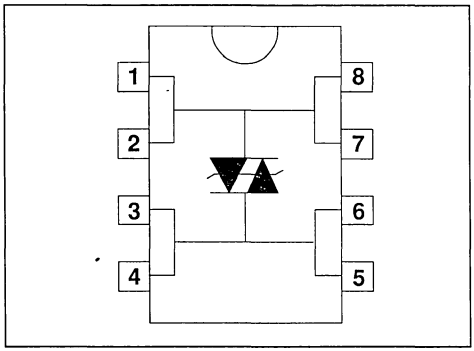


DIL 8
(Plastic)

DESCRIPTION

The LS50xxB series has been designed to protect telecommunication equipment against lightning and transients induced by AC power lines.
Its high surge current capability makes the LS50xxB a reliable protection device for very exposed equipment, or when series resistors are very low.

SCHEMATIC DIAGRAM



IN ACCORDANCE WITH FOLLOWING STANDARDS :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

ABSOLUTE RATINGS (limiting values) (- 40°C ≤ T_{amb} ≤ +85°C)

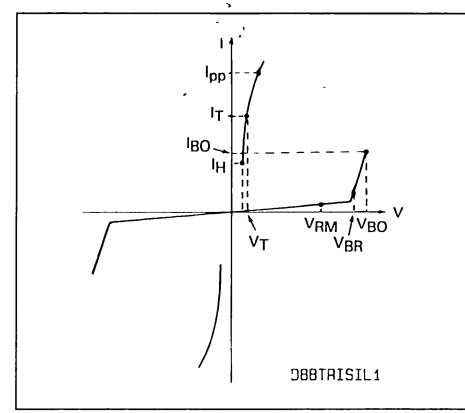
Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current	10/1000 µs 8/20 µs	100 250	A
I_{TSM}	Non repetitive surge peak on-state current	tp = 20 ms	50	A
di/dt	Critical rate of rise of on-state current	Non repetitive	100	A/µs
dv/dt	Critical rate of rise of off-state voltage	67% V_{BR}	5	KV/µs
T_{stg} T_j	Storage and operating junction temperature range		- 40 to + 150 150	°C °C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
R_{th} (j-a)	Junction-to-ambient	80	°C/W

ELECTRICAL CHARACTERISTICS.

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{BO}	Breakover voltage
I_H	Holding current
V_T	On-state voltage @ I_T
I_{BO}	Breakover current
I_{PP}	Peak pulse current

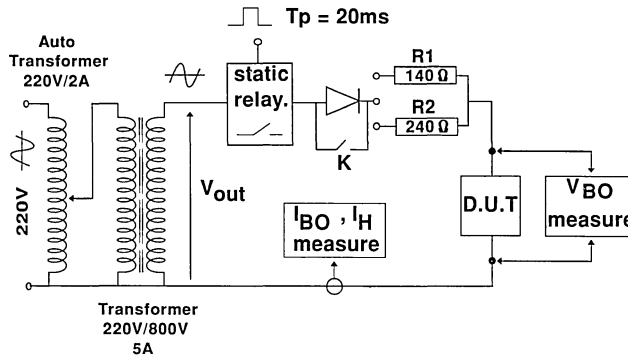


Type	I_{RM} @ V_{RM} max		V_{BR} @ I_R min		V_{BO} max	@ min note 1	I_{BO} max	I_H min note 1	V_T max note 2	C max note 3
	µA	V	V	mA	V	mA	mA	mA	V	pF
LS5018B	5	16	17	1	22		1300	200	3	150
LS5060B	10	50	60	1	85		1000	200	3	150
LS5120B	20	100	120	1	180	500	1250	250	3	150

All parameters tested at 25°C, except where indicated.

Note 1 : See the reference test circuit for I_H, I_{BO} and V_{BO} parameters.
Note 2 : Square pulse T_P= 500µs - I_T = 1A.
Note 3 : V_R = 5 V, F = 1MHz.

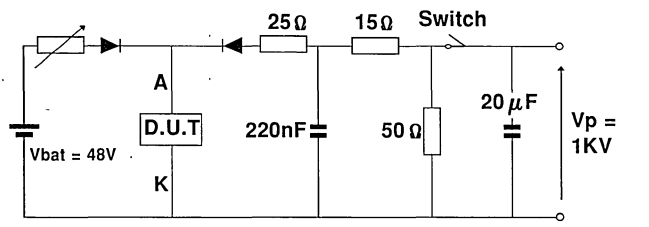
REFERENCE TEST CIRCUIT FOR I_H, I_{BO} and V_{BO} parameters :



TEST PROCEDURE :

- Pulse Test duration (Tp = 20ms):
  - For Bidirectional devices = Switch K is closed
  - For Unidirectional devices = Switch K is open.
- V_{OUT} Selection
  - Device with $V_{BR} \leq 150$ Volt
    - $V_{OUT} = 250\ V_{RMS}$, $R_1 = 140\ \Omega$.
  - Device with $V_{BR} \geq 150$ Volt
    - $V_{OUT} = 480\ V_{RMS}$, $R_2 = 240\ \Omega$.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT = GO - NOGO TEST.



Surge Generator
10/700 µsec
Vp =1KV / Ipp = 25A

This is a GO-NOGO Test which allows to confirm the holding current (I_H) level in a functional test circuit. This test can be performed if the reference test circuit can't be implemented.

TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.
2) Fire the D.U.T with a surge Current : Ipp = 25A , 10/700 µs.
3) The D.U.T will come back to the OFF-State within a duration of 50 ms max.

Figure 1 : Non repetitive surge peak on state current versus number of cycles. (with sinusoïdal pluse: F = 50 Hz).

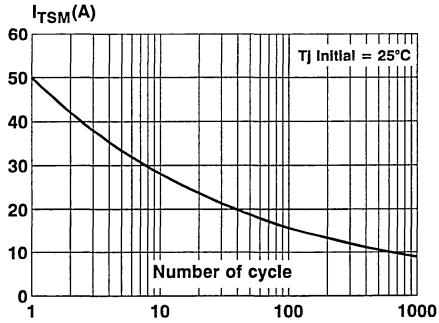


Figure 2 : Relative variation of holding current versus ambient temperature.

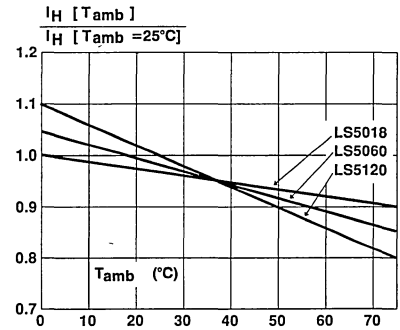


Figure 3 : Relative variation of breakdown voltage versus ambient temperature.

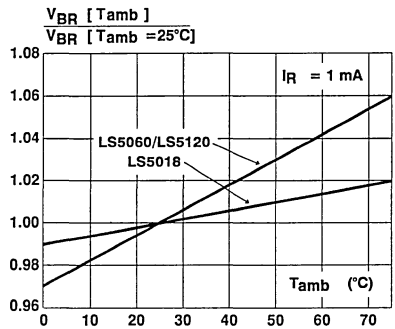
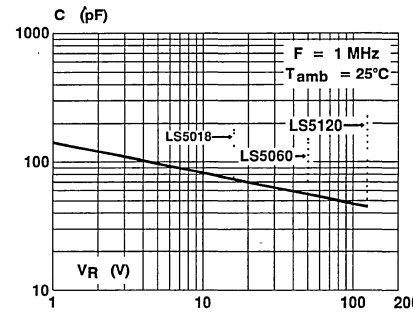
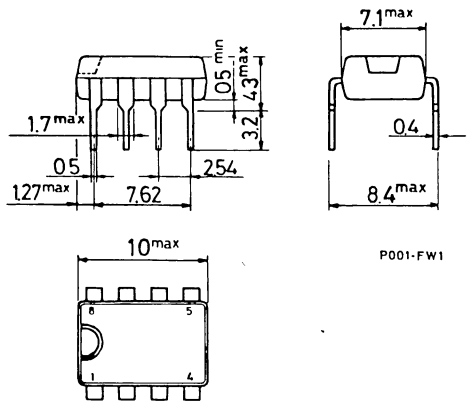


Figure 4 : Junction capacitance versus reverse applied voltage.



PACKAGE MECHANICAL DATA (in millimeters).

DIL 8 Plastic



MARKING : Logo, Date Code,part Number.

PACKAGING : Products supplied in antistatic tubes.

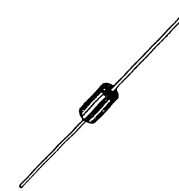
SGS-THOMSON MICROELECTRONICS

P6KE6V8P,A/440P,A
P6KE6V8CP,A/440CP,CA

TRANSIL

FEATURES

- PEAK PULSE POWER= 600 W @ 1ms.
- BREAKDOWN VOLTAGE RANGE : From 6V8 to 440 V.
- UNI AND BIDIRECTIONAL TYPES.
- LOW CLAMPING FACTOR.
- FAST RESPONSE TIME: Tclamping : 1ps (0 V to V_{BR}).
- UL RECOGNIZED.



CB417
(Plastic)

DESCRIPTION

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous reponse to transients makes them particularly suited to protect voltage sensitive devices such as MOS Technology and low voltage supplied IC's.

MECHANICAL CHARACTERISTICS

- Body marked with : Logo, Date Code, Type Code, and Cathode Band (for unidirectional types only).
- Tinned copper leads.
- High temperature soldering.

ABSOLUTE RATINGS (limiting values)

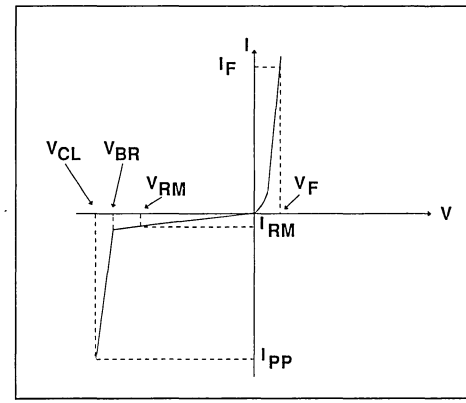
Symbol	Parameter		Value	Unit
P_p	Peak pulse power dissipation See note 1 and derating curve Fig 1.	Tamb = 25°C	600	W
P	Power dissipation on infinite heatsink See note 1 and derating curve Fig 1.	Tlead = 75°C	5	W
I_{FSM}	Non repetitive surge peak forward current For Unidirectional types.	Tamb = 25°C t =10 ms	100	A
T_{stg} T_j	Storage and junction temperature range		- 65 to + 175 175	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		230	°C

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction-leads on infinite heatsink	20	°C/W
R_{th} (j-a)	Junction to ambient. on printed circuit. L_{lead} = 10 mm	85	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage.
V_{BR}	Breakdown voltage.
V_{CL}	Clamping voltage.
I_{RM}	Leakage current @ VRM.
I_{PP}	Surge current.
αT	Voltage temperature coefficient.
V_F	Forward Voltage drop V_F < 3.5V @ I_F = 50 A.



TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Unidirectional	Bidirectional	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
P6KE6V8P	P P6KE6V8CP	1000	5.8	6.45	6.8	7.48	10	10.5	57	13.4	298	5.7	4000
P P6KE6V8A	P P6KE6V8CA	1000	5.8	6.45	6.8	7.14	10	10.5	57	13.4	298	5.7	4000
P6KE7V5P	P6KE7V5CP	500	6.4	7.13	7.5	8.25	10	11.3	53	14.5	276	6.1	3700
P6KE7V5A	P P6KE7V5CA	500	6.4	7.13	7.5	7.88	10	11.3	53	14.5	276	6.1	3700
P6KE8V2P	P P6KE8V2CP	200	7.02	7.79	8.2	9.02	10	12.1	50	15.5	258	6.5	3400
P P6KE8V2A	P6KE8V2CA	200	7.02	7.79	8.2	8.61	10	12.1	50	15.5	258	6.5	3400
P6KE9V1P	P6KE9V1CP	50	7.78	8.65	9.1	10	1	13.4	45	17.1	234	6.8	3100
P6KE9V1A	P6KE9V1CA	50	7.78	8.65	9.1	9.55	1	13.4	45	17.1	234	6.8	3100
P P6KE10P	P6KE10CP	10	8.55	9.5	10	11	1	14.5	41	18.6	215	7.3	2800
P6KE10A	P6KE10CA	10	8.55	9.5	10	10.5	1	14.5	41	18.6	215	7.3	2800
P6KE11P	P6KE11CP	5	9.4	10.5	11	12.1	1	15.6	38	20.3	197	7.5	2500
P6KE11A	P6KE11CA	5	9.4	10.5	11	11.6	1	15.6	38	20.3	197	7.5	2500
P P6KE12P	P P6KE12CP	5	10.2	11.4	12	13.2	1	16.7	36	21.7	184	7.8	2300
P6KE12A	P6KE12CA	5	10.2	11.4	12	12.6	1	16.7	36	21.7	184	7.8	2300
P6KE13P	P6KE13CP	5	11.1	12.4	13	14.3	1	18.2	33	23.6	169	8.1	2150
P P6KE13A	P P6KE13CA	5	11.1	12.4	13	13.7	1	18.2	33	23.6	169	8.1	2150
P P6KE15P	P P6KE15CP	5	12.8	14.3	15	16.5	1	21.2	28	27.2	147	8.4	1900
P6KE15A	P6KE15CA	5	12.8	14.3	15	15.8	1	21.2	28	27.2	147	8.4	1900
P6KE16P	P6KE16CP	5	13.6	15.2	16	17.6	1	22.5	27	28.9	138	8.6	1800
P6KE16A	P6KE16CA	5	13.6	15.2	16	16.8	1	22.5	27	28.9	138	8.6	1800
P P6KE18P	P P6KE18CP	5	15.3	17.1	18	19.8	1	25.2	24	32.5	123	8.8	1600
P P6KE18A	P P6KE18CA	5	15.3	17.1	18	18.9	1	25.2	24	32.5	123	8.8	1600
P6KE20P	P P6KE20CP	5	17.1	19	20	22	1	27.7	22	36.1	111	9.0	1500
P P6KE20A	P P6KE20CA	5	17.1	19	20	21	1	27.7	22	36.1	111	9.0	1500
P6KE22P	P P6KE22CP	5	18.8	20.9	22	24.2	1	30.6	20	39.3	102	9.2	1350

P = Prefered device

TYPES		I_{RM} @ V_{RM}		V_{BR} @ I_R				V_{CL} @ I_{PP}		V_{CL} @ I_{PP}		αT	C
		max		min	nom	max		max		max		max	typ
						note2		10/1000µs		8/20µs		note3	note4
Unidirectional	**Bidirectional**	**µA**	**V**	**V**	**V**	**V**	**mA**	**V**	**A**	**V**	**A**	**10^{-4}/°C**	**(pF)**
P6KE22A	P6KE22CA	5	18.8	20.9	22	23.1	1	30.6	20	39.3	102	9.2	1350
P6KE24P	P6KE24CP	5	20.5	22.8	24	26.4	1	33.2	18	42.8	93	9.4	1250
P P6KE24A	P6KE24CA	5	20.5	22.8	24	25.2	1	33.2	18	42.8	93	9.4	1250
P P6KE27P	P P6KE27CP	5	23.1	25.7	27	29.7	1	37.5	16	48.3	83	9.6	1150
P6KE27A	P6KE27CA	5	23.1	25.7	27	28.4	1	37.5	16	48.3	83	9.6	1150
P P6KE30P	P P6KE30CP	5	25.6	28.5	30	33	1	41.5	14.5	53.5	75	9.7	1075
P P6KE30A	P P6KE30CA	5	25.6	28.5	30	31.5	1	41.5	14.5	53.5	75	9.7	1075
P6KE33P	P6KE33CP	5	28.2	31.4	33	36.3	1	45.7	13.1	59.0	68	9.8	1000
P P6KE33A	P P6KE33CA	5	28.2	31.4	33	34.7	1	45.7	13.1	59.0	68	9.8	1000
P P6KE36P	P P6KE36CP	5	30.8	34.2	36	39.6	1	49.9	12	64.3	62	9.9	950
P P6KE36A	P6KE36CA	5	30.8	34.2	36	37.8	1	49.9	12	64.3	62	9.9	950
P P6KE39P	P P6KE39CP	5	33.3	37.1	39	42.9	1	53.9	11.1	69.7	57	10.0	900
P P6KE39A	P P6KE39CA	5	33.3	37.1	39	41.0	1	53.9	11.1	69.7	57	10.0	900
P6KE43P	P6KE43CP	5	36.8	40.9	43	47.3	1	59.3	10.1	76.8	52	10.1	850
P6KE43A	P6KE43CA	5	36.8	40.9	43	45.2	1	59.3	10.1	76.8	52	10.1	850
P6KE47P	P P6KE47CP	5	40.2	44.7	47	51.7	1	64.8	9.3	84	48	10.1	800
P6KE47A	P P6KE47CA	5	40.2	44.7	47	49.4	1	64.8	9.3	84	48	10.1	800
P6KE51P	P P6KE51CP	5	43.6	48.5	51	56.1	1	70.1	8.6	91	44	10.2	750
P6KE51A	P P6KE51CA	5	43.6	48.5	51	53.6	1	70.1	8.6	91	44	10.2	750
P6KE56P	P P6KE56CP	5	47.8	53.2	56	61.6	1	77	7.8	100	40	10.3	700
P6KE56A	P6KE56CA	5	47.8	53.2	56	58.8	1	77	7.8	100	40	10.3	700
P6KE62P	P6KE62CP	5	53.0	58.9	62	68.2	1	85	7.1	111	36	10.4	650
P6KE62A	P6KE62CA	5	53.0	58.9	62	65.1	1	85	7.1	111	36	10.4	650
P6KE68P	P P6KE68CP	5	58.1	64.6	68	74.8	1	92	6.5	121	33	10.4	625
P6KE68A	P6KE68CA	5	58.1	64.6	68	71.4	1	92	6.5	121	33	10.4	625
P6KE75P	P6KE75CP	5	64.1	71.3	75	82.5	1	103	5.8	134	30	10.5	575
P6KE75A	P6KE75CA	5	64.1	71.3	75	78.8	1	103	5.8	134	30	10.5	575
P6KE82P	P P6KE82CP	5	70.1	77.9	82	90.2	1	113	5.3	146	27	10.5	550
P6KE82A	P6KE82CA	5	70.1	77.9	82	86.1	1	113	5.3	146	27	10.5	550
P6KE91P	P6KE91CP	5	77.8	86.5	91	100	1	125	4.8	162	25	10.6	525
P6KE91A	P6KE91CA	5	77.8	86.5	91	95.5	1	125	4.8	162	25	10.6	525
P6KE100P	P6KE100CP	5	85.5	95.0	100	110	1	137	4.4	178	22.5	10.6	500
P6KE100A	P6KE100CA	5	85.5	95.0	100	105	1	137	4.4	178	22.5	10.6	500
P6KE110P	P6KE110CP	5	94.0	105	110	121	1	152	3.9	195	20.5	10.7	470
P6KE110A	P6KE110CA	5	94.0	105	110	116	1	152	3.9	195	20.5	10.7	470
P6KE120P	P6KE120CP	5	102	114	120	132	1	165	3.6	212	19	10.7	450
P6KE120A	P6KE120CA	5	102	114	120	126	1	165	3.6	212	19	10.7	450
P6KE130P	P P6KE130CP	5	111	124	130	143	1	179	3.4	230	17.5	10.7	420
P6KE130A	P6KE130CA	5	111	124	130	137	1	179	3.4	230	17.5	10.7	420
P6KE150P	P P6KE150CP	5	128	143	150	165	1	207	2.9	265	15	10.8	400
P P6KE150A	P P6KE150CA	5	128	143	150	158	1	207	2.9	265	15	10.8	400
P6KE160P	P P6KE160CP	5	136	152	160	176	1	219	2.7	282	14	10.8	380
P6KE160A	P6KE160CA	5	136	152	160	168	1	219	2.7	282	14	10.8	380
P6KE170P	P6KE170CP	5	145	161	170	187	1	234	2.6	301	13	10.8	370
P6KE170A	P6KE170CA	5	145	161	170	179	1	234	2.6	301	13	10.8	370
P6KE180P	P P6KE180CP	5	154	171	180	198	1	246	2.4	317	12.6	10.8	360
P6KE180A	P6KE180CA	5	154	171	180	189	1	246	2.4	317	12.6	10.8	360
P6KE200P	P P6KE200CP	5	171	190	200	220	1	274	2.2	353	11.3	10.8	350
P P6KE200A	P P6KE200CA	5	171	190	200	210	1	274	2.2	353	11.3	10.8	350
P6KE220P	P6KE220CP	5	188	209	220	242	1	328	2	388	10.3	10.8	330
P6KE220A	P6KE220CA	5	188	209	220	231	1	328	2	388	10.3	10.8	330
P6KE250P	P P6KE250CP	5	213	237	250	275	1	344	2	442	9	11	310
P6KE250A	P6KE250CA	5	213	237	250	263	1	344	2	442	9	11	310
P6KE280P	P6KE280CP	5	239	266	280	308	1	384	2	494	8	11	300
P6KE280A	P6KE280CA	5	239	266	280	294	1	384	2	494	8	11	300

P = Prefered device

TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Unidirectional	**Bidirectional**	**µA**	**V**	**V**	**V**	**V**	**mA**	**V**	**A**	**V**	**A**	**10^{-4}/°C**	**(pF)**
P6KE300P	P6KE300CP	5	256	285	300	330	1	414	1.6	529	7.6	11	290
P6KE300A	P6KE300CA	5	256	285	300	315	1	414	1.6	529	7.6	11	290
P6KE320P	P6KE320CP	5	273	304	320	352	1	438	1.6	564	7.1	11	280
P6KE320A	P6KE320CA	5	273	304	320	336	1	438	1.6	564	7.1	11	280
P6KE350P	P6KE350CP	5	299	332	350	385	1	482	1.6	618	6.5	11	270
P6KE350A	P6KE350CA	5	299	332	350	368	1	482	1.6	618	6.5	11	270
P6KE400P	P6KE400CP	5	342	380	400	440	1	548	1.3	706	5.7	11	360
P6KE400A	P6KE400CA	5	342	380	400	420	1	548	1.3	706	5.7	11	360
P6KE440P	P6KE440CP	5	376	418	440	484	1	603	1.3	776	5.2	11	350
P6KE440A	P6KE440CA	5	376	418	440	462	1	603	1.3	776	5.2	11	350

All parameters tested at 25 °C, except where indicated.

P = Prefered device

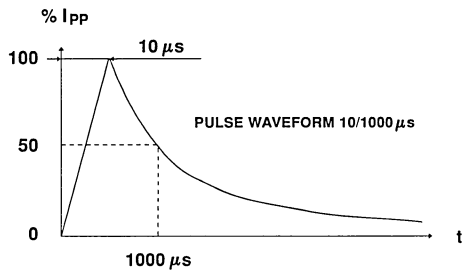
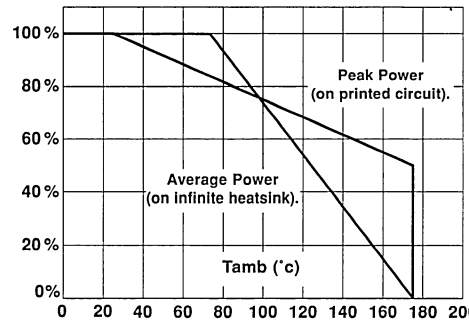


Figure 1: Power dissipation derating versus ambient temperature



Note 1 : For surges greater than the maximum values, the diode will present a short-circuit Anode - Cathode.

Note 2 : Pulse test: $T_P < 50$ ms.

Note 3 : $\Delta V_{BR} = \alpha T \cdot (Ta - 25) \cdot V_{BR(25°C)}$

Note 4 : VR = 0 V, F = 1 MHz For bidirectional types, capacitance value is divided by 2.

Figure 2 : Peak pulse power versus exponential pulse duration.

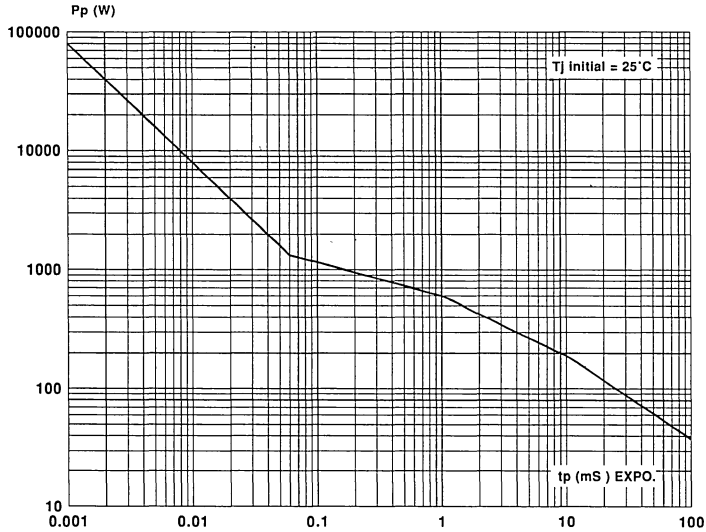
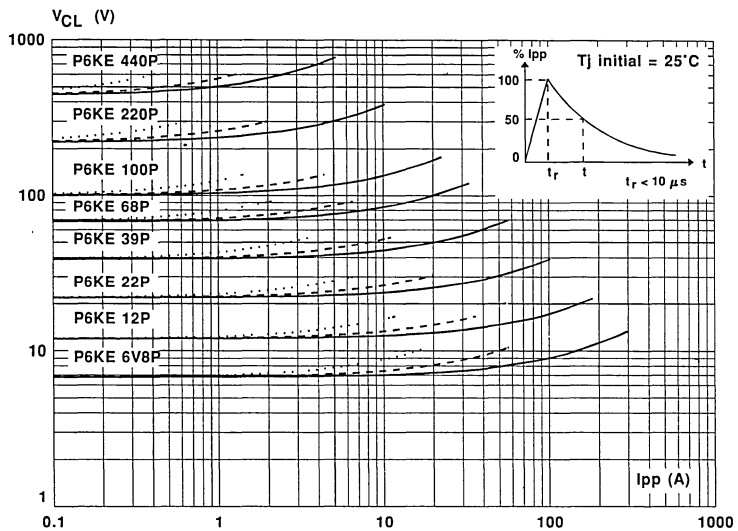


Figure 3 : Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs _____
t = 1 ms ----------
t =10 ms .....



Note : The curves of the figure 3 are specified for a junction temperature of 25 °C before surge.
The given results may be extrapolated for other junction temperatures by using the following formula :
$\Delta V_{(BR)} = \alpha T_{(V(BR))} \cdot [T_a - 25] \cdot V_{(BR)}$.
For intermediate voltages, extrapolate the given results.

Figure 4a : Capacitance versus reverse applied voltage for unidirectional types (typical values).

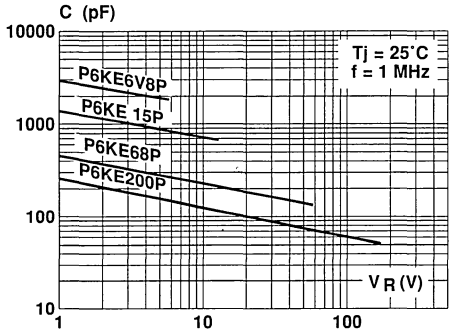


Figure 4b : Capacitance versus reverse applied voltage for bidirectional types (typical values)

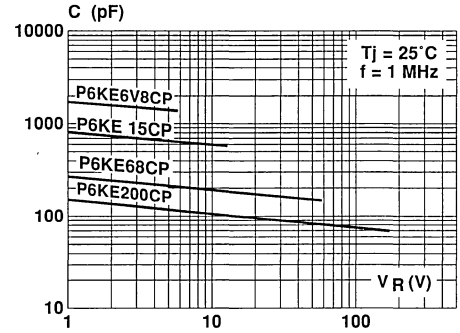


Figure 5 : Peak forward voltage drop versus peak forward current (typical values for unidirectional types).

Note : For units with V_{BR} > 200 V
V_F is twice than shown

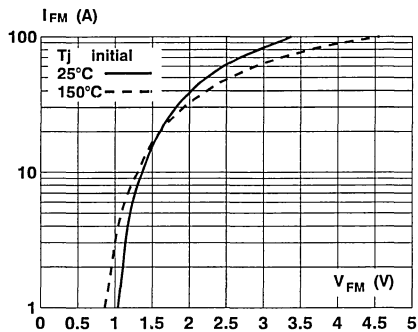
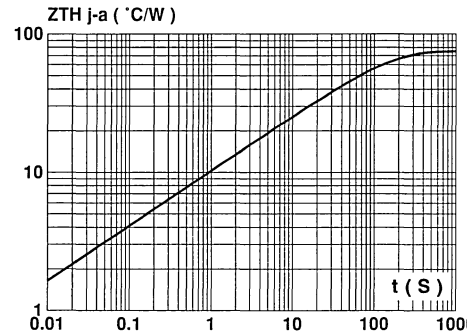


Figure 6 : Transient thermal impedance junction-ambient versus pulse duration. For a mounting on PC Board with L_{lead} = 10mm.



ORDER CODE

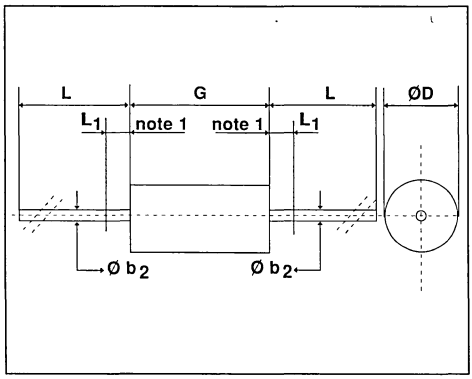
P6 KE 100 C A RL

- 600 W
- BREAKDOWN VOLTAGE
- BIDIRECTIONAL
- TOLERANCE : A = +/- 5%, P = -5%, +10%.
- PACKAGING: = Ammopack, RL = Tape and reel.

MARKING : Logo, Date Code, Type Code, Cathode Band (for unidirectional types only).

PACKAGE MECHANICAL DATA

CB417 (Plastic).



Ref	Millimeters		Inches	
	min	max	min	max
Ø b_2	- -	1.092	-	0.043
Ø D	-	3.683	-	0.145
G	-	8.89	-	0.350
L	25.4	-	1.000	-
L_1	-	1.25	-	0.049

note1:The diameter Ø b_2 is not controlled over zone L_1

Weight = 0.65 g.

Packaging : standard packaging is in tape and reel.

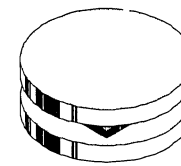
SGS-THOMSON MICROELECTRONICS

SA100 SERIES

SURGE ARRESTORS

FEATURES

- SOLID STATE SURGE ARRESTOR
- VOLTAGE RANGE = 200 V TO 265 V
- TIGHT VOLTAGE TOLERANCE
- FAST RESPONSE TIME
- VERY LOW AND STABLE LEAKAGE CURRENT
- REPETITIVE SURGE CAPABILITY Ipp = 100 A, 10/1000 µs
- FAIL-SAFE WHEN DESTROYED



BUTTON CELL

DESCRIPTION

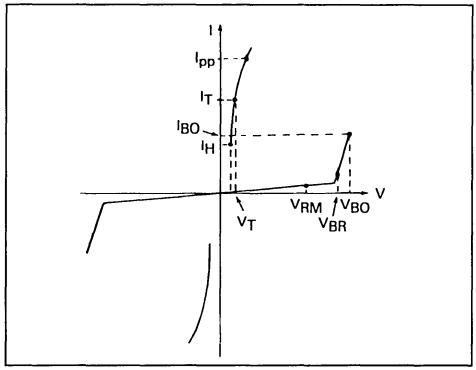
Bidirectional device used for primary protection in telecom equipments.
Providing long service life, and adapted for sensitive electronic equipments protection.
If destroyed the component will continue to guarantee a protection with a permanent short circuit, meaning "fail save criteria" . This particular behaviour will also allow an easy failure detection on the line.

ABSOLUTE RATINGS (limiting values) - 40°C < T_{amb} < +80°C

Symbol	Parameter		Value	Unit
I_{PP}	Peak Pulse Current.	10/1000 µs	100	A
		8/20 µs	200	A
	Fail Save Criteria.	8/20 µs	10	kA
I_{TSM}	Non Repetitive Surge Peak on-state Current One cycle.	60 Hz	30	A
		50Hz	25	A
	Non Repetitive Surge Peak on-state Current F = 50 Hz.	1s	14	A
		2s	10	A
dv/dt	Critical Rate of Rise of on-state Voltage.	67% V_{BR}	10	kV/µs
T_L	Maximum Lead Temperature to Soldering During 10 s.		250	°C

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off Voltage
V_{BR}	Breakdown Voltage
V_{BO}	Breakover Voltage
I_H	Holding Current
V_T	On-state Voltage
I_{BO}	Breakover Current

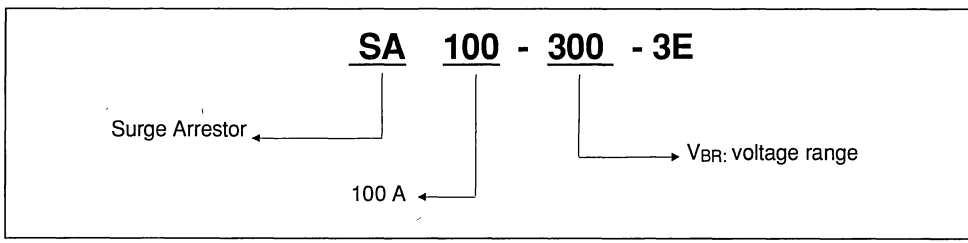


Type	I_{RM} @ V_{RM} max		V_{BR} @ I_R min.		V_{BO} max. note 1	VBO max. note 2	VBO max. note 3	I_{BO} min. note 1	I_H min. note 1	V_T max. note 4	C max. note 5
	(µA)	(V)	(V)	(mA)	(V)	(V)	(V)	(mA)	(mA)	(V)	pF
SA100-230	10	170	200	1	265	350	350	200	260	3.5	200
SA100-300	10	225	265	1	400	400	400	200	260	3.5	200

All parameters tested at 25°C, except where indicated.

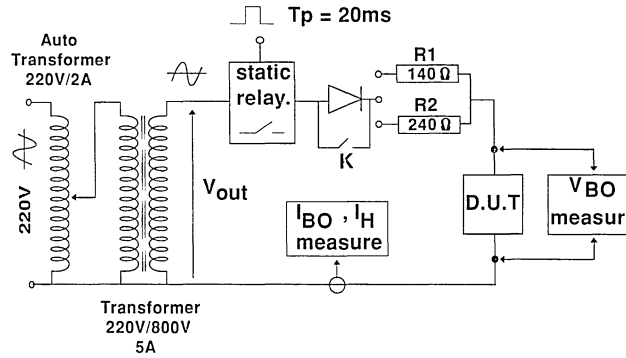
Note 1 : See the reference test circuit for I_H,I_{BO} and V_{BO} parameters
Note 2 : V_{RISE} = 100V/µs.
Note 3 : V_{RISE} = 1KV/µs, di/dt < 10A/µs, I_{PP}= 10A.
Note 4 : Square pulse, T_P = 500 µs, I_T = 5 A.
Note 5 : V_R = 0 V, F = 1 MHz.

ORDER CODE



Product Availability is Submitted to Restricted Conditions- Consult Factory.

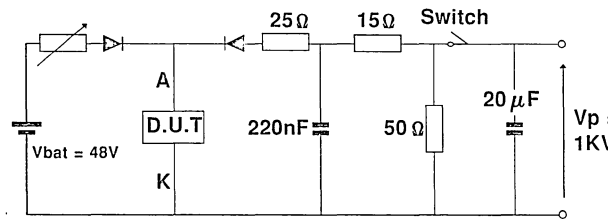
REFERENCE TEST CIRCUIT FOR I_H, I_{BO} and V_{BO} parameters :



TEST PROCEDURE :

- Pulse Test duration (Tp = 20ms):
  - For Bidirectional devices = Switch K is closed
  - For Unidirectional devices = Switch K is open.
- V_{OUT} Selection
  - Device with $V_{BR} \leq 150$ Volt
    - $V_{OUT} = 250\ V_{RMS}$, $R_1 = 140\ \Omega$.
  - Device with $V_{BR} \geq 150$ Volt
    - $V_{OUT} = 480\ V_{RMS}$, $R_2 = 240\ \Omega$.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT = GO - NOGO TEST.



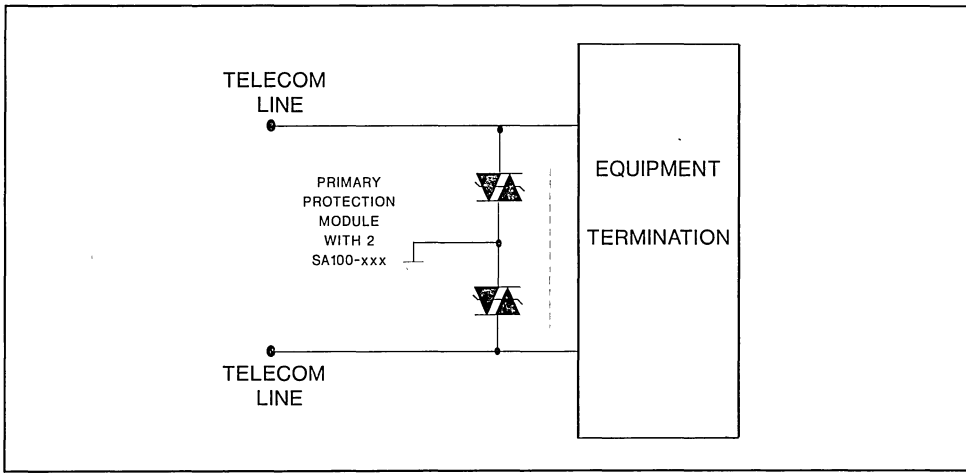
Surge Generator
10/700 µsec
Vp =1KV / Ipp = 25A

This is a GO-NOGO Test which allows to confirm the holding current (I_H) level in a functional test circuit. this test can be performed if the reference test circuit can't be implemented.

TEST PROCEDURE :

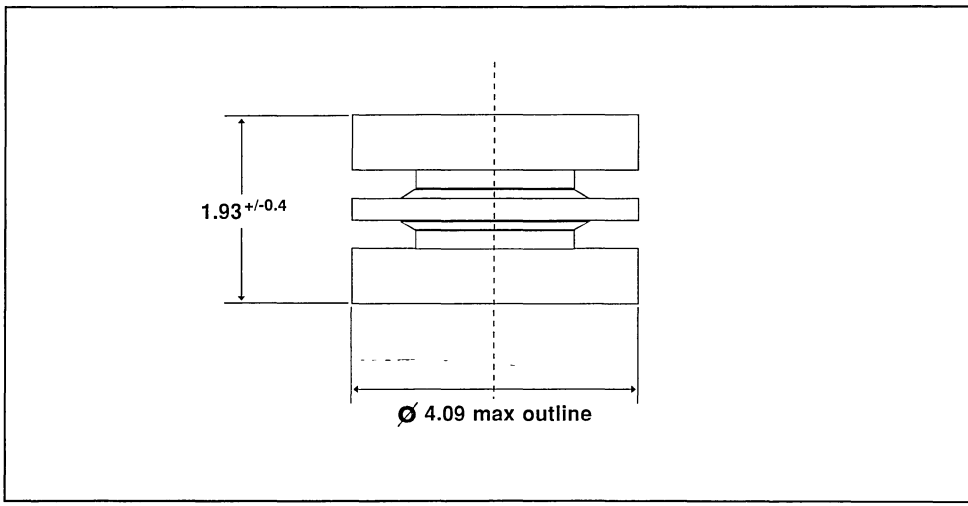
1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.
2) Fire the D.U.T with a surge Current : Ipp = 25A , 10/700 µs.
3) The D.U.T will come back to the OFF-State within a duration of 50 ms max.

APPLICATION DIAGRAM



MECHANICAL DATA

BUTTON CELL (Millimeters)



Packaging : Products are supplied in tubes.

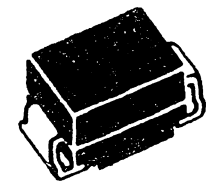
SGS-THOMSON MICROELECTRONICS

SM4T6V8,A/220,A
SM4T6V8C,CA/220C,CA

TRANSIL

FEATURES

- PEAK PULSE POWER= 400 W @ 1ms.
- BREAKDOWN VOLTAGE RANGE : From 6V8 to 220 V.
- UNI AND BIDIRECTIONAL TYPES.
- LOW CLAMPING FACTOR.
- FAST RESPONSE TIME: Tclamping : 1ps (0 V to VBR).
- JEDEC REGISTRED.



SOD 6
(Plastic)

DESCRIPTION

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous reponse to transients makes them praticularly suited to protect voltage sensitive devices such as MOS Technology and low voltage supplied IC's.

MECHANICAL CHARACTERISTICS

- Body marked with : Logo, Date Code, Type Code and Cathode Band (for unidirectional types only).
- Full compatibility with both gluing and paste soldering technologies.
- Excellent on board stability.
- Tinned copper leads.
- High temperature resistant resin.

ABSOLUTE RATINGS (limiting values)

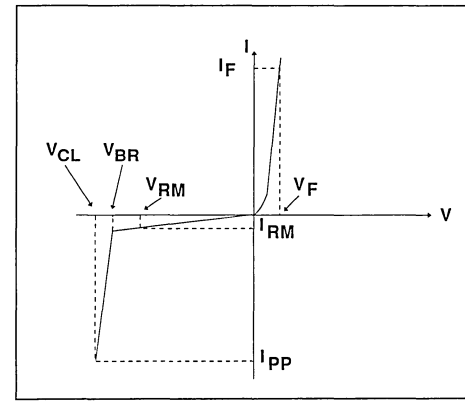
Symbol	Parameter		Value	Unit
P_p	Peak pulse power dissipation See note 1 and derating curve Fig 1.	Tamb = 25°C	400	W
P	Power dissipation on infinite heatsink See note 1 and derating curve Fig 1.	Tlead = 50°C	5	W
I_{FSM}	Non repetitive surge peak forward current. For unidirectional types.	Tamb = 25°C t =10 ms	50	A
T_{stg} T_j	Storage and junction temperature range		- 65 to + 175 150	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		260	°C

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction-leads on infinite heatsink	20	°C/W
R_{th} (j-a)	Junction to ambiant. on printed circuit. With standard footprint dimensions.	100	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage.
V_{BR}	Breakdown voltage.
V_{CL}	Clamping voltage.
I_{RM}	Leakage current @ VRM.
I_{PP}	Surge current.
αT	Voltage temperature coefficient.
V_F	Forward Voltage drop V_F < 3.5V @ I_F = 25 A.



TYPES				I_{RM} @ V_{RM} max		V_{BR} @ I_R min	nom	max		V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
						note2									
Uni directional	*	Bi directional	*	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
SM4T6V8	QD	SM4T6V8C	VD	1000	5.8	6.45	6.8	7.48	10	10.5	38	13.4	174	5.7	3500
SM4T6V8A	QE	SM4T6V8CA	VE	1000	5.8	6.45	6.8	7.14	10	10.5	38	13.4	174	5.7	3500
SM4T7V5	QF	SM4T7V5C	VF	500	6.4	7.13	7.5	8.25	10	11.3	35.4	14.5	160	6.1	3100
SM4T7V5A	QG	SM4T7V5CA	VG	500	6.4	7.13	7.5	7.88	10	11.3	35.4	14.5	160	6.1	3100
SM4T10	QN	SM4T10C	VN	10	8.55	9.5	10	11	1	14.5	27.6	18.6	124	7.3	2000
SM4T10A	QP	SM4T10CA	VP	10	8.55	9.5	10	10.5	1	14.5	27.6	18.6	124	7.3	2000
SM4T12	QS	SM4T12C	VS	5	10.2	11.4	12	13.2	1	16.7	24	21.7	106	7.8	1550
SM4T12A	QT	SM4T12CA	VT	5	10.2	11.4	12	12.6	1	16.7	24	21.7	106	7.8	1550
SM4T15	QW	SM4T15C	VW	5	12.8	14.3	15	16.5	1	21.2	19	27.2	85	8.4	1200
SM4T15A	QX	SM4T15CA	VX	5	12.8	14.3	15	15.8	1	21.2	19	27.2	85	8.4	1200
SM4T18	RD	SM4T18C	UD	5	15.3	17.1	18	19.8	1	25.2	16	32.5	71	8.8	975
SM4T18A	RE	SM4T18CA	UE	5	15.3	17.1	18	18.9	1	25.2	16	32.5	71	8.8	975
SM4T22	RH	SM4T22C	UH	5	18.8	20.9	22	24.2	1	30.6	13	39.3	59	9.2	800
SM4T22A	RK	SM4T22CA	UK	5	18.8	20.9	22	23.1	1	30.6	13	39.3	59	9.2	800
SM4T24	RL	SM4T24C	UL	5	20.5	22.8	24	26.4	1	33.2	12	42.8	54	9.4	725
SM4T24A	RM	SM4T24CA	UM	5	20.5	22.8	24	25.2	1	33.2	12	42.8	54	9.4	725
SM4T27	RN	SM4T27C	UN	5	23.1	25.7	27	29.7	1	37.5	10.7	48.3	48	9.6	625
SM4T27A	RP	SM4T27CA	UP	5	23.1	25.7	27	28.4	1	37.5	10.7	48.3	48	9.6	625
SM4T30	RQ	SM4T30C	UQ	5	25.6	28.5	30	33	1	41.5	9.6	53.5	43	9.7	575
SM4T30A	RR	SM4T30C4	UR	5	25.6	28.5	30	31.5	1	41.5	9.6	53.5	43	9.7	575
SM4T33	RS	SM4T33C	US	5	28.2	31.4	33	36.3	1	45.7	8.8	59.0	39	9.8	510
SM4T33A	RT	SM4T33CA	UT	5	28.2	31.4	33	34.7	1	45.7	8.8	59.0	39	9.8	510
SM4T36	RU	SM4T36C	UU	5	30.8	34.2	36	39.6	1	49.9	8	64.3	36	9.9	480
SM4T36A	RV	SM4T36CA	UV	5	30.8	34.2	36	37.8	1	49.9	8	64.3	36	9.9	480
SM4T39	RW	SM4T39C	UW	5	33.3	37.1	39	42.9	1	53.9	7.4	69.7	33	10.0	450
SM4T39	RX	SM4T39	UX	5	33.3	37.1	39	41.0	1	53.9	7.4	69.7	33	10.0	450

TYPES				I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Uni directional	*	Bi directional	*	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
SM4T68	SN	SM4T68C	WN	5	58.1	64.6	68	74.8	1	92	4.3	121	19	10.4	270
SM4T68A	SP	SM4T68CA	WP	5	58.1	64.6	68	71.4	1	92	4.3	121	19	10.4	270
SM4T100	SW	SM4T100C	WW	5	85.5	95.0	100	110	1	137	2.9	178	13	10.6	200
SM4T100A	SX	SM4T100CA	WX	5	85.5	95.0	100	105	1	137	2.9	178	13	10.6	200
SM4T150	TH	SM4T150C	XH	5	128	143	150	165	1	207	2.0	265	9	10.8	145
SM4T150A	TK	SM4T150CA	XK	5	128	143	150	158	1	207	2.0	265	9	10.8	145
SM4T200	TS	SM4T200C	XS	5	171	190	200	220	1	274	1.5	353	6.5	10.8	120
SM4T200A	TT	SM4T200CA	XT	5	171	190	200	210	1	274	1.5	353	6.5	10.8	120
SM4T220	TU	SM4T220C	XU	5	188	209	220	242	1	328	1.4	388	6	10.8	110
SM4T220A	TV	SM4T220CA	XV	5	188	209	220	231	1	328	1.4	388	6	10.8	110

All parameters tested at 25 °C, except where indicated.

*** = Marking**

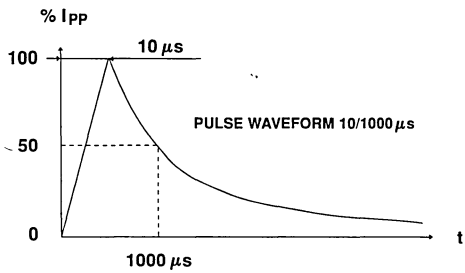
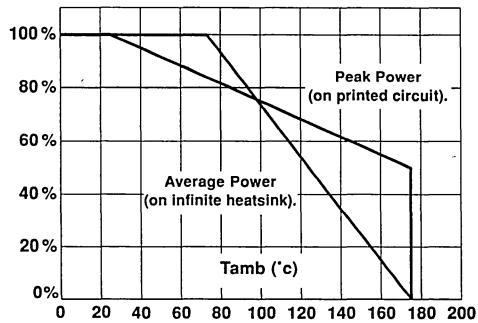


Figure 1: Power dissipation derating versus ambient temperature



Note 1 : For surges greater than the maximum values, the diode will present a short-circuit Anode - Cathode.

Note 2 : Pulse test: $T_P < 50$ ms.

Note 3 : $\Delta V_{BR} = \alpha T \cdot (Ta - 25) \cdot V_{BR(25°C)}$

Note 4 : VR = 0 V, F = 1 MHz. For bidirectional types, capacitance value is divided by 2.

Figure 2 : Peak pulse power versus exponential pulse duration.

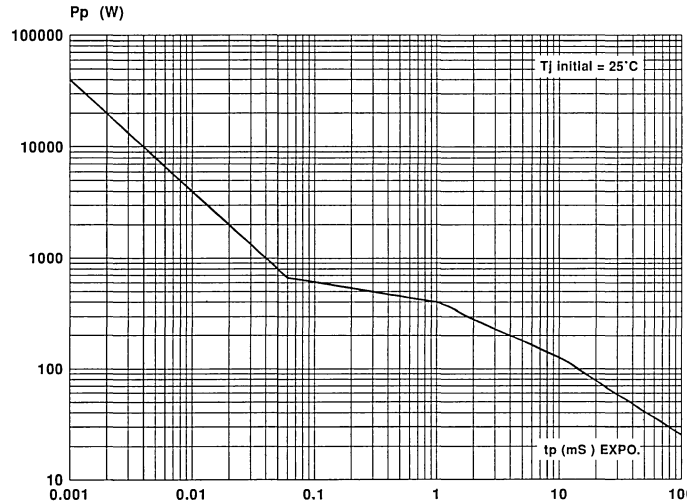
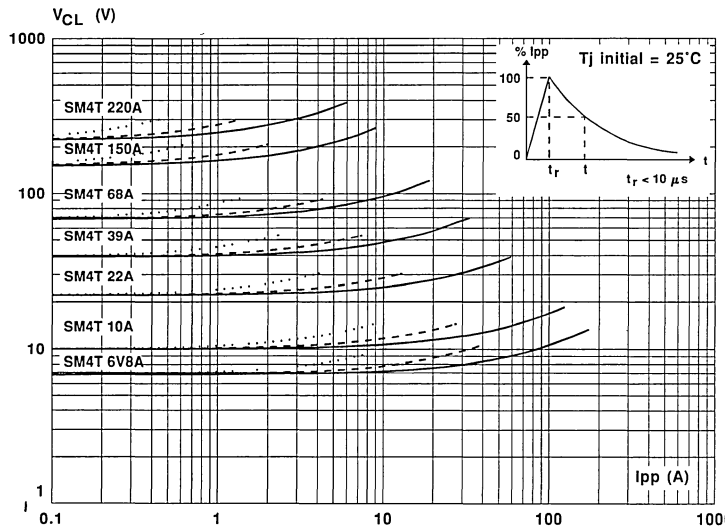


Figure 3 : Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs _____
t = 1 ms ----------
t =10 ms .....



Note : The curves of the figure 3 are specified for a junction temperature of 25 °C before surge.
The given results may be extrapolated for other junction temperatures by using the following formula :
$\Delta V_{(BR)} = \alpha T_{(V(BR))} * [T_a - 25] * V_{(BR)}$.
For intermediate voltages, extrapolate the given results.

Figure 4a : Capacitance versus reverse applied voltage for unidirectional types (typical values).

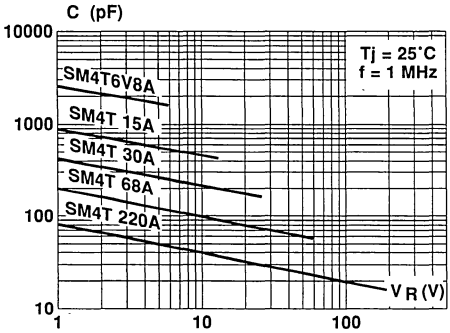


Figure 4b : Capacitance versus reverse applied voltage for bidirectional types (typical values)

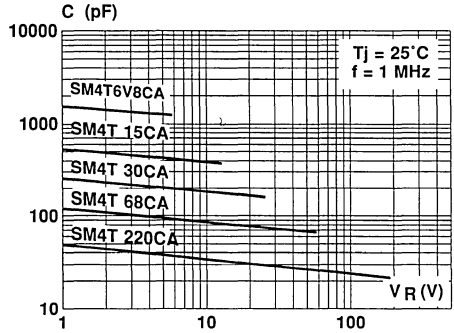


Figure 5 : Peak forward voltage drop versus peak forward current (typical values for unidirectional types).

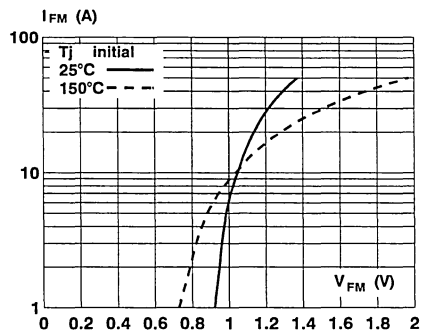
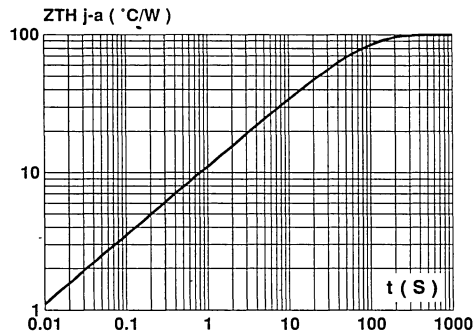
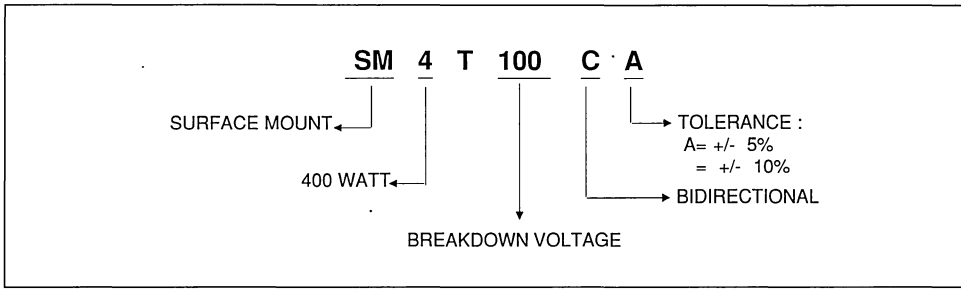


Figure 6 : Transient thermal impedance junction-ambient versus pulse duration. For a mounting on PC Board with standard footprint dimensions.



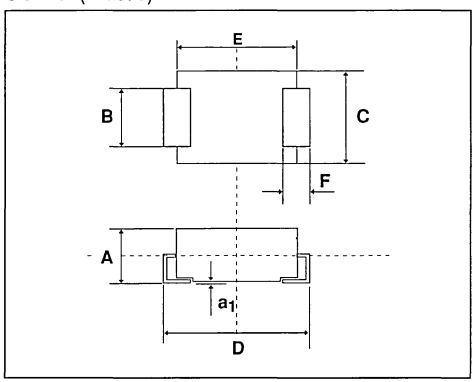
ORDER CODE



MARKING : Logo, Date Code, Type Code, Cathode Band (for unidirectional types only).

PACKAGE MECHANICAL DATA

SOD 6 (Plastic).

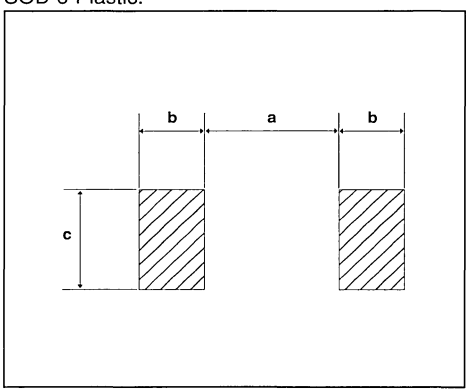


Ref	Millimeters		Inches	
	min	max	min	max
A	2.48	2.61	0.096	0.103
a1	0.10	0.20	0.004	0.008
B	1.96	2.11	0.077	0.083
C	3.65	3.93	0.143	0.155
D	5.39	5.59	0.212	0.220
E	4.15	4.30	0.163	0.170
F	1.00	1.27	0.039	0.050

Weight = 0.12 g.

FOOTPRINT DIMENSIONS (Millimeter).

SOD 6 Plastic.



Ref	Millimeters
a	2.75
b	1.52
c	2.30

Packaging : standard packaging is in film.

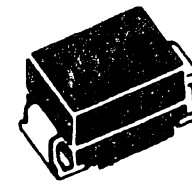
SGS-THOMSON MICROELECTRONICS

SM6T6V8,A/220,A
SM6T6V8C,CA/220C,CA

TRANSIL

FEATURES

- PEAK PULSE POWER= 600 W @ 1ms.
- BREAKDOWN VOLTAGE RANGE : From 6V8 to 220 V.
- UNI AND BIDIRECTIONAL TYPES.
- LOW CLAMPING FACTOR.
- FAST RESPONSE TIME: $T_{clamping}$: 1ps (0 V to V_{BR}).
- JEDEC REGISTRED.



SOD 6
(Plastic)

DESCRIPTION

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous reponse to transients makes them particularly suited to protect voltage sensitive devices such as MOS Technology and low voltage supplied IC's.

MECHANICAL CHARACTERISTICS

- Body marked with : Logo, Date Code, Type Code and Cathode Band (for unidirectional types only).
- Full compatibility with both gluing and paste soldering technologies.
- Excellent on board stability.
- Tinned copper leads.
- High temperature resistant resin.

ABSOLUTE RATINGS (limiting values)

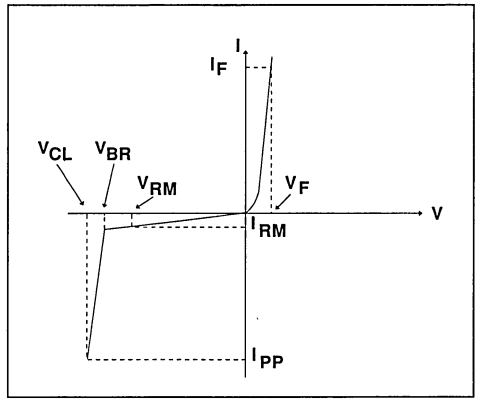
Symbol	Parameter		Value	Unit
P_p	Peak pulse power dissipation See note 1 and derating curve Fig 1.	Tamb = 25°C	600	W
P	Power dissipation on infinite heatsink See note 1 and derating curve Fig 1.	Tlead = 50°C	5	W
I_{FSM}	Non repetitive surge peak forward current. For unidirectional types.	Tamb = 25°C t =10 ms	100	A
T_{stg} T_j	Storage and junction temperature range		- 65 to + 175 150	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		260	°C

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction-leads on infinite heatsink	20	°C/W
R_{th} (j-a)	Junction to ambient. on printed circuit. With standard footprint dimensions.	100	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage.
V_{BR}	Breakdown voltage.
V_{CL}	Clamping voltage.
I_{RM}	Leakage current @ VRM.
I_{PP}	Surge current.
αT	Voltage temperature coefficient.
V_F	Forward Voltage drop V_F < 3.5V @ I_F = 50 A.

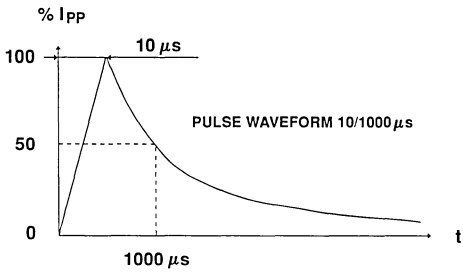


TYPES				I_{RM} @ V_{RM} max		V_{BR} @ I_R min	nom	max		V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
						note2									
Uni directional	*	Bi directional	*	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
SM6T6V8	DD	SM6T6V8C	LD	1000	5.8	6.45	6.8	7.48	10	10.5	57	13.4	298	5.7	4000
SM6T6V8A	DE	SM6T6V8CA	LE	1000	5.8	6.45	6.8	7.14	10	10.5	57	13.4	298	5.7	4000
SM6T7V5	DF	SM6T7V5C	LF	500	6.4	7.13	7.5	8.25	10	11.3	53	14.5	276	6.1	3700
SM6T7V5A	DG	SM6T7V5CA	LG	500	6.4	7.13	7.5	7.88	10	11.3	53	14.5	276	6.1	3700
SM6T10	DN	SM6T10C	LN	10	8.55	9.5	10	11	1	14.5	41	18.6	215	7.3	2800
SM6T10A	DP	SM6T10CA	LP	10	8.55	9.5	10	10.5	1	14.5	41	18.6	215	7.3	2800
SM6T12	DS	SM6T12C	LS	5	10.2	11.4	12	13.2	1	16.7	36	21.7	184	7.8	2300
SM6T12A	DT	SM6T12CA	LT	5	10.2	11.4	12	12.6	1	16.7	36	21.7	184	7.8	2300
SM6T15	DW	SM6T15C	LW	5	12.8	14.3	15	16.5	1	21.2	28	27.2	147	8.4	1900
SM6T15A	DX	SM6T15CA	LX	5	12.8	14.3	15	15.8	1	21.2	28	27.2	147	8.4	1900
SM6T18	ED	SM6T18C	MD	5	15.3	17.1	18	19.8	1	25.2	24	32.5	123	8.8	1600
SM6T18A	EE	SM6T18CA	ME	5	15.3	17.1	18	18.9	1	25.2	24	32.5	123	8.8	1600
SM6T22	EH	SM6T22C	MH	5	18.8	20.9	22	24.2	1	30.6	20	39.3	102	9.2	1350
SM6T22A	EK	SM6T22CA	MK	5	18.8	20.9	22	23.1	1	30.6	20	39.3	102	9.2	1350
SM6T24	EL	SM6T24C	ML	5	20.5	22.8	24	26.4	1	33.2	18	42.8	93	9.4	1250
SM6T24A	EM	SM6T24CA	MM	5	20.5	22.8	24	25.2	1	33.2	18	42.8	93	9.4	1250
SM6T27	EN	SM6T27C	MN	5	23.1	25.7	27	29.7	1	37.5	16	48.3	83	9.6	1150
SM6T27A	EP	SM6T27CA	MP	5	23.1	25.7	27	28.4	1	37.5	16	48.3	83	9.6	1150
SM6T30	EQ	SM6T30C	MQ	5	25.6	28.5	30	33	1	41.5	14.5	53.5	75	9.7	1075
SM6T30A	ER	SM6T30CA	MR	5	25.6	28.5	30	31.5	1	41.5	14.5	53.5	75	9.7	1075
SM6T33	ES	SM6T33C	MS	5	28.2	31.4	33	36.3	1	45.7	13.1	59.0	68	9.8	1000
SM6T33A	ET	SM6T33CA	MT	5	28.2	31.4	33	34.7	1	45.7	13.1	59.0	68	9.8	1000
SM6T36	EU	SM6T36C	MU	5	30.8	34.2	36	39.6	1	49.9	12	64.3	62	9.9	950
SM6T36A	EV	SM6T36CA	MV	5	30.8	34.2	36	37.8	1	49.9	12	64.3	62	9.9	950
SM6T39	EW	SM6T39C	MW	5	33.3	37.1	39	42.9	1	53.9	11.1	69.7	57	10.0	900
SM6T39	EX	SM6T39	MX	5	33.3	37.1	39	41.0	1	53.9	11.1	69.7	57	10.0	900

TYPES				I_{RM} @ V_{RM}		V_{BR} @ I_R				V_{CL} @ I_{PP}		V_{CL} @ I_{PP}		αT	C
				max		min	nom	max		max		max		max	typ
							note2			10/1000µs		8/20µs		note3	note4
Uni directional	*	Bi directional	*	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
SM6T68	FP	SM6T68C	NP	5	58.1	64.6	68	74.8	1	92	6.5	121	33	10.4	625
SM6T68A	FQ	SM6T68CA	NQ	5	58.1	64.6	68	71.4	1	92	6.5	121	33	10.4	625
SM6T100	FX	SM6T100C	NX	5	85.5	95.0	100	110	1	137	4.4	178	22.5	10.6	500
SM6T100A	FY	SM6T100CA	NY	5	85.5	95.0	100	105	1	137	4.4	178	22.5	10.6	500
SM6T150	GK	SM6T150C	OK	5	128	143	150	165	1	207	2.9	265	15	10.8	400
SM6T150A	GL	SM6T150CA	OL	5	128	143	150	158	1	207	2.9	265	15	10.8	400
SM6T200	GT	SM6T200C	OT	5	171	190	200	220	1	274	2.2	353	11.3	10.8	350
SM6T200A	GU	SM6T200CA	OU	5	171	190	200	210	1	274	2.2	353	11.3	10.8	350
SM6T220	GV	SM6T220C	OV	5	188	209	220	242	1	328	2	388	10.3	10.8	330
SM6T220A	GW	SM6T220CA	OW	5	188	209	220	231	1	328	2	388	10.3	10.8	330

All parameters tested at 25 °C, except where indicated.

*** = Marking**



Note 1 : For surges greater than the maximum values, the diode will present a short-circuit Anode - Cathode.

Note 2 : Pulse test: $T_P < 50$ ms

Note 3 : $\Delta V_{BR} = \alpha T \cdot (Ta - 25) \cdot V_{BR(25°C)}$.

Note 4 : VR = 0 V, F = 1 MHz For bidirectional types, capacitance value is divided by 2.

Figure 1: Power dissipation derating versus ambient temperature

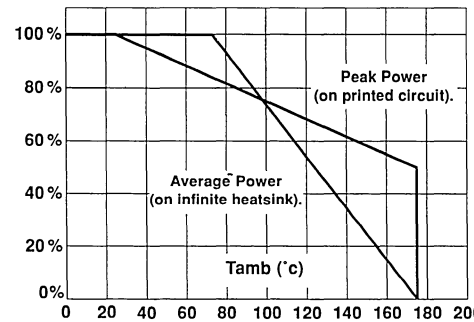


Figure 2 : Peak pulse power versus exponential pulse duration.

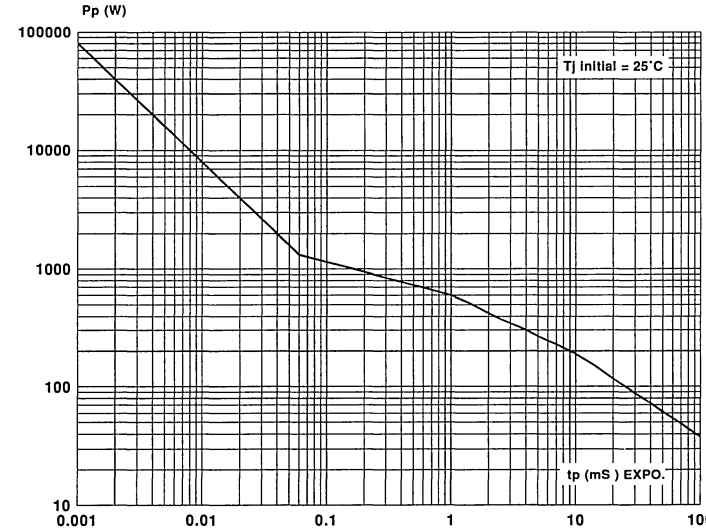
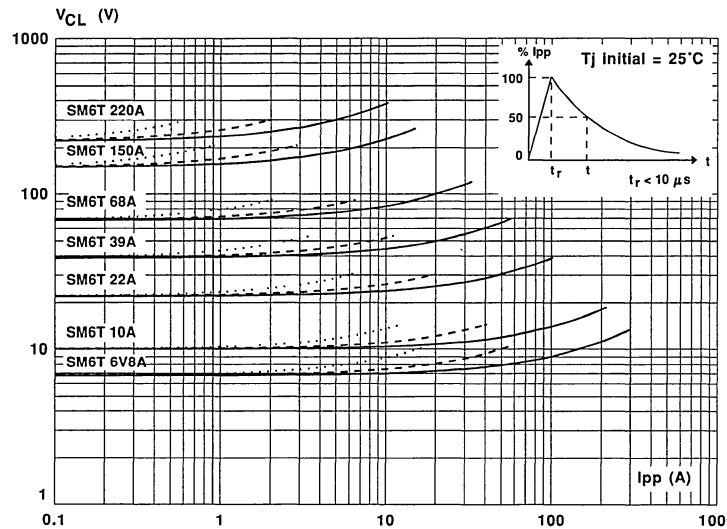


Figure 3 : Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs _____
t = 1 ms ----------
t =10 ms .....



Note : The curves of the figure 3 are specified for a junction temperature of 25 °C before surge.
The given results may be extrapolated for other junction temperatures by using the following formula :
$\Delta V_{(BR)} = \alpha T_{(V(BR))} \cdot [T_a - 25] \cdot V_{(BR)}$.
For intermediate voltages, extrapolate the given results.

Figure 4a : Capacitance versus reverse applied voltage for unidirectional types (typical values).

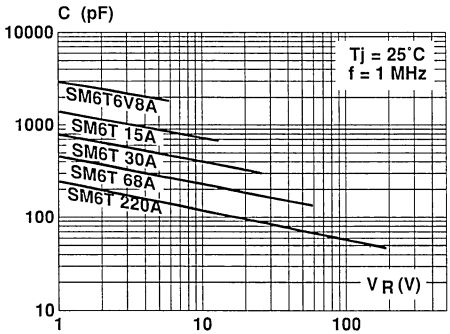


Figure 4b : Capacitance versus reverse applied voltage for bidirectional types (typical values)

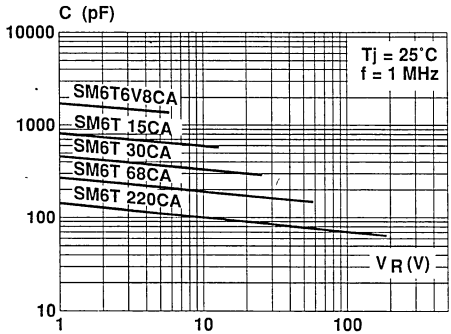


Figure 5 : Peak forward voltage drop versus peak forward current (typical values for unidirectional types).

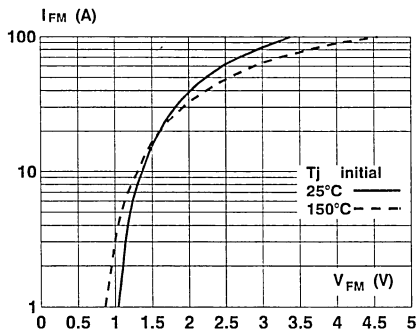
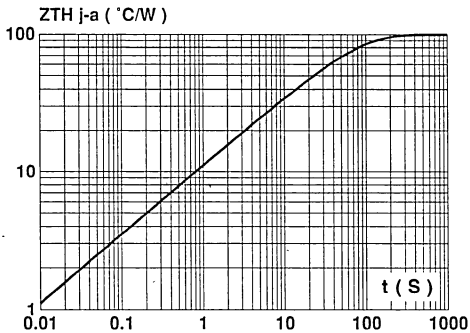
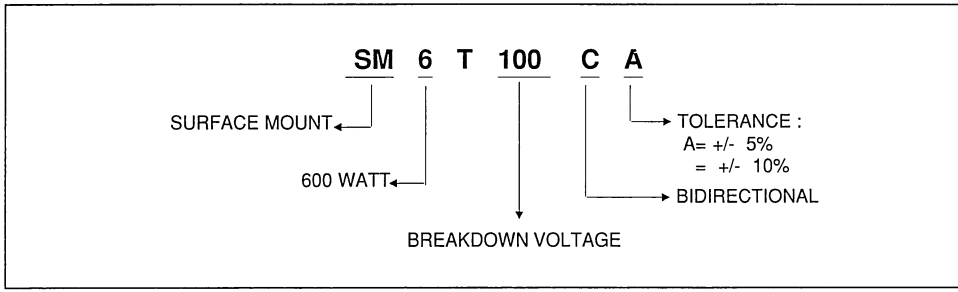


Figure 6 : Transient thermal impedance junction-ambient versus pulse duration. For a mounting on PC Board with standard footprint dimensions.



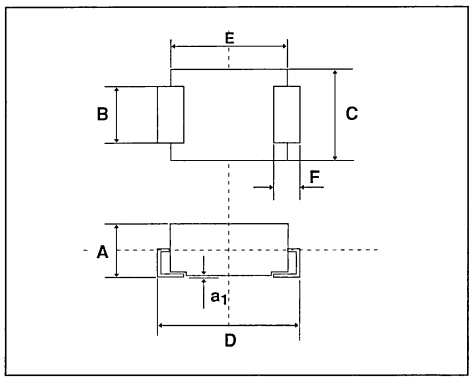
ORDER CODE



MARKING : Logo, Date Code, Type Code, Cathode Band (for unidirectional types only).

PACKAGE MECHANICAL DATA

SOD 6 (Plastic).



Ref	Millimeters		Inches	
	min	max	min	max
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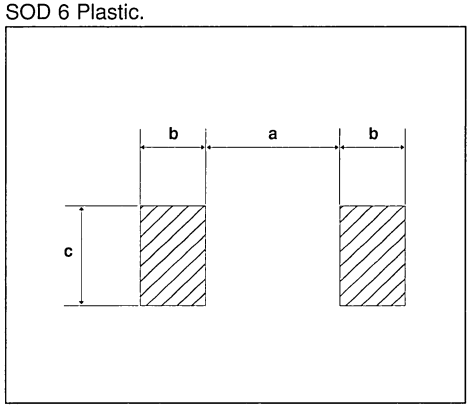
a1	0.10	0.20	0.004	0.008
B	1.96	2.11	0.077	0.083
C	3.65	3.93	0.143	0.155
D	5.39	5.59	0.212	0.220
E	4.15	4.30	0.163	0.170
F	1.00	1.27	0.039	0.050

Weight = 0.12 g.

FOOTPRINT DIMENSIONS (Millimeter).

SOD 6 Plastic.



Ref	Millimeters
a	2.75
b	1.52
c	2.30

Packaging : standard packaging is in film.

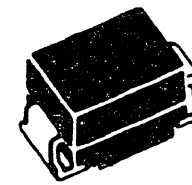
SGS-THOMSON MICROELECTRONICS

SM15T6V8,A/220,A
SM15T6V8C,CA/220C,CA

TRANSIL

FEATURES

- PEAK PULSE POWER= 1500 W @ 1ms.
- BREAKDOWN VOLTAGE RANGE : From 6V8 to 220 V.
- UNI AND BIDIRECTIONAL TYPES.
- LOW CLAMPING FACTOR.
- FAST RESPONSE TIME: Tclamping : 1ps (0 V to VBR).



SOD 15
(Plastic)

DESCRIPTION

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous reponse to transients makes them particularly suited to protect voltage sensitive devices such as MOS Technology and low voltage supplied IC's.

MECHANICAL CHARACTERISTICS

- Body marked with : Logo, Date Code, Type Code, and Cathode Band (for unidirectional types only).
- Full compatibility with both gluing and paste soldering technologies.
- Excellent on board stability.
- Tinned copper leads.
- High temperature resistant resin.

ABSOLUTE RATINGS (limiting values)

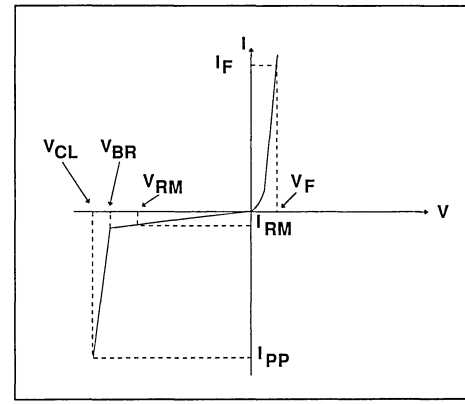
Symbol	Parameter		Value	Unit
P_p	Peak pulse power dissipation See note 1 and derating curve Fig 1.	Tamb = 25°C	1500	W
P	Power dissipation on infinite heatsink See note 1 and derating curve Fig 1.	Tlead = 50°C	10	W
I_{FSM}	Non repetitive surge peak forward current. For unidirectional types.	Tamb = 25°C t =10 ms	250	A
T_{stg} T_j	Storage and junction temperature range		- 65 to + 175 150	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		260	°C

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction-leads on infinite heatsink	10	°C/W
R_{th} (j-a)	Junction to ambient. on printed circuit. With standard footprint dimensions.	75	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage.
V_{BR}	Breakdown voltage.
V_{CL}	Clamping voltage.
I_{RM}	Leakage current @ VRM.
I_{PP}	Surge current.
αT	Voltage temperature coefficient.
V_F	Forward Voltage drop V_F < 3.5V @ I_F = 100 A.



TYPES		I_{RM} @ V_{RM} max		V_{BR} @ I_R min nom max note2				V_{CL} @ I_{PP} max 10/1000µs		V_{CL} @ I_{PP} max 8/20µs		αT max note3	C typ note4
Uni directional	Bi directional	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(PF)
SM15T6V8	SM15T6V8C	1000	5.8	6.45	6.8	7.48	10	10.5	143	13.4	746	5.7	9500
SM15T6V8A	SM15T6V8CA	1000	5.8	6.45	6.8	7.14	10	10.5	143	13.4	746	5.7	9500
SM15T7V5	SM15T7V5C	500	6.4	7.13	7.5	8.25	10	11.3	132	14.5	690	6.1	8500
SM15T7V5A	SM15T7V5CA	500	6.4	7.13	7.5	7.88	10	11.3	132	14.5	690	6.1	8500
SM15T10	SM15T10C	10	8.55	9.5	10	11.0	1	14.5	103	18.6	538	7.3	7000
SM15T10A	SM15T10CA	10	8.55	9.5	10	10.5	1	14.5	103	18.6	538	7.3	7000
SM15T12	SM15T12C	5	10.2	11.4	12	13.2	1	16.7	90	21.7	461	7.8	6000
SM15T12A	SM15T12CA	5	10.2	11.4	12	12.6	1	16.7	90	21.7	461	7.8	6000
SM15T15	SM15T15C	5	12.8	14.3	15	16.5	1	21.2	71	27.2	368	8.4	5000
SM15T15A	SM15T15CA	5	12.8	14.3	15	15.8	1	21.2	71	27.2	368	8.4	5000
SM15T18	SM15T18C	5	15.3	17.1	18	19.8	1	25.2	59.5	32.5	308	8.8	4300
SM15T18A	SM15T18CA	5	15.3	17.1	18	18.9	1	25.2	59.5	32.5	308	8.8	4300
SM15T22	SM15T22C	5	18.8	20.9	22	24.2	1	30.6	49	39.3	254	9.2	3700
SM15T22A	SM15T22CA	5	18.8	20.9	22	23.1	1	30.6	49	39.3	254	9.2	3700
SM15T24	SM15T24C	5	20.5	22.8	24	26.4	1	33.2	45	42.8	234	9.4	3500
SM15T24A	SM15T24CA	5	20.5	22.8	24	25.2	1	33.2	45	42.8	234	9.4	3500
SM15T27	SM15T27C	5	23.1	25.7	27	29.7	1	37.5	40	48.3	207	9.6	3200
SM15T27A	SM15T27CA	5	23.1	25.7	27	28.4	1	37.5	40	48.3	207	9.6	3200
SM15T30	SM15T30C	5	25.6	28.5	30	33.0	1	41.5	36	53.5	187	9.7	2900
SM15T30A	SM15T30CA	5	25.6	28.5	30	31.5	1	41.5	36	53.5	187	9.7	2900
SM15T33	SM15T33C	5	28.2	31.4	33	36.3	1	45.7	33	59.0	169	9.8	2700
SM15T33A	SM15T33CA	5	28.2	31.4	33	34.7	1	45.7	33	59.0	169	9.8	2700
SM15T36	SM15T36C	5	30.8	34.2	36	39.6	1	49.9	30	64.3	156	9.9	2500
SM15T36A	SM15T36CA	5	30.8	34.2	36	37.8	1	49.9	30	64.3	156	9.9	2500
SM15T39	SM15T39C	5	33.3	37.1	39	42.9	1	53.9	28	69.7	143	10.0	2400
SM15T39	SM15T39	5	33.3	37.1	39	41.0	1	53.9	28	69.7	143	10.0	2400

TYPES		I_{RM} @ V_{RM}		V_{BR} @ I_R				V_{CL} @ I_{PP}		V_{CL} @ I_{PP}		αT	C
		max		min	nom	max		max		max		max	typ
						note2		10/1000µs		8/20µs		note3	note4
Uni directional	Bi directional	µA	V	V	V	V	mA	V	A	V	A	10^{-4}/°C	(pF)
SM15T68	SM15T68C	5	58.1	64.6	68	74.8	1	92	16.3	121	83	10.4	1550
SM15T68A	SM15T68CA	5	58.1	64.6	68	71.4	1	92	16.3	121	83	10.4	1550
SM15T100	SM15T100C	5	85.5	95.0	100	110	1	137	11	178	56	10.6	1150
SM15T100A	SM15T100CA	5	85.5	95.0	100	105	1	137	11	178	56	10.6	1150
SM15T150	SM15T150C	5	128	143	150	165	1	207	7.2	265	38	10.8	850
SM15T150A	SM15T150CA	5	128	143	150	158	1	207	7.2	265	38	10.8	850
SM15T200	SM15T200C	5	171	190	200	220	1	274	5.5	353	28	10.8	675
SM15T200A	SM15T200CA	5	171	190	200	210	1	274	5.5	353	28	10.8	675
SM15T220	SM15T220C	5	188	209	220	242	1	328	4.6	388	26	10.8	625
SM15T220A	SM15T220CA	5	188	209	220	231	1	328	4.6	388	26	10.8	625

All parameters tested at 25 °C, except where indicated.

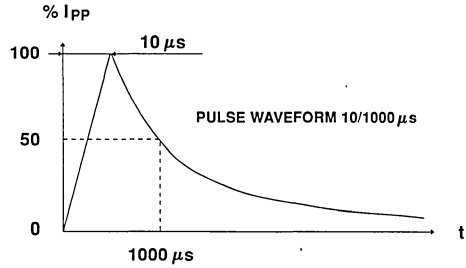
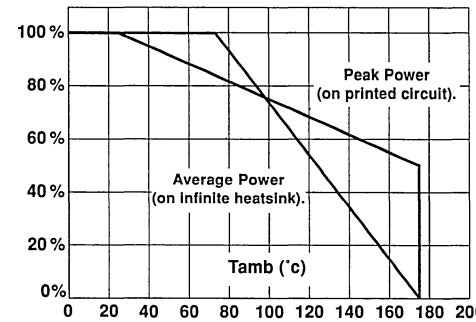


Figure 1: Power dissipation derating versus ambient temperature



Note 1 : - For surges greater than the maximum values, the diode will present a short-circuit Anode - Cathode.
Note 2 : - Pulse test: $T_P < 50$ ms.
Note 3 : - $\Delta V_{BR} = \alpha T \cdot (Ta - 25) \cdot V_{BR(25°C)}$.
Note 4 : - VR = 0 V, F = 1 MHz. For bidirectional types, capacitance value is divided by 2.

TYPES		TYPES		TYPES		TYPES	
Unidirectional	Marking	Bidirectional	Marking	Unidirectional	Marking	Bidirectional	Marking
SM15T6V8	MDD	SM15T6V8C	BDD	SM15T30	MEQ	SM15T30C	BEQ
SM15T6V8A	MDE	SM15T6V8CA	BDE	SM15T30A	MER	SM15T30CA	BER
SM15T7V5	MDF	SM15T7V5C	BDF	SM15T33	MES	SM15T33C	BES
SM15T7V5A	MDG	SM15T7V5CA	BDG	SM15T33A	MET	SM15T33CA	BET
SM15T10	MDN	SM15T10C	BDN	SM15T36	MEU	SM15T36C	BEU
SM15T10A	MDP	SM15T10CA	BDP	SM15T36A	MEV	SM15T36CA	BEV
SM15T12	MDS	SM15T12C	BDS	SM15T39	MEW	SM15T39C	BEW
SM15T12A	MDT	SM15T12CA	BDT	SM15T39A	MEX	SM15T39CA	BEX
SM15T15	MDW	SM15T15C	BDW	SM15T68	MFN	SM15T68C	BFN
SM15T15A	MDX	SM15T15CA	BDX	SM15T68A	MFP	SM15T68CA	BFP
SM15T18	MED	SM15T18C	BED	SM15T100	MFW	SM15T100C	BFW
SM15T18A	MEE	SM15T18CA	BEE	SM15T100A	MFX	SM15T100CA	BFX
SM15T22	MEH	SM15T22C	BEH	SM15T150	MGH	SM15T150C	BGH
SM15T22A	MEK	SM15T22CA	BEK	SM15T150A	MGK	SM15T150CA	BGK
SM15T24	MEL	SM15T24C	BEL	SM15T200	MGU	SM15T200C	BGU
SM15T24A	MEM	SM15T24CA	BEM	SM15T200A	MGV	SM15T200CA	BGV
SM15T27	MEN	SM15T27C	BEN	SM15T220	MGW	SM15T220C	BGW
SM15T27A	MEP	SM15T27CA	BEP	SM15T220A	MGVX	SM15T220CA	BGX

Figure 2 : Peak pulse power versus exponential pulse duration.

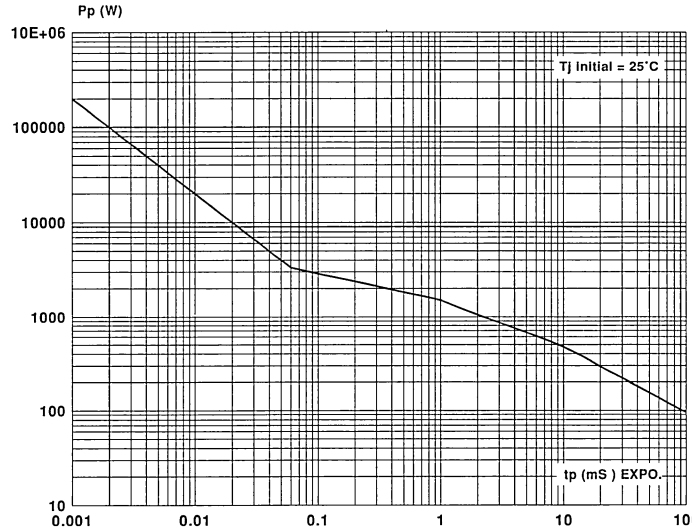
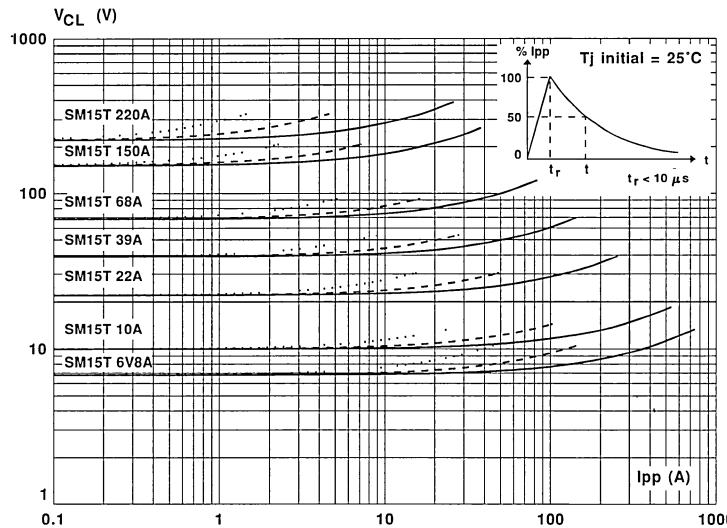


Figure 3 : Clamping voltage versus peak pulse current.
exponential waveform t = 20 µs _____
t = 1 ms ----------
t =10 ms .....



Note : The curves of the figure 3 are specified for a junction temperature of 25 °C before surge.
The given results may be extrapolated for other junction temperatures by using the following formula :
$\Delta V_{(BR)} = \alpha T_{(V(BR))} * [T_a - 25] * V_{(BR)}$.
For intermediate voltages, extrapolate the given results.

Figure 4a : Capacitance versus reverse applied voltage for unidirectional types (typical values).

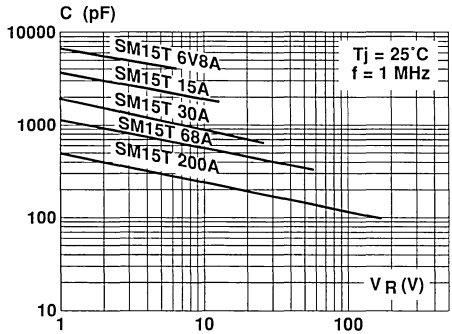


Figure 4b : Capacitance versus reverse applied voltage for bidirectional types (typical values)

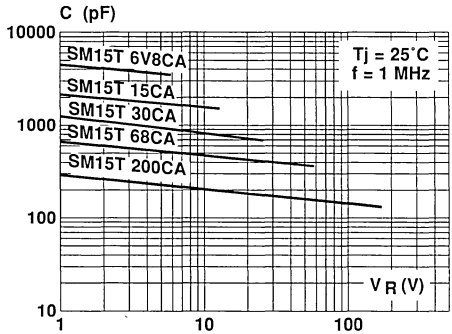


Figure 5 : Peak forward voltage drop versus peak forward current (typical values for unidirectional types).

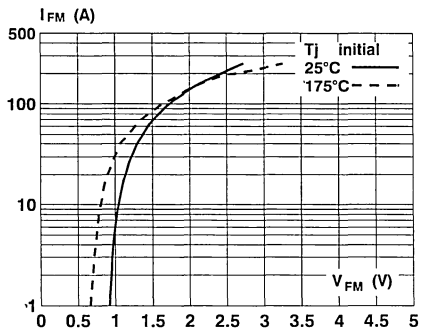
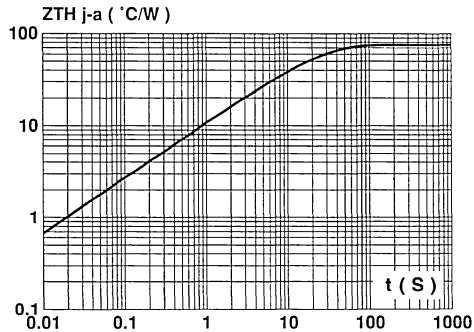
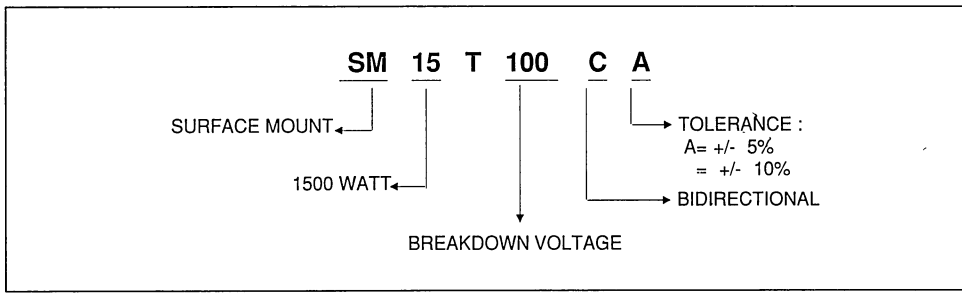


Figure 6 : Transient thermal impedance junction-ambient versus pulse duration. For a mounting on PC Board with standard footprint dimensions.



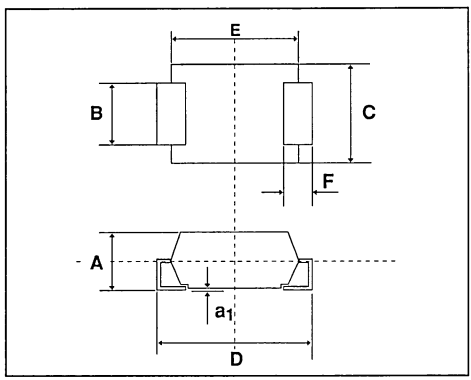
ORDER CODE



MARKING : Logo, Date Code, Type Code, Cathode Band (for unidirectional types only).

PACKAGE MECHANICAL DATA

SOD 15 (Plastic).

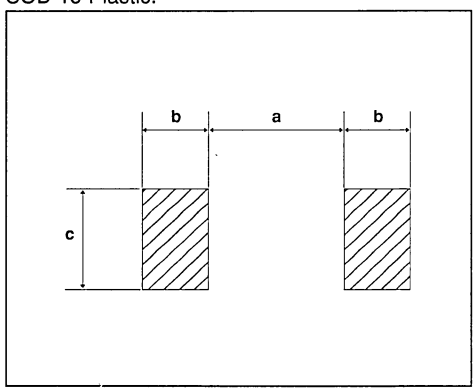


Ref	Millimeters		Inches	
	min	max	min	max
A	2.5	3.1	0.098	0.122
a1	-	0.2	-	0.008
B	2.9	3.1	0.114	0.122
C	4.8	5.2	0.190	0.200
D	7.6	8.0	0.300	0.315
E	6.3	6.6	0.248	0.259
F	1.3	1.7	0.051	0.067

Weight = 0.25 g.

FOOTPRINT DIMENSIONS (Millimeter).

SOD 15 Plastic.



Ref	Millimeters
a	4.2
b	2
c	3.3

Packaging : standard packaging is in film.

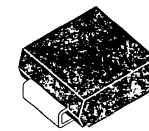
SGS-THOMSON MICROELECTRONICS

SMA100 SERIES

SURFACE MOUNT SURGE ARRESTORS

FEATURES

- SOLID STATE SURGE ARRESTOR
- VOLTAGE RANGE = 200 V TO 265 V
- TIGHT VOLTAGE TOLERANCE
- FAST RESPONSE TIME
- VERY LOW AND STABLE LEAKAGE CURRENT
- REPETITIVE SURGE CAPABILITY Ipp = 100 A, 10/1000 µs
- FAIL-SAFE WHEN DESTROYED



SOD 15

DESCRIPTION

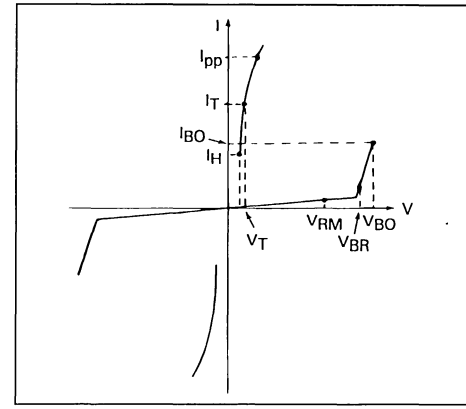
Bidirectional device providing long service life used for primary protection in telecom equipments.
If destroyed the component will continue to guarantee protection with a permanent short circuit, i.e. the "fail safe criterian " . This behaviour will also allow an easy failure detection on the line.

ABSOLUTE RATINGS (limiting values) - Ta = 25°C

Symbol	Parameter		Value	Unit
I_{PP}	Peak Pulse Current.	10/1000 µs	100	A
		8/20 µs	200	A
	Fail Safe Criterian.	8/20 µs	10	kA
I_{TSM}	Non Repetitive Surge Peak on-state Current One cycle.	60Hz	30	A
		50Hz	25	A
	Non Repetitive Surge Peak on-state Current F = 50 Hz.	1s	14	A
		2s	10	A
dv/dt	Critical Rate of Rise of on-state Voltage.	67% V_{BR}	10	kV/µs
Top	Operating ambient temperature range		- 20 to + 80	°C
T_L	Maximum Lead Temperature to Soldering During 10 s.		250	°C

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off Voltage
V_{BR}	Breakdown Voltage
V_{BO}	Breakover Voltage
I_H	Holding Current
V_T	On-state Voltage
I_{BO}	Breakover Current



Types	I_{RM} @ V_{RM} max		V_{BR} @ I_R min.		V_{BO} max. note 1	VBO max. note 2	VBO max. note 3	I_{BO} min. note 1	I_H min. note 4	V_T typ. note 5	C max. note 6
	(µA)	(V)	(V)	(mA)	(V)	(V)	(V)	(mA)	(mA)	(V)	pF
SMA100-230	10	170	200	1	265	350	350	100	260	3.5	200
SMA100-300	10	225	265	1	400	400	400	100	260	3.5	200

All parameters tested at 25°C, except where indicated.

Note 1 : See the reference test circuit for IBO and VBO parameters
Note 2 : V_{RISE} = 100V/µs.
Note 3 : V_{RISE} = 1KV/µs, di/dt < 10A/µs, I_{PP}= 10A
Note 4 : See functional holding current test circuit.
Note 5 : Square pulse, T_P = 500 µs, I_T = 5 A.
Note 6 : V_R = 0 V, F = 1 MHz..

ORDER CODE

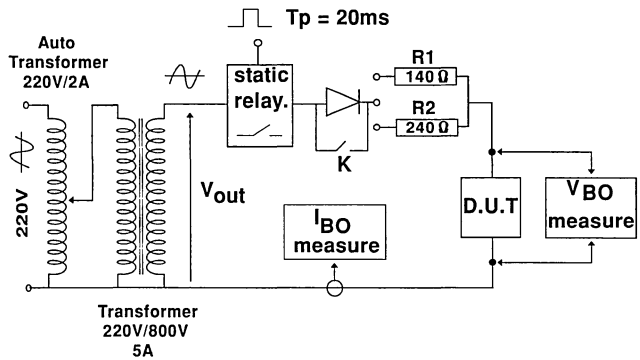
SMA 100 - 300

Surface Mount Arrestor

100 A

V_{BR}: voltage range

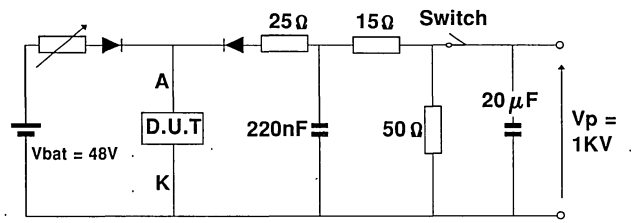
REFERENCE TEST CIRCUIT FOR I_{BO} and V_{BO} parameters :



TEST PROCEDURE :

- Pulse Test duration (Tp = 20ms):
  - For Bidirectional devices = Switch K is closed
  - For Unidirectional devices = Switch K is open.
- V_{OUT} Selection
  - Device with $V_{BR} \leq 150$ Volt
    - $V_{OUT} = 250\ V_{RMS}$, $R_1 = 140\ \Omega$.
  - Device with $V_{BR} \geq 150$ Volt
    - $V_{OUT} = 480\ V_{RMS}$, $R_2 = 240\ \Omega$.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT = GO - NOGO TEST.



Surge Generator
10/700 µsec
Vp =1KV / Ipp = 25A

This is a functional test circuit which performs a GO-NOGO test on the holding current I_H.

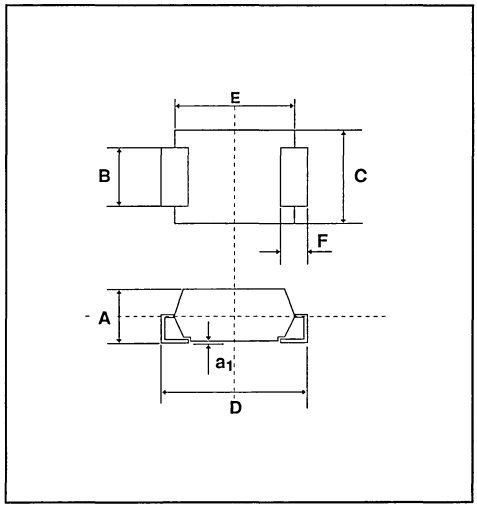
TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.

2) Fire the D.U.T with a surge Current : Ipp = 25A , 10/700 µs.

3) The D.U.T will come back to the OFF-State within a duration of 50 ms max.

MECHANICAL DATA
SOD 15 (Plastic)

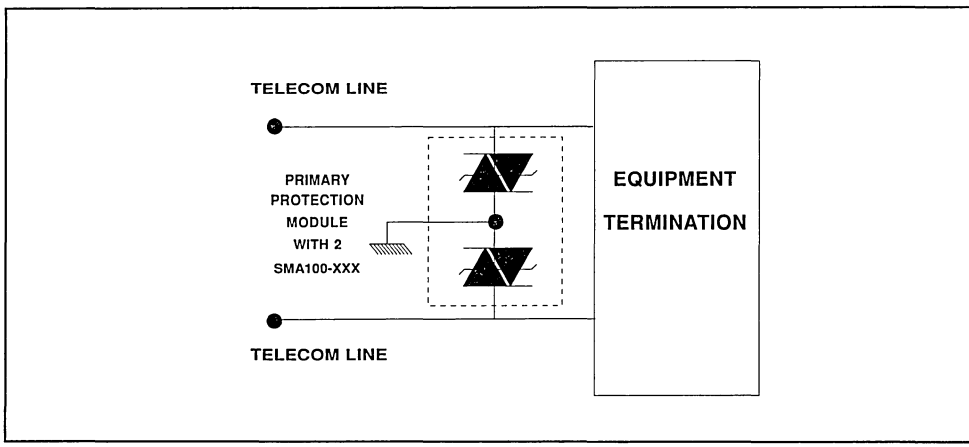


Ref	Millimeters		Inches	
	min	max	min	max
A	2.5	3.1	0.098	0.122
a_1	-	0.2	-	0.008
B	2.9	3.1	0.114	0.122
C	4.8	5.2	0.190	0.200
D	7.6	8.0	0.300	0.315

MARKING : Logo, date code, device code.

Type	Device code
SMA100-230 SMA100-300	W37 W45

APPLICATION DIAGRAM



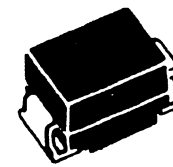
SGS-THOMSON MICROELECTRONICS

SMTHBT200

TRISIL FOR LINE CARD PROTECTION

FEATURES

- BIDIRECTIONAL CROWBAR PROTECTION.
- PEAK PULSE CURRENT :
  - I_{PP} = 75 A, 10/1000 µs.
- HOLDING CURRENT = 150 mA min
- BREAKDOWN VOLTAGE = 200 V min.
- BREAKOVER VOLTAGE = 290 V max.

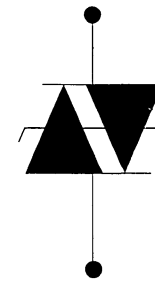


SOD 15
(Plastic)

DESCRIPTION

This protection device has been especially designed to protect subscriber line cards using SLICS without integrated ring generators. The SMTHBT200 device protects ring generator relays against transient overvoltages.

SCHEMATIC DIAGRAM

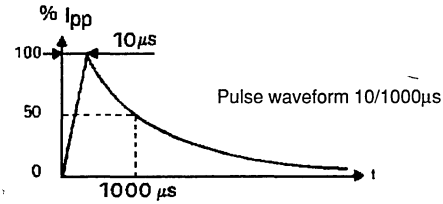


IN ACCORDANCE WITH FOLLOWING STANDARDS :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

ABSOLUTE RATINGS (limiting values) (-40°C ≤ T_{amb} ≤ + 85°C)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current	10/1000 µs 8/20 µs	75 150	A
I_{TSM}	Non repetitive surge peak on-state current	tp = 20 ms	30	A
di/dt	Critical rate of rise of on-state current	Non repetitive	100	A/µs
dv/dt	Critical rate of rise of off-state voltage	67% V_{BR}	5	KV/µs
T_{stg} T_j	Storage and operating junction temperature range		- 40 to + 150 150	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		260	°C

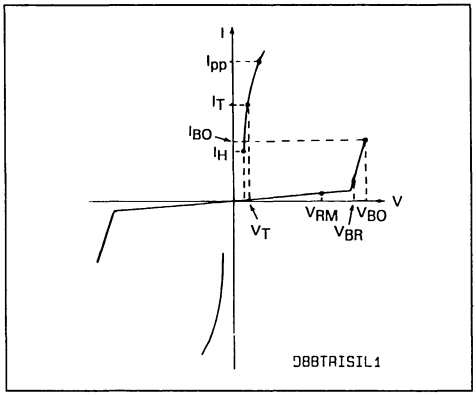


THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction to leads.	10	°C/W
R_{th} (j-a)	Junction-to-ambient.	75	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{BO}	Breakover voltage
I_H	Holding current
V_T	On-state voltage
I_{BO}	Breakover current
I_{PP}	Peak pulse current

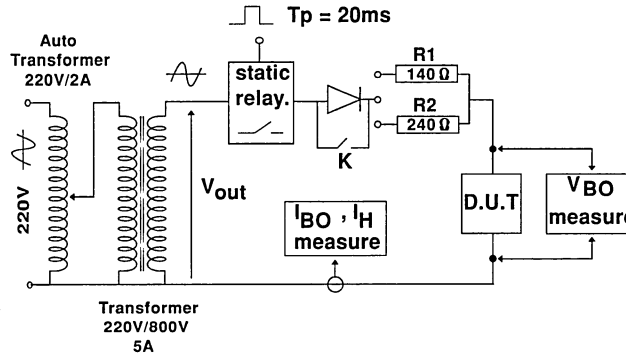


TYPE	I_{RM} @ V_{RM} max		V_{BR} @ I_R min		V_{BO} @ I_{BO} max			I_H min note1	V_T max note2	C max note3
	µA	V	V	mA	V	mA	mA	mA	V	pF
SMTHBT200	10	180	200	1	290	150	800	150	8	200

All parameters tested at 25°C, except where indicated

Note 1 : See the reference test circuit for I_H, I_{BO} and V_{BO} parameters.
Note 2 : Square pulse Tp = 500 µs - I_T = 5A.
Note 3 : V_R = 1V, F = 1MHz.

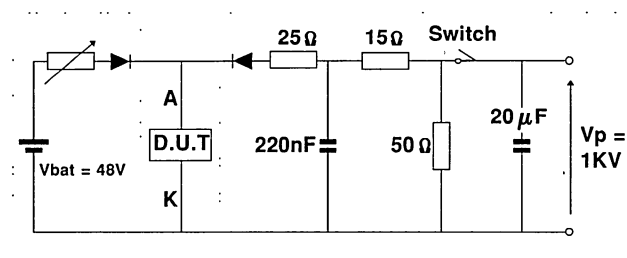
REFERENCE TEST CIRCUIT FOR I_H, I_{BO} and V_{BO} parameters :



TEST PROCEDURE :

- Pulse Test duration (Tp = 20ms):
  - For Bidirectional devices = Switch K is closed
  - For Unidirectional devices = Switch K is open.
- V_{OUT} Selection
  - Device with $V_{BR} \leq 150$ Volt
    - $V_{OUT} = 250\ V_{RMS}$, $R_1 = 140\ \Omega$.
  - Device with $V_{BR} \geq 150$ Volt
    - $V_{OUT} = 480\ V_{RMS}$, $R_2 = 240\ \Omega$.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT =GO - NOGO TEST.



Surge Generator
10/700 µsec
Vp =1KV / Ipp = 25A

This is a GO-NOGO Test which allows to confirm the holding current (I_H) level in a functional test circuit. This test can be performed if the reference test circuit can't be implemented.

TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.
2) Fire the D.U.T with a surge Current : Ipp = 25A , 10/700 µs.
3) The D.U.T will come back to the OFF-State within a duration of 50 ms max.

Figure 1 : Relative variation of holding current versus junction temperature.

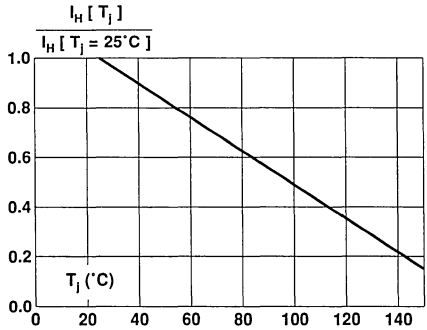


Figure 2 : Non repetitive surge peak on state current versus number of cycles (1 cycle = 20

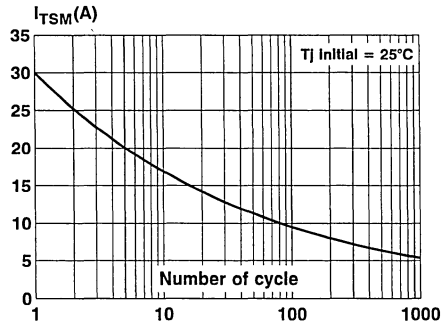


Figure 3 : Peak on state voltage versus peak on state current (typical values).

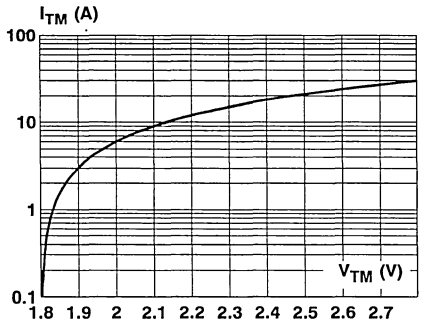
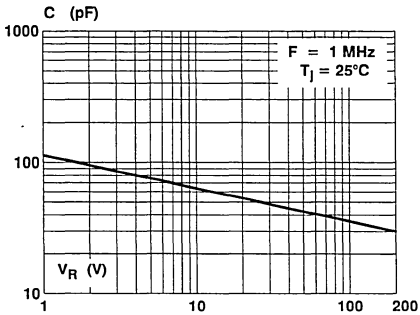
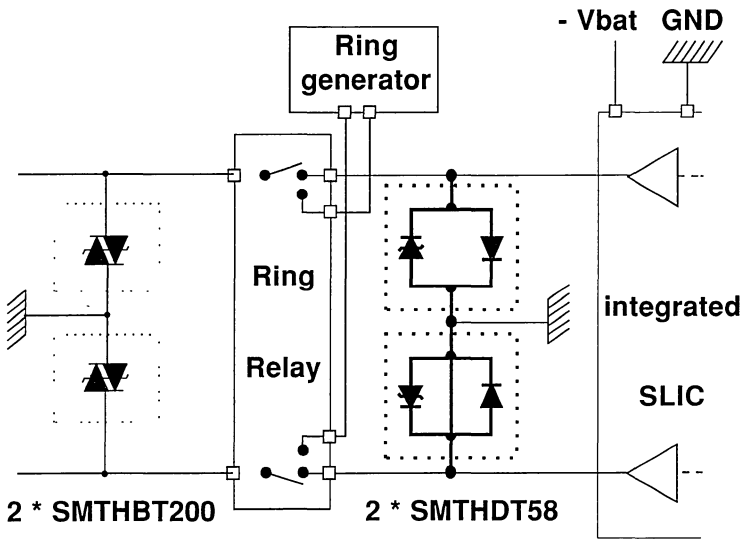


Figure 5 : Capacitance versus reverse applied voltage (typical values).

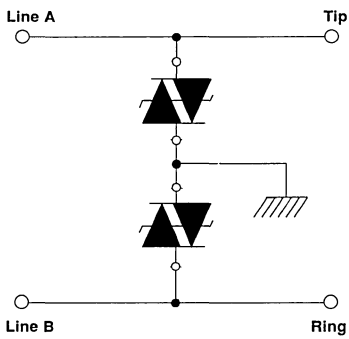


APPLICATION CIRCUIT

Typical line card protection concept.



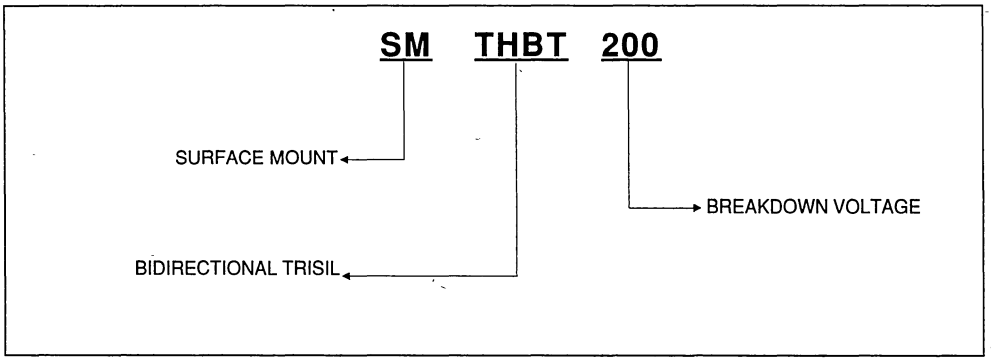
FUNCTIONAL DESCRIPTION



LINE A AND LINE B PROTECTION.

Each line (TIP and RING) is protected by the bidirectional Trisil, which triggers at a maximum voltage equal to the V_{BO}.

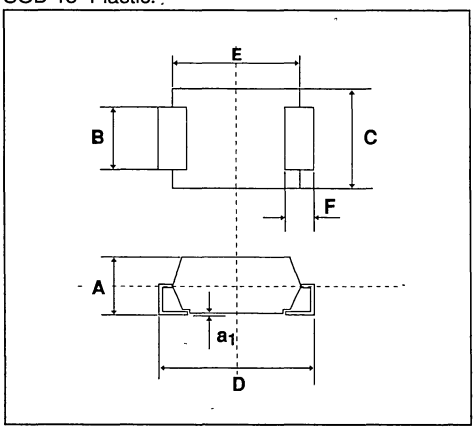
ORDER CODE



MARKING = Logo, WO4

PACKAGE MECHANICAL DATA .

SOD 15 Plastic.



Ref	Millimeters		Inches	
	min	max	min	max
A	2.5	3.1	0.098	0.122
a_1	-	0.2	-	0.008
B	2.9	3.1	0.114	0.122
C	4.8	5.2	0.190	0.200
D	7.6	8.0	0.300	0.315
E	6.3	6.6	0.248	0.259
F	1.3	1.7	0.051	0.067

Packaging : Standard packaging is in film.

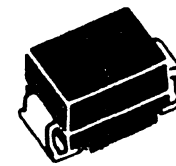
SGS-THOMSON MICROELECTRONICS

SMTPA SERIES

TRISIL

FEATURES

- BIDIRECTIONAL CROWBAR PROTECTION.
- BREAKDOWN VOLTAGE RANGE:
  From 62 V To 270 V.
- HOLDING CURRENT = 150 mA min
- PEAK PULSE CURRENT :
  I_{PP} = 50 A, 10/1000 µs.

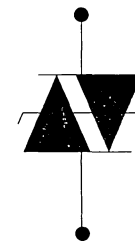


SOD 6
(Plastic)

DESCRIPTION

The SMTPAxx series has been designed to protect telecommunication equipments against lightning and transient induced by AC power lines.

SCHEMATIC DIAGRAM



IN ACCORDANCE WITH FOLLOWING STANDARDS :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

ABSOLUTE RATINGS (limiting values) (-40°C ≤ T_{amb} ≤ + 85°C)

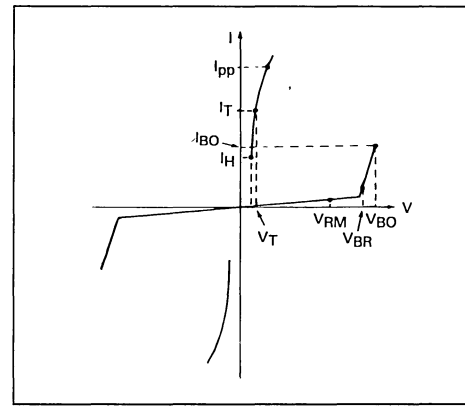
Symbol	Parameter		Value	Unit
P	Power dissipation on infinite heatsink	T_{lead} = 50 °C	5	W
I_{PP}	Peak pulse current	10/1000 µs 8/20 µs	50 100	A
I_{TSM}	Non repetitive surge peak on-state current	tp = 20 ms	30	A
di/dt	Critical rate of rise of on-state current	Non repetitive	100	A/µs
dv/dt	Critical rate of rise of off-state voltage	67% V_{BR}	5	KV/µs
T_{stg} T_j	Storage and operating junction temperature range		- 40 to + 150 150	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		260	°C

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction to leads. on infinite heatsink.	20	°C/W
R_{th} (j-a)	Junction to ambient. on printed circuit with standard footprint dimensions.	100	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{BO}	Breakover voltage
I_H	Holding current
V_T	On-state voltage
I_{BO}	Breakover current
I_{PP}	Peak pulse current

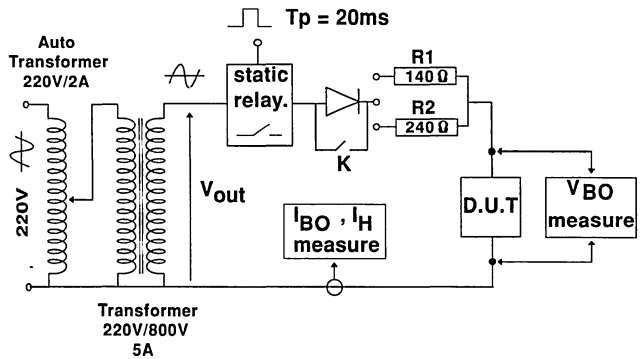


Type	Marking	I_{RM} @ V_{RM} max		V_{BR} @ I_R min		V_{BO} @ I_{BO} max note1		I_H min note1	V_T max note2	C max note3
	Laser	µA	V	V	mA	V	mA	mA	V	pF
SMTPA62	U01	2	56	62	1	82	800	150	2	150
SMTPA68	U05	2	61	68	1	90	800	150	2	150
SMTPA100	U13	2	90	100	1	133	800	150	2	100
SMTPA120	U17	2	108	120	1	160	800	150	2	100
SMTPA130	U19	2	117	130	1	173	800	150	2	100
SMTPA180	U25	2	162	180	1	240	800	150	2	100
SMTPA200	U27	2	180	200	1	267	800	150	2	100
SMTPA220	U31	2	198	220	1	293	800	150	2	100
SMTPA240	U35	2	216	240	1	320	800	150	2	100
SMTPA270	U39	2	243	270	1	360	800	150	2	100

All parameters tested at 25°C, except where indicated.

Note 1 : See the reference test circuit for I_H, I_{BO} and V_{BO} parameters.
Note 2 : Square pulse Tp = 1 ms - I_T = 3A
Note 3 : V_R = 1V, F = 1MHz.

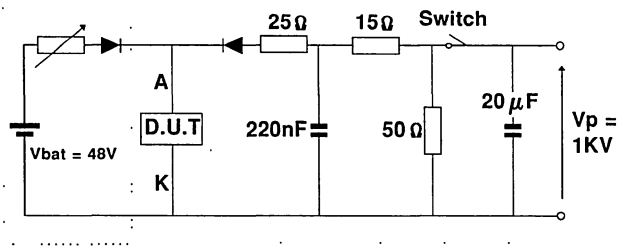
REFERENCE TEST CIRCUIT FOR I_H, I_{BO} and V_{BO} parameters :



TEST PROCEDURE :

- Pulse Test duration (Tp = 20ms):
  - For Bidirectional devices = Switch K is closed
  - For Unidirectional devices = Switch K is open.
- V_{OUT} Selection
  - Device with $V_{BR} \leq 150$ Volt
    - V_{OUT} = 250 V_{RMS}, R_1 = 140 Ω.
  - Device with $V_{BR} \geq 150$ Volt
    - V_{OUT} = 480 V_{RMS}, R_2 = 240 Ω.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT = GO - NOGO TEST.



Surge Generator
10/700 µsec
Vp =1KV / Ipp = 25A

This is a GO-NOGO Test which allows to confirm the holding current (I_H) level in a functional test circuit. This test can be performed if the reference test circuit can't be implemented.

TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.
2) Fire the D.U.T with a surge Current : Ipp = 25A , 10/700 µs.
3) The D.U.T will come back to the OFF-State withing a duration of 50 ms max.

Figure 1 : Non repetitive surge peak on state current versus number of cycles. (with sinusoidal pulse: F= 50 Hz).

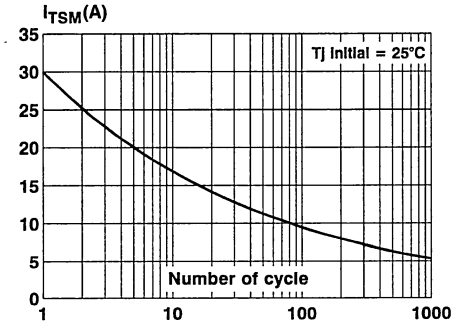


Figure 2 : On state characteristics (typical values).

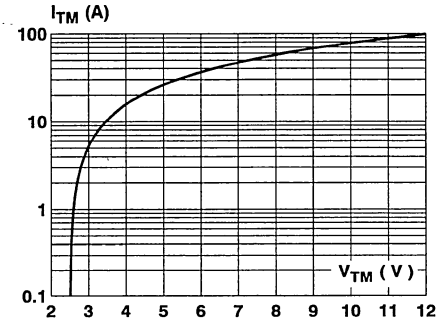
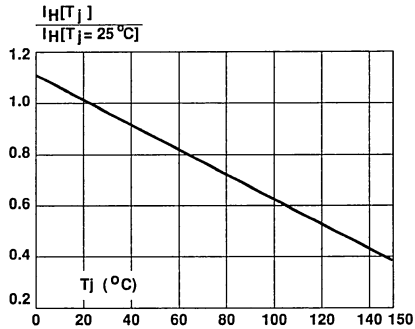
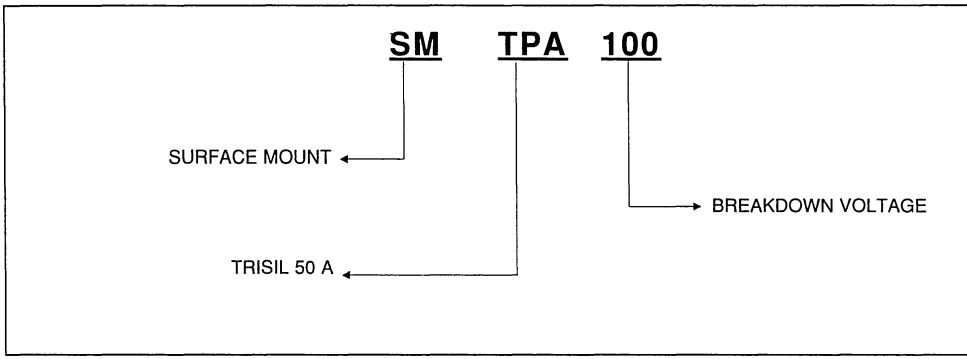


Figure 3 : Relative variation of holding current versus junction temperature.



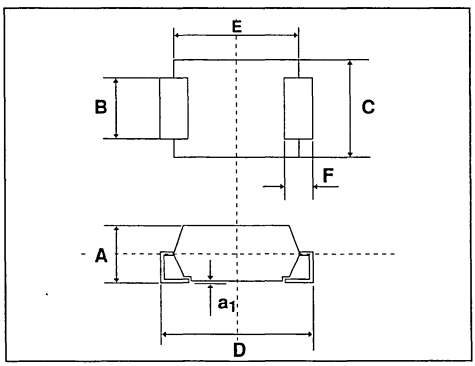
ORDER CODE



MARKING : Logo, date code, type code.

PACKAGE MECHANICAL DATA.

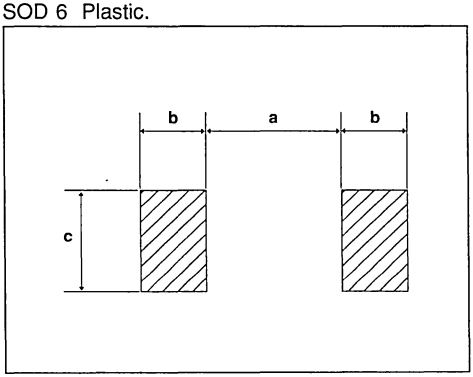
SOD 6 Plastic.



Ref	Millimeters		Inches	
	min	max	min	max
A	2.48	2.61	0.096	0.103
a_1	0.10	0.20	0.004	0.008
B	1.96	2.11	0.077	0.083
C	3.65	3.93	0.143	0.155
D	5.39	5.59	0.212	0.220
E	4.15	4.30	0.163	0.170
F	1.00	1.27	0.039	0.050

FOOTPRINT DIMENSIONS (Millimeters)

SOD 6 Plastic.



Ref	Millimeters
a	2.75
b	1.52
c	2.30

Packaging : Standard packaging is in film.

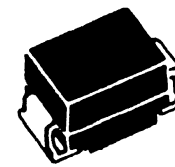
SGS-THOMSON MICROELECTRONICS

SMTPB SERIES

TRISIL

FEATURES

- BIDIRECTIONAL CROWBAR PROTECTION.
- BREAKDOWN VOLTAGE RANGE:
  From 62 V To 270 V.
- HOLDING CURRENT = 150 mA min
- PEAK PULSE CURRENT :
  I_{PP} = 90 A, 10/1000 µs.

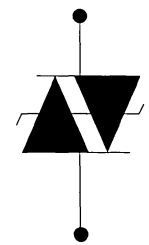


SOD 15
(Plastic)

DESCRIPTION

The SMTPBxx series has been designed to protect telecommunication equipment against lightning and transient induced by AC power lines.

SCHEMATIC DIAGRAM



IN ACCORDANCE WITH FOLLOWING STANDARDS :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

ABSOLUTE RATINGS (limiting values) ($-40°C \leq T_{amb} \leq +85°C$)

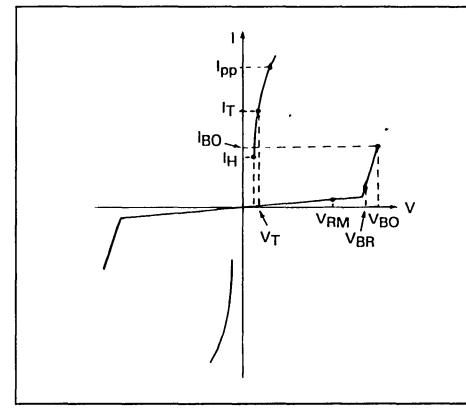
Symbol	Parameter		Value	Unit
P	Power dissipation on infinite heatsink	T_{lead} = 50 °C	10	W
I_{PP}	Peak pulse current	10/1000 µs 8/20 µs	90 150	A
I_{TSM}	Non repetitive surge peak on-state current	tp = 20 ms	50	A
di/dt	Critical rate of rise of on-state current	Non repetitive	100	A/µs
dv/dt	Critical rate of rise of off-state voltage	67% V_{BR}	5	KV/µs
T_{stg} T_j	Storage and operating junction temperature range		- 40 to + 150 + 150	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		+ 260	°C

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction to leads. On infinite heatsink.	10	°C/W
R_{th} (j-a)	Junction to ambient. On printed circuit with standard footprint dimensions.	75	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{BO}	Breakover voltage
I_H	Holding current
V_T	On-state voltage
I_{BO}	Breakover current
I_{PP}	Peak pulse current

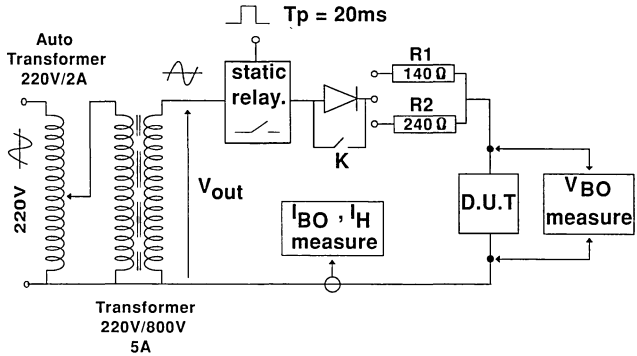


Type	Marcking	I_{RM} @ V_{RM} max		V_{BR} @ I_R min		V_{BO} @ I_{BO} max note1		I_H min note1	V_T max note2	C max note3
	Laser	µA	V	V	mA	V	mA	mA	V	pF
SMTPB62	W07	2	56	62	1	82	800	150	3.5	350
SMTPB68	W11	2	61	68	1	90	800	150	3.5	350
SMTPB100	W17	2	90	100	1	133	800	150	3.5	200
SMTPB120	W21	2	108	120	1	160	800	150	3.5	200
SMTPB130	W23	2	117	130	1	173	800	150	3.5	200
SMTPB180	W29	2	162	180	1	240	800	150	3.5	200
SMTPB200	W31	2	180	200	1	267	800	150	3.5	200
SMTPB220	W35	2	198	220	1	293	800	150	3.5	200
SMTPB240	W39	2	216	240	1	320	800	150	3.5	200
SMTPB270	W43	2	243	270	1	360	800	150	3.5	200

All parameters tested at 25°C, except where indicated.

Note 1 : See the reference test circuit for I_H, I_{BO} and V_{BO} parameters.
Note 2 : Square pulse Tp = 1 ms - I_T = 5A.
Note 3 : V_R = 1V, F = 1MHz.

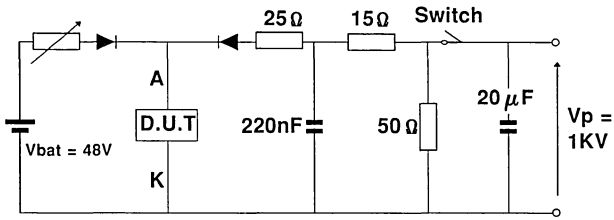
REFERENCE TEST CIRCUIT FOR I_H, I_{BO} and V_{BO} parameters :



TEST PROCEDURE :

- Pulse Test duration (Tp = 20ms):
  - For Bidirectional devices = Switch K is closed
  - For Unidirectional devices = Switch K is open.
- V_{OUT} Selection
  - Device with $V_{BR} \leq 150$ Volt
    - $V_{OUT} = 250\ V_{RMS}$, $R_1 = 140\ \Omega$.
  - Device with $V_{BR} \geq 150$ Volt
    - $V_{OUT} = 480\ V_{RMS}$, $R_2 = 240\ \Omega$.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT = GO - NOGO TEST.



Surge Generator
10/700 µsec
Vp =1KV / Ipp = 25A

This is a GO-NOGO Test which allows to confirm the holding current (I_H) level in a functional test circuit. This test can be performed if the reference test circuit can't be implemented.

TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.
2) Fire the D.U.T with a surge Current : Ipp = 25A , 10/700 µs.
3) The D.U.T will come back to the OFF-State withing a duration of 50 ms max.

Figure 1 : Non repetitive surge peak on state current versus number of cycles. (with sinusoïdal pluse: F= 50 Hz).

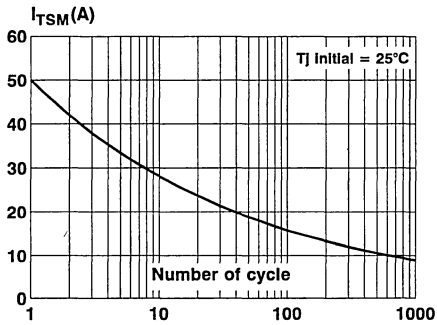


Figure 2 : On - state characteristics (typical values).

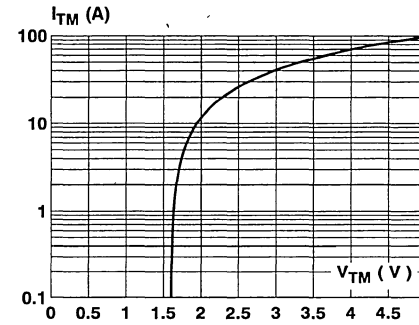
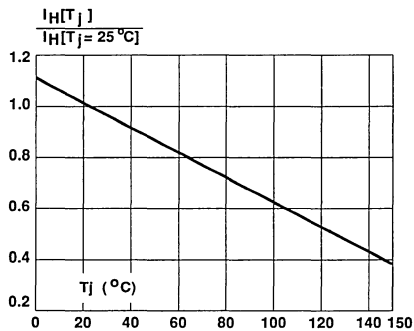
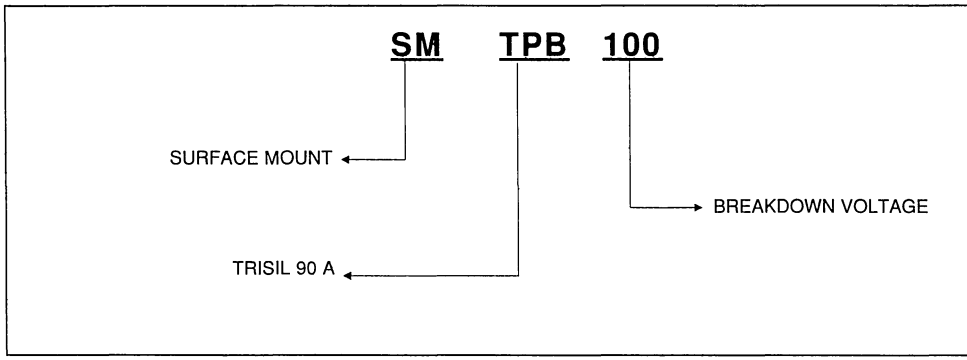


Figure 3 : Relative variation of holding current versus junction temperature.



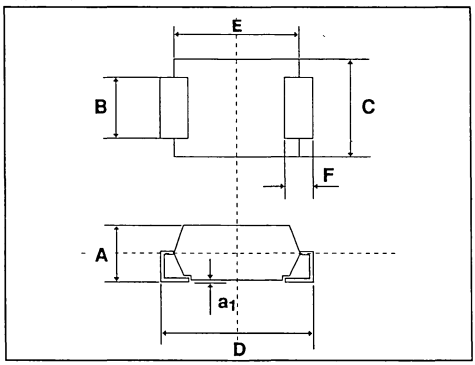
ORDER CODE



MARKING : Logo, date code, type code.

PACKAGE MECHANICAL DATA.

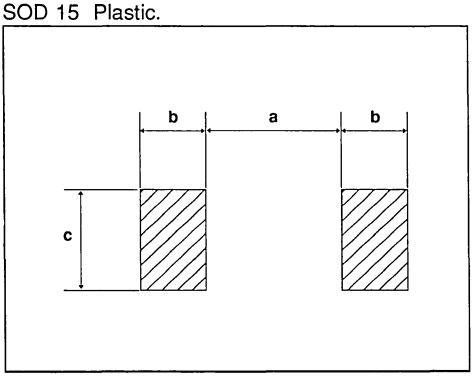
SOD 15 Plastic.



Ref	Millimeters		Inches	
	min	max	min	max
A	2.5	3.1	0.098	0.122
a_1	-	0.2	-	0.008
B	2.9	3.1	0.114	0.122
C	4.8	5.2	0.190	0.200
D	7.6	8.0	0.300	0.315
E	6.3	6.6	0.248	0.259
F	1.3	1.7	0.051	0.067

FOOTPRINT DIMENSIONS.

SOD 15 Plastic.



Ref	Millimeters
a	4.2
b	2
c	3.3

Packaging : Standard packaging is in film.

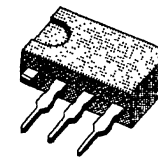
SGS-THOMSON MICROELECTRONICS

THBT200S

TRISIL FOR LINE CARD PROTECTION

FEATURES

- DUAL BIDIRECTIONAL CROWBAR PROTECTION.
- PEAK PULSE CURRENT :
  - I_{PP} = 75 A, 10/1000 µs.
- HOLDING CURRENT = 150 mA min
- BREAKDOWN VOLTAGE = 200 V min.
- BREAKOVER VOLTAGE = 290 V max.

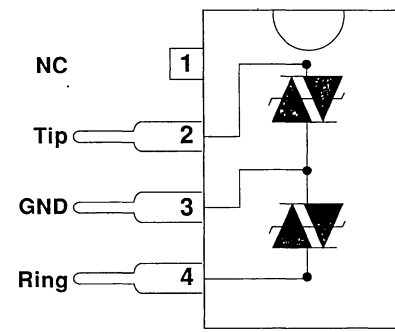


SIP 3
(Plastic)

DESCRIPTION

This protection device has been especially designed to protect subscriber line cards using SLICS without integrated ring generator. THBT200 device protects ring generator relays against transient overvoltages.

SCHEMATIC DIAGRAM

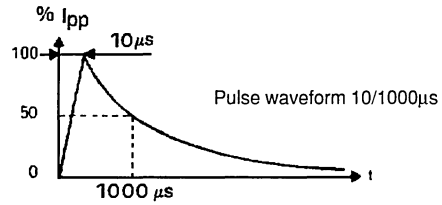


IN ACCORDANCE WITH FOLLOWING STANDARDS :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

ABSOLUTE RATINGS (limiting values) (-40°C ≤ T_{amb} ≤ + 85°C)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current	10/1000 µs 8/20 µs	75 150	A
I_{TSM}	Non repetitive surge peak on-state current	tp = 20 ms	30	A
di/dt	Critical rate of rise of on-state current	Non repetitive	100	A/µs
dv/dt	Critical rate of rise of off-state voltage	67% V_{BR}	5	KV/µs
T_{stg} T_j	Storage and operating junction temperature range		- 40 to + 150 + 150	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		260	°C

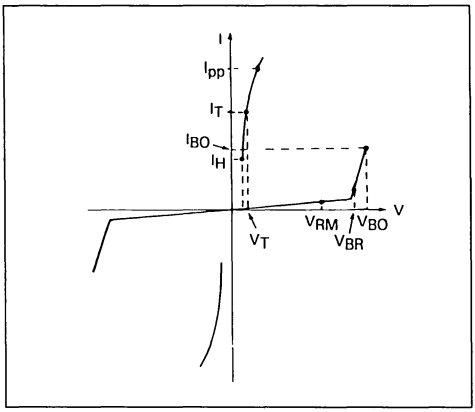


THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
R_{th} (j-a)	Junction-to-ambient	70	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{BO}	Breakover voltage
I_H	Holding current
V_T	On-state voltage
I_{BO}	Breakover current
I_{PP}	Peak pulse current



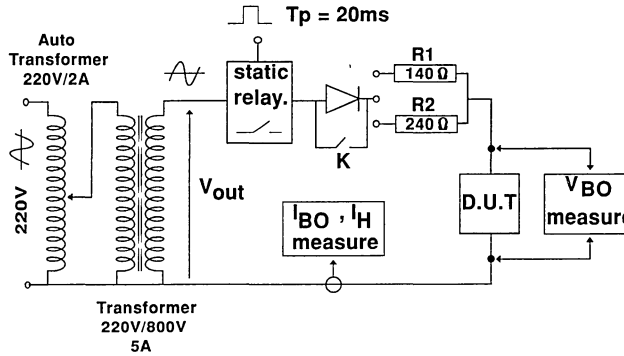
PARAMETERS RELATED TO ONE TRISIL.

Type	I_{RM} @ V_{RM}		V_{BR} @ I_R		V_{BO} @ I_{BO}			I_H	V_T	C
	max		min		max	min note1	max	min note1	max note2	max note3
	µA	V	V	mA	V	mA	mA	mA	V	pF
THBT200S	10	180	200	1	290	150	800	150	8	200

All parameters tested at 25°C, except where indicated

Note 1 : See test reference test circuit for I_H, I_{BO} and V_{BO} parameters
Note 2 : Square pulse Tp = 500 µs - I_T = 5A
Note 3 : V_R = 1V, F = 1MHz.

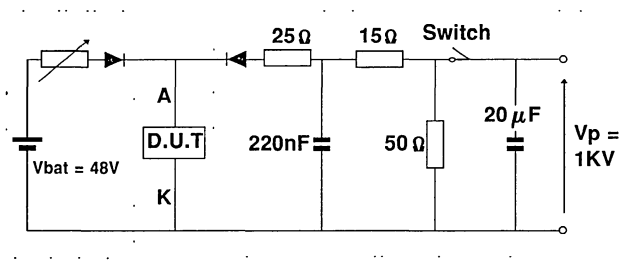
REFERENCE TEST CIRCUIT FOR I_H, I_{BO} and V_{BO} parameters :



TEST PROCEDURE :

- Pulse Test duration (Tp = 20ms):
  - For Bidirectional devices = Switch K is closed
  - For Unidirectional devices = Switch K is open.
- V_{OUT} Selection
  - Device with $V_{BR} \leq 150$ Volt
    - $V_{OUT} = 250\ V_{RMS}$, $R_1 = 140\ \Omega$.
  - Device with $V_{BR} \geq 150$ Volt
    - $V_{OUT} = 480\ V_{RMS}$, $R_2 = 240\ \Omega$.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT = GO - NOGO TEST.



Surge Generator
10/700 μsec
Vp =1KV / Ipp = 25A

This is a GO-NOGO Test which allows to confirm the holding current (I_H) level in a functional test circuit. This test can be performed if the reference test circuit can't be implemented.

TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.
2) Fire the D.U.T with a surge Current : Ipp = 25A , 10/700 μs.
3) The D.U.T will come back to the OFF-State within a duration of 50 ms max.

Figure 1 : Relative variation of holding current versus junction temperature.

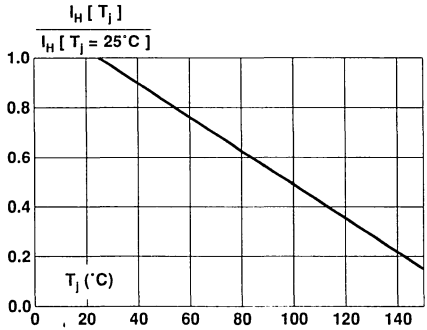


Figure 2 : Non repetitive surge peak on state current versus number of cycles (1 cycle = 20

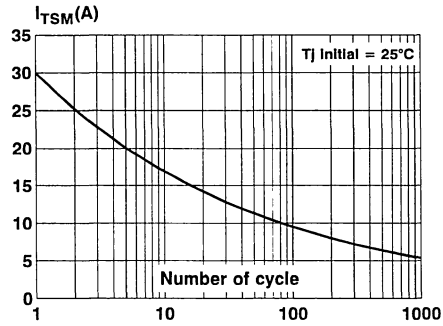


Figure 3 : Peak on state voltage versus peak on state current (typical values).

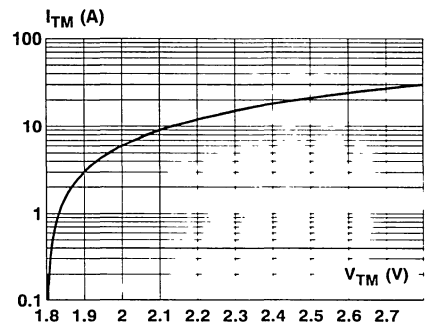
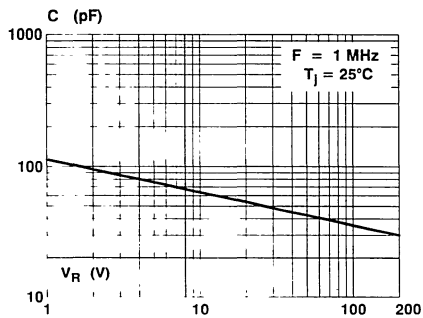
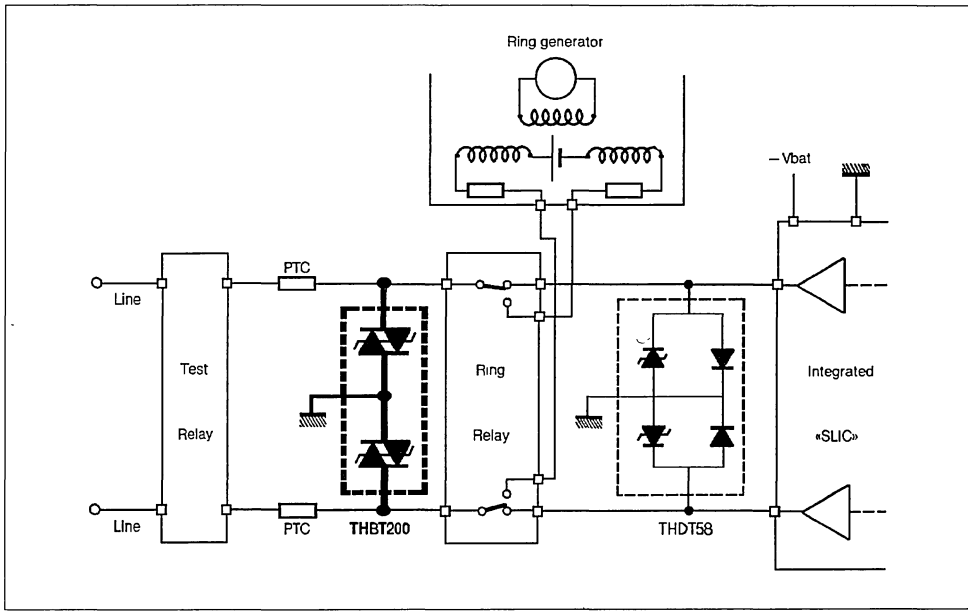


Figure 4 : Capacitance versus reverse applied voltage (typical values).

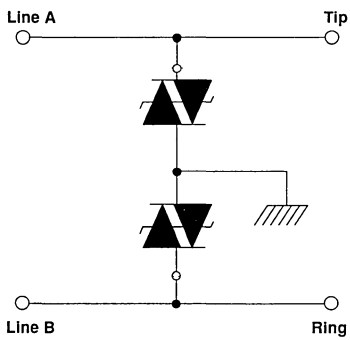


APPLICATION CIRCUIT

Typical line card protection concept



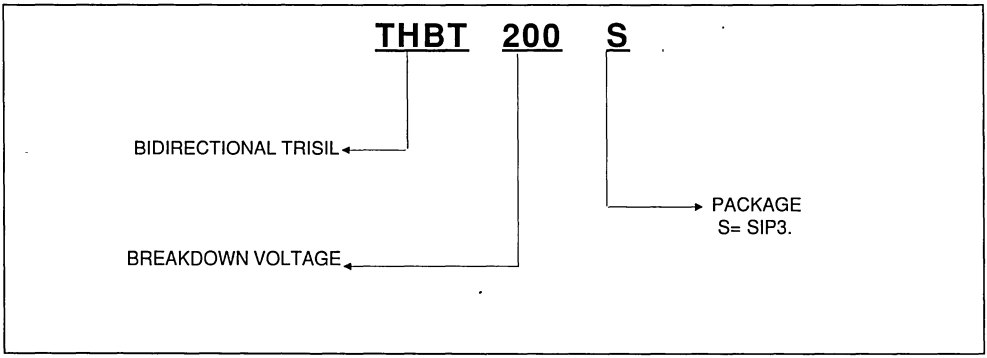
FUNCTIONAL DESCRIPTION



LINE A AND LINE B PROTECTION.

Each line (TIP and RING) is protected by a bidirectional Trisil, which triggers at a maximum voltage equal to the V_{BO}.

ORDER CODE

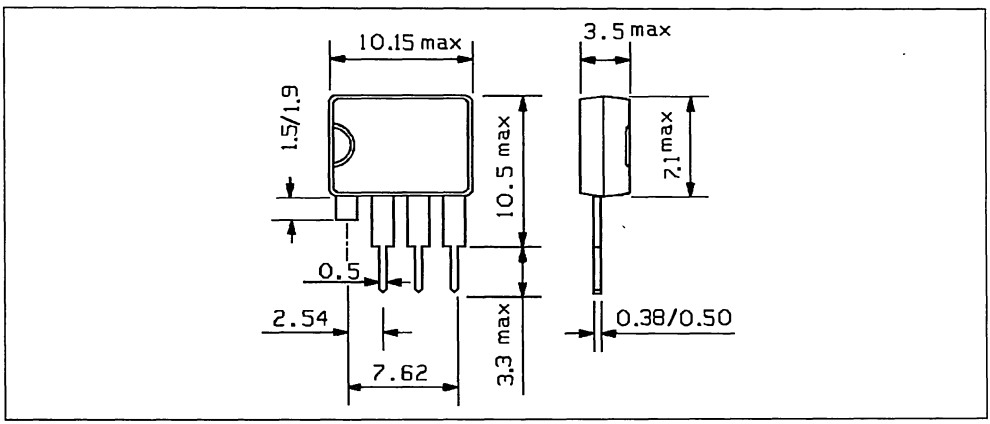


MARKING

Package	Type	Marking
SIP3	THBT200S	THBT200S

PACKAGE MECHANICAL DATA (in millimeters)

SIP 3 Plastic.



Packaging : Products supplied in antistatic tubes.

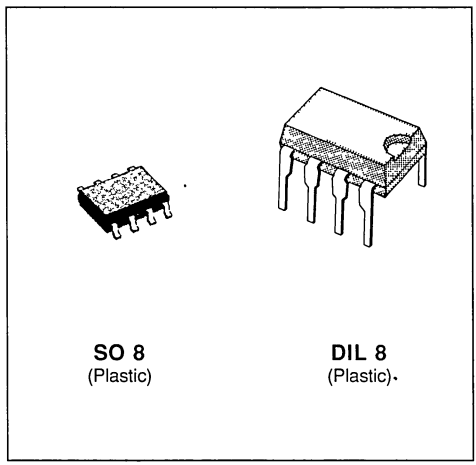
SGS-THOMSON MICROELECTRONICS

THDT51
THDT65

TRISIL FOR SLIC PROTECTION

FEATURES

- DUAL ASYMETRICAL TRANSIENT SUPPRESSOR
- PEAK PULSE CURRENT :
  I_{PP} = 30 A, 10/1000 µs.
- HOLDING CURRENT = 150 mA min
- BREAKDOWN VOLTAGE
  - THDT51 = 51 V
  - THDT65 = 65 V.
- LOW DYNAMIC CHARACTERISTICS
- AVAILABLE IN SO8 AND DIL8.



SO 8
(Plastic)

DIL 8
(Plastic)

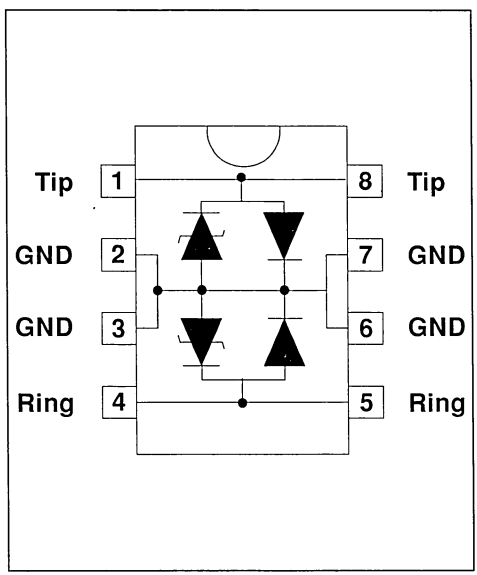
DESCRIPTION

These devices have been especially designed to protect subscriber line card interfaces (SLIC) against transient overvoltages.

A particular attention has been given to the internal wire bonding . A 4-points configuration ensures a reliable protection, eliminating the overvoltage introduced by the parasitic inductances of the wiring (Ldi/dt) especially for very fast transients.

This new product generation, is providing very high surge current capability, in small packages like SO 8 and DIL 8. Dynamic characteristics have also been defined in order to meet SLIC max rating.

SCHEMATIC DIAGRAM

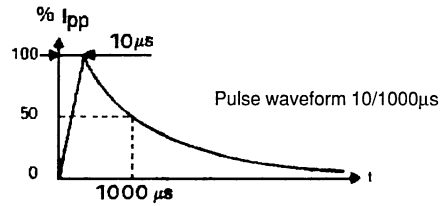


IN ACCORDANCE WITH FOLLOWING STANDARDS :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

ABSOLUTE RATINGS (limiting values) (-40°C ≤ T_{amb} ≤ +85°C)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current	10/1000 µs 5/320 µs 2/10 µs	30 40 90	A
I_{TSM}	Non repetitive surge peak on-state current	tp = 10 ms tp = 1 s	10 5	A
di/dt	Critical rate of rise of on-state current	Non repetitive	100	A/µs
dv/dt	Critical rate of rise of off-state voltage	67% V_{BR}	5	KV/µs
T_{stg} T_j	Storage and operating junction temperature range		- 55 to + 150 + 150	°C °C



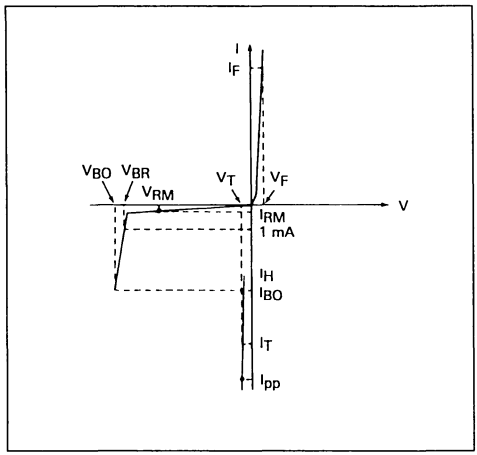
Pulse waveform 10/1000µs

THERMAL RESISTANCES

Symbol	Parameter		Value	Unit
R_{th} (j-a)	Junction-to-ambient	DIL 8 SO 8	125 170	°C/W °C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{BO}	Breakover voltage
I_H	Holding current
V_T	On-state voltage
V_F	Forward Voltage Drop
I_{BO}	Breakover current
I_{PP}	Peak pulse current



PARAMETERS RELATED TO DIODE LINE/GND

Symbol	Test conditions	Value	Unit
V_F	Square pulse, tp = 500 µs, I_F = 3 A.	3	V
V_{FP}	I_{PP} = 30A, 10/1000µs	7	V

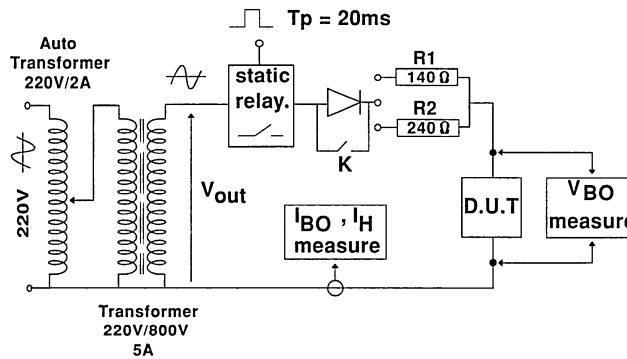
PARAMETERS RELATED TO PROTECTION THYRISTOR

Types	I_{RM} @ V_{RM} max		VBR @ I_R min		V_{BO} @ I_{BO} max	min note1		I_H min note1	V_T max note2	C max note3
	µA	V	V	mA	V	mA	mA	mA	V	pF
THDT51	10	50	51	1	70	50	500	150	4	200
THDT65	10	56	65	1	85	50	500	150	4	200

All parameters tested at 25°C, except where indicated

Note 1 : See the reference test circuit for I_H, I_{BO} and V_{BO} parameters.
Note 2 : Square pulse Tp = 500 µs - I_T = 5A.
Note 3 : V_R = 1V, F = 1MHz.

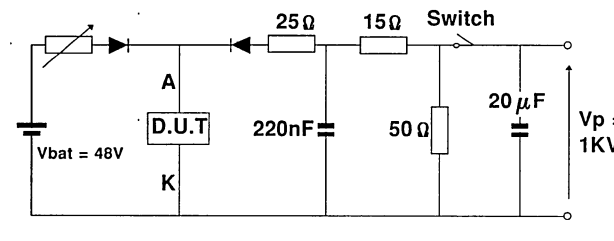
REFERENCE TEST CIRCUIT FOR I_H, I_{BO} and V_{BO} parameters :



TEST PROCEDURE :

- Pulse Test duration (Tp = 20ms):
  - For Bidirectional devices = Switch K is closed
  - For Unidirectional devices = Switch K is open.
- V_{OUT} Selection
  - Device with $V_{BR} \leq 150$ Volt
    - V_{OUT} = 250 V_{RMS}, R_1 = 140 Ω.
  - Device with $V_{BR} \geq 150$ Volt
    - V_{OUT} = 480 V_{RMS}, R_2 = 240 Ω.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT = GO - NOGO TEST.



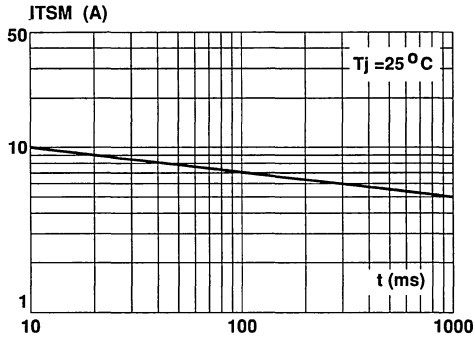
Surge Generator
10/700 µsec
Vp =1KV / Ipp = 25A

This is a GO-NOGO Test which allows to confirm the holding current (I_H) level in a functional test circuit. This test can be performed if the reference test circuit can't be implemented

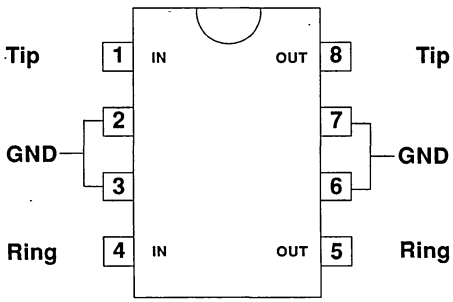
TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.
2) Fire the D.U.T with a surge Current : Ipp = 25A , 10/700 µs.
3) The D.U.T will come back to the OFF-State within a duration of 50 ms max.

Figure 1 : Non repetitive surge peak on-state current. (with sinusoidal pulse : F =50Hz)



APPLICATION NOTE.



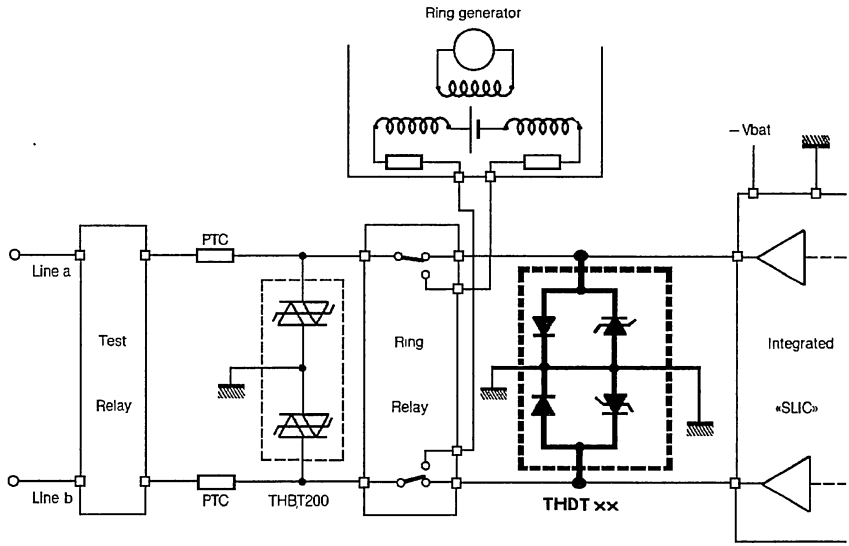
4- points structure lay-out.

1) Connect pins 2, 3, 6 and 7 to ground in order to guarantee a good surge current capability for long duration disturbances.

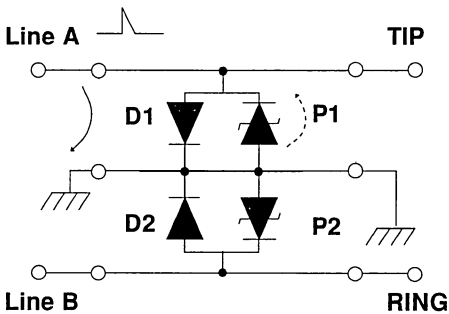
2) In order to take advantage of the "4-points structure" of the THDTxx, the tip and Ring lines have to cross through the device. in this case, the device will eliminate the overvoltages generated by the parasitic inductances of the wiring (Ldi/dt), especially for very fast Transients.

APPLICATION CIRCUIT

Typical slic protection concept



FUNCTIONAL DESCRIPTION



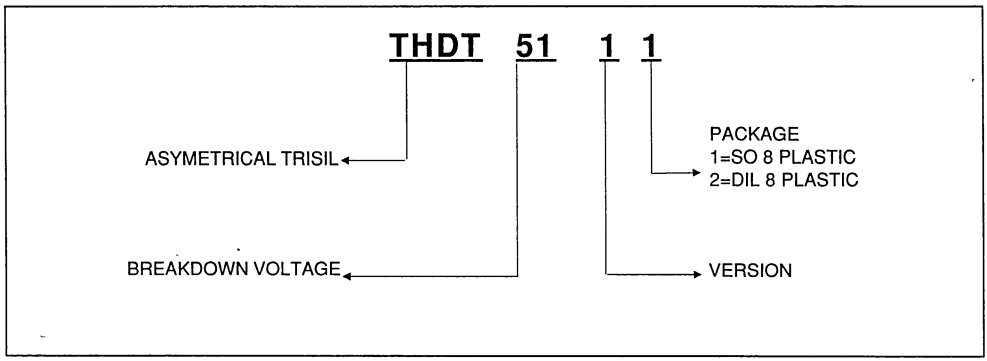
Line A Protection =

- For positive Surges versus GND, the diode D1 will conduct
- For negative Surges versus GND, the Protection device P1 will trigger at a maximum voltage equal to the V_{BO}.

Line B Protection =

- For Surges on line B, the operating mode is the same, D2 or P2 is activated.

ORDER CODE



MARKING

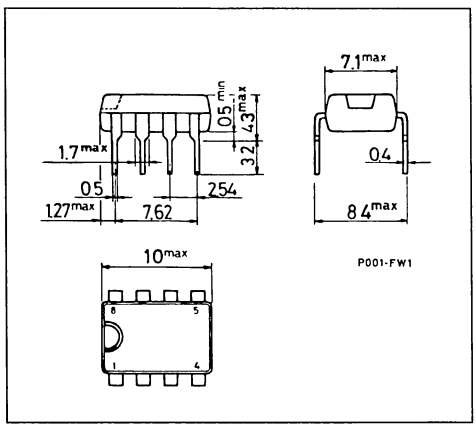
Package	Type	Marking
SO8	THDT5111 THDT6511	DT5111 DT6511

Package	Type	Marking
DIL8	THDT5112 THDT6512	DT5112 DT6512

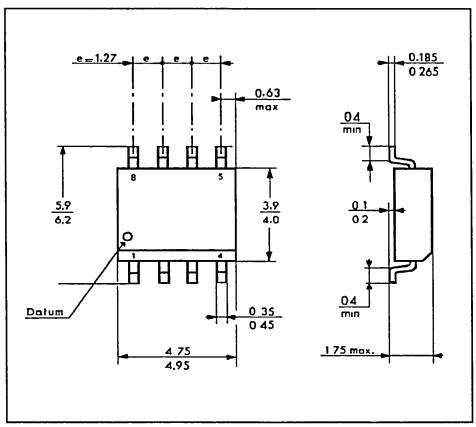
Packaging : Products supplied in antistatic tubes.

PACKAGE MECHANICAL DATA (in millimeters)

DIL 8 Plastic

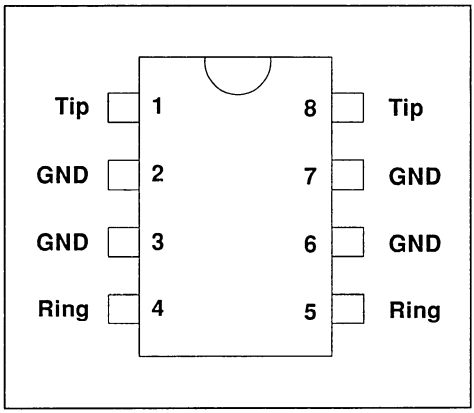


SO 8 Plastic

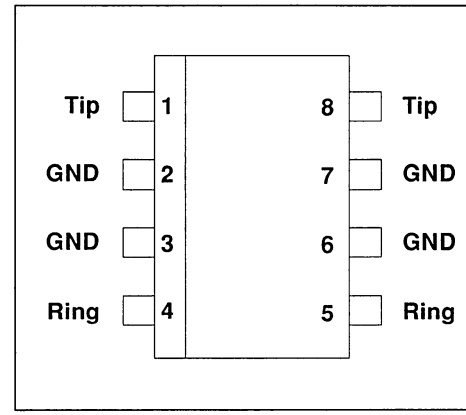


CONNECTION DIAGRAM

DIL 8 Plastic



SO 8 Plastic



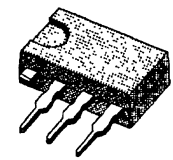
SGS-THOMSON MICROELECTRONICS

THDT58S

TRISIL FOR SLIC PROTECTION

FEATURES

- CROWBAR PROTECTION
- DUAL ASYMETRICAL TRANSIENT SUPPRESSOR
- PEAK PULSE CURRENT :
  - I_{PP} = 75 A, 10/1000 µs.
- HOLDING CURRENT = 150 mA min
- BREAKDOWN VOLTAGE = 58 V.
- BREAKOVER VOLTAGE = 80V max.



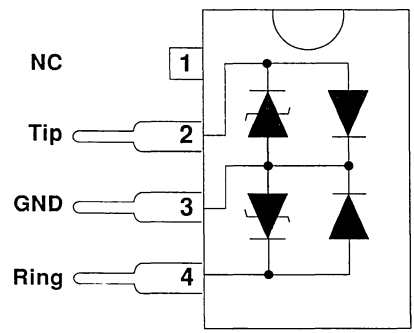
SIP 3
(Plastic)

DESCRIPTION

This device has been especially designed to protect subscriber line card interfaces (SLIC) against transient overvoltages.

Its ion-implanted technology confers excellent electrical characteristics on it.
This is why this device easily fits the main protection standards which are related to the overvoltages on telecom lines.
This product is compatible with TO202 and TO220 packages.

SCHEMATIC DIAGRAM

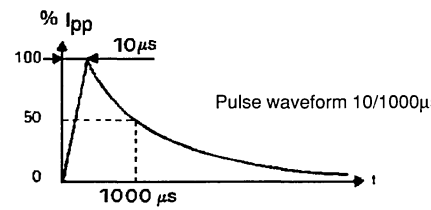


IN ACCORDANCE WITH FOLLOWING STANDARDS :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

ABSOLUTE RATINGS (limiting values) (-40°C ≤ T_{amb} ≤ + 85°C)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current	10/1000 µs 8/20 µs	75 150	A
I_{TSM}	Non repetitive surge peak on-state current	tp = 20 ms	30	A
I_{FSM}	Non repetitive surge peak forward current	tp = 20 ms	30	A
di/dt	Critical rate of rise of off-state current	Non repetitive	100	A/µs
dv/dt	Critical rate of rise of off-state voltage	67% V_{BR}	5	KV/µs
T_{stg} T_j	Storage and operating junction temperature range		- 40 to + 150 + 150	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		260	°C

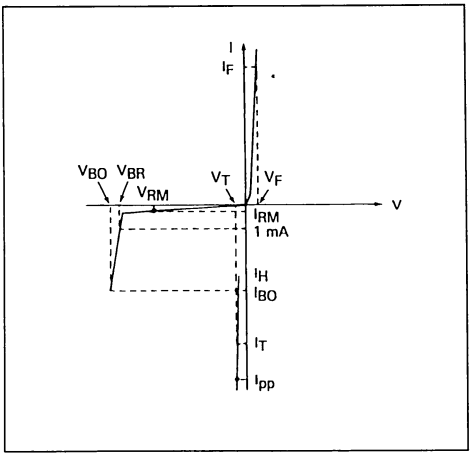


THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
R_{th} (j-a)	Junction-to-ambient	70	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{BO}	Breakover voltage
I_H	Holding current
V_T	On-state voltage
V_F	Forward Voltage Drop
I_{BO}	Breakover current
I_{PP}	Peak pulse current



PARAMETER RELATED TO THE DIODE LINE/GND

Symbol	Test conditions	Value	Unit
V_F	Square pulse, tp = 500 µs I_F = 5 A.	5	V

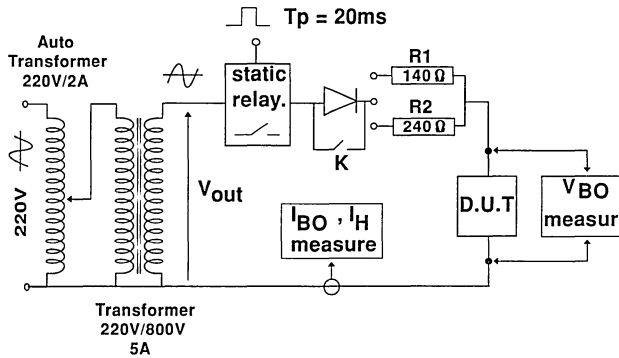
PARAMETERS RELATED TO THE PROTECTION THYRISTOR

Type	I_{RM} @ V_{RM}		V_{BR} @ I_R		V_{BO} @ I_{BO}			I_H	V_T	C
	max		min		max	min note1	max	min note1	max note2	max note3
	µA	V	V	mA	V	mA	mA	mA	V	pF
THDT58S	10	56	58	1	80	150	800	150	5	400

All parameters tested at 25°C, except where indicated

Note 1 : See the reference test circuit for I_H, I_{BO} and V_{BO} parameters
Note 2 : Square pulse Tp = 500 µs - I_T = 5A
Note 3 : V_R = 1V, F = 1MHz.

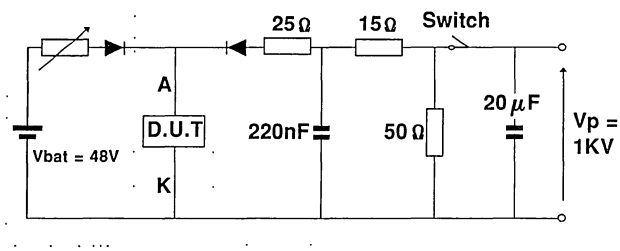
REFERENCE TEST CIRCUIT FOR I_H, I_{BO} and V_{BO} parameters :



TEST PROCEDURE :

- Pulse Test duration (Tp = 20ms):
  - For Bidirectional devices = Switch K is closed
  - For Unidirectional devices = Switch K is open.
- V_{OUT} Selection
  - Device with $V_{BR} \leq 150$ Volt
    - $V_{OUT} = 250\ V_{RMS}$, $R_1 = 140\ \Omega$.
  - Device with $V_{BR} \geq 150$ Volt
    - $V_{OUT} = 480\ V_{RMS}$, $R_2 = 240\ \Omega$.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT = GO - NOGO TEST.



Surge Generator
10/700 μsec
Vp =1KV / Ipp = 25A

This is a GO-NOGO Test which allows to confirm the holding current (I_H) level in a functional test circuit. This test can be performed if the reference test circuit can't be implemented.

TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.
2) Fire the D.U.T with a surge Current : Ipp = 25A , 10/700 μs.
3) The D.U.T will come back to the OFF-State withing a duration of 50 ms max.

Figure 1 : Relative variation of holding current versus junction temperature.

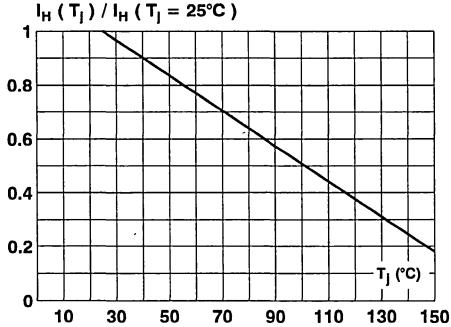


Figure 2 : Non repetitive surge peak on state current versus number of cycles (1 cycle = 20 ms.

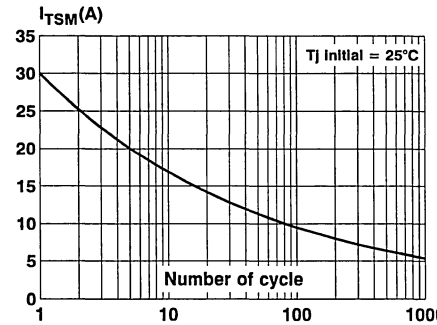


Figure 3 : Peak on state voltage versus peak on state current (typical values).

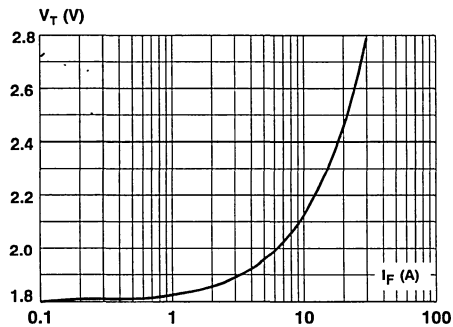


Figure 4 : Peak forward voltage drop versus peak forward current (typical values).

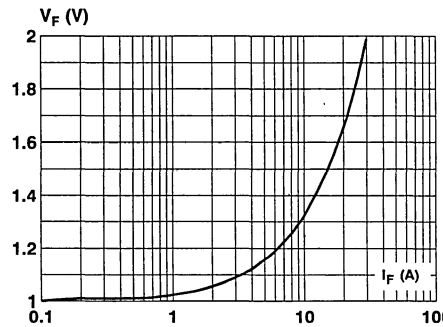
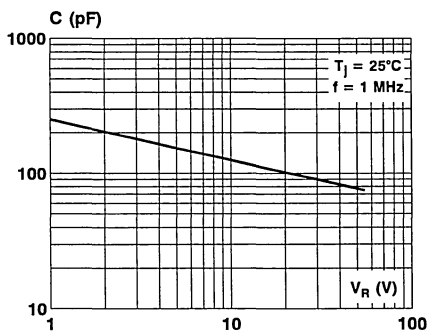
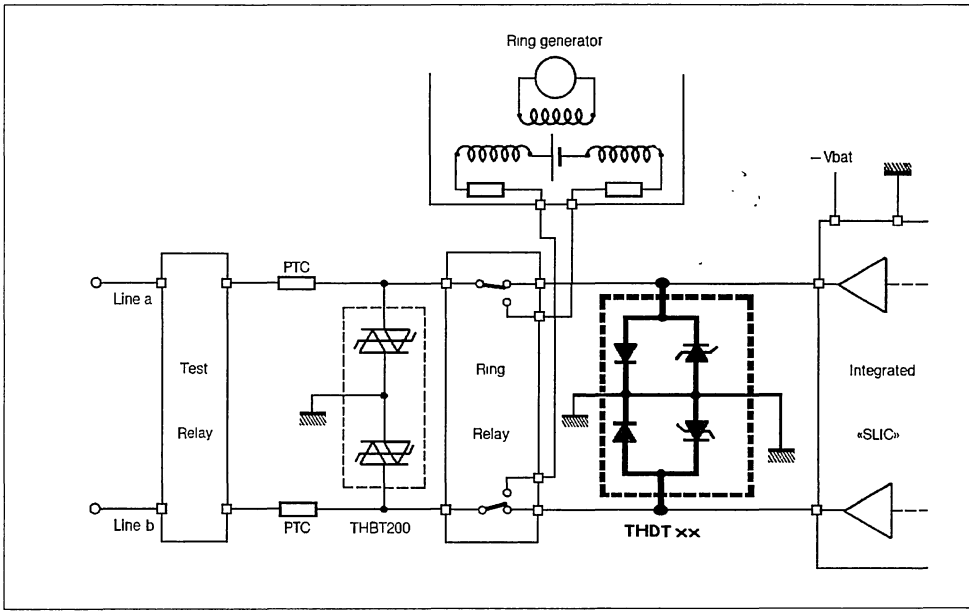


Figure 5 : Capacitance versus reverse applied voltage (typical values).

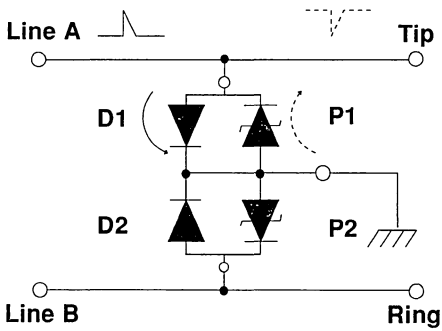


APPLICATION CIRCUIT

Typical slic protection concept



FUNCTIONAL DESCRIPTION



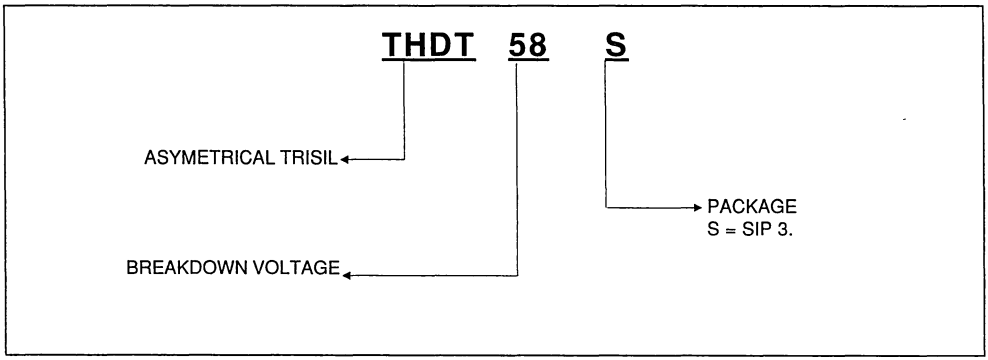
Line A Protection =

- For positive Surges versus GND, the diode D1 will conduct
- For negative Surges versus GND, the Protection device P1 will trigger at a maximum voltage equal to the V_{BO}.

Line B Protection =

- For Surges on line B, the operating mode is the same, D2 or P2 is activated.

ORDER CODE

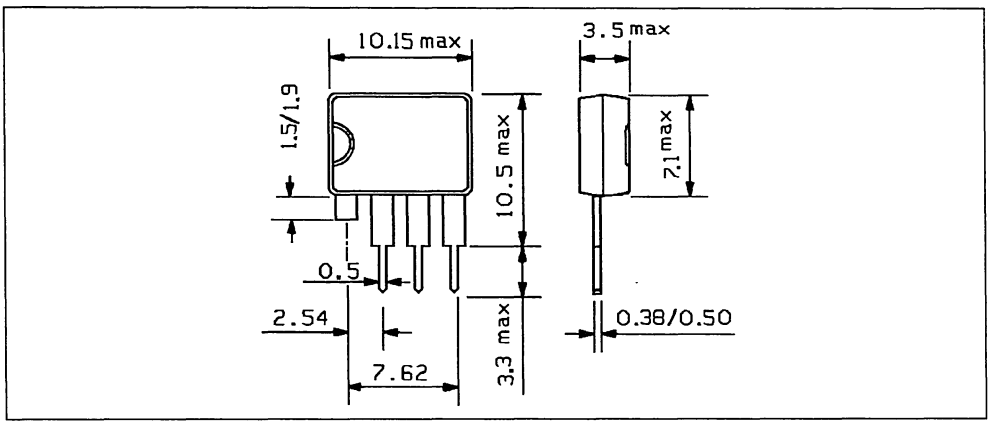


MARKING

Package	Type	Marking
SIP3	THDT58S	THDT58S

PACKAGE MECHANICAL DATA (in millimeters)

SIP 3 Plastic.



Packaging : Products supplied in antistatic tubes.

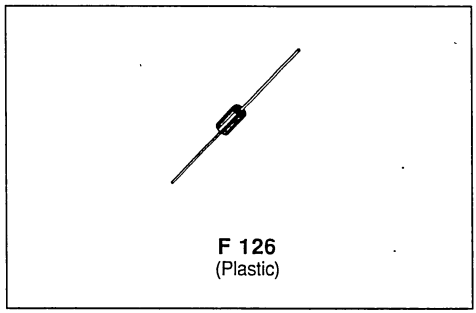
SGS-THOMSON MICROELECTRONICS

TPA SERIES

TRISIL

FEATURES

- BIDIRECTIONAL CROWBAR PROTECTION.
- BREAKDOWN VOLTAGE RANGE:
  From 62 V To 270 V.
- HOLDING CURRENT = I_H
  Suffix 12 = 120mA min.
  Suffix 18 = 180mA min.
- PEAK PULSE CURRENT :
  I_{PP} = 50 A, 10/1000 µs.

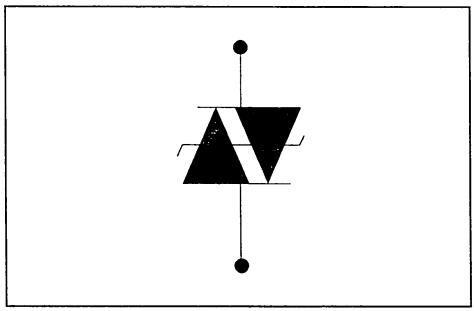


F 126
(Plastic)

DESCRIPTION

The TPAxx series has been designed to protect telecommunication equipments against lightning and transient induced by AC power lines.

SCHEMATIC DIAGRAM



IN ACCORDANCE WITH FOLLOWING STANDARDS :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

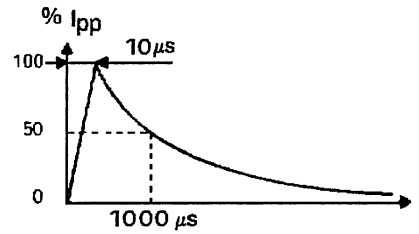
ABSOLUTE RATINGS (limiting values) (-40°C ≤ T_{amb} ≤ + 85°C)

Symbol	Parameter		Value	Unit
P	Power dissipation on infinite heatsink	T_{amb} = 50 °C	1.7	W
I_{PP}	Peak pulse current See note1	10/1000 µs 8/20 µs	50 100	A
I_{TSM}	Non repetitive surge peak on-state current	tp = 20 ms	30	A
di/dt	Critical rate of rise of on-state current	Non repetitive	100	A/µs
dv/dt	Critical rate of rise of off-state voltage	67% V_{BR}	5	KV/µs
T_{stg} T_j	Storage and operating junction temperature range		- 40 to + 150 + 150	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		230	°C

THERMAL RESISTANCES

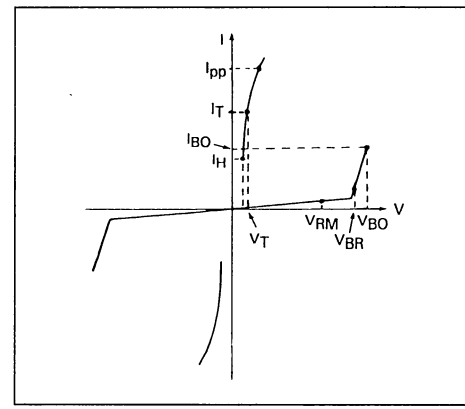
Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction to leads on infinite heatsink.	60	°C/W
R_{th} (j-a)	Junction to ambient. on printed circuit. Llead = 10 mm	100	°C/W

Note 1: 10/1000 µs wave form.



ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{BO}	Breakover voltage
I_H	Holding current
V_T	On-state voltage
I_{BO}	Breakover current
I_{PP}	Peak pulse current



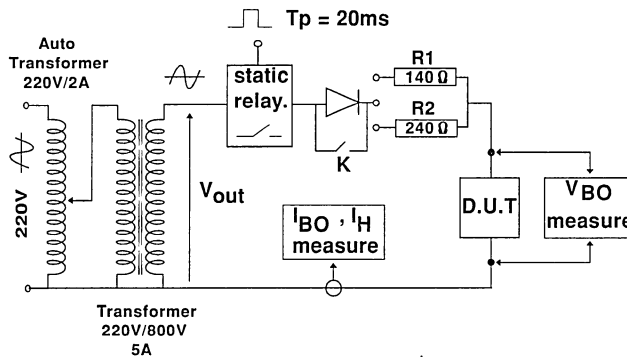
ELECTRICAL CHARACTERISTICS

Type	I_{RM} @ V_{RM} max		V_{BR} @ I_R min		V_{BO} @ I_{BO} max note2	max	V_T max note3	C max note4	I_H min note2
	µA	V	V	mA	V	mA	V	pF	mA
P TPA62A - 12 or 18	2	56	62	1	82	300	2	150	
TPA62B - 12 or 18	2	56	62	1	75	300	2	150	
P TPA68A - 12 or 18	2	61	68	1	90	300	2	150	
TPA68B - 12 or 18	2	61	68	1	82	300	2	150	
(1) TPA75A - 12 or 18	2	67	75	1	100	300	2	150	
(1) TPA75B - 12 or 18	2	67	75	1	91	300	2	150	
(1) TPA82A - 12 or 18	2	74	82	1	109	300	2	150	
(1) TPA82B - 12 or 18	2	74	82	1	99	300	2	150	Suffix 12
(1) TPA91A - 12 or 18	2	82	91	1	121	300	2	150	for 120 mA.
(1) TPA91B - 12 or 18	2	82	91	1	110	300	2	150	
P TPA100A - 12 or 18	2	90	100	1	133	300	2	100	
TPA100B - 12 or 18	2	90	100	1	121	300	2	100	
P TPA110A - 12 or 18	2	99	110	1	147	300	2	100	
TPA110B - 12 or 18	2	99	110	1	133	300	2	100	
P TPA120A - 12 or 18	2	108	120	1	160	300	2	100	Suffix 18
TPA120B - 12 or 18	2	108	120	1	145	300	2	100	for 180 mA.
P TPA130A - 12 or 18	2	117	130	1	173	300	2	100	
TPA130B - 12 or 18	2	117	130	1	157	300	2	100	
(1) TPA150A - 12 or 18	2	135	150	1	200	300	4	75	
(1) TPA150B - 12 or 18	2	135	150	1	181	300	4	75	
(1) TPA160A - 12 or 18	2	144	160	1	213	300	4	75	
(1) TPA160B - 12 or 18	2	144	160	1	193	300	4	75	
P TPA180A - 12 or 18	2	162	180	1	240	300	4	75	
TPA180B - 12 or 18	2	162	180	1	217	300	4	75	
P TPA200A - 12 or 18	2	180	200	1	267	300	4	75	
TPA200B - 12 or 18	2	180	200	1	241	300	4	75	
P TPA220A - 12 or 18	2	198	220	1	293	300	4	75	
TPA220B - 12 or 18	2	198	220	1	265	300	4	75	
P TPA240A - 12 or 18	2	216	240	1	320	300	4	75	
TPA240B - 12 or 18	2	216	240	1	289	300	4	75	
P TPA270A - 12 or 18	2	243	270	1	360	300	4	75	
TPA270B - 12 or 18	2	243	270	1	325	300	4	75	

All parameters tested at 25°C, except where indicated.

P : Preferred device.
(1): These voltages are on request.
Note 2 : See the reference test circuit for I_H, I_{BO} and V_{BO} parameters.
Note 3 : Square pulse Tp = 1 ms - I_T = 3A.
Note 4 : V_R = 1V, F = 1MHz.

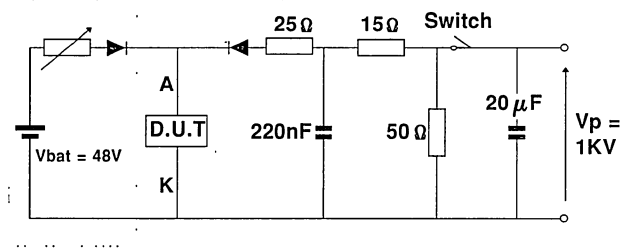
REFERENCE TEST CIRCUIT FOR I_H, I_{BO} and V_{BO} parameters :



TEST PROCEDURE :

- Pulse Test duration (Tp = 20ms):
  - For Bidirectional devices = Switch K is closed
  - For Unidirectional devices = Switch K is open.
- V_{OUT} Selection
  - Device with $V_{BR} \leq 150$ Volt
    - V_{OUT} = 250 V_{RMS}, R_1 = 140 Ω.
  - Device with $V_{BR} \geq 150$ Volt
    - V_{OUT} = 480 V_{RMS}, R_2 = 240 Ω.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT = GO - NOGO TEST.



Surge Generator
10/700 µsec
Vp =1KV / Ipp = 25A

This is a GO-NOGO Test which allows to confirm the holding current (I_H) level in a functional test circuit. This test can be performed if the reference test circuit can't be implemented.

TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.
2) Fire the D.U.T with a surge Current : Ipp = 25A , 10/700 µs.
3) The D.U.T will come back to the OFF-State withing a duration of 50 ms max.

Figure 1 : Non repetitive surge peak on state current versus number of cycles. (with sinusoidal

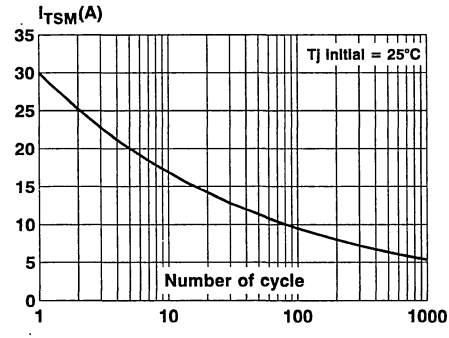
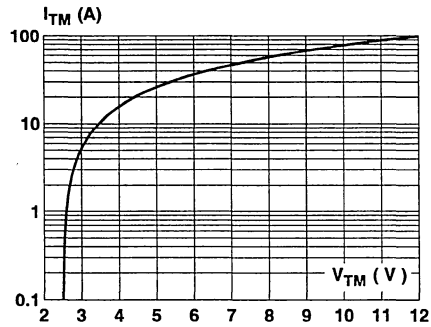
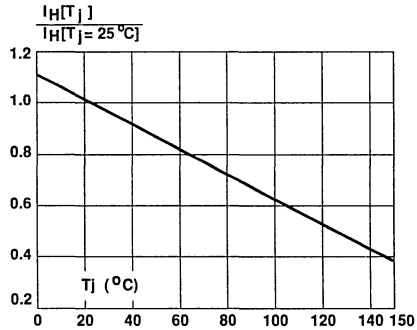


Figure 2 : On - state characteristics (typical values).

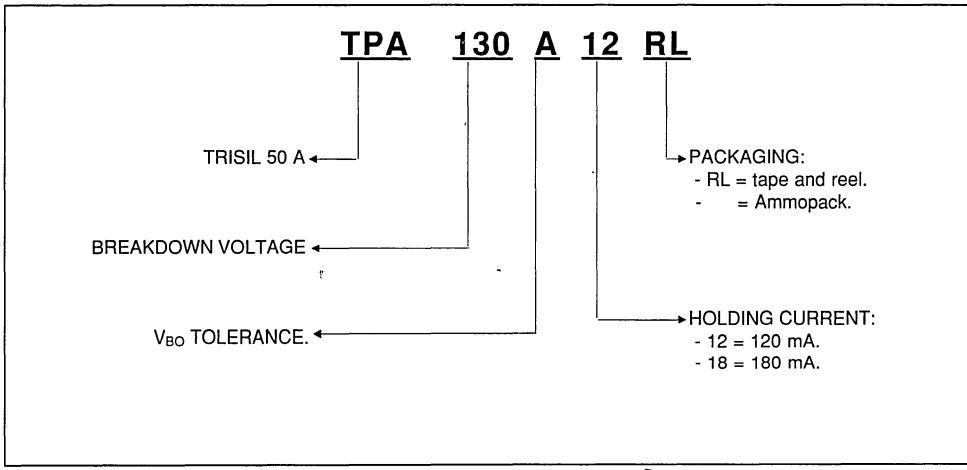


Note : For device with V_{BR} > 150 Volt
The V_T value is twice that shown.

Figure 3 : Relative variation of holding current versus junction temperature.



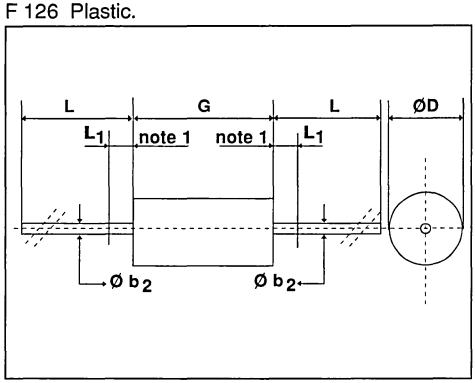
ORDER CODE



MARKING : Logo, Date Code, Part Number.

PACKAGE MECHANICAL DATA.

F 126 Plastic.



Ref	Millimeters		Inches	
	min	max	min	max
Ø b_2	0.76	0.86	0.03	0.034
Ø D	-	3.05	-	0.12
G	-	6.35	-	0.25
L	26	-	1.02	-
L_1	-	1.27	-	0.05

note 1:The diameter Ø b_2 is not controlled over zone L_1.

Packaging : Standard packaging is in tape and reel.

SGS-THOMSON MICROELECTRONICS

TPB SERIES

TRISIL

FEATURES

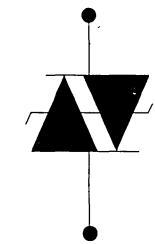
- BIDIRECTIONAL CROWBAR PROTECTION.
- BREAKDOWN VOLTAGE RANGE:
  From 62 V To 270 V.
- HOLDING CURRENT = I_H
  Suffix 12 = 120mA min.
  Suffix 18 = 180mA min.
- PEAK PULSE CURRENT :
  I_{PP} = 90 A, 10/1000 µs.

CB 429
(Plastic)

DESCRIPTION

The TPBxx series has been designed to protect telecommunication equipments against lightning and transient induced by AC power lines.

SCHEMATIC DIAGRAM



IN ACCORDANCE WITH FOLLOWING STANDARDS :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

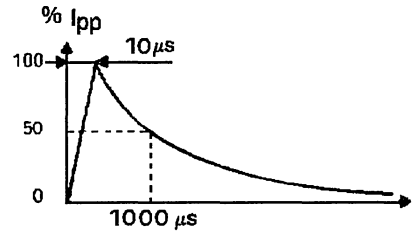
ABSOLUTE RATINGS (limiting values) (-40°C ≤ T_{amb} ≤ + 85°C)

Symbol	Parameter		Value	Unit
P	Power dissipation on infinite heatsink	T_{amb} = 50 °C	5	W
I_{PP}	Peak pulse current See note1	10/1000 µs 8/20 µs	90 150	A
I_{TSM}	Non repetitive surge peak on-state current	tp = 20 ms	50	A
di/dt	Critical rate of rise of on-state current	Non repetitive	100	A/µs
dv/dt	Critical rate of rise of off-state voltage	67% V_{BR}	5	KV/µs
T_{stg} T_j	Storage and operating junction temperature range		- 40 to + 150 + 150	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		230	°C

THERMAL RESISTANCES

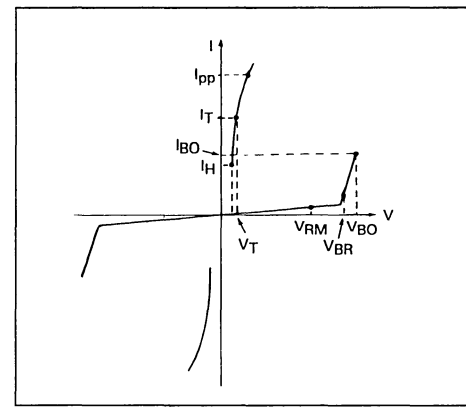
Symbol	Parameter	Value	Unit
R_{th} (j-l)	Junction to leads. On infinite heatsink.	20	°C/W
R_{th} (j-a)	Junction to ambient. On printed circuit. L_{lead} = 10 mm	75	°C/W

Note 1: 10/1000 µs wave form.



ELECTRICAL CHARACTERISTICS

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{BO}	Breakover voltage
I_H	Holding current
V_T	On-state voltage
I_{BO}	Breakover current
I_{PP}	Peak pulse current



ELECTRICAL CHARACTERISTICS

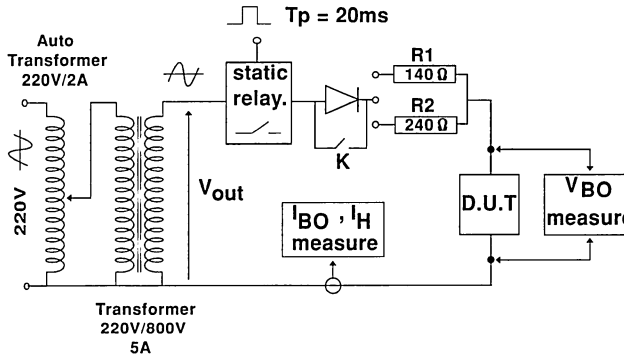
Type	I_{RM} @ V_{RM} max		V_{BR} @ I_R min		V_{BO} @ I_{BO} max note2	max	V_T max note3	C max note4	I_H min note2
	µA	V	V	mA	V	mA	V	pF	mA
P TPB62A - 12 or 18	2	56	62	1	82	300	3.5	300	
TPB62B - 12 or 18	2	56	62	1	75	300	3.5	300	
P TPB68A - 12 or 18	2	61	68	1	90	300	3.5	300	
TPB68B - 12 or 18	2	61	68	1	82	300	3.5	300	
(1) TPB75A - 12 or 18	2	67	75	1	100	300	3.5	300	
(1) TPB75B - 12 or 18	2	67	75	1	91	300	3.5	300	
(1) TPB82A - 12 or 18	2	74	82	1	109	300	3.5	300	
(1) TPB82B - 12 or 18	2	74	82	1	99	300	3.5	300	Suffix 12
(1) TPB91A - 12 or 18	2	82	91	1	121	300	3.5	300	for 120 mA.
(1) TPB91B - 12 or 18	2	82	91	1	110	300	3.5	300	
P TPB100A - 12 or 18	2	90	100	1	133	300	3.5	200	
TPB100B - 12 or 18	2	90	100	1	121	300	3.5	200	
P TPB110A - 12 or 18	2	99	110	1	147	300	3.5	200	
TPB110B - 12 or 18	2	99	110	1	133	300	3.5	200	
P TPB120A - 12 or 18	2	108	120	1	160	300	3.5	200	Suffix 18
TPB120B - 12 or 18	2	108	120	1	145	300	3.5	200	for 180 mA.
P TPB130A - 12 or 18	2	117	130	1	173	300	3.5	200	
TPB130B - 12 or 18	2	117	130	1	157	300	3.5	200	
(1) TPB150A - 12 or 18	2	135	150	1	200	300	7	150	
(1) TPB150B - 12 or 18	2	135	150	1	181	300	7	150	
(1) TPB160A - 12 or 18	2	144	160	1	213	300	7	150	
(1) TPB160B - 12 or 18	2	144	160	1	193	300	7	150	
P TPB180A - 12 or 18	2	162	180	1	240	300	7	150	
TPB180B - 12 or 18	2	162	180	1	217	300	7	150	
P TPB200A - 12 or 18	2	180	200	1	267	300	7	150	
TPB200B - 12 or 18	2	180	200	1	241	300	7	150	
P TPB220A - 12 or 18	2	198	220	1	293	300	7	150	
TPB220B - 12 or 18	2	198	220	1	265	300	7	150	
P TPB240A - 12 or 18	2	216	240	1	320	300	7	150	
TPB240B - 12 or 18	2	216	240	1	289	300	7	150	
P TPB270A - 12 or 18	2	243	270	1	360	300	7	150	
TPB270B - 12 or 18	2	243	270	1	325	300	7	150	

All parameters tested at 25°C, except where indicated.

P : Preferred device.
(1): These voltages are on request.

Note 2 : See the reference test circuit for I_H, I_{BO} and V_{BO} parameters.
Note 3 : Square pulse T_p = 1 ms - I_T = 5A.
Note 4 : V_R = 1V, F = 1MHz.

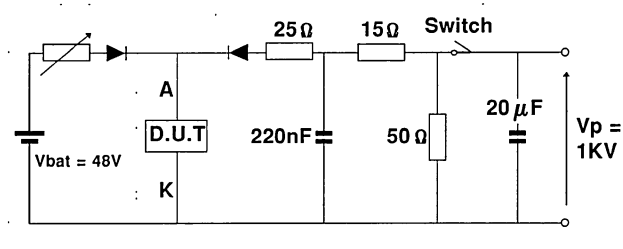
REFERENCE TEST CIRCUIT FOR I_H, I_{BO} and V_{BO} parameters :



TEST PROCEDURE :

- Pulse Test duration (Tp = 20ms):
  - For Bidirectional devices = Switch K is closed
  - For Unidirectional devices = Switch K is open.
- V_{OUT} Selection
  - Device with $V_{BR} \leq 150$ Volt
    - V_{OUT} = 250 V_{RMS}, R_1 = 140 Ω.
  - Device with $V_{BR} \geq 150$ Volt
    - V_{OUT} = 480 V_{RMS}, R_2 = 240 Ω.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT = GO - NOGO TEST.



Surge Generator
10/700 µsec
Vp =1KV / Ipp = 25A

This is a GO-NOGO Test which allows to confirm the holding current (I_H) level in a functional test circuit. This test can be performed if the reference test circuit can't be implemented.

TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.
2) Fire the D.U.T with a surge Current : Ipp = 25A , 10/700 µs.
3) The D.U.T will come back to the OFF-State withing a duration of 50 ms max.

Figure 1 : Non repetitive surge peak on state current versus number of cycles. (with sinusoïdal

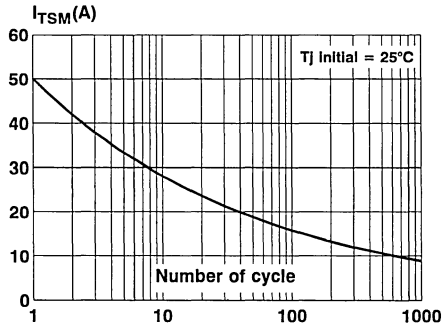
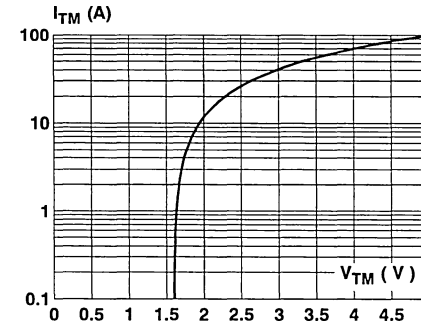
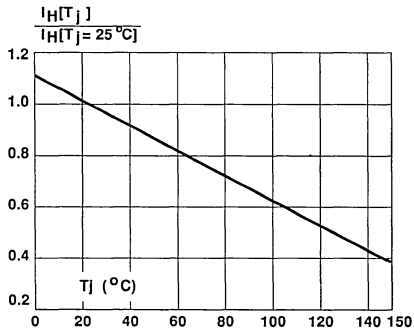


Figure 2 : On - state characteristics (typical values).

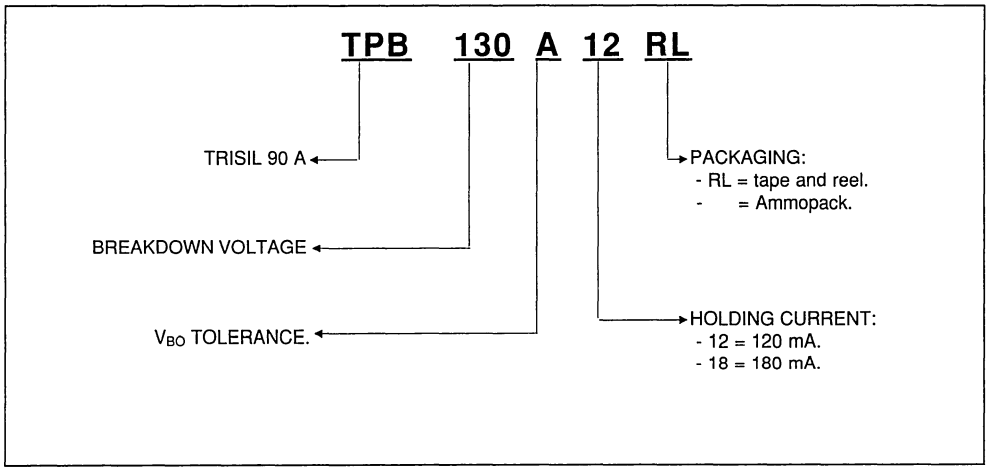


Note : For devices with $V_{BR} > 150$ V
The V_T value is twice that shown

Figure 3 : Relative variation of holding current versus junction temperature.



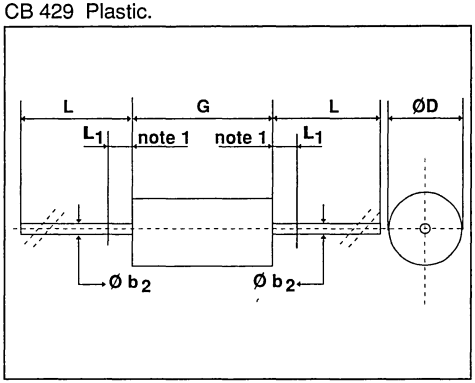
ORDER CODE



MARKING : Logo, Date Code, Part Number.

PACKAGE MECHANICAL DATA.

CB 429 Plastic.



Ref	Millimeters		Inches	
	min	max	min	max
Ø b_2	-	1.06	-	0.042
Ø D	-	5.1	-	0.20
G	-	9.8	-	0.386
L	26	-	1.024	-
L_1	-	1.27	-	0.050

note 1:The diameter Ø b_2 is not controlled over zone L_1.

Packaging : Standard packaging is in tape and reel.

SGS-THOMSON MICROELECTRONICS

TPB200S TPB245S/TPB265S

SURGE ARRESTORS

FEATURES

- SOLID STATE SURGE ARRESTOR PACKAGED IN AXIAL DIODE.
- VOLTAGE RANGE = 200 V TO 265 V
- TIGHT VOLTAGE TOLERANCE
- FAST RESPONSE TIME
- VERY LOW AND STABLE LEAKAGE CURRENT
- REPETITIVE SURGE CAPABILITY I_{PP} = 100 A, 10/1000 µs.
- FAIL-SAFE WHEN DESTROYED

CB429
Plastic

DESCRIPTION

Bidirectional device used for primary protection in telecom equipments.
Providing long service life, and adapted for sensitive electronic equipments protection.
If destroyed the component will continue to guarantee a protection with a permanent short circuit, meaning "fail save criteria" . This particular behaviour will also allow an easy failure detection on the line.

ABSOLUTE RATINGS (limiting values) - 40°C < T_{amb} < +80°C

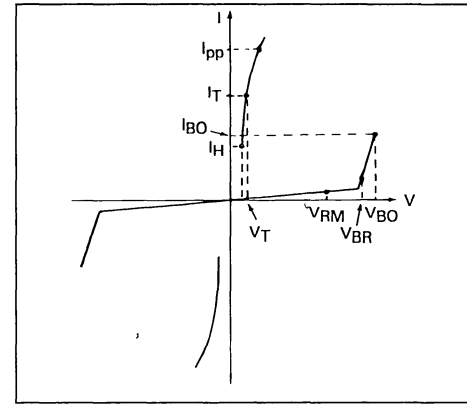
Symbol	Parameter		Value	Unit
I_{PP}	Peak Pulse Current.	10/1000 µs	100	A
		8/20 µs	200	A
	Fail Save Criteria.	8/20 µs	10	kA
I_{TSM}	Non Repetitive Surge Peak on-state Current. One cycle.	60 Hz	30	A
		50Hz	25	A
	Non Repetitive Surge Peak on-state Current F = 50 Hz.	1s	14	A
		2s	10	A
dv/dt	Critical Rate of Rise of on-state Voltage.	67% V_{BR}	10	kV/µs
T_L	Maximum Lead Temperature to Soldering During 10 s.		250	°C

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
RTH (j-a)	Junction-leads Thermal Resistance	20	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
VRM	Stand-off voltage
VBR	Breakdown voltage
VBO	Breakover voltage
IH	Holding current
VT	On-state voltage
IBO	Breakover current
IPP	Peak pulse current

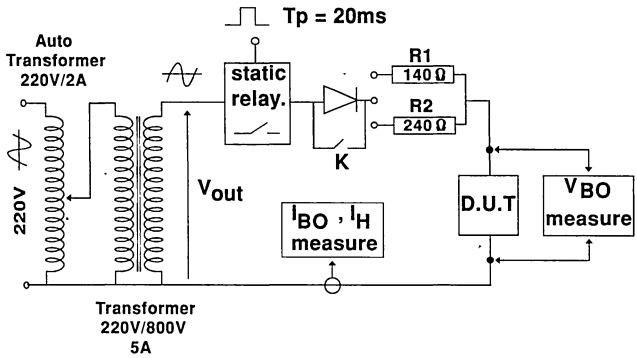


Types	I_R @ V_{RM} max		VBR @ I_R min		V_{BO} @ I_{BO} max	max	I_H min note1	V_T max note2	C max note3
	µA	V	V	mA	V	mA	mA	V	pF
TPB200S	10	170	200	1	265	600	260	3.5	200
TPB245S	10	210	245	1	350	600	260	3.5	200
TPB265S	10	225	265	1	400	600	260	3.5	200

All parameters tested at 25°C, except where indicated

Note 1 : See the reference test circuit for I_H, I_{BO} and V_{BO} parameters
Note 2 : Square pulse Tp = 500 µs - I_T = 5A.
Note 3 : V_R = 1V, F = 1MHz.

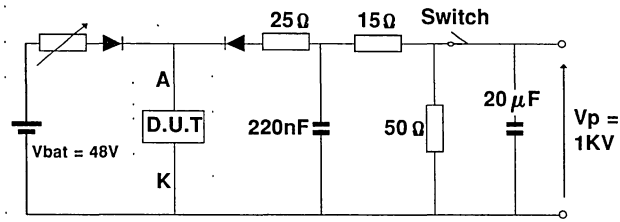
REFERENCE TEST CIRCUIT FOR I_H, I_{BO} and V_{BO} parameters :



TEST PROCEDURE :

- Pulse Test duration (Tp = 20ms):
  - For Bidirectional devices = Switch K is closed
  - For Unidirectional devices = Switch K is open.
- V_{OUT} Selection
  - Device with $V_{BR} \leq 150$ Volt
    - $V_{OUT} = 250\ V_{RMS}$, $R_1 = 140\ \Omega$.
  - Device with $V_{BR} \geq 150$ Volt
    - $V_{OUT} = 480\ V_{RMS}$, $R_2 = 240\ \Omega$.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT GO - NOGO TEST.



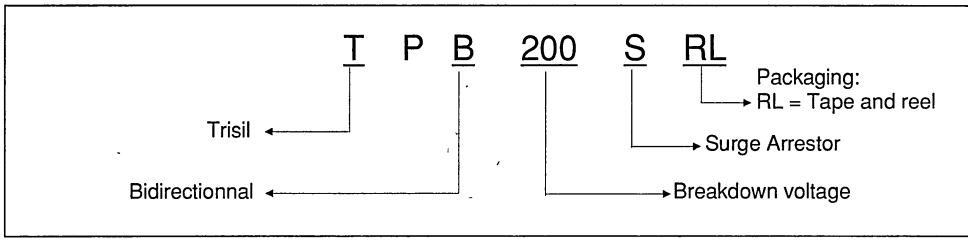
Surge Generator
10/700 μsec
Vp =1KV / Ipp = 25A

This is a GO-NOGO Test which allows to confirm the holding current (I_H) level in a functional test circuit. This test can be performed if the reference test circuit can't be implemented.

TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.
2) Fire the D.U.T with a surge Current : Ipp = 25A , 10/700 μs.
3) The D.U.T will come back to the OFF-State within a duration of 50 ms max.

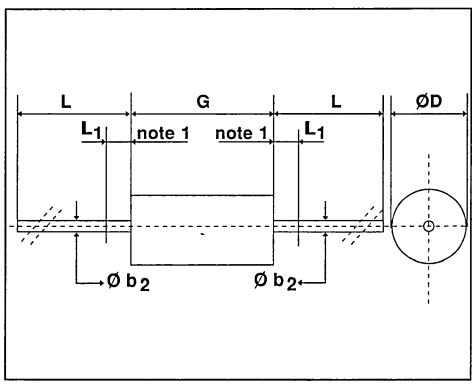
ORDER CODE



MARKING

Type	Marking
TPB200S TPB245S TPB265S	TPB200S TPB245S TPB265S

PACKAGE MECHANICAL DATA



Ref	Millimeters		Inches	
	min	max	min	max
Ø b2	-	1.06	-	0.042
Ø D	-	5.1	-	0.20
G	-	9.8	-	0.386
L	26	-	1.024	-
L1	-	1.27	-	0.050

note 1:The diameter Ø b2 is not controllec over zone L1.

Packaging : Products are supplied in tape and reel.

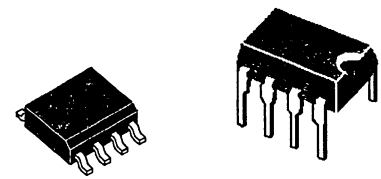
SGS-THOMSON MICROELECTRONICS

TPI80xxN/TPI120xxN

TRIBALANCED PROTECTION WITH LOW DYNAMIC V_{BO} FOR ISDN INTERFACES

FEATURES

- BIDIRECTIONAL TRIPLE PROTECTION.
- CROWBAR PROTECTION.
- PEAK PULSE CURRENT :
  I_{PP} = 30 A , 10/1000 µs.
- BREAKDOWN VOLTAGE:
  TPI80N = 80V
  TPI120N = 120V.
- AVAILABLE IN DIL8 AND SO8 PACKAGES.
- LOW DYNAMIC BREAKOVER VOLTAGE :
  TPI80N = 150V
  TPI120 = 200V



SO 8
(Plastic)

DIL 8
(Plastic)

DESCRIPTION: TRIBALANCED PROTECTION

Dedicated devices for ISDN interface and high speed data telecom lines protection. Equivalent to a triple TRISIL with low capacitance providing:

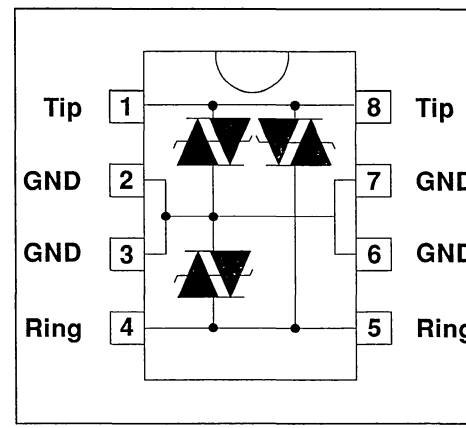
Low capacitance from lines to ground :
allowing high speed transmission without signal attenuation.

Good capacitance balance (Line A/Line B) in order to insure the longitudinal balance of the line.

Fixed breakdown voltage in both common and differential modes.

The same surge current capability in both common and differential modes.

SCHEMATIC DIAGRAM

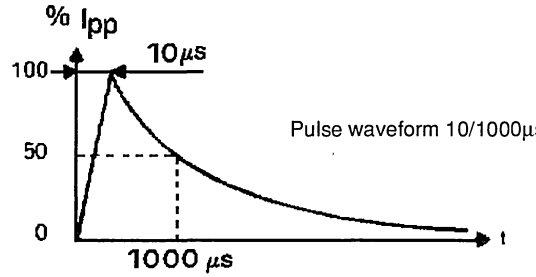


IN ACCORDANCE WITH FOLLOWING STANDARDS :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

ABSOLUTE RATINGS (limiting values) (-40°C ≤ Ta ≤ +85°C)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current	10/1000 µs 5/320 µs 2/10 µs	30 40 90	A
I_{TSM}	Non repetitive surge peak on-state current	tp = 10 ms tp = 1 s	5 3.5	A
di/dt	Critical rate of rise of on-state current	Non repetitive	100	A/µs
dv/dt	Critical rate of rise of off-state voltage	67% V_{BR}	5	KV/µs
T_{stg} T_j	Storage and operating junction temperature range		- 40 to + 150 150	°C °C



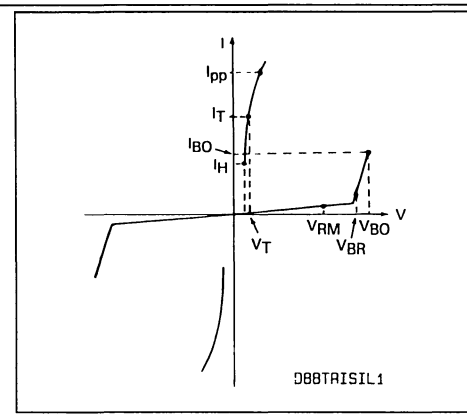
Pulse waveform 10/1000µs

THERMAL RESISTANCES

Symbol	Parameter		Value	Unit
R_{th} (j-a)	Junction to ambient	DIL 8 SO 8	125 171	°C/W °C/W

ELECTRICAL CHARACTERISTICS

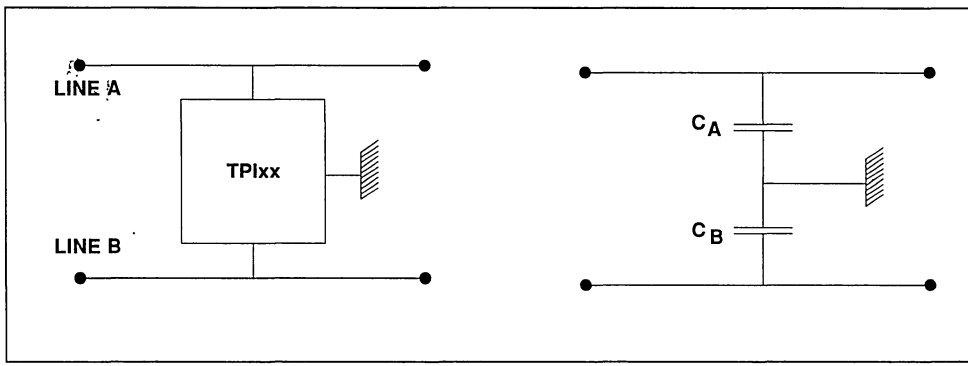
Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{BO}	Breakover voltage
I_H	Holding current
V_T	On-state voltage
I_{BO}	Breakover current
I_{PP}	Peak pulse current
V_F	Forward Voltage Drop



Types	I_R @ V_{RM} max		VBR @ I_R min		V_{BO} max note1	VBO typ note2	I_{BO} max note1	I_H min note3	V_T max note4
	µA	V	V	mA	V	V	mA	mA	V
TPI80xxN	10	70	80	1	120	150	800	150	8
TPI120xxN	10	105	120	1	180	200	800	150	8

Note 1 : See the reference test circuit for I_{BO} and V_{BO} parameters.
Note 2 : Surge test according CCITT 1.5kV,10/700 µs between Tip or Ring and ground.
Note 3 : See functional holding current test circuit.
Note 4 : Square pulse Tp = 500 ms - IT = 5A

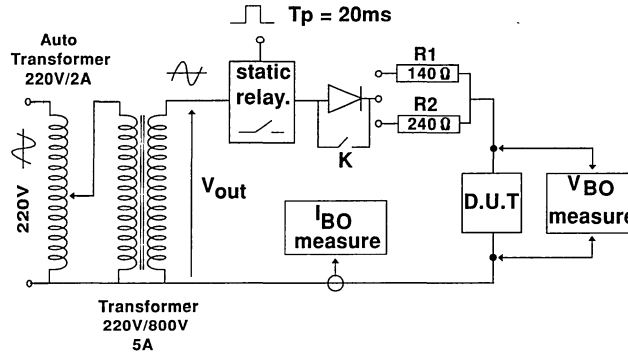
CAPACITANCES CHARACTERISTICS



CONFIGURATION	C_A (pf) max	C_B (pf) max	$C_A - C_B$ (pf) max
V_A =1V V_B =56V	70	50	30
V_A = 56V V_B= 1V	50	70	30

All parameters tested at 25°C, except where indicated

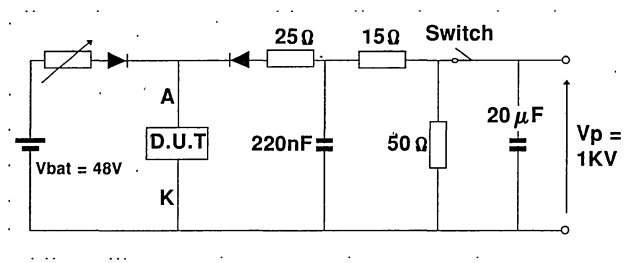
REFERENCE TEST CIRCUIT FOR I_{BO} and static V_{BO} parameters :



TEST PROCEDURE :

- Pulse Test duration (Tp = 20ms):
  - For Bidirectional devices = Switch K is closed
  - For Unidirectional devices = Switch K is open.
- V_{OUT} Selection
  - Device with $V_{BR} \leq 150$ Volt
    - $V_{OUT} = 250\ V_{RMS}$, $R_1 = 140\ \Omega$.
  - Device with $V_{BR} \geq 150$ Volt
    - $V_{OUT} = 480\ V_{RMS}$, $R_2 = 240\ \Omega$.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT = GO - NOGO TEST.



Surge Generator
10/700 μsec
Vp =1KV / Ipp = 25A

This is a functional test circuit which performs a GO-NOGO test on the holding current level I_H .

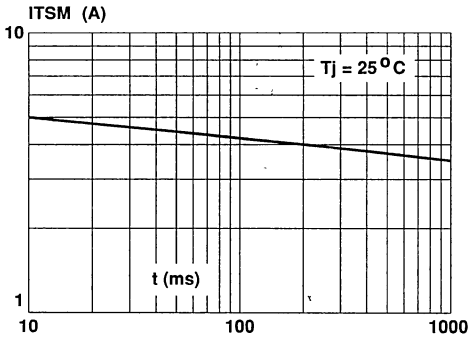
TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.

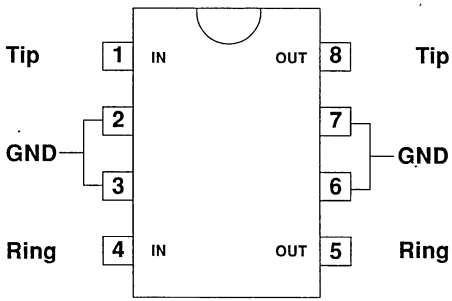
2) Fire the D.U.T with a surge Current : Ipp = 25A , 10/700 μs.

3) The D.U.T will come back to the OFF-State within a duration of 50 ms max.

Fig. 1 : Non repetitive surge peak on-state current. (with sinusoidal pulse : F =50Hz)



APPLICATION NOTE.



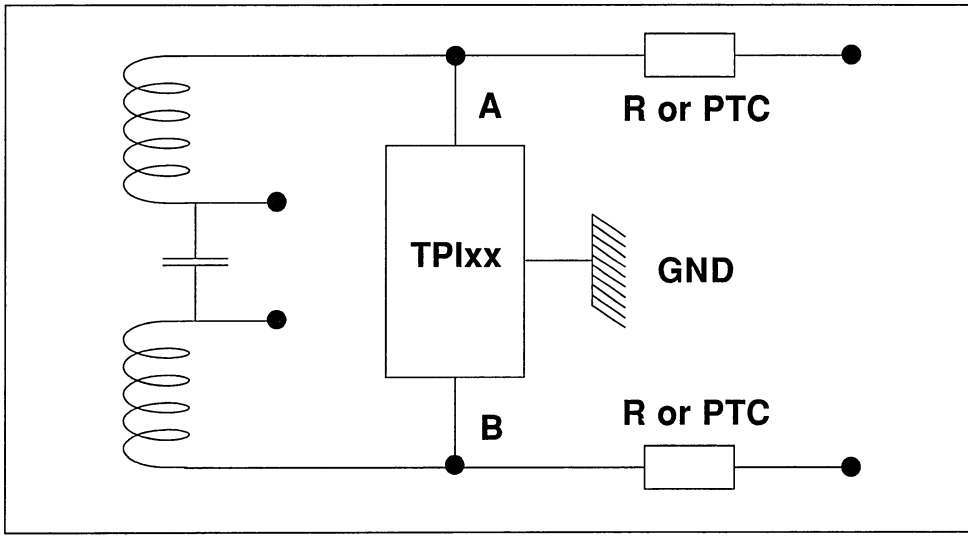
4- points structure lay-out.

1) Connect pins 2, 3, 6 and 7 to ground in order to guarantee a good surge current capability for long duration disturbances.

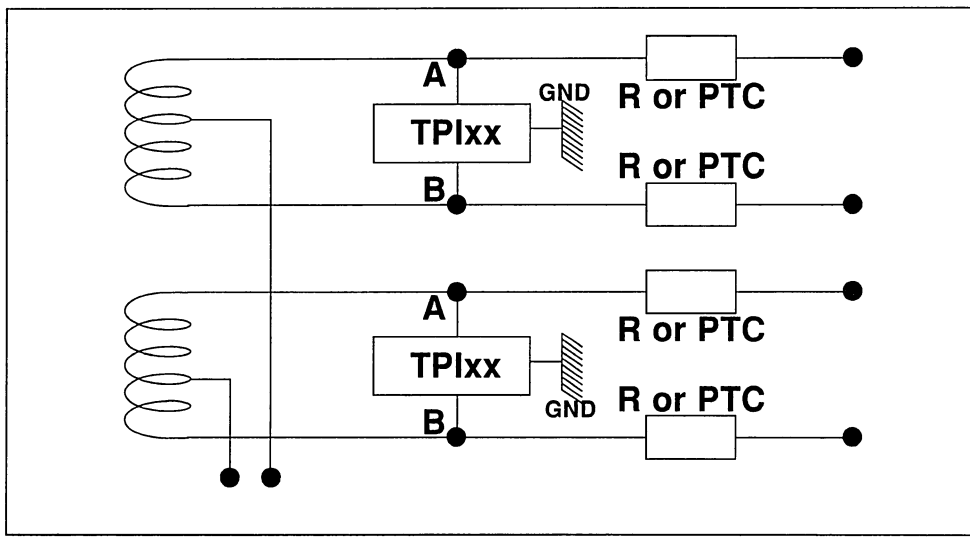
2) In order to take advantage of the "4-points structure" of the TPIxxxP, the tip and Ring lines have to cross through the device. in this case, the device will eliminate the overvoltages generated by the parasitic inductances of the wiring (Ldi/dt), especially for very fast Transients.

APPLICATION NOTE:

U INTERFACE PROTECTION

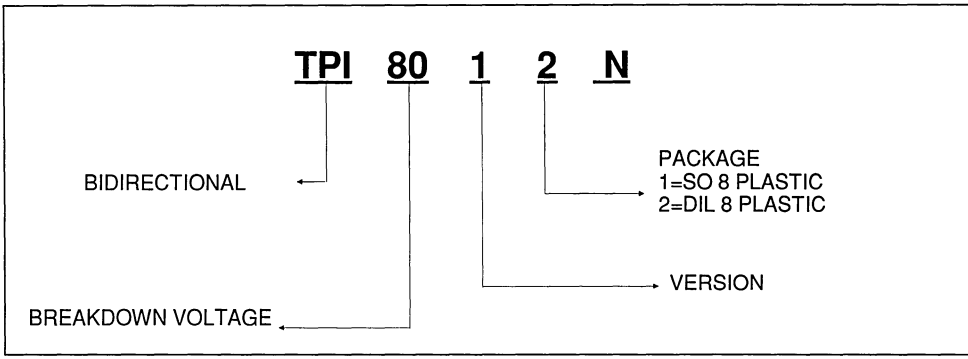


S INTERFACE PROTECTION



This component use an intemal structure resulting in symetrical characteristics with a good balanced behaviour.
This topology ensures the same breakdown voltage level for positive and negative surges in differential and common mode .

ORDER CODE



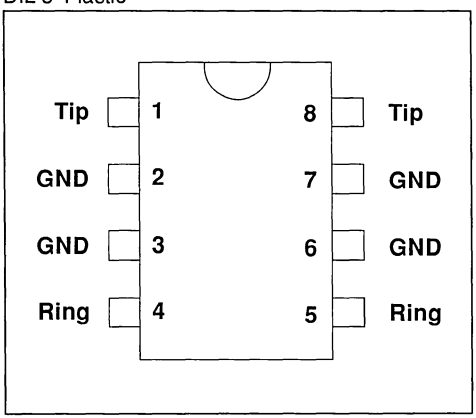
MARKING

Package	Type	Marking
SO8	TPI8011N TPI12011N	TP80N TP120N

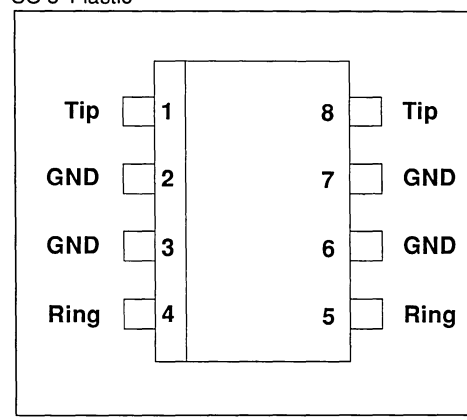
Package	Type	Marking
DIL8	TPI8012N TPI12012N	TP80N TP120N

CONNECTION DIAGRAM

DIL 8 Plastic



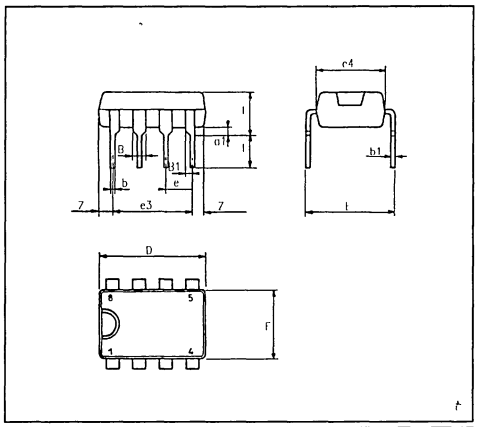
SO 8 Plastic



Packaging : Products supplied in antistatic tubes.

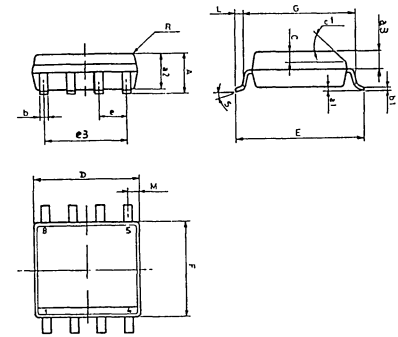
PACKAGE MECHANICAL DATA (in millimeters)

DIL 8 Plastic



REF.	DIMENSIONS					
	Millimetres			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.7			0.027		
B	1.39		1.65	0.054		0.065
B1	0.91		1.04	0.036		0.041
b		0.5			0.020	
b1	0.38		0.50	0.015		0.020
D			9.8			0.386
E		8.8			0.346	
e		2.54			0.100	
e4		7.52			0.300	
F			7.1			0.280
I			4.8			0.189
L	3.3			0.130		
Z	0.44		1.60	0.017		0.063

SO 8 Plastic



REF.	DIMENSIONS					
	Millimetres			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max)					

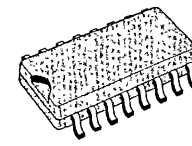
SGS-THOMSON MICROELECTRONICS

TSIxxxB5

TELEPHONE SET INTERFACE

FEATURES

- SINGLE DEVICE PROVIDING :
  DIODE BRIDGE
  BIDIRECTIONAL PROTECTION
- CROWBAR PROTECTION
- PEAK PULSE CURRENT :
  I_{PP} = 30A, 10/1000 µs
- VOLTAGE RANGE FROM 62V to 270V
- Maximum current : Io = 0.5A

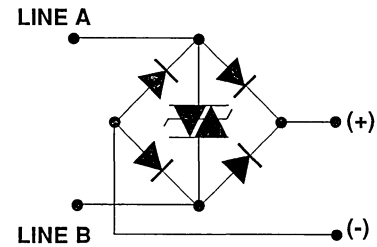


SO16
(Plastic)

IN COMPLIES WITH FOLLOWING :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

FUNCTIONAL DIAGRAM



ABSOLUTE RATINGS (limiting values) (-40°C ≤ Tamb ≤ +85°C)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current	10/1000 µs 5/310 µs 2/10 µs	30 40 75	A
Io	Maximum current		0.5	A
I_{TSM}	Non repetitive surge peak on-state current	tp = 10 ms tp = 1 s	5 3.5	A
dv/dt	Critical rate of rise of off-state voltage	67% V_{BR}	5	KV/µs
T_{stg} T_j	Storage and operating junction temperature range		- 40 to + 150 150	°C °C

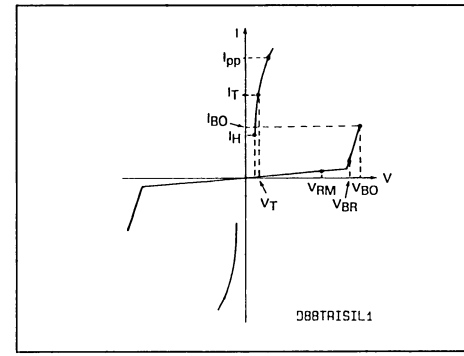
THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
R_{th} (j-a)	Junction-ambient thermal resistance - mounting on FR4	80	°C/W

ELECTRICAL CHARACTERISTICS

Tamb = 25°C

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{BO}	Breakover voltage
I_H	Holding current
V_T	On-state voltage
V_F	Forward Voltage Drop
I_{BO}	Breakover current
I_{PP}	Peak pulse current



PROTECTION DEVICE PARAMETERS

Types	I_R @ V_{RM} max		V_{BO} @ I_{BO} max note1	I_H min note1	I_{BO} min note1	I_{BO} max	V_T max note2
	µA	V	V	mA	mA	mA	V
TSI62B5	1 5	50 62	90	150	50	400	8
TSI120B5	1 5	50 120	180	150	50	400	8
TSI150B5	1 5	50 150	230	150	50	400	8
TSI180B5	1 5	50 180	250	150	50	400	8
TSI200B5	1 5	50 200	290	150	50	400	8
TSI270B5	1 5	50 270	380	150	50	400	8

DIODE BRIDGE PARAMETERS

Symbol	Test conditions	Value	Unit
V_F	I_F = 20mA note 3 I_F = 100mA note 3	0.9 1.0	V
C	note 4	200	pF

All parameters are tested at 25°C except where indicated

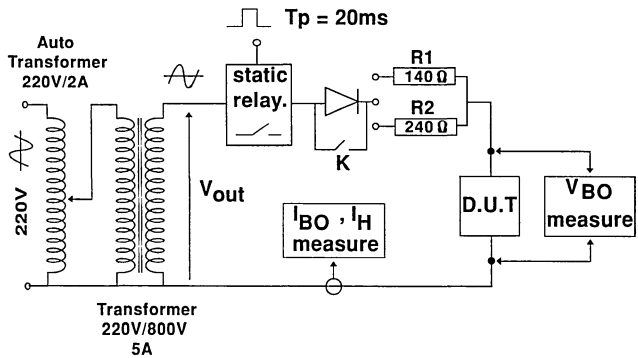
Note 1 : See test condidions for V_{BO}, I_{BO}, I_H parameters

Note 2 : Square pulse tp = 500 µs - I_T = 5A.

Note 3 : V_F is given for one diode

Note 4 : V_R = 0V, F = 1MHz.

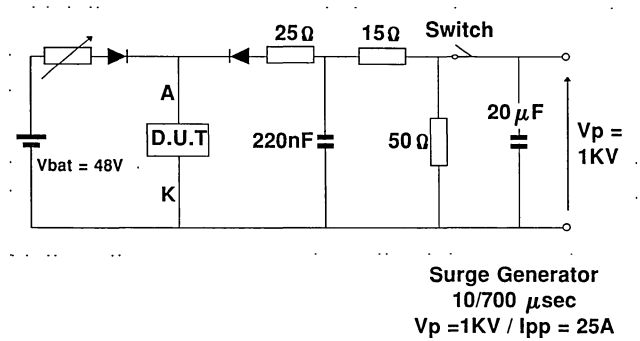
REFERENCE TEST CIRCUIT FOR I_{BO} and V_{BO} parameters :



TEST PROCEDURE :

- Pulse Test duration (Tp = 20ms):
  - For Bidirectional devices = Switch K is closed
  - For Unidirectional devices = Switch K is open.
- V_{OUT} Selection
  - Device with $V_{BR} \leq 150$ Volt
    - $V_{OUT} = 250\ V_{RMS}$, $R_1 = 140\ \Omega$.
  - Device with $V_{BR} \geq 150$ Volt
    - $V_{OUT} = 480\ V_{RMS}$, $R_2 = 240\ \Omega$.

FUNCTIONAL HOLDING CURRENT (I_H) TEST CIRCUIT = GO - NOGO TEST.



This test circuit performs a GO-NOGO test on the holding current I_H.

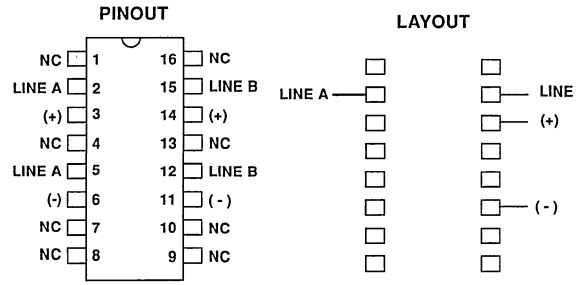
TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.

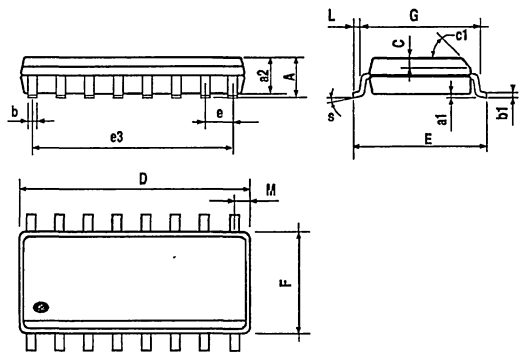
2) Fire the D.U.T with a surge Current : Ipp = 25A , 10/700 µs.

3) The D.U.T will come back to the OFF-State withing a duration of 50 ms max.

PINOUT CONFIGURATION AND LAYOUT RECOMMENDATIONS :



PACKAGE MECHANICAL DATA



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.2	0.004		0.008
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° max					
D	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.150		0.157
G	4.6		5.3	0.181		0.209
L	0.5		1.27	0.020		0.050
M			0.62			0.024
S	8° max					

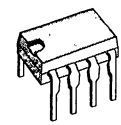
MARKING : LOGO, DATE CODE, DEVICE CODE.

DEVICE	TSI62B5	TSI120B5	TSI150B5	TSI180B5	TSI200B5	TSI270B5
MARKING	TSI62	TSI120	TSI150	TSI180	TSI200	TSI270

SPECIAL OP-AMPs and COMPARATORS DATASHEETS

HIGH PERFORMANCE DUAL OPERATIONAL AMPLIFIERS

- LOW POWER CONSUMPTION
- SHORT CIRCUIT PROTECTION
- LOW DISTORTION, LOW NOISE
- HIGH GAIN-BANDWIDTH PRODUCT
- HIGH CHANNEL SEPARATION



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

H
TO99
(Metal Can)

DESCRIPTION

The LS204 is a high performance dual operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth products.

The circuit presents very stable electrical characteristics over the entire supply voltage range, and is particularly intended for professional and telecom applications (active filters, etc).

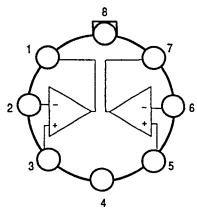
ORDER CODES

Part Number	Temperature Range	Package		
		H	N	D
LS204C	0°C, +70°C	•	•	•
LS204I	-40°C, +105°C	•	•	•
LS204M	-55°C, +125°C	•	•	•

204-01 TBL

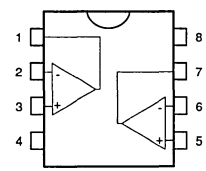
PIN CONNECTIONS (top views)

TO99



204-01 EPS

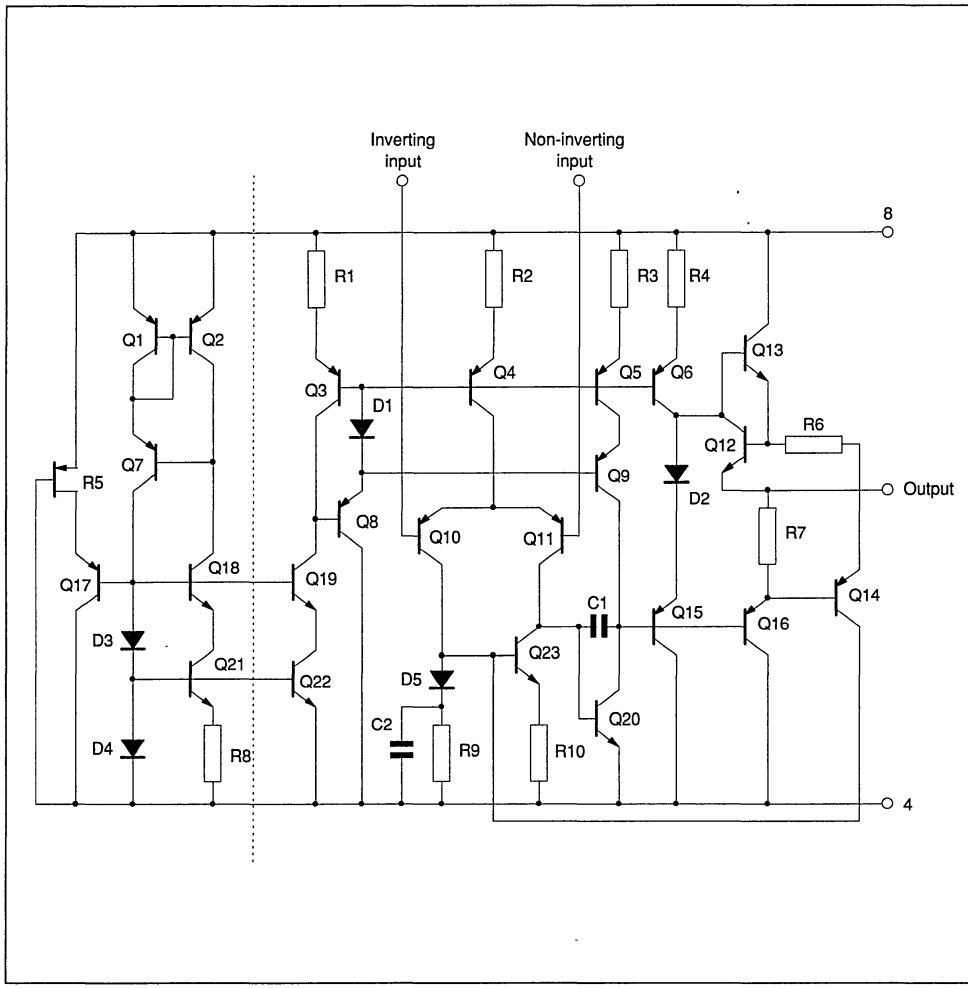
DIP8/SO8



204-02 EPS

1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output
8 - V_{CC}^+

SCHEMATIC DIAGRAM (1/2 LS204)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		±18	V
V_i	Input Voltage		$\pm V_{CC}$	
V_{id}	Differential Input Voltage		$\pm(V_{CC} - 1)$	
T_{oper}	Operating Temperature Range	LS204C LS204I LS204M	0 to +70 -40 to +105 -55 to +125	°C
P_{tot}	Power Dissipation at T_{amb} = 70°C		500	mW
T_j	Junction Temperature		150	°C
T_{stg}	Storage Temperature		-65 to 150	°C

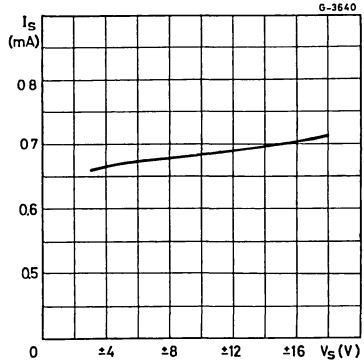
204-02.TBL

ELECTRICAL CHARACTERISTICS (V_{CC} = ±15V, T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	LS204I - LS204M			LS204C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{CC}	Supply Current			0.7	1.2		0.8	1.5	mA
I_{ib}	Input Bias Current			50	150		100	300	nA
		$T_{min} < T_{op} < T_{max}$.			300			700	nA
R_I	Input Resistance	f = 1kHz		1			0.5		MΩ
V_{io}	Input Offset Voltage	$R_s \leq 10k\Omega$		0.5	2.5		0.5	3.5	mV
		$R_s \leq 10k\Omega$ $T_{min} < T_{op} < T_{max}$.			3.5			5	mV
DV_{io}	Input Offset Voltage Drift	$R_s \leq 10k\Omega$ $T_{min.} < T_{op} < T_{max}$.		5			5		µV/°C
I_{io}	Input Offset Current			5	20		12	50	nA
		$T_{min.} < T_{op} < T_{max}$.			40			100	nA
DI_{io}	Input Offset Current Drift	$T_{min.} < T_{op} < T_{max}$.		0.08			0.1		$\frac{nA}{°C}$
I_{os}	Output Short Circuit Current			23			23		mA
A_{vd}	Large Signal Voltage Gain	$T_{min.} < T_{op} < T_{max}$. R_L = 2kΩ V_{CC} = ±15V V_{CC} = ±4V	90	100 95		86	100 95		dB
GBP	Gain-bandwidth Product	f = 100kHz	1.8	3		1.5	2.5		MHz
e_n	Equivalent Input Noise Voltage	f = 1kHz R_s = 50Ω R_s = 1kΩ R_s = 10kΩ		8 10 18	15		10 12 20		$\frac{nV}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	A_V = 20dB R_L = 2kΩ V_O = 2V_{PP} f = 1kHz		0.03	0.1		0.03	0.1	%
±V_{opp}	Output Voltage Swing	R_L = 2kΩ V_{CC} = ±15V V_{CC} = ±4V	±13	±3		±13	±3		V
V_{opp}	Large Signal Voltage Swing	R_L = 10kΩ f = 10kHz		28			28		V_{PP}
SR	Slew Rate	Unity Gain, R_L = 2kΩ	0.8	1.5			1		V/µs
CMR	Common Mode Rejection Ratio	V_{ic} = 10V $T_{min.} < T_{op} < T_{max}$.	90			86			dB
SVR	Supply Voltage Rejection Ratio	V_{ic} = 1V f = 100Hz $T_{min.} < T_{op} < T_{max}$.	90			86			dB
V_{O1}/V_{O2}	Channel Separation	f = 1kHz	100	120			120		dB

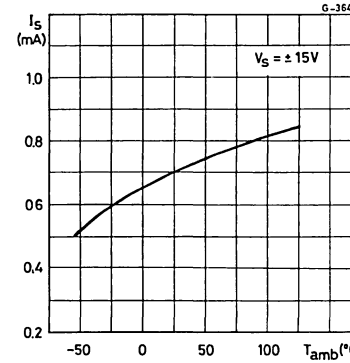
204-03 TBL

Figure 1 : Supply Current versus Supply Voltage



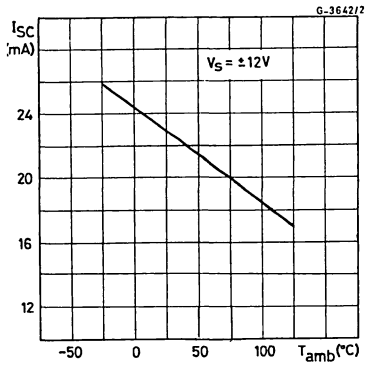
204-04 EPS

Figure 2 : Supply Current versus Ambient Temperature



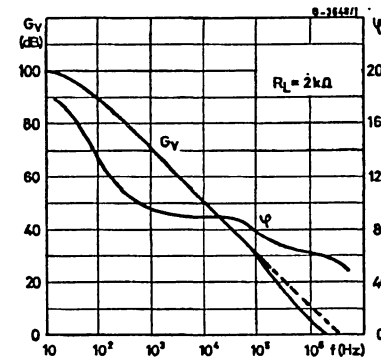
204-05 EPS

Figure 3 : Output Short Circuit Current versus Ambient Temperature



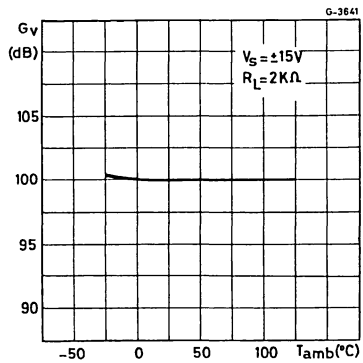
204-06 EPS

Figure 4 : Open Loop Frequency and Phase Response



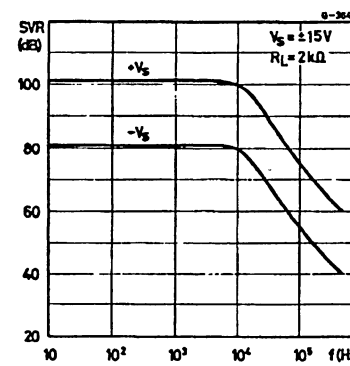
204-07 EPS

Figure 5 : Output Loop Gain versus Ambient Temperature



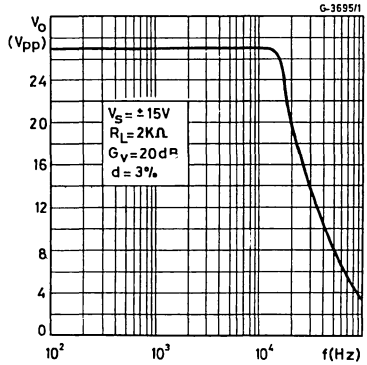
204-08 EPS

Figure 6 : Supply Voltage Rejection versus Frequency



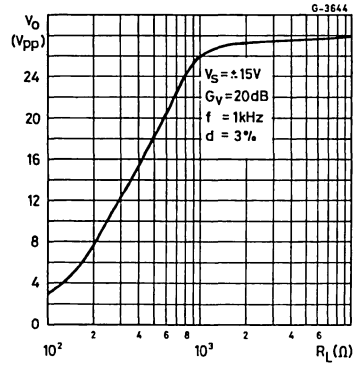
204-09 EPS

Figure 7 : Large Signal Frequency Response



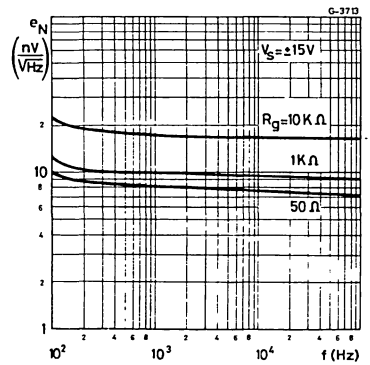
204-10 EPS

Figure 8 : Output Voltage Swing versus Load Resistance



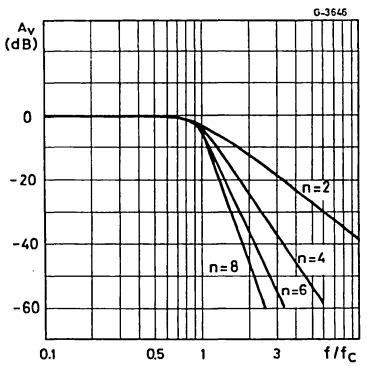
204-11 EPS

Figure 9 : Total Input Noise versus Frequency



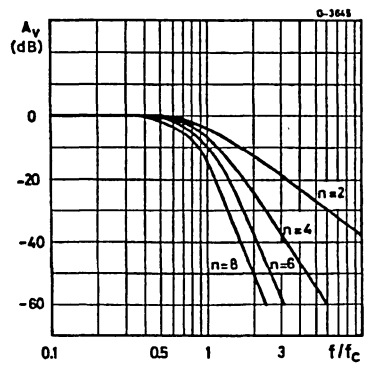
204-12 EPS

Figure 10 : Amplitude Response



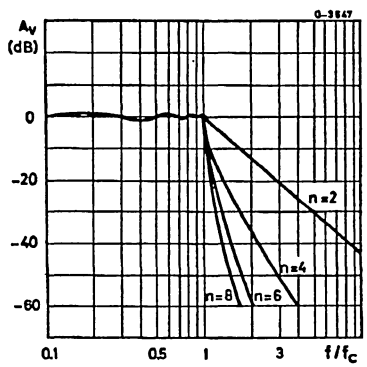
204-13 EPS

Figure 11 : Amplitude Response



204-14 EPS

Figure 12 : Amplitude Response (±1dB ripple)



204-15 EPS

APPLICATION INFORMATION : Active low-pass filter

BUTTERWORTH

The Butterworth is a "maximally flat" amplitude response filter. Butterworth filters are used for filtering signals in data acquisition systems to prevent aliasing errors in sampled-data applications and for general purpose low-pass filtering.

The cut-off frequency f_c, is the frequency at which the amplitude response is down 3dB. The attenuation rate beyond the cutoff frequency is n6 dB per octave of frequency where n is the order (number of poles) of the filter.

Other characteristics :

- Flattest possible amplitude response.
- Excellent gain accuracy at low frequency end of passband.

BESSEL

The Bessel is a type of "linear phase" filter. Because of their linear phase characteristics, these filters approximate a constant time delay over a limited frequency range. Bessel filters pass transient waveforms with a minimum of distortion. They are also used to provide time delays for low pass filtering of modulated waveforms and as a "running average" type filter.

The maximum phase shift is $\frac{-n\Pi}{2}$ radians where n is the order (number of poles) of the filter. The cut-off frequency fc, is defined as the frequency at which the phase shift is one half of this value. For accurate delay, the cut-off frequency should be twice the maximum signal frequency.

The following table can be used to obtain the -3dB frequency of the filter.

	2 pole	4 Pole	6 Pole	8 Pole
–3dB Frequency	$0.77f_c$	$0.67f_c$	$0.57f_c$	$0.50f_c$

Other characteristics :

- Selectivity not as great as Chebyschev or Butterworth.
- Very little overshoot response to step inputs.
- Fast rise time.

CHEBYSCHEV

Chebyschev filters have greater selectivity than either Bessel or Butterworth at the expense of ripple in the passband.

Chebyschev filters are normally designed with peak-to-peak ripple values from 0.2dB to 2dB.

Increased ripple in the passband allows increased attenuation above the cut-off frequency.

The cut-off frequency is defined as the frequency at which the amplitude response passes through the specified maximum ripple band and enters the stop band.

Other characteristics :

- Greater selectivity
- Very non-linear phase response
- High overshoot response to step inputs

The table below shows the typical overshoot and settling time response of the low pass filters to a step input.

	Number of Poles	Peak Overshoot	Settling Time (% of final value)		
		% Overshoot	±1%	±0 .1%	±0 0.1%
Butterworth	2	4	$1.1/f_c$sec.	$1.7/f_c$sec.	$1.9/f_c$sec.
	4	11	$1.7/f_c$	$2.8/f_c$	$3.8/f_c$
	6	14	$2.4/f_c$	$3.9/f_c$	$5.0/f_c$
	8	16	$3.1/f_c$	$5.1/f_c$	$7.1/f_c$
Bessel	2	0.4	$0.8/f_c$	$1.4/f_c$	$1.7/f_c$
	4	0.8	$1.0/f_c$	$1.8/f_c$	$2.4/f_c$
	6	0.6	$1.3/f_c$	$2.1/f_c$	$2.7/f_c$
	8	0.3	$1.6/f_c$	$2.3/f_c$	$3.2/f_c$
Chebyschev (ripple ±0.25dB)	2	11	$1.1/f_c$	$1.6/f_c$	–
	4	18	$3.0/f_c$	$5.4/f_c$	–
	6	21	$5.9/f_c$	$10.4/f_c$	–
	8	23	$8.4/f_c$	$16.4/f_c$	–
Chebyschev (ripple ±1dB)	2	21	$1.6/f_c$	$2.7/f_c$	–
	4	28	$4.8/f_c$	$8.4/f_c$	–
	6	32	$8.2/f_c$	$16.3/f_c$	–
	8	34	$11.6/f_c$	$24.8/f_c$	–

204-04 TBL

Design of 2nd order active low pass filter (Sallen and Key configuration unity gain-op-amp)

Fixed R = R1 = R2, we have (see fig. 13).

$$C1 = \frac{1}{R}\frac{\xi}{\omega_c}$$

$$C2 = \frac{1}{R}\frac{1}{\xi\omega_c}$$

The diagram of fig.14 shows the amplitude response for different values of damping factor ξ in 2nd order filters.

Figure 13 : Filter Configuration

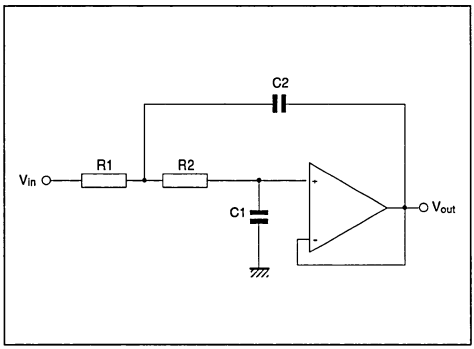
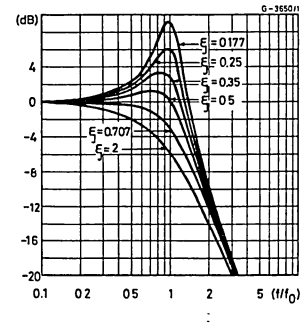


Figure 14 : Filter Respons versus Damping Factor



Three parameters are needed to characterize the frequency and phase response of a 2nd order active filter : the gain (G_V), the damping factor (ξ) or the Q-factor ($Q = (2\xi)^{-1}$), and the cutoff frequency (f_c).

The higher order responses are obtained with a series of 2nd order sections. A simple RC section is introduced when an odd filter is required.

The choice of 'ξ' (or Q-factor) determines the filter response (see table 1).

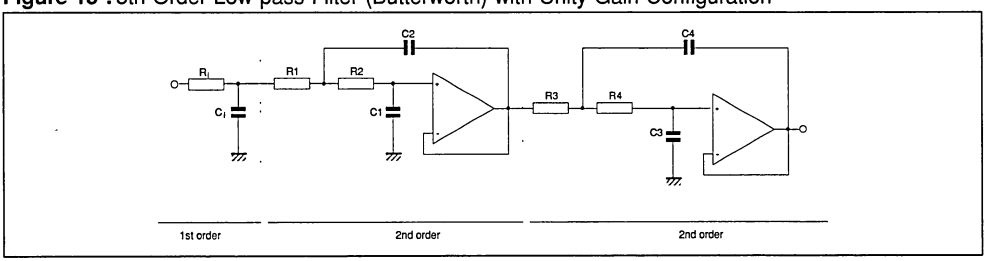
Table 1

Filter Response	ξ	Q	Cutoff Frequency f_c
Bessel	$\frac{\sqrt{3}}{2}$	$\frac{\sqrt{1}}{3}$	Frequency at which Phase Shift is -90°C
Butterworth	$\frac{\sqrt{2}}{2}$	$\frac{\sqrt{1}}{2}$	Frequency at which G_V = -3dB
Chebyschev	$\frac{\sqrt{2}}{2}$	$\frac{\sqrt{1}}{2}$	Frequency at which the amplitude response passes through specified max. ripple band and enters the stop band.

204-05 TBL

EXAMPLE

Figure 15 : 5th Order Low-pass Filter (Butterworth) with Unity Gain Configuration



In the circuit of fig. 15, for f_c = 3.4kHz and $R_i = R_1 = R_2 = R_3 = R_4$ = 10kΩ, we obtain :

$$C_i = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\Pi f_C} = 6.33nF$$

$$C_1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\Pi f_C} = 1.97nF$$

$$C_2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\Pi f_C} = 8.20nF$$

$$C_3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\Pi f_C} = 1.45nF$$

$$C_4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2\Pi f_C} = 15.14nF$$

The attenuation of the filter is 30dB at 6.8kHz and better than 60dB at 15kHz.

The same method, referring to Tab. 2 and fig. 16, is used to design high-pass filter. In this case the damping factor is found by taking the reciprocal of the numbers in Tab. 2. For f_c = 5kHz and $C_i = C_1 = C_2 = C_3 = C_4$ = 1nF we obtain :

$$R_i = \frac{1}{0.354} \cdot \frac{1}{C} \cdot \frac{1}{2\Pi f_C} = 25.5k\Omega$$

$$R_1 = \frac{1}{0.421} \cdot \frac{1}{C} \cdot \frac{1}{2\Pi f_C} = 75.6k\Omega$$

$$R_2 = \frac{1}{1.753} \cdot \frac{1}{C} \cdot \frac{1}{2\Pi f_C} = 18.2k\Omega$$

$$R_3 = \frac{1}{0.309} \cdot \frac{1}{C} \cdot \frac{1}{2\Pi f_C} = 103k\Omega$$

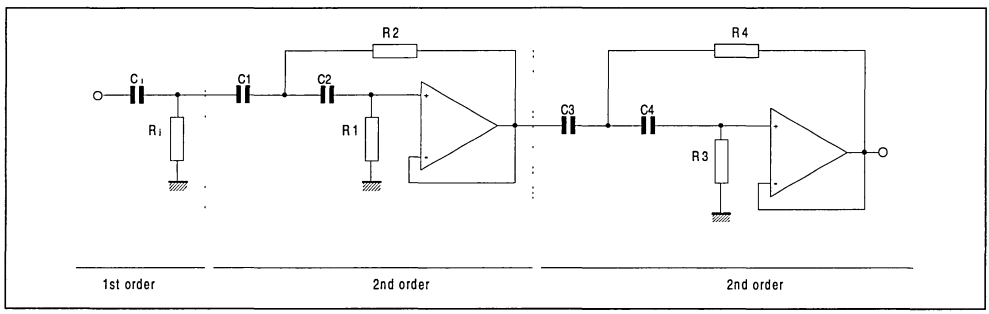
$$R_4 = \frac{1}{3.325} \cdot \frac{1}{C} \cdot \frac{1}{2\Pi f_C} = 9.6k\Omega$$

Table 2 : Damping Factor for Low-pass Butterworth Filters

Order	C_i	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
2		0.707	1.41						
3	1.392	0.202	3.54						
4		0.92	1.08	0.38	2.61				
5	1.354	0.421	1.75	0.309	3.235				
6		0.966	1.035	0.707	1.414	0.259	3.86		
7	1.336	0.488	1.53	0.623	1.604	0.222	4.49		
8		0.98	1.02	0.83	1.20	0.556	1.80	0.195	5.125

204-06 TBL

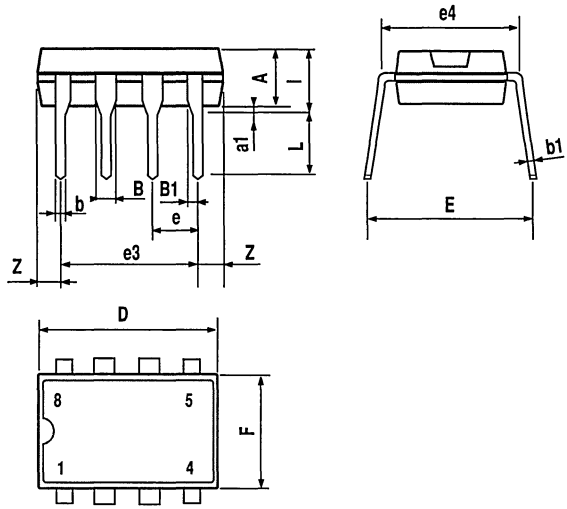
Figure 16 : 5th Order High-pass Filter (Butterworth) with Unity Gain Configuration



204-19 EPS

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP



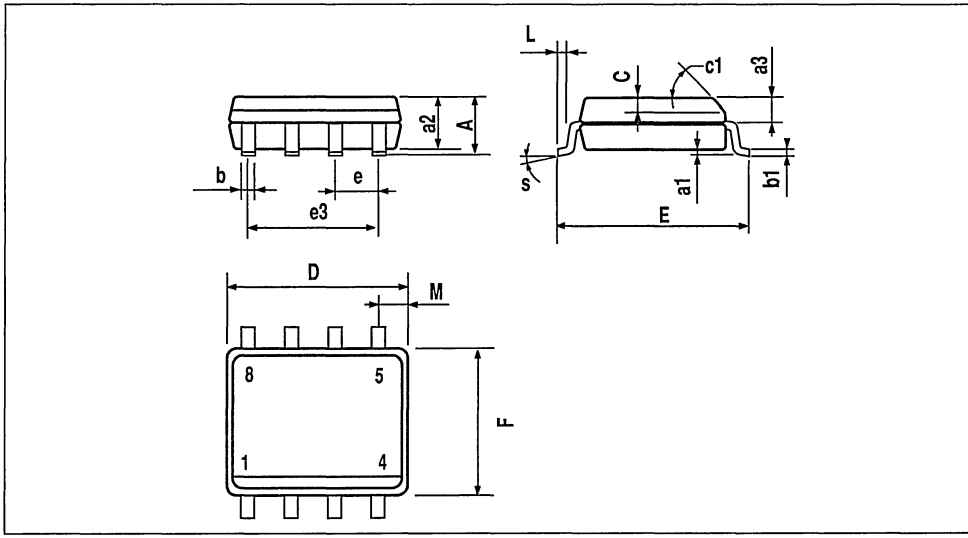
PM-DIP8.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0260
i			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

DIP8 TBL

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC MICROPACKAGE (SO)

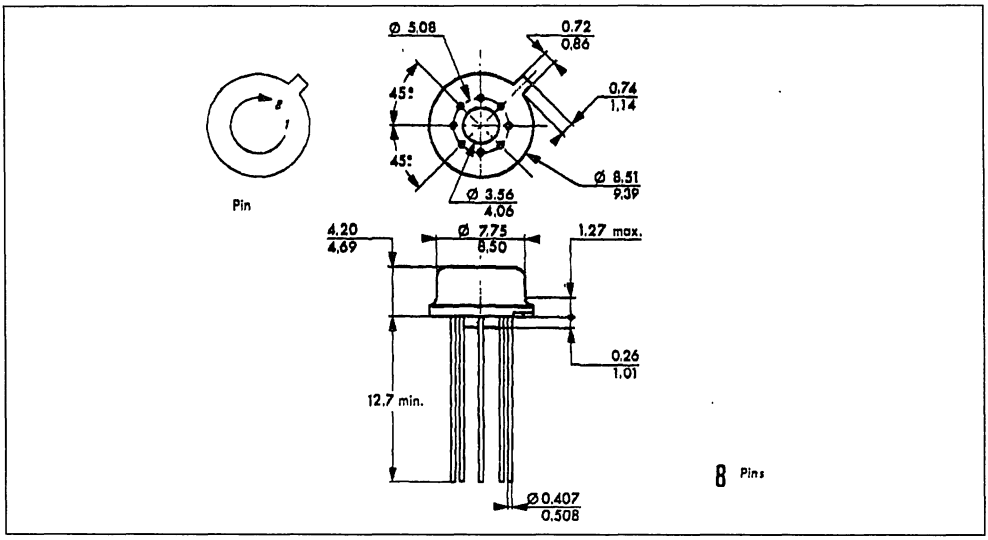


Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

SO8.TBL

PACKAGE MECHANICAL DATA

8 PINS - METAL CAN TO99

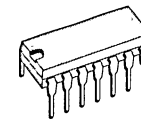


PM-TO99.IMG

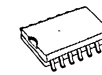
ORDER CODE

HIGH PERFORMANCE QUAD OPERATIONAL AMPLIFIERS

- SINGLE OR SPLIT SUPPLY OPERATION
- LOW POWER CONSUMPTION
- SHORT CIRCUIT PROTECTION
- LOW DISTORTION, LOW NOISE
- HIGH GAIN-BANDWIDTH PRODUCT
- HIGH CHANNEL SEPARATION



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

DESCRIPTION

The LS404 is a high performance quad operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth products.

The circuit presents very stable electrical characteristics over the entire supply voltage range, and it particularly intended for professional and telecom applications (active filters, etc).

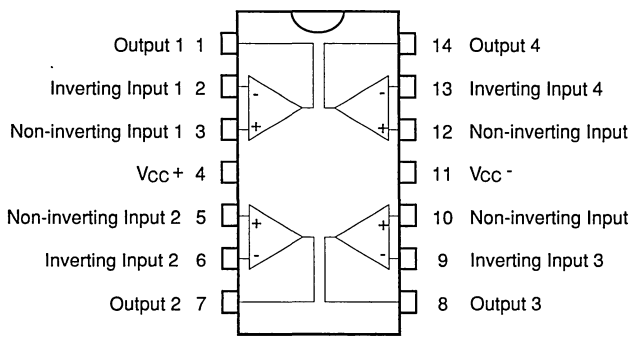
The patented input stage circuit allows small input signal swings below the negative supply voltage and prevents phase inversion when the inputs is over driver.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
LS404C	0°C, +70°C	•	•
LS404I	-40°C, +105°C	•	•
LS404M	-55°C, +125°C	•	•

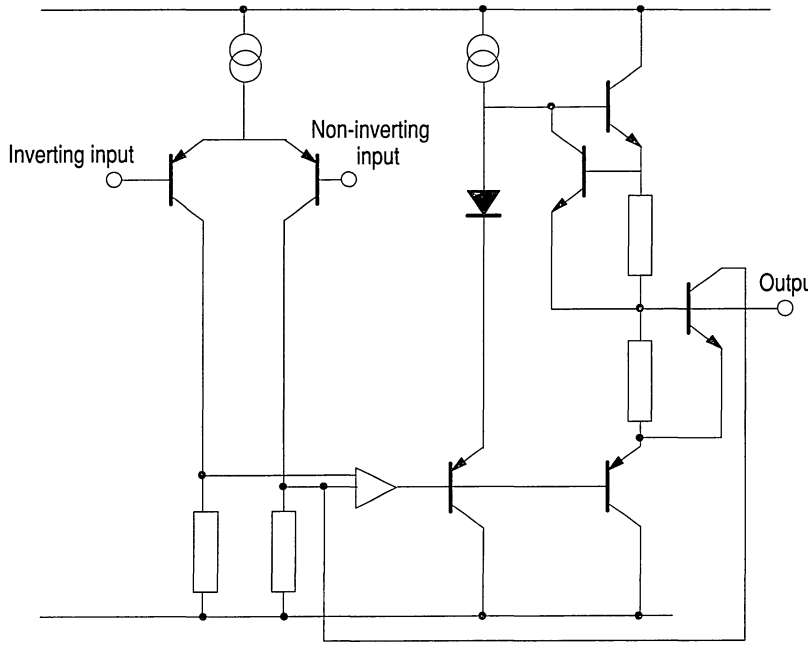
404-01.TBL

PIN CONNECTIONS (top view)



404-01.EPS

EQUIVALENT SCHEMATIC DIAGRAM (1/4 LS404)



404-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		±18	V
V_i	Input Voltage	(positive) (negative)	$+V_{CC}$ $-V_{CC}$ - 0.5	V
V_{id}	Differential Input Voltage		± (V_{CC} - 1)	
T_{oper}	Operating Temperature Range	LS404C LS404I LS404M	0 to +70 -40 to +105 -55 to +125	°C
P_{tot}	Power Dissipation at T_{amb} = 70°C		400	mW
T_{stg}	Storage Temperature		-65 to 150	°C

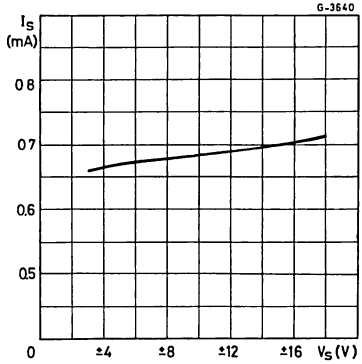
404-02.TBL

ELECTRICAL CHARACTERISTICS (V_{CC} = ±15V, T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	LS404I - LS404M			LS404C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{CC}	Supply Current			1.3	2		1.5	3	mA
I_{ib}	Input Bias Current			50	200		100	300	nA
R_i	Input Resistance	f = 1kHz		1			1		MΩ
V_{io}	Input Offset Voltage	$R_s \leq 10k\Omega$		0.7	2.5		0.5	5	mV
DV_{io}	Input Offset Voltage Drift	$R_s \leq 10k\Omega$ $T_{min.} < T_{op} < T_{max.}$		5			5		µV/°C
I_{io}	Input Offset Current			10	40		20	80	nA
DI_{io}	Input Offset Current Drift	$T_{min.} < T_{op} < T_{max.}$		0.08			0.1		$\frac{nA}{°C}$
I_{os}	Output Short Circuit Current			23			23		mA
A_{vd}	Large Signal Voltage Gain	R_L = 2kΩ V_{CC} = ±15V V_{CC} = ±4V	90	100 95		86	100 95		dB
GBP	Gain-bandwidth Product	f = 100kHz R_L = 2k C_L = 100pF	1.8	3		1.5	2.5		MHz
e_n	Equivalent Input Noise Voltage	f = 1kHz R_s = 50Ω R_s = 1kΩ R_s = 10kΩ		8 10 18	15		10 12 20		$\frac{nV}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	Unity Gain R_L = 2kΩ, V_O = $2V_{pp}$ f = 1kHz f = 20kHz		0.01 0.03	0.4		0.01 0.03		%
$\pm V_{opp}$	Output Voltage Swing	R_L = 2kΩ V_{CC} = ±15V V_{CC} = ±4V	±13	 ±3		±13	 ±3		V
V_{opp}	Large Signal Voltage Swing	f = 10kHz R_L = 10kΩ R_L = 1kΩ		22 20			22 20		V_{PP}
SR	Slew Rate	Unity Gain, R_L = 2kΩ	0.8	1.5			1		V/µs
CMR	Common Mode Rejection Ratio	V_{ic} = 10V	90	94		80	90		dB
SVR	Supply Voltage Rejection Ratio	V_{ic} = 1V f = 100Hz	90	94		86	90		dB
V_{O1}/V_{O2}	Channel Separation	f = 1kHz	100	120			120		dB

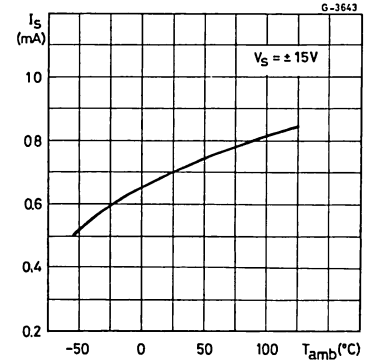
404-03.TBL

Figure 1: Supply Current versus Supply Voltage



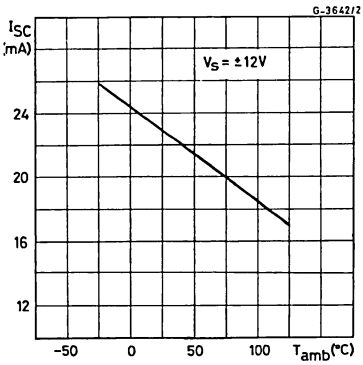
404-03 EPS

Figure 2 : Supply Current versus Ambient Temperature



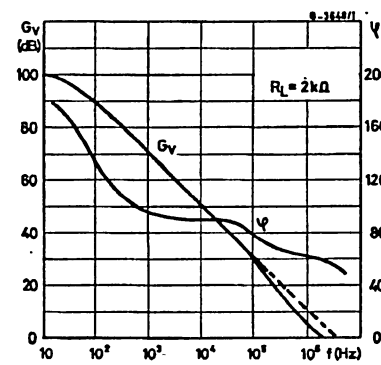
404-04 EPS

Figure 3 : Output Short Circuit Current versus Ambient Temperature



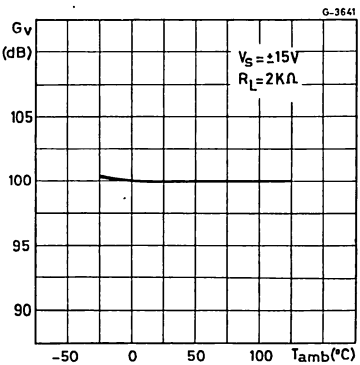
404-05 EPS

Figure 4 : Open Loop Frequency and Phase Response



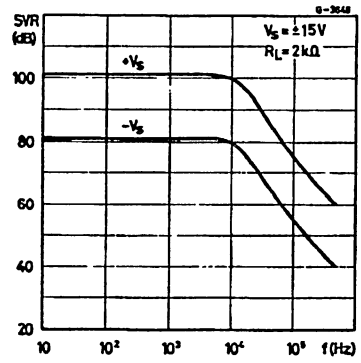
404-06 EPS

Figure 5 : Output Loop Gain versus Ambient Temperature



404-07 EPS

Figure 6 : Supply Voltage Rejection versus Frequency



404-08 EPS

Figure 7: Large Signal Frequency Response

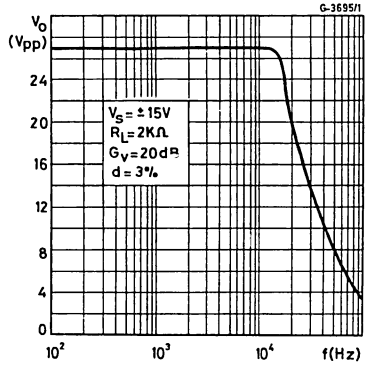


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Figure 8 : Output Voltage Swing versus Load Resistance

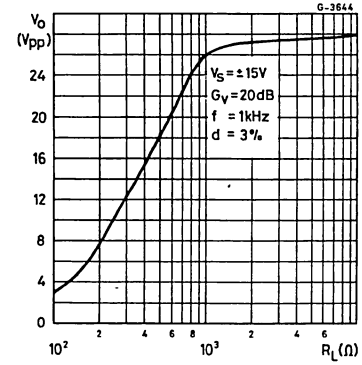

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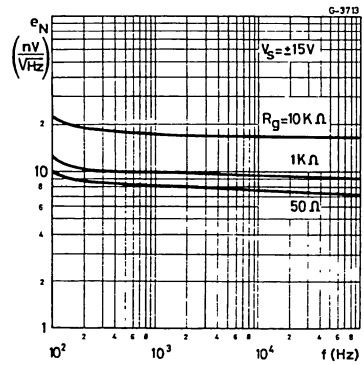
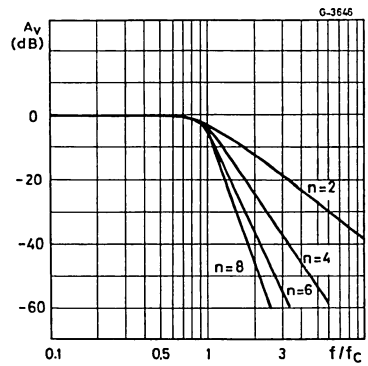
Figure 9 : Total Input Noise versus Frequency



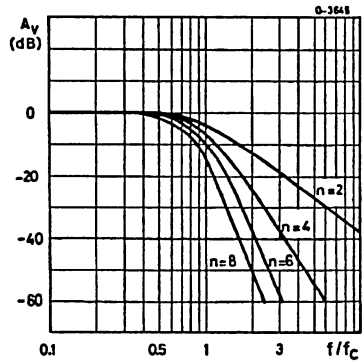
404-11.EPS

Figure 10 : Amplitude Response



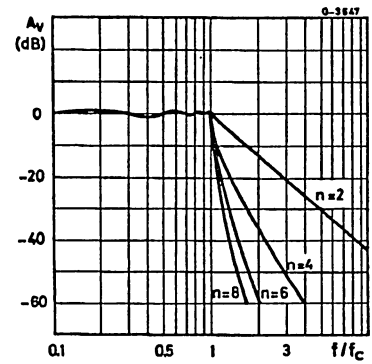
404-12.EPS

Figure 11 : Amplitude Response



404-13.EPS

Figure 12 : Amplitude Response (±1dB ripple)



404-14.EPS

APPLICATION INFORMATION : Active low-pass filter

BUTTERWORTH

The Butterworth is a "maximally flat" amplitude response filter. Butterworth filters are used for filtering signals in data acquisition systems to prevent aliasing errors in sampled-data applications and for general purpose low-pass filtering.

The cut-off frequency f_c, is the frequency at which the amplitude response is down 3dB. The attenuation rate beyond the cutoff frequency is -n6 dB per octave of frequency where n is the order (number of poles) of the filter.

Other characteristics :

- Flattest possible amplitude response.
- Excellent gain accuracy at low frequency end of passband.

BESSEL

The Bessel is a type of "linear phase" filter. Because of their linear phase characteristics, these filters approximate a constant time delay over a limited frequency range. Bessel filters pass transient waveforms with a minimum of distortion. They are also used to provide time delays for low pass filtering of modulated waveforms and as a "running average" type filter.

The maximum phase shift is $\frac{-n\Pi}{2}$ radians where n is the order (number of poles) of the filter. The cut-off frequency fc, is defined as the frequency at which the phase shift is one half of this value. For accurate delay, the cut-off frequency should be twice the maximum signal frequency.

The following table can be used to obtain the -3dB frequency of the filter.

	2 pole	4 Pole	6 Pole	8 Pole
–3dB Frequency	$0.77f_c$	$0.67f_c$	$0.57f_c$	$0.50f_c$

Other characteristics :

- Selectivity not as great as Chebyschev or Butterworth.
- Very little overshoot response to step inputs.
- Fast rise time.

CHEBYSCHEV

Chebyschev filters have greater selectivity than either Bessel or Butterworth at the expense of ripple in the passband.

Chebyschev filters are normally designed with peak-to-peak ripple values from 0.2dB to 2dB.

Increased ripple in the passband allows increased attenuation above the cut-off frequency.

The cut-off frequency is defined as the frequency at which the amplitude response passes through the specified maximum ripple band and enters the stop band.

Other characteristics :

- Greater selectivity
- Very non-linear phase response
- High overshoot response to step inputs

The table below shows the typical overshoot and settling time response of the low pass filters to a step input.

	Number of Poles	Peak Overshoot	Settling Time (% of final value)		
		% Overshoot	±1%	±0 .1%	±0 0.1%
Butterworth	2	4	$1.1/f_c$sec.	$1.7/f_c$sec.	$1.9/f_c$sec.
	4	11	$1.7/f_c$	$2.8/f_c$	$3.8/f_c$
	6	14	$2.4/f_c$	$3.9/f_c$	$5.0/f_c$
	8	16	$3.1/f_c$	$5.1/f_c$	$7.1/f_c$
Bessel	2	0.4	$0.8/f_c$	$1.4/f_c$	$1.7/f_c$
	4	0.8	$1.0/f_c$	$1.8/f_c$	$2.4/f_c$
	6	0.6	$1.3/f_c$	$2.1/f_c$	$2.7/f_c$
	8	0.3	$1.6/f_c$	$2.3/f_c$	$3.2/f_c$
Chebyschev (ripple ±0.25dB)	2	11	$1.1/f_c$	$1.6/f_c$	–
	4	18	$3.0/f_c$	$5.4/f_c$	–
	6	21	$5.9/f_c$	$10.4/f_c$	–
	8	23	$8.4/f_c$	$16.4/f_c$	–
Chebyschev (ripple ±1dB)	2	21	$1.6/f_c$	$2.7/f_c$	–
	4	28	$4.8/f_c$	$8.4/f_c$	–
	6	32	$8.2/f_c$	$16.3/f_c$	–
	8	34	$11.6/f_c$	$24.8/f_c$	–

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Design of 2nd order active low pass filter (Sallen and Key configuration unity gain-op-amp)

Fixed R = R1 = R2, we have (see fig. 13).

$$C1 = \frac{1}{R}\,\frac{\xi}{\omega_c}$$

$$C2 = \frac{1}{R}\,\frac{1}{\xi\omega_c}$$

The diagram of fig.14 shows the amplitude response for different values of damping factor ξ in 2nd order filters.

Figure 13 : Filter Configuration

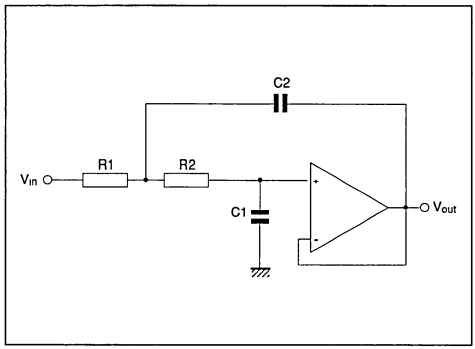
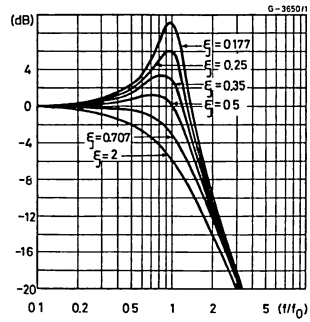


Figure 14 : Filter Respons versus Damping Factor



Three parameters are needed to characterize the frequency and phase response of a 2nd order active filter : the gain (G_v), the damping factor (ξ) or the Q-factor ($Q = (2\xi)^{-1}$), and the cut-off frequency (f_c).

The higher order responses are obtained with a series of 2nd order sections. A simple RC section is introduced when an odd filter is required.

The choice of 'ξ' (or Q-factor) determines the filter response (see table 1).

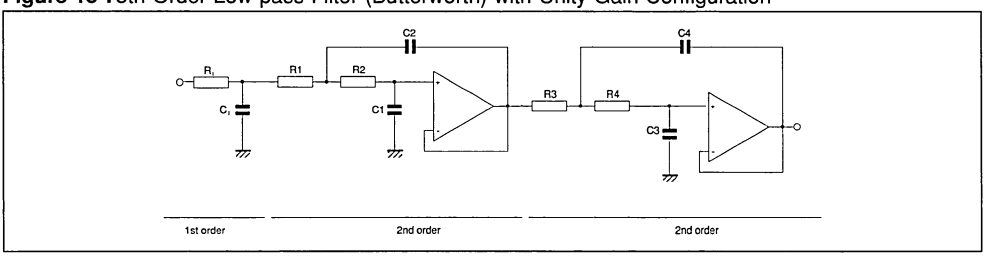
Table 1

Filter Response	ξ	Q	Cutoff Frequency f_c
Bessel	$\frac{\sqrt{3}}{2}$	$\frac{\sqrt{1}}{3}$	Frequency at which Phase Shift is -90°C
Butterworth	$\frac{\sqrt{2}}{2}$	$\frac{\sqrt{1}}{2}$	Frequency at which G_V = -3dB
Chebyschev	$\frac{\sqrt{2}}{2}$	$\frac{\sqrt{1}}{2}$	Frequency at which the amplitude response passes through specified max. ripple band and enters the stop band.

404-05.TBL

EXAMPLE

Figure 15 : 5th Order Low-pass Filter (Butterworth) with Unity Gain Configuration



In the circuit of fig. 15, for f_c = 3.4kHz and $R_i = R_1 = R_2 = R_3 = R_4$ = 10kΩ, we obtain :

$$C_i = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\Pi f_C} = 6.33nF$$

$$C_1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\Pi f_C} = 1.97nF$$

$$C_2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\Pi f_C} = 8.20nF$$

$$C_3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\Pi f_C} = 1.45nF$$

$$C_4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2\Pi f_C} = 15.14nF$$

The attenuation of the filter is 30dB at 6.8kHz and better than 60dB at 15kHz.

The same method, referring to Tab. 2 and fig. 16, is used to design high-pass filter. In this case the damping factor is found by taking the reciprocal of the numbers in Tab. 2. For f_c = 5kHz and $C_i = C_1 = C_2 = C_3 = C_4$ = 1nF we obtain :

$$R_i = \frac{1}{0.354} \cdot \frac{1}{C} \cdot \frac{1}{2\Pi f_C} = 25.5k\Omega$$

$$R_1 = \frac{1}{0.421} \cdot \frac{1}{C} \cdot \frac{1}{2\Pi f_C} = 75.6k\Omega$$

$$R_2 = \frac{1}{1.753} \cdot \frac{1}{C} \cdot \frac{1}{2\Pi f_C} = 18.2k\Omega$$

$$R_3 = \frac{1}{0.309} \cdot \frac{1}{C} \cdot \frac{1}{2\Pi f_C} = 103k\Omega$$

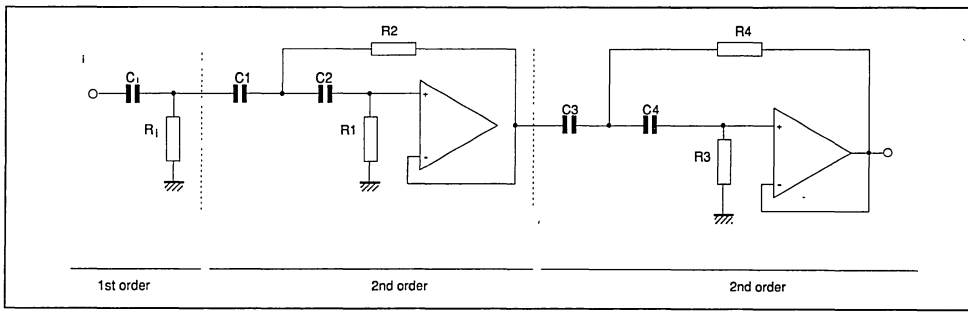
$$R_4 = \frac{1}{3.325} \cdot \frac{1}{C} \cdot \frac{1}{2\Pi f_C} = 9.6k\Omega$$

Table 2 : Damping Factor for Low-pass Butterworth Filters

Order	C_i	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
2		0.707	1.41						
3	1.392	0.202	3.54						
4		0.92	1.08	0.38	2.61				
5	1.354	0.421	1.75	0.309	3.235				
6		0.966	1.035	0.707	1.414	0.259	3.86		
7	1.336	0.488	1.53	0.623	1.604	0.222	4.49		
8		0.98	1.02	0.83	1.20	0.556	1.80	0.195	5.125

404-06.TBL

Figure 16 : 5th Order High-pass Filter (Butterworth) with Unity Gain Configuration



404-18.EPS

Figure 17 : Mutliple Feedback 8-pole Bandpass Filter

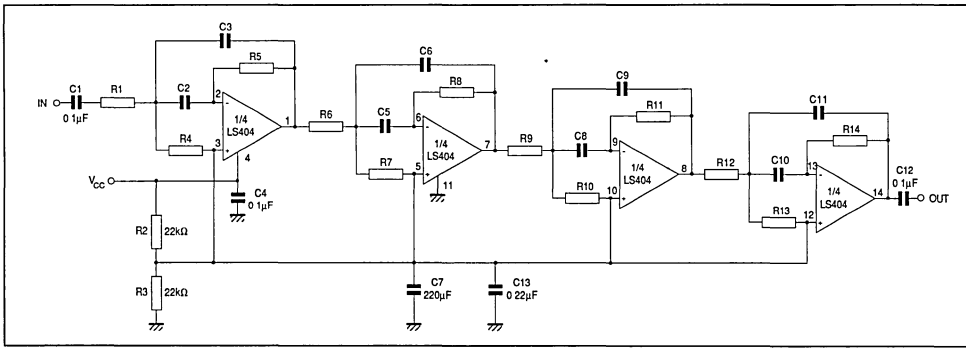


Figure 18 : Frequency Response of Bandpass Filter

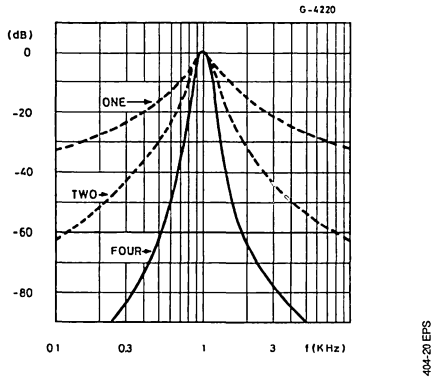


Figure 19 : Bandwidth of Bandpass Filter

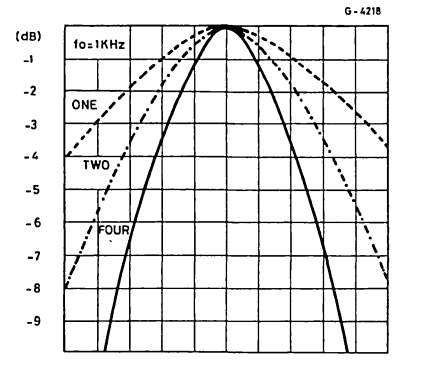
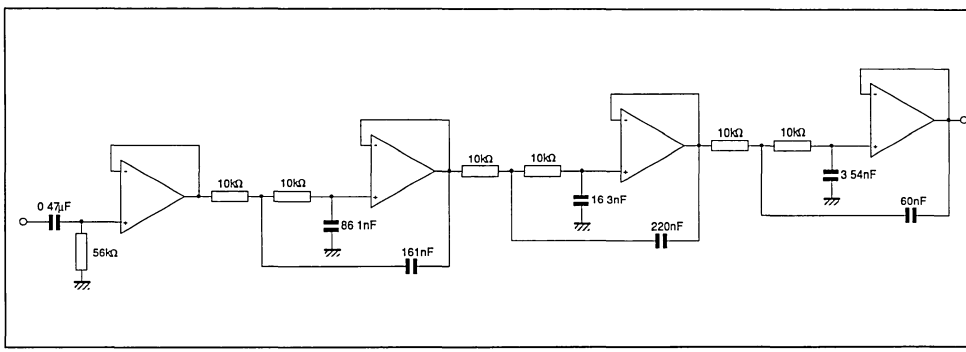
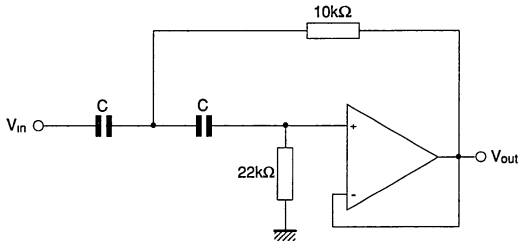


Figure 20 : Six-pole 355Hz Low-pass Filter (chebychev type)



This is a 6-pole Chebychev type with ±0.25dB ripple in the passband. A decoupling stage is used to avoid the influence of the input impedance on the filter's characteristics. The attenuation is about 55dB at 710Hz and reaches 80dB at 1065Hz. The in band attenuation is limited in practise to the ±0.25dB ripple and does not exceed 0.5dB at 0.9fc.

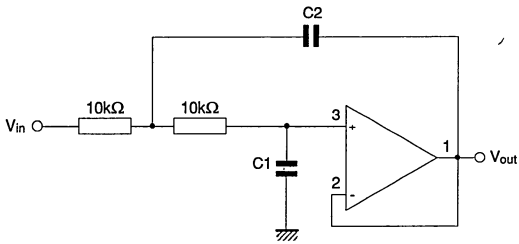
Figure 21 : Subsonic Filter (G_V = 0dB)



f_C (Hz)	C (µF)
15	0.68
22	0.47
30	0.33
55	0.22
100	0.10

404-23 EPS

Figure 22 : High Cut Filter (G_V = 0dB)



f_C (Hz)	C1 (nF)	C2 (nF)
3	3.9	6.8
5	2.2	4.7
10	1.2	2.2
15	0.68	1.5

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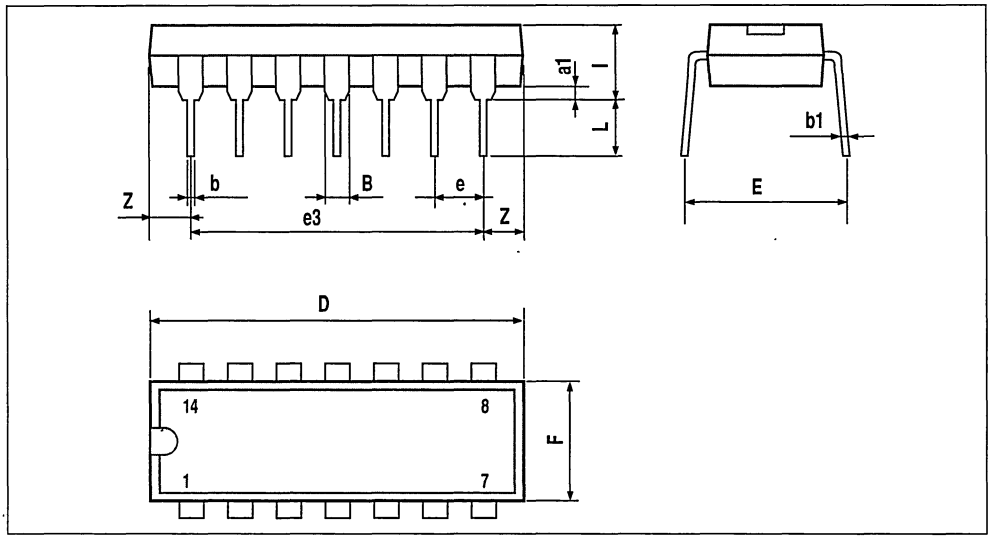
PACKAGE MECHANICAL DATA

14 PINS - PLASTIC DIP



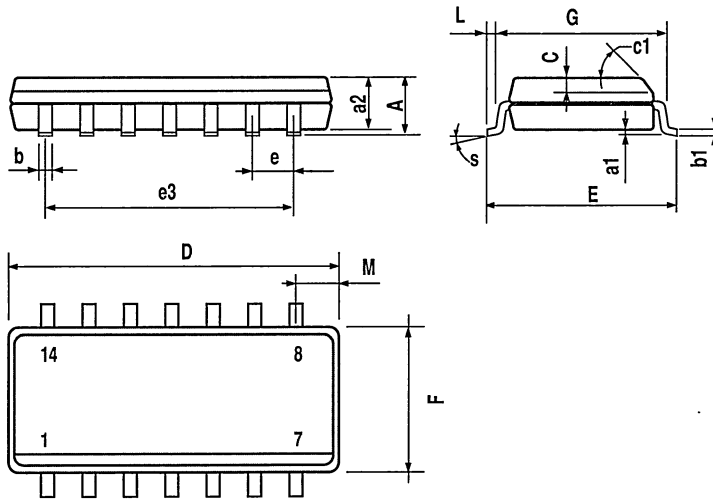
PM-DIP14.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
i			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

DIP14.TBL

PACKAGE MECHANICAL DATA

14 PINS - PLASTIC MICROPACKAGE (SO)



PM-SO14.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.2	0.004		0.008
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.334
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.150		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.020		0.050
M			0.68			0.027
S	8° (max.)					

SO14.TBL

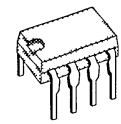
ORDER CODE

SGS-THOMSON MICROELECTRONICS

TSH150

WIDE BANDWIDTH AND BIPOLAR INPUTS SINGLE OPERATIONAL AMPLIFIER

- LOW DISTORTION
- GAIN BANDWIDTH PRODUCT : 150MHz
- UNITY GAIN STABLE
- SLEW RATE : 190V/µs
- VERY FAST SETTLING TIME : 20ns (0.1%)



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

DESCRIPTION:

The TSH150 is a wideband monolithic operational amplifier, internally compensated for unity-gain stability.

Low noise and low distortion, wide bandwidth and high linearity make this amplifier suitable for RF and video applications. Short circuit protection is provided by an internal current-limiting circuit.

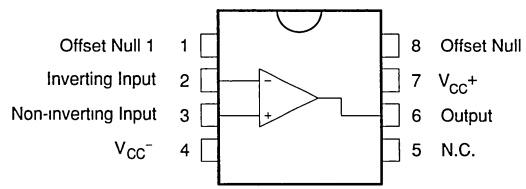
The TSH150 has internal electrostatic discharge (ESD) protection circuits and fulfills MILSTD883C-Class2.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TSH150C	0°C, 70°C	•	•
TSH150I	-40°C, 105°C	•	•
TSH150M	-55°C, 125°C	•	•

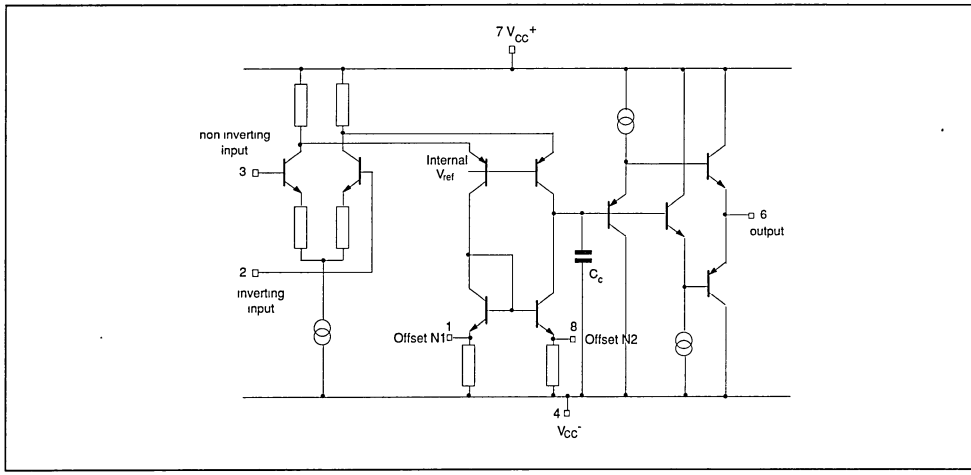
150-01 TBL

PIN CONNECTIONS (top view)

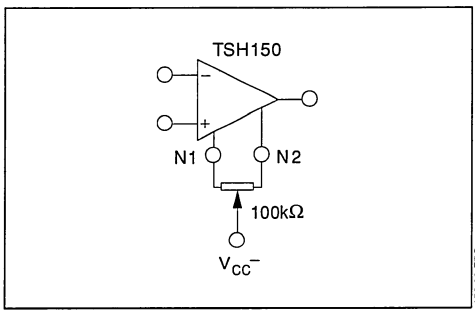


150-01 EPS

SCHEMATIC DIAGRAM



INPUT OFFSET VOLTAGE NULL CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		±7	V
V_{id}	Differential Input Voltage		±5	V
V_i	Input Voltage Range		±5	V
I_{in}	Current On Inputs Current On Offset Null Pins		±50 ±20	mA
T_{oper}	Operating Free-Air Temperature Range	TSH150C TSH150I TSH150M	0 to +70 -40 to +105 -55 to +125	°C
T_{stg}	Storage Temperature Range		-65 to 150	°C

150-02.TBL

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	±3 to ±6	V
V_{ic}	Common Mode Input Voltage Range	V_{CC}^- +2 to V_{CC}^+ -1	V

150-03.TBL

ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 5V$, $T_{amb} = 25°C$ (unless otherwise specified)

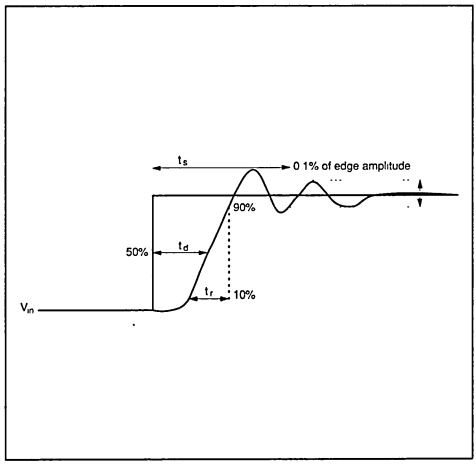
Symbol	Parameter		TSH150C, I, M			Unit
			Min.	Typ.	Max.	
V_{io}	Input Offset Voltage $T_{min} \le T_{amb} \le T_{max}$			0.3	10 12	mV
DV_{io}	Input Offset Voltage Drift $T_{min} \le T_{amb} \le T_{max}$				10	µV/°C
I_{ib}	Input Bias Current			5	30	µA
I_{io}	Input Offset Current			0.1	2	µA
I_{CC}	Supply Current, no load					mA
		$V_{CC} = \pm 5V$		23	30	
		$V_{CC} = \pm 3V$		21	28	
		$V_{CC} = \pm 6V$		25	40	
	$T_{min} \le T_{amb} \le T_{max}$	$V_{CC} = \pm 5V$			32	
A_{vd}	Large Signal Voltage Gain $V_o = \pm 2.5V$					V/V
		$R_L = \infty$	800	1300		
		$R_L = 100\Omega$	300	850		
		$R_L = 50\Omega$	200	650		
V_{icm}	Input Common Mode Voltage Range		-3 to +4	-3.5 to +4.5		V
CMR	Common Mode Rejection Ratio	$V_{ic} = V_{icm\ min}$	60	100		dB
SVR	Supply Voltage Rejection Ratio $V_{CC} = \pm 5V$ to $\pm 3V$		50	70		dB
V_o	Output Voltage	$R_L = 100\Omega$	± 3	+3.5 -3.7		V
		$R_L = 50\Omega$	± 2.8	+3.3 -3.5		
	$T_{min} \le T_{amb} \le T_{max}$	$R_L = 100\Omega$	± 2.9			
		$R_L = 50\Omega$	± 2.7			
I_o	Output Short Circuit Current $V_{id} = \pm 1V$, $V_o = 0V$		± 50	± 100		mA
GBP	Gain Bandwidth Product $A_{VCL} = 100$, $R_L = 100\Omega$, $C_L = 15pF$, $f = 7.5MHz$			150		MHz
SR	Slew Rate $V_{in} = \pm 2V$, $A_{VCL} = 1$, $R_L = 100\Omega$, $C_L = 15pF$		100	190		V/µs
e_n	Equivalent Input Voltage Noise $R_S = 50\Omega$					$\frac{nV}{\sqrt{Hz}}$
		fo = 1kHz		7		
		fo = 10kHz		6.5		
		fo = 100kHz		6.2		
		fo = 1MHz		5.5		
K_{ov}	Overshoot $V_{in} = \pm 2V$, $A_{VCL} = 1$, $R_L = 100\Omega$, $C_L = 15pF$			5		%
t_s	Settling Time 0.1% - (note 1) $V_{in} = \pm 1V$, $A_{VCL} = -1$			20		ns
t_r, t_f	Rise and Fall Time - (note 1) $V_{in} = \pm 100mV$, $A_{VCL} = 2$			3.5		ns
t_d	Delay Time - (note 1) $V_{in} = \pm 100mV$, $A_{VCL} = 2$			2.5		ns
Øm	Phase Margin $A_{VM} = 1$, $R_L = 100\Omega$, $C_L = 15pF$			50		Degrees
THD	Total Harmonic Distortion $A_{VCL} = 10$, $f = 1KHz$, $V_o = \pm 2.5V$, no load			0.02		%
FPB	Full Power Bandwidth - (note 2) $V_o = 5Vpp$, $R_L = 100\Omega$ $V_o = 2Vpp$, $R_L = 100\Omega$			12 30		MHz

150-04 TBL

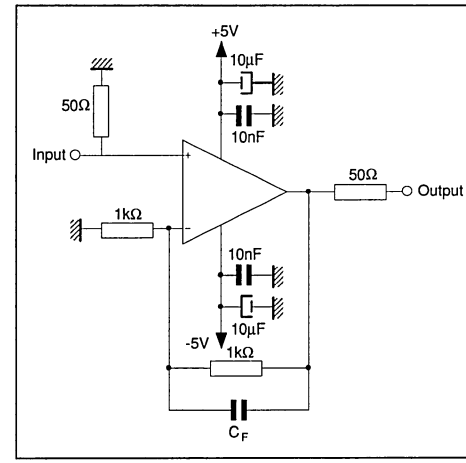
Note 1 : See test waveform figure

Note 2 : Full power bandwidth = $\frac{SR}{\Pi V_{opp}}$

TEST WAVEFORM



EVALUATION CIRCUIT



PRINTED CIRCUIT LAYOUT

As for any high frequency device, a few rules must be observed when designing the PCB to get the best performances from this high speed op amp.

From the most to the least important points :

- Each power supply lead has to be bypassed to ground with a 10nF ceramic capacitor very close to the device and a 10µF tantalum capacitor.
- To provide low inductance and low resistance common return, use a ground plane or common point return for power and signal.
- All leads must be wide and as short as possible especially for op amp inputs. This is in order to decrease parasitic capacitance and inductance.
- Use small resistor values to decrease time constant with parasitic capacitance. Be aware on TSH150 device of the I_{io} error and input noise currents with high feedback resistor values.
- Choose component sizes as small as possible (SMD).
- On output, decrease capacitor load so as to avoid circuit stability being degraded which may cause oscillation. You can also add a serial resistor in order to minimise its influence.
- One can add in parallel with feedback resistor a few pF ceramic capacitor C_F adjusted to optimize the settling time.

MACROMODEL

- LOW DISTORTION
- GAIN BANDWIDTH PRODUCT : 150MHz
- UNITY GAIN STABLE
- SLEW RATE : 190V/µs
- VERY FAST SETTLING TIME : 20ns (0.1%)

Applies to : TSH150C,I,M

```
** Standard Linear Ics Macromodels, 1993.
** CONNECTIONS :
* 1 INVERTING INPUT
* 2 NON-INVERTING INPUT
* 3 OUTPUT
* 4 POSITIVE POWER SUPPLY
* 5 NEGATIVE POWER SUPPLY

.SUBCKT TSH150 1 3 2 4 5 (analog)
**********************************************************
.MODEL MDTH D IS=1E-8 KF=1.568191E-15 CJO=10F
* INPUT STAGE
CIP 2 5 1.000000E-12
CIN 1 5 1.000000E-12
EIP 10 5 2 5 1
EIN 16 5 1 5 1
RIP 10 11 1.040000E+02
RIN 15 16 1.040000E+02
RIS 11 15 3.264539E+02
DIP 11 12 MDTH 400E-12
DIN 15 14 MDTH 400E-12
VOFP 12 13 DC -9.162265E-05
VOFN 13 14 DC 0
IPOL 13 5 1.000000E-03
CPS 11 15 5.757255E-12
DINN 17 13 MDTH 400E-12
VIN 17 5 1.5000000e+00
DINR 15 18 MDTH 400E-12
VIP 4 18 0.500000E+00
FCP 4 5 VOFP 2.200000E+01
FCN 5 4 VOFN 2.200000E+01
FIBP 2 5 VOFP 1.000000E-02
FIBN 5 1 VOFN 1.000000E-02
* AMPLIFYING STAGE
FIP 5 19 VOFP 4.370000E+02
FIN 5 19 VOFN 4.370000E+02
RG1 19 5 1.124121E+03
RG2 19 4 1.124121E+03
CC 19 29 2.000000E-09
HZTP 30 29 VOFP 5.574976E+01
HZTN  5 30 VOFN 5.574976E+01
DOPM 19 22 MDTH 400E-12
DONM 21 19 MDTH 400E-12
HOPM 22 28 VOUT 5.000000E+02
VIPM 28 4 5.000000E+01
HONM 21 27 VOUT 5.000000E+02
VINM 5 27 5.000000E+01
EOUT 26 23 19 5 1
VOUT 23 5 0
ROUT 26 3 2.180423E+01
COUT 3 5 1.000000E-12
DOP 19 25 MDTH 400E-12
VOP 4 25 1.511965E+00
DON 24 19 MDTH 400E-12
VON 24 5 1.511965E+00
.ENDS
```

ELECTRICAL CHARACTERISTICS

V_{CC} = ±5V, T_{amb} = 25°C (unless otherwise specified)

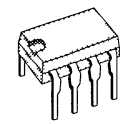
Symbol	Conditions	Value	Unit
V_{io}		0	mV
A_{vd}	R_L = 100Ω	1	V/mV
I_{CC}	No load	21	mA
V_{icm}		-3.5 to 4.5	V
V_{OH}	R_L = 100Ω	+3.6	V
V_{OL}	R_L = 100Ω	-3.6	V
I_{sink}	V_O = 0V	108	mA
I_{source}	V_O = 0V	108	mA
GBP	R_L = 100Ω, C_L = 15pF	147	MHz
SR	R_L = 100Ω, C_L = 15pF	180	V/µs
Øm	R_L = 100Ω, C_L = 15pF	42	Degrees
t_s	A_V = -1 at 0.1%	22.6	ns

SGS-THOMSON MICROELECTRONICS

TSH151

WIDE BANDWIDTH AND MOS INPUTS SINGLE OPERATIONAL AMPLIFIER

- LOW DISTORTION
- GAIN BANDWIDTH PRODUCT : 150MHz
- UNITY GAIN STABLE
- SLEW RATE : 200V/µs
- VERY FAST SETTLING TIME : 70ns (0.1%)
- VERY HIGH INPUT IMPEDANCE



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

DESCRIPTION:

The TSH151 is a wideband monolithic operational amplifier, internally compensated for unity-gain stability.

The TSH151 features extremely high input impedance (typically greater than $10^{12}\Omega$) allowing direct interfacing with high impedance sources.

Low distortion, wide bandwidth and high linearity make this amplifier suitable for RF and video applications. Short circuit protection is provided by an internal current-limiting circuit.

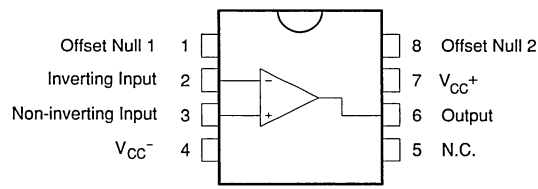
The TSH151 has internal electrostatic discharge (ESD) protection circuits and fulfills MILSTD883C-Class2.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TSH151C	0°C, 70°C	•	•
TSH151I	-40°C, 105°C	•	•
TSH151M	-55°C, 125°C	•	•

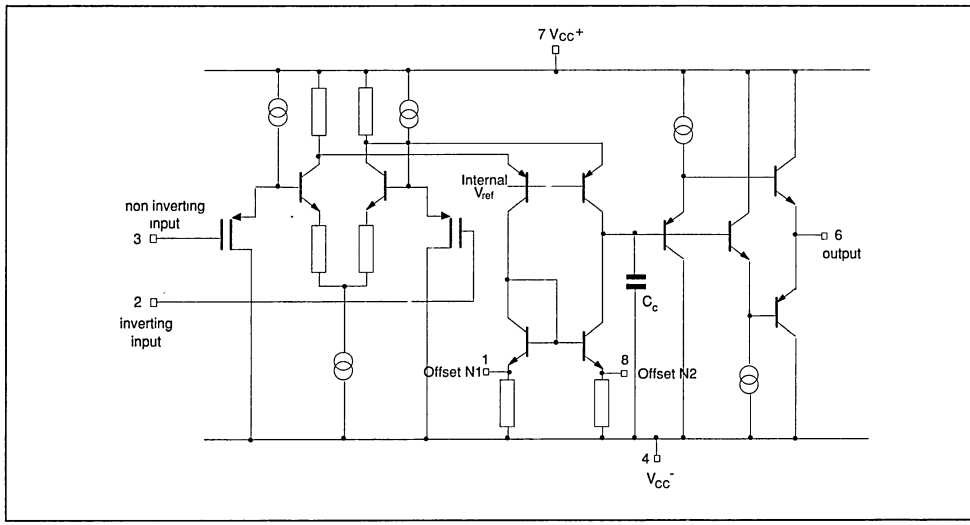
151-01 TBL

PIN CONNECTIONS (top view)

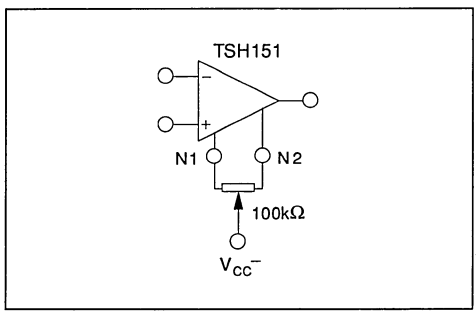


151-01 EPS

SCHEMATIC DIAGRAM



INPUT OFFSET VOLTAGE NULL CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		±7	V
V_{id}	Differential Input Voltage		±5	V
V_i	Input Voltage Range		±5	V
I_{in}	Current On Offset Null Pins		±20	mA
T_{oper}	Operating Free-Air Temperature Range	TSH151C TSH151I TSH151M	0°C, 70°C -40°C, 105°C -55°C, 125°C	°C

151-02 TBL

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	±3 to ±6	V
V_{ic}	Common Mode Input Voltage Range	V_{CC}^- to V_{CC}^+ -3	V

151-03 TBL

ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 5V$, $T_{amb} = 25°C$ (unless otherwise specified)

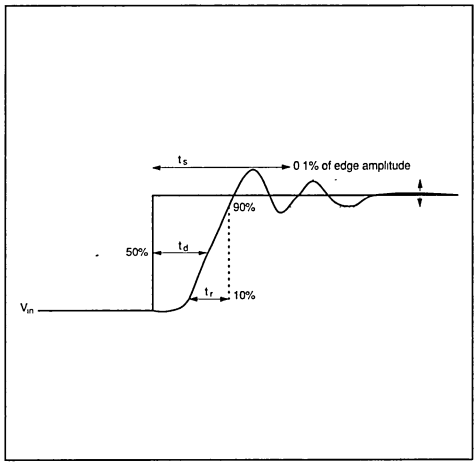
Symbol	Parameter		TSH151C, I, M			Unit
			Min.	Typ.	Max.	
V_{io}	Input Offset Voltage $T_{min} \le T_{amb} \le T_{max}$			0.5	10 12	mV
DV_{io}	Input Offset Voltage Drift $T_{min} \le T_{amb} \le T_{max}$			10		µV/°C
I_{ib}	Input Bias Current			2	300	pA
I_{io}	Input Offset Current			2	200	pA
I_{CC}	Supply Current, no load					mA
		$V_{CC} = \pm 5V$		23	30	
		$V_{CC} = \pm 3V$		21	28	
		$V_{CC} = \pm 6V$		25	40	
	$T_{min} \le T_{amb} \le T_{max}$.	$V_{CC} = \pm 5V$			32	
A_{vd}	Large Signal Voltage Gain $V_o = \pm 2.5V$					V/V
		$R_L = \infty$	800	1300		
		$R_L = 100\Omega$	300	850		
		$R_L = 50\Omega$	200	650		
V_{icm}	Input Common Mode Voltage Range		-5 to +2	-5.5 to +2.5		V
CMR	Common Mode Rejection Ratio	$V_{ic} = V_{icm\ min.}$	60	100		dB
SVR	Supply Voltage Rejection Ratio $V_{CC} = \pm 5V$ to $\pm 3V$		50	70		dB
V_o	Output Voltage	$R_L = 100\Omega$	æ 3	+3.5 -3.7		V
		$R_L = 50\Omega$	± 2.8	+3.3 -3.5		
	$T_{min} \le T_{amb} \le T_{max}$	$R_L = 100\Omega$	± 2.9			
		$R_L = 50\Omega$	± 2.7			
I_o	Output Short Circuit Current $V_{id} = \pm 1V$, $V_o = 0V$		±50	±100		mA
GBP	Gain Bandwidth Product $A_{VCL} = 100$, $R_L = 100\Omega$, $C_L = 15pF$, f = 7.5MHz			150		MHz
SR	Slew Rate $V_{in} = \pm 2V$, $A_{VCL} = 1$, $R_L = 100\Omega$, $C_L = 15pF$		100	200		V/µs
e_n	Equivalent Input Voltage Noise $R_S = 50\Omega$					$\frac{nV}{\sqrt{Hz}}$
		fo = 1kHz		20		
		fo = 10kHz		18.2		
		fo = 100kHz		18.1		
		fo = 1MHz		18.2		
K_{ov}	Overshoot $V_{in} = \pm 2V$, $A_{VCL} = 1$, $R_L = 100\Omega$, $C_L = 15pF$			10		%
t_s	Settling Time 0.1% - (note 1) $V_{in} = \pm 1V$, $A_{VCL} = -1$			70		ns
t_r, t_f	Rise and Fall Time - (note 1) $V_{in} = \pm 100mV$, $A_{VCL} = 2$			5		ns
t_d	Delay Time - (note 1) $V_{in} = \pm 100mV$, $A_{VCL} = 2$			4		ns
Øm	Phase Margin $A_{VM} = 1$, $R_L = 100\Omega$, $C_L = 15pF$			45		Degrees
THD	Total Harmonic Distortion $A_{VCL} = 10$, f = 1KHz, $V_o = \pm 2.5V$, no load			0.02		%
FPB	Full Power Bandwidth - (note 2) V_o = 5Vpp, $R_L = 100\Omega$			13		MHz
	V_o = 2Vpp, $R_L = 100\Omega$			32		

151-04 TBL

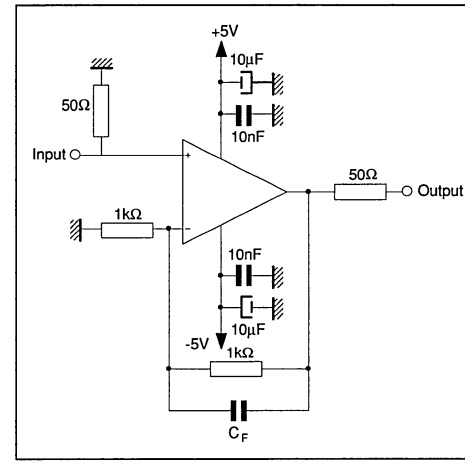
Note 1 : See test waveform figure

Note 2 : Full power bandwidth = $\frac{SR}{\Pi V_{opp}}$

TEST WAVEFORM



EVALUATION CIRCUIT



PRINTED CIRCUIT LAYOUT

As for any high frequency device, a few rules must be observed when designing the PCB to get the best performances from your this speed op amp.

From the most to the least important points :

- Each power supply lead has to be bypassed to ground with a 10nF ceramic capacitor very close to the device and a 10µF tantalum capacitor.
- To provide low inductance and low resistance common return, use a ground plane or common point return for power and signal.
- All leads must be wide and as short as possible especially for op amp inputs. This is in order to decrease parasitic capacitance and inductance.
- Use small resistor values to decrease time constant with parasitic capacitance.
- Choose component sizes as small as possible (SMD).
- On output, decrease capacitor load so as to avoid circuit stability being degraded which may cause oscillation. One can also add a serial resistor in order to minimise its influence.
- One can add in parallel with feedback resistor a few pF ceramic capacitor C_F adjusted to optimize the settling time.

MACROMODEL

- LOW DISTORTION
- GAIN BANDWIDTH PRODUCT : 150MHz
- UNITY GAIN STABLE
- SLEW RATE : 200V/µs
- VERY FAST SETTLING TIME : 70ns (0.1%)
- VERY HIGH INPUT IMPEDANCE

Applies to : TSH151C,I,M

```
** Standard Linear Ics Macromodels, 1993.
** CONNECTIONS :
* 1 INVERTING INPUT
* 2 NON-INVERTING INPUT
* 3 OUTPUT
* 4 POSITIVE POWER SUPPLY
* 5 NEGATIVE POWER SUPPLY

.SUBCKT TSH151 1 3 2 4 5 (analog)
**********************************************************
.MODEL MDTH D IS=1E-8 KF=3.322525E-14 CJO=10F
* INPUT STAGE
RESD1 2 202 150
RESD2 1 201 150
CIP 202 5 10.000000E-12
CIN 201 5 10.000000E-12
EIP 10 5 202 5 1
EIN 16 5 201 5 1
RIP 10 11 2.600000E-01
RIN 15 16 2.600000E-01
RIS 11 15 1.683423E-01
DIP 11 12 MDTH 400E-12
DIN 15 14 MDTH 400E-12
VOFP 12 13 DC 0.000000E+00
VOFN 13 14 DC 0
IPOL 13 5 1.000000E-03
CPS 11 15 8E-09
DINN 17 13 MDTH 400E-12
VIN 17 5 1.500000e+00
DINR 15 18 MDTH 400E-12
VIP 4 18 5.000000E-01
FCP 4 5 VOFP 2.200000E+01
FCN 5 4 VOFN 2.200000E+01
* AMPLIFYING STAGE
FIP 5 19 VOFP 3.800000E+02
FIN 5 19 VOFN 3.800000E+02
RG1 19 5 1.455096E+03
RG2 19 4 1.455096E+03
CC 19 29 2.000000E-09
HZTP 29 30 VOFP 100
HZTN 30 5 VOFN 100
DOPM 19 22 MDTH 400E-12
DONM 21 19 MDTH 400E-12
HOPM 22 28 VOUT 5.000000E+02
VIPM 28 4 5.000000E+01
HONM 21 27 VOUT 5.000000E+02
VINM 5 27 5.000000E+01
EOUT 26 23 19 5 1
VOUT 23 5 0
ROUT 26 3 9.978126E+00
COUT 3 5 1.000000E-13
DOP 19 25 MDTH 400E-12
VOP 4 25 1.946965E+00
DON 24 19 MDTH 400E-12
VON 24 5 1.946965E+00
.ENDS
```

ELECTRICAL CHARACTERISTICS

V_{CC} = ±5V, T_{amb} = 25°C (unless otherwise specified)

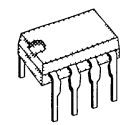
Symbol	Conditions	Value	Unit
V_{io}		0	mV
A_{vd}	R_L = 100Ω	1.18	V/mV
I_{CC}	No load, per operator	23	mA
V_{icm}		-5 to 2.5	V
V_{OH}	R_L = 100Ω	+3.6	V
V_{OL}	R_L = 100Ω	-3.6	V
I_{sink}	V_O = 0V	108	mA
I_{source}	V_O = 0V	108	mA
GBP	R_L = 100Ω, C_L = 15pF	130	MHz
SR	R_L = 100Ω, C_L = 15pF	172	V/µs
Øm	R_L = 100Ω, C_L = 15pF	25	Degrees
t_s	A_V = -1 at 0.1%	40	ns

SGS-THOMSON MICROELECTRONICS

TSH321

WIDE BANDWIDTH AND MOS INPUTS SINGLE OPERATIONAL AMPLIFIER

- LOW DISTORTION
- GAIN BANDWIDTH PRODUCT : 300MHz
- GAIN OF 2 STABILITY
- SLEW RATE : 400V/µs
- VERY FAST SETTLING TIME : 60ns (0.1%)
- VERY HIGH INPUT IMPEDANCE



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

DESCRIPTION:

The TSH321 is a wideband monolithic operational amplifier, requiring a minimum close loop gain of 2 for stability.

The TSH321 features extremely high input impedance (typically greater than $10^{12}\Omega$) allowing direct interfacing with high impedance sources.

Low distortion, wide bandwidth and high linearity make this amplifier suitable for RF and video applications. Short circuit protection is provided by an internal current-limiting circuit.

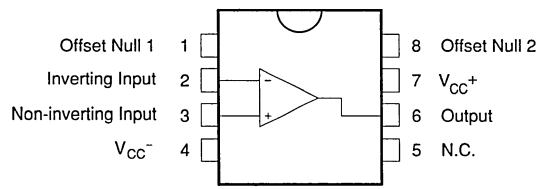
The TSH321 has internal electrostatic discharge (ESD) protection circuits and fulfills MILSTD883C-Class2.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TSH321I	-40°C, 105°C	•	•

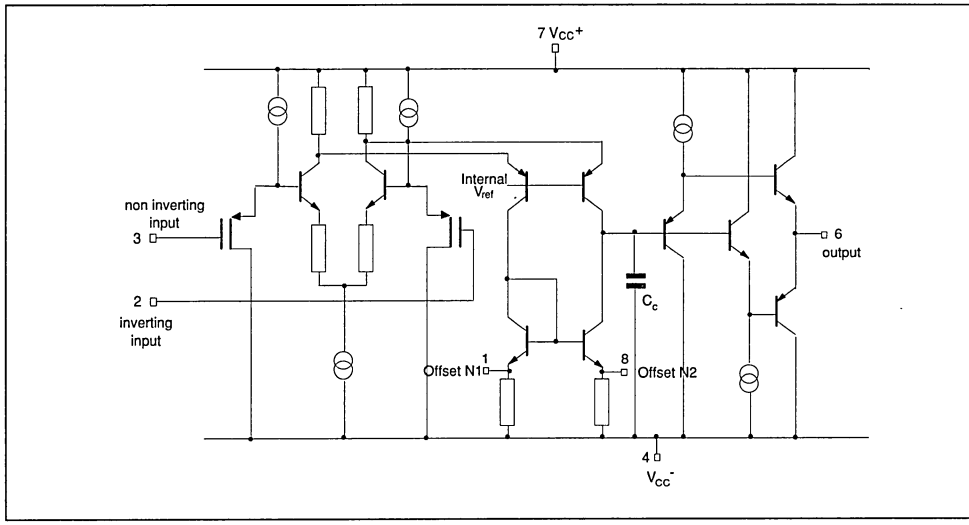
321-01 TBL

PIN CONNECTIONS (top view)

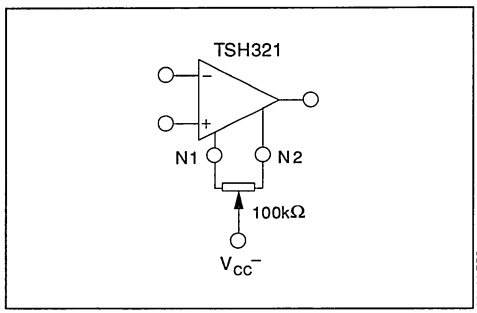


321-01 EPS

SCHEMATIC DIAGRAM



INPUT OFFSET VOLTAGE NULL CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	± 7	V
V_{id}	Differential Input Voltage	± 5	V
V_i	Input Voltage Range	± 5	V
I_{in}	Current On Offset Null Pins	± 20	mA
T_{oper}	Operating Free-Air Temperature Range TSH321I	-40°C, 105°C	°C

321-02.TBL

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	± 3 to ± 6	V
V_{ic}	Common Mode Input Voltage Range	V_{CC}^- to V_{CC}^+ -3	V

321-03.TBL

ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 5V$, $T_{amb} = 25°C$ (unless otherwise specified)

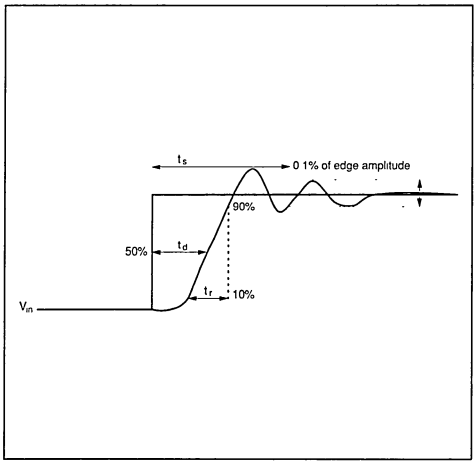
Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage $T_{min} \le T_{amb} \le T_{max}$			0.5	10 12	mV
DV_{io}	Input Offset Voltage Drift $T_{min} \le T_{amb} \le T_{max}$			10		µV/°C
I_{ib}	Input Bias Current			2	300	pA
I_{io}	Input Offset Current			2	200	pA
I_{CC}	Supply Current, no load					mA
		$V_{CC} = \pm 5V$		23	30	
		$V_{CC} = \pm 3V$		21	28	
		$V_{CC} = \pm 6V$		25	40	
	$T_{min} \le T_{amb} \le T_{max}$	$V_{CC} = \pm 5V$			32	
A_{vd}	Large Signal Voltage Gain $V_o = \pm 2.5V$					V/V
		$R_L = \infty$	800	1300		
		$R_L = 100\Omega$	300	850		
		$R_L = 50\Omega$	200	650		
V_{icm}	Input Common Mode Voltage Range		-5 to +2	-5.5 to +2.5		V
CMR	Common Mode Rejection Ratio	$V_{ic} = V_{icm\ min}$	60	100		dB
SVR	Supply Voltage Rejection Ratio $V_{CC} = \pm 5V$ to $\pm 3V$		50	70		dB
V_o	Output Voltage	$R_L = 100\Omega$	æ 3	+3.5 -3.7		V
		$R_L = 50\Omega$	± 2.8	+3.3 -3.5		
	$T_{min} \le T_{amb} \le T_{max}$	$R_L = 100\Omega$	± 2.9			
		$R_L = 50\Omega$	± 2.7			
I_o	Output Short Circuit Current $V_{id} = \pm 1V$, $V_o = 0V$		± 50	± 100		mA
GBP	Gain Bandwidth Product $A_{VCL} = 100$, $R_L = 100\Omega$, $C_L = 15pF$, f = 7.5MHz			300		MHz
SR	Slew Rate $V_{in} = \pm 1V$, $A_{VCL} = 2$ $R_L = 100\Omega$, $C_L = 15pF$		200	400		V/µs
e_n	Equivalent Input Voltage Noise $R_S = 50\Omega$					$\frac{nV}{\sqrt{Hz}}$
		fo = 1kHz		20		
		fo = 10kHz		18.2		
		fo = 100kHz		18.1		
		fo = 1MHz		18.2		
K_{ov}	Overshoot $V_{in} = \pm 1V$ $A_{VCL} = 2$, $R_L = 100\Omega$, $C_L = 15pF$			15		%
t_s	Settling Time 0.1% - (note 1) $V_{in} = \pm 1V$, $A_{VCL} = -1$			60		ns
t_r, t_f	Rise and Fall Time - (note 1) $V_{in} = \pm 100mV$, $A_{VCL} = 2$			2		ns
t_d	Delay Time - (note 1) $V_{in} = \pm 100mV$, $A_{VCL} = 2$			2		ns
Øm	Phase Margin $A_{VM} = 2$, $R_L = 100\Omega$, $C_L = 15pF$			45		Degrees
THD	Total Harmonic Distortion $A_{VCL} = 10$, f = 1KHz, $V_o = \pm 2.5V$, no load			0.02		%
FPB	Full Power Bandwidth - (note 2) V_o = 5Vpp, $R_L = 100\Omega$			26		MHz
	V_o = 2Vpp, $R_L = 100\Omega$			64		

321-04 TBL

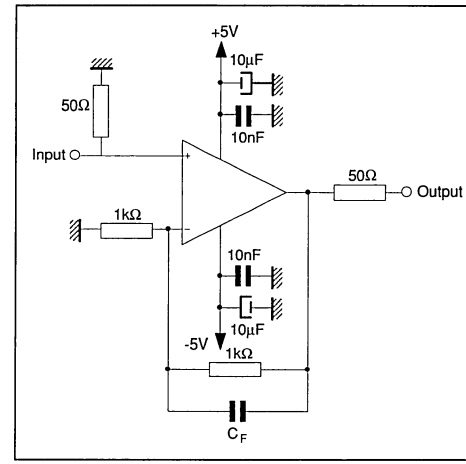
Note 1 : See test waveform figure

Note 2 : Full power bandwidth = $\frac{SR}{\Pi V_{opp}}$

TEST WAVEFORM



EVALUATION CIRCUIT



PRINTED CIRCUIT LAYOUT

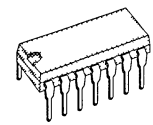
As for any high frequency device, a few rules must be observed when designing the PCB to get the best performances from this high speed op amp.

From the most to the least important points :

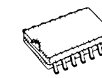
- Each power supply lead has to be bypassed to ground with a 10nF ceramic capacitor very close to the device and a 10µF tantalum capacitor.
- To provide low inductance and low resistance common return, use a ground plane or common point return for power and signal.
- All leads must be wide and as short as possible especially for op amp inputs. This is in order to decrease parasitic capacitance and inductance.
- Use small resistor values to decrease time constant with parasitic capacitance.
- Choose component sizes as small as possible (SMD).
- On output, decrease capacitor load so as to avoid circuit stability being degraded which may cause oscillation. One can also add a serial resistor in order to minimise its influence.
- One can add in parallel with feedback resistor a few pF ceramic capacitor C_F adjusted to optimize the settling time.

3V MICROPOWER QUAD VOLTAGE COMPARATORS

- DEDICATED TO **3.3V** OR **BATTERY SUPPLY** (specified at 3V and 5V)
- EXTREMELY LOW SUPPLY CURRENT : **9µA typ/comparator**
- WIDE SINGLE SUPPLY RANGE **2.7V to 16V**
- EXTREMELY LOW INPUT CURRENTS : **1pA TYP**
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GND
- FAST RESPONSE TIME : 2.5µs typ for 5mV overdrive
- PIN-TO-PIN AND FUNCTIONALLY COMPATIBLE WITH BIPOLAR LM339



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

DESCRIPTION

The TS3V339 is a micropower quad CMOS voltage comparator with extremely low consumption of 9µA typ / comparator (20 times less than bipolar LM339). Similar performances are offered by the quad micropower comparator TS3V3704 with a push-pull CMOS output.

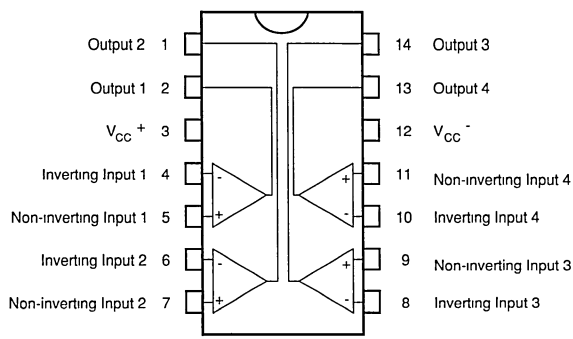
Thus response times remain similar to the LM339.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS3V339I	-40°C, +125°C	•	•

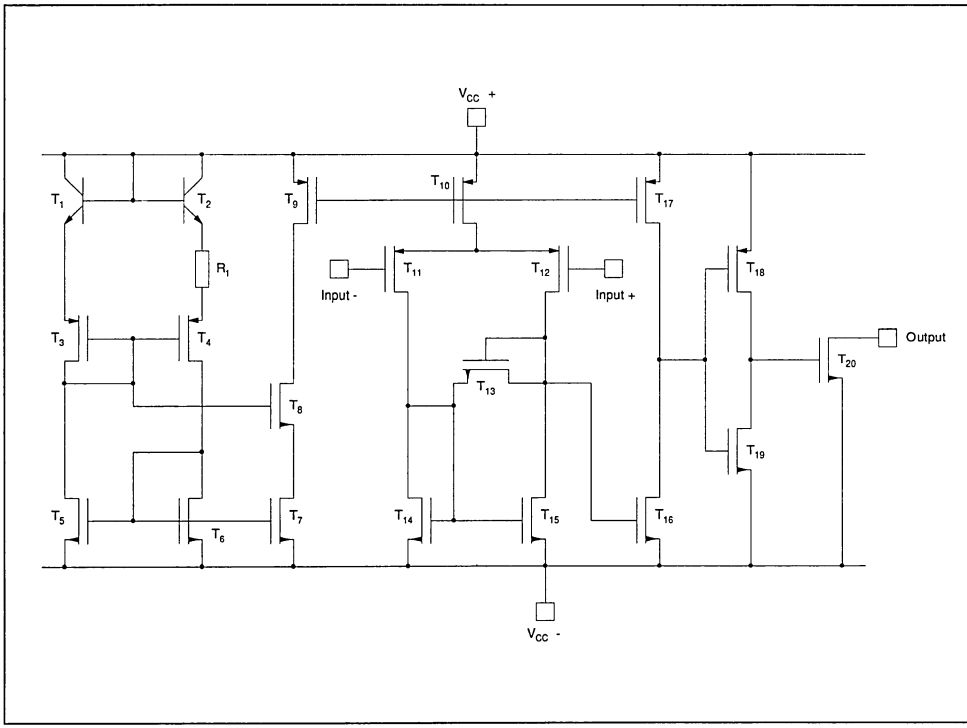
339-01.TBL

PIN CONNECTIONS (top view)



339-01.EPS

SCHEMATIC DIAGRAM (for 1/4 TS3V339)



339-02.EPS

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage - (note 1)	18	V
V_{id}	Differential Input Voltage - (note 2)	±18	V
V_i	Input Voltage - (note 3)	18	V
V_O	Output Voltage	18	V
I_O	Output Current	20	mA
T_{oper}	Operating Free-Air Temperature Range TS3V339I	 -40 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

339-02 TBL

Notes : 1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage.
4. Short circuit from outputs to V_{CC}^+ can cause excessive heating and eventual destruction.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	2.7 to 16	V
V_{icm}	Common Mode Input Voltage Range	0 to V_{CC}^+ -1.5	V

339-03 TBL

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = 3V$, $V_{CC}^- = 0V$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage - (note 1) $V_{ic} = 1.5V$ $T_{min} \leq T_{amb} \leq T_{max}$.			5 6.5	mV
I_{io}	Input Offset Current - (note 2) $V_{ic} = 1.5$ V $T_{min} \leq T_{amb} \leq T_{max}$.		1	 300	pA
I_{ib}	Input Bias Current - (note 2) $V_{ic} = 1.5$ V $T_{min} \leq T_{amb} \leq T_{max}$.		1	 600	pA
V_{icm}	Input Common Mode Voltage Range $T_{min} \leq T_{amb} \leq T_{max}$.	0 to V_{CC}^+-1.2 0 to V_{CC}^+ -1.5			V
CMR	Common-mode Rejection Ratio $V_{ic} = V_{icm\ min}$.		70		dB
SVR	Supply Voltage Rejection Ratio $V_{CC}^+ = 3V$ to $5V$		70		dB
I_{OH}	High Level Output Current $V_{id} = -1V$, $V_{OH} = 3V$ $T_{min.} \leq T_{amb} \leq T_{max}$.		2	40 1000	mA
V_{OL}	Low Level Output Voltage $V_{id} = -1V$, $I_{OL} = -6mA$ $T_{min} \leq T_{amb} \leq T_{max}$.		400	500 600	mV
I_{CC}	Supply Current (each comparator) No load - Outputs low $T_{min} \leq T_{amb} \leq T_{max}$.		9	20 25	µA
t_{PLH}	Response Time Low to High $V_{ic} = 0V$, f = 10kHz, $R_L = 5.1k\Omega$, $C_L = 15pF$, Overdrive = 5mV TTL Input		2 0.7		µs
t_{PHL}	Response Time High to Low $V_{ic} = 0V$, f = 10kHz, $R_L = 5.1k\Omega$, $C_L = 50pF$, Overdrive = 5mV TTL Input		2.5 0.08		µs

339-04.TBL

Note : 1. The specified offset voltage is the maximun value required to drive the output up to 4.5V or down to 0.3V.
2. Maximum values including unavoidable inaccuracies of the industrial test.

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = 5V$, $V_{CC}^- = 0V$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage - (note 1) $V_{ic} = 2.5V$ $T_{min} \leq T_{amb} \leq T_{max}$.		1.4	5 6.5	mV
I_{io}	Input Offset Current - (note 2) $V_{ic} = 2.5$ V $T_{min} \leq T_{amb} \leq T_{max}$.		1	 300	pA
I_{ib}	Input Bias Current - (note 2) $V_{ic} = 2.5$ V $T_{min} \leq T_{amb} \leq T_{max}$.		1	 600	pA
V_{icm}	Input Common Mode Voltage Range $T_{min} \leq T_{amb} \leq T_{max}$.	0 to V_{CC}^+-1.2 0 to V_{CC}^+ -1.5			V
CMR	Common-mode Rejection Ratio $V_{ic} = V_{icm\ min}$.		70		dB
SVR	Supply Voltage Rejection Ratio $V_{CC}^+ = +5V$ to $+10V$		80		dB
I_{OH}	High Level Output Current $V_{id} = 1V$, $V_{OH} = +5V$ $T_{min} \leq T_{amb} \leq T_{max}$.		2	40 1000	mA
V_{OL}	Low Level Output Voltage $V_{id} = -1V$, $I_{OL} = 6mA$ $T_{min} \leq T_{amb} \leq T_{max}$.		260	400 650	mV
I_{CC}	Supply Current (each comparator) No load - Outputs low $T_{min} \leq T_{amb} \leq T_{max}$.		10	20 25	µA
t_{PLH}	Response Time Low to High $V_{ic} = 0V$, f = 10kHz, $R_L = 5.1k\Omega$, $C_L = 50pF$, Overdrive = 5mV TTL Input		1.5 0.7		µs
t_{PHL}	Response Time High to Low $V_{ic} = 0V$, f = 10kHz, $R_L = 5.1k\Omega$, $C_L = 50pF$, Overdrive = 5mV TTL Input		2.5 0.08		µs

339-05.TBL

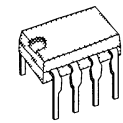
Note : 1. The specified offset voltage is the maximun value required to drive the output up to 4.5V or down to 0.3V.
2. Maximum values including unavoidable inaccuracies of the industrial test.

SGS-THOMSON MICROELECTRONICS

TS3V393

3V MICROPOWER DUAL VOLTAGE COMPARATORS

- DEDICATED TO **3.3V** OR **BATTERY SUPPLY** (specified at 3V and 5V)
- EXTREMELY LOW SUPPLY CURRENT : **9µA typ/comparator**
- WIDE SINGLE SUPPLY RANGE **2.7V to 16V**
- EXTREMELY LOW INPUT CURRENTS : **1pA TYP**
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GND
- FAST RESPONSE TIME : 2.5µs typ for 5mV overdrive
- PIN-TO-PIN AND FUNCTIONALLY COMPATIBLE WITH BIPOLAR LM393



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

DESCRIPTION

The TS3V393 is a micropower dual CMOS voltage comparator with extremely low consumption of 9µA typ / comparator (20 times less than bipolar LM393). Similar performances are offered by the dual micropower comparator TS3V3702 with a push-pull CMOS output.

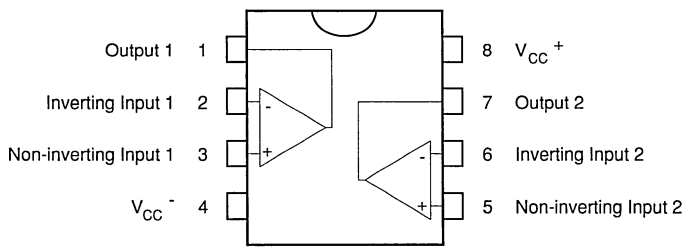
Thus response times remain similar to the LM393.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS3V393I	-40°C, +125°C	•	•

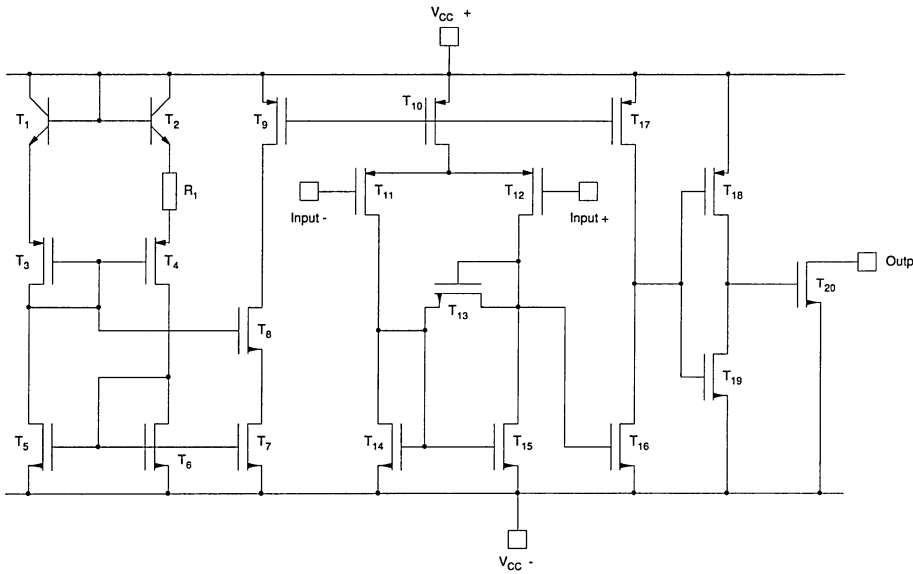
393-01.TBL

PIN CONNECTIONS (top view)



393-01.EPS

SCHEMATIC DIAGRAM (for 1/2 TS3V393)



393-02.EPS

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage - (note 1)	18	V
V_{id}	Differential Input Voltage - (note 2)	±18	V
V_i	Input Voltage - (note 3)	18	V
V_O	Output Voltage	18	V
I_O	Output Current	20	mA
T_{oper}	Operating Free-Air Temperature Range TS3V393I	-40 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

393-02.TBL

Notes : 1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage.
4. Short circuit from outputs to V_{CC}^+ can cause excessive heating and eventual destruction.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	2.7 to 16	V
V_{icm}	Common Mode Input Voltage Range	0 to V_{CC}^+ -1.5	V

393-03.TBL

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = 3V$, $V_{CC}^- = 0V$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage - (note 1) $V_{ic} = 1.5V$ $T_{min} \leq T_{amb} \leq T_{max}$.			5 6.5	mV
I_{io}	Input Offset Current - (note 2) $V_{ic} = 1.5$ V $T_{min.} \leq T_{amb} \leq T_{max}$.		1	 300	pA
I_{ib}	Input Bias Current - (note 2) $V_{ic} = 1.5$ V $T_{min} \leq T_{amb} \leq T_{max}$.		1	 600	pA
V_{icm}	Input Common Mode Voltage Range $T_{min.} \leq T_{amb} \leq T_{max}$.	0 to V_{CC}^+-1.2 0 to V_{CC}^+ -1.5			V
CMR	Common-mode Rejection Ratio $V_{ic} = V_{icm\ min.}$		70		dB
SVR	Supply Voltage Rejection Ratio $V_{CC}^+ = 3V$ to 5V		70		dB
I_{OH}	High Level Output Current $V_{id} = -1V$, $V_{OH} = 3V$ $T_{min} \leq T_{amb} \leq T_{max}$.		2	40 1000	mA
V_{OL}	Low Level Output Voltage $V_{id} = -1V$, $I_{OL} = -6mA$ $T_{min.} \leq T_{amb} \leq T_{max}$.		400	500 600	mV
I_{CC}	Supply Current (each comparator) No load - Outputs low $T_{min} \leq T_{amb} \leq T_{max}$.		9	20 25	µA
t_{PLH}	Response Time Low to High $V_{ic} = 0V$, f = 10kHz, $R_L = 5.1k\Omega$, $C_L = 15pF$, Overdrive = 5mV TTL Input		2 0.7		µs
t_{PHL}	Response Time High to Low $V_{ic} = 0V$, f = 10kHz, $R_L = 5.1k\Omega$, $C_L = 50pF$, Overdrive = 5mV TTL Input		2.5 0.08		µs

393-04 TBL

Note : 1. The specified offset voltage is the maximun value required to drive the output up to 4.5V or down to 0.3V.
2. Maximum values including unavoidable inaccuracies of the industrial test.

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = 5V$, $V_{CC}^- = 0V$, $T_{amb} = 25°C$ (unless otherwise specified)

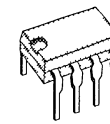
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage - (note 1) $V_{ic} = 2.5V$ $T_{min} \leq T_{amb} \leq T_{max}$.		1.4	5 6.5	mV
I_{io}	Input Offset Current - (note 2) $V_{ic} = 2.5$ V $T_{min} \leq T_{amb} \leq T_{max}$.		1	300	pA
I_{ib}	Input Bias Current - (note 2) $V_{ic} = 2.5$ V $T_{min} \leq T_{amb} \leq T_{max}$.		1	600	pA
V_{icm}	Input Common Mode Voltage Range $T_{min} \leq T_{amb} \leq T_{max}$.	0 to V_{CC}^+-1.2 0 to V_{CC}^+ -1.5			V
CMR	Common-mode Rejection Ratio $V_{ic} = V_{icm\ min}$.		70		dB
SVR	Supply Voltage Rejection Ratio $V_{CC}^+ = +5V$ to $+10V$		80		dB
I_{OH}	High Level Output Current $V_{id} = 1V$, $V_{OH} = +5V$ $T_{min} \leq T_{amb} \leq T_{max}$.		2	40 1000	mA
V_{OL}	Low Level Output Voltage $V_{id} = -1V$, $I_{OL} = 6mA$ $T_{min} \leq T_{amb} \leq T_{max}$.		260	400 650	mV
I_{CC}	Supply Current (each comparator) No load - Outputs low $T_{min} \leq T_{amb} \leq T_{max}$.		10	20 25	µA
t_{PLH}	Response Time Low to High $V_{ic} = 0V$, f = 10kHz, $R_L = 5.1k\Omega$, $C_L = 50pF$, Overdrive = 5mV TTL Input		1.5 0.7		µs
t_{PHL}	Response Time High to Low $V_{ic} = 0V$, f = 10kHz, $R_L = 5.1k\Omega$, $C_L = 50pF$, Overdrive = 5mV TTL Input		2.5 0.08		µs

393-05.TBL

Note : 1. The specified offset voltage is the maximun value required to drive the output up to 4.5V or down to 0.3V.
2 Maximum values including unavoidable inaccuracies of the industrial test.

3V LOW POWER SINGLE TIMERS

- DEDICATED TO **3.3V** OR **BATTERY SUPPLY** (Specified at 3V and 5V plus 1.5V for A version)
- VERY LOW POWER CONSUMPTION : **90µA at V_{CC} = 3V**
- WIDE SINGLE SUPPLY RANGE : **+1.5V to +16V**
- HIGH OUTPUT CURRENT CAPABILITY
- SUPPLY CURRENT SPIKES REDUCED DURING OUTPUT TRANSITIONS
- HIGH INPUT IMPEDANCE : $10^{12}\ \Omega$
- PIN-TO-PIN AND FUNCTIONALLY COMPATIBLE WITH BIPOLAR NE555 AND CMOS TS555
- OUTPUT COMPATIBLE WITH TTL,CMOS AND LOGIC MOS



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

DESCRIPTION

The TS3V555 with its low consumption (90µA at V_{CC} = 3V) is a single CMOS timer dedicated to 3.3V or battery supply (specified at 3V and 5V plus 1.5V for A version) offering also a high frequency ($f_{(max)}$ 2MHz at V_{CC} = 3V and 2.7 MHz at V_{CC} = 5V). Thus, either in monostable or astable mode, timing remains very accurate.

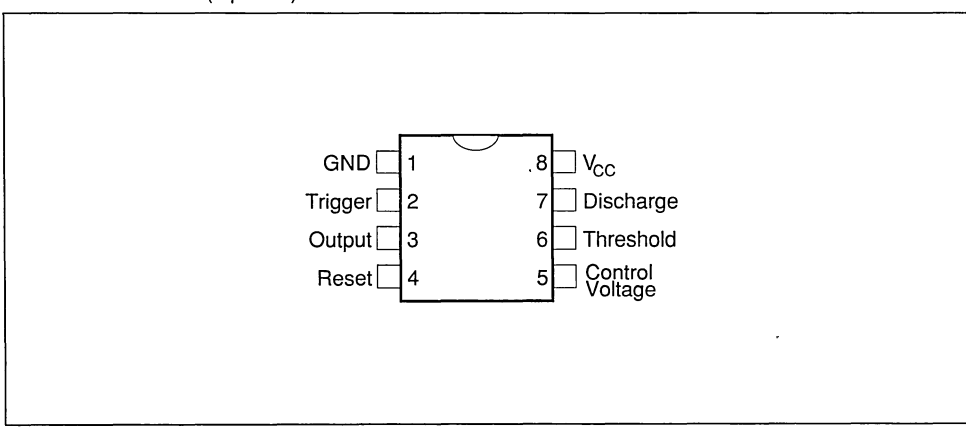
Timing capacitors can also be minimized due to high input impedance ($10^{12}\ \Omega$).

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS3V555I,AI	-40, +125°C	●	●

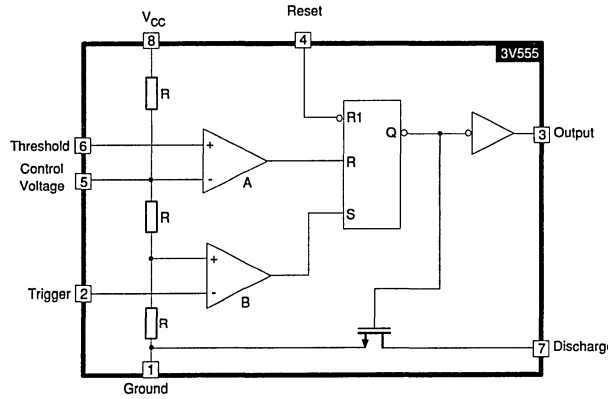
3V555-01 TBL

PIN CONNECTIONS (top view)



3V555-01 EPS

BLOCK DIAGRAM



3V555-02 EPS

FUNCTION TABLE

RESET	TRIGGER	THRESHOLD	OUTPUT
Low	x	x	Low
High	Low	x	High
High	High	High	Low
High	High	Low	Previous State

3V555-02 TBL

LOW ↔ Level Voltage ≤ Min voltage specified

HIGH ↔ Level Voltage ≥ Max voltage specified

X ↔ Irrelevant

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+18	V
T_J	Junction Temperature	+150	°C

3V555-03 TBL

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
T_{oper}	Operating Temperature Range TS3V555I,AI	-40 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

3V555-04 TBL

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+1.5 to +16	V

3V555-05 TBL

ELECTRICAL CHARACTERISTICS

V_{CC} = +3V , T_{amb} = +25°C , Reset to V_{CC} (unless otherwise specified)

STATIC

Symbol	Parameter	TS3V555I,AI			Unit
		Min.	Typ.	Max.	
I_{CC}	Supply Current - (no load, High and Low States) T_{amb} = +25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		90	230 230	µA
V_{CL}	Control Voltage T_{amb} = +25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	1.8 1.7	2	2.2 2.3	V
V_{DIS}	Discharge Saturation Voltage (I_{DIS} = 1mA) T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max.}$		0.05 -	0.2 0.25	V
V_{OL}	Low Level Output Voltage (I_{SINK} = 1mA) T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max.}$		0.1	0.3 0.35	V
V_{OH}	High Level Output Voltage (I_{SOURCE} = -0.3mA) T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max.}$	2.5 2.5	2.9		V
V_{TRIG}	Trigger Voltage T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max.}$	0.9 0.8	1	1.1 1.2	V
I_{TRIG}	Trigger Current		10		pA
I_{TH}	Threshold Current		10		pA
V_{RESET}	Reset Voltage T_{amb} = +25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	0.4 0.3	1.1	1.5 2.0	V
I_{RESET}	Reset Current		10		pA
I_{DIS}	Discharge Pin Leakage Current		1	100	nA

3V555-06 TBL

DYNAMIC

Symbol	Parameter	TS3V555I,AI			Unit
		Min.	Typ.	Max.	
	Timing Accuracy (Monostable) R = 10kΩ , C = 0.1µF - (note 1)		1		%
	Timing Shift with supply voltage variations (Monostable) R = 10kΩ , C = 0.1µF, V_{CC} = +3V +/-0.3V - (note 1)		0.5		%/V
	Timing Shift with temperature - (note 1) $T_{min.} \leq T_{amb} \leq T_{max.}$		75		ppm/°C
fmax	Maximum astable frequency - (note 2) R_A = 470Ω , R_B = 200Ω, C = 200pF		2		MHz
	Astable frequency accuracy - (note 2) $R_A = R_B$ = 1kΩ to 100kΩ, C = 0.1µF		5		%
	Timing Shift with supply voltage variations (Astable mode) - (note 2) $R_A = R_B$ = 10kΩ, C = 0.1µF, V_{CC} = +3 to+5V		0.5		%/V
t_r	Output Rise Time (C_{LOAD} = 10pF)		25		ns
t_f	Output Fall Time (C_{LOAD} = 10pF)		20		ns
t_{PD}	Trigger Propagation Delay		100		ns
t_{RPW}	Minimum Reset Pulse Width (V_{TRIG} = +3V)		350		ns

3V555-07 TBL

Note : 1. See Figure 2
2. See Figure 4

ELECTRICAL CHARACTERISTICS

V_{CC} = +5V , T_{amb} = +25°C , Reset to V_{CC} (unless otherwise specified)

STATIC

Symbol	Parameter	TS3V555I,AI			Unit
		Min.	Typ.	Max.	
I_{CC}	Supply Current - (no load, High and Low States) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$		110	250 250	µA
V_{CL}	Control Voltage T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$	2.9 2.8	3.3	3.8 3.9	V
V_{DIS}	Discharge Saturation Voltage (I_{DIS} = 10mA) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$		0.2	0.3 0.35	V
V_{OL}	Low Level Output Voltage (I_{SINK} = 8mA) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$		0.3	0.6 0.8	V
V_{OH}	High Level Output Voltage (I_{SOURCE} = -2mA) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$	4.4 4.4	4.6		V
V_{TRIG}	Trigger Voltage T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$	1.36 1.26	1.67	1.96 2.06	V
I_{TRIG}	Trigger Current		10		pA
I_{TH}	Threshold Current		10		pA
V_{RESET}	Reset Voltage T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$	0.4 0.3	1.1	1.5 2.0	V
I_{RESET}	Reset Current		10		pA
I_{DIS}	Discharge Pin Leakage Current		1	100	nA

3V555-08 TBL

DYNAMIC

Symbol	Parameter	TS3V555I,AI			Unit
		Min.	Typ.	Max.	
	Timing Accuracy (Monostable) - (note1) R = 10kΩ , C = 0.1µF - (note 1)		2		%
	Timing Shift with supply voltage variations (Monostable) - (note1) R = 10kΩ , C = 0.1µF, V_{CC} = +5V +/-1V		0.38		%/V
	Timing Shift with temperature - (note1) $T_{min.} \le T_{amb} \le T_{max.}$		75		ppm/°C
fmax	Maximum astable frequency - (note 2) R_A = 470Ω , R_B = 200Ω, C = 200pF		2.7		MHz
	Astable frequency accuracy - (note 2) $R_A = R_B$ = 1kΩ to 100kΩ, C = 0.1µF		3		%
	Timing Shift with supply voltage variations (Astable mode) - (note 2) $R_A = R_B$ = 10kΩ, C = 0.1µF, V_{CC} = +5V to+12V		0.1		%/V
t_r	Output Rise Time (C_{LOAD} = 10pF)		25		ns
t_f	Output Fall Time (C_{LOAD} = 10pF)		20		ns
t_{PD}	Trigger Propagation Delay		100		ns
t_{RPW}	Minimum Reset Pulse Width (V_{TRIG} = +5V)		350		ns

3V555-09 TBL

Note : 1. See Figure 2
2. See Figure 4

ELECTRICAL CHARACTERISTICS

TS3V555AI only

V_{CC} = +1.5V , T_{amb} = +25°C, Reset to V_{CC} (unless otherwise specified)

STATIC

Symbol	Parameter	TS3V555AI			Unit
		Min.	Typ.	Max.	
I_{CC}	Supply Current - (no load, High and Low States) T_{amb} = +25°C		50	150	µA
V_{CL}	Control Voltage T_{amb} = +25°C	0.8	1.0	1.2	V
V_{DIS}	Discharge Saturation Voltage (I_{DIS} = 1mA) T_{amb} = +25°C		75	150	mV
V_{OL}	Low Level Output Voltage (I_{SINK} = 1mA) T_{amb} = +25°C		0.2	0.4	V
V_{OH}	High Level Output Voltage (I_{SOURCE} = -0.25mA) T_{amb} = +25°C	1.0	1.25		V
V_{TRIG}	Trigger Voltage T_{amb} = +25°C	0.4	0.5	0.6	V
I_{TRIG}	Trigger Current		10		pA
I_{TH}	Threshold Current		10		pA
V_{RESET}	Reset Voltage T_{amb} = +25°C	0.4	1.1	1.4	V
I_{RESET}	Reset Current		10		pA

3V555-10.TBL

DYNAMIC

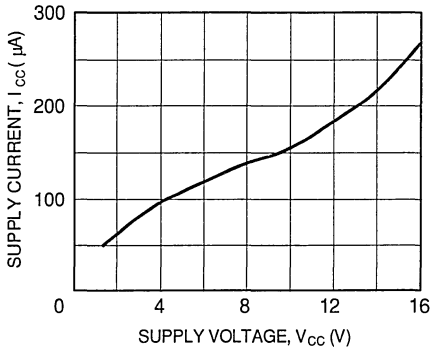
Symbol	Parameter	TS3V555AI			Unit
		Min.	Typ.	Max.	
	Timing Accuracy (Monostable) R = 10kΩ , C = 0.1µF - (note 1)		4		%

3V555-11.TBL

Note : 1. See Figure 2

TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each timer) versus supply voltage.



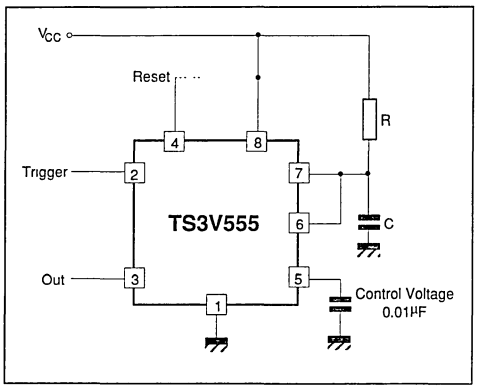
3V555-03 EPS

APPLICATION INFORMATION

MONOSTABLE OPERATION

In the monostable mode,the timer functions as a one-shot. Referring to figure 2 the external capacitor is initially held discharged by a transistor inside the timer.

Figure 2



3V555-04 EPS

The circuit triggers on a negative-going input signal when the level reaches 1/3 V_{CC}. Once triggered,the circuit remains in this state until the set time has elapsed,even if it is triggered again during this interval. The duration of the output HIGH state is given by t = 1.1 R x C.

Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the Reset terminal (pin 4) and the Trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its LOW state.

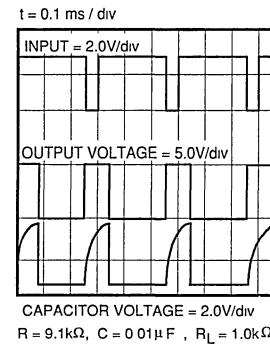
When a negative trigger pulse is applied to pin 2, the flip-flop is set, releasing the short circuit across the external capacitor and driving the output HIGH. The voltage across the capacitor increases exponentially with the time constant τ = R x C.

When the voltage across the capacitor equals 2/3 V_{CC}, the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state.

Figure 3 shows the actual waveforms generated in this mode of operation.

When Reset is not used, it should be tied high to avoid any possible or false triggering.

Figure 3



3V555-05 EPS

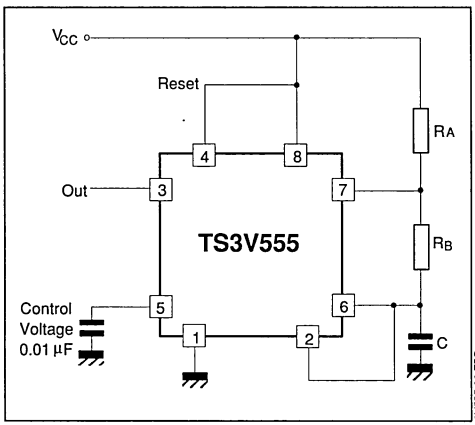
ASTABLE OPERATION

When the circuit is connected as shown in figure 4 (pin 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times and therefore frequency, are independent of the supply voltage.

Figure 5 shows actual waveforms generated in this mode of operation.

Figure 4



The charge time (output HIGH) is given by :

$t1 = 0.693 (R_A + R_B) C$

and the discharge time (output LOW) by :

$t2 = 0.693 (R_B) C$

Thus the total period T is given by :

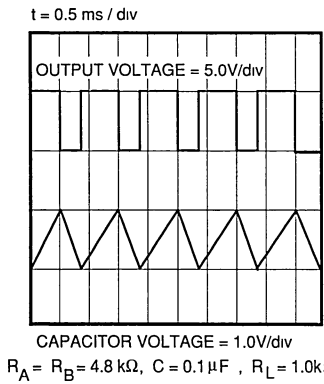
$T = t1 + t2 = 0.693 (R_A + 2R_B) C$

The frequency of oscillation is then :

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B) C}$$

The duty cycle is given by : $D = \frac{R_B}{R_A + 2R_B}$

Figure 5

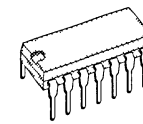


SGS-THOMSON MICROELECTRONICS

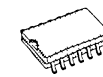
TS3V556

3V LOW POWER DUAL TIMERS

- DEDICATED TO **3.3V** OR **BATTERY SUPPLY** (Specified at 3V and 5V plus 1.5V for A version)
- VERY LOW POWER CONSUMPTION : **90µA/tim at V_{CC} = 3V**
- WIDE SINGLE SUPPLY RANGE : **+1.5V to +16V**
- HIGH OUTPUT CURRENT CAPABILITY
- SUPPLY CURRENT SPIKES REDUCED DURING OUTPUT TRANSITIONS
- HIGH INPUT IMPEDANCE : **10^{12} Ω**
- PIN-TO-PIN AND FUNCTIONALLY COMPATIBLE WITH BIPOLAR NE556 AND CMOS TS556
- OUTPUT COMPATIBLE WITH TTL,CMOS AND LOGIC MOS



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

DESCRIPTION

The TS3V556 with its low consumption (90µA/tim at V_{CC} = 3V) is a dual CMOS timer dedicated to 3.3V or battery supply (specified at 3V and 5V plus 1.5V for A version) offering also a high frequency ($f_{(max)}$ 2MHz at V_{CC} = 3V and 2.7 MHz at V_{CC} = 5V). Thus, either in monostable or astable mode, timing remains very accurate.

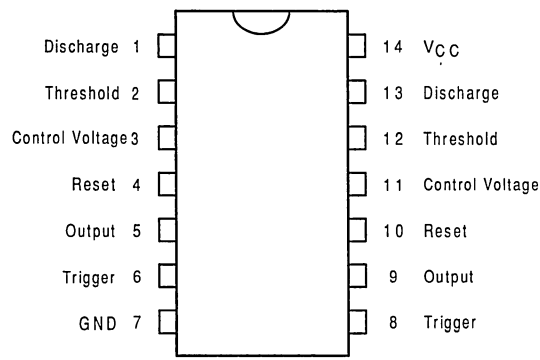
Timing capacitors can also be minimized due to high input impedance (10^{12} Ω).

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS3V556I,AI	-40, +125°C	●	●

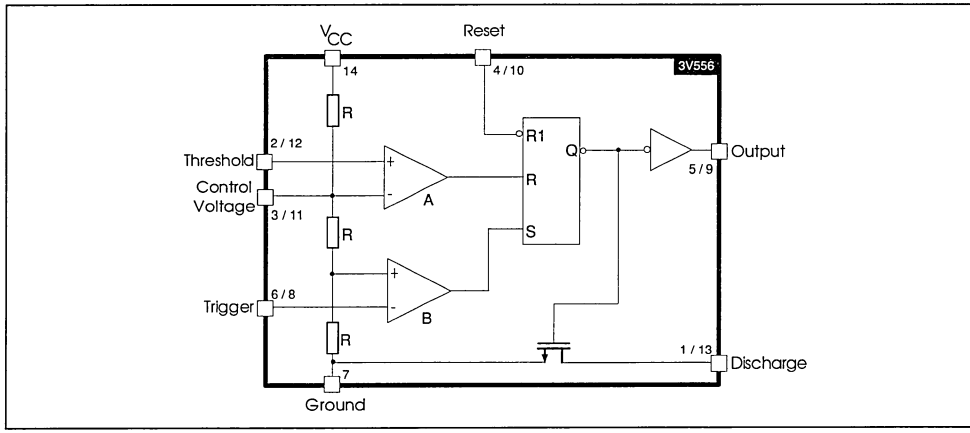
3V556-01 TBL

PIN CONNECTIONS (top view)



3V556-01 EPS

BLOCK DIAGRAM (1/2 TS3V556)



FUNCTION TABLE

RESET	TRIGGER	THRESHOLD	OUTPUT
Low	x	x	Low
High	Low	x	High
High	High	High	Low
High	High	Low	Previous State

3V556-02 TBL

LOW ↔ Level Voltage ≤ Min voltage specified

HIGH ↔ Level Voltage ≥ Max voltage specified

X ↔ Irrelevant

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+18	V
T_J	Junction Temperature	+150	°C

3V556-03 TBL

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
T_{oper}	Operating Temperature Range TS3V556I,AI	-40 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

3V556-04 TBL

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+1.5 to +16	V

3V556-05 TBL

ELECTRICAL CHARACTERISTICS

V_{CC} = +3V , T_{amb} = +25°C , Reset to V_{CC} (unless otherwise specified)

STATIC

Symbol	Parameter	TS3V556I,AI			Unit
		Min.	Typ.	Max.	
I_{CC}	Supply Current - (no load, High and Low States, per timer) T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$.		90	230 230	µA
V_{CL}	Control Voltage T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$.	1.8 1.7	2	2.2 2.3	V
V_{DIS}	Discharge Saturation Voltage (I_{DIS} = 1mA) T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$.		0.05 -	0.2 0.25	V
V_{OL}	Low Level Output Voltage (I_{SINK} = 1mA) T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$.		0.1	0.3 0.35	V
V_{OH}	High Level Output Voltage (I_{SOURCE} = -0.3mA) T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$.	2.5 2.5	2.9		V
V_{TRIG}	Trigger Voltage T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$.	0.9 0.8	1	1.1 1.2	V
I_{TRIG}	Trigger Current		10		pA
I_{TH}	Threshold Current		10		pA
V_{RESET}	Reset Voltage T_{amb} = +25°C $T_{min.} \leq T_{amb} \leq T_{max}$	0.4 0.3	1.1	1.5 2.0	V
I_{RESET}	Reset Current		10		pA
I_{DIS}	Discharge Pin Leakage Current		1	100	nA

3V556-06 TBL

DYNAMIC

Symbol	Parameter	TS3V556I,AI			Unit
		Min.	Typ.	Max.	
	Timing Accuracy (Monostable) R = 10kΩ , C = 0.1µF - (note 1)		1		%
	Timing Shift with supply voltage variations (Monostable) R = 10kΩ , C = 0.1µF, V_{CC} = +3V +/-0.3V - (note 1)		0.5		%/V
	Timing Shift with temperature - (note 1) $T_{min.} \leq T_{amb} \leq T_{max}$.		75		ppm/°C
fmax	Maximum astable frequency - (note 2) R_A = 470Ω , R_B = 200Ω, C = 200pF		2		MHz
	Astable frequency accuracy - (note 2) $R_A = R_B$ = 1kΩ to 100kΩ, C = 0.1µF		5		%
	Timing Shift with supply voltage variations (Astable mode) - (note 2) $R_A = R_B$ = 10kΩ, C = 0.1µF, V_{CC} = +3 to+5V		0.5		%/V
t_r	Output Rise Time (C_{LOAD} = 10pF)		25		ns
t_f	Output Fall Time (C_{LOAD} = 10pF)		20		ns
t_{PD}	Trigger Propagation Delay		100		ns
t_{RPW}	Minimum Reset Pulse Width (V_{TRIG} = +3V)		350		ns

3V556-07 TBL

Note : 1. See Figure 2
2. See Figure 4

ELECTRICAL CHARACTERISTICS

V_{CC} = +5V , T_{amb} = +25°C , Reset to V_{CC} (unless otherwise specified)

STATIC

Symbol	Parameter	TS3V556I,AI			Unit
		Min.	Typ.	Max.	
I_{CC}	Supply Current - (no load, High and Low States, per timer) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$		110	250 250	µA
V_{CL}	Control Voltage T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$	2.9 2.8	3.3	3.8 3.9	V
V_{DIS}	Discharge Saturation Voltage (I_{DIS} = 10mA) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$		0.2	0.3 0.35	V
V_{OL}	Low Level Output Voltage (I_{SINK} = 8mA) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$		0.3	0.6 0.8	V
V_{OH}	High Level Output Voltage (I_{SOURCE} = -2mA) T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$	4.4 4.4	4.6		V
V_{TRIG}	Trigger Voltage T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$	1.36 1.26	1.67	1.96 2.06	V
I_{TRIG}	Trigger Current		10		pA
I_{TH}	Threshold Current		10		pA
V_{RESET}	Reset Voltage T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$	0.4 0.3	1.1	1.5 2.0	V
I_{RESET}	Reset Current		10		pA
I_{DIS}	Discharge Pin Leakage Current		1	100	nA

3V556-08 TBL

DYNAMIC

Symbol	Parameter	TS3V556I,AI			Unit
		Min.	Typ.	Max.	
	Timing Accuracy (Monostable) - (note1) R = 10kΩ , C = 0.1µF - (note 1)		2		%
	Timing Shift with supply voltage variations (Monostable) - (note1) R = 10kΩ , C = 0.1µF, V_{CC} = +5V +/-1V		0.38		%/V
	Timing Shift with temperature - (note1) $T_{min.} \le T_{amb} \le T_{max.}$		75		ppm/°C
fmax	Maximum astable frequency - (note 2) R_A = 470Ω , R_B = 200Ω, C = 200pF		2.7		MHz
	Astable frequency accuracy - (note 2) $R_A = R_B$ = 1kΩ to 100kΩ, C = 0.1µF		3		%
	Timing Shift with supply voltage variations (Astable mode) - (note 2) $R_A = R_B$ = 10kΩ, C = 0.1µF, V_{CC} = +5V to+12V		0.1		%/V
t_r	Output Rise Time (C_{LOAD} = 10pF)		25		ns
t_f	Output Fall Time (C_{LOAD} = 10pF)		20		ns
t_{PD}	Trigger Propagation Delay		100		ns
t_{RPW}	Minimum Reset Pulse Width (V_{TRIG} = +5V)		350		ns

3V556-09 TBL

Note : 1. See Figure 2
2. See Figure 4

ELECTRICAL CHARACTERISTICS

TS3V556AI only

V_{CC} = +1.5V , T_{amb} = +25°C, Reset to V_{CC} (unless otherwise specified)

STATIC

Symbol	Parameter	TS3V556AI			Unit
		Min.	Typ.	Max.	
I_{CC}	Supply Current - (no load, High and Low States, per timer) T_{amb} = +25°C		50	150	µA
V_{CL}	Control Voltage T_{amb} = +25°C	0.8	1.0	1.2	V
V_{DIS}	Discharge Saturation Voltage (I_{DIS} = 1mA) T_{amb} = +25°C		75	150	mV
V_{OL}	Low Level Output Voltage (I_{SINK} = 1mA) T_{amb} = +25°C		0.2	0.4	V
V_{OH}	High Level Output Voltage (I_{SOURCE} = -0.25mA) T_{amb} = +25°C	1.0	1.25		V
V_{TRIG}	Trigger Voltage T_{amb} = +25°C	0.4	0.5	0.6	V
I_{TRIG}	Trigger Current		10		pA
I_{TH}	Threshold Current		10		pA
V_{RESET}	Reset Voltage T_{amb} = +25°C	0.4	1.1	1.4	V

3V556-10 TBL

DYNAMIC

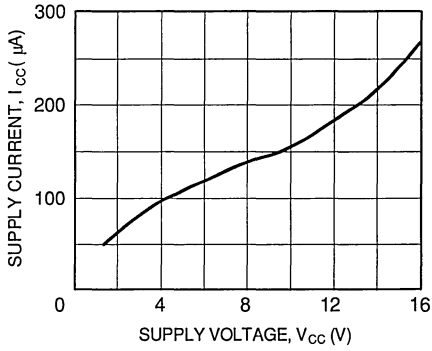
Symbol	Parameter	TS3V556AI			Unit
		Min.	Typ.	Max.	
	Timing Accuracy (Monostable) R = 10kΩ , C = 0.1µF - (note 1)		4		%

3V556 11 TBL

Note : 1. See Figure 2

TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each timer) versus supply voltage.



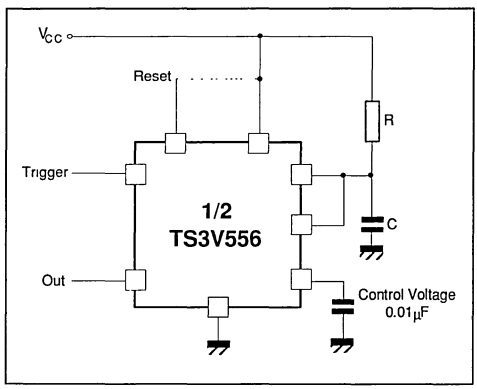
3V556-03 EPS

APPLICATION INFORMATION

MONOSTABLE OPERATION

In the monostable mode,the timer functions as a one-shot. Referring to figure 2 the external capacitor is initially held discharged by a transistor inside the timer.

Figure 2



3V556-04 EPS

The circuit triggers on a negative-going input signal when the level reaches 1/3 V_{CC}. Once triggered,the circuit remains in this state until the set time has elapsed,even if it is triggered again during this interval. The duration of the output HIGH state is given by t = 1.1 R x C.

Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the Reset terminal (pin 4 or 10) and the Trigger terminal (pin 2 or 8) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its LOW state.

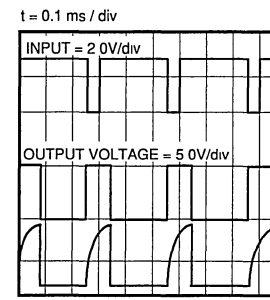
When a negative trigger pulse is applied to the trigger terminal, the flip-flop is set, releasing the short circuit across the external capacitor and driving the output HIGH. The voltage across the capacitor increases exponentially with the time constant τ = R x C.

When the voltage across the capacitor equals 2/3 V_{CC}, the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state.

Figure 3 shows the actual waveforms generated in this mode of operation.

When Reset is not used, it should be tied high to avoid any possible or false triggering.

Figure 3



3V556-05 EPS

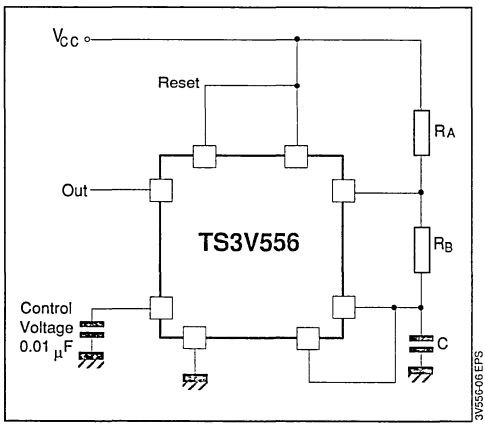
ASTABLE OPERATION

When the circuit is connected as shown in figure 4 , it triggers itself and free runs as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times and therefore frequency, are independent of the supply voltage.

Figure 5 shows actual waveforms generated in this mode of operation.

Figure 4



The charge time (output HIGH) is given by :

$t1 = 0.693\ (R_A + R_B)\ C$

and the discharge time (output LOW) by :

$t2 = 0.693\ (R_B)\ C$

Thus the total period T is given by :

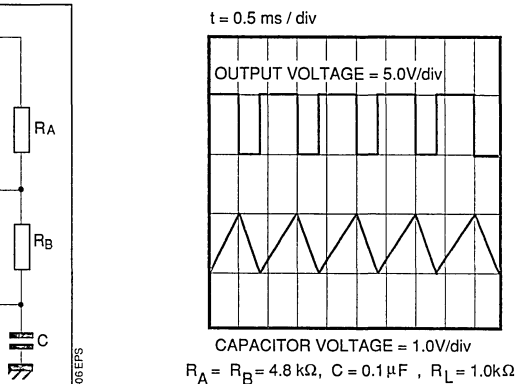
$T = t1 + t2 = 0.693\ (R_A + 2R_B)\ C$

The frequency of oscillation is then :

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\ C}$$

The duty cycle is given by : $D = \dfrac{R_B}{R_A + 2R_B}$

Figure 5

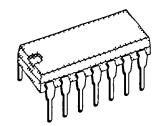


SGS-THOMSON MICROELECTRONICS

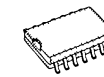
TS3V902

3V INPUT/OUTPUT **RAIL TO RAIL** DUAL OPERATIONAL AMPLIFIER (WITH **STANDBY** POSITION)

- DEDICATED TO **3.3V** OR **BATTERY SUPPLY** (specified at 3V and 5V)
- RAIL TO RAIL INPUT AND OUTPUT VOLTAGE RANGES
- **STANDBY** POSITION : REDUCED **CONSUMPTION (1µA)** AND **HIGH IMPEDANCE OUTPUTS**
- SINGLE SUPPLY OPERATION FROM **2.7V TO 16V**
- EXTREMELY LOW INPUT BIAS CURRENT : **1pA** TYP
- LOW INPUT OFFSET VOLTAGE : **1.5mV max.**
- SPECIFIED FOR **600Ω** AND **100Ω** LOADS
- LOW SUPPLY CURRENT : 200µA/Ampli



N
DIP14
(Plastic Package)



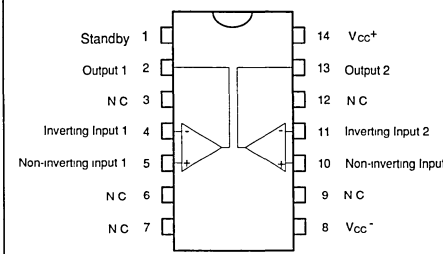
D
SO14
(Plastic Micropackage)

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS3V902I/AI/BI	-40, +125°C	•	•

902-01 TBL

PIN CONNECTIONS (top view)



902-01 EPS

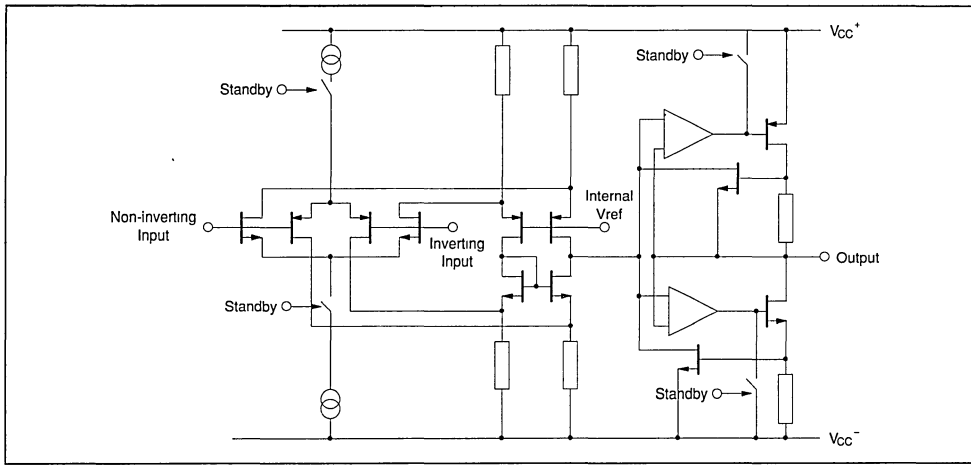
DESCRIPTION

The TS3V902 is a RAIL TO RAIL dual CMOS operational amplifier designed to operate with a single 3V supply voltage.
The input voltage range V_{icm} includes the two supply rails V_{CC}^+ and V_{CC}^-.
The output reaches :

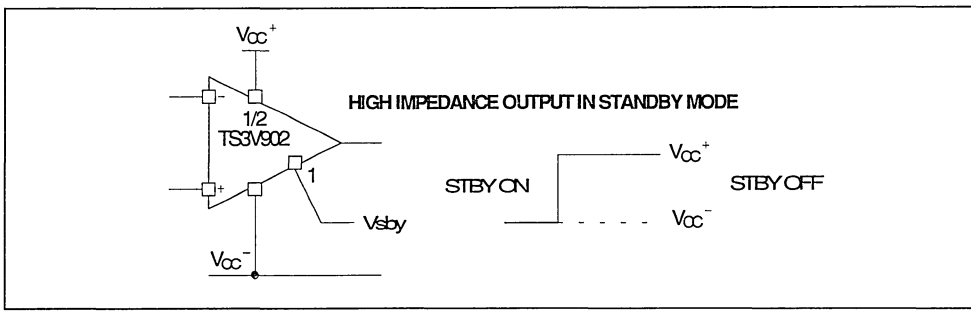
- V_{CC}^- +50mV V_{CC}^+ -50mV with R_L = 10kΩ
- V_{CC}^- +350mV V_{CC}^+ -350mV with R_L = 600Ω

This product offers a broad supply voltage operating range from 2.7V to 16V and a supply current of only 200µA/amp. (V_{CC} = 3V).
The TS3V902 can be put on STANDBY position (only 0.5µA and high impedance outputs).

SCHEMATIC DIAGRAM (1/2 TS3V902)



STANDBY POSITION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage - (note 1)	18	V
V_{id}	Differential Input Voltage - (note 2)	±18	V
V_i	Input Voltage - (note 3)	-0.3 to 18	V
I_{in}	Current on Inputs	±50	mA
I_o	Current on Outputs	±130	mA
T_{oper}	Operating Free Air Temperature Range . TS3V902I/AI/BI	-40 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

902-02 TBL

Notes : 1. All voltage values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of input and output voltages must never exceed V_{CC}^+ +0.3V.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2.7 to 16	V
V_{icm}	Common Mode Input Voltage Range	V_{CC}^- -0.2 to V_{CC}^+ +0.2	V

902-03 TBL

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = 3V$, $V_{CC}^- = 0V$, R_L,C_L connected to $V_{CC}/2$, Standby OFF, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter		TS3V902I/AI/BI Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage ($V_{ic} = V_o = V_{CC}/2$)	TS3V902			12	mV
		TS3V902A			5	
		TS3V902B			1.5	
	$T_{min} \le T_{amb} \le T_{max}$	TS3V902			12	
		TS3V902A			7	
		TS3V902B			3	
DV_{io}	Input Offset Voltage Drift			2		µV/°C
I_{io}	Input Offset Current - (note 1)			1	100	pA
	$T_{min} \le T_{amb} \le T_{max}$				200	
I_{ib}	Input Bias Current - (note 1)			1	150	pA
	$T_{min} \le T_{amb} \le T_{max}$				300	
I_{CC}	Supply Current (per amplifier, $A_{VCL} = 1$, no load)			200	300	µA
	$T_{min} \le T_{amb} \le T_{max}$				400	
CMR	Common Mode Rejection Ratio					dB
	$V_{ic} = 0$ to 3V, $V_o = 1.5V$			70		
SVR	Supply Voltage Rejection Ratio ($V_{CC}^+ = 2.7$ to 3.3V, $V_O = V_{CC}/2$)			70		dB
A_{vd}	Large Signal Voltage Gain ($R_L = 10k\Omega$, $V_O = 1.2V$ to 1.8V)		3	10		V/mV
	$T_{min} \le T_{amb} \le T_{max}$.		3			
V_{OH}	High Level Output Voltage ($V_{id} = 1V$)	$R_L = 100k\Omega$	2.95			V
		$R_L = 10k\Omega$	2.9	2.96		
		$R_L = 600\Omega$	2.2	2.6		
		$R_L = 100\Omega$		2		
	$T_{min} \le T_{amb} \le T_{max}$.	$R_L = 10k\Omega$	2.8			
		$R_L = 600\Omega$	2.1			
V_{OL}	Low Level Output Voltage ($V_{id} = -1V$)	$R_L = 100k\Omega$			50	mV
		$R_L = 10k\Omega$		50	100	
		$R_L = 600\Omega$		350	600	
		$R_L = 100\Omega$		900		
	$T_{min} \le T_{amb} \le T_{max}$	$R_L = 10k\Omega$			150	
		$R_L = 600\Omega$			900	
I_o	Output Short Circuit Current ($V_{id} = \pm 1V$)	Source ($V_o = V_{CC}^-$)		30		mA
		Sink ($V_o = V_{CC}^+$)		30		
GBP	Gain Bandwidth Product					MHz
	($A_{VCL} = 100$, $R_L = 10k\Omega$, $C_L = 100pF$, f = 100kHz)			0.7		
SR	Slew Rate ($A_{VCL} = 1$, $R_L = 10k\Omega$, $C_L = 100pF$, $V_i = 1.3V$ to 1.7V)			0.5		V/µs
Øm	Phase Margin			30		Degrees
e_n	Equivalent Input Noise Voltage ($R_s = 100\Omega$, f = 1kHz)			40		$\frac{nV}{\sqrt{Hz}}$
V_{O1}/V_{O2}	Channel Separation (f = 1kHz)			120		dB

902-04 TBL

Note 1 : Maximum values including unavoidable inaccuracies of the industial test.

STANDBY MODE

$V_{CC}^+ = 3V$, $V_{CC}^- = 0V$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter	TS3V902I/AI/BI Min.	Typ.	Max.	Unit
$V_{inSBY/ON}$	Pin 1 Threshold Voltage for STANDBY ON		1.2		V
$V_{inSBY/OFF}$	Pin 1 Threshold Voltage for STANDBY OFF		1.5		V
$I_{CC\ SBY}$	Total Consumption in Standby Position (STANDBY ON)		0.5		µA

902-06 TBL

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = 5V$, $V_{CC}^- = 0V$, R_L,C_L connected to $V_{CC}/2$, Standby OFF, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter		TS3V902I/AI/BI			Unit
			Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($V_{ic} = V_o = V_{CC}/2$)	TS3V902			12	mV
		TS3V902A			5	
		TS3V902B			1.5	
	$T_{min} \le T_{amb} \le T_{max}$	TS3V902			12	
		TS3V902A			7	
		TS3V902B			3	
DV_{io}	Input Offset Voltage Drift			2		µV/°C
I_{io}	Input Offset Current - (note 1)			1	100	pA
	$T_{min} \le T_{amb} \le T_{max}$				200	
I_{ib}	Input Bias Current - (note 1)			1	150	pA
	$T_{min} \le T_{amb} \le T_{max}$.				300	
I_{CC}	Supply Current (per amplifier, $A_{VCL} = 1$, no load)			230	350	µA
	$T_{min} \le T_{amb} \le T_{max}$.				450	
CMR	Common Mode Rejection Ratio					dB
	V_{ic} = 1.5 to 3.5V, V_o = 2.5V			85		
SVR	Supply Voltage Rejection Ratio (V_{CC}^+ = 3 to 5V, $V_O = V_{CC}/2$)			80		dB
A_{vd}	Large Signal Voltage Gain (R_L = 10kΩ, V_O = 1.5V to 3.5V)		7	30		V/mV
	$T_{min} \le T_{amb} \le T_{max}$		7			
V_{OH}	High Level Output Voltage (V_{id} = 1V)	R_L = 100kΩ	4.95			V
		R_L = 10kΩ	4.85	4.9		
		R_L = 600Ω	4.2	4.55		
		R_L = 100Ω		3.7		
	$T_{min} \le T_{amb} \le T_{max}$.	R_L = 10kΩ	4.8			
		R_L = 600Ω	4.1			
V_{OL}	Low Level Output Voltage (V_{id} = -1V)	R_L = 100kΩ			50	mV
		R_L = 10kΩ		50	100	
		R_L = 600Ω		450	680	
		R_L = 100Ω		1400		
	$T_{min} \le T_{amb} \le T_{max}$.	R_L = 10kΩ			150	
		R_L = 600Ω			900	
I_o	Output Short Circuit Current (V_{id} = ±1V)	Source ($V_o = V_{CC}^-$)		50		mA
		Sink ($V_o = V_{CC}^+$)		50		
GBP	Gain Bandwidth Product					MHz
	(A_{VCL} = 100, R_L = 10kΩ, C_L = 100pF, f = 100kHz)			0.8		
SR	Slew Rate (A_{VCL} = 1, R_L = 10kΩ, C_L = 100pF, V_i =1V to 4V)			0.8		V/µs
Øm	Phase Margin			30		Degrees

902-05 TBL

Note 1 : Maximum values including unavoidable inaccuracies of the industial test.

STANDBY MODE

$V_{CC}^+ = 5V$, $V_{CC}^- = 0V$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter	TS3V902I/AI/BI			Unit
		Min.	Typ.	Max.	
$V_{inSBY/ON}$	Pin 1 Threshold Voltage for STANDBY ON		5.2		V
$V_{inSBY/OFF}$	Pin 1 Threshold Voltage for STANDBY OFF		5.5		V
$I_{CC\ SBY}$	Total Consumption in Standby Position (STANDBY ON)		0.5		µA

902-07 TBL

TYPICAL CHARACTERISTICS

Figure 1a : Supply Current (each amplifier) versus Supply Voltage

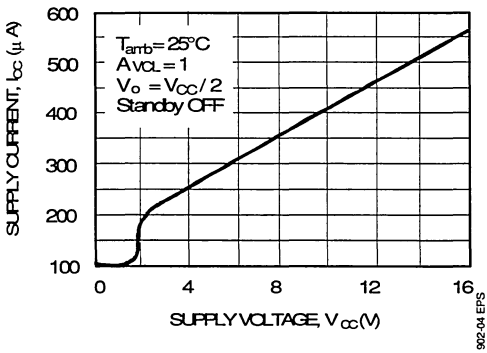


Figure 1b : Supply Current (each amplifier) versus Supply Voltage (in STANDBY)

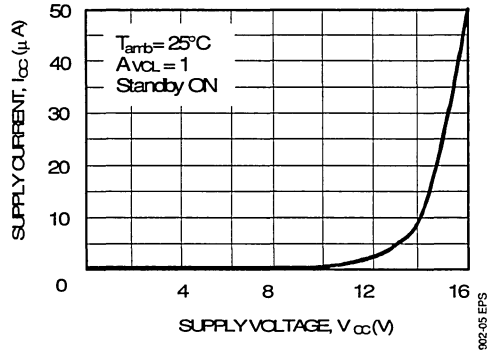


Figure 2 : Input Bias Current versus Temperature

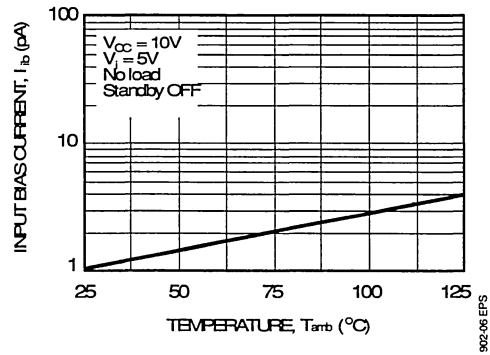


Figure 3a : High Level Output Voltage versus High Level Output Current

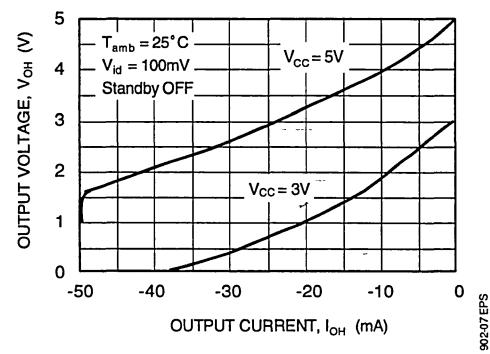


Figure 3b : High Level Output Voltage versus High Level Output Current

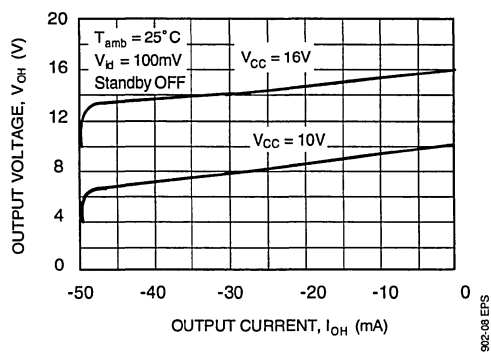


Figure 4a : Low Level Output Voltage versus Low Level Output Current

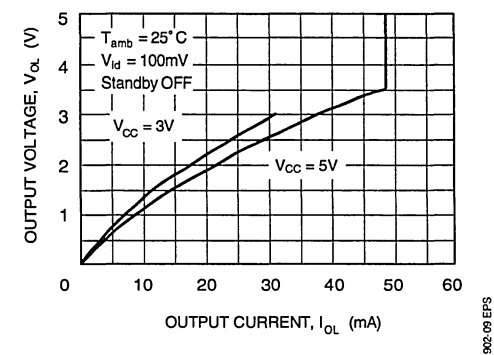


Figure 4b : Low Level Output Voltage versus Low Level Output Current

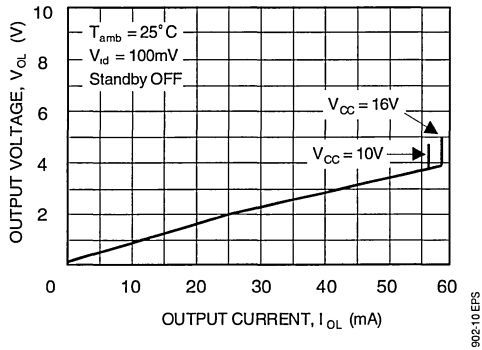


Figure 5a : Open Loop Frequency Response and Phase Shift

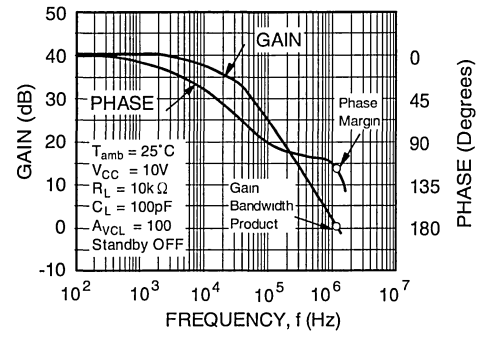


Figure 5b : Open Loop Frequency Response and Phase Shift

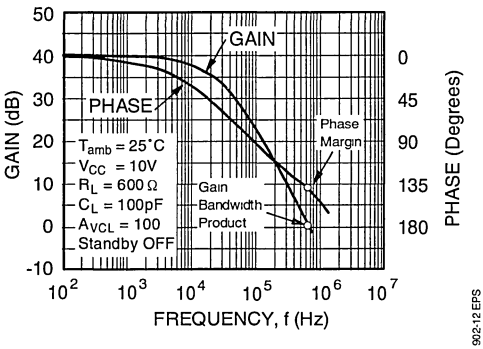


Figure 6a : Gain Bandwidth Product versus Supply Voltage

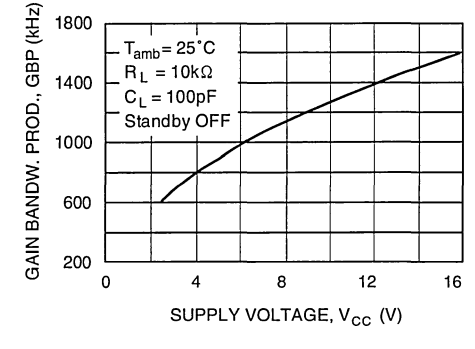


Figure 6b : Gain bandwidth Product versus Supply Voltage

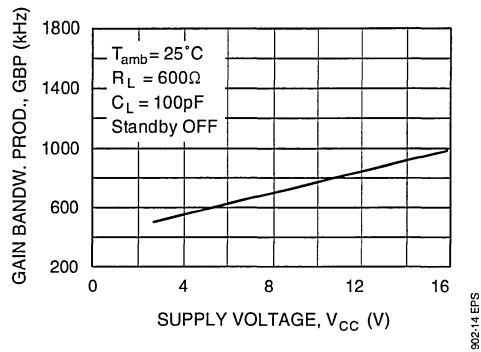


Figure 7a : Phase Margin versus Supply Voltage

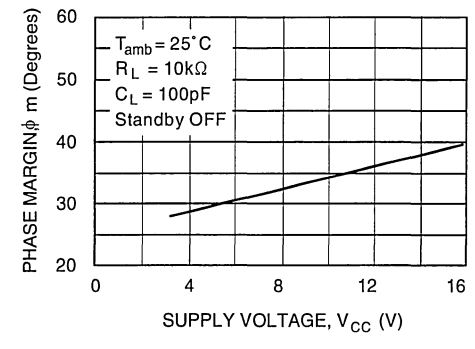


Figure 7b : Phase Margin versus Supply Voltage

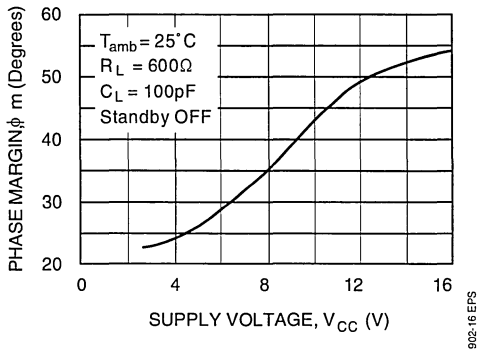
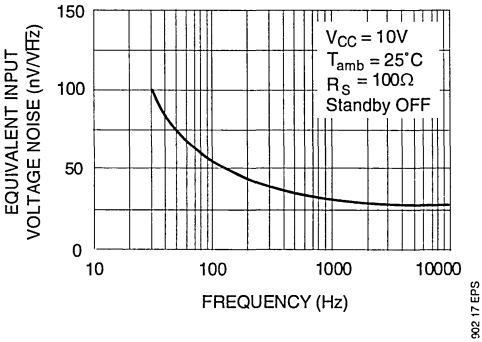


Figure 8 : Input Voltage Noise versus Frequency



STANDBY APPLICATION

The two operators of the TS3V902 are **both** put on **STANDBY.**

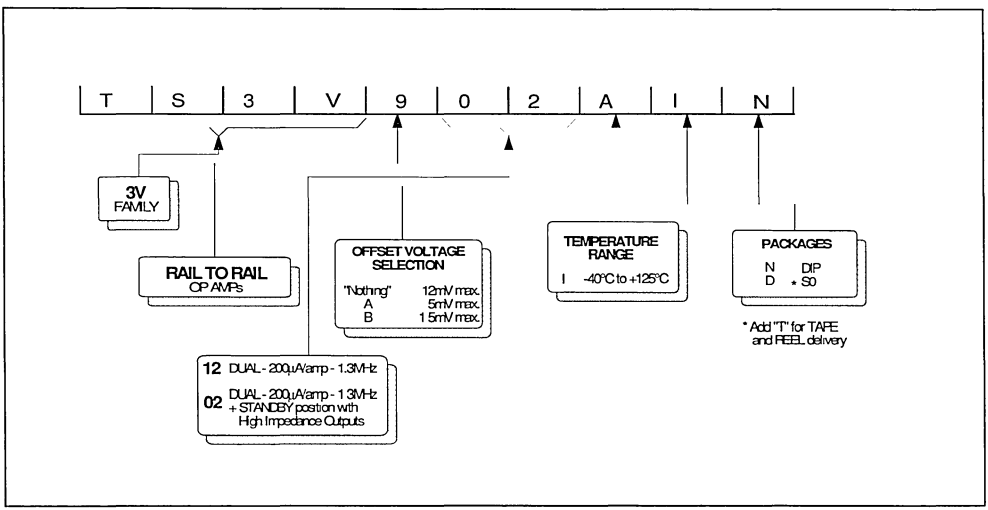
In this configuration (standby ON) :

- The **total consumption** of the circuit is considerably **reduced** down to **0.5µA** (V_{CC} = 3V). This standby consumption versus V_{CC} curve is given figure 1b.
- The **both outputs** are in **high impedance** state. No output current can then be sourced or sinked by the device.

The standby pin 1 should never stay unconnected.

- The **"standby OFF"** state, is reached when the pin 1 voltage is **higher than $V_{in\ SBY/OFF}$.**
- The **"standby ON"** state is assured by a pin 1 voltage **lower than $V_{in\ SBY/ON}$.** (see electrical characteristics)

ORDERING INFORMATION

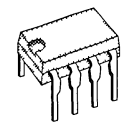


SGS-THOMSON MICROELECTRONICS

TS3V912

3V INPUT/OUTPUT **RAIL TO RAIL** DUAL OPERATIONAL AMPLIFIER

- DEDICATED TO **3.3V** OR **BATTERY SUPPLY** (specified at 3V and 5V)
- RAIL TO RAIL INPUT AND OUTPUT VOLTAGE RANGES
- SINGLE SUPPLY OPERATION FROM **2.7V TO 16V**
- EXTREMELY LOW INPUT BIAS CURRENT : **1pA** TYP
- LOW INPUT OFFSET VOLTAGE : **5mV max.**
- SPECIFIED FOR **600Ω** AND **100Ω** LOADS
- LOW SUPPLY CURRENT : 200µA/Ampli



N
DIP8
(Plastic Package)

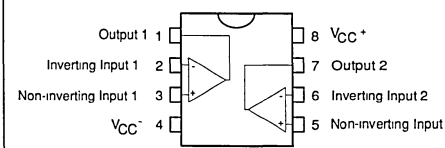
D
SO8
(Plastic Micropackage)

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS3V912I/AI	-40, +125°C	•	•

912-01 TBL

PIN CONNECTIONS (top view)



912-01 EPS

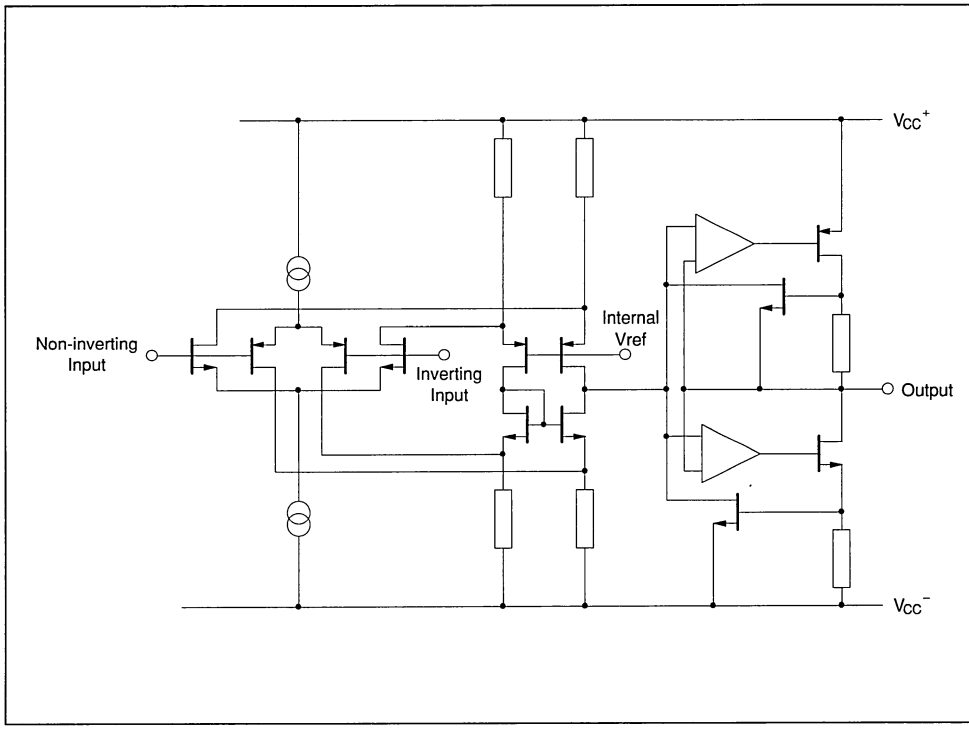
DESCRIPTION

The TS3V912 is a RAIL TO RAIL dual CMOS operational amplifier designed to operate with a single 3V supply voltage.
The input voltage range V_{icm} includes the two supply rails V_{CC}^+ and V_{CC}^-.
The output reaches :

- V_{CC}^- +50mV V_{CC}^+ -50mV with R_L = 10kΩ
- V_{CC}^- +350mV V_{CC}^+ -350mV with R_L = 600Ω

This product offers a broad supply voltage operating range from 2.7V to 16V and a supply current of only 200µA/amp. (V_{CC} = 3V).

SCHEMATIC DIAGRAM (1/2 TS3V912)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage - (note 1)	18	V
V_{id}	Differential Input Voltage - (note 2)	±18	V
V_i	Input Voltage - (note 3)	-0.3 to 18	V
I_{in}	Current on Inputs	±50	mA
I_o	Current on Outputs	±130	mA
T_{oper}	Operating Free Air Temperature Range TS3V912I/AI	-40 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

91202 TBL

Notes : 1. All voltage values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of input and output voltages must never exceed V_{CC}^+ +0.3V.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2.7 to 16	V
V_{icm}	Common Mode Input Voltage Range	V_{CC}^- -0.2 to V_{CC}^++0.2	V

91203 TBL

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = 3V$, $V_{CC}^- = 0V$, R_L,C_L connected to $V_{CC}/2$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter		TS3V912I/AI			Unit
			Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($V_{ic} = V_o = V_{CC}/2$)	TS3V912			12	mV
		TS3V912A			5	
	$T_{min} \le T_{amb} \le T_{max}$.	TS3V912			12	
		TS3V912A			7	
DV_{io}	Input Offset Voltage Drift			2		µV/°C
I_{io}	Input Offset Current - (note 1)			1	100	pA
	$T_{min} \le T_{amb} \le T_{max}$.				200	
I_{ib}	Input Bias Current - (note 1)			1	150	pA
	$T_{min} \le T_{amb} \le T_{max}$				300	
I_{CC}	Supply Current (per amplifier, $A_{VCL} = 1$, no load)			200	300	µA
	$T_{min} \le T_{amb} \le T_{max}$				400	
CMR	Common Mode Rejection Ratio					dB
	V_{ic} = 0 to 3V, V_o = 1.5V			70		
SVR	Supply Voltage Rejection Ratio (V_{CC}^+ = 2.7 to 3.3V, $V_O = V_{CC}/2$)			70		dB
A_{vd}	Large Signal Voltage Gain (R_L = 10kΩ, V_O = 1.2V to 1.8V)		3	10		V/mV
	$T_{min} \le T_{amb} \le T_{max}$		3			
V_{OH}	High Level Output Voltage (V_{id} = 1V)	R_L = 100kΩ	2.95			V
		R_L = 10kΩ	2.9	2.96		
		R_L = 600Ω	2.2	2.6		
		R_L = 100Ω		2		
	$T_{min} \le T_{amb} \le T_{max}$	R_L = 10kΩ	2.8			
		R_L = 600Ω	2.1			
V_{OL}	Low Level Output Voltage (V_{id} = -1V)	R_L = 100kΩ			50	mV
		R_L = 10kΩ		50	100	
		R_L = 600Ω		350	600	
		R_L = 100Ω		900		
	$T_{min} \le T_{amb} \le T_{max}$	R_L = 10kΩ			150	
		R_L = 600Ω			900	
I_o	Output Short Circuit Current (V_{id} = ±1V)	Source ($V_o = V_{CC}^-$)		30		mA
		Sink ($V_o = V_{CC}^+$)		30		
GBP	Gain Bandwidth Product					MHz
	(A_{VCL} = 100, R_L = 10kΩ, C_L = 100pF, f = 100kHz)			0.7		
SR	Slew Rate (A_{VCL} = 1, R_L = 10kΩ, C_L = 100pF, V_i =1.3V to 1.7V)			0.5		V/µs
Øm	Phase Margin			30		Degrees
e_n	Equivalent Input Noise Voltage (R_s = 100Ω, f = 1kHz)			40		$\frac{nV}{\sqrt{Hz}}$
V_{O1}/V_{O2}	Channel Separation (f = 1kHz)			120		dB

912-04 TBL

Note 1 : Maximum values including unavoidable inaccuracies of the industial test

ELECTRICAL CHARACTERISTICS

V_{CC}^+ = 5V, V_{CC}^- = 0V, R_L,C_L connected to $V_{CC}/2$, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter		TS3V912I/AI			Unit
			Min.	Typ.	Max.	
V_{io}	Input Offset Voltage (V_{ic} = V_o = $V_{CC}/2$)	TS3V912			12	mV
		TS3V912A			5	
	$T_{min} \le T_{amb} \le T_{max}$	TS3V912			12	
		TS3V912A			7	
DV_{io}	Input Offset Voltage Drift			2		µV/°C
I_{io}	Input Offset Current - (note 1)			1	100	pA
	$T_{min} \le T_{amb} \le T_{max}$				200	
I_{ib}	Input Bias Current - (note 1)			1	150	pA
	$T_{min.} \le T_{amb} \le T_{max}$				300	
I_{CC}	Supply Current (per amplifier, A_{VCL} = 1, no load)			230	350	µA
	$T_{min} \le T_{amb} \le T_{max}$				450	
CMR	Common Mode Rejection Ratio					dB
	V_{ic} = 1.5 to 3.5V, V_o = 2.5V			85		
SVR	Supply Voltage Rejection Ratio (V_{CC}^+ = 3 to 5V, V_O = V_{CC} /2)			80		dB
A_{vd}	Large Signal Voltage Gain (R_L = 10kΩ, V_O = 1.5V to 3.5V)		7	30		V/mV
	$T_{min} \le T_{amb} \le T_{max}$		7			
V_{OH}	High Level Output Voltage (V_{id} = 1V)	R_L = 100kΩ	4.95			V
		R_L = 10kΩ	4.85	4.9		
		R_L = 600Ω	4.2	4.55		
		R_L = 100Ω		3.7		
	$T_{min} \le T_{amb} \le T_{max}$	R_L = 10kΩ	4.8			
		R_L = 600Ω	4.1			
V_{OL}	Low Level Output Voltage (V_{id} = -1V)	R_L = 100kΩ			50	mV
		R_L = 10kΩ		50	100	
		R_L = 600Ω		450	680	
		R_L = 100Ω		1400		
	$T_{min} \le T_{amb} \le T_{max}$	R_L = 10kΩ			150	
		R_L = 600Ω			900	
I_o	Output Short Circuit Current (V_{id} = ±1V)	Source (V_o = V_{CC}^-)		50		mA
		Sink (V_o = V_{CC}^+)		50		
GBP	Gain Bandwidth Product					MHz
	(A_{VCL} = 100, R_L = 10kΩ, C_L = 100pF, f = 100kHz)			0.8		
SR	Slew Rate (A_{VCL} = 1, R_L = 10kΩ, C_L = 100pF, V_i =1V to 4V)			0.8		V/µs
Øm	Phase Margin			30		Degrees

912-05 TBL

Note 1 : Maximum values including unavoidable inaccuracies of the industrial test.

TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each amplifier) versus Supply Voltage

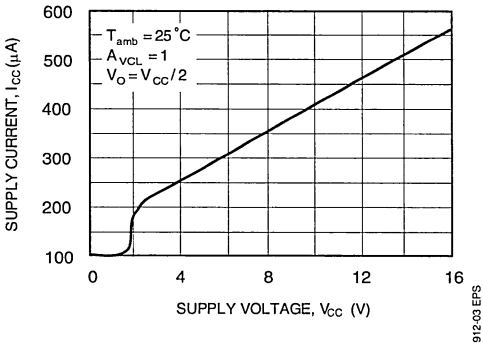


Figure 2 : Input Bias Current versus Temperature

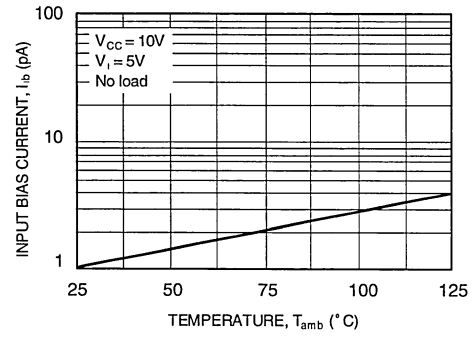


Figure 3a : High Level Output Voltage versus High Level Output Current

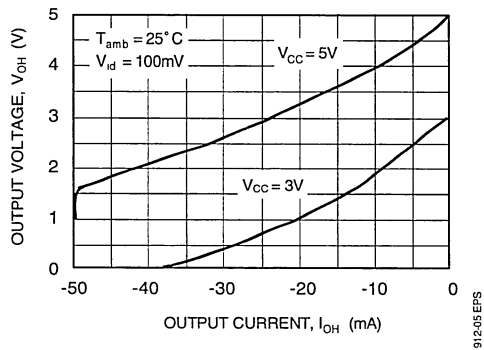


Figure 3b : High Level Output Voltage versus High Level Output Current

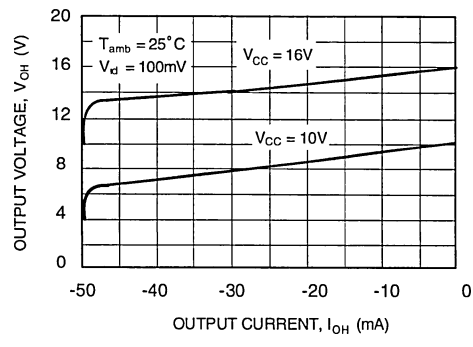


Figure 4a : Low Level Output Voltage versus Low Level Output Current

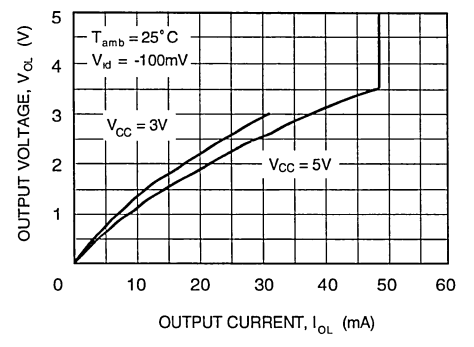


Figure 4b : Low Level Output Voltage versus Low Level Output Current

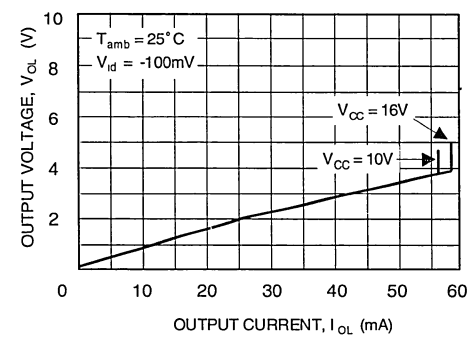


Figure 5a : Open Loop Frequency Response and Phase Shift

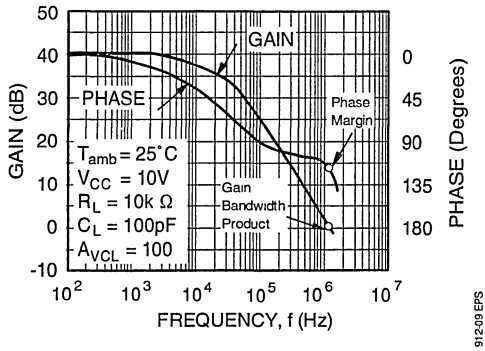


Figure 5b : Open Loop Frequency Response and Phase Shift

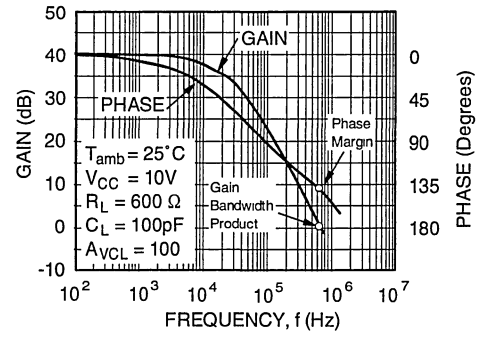


Figure 6a : Gain Bandwidth Product versus Supply Voltage

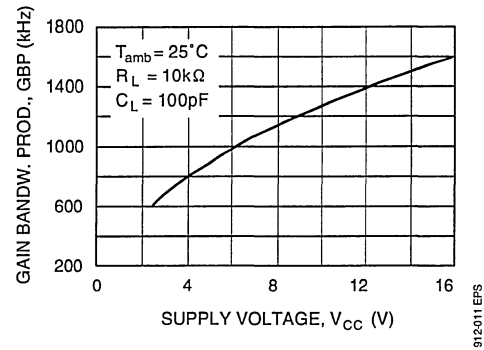


Figure 6b : Gain bandwidth Product versus Supply Voltage

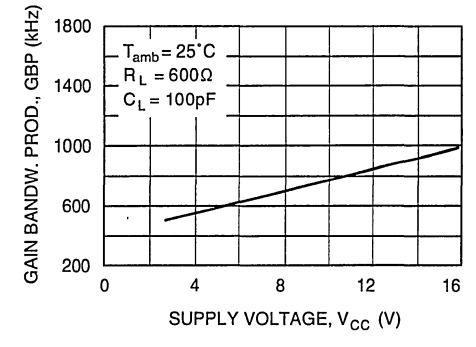


Figure 7a : Phase Margin versus Supply Voltage

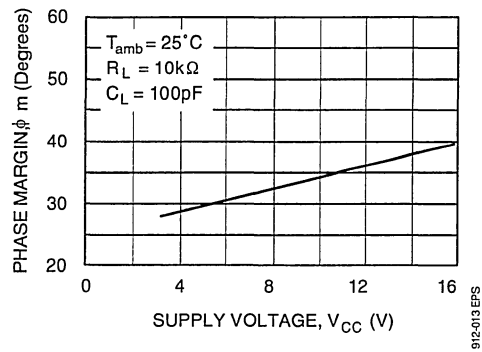


Figure 7b : Phase Margin versus Supply Voltage

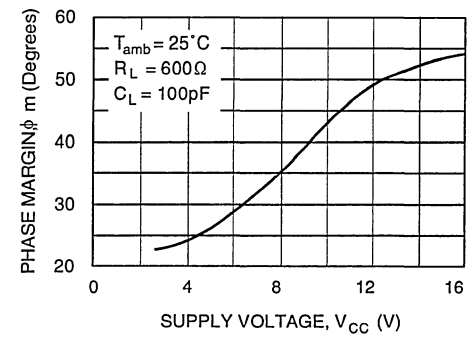
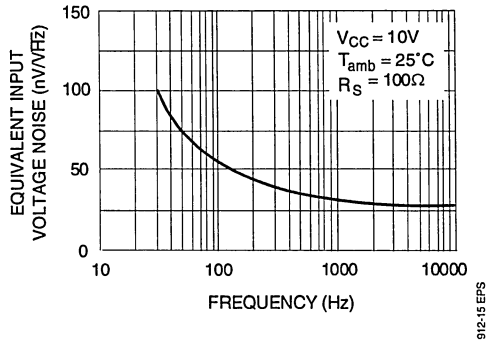
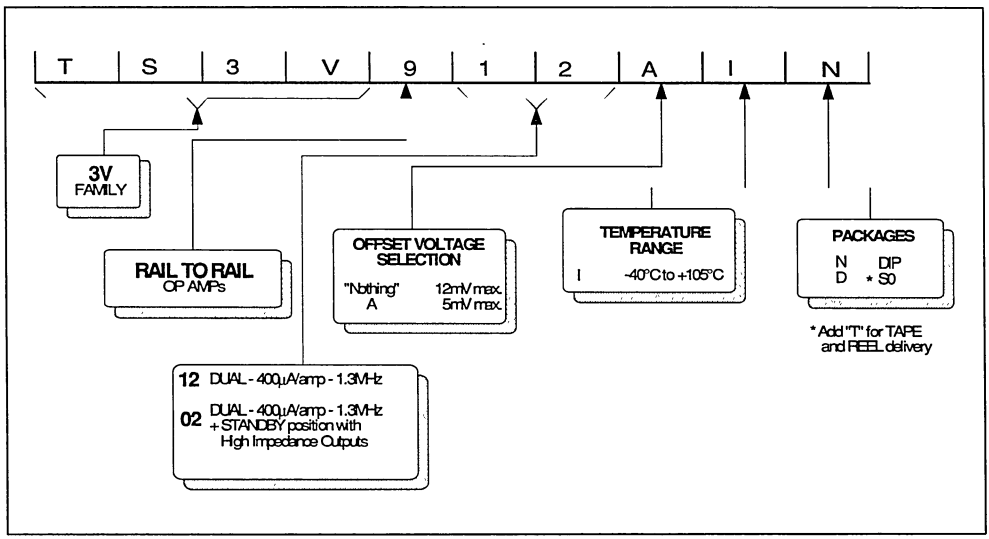


Figure 8 : Input Voltage Noise versus Frequency



ORDERING INFORMATION

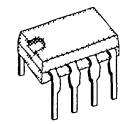


SGS-THOMSON MICROELECTRONICS

TS3V3702

3V MICROPOWER DUAL VOLTAGE COMPARATORS

- DEDICATED TO **3.3V** OR **BATTERY SUPPLY** (specified at 3V and 5V)
- PUSH-PULL CMOS OUTPUT (NO EXTERNAL PULL-UP RESISTOR REQUIRED)
- EXTREMELY LOW SUPPLY CURRENT : **7µA typ / comparator**
- WIDE SINGLE SUPPLY RANGE **2.7V TO 16V**
- EXTREMELY LOW INPUT CURRENTS : **1pA TYP**
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GND
- FAST RESPONSE TIME : 2µs typ for 5mV overdrive
- PIN-TO-PIN AND FUNCTIONALLY COMPATIBLE WITH BIPOLAR LM393



N
DIP8
(Plastic Package)

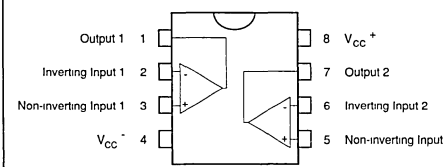
D
SO8
(Plastic Micropackage)

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS3V3702I	-40°C, +125°C	•	•

3702-01 TBL

PIN CONNECTIONS (top view)



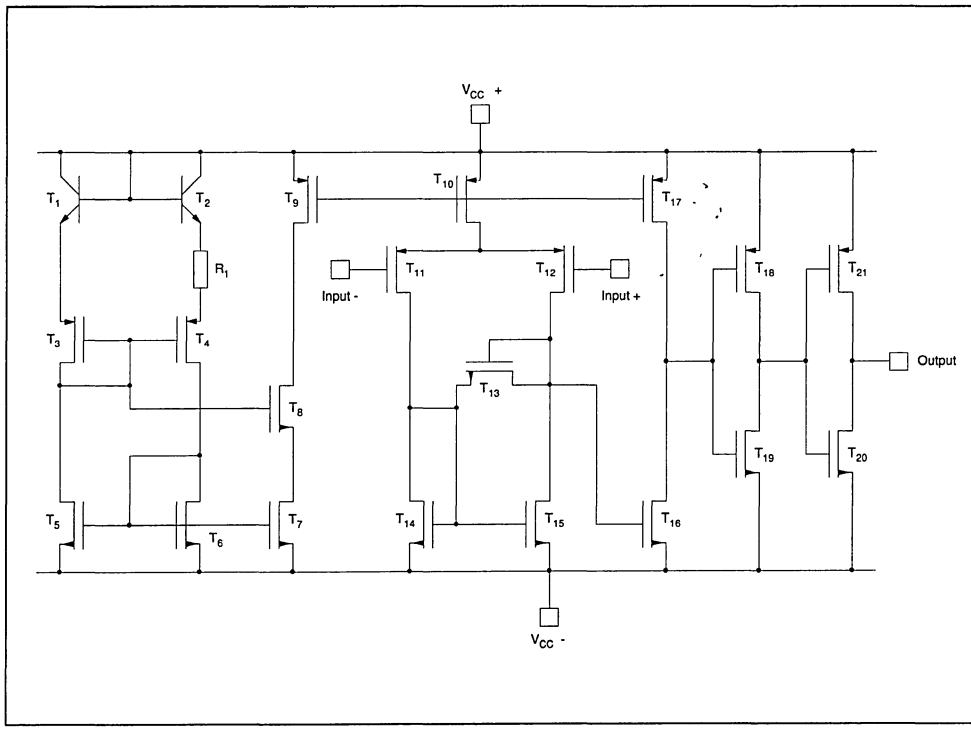
3702-01 EPS

DESCRIPTION

The TS3V3702 is a micropower dual CMOS voltage comparator with extremely low consumption of 7µA typ / comparator (20 times less than bipolar LM393). The push-pull CMOS output stage allows power and space saving by eliminating the external pull-up resistor required by usual open-collector output comparators.

Thus response times remain similar to the LM393.

SCHEMATIC DIAGRAM (for 1/2 TS3V3702)



MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage - (note 1)	18	V
V_{id}	Differential Input Voltage - (note 2)	±18	V
V_i	Input Voltage - (note 3)	18	V
V_O	Output Voltage	18	V
I_O	Output Current	20	mA
T_{oper}	Operating Free-Air Temperature Range TS3V3702I	 -40 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

3702-02 TBL

Notes : 1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage.
4. Short circuit from outputs to V_{CC}^+ can cause excessive heating and eventual destruction.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	2.7 to 16	V
V_{icm}	Common Mode Input Voltage Range	0 to V_{CC}^+ -1.5	V

3702-03 TBL

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = 3V$, $V_{CC}^- = 0V$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage - (note 1) $V_{ic} = 1.5V$ $T_{min} \leq T_{amb} \leq T_{max}$.			5 6.5	mV
I_{io}	Input Offset Current - (note 2) $V_{ic} = 1.5$ V $T_{min} \leq T_{amb} \leq T_{max}$.		1	 300	pA
I_{ib}	Input Bias Current - (note 2) $V_{ic} = 1.5$ V $T_{min} \leq T_{amb} \leq T_{max}$.		1	 600	pA
V_{icm}	Input Common Mode Voltage Range $T_{min} \leq T_{amb} \leq T_{max}$.	0 to V_{CC}^+-1.2 0 to V_{CC}^+ -1.5			V
CMR	Common-mode Rejection Ratio $V_{ic} = V_{icm\ min}$.		80		dB
SVR	Supply Voltage Rejection Ratio $V_{CC}^+ = 3V$ to 5V		75		dB
V_{OH}	High Level Output Voltage $V_{id} = 1V$, $I_{OH} = -4mA$ $T_{min} \leq T_{amb} \leq T_{max}$.	 2 1.8	 2.4		V
V_{OL}	Low Level Output Voltage $V_{id} = -1V$, $I_{OL} = 4mA$ $T_{min} \leq T_{amb} \leq T_{max}$.		 300	 400 450	mV
I_{CC}	Supply Current (each comparator) No load - Outputs low $T_{min} \leq T_{amb} \leq T_{max}$.		7	 20 25	µA
t_{PLH}	Response Time Low to High $V_{ic} = 0V$, f = 10kHz, $C_L = 50pF$, Overdrive = 5mV TTL Input		 1 0.7		µs
t_{PHL}	Response Time High to Low $V_{ic} = 0V$, f = 10kHz, $C_L = 50pF$, Overdrive = 5mV TTL Input		 1.5 0.15		µs

3702 04 TBL

Note : 1. The specified offset voltage is the maximun value required to drive the output up to 4.5V or down to 0.3V.
2. Maximum values including unavoidable inaccuracies of the industrial test.

ELECTRICAL CHARACTERISTICS

V_{CC}^+ = 5V, V_{CC}^- = 0V, T_{amb} = 25°C (unless otherwise specified)

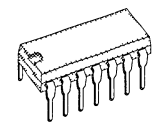
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage - (note 1) V_{ic} = 2.5V $T_{min} \leq T_{amb} \leq T_{max}$.		1.2	5 6.5	mV
I_{io}	Input Offset Current - (note 2) V_{ic} = 2.5 V $T_{min} \leq T_{amb} \leq T_{max}$.		1	 300	pA
I_{ib}	Input Bias Current - (note 2) V_{ic} = 2.5 V $T_{min} \leq T_{amb} \leq T_{max}$.		1	 600	pA
V_{icm}	Input Common Mode Voltage Range $T_{min} \leq T_{amb} \leq T_{max}$.	0 to V_{CC}^+-1.2 0 to V_{CC}^+ -1.5			V
CMR	Common-mode Rejection Ratio $V_{ic} = V_{icm\ min}$.		80		dB
SVR	Supply Voltage Rejection Ratio V_{CC}^+ = +5V to +10V		90		dB
V_{OH}	High Level Output Voltage V_{id} = 1V, I_{OH} = -4mA $T_{min} \leq T_{amb} \leq T_{max}$.	 4.5 4.3	4.7		V
V_{OL}	Low Level Output Voltage V_{id} = -1V, I_{OL} = 4mA $T_{min} \leq T_{amb} \leq T_{max}$.		200	300 375	mV
I_{CC}	Supply Current (per comparator) No load - Outputs low $T_{min} \leq T_{amb} \leq T_{max}$.		9	20 25	µA
t_{PLH}	Response Time Low to High V_{ic} = 0V, f = 10kHz, C_L = 50pF, Overdrive = 5mV TTL Input		1 0.7		µs
t_{PHL}	Response Time High to Low V_{ic} = 0V, f = 10kHz, C_L = 50pF, Overdrive = 5mV TTL Input		1.5 0.15		µs

3702-05.TBL

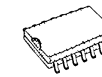
Note : 1. The specified offset voltage is the maximun value required to drive the output up to 4.5V or down to 0 3V.
2. Maximum values including unavoidable inaccuracies of the industrial test.

3V MICROPOWER QUAD VOLTAGE COMPARATORS

- DEDICATED TO **3.3V** OR **BATTERY SUPPLY** (specified at 3V and 5V)
- PUSH-PULL CMOS OUTPUT (NO EXTERNAL PULL-UP RESISTOR REQUIRED)
- EXTREMELY LOW SUPPLY CURRENT : 7µA typ / comparator
- WIDE SINGLE SUPPLY RANGE **2.7V to 16V**
- EXTREMELY LOW INPUT CURRENTS : **1pA TYP**
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GND
- FAST RESPONSE TIME : 2µs typ for 5mV overdrive
- PIN-TO-PIN AND FUNCTIONALLY COMPATIBLE WITH BIPOLAR LM339



N
DIP14
(Plastic Package)



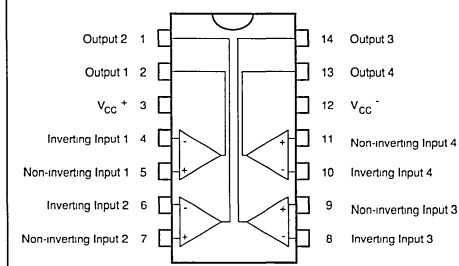
D
SO14
(Plastic Micropackage)

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS3V3704I	-40°C, +125°C	•	•

374 01 TBL

PIN CONNECTIONS (top view)



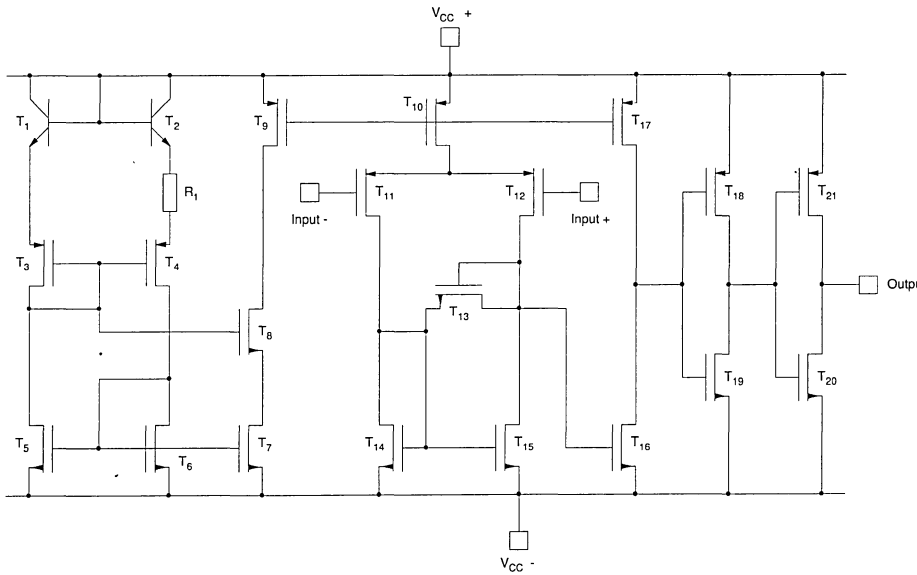
3704 01 EPS

DESCRIPTION

The TS3V3704 is a micropower quad CMOS voltage comparator with extremely low consumption of 7µA typ / comparator (20 times less than bipolar LM339). The push-pull CMOS output stage allows power and space saving by eliminating the external pull-up resistor required by usual open-collector output comparators.

Thus response times remain similar to the LM339.

SCHEMATIC DIAGRAM (for 1/4 TS3V3704)



3704-02 EPS

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage - (note 1)	18	V
V_{id}	Differential Input Voltage - (note 2)	±18	V
V_i	Input Voltage - (note 3)	18	V
V_O	Output Voltage	18	V
I_O	Output Current	20	mA
T_{oper}	Operating Free-Air Temperature Range TS3V3704I	-40 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

3704-02 TBL

Notes : 1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage.
4. Short circuit from outputs to V_{CC}^+ can cause excessive heating and eventual destruction.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	2.7 to 16	V
V_{icm}	Common Mode Input Voltage Range	0 to V_{CC}^+ -1.5	V

3704-03 TBL

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = 3V$, $V_{CC}^- = 0V$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage - (note 1) $V_{ic} = 1.5V$ $T_{min} \leq T_{amb} \leq T_{max}$.			5 6.5	mV
I_{io}	Input Offset Current - (note 2) $V_{ic} = 1.5$ V $T_{min} \leq T_{amb} \leq T_{max}$.		1	 300	pA
I_{ib}	Input Bias Current - (note 2) $V_{ic} = 1.5$ V $T_{min} \leq T_{amb} \leq T_{max}$.		1	 600	pA
V_{icm}	Input Common Mode Voltage Range $T_{min} \leq T_{amb} \leq T_{max}$.	0 to V_{CC}^+-1.2 0 to V_{CC}^+ -1.5			V
CMR	Common-mode Rejection Ratio $V_{ic} = V_{icm\ min}$.		80		dB
SVR	Supply Voltage Rejection Ratio $V_{CC}^+ = 3V$ to $5V$		75		dB
V_{OH}	High Level Output Voltage $V_{id} = 1V$, $I_{OH} = -4mA$ $T_{min} \leq T_{amb} \leq T_{max}$.	2 1.8	2.4		V
V_{OL}	Low Level Output Voltage $V_{id} = -1V$, $I_{OL} = 4mA$ $T_{min} \leq T_{amb} \leq T_{max}$.		300	400 450	mV
I_{CC}	Supply Current (each comparator) No load - Outputs low $T_{min} \leq T_{amb} \leq T_{max}$.		7	20 25	µA
t_{PLH}	Response Time Low to High $V_{ic} = 0V$, f = 10kHz, $C_L = 50pF$, Overdrive = 5mV TTL Input		1 0.7		µs
t_{PHL}	Response Time High to Low $V_{ic} = 0V$, f = 10kHz, $C_L = 50pF$, Overdrive = 5mV TTL Input		1.5 0.15		µs

374-04 TBL

Note : 1. The specified offset voltage is the maximun value required to drive the output up to 4.5V or down to 0.3V.
2. Maximum values including unavoidable inaccuracies of the industrial test.

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = 5V$, $V_{CC}^- = 0V$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage - (note 1) $V_{ic} = 2.5V$ $T_{min} \leq T_{amb} \leq T_{max}$.		1.2	5 6.5	mV
I_{io}	Input Offset Current - (note 2) $V_{ic} = 2.5\ V$ $T_{min} \leq T_{amb} \leq T_{max}$.		1	 300	pA
I_{ib}	Input Bias Current - (note 2) $V_{ic} = 2.5\ V$ $T_{min} \leq T_{amb} \leq T_{max}$.		1	 600	pA
V_{icm}	Input Common Mode Voltage Range $T_{min} \leq T_{amb} \leq T_{max}$.	0 to V_{CC}^+-1.2 0 to V_{CC}^+ -1.5			V
CMR	Common-mode Rejection Ratio $V_{ic} = V_{icm\ min}$.		80		dB
SVR	Supply Voltage Rejection Ratio $V_{CC}^+ = +5V$ to $+10V$		90		dB
V_{OH}	High Level Output Voltage $V_{id} = 1V$, $I_{OH} = -4mA$ $T_{min} \leq T_{amb} \leq T_{max}$.	4.5 4.3	4.7		V
V_{OL}	Low Level Output Voltage $V_{id} = -1V$, $I_{OL} = 4mA$ $T_{min} \leq T_{amb} \leq T_{max}$.		200	300 375	mV
I_{CC}	Supply Current (per comparator) No load - Outputs low $T_{min} \leq T_{amb} \leq T_{max}$.		9	20 25	µA
t_{PLH}	Response Time Low to High $V_{ic} = 0V$, f = 10kHz, $C_L = 50pF$, Overdrive = 5mV TTL Input		1 0.7		µs
t_{PHL}	Response Time High to Low $V_{ic} = 0V$, f = 10kHz, $C_L = 50pF$, Overdrive = 5mV TTL Input		1.5 0.15		µs

374-05.TBL

Note : 1. The specified offset voltage is the maximun value required to drive the output up to 4.5V or down to 0.3V.
2. Maximum values including unavoidable inaccuracies of the industrial test.

DC-DC CONVERTERS DATASHEETS

SGS-THOMSON MICROELECTRONICS

GS1T70-D540

ISDN DC-DC CONVERTER

Type	V_i	V_o	I_o
GS1T70-D540	25 to 115 V	5 V	90 mA
		40 V	10,5 mA

FEATURES

- Wide operating line termination voltage
- Peak input overvoltage withstand: 1kV for 1.2/50µs
- Peak overvoltage withstand on Output 2 (40V): 250V for 10/700µs
- Positive or negative input voltage polarity
- Input and output filtering
- Short-circuit protection on both outputs
- Input power during shortcircuit within specification
- Minimum current drain during stand-by condition: 10µA for Vi<18V
- Input-output isolation voltage: 2000V_{RMS} for 60 seconds
- Output1-output2 isolation voltage: 2000V_{RMS} for 60 seconds
- Mechanical dimensions (L x W x H): 50.8 mm x 50.8 mm x 18 mm (2" x 2" x 0.71")

DESCRIPTION

The GS1T70-D540 converter has been designed for the "U" interface of an ISDN-NTBA (Network Termination Basic Access) system with either 4B3T or 2B1Q standard trasmission.

It meets the requirements of the following specifications:

EN 60950

CCITT I.430

CCITT G.960

CCITT G.961

ETS 300 002

ETS 300 012

ETS 300 047 (ISDN BASIC ACCESS, Safety and Protection)

Two isolated outputs, 5V/90mA and 40V/10.5mA are supplied. The converter offers short-circuit protection (short-circuit on 40V output doesn't affect 5V output and the input power never exceeds the limit of the specification), input either voltage polarity, 80% minimum efficiency at maximum load, input and output filtering to meet very stringent noise requirements.

The input and the output 2 (40V) stages are protected against differential overvoltage up to 1kV (1.2/50µs) and 250V (10/700µs) respectively.

When the input voltage is below 18V, the converter offers a very high input impedance and a maximum quiescent current of 10µA.

These features allow the converter to operate directly connected to the telephone line without any external components.

In addition, the wide operating input voltage range allows it to operate within the whole range of LT (Line Termination) battery voltage and its relevant line resistance.

2000V_{RMS} isolation voltage for 60 second is provided between input to outputs and between output 1 and output 2.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Std. Conditions:

Line Termination voltage: 47 to 71V
87 to 99V

Line Resistance (Rs): 10 to 560 Ω
550 to 1400 Ω

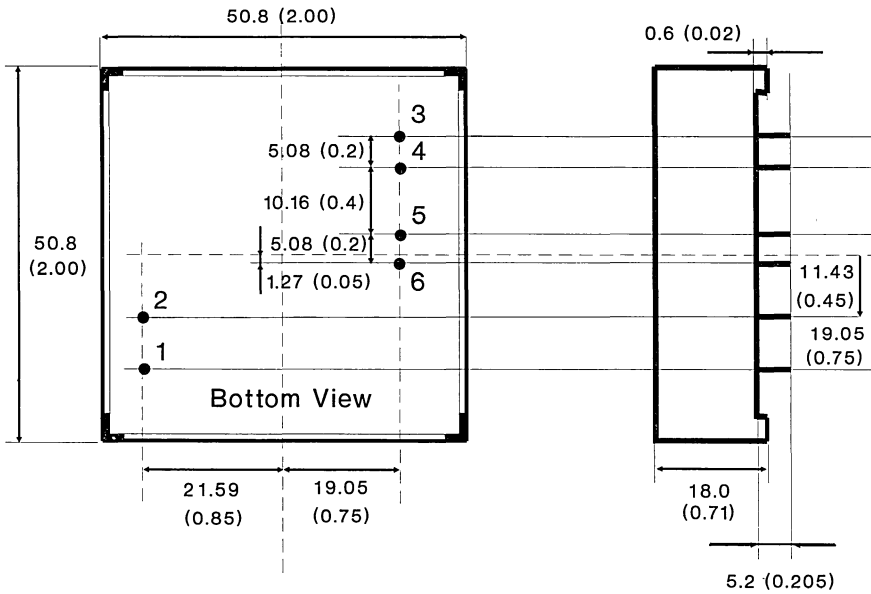
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_i	Input Voltage	Std. Conditions	25		115	V
V_{ipk}	Input Transient Overvoltage	t = 1.2/50µs (pulse)			1	kV
V_{ist}	Start Up Input Voltage	See fig. 2	28		44	V
V_{o1}	Output Voltage 1	Std. Conditions	4.75	5	5.25	V
V_{o2}	Output Voltage 2	Std. Conditions	34	40	42	V
V_{or1}	Output Ripple Voltage 1	Std. Conditions BW = 0 to 20MHz		5	20	mVpp
V_{or2}	Output Ripple Voltage 2	Std. Conditions BW = 0 to 20MHz		10	30	mVpp
eN	Input Noise Voltage	Std. Conditions BW = 0 to 20MHz		10	30	mVpp
I_{o1}	Output Current 1	Std. Conditions I_{o2} = 0 to 10.5 mA V_{o1} = 5V	2		90	mA
I_{o1l}	Output Current 1 Limit Initiation	Std. Conditions V_{o1} = 4.75 to 5.25V	110		130	mA
I_{o2}	Output Current 2	Std. Conditions I_{o1} = 2 to 90 mA V_{o2} = 40V	0		10.5	mA
I_{osc2}	Output 2 Short Circuit Current	Std. Conditions Output Shorted (Indefinite time)	9		14	mA
V_{is}	Isolation Voltage (pulse)	Input to Output 1 Input to Output 2 Output 1 to Output 2	2000			VRMS
Top	Operating Ambient Temperature Range		0		+80	°C
Tstg	Storage Temperature Range		− 40		+85	°C

OUTPUT POWER CHARACTERISTICS

LT (Line Termination Voltage) = **47V to 71V** **Rs** (Line Resistance) = 10 to 560 Ω				**LT** (Line Termination Voltage) = **87V to 99V** **Rs** (Line Resistance) = 550 to 1400 Ω			
Max Input Power (mW)	**NT Status**	**Min Output Power 1 (5V)[mW]**	**Min Output Power 2 (40V)[mW]**	**Max Input Power (mW)**	**NT Status**	**Min Output Power 1 (5V)[mW]**	**Min Output Power 2 (40V)[mW]**
450	Activated	320	0	450	Activated	320	0
950	Activated Emergency	330	410	950	Activated Emergency	330	410
90	Deactivated	25	0	90	Deactived	25	0
180	Deactivated Emergency	25	45	180	Deactivated Emergency	25	45
950	Activated with 40 V Short circuit	330	Short circuit	950	Activated with 40V Short circuit	330	Short circuit

CONNECTION DIAGRAM AND MECHANICAL DATA

Figure 1.



Package V. Dimensions in mm (inches).

PIN DESCRIPTION

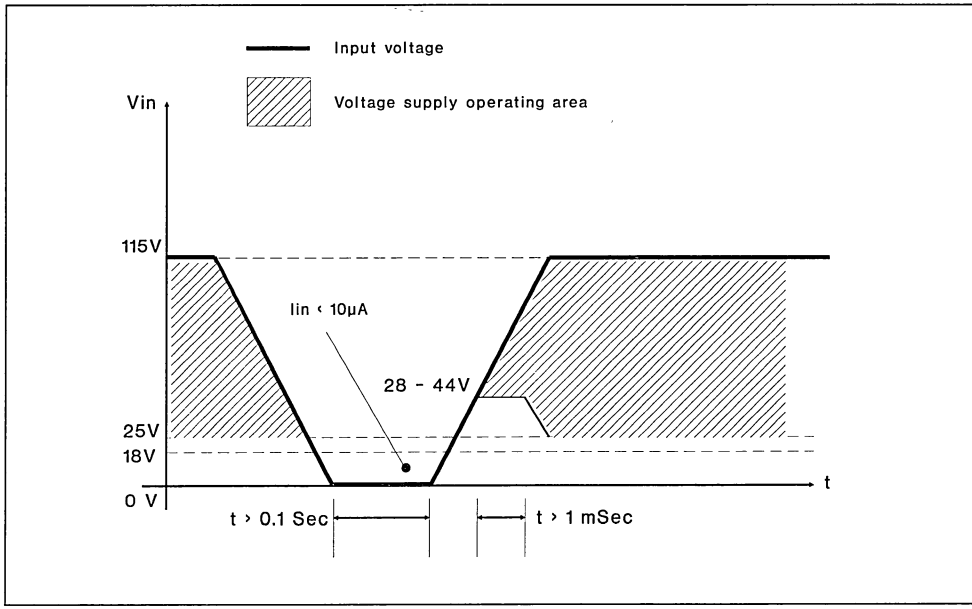
Pin	Description
1	Input (either polarity).
2	Input (either polarity).
3	+5V Output.
4	Return for +5V Output.
5	+40V Output.
6	Return for +40V Output.

VOLTAGE SUPPLY OPERATING AREA

Figure 2 shows the Voltage Supply Operating area during a switching OFF-ON sequence.

The start-up voltage is 44V maximum. When the input voltage is below 18V the maximum quiescent current is lower than 10µA.

Figure 2.



SGS-THOMSON MICROELECTRONICS

GS1T70-D540F

ISDN DC-DC CONVERTER (FRENCH VERSION)

Type	V_i	V_o	I_o
GS1T70-D540F	25 to 115 V	5 V	90 mA
		40 V	10,5 mA

FEATURES

- Wide operating line termination battery voltage
- Peak input overvoltage withstand: 1kV for 1.2/50µs
- Peak overvoltage withstand on Output 2 (40V): 250V for 10/700µs
- Positive or negative input voltage polarity
- Input and output filtering
- Short-circuit protection on both outputs
- Input power during shortcircuit within specification
- Minimum current drain during stand-by condition: 10µA for Vi<18V
- Undervoltage lock out at 10V
- Input-output isolation voltage: 10 kV pulse 1,2/50 µseconds
- Output1-output2 isolation voltage: 2000V_{RMS} for 60 seconds
- Mechanical dimensions (L x W x H): 56 mm x 56 mm x 18 mm (2.2" x 2.2" x 0.71")

DESCRIPTION

The GS1T70-D540F converter has been designed for the "U" interface of an ISDN-NTBA (Network Termination Basic Access) system with either 4B3T or 2B1Q standard trasmission.

It meets the requirements of the following specifications:

EN 60950

CCITT I.430

CCITT G.960

CCITT G.961

ETS 300 002

ETS 300 012

ETS 300 047 (ISDN BASIC ACCESS, Safety and Protection)

Two isolated outputs, 5V/90mA and 40V/10.5mA are supplied. The converter offers short-circuit protection (short-circuit on 40V output doesn't affect 5V output and the input power never exceeds the limit of the specification), input either voltage polarity, 80% minimum efficiency at maximum load, input and output filtering to meet very stringent noise requirements.

The input and the output 2 (40V) stages are protected against differential overvoltage up to 1kV (1.2/50µs) and 250V (10/700µs) respectively.

When the input voltage is below 18V, the converter offers a very high input impedance and a maximum quiescent current of 10µA.

These features allow the converter to operate directly connected to the telephone line without any external components.

In addition, the wide operating input voltage range allows it to operate within the whole range of LT (Line Termination) battery voltage and its relevant line resistance.

2000V_{RMS} isolation voltage for 60 second is provided between input to outputs and between output 1 and output 2.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Std. Conditions:

Line Termination voltage: 90 to 110V
105 to 115V

Line Resistance (Rs): 50 to 1400 Ω
500 to 1900 Ω

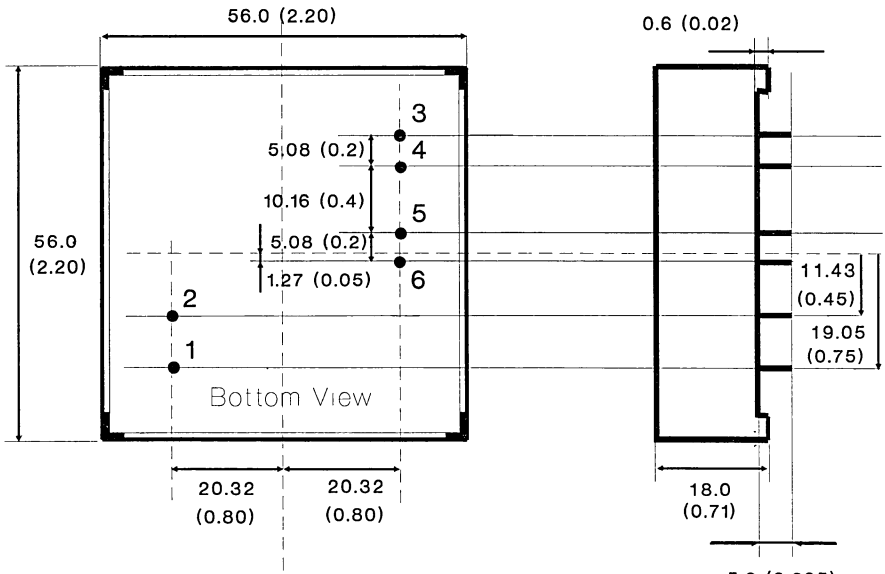
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_i	Input Voltage	Std. Conditions	25		115	V
V_{ipk}	Input Transient Overvoltage	t = 1.2/250µs (pulse)			1	kV
V_{ist}	Start Up Input Voltage	See fig. 2	28		44	V
V_{iuv}	Input Undervoltage Lockout		10			V
V_{o1}	Output Voltage 1	Std. Conditions	4.75	5	5.25	V
V_{o2}	Output Voltage 2	Std. Conditions	34	40	42	V
V_{or1}	Output Ripple Voltage 1	Std. Conditions BW = 0 to 20MHz		5	20	mVpp
V_{or2}	Output Ripple Voltage 2	Std. Conditions BW = 0 to 20MHz		10	30	mVpp
eN	Input Noise Voltage	Std. Conditions BW = 0 to 20MHz		10	30	mVpp
I_{o1}	Output Current 1	Std. Conditions I_{o2} = 0 to 10.5 mA V_{o1} = 5V	2		90	mA
I_{o1l}	Output Current 1 Limit Initiation	Std. Conditions V_{o1} = 4.75 to 5.25V	110		130	mA
I_{o2}	Output Current 2	Std. Conditions I_{o1} = 2 to 90 mA V_{o2} = 40V	0		10.5	mA
I_{osc2}	Output 2 Short Circuit Current	Std. Conditions Output Shorted (Indefinite time)	9		14	mA
V_{is}	Isolation Voltage (pulse)	Input to Output 1 t = 1.2/50 µs Input to Output 2 t = 1.2/50 µs Output 1 to Output 2 t = 1.2/50 µs	10000 10000 4000			VRMS
T_{op}	Operating Ambient Temperature Range		0		+75	°C
T_{stg}	Storage Temperature Range		−40		+85	°C

OUTPUT POWER CHARACTERISTICS

LT (Line Termination Voltage) = **90V to 110V** **Rs** (Line Resistance) = 50 to 1400 Ω				**LT** (Line Termination Voltage) = **105V to 115V** **Rs** (Line Resistance) = 500 to 1900 Ω			
Max Input Power (mW)	**NT Status**	**Min Output Power 1 (5V)[mW]**	**Min Output Power 2 (40V)[mW]**	**Max Input Power (mW)**	**NT Status**	**Min Output Power 1 (5V)[mW]**	**Min Output Power 2 (40V)[mW]**
600	Activated	420	0	600	Activated	420	0
1150	Activated Emergency	450	420	1150	Activated Emergency	450	420
200	Deactivated	110	0	200	Deactivated	110	0
270	Deactivated Emergency	110	60	270	Deactivated Emergency	110	60
1150	Activated with 40 V Short circuit	450	Short circuit	1150	Activated with 40V Short circuit	450	Short circuit

CONNECTION DIAGRAM AND MECHANICAL DATA

Figure 1.



Package V. Dimensions in mm (inches).

PIN DESCRIPTION

Pin	Description
1	Input (either polarity).
2	Input (either polarity).
3	+5V Output.
4	Return for +5V Output.
5	+40V Output.
6	Return for +40V Output.

VOLTAGE SUPPLY OPERATING AREA

Figure 2 shows the Voltage Supply Operating area during the switch ON-OFF and OFF-ON sequence.

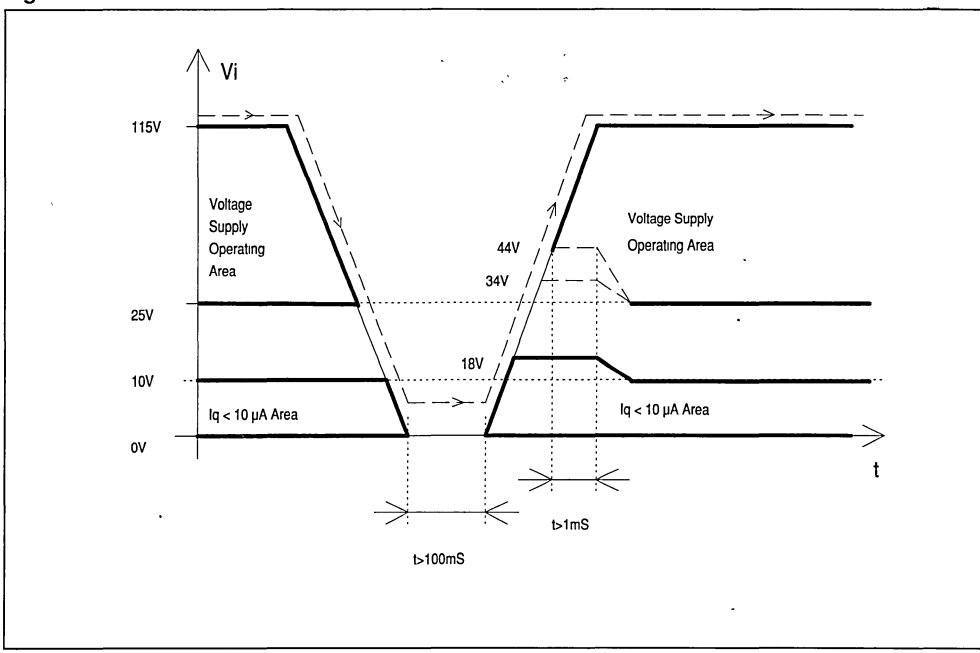
- Switch ON-OFF sequence:

For an Input Voltage Vi > 25V, the circuit operates correctly, because it lies in the Voltage Supply Operating Area.
The converter goes in High Input Impedance mode (I_q < 10µA) when the V_i is lower than 10V. If V_i remains between 0 -10V range for almost for almost 100 ms, the converter is in OFF condition.

- Switch OFF-ON sequence:

The quiescent current Iq remains below 10µA if Vi is lower than 18V.
The start-up voltage is between 34 to 44V. After 1 ms in this condition, the converter is in Voltage Supply Operating Area (V_{in} = 25 to 115V).

Figure 2.

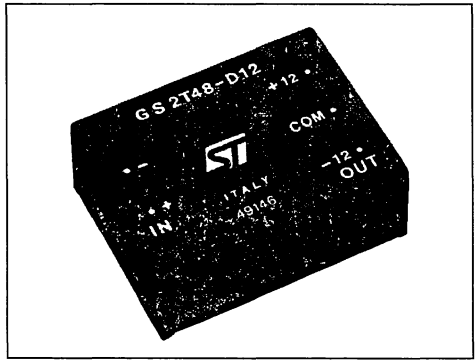


SGS-THOMSON MICROELECTRONICS

GS2T48-D12

2W DUAL OUTPUT DC-DC CONVERTER

Type	V_I	V_O	I_O
GS2T48-D12	38 to 60 V	±12 V	±100mA



DESCRIPTION

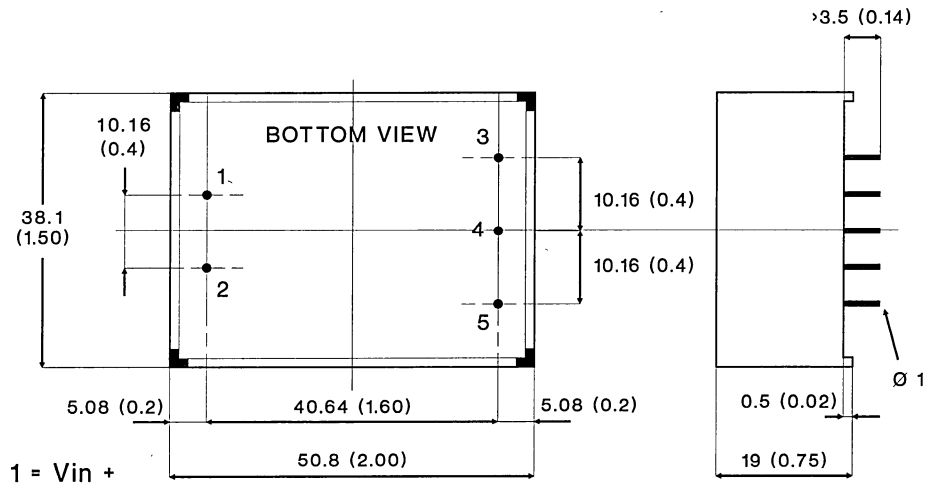
The GS2T48-D12 is a 2.4W DC-DC converter designed to provide an isolated +12V/100mA and -12V/100mA power source.

The module operates from wide input range (38 to 60V) and offers low reflected input current and continuous short-circuit protection.

ELECTRICAL CHARACTERISTICS ($T_{amb.}$= 25° C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_i	Input Voltage	V_{o1} = +12V I_{o1}= 0 to 100mA V_{o2} = – 12V I_{o2} = 0 to – 100mA	38	48	60	V
I_{ir}	Input Reflected Current	V_i = 38 to 60V Full Load		3	5	mApp
V_{o1}	Output Voltage 1	V_i = 38 to 60V I_{o1} = 0 to 100mA I_{o2} = 0 to – 100mA	11.2	12.0	12.8	V
V_{o2}	Output Voltage 2	V_i = 38 to 60V I_{o2} = 0 to – 100mA I_{o1} = 0 to 100mA	– 11.2	– 12.0	– 12.8	V
V_{or1}	Output Ripple Voltage 1	V_i = 38 to 60 I_{o1} = 100mA		30	50	mV_{RMS}
V_{or2}	Output Ripple Voltage 2	V_i = 38 to 60 I_{o2} = – 100mA		30	50	mV_{RMS}
I_{o1}	Output Current 1	V_i = 38 to 60V V_{o1} = 12V	0		100	mA
I_{o2}	Output Current 2	V_i = 38 to 60V V_{o2} = – 12V	0		– 100	mA
V_{is}	Isolation Voltage		500			V_{DC}
f_s	Switching Frequency	V_i = 48V	50	100	150	kHz
η	Efficiency	V_i = 48V Full Load	70	73		%
T_{op}	Operating Ambient Temperature Range		0		+70	°C
T_{stg}	Storage Temperature Range		– 40		+85	°C

CONNECTION DIAGRAM AND MECHANICAL DATA



1 = Vin +
2 = Vin -
3 = Vout -
4 = Out Common Ground
5 = Vout +

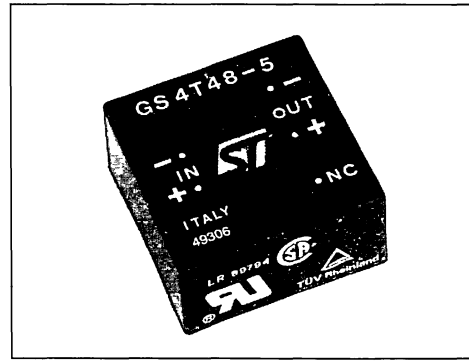
Package E. Dimensions in mm (inches)

SGS-THOMSON MICROELECTRONICS

GS4T48-5

4 W DC-DC CONVERTER

Type	V_I	V_O	I_O
GS4T48-5	38 to 60 V	5 V	800 mA



DESCRIPTION

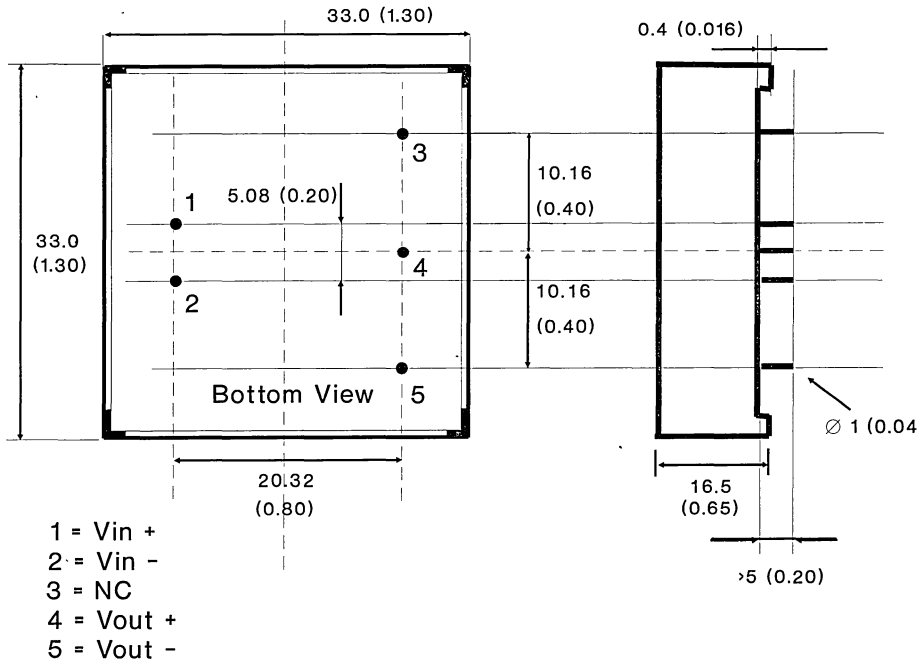
The GS4T48-5 is a 4W DC-DC converter designed to provide a 5V/800mA isolated power source.

The module features a wide input voltage range (38 to 60V), low reflected input current and continuous short-circuit protection. It is certified by UL, CSA (level 3) and TUV as having SELV output when provided with a SELV input.

ELECTRICAL CHARACTERISTICS ($T_{amb.}$= 25° C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_i	Input Voltage	V_O = 5V I_O = 50 to 800mA	38	48	60	V
I_i	Input Current	V_i = 38 to 60V I_O = 800mA			140	mA
I_{ir}	Input Reflected Current	V_i = 48V V_O = 5V I_O = 800mA		20	30	mApp
V_O	Output Voltage	V_i = 38 to 60V I_O = 50 to 800mA	4.8	5	5.2	V
V_{or}	Output Ripple Voltage	V_i = 48V I_O = 800mA BW = 5Hz to 20MHz		30	50	mVpp
δV_{OL}	Line Regulation	V_i = 38 to 60V I_O = 800mA		1	2	mV/V
δV_{OO}	Load Regulation	V_i = 48V I_O = 50 to 800mA		50	75	mV/A
I_O	Output Current	V_i = 38 to 60V V_O = 5V	50		800	mA
I_{osc}	Output Short-circuit Current	V_i = 48V			2	A
V_{is}	Isolation Voltage		500			V_{DC}
f_s	Switching Frequency	V_i = 38 to 60V I_O = 50 to 800mA	50		200	kHz
η	Efficiency	V_i = 48V I_O = 800mA	70	73		%
T_{op}	Operating Ambient Temperature Range	Still Air	0		+55	°C
T_{op}	Operating Ambient Temperature Range	Forced ventilation, air speed = 100 LFM	0		+65	°C
T_{stg}	Storage Temperature Range		−40		+85	°C

CONNECTION DIAGRAM AND MECHANICAL DATA



Package C. Dimensions in mm (inches)

SAFETY APPROVALS

The converter is agency certified to the following safety requirements:

Agency	Requirements	File Number
UL	UL-STD-1950	E141284
CSA	CSA-STD-C22.2 No. 234	LR 99794-3
TUV	EN 60950 DIN VDE 0805	R 9172410

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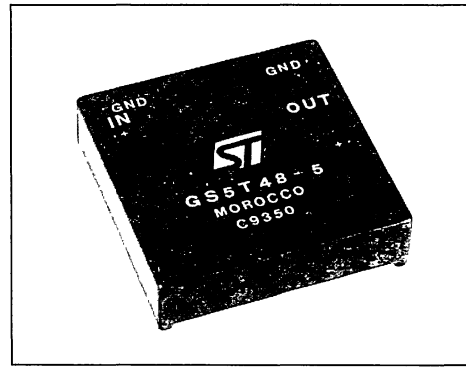
SGS-THOMSON MICROELECTRONICS

GS5T48-5

5 W DC-DC CONVERTER

Type	V_I	V_o	I_o
GS5T48-5	40 to 60 V	5 V	1 A



DESCRIPTION

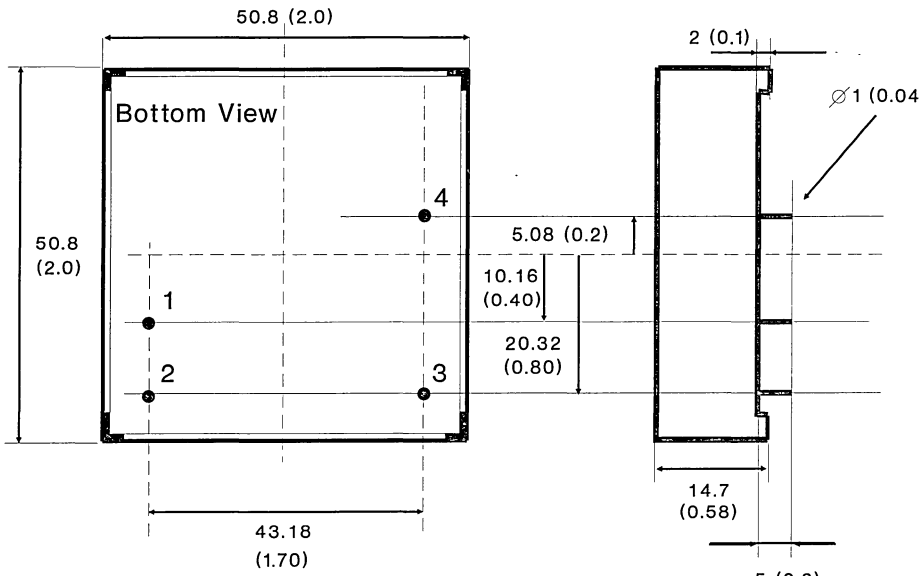
The GS5T48-5 is a 5W DC-DC converter designed to provide a 5V/1A isolated power source in a metal package.

The module features a wide input voltage range (40 to 60V), low reflected input current and continuous short-circuit protection.

ELECTRICAL CHARACTERISTICS ($T_{amb.}$= 25° C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_i	Input Voltage	V_o = 5V I_o = 50 to 1000mA	40	48	60	V
I_i	Input Current	V_i = 40 to 60V I_o = 1000mA			115	mA
I_{ir}	Input Reflected Current	V_i = 48V V_o = 5V I_o= 1000mA		10	15	mApp
V_o	Output Voltage	V_i = 40 to 60V I_o = 50 to 1000mA	4.85	5.00	5.15	V
V_{or}	Output Ripple Voltage	V_i = 48V I_o = 1000mA BW = 5Hz to 20MHz		20	35	mVpp
I_o	Output Current	V_i = 40 to 60V V_o = 5V	50		1000	mA
I_{osc}	Output Short-circuit Current	V_i = 48V			2.3	A
V_{is}	Isolation Voltage		500			V_{DC}
f_s	Switching Frequency	V_i = 40 to 60V I_o = 50 to 1000mA		100		kHz
η	Efficiency	V_i = 48V I_o = 1000mA	70	72		%
T_{op}	Operating Case Temperature Range		−25		+85	°C
T_{stg}	Storage Temperature Range		−40		+105	°C

CONNECTION DIAGRAM AND MECHANICAL DATA



1 = + Vin
2 = - Vin
3 = - Vout
4 = + Vout

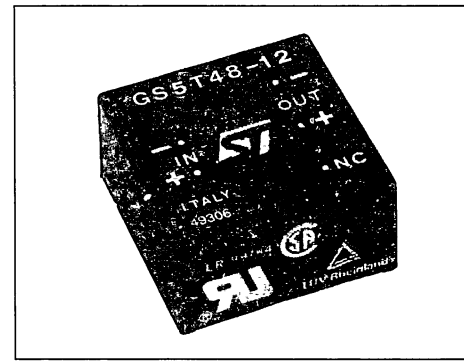
Package G. Dimensions in mm (inches)

SGS-THOMSON MICROELECTRONICS

GS5T48-12

5 W DC-DC CONVERTER

Type	V_i	V_o	I_o
GS5T48-12	38 to 60 V	12 V	420 mA



DESCRIPTION

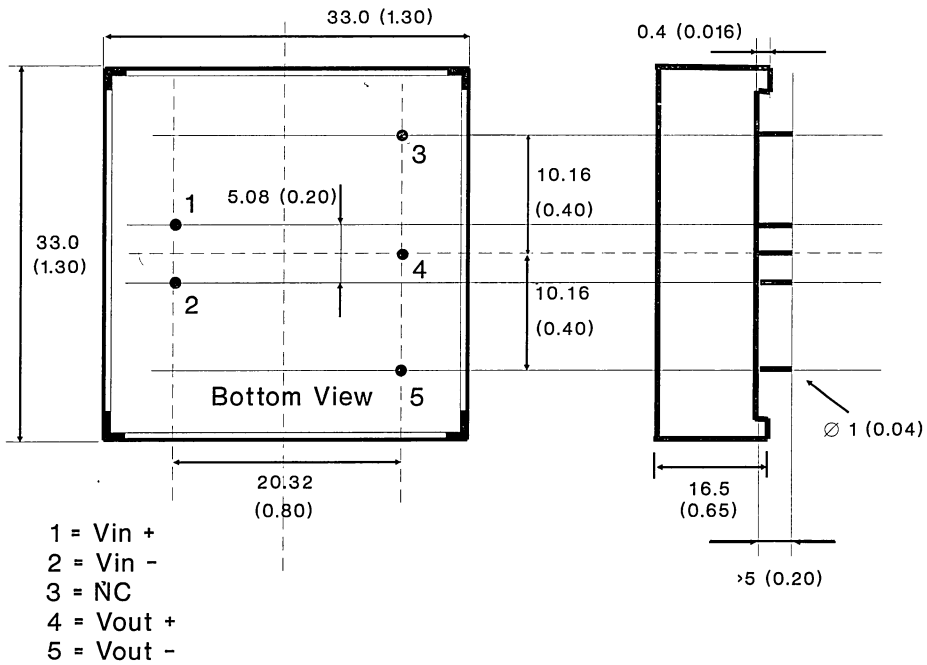
The GS5T48-12 is a 5W DC-DC converter designed to provide a 12V/420mA isolated power source.

The module features a wide input voltage range (38 to 60V), low reflected input current and continuous short-circuit protection. It is certified by UL, CSA (level 3) and TUV as having SELV output when provided with a SELV input.

ELECTRICAL CHARACTERISTICS ($T_{amb.}$= 25° C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_i	Input Voltage	V_o = 12V I_o = 50 to 420mA	38	48	60	V
I_i	Input Current	V_i = 38 to 60V I_o = 420mA			500	mA
I_{ir}	Input Reflected Current	V_i = 48V V_o = 12V I_o = 420mA		25	40	mApp
V_o	Output Voltage	V_i = 38 to 60V I_o = 50 to 420mA	11.5	12	12.5	V
V_{or}	Output Ripple Voltage	V_i = 48V I_o = 420mA BW = 5Hz to 20MHz		50	100	mVpp
δV_{OL}	Line Regulation	V_i = 38 to 60V I_o = 420mA		1	2	mV/V
δV_{OO}	Load Regulation	V_i = 48V I_o = 50 to 420mA		100	150	mV/A
I_o	Output Current	V_i = 38 to 60V V_o = 12V	50		420	mA
I_{osc}	Output Short-circuit Current	V_i = 48V			1.8	A
V_{is}	Isolation Voltage		500			V_{DC}
f_s	Switching Frequency	V_i = 38 to 60V I_o = 50 to 420mA	30		200	kHz
η	Efficiency	V_i = 48V I_o = 420mA	78	80		%
T_{op}	Operating Ambient Temperature Range	Still air	0		+60	°C
T_{op}	Operating Ambient Temperature Range	Forced ventilation, air speed = 100 LFM	0		+70	°C
T_{stg}	Storage Temperature Range		– 40		+85	°C

CONNECTION DIAGRAM AND MECHANICAL DATA



Package C. Dimensions in mm (inches)

SAFETY APPROVALS

The converter is agency certified to the following safety requirements:

Agency	Requirements	File Number
UL	UL-STD-1950	E141284
CSA	CSA-STD-C22.2 No. 234	LR 99794-3
TUV	EN 60950 DIN VDE 0805	R 9172410

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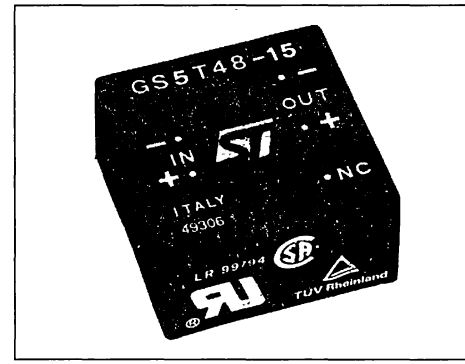
SGS-THOMSON MICROELECTRONICS

GS5T48-15

5 W DC-DC CONVERTER

Type	V_I	V_o	I_o
GS5T48-15	38 to 60 V	15 V	330 mA



DESCRIPTION

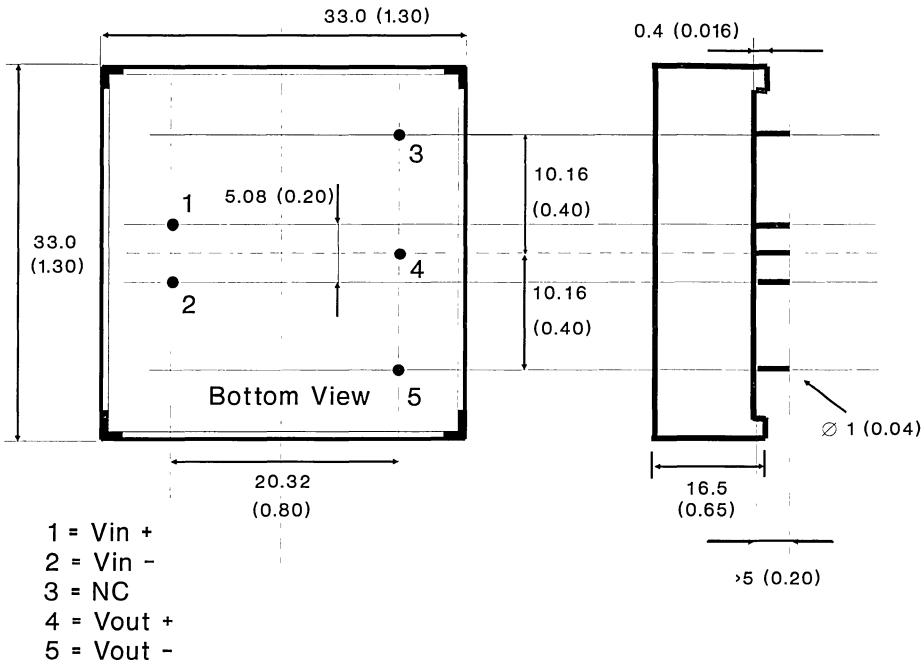
The GS5T48-15 is a 5W DC-DC converter designed to provide a 15V/330mA isolated power source.

The module features a wide input voltage range (38 to 60V), low reflected input current and continuous short-circuit protection. It is certified by UL, CSA (level 3) and TUV as having SELV output when provided with a SELV input.

ELECTRICAL CHARACTERISTICS ($T_{amb.}$= 25° C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_i	Input Voltage	V_o = 15V I_o = 50 to 330mA	38	48	60	V
I_i	Input Current	V_i = 38 to 60V I_o = 330mA			500	mA
I_{ir}	Input Reflected Current	V_i = 48V V_o = 15V I_o = 330mA		25	40	mApp
V_o	Output Voltage	V_i = 38 to 60V I_o = 50 to 330mA	14.5	15	15.5	V
V_{or}	Output Ripple Voltage	V_i = 48V I_o = 330mA BW = 5Hz to 20MHz		50	100	mVpp
δV_{OL}	Line Regulation	V_i = 38 to 60V I_o = 330mA		1	2	mV/V
δV_{OO}	Load Regulation	V_i = 48V I_o = 50 to 330mA		100	150	mV/A
I_o	Output Current	V_i = 38 to 60V V_o = 15V	50		330	mA
I_{osc}	Output Short-circuit Current	V_i = 48V			1.8	A
V_{is}	Isolation Voltage		500			V_{DC}
f_s	Switching Frequency	V_i = 38 to 60V I_o = 50 to 330mA	30		200	kHz
η	Efficiency	V_i = 48V I_o = 330mA	80	82		%
T_{op}	Operating Ambient Temperature Range	Still air	0		+60	°C
T_{op}	Operating Ambient Temperature Range	Forced ventilation, air speed = 100 LFM	0		+70	°C
T_{stg}	Storage Temperature Range		−40		+85	°C

CONNECTION DIAGRAM AND MECHANICAL DATA



Package C. Dimensions in mm (inches)

SAFETY APPROVALS

The converter is agency certified to the following safety requirements:

Agency	Requirements	File Number
UL	UL-STD-1950	E141284
CSA	CSA-STD-C22.2 No. 234	LR 99794-3
TUV	EN 60950 DIN VDE 0805	R 9172410

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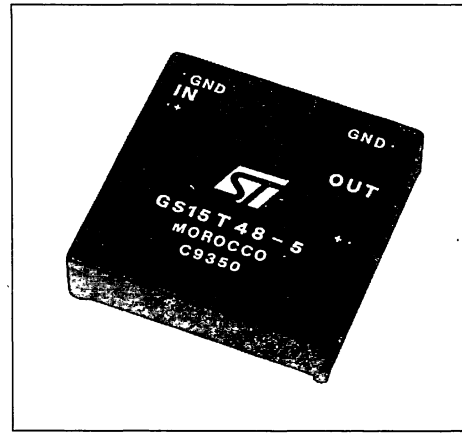
SGS-THOMSON MICROELECTRONICS

GS15T48-5

15W DC-DC CONVERTER

Type	V_I	V_o	Io
GS15T48-5	40 to 60 V	5 V	3 A



DESCRIPTION

The GS15T48-5 is a 15W DC-DC converter designed to provide a 5V/3A isolated output from a 48V input in a metal package.

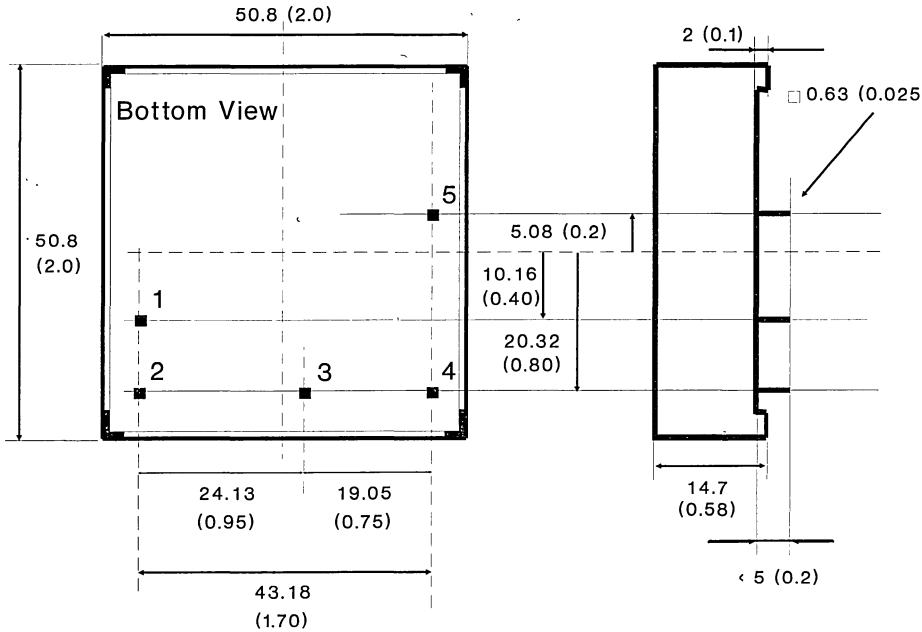
High frequency forward switching configuration ensures high efficiency (80% typ.); input filter minimizes reflected input current and continuous short-circuit protection is provided.

The integral heatsink allows a large power handling capability and it features also an effective shielding to minimize EMI.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_i	Input Voltage	V_O = 5V I_O = 0 to 3A	40	48	60	V
I_i	Input Current	V_i = 48V I_O = 3A		400		mA
I_{ir}	Input Reflected Current	V_i = 48V V_O = 5V I_O = 3A		50	80	mApp
I_{iq}	Input Quiescent Current	V_i = 48V V_O = 5V I_O = 0A		20		mA
V_O	Output Voltage	V_i = 40 to 60V I_O = 0 to 3A	4.75	5	5.25	V
δV_{OL}	Line Regulation	V_i = 40 to 60V I_O = 3A		10	20	mV
δV_{OO}	Load Regulation	V_i = 48V I_O = 0 to 3A		10	20	mV
V_{or}	Output Ripple Voltage	V_i = 48V I_O = 3A		20	50	mVpp
I_O	Output Current	V_i = 40 to 60V	0		3	A
I_{osc}	Output Short-circuit Current	V_i = 48V		5	6	A
V_{is}	Isolation Voltage		750			V_{DC}
f_s	Switching Frequency	V_i = 40 to 60V I_O = 0 to 3A		250		kHz
η	Efficiency	V_i = 48V I_O = 3A		80		%
R_{thc}	Thermal Resistance Case to Ambient	T_{amb} = 25°C V_i = 48V I_O = 3A		8		°C/W
T_{cmax}	Maximum Case Temperature				+85	°C
T_{stg}	Storage Temperature Range		−40		+105	°C

CONNECTION DIAGRAM AND MECHANICAL DATA



Package G. Dimensions in mm (inches)

PIN DESCRIPTION

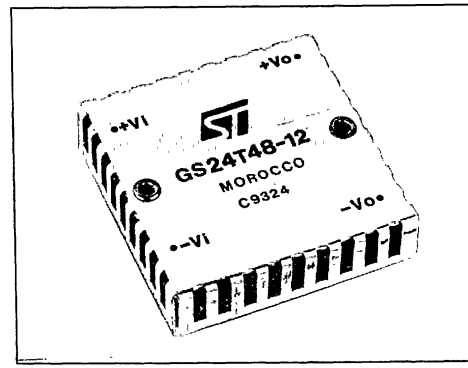
Pin	Function	Description
1	+ Input	DC input voltage (48V nom.)
2	- Input	Return for input voltage
3	Case	Case connection
4	- Output	Negative isolated output voltage
5	+ Output	Positive isolated output voltage

SGS-THOMSON MICROELECTRONICS

GS24T48-12

24 W DC-DC CONVERTER

Type	V_i	V_o	I_o
GS24T48-12	36 to 72 V	12 V	2 A



DESCRIPTION

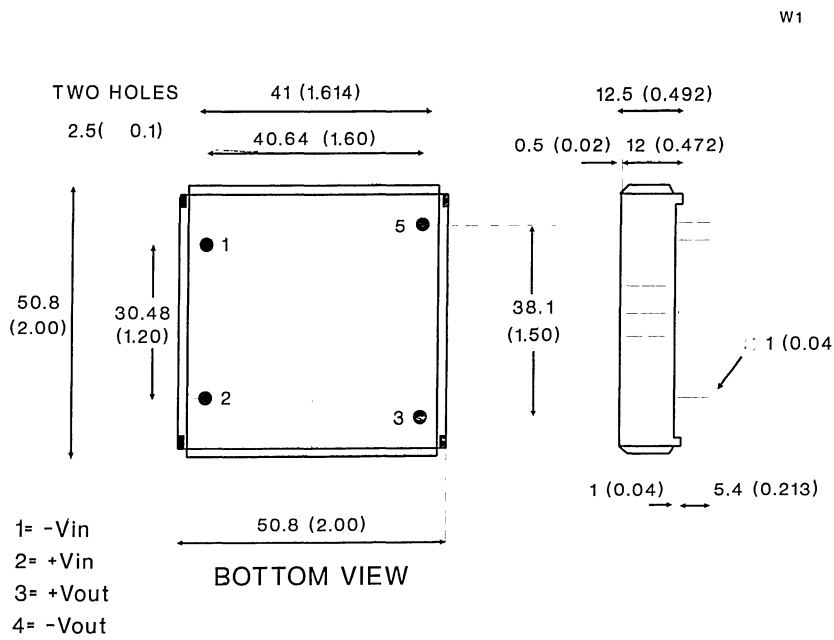
The GS24T48-12 is a 24W DC-DC converter designed to provide a 12V/2A isolated power source.

The module features a wide input voltage range (36 to 72V), low reflected input currend and short-circuit protection.

ELECTRICAL CHARACTERISTICS ($T_{amb.}$= 25° C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_i	Input Voltage	V_O = 12V I_O = 0.1 to 2A	36	48	72	V
I_i	Input Current	V_i = 48V V_O = 12V I_O = 2A		0.58	0.60	A
I_{ir}	Input Reflected Current	V_i = 48V V_O = 12V I_O = 2A		90	120	mApp
$I_{iinr.}$	Input Inrush Current	V_i = 48V V_O = 12V I_O = 2A		18	22	Ap
I_{isc}	Input Shortcircuit Current	V_i = 48V V_O = 0V		100	150	mA
V_O	Output Voltage	V_i = 36 to 72V I_O = 0.1 to 2A	11.4	12	12.6	V
V_{or}	Output Ripple Voltage	V_i = 48V V_O = 12V I_O = 2A		30	60	mVpp
V_{on}	Output Noise Voltage	V_i = 48V V_O = 12V I_O = 2A BW = 100MHz			500	mVpp
δV_{OL}	Line Regulation	V_i = 36 to 72V I_O = 2A		20	30	mV
δV_{OO}	Load Regulation	V_i = 48V I_O = 0.1 to 2A		20	30	mV
I_O	Output Current	V_i = 36 to 72V V_O = 12V	0.1		2	A
I_{osc}	Output Short-circuit Current	V_i = 48V V_O = 0V		1.0	1.5	A
V_{is}	Isolation Voltage		500			V_{DC}
f_s	Switching Frequency	V_i = 36 to 72V I_O = 0.1 to 2A		450		kHz
η	Efficiency	V_i = 48V V_O = 12V I_O = 2A	84	86		%
R_{th}	Thermal Resistance	Case-to-Ambient		13		°C/W
T_{cop}	Operating Case Temperature Range		0		+85	°C
T_{stg}	Storage Temperature Range		− 20		+105	°C

CONNECTION DIAGRAM AND MECHANICAL DATA



Package W. Dimensions in mm. (inches)

GS25/30T48 Family

25/30 W DC-DC CONVERTER FAMILY

Type	V_I	V_O	I_O
GS25T48-5	36 to 72 V	5 V	5 A
GS30T48-12	36 to 72 V	12 V	2,5 A
GS30T48-15	36 to 72 V	15 V	2 A

FEATURES

- MTBF in excess of 1M hours at +45°C ambient temperature
- Wide input voltage range (36 to 72V)
- No external component required
- High efficiency (see data)
- Non latching permanent short-circuit protection
- Overvoltage protection
- Redundant operation
- Remote output voltage sense
- Remote INHIBIT/ENABLE
- Soft-start
- Minimized reflected input current
- Reverse input polarity protection
- Peak input overvoltage withstand
- No derating over the temperature range
- 500V_{DC} minimum isolation between input and output
- PCB or chassis mountable

DESCRIPTION

The GS25T48-5, GS30T48-12 and GS30T48-15 are isolated DC-DC converters designed for general purpose application.

The output power is in the range of 25W to 30W. To ensure very long life, these converters do not use electrolytic aluminum capacitors or optoelectronic feedback systems.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage	34 to 72V	V
V_{ipk}	Input Transient Overvoltage (t ≤ 1sec.)	90	V
V_{ir}	Input Reverse Voltage	– 100	V
T_{stg}	Storage Temperature Range	– 55 to +105	°C
T_{op}	Operating Temperature Range	– 25 to +71	°C

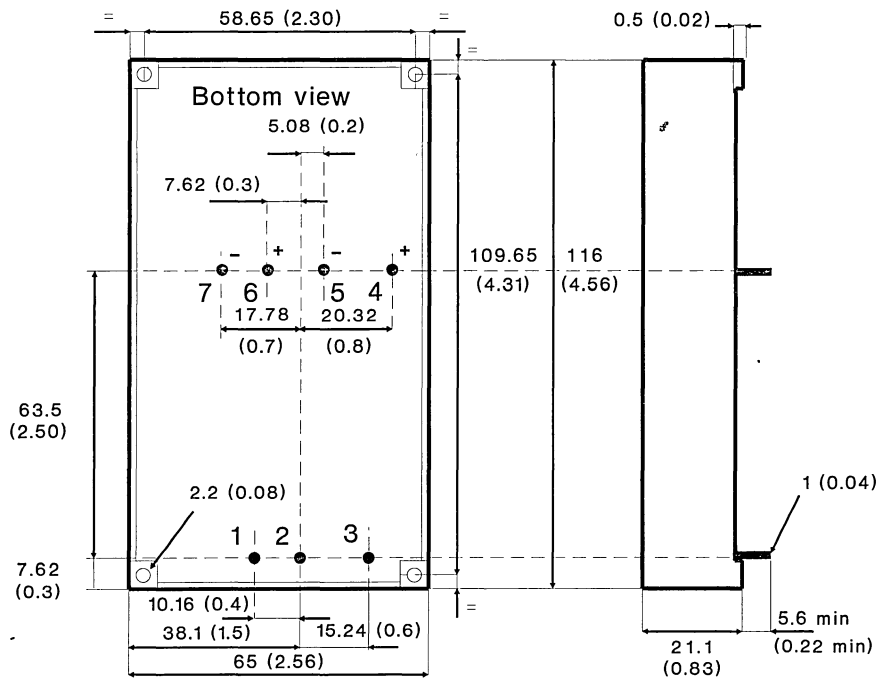
ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_i	Input Voltage	Full Load	36	48	72	V
I_i	Input Current	GS25T48-5 Full Load		640		mA
		GS30T48-12 Full Load		730		
		GS30T48-15 Full Load		730		
I_{ir}	Input Reflected Current	V_i = 48V Full Load		50		mApp
I_{isc}	Input Short-circuit Current	GS25T48-5 V_i = 48V		710		mA
		GS30T48-12 V_i = 48V		820		
		GS30T48-15 V_i = 48V		820		
I_{iq}	Input Quiescent Current	V_i = 48V Converter OFF		5		mA
V_{inhl}	Low Inhibit Voltage	V_i = 48V Full Load			1.2	V
V_{enh}	High Enable Voltage	V_i = 48V Full Load	1.8 (open)			V
I_{inh}	Input Inhibit Current	V_i = 48V Full Load		1		mA
V_o	Output Voltage	GS25T48-5 V_i = 48V Full Load	4.95	5.00	5.05	V
		GS30T48-12 V_i = 48V Full Load	11.88	12.00	12.12	
		GS30T48-15 V_i = 48V Full Load	14.85	15.00	15.15	
V_{or}	Output Ripple and Noise Voltage	V_i = 48V Full Load		10		mVpp
δV_{OL}	Line Regulation	V_i = 36 to 72V Full Load		±0.001		%
δV_{OO}	Load Regulation	V_i = 48V Full Load to No Load		±0.05		%
V_{oov}	Output Overvoltage Protection	GS25T48-5 Full Load V_i = 48V			6.8	V
		GS30T48-12 Full Load V_i = 48V			15	
		GS30T48-15 Full Load V_i = 48V			18	
ΔV_o	Total remote sense compensation	V_i = 36V			1	V
T_c	Temperature Coefficient	V_i = 48V Full Load Operating Temperature Range			+0.02	%/°C

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified) (cont'd)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_o	Output Current	GS25T48-5 V_i = 36 to 72V	0		5	A
		GS30T48-12 V_i = 36 to 72V	0		2.5	
		GS30T48-15 V_i = 36 to 72V	0		2	
I_{osck}	Output Current Limit	GS25T48-5 V_i = 48V Overload			5.5	A
		GS30T48-12 V_i = 48V Overload			2.75	
		GS30T48-15 V_i = 48V Overload			2.2	
t_{ss}	Soft-start Time	V_i = 48V Full Load		30		ms
t_{rt}	Transient Recovery Time	V_i = 48V Step Load Change δI_o = 25%		75		µs
V_{is}	Isolation Voltage		500			V_{DC}
R_{is}	Isolation Resistance		10^9			Ω
f_s	Switching Frequency			150		kHz
η	Efficiency	GS25T48-5 V_i = 48V Full Load		81		%
		GS30T48-12 V_i = 48V Full Load		86		
		GS30T48-15 V_i = 48V Full Load		86		
R_{thc}	Thermal Resistance Case to Ambient			4		°C/W

CONNECTION DIAGRAM AND MECHANICAL DATA



Package F. Dimensions in mm. (inches)

PIN DESCRIPTION

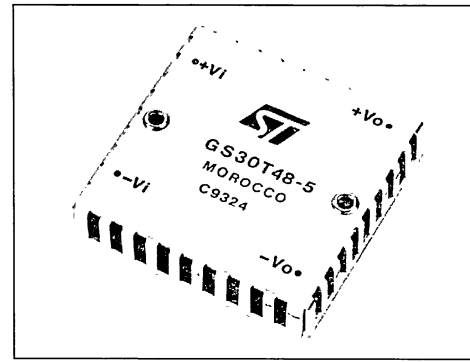
Pin	Function	Description
1	- IN	Negative input voltage.
2	+ IN	Positive input voltage. Unregulated input voltage (typically 48V) must be applied between pins 1-2. The input section of the DC-DC converter is protected against reverse polarity by a series diode. No external fuse is required. Input is filtered by a Pi network.
3	ON/OFF	Logically compatible with CMOS or open collector TTL. The converter is ON (Enable) when the voltage applied to this pin with reference to pin 1 is higher than 1.8V. The converter is OFF (Inhibit) for a control voltage lower than 1.2V. When the pin is unconnected the converter is ON (Enable).
4	+ SENSE	Senses the remote load high side. To be connected to pin 6 when remote sense is not used.
5	- SENSE	Senses the remote load return. To be connected to pin 7 when remote sense is not used.
6	+ OUT	Output voltage.
7	- OUT	Output voltage return.

SGS-THOMSON MICROELECTRONICS

GS30T48-5

30 W DC-DC CONVERTER

Type	V_I	V_o	I_o
GS30T48-5	36 to 72 V	5 V	6 A



DESCRIPTION

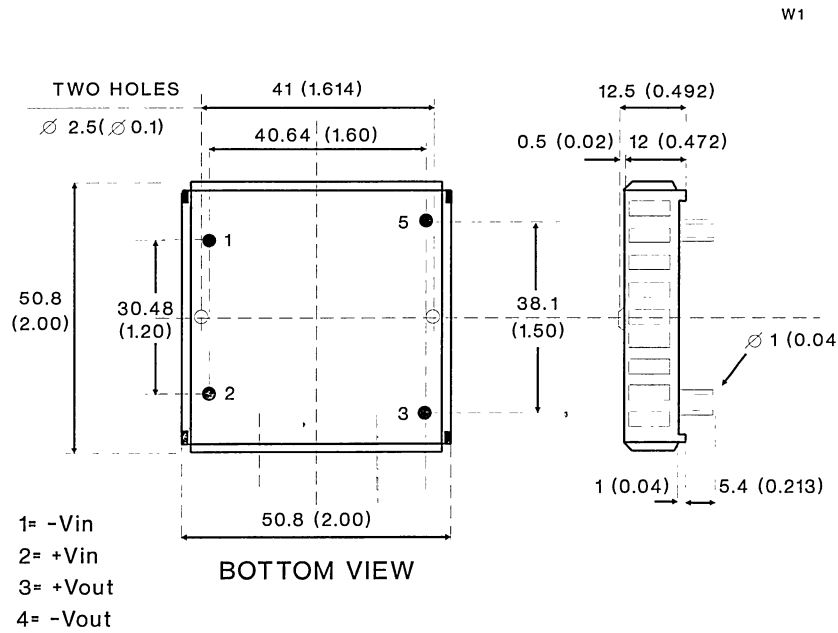
The GS30T48-5 is a 30W DC-DC converter designed to provide a 5V/6A isolated power source.

The module features a wide input voltage range (36 to 72V), low reflected input current and short-circuit protection.

ELECTRICAL CHARACTERISTICS ($T_{amb.}$= 25° C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_i	Input Voltage	V_o = 5V I_o = 0.05 to 6A	36	48	72	V
I_i	Input Current	V_i = 48V V_o = 5V I_o = 6A		0.79	0.82	A
I_{ir}	Input Reflected Current	V_i = 48V V_o = 5V I_o = 6A		250	300	mApp
I_{iinr}	Input Inrush Current	V_i = 48V V_o = 5V I_o = 6A		18	22	Ap
I_{isc}	Input Shortcircuit Current	V_i = 48V V_o = 0V		45	70	mA
V_o	Output Voltage	V_i = 36 to 72V I_o = 0.05 to 6A	4.75	5.00	5.25	V
V_{or}	Output Ripple Voltage	V_i = 48V V_o = 5V I_o = 6A		150	200	mVpp
δV_{OL}	Line Regulation	V_i = 36 to 72V I_o = 6A		2	10	mV
δV_{OO}	Load Regulation	V_i = 48V I_o = 0.05 to 6A		2	10	mV
I_o	Output Current	V_i = 36 to 72V V_o = 5V	0.05		6	A
I_{osc}	Output Short-circuit Current	V_i = 48V V_o = 0V		0.85	1.1	A
V_{is}	Isolation Voltage		500			V_{DC}
f_s	Switching Frequency	V_i = 36 to 72V I_o = 0.05 to 6A		450		kHz
η	Efficiency	V_i = 48V V_o = 5V I_o = 6A	77	80		%
R_{th}	Thermal Resistance	Case-to-Ambient		13		°C/W
T_{cop}	Operating Case Temperature Range		0		+85	°C
T_{stg}	Storage Temperature Range		– 20		+105	°C

CONNECTION DIAGRAM AND MECHANICAL DATA



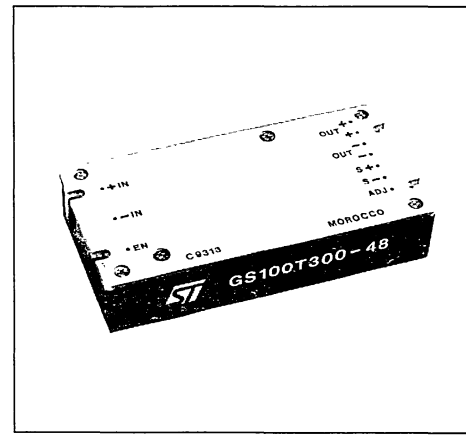
Package W. Dimensions in mm (inches)

70W/100W DC-DC CONVERTERS FAMILY

Type	V_I	V_O	I_O
GS70T300-3.5	200 to 400 V	3,5 V	20 A
GS100T300-5	200 to 400 V	5,2 V	20 A
GS100T300-12	200 to 400 V	12,0 V	8,3 A
GS100T300-15	200 to 400 V	15,0 V	6,6 A
GS100T300-24	200 to 400 V	24,0 V	4,2 A
GS100T300-48	200 to 400 V	48,0 V	2,0 A

FEATURES

- High input voltage range bus: 200 to 400Vdc
- UL, TUV approved
- High output power (up to 100W)
- High efficiency (80% min. on GS100T300-5 module)
- Output voltages range: 3.5-5.2-12-15-24 and 48V
- Output voltage adjustable by external pin
- Remote load voltage sense compensation
- Output short-circuit protection
- Output overvoltage protection
- Undervoltage lock-out
- Minimal overshoot during load transients
- 3750V_{RMS} input to output isolation voltage
- Internal input and output filtering
- Softstart
- PCB or chassis mountable
- Mechanical Dimensions 101,6 • 50,8 • 20 mm (4,00 • 2,00 • 0,79 inches)



DESCRIPTION

The GS70/100T300 family includes 70/100W DC-DC converters used to generate isolated output voltages with an output current up to 20A from a wide range input voltage (200 to 400Vdc).
All the GS70/100T300 family modules require an external fuse (1 Amps.) on the input side.

GS70T300-3.5 ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_i	Input Voltage	V_O = 3.5V I_O = 0 to 20A (Operating Conditions)	200	300	400	V_{DC}
Q_i	Inrush Charge	V_i = 400V I_O = 20A		$40 \bullet 10^{-6}$		C
P_i	Input Power	V_i = 300V I_O = 0A (No Load)		2.5		W
V_O	Output Voltage	V_i = 200 to 400V I_O = 0 to 20A	3.43	3.5	3.57	V
V_O	Output Voltage Range	V_i = 200 to 400V I_O = 0 to 20A (see fig. 2)	1.75		3.5	V
Vorn	Output Ripple and Noise Voltage	V_i = 300V I_O = 20A BW = 0 to 20Mhz		35	40	mVpp
Vol	Output Overvoltage Limit Initiation	V_i = 200 to 400V I_O = 0 to 20A		1.2•Vo		V
δV_{OL}	Line Regulation	V_i = 200 to 400V I_O = 20A			±0.1	%
δV_{OO}	Load Regulation	V_i = 300V I_O = 0 to 20A			±0.1	%
ΔV_O	Total Remote Sense Compensation	V_i = 200 to 400V			0.6	V
δV_O	Peak Load Transient Response	V_i = 300V δI_O = 10A		500		mVp
SVR	Supply Voltage Rejection	f = 100Hz		55		dB
I_O	Output Current	V_i = 200 to 400V V_O = 3.3V	0		20	A
I_{OI}	Overcurrent Limit Initiation	V_i = 300V	21	23	25	A
I_{OSC}	Shortcircuit Output Current	V_i = 300V	18	23	28	A
t_S	Load Transient Settling Time	V_i = 300V δI_O = 10A		300		µs
ton	Turn-on Time	V_i = 200V I_O = 20A		6	10	ms
Vis	Isolation Voltage	Input to Output	3750			V_{RMS}
		Input to Baseplate	2500			
		Output to Baseplate	500			
f_S	Switching Frequency	V_i = 200 to 400V I_O = 0 to 20A		150		kHz
η	Efficiency	V_i = 300V I_O = 20A	78	79		%
Rth	Thermal Resistance	Baseplate to Ambient		7.5		°C/W
Tcop	Operating Case Temperature Range		0		+70	°C
Tstg	Storage Temperature Range		−40		+100	°C

GS100T300-5 ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_i	Input Voltage	V_O = 5V I_O = 0 to 20A (Operating Conditions)	200	300	400	V_{DC}
Q_i	Inrush Charge	V_i = 400V I_O = 20A		$40 \bullet 10^{-6}$		C
P_i	Input Power	V_i = 300V I_O = 0A (No Load)		2.5		W
V_O	Output Voltage	V_i = 200 to 400V I_O = 0 to 20A	5.09	5.20	5.30	V
V_O	Output Voltage Range	V_i = 200 to 400V I_O = 0 to 20A (see fig. 2)	2.6		5.20	V
V_{orn}	Output Ripple and Noise Voltage	V_i = 300V I_O = 20A BW = 0 to 20Mhz		40	50	mVpp
V_{OI}	Output Overvoltage Limit Initiation	V_i = 200 to 400V I_O = 0 to 20A		1.2•Vo		V
δV_{OL}	Line Regulation	V_i = 200 to 400V I_O = 20A			±0.1	%
δV_{OO}	Load Regulation	V_i = 300V I_O = 0 to 20A			±0.1	%
ΔV_O	Total Remote Sense Compensation	V_i = 200 to 400V			0.6	V
δV_O	Peak Load Transient Response	V_i = 300V δI_O = 1A		500		mVp
SVR	Supply Voltage Rejection	f = 100Hz		55		dB
I_O	Output Current	V_i = 200 to 400V V_O = 5V	0		20	A
I_{OI}	Overcurrent Limit Initiation	V_i = 300V	21	23	25	A
I_{OSC}	Shortcircuit Output Current	V_i = 300V	18	23	28	A
t_S	Load Transient Settling Time	V_i = 300V δI_O = 1A		300		µs
t_{on}	Turn-on Time	V_i = 200V I_O = 20A		6	10	ms
V_{IS}	Isolation Voltage	Input to Output	3750			V_{RMS}
		Output to Baseplate	500			
		Input to Baseplate	2500			
f_S	Switching Frequency	V_i = 200 to 400V I_O = 0 to 20A		150		kHz
η	Efficiency	V_i = 300V I_O = 20A	80	81		%
R_{th}	Thermal Resistance	Baseplate to Ambient		7.5		°C/W
T_{cop}	Operating Case Temperature Range		0		+70	°C
T_{stg}	Storage Temperature Range		− 40		+100	°C

GS100T300-12 ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_i	Input Voltage	V_o = 12V I_o = 0 to 8.3A (Operating Conditions)	200	300	400	V_{DC}
Q_i	Inrush Charge	V_i = 400V I_o = 8.3A		$40 \bullet 10^{-6}$		C
P_i	Input Power	V_i = 300V I_o = 0A (No Load)		2.5		W
V_o	Output Voltage	V_i = 200 to 400V I_o = 0 to 8.3A	11.76	12.00	12.24	V
V_o	Output Voltage Range	V_i = 200 to 400V I_o = 0 to 8.3A (see fig. 2)	6.0		13.2	V
V_{orn}	Output Ripple and Noise Voltage	V_i = 300V I_o = 8.3A BW = 0 to 20Mhz		100	120	mVpp
V_{ol}	Output Overvoltage Limit Initiation	V_i = 200 to 400V I_o = 0 to 8.3A		1.2•Vo		V
δV_{OL}	Line Regulation	V_i = 200 to 400V I_o = 8.3A			±0.1	%
δV_{OO}	Load Regulation	V_i = 300V I_o = 0 to 8.3A			±0.1	%
ΔV_o	Total Remote Sense Compensation	V_i = 200 to 400V			0.6	V
δV_o	Peak Load Transient Response	V_i = 300V δI_o = 4A		500		mVp
SVR	Supply Voltage Rejection	f = 100Hz		45		dB
I_o	Output Current	V_i = 200 to 400V V_o = 12V	0		8.3	A
I_{ol}	Overcurrent Limit Initiation	V_i = 300V	8.8	9.1	11.0	A
I_{osc}	Shortcircuit Output Current	V_i = 300V	7.5	9.0	11.0	A
t_s	Load Transient Settling Time	V_i = 300V δI_o = 4A		300		µs
t_{on}	Turn-on Time	V_i = 200V I_o = 8.3A		6	10	ms
V_{is}	Isolation Voltage	Input to Output	3750			V_{RMS}
		Input to Baseplate	2500			
		Output to Baseplate	500			
f_s	Switching Frequency	V_i = 200 to 400V I_o = 0 to 8.3A		150		kHz
η	Efficiency	V_i = 300V I_o = 8.3A	83	84		%
Rth	Thermal Resistance	Baseplate to Ambient		7.5		°C/W
Tcop	Operating Case Temperature Range		0		+70	°C
Tstg	Storage Temperature Range		– 40		+100	°C

GS100T300-15 ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_i	Input Voltage	V_O = 15V I_O = 0 to 6.6A (Operating Conditions)	200	300	400	V_{DC}
Q_i	Inrush Charge	V_i = 400V I_O = 6.6A		$40 \bullet 10^{-6}$		C
P_i	Input Power	V_i = 300V I_O = 0A (No Load)		2.5		W
V_O	Output Voltage	V_i = 200 to 400V I_O = 0 to 6.6A	14.7	15.0	15.3	V
V_O	Output Voltage Range	V_i = 200 to 400V I_O = 0 to 6.6A (see fig. 2)	7.5		16.5	V
Vorn	Output Ripple and Noise Voltage	V_i = 300V I_O = 6.6A BW = 0 to 20Mhz		110	150	mVpp
Vol	Output Overvoltage Limit Initiation	V_i = 200 to 400V I_O = 0 to 6.6A		1.2•Vo		V
δV_{OL}	Line Regulation	V_i = 200 to 400V I_O = 6.6A			±0.1	%
δV_{OO}	Load Regulation	V_i = 300V I_O = 0 to 6.6A			±0.1	%
ΔV_O	Total Remote Sense Compensation	V_i = 200 to 400V			0.6	V
δV_O	Peak Load Transient Response	V_i = 300V δI_O = 3.3A		500		mVp
SVR	Supply Voltage Rejection	f = 100Hz		45		dB
I_O	Output Current	V_i = 200 to 400V V_O = 15V	0		6.6	A
Iol	Overcurrent Limit Initiation	V_i = 300V	7.1	7.5	8.0	A
Iosc	Shortcircuit Output Current	V_i = 300V	6.5	8.0	10.0	A
t_s	Load Transient Settling Time	V_i = 300V δI_O = 3.3A		300		µs
ton	Turn-on Time	V_i = 200V I_O = 6.6A		6	10	ms
Vis	Isolation Voltage	Input to Output	3750			V_{RMS}
		Input to Baseplate	2500			
		Output to Baseplate	500			
f_s	Switching Frequency	V_i = 200 to 400V I_O = 0 to 6.6A		150		kHz
η	Efficiency	V_i = 300V I_O = 6.6A	84	85		%
Rth	Thermal Resistance	Baseplate to Ambient		7.5		°C/W
Tcop	Operating Case Temperature Range		0		+70	°C
Tstg	Storage Temperature Range		−40		+100	°C

GS100T300-24 ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

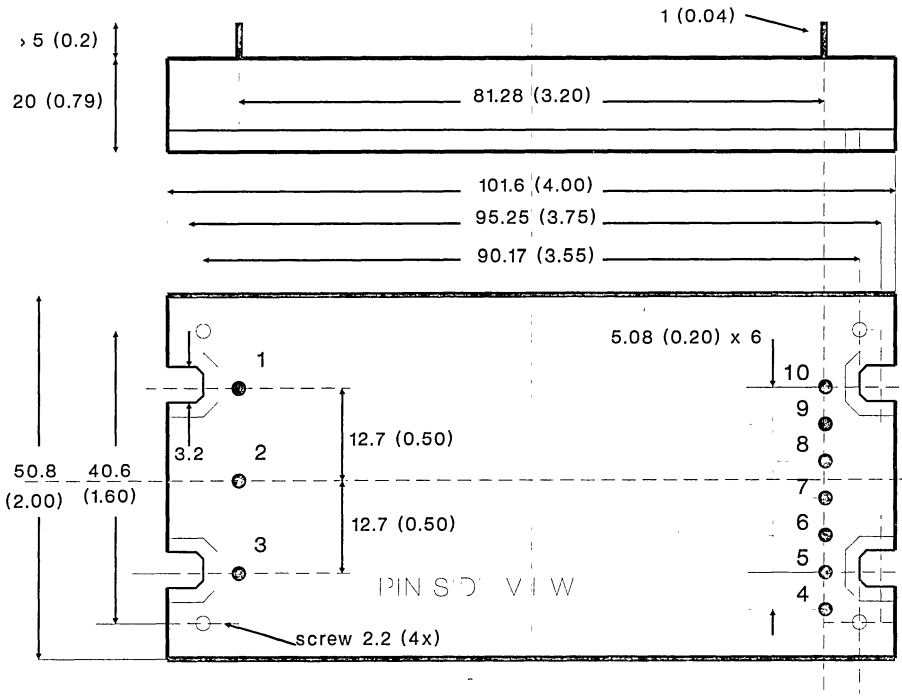
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_i	Input Voltage	V_o = 24V I_o = 0 to 4.2A (Operating Conditions)	200	300	400	V_{DC}
Q_i	Inrush Charge	V_i = 400V I_o = 4.2A		$40 \bullet 10^{-6}$		C
P_i	Input Power	V_i = 300V I_o = 0A (No Load)		2.5		W
V_o	Output Voltage	V_i = 200 to 400V I_o = 0 to 4.2A	23.5	24.0	24.5	V
V_o	Output Voltage Range	V_i = 200 to 400V I_o = 0 to 4.2A (see fig. 2)	12.0		26.4	V
V_{orn}	Output Ripple and Noise Voltage	V_i = 300V I_o = 4.2A BW = 0 to 20Mhz		200	240	mVpp
V_{ol}	Output Overvoltage Limit Initiation	V_i = 200 to 400V I_o = 0 to 4.2A		1.2•Vo		V
δV_{OL}	Line Regulation	V_i = 200 to 400V I_o = 4.2A			±0.1	%
δV_{OO}	Load Regulation	V_i = 300V I_o = 0 to 4.2A			±0.1	%
ΔV_o	Total Remote Sense Compensation	V_i = 200 to 400V			0.6	V
δV_o	Peak Load Transient Response	V_i = 300V δI_o = 2.1A		500		mVp
SVR	Supply Voltage Rejection	f = 100Hz		40		dB
I_o	Output Current	V_i = 200 to 400V V_o = 24V	0		4.2	A
I_{ol}	Overcurrent Limit Initiation	V_i = 300V	4.5	5.0	5.5	A
I_{osc}	Shortcircuit Output Current	V_i = 300V	3.8	4.5	6.0	A
t_s	Load Transient Settling Time	V_i = 300V δI_o = 2.1A		300		µs
t_{on}	Turn-on Time	V_i = 200V I_o = 4.2A		6	10	ms
V_{is}	Isolation Voltage	Input to Output	3750			V_{RMS}
		Input to Baseplate	2500			
		Output to Baseplate	500			
f_s	Switching Frequency	V_i = 200 to 400V I_o = 0 to 4.2A		150		kHz
η	Efficiency	V_i = 300V I_o = 4.2A	84	85		%
R_{th}	Thermal Resistance	Baseplate to Ambient		7.5		°C/W
T_{cop}	Operating Case Temperature Range		0		+70	°C
T_{stg}	Storage Temperature Range		– 40		+100	°C

GS100T300-48 ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_i	Input Voltage	V_o = 48V I_o = 0 to 2.1A (Operating Conditions)	200	300	400	V_{DC}
Q_i	Inrush Charge	V_i = 400V I_o = 2.1A		$40 \bullet 10^{-6}$		C
P_i	Input Power	V_i = 300V I_o = 0A (No Load)		2.5		W
V_o	Output Voltage	V_i = 200 to 400V I_o = 0 to 2.1A	47.04	48.00	48.96	V
V_o	Output Voltage Range	V_i = 200 to 400V I_o = 0 to 2.1A (see fig. 2)	24.0		52.8	V
V_{orn}	Output Ripple and Noise Voltage	V_i = 300V I_o = 2.1A BW = 0 to 20Mhz		400	500	mVpp
V_{ol}	Output Overvoltage Limit Initiation	V_i = 200 to 400V I_o = 0 to 2.1A		1.2•Vo		V
δV_{OL}	Line Regulation	V_i = 200 to 400V I_o = 2.1A			±0.1	%
δV_{OO}	Load Regulation	V_i = 300V I_o = 0 to 2.1A			±0.1	%
ΔV_o	Total Remote Sense Compensation	V_i = 200 to 400V			0.6	V
δV_o	Peak Load Transient Response	V_i = 300V δI_o = 1A		500		mVp
SVR	Supply Voltage Rejection	f = 100Hz		35		dB
I_o	Output Current	V_i = 200 to 400V V_o = 48V	0		2	A
I_{ol}	Overcurrent Limit Initiation	V_i = 300V	2.1	2.3	2.5	A
I_{osc}	Shortcircuit Output Current	V_i = 300V	1.8	2.3	2.8	A
t_s	Load Transient Settling Time	V_i = 300V δI_o = 1A		300		µs
t_{on}	Turn-on Time	V_i = 200V I_o = 2.1A		6	10	ms
V_{is}	Isolation Voltage	Input to Output	3750			V_{RMS}
		Input to Baseplate	2500			
		Output to Baseplate	500			
f_s	Switching Frequency	V_i = 200 to 400V I_o = 0 to 2.1A		150		kHz
η	Efficiency	V_i = 300V I_o = 2.1A	84	85		%
Rth	Thermal Resistance	Baseplate to Ambient		7.5		°C/W
Tcop	Operating Case Temperature Range		0		+70	°C
Tstg	Storage Temperature Range		− 40		+100	°C

CONNECTION DIAGRAM AND MECHANICAL DATA

Figure 1.



Package R; dimensions in mm (inches)

PIN DESCRIPTION

Pin	Function	Description
1	ENABLE	The converter is ON (Enable) when the voltage applied to this pin with reference to pin 2 is lower than 1.2V. The converter is OFF (Inhibit) for a control voltage in the range of 2.1 to 5V. When the pin is unconnected the converter is OFF (Inhibit).
2	- Vin	Negative input voltage.
3	+ Vin	Positive input voltage. Unregulated input voltage in the range of 200 to 400Vdc must be applied between pin 2-3.
4,5	+ Vo	+Vo output voltage.
6,7	- Vo	+Vo output voltage return.
8	+ SENSE	Senses the remote load high side. To be connected to pins 4,5 when remote sense is not used.
9	- SENSE	Senses the remote load return. To be connected to pins 6,7 when remote sense is not used.
10	ADJ	Adjust output voltage pin. A voltage generator between the ADJ. pin and -SENSE pin sets the Vo. When unconnected Vo is at nominal value (see fig. 2).

ADJUSTMENT OF THE OUTPUT VOLTAGE

The output voltage can be fixed following the indications given in fig. 2. The external reference voltage Vadj can be calculated using the following formula:

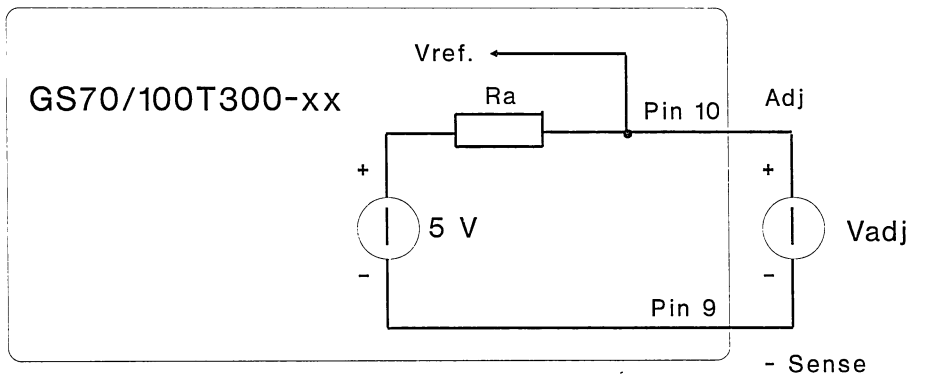
$$V_{adj} = 5 \cdot \frac{V_o}{V_{nom}}$$

The Vout and Vadj ranges are given in the following table:

Table 1: Output voltage generation with external voltage generator

Type	Nominal Output Voltage (V)	Output Voltage Range (V_{out})	External Voltage Generator allowed Range (V_{adj})
GS70T300-3.5	3.5	1.75 to 3.50	2.5 to 5.0
GS100T300-5	5.2	2.60 to 5.20	2.5 to 5.0
GS100T300-12	12.0	6.00 to 13.20	2.5 to 5.5
GS100T300-15	15.0	7.50 to 16.50	2.5 to 5.5
GS100T300-24	24.0	12.00 to 26.40	2.5 to 5.5
GS100T300-48	48.0	24.00 to 52.80	2.5 to 5.5

Figure 2. Output voltage adjustment



Safety approvals

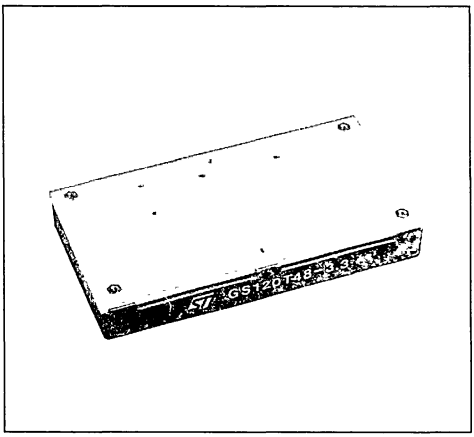
The converter is agency certified to the following safety requirements.

Agency	Requirements	License Number
UL	UL-STD-1950	E141284
TUV	EN 60950	R 9371740.1

® UL is a registered trademark of UNDERWRITERS LABORATORIES inc.
® TUV is a registered trademark of TUV Rheinland.

120W/175W DC-DC CONVERTERS FAMILY

Type	V_i	V_o	I_o
GS120T48-3.3 GS120T48-3.3E	38 to 60 V	3,35 V	35 A
GS175T48-5 GS175T48-5E	38 to 60 V	5,075 V	35 A
GS175T48-12 GS175T48-12E	38 to 60 V	12,0 V	15 A
GS175T48-15 GS175T48-15E	38 to 60 V	15,0 V	12 A



FEATURES

- UL, CSA, TUV approved
- High output power (up to 175W)
- High efficiency (82% typ. on GS175T48-5 module)
- Parallel operation with equal current sharing
- Synchronization pin
- Remote ON/OFF
- Remote load voltage sense compensation
- Output short-circuit protection
- Undervoltage lock-out
- Minimal overshoot during load transients
- Output overvoltage protection
- 500V_{DC} input to output isolation voltage
- Internal input and output filtering
- Softstart
- PCB or chassis mountable
- Optional additional finned heatsink
- Mechanical dimensions 125 • 66,5 • 19 (4,92 • 2,62 • 0,75)

DESCRIPTION

The GS120/175T48 family includes 120/175W DC-DC converters used to generate fixed isolated output voltages with an output current up to 35A from a wide range input voltage (38 to 60V).
The suffix E Identifies the metric threading on the planar heatsink (see fig. 1).

OPTION

Type Ordering Number	Description	Thermal Resistance	Dimensions L • W • H mm (inches)
HS01	Additional finned heatsink (See fig. 7)	2.8°C/W	125 • 66.5 • 15 (4.92 • 2.62 • 0.59)

GS120T48-3.3 ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_i	Input Voltage	V_o = 3.35V I_o = 0 to 35A (Operating Conditions)	38	48	60	VDC
V_{iuv}	Input Undervoltage Lockout	V_o = 3.35V I_o = 0 to 35A	32	34	36	VDC
I_i	Average Input Current	V_i = 0 to 60V I_o = 35A			4.2	A
I_{ipk}	Inrush Transient Peak Current	V_i = 60V I_o = 35A			0.2	A^2s
I_{ir}	Reflected Input Current	V_i = 38 to 60V BW = 5Hz to 20MHz I_o = 35A (See fig. 2)			20	mApp
V_{ien}	Enable Input Voltage	V_i = 38 to 60V I_o = 0 to 35A	0		1.2	V
I_{ien}	Enable Input Current	V_i = 38 to 60V I_o = 0 to 35A V_{ien} = 0V			-1	mA
V_{iinh}	Inhibit Voltage	V_i = 38 to 60V I_o = 0 to 35A Vien = open	8		18	V
P_i	Input Power	V_i = 38 to 60V I_o = 0A (No Load)		1.5	2	W
V_o	Total Output Voltage Regulation	V_i = 38 to 60V I_o = 0 to 35A	3.25	3.35	3.45	V
V_{ost}	Short-term Output Voltage Regulation	V_i = 38 to 60V I_o = 0 to 35A	3.30	3.35	3.40	V
V_{ots}	Total Static Tolerance	V_i = 38 to 60V I_o = 0 to 35A	3.28	3.35	3.42	V
V_{ol}	Output Overvoltage Limit Initiation	V_i = 38 to 60V I_o = 0 to 35A	4	4.5	5.2	VDC
V_{or}	Output Ripple Voltage	V_i = 38 to 60V I_o = 35A		20	30	mVpp
V_{on}	Output Noise Voltage	V_i = 38 to 60V I_o = 35A		50	80	mVpp
ΔV_o	Total Remote Sense Compensation	V_i = 38 to 60V			0.6	V
δV_o	Peak Load Transient Response	V_i = 48V δI_o = 5A slope = 0.1A/µs			60	mVp
I_o	Output Current	V_i = 38 to 60V V_o = 3.35V	0		35	A
I_{ol}	Overcurrent Limit Initiation	V_i = 48V	36		39	A
I_{osc}	Shortcircuit Output Current	V_i = 48V V_o = 0.2 to 0.5V			51	A
t_s	Load Transient Settling Time	V_i = 48V δI_o = 5A slope = 0.1A/µs			200	µs
t_{on}	Turn-on Time	V_i = 48V I_o = 35A V_{ien} = from high to low			5	ms
		V_i = 0 to 60V I_o = 35A V_{ien} = low	3		10	
V_{is}	Isolation Voltage		500			V
f_s	Switching Frequency	V_i = 38 to 60V I_o = 0 to 35A	160	175	200	kHz
η	Efficiency	V_i = 38 to 60V I_o = 35A	76	77		%
R_{th}	Thermal Resistance	Case to Ambient		5.2		°C/W
T_{cop}	Operating Case Temperature Range		−10		+85	°C
T_{stg}	Storage Temperature Range		−40		+105	°C

GS175T48-5 ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_i	Input Voltage	V_o = 5.075V I_o = 0 to 35A (Operating Conditions)	38	48	60	VDC
V_{iuv}	Input Undervoltage Lockout	V_o = 5.075V I_o = 0 to 35A	32	34	36	VDC
I_i	Average Input Current	V_i = 0 to 60V I_o = 35A			6.1	A
I_{ipk}	Inrush Transient Peak Current	V_i = 60V I_o = 35A			0.2	A^2s
I_{ir}	Reflected Input Current	V_i = 38 to 60V BW = 5Hz to 20MHz I_o = 35A (See fig. 2)			30	mApp
V_{ien}	Enable Input Voltage	V_i = 38 to 60V I_o = 0 to 35A	0		1.2	V
I_{ien}	Enable Input Current	V_i = 38 to 60V I_o = 0 to 35A V_{ien} = 0V			-1	mA
V_{iinh}	Inhibit Voltage	V_i = 38 to 60V I_o = 0 to 35A V_{ien} = open	8		18	V
P_i	Input Power	V_i = 38 to 60V I_o = 0A (No Load)		1.5	2	W
V_o	Total Output Voltage Regulation	V_i = 38 to 60V I_o = 0 to 35A	4.94	5.075	5.21	V
V_{ost}	Short-term Output Voltage Regulation	V_i = 38 to 60V I_o = 0 to 35A	5.002	5.075	5.148	V
V_{ots}	Total Static Tolerance	V_i = 38 to 60V I_o = 0 to 35A	4.97	5.075	5.18	V
V_{ol}	Output Overvoltage Limit Initiation	V_i = 38 to 60V I_o = 0 to 35A	6	6.3	7	VDC
V_{or}	Output Ripple Voltage	V_i = 38 to 60V I_o = 35A		20	30	mVpp
V_{on}	Output Noise Voltage	V_i = 38 to 60V I_o = 35A		50	80	mVpp
ΔV_o	Total Remote Sense Compensation	V_i = 38 to 60V			0.6	V
δV_o	Peak Load Transient Response	V_i = 48V δI_o = 5A slope = 0.1A/µs			100	mVp
I_o	Output Current	V_i = 38 to 60V V_o = 5.075V	0		35	A
I_{ol}	Overcurrent Limit Initiation	V_i = 48V	36		39	A
I_{osc}	Shortcircuit Output Current	V_i = 48V V_o = 0.2 to 0.5V			51	A
t_s	Load Transient Settling Time	V_i = 48V δI_o = 5A slope = 0.1A/µs			250	µs
t_{on}	Turn-on Time	V_i = 48V I_o = 35A V_{ien} = from high to low			5	ms
		V_i = 0 to 60V I_o = 35A V_{ien} = low	3		10	
V_{is}	Isolation Voltage		500			V
f_s	Switching Frequency	V_i = 38 to 60V I_o = 0 to 35A	160	175	200	kHz
η	Efficiency	V_i = 38 to 60V I_o = 35A	81	82		%
R_{th}	Thermal Resistance	Case to Ambient		5.2		°C/W
T_{cop}	Operating Case Temperature Range		– 10		+85	°C
T_{stg}	Storage Temperature Range		– 40		+105	°C

GS175T48-12 ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

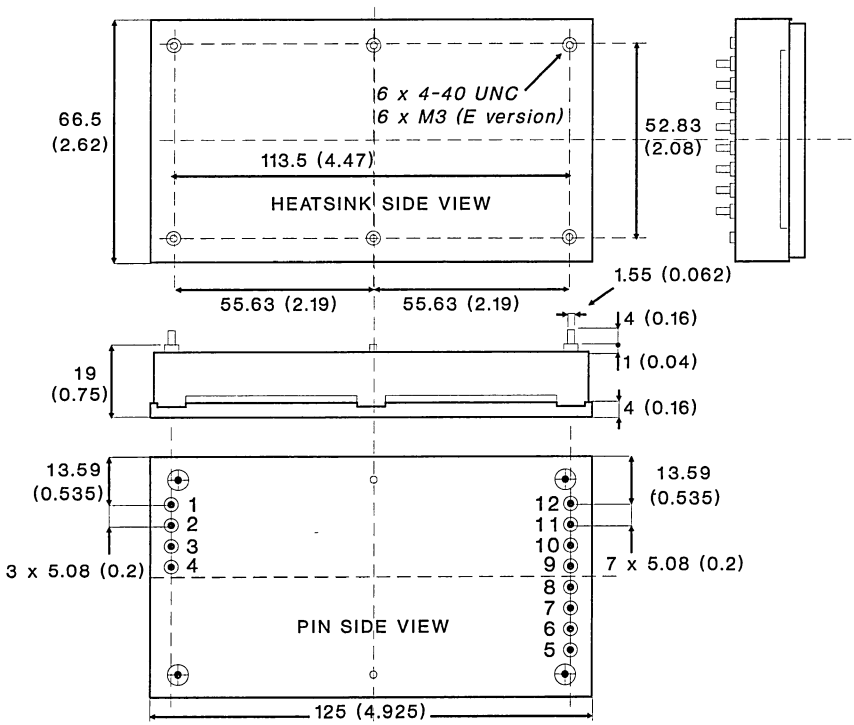
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_i	Input Voltage	V_O = 12V I_O = 0 to 15A (Operating Conditions)	38	48	60	VDC
V_{iuv}	Input Undervoltage Lockout	V_O = 12V I_O = 0 to 15A	32	34	36	VDC
I_i	Average Input Current	V_i = 0 to 60V I_O = 15A			5.5	A
I_{ipk}	Inrush Transient Peak Current	V_i = 60V I_O = 15A			0.2	A^2s
I_{ir}	Reflected Input Current	V_i = 38 to 60V BW = 5Hz to 20MHz I_O = 15A (See fig. 2)			20	mApp
V_{ien}	Enable Input Voltage	V_i = 38 to 60V I_O = 0 to 15A	0		1.2	V
I_{ien}	Enable Input Current	V_i = 38 to 60V I_O = 0 to 15A V_{ien} = 0V			-1	mA
V_{iinh}	Inhibit Voltage	V_i = 38 to 60V I_O = 0 to 15A V_{ien} = open	8		18	V
P_I	Input Power	V_i = 38 to 60V I_O = 0A (No Load)		1.5	2	W
V_O	Total Output Voltage Regulation	V_i = 38 to 60V I_O = 0 to 15A	11.4	12.0	12.6	V
V_{ost}	Short-term Output Voltage Regulation	V_i = 38 to 60V I_O = 0 to 15A	11.76	12.0	12.24	V
V_{ots}	Total Static Tolerance	V_i = 38 to 60V I_O = 0 to 15A	11.64	12.0	12.36	V
V_{ol}	Output Overvoltage Limit Initiation	V_i = 38 to 60V I_O = 0 to 15A	13.2	14	15	VDC
V_{or}	Output Ripple Voltage	V_i = 38 to 60V I_O = 15A		35	70	mVpp
V_{on}	Output Noise Voltage	V_i = 38 to 60V I_O = 15A		60	120	mVpp
ΔV_O	Total Remote Sense Compensation	V_i = 38 to 60V			0.6	V
δV_O	Peak Load Transient Response	V_i = 48V δI_O = 3A slope = 0.2A/µs			200	mVp
I_o	Output Current	V_i = 38 to 60V V_O = 12V	0		15	A
I_{ol}	Overcurrent Limit Initiation	V_i = 48V	16		19	A
I_{osc}	Shortcircuit Output Current	V_i = 48V			25	A
t_s	Load Transient Setting Time	V_i = 48V δI_O = 3A slope = 0.2A/µs			300	µs
t_{on}	Turn-on Time	V_i = 48V I_O = 15A V_{ien} = from high to low			5	ms
		V_i = 0 to 60V I_O = 15A V_{ien} = low	3		10	
V_{is}	Isolation Voltage		500			V
f_s	Switching Frequency	V_i = 38 to 60V I_O = 0 to 15A	160	175	200	kHz
η	Efficiency	V_i = 38 to 60V I_O = 15A	84	86		%
R_{th}	Thermal Resistance	Case to Ambient		5.2		°C/W
T_{cop}	Operating Case Temperature Range		−10		+85	°C
T_{stg}	Storage Temperature Range		−40		+105	°C

GS175T48-15 ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_i	Input Voltage	V_O = 15V I_O = 0 to 12A (Operating Conditions)	38	48	60	VDC
V_{iuv}	Input Undervoltage Lockout	V_O = 15V I_O = 0 to 12A	32	34	36	VDC
I_i	Average Input Current	V_i = 0 to 60V I_O = 12A			5.5	A
I_{ipk}	Inrush Transient Peak Current	V_i = 60V I_O = 12A			0.2	A^2s
I_{ir}	Reflected Input Current	V_i = 38 to 60V I_O = 12A			20	mApp
V_{ien}	Enable Input Voltage	V_i = 38 to 60V I_O = 0 to 12A	0		1.2	V
I_{ien}	Enable Input Current	V_i = 38 to 60V I_O = 0 to 12A V_{ien} = 0V			-1	mA
V_{iinh}	Inhibit Voltage	V_i = 38 to 60V I_O = 0 to 12A V_{ien} = open	8		18	V
P_i	Input Power	V_i = 38 to 60V I_O = 0A (No Load)		1.5	2	W
V_O	Total Output Voltage Regulation	V_i = 38 to 60V I_O = 0 to 12A	14.25	15.0	15.75	V
V_{ost}	Short-term Output Voltage Regulation	V_i = 38 to 60V I_O = 0 to 12A	14.7	15.0	15.3	V
V_{ots}	Total Static Tolerance	V_i = 38 to 60V I_O = 0 to 12A	14.55	15.0	15.45	V
V_{ol}	Output Overvoltage Limit Initiation	V_i = 38 to 60V I_O = 0 to 12A	16.5	17	18	VDC
V_{or}	Output Ripple Voltage	V_i = 38 to 60V I_O = 12A		45	90	mVpp
V_{on}	Output Noise Voltage	V_i = 38 to 60V I_O = 12A		75	150	mVpp
ΔV_O	Total Remote Sense Compensation	V_i = 38 to 60V			0.6	V
δV_O	Peak Load Transient Response	V_i = 48V δI_O = 3A slope = 0.2A/µs			200	mVp
I_O	Output Current	V_i = 38 to 60V V_O = 15V	0		12	A
I_{ol}	Overcurrent Limit Initiation	V_i = 48V	13		16	A
I_{osc}	Shortcircuit Output Current	V_i = 48V V_O = 0.2 to 0.5V			21	A
t_s	Load Transient Settling Time	V_i = 48V δI_O = 3A slope = 0.2A/µs			300	µs
t_{on}	Turn-on Time	V_i = 48V I_O = 12A V_{ien} = from high to low			5	ms
		V_i = 0 to 60V I_O = 12A V_{ien} = low	3		10	
V_{is}	Isolation Voltage		500			V
f_s	Switching Frequency	V_i = 38 to 60V I_O = 0 to 12A	160	175	200	kHz
η	Efficiency	V_i = 38 to 60V I_O = 12A	86	88		%
R_{th}	Thermal Resistance	Case to Ambient		5.2		°C/W
T_{cop}	Operating Case Temperature Range		– 10		+85	°C
T_{stg}	Storage Temperature Range		– 40		+105	°C

CONNECTION DIAGRAM AND MECHANICAL DATA

Figure 1.



Package T. Dimensions in mm (inches).

PIN DESCRIPTION

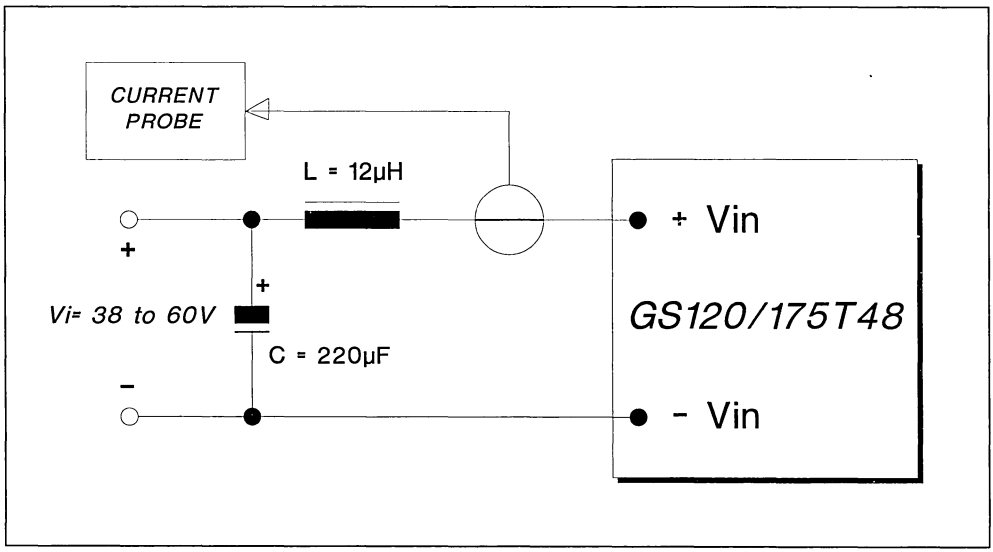
Pin	Function	Description
1	- IN	Negative input voltage.
2	+ IN	Positive input voltage. Unregulated input voltage (typically 48V) must be applied between pin 1-2.
3	ON/OFF	The converter is ON (Enable) when the voltage applied to this pin with reference to pin 1 is lower than 1.2V (see Vien). The converter is OFF (Inhibit) for a control voltage in the range of 8 to 18V. When the pin is unconnected the converter is OFF (Inhibit).
4	CASE	Case connection pin.
5	SYNC	Synchronization pin. See figures 3, 4, 5, 6. Open when not used.
6	PARALLEL	Parallel output. See figures 3, 4, 5, 6. Open when not used.
7	+ SENSE	Senses the remote load high side. To be connected to pin 11,12 when remote sense is not used.
8	- SENSE	Senses the remote load return. To be connected to pin 9,10 when remote sense is not used. In parallel configuration, take care to connect all -S pins together (see figures 3,4,5,6).
9,10	- OUT	Fixed output voltage return.
11,12	+ OUT	Fixed output voltage.

USER NOTES

Reflected Input Current

The reflected input current measurement (Iir, see Electrical Characteristics) is performed according to the test set-up of fig. 2.

Figure 2.



Softstart

To avoid heavy inrush current the output voltage rise time is 10ms maximum in any condition of load.

Remote Sensing

The remote voltage sense compensation range is for a total drop of 0.6V equally shared between the load connecting wires.

It is a good practice to shield the sensing wires to avoid oscillations.

See the connection diagram on figures 3, 4, 5, 6.

Remote ON/OFF

The module is controlled by the voltage applied between the ON/OFF pin and -IN pin.

The converter is ON (Enable) when the voltage applied is lower than 1.2 V (see Vien on Electrical Characteristics).

The converter is OFF (Inhibit) for a control voltage in the range of 8 to 18V (see Viinh).

When the pin is unconnected the converter is OFF. Maximum sinking current is 1mA.

Module Protection

The module is protected against occasional and permanent shortcircuits of the output pins to ground, as well as against output current overload. It uses a current limiting protection circuitry, avoiding latch-up problems with certain type of loads.

A crowbar output overvoltage protection is activated when the output voltage exceeds the specified values (see Electrical Characteristics).

Parallel Operation

To increase available output regulated power, the module features the parallel connection possibility with equal current sharing and maximum deviation of 10% (two modules in parallel).

See the connection diagram on figures 3, 4, 5, 6.

Figure 3.

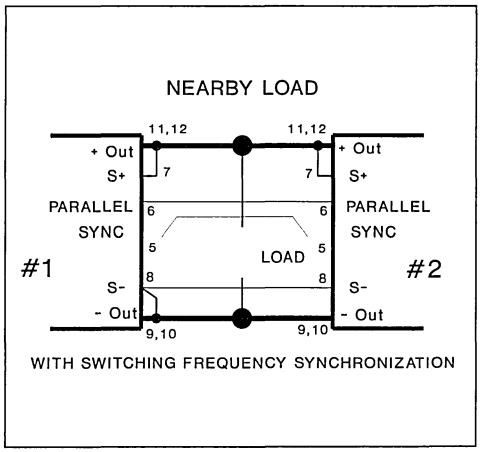


Figure 4.

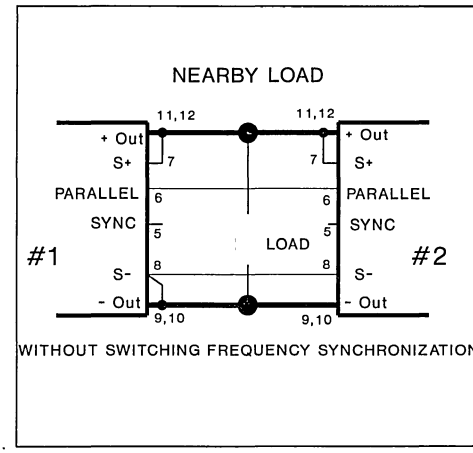


Figure 5.

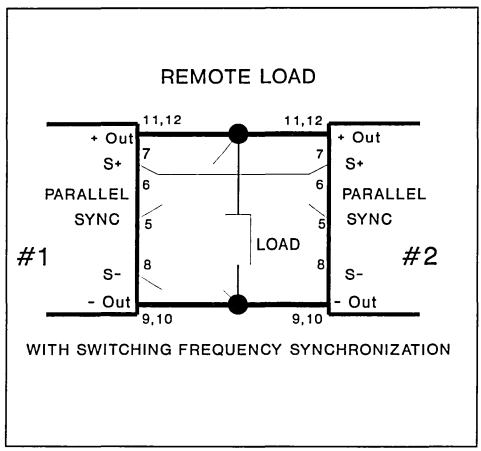
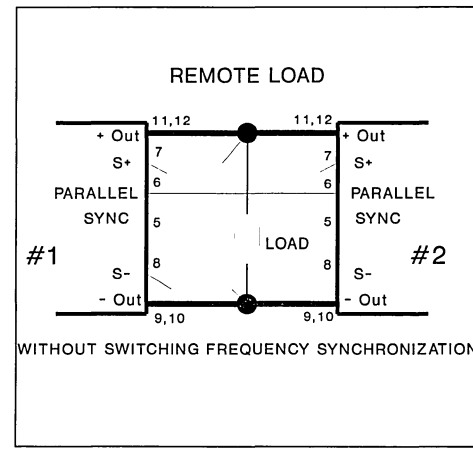


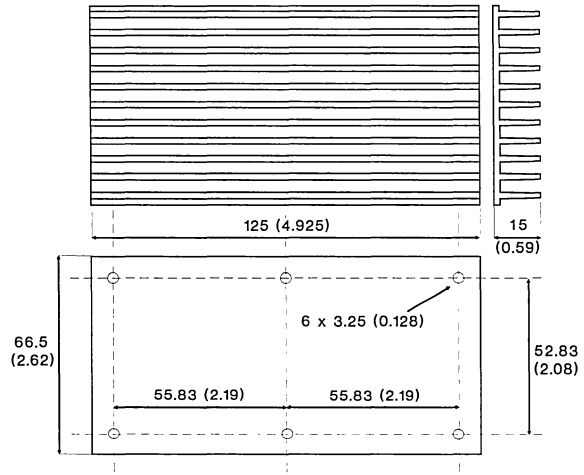
Figure 6.



Finned heatsink option

An additional finned heatsink is available (type ordering number HS01) to allow the user to decrease the total thermal resistance of the module to a typical value of 2.8 °C/W. The heatsink is suitable both for standard (4-40 UNC threading) and E version (M3 threading); screw length in the range of 6 to 8 mm (0.24 to 0.32"). See fig. 7.

Figure 7. - HS01 Heatsink.



Dimensions in mm (inches).

Thermal Characteristics

Following figures show the behaviour at still air and forced ventilation operation of the GS175T48-5 module (typical efficiency 82%) without (fig. 8) and with the additional finned HS01 heatsink (fig. 9)

Figure 8. - GS175T48-5 with stadard flat heatsink.

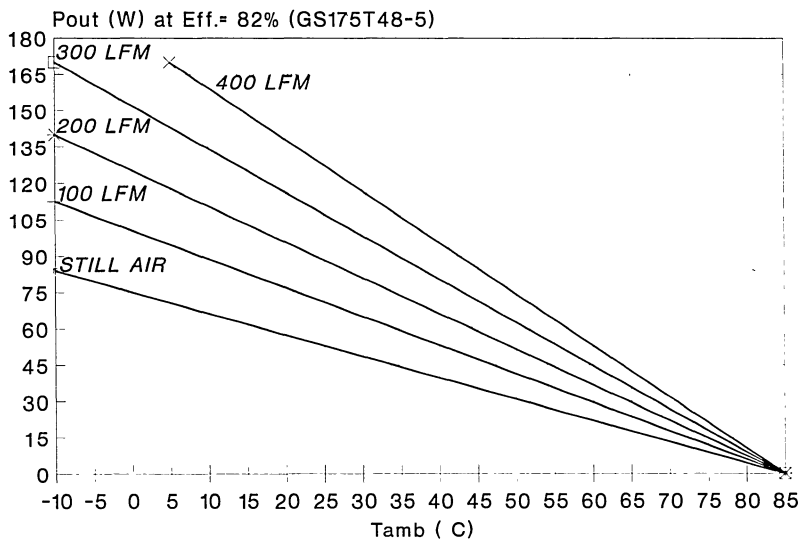
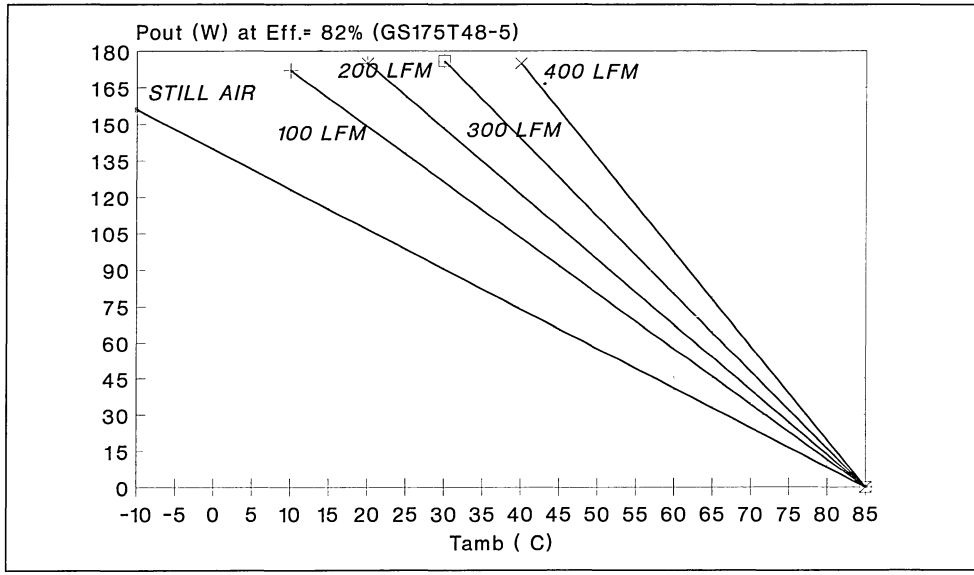


Figure 9. - GS175T48-5 with additional HS01 finned heatsink



Safety approvals

The converter is agency certified to the following safety requirements.

Agency	Requirements	License Number
UL	UL-STD-1950	E141284
CSA	CSA-STD-C22.2 No.234 (level 3)	LR 99794-2
TUV	EN 60950 DIN VDE 0805	R 9272137

® UL is a registered trademark of UNDERWRITERS LABORATORIES inc.
® CSA is a registered trademark of CANADIAN STANDARDS ASSOCIATION.
® TUV is a registered trademark of TUV Rheinland.

SGS-THOMSON MICROELECTRONICS

GS300T48-5

300W DC-DC CONVERTER

Type	V_i	V_o	I_o
GS300T48-5	38 to 60 V	5,075 V	60 A

FEATURES

- Very high output power (300W)
- High efficiency (80% min.)
- Parallel operation with current sharing
- Synchronization pin
- Remote ON/OFF
- Remote load voltage sense compensation
- Output short-circuit protection
- Output overvoltage protection
- Thermal protection
- Undervoltage lock-out
- Minimal overshoot during load transients
- 500 V_{DC} input to output isolation
- Internal input and output filtering
- Softstart
- PCB or chassis mountable

DESCRIPTION

The GS300T48-5 is a 300W DC-DC converters used to generate a 5.075V isolated output with a current of 60A from a wide range input voltage (38 to 60V).

SELECTION GUIDE

Type Ordering Number	Input Voltage (V)	Output Voltage (V)	Output Current (A)	Dimensions L • W • H mm (inches)
GS300T48-5 GS300T48-5E	38 to 60	5.075	60	125 • 66.5 • 20 (4.92 • 2.62 • 0.79) **The suffix E identifies the metric threading on the planar heatsink (see fig. 1).**

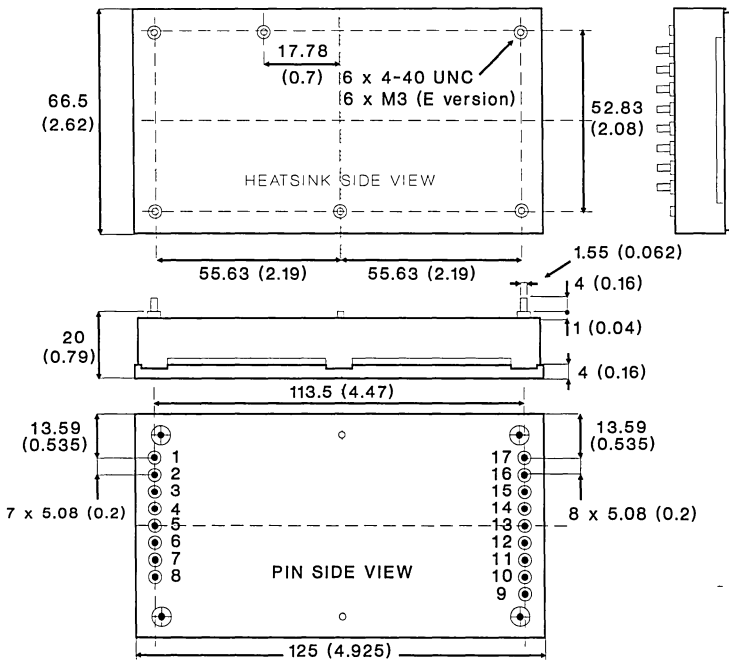
ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_i	Input Voltage	V_o = 5.075V I_o = 0 to 30A (Operating Conditions)	38	48	60	VDC
V_{iuv}	Input Undervoltage Lockout	I_o = 0 to 60A	29		36	V
I_i	Average Input Current	V_i = 48V I_o = 60A			7.8	A
I_{ipk}	Inrush Transient Peak Current	V_i = 60V I_o = 60A			0.3	A^2s
I_{ir}	Reflected Input Current	V_i = 48V I_o = 60A BW = 5Hz to 20MHz (see fig. 2)			30	mApp
V_{ien}	Enable Input Voltage	V_i = 38 to 60V I_o = 0 to 60A	0		1.2	V
I_{ien}	Enable Input Current	V_i = 38 to 60V I_o = 0 to 60A V_{ien} = 0V			– 1	mA
V_{iinh}	Max Inhibit Voltage	V_i = 38 to 60V I_o = 0 to 60A V_{ien} = open	8		18	V
P_i	Input Power	V_i = 38 to 60V I_o = 0A (No Load)		1.5	2	W
V_o	Total Output Voltage Regulation	V_i = 38 to 60V I_o = 0 to 60A	4.490	5.075	5.210	V
V_{ost}	Short-term Output Voltage Regulation	V_i = 38 to 60V I_o = 0 to 60A	5.002	5.075	5.148	V
V_{ots}	Total Static Output Voltage Regulation	V_i = 38 to 60V I_o = 0 to 60A	4.970	5.075	5.180	V
V_{ol}	Output Overvoltage Limit Initiation	V_i = 38 to 60V I_o = 0 to 60A		6.3		V
V_{or}	Output Ripple Voltage	V_i = 38 to 60V I_o = 60A BW = 0 to 20 Mhz			50	mVpp
V_{on}	Output Noise Voltage	V_i = 38 to 60V I_o = 60A BW = 0 to 20 Mhz			100	mVpp
ΔV_o	Total Remote Sense Compensation	V_i = 38 to 60V			0.6	V
δV_o	Peak Load Transient Response	V_i = 48V δI_o = 10A slope = 0.1A/µs			100	mVp
I_o	Output Current	V_i = 38 to 60V V_o = 5V	0		60	A
I_{ol}	Overcurrent Limit Initiation	V_i = 48V		63		A
I_{osc}	Shortcircuit Output Current	V_i = 48V		69		A
t_s	Load Transient Setting Time	V_i = 48V δI_o = 10A slope = 0.1A/µs			250	µs
t_{on}	Turn-on Time	V_i = 38 to 60V I_o = 0 to 60A V_{ien} = from high to low			10	ms
		V_i = 0 to 60V I_o = 0 to 60A V_{ien} = low			10	
V_{is}	Isolation Voltage		500			V
f_s	Switching Frequency	V_i = 38 to 60V I_o = 0 to 60A	160	180	200	kHz
η	Efficiency	V_i = 38 to 60V I_o = 60A	80	81		%
R_{th}	Thermal Resistance	Case to Ambient		5.2		°C/W
T_{cop}	Operating Case Temperature Range*		0		+70	°C
T_{stg}	Storage Temperature Range		– 40		+105	°C

* Thermal intervention @ T_{cop} = 85°C

CONNECTION DIAGRAM AND MECHANICAL DATA

Figure 1.



Package U. Dimensions in mm (inches)

PIN DESCRIPTION

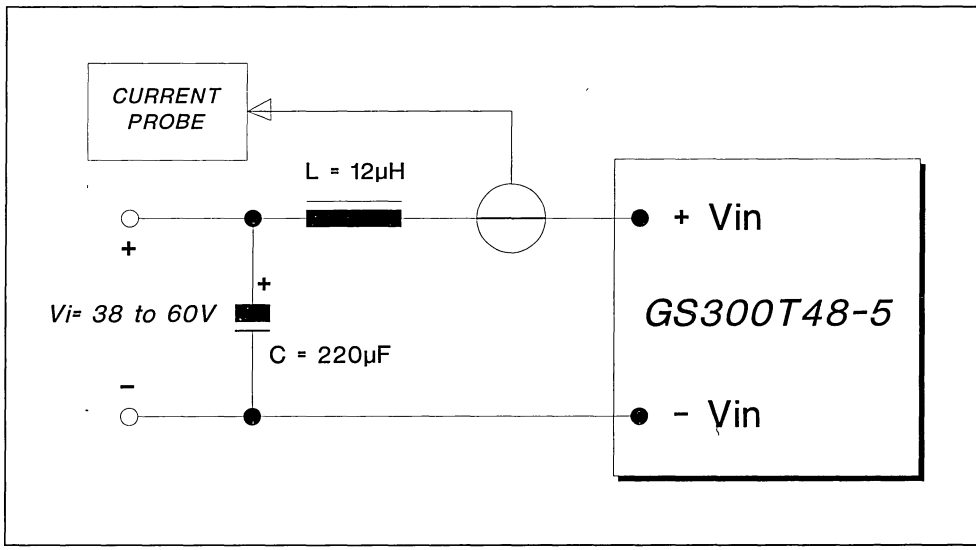
Pin	Function	Description
1,2	- Vin	Negative input voltage.
3,4	+ Vin	Positive input voltage. Unregulated input voltage (typically 48V) must be applied between pin 1,2-3,4.
5	SYNC	Synchronization pin. See figures 3, 4, 5, 6. Open when not used.
6	PARALLEL	Parallel output. See figures 3, 4, 5, 6. Open when not used.
7	ON/OFF	The converter is ON (Enable) when the voltage applied to this pin with reference to pin 1,2 is lower than 1,2 V (see Vien). The converter is OFF (Inhibit) for a control voltage in the range of 8 to 18V. When the pin is unconnected the converter is OFF (Inhibit).
8	CASE	Case connection pin
9	+ SENSE	Senses the remote load high side. To be connected to pin 15,16,17 when remote sense is not used.
10	- SENSE	Senses the remote load return. To be connected to pin 11,12,13,14 when remote sense is not used. In parallel configuration, take care to connect all -SENSE pins together (see figures 3,4,5,6).
11,12, 13,14	- OUT	-5V voltage return.
15,16, 17	+ OUT	+5V output voltage.

USER NOTES

Reflected Input Current

The reflected input current measurement (Iir, see Electrical Characteristics) is performed according to the test set-up of fig. 2.

Figure 2.



Softstart

To avoid heavy inrush current the output voltage rise time is 10ms maximum in any condition of load.

Remote Sensing

The remote voltage sense compensation range is for a total drop of 0.6V equally shared between the load connecting wires.

It is a good practice to shield the sensing wires to avoid osciliations.

See the connection diagram on figures 3, 4, 5, 6.

Remote ON/OFF

The module is controlled by the voltage applied between the ON/OFF pin and -IN pin.

The converter is ON (Enable) when the voltage applied is lower than 1.2 V (see Vien on Electrical Characteristics).

The converter is OFF (Inhibit) for a control voltage in the range of 8 to 18V (see Viinh).

When the pin is unconnected the converter is OFF. Maximum sinking current is 1mA.

Module Protection

The module is protected against occasional and permanent shortcircuits of the output pins to ground, as well as against output current overload. It uses a current limiting protection circuitry, avoiding latch-up problems with certain type of loads.

A latching crowbar output overvoltage protection is activated when the output voltage exceeds the typical value of 6.3V (see Electrical Characteristics). A thermal non-latching protection disables the module whenever the heatsink temperature reaches about 85°C.

Parallel Operation

To increase available output regulated power, the module features the parallel connection possibility with equal current sharing and maximum deviation of 10% (two modules in parallel).

See the connection diagram on figures 3, 4, 5, 6.

Figure 3.

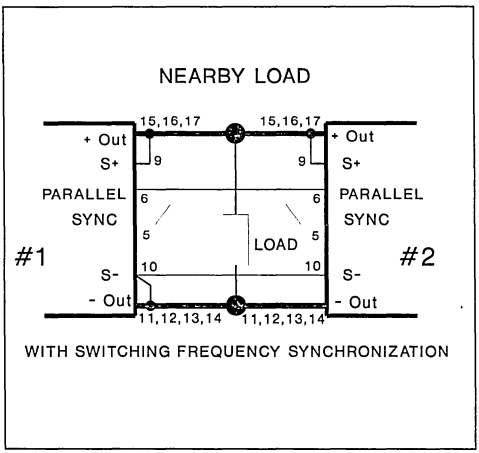


Figure 4.

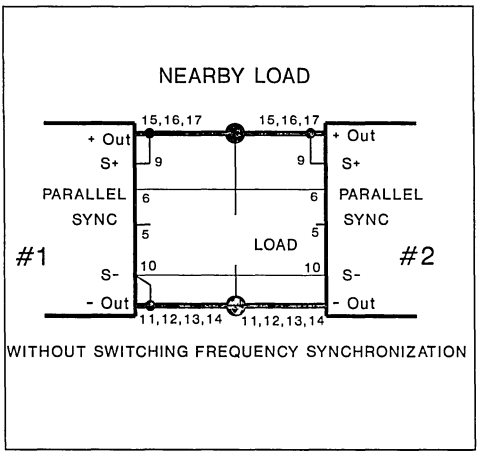


Figure 5.

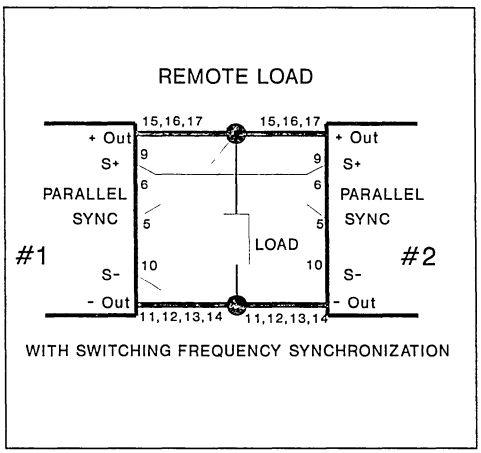
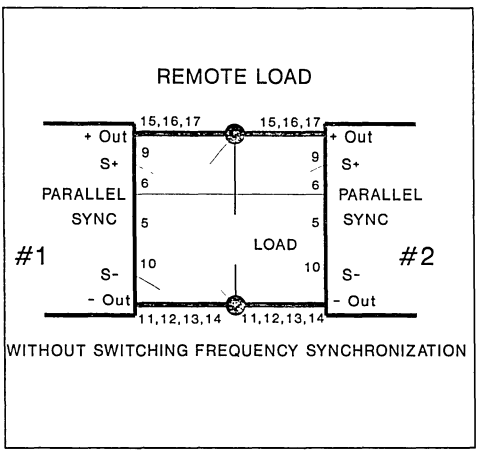


Figure 6.



Thermal Characteristics

The case-to-ambient thermal resistance of the GS300T48-5 module is 5.2°C/W typical. It may be decreased, improving the convection cooling, by mounting an external heatsink to the top of the unit heatsink.

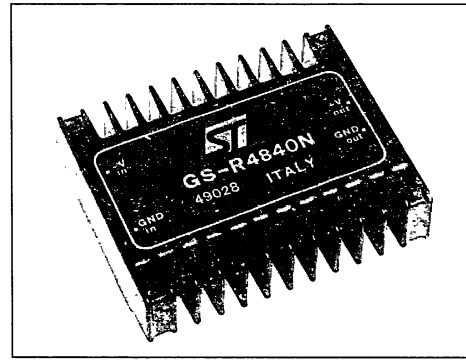
Six threaded holes, # 4-40 UNC on the standard or # M3 on the E version, 5 mm (0,2") maximum deep, are provided for this purpose (see fig. 1).

SGS-THOMSON MICROELECTRONICS

GS-R4840N

44W NEGATIVE SWITCHING REGULATOR

Type	V_i	V_o	I_o
GS-R4840N	– 43 to – 60 V	– 40 V	1,08 A



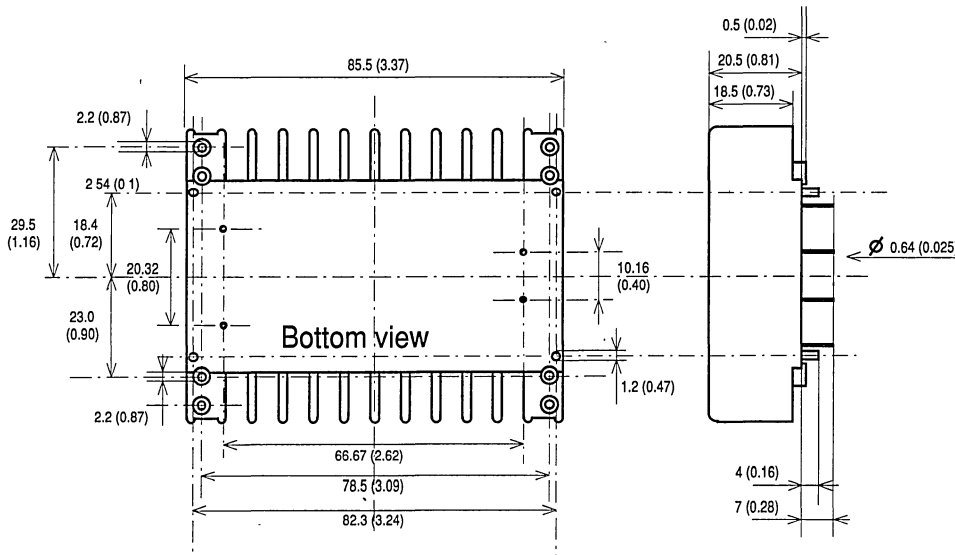
DESCRIPTION

The GS-R4840N is a negative input, negative output switching voltage regulator that can provide up to 44W output power without input to output isolation.

ELECTRICAL CHARACTERISTICS ($T_{amb.}$= 25° C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_i	Input Voltage	I_O = 1.08A	– 43	– 48	– 60	V
V_{ni}	Input noise (CCITTP53)	V_i = – 48V I_O = – 1A			1	mV
I_i	Input Current	V_i = – 48V I_O = – 1.08A			– 1	A
V_o	Output Voltage	V_i = – 43 to – 60V I_O = 0 to – 1.08A	– 38.5	– 40.5	– 42.5	V
V_{or}	Output Ripple Voltage	V_i = – 48V I_O = – 1.08A			100	mVpp
V_{on}	Output noise Voltage (CCITTP53)	V_i = – 48V I_O = – 1A			1	mV
I_{osc}	Output Current Limit	V_i = – 48V		– 1.6		A
f_s	Switching Frequency			50		kHz
η	Efficiency	V_i = – 48V I_O = – 1.08A		93		%
Top	Operating Case Temperature Range		0		+70	°C
Tstg	Storage Temperature Range		– 20		+85	°C

CONNECTION DIAGRAM AND MECHANICAL DATA



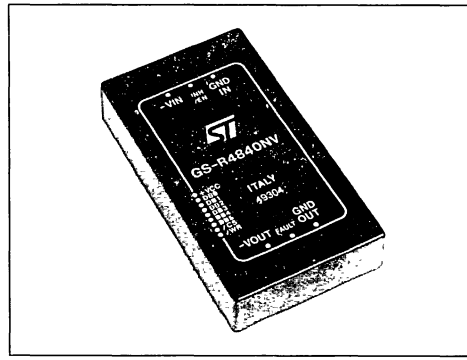
Package H. Dimensions in mm.
Note: Pins 1 and 4 are internally connected

SGS-THOMSON MICROELECTRONICS

GS-R4840NV

36 W NEGATIVE SWITCHING REGULATOR

Type	V_I	V_O	I_O
GS-R4840NV	– 40 to – 60 V	–22 to –60 V	– 600 mA



FEATURES

- Digital input for voltage selection
- Short-circuit protection
- Overvoltage protection
- Thermal protection
- Softstart
- Fault signal indication output
- High efficiency (>80%)

DESCRIPTION

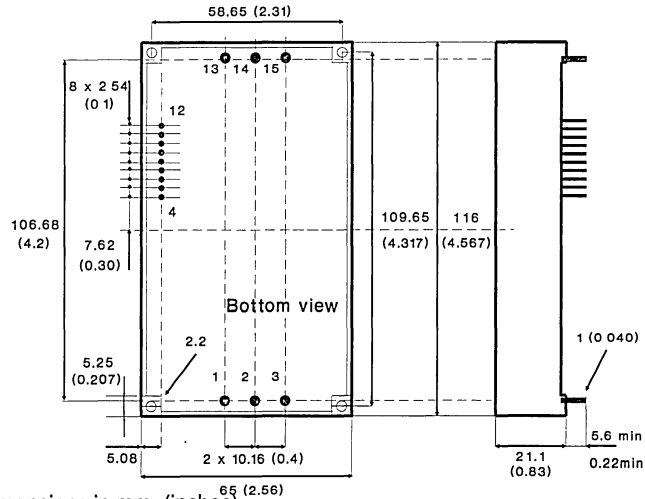
The GS-R4840NV is a negative input, negative output switching voltage regulator that provides up to 36W output power without input-output isolation.

The output voltage is programmable by input logic signals that allow 64 steps (6 bit) of regulated output, from –22 to –60V.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_i	Input Voltage	V_O = – 22 to – 60V I_O = – 10 to – 600mA	– 40	– 48	– 60	V
V_{ir}	Input Ripple Voltage	V_i = – 40 to – 60V I_O = – 600mA			20	mVpp
V_o	Output Voltage	V_i = – 40 to – 60V I_O = – 10 to – 600mA	– 22		– 60	V
V_{or}	Output Ripple Voltage	V_O = – 22 to – 60V I_O = – 600mA		4	10	mVpp
V_{oov}	Output Overvoltage Protection	V_i = – 40 to – 60V I_O = – 10 to – 600mA	Vo+5%		Vo+10%	V
I_o	Output Current	V_i = – 40 to – 60V V_O = – 22 to – 60V	– 10		– 600	mA
I_{ol}	Current Limit	V_i = – 40 to – 60V Overload Condition			– 900	mA
I_{osc}	Output Average Short Circ. Current	V_i = – 40 to – 60V			– 80	mA
f_s	Switching Frequency			100		kHz
η	Efficiency	V_i = – 48V I_O = – 600mA V_O = – 48V	80	82		%
R_{th}	Thermal Resistance	Case to Ambient		4		°C/W
T_{cop}	Operating Case Temperature Range		0		+85	°C
T_{stg}	Storage Temperature Range		– 20		+105	°C

CONNECTION DIAGRAM AND MECHANICAL DATA



Package F. Dimensions in mm. (inches)

PIN DESCRIPTION

Pin	Function	Description
1	-Vin	Negative input voltage.
2	Inhibit/ $\overline{\text{Enable}}$	Remote Inhibit/Enable logically compatible with CMOS or open collector TTL. The converter is OFF (Inhibit) when this pin is unconnected or the voltage applied is in the range of 2 to 5V (referred to GND). The converter is ON (Enable) for a control voltage in the range of 0 to 0.8V maximum.
3	GND IN	Return for input voltage source and +5V logic supply voltage. Internally connected to pin 15.
4	+5V IN	+5V logic supply voltage. Maximum voltage must not exceed 7V.
5	DB0	Data bit 0 (LSB).
6	DB1	Data bit 1.
7	DB2	Data bit 2.
8	DB3	Data bit 3.
9	DB4	Data bit 4.
10	DB5	Data bit 5 (MSB).
11	$\overline{\text{CS}}$	Chip select. An active low input control which is the device enable input terminal.
12	$\overline{\text{WR}}$	Write control. An active low control which enables the microprocessor to write data to the DAC.
13	-Vout	Negative output voltage.
14	FAULT	FAULT indication output (referred to GND). The FAULT signal is high (TTL compatible level) when: - the INHIBIT is ON (high) - an output overload is present (Vo < 18V typ.) - an overtemperature is present - an overvoltage is present (Vo > Vo+5%)
15	GND OUT	Return for output voltage source. Internally connected to pin 3.

Note: Case internally connected to Ground.

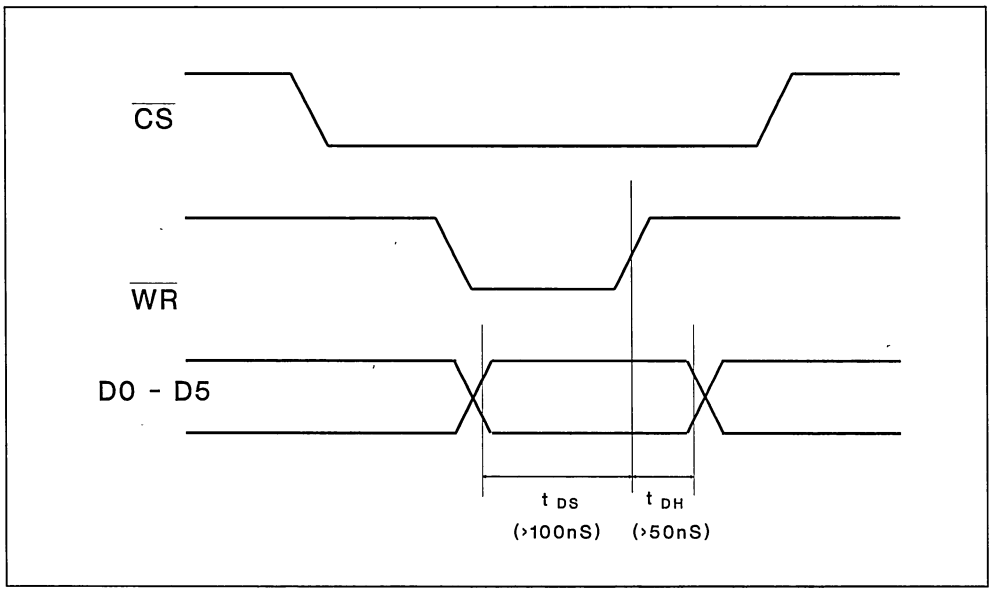
USER NOTES

Digital Information

The GS-R4840NV accepts 6 bit binary at the data inputs DB0 to DB5. Data are transferred when CS is low and during the rising edge of WR signal.

t_{DS} and t_{DH} have to be 100ns and 50ns minimum respectively (see fig. 1).

Figure 1 - Signals Timing.



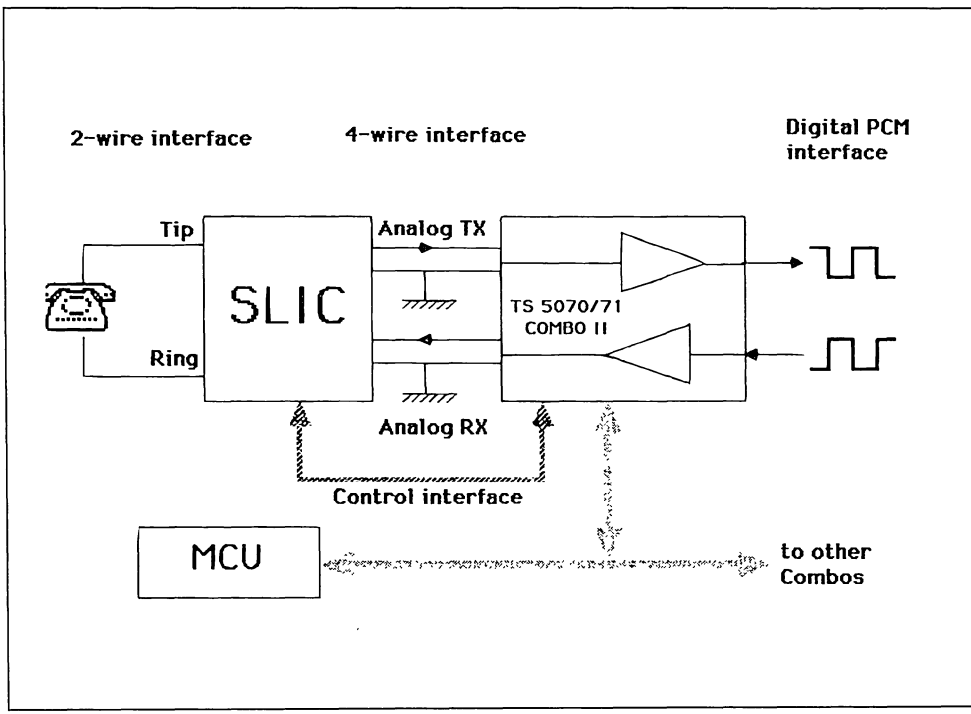
APPLICATION NOTES

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TS5070/5071 COMBO II PROGRAMMING AND HYBRID BALANCING WITH SOLID-STATE SLICs

By Bernard SABY



1. INTRODUCTION

The TS5070/71 COMBO II is a programmable Codec/Filter circuit especially developped for the subscriber line card applications in a central office or PABX.

Compared to the currently used first generation cofidecs, such as : ETC 5054/57, M5913/14, ... the TS5070/71 COMBO II provides two major enhancements :

1) Several functions, previously assumed by external components, are now "on-chip" with the TS5070/71 COMBO II. Such features include :

- Gain adjustable transmit and receive amplifiers (25.4dB range).
- Time-slot assignment (one out of 64).
- PCM port assignment (2 transmit and receive ports, on the TS5070).
- Analog and digital loopback, for test mode.
- Hybrid balance cancellation filter.

2) All these added functions are programmed by the card-controller, through a 4-wire serial bus. Other programmable features include :

- A-law or μ-law selection.
- European (2.048 or 4.096MHz) or North American master clock (1.536 or 1.544MHz).
- 6 input/output interface latches (5 on the TS5071). These latches facilitate the logical interface with a transformer or an electronic parallel control SLIC, such as L3000N+L3092 kit or L303X monochip SLIC or any other function.

The programmable features of the TS5070/71 COMBO II simplify the design of the line card and provide more flexibility, especially when the same module must operate in different countries and must deal with the various telecom administrations requirements : only a few external components must be changed in the SLIC and the major adaptations are assumed by the TS5070/71 COMBO II programming.

As an example, this note describes briefly the design of a line card module, using a TS5070/71 COMBO II with a transformer SLIC and the solid state SLICs from SGS-THOMSON Microelectronics L3000N/L3092 kit and the L303X monochip SLIC. The adaptation of the line card kit to several telecom administrations requirements is also discussed..

The TS5071 basic version of the COMBO II is packaged in a 20-pin DIL case. The TS5070 is a full feature version available in a 28-pin PLCC or 28-pin DIP package :

- Interface latch pin IL5 is bonded out : 6 input/output latches are available.
- Programmable ports : DX1, DR1, and TSX1 are bonded out : 2 PCM port are available.
- Serial interface : CI and CO are separated.
- Clock inputs : BCLK and MCLK are not bonded together, providing two separate clock inputs.

2. SCHEMATIC DIAGRAM

TRANSFORMER SLIC

The design of the transformer is greatly simplified, due to the on-chip hybrid balance cancellation filter : Only one single secondary winding is required (see fig. 1). ZT is the line termination impedance as reflected through the transformer (impedance measured between Tip and Ring) : its value is determined by the administration requirements and the transformer characteristics.

ZT provides an echo : a part of the receive signal on VFRO is injected into the transmit path VFXI. The internal hybrid balance filter is designed in order to replicate the echo path, and thus to cancel it.

In this application, the input/output latches are used as relay drivers (buffered through an external transistor) : ring relay, test relays... and line monitoring : off-hook detection, ground key detection. Thus, the card controller can monitor the whole line card module through the unique control port of the TS5070/71 COMBO II.

When the CS pin is held high by the card controller (chip disabled), the CO output of the TS5070 is placed in a high impedance state, allowing several TS5070/71 COMBO II to share the same data link.

SGS-THOMSON MICROELECTRONICS SLIC AND THE TS5070/71 COMBO II : A KIT APPROACH

SGS-THOMSON Microelectronics provides now solid-state monolithic SLICs. These chips associated with the TS5070/71 COMBO II and the especially designed protection components, feature all the BORSCH functions (i.e. Battery feeding, Overvoltage protection, Ringing injection, Supervision of the loop, Codec/Filter and Hybrid 2-wire to 4-wire conversion). The versatility of these kits allows an easy adaptation for the different Telecom Administrations requirements throughout the world.

The schematic diagrams are detailed in fig. 2 and 3. The SGS-THOMSON SLICS parallel control interface allows the use of the IL interface latches of the TS5070/71 COMBO II (see fig. 2 and 3).

The ZAC impedance synthesizes the output impedance of the SLIC on Tip & Ring ; hence, this network should be designed differently for each country. The

structure of this network is a copy of the line impedance ; please, refer to the relevant SLIC data-sheet for more details. The "balancing" network, ZA and ZB is used by the SLIC to balance the 2-wire/4-wire conversion. When using the TS5070/71 COMBO II, this balancing network is no more necessary (ZB pin to GND) being the hybrid balancing performed by the "Hybal" filter of the Combo.

3. PROGRAMMING THE TS5070/71 COMBO II

The control information of the TS5070/71 COMBO II require 2 bytes of informations, with the exception of a single-byte power-up/down command.

When CS is pulled low a first "instruction" byte is shifted into the TS5070 COMBO II, at pin CI (or CI/O for the TS5071) on the falling edge of each CCLK clock pulse, the most significant bit first. During the 8th (dummy) bit, the content of this instruction is decoded by the Combo and, depending wether a "read" or a "write" instruction is performed, a second "data" byte is shifted into or shifted out from the Combo.

* Bit #1 is the single-byte control bit : when 0, this is a single-byte power-up/down instruction, no data byte is expected.

* Bit #2 is the read/write control bit : when 0, the data byte will be written by the card controller into the Combo. When 1, the data byte will be read by the card controller from the Combo.

* Bit #3, 4, 5, 6 specify which one of the 10 registers of the TS5070/71 COMBO II is to be accessed.

* Bit #7 is the power control bit : when 0, the Combo is placed in power-up state ; when 1, the Combo is placed in power-down. Note that the power state can be set in any instruction.

* Bit #0, the last bit, is a dummy bit to allow for decoding of the 7 previously entered bits. Its value is not taken into account and has no influence on the TS5070/71 COMBO II operation.

When writing to the TS5070/71 COMBO II, the data byte may follow the instruction byte immediately, or CS may be pulled high between the 2 bytes. The data byte is shifted into the Combo in the same way as the instruction byte : MSB first, on the falling edge of each CCLK clock pulse.

When reading from the TS5070 COMBO II, the data byte is shifted out, onto the CO pin (CI/O pin for the TS5071), MSB first, on the rising edge of each CCLK clock pulse. As for the write operation, CS can be pulled high between the instruction and the data byte.

After a read or a write operation is completed, it is recommended, although this is not mandatory, that the CS pin should be put high to reset the control port logic.

The content of the instruction byte is detailed in table 1 :

Table 1 : Instruction Byte.

Bit #	7	6	5	4	3	2	1	0
Single Byte Power-up/down	P	X	X	X	X	X	0	X
Control Register	P	0	0	0	0	W	1	X
Latch Direction Register	P	0	0	1	0	W	1	X
Interface Latch Register	P	0	0	0	1	W	1	X
Receive Time-slot/port	P	1	0	0	1	W	1	X
Transmit Time-slot/port	P	1	0	1	0	W	1	X
Receive Gain Register	P	0	1	0	0	W	1	X
Transmit Gain Register	P	0	1	0	1	W	1	X
Hybrid Balance Register # 1	P	0	1	1	0	W	1	X
Hybrid Balance Register # 2	P	0	1	1	1	W	1	X
Hybrid Balance Register # 3	P	1	0	0	0	W	1	X

P = Power control bit : "0" = Power-up, "1" Power-down
W = Read/Write control bit : "0" = Write, "1" = Read
X = don't care (0 or 1)

DATA BYTE : CONTROL REGISTER

The content of the control register is detailed in table 2 :

Table 2 : Control Register.

Bit Number							Function
7	6	5	4	3	2	1	0	
0	0							MCLK = 512KHz
0	1							MCLK = 1.536 or 1.544MHz
1	0							MCLK = 2.048MHz*
0	1							MCLK = 4.096MHz
		0	X					μ-255 Law*
		1	0					A-law, with Even Bit Inversion
		1	1					A-law, no Even Bit Inversion
				0				Delayed Data Timing
				1				Non-delayed Data Timing*
					0	0		Normal Operation*
					1	X		Digital Loopback
					0	1		Analog Loopback
							0	Power Amp Enabled in PDN
							1	Power Amp Disabled in PDN*

* = State at power-on initialization.

The * specifies the default value of the control register at the power-on initialization.

MCLK : Master clock used by the Combo's filters, encoder and decoder. It is necessary to indicate which frequency is beeing applied to the Combo, for a correct filter operation.

COMPANDING LAW : the μ-255 compressing and expanding law is used in USA & Japan, A-law in Europe. Usually, in A-law, even bits are inverted : 0000 0000 becomes : 0101 0101 ; if this even bit inversion is performed in another part of the switching system, a "No even bit inversion" is available.

DATA TIMING : In Non-delayed Data Timing mode, the time-slot always begin with the rising-edge of FSX or FSR ; Time-slot Assignment is not available in this mode.
In Delayed Data Timing mode, time-slot begins after a falling edge of BCLK, when FSX or FSR is set high ; the Time-slot Assignment feature of COMBO II can be used in this mode only.

Note that PCM port selection is available in both timing modes.

LOOPBACK : Test modes : In Analog Loopback, VFXI is isolated from input pin and internally connected to the VFRO output, providing a complete D to D test loop.

In Digital Loopback, the PCM byte written into the Receive register, can be read back in any Transmit Time-slot at DX0 (or DX1) pin.

POWER AMP : if "1", the power amplifier, at VFRO output is disabled during the power-down state, i.e. VFRO pin is high impedance state.

It is very easy to set the TS5070/71 COMBO II configuration in any "U.S." or "European" environment.

In the following example, the line card module must be adapted to an european telecom administration specifications ; should be selected :

- Master clock = 2.048MHz
- A-law with even bit inversion
- Delayed data timing (which allows the Time-slot assignment feature)
- Normal operation (no loop back)
- Power amp disabled in power-down

Consequently, the instruction byte 10000010 (82 hexadecimal), followed by the data byte "10100001" (A1 hexadecimal) should be written into the COMBO II.

DATA BYTE : LATCH DIRECTION REGISTER

Bit Number							
7	6	5	4	3	2	1	0
L0	L1	L2	L3	L4	L5	X	X

* The bits #7 to #2 specify the function of each interface latch pin ; bit #0 and bit #1 are dummy bits.
* If Ln = 0 then ILn is a high-impedance input.
* If Ln = 1 then ILn is an output.

Notes : - unused pins should be programmed as outputs.
- When using the TS5071 the IL5 pin should be programmed as an output.

In the case of a L3092 SLIC, as described in fig. 3, IL0 pin, IL1 and IL4 are connected to L3092 inputs : they must be programmed as outputs. IL2 and IL3 must be set as inputs, because they are connected to L3092 outputs and IL5 is not used : this pin should be set as output.

In this example a "11001100" (CC hexadecimal) code should be written into the Latch Direction Register.

DATA BYTE : INTERFACE LATCH REGISTER

Bit Number							
7	6	5	4	3	2	1	0
D0	D1	D2	D3	D4	D5	X	X

X = Don't Care.

* When writing to this register, the IL pins programmed as outputs assume the state of the corresponding bit Dn, in data byte.

* When reading from this register : for the IL pins programmed as outputs, the Dn bits correspond to the data previously written in this register ; for the IL pins programmed as inputs, the Dn bits correspond to the data read by these input pins.

In the case of the L3092 (fig. 3), if the SLIC must be put in "stand-by" mode, i.e. PWON and RNG pins = 0 and NCS = 1, "00001000" (08 hexadecimal) should be written into the Interface Latch Register. Note that bit #5 and bit #4 have no effect, since the IL2 and IL3 pins are programmed as input.

DATA BYTE : RECEIVE TIME-SLOT REGISTER AND TRANSMIT TIME-SLOT REGISTER

Bit Number and Name								
7	6	5	4	3	2	1	0	
EN	PS	T5	T4	T3	T2	T1	T0	
0	1	X	X	X	X	X	X	Disable DX Outputs (in TX reg.) Disable DR Inputs (in RX reg.)
1	0	Time-slot (0-63)						Enable DX0 Output, Disable DX1 (in TX reg.) Enable DR0 Input, Disable DR1 (in RX reg.)
1	1	Time-slot (0-63)						Enable DX1 Output, Disable DX0 (in TX reg.) Enable DR1 Input, Disable DR0 (in TX reg.)

* The 6 bits T5-T0 assign one time-slot from 0 to 63 (111111 in binary) ; available in Delayed Data Timing only.

* The PS "Port Selection" bit #6 selects the DR0 input, when 0, or the DR1 input, when 1, in the Receive Time-slot register, and, respectively DX0 or DX1 output in the Transmit Time-slot register.

Note : On the TS5071 the DR1 and DX1 pins are not bonded out : the PS bit must always be set to 0.

* The EN bit enables (when 1) the PCM input or output selected by the PS bit or disables them (when 0).

Note : the disabled pins are in a high impedance state.

In the above example, "Delayed Data Timing" was selected in the Control Register : when using the DX0/DR0 PCM port, time-slot #5 for transmission and time-slot #27 for reception, the contents of the TX time-slot and RX time-slot registers must be : "10000101" (85 hexadecimal) and "10011011" (9B hexadecimal).

DATA BYTE : TRANSMIT GAIN AND RECEIVE GAIN REGISTER

The TS5070/71 COMBO II includes a transmit and a receive programmable amplifier ; these amplifiers allow an easy setting of the transmission level point (0TLP = 0dBm0) of the COMBO II, within the specified limits. The following formulas give the 2 bytes to be programmed in the TX and the RX gain registers :

200 X log10 (V_{VFXI} / $\sqrt{0.6}$) + 191, for the TX Gain Register, converted in binary.

200 X log10 (V_{VFRO} / $\sqrt{0.6}$) + 174, for the RX Gain Register, converted in binary.

V is the desired analog voltage, at VFXI pin for TX gain and VFRO pin for RX gain, expressed in Vrms, and corresponding to a digital 0dBm0 PCM level, as defined in CCITT G.711 ; the transmit input signal at VFXI must be in the range of 0.087 to 1.619Vrms, and the output receive amplifier at VFRO provides a signal from 0.106 to 1.96Vrms (for a 0dBm0 PCM signal).

The TX and RX gains can be also calculated from

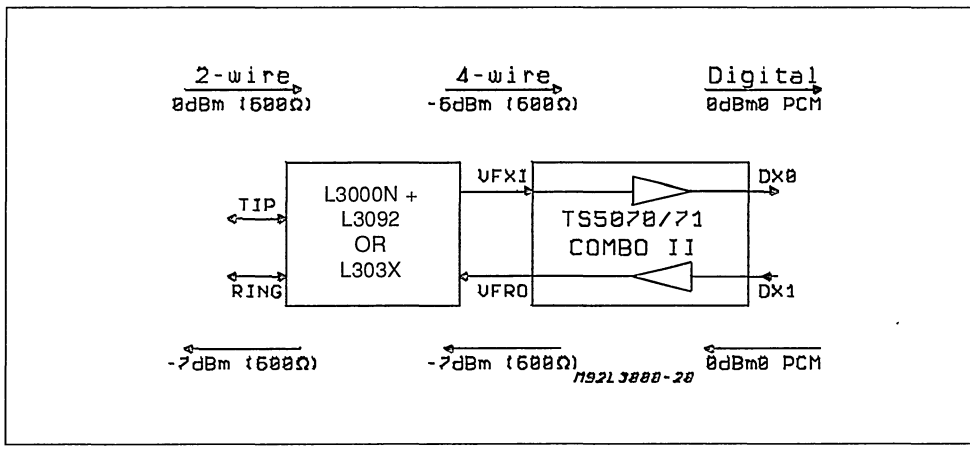
the desired analog levels at VFXI and VFRO expressed in dBm into 600Ω ; in this case, the bytes to be programmed are calculated as follows :

10 X (VFXI level in dBm 600Ω) + 191, for the TX Gain Register, converted in binary.

10 X (VFRO level in dBm 600Ω) + 174, for the RX Gain Register, converted in binary.

Refer to the following example (fig. 4) :

Figure 4 : Example of TX and RX Levels.



- the transmit signal is 0dBm (600Ω) on Tip-Ring wires for a 0dBm0 PCM level at the DX0 output.
- the receive signal is - 7dBm (600Ω) on Tip-Ring wires for a 0dBm0 PCM level at the DR0 input.

The 0dBm0 PCM level is the bit sequence defined in the CCITT recommendation G.711.

We must first determine the analog levels at VFXI input and VFRO output of the TS5070/71 COMBO II. Due to their "feedback loop" structure, the SGS-THOMSON SLICs considered have a 0dB gain, in RX direction and –6dB in TX direction. This particular TX gain has been chosen in order to optimize hybal COMBO II filter dynamic range. Consequently the analog level at VFXI input will be : –6dBm (600Ω) = 0.3873Vrms, and the output level at VFRO : – 7dBm(600Ω) = 0.346Vrms.

The TX gain to be programmed in the TS5070/71 COMBO II will be :

10 X (–6dBm) + 131 = 83 hexa = 10000011 binary

this byte must be written in the TX gain register.

The RX gain will be :

10 X (- 7dBm) + 174 = 174 - 70 = 104 = 68 hexa = 01101000 binary

this byte must be written into the RX gain register.

These programmable gains provide more flexibility for the design of the line-card : if the transmit signal is - 8dBm instead of –6dBm, it is easy to re-program the TX gain register :

10 X (- 8dBm) + 191 = 191 - 80 = 111 = 6F hexa = 01101111 binary

In this case, TX gain must be set to 111 decimal = 6F hexadecimal = 01101111 binary. It is easy to adapt this example to any particular configuration. The designers shall notice that the gains are adjusted in 0.1dB steps. Consequently, the gain for - 8dBm will be 20 steps below the gain for –6dBm, i.e. 131 - 20 = 111.

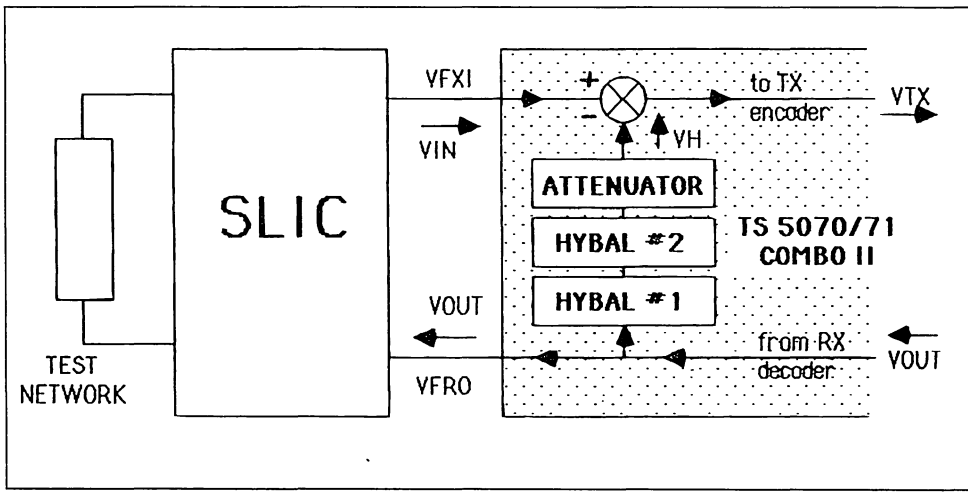
Note that if the analog output level, at VFRO, exceeds 1.7Vrms, for a 0dBm0 PCM input at DR0, there are some restrictions on the value of the load connected at VFRO :

- if the level is less than 1.7Vrms, the load impedance must be greater than 300Ω
- if the level is between 1.7Vrms and 1.9Vrms, the load impedance must be greater than 600Ω
- if the level is between 1.9Vrms and 1.96Vrms, the load impedance must be greater than 15KΩ

4. HYBRID BALANCING

The hybrid balance filter of the TS5070/71 COMBO II is entirely programmable : the "zero" and "pole" combinations for the low frequency Hybal filter #1 and the high frequency Hybal filter #2 can be set by the card controller ; in addition, a programmable attenuator adjust the amplitude of the cancellation signal (see fig. 5).

Figure 5 : Hybrid Balance Cancellation Filter.



The Hybrid Balance Filter is set by the contents of 3 registers ; an optimization software (TS5077) determines the 3 bytes to be written in these registers.

ECHO PATH OF THE SLIC

The first step for the calculation of the Hybrid Balance Filter is the echo path of the SLIC : VIN/VOUT (see fig. 5). The amplitude and the phase of the echo signal must be determined for 14 frequencies, from 200 to 3500Hz. A "Hybrid Balance" test network must be connected between Tip and Ring wires.

The echo path can be measured or calculated by simulation of the transfer function of the SLIC. The TS5077 optimization software includes a simulation module for a transformer SLIC.

OPTIMIZATION SOFTWARE

The echo path must be entered into the program, for each balancing network, then the optimization routine is run. This routine tests all the combinations of the Hybrid Balance Filter and selects the one which is the closest to the echo path, and then provides the three bytes to be programmed into the three Hybrid Balance registers. Some optimization examples with the different SLIC kits from SGS-THOMSON Microelectronics are described in the Application Note "SGS-THOMSON SLIC KITS and COMBO II".

5. CONCLUSION

These examples show the great flexibility of the TS5070/71 COMBO II in its adaptation with different line-cards, different SLICs and different countries. This flexibility, coupled with the programmable features, enhance the integration of the line-card : more subscribers per board, more reliability, easier adaptation, ... and, last but not least : a significant reduction of the total cost of the line card.

Figure 1 : Interface with Transformer SLIC.

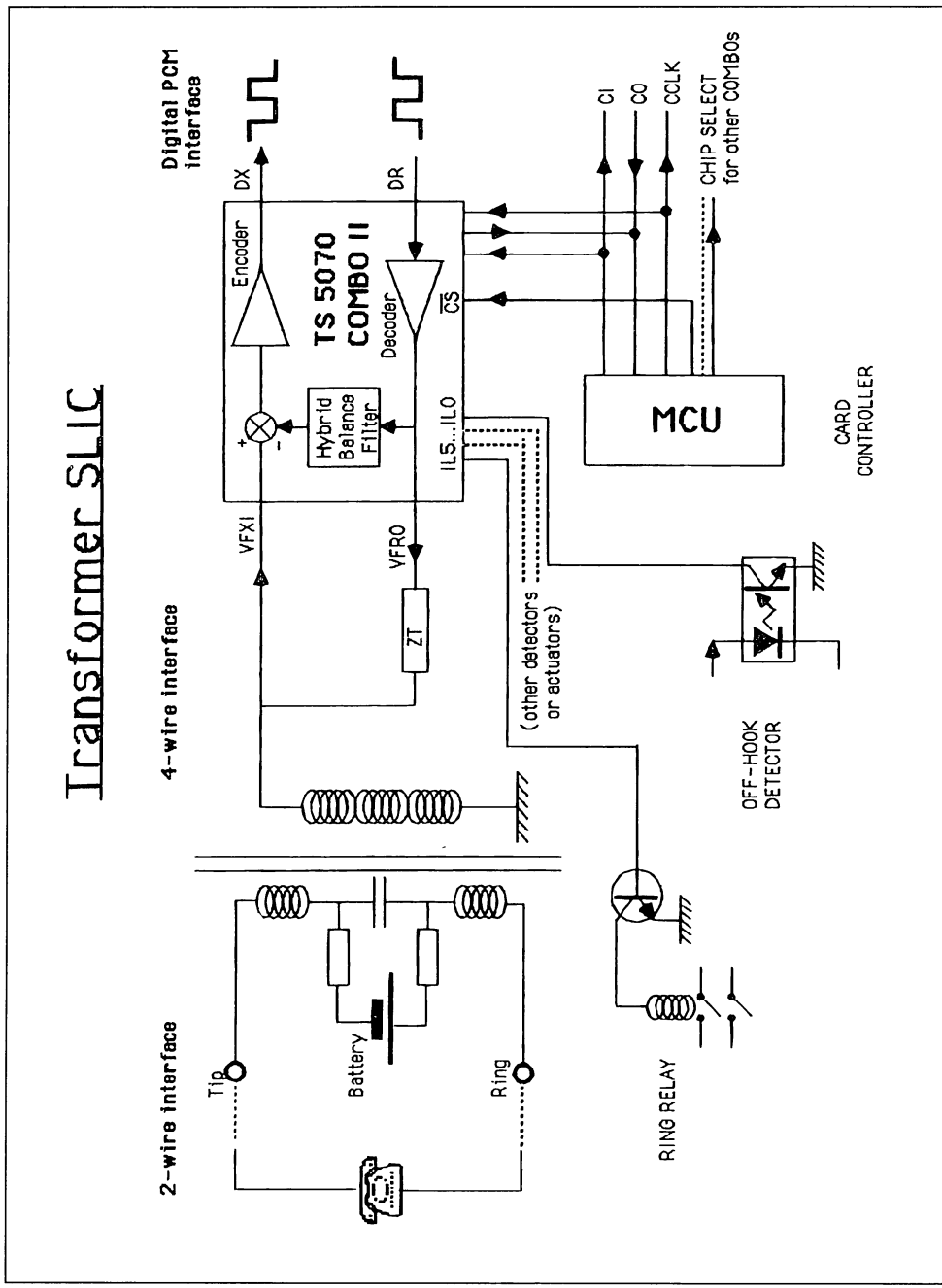


Figure 2 : Interface with L3037 Monochip SLIC.

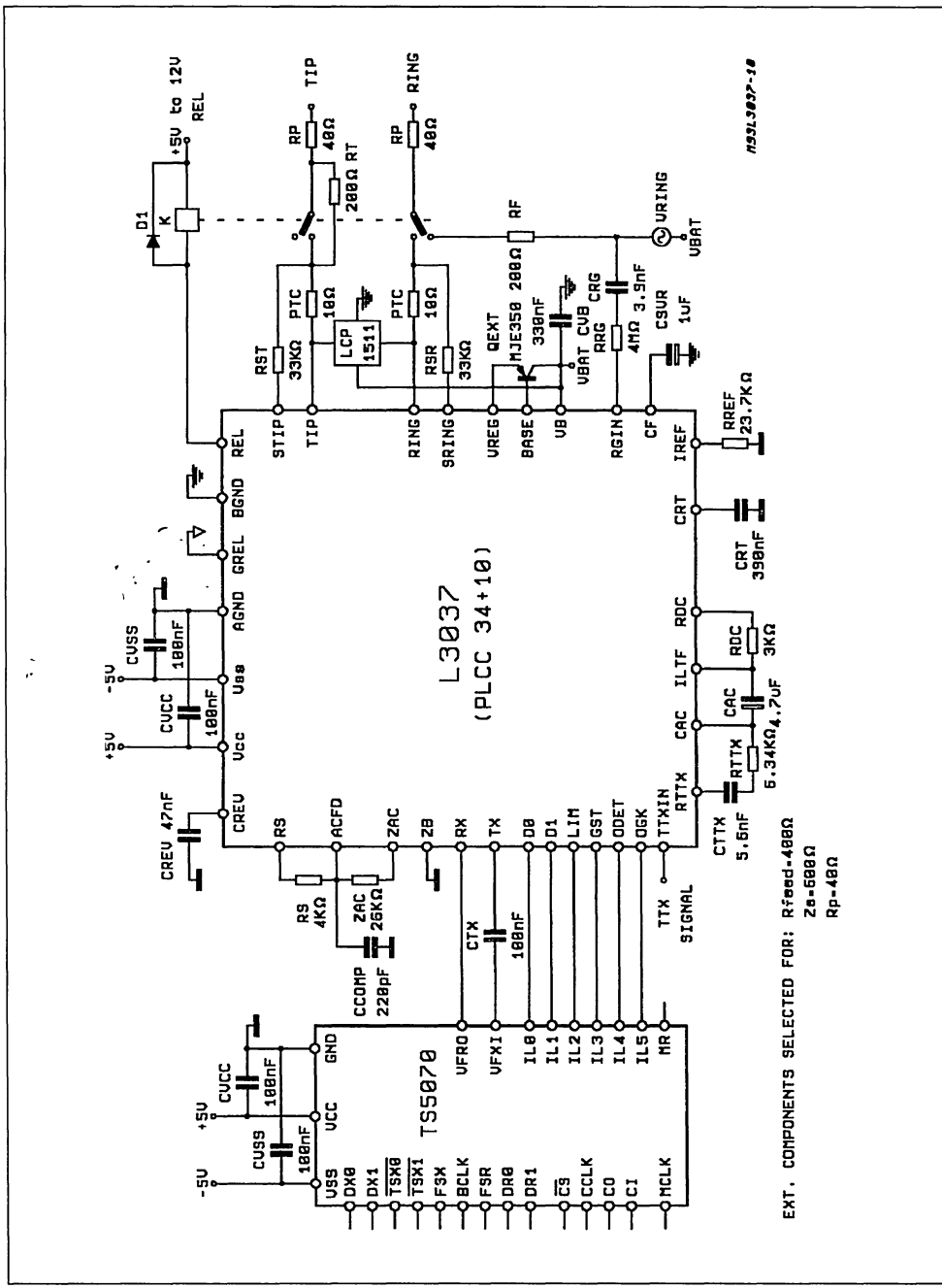
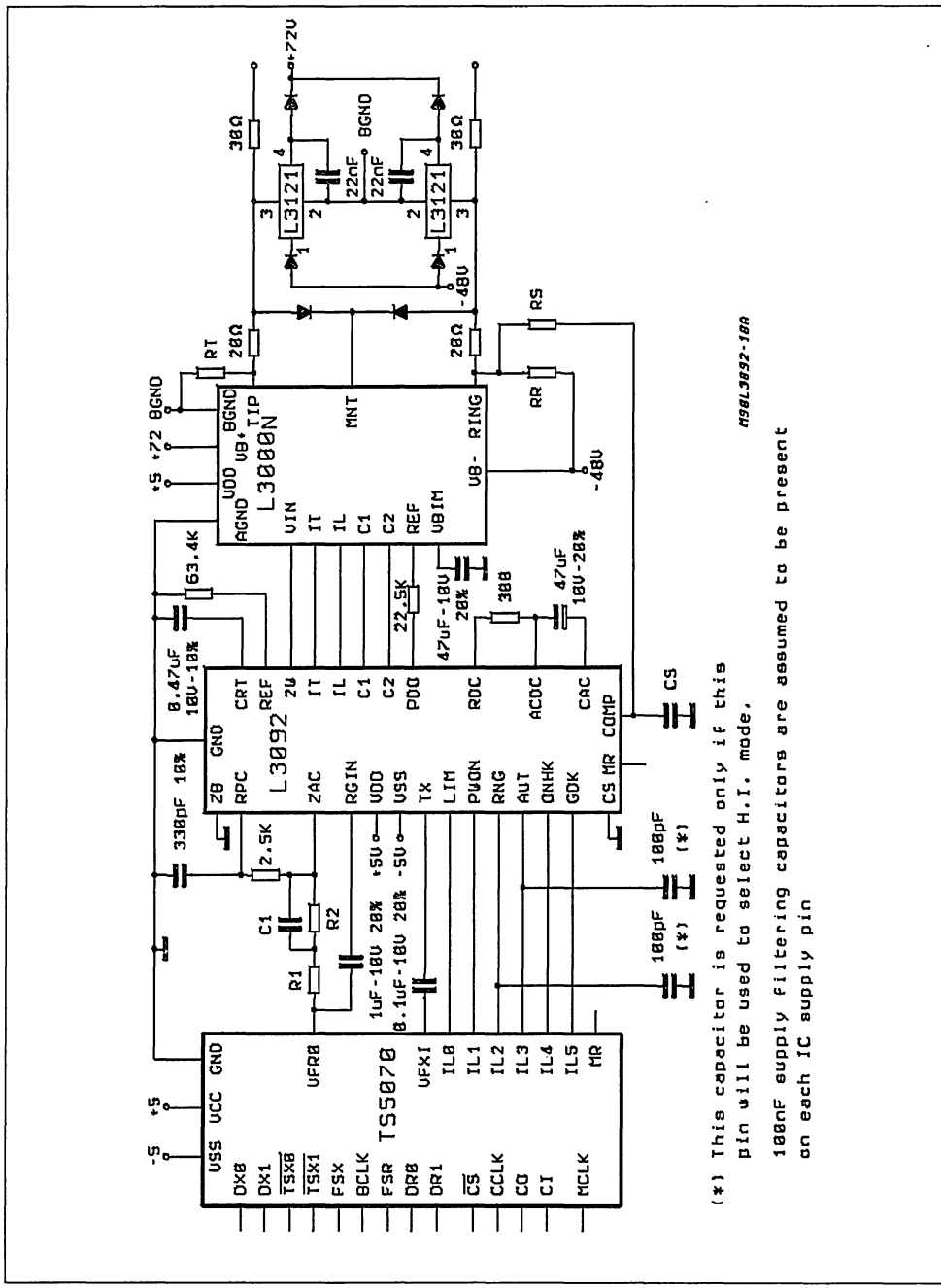


Figure 3 : Interface with L3000N + L3092 Solid-state SLIC.



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

PABX BIG COST REDUCTION AND PERFORMANCE IMPROVEMENT ARE OBTAINED WITH A NEW SLIC CHIP SET

by W. Rossi

The new L3000N/L3092 SLIC need very few external components, very low power in ON-HOOK and provide innovative functions like Ringing injection, message waiting, line length measurement for autoadaptive systems.

Abstract

The new SGS-THOMSON SLIC (Subscriber Line Interface Circuit) kit L3000N/L3092 suitable for PABX (Private Automatic Branch Exchange), low end C.O. (Central Office) and ISDN terminal adaptor applications is described. The two chip approach allows the integration of innovative functions as ringing generation and injection, line length evaluation, message waiting, loop extension all software programmable. High level DC/AC performances are provided and very low power is requested in on hook condition (less than 10mW from battery and typ. 50mW from ±5V supplies).

1. INTRODUCTION

The '90 years represent a transition period from fully analog solution to fully digital (ISDN) one in PABX systems design. In particular in this new systems generation analog and digital line cards will coexist. The SLICs for this new systems should satisfy the following requirements:

- do not degrade the transmission performances of the digital part (ex: noise due to relay bounces during ringing injection).

- Software programmability of the DC/AC characteristics in order to have an easy adaptation to different countries requirements.

- Signaling self management in order to simplify the card controller software.

- Low number of external components.

- High reliability and low cost.

In order to satisfy the above requirements a complex circuit structure is necessary. Such a structure cannot be integrated in a single chip because high voltage technology is required to interface the subscriber line. Single chip solutions based on present H.V. Technology are possible only giving up most of the above requirements or increasing too much the device size and the external components number. The SGS-THOMSON SLIC family actually in production and based on a two chip approach is able to satisfy the above requirements. In fact only the circuit directly connected to the line is realized in High Voltage Technology while all the control and signal management functions are performed in the control chip realized in high density, Low Voltage Technology. (15V). In addition this approach allows an easy adaptation to different applicative situation only selecting the proper low voltage control chip. In the following the L3000N/L3092 kit is deeply described.

2. L3000N-L3092 GENERAL DESCRIPTION

The SLIC KIT L3000N/L3092 integrate all the functions, except the overvoltage protection, needed to interface a subscriber line. As shown in fig.1 the L3000N chip is a directly connected to the telephone line. On the L3092 chip two interfaces are present. The first is an analog interface (4W) connected to the analog input/output of a Codec/Filter. The second one is a parallel digital interface that allows to set different operating modes of the kit and to transfer information about line status. Because of the internal latches circuit this interface can be connected to a SLIC common control bus driven by the Line Card Controller (see fig. 1). In alternative this interface can be directly connected to the I/O control port of a second generation COMBO as SGS-THOMSON TS5070/TS5071 (see fig. 2). The main features of the L3000N/L3092 are the following :

- Programmable DC feeding resistance and limiting current (25/40/60mA)

- Low power dissipation (50mW) in on hook condition (off-hook detector active).

- Loop extension / Integrated message waiting function.

- Signaling function (ON-HOOK/OFF-HOOK; GROUND-KEY/GROUND-START detection)
- Line length evaluation
- Hybrid function
- Line impedance synthesis (real/complex)
- Balanced ringing signal generation with zero crossing injection
- Automatic ringing stop with zero crossing when OFF-HOOK is detected.
- Parallel latched digital interface for direct connection with 2nd generation COMBO or Card Controller
- Low number of external standard tolerance components.
- Integrated thermal protection that disable output stages when junction temperature exceeds 140°C

Figure 1: The latched parallel digital interface of L3092 allows an easy common bus control structure. The card controller select the proper SLIC via the corresponding CS pin.

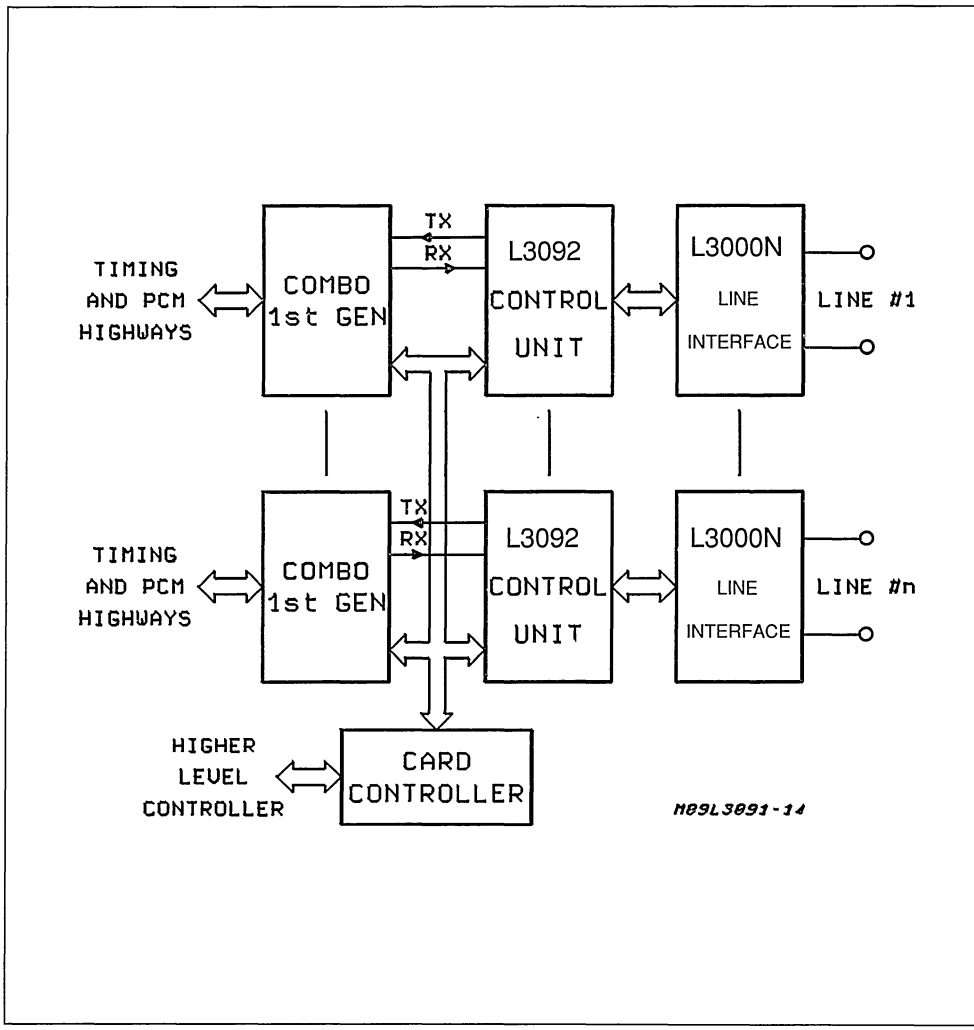
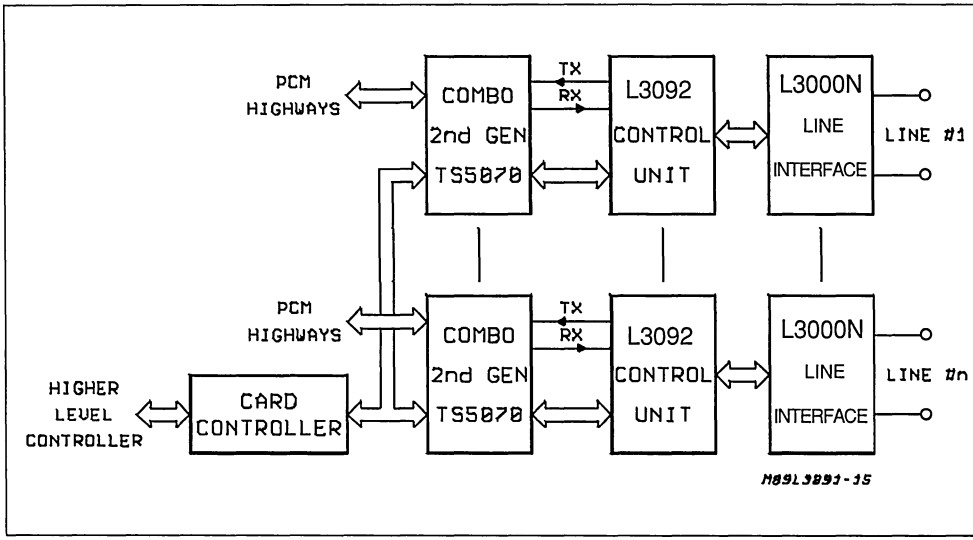


Figure 2: The digital interface of L3092 is directly connected to the COMBOII I/O ports. The card controller manage this I/O digital interface via a 2Mbit serial control port.



3. OPERATING MODES

Three input and two output pins represent the parallel digital interface. In addition a CS pin allows to connect the digital interfaces of all the SLICs on the Line Card to the same control bus; the digital datas applied to this interface selects one of the following operating modes:

- Conversation or Active Mode
- Stand-by or On-Hook Mode
- Power Down or Disable Mode
- Ringing Mode

4. CONVERSATION OR ACTIVE MODE

The SLIC is setted in this mode when the off-hook condition has been detected and the communication must be activated; the main functions performed in this mode are:

1) DC current feeding into subscriber loop.

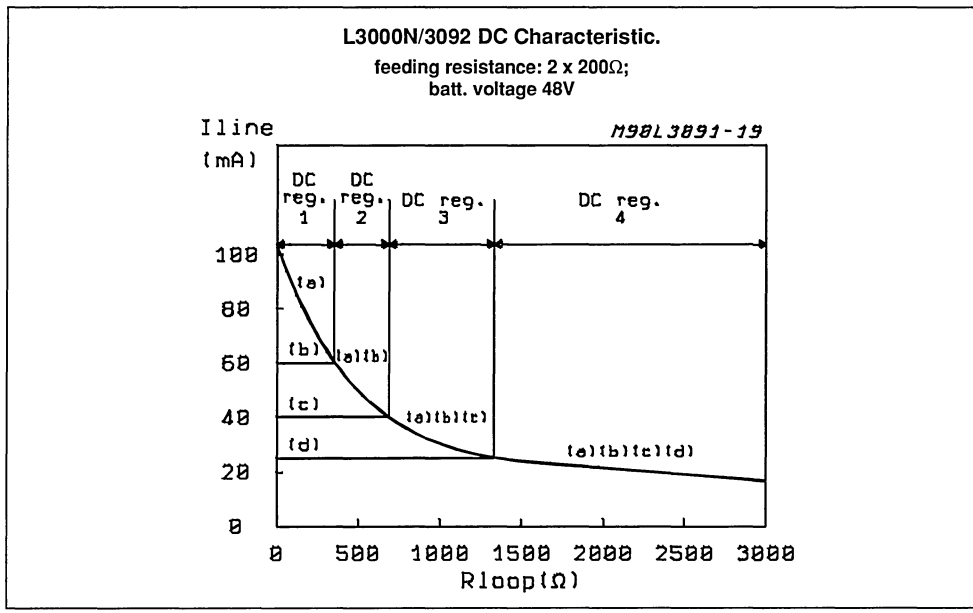
2) Signaling recognition (OFF-HOOK; GND-KEY; DIAL PULSES)

3) Bidirectional transfer of speech band signals between line (2wire) and COMBO (4wire) interfaces.

4.1 DC CHARACTERISTIC

One of the main SLIC function is to provide a DC current to the subscriber loop in order to feed properly the connected telephone set. In fig. 3 different DC characteristics Line Current (Il) versus loop resistance (Rl) are shown. The (a) curve represents the DC characteristic obtained with traditional line interface based on transformer; as you can see it is a purely resistive characteristic (Il=VBAT/(2xRFS)) where typical RFS values are 200ohm and 400ohm. The (b), (c), (d) curves represent the three different programmable DC characteristics that can be obtained with the L3000N/L3092 SLIC kit in conversation mode. Each curve is composed by two regions the first with constant line current and the second resistive were the RFS value is programmed by means of one external resistor. The constant current region allows a big power dissipation reduction with short lines if compared with the transformer solution. In addition the possibility to program by software different limiting currents (25,40,60mA) make the system more flexible allowing an easy adaptation to the different administration requirements and the possibility of the line length measurement. In fact when TEST MODE function is activated one of the digital interface output will show if the actual line current is equal or lower than the programmed limiting current value. The possibility to program three different limiting current values allows to distinguish four different line resistances ranges as shown in fig. 3; this information is very useful in order to optimize the transmission performances for each line length.

Figure 3: The (a) curve represents the DC characteristic obtained with traditional line interface based on transformer. The (b), (c), (d) curves represent the three different programmable DC characteristics that can be obtained with the L3000N/L3092 SLIC kit in conversation mode.

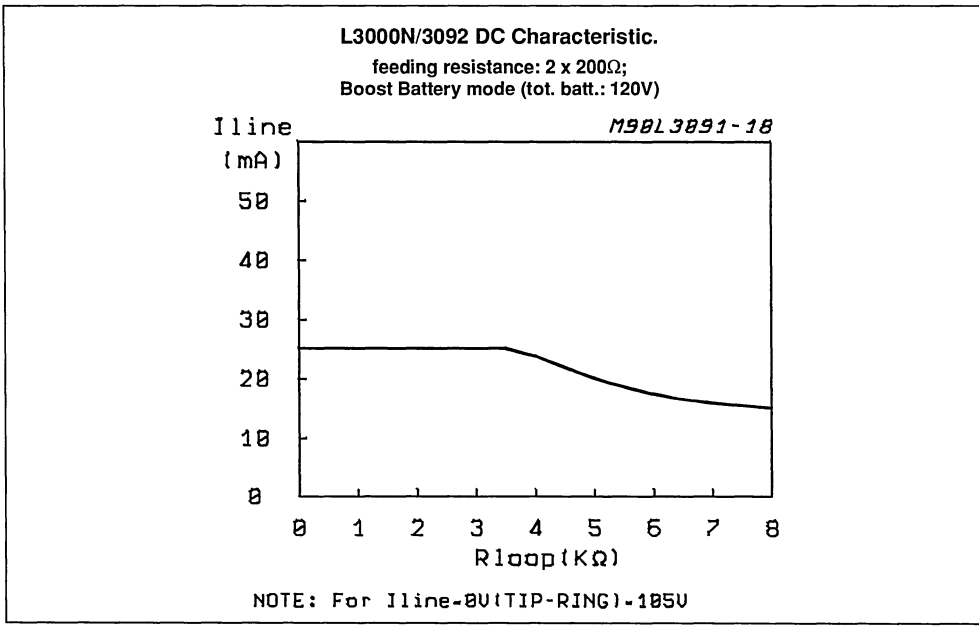


In particular if a second generation COMBO, as SGS-THOMSON TS5070/71 is adopted the line length can be used to select by software proper transmit/receive gains and balance impedances obtaining in this way an autoadaptive system at four states. Another important feature consists in the balanced line feeding circuit; it means that line current variations will produce equal and opposite voltage variations on the A, B, or TIP, RING SLIC line terminations. This characteristic is very important because during dial pulse selection the line current change from zero to the maximum value producing large line voltage variations. The balanced structure avoid high common mode signals generation with very short rise/fall time. It should be noted that this problem is always present when monolithic SLICs with integrated DC/DC converter are adopted in fact in this case doesn't exist voltage symmetry between the two line terminations. This kind of common mode signals produce serious transmission problems on the ISDN line present in the same system; in addition they are also noise sources for the other analog lines. The L3000N/L3092 SLIC kit has been studied not only in order to avoid common mode noise on the line, but also to be less sensitive to the noise present on the battery voltage typically generated by dial pulse selection and ringing injection operations. In particular the noise on the battery voltage is transferred to the line with an attenuation higher than 20dB for low frequency components (10Hz) and with more than 40dB for speech band components (typ. 1kHz).

4.2 LONG LINES FEEDING.

The L3000N/L3092 SLIC kit is also suitable for public central office, since in this application is sometimes required to feed very long lines a particular operating mode (Boost Battery) is provided. When the boost battery mode is activated the DC characteristic is modified allowing 20mA of feeding current for 4Kohm of loop resistance equivalent to more than 10Km (see fig.4). Considering PABX dedicated to Hotel applications this operating mode can be used to perform the "MESSAGE WAITING" function. In fact when the Boost Battery mode is selected and the line current is zero the line voltage is greater than 100V; this voltage is high enough to switch on the neon lamp on the telephone set typically used to inform the subscriber to call back the operator. During Boost Battery operation the L3000N line interface circuit fed its internal output stages between the negative battery (typ -48V) and the positive bat-

Figure 4: DC characteristic in Boost Battery mode allows to feed very long lines (20mA/4Kohm) and to perform the "message waiting" function. For line current close to zero the TIP/RING voltage is greater than 100V.



tery voltage (typ. +72V) already present for the ringing operation.

4.3 SIGNALING.
When the Conversation operating mode is selected on the two output pins of the digital interface the following informations are provided:
1) ON-HOOK/OFF-HOOK detection
2) GROUND KEY / GROUND START detection.
In addition the off-hook detection delay is very low allowing dial pulse detection with a distortion lower than 1% . On the contrary the ground key information is filtered with a time constant in the range of 100ms.

4.4 AC CHARACTERISTIC.
The L3000N/L3092 SLIC kit provide excellent AC characteristics, in addition its internal structure allows an easy programming of the line and balance impedances both real or complex by means of external scaled (by 25) components. It means that in case of complex impedances the external capacitors values will be 25 time lower than the synthetized values. Another peculiarity of the L3000N/L3092 SLIC kit is the possibility to recover the insertion loss due to the external protection resistors connected between the SLIC TIP and RING (A, B) output pins and the line; such resistors cannot be avoided being necessary to limit the line current when surges or other causes produces overvoltages on the line. The major part of the monolithic SLICs available on the market requires low values for the external protection resistors (< 20ohm) being not able to recover the attenuation produced by such components.

This attenuation become a problem in presence of complex line impedance because its value depends also on the frequency. If protection resistors higher than 20ohm are adopted the correspondent amplitude distortion with frequency will not be acceptable and external complex equalizing circuit required.

On the contrary the L3000N/L3092 SLIC kit allows to use protection resistors in the range from 30 to 100ohm increasing in this way the system protection level. In this condition the guaranteed insertion loss flatness (including external protection resistors) between 2W (line) and 4W (COMBO) interfaces is +/- 0.1dB for both real or complex line impedances.

Another important L3000N/L3092 SLIC kit feature for the overall system performances is the capability to work also in presence of high induced lon-

gitudinal line current. The longitudinal current can be generated by the following causes:

1) Magnetic/capacitive coupling between the subscriber line and the AC main power distribution network (110/220V; 50/60Hz).

2) Magnetic/capacitive coupling with adjacent subscriber line on which large voltage/current variations are present (ex: dial pulse selection; ringing injection..)

3) Magnetic/capacitive coupling with high frequency electromagnetic waves.

For a proper SLIC operation in presence of the above conditions the following characteristics are necessary:

1) High value of Longitudinal to Transversal Conversion (LTC)

2) High value of Longitudinal to Transversal Conversion also in presence of high common mode current.

3) High value of Longitudinal to Transversal Conversion also in presence of high frequency common mode current.

The L3000N/L3092 SLIC kit is able to satisfy all the above requirements; in particular the LTC guaranteed value is 52dB; the typical is 60dB. This value remain nearly unchanged also for high common mode current (ex. 65mA peak on each wire with 25 mA of transversal DC line current or 50mA peak with 40mA of transversal DC line current).

In addition the high gain-bandwidth product of the L3000N integrated operational amplifiers allows to keep the LTC value very high also for common mode current frequencies up to 200/300kHz. Higher frequencies common mode current can be easily attenuated connecting between the line terminations and ground small capacitors (10/20nF). The low effect of such capacitors on the SLIC AC parameters (gains, impedances, two to four wire conversion....) can be easily recovered acting on the SLIC external components thanks to the high flexibility of the two chip architecture.

In fig.5 are shown the test circuit used for EMI evaluation up to 10MHz and the results obtained with and without the filtering capacitors on line terminations. This excellent result show that the L3000N/L3092 SLIC kit provide very high rejection to EMI signals without requiring expensive H.F. coils.

Figure 5a: Test circuit for EMI evaluation.

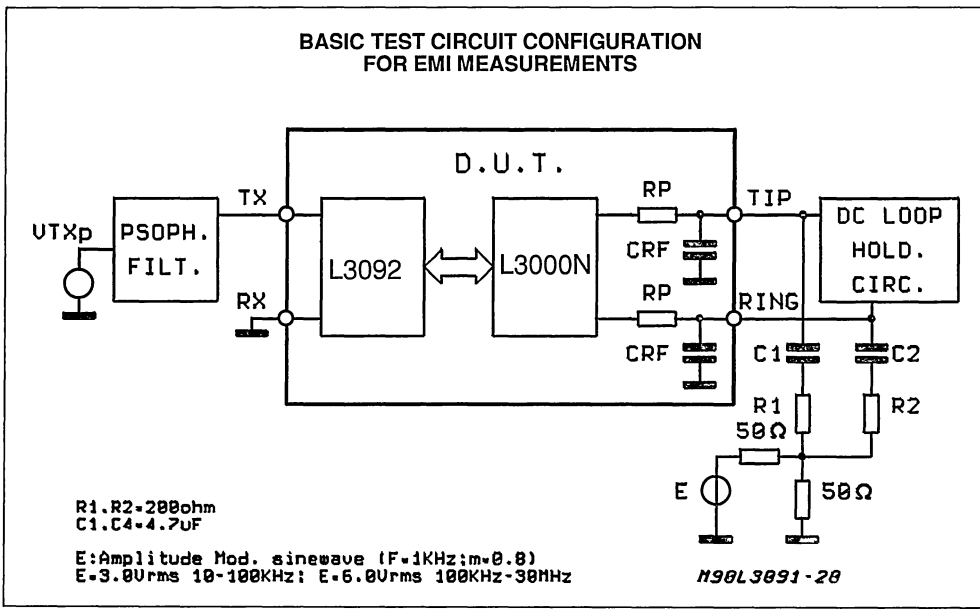
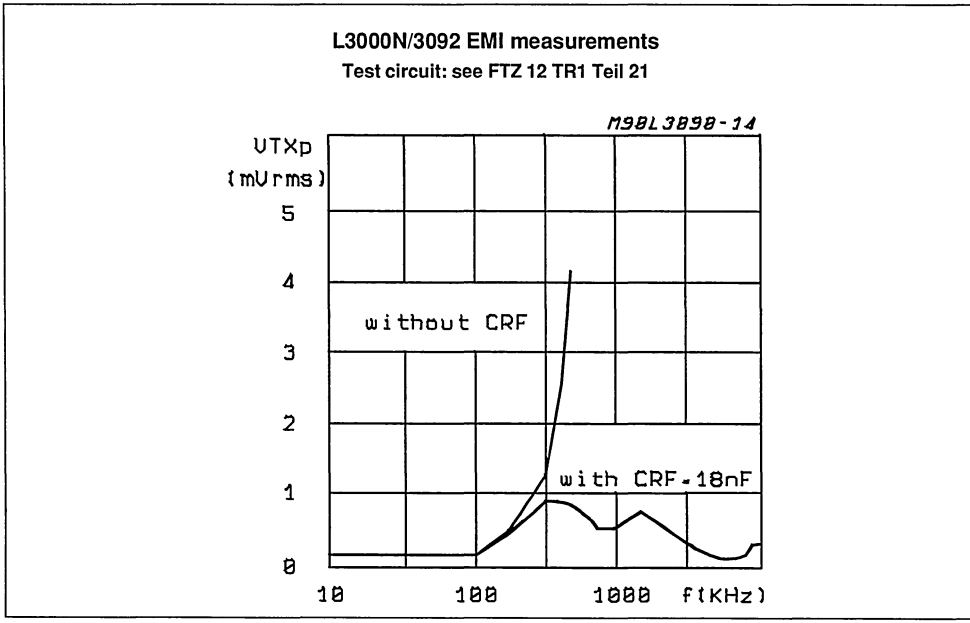


Figure 5b: The high bandwidth and high current capability of L3000N output operational amplifier allows an excellent rejection to longitudinal EMI signals up to 200kHz (a) curve. This good performances are maintained for higher frequencies using two inexpensive small capacitors (Crf=10/20nF).



5. STAND-BY OR ON-HOOK MODE

The L3000N/L3092 SLIC kit is usually programmed in Stand-By mode when the connected telephone set is in on-hook condition; the only functions performed in this mode are:

1) DC line feeding with low limiting current value (10mA)

2) OFF-HOOK detection This second function is performed by a sophisticate circuit that allows a proper off-hook detection also in presence of high common mode currents induced on the line therefore the off-hook information provided by the SLIC doesn't need additional processing by the card controller. The reduced number of functions provided in this mode allows a significative SLIC power dissipation reduction (150mW).

6. POWER DOWN MODE

This mode is used in all those condition in which it is necessary to reduce to zero the power delivered to the line (power failure, emergency, line not connected ....). In power down mode the line interface circuit L3000N is completely switched off therefore not able to detect OFF-HOOK, its impedance at line terminations is 1Mohm and the current sinked from the battery is reduced to zero. In this mode the power dissipation from the +/-5V supplies is typ. 50mW. In case a very low power dissipation is requested also when the telephone is in on-hook and in such condition it doesn't sink more than 500µA the Automatic Stand-by Mode can be selected. The Automatic Stand-by Mode combine the advantages of the two previous operating modes, in particular:

1) Accurate OFF-HOOK detection

2) Low power consumption (50mW from +/-5V and <10mW from battery).

When this mode is selected the L3000N is normally in Power-Down Mode. A dedicated circuitry inside L3092 will sense the line voltage and will automatically program in Stand-by Mode the L3000N if a possible off-hook condition is detected.

7. RINGING MODE

One of the L3000N/L3092 SLIC kit main characteristic is the possibility to inject directly the ringing signal on the line without request of external electromechanical relay and high level ringing

generator. In order to obtain from the L3000N the proper level for the ringing signal an additional positive voltage source is requested (typically +72V).

The ringing signal is obtained amplifying a low level signal (1.5Vrms) applied to the SLIC, this low level oscillation can be obtained either from a local oscillator or from the COMBO RX path. The ringing signal is injected on the line in balanced mode with a nominal amplitude of 60Vrms that can be increased up to 70Vrms.

During the ringing injection the SLIC output impedance is just equal to the two series protection resistors (dohm); this characteristic allows to use lower ringing signal amplitude compared with the standard solutions where the ringing generator series impedance is typically 800ohm. In fig.6 is represented the effect of the low output impedance with different ringer load and compared with the traditional solution with a source voltage of 75Vrms and 800ohm of output impedance.

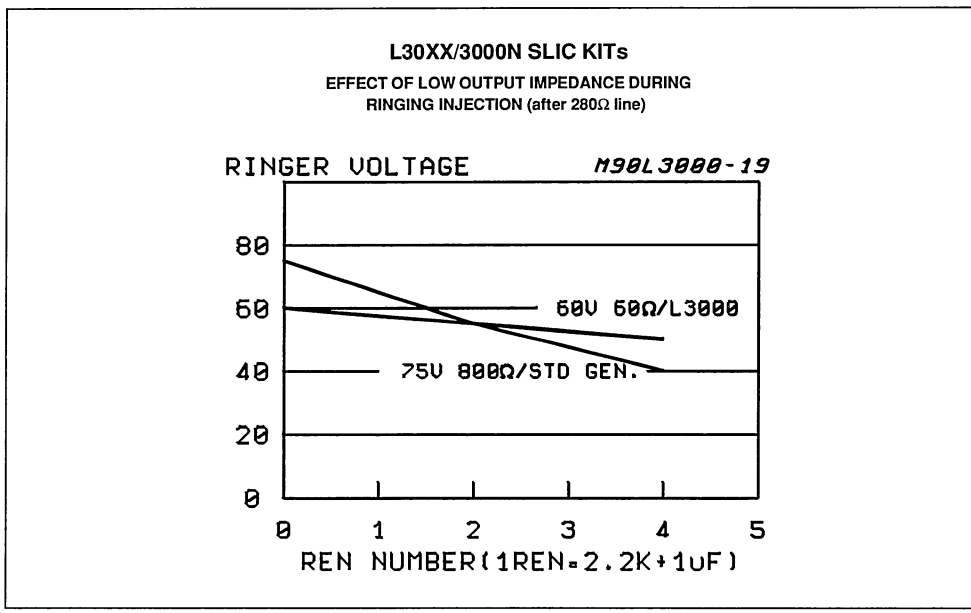
A dedicated circuitry guarantee that the ringing signal is injected and disconnected from the line always in presence of the zero voltage crossing transition, avoiding the generation of very fast voltage transition on the line.

During ringing injection a sophisticate circuit will perform a complete ring trip detection; when off-hook condition is recognized the SLIC will automatically stop the ringing signal without waiting for the card controller command.

In conclusion the L3000N/L3092 SLIC kit allows to save:

- The centralized H.V. ringing generator
- all the ringing relays
- all the zero crossing circuitry
- all the software for ring trip detection.

Figure 6: Comparison between L3000N/L3092 SLIC kit and standard solutions ringing performances. The voltage across the ringer load after 1Km line (280ohm) is shown for different REN (Ringer Equivalent Number). The L3000N low output impedance in ringing mode allows to recover the lower source voltage (60Vrms versus 75Vrms) and to be better than standard solution when the REN increase.



8. CONCLUSIONS

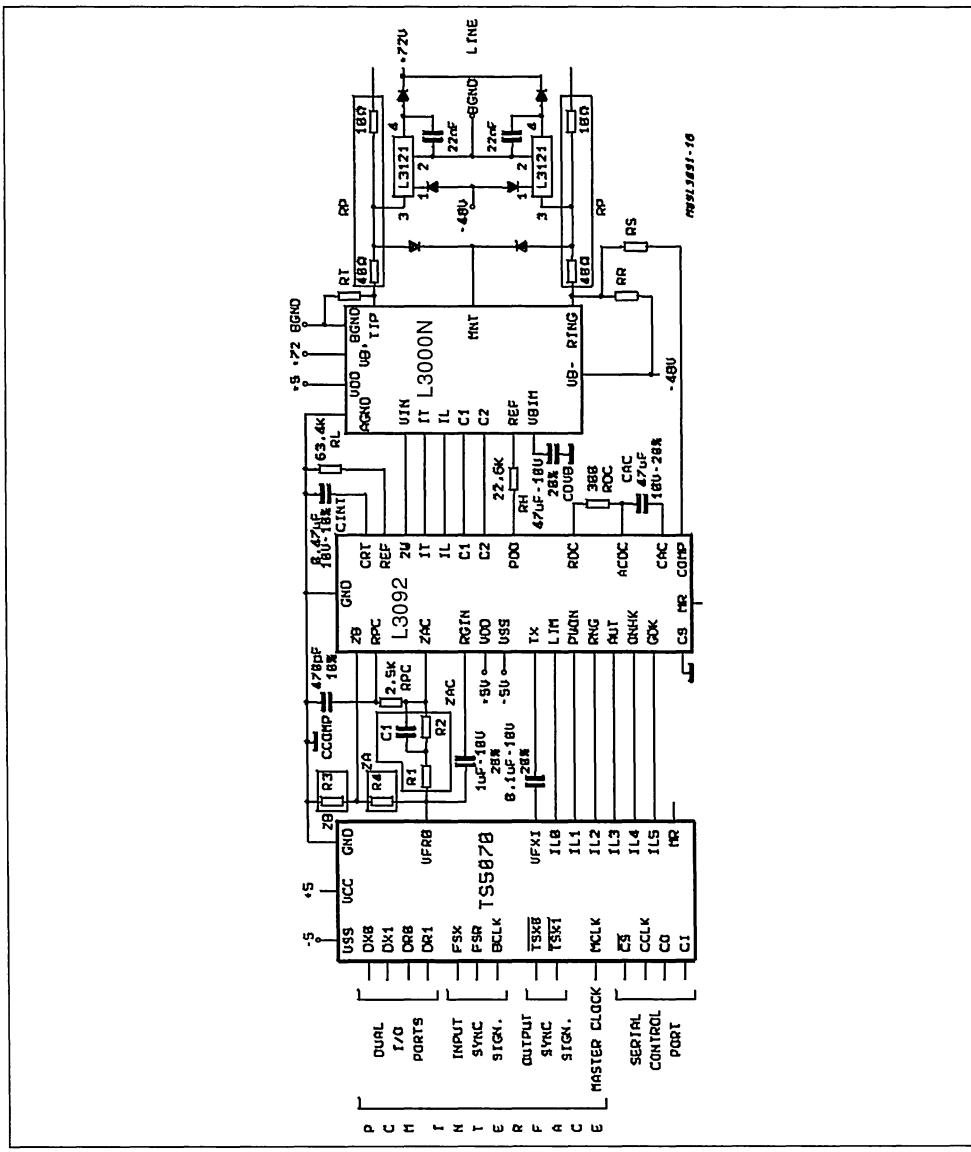
The complete circuitry needed to interface the PCM system highways to the subscriber line is shown in fig.7. The SLIC two chip approach allows to reduce drastically the number of external components, to save the centralized ringing generator, the ringing relay, the zero crossing ringing control and to implement the "message waiting" function. In addition the combination of the

L3000N/L3092 SLIC with COMBOII increase the system flexibility and performances. In particular the card controller can select by software:

- DC feeding currents (25/40/60mA)
- TX and RX gains (25dB range; 0.1dB step) -
- Balance networks
- Time slot assignment (up to 64x2 slots)

In addition the Test Mode implemented on L3092 in conjunction with COMBOII allows to realize a four step autoadaptive balance system.

Figure 7: Complete application circuit needed to interface a subscriber line with system PCM highways. Very low number of external components and high flexibility are achieved due to the SLIC two chip architecture.



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

L3845 FOR PABX AND MODEM LINE INTERFACE APPLICATIONS

by D. Salomoni

INDEX Page

1 INTRODUCTION

The L3845 is used for MODEM and PABX Line Interface applications. The circuit provides DC loop termination for analog trunk lines. The V/I characteristic is equivalent to a fixed voltage drop (zener characteristic) in series with an external resistance that determines the slope of the DC characteristic. An external low voltage electrolytic capacitor causes the circuit to exibit high impedance to all AC signal in the voice band frequency range (>20 Kohm). The OFF-HOOK status is detected when the Line Current is higher than 8 mA. In this condition a constant current generator is activated to supply an external device (typically an optocoupler) without affecting the DC/AC characteristics of the circuit. An additional function is provided in order to reduce the DC fixed voltage drop and the AC impedance (PULSE MODE) This function can be used to respect some European Countries specifications during Pulse Dialling Operation.

2 GENERAL APPLICATION DESCRIPTION

Figure 1 shows the block diagram of L 3845. Figure 2 and figure 3 give two typical circuits for analog or digital applications. It is worth to note that the TRUNK TERMINATION CIRCUIT, together with the LS 5018 transient suppressor provides a compact and low cost module fully protected against lighting or overvoltage frequently present of telephone lines. When it is not necessary to make the protection against high energy pulses the LS 5018 can be replaced with two zeners of 16 V connected in series back to back. With the use of this circuit it is possible to terminate an analog trunk so that the DC current component is flowing in the TRUNK TERMINATION CIRCUIT. The AC signal through a low voltage capacitor it is provided to a low cost audio transformer and to the internal circuits. In figure 2 is indicated as example a simple hybrid circuit to made the 2 wire / 4 wire convertion. In figure 3 is indicated an application circuit with the SGS-THOMSON TS 5070 second generation COMBO that provide a programmable 2 wire / 4 wire convertion in addition to CODEC FILTER and other functions. In some European Countries it is requested that when the system is in PULSE DIALLING OPERATION the DC voltage at the Line Terminals during the MAKE pulses must be lower than the DC Line voltage in OFF-HOOK condition. By connecting the PULSE input (pin 3) to the reference ground V- (pin 2) the device reduces the DC charcteristic of about 1.5 V and the same time the AC impedance will decrease from 20 Kohm to a value equal to the external resistor (56 ohm typical). The PULSE function will be automatically set by the device if one capacitor is connected between pin 3 and pin 2 as will be explain in deep in the paragraf 3.2.d.

Figure 1: L3845 Trunk Interface

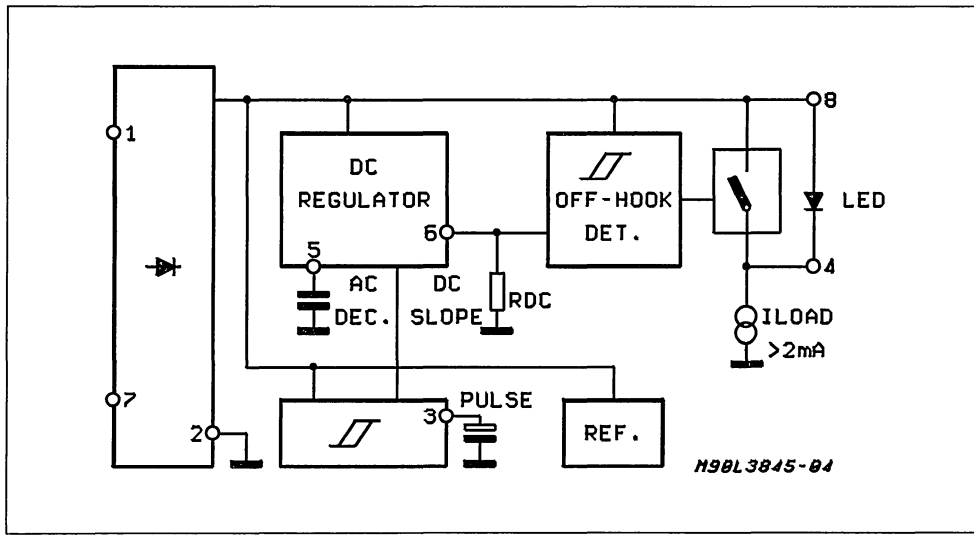


Figure 2

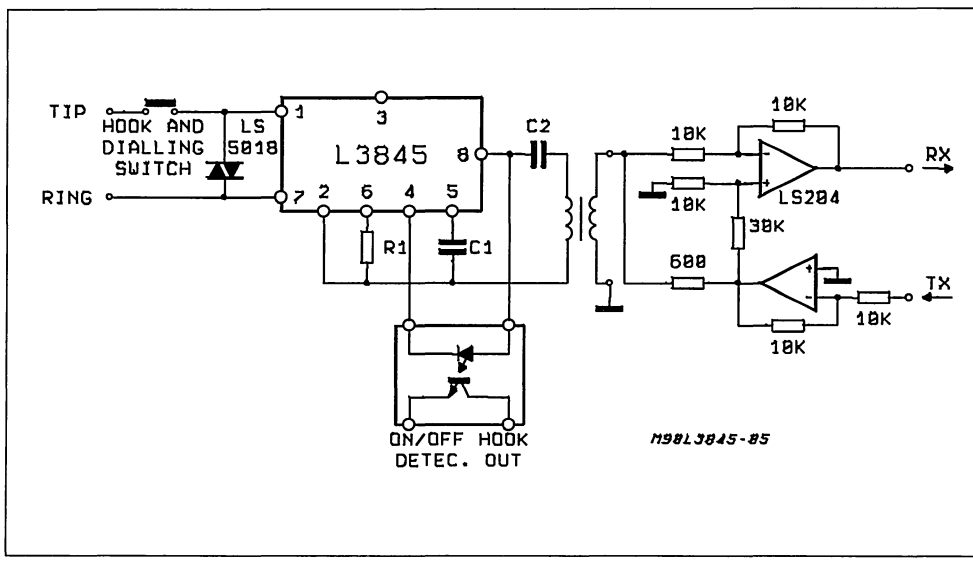
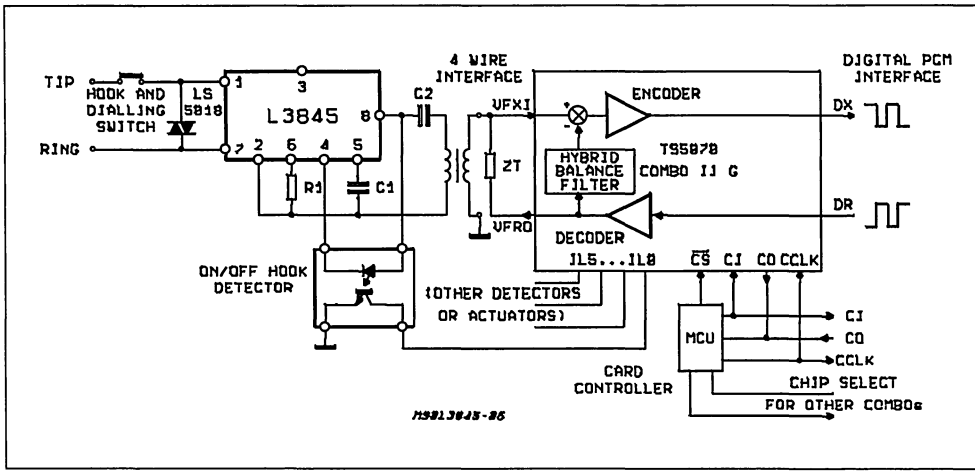


Figure 3



3 GENERAL CHARACTERISTIC DESCRIPTION

In this chapter are described the characteristics of L 3845.

3.1 DC CHARACTERISTICS

The DC characteristic are divided in three parts:

- DC characteristic in NORMAL MODE
- DC characteristic in PULSE MODE
- OFF-HOOK DETECTION.

3.1.a DC CHARACTERISTIC IN NORMAL MODE

The NORMAL MODE is set when pin 3 is left open. In this mode the AC impedance is high (typical 20 Kohm).
Figure 4 shows the typical DC characteristic for different R1 values. With a good approximation, the characteristic is linear for values of IL greater that 6 mA. The slope (ΔV_L / ΔI_L) of this characteristic is programmable and it is equivalent to the external resistor value. The test circuit is shown in figure 5.

Figure 4: DC Characteristics

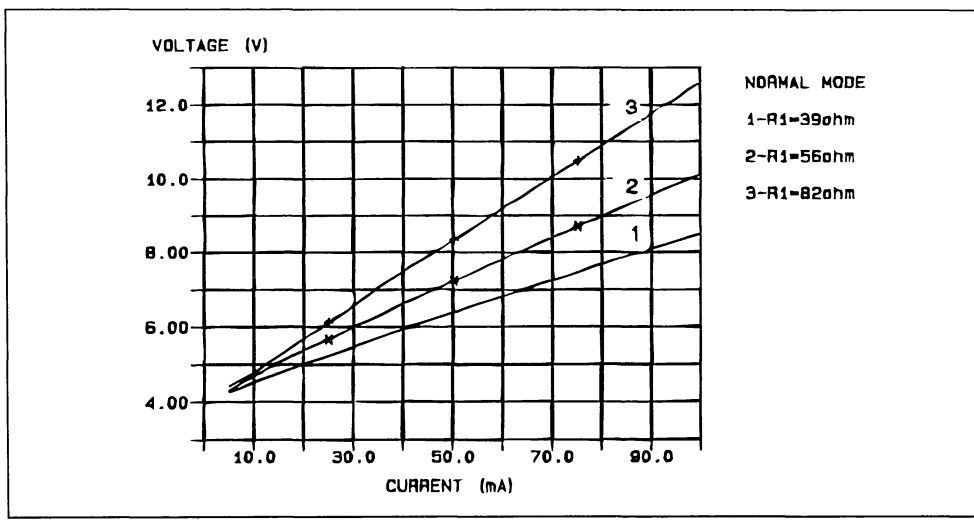
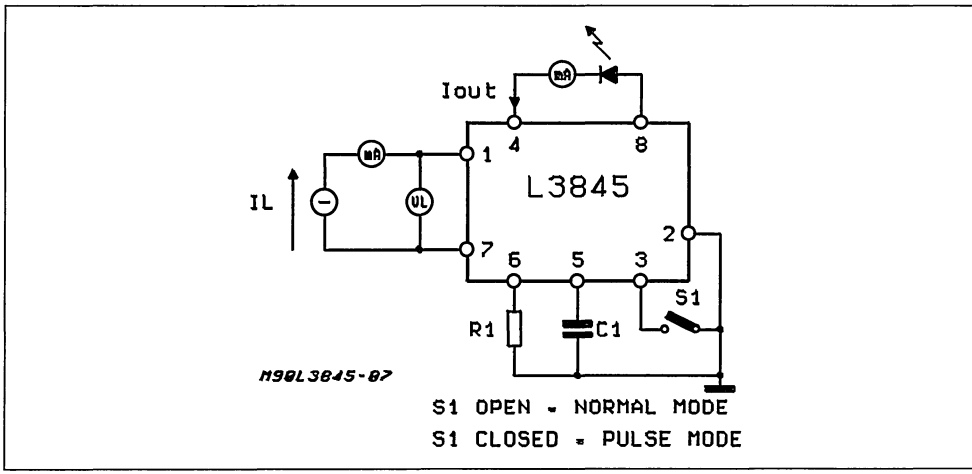


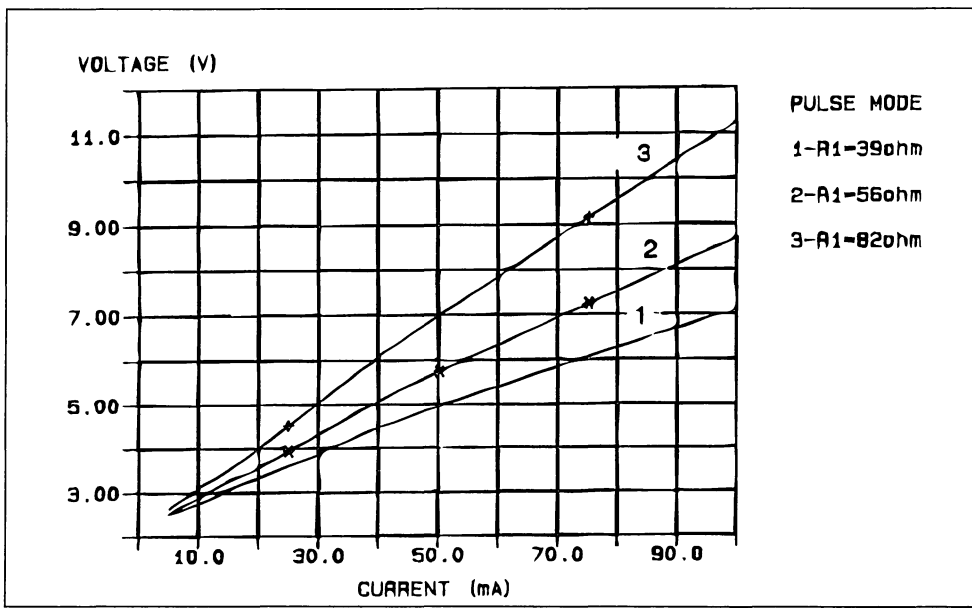
Figure 5



3.1.b DC CHARACTERISTIC IN PULSE MODE

This mode is set by connecting the PULSE input (pin 3) to V- (pin 2). In this mode the DC Line Voltage is reduced of about 1.5 V and the slope of the DC characteristic (/\VL / /\IL) is the same of the slope of the DC characteristic in NORMAL MODE, and equal to the external resistor R1 value. The test circuit is shown in figure 5 with S1 closed. Figure 6 shows the typical characteristic for different R1 resistor values.

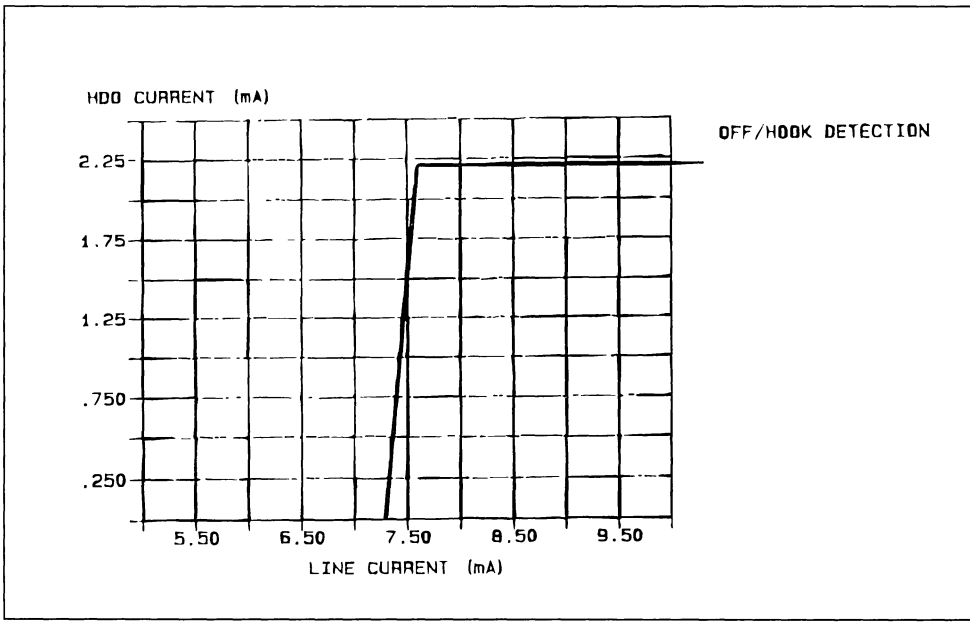
Figure 6: DC Characteristics



3.1.c OFF-HOOK DETECTION CIRCUIT

The L 3845 has a circuit to detect the OFF-HOOK condition. When the Line Current is over than 8 mA the constant current generator at pin HDO (pin 4) is activated. Figure 7 shows the Output Drive Current at the output HDO (pin 4) versus the Line Current IL. This circuit has the same characteristic both in NORMAL and in PULSE MODE. The test circuit is shown in figure 5.

Figure 7: DC Characteristics



3.2 AC CHARACTERISTICS

The AC characteristics are divided in four parts:

- AC IMPEDANCE
- RETURN LOSS
- DISTORTION
- AUTOMATIC PULSE MODE

3.2.a AC IMPEDANCE

Figure 8 shows the AC IMPEDANCE of the device L 3845 for different Line Current values. Figure 9 shows the AC IMPEDANE for different C1 capacitor values and figure 10 shows the AC IMPEDANCE for different R1 resistor values. The test circuit is shown in figure 11.

Figure 8: Impedance

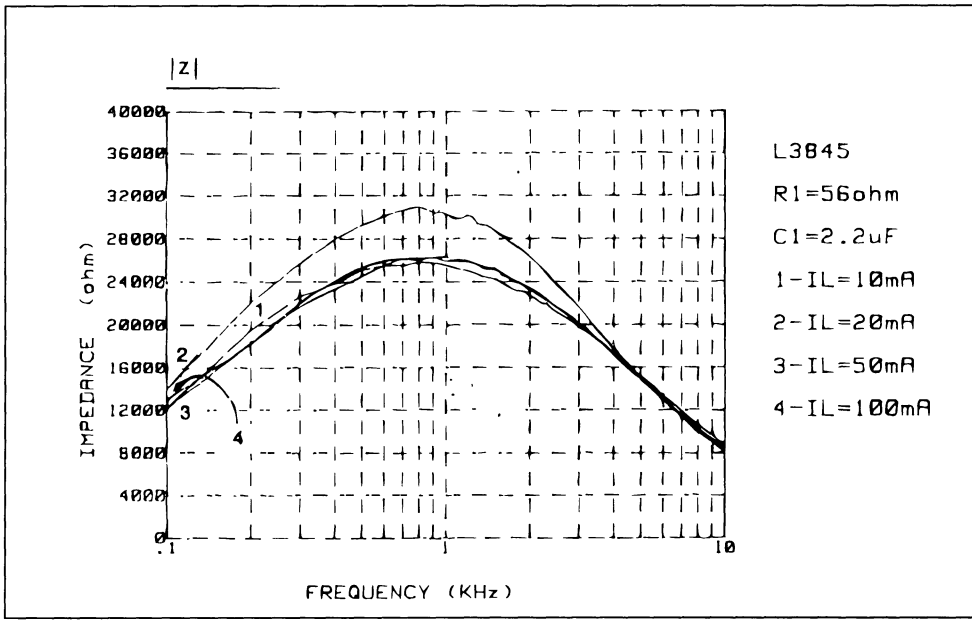


Figure 9: Impedance

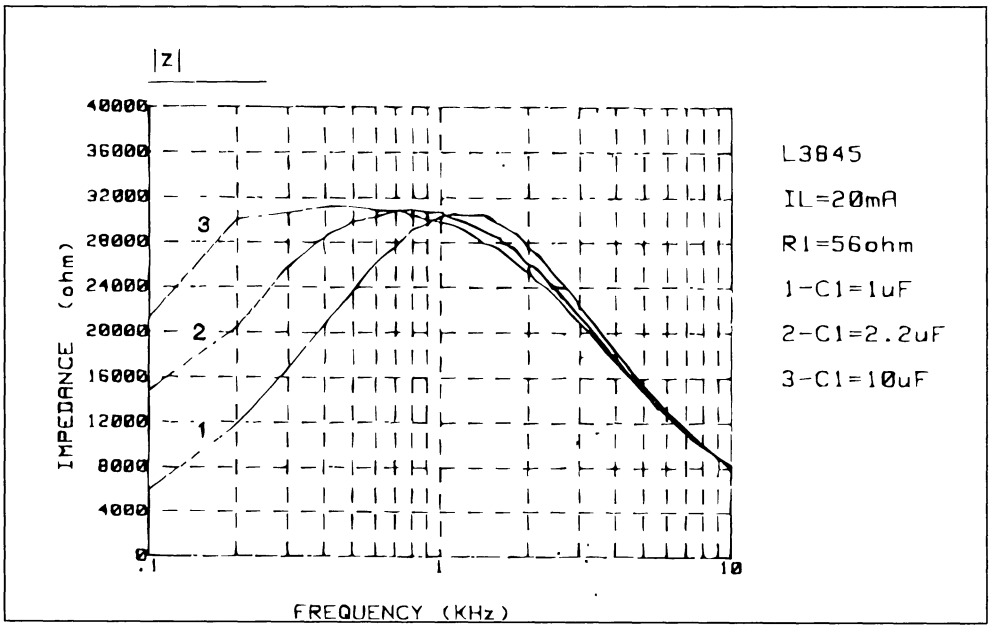


Figure 10: Impedance

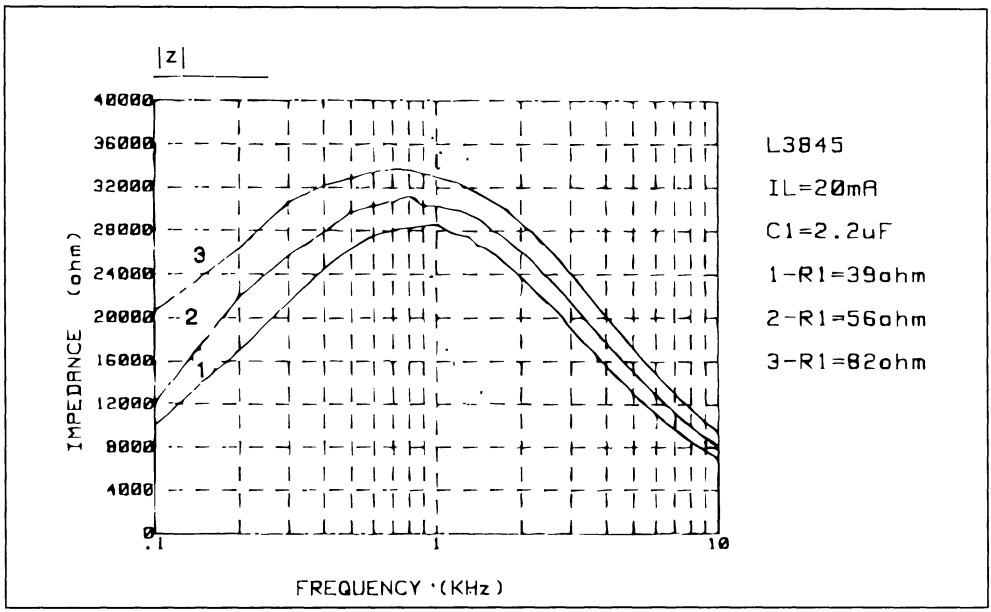
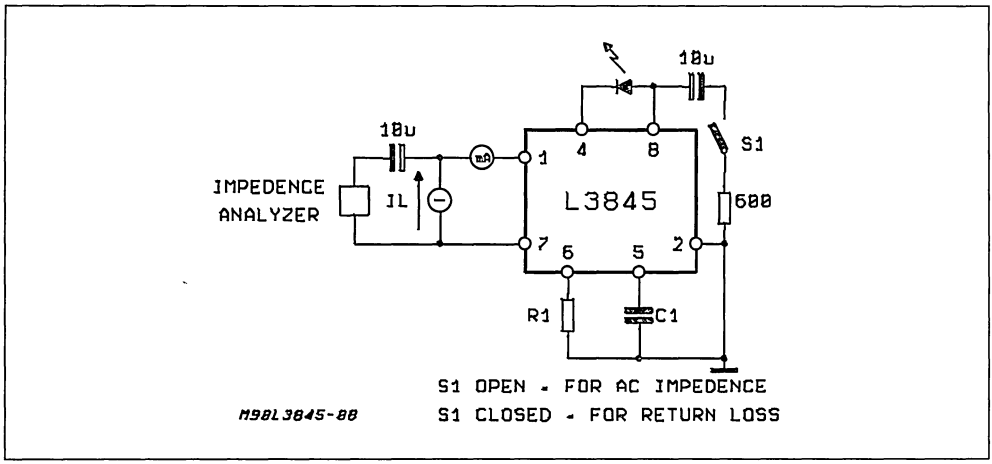


Figure 11



3.2.b RETURN LOSS

Figure12 shows the RETURN LOSS referred to 600 ohm impedance for different C1 capacitor values. Figure 13 shows the RETURN LOSS referred to 600 ohm impedance for different R1 resistor values. The test circuit is shown in figure 11 with S1 closed. The definition of the RETURN LOSS is:

$$RL = 20 \log \frac{|Zout + 600|}{|Zout - 600|}$$

Figure 12: Return Loss

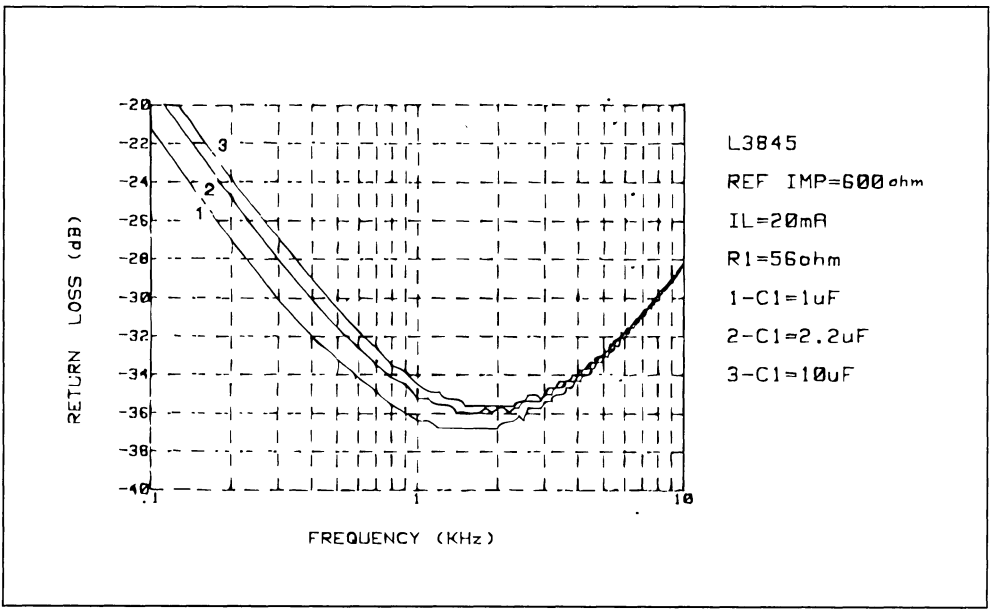
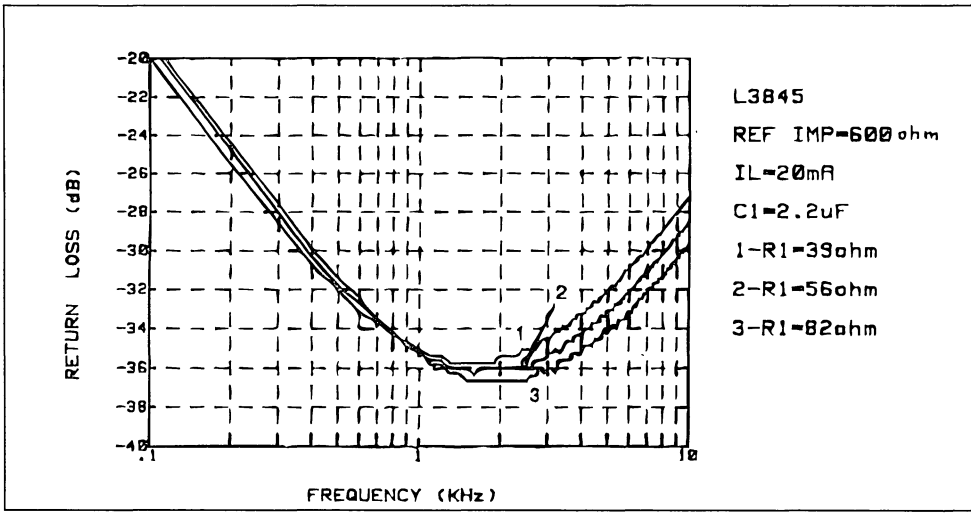


Figure 13: Return Loss



3.2.c DISTORTION

The measurements had been performed using the test circuit of figure 14. Figure 15 shows the maximum amplitude of the input signal between the pins 1-7 in order to measure a Total Harmonic Distortion less than 2%. It is possible to improve this performance connecting a resistor R2 in parallel to capacitor C1. A typical value for R2 is 300 Kohm. By this way, it is possible to increase the DC characteristic and therefore to improve the signal swing. The resistor R2 will influence also the slope of the DC characteristic, that will become:

$$\frac{/\backslash V_L}{/\backslash I_L} = R_1 \left(1 + \frac{150\ \text{Kohm}}{R_2} \right)$$

and the value of the AC impedance in the low frequency range.

Figure 14

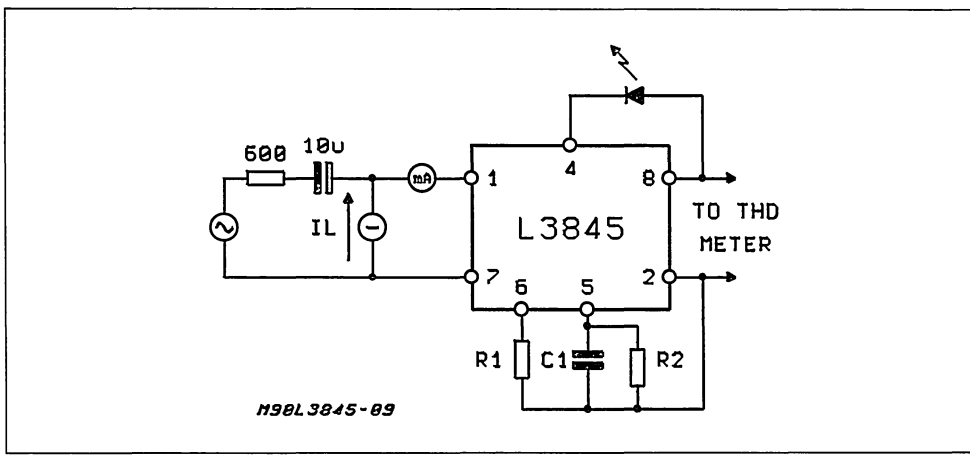


Figure 15: Max. Line Voltage

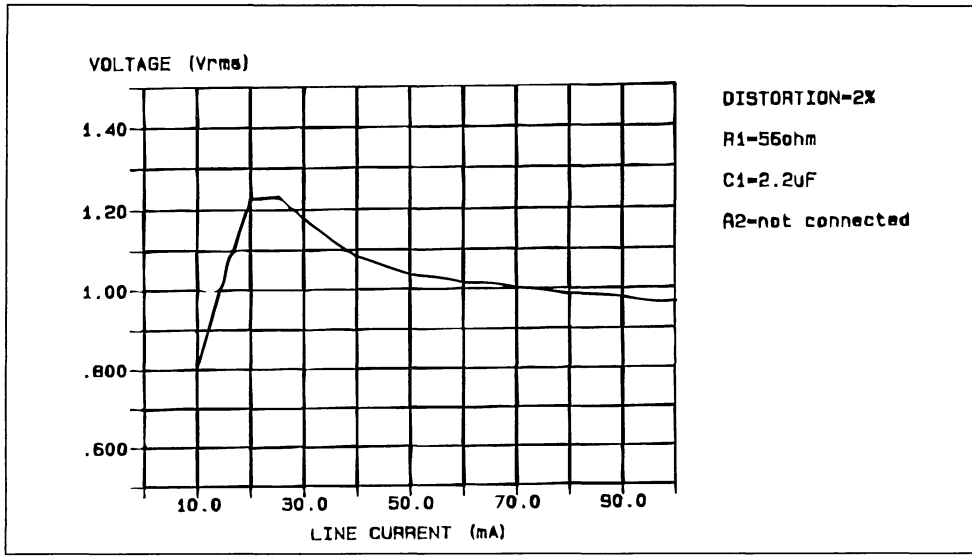


Figure 16 shows the MAX. Line Voltage versus Line Current for a THD = 2% and with R2 = 300 Kohm and different R1 resistor values. Figure 17 shows the DC characteristic with R2 = 300 Kohm and for different R1 values. Figure 18 shows the AC impedance with R2 = 300 Kohm and for different R1 values. When the signal is applied between the pins 8-2 and the THD is measured at pins 1-7 the results are exactly the same.

Figure 16: Max. Line Voltage

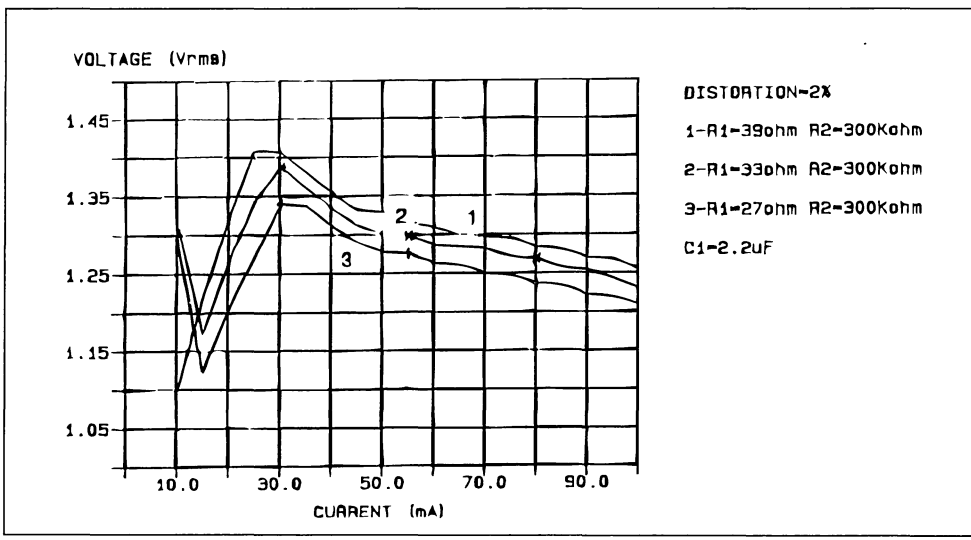


Figure 17: DC Characteristics

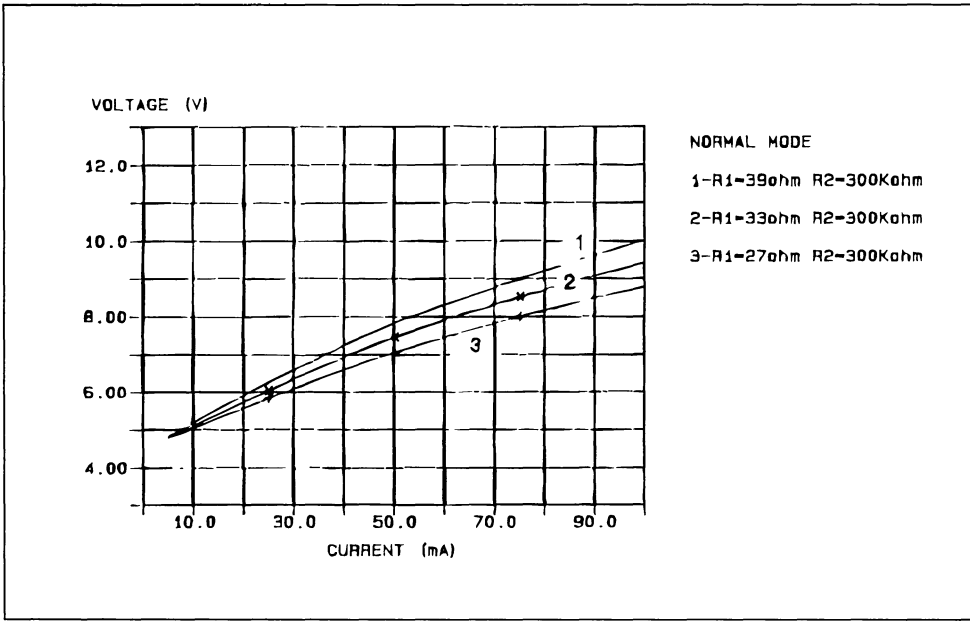
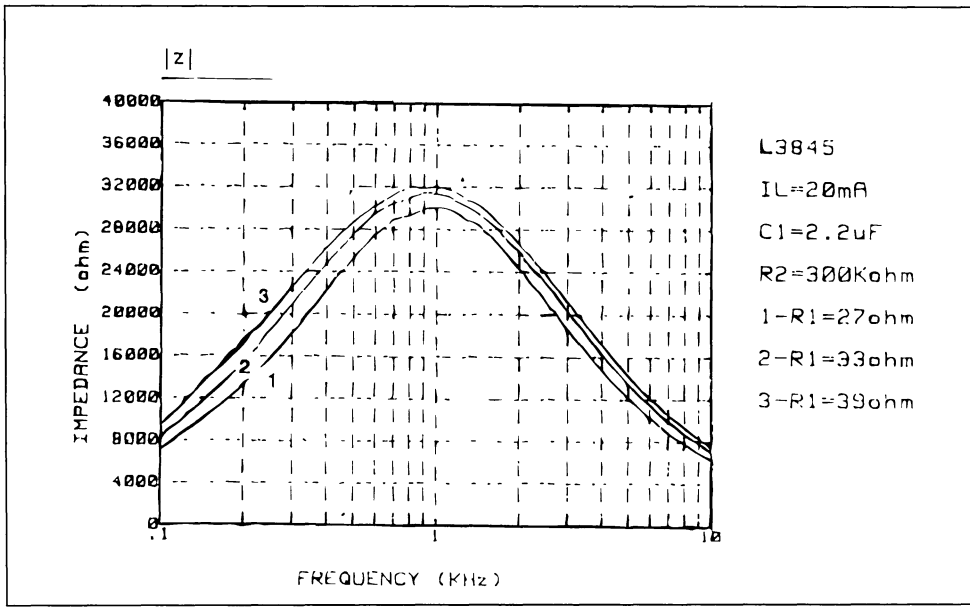


Figure 18: Impedance



3.2.d AUTOMATIC PULSE MODE

The PULSE MODE is set by connecting the input PULSE (pin 3) to the reference ground V- (pin 2). To set L3845 in NORMAL MODE the PULSE input (pin 3) must be open. The device is able to set automatically the PULSE MODE, without any external operation, by connecting a capacitor C2 between pin 3 and pin 2, the suggested value for C2 is 1 µF. In this case when the device recognise an ON-HOOK condition (I_L < 8 mA) automatically it goes in PULSE MODE. The delay time t1 to go from NORMAL MODE to PULSE MODE is about 0.8 mSec with C2 = 1 µF. When the Line Current returns higher than 8 mA the device will stay in PULSE MODE for a time t2 fixed by external C2 capacitor. This time is long enough in order to keep in PULSE MODE the device during PULSE DIALLING at 10 Hz. The delay time t2 is determinate by the relationship:

$$t_2 = \frac{C_2 * (V_T - V_{BE})}{I_T}$$

Where VT is a voltage threshold of an internal comparator (VT = 1.4 V) and IT = 10 µA is the value of the internal current generator that charge the external capacitor C2 connected between pin 3 and reference ground V- (pin 2). For: C2 = 1 µF, t2 will be = 80ms. Figure 19 shows the waveforms at pins 8 and 3 for the function "AUTOMATIC PULSE MODE". Figure 20 shows the waveform between pins 1 and 7. Figure 21 shows the test circuit. From figure 20 you can see that the DC voltage at pin 1 during the MAKE pulses is 1.5V lower than the voltage in NORMAL MODE. In conclusion, how you can see, the device performs automatically the pulse function without any external device.

Figure 19: Automatic Pulse Mode

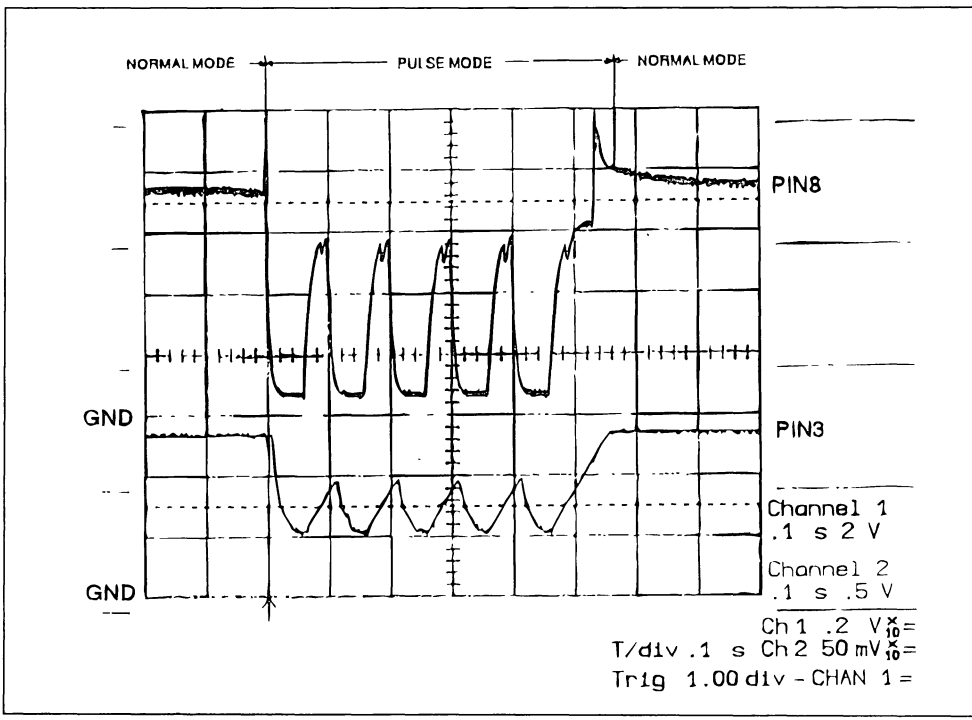


Figure 20: Automatic Pulse Mode

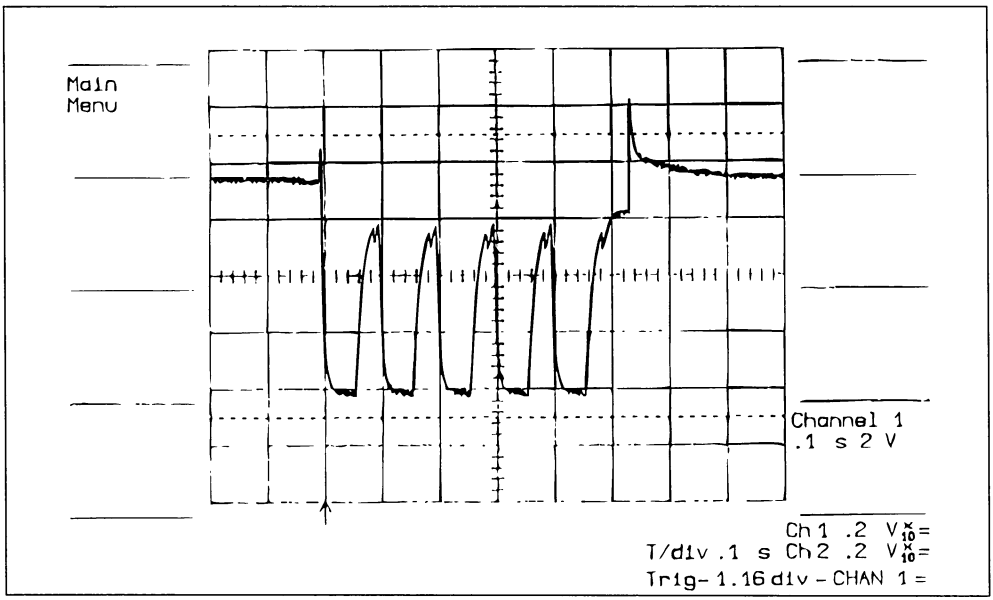
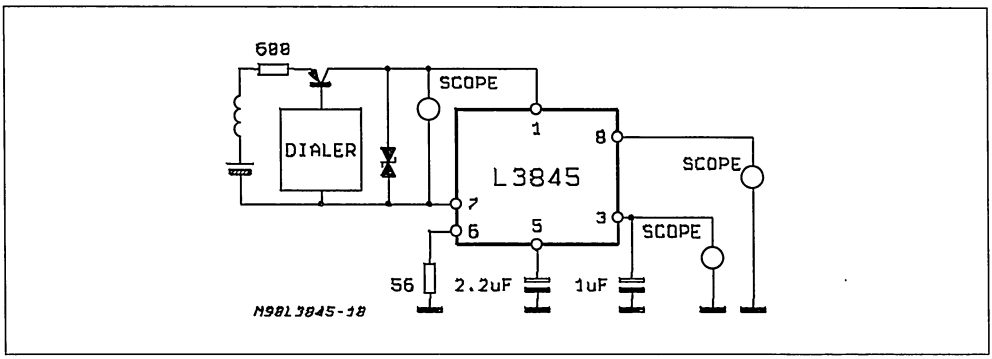


Figure 21



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

L3035 - L3036-L3037 MONOCHIP SLICs

by Arturo Vigano

CONTENTS

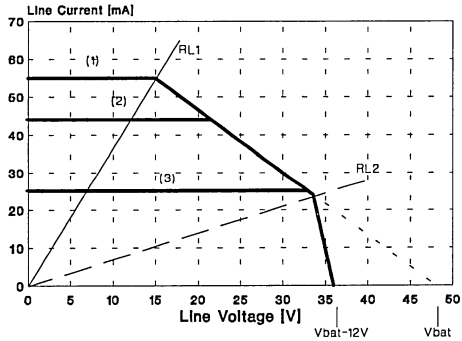
1. DC PERFORMANCES

1.1 DC FEEDING CHARACTERISTICS

1.1.1 Active Mode: (D0 = High, D1 = High)

Three different feeding regions are present (see Fig.1) and the operation point is related to the Line Resistance (length) to be fed.

Figure 1: Line Current vs. Line Voltage



1) Current Limiting Region.

Line Resistance > 0
Line Resistance < RL1 (Maximum Res. for Limiting region)

A constant current is supplied to the Line,indipendently of the Line Resistance .
The value of the current is selected out of three values according to the status of the control input ILIM:

ILIM	FEED CURRENT
Low	25mA
NC	44mA
High	55mA

2) Resistive Feeding Region.

Line Resistance > RL1
Line Resistance < RL2 (Maximum Res. for Resistive region).

The DC feeding behaves as a Voltage Generator with an RFEED Equivalent Series Resistance:the current is not constant as in the Limiting region, but decreases proportionally to the Line resistance.

This dependency allows the AGC operation on telephone side.

Equivalent Voltage Generator:

V = VBAT

RFEED = RDC/10 + 2RP

RDC/10 : synthesized DC resistance

2RP : series of two protection resistors

3) Low Impedance Region.

Line Resistance > RL2

The synthesized DC resistance becomes very low and the DC feeding,seen at TIP and RING Pins,behaves as an ideal voltage generator.
Seen at TIP and RING Terminals,a series resistance is added, due to protection resistors,connected between pin and terminal.

Equivalent Voltage Generator:

V = VBAT-12V

RFEED = 2RP

This region has been provided,not just for the low out impedance itself,but in order to have a 12V drop when Line Current is 0mA: it is necessary condition to allow sufficient output swing in ON-HOOK Transmition.

Varying with continuity the Line Resistance,from the Short to the Open Circuit,the three regions are passed through,without discontinuities of operation,changing from one to another.
AC operation is not affected and the correct functionality is not corrupted at the corners.

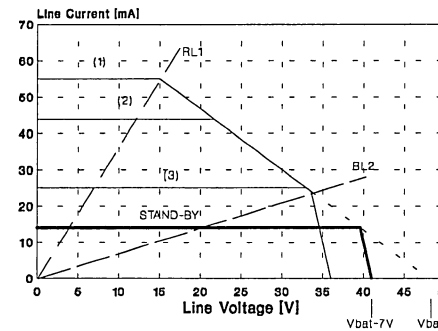
1.1.2 DC Feeding in Stand-by Mode.

(D0=High, D1=High)

In Stand-By mode,a constant current of 14mA is fed to the line (see Fig.2) up to the end of limiting region.
Then, a 0Ω impedance is shown at Tip and Ring output pins: the output impedance seen at Line-Card terminals is due to protection resistors Rp in series to the line.

A Vdrop 7V is still present when Il=0mA.

Figure 2: Line Current vs. Line Voltage



1.2 FORMULAS AND CALCULATION

- Feed Current: IFEED = f (RL)
  - Limiting ILIM
  - Resistive VBAT/(RFEED+RL)
  - Low Imp. (VBAT-12V)/(2RP+RL)

- Feed Resistance :

The value is defined by an external resistor RDC according to the formula:

RFEED = RDC/10 + 2RP

RDC =10 · (RFEED - 2RP)

- Maximum Line Resistance in Limiting region.

IL = VBAT/(RFEED+RL)
ILIM = VBAT/(RFEED+RL1)

RL1 = VBAT/ILIM - RFEED

Known the R/Km of the wire,the formula give the max length of the line that can be feeded with constant current.

- Maximum Line Resistance in Resistive region.

At the corner Resistive-Low Imp. must be:

IL = VBAT / (RFEED + RL)

and

IL = (VBAT-12) / (2RP + RL) -->

VBAT / (RFEED+RL2) = (VBAT-12) / (2RP+RL2)

developing:

RL2 = [VBAT · (RFEED-2RP)/12] - RFEED

Depending on values of ILIM, RFEED and RP the DC charcteristic of L303X shows different shapes: it can start with Limiting region and continue through Resistive and Low Impedance or start directly with Resistive or start in Limiting and entering directly to Low Impedance, without passing through the Resistive region.

Following examples will clarify the subject:

Example 1.

VBAT=48V RFEED=900Ω RP=50Ω

If ILIM= 56mA

RL1 = VBAT/ILIM - RFEED.

RL1 = 48/(56E-3) -900 < 0Ω (DC char. starts in Resistive region)

RL2 = [VBAT*(RFEED-2RP)/12] - RFEED.

= [48 · (900-100)]/12 -900=2300Ω

IL2= VBAT/(RFEED+RL2)

= 48/(900+2300)=15mA

If ILIM=43mA

RL1= 48/(43E-3) 900=216Ω

RL2=2300Ω

If ILIM=25mA

RL1= 48/(25E-3) -900=1020Ω

RL2=2000Ω

Example 2.

VBAT=48V RFEED=400Ω RP=60Ω

If ILIM=56mA

RL1=48/(56E-3) -400=457Ω

RL2=[48 · (400-120)]/12 -400=720Ω

IL2=48/(400+720)=42.85mA

When ILIM=43mA or ILIM=25mA , as their value is <IL2=42.85mA or very closed to this value,the DC charactristics will directly change from Limitation to Low Impedance region.

In this case:

RL2=(VB-12)/ILIM -2RP

If ILIM=43mA

RL2=(48-12)/(43E-3) -120=720Ω

If ILIM=25mA

RL2=(48-12)/(25E-3) -120=1320Ω

Given the Length of a Line and the Resistance per Km ,with the a.m. formulas the calculation of the operating point is immediate and also the definition of the DC feeding parameters.

1.3. SIGNALING

- OFF/HOOK detection.

When Stand-By or Active mode is set, the L303X monitors the status of the Line,forcing the output ODET (pin 18) of the Logic Interface as follow:

ODET = HIGH ON/HOOK

LOW OFF/HOOK

On the Line Card,when the controller detects ON-OFF/HOOK conditions it performs different operations, according to the status of the Slic:

SLIC STATUS	OPERATION
Stand-by	Forces L303X in Active mode when OFF/HOOK is detected
Active before conversation	Monitors ODET for dialing
Active during conversation	Stops conversation when ON/HOOK condition is detected, forcing the two Slics in Stand-By.

The OFF/HOOK condition is detected by sensing the Transversal DC current flowing from TIP to RING ,Line drive outputs.

When this current is higher than a threshold of 10mA, ODET is forced Low; 0.5mA below that threshold ODET returns High.

No low-pass filtering is provided: ODET output has to follow in real time the status of the Line .

Common Mode Current is not affecting the status of ODET.

Note: in RINGING mode,ODET signals the RING-TRIP detection; the subject will be further described in §.6.

- GND KEY detection.

When a DC common mode current ILL [defined as ILL= (IB-IA)/2 with IA=current sourced from TIP and IB=current sunk into RING] is greater than 5mA, the Ground Key condition is detected and the output OGK (pin20) of Logic Interface is forced Low.

As the Line,normally, can be coupled to Common Mode AC sources (Mains),in order to give immunity to GND KEY detection, a Low-Pass filtering is provided to the sensing circuit.
For that purpose, the CRT capacitor connected between CRT (pin17) and AGND is used.

The same capacitor and circuitry is used for RING TRIP detection (see § 6).

Note:

- OGK is not affected by the Transversal component.
- When TIP and RING have a DC conduction to GND with a Transversal component (|IA| ≠ |IB|), the OFF/HOOK condition is also detected (ODET=Low).

1.4 TIP OPEN MODE.

In Tip Open mode , with GST (pin21) input High, TIP is set in High Impedance and RING only can drive the Line.

RING output current capability is limited to 30mA.

With Line open the output voltage is typically :

VRING= VBAT + 4.5V = - 43.5V

In L3037, GST also controls the Polarity Reversal: see control interface table in §4.

2. AC PERFORMANCES.

The complete AC model of L303X Slic appears in Fig.3. In this § ,as a tutorial chapter,we refer to the simplified model of Fig. 4, for the AC parameters calculation.

In such a model the capacitors CCOMP (loop stability) and CAC (separation of AC from DC component of Line current) are not considered. In speech band in fact CAC can be considered a

Figure 3.

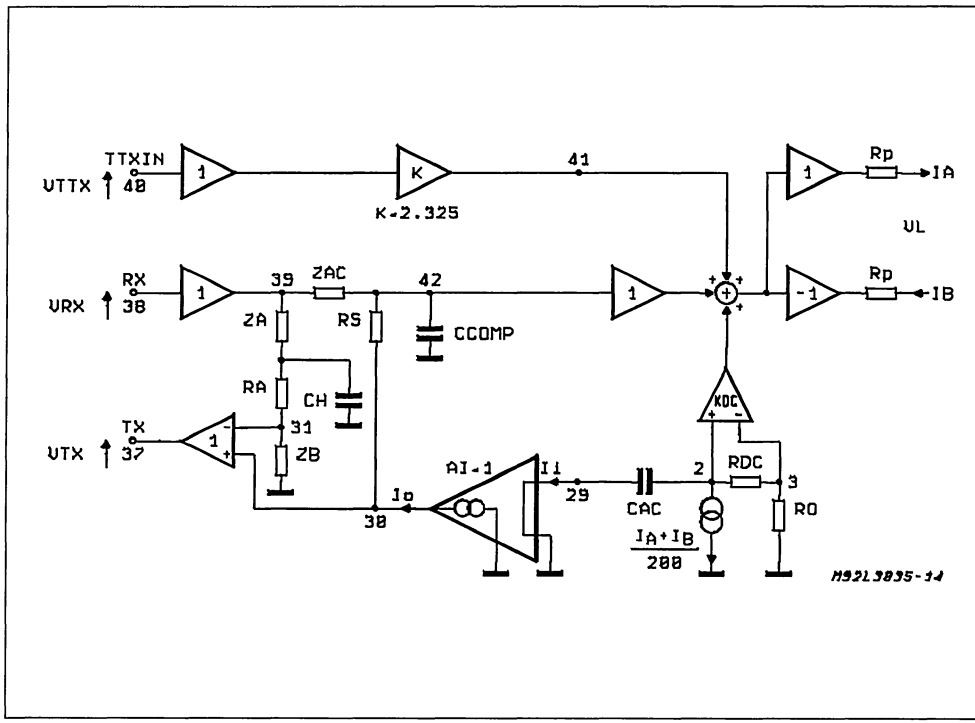
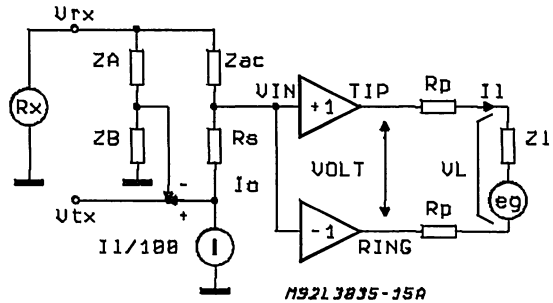


Figure 4.



short circuit and CCOMP an open circuit. The metering cancellation network RTTX and CTTX is also not considered.

SPICE simulation will show their influence on the AC performances (see AN501).

2.1 IMPEDANCE SYNTHESIS.

L303X provides an active synthesis of AC output impedance real or complex:

VOUT= 2 · VIN=2 · ZAC · IL/100

ZTR = VOUT/IL = ZAC/50 Equivalent Impedance at TIP-RING pins of the IC.

Considering the protection resistors Rp,the impedance shown to the Line is:

ZS= ZTR + 2Rp

2.1.1 Examples (ZRL = Return Loss Test Impedance)

a)ZRL =600Ω
Rp=40Ω
ZS= ZTR + 2Rp = ZRL
ZTR = 600Ω-80Ω
ZAC = 50 · ZTR =26KΩ

b)ZRL =220Ω + (820Ω//115nF) (GERMANY)
Rp=40Ω
ZS = ZTR + 2Rp = ZRL
ZTR = 220Ω + (820Ω//115nF) - 80Ω
ZAC = 50 · ZTR= 7K + (41K//2.3nF)

c)ZL =900Ω + 2.12µF (USA)
Rp=62Ω

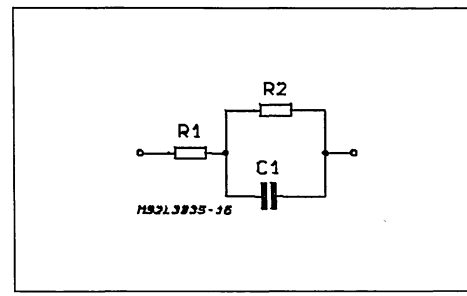
In principle, ZAC should be calculated as follow:
ZS = ZTR + 2Rp = ZRL
ZTR = 900Ω + 2.12µF - 124Ω
ZAC = 50 · ZTR=38.8K + 42.4nF

In fact this impedance cannot be used because, due to the internal chip architecture, the ZAC has to provide a DC path between pin 42 and pin 39 and it is not possible with a capacitor in series.

A different ZAC* has to be used and it must be equivalent inside the speech band (same amplitude and phase),in order to fulfill R.L. requirements.

The simplest network ZAC* that can replace the

Figure 5.



original one is shown in fig. 5.

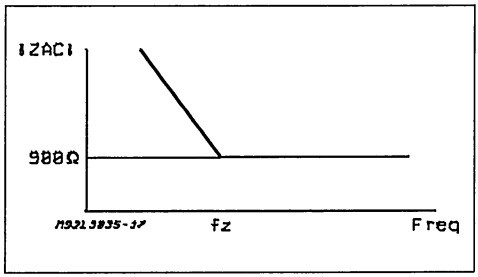
Calculation of ZAC*:

ZAC= R + C = 38.8K + 42.4nF

ZAC(ω)= (1+jωRC) / jωC ω = 2πf

The Bode diagram (see Fig. 6) shows a Zero at:
fz= 1/2πRC= 96.7 Hz

Figure 6.



ZAC* = R1 + (R2// C1)

ZAC*(ω)=(R1+jωC1R1R2+R2)/ (1+jωC1R2)

$\omega = 2\pi f$

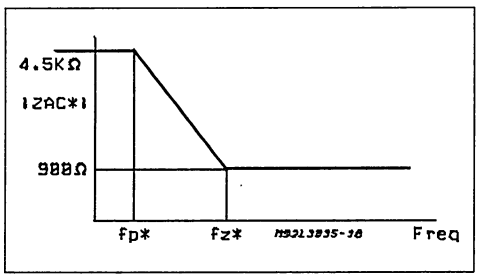
The Bode diagram shows pole at

fp*= 1/ (2πR2C1)

and zero at

fz* = (R1+R2)/ 2πC1R1R2

Figure 7.



From the conditions to be met :

R1= R

fz*= fz

R1+R2= RT

RT=225K

(RT is the resistance between pin 39 and pin 42; its value is related to the max allowed offset due to the input leakage current)

We obtain:

R1= R	R1= 38.8K
R2= RT-R	R2= 225K-38.8K= 186.2K
C1= C * RT/(RT-R)	C1= 51.2nF

Note that fp*= 1/2πR2C1= 16.7Hz affects ZAC* at very low frequency,outside the speech band. Inside the band, ZAC* can be considered with same frequency response as ZAC.

2.2 RECEIVE GAIN.

GRX= VL / VRX = 2 · [ZL / (ZL + ZS)]

GRX = 1 (0dB) if ZL = ZS

2.3 TRANSMIT GAIN.

GTX = VTX / VL (with VRX=0)

VTX = (IL / 100) · (ZAC+RS)
= [(VL / ZS) / 100)] · (ZAC+RS)

GTX = VTX / VL = (1/2) · [(ZAC + RS) / (ZS · 50)]
= (1 / 2) · [(ZAC + RS) · (ZAC + 50 · 2Rp)]

GTX = 1 / 2 (-6dB) if RS=50 · 2Rp

2.4 TRANSHYBRID LOSS.

THL = VTX / VRX (with EG = 0)

VTX = [VRX - (ZAC + RS) · IL / 100] - VRX · ZB / (ZA+ZB)

= [VRX - (ZAC + RS) · (VRX · GRX / ZL) / 100)] - VRX ZB / (ZA + ZB)

and :

THL = (ZL + 2 · RP - RS / 50) / (ZL + 2 · Rp + ZAC / 50) - ZB / (ZA + ZB)

TH L = ZL / (ZL + ZS) - ZB / (ZA+ZB)

THL = 0 if ZB / (ZA + ZB) = ZL / (ZL + ZS)

ZA = K · ZS
ZB = K · ZL

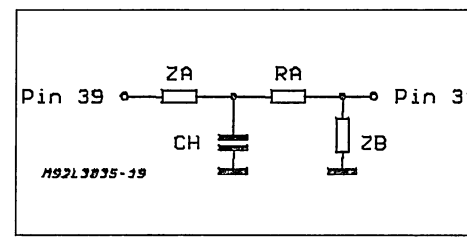
In fact it is reccomended to use K = 50, same scaling factor of ZAC

ZA = 50 · ZS = ZAC + RS

ZB = 50 · ZL

The capacitor Ccomp has not been considered. In fact, when high THL performances are required, Ccomp has to be taken in account. In that case the cancelling network of Fig 8A has to be used, where CH is the image of Ccomp.

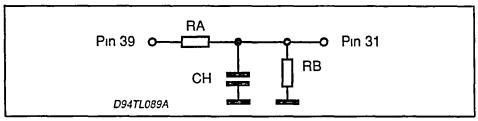
Figure 8A.



Where:
ZA = 50 · ZTR = ZAC
RA = 50 · 2Rp = RS
ZB = 50 · ZL
CH = Ccomp

NOTE: when ZL is the same specified in Gain and Return-Loss measurements, the cancelling network can be simplified as in Fig. 8B

Figure 8B.



Where:RA = RB = 50 · |ZL|
CH = Ccomp
The component count is reduced and THL performances are, in many case, acceptable.

Figure 9.

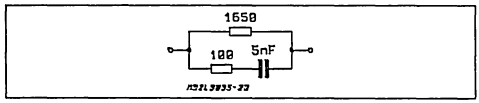
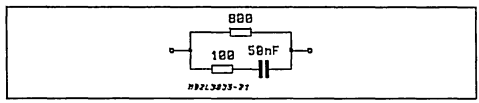


Figure 10.



2.4.1 Example

ZA and ZB calculation for USA:
ZL1 (fig. 9) and ZL2 (fig. 10) represent the two THL test networks.
$R_P = 62\Omega$

ZL1 = 1650Ω // (100Ω + 5nF) Loaded Line

ZL2 = 800Ω // (100Ω + 50nF) Unloaded Line

ZA = ZAC = 38.8K // (186.2K + 51.2nF)

RA = RS = 50 · 2Rp = 6.2K

ZB1 = 50 · ZL1= 82.5K // (5K + 100pF)

ZB2 = 50 · ZL2 = 40K // (5K + 1nF)

2.5 AC SIGNAL SWING AND DC CHARACTERISTIC ADJUSTMENT.

Quite often an optimization of the AC swing capability of L303X when operating with very long lines or low battery voltages is requested.

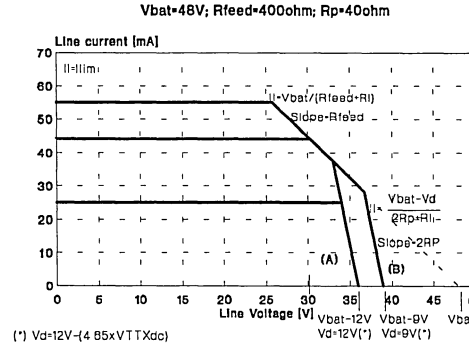
The following example will clarify about the subject. Let's calculate the output swing available in the condition:

IL = 21mA R-Loop = 600Ω Rp=50Ω VBAT=-24V

1) First of all the DC Feeding characteristic (see Fig. 11) must be modified.

To have the requested feeding current,the voltage drop must be reduced from 12V to 9V. The DC characteristic is translated from (A) to (B) by

Figure 11.



forcing at pin 40 a DC offset Voff:

Voff = (12V - 9V) / 4.65 = 645mV (see fig. 3)

With IL = 21mA the Slic operates in the DC Low Impedance region.

2) AC swing .

Figure 12.

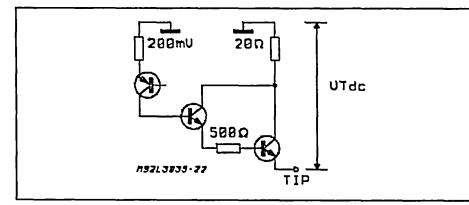


Fig. 12 shows a simplified schematic diagram of TIP output stage.

The DC voltage on TIP output is:

VTdc = -(9V - 1.7V) / 2= -3.65V

where 9V is the total voltage drop referred to the battery voltage (after a.m. modification of DC characteristic) and 1.7V is the VCE of external transistor in the resistive region.

Considering the circuit in Fig. 12 the maximum voltage that TIP can reach is:

VTmax = -(200mV + VSAT + VBE + 500Ω · IL/Hfe + VBE)

= -(200 + 100 + 700 + 100 + 700)mV

= -1.8V

Therefore the max AC peak we can get is:

VTpk = 3.65V - 1.8V = 1.85V

The same,in the opposite direction, is for RING output. So the peak voltage between TIP and RING available is:

VTRpk = 3.7V

This level is available at IC pins; at line terminals a lower value,due to protection resistors Rp,must be considered:

suppose ZL = 600Ω

VLpk = VTRpk · [ZL / (ZL+2Rp)] = 4.0V · [600 / (600+100)] = 3.2V

3. METERING PULSE INJECTION.

L303X provides an input (TTXIN pin 40) for Tele-Tax metering pulse injection. In §2.5 you can see how this pin can be used also for DC characteristic adjustment.

Typically the metering pulse is a 12KHz or 16KHz sinusoidal burst, with shaped start and stop, in order to minimize the interference in the phonic band.

In order to reduce the echo on TX stage and achieve a low output impedance, the cancellation network Zttx = Rttx + Cttx is provided in the 4 wire transmission path.

When Zttx matches the line impedance Z1 (at TTX frequency) the echo is minimized and the output impedance, is 2RP (due to protection resistors only).

Mismatching imply an increase of echo and output impedance

Fig. 13 and Fig. 14 show the equivalent model concerning the injection and cancellation of metering signal

Calculation of the cancellation network:

Vl = 2K · (1-G) · [(Zac + Rs) / Zac] · Vttx

where: G = [1 + Zac / K · Zttx] / {1 + Zac / [(Zl + + 2Rp) · 50]}

and K=2.3

the target is: Vtx = 0

that means: G = 1 ----> Zttx = 50 (Zl + 2Rp) / K

Note: higher attenuation of the TTX echo can be achieved; the simplest way is Low-Pass filtering the TX signal.

Figure 13.

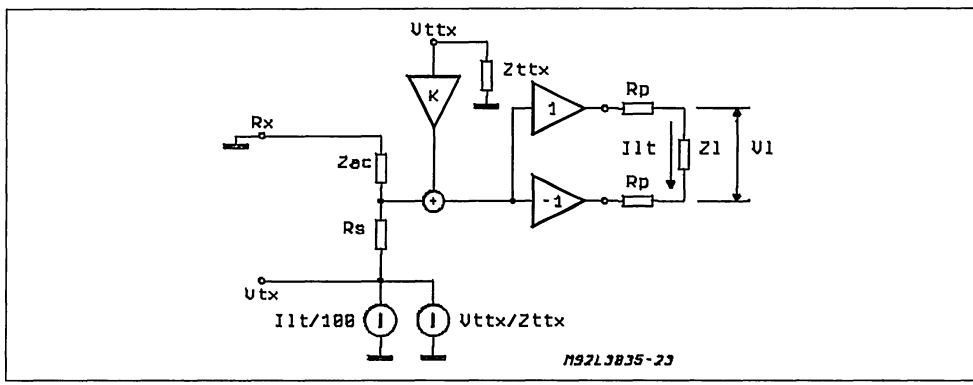
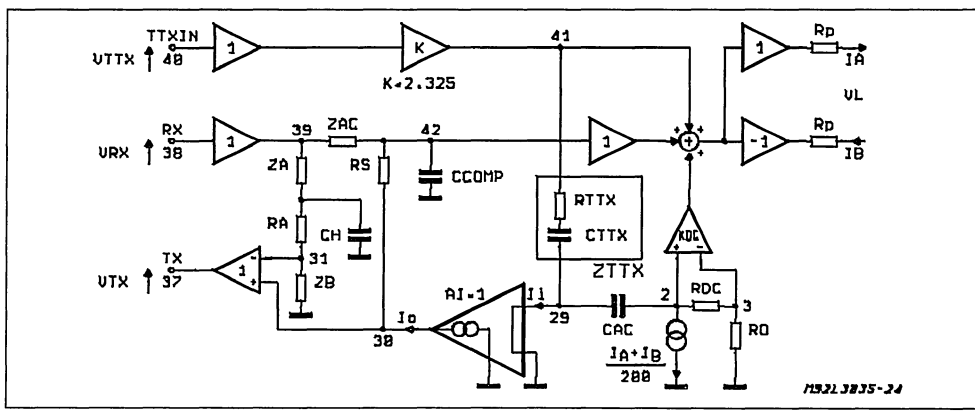


Figure 14.



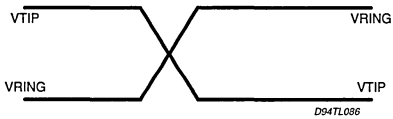
4. REVERSE POLARITY (L3037 only)

L3037 version provides the Reverse Polarity mode, selected by the control interface combination:

	D0	D1	GST	LIM
STAND-BY R.P.	1	1	1	X
ACTIVE R.P.	1	0	1	X

Reverse Polarity is not available in Ringing mode

AC characteristics are not affected; only the polarity of the DC voltage between Tip and Ring is reversed.
A linear shaped transition, see following figure, which dV/dT is defined by the capacitor CREV connected between the pin CREV and AGND, highly reduces the crosstalk level compared to a step reversal.



The CREV capacitance, depending on the dV/dT value, is given by the formula:

CREV = K / (dV / dT)
where $k = 2 \cdot 10^{-4}$ (± 10%)

NOTE: when the R.P. feature is not used, CREV pin must be grounded to AGND.

5. LONGITUDINAL BALANCE.

5.1 TRANSVERSAL TO LONGITUDINAL CONVERSION (T/L).

The transversal to longitudinal conversion ratio is defined in this way:

Tlc = 20·log (Vx / Vl) as shown in fig. 15

The ratio Vx / Vrx is indipendent from the AC feedback, in fact it depends from the line signal and it doesn't take in account the absolute value of line voltage. This ratio depends on the matching of the output amplifiers gain K1 and K2 and on the mismatch of the protection resistors.
The Tlck due to the mismatch of the of the output amplifiers gain can be computed as follows:

Vx = V · (K1 - K2) / 2

$$Vl = (K1 - K2) \cdot \frac{R}{R + Rp}$$

$$Tlck = 20 \cdot \log(Vx / Vl) = 20 \cdot \log\left(\frac{K1 + K2}{K1 - K2} \cdot \frac{Rp + R}{2R}\right) \quad (1)$$

The Tlce due to mismatch of the external protection resistors is :

$$Tlce = 20 \cdot \log \frac{E \cdot Rp}{2R} \quad (2)$$

Where E is the mismatch between Rp1 and Rp2
Rp1 = Rp(1 - E) and Rp2 = Rp(1 + E)
The complete formula of the transversal to longitudinal conversion is:

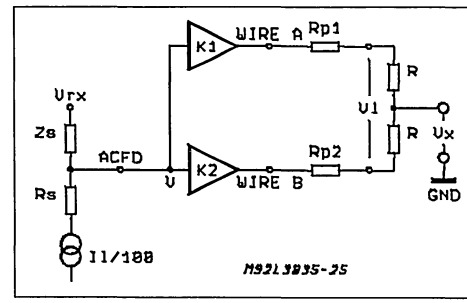
$$Tlc = 20 \cdot \log\left(\frac{K1 + K2}{K1 - K2} \cdot \frac{Rp + R}{2R} + \frac{E \cdot Rp}{2R}\right) \quad (3)$$

Note:
When the SLIC is in current limiting the unbalanced DC path provides an additional contribution. In that case the transversal to longitudinal conversion becomes:

$$Tlc = 20 \log \left| \frac{K1 + K2}{K1 - K2} \cdot \frac{Rp + R}{2R} + \frac{E \cdot Rp}{2R} + i \frac{Xc}{2R} \cdot \frac{Greg}{200} \right| \quad (4)$$

Where: Greg = 14
Xc = 1/ (2 · π · f · Cac)

Figure 15: Transversal to longitudinal conversion.



5.2 LONGITUDINAL TO TRANSVERSAL CONVERSION (L/T)

The longitudinal to transversal conversion ratio is defined as:
$Ltc = 20log\left(\frac{Vl}{Vin}\right)$ as shown in fig. 16.

where: $It = \frac{K \cdot (I1 + I2) + I1 - I2}{2}$; $Zac = Zs - 2Rp$

The transversal current value, It, depends on the precision reached by the current mirror circuit and on the mismatch of the two protection resistors.
The "Ltc"due to the mismatch of the internal circuit (K) is:

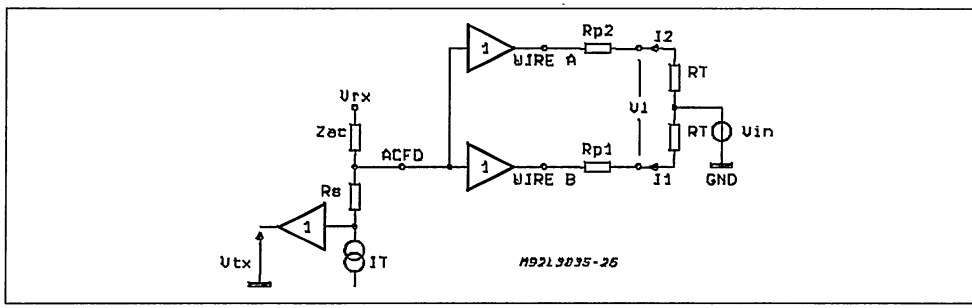
$$Ltck = 20log(K \cdot \frac{Zac}{Rt + Rp} \cdot \frac{Rt}{Rt + Rp + Zac/2})$$

The "Ltc"due to mismatch of the external protection resistors is:

$$Ltce = 20log(2E \cdot \frac{Rp}{Rt + Rp} \cdot \frac{Rt}{Rt + Rp + Zac/2})$$

Where E is the mismatch between Rp1 and Rp2
Rp1 = Rp · (1 + E) Rp2 = Rp · (1 - E)

Figure 16: Longitudinal to transversal conversion



Therefore the complete formula is:

$$Ltc = 20log\left(\frac{K \cdot Zac \cdot Rt + 2E \cdot Rp \cdot Rt}{(Rt + Rp) \cdot (Rt + Rp + \frac{Zac}{2})}\right) \qquad (4)$$

$K \leq 1.75$ E -3 for L3036
$K \leq 0.75$ E -3 for L3035

Example:

L3036 Rp = 40Ω 1% tolerance (E = 0.01), Zac = 520Ω, Rt = 300Ω

Assuming worst case for L3036 K = 1.75 E- 3

from the (4)

$$Ltc = 20log\frac{273 + 240}{204E3} = -52dB$$

6. RINGING.

With L303X an external ringing generator that injects the signal in the line through a relay is needed.

The Slic provides:

- Drive relay capability
- Activation/Deactivation of relay, syncronous with zero-crossing of ringing signal.
- Ring-Trip detection

L303X enters Ringing-Mode with the control inputs:

D0 = LOW D1= HIGH

When the ringing relay is activated REL (pin26) is forced Low and TIP and RING output stage become voltage generators, with current limitation, able to source and sink the line current injected by the external ring generator.This current,internally processed,allow the Slic to detect the status of the line (ON-OFF/HOOK).

6.1 RINGING INJECTION.

Different ways to inject the ringing signal are possible:

a)Battery backed (see Fig. 17)
The ring generator has one terminal connected to the battery. TIP current only is sensed for Ring-Trip detection.

b)Earth referred (see Fig. 18)
Dual configuration of a). The ring generator has one terminal connected to GND. RING current only is sensed for Ring-Trip detection.

c)Balanced (see Fig. 19).
The ringing signals injected on TRIP and RING wires are in phase opposition. SLIC terminals are disconnected from the line: Ring-Trip detection is obtained from additional hardware.

§ 6.4 will describe the subject.

Figure 17.

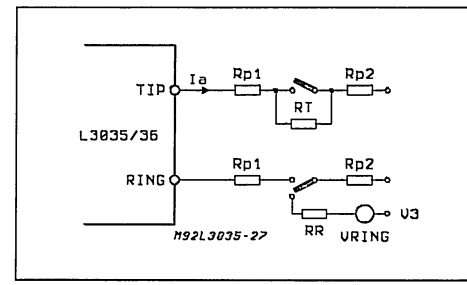


Figure 18.

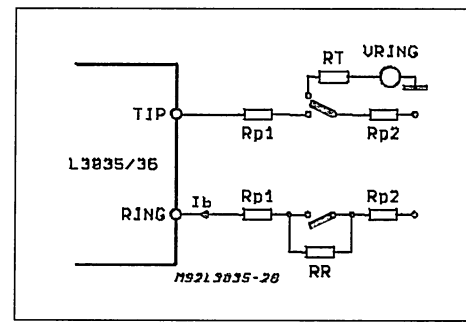
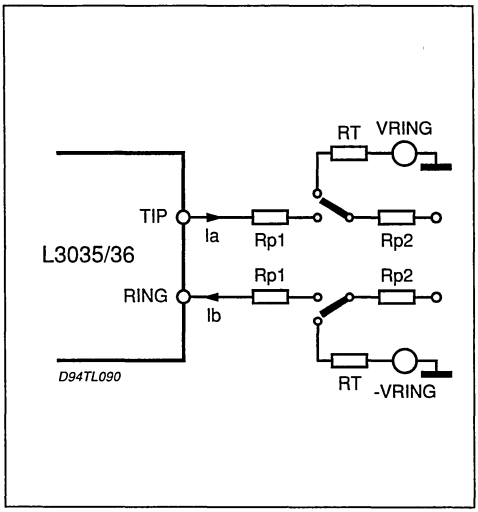


Figure 19



6.2 RING-TRIP DETECTION.

Ring-Trip condition is detected by sensing the currents Itip and Iring (see Fig. 20)

It = (Itip + Iring)/2

When the DC component of It >5mA the Ring-Trip condition is detected and L303X reacts:

- deactivating the ringing relay :REL (pin26) forced High
- forcing ODET (pin18) at Low level (OFF/HOOK).

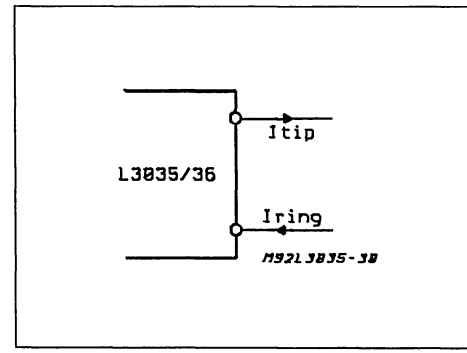
REL and ODET are latched and do not change opening the current loop. To leave this status Active Mode (D0=High D1= Low) has to be entered or in general, change status. Although the Ring-Trip detection uses ODET to signal the status of the line, there is a substantial difference respect to the ON-OFF/HOOK detection in Stand-By and Active mode.

In Ring-Mode and ON-HOOK condition an AC current is present in line: the Ring-Trip detection must ignore it and be dependent on the presence of a DC component only. The Ring-Trip detector reject the AC component by integrating the line current.

The detection threshold can be reached only if Il has a DC component. The consequence is that the response is not immediate (as in Stand-By or Active) but takes some delay time that is dipendent on the DC current value (i.e. line length).

AC rejection and delay time depends on capacitor CRT (Ring-Trip Capacitor) connected between pin17 and GND.

Figure 20.

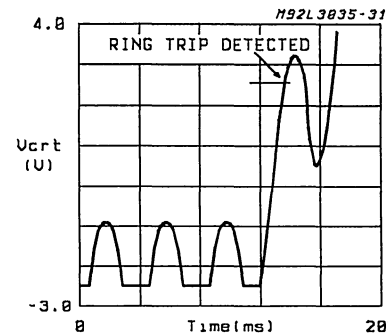


6.2.1 CRT calculation.

Referring to the battery backed case,the Ring-Trip is detected by integration the line current (sensed on Tip wire) on the CRT capacitor.

When the voltage on the capacitor exceedes 2.5V,the Ring-Trip is detected (see Fig. 21)

Figure 21.



CRT should be selected in order to avoid that during one half sinewave cycle, in On/Hook,its voltage Vcrt exceeds +2.5V (Ring-Trip Threshold).

Fig. 22 shows the correspondence between the CRT charging current Icrt and the line current I_L.

In Fig. 23 and Fig. 24 are reported the Line current and the CRT charging current Icrt, referred to the case:

Line Length = 1Km Load = 2 REN Freq.= 25 Hz Vring = 60Vrms
suppose CRT charged during one half-cycle with Icrt =100µA, its value must be:

CRT(100µA · 20ms) / 5V = 400nF

Of course this is a worst case, supposing I_L > 20mA for the whole half-sinewave. An optimized value will be lower and be calculated considering

the I_L in the worst condition:
maximum REN#, shortest loop,maximum ring level.

Figure 22.

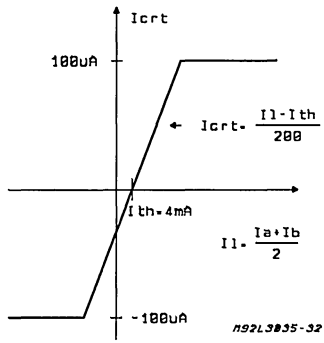


Figure 23.

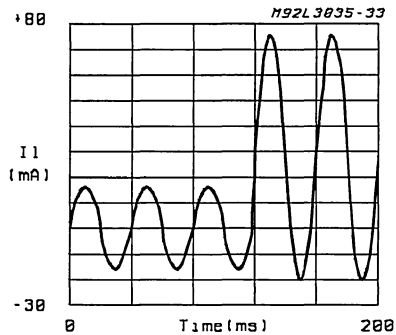
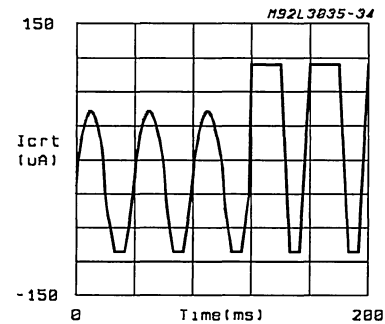


Figure 24.



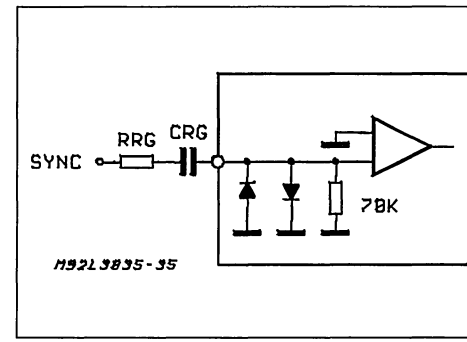
6.3 RELAY DRIVE SYNCHRONIZATION.

L303X provides the possibility to synchronize the activation and deactivation of the relay with the zero-crossing of the ringing signal.
The synchronization improves the reliability of relay and reduces the level of interferences induced in the adiacent lines.

The synchronization is locked to the zero-crossing of the voltage signal at RGIN input (pin15) (see Fig. 25).

The current flowing in RGIN input has a positive phase respect to SYNC sinusoidal voltage,due to the RC impedance (RRG and CRG) in series.
The zero-cross at RGIN anticipates the SYNC zero-cross with the possibility to compensate the activation time of the relay.
Depending on the signal used as SYNC, three possibilities of synchronization can be considered: (we refer to the battery backed solution but the concept is general)

Figure 25.



1) Line Voltage Synchronization (see Fig. 26):
SYNC = Ringing Generator Voltage

Activation and deactivation of relay happen at ZERO VOLTAGE condition.

RRG = (Vring / 25μA) · cos(2 Fring · T 180°)

CRG = 25μA / [Vring · sin(2 Fring · T 180°) · 2πFring]

T = Relay response time
Fring= Ringing Frequency

2) Line Current Synchronization (see Fig. 27):

SYNC = Voltage drop on Tip side (image of the Line Current)

Activation of relay is not synchronized : before activation the synchronizing signal is disconnected. Activation happen immediately after L303X enter in Ringing Mode (D0 = Low D1 = High).

Deactivation happens at ZERO CURRENT condition.

RRGC = RRG / K

CRGC = CRG · K

where: K= |ZR| / RT

Figure 26.

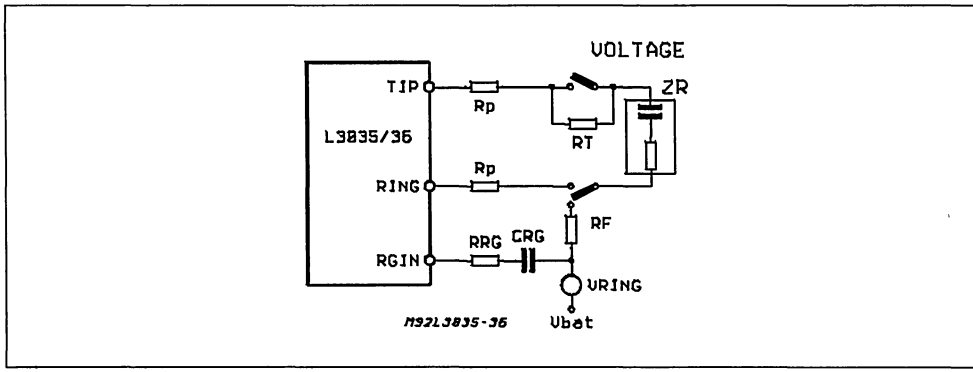


Figure 27.

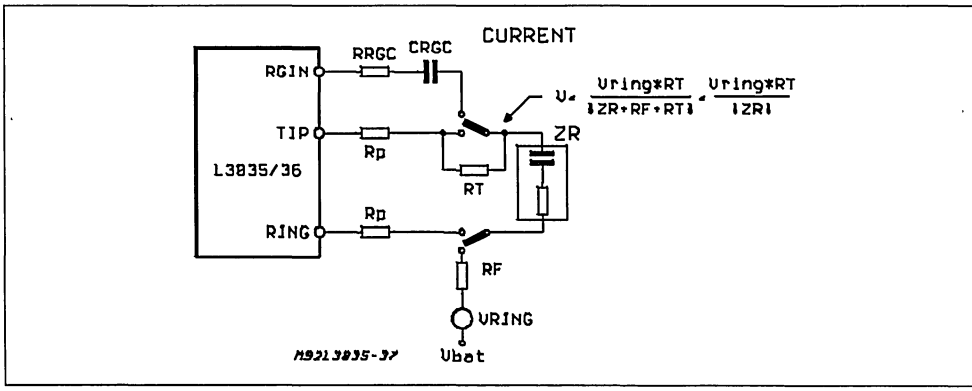
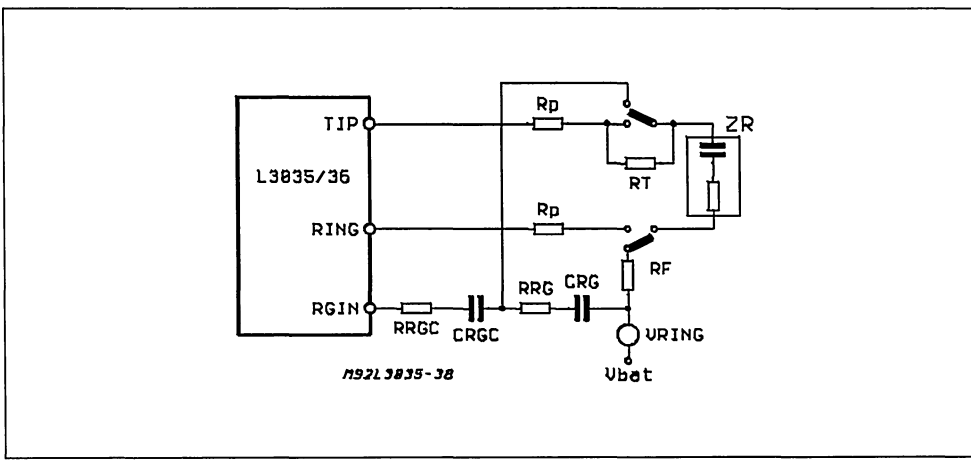


Figure 28.



3) Voltage and Current Syncronization (see Fig.28):

Activation takes place at ZERO VOLTAGE condition and deactivation happens at ZERO CURRENT condition.

RRGC = RRG / K

CRGC = CRG · K

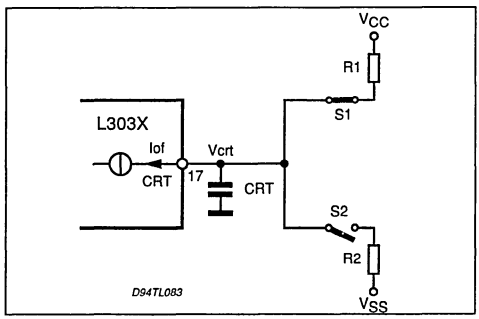
where: K = |ZR| / RT

6.4 BALANCED RINGING: Ring-Trip detection.

6.4.1 General information.

Although specifically designed for unbalanced Ringing injection, L303X can be adapted, with additional hardware, in order to manage the Ring-Trip detection with balanced injection.

Figure 29: Shows the Basic Equivalent Circuit



When the Line current is positive the switch S1 is On and S2 Off and the capacitor CRT is charged through the pull-up resistor R1. When the Line current is negative S1 is Off and S2 On,and CRT is discharged through the pull-down resistor R2.

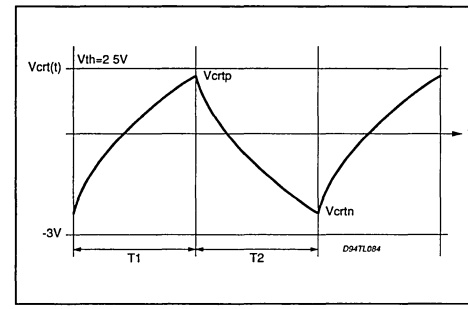
The internal current generator,at pin 17 (CRT) of L303X,sinks a current Iof of about 15μA to produce a negative voltage offset on CRT capacitor. When IL=0, both S1 and S2 are off,and the current generator forces CRT at a negative level that is clamped at -3V.

The voltage Vcrt(t) is a periodic waveform (see Fig.30) with exponentially shaped edges,that swings between a maximum (Vcrtp) and a minimum (Vcrtn) peaks that depend on Vcc, Vss, R1, R2, T1, T2 and Iof.

In On-Hook,T1=T2=T,and Vcrt must stay below a threshold Vth=2.5V to prevent Ring-Trip detection.

In Off-Hook,T1 > T2, Vcrt drifts up and Vcrtp must exceed Vth = 2.5V in order that L303X will detect a Ring-Trip.

Figure 30.



6.4.2. Calculation.

An approach is now given in order to properly calculate the value of R1,R2 and CRT that are functions of:

Battery Voltage	VBAT
Positive Voltage	Vcc
Negative Voltage	Vss
Ringing Level	Vrng
Ringing Frequency	Frng

To make the calculation easy let's refer to the particular case:

Vcc = -Vss = V and R1= R2 = R

Basically CRT and R are calculated through a successive approximation procedure that develops in three steps .

Step 1: suppose Iof=0 ,define a time constant R · CRT in order to have Vcrt with a peak value VM= V/2 (one half of the voltage swing available)
It corresponds to a condition half way between a very short and a very long time-constant

In case of very short time-constant Vcrt would be a square wave,reaching the maximum level available, producing a ring-trip detection anyway,regardless to the Hook status:it's a condition to be absolutely avoided.

In case of very long time-constant,Vcrt will be a continous level (due to the heavy low-pass filtering on ringing frequency) depending on the hook status. Ring-Trip detection should be possible but the detection time will be too long.

If T1 is the time duration of positive half wave and T2 of the negative,and given:

K1= -T1 / RC and K2= -T2 / RC

the positive and negative peaks of Vcrt, VM and Vm are given by:

a) $VM = V \cdot [1-2e^{K1} + e^{(K1+K2)}] / [1-e^{(K1+K2)}]$

b) $Vm = -V \cdot [1-2e^{K2} + e^{(K1+K2)}] / [1-e^{(K1+K2)}]$

In On-Hook: T1 = T2 = T and K1 = K 2 = K

and the formulas are simplified:

c) $VM = V \cdot [1-e^{K}] / [1+e^{K}]$

d) $Vm = -V \cdot [1-e^{K}] / [1+e^{K}] = -VM$

From c) comes the value of K:

$$K = Ln[(V-VM) / (V+VM)]$$

Given the ringing frequency and fixed a CRT value comes the first approximation value of R:

$$R = - T/(K \cdot CRT)$$

Step 2 : Iof is now taken in account.
The influence of Iof is to add a negative DC offset on Vcrt waveform (in step 1 has been considered the AC component) wich value is:

$VDC = -R \cdot Iof$

The real peak voltage of Vcrt is:
$Vcrtp = VM - R \cdot Iof$
In On-Hook, to avoid ring-trip detection we have to meet the condition (with 0.5V of margin):

$Vcrtp < Vth - 0.5V = 2.0V$

If the condition is not satisfied CRT value and R value must be modified:
to reduce Vcrtp must be reduced CRT and increased R (the contrary to increase it).

Besides, the internal Ring-Trip circuit of L303X needs, to detect a Ring-Trip, that a negative level of -3.0V has been previously present on CRT pin.
The condition is met if:
$Vcrtn = Vm - R \cdot Iof = -VM - R \cdot Iof < -3V$
If the condition is not met, Vcrtn can be reduced increasing R and reducing CRT.

Step 3 : Ring-Trip detection:
in Off-Hook the presence of a DC component in the line current increases the time duration T1 and decreases T2 according to the formulas:

$T1 = T \cdot [1+(2/\pi) \mid \sin^{-1} (Vbat / \sqrt{2}\, Vrng) \mid]$
$T2 = T \cdot [1-(2/\pi) \mid \sin^{-1} (Vbat / \sqrt{2}\, Vrng) \mid] = 2T-T1$

were: Vbat = battery voltage
Vrng = rms value of ringing voltage
T = 1/(2 · Frng) half period of the ringing signal

The value of VM calculated from formula a) gives the peak value of Vcrt in Off-Hook,that has to meet the condition:

$Vcrtp = VM - R \cdot Iof > Vth+0.5V = 3.0V$

in order to guarantee a ring trip detection (with a margin of 0.5V).
If the condition is not met,the wanted limit can be reached with a grater VM value :in that case a lower time constant must be adopted.

Example.

Given: Frng = 50Hz |VBAT| = 48V Vrng = 60Vrms
Vcc = -Vss = V = 5V

1): $K = Ln[(V-VM) / (V+VM)] =$
$= Ln[(5-2.5) / (5+2.5) = -1.1$

choosen a CRT=220nF

$R = -T / (CRT \cdot K) = 10ms / 220nF \cdot 1.1 =$
$41.4K\Omega$
(R = 43K2 will be next considered).

2): The negative offset is:
$Vdc = -R \cdot Iof = -43K\Omega \cdot 15\mu A = -645mV$
and the positive and negative peak value in On-Hook:

$Vcrtp = VM + Vdc = 2.5 - 0.645 = 1.85V$
$Vcrtn = Vm + Vdc = -2.5 - 0.645 = -3.15V$

The values meet the conditions:

$Vcrtp < 2.0V$ and $Vcrtn < -3.15V$.

3): Off-Hook condition:

$T1 = T \cdot [1 + (2/\pi)\sin^{-1} (Vbat / Vrng) =$
$= 10ms (1 + 0.64 \sin^{-1} (48 / 85) =$
$= 10ms \cdot 1.38 = 13.8ms$

$T2 = 2T - T1 = 20 - 13.8 = 6.2ms$
$K1 = T1 / R \cdot CRT = 13.8 / 9.46 = -1.46$
$K2 = T2 / R \cdot CRT = 6.2 / 9.46 = -0.66$

from a): $VM = 5 \cdot [1-2e^{(-1.46)}+e^{(-1.46-0.66)} /$
$/ (1-e^{(-1.46-0.66)} = 3.69V$
$Vcrtp = VM - Vdc = 3.69 - 0.645 = 3.05V$

Also this parameter fulfils the requirement for ring trip detection:
$Vcrtp > 3.0V$

Note: in case of iteration,to easily reach the solution,two concepts have to be kept in mind:

- fixed a time constant,the negative DC offset increases with the R value.
- fixed an R value,reducing the time constant increases the peak to peak value of the AC component of Vcrt.

6.4.3 Applicative solutions.

1) Fig. 31 shows the simplest solution in terms of components count. The current of the Line, wich is insulated form the Slic, is sensed through a dual optocoupler. The ringing current is sensed by the LEDs and a push-pull structure to charge and discharge the capacitor is made up with the foto-transistors.

When the line current is positive LED1 switches on FT1 charging the capacitor CRT ; when negative, LED2 switches on FT2 , discharging CRT.

The calculation in 6.4.2) can be directly applied;only the VCEsat of FT1 and FT2 has to be taken in account as Vcc and Vss reduction.

2) Fig. 32 and Fig. 33 show a not insulated solution that, although requiring higher component count,features high rejection to the longitudinal current.

Figure 31.

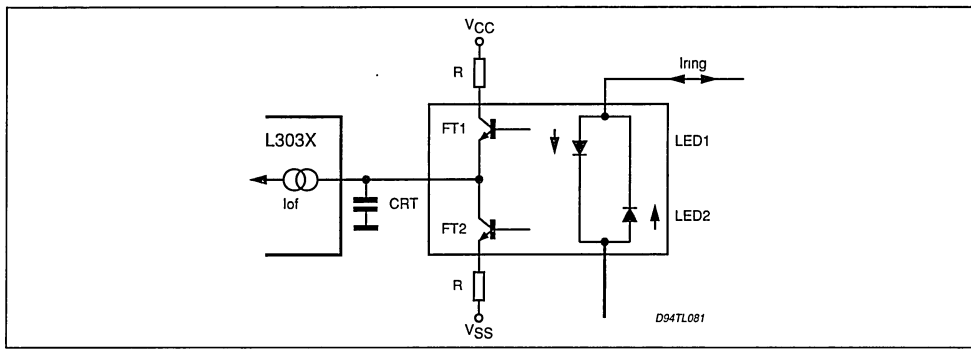


Figure 32.

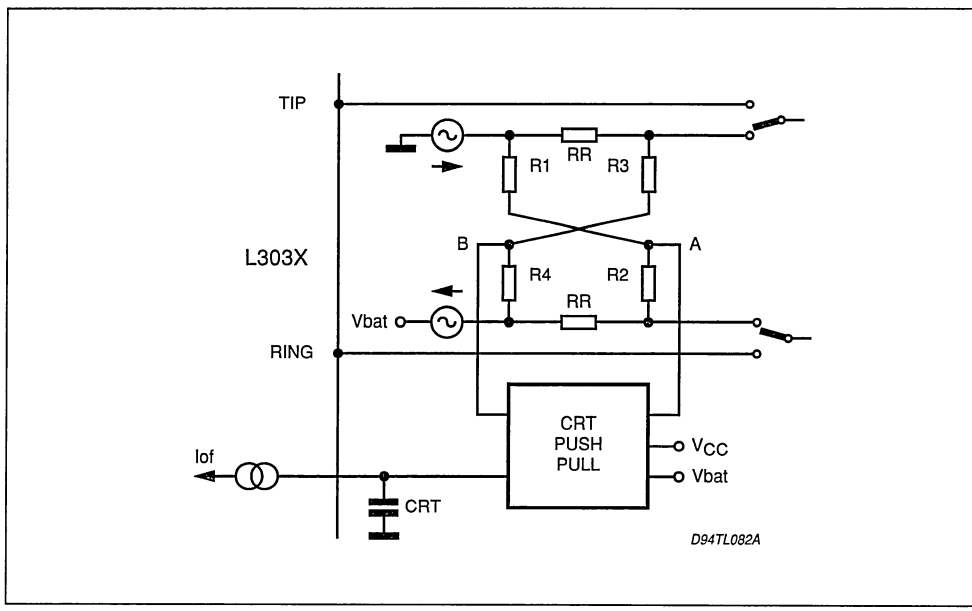
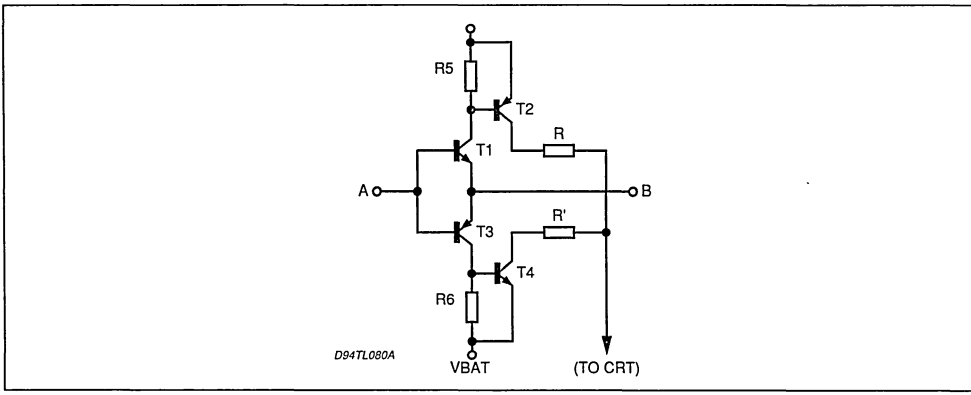


Figure 33: Balanced Ring Trip Detector 2. CRT Push Pull.



The bridge structure, R1/R2 and R3/R4,rejects the balanced AC voltage of the ringing generator at the nodes A and B,that are biased with a common mode DC voltage VA = VB = Vbat/2.
The differential voltage VAB= RR*Iring,is depending on transversal current only.
According to the direction of the Line current the transistors T1-T2 or T3-T4 charge or discharge the capacitor CRT.

In absence of ringing current the push-pull structure remains tri-state.

A and B nodes are biased at Vbat/2 and the negative supply of the push-pull is Vbat.

Procedure in 6.4.2) can be used again:

calculate CRT and R as though Vbat = -Vcc; then R' value is obtained by multiplying R by the factor Vbat / Vcc: R' = R · (Vbat / Vcc).

It's a first approximation value and in general a final adjustement is needed.

In order to minimize the power dissipation, R1 R2 R3 R4 must be high value resistors, compatibly with the capability to drive the push-pull.

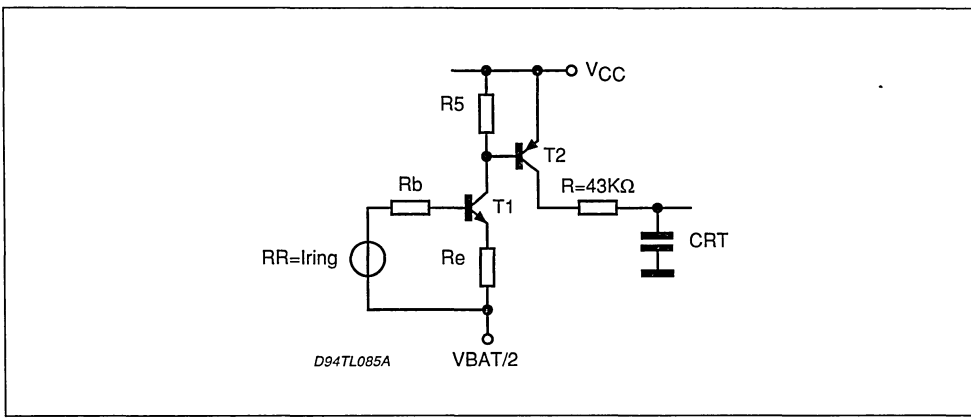
Example.

For calculation assume:

- hfe > 100 for T1 and T3 (linear operation)
  hfe = 10 for T2 and T4 (saturated operation)
- R5 = R6 = 300KΩ to maintain T2 and T4 in Off condition
- RR = 220Ω depending on the maximum ringing current allowed in case of short circuit.
- Ith = 10mA minimum current sensed;below this threshold the push-pull remains tri-state.

Let's consider the CRT charging cycle; the equivalent circuit is shown in Fig. 34:

Figure 34.



were: Rb= R1 / / R2 and Re = R3 / / R4

Ic2 = (Vcc - Vce) / R = (5.0-0.2) / 43 = 112µA

Ib2 = Ic2 / hfe = 112 / 10 = 11µA

IR5 = Vbe / R5 = 0.7 / 300 = 2µA

Ic1= Ib2 + IR5 = 11 + 2 = 13µA

$VABmin = RR \cdot Ith = 220\Omega \cdot 10mA = 2.2V$

disregarding the very low voltage drop on Rb:

VABmin = Vbe + (Re · Ic1)
and $Re \leq (VABmin-Vbe)/Ic1$

$Re \leq (2.2 -0.7) / 13\mu A = 115K\Omega$

$R2 = R3 = 2 \cdot Re \leq 230K\Omega$

Considering that in Rb flows a very low base current, R1 and R2 can be defined with higher value than R3 and R4.

The condition limiting the value is that the voltage drop Rb · Ib must be negligible respect to Re · Ie.

Rb = 2 · Re

can be used as a rule of thumb formula.

$R1 = R2 = 2 \cdot Rb = 4 \cdot Re \leq 460K\Omega$

With the calculated values the power dissipated by the bridge in stand-by condition is:

$PWB = PW12 + PW34 = Vbat^2 / (R1 + R2) +$
$+ Vbat^2 / (R3+R4) = 2.5mW + 5.4mW = 7.9mW$

Lower limit of the bridge resistance is defined by the maximum power dissipation PWB_{MAX} allowed.

$R1 = R2 \ (3/2) \cdot (Vbat^2 / PWB_{MAX})$

$R3 = R4 \ (3/4) \cdot (Vbat^2 / PWB_{MAX})$

7. POWER CONSUMPTION AND DISSIPATION.

In order to optimize the power consumption and consequentely the thermal dissipation, L303X Slic provides a regulation of the negative voltage VREG, with a series external transistor (see Fig. 35). This transistor, in addition to the VBAT ripple rejection, performs the basic function of sharing the power dissipation, reduces the amount due to the Slic and avoids, in most cases, the use of heat-sinks.

The power share depends on:

1)Rfeed (equivalent feeding resistance)

2)Line Resistance: that defines the operation point in the DC characteristic.

Fig. 36 and Fig. 37 show the power dissipation of Slic and ext. transistor as a function of the load (line resistance) for two DC feeding values:
Rfeed = 400Ω and Rfeed = 800Ω.

For a better understanding, some remarks have to be done. Referring to the DC characteristic:

1)In resistive region (Il < Ilim) the transistor has a VCE = 1.7V indipendent from Il value. In that region the transistor dissipation is:

Ptr = VCE · Ic

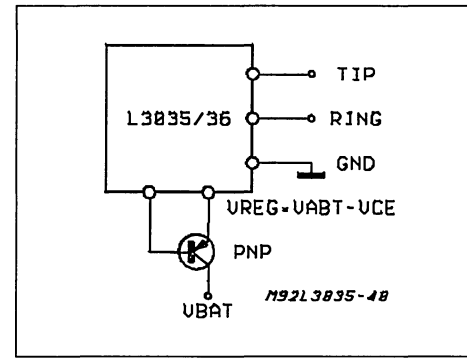
It is very low (low VCE and low Ic)

Increasing the line current Ptr increases proportionally but much less than the Slic dissipation Psl.

In resistive region the thermal contribution of the transistor is not important.

The function of the transistor is only the rejection of the ripple on Vbat.

Figure 35.



2)Once the limiting region is reached Il=Ilim,the transistor acts as a current regulator.
As RL decreases VCE increases, with the result that Ptr increases and Psl decreases.

In other words this kind of regulation provides the Slic of a variable battery that adapts its voltage to the length of the line; the exceeding voltage drops on the external transistor.

As shown in Fig. 36 and Fig. 37 the Slic has the maximum dissipation at the limit of the two operating regions.
In this condition we have Il = Ilim and maximum voltage Vtp between TIP and RING.
With lower line resistance Il remains constant but Vtp decreases and, consequentely, the dissipation.
For the transistor the maximum dissipation corresponds to a short-circuit on the line. In such a condition we have Il = Ilim and maximum VCE on the transistor.

The worst case dissipation values depend on the value of the feeding resistance Rfeed.

At higher Rfeed values correspond higher Psl and lower Ptr values.
From the diagrams we can see for I_{LIM} = 43mA

1) Rfeed = 400Ω Psl = 700 mW Ptr = 1500mW

2) Rfeed = 800Ω Psl = 1400mW Ptr= 800mW

This point is important and has to be considered for proper definition of on-board heat-sink copper area and transistor choice (Rth).

Figure 36: Power Dissipation/1

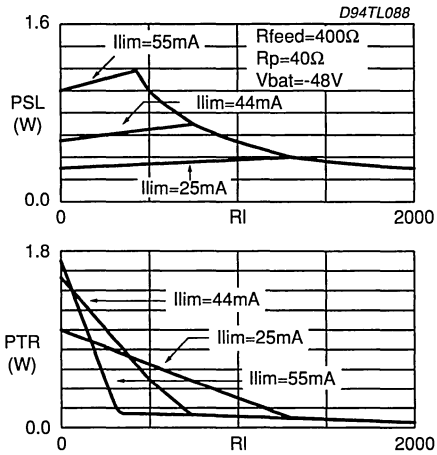
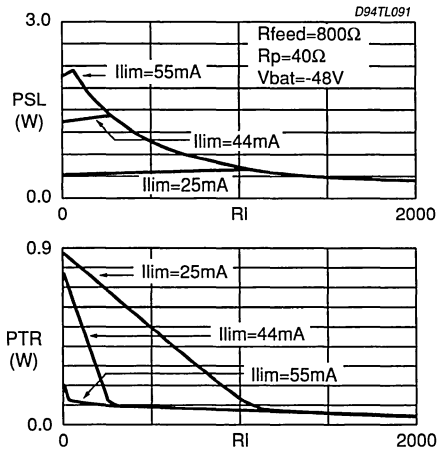


Figure 37: Power Dissipation/2



7.1 PACKAGE.

L303X is assembled in PLCC(34+10)
Ten pins, pin10 to pin14 and pin32 to pin36, are an extension of the frame and give a good contribution to heat dissipation when soldered to an on-board heat-sink.

Fig. 38 and Fig.39 show the diagrams:

Figure 38: PLCC 34+5+5 - Rth(j-a) on PCB vs PCB heat sink.

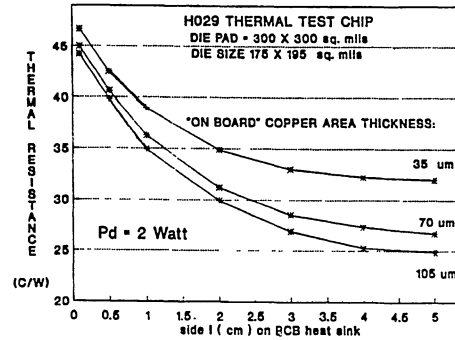
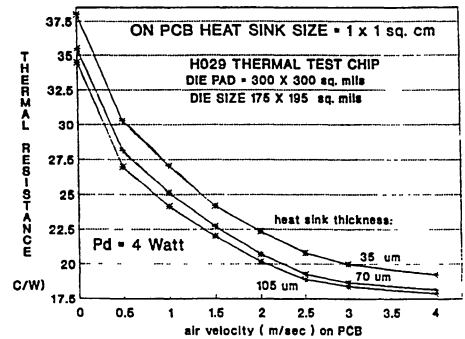


Figure 39: PLCC 34+5+5 - Rth (j-a) vs. air flow.



EXAMPLES:

ex1: Ilim = 25mA, Rfeed = 800Ω, Tamb = 50°C
Pd = 580mW
Supposing no heat sink on PCB and no air flow:
Rthj-a = 45°C/W ---> Tj = 50+45 · 0.58 =
= 50+26 = **76**°C

ex2: Ilim = 43mA, Rfeed = 800Ω, Tamb = 50°C
Pd = 1480mW
Supposing l = 1cm heat sink on PCB and no air flow:
Tthj-a = 36°C/W ---> Tj = 50+36 · 0.58 = **103**°C
Supposing l = 1cm heat sink on PCB and 0.5m/s air flow:
Rthj-a = 27.5°C/W ---> Tj = 50+27.5 · 1.48 = **90.7**°C

ex3: Ilim = 56mA, Rfeed = 400Ω, Tamb = 50°C
Pd = 1200mW
Supposing l = 1cm heat sink on PCB and no air flow:
Tthj-a = 36°C/W ---> Tj = 50+36 · 1.20 = **93**°C
Supposing l = 1cm heat sink on PCB and 0.5m/s air flow:
Rthj-a = 27.5°C/W ---> Tj = 50+27.5 · 1.20 = **83**°C

8. OVERVOLTAGE PROTECTIONS.

8.1 LIGHTNING PROTECTIONS.

The protection against lightning is obtained suppressing to GND the surges, positive and negative, by a transient voltage suppressor TVS, directly connected to TIP and RING pins of L303X (see Fig. 40).

Positive surges are suppressed to GND by a clamping Diode and negative are suppressed to GND by a Thyristor.

The protection IC suggested, is a single chip dual suppressor, programmable type: Thyristor starts coducting when the voltage on the wire (TIP or RING) goes below the potential of the GATE.
In the application the GATE in connected to VBAT.
The thyristor is switched-on when the current reach the firing threshold.

The structure and electric characteristics is according to Fig. 41 and 42.

To meet different assembly needs it's available in three different plastic packages:

IC	PACKAGE
LCP150S LCP1511 LCP1512	SIP-4 SO-8 MINIDIP

Refer to LCP15XX Data-Sheets for more detailed information.

Figure 40.

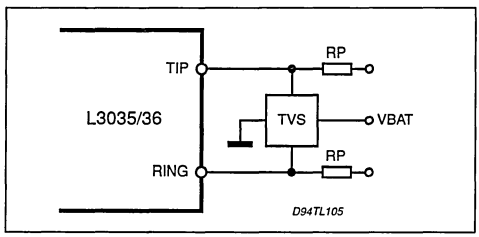


Figure 41.

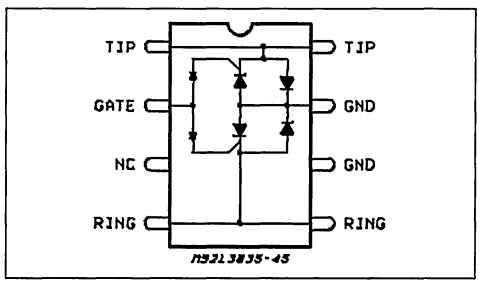
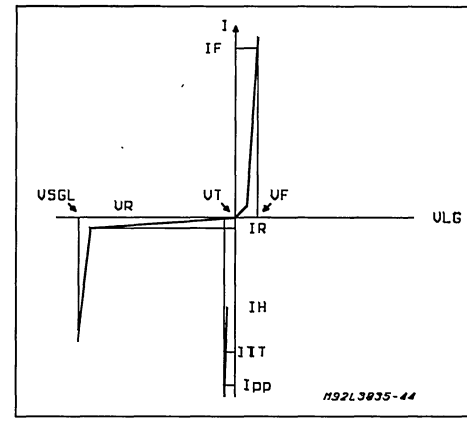


Figure 42.



8.1.1 Note.

During positive or negative surges the current flowing through the suppressor is mainly limited by the two RP resistors that dissipate most of the surge energy .

Suggested RP type are 2W wire wound resistors or thick film resistors on ceramic substrate.

8.2 POWER-CROSS PROTECTION.

In case of power-cross a long time overvoltage, continous or intermittent, is applied to the line.

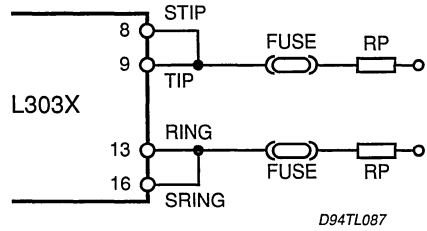
Specific protection has to be provided: lightning protection can absorbe fast transients only and a long duration event like a power-cross will burn it out.

Typically two different solutions can be adopted:

1) Fuse:
in series to each wire is provided a fuse that opens when the current exceeds a certain value.
Besides a proper fusing current, a sufficientaly long thermal time-constant is required, in order to withstand lightings; on the contrary, maintenance intervention will statistically increase.
Typically it's a metal strip that take place on the same ceramic substrate of the protetction resistors.

In this case the feedback for PTCs mismatch compensation is not necessary.
STIP (Pin 8) can be directly connected to TIP (Pin 9) and SRING (Pin 16) to RING (Pin 15) see Fig. 43.

Figure 42.



2) PTC:
another solution widely adopted is to put PTCs in series to the line wires.
In case of high current injection when the PTC, after a thermal transient, reaches a sufficiently high temperature (tripped state) its resistance highly increases limiting the injected current, preventing the damage of the Slic and lightning protection.

The value of the resistance in trip condition depends on the overvoltage level.
Under power-cross condition the injected power is mainly dissipated by the PTCs.

PTCs have not to trip in the operating current range of the Slic and in tripped state the dissipation of the Slic and TVS has to stay below the maximum allowed.

An aspect to be considered is the transient time.
During the transient, before the trip condition, the power is mainly dissipated inside the Slic and TVS.
The temperature of Slic and TVS increases till the tripped state is reached and its maximum value is related to the ratio of the time-constants.
If the transient takes too long, Slic and TVS can be damaged before the tripped state is reached.
As a general rule the PTC has to be the fastest.

To evaluate power dissipation in the Slic and protection, before the PTCs trip consider that:

1)Slic: TIP and RING can sink or source a maximum current of 100mA; exceeding current flows through the protection IC.

2)Protection IC: when the positive half-wave goes over GND the overcurrent flows through the clamping diode and the power dissipation is PD = I · Vf.
When the negative half-wave goes below VBAT the current flows through SCR not yet fired the dissipation is at the maximum level : PD= I · Vsgl.
When the current reaches the firing threshold the power dissipation becomes: PD = I · Vt.

8.3 CONCLUSIONS

Fig. 43 and 44 shows the typical configuration for L303X SLIC protection with fuse or PTC, solution used in fig.43 can be used also replacing fuse with PTC, but in this case the PTC mismatch is not compensated, therefore the longitudinal balance performance of the application will depends on the PTC matching value.
Refer to device datasheet for the components value.

Figure 43: Typical Application Circuit with Fuse

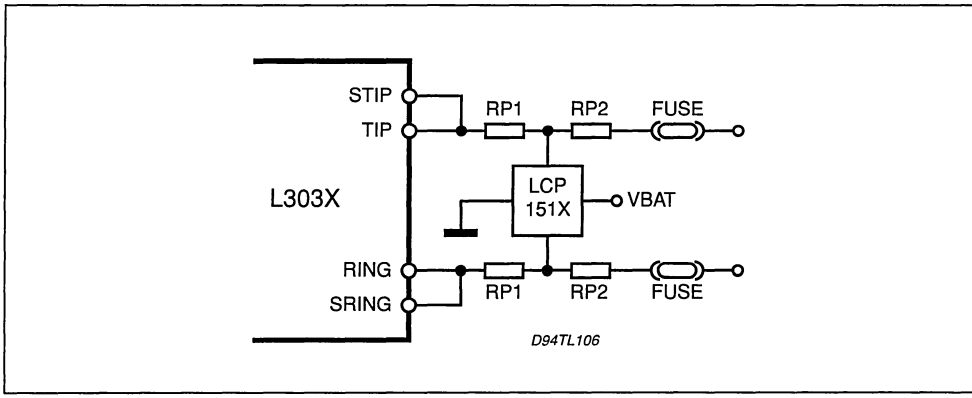
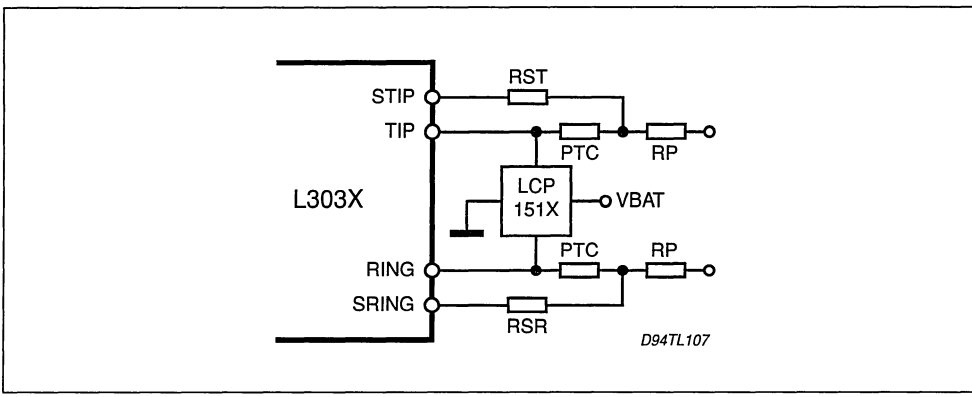


Figure 44: Typical Application Circuit with PTC



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

SLIC L3000N/L3092 MAXIMUM LOOP RESISTANCE ANALYSIS

by W. Rossi

1. INTRODUCTION

This evaluation was carried out in order to evaluate the maximum loop resistance allowed using the SLIC KIT L3000N/L3092.

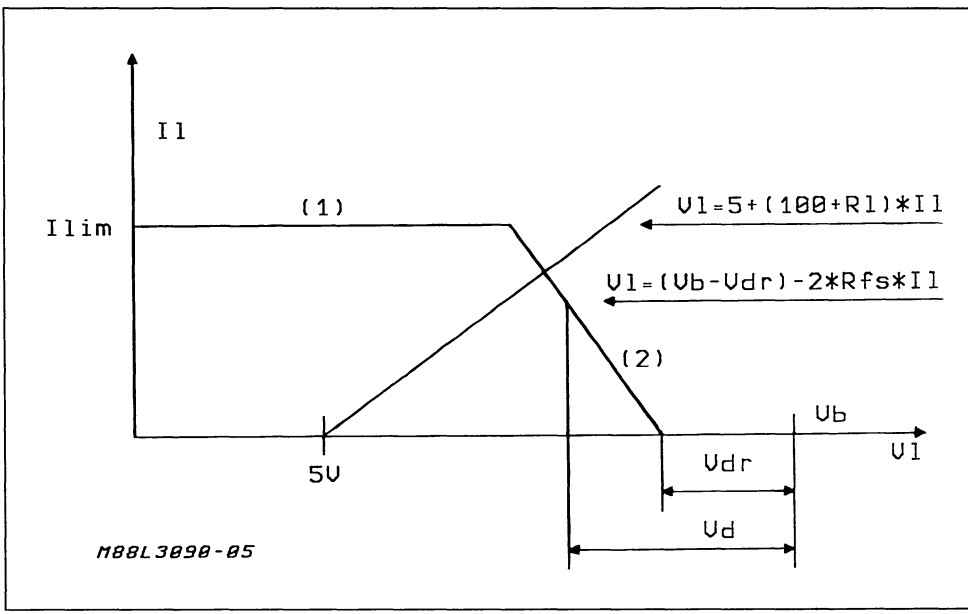
The evaluation is performed in conversation mode ; it shows how the maximum loop resistance (Rl) is influenced by the battery voltage (Vb), the feeding resistance (Rfs) and the common mode current (Icm).

2. MAXIMUM LOOP RESISTANCE EVALUATION

In fig. 1 you can see the L3000N + L3092 DC characteristic and the load curve. The load curve is obtained as the series of the loop resistance (Rl) and the sub-scriber telephone set. The subscriber telephone set is represented as the series of a 100Ω resistor and a 5V zener diode.

If the operating point is on region (1) its coordinates

Figure 1 : SLIC Characteristic and Load Curve.



are :

Il1 = Ilim

Vl1 = 5 + (100+Rl)xIlim (1)

Note : The slope of region (2) is 2xRfs where the feeding resistor Rfs is fixed by an external resistor.

If the operating point is on region (2) you can find its coordinates solving the system of two equations :

1) Vl = (Vb-Vdr)-2xRfsxIl

2) Vl = 5+(100+Rl)xIl

obtaining :

Il2 = (Vb-Vdr-5)/(100+Rl+2*Rfs)

Vl2 = 5+(100+Rl)x(Vb-Vdr-5)/(100+Rl+2xRfs) (2)

If you consider the DC characteristic of the device you can see that the longer is the line the lower is the voltage drop between the battery voltage (Vb) and the line voltage (Vl). It can happens that for very

long line the voltage drop is not large enough to guarantee the fully AC performance of the device. In such condition the device is still working, but large signal can appear slightly distorted on the line. If you want guarantee the optimum behavior of the device you must be sure that the operating point of the device (Il, Vl) satisfy the following condition :

$Vl \leq Vb-Vd$

with $Vd=5+100xIl+60xIl+2+Vdcm$

where :

5 : internal drop

100xIl : drop on sensing resistors (2x50Ω max)

60xIl : drop on external resistors (2x30Ω)

2 : maximum AC signal peak

Vdcm : (=100xIcm) drop for common mode current (Icm)

You can obtain the maximum value for Rl (maximum loop length) imposing :

$Vl = Vb-Vd$

If the operating point is on region (1) solving the equation $Vl1=Vb-Vd$ where Vl1 is given by the relation (1) you obtain :

$Rlmax= (Vb-12-260xIlim-100xIcm)/Ilim$ (3)

If the operating point is on region (2) solving the equation $Vl2=Vb-Vd$ where Vl2 is given by the relation (2) you obtain :

$Rlmax = ((100+2xRfs)x(Vb-12-100xIcm)-260x(Vb-Vdr-5))/(7-Vdr+100xIcm)$

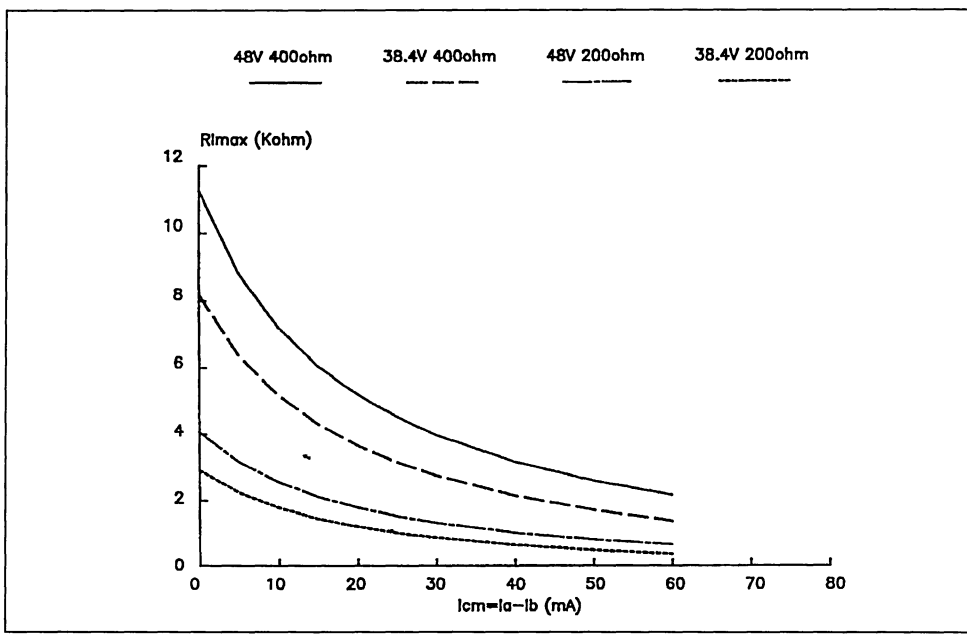
In the following you can find graphical representations of Rlmax versus Icm in four different situations :

3. CONCLUSION

The above relations show the possibility to work with good performances also in presence of common mode current. With a battery voltage of –48V, Rfs = 200Ω and no common mode current, the maximum loop resistance is over 3KΩ ; in the same condition but with a common mode current of 20mA the maximum loop resistance is about 2KΩ. Higher loop resistance can be obtained increasing Rfs (see fig. 2).

The parameters of each curve are the battery voltage (Vb) and the feeding resistance (Rfs).

Figure 2 : Maximum Line Resistance Versus Common Mode Current (conversation mode).



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

SLIC L3000N/L3092 PERFORMANCE ANALYSIS WITH -24V BATTERY

by W.Rossi

INTRODUCTION

This technical note describes the L3000N/L3092 SLIC performances when used with a battery voltage of –24V. All the main characteristics are analyzed and compared with the results obtained with a standard battery voltage of –48V.

The following data were obtained from a typical device in order to have an idea on how DC characteristic, power consumption, ringing voltage and AC performances are influenced by a reduced battery voltage.

POWER CONSUMPTION

Table 1 shows the L3000N-L3092 current consumption with two batteries combination V_{B-} = -48V; V_{B+} = 72V and V_{B-} = -24V; V_{B+} = +50V. The measurements are made in the different operating modes (Power Down; Stand-by; Conversion with I_L = 0; I_L = 40mA and Ringing without AC Line Load (Ringing Equivalent Number REN = 0).

Table 1: SLIC Typical Current Consumption with Different Battery Voltages.

	Current Consumption (mA)			
	–48V	+72V	–24V	+60V
PW - DOWN	0	0	0	0
SBY (I_L = 0)	1.93	0	1.9	0
CVS (I_L = 0)	4.91	–	4.4	0
CVS (I_L = 40mA)	52.2	–	50	0
RING (0 REN)	13.4	10.8	10.0	7.9

DC CHARACTERISTICS

In fig 1 you can see the typical DC characteristics for the two battery voltages: feeding resistance was set to 2 x 200Ω (RFS = 200Ω).

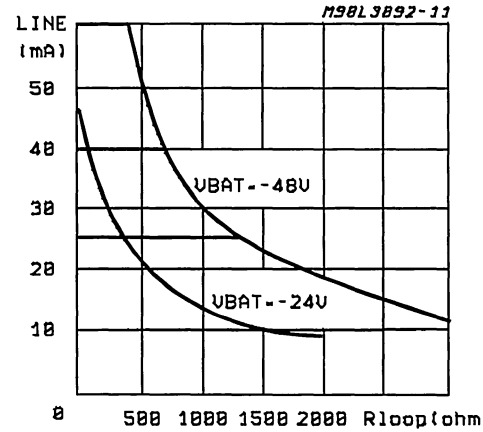
The typical current value versus loop resistance is given by:

$$I_L = Ilim \quad \text{for } R_L < \frac{|V_{B-}| - 5V}{Ilim} - 2RFS$$

$$I_L = \frac{|V_{B-}| - 5V}{R_L + 2RFS} \quad \text{for } R_L > \frac{|V_{B-}| - 5V}{Ilim} - 2RFS$$

Where RFS represents the resistance of each side of the traditional feeding system (most common values for RFS are 200, 400 and 500Ω).

Figure 1: L3000N/L3092 DC Characteristic with a 2 x 200Ω Feeding Resistance.



MAXIMUM LOOP LENGHT

Two are the parameters influenced by line lenght increment: the first is the DC line current and the second is the maximum AC signal that can be sent without distortion (THD = 1%). Here below are shown the typical maximum loop resistance values and the relative line current in corrispondance of which distortion is still less than 1% for +4dBm (1.23 VRMS) AC signals. The SLIC feeding resistance is set 2 x 200Ω.

V_{B-} = -48V	V_{B-} = -24V
Rmax. = 2200Ω	Rmax. = 940Ω
I_L = 16.61mA	I_L = 14.47mA

ON/OFF HOOK CURRENT THRESHOLDS

Here below are reported the typical values of the DC current thresholds used by the SLIC to detect the ON hook and OFF hook line conditions.

$V_{B-} = -48V$

ON/OFF Hook commutation

IL = 8.10mA VL = 40.58V RL = 5KΩ

OFF/ON Hook commutation.

IL = 5.91mA VL = 41.30V RL = 7KΩ

$V_{B-} = -24V$

ON/OFF Hook commutation

IL = 8.10mA VL = 16.52V RL = 2KΩ

OFF/ON Hook commutation.

IL = 5.82mA VL = 17.44V RL = 3KΩ

$V_{B-} = -24V$

AC PERFORMANCES

All the AC performances: TXgain, RX gain, Return Loss, Transhybrid Loss and Longitudinal Balance were measured and no significative variations were found changing from –48V to –24V of battery voltage.

GRX, GTX and THL variation were inside 0.03dB; RL inside .07dB and longitudinal balance inside .9dB.

RINGING PERFORMANCES

L3000N/L3092 SLIC injects directly the ringing signal into the line. The ringing signal has a DC component superimposed with the AC one.

The maximum ringing amplitude that can be obtained by L3000N without distortion depends on the total battery voltage available:

Let:

VBT = |VB+| + |VB-|

VRING = 0.58VBT - 8.6 (Vrms) (1)

VDCRING = 0.1736VBT + 0.75 (V)

EX:

VB+ = 72V; VB- = -48V

VRING = 0.58 x 120 - 8.6 = 61Vrms

VDCRING = 21.6V

VB+ = 50V; VB- = -24V

VRING = 0.58 x 74 - 8.6 = 34.3Vrms

VDCRING = 13.6V

From eq. (1):

VBT = (VRING + 8.6)/0.58

CONCLUSIONS

The measurements carried on show that it is possible to make the SLIC working also with reduced battery voltage (down to –24V) without any degradation in terms of AC performances.

It should be noted that with –24 battery voltage you can get good performances up to 950Ω of loop lenght. In case you need higher line currents you can increase the battery voltage of the amount you need, optimizing in this way power dissipation.

SGS-THOMSON SLIC KIT AC MODELS

by W. Rossi

INDEX

1. INTRODUCTION

In this note you can find the basic structure of all SGS-THOMSON Microelectronics SLICs concerning AC performances.

In all these SLICs are present two capacitors one for AC/DC path splitting and the other for loop stability. The effect of these capacitors is neglectible in speech band (300 - 3400Hz) therefore for each KIT are evaluated the typical AC performances not considering their influence.

If performances on a wider band or very high accuracy are requested the effect of these capacitors must be included.

Another possibility to study the effect of these capacitors is to enter the SLIC structure in a circuit simulator like SPICE, as shown at the end of this note with the L3000N/L3092 SLIC KIT and L303X monochip SLIC.

2. L3000N/L3010 SLIC KIT BASIC STRUCTURE

Here below you can see the basic structure of the L3000N/L3010 SLIC KIT concerning AC performances.

For an easier representation the high voltage part is drawn as a single ended amplifier with a gain of 40. Close to each node is written the corresponding pin number of L3010. The components names are the same used in the data sheet.

Figure 1: L3000N/3010 SLIC Basic Structure.

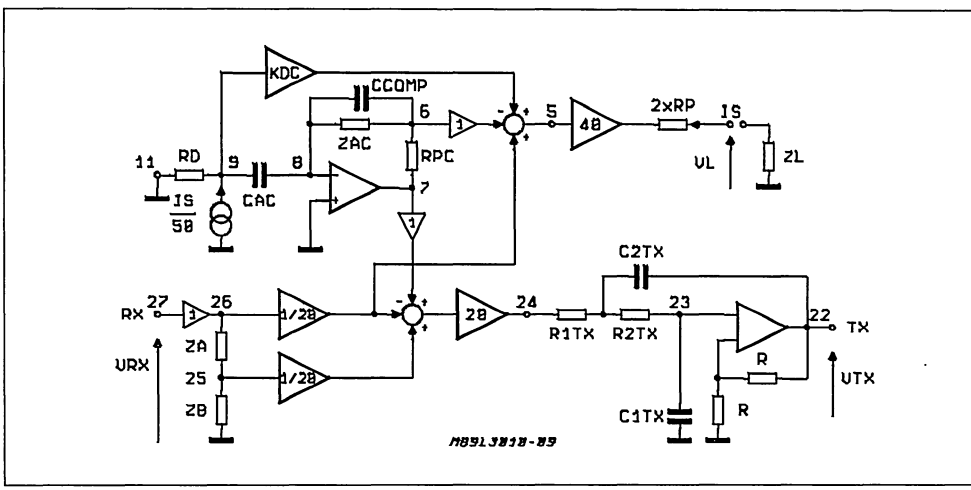
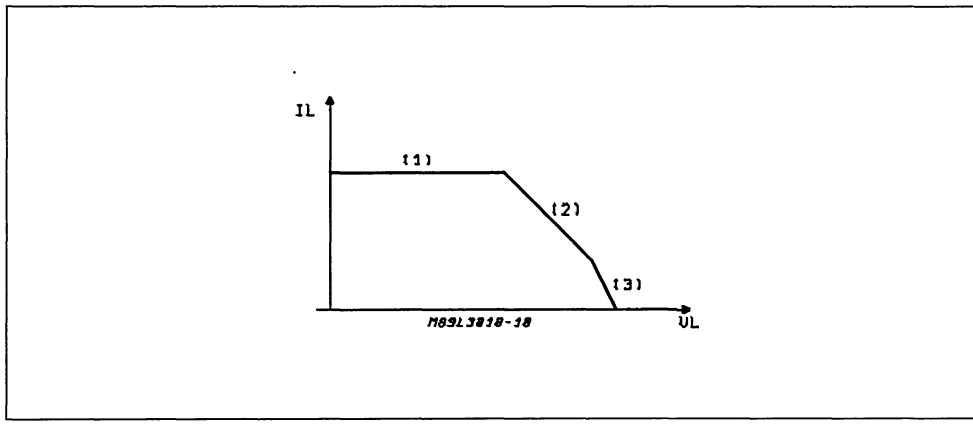


Figure 2: L3000N/3010 DC Characteristic.



The RD and KDC values depends on the working point on DC characteristic, in particular :

RD = infinite ; KDC = 2 for region 1

RD = RDC ; KDC = 2 for region 2

RD = RDC ; KDC = 2/3 for region 3

CAC is a large capacitor (typ. 22µF) used to split AC and DC components of line current.

CCOMP is a small capacitor (typ. 8.2nF) used to guarantee loop stability.

CAC and CCOMP values are chosen in order to have a neglectible effect on speech band signals, therefore supposing CCOMP equivalent to an open circuit and CAC to a short circuit the following relationships can be easily obtained from the circuit diagram of fig. 2.1. Also the TTX filter influence in speech band is neglected.

2.1. SLIC IMPEDANCE AT LINE TERMINATIONS:

$$ZML = \left.\frac{V_L}{I_S}\right|_{VRX=0} = (4/5)\ x\ ZAC + 2\ x\ RP$$

2.2. RECEIVING GAIN :

$$G_R = \frac{V_L}{V_{RX}} = 2 \cdot \frac{ZL}{ZL + ZML}$$

therefore if ZL = ZML

$$G_R = 1$$

2.3. SENDING GAIN

$$G_S = \left.\frac{V_{TX}}{V_L}\right|_{VRX=0} = -\frac{ZAC + RPC}{ZAC + (5/2) \cdot RP}$$

therefore if RPC = (5/2) x RP

$$G_S = -1$$

2.4. TRANS-HYBRID LOSS

$$THL = \frac{V_{TX}}{V_{RX}} = 2 \cdot \left(\frac{ZB}{ZA + ZB} - \frac{ZL + 2 \cdot RP - (4/5) \cdot RPC}{ZL + ZML}\right)$$

therefore if RPC = (5/2) · RP and ZA/ZB = ZML/ZL

THL = 0

If you need a more careful evaluation of AC performances you can include also the effect of CCOMP, CAC and TTX filter in the above relations or you can simulate the system behavior with SPICE or other circuit simulators (see example at par. 6).

3. L3000N/L3030 SLIC KIT BASIC STRUCTURE

Here below you can see the basic structure of the L3000N/L3030 SLIC KIT concerning AC performances.

For an easier representation the high voltage part is drawn as a single ended amplifier with a gain of 40. Close to each node is written the corresponding pin number of L3030 in PLCC package. The components names are the same used in the data sheet.

As you can see on the L3000N/L3030 data sheet the large AC/DC splitting capacitor (typ. 22µF) can be avoided using the on chip capacitor multiplier. In the following you can see the basic structure in both cases.

Figure 3: L3000N/L3030 SLIC Configured without Capacitor Multiplier Basic Structure.

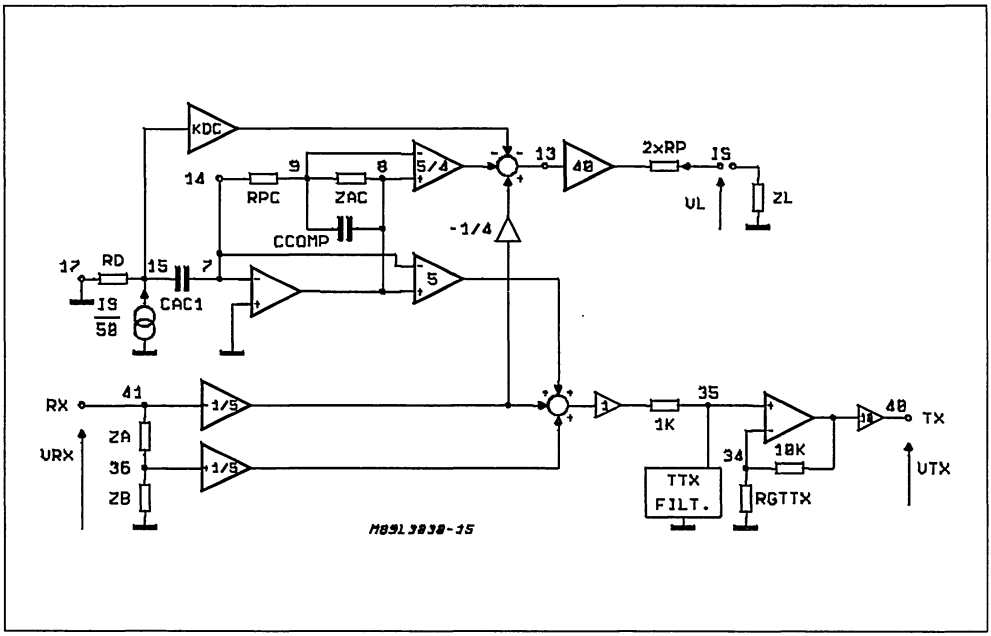


Figure 4: L3000N/L3030 SLIC Configured with Capacitor Multiplier Basic Structure.

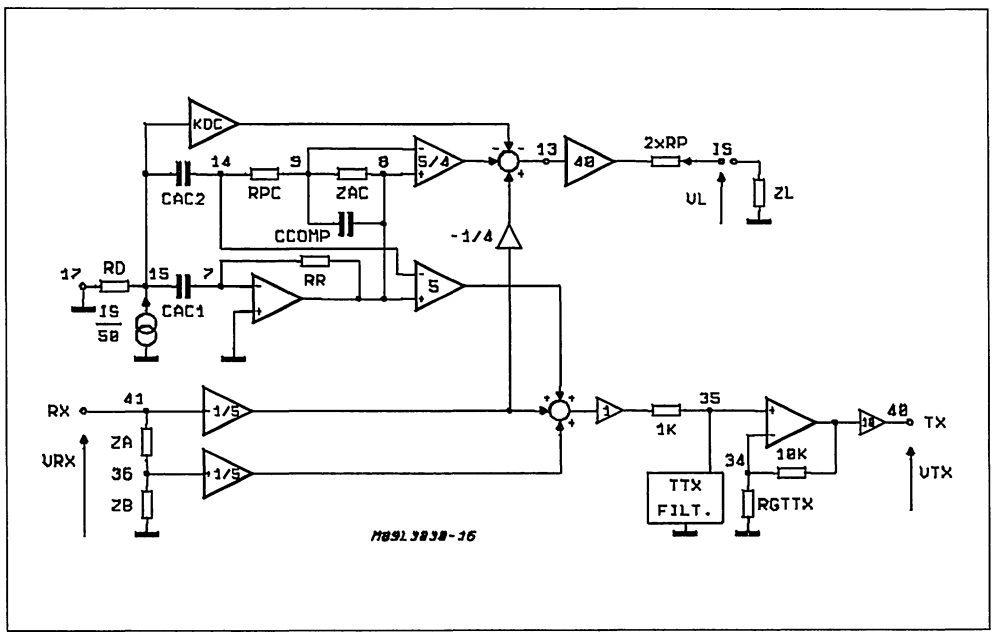
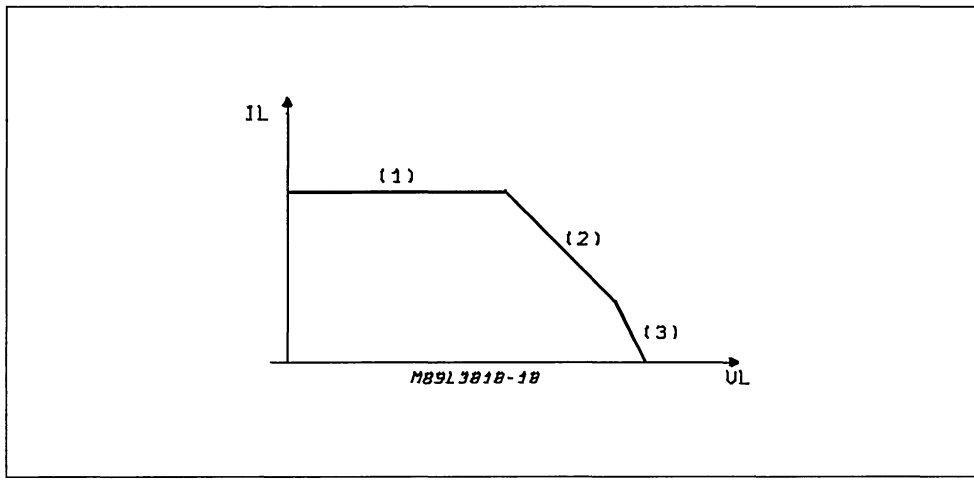


Figure 5: L3000N/3030 DC Characteristic.



The RD and KDC values depends on the working point on DC characteristic, in particular :

RD = infinite ; KDC = 5/4 for region 1

RD = RDC ; KDC = 5/4 for region 2

RD = RDC ; KDC = 5/12 for region 3

CAC1 or the sinthesized capacitor obtained with the capacitor multiplier is relatively large (typ. 22μF) and it is used to split AC and DC components of line current.

CCOMP is a small capacitor (typ. 10nF) used to guarantee loop stability.

CAC1, CAC2 and CCOMP values are chosen in order to have a neglectible effect on speech band signals, therefore supposing CCOMP equivalent to an open circuit and CAC1 or the sinthetized capacitor obtained with the capacitor multiplier equivalent to a short circuit the following relationships can be easily obtained from the circuit diagram of fig. 3. Also the TTX filter influence in speech band is neglected. The TTX filter impedance is supposed to be equal to RGTTX/10 in speech band and zero at the TTX frequency

3.1. SLIC IMPEDANCE AT LINE TERMINATIONS:

$$ZML = \left.\frac{V_L}{I_S}\right|_{VRX = 0} = ZAC + 2 \times RP$$

3.2. RECEIVING GAIN :

$$G_R = \frac{V_L}{V_{RX}} = 2 \cdot \frac{ZL}{ZL + ZML}$$

therefore if ZL = ZML

$$G_R = 1$$

3.3. SENDING GAIN

$$G_S = \left.\frac{V_{TX}}{V_L}\right|_{VRX = 0} = -\frac{ZAC + RPC}{ZAC + 2 \cdot RP}$$

therefore if RPC = 2 x RP

$$G_S = -1$$

3.4. TRANS-HYBRID LOSS

$$THL = \frac{V_{TX}}{V_{RX}} = 2 \cdot \left(\frac{ZB}{ZA + ZB} - \frac{ZL + 2 \cdot RP - (4/5) \cdot RPC}{ZL + ZML}\right)$$

therefore if RPC = 2 · RP and ZA/ZB = ZML/ZL

THL = 0

If you need a more careful evaluation of AC performances you can include also the effect of CCOMP, CAC and TTX filter in the above relations or you can simulate the system behavior with SPICE or other circuit simulators (see example at par. 6).

4. L3000N/L3092 SLIC KIT BASIC STRUCTURE

Here below you can see the basic structure of the L3000N/L3092 SLIC KIT concerning AC performances.

For an easier representation the high voltage part is drawn as a single ended amplifier with a gain of 40. Close to each node is written the corresponding pin number of L3092. The components names are the same used in the data sheet.

Figure 6: L3000N/3092 SLIC Basic Structure.

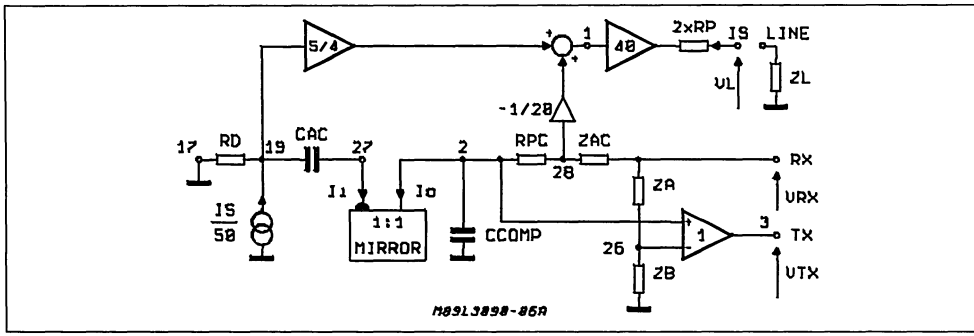
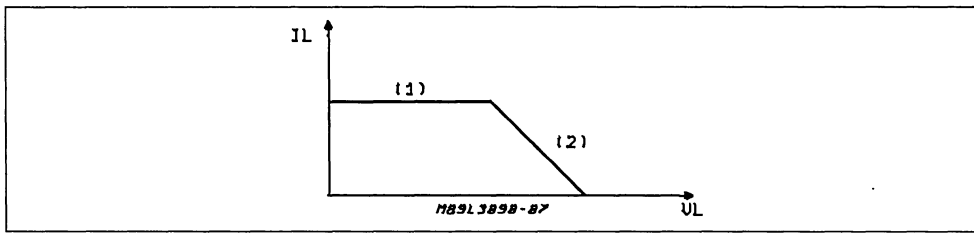


Figure 7: L3000N/3092 DC Characteristic.



The RD value depends on the working point on DC characteristic, in particular :

RD = infinite for region 1

RD = RDC for region 2

CAC is a large capacitor (typ. 47µF) used to split AC and DC components of line current.

CCOMP is a small capacitor (typ. 390pF) used to guarantee loop stability.

CAC and CCOMP values are chosen in order to have a neglectible effect on speech band signals, therefore supposing CCOMP equivalent to an open circuit and CAC to a short circuit the following relationships can be easily obtained from the circuit diagram of fig. 4.1.

4.1. SLIC IMPEDANCE AT LINE TERMINATION

$$ZML = \frac{V_L}{I_S}\Bigg|_{VRX=0} = (ZAC/25) + 2 \times RP$$

4.2. RECEIVING GAIN :

$$G_R = \frac{V_L}{V_{RX}} = 2 \cdot \frac{ZL}{ZL + ZML}$$

therefore if ZL = ZML

$G_R = -1$

4.3. SENDING GAIN

$$G_S = \frac{V_{TX}}{V_L}\Bigg|_{VRX=0} = -0.5 \cdot \left(\frac{ZAC + RPC}{ZAC + 25 \cdot (2 \cdot RP)}\right)$$

therefore if RPC = 25 x (2 x RP)

$G_S = -1$

4.4. TRANS-HYBRID LOSS

$$THL = \frac{V_{TX}}{V_{RX}} = \frac{ZL + 2 \cdot RP - (RPC/25)}{ZL + ZML} - \frac{ZB}{ZA + ZB}$$

therefore if RPC = 25 (2 · RP) and ZA/ZB = ZML/ZL

THL = 0

If you need a more careful evaluation of AC performances you can include also the effect of CCOMP and CAC in the above relations or you can simulate the system behavior with SPICE or other circuit simulators (see example at par. 6).

5. L303X MONOCHIP SLIC BASIC STRUCTURE

Here below you can see the basic structure of the L303X MONOCHIP SLIC family (L3035, L3036, L3037) concerning AC performances.
Close to each node is written the corresponding pin number. The components names are the same used in the data sheet.

Figure 8: L303X Monochip SLIC Basic Structure.

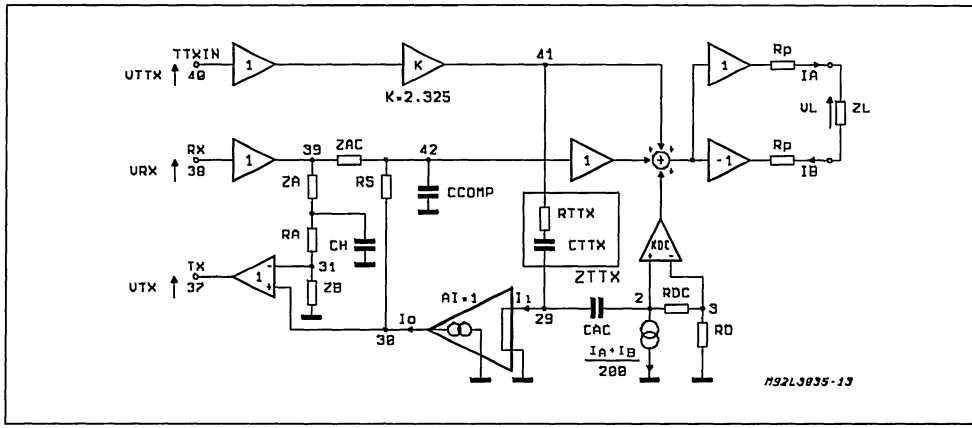
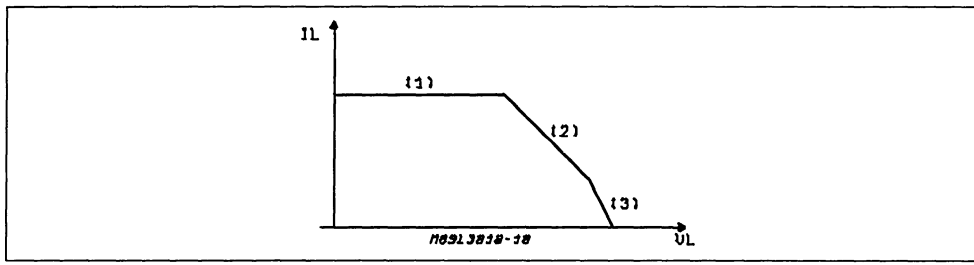


Figure 9: L303X DC Characteristic.



The R0 and KDC values depends on the working point on DC characteristic, in particular:

R0 = infinite ; KDC = 5 for region 1

R0 = 0 ; KDC = 5 for region 2

R0 = 0 ; KDC = 0 for region 3

CAC is a large capacitor (typ. 4.7µF) used to split AC and DC components of line current.

CCOMP and CH are small capacitors (typ.220pF) used to guarantee loop stability and good THL performances.

CAC, CCOMP and CH values are chosen in order to have a neglectible effect on speech band signals, therefore supposing CCOMP equivalent to an open circuit and CAC to a short circuit the following relation ships can be easily obtained from the circuit diagram of fig. 5.1.

5.1. SLIC IMPEDANCE AT LINE TERMINATIONS:

$$ZS = \frac{V_L}{I_S}\Bigg|_{VRX=0} = (ZAC/50) + 2 \times RP$$

5.2. RECEIVING GAIN :

$$G_R = \frac{V_L}{V_{RX}} = 2 \cdot \frac{ZL}{ZL + ZS}$$

therefore if ZL = ZS

$G_R = 1$

5.3. SENDING GAIN

$$G_S = \frac{V_{TX}}{V_L}\Bigg|_{VRX=0} = 0.5 \cdot \left(\frac{ZAC + RS}{ZAC + (50 \cdot 2RP)}\right)$$

therefore if RS = 50 · 2RP

$G_S = 1$

5.4. TRANS-HYBRID LOSS

$$THL = \frac{V_{TX}}{V_{RX}} = \frac{ZL + 2 \cdot RP - (RS/50)}{ZL + ZS} - \frac{ZB}{ZA + RA + ZB}$$

therefore if RS = 50 · 2RP and (ZA+RA)/ZB = ZS/ZL

THL = 0

5.5. TTX GAIN

Let's define ZL_{TTX} = line impedance at TTX frequency

$Z_{TTX} = R_{TTX} + \frac{1}{j\,\omega\,C_{TTX}}$: impedance of the TTX filter (R_{TTX} in series with C_{TTX}) at TTX frequency.

K = 2.325 TTX buffer gain.

From the block diagram of fig. 8 the TTX gain become:

$$G_{TTX} = \frac{V_L}{V_{TTX}} = 2K \cdot G \cdot \left(\frac{ZL_{TTX}}{ZL_{TTX} + 2Rp}\right) \cdot V_{TTX} \quad (1)$$

The residual at TX output is:

$$VTX_{res} = K \cdot (1 - G) \left(\frac{ZAC + RS}{ZAC}\right) \cdot V_{TTX} \quad (2)$$

Where

$$G = \frac{\left[\frac{1 + ZAC}{(K \cdot Z_{TTX})}\right]}{1 + \frac{ZAC}{[(ZL_{TTX} + 2Rp) \cdot 50]}}$$

The optimum TTX filter is obtained for G = 1 that means

$$Z_{TTX} = 50(ZL_{TTX} + 2Rp) / K$$

In this case the (1) and (2) become:

$$G_{TTX} = 2K \cdot \left[\frac{ZL_{TTX}}{ZL_{TTX} + ZRp}\right]$$

$VTX_{res} = 0$

If you need a more careful evaluation of AC performances you can include also the effect of CCOMP and CAC in the above relations or you can simulate the system behavior with SPICE or other circuit simulators (see example at par. 7).

6. ONE EXAMPLE OF SPICE SIMULATION WITH L3000N/L3092 SLIC KIT

Figure 10: Circuit Diagram for L3000N/L3092 SLIC KIT ASpice Simulation.

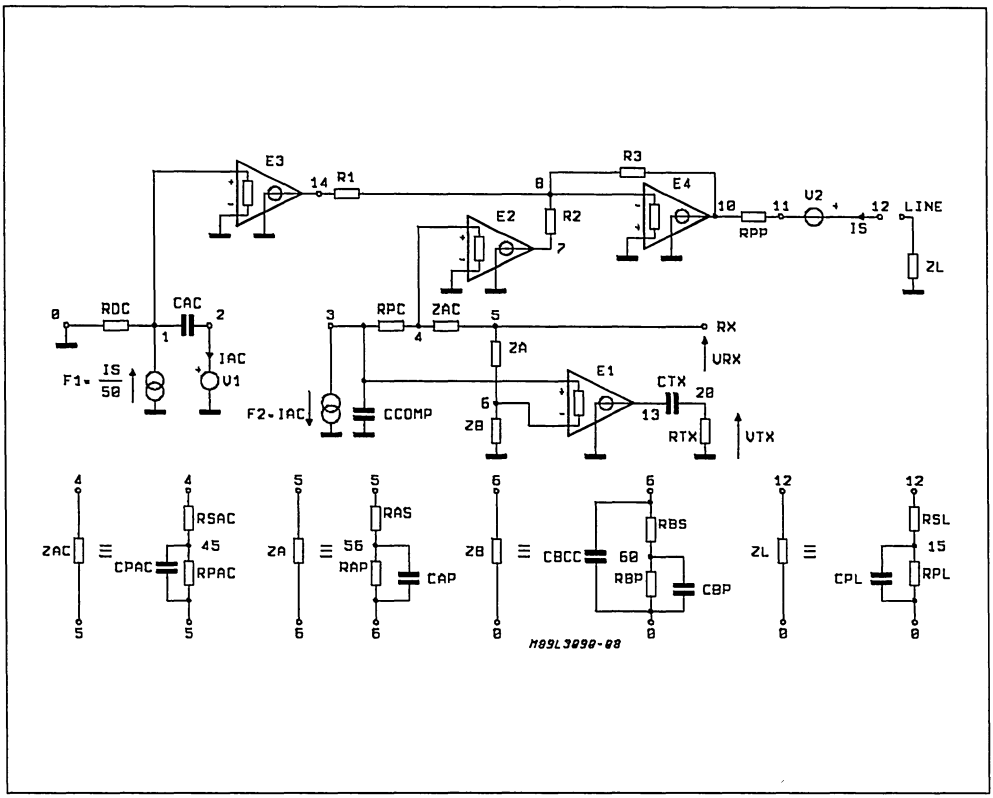
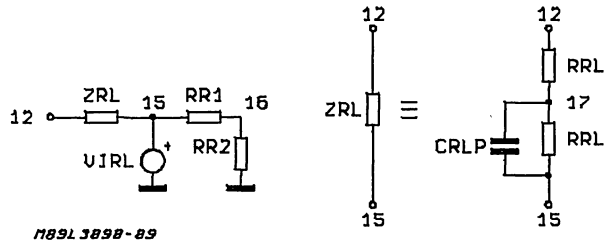
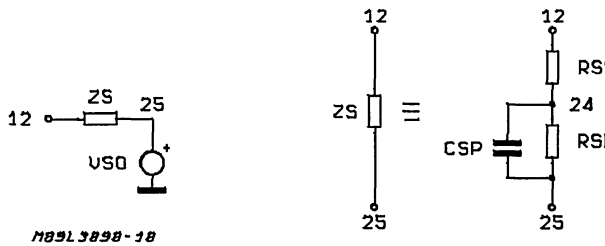


Figure 11: Network for RL Evaluation; ZRL = Return Loss Test Impedance.



$$RL = 20\log_{10}\left|\frac{ZRL - ZML}{ZRL + ZML}\right| = 20\log_{10}\left|\frac{2 \times V(12,16)}{VIRL}\right|$$

Figure 12: Network for TX Gain Evaluation with Sending Generator Series Impedance Equal to ZS.



$G_S = 2 \times VTX/VSO$

SPICE INPUT FILE FOR L3000N/L3092 SLIC KIT SIMULATION

```
L3092 AC ANALYSIS

********** CIRCUIT CONFIGURATION USED ********************
* PROT. RES. 2x50 OHM -- RPP = 100 OHM; RPC=2.5KOHM      *
* FEEDING RES. 2x200 OHM -- RDC = 300 OHM                *
* AC LINE IMPEDANCE 600 OHM -- RZAC = 12.5KOHM           *
* (SAME CONFIGURATION AS L3000N/L3092 TEST CIRCUIT)      *
**********************************************************************

********** EXTERNAL COMPONENTS *********************************

RPC 3 4 2.5K
RSAC 4 45 .5K
RPAC 45 5 12K
*CPAC 45 5 1P
RAS 5 56 6K
RAP 56 6 6K
*CAP 56 6 1P
RBS 6 60 6K
RBP 60 0 6K
*CBP 60 0 1P
CBCC 6 0 470P
RPP 10 11 100
RTX 20 0 1MEG

CAC 1 2 47U
CCOMP 3 0 390P
CTX 13 20 10U

********** END EXT. COMPONENTS *******************************

********** MODEL COMPONENTS ************************************
R1 14 8 1K
R2 7 8 1K
R3 8 10 40K
R4 8 0 10MEG

E1 13 0 3 6 1
E2 7 0 4 0 +.05
E3 14 0 1 0 -1.25
E4 10 0 8 0 -1MEG

V1 2 0
V2 12 11
```

```
F1 0 1 V2 .02
F2 3 0 V1 1

.AC LIN 40 100 4K
*.AC DEC 10 10 20K
.WIDTH IN=80 OUT=80

****** INSERT ONLY ONE OF THE FOLLOWING BLOCKS DEPENDING *******
****** ON THE DC CHARACTERISTIC REGION                  *******
*** LIM CURRENT REGION ***********
* RDC 1 0 10MEG
*** END LIM REGION ***************

*** RES. FEED REGION *************
* RDC 1 0 300
*** END RES. REGION **************

****** INSERT ONLY ONE OF THE FOLLOWING BLOCKS DEPENDING *******
****** ON WHICH ANALYSIS YOU WANT                       *******

*** TX GAIN EVALUATION VTX/VL WITH VRX = 0 ***
*VRX 5 0 DC 0
*VL 12 0 AC
*.PRINT AC VDB(20) VP(20)
*.PLOT AC VDB(20) VP(20)
* .STORE AC VDB(20) VP(20)
*** END TX GAIN ************************************

*** TX GAIN EVALUATION 2VTX/VSO WITH VRX=0 ***
*** (SERIES IMP. OF SENDING GENERATOR = ZS)***
* VRX 5 0 DC 0
* VSO 25 0 AC 2
* RSS 24 12 300
* RSP 24 25 300
** CSP 24 25 1P
* .PRINT AC VDB(20) VP(20)
* .PLOT AC VDB(20) VP(20)
* .STORE AC VDB(20) VP(20)
*** END TX GAIN ************************************

*** RX GAIN EVALUATION VL/VRX ****************
* RSL 12 15 300
* RPL 15 0 300
** CPL 15 0 1P
* VRX 5 0 AC
* .PRINT AC VDB(12) VP(12)
```

```
* .PLOT AC VDB(12) VP(12)
* .STORE AC VDB(12) VP(12)
*** END RX GAIN ******************************

*** THL EVALUATION VTX/VRX ********************
* RSL 12 15 300
* RPL 15 0 300
** CPL 15 0 1P
* VRX 5 0 AC
* .PRINT AC VDB(20) VP(20)
* .PLOT AC VDB(20) VP(20)
* .STORE AC VDB(20) VP(20)
*** END THL EVALUATION ************************

*** RETURN LOSS EVALUATION ********************
* VRX 5 0 DC 0
* VIRL 15 0 AC 2
* RCS 12 17 300
* RCP 17 15 300
** CCP 17 15 1P
* RR1 15 16 1K
* RR2 16 0 1K
* .PRINT AC VDB(12,16)
* .PLOT AC VDB(12,16)
* .STORE AC VDB(12,16)
*** END RETURN LOSS EVALUATION ***************

*** INPUT IMPEDANCE EVAL. AT LINE TERMINALS **
* VRX 5 0 DC 0
* IL 0 12 AC
* .PRINT AC VM(12) VP(12)
* .PLOT AC VM(12) VP(12)
* .STORE AC VM(12) VP(12)
*** END INPUT IMPED. EVALUATION **************

.END
```

7. ONE EXAMPLE OF SPICE SIMULATION WITH L303X MONOCHIP SLIC.

Figure 13: Circuit Diagram for L303X Monochip SLIC SPICE Simulation.

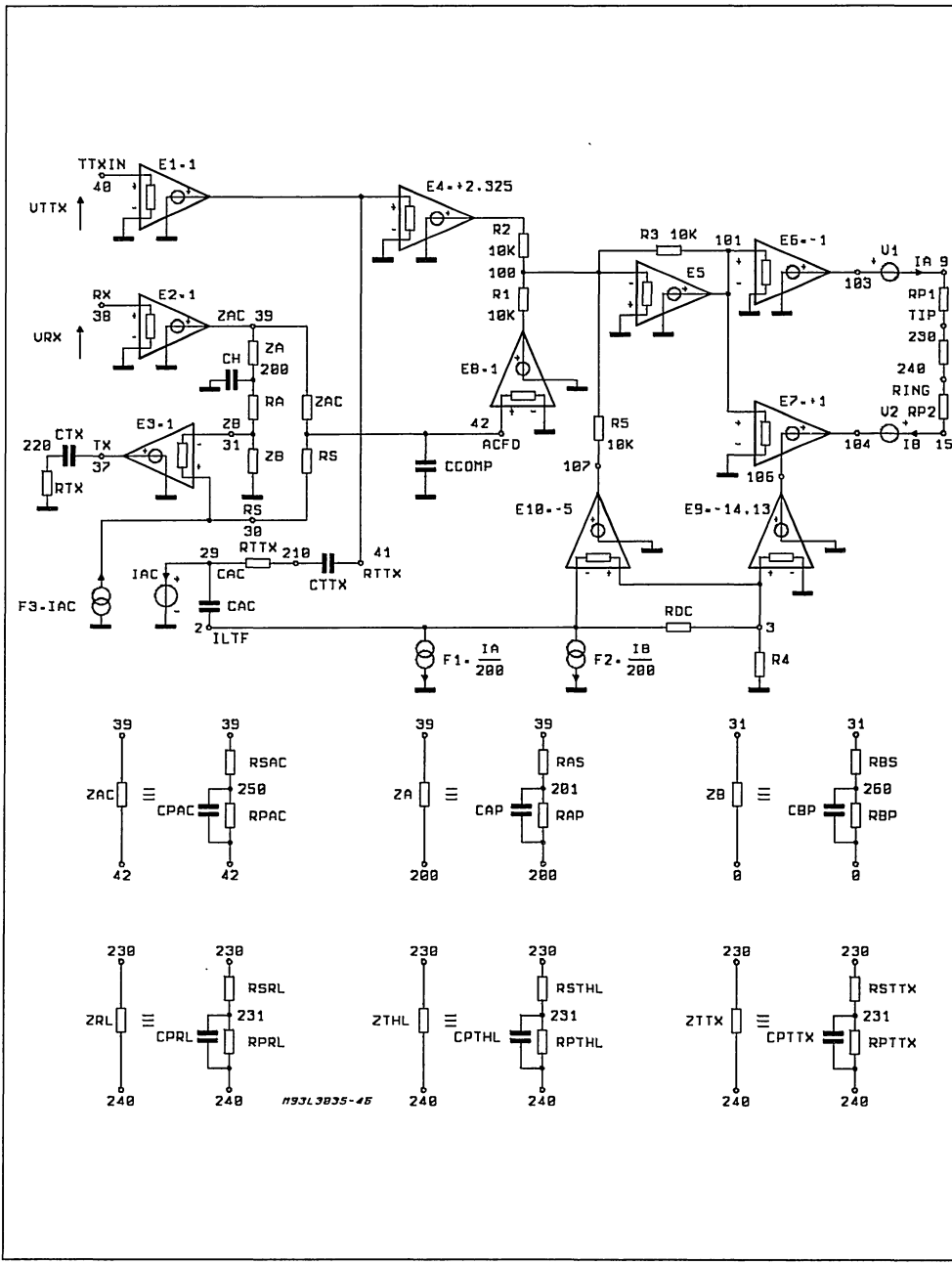
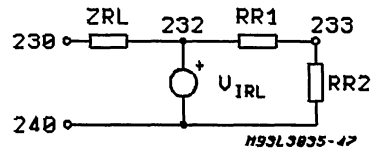
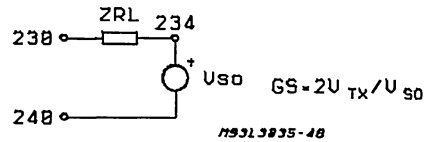


Figure 14: Network for RL Evaluation; ZRL = Return Loss Test Impedance.



$$RL = 20LOG_{10}\left|\frac{Z_{RL}-Z_S}{Z_{RL}+Z_S}\right| = 20LOG_{10}\left|\frac{2 \times V(230.233)}{V_{IRL}}\right|$$

Figure 15: Network for TX Gain Evaluationwith Sending Generator Series Impedance Equal to ZRL.



SPICE INPUT FILE FOR L303X SLIC SIMULATION

L303X MONOCHIP SLIC AC ANALYSIS

```
************************************ DEFAULT CIRCUIT CONFIGURATION ************************************
* PROT RESISTOR 2x40ohm -- RP1=RP2=40ohm -- RS=4Kohm                                                  *
* FEEDING RESISTANCE 400ohm -- RDC=3.2Kohm                                                            *
* RETURN LOSS IMPEDANCE 600ohm -- ZAC=26Kohm                                                          *
* TRANS HYBRID LOSS IMPEDANCE 600ohm -- RA=4Kohm, ZA=26Kohm, ZB=30Kohm                                *
* (SAME CONFIGURATION AS L3036 TEST CIRCUIT)                                                          *
*******************************************************************************************************

************ SLIC EXTERNAL COMPONENTS (SHOULD MATCH WITH THE APPLICATION )***********

RP1 9 230 40
RP2 15 240 40
RS 42 30 4K
RA 200 31 4K
RDC 2 3 3.2K
RTTX 29 210 6.34K
RTX 220 0 1MEG
RITTX 40 0 10MEG
RIRX 38 0 10MEG
RIZB 31 30 10MEG

CAC 2 29 4.7U
CCOMP 42 0 220P
CH 200 0 220P
CTTX 41 210 5.6N
CTX 37 220 100N

******** ZAC ********
RSAC 39 250 13K
RPAC 250 42 13K
*CPAC 250 42 4.4N
************************

********* ZA *********
RAS 39 201 13K
RAP 201 200 13K
*CAP 201 200 4.4N
************************

********* ZB *********
RBS 31 260 15K
RBP 260 0 15K
```

```
*CBP 260 0 4.4N
************************************************

**** RETURN LOSS IMPEDANCE ******
.SUBCKT ZRL 1 2
RSRL 1 3 300
RPRL 3 2 300
*CPRL 3 2 220N
.ENDS
************************************************

********** THL IMPEDANCE **************
.SUBCKT ZTHL 1 2
RSTHL 1 3 300
RPTHL 3 2 300
*CPTHL 3 2 220N
.ENDS
************************************************

********** TTX LINE IMPEDANCE *******
.SUBCKT ZTTX 1 2
RSTTX 1 3 216
*RPTTX 3 2 200
CPTTX 3 2 120N
.ENDS
************************************************


************************************ END SLIC EXTERNAL COMPONENTS ************************************


************************** MODEL COMPONENTS (SHOULD NOT BE MODIFIED) **************************

R1 100 105 10K
R2 100 102 10K
R3 100 101 10K

E1 41 0 40 0 1
E2 39 0 38 0 1
E3 37 0 30 31 1
E4 102 0 41 0 2.325
E5 101 0 100 0 -10MEG
E6 103 0 101 0 -1
E7 104 106 101 0 1
E8 105 0 42 0 1
E9 106 0 3 0 -14.13
```

```
V1 103 9
V2 15 104
V3 29 0

F1 2 0 V1 .005
F2 2 0 V2 .005
F3 0 30 V3 1

*.AC LIN 40 100 4K
.WIDTH IN=80 OUT=80

****************************************** END MODEL COMPONENTS ***************************************


******* INSERT ONLY ONE OF THE FOLLOWING BLOCKS DEPENDING ON THE ***********
******* DC CHARACTERISTIC REGION                                  ***********

******** LIMITING CURRENT REGION ******************
*R4 3 0 1MEG
******** END LIMITING REGION ********     ***************

************* CONST VOLTAGE REGION *****************
*R4 3 0 1M
************* END CONST VOLTAGE REGION *************

**** RESISTIVE FEED REGION (NOT ALWAYS PRESENT) ****
*R4 3 0 1M
*R5 107 100 10K
*E10 107 0 3 2 -5
*********** END RESISTIVE FEED REGION **************

******* INSERT ONLY ONE OF THE FOLLOWING BLOCKS DEPENDING ON ***************
******* WHICH ANALYSIS YOU WANT                               ***************

******* TX GAIN EVALUATION VTX/VL WITH VRX=0 ********************
* VRX 38 0 DC 0
* VTTX 40 0 DC 0
* VL 230 240 AC
* .AC LIN 40 100 4K
* .PRINT AC VDB(220) VP(220)
* .PLOT AC VDB(220) VP(220)
* .PROBE AC V(220)
******* END TX GAIN ***********************************************

******* TX GAIN EVALUATION 2VTX/VSOL WITH VRX=0 *****************
*VRX 38 0 DC 0
```

```
*VTTX 40 0 DC 0
*VSO 234 240 AC 2
*XZRL 230 234 ZRL
*.AC LIN 40 100 4K
*.PRINT AC VDB(220) VP(220)
*.PLOT AC VDB(220) VP(220)
*.PROBE AC V(220)
******** END TX GAIN ************************************************

******** RX GAIN EVALUATION VL/VRX ******************************
*VTTX 40 0 DC 0
*XZRL 230 240 ZRL
*VRX 38 0 AC
*.AC LIN 40 100 4K
*.PRINT AC VDB(230,240) VP(230,240)
*.PLOT AC VDB(230,240) VP(230,240)
*.PROBE AC V(230,240)
******** END RX GAIN ************************************************

******** THL EVALUATION VTX/VRX *********************************
*VTTX 40 0 DC 0
*XZTHL 230 240 ZTHL
*VRX 38 0 AC
*.AC LIN 40 100 4K
*.PRINT AC VDB(220) VP(220)
*.PLOT AC VDB(220) VP(220)
*.PROBE AC V(220)
******** END THL EVALUATION *************************************

******** RETURN LOSS EVALUATION *********************************
*VTTX 40 0 DC 0
*VRX 38 0 DC 0
*XZRL 230 232 ZRL
*RR1 232 233 1K
*RR2 233 240 1K
*VIRL 232 240 AC 2
*.AC LIN 40 100 4K
*.PRINT AC VDB(230,233)
*.PLOT AC VDB(230,233)
*.PROBE AC V(230,233)
******** END RETURN LOSS EVALUATION ***********************************

******** INPUT IMPEDANCE EVALUATION AT LINE TERMINALS ***********
*VTTX 40 0 DC 0
*VRX 38 0 DC 0
*IL 240 230 AC
```

```
*.AC LIN 40 100 4K
*.PRINT AC VM(230,240) VP(230,240)
*.PLOT AC VM(230,240) VP(230,240)
*.PROBE AC V(230,240)
******** END INPUT IMPEDANCE EVALUATION ************************

******** TTX GAIN EVALUATION VL/VTTXIN ******************************
*VRX 38 0 DC 0
*XZTTX 230 240 ZTTX
*VTTXIN 40 0 AC 1
*.AC LIN 2 12K 16K
*.PRINT AC VM(230,240) VP(230,240)
*.PLOT AC VM(230,240) VP(230,240)
*.PROBE AC V(230,240)
******** END TTX GAIN ***************************************************

******** TTX CANCELLATION VTX/VTTXIN ****************************
*VRX 38 0 DC 0
*XZTTX 230 240 ZTTX
*VTTXIN 40 0 AC 1
*.AC LIN 2 12K 16K
*.PRINT AC VM(220) VP(220)
*.PLOT AC VM(220) VP(220)
*.PROBE AC V(220)
******** END TTX CANCELLATION ***************************************

.END
```

SGS-THOMSON SLIC KITS AND COMBO II

by W. Rossi

1. INTRODUCTION

One of the main feature of COMBO II is the possibility to program TX and RX gains and to perform the two to four wire conversion (echo cancellation).

In particular the echo cancellation feature allows you to save external components in the SLIC circuitry.

In the following tables you can find different values for COMBOII hybrid balance filter in order to satisfy different administrations requirements.

Three SLIC KITS are analyzed :

L3000N/L3030
L3000N/L3092
L303X(L3035/6/7)

for each administration also the external components are specified.

If you need more specific informations the complete Application Note is available, ask for it to our sales office.

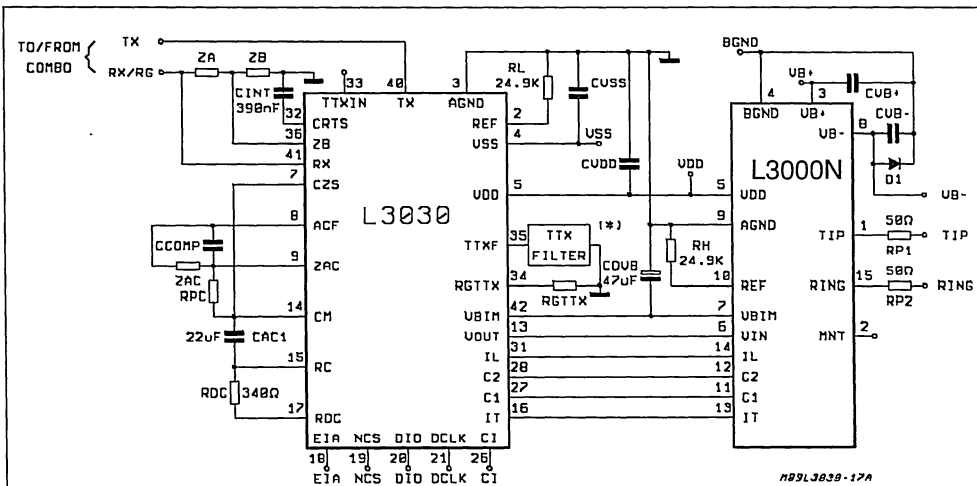
In the complete Application Note you can find all the details for each country in particular :

- Echo measurements
- Combo II simulation software results
- Bench measurements with PCM-4 Wandel & Goltermann

Table 1.

	Administration	R. L. Test Netw.	SLIC Ext. Comp.	THL. Test Netw.	COMBO II Hybal Coeff.
1.	Germany/Austria/ Switzerland	R1 = 220Ω R2 = 820Ω C1 = 115nF	ZAC = (1) RPC = 60Ω ZA = 2K ZB = 6.19K CCOMP = 10nF (1): 160W + (820Ω//115nF)	R1 = 220Ω R2 = 820Ω C1 = 115nF	EC; 32; C4

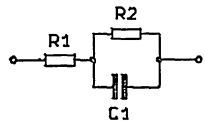
Figure 1: L3000N+L3030 Application Diagram.



(*) All measurements were made substituting the TTX filter with 1K resistor and RGTTX with 10K. The 1K resistor is equivalent to TTX filter for speech band signals.

2. L3000N/L3030 + COMBO II APPLICATION

Test network :



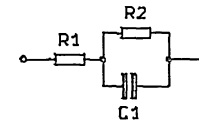
In Table 1 you can find the SLIC external components and the COMBO II programming coefficient for Germany, Austria and Switzerland followed by the application diagram (Fig. 1).

TX and RX gain are chosen in order to have :

0dBm0 ⇔ 0dBm 600 ohm (TXgain reg. = BF ; RXgain reg. = AE)

3. L3000N/L3092 + COMBO II APPLICATION

Test network :



In Table 2 you can find the SLIC external components and the COMBO II programming coefficient for different countries followed by the application diagram (Fig. 2).

TX and RX gain are chosen in order to have :

0dBm0 ⇔ 0dBm 600 ohm (TXgain reg. = 83; RXgain reg. = AE)

Table 2.

	Administration	R. L. Test Netw.	SLIC Ext. Comp.	THL. Test Netw.	COMBO II Hybal Coeff.
1	600Ω KOREA/US PRIV. PORTUGAL PRIV. FRANCE PUB.	R1 = 600Ω R2 = 0 C1 = 0	R1 = 0 R2 = 12.5K C1 = 0	R1 = 600Ω R2 = 0 C1 = 0	EE 01 44
2	CHINA	R1 = 200Ω R2 = 680 C1 = 0.1µF	R1 = 2.5K R2 = 17K C1 = 4nF	R1 = 200Ω R2 = 680Ω C1 = 0.1µF	EE 11 A6
3	ITALY PRIV.	R1 = 180Ω R2 = 630Ω C1 = 60nF	R1 = 2K R2 = 15.75K C1 = 2.4nF	R1 = 0 R2 = 750Ω C1 = 18nF	EF 00 A1
4	ITALY PUBL.	R1 = 600Ω R2 = 0 C1 = 0	R1 = 0 R2 = 12.5K C1 = 0	R1 = 0 R2 = 1.1K C1 = 33nF	E5 11 C0
5	GERMANY AUSTRIA SWITZERLAND	R1 = 220Ω R2 = 820Ω C1 = 115nF	R1 = 3K R2 = 20.5K C1 = 4.6nF	R1 = 220Ω R2 = 820Ω C1 = 115nF	EE 00 44
6	FINLAND	R1 = 270Ω R2 = 910Ω C1 = 120nF	R1 = 4.25K R2 = 22.75K C1 = 4.8nF	A: R1 = 270Ω R2 = 1.2K C1 = 120nF	 EB 11 FF
				B: R1 = 390Ω R2 = 620Ω C1 = 100nF	 F1 11 EF
7	BELGIUM PRIV.	R1 = 150Ω R2 = 830Ω C1 = 72nF	R1 = 1.25K R2 = 20.75K C1 = 2.88nF	A: R1 = 150Ω R2 = 830Ω C1 = 72nF	 EF 11 6E
				B: R1 = 600Ω R2 = 0 C1 = 0	 F8 01 0E
8	UK PRIV.	R1 = 300Ω R2 = 1K C1 = 220nF	R1 = 5K R2 = 25K C1 = 8.8nF	R1 = 370Ω R2 = 620Ω C1 = 310nF	F4 12 6B

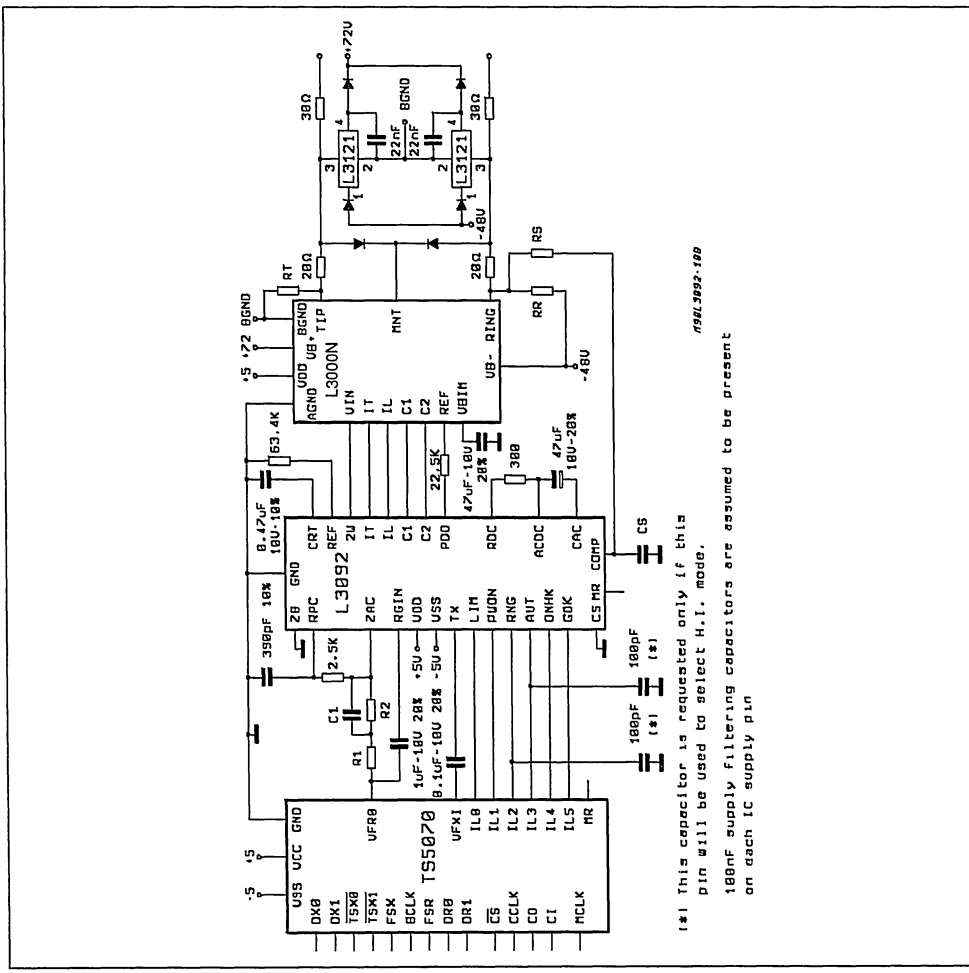
	Administration	R. L. Test Netw.	SLIC Ext. Comp.	THL. Test Netw.	COMBO II Hybal Coeff.
9	UK PUBL.	R1 = 370Ω R2 = 620Ω C1 = 310nF	R1 = 6.75K R2 = 15.5K C1 = 12.4nF	Note 1 A: SHORT LINE B: LONG LINE S.G C: LONG LINE L.G	 ED, 23, 48 EF, 39, AC E8, 35, EA
10	USA PUBL.	R1 = 900Ω R2 = INF. C1 = 2.16µF	R1 = 20K R2 = 90K C1 = 110nF *CCOMP = 150pF	Note 2 A: LOAD LINE B: NOT LOAD LINE	 E5, 20, 48 F1, 41, 20

Notes :

1. U.K THL TEST NETWORKS (See Figure 3)

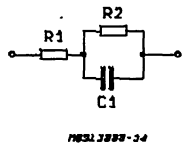
2. U.S. THL TEST NETWORKS (See Figure 4)

Figure 2: L3000N/L3092 + COMBO II



4. L303X (L3035/6/7) + COMBO II APPLICATION

Test network :



In Table 3 you can find the SLIC external components and the COMBO II programming coefficient for different countries followed by the application diagram (Fig. 3).

TX and RX gain are chosen in order to have :

0dBm0 ⇔ 0dBm 600 ohm (TXgain reg. = 83 ; RXgain reg. = AE)

Table 3.

	Administration	R. L. Test Netw.	SLIC Ext. Comp. (ZAC)	THL. Test Netw.	COMBO II Hybal Coeff.
1	600Ω FRANCE PUB. AUSTRIA (I) PRI. USA PRI. PORTUGAL PRI. KOREA	R1 = 600Ω R2 = 0 C1 = 0	R1 = 0 R2 = 26K C1 = 0	R1 = 600Ω R2 = 0 C1 = 0	EE 01 44
2	CHINA –A–	R1 = 200Ω R2 = 680Ω C1 = 100nF	R1 = 6K R2 = 34K C1 = 2nF	R1 = 200Ω R2 = 680Ω C1 = 100nF	EE 00 6E
3	CHINA –B–	R1 = 200Ω R2 = 560Ω C1 = 100nF	R1 = 6K R2 = 28K C1 = 2nF	R1 = 200Ω R2 = 560Ω C1 = 100nF	EF 12 2A
4	ITALY PRI.	R1 = 180Ω R2 = 630Ω C1 = 60nF	R1 = 5K R2 = 31.5K C1 = 1.2nF	R1 = 0 R2 = 750Ω C1 = 18nF	F0 01 9B
5	ITALY PUBL.	R1 = 600Ω R2 = 0 C1 = 0	R1 = 0 R2 = 26K C1 = 0	R1 = 0 R2 = 1.1K C1 = 33nF	E5 11 C0
6	GERMANY AUSTRIA AUSTRALIA PR. SWITZERLAND	R1 = 220Ω R2 = 820Ω C1 = 115nF	R1 = 7K R2 = 41K C1 = 2.3nF	R1 = 220Ω R2 = 820Ω C1 = 115nF	EF 11 C2
7	AUSTRIA (II) PRIV.	R1 = 220Ω R2 = 820Ω C1 = 115nF	R1 = 7K R2 = 41K C1 = 2.3nF	R1 = 220Ω R2 = 1.2K C1 = 150	EB 23 FB
8	BELGIUM PRI.	R1 = 150Ω R2 = 830Ω C1 = 72nF	R1 = 3.5K R2 = 41.5K C1 = 1.44nF	A: R1 = 150Ω R2 = 830Ω C1 = 72nF	 FF 00 6E
				B: R1 = 600Ω R2 = 0 C1 = 0	 F7 01 06
9	DENMARK	R1 = 400Ω R2 = 500Ω C1 = 330nF	R1 = 16K R2 = 25K C1 = 6.6nF	R1 = 300Ω R2 = 1K C1 = 220nF	E9 22 39
10	NETHERLANDS	R1 = 600Ω R2 = 0 C1 = 0	R1 = 26K R2 = 0 C1 = 0	R1 = 340Ω R2 = 422Ω C1 = 100nF	EA 01 24
11	NORWAY	R1 = 120Ω R2 = 820Ω C1 = 112nF	R1 = 2K R2 = 41K C1 = 2.24nF	R1 = 120Ω R2 = 820Ω C1 = 110nF	EF 12 4C

	Administration	R. L. Test Netw.	SLIC Ext. Comp.	THL. Test Netw.	COMBO II Hybal Coeff.
12	SWEDEN	R1 = 200Ω R2 = 1K C1 = 100nF	R1 = 6K R2 =50K C1 = 2nF	R1 = 0 R2 = 900Ω C1 = 30nF	F3 01 6F
13	FINLAND	R1 = 270Ω R2 = 910Ω C1 = 120nF	R1 = 9.5K R2 = 45.5K C1 = 2.4nF	A: R1 = 270Ω R2 = 1.2K C1 = 120nF	 EB 11 77
				B: R1 = 390Ω R2 = 620Ω C1 = 100nF	 F1 01 EF
14	FRANCE PRI.	R1 = 215Ω R2 = 1K C1 = 137nF	R1 = 6.75K R2 = 50K C1 = 2.74nF	R1 = 600Ω R2 = 0 C1 = 0	F8 00 0F
15	GREECE	R1 = 400Ω R2 = 500Ω C1 = 50nF	R1 = 16K R2 = 25K C1 = 1nF	R1 = 220Ω R2 = 820Ω C1 = 115nF	ED 23 92
16	SPAIN	R1 = 220Ω R2 = 820Ω C1 = 120nF	R1 = 7K R2 = 41K C1 = 2.4nF	R1 = 220Ω R2 = 820Ω C1 = 120nF	EF 12 DF
17	UK PRI.	R1 = 300Ω R2 = 1K C1 = 220nF	R1 = 11K R2 = 50K C1 = 4.4nF	R1 = 370Ω R2 = 620Ω C1 = 310nF	F4 12 6B
18	UK PUB.	R1 = 370Ω R2 = 620Ω C1 = 310nF	R1 = 14.5K R2 = 31K C1 = 6.2nF	Note 1 A: SHORT LINE B: LONG LINE (S. GAUGE) C: LONG LINE (L. GAUGE)	 EE, 12, CC EE, 38, 1A E9, 36, EA
19	USA PUB.	R1 = 900Ω R2 = INF. C1 = 2.16µF	R1 = 39K R2 = 180K C1 = 55nF Note 3	Note 2 A: LOAD LINE B: NOT LOAD LINE	 E6, 20, 48 F2, 20, A0

Notes :

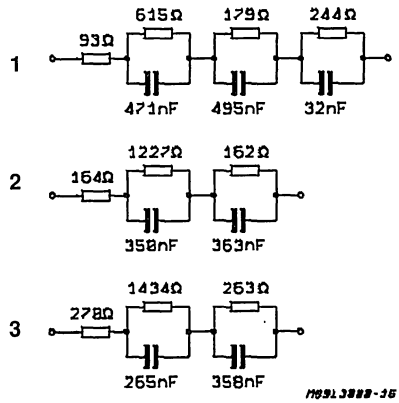
1. U.K THL TEST NETWORKS (see Figure 3)

2. U.S. THL TEST NETWORKS (see Figure 4)

3. CCOMP = 100pF; Rp = 62Ω; Rs = 6.2K

4. CREV is used for reversal polarity transition time programming only with L3037. With L3035/6 this pin is shorted to AGND. (see Figure 5)

Figure 3:



1. Short lines
2. Long lines (small gauge)
3. Long lines (large gauge)

Figure 4:

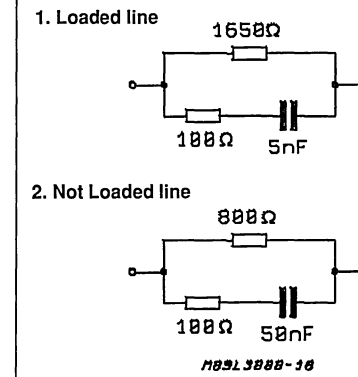
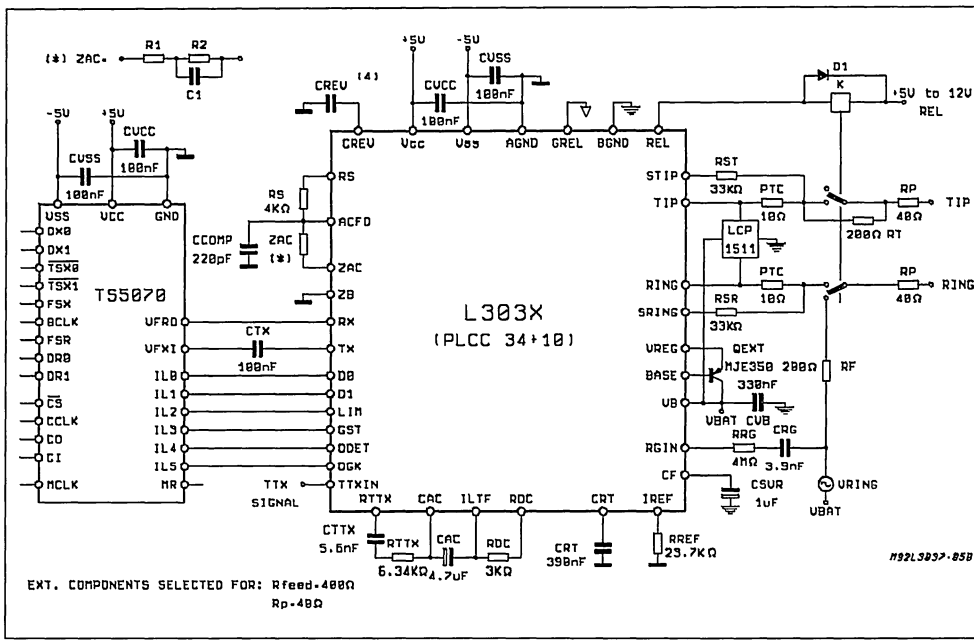


Figure 5: Typical Application Circuit (Full Feature) TS5070 + L303X + LCP1511.



L3000N/L30XX SLICs PROTECTION CIRCUITS

by W. Rossi

INTRODUCTION

In this application note are described different ways to protect L3000N/L30XX SLIC KITs.

The L3000N/L30XX are, COMPARED TO STANDARD SOLUTIONS, more complex to protect because the positive battery can be either GND or VB+ (typ. + 72V) depending on the SLIC operating mode. In the following three protection solutions for the L3000N/L30XX KITs are described.

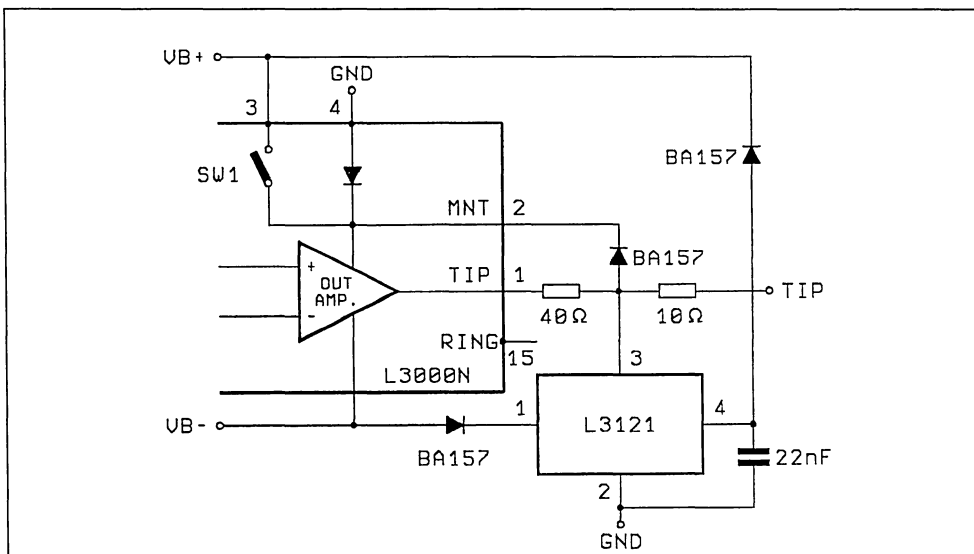
The first solution is based on programmable transient suppressor L3121; and this is the most complete one: another simpler solution, based on standard transient suppressor like LS5120 or TRISIL is proposed. Finally a way to use only one transient suppressor for more subscribers is described.

L3000N/L30XX PROTECTION CIRCUIT BASED ON PROGRAMMABLE TRAN-SIENT SUPPRESSOR L3121

In fig. 1 you can see the circuit configuration used to protect the L3000N/L30XX SLIC KITs with L3121. (The same structure is applied to the RING termination). When the voltage on the line increase above VB+ (typ +72V) or decrease below VB (typ. -48V) the transient suppressor L3121 intervenes and shorts the wire to ground.

For each wire we need one L3121 ; one 22nF capacitor to increase the intervention speed and three diodes : two to program the intervention voltage levels and one to pull up the supply voltage of the internal stages in order to avoid reverse voltage between line termination and supply voltage. In fact if you look at fig. 2.1. you can see that the internal output stage of the device can be fed either by GND or by VB+ depending on the status of the internal switch SW1. Since in normal operation the circuit is fed by GND and the protection intervenes when the line voltage exceeds VB+ it is evident that the reverse voltage between line termination and supply can damage the device. To avoid this fact a diode connected between line and supply increases the supply voltage when the line voltage increases (see fig.1).

Figure 1: Protection Circuit for L3000N (half section)



L3000N/L30XX PROTECTION CIRCUIT BASED ON STANDARD TRANSIENT SUPPRESSOR AS L5120 OR TRISIL.

In this paragraph is described a cheaper solution (respect to the one described in par. 2) to protect L3000N/L30XX SLIC KITs.

The protection circuit is based on two LS5120 or equivalent TRISIL, a polarity guard and two diodes to avoid reverse voltages between line termination and internal stages supply (see par. 2). The two external 50ohm resistors are splitted in three parts.

See the circuit of fig. 2.

If a surge is induced on the line the LS5120 intervenes and within 100ns it clamps the surge. During the first 100ns the LS5120 works like a 180V Zener Diode. The polarity guard avoid this 180V pulse to reach SLIC line terminations shorting it to the supply voltage (see fig. 3.1.).

Two capacitors C1 and C2 guarantee that in presence of negative or positive surges the supply vol-tage remain constant enough. These capacitors can be easily dimensioned considering that the 100ns current peak flowing through the polarity guard is equal to about 110V/10Ω = 11A in the case of positive surges and about 130V/10Ω = 13A in the case of negative ones.

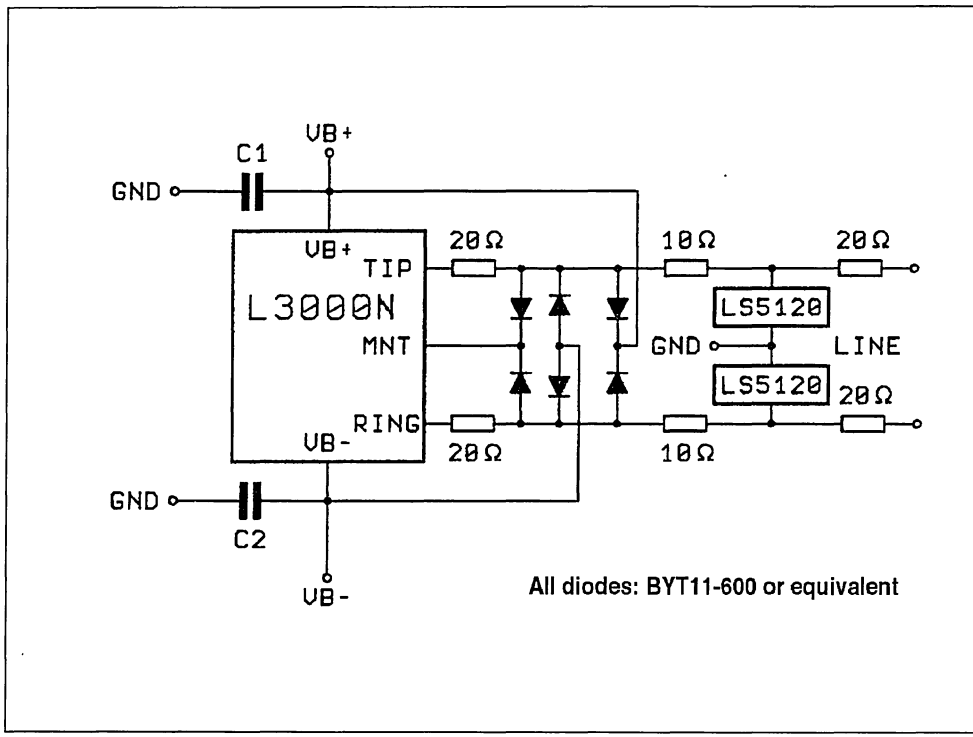
For negative surges (worst case) the charge Q injected in the capacitor is 13A x 100ns=1.3μC (supposing that no current flows through the power supply) therefore a 1μF capacitor is large enough to guarantee a less than 1.5V supply variation.

If instead of LS5120 another similar device like Trisil is used the capacitors C1 and C2 have to be dimensioned depending on the clamping time of such device.

It should be noted that the diode type used in the polarity guard is important in order to guarantee good performances. The suggested diodes for this application are BYT11-600 or equivalent. We observe that this kind of diodes in presence of a 10A, 200ns current pulse show a voltage drop of about 3V, while diodes as 1N4004 in presence of the same pulse shows a vol-tage drop ten times larger (30V).

It should be noted that in presence of power cross the V_{B+} supply should be able to sink current and the V_{B-} to source current.

Figure 2: L3000 Surge Protection Circuit Based on LS5120.



L3000N/L30XX COMMON PROTECTION CIRCUIT FOR MORE SUBSCRIBERS BASED ON PROGRAMMABLE TRANSIENT SUPPRESSOR L3100.

In this solution each SLIC is protected by means of a polarity guard that, in case of a surge, avoid the line terminations to exceed the supply voltages. In the following page you can see the circuit schematic of this solution.

Consider that in this application the current peak flowing through the polarity guard can reach 100A for 3KV surges ; therefore proper diodes must be used in order to avoid excessive voltage drop in presence of such current peak.

When a positive (negative) surge occurs on one line the common protection P1 (P2) clamps all the lines to ground.

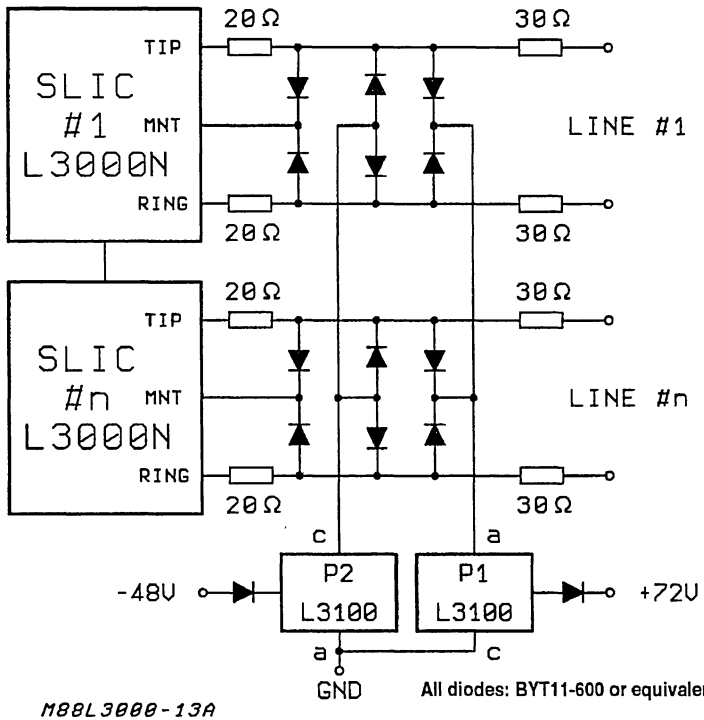
Since when you short a line termination to ground the SLIC can source or sink (depending on the line termination status) up to 100mA, it can happens that once finished the surge the protection remain clamped because of the line currents.

If this fact happens all the SLICs connected to the same protection detect ground key, in this way the controller can recognize that one protection is clamped.

One possible way to open clamped protection (once the surge is finished) is to set all the SLICs connected to it in power down mode for a short time. In this way for a moment no current flow through protection allowing it to open.

Finally the protection intervention time can be further improved connecting one 6.8nF/100V capacitor between pin 1 and pin 3 of each L3100.

Figure 3: L3000 Common Protection Circuit.



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

M3488 DIGITAL SWITCHING MATRIX

INTRODUCTION

The M3488 DIGITAL SWITCHING MATRIX device can be used as a basic component in modern digital switching systems.

This Technical Note is a guide for designers who wish to use the M3488 in their systems.

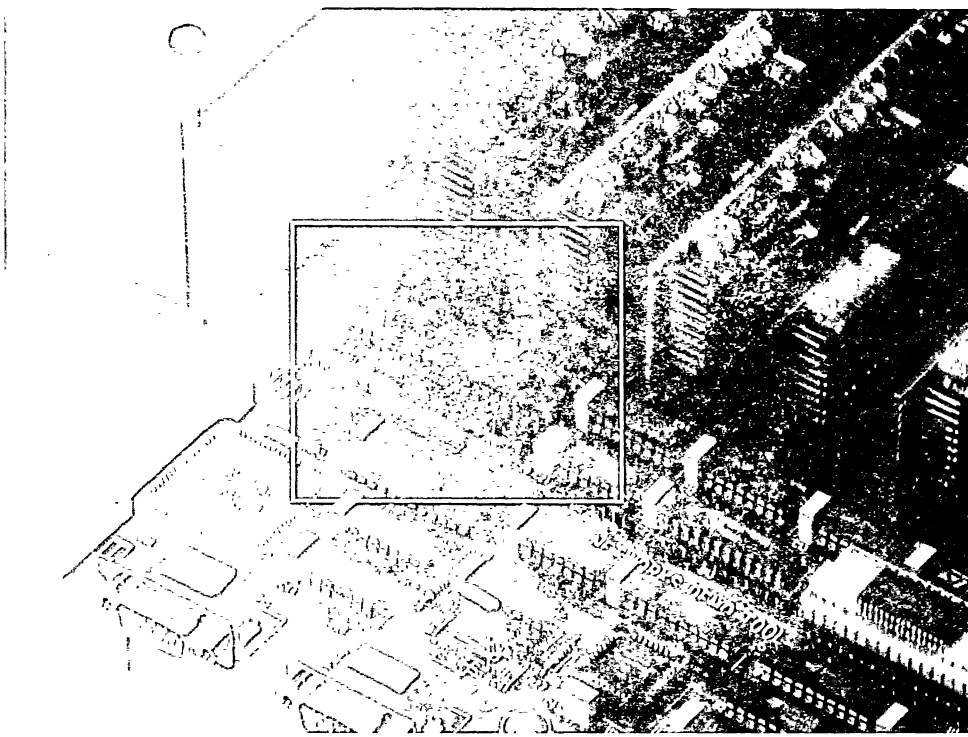
Section 1 contains introductory material in the field of digital switching and can be quickly passed over by experienced designers.

The main characteristics of the M3488 are shown in Section 2.

Sections 3 and 4 describe, respectively, the internal structure, and the various functions which may be implemented.

Some detailed material concerning timing and some important services are examined in Section 5.

Section 6 is dedicated to applications. Another component, the M3116, used in this field, is introduced in this section ; of particular note is the fact that the M3116 is a digital device which realizes conference and tone generation functions.



1. DIGITAL SWITCHING TUTORIAL

WHAT IS A DIGITAL SWITCHING MATRIX (DSM) ?

A Digital Switching Matrix is a device which permits switching a certain number of signals among themselves.

The signals to be switched can either be digital or analog ; in the latter case, digitalization of these signals must be provided before switching takes place.

Digitalization takes place in three stages :

a) band limiting (by a low pass filter) ;

b) sampling ;

c) digital coding.

PULSE CODE MODULATION (PCM)

The technique of digitalizing signals used in telephonic applications is called PCM.

The signal to be digitalized is sampled every 125 µs, in other words, with a frequency equal to 8 KHz since, according to the Nyquist law, the sampling frequency must be greater or equal to twice the maximum frequency of the analog signal being sampled. As is well known in telephony, this frequency is less than 4 KHz.

Based on input signal sampling (see fig. 1-1), the coding links a given sample to an 8-bit binary number.

Thus, the number of discrete levels becomes $2^8 = 256$.

Non-linear coding laws are used. The main ones are the two following :

- Mu law used in the USA, Canada and Japan ;
- A law used in Europe, South America, Australia and Africa (see fig. 1-2).

Since the sampling frequency is 8 KHz, the digitalized signal will be made up of a number of bits per second equal to (8 • 8000) = 64000 bit/s.

TIME DIVISION MULTIPLEXER (TDM)

TDM is a technique which permits merging various digital signals into a single high velocity signal. Many stages of switching will, thus, become easier.

Fig. 1-3 presents a diagram of the TDM principle.

TDM is based on the serializer, which accepts PCM signals at the input, and provides them at the output, accessed cyclically.

Each input channel is linked to a time slot, and is thus fixed precisely in the serialized output stream.

Figure 1.1 : SAMPLING & CODING. The Analog Signal to be digitalized is First Bandwidth limited (fig. 1.1a) Then Sampled at a Frequency f_s (fig. 1.1b). The Resulting Periodic Sequence of Samples is shown in Fig. 1.1c. Each Sample is then replaced with an 8–Bit Word representing the Amplitude (fig. 1.1d).

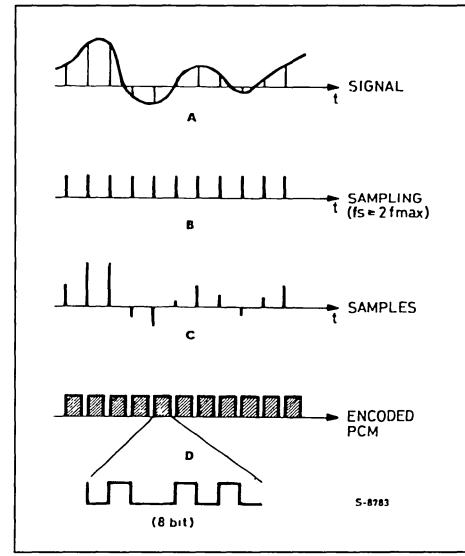
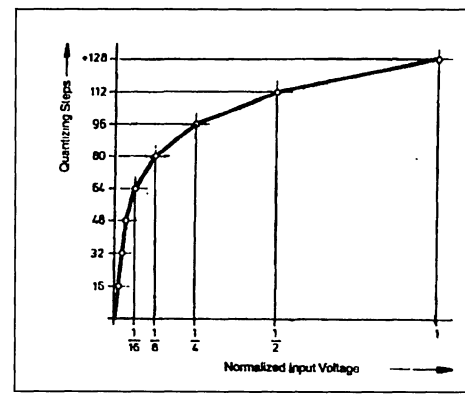


Figure 1.2 : The Quantization Curve for A-law Limited to Positive Samples. Each Group of 16 Steps is Contained in a Segment and the Normalized Values of the Input Signal Corresponding to the Extremes of Each Segment are One Half of Each Other.



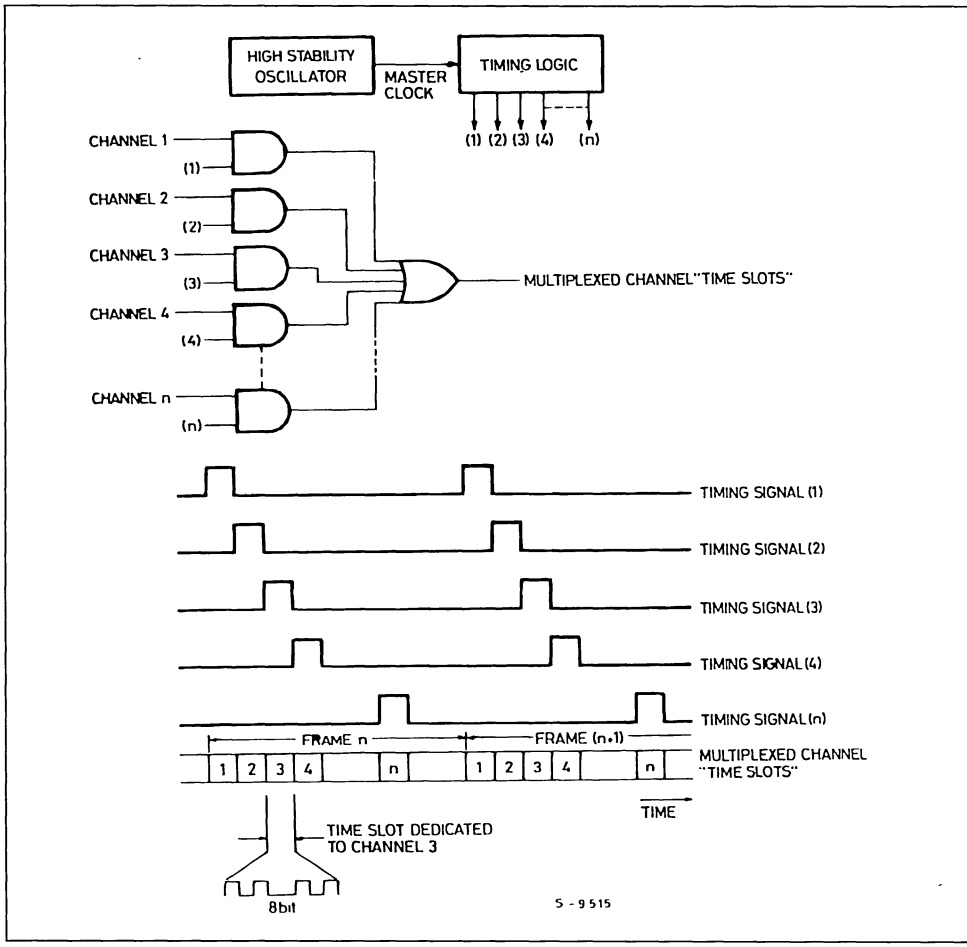
A very stable oscillator provides the master clock and all the timing functions used in the multiplexer.

The international standards for the TDM are two, namely :

a) the North American Standard (PCM 24 Transmission System) ;

b) the European Primary System (PCM 30 Transmission System) ;

Figure 1.3 : The Basic Principle of Time Division Multiplexing (TDM). Data from n Independent Channels are Compressed and Transferred to a Single Output. Each Channel Outputs Its Data in Separate Time Slots Defined by a Timing Circuit.



THE NORTH AMERICAN STANDARD (PCM 24)

Fig. 1-4 presents the PCM 24 Transmission System frame format.

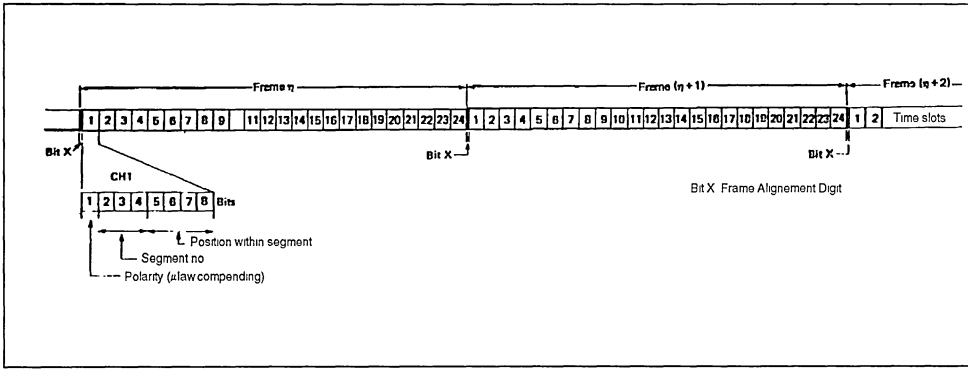
Each of the 24 channels has already been sampled at 8 KHz and coded, using Mu law with 8-bit words.

Messages reaching the channels are word interleaved, forming an uninterrupted sequence of 192 bits.

A single alignment framing digit (bit X) is inserted at the beginning of each sequence ; thus the total number of digits in a frame is 193. The velocity of the signal in bit/s is thus (8000 · 193) = 1544 Kbit/s.

In certain applications, usually PABX, the Extra bit (bit X) is omitted. In this last case the velocity of the signal becomes (8000 · 192) = 1536 Kbit/s.

Figure 1.4 : Frame Format of the Bell T1 (PCM24) System. Each Frame Contains 24 Channels PLus One Signalling Bit (bit X). This Format is Used in the USA, Canada and Japan.



THE EUROPEAN PRIMARY SYSTEM (PCM 30)

Fig. 1-5 shows the European Primary System frame format.

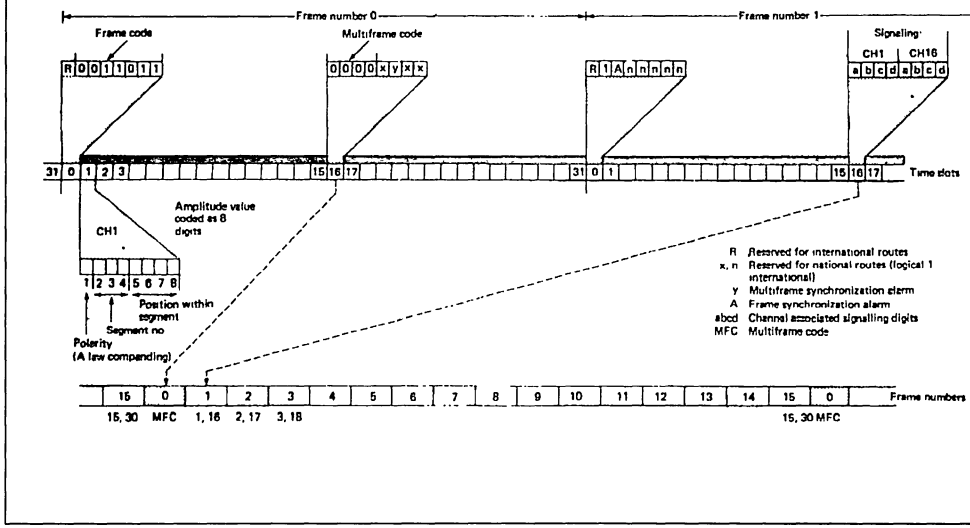
TDM combines 30 voice channels, sampled at 8 KHz, and coded using A law with 8-bit words.

Various channels messages are combined by word interleaving ; thirty 8-bit words are inserted in a frame with 32 time slots, numbered from 0 to 31.

Two of the slots (0 and 16) are used for frame alignment and signalling.

Each frame has (8 · 32) = 256 bits, and its velocity is (8000 · 256) = 2048 Kbit/s.

Figure 1.5 : Frame Format of the European System (PCM30). Each Frame contains 32 Channels of which two are dedicated to signalling. This Format is used in Europe, Latin America, Australia and Africa.



TIME AND SPACE DIVISION SWITCHING

Fig. 1-6 represents, using blocks, a digital switching system. Individual analog lines are applied to a multiplexer, which provides for their digitalization and merges them into a frame.

The various frames are transmitted to the switching matrix which carries out exactly the switching function, building various output frames as required.

These frames are transmitted to a demultiplexer which separates them into single channels, which, after conversion from digital to analog, are transmitted to the respective analog output lines.

Fig. 1-6 presents an example : subscriber S1-5 wishes to be connected to subscriber S8-11 ; S1-8 with S4-10.

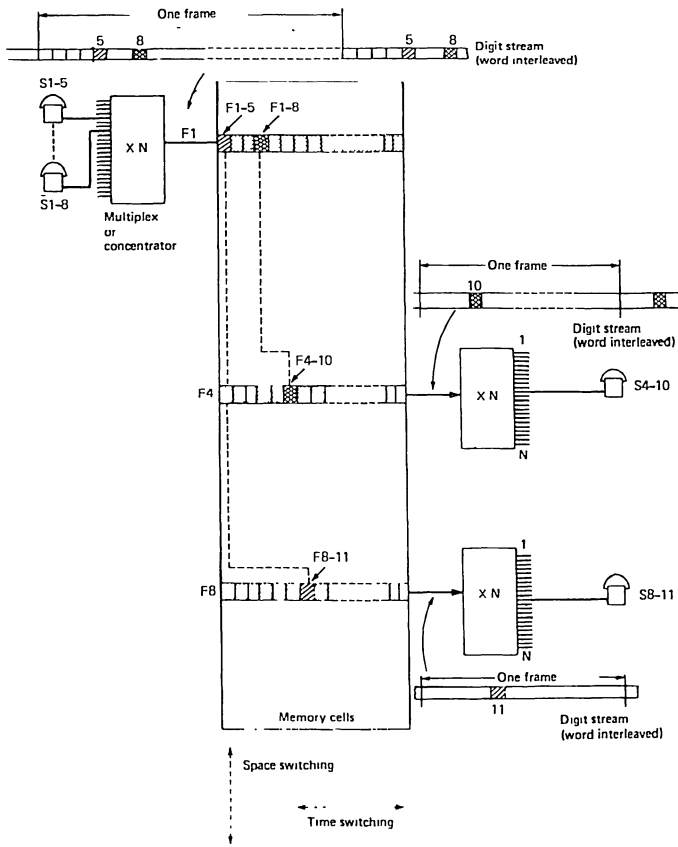
The connection operation between S1-5 and S8-11 involves two operations :

1) transfer of information from layer F1 to layer F8 (space division switching) ;
2) transfer from position 5 to 11 (time division switching).

Likewise, the connection between S1-8 and S4-10 involves space switching between F1 and F4, and time switching between positions 8 and 10.

SGS THOMSON digital switching matrixes operate, using this technique of time and space division switching, permitting switching without blocking, in other words, simultaneously of 256 channels.

Figure 1.6 : Space-and-Time-switching Digitally encoded Signals.



2. INTRODUCTION TO THE M3488 DSM

GENERAL DESCRIPTION

The M3488 device implements a non-blocking digital switching matrix, which operates with a maximum of 256 x 256 channels.

These channels are applied and extracted from the device, using 8 PCM frames at 2048 Kbit/s, each containing 32 channels.

The M3488 can connect each input channel with, or disconnect it from, any output channel in addition to carrying out other functions described in Section 4.

It can also be used at lower velocity, for example, to switch 192 x 192 channels, organized in eight frames of 24 channels each, at 1544 Kbit/s, using the North American Standard (PCM 24) or at 1536 Kbit/s.

Finally, there is no prohibition against using the device for non-standard applications, for example, in the field of Data Communications. A few examples are cited in Section 6.

KEY FEATURES

- A 256 input and 256 output channels digital switching matrix ;
- A building block designed for large capacity electronic exchanges, subsystems, voice-data PABXs ;
- European Primary System compatible (32 channels per frame) ;
- North American Standard (T1 System) compatible (24 channels par frame) (*) ;
- PCM input and output mutually compatible ;
- Actual input-output channel connections stored and modified using an on-chip 8-bit parallel microprocessor interface.
- 6 main functions or instructions available ;
- 5-volt power supply ;
- MOS and TTL input/output levels compatible ;
- High density advanced 1.2µm HCMOS3 process.

(*) For further information, see below, Section 6.

3. M3488 INTERNAL STRUCTURE

The component includes a Speech Memory, Control Memory, circuits for Serial to Parallel Conversion of incoming PCM links and for Parallel to Serial Conversion of the outgoing PCM links and a Bidirectional Interface for an 8-bit microprocessor. In addition, the M3488 performs other useful functions, such as Byte Insertion and Extraction, Addressing Memory Reading and 0 Channel Extraction. Referring to Fig. 3-1, the following functional blocks can be distinguished :

- Time Base
- Serial Parallel Converter for the PCM input links
- Speech Memory
- Control Memory
- Internal PCM Bus
- Parallel Serial Converter for the PCM output links
- Control and Interface Logic to and from the µP

TIME BASE

The time base generates the internal synchronous timing signals, using only two external signals, the clock (4.096 MHz) and the frame synchronism (8 KHz), supplied to the corresponding external pins of the device (CK and SYNC pins). The time base provides two ring counters, generating two sets of timing signals (e1 to e8 and u1 to u8), used for Serial to Parallel Conversion of input time slots and Parallel to Serial reconversion of output PCM time slots, respectively.

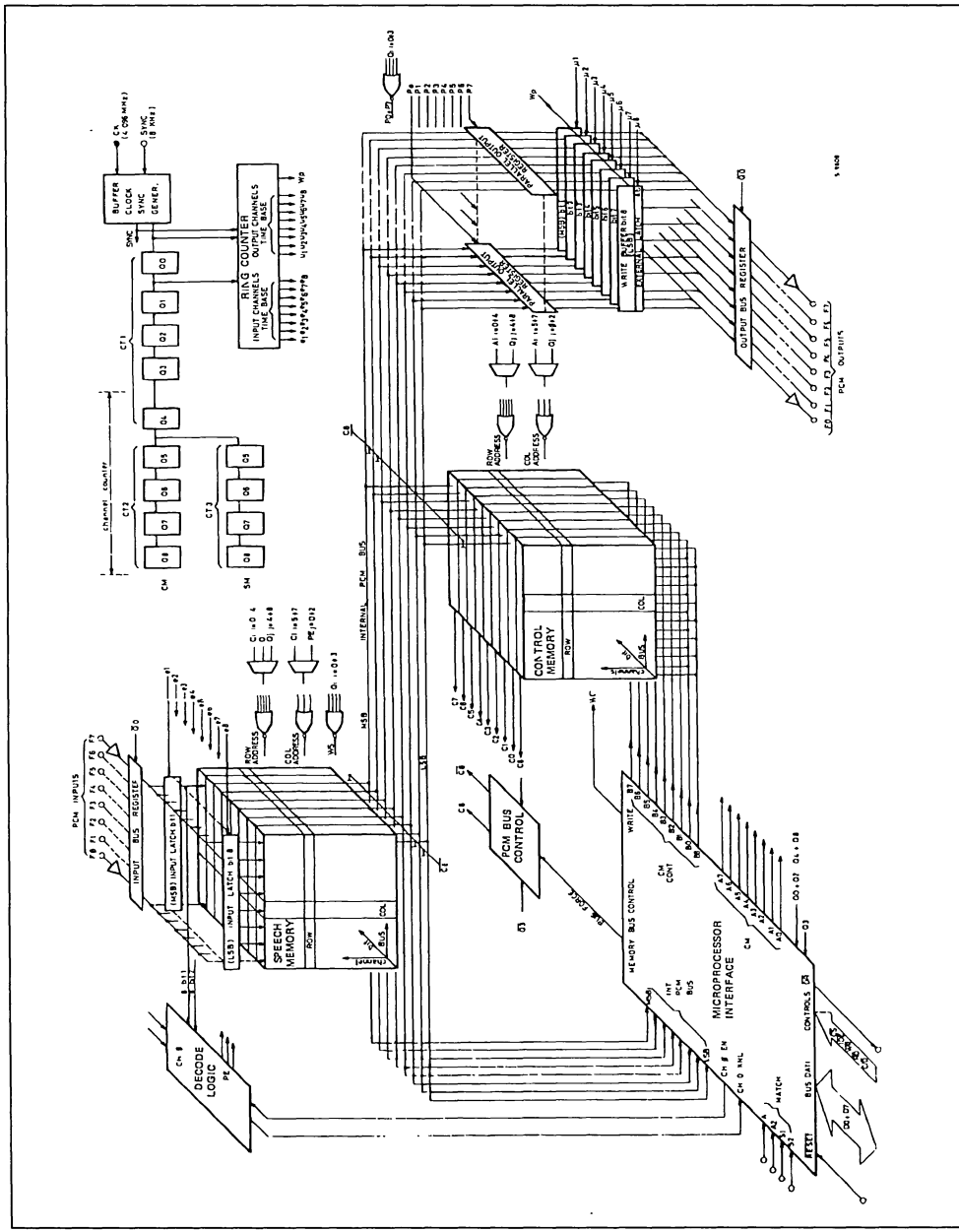
The time base consists mainly of a fast synchronous parallel resettable counter of which stages are obtained by repeated clock division and grouped into three subsets : the first, CT1, starting from the 250ns rate, generates the time phases controlling the 4µs input and output time slot servicing ; in particular, the signal Q3 (4µs) specifies two working phases : one dedicated to the microprocessor interface operations, the other related to PCM operations. The other two subsets, CT2 and CT3, operating synchronously with respect to CT1, generate the sequential channel addresses for control memory reading and for speech memory reading, respectively.

The counter CT2 addresses the control memory, using the output PCM channel address increased by one ; the counter CT3 addresses the speech memory, using the input PCM channel address decreased by one. This address difference is necessary to compensate for the internal component delay due to input and output PCM conversion.

INPUT SERIAL TO PARALLEL PCM CONVERTER

During each time slot (4µs), the 8 serial PCM (2048 Kbit/s) input bits are regenerated and sampled using a 500 ns clock signal, Q0, and then are stored in 8-bit latches clocked by the input ring counter's e1 to e8 signals. As soon as the 64 bits are updated, they are written, using a single write pulse, into the speech memory at the corresponding input channel address, selected by subset counter CT3, performing the parallel conversion in the same writing operation.

Figure 3.1 : The Fundamental Blocks are the Speech Memory (SM), which memorizes for Each Frame the Contents of All 256 Channels, and the Control Memory (CM) which contains Information on the Status of the 256 Output Channels (connected or not connected, loaded by the micro with a given byte).



SPEECH MEMORY

The memory is organized as 32 planes of 8 rows and 8 columns each ; every plane corresponds to an input PCM channel, every row to a bit of content and every column to an input PCM line. The working cycle is about 4µs, with this time divided into 2µs phases. The first one consists of eight 250 ns cycles : one particular cycle is devoted to memory updating according to input channel data ; in the other cycles, functions engaged by the µP interface logic can be performed at random in the memory (that is the case of PCM output channel reading). In the second, memory is cyclically read 8 times, using the control memory addresses, C0 to C7 (switching function).

CONTROL MEMORY

Control Memory is organized in 32 planes of 9 rows and 8 columns each ; every plane corresponds to any output PCM channel, every row to a content bit and every column to an output PCM line. The Control Memory working cycle is similar to the Speech Memory.

During the first 2µs phase, the Control Memory is idle and normally accessible to µP interface. On occasion, because of network connection updating or µP requests, some cycles are stolen here for this purpose. During the latter 2µs phase, the memory is read eight times, using the addresses coming from the time base (subsets CT1 and CT2). The output contents of 9 bits each are used as addresses for Speech Memory (C0 to C7) and as a control signal for switching the internal PCM bus to the proper Control or Speech Memory output data (C8).

INTERNAL PCM BUS

Speech and Control Memories are connected to the internal 8-bit parallel bus. The 9th Control Memory bit controls each memory's output during the switch function ; otherwise, it is forced by the µP interface.

The internal bus is connected on one side to the µP interface to perform functions like memory content transfer. On the other side, the bus connects the PCM Parallel to Serial conversion unit.

OUTPUT PARALLEL TO SERIAL CONVERTER

The bytes of the internal PCM bus, belonging to the 8 cycles previously mentioned in Control Memory, are saved in a group of 8 temporary registers, each selected by the timing signals P0 to P7 (see fig. 3-1). When all bytes are stored, a single pulse transfer takes place in order to supply new PCM data to the output registers.

The proper time phases u1 and u8 sequentially scan the 8 output registers and simultaneously feed the output pins performing the Parallel to Serial conversion. The output PCM flows are resynchronized, using a 500ns clock signal (Q0). PCM outputs are open drain type.

MICROPROCESSOR INTERFACE LOGIC

The interface logic controls, asynchronously with respect to the PCM timing, the 8 bit data bus and the control bus to and from the microprocessor. It also stores, in a five byte stack, the data field and the opcode instruction. It gives the other internal blocks the necessary signals to perform the function in the right time phase. Moreover, it stores the status information, which can be read by the µP for diagnostic purposes, in two internal registers, OR1 and OR2.

The external control bus allows the component to be used as a standard 8-bit peripheral device. It consists of RD and WR signals for reading and writing into the M3488 respectively, and the C/D signals, which selects between data and operating the code of command bytes to the written into the M3488. Signals CS1 and CS2 activate the component when other peripheral devices are connected to the same bus.

Signals A1, S1, A2 and S2 allow more M3488s to be connected in a simple way to obtain non-blocking matrix structures. An M3488 in a match condition where A1 = S1 and A2 = S2 is active, while the others are automatically disabled.

4. FUNCTIONAL DESCRIPTION

The device, controlled by the microprocessor, implements six different instructions. A specific function is executed after the microprocessor has transmitted, using the data bus, the data bytes and the command bytes.

Two or four data bytes carry the information necessary for the correct interpretation of the function. The command byte follows these with the operative coding information necessary for M3488 to execute the function.

Brief descriptions of individual functions are given here. For further information, the M3488 data sheet for the device should be consulted.

FUNCTION 1 : CHANNEL CONNECTION/DISCONNECTION

This function permits the formation of a new connection between a given input channel (C_{IN}) and a given output channel (C_{OUT}). See fig. 4-1.

The message coming from the microprocessor consist of four data bytes plus a command byte.

The first two data bytes carry, respectively, information about the PCM input line and the input channel ; the third and fourth bytes carry information about the PCM output line and the output channel.

The first two bytes are loaded in the control memory cell (CM), the address of which is specified in the last two bytes.

It cases of switching systems of more than 256 x 256 channels some examples are given in Section 6 use is made of additional M3488 chips, interconnected as required (multi-chip matrices).

In this case, the connection function is executed only by the M3488 in match condition (A1 = S1 and A2 = S2) ; all the other M3488s of the multi-chip matrix involved with channel C_{OUT} will execute a disconnection operation from that selected output channel (C_{OUT}).

FUNCTION 2 : CHANNEL DISCONNECTION

Disconnect the selected output (C_{OUT}). See fig. 4-2.

The message coming from the microprocessor is made up of two data bytes plus a command byte.

The first and the second bytes carry, respectively, information about the PCM output line and the output channel which must be disabled.

FUNCTION 3 : BYTE INSERTION/CHANNEL DISCONNECTION

The function permits a byte furnished by the microprocessor to be inserted in an output data channel (C_{OUT}). See fig. 4-3.

The message is made up of four data bytes plus a command byte.

The first and second bytes contain information for transferral to the PCM output channel. This 8-bit information is memorized inside a control memory cell (CM).

The third and fourth data bytes contain, respectively, information on the PCM output lines and on the output channel in which the byte is to be inserted. These last bytes are used as an address to specify the CM cell in which to load the information contained in the first two data bytes.

As was the case for the first instruction examined, in the case of multi-chip matrices, this instruction is executed only by the selected M3488 ; all the remaining M3488s of the matrix will execute a disconnection operation on the selected output channel.

FUNCTION 4 : BYTE EXTRACTION

This function permits transferral of the byte contained in an output data channel to the microprocessor, using the data bus.

The message is made up of two data bytes plus a command byte.

The first and second bytes contain, respectively, the number of PCM output line and of the output channel, the contents of which are to be read by the microprocessor.

The PCM octet is memorized by the device in register OR1 ; thereafter, the microprocessor, using the aforementioned register's read cycle, transfers the PCM sample to the CPU.

If it is useful to read the PCM byte from an input data channel C_{IN}, C_{IN} must be connected with a particular output channel C_{OUT}, and thus apply the extraction function to C_{OUT}. See fig. 4-4.

Figure 4.1 : Connection Any of the 256 Input Channels (C_{IN}) can be Permanently connected to any of the 256 Output Channels (C_{OUT}). It is Possible tohave 256 Connections simultaneously.

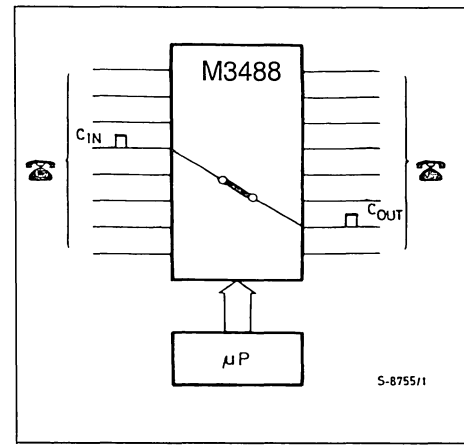


Figure 4.2 : Disconnection. Each Connection Previously made can be interrupted at any Time.

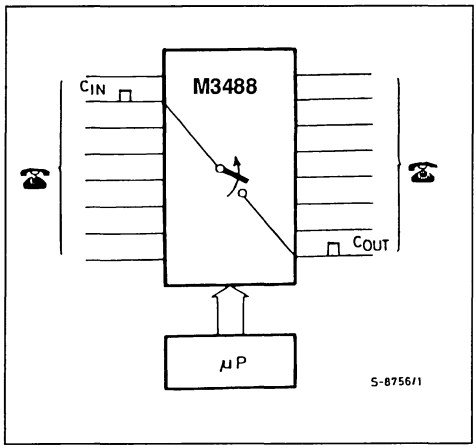


Figure 4.3 : Insertion of a Byte. The Control Microprocessor can send a given Byte to Any Output Channel.

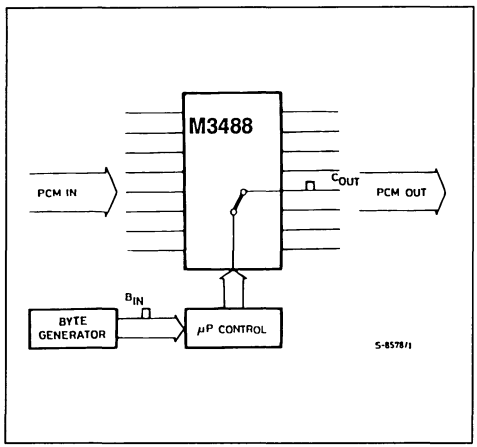
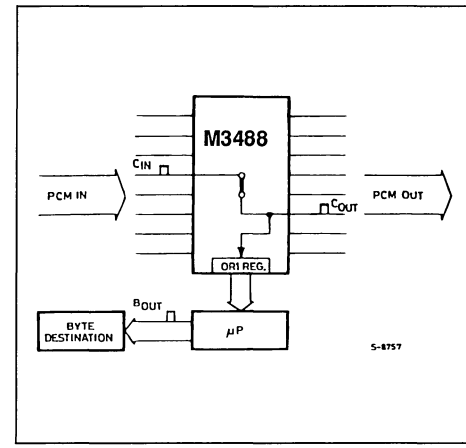


Figure 4.4 : Extraction of a Byte. The Micro Can Extract from Any Output Channel (C_{OUT}) the Contents (B_{OUT}) at the Time of the Request.



FUNCTION 5 : CONNECTION MAP READING

This function makes it possible to know, starting from a particular output channel C_{OUT}, the contents of the corresponding control memory cell CM, the address of which is exactly the same as C_{OUT}. See fig. 4-5.

As already explained in Section 3, each control memory cell CM is made up of nine bits (C8, C7.... C0).

If the ninth bit is equal to zero, the eight remaining bits (C7, C6.... C0) provide information concerning the input channel C_{IN} connected simultaneously with C_{OUT}. In particular, C7, C6 and C5 provide the PCM input line number, while C4, C3, C2, C1 and C0 provide the relevant C_{IN} channel number.

On the contrary, if bit C8 is equal to one, two possibilities can be examined :

a) byte C7, C6.... C0 is equal to 11111111 – in this case, output channel C_{OUT} is not connected to any input channel C_{IN}, and the microprocessor

never loaded any byte on the basis of instruction 3 ;

b) byte C7, C6.... C0 is not equal to 11111111 – also, in this case, the C_{OUT} channel is not connected to any input channel C_{IN}, however, the aforementioned byte is a copy of the one which the microprocessor has already loaded in C_{OUT}.

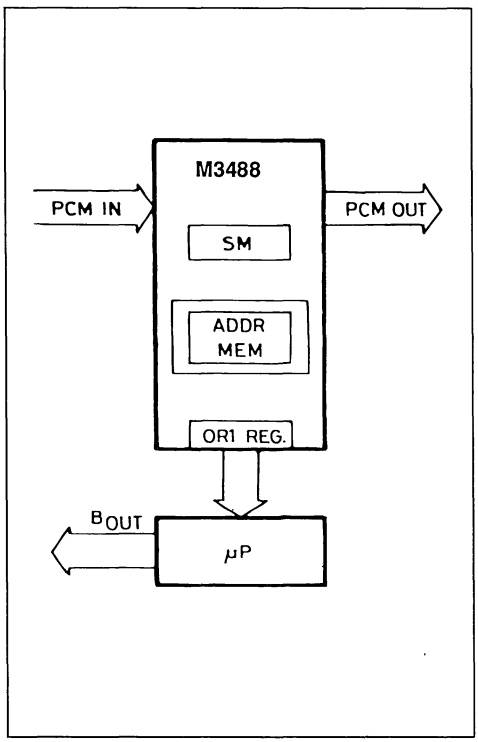
The message coming from the microprocessor is made up of two data bytes plus a command byte.

The first and second bytes correspond, respectively, to the number of PCM output line and to the C_{OUT} channel, and, as already mentioned, correspond to the CM cell address whose contents the microprocessor must read.

Bits C7, C6.... C0 are memorized in the OR1 register, while bit C8 is memorized in the OR2 register.

With two read cycles, the microprocessor can thus transfer the contents of the two registers OR1 and OR2 into the CPU.

Figure 4.5 : Reading the Control Memory. Through This Operation the Microprocessor Can Read the Status of Every Output Channel.



FUNCTION 6 : CHANNEL 0 CONNECTION MASK STORE/DATA TRANSFER

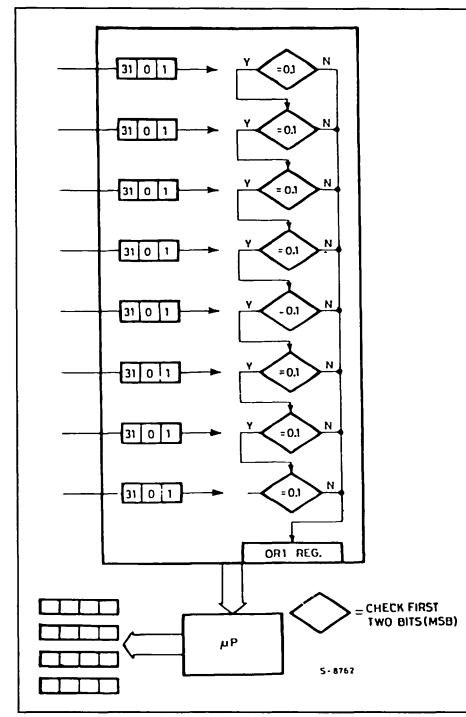
This last function is used to extract information rapidly from channel 0. See fig. 4-6. The indispensable requirement for the extraction to take place is that the two most significant bits of the byte contained in channel 0 not be equal to 01.

The PCM input lines from which the 0 channels are extracted are selected by using the microprocessor to load two data bytes, comprising the mask byte and a command byte.

The contents of channel 0 are available from the OR1 register, from which the microprocessor can transfer them externally by successive reads from the same register.

Experimental testing has shown that, with a CPU clock of 4.000 MHz in a time frame (125µs), it is possible to extract the 0 channels from all eight PCM lines.

Figure 4.6 : Rapid Extraction of Channel 0. Allows the Extraction of the Contents of the Active Channel Zeros and Channels with the Most Significant Bits Not Equal to 01.



5. VARIOUS NOTES AND CONSIDERATIONS ABOUT THE M3488

In this section, certain aspects of the timing and operation of the device will be described in some detail.

In order to better understand the subject matter, it is recommended to have already read the component's data sheet.

SYNC TIMING

One of the aspects which should be handled with particular attention in the use of the component is the timing relation between the synchronization signal ($\overline{SYNC}$) and the clock signal (CK).

The $\overline{SYNC}$ signal, specifically its rising edge, specifies the beginning of the frame and, thus, bit 0 of channel 0.

The zone sketched in fig. 5-1 shows the areas of possible transition of the rising and falling edges of the $\overline{SYNC}$ signal with respect to the CK signal.

The absolute value of the width of this zone (t_V) is :

$$t_V(\overline{SY}) = t_{CK} - t_R - t_{HL}(\overline{SY}) - t_{SH}(\overline{SY})$$

in which :

$t_V(\overline{SY})$ is the maximum time width of the area of the rising edge of SYNC ;

t_{CK} is the clock (CK) period ;

t_R is the maximum clock (CK) rise time (= 25 ns) ;

$t_{HL}(\overline{SY})$ is the $\overline{SYNC}$ minimum low level hold time (= 30 ns) ;

$t_{SH}(\overline{SY})$ is the $\overline{SYNC}$ minimum high level set-up time (= 80 ns).

The falling edge of $\overline{SYNC}$ can take place anywhere if the length of level 1 is greater or equal to t_{CK} and the length of level 0 is greater than or equal to :

$$t_{SL}(SY) + t_R + t_{HL}(SY) = 115 \text{ ns},$$

$t_{SL}(\overline{SY})$ being the $\overline{SYNC}$ min low level set-up time (60 ns).

PCM INPUT SIGNAL TIMING

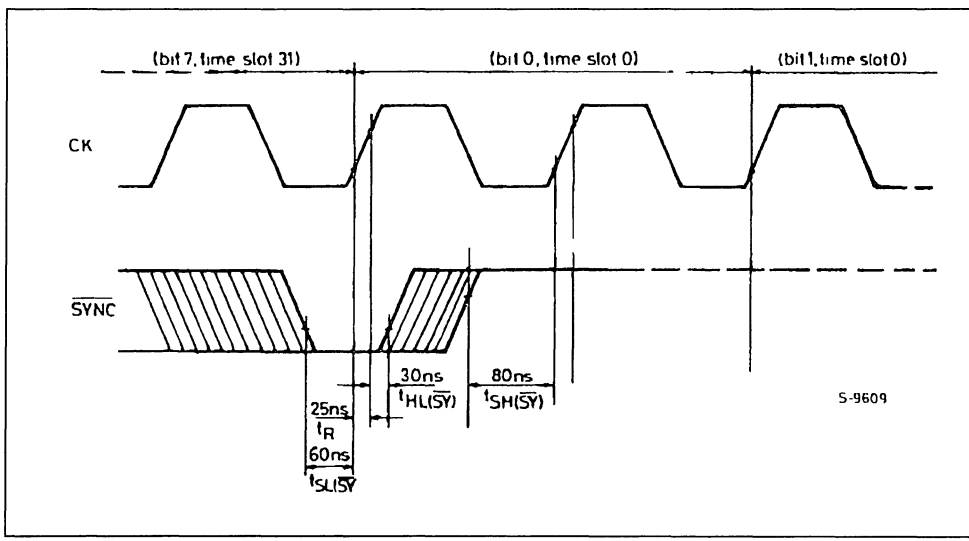
Another very important point is the timing relationship between the PCM input signals and the SYNC signal.

In many cases, it is of major importance to know how much the eight PCM input signals can be mutually dephased with respect to the CK signal.

Fig. 5-2 presents an example of dephasing of the general PCM input signal with respect to CK. To better illustrate this aspect in the figure, the PCM input signal is represented both with the minimum, and with the maximum, permissible delay.

In the same figure, an extremely interesting aspect is evident, namely, that the various PCM input flows

Figure 5.1 : SYNC Signal Timing. The Shaded Zones are the Regions of Possible Transitions. The Rising Edge of SYNC Determines Bit 0 of Channel 0.



are able to mutually tolerate dephasing at a level of nearly one bit-time.

Indeed, the time variation between the PCM input signals with minimum and maximum permissible delays, t_V (PCM), is as follows :

$t_V (PCM) = (2 \cdot t_{CK}) - (t_H (PCM) + t_R (CK) + t_S (PCM))$

Therefore, referring to fig. 5-2 ;

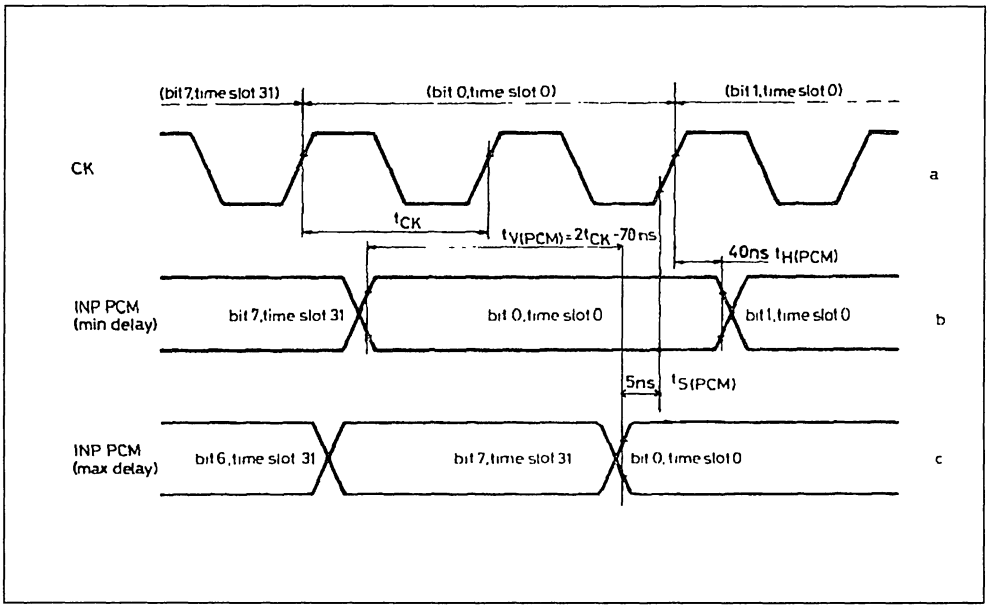
$t_V (PCM) = (2 \cdot t_{CK})$ -70 ns.

In the case of the European PCM (2048 Kbit/s), t_V (PCM) = 418 ns, or 86 % of bit-time.

In the case of the North American PCM (1544 Kbit/s, t_V (PCM) = 577 ns, or 89 % of bit-time.

This fact suggests one of the component's possible alternative applications, namely that of the PCM flow rephaser for delays included in values which have already been mentioned.

Figure 5.2 : Timing of the PCM Input Signal (INP PCM). This Diagram Illustrates the Cases of (INP PCM) with the Minimum (b) and Maximum (c) Tolerated delay Referred to the Clock Period (a) Corresponding to Bit 0 of Channel 0. Note That the Regions of Possible Variation Correspond to Almost One PCM Bit Period.



PCM OUTPUT SIGNAL TIMING

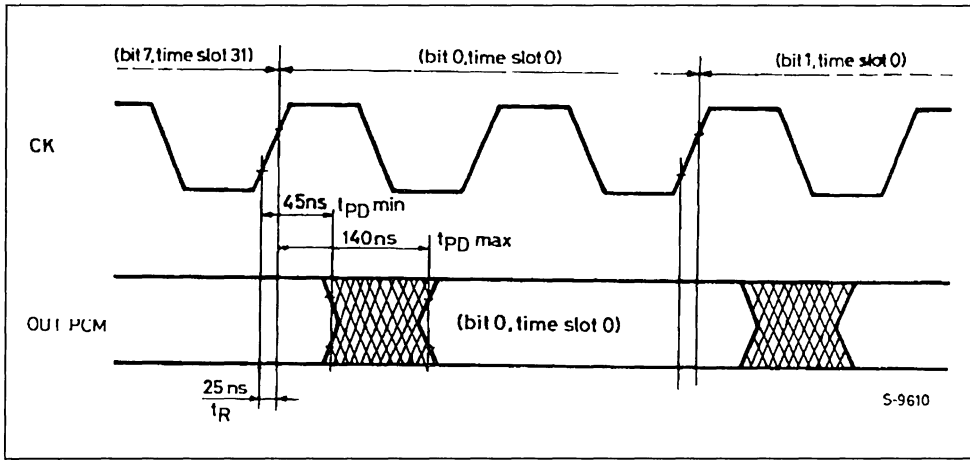
Fig. 5-3 shows the areas of variation of the edges of the PCM output signal with respect to the CK signal, the PCM input signal with maximum and minimum delay.

The width of such areas amounts to 155ns.

Also, the figure clearly indicates the possibility of using the PCM output flows as PCM input flows, in other words, to create a loop between the PCM outputs and inputs.

This could be used for test operations or for introducing frame delays into the PCM flow.

Figure 5.3 : Timing of the PCM Output Signal (OUT PCM). The Shaded Regions Indicate Where the Transitions May Take Place.



READ AND WRITE TIMING

The M3488 device requires that the PCM signals be correlated with the CK signal.

In theory, the microprocessor interface signals could be completely asynchronous with the CK signal.

In reality, that is completely true only in cases where M3488 is not inserted in a multi-chip matrix. In this last case, it is indeed to be recommended to link the RD and WR signals to the CK signal.

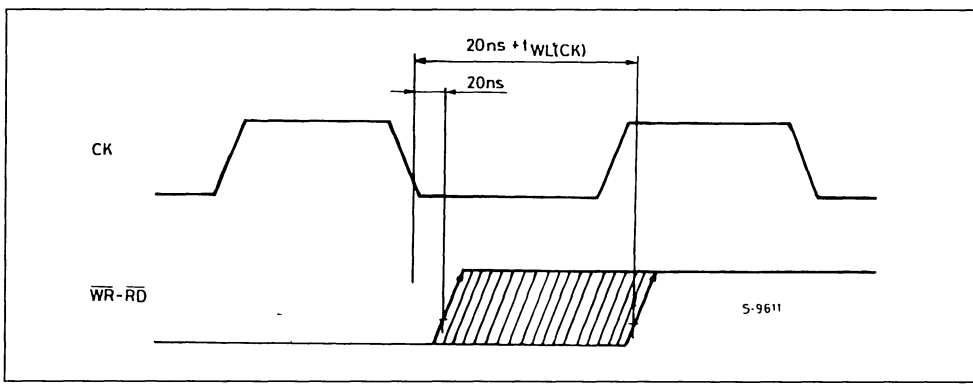
In particular, their rising edges must be delayed with respect to the falling edge of CK in a single phase, t_V (RW), in the range between 20ns and (20ns + t_{WL} (CK) = 120ns.

Fig. 5-4 presents an example of areas of transition among the rising edges of the aforementioned signals with respect to CK.

Given certain special conditions which are very difficult to deal with, problems could occur if the recommended synchronization for a multi-chip switching matrix is not respected. The connection of the relevant M3488 will be carried out before the disconnection of the output channels of all the remaining M3488s of the matrix.

This could cause an error in the correlation of the first bit in the first byte of the signal transferred.

Figure 5.4 : The Shaded Area Shows the Recommended Variation in the Rising Edge of the READ and WRITE Signals in the Case of Multi-chip Matrices.



Anyhow, this only concerns the first byte transferred ; there will be no problem with those following. Another interesting parameter concerning the $\overline{RD}$ and $\overline{WR}$ signals is the minimum timing interval to maintain between two consecutive cycles, in other words, between the two rising edges.

The timing, t_{REP}, is a CK period function, namely :

$$t_{REP} = 40 \text{ ns} + 2\, t_{CK} + t_{WL}\,(CK) + t_R\,(CK).$$

When $t_{CK} = 244$ns, $t_{REP} = 653$ns.

The reading operations of the OR1 and OR2 registers during instruction 6 are the only exceptions.

In this case, a request is indeed made for the minimum time between $\overline{RD}$ rising edges to be 3 CK periods for sequences from OR1 to OR2, and 13, for sequences from OR2 to OR1.

INSTRUCTION EXECUTION TIMING

Within a time slot (3.92µs for PCM input flows of 2048 Kbit/s), there are 16 CK periods. Each period corresponds to a machine cycle.

Of the 16 cycles contained in a time slot, 8 are free and are used to carry out instructions received from the microprocessor. Fig. 5-5 shows the internal distribution in a time slot with these cycles.

Physical time for internal execution of an instruction amounts to 5 cycles, excluding loading time for data bytes and commands coming from the microprocessor.

This time can be increased by 8 cycles if the instruction execution is not complete before the beginning of the block of 8 cycles reserved for internal operations.

Moreover, if instruction 6 is activated, all other instructions will be processed after instruction 6 has been completed or, at the latest, at the beginning of the new frame.

By activating instruction 1 (Connection/Disconnection) between a given input channel C_{IN} and an output channel C_{OUT}, the byte transferred to C_{OUT} corresponds to the byte taken from C_{IN} in the same or the preceding frame, based on the relative position of C_{OUT} with respect to C_{IN}.

In particular, if the number of C_{OUT} channels (NC_{OUT}) is greater than or equal to two units as compared with the number of C_{IN} channels (NC_{IN}), the connection occurs in the same frame.

6. APPLICATIONS

EXCHANGE NETWORK

The M3488 device was designed to be used as a basic element in large-scale switching systems, with up to 65536 connections.

An example of a structure which could be used for this purpose is shown in fig. 6-1, which shows that a system of 64 K users (2048 PCM links, each having 32 channels) is made up of eight central modules, each with a capacity equal to 8 K connections (256 PCM links, each having 32 channels) and of (256 + 256) M3488 peripherals.

Fig. 6-2 shows the internal organization of a central module with 8 K connections.

It should be noted that it is made up of eight switching units, each with a capacity equal to 1 K connections (32 PCM links, each having 32 channels) and of (32 + 32) M3488 peripherals.

Figure 5.5 : The Division within Each Time Slot Between the Time Reserved for Internal Processing and That Reserved for the Execution of Commands Supplied by the Microprocessor.

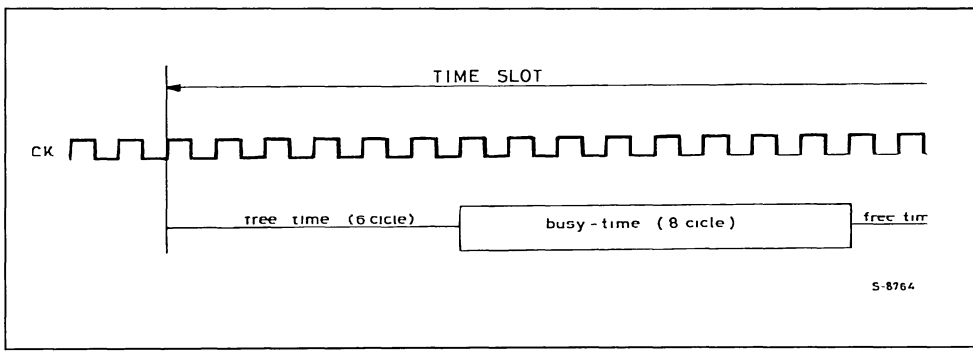


Figure 6.1 : Simplified Block Diagram of a Switching Matrix with 65536 Channels Concentrated in 2048 PCM Links at 2048 Kbit/s Each.

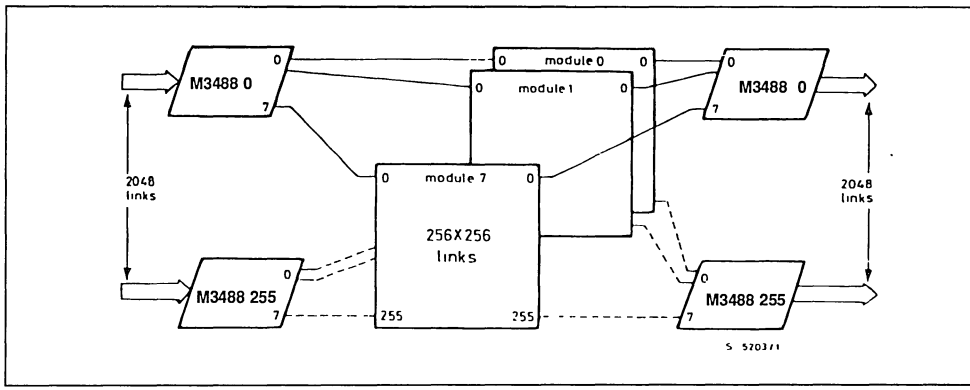
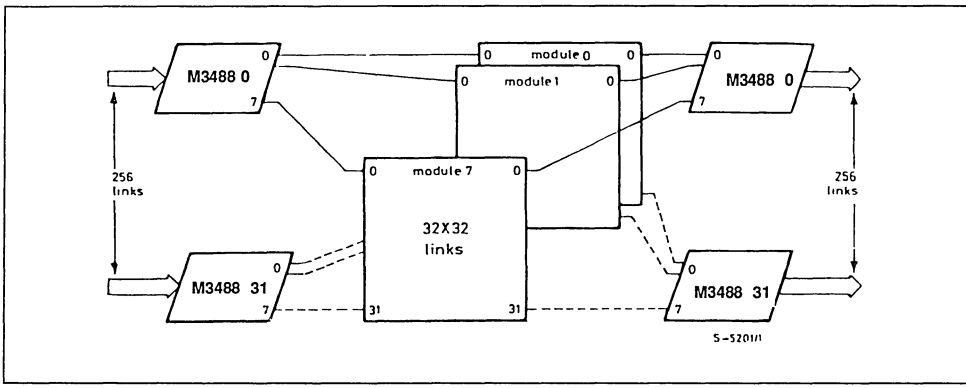


Figure 6.2 : Simplified Block Diagram of a Switching Module Four 8192 Channels Concentrated Into 256 PCM Links at 2048 Kbits/s.



The internal structure of a switching unit with 1K connections is shown in fig. 6.3.

It is made up of 16 M3488s organized in a square matrix (multi–chip matrix).

It is important to stop, finally, with this last structure, insofar as it could, without any variation, be used as a PABX switching matrix, up to 1000 lines.

The 1000 lines, or, more precisely, 1024, are concentrated in 32 PCM flows at 2048 Kbit/s.

All 16 M3488s have microprocessor interface signals in common (D7 to D0, RD, WR, C/D, RESET), as well as CK, SYNC and selection pins A1, A2 and CS2.

Also, all 4 M3488s belonging to the same column have the same output channels in common and all 4 M3488s belonging to the same row have the same input channels. When the microprocessor needs to execute an operation on a certain output channel COUT, the relevant M3488 column is chosen from among the chip select signals CS10, CS11, CS12 and CS13.

Thus, the microprocessor transmits the relevant bytes which, obviously, are received by all the M3488s of the matrix.

However, only one of these M3488s should execute the instruction.

The single M3488 which should execute the function request is the one in which pins S1 and S2 have been connected to V_{CC} and V_{SS} in such a way as to correspond to the signals present, respectively, on the common wires A1 and A2.

Figure 6.3 : Switching Matrix for 1024 Channels Concentrated Into 32 Links at 2048 Kbits/s.

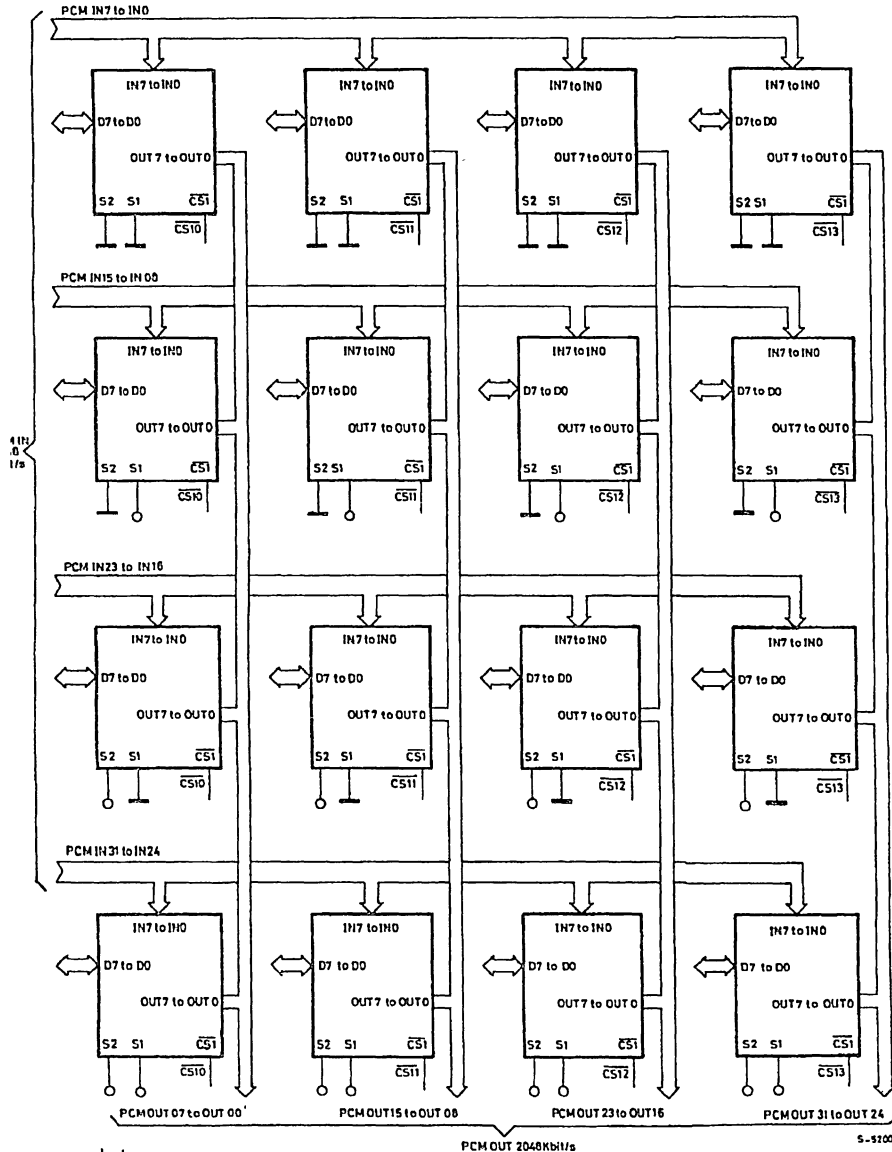


Figure 6.4 : Switching Matrix for 512 Channels Concentrated Into 16 PCM Links at 2048 Kbits/s.

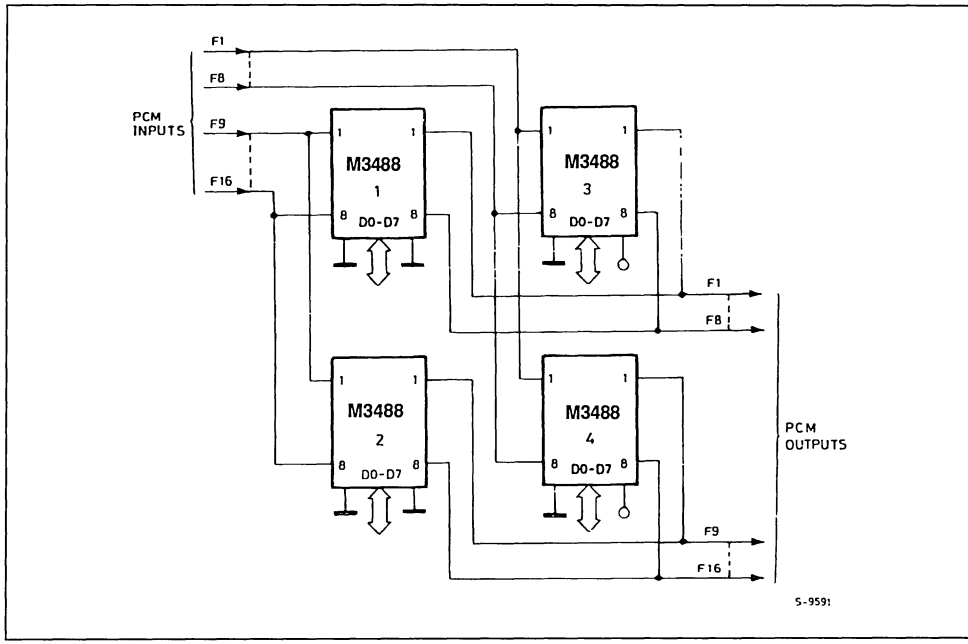
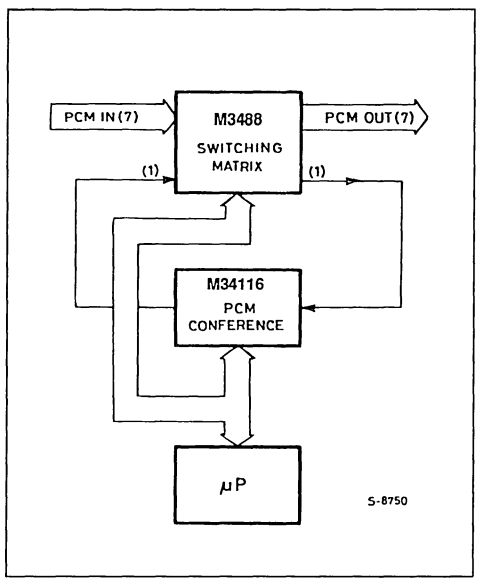


Figure 6.5 : Typical M3488-M34116-µP Configuration. One Output Stream of the M3488 are Connected to the M34116 and Dedicated to the Conference Function.



The other M3488s in the column selected recognize that, even though having to do with an operation of a channel under their control, this operation must be carried out by another M3488 in their column and they act on this basis.

In the case of instructions 1 and 3, they carry out a disconnection from the relevant output channel C_{OUT}, instruction 5 is unaffected and instructions 2, 4 and 6 are not executed.

*Bus reading only takes place on M3488 in match condition (A1 = S1, A2 = S2).

This fact greatly simplifies the controlling software of the matrix insofar as, when a new connectionneeds to be executed or a byte loaded on a certain C_{OUT}, it is possible to ignore the same C_{OUT} disconnection from earlier connections because the disconnection is carried out automatically by the multichip matrix.

PABX

What was explained in the previous paragraph applies to switching systems up to 1024 lines.

The switching matrix for systems up to 512 users is represented in fig. 6-4.

Also, in this case, it is important to demonstrate the great simplification in the control software determined by the use of S1, S2, A1 and A2 for the choice

of M3488 involved in operations.

A single M3488 will suffice for switching system up to 256 channels.

In the sphere of the PABX, regardless of its size, a function currently always in demand is the conference function, that is, the possibility to interconnect several users.

SGS-THOMSON has developped a device for this purpose, called CONFERENCE CALL (M34116), which is used in conjunction with the M3488 to carry out this function.

In addition M34116 is able to generate up to 7 tones +1 Melody simultaneously fully programmable in amplitude, duration and frequencies saving all the circuitry normally dedicated to tone generation inside a PABX.

Fig. 6-5 demonstrates this application.

The M34116 is also controlled by an 8-bit microprocessor, and, therefore, has been given a parallel interface for the microprocessor, using characteristics exactly the same as those available in the M3488.

In order to carry out a conference operation, it is essential to reserve a PCM output and input in the matrix, for which, when using a single M3488, switching capacity decreases to (224 x 224) users. With a single M34116, it is possible to carry out from 1 to 29 conferences simultaneously, with the only limitation being that the total number of users involved in the conferences must be less than 32 ; fig. 6-6 illustrates this aspect.

With reference to fig. 6-7, in which the case of three users in conference is examinated, we can see which phases are required to bring about a conference :

1) the channels to use for the conference (A, B and C, in the example) are allocated in any channel position of the reserved PCM bus. The operation is carried out by the M3488.
2) the supplementary channels are added together, in other words, the contents of channel B arereplaced by the sum of channels (A and C) etc. This is carried out by the M34116. These sum signals are loaded in the reserved PCM output bus.
3) the sum signal are withdrawn from the reserved PCM bus and switched into the relevant output channels. This operation is carried out by the M3488.

It is also possible to use the M34116 in a multi-chip switching matrix - see fig. 6-8 - or use more than one M34116 in the same matrix - see fig. 6-9.

Figure 6.6 : With a Single M34116 It is Possible to Realize from 1 to 29 Independent Conferences with a Total of up to 32 Channels Conferenced.

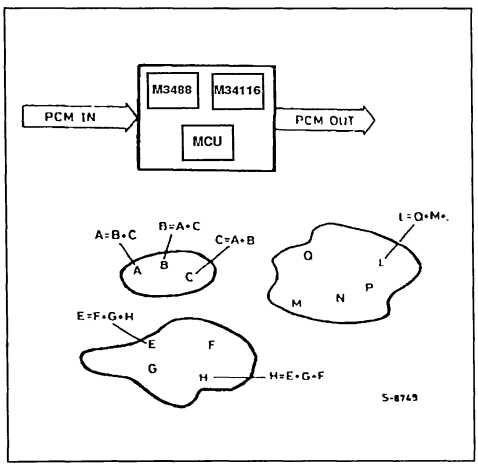


Figure 6.7 : Example of a conference with three channels ; A, B and C.

1) The M3488 allocated A, B and C to the PCM stream applied to the M34116.
2) The M34116 processes the channels A, B and C, returning to the outputs B+C, A+C and A+B respectively.
3) The M3488 allocates the signals B+C, A+C and A+B, to the outputs corresponding to the time slots of the channels A, B & C.

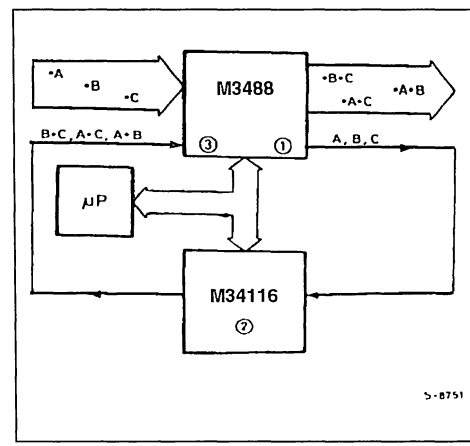


Figure 6.8 : The M34116 Can Also Been Used in Multichip Matrices.

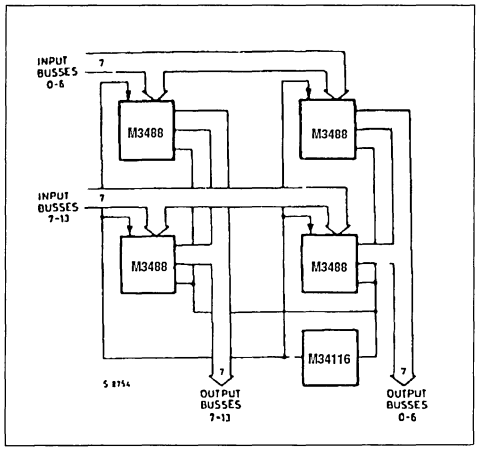
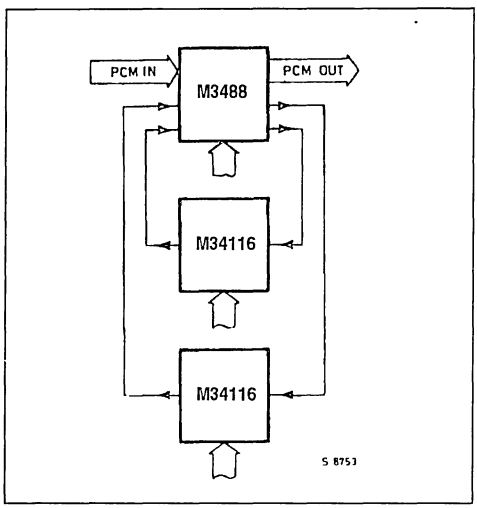


Figure 6.9 : More Than One M34116 May be Added to Each Matrix to Increase the Number fo Conferences (10 per device).



For more detailed information see the M34116 datasheet.

Finally, it is interesting to note how the M34116, on its own, can be used with other types of switching matrixes ; however, two considerations lead to recommending its use with the M3488 ;

a) M34116 PCM signal timing and microprocessor interface are exactly the same as those of the M3488 ;

b) the command format that the microprocessor sends to the M34116 to program the different operations is the same as the one used to program the M3488.

To sum up, by using the M34116 with the M3488, complete compatibility is obtained, both with hardware and software, between switching matrices and the M34116.

M3488 WITH LESS PCM LINKS THAN 32 CHANNELS

It is also possible to use M3488 when the PCM frames are made up of a number of channels other than 32.

Suppose that the PCM frames are made up of N-Channels, which will be numbered from 0 to (N-1).

Each PCM frame will thus be made up of a number of bits multiplied by 8 ; this exactly equal to (N · 8).

Also, in this case, it is necessary to respect the timing relationship between the different signals shown on the data sheet ; in particular, a relationship is always carefully made between the rising edge of SYNC and the first clock (CK) bit contained in the slot time for bit 0 of channel 0.

In order to use M3488 with these frames, it is sufficient, using the data bytes sent by the microprocessor, to modify the numbering of a few channels.

In particular :

a) in all instructions in which reference is made to the input channel (N-1), the number 31 should be substituted for the number (N-1) ;

b) in all instructions in which reference is made to the output channel 0, the number N should be substituted for the number 0.

These variations can be made insofar as the M3488 is internally programmed to execute the different operations using 32 channels.

In particular, during the time slot which corresponds to the last channel of the frame, channel (N-1), the M3488 loads the bits corresponding to the next channel to be output in the next slot time into its registers.

We consider this last channel to be channel 0, but for the M3488 it is Channel N ; indeed, the M3488 draws the bits that it will successively output from the corresponding cells of Channel-N.

Likewise, during the general time slot X, M3488 loads the PCM input frame bits corresponding to channel X ; simultaneously, it memorizes the bits loaded in the previous time slot into the Speech Memory (SM) memory location corresponding to channel (X-1).

Therefore, during the time slot corresponding to channel 0, M3488 memorizes the bits received in the previous time slot, which we consider to be channel (N-1), in the SM memory locations corresponding to channel 31.

For whoever wishes to connect the input channel (N-1) to any output channel, the same channel's PCM samples will be drawn from locations reserved for channel 31.

M3488 WITH THE NORTH AMERICAN PCM STANDARD

The operation of the M3488 with PCM frames using the North American standard can be considered a special case of the operating mode described in the previous paragraph.

The only variable in this case is the presence in each frame of an auxiliary bit (bit X), for which the total number of bits in a frame is :

(24 channels . 8 bits) + 1 bit = 193 bits/frame

As in the preceding case, in alteration in the numbering of the canals is introduced, in particular, the number 23 is replaced by the number 31 in every case in which reference is made to the last channel of the PCM input frame, and in every case where reference is made to output channel 0, the number 0 is replaced by the number 24.

Also, the signals for synchronization ($\overline{SYNC}$) and for clock (CK) are modified as shown in fig. 6-10.

In particular, the rising edge of the $\overline{SYNC}$ signal must appear in bit X's bit time (the 193rd of the PCM input frame). The single variation in the timing of this signal as far as the MCK and CK signals is concerned in that the minimum time for t_{WH} $\overline{SYNC}$ high level width must be from 1 t_{CK} to 3 t_{CK} and thus with (3 . 324) ns = 972ns.

The clock (CK) signal to be applied to the M3488 (pin 6) must be frozen for two clock periods during bit X's bit time. A scheme which is recommended for obtain CK beginning from the MCK and $\overline{SYNC}$ signals is shown in fig. 6-11.

The signal bits located in the PCM input frames are ignored, while, in the corresponding positions of the PCM output frames, they assume the same logical values of the 0 bits of channel 0.

If you use the M3488 with an M34116 the scheme recommended of fig. 6.11 is not necessary. In fact the "frozen clock" is provide by M34116 itself (pin EC).

Therefore is enough to connect pin EC of M34116 to pin CK of M3488. Of course the $\overline{SYNC}$ signal must be the same as shown in Fig. 6.10 and must be connect both to M3488 and M34116.

DATA FLOW SWITCHING

A very simple, but very important, application of the M3488 is that of using it to switch PCM or other high speed data links.

To enable this function, it suffices to switch all relevant input channels to their preselected output channels.

The data rate of these data flows can have any value less that the maximum permissible velocity (2048 Kbit/s).

Obviously, the CK frequency must be the double of the data rate chosen, while the $\overline{SYNC}$ frequency must be included between 1/16 and 1/256 of the same data rate.

Figure 6.10 : Timing of the CLOCK, $\overline{SYNC}$ and PCM IN Signals for 1544 Kbit/s PCM Streams. At the 193 rd Bit (bit X) the CLOCK Signal applied to the M3488 is frozen for two Periods.

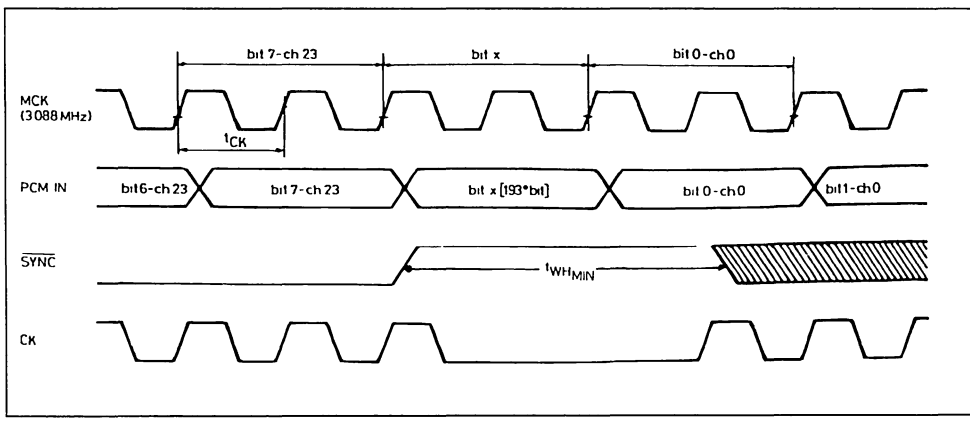
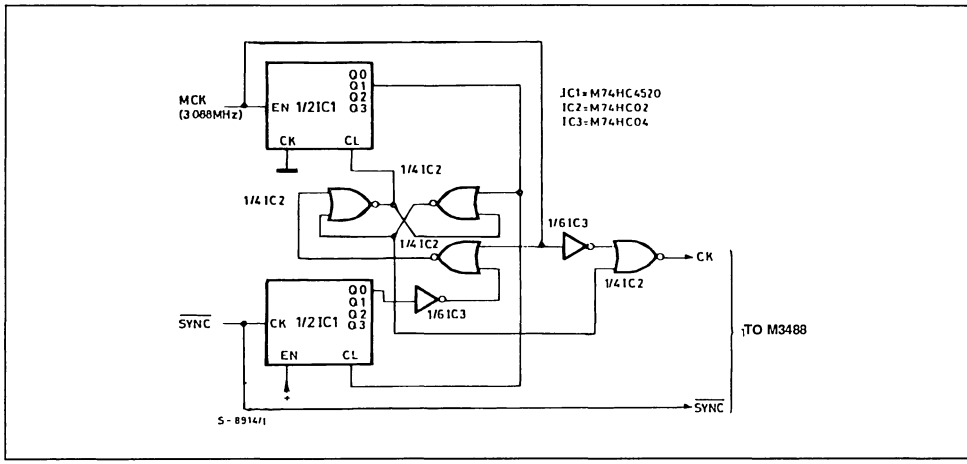


Figure 6.11 : Auxiliary Circuit to use the M3488 with 1544 Kbits/s PCM Streams. This Circuit is not necessary if the M3488 is used with an M34116.



It is particularly interesting, in this application, to demonstrate a characteristic of the M3488 which has already been mentioned and, therefore, of the fact that the device accepts that a certain delay can exist between one data flow and another.

The absolute value of the maximum acceptable delay is not constant, but depends on the velocity of the data flow ; in any case, it is always greater than 80 % of bit time.

This obviously means that when the data flows are not generated internally, but come from peripheral devices located at different distances - See fig. 6-12- within certain limits, it is not necessary to equalize the delays caused by variable arrival times.

RS232 C/V-24 DATA INTERFACE SWITCHING

One of the alternative fields for possible use of the M3488 is that of DATA COMMUNICATIONS.

Fig. 6-13 presents the block diagram of one of the possible applications : a device which allows for switching between the V-24 interface of four DTEs and the V-24 of four DCEs.

As is well known, the RS232 C/V-24 is one of the most common connection interfaces between Data Terminal Equipment (DTE), i.e., computers and terminals, and Data Communication Equipment (DCE), i.e., modems, etc.

Figure 6.12 : Structure of a PABX with Peripheral Concentration Blocks. Note That the CE-PP Connections are PCM Links.

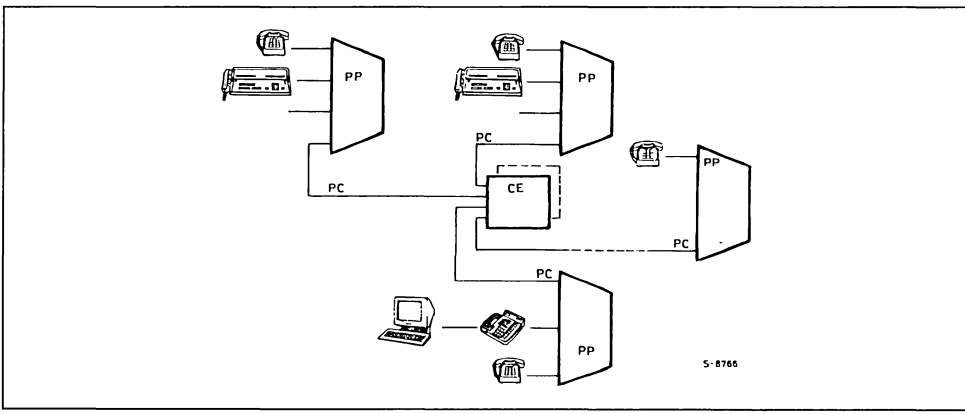
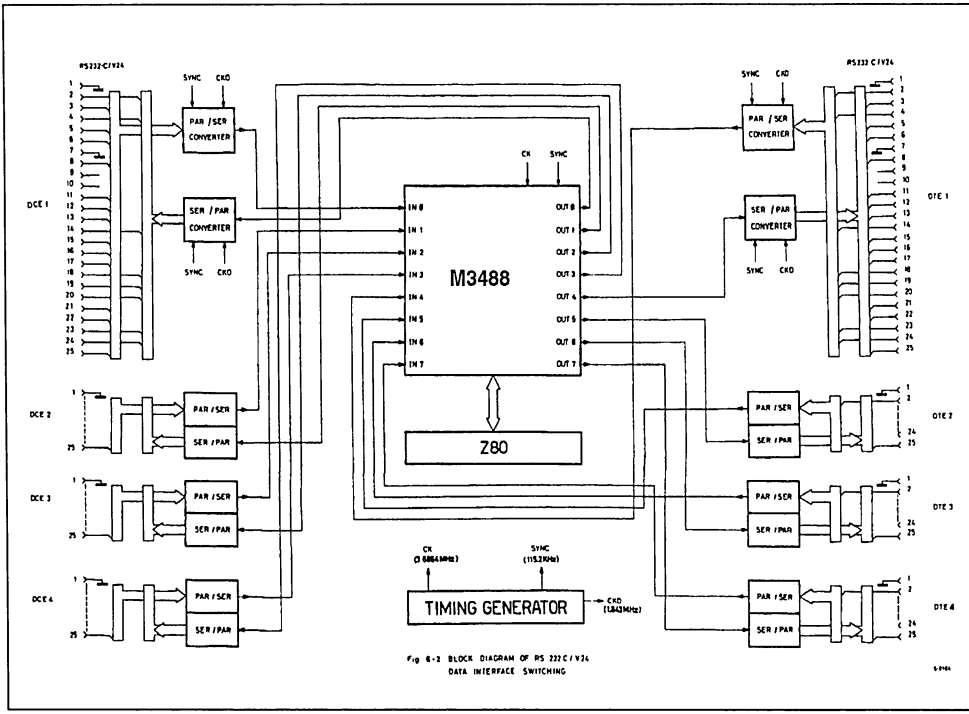


Figure 6.13 : Switching Matrix for Parallel Data Interfaces (eg : RS232C/V24). Signals from the Parallel Interfaces are Serialized, Switched and Parallelized.



The table in fig. 6-14 presents the names of 25 distinct pins which determine the interface and the direction of the same signals (13 DCE → DTE and 8 DTE → DCE).

The basic idea of the device is to sample, using a frequency of 115.2 KHz, the 21 usable interface signals, serialized at a velocity of 1843.2 Kbit/s, and send or receive them through the switching matrix exactly as if they were PCM streams.

In the case of interfaces coming from DCE, of the 21 usable signals, 13 are signals inputting the device, and 8 outputting it, thus it is necessary to run a parallel/serial conversion on the first, and obviously, serial/parallel on the second.

For reasons of simplicity in the serialization phase for the 13 bits, three bits are added so that every sampling period (8.7 µs) will amount to exactly two octets ; in the parallel/serial conversion phase, the three additional bits are disregarded.

Concerning the DTE, the discussion is similar, with the obvious exception of the fact that the signals undergoing serial/parallel conversion are 13 and those which undergoing parallel/serial conversion are 8.

To these last 8 bits should be added, for the same reasons mentioned before, 8 bits so that, during each sampling period, exactly 16 bits are serialized.

An input and an output made available by the M3488 are reserved for each interface.

The M3488 views the data streams which are entering exactly if they were PCM frames at 1843 Kbit/s.

In this case, the difference is that the number of channels used is only two, thus each two octets require that the M3488 internal channel counter be reset to zero.

This is obtained simply by raising the frequency of the SYNC signal from the usual 8 KHz to 115.2 Khz, in other words, to use as SYNC the same signal used to sample the interfaces (see fig. 6-13).

Wanting, for example, to switch the V-24 from DCE1 to that of DTE4 is sufficient through the microprocessor sending to the M3488 instructions for connecting channels 0 and 1 of input 0 with channels 0 and 1 of output 7, channels 0 and 1 of input 7 with 0 and 1 of output 0.

Figure 6.14 : RS-232-C/V. 24 Data Interface Connector Pin Assignements.

Pin	Circuit EIA	Circuit CCITT	SIGNAL NAME	Direction DTE ——— DCE
1	AA	101	Protective Ground	→
2	BA	103	Transmitted Data	→
3	BB	104	Received Data	←
4	CA	105	Request to Send	→
5	CB	106	Clear to Send	←
6	CC	107	Data Set Ready	←
7	AB	102	Signal Ground (Common Return)	↔
8	CF	109	Received Line Signal Detector	←
9			Unassigned	
10			Unassigned	
11		126	Select Tx Frequency	←
12	SCF	122	Secondary Received Line Signal Detector	←
13	SCB	121	Secondary Clear to Send	←
14	SBA	118	Secondary Transmitted Data	→
15	DB	114	Transmit Signal Element Timing (DCE Source)	←
16	SBB	119	Secondary Received Data	←
17	DD	115	Receiver Signal Element Timing (DCE Source)	←
18		141	Local Loopback	→
19	SCA	120	Secondary Request to Send	→
20	CD	108/2	Data Terminal Ready	→
21	CG	110	Signal Quality Detector	←
22	CE	125	Ring Indicator	←
23	CH	111	Data Signal Rate Selector (DTE Source)	→
24	DA	113	Transmit Signal Element Timing (DTE Source)	→
25		142	Test Indicator	←

Obviously, it is possible to carry out simultaneously all four connections in any combination.

Using M3488 instead of standard analog cross-point besides switching, you can also implement addition functions as monitoring or programming by µP the status of the interfaces using the instruction 3 and 4 of the M3488 itself.

Using more M3488s extends at will the number of interfaces thus switchable due to their subdivision between DTE and DCE V-24s.

Finally, there are no limits to the use of this system for switching other interface types.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

PROTECTION CONCEPTS IN TELECOMMUNICATIONS EQUIPMENT

A. Bremond

I INTRODUCTION

The goal of a telecommunication network (fig.1) is to permit data exchange (speech or digital) between two or more subscribers.

The network is made up of different parts which are subject to various disturbances.

The most susceptible elements are the lines, due to their length and their geographical location.

Disturbances strike the lines and are then propagated to the extremities of the lines at which lie telephone sets and the subscriber line interface cards (SLIC).

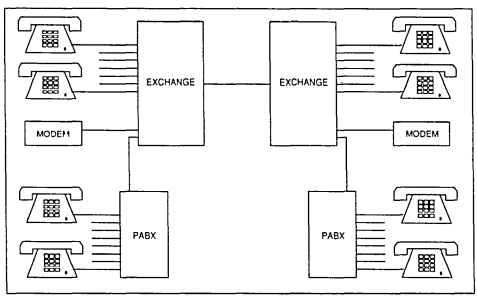
So the lines receive two kinds of overvoltages :

Surges of short duration with high peak voltage value (a few hundred micro-seconds for a few thousand volts). These are generated by atmospheric phenomena.

Surges of long duration with medium voltage value (greater than one second for a few hundred volts RMS) which are due to the mains AC power networks.

The purpose of this application note is to analyse these 2 kinds of overvoltages .

Figure 1 : Classical telecommunication network topology



II OVERVOLTAGES ACROSS TELECOMMUNICATION LINES :

II.1 Atmospheric effects :

Lightning phenomena are the most common surge causes. They are mainly due to a voltage difference between the ground and the clouds (a few 100 kV). Two kinds of strikes may occur:

1) Negative discharge with a peak current of 50 kA, rise time of 10µs to 15µs and 100µs duration.

2) Positive discharge with a peak value of 150 kA, rise time between 20µs and 50µs and a duration between 100ms and 200ms.

The lightning effect appears on the lines in two ways.

– Direct shock.
– Induced shock.

Figure 2 : Lightning phenomenon

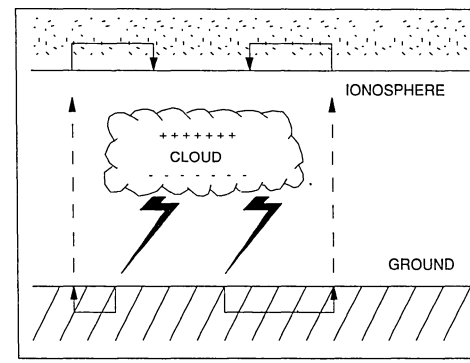


Figure 3 : Direct lightning strike

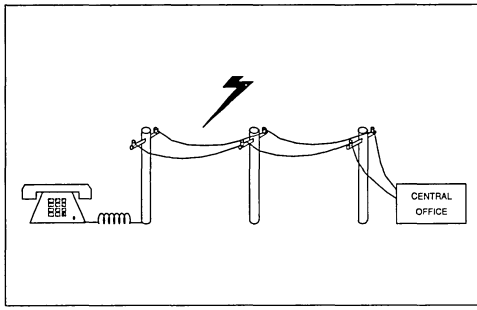
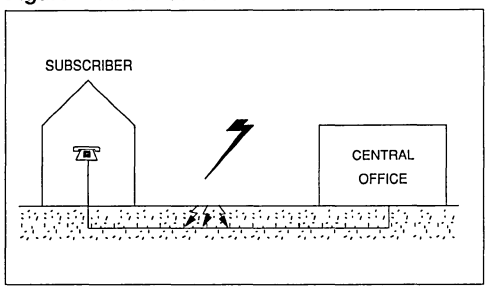


Fig.3 shows the first case which is produced mainly on overhead lines.

Induced shock is more frequent than a direct shock. Lightning strikes the ground and a current flows in the cable shield. This current produces a voltage gradient which in some places is above the insulation capability of the cable material (Fig.4).

Figure 4 : Induced strike



II.2 Proximity and crossing with AC mains lines :

For these kinds of surges two cases may be seen :

The first one is due to the falling of an AC mains cable on a telephone line.

The second case is produced by the proximity of a subcriber line with an AC mains line or equipment (mainly capacitive coupling).

It is interesting to note for these types of disturbances a RMS value of a few Amps for a duration of between 1 s and 15 mn.

III PRIMARY AND SECONDARY PROTECTION :

The figures in chapter II give us an idea of the energy which may appear on the lines. In the field these surge values are lower due to the losses of ground resistance, the capacitive coupling and so on, but are signifiant nevertheless.

We have to divide these disturbances into two families :

High peak value and short duration (lightning)

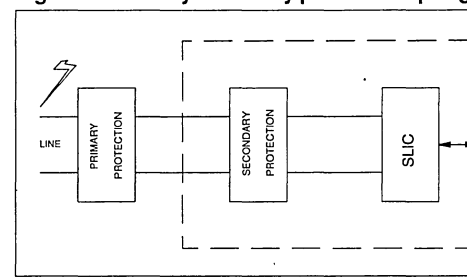
Short peak value and long duration (crossing with AC power).

For both cases the present state of the art of silicon protection devices does not permit the suppression of these levels of energy.

A second parameter to keep in mind is the very low clamping factor (1) needed by the IC's used to realize the line interface. This forces the designer to use a protection solution with silicon (fast response time/low clamping factor).

High energy values and low clamping factor impose two protection levels.

Figure 5 : Primary/secondary protection topology



The first level called primary protection (fig.5) located on the connecting terminal of the exchange, suppresses the major part of the disturbance. The second level called secondary protection reduces the remaining overvoltage.

(1) the clamping factor is the ratio of the normal operating voltage over the maximum clamping voltage.

Figure 6 : Primary/secondary protection level effects

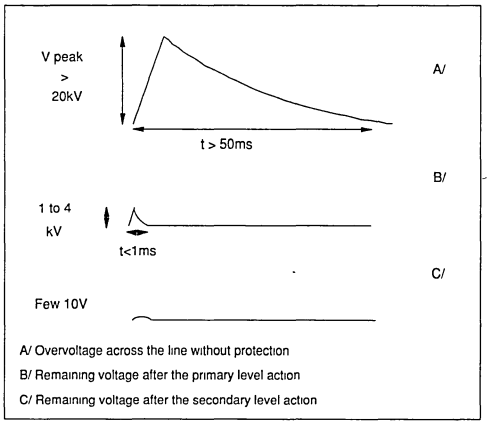


Figure 6 shows the goal of both protection levels.

In this example the surge across the line without protection will be several 10 kV peak value for several 10 ms duration (Fig.6A)

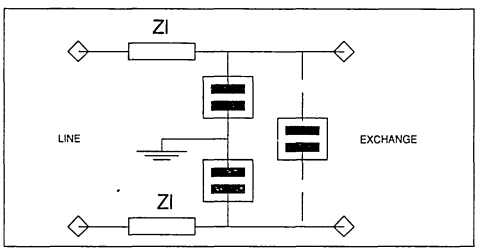
After the primary protection the major part of the energy is cancelled (Fig.6.B). The remaining overvoltage may be a few kV (depending on the dv/dt of the surge and the surge arrestor technology used).

Across the second level protection the voltage does not exceed a few 10 Volts.

III.1 Primary protection :

Actually two kinds of primary protection are used :
– carbon gaps.
– gas tubes.

Figure 7 : Carbon gap based primary protection

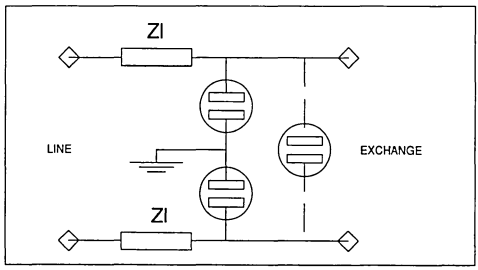


III.1.A Carbon gaps :

These components are made by two carbon electrodes. The carbon gap is a low cost primary protection but it has two major disadvantages :
– its short life duration
– its variable spark threshold.

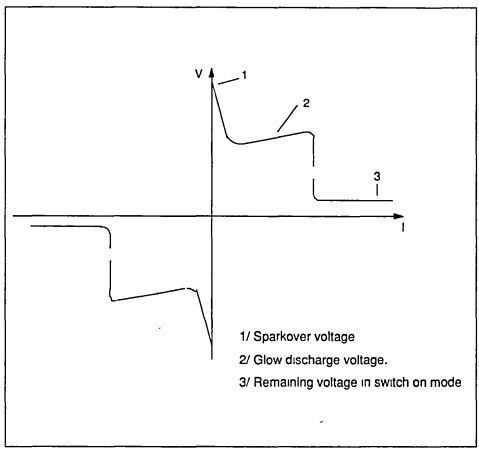
III.1.B Gas tubes :

Figure 8 : Gas tube based primary protection



These components are made by two metallic electrodes in a sealed case. Generally the sealed tub contains a low pressure gas.

Figure 9 : Gas tube characteristics

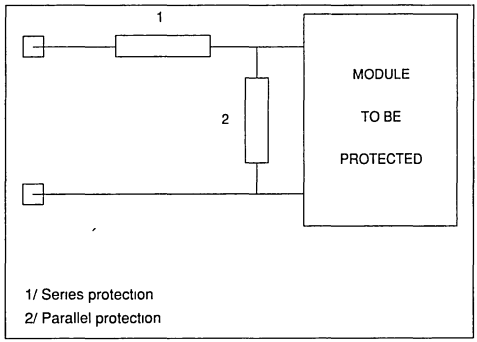


The major disadvantage of this kind of device is its response time, in fact the maximum voltage across the gas tube depends on the dv/dt of the surge.

III.2 Secondary protection :

III.2.A Series and parallel protection :

Figure 10 : Series and parallel protection



The secondary protection level is generally achieved with two types of devices :

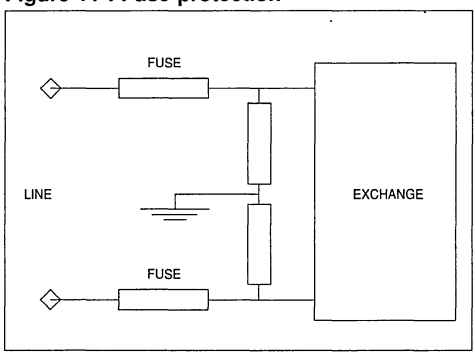
The series protection ensures protection against the proximity of or the crossing with AC power lines.

The parallel protection operates to suppress the overvoltages due to the lightning effects.

* Series devices :

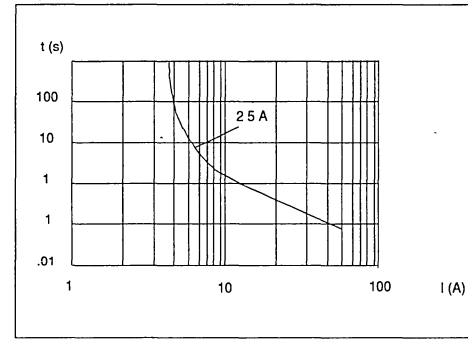
Series devices operate by opening the circuit or by an increment of the resistance.

Figure 11 : Fuse protection



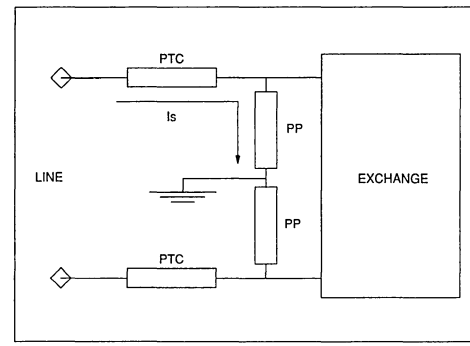
The fuse is a classical case of protection by opening the circuit. Figure 11 shows an exchange protected by fuses and figure 12 represents an example of the limit curve of the fusing action.

Figure 12 : Fuse blowing function



These components provide an absolute security after action, but their major disadvantage is the need for maintenance.

Figure 13 : PTC based protection

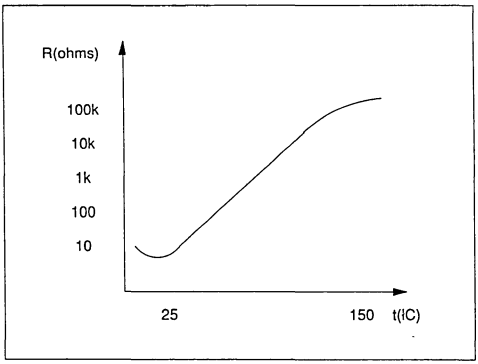


The PTC thermistor is a device which operates by very rapid resistance increase as a function of the temperature.

When the surge occurs across the line, the parallel protection PP is activated.

The surge current Is, generated by PP action, flows through the PTC device and increases its internal temperature. As shown in figure 14 the resistance value of the PTC device rises quickly with the temperature.

Figure 14 : Resistance versus temperature



The major disadvantage of the fuse does not exist with the PTC device. Unfortunately this kind of component has a large tolerance, a long time to return to its stand off point and a drift of its value.

Another series device is the resistance which limits the current through the parallel protector.

* Parallel devices :

The parallel protection function may be assumed by different devices based on different technologies.

In fact it is clear that the future in term of SLIC topology is based on the use of ICs. So the consequent requirement for good response times and high clamping factor necessitates the use of silicon protection.

Parallel silicon protection functions in two different modes.

- The clamping mode with the TRANSIL.
- The crowbar mode with the TRISIL.

IV CONCLUSION

Due to atmospheric effects and disturbances on mains networks, telecommunication lines have to be protected. Due to the improvement in telecommunication system technology, a need for fast and precise protection solutions results.

The choice of the protection diagram will be done considering local standards and the technology of the devices to be protected.

This protection will be assumed to be dual level

- Primary level to suppress high energy.
- Secondary level to optimize the remaining overvoltage.

VOLTAGE TO CURRENT WAVEFORM CONVERSION (Example Of The 10/700 µs Surge)

A. Bremond

INTRODUCTION

CCITT members have generated a great deal of recommendations which have permitted national administrations to publish local standards. In particular they have defined a 10/700 µs surge waveform and its associated generator diagram (see fig.1).

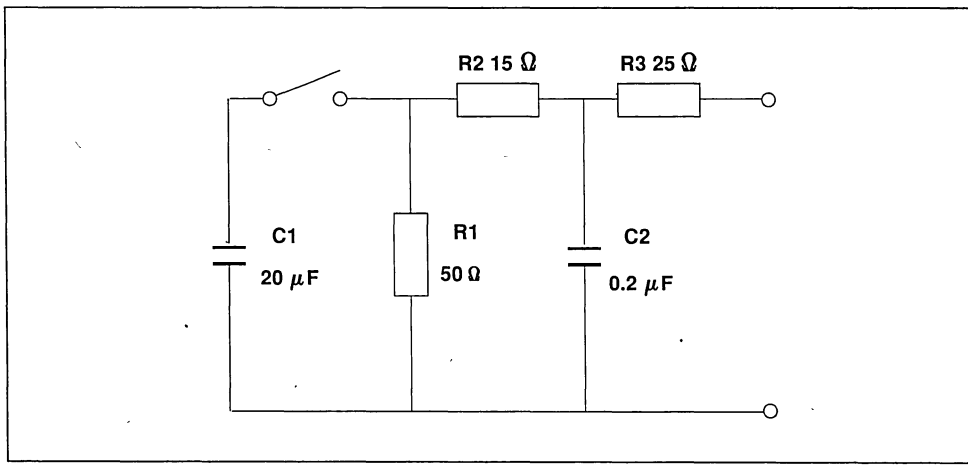
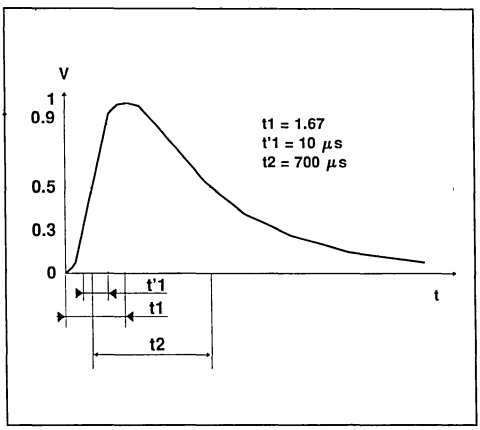


Figure 1 : CCITT 10/700 µs Surge Definition



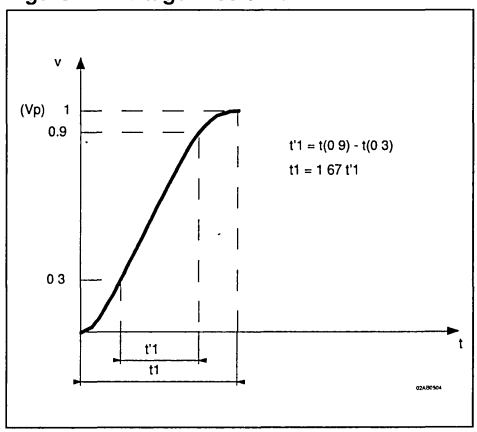
GENERATOR DIAGRAM OPEN OUTPUT SURGE WAVEFORM

It is important to note that the given waveform is the generator output voltage without load. For a protection component user the most important parameter to take into account is the current waveform flowing through the surge suppressor. The goal of this paper is to give the current waveform parameters.

2 - WAVEFORM CALCULATION

2.1 : Generator output voltage without load.

Figure 2 : Voltage Rise time



2.1.1 : Rise time

The equation of this curve is :

$$v(t) = Vp\ (1 - \exp(-t/T))$$

$$\Rightarrow t = -\ T \log_n (1 - (v(t)/Vp)) \qquad (1)$$

In this case the time constant may be estimated as :

$$T = R_2\ C_2$$

So t(0.3) and t(0.9) will be calculated respectively with v(t)/Vp = 0.3 and 0.9

$$t(0.3) = 1\ \mu s$$

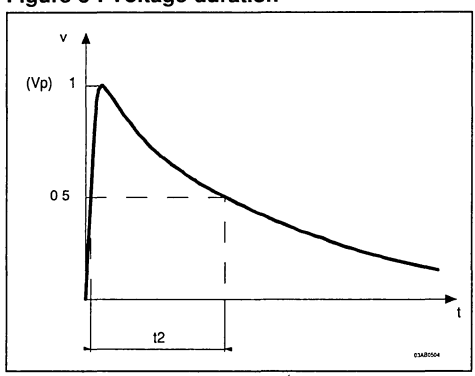
$$t(0.9) = 6.9\ \mu s$$

and then

$$t1 = 1.67\ (t_{(0.9)} - t_{(0.1)})$$

$$= 9.8\ \mu s \approx \underline{\underline{10\ \mu s}}$$

Figure 3 : Voltage duration



2.1.2 : Voltage surge duration

The equation of this curve is:

$$v(t) = Vp \exp(-t/T))$$

$$\Rightarrow t = -\ \log_n (v(t)/Vp)) \qquad (2)$$

with a time constant due essentially to R_1 and C_1

$$T = R_1\ C_1$$

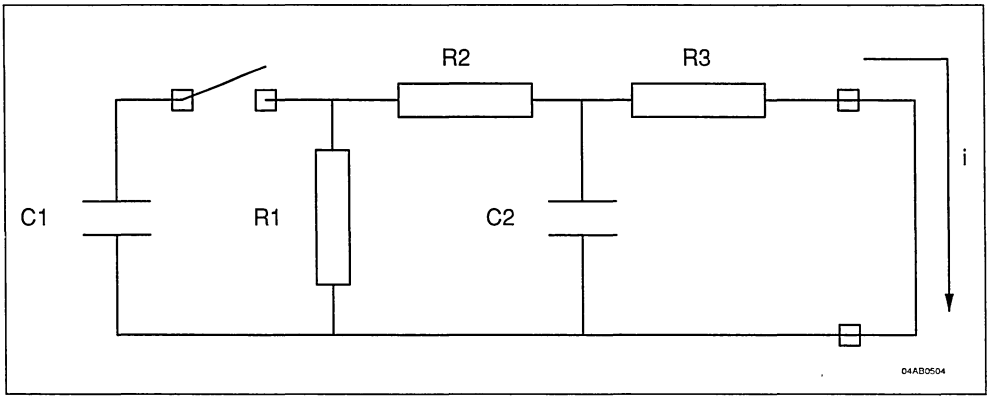
So t_2 may be calculated with v(t)/Vp = 0.5

$$\Rightarrow t2 = 693\ \mu s \approx \underline{\underline{700\ \mu s}}$$

2.2 Generator short circuted output current.

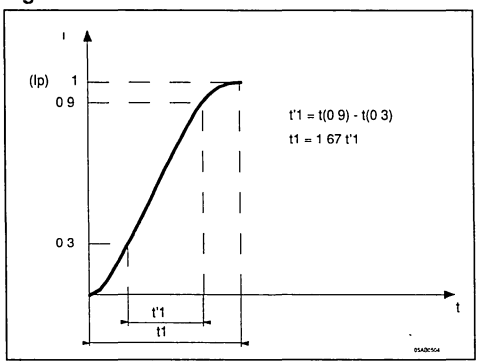
In this chapter we will do the calculations with the generator output in short circuit (see fig.4), this is generally the case during the surge suppressor action (for example the Trisil technogy devices from SGS THOMSON).

Figure 4 : CCITT 10/700 ms generator with output in short circuit



2.2.1 : Rise time

Figure 5 : Current rise time



The formula (1) given in the chapter 2.1.1. remains true, but the time constant must take into account R_3 and may be estimated as :

$$T = (R_2 R_3/(R_2 + R_3))\ C_2$$

So $t_{(0\,3)} = 0.67\ \mu s$

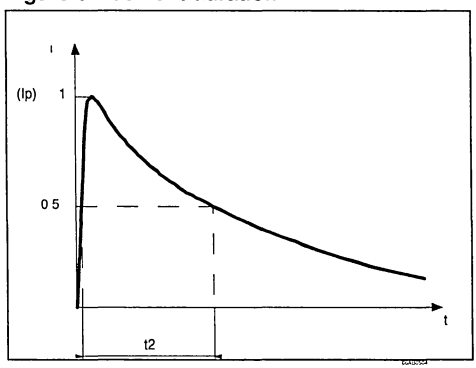
$t_{(0.9)} = 4.3\ \mu s$

$$\Rightarrow t1 = 1.67\ (t(0.9) - t(0.1))$$

$$= 6\ \mu s \approx \underline{\underline{5\ \mu s}}$$

2.1.2 : Current surge duration.

Figure 6 : Current duration



The formula (2) given in the chapter 2.1.2. remains true but the time constant is now due to the capacitor C_1 with the resistor R_1 in parallel with $R_2 + R_3$

$$T = (R_1\ (R_2 + R_3)/(R_1 + R_2 + R_3)\ C_1$$

$$\Rightarrow t2 = 308\ \mu s \approx \underline{\underline{310\ \mu s}}$$

3 - SUMMARY

The 10/700 µs surge waveform given by the CCITT recommendation is a voltage wave produced by the generator in open circuit. This curve is very important as a test reference for telecommunication equipment.

The protection function designers or users have to know the actual current waveform flowing through the protector in order to optimize it.

The 10/700 µs CCITT generator gives a 5/310 µs current wave when its outputs are in short circuit. (In the case of a crowbar device, for example Trisil).

For certain cases the resistor R3 is equal to zero and then the duration time becomes 160 µs.

Please note that in certain documents we find a 8/320 µs current wave which represents the same surge test.

PROTECTION STANDARDS APPLICABLE TO TERMINALS

C. Politano

1. INTRODUCTION

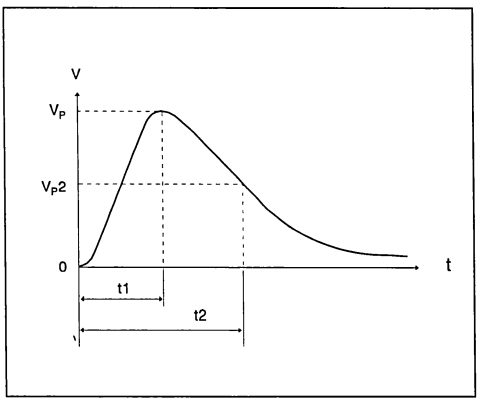
The purpose of this document is to summarize the main telecommunication standards with regard to the protection requirements against two types of overvoltage :

- lightning surges
- power crossing perturbations

2. LIGHTNING SURGES

The lightning overvoltage is simulated by a biexponentional wave, which is defined by the rise time t1 and the duration t2 between the start and the time at which the falling edge crosses half the peak value (fig.1)

Figure 1 : Standard wave



Each country publishes it standard, which can be summarized by the times t1 and t2, the peak voltage of the wave and the surge generator diagram. Table 1 gives on inexhaustive list of the standards :

Table 1 : Lightning surges standards.

COUNTRY	AUTHORITY	WAVEFORM (µs)
ENGLAND	CCITT-417	10/700
	BRITISH TELECOM	10/700
FRANCE	PTT	0.5/700
GERMANY	BUNDESPOST	10/700
ITALY	SIP	10/700
		1/1000
SPAIN	COMPANY TELEFONICA DE ESPANA	1/1000
SWEDEN	TELEVERKET	10/700
SWITZERLAND	PTT - BETRIEBE	10/700
		1.2/50
USA	BELL	10/1000
		10/360
		2/10
	FCC	10/560
		10/160
		2/10

The peak voltage value varies from 1 kV to 2 kV according to the country.

The following figures give the schematics of the surge generators mainly used :

Figure 2 : 10/700 µs wave generator

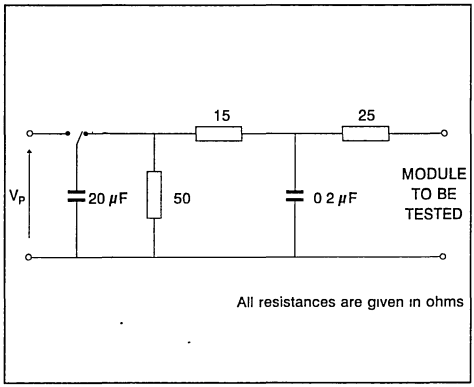


Figure 3 : 1.2/50 µs wave generator

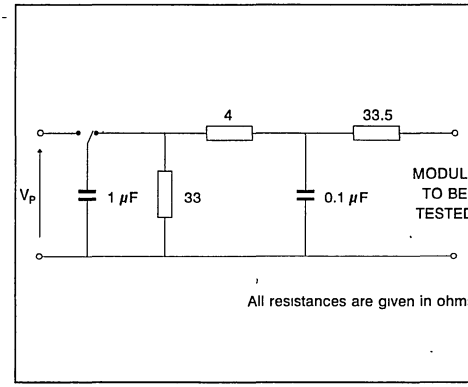


Figure 4 : 0.5/700 µs wave generator

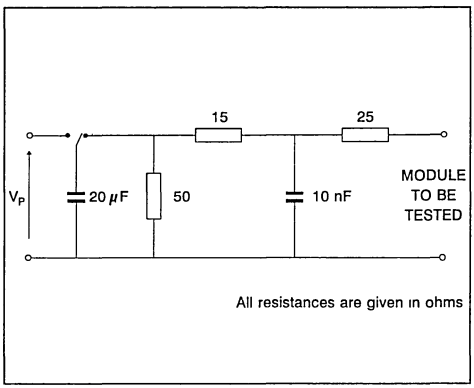


Figure 5 : 10/560 µs wave generator

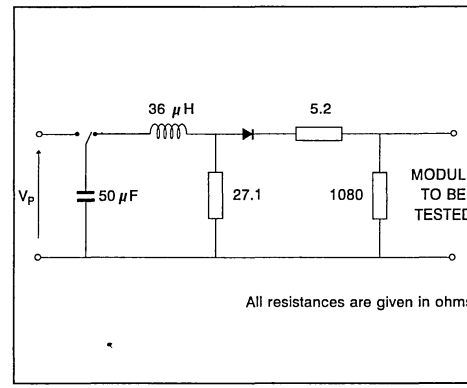


Figure 6 : 1/1000 µs wave generator

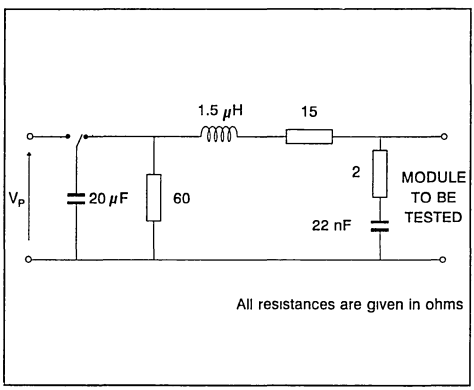


Figure 7 : 10/160 µs wave generator

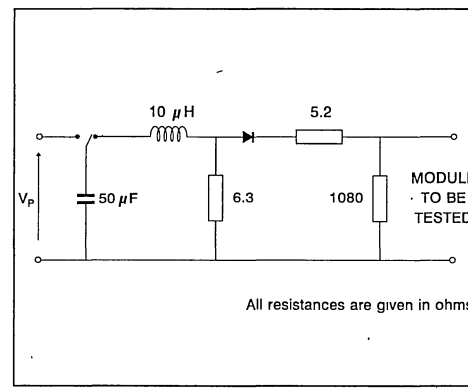
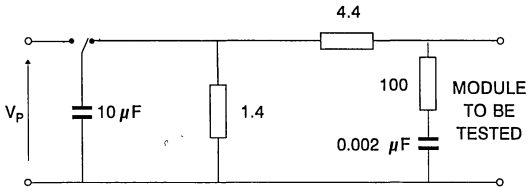


Figure 8 : 2/10 µs wave generator

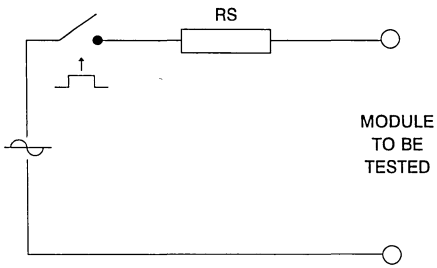


All resistances are given in ohms

3. CROSSING OR PROXIMITY WITH MAINS AC LINES :

Crossing or proximity is simulated by a sine wave generator (50 or 60 Hz) connected through a series resistor for a defined time (fig.9)

Figure 9 : Crossing simulation generator



For terminal applications this power crossing test is not widely required because only a few countries impose this standard.

The typical protection arrangement consists of a crowbar device plus a PTC.

4. CONCLUSION

Many different telecommunications protection standards are currently in use around the world. The SGS-THOMSON range of protection devices enables all of these to be covered.

PROTECTION SCHEMATICS FOR TELEPHONE SETS

C. Politano

INTRODUCTION

The type of telephone set that is being protected must first be identified.

A telephone set connected to a public network must be able to withstand surges described in standards such as CCITTK17, VDE0433, I3121, etc.

A telephone set connected to a private network is subjected to much less severe surge conditions.

In each case, SGS-THOMSON offers a suitable protection solution based on crowbar devices which can provide a very high surge current capability (from 30 Amp. to 100 Amp., 10/1000µs pulse width).

Table 1 below shows the complete product range available for telephone set protection.

Table 1 : Telephone set protection product range

TRISIL			3 TERMINAL TRISIL		GATE TRIGGERED SUPPRESSOR (current limitation)	
						
AXIAL	**SOD**	**DIL8**	**SO8**	**DIL8**	**SO8**	**DIL8**
50A TPAxx 100A TPBxx	50A SMTPAxx 100A SMTPBxx	100A @10/1000µS LS5018B LS5060B LS5120B	 THBT15011 THBT20011 THBT27011	 THBT15012 THBT20012 THBT27012	30A @ 10/1000µS TPP25011	30A @ 10/1000µS TPP25012 100A@10/1000µS L3100B1

1. CHOICE OF THE PROTECTION DEVICE:

To choose the right protection device, the user will have to determine the following characteristics :

1) Surge current capability

2) Functional parameters

1.1. Surge current capability

There are two kinds of disturbances which have to be evaluated in order to define correctly the surge current capability of the protection device :

I.1.1. Protection against short duration disturbances :

These are transient overvoltages, which are specified in telecom standards such as CCITT k17, VDE04-33, I3121. The typical voltage waveforms are the 10/700µs and the 1.2/ 50µs types.

The user has to take care that the protection standard specifies voltage pulse waveforms, which have to be converted into pulse current waveforms. Thus he will obtain the peak surge current value Ipp which has to be withstood by the protection device.
(See application note 2.2 : Voltage to current waveform conversion).

I.1.2. Protection against long duration disturbances.

In this case, the standards can be very different from one country to another, and the duration of the superimposed mains on telephone lines can reach more than 10 minutes with a current of around 8A. Obviously, it is not possible to withstand such surges with a plastic component. An economical and reliable solution is to use a PTC (positive temperature coefficient thermistor). These PTC devices with 10 Ω resistance (at 25°C) can reach a few k during the surge. The switching time depends on the surge current and the PTC. Nevertheless, most PTCs tested with an alternating surge current of 8 A react in 10 to 100 ms. Such a device could therefore be combined with a TPA Trisil which is able to withstand 8 A for 150 ms without any problem (see data sheet). In case of higher current the TPB versions should be used.

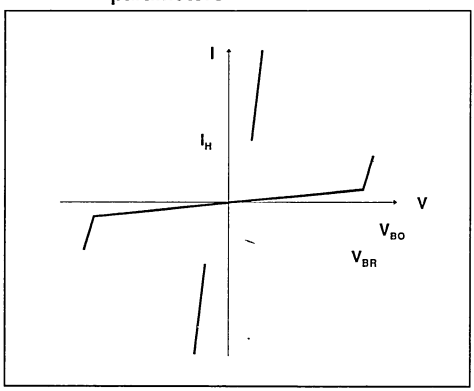
In conclusion, Trisil + PTC thermistor is the best performance / cost compromise for the subscriber telephone set protection.

1.2. Functional parameters :

To select the right CROWBAR protection, three main parameters have to be defined according to the application (see fig.1) :

- The minimum breakdown voltage : V_{BR}
- The maximum breakover voltage : V_{BO}
- The minimum holding current : I_H

Figure 1 : Crowbar protection electrical parameters



I.2.1. The breakdown voltage : V_{BR}

The V_{BR} has to be greater than the maximum voltage value which will be supplied in the line.

This condition will guarantee that the protection is not activated in the normal operating mode (no overvoltage).

I.2.2. The breakover voltage : V_{BO}

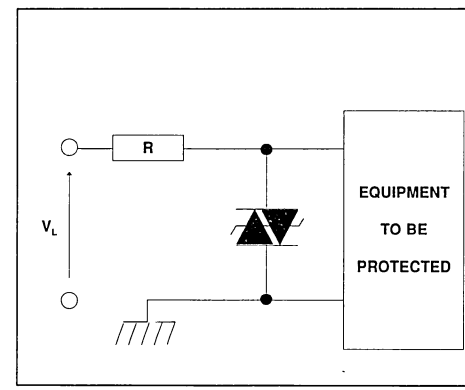
The breakover voltage (V_{BO}) has to be lower than the max-ratings of the component to be protected. This level is reached just before the protection device switches to the ON-STATE. The duration of the residual transient linked to the break-over voltage is very short : it does not exceed 1 us.

I.2.3. The holding current : I_H

When a crowbar device is used for protection, it is absolutely necessary to ensure that the holding current is higher than the maximum current available in the Telecom line. If this criterion is not obeyed, the Trisil triggers but does not return correctly to its blocked state after the disturbance.

Since the Trisil voltage in the conduction state is low, the condition can be expressed by the inequality $I_H > (V_L/R)$. See fig.2.

Figure 2 : Equipment protection by Trisil



This is shown in figure 3 where the current does not drop below the holding current. The Trisil cannot return to the blocked state and thus remains as a quasi short-circuit, preventing operation of the equipment to be protected.

In the case of figure 4, the current drops below the value of the holding current and the internal mechanism of the Trisil enables it to return to the blocked state after the current surge.

Figure 3 : Wrong choice of the Trisil

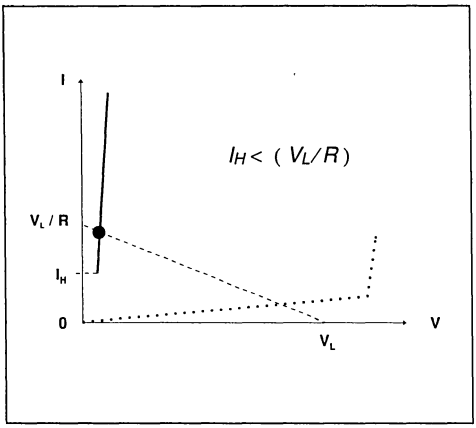
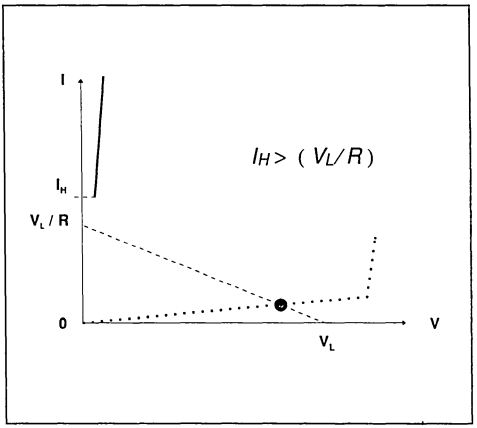


Figure 4 : Right choice of the Trisil



2. APPLICATION DIAGRAMMS :

Fig. 5 to 8 show typical protection solutions used for telephone sets and other terminals.

Figure 5 : Ring and speech circuit protection

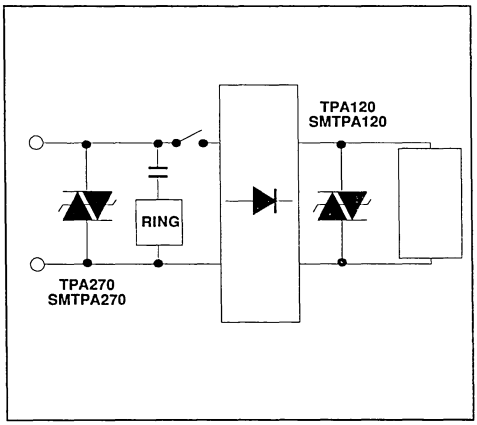


Figure 6 : Monochip circuit protection

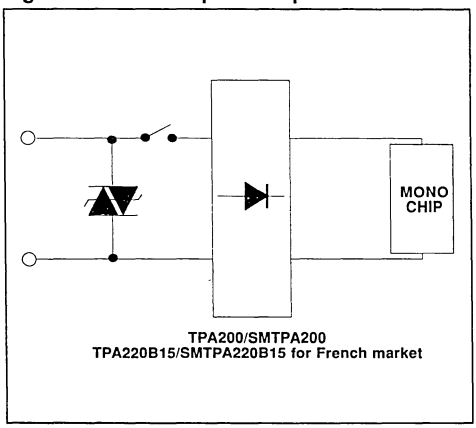


Figure 7a : Overvoltage protection and current limitation (I_{PP} = 100 A 10/1000 µs)

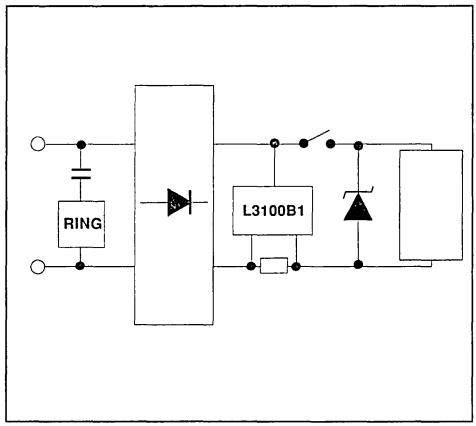


Figure 7b : Overvoltage portection and current limitation (IPP = 30 A 10/1000 ms)

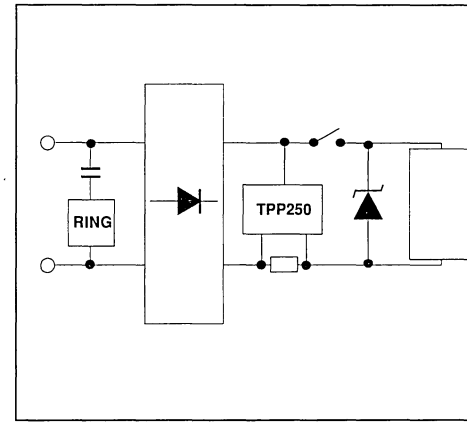


Figure 8a : Electronic hook switch protection

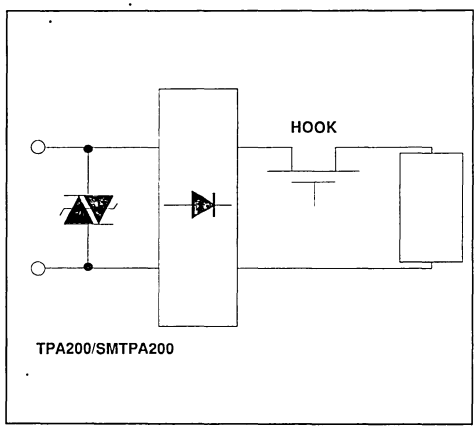


Figure 8b : Electronic hook switch protection

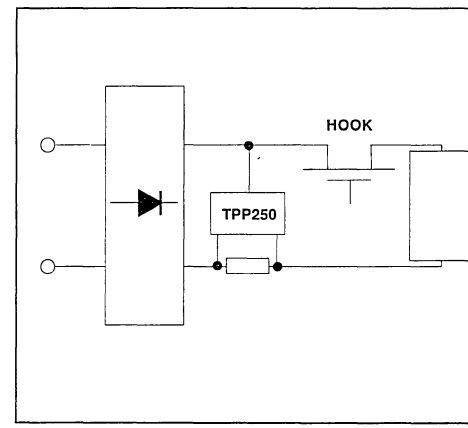
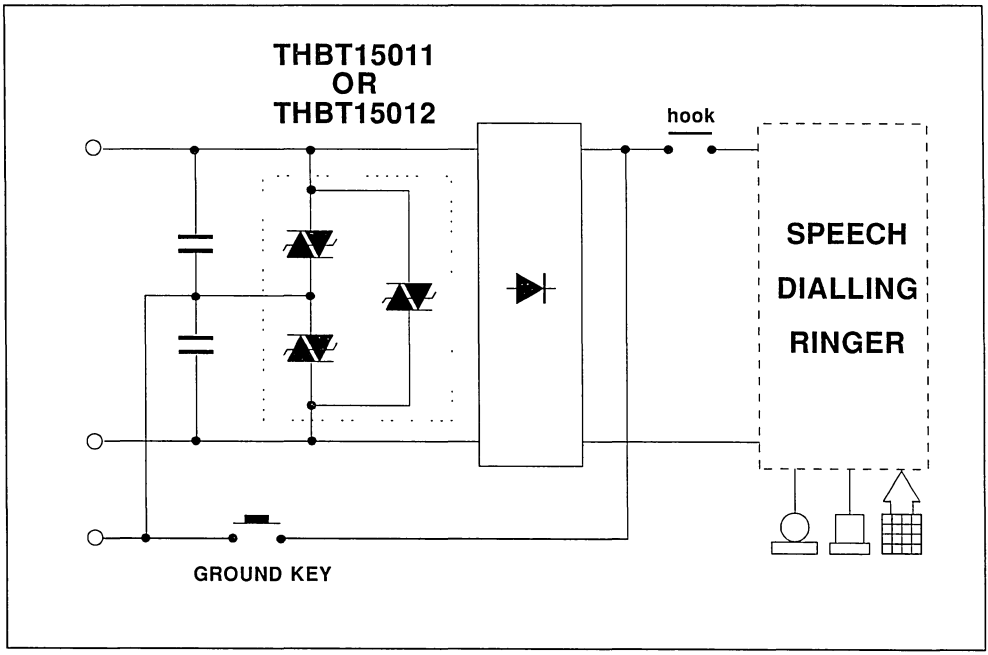


Figure 9 : German version with ground key



3. CONCLUSION

Whether the telephone set is connected to a public or private network, SGS-THOMSON offers a range of protection devices to cover all relevant standards.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

PROTECTION STANDARDS APPLICABLE TO SWITCHING EQUIPMENT

A. Bremond

1. INTRODUCTION

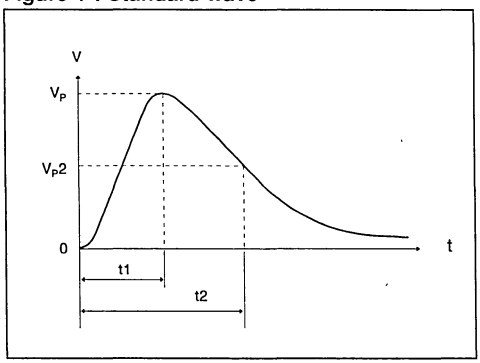
The purpose of this document is to summarize the main telecommunication standards with regard to the protection requirements against two types of overvoltage :

- lightning surges
- power crossing perturbations

2. LIGHTNING SURGES

The lightning overvoltage is simulated by a biexponentional wave, which is defined by the rise time t1 and the duration t2 between the start and the time at which the falling edge crosses half the peak value (fig.1)

Figure 1 : Standard wave



Each country publishes its standard, which can be summarized by the times t1 and t2, the peak voltage of the wave and the surge generator diagram. Table 1 gives on inexhaustive list of the standards .

Table 1 : Lightning surge standards

COUNTRY	AUTHORITY	WAVEFORM (µs)
ENGLAND	BRITISH TELECOM	10/700
FRANCE	PTT	0.5/700
GERMANY	BUNDESPOST	10/700
ITALY	SIP	10/700 1/1000
SPAIN	COMPANY TELEFONICA DE ESPANA	1/1000
SWEDEN	TELEVERKET	10/700
SWITZERLAND	PTT - BETRIEBE	10/700 1.2/50
USA	BELL	10/1000 10/360 2/10
	FCC	10/560 10/160 2/10

The following figures give the schematics of the surge generators mainly used :

Figure 2 : 10/700 µs wave generator

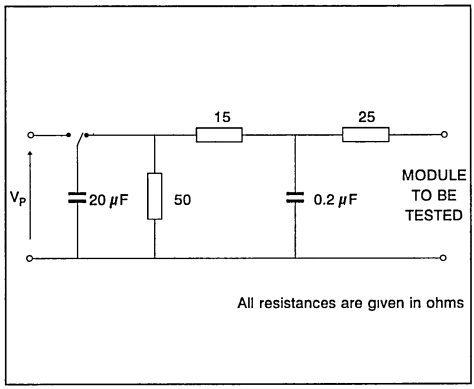


Figure 3 : 1.2/50 µs wave generator

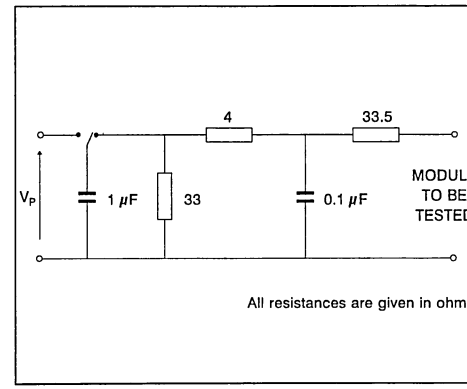


Figure 4 : 0.5/700 µs wave generator

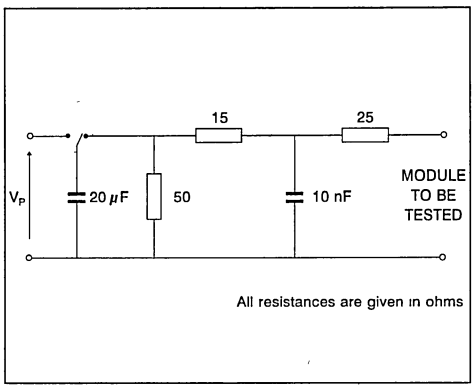


Figure 5 : 10/560 µs wave generator

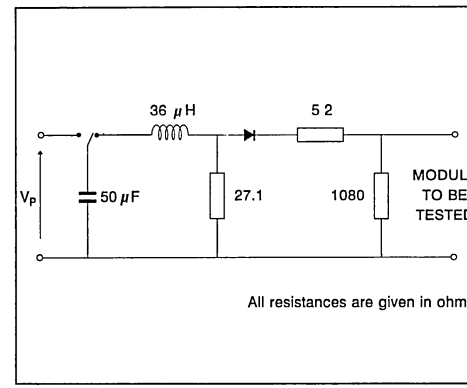


Figure 6 : 1/1000 µs wave generator

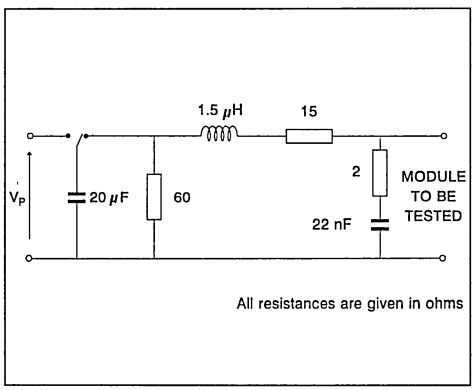


Figure 7 : 10/160 µs wave generator

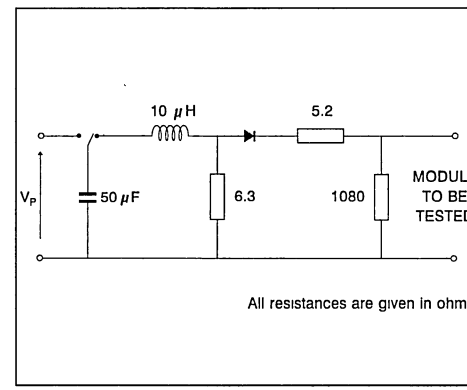
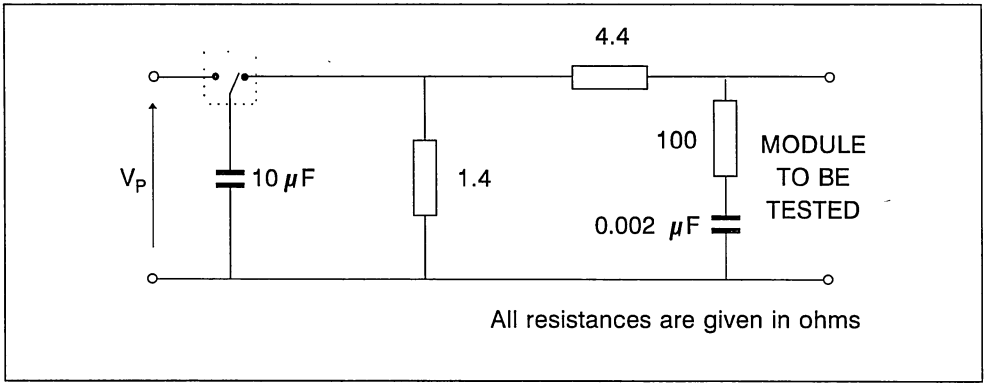


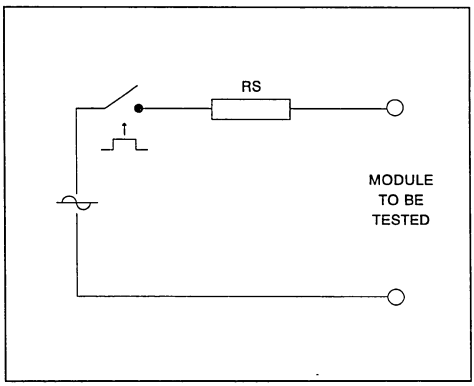
Figure 8 : 2/10 µs wave generator



3. CROSSING OR PROXIMITY WITH MAINS AC LINES :

Crossing or proximity is simulated by a sine wave generator (50 or 60 Hz) connected through a series resistor for a defined time (fig.9).

Figure 9 : Crossing simulation generator



4. CONCLUSION

Telecommunications is a field in which the protection against overvoltages is well defined by standards. The SGS-THOMSON range of protection devices enables all of these to be covered.

Table 2 give some example of crossing simulations.

Table 2 : Power crossing simulations

COUNTRY	VOLTAGE Volts RMS	SERIES RESISTOR (Ohms)	DURATION
ENGLAND	0 TO 250 0 TO 650 0 TO 430 (50 Hz)	40 TO 400 150 150	15mn 1s 2s
FRANCE	0 TO 1000 > 1000 (50 Hz)	20 3000	Trains of - 1s "on" - 1s "off" -1s "on" 10 times with 10mn between trains
GERMANY	300 (50 Hz or 16.6Hz)	600	200 ms
ITALY	300 650 220	600 200 10 or 600	500 ms 500 ms 15 mn
USA	0 - 50 50 - 100 100 - 600	150 600 600	15 mn 15 mn 60 x 1s application

Note : Protection resistors on the line card inputs decrase the peak surge current.
These elements have to be taken into account during the line card design to optimize the protection function.

PROTECTION SCHEMATICS FOR SWITCHING SYSTEMS

A. Bremond

1. INTRODUCTION

The aim of this note is to summarize the major characteristics of a SLIC and to propose protection solutions for each configuration.

2. SLIC FUNCTION

2.1. Slic generalities :

The Slic function is defined by the acronym BORCHT :

- Battery feeding
- Overvoltage protection
- Ringing
- Signalling
- Codec
- Hybrid
- Test

The important parameters to define the OVERVOLTAGE PROTECTION are the battery feeding and the ringing signal.

2.1.A/ battery feeding :

This sub-function of the Slic is characterized by:

- The battery voltage typical value (generally between 45 and 65 V)
- The tolerance of the voltage value
- The possibility to switch from one value to another one (line cards designed to operate equally on normal and long lines)

2.1.B/ Ringing signal :

For the ringing, two parameters need to be taken into account :
- The voltage value (generally between 70 and 100 V RMS)
- The ringing configuration (fig.1)

2.2. Different kinds of Slic :

There are two Slic families :
- The Slic without integrated ring generator
- The Slic with integrated ring generator

Figure 1 : Different ringing configurations

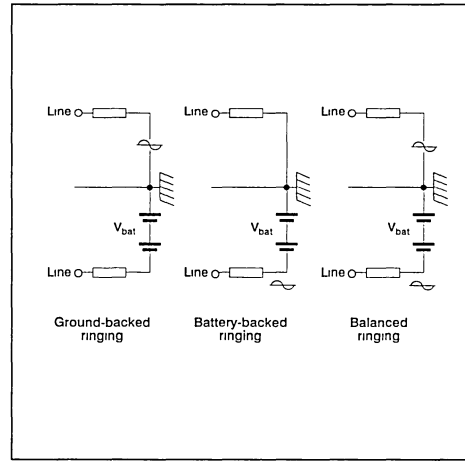
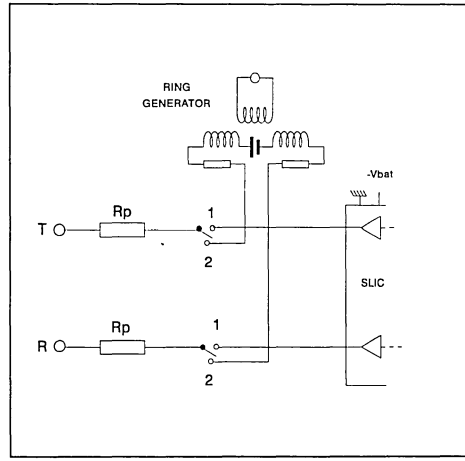


Figure 2a : Slic without integrated ring generator

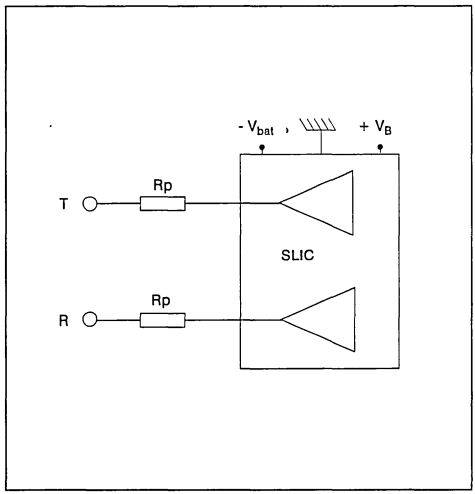


2.2.A/ Slic without integrated ring generator :

For this case the Slic IC is supplied between ground and the battery voltage (- V_{bat}).

The relay operates the selection of functions, ringing mode in position 2 and the other modes in position 1. (see fig 2a).

Figure 2b : Slic with integrated ring generator



2.2.B/ Slic with integrated ring generator :

This kind of Slic, e.g. the L3000 family of SGS-THOMSON, is supplied between ground, the battery (-V_{bat}) and a positive voltage (+V_B) up to +72 V. (see fig 2b).

2.3. Goal of the Slic protection :

The purpose of the protection is to suppress all overvoltages out of the normal operating voltage range of the Slic.

We have to take into account the two kinds of Slic described in section 2.2.

2.2.A/ Slic without integrated ring generator :

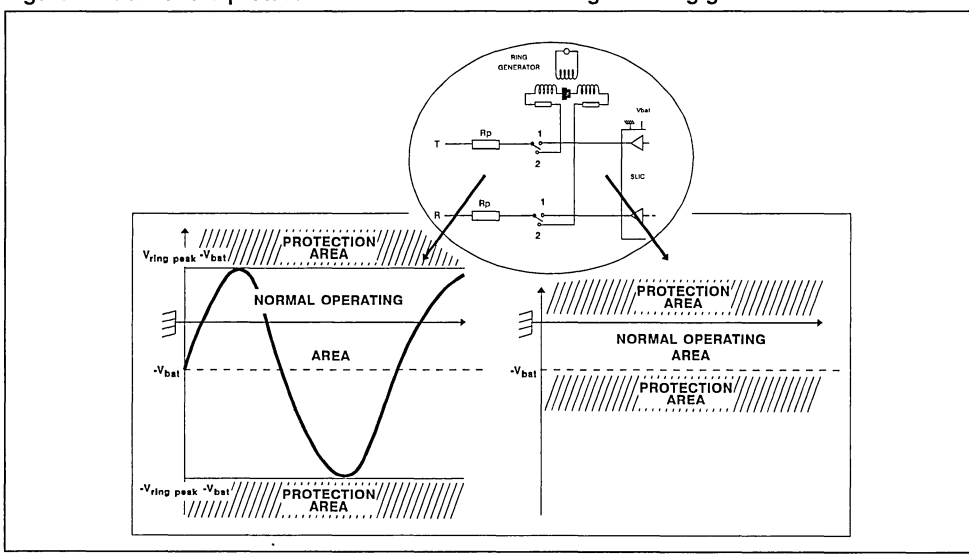
As shown in Fig.3, the protection areas are located differently before and after the ring relay.

Before the relay the protection must operate over the peak value of the ring signal (generally +90V and -190V). As the relay protection does not require a very precise clamping threshold, we usually use a symmetrical overvoltage suppressor (generally + or -200 V).

After the relay the protection acts to suppress all spikes above ground and below the battery voltage (-V_{bat}).

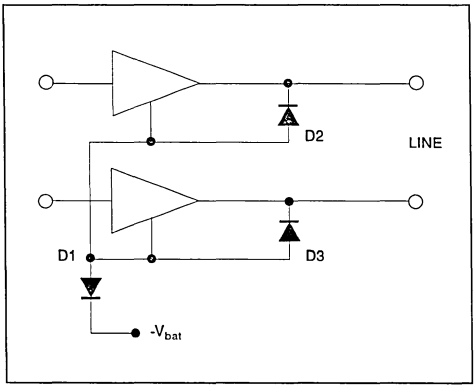
It is important to note that the integrated circuit needs a protection threshold as close as possible to the supply voltage.

Figure 3 : Goal of the protection for the SLIC without integrated ring generator



In certain cases an internal network of diodes allows the output stages of the Slic to be oversupplied (see fig.4).

Figure 4 : Internal diode network of the TDB7722

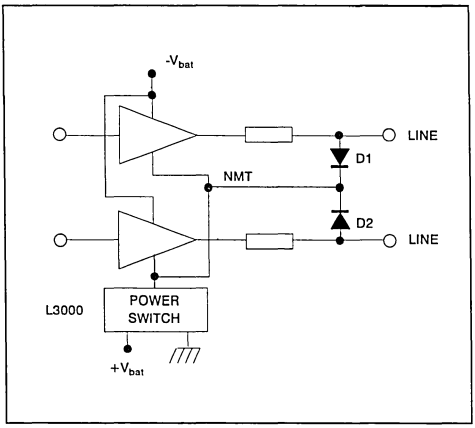


2.3.B/ Slic with integrated ring generator :

The integrated circuit L3000 of SGS-THOMSON is presently the only Slic of this kind. It operates between ground and the battery voltage for all the modes except for the ringing, where the operating area is located between $+V_B$ (up to 72 V) and the battery voltage ($-V_{Bat}$) (see Fig.5). The protection takes into account this fact and operates above $+V_B$ and below $-V_{Bat}$.

The diodes D1 and D2 (fig.5) act when the L3000 operates out of the ringing mode and when a positive overvoltage is clamped at $+V_B$. The output stages are then temporarily oversupplied at $+V_B$.

Figure 5 : External diode network used with the L3000



3. APPLICATION DIAGRAMS

3.1. Slic without integrated ring generator

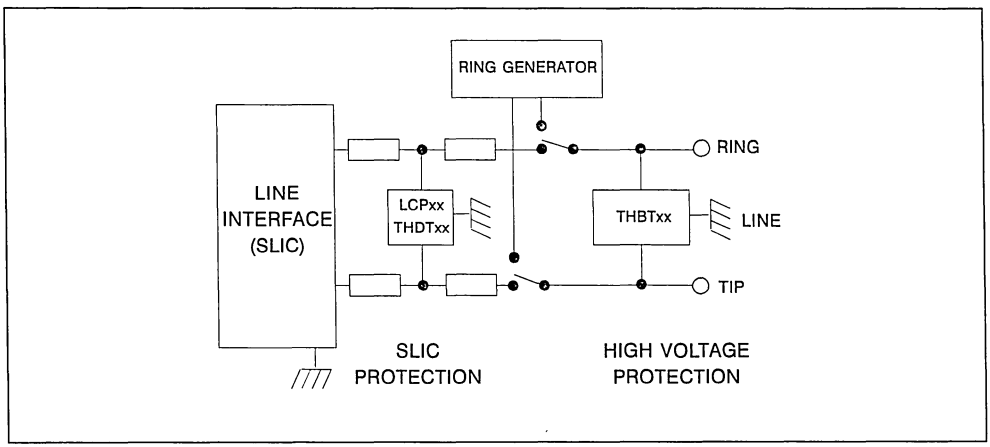
Fig.6 below shows the protection topology for line card protection. The protection is divided into two stages :

- The high voltage protection for ring relays (THBTxx series)

- The low voltage protection for the Slic. Here there are two possibilities :

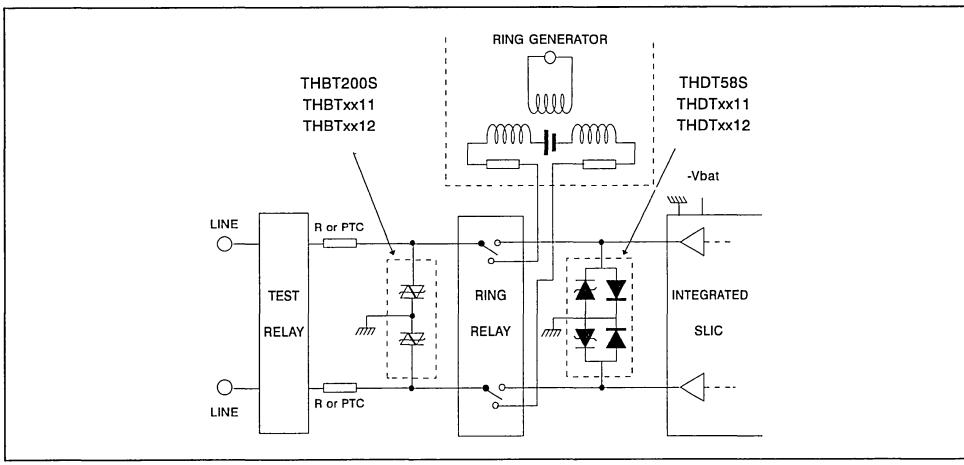
- Fixed breakdown voltage (THDTxx series).
- Programmable breakdown voltage (LCPXX series)

Figure 6 : Typical line card protection at PC board level



3.1.1. Slic protection with fixed breakdown voltage.

Figure 7 : Line card protection kit



A specific product range for line card protection is available with kit solutions (for ring relays and Slic protection) in S08, DIL8 and SIP3 packages. As shown in figure 7, they are bidirectional functions for relay protection and asymmetrical functions for Slic protection.

These solutions provide the following advantages :

- Different surge current capabilities are available.
- Area used by the protection on the PC board is reduced.
- Optimum cost/performance compromise is possible.

Fig. 8 and fig.9 show the product range offered by SGS-THOMSON, with versions available also in axial from or in the surface mount package SOD15.

Figure 8 : High voltage protection range = THBTxx

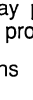
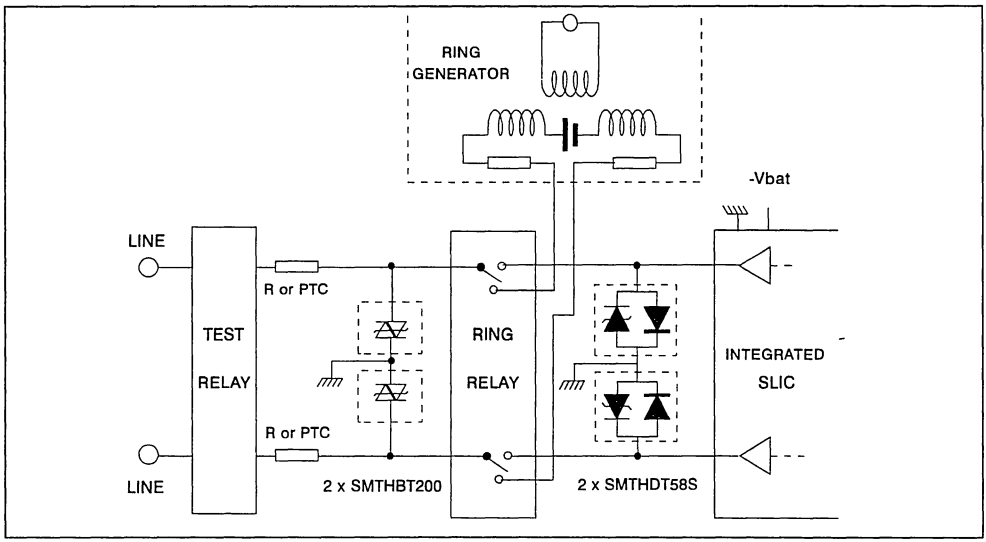
TRISIL	DUAL TRISIL	3 TERMINAL TRISIL	
			
SOD15	SIP3	SO8	DIL8
75A @ 10/1000 µsec		30A @ 10/1000 µsec	
SMTHBT 200	THBT200S	THBT15011 THBT20011 THBT27011	THBT15012 THBT20012 THBT27012

Figure 9 : Slic protection range fixed breakdown voltage = THDTxx

SOD15	CB429	SIL3	SO8	DIL8
HIGH SURGE CAPABILITY 75A @ 10/1000 µsec			**MEDIUM SURGE CAPABILITY 30A @ 10/1000 µsec**	
SINGLE FUNCTION		DUAL FUNCTION	DUAL FUNCTION	
SMTHBT58	TPU58	THDT58S	THBT5111 THBT6511	THBT5112 THBT6512

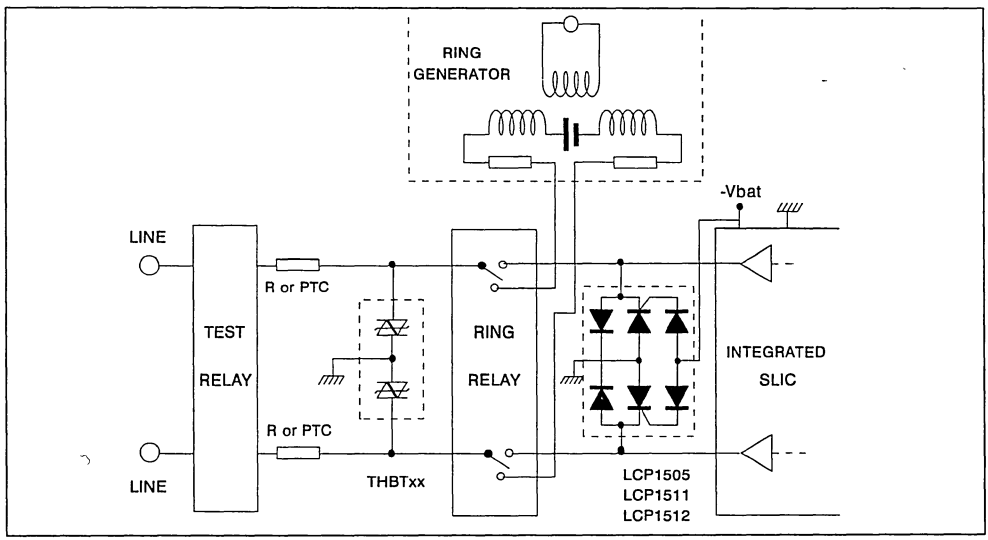
Figure 10 : Surface mount solution in SOD 15



This solution is mainly used to benefit from the high surge current capability of the SOD 15 package for AC tests. Such high surge performance can only be achieved with this SMD package.

3.1.2. Slic protection with programmable breakdown voltage

Figure 11 : Monochip programmable breakover voltage solution



With this solution, the protection performance is improved by the possibility of adjusting the breakdown voltage to the battery voltage. This function is well suited to variable battery voltage applications such as short / long line switching.

Figure 12 gives the product range with this function, available in SIL4, DIL8 and SO8 packages.

Figure 12 : Slic protection range LCPxx - Programmable breakdown voltage

SIL4	SO8	DIL8
HIGH SURGE CAPABILITY 75A @ 10/1000 µsec	**MEDIUM SURGE CAPABILITY** 30A @ 10/1000 µsec	
LCP150S	LCP1511	LCP1512

3.2. Slic with integrated ring generator : (Slic L3000)

Many types of Slic protection solutions exist, depending on :
- The battery voltage
- The PC board area available for the protection
- The cost / performance compromise

3.2.1. L3000 protection with 2 x L3121B

This topology (Fig.13) is the most efficient one for this kind of Slic.

3.2.2. L3000 protection with 2 x L3100B

Figure 13 : L3000 protection with 2 L3121B

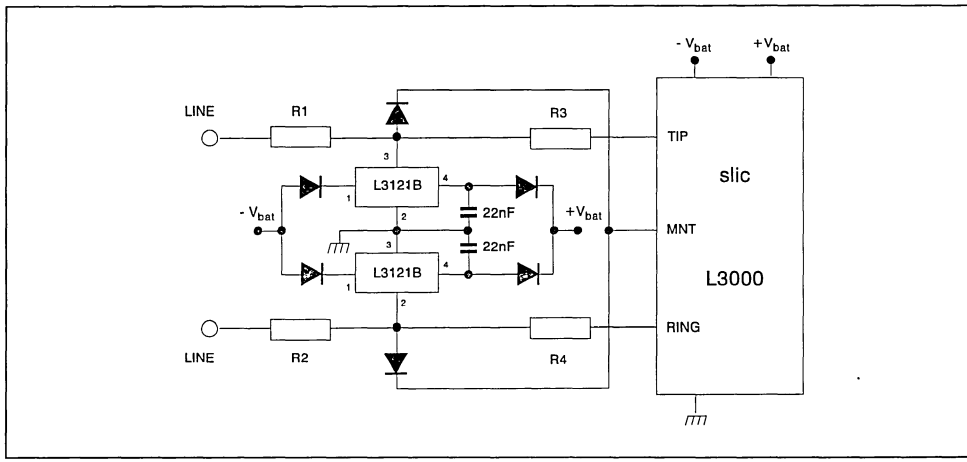


Figure 14 : L3000 protection with 2 L3100B

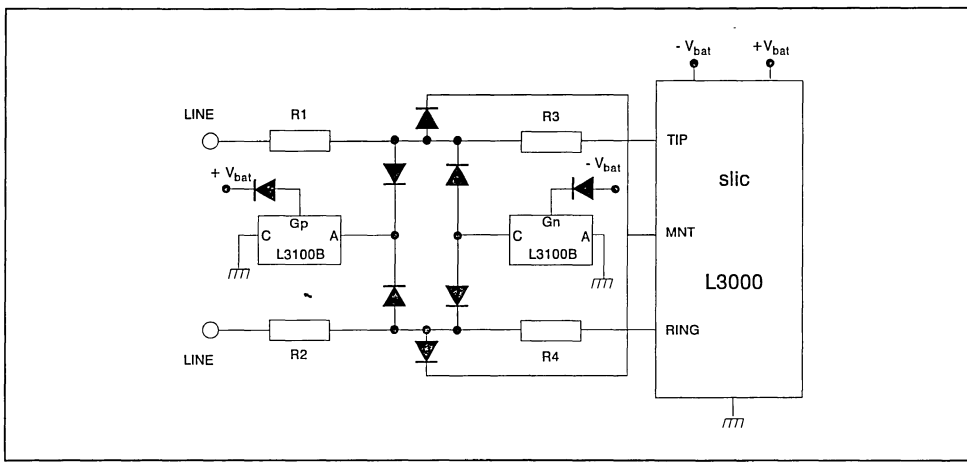


Figure 14 has the same electrical behaviour as the previous one but with lower cost.

3.2.3. Multiline common protection :

These types of application (Fig.15 and 16) decrease the cost of the protection per line. The major drawbacks of these solutions are :

- The short circuit across all the lines when the protection device fires.

- The current remaining through the protection device after the surge is too high to allow its automatic switch-off. This must then be effected by a software instruction, e.g. power-down.

4. CONCLUSION

The wide range of protection devices on offer from SGS-THOMSON makes an optimized protection solution possible for every application.

Figure 15 : Common protection for Slic without integrated ring generator

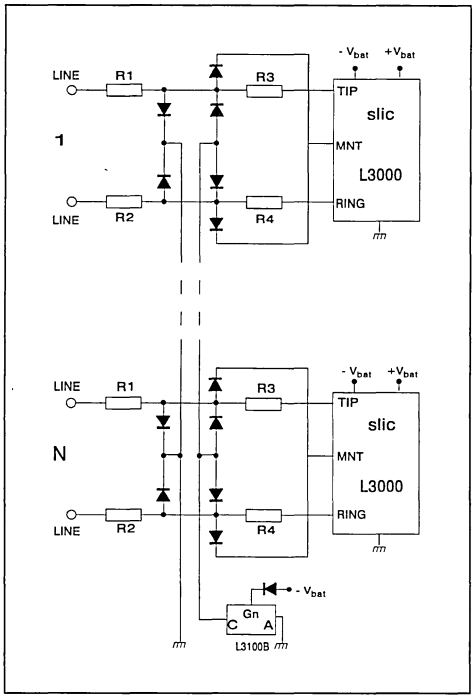
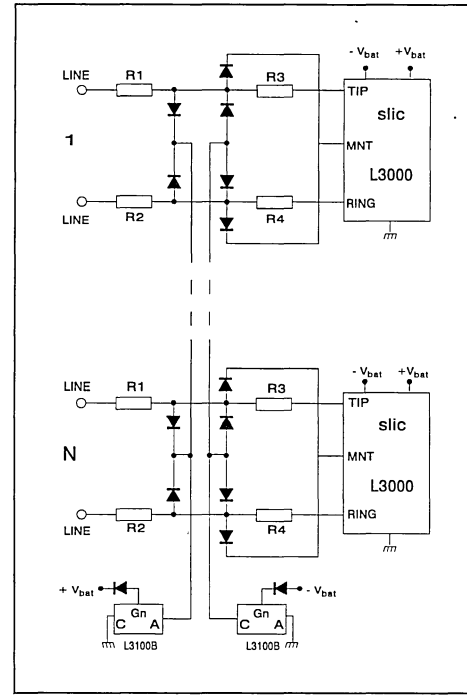


Figure 16 : Common protection for Slic with integrated ring generator



ISDN INTERFACE PROTECTION

C. Politano

I. INTRODUCTION

The choice of a suitable protection device for an ISDN line interface requires consideration of a parameter which is not critical in analogue line applications : the parasitic capacitance that the device introduces. Because of the high data rates used, parasitic capacitances must be minimized in order to ensure correct signal transmission. In particular, attention must be paid to the capacitance imbalance in the line which can cause considerable signal degradation. Such imbalance most frequently results from the presence of common-mode protection, in which the capacitance introduced between each line and earth is frequently unequal.

SGS-THOMSON has developed a complete range of specific protection devices for ISDN applications : the " TRIBALANCED PROTECTION " TPIxx series.

These devices introduce only a minimum of capacitance imbalance (30pF), which does not affect the transmission performance of the line.

2. TRIBALANCED PROTECTION = TPIxx SERIES

The use of TRIBALANCED protection is mandatory under the following conditions :

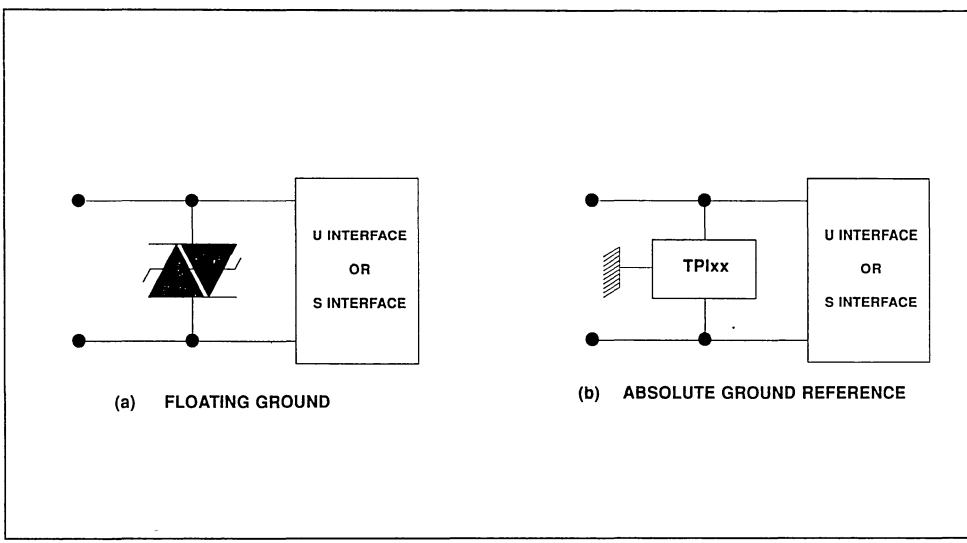
- The bias voltage on line A and line B is different (line A = GND, Line B = -Vbat)

- The protection is realized in common mode, as illustrated in fig.1 (b).

In this case, two conditions must be satisfied :

1) Low capacitance from line to ground → No signal attenuation
2) Good capacitance balance between line a and line b → Good longitudinal balance on the line.

Figure 1 : ISDN interface protection



3. ISDN PROTECTION - PRODUCT RANGE :

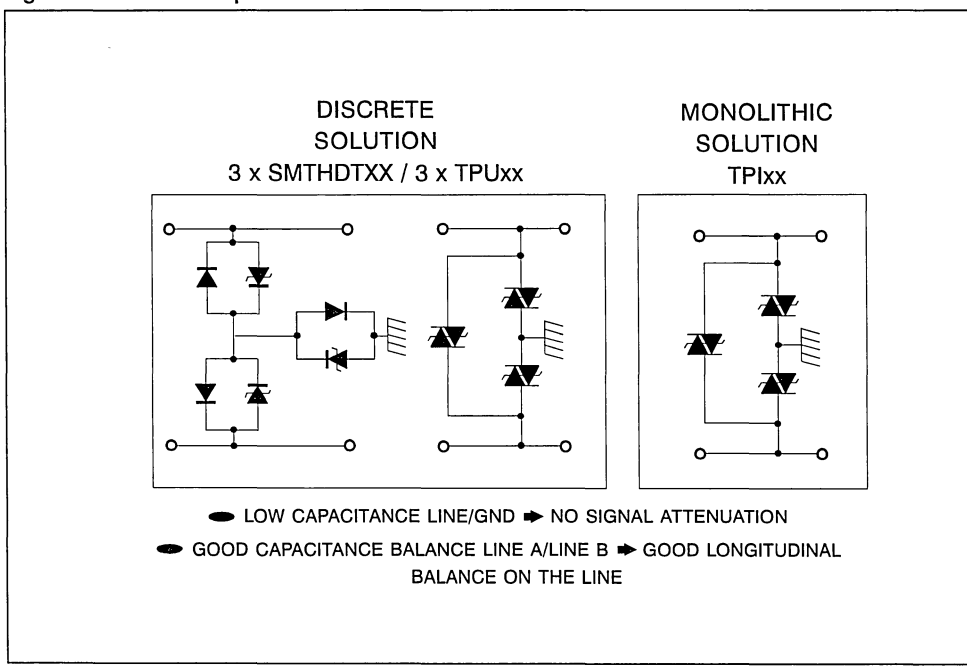
SGS-THOMSON offers specific protection devices for ISDN interface protection. The product range is given in fig.2, which shows that this function is available with different package versions.

Discrete and monolithic versions are available, in order to provide a wide choice of cost/performance compromises.
Depending on the solution chosen, different recommendations apply with regard to the optimum configuration to use. Fig.3 illustrates the typical application schematic for TRIBALANCED PROTECTION. When the discrete solution is used, three components per line are necessary.

Figure 2 : Tribalanced protection - product range

DISCRETE SOLUTION (3 devices per line)	**MONOLITHIC DEVICES**
SOD15 / CB429	SO8 / DIL8
HIGH SURGE CAPABILITY 75A 10/1000 msec	**MEDIUM SURGE CAPABILITY** 30A 10/1000 msec
SMTHDT58 / TPU58 SMTHDT80 / TPU80 SMTHDT120 / TPU120	TPI8011P / TPI8012P TPI12011P / TPI12012P

Figure 3 : Tribalanced protection - functional schematic



4. APPLICATION SCHEMATICS

Fig.4 and 5 illustrate the use of tribalanced protection in a u-interface and an s-interface respectively. In each case there is the choice of a discrete solution (SMTHDTxx or TPUxx) where a high surge capability is required, or a single-chip solution for low cost (TPIxx). Thus cost and performance can be traded in a variety of combinations. All of these components are innovative and ideal for use in high-speed transmission lines.

Figure 4 : Central office / PABX - U-Interface protection

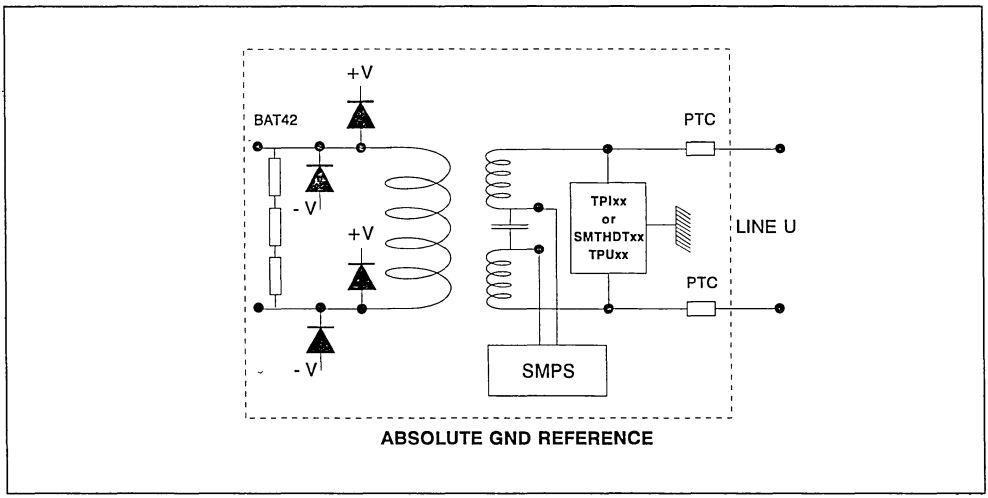
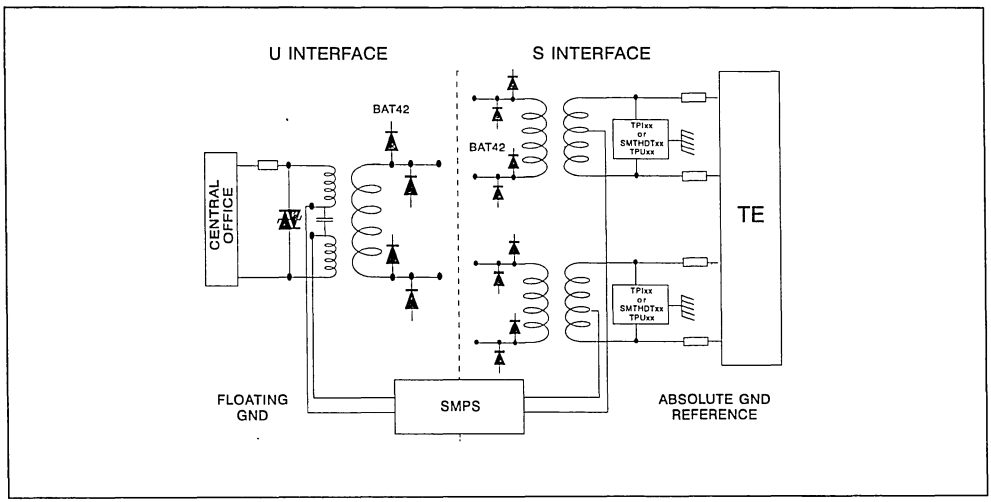


Figure 5 : NT1 = S-Interface protection



5. CONCLUSION

Due to the sensitivity of ISDN to capacitance imbalance on the lines, tribalanced protection has to be used where common-mode protection of lines with different bias voltages is required. SGS-THOMSON offers a wide range of devices designed specifically for ISDN protection, enabling this requirement to be satisfied.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

SGS-THOMSON SYSTEMS FOR RECHARGEABLE BATTERIES

1 - FOREWORD

In casual language a battery pack is anything that supplies electrical power through a chemical reaction whose description is beyond the scope of this note and it is normally built by a combination (series, parallel, or both) of cells that are the basic electrochemical building blocks.
In the following a battery pack will be simply named battery.
Batteries can be grouped into two distinct categories:

- Disposable Primary Batteries
- Rechargeable Secondary Batteries

This note deals with the SGS-THOMSON systems for rechargeable batteries but it is worth to mention some typical characteristics of primary batteries too.

Primary batteries

The variety of types, based on different chemistries, is very high (for lithium batteries alone there are more than 30 different types).
However these types of batteries share some common characteristics:

- Primary batteries offer significantly higher energy density, i.e. for a given volume more watts per hour are available when compared with secondary batteries.
- Primary batteries offer a lower self-discharge rate
- Primary batteries are less expensive than secondary
- Primary batteries have higher internal impedance so that they have less current sourcing capability.
- Thanks to standardization, replacement is easy world wide.

Secondary batteries

Despite the advantages mentioned above, there is a growing demand on secondary batteries because of:

- Increased electrical power drain of portable equipment that would exhaust very rapidly the energy stored into a primary battery.
- Increased sensitivity to the environment protection: primary batteries must be disposed of and they contain materials that are hazardous for the environment.

Some types of rechargeable batteries contains hazardous materials too but they exhibit a much longer usable life so that one secondary battery can replace more than 500 disposable batteries.
The most popular secondary batteries can be divided into three major groups:

- Lead-acid
- Nickel-cadmium
- Nickel-Metal hydride

A fourth technology, Lithium-Jon, is now reaching the market even if the number of manufacturers as well as the volumes are still limited. This new technology is quite promising because it will offer a significant leap in energy density.

The table 1 shows some typical values for primary and secondary batteries that, however, can vary with manufacturer and battery size.

SGS-THOMSON have developed various families of products for the specific application in the field of secondary batteries. These families are briefly described in the data book. It must be noted that the large variety of:

- battery types and sizes.
- available energy source (mains or car batteries).
- connections to the final sets where batteries are employed.
- etc.

does not allow an appropriate product standardization. Therefore the following descriptions deal mainly with the basic principles of SGS-THOMSON products.

For specific application, please contact the local SGS-THOMSON organization or the Division Product Marketing:

SUBSYSTEMS PRODUCTS GROUP
SGS-THOMSON MICROELECTRONICS
20041 AGRATE BRIANZA - ITALY
CENTRO DIREZIONALE COLLEONI
PALAZZO ANDROMEDA, 3
Tel: 0039-39-635574 Fax: 0039-39-635582

Table 1: Typical battery performance at 20 °C

Type : PRIMARY	Nominal Voltage	Energy Density W•h / Kg
Alkaline - MnO2	1.4	130
Carbon - Zinc	1.3	65
Lithium - MnO2	2.7	230
Mercury - Zinc	1.3	110
Silver - Oxide *	1.5	130
Zinc - Air *	1.3	300
Type : SECONDARY		
Lead - Acid	2	35
Nickel - Cadmium	1.2	35
Nickel - Metal Hydride	1.2	55
Lithium - Jon	3.6	130

* For button cells

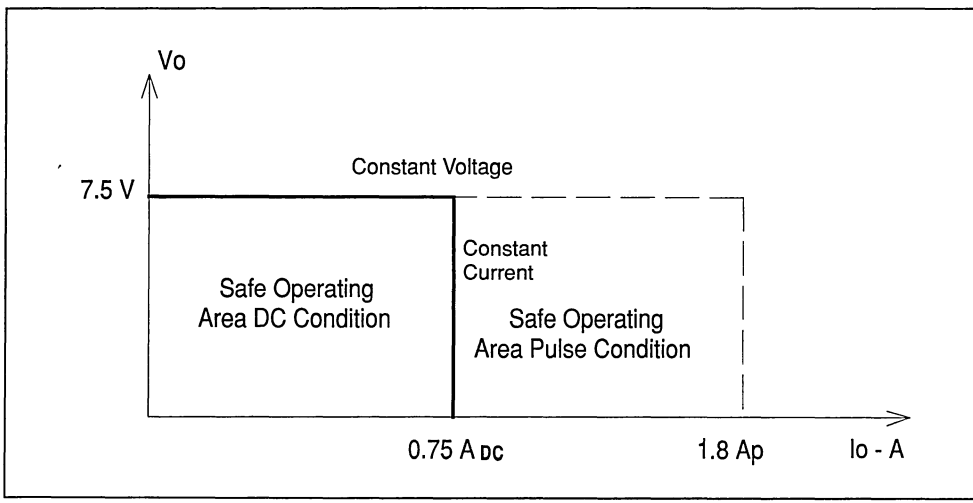
2 - BATTERY ELIMINATORS

Whenever another power source is available, it may be convenient to preserve the battery by providing an alternate method to deliver the power required by the electronic equipment.

In this case the battery is replaced by a battery eliminator that is, essentially, a constant voltage regulator. As typical example, a battery eliminator can be used to supply a handheld phone from a car battery thus avoiding the use of the phone battery during travels.

For replacement of a 5/6 cell battery pack, the GS-R28.0BE switch mode battery eliminator can be used. See the corresponding data sheet.

Figure 1. Output characteristics of GS-R28.0BE
Peak current duration: 0,6 ms with 0,13 duty cycle



3. BATTERY SAVERS

While a battery eliminator replaces completely the battery pack, a battery saver is used together with the battery pack. The battery is charged in a float mode and it is maintained in a ready-to-serve condition.
The principle is shown in fig. 2

Figure 2. Battery Saver

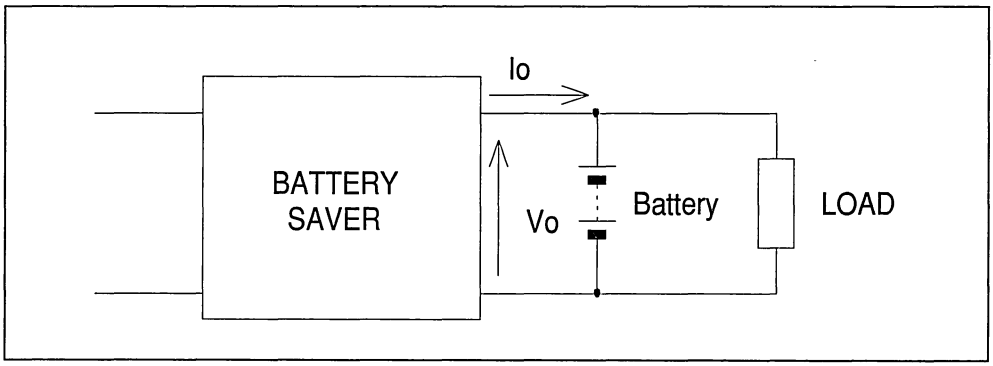


Figure 3.

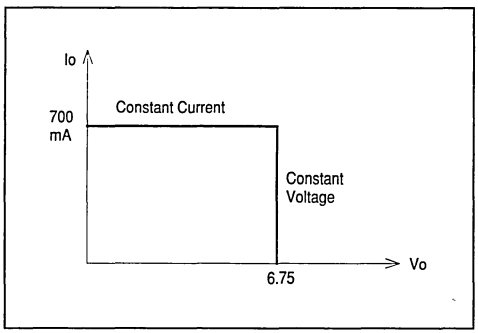
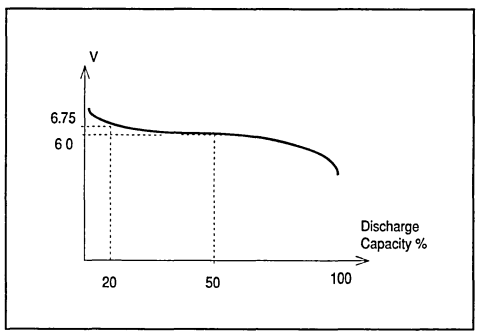


Figure 4.



The output electrical characteristics of a battery saver is shown in fig. 3.
The indicated values are relevant to a 5 cell battery pack.
If the initial battery voltage is greater than 6.75V, the battery will supply the load and no current is delivered by the battery saver. Therefore the battery is discharged by the load until its voltage reaches 6.75 V. At this point, the battery saver, working in a voltage mode (vertical line of the characteristic of fig. 3), supplies the current required by the load and the battery can save its stored energy. After removal of the battery saver, the battery is still retaining more than 80 % of its capacity (for a 5 cell battery, 50 % of capacity correspond to about 5 x 1,2 = 6.0 V as shown on the discharge curve of fig. 4).

If the initial battery voltage is lower than the preset value of 6.75 V, the battery saver works in constant current mode (horizontal line of the characteristics of fig. 3) by delivering a constant current of 700 mA that charges the battery to about 80 % of its capacity until the battery voltage reaches 6.75 V. Clearly if the load is ON, just the net difference between 700 mA and the load current is available to charge the battery.
As a typical example, a battery saver can be used to supply a handheld phone from a car battery thus providing the current needed by the phone and maintaining, in the mean time, about 80% of the battery capacity.
For utilization together with a 5 cell battery pack, the GSCC-7.007BS switch mode battery saver can be used. See the corresponding data sheet.

4. BATTERY CHARGERS

The SGS-THOMSON battery chargers are high-quality systems particularly designed to charge NiCd and NiMH batteries (for Lead-Acid and Lithium-Jon batteries, please consult SGS-THOMSON).
Proper charging is a key to success with any battery application since improper charging methodology can be detrimental to the battery life. Depending on the accuracy of this charging methodology, a NiCd or a NiMH battery can withstand more than 500 recharging cycles (typically 1000 cycles) before being disposed off.
The basic charging process consists in returning to the battery the electrons that were delivered during the discharge.
In all the SGS-THOMSON battery chargers, the electrons are returned as a constant DC current of proper polarity and magnitude.
While it could be desirable to reduce the time to completely recharge a battery by increasing the magnitude of the charging DC current, it must be clearly understood that the maximum charge rate is normally specified by the manufacturer for every specific battery type.
Four different charge rates (expressed in terms of C) are defined in industry as shown in the Table 1.

METHOD OF CHARGING	CHARGE RATE
Trickle	0.01 C to 0.02 C
Standard	0.05 C to 0.1 C
Quick	0.2 C to 0.33 C
Fast & Ultra Fast	1 C to 4 C

The C rate is the charging current in Amperes numerically equivalent to the capacity given in Ah. For example, a battery with a capacity C=1.2 Ah is charged at 1C if the charging current is1,2 A.
The variety of different battery types (standard, quick, fast and each one with a different capacity C), the variety of available energy for charge (DC or AC), the variety of mechanical constraints and the variety of economical considerations do not allow the conception of a unique, universal and economic battery charger to be used under all the circumstances.
Therefore SGS-THOMSON has developed a product strategy by a differentiated approach specific for each type of battery pack and for each customer.
However SGS-THOMSON battery chargers share some common features as outlined in the following:

- fast charge by a constant current to allow a perfect control of the current level.
- constant current generation by a switch mode approach to allow very high efficiency i.e. reduction of power dissipation and waste.
- constant monitoring of charge status by microprocessors to allow the shortest charging time without reaching hazardous conditions of overcharge and so ensuring several hundreds recharge cycles.
- common software algorithm for NiCd and NiMH batteries to allow freedom to the user in the adoption of battery types.
- continuous display of charge status by LEDs driven directly by microprocessors.
- back up protection by timers to stop the fast charge even under anomalous conditions.
- possibility to use the electronic system even when its battery is under charge.
- stop of fast charge when the battery temperature is outside the allowed range (T_{batt} <0°C or T_{batt} >50°C)
- charging current level adjusted according to the battery temperature (trickle mode is imposed if 0 ° < T_{batt} < 10 ° C or 40 ° C < T_{batt} < 50 ° C).
- sensing of the battery presence (if the battery is not connected to the charger, the output voltage of the charger is automatically switched off).
- sensing of one or more default cells inside the battery pack (if this condition occurs the charger is switched off and the condition is signaled by LED status).
- sensing of the maximum battery voltage to stop the charge in case of anomalous conditions
- initial trickle charge followed by fast charge in case of deeply discharged batteries
- minimum current drain (less than 100 µA) in case the charger is left connected to the battery even when it is not used.

The a.m. features are performed by continuous monitoring of battery absolute voltage and battery voltage variation in time, of battery absolute temperature and battery temperature variation in time, of elapsed time.
Depending on the type of available power source and on the application, the SGS- THOMSON battery chargers can be grouped into four different categories:

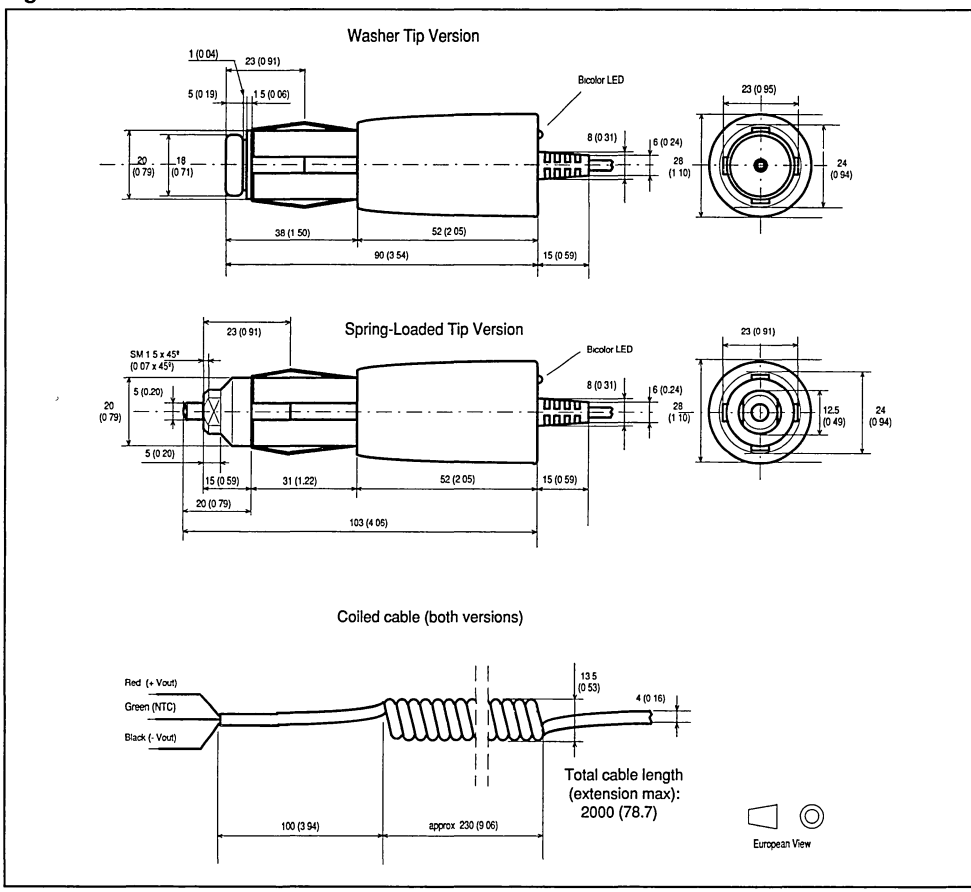
- in-car battery chargers (cigar lighter types): **GSCC-8.507BC**
- wall-mount battery chargers (for mains plug) : **GSAC-8.507AC**
- desk top battery chargers
- in car battery chargers with hands free operation (cradle types).

4.1 IN-CAR BATTERY CHARGERS (GSCC-8.507BC).

These chargers can be used in a car when the battery pack consists of no more than 6 cells (either NiCd or NiMH).

They are assembled into a cigar lighter package as shown in fig 5.

Figure 5.



The package has been particularly designed to avoid mechanical interferences with other mechanical part of a car when the charger is inserted into the car cigar lighter plug.

All the used materials are non flammable and UL recognized.

A dual color LED is used to display different charge status or anomalous battery conditions by continuous or flashing green and red colors or both off so that five different messages can be sent to the user. ST can assist the customer in assigning the proper color (green or red) and condition (continuous or flashing or off) according to different battery status. For optimum charger performance, customers should specify the NTC type. These cigar lighter types retain all the feature common to ST battery chargers.

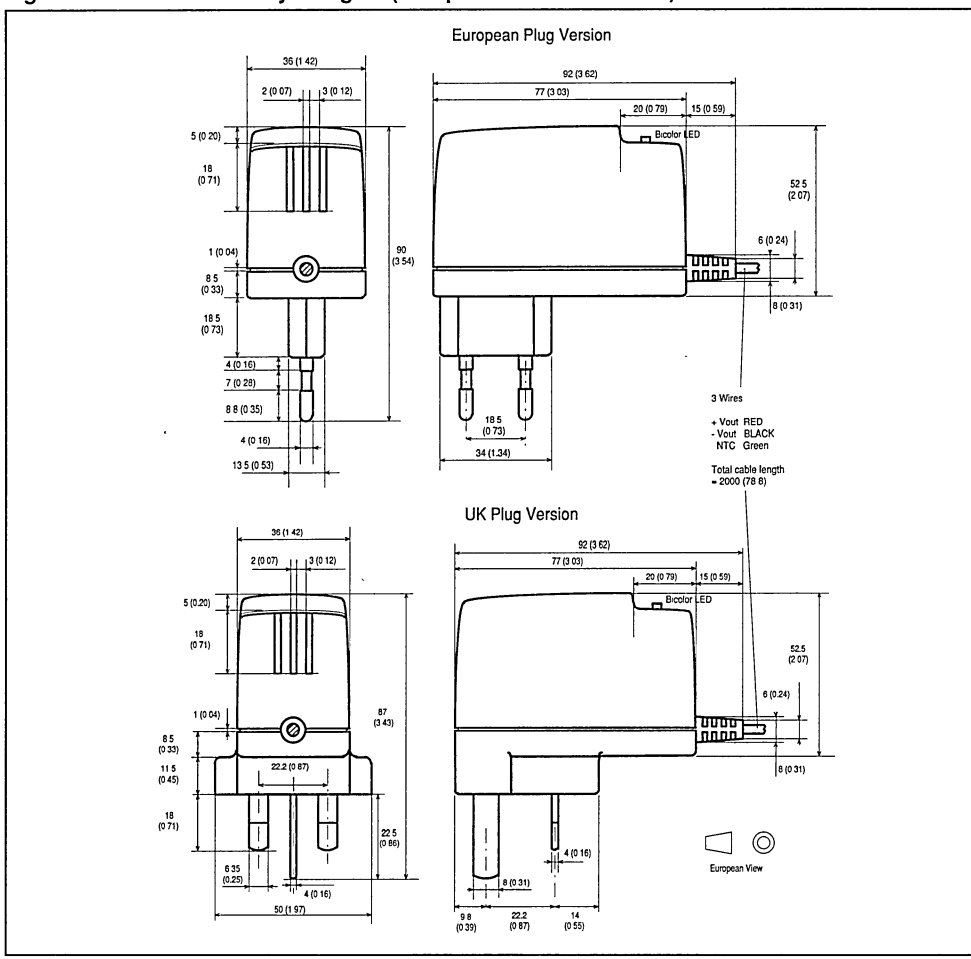
This charger can deliver a maxim charge current of 1A. The actual value depends on the battery charge status and temperature. Trickle charge is normally 5% of the maximum fast charge current.

4.2 WALL MOUNT BATTERY CHARGERS (GSAC-8.507BC).

These chargers can be used when the available energy source is the mains.

Thanks to the adoption of a switch mode technology, these chargers are housed in a small and light package as shown in fig 6.

Figure 6. Wall-Mount battery chargers (European and UK Versions).



The American and the Australian version of the input plug will be available in 1994.
A dual color LED is used to display different charge status or anomaly battery conditions by continuous or flashing green and red colors or both off so that five different messages can be sent to the user.

ST can assist the customer in assigning the proper color (GREEN or RED) and condition (continuous or flashing) according to different battery status. For optimum charger performance, customers should specify the NTC type. The wall-mount types retain all the feature common to ST battery chargers.

4.3 DESKTOP BATTERY CHARGERS FOR HANDHELD PHONES.

SGS-THOMSON design and manufacture many types of desktop battery chargers for handheld phones application. These chargers are designed under contracts for specific customers because no standardization exists for this type of application.
These contracts are covered by NON DISCLOSURE AGREEMENTS so that no mechanical information can be provided.
Nevertheless the following information can be provided here.
Mechanically the Desk top chargers are divided into two groups:

- Single slot desk top chargers. The phone is inserted inside this slot. Electrically the phone may be in OFF status, stand by or receiving mode. If the status of the phone is available on one or more phone pins, the desk top charger can accommodate the charging current to supply the additional current requested by the phone without affecting the charging time for the battery.
  Upon request ST can provide an additional feature to allow the charge of the battery and an additional power supply for the phone regardless of its status (OFF, stand-by, receiving or transmitting mode). ST Patent.
- Dual slot desk top chargers.
  In these type of chargers the front slot is normally used to charge the battery that is directly connected to the phone while the rear slots is used to charge a spare battery pack.
  ST can offer versions for simultaneous charging of the two battery packs or for sequential charging: in this last case the charging priority is assigned to the front slot.
  In all the cases, ST use separate current generation and overcharge detection by microprocessors for each slot.

The ST Desk Top chargers are normally powered by an external power supply: depending on the total power available by this external supply, the simultaneous or sequential charge can be adopted.

For simultaneous charge with a maximum current of 1 A per slot, ST can provide the relevant external off line power supply.

Alternatively ST may consider the inclusion of an AC-DC switch mode power supply inside the Desk top charger.

As said previously, ST can deliver an AC-DC off-line power supply to be used in combination with dual or single slot desk top chargers.

This off-line power supply is assembled into a wall mount package. See GS20AC-12 data sheet.

DESK TOP CHARGERS (SINGLE OR DUAL SLOT)

ELECTRICAL CHARACTERISTICS (Tamb=25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit	Note
V_i	Input Voltage	V_O = 0 to max I_O = 0 to max	12		22	V	1
V_O	Output Voltage	Determined by number of cells	0		9.8	V	2
I_O	Output Current per slot	V_i = 12 to 22 V	0		1	A	3
η	Efficiency	V_i = 12 V I_O = 0.7 A per slot		75		%	
f_S	Switching frequency	V_i = 12 V to 22 V any value for V_O and I_O		100		kHz	4
Top	Operating Ambient Temperature		0		35	°C	

Note 1: The wide input voltage range allows the use of an unregulated external power supply.

Note 2: The output voltage depends on the number of cells in the battery pack and on the battery charge status. The reported maximum value is for a 6 cell battery pack.

Note 3: The reported value (1 A) is the maximum charging current for a battery pack of 6 cell. For a higher number of cells, the max charging current must be scaled down accordingly. The real value of fast charge current depends on the actual type of battery. Trickle charge current is normally 5% of the maximum fast charge current.

Note 4: For the dual slot version, the switching frequency is synchronized for the two slots to avoid frequency beats and interference.

4.4 IN CAR BATTERY CHARGERS WITH HANDS FREE OPERATION FOR HAND HELD PHONES (CRADLE TYPES).

SGS-THOMSON design and manufacture cradle type battery chargers for in car hands free operation.
These products are so peculiar in their application (battery charge is just one of the several function performed) that no general description can be provided here.
Nevertheless it is worth to mention that the battery charge is performed along the same feature already described.
Even if ST use a switch mode approach for constant current generation, no interference is induced on the phone (radiated or conducted noise).

5. CONCLUSION

The range of ST products devoted to battery charge is very broad and each product is designed specifically according to customer requests.
This note is intended as a general description of these products to outlight some specific (and in many case unique) feature of ST chargers.
In this domain, the best results are obtained by a close cooperation between ST and the customers and ST is available to customize any type of application for any type of battery.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

L3235 WITH EXTERNAL RINGING

by L. Vergani, W Rossi

This application note shows an easy way, adding few external components, to adapt the L3235 SLIC to operate together with electromechanical ringing relay and to perform RING/TRIP function.

INTRODUCTION

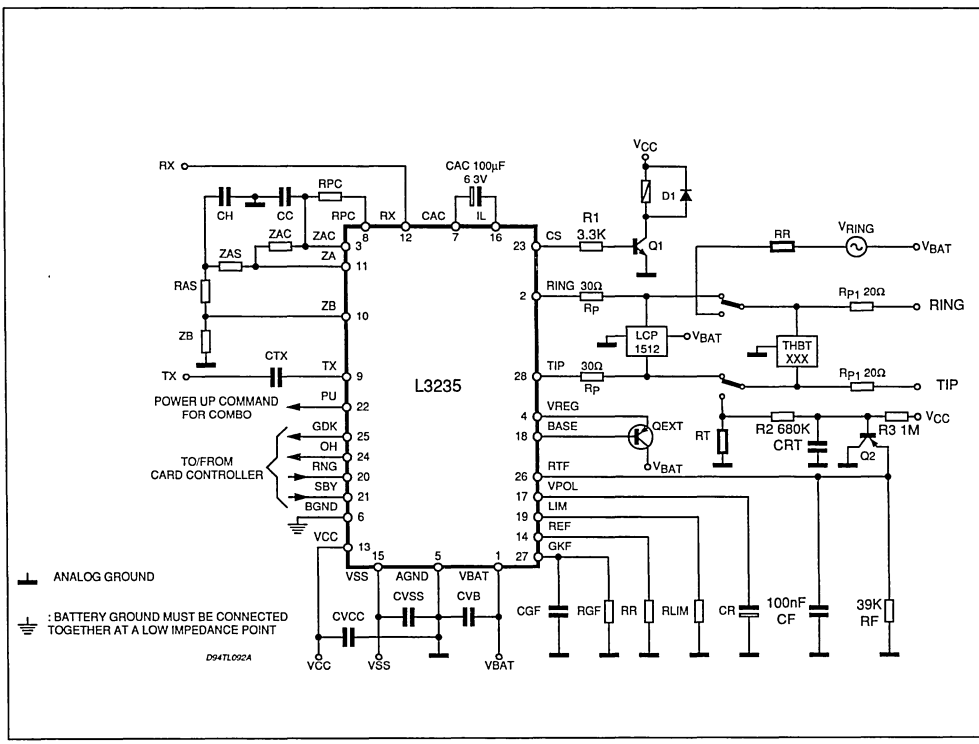
The SGS-THOMSON SLIC kit L3234/L3235 designed for PABX application and providing also the ringing generation function (L3234), can be easily used also in system where a standard ringing generator is already present and there are difficulties in providing the 100V positive supply for the L3234 ringing injector.

CIRCUIT IMPLEMENTATION

Here below you can find a detailed description of the RING TRIP circuitry behavior and its dimensioning.

For all other characteristics like DC, AC performance, voice path, control interface and other details, the application is the same as the L3234/L3235 KIT therefore please refer to the L3234/L3235 datasheet for more informations.

Figure 1.



The different operating modes of the L3235 can be programmed through the digital interface based on two input pins SBY and RNG.

When ringing mode is selected, through RNG and SBY control pins, the L3235 set CS pin to 1 activating, the relay, with 1mA base current into Q1 (max. CS current).

In this condition the relay is activated and the ringing signal is connected to the line through RR and terminated to GND by RT resistor.

Dimensioning opportunely the resistors R2 and R3 and the capacitor CRT, connected to the base of the transistor Q2, it is possible to fix a DC level that will keep the transistor T2 in OFF condition when no DC current is flowing into the line (telephone in ON-HOOK condition).

When the phone goes OFF-HOOK the negative voltage across ringing resistor force rapidly in conduction the transistor connected to the RTF pin, producing an OFF-HOOK DETECTION.

Once OFF-HOOK is detected, the CS pin is automatically driven low by L3235, disconnecting the ring relay and therefore performing an AUTO RING TRIP function.

The key component for good Ring Trip performances is the CRT capacitor.

It must have a proper value to reduce the ringing signal that appears on the resistor RT and therefore on the base of Q2.

In particular it is important to avoid that the ripple on the Q2 base produces an false Ring Trip detection when an high ringing signal is used (90Vrms) and five phone are connected in parallel (5REN) with 0Ω line resistor and in particular when the value of RR and RT is 400Ω (2X400).

These are the worst condition that can produce an high ripple level on Q2 base, this effect can be prevented choosing an high value CRT.

At the same time this capacitor can't have a too high value otherwise the Ring Trip Detection Time will be too long in particular for long loops.

In this application the CRT capacitor has been optimized in order to keep the Ring Trip Time always lower than 100ms even with line resistor greater than 2KΩ.

The components value shown in fig.1 have been chosen in order to obtain the best compromise with the constraints above explaned.

In the table below it is possible to observe the minimum value that the capacitor CRT must assume versus frequency for different RR/RT resistor and VRING up to 90Vrms.

	16Hz	25Hz	40Hz	50Hz	68Hz	RR/RT
CRT≥	270nF	220nF	170nF	150nF	150nF	2x400
CRT≥	150nF	150nF	120nF	100nF	82nF	2x200

SUPPORT TOOLS LIST

PRCD DEMONSTRATION BOARD

PRCD demo-board is a conversational demonstration and evaluation tool for the ST5432 PRCD chip produced by SGS-THOMSON Microelectronics. The board includes:

- 2 ST5432 PRCD device
- 4 ST5451 HDLC controllers for protocol handling.

The line interface of each PRCD can be connected to two copper twisted pairs, one in transmit direction the other in receive direction. The Digital interface of the PRCDs can be connected to a test equipment, like BER measurement equipment.

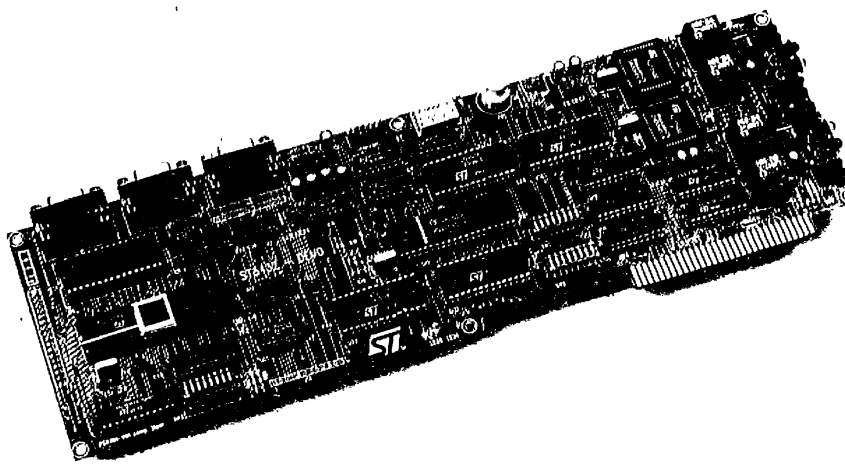
Digital and analog loops on board allow full functional transmissions and tests.

The user interface with the board is performed by an IBM personal computer or compatible. The connection with the PC can be done in two ways:

- Serial link. In this case the board is controlled through a serial port of the PC, using a RS232 cable.
- Plug-in. The board is inserted in an expansion slot of the PC. In this case you can perform file transfer between two PCs using two PRCD demo-boards connected through twisted pair cables.

An interactive software inputs the commands from the user and displays results on the screen. A multi-level menu approach is used, to make easy the programming of the PRCD demo-board.

Order code: PRCDDEMO



PAIR-GAIN DEMONSTRATION SYSTEM

PAIR-GAIN SYSTEM (order code: PGAINDEMO) is a demo-tool developed by SGS-THOMSON Microelectronics basically for demonstration of functionality and performances of a complete pair gain system based on SGS-THOMSON products.

The system is an ISDN application that links N.2 subscribers to C.O. through a single twisted pair. An A/D and D/A conversion is done, at C.O. and Subscribers ends, on the signal transmitted and received respectively.
The two 64KB/s B channels and the 16KB/s D channel of ISDN link provide two fully transparent telephone lines: B channels for phonic signal and D channel for signaling (ON/OFF-OOK, RINGING, RING-TRIP, TELE-TAX).

Analog>PCM and PCM>Analog conversions are performed by TS5070 Combos, whereas PCM>2B1Q and 2B1Q>PCM conversions are done by ST5410 U-Interface.

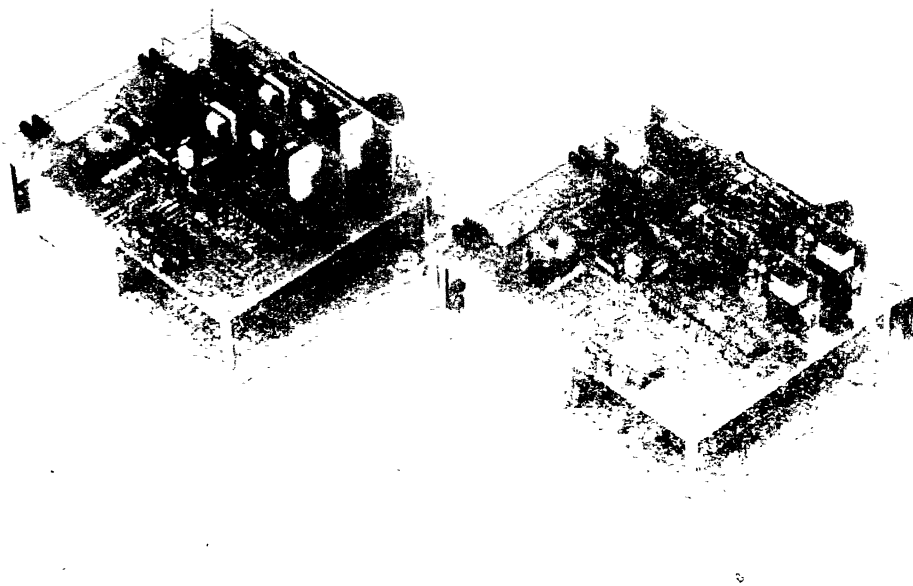
Analog-Trunks using L3845 Trunk Interface and L3036 Slics are the analog interfaces to C.O. and Subscribers respectively.

The control of the system is done by ST90E26.

Pair gain system is composed by two sets of boards:

Line Terminal (L.T.) set:
- U-Interface and Control board.
- N.2 Analog Trunk and COMBOII modules.
- Power Supply Board.

Network Terminal (N.T.) set:
- U-Interface and control board.
- N.2 Slic and COMBOII modules.
- Power Supply Board, including Ringing and Tele-Tax signaling.



NETWORKS DEMONSTRATION BOARD

The NETWORKS demonstration board is a conversational demonstration and evaluation tool for the networks oriented circuits developed by SGS-THOMSON Microelectronics.

The mother-board includes:

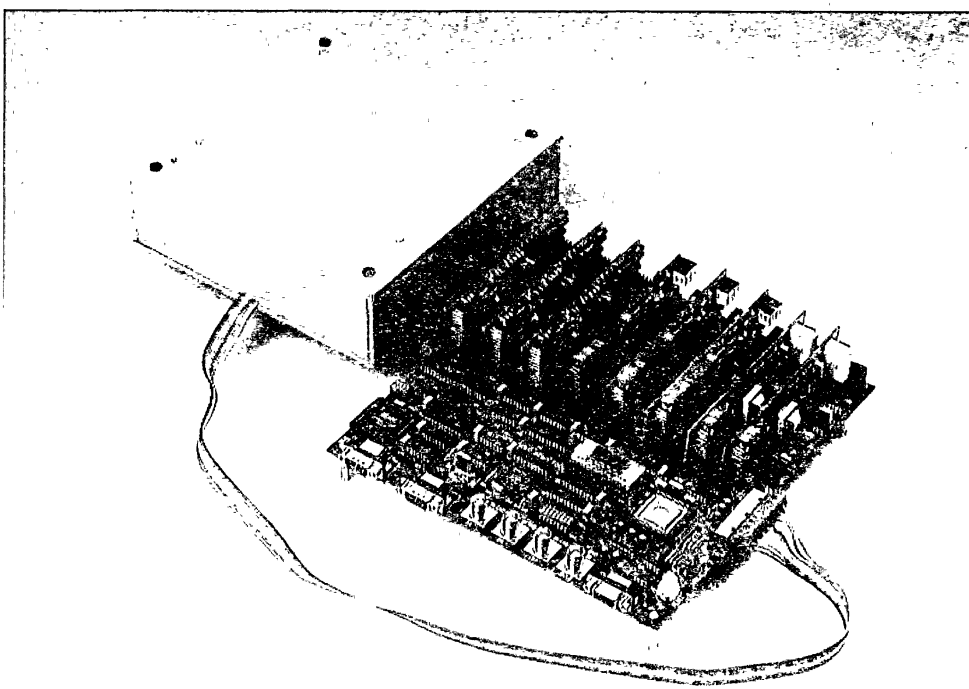
- M3488 Digital Switching Matrix chip.
- M34116 PCM Conference Call and Tone Generator chip.
- Two slots for insertion of L3845 Analog Trunk modules.
- Six slots for insertion of complete transmission modules, each of them made of a programmable codec/filter COMBOII associated with a full silicon SLIC to achieve the "BORSCHT" function.

The 2-wire interface of each SLIC can be connected to a telephone set or to an appropriate test equipment. The PCM interface of the COMBOs can be connected to a PCM test equipment. The on board M3488 DSM can perform channel connections, thus allowing real phone conversations between two telephone sets through the corrisponding SLICs.

The user interface with the board is performed by an IBM personal computer or compatible. An interactive software inputs the commands from the user and displays results on the screen. A multilevel menu approach is used, to make easy the programming of the NETWORKS board.

Three operating modes can be selected:

- Stand-alone. The board works as a PABX without PC interface for quick demonstrations.
- Demo PABX. Computer show of a running PABX system, reporting the current status on



the PC screen. Basic PABX setting can be modified via PC

- Debug mode. Via PC control each individual register of all devices can be accessed.

Different configurations of the board are available. In addition a dedicated power supply (110V or 220V option) will be included.

Order code: NETWDEMO / X / nnn

X specifies the type of modules present on the mother board:

X=A: 2 Analog Trunk + 6 L3092/L3000N Integrated Ringing SLIC

X=B: 2 Analog Trunk + 6 L3037 Monochip SLIC

X=C: 2 Analog Trunk + 3 L3037 Monochip SLIC
3 L3092/L3000N Integrated Ringing SLIC

X=D: Mother-board only. (no modules provided)

nnn=110: 110V Power Supply

nnn=220: 220V Power Supply

Example:

In order to get one NETWORKS demonstration board fully equipped with L3037 modules and power supply for 220V MAIN, the order code should be: NETWDEMO/B/220.

Additional SLIC and AT modules can be ordered apart:

L3092/L3000N SLIC	order code: L3092EVAL
L3035 SLIC	order code: L3035EVAL
L3036 SLIC	order code: L3036EVAL
L3037 SLIC	order code: L3037EVAL
L3845 A.T.	order code: L3845EVAL

SLIC EVALUATION KIT

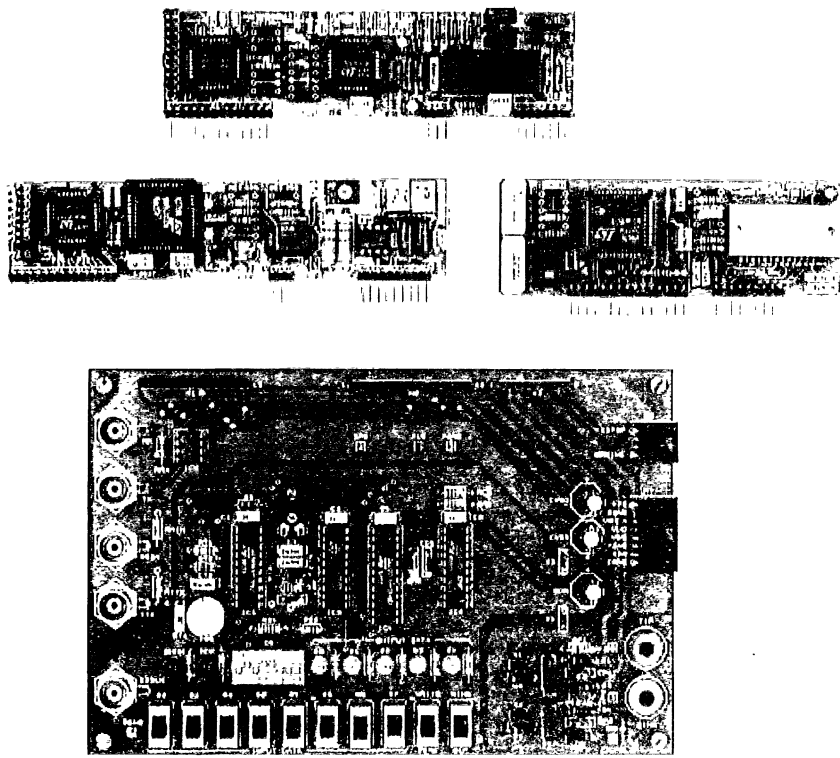
This evaluation kit is arranged to make easier bench analysis and measurements on SGS-THOMSON Microelectronics SLICs.

A MOTHER BOARD provides the control and the connections to external instruments. The basic version (order code SLICDEMOBOARD) supports L3035/6/7 Single Chip Slic and L3000N/L3092 Slic Kit.

The version with Serial Control Interface (order code SLICDEMOB3030), in addition to the a.m. Slics, supports the L3000N/L3030 Slic Kit as well.

The SLIC MODULES today available are:

L3000N/L3030	order code: L3030EVAL
L3000N/L3092	order code: L3092EVAL
L3035	order code: L3035EVAL
L3036	order code: L3036EVAL
L3037	order code: L3037EVAL
L3234/L3235	order code: L3235EVAL



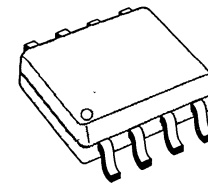
PACKAGES

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

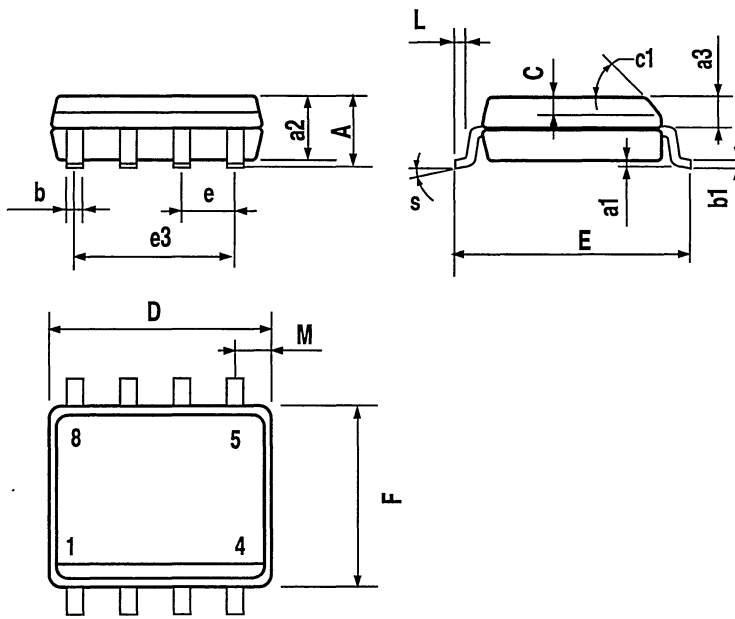
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA

Weight: 0.10gr



SO8



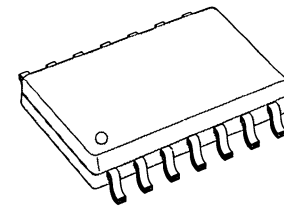
0016023

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.009
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45 (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.68			0.027
S	8 (max.)					

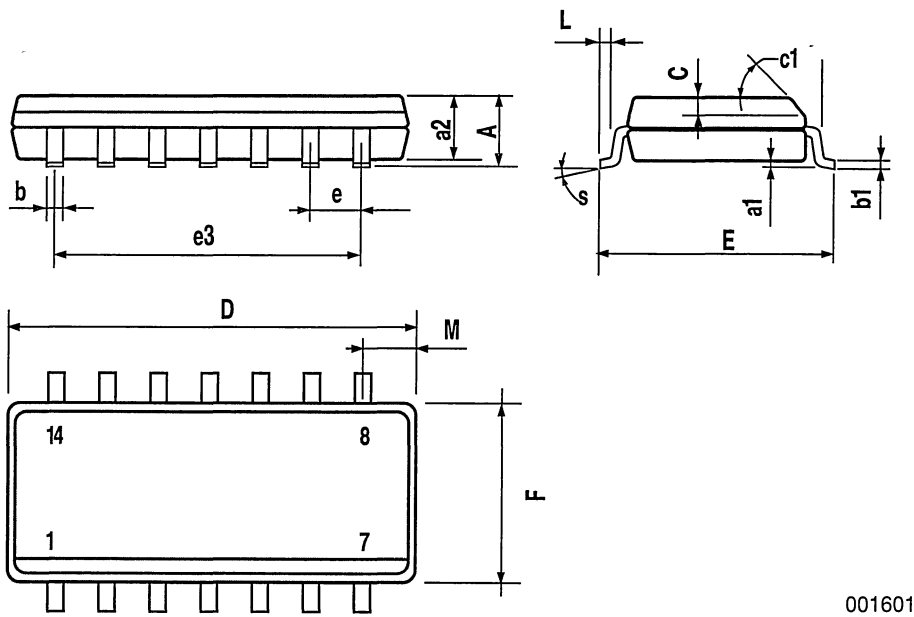
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA

Weight: 0.10gr



SO14



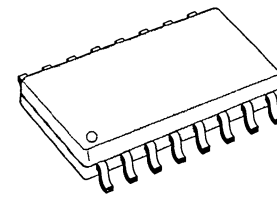
0016019

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	10.1		10.5	0.398		0.413
E	10.0		10.65	0.394		0.419
e		1.27			0.050	
e3		8.89			0.350	
F	7.4		7.6	0.291		0.299
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8° (max.)					

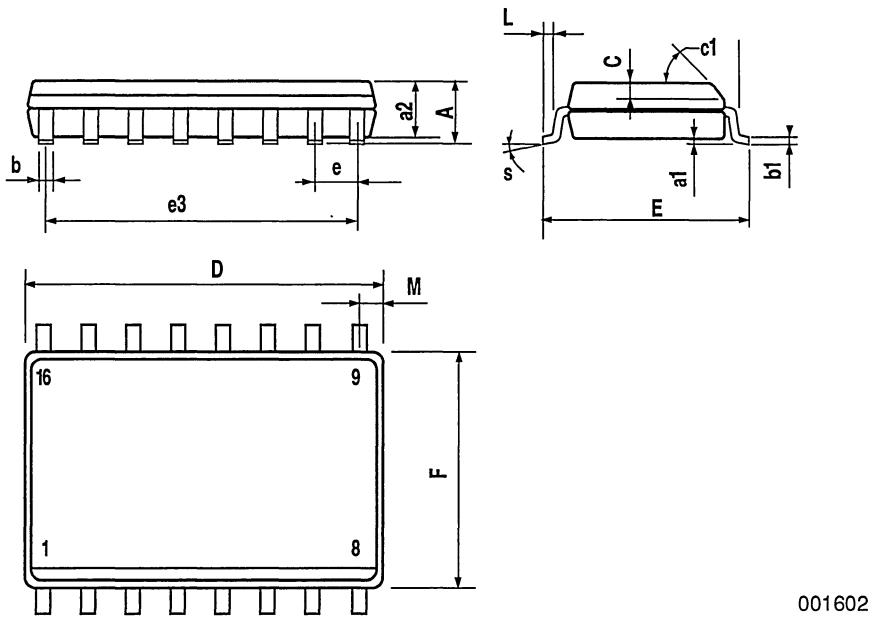
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA

Weight: 0.40gr



SO16 Wide



0016021

SO20L PACKAGE MECHANICAL DATA

DIM.	mm			inch		
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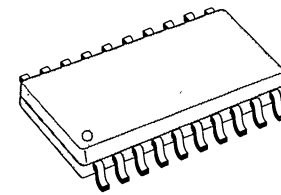
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	12.6		13.0	0.496		0.512
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.299
L	0.5		1.27	0.020		0.050
M			0.75			0.030

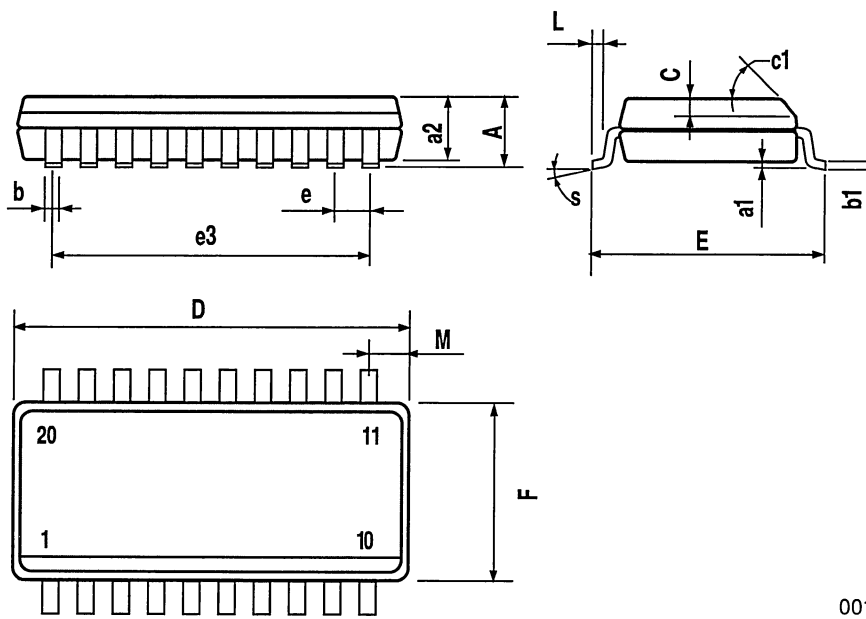
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA

Weight: 0.50gr



SO20



0016022

DIM.	mm			inch		
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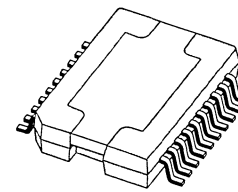
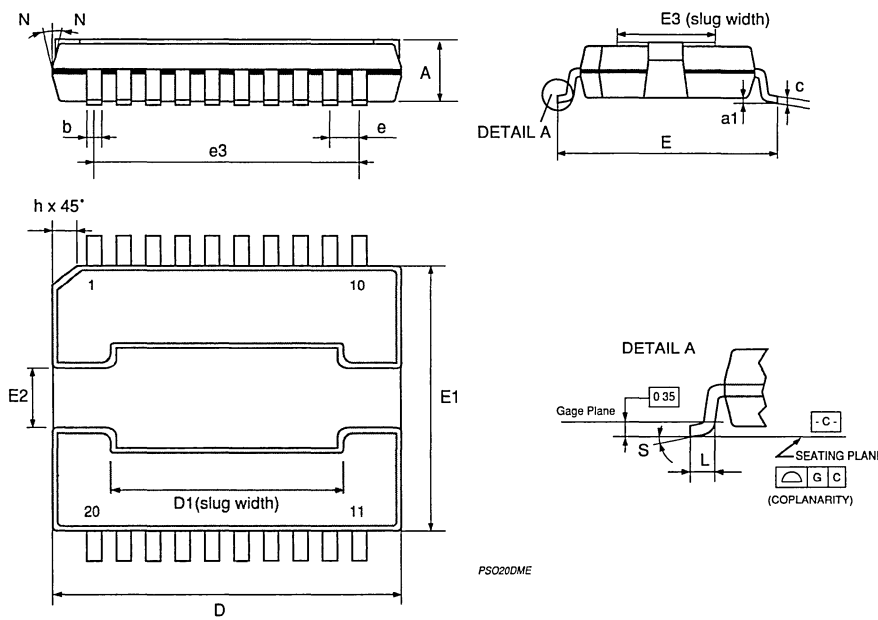
A			3.70			0.145
a1	0		0.25	0		0.01
b	0.40		0.53	0.016		0.021
c	0.23		0.32	0.009		0.012
D	15.80		16.00	0.622		0.63
D1	9.4		9.80	0.37		0.385
E	13.90		14.50	0.547		0.57
e		1.27			0.05	
e3		11.43			0.45	
E1	10.90		11.10	0.429		0.437
E2			2.90			0.114
E3	5.80		6.20	0.228		0.244
G	0		0.10	0		0.004
h			1.10			0.043
L	0.80		1.10	0.031		0.043
N	10° (Max.)					
S	8° (Max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



PowerSO-20 (Slug-up)



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA

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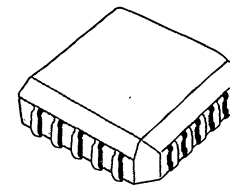
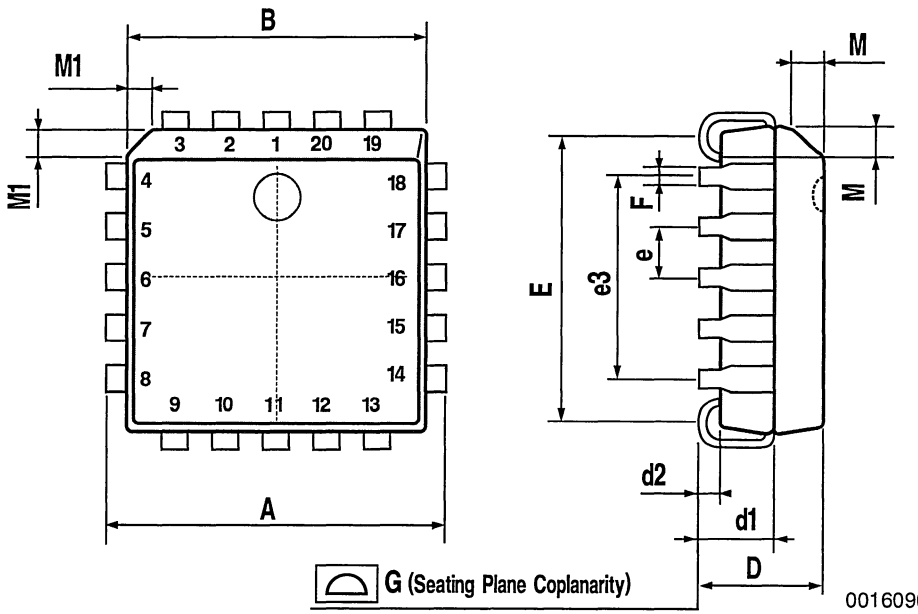


PLCC20

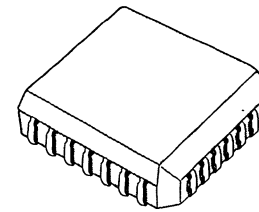


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	12.32		12.57	0.485		0.495
B	11.43		11.58	0.450		0.456
D	4.2		4.57	0.165		0.180
D1	2.29		3.04	0.090		0.120
D2	0.51			0.020		
E	9.91		10.92	0.390		0.430
e		1.27			0.050	
e3		7.62			0.300	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.24			0.049	
M1		1.143			0.045	

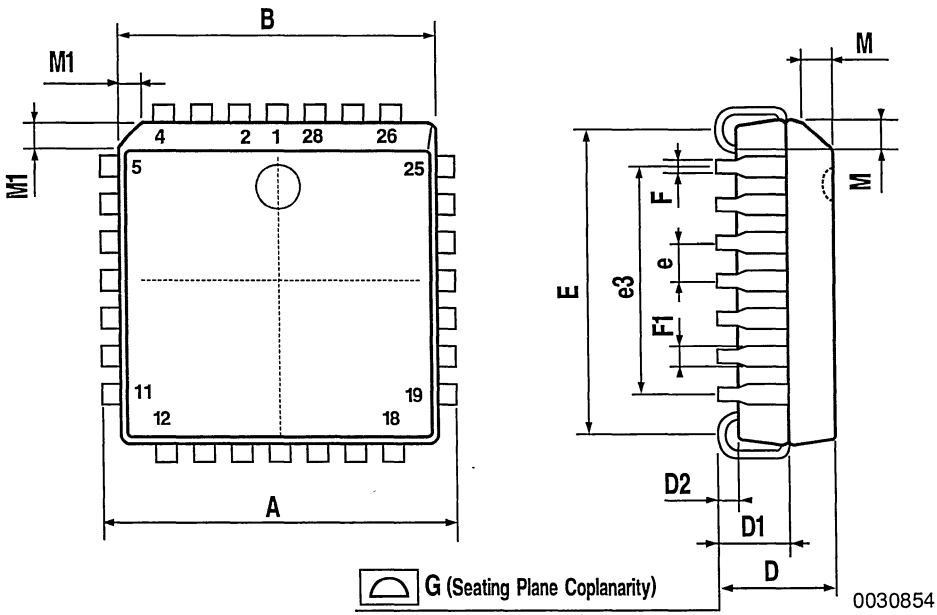
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA

Weight: 1.10gr



PLCC28

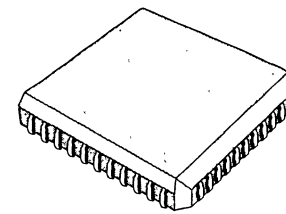


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	17.4		17.65	0.685		0.695
B	16.51		16.65	0.650		0.656
C	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16	0.590		0.630
e		1.27			0.050	
e3		12.7			0.500	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.16			0.046	
M1		1.14			0.045	

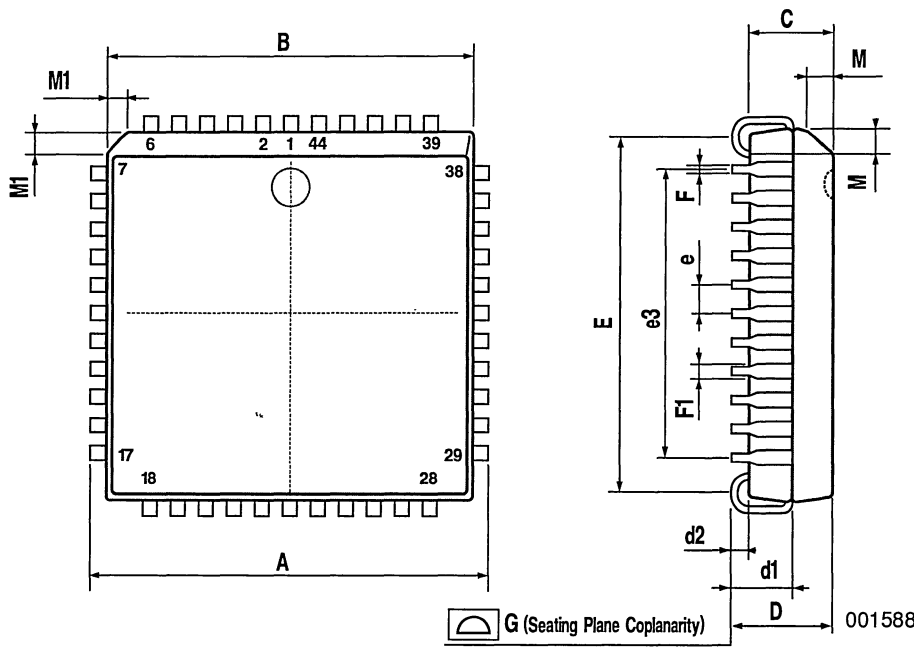
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA

Weight: 2.30gr



PLCC44

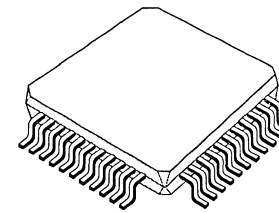


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.45			0.096
A1	0.25			0.010		
A2	1.95	2.00	2.10	0.077	0.079	0.083
B	0.30		0.45	0.012		0.018
c	0.13		0.23	0.005		0.009
D	12.95	13.20	13.45	0.51	0.52	0.53
D1	9.90	10.00	10.10	0.390	0.394	0.398
D3		8.00			0.315	
e		0.80			0.031	
E	12.95	13.20	13.45	0.510	0.520	0.530
E1	9.90	10.00	10.10	0.390	0.394	0.398
E3		8.00			0.315	
L	0.65	0.80	0.95	0.026	0.031	0.037
L1		1.60			0.063	
K	0°(min.), 7°(max.)					

SGS-THOMSON MICROELECTRONICS

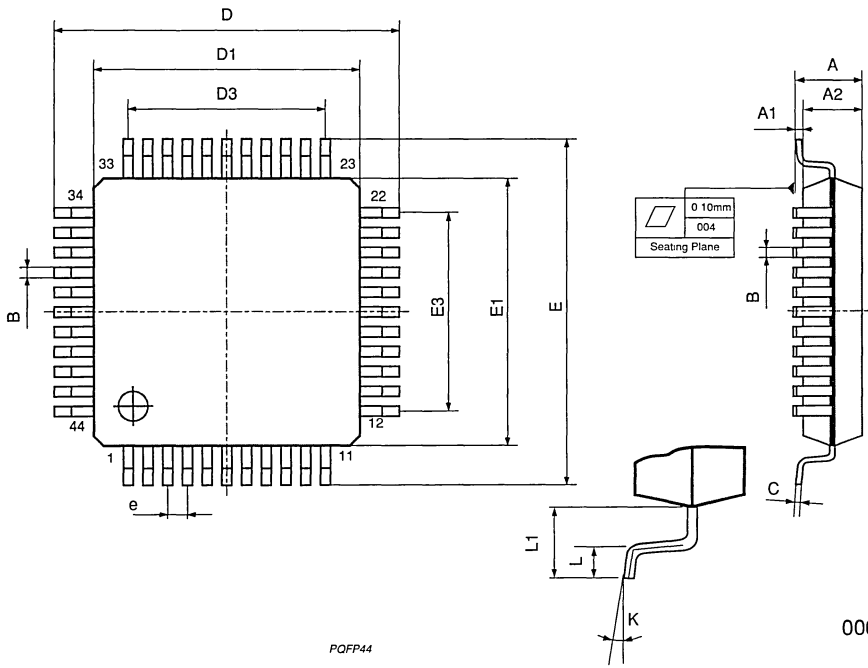
OUTLINE AND MECHANICAL DATA

Weight: 0.50gr



Body: 10 x 10 x 2.00mm

PQFP44 (10 x 10)

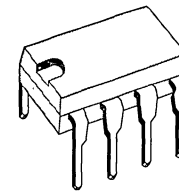


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

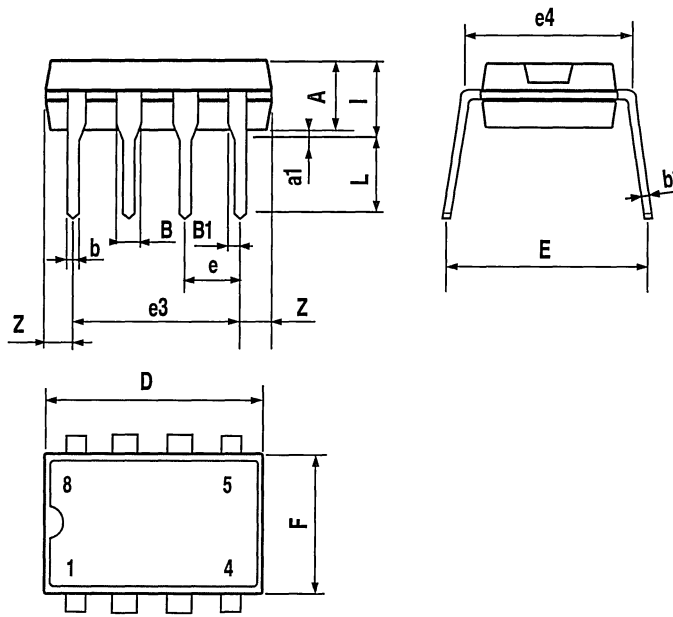
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA

Weight: 0.50gr



Minidip (0.300")



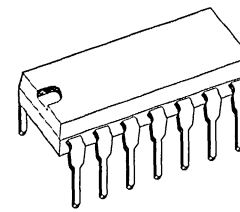
0037880

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

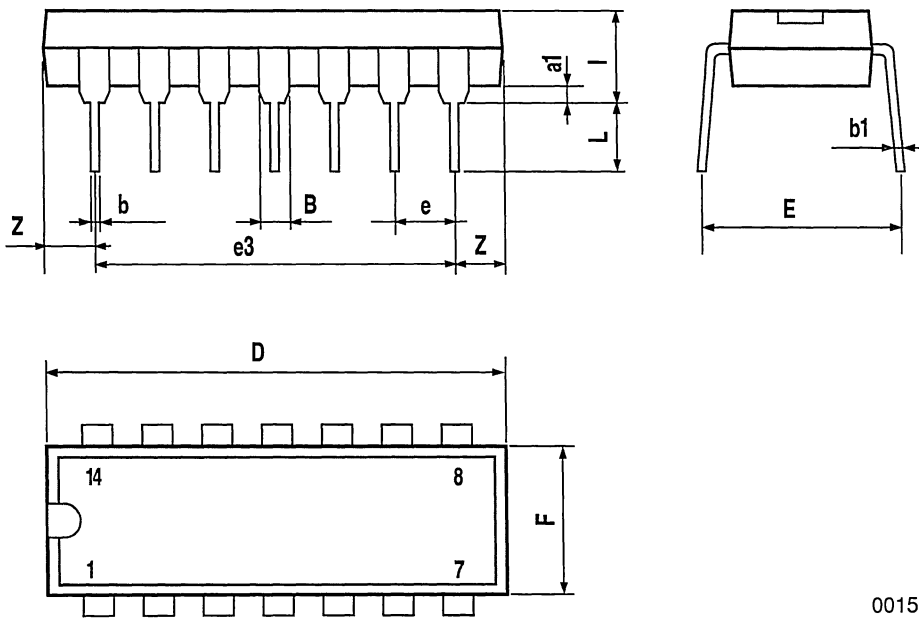
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA

Weight: 1.00gr



DIP14 (0.300")



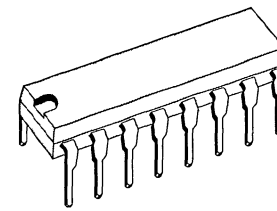
0015893

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

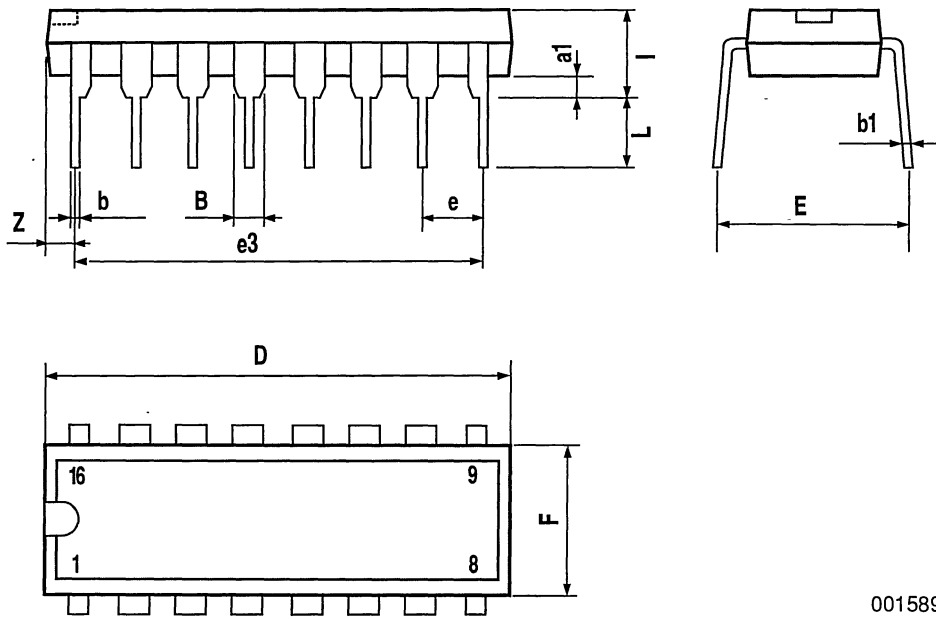
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA

Weight: 1.00gr



DIP16 (0.300")



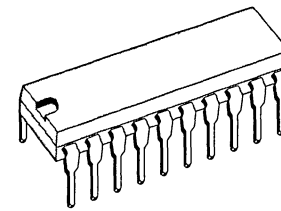
0015895

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053

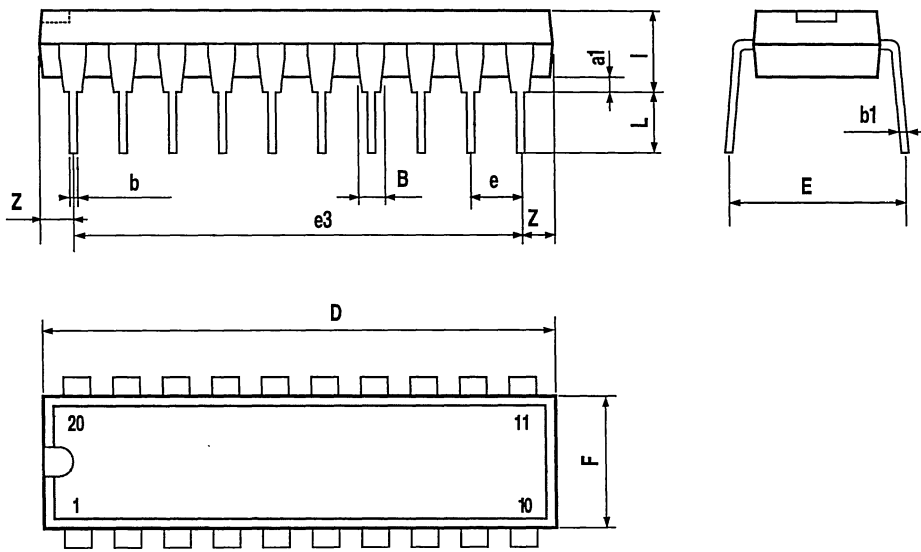
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA

Weight: 1.40gr



DIP20 (0.300")



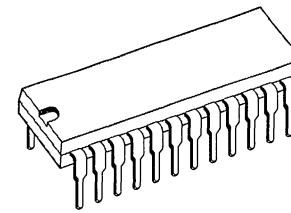
0015902

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			32.2			1.268
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		27.94			1.100	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	

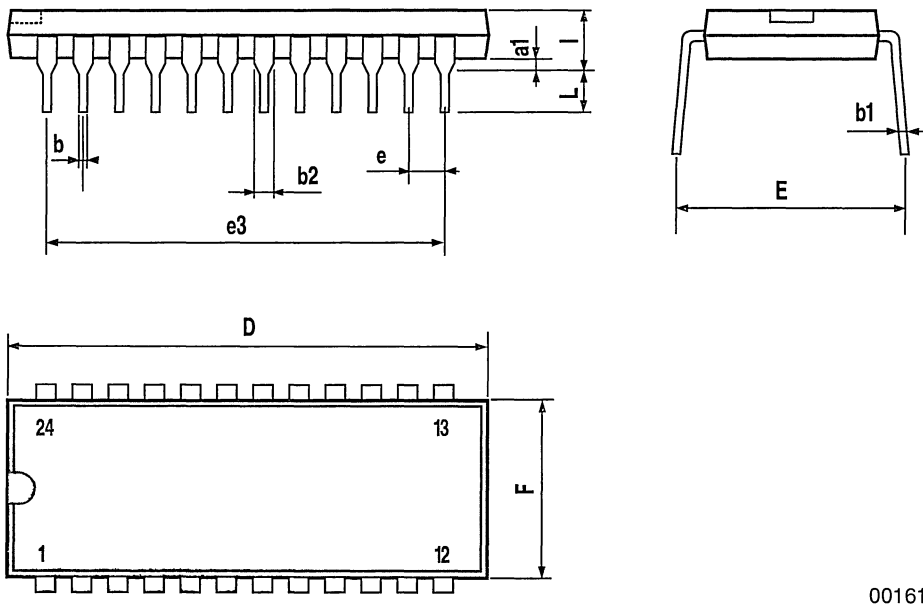
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA

Weight: 3.70gr



DIP24 (0.600")



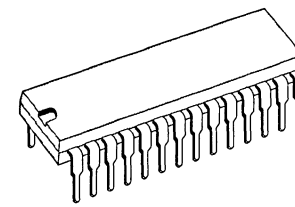
0016128

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			37.34			1.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	

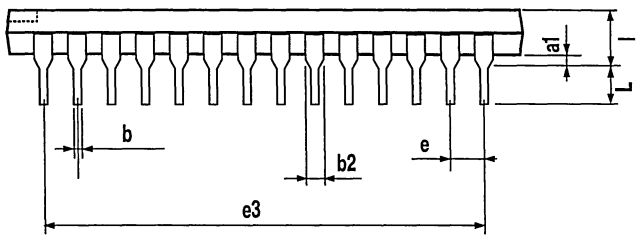
SGS-THOMSON MICROELECTRONICS

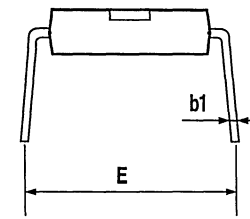
OUTLINE AND MECHANICAL DATA

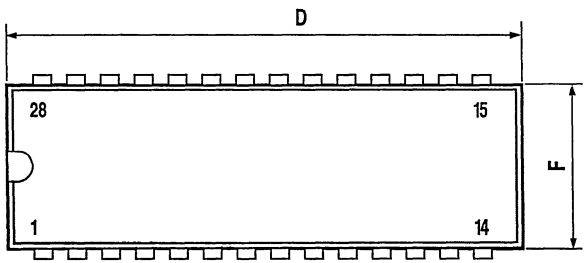
Weight: 4.20gr



DIP28 (0.600")







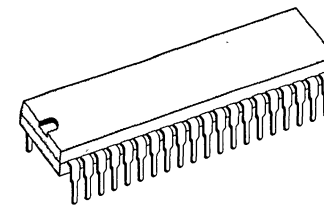
0016130

DIM.	mm			inch		
	MIN	TYP	MAX	MIN	TYP	MAX
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			52.58			2.070
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		48.26			1.900	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	

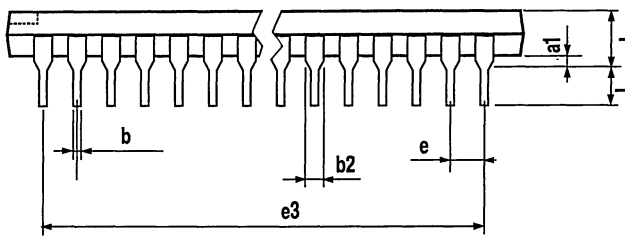
SGS-THOMSON MICROELECTRONICS

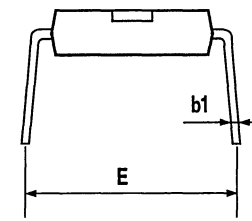
OUTLINE AND MECHANICAL DATA

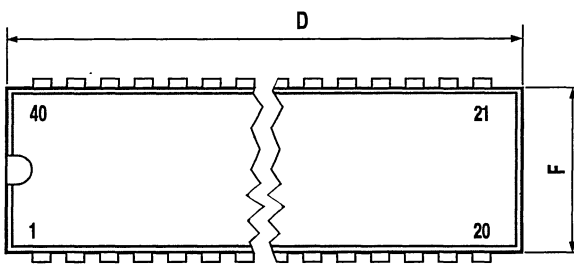
Weight: 6.00gr



DIP40 (0.600")







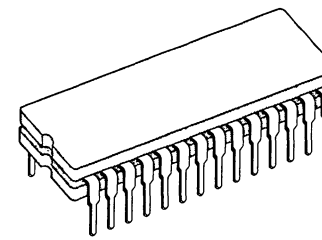
0016131

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			38.1			1.500
B	14.50		14.90	0.571		0.587
C	3.9		5.08	0.154		0.200
D	3.18			0.125		
E	0.5		1.78	0.020		0.070
e3		33.02			1.300	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
I	1.17		1.42	0.046		0.056
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N1	4°(min.), 15°(max.)					
P	15.4		15.8	0.606		0.622
Q			5.71			0.225

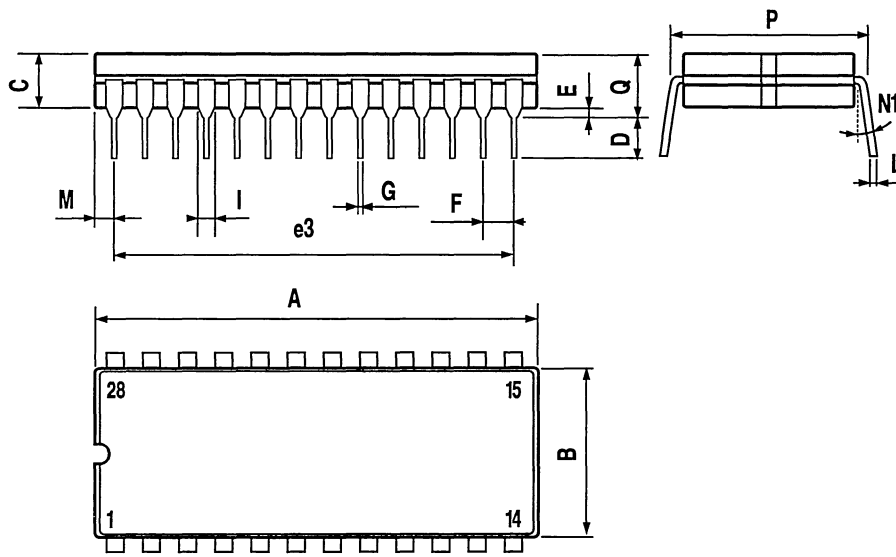
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA

Weight: 8.76gr



Ceramic DIP28 (0.600")

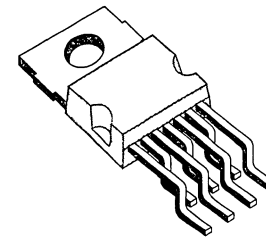


0016166

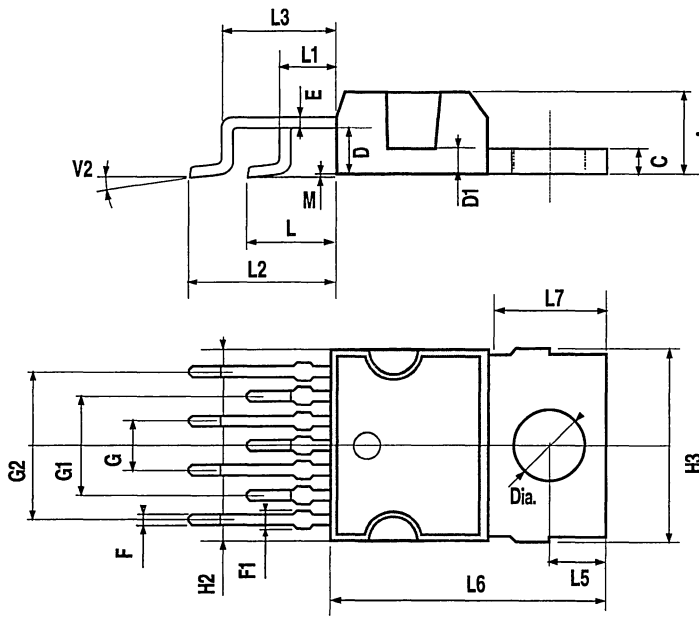
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.6		0.8	0.024		0.031
F1			0.9			0.035
G	2.41	2.54	2.67	0.095	0.100	0.105
G1	4.91	5.08	5.21	0.193	0.200	0.205
G2	7.49	7.62	7.8	0.295	0.300	0.307
H2	9.2		10.4	0.362		0.409
H3	10.05		10.4	0.396		0.409
L	4.6		5.05	0.181		0.198
L1	3.9	4.1	4.3	0.153	0.161	0.170
L2	6.55	6.75	6.95	0.253	0.265	0.273
L3	5.9	6.1	6.3	0.232	0.240	0.248
L5	2.6	2.8	3	0.102	0.110	0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M	0.17		0.32	0.007		0.012
V2	8° (max.)					
Dia	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Heptawatt (Surface Mount)



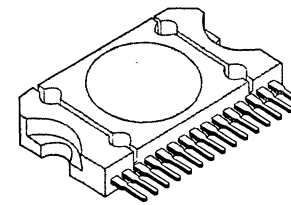
033587

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5.00			0.196
B			1.90			0.074
b1			0.1			0.004
D	4° (typ.)					
E		0.30			0.012	
F		0.90			0.035	
F1			0.57			0.022
G	1.77	1.9	2.03	0.070	0.075	0.080
G1		26.77			1.054	
H1		29.00			1.142	
H2		28.00			1.102	
H3		17.00			0.669	
H4		0.80			0.031	
L	19.05		19.95	0.75		0.785
L1	1.10		1.40	0.043		0.055
L2	2.60		2.90	0.102		0.114
L3	15.35		15.65	0.604		0.616
N1		10			0.394	
N3		6.8			0.268	
N4		3.8			0.15	
Dia1		13.00			0.511	
Dia2		14.00			0.551	
Dia3		2.50			0.098	
Dia4		12.00			0.472	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA

Weight: 4.9gr



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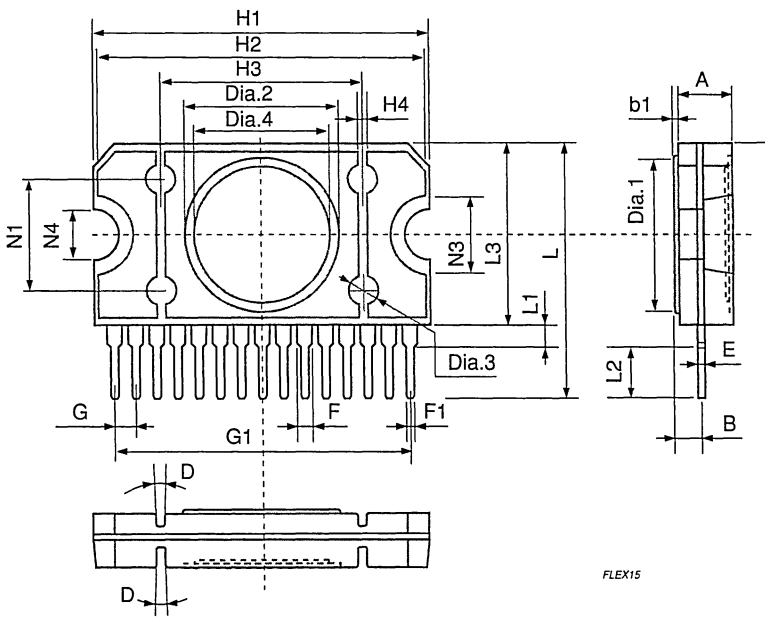

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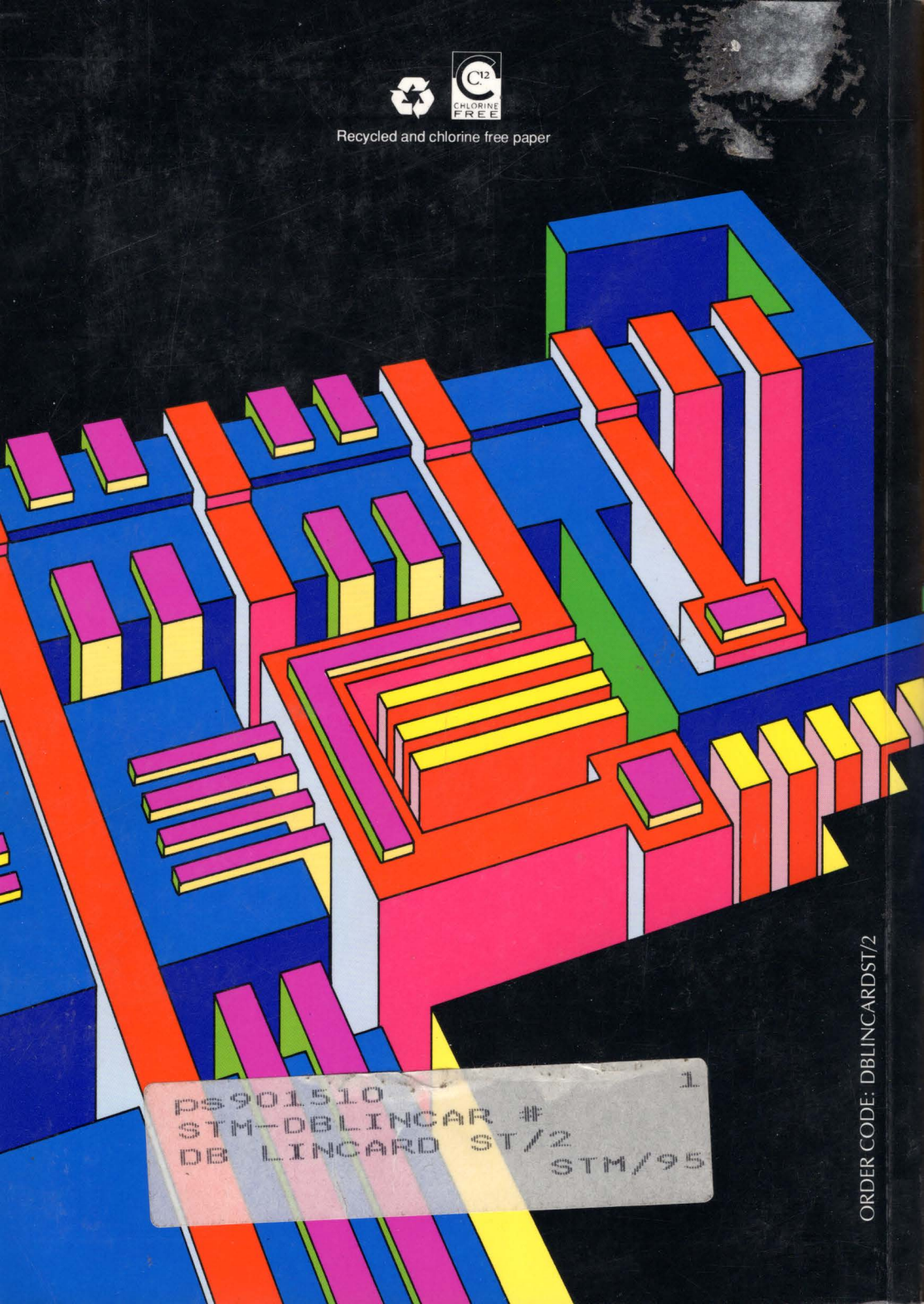
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