SIGNETICS ANALOG
—SPECIFICATIONS
—APPLICATIONS
—MILITARY SUMMARY

DATA MANUAL

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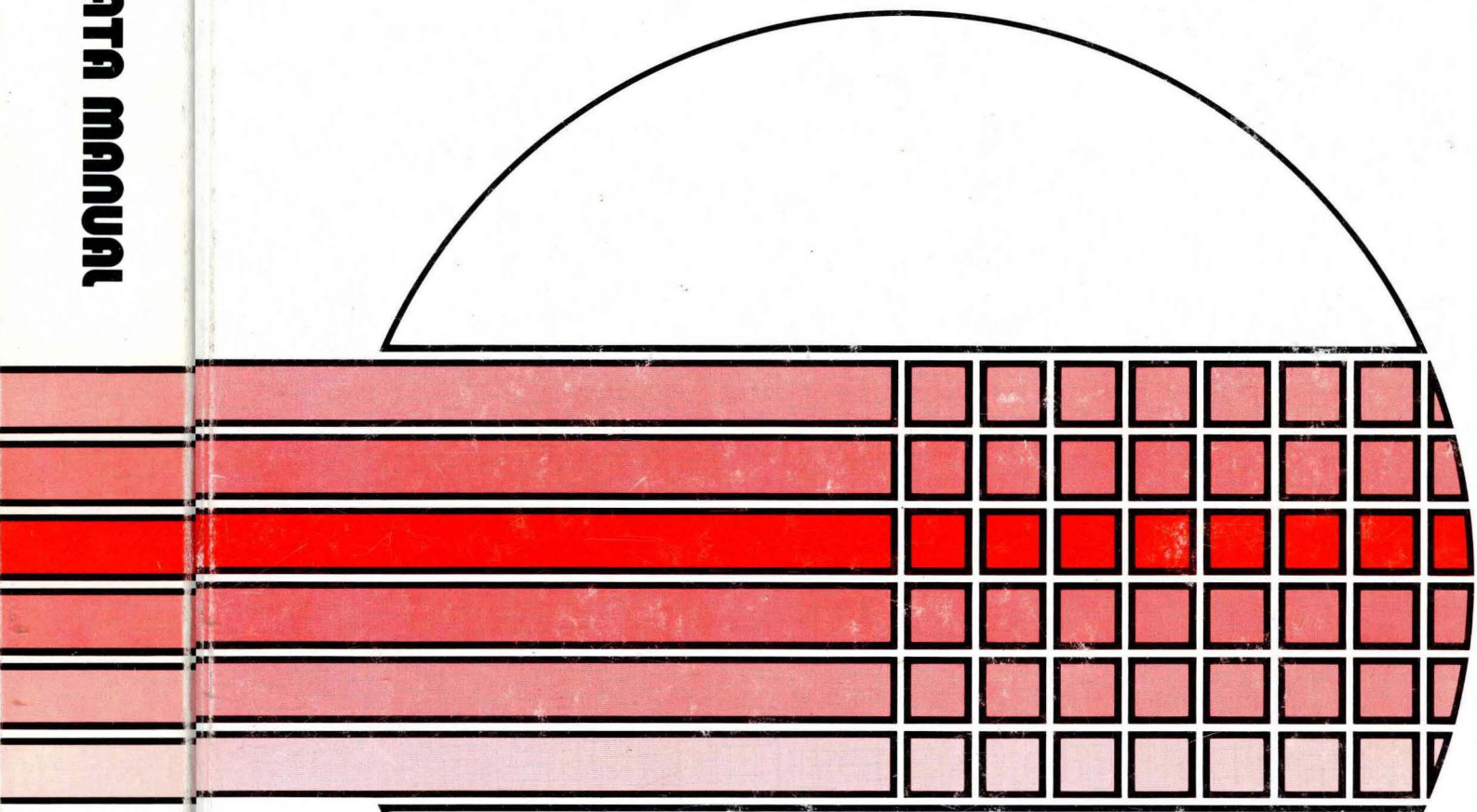

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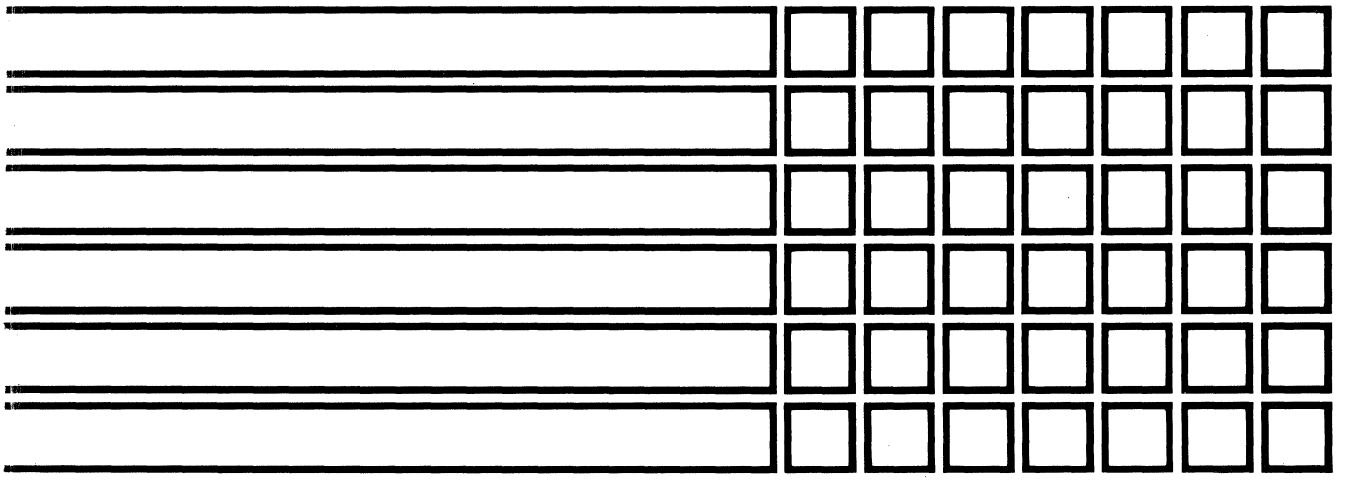

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μA78HV24C	Three Terminal Positive Voltage Regulator	198
SA78HV05C	Three Terminal Positive Voltage Regulator	198
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INTRODUCTION

As one of the world's largest manufacturers of integrated circuits, Signetics designs, develops, manufactures and sells over 1600 different types of integrated circuits. Signetics produces digital and linear circuits, utilizing both bipolar and metal-oxide-semiconductor (MOS) manufacturing processes.

The Analog division is a major broad line supplier of both Signetics' original designs and industry standard devices. The NE535 High Performance Operational Amplifier, the NE555 Timer and the NE567 Phase Locked Loop are among Signetics' original products. Leading industry standard products available from Signetics include the LM124/224/324 Quad Operational Amplifier, the LM139/239/339 Quad Comparator, the μA741 and MC1458 General Purpose Operational Amplifiers. The breadth of the Analog product line offers the designer, the component engineer, and the purchasing agent a varied approach to linear circuits ranging from the μA741 to the latest in high technology products—a microprocessor compatible digital-to-analog converter—the NE5018.

This broad analog circuit product line is backed by Signetics' industry image as a quality manufacturer to whom the servicing of the customer's needs is paramount. In order to continually improve this service capability, Signetics has, and will continue to implement, product development plans to include both original designs and leading industry standards. Examples of new products expected to be available within the next six months, but not included in this edition of the Analog manual are:

TYPE	DESCRIPTION
NE530	High Speed Operational Amplifier
NE5530	Dual High Speed Operational Amplifier (Dual 530)
NE503	1536-Bit Bucket Brigade
NE5533	Dual 5534
79HV00	High Breakdown 79XX
TDA2002	Audio Amp
TDA2573	TV Vertical Countdown
NE5034	8-Bit A/D Converter
NE588	LED Display Driver - Source Outputs
NE589	LED Display Driver - Source Outputs
NE5010	10-Bit D/A Converter
MC1399	TV Color Processing Circuit
μA79HV00	Three Terminal Negative High Voltage Regulator

The 1977 Analog Data Manual is one in a series of four data manuals published by Signetics. This publication is intended to serve as a single technical reference for designing with linear circuits by presenting both data specifications and applications information in one manual.

The format of this year's edition differs from that of the 1976 Analog manual. Data specifications and applications material are presented in two sections indexed for ease of use. The Data Specifications portion is completely new data presented in standard data sheet format reflecting commercial and military grade availability. The Applications portion is updated and rewritten to reflect data on new products issued in the last year. In addition, a section on Military provides information on product availability and processing options.

ORDERING INFORMATION

Signetics' Analog integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors. A complete listing is located on the back cover of this manual.

Minimum Factory Order:

Commercial Product:

$1000 per order

$50 per line item per order

Military Product:

$250 per line item per order

Table 1 provides part number information concerning for both Signetics originated products and industry standard products.

Table 2 is a cross reference of both the old and new package suffixes for all presently existing types, while Table 3 and 4 provide appropriate explanations on the various prefixes employed in the part number descriptions.

As noted in Table 3, Signetics defines device operating temperature range by the appropriate prefix. It should be noted however, that devices with a SE prefix (-55°C to +125°C) indicates only its operating temperature range and *not* its military qualification status. The military qualification status of any analog product can be determined by either looking in the Military Section in this manual and/or contacting your local sales office.

PART NUMBER	CROSS REF PART NO.	PRODUCT FAMILY	PRODUCT DESCRIPTION
NE535N	MC1741SC	ANA	High Slew Rate OP-AMP
μA741C	LM741CJ	ANA	General Purpose OP-AMP

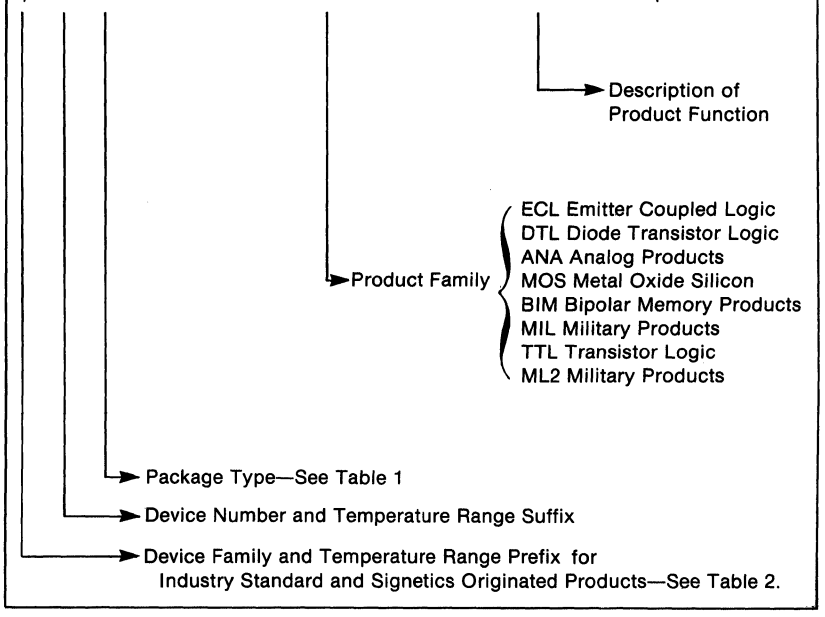


Table 1 PART NUMBER DESCRIPTION

SUFFIX		PACKAGE DESCRIPTION[2]
Old	New	
A,AA	N	14-lead plastic DIL
A	N-14	14-lead plastic DIL (Selected Analog products only)
B,BA	N	16-lead plastic DIL
DA	DA	2-lead TO-3
DB	DB	3-lead TO-5
DC	DC	4-lead TO-46
DE	DE	4-lead TO-72
F	F	14, 16, 18, 22 and 24-lead ceramic (Cerdip) DIL
I,IK	I	14, 16, 18, 22, 28 and 4-lead ceramic DIL
K	K	10-lead TO-100
L	L	10-lead high-profile TO-100 can
NA,NX	N	24-lead plastic DIL
PN	PHA	12 + 1 GND pin DIL
Q,R	Q	10, 14, 16 and 24-lead ceramic flat
S	S	3-lead TO-92 plastic
SK	SK	Microprocessor kit
T,TA	T	8-lead TO-99
U	U	Plastic power TO-220
V	N	8-lead plastic DIL
W,WJ	W	10, 14, 16 and 24-lead ceramic (Cerpac) flat
XA	N	18-lead plastic DIL
XC	N	20-lead plastic DIL
XC	N	22-lead plastic DIL
XL,XF	N	28-lead plastic DIL

Table 2 PACKAGE DESCRIPTIONS

PREFIX	DEVICE TEMPERATURE RANGE
N-	0° to +70°C
S-	-55° to +125°C
NE-	0° to +70°C
SE-	-55° to +125°C
SA	-44° to +85°C
SU	-25° to +85°C

Table 3 DEVICE TEMPERATURE

PREFIX	DEVICE FAMILY
CA	Linear Industry Standard
DM	Linear Industry Standard
JB	Mil Rel—Jan Qualified—Old Designator
JM	Mil Rel—Jan Qualified—New Designator
LH	Linear Industry Standard
LM	Linear Industry Standard
M	Mil Rel—Jan Processed
MC	Linear Industry Standard
PA	Linear Industry Standard
SD	Linear DMOS
SP	DTL Series
UA	Linear Industry Standard
ULN	Linear Industry Standard

Table 4 FAMILY PREFIX

SPECIAL PROCESSING

Signetics offers two major processing levels: Mil-Spec and Supr II. Following are brief descriptions of these processes. For further information in either product availability or process data, contact your local Signetics sales office.

SUPR II

Signetics Upgraded Product Reliability (SUPR) program is designed to provide industrial manufacturers with integrated circuits of a higher level of quality and reliability than is available with standard commercial product. Improvements in quality and reliability will result in significant cost savings to the integrated circuit user. Signetics has maintained a quality and reliability leadership position via its SUPR-DIP program (1972) and SUPR II program (1975). SUPR II is a two-level program. Level A boosts the AQL functional guarantee on all Signetics product families. Level B, for maximum reliability, includes an additional 100% burn-in to Mil std 883. Condition F.

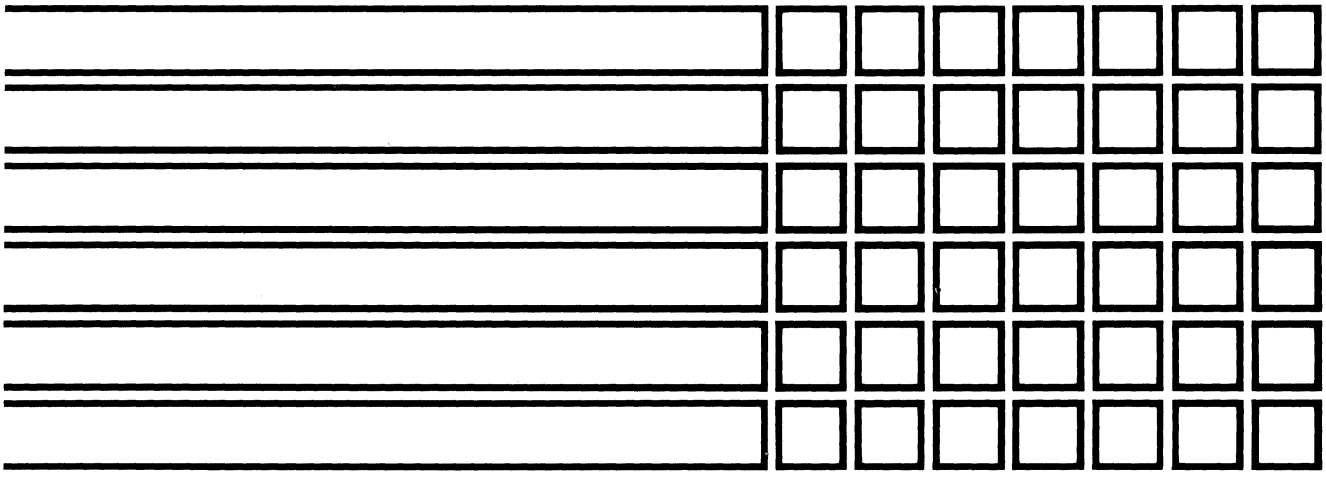
LEVEL A HIGHLIGHTS

- Thermal shock preconditioning (per Mil std 883)
- 100% dc testing
- 100% functional testing at 100°
- SEM wafer quality monitor
- Die and preseal visual inspection criteria (per Mil std 883)

The Analog division is continually expanding the availability list of products processed to SUPR II Levels A and B. For information concerning the SUPR II status of products not shown in Table 5, contact your local Signetics sales office.

DM8820	LM319	μA723C
DM8830	LM324	μA741C
DM8880	LM339	μA747C
DM8880-1	MC1458	μA748C
LM124	MC3302	μA7805C
LM201H	μA709C	μA7812C
LM301A	μA710C	75450B
LM307	μA711C	75451B
LM308	NE555	75452B
LM309	NE556	75453B
LM3111	75454B	
MC1496		

Table 5 PRODUCT PRESENTLY AVAILABLE TO LEVELS A AND B



DATA SPECIFICATIONS

SECTION I
OPERATIONAL AMPLIFIERS

LF155/A/156/A/157/A, LF255/256/257,
LF355/A/356/A/357/A-T

DESCRIPTION

LF155, LF155A, LF255, LF355, LF355A (Low Supply Current)
LF156, LF156A, LF256, LF356, LF356A (Wide Band)
LF157, LF157A, LF257, LF357, LF357A (Wide Band)
The LF155, LF156, LF157 Series of operational amplifiers employ well matched, high voltage JFET input structures on the same monolithic chip as bipolar devices. These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time and low noise.

COMMON FEATURES

(LF155A/156A/157A)

- **Low input bias current 30pA**
- **Low input offset current 3pA**
- **High input impedance $10^{12}\Omega$**
- **Low input offset voltage 1mV**
- **Low V_{OS} temperature drift 3μV/°C**
- **Low input noise current 0.01pA/$\sqrt{Hz}$**

SPECIFIC FEATURES

	LF155A	LF156A
• Settling time (0.01%)	4μs	1.5μs
• High slew rate	5v/μs	12v/μs
• Wide bandwidth	2.5MHz	5MHz
• Low input noise	20nV/$\sqrt{Hz}$	12nV/$\sqrt{Hz}$

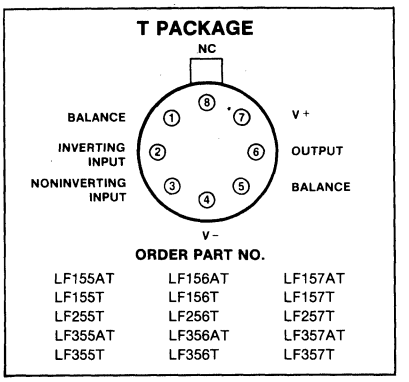
- **LF155, LF156—military qualifications pending**

	LF157A (A_V = 5)
• Settling time (0.01%)	1.5μs
• High slew rate	50v/μs
• Wide bandwidth	20MHz
• Low input noise	12nV/$\sqrt{Hz}$

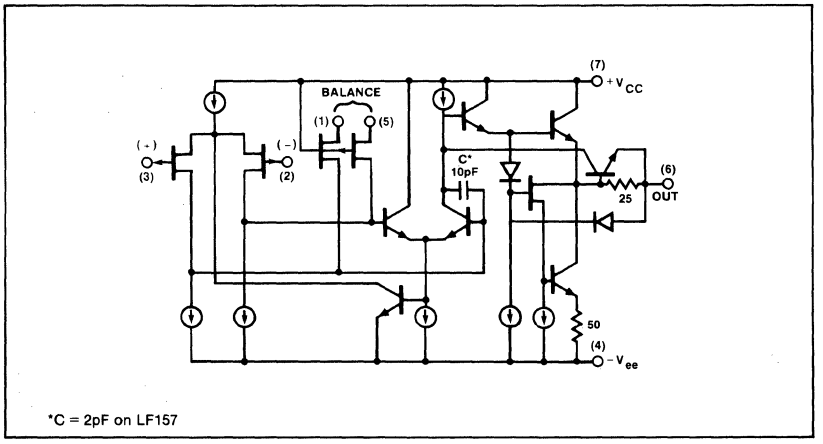
APPLICATIONS

- **Precision high speed integrators**
- **Fast A/D, D/A converters**
- **High impedance buffers**
- **Wideband, low noise, low drift amplifier**

PIN CONFIGURATION



EQUIVALENT SCHEMATIC



*C = 2pF on LF157

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
LF155A/6A/7A, LF155/6/7	±22	V
LF255/6/7	±22	V
LF355A/6A/7A, LF355/6/7	±18	V
Power dissipation[1] TO-99 (T-package)		
LF155A/6A/7A, LF155/6/7	670	mW
LF255/6/7	570	mW
LF355A/6A/7A, LF355/6/7	500	mW
Operating temperature range		
LF155A/6A/7A, LF155/6/7	-55 to +125	°C
LF255/6/7	-25 to +85	°C
LF355A/6A/7A, LF355/6/7	0 to +70	°C
T_J (Max)		
LF155A/6A/7A, LF155/6/7	150	°C
LF255/6/7	115	°C
LF355A/6A/7A, LF355/6/7	100	°C
Input voltage range[2]		
LF155A/6A/7A, LF155/6/7	±20	V
LF255/6/7	±20	V
LF355A/6A/7A, LF355/6/7	±20	V
Output short circuit duration		
LF155A/6A/7A, LF155/6/7	Continuous	
LF255/6/7	Continuous	
LF355A/6A/7A, LF355/6/7	Continuous	
Storage temperature range		
LF155A/6A/7A, LF155/6/7	-65 to +150	°C
LF255/6/7	-65 to +150	°C
LF355A/6A/7A, LF355/6/7	-65 to +150	°C
Lead temperature (soldering, 10sec.)	300	°C
LF155A/6A/7A, LF155/6/7	300	°C
LF255/6/7	300	°C
LF355A/6A/7A, LF355/6/7	300	°C

NOTES

1. The TO-99 package must be derated based on a thermal resistance of 150°C/W junction to ambient or 25°C/W junction to case.
2. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

LF155/A/156/A/157/A, LF255/256/257,
LF355/A/356/A/357/A-T

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$ unless otherwise specified. (See notes on following page.)

PARAMETER		TEST CONDITIONS	LF155A/6A/7A			LF355A/6A/7A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S = 50\Omega$		1	2 2.5		1	2 2.3	mV mV
$\Delta V_{OS}/\Delta T$	Avg. TC of input offset voltage	$R_S = 50\Omega$		3	5		3	5	$\mu V/°C$
$\Delta TC/\Delta V_{OS}$	Change in average TC[2] with V_{OS} adjust	$R_S = 50\Omega$		0.5			0.5		$\mu V/°C$ per mV
I_{OS}	Input offset current[1,3]	$T_J = 25°C$ $T_J \leq T_{high}$		3	10 10		3	10 1	pA nA
I_B	Input bias current[1,3]	$T_J = 25°C$ $T_J \leq T_{high}$		30	50 25		30	50 5	pA nA
R_{IN}	Input resistance	$T_J = 25°C$		10^{12}			10^{12}		Ω
A_{VOL}	Large signal voltage gain	$V_S = \pm 15V$ $V_O = \pm 10V$, $R_L = 2k\Omega$ Over temp.	50 25	200		50 25	200		V/mV V/mV
V_O	Output voltage swing	$V_S = \pm 15V$, $R_L = 10k\Omega$ $V_S = \pm 15V$, $R_L = 2k\Omega$	±12 ±10	±13 ±12		±12 ±10	±13 ±12		V V
V_{CM}	Input common mode Voltage range	$V_S = \pm 15V$	±11	+15.1 -12		±11	+15.1 -12		V V V
CMRR	Common-mode rejection ratio		85	100		85	100		dB
PSRR	Supply volt. rej. ratio[4]		85	100		85	100		dB

DC ELECTRICAL CHARACTERISTICS

(Cont'd) $T_A = 25°C$ unless otherwise specified. (See notes on following page.)

PARAMETER		TEST CONDITIONS	LF155/6/7			LF255/6/7			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S = 50\Omega$		3	5 7		3	5 6.5	mV mV
$\Delta V_{OS}/\Delta T$	Avg. TC of input offset voltage	$R_S = 50\Omega$		5			5		$\mu V/°C$
$\Delta TC/\Delta V_{OS}$	Change in average TC[2] with V_{OS} adjust	$R_S = 50\Omega$		0.5			0.5		$\mu V/°C$ per mV
I_{OS}	Input offset current[1,3]	$T_J = 25°C$ $T_J \leq T_{high}$		3	20 20		3	20 1	pA nA
I_B	Input bias current[1,3]	$T_J = 25°C$ $T_J \leq T_{high}$		30	100 50		30	100 5	pA nA
R_{IN}	Input resistance	$T_J = 25°C$		10^{12}			10^{12}		Ω
A_{VOL}	Large signal voltage gain	$V_S = \pm 15V$ $V_O = \pm 10V$, $R_L = 2k\Omega$ Over temp.	50 25	200		50 25	200		V/mV V/mV
V_O	Output voltage swing	$V_S = \pm 15V$, $R_L = 10k\Omega$ $V_S = \pm 15V$, $R_L = 2k\Omega$	±12 ±10	±13 ±12		±12 ±10	±13 ±12		V V
V_{CM}	Input common mode Voltage range	$V_S = \pm 15V$	±11	+15.1 -12		±11	+15.1 -12		V V V
CMRR	Common-mode rejection ratio		85	100		85	100		dB
PSRR	Supply volt. rej. ratio[4]		85	100		85	100		dB

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	LF355/6/7			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S = 50\Omega$		3	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Avg. TC of input offset voltage	$R_S = 50\Omega$		5		$\mu V/°C$
$\Delta TC/\Delta V_{OS}$	Change in average TC[2] with V_{OS} adjust	$R_S = 50\Omega$		0.5		$\mu V/°C$ per mV
I_{OS}	Input offset current[1,3]	$T_J = 25°C$ $T_J \leq T_{high}$		3	50 2	pA nA
I_B	Input bias current[1,3]	$T_J = 25°C$ $T_J \leq T_{high}$		30	200 8	pA nA
R_{IN}	Input resistance	$T_J = 25°C$				Ω
A_{VOL}	Large signal voltage gain	$V_S = \pm 15V$ $V_O = \pm 10V$, $R_L = 2k\Omega$ Over temp.	25 15	10^{12} 200		V/mV V/mV
V_O	Output voltage swing	$V_S = \pm 15V$, $R_L = 10k\Omega$ $V_S = \pm 15V$, $R_L = 2k\Omega$	±12 ±10	±13 ±12		V V
V_{CM}	Input common mode Voltage range	$V_S = \pm 15V$	±10	+15.1 -12		V V V
CMRR	Common-mode rejection ratio		80	100		dB
PSRR	Supply volt. rej. ratio[4]		80	100		dB

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

PARAMETER	LF155A/355A LF155/255			LF355			LF156A/LF156/256			UNIT
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supply current		2	4		2	4		5	7	mA

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

PARAMETER	LF356A/LF356			LF157A/LF157/257			LF357A/LF357			UNIT
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supply current		5	10		5	7		5	10	mA

NOTES

1. These specifications apply for $\pm 15V \leq V_S \leq \pm 20V$, $-55°C \leq T_A \pm 125°C$ and $T_{HIGH} = +125°C$ unless otherwise stated for the LF155A/6A/7A and the LF155/6/7. For the LF255/6/7, these specifications apply for $\pm 15V \leq V_S \leq \pm 20V$, $-25°C \leq T_A \leq +85°C$ and $T_{HIGH} = 85°C$ unless otherwise stated. For the LF355A/6A/7A, these specifications apply for $\pm 15V \leq V_S \leq \pm 20V$, $0°C \leq T_A \leq +70°C$ and $T_{HIGH} = +70°C$, and for the LF355/6/7 these specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.
2. The Temperature Coefficient of the adjusted input offset voltage changes only a small amount ($0.5\mu V/°C$ typically) for each mV of adjustment from its original unadjusted value. Common mode rejection and open loop voltage gain are also unaffected by offset adjustment.
3. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \theta_{jA}$ Pd where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
4. Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

LF155/A/156/A/157/A, LF255/256/257,
LF355/A/356/A/357/A-T

AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.[1]

PARAMETER		TEST CONDITIONS	LF155A/LF355A			LF156A/356A			LF157A/357A			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SR	Slew rate	LF155/156 LF155A/6A: $A_V = 1$	3	5		10	12		40	50		V/μs
GBW	Gain bandwidth product			2.5		4	4.5		15	20		MHz
t_s	Settling time[5] to 0.01%			4			1.5			1.5		μs
e_n	Equiv. input noise volt.	$R_S = 100\Omega$										
		f = 100Hz		25			15			15		nV/√Hz
		f = 1000Hz		20			12			12		nV/√Hz
i_n	Equiv. input noise current	f = 100Hz		0.01			0.01			0.01		pA/√Hz
		f = 1000Hz		0.01			0.01			0.01		pA/√Hz
C_{IN}	Input capacitance			3			3			3		pF

AC ELECTRICAL CHARACTERISTICS

(Cont'd) $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.[1]

PARAMETER		TEST CONDITIONS	LF155/255/355			LF156/256			LF356			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SR	Slew rate	LF155/156 LF155A/6A: $A_V = 1$,		5		7.5	12			12		V/μs
GBW	Gain bandwidth product			2.5			5			5		MHz
t_s	Settling time[5] to 0.01%			4			1.5			1.5		μs
e_n	Equiv. input noise volt.	$R_S = 100\Omega$										
		f = 100Hz		25			15			15		nV/√Hz
		f = 1000Hz		20			12			12		nV/√Hz
i_n	Equiv. input noise current	f = 100Hz		0.01			0.01			0.01		pA/√Hz
		f = 1000Hz		0.01			0.01			0.01		pA/√Hz
C_{IN}	Input capacitance			3			3			3		pF

AC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.[1]

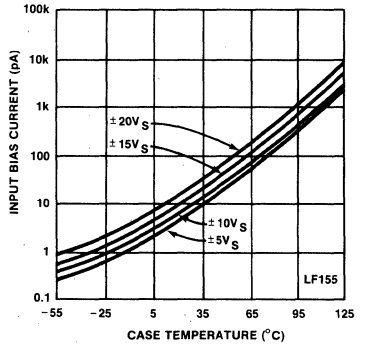
PARAMETER		TEST CONDITIONS	LF157/257			LF357			UNIT
			Min	Typ	Max	Min	Typ	Max	
SR	Slew rate	LF157A/LF157: $A_V = 5$	30	50			50		V/μs
GBW	Gain bandwidth product			20			20		MHz
t_s	Settling time[5] to 0.01%			1.5			1.5		μs
e_n	Equiv. input noise volt.	$R_s = 100\Omega$							
		f = 100Hz		15			15		nV/√Hz
		f = 1000Hz		12			12		nV/√Hz
i_n	Equiv. input noise current	f = 100Hz		0.01			0.01		pA/√Hz
		f = 1000Hz		0.01			0.01		pA/√Hz
C_{IN}	Input capacitance			3			3		pF

NOTE

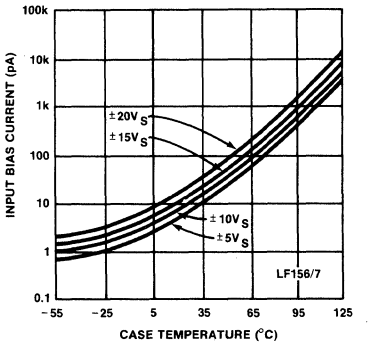
5. Settling time is defined here, for a unity gain inverter connection using 2kΩ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157, $A_V = -5$, the feedback resistor from output to input is 2kΩ and the output step is 10V (See Settling Time Test Circuit).

TYPICAL DC PERFORMANCE CHARACTERISTICS (curves are for LF155, LF156 and LF157 unless otherwise specified.)

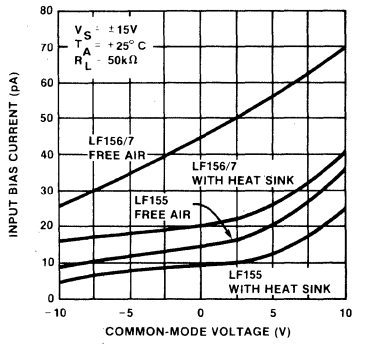
INPUT BIAS CURRENT



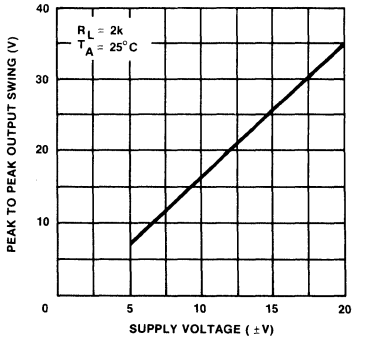
INPUT BIAS CURRENT



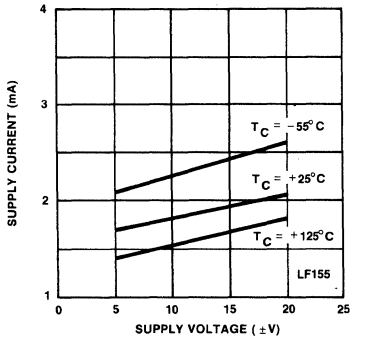
INPUT BIAS CURRENT



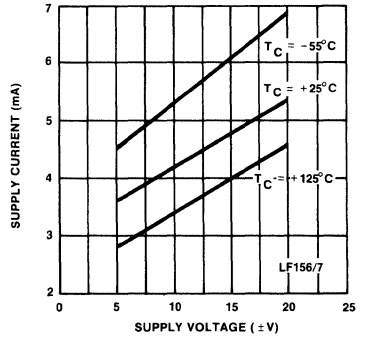
VOLTAGE SWING



SUPPLY CURRENT

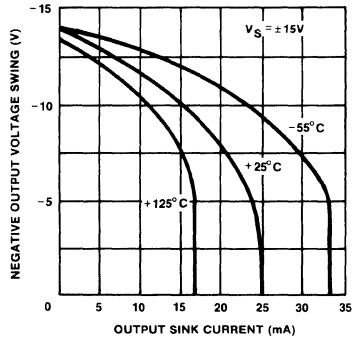


SUPPLY CURRENT

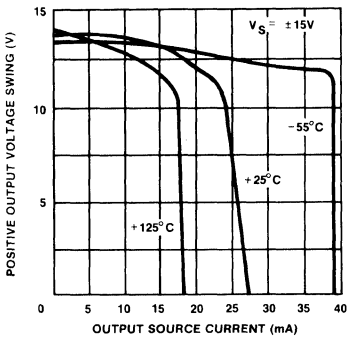


TYPICAL DC PERFORMANCE CHARACTERISTICS (Cont'd)

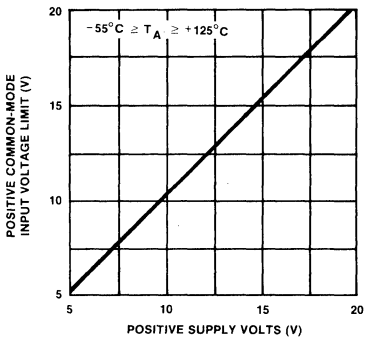
NEGATIVE CURRENT LIMIT



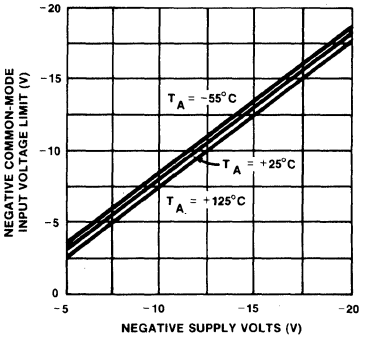
POSITIVE CURRENT LIMIT



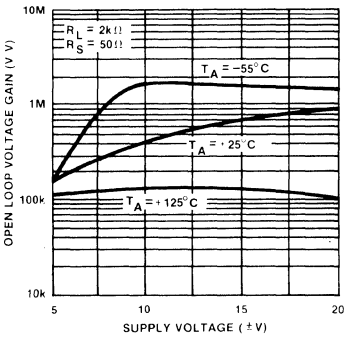
POSITIVE COMMON-MODE INPUT VOLTAGE LIMIT



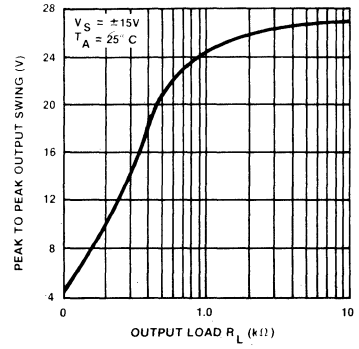
NEGATIVE COMMON-MODE INPUT VOLTAGE LIMIT



OPEN LOOP VOLTAGE GAIN

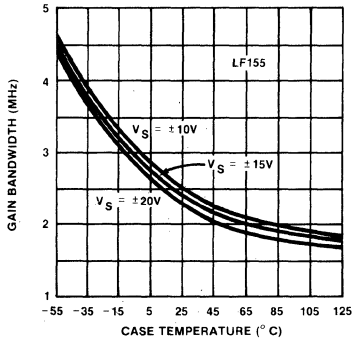


OUTPUT VOLTAGE SWING

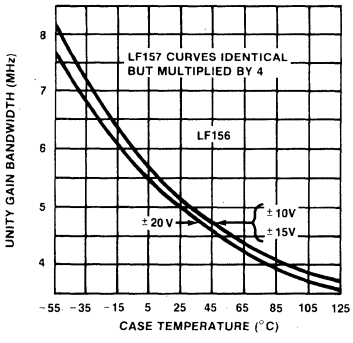


TYPICAL AC PERFORMANCE CHARACTERISTICS

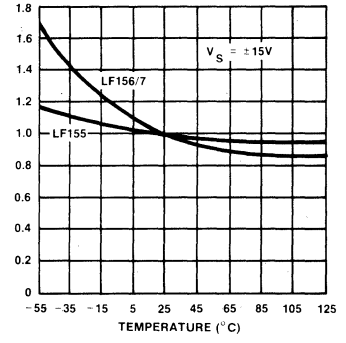
GAIN BANDWIDTH



UNITY GAIN BANDWIDTH

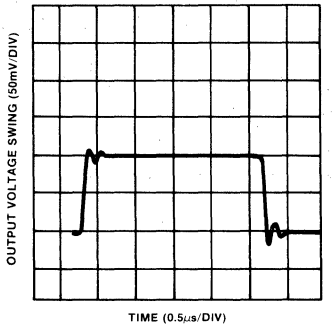


NORMALIZED SLEW RATE

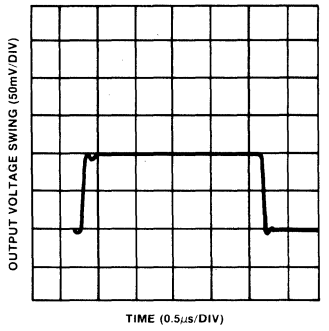


TYPICAL AC PERFORMANCE CHARACTERISTICS (Cont'd)

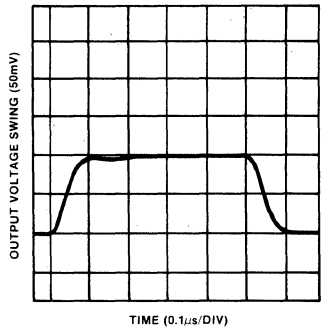
LF155 SMALL SIGNAL PULSE RESPONSE, $A_V = +1$



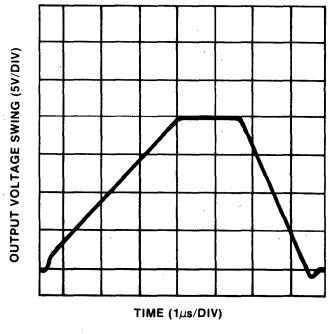
LF156 SMALL SIGNAL PULSE RESPONSE, $A_V = +1$



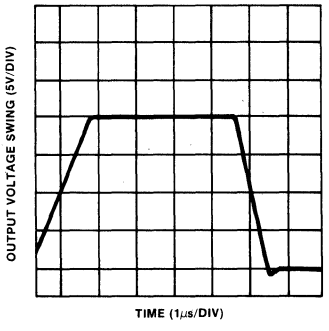
LF157 SMALL SIGNAL PULSE RESPONSE, $A_V = +5$



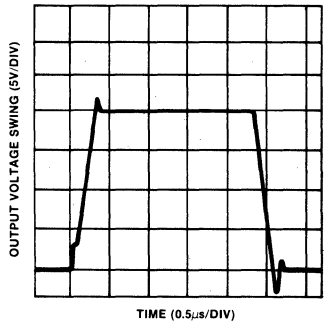
LF155 LARGE SIGNAL PULSE RESPONSE, $A_V = +1$



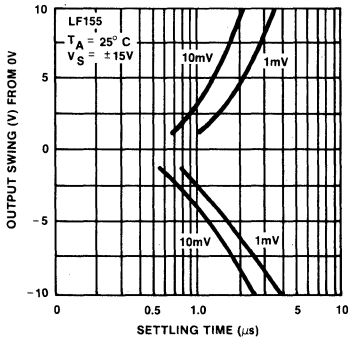
LF156 LARGE SIGNAL PULSE RESPONSE, $A_V = +1$



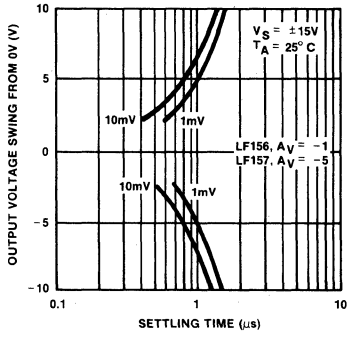
LF157 LARGE SIGNAL PULSE RESPONSE, $A_V = +5$



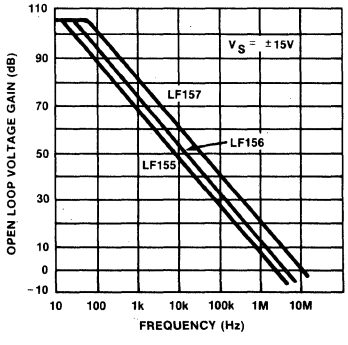
INVERTER SETTLING TIME



INVERTER SETTLING TIME

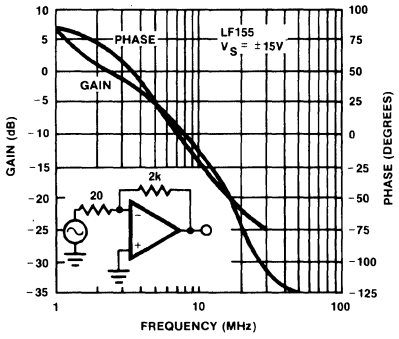


OPEN LOOP FREQUENCY RESPONSE

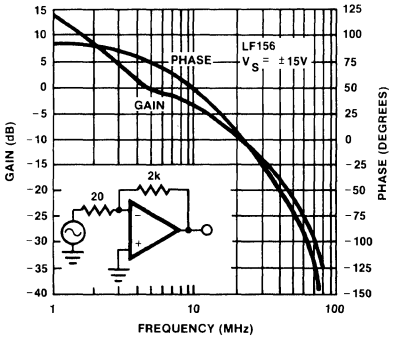


TYPICAL AC PERFORMANCE CHARACTERISTICS (Cont'd)

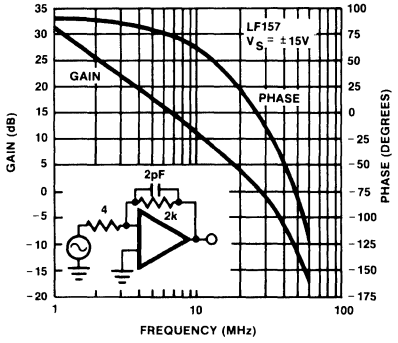
BODE PLOT



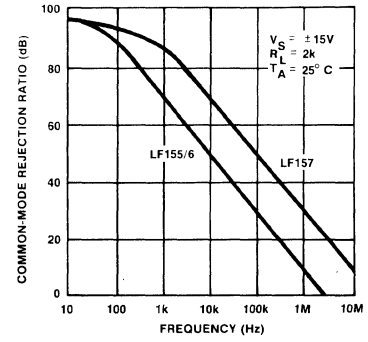
BODE PLOT



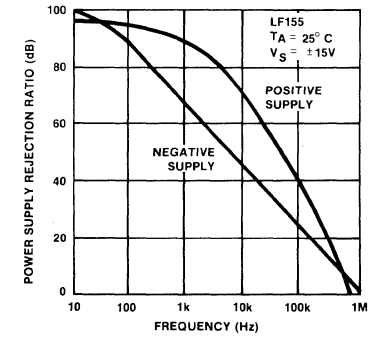
BODE PLOT



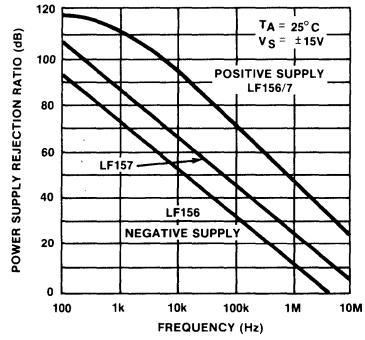
COMMON-MODE REJECTION RATIO



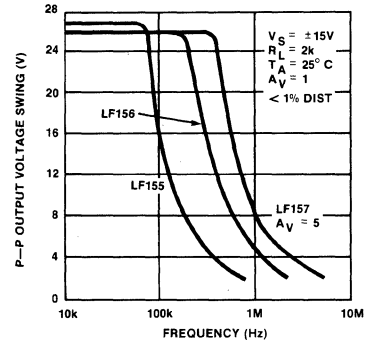
POWER SUPPLY REJECTION RATIO



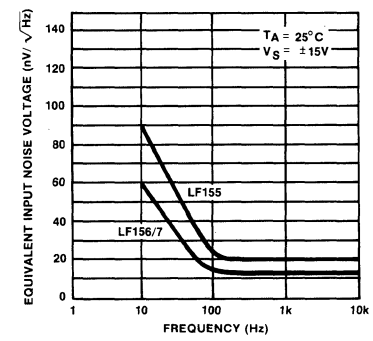
POWER SUPPLY REJECTION RATIO



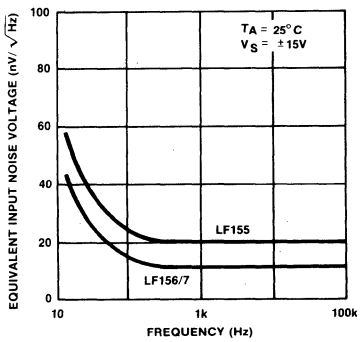
UNDISTORTED OUTPUT VOLTAGE SWING



EQUIVALENT INPUT NOISE VOLTAGE

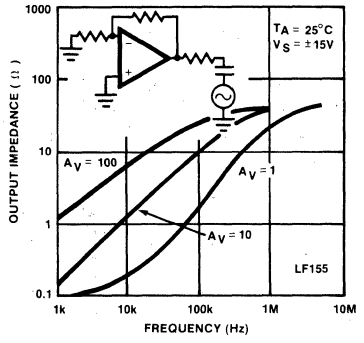


EQUIVALENT INPUT NOISE VOLTAGE (EXPANDED SCALE)

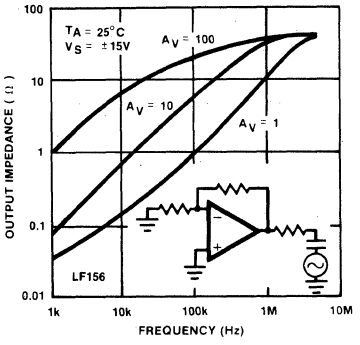


TYPICAL AC PERFORMANCE CHARACTERISTICS (Cont'd)

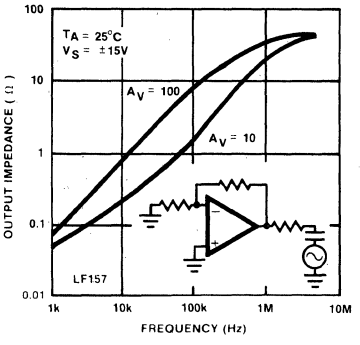
OUTPUT IMPEDANCE



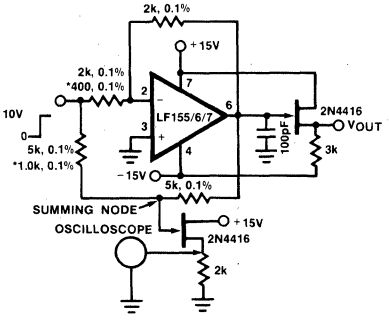
OUTPUT IMPEDANCE



OUTPUT IMPEDANCE



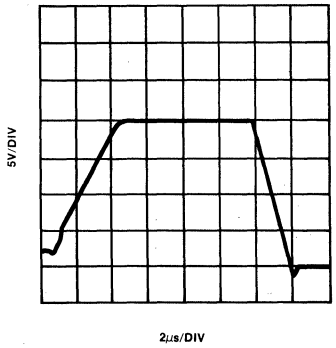
SETTLING TIME TEST CIRCUIT



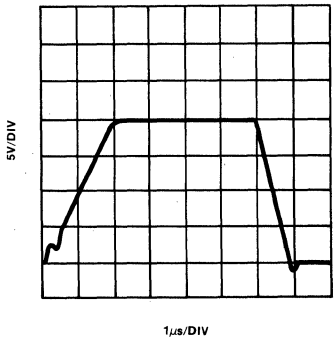
- Settling time is tested with the LF155/6 connected as unity gain inverter and LF157 connected for $A_V = -5$
- FET used to isolate the probe capacitance
- Output = 10V step
- $A_V = -5$ for LF157

LARGE SIGNAL INVERTER OUTPUT, V_{OUT} (FROM SETTLING TIME CIRCUIT)

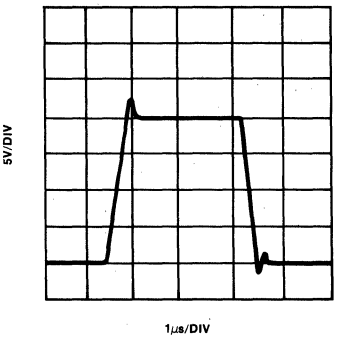
LF155



LF156



LF157



APPLICATION HINTS

The LF155/6/7 series are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

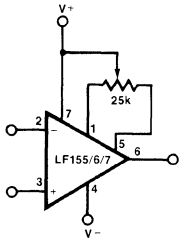
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

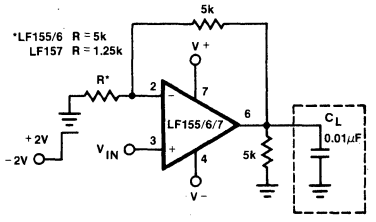
TYPICAL CIRCUIT CONNECTIONS

V_{OS} ADJUSTMENT



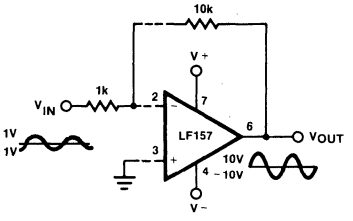
- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V+
- For potentiometers with temperature coefficient of 100ppm/°C or less the additional drift with adjust is ≃ 0.5μV/°C/mV of adjustment
- Typical overall drift: 5μV/°C ± (0.5μV/°C/mV of adj.)

DRIVING CAPACITIVE LOADS



Due to a unique output stage design these amplifiers have the ability to drive large capacitive loads and still maintain stability. C_L max ≤ 0.01μF.
Overshoot ≤ 20%
Setting time (ts) ≥ 5μs

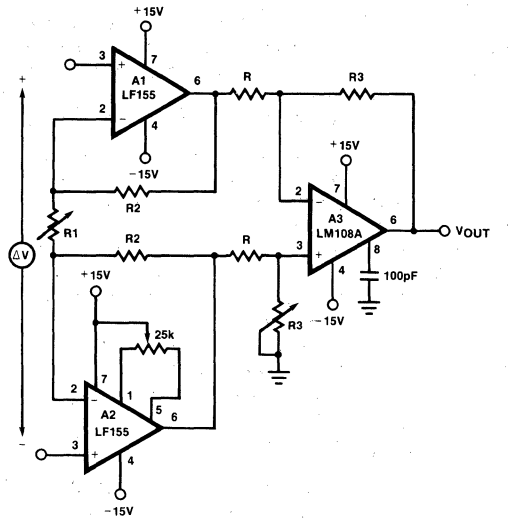
LF157. A LARGE POWER BW AMPLIFIER



For distortion < 1% and a 20V p-p V_{OUT} swing power bandwidth is: 500kHz.

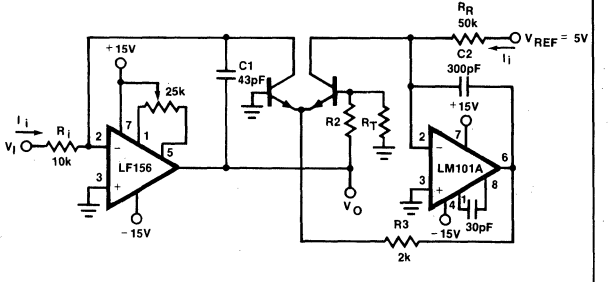
TYPICAL APPLICATIONS

HIGH IMPEDANCE, LOW DRIFT INSTRUMENTATION AMPLIFIER



- $V_{OUT} = \frac{R3}{R}\left[\frac{2R2}{R1} + 1\right]\Delta V$, V- +2V ≤ V_{IN} Common-Mode ≤ V+
- System V_{OS} adjusted via A2 V_{OS} adjust
- Trim R3 to boost up CMRR to 120dB.

FAST LOGARITHMIC CONVERTER

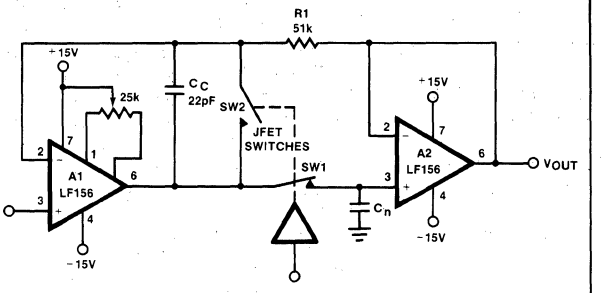


$$|V_{OUT}| = \left[1 + \frac{R2}{R_T}\right]\frac{kT}{q} \ln V_I\left[\frac{R_r}{V_{REF}\, R_i}\right] = \log V_I \frac{1}{R_i\, I_R}$$

R2 = 15.71, R_1 = 1k, 0.3%°C (for temperature compensation)

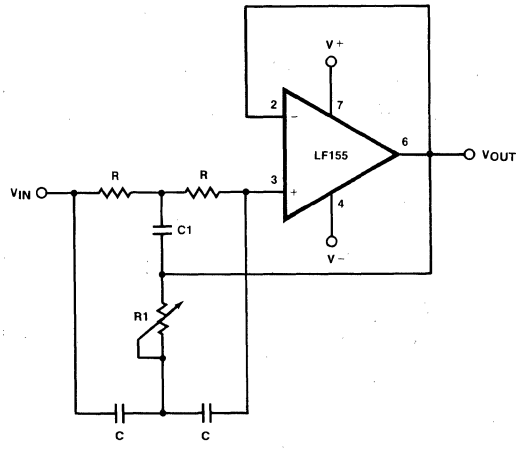
- Dynamic range: 100μA ≤ I_i ≤ 1mA (5 decades, $|V_O|$ = 1V/decades)
- Transient response: 3μs for Δ, = decades
- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF156 to minimize quiescent error
- R_T: Tel Labs type Q81 + 0.3%/°C.

HIGH ACCURACY SAMPLE AND HOLD



- By closing the loop through A2 the V_{OUT} accuracy will be determined uniquely by A1. No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added on propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold.
- R1, C_C: additional compensation
- Use LF156 for
  Δ Fast settling time
  Δ Low V_{OS}

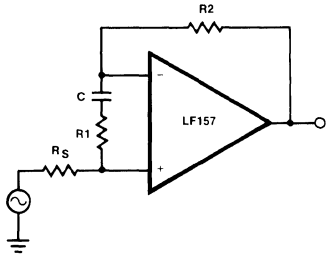
HIGH Q NOTCH FILTER



- 2R1 = R = 10MΩ
  2C = C1 = 300pF
- Capacitors should be matched to obtain high Q
- f_{NOTCH} = 120Hz, notch = 55dB, Q > 180
- Use LF155 for
  Δ Low I_B
  Δ Low supply current

TYPICAL APPLICATIONS (Cont'd)

NON-INVERTING UNITY GAIN OPERATION FOR LF157

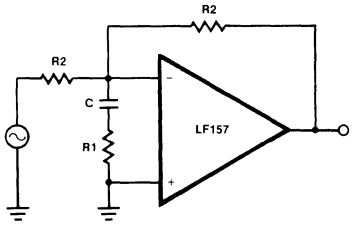


$$R1C1 \geq \frac{1}{(2\pi)\,(5MHz)}$$

$$R1 = \frac{R2 + R5}{4}$$

$A_{V(DC)} = -1$
f-3dB ≈ 5MHz

INVERTING UNITY GAIN FOR LF157

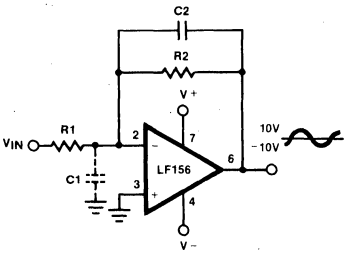


$$R1C1 \geq \frac{1}{(2\pi)\,(5MHz)}$$

$$R1 = \frac{R2}{4}$$

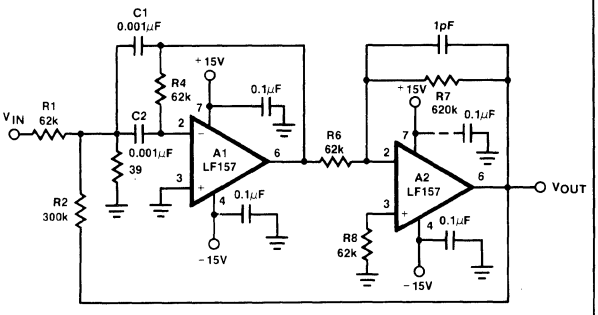
$A_{VI(DC)} \approx -1$
f-3dB ≈ 5MHz

WIDE BW LOW NOISE, LOW DRIFT AMPLIFIER



- Power BW: $f_{MAX} = \frac{S_r}{2\pi/p} \cong 240kHz$
- Parasitic input capacitance C1 ≅ (3pF for LF155, LF156, and LF157 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2C2 ≅ R1C1.

HIGH Q BAND PASS FILTER



- By adding positive feedback (R2) Q increases to 40
- f_{BP} = 100kHz

$$\frac{V_{OUT}}{V_{IN}} = 10\sqrt{Q}$$

- Clean layout recommended
- Response to a 1V p-p tone burst: 300μs

LM101/A/201/A/301/A, LH2101A/2201A/2301A-F,N,N-14,T

DESCRIPTION

The LM101, LM201, LM101A, LM201A, and LM301A are high performance operational amplifiers featuring high gain, short circuit protection, simplified compensation and excellent temperature stability.

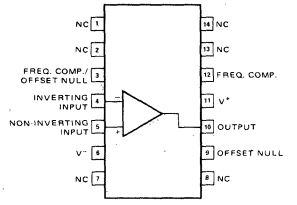
The LH2101A, LH2201A, LH2301A are dual amplifier using two LM101A type devices in the same hermetic package. All electrical specifications are the same as the single amplifiers.

FEATURES

- **Short circuit protection**
- **Offset voltage null capability**
- **Large common-mode and differential voltage ranges**
- **Low power consumption**
- **No latch up**
- **LM101, LM101A Mil std 883A,B,C available**
- **LM101A Mil std 38510 (JAN) planned, Mil std M38510 processing available**

PIN CONFIGURATIONS

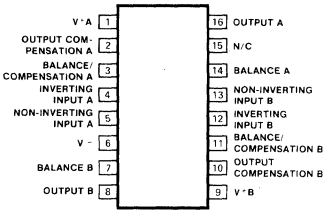
F,N-14 PACKAGE



ORDER PART NO.

LM101N-14	LM101AF
LM201N-14	LM201AF
LM101AN-14	LM301AF
LM201AN-14	LM101F
LM301AN-14	LM201F

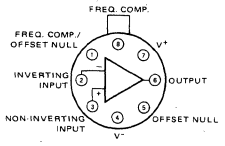
F PACKAGE



ORDER PART NO.

LH2101AF
LH2201AF
LH2301AF

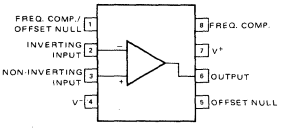
T PACKAGE



ORDER PART NO.

LM101T
LM201T
LM101AT
LM201AT
LM301AT

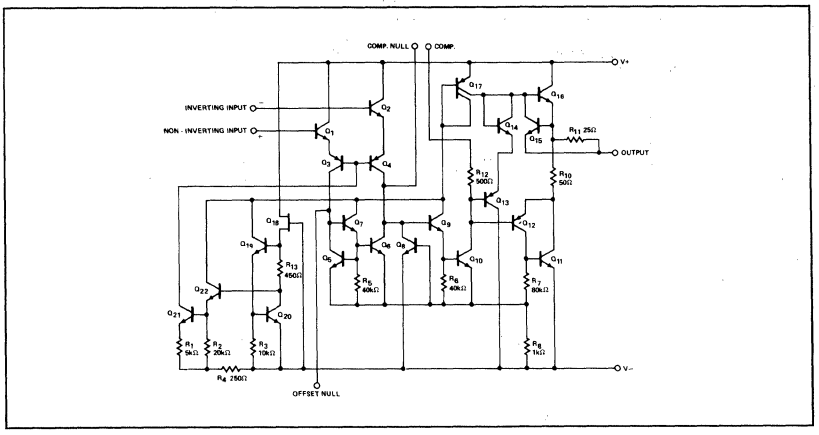
N PACKAGE



ORDER PART NO.

LM101N
LM201N
LM101AN
LM201AN
LM301AN

EQUIVALENT SCHEMATIC



LM101/A/201/A/301/A, LH2101A/2201A/2301A-F,N,N-14,T

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage		
LH2101A, LH2201A, LM101, LM201, LM101A, LM201A	±22	V
LM301A, LH2301A	±18	
Power dissipation[1]	500	mW
Differential input voltage	±30	V
Input voltage[2]	±15	V
Output short circuit duration	Indefinite	
Operating temperature range		
LM101, LM101A, LH2101A	-55 to +125	°C
LM201A, LH2201A	-25 to +85	°C
LM201, LM301A, LH2301A	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 60sec)	300	°C

NOTES

1. Absolute maximum rating holds for all packages. The maximum junction temperature is 150°C for the LM101 and 100°C for the LM201. For operation at elevated temperatures, derate according to appropriate thermal resistances given under package information.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $\pm5V \leq V_S \leq +20V$ unless otherwise specified.*

PARAMETER		TEST CONDITIONS	LM101			LM201			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \leq 10k\Omega$, $C_1 = 30pF$		1.0	5.0		2.0	7.5	mV
		Over temp.			6.0			10	mV
V_{OS}	Drift	$R_S \leq 50\Omega$, $C_1 = 30pF$		3.0			6		µV/°C
		$R_S \leq 10k\Omega$		6.0			10		µV/°C
I_{OS}	Offset current	$C_1 = 30pF$		40	200		100	500	nA
		T_A = high, $C_1 = 30pF$		10	200				nA
		T_A = low		100	500				nA
		Over temp.							nA
		$T_A = +70°C$					50	400	nA
		$T_A = 0°C$					150	750	nA
I_{BIAS}	Input current	$C_1 = 30pF$		120	500		250	1500	nA
		$T_A = -55°C$, $C_1 = 30pF$		280	1500				nA
		$T_A = 0°C$					320	2000	nA
V_{CM}	Common mode voltage range	Over temp., $V_S = \pm15V$, $C_1 = 30pF$	±12			±12			V
CMRR	Common mode rejection ratio	$R_S \leq 10k\Omega$, $C_1 = 30pF$, over temp.	70	90		65	90		dB
R_{IN}	Input resistance	$C_1 = 30pF$	0.3	0.8		0.1	0.4		MΩ
A_{VOL}	Large signal voltage gain	$R_L \geq 2k\Omega$, $V_{OUT} \pm10V$, $V_S = \pm15V$	50	160		20	150		V/mV
		Over temp.	25			15			V/mV
	Supply current	$V_S = \pm20V$		1.8	3.0		1.8	3.0	mA

*NOTE

Unless otherwise specified, all specifications for LM301A are $\pm5V \leq V_S \leq \pm15V$.

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $\pm5V \leq V_S \leq +20V$ unless otherwise specified.*

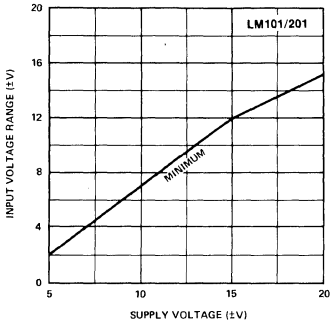
PARAMETER		TEST CONDITIONS	LM101A/LM201A/ LH2101A/LH2201A			LM301A/LH2301A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \leq 50k\Omega$, $C_1 = 30pF$ Over temp.		0.7	2.0 3.0		2.0	7.5 10	mV mV
V_{OS}	Drift	$R_S = 0\Omega$, over temp.		3.0	1.5		6.0	30	$\mu V/°C$
I_{OS}	Offset current	$C_1 = 30pF$ Over temp.		1.5	10 20		3	50 70	nA nA
I_{OS}	Drift	$+25°C \leq T_A \leq T_{MAX}$, $C_1 = 30pF$ $T_{MIN} \leq T_A \leq +25°C$		0.01 0.02	0.1 0.2		0.01 0.02	0.3 0.6	nA/°C nA/°C
I_{BIAS}	Input current	$C_1 = 30pF$ Over temp.		30	75 100		70	250 300	nA nA
V_{CM}	Common mode voltage range	Over temp., $V_S = \pm15V$, $C_1 = 30pF$ $V_S = \pm20$	±15			±12			V V
CMRR	Common mode rejection ratio	$R_S \leq 50k\Omega$, $C_1 = 30pF$, over temp.	80	96		70	90		dB
R_{IN}	Input resistance	$C_1 = 30pF$	1.5	4		0.5	2		MΩ
A_{VOL}	Large signal voltage gain	$R_L \geq 2k\Omega$, $V_{OUT} \pm10V$, $V_S = \pm15V$ Over temp.	50 25	160		25 15	160		V/mV V/mV
	Supply current	$V_S = \pm20V$ $V_S = \pm15V$		1.8	3.0		1.8	3.0	mA mA

*NOTE

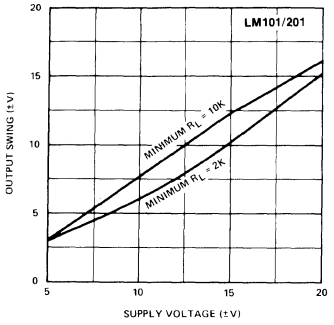
Unless otherwise specified, all specifications for LM301A are $\pm5V \leq V_S \leq \pm15V$.

TYPCIAL PERFORMANCE CHARACTERISTICS

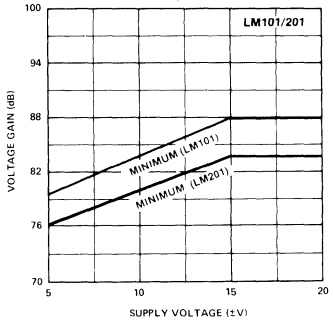
INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE



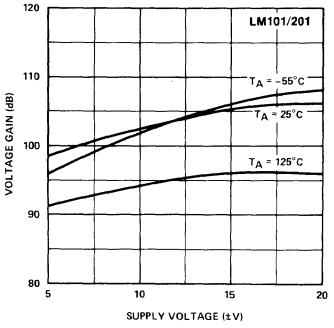
OUTPUT SWING vs SUPPLY VOLTAGE



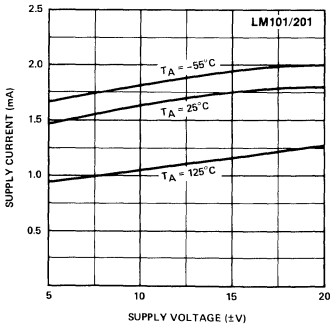
VOLTAGE GAIN vs SUPPLY VOLTAGE



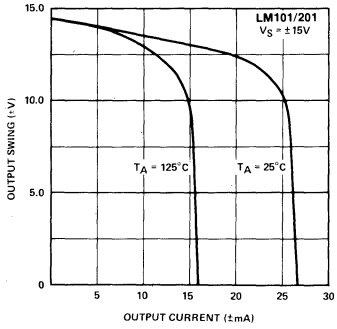
VOLTAGE GAIN



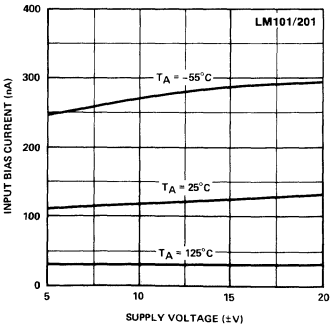
SUPPLY CURRENT



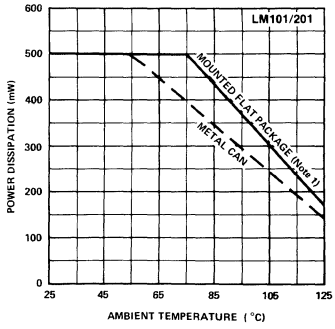
CURRENT LIMITING



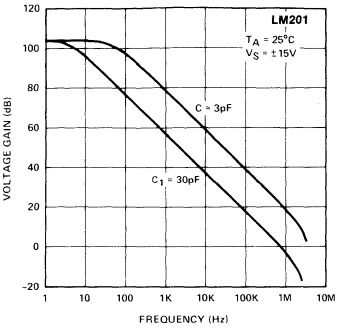
INPUT CURRENT



MAXIMUM POWER DISSIPATION

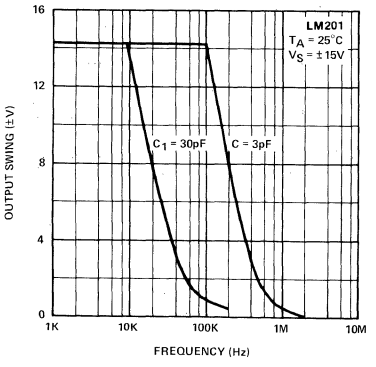


OPEN LOOP FREQUENCY RESPONSE

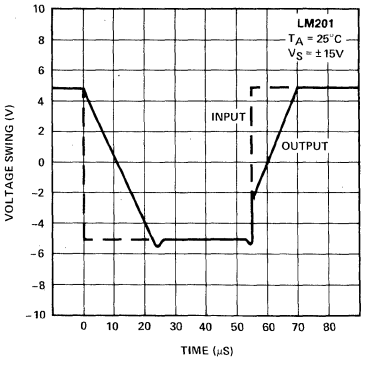


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

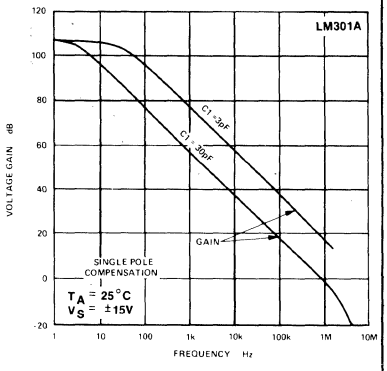
LARGE SIGNAL FREQUENCY RESPONSE



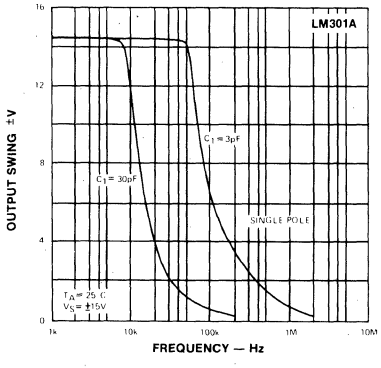
VOLTAGE FOLLOWER PULSE RESPONSE



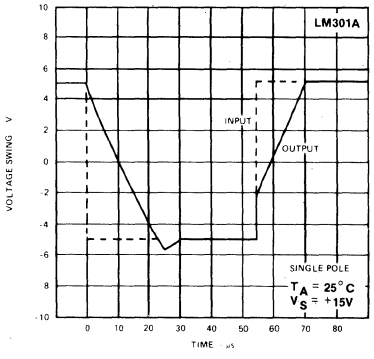
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE

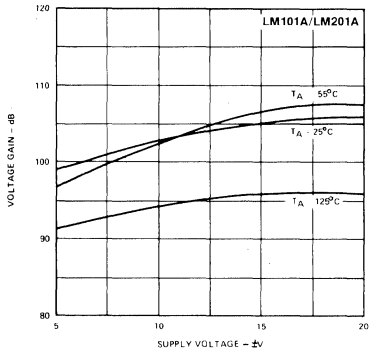


VOLTAGE FOLLOWER PULSE RESPONSE

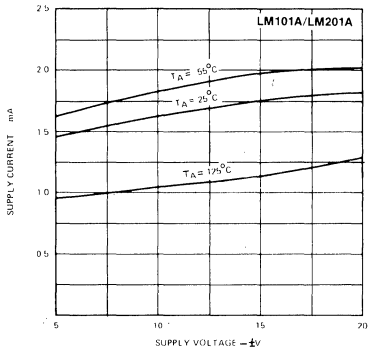


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

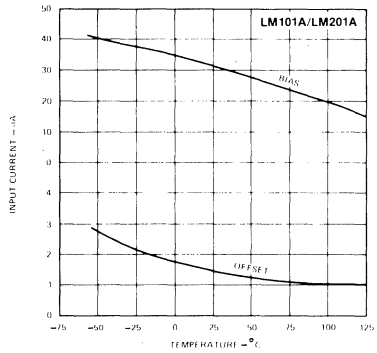
VOLTAGE GAIN



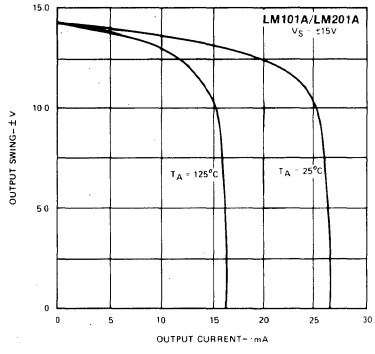
SUPPLY CURRENT



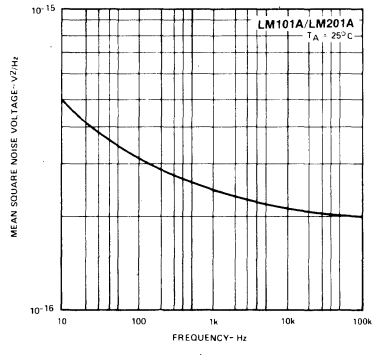
INPUT CURRENT



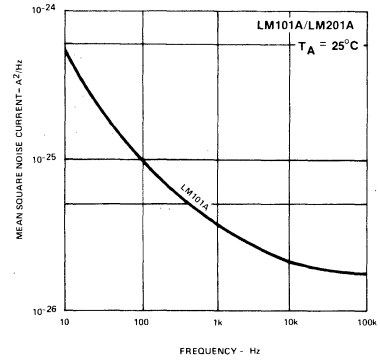
CURRENT LIMITING



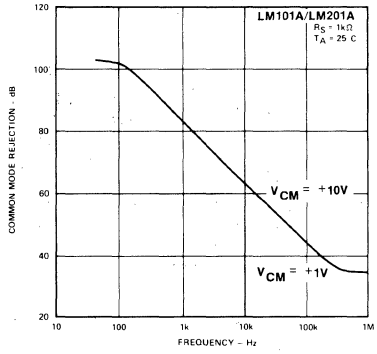
INPUT NOISE VOLTAGE



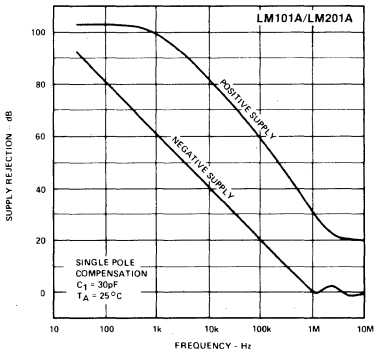
INPUT NOISE CURRENT



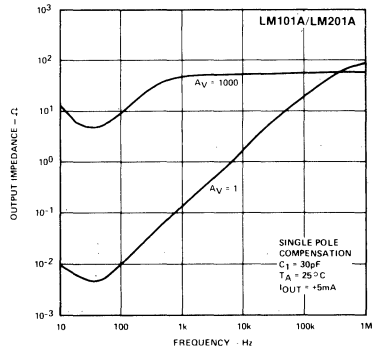
COMMON MODE REJECTION



POWER SUPPLY REJECTION

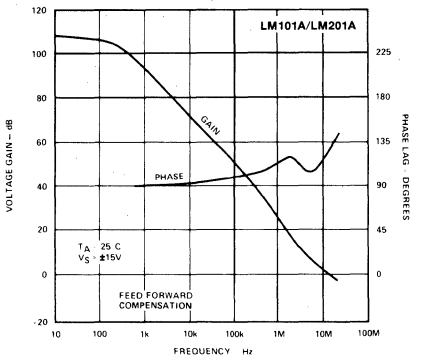


CLOSED LOOP OUTPUT IMPEDANCE

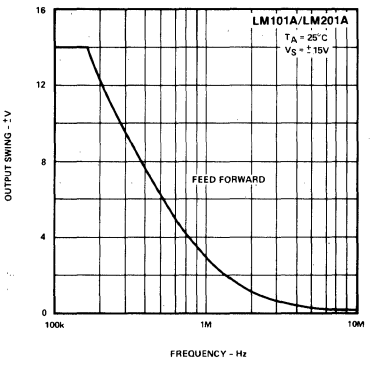


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

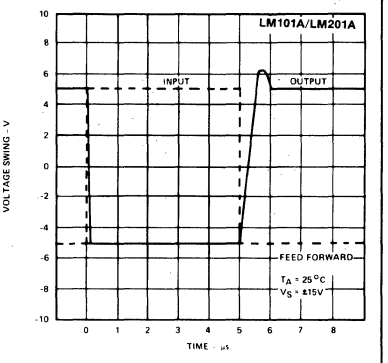
OPEN LOOP FREQUENCY RESPONSE



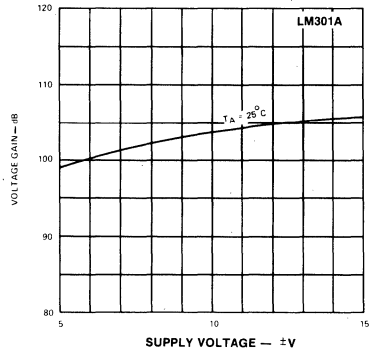
LARGE SIGNAL FREQUENCY RESPONSE



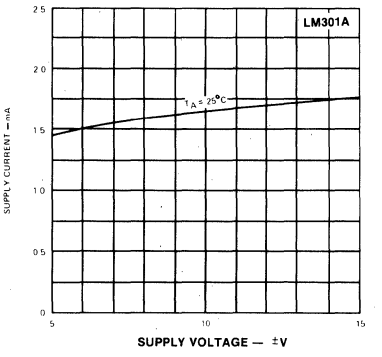
INVERTER PULSE RESPONSE



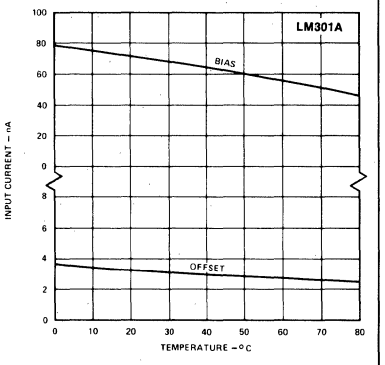
VOLTAGE GAIN



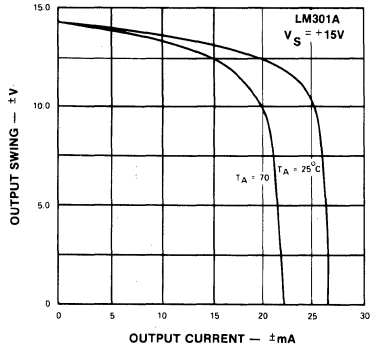
SUPPLY CURRENT



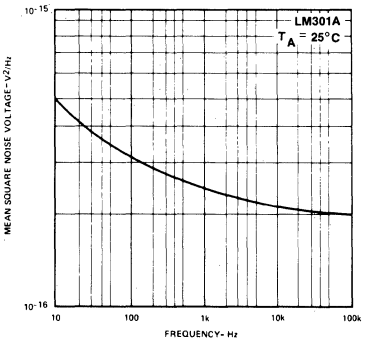
INPUT CURRENT



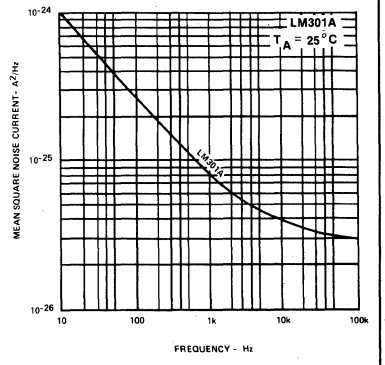
CURRENT LIMITING



INPUT NOISE VOLTAGE

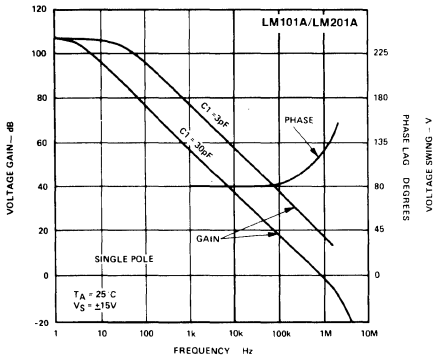


INPUT NOISE CURRENT

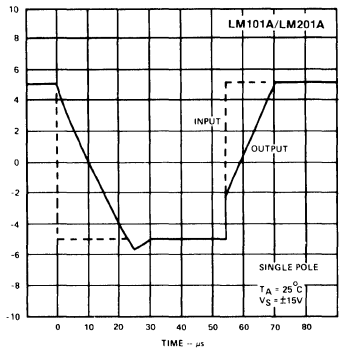


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

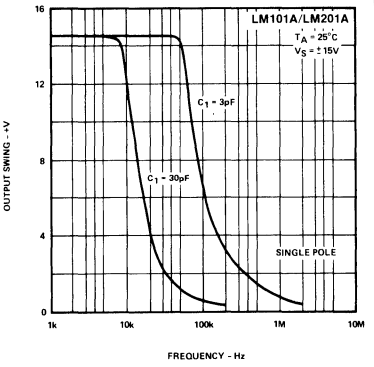
OPEN LOOP FREQUENCY RESPONSE



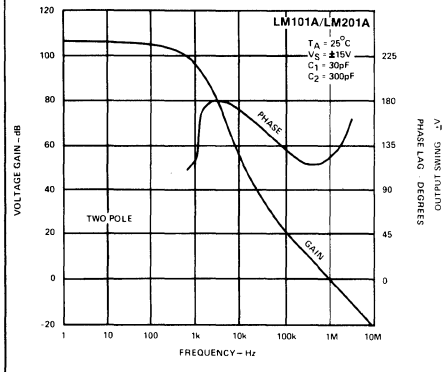
VOLTAGE FOLLOWER PULSE RESPONSE



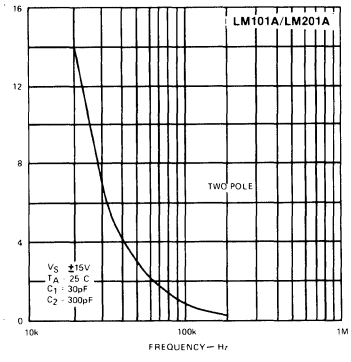
LARGE SIGNAL FREQUENCY RESPONSE



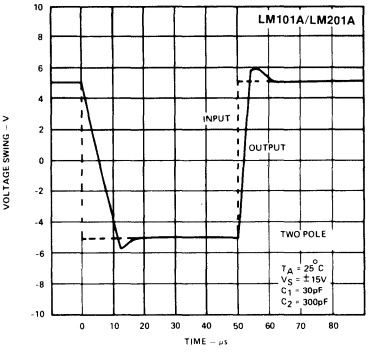
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE

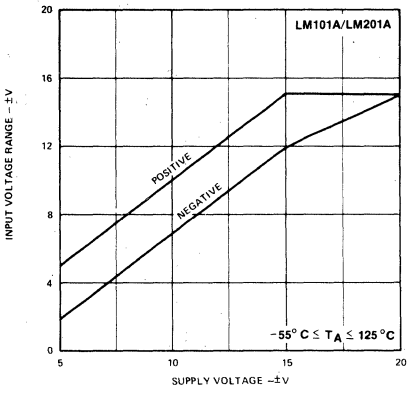


VOLTAGE FOLLOWER PULSE RESPONSE

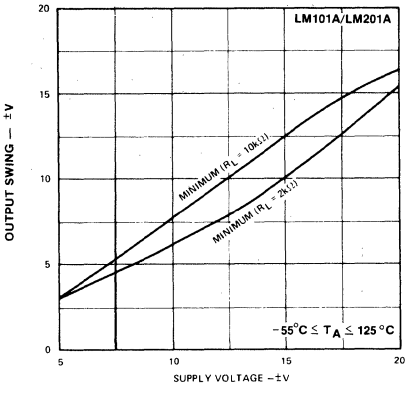


GUARANTEED PERFORMANCE CHARACTERISTICS

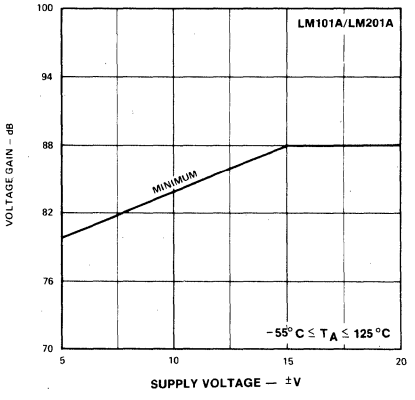
INPUT VOLTAGE RANGE



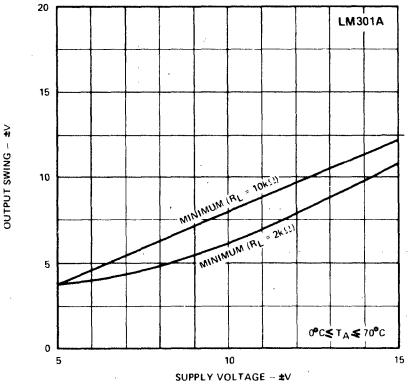
OUTPUT SWING



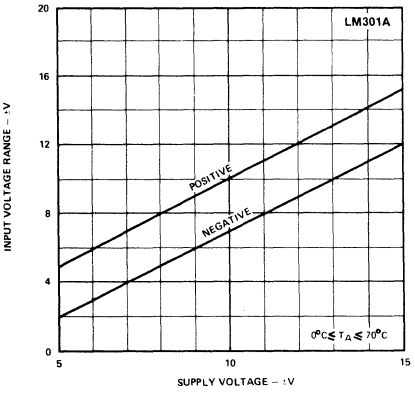
VOLTAGE GAIN



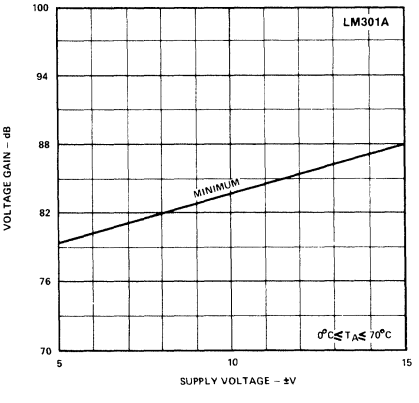
OUTPUT SWING



INPUT VOLTAGE RANGE



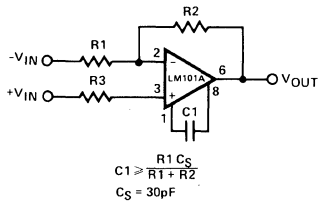
VOLTAGE GAIN



LM101/A/201/A/301/A, LH2101A/2201A/2301A-F,N,N-14,T

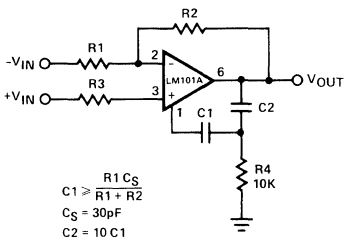
COMPENSATION CIRCUITS

SINGLE POLE COMPENSATION

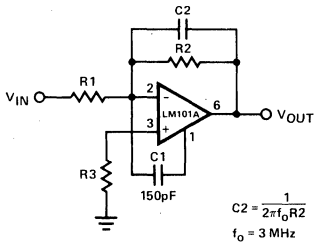


NOTE: Pin connections shown are for T package.

TWO POLE COMPENSATION

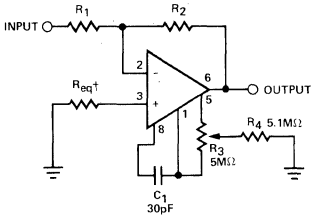


FEED FORWARD COMPENSATION



TYPICAL APPLICATIONS

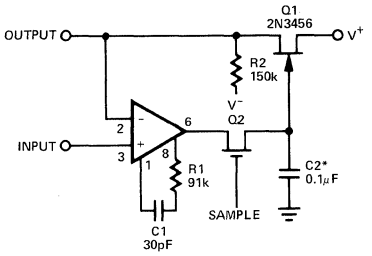
INVERTING AMPLIFIER WITH BALANCING CIRCUIT



†May be zero or equal to parallel combination of R_1 and R_2 for minimum offset.

NOTE: Pin numbers shown refer to T or N package only.

LOW DRIFT SAMPLE AND HOLD



*Polycarbonate Dielectric Capacitor

NOTE: Pin numbers shown refer to T or N package only.

DESCRIPTION

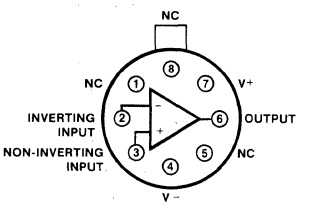
The LM107/207/307 is a general purpose internally compensated operational amplifier. Advanced processing techniques provide input currents which are an order of magnitude lower than the μA709. Standard pin out allows plug in replacement for the μA709, LM101, LM101A, and the μA741.

FEATURES

- **3mV max offset voltage over temp**
- **100nA max input current over temp**
- **20nA max input offset current over temp**
- **Offsets guaranteed over common mode range**
- **Input/output short circuit protected**
- **Mil std 883A,B,C available**

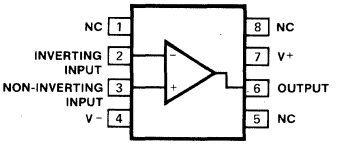
PIN CONFIGURATIONS

T PACKAGE



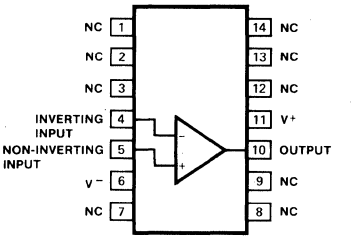
ORDER PART NO.
LM107T/LM207T/LM307T

N PACKAGE



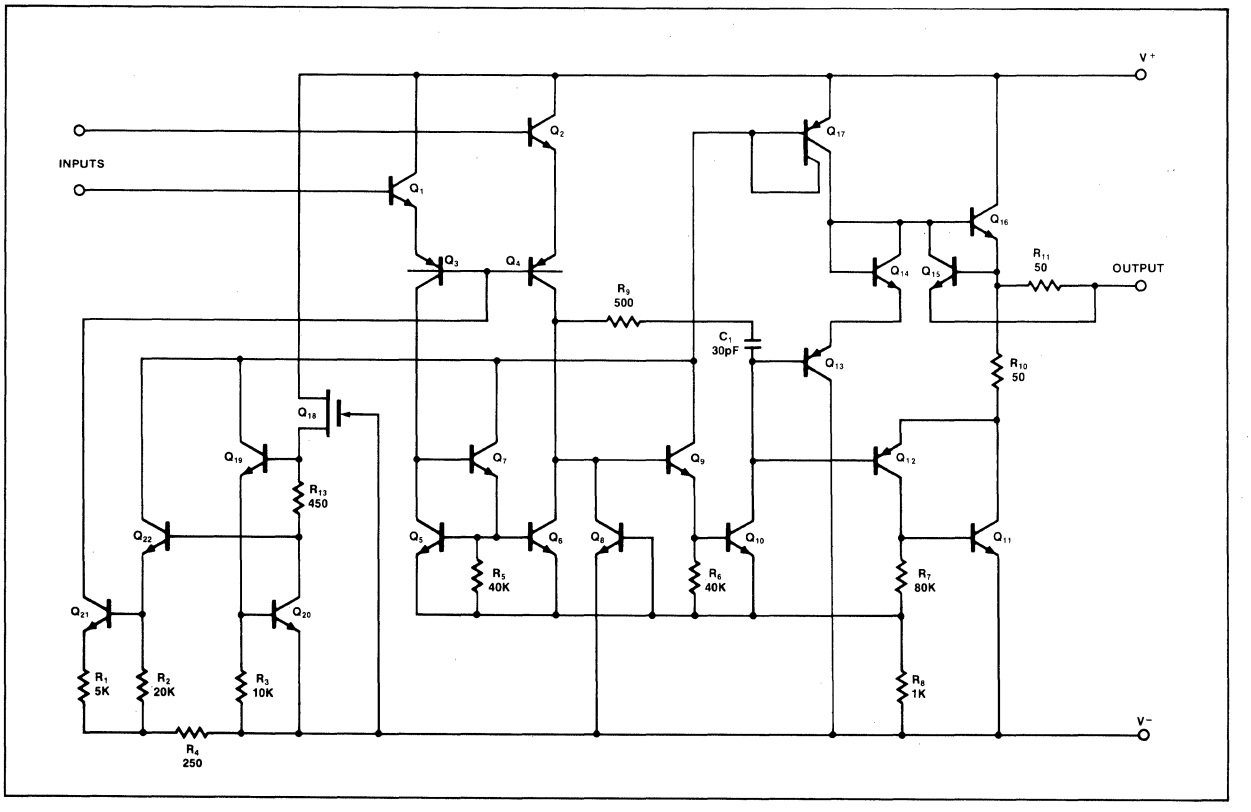
ORDER PART NO.
LM107N/LM207N/LM307N

F PACKAGE



ORDER PART NO.
LM107F/LM207F/LM307F

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
LM107	±22	V
LM307	±18	V
Power dissipation	500	mW
Differential input voltage	±30	V
Input voltage	±15	V
Output short circuit duration	Indefinite	
Operating temperature range		
LM107	-55 to +125	°C
LM207	-25 to +85	°C
LM307	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature		
(soldering, 60sec)	300	°C

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $\pm5V \leq V_S \leq \pm20V$ unless otherwise specified.

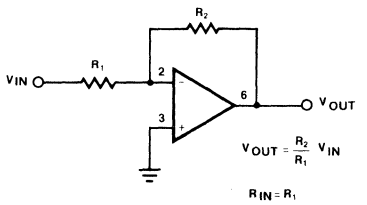
PARAMETER		TEST CONDITIONS	LM107/LM207			LM307[4]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \leq 10k\Omega$		0.7	2.0				mV
		$R_S \leq 10k\Omega$, over temp.			3.0				mV
		$R_S \leq 50k\Omega$					2.0	7.5	mV
		$R_S \leq 50k\Omega$, over temp.						10	mV
V_{OS}	Drift	$R_S = 0\Omega$, over temp.		3.0	15		6.0	30	μV/°C
I_{OS}	Offset current			1.5	10		3	50	nA
		Over temp.			20			70	nA
I_{OS}	Drift	$25°C \leq T_A \leq T_{max}$		0.01	0.1		0.01	0.3	nA/°C
		$T_{min} \leq T_A \leq 25°C$		0.02	0.2		0.02	0.6	nA/°C
I_{BIAS}	Input current			30	75		70	250	nA
		Over temp.			100			300	nA
V_{CM}	Common mode voltage range	$V_S = \pm20V$, over temp.	±15						V
		$V_S = \pm15V$, over temp.				±12			V
CMRR	Common mode rejection ratio	$R_S \leq \pm10k$, over temp.	80	96					dB
		$R_S \leq 50k$, over temp.					70	90	dB
R_{IN}	Input resistance		1.5	4		0.5	2		MΩ
A_{VOL}	Large signal voltage gain	$R_L \geq 2k\Omega$, $V_{OUT} \pm10V$, $V_S = \pm15V$	50	160		25	160		V/mV
		$R_L \geq 2k\Omega$, $V_{OUT} \pm10V$, $V_S = \pm15V$, over temp.	25			15			V/mV
	Supply current	$T_A = +125°C$, $V_S = \pm20V$		1.2	2.5				mA

NOTES

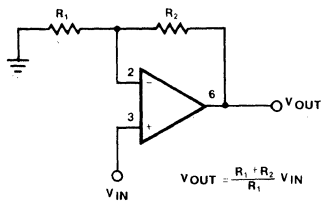
1. The maximum junction temperature of the LM1XX is 150°C, while that of the LM2XX is 100°C. For operating at elevated temperatures, devices must be derated based on the thermal resistance of the package as given in the package information section.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Continuous short-circuit is allowed for case temperatures to 70°C and ambient temperatures to 55°C.
4. All specifications shown for LM307 are $\pm5V \leq V_S \leq \pm15V$.

TYPICAL APPLICATIONS

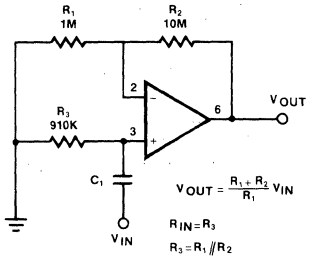
INVERTING AMPLIFIER



NON-INVERTING AMPLIFIER



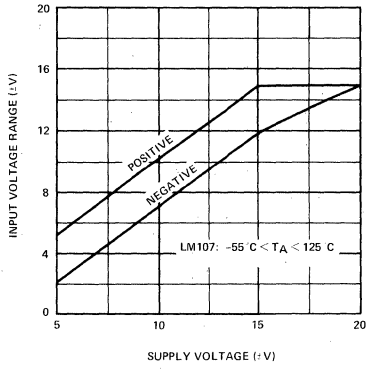
NON-INVERTING AC AMPLIFIER



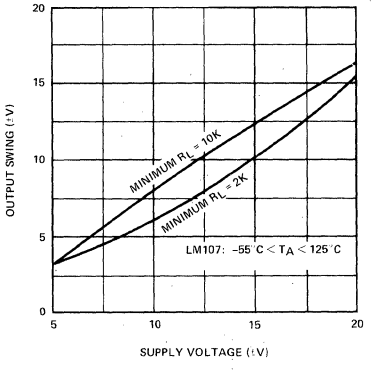
TYPICAL PERFORMANCE CHARACTERISTICS

LM107/LM207

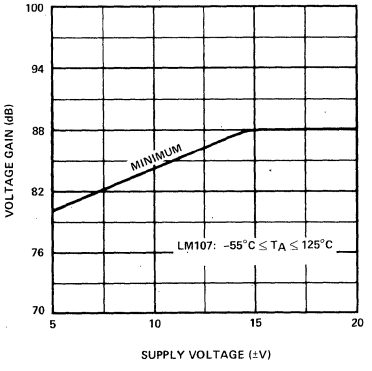
INPUT VOLTAGE RANGE



OUTPUT SWING

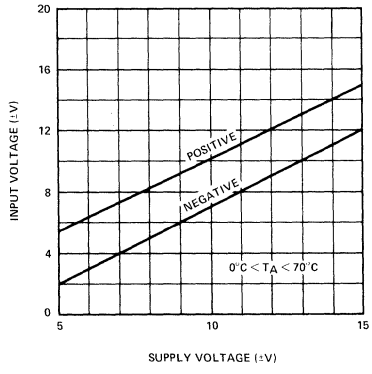


VOLTAGE GAIN

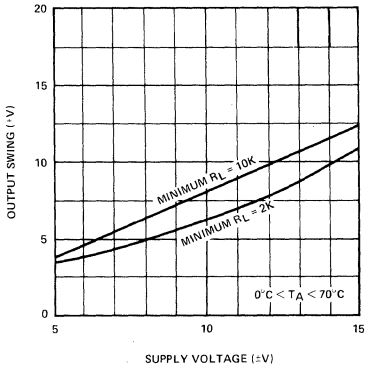


LM307

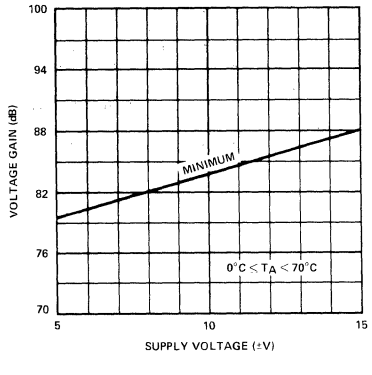
INPUT VOLTAGE RANGE



OUTPUT SWING

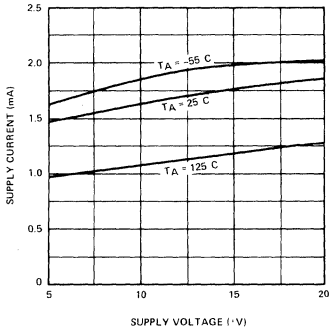


VOLTAGE GAIN

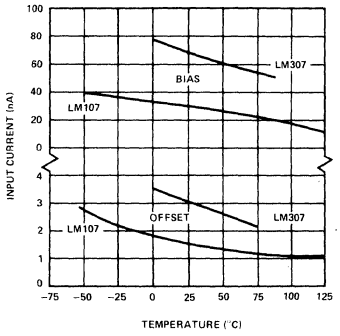


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

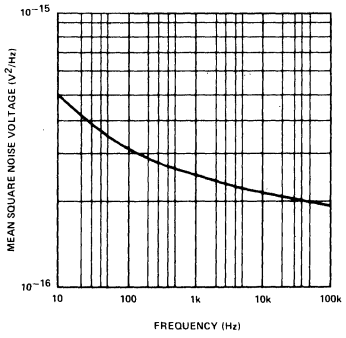
SUPPLY CURRENT



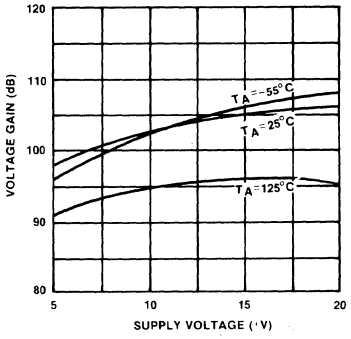
INPUT CURRENT



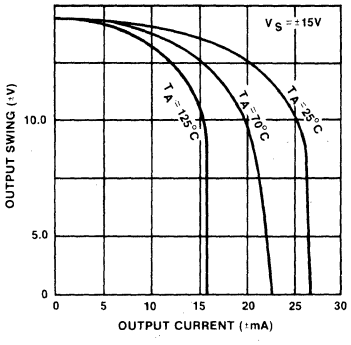
INPUT NOISE VOLTAGE



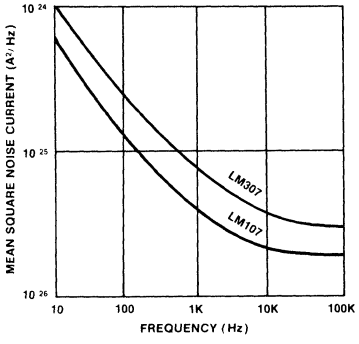
VOLTAGE GAIN



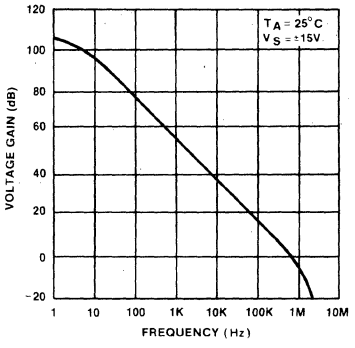
CURRENT LIMITING



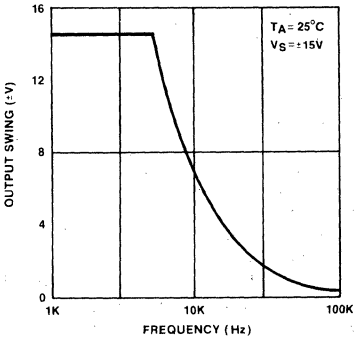
INPUT NOISE CURRENT



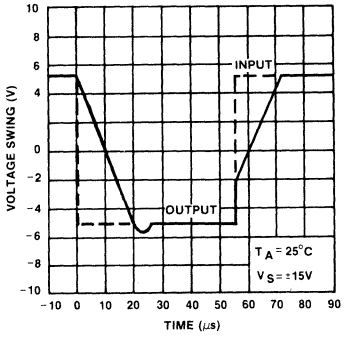
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE



VOLTAGE FOLLOWER PULSE RESPONSE



LM108/A/208/A/308/A-F,N,N-14,T
LH2108/A/2208/A/2308/A-F,N,N-14,T

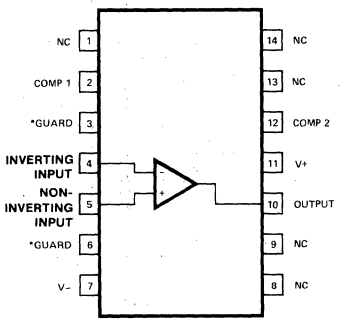
DESCRIPTION

The LM108/108A series are precision operational amplifiers having specifications a factor of ten better than FET amplifiers over their operating temperature range. In addition to low input currents, these devices have extremely low offset voltage, making it possible in most cases, to eliminate offset adjustments.

The LH2108 series are hybrids featuring two LM108A type dice in the same hermetic package. The electrical parameters are the same as the single amplifier.

PIN CONFIGURATIONS

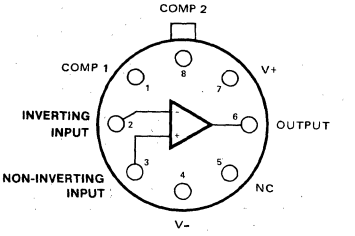
F PACKAGE



ORDER PART NO.
LM108AF, LM208AF, LM308AF
LM108F, LM208F, LM308F

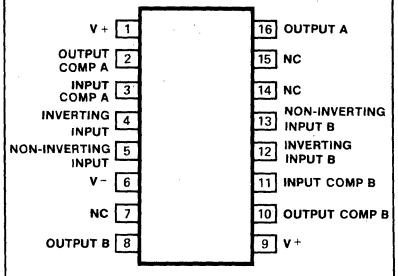
*Unused pin (no internal connection) to allow for input anti-leakage.

T PACKAGE



ORDER PART NO.
LM108AT, LM208AT, LM308AT,
LM108T, LM208T, LM308T

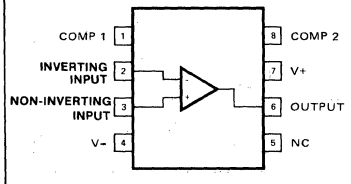
F PACKAGE



ORDER PART NO.

LH2108F	LH2108AF
LH2208F	LH2208AF
LH2308F	LH2308AF

N PACKAGE

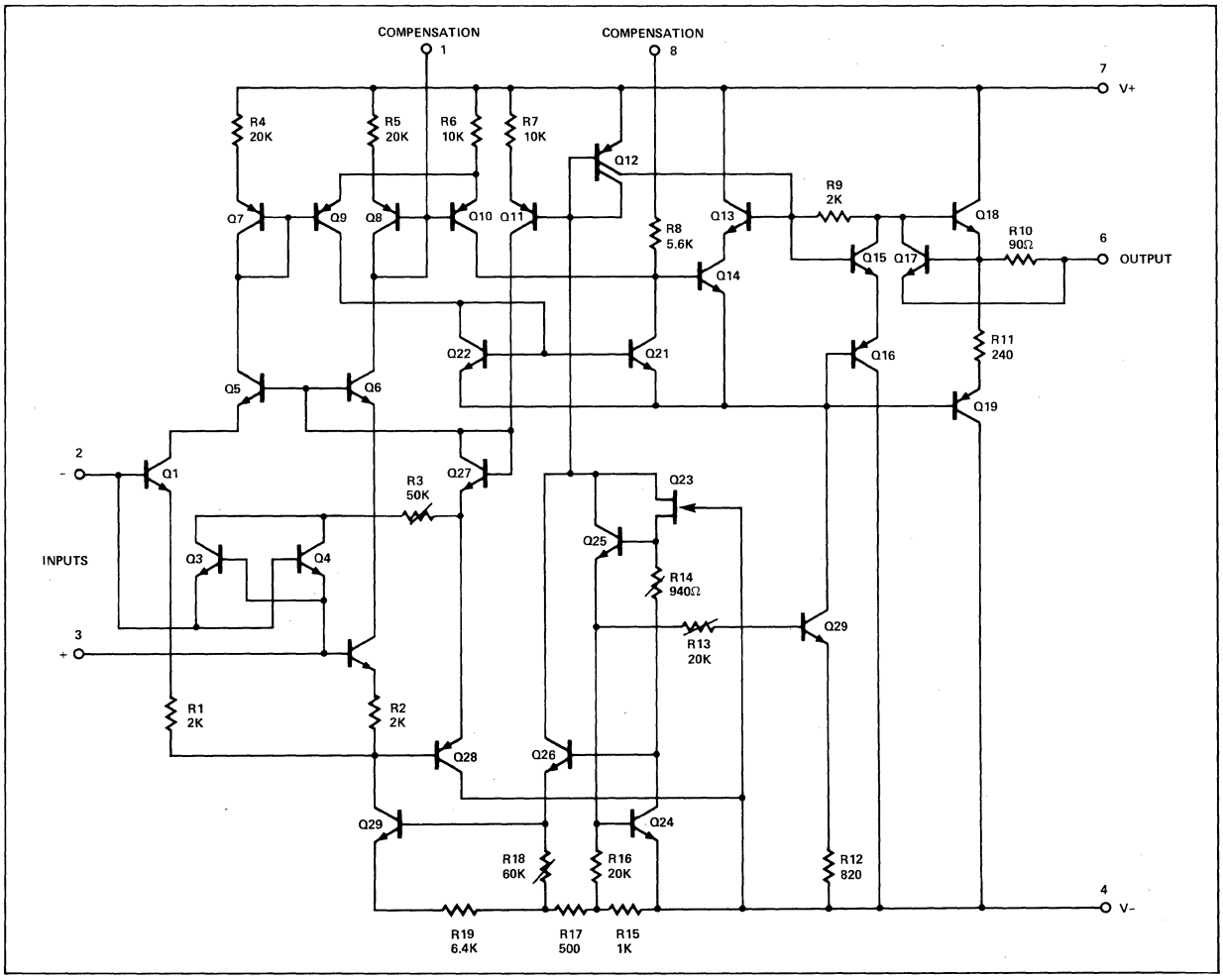


ORDER PART NO.
LM308AN, LM108N, LM208N, LM308N

FEATURES	LM108/208	LM308	LM108A/208A/308A
Maximum input bias current	3.0nA over temp.	7.0nA	3.0nA over temp.
Offset current	Less than 400pA over temp.	Less than 1.0nA	Less than 400pA over temp.
Supply current (even in saturation)	300μA	300μA	300μA
Guaranteed drift characteristics			5μV/°C
Offset voltage guaranteed Low current error LM108, 208, 308, 108A Mil std 883A, B,C available LM108A Mil std M38510 (JAN) planned LH2108A series—military qualification pending			Less than 0.5mV

LM108/A/208/A/308/A-F,N,N-14,T
LH2108/A/2208/A/2308/A-F,N,N-14,T

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING		UNIT
	LH2108/LH2208 LH2108A/LH2208A LM108A/208A/ 108/208	LM308A/308 LH2308A/LH2308	
Supply voltage	±20	±18	V
Power dissipation[1,4]	500	500	mW
Differential input current[2]	±10	±10	mA
Input voltage[3]	±15	±15	V
Output short-circuit duration	Continuous	Continuous	
Operating temperature range			
LM108, LH2108	-55 to +125	0 to +70	°C
LM208, LH2208	-25 to +85		°C
Storage temperature range	-65 to +150	-65 to +150	°C
Lead temperature (soldering 10sec)	+300	+300	°C

NOTES

1. The maximum junction temperature of the LM108/108A is 150°C, while that of the LM208/208A is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.
2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.
3. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
4. The maximum junction temperature of the LM308 is 85°C. For operation at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $\pm5V \leq V_S \leq \pm20V$ unless otherwise specified.[1,2]

PARAMETER		TEST CONDITIONS	LM108/LH2108			LM208/LH2208			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \leq 10k\Omega$ $R_S \leq 10k\Omega$, over temp.		.7	2.0 3.0		0.7	2.0 3.0	mV mV
V_{OS}	Drift	$R_S = 0\Omega$, over temp.		3.0	15		3.0	15	μV/°C
I_{OS}	Offset current	 Over temp.		0.05	0.2 0.4		0.05	0.2 0.4	nA nA
I_{OS}	Drift	Over temp.		0.5	2.5		0.5	2.5	pA/°C
I_{BIAS}	Input current	 Over temp.		0.8	2.0 3.0		0.8	2.0 3.0	nA nA
V_{CM}	Common mode voltage range	Over temp.	±13.5			±13.5			V
CMRR	Common mode rejection ratio	$R_S \leq 10k\Omega$, over temp. $R_S \leq 10k\Omega$, $-25 \leq T_A \leq 85°C$	85	100		 85	 100		dB dB
R_{IN}	Input resistance		30	70		30	70		MΩ
V_{OUT}	Output voltage swing	$R_L = 10k\Omega$, over temp.	±13	±14		±13	±14		V
I_{CC}	Supply current	 $T_A = +125°C$		0.3 0.15		0.6 0.4	0.3 0.15	0.6 0.4	mA mA
P_{SRR}	Supply voltage rejection ratio	$R_S \leq 10k\Omega$, over temp. $\pm5V \leq V_S \leq \pm15V$, over temp.	80	96		80	96		dB
	Average temperature Coefficient of input Offset voltage[2]	$\pm5V \leq V_S \leq \pm15V$, over temp.		3.0	15		3.0	15	μV/°C
	Coefficient of input Offset current	Over temp. $\pm5V \leq V_S \leq \pm15V$		0.5	2.5		0.5	2.5	pA/°C

NOTES

1. The maximum junction temperature of the LM1XX is 150°C, while that of the LM2XX is 200°C. For operating at elevated temperatures, devices must be derated based on the thermal resistance of the package as given in the package information section.
2. The LM108A has a guaranteed offset voltage less than 0.5mV at 25°C and 1.0mV for $-55°C \leq 125°C$ and $V_S = \pm15V$. The average temperature coefficient of input offset voltage is guaranteed to be less than 5μV/°C for these same conditions.

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $\pm5V \leq V_S \leq \pm20V$ unless otherwise specified.[1,2]

PARAMETER		TEST CONDITIONS	LM308/LH2308			LM108A/LH2108A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \leq 10k\Omega$					0.3	0.5	mV
		$R_S \leq 10k\Omega$, over temp.						1.0	mV
		$R_S \leq 10k\Omega$, $\pm5V \leq V_S \leq \pm15V$		2.0	7.5				mV
		$R_S \leq 10k\Omega$, $\pm5V \leq V_S \leq \pm15V$, over temp.			10				mV
V_{OS}	Drift	$R_S = 0\Omega$, over temp.					1.0	5.0	$\mu V/°C$
		$R_S = 0\Omega$, $\pm5V \leq V_S \leq \pm15V$, over temp.			10				$\mu V/°C$
I_{OS}	Offset current						0.05	0.2	nA
		Over temp.						0.4	nA
		$\pm5V \leq V_S \leq \pm15V$		0.2	1				nA
		$\pm5V \leq V_S \leq \pm15V$, over temp.			1.5				nA
I_{OS}	Drift	Over temp.					0.5	2.5	pA/°C
		$\pm5V \leq V_S \leq \pm15V$, over temp.		2.0	10				pA/°C
I_{BIAS}	Input current						0.8	2.0	nA
		Over temp.						3.0	nA
		$\pm5V \leq V_S \leq \pm15V$		1.5	7.0				nA
		$V_S = \pm15V$, over temp.			10				nA
V_{CM}	Common mode voltage range	Over temp.				±13.5			V
		$\pm5V \leq V_S \leq \pm15V$, over temp.	±14V						V
CMRR	Common mode rejection ratio	$R_S \leq 10k\Omega$, over temp.				96	110		dB
		$R_S \leq 10k\Omega$, $\pm5V \leq V_S \leq \pm15V$, over temp.	80	100					dB
R_{IN}	Input resistance		10	40		30	70		MΩ
V_{OUT}	Output voltage swing	$R_L = 10k\Omega$, over temp.				±13	±14		V
		$\pm5V \leq V_S \leq \pm15V$, over temp.	±13	±14					V
I_{CC}	Supply current						0.3	0.6	mA
		$T_A = +125°C$					0.15	0.4	mA
		$V_S = \pm15V$		0.3	0.8				mA
P_D	Power consumption	$\pm5V \leq V_S \leq \pm15V$		9.0	24				mW
P_{SRR}	Supply voltage rejection ratio	$R_S \leq 10k\Omega$, over temp.				96	110		dB
		$\pm5V \leq V_S \leq \pm15V$, over temp.	80	96					dB
	Average temperature	$\pm5V \leq V_S \leq \pm15V$, over temp.					1.0	5.0	$\mu V/°C$
	Coefficient of input			6.0	30				$\mu V/°C$
	Offset voltage[2]								$\mu V/°C$
	Coefficient of input	Over temp.					0.5	2.5	pA/°C
	Offset current	$\pm5V \leq V_S \leq \pm15V$		2.0	10				pA/°C

NOTES

1. The maximum junction temperature of the LM1XX is 150°C, while that of the LM2XX is 200°C. For operating at elevated temperatures, devices must be derated based on the thermal resistance of the package as given in the package information section.
2. The LM108A has a guaranteed offset voltage less than 0.5mV at 25°C and 1.0mV for $-55°C \leq 125°C$ and $V_S = \pm15V$. The average temperature coefficient of input offset voltage is guaranteed to be less than $5\mu V/°C$ for these same conditions.

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $\pm5V \leq V_S \leq \pm20V$ unless otherwise specified.[1,2]

PARAMETER		TEST CONDITIONS	LM208A/LH2208A			LM308A/LH2308A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \leq 10k\Omega$		0.3	0.5		0.3	0.5	mV
		$R_S \leq 10k\Omega$, over temp.			1.0			.75	mV
V_{OS}	Drift	$R_S = 0\Omega$, over temp.		1.0	5.0		1.0	5.0	$\mu V/°C$
I_{OS}	Offset current			0.05	0.2			1	nA
		Over temp.			0.4			1.5	nA
I_{OS}	Drift	Over temp.		0.5	2.5		2.0	10	pA/°C
I_{BIAS}	Input current			0.8	2.0		1.5	7.0	nA
		Over temp.			3.0			10	nA
V_{CM}	Common mode voltage range	Over temp.	±13.5			±14			V
		$\pm5V \leq V_S \leq \pm15V$, over temp.							V
CMRR	Common mode rejection ratio								
		$R_S \leq 10k\Omega$, $-25 \leq T_A \leq 85°C$	96	110					dB
		$R_S \leq 10k\Omega$, $\pm5V \leq V_S \leq \pm15V$, over temp.				96	110		dB
R_{IN}	Input resistance		30	70					MΩ
		$R_S \leq 10k\Omega$, $\pm5V \leq V_S \leq \pm15V$				10	40		MΩ
V_{OUT}	Output voltage swing	$R_L = 10k\Omega$, over temp.	±13	±14					V
		$\pm5V \leq V_S \leq \pm15V$, over temp.				±13	±14		V
I_{CC}	Supply current			0.3	0.6				mA
		$T_A = +125°C$		0.15	0.4				mA
		$V_S = \pm15V$					0.3	0.8	mA
P_D	Power consumption	$\pm5V \leq V_S \leq \pm15V$					9.0	24	mW
P_{SRR}	Supply voltage rejection ratio	$R_S \leq 10k\Omega$, over temp.	96	110					dB
		$\pm5V \leq V_S \leq \pm15V$, over temp.				96	110		dB
	Average temperature	$\pm5V \leq V_S \leq \pm15V$, over temp.		1.0	5.0				$\mu V/°C$
	Coefficient of input						1.0	5.0	$\mu V/°C$
	Offset voltage[2]								
	Coefficient of input	Over temp.		0.5	2.5				pA/°C
	Offset current	$\pm5V \leq V_S \leq \pm15V$					2.0	10	pA/°C

NOTES

1. The maximum junction temperature of the LM1XX is 150°C, while that of the LM2XX is 200°C. For operating at elevated temperatures, devices must be derated based on the thermal resistance of the package as given in the package information section.
2. The LM108A has a guaranteed offset voltage less than 0.5mV at 25°C and 1.0mV for $-55°C \leq 125°C$ and $V_S = \pm15V$. The average temperature coefficient of input offset voltage is guaranteed to be less than $5\mu V/°C$ for these same conditions.

LM108/A/208/A/308/A-F,N,N-14,T
LH2108/A/2208/A/2308/A-F,N,N-14,T

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $\pm5V \leq V_S \leq \pm20V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	LM108/LH2108			LM208/LH2208			LM308/LH2308			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
A_{VOL} Large signal voltage gain[1]	$R_L \geq 10k\Omega$	50	300		50	300					V/mV
	Over temp.	25			25						V/mV
	$V_S = 15V$, $V_{OUT} = \pm10V$, $R_L \geq 10k$							25	300		V/mV
	Over temp.							15			V/mV

NOTE

1. The maximum junction temperature of the LM1XX is 150°C, while that of the LM2XX is 200°C. For operating at elevated temperatures, devices must be derated based on the thermal resistance of the package as given in the package information section.

AC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $\pm5V \leq V_S \leq \pm20V$ unless otherwise specified.

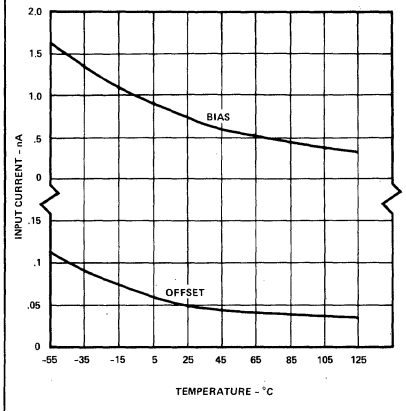
PARAMETER	TEST CONDITIONS	LM108A/LH2108A			LM208A/LH2208A			LM308A/LH2308A			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
A_{VOL} Large signal voltage gain[1]	$R_L \geq 10k\Omega$	80	300		80	300					V/mV
	Over temp.	40			40						V/mV
	$V_S = 15V$, $V_{OUT} = \pm10V$, $R_L \geq 10k$							80	300		V/mV
	Over temp.							60			V/mV

NOTE

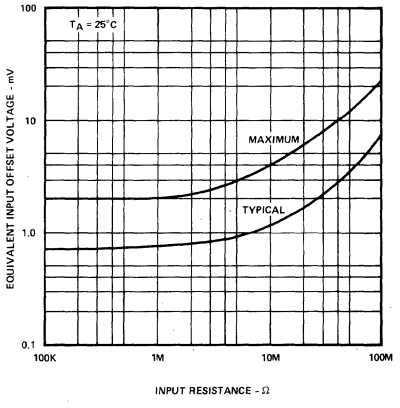
1. The maximum junction temperature of the LM1XX is 150°C, while that of the LM2XX is 200°C. For operating at elevated temperatures, devices must be derated based on the thermal resistance of the package as given in the package information section.

TYPICAL PERFORMANCE CHARACTERISTICS LM108/208

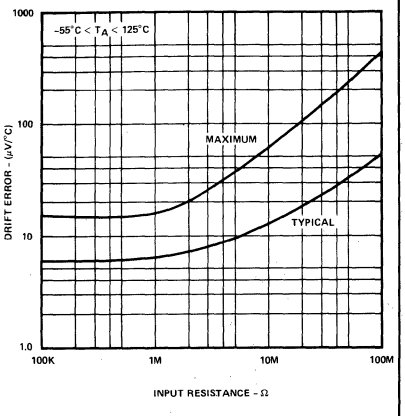
INPUT CURRENTS



OFFSET ERROR

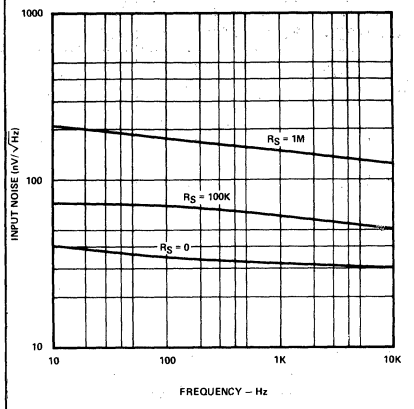


DRIFT ERROR

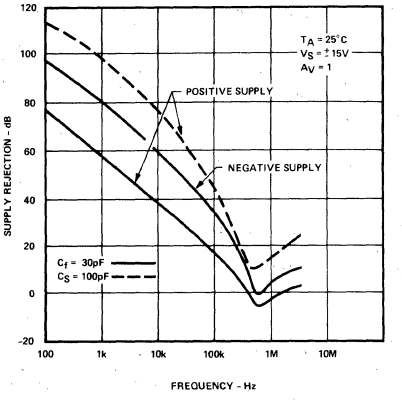


TYPICAL PERFORMANCE CHARACTERISTICS LM108/208 (Cont'd)

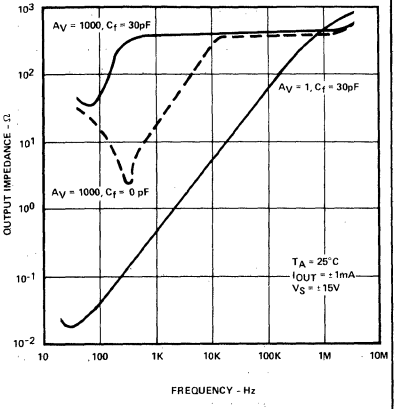
INPUT NOISE VOLTAGE



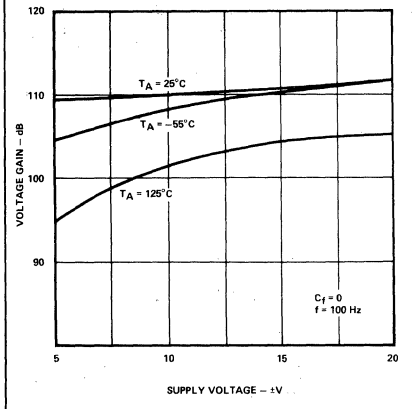
POWER SUPPLY REJECTION



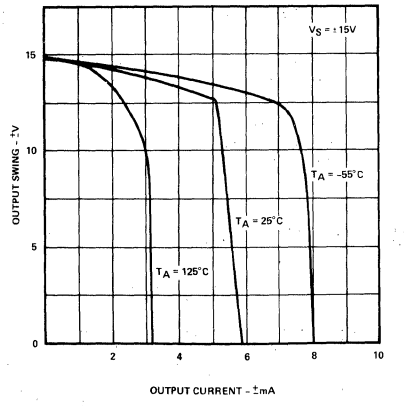
CLOSED LOOP OUTPUT IMPEDANCE



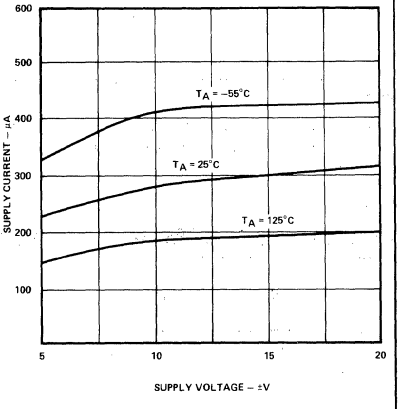
VOLTAGE GAIN



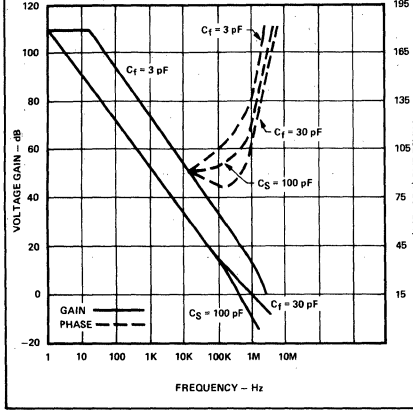
OUTPUT SWING



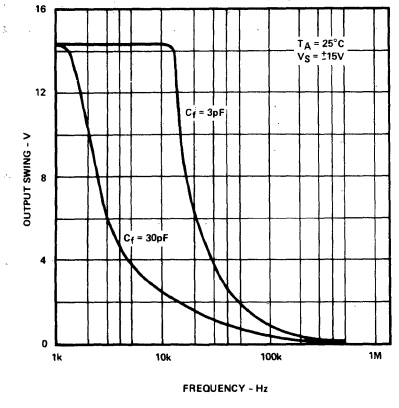
SUPPLY CURRENT



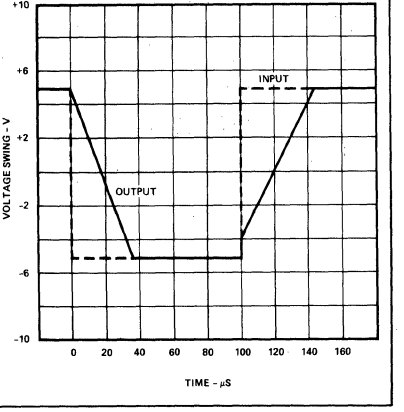
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE



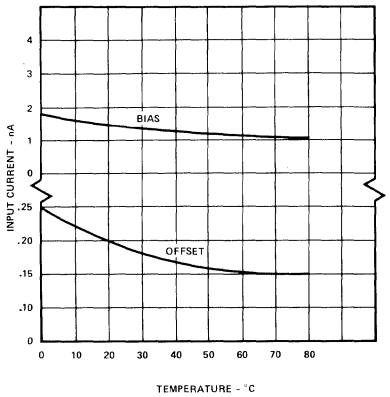
VOLTAGE FOLLOWER PULSE RESPONSE



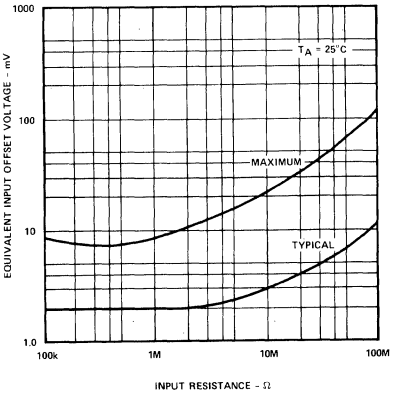
LM108/A/208/A/308/A-F,N,N-14,T
LH2108/A/2208/A/2308/A-F,N,N-14,T

TYPICAL PERFORMANCE CHARACTERISTICS LM308

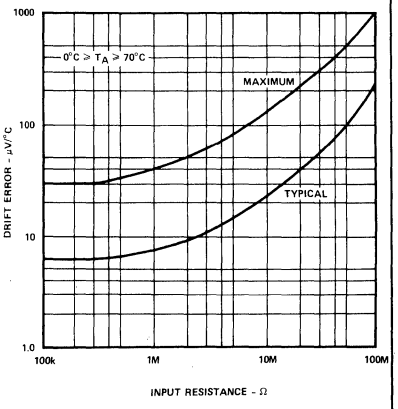
INPUT CURRENTS



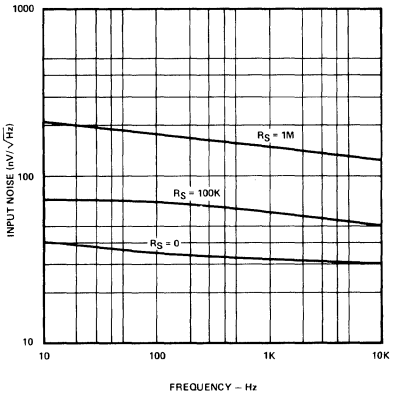
OFFSET ERROR



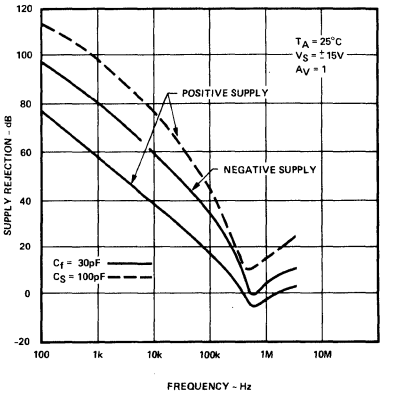
DRIFT ERROR



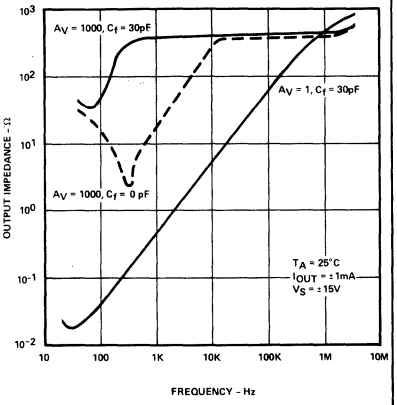
INPUT NOISE VOLTAGE



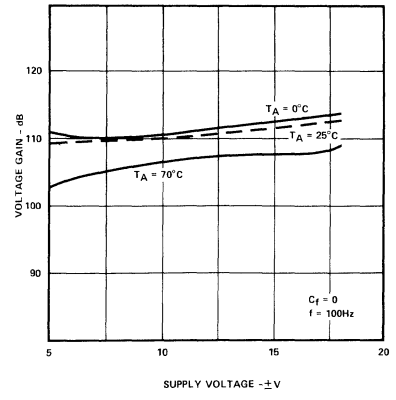
POWER SUPPLY REJECTION



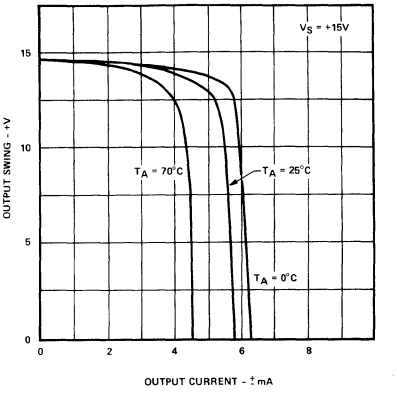
CLOSED LOOP OUTPUT IMPEDANCE



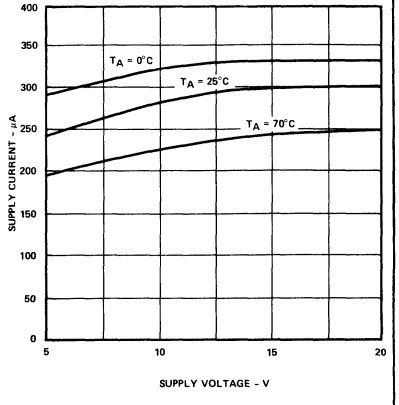
VOLTAGE GAIN



OUTPUT SWING

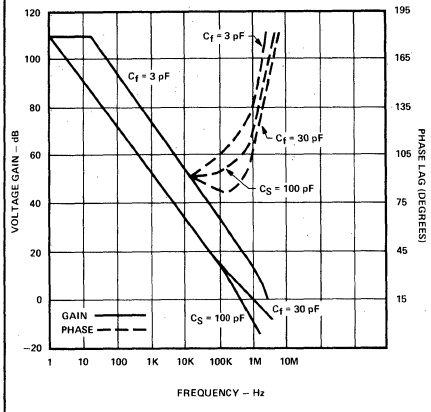


SUPPLY CURRENT

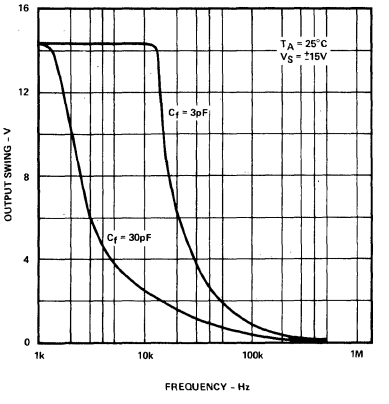


TYPICAL PERFORMANCE CHARACTERISTICS LM308 (Cont'd)

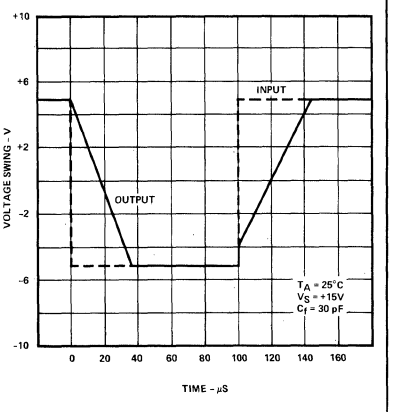
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE

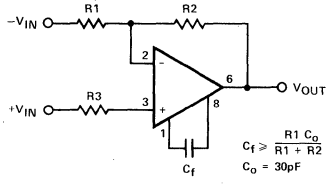


VOLTAGE FOLLOWER PULSE RESPONSE



TEST LOAD CIRCUITS

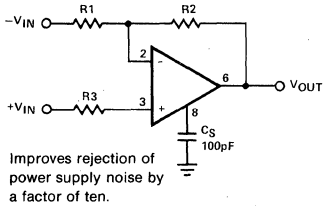
STANDARD COMPENSATION CIRCUIT



$C_f \geq \frac{R1\ C_o}{R1 + R2}$

C_o = 30pF

ALTERNATE FREQUENCY COMPENSATION



Improves rejection of power supply noise by a factor of ten.

LM124/A/224/A/324/A/SA534-F,N-14,T
LM158/A/258/A/358A-F,N,T

DESCRIPTION

The LM124/SA534 series consists of four independent, high gain, internally frequency compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages.

The LM158 series consists of two operational amplifiers designed as above. Operation from dual supplies is also possible for both series and the low power supply current drain is independent of the magnitude of the power supply voltage.

FEATURES

- **Internally frequency compensated for unity gain**
- **Large dc voltage gain—(100dB)**
- **Wide bandwidth (unity gain)—1MHz (temperature compensated)**
- **Wide power supply range**
  Single supply—(3Vdc to 30Vdc) or dual supplies—(±1.5Vdc to ±15Vdc)
- **Very low supply current drain—essentially independent of supply voltage (1mW/op amp at +5Vdc)**
- **Low input biasing current—(45nAdc temperature compensated)**
- **Low input offset voltage—(2mVdc) and offset current—(5nAdc)**
- **Differential input voltage range equal to the power supply voltage**
- **Large output voltage—(0Vdc to V+—1.5Vdc swing)**
- **LM124 Mil std 883A,B,C available**

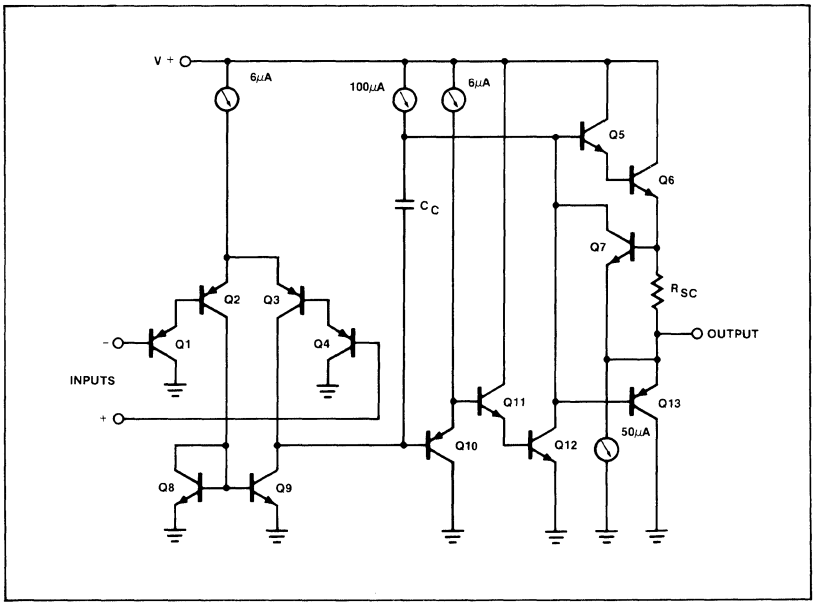
UNIQUE FEATURES

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

The unity gain cross frequency is temperature compensated.

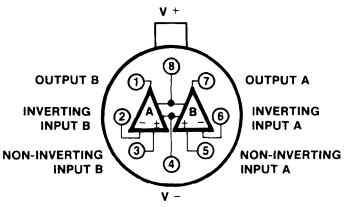
The input bias current is also temperature compensated.

EQUIVALENT SCHEMATIC



PIN CONFIGURATIONS

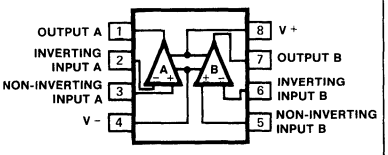
T PACKAGE



ORDER PART NO.

LM158T	LM258T
LM358T	LM158AT
LM258AT	LM358AT

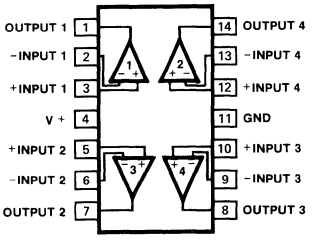
N PACKAGE



ORDER PART NO.

LM158N	LM258N
LM358N	LM158AN
LM258AN	LM358AN

F,N-14 PACKAGE



ORDER PART NO.

LM124N	LM224N	LM324N
LM124F	LM224F	LM324F
LM124AN	LM224AN	LM324AN
LM124AF	LM224AF	LM324AF
SA534N	SA534F	

LM124/A/224/A/324/A/SA534-F,N-14,T
LM158/A/258/A/358A-F,N,T

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V+	Supply voltage	32 or ±16	Vdc
	Differential input voltage	32	Vdc
	Input voltage	-0.3 to +32	Vdc
	Power dissipation[1]		
	T package	680	mW
	N package	570	mW
	F package	900	mW
	Output short-circuit to GND		
	1 amplifier[2]	Continuous	
	V+ < 15Vdc and T_A = 25°C		
	Input current (V_{IN} < -0.3V)[3]	50	mA
	Operating temperature range		
	LM324A, LM324, LM358	0 to +70	°C
	LM224A, LM224, LM258	-25 to +85	°C
	SA534	-40 to +85	°C
	LM124A, LM124, LM158	-55 to +125	°C
	Storage temperature range	-65 to +150	°C
	Lead temperature (soldering, 10sec)	300	°C

NOTES

1. For operating at high temperatures, all devices must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. LM124/224 and LM158/258 can be derated based on a +150°C maximum junction temperature.
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15Vdc continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
3. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the input lines.

LM124/A/224/A/324/A/SA534-F,N-14,T
LM158/A/258/A/358A-F,N,T

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V+ = 5V$, $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	LM124A			LM224A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage[1]	$R_S \leq 10k\Omega$		1	2		1	3	mV
		$R_S \leq 10k\Omega$, over temp.			4			4	mV
V_{OS}	Drift	$R_S = 0\Omega$, over temp.		7	20		7	20	$\mu V/°C$
I_{BIAS}	Input current[2]	$I_{IN}(+) - I_{IN}(-)$		20	50		40	80	nA
		$I_{IN}(+) - I_{IN}(-)$, over temp.		40	100		40	100	nA
I_{OS}	Offset current	$I_{IN}(+) - I_{IN}(-)$		2	10		2	15	nA
		$I_{IN}(+) - I_{IN}(-)$, over temp.			30			30	nA
I_{OS}	Drift	over temp.		10	200		10	200	pA/°C
V_{CM}	Common mode voltage range[3]	V+ = 30V	0		V+-1.5	0		V+-1.5	V
		V+ = 30V, over temp.	0		V+-2	0		V+-2	V
C_{MRR}	Common mode rejection ratio		70	85		70	85		dB
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$, V+ = +30V, over temp.	26			26			V
V_{OH}		$R_L \leq 10k\Omega$, over temp	27	28		27	28		V
V_{OL}		$R_L \leq 10k\Omega$, V+ = 5V, over temp.		5	20		5	20	V
I_{CC}	Supply current	$R_L = \infty$, $V_{CC} = 30V$, over temp.		1.5	3		1.5	3	mA
		$R_L = \infty$, on all op amps, over temp.		0.7	1.2		0.7	1.2	mA
A_{VOL}	Large signal voltage gain	V+ = +15V (for large V_O swing), $R_L \geq 2k\Omega$	50	100		50	100		V/mV
		V+ = +15V (for large V_O swing), $R_L \geq 2k\Omega$, over temp.	25			25			V/mV
	Amplifier-to-amplifier coupling[4]	f = 1kHz to 20kHz, input referred		-120			-120		dB
P_{SRR}		$R_S \leq 10k\Omega$	65	100		65	100		dB
	Output current								
	Source	$V_{IN}+ = +1Vdc$, $V_{IN}- = 0Vdc$, V+ = 15Vdc	20	40		20	40		mA
		$V_{IN}+ = +1Vdc$, $V_{IN}- = 0Vdc$, V+ = 15Vdc, over temp.	10	20		10	20		mA
	Sink	$V_{IN}- = +1Vdc$, $V_{IN}+ = 0Vdc$, V+ = 15Vdc	10	20		10	20		mA
		$V_{IN}- = +1Vdc$, $V_{IN}+ = 0Vdc$, V+ = 15Vdc, over temp.	10	15		5	8		mA
		$V_{IN}- = +1Vdc$, $V_O = 200mV$	12	50		12	50		μA
I_{SC}	Short circuit current[4]			40	60		40	60	mA
	Differential input voltage[6]				V+			V+	V

NOTES

1. $V_O \cong 1.4Vdc$, $R_S = 0\Omega$ with V+ from 5V to 30V and over full input common mode range (OVdc+ to V+ -1.5V).
2. The direction of the input current is out of the IC due to the pnp input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ -1.5, but either or both inputs can go to +32V without damage.
4. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15Vdc continous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
5. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ -1.5V, but either or both inputs can go to +32Vdc without damage.

LM124/A/224/A/324/A/SA534-F,N-14,T
LM158/A/258/A/358A-F,N,T

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V+ = 5V$, $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	LM324A			LM124/LM224/ LM158/LM258			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage[1]	$R_S \leq 10k\Omega$		2	3		±2	±5	mV
		$R_S \leq 10k\Omega$, over temp.			5			±7	mV
V_{OS}	Drift	$R_S = 0\Omega$, over temp.		7	30		7		μV/°C
I_{BIAS}	Input current[2]	$I_{IN}(+) - I_{IN}(-)$		45	100		45	150	nA
		$I_{IN}(+) - I_{IN}(-)$, over temp.		40	200		40	300	nA
I_{OS}	Offset current	$I_{IN}(+) - I_{IN}(-)$		5	30		±3	±30	nA
		$I_{IN}(+) - I_{IN}(-)$, over temp.			75			±100	nA
I_{OS}	Drift	over temp.		10	300		10		pA/°C
V_{CM}	Common mode voltage range[3]	V+ = 30V	0		V+-1.5	0		V+-1.5	V
		V+ = 30V, over temp.	0		V+-2	0		V+-2	V
C_{MRR}	Common mode rejection ratio		65	85		70	85		dB
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$, V+ = +30V, over temp.	26			26			V
V_{OH}		$R_L \leq 10k\Omega$, over temp	27	28		27	28		V
V_{OL}		$R_L \leq 10k\Omega$, V+ = 5V, over temp.		5	20		5	20	V
I_{CC}	Supply current	$R_L = \infty$, V_{CC} = 30V, over temp.		1.5	3		1.5	3	mA
		$R_L = \infty$, on all op amps, over temp.		0.7	1.2		0.7	1.2	mA
A_{VOL}	Large signal voltage gain	V+ = +15V (for large V_O swing), $R_L \geq 2k\Omega$	25	100		50	100		V/mV
		V+ = +15V (for large V_O swing), $R_L \geq 2k\Omega$, over temp.	15			25			V/mV
	Amplifier-to-amplifier coupling[4]	f = 1kHz to 20kHz, input referred		-120			-120		dB
P_{SRR}		$R_S \leq 10k\Omega$	65	100		65	100		dB
	Output current								
	Source	$V_{IN}+ = +1Vdc$, $V_{IN}- = 0Vdc$, V+ = 15Vdc	20	40		20	40		mA
		$V_{IN}+ = +1Vdc$, $V_{IN}- = 0Vdc$, V+ = 15Vdc, over temp.	10	20		10	20		mA
	Sink	$V_{IN}- = +1Vdc$, $V_{IN}+ = 0Vdc$, V+ = 15Vdc	10	20		10	20		mA
		$V_{IN}- = +1Vdc$, $V_{IN}+ = 0Vdc$, V+ = 15Vdc, over temp.	5	8		5	8		mA
		$V_{IN}- = +1Vdc$, $V_O = 200mV$	12	50		12	50		μA
I_{SC}	Short circuit current[4]			40	60		40	60	mA
	Differential input voltage[6]				V+			V+	V

NOTES

1. $V_O \cong 1.4Vdc$, $R_S = 0\Omega$ with V+ from 5V to 30V and over full input common mode range (0Vdc+ to V+ -1.5V).
2. The direction of the input current is out of the IC due to the pnp input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ -1.5, but either or both inputs can go to +32V without damage.
4. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15Vdc continous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
5. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ -1.5V, but either or both inputs can go to +32Vdc without damage.

LM124/A/224/A/324/A/SA534-F,N-14,T
LM158/A/258/A/358A-F,N,T

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V+ = 5V$, $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	LM324/LM358			SA534			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage[1]	$R_S \leq 10k\Omega$		±2	±7		±2	±7	mV
		$R_S \leq 10k\Omega$, over temp.			±9			±9	mV
V_{OS}	Drift	$R_S = 0\Omega$, over temp.		7			7		μV/°C
I_{BIAS}	Input current[2]	$I_{IN}(+) - I_{IN}(-)$		45	250		45	250	nA
		$I_{IN}(+) - I_{IN}(-)$, over temp.		40	500		40	500	nA
I_{OS}	Offset current	$I_{IN}(+) - I_{IN}(-)$		±5	±50		±5	±50	nA
		$I_{IN}(+) - I_{IN}(-)$, over temp.			±150			±150	nA
I_{OS}	Drift	over temp.		10			10		pA/°C
V_{CM}	Common mode voltage range[3]	$V+ = 30V$	0		V+-1.5	0		V+-1.5	V
		$V+ = 30V$, over temp.	0		V+-2	0		V+-2	V
C_{MRR}	Common mode rejection ratio		65	70		65	70		dB
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$, $V+ = +30V$, over temp.	26			26			V
V_{OH}		$R_L \leq 10k\Omega$, over temp	27	28		27	28		V
V_{OL}		$R_L \leq 10k\Omega$, $V+ = 5V$, over temp.		5	20		5	20	V
I_{CC}	Supply current	$R_L = \infty$, $V_{CC} = 30V$, over temp.		1.5	3		1.5	3	mA
		$R_L = \infty$, on all op amps, over temp.		0.7	1.2		0.7	1.2	mA
A_{VOL}	Large signal voltage gain	$V+ = +15V$ (for large V_O swing), $R_L \geq 2k\Omega$	25	100		25	100		V/mV
		$V+ = +15V$ (for large V_O swing), $R_L \geq 2k\Omega$, over temp.	15			15			V/mV
	Amplifier-to-amplifier coupling[4]	f = 1kHz to 20kHz, input referred		-120			-120		dB
P_{SRR}		$R_S \leq 10k\Omega$	65	100		65	100		dB
	Output current								
	Source	$V_{IN}+ = +1Vdc$, $V_{IN}- = 0Vdc$, $V+ = 15Vdc$	20	40		20	40		mA
		$V_{IN}+ = +1Vdc$, $V_{IN}- = 0Vdc$, $V+ = 15Vdc$, over temp.	10	20		10	20		mA
	Sink	$V_{IN}- = +1Vdc$, $V_{IN}+ = 0Vdc$, $V+ = 15Vdc$	10	20		10	20		mA
		$V_{IN}- = +1Vdc$, $V_{IN}+ = 0Vdc$, $V+ = 15Vdc$, over temp.	5	8		5	8		mA
		$V_{IN}- = +1Vdc$, $V_O = 200mV$	12	50		12	50		μA
I_{SC}	Short circuit current[4]			40	60		40	60	mA
	Differential input voltage[6]				V+			V+	V

NOTES

1. $V_O \cong 1.4Vdc$, $R_S = 0\Omega$ with V+ from 5V to 30V and over full input common mode range (0Vdc+ to V+ -1.5V).
2. The direction of the input current is out of the IC due to the pnp input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ -1.5, but either or both inputs can go to +32V without damage.
4. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15Vdc continous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
5. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ -1.5V, but either or both inputs can go to +32Vdc without damage.

LM124/A/224/A/324/A/SA534-F,N-14,T
LM158/A/258/A/358A-F,N,T

DC ELECTRICAL CHARACTERISTICS

$V+ = 5V$, $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	LM158A			LM258A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage[1]	$R_S \leq 10k\Omega$		1	2		1	3	mV
		$R_S \leq 10k\Omega$, over temp.			4			4	mV
V_{OS}	Drift	$R_S = 0\Omega$, over temp.		7	15		7	15	$\mu V/°C$
I_{BIAS}	Input current[2]	$I_{IN}(+) - I_{IN}(-)$		20	50		40	80	nA
		$I_{IN}(+) - I_{IN}(-)$, over temp.		40	100		40	100	nA
I_{OS}	Offset current	$I_{IN}(+) - I_{IN}(-)$		2	10		2	15	nA
		$I_{IN}(+) - I_{IN}(-)$, over temp.			30			30	nA
I_{OS}	Drift	over temp.		10	200		10	200	pA/°C
V_{CM}	Common mode voltage range[3]	V+ = 30V	0		V+-1.5	0		V+-1.5	V
		V+ = 30V, over temp.	0		V+-2	0		V+-2	V
C_{MRR}	Common mode rejection ratio		70	85		70	85		dB
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$, V+ = +30V, over temp.	26			26			V
V_{OH}		$R_L \leq 10k\Omega$, over temp	27	28		27	28		V
V_{OL}		$R_L \leq 10k\Omega$, V+ = 5V, over temp.		5	20		5	20	V
I_{CC}	Supply current	$R_L = \infty$, V_{CC} = 30V, over temp.		1.5	3		1.5	3	mA
		$R_L = \infty$, on all op amps, over temp.		0.7	1.2		0.7	1.2	mA
A_{VOL}	Large signal voltage gain	V+ = +15V (for large V_O swing), $R_L \geq 2k\Omega$	50	100		50	100		V/mV
		V+ = +15V (for large V_O swing), $R_L \geq 2k\Omega$, over temp.	25			25			V/mV
	Amplifier-to-amplifier coupling[4]	f = 1kHz to 20kHz, input referred		-120			-120		dB
P_{SRR}		$R_S \leq 10k\Omega$	65	100		65	100		dB
	Output current								
	Source	$V_{IN}+ = +1Vdc$, $V_{IN}- = 0Vdc$, V+ = 15Vdc	20	40		20	40		mA
		$V_{IN}+ = +1Vdc$, $V_{IN}- = 0Vdc$, V+ = 15Vdc, over temp.	10	20		10	20		mA
	Sink	$V_{IN}- = +1Vdc$, $V_{IN}+ = 0Vdc$, V+ = 15Vdc	10	20		10	20		mA
		$V_{IN}- = +1Vdc$, $V_{IN}+ = 0Vdc$, V+ = 15Vdc, over temp.	5	8		5	8		mA
		$V_{IN}- = +1Vdc$, $V_O = 200mV$	12	50		12	50		μA
I_{SC}	Short circuit current[4]			40	60		40	60	mA
	Differential input voltage[6]				V+			V+	V

NOTES

1. $V_O \cong 1.4Vdc$, $R_S = 0\Omega$ with V+ from 5V to 30V and over full input common mode range (0Vdc+ to V+ -1.5V).
2. The direction of the input current is out of the IC due to the pnp input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ -1.5, but either or both inputs can go to +32V without damage.
4. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15Vdc continous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
5. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ -1.5V, but either or both inputs can go to +32Vdc without damage.

LM124/A/224/A/324/A/SA534-F,N-14,T
LM158/A/258/A/358A-F,N,T

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V+ = 5V$, $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	LM358A			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage[1]	$R_S \leq 10k\Omega$		2	3	mV
		$R_S \leq 10k\Omega$, over temp.			5	mV
V_{OS}	Drift	$R_S = 0\Omega$, over temp.		7	20	$\mu V/°C$
I_{BIAS}	Input current[2]	$I_{IN}(+) - I_{IN}(-)$		45	100	nA
		$I_{IN}(+) - I_{IN}(-)$, over temp.		40	200	nA
I_{OS}	Offset current	$I_{IN}(+) - I_{IN}(-)$		5	30	nA
		$I_{IN}(+) - I_{IN}(-)$, over temp.			75	nA
I_{OS}	Drift	over temp.		10	300	pA/°C
V_{CM}	Common mode voltage range[3]	V+ = 30V	0		V+-1.5	V
		V+ = 30V, over temp.	0		V+-2	V
C_{MRR}	Common mode rejection ratio		65	85		dB
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$, V+ = +30V, over temp.	26			V
V_{OH}		$R_L \leq 10k\Omega$, over temp	27	28		V
V_{OL}		$R_L \leq 10k\Omega$, V+ = 5V, over temp.		5	20	V
I_{CC}	Supply current	$R_L = \infty$, V_{CC} = 30V, over temp.		1.5	3	mA
		$R_L = \infty$, on all op amps, over temp.		0.7	1.2	mA
A_{VOL}	Large signal voltage gain	V+ = +15V (for large V_O swing), $R_L \geq 2k\Omega$	25	100		V/mV
		V+ = +15V (for large V_O swing), $R_L \geq 2k\Omega$, over temp.	15			V/mV
	Amplifier-to-amplifier coupling[4]	f = 1kHz to 20kHz, input referred		-120		dB
P_{SRR}		$R_S \leq 10k\Omega$	65	100		dB
	Output current					
	Source	$V_{IN}+ = +1Vdc$, $V_{IN}- = 0Vdc$, V+ = 15Vdc	20	40		mA
		$V_{IN}+ = +1Vdc$, $V_{IN}- = 0Vdc$, V+ = 15Vdc, over temp.	10	20		mA
	Sink	$V_{IN}- = +1Vdc$, $V_{IN}+ = 0Vdc$, V+ = 15Vdc	10	20		mA
		$V_{IN}- = +1Vdc$, $V_{IN}+ = 0Vdc$, V+ = 15Vdc, over temp.	5	8		mA
		$V_{IN}- = +1Vdc$, $V_O = 200mV$	12	50		μA
I_{SC}	Short circuit current[4]			40	60	mA
	Differential input voltage[6]				V+	V

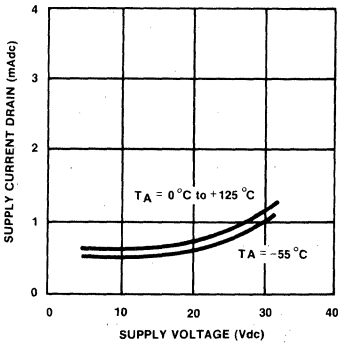
NOTES

1. $V_O \cong 1.4Vdc$, $R_S = 0\Omega$ with V+ from 5V to 30V and over full input common mode range (OVdc+ to V+ -1.5V).
2. The direction of the input current is out of the IC due to the pnp input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ -1.5, but either or both inputs can go to +32V without damage.
4. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15Vdc continous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
5. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ -1.5V, but either or both inputs can go to +32Vdc without damage.

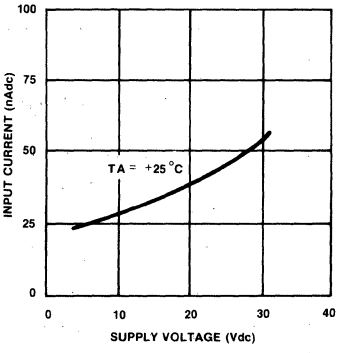
LM124/A/224/A/324/A/SA534-F,N-14,T
LM158/A/258/A/358A-F,N,T

TYPICAL PERFORMANCE CHARACTERISTICS

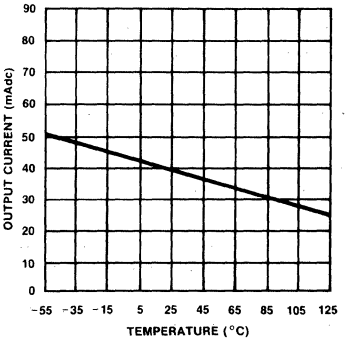
SUPPLY CURRENT



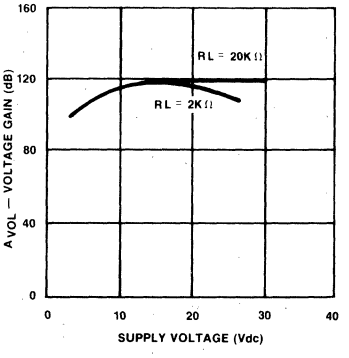
INPUT CURRENT



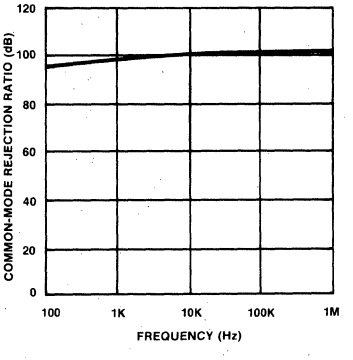
CURRENT LIMITING



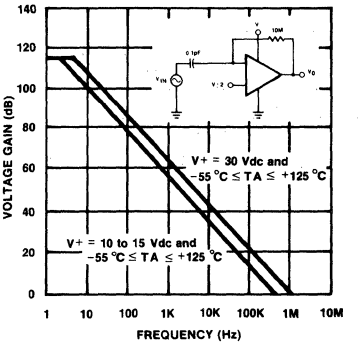
VOLTAGE GAIN



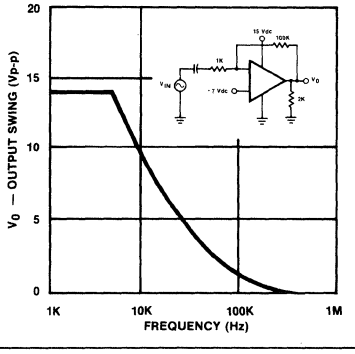
COMMON-MODE REJECTION RATIO



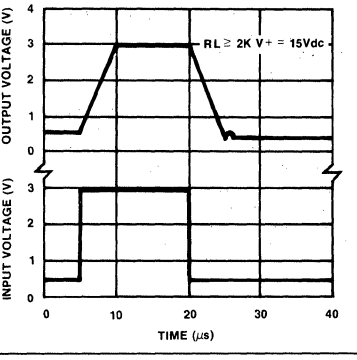
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE



VOLTAGE FOLLOWER PULSE RESPONSE



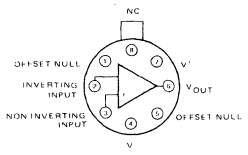
MC1456/1556-F,N,T

DESCRIPTION

The MC1456/1556 is an internally compensated precision monolithic operational amplifier featuring extremely low offset and bias currents and offset null capability. The MC1456/1556 is short circuit protected and its high common mode and differential input voltage range provides exceptional performance when used as an integrator, summing amplifier, and voltage follower.

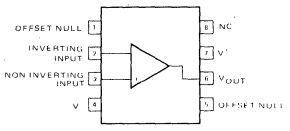
PIN CONFIGURATIONS

T PACKAGE



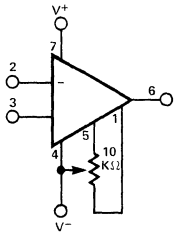
ORDER PART NO.
MC1456T
MC1556T

N PACKAGE



ORDER PART NO.
MC1456N
MC1556N

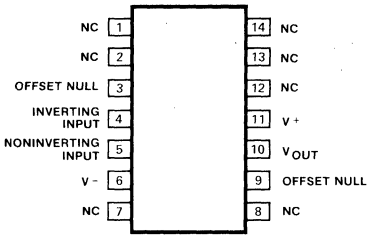
OFFSET ADJUST CIRCUIT



FEATURES

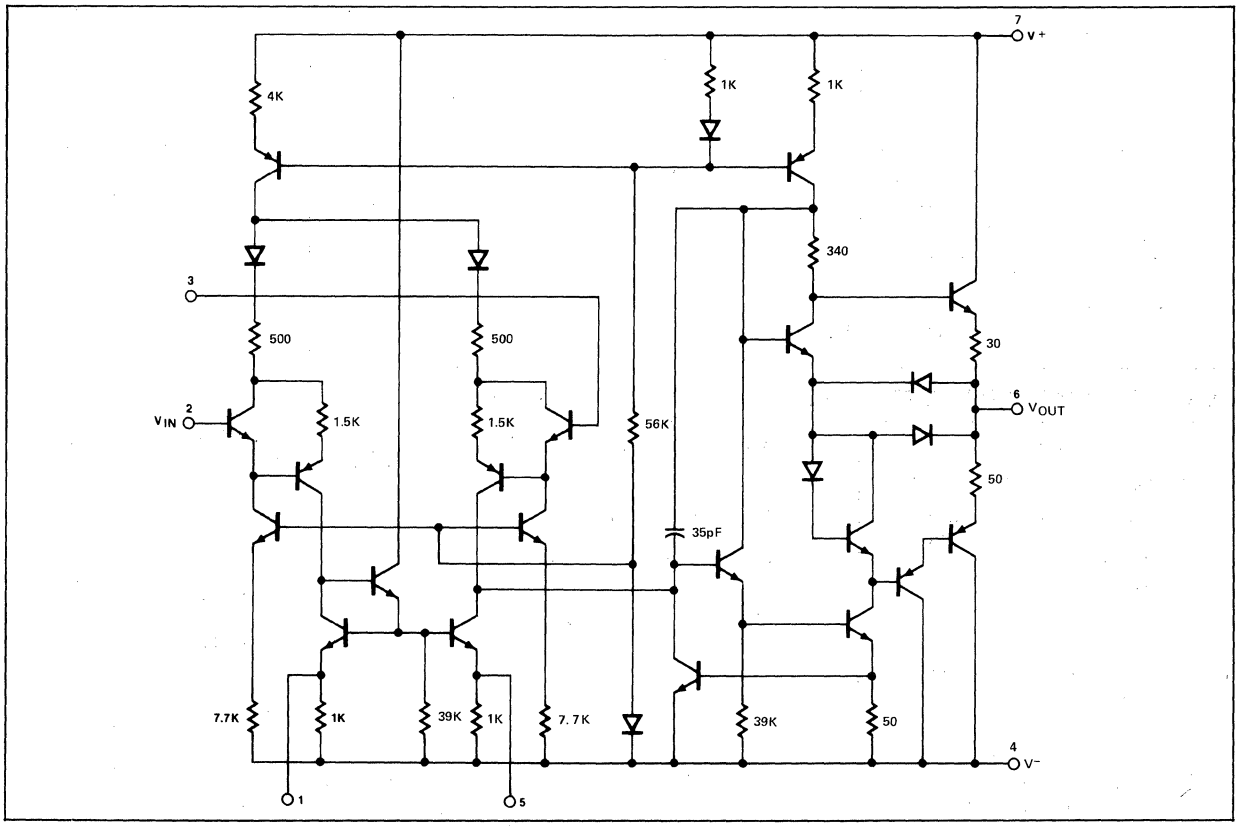
- **Low input bias current—15nA maximum**
- **Low input offset current—2.0nA maximum**
- **Low input offset voltage—4.0mV maximum**
- **High slew rate—2.5V/μs typical**
- **Large power bandwidth—40kHz typical**
- **Low power consumption—45mW maximum**
- **Offset voltage null capability**
- **Output short circuit protection**
- **Input over-voltage protection**
- **Mil std 883A,B,C, available**

F PACKAGE



ORDER PART NO.
MC1456F
MC1556F

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Power supply voltage MC1556	±22	V
MC1456	±18	V
Differential input voltage	± V_{CC}	V
Common mode input voltage	± V_{CC}	V
Load current	20	mA
Output short circuit duration	Continuous	
Power dissipation	680	mW
Derate above T_A = 25°C	4.6	mW/°C
Operating temperature range		
MC1556	-55 to +125	°C
MC1456	0 to +70	°C
Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_S = ± 15V unless otherwise specified

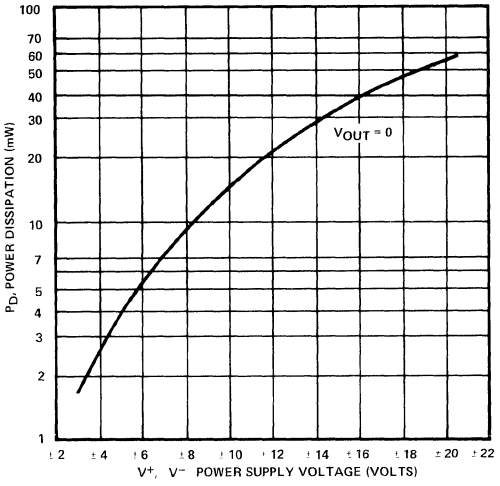
PARAMETER		TEST CONDITIONS	MC1556			MC1456			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage			2.0	4.0		5.0	10.0	mVdc
		Over temperature			6.0			14.0	mVdc
I_{OS}	Offset current			1.0	2.0		5.0	10.0	nA
		0°C ≤ T_A ≤ 70°C						14	nA
		25°C ≤ T_A ≤ 125°C			3.0				nA
		-55°C ≤ T_A ≤ 25°C			5.0				nA
I_{BIAS}	Input current			8.0	15		15.0	30.0	nA
		Over temperature			30			40	nA
V_{CM}	Common mode voltage range		±12	±13		±11	±12		V
CMRR	Common mode rejection ratio	R_S ≤ 10kΩ, T_A = 25°C, f = 100Hz	80	110		70	110		dB
Z_{IN}	Common mode input impedance	f = 20Hz		250			250		MΩ
V_{OUT}	Output voltage swing	R_L = 2kΩ	±12	±13		±11	±12		V
I_{CC}	Supply current			1.0	1.5		1.3	3.0	mA
P_D	DC quiescent power dissipation (V_O = 0)			30	45		40	90	mW
P_{SRR}	Supply voltage rejection ratio	R_S ≤ 10kΩ		50	100		75	200	μV/V
	Large signal voltage gain	R_L ≤ 2kΩ, V_{OUT} = ±10V, T_A = 25°C	100	200		70	100		V/mV
		Over temperature	40			40			V/mV

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_S = ± 15V unless otherwise specified.

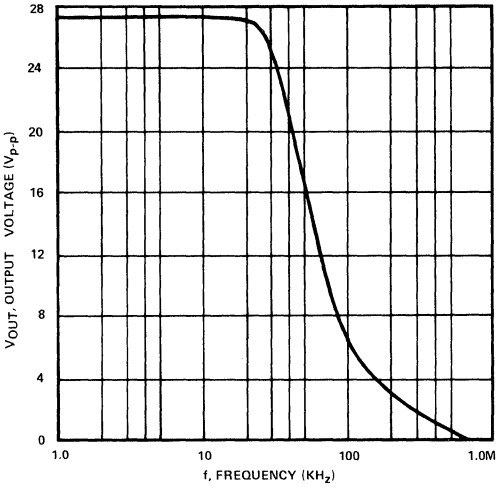
PARAMETER		TEST CONDITIONS	MC1556			MC1456			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Differential input impedance								
c_p	Parallel input capacitance	Open loop f = 20Hz		6.0			6.0		pF
r_p	Parallel input resistance			5			3		MΩ
e_n	Equivalent input noise voltage	A_V = 100, R_S = 10kΩ, f = 1.0kHz, BW = 1.0Hz		45			45		$nV/\sqrt{Hz}$
BW_p	Power bandwidth	A_V = 1, R_L = 2kΩ, THD ≤ 5% V_{OUT} = ±10V		40			40		kHz
	Phase margin (open loop, unity gain)			70			70		degrees
	Gain margin			18			18		dB
S_R	Slew rate (unity gain)			2.5			2.5		V/μsec
Z_{OUT}	Output impedance	f = 20Hz		1.0	2.0		1.0	2.5	kΩ
BW	Unity gain crossover frequency (open loop)			1.0			1.0		MHz

TYPICAL PERFORMANCE CHARACTERISTICS

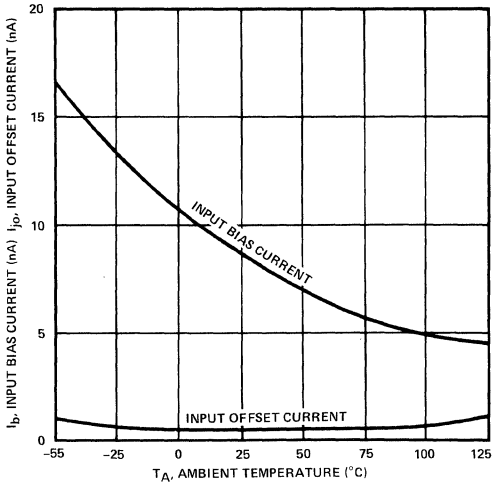
POWER DISSIPATION vs POWER SUPPLY VOLTAGE



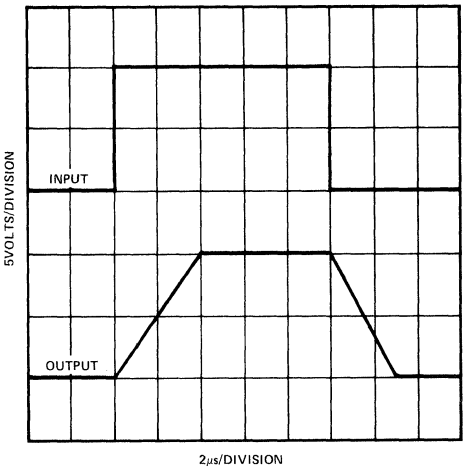
POWER BANDWIDTH



TYPICAL INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs TEMPERATURE FOR MC1556



VOLTAGE FOLLOWER PULSE RESPONSE



μA741/741C/SA741C,
MC1458/1558/SA1458-F,N,T

DESCRIPTION

The μA741 is a high performance operational amplifier with high open loop gain, internal compensation, high common mode range and exceptional temperature stability. The μA741 is short-circuit protected and allows for nulling of offset voltage.

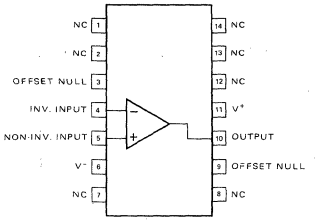
The MC1558/MC1458/SA1458 consist of a pair of 741 operational amplifiers on a single chip.

FEATURES

- **Internal frequency compensation**
- **Short circuit protection**
- **Excellent temperature stability**
- **High input voltage range**
- **No latch-up**
- **1558/1458 are 2 "op amps" in space of one 741 package**
- **MC1558 Mil std 883A,B,C available**
- **μA741 Mil std 883A,B,C available**

PIN CONFIGURATIONS

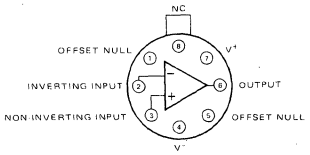
F,N-14 PACKAGE



ORDER PART NO.

μA741F
μA741N-14
μA741CF
μA741CN-14
SA741CF
SA741CN-14

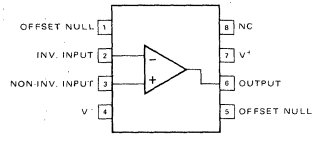
T PACKAGE



ORDER PART NO.

μA741T
μA741CT
SA741CT

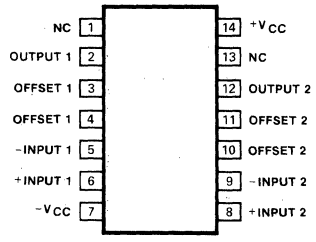
N PACKAGE



ORDER PART NO.

μA741N
μA741CN
SA741CN

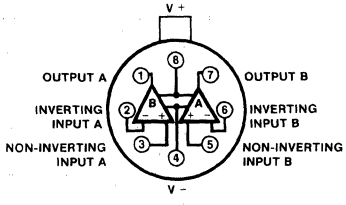
F,N-14 PACKAGE



ORDER PART NO.

MC1458F
MC1558F
SA1458F
MC1458N-14
MC1558N-14
SA1458N-14

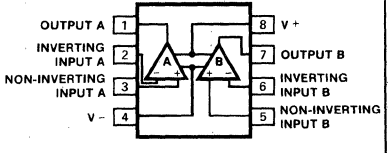
T PACKAGE



ORDER PART NO.

MC1458T
MC1558T
SA1458T

N PACKAGE

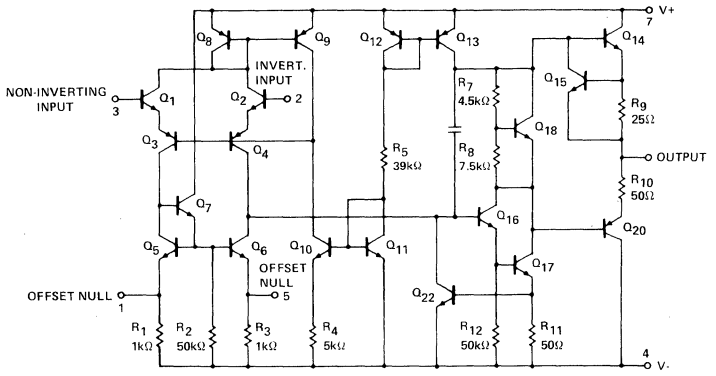


ORDER PART NO.

MC1458N
MC1558N
SA1458N

EQUIVALENT SCHEMATIC

μA741, A741C, SA741C
ONE AMPLIFIER OF MC1558, MC1458, SA1458



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SA741C, μA741C, MC1458, SA1458	±18	V
μA741, MC1558	±22	V
Internal power dissipation, N-14[4]	600	mW
N package	500	mW
T package[1]	800	mW
F package	1000	mW
Differential input voltage	±30	V
Input voltage[2]	±15	V
Output short-circuit duration	Continuous	
Operating temperature range		
μA741C, MC1458	0 to +70	°C
SA741C, SA1458	-40 to +85	°C
μA741, MC1558	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 60sec)	300	°C

NOTES

1. Ratings based on thermal resistances, junction to ambient, of 208°C/W, 240°C/W, 150°C/W, 110°C/W for N-14, N, T and F packages respectively, and a maximum junction temperature of 150°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

μA741/741C/SA741C,
MC1458/1558/SA1458-F,N,T

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

PARAMETER		TEST CONDITIONS	μA741			μA741C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10k\Omega$ $R_S = 10k\Omega$, over temp.		1.0 1.0	5.0 6.0		2.0	6.0 7.5	mV mV
I_{OS}	Offset current	 Over temp. $T_A = +125°C$ $T_A = -55°C$		20 7.0 20	200 200 500		20	200 300	nA nA nA nA
I_{BIAS}	Input bias current	 Over temp. $T_A = +125°C$ $T_A = -55°C$		80 30 300	500 500 1500		80	500 800	nA nA nA nA
V_{OUT}	Output voltage swing	$R_L = 10k\Omega$ $R_L = 2k\Omega$, over temp.	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
A_{VOL}	Large signal voltage gain	$R_L = 2k\Omega$, $V_O = \pm 10V$ $R_L = 2k\Omega$, $V_O = \pm 10V$, over temp.	50 25	200		20 15	200		V/mV V/mV
	Offset voltage adjustment range			±30			±30		mV
P_{SRR}	Supply voltage rejection ratio	$R_S \leq 10k\Omega$ $R_S \leq 10k\Omega$, over temp.		 10	 150		10	150	μV/V μV/V
CMRR	Common mode rejection ratio	 Over temp.	 70	 90					dB dB
I_{CC}	Supply current	 $T_A = +125°C$ $T_A = -55°C$		1.4 1.5 2.0	2.8 2.5 3.3		1.4	2.8	mA mA mA
V_{IN} R_{IN}	Input voltage range Input resistance	(μA741, over temp.)	±12 0.3	±13 2.0		±12 0.3	±13 2.0		V MΩ
P_d	Power consumption	 $T_A = +125°C$ $T_A = -55°C$		50 45 45	85 75 100		50	85	mW mW mW
R_{OUT} I_{SC}	Output resistance Output short-circuit current			75 25			75 25		Ω mA

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

PARAMETER		TEST CONDITIONS	SA741C			MC1558			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10k\Omega$ $R_S = 10k\Omega$, over temp.		2.0	6.0 7.5		1.0	5.0 6.0	mV mV
I_{OS}	Offset current	 Over temp.		20	200 500		20	200 500	nA nA
I_{BIAS}	Input bias current	 Over temp.		80	500 1500		80	500 1500	nA nA
V_{OUT}	Output voltage swing	$R_L = 10k\Omega$ $R_L = 2k\Omega$, over temp.	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
A_{VOL}	Large signal voltage gain	$R_L = 2k\Omega$, $V_O = \pm 10V$ $R_L = 2k\Omega$, $V_O = \pm 10V$, over temp.	20 15	200		50 25	100		V/mV V/mV
	Offset voltage adjustment range			±30			±30		mV
P_{SRR}	Supply voltage rejection ratio	$R_S \leq 10k\Omega$		10	150		30	150	μV/V
CMRR	Common mode rejection ratio						70	90	dB
I_{CC}	Supply current			1.4	2.8		2.3	5.6	mA
V_{IN} R_{IN}	Input voltage range Input resistance	(μA741, over temp.)	±12 0.3	±13 2.0		±12	±13		V MΩ
P_d	Power consumption			50	85		70	150	mW
 R_{OUT} I_{SC}	Channel separation Output resistance Output short-circuit current			 75 25			120 25		dB Ω mA

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MC1458			SA1458			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10k\Omega$ $R_S = 10k\Omega$, over temp.		2.0	6.0 7.5		2.0	6.0 7.5	mV mV
I_{OS}	Offset current	 Over temp.		20	200 300		20	200 500	nA nA
I_{BIAS}	Input bias current	 Over temp.		80	500 800		80	500 1500	nA nA
V_{OUT}	Output voltage swing	$R_L = 10k\Omega$ $R_L = 2k\Omega$, over temp.	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
A_{VOL}	Large signal voltage gain	$R_L = 2k\Omega$, $V_O = \pm 10V$ $R_L = 2k\Omega$, $V_O = \pm 10V$, over temp.	25 15	200		25 15	200		V/mV V/mV
	Offset voltage adjustment range			±30			±30		mV
P_{SRR}	Supply voltage rejection ratio	$R_S \leq 10k\Omega$		30	170		30	150	μV/V
CMRR	Common mode rejection ratio			70	90		70	90	dB
I_{CC}	Supply current			2.3	5.0		2.3	5.6	mA
V_{IN} R_{IN}	Input voltage range Input resistance	(μA741, over temp.)	±12	±13		±12	±13		V MΩ
P_d	Power consumption			70	170		70	170	mW
 I_{SC}	Channel separation Output short-circuit current			120 25			120 25		dB mA

μA741/741C/SA741C,
MC1458/1558/SA1458-F,N,T

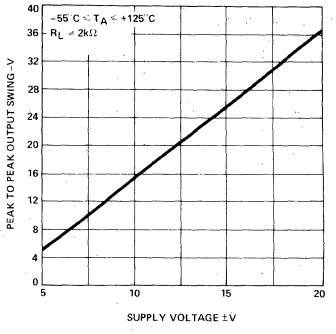
AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

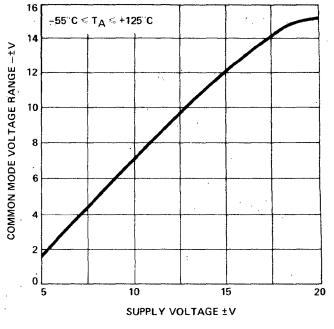
PARAMETER	TEST CONDITIONS	μA741, μA741C, SA741C			MC1558, MC1458, SA1458			UNIT
		Min	Typ	Max	Min	Typ	Max	
Parallel input resistance	Open loop, f = 20Hz				0.3			MΩ
Parallel input capacitance	Open loop, f = 20Hz		1.4					pF
Common mode input impedance	f = 20Hz					200		MΩ
Equivalent input noise voltage	$A_V = 100$, $R_S = 10k\Omega$, $B_W = 1.0kHz$ f = 1.0kHz					45		$nV\sqrt{Hz}$
Power bandwidth	$A_V = 1$, $R_L = 2.0k\Omega$, THD ≤ 5% $V_{OUT} = 20Vp\text{-}p$					14		kHz
Phase margin						65		degrees
Gain margin						11		dB
Unity gain crossover frequency	Open loop		1.0			1.0		MHz
Transient response unity gain	$V_{IN} = 20mV$, $R_L = 2k\Omega$, $C_L \leq 100pf$							
Rise time			0.3			0.3		μs
Overshoot			5.0			5.0		%
Slew rate	$C \leq 100pf$, $R_L \geq 2k$, $V_{IN} = \pm 10V$		0.5			0.8		V/μs

TYPICAL PERFORMANCE CHARACTERISTICS

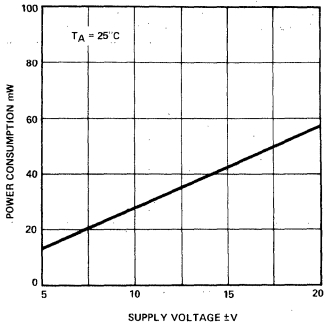
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



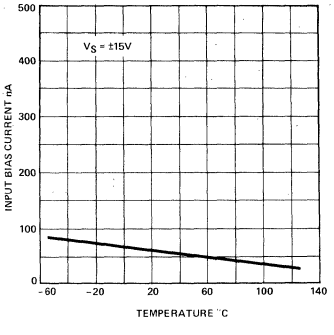
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



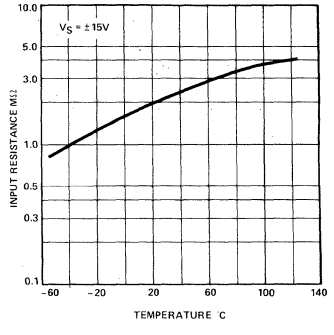
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



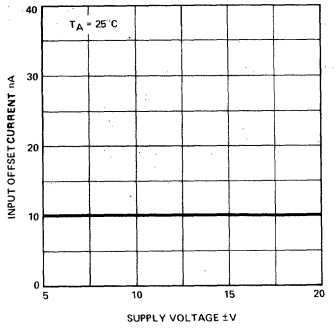
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

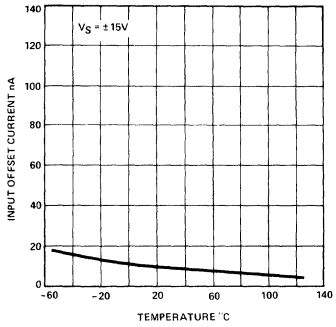


INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

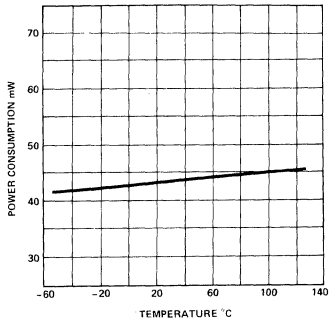


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

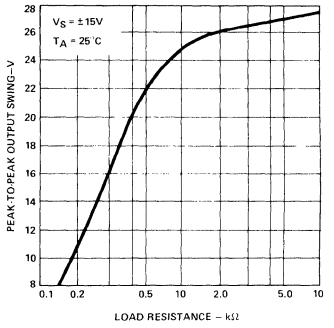
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



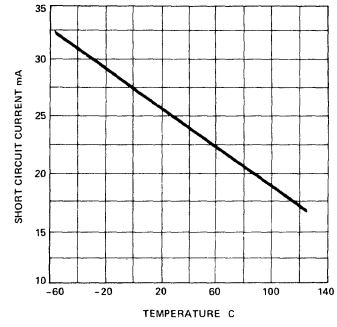
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



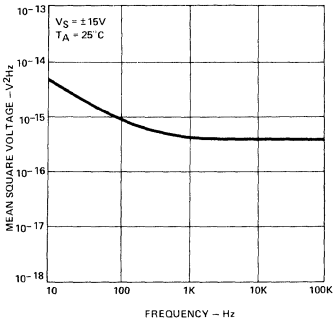
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



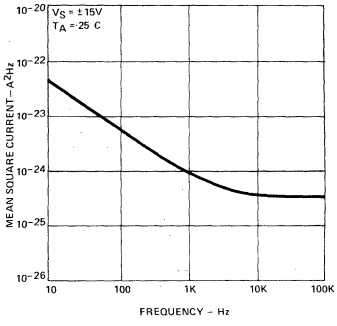
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



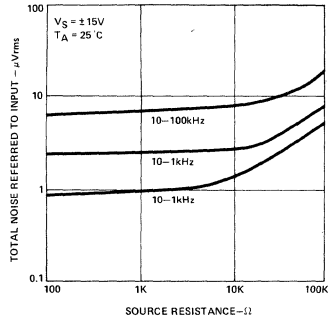
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



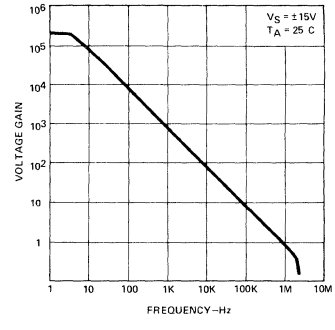
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



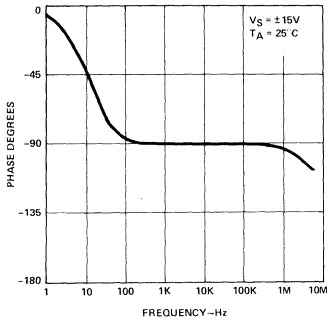
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

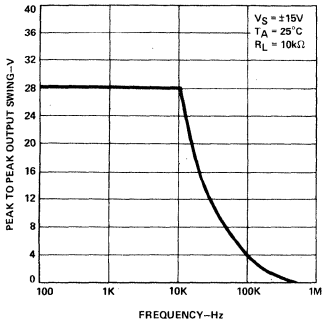


OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY

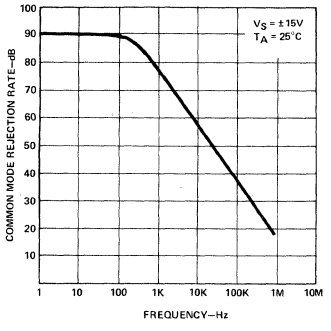


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

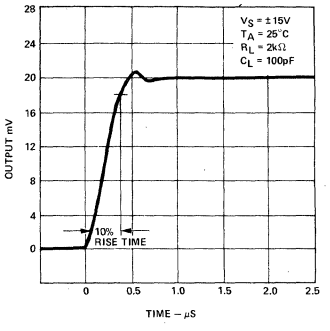
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



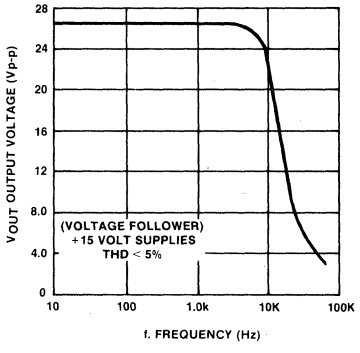
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



TRANSIENT RESPONSE



POWER BANDWIDTH (Large Signal Swing vs Frequency)



NE/SE515-F,K,N

DESCRIPTION

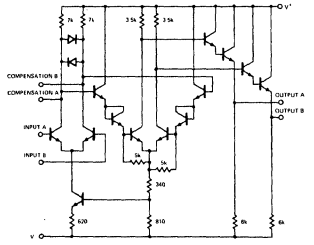
The 515 is a general purpose high-gain amplifier with differential input and output. It is fabricated within a monolithic silicon substrate by planar and epitaxial techniques. A pair of compensation points is provided to allow frequency compensation for stable closed loop operation.

This device is not internally referenced to ground and with proper input bias may be operated from a single power supply.

FEATURES

- **Differential voltage gain (open loop) = 4,500**
- **Input offset voltage = 0.5mV**
- **Input offset voltage stability = 5.0μV/°C**
- **Input common mode range = 1.5V, -1.0V**
- **Common mode rejection ratio = 100dB**
- **Bandwidth (open loop) = 1.0MHz**
- **Mil std 883A,B,C available**

EQUIVALENT SCHEMATIC

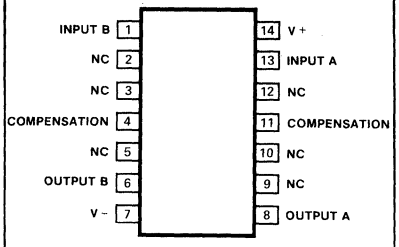


NOTE

All resistors values are typical and in ohms.
Component values are typical.

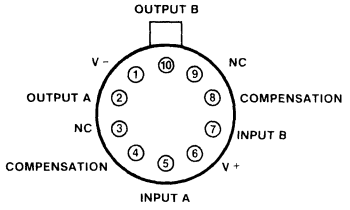
PIN CONFIGURATION

F,N PACKAGE



ORDER PART NO.
NE515N/NE515F/SE515F

K PACKAGE



ORDER PART NO.
SE515K/NE515K

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Voltage		
Applied (V+ to V-)	12	V
Differential input (V_5 to V_7)	±5.0	V
Current		
Input (I_5, I_7)	±2.0	mA
Output (I_2, I_{10})	±30	mA
Temperature range		°C
Operating	0 to +75	
Storage	-65 to +150	
Junction	150	

Maximum ratings are limiting values above which serviceability may be impaired.
Pin numbers refer to K package.

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_7 = 0V, V_1 = 3.0V unless otherwise specified. 1,2,3,4,5,6,7,8,9,10,11

PARAMETER	TEST CONDITIONS	SE515 (V_6 = +4V)			SE515 (V_6 = +6V)			UNITS
		Min	Typ	Max	Min	Typ	Max	
Open loop voltage gain[2]			2500		3500	4500		V/V
	T_A = high temp.		1800			3000		V/V
Input offset voltage[1]	T_A = low temp.		.5			0.5	3.0	mV
			.5			0.5	2.0	mV
	T_A = high temp.		.5			0.5	3.0	mV
Input bias current[1]	T_A = low temp.		18			25	40	μA
	@ +25°C		12			16	24	μA
Differential input resistance[10]	T_A = low temp.		2		1.0	1.5		kΩ
			4		2.0	3.2		kΩ
Input common mode range			±1.0			+1.5 -1.0		V
Balanced output DC level	T_A = low temp.		-0.1			+1.2		V
	@ +25°C		+0.3			+1.6	1.8	V
	T_A = high temp.		+.6			+1.9		V
Output voltage swing[3]	Over temp.		4.7		5.7	6.3		V
High output level	V_5 = 10mV, T_A = low temp.		+2.3		+4.0	+4.3		V
	V_5 = 10mV		+2.6		+4.3	+4.6		V
	V_5 = 10mV, T_A = high temp.		+3.0		+4.7	+5.0		V
Low output level	V_5 = 10mV, T_A = low temp.		-2.4		-1.7	-2.0		V
	V_5 = 10mV		-2.1		-1.4	-1.7		V
	V_5 = 10mV, T_A = high temp.		-1.7		-1.0	-1.3		V
Output resistance[1]			100			100		Ω
Common mode rejection ratio			100			100		dB
Power supply current[1]	T_A = low temp.						7.0	mA
			3.5			5.5	7.0	mA
	T_A = high temp.						7.0	mA

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $V_7 = 0V$, $V_1 = 3.0V$ unless otherwise specified.[1,2,3,4,5,6,7,8,9,10,11]

PARAMETER	TEST CONDITIONS	NE515 (V_6 = +4V)			NE515 (V_6 = +6V)			UNIT
		Min	Typ	Max	Min	Typ	Max	
Open loop voltage gain[2]			1800		2500	3200		V/V
	T_A = high temp.		1350			2200		V/V
Input offset voltage[1]	T_A = low temp.		0.5			0.5	4.0	mV
			0.5			0.5	3.0	mV
	T_A = high temp.		0.5			0.5	4.0	mV
Input bias current[1]	T_A = low temp.		18			25	40	μA
	@ +25°C		15			20	31	μA
Differential input resistance[10]	T_A = low temp.		3.2		1.4	2.3		kΩ
			3.5		1.7	2.6		kΩ
Input common mode range			±1.0			+1.5 -1.0		V
Balanced output DC level	T_A = low temp.		-0.1			+1.2		V
	@ +25°C		+0.3			+1.6	+1.8	V
	T_A = high temp.		+0.6			+1.9		V
Output voltage swing[3]	Over temp.		4.5		5.3	6.1		V
High output level	V_5 = 10mV, T_A = low temp.		+2.3		+3.9	+4.3		V
	V_5 = 10mV		+2.5		+4.1	+4.5		V
	V_5 = 10mV, T_A = high temp.		+2.8		+4.3	+4.8		V
Low output level	V_5 = 10mV, T_A = low temp.		-2.2		-1.4	-1.8		V
	V_5 = 10mV		-2.0		-1.2	-1.6		V
	V_5 = 10mV, T_A = high temp.		-1.7		-1.0	-1.3		V
Output resistance[1]			100			100		Ω
Common mode rejection ratio			100			100		dB
Power supply current[1]	T_A = low temp.						7.0	mA
			3.5			5.5	7.0	mA
	T_A = high temp.						7.0	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_7 = 0V$, $V_1 = 3.0V$ unless otherwise specified.[1,2,3,4,5,6,7,8,9,10,11]

PARAMETER	TEST CONDITIONS	SE515 (V_6 = +4V)			SE515 (V_6 = +6V)			UNIT
		Min	Typ	Max	Min	Typ	Max	
Open loop voltage gain	f = 800kHz		2000		2500	3500		μV/V

AC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $V_7 = 0V$, $V_1 = 3.0V$ unless otherwise specified.[1,2,3,4,5,6,7,8,9,10,11]

PARAMETER	TEST CONDITIONS	NE515 (V_6 = +4V)			NE515 (V_6 = +6V)			UNIT
		Min	Typ	Max	Min	Typ	Max	
Open loop voltage gain	f = 800kHz		1500		1700	2500		μV/V

NOTES

1. Adjust V5 to obtain $V_2 = V_{10}$.
2. Output voltage swing = 1.3V peak to peak.
3. Output voltage swing is guaranteed by output voltage limit tests.
4. Voltage and current subscripts refer to pin numbers for K Package.
5. All measurements are referenced to power supply common. Positive current flow is defined as into the terminal indicated.
6. All specifications herein apply for interchange of voltages and currents at Pins 5 and 7.
7. Acceptance Test Sub-Group references apply to minimum and maximum limits only.
8. The SE515k has Pins 1, 3 and 9 connected to the case.
9. See Signetics SURE Program Bulletin No. 5001 for definition of Acceptance Test Sub-Group. Sub-Group A-7 is used for electrical end points for Linear Products.
10. Differential Input Resistance is computed from input bias current.
11. Operating temperature range:
    SE515 -55°C T_A 125°C
    NE515 0°C T_A 75°C

NE/SE531-N,T

DESCRIPTION

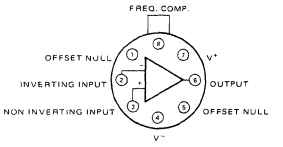
The 531 is a fast slewing high performance operational amplifier which retains dc performance equal to the best general purpose types while providing far superior large signal ac performance. A unique input stage design allows the amplifier to have a large signal response nearly identical to its small signal response. The amplifier is compensated for truly negligible overshoot with a single capacitor. In applications where fast settling and superior large signal bandwidths are required, the amplifier out performs conventional designs which have much better small signal response. Also, because the small signal response is not extended, no special precautions need be taken with circuit board layout to achieve stability. The high gain, simple compensation and excellent stability of this amplifier allow its use in a wide variety of instrumentation applications.

FEATURES

- **35V/μsec slew rate at unity gain**
- **Pin for pin replacement for μA709, μA748 or LM101**
- **Compensated with a single capacitor**
- **Same low drift offset null circuitry as μA741**
- **Small signal bandwidth 1MHz**
- **Large signal bandwidth 500KHz**
- **True op amp dc characteristics make the 531 the ideal answer to all slew rate limited operational amplifier applications.**

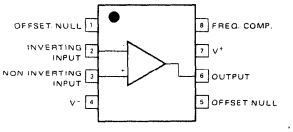
PIN CONFIGURATIONS

T PACKAGE
(Top View)



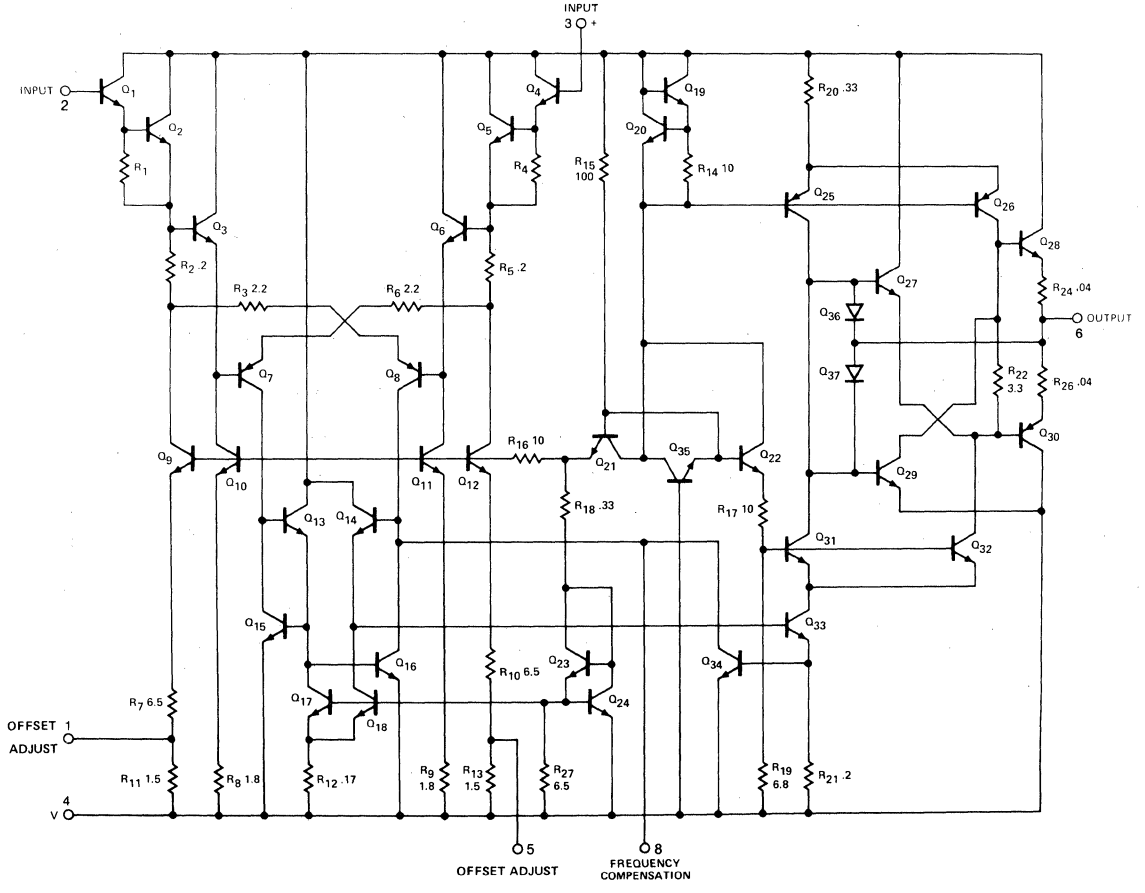
ORDER PART NO.
SE531T/NE531T

N PACKAGE



ORDER PART NO.
NE531N

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	±22	V
Internal power dissipation[1]	300	mW
Differential input voltage	±15	V
Common mode input voltage[2]	±15	V
Voltage between offset null and V-	±0.5	V
Operating temperature range		
NE531	0 to +70	°C
SE531	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60 sec)	300	°C
Output short circuit duration[3]	indefinite	

NOTES

1. Rating applies for case temperature to 125°C, derate linearly at 6.5mW/°C for ambient temperatures above +75°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or to +75°C ambient temperature.

DC ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SE531			NE531			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \leq 10k\Omega$, $T_A = 25°C$		2.0	5.0		2.0	6.0	mV
		$R_S \leq 10k\Omega$, over temp			6.0			7.5	mV
I_{OS}	Offset current	$T_A = 25°C$		30	200		50	200	nA
		T_A = HIGH			200			200	nA
		T_A = LOW			500			300	nA
I_{BIAS}	Input current	$T_A = 25°C$		300	500		400	1500	nA
		T_A = HIGH			500			1500	nA
		T_A = LOW			1500			2000	nA
V_{CM}	Common mode voltage range	$T_A = 25°C$	±10			±10			V
CMRR	Common mode rejection ratio	$T_A = 25°C$, $R_S \leq 10k\Omega$				70	100		dB
		Over temp $R_S \leq 10k\Omega$	70	90					dB
R_{IN}	Input resistance	$T_A = 25°C$		20			20		MΩ
V_{OUT}	Output voltage swing	$R_L \geq 2k\Omega$, over temp	±10	±13		±10	±13		V
I_{CC}	Supply current	$T_A = 25°C$			7.0			10	mA
		T_{MAX}			5.5			10	mA
P_D	Power consumption	$T_A = 25°C$			210			300	mW
P_{SRR}	Power supply rejection ratio	$R_S \leq 10k\Omega$, $T_A = 25°C$					10	150	μV/V
		$R_S \leq 10k\Omega$, over temp		10	150				μV/V
R_{OUT}	Output resistance	$T_A = 25°C$		75			75		Ω
A_{VOL}	Large signal voltage gain	$T_A = 25°C$, $R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	50	100		20	60		V/mV
		$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$, over temp.	25			15			V/mV

NOTE

1. Temperature range:
   SE531 $-55°C \leq T_A \leq 125°C$
   NE531 $0°C \leq T_A \leq 70°C$

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

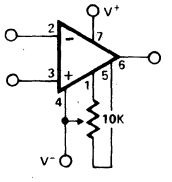
PARAMETER	TEST CONDITIONS	NE531			SE531			UNIT
		Min	Typ	Max	Min	Typ	Max	
Full power bandwidth			500			500		kHz
Settling time (1%) (.01%)	Av = +1, $V_{IN} = \pm 10V$		1.5 2.5			1.5 2.5		μs μs
Large signal overshoot Small signal overshoot	Av = +1, $V_{IN} = \pm 10V$ Av = +1, V_{IN} = 400mV		2 5			2 5		% %
Small signal risetime	Av = +1, V_{IN} = 400mV		300			300		ns
Slew rate	A_V = 100 A_V = 10 Av = 1 (noninverting) Av = 1 (inverting)		35 35 30 35		 20 25	35 35 30 35		V/μs V/μs V/μs V/μs

NOTE

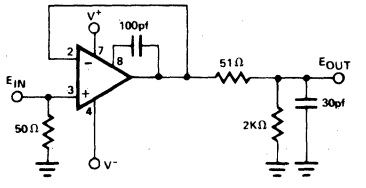
1. All AC testing is performed in the transient response test circuit.

TEST LOAD CIRCUITS

OFFSET NULL CIRCUIT

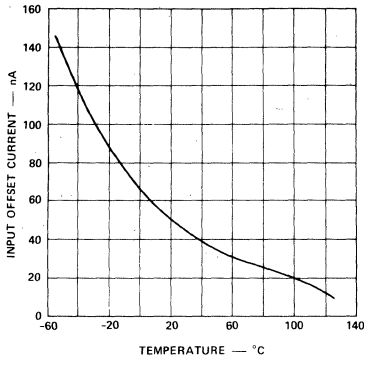


TRANSIENT RESPONSE CIRCUIT

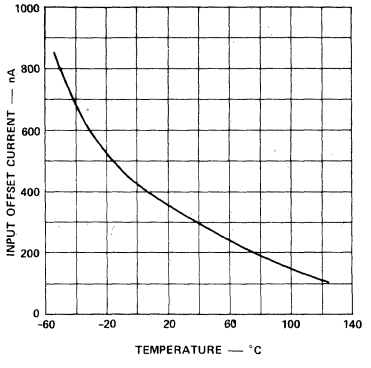


TYPICAL PERFORMANCE CHARACTERISTICS ($V_S = \pm 15V$, $T_A = +25°C$, unless otherwise specified.)

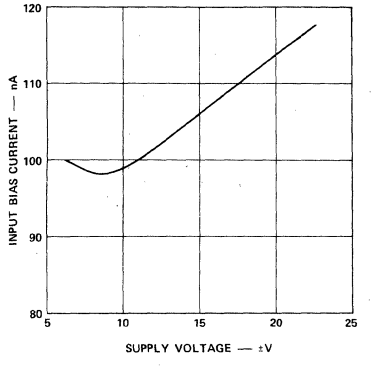
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

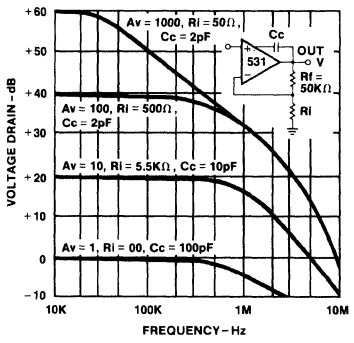


INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

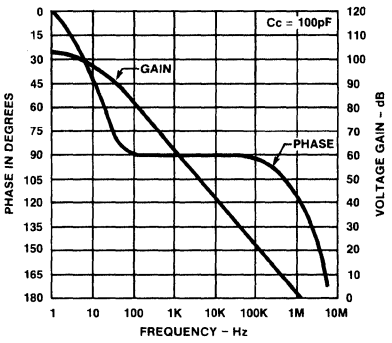


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

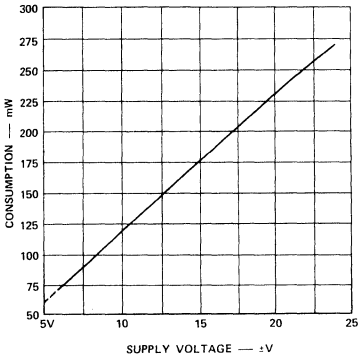
CLOSED LOOP NON-INVERTING VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



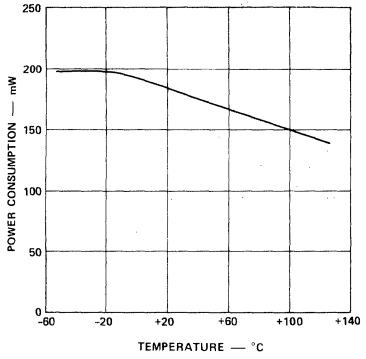
OPEN LOOP PHASE RESPONSE AND VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



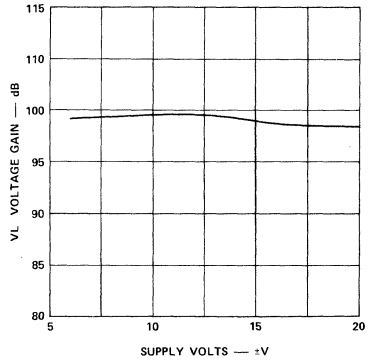
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



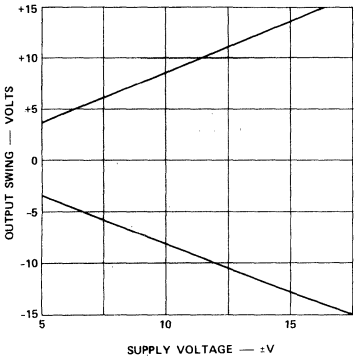
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



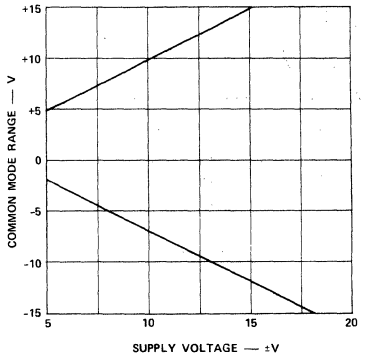
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



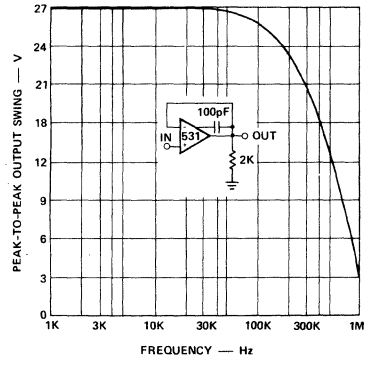
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



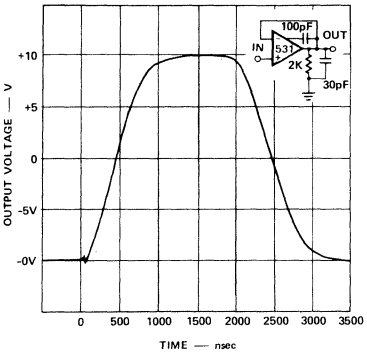
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

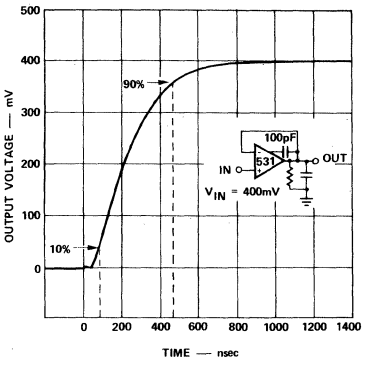


VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE

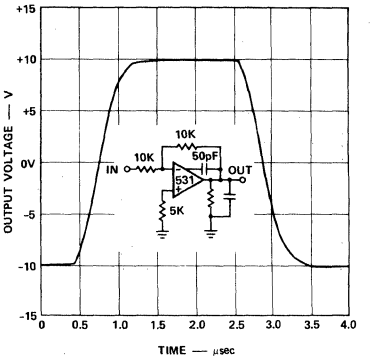


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

VOLTAGE FOLLOWER TRANSIENT RESPONSE

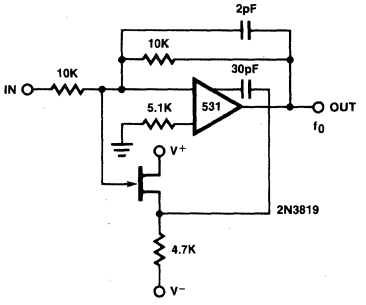


UNITY GAIN INVERTING AMPLIFIER LARGE SIGNAL RESPONSE

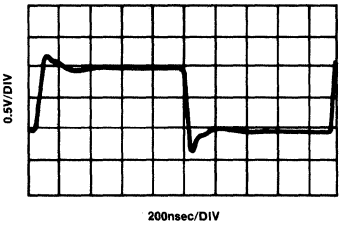


TYPICAL APPLICATIONS

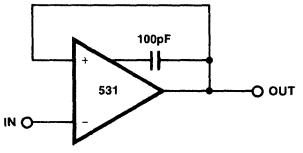
HIGH SPEED INVERTER (10MHz BANDWIDTH)



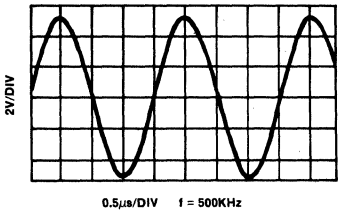
PULSE RESPONSE HIGH SPEED INVERTER



FAST SETTLING VOLTAGE FOLLOWER

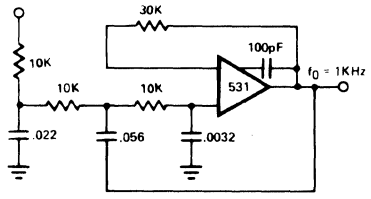


LARGE SIGNAL RESPONSE VOLTAGE FOLLOWER

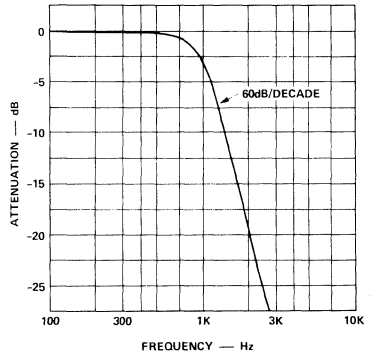


TYPICAL APPLICATIONS (Cont'd)

POLE ACTIVE LOW PASS FILTER BUTTERWORTH MAXIMALLY FLAT RESPONSE*



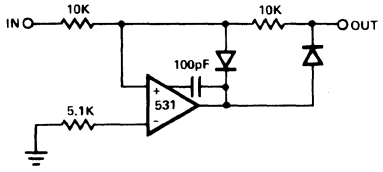
RESPONSE OF 3-POLE ACTIVE BUTTERWORTH MAXIMALLY FLAT FILTER



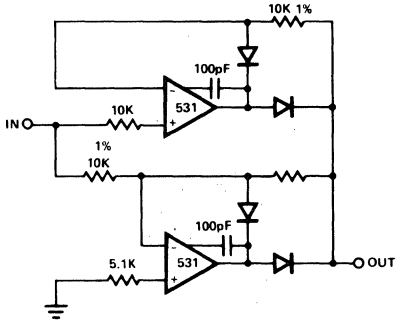
*Reference—EDN Dec. 15, 1970
Simplify 3-Pole Active Filter Design
A. Paul Brokow

PRECISION RECTIFIERS

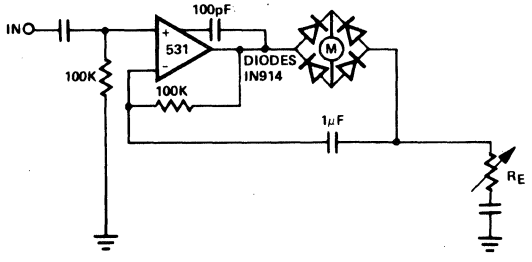
(a) HALF WAVE



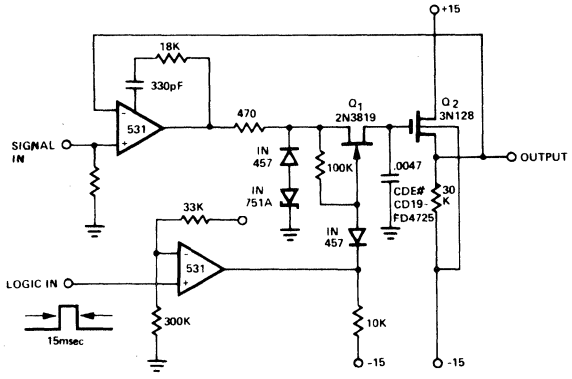
(b) FULL WAVE



AC MILLIVOLTMETER



SAMPLE AND HOLD



DESCRIPTION

The 532 consists of two independent, high gain, internally frequency compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages. Operation from dual power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

FEATURES

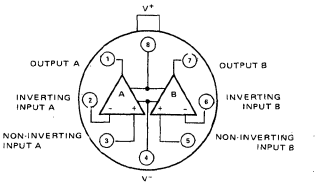
- **Internally frequency compensated for unity gain**
- **Large dc voltage gain—(100dB)**
- **Wide bandwidth (unity gain)—1MHz (temperature compensated)**
- **Wide power supply range**
  single supply—(3Vdc to 30Vdc)
  or dual supplies—(±1.5Vdc to ±15Vdc)
- **Very low supply current drain (400μA)—essentially independent of supply voltage (1mW/op amp at +5Vdc)**
- **Low input biasing current—(45nA dc temperature compensated)**
- **Low input offset voltage—(2mVdc) and offset current—(5nA dc)**
- **Differential input voltage range equal to the power supply voltage**
- **Large output voltage—(0Vdc to V+— - 1.5Vdc swing)**
- **SE532 Mil std 883A,B,C available**

UNIQUE FEATURES

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage. The unity gain cross frequency is temperature compensated. The input bias current is also temperature compensated.

PIN CONFIGURATIONS

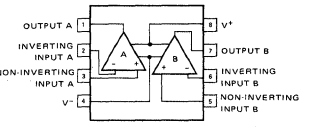
T PACKAGE
(Top View)



ORDER PART NO.

SE532T	NE532T
SE532AT	NE532AT
SA532T	

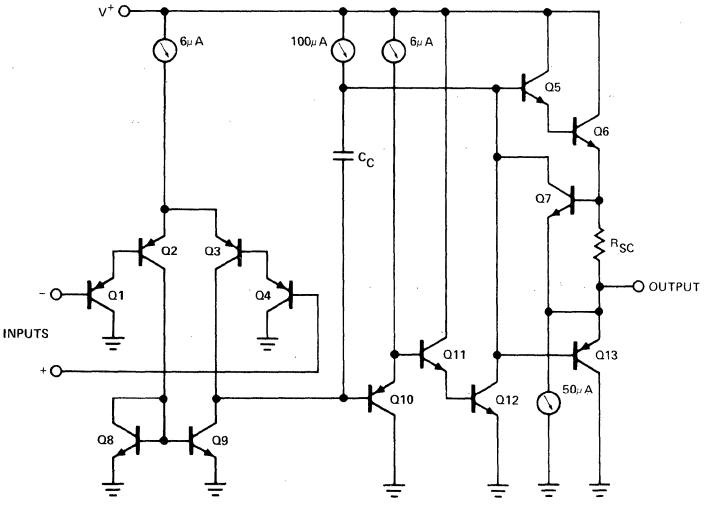
N PACKAGE
(Top View)



ORDER PART NO.

SE532N	NE532N
SA532N	
SE532AN	NE532AN

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage, V+	32 or ±16	Vdc
Differential input voltage	32	Vdc
Input voltage	-0.3 to +32	Vdc
Power dissipation		
T package	680	mW
N package	625	mW
Output short-circuit to GND		
V+ < 15 Vdc and T_A = 25°C	Continuous	
Operating temperature range		
NE532	0 to +70	°C
SA532	-40 to +85	°C
SE532	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

NE/SE532/532A/SA532-N,T

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V+ = +5V$ unless otherwise specified (see Notes on following page).

PARAMETER	TEST CONDITIONS	SE532			NE532			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Offset voltage[1]	$R_S \leq 10k$		±2	±5		±2	±6	mV
	$R_S \leq 10k\Omega$, over temp.			±7			±7.5	mV
V_{OS} Drift	$R_S = 0\Omega$, over temp.		7			7		μV/°C
I_{OS} Offset current	$I_{IN}(+)$ or $I_{IN}(-)$		±3	±30		+5	±50	nA
I_{OS} Offset current	Over temp.			±100			±150	nA
I_{OS} Drift	Over temp.		10			10		pA/°C
I_{BIAS} Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$		45	150		45	250	nA
	Over temp., $I_{IN}(+)$ or $I_{IN}(-)$		40	300		40	500	nA
V_{CM} Common mode voltage range[3]	$V+ = 30V$	0		V+–1.5	0		V+–1.5	V
	Over temp., $V+ = 30V$			V+–2.0			V+–2.0	V
C_{MRR} Common mode rejection ratio	$R_S \leq 10k\Omega$	70	85		65	70		dB
V_{OUT} Output voltage swing (V_{OH})	$R_L \geq 2k\Omega$, $V+ = 30V$	26			26			V
	$R_L \geq 10k\Omega$, $V+ = 30V$	27	28		27	28		V
V_{OUT} Output voltage swing (V_{OL})	$R_L \leq 10k\Omega$, over temp.		5	20		5	20	mV
I_{CC} Supply current	$R_L = \infty$ on all amplifiers, over temp		0.5	1.2		0.5	1.2	mA
A_{VOL} Large signal voltage Gain	$R_L \geq 2k\Omega$, $V_{OUT} \pm 10V$, $V_S = \pm 15V$	50	100		25	100		V/mV
	Over temp.	25			15			V/mV
P_{SRR} Supply voltage rejection ratio	$R_S \leq 10k\Omega$	65	100		65	100		dB
Amplifier-to-amplifier coupling[4]	f = 1kHz to 20kHz (input referred)		–120			–120		dB
Output current source	$V_{IN}+ = 1Vdc$, $V_{IN}- = 0Vdc$, $V+ = 15Vdc$	20	40		20	40		mA
Output current sink	$V_{IN}- = 1Vdc$, $V_{IN} = 0Vdc$, $V+ = 15Vdc$	10	20		10	20		mA
	$V_{IN}- = 1Vdc$, $V_{IN} = 0Vdc$, $V_{OUT} = 200mVdc$	12	50		12	50		μA
I_{SC}[5]			40	60		40	60	mA

DC ELECTRICAL CHARACTERISTICS

(Cont'd) $T_A = 25°C$, $V+ = +5V$ unless otherwise specified (see Notes on following page).

PARAMETER	TEST CONDITIONS	SA532			SE532A			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Offset voltage[1]	$R_S \leq 10k$		±2	±6		1	2	mV
	$R_S \leq 10k\Omega$, over temp.			±7.5			4	mV
V_{OS} Drift	$R_S = 0\Omega$, over temp.		7			7	15	μV°C
I_{OS} Offset current	$I_{IN}(+)$ or $I_{IN}(-)$		±5	±50		2	10	nA
I_{OS} Offset current	Over temp.			±150			30	nA
I_{OS} Drift	Over temp.		10			10	200	pA/°C
I_{BIAS} Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$		45	250		20	50	nA
	Over temp., $I_{IN}(+)$ or $I_{IN}(-)$		40	500		40	100	nA
V_{CM} Common mode voltage range[3]	$V+ = 30V$	0		V+–1.5	0		V+–1.5	V
	Over temp., $V+ = 30V$			V+–2.0	0		V+–1.5	V
C_{MRR} Common mode rejection ratio	$R_S \leq 10k\Omega$	65	70		70	85		dB
V_{OUT} Output voltage swing (V_{OH})	$R_L \geq 2k\Omega$, $V+ = 30V$	26						V
	$R_L \geq 10k\Omega$, $V+ = 30V$	27	28					V
V_{OUT} Output voltage swing (V_{OL})	$R_L \leq 10k\Omega$, over temp.		5	20				mV
I_{CC} Supply current	$R_L = \infty$ on all amplifiers, over temp.		0.5	1.2		0.5	1.2	mA
A_{VOL} Large signal voltage Gain	$R_L \geq 2k\Omega$, $V_{OUT} \pm 10V$, $V_S = \pm 15V$	25	100		50	100		V/mV
	Over temp.	15			25			V/mV
P_{SRR} Supply voltage rejection ratio	$R_S \leq 10k\Omega$	65	100		65	100		dB
Amplifier-to-amplifier coupling[4]	f = 1kHz to 20kHz (input referred)		–120			–120		dB
Output current source	$V_{IN}+ = 1Vdc$, $V_{IN}- = 0Vdc$, $V+ = 15Vdc$	20	40		20	40		mA
Output current sink	$V_{IN}- = 1Vdc$, $V_{IN} = 0Vdc$, $V+ = 15Vdc$	10	20		10	20		mA
	$V_{IN}- = 1Vdc$, $V_{IN} = 0Vdc$, $V_{OUT} = 200mVdc$	12	50		12	50		μA
I_{SC}[5]			40	60		40	60	mA

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $V+ = +5V$ unless otherwise specified.

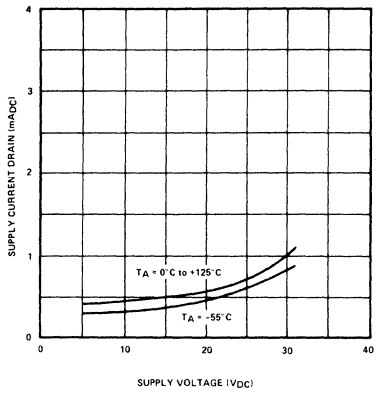
PARAMETER		TEST CONDITIONS	NE532A			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage[1]	$R_S \leq 10k$		2	3	mV
		$R_S \leq 10k\Omega$, over temp.			5	mV
V_{OS}	Drift	$R_S = 0\Omega$, over temp.		7	20	$\mu V°C$
I_{OS}	Offset current	$I_{IN}(+)$ or $I_{IN}(-)$		5	30	nA
I_{OS}	Offset current	Over temp.			75	nA
I_{OS}	Drift	Over temp.		10	300	pA/°C
I_{BIAS}	Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$		45	100	nA
		Over temp., $I_{IN}(+)$ or $I_{IN}(-)$		40	200	nA
V_{CM}	Common mode voltage range[3]	$V+ = 30V$	0		V+-1.5	V
		Over temp., $V+ = 30V$	0		V+-1.5	V
C_{MRR}	Common mode rejection ratio	$R_S \leq 10k\Omega$	65	85		dB
V_{OUT}	Output voltage swing (V_{OH})	$R_L \geq 2k\Omega$, $V+ = 30V$				V
		$R_L \geq 10k\Omega$, $V+ = 30V$				V
V_{OUT}	Output voltage swing (V_{OL})	$R_L \leq 10k\Omega$, over temp.				mV
I_{CC}	Supply current	$R_L = \infty$ on all amplifiers, over temp.		0.5	1.2	mA
A_{VOL}	Large signal voltage Gain	$R_L \geq 2k\Omega$, $V_{OUT} \pm 10V$, $V_S = \pm 15V$	25	100		V/mV
		Over temp.	15			V/mV
P_{SRR}	Supply voltage rejection ratio	$R_S \leq 10k\Omega$	65	100		dB
	Amplifier-to-amplifier coupling[4]	f = 1kHz to 20kHz (input referred)		-120		dB
	Output current source	$V_{IN}+ = 1Vdc$, $V_{IN}- = 0Vdc$, $V+ = 15Vdc$	20	40		mA
	Output current sink	$V_{IN}- = 1Vdc$, $V_{IN} = 0Vdc$, $V+ = 15Vdc$	10	20		mA
		$V_{IN}- = 1Vdc$, $V_{IN} = 0Vdc$, $V_{OUT} = 200mVdc$	12	50		μA
I_{SC}[5]				40	60	mA

NOTES

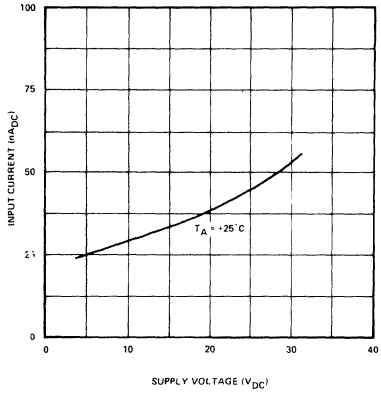
1. $V_O \cong 1.4V$, $R_S = 0\Omega$ with V+ from 5V to 30V; and over the full input common-mode range (9V to V+ -1.5V).
2. The direction of the input current is out of the IC due to the pnp input stage. This current is essentially contant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ -1.5V, but either or both inputs can go to +32V without damage.
4. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive coupling increases at higher frequencies.
5. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15Vdc, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.

TYPICAL PERFORMANCE CHARACTERISTICS

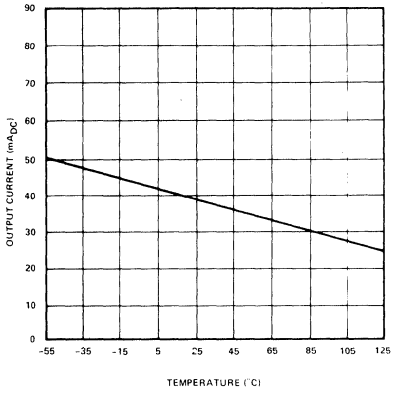
SUPPLY CURRENT



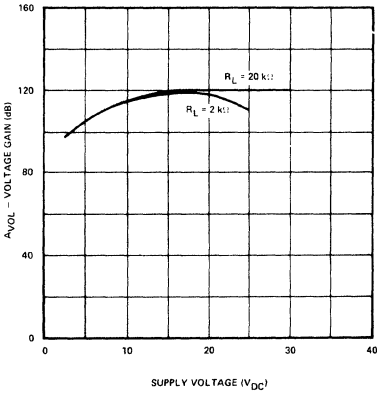
INPUT CURRENT



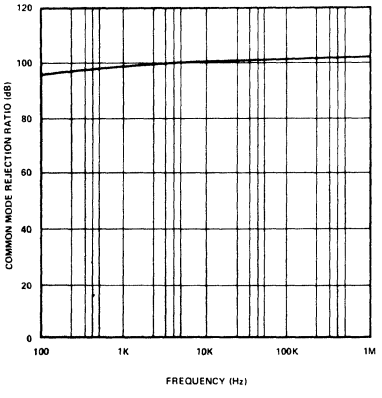
CURRENT LIMITING



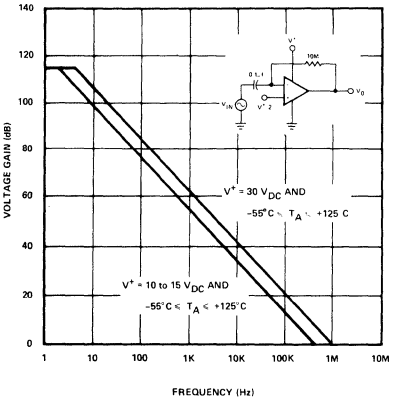
VOLTAGE GAIN



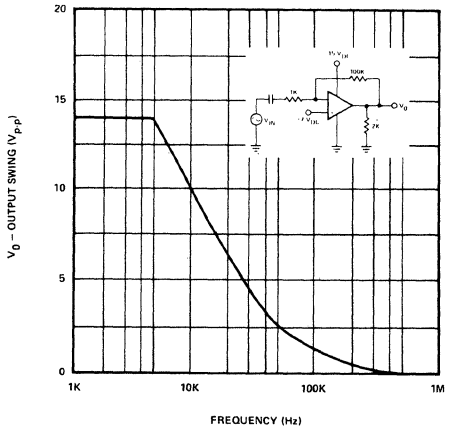
COMMON-MODE REJECTION RATIO



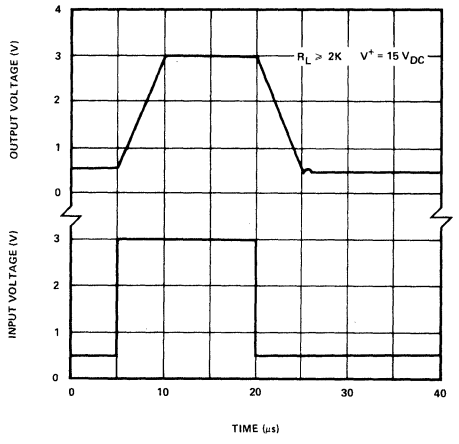
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE



VOLTAGE FOLLOWER PULSE RESPONSE



NE/SE535-T • NE/SE5535-F,K,N,N-14

DESCRIPTION

The 535 and 5535 are new generation operational amplifiers featuring high slew rates combined with improved input characteristics. The 535 is a single device while the 5535 is a dual configuration. Internally compensated for unity gain, the SE535 and SE5535 feature a guaranteed unity gain slew rate of 10V/μs with 2mV maximum offset voltage. Industry standard pin out and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers, such as 741, 747 and 1558.

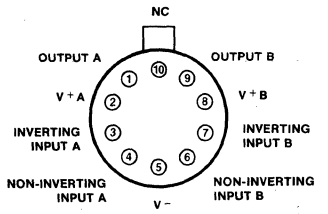
FEATURES

- **15V/μs unity gain slew rate**
- **Internal frequency compensation**
- **Low input offset voltage—2mV max**
- **Low input bias current 60nA max**
- **Short circuit protected**
- **Offset null capability**
- **Large common mode and differential voltage ranges**

	535	5535
• **Pin out**	**741**	**747,1558**
• **Configuration**	**Single**	**Dual**

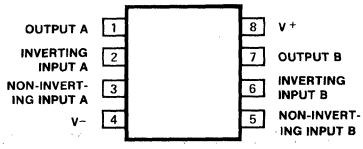
PIN CONFIGURATIONS

K PACKAGE



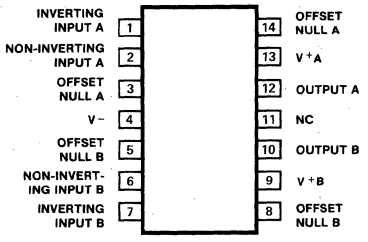
ORDER PART NO.
SE5535K NE5535K

N PACKAGE



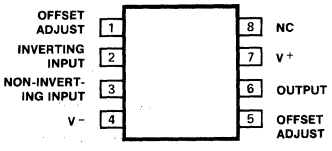
ORDER PART NO.
SE5535N NE5535N

F,N-14 PACKAGE



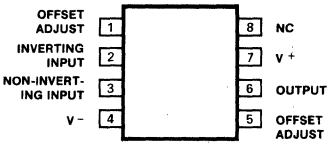
ORDER PART NO.
SE5535N-14 SE5535F
NE5535N-14 NE5535F

N PACKAGE



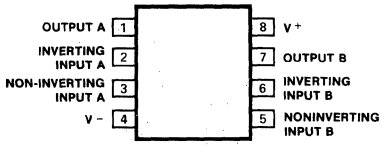
ORDER PART NO.
SE535N NE535N

T PACKAGE



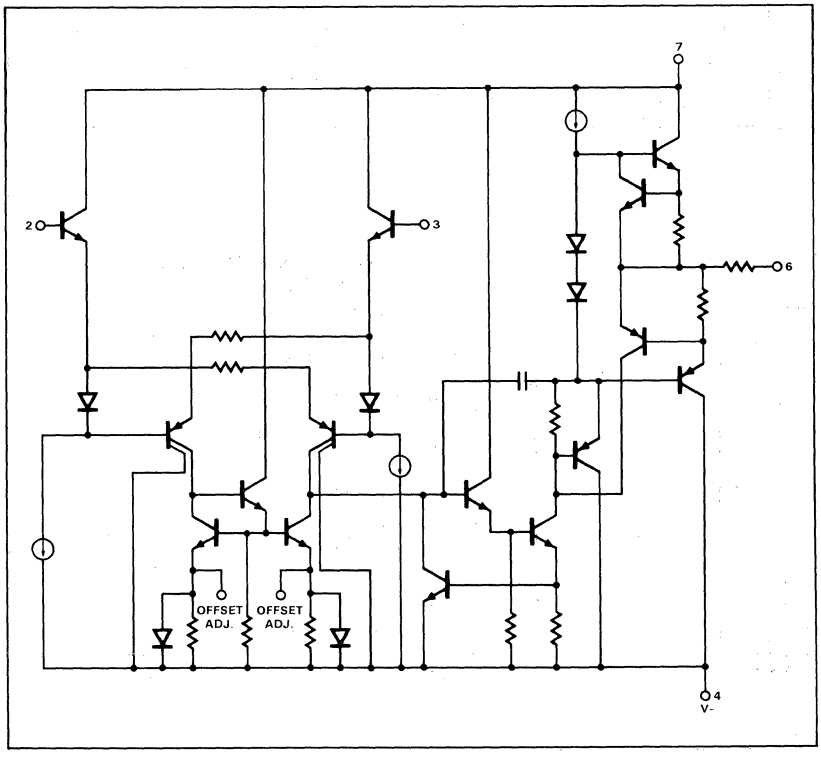
ORDER PART NO.
SE535T NE535T

T PACKAGE



ORDER PART NO.
SE5535T NE5535T

EQUIVALENT SCHEMATIC (One Amplifier)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SE535/ SE5535	NE535/ NE5535	UNIT
Supply voltage	±22	±18	V
Internal power dissipation[1]			
N Package	500	500	mW
K/T Package	800	800	mW
F Package	1000	1000	mW
Differential input voltage	±30	±30	V
Input voltage[2]	±15	±15	V
Operating temperature range	-55 to +125	0 to +70	°C
Storage temperature range	-65 to +150	-65 to +150	°C
Lead temperature (solder, 60sec)	300	300	°C
Output short circuit[3]	Indefinite	Indefinite	

NOTES

1. Rating applies for thermal resistances junction to ambient of 240°C/W and 150°C/W for N and K, T packages, respectively. Maximum chip temperature is 150°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.*

PARAMETER		TEST CONDITIONS	SE535/SE5535			NE535/NE5535			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S \leq 10k\Omega$ $R_S \leq 10k\Omega$, over temp.		0.7	2.0 3.0		2.0	5.0 6.0	mV mV
ΔV_{OS}	Input offset voltage drift	$R_S = 0\Omega$, over temp.		3.0	15		6.0		V/°C
I_{OS}	Input offset current	 Over temp.		5	10 20		15	40 80	nA μVnA
I_B	Input current	 Over temp.		45	60 100		65	150 200	nA nA
V_{CM} CMRR	Common mode voltage range Common mode rejection ratio	 $R_S \leq 10k\Omega$, over temp.	±12 70	±13 90		±12 70	±13 90		V dB
P_{SRR}	Power supply rejection	$R_S \leq 10k\Omega$, over temp.		30	150		30	150	μV/V
R_{IN}	Input resistance		3	10		1	6		MΩ
A_{VOL}	Large signal voltage gain	$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$ $R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$, over temp.	50 25	500		50 25	500		V/mV V/mV
V_{OUT}	Output voltage	$R_L \geq 2k\Omega$, over temp. $R_L \geq 10k\Omega$, over temp.	±10 ±12	±13 ±14		±10 ±12	±13 ±14		V V
I_{CC}	Supply current	Per amplifier Per amplifier, over temp.		1.8 2	2.8 3.3		1.8 2	2.8	mA mA
P_D	Power dissipation	Per amplifier Per amplifier, over temp.		54 60	84 99		54 60	84	mW mW
I_{SC}	Output short circuit current			25			25		mA
R_{OUT}	Output resistance			100			100		Ω

*NOTE

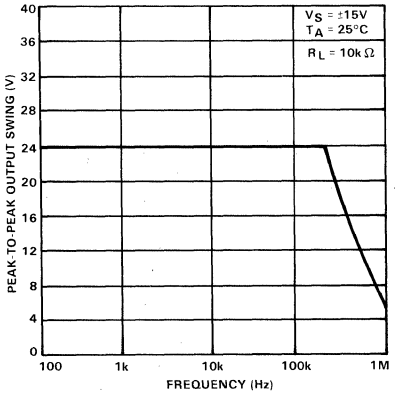
Temperature range
SE types $-55°C \leq T_A \leq 125°C$
NE types $0°C \leq T_A \leq 70°C$

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

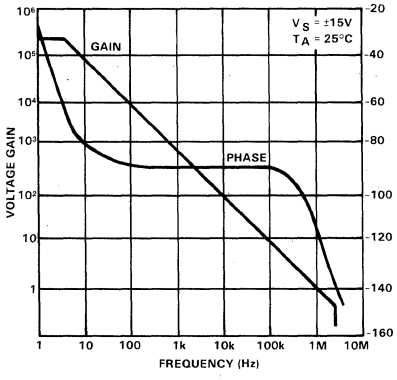
PARAMETER	TEST CONDITIONS	SE535/SE5535			NE535/NE5535			UNIT
		Min	Typ	Max	Min	Typ	Max	
Gain/bandwidth product			1			1		MHz
Transient response								
Small signal rise time			0.25			0.25		μs
Small signal overshoot			6			6		%
Settling time	To 0.1%		3			3		μs
Slew rate	$T_A = 25C$, $R_L \geq 10k\Omega$, unity gain, non-inverting	10	15		10	15		V/μs

TYPICAL PERFORMANCE CHARACTERISTICS

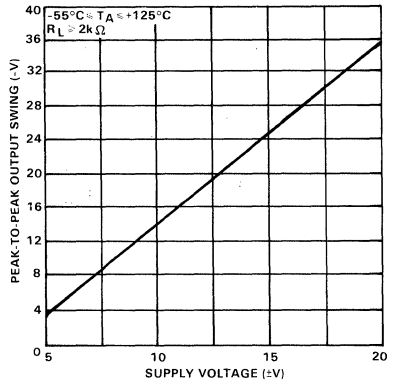
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



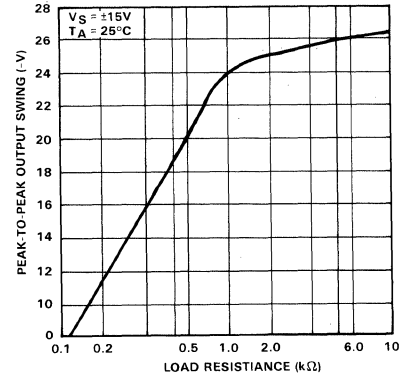
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

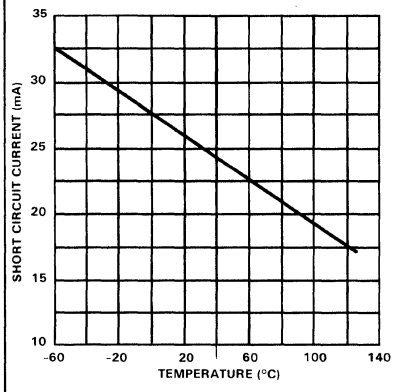


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

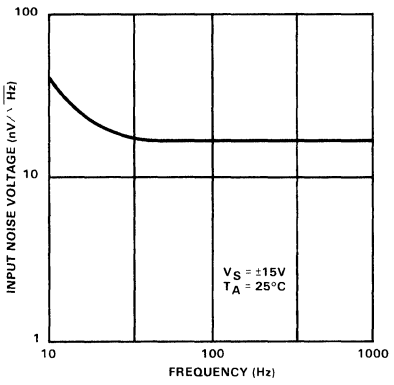


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

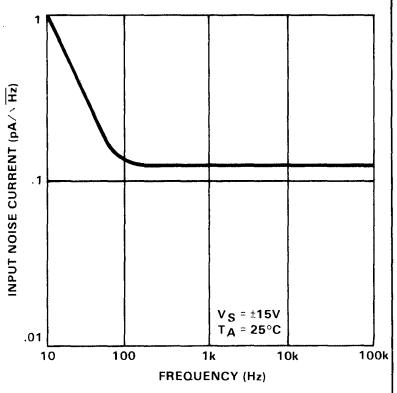
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



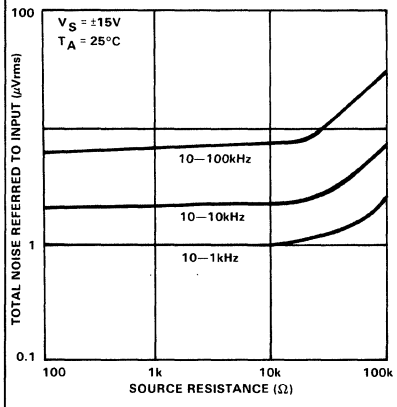
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



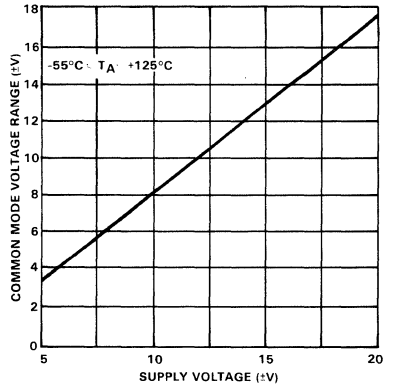
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



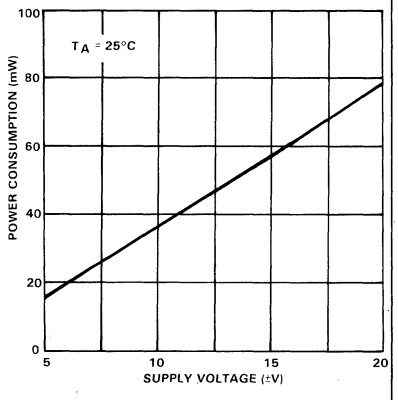
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



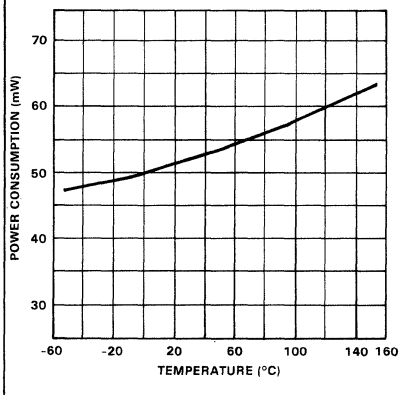
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



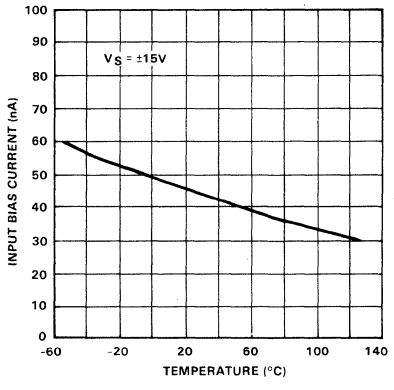
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



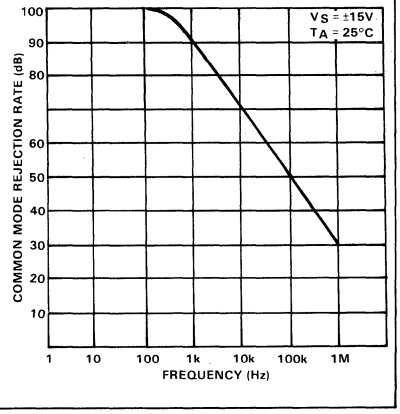
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

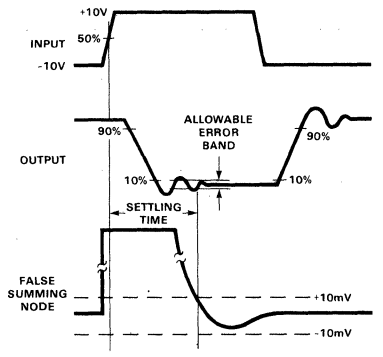


COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY

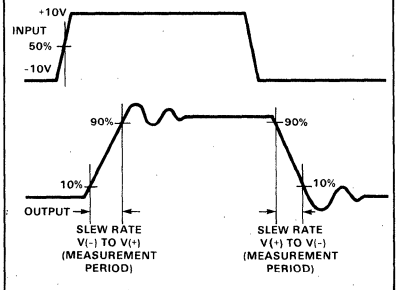


VOLTAGE WAVEFORMS

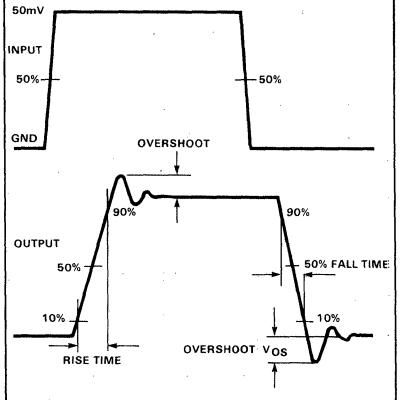
SETTLING TIME MEASUREMENT



SLEW RATE MEASUREMENT

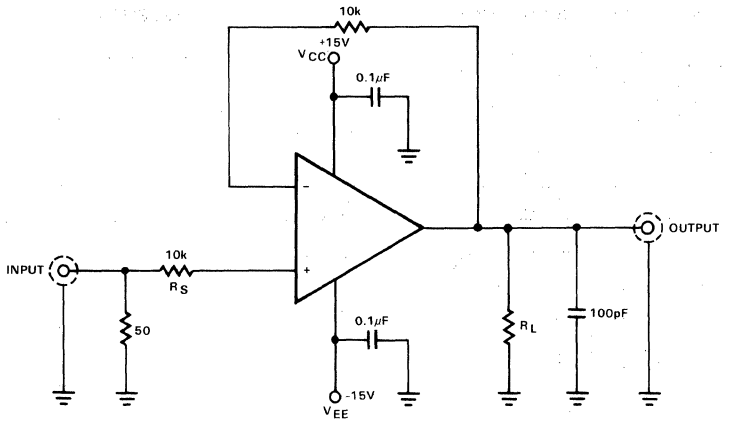


SMALL-SIGNAL TRANSIENT RESPONSE DEFINITIONS



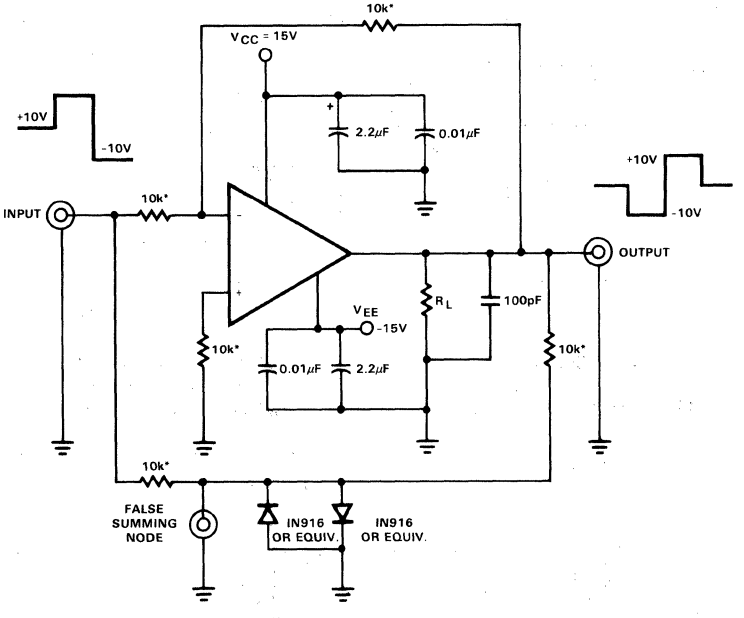
TEST CIRCUITS

SLEW RATE AND SMALL SIGNAL TRANSIENT RESPONSE



NOTE
Pins not shown are not connected.
All resistors values are typical and in ohms.

SETTLING TIME



*Match to within 0.01%.

NOTE

Pins not shown are not connected.
All resistors values are typical and in ohms.

NE/SU536-T

DESCRIPTION

The 536 is a special purpose high performance operational amplifier utilizing an FET input stage for extremely high input impedance and low input current.

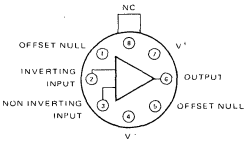
The device features internal compensation, standard pinout, wide differential and common mode input voltage range, high slew rate and high output drive capability.

FEATURES

- **5pA input bias current**
- **Input and output protection**
- **Offset null capability**
- **Internally compensated**
- **6V/μsec slew rate**
- **Standard pinout**
- **1MHz unity gain bandwidth**

PIN CONFIGURATION

T PACKAGE



ORDER PART NO.
SU536T
NE536T

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	±22	V
Differential input voltage range	±30	V
Common mode input voltage range	$\pm V_S$	
Power dissipation[1]	500	mW
Operating temperature range		
SU536T	-55 to +85	°C
NE536T	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (solder, 60sec)	300	°C
Output short circuit duration[2]	indefinite	

NOTES

1. Rating applies for case temperature to +25°C; derate linearly at 6.5mW/°C for ambient temperatures above 75°C.
2. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = ±15V unless otherwise specified.[1]

PARAMETER		TEST CONDITIONS	NE536			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \leq 10k\Omega$		30	90	mV
		Over temp., $R_S \leq 10k\Omega$		30		mV
V_{OS}	Drift	$R_S = 0\Omega$, over temp.		30		μV/°C
I_{OS}	Offset current			5		pA
I_{BIAS}	Input current[2]			30	100	pA
V_{CM}	Common mode voltage range		±10	±11		V
CMRR	Common mode rejection ratio	$R_S \leq 10k\Omega$, $V_{IN} = \pm 10V$	64	80		dB
R_{IN}	Input resistance			10^{14}		Ω
V_{OUT}	Output voltage swing	$R_L \geq 2k\Omega$, over temp.	±10	±11		V
		R_L 10kΩ, over temp.	±12	±13		V
I_{CC}	Supply current	V_{OUT} = OV		6.0	8.0	mA
P_{SRR}	Supply voltage rejection ratio	$R_S \leq 10k\Omega$, $\pm 6 \leq V_S \pm 15$		100	300	μV/V
A_{VOL}	Large signal voltage gain	$V_O = \pm 10V$, R_L 2kΩ	50			V/mV
		$V_O = \pm 10V$, $R_L \geq 2k\Omega$, over temp.	25			V/mV
P_S	Power supply range		±6	±18		V

NOTES

1. Operating temperature range: NE536 is 0°C to 70°C.
2. Input current typically doubles every 10°C.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $\pm6V \leq V_S \leq \pm 20V$ unless otherwise specified.[2]

PARAMETER	TEST CONDITIONS	SU536			UNIT
		Min	Typ	Max	
V_{OS} Offset voltage	$R_S \leq 10k\Omega$ $R_S \leq 10k\Omega$, over temp.		7.5 7.5	20 30	mV mV
V_{OS} Drift	$R_S \leq 10k\Omega$		20		$\mu V/°C$
I_{OS} Offset current			5		pA
I_{BIAS} Input current[1]	 Over temp.		5 250	30 3000	pA pA
V_{CM} Common mode voltage range CMRR Common mode rejection ratio	$V_S = \pm15V$ $R_S \leq 10k\Omega$, $V_{IN} = \pm10V$	±10 70	±11 80		V dB
R_{IN} Input resistance			10^{14}		Ω
V_{OUT} Output voltage swing	$R_L \geq 2k\Omega$, $V_S = \pm15V$, over temp. $R_L \geq 10k\Omega$, $V_S = \pm15V$, over temp.	±10 ±12	±12 ±13		V V
I_{CC} Supply current	$V_{OUT} = OV$, $V_S = \pm20V$		4.5	5.5	mA
P_{SRR} Supply voltage rejection ratio	$R_S \leq 10k\Omega$		50	150	$\mu V/V$
A_{VOL} Large signal voltage gain	Over temp., $V_S = \pm15V$, $V_O = \pm10V$, $R_L \geq 2k\Omega$	50			V/mV
P_S Power supply range		±6		±20	V

NOTES

1. Input current typically doubles every 10°C.
2. Operating temperature range for SU536 is -55°C to +85°C.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.[1,2]

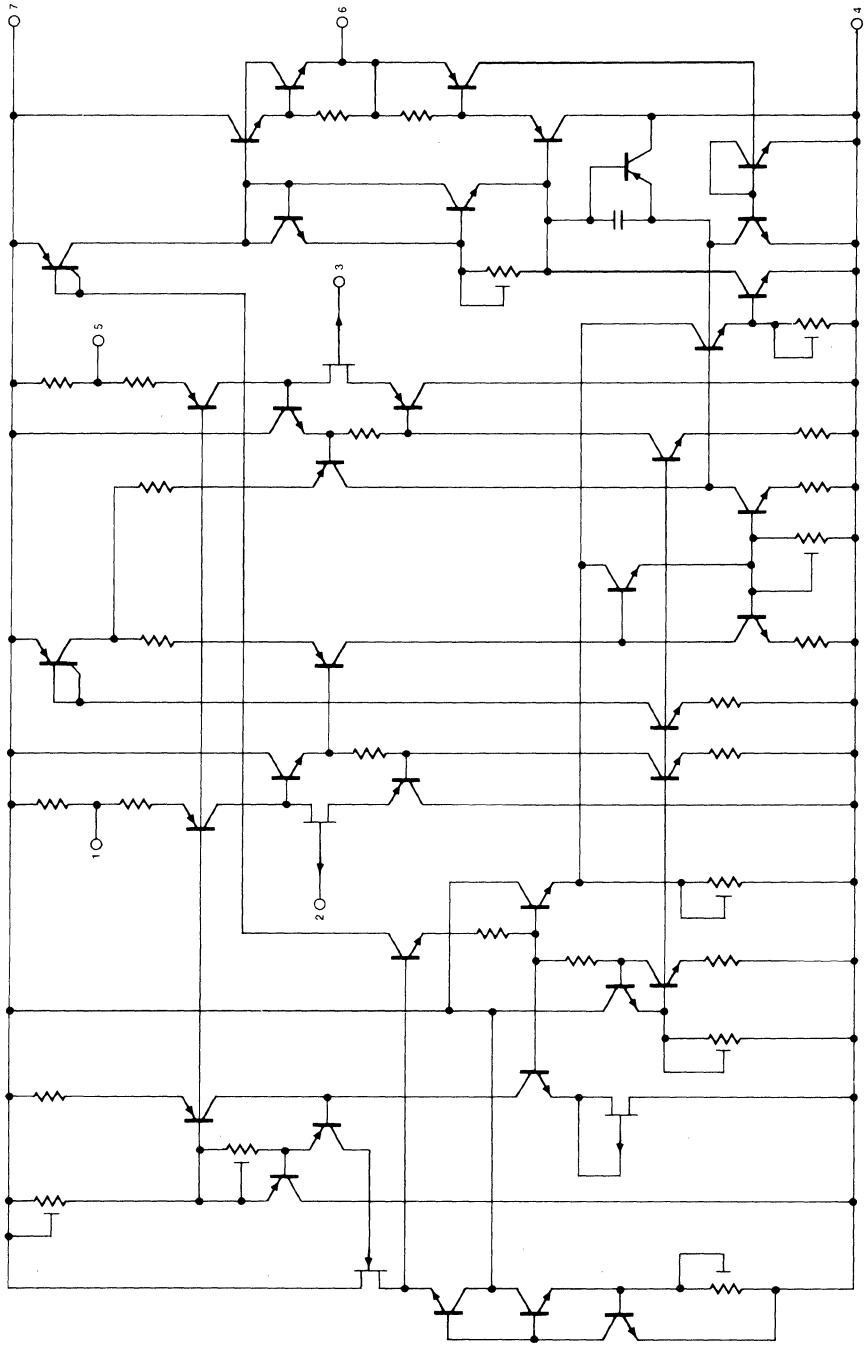
PARAMETER	TEST CONDITIONS	NE536			SU536			UNIT
		Min	Typ	Max	Min	Typ	Max	
Differential capacitance			6			6		pF
Input noise voltage	0.1Hz — 100kHz		20			20		μVrms
Output impedance			100			100		
Unity gain frequency Full power bandwidth	$V_S = \pm15V$ $V_S = \pm15V$		1 100			1 100		MHz KHz
Slew rate, inverter Slew rate, follower	$V_S = \pm15V$, A = -1V $V_S = \pm15V$, A = +1V		6 6			6 6		V/μs V/μs

NOTES

1. Temperature range for SU536 is $-55 \leq T_A \leq 85°C$
   Temperature range for NE536 is $0°C \leq T_A \leq 70°C$
2. SU536 — $\pm6V \leq T_A \pm 20V$
   NE536 — $\pm15V$

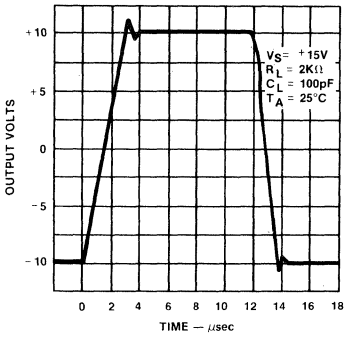
NE/SU536-T

CIRCUIT SCHEMATIC

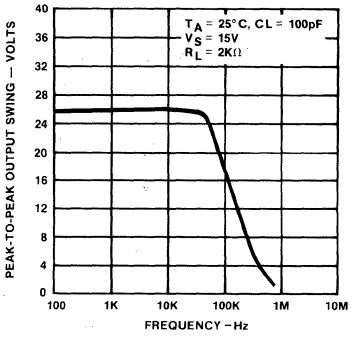


TYPICAL PERFORMANCE CHARACTERISTICS

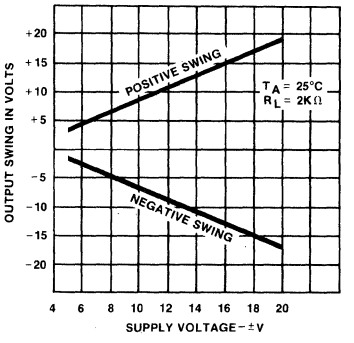
LARGE SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE



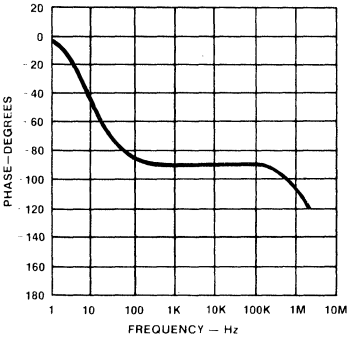
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



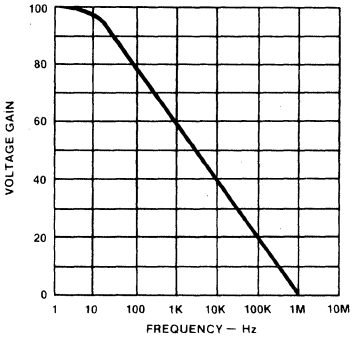
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



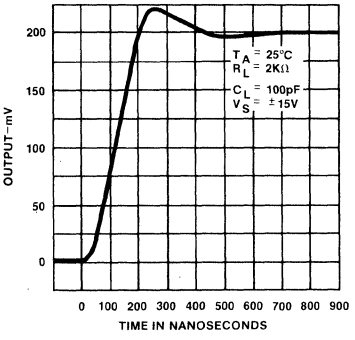
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



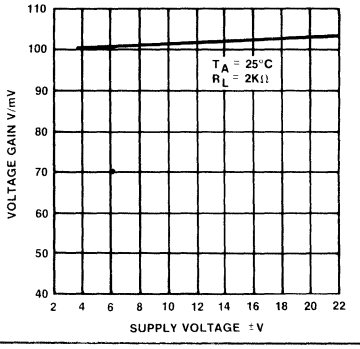
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



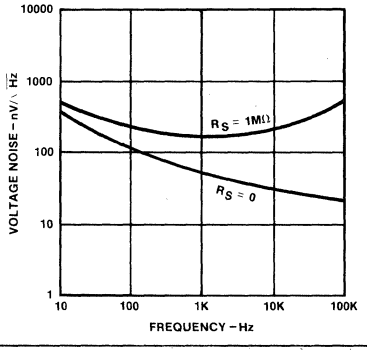
VOLTAGE FOLLOWER TRANSIENT RESPONSE



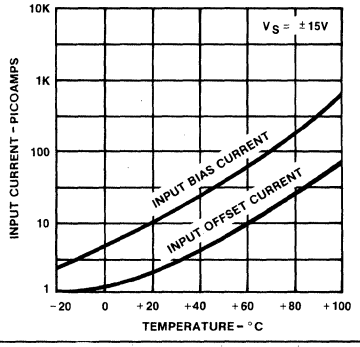
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



INPUT VOLTAGE NOISE AS A FUNCTION OF FREQUENCY

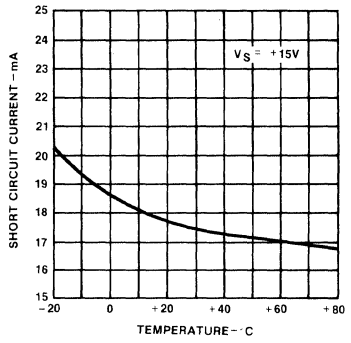


INPUT CURRENTS AS A FUNCTION OF AMBIENT TEMPERATURE



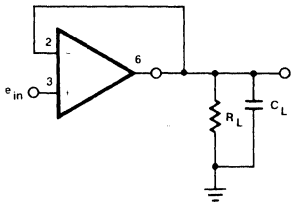
TYPICAL PERFORMANCE CHARACERISTICS (Cont'd)

OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

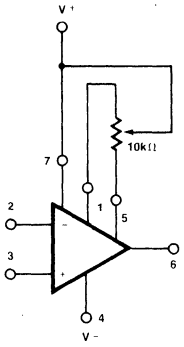


TEST CIRCUITS

VOLTAGE FOLLOWER CIRCUIT



OFFSET NULL CIRCUIT



NE/SE538-N,T • NE/SE5538-F,K,N,N-14,T

DESCRIPTION

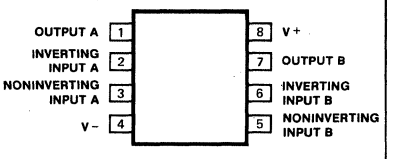
The 538/5538 are new generation operational amplifiers featuring high slew rates combined with improved input characteristics. Internally compensated for gains of 5 or larger, the SE538/SE5538 offer guaranteed minimum slew rates of 40V/μs or larger. Featuring 2mV max input offset voltage, the 538 is a single amplifier while the 5538 is a dual version. Industry standard pin out and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers, such as 748, 101A, 741, 747 and 1458.

FEATURES

- **2mV max input offset voltage**
- **60nA max input offset current**
- **Short circuit protected**
- **Offset null capability**
- **Large common mode and differential voltage ranges**
- **60V/μs slew rate (gain of +5, -4 min)**
- **6MHz gain bandwidth product (gain +5, -4 minimum)**
- **Internal frequency compensation (gain of +5, -4 minimum)**
- **Pin out: 538 same as 741 (single)**
  5538 same as 747, 1458 (dual)

PIN CONFIGURATIONS

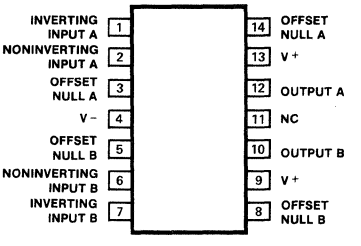
N PACKAGE



ORDER PART NO.

SE5538N, NE5538N

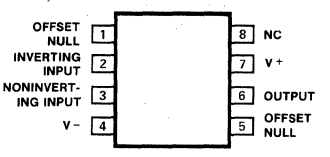
N-14, F PACKAGE



ORDER PART NO.

SE5538 N-14, F
NE5538 N-14, F

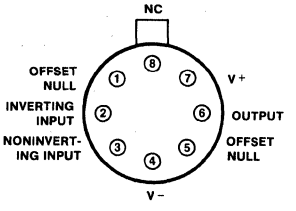
N PACKAGE



ORDER PART NO.

SE538N, NE538N

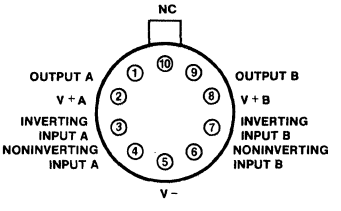
T PACKAGE



ORDER PART NO.

SE538T, NE538T

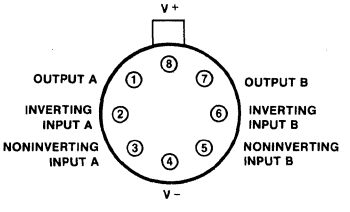
K PACKAGE



ORDER PART NO.

SE5538K, NE5538K

T PACKAGE



ORDER PART NO.

SE5538T, NE5538T

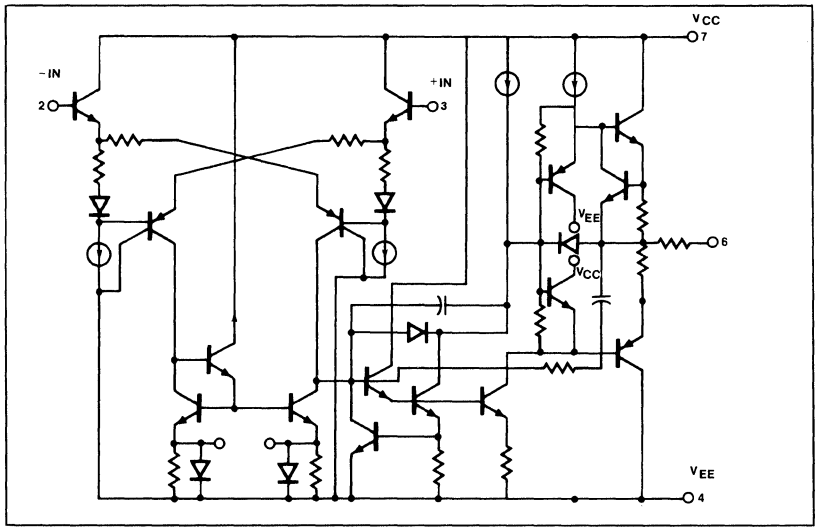
ABSOLUTE MAXIMUM RATINGS[1,2,3]

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		
	SE military grade	±22	V
	NE commercial grade	±18	V
P_D	Internal power dissipation F package	1000	mW
P_D	Internal power dissipation[1] N package	500	mW
P_D	Internal power dissipation[1] K, T package	800	mW
	Differential input voltage	±30	V
	Input voltage[2]	±15	V
	Operating temperature range		
	SE military grade	-55 to +125	°C
	NE commercial grade	0 to 70	°C
	Output short circuit[3]	indefinite	
	Storage temperature range	-65 to +150	°C
	Lead temperature (solder, 60sec.)	300	°C

NOTES

1. Rating applies for thermal resistances of 240°C/W and 150°C/W junction to ambient for N and K, T packages, respectively. Maximum chip temperature is 150°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

EQUIVALENT SCHEMATIC (EACH AMPLIFIER)



DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SE538/SE5538			NE538/NE5538			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S \leq 10k\Omega$		0.7	2.0		2.0	5.0	mV
V_{OS}	Input offset voltage	$R_S \leq 10k\Omega$, over temp.			3.0			6.0	mV
ΔV_{OS}	Input offset voltage drift	$R_S = 0\Omega$, over temp.		3.0	15		6.0		$\mu V/°C$
I_{OS}	Input offset current			5	10		15	40	nA
I_{OS}	Input offset current	Over temp.			20			80	nA
I_B	Input current			45	60		65	150	nA
I_B	Input current	Over temp.			100			200	nA
V_{CM}	Input common mode voltage range		±12	±13		±12	±13		V
C_{MRR}	Common mode rejection ratio	$R_S \leq 10k\Omega$, over temp.	70	90		70	90		dB
P_{SRR}	Power supply rejection	$R_S \leq 10k\Omega$, over temp.		30	150		30	150	$\mu V/V$
R_{IN}	Input resistance		3	10		1	6		MΩ
A_{VOL}	Large signal voltage gain	$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	50	200		50	200		V/mV
A_{VOL}	Large signal voltage gain	Over temp., $R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	25			25			V/mV
V_{OUT}	Output voltage	Over temp., $R_L \geq 2k\Omega$	±10	±13		±10	±13		V
V_{OUT}	Output voltage	Over temp., $R_L \geq 10k\Omega$	±12	±14		±12	±14		V
I_{CC}	Supply current	Per amplifier		2	3		2	3	mA
I_{CC}	Supply current	Over temp., per amplifier		2.2	3.6		2.2		mA
P_D	Power dissipation	Per amplifier		60	90		60	90	mW
P_D	Power dissipation	Over temp., per amplifier		66	108		66		mW
I_{SC}	Output short circuit current			25			25		mA
R_{OUT}	Output resistance			100			100		Ω

NOTE

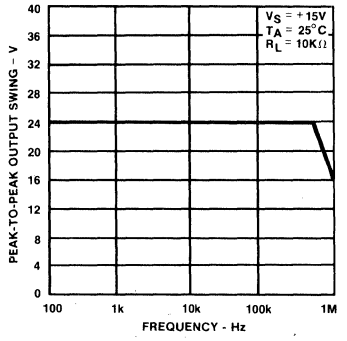
Temperature Range
SE Types $-55°C \leq T_A \leq 125°C$
NE Types $0°C \leq T_A \leq 70°C$

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

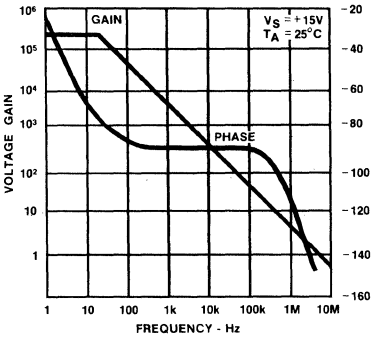
PARAMETER	TEST CONDITIONS	SE538/SE5538			NE538/NE5538			UNIT
		Min	Typ	Max	Min	Typ	Max	
Gain bandwidth product (Gain +5, -4 minimum)			6			6		MHz
Transient response Small signal rise time Small signal overshoot			0.25 6			0.25 6		μs %
Settling time	To 0.1%		1.2			1.2		μs
Slew rate	Minimum gain = 5 Noninverting $R_L \geq 2k\Omega$	40	60			60		V/μs

TYPICAL PERFORMANCE CHARACTERISTICS

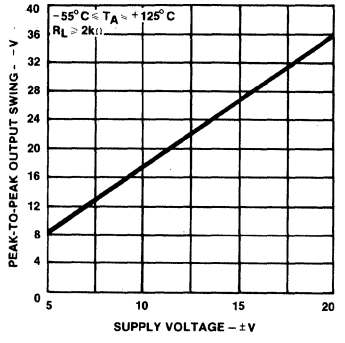
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



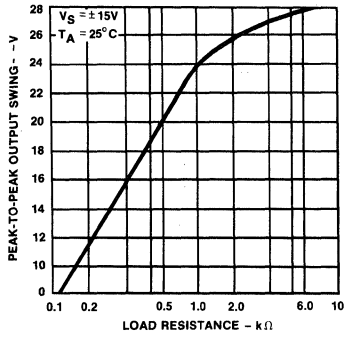
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



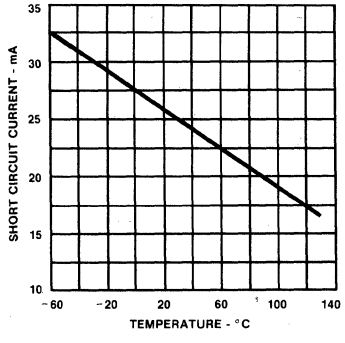
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



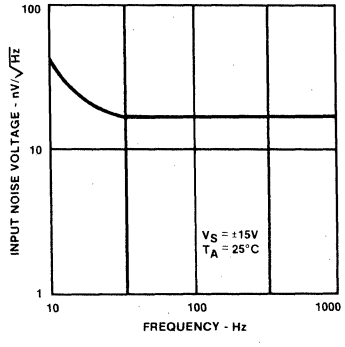
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

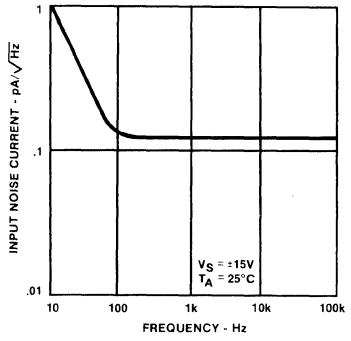


INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY

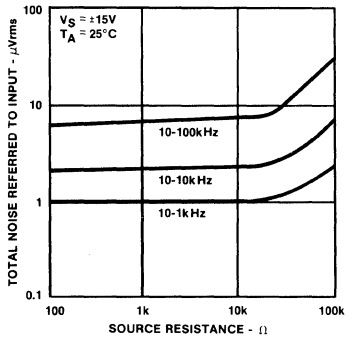


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

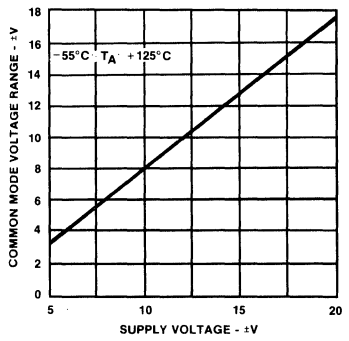
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



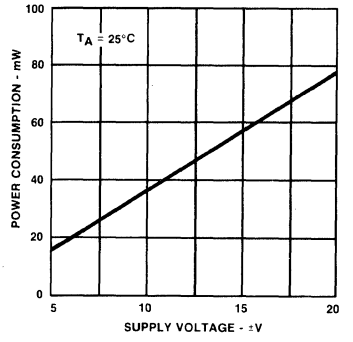
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



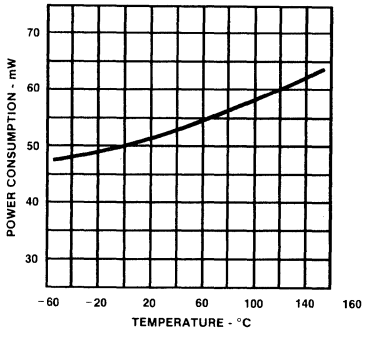
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



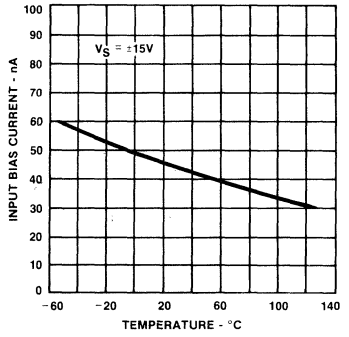
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



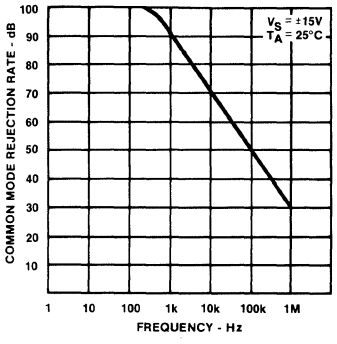
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



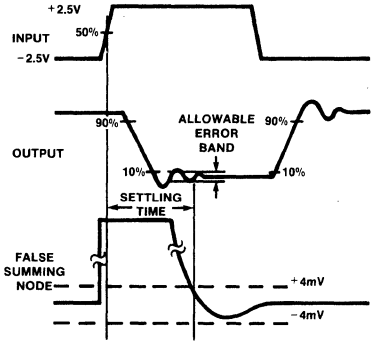
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



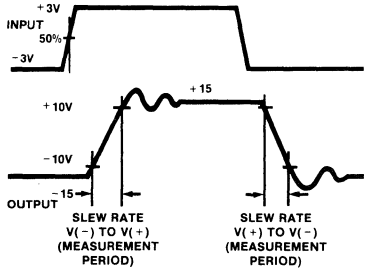
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



SETTLING TIME MEASUREMENT WAVEFORMS

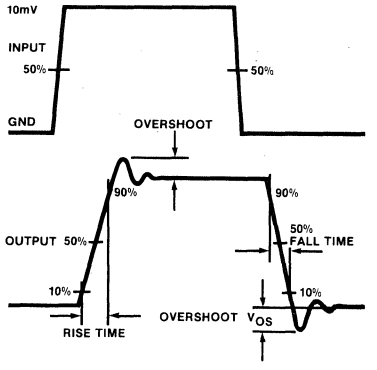


SLEW RATE MEASUREMENT VCC = ±20V



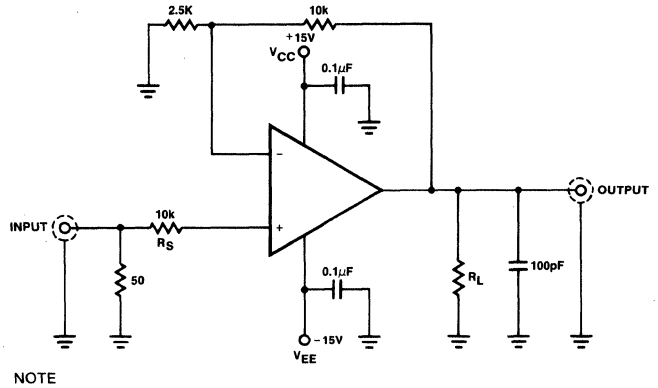
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

SMALL-SIGNAL TRANSIENT RESPONSE DEFINITIONS



TEST LOAD CIRCUITS

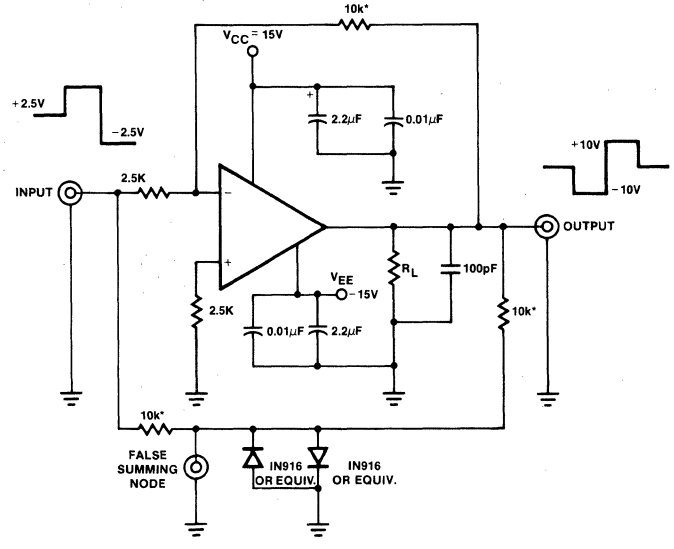
SLEW RATE AND SMALL SIGNAL TRANSIENT RESPONSE TEST CIRCUIT



NOTE
Pins not shown are not connected.
All resistors values are typical and in ohms.

TEST LOAD CIRCUITS (Cont'd)

SETTLING TIME TEST CIRCUIT



*Match to within 0.01%.
NOTE
Pins not shown are not connected.
All resistors values are typical and in ohms.

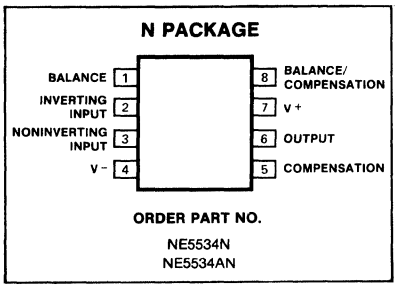
NE/SE5534, NE/SE5534A-N,T

DESCRIPTION

The SE/NE5534 is a high-performance low noise operational amplifier. Compared to most of the standard operational amplifiers, such as 741 and 301A, it shows better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

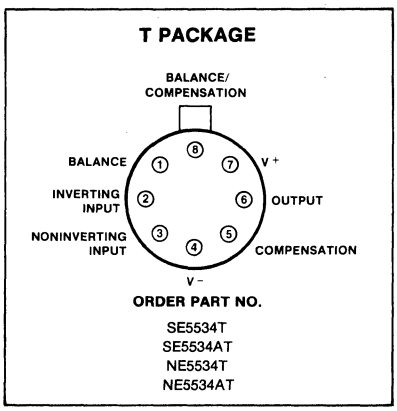
This makes the device especially suitable for application in high quality and professional audio equipment, in instrumentation and control circuits and telephone channel amplifiers. The op amp is internally compensated for gain equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew-rate, low overshoot, etc.) If very low noise is of prime importance, it is recommended that the SE/NE5534A version be used which has guaranteed noise specifications.

PIN CONFIGURATIONS



ORDER PART NO.

NE5534N
NE5534AN



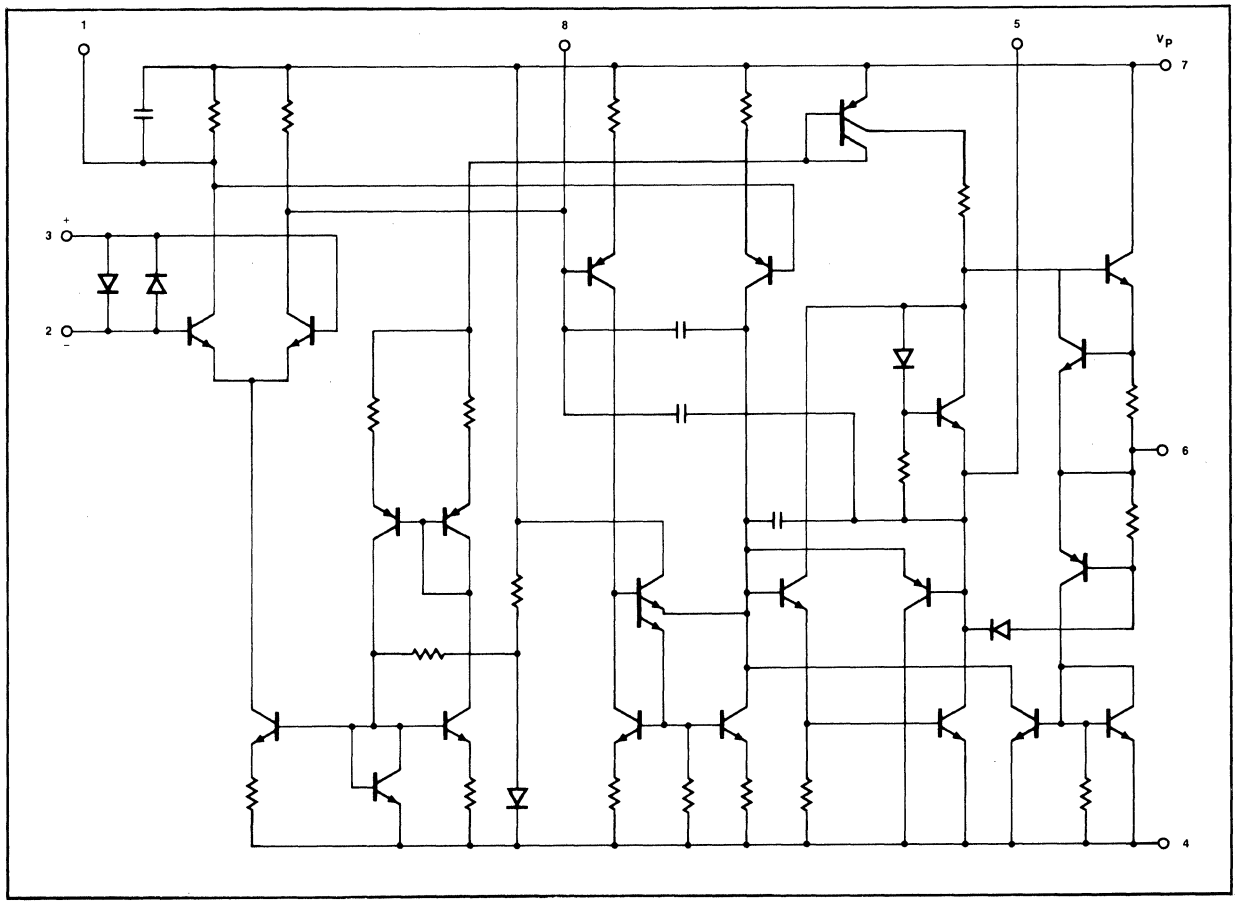
ORDER PART NO.

SE5534T
SE5534AT
NE5534T
NE5534AT

FEATURES

- **Small-signal bandwidth: 10MHz**
- **Output drive capability: 600Ω, 10V (rms) at $V_S = \pm 18V$**
- **Input noise voltage: 4nV/$\sqrt{Hz}$**
- **DC voltage gain: 100000**
- **AC voltage gain: 6000 at 10kHz**
- **Power bandwidth: 200kHz**
- **Slew-rate: 13V/μs**
- **Large supply voltage range: ±3 to ±20V**

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_S	Supply voltage	±22	V
V_{IN}	Input voltage	±V supply	V
V_{DIFF}	Differential input voltage	±.5	V
T_A	Operating temperature range[1]		
	SE	-55 to +125	°C
	NE	0 to 70	°C
T_{STG}	Storage temperature	-65 to +150	°C
T_J	Junction temperature	150	°C
P_D	Power dissipation		
	5534T	680	mW
	5534N	500	mW
	Output short circuit duration [2]	indefinite	
	Lead temperature (soldering 10 sec)[3]	300	°C

NOTES

1. Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
2. For operation at elevated temperature T package must be derated based on a thermal resistance of 150°C/W junction to ambient, 45°C/W junction to case. Thermal resistance of the N package is 240°C/W.
3. Output may be shorted to ground at $V_S = \pm 15V$, $T_A = 25°C$. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.[1,2]

PARAMETER		TEST CONDITIONS	SE5534/5534A			NE5534/5534A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage			.5	2		.5	4	mV
		Over temperature			3			5	mV
I_{OS}	Offset current			10	200		20	300	nA
		Over temperature			500			400	nA
I_B	Input current			400	800		500	1500	nA
		Over temperature			1500			2000	nA
I_{CC}	Supply current			4	6.5		4	8	mA
		Over temperature			9				mA
V_{CM}	Common mode input range		±12	±13		±12	±13		V
CMRR	Common mode rejection ratio		80	100		70	100		dB
PSRR	Power supply rejection ratio			10	50		10	100	μV/V
A_{VOL}	Large signal voltage gain	$R_L \geq 600\Omega$, $V_O = \pm 10V$	50	100		25	100		V/mV
		Over temperature	25			15			V/mV
V_{OUT}	Output swing	$R_L \geq 600\Omega$	±12	±13		±12	±13		V
		$R_L \geq 600\Omega$ $V_S = \pm 18V$	±15	±16		±15	±16		V
R_{IN}	Input resistance		50	100		30	100		KΩ
I_{SC}	Output short circuit current			38			38		mA

NOTES

1. For NE5534, NE5534A, $T_{MIN} = 0°C$, $T_{MAX} = 70°C$
2. For SE5534, SE5534A, $T_{MIN} = -55°C$, $T_{MAX} = +125°C$

NE/SE5534, NE/SE5534A-N,T

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

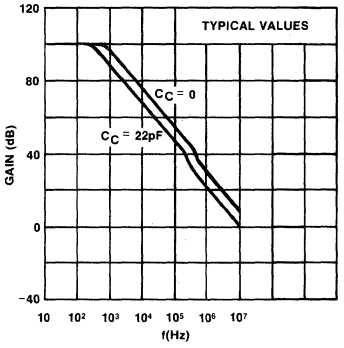
PARAMETER	TEST CONDITIONS	SE5534/5534A			NE5534/5534A			UNIT
		Min	Typ	Max	Min	Typ	Max	
R_{OUT} Output resistance	A_V = 30dB closed loop f = 10kHz, $R_L = 600\Omega$, $C_C = 22pF$		0.3			0.3		Ω
Transient response	Voltage follower, V_{IN} = 50mV $R_L = 600\Omega$, $C_C = 22pF$, $C_L = 100pF$							
T_R Rise time			20			20		ns
Overshoot			20			20		%
Transient response	V_{IN} = 50mv, $R_L = 600\Omega$ C_C = 47pF, C_L = 500pF							
T_R Rise time			50			50		ns
Overshoot			35			35		%
AC Gain	f = 10kHz, C_C = 0		6			6		V/mV
	f = 10kHz, C_C = 22pF		2.2			2.2		V/mV
Gain bandwidth product	C_C = 22pF, C_L = 100pF		10			10		mHz
Slew rate	C_C = 0		13			13		V/μS
	C_C = 22pF		6			6		V/μS
Power bandwidth	$V_{OUT} = \pm 10V$, C_C = 0		200			200		kHz
	$V_{OUT} = \pm 10V$, C_C = 22pF		95			95		kHz
	$V_{OUT} = \pm 14V$, $R_L = 600\Omega$		70			70		kHz
	C_C = 22pF, $V_{CC} = \pm 18V$							

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

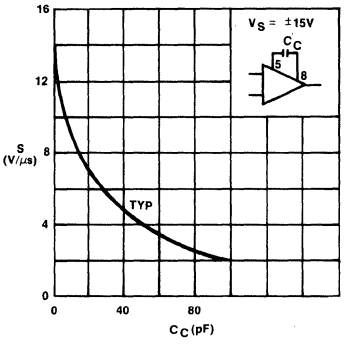
PARAMETER	TEST CONDITIONS	SE5534/NE5534			SE5534A/NE5534A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input noise voltage	f_o = 30Hz		7			5.5	7	$nV/\sqrt{Hz}$
	f_o = 1kHz		4			3.5	4.5	$nV/\sqrt{Hz}$
Input noise current	f_o = 30Hz		2.5			1.5		$pA/\sqrt{Hz}$
	f_o = 1kHz		0.6			0.4		$pA/\sqrt{Hz}$
Broadband noise figure	f = 10Hz - 20kHz, $R_S = 5k\Omega$		-			0.9		dB

TYPICAL PERFORMANCE CHARACTERISTICS

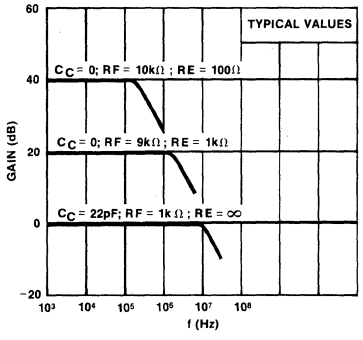
OPEN LOOP FREQUENCY RESPONSE



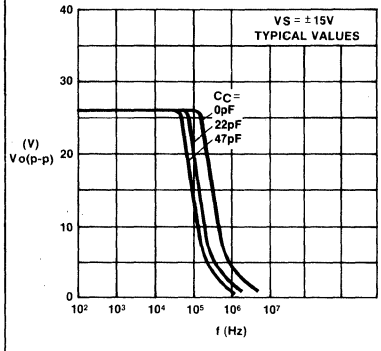
SLEW-RATE AS A FUNCTION OF COMPENSATION CAPACITANCE



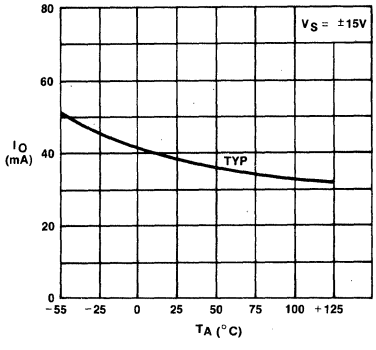
CLOSED LOOP FREQUENCY RESPONSE



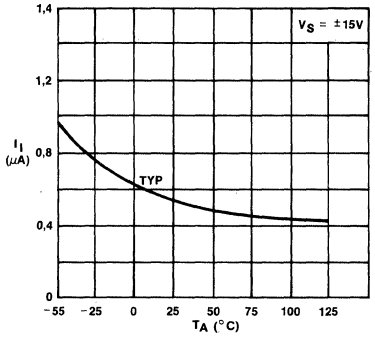
LARGE-SIGNAL FREQUENCY RESPONSE



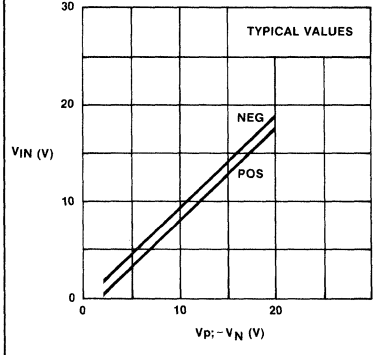
OUTPUT SHORT-CIRCUIT CURRENT



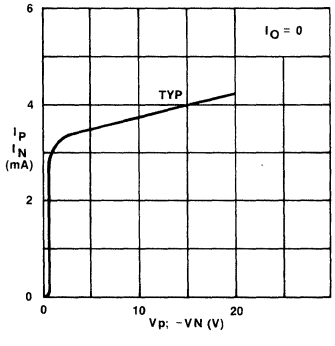
INPUT BIAS CURRENT



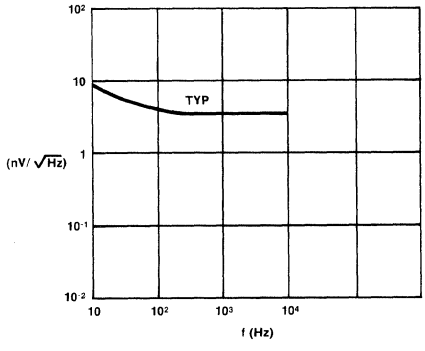
INPUT COMMON MODE VOLTAGE RANGE



SUPPLY CURRENT

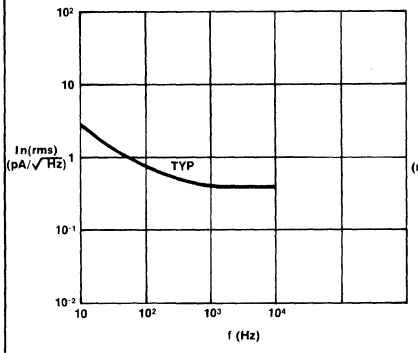


INPUT NOISE VOLTAGE DENSITY

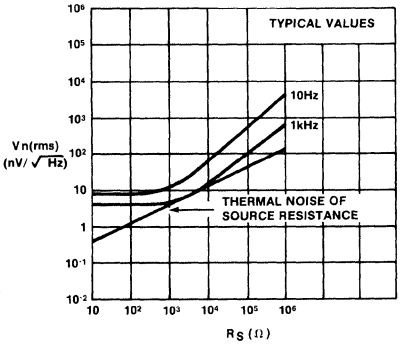


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

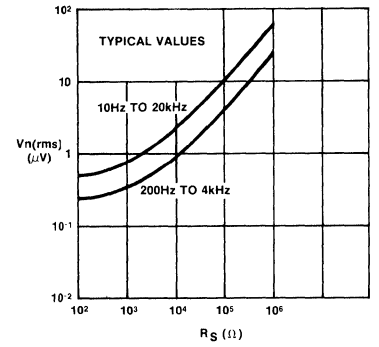
INPUT NOISE CURRENT DENSITY



TOTAL INPUT NOISE DENSITY

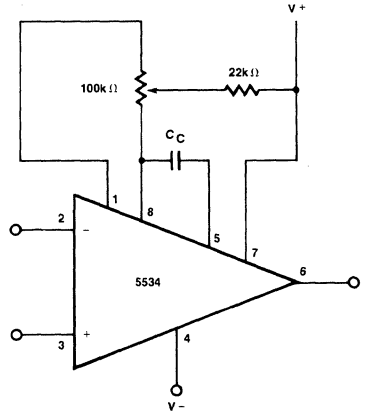


BROADBAND INPUT NOISE VOLTAGE

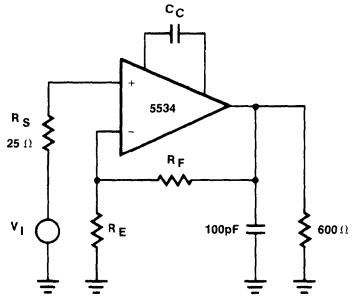


TEST LOAD CIRCUITS

FREQUENCY COMPENSATION AND OFFSET VOLTAGE ADJUSTMENT CIRCUIT



CLOSED LOOP FREQUENCY RESPONSE



μA709/709A/709C/SA709C-F,N,N-14,T

DESCRIPTION

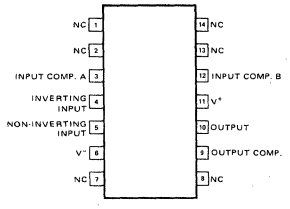
The 709 is a high performance monolithic operational amplifier with differential inputs. High open loop gain, high input impedance, wide input common mode and output voltage ranges plus low temperature drift enable it to be used in many applications formerly satisfied only by discrete amplifiers.

FEATURES

- **Open loop voltage gain = 45,000**
- **Output voltage swing = ±14V**
- **Input common mode range = ±10V**
- **Differential input resistance =**
  SA709C 250K
  μA709C 250K
  μA709 400K
  μA709A 700K
- **μA709, 709A Mil Std 883 A,B,C available**

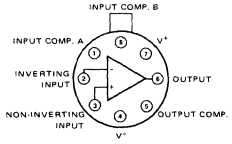
PIN CONFIGURATIONS

F,N-14 PACKAGE



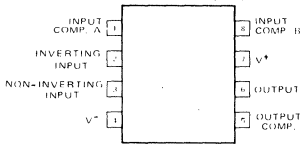
ORDER PART NO.
μA709AF, μA709AN-14, μA709F, μA709N-14, SA709CF, SA709CN-14, μA709CN-14

T PACKAGE



ORDER PART NO.
μA709AT, μA709T, μA709CT

N PACKAGE



ORDER PART NO.
μA709AN, μA709N, μA709CN, SA709CN

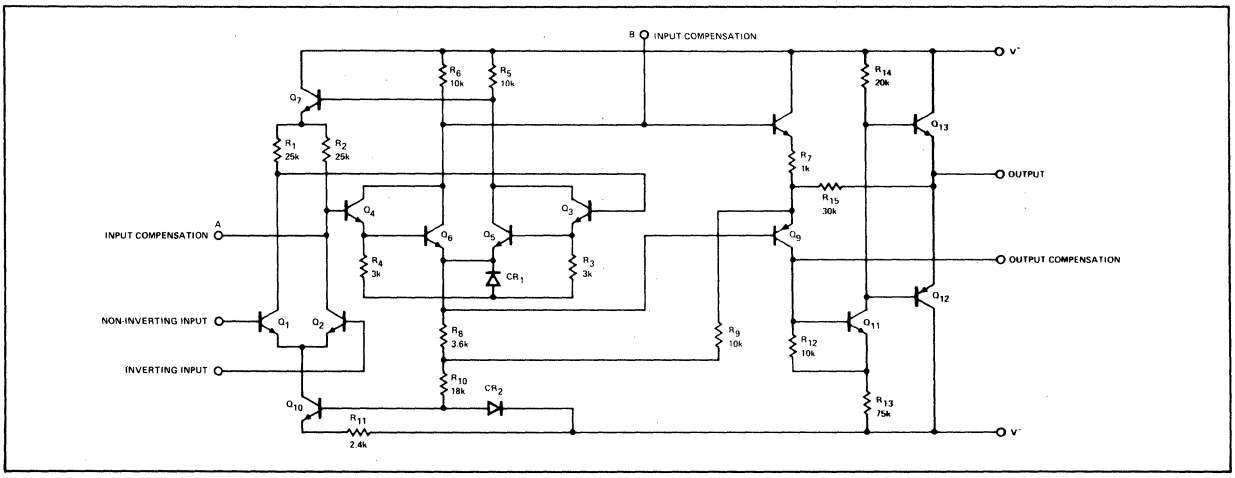
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	±18	V
Internal power dissipation*		
μA709C	250	mW
μA709	300	mW
Differential input voltage	±5.0	V
Input voltage	±10	V
Output short-circuit duration ($T_A = 25°C$)	5	sec
Operating temperature range		
μA709C	0 to +75	°C
μA709	-55 to +125	°C
SA709	-40 to +85	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	300	°C

*NOTE

Rating applied for case temperatures to +125°C. Derate linearly at 5.6mW/°C for ambient temperatures above +95°C.

EQUIVALENT SCHEMATIC



μA709/709A/709C/SA709C-F,N,N-14,T

DC ELECTRICAL CHARACTERISTICS

$\pm 9V \leq V_S \leq \pm 15V$ (μA709, μA709A) $V_S = \pm 15V$ (μA709C, SA709C)
$T_A = 25°C$ unless otherwise specified.*

PARAMETER		TEST CONDITIONS	μA709			μA709C			μA709A			SA709C			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \leq 10k\Omega$		1.0	5.0		2.0	7.5		0.6	2.0		2.0	7.5	mV
V_{OS}	Offset voltage	Over temp			6.0			10			3.0			10	mV
V_{OS}	Drift	$R_S = 50$ over temp		3.0						1.8	10				μV/°C
		$R_S \leq 10k + 25°C \leq T_A \leq T_{max}$		6.0						2.0	15				μV/°C
		$R_S \leq 10k$ $T_{min} \leq T_A \leq +25°C$		6.0						4.8	25				
I_{OS}	Offset current			50	200		100	500		10	50		100	500	nA
		T_{max}		20	200			750		3.5	50			750	nA
		T_{min}		100	500			750		40	250			750	nA
I_{BIAS}	Input current			200	500		300	1500		100	200		300	1500	nA
		T_{min}		500	1500			2000		300	600			2000	nA
		T_{max}						2000						2000	nA
V_{CM}	Common mode voltage range	$V_S = \pm 15V$				±8.0	±10					±8.0	±10		V
		$V_S = \pm 15V$ over temp	±8.0	±10					±8.0	±10					V
CMRR	Common mode rejection ratio	$R_S \leq 10k\Omega$				65	90					65	90		dB
		$R_X \leq 10k\Omega$ over temp		70	90				80	110					dB
R_{IN}	Input resistance		150	400		50	250		350	700		50	250		kΩ
		Over temp	40	100		35			85	170		35			kΩ
A_{VOL}	Large signal voltage gain	$R_L \geq 2k\Omega$, $V_{out} = \pm 10V$				15	45					15	45		V/mV
		$R_L \geq 2k\Omega$, $V_{out} = \pm 10V$, over temp	25	45	70	12			25		70	12			V/mV
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$, $V_S = \pm 15V$	±10	±13		±10	±13		±10	±13		±10	±13		V
		$R_L = 10k\Omega$, $V_S = \pm 15V$	±12	±14		±12	±14		±12	±14		±12	±14		V
		$R_L = 2k\Omega$, $V_{CC} = \pm 15V$ over temp	±10	±13					±10	±13					V
		$R_L = 10k\Omega$, $V_{CC} = \pm 15V$ over temp	±12	±14					±12	±14					V
P_D	Power consumption	$V_S = \pm 15V$		80	165		80	200		75	108		80	200	mW
		T_A = high								63	90				mW
		T_A = low								81	135				mW
P_{SRR}	Supply voltage rejection ratio	$R_S \leq 10k\Omega$					25	200					25	200	μV/V
		$R_S \leq 10k\Omega$, over temp	25	150						40	100				
R_{OUT}	Output resistance			150			150			150			150		Ω

*NOTE

Operating temperature range

μA709, μA709A	$-55°C \leq T_A \leq 125°C$
SA709C	$-40°C \leq T_A \leq 85°C$
μA709C	$0°C \leq T_A \leq 70°C$

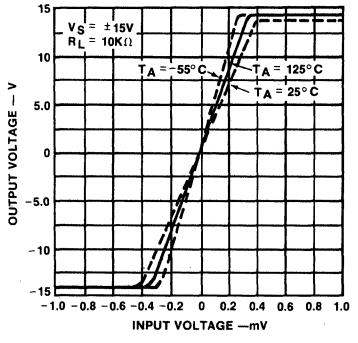
AC ELECTRICAL CHARACTERISTICS

$\pm 9V \leq V_S \leq \pm 15V$ (μA709, μA709A) $V_S = \pm 15V$ (μA709C, SA709C)
$T_A = 25°C$ unless otherwise specified.

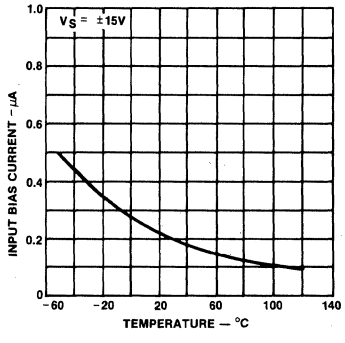
PARAMETER	TEST CONDITIONS	μA709			μA709C/SA709C			μA709A			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Transient response											
Rise time	$V_{IN} = 10mV$, $R_L = 2k\Omega$		0.3	1.0		0.3			0.3		μs
	$R_1 = 1.5k\Omega$ $C_2 = 200pF$,										
	$R_2 = 50\Omega$ $V_{IN} = 2mV$,										
	$R_L = 2k\Omega$ $C_1 = 5nF$									1.5	μs
Overshoot	$C_L \leq 100pF$		10	30		10			10	30	%

TYPICAL PERFORMANCE CHARACTERISTICS

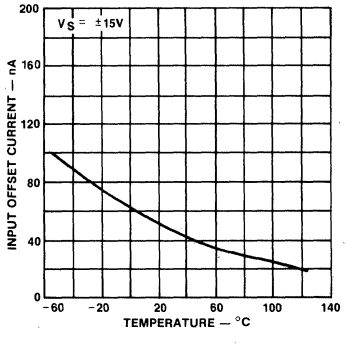
VOLTAGE TRANSFER CHARACTERISTIC (μA709 AND μA709C)



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE (μA709 AND μA709C)

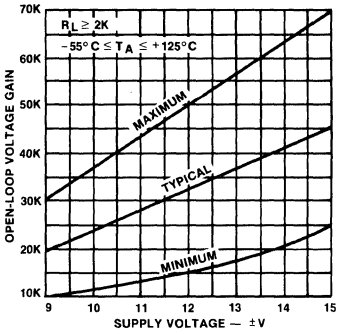


INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE (μA709 AND μA709C)

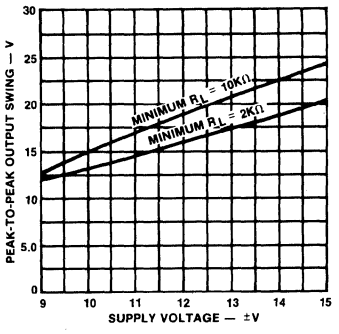


TYPICAL PERFORMANCE CHARACTERISTICS

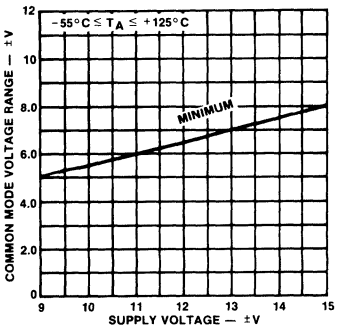
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE (μA709A)



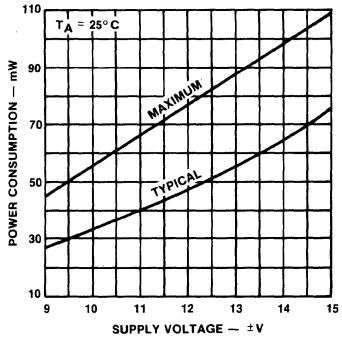
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE (μA709A)



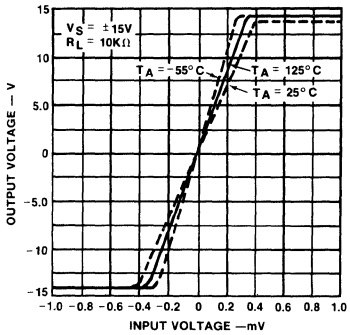
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE (μA709A)



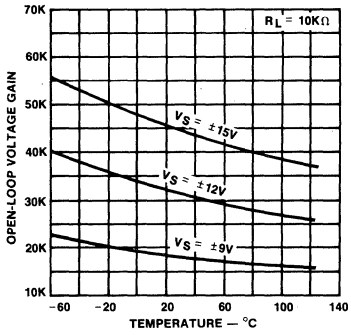
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE (μA709A)



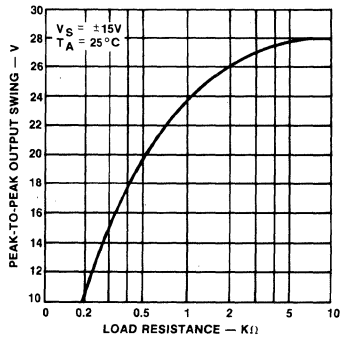
VOLTAGE TRANSFER CHARACTERISTICS (μA709A)



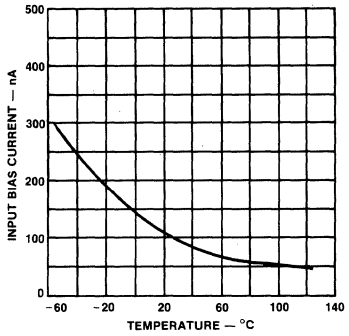
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE (μA709A)



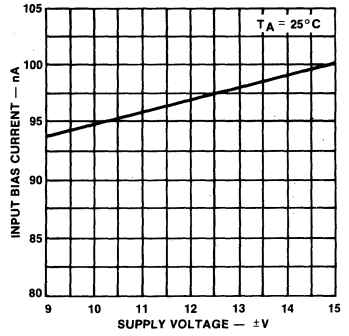
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE (μA709A)



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE (μA709A)

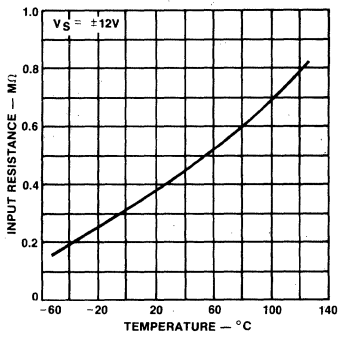


INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE (μA709A)

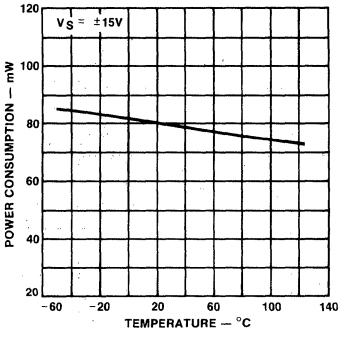


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

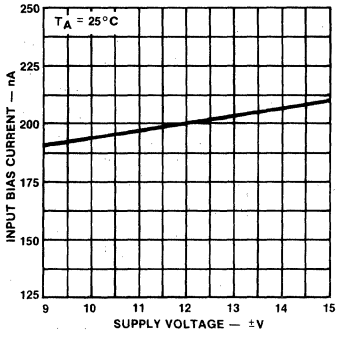
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE (μA709 AND μA709C)



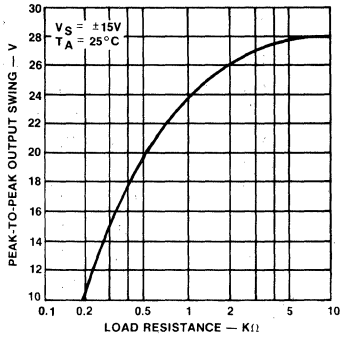
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE (μA709 AND μA709C)



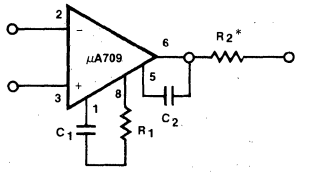
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE (μA709 AND μA709C)



OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE (μA709 AND μA709C)



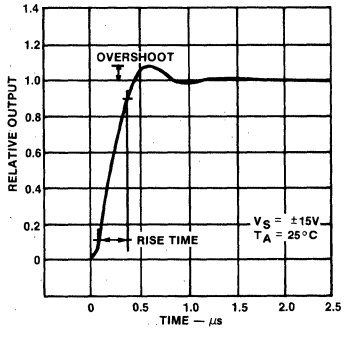
FREQUENCY COMPENSATION CIRCUIT (μA709 AND μA709C)



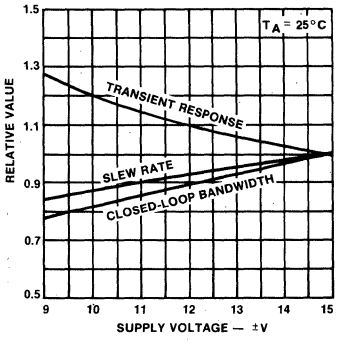
*NOTE

Use R2 = 50Ω when the amplifier is operated with capacitive loading.

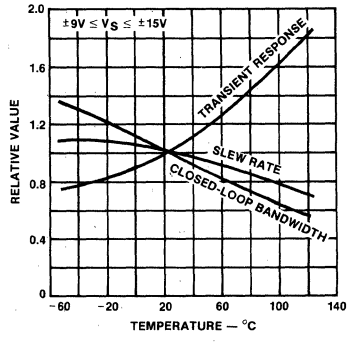
TRANSIENT RESPONSE (μA709 AND μA709C)



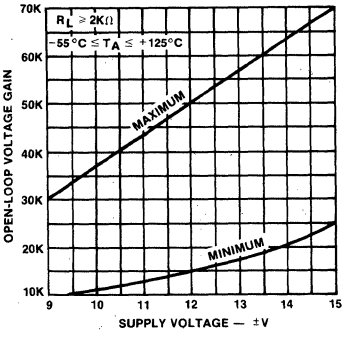
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE (μA709 AND μA709C)



FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE (μA709 AND μA709C)

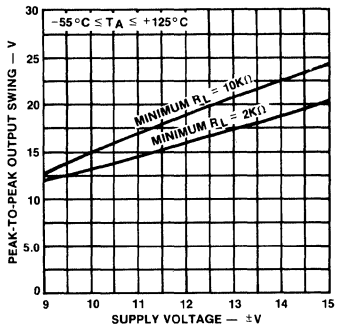


VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE (μA709)

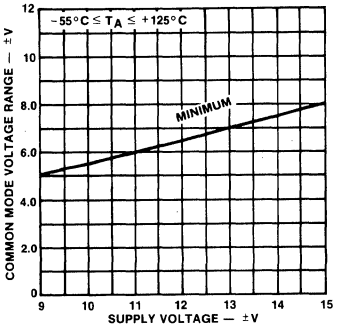


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

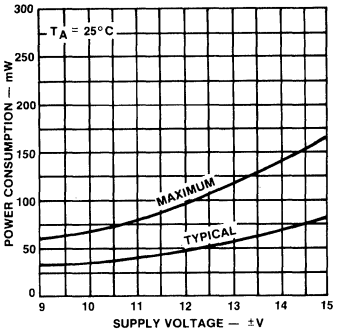
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE (μA709)



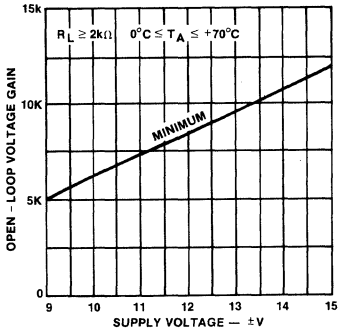
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE (μA709)



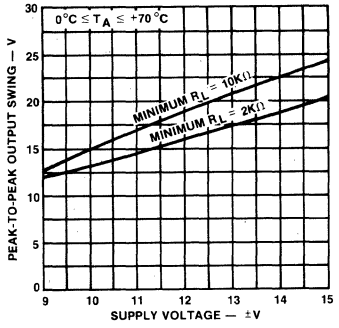
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE (μA709)



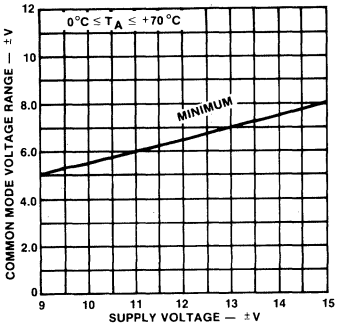
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE (μA709C)



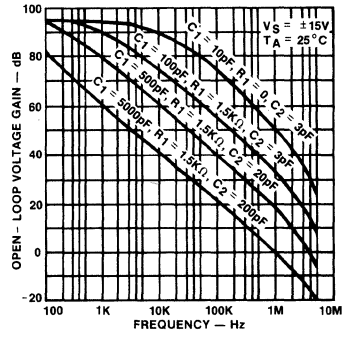
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE (μA709C)



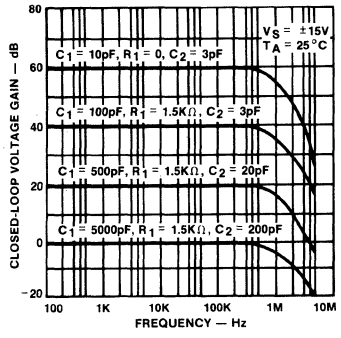
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE (μA709C)



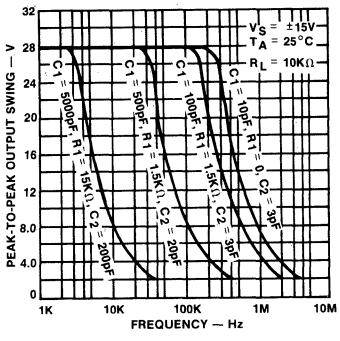
OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION (ALL TYPES)



FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS (ALL TYPES)

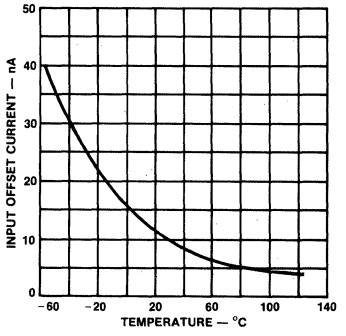


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS (ALL TYPES)

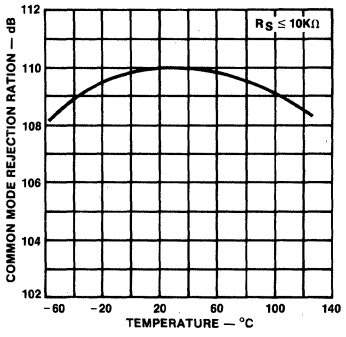


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

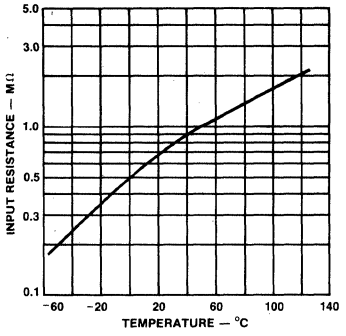
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE (μA709A)



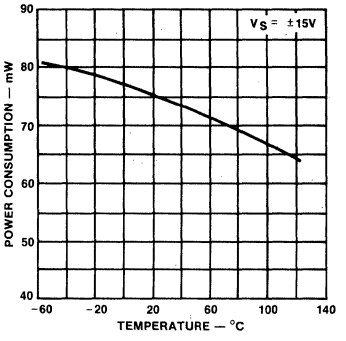
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE (μA709A)



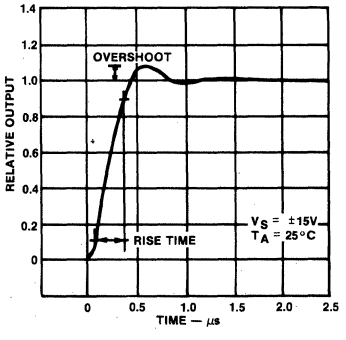
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE (μA709A)



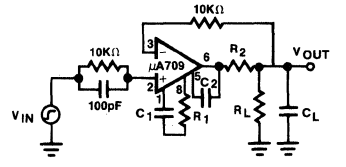
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE (μA709A)



TRANSIENT RESPONSE (μA709A)

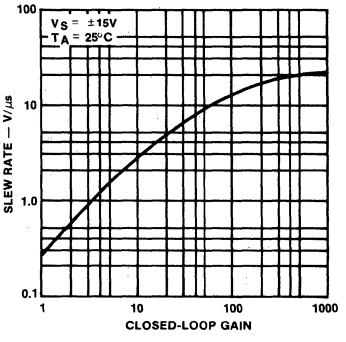


TRANSIENT RESPONSE TEST CIRCUIT (μA709A)

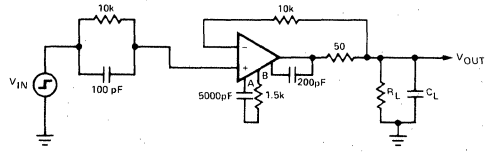


Pin numbers on this and all succeeding circuits apply to metal can or mini DIP package.

SLEW RATE AS A FUNCTION OF CLOSED-LOOP GAIN USING RECOMMENDED COMPENSATION NETWORKS (μA709A)



TEST CIRCUIT



μA740C-T

DESCRIPTION

The μA740C is a special purpose high performance operational amplifier utilizing a FET input stage for high input impedance and low input current.

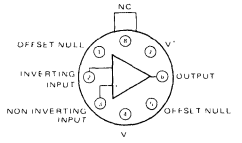
The device features internal compensation, standard pinout, wide differential and common mode input voltage range, high slew rate and high output drive capability.

FEATURES

- **0.1nA input bias current**
- **Input and output protection**
- **Offset null capability**
- **Internally compensated**
- **6V/μs slew rate**
- **Standard pinout**
- **No latch-up**

PIN CONFIGURATION

T PACKAGE



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	±22	V
Differential input voltage range	±30	V
Common mode input voltage range	$\pm V_S$	
Power dissipation[1]	500	mW
Operating temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (solder, 60sec)	300	°C
Output short circuit duration[2]	indefinite	

NOTES

1. Rating applies to case temperature to +25°C. Derate linearly at 6.5mW/°C for ambient temperatures above 75°C.
2. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

DC ELECTRICAL CHARACTERISTICS

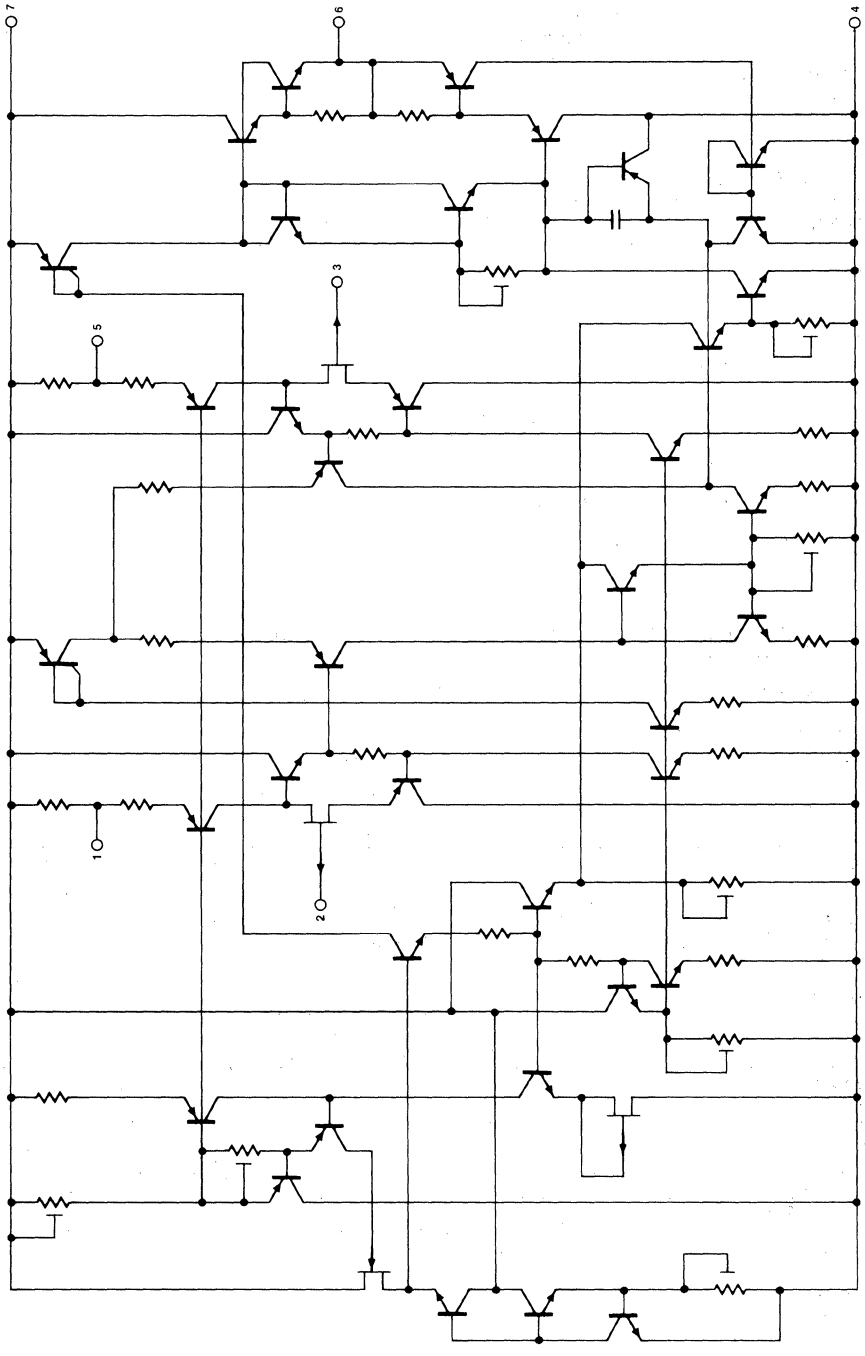
$T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	μA740C			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \leq 100k\Omega$ $R_S \leq 100k\Omega$, over temp.		30 30	110	mV mV
I_{OS}	Offset current	 Over temp.		60 60	300	pA pA
I_{BIAS}	Input current[1]	 Over temp.		0.1 1.1	2.0 10	nA nA
V_{CM} CMRR	Common mode voltage range[2] Common mode rejection ratio	Over temp. Over temp.	±10 55	±12 80		V dB
R_{IN}	Input resistance			1,000,000		MΩ
V_{OUT}	Output voltage swing	Over temp., $R_L \geq 2k\Omega$ Over temp., $R_L \geq 10k\Omega$	±10 ±12	±13 ±14		V V
I_{CC} Pd	Supply current Power consumption			4.2 126	8.0 240	mA mW
P_{SRR}	Supply voltage rejection ratio	$R_S \leq 10k\Omega$, over temp.		70	500	μV/V
	Output resistance			75		Ω
A_{VOL}	Large signal voltage gain	$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$, over temp.	20	1000 500		V/mV V/mV

NOTES

1. Typically doubles for every 10°C increase in temperature.
2. For supply voltages less than ±15V, absolute maximum input voltage is equal to the supply voltage.

EQUIVALENT SCHEMATIC



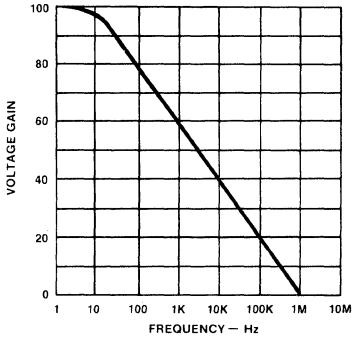
AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

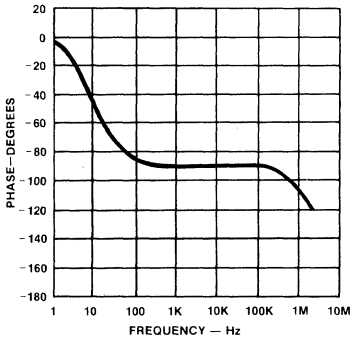
PARAMETER	TEST CONDITIONS	μA740C			UNIT
		Min	Typ	Max	
Slew rate			6.0		V/μs
Unity gain bandwidth			1.0		MHz
Transient response (voltage follower circuit)	$T_A = 25°C$, $V_{IN} = 100mV$ $C_L \leq 100pf$, $R_L = 2k\Omega$				
Rise time			300		ns
Overshoot			10		%

TYPICAL PERFORMANCE CHARACTERISTICS

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

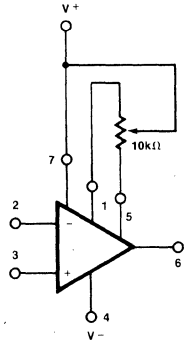


OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY

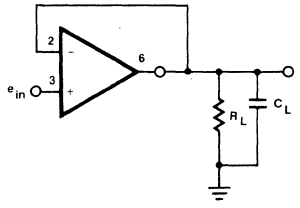


TEST CIRCUITS

OFFSET NULL CIRCUIT



VOLTAGE FOLLOWER CIRCUIT



μA747/747C/SA747C-F,K,N

DESCRIPTION

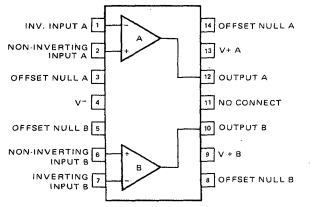
The 747 is a pair of high performance monolithic operational amplifiers constructed on a single silicon chip. High common mode voltage range and absence of "latch-up" make the 747 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. The 747 is short-circuit protected and requires no external components for frequency compensation. The internal 6dB/octave roll-off insures stability in closed loop applications. For single amplifier performance, see μA741 data sheet.

FEATURES

- **No frequency compensation required**
- **Short-circuit protection**
- **Offset voltage null capability**
- **Large common-mode and differential voltage ranges**
- **Low power consumption**
- **No latch-up**
- **μA747, SA747C Mil std 883A,B,C available**

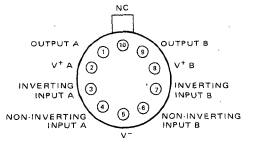
PIN CONFIGURATIONS

F/N PACKAGE



ORDER PART NO.
μA747CN, μA747CF, μA747N, μA747F, SA747CN, SA747CF

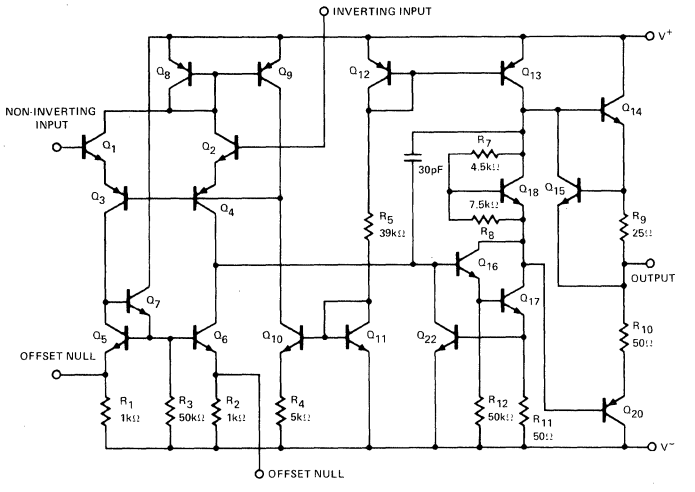
K PACKAGE



ORDER PART NO.
μA747CK, μA747K

EQUIVALENT SCHEMATIC

EQUIVALENT CIRCUIT (EACH SIDE)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
μA747	±22	V
μA747C	±18	V
SA747C	±18	V
Internal power dissipation		
Metal can	500	mW
DIP	670	mW
Differential input voltage	±30	V
Input voltage	±15	V
Voltage between offset null and V-	±0.5	V
Storage temperature range	-65 to +155	°C
Operating temperature range		
μA747	-55 to +125	°C
μA747C	0 to +70	°C
SA747C	-40 to +85	°C
Lead temperature (soldering, 60 sec)	300	°C
Output short-circuit duration	indefinite	

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

	PARAMETER	TEST CONDITIONS	μA747			μA747C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \leq 10k\Omega$		2.0	5.0		2.0	6.0	mV
V_{OS}	Offset voltage	$R_S \leq 10k\Omega$, over temp		3.0	6.0		3.0	7.5	mV
I_{OS}	Offset current			20	200		20	200	nA
I_{OS}	Offset current	$T_A = +125°C$		7.0	200				nA
I_{OS}	Offset current	$T_A = -55°C$		85	500				nA
I_{OS}	Offset current	Over temp					7.0	300	nA
I_{BIAS}	Input current			80	500		80	500	nA
I_{BIAS}	Input current	$T_A = 125°C$		30	500				nA
I_{BIAS}	Input current	$T_A = -55°C$		300	1500				nA
I_{BIAS}	Input current	Over temp					30	800	nA
V_{OUT}	Output voltage swing	$R_L \geq 2k\Omega$, over temp	±10	±13		±10	±13		V
		$R_L \geq 10k\Omega$, over temp	±12	±14		±12	±14		V
I_{CC}	Supply current			1.7	2.8		1.7	2.8	mA
		$T_A = 125°C$		1.5	2.5				mA
		$T_A = -55°C$		2.0	3.3				mA
		Over temp					2.0	3.3	mA
	Power consumption			50	85		50	85	mW
		$T_A = 125°C$		45	75				mW
		$T_A = -55°C$		60	100				mW
		Over temp					60	100	mW
	Input capacitance			1.4			1.4		pF
	Offset voltage adjustment range			±15			±15		V
	Output resistance			75			75		Ω
	Channel separation			120			120		dB
P_{SRR}	Supply voltage rejection ratio	$R_S \leq 10k\Omega$, over temp		30	150		30	150	μV/V
A_{VOL}	Large signal voltage gain (DC)	$R_L \geq 2k\Omega$ $V_{OUT} = \pm 10V$	50,000			25,000			V/V

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SA747C			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \leq 10k\Omega$		2.0	6.0	mV
V_{OS}	Offset voltage	$R_S \leq 10k\Omega$, over temp		3.0	7.5	mV
I_{OS}	Offset current			20	200	nA
I_{OS}	Offset current	Over temp			500	nA
I_{BIAS}	Input current				1500	nA
I_{BIAS}	Input current	Over temp			500	nA
V_{OUT}	Output voltage swing	$R_L \geq 2k\Omega$, over temp	±10	±13		V
		$R_L \geq 10k\Omega$, over temp	±12	±14		V
I_{CC}	Supply current			1.7	2.8	mA
		Over temp		2.0	3.3	mA
	Power consumption			50	85	mW
		Over temp		60	100	mW
	Input capacitance			1.4		pF
	Offset voltage adjustment range			±15		V
	Output resistance			75		Ω
	Channel separation			120		dB
P_{SRR}	Supply voltage rejection ratio	$R_S \leq 10k\Omega$, over temp		30	150	μV/V
	Large signal voltage gain (DC)	$R_L \geq 2k\Omega$ $V_{OUT} = \pm 10V$	25,000			V/V

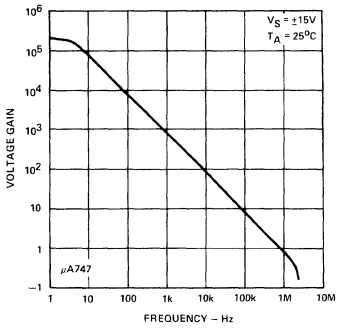
AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

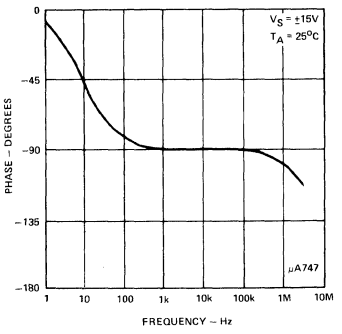
PARAMETER	TEST CONDITIONS	μA747/μA747C/SA747C			UNIT
		Min	Typ	Max	
Transient response	$V_{IN} = 20mV$, $R_1 = 2k\Omega$, $C_1 < 100pf$				
Risetime	Unity gain CL ≤ 100pf		0.3		μs
Overshoot	Unity gain CL ≤ 100pf		5.0		%
Slew rate	RL > 2kΩ		0.5		V/μs

TYPICAL PERFORMANCE CHARACTERISTICS

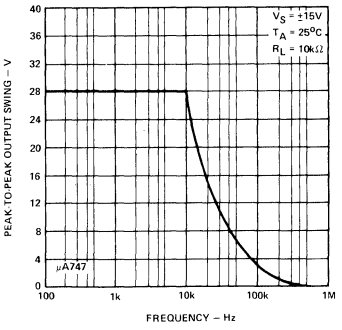
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



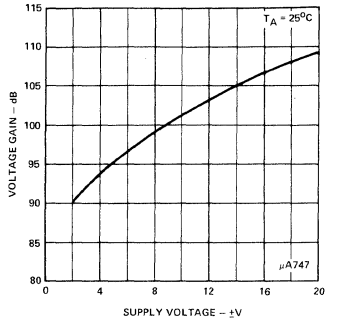
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



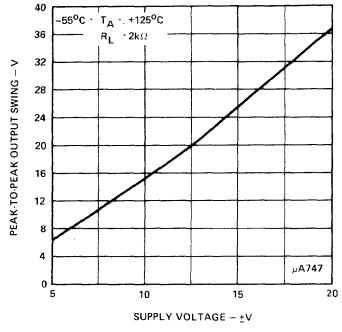
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



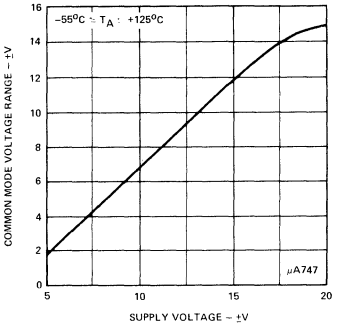
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



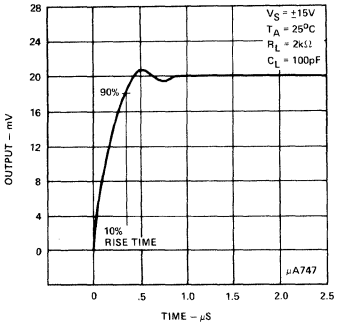
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



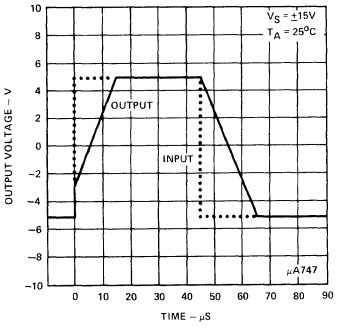
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



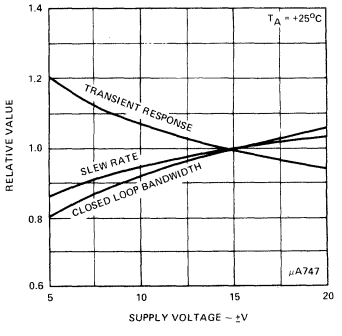
TRANSIENT RESPONSE



VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE

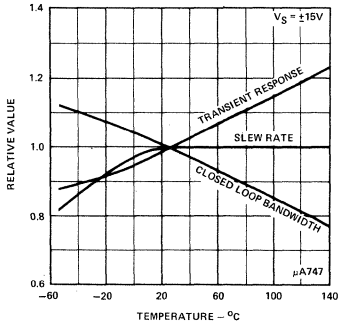


FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE

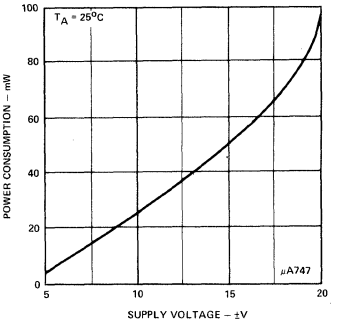


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

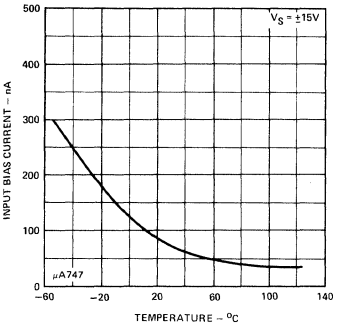
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



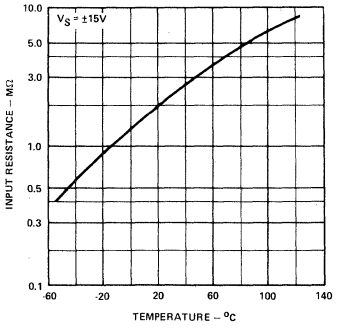
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



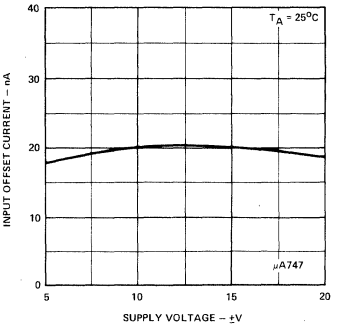
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



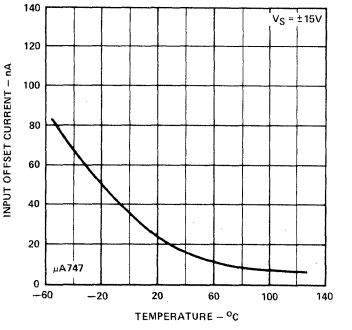
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



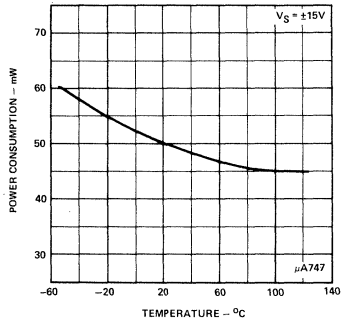
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



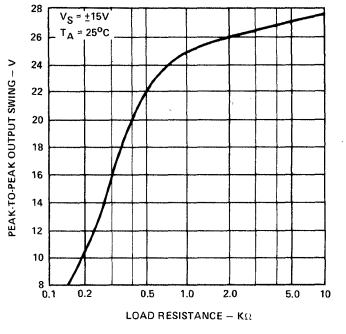
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



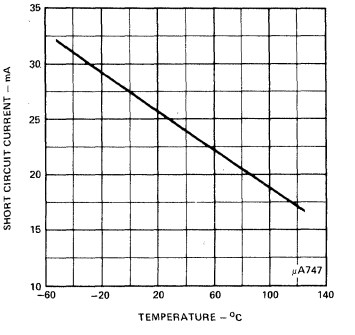
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

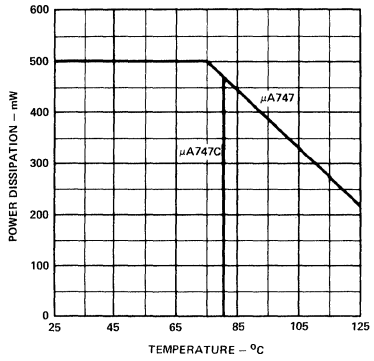


OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

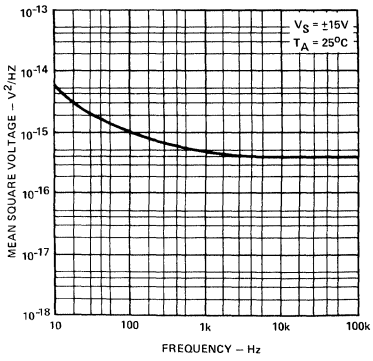


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

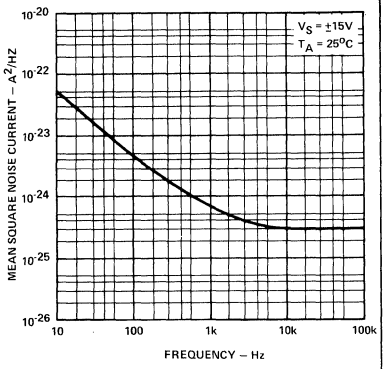
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



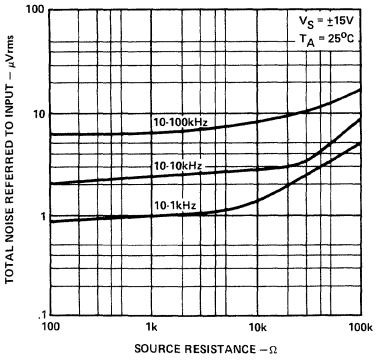
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



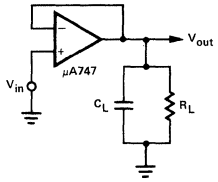
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



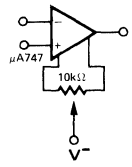
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



TRANSIENT RESPONSE TEST CIRCUIT



VOLTAGE OFFSET NULL CIRCUIT



μA748/748C/SA748C-F,N,N-14

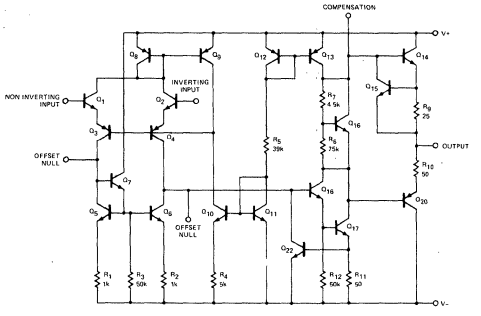
DESCRIPTION

The 748 is a High Performance Operational Amplifier featuring high gain, short circuit immunity, offset voltage null capability, simplified compensation and excellent temperature stability.

FEATURES

- **Short circuit protection**
- **Offset voltage null capability**
- **Large common-mode and differential voltage ranges**
- **Low power consumption**
- **No latch-up**
- **Mil std 883A,B,C available**

EQUIVALENT CIRCUIT

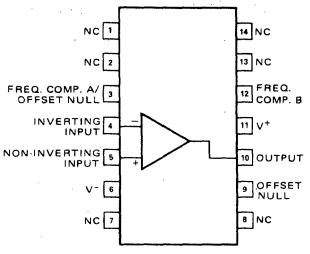


NOTE

All resistors values are typical and in ohms.

PIN CONFIGURATIONS

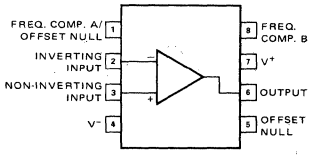
F,N-14 PACKAGE



ORDER PART NO.

μA748F, μA748N-14, μA748CF, SA748CF, μA748CN-14, SA748CN-14

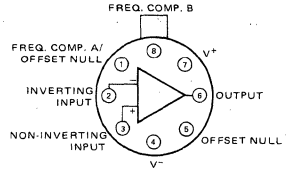
N PACKAGE



ORDER PART NO.

μA748N, μA748CN, SA748CN

T PACKAGE



ORDER PART NO.

μA748T, μA748CT

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
μA748	±22	V
μA748C }	±18	V
SA748C }		
Internal power dissipation[1]	500	mW
Differential output voltage	±30	V
Input voltage[2]	±15	V
Storage temperature range	-65 to +150	°C
Operating temperature range		
μA748	-55 to +125	°C
μA748C	0 to +70	°C
SA748C	-40 to +85	°C
Lead temperature	300	°C
Output short circuit duration[3]	indefinite	

NOTES

1. Rating applies for case temperatures to +70°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	μA748			μA748C			SA748C			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \leq 10k\Omega$, $T_A = 25°C$		1.0	5.0		2.0	6.0		2.0	6.0	mV
		Over temperature			6.0			7.5		7.5		mV
I_{OS}	Offset current			20	200		20	200		20	200	nA
I_{OS}	Offset current	$25° \leq T_A \leq T_{max}$		7.0	200		9.0	300		7.0	200	nA
I_{OS}	Offset current	$T_{min} \leq T_A \leq 25°C$		85	500		35	300		85	500	nA
I_{BIAS}	Input current			80	500		80	500		80	500	nA
I_{BIAS}	Input current	$25° \leq T_A \leq T_{max}$		30	500		40	800		30	500	nA
I_{BIAS}	Input current	$T_{min} \leq T_A \leq 25°C$		300	1500		130	800		300	1500	nA
V_{CM}	Common mode voltage range	Over temperature	±12	±13		±12	±13			±12	±13	V

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

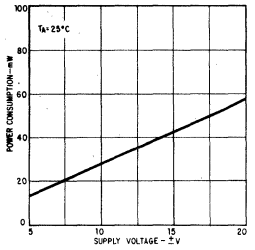
PARAMETER		TEST CONDITIONS	μA748			μA748C/SA748C			UNIT
			Min	Typ	Max	Min	Typ	Max	
C_{MRR}	Common mode rejection ratio	$R_S \leq \pm 10k\Omega$, over temperature	70	90		70	90		dB
R_{IN}	Input resistance		0.3	2.0		.30	2.0		MΩ
V_{OUT}	Output voltage swing	$R_L \geq 2k\Omega$, over temperature	±10	±13		±10	±13		V
V_{OUT}	Output voltage swing	$R_L \geq 10k\Omega$, over temperature	±12	±14		±12	±14		V
I_{CC}	Supply current			1.7	2.8		1.7	2.8	mA
I_{CC}	Supply current	$25° \leq T_A \leq T_{max}$		1.5	2.5		1.6	3.3	mA
I_{CC}	Supply current	$T_{min} \leq T_A \leq 25°C$		2.0	3.3		1.8	3.3	mA
P_d	Power consumption	$T_A = 25°C$		50	85		50	85	mW
P_d	Power consumption	$25° \leq T_A \leq T_{max}$		45	75		48	100	mW
P_d	Power consumption	$T_{min} \leq T_A \leq 25°C$		60	100		54	100	mW
P_{SRR}	Supply voltage rejection ratio	$R_S \leq 10k\Omega$, over temperature		30	150		30	150	μV/V
	Output resistance	$T_A = 25°C$		75			75		Ω
A_{VOL}	Large signal voltage gain	$R_L \geq 2k\Omega$ V_{OUT} ±10V ±15V	50	200		50	200		V/mV
A_{VOL}	Large signal voltage gain	Over temperature	25			25			V/mV
	Input capacitance			1.4			1.4		pF
	Offset voltage adjustment range			±15			±15		mV

AC ELECTRICAL CHARACTERISTICS

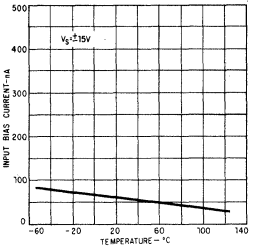
PARAMETER	TEST CONDITIONS	μA748			μA748C/SA748C			UNIT
		Min	Typ	Max	Min	Typ	Max	
Transient response (unity gain)	$V_{IN} = 20mV$, $R_L = 2k\Omega$ $C_L \leq 100pF$							
Rise time	$C_1 = 30pF$		0.3			0.3		μs
Overshoot			5.0			5.0		%
Slew rate	$R_L \geq 2k\Omega$ $C_1 = 30pF$		0.5			0.5		V/μs

TYPICAL CHARACTERISTIC CURVES

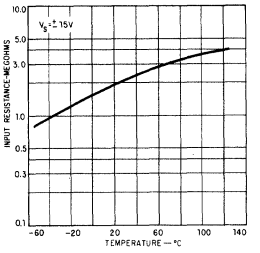
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



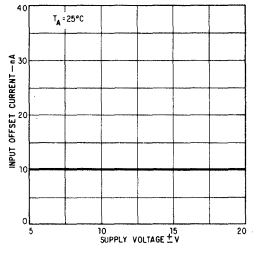
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



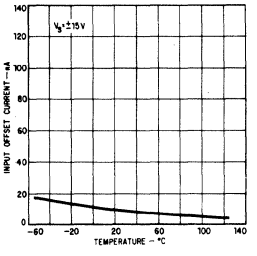
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



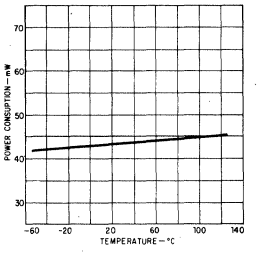
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



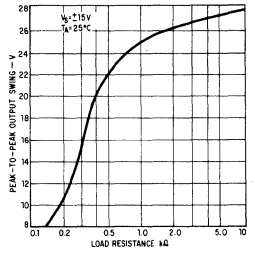
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



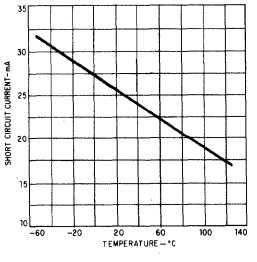
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



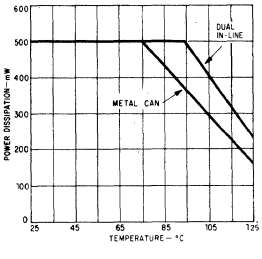
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



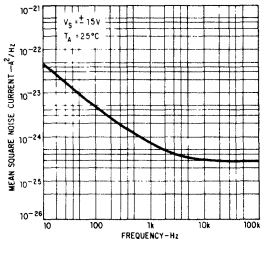
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



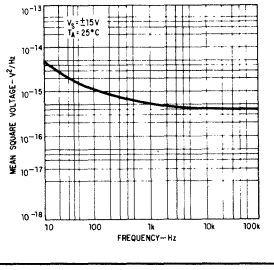
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



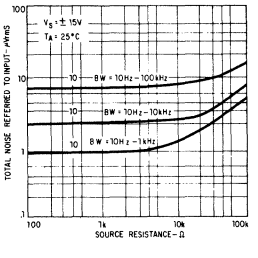
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY

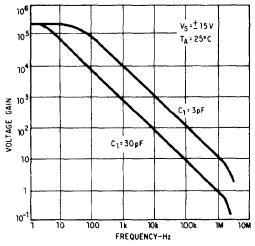


BROADBAND NOISE AS A FUNCTION OF SOURCE RESISTANCE

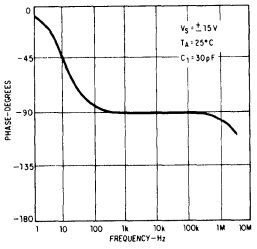


TYPICAL CHARACTERISTIC CURVES (Cont'd)

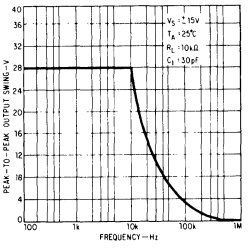
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



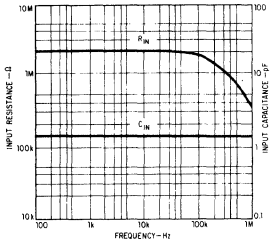
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



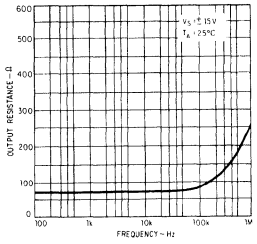
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



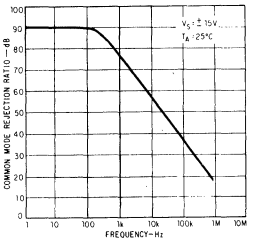
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



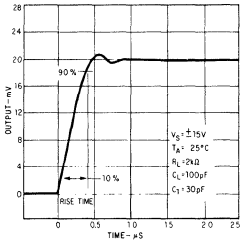
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



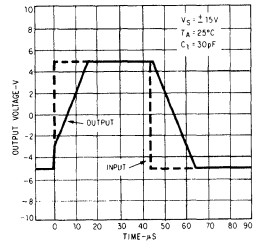
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



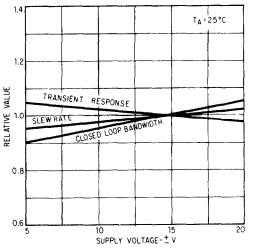
TRANSIENT RESPONSE



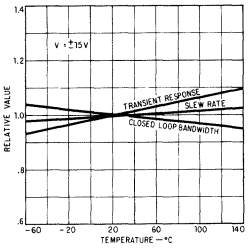
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



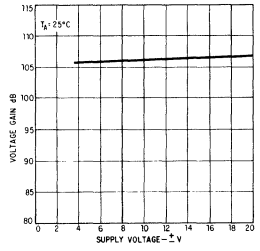
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



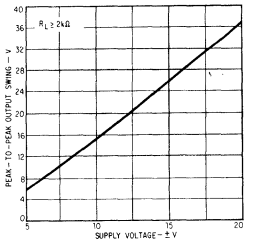
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



SECTION 2
VIDEO AMPLIFIERS

DESCRIPTION

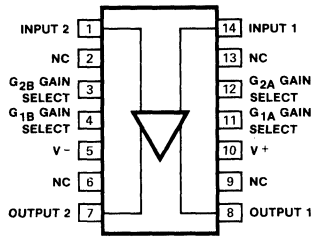
The SE/NE592 is a monolithic, two stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display and video recorder systems. The 592 is a pin-for-pin replacement for the μA733.

FEATURES

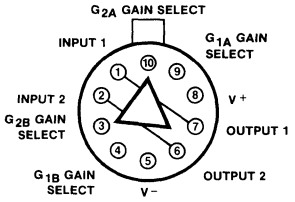
- **120MHz bandwidth**
- **Adjustable gains from 0 to 400**
- **Adjustable pass band**
- **No frequency compensation required**

PIN CONFIGURATION

F,N PACKAGE

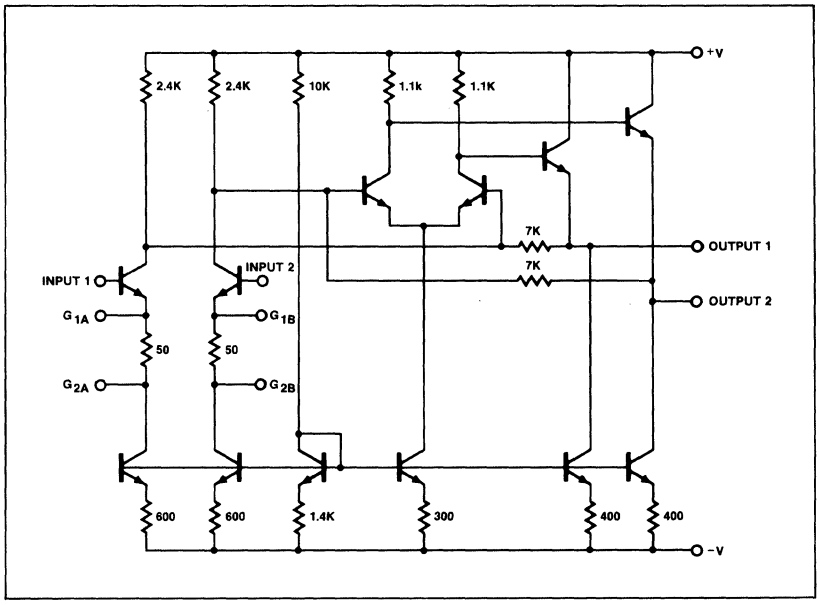


K PACKAGE



NOTE
Pin 5 connected to case.

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$ unless otherwise specified.

PARAMETER	RATING	UNIT
Supply voltage	±8	V
Differential input voltage	±5	V
Common mode		
Input voltage	±6	V
Output current	10	mA
Operating temperature range		
SE592K	-55 to +125	°C
NE592K	0 to +70	°C
Storage temperature range	-65 to +150	°C
Power dissipation	500	mW

NE/SE592-F,K,N

DC ELECTRICAL CHARACTERISTICS

T_A = +25°C, V_S = ±6V, V_{CM} = 0 unless otherwise specified
Recommend operating supply voltages V_S = ±6.0V

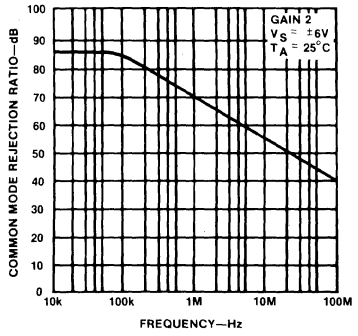
PARAMETER	TEST CONDITIONS	NE592			SE592			UNITS
		Min	Typ	Max	Min	Typ	Max	
Differential voltage gain								
Gain 1[1]	R_L = 2kΩ, V_{OUT} = 3V p-p	250	400	600	300	400	500	V/V
Gain 2[2]		80	100	120	90	100	110	V/V
Bandwidth								
Gain 1[1]			40			40		MHz
Gain 2[2]			90			90		MHz
Rise time								
Gain 1[1]	V_{OUT} = 1V p-p		10.5			10.5		ns
Gain 2[2]			4.5	12		4.5	10	ns
Propagation delay								
Gain 1[1]	V_{OUT} = 1V p-p		7.5			7.5		ns
Gain 2[2]			6.0	10		6.0	10	ns
Input resistance								
Gain 1[1]			4.0			4.0		kΩ
Gain 2[2]		10	30		20	30		kΩ
Input capacitance[2]	Gain 2		2.0			2.0		pF
Input offset current			0.4	5.0		0.4	3.0	μA
Input bias current			9.0	30		9.0	20	μA
Input noise voltage	BW 1kHz to 10kHz		12			12		μVrms
Input voltage range				±1.0			±1.0	V
Common mode rejection ratio								
Gain 2	VCM ±1V,F < 100kHz	60	86		60	86		dB
Gain 2	VCM ±1V,F = 5MHz		60			60		dB
Supply voltage rejection ratio								
Gain 2	ΔVS = ±0.5V	50	70		50	70		dB
Output offset voltage								
Gain 3[3]	R_L = ∞		0.35	0.75		0.35	0.75	V
Output common mode voltage	R_L = ∞	2.4	2.9	3.4	2.4	2.9	3.4	V
Ouptut voltage swing	R_L = 2K	3.0	4.0		3.0	4.0		
Ouput resistance			20			20		Ω
Power supply current	R_L = ∞		18	24		18	24	mA

NOTES

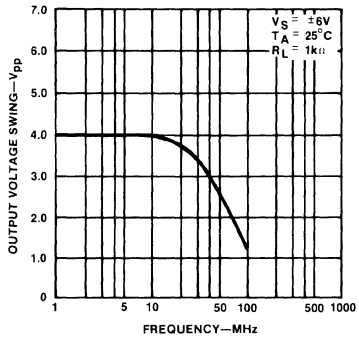
1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

TYPICAL PERFORMANCE CHARACTERISTICS

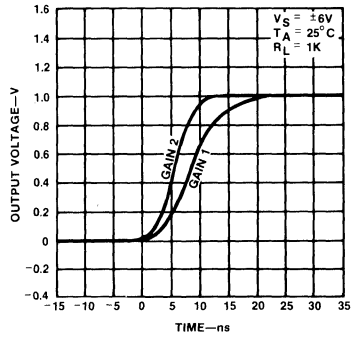
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



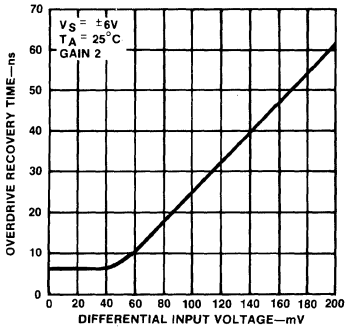
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



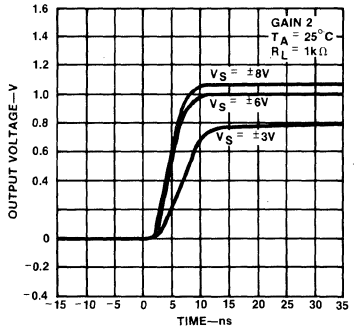
PULSE RESPONSE



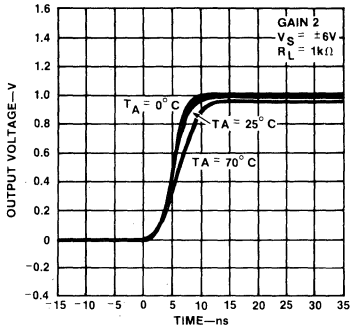
DIFFERENTIAL OVERDRIVE RECOVERY TIME



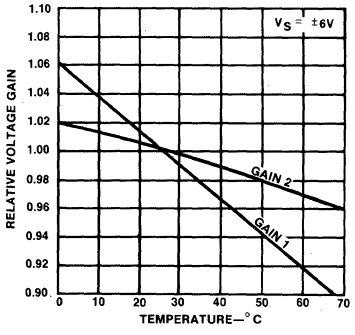
PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE



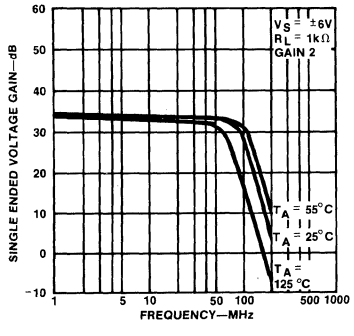
PULSE RESPONSE AS A FUNCTION OF TEMPERATURE



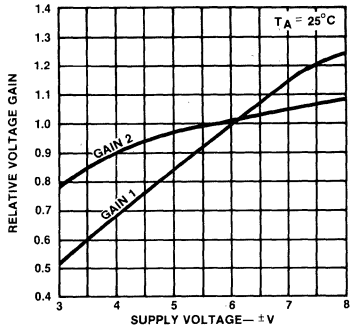
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



GAIN vs FREQUENCY AS A FUNCTION OF TEMPERATURE

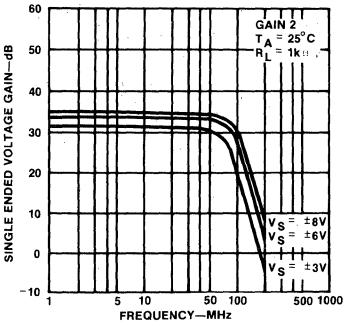


VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

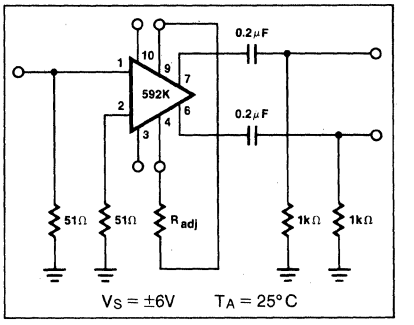


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

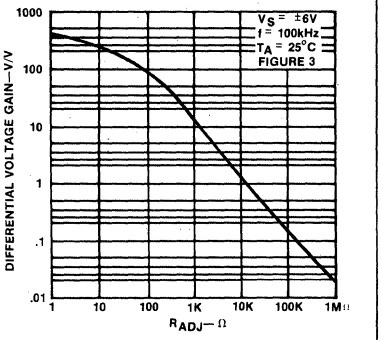
GAIN vs FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



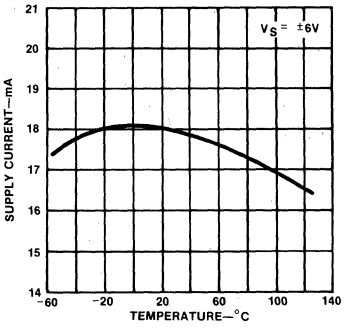
VOLTAGE GAIN ADJUST CIRCUIT



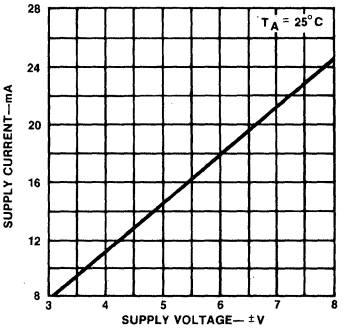
VOLTAGE GAIN AS A FUNCTION OF RADJ (FIGURE 3)



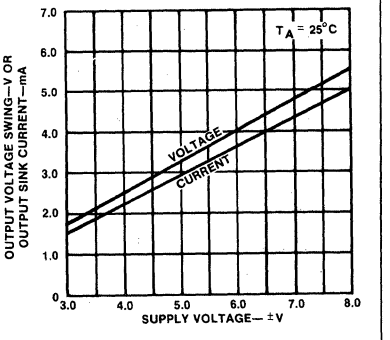
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



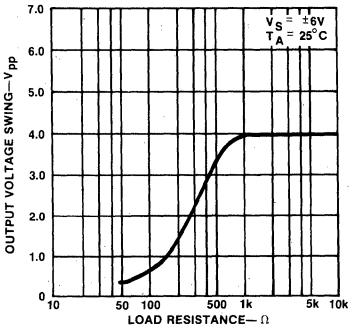
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



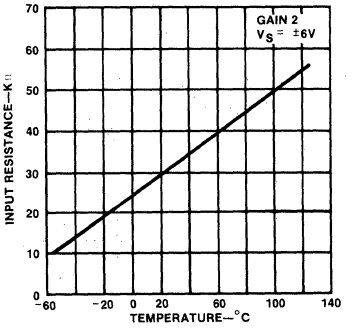
OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE



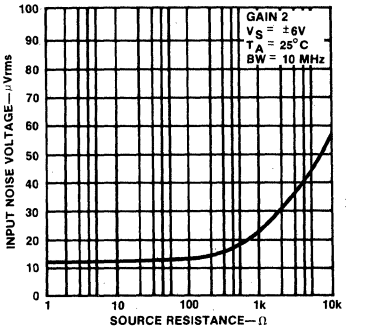
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE

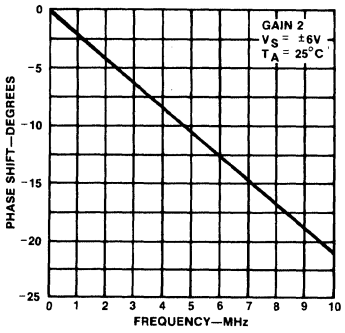


INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE

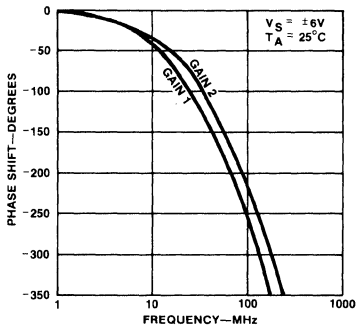


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

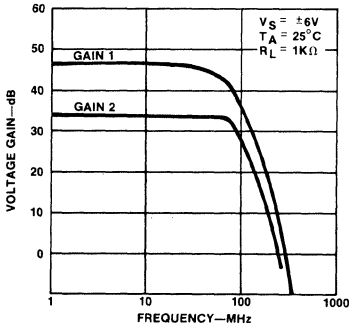
PHASE SHIFT AS A FUNCTION OF FREQUENCY



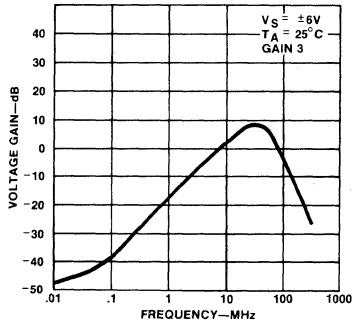
PHASE SHIFT AS A FUNCTION OF FREQUENCY



VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

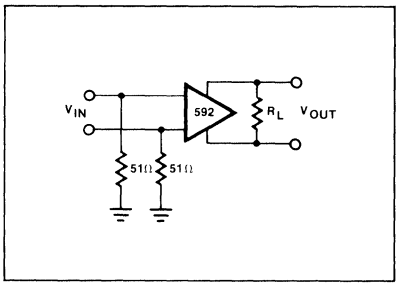


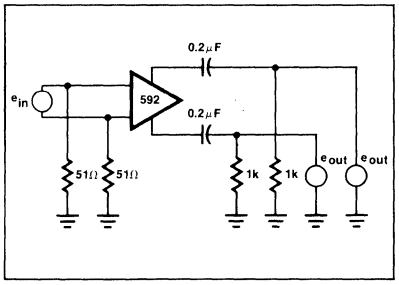
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY (ALL GAIN SELECT PINS OPEN)



TEST CIRCUITS

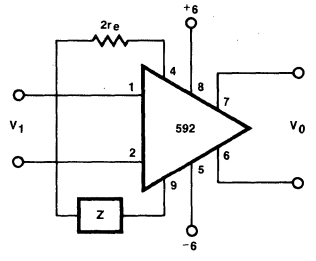
T_A = 25°C unless otherwise specified





TYPICAL APPLICATIONS

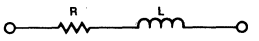
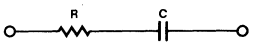
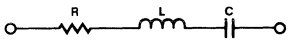
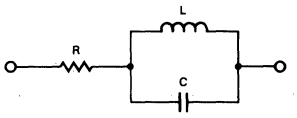
FILTER NETWORKS



$$\frac{V_0(s)}{V_1(s)} \cong \frac{1.4 \times 10^4}{Z(s) + 2r_e}$$

$$\cong \frac{1.4 \times 10^4}{Z(s) + 32}$$

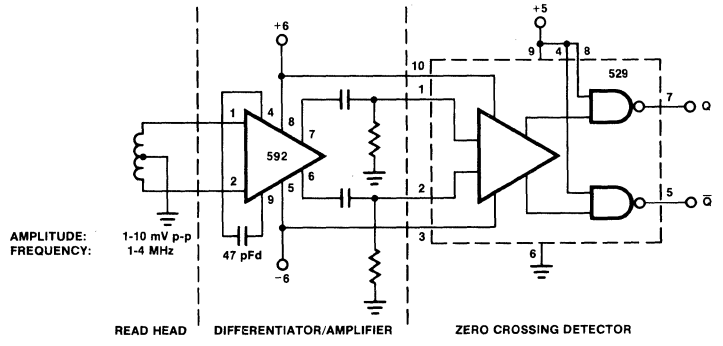
BASIC CONFIGURATION

Z NETWORK	FILTER TYPE	V_0 (s) TRANSFER V_1 (s) FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/L\, s + 1/LC}\right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

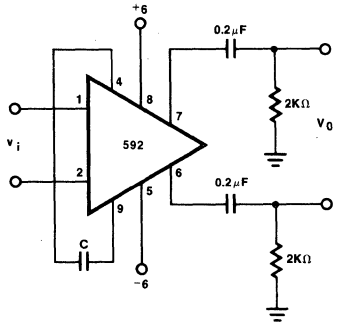
NOTE

In the networks above, the R value used is assumed to include $2r_e$, or approximately 32Ω.

DISC/TAPE PHASE MODULATED READBACK SYSTEMS



DIFFERENTIATION WITH HIGH COMMON MODE NOISE REJECTION



FOR FREQUENCY $F_1 << 1/2\,\pi\,(32)\,C$

$V_0 \cong 1.4 \times 10^4 C \frac{dV_i}{dT}$

DESCRIPTION

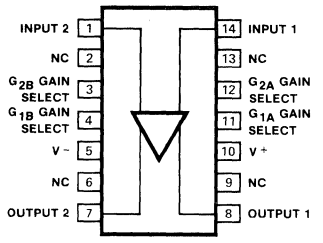
The 733 is a monolithic differential input, differential output, wideband video amplifier. It offers fixed gains of 10,100 or 400 without external components, and adjustable gains from 10 to 400 by the use of an external resistor. No external frequency compensation components are required for any gain option. Gain stability, wide bandwidth and low phase distortion are obtained through use of the classic series-shunt feedback from the emitter follower outputs to the inputs of the second stage. The emitter follower outputs provide low output impedance, and enable the device to drive capacitive loads. The 733 is intended for use as a high performance video and pulse amplifier in communications, magnetic memories, display and video recorder systems.

FEATURES

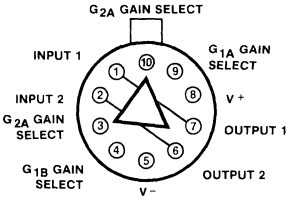
- **120MHz bandwidth**
- **250kΩ input resistance**
- **Selectable gains of 10,100 and 400**
- **No frequency compensation required**
- **Mil std 883A,B,C available**

PIN CONFIGURATION

F,N PACKAGE

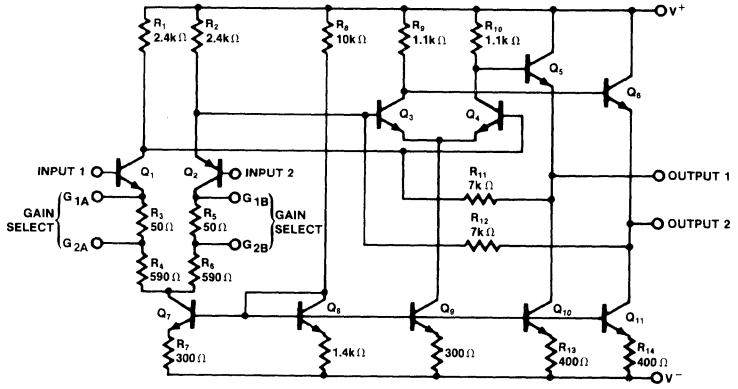


K PACKAGE



NOTE
Pin 5 connected to case.

CIRCUIT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Differential input Voltage	±5	V
Common mode input Voltage	±6	V
V_{CC}	±8	V
Ouput current	10	mA
Junction temperature	+150	°C
Storage temperature range	-65 to +150	°C
Operation temperature range		
μA733C	0 to +75	°C
μA733	-55 to +125	°C
P_D Power dissipation		
K package	500	mW
N, F package	670	mW

DC ELECTRICAL CHARACTERISTICS

T_A = +25°C, V_S = ±V, VCM = 0 unless otherwise specified.
Recommended operating supply voltages V_S = ±6.0V.

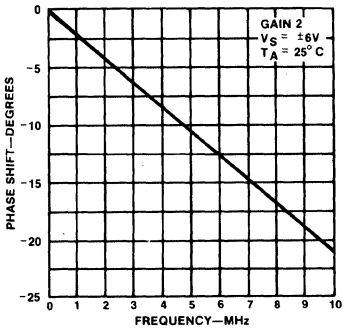
PARAMETER	TEST CONDITIONS	μA733C			μA733			UNITS
		Min	Typ	Max	Min	Typ	Max	
Differential voltage gain								
Gain 1[1]		250	400	600	300	400	500	V/V
Gain 2[2]	R_l = 2kΩ, V_{OUT} = 3Vp-p	80	100	120	90	100	110	V/V
Gain 3[3]		8.0	10	12	9.0	10	11	V/V
Bandwidth								
Gain 1[1]			40			40		MHz
Gain 2[2]			90			90		MHz
Gain 3[3]			120			120		MHz
Rise time								
Gain 1[1]			10.5			10.5		ns
Gain 2[2]	V_{OUT} = 1Vp-p		4.5	12		4.5	10	ns
Gain 3[3]			2.5			2.5		ns
Propagation delay								
Gain 1[1]			7.5			7.5		ns
Gain 2[2]	V_{OUT} = 1Vp-p		6.0	10		6.0	10	ns
Gain 3[3]			3.6			3.6		ns
Input resistance								
Gain 1[1]			4.0			4.0		kΩ
Gain 2[2]		10	30		20	30		kΩ
Gain 3[3]			250			250		kΩ
Input capacitance[2]	Gain 2		2.0			2.0		pF
Input offset current			0.4	5.0		0.4	3.0	μA
Input bias current			9.0	30		9.0	20	μA
Input noise voltage	BW = 1kHz to 10MHz		12			12		μVrms
Input voltage range		±1.0			±1.0			V
Common mode Rejection ratio								
Gain 2	VCM = ±V,f ≤ 100kHz	60	86		60	86		dB
Gain 2	VCM = ±1V,F = 5MHz		60			60		dB
Supply voltage Rejection ratio								
Gain 2	ΔV_S = ±0.5V	50	70		50	70		dB
Output offset voltage								
Gain 1[1]	R_L = ∞		0.6	1.5		0.6	1.5	V
Gain 2 and 3[2,3]			0.35	1.5		0.35	1.0	V
Output common mode voltage	R_L= ∞	2.4	2.9	3.4	2.4	2.9	3.4	V
Output voltage swing	R_L = 2k	3.0	4.0		3.0	4.0		
Output sink current		2.5	3.6		2.5	3.6		mA
Output resistance			20			20		Ω
Power supply current	R_L ± ∞		18	24		18	24	mA

NOTES

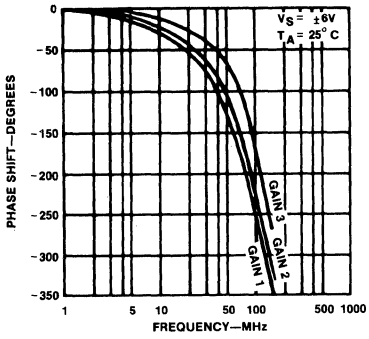
1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

TYPICAL PERFORMANCE CHARACTERISTICS

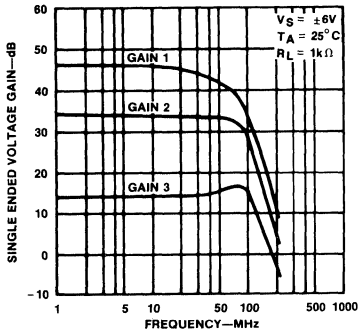
PHASE SHIFT AS A FUNCTION OF FREQUENCY



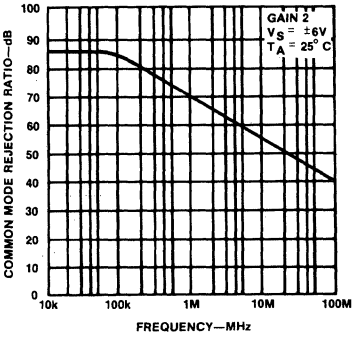
PHASE SHIFT AS A FUNCTION OF FREQUENCY



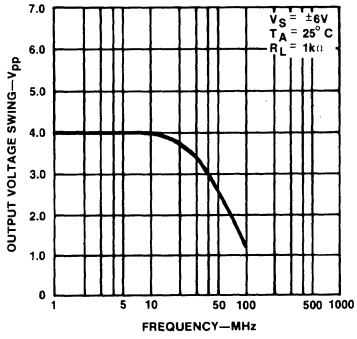
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



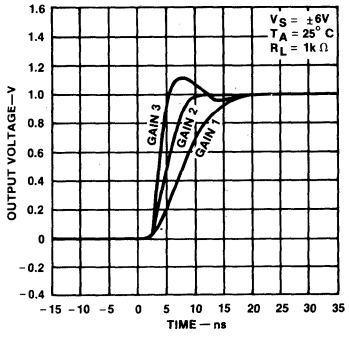
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



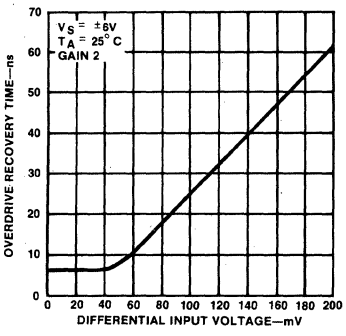
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



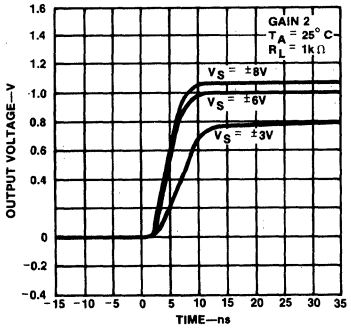
PULSE RESPONSE



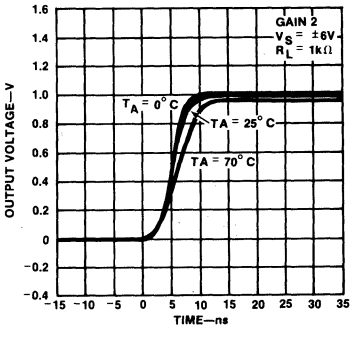
DIFFERENTIAL OVERDRIVE RECOVERY TIME



PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE

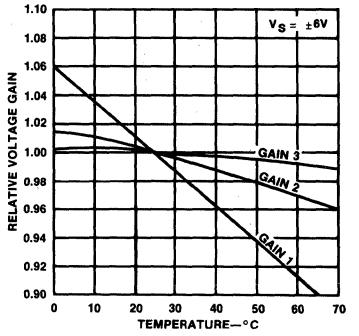


PULSE RESPONSE AS A FUNCTION OF TEMPERATURE

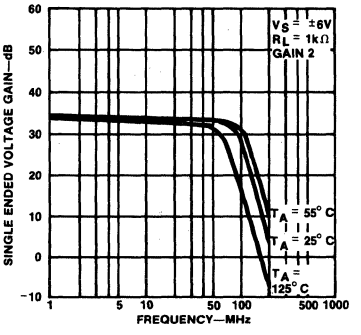


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

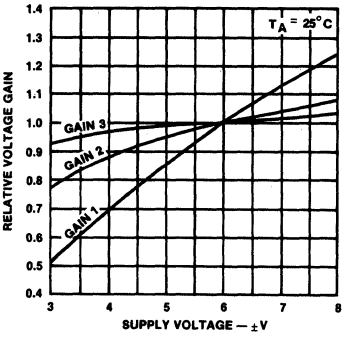
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



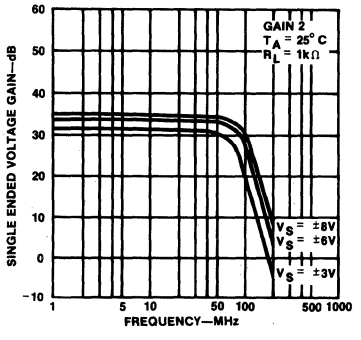
GAIN vs FREQUENCY AS A FUNCTION OF TEMPERATURE



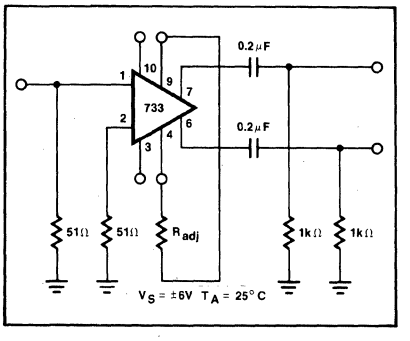
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



GAIN vs FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

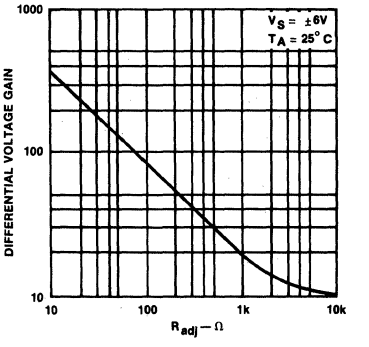


VOLTAGE GAIN ADJUST CIRCUIT

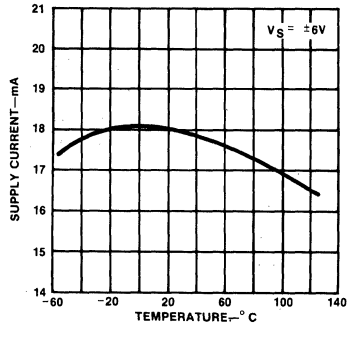


(Pin numbers apply to K Package)

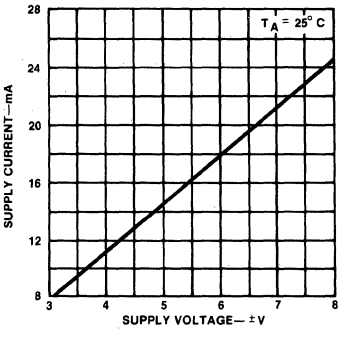
VOLTAGE GAIN AS A FUNCTION OF RADJ (FIGURE 3)



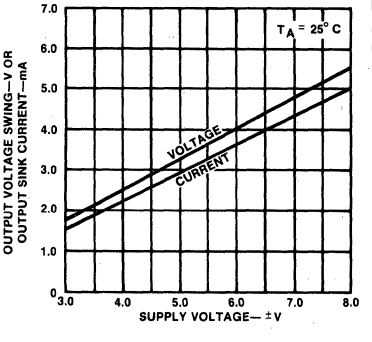
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

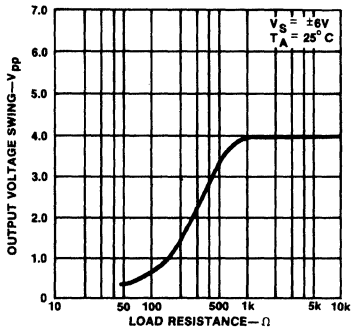


OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE

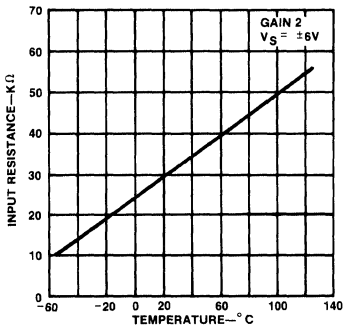


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

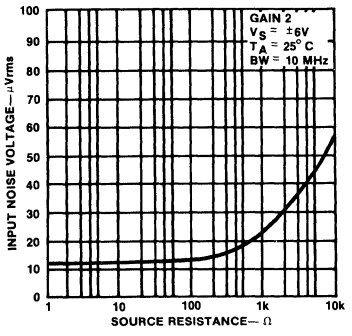
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



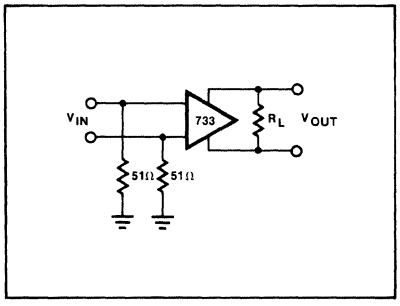
INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE

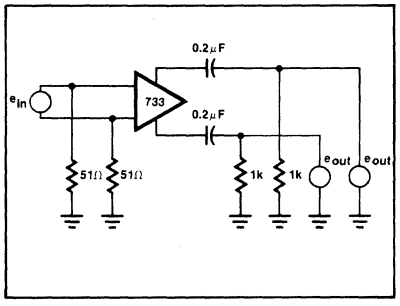


INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE



TEST CIRCUITS $T_A = 25°C$ unless otherwise specified.





SECTION 3
VOLTAGE REGULATORS

LM109/209/309-DA,DB

DESCRIPTION

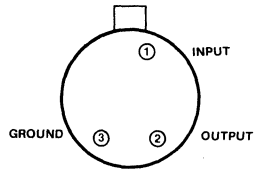
The LM109/209/309 are complete 5 volt regulators fabricated on a single silicon chip. These regulators are designed for local "on card" regulation to eliminate many of the noise and ground loop problems associated with single-point regulation. They employ internal current limiting, thermal shutdown, and safe-area compensation which makes the circuitry essentially blow-out proof. If adequate heat sinking is provided, the devices can deliver output currents in excess of 200mA from the TO-5 package, and 1A from the TO-3 package. In addition to their use as fixed 5 volt regulators, these devices may be used with external components to obtain adjustable output levels. They may also be used as the power pass element in precision regulators.

FEATURES

- **Output currents in excess of 1mA**
- **Internal thermal overload protection**
- **Internal current limiting**
- **No external components required**
- **LM109 military qualifications pending**

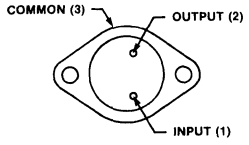
PIN CONFIGURATION

DB PACKAGE (TO-5).



ORDER PART NOS. LM109DB/LM209DB/LM309DB

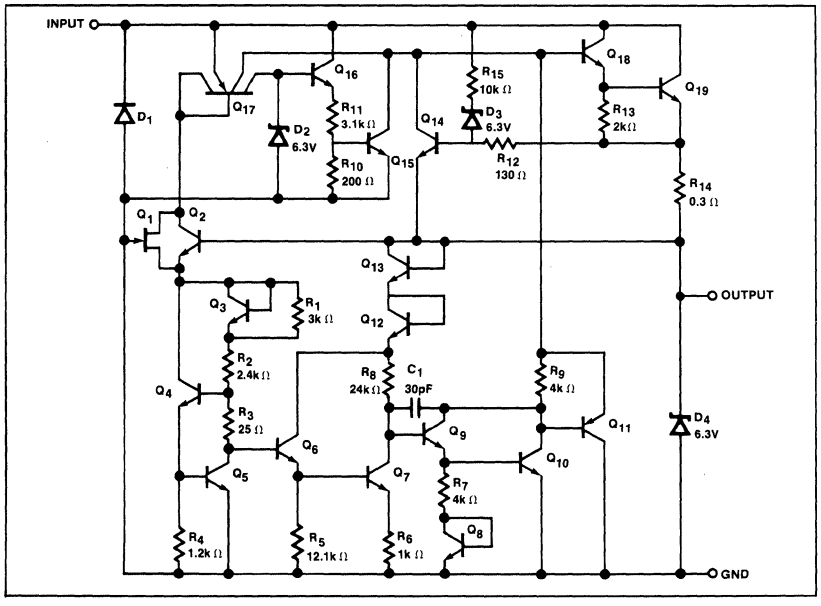
DA PACKAGE (TO-3)



CASE IS CONNECTED TO GROUND.

ORDER PART NO. LM109DA/LM209DA/LM309DA

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Input voltage	35	V
Power dissipation	Internally limited	
Operating junction temperature range		
LM109	-55 to 150	°C
LM209	-25 to 150	°C
LM309	0 to 125	°C
Storage temperature range	-65 to 150	°C
Lead temperature (soldering, 10 sec)	300	°C

DC ELECTRICAL CHARACTERISTICS

$T_J = 25°C$, $V_{IN} = 10V$ unless otherwise specified[1,2]

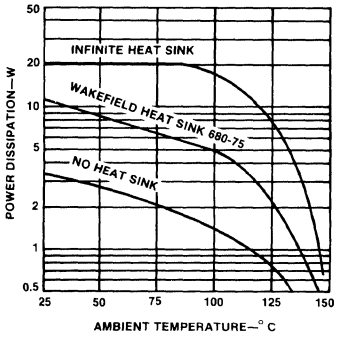
PARAMETER	TEST CONDITIONS	LM109/LM209			LM309			UNIT
		Min	Typ	Max	Min	Typ	Max	
Output voltage		4.7	5.05	5.3	4.8	5.05	5.2	V
Line regulation	$7V \le V_{IN} \le 25V$		4	50		4	50	mV
Load regulation								
TO-5	$5mA \le I_{OUT} \le 0.5A$		20	50		20	50	mV
TO-3	$5mA \le I_{OUT} \le 1.5A$		50	100		50	100	mV
Output voltage	$5mA \le I_{OUT} \le I_{max}$, $P < P_{max}$, over temp.							
	$8V \le V_{IN} \le 20V$	4.6		5.4				V
	$7V \le V_{IN} \le 25V$				4.75		5.25	V
Quiescent current	$7V \le V_{IN} \le 25V$, over temp.		5.2	10		5.2	10	mA
Quiescent current change	$5mA \le I_{OUT} \le I_{max}$			0.5			0.5	mA
	$8V \le V_{IN} \le 25V$			0.8				mA
	$7V \le V_{IN} \le 25V$						0.8	mA
Output noise voltage	$10Hz \le f \le 100kHz$		40			40		μV
Long term stability				10			20	mV
Thermal resistance junction to case[2]								
TO-5			15			15		°C/W
TO-3			3			3		°C/W

NOTES

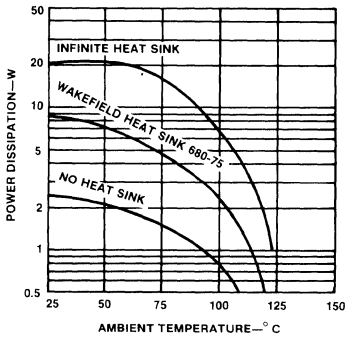
1. Unless otherwise specified, $I_{OUT} = 0.1A$ for the TO-5 package or $I_{OUT} = 0.5A$ for the TO-3 package. For the TO-5 package, Imax = 0.2A and Pmax = 2.0W. For the TO-3 package, Imax = 1.0A and Pmax = 20W.
2. Without a heat sink, the thermal resistance of the TO-5 package is about 150°C/W, while that of the TO-3 package is approximately 35°C/W. With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the sink.

TYPICAL PERFORMANCE CHARACTERISTICS

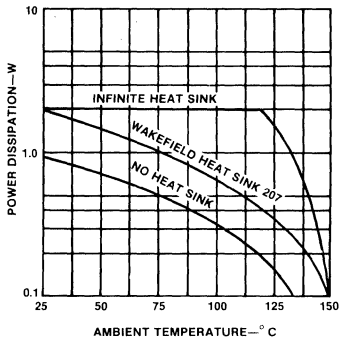
MAXIMUM AVERAGE POWER DISSIPATION LM109/LM209 (TO-3)



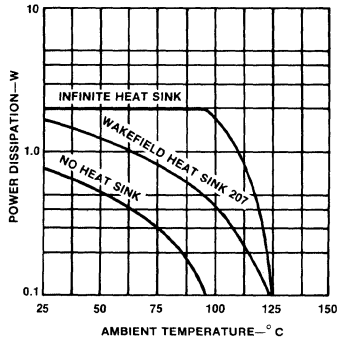
MAXIMUM AVERAGE POWER DISSIPATION LM309 (TO-3)



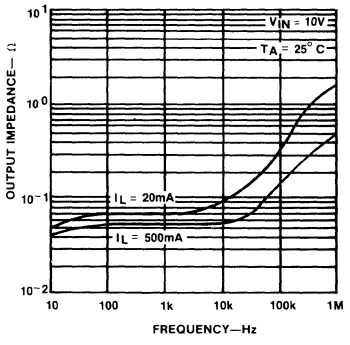
MAXIMUM AVERAGE POWER DISSIPATION LM109/LM209 (TO-5)



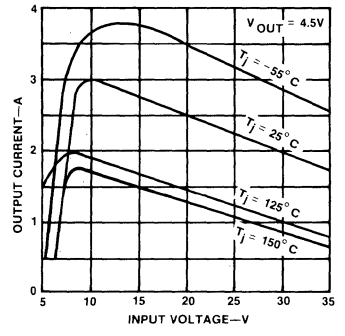
MAXIMUM AVERAGE POWER DISSIPATION LM309 (TO-5)



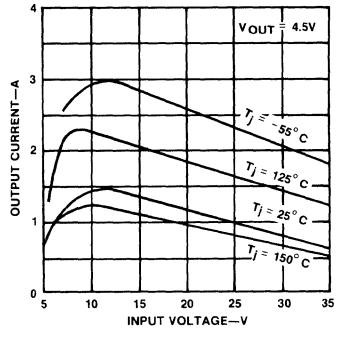
OUTPUT IMPEDANCE



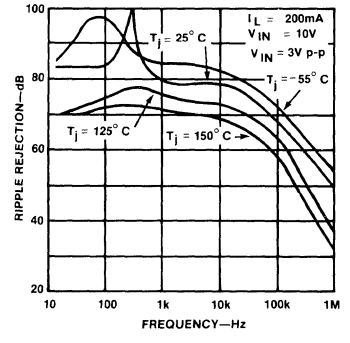
PEAK OUTPUT CURRENT DA PACKAGE (TO-3)



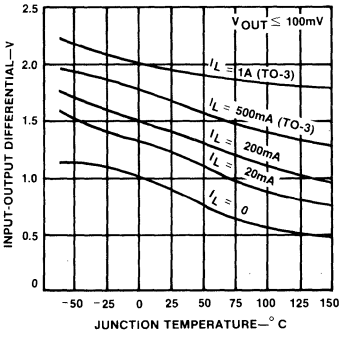
PEAK OUTPUT CURRENT DB PACKAGE (TO-5)



RIPPLE REJECTION



DROPOUT VOLTAGE



LM340-DA,U

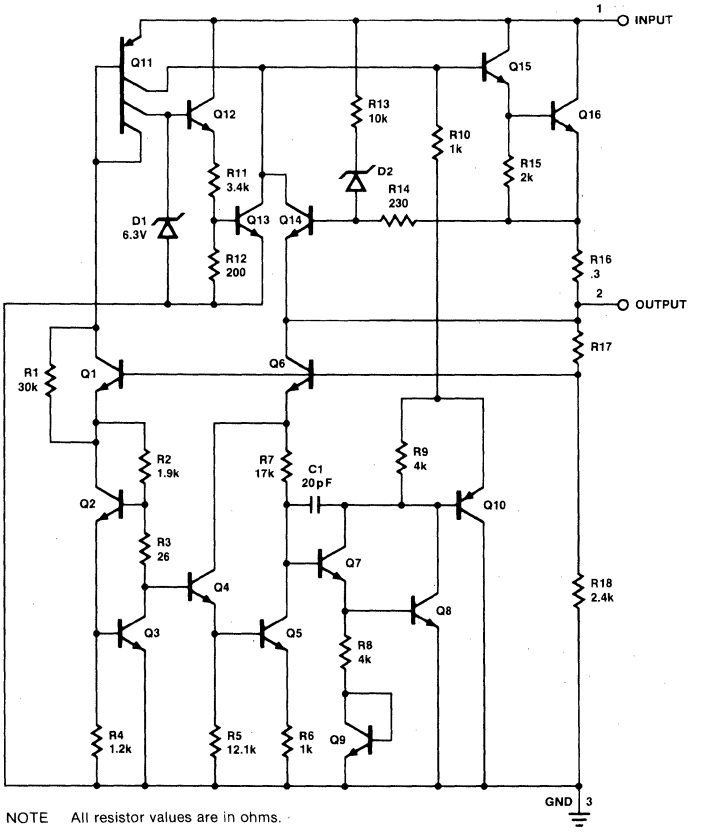
DESCRIPTION

The LM340 series of 3-terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages.

FEATURES

- **Output current in excess of 1A**
- **Internal thermal overload protection**
- **No external components required**
- **Output transistor safe area protection**
- **Internal short circuit current limit**
- **Available in plastic TO-220 and metal TO-3 packages**

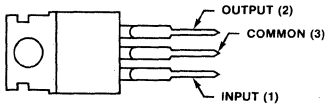
EQUIVALENT SCHEMATIC



NOTE All resistor values are in ohms.

PIN CONFIGURATION

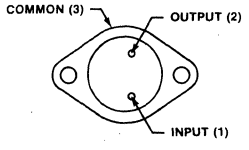
U PACKAGE (TO-220)
(Top View)



ORDER INFORMATION

OUTPUT VOLTAGE	ORDER PART NO.
5V	LM340-5U
6V	LM340-6U
8V	LM340-8U
12V	LM340-12U
15V	LM340-15U
18V	LM340-18U
24V	LM340-24U

DA PACKAGE (TO-3)
(Top View)



ORDER INFORMATION

OUTPUT VOLTAGE	ORDER PART NO.
5V	LM340-5DA
6V	LM340-6DA
8V	LM340-8DA
12V	LM340-12DA
15V	LM340-15DA
18V	LM340-18DA
24V	LM340-24DA

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Input voltage		
V_O = 5V through 18V	35	V
V_O = 24V	40	V
Internal power dissipation[1]	Internally limited	
Operating temperature range	0 to 70	°C
Maximum junction temperature		
TO-3 package	150	°C
TO-220 package	150	°C
Storage temperature range	-65 to +150	°C
Lead temperature		
TO-3 package (soldering 10sec)	300	°C
TO-220 package (soldering, 10sec)	230	°C

NOTE

1. Thermal resistance without a heat sink for junction to case temperature is 4°C/W for the TO-3 package and 6°C/W for the TO-220 package. Thermal resistance for case to ambient temperature is 35°C/W for the TO-3 package and 50°C/W for the TO-220 package.

DC ELECTRICAL CHARACTERISTICS

I_{OUT} = 500mA, (0°C ≤ T_A ≤ 70°C) unless otherwise specified.

PARAMETER	TEST CONDITIONS	LM340-5			LM340-6			LM340-8			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output voltage	T_J = 25°C	V_{IN} = 10V			V_{IN} = 11V			V_{IN} = 14V			
		4.8	5	5.2	5.75	6	6.25	7.7	8	8.3	V
	P_D = ≤ 15W	7V ≤ V_{IN} ≤ 20V			8V ≤ V_{IN} ≤ 21V			10.5V ≤ V_{IN} ≤ 23V			
	5mA ≤ I_{OUT} ≤ 1.0A	4.75		5.25	5.7		6.3	7.6		8.4	V
Line regulation	T_J = 25°C	7V ≤ V_{IN} ≤ 25V			8V ≤ V_{IN} ≤ 25V			10.5V ≤ V_{IN} ≤ 25V			
	I_{OUT} = 100mA			50			60			80	mV
	I_{OUT} = 500mA			100			120			160	
Load regulation	T_J = 25°C 5mA ≤ I_{OUT} ≤ 1.5A			100			120			160	mV
Quiescent current	T_J = 25°C		4.2	10		4.2	10		4.2	10	mA
Quiescent current change		7V ≤ V_{IN} ≤ 25V		1.3	8V ≤ V_{IN} ≤ 25V		1.3	10.5V ≤ V_{IN} ≤ 25V		1	mA
	5mA ≤ I_{OUT} ≤ 1.5A			.5			.5			.5	mA
Output noise voltage	T_J = 25°C 10Hz ≤ f ≤ 100kHz		40			45			52		μA
Voltage drift	mV/1000 Hrs.			20			24			32	mV
Ripple rejection	I_{OUT} = 20mA f = 120Hz		60			57			55		dB
Dropout voltage	T_J = 25°C	2			2			2.5			V

DC ELECTRICAL CHARACTERISTICS (Cont'd) I_{OUT} = 500mA, (0°C ≤ T_A ≤ 70°C) unless otherwise specified.

PARAMETER	TEST CONDITIONS	LM340-12			LM340-15			LM340-18			LM340-24			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output voltage	T_J = 25°C	V_{IN} = 19V			V_{IN} = 23V			V_{IN} = 27V			V_{IN} = 33V			
		11.5	12	12.5	14.4	15	15.6	17.3	18	18.7	23	24	25	V
	P_D = ≤ 15W	14.5V ≤ V_{IN} ≤ 27V			17.5V ≤ V_{IN} ≤ 30V			21V ≤ V_{IN} ≤ 33V			27V ≤ V_{IN} ≤ 38V			
	5mA ≤ I_{OUT} ≤ 1.0A	11.4		12.6	14.25		15.75	17.1		18.9	22.8		25.2	V
Line regulation	T_J = 25°C	14.5V ≤ V_{IN} ≤ 30V			17.5V ≤ V_{IN} ≤ 30V			21V ≤ V_{IN} ≤ 33V			27V ≤ V_{IN} ≤ 38V			
	I_{OUT} = 100mA			120			150			180			240	mV
	I_{OUT} = 500mA			240			300			360			480	mV
Load regulation	T_J = 25°C			240			300			360			480	mV
	5mA ≤ I_{OUT} ≤ 1.5A													
Quiescent current	T_J = 25°C		4.2	10		4.2	10		4.2	10		4.2	10	mA
Quiescent current change		14.5V ≤ V_{IN} ≤ 30V			17.5V ≤ V_{IN} ≤ 30V			21V ≤ V_{IN} ≤ 33V			27V ≤ V_{IN} ≤ 38V			
				1			1			1			1	mA
	5mA ≤ I_{OUT} ≤ 1.5A			.4			.5			.5			.5	mA
Output noise voltage	T_J = 25°C													
	10Hz ≤ f ≤ 100kHz		75			90			110			170		μV
voltage drift	mV/1000 Hrs.			48			60			72			96	mV
Ripple rejection	I_{OUT} = 20mA		52			50			48			44		dB
	f = 120Hz													
Dropout voltage	T_J = 25°C	2.5			2.5			3			3			V

OBJECTIVE SPECIFICATION NE/SE5551/2/3/4/5-N,T

DESCRIPTION

The NE/SE5551, 2, 3, 4, 5 are dual polarity tracking regulators designed to produce balanced or unbalanced output voltages from 5 to 20 volts with up to 300 mA output current. Similar in specifications to the 78MXX and 79MXX fixed regulators, the 5551 series can be continuously adjusted, balanced or unbalanced. Standard fixed voltages available are ±5, ±6, ±12, ±15, and +5, -12 volts. Employing current limiting and thermal shutdown protection, these dual polarity regulators are ideal for local on-card regulation.

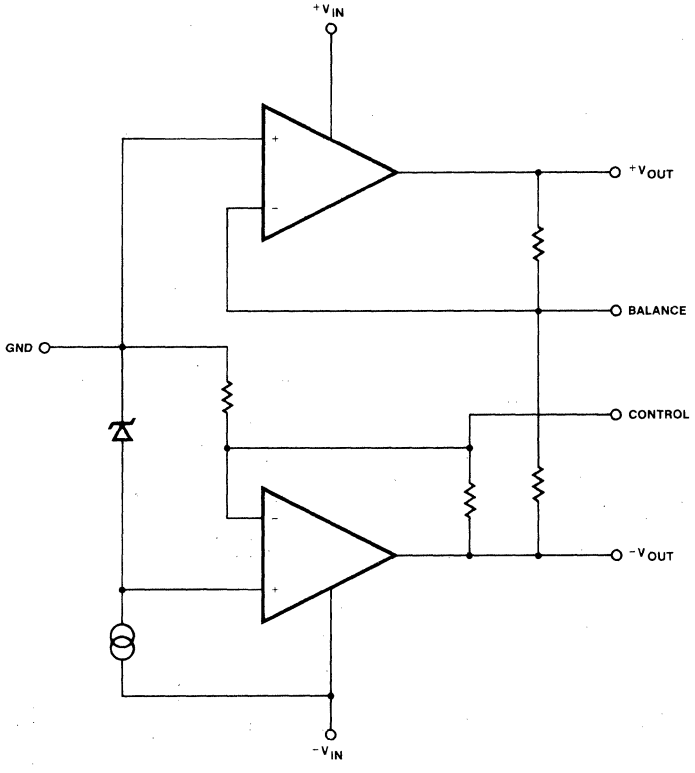
FEATURES

- **Output current to 300mA**
- **Internally current limited**
- **Thermal overload protected**
- **Input voltage to ±32V**
- **Output balance 1% typ.**
- **External balance control**
- **Continuously adjustable from 5 to 20 volts, balanced or unbalanced**
- **No external components required**
- **Short circuit current 400mA**
- **Heat sink available for increased power dissipation**

ABSOLUTE MAXIMUM RATINGS

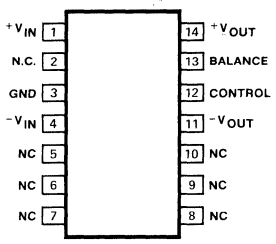
PARAMETER	RATING	UNIT
V_{IN} input voltage	±32	V
T_{SG} storage temperature	-65 to +150	°C
T_J operating junction temperature		
NE5551,2,3,4,5	0 to +125	°C
SE5551,2,3,4,5	-55 to +150	°C
Lead temperature 10 sec.	300	°C

BLOCK DIAGRAM



PIN CONFIGURATIONS

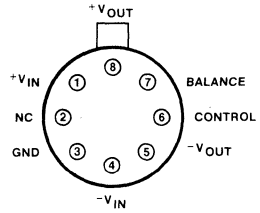
N PACKAGE



ORDER PART NUMBERS

VOLTAGE	PART NO.
±5V	SE/NE5551N
±6V	SE/NE5552N
±12V	SE/NE5553N
±15V	SE/NE5554N
+5, -12V	SE/NE5555N

T PACKAGE



ORDER PART NUMBERS

VOLTAGE	PART NO.
±5V	SE/NE5551T
±6V	SE/NE5552T
±12V	SE/NE5553T
±15V	SE/NE5554T
+5, -12V	SE/NE5555T

Power dissipation (without heat sink)
T Package 2.0W
N Package 2.0W
New power package pending for over 8W dissipation.

DC ELECTRICAL CHARACTERISTICS

V_{IN} = ±20V, I_L = 100mA, T_J = 25°C, C_{IN} = C_{OUT} = 0.1μF unless otherwise specified.

PARAMETER		TEST CONDITIONS	SE5551			NE5551			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage		+4.8 -5.2	+5 +5	+5.2 -4.8	+4.8 -5.2	+5 -5	+5.2 -4.8	V
	Line regulation Load regulation	±20 ≤ V_{IN} ≤ ±30V 1mA ≤ I_{Load} ≤ 50mA 1mA ≤ I_{Load} ≤ 200mA		100 5 15	150 15 50		100 5 15	300 25 100	mV mV mV
V_{OUT}	Output voltage	1mA ≤ I_L ≤ 100mA ±20V ≤ V_{IN} ≤ ±30V over temp.[1]	+4.7 -5.3	+5 -5	+5.3 -4.7	+4.7 -5.3	+5 -5	+5.3 -4.7	V V
I_Q+ I_Q-	Positive quiescent current Negative quiescent current	I_{Load} = 0 I_{Load} = 0		1.70 5.6	3.5 8.5		1.70 5.6	3.5 8.5	mA mA
V_{BAL}	Input/output differential voltage Output voltage balance Output noise voltage	 100Hz to 10kHz		7 .2 55			7 .2 55		V V μVRMS
I_{Peak}	Peak output current Temperature stability of output voltage			400 1			400 1		mA mV/°C

DC ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS	SE5552			NE5552			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage		+5.75 -6.25	+6 -6	+6.25 -5.75	+5.75 -6.25	+6 -6	+6.25 -5.75	V
	Line regulation Load regulation	±20 ≤ V_{IN} ≤ +30V 1mA ≤ I_{Load} ≤ 50mA 1mA ≤ I_{Load} ≤ 200mA		100 5 15	150 15 50		100 5 15	300 25 100	mV mV mV
V_{OUT}	Output voltage	1mA ≤ I_L ≤ 100mA ±20V ≤ V_{IN} ≤ ±30V over temp.[1]	+5.7 -6.3	+6 -6	+6.3 -5.7	+5.7 -6.3	+6 -6	+6.3 -5.7	V V
I_Q+ I_Q-	Positive quiescent current Negative quiescent current	I_{Load} = 0 I_{Load} = 0		1.70 5.6	3.5 8.5		1.70 5.60	3.5 8.5	mA mA
V_{BAL}	Input/output differential voltage Output voltage balance Output noise voltage	 100Hz to 10kHz		6 .2 55			6 .2 55		V V μVrms
I_{Peak}	Peak output current Temperature stability of output voltage			400 1			400 1		mA mV/°C

DC ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS	SE5553			NE5553			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage		+11.5 -12.5	+12 -12	+12.5 -11.5	+11.5 -12.5	+12 -12	+12.5 -11.5	V
	Line regulation Load regulation	±20 ≤ V_{IN} ≤ ±30V 1mA ≤ I_{Load} ≤ 50mA 1mA ≤ I_{Load} ≤ 200mA		100 10 30	150 25 100		100 10 30	300 50 200	mV mV mV
V_{OUT}	Output voltage	1mA ≤ I_L ≤ 100mA ±20V ≤ V_{IN} ≤ ±30V over temp.[1]	+11.4 -12.6	+12 -12	+12.6 -11.4	+11.4 -12.6	+12 -12	+12.6 -11.4	V V
I_Q+ I_Q-	Positive quiescent current Negative quiescent current	I_{Load} = 0 I_{Load} = 0		1.70 5.60	3.5 8.5		1.70 5.60	3.5 8.5	mA mA
V_{BAL}	Input/output differential voltage Output voltage balance Output noise voltage	 100Hz to 10kHz		2.5 .2 55			2.5 .2 55		V V μVrms
I_{Peak}	Peak output current Temperature stability of output voltage			400 1			400 1		mA mV/°C

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_{IN} = \pm 20V$, $I_L = 100mA$, $T_J = 25°C$, $C_{IN} = C_{OUT} = 0.1\mu F$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SE5554			NE5554			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage		+14.4 -15.6	+15 -15	+15.6 -14.4	+14.4 -15.6	+15 -15	+15.6 -14.4	V
	Line regulation Load regulation	$\pm 20 \leq V_{IN} \leq \pm 30V$ $1mA \leq I_{Load} \leq 50mA$ $1mA \leq I_{Load} \leq 200mA$		100 10 30	150 25 100		100 10 30	300 50 200	mV mV mV
V_{OUT}	Output voltage	$1mA \leq I_L \leq 100mA$ $\pm 20V \leq V_{IN} \leq \pm 30V$ over temp.[1]	+14.25 -15.75	+15 -15	+15.75 -14.25	+14.25 -15.75	+15 -15	+15.75 -14.25	V V
I_Q+ I_Q-	Positive quiescent current Negative quiescent current	$I_{Load} = 0$ $I_{Load} = 0$		1.70 5.60	3.5 8.5		1.70 5.60	3.5 8.5	mA mA
V_{BAL}	Input/output differential voltage Output voltage balance Output noise voltage	100Hz to 10kHz		2.5 .2 55			2.5 .2 55		V V μVrms
I_{Peak}	Peak output current Temperature stability of output voltage			400 1			400 1		mA mV/°C

DC ELECTRICAL CHARACTERISTICS (Cont'd)

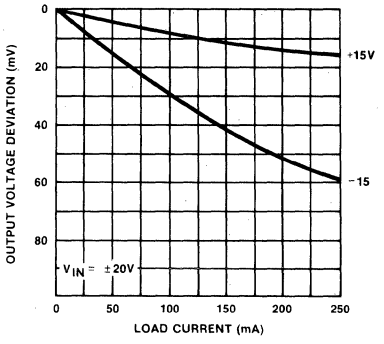
PARAMETER		TEST CONDITIONS	SE5555			NE5555			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage		+4.8 -12.5	+5 -12	+5.2 -11.5	+4.8 -12.5	+5 -12	+5.2 -11.5	V
	Line regulation Load regulation	$\pm 20 \leq V_{IN} \leq \pm 30V$ $1mA \leq I_{Load} \leq 50mA$ $1mA \leq I_{Load} \leq 200mA$		100 10 30	150 25 100		100 10 30	300 50 200	mV mV mV
V_{OUT}	Output voltage	$1mA \leq I_L \leq 100mA$ $\pm 20V \leq V_{IN} \leq \pm 30V$ over temp.[1]	+4.7 -12.6	+5 -12	+5.3 -11.4	+4.7 -12.6	+5 -12	+5.3 -11.4	V V
I_Q+ I_Q-	Positive quiescent current Negative quiescent current	$I_{Load} = 0$ $I_{Load} = 0$		1.70 5.60	3.5 8.5		1.70 5.60	3.5 8.5	mA mA
V_{BAL}	Input/output differential voltage Output voltage balance Output noise voltage	100Hz to 10kHz		2.5 .2 55			2.5 .2 55		V V μVrms
I_{Peak}	Peak output current Temperature stability of output voltage			400 1			400 1		mA mV/°C

NOTES

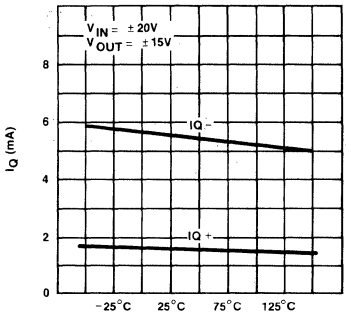
1. Junction temperature range
   SE prefix $-55°C < T_J < 150°C$
   NE prefix $0°C < T_J < 125°C$
2. C_{IN} needed only when isolated from filter capacitors
   C_{OUT} needed only if dynamic regulation is to be improved.
3. Thermal resistance, DIP
   $\theta_{JA} = 95°C/W$ $\theta_{JC} = 35°C/W$, TO-5
   $\theta_{JA} = 150°C/W$ $\theta_{JC} = 25°C/W$

TYPICAL PERFORMANCE CHARACTERISTICS

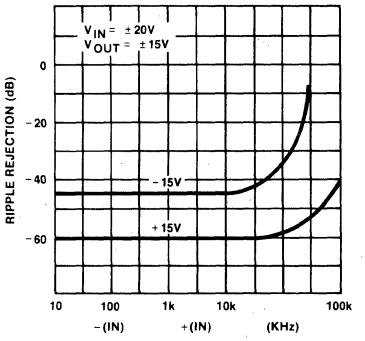
LOAD REGULATION



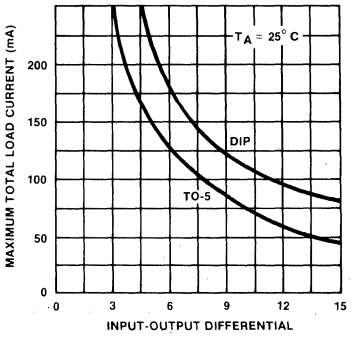
IQ +, IQ -



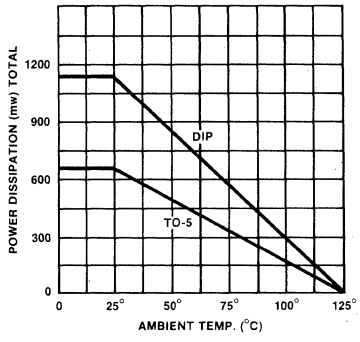
RIPPLE REJECTION



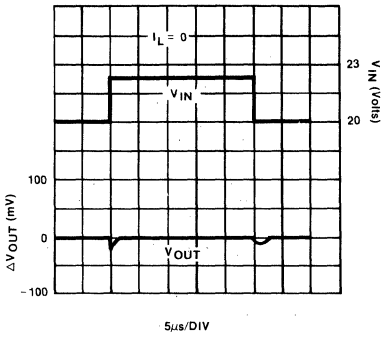
MAXIMUM CURRENT CAPABILITY



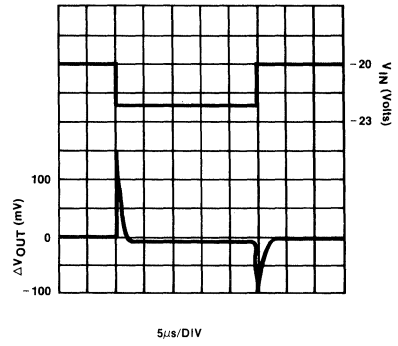
MAXIMUM POWER DISSIPATION[4]



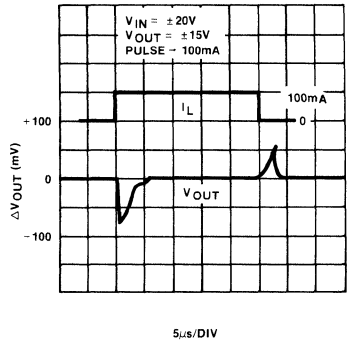
LINE TRANSIENT RESPONSE, POSITIVE



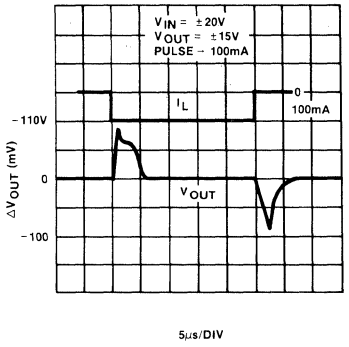
LINE TRANSIENT RESPONSE, NEGATIVE



LOAD TRANSIENT RESPONSE, POSITIVE



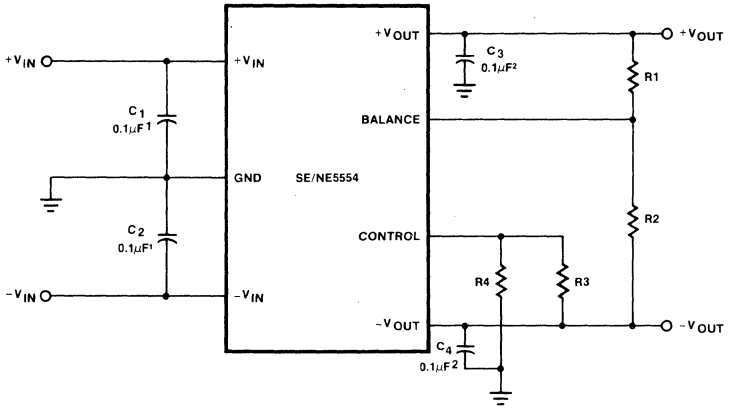
LOAD TRANSIENT RESPONSE, NEGATIVE



4. Device capability in free air.

BLOCK DIAGRAM

TYPICAL CONNECTION



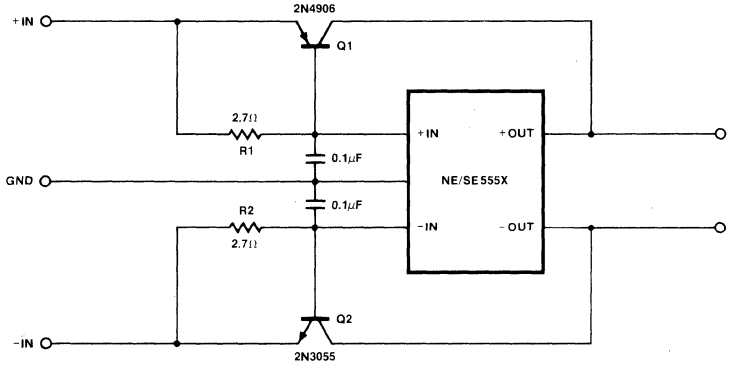
R1 and R2 adjust $+V_{OUT}$ with respect to $-V_{OUT}$
R3 and R4 adjust $-V_{OUT}$ From -5V to -20V

NOTES

1. Required if regulator is operated any distance from filter capacitor.
2. Not required for stability, but improves dynamic regulation.

TYPICAL APPLICATIONS

HIGH CURRENT TRACKING REGULATOR



$$R1 = R2 = \frac{V_{BE}}{I_{REG}(max)\,(\beta + 1) - I_{out}(max)}$$

For

$$\beta(Q) \geq \frac{I_{out\ (max)}}{I_{reg\ (max)}}$$

SE/NE550-F,L,N

DESCRIPTION

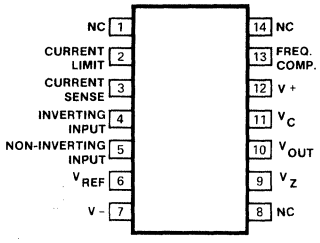
The 550 is a precision monolithic voltage regulator capable of positive or negative supply operation as series, shunt, switching or floating regulator. Guaranteed line regulation is provided for input voltages ranging from 8.5 volts to as high as 50 volts. The output voltage can be continuously adjusted from 2 volts to 40 volts. Foldback current limiting can be accomplished through the use of one external resistor. Internal circuitry permits on and off strobing with DTL and TTL logic inputs and latched shut-down with a pulsed input.

FEATURES

- **Line regulation guaranteed over input voltage range of 8.5 volts to as high as 50 volts.**
- **Output voltage continuously adjustable from 2 volts to 40 volts**
- **.01% line and load regulation**
- **Adjustable limiting of short circuit current**
- **Foldback current limiting with one external resistor**
- **Remote and latching shutdown**
- **Output current up to 150mA without external power transistors**

PIN CONFIGURATIONS

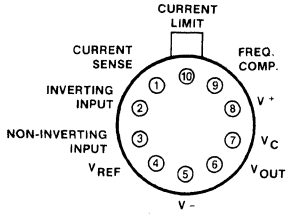
F,N PACKAGE



ORDER PART NO.

SE550F	NE550N
SE550F	NE550F

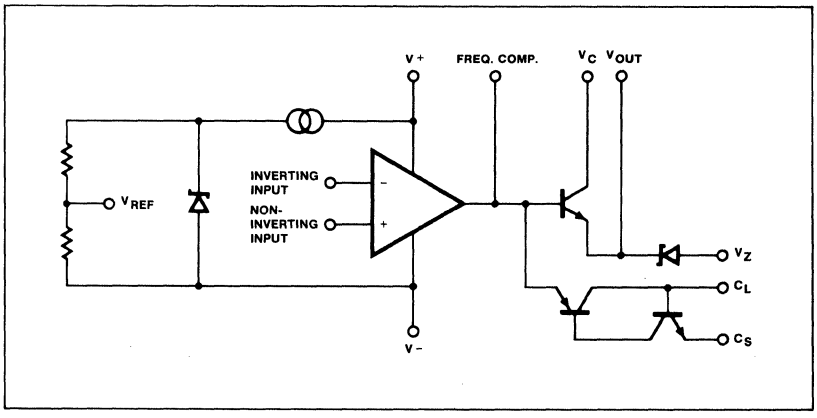
L PACKAGE



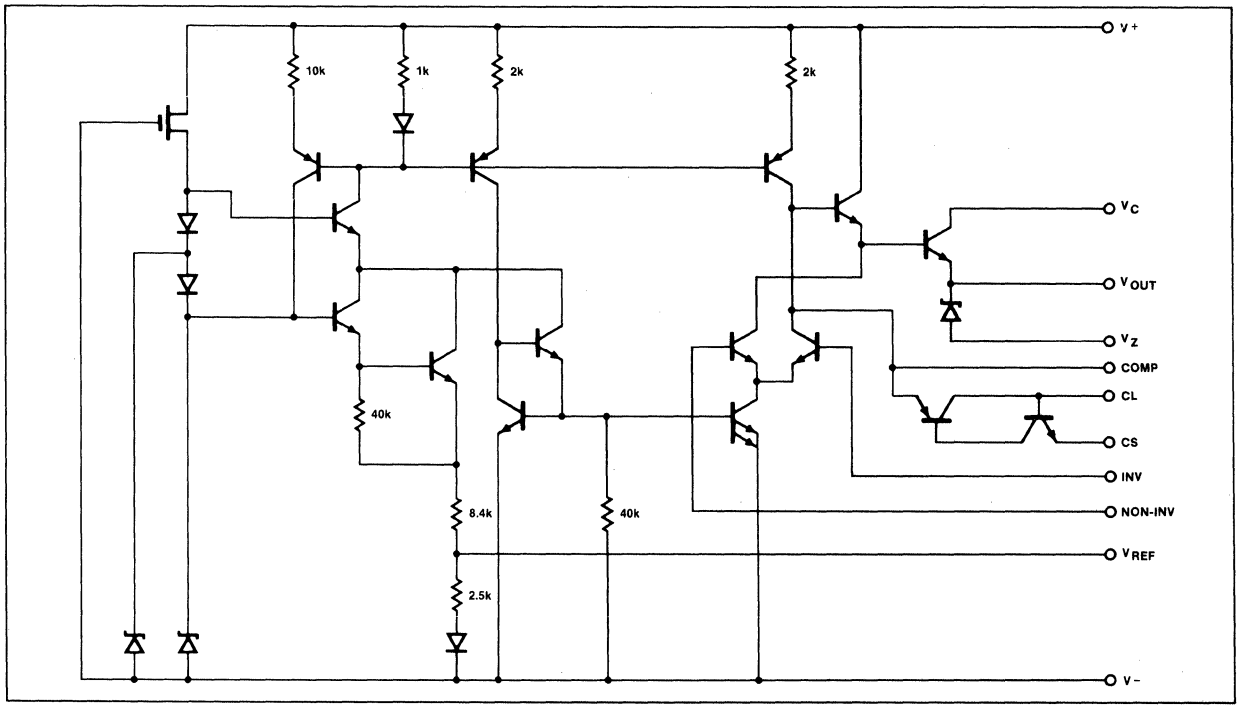
ORDER PART NO.

SE550L	NE550L

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Voltage from V+ to V-		
SE550	50	V
NE550	40	V
Input-output voltage differential		
SE550	45	V
NE550	37	V
Maximum output current		
SE550	150	mA
NE550	150	mA
Current from V_Z		
SE550	15	mA
NE550	15	mA
Internal power dissipation[1]		
SE550	800	mW
NE550	800	mW
Operating temperature range		
SE550	-55 to +125	°C
NE550	0 to 70	°C
Storage temperature range		
SE550	-65 to +150	°C
NE550	-65 to +150	°C
Lead temperature		
SE550	300	°C
NE550	300	°C

NOTE

1. Rating applies for case temperatures to 125°C; derate linearly at 6.5mW/°C for ambient termperature above +75°C.

DC ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise specified.[1,2]

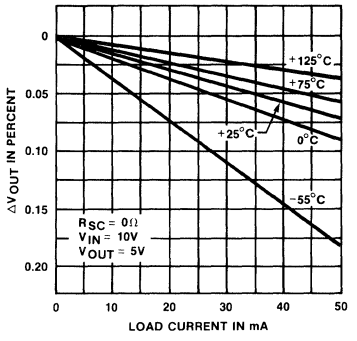
PARAMETER	TEST CONDITIONS	NE550			SE550			UNIT
		Min	Typ	Max	Min	Typ	Max	
Line regulation	V_{IN} = 8.5 to 40V		.08	0.3				%V_{OUT}
	0°C ≤ T_A ≤ 70°C, V_{IN} = 12 to 40V			0.35				%V_{OUT}
	V_{IN} = 12 to 40V					0.05	0.1	%V_{OUT}
	V_{IN} = 8.5 to 50V					0.2	0.6	%V_{OUT}
	-55°C ≤ T_A ≤ +125°C, V_{IN} = 12 to 40V						0.25	%V_{OUT}
Load regulation	I_L = 1mA to 50mA		.03	0.2		0.03	.10	%V_{OUT}
	0°C ≤ T_A ≤ 70°C			0.4				%V_{OUT}
	-55°C ≤ T_A ≤ +125°C						.6	%V_{OUT}
Ripple rejection	f = 50Hz to 10kHz							dB
	C_{REF} = 0		75			75		dB
	C_{REF} = 5μF		90			90		dB
Average temperature coefficient of output voltage	-55° ≤ T_A ≤ +125°C					.002	.012	%/°C
	0°C ≤ T_A ≤ 70°		.002	.015				%/°C
Short circuit limit	RSC = 10Ω, V_{OUT} = 0	50	60	70	50	60	70	mA
Reference voltage		1.58	1.63	1.73	1.58	1.63	1.68	V
Output noise voltage	BW = 100Hz to 10kHz, C_{REF} = 0		20			20		μVrms
	BW = 100Hz to 10kHz, C_{REF} = 5μF		2.5			2.5		μVrms
Long term stability						0.1		%/1000hrs.
Standby current drain	I_L = 0, V_{IN} = 50V					1.3	2.0	mA
	I_L = 0, V_{IN} = 40V		1.6	3.0				mA
Input voltage range		8.5		40	8.5		50	V
Output voltage range		2.0		40	2.0		37	V
Input-output voltage differential		3.0		38	3.0		45	V

NOTES

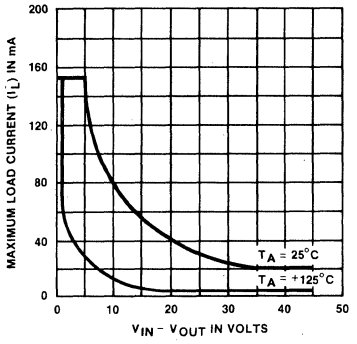
1. V_{IN} = V+ = V_C = 12V, V- = 0V, V_{OUT} = 5V, I_L = 1mA, R_{SC} = 0, CI = 100pF, and divider impedance as seen by error amplifier ≈ 2kΩ.
2. The load and line regulation specifications are for constant temperature junction. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high or varying dissipation.

TYPICAL PERFORMANCE CHARACTERISTICS

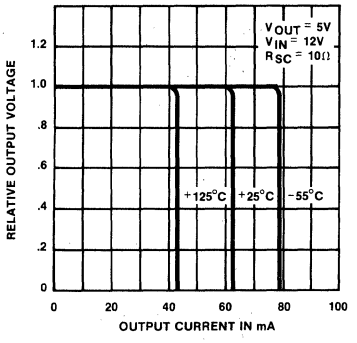
LOAD REGULATION AS A FUNCTION OF LOAD CURRENT



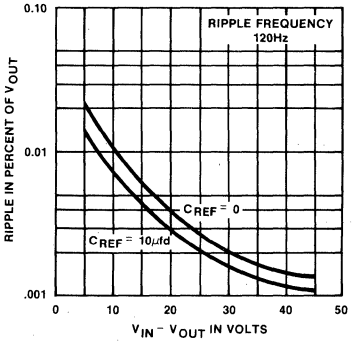
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



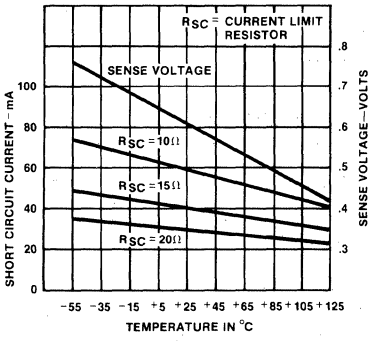
RELATIVE OUTPUT VOLTAGE AS A FUNCTION OF LIMITED OUTPUT CURRENT



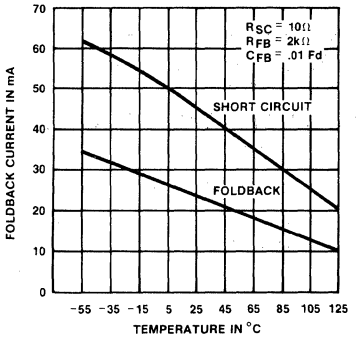
RIPPLE REJECTION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



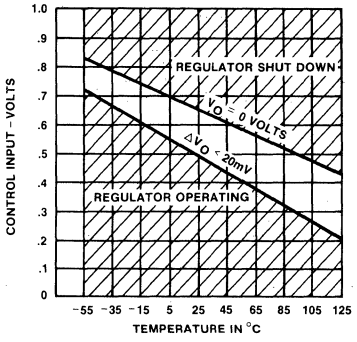
SENSE VOLTAGE AND SHORT CIRCUIT CURRENT LIMIT AS A FUNCTION OF TEMPERATURE



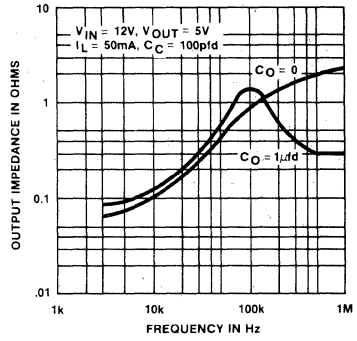
SHORT CIRCUIT AND FOLDBACK CURRENTS AS A FUNCTION OF TEMPERATURE



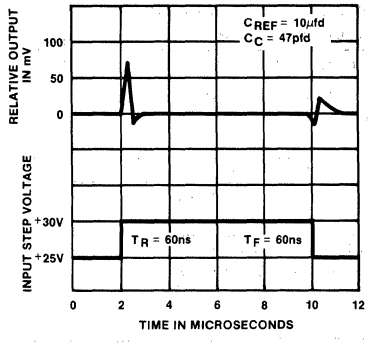
REMOTE CONTROL CHARACTERISTICS AS A FUNCTION OF TEMPERATURE



OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY

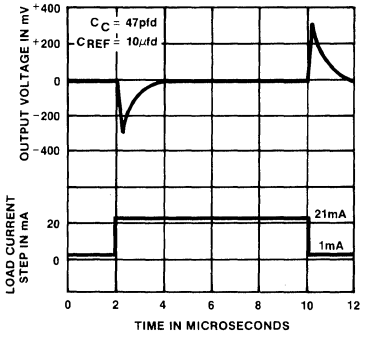


LINE TRANSIENT RESPONSE

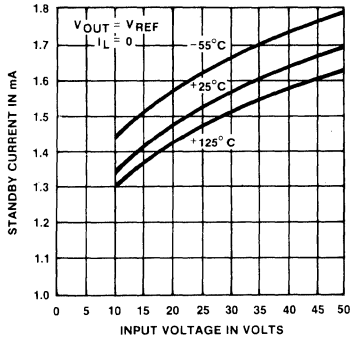


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

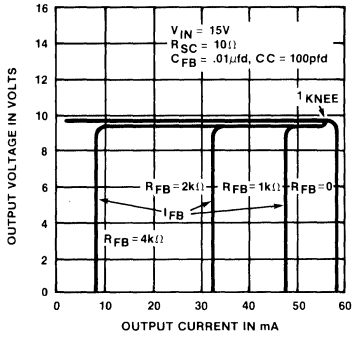
LOAD TRANSIENT RESPONSE



STANDBY CURRENT AS A FUNCTION OF INPUT VOLTAGE

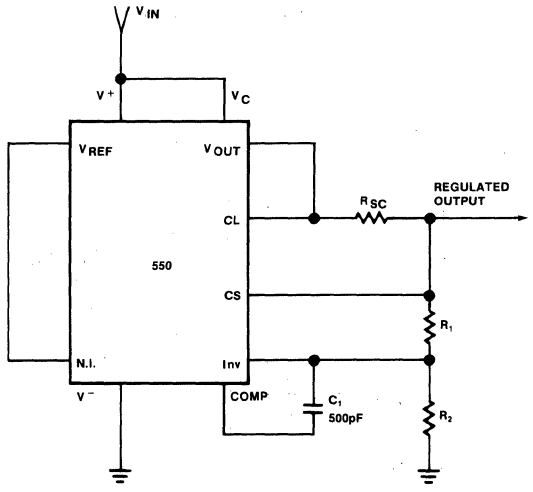


FOLDBACK CURRENT LIMITED OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



TYPICAL APPLICATIONS

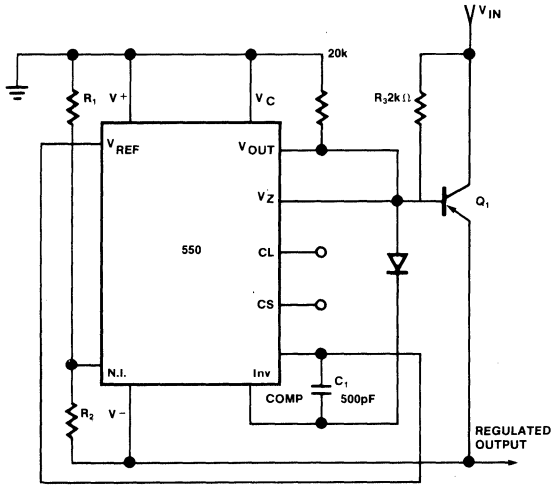
BASIC POSITIVE VOLTAGE REGULATOR



$$V_{OUT} = V_{REF}\frac{R_1 + R_2}{R_2} \quad ISC = \frac{V_{SENSE}}{RSC}$$

$$\frac{R_1R_2}{R_1 + R_2} = 2k\Omega \text{ for minimum temperature drift}$$

NEGATIVE VOLTAGE REGULATOR



$$V_{OUT} = -V_{REFX}\frac{R_1 + R_2}{R_2}$$

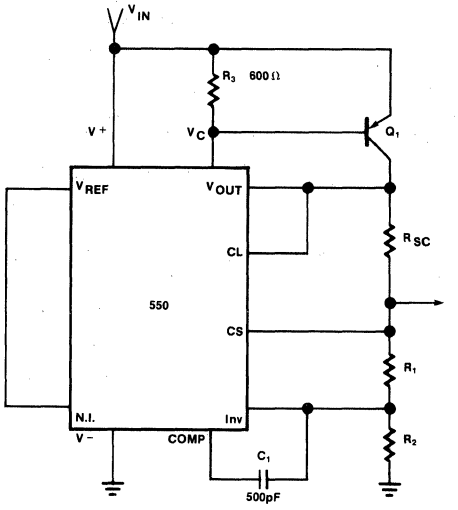
$$\frac{R_1R_2}{R_1 + R_2} = 2k\Omega \text{ for minimum temperature drift}$$

NOTE

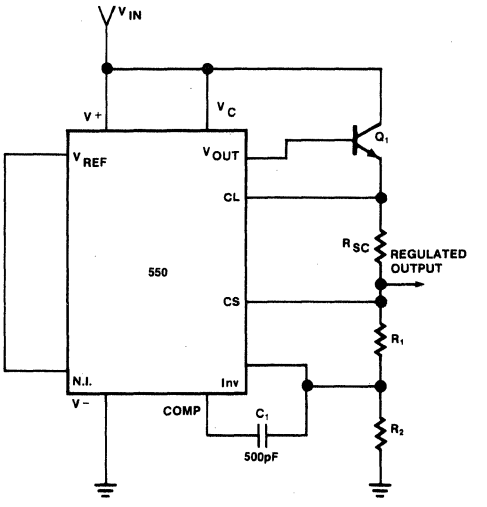
To utilize the SE550L in applications which require Vz, an external 6.2 volt zener diode should be connected in series with V_{OUT}.

TYPICAL APPLICATIONS (Cont'd)

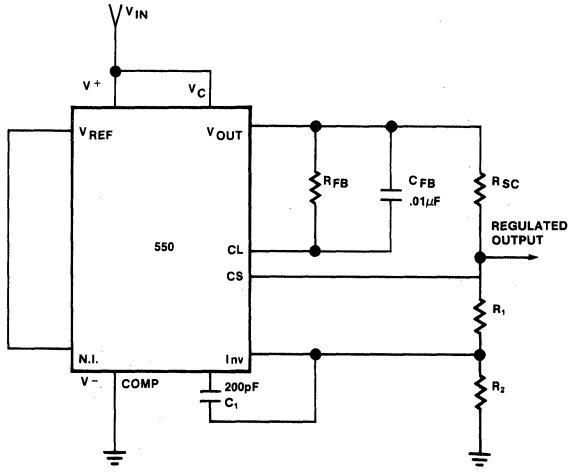
POSITIVE VOLTAGE REGULATOR (External PNP Pass Transistor)



POSITIVE VOLTAGE REGULATOR (External NPN Pass Transistor)



FOLDBACK CURRENT LIMITED REGULATOR

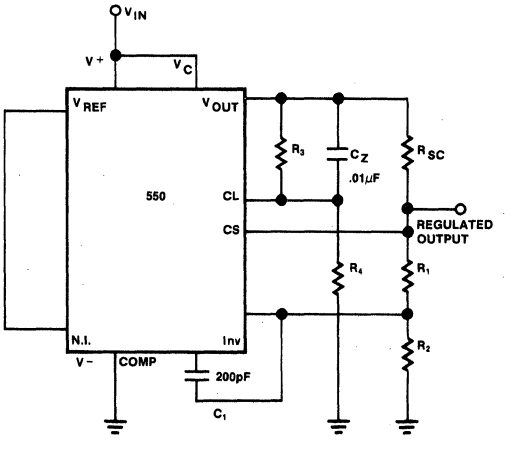


$$I_{KNEE} = \frac{V_{SENSE}}{R_{SC}}$$

$$I_{FB} = \frac{V_{SENSE} - (R_{FB} - I_{CL})}{R_{SC}}$$

$$I_{CL} = 125\mu A$$

SECOND ORDER FOLDBACK CURRENT LIMITED REGULATOR



$$R_3 = \frac{V_{SENSE}\,(I_{KNEE} - I_{FB})\,V_{OUT}}{I_{CL}\,(I_{KNEE} - I_{FB} + I_{SC})\,V_{OUT} - (I_{FB} - I_{SC})\,V_{SENSE}}$$

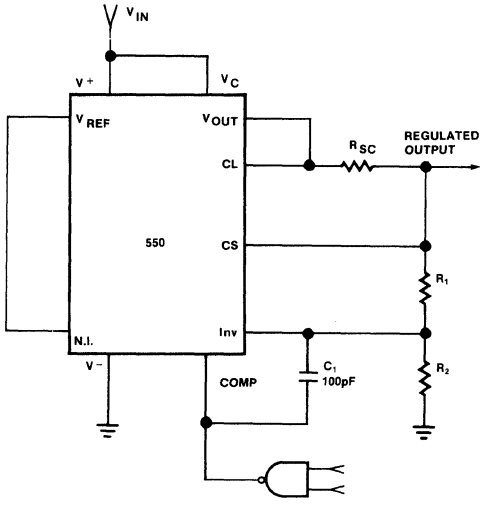
$$\frac{R_3}{R_4} = \frac{(V_{SENSE} - I_{CL}\,R_3)\,(I_{FB} - I_{SC})}{V_{OUT}\,I_{SC} - V_{SENSE}\,(I_{FB} - I_{SC})}$$

$$R_{SC} = \frac{(V_{OUT} + V_{SENSE})\,R_3/R_4 + V_{SENSE}}{I_{KNEE}}$$

$$I_{CL} = 125\mu A$$

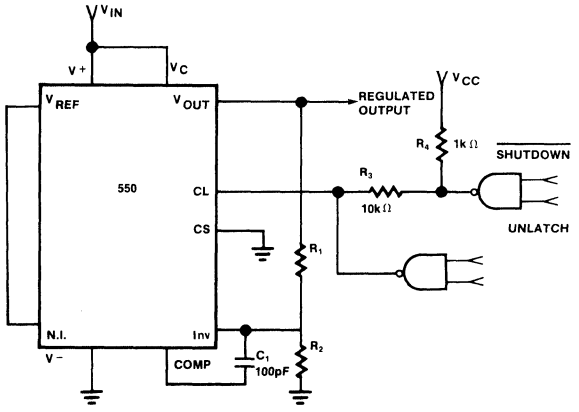
TYPICAL APPLICATIONS (Cont'd)

REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING



1/4 8T80, 1/6 8T90, 1/10 8TO1B, etc.

REMOTE LATCHING SHUTDOWN REGULATOR

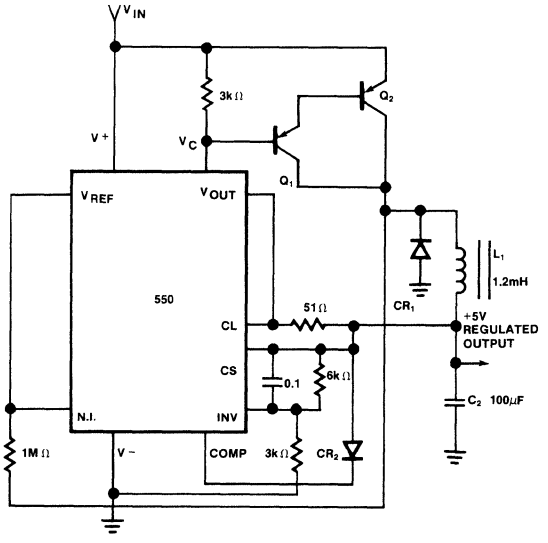


8415, 8417, 2/3 8471, 1/3 8891, 8T90, 1/2 8481, 8881, 8T90

NOTE

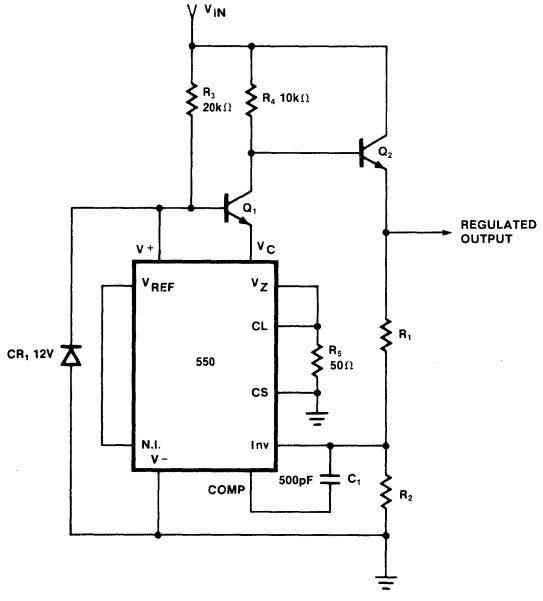
The "Shut-down" gate need only be pulsed to latch the regulator output to zero. R4 may omitted for active pull-up devices. The "Unlatch" gate must have an open collector.

POSITIVE SWITCHING REGULATOR



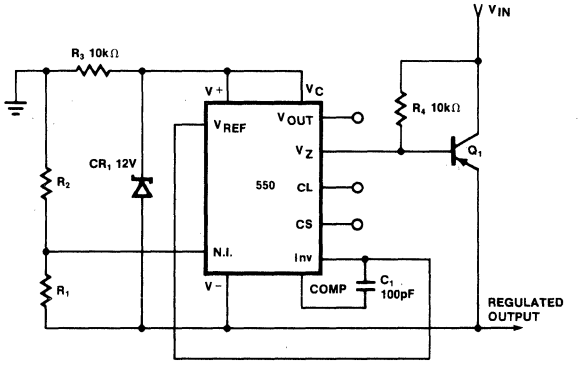
L_1 is 50 turns of #22 wire wound on Ferroxcube. 42/29-377 A400

POSITIVE FLOATING REGULATOR



TYPICAL APPLICATIONS (Cont'd)

NEGATIVE FLOATING REGULATOR



μA723/723C/SA723C-F,L,N

DESCRIPTION

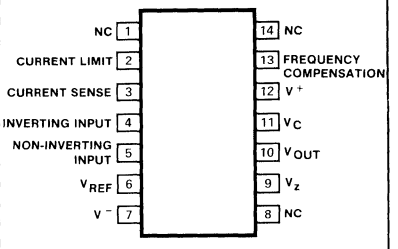
The μA723/SA723C is a Monolithic Precision Voltage Regulator capable of operation in positive or negative supplies as a series, shunt, switching or floating regulator. The 723 contains a temperature compensated reference amplifier, error amplifier, series pass transistor, and current limiter, with access to remote shutdown.

FEATURES

- **Positive or negative supply operation**
- **Series, shunt, switching or floating operation**
- **.01% line and load regulation**
- **Output voltage adjustable from 2 to 37 volts**
- **Output current to 150mA without external pass transistor**
- **μA723 MIL STD 88 3A, B, C available**

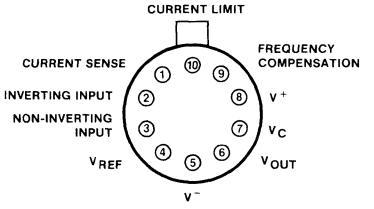
PIN CONFIGURATION

F,N PACKAGE



ORDER PART NOS. μA723N, μA723F, μA723CN, μA723CF, SA723CF, SA723CN

L PACKAGE

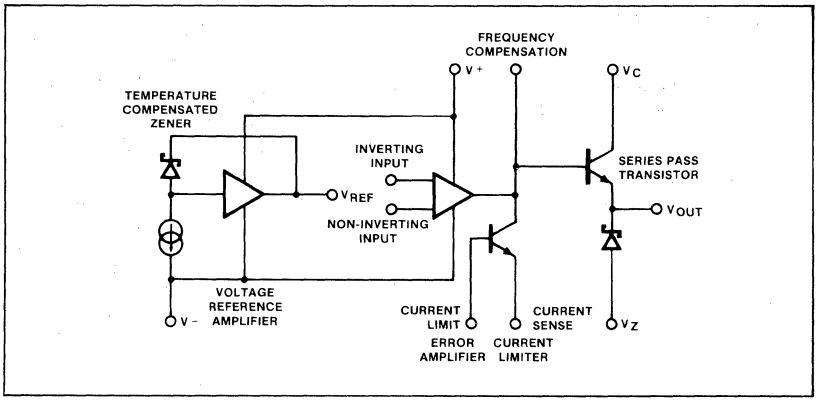


ORDER PART NOS. μA723L/μA723CL

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Pulse voltage from V+ to V- (50 ms)		
μA723	50	V
μA723C		
SA723C		
Continous voltage from V+ to V-		
μA723	40	V
μA723C	40	V
SA723C	40	V
Input-output voltage differential	40	V
Maximum output current		
μA723	150	mA
μA723C	150	mA
SA723C	150	mA
Current from V_{REF}		
μA723	15	mA
μA723C		
SA723C		
Current from V_Z		
μA723		
μA723C	25	mA
SA723C	25	mA
Internal power dissipation[1]		
μA723	800	mA
μA723C	800	mA
SA723C	800	mA
Operating temperature range		
μA723	-55 to +125	°C
μA723C	0 to 70	°C
SA723C	-40 to +85	°C
Storage temperature range		
μA723	-65 to +150	°C
μA723C	-65 to +150	°C
SA723C	-65 to +150	°C
Lead temperature		
μA723	300	°C
μA723C	300	°C
SA723C	300	°C

EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.[1]

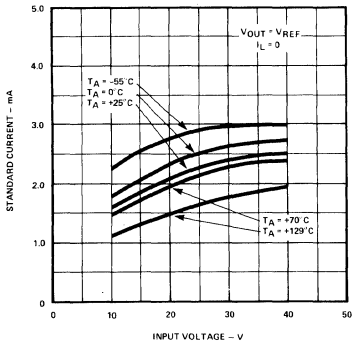
PARAMETER	TEST CONDITIONS	μA723C/SA723C			μA723			UNIT
		Min	Typ	Max	Min	Typ	Max	
Line regulation[2]	V_{IN} = 12V to V_{IN} = 15V V_{IN} = 12V to V_{IN} = 40V		0.01 0.1	0.1 0.5		0.01 0.02	0.1 0.2	$\%V_{OUT}$ $\%V_{OUT}$
Load regulation[2]	I_L = 1mA to I_L = 50mA f = 50Hz to 10kHz, C_{REF} = 0 f = 50Hz to 10kHz, C_{REF} = 5μF		0.03 74 86	0.2		0.03 74 86	0.15	$\%V_{OUT}$ dB dB
Short circuit current limit	R_{SC} = 10Ω, V_{OUT} = 0		65			65		mA
Reference voltage Output noise voltage	 BW = 100Hz to 10kHz, C_{REF} = 0 BW = 100Hz to 10kHz, C_{REF} = 5μF	6.80	7.15 20 2.5	7.50	6.95	7.15 20 2.5	7.35	V μVrms μVrms
Long term stability Standby current drain	 I_L = 0, V_{IN} = 30V		0.1 2.3	0.1 4.0	 2.3	0.1 3.5		%/1000hrs. mA
Input voltage range Output voltage range		9.5 2.0		40 37	9.5 2.0		40 37	V V
Input-output voltage differential		3.0		38	3.0		38	V
The following specifications apply over the operating temperature ranges Line regulation				0.3			0.3	$\%V_{OUT}$
Load regulation				0.6			0.6	$\%V_{OUT}$
Average temperature coefficient of output voltage	V_{IN} = 12V to V_{IN} = 15V I_L = 1mA to I_L = 50mA		0.003	0.015		0.002	0.015	%/°C

NOTES

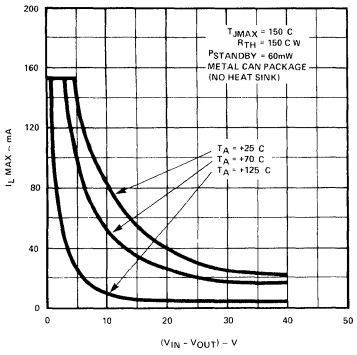
1. $V_{IN} = V+ = V_C = 12V$, $V- = 0V$, $V_{OUT} = 5V$, $I_L = 1mA$, $R_{SC} = 0$, $C_1 = 100pF$, $C_{REF} = 0$ and divider impedance as seen by error amplifier ≤ 10kΩ when connected as shown in Figure 3.
2. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

TYPICAL PERFORMANCE CHARACTERISTICS

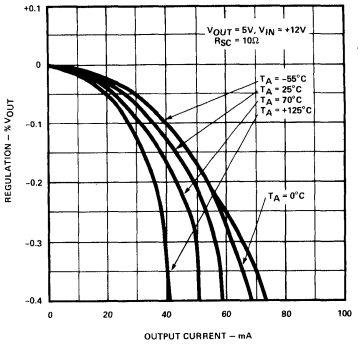
STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE



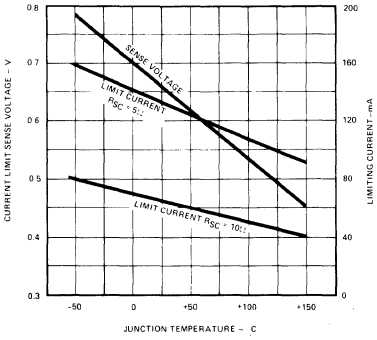
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



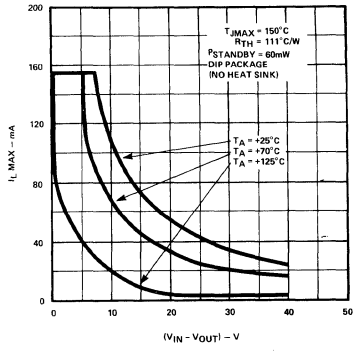
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



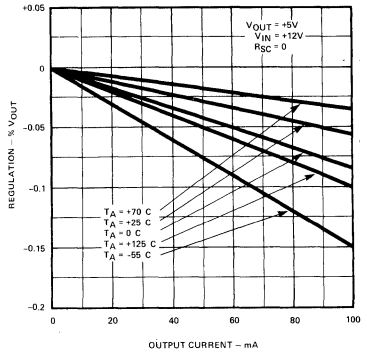
CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



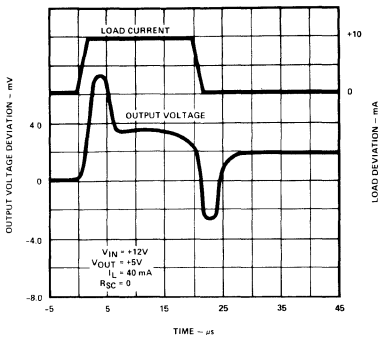
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



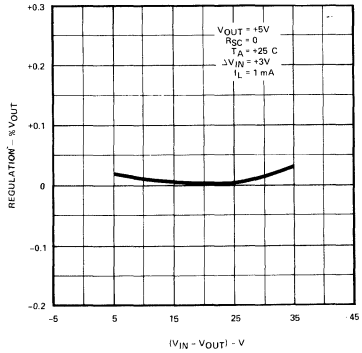
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



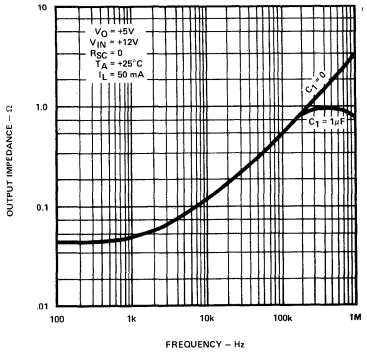
LOAD TRANSIENT RESPONSE



LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

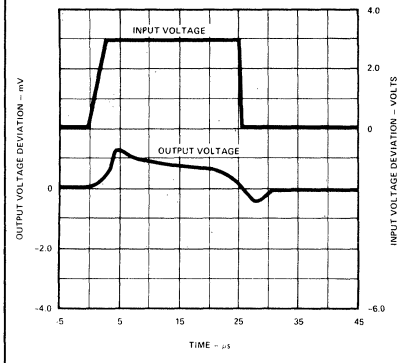


OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY

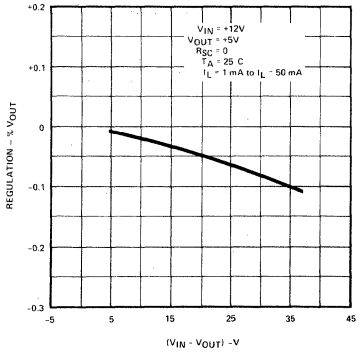


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

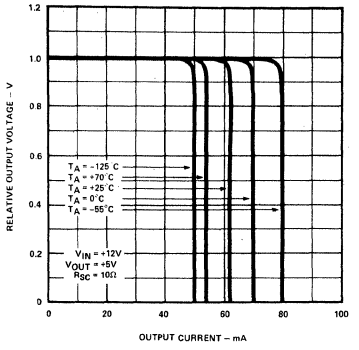
LINE TRANSIENT RESPONSE



LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

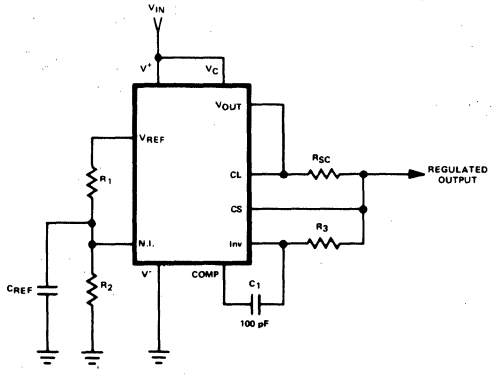


CURRENT LIMITING CHARACTERISTICS



TYPICAL APPLICATIONS

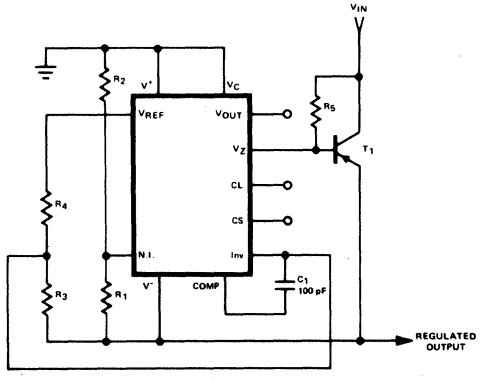
LOW VOLTAGE REGULATOR (V_{OUT} = 2 TO 7 VOLTS)



$$V_{out} = \left[V_{REF} \times \frac{R_2}{R_1 + R_2} \right]$$

$$R_3 = \frac{R_1 \ R_2}{R_1 + R_2} \quad \text{for minimum temperature drift}$$

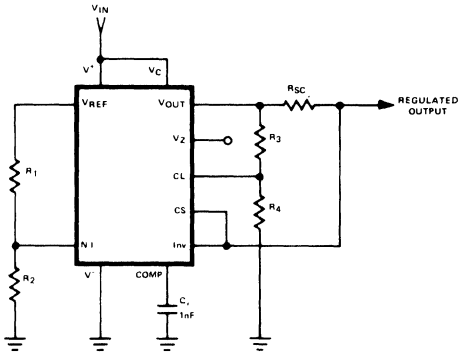
NEGATIVE VOLTAGE REGULATOR

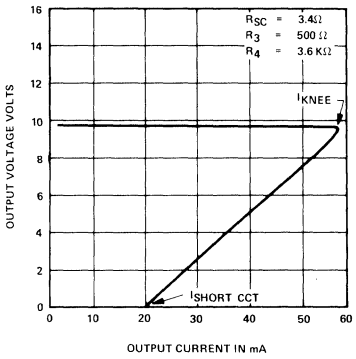


$$V_{out} = \left[\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1} \right]; \quad R_3 = R_4$$

TYPICAL APPLICATIONS (Cont'd)

FOLDBACK CURRENT LIMITING REGULATOR (V_{OUT} = 2 TO 7 VOLTS)





$$I_{KNEE} = \left[\frac{V_{out}\,R_3}{R_{SC}\,R_4} + \frac{V_{SENSE}\,(R_3 + R_4)}{R_{SC}\,R_4}\right]$$

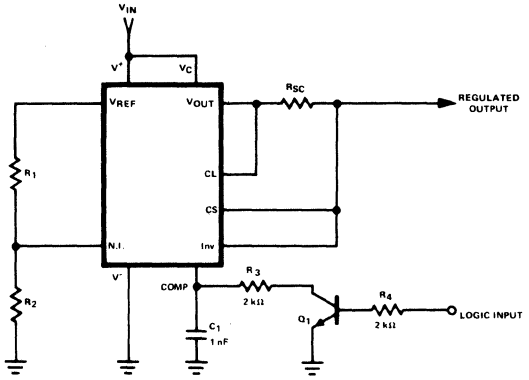
$$V_{out} = \left[V_{REF} \times \frac{R_1 + R_2}{R_2}\right]$$

$$I_{SHORT\ CKT} = \left[\frac{V_{SENSE}}{R_{SC}} \times \frac{R_3 + R_4}{R_4}\right]$$

$$\frac{R_4}{R_3} = \frac{V_{OUT}\ I_{SC}}{V_{SENSE}\ (I_{KNEE} - I_{SHORTCKT})} - 1$$

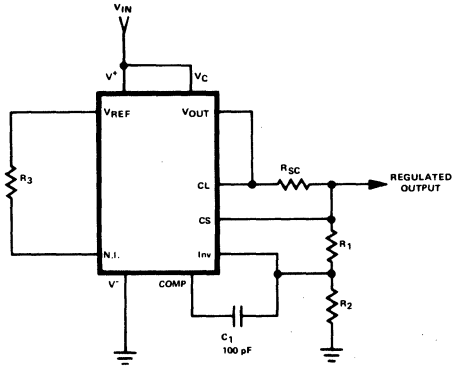
$$R_{SC} = \frac{V_{SENSE}}{I_{SC}}\left[1 + \frac{R_3}{R_4}\right]$$

REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING (V_{OUT} = 2 TO 7 VOLTS)



$$V_{out} = \left[V_{REF} \times \frac{R_2}{R_1 + R_2}\right]$$

HIGH VOLTAGE REGULATOR (V_{OUT} = 7 TO 37 VOLTS)



$$V_{out} = \left[V_{REF} \times \frac{R_1 + R_2}{R_2}\right]$$

$R_3 = \frac{R_1\,R_2}{R_1 + R_2}$ for minimum temperature drift

R_3 may be eliminated for minimum component count

μA78L02/5/6/8/12/15-DB,S

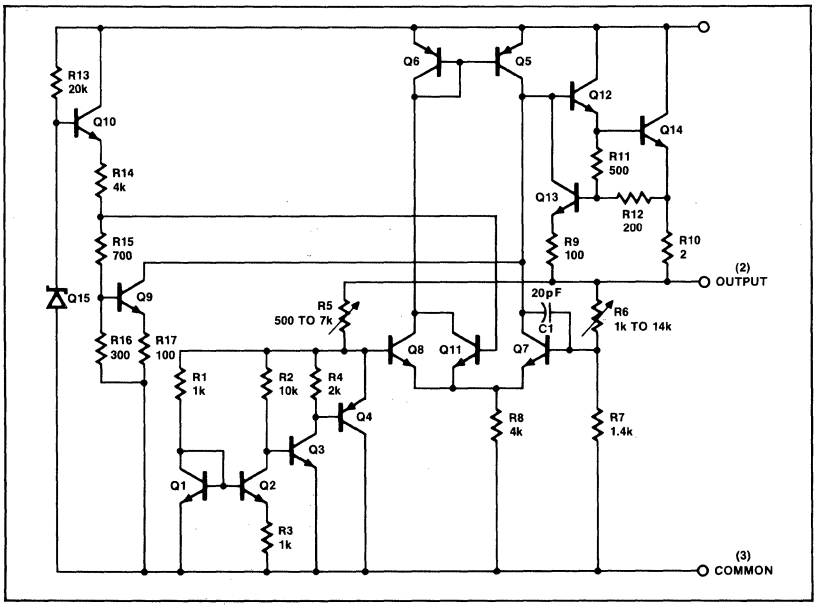
DESCRIPTION

The μA78L00 series of 3-Terminal Positive Voltage Regulators employ internal current limiting and thermal shutdown, making them essentially indestructible. If adequate heat sinking is provided, they can deliver up to 100mA output current. They are intended as fixed voltage regulators in a wide range of applications including local or on card regulation for elimination of noise and distribution problems associated with single point regulation. In addition, they can be used with power pass elements to make high current voltage regulators. The μA78L00 used as a Zener diode/resistor combination replacement, offers an effective output impedance improvement of typically two orders of magnitude, along with lower quiescent current and lower noise.

FEATURES

- **Output curent up to 100mA**
- **No external components**
- **Internal thermal overload protection**
- **Internal short circuit current limiting**
- **Available in JEDEC TO-92 and low profile TO-39 packages**
- **Output voltages of 2.6V, 5V, 6.2V, 8.2V, 12V and 15V**
- **Output voltage tolerances or ±5% (78L00-A) and ±10% (78L00) over the temperature range**

EQUIVALENT CIRCUIT

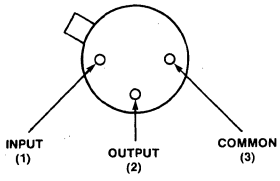


ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Input voltage		
2.6V, 5V, 6.2V and 8.2V	30	V
12V and 15V	35	V
Internal power dissipation	Internally limited	
Storage temperature range		
Metal can (TO-39 type)	-65 to +150	°C
Molded TO-92	-55 to +150	°C
Operating junction temperature range	0 to +150	°C
Lead temperatures		
Metal can (soldering, 60s time limit)	300	°C
Molded TO-92 (soldering, 10s time limit)	260	°C

CONNECTION DIAGRAMS

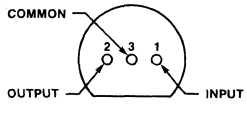
DB PACKAGE (TO-39)



ORDER INFORMATION

OUTPUT VOLTAGE	PART NO.
2.6V	78L02CDB
2.6V	78L02ACDB
5V	78L05CDB
5V	78L05ACDB
6V	78L06CDB
6V	78L06ACDB
8.2V	78L08CDB
8.2V	78L08ACDB
12V	78L12CDB
12V	78L12ACDB
15V	78L15CDB
15V	78L15ACDB

S PACKAGE (JEDEC TO-92)



ORDER INFORMATION

OUTPUT VOLTAGE	PART NO.
2.6V	78L02CS
2.6V	78L02ACS
5V	78L05CS
5V	78L05ACS
6V	78L06CS
6V	78L06ACS
8.2V	78L08CS
8.2V	78L08ACS
12V	78L12CS
12V	78L12ACS
15V	78L15CS
15V	78L15ACS

DC ELECTRICAL CHARACTERISTICS

I_{OUT} = 40mA, 0°C ≤ T_J ≤ +125°C, C_{IN} = 0.33μF, C_{OUT} = 0.1μF unless otherwise specified.

PARAMETER		TEST CONDITIONS	78L02AC			78L02C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage	T_J = 25°C		V_{IN} = 9.0V 2.6			V_{IN} = 9.0V 2.6		V
			2.5	4.75V ≤ V_{IN} ≤ 20V	2.7	2.4	4.75V ≤ V_{IN} ≤ 20V	2.8	
		1mA ≤ I_{OUT} ≤ 70mA	2.45		2.75	2.35		2.85	V
		1mA ≤ I_{OUT} ≤ 40mA	2.45		2.75	2.35		2.85	V
	Line regulation	T_J = 25°C		4.75 ≤ V_{IN} ≤ 20V 40	100		4.75V ≤ V_{IN} ≤ 20V 40	125	mV
				5V ≤ V_{IN} ≤ 20V 30	75		5V ≤ V_{IN} ≤ 20V 30	100	mV
	Load regulation	1mA ≤ I_{OUT} ≤ 100mA, T_J = 25°C		10	50		10	50	mV
		1mA ≤ I_{OUT} ≤ 40mA, T_J = 25°C		4.0	25		4.0	25	mW
I_{CC}		T_J = 25°C		3.6	6.0		3.6	6.0	mA
		T_J = 125°C			5.5			5.5	mA
ΔI_{CC}				5V ≤ V_{IN} ≤ 20V			5V ≤ V_{IN} ≤ 20V		
		With line			2.5			2.5	mA
		With load, 1mA ≤ I_{OUT} ≤ 40mA			0.1			0.2	mA
	Output noise voltage	T_J = 25°C, 10Hz ≤ f ≤ 100kHz		30			30		μV
	Long term stability			10			10		mV
	Ripple rejection	T_J = 25°C, f = 120Hz	43	6V ≤ V_{IN} ≤ 16V 51		42	6V ≤ V_{IN} ≤ 16V 51		dB
	Dropout voltage	T_A = 25°C		1.7			1.7		V
V_{OUT}	Output temperature drift	I_{OUT} = 5mA		-0.4			-0.4		mV/°C
I_{SC}		T_J = 25°C		140			140		mA

DC ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS	78L05AC			78L05C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage	T_J = 25°C		V_{IN} = 10V 5.0			V_{IN} = 10V 5.0		V
			4.8	7V ≤ V_{IN} ≤ 20V	5.2	4.6	7V ≤ V_{IN} ≤ 20V	5.4	
		1mA ≤ I_{OUT} ≤ 70mA	4.75		5.25	4.50		5.50	V
		1mA ≤ I_{OUT} ≤ 40mA	4.75		5.25	4.50		5.50	V
	Line regulation	T_J = 25°C		7V ≤ V_{IN} ≤ 20V 55	150		7V ≤ V_{IN} ≤ 20V 55	200	mV
				8V ≤ V_{IN} ≤ 20V 45	100		8V ≤ V_{IN} ≤ 20V 45	150	mV
	Load regulation	1mA ≤ I_{OUT} ≤ 100mA, T_J = 25°C		11	60		11	60	mV
		1mA ≤ I_{OUT} ≤ 40mA, T_J = 25°C		5.0	30		5.0	30	mW
I_{CC}		T_J = 25°C		3.8	6.0		3.8	6.0	mA
		T_J = 125°C			5.5			5.5	mA
ΔI_{CC}				8V ≤ V_{IN} ≤ 20V			8V ≤ V_{IN} ≤ 20V		
		With line			1.5			1.5	mA
		With load, 1mA ≤ I_{OUT} ≤ 40mA			0.1			0.2	mA
	Output noise voltage	T_J = 25°C, 10Hz ≤ f ≤ 100kHz		40			40		μV
	Long term stability			12			12		mV
	Ripple rejection	T_J = 25°C, f = 120Hz	41	8V ≤ V_{IN} ≤ 18V 49		40	8V ≤ V_{IN} ≤ 18V 49		dB
	Dropout voltage	T_A = 25°C		1.7			1.7		V
V_{OUT}	Output temperature drift	I_{OUT} = 5mA		-0.65			-0.65		mV/°C
I_{SC}		T_J = 25°C		140			140		mA

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 40mA, 0°C ≤ T_J ≤ +125°C, C_{IN} = 0.33μF, C_{OUT} = 0.1μF unless otherwise specified.

PARAMETER	TEST CONDITIONS	78L06AC			78L06C			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OUT} Output voltage			V_{IN} = 12V			V_{IN} = 12V		
	T_J = 25°C	5.95	6.2	6.45	5.7	6.2	6.7	V
			8.5V ≤ V_{IN} ≤ 20V			8.5V ≤ V_{IN} ≤ 20V		
	1mA ≤ I_{OUT} ≤ 70mA	5.90		6.50	5.60		6.80	V
	1mA ≤ I_{OUT} ≤ 40mA	5.90		6.50	5.6		6.8	V
Line regulation	T_J = 25°C		8.5V ≤ V_{IN} ≤ 20V			8.5V ≤ V_{IN} ≤ 20V		
			65	175		65	200	mV
			9V ≤ V_{IN} ≤ 20V			9V ≤ V_{IN} ≤ 20V		
			55	125		55	150	mV
Load regulation	1mA ≤ I_{OUT} ≤ 100mA, T_J = 25°C		13	80		13	80	mV
	1mA ≤ I_{OUT} ≤ 40mA, T_J = 25°C		6.0	40		6.0	40	mV
I_{CC}	T_J = 25°C		3.9	6.0		3.9	6.0	mV
	T_J = 125°C			5.5			5.5	mA
ΔI_{CC}			9.0V ≤ V_{IN} ≤ 20V			9.0V ≤ V_{IN} ≤ 20V		
	With line			1.5			1.5	mA
	With load, 1mA ≤ I_{OUT} ≤ 40mA			0.1			0.2	mA
Output noise voltage	T_J = 25°C, 10Hz ≤ f ≤ 100kHz		50			50		μA
Long term stability			14			14		mV
Ripple rejection	T_J = 25°C, f = 120Hz		10V ≤ V_{IN} ≤ 20V			10V ≤ V_{IN} ≤ 20V		
		40	46		39	46		dB
Dropout voltage	T_A = 25°C		1.7			1.7		V
V_{OUT} Output temperature drift	I_{OUT} = 5mA		-0.75			-0.75		mV/°C
I_{SC}	T_J = 25°C		140			140		mA

DC ELECTRICAL CHARACTERISTICS

(Cont'd)

PARAMETER	TEST CONDITIONS	78L08AC			78L08C			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OUT} Output voltage			V_{IN} = 14V			V_{IN} = 14V		
	T_J = 25°C	7.87	8.2	8.53	7.54	8.20	8.86	V
			11V ≤ V_{IN} ≤ 23V			11V ≤ V_{IN} ≤ 23V		
	1mA ≤ I_{OUT} ≤ 70mA	7.8		8.60	7.40		9.0	V
	1mA ≤ I_{OUT} ≤ 40mA	7.8		8.6	7.40		9.0	V
Line regulation	T_J = 25°C		11V ≤ V_{IN} ≤ 23V			11V ≤ V_{IN} ≤ 23V		
			80	175		80	200	mV
			12V ≤ V_{IN} ≤ 23V			12V ≤ V_{IN} ≤ 23V		
			70	125		70	150	mV
Load regulation	1mA ≤ I_{OUT} ≤ 100mA, T_J = 25°C		15	80		20	90	mV
	1mA ≤ I_{OUT} ≤ 40mA, T_J = 25°C		8.0	40		10	45	mV
I_{CC}	T_J = 25°C		3.9	6.0		4.2	6.5	mV
	T_J = 125°C			5.5			6.0	mA
ΔI_{CC}			12V ≤ V_{IN} ≤ 23V			12V ≤ V_{IN} ≤ 23V		
	With line			1.5			1.5	mA
	With load, 1mA ≤ I_{OUT} ≤ 40mA			0.1			0.2	mA
Output noise voltage	T_J = 25°C, 10Hz ≤ f ≤ 100kHz		60			60		μA
Long term stability			19			19		mV
Ripple rejection	T_J = 25°C, f = 120Hz		12V ≤ V_{IN} ≤ 22V			12V ≤ V_{IN} ≤ 22V		
		39	45		38	49		dB
Dropout voltage	T_A = 25°C		1.7			1.7		V
V_{OUT} Output temperature drift	I_{OUT} = 5mA		-0.8			-0.8		mV/°C
I_{SC}	T_J = 25°C		140			140		mA

DC ELECTRICAL CHARACTERISTICS (Cont'd) I_{OUT} = 40mA, 0°C ≤ T_J ≤ +125°C, C_{IN} = 0.33μF, C_{OUT} = 0.1μF unless otherwise specified.

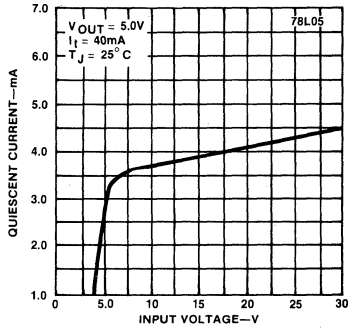
PARAMETER		TEST CONDITIONS	78L12AC			78L12C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage	T_J = 25°C		V_{IN} = 19V 12			V_{IN} = 19V 12		
			11.5		12.5	11.1		12.9	V
				14.5V ≤ V_{IN} ≤ 27V			14.5V ≤ V_{IN} ≤ 27V		
		1mA ≤ I_{OUT} ≤ 70mA	11.4		12.6	10.8		13.2	V
		1mA ≤ I_{OUT} ≤ 40mA	11.4		12.6	10.8		13.2	V
	Line regulation	T_J = 25°C		14.5V ≤ V_{IN} ≤ 27V 120	250		14.5V ≤ V_{IN} ≤ 27V 120	250	mV
				16V ≤ V_{IN} ≤ 27V			16V ≤ V_{IN} ≤ 27V		
				100	200		100	200	mV
	Load regulation	1mA ≤ I_{OUT} ≤ 100mA, T_J = 25°C		20	100		20	100	mV
		1mA ≤ I_{OUT} ≤ 40mA, T_J = 25°C		10	50		10	50	mV
I_{CC}		T_J = 25°C		4.2	6.5		4.2	6.5	mA
		T_J = 125°C			6.0			6.0	mA
ΔI_{CC}				16V ≤ V_{IN} ≤ 27V			16V ≤ V_{IN} ≤ 27V		
		With line			1.5			1.5	mA
		With load, 1mA ≤ I_{OUT} ≤ 40mA			0.1			0.2	mA
	Output noise voltage	T_J = 25°C, 10Hz ≤ f ≤ 100kHz		80			80		μA
	Long term stability			24			24		mV
				15V ≤ V_{IN} ≤ 25V			15V ≤ V_{IN} ≤ 25V		
	Ripple rejection	T_J = 25°C, f = 120Hz	37	42		36	42		dB
	Dropout voltage	T_A = 25°C		1.7			1.7		V
V_{OUT}	Output temperature drift	I_{OUT} = 5mA		-1.0			-1.0		mV/°C
I_{SC}		T_J = 25°C		140			140		mA

DC ELECTRICAL CHARACTERISTICS (Cont'd)

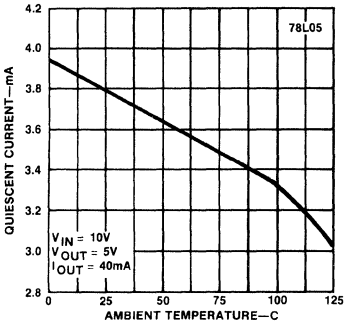
PARAMETER		TEST CONDITIONS	78L15AC			78L15C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage	T_J = 25°C		V_{IN} = 23V 15			V_{IN} = 23V 15		
			14.4		15.6	13.8		16.2	V
				17.5V ≤ V_{IN} ≤ 30V			17.5V ≤ V_{IN} ≤ 30V		
		1mA ≤ I_{OUT} ≤ 70mA	14.25		15.75	13.5		16.5	V
		1mA ≤ I_{OUT} ≤ 40mA	14.25		15.75	13.5		16.5	V
	Line regulation	T_J = 25°C		17.5V ≤ V_{IN} ≤ 30V 130	300		17.5V ≤ V_{IN} ≤ 30V 130	300	mV
				20V ≤ V_{IN} ≤ 30V			20V ≤ V_{IN} ≤ 30V		
				110	250		110	250	mV
	Load regulation	1mA ≤ I_{OUT} ≤ 100mA, T_J = 25°C		25	150		25	150	mV
		1mA ≤ I_{OUT} ≤ 40mA, T_J = 25°C		12	75		12	75	mV
I_{CC}		T_J = 25°C		4.4	6.5		4.4	6.5	mA
		T_J = 125°C			6.0			6.0	mA
ΔI_{CC}				20V ≤ V_{IN} ≤ 30V			20V ≤ V_{IN} ≤ 30V		
		With line			1.5			1.5	mA
		With load, 1mA ≤ I_{OUT} ≤ 40mA			0.1			0.2	mA
	Output noise voltage	T_J = 25°C, 10Hz ≤ f ≤ 100kHz		90			90		μV
	Long term stability			30			30		mV
				18.5V ≤ V_{IN} ≤ 28.5V			18.5V ≤ V_{IN} ≤ 28.5V		
	Ripple rejection	T_J = 25°C, f = 120Hz	34	39		33	39		dB
	Dropout voltage	T_A = 25°C		1.7			1.7		V
V_{OUT}	Output temperature drift	I_{OUT} = 5mA		-1.3			-1.3		mV/°C
I_{SC}		T_J = 25°C		140			140		mA

TYPICAL PERFORMANCE CHARACTERISTICS

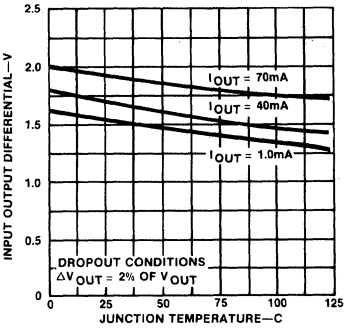
QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



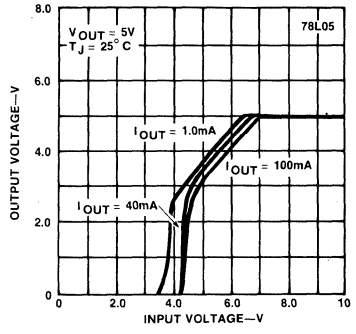
QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



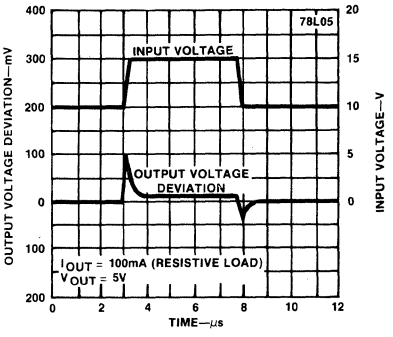
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



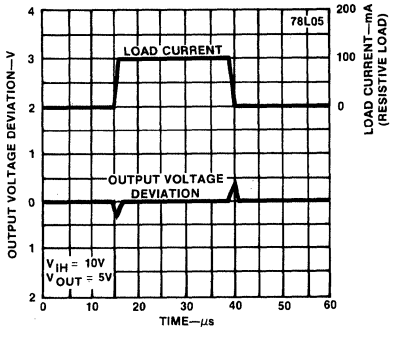
DROPOUT CHARACTERISTICS



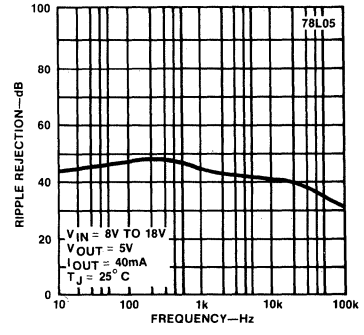
LINE TRANSIENT RESPONSE



LOAD TRANSIENT RESPONSE



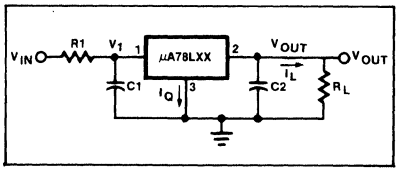
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



NOTE

Other μA78L00 Series Devices have similar curves.

HIGH DISSIPATION APPLICATION



When it is necessary to operate a μA78L00 regulator with a large input-output differential voltage, the addition of series resistor R1 will extend the output current range of the device by sharing the total dissipation between R1 and the regulator.

R1 may be calculated from

$$R1 = \frac{V_{IN(MIN)} - V_{OUT} - 2.0V}{I_{L(MAX)} + I_Q}$$

where IQ is the regulator quiescent current.

Regulator power dissipation at maximum input voltage and maximum load current is now

$$P_{D(MAX)} = (V_1 - V_{OUT})\, I_{L(MAX)} + V_1\, I_Q$$

where

$$V_1 = V_{IN(MAX)} - (I_{L(MAX)} + I_Q)\, R1$$

The presence of R1 will affect load regulation according to the equation:

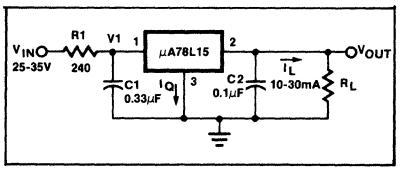
load regulation (at constant V_{IN}) = load regulation (at constant V_1) + (line regulation, mV per V) X (R1) X (ΔI_L).

As an example, consider a 15V regulator with a supply voltage of 30 ± 5V, required to supply a maximum load current of 30mA. IQ is 4.3mA, and minimum load current is to be 10mA.

$$R1 = \frac{25 - 15 - 2}{30 + 4.3} \quad \frac{8}{34.3} = 240\Omega$$

$$V_1 = 35 - (30 + 4.3)\ .24 = 35 - 8.2 = 26.8V$$

$$P_{D(MAX)} = (26.8 - 15)\ 30 + 26.8\ (4.3)$$
$$= 354 + 115$$
$$= 470mW,$$ which will permit operation up to 70°C in most applications.



Line regulation of this circuit is typically 110mV for an input range of 25-35V at a constant load current, i.e. 11mV/V.

Load regulation = constant V_1 load regulation (typically 10mV, 10-30mA I_L) + (11mV/V) X 0.24 X 20mA (typically 53mV)
= 63mV for a load current change of 20mA at a constant V_{IN} of 30V.

THERMAL CONSIDERATIONS

The TO-92 molded package is capable of unusually high power dissipation due to the lead frame design. However, its thermal capabilities are generally overlooked because of a lack of understanding of the thermal paths from the semiconductor junction to ambient temperature. While thermal resistance is normally specified for the device mounted 1cm above an infinite heat sink, very little has been mentioned of the options available to improve on the conservatively rated thermal capability.

An explanation of the thermal paths of the TO-92 and comparison of the thermal equivalent circuit of the TO-39 metal package with that of the TO-92 will allow the designer to determine the thermal stress he is applying in any give application.

THE METAL CAN THERMAL MODEL

In the TO-39 case, where the die is attached directly to the base of a metal package, the thermal equivalent circuit is often represented simply as a series connection of the junction-to-case thermal resistance, θ_{JC}, and the case-to-ambient thermal resistance, θ_{CA}, as shown in Figure 1.

In this model, the current source represents the thermal energy source; TJ is the junction temperature, assuming a constant surface temperature across the die; θ_{JC} is the junction-to-case thermal resistance, measured at a point on the case directly beneath the die location; θ_{CA} is the thermal resistance from the case to the ultimate heat sink, ambient temperature, as represented by the battery. The heat flow is analogous to electrical current, and temperature to voltage. The total thermal resistance from junction to ambient is then:

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

The maximum power dissipation is a function of the maximum permissible junction temperature (which is a function of the package materials and construction) and the total thermal resistance from the junction to ambient temperature. Junction temperature is assumed to the limiting factor.

Thus: maximum power dissipation

$$P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JC} + \theta_{CA}}$$

Since $\theta_{JA} = \theta_{JC} + \theta_{CA}$

then $$\theta_{JA} = \frac{T_{J(MAX)} - T_A}{P_D}$$

or $$\theta_{JA}\, P_D = T_J - T_A$$

$$P_D = \frac{T_J - T_A}{\theta_{JA}}$$

Therefore, using the V_{BE} method of junction temperature sensing, and attaching a thermocouple to the case at the location specified, the relative values of θ_{JC}, and θ_{CA} can readily be determined.

The thermal ratings of the metal can package are normally presented with the case attached to an infinite heat sink at still air ambient temperature. This causes θ_{CA} to go to zero resulting in θ_{JC} representing the total θ_{JA}. The infinite heat sink is an unrealizable condition in the practical world, but serves to project a goal.

THE TO-92 PACKAGE

The TO-92 package thermal paths are considerably more complex than those of the TO-39 metal can package. In addition to the path through the molding compound to ambient temperature, there is another path through the leads in parallel with the case path, to ambient temperature, as shown in Figure 2.

The total thermal resistance in this model is then:

$$\theta_{JA} = \frac{(\theta_{JC} + \theta_{CA})\ (\theta_{JL} + \theta_{LA})}{\theta_{JC} + \theta_{CA} + \theta_{JL}\ \theta_{LA}}$$

Where:
- θ_{JC} = thermal resistance of the case between the regulator die and a point on the case directly above the die location.
- θ_{CA} = thermal resistance between the case and air at ambient temperature.
- θ_{JL} = thermal resistance from transistor die through the collector lead to a point $1/16$" below the regulator case.
- θ_{LA} = total thermal resistance of the collector-base-emitter leads to ambient temperature.

As one can see from Figure 1, the metal can package generally does not have the lead cooling path because of the high thermal resistances resulting from the construction of the header, case and leads. Normally, this material is kovar. Now, θ_{JC} and θ_{JL} are within the package and not variable by the user. However, θ_{CA} and θ_{LA} are outside the package and can be effectively used to control the total thermal resistance and, therefore, junction temperature.

Replacing θ_{JA} of equation (1) with θ_{JA} equation (3) gives:

$$\theta_{JA} = \frac{(\theta_{JC} + \theta_{CA})(\theta_{JL} \alpha \theta_{LA})}{\theta_{JC} + \theta_{CA} + \theta_{JL} + \theta_{LA}} = \frac{T_J - T_A}{P_D}$$

The maximum T_J allowed in equation (4) is 150°C. The maximum power dissipation is determined by the net total thermal resistance θ_{JA}, the parallel equivalent networks of the case series path and lead series path, divided into the difference of the maximum junction temperature, 150°C, and ambient temperature generally specified as 25°C. In the case of the 78LXX, the maximum dissipation of a .4 inch condition is:

$$P_D = \frac{150 - 25}{\theta_{JA}}, \theta_{JA} = 180°C/W$$

$$P_D = 0.7W$$

If lead length is reduced to .125 inch θ_{JA} becomes 160°C, and $P_D(MAX) = 0.78W$.

METHODS OF HEAT SINKING

With two external thermal resistances in each leg of a parallel network available to the circuit designer as variables, he can choose the method of heat sinking most applicable to his particular situation. To demonstrate, consider the effect of placing a small 72°C/W flag type heat sink, such as the Staver F1-7D-2, on the 78LXX molded case. The heat sink effectively replaces the θ_{CA} (Figure 2) and the new thermal resistance, θ_{JA}, is:

θ_{JA} = 145°C/W (assuming .125 inch lead length)

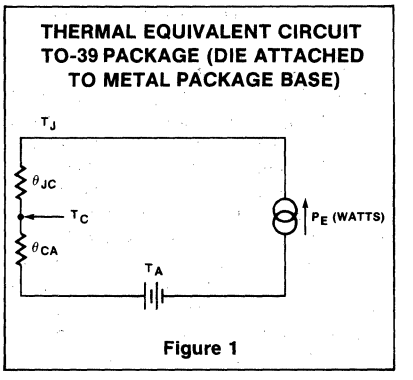


Figure 1

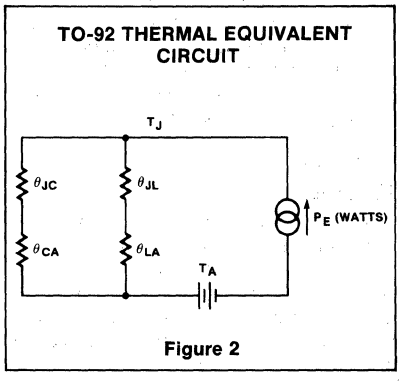


Figure 2

The net change of 15°C/W increases the allowable power dissipation to 0.86W with an inserted cost of 1-2 cents. A still further decrease in θ_{JA} could be achieved by using a sink rated at 46°C/W, such as the Staver FS-7A. Also, if the case sinking does not provide an adequate reduction in total θ_{JA}, the other external thermal resistance, θ_{LA}, may be reduced by shortening the lead length from package base to mounting medium. However, one point must be kept in mind. The lead thermal path includes a thermal resistance, θ_{SA}, from the leads at the mounting point to ambient, that is, the mounting medium, θ_{LA} is then equal to $\theta_{LS} + \theta_{SA}$. The new model is shown in Figure 3.

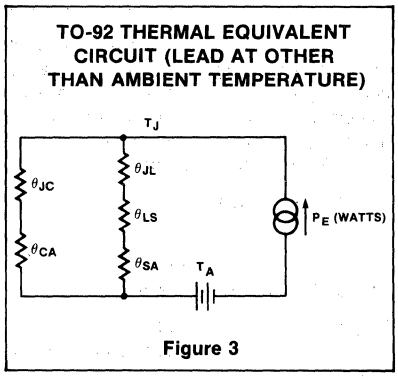


Figure 3

In the case of a socket, θ_{SA} could be as high as 270°C/W, thus causing a net increase in θ_{JA} and a consequent decrease in the maximum dissipation capability. Shortening the lead length may return the net θ_{JA} to the original value, but lead sinking would not be accomplished.

In those cases where the regulator is inserted into a copper clad printed circuit board, it is advantageous to have a maximum area of copper at the entry points of the leads. While it would be desirable to rigorously define the effect of PC board copper, the real world variables are too great to allow anything more than a few general observations.

The best analogy for PC board copper is to compare it with parallel resistors. Beyond some point, additonal resistors are not significantly effective; beyond some point, additional copper area is not effective.

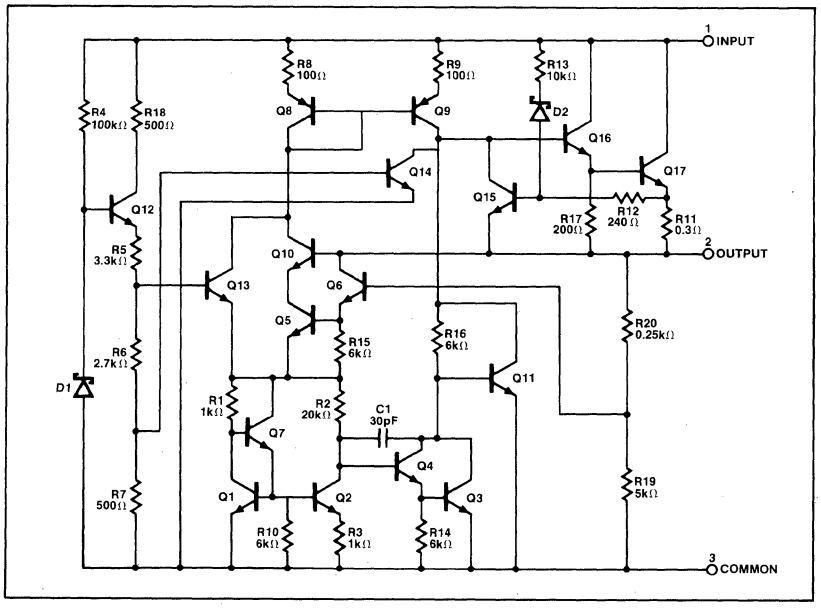
DESCRIPTION

The 78M00 series of monolithic Three Terminal Positive Voltage Regulators employs internal current limiting, thermal shut down, and safe-area compensation making them essentially indestructible. If adequate heat sinking is provided, the device can deliver over 500mA output current. They are intended as fixed voltage regulators, but used with external components, can provide adjustable output voltages and currents.

FEATURES

- **Output current up to 500mA**
- **No external components**
- **Internal thermal overload protection**
- **Internal short circuit current limiting**
- **Output transistor safe-area compensation**
- **Available in the TO-220 and the TO-39 package**
- **Output voltages of 5,6,8,12,15,20, and 24 volts**

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

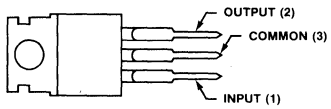
PARAMETER	RATING	UNIT
Input voltage (5V through 15V) (20V, 24V)[1]	35	V
Internal power dissipation	40	V
Storage temperature range	Internally limited	
TO-39	-65 to +150	°C
TO-220	-55 to +125	°C
Operating junction temperature range[2]		
78M00	-55 to +150	°C
SA78M00C	-40 to +125	°C
78M00C	0 to +125	°C
Lead temperature		
TO-39 package (soldering, 60 second time limit)	300	°C
TO-220 package (soldering, 10 second time limit)	230	°C

NOTES

1. Thermal resistance of the packages (without a heat sink)
   Junction to case: TO-220 package 2°C/W TO-39 package 20°C/W.
   Junction to ambient: TO-220 package 50°C/W TO-39 package 170C/W.
2. Operating ambient temperature range
   78M00 -55°C to +125°C
   SA78M00C -40°C to -125°C
   78M00C 0°C to +85°C

PIN CONFIGURATIONS

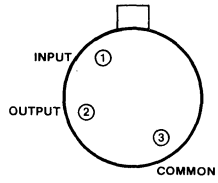
U PACKAGE (TO-220)



ORDER INFORMATION

OUTPUT VOLTAGE	ORDER PART NO.
5V	78M05CU/SA78M05CU
6V	78M06CU/SA78M06CU
8V	78M08CU/SA78M08CU
12V	78M12CU/SA78M12CU
15V	78M15CU/SA78M15CU
20V	78M20CU/SA78M20CU
24V	78M24CU/SA78M24CU

DB PACKAGE (TO-39)



OUTPUT VOLTAGE	ORDER PART NO.
5V	78M05DB
6V	78M06DB
8V	78M08DB
12V	78M12DB
15V	78M15DB
20V	78M20DB
24V	78M24DB
5V	78M05CDB
6V	78M06CDB
8V	78M08CDB
12V	78M12CDB
15V	78M15CDB
20V	78M20CDB
24V	78M24CDB

DC ELECTRICAL CHARACTERISTICS

I_{OUT} = 350mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	78M05[1]			78M05C[1]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 10V			V_{IN} = 10V		
			4.8	5.0	5.2	4.8	5.0	5.2	V
		Over temp.[1], 5mA ≤ I_{OUT} ≤ 350mA		8V ≤ V_{IN} ≤ 20V			7V ≤ V_{IN} ≤ 20V		
			4.7		5.3	4.75		5.25	V
	Line regulation	I_{OUT} = 200mA		7V ≤ V_{IN} ≤ 25V			7V ≤ V_{IN} ≤ 25V		
				3	50		3	100	mV
				8V ≤ V_{IN} ≤ 20V			8V ≤ V_{IN} ≤ 25V		
				1	25		1	50	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 500mA		20	50		20	100	mV
		5mA ≤ I_{OUT} ≤ 200mA		10	25		10	50	mV
I_{CC}				4.5	6.0		4.5	6.0	mA
ΔI_{CC}	With line	Over temp.[1], I_{OUT} = 200mA		8V ≤ V_{IN} ≤ 25V			8V ≤ V_{IN} ≤ 25V		
					0.8			0.8	mA
ΔI_{CC}	With load	5mA ≤ I_{OUT} ≤ 350mA			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz, T_A = 25°C		40			40		μV
	Voltage drift	mV/1000hrs.			20			20	mV
	Ripple rejection	Over temp.[1], f = 120Hz		8V ≤ V_{IN} ≤ 18V					
			68	80		62	80		dB
	Dropout voltage			2.0			2.0		V
I_{SC}		V_{IN} = 35V		300			300		mA
	Peak output current			700			700		mA
V_{OUT}	Output temperature drift	I_{OUT} = 5mA	0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C			
				-1.0			-1.0		mV/°C

DC ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS	78M06[1]			78M06C[1]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 11V			V_{IN} = 11V		
			5.75	6.0	6.25	5.75	6.0	6.25	V
		Over temp.[1], 5mA ≤ I_{OUT} ≤ 350mA		9V ≤ V_{IN} ≤ 21V			8.0V ≤ V_{IN} ≤ 21V		
			5.7		6.3	5.7		6.3	V
	Line regulation	I_{OUT} = 200mA		8V ≤ V_{IN} ≤ 25V			8V ≤ V_{IN} ≤ 25V		
				5	60		5	100	mV
				9V ≤ V_{IN} ≤ 20V			9V ≤ V_{IN} ≤ 25V		
				1.5	30		1.5	50	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 500mA		20	60		20	120	mV
		5mA ≤ I_{OUT} ≤ 200mA		10	30		10	60	mV
I_{CC}				4.5	6.0		4.5	8.0	mA
ΔI_{CC}	With line	Over temp.[1], I_{OUT} = 200mA		9V ≤ V_{IN} ≤ 25V			9V ≤ V_{IN} ≤ 25V		
					0.8			0.8	mA
ΔI_{CC}	With load	5mA ≤ I_{OUT} ≤ 350mA			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz, T_A = 25°C		45			45		μV
	Voltage drift	mV/1000hrs.			24			24	mV
	Ripple rejection	Over temp.[1], f = 120Hz		9V ≤ V_{IN} ≤ 19V			9V ≤ V_{IN} ≤ 19V		
			59	80		59	80		dB
	Dropout voltage			2.0			2.0		V
I_{SC}		V_{IN} = 35V		270			270		mA
	Peak output current			700			700		mA
V_{OUT}	Output temperature drift	I_{OUT} = 5mA	0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C			
				-0.5			-0.5		mV/°C

DC ELECTRICAL CHARACTERISTICS (Cont'd) I_{OUT} = 350mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	78M08[1]			78M08C[1]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 14V			V_{IN} = 14V		
			7.7	8.0	8.3	7.7	8.0	8.3	V
		Over temp.[1], 5mA ≤ I_{OUT} ≤ 350mA		11.5V ≤ V_{IN} ≤ 23V			10.5V ≤ V_{IN} ≤ 23V		
			7.6		8.4	7.6		8.4	V
	Line regulation	I_{OUT} = 200mA		10.5V ≤ V_{IN} ≤ 25V			10.5V ≤ V_{IN} ≤ 25V		
				6	60		6	100	mV
				11V ≤ V_{IN} ≤ 20V			11V ≤ V_{IN} ≤ 25V		
				2	30		2	50	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 500mA		25	80		25	160	mV
		5mA ≤ I_{OUT} ≤ 200mA		10	40		10	80	mV
I_{CC}				4.6	6.0		4.6	6.0	mA
ΔI_{CC}	With line	Over temp.[1], I_{OUT} = 200mA		11.5V ≤ V_{IN} ≤ 25V			10.5V ≤ V_{IN} ≤ 25V		
					0.8			0.8	mA
ΔI_{CC}	With load	5mA ≤ I_{OUT} ≤ 350mA			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz, T_A = 25°C		52			52		μV
	Voltage drift	mV/1000hrs.			32			32	mV
	Ripple rejection	Over temp.[1], f = 120Hz		11.5V ≤ V_{IN} ≤ 21.5V			11.5V ≤ V_{IN} ≤ 21.5V		
			56	80		56	80		dB
	Dropout voltage			2.0			2.0		V
I_{SC}		V_{IN} = 35V		250			250		mA
	Peak output current			700			700		mA
V_{OUT}	Output temperature drift	I_{OUT} = 5mA		0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C		
				-0.5			-0.5		mV/°C

DC ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS	78M12[1]			78M12C[1]			78M15[1]			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 19V			V_{IN} = 19V			V_{IN} = 23V		
			11.5	12.0	12.5	11.5	12.0	12.5	14.4	15.0	15.6	V
		Over temp.[1], 5mA ≤ I_{OUT} ≤ 350mA		15.5V ≤ V_{IN} ≤ 27V		14.5V ≤ V_{IN} ≤ 27V			18.5V ≤ V_{IN} ≤ 30V			
			11.4		12.6	11.4		12.6	14.5		15.75	V
	Line regulation	I_{OUT} = 200mA		14.5V ≤ V_{IN} ≤ 30V		14.5V ≤ V_{IN} ≤ 30V			17.5V ≤ V_{IN} ≤ 30V			
				8	60		8	100		10	60	mV
				16V ≤ V_{IN} ≤ 25V		16V ≤ V_{IN} ≤ 30V			20V ≤ V_{IN} ≤ 30V			
				2	30		2	50		3	30	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 500mA		25	120		25	240		25	150	mV
		5mA ≤ I_{OUT} ≤ 200mA		10	60		10	120		10	75	mV
I_{CC}				4.8	6.0		4.8	6.0		4.8	6.0	mA
ΔI_{CC}	With line	Over temp.[1], I_{OUT} = 200mA		15V ≤ V_{IN} ≤ 30V			14.5V ≤ V_{IN} ≤ 30V			18.5V ≤ V_{IN} ≤ 30V		
					0.8			0.8			0.8	mA
ΔI_{CC}	With load	5mA ≤ I_{OUT} ≤ 350mA			0.5			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz, T_A = 25°C		75			75			90		μV
	Voltage drift	mV/1000hrs.			48			48			60	mV
	Ripple rejection	Over temp.[1], f = 120Hz		15V ≤ V_{IN} ≤ 25V			15V ≤ V_{IN} ≤ 25V			18.5V ≤ V_{IN} ≤ 28.5V		
			55	80		55	80		54	70		dB
	Dropout voltage			2.0			2.0			2.0		V
I_{SC}		V_{IN} = 35V		240			240			240		mA
	Peak output current			700			700			700		mA
V_{OUT}	Output temperature drift	I_{OUT} = 5mA		0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C			0°C ≤ T_J ≤ 150°C		
				-1.0			-1.0			-1.0		mV/°C

DC ELECTRICAL CHARACTERISTICS (Cont'd) I_{OUT} = 350mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	78M15C[1]			78M20[1]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 23V			V_{IN} = 29V		
			14.4	15.0	15.6	19.2	20	20.8	V
		Over temp.[1], 5mA ≤ I_{OUT} ≤ 350mA		17.5V ≤ V_{IN} ≤ 30V			24V ≤ V_{IN} ≤ 35V		
			14.25		15.75	19		21	V
	Line regulation	I_{OUT} = 200mA		17.5V ≤ V_{IN} ≤ 30V			23V ≤ V_{IN} ≤ 35V		
				10	100		10	60	mV
				20V ≤ V_{IN} ≤ 30V			24V ≤ V_{IN} ≤ 35V		
				3	50		5	30	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 500mA		25	150		30	200	mV
		5mA ≤ I_{OUT} ≤ 200mA		10	75		10	100	mV
I_{CC}				4.8	6.0		4.9	6.0	mA
ΔI_{CC}	With line	Over temp.[1], I_{OUT} = 200mA		17.5V ≤ V_{IN} ≤ 30V			24V ≤ V_{IN} ≤ 35V		
					0.8			0.8	mA
ΔI_{CC}	With load	5mA ≤ I_{OUT} ≤ 350mA			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz, T_A = 25°C		90			110		μV
	Voltage drift	mV/1000hrs.			60			80	mV
	Ripple rejection	Over temp.[1], f = 120Hz		18.5V ≤ V_{IN} ≤ 28.5V			24V ≤ V_{IN} ≤ 34V		
			54	70		53	70		dB
	Dropout voltage			2.0			2.0		V
I_{SC}		V_{IN} = 35V		240			240		mA
	Peak output current			700			700		mA
V_{OUT}	Output temperature drift	I_{OUT} = 5mA		0°C ≤ T_J ≤ 125°C			0°C ≤ T_J ≤ 150°C		
				-1.0			-1.1		mV/°C

DC ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS	78M20C[1]			78M24[1]			78M24C[1]			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 29V			V_{IN} = 33V			V_{IN} = 33V		
			19.2	20	20.8	23.0	24.0	25.0	23.0	24.0	25.0	V
		Over temp.[1], 5mA ≤ I_{OUT} ≤ 350mA		23V ≤ V_{IN} ≤ 35V			28V ≤ V_{IN} ≤ 38V			27V ≤ V_{IN} ≤ 38V		
			19		21	22.8		25.2	22.8		25.2	V
	Line regulation	I_{OUT} = 200mA		23V ≤ V_{IN} ≤ 35V			27V ≤ V_{IN} ≤ 38V			27V ≤ V_{IN} ≤ 38V		
				10	100		10	60		10	100	mV
				24V ≤ V_{IN} ≤ 35V			30V ≤ V_{IN} ≤ 36V			28V ≤ V_{IN} ≤ 38V		
				5	50		5	30		5	50	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 500mA		30	400		30	240		30	480	mV
		5mA ≤ I_{OUT} ≤ 200mA		10	200		10	120		10	240	mV
I_{CC}				4.9	6.0		5	6.0		5	6.0	mA
ΔI_{CC}	With line	Over temp.[1], I_{OUT} = 200mA		23V ≤ V_{IN} ≤ 35V			28V ≤ V_{IN} ≤ 38V			27V ≤ V_{IN} ≤ 38V		
					0.8			0.8			0.8	mA
ΔI_{CC}	With load	5mA ≤ I_{OUT} ≤ 350mA			0.5			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz, T_A = 25°C		110			170			170		μV
	Voltage drift	mV/1000hrs.			80			96			96	mV
	Ripple rejection	Over temp.[1], f = 120Hz		24V ≤ V_{IN} ≤ 34V			28V ≤ V_{IN} ≤ 38V			28V ≤ V_{IN} ≤ 38V		
			53	70		50	70		50	70		dB
	Dropout voltage			2.0			2.0			2.0		V
I_{SC}		V_{IN} = 35V		240			240			240		mA
	Peak output current			700			700			700		mA
V_{OUT}	Output temperature drift	I_{OUT} = 5mA	0°C ≤ T_J ≤ 125°C			0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C			
				-1.1			-1.2			-1.2		mV/°C

DC ELECTRICAL CHARACTERISTICS (Cont'd) I_{OUT} = 350mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	SA78M05C[2]			SA78M06C[2]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 10V			V_{IN} = 11V		
			4.8	5.0	5.2	5.75	6.0	6.25	V
		Over temp.[2], 5mA ≤ I_{OUT} ≤ 350mA		7V ≤ V_{IN} ≤ 25V			8.0V ≤ V_{IN} ≤ 21V		
			4.7		5.3	5.7		6.3	V
	Line regulation	I_{OUT} = 200mA		7V ≤ V_{IN} ≤ 25V			8V ≤ V_{IN} ≤ 25V		
				3	100		5	100	mV
				8V ≤ V_{IN} ≤ 25V			9V ≤ V_{IN} ≤ 25V		
				1	50		1.5	50	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 500mA		20	100		20	120	mV
		5mA ≤ I_{OUT} ≤ 200mA		10	50		10	60	mV
I_{CC}				4.5	6.0		4.5	8.0	mA
ΔI_{CC}	With line	Over temp.[2], I_{OUT} = 200mA		8V ≤ V_{IN} ≤ 25V			9V ≤ V_{IN} ≤ 25V		
				0.6			0.6		mA
ΔI_{CC}	With load	5mA ≤ I_{OUT} ≤ 350mA		0.3			0.3		mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz, T_A = 25°C		40			45		μV
	Voltage drift	mV/1000hrs.			20			24	mV
	Ripple rejection	Over temp.[2], f = 120Hz		8V ≤ V_{IN} ≤ 18V			9V ≤ V_{IN} ≤ 19V		
			62	80		59	80		dB
	Dropout voltage			2.0			2.0		V
I_{SC}		V_{IN} = 35V		300			270		mA
	Peak output current			700			700		mA
V_{OUT}	Output temperature drift	0°C ≤ T_J ≤ +125°C, I_{OUT} = 5mA		-1.0			-0.5		mV/°C

DC ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS	SA78M08C[2]			SA78M12C[2]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 14V			V_{IN} = 19V		
			7.7	8.0	8.3	11.5	12.0	12.5	V
		Over temp.[2], 5mA ≤ I_{OUT} ≤ 350mA		10.5V ≤ V_{IN} ≤ 23V			14.5V ≤ V_{IN} ≤ 27V		
			7.6		8.4	11.4		12.6	V
	Line regulation	I_{OUT} = 200mA		10.5V ≤ V_{IN} ≤ 25V			14.5V ≤ V_{IN} ≤ 30V		
				6	100		8	100	mV
				11V ≤ V_{IN} ≤ 25V			16V ≤ V_{IN} ≤ 30V		
				2	50		2	50	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 500mA		25	160		25	240	mV
		5mA ≤ I_{OUT} ≤ 200mA		10	80		10	120	mV
I_{CC}				4.6	8.0		4.8	8.0	mA
ΔI_{CC}	With line	Over temp.[2], I_{OUT} = 200mA		10.5V ≤ V_{IN} ≤ 25V			14.5V ≤ V_{IN} ≤ 30V		
				0.6			0.6		mA
ΔI_{CC}	With load	5mA ≤ I_{OUT} ≤ 350mA		0.3			0.3		mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz, T_A = 25°C		52			75		μV
	Voltage drift	mV/1000hrs.			32			48	mV
	Ripple rejection	Over temp.[2], f = 120Hz		11.5V ≤ V_{IN} ≤ 21.5V			15V ≤ V_{IN} ≤ 25V		
			56	80		55	80		dB
	Dropout voltage			2.0			2.0		V
I_{SC}		V_{IN} = 35V		250			240		mA
	Peak output current			700			700		mA
V_{OUT}	Output temperature drift	0°C ≤ T_J ≤ +125°C, I_{OUT} = 5mA		-0.5			-1.0		mV/°C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 350mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

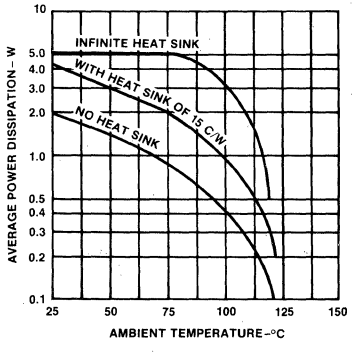
PARAMETER		TEST CONDITIONS	SA78M15C[2]			SA78M20C[2]			SA78M24C[2]			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 23V			V_{IN} = 29V			V_{IN} = 33V		
			14.4	15.0	15.6	19.2	20	20.8	23.0	24.0	25.0	V
				17.5V ≤ V_{IN} ≤ 30V			23V ≤ V_{IN} ≤ 35V			27V ≤ V_{IN} ≤ 38V		
		Over temp[2], 5mA ≤ I_{OUT} ≤ 350mA	14.25		15.75	19		21	22.8		25.2	V
	Line regulation	I_{OUT} = 200mA		17.5V ≤ V_{IN} ≤ 30V			23V ≤ V_{IN} ≤ 35V			27V ≤ V_{IN} ≤ 38V		
				10	100		10	100		10	100	mV
				20V ≤ V_{IN} ≤ 30V			24V ≤ V_{IN} ≤ 35V			30V ≤ V_{IN} ≤ 38V		
				3	50		5	50		5	50	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 500mA		25	150		30	400		30	480	mV
		5mA ≤ I_{OUT} ≤ 200mA		10	75		10	200		10	240	mV
I_{CC}				4.8	8.0		4.9	6.5		5	7	mA
ΔI_{CC}	With line	Over temp[2], I_{OUT} = 200mA		17.5V ≤ V_{IN} ≤ 30V			23V ≤ V_{IN} ≤ 35V			27V ≤ V_{IN} ≤ 38V		
				0.6			0.6			0.6		mA
ΔI_{CC}	With load	5mA ≤ I_{OUT} ≤ 350mA		0.3			0.3			0.3		mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz, T_A = 25°C		90			110			170		μV
	Voltage drift	mV/1000hrs.			60			80			96	mV
	Ripple rejection	Over temp[2], f = 120Hz		18.5V ≤ V_{IN} ≤ 28.5V			24V ≤ V_{IN} ≤ 34V			28V ≤ V_{IN} ≤ 38V		
			54	70		53	70		50	70		dB
	Dropout voltage			2.0			2.0			2.0		V
I_{SC}		V_{IN} = 35V		240			240			240		mA
	Peak output current			700			700			700		mA
V_{OUT}	Output temperature drift	0°C ≤ T_J ≤ +125°C, I_{OUT} = 5mA		-1.0			-1.1			-1.2		mV/°C

NOTES

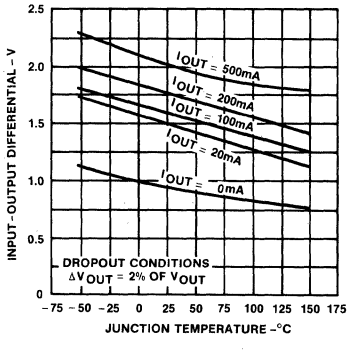
1. -55°C ≤ T_J ≤ +150°C for 78M00
   0°C ≤ T_J ≤ +125°C for 78M00C
2. -40°C ≤ T_J ≤ +125°C for SA78M00C

TYPICAL PERFORMANCE CHARACTERISTICS

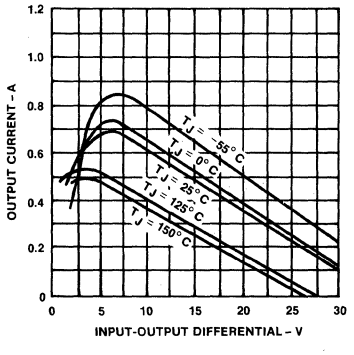
MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-220, 78M00C, SA78M00C)



DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE

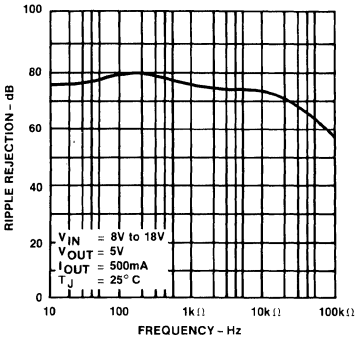


PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT/OUTPUT DIFFERENTIAL VOLTAGE

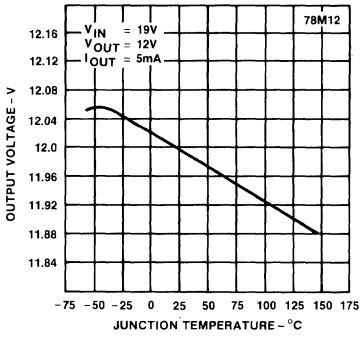


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

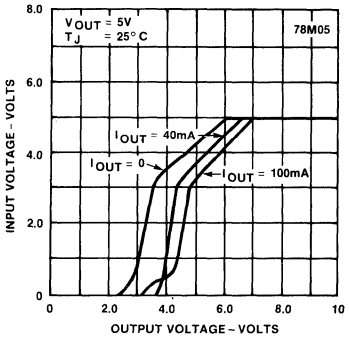
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



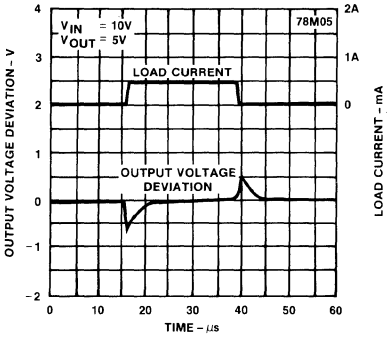
OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



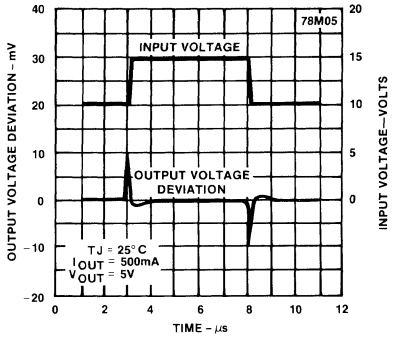
DROPOUT CHARACTERISTICS



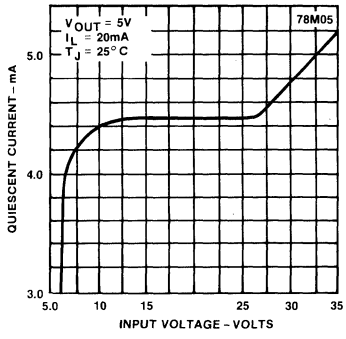
LOAD TRANSIENT RESPONSE



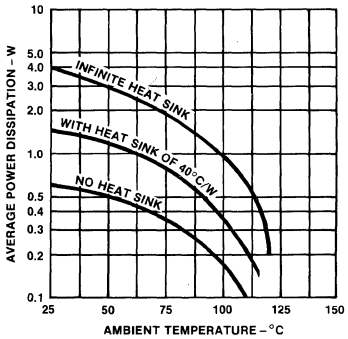
LINE TRANSIENT RESPONSE



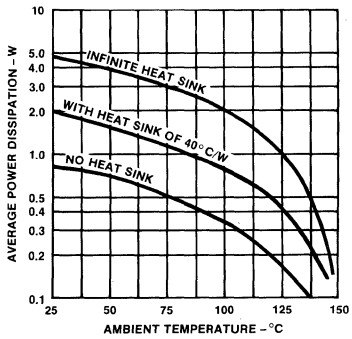
QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-39, 78M00C)



MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-39, 78M00)



7800-DA,U

DESCRIPTION

The 7800 series of monolithic Three-Terminal Positive Voltage Regulators employ internal current limiting, thermal shutdown and safe-area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. They are intended as fixed-voltage regulators in a wide range of applications including local, on-card regulation for elimination of distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power pass element in precision regulators.

FEATURES

- **Output current in excess of 1 amp**
- **No external components**
- **Internal thermal overload protection**
- **Internal short circuit current limiting**
- **Output transistor safe-area compensation**
- **Available in the TO-220 and the TO-3 package**
- **Output voltages of 5, 6, 8, 12, 14, 15, 18, and 24 volts**
- **Mil std 883 A, B, C available**

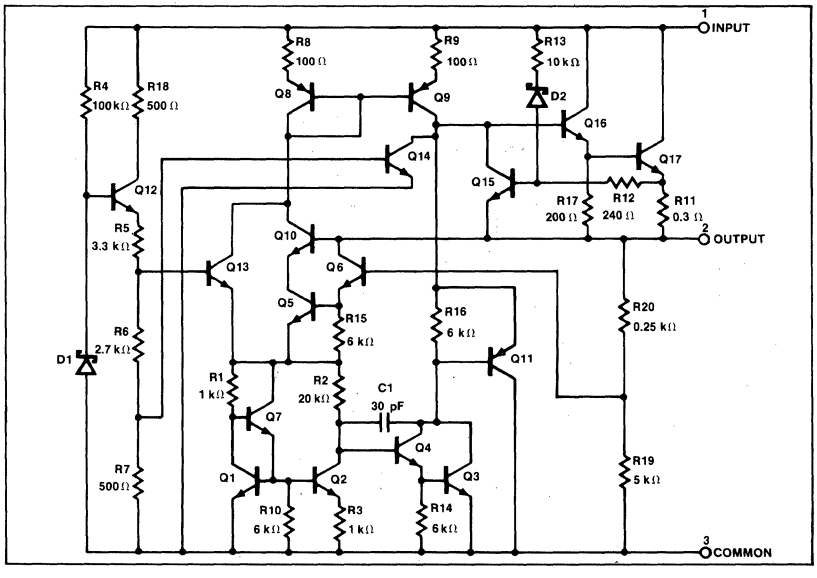
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Input voltage		
5V through 12V	35	V
14V through 24V	40	V
Internal power dissipation[1]	Internally limited	
Storage temperature range	-65 to +150	°C
Operating junction temperature range[2]		
7800	-55 to +150	°C
SA7800C	-40 to +85	°C
7800C	0 to +125	°C
Lead temperature		°C
TO-3 package (soldering, 60 second time limit)	300	
TO-220 package (soldering, 60 second time limit)	230	°C

NOTES

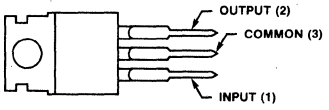
1. Thermal resistance of the packages (without a heat sink)
   Junction to case: TO-3 package 4°C/W; TO-220 package 2°C/W
   Junction to ambient: TO-3 package 35°C/W; TO-220 package 50°C/W
2. Operating ambient temperature range
   7800 -55°C to +125°C
   7800C 0°C to +85°C
   SA7800C -40°C to +85°C

SCHEMATIC DIAGRAM



PIN CONFIGURATION

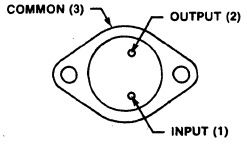
U PACKAGE (TO-220)



ORDER INFORMATION

OUTPUT VOLTAGE	ORDER PART NO.
5V	7805CU/SA7805CU
6V	7806CU/SA7806CU
8V	7808CU/SA7808CU
12V	7812CU/SA7812CU
13.8V	7814CU/SA7814CU
15V	7815CU/SA7815CU
18V	7818CU/SA7818CU
24V	7824CU/SA7824CU

DA PACKAGE (TO-3)



ORDER INFORMATION

OUTPUT VOLTAGE	ORDER PART NO.
5V	7805DA/SA7805CDA
6V	7806DA/SA7806CDA
8V	7808DA/SA7808CDA
12V	7812DA/SA7812CDA
13.8V	7814DA/SA7814CDA
15V	7815DA/SA7815CDA
18V	7818DA/SA7818CDA
24V	7824DA/SA7824CDA
5V	7805CDA
6V	7806CDA
8V	7808CDA
12V	7812CDA
13.8V	7814CDA
15V	7815CDA
18V	7818CDA
24V	7824CDA

DC ELECTRICAL CHARACTERISTICS

I_{OUT} = 500mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	7805[1]			7805C[1]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 10V			V_{IN} = 10V		
			4.8	5.0	5.2	4.8	5.0	5.2	V
		Over temp.,[1] 5mA ≤ I_{OUT} ≤ 1.0A, P_D ≤ 15W	8V ≤ V_{IN} ≤ 20V			7V ≤ V_{IN} ≤ 25V			
			4.65		5.35	4.75		5.25	V
	Line regulation		7V ≤ V_{IN} ≤ 25V			7V ≤ V_{IN} ≤ 25V			
				3	50		3	100	mV
			8V ≤ V_{IN} ≤ 12V			8V ≤ V_{IN} ≤ 12V			
				1	25		1	50	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 1.5A		15	50		15	100	mV
		250mA ≤ I_{OUT} ≤ 750mA		5	25		5	50	mV
I_{CC}				4.2	6.0		4.2	8.0	mA
ΔI_{CC}		Over temp.,[1] with line	8V ≤ V_{IN} ≤ 25V			7V ≤ V_{IN} ≤ 25V			
					0.8			1.3	mA
		With load, 5mA ≤ I_{OUT} ≤ 1.0A			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		40			40		μV
	Voltage drift				20			20	mV/1000hrs.
	Ripple rejection	Over temp.,[1] f = 120Hz	8V ≤ V_{IN} ≤ 18V			8V ≤ V_{IN} ≤ 18V			
			68	78		62	78		dB
	Dropout voltage	I_{OUT} = 1.0A		2.0			2.0		V
	Output resistance	f = 1kHz		17			17		mΩ
I_{SC}				750			750		mA
	Peak output current			2.2			2.2		A
V_{OUT}	Output temperature drift	I_{OUT} = 5mA	0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C			
				-1.1			-1.1		mV/°C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 500mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	7806[1]			7806C[1]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 11V			V_{IN} = 11V		
			5.75	6.0	6.25	5.75	6.0	6.25	V
		Over temp.,[1] 5mA ≤ I_{OUT} ≤ 1.0A, P_D ≤ 15W	9V ≤ V_{IN} ≤ 21V			8V ≤ V_{IN} ≤ 21V			
			5.65		6.35	5.7		6.3	V
	Line regulation		8V ≤ V_{IN} ≤ 25V			8V ≤ V_{IN} ≤ 25V			
				5	60		5	120	mV
			9V ≤ V_{IN} ≤ 13V			9V ≤ V_{IN} ≤ 13V			
				1.5	30		1.5	60	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 1.5A		14	60		14	120	mV
		250mA ≤ I_{OUT} ≤ 750mA		4	30		4	60	mV
I_{CC}				4.3	6.0		4.3	8.0	mA
ΔI_{CC}		Over temp.,[1] with line	9V ≤ V_{IN} ≤ 25V			8V ≤ V_{IN} ≤ 25V			
					0.8			1.3	mA
		With load, 5mA ≤ I_{OUT} ≤ 1.0A			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		45			45		μV
	Voltage drift				24			24	mV/1000hrs.
	Ripple rejection	Over temp.,[1] f = 120Hz	9V ≤ V_{IN} ≤ 19V			9V ≤ V_{IN} ≤ 19V			
			65	75		59	75		dB
	Dropout voltage	I_{OUT} = 1.0A		2.0			2.0		V
	Output resistance	f = 1kHz		19			19		mΩ
I_{SC}				550			550		mA
	Peak output current			2.2			2.2		A
V_{OUT}	Output temperature drift	I_{OUT} = 5mA	0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C			
				-0.8			-0.8		mV/°C

NOTES
1. −55°C ≤ T_J ≤ 150°C for 7800
   0°C ≤ T_J ≤ 125°C for 7800C
2. 40°C ≤ T_J ≤ +125°C for SA7800C

7800-DA,U

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 500mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	7808[1]			7808C[1]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 14V			V_{IN} = 14V		
			7.7	8.0	8.3	7.7	8.0	8.3	V
		Over temp., 5mA ≤ I_{OUT} ≤ 1.0A, P_D ≤ 15W		11.5V ≤ V_{IN} ≤ 23V			10.5V ≤ V_{IN} ≤ 23V		
			7.6		8.4	7.6		8.4	V
	Line regulation			10.5V ≤ V_{IN} ≤ 25V			10.5V ≤ V_{IN} ≤ 25V		
				6	80		6	160	mV
				11V ≤ V_{IN} ≤ 17V			11V ≤ V_{IN} ≤ 17V		
				2	40		2	80	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 1.5A		12	80		12	160	mV
		250mA ≤ I_{OUT} ≤ 750mA		4	40		4	80	mV
I_{CC}				4.3	6.0		4.3	8.0	mA
ΔI_{CC}		Over temp.,[1] with line		11.5V ≤ V_{IN} ≤ 25V			10.5V ≤ V_{IN} ≤ 25V		
					0.8			1.0	mA
		With load, 5mA ≤ I_{OUT} ≤ 1.0A			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		52			52		μV
	Voltage drift				32			32	mV/1000hrs.
	Ripple rejection	Over temp.,[1] f = 120Hz		11.5V ≤ V_{IN} ≤ 21.5V			11.5V ≤ V_{IN} ≤ 21.5V		
			62	72		56	72		dB
	Dropout voltage	I_{OUT} = 1.0A		2.0			2.0		V
	Output resistance	f = 1kHz		16			16		mΩ
I_{SC}				450			450		mA
	Peak output current			2.2			2.2		A
V_{OUT}	Output temperature drift	I_{OUT} = 5mA		0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C		
				-0.8			-0.8		mV/°C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 500mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	7812[1]			7812C[1]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 19V			V_{IN} = 19V		
			11.5	12.0	12.5	11.5	12.0	12.5	V
		Over temp.,[1] 5mA ≤ I_{OUT} ≤ 1.0A, P_D ≤ 15W		15.5V ≤ V_{IN} ≤ 27V			14.5V ≤ V_{IN} ≤ 27V		
			11.4		12.6	11.4		12.6	V
	Line regulation			14.5V ≤ V_{IN} ≤ 30V			14.5V ≤ V_{IN} ≤ 30V		
				10	120		10	240	mV
				16V ≤ V_{IN} ≤ 22V			16V ≤ V_{IN} ≤ 22V		
				3	60		3	120	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 1.5A		12	120		12	240	mV
		250mA ≤ I_{OUT} ≤ 750mA		4	60		4	120	mV
I_{CC}				4.3	6.0		4.3	8.0	mA
ΔI_{CC}		Over temp.,[1] with line		15V ≤ V_{IN} ≤ 30V			14.5V ≤ V_{IN} ≤ 30V		
					0.8			1.0	mA
		With load, 5mA ≤ I_{OUT} ≤ 1.0A			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		75			75		μV
	Voltage drift				48			48	mV/1000hrs.
	Ripple rejection	Over temp.,[1] f = 120Hz		15V ≤ V_{IN} ≤ 25V			15V ≤ V_{IN} ≤ 25V		
			61	71		55	71		dB
	Dropout voltage	I_{OUT} = 1.0A		2.0			2.0		V
	Output resistance	f = 1kHz		18			18		mΩ
I_{SC}				350			350		mA
	Peak output current			2.2			2.2		A
V_{OUT}	Output temperature drift	I_{OUT} = 5mA		0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C		
				-1.0			-1.0		mV/°C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 500mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	7814[1]			7814C[1]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 22V			V_{IN} = 22V		
			13.3	13.8	14.3	13.3	13.8	14.3	V
		Over temp.[1] 5mA ≤ I_{OUT} ≤ 1.0A, P_D ≤ 15W		17.5V ≤ V_{IN} ≤ 29V			16.5V ≤ V_{IN} ≤ 29V		
			13.15		14.45	13.15		14.95	V
	Line regulation			16.5V ≤ V_{IN} ≤ 30V			16.5V ≤ V_{IN} ≤ 30V		
				10	140		10	280	mV
				19V ≤ V_{IN} ≤ 25V			19V ≤ V_{IN} ≤ 25V		
				3	70		3	140	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 1.5A		12	140		12	280	mV
		250mA ≤ I_{OUT} ≤ 750mA		4	70		4	140	mV
I_{CC}				4.3	6.0		4.3	8.0	mA
ΔI_{CC}		Over temp.[1] with line		17V ≤ V_{IN} ≤ 30V			16.5V ≤ V_{IN} ≤ 30V		
					0.8			1.0	mA
		With load, 5mA ≤ I_{OUT} ≤ 1.0A			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		85			85		μV
	Voltage drift				56			56	mV/1000hrs.
	Ripple rejection	Over temp.[1] f = 120Hz		17V ≤ V_{IN} ≤ 27V			17V ≤ V_{IN} ≤ 27V		
			54	70		60	70		dB
	Dropout voltage	I_{OUT} = 1.0A		2.0			2.0		V
	Output resistance	f = 1kHz		18			18		mΩ
I_{SC}				350			350		mA
	Peak output current			2.2			2.2		A
V_{OUT}	Output temperature drift	I_{OUT} = 5mA		0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C		
				1.0			1.0		mV/°C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 500mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	7815[1]			7815C[1]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 23V			V_{IN} = 23V		
			14.4	15.0	15.6	14.4	15.0	15.6	V
		Over temp.[1] 5mA ≤ I_{OUT} ≤ 1.0A, P_D ≤ 15W		18.5V ≤ V_{IN} ≤ 30V			17.5V ≤ V_{IN} ≤ 30V		
			14.25		15.75	14.25		15.75	V
	Line regulation			17.5V ≤ V_{IN} ≤ 30V			17.5V ≤ V_{IN} ≤ 30V		
				11	150		11	300	mV
				20V ≤ V_{IN} ≤ 26V			20V ≤ V_{IN} ≤ 26V		
				3	75		3	150	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 1.5A		12	150		12	300	mV
		250mA ≤ I_{OUT} ≤ 750mA		4	75		4	150	mV
I_{CC}				4.4	6.0		4.4	8.0	mA
ΔI_{CC}		Over temp.[1] with line		18.5V ≤ V_{IN} ≤ 30V			17.5V ≤ V_{IN} ≤ 30V		
					0.8			1.0	mA
		With load, 5mA ≤ I_{OUT} ≤ 1.0A			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		90			90		μV
	Voltage drift				60			60	mV/1000hrs.
	Ripple rejection	Over temp.[1] f = 120Hz		18.5V ≤ V_{IN} ≤ 28.5V			18.5V ≤ V_{IN} ≤ 28.5V		
			60	70		54	70		dB
	Dropout voltage	I_{OUT} = 1.0A		2.0			2.0		V
	Output resistance	f = 1kHz		19			19		mΩ
I_{SC}				230			230		mA
	Peak output current			2.1			2.1		A
V_{OUT}	Output temperature drift	I_{OUT} = 5mA		0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C		
				-1.0			-1.0		mV/°C

7800-DA,U

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 500mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

	PARAMETER	TEST CONDITIONS	7818[1]			7818C[1]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 27V			V_{IN} = 27V		
			17.3	18.0	18.7	17.3	18.0	18.7	V
		Over temp.,[1] 5mA ≤ I_{OUT} ≤ 1.0A, P_D ≤ 15W		22V ≤ V_{IN} ≤ 33V			21V ≤ V_{IN} ≤ 33V		
			17.1		18.9	17.1		18.9	V
	Line regulation			21V ≤ V_{IN} ≤ 33V			21V ≤ V_{IN} ≤ 33V		
				15	180		15	360	mV
				24V ≤ V_{IN} ≤ 30V			24V ≤ V_{IN} ≤ 30V		
				5	90		5	180	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 1.5A		12	180		12	360	mV
		250mA ≤ I_{OUT} ≤ 750mA		4	90		4	180	mV
I_{CC}				4.5	6.0		4.5	8.0	mA
ΔI_{CC}		Over temp.,[1] with line		22V ≤ V_{IN} ≤ 33V			21V ≤ V_{IN} ≤ 33V		
					0.8			1.0	mA
		With load, 5mA ≤ I_{OUT} ≤ 1.0A			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		110			110		μV
	Voltage drift				72			72	mV/1000hrs.
	Ripple rejection	Over temp.,[1] f = 120Hz		22V ≤ V_{IN} ≤ 32V			22V ≤ V_{IN} ≤ 32V		
			59	69		53	69		dB
	Dropout voltage	I_{OUT} = 1.0A		2.0			2.0		V
	Output resistance	f = 1kHz		22			22		mΩ
I_{SC}				200			200		mA
	Peak output current			2.1			2.1		A
V_{OUT}	Output temperature drift	I_{OUT} = 5mA		0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C		
				-1.0			-1.0		mV/°C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 500mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

	PARAMETER	TEST CONDITIONS	7824[1]			7824C[1]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 33V			V_{IN} = 33V		
			23.0	24.0	25.0	23.0	24.0	25.0	V
		Over temp.,[1] 5mA ≤ I_{OUT} ≤ 1.0A, P_D ≤ 15W		28V ≤ V_{IN} ≤ 38V			28V ≤ V_{IN} ≤ 38V		
			22.8		25.2	22.8		25.2	V
	Line regulation			27V ≤ V_{IN} ≤ 38V			27V ≤ V_{IN} ≤ 38V		
				18	240		18	480	mV
				30V ≤ V_{IN} ≤ 36V			30V ≤ V_{IN} ≤ 36V		
				6	120		6	240	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 1.5A		12	240		12	480	mV
		250mA ≤ I_{OUT} ≤ 750mA		4	120		4	240	mV
I_{CC}				4.6	6.0		4.6	8.0	mA
ΔI_{CC}		Over temp.,[1] with line		28V ≤ V_{IN} ≤ 38V			27V ≤ V_{IN} ≤ 38V		
					0.8			1.0	mA
		With load, 5mA ≤ I_{OUT} ≤ 1.0A			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		170			170		μV
	Voltage drift				96			96	mV/1000hrs.
	Ripple rejection	Over temp.,[1] f = 120Hz		28V ≤ V_{IN} ≤ 38V					
			56	66		50	66		dB
	Dropout voltage	I_{OUT} = 1.0A		2.0			2.0		V
	Output resistance	f = 1kHz		28			28		mΩ
I_{SC}				150			150		mA
	Peak output current			2.1			2.1		A
V_{OUT}	Output temperature drift	I_{OUT} = 5mA		0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C		
				-1.5			-1.5		mV/°C

7800-DA,U

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 500mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	SA7805C[2]			SA7806C[2]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 10V			V_{IN} = 11V		
			4.8	5.0	5.2	5.75	6.0	6.25	V
		Over temp.,[2] 5mA ≤ I_{OUT} ≤ 1.0A, P_D ≤ 15W		7V ≤ V_{IN} ≤ 25V			8V ≤ V_{IN} ≤ 25V		
			4.65		5.35	5.65		6.35	V
	Line regulation			7V ≤ V_{IN} ≤ 25V			8V ≤ V_{IN} ≤ 25V		
				3	100		5	120	mV
				8V ≤ V_{IN} ≤ 12V			9V ≤ V_{IN} ≤ 13V		
				1	50		1.5	60	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 1.5A		15	100		14	120	mV
		250mA ≤ I_{OUT} ≤ 750mA		5	50		4	60	mV
I_{CC}				4.2	8.0		4.3	8.0	mA
ΔI_{CC}		Over temp.,[2] with line		7V ≤ V_{IN} ≤ 25V			8V ≤ V_{IN} ≤ 25V		
				0.8			0.8		mA
		With load, 5mA ≤ I_{OUT} ≤ 1.0A		0.3			0.3		mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		40			45		μV
	Voltage drift				20			24	mV/1000hrs.
	Ripple rejection	Over temp.,[2] f = 120Hz		8V ≤ V_{IN} ≤ 18V			9V ≤ V_{IN} ≤ 19V		
			62	78		59	75		dB
	Dropout voltage	I_{OUT} = 1.0A		2.0			2.0		V
	Output resistance	f = 1kHz		17			19		mΩ
I_{SC}				750			550		mA
	Peak output current			2.2			2.2		A
V_{OUT}	Output temperature drift	0°C ≤ T_J ≤ 125°C, I_{OUT} = 5mA		-1.1			-0.8		mV/°C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 500mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	SA7808C[2]			SA7812C[2]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 14V			V_{IN} = 19V		
			7.7	8.0	8.3	11.5	12.0	12.5	V
		Over temp.,[2] 5mA ≤ I_{OUT} ≤ 1.0A, P_D ≤ 15W		10.5V ≤ V_{IN} ≤ 23V			14.5V ≤ V_{IN} ≤ 27V		
			7.6		8.4	11.4		12.6	V
	Line regulation			10.5V ≤ V_{IN} ≤ 25V			14.5V ≤ V_{IN} ≤ 30V		
				6	160		10	240	mV
				11V ≤ V_{IN} ≤ 17V			16V ≤ V_{IN} ≤ 22V		
				2	80		3	120	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 1.5A		12	160		12	240	mV
		250mA ≤ I_{OUT} ≤ 750mA		4	80		4	120	mV
I_{CC}				4.3	8.0		4.3	8.0	mA
ΔI_{CC}		Over temp.,[2] with line		10.5V ≤ V_{IN} ≤ 25V			14.5V ≤ V_{IN} ≤ 30V		
				0.8			0.8		mA
		With load, 5mA ≤ I_{OUT} ≤ 1.0A		0.3			0.3		mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		52			75		μV
	Voltage drift				32			48	mV/1000hrs.
	Ripple rejection	Over temp.,[2] f = 120Hz		11.5V ≤ V_{IN} ≤ 21.5V			15V ≤ V_{IN} ≤ 25V		
			56	72		61	71		dB
	Dropout voltage	I_{OUT} = 1.0A		2.0			2.0		V
	Output resistance	f = 1kHz		16			18		mΩ
I_{SC}				450			350		mA
	Peak output current			2.2			2.2		A
V_{OUT}	Output temperature drift	0°C ≤ T_J ≤ 125°C, I_{OUT} = 5mA		-0.8			-1.0		mV/°C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 500mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	SA7814C[2]			SA7815C[2]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 22V			V_{IN} =23V		
			13.3	13.8	14.3	14.4	15.0	15.6	V
		Over temp.[2], 5mA ≤ I_{OUT} ≤ 1.0A,		16.5V ≤ V_{IN} ≤ 29V			17.5 ≤ V_{IN} ≤ 30V		
		P_D ≤ 15W	13.15		14.95	14.25		15.75	V
	Line regulation			16.5V ≤ V_{IN} ≤ 30V			17.5V ≤ V_{IN} ≤ 30V		
				10	280		11	300	mV
				19V ≤ V_{IN} ≤ 25V			20V ≤ V_{IN} ≤ 26V		
				3	140		3	150	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 1.5A		12	280		12	150	mV
		250mA ≤ I_{OUT} ≤ 750mA		4	140		4	75	mV
I_{CC}				4.3	8.0		4.4	8.0	mA
I_{CC}		Over temp.[2], with line		16.5V ≤ V_{IN} ≤ 30V			17.5V ≤ V_{IN} ≤ 30V		
				0.8			0.8		mA
		With load, 5mA ≤ I_{OUT} ≤ 1.0A		0.3			0.3		mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		85			90		μV
	Voltage drift				56			60	mV/1000hrs.
	Ripple rejection	Over temp.[2], f = 120Hz		17V ≤ V_{IN} ≤ 27V			18.5V ≤ V_{IN} ≤ 28.5V		
			60	70		60	70		dB
	Dropout voltage	I_{OUT} = 1.0A		2.0			2.0		V
	Output resistance	f = 1kHz		18			19		mΩ
I_{SC}				350			230		mA
	Peak output current			2.2			2.1		A
V_{OUT}	Output temperature drift	0°C ≤ T_J ≤ 125°C, I_{OUT} = 5mA		-1.0			-1.0		mV/°C

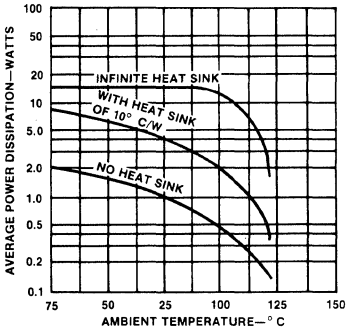
DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 500mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

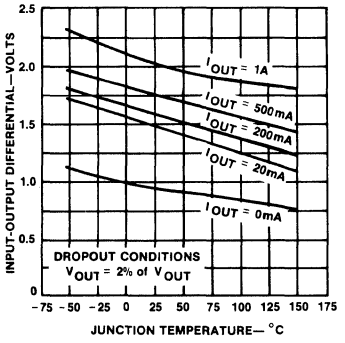
PARAMETER		TEST CONDITIONS	SA7818C[2]			SA7824C[2]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 27V			V_{IN} = 33V		
			17.3	18.0	18.7	23.0	24.0	25.0	V
		Over temp.[2], 5mA ≤ I_{OUT} ≤ 1.0A,		21V ≤ V_{IN} ≤ 33V			28V ≤ V_{IN} ≤ 38V		
		P_D ≤ 15W	17.1		18.9	22.8		25.2	V
	Line regulation			21V ≤ V_{IN} ≤ 33V			27V ≤ V_{IN} ≤ 38V		
				15	360		18	480	mV
				24V ≤ V_{IN} ≤ 30V			30V ≤ V_{IN} ≤ 36V		
				5	180		6	240	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 1.5A		12	360		12	480	mV
		250mA ≤ I_{OUT} ≤ 750mA		4	180		4	240	mV
I_{CC}				4.5	8.0		4.6	8.0	mA
I_{CC}		Over temp.[2], with line		21V ≤ V_{IN} ≤ 33V			27V ≤ V_{IN} ≤ 38V		
				0.8			0.8		mA
		With load, 5mA ≤ I_{OUT} ≤ 1.0A		0.3			0.3		mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		110			170		μV
	Voltage drift				72			96	mV/1000hrs.
	Ripple rejection	Over temp.[2], f = 120Hz		22V ≤ V_{IN} ≤ 32V			27V ≤ V_{IN} ≤ 38V		
			59	69		56	66		dB
	Dropout voltage	I_{OUT} = 1.0A		2.0			2.0		V
	Output resistance	f = 1kHz		22			28		mΩ
I_{SC}				200			150		mA
	Peak output current			2.1			2.1		A
V_{OUT}	Output temperature drift	0°C ≤ T_J ≤ 125°C, I_{OUT} = 5mA		-1.0			-1.5		mV/°C

TYPICAL PERFORMANCE CHARACTERISTICS

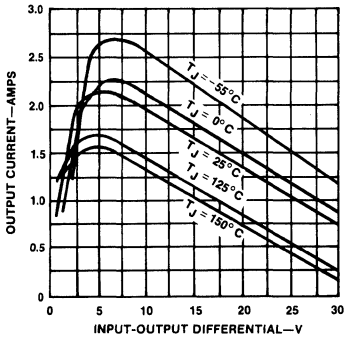
MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-220, 7800C)



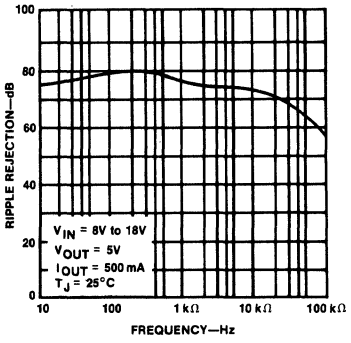
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



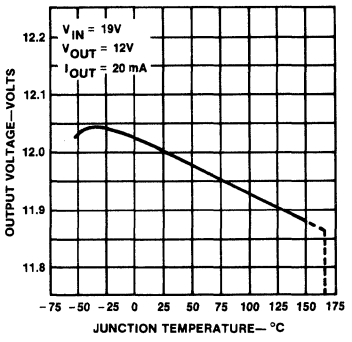
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT/OUTPUT DIFFERENTIAL VOLTAGE



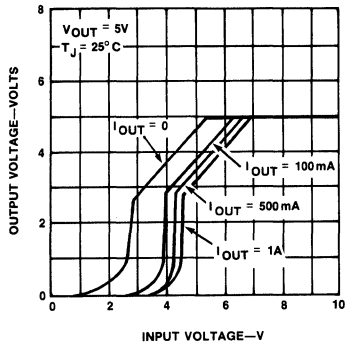
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



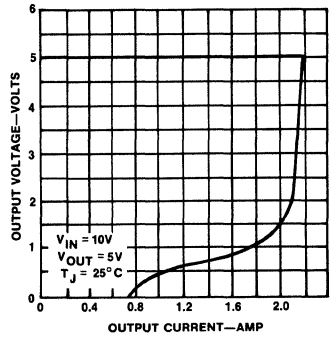
OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



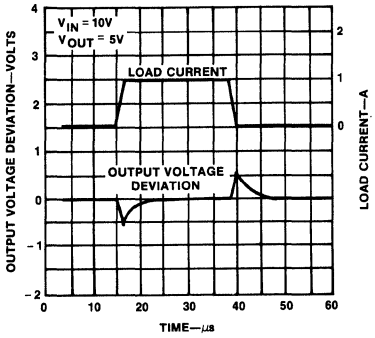
DROPOUT CHARACTERISTICS



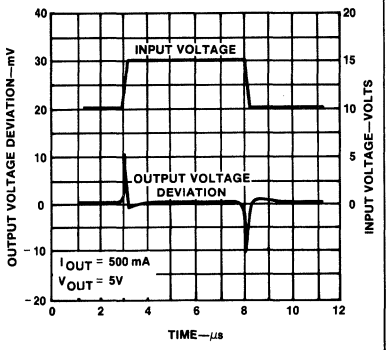
CURRENT LIMITING CHARACTERISTICS



LOAD TRANSIENT RESPONSE

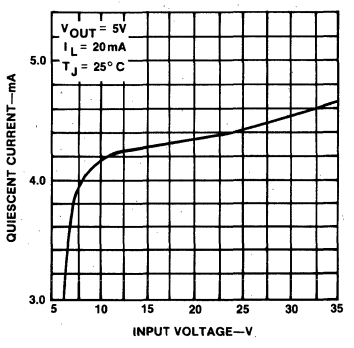


LINE TRANSIENT RESPONSE

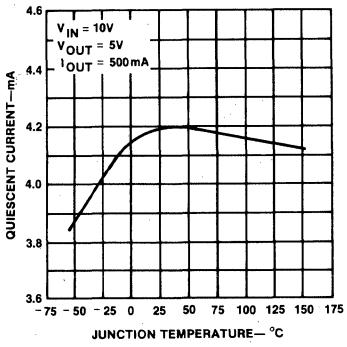


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

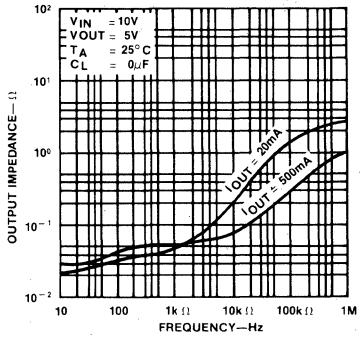
QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE

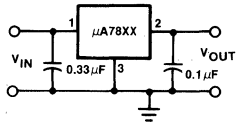


OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY

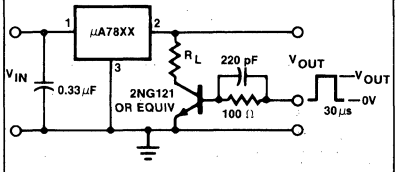


EQUIVALENT TEST CIRCUITS

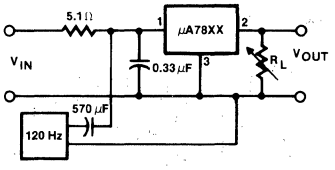
DC PARAMETER TEST CIRCUIT



LOAD REGULATION TEST CIRCUIT



RIPPLE REJECTION TEST CIRCUIT



μA7905/05.2/06/08/12/15/18/24-U,DA

DESCRIPTION

The μA7900 series of monolithic Three-Terminal Negative Voltage Regulators employs internal current limiting, thermal shutdown and safe-area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. They are intended as fixed-voltage complements to the μA7800 positive regulators.

FEATURES

- **Output current in excess of 1 amp**
- **No external components**
- **Internal thermal overload protection**
- **Internal short circuit current limiting**
- **Output transistor safe-area compensation**
- **Available in the TO-220 and the TO-3 packages**
- **Output voltages of -5, -5.2, -6, -8, -12, -15, -18 and -24 volts**
- **Mil std 883A,B,C available**

ABSOLUTE MAXIMUM RATINGS

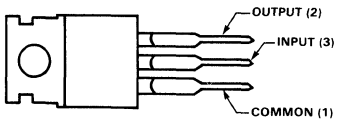
	PARAMETER	RATING	UNIT
V_{IN}	Input voltage		V
	-5V through -18V	-35	
	-24V	-40	
	Internal power dissipation[1]	Internally limited	
T_{stg}	Storage temperature range	-65 to +150	°C
T_J	Operating junction temperature range[2]		°C
	7900	-55 to +150	
	7900C	0 to +125	
	Lead temperature		°C
	TO-3 package (soldering, 60 second time limit)	300	
	TO-220 package (soldering, 10 second time limit)	230	

NOTES

1. Thermal resistance of the packages (without a heat sink)
   Junction to case: TO-3 Package 4°C/W; TO-220 Package 2°C/W
   Junction to ambient: TO-3 Package 35°C/W; TO-220 Package 50°C/W
2. Operating Ambient Temperature Range
   7900 -55°C to +125°C
   7900C 0°C to +85°C

PIN CONFIGURATION

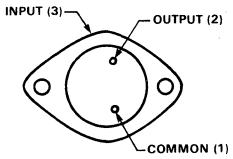
U PACKAGE (TO-220)



ORDER INFORMATION

Output voltage	Order part no.
-5V	7905CU
-5.2V	7905.2CU
-6V	7906CU
-8V	7908CU
-12V	7912CU
-15V	7915CU
-18V	7918CU
-24V	7924CU

DA PACKAGE (TO-3)



ORDER INFORMATION

Output voltage	Order part no.
-5V	7905DA
-5.2V	7905.2DA
-6V	7906DA
-8V	7908DA
-12V	7912DA
-15V	7915DA
-18V	7918DA
-24V	7924DA
-5V	7905CDA
-5.2V	7905.2CDA
-6V	7906CDA
-8V	7908CDA
-12V	7912CDA
-15V	7915CDA
-18V	7918CDA
-24V	7924CDA

DC ELECTRICAL CHARACTERISTICS

I_{OUT} = 500mA, -55°C ≤ T_J ≤ 150°C,[1]
C_{IN} = 2μF, C_{OUT} = 1μF unless otherwise specified.

PARAMETER	TEST CONDITIONS	7905			7095C			7905.2			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OUT}	T_J = 25°C	V_{IN} = -10V			V_{IN} = -10V			V_{IN} = -10V			V
		-4.8	-5.0	-5.2	-4.8	-5.0	-5.2	-5.0	-5.2	-5.4	
	P ≤ 15W	-8V ≤ V_{IN} ≤ -20V			-7V ≤ V_{IN} ≤ -20V			-8V ≤ V_{IN} ≤ -20V			
	5mA ≤ I_{OUT} ≤ 1.0A	-4.7		-5.3	-4.75		-5.25	-5.0		-5.4	
Line regulation	T_J = 25°C	-7V ≤ V_{IN} ≤ -25V			-7V ≤ V_{IN} ≤ -25V			-7.2V ≤ V_{IN} ≤ -25V			mV
			3	50		3	100		3	52	
		-8V ≤ V_{IN} ≤ -12V			-8V - V_{IN} ≤ -12V			-8V ≤ V_{IN} ≤ -12V			
			1	25		1	50		1	27	
Load regulation	T_J = 25°C										mV
	5mA ≤ I_{OUT} ≤ 1.5A		15	50		15	100		15	52	
	250mA ≤ I_{OUT} ≤ 750mA		5	25		5	50		5	27	
I_{CC}	T_J = 25°C		1	2		1	2		1	2	mA
with line		-8V ≤ V_{IN} ≤ -25V			-7V ≤ V_{IN} ≤ -25V			-8V ≤ V_{IN} ≤ -25V			
				1.3			1.3			1.3	
with load	5mA ≤ I_{OUT} ≤ 1.0A		.1	0.5		.1	0.5		.1	0.5	
Output noise voltage	T_A = 25°C 10Hz ≤ f ≤ 100kHz		125			125			130		μV
Long term stability			20			20			22		mV
Ripple rejection	f = 120Hz	-8V ≤ V_{IN} ≤ -18V			-8V ≤ V_{IN} ≤ -18V			-8V ≤ V_{IN} ≤ -18V			dB
	I_{OUT} = 20mA	54	60		54	60		54	60		
Dropout voltage	T_J = 25°C I_{OUT} = 1.0A		1.1			1.1			1.1		V
Output resistance	f = 1kHz		17			17			17		mΩ
I_{OS}	T_J = 25°C		500			500			500		mA
Peak output current	T_J = 25°C		2.1			2.1			2.1		A
Average temperature coefficient of input voltage	I_{OUT} = 5mA	0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C			0°C ≤ T_J ≤ 150°C			mV/°C
			-.4			-.4			-.4		

NOTE

1. 7900C - 0°C ≤ T_J ≤ 125°C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 500mA, -55°C ≤ T_J ≤ 150°C,[1] C_{IN} = 2μF, C_{OUT} = 1μF unless otherwise specified.

PARAMETER	TEST CONDITIONS	7905.2C			7906			7906C			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OUT}	T_J = 25°C		V_{IN} = -10V			V_{IN} = -11V			V_{IN} = -11V		V
		-5.0	-5.2	-5.4	-5.75	-6.0	-6.25	-5.75	-6.0	-6.25	
	P ≤ 15W		-7.2V ≤ V_{IN} ≤ -20V			-9V ≤ V_{IN} ≤ -21V			-8V ≤ V_{IN} ≤ -25V		
	5mA ≤ I_{OUT} ≤ 1.0A	-4.94		-5.46	-5.65		-6.35	-5.7		-6.3	
Line regulation	T_J = 25°C		-7.2V ≤ V_{IN} ≤ -25V			-8V ≤ V_{IN} ≤ -25V			-8V≤ V_{IN} ≤ -25V		mV
			3	105		5	60		5	120	
			-8V ≤ V_{IN} ≤ -12V			-9V ≤ V_{IN} ≤ -13V			-9V ≤ V_{IN} ≤ -13V		
			1	52		1.5	30		1.5	60	
Load regulation	T_J = 25°C										mV
	5mA ≤ I_{OUT} ≤ 1.5A		15	105		14	60		14	120	
	250mA ≤ I_{OUT} ≤ 750mA		5	52		4	30		4	60	
I_{CC}	T_J = 25°C		1	2		1	2		1	2	mA
with line			-7.2V ≤ V_{IN} ≤ -25V			-9V ≤ V_{IN} ≤ -25V			-8V ≤ V_{IN} ≤ -25V		
				1.3			1.3			1.3	
with load	5mA ≤ I_{OUT} ≤ 1.0A		0.1	0.5		0.1	0.5		0.1	0.5	
Output noise voltage	T_A = 25°C 10Hz ≤ f ≤ 100kHz		130			150			150		μV
Long term stability			22			24			24		mV
Ripple rejection	f = 120Hz		-8V ≤ V_{IN} ≤ -18V			-9V ≤ V_{IN} ≤ -19V			-9V ≤ V_{IN} ≤ -19V		dB
	I_{OUT} = 20mA	54	60		54	60		54	60		
Dropout voltage	T_J = 25°C I_{OUT} = 1.0A		1.1			1.1			1.1		V
Output resistance	f = 1kHz		17			19			19		mΩ
I_{OS}	T_J = 25°C		500			500			500		mA
Peak output current	T_J = 25°C		2.1			2.1			2.1		A
Average temperature coefficient of input voltage	I_{OUT} = 5mA		0°C ≤ T_J ≤ 125°C -0.4			0°C ≤ T_J ≤ 150°C -0.4			0°C ≤ T_J ≤ 125°C -0.4		mV/°C

NOTE

1. 7900 - 0°C ≤ T_J ≤ 125°C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 500mA, -55°C ≤ T_J ≤ 150°C,[1] C_{IN} = 2μF, C_{OUT} = 1μF unless otherwise specified.

PARAMETER	TEST CONDITIONS	7908			7908C			7912			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OUT}	T_J = 25°C		V_{IN} = - 14V			V_{IN} = -14V			V_{IN}= -19V		V
		-7.7	-8.0	-8.3	-7.7	-8.0	-8.3	-11.5	-12.0	-12.5	
	P ≤ 15W		-11.5V ≤ V_{IN} ≤ -23V			-10.5V ≤ V_{IN} ≤ -23V			-15.5V ≤ V_{IN} ≤ -27V		
	5mA ≤ I_{OUT} ≤ 1.0A	-7.6		-8.4	-7.6		-8.4	-11.4		-12.6	
Line regulation	T_J = 25°C		-10.5V ≤ V_{IN} ≤ -25V			-10.5V ≤ V_{IN} ≤ -25V			-14.5V ≤ V_{IN} ≤ -30V		mV
			6	80		6	160		10	120	
			-11V ≤ V_{IN} ≤ -17V			-11V ≤ V_{IN} ≤ -17V			-16V ≤ V_{IN} ≤ -22V		
			2	40		2	80		3	60	
Load regulation	T_J = 25°C										mV
	5mA ≤ I_{OUT} ≤ 1.5A		12	80		12	160		12	120	
	250mA ≤ I_{OUT} ≤ 750mA		4	40		4	80		4	60	
I_{CC}	T_J = 25°C		1	2		1	2		1.5	3.0	mA
with line			-11.5V ≤ V_{IN} ≤ -25V			-10.5V ≤ V_{IN} ≤ -25V			-15V ≤ V_{IN} ≤ -30V		
				1.0			1.0			1.0	
with load	5mA ≤ I_{OUT} ≤ 1.0A		.1	0.5		.1	0.5		.1	0.5	
Output noise voltage	T_A = 25°C 10Hz ≤ f ≤ 100kHz		200			200			300		μV
Long term stability			32			32			48		mV
Ripple rejection	f = 120Hz		-11.5V ≤ V_{IN} ≤ -21.5V			-11.5V ≤ V_{IN} ≤ -21.5V			-15V ≤ V_{IN} ≤ -25V		dB
	I_{OUT} = 20mA	54	60		54	60		54	60		
Dropout voltage	T_J = 25°C I_{OUT} = 1.0A		1.1			1.1			1.1		V
Output resistance	f = 1kHz		16			16			18		mΩ
I_{OS}	T_J = 25°C		500			500			500		mA
Peak output current	T_J = 25°C		2.1			2.1			2.1		A
Average temperature coefficient of input voltage	I_{OUT} = 5mA		0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C			0°C ≤ T_J ≤ 150°C		mV/°C
			-0.6			-0.6			-0.8		

NOTE

1. 7900C - 0°C ≤ T_J ≤ 125°C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 500mA, -55°C ≤ T_J ≤ 150°C,[1] C_{IN} = 2μF, C_{OUT} = 1μF unless otherwise specified.

PARAMETER	TEST CONDITIONS	7912C			7915			7915C			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OUT}	T_J = 25°C		V_{IN} = -19V			V_{IN} = -23V			V_{IN} = -23V		V
		-11.5	-12.0	-12.5	-14.4	-15.0	-15.6	-14.4	-15.0	-15.6	
	P ≤ 15W		-14.5V ≤ V_{IN} ≤ -27V			-18.5V ≤ V_{IN} ≤ -30V			-17.5V ≤ V_{IN} ≤ -30V		
	5mA ≤ I_{OUT} ≤ 1.0A	-11.4		-12.6	-14.25		-15.75	-14.25		-15.75	
Line regulation	T_J = 25°C		-14.5V ≤ V_{IN} ≤ -30V			-17.5V ≤ V_{IN} ≤ -30V			-17.5V ≤ V_{IN} -30V		mV
			10	240		11	150		11	300	
			-16V ≤ V_{IN} ≤ -22V			-20V ≤ V_{IN} ≤ -26V			-20V ≤ V_{IN}≤ -26V		
			3	120		3	75		3	150	
Load regulation	T_J = 25°C										mV
	5mA ≤ I_{OUT} ≤ 1.5A		12	240		12	150		12	300	
	250mA ≤ I_{OUT} ≤ 750mA		4	120		4	75		4	150	
I_{CC}	T_J = 25°C		1.5	3.0		1.5	3.0		1.5	3.0	mA
with line			-14.5V ≤ V_{IN} ≤ -30V			-18.5V ≤ V_{IN} ≤ -30V			-17.5V ≤ V_{IN} ≤ -30V		
				1.0			1.0			1.0	
with load	5mA ≤ I_{OUT} ≤ 1.0A		.1	0.5		.1	0.5		.1	0.5	
Output noise voltage	T_A = 25°C 10Hz ≤ f ≤ 100kHz		300			375			375		μV
Long term stability			48			60			60		mV
Ripple rejection	f = 120Hz		-15V ≤ V_{IN} ≤ -25V			18.5V ≤ V_{IN} ≤ -28.5V			-18.5V ≤ V_{IN} ≤ -28.5V		dB
	I_{OUT} = 20mA	54	60		54	60		54	60		
Dropout voltage	T_J = 25°C I_{OUT} = 1.0A		1.1			1.1			1.1		V
Output resistance	f = 1kHz		18			19			19		mΩ
I_{OS}	T_J = 25°C		500			500			500		mA
Peak output current	T_J = 25°C		2.1			2.1			2.1		A
Average temperature coefficient of input voltage	I_{OUT} = 5mA		0°C ≤ T_J ≤ 125°C			0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C		mV/°C
			-0.8			-1.0			-1.0		

NOTE

1. 7900C - 0°C ≤ T_J ≤ 125°C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 500mA, -55°C ≤ T_J ≤ 150°C,[1] C_{IN} = 2μF, C_{OUT} = 1μF unless otherwise specified.

PARAMETER	TEST CONDITIONS	7918			7918C			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OUT}	T_J = 25°C		V_{IN} = -27V			V_{IN} = -27V		V
		-17.3	-18.0	-18.7	-17.3	-18.0	-18.7	
	P ≤ 15W		-22V ≤ V_{IN} ≤ -33V			-21V ≤ V_{IN} ≤ -33V		
	5mA ≤ I_{OUT} ≤ 1.0A	-17.1		-18.9	-17.1		-18.9	
Line regulation	T_J = 25°C		-21V ≤ V_{IN} ≤ -33V			-21V ≤ V_{IN} ≤ -33V		mV
			15	180		15	360	
			-24V ≤ V_{IN} ≤ -30V			-24V ≤ V_{IN} ≤ -30V		
			5	90		5	180	
Load regulation	T_J = 25°C							mV
	5mA ≤ I_{OUT} ≤ 1.5A		12	180		12	360	
	250mA ≤ I_{OUT} ≤ 750mA		4	90		4	180	
I_{CC}	T_J = 25°C		1.5	3.0		1.5	3.0	mA
with line			-22V ≤ V_{IN} ≤ -33V			-21V ≤ V_{IN} ≤ -33V		
				1.0			1.0	
with load	5mA ≤ I_{OUT} ≤ 1.0A		.1	0.5		.1	0.5	
Output noise voltage	T_A = 25°C 10Hz ≤ f ≤ 100kHz		450			450		μV
Long term stability			72			72		mV
Ripple rejection	f = 120Hz		-22V ≤ V_{IN} ≤ -32V			-22V ≤ V_{IN} ≤ -32V		dB
	I_{OUT} = 20mA	54	60		54	60		
Dropout voltage	T_J = 25°C I_{OUT} = 1.0A		1.1			1.1		V
Output resistance	f = 1kHz		22			22		mΩ
I_{OS}	T_J = 25°C		500			500		mA
Peak output current	T_J = 25°C		2.1			2.1		A
Average temperature coefficient of input voltage	I_{OUT} = 5mA		0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C		mV/°C
			-1.0			-1.0		

NOTE

1. 7900C - 0°C ≤ T_J ≤ 125°C

DC ELECTRICAL CHARACTERISTICS

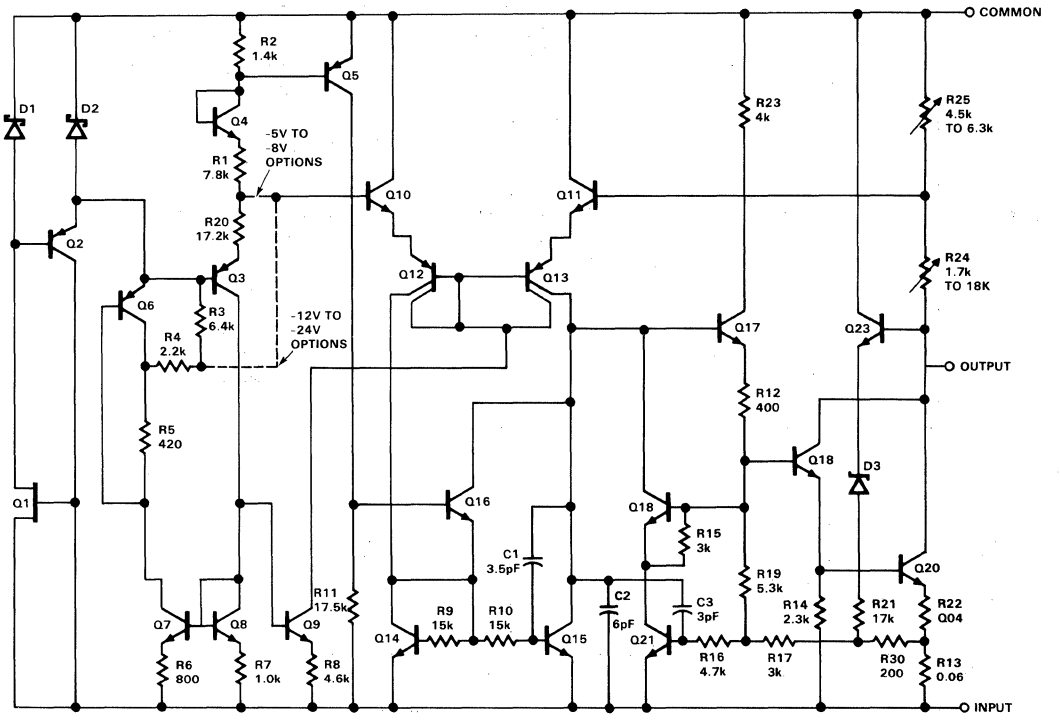
(Cont'd) I_{OUT} = 500mA, -55°C ≤ T_J ≤ 150°C,[1] C_{IN} = 2μF, C_{OUT} = 1μF unless otherwise specified.

PARAMETER	TEST CONDITIONS	7924			7924C			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OUT}	T_J = 25°C		V_{IN} = -33V			V_{IN} = -33V		V
		-23.0	-24.0	-25.0	-23.0	-24.0	-25.0	
	P ≤ 15W		-28V ≤ V_{IN} ≤ -38V			-27V ≤ V_{IN} ≤ -38V		
	5mA ≤ I_{OUT} ≤ 1.0A	-22.8		-25.2	-22.8		-25.2	
Line regulation	T_J = 25°C		-27V ≤ V_{IN} ≤ -38V			-27V ≤ V_{IN} ≤ -38V		mV
			18	240		18	480	
			-30V ≤ V_{IN} ≤ -36V			-30V ≤ V_{IN} ≤ -36V		
			6	120		6	240	
Load regulation	T_J = 25°C							mV
	5mA ≤ I_{OUT} ≤ 1.5A		12	240		120	480	
	250mA ≤ I_{OUT} ≤ 750mA		4	120		4	240	
I_{CC}	T_J = 25°C		1.5	3.0		1.5	3.0	mA
with line			-28V ≤ V_{IN} ≤ -38V			-27V ≤ V_{IN} ≤ -38V		
				1.0			1.0	
with load	5mA ≤ I_{OUT} ≤ 1.0A		0.1	0.5		0.1	0.5	
Output noise voltage	T_A = 25°C							μV
	10Hz ≤ f ≤ 100kHz		600			600		
Long term stability			96			96		mV
Ripple rejection	f = 120Hz		-28V ≤ V_{IN} ≤ -38V			-28V ≤ V_{IN} ≤ -38V		dB
	I_{OUT} = 20mA	54	60		54	60		
Dropout voltage	T_J = 25°C		1.1			1.1		V
	I_{OUT} = 1.0A							
Output resistance	f = 1kHz		28			28		mΩ
I_{OS}	T_J = 25°C		500			500		mA
Peak output current	T_J = 25°C		2.1			2.1		A
Average temperature coefficient of input voltage	I_{OUT} = 5mA		0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C		mV/°C
			-1.0			-1.0		

NOTE

1. 7900C - 0°C ≤ T_J ≤ 125°C

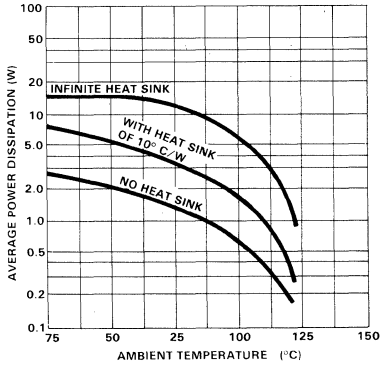
EQUIVALENT CIRCUIT



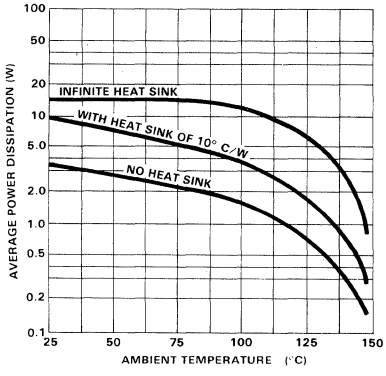
RESISTOR VALUES IN Ω UNLESS OTHERWISE NOTED.

TYPICAL PERFORMANCE CURVES

MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-3, 7900C)

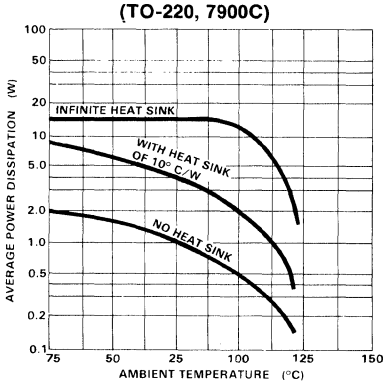


MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-3, 7900)

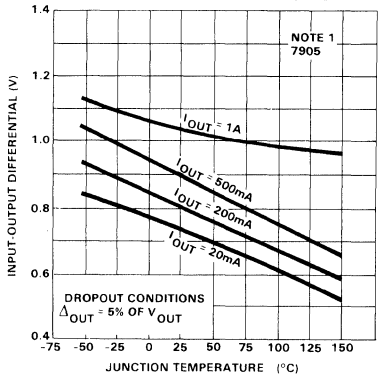


TYPICAL PERFORMANCE CURVES (Cont'd)

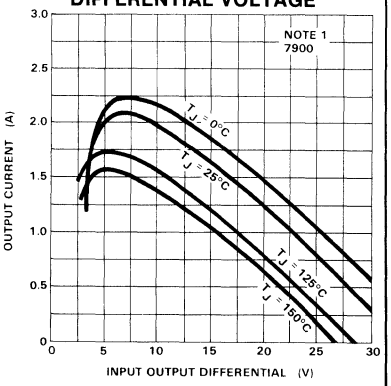
MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-220, 7900C)



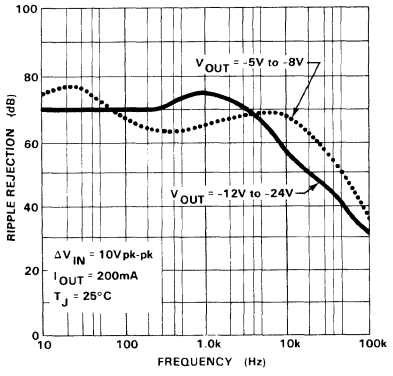
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



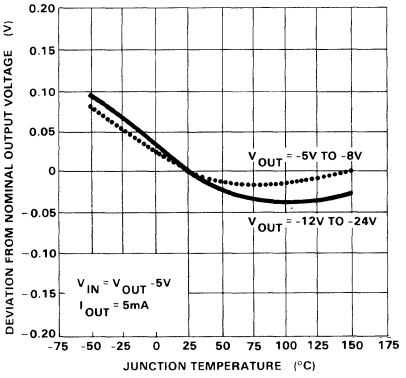
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE



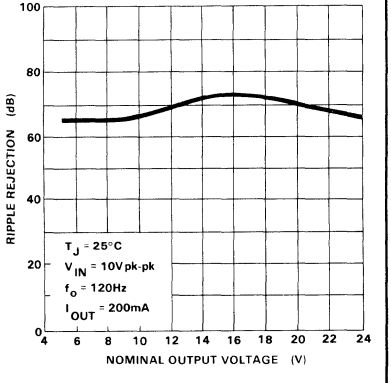
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



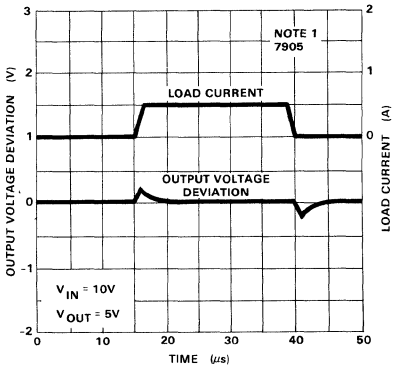
OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



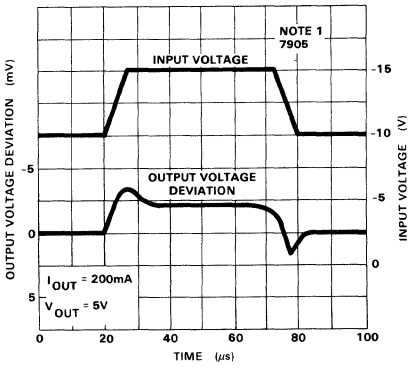
RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES



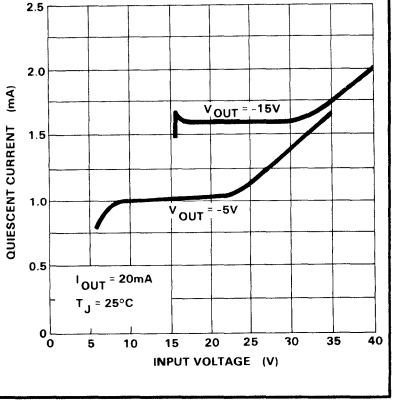
LOAD TRANSIENT RESPONSE



LINE TRANSIENT RESPONSE

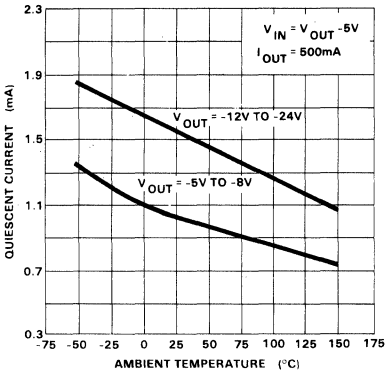


QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE

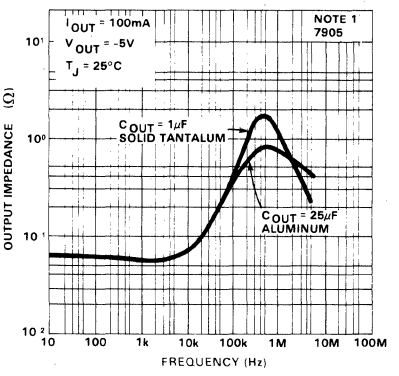


TYPICAL PERFORMANCE CURVES (Cont'd)

QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY



NOTE
The other μA7900 series devices have similar performance curves.

DESCRIPTION

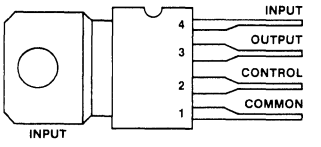
The μA78G and μA79G are Four-Terminal Adjustable Voltage Regulators. They are designed to deliver continuous load currents of up to 1.0A with a maximum input voltage of 40V for the positive regulator 78G and -40V for the negative regulator 79G. Output current capability can be increased to greater than 1.0A through use of one or more external transistors. The output voltage range of the 78G positive voltage regulator is 5V to 30V and the output voltage range of the negative 79G is -30V to -2.2V. For systems requiring both positive and negative voltages, the 78G and 79G are excellent for use as a dual tracking regulator with appropriate external circuitry.

FEATURES

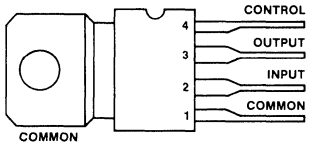
- **Output current in excess of 1.0A**
- **μA78G positive output voltages 5 to 30V**
- **μA79G negative output voltage -30 to -2.2V**
- **Internal thermal overload protection**
- **Internal short circuit current protection**
- **Output transistor safe area protection**
- **Available in 4-Pin TO-202 package**

PIN CONFIGURATIONS

U1 PACKAGE 79G
(Top View)

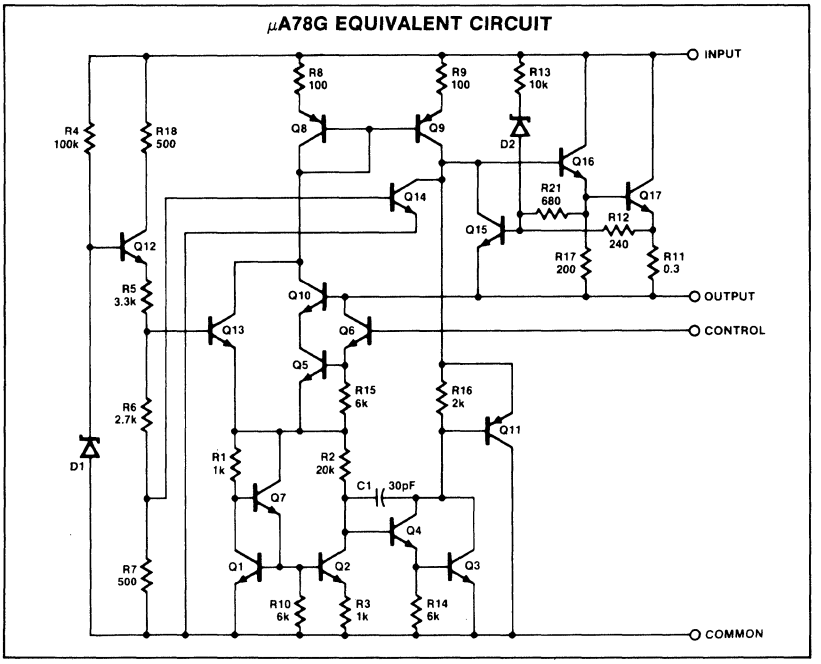


U1 PACKAGE 78G
(Top View)



EQUIVALENT SCHEMATIC

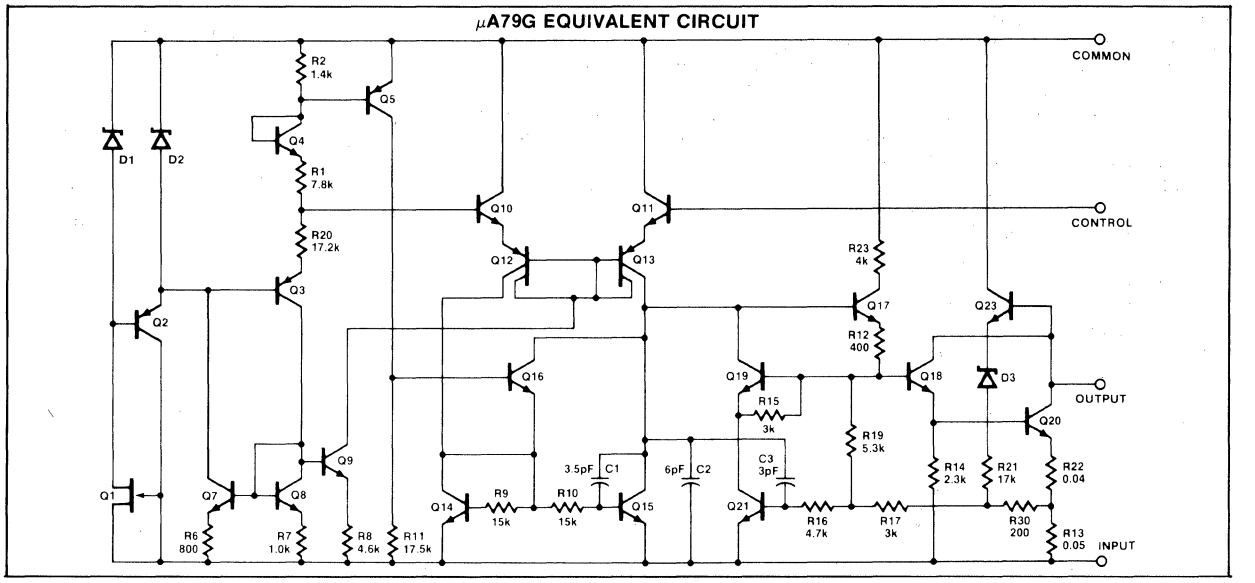
μA78G EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Input voltage		
μA78GC	40	V
μA79GC	-40	V
Control pin voltage		
μA78GC	$0 \le V \le V_{OUT}$	
μA79GC	$-V_{OUT} \le -V \le 0$	
Power dissipation	Internally limited	
Operating junction temperature range		
Commercial (μA78GC, μA79GC)	0 to 150	°C
Storage temperature range		
4-pin power TAB (U1)	-55 to +150	°C
Lead temperature		
4-pin power TAB (U1) (Soldering, 10s)	230	°C

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

μA78GC—0°C ≤ T_J ≤ 125°C, V_{IN} = 10V, I_{OUT} = 500mA, Test circuit 1, unless otherwise specified.[1,2,3]

PARAMETER	TEST CONDITIONS	μA78GC			UNIT
		Min	Typ	Max	
Input voltage range	T_J = 25°C	7.5		40	V
Output voltage range	V_{IN} = V_{OUT} + 5V	5.0		30	V
Output voltage tolerance	(V_{OUT} + 3V) ≤ V_{IN} ≤ (V_{OUT} + 15V), T_J = 25°C			4.0	%V_{OUT}
	5mA ≤ I_{OUT} ≤ I_A				
	P_O ≤ 15W, V_{IN} (MAX) = 38V			5.0	%V_{OUT}
Line regulation	T_J = 25°C, V_{OUT} ≤ 10V				
	(V_{OUT} + 2.5V) ≤ V_{IN} ≤ (V_{OUT} + 20V)			1.0	%V_{OUT}
	T_J = 25°C, V_{OUT} ≥ 10V				
	(V_{OUT} + 3V) ≤ V_{IN} ≤ V_{OUT} + 15V			0.75	%V_{OUT}
	T_J = 25°C, V_{OUT} ≥ 10V				
	(V_{OUT} + 3V) ≤ V_{IN} ≤ V_{OUT} + 7V			0.67	%V_{OUT}
Load regulation	T_J = 25°C, 250mA ≤ I_{OUT} ≤ 750mA				
	V_{IN} = V_{OUT} + 5V			1.0	%V_{OUT}
	T_J = 25°C, V_{IN} = V_{OUT} + 5V				
	5mA ≤ I_{OUT} ≤ 1.5A			2.0	%V_{OUT}
Control pin current	T_J = 25°C		1.0	5.0	μA
				8.0	μA
Quiescent current	T_J = 25°C		3.2	5.0	mA
				6.0	mA
Ripple rejection	8V ≤ V_{IN} ≤ 18V, f = 120Hz				
	V_{OUT} = 5V	62	78		dB
Output noise voltage	T_J = 25°C,				
	10Hz ≤ f ≤ 100kHz, V_{OUT} = 5V		40		μV
Dropout voltage				2.5	V
Short circuit current	T_J = 25°C, V_{IN} = 30V		750		mA
Peak output current	T_J = 25°C		2.2		A
Temperature coefficient of V_{OUT}	V_{OUT} = 5V, I_{OUT} = 5mA		-1.1		mV/°C
Control pin voltage (reference)	T_J = 25°C	4.8	5.0	5.2	V
		4.75		5.25	V

DC ELECTRICAL CHARACTERISTICS

μA79GC—0°C ≤ T_J ≤ 125°C, V_{IN} = -10V, I_{OUT} = 500mA, Test circuit 2, unless otherwise specified[1,2,3]

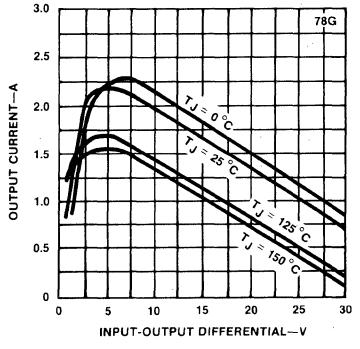
PARAMETER	TEST CONDITIONS	μA79GC			UNIT
		Min	Typ	Max	
Input voltage range	T_J = 25°C	-40		-7.0	V
Output voltage range	V_{IN} = V_{OUT} -5V	-30		-2.23	V
Output voltage tolerance	(V_{OUT} -15V) ≤ V_{IN} ≤ (V_{OUT} -3V), T_J = 25°C			4.0	%(V_{OUT})
Line regulation	5mA ≤ I_{OUT} ≤ 1A, P_D ≤ 15W, V_{IN} (MAX) = -38V			5.0	%(V_{OUT})
	T_J = 25°C, V_{OUT} ≥ -10V, (V_{OUT} -20V) ≤ V_{IN} ≤ (V_{OUT} -2.5V)			1.0	%(V_{OUT})
	T_J = 25°C, V_{OUT} ≤ -10V, (V_{OUT} -15V) ≤ V_{IN} ≤ (V_{OUT} -3V)			0.75	%(V_{OUT})
Load regulation	T_J = 25°C, V_{OUT} ≤ -10V, (V_{OUT} -7V) ≤ V_{IN} ≤ (V_{OUT} -3V)			0.67	%(V_{OUT})
	T_J = 25°C, V_{IN} = V_{OUT} -5V, 250mA ≤ I_{OUT} ≤ 750mA			1.0	%(V_{OUT})
	T_J = 25°C, V_{IN} = V_{OUT} -5V, 5mA ≤ I_{OUT} ≤ 1.5A			2.0	%(V_{OUT})
Control pin current	T_J = 25°C		0.4	2.0 3.0	μA μA
Quiescent current	T_J = 25°C		.5	1.5 2.0	mA mA
Ripple rejection	-18V ≤ V_{IN} ≤ -8V, V_{OUT} = -5V, f = 120Hz	50	60		dB
Output noise voltage	T_J = 25°C, 10Hz ≤ f ≤ 100kHz, V_{OUT} = -5V		125		μV
Dropout voltage				2.3	V
Short circuit current	T_J = 25°C, V_{IN} = -30V		500		mA
Peak output current	T_J = 25°C		2.2		A
Temperature coefficient of output voltage	V_{OUT} = -5V, I_{OUT} = 5mA		-0.4		mV/°C
Control pin voltage (reference)	T_J = 25°C	-2.32 -2.35	-2.23	-2.14 -2.11	V V

NOTES

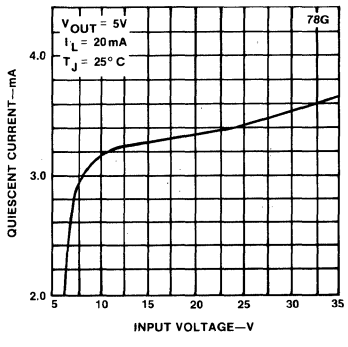
1. V_{OUT} is defined for the 78GC as $V_{OUT} = \frac{R1 + R2}{R2}$ (5.0); The 79GC as $V_{OUT} = \frac{R1 + R2}{R2}$ (-2.23).
2. Dropout voltage is defined as that input-output voltage differential which causes the output voltage to decrease by 5% of its initial value.
3. The convention for negative is the algebraic value, thus -15 is less than -10V.

TYPICAL PERFORMANCE CHARACTERISTICS

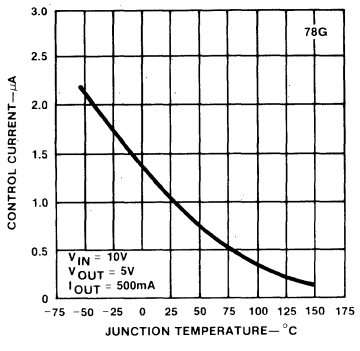
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE



QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE

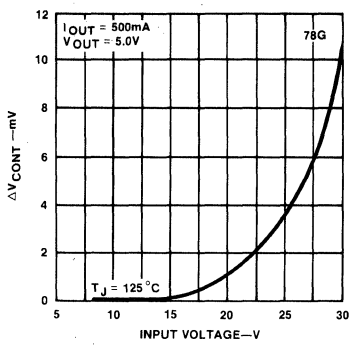


CONTROL CURRENT AS A FUNCTION OF TEMPERATURE

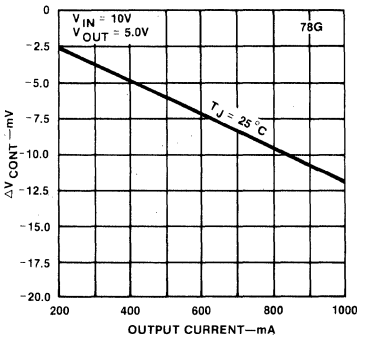


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

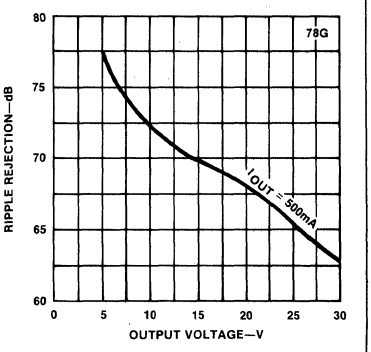
DIFFERENTIAL CONTROL VOLTAGE AS A FUNCTION OF INPUT VOLTAGE



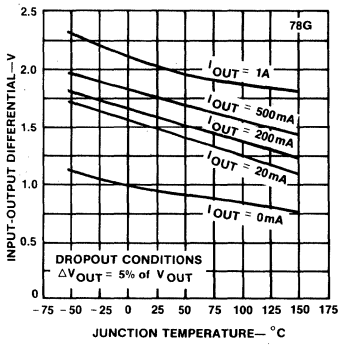
DIFFERENTIAL CONTROL VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



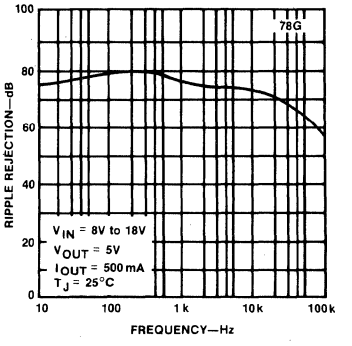
RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGE



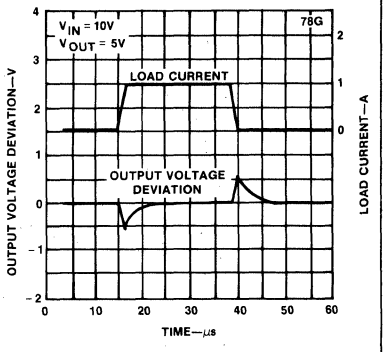
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



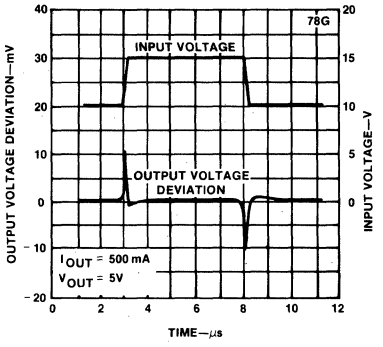
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



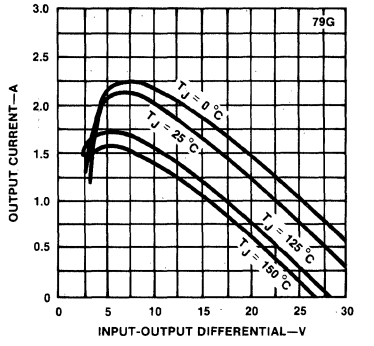
LOAD TRANSIENT RESPONSE



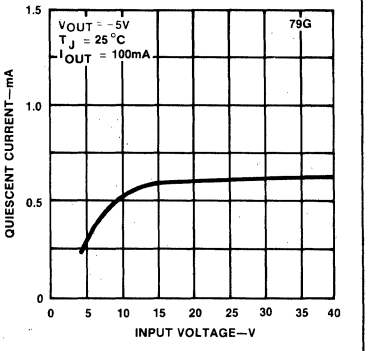
LINE TRANSIENT RESPONSE



PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE

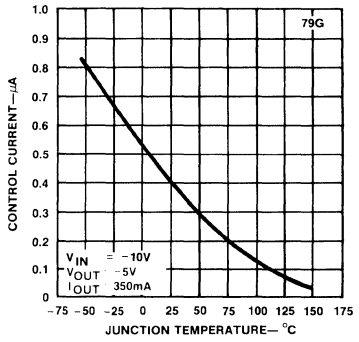


QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE

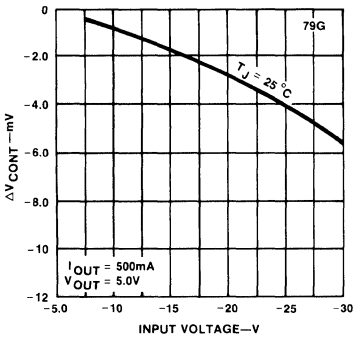


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

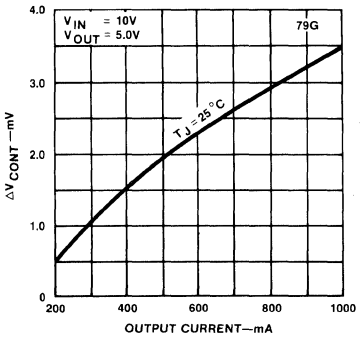
CONTROL CURRENT AS A FUNCTION OF TEMPERATURE



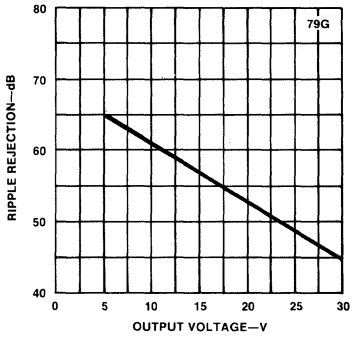
DIFFERENTIAL CONTROL VOLTAGE AS A FUNCTION OF INPUT VOLTAGE



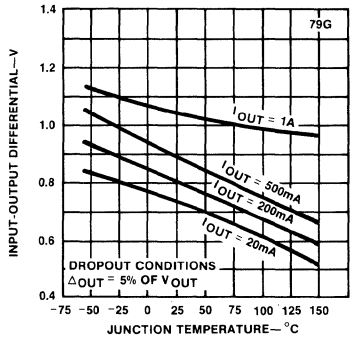
DIFFERENTIAL CONTROL VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



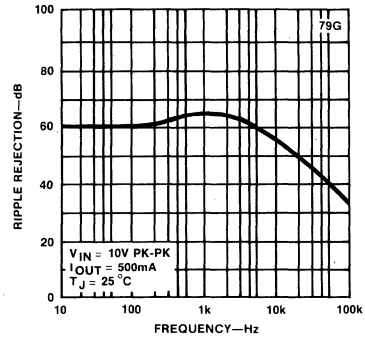
RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGE



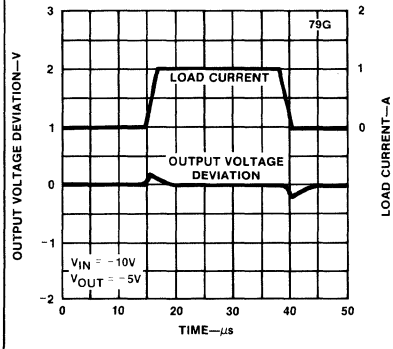
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



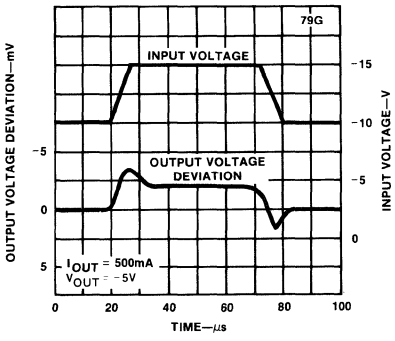
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



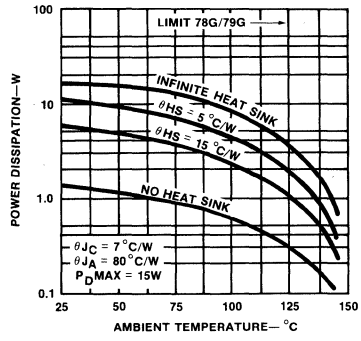
LOAD TRANSIENT RESPONSE



LINE TRANSIENT RESPONSE



μA78G AND μA79G POWER TAB (U1) PACKAGE WORST CASE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



DESCRIPTION

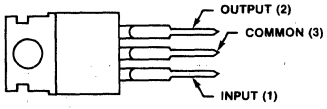
The 78HV00 series of monolithic Three-Terminal Positive Voltage Regulators employ 60 volt input breakdown, thermal shutdown and safe-area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current, (78HV00 series) and 500mA (78MHV00 series). They are intended as fixed-voltage regulators in a wide range of applications including local, on-card regulation for elimination of distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power pass element in precision regulators.

FEATURES

- **Input voltage greater than 60 volts**
- **No external components**
- **Internal thermal overload protection**
- **Internal short circuit current limiting**
- **Output transistor safe-area compensation**
- **Available in the TO-220, the TO-3, and the TO-39 package**
- **Output voltages of 5, 6, 8, 12, 13.8, 15, 18, and 24 volts**

PIN CONFIGURATIONS

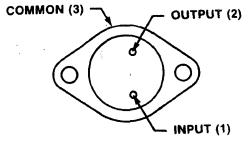
U PACKAGE (TO-220)



ORDER INFORMATION

OUTPUT VOLTAGE	ORDER PART NO.
5V	78HV05CU/SA78HV05CU
6V	78HV06CU/SA78HV06CU
8V	78HV08CU/SA78HV08CU
12V	78HV12CU/SA78HV12CU
13.8V	78HV14CU/SA78HV14CU
15V	78HV15CU/SA78HV15CU
18V	78HV18CU/SA78HV18CU
24V	78HV24CU/SA78HV24CU
5V	78MHV05CU/SA78MHV05CU
6V	78MHV06CU/SA78MHV06CU
8V	78MHV08CU/SA78MHV08CU
12V	78MHV12CU/SA78MHV12CU
15V	78MHV15CU/SA78MHV15CU
18V	78MHV18CU/SA78MHV18CU
24V	78MHV24CU/SA78MHV24CU

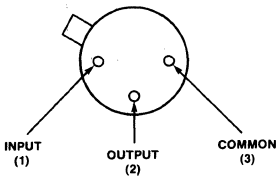
DA PACKAGE (TO-3)



ORDER INFORMATION

OUTPUT VOLTAGE	ORDER PART NO.
5V	78HV05DA
6V	78HV06DA
8V	78HV08DA
12V	78HV12DA
13.8V	78HV14DA
15V	78HV15DA
18V	78HV18DA
24V	78HV24DA
5V	78HV05CDA/SA78HV05CDA
6V	78HV06CDA/SA78HV06CDA
8V	78HV08CDA/SA78HV08CDA
12V	78HV12CDA/SA78HV12CDA
13.8V	78HV14CDA/SA78HV14CDA
15V	78HV15CDA/SA78HV15CDA
18V	78HV18CDA/SA78HV18CDA
24V	78HV24CDA/SA78HV24CDA

DB PACKAGE (TO-39)



ORDER INFORMATION

OUTPUT VOLTAGE	ORDER PART NO.
5V	78MHV05DB
6V	78MHV06DB
8V	78MHV08DB
12V	78MHV12DB
15V	78MHV15DB
20V	78MHV20DB
24V	78MHV24DB
5V	78MHV05CBD/SA78MHV05CDB
6V	78MHV06CDB/SA78MHV06CDB
8V	78MHV08CDB/SA78MHV08CDB
12V	78MHV12CDB/SA78MHV12CDB
15V	78MHV15CDB/SA78MHV15CDB
20V	78MHV20CDB/SA78MHV20CDB
24V	78MHV24CDB/SA78MHV24CDB

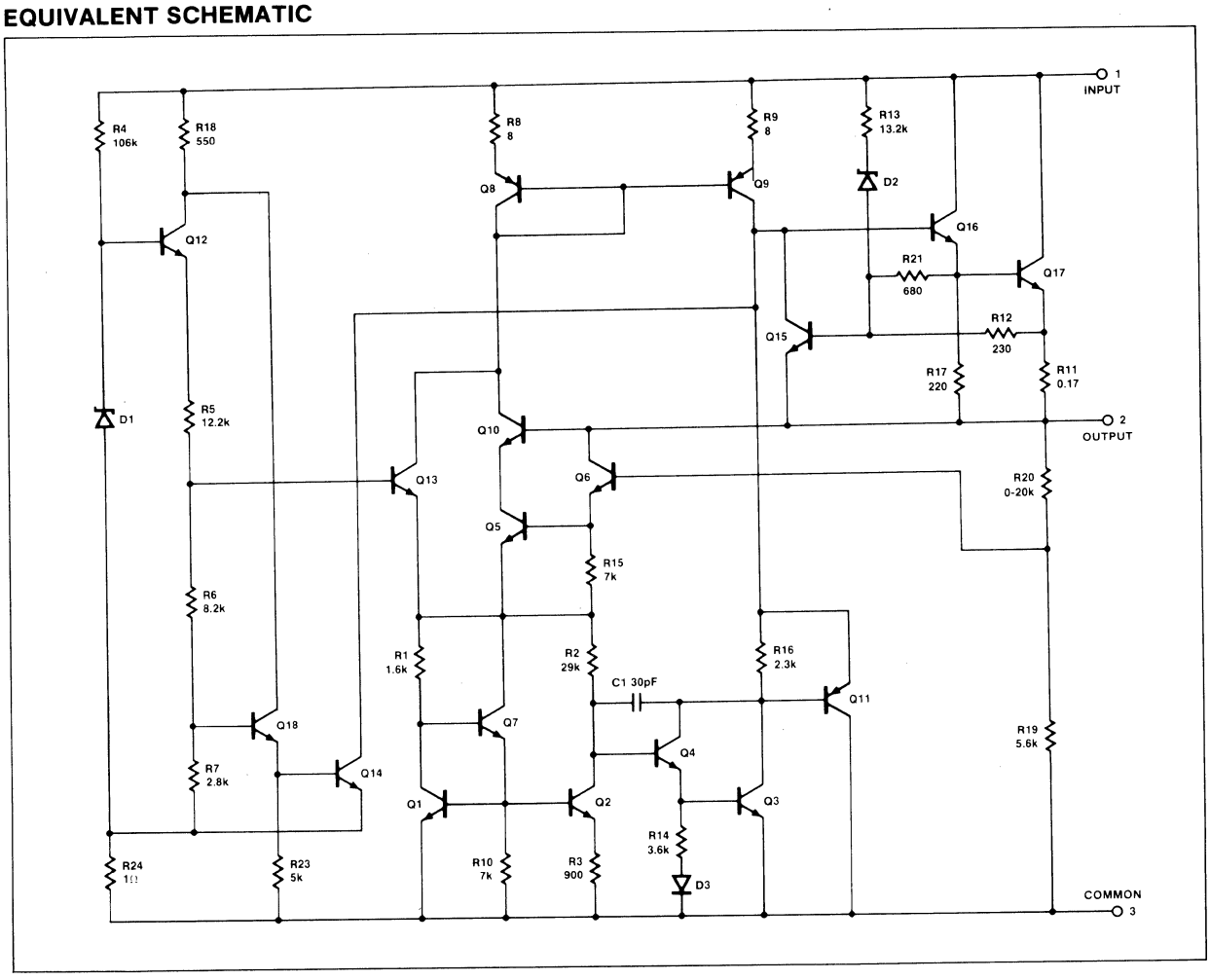
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Input voltage (5V through 24V)	60	V
Internal power dissipation[1]	Internally limited	
Storage temperature range	-65 to +150	°C
Operating junction temperature range[2]		
78HV00, 78MHV00	-55 to +150	°C
78HV00C, 78MHV00C	0 to +125	°C
SA78HV00C, SA78MHV00C	-40 to +125	°C
Lead temperature		
TO-3 package (soldering, 60 second time limit)	300	°C
TO-220 package (soldering, 10 second time limit)	230	°C

NOTES

1. Thermal resistance of the packages (without a heat sink)
   Junction to case: TO-3 package 4°C/W; TO-220 package 2°C/W, TO-39 package 20°C/W
   Junction to ambient: TO-3 package 35°C/W; TO-220 package 50°C/W, TO-39 package 170°C/W
2. Operating ambient temperature range
   78HV00 -55°C to +125°C
   78HV00C 0°C to +85°C
   SA78HV00C -40°C to +85°C

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS

I_{OUT} = 500mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	78HV05[1]			78HV05C[1]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 10V			V_{IN} = 10V		
			4.8	5.0	5.2	4.8	5.0	5.2	V
		Over temp.,[1] 5mA ≤ I_{OUT} ≤ 1.0A, P_D ≤ 15W		8V ≤ V_{IN} ≤ 20V			7V ≤ V_{IN} ≤ 25V		
			4.65		5.35	4.75		5.25	V
	Line regulation			7V ≤ V_{IN} ≤ 25V			7V ≤ V_{IN} ≤ 25V		
				3	50		3	100	mV
				8V ≤ V_{IN} ≤ 12V			8V ≤ V_{IN} ≤ 12V		
				1	25		1	50	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 1.5A		15	50		15	100	mV
		250mA ≤ I_{OUT} ≤ 750mA		5	25		5	50	mV
I_{CC}				4.2	6.0		4.2	8.0	mA
ΔI_{CC}				8V ≤ V_{IN} ≤ 25V			7V ≤ V_{IN} ≤ 25V		
		Over temp.,[1] with line			0.8			1.3	mA
		With load, 5mA ≤ I_{OUT} ≤ 1.0A			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		40			40		μV
	Voltage drift	mV/1000hrs.			20			20	mV
				8V ≤ V_{IN} ≤ 18V			8V ≤ V_{IN} ≤ 18V		
	Ripple rejection	Over temp.,[1] f = 120Hz	68	78		62	78		dB
	Dropout voltage	I_{OUT} = 1.0A		2.0			2.0		V
	Output resistance	f = 1kHz		17			17		mΩ
I_{SC}				750			750		mA
	Peak output current			2.2			2.2		A
V_{OUT}	Output temperature drift	I_{OUT} = 5mA		0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C		
				-1.1			-1.1		mV/°C

NOTES

1. -55°C ≤ T_J ≤ 150°C for 78HV00
   0°C ≤ T_J ≤ 125°C for 78HV00C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 500mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	78HV06[1]			78HV06C[1]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 11V			V_{IN} = 11V		
			5.75	6.0	6.25	5.75	6.0	6.25	V
		Over temp.,[1] 5mA ≤ I_{OUT} ≤ 1.0A,		9V ≤ V_{IN} ≤ 21V			8V ≤ V_{IN} ≤ 21V		
		P_D ≤ 15W	5.65		6.35	5.7		6.3	V
	Line regulation			8V ≤ V_{IN} ≤ 25V			8V ≤ V_{IN} ≤ 25V		
				5	60		5	120	mV
				9V ≤ V_{IN} ≤ 13V			9V ≤ V_{IN} ≤ 13V		
				1.5	30		1.5	60	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 1.5A		14	60		14	120	mV
		250mA ≤ I_{OUT} ≤ 750mA		4	30		4	60	mV
I_{CC}				4.3	6.0		4.3	8.0	mA
ΔI_{CC}				9V ≤ V_{IN} ≤ 25V			8V ≤ V_{IN} ≤ 25V		
		Over temp.,[1] with line			0.8			1.3	mA
		With load, 5mA ≤ I_{OUT} ≤ 1.0A			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		45			45		μV
	Voltage drift	mV/1000hrs.			24			24	mV
				9V ≤ V_{IN} ≤ 19V			9V ≤ V_{IN} ≤ 19V		
	Ripple rejection	Over temp.,[1] f = 120Hz	65	75		59	75		dB
	Dropout voltage	I_{OUT} = 1.0A		2.0			2.0		V
	Output resistance	f = 1kHz		19			19		mΩ
I_{SC}				550			550		mA
	Peak output current			2.2			2.2		A
V_{OUT}	Output temperature drift	I_{OUT} = 5mA		0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C		
				-0.8			-0.8		mV/°C

NOTES

1. -55°C ≤ T_J ≤ 150°C for 78HV00
   0°C ≤ T_J ≤ 125°C for 78HV00C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 500mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	78HV08[1]			78HV08C[1]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 14V			V_{IN} = 14V		
			7.7	8.0	8.3	7.7	8.0	8.3	V
		Over temp.,[1] 5mA ≤ I_{OUT} ≤ 1.0A, P_D ≤ 15W		11.5V ≤ V_{IN} ≤ 23V			10.5V ≤ V_{IN} ≤ 23V		
			7.6		8.4	7.6		8.4	V
	Line regulation			10.5 ≤ V_{IN} ≤ 25V			10.5V ≤ V_{IN} ≤ 25V		
				6	80		6	160	mV
				11V ≤ V_{IN} ≤ 17V			11V ≤ V_{IN} ≤ 17V		
				2	40		2	80	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 1.5A		12	80		12	160	mV
		250mA ≤ I_{OUT} ≤ 750mA		4	40		4	80	mV
I_{CC}				4.3	6.0		4.3	8.0	mA
ΔI_{CC}				11.5V ≤ V_{IN} ≤ 25V			10.5V ≤ V_{IN} ≤ 25V		
		Over temp.,[1] with line			0.8			1.0	mA
		With load, 5mA ≤ I_{OUT} ≤ 1.0A			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		52			52		μV
	Voltage drift	mV/1000hrs.			32			32	mV
				11.5V ≤ V_{IN} ≤ 21.5V			11.5V ≤ V_{IN} ≤ 21.5V		
	Ripple rejection	Over temp.,[1] f = 120Hz	62	72		56	72		dB
	Dropout voltage	I_{OUT} = 1.0A		2.0			2.0		V
	Output resistance	f = 1kHz		16			16		mΩ
I_{SC}				450			450		mA
	Peak output current			2.2			2.2		A
V_{OUT}	Output temperature drift	I_{OUT} = 5mA		0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C		
				-0.8			-0.8		mV/°C

NOTES

1. -55°C ≤ T_J ≤ 150°C for 78HV00
   0°C ≤ T_J ≤ 125°C for 78HV00C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 500mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	78HV12[1]			78HV12C[1]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 19V			V_{IN} =19V		
			11.5	12.0	12.5	11.5	12.0	12.5	V
		Over temp.,[1] 5mA ≤ I_{OUT} ≤ 1.0A, P_D ≤ 15W		15.5V ≤ V_{IN} ≤ 27V			14.5V ≤ V_{IN} ≤ 27V		
			11.4		12.6	11.4		12.6	V
	Line regulation			14.5V ≤ V_{IN} ≤ 30V			14.5V ≤ V_{IN} ≤ 30V		
				10	120		10	240	mV
				16V ≤ V_{IN} ≤ 22V			16V ≤ V_{IN} ≤ 22V		
				3	60		3	120	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 1.5A		12	120		12	240	mV
		250mA ≤ I_{OUT} ≤ 750mA		4	60		4	120	mV
I_{CC}				4.3	6.0		4.3	8.0	mA
ΔI_{CC}				15V ≤ V_{IN} ≤ 30V			14.5V ≤ V_{IN} ≤ 30V		
		Over temp.,[1] with line			0.8			1.0	mA
		With load, 5mA ≤ I_{OUT} ≤ 1.0A			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		75			75		μV
	Voltage drift	mV/1000hrs.			48			48	mV
	Ripple rejection	Over temp.,[1] f = 120Hz	61	15V ≤ V_{IN} ≤ 25V 71		55	15V ≤ V_{IN} ≤ 25V 71		dB
	Dropout voltage	I_{OUT} = 1.0A		2.0			2.0		V
	Output resistance	f = 1kHz		18			18		mΩ
I_{SC}				350			350		mA
	Peak output current			2.2			2.2		A
V_{OUT}	Output temperature drift	I_{OUT} = 5mA		0°C ≤ T_J ≤ 150°C -1.0			0°C ≤ T_J ≤ 125°C -1.0		mV/°C

NOTES

1. -55°C ≤ T_J ≤ 150°C for 78HV00
   0°C ≤ T_J ≤ 125°C for 78HV00C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 500mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	78HV14[1]			78HV14C[1]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage		V_{IN} = 22V			V_{IN} = 22V			
			13.3	13.8	14.3	13.3	13.8	14.3	V
		Over temp.,[1] 5mA ≤ I_{OUT} ≤ 1.0A, P_D ≤ 15W	17.5V ≤ V_{IN} ≤ 29V			16.5V ≤ V_{IN} ≤ 29V			
			13.15		14.45	13.15		14.95	V
	Line regulation		16.5V ≤ V_{IN} ≤ 30V			16.5V ≤ V_{IN} ≤ 30V			
				10	140		10	280	mV
			19V ≤ V_{IN} ≤ 25V			19V ≤ V_{IN} ≤ 25V			
				3	70		3	140	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 1.5A		12	140		12	280	mV
		250mA ≤ I_{OUT} ≤ 750mA		4	70		4	140	mV
I_{CC}				4.3	6.0		4.3	8.0	mA
ΔI_{CC}			17V ≤ V_{IN} ≤ 30V			16.5V ≤ V_{IN} ≤ 30V			
		Over temp.,[1] with line			0.8			1.0	mA
		With load, 5mA ≤ I_{OUT} ≤ 1.0A			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		85			85		μV
	Voltage drift	mV/1000hrs.			56			56	mV
			17V ≤ V_{IN} ≤ 27V			17V ≤ V_{IN} ≤ 27V			
	Ripple rejection	Over temp.,[1] f = 120Hz	54	70		60	70		dB
	Dropout voltage	I_{OUT} = 1.0A		2.0			2.0		V
	Output resistance	f = 1kHz		18			18		mΩ
I_{SC}				350			350		mA
	Peak output current			2.2			2.2		A
V_{OUT}	Output temperature drift	I_{OUT} = 5mA	0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C			
				-1.0			-1.0		mV/°C

NOTES

1. -55°C ≤ T_J ≤ 150°C for 78HV00
   0°C ≤ T_J ≤ 125°C for 78HV00C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 500mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	78HV15[1]			78HV15C[1]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage		V_{IN} = 23V			V_{IN} = 23V			
			14.4	15.0	15.6	14.4	15.0	15.6	V
		Over temp.,[1] 5mA ≤ I_{OUT} ≤ 1.0A, P_D ≤ 15W	18.5V ≤ V_{IN} ≤ 30V			17.5V ≤ V_{IN} ≤ 30V			
			14.25		15.75	14.25		15.75	V
	Line regulation		17.5V ≤ V_{IN} ≤ 30V			17.5V ≤ V_{IN} ≤ 30V			
				11	150		11	300	mV
			20V ≤ V_{IN} ≤ 26V			20V ≤ V_{IN} ≤ 26V			
				3	75		3	150	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 1.5A		12	150		12	300	mV
		250mA ≤ I_{OUT} ≤ 750mA		4	75		4	150	mV
I_{CC}				4.4	6.0		4.4	8.0	mA
ΔI_{CC}			18.5V ≤ V_{IN} ≤ 30V			17.5V ≤ V_{IN} ≤ 30V			
		Over temp.,[1] with line			0.8			1.0	mA
		With load, 5mA ≤ I_{OUT} ≤ 1.0A			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		90			90		μV
	Voltage drift	mV/1000hrs.			60			60	mV
			18.5V ≤ V_{IN} ≤ 28.5V			18.5V ≤ V_{IN} ≤ 28.5V			
	Ripple rejection	Over temp.,[1] f = 120Hz	60	70		54	70		dB
	Dropout voltage	I_{OUT} = 1.0A		2.0			2.0		V
	Output resistance	f = 1kHz		19			19		mΩ
I_{SC}				230			230		mA
	Peak output current			2.1			2.1		A
V_{OUT}	Output temperature drift	I_{OUT} = 5mA	0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C			
				-1.0			-1.0		mV/°C

NOTES

1. -55°C ≤ T_J ≤ 150°C for 78HV00
   0°C ≤ T_J ≤ 125°C for 78HV00C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 500mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	78HV18[1]			78HV18C[1]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 27V			V_{IN} = 27V		
			17.3	18.0	18.7	17.3	18.0	18.7	V
		Over temp.,[1] 5mA ≤ I_{OUT} ≤ 1.0A, P_D ≤ 15W		22V ≤ V_{IN} ≤ 33V			21V ≤ V_{IN} ≤ 33V		
			17.1		18.9	17.1		18.9	V
	Line regulation			21V ≤ V_{IN} ≤ 33V			21V ≤ V_{IN} ≤ 33V		
				15	180		15	360	mV
				24V ≤ V_{IN} ≤ 30V			24V ≤ V_{IN} ≤ 30V		
				5	90		5	180	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 1.5A		12	180		12	360	mV
		250mA ≤ I_{OUT} ≤ 750mA		4	90		4	180	mV
I_{CC}				4.5	6.0		4.5	8.0	mA
ΔI_{CC}				22V ≤ V_{IN} ≤ 33V			21V ≤ V_{IN} ≤ 33V		
		Over temp.,[1] with line			0.8			1.0	mA
		With load, 5mA ≤ I_{OUT} ≤ 1.0A			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		110			110		μV
	Voltage drift	mV/1000hrs.			72			72	mV
				22V ≤ V_{IN} ≤ 32V			22V ≤ V_{IN} ≤ 32V		
	Ripple rejection	Over temp.,[1] f = 120Hz	59	69		53	69		dB
	Dropout voltage	I_{OUT} = 1.0A		2.0			2.0		V
	Output resistance	f = 1kHz		22			22		mΩ
I_{SC}				200			200		mA
	Peak output current			2.1			2.1		A
V_{OUT}	Output temperature drift	I_{OUT} = 5mA		0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C		
				-1.0			-1.0		mV/°C

NOTES

1. -55°C ≤ T_J ≤ 150°C for 78HV00
   0°C ≤ T_J ≤ 125°C for 78HV00C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 500mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	78HV24[1]			78HV24C[1]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 33V			V_{IN} = 33V		
			23.0	24.0	25.0	23.0	24.0	25.0	V
		Over temp.,[1] 5mA ≤ I_{OUT} ≤ 1.0A, P_D ≤ 15W		28V ≤ V_{IN} ≤ 38V			28V ≤ V_{IN} ≤ 38V		
			22.8		25.2	22.8		25.2	V
	Line regulation			27V ≤ V_{IN} ≤ 38V			27V ≤ V_{IN} ≤ 38V		
				18	240		18	480	mV
				30V ≤ V_{IN} ≤ 36V			30V ≤ V_{IN} ≤ 36V		
				6	120		6	240	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 1.5A		12	240		12	480	mV
		250mA ≤ I_{OUT} ≤ 750mA		4	120		4	240	mV
I_{CC}				4.6	6.0		4.6	8.0	mA
ΔI_{CC}				28V ≤ V_{IN} ≤ 38V			27V ≤ V_{IN} ≤ 38V		
		Over temp.,[1] with line			0.8			1.0	mA
		With load, 5mA ≤ I_{OUT} ≤ 1.0A			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		170			170		μV
	Voltage drift	mV/1000hrs.			96			96	mV
				28V ≤ V_{IN} ≤ 38V			28V ≤ V_{IN} ≤ 38V		
	Ripple rejection	Over temp.,[1] f = 120Hz	56	66		50	66		dB
	Dropout voltage	I_{OUT} = 1.0A		2.0			2.0		V
	Output resistance	f = 1kHz		28			28		mΩ
I_{SC}				150			150		mA
	Peak output current			2.1			2.1		A
V_{OUT}	Output temperature drift	I_{OUT} = 5mA		0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C		
				-1.5			-1.5		mV/°C

NOTES

1. -55°C ≤ T_J ≤ 150°C for 78HV00
   0°C ≤ T_J ≤ 125°C for 78HV00C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 500mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	SA78HV05C[2]			SA78HV06C[2]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage	Over temp.,[2] 5mA ≤ I_{OUT} ≤ 1.0A, P_D ≤ 15W		V_{IN} = 10V			V_{IN} = 11V		
			4.8	4.0	5.2	5.75	6.0	6.25	V
				7V ≤ V_{IN} ≤ 25V			8V ≤ V_{IN} ≤ 25V		
			4.65		5.35	5.65		6.35	V
	Line regulation			7V ≤ V_{IN} ≤ 25V			8V ≤ V_{IN} ≤ 25V		
				3	100		5	120	mV
				8V ≤ V_{IN} ≤ 12V			9V ≤ V_{IN} ≤ 13V		
				1	50		1.5	60	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 1.5A		15	100		14	120	mV
		250mA ≤ I_{OUT} ≤ 750mA		5	50		4	60	mV
I_{CC}				4.2	8.0		4.3	8.0	mA
ΔI_{CC}				7V ≤ V_{IN} ≤ 25V			8V ≤ V_{IN} ≤ 25V		
		Over temp.,[2] with line		0.8			0.8		mA
		With load, 5mA ≤ I_{OUT} ≤ 1.0A		0.3			0.3		mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		40			45		μV
	Voltage drift	mV/1000hrs.			20			24	mV
	Ripple rejection	Over temp.,[2] f = 120Hz		8V ≤ V_{IN} ≤ 18V			9V ≤ V_{IN} ≤ 19V		
			62	78		59	75		dB
	Dropout voltage	I_{OUT} = 1.0A		2.0			2.0		V
	Output resistance	f = 1kHz		17			19		mΩ
I_{SC}				750			550		mA
	Peak output current			2.2			2.2		A
V_{OUT}	Output temperature drift	0°C ≤ T_J ≤ 125°C, I_{OUT} = 5mA		-1.1			-0.8		mV/°C

NOTES
2. -40°C ≤ T_J ≤ +125°C for SA78HV00C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 500mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	SA78HV08C[2]			SA78HV12C[2]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 14V			V_{IN} = 19V		
			7.7	8.0	8.3	11.5	12.0	12.5	V
		Over temp.,[2] 5mA ≤ I_{OUT} ≤ 1.0A,		10.5V ≤ V_{IN} ≤ 23V			14.5V ≤ V_{IN} ≤ 27V		
		P_D ≤ 15W	7.6		8.4	11.4		12.6	V
				10.5V ≤ V_{IN} ≤ 25V			14.5V ≤ V_{IN} ≤ 30V		
	Line regulation			6	160		10	240	mV
				11V ≤ V_{IN} ≤ 17V			16V ≤ V_{IN} ≤ 22V		
				2	80		3	120	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 1.5A		12	160		12	240	mV
		250mA ≤ I_{OUT} ≤ 750mA		4	80		4	120	mV
I_{CC}				4.3	8.0		4.3	8.0	mA
				10.5V ≤ V_{IN} ≤ 25V			14.5V ≤ V_{IN} ≤ 30V		
ΔI_{CC}		Over temp.,[2] with line		0.8			0.8		mA
		With load, 5mA ≤ I_{OUT} ≤ 1.0A		0.3			0.3		mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		52			75		μV
	Voltage drift	mV/1000hrs.			32			48	mV
				11.5V ≤ V_{IN} ≤ 21.5V			15V ≤ V_{IN} ≤ 25V		
	Ripple rejection	Over temp.,[2] f = 120Hz	56	72		61	71		dB
	Dropout voltage	I_{OUT} = 1.0A		2.0			2.0		V
	Output resistance	f = 1kHz		16			18		mΩ
I_{SC}				450			350		mA
	Peak output current			2.2			2.2		A
V_{OUT}	Output temperature drift	0°C ≤ T_J ≤ 125°C, I_{OUT} = 5mA		-0.8			-1.0		mV/°C

NOTES
2. -40°C ≤ T_J ≤ +125°C for SA78HV00C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 5mA C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER	TEST CONDITIONS	SA78HV14C[2]			SA78HV15C[2]			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OUT} Output voltage			V_{IN} = 22V			V_{IN} = 23V		
	Over temp.,[2] 5mA ≤ I_{OUT} ≤ 1.0A, P_D ≤ 15W	13.3	13.8	14.3	14.4	15.0	15.6	V
			16.5V ≤ V_{IN} ≤ 29V			17.5V ≤ V_{IN} ≤ 30V		
		13.15		14.95	14.25		15.75	V
	Line regulation		16.5V ≤ V_{IN} ≤ 30V			17.5V ≤ V_{IN} ≤ 30V		
			10	280		11	300	mV
			19V ≤ V_{IN} ≤ 25V			20V ≤ V_{IN} ≤ 26V		
			3	140		3	150	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 1.5A	12	280		12	150	mV
		250mA ≤ I_{OUT} ≤ 750mA	4	140		4	75	mV
I_{CC}			4.3	8.0		4.4	8.0	mA
I_{CC}			16.5V ≤ V_{IN} ≤ 30V			17.5V ≤ V_{IN} ≤ 30V		
	Over temp.,[2] with line		0.8			0.8		mA
	With load, 5mA ≤ I_{OUT} ≤ 1.0A		0.3			0.3		mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz	85			90		μV
	Voltage drift	mV/1000hrs.		56			60	mV
	Ripple rejection	Over temp.,[2] f = 120Hz	17V ≤ V_{IN} ≤ 27V			18.5V ≤ V_{IN} ≤ 28.5V		
			60	70		60	70	dB
	Dropout voltage	I_{OUT} = 1.0A	2.0			2.0		V
	Output resistance	f = 1kHz	18			19		mΩ
I_{SC}			350			230		mA
	Peak output current		2.2			2.1		A
V_{OUT} Output temperature drift	0°C ≤ T_J ≤ 125°C, I_{OUT} = 5mA		-1.0			-1.0		mV/°C

NOTES
2. -40°C ≤ T_J ≤ +125°C for SA78HV00C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 5mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	SA78HV18C[2]			SA78HV24C[2]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 27V			V_{IN} = 33V		
		Over temp.,[2] 5mA ≤ I_{OUT} ≤ 1.0A, P_D ≤ 15W	17.3	18.0	18.7	23.0	24.0	25.0	V
				21V ≤ V_{IN} ≤ 33V			28V ≤ V_{IN} ≤ 38V		
			17.1		18.9	22.8		25.2	V
	Line regulation			21V ≤ V_{IN} ≤ 33V			27V ≤ V_{IN} ≤ 38V		
				15	360		18	480	mV
				24V ≤ V_{IN} ≤ 30V			30V ≤ V_{IN} ≤ 36V		
				5	180		6	240	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 1.5A		12	360		12	480	mV
		250mA ≤ I_{OUT} ≤ 750mA		4	180		4	240	mV
I_{CC}				4.5	8.0		4.6	8.0	mA
I_{CC}				21V ≤ V_{IN} ≤ 33V			27V ≤ V_{IN} ≤ 38V		
		Over temp.,[2] with line		0.8			0.8		mA
		With load, 5mA ≤ I_{OUT} ≤ 1.0A		0.3			0.3		mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		110			170		μV
	Voltage drift	mV/1000hrs.			72			96	mV
				22V ≤ V_{IN} ≤ 32V			28V ≤ V_{IN} ≤ 38V		
	Ripple rejection	Over temp.,[2] f = 120Hz	59	69		56	66		dB
	Dropout voltage	I_{OUT} = 1.0A		2.0			2.0		V
	Output resistance	f = 1kHz		22			28		mΩ
I_{SC}				200			150		mA
	Peak output current			2.1			2.1		A
V_{OUT}	Output temperature drift	0°C ≤ T_J ≤ 125°C, I_{OUT} = 5mA		-1.0			-1.5		mV/°C

NOTES
2. -40°C ≤ T_J ≤ +125°C for SA78HV00C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 350mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	78MHV05[3]			78MHV05C[3]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 10V			V_{IN} = 10V		
			4.8	5.0	5.2	4.8	5.0	5.2	V
		Over temp.,[3] 5mA ≤ I_{OUT} ≤ 350mA		8V ≤ V_{IN} ≤ 20V			7V ≤ V_{IN} ≤ 20V		
			4.7		5.3	4.75		5.25	V
	Line regulation	I_{OUT} = 200mA		7V ≤ V_{IN} ≤ 25V			7V ≤ V_{IN} ≤ 25V		
				3	50		3	100	mV
				8V ≤ V_{IN} ≤ 20V			8V ≤ V_{IN} ≤ 25V		
				1	25		1	50	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 500mA		20	50		20	100	mV
		5mA ≤ I_{OUT} ≤ 200mA		10	25		10	50	mV
I_{CC}				4.5	6.0		4.5	6.0	mA
				8V ≤ V_{IN} ≤ 25V			8V ≤ V_{IN} ≤ 25V		
ΔI_{CC}	With line	Over temp.,[3] I_{OUT} = 200mA			0.8			0.8	mA
ΔI_{CC}	With load	5mA ≤ I_{OUT} ≤ 350mA			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		40			40		μV
	Voltage drift	mV/1000hrs.			20			20	mV
				8V ≤ V_{IN} ≤ 18V			8V ≤ V_{IN} ≤ 18V		
	Ripple rejection	Over temp.,[3] f = 120Hz	68	80		62	80		dB
	Dropout voltage			2.0			2.0		V
I_{SC}		V_{IN} = 35V		300			300		mA
	Peak output current			700			700		mA
				0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C		
V_{OUT}	Output temperature drift	I_{OUT} = 5mA		-1.0			-1.0		mV/°C

NOTE

3. -55°C ≤ T_J ≤ 150°C for 78MHV00
   0°C ≤ T_J ≤ 125°C for 78MHV00C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 350mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	78MHV06[3]			78MHV06C[3]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage	Over temp.,[3] 5mA ≤ I_{OUT} ≤ 350mA		V_{IN} = 11V			V_{IN} = 11V		
			5.75	6.0	6.25	5.75	6.0	6.25	V
				9V ≤ V_{IN} ≤ 21V			8.0V ≤ V_{IN} ≤ 21V		
			5.7		6.3	5.7		6.3	V
	Line regulation	I_{OUT} = 200mA		8V ≤ V_{IN} ≤ 25V			8V ≤ V_{IN} ≤ 25V		
				5	60		5	100	mV
				9V ≤ V_{IN} ≤ 20V			9V ≤ V_{IN} ≤ 25V		
				1.5	30		1.5	50	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 500mA		20	60		20	120	mV
		5mA ≤ I_{OUT} ≤ 200mA		10	30		10	60	mV
I_{CC}				4.5	6.0		4.5	8.0	mA
				9V ≤ V_{IN} ≤ 25V			9V ≤ V_{IN} ≤ 25V		
ΔI_{CC}	With line	Over temp.,[3] I_{OUT} = 200mA			0.8			0.8	mA
ΔI_{CC}	With load	5mA ≤ I_{OUT} ≤ 350mA			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		45			45		μV
	Voltage drift	mV/1000hrs.			24			24	mV
				9V ≤ V_{IN} ≤ 19V			9V ≤ V_{IN} ≤ 19V		
	Ripple rejection	Over temp.,[3] f = 120Hz	59	80		59	80		dB
	Dropout voltage			2.0			2.0		V
I_{SC}		V_{IN} = 35V		270			270		mA
	Peak output current			700			700		mA
				0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C		
V_{OUT}	Output temperature drift	I_{OUT} = 5mA		-0.5			-0.5		mV/°C

NOTE

3. -55°C ≤ T_J ≤ 150°C for 78MHV00
   0°C ≤ T_J ≤ 125°C for 78MHV00C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 350mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	78MHV08[3]			78MHV08C[3]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 14V			V_{IN} = 14V		
		Over temp.,[3] 5mA ≤ I_{OUT} ≤ 350mA	7.7	8.0	8.3	7.7	8.0	8.3	V
				11.5V ≤ V_{IN} ≤ 23V			10.5V ≤ V_{IN} ≤ 23V		
			7.6		8.4	7.6		8.4	V
	Line regulation	I_{OUT} = 200mA		10.5V ≤ V_{IN} ≤ 25V			10.5 ≤ V_{IN} ≤ 25V		
				6	60		6	100	mV
				11V ≤ V_{IN} ≤ 20V			11V ≤ V_{IN} ≤ 25V		
				2	30		2	50	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 500mA		25	80		25	160	mV
		5mA ≤ I_{OUT} ≤ 200mA		10	40		10	80	mV
I_{CC}				4.6	6.0		4.6	6.0	mA
				11.5V ≤ V_{IN} ≤ 25V			10.5V ≤ V_{IN} ≤ 25V		
ΔI_{CC}	With line	Over temp.,[3] I_{OUT} = 200mA			0.8			0.8	mA
ΔI_{CC}	With load	5mA ≤ I_{OUT} ≤ 350mA			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		52			52		μV
	Voltage drift	mV/1000hrs.			32			32	mV
				11.5V ≤ V_{IN} ≤ 21.5V			11.5V ≤ V_{IN} ≤ 21.5V		
	Ripple rejection	Over temp.,[3] f = 120Hz	56	80		56	80		dB
	Dropout voltage			2.0			2.0		V
I_{SC}		V_{IN} = 35V		250			250		mA
	Peak output current			700			700		mA
				0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C		
V_{OUT}	Output temperature drift	I_{OUT} = 5mA		-0.5			-0.5		mV/°C

NOTE

3. -55°C ≤ T_J ≤ 150°C for 78MHV00
   0°C ≤ T_J ≤ 125°C for 78MHV00C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 350mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	78MHV12[3]			78MHV12C[3]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage	Over temp.,[3] 5mA ≤ I_{OUT} ≤ 350mA	V_{IN} = 19V 11.5 | 12.0 | 12.5 15.5V ≤ V_{IN} ≤ 27V 11.4 | | 12.6			V_{IN} = 19V 11.5 | 12.0 | 12.5 14.5V ≤ V_{IN} ≤ 27V 11.4 | | 12.6			V V
	Line regulation	I_{OUT} = 200mA	14.5V ≤ V_{IN} ≤ 30V | 8 | 60 16V ≤ V_{IN} ≤ 25V | 2 | 30			14.5V ≤ V_{IN} ≤ 30V | 8 | 100 16V ≤ V_{IN} ≤ 30V | 2 | 50			mV mV
	Load regulation	5mA ≤ I_{OUT} ≤ 500mA 5mA ≤ I_{OUT} ≤ 200mA		25 10	120 60		25 10	240 120	mV mV
I_{CC}				4.8	6.0		4.8	6.0	mA
ΔI_{CC} ΔI_{CC}	With line With load	Over temp.,[3] I_{OUT} = 200mA 5mA ≤ I_{OUT} ≤ 350mA	15V ≤ V_{IN} ≤ 30V		0.8 0.5	14.5V ≤ V_{IN} ≤ 30V		0.8 0.5	mA mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		75			75		μV
	Voltage drift	mV/1000hrs.			48			48	mV
	Ripple rejection	Over temp.,[3] f = 120Hz	15V ≤ V_{IN} ≤ 25V 55	80		15V ≤ V_{IN} ≤ 25V 55	80		dB
	Dropout voltage			2.0			2.0		V
I_{SC}		V_{IN} = 35V		240			240		mA
	Peak output current			700			700		mA
V_{OUT}	Output temperature drift	I_{OUT} = 5mA	0°C ≤ T_J ≤ 150°C	-1.0		0°C ≤ T_J ≤ 125°C	-1.0		mV/°C

NOTE

3. −55°C ≤ T_J ≤ 150°C for 78MHV00
   0°C ≤ T_J ≤ 125°C for 78MHV00C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 350mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	78MHV15[3]			78MHV15C[3]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 23V			V_{IN} = 23V		
			14.4	15.0	15.6	14.4	15.0	15.6	V
		Over temp.,[3] 5mA ≤ I_{OUT} ≤ 350mA		18.5V ≤ V_{IN} ≤ 30V			17.5V ≤ V_{IN} ≤ 30V		
			14.25		15.75	14.25		15.75	V
	Line regulation	I_{OUT} = 200mA		17.5V ≤ V_{IN} ≤ 30V			17.5V ≤ V_{IN} ≤ 30V		
				10	60		10	100	mV
				20V ≤ V_{IN} ≤ 30V			20V ≤ V_{IN} ≤ 30V		
				3	30		3	50	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 500mA		25	150		25	150	mV
		5mA ≤ I_{OUT} ≤ 200mA		10	75		10	75	mV
I_{CC}				4.8	6.0		4.8	6.0	mA
				18.5V ≤ V_{IN} ≤ 30V			17.5V ≤ V_{IN} ≤ 30V		
ΔI_{CC}	With line	Over temp.,[3] I_{OUT} = 200mA			0.8			0.8	mA
ΔI_{CC}	With load	5mA ≤ I_{OUT} ≤ 350mA			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		90			90		μV
	Voltage drift	mV/1000hrs.			60			60	mV
				18.5V ≤ V_{IN} ≤ 28.5V			18.5V ≤ V_{IN} ≤ 28.5V		
	Ripple rejection	Over temp.,[3] f = 120Hz	54	70		54	70		dB
	Dropout voltage			2.0			2.0		V
I_{SC}		V_{IN} = 35V		240			240		mA
	Peak output current			700			700		mA
				0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C		
V_{OUT}	Output temperature drift	I_{OUT} = 5mA		-1.0			-1.0		mV/°C

NOTE

3. -55°C ≤ T_J ≤ 150°C for 78MHV00
   0°C ≤ T_J ≤ 125°C for 78MHV00C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 350mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	78MHV20[3]			78MHV20C[3]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 29V			V_{IN} = 29V		
			19.2	20	20.8	19.2	20	20.8	V
				24V ≤ V_{IN} ≤ 35V			23V ≤ V_{IN} ≤ 35V		
		Over temp.,[3] 5mA ≤ I_{OUT} ≤ 350mA	19		21	19		21	V
	Line regulation	I_{OUT} = 200mA		23V ≤ V_{IN} ≤ 35V			23V ≤ V_{IN} ≤ 35V		
				10	60		10	100	mV
				24V ≤ V_{IN} ≤ 35V			24V ≤ V_{IN} ≤ 35V		
				5	30		5	50	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 500mA		30	200		30	400	mV
		5mA ≤ I_{OUT} ≤ 200mA		10	100		10	200	mV
I_{CC}				4.9	6.0		4.9	6.0	mA
				24V ≤ V_{IN} ≤ 35V			23V ≤ V_{IN} ≤ 35V		
ΔI_{CC}	With line	Over temp.,[3] I_{OUT} = 200mA			0.8			0.8	mA
ΔI_{CC}	With load	5mA ≤ I_{OUT} ≤ 350mA			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		110			110		μV
	Voltage drift	mV/1000hrs.			80			80	mV
				24V ≤ V_{IN} ≤ 34V			24V ≤ V_{IN} ≤ 34V		
	Ripple rejection	Over temp.,[3] f = 120Hz	53	70		53	70		dB
	Dropout voltage			2.0			2.0		V
I_{SC}		V_{IN} = 35V		240			240		mA
	Peak output current			700			700		mA
				0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C		
V_{OUT}	Output temperature drift	I_{OUT} = 5mA		-1.1			-1.1		mV/°C

NOTE

3. -55°C ≤ T_J ≤ 150°C for 78MHV00
   0°C ≤ T_J ≤ 125°C for 78MHV00C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 350mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	78MHV24[3]			78MHV24C[3]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 33V			V_{IN} = 33V		
			23.0	24.0	25.0	23.0	24.0	25.0	V
		Over temp.,[3] 5mA ≤ I_{OUT} ≤ 350mA		28V ≤ V_{IN} ≤ 38V			27V ≤ V_{IN} ≤ 38V		
			22.8		25.2	22.8		25.2	V
	Line regulation	I_{OUT} = 200mA		27V ≤ V_{IN} ≤ 38V			27V ≤ V_{IN} ≤ 38V		
				10	60		10	100	mV
				30V ≤ V_{IN} ≤ 36V			28V ≤ V_{IN} ≤ 38V		
				5	30		5	50	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 500mA		30	240		30	480	mV
		5mA ≤ I_{OUT} ≤ 200mA		10	120		10	240	mV
I_{CC}				5	6.0		5	6.0	mA
				28V ≤ V_{IN} ≤ 38V			27V ≤ V_{IN} ≤ 38V		
ΔI_{CC}	With line	Over temp.,[3] I_{OUT} = 200mA			0.8			0.8	mA
ΔI_{CC}	With load	5mA ≤ I_{OUT} ≤ 350mA			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		170			170		μV
	Voltage drift	mV/1000hrs.			96			96	mV
				28V ≤ V_{IN} ≤ 38V			28V ≤ V_{IN} ≤ 38V		
	Ripple rejection	Over temp.,[3] f = 120Hz	50	70		50	70		dB
	Dropout voltage			2.0			2.0		V
I_{SC}		V_{IN} = 35V		240			240		mA
	Peak output current			700			700		mA
				0°C ≤ T_J ≤ 150°C			0°C ≤ T_J ≤ 125°C		
V_{OUT}	Output temperature drift	I_{OUT} = 5mA		-1.2			-1.2		mV/°C

NOTE

3. -55°C ≤ T_J ≤ 150°C for 78MHV00
   0°C ≤ T_J ≤ 125°C for 78MHV00C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 350mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	SA78MHV05C[4]			SA78MHV06C[4]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage	Over temp.,[4] 5mA ≤ I_{OUT} ≤ 350mA		V_{IN} = 10V 4.8 | 5.0 | 5.2 7V ≤ V_{IN} ≤ 25V 4.7 | | 5.3			V_{IN} = 11V 5.75 | 6.0 | 6.25 8.0V ≤ V_{IN} ≤ 21V 5.7 | | 6.3		V V
	Line regulation	I_{OUT} = 200mA		7V ≤ V_{IN} ≤ 25V | 3 | 100 8V ≤ V_{IN} ≤ 25V | 1 | 50			8V ≤ V_{IN} ≤ 25V | 5 | 100 9V ≤ V_{IN} ≤ 25V | 1.5 | 50		mV mV
	Load regulation	5mA ≤ I_{OUT} ≤ 500mA 5mA ≤ I_{OUT} ≤ 200mA		20 10	100 50		20 10	120 60	mV mV
I_{CC}				4.5	6.0		4.5	8.0	mA
ΔI_{CC} ΔI_{CC}	With line With load	Over temp.,[4] I_{OUT} = 200mA 5mA ≤ I_{OUT} ≤ 350mA		8V ≤ V_{IN} ≤ 25V 0.6 0.3			9V ≤ V_{IN} ≤ 25V 0.6 0.3		mA mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		40			45		μV
	Voltage drift	mV/1000hrs.			20			24	mV
	Ripple rejection	Over temp.,[4] f = 120Hz	62	8V ≤ V_{IN} ≤ 18V 80		59	9V ≤ V_{IN} ≤ 19V 80		dB
	Dropout voltage			2.0			2.0		V
I_{SC}		V_{IN} = 35V		300			270		mA
	Peak output current			700			700		mA
V_{OUT}	Output temperature drift	0°C ≤ T_J ≤ 125°C, I_{OUT} = 5mA		-1.0			-0.5		mV/°C

NOTE

4. -40°C ≤ T_J ≤ +125°C for SA78MHV00C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 350mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	SA78MHV08C[4]			SA78MHV12C[4]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 14V			V_{IN} = 19V		
			7.7	8.0	8.3	11.5	12.0	12.5	V
				10.5V ≤ V_{IN} ≤ 23V			14.5V ≤ V_{IN} ≤ 27V		
		Over temp.,[4] 5mA ≤ I_{OUT} ≤ 350mA	7.6		8.4	11.4		12.6	V
	Line regulation	I_{OUT} = 200mA		10.5V ≤ V_{IN} ≤ 25V			14.5V ≤ V_{IN} ≤ 30V		
				6	100		8	100	mV
				11V ≤ V_{IN} ≤ 25V			16V ≤ V_{IN} ≤ 30V		
				2	50		2	50	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 500mA		25	160		25	240	mV
		5mA ≤ I_{OUT} ≤ 200mA		10	80		10	120	mV
I_{CC}				4.6	8.0		4.8	8.0	mA
				10.5V ≤ V_{IN} ≤ 25V			14.5V ≤ V_{IN} ≤ 30V		
ΔI_{CC}	With line	Over temp.,[4] I_{OUT} = 200mA		0.6			0.6		mA
ΔI_{CC}	With load	5mA ≤ I_{OUT} ≤ 350mA		0.3			0.3		mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		52			75		μV
	Voltage drift	mV/1000hrs.			32			48	mV
				11.5V ≤ V_{IN} ≤ 21.5V			15V ≤ V_{IN} ≤ 25V		
	Ripple rejection	Over temp.,[4] f = 120Hz	56	80		55	80		dB
	Dropout voltage			2.0			2.0		V
I_{SC}		V_{IN} = 35V		250			240		mA
	Peak output current			700			700		mA
V_{OUT}	Output temperature drift	0°C ≤ T_J ≤ +125°C, I_{OUT} = 5mA		-0.5			-1.0		mV/°C

NOTE

4. −40°C ≤ T_J ≤ +125°C for SA78MHV00C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 350mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	SA78MHV15C[4]			SA78MHV20C[4]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 23V			V_{IN} = 29V		
			14.4	15.0	15.6	19.2	20	20.8	V
				17.5V ≤ V_{IN} ≤ 30V			23V ≤ V_{IN} ≤ 35V		
		Over temp.,[4] 5mA ≤ I_{OUT} ≤ 350mA	14.25		15.75	19		21	V
	Line regulation			17.5V ≤ V_{IN} ≤ 30V			23V ≤ V_{IN} ≤ 35V		
		I_{OUT} = 200mA		10	100		10	100	mV
				20V ≤ V_{IN} ≤ 30V			24V ≤ V_{IN} ≤ 35V		
				3	50		5	50	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 500mA		25	150		30	400	mV
		5mA ≤ I_{OUT} ≤ 200mA		10	75		10	200	mV
I_{CC}				4.8	8.0		4.9	6.5	mA
				17.5V ≤ V_{IN} ≤ 30V			23V ≤ V_{IN} ≤ 35V		
ΔI_{CC}	With line	Over temp.,[4] I_{OUT} = 200mA		0.6			0.6		mA
ΔI_{CC}	With load	5mA ≤ I_{OUT} ≤ 350mA		0.3			0.3		mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		90			110		μV
	Voltage drift	mV/1000hrs.			60			80	mV
				18.5V ≤ V_{IN} ≤ 28.5V			24V ≤ V_{IN} ≤ 34V		
	Ripple rejection	Over temp.,[4] f = 120Hz	54	70		53	70		dB
	Dropout voltage			2.0			2.0		V
I_{SC}		V_{IN} = 35V		240			240		mA
	Peak output current			700			700		mA
V_{OUT}	Output temperature drift	0°C ≤ T_J ≤ +125°C, I_{OUT} = 5mA		-1.0			-1.1		mV/°C

NOTE

4. -40°C ≤ T_J ≤ +125°C for SA78MHV00C

DC ELECTRICAL CHARACTERISTICS

(Cont'd) I_{OUT} = 350mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

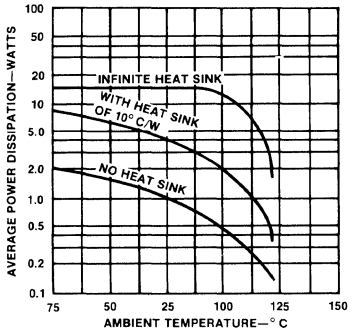
PARAMETER		TEST CONDITIONS	SA78MHV24C[4]			UNIT
			Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = 33V		
			23.0	24.0	25.0	V
				27V ≤ V_{IN} ≤ 38V		
		Over temp.,[4] 5mA ≤ I_{OUT} ≤ 350mA	22.8		25.2	V
	Line regulation			27V ≤ V_{IN} ≤ 38V		
		I_{OUT} = 200mA		10	100	mV
				30V ≤ V_{IN} ≤ 38V		
				5	50	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 500mA		30	480	mV
		5mA ≤ I_{OUT} ≤ 200mA		10	240	mV
I_{CC}				5	7	mA
				27V ≤ V_{IN} ≤ 38V		
ΔI_{CC}	With line	Over temp.,[4] I_{OUT} = 200mA		0.6		mA
ΔI_{CC}	With load	5mA ≤ I_{OUT} ≤ 350mA		0.3		mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz		170		μV
	Voltage drift	mV/1000hrs.			96	mV
				28V ≤ V_{IN} ≤ 38V		
	Ripple rejection	Over temp.,[4] f = 120Hz	50	70		dB
	Dropout voltage			2.0		V
I_{SC}		V_{IN} = 35V		240		mA
	Peak output current			700		mA
V_{OUT}	Output temperature drift	0°C ≤ T_J ≤ +125°C, I_{OUT} = 5mA		-1.2		mV/°C

NOTE

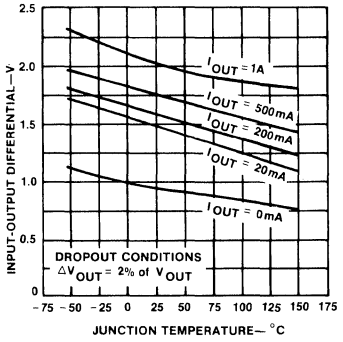
4. -40°C ≤ T_J ≤ +125°C for SA78MHV00C

TYPICAL PERFORMANCE CHARACTERISTICS 78HV00

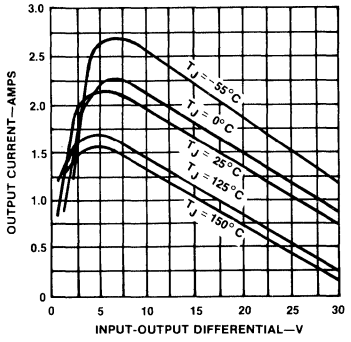
MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-220, 7800C)



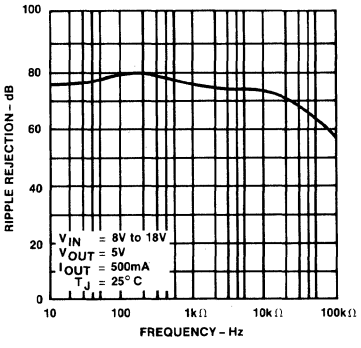
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



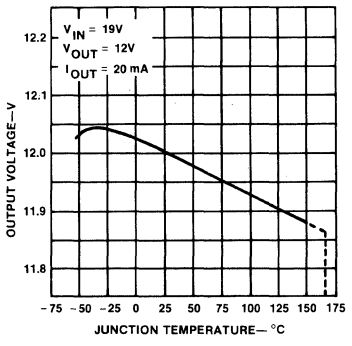
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT/OUTPUT DIFFERENTIAL VOLTAGE



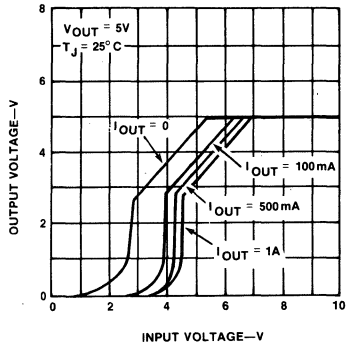
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



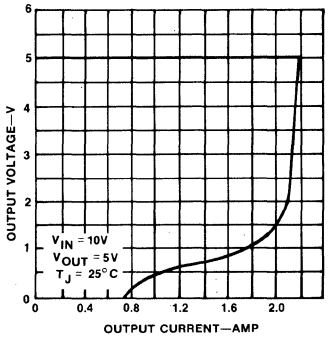
OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



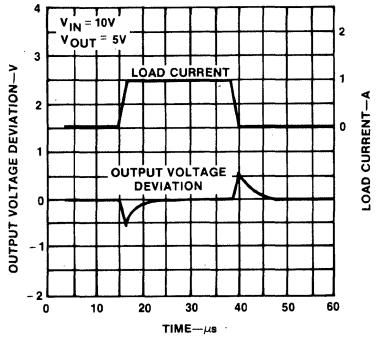
DROPOUT CHARACTERISTICS



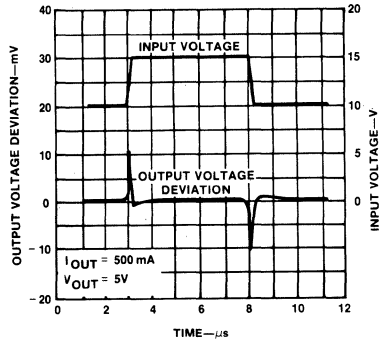
CURRENT LIMITING CHARACTERISTICS



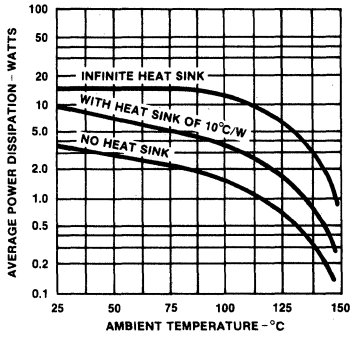
LOAD TRANSIENT RESPONSE



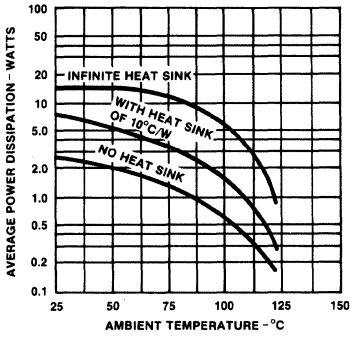
LINE TRANSIENT RESPONSE



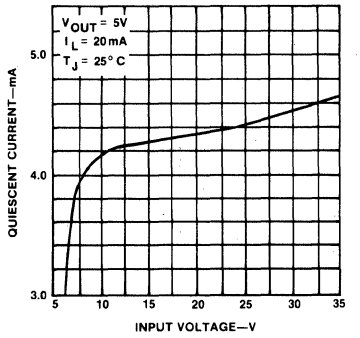
MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO 3, 78HV00)



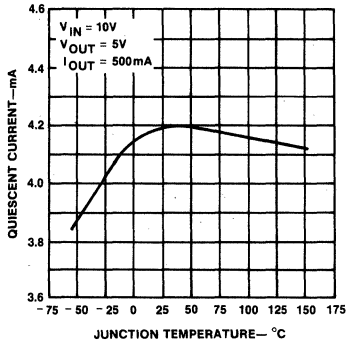
MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-3, 78HV00C, SA78HV00C)



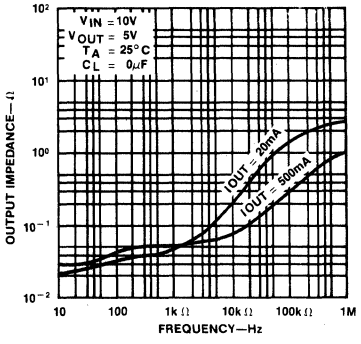
QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



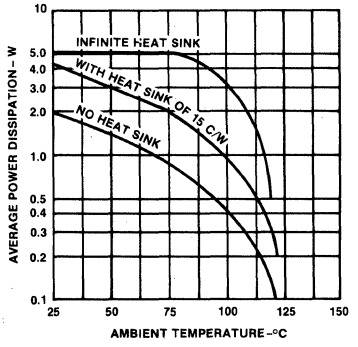
QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY

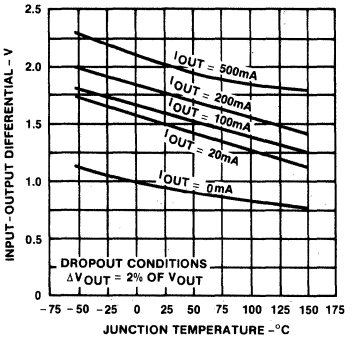


MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERAMENT (TO-220, 78M00C)

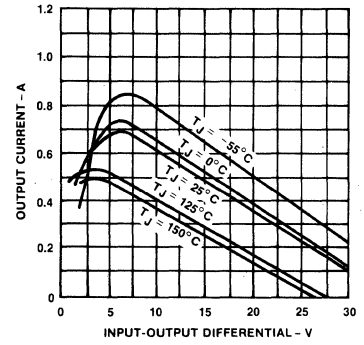


78MHV

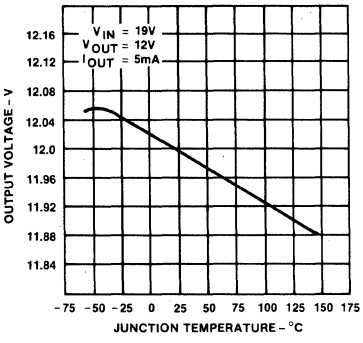
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



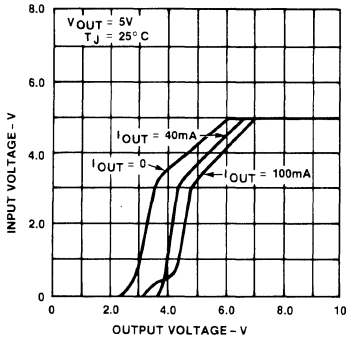
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT/OUTPUT DIFFERENTIAL VOLTAGE



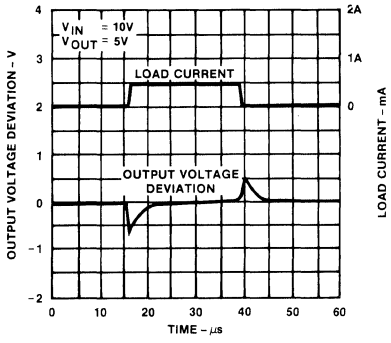
OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



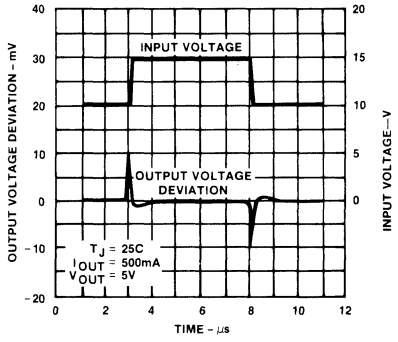
DROPOUT CHARACTERISTICS



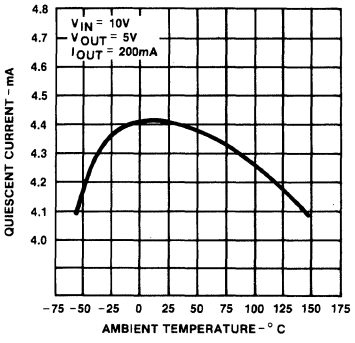
78MHV LOAD TRANSIENT RESPONSE



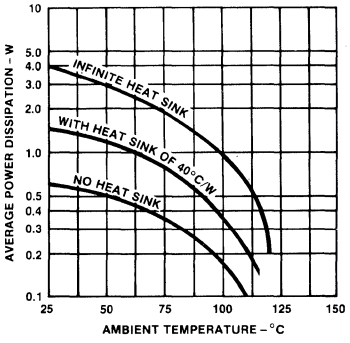
LINE TRANSIENT RESPONSE



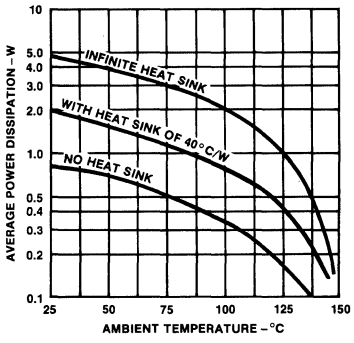
QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-39, 78M00C)



MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-39, 78M00)



DESCRIPTION

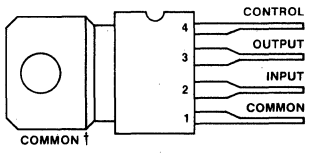
The μA78MG and μA79MG are 4-Terminal Adjustable Voltage Regulators. They are designed to deliver continuous load currents of up to 500mA with a maximum input voltage of 40V for the positive regulator 78MG and -40V for the negative regulator 79MG. Output current capability can be increased to greater than 10A through use of one or more external transistors. The output voltage range of the 78MG positive voltage regulator is 5V to 30V and the output voltage range of the negative 79MG is -30V to -2.2V. For systems requiring both a positive and negative, the 78MG and 79MG are excellent for use as a dual tracking regulator.

FEATURES

- **Output current in excess of 0.5A**
- **μA78MG positive output voltage 5 to 30V**
- **μA79MG negative output voltage -30V to -2.2V**
- **Internal thermal overload protection**
- **Internal short circuit current protection**
- **Output transistor safe area protection**

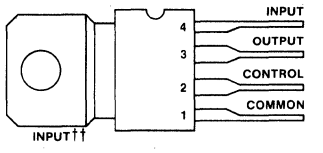
PIN CONFIGURATIONS

U1 PACKAGE
Power Tab



ORDER INFORMATION

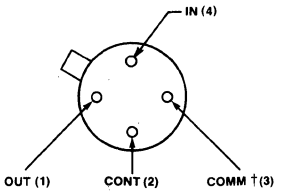
TYPE	PART NO.
μA78MGC	μA78MGCU1



ORDER INFORMATION

TYPE	PART NO.
μA79MG	μA79MGCU1

H PACKAGE



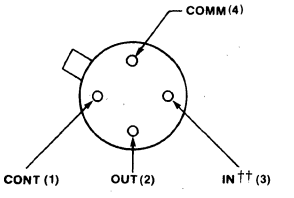
ORDER INFORMATION

TYPE	PART NO.
μA78MG	μA78MGH
μA78MGC	μA78MGCH

†NOTE

Heat sink tabs connected to common through device substrate.

H PACKAGE



ORDER INFORMATION

TYPE	PART NO.
μA79MG	μA79MGH
μA79MGC	μA79MGCH

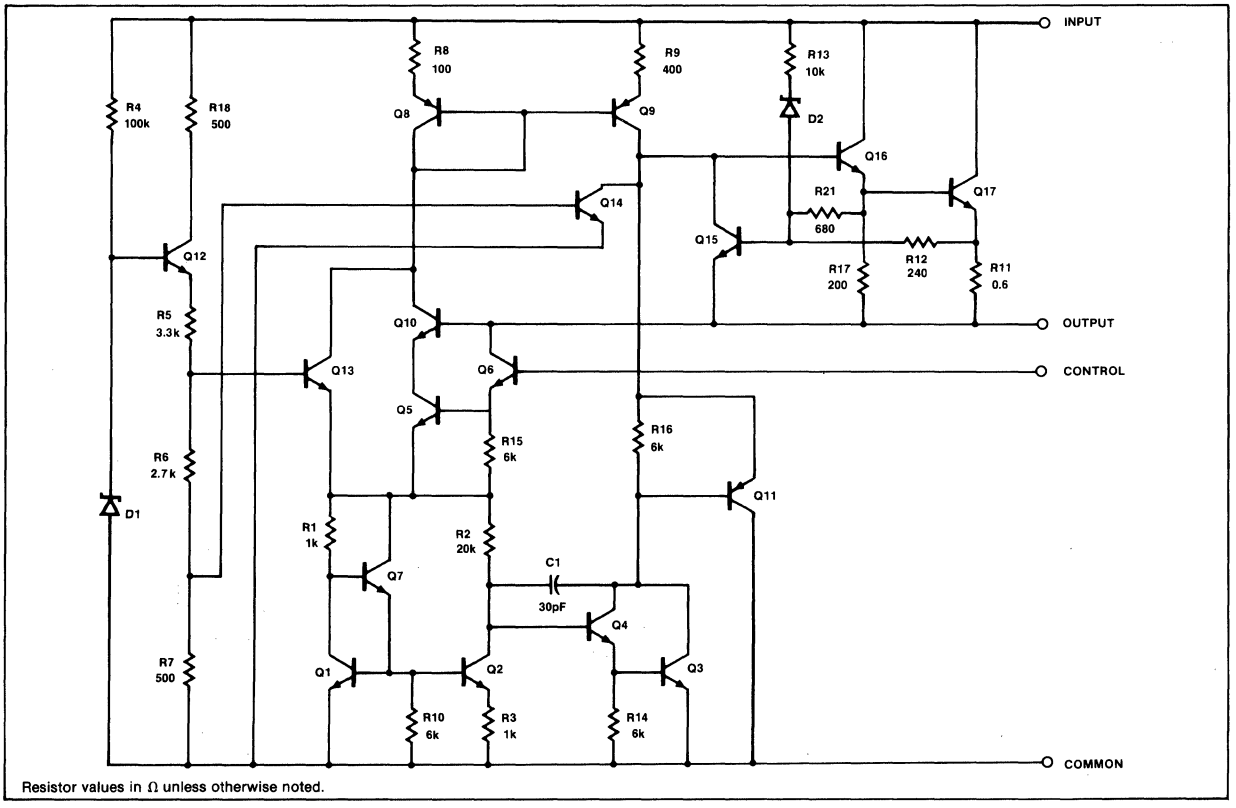
††NOTE

Heat sink tabs connected to input through device substrate. Not recommended for direct electrical connection.

ABSOLUTE MAXIMUM RATINGS

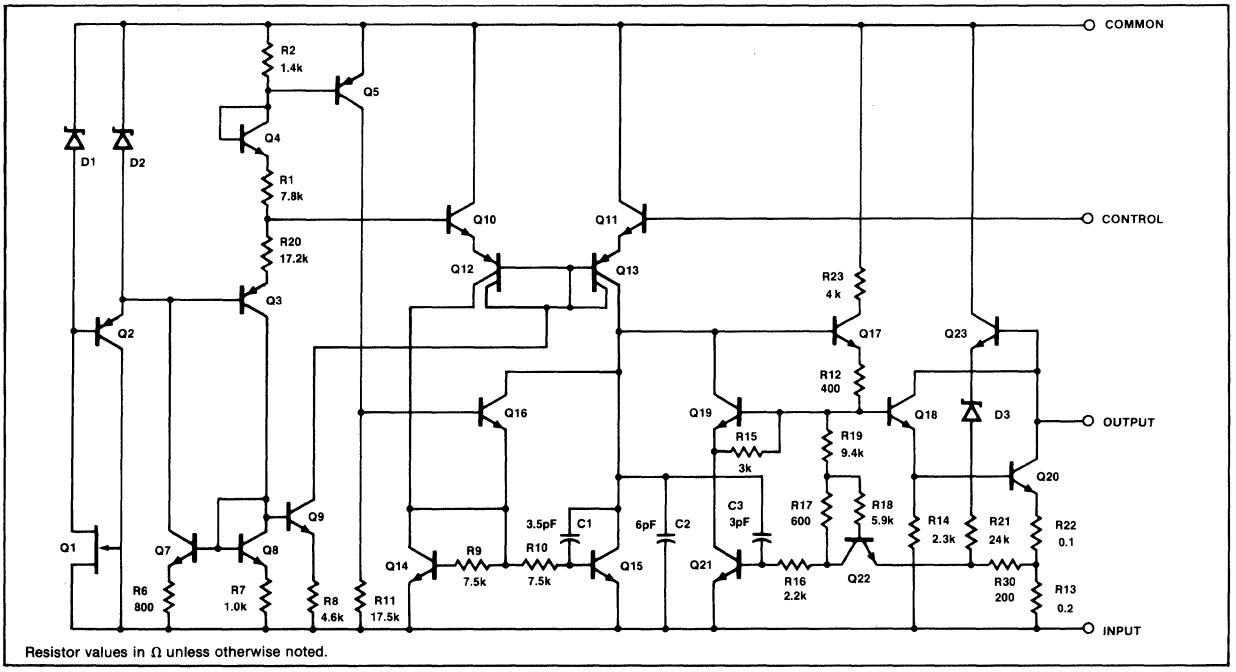
PARAMETER	RATING	UNIT
Input voltage		
μA78MG, μA78MGC	40	V
μA79MG, μA79MGC	-40	V
Control pin voltage		
μA78MG, μA78MGC	$0 < V < V_{OUT}$	
μA79MG, μA79MGC	$-V_{OUT} < -V < 0$	
Power dissipation	Internally limited	
Operating junction temperature range		
Military (μA78MG, μA79MG)	-55 to 150	°C
Commercial (μA78MGC, μA79MGC)	0 to 150	°C
Storage temperature range		
H	-65 to +150	°C
U1	-55 to +150	°C
Lead temperature		
U1 (soldering, 10s)	230	°C
H (soldering, 60s)	300	°C

78MG EQUIVALENT CIRCUIT



Resistor values in Ω unless otherwise noted.

79MG EQUIVALENT CIRCUIT



Resistor values in Ω unless otherwise noted.

DC ELECTRICAL CHARACTERISTICS

$0°C \le T_J \le 125°C$ for μA78MGC, $-55°C \le T_J \le 150°C$ for μA78MG, V_{IN} = 10V, I_{OUT} = 350mA unless otherwise specified.[1,2]

PARAMETER	TEST CONDITIONS[1]	μA78MG			UNIT
		Min	Typ	Max	
Input voltage range	$T_J = 25°C$	7.5		40	V
Output voltage range	$V_{IN} = V_{OUT} + 5V$	5.0		30	V
Output voltage tolerance	$V_{OUT}+3V \le V_{IN} \le V_{OUT}+15V$, $T_J=25°C$ $5mA \le I_{OUT} \le 350mA$ $P_D \le 5W$, $V_{INMAX} = 38V$			4.0 5.0	%(V_{OUT}) %(V_{OUT})
Line regulation	$T_J = 25°C$, $I_{OUT} = 200mA$, $V_{OUT} \le 10V$ $(V_{OUT} + 2.5V) \le V_{IN} \le (V_{OUT} + 20V)$ $T_J = 25°C$, $I_{OUT} = 200mA$, $V_{OUT} \ge 10V$ $(V_{OUT} + 3V) \le V_{IN} \le (V_{OUT} + 15V)$ $(V_{OUT} + 3V) \le V_{IN} \le (V_{OUT} + 7V)$			1.0 0.75 0.67	%(V_{OUT}) %(V_{OUT}) %(V_{OUT})
Load regulation	$T_J = 25°C$ $5mA \le I_{OUT} \le 500mA$, $V_{IN} = V_{OUT} + 7V$			1.0	%(V_{OUT})
Control pin current	$T_J = 25°C$		1.0	5.0 8.0	μA μA
Quiescent current	$T_J = 25°C$		2.8	4.0 5.0	mA mA
Ripple rejection	$8V \le V_{IN} \le 18V$ $I_{OUT}=300mA$, $T_J=25°C$ $V_{OUT} = 5V$, f = 120Hz $I_{OUT} = 100mA$	62 62	80		dB dB
Output noise voltage	$10Hz \le f \le 100kHz$, $V_{OUT} = 5V$		25		μV
Dropout voltage[2]	μA78MG μA78MGC			3.0 2.5	V
Short circuit current	$V_{IN} = 35V$, $T_J = 25°C$		300		mA
Peak output current	$T_J = 25°C$		800		mA
Average temperature coefficient of output voltage	$V_{OUT} = 5V$ $I_{OUT} = 5mA$		-0.5		mV/°C
Control pin voltage (reference)	$T_J = 25°C$	4.8 4.75	5.0	5.2 5.25	V V

NOTES

1. V_{OUT} is defined for the 78MGC as $V_{OUT} = \frac{R1+R2}{R2}(5.0)$; The 79MGC as $V_{OUT} = \frac{R1+R2}{}(-2.23)$.
2. Dropout voltage is defined as that input-output voltage differential which causes the output voltage to decrease by 5% of its initial value.

DC ELECTRICAL CHARACTERISTICS

$0°C \le T_J \le 125°C$ for μA79MGC, $-55°C \le T_J \le 150°C$ for μA79MG $V_{IN} = -10V$ μA79MG $I_{OUT} = 350mA$, unless otherwise specified.*

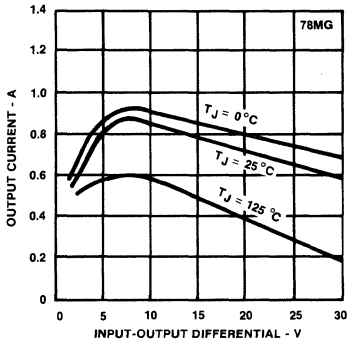
PARAMETER	TEST CONDITIONS[1]	μA79MG			UNIT
		Min	Typ	Max	
Input voltage range	$T_J = 25°C$	-40		-7.0	V
Output voltage range	$V_{IN} = V_{OUT} - 5V$	-30		-2.23	V
Output voltage tolerance	$V_{OUT} - 15V \le V_{IN} \le V_{OUT} - 3V$, $T_J = 25°C$			4.0	%(V_{OUT})
	$5mA \le I_{OUT} \le 350mA$			5.0	%(V_{OUT})
	$P_D \le 5W$, V_{IN} (MAX) = -38V				
Line regulation	$T_J = 25°C$, $I_{OUT} = 200mA$, $V_{OUT} \ge -10V$				
	$(V_{OUT} - 20V) \le V_{IN} \le (V_{OUT} - 2.5V)$			1.0	%(V_{OUT})
	$T_J = 25°C$, $I_{OUT} = 200mA$, $V_{OUT} \le -10V$				
	$(V_{OUT} - 15V) \le V_{IN} \le (V_{OUT} - 3V)$			0.75	%(V_{OUT})
	$(V_{OUT} - 7V) \le V_{IN} \le (V_{OUT} - 3V)$			0.67	%(V_{OUT})
Load regulation	$V_{IN} = V_{OUT} - 7V$, $5mA \le I_{OUT} \le 500mA$			1.0	%(V_{OUT})
	$T_J = 25°C$				
Control pin current	$T_J = 25°C$			3.0	μA
				2.0	μA
Quiescent current	$T_J = 25°C$		0.5	1.5	mA
				2.5	mA
Ripple rejection	$-18V \le V_{IN} \le -8V$ $T_J = 25°C$, $I_{OUT} = 300mA$	54	65		dB
	$V_{OUT} = -5V$, $f = 120Hz$ $I_{OUT} = 100mA$	50			dB
Output noise voltage	$10Hz \le f \le 100kHz$, $V_{OUT} = -5V$		125		μV
Dropout voltage[2]	μA79MG			2.5	V
	μA79MGC			2.3	
Short circuit current	$V_{IN} = -35V$		500		mA
Peak output current			650		mA
Average temperature coefficient of output voltage	$V_{OUT} = -5V$ $I_{OUT} = 5mA$		-0.4		mV/°C
Control pin voltage (reference)	$T_J = 25°C$	-2.32	-2.23	-2.14	V
		-2.35		-2.11	V

*NOTE

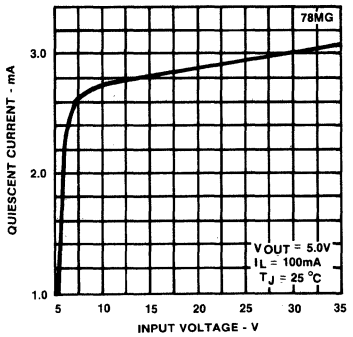
The convention for Negative Regulators is the Algebraic value, thus -15 is less than -10V.

TYPICAL PERFORMANCE CHARACTERISTICS FOR μA78MG

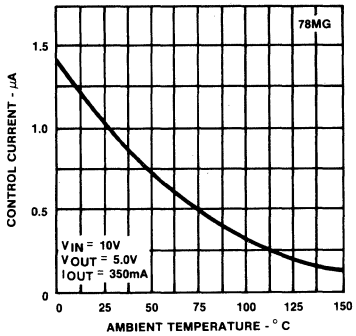
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE



QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE

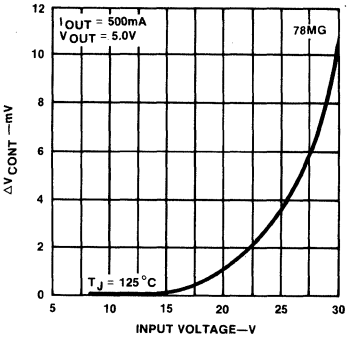


CONTROL CURRENT AS A FUNCTION OF TEMPERATURE

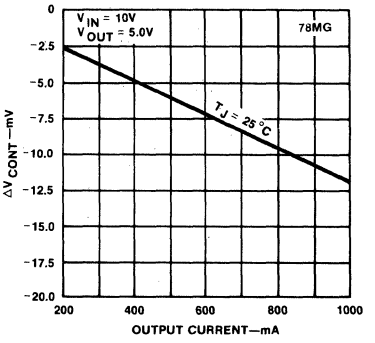


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

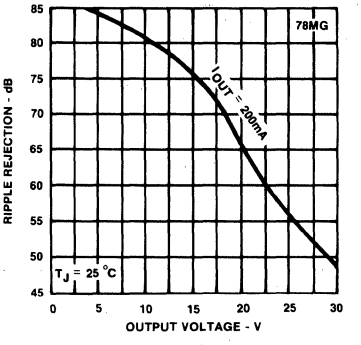
DIFFERENTIAL CONTROL VOLTAGE AS A FUNCTION OF INPUT VOLTAGE



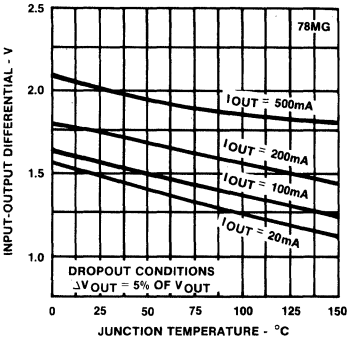
DIFFERENTIAL CONTROL VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



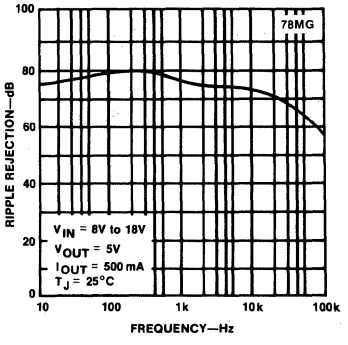
RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGE



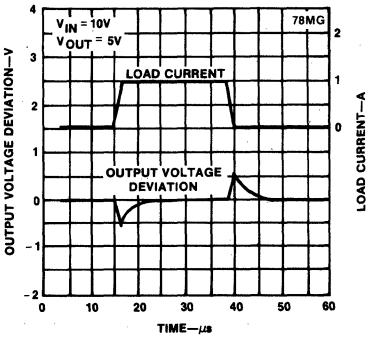
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



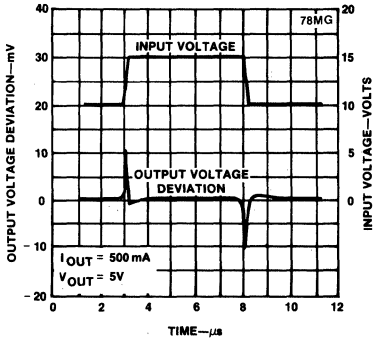
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



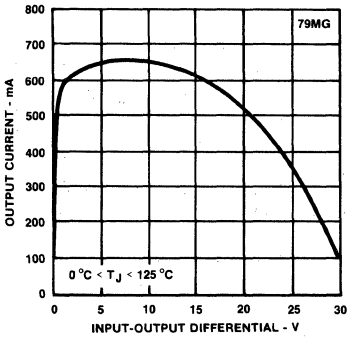
LOAD TRANSIENT RESPONSE



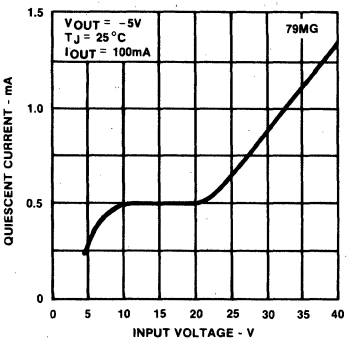
LINE TRANSIENT RESPONSE



PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE

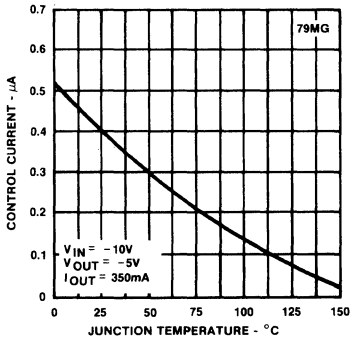


QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE

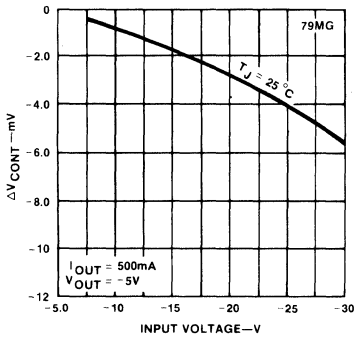


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

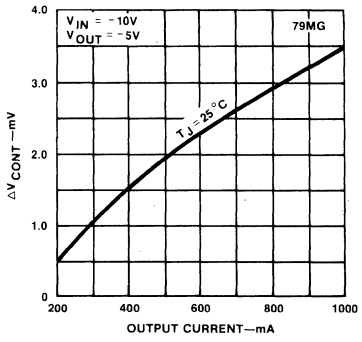
CONTROL CURRENT AS A FUNCTION OF TEMPERATURE



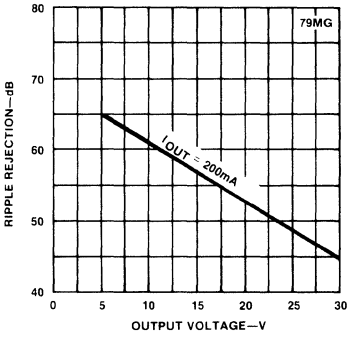
DIFFERENTIAL CONTROL VOLTAGE AS A FUNCTION OF INPUT VOLTAGE



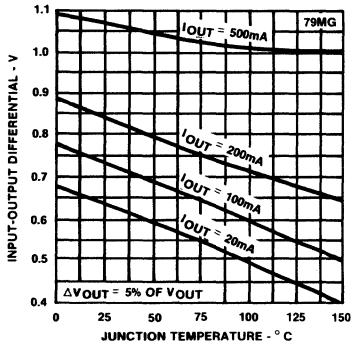
DIFFERENTIAL CONTROL VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



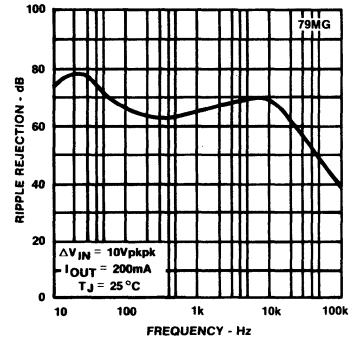
RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGE



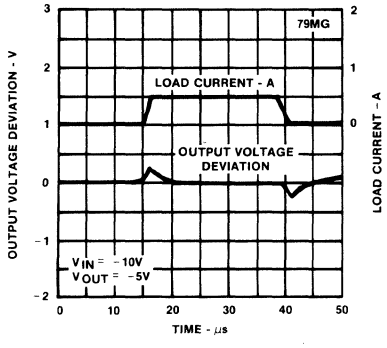
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



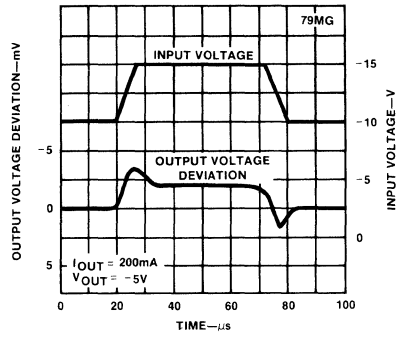
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



LOAD TRANSIENT RESPONSE



LINE TRANSIENT RESPONSE



μA79M00-DB,U

DESCRIPTION

The μA79M00 series of monolithic Three Terminal Negative Regulators employs internal current limiting, thermal shutdown, and safe-area compensation making them essentially indestructable. If adequate heat sinking is provided they can deliver over 500mA output current. They are intended as fixed voltage regulators, but used uith external components, can provide adjustable output voltages and currents.

FEATURES

- **Output current up to 500mA**
- **No external components**
- **Internal thermal overload protection**
- **Internal short circuit current limiting**
- **Output transistor safe-area compensation**
- **Available in the TO-220 and the TO-39 package**
- **Output voltages of -5, -5.2, -6, -8, -12, -15, -18 and -24 volts**
- **Mil std 883B pending**

ABSOLUTE MAXIMUM RATINGS

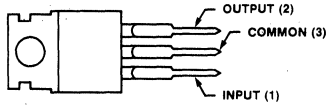
PARAMETER	RATING	UNIT
Input voltage		
(-5V through -15V)[1]	-35	V
(-20V, -24V)	-40	V
Internal power dissipation	Internally limited	
Storage temperature range		
TO-39	-65 to +150	°C
TO-220	-55 to +125	°C
Operating junction temperature range[2]		
79MOO	-55 to +150	°C
79MOOC	0 to +125	°C
Lead temperature		
TO-39 package		
(soldering, 60 sec)	300	°C
TO-220 package		
(soldering, 10 sec)	230	°C

NOTES

1. Thermal resistance of the packages (without a heat sink)
   Junction to case: TO-220 Package 2°C/W TO-39 Package 20°C/W.
   Junction to ambient: TO-220 Package 50°C/W TO-39 Package 170°C/W.
2. Operating ambient temperature range
   -55°C to +125°C
   0°C to +85°C

PIN CONFIGURATIONS

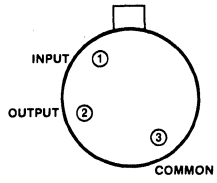
U PACKAGE (TO-220)



ORDER INFORMATION

OUTPUT VOLTAGE	ORDER PART NO.
-5V	79M05 CU
-5.2V	79M05.2 CU
-6V	79M06 CU
-8V	79M08 CU
-12V	79M12 CU
-15V	79M15 CU
-18V	79M18 CU
-24V	79M24 CU

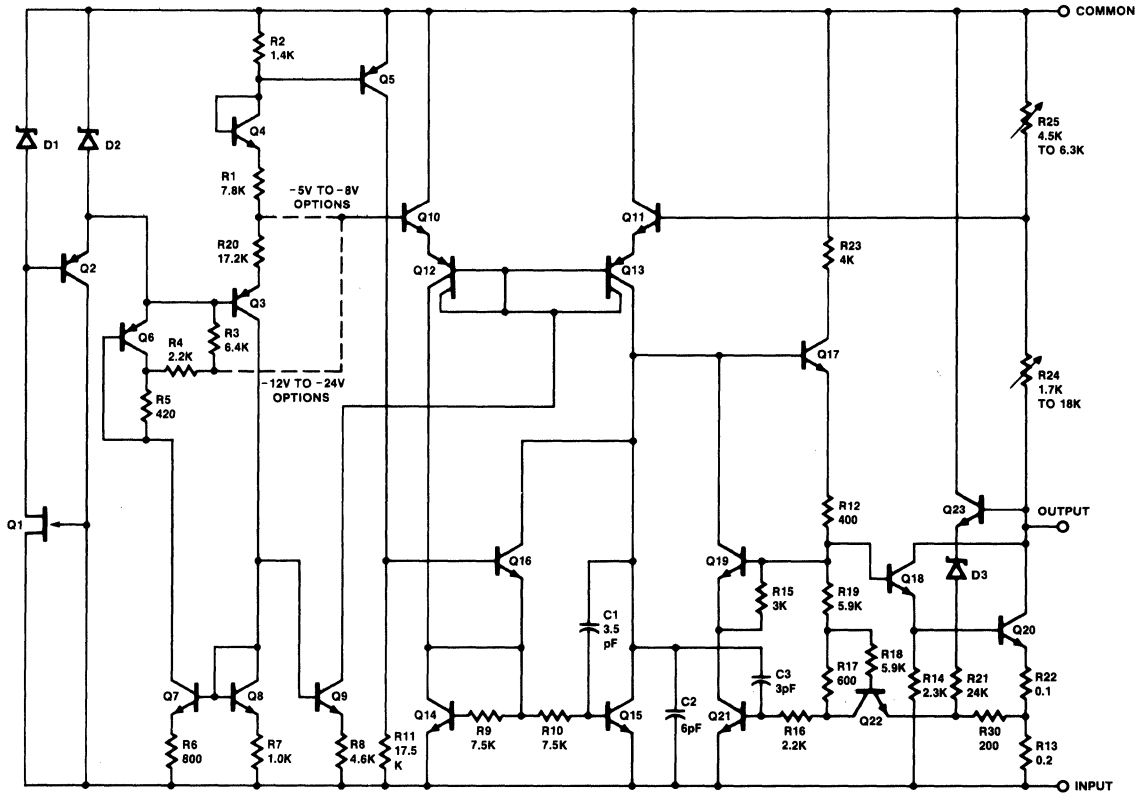
DB PACKAGE (TO-39)



OUTPUT VOLTAGE	ORDER PART NO.
-5V	79M05 DB
-5.2V	79M05.2 DB
-6V	79M06 DB
-8V	79M08 DB
-12V	79M12 DB
-15V	79M15 DB
-18V	79M18 DB
-24V	79M24 DB
-5V	79M05 CDB
-5.2V	79M05.2 CDB
-6V	79M06 CDB
-8V	79M08 CDB
-12V	79M12 CDB
-15V	79M15 CDB
-18V	79M18 CDB
-24V	79M24 CDB

μA79M00-DB,U

EQUIVALENT CIRCUIT



Resistor values in kΩ unless otherwise noted.

μA79M00-DB,U

DC ELECTRICAL CHARACTERISTICS

I_{OUT} = 350mA, T_J = 25°C, C_{IN} = 2μF, C_{OUT} = 1μF, unless otherwise specified.

PARAMETER		TEST CONDITIONS	79M05			79M05C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = -10V			V_{IN} = -10V		
			-5.2	-5.0	-4.8	-5.2	-5.0	-4.8	V
				-25V ≤ V_{IN} ≤ -7V			-25V ≤ V_{IN} ≤ -7V		
		5mA ≤ I_{OUT} ≤ 350mA, P_D ≤ 4W, over temp.*	-5.25		-4.75	-5.25		-4.75	V
	Line regulation			-25V ≤ V_{IN} ≤ -7V			-25V ≤ V_{IN} ≤ -7V		
				7.0	50		7.0	50	mV
				-18V ≤ V_{IN} ≤ -8V			-18V ≤ V_{IN} ≤ -8V		
				3.0	30		3.0	30	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 500mA		75	100		75	100	mV
		5mA ≤ I_{OUT} ≤ 350mA		50			50		mV
I_{CC}				1.0	2.0		1.0	2.0	mA
				-25V ≤ V_{IN} ≤ -8V			-25V ≤ V_{IN} ≤ -8V		
ΔI_{CC}		With line			0.4			0.4	mA
ΔI_{CC}		With load, 5mA ≤ I_{OUT} ≤ 350mA			0.4			0.4	mA
	Output noise voltage	10Hz ≤ f ≤ 100KHz		125		125			μV
				-18V ≤ V_{IN} ≤ -8V			-18V ≤ V_{IN} ≤ -8V		
	Ripple rejection	f = 120Hz I_{OUT} = 100mA, over temp.*	50			50			dB
	Dropout voltage			1.1			1.1		V
	Peak output current			650			650		mA
	Average temperature coefficient of output voltage	I_{OUT} = 5mA		-0.4			-0.4		mV/°C
I_{SC}		V_{IN} = -30V		140			140		mA

DC ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS	79M05.2			79M05.2C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage			V_{IN} = -10V			V_{IN} = -10V		
			-5.0	-5.2	-5.4	-5.0	-5.2	-5.4	V
				-25V ≤ V_{IN} ≤ -7V			-25V ≤ V_{IN} ≤ -7V		
		5mA ≤ I_{OUT} ≤ 350mA, P_D ≤ 4W, over temp.*	-5.45		-4.95	-5.00		-5.4	V
	Line regulation			-25V ≤ V_{IN} ≤ -7V			-25V ≤ V_{IN} ≤ -7V		
				7.0	50		7.0	50	mV
				-18V ≤ V_{IN} ≤ -8V			-18V ≤ V_{IN} ≤ -8V		
				3.0	30		3.0	30	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 500mA		75	100		75	100	mV
		5mA ≤ I_{OUT} ≤ 350mA		52			52		mV
I_{CC}				1.0	2.0		1.0	2.0	mA
				-25V ≤ V_{IN} ≤ -8V			-25V ≤ V_{IN} ≤ -8V		
ΔI_{CC}		With line			0.4			0.4	mA
ΔI_{CC}		With load, 5mA ≤ I_{OUT} ≤ 350mA			0.4			0.4	mA
	Output noise voltage	10Hz ≤ f ≤ 100KHz		125			125		μV
				-18V ≤ V_{IN} ≤ -8V			-18V ≤ V_{IN} ≤ -8V		
	Ripple rejection	f = 120Hz I_{OUT} = 100mA, over temp.*	50			50			dB
	Dropout voltage			1.1			1.1		V
	Peak output current			650			650		mA
	Average temperature coefficient of output voltage	I_{OUT} = 5mA		-0.4			-0.4		mV/°C
I_{SC}		V_{IN} = -30V		140			140		mA

*NOTE

-55°C ≤ T_J ≤ +150°C for 79M00
0°C ≤ T_J ≤ +125°C for 79M00C

μA79M00-DB,U

DC ELECTRICAL CHARACTERISTICS (Cont'd) I_{OUT} = 350mA, T_J = 25°C, C_{IN} = 2μF, C_{OUT} = 1μF, unless otherwise specified.

PARAMETER	TEST CONDITIONS	79M06			79M06C			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OUT} Output voltage			V_{IN} = -11V			V_{IN} = -11V		
		-6.25	-6.0	-5.75	-6.25	-6.0	-5.75	V
			-25V ≤ V_{IN} ≤ -8V			-25V ≤ V_{IN} ≤ -8V		
	5mA ≤ I_{OUT} ≤ 350mA, P_D ≤ 4W, over temp.*	-6.3		-5.7	-6.3		-5.7	V
	Line regulation		-25V ≤ V_{IN} ≤ -7V			-25V ≤ V_{IN} ≤ -7V		
			7.0	60		7.0	60	mV
			-19V ≤ V_{IN} ≤ -9V			-19V ≤ V_{IN} ≤ -9V		
			3.0	40		3.0	40	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 500mA		80	120		80	120	mV
		5mA ≤ I_{OUT} ≤ 350mA		55			55		mV
I_{CC}				1.0	2.0		1.0	2.0	mA
			-25V ≤ V_{IN} ≤ -9V			-25V ≤ V_{IN} ≤ -9V		
ΔI_{CC}	With line			0.4			0.4	mA
ΔI_{CC}	With load, 5mA ≤ I_{OUT} ≤ 350mA			0.4			0.4	mA
	Output noise voltage	10Hz ≤ f ≤ 100KHz		150			150		μV
			-19V ≤ V_{IN} ≤ -9V			-19V ≤ V_{IN} ≤ -9V		
	Ripple rejection	f = 120Hz I_{OUT} = 100mA, over temp.*	50			50			dB
	Dropout voltage			1.1			1.1		V
	Peak output current			650			650		mA
	Average temperature coefficient of output voltage	I_{OUT} = 5mA		-0.4			-0.4		mV/°C
I_{SC}		V_{IN} = -30V		140			140		mA

DC ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER	TEST CONDITIONS	79M08			79M08C			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OUT} Output voltage			V_{IN} = -14V			V_{IN} = -14V		
		-8.3	-8.0	-7.7	-8.3	-8.0	-7.7	V
			-25V ≤ V_{IN} ≤ -10.5V			-25V ≤ V_{IN} ≤ -10.5V		
	5mA ≤ I_{OUT} ≤ 350mA, P_D ≤ 4W, over temp.*	-8.4		-7.6	-8.4		7.6	V
	Line regulation		-25V ≤ V_{IN} ≤ -10.5V			-25V ≤ V_{IN} ≤ -10.5V		
			8.0	80		8.0	80	mV
			-21V ≤ V_{IN} ≤ -11V			-21V ≤ V_{IN} ≤ -11V		
			4.0	50		4.0	50	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 500mA		90	160		90	160	mV
		5mA ≤ I_{OUT} ≤ 350mA		60			60		mV
I_{CC}				1.0	2.0		1.0	2.0	mA
			-25V ≤ V_{IN} ≤ -10.5V			-25V ≤ V_{IN} ≤ -10.5V		
ΔI_{CC}	With line			0.4			0.4	mA
ΔI_{CC}	With load, 5mA ≤ I_{OUT} ≤ 350mA			0.4			0.4	mA
	Output noise voltage	10Hz ≤ f ≤ 100KHz		200			200		μV
			-21.5V ≤ V_{IN} ≤ -11.5V			-21.5V ≤ V_{IN} ≤ -11.5V		
	Ripple rejection	f = 120Hz I_{OUT} = 100mA, over temp.*	50			50			dB
	Dropout voltage			1.1			1.1		V
	Peak output current			650			650		mA
	Average temperature coefficient of output voltage	I_{OUT} = 5mA		-0.6			-0.6		mV/°C
I_{SC}		V_{IN} = -30V		140			140		mA

*NOTE

-55°C ≤ T_J ≤ +150°C for 79M00
0°C ≤ T_J ≤ +125°C for 79M00C

DC ELECTRICAL CHARACTERISTICS (Cont'd) I_{OUT} = 350mA, T_J = 25°C, C_{IN} = 2μF, C_{OUT} = 1μF, unless otherwise specified.

PARAMETER	TEST CONDITIONS	79M12			79M12C			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OUT} Output voltage		V_{IN} = -19V			V_{IN} = -19V			
		-12.5	-12	-11.5	-12.5	-12	-11.5	V
		-30V ≤ V_{IN} ≤ -14.5V			-30V ≤ V_{IN} ≤ -14.5V			
	5mA ≤ I_{OUT} ≤ 350mA, P_D ≤ 4W, over temp.*	-12.6		-11.4	-12.6		-11.4	V
Line regulation		-30V ≤ V_{IN} ≤ -14.5V			-30V ≤ V_{IN} ≤ -14.5V			
			9.0	80		9.0	80	mV
		-25V ≤ V_{IN} ≤ -15V			-25V ≤ V_{IN} ≤ -15V			
			5.0	50		5.0	50	mV
Load regulation	5mA ≤ I_{OUT} ≤ 500mA		65	240		65	240	mV
	5mA ≤ I_{OUT} ≤ 350mA		45			45		mV
I_{CC}			1.5	3.0		1.5	3.0	mA
		-30V ≤ V_{IN} ≤ -14.5V			-30V ≤ V_{IN} ≤ -14.5V			
ΔI_{CC}	With line			0.4			0.4	mA
ΔI_{CC}	With load, 5mA ≤ I_{OUT} ≤ 350mA			0.4			0.4	mA
Output noise voltage	10Hz ≤ f ≤ 100KHz		300			300		μV
		-28.5V ≤ V_{IN} ≤ -18.5V			-28.5V ≤ V_{IN} ≤ -18.5V			
Ripple rejection	f = 120Hz I_{OUT} = 100mA, over temp.*	50			50			dB
Dropout voltage			1.1			1.1		V
Peak output current			650			650		mA
Average temperature coefficient of output voltage	I_{OUT} = 5mA		-0.8			-0.8		mV/°C
I_{SC}	V_{IN} = -30V		140			140		mA

DC ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER	TEST CONDITIONS	79M15			79M15C			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OUT} Output voltage		V_{IN} = -23V			V_{IN} = -23V			
		-15.6	-15	-14.4	-15.6	-15	-14.4	V
		-30V ≤ V_{IN} ≤ -17.5V			-30V ≤ V_{IN} ≤ -17.5V			
	5mA ≤ I_{OUT} ≤ 350mA, P_D ≤ 4W, over temp.*	-15.75		-14.25	-15.75		-14.25	V
Line regulation		-30V ≤ V_{IN} ≤ -17.5V			-30V ≤ V_{IN} ≤ -17.5V			
			9.0	80		9.0	80	mV
		-28V ≤ V_{IN} ≤ -18V			-28V ≤ V_{IN} ≤ -18V			
			7.0	50		7.0	50	mV
Load regulation	5mA ≤ I_{OUT} ≤ 500mA		65	240		65	240	mV
	5mA ≤ I_{OUT} ≤ 350mA		45			45		mV
I_{CC}			1.5	3.0		1.5	3.0	mA
		-30V ≤ V_{IN} ≤ -17.5V			-30V ≤ V_{IN} ≤ -17.5V			
ΔI_{CC}	With line			0.4			0.4	mA
ΔI_{CC}	With load, 5mA ≤ I_{OUT} ≤ 350mA			0.4			0.4	mA
Output noise voltage	10Hz ≤ f ≤ 100KHz		375			375		μV
		-28.5V ≤ V_{IN} ≤ -18.5V			-28.5V ≤ V_{IN} ≤ -18.5V			
Ripple rejection	f = 120Hz I_{OUT} = 100mA, over temp.*	50			50			dB
Dropout voltage			1.1			1.1		V
Peak output current			650			650		mA
Average temperature coefficient of output voltage	I_{OUT} = 5mA		-1.0			-1.0		mV/°C
I_{SC}	V_{IN} = -30V		140			140		mA

*NOTE

-55°C ≤ T_J ≤ +150°C for 79M00
0°C ≤ T_J ≤ +125°C for 79M00C

DC ELECTRICAL CHARACTERISTICS (Cont'd) I_{OUT} = 350mA, T_J = 25°C, C_{IN} = 2μF, C_{OUT} = 1μF, unless otherwise specified.

PARAMETER	TEST CONDITIONS	79M18			79M18C			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OUT} Output voltage		V_{IN} = -27V			V_{IN} = -27V			
		-18.7	-18	-17.3	-18.7	-18	-17.3	V
		-33V ≤ V_{IN} ≤ -21V			-33V ≤ V_{IN} ≤ -21V			
	5mA ≤ I_{OUT} ≤ 350mA, P_D ≤ 4W, over temp.*	-18.9		-17.1	-18.9		-17.1	V
	Line regulation	-33V ≤ V_{IN} ≤ -21V			-33V ≤ V_{IN} ≤ -21V			
			11	80		11	80	mV
		-32V ≤ V_{IN} ≤ -22V			-32V ≤ V_{IN} ≤ -22V			
			11	70		11	70	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 500mA		70		70	300	mV
	5mA ≤ I_{OUT} ≤ 350mA			48		48		mV
I_{CC}			1.5	3.5		1.5	3.5	mA
		-33V ≤ V_{IN} ≤ -21V			-33V ≤ V_{IN} ≤ -21V			
ΔI_{CC}	With line			.4			.4	mA
ΔI_{CC}	With load, 5mA ≤ I_{OUT} ≤ 350mA			.4			.4	mA
	Output noise voltage	10Hz ≤ f ≤ 100KHz		450			450	μV
		-32V ≤ V_{IN} ≤ -22V			-32V ≤ V_{IN} ≤ -22V			
	Ripple rejection	f = 120Hz I_{OUT} = 100mA, over temp.*	50			50		dB
	Dropout voltage		1.1			1.1		V
	Peak output current		650			650		mA
	Average temperature coefficient of output voltage	I_{OUT} = 5mA	-1.0			-1.0		mV/°C
I_{SC}		V_{IN} = -30V	140			140		mA

DC ELECTRICAL CHARACTERISTICS (Cont'd)

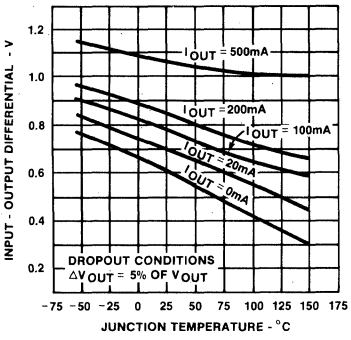
PARAMETER	TEST CONDITIONS	79M24			79M24C			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OUT} Output voltage		V_{IN} = -33V			V_{IN} = -33V			
		-25	-24	-23	-25	-24	-23	V
		-38V ≤ V_{IN} ≤ -27V			-38V ≤ V_{IN} ≤ -27V			
	5mA ≤ I_{OUT} ≤ 350mA, P_D ≤ 4W, over temp.*	-25.2		-22.8	-25.2		-22.8	V
	Line regulation	-38V ≤ V_{IN} ≤ -27V			-38V ≤ V_{IN} ≤ -27V			
			12	80		12	80	mV
		-38V ≤ V_{IN} ≤ -28V			-38V ≤ V_{IN} ≤ -28V			
			12	70		12	70	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 500mA		75		75	300	mV
	5mA ≤ I_{OUT} ≤ 350mA			50		50		mV
I_{CC}			1.5	3.5		1.5	3.5	mA
			-38V ≤ V_{IN} ≤ -27V			-38V ≤ V_{IN} ≤ -27V		
ΔI_{CC}	With line			0.4			0.4	mA
ΔI_{CC}	With load, 5mA ≤ I_{OUT} ≤ 350mA			0.4			0.4	mA
	Output noise voltage	10Hz ≤ f ≤ 100KHz		600			600	μV
		-38V ≤ V_{IN} ≤ -28V			-38V ≤ V_{IN} ≤ -28V			
	Ripple rejection	f = 120Hz I_{OUT} = 100mA, over temp.*	50			50		dB
	Dropout voltage	I_{OUT} = 5mA	1.1			1.1		V
	Peak output current		650			650		mA
	Average temperature coefficient of output voltage	V_{IN} = -30V	-1.0			-1.0		mV/°C
I_{SC}			140			140		mA

*NOTE

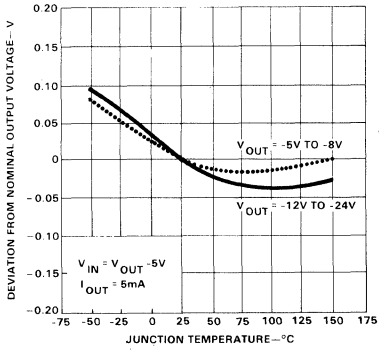
-55°C ≤ T_J ≤ +150°C for 79M00
0°C ≤ T_J ≤ +125°C for 79M00C

TYPICAL PERFORMANCE CHARACTERISTICS

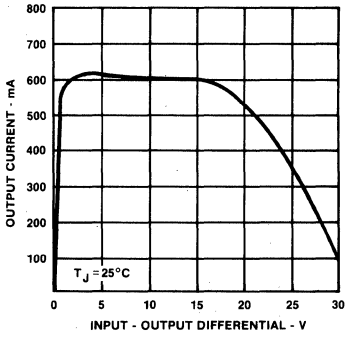
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



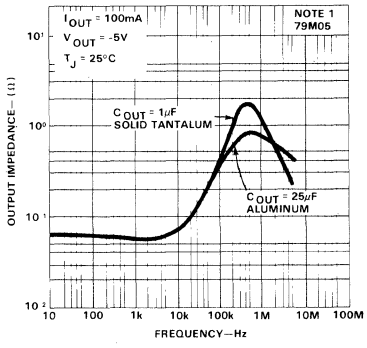
OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



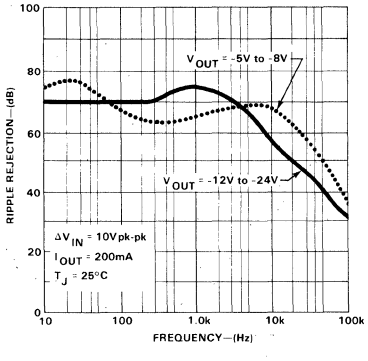
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE



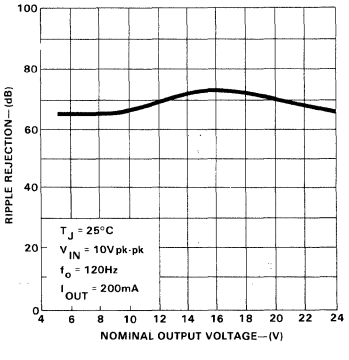
OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY



RIPPLE REJECTION AS A FUNCTION OF FREQUENCY

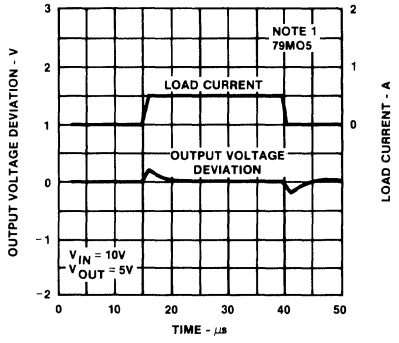


RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES

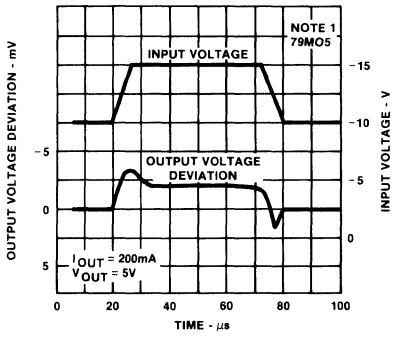


TYPICAL PERFORMANCE CHARACTRISTICS (Cont'd)

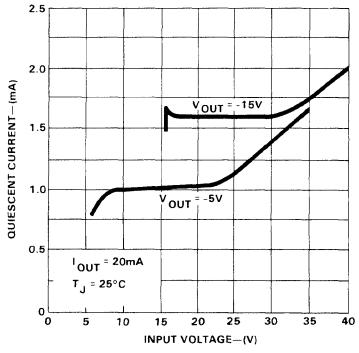
LOAD TRANSIENT RESPONSE



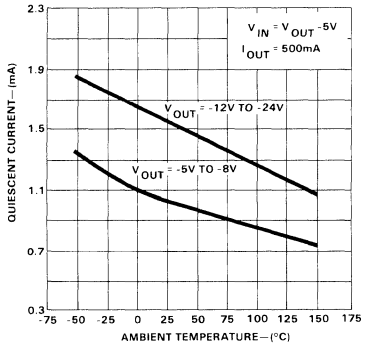
LINE TRANSIENT RESPONSE



QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



NOTE

The other μA79MOO voltage series devices have similar performance curves.

SECTION 4
TIMERS

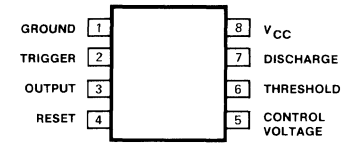
SA555F,N,N-14 • SE555F,T,N,N-14 • SE555C,F,T,N,N-14 • NE555F,T,N,N-14

FEATURES

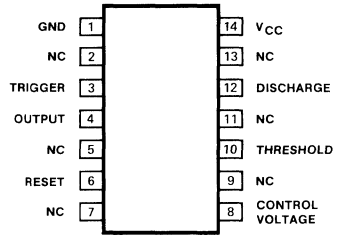
- Turn off time less than 2μs
- Maximum operating frequency greater than 500kHz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C
- SE555 Mil std 883A,B,C available M38510 (JAN) approved, M38510 processing available.

PIN CONFIGURATIONS

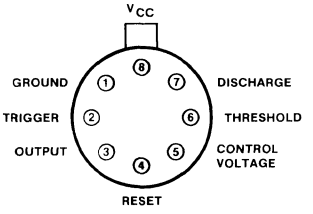
N PACKAGE



F,N-14 PACKAGE



T PACKAGE



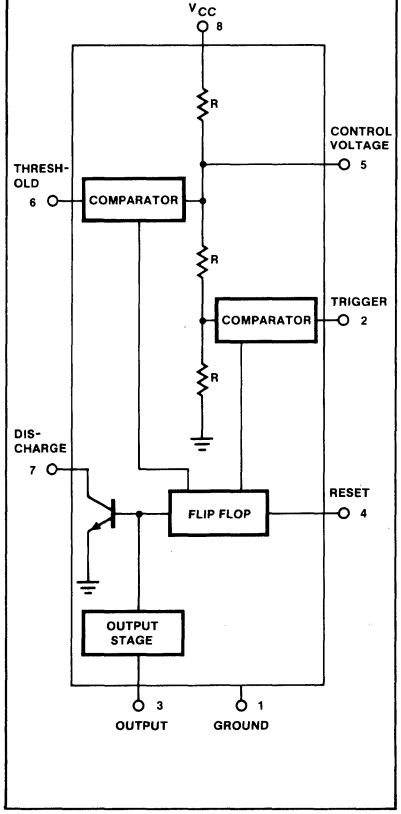
APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Missing pulse detector

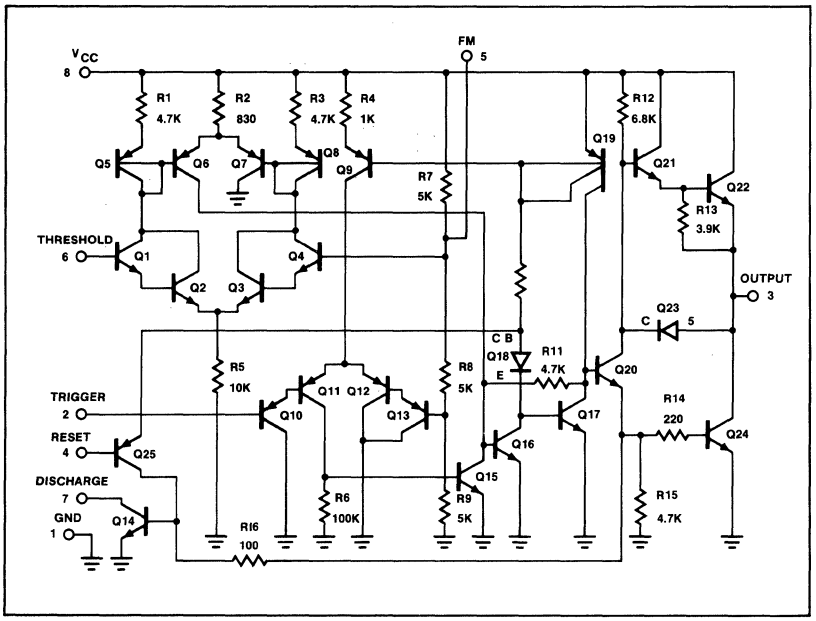
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE555	+18	V
NE555, SE555C, SA555	+16	V
Power dissipation	600	mW
Operating temperature range		
NE555	0 to +70	°C
SA555	-40 to +85	°C
SE555, SE555C	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Load temperature (soldering, 60sec)	300	°C

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = +5V$ to $+15$ unless otherwise specified.

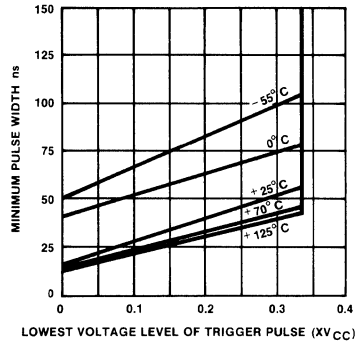
PARAMETER	TEST CONDITIONS	SE555			NE555/SE555C/SA555			UNIT
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current (low state)[1]	$V_{CC} = 5V$ $R_L = \infty$		3	5		3	6	mA
	$V_{CC} = 15V$ $R_L = \infty$		10	12		10	15	mA
Timing error (monostable)	$R_A = 2K\Omega$ to $100K\Omega$							
Initial accuracy[2]	$C = 0.1\mu F$		0.5	2.0		1.0	3.0	%
Drift with temperature			30	100		50		ppm/°C
Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
Timing error (astable)	R_A, $R_B = 1k\Omega$ to $100k\Omega$							
Initial accuracy[2]	$C = 0.1\mu F$		1.5			2.25		%
Drift with temperature	$V_{CC} = 15V$		90			150		ppm/°C
Drift with supply voltage			0.15			0.3		%/V
Control voltage level	$V_{CC} = 15V$	9.6	10.0	10.4	9.0	10.0	11.0	V
	$V_{CC} = 5V$	2.9	3.33	3.8	2.6	3.33	4.0	V
Threshold voltage	$V_{CC} = 15V$	9.4	10.0	10.6	8.8	10.0	11.2	V
	$V_{CC} = 5V$	2.7	3.33	4.0	2.4	3.33	4.2	V
Threshold current[3]			0.1	0.25		0.1	0.25	μA
Trigger voltage	$V_{CC} = 15V$	4.8	5.0	5.2	4.5	5.0	5.6	V
	$V_{CC} = 5V$	1.45	1.67	1.9	1.1	1.67	2.2	V
Trigger current	$V_{TRIG} = 0V$		0.5	0.9		0.5	2.0	μA
Reset voltage[4]		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset current			0.1	0.4		0.1	0.4	mA
Reset current	$V_{RESET} = 0V$		0.4	1.0		0.4	1.5	mA
Output voltage (low)	$V_{CC} = 15V$							
	$I_{SINK} = 10mA$		0.1	0.15		0.1	0.25	V
	$I_{SINK} = 50mA$		0.4	0.5		0.4	0.75	V
	$I_{SINK} = 100mA$		2.0	2.2		2.0	2.5	V
	$I_{SINK} = 200mA$		2.5			2.5		V
	$V_{CC} = 5V$							
	$I_{SINK} = 8mA$		0.1	0.25		0.3	0.4	V
	$I_{SINK} = 5mA$		0.05	0.2		0.25	0.35	V
Output voltage (high)	$V_{CC} = 15V$							
	$I_{SOURCE} = 200mA$		12.5			12.5		V
	$I_{SOURCE} = 100mA$	13.0	13.3		12.75	13.3		V
	$V_{CC} = 5V$							
	$I_{SOURCE} = 100mA$	3.0	3.3		2.75	3.3		V
Turn off time[5]	$V_{RESET} = V_{CC}$		0.5	2.0		0.5		μs
Rise time of output			100	200		100	300	ns
Fall time of output			100	200		100	300	ns
Discharge leakage current			20	100		20	100	na

NOTES

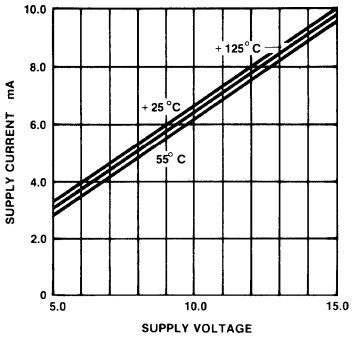
1. Supply current when output high typically 1mA less.
2. Tested at $V_{CC} = 5V$ and $V_{CC} = 15V$.
3. This will determine the maximum value of $R_A + R_B$, for 15V operation, the max total R = 10 megohm, and for 5V operation, the max total R = 3.4 megohm.
4. Specified with trigger input high.
5. Time measured from a positive going input pulse from 0 to $0.8 \times V_{CC}$ into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

TYPICAL PERFORMANCE CHARACTERISTICS

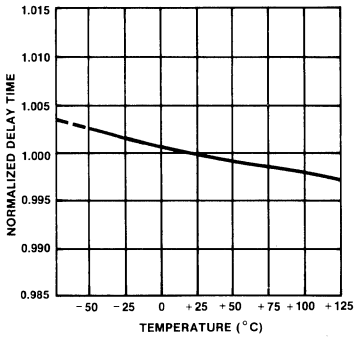
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



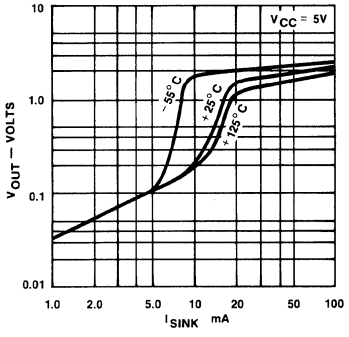
SUPPLY CURRENT vs SUPPLY VOLTAGE



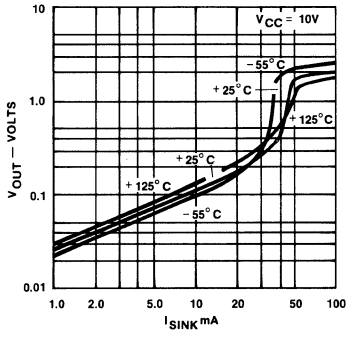
DELAY TIME vs TEMPERATURE



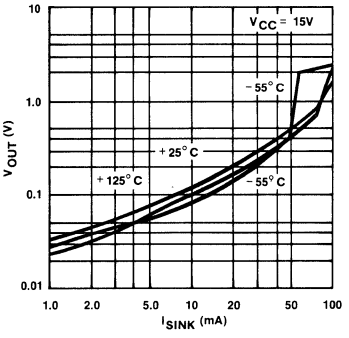
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



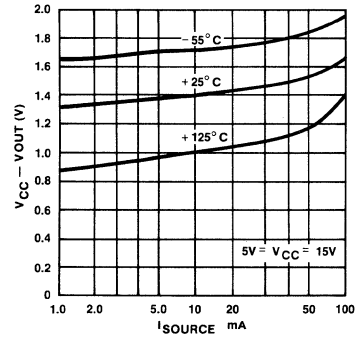
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



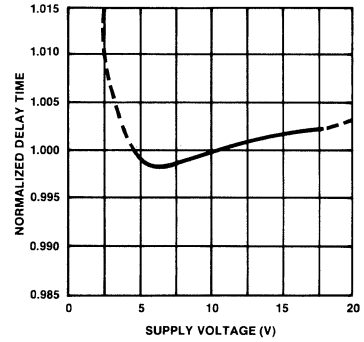
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



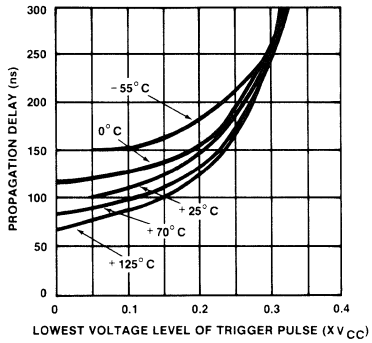
HIGH OUTPUT VOLTAGE DROP vs OUTPUT SOURCE CURRENT



DELAY TIME vs SUPPLY VOLTAGE



PROPAGATION DELAY vs VOLTAGE LEVEL OF TRIGGER PULSE



SA556F,N • SE556N,F • NE556F,N • SE556C,F,N

FEATURES

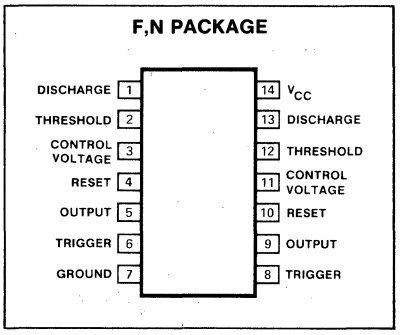
- Timing from microseconds to hours
- Replaces two 555 timers
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C
- SE566 MIL STD 883A, B, C available, N38510 (JAN planned, 38510 processing available).

APPLICATIONS

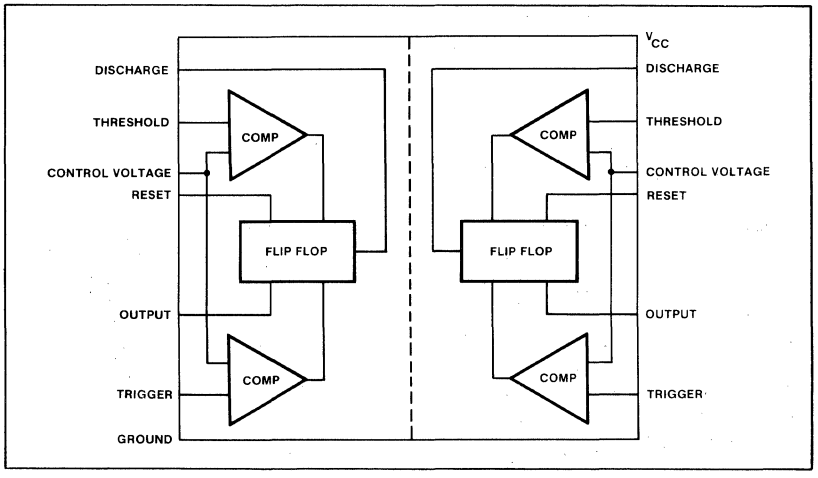
- Precision timing
- Sequential timing
- Pulse shaping
- Pulse generator
- Missing pulse detector
- Tone burst generator
- Pulse width modulation
- Time delay generator
- Frequency division
- Industrial controls
- Pulse position modulation
- Appliance timing
- Traffic light control
- Touch tone encoder

PIN CONFIGURATION

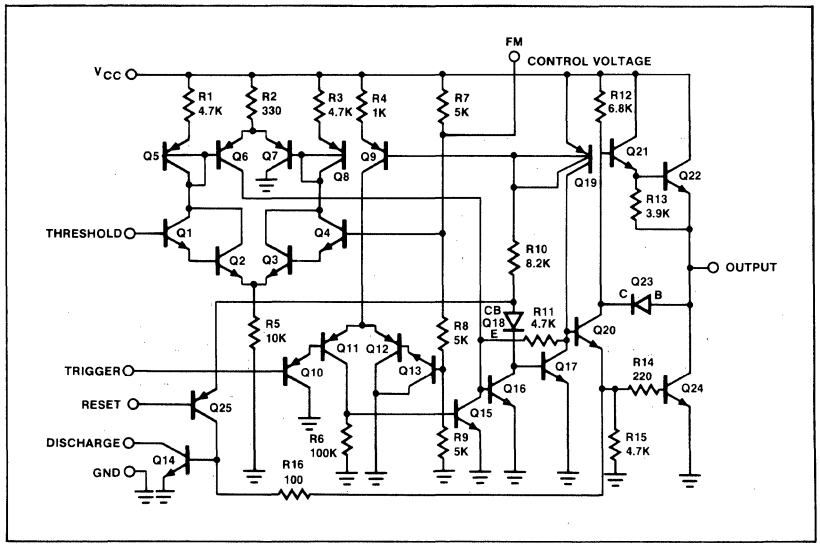
F,N PACKAGE



BLOCK DIAGRAM



EQUIVALENT SCHEMATIC (Shown for one circuit only)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE556	+18	V
NE556, SE556C, SA556	+16	V
Power dissipation	600	mW
Operating temperature range		
NE556	0 to +70	°C
SA556	-40 to +85	°C
SE556, SE556C	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (Soldering, 60 sec)	+300	°C

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = +5V$ to $+15V$ unless otherwise specified.

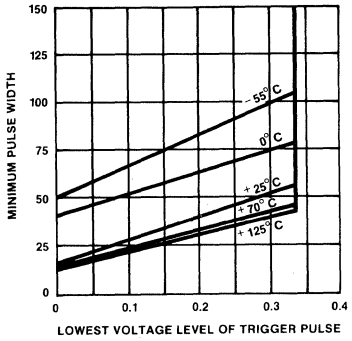
PARAMETER	TEST CONDITIONS	SE556			NE556/SE556C/SA556			UNITS
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current (low state)[1]	$V_{CC} = 5V$ $R_L = \infty$		6	10		6	12	mA
	$V_{CC} = 15V$ $R_L = \infty$		20	24		20	30	mA
Timing error (monostable)	$R_A = 2k\Omega$ to $100k\Omega$							
Initial accuracy[2]	$C = 0.1\mu F$		0.5	1.5		0.75	3.0	%
Drift with temperature			30	100		50		ppm/°C
Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
Timing error (astable)	R_A, $R_B = 1k\Omega$ to $100k\Omega$							
Initial accuracy[2]	$C = 0.1\mu F$		1.5			2.25		%
Drift with temperature	$V_{CC} = 15V$		90			150		ppm/°C
Drift with supply voltage			0.15			0.3		%/V
Control voltage level	$V_{CC} = 15V$	9.6	10.0	10.4	9.0	10.0	11.0	V
	$V_{CC} = 5V$	2.9	3.33	3.8	2.6	3.33	4.0	V
Threshold voltage	$V_{CC} = 15V$	9.4	10.0	10.6	8.8	10.0	11.2	V
	$V_{CC} = 5V$	2.7	3.33	4.0	2.4	3.33	4.2	V
Threshold current[3]			30	250		30	250	nA
Trigger voltage	$V_{CC} = 15V$	4.8	5.0	5.2	4.5	5.0	5.6	V
	$V_{CC} = 5V$	1.45	1.67	1.9	1.1	1.67	2.2	V
Trigger current	$V_{TRIG} = 0V$		0.5	0.9		0.5	2.0	μA
Reset voltage[5]		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset current			0.1	0.4		0.1	0.6	mA
Reset current	$V_{RESET} = 0V$		0.4	1.0		0.4	1.5	mA
Output voltage (low)	$V_{CC} = 15V$							
	$I_{SINK} = 10mA$		0.1	0.15		0.1	0.25	V
	$I_{SINK} = 50mA$		0.4	0.5		0.4	0.75	V
	$I_{SINK} = 100mA$		2.0	2.25		2.0	3.2	V
	$I_{SINK} = 200mA$		2.5			2.5		V
	$V_{CC} = 5V$							
	$I_{SINK} = 8mA$		0.1	0.2		0.25	0.3	V
	$I_{SINK} = 5mA$		0.05	0.15		0.15	0.25	V
Output voltage (high)	$V_{CC} = 15V$							
	$I_{SOURCE} = 200mA$		12.5			12.5		V
	$I_{SOURCE} = 100mA$	13.0	13.3		12.75	13.3		V
	$V_{CC} = 5V$							
	$I_{SOURCE} = 100mA$	3.0	3.3		2.75	3.3		V
Rise time of output			100	200		100	300	ns
Fall time of output			100	200		100	300	ns
Discharge leakage current			20	100		20	100	nA
Matching characteristics[4]								
Initial accuracy[2]			0.5	1.0		1.0	2.0	%
Drift with temperature			10			10		ppm/°C
Drift with supply voltage			0.1	0.2		0.2	0.5	%/V

NOTES

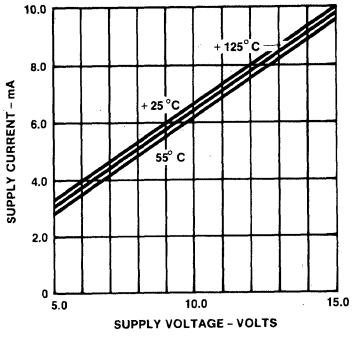
1. Supply current when output is high is typically 1.0mA less.
2. Tested at V_{CC} = 5V and V_{CC} = 15V.
3. This will determine the maximum value of $R_A + R_B$. For 15V operation, the maximum total R = 10 meg-ohms, and for 5V operation, the max. total R = 3.4 meg-ohms.
4. Matching charactristics refer to the difference between performance characteristics for each timer section in the monostable mode.
5. Specified with trigger input high.

TYPICAL PERFORMANCE CHARACTERISTICS

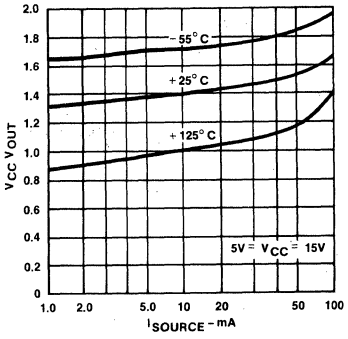
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



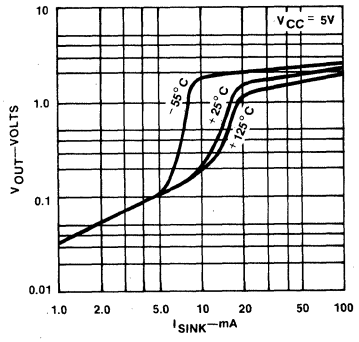
SUPPLY CURRENT vs SUPPLY VOLTAGE



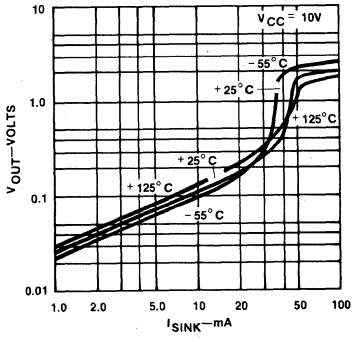
HIGH OUTPUT VOLTAGE DROP vs OUTPUT SOURCE CURRENT



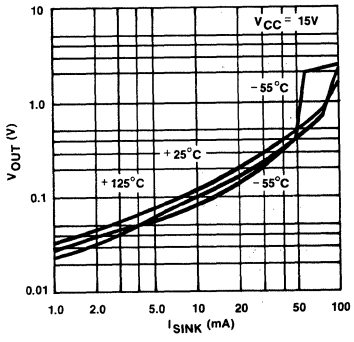
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



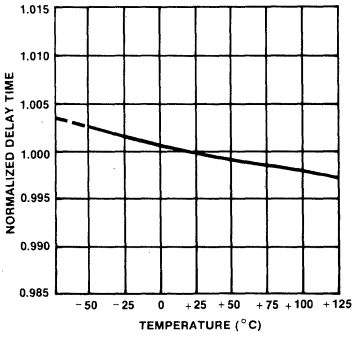
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



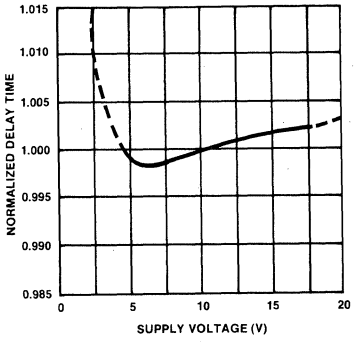
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



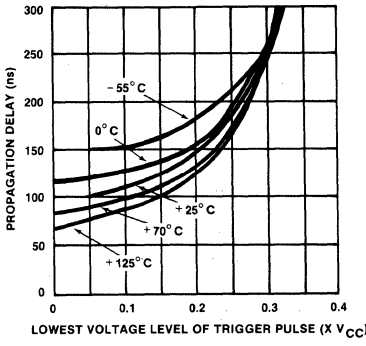
DELAY TIME vs TEMPERATURE



DELAY TIME vs SUPPLY VOLTAGE



PROPAGATION DELAY vs VOLTAGE LEVEL OF TRIGGER PULSE



SA556-1F,N • SE556-1N,F • NE556-1N,F • SE556-1CN,F

FEATURES

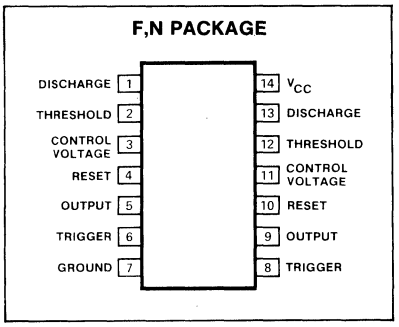
- Turn off time less than 2μS
- Maximum operating frequency greater than 500kHz
- Timing from microseconds to hours
- Replaces two 555 timers
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C

APPLICATIONS

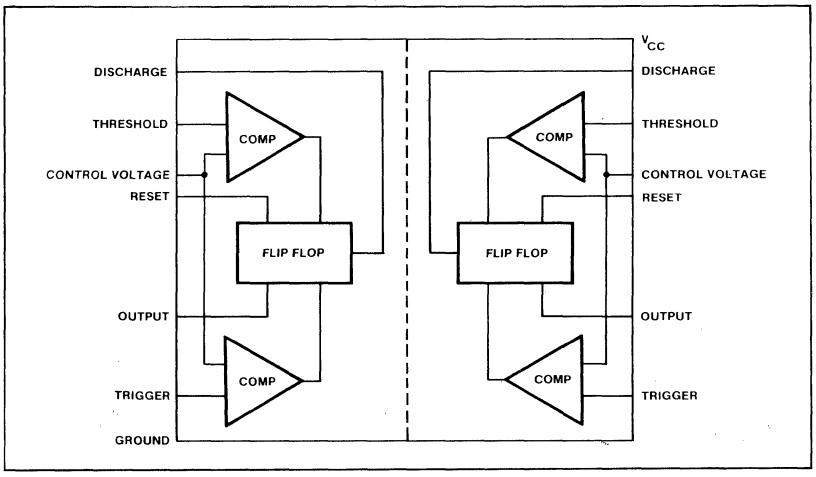
- Precision timing
- Sequential timing
- Pulse shaping
- Pulse generator
- Missing pulse detector
- Tone burst generator
- Pulse width modulation
- Time delay generator
- Frequency division
- Industrial controls
- Pulse position modulation
- Appliance timing
- Traffic light control
- Touch tone encoder

PIN CONFIGURATION

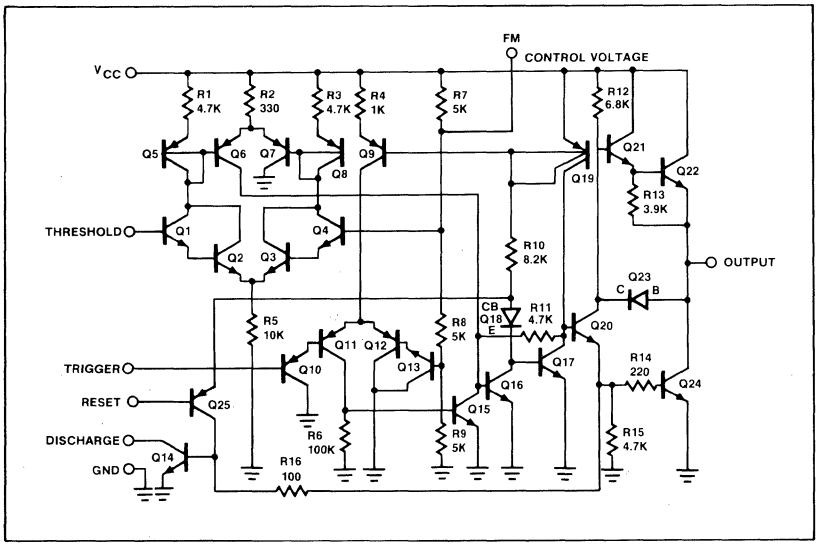
F,N PACKAGE



BLOCK DIAGRAM



EQUIVALENT SCHEMATIC (Shown for one circuit only)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE556-1	+18	V
NE556-1, SE556-1C, SA556-1	+16	V
Power dissipation	1.20	W
Operating temperature range		
NE556-1	0 to +70	°C
SA556-1	-40 to +85	°C
SE556-1, SE556-1C	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature		
(soldering, 60 sec)	+300	°C

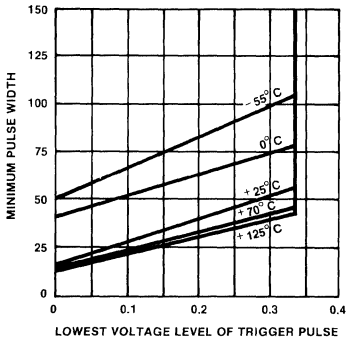
ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +5V to +15V unless otherwise specified.

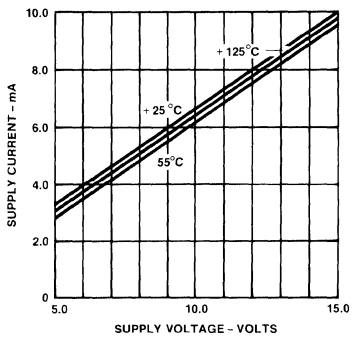
PARAMETER	TEST CONDITIONS	SE556-1			SA556-1/NE556-1/SE556-1C			UNITS
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current (low state)[1]	V_{CC} = 5V R_L = ∞		6	10		6	12	mA
	V_{CC} = 15V R_L = ∞		20	24		20	30	mA
Timing error (monostable)	R_A = 2kΩ to 100kΩ							
Initial accuracy[2]	C = 0.1μF		0.5	1.5		0.75	3.0	%
Drift with temperature			30	100		50		ppm/°C
Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
Timing error (astable)	R_A, R_B = 1kΩ to 100kΩ							
Initial accuracy[2]	C = 0.1μF		1.5			2.25		%
Drift with temperature	V_{CC} = 15V		90			150		ppm/°C
Drift with supply voltage			0.15			0.3		%/V
Control voltage level	V_{CC} = 15V	9.6	10.0	10.4	9.0	10.0	11.0	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4.0	V
Threshold voltage	V_{CC} = 15V	9.4	10.0	10.6	8.8	10.0	11.2	V
	V_{CC} = 5V	2.7	3.33	4.0	2.4	3.33	4.2	V
Threshold current[3]			30	250		30	250	nA
Trigger voltage	V_{CC} = 15V	4.8	5.0	5.2	4.5	5.0	5.6	V
	V_{CC} = 5V	1.45	1.67	1.9	1.1	1.67	2.2	V
Trigger current	V_{TRIG} = 0V		0.5	0.9		0.5	2.0	μA
Reset voltage[5]		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset current			0.1	0.4		0.1	0.6	mA
Reset current	V_{RESET} = 0V		0.4	1.0		0.4	1.5	mA
Output voltage (low)	V_{CC} = 15V							
	I_{SINK} = 10mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100mA		0.8	1.2		2.0	2.5	V
	I_{SINK} = 200mA		2.5			2.5		V
	V_{CC} = 5V							
	I_{SINK} = 8mA		0.1	0.2		0.25	0.3	V
	I_{SINK} = 5mA		0.05	0.15		0.15	0.25	V
Output voltage (high)	V_{CC} = 15V							
	I_{SOURCE} = 200mA		12.5			12.5		V
	I_{SOURCE} = 100mA	13.0	13.3		12.75	13.3		V
	V_{CC} = 5V							
	I_{SOURCE} = 100mA	3.0	3.3		2.75	3.3		V
Turn off time[6]	V_{RESET} = V_{CC}		0.5	2.0		0.5		μs
Rise time of output			100	200		100	300	ns
Fall time of output			100	200		100	300	ns
Discharge leakage current			20	100		20	100	nA
Matching characteristics[4]								
Initial accuracy[2]			0.5	1.0		1.0	2.0	%
Drift with temperature			±10			±10		ppm/°C
Drift with supply voltage			0.1	0.2		0.2	0.5	%/V

TYPICAL CHARACTERISTICS

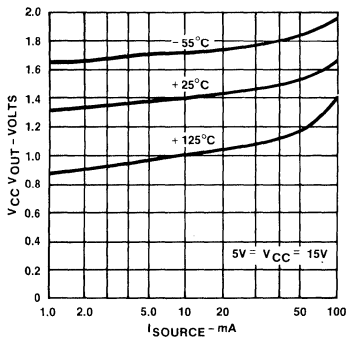
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



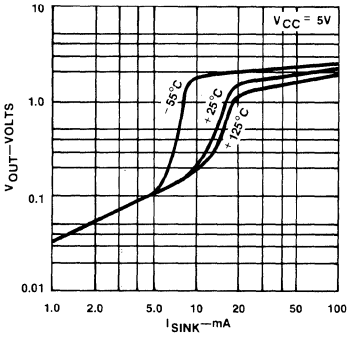
SUPPLY CURRENT vs SUPPLY VOLTAGE



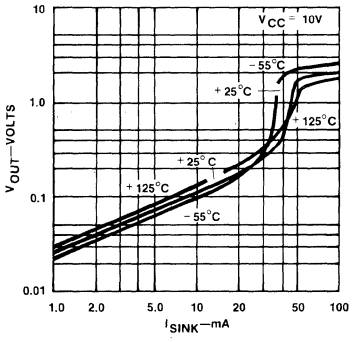
HIGH OUTPUT VOLTAGE DROP vs OUTPUT SOURCE CURRENT



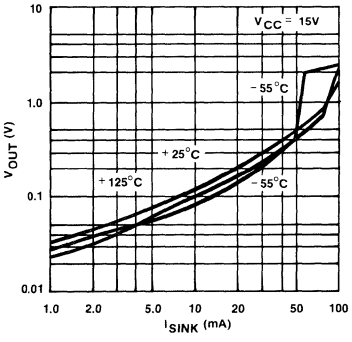
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



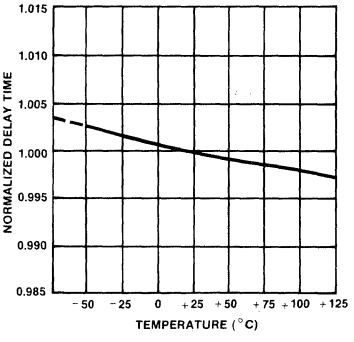
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



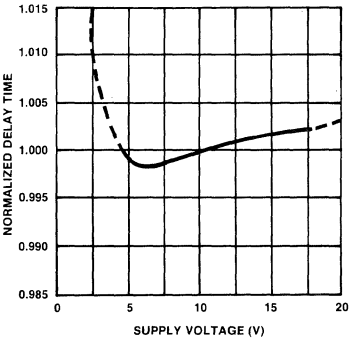
LOW OUTPUT VOLTAGE vs OUTPUT SINK CURRENT



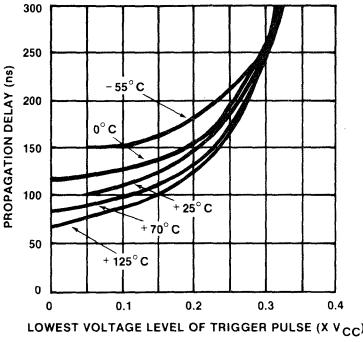
DELAY TIME vs TEMPERATURE



DELAY TIME vs SUPPLY VOLTAGE



PROPAGATION DELAY vs VOLTAGE LEVEL OF TRIGGER PULSE



NOTES

1. Supply current when output is high is typically 1.0mA less.
2. Tested at V_{CC} = 5V and V_{CC} = 15V.
3. This will determine the maximum value of $R_A + R_B$. For 15V operation, the maximum total R = 10 megohms, and for 5V operation, the max. total R = 3.4 megohms.
4. Matching characteristics refer to the difference between performance characteristics for each timer section in the monostable mode.
5. Specified with trigger input high.
6. Time measured from a positive going input pulse from 0 to 0.8 V_{CC} into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

DESCRIPTION

The SA/SE/NE558 and 559 Quad Timers are monolithic timing devices which can be used to produce four entirely independent timing functions. The 558 output sinks current whereas the 559 sources current. These highly stable, general purpose controllers can be used in a monostable mode to produce accurate time delays, from microseconds to hours. In the time delay mode of operation, the time is precisely controlled by one external resistor and one capacitor. Astable operation can be achieved by using two of the four timer sections.

The four timing sections in the 558 and 559 are edge triggered; therefore, when connected in tandem for sequential timing applications, no coupling capacitors are required. Output current capability of 100mA is provided in both devices.

FEATURES

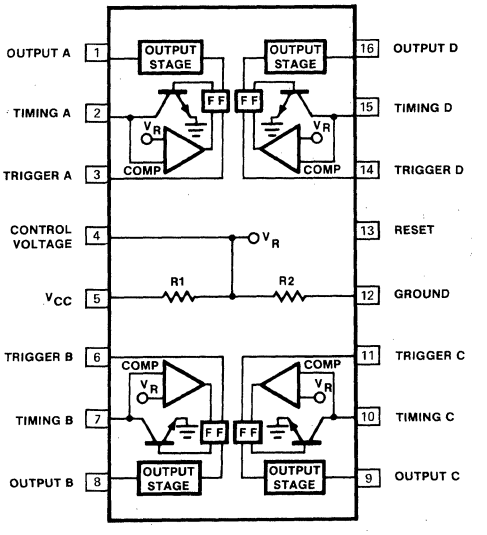
- **100mA output current per section**
- **Edge triggered (no coupling capacitor)**
- **Output independent of trigger conditions**
- **Wide supply voltage range 4.5V to 18V**
- **Timer intervals from microseconds to hours**
- **Time period equals RC**
- **Military qualifications pending**

APPLICATIONS

- **Sequential timing**
- **Time delay generation**
- **Precision timing**
- **Industrial controls**
- **Quad one-shot**

PIN CONFIGURATION

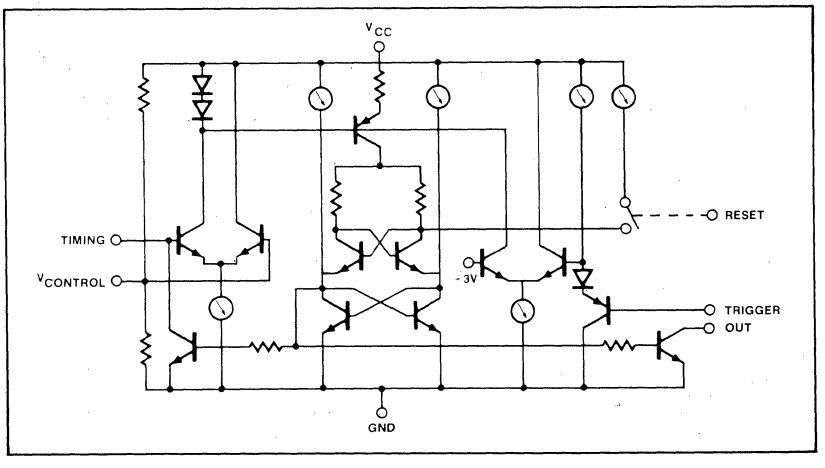
F,N PACKAGE



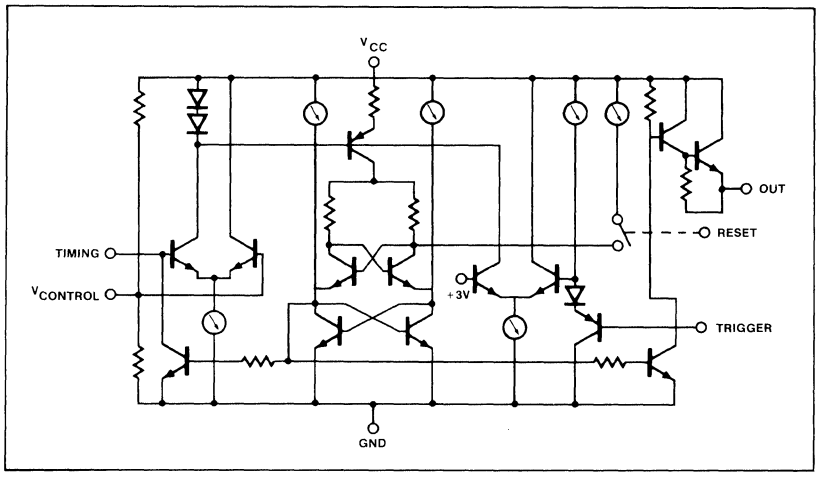
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE558, SE559	+18	V
NE558, NE559	+16	V
SA558, SA559	+16	V
Power dissipation	1.25	W
Operating temperature range		
NE558, NE559	0 to +70	°C
SA558, SA559	-40 to +85	°C
SE558, SE559	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

558 EQUIVALENT CIRCUIT



559 EQUIVALENT CIRCUIT



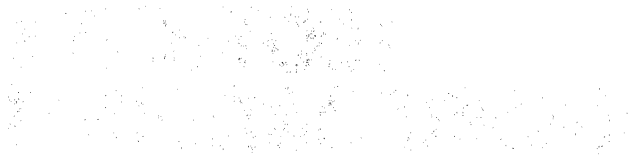
ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = +5V$ to $+15V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE558/SE559			NE558/NE559 SA558/SA559			UNIT
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current (558) (559) Timing accuracy (T = RC)	V_{CC} = Reset = 15V V_{CC} = Reset = 15V R = 2kΩ to 100kΩ C = 1μF		21 9	32 16		27 12	36 18	mA mA
Initial accuracy Drift with temperature Drift with supply voltage			1.0 150 0.1	3		2 150 0.1		% ppm/°C %/V
Trigger voltage[1] Trigger current	V_{CC} = 15V Trigger = 0V	0.8	1.5 5	2.4 30	0.8	1.5 5	2.4 100	V μA
Reset voltage[2] Reset current	Reset	0.8	1.5 50	2.4 300	0.8	1.5 50	2.4	V μA
Threshold voltage Threshold leakage			0.63 15			0.63 15		xVCC nA
Output voltage (558)[3]	I_L = 10mA I_L = 100mA		0.1 0.7	0.2 1.5		0.1 1.0	0.4 2.0	V V
Output voltage (559)[4]	I_L = 10mA I_L = 100mA	13 12.5	13.6 13.3		12.5 12.0	13.3 13.0		V V
Output leakage Propagation delay (558) (559)			10 1.0 0.4			10 1.0 0.4		nA μs μs
Risetime of output Falltime of output	I_L = 100mA I_L = 100mA		100 100			100 100		ns ns

NOTES

1. The trigger functions only on the falling edge of the trigger pulse only after previously being high. After reset the trigger must be brought high and then low to implement triggering.
2. For reset below 0.8 volts, outputs set low and trigger inhibited. For reset above 2.4 volts, trigger enabled.
3. The 558 output structure is open collector which requires a pull up resistor to V_{CC} to sink current. The output is normally low sinking current.
4. The 559 output structure is a darlington emitter follower which requires a pull down resistor to ground to source current. The output is normally low and sources current only when switched high.

SECTION 5
COMPARATORS



LM111/211/311-F,N,N-14,T
LH2111/2211/2311-F,N,N-14

DESCRIPTION

The LM111 series are voltage comparators that have input currents approximately a hundred times lower than devices like the μA710. They are designed to operate over a wider range of supply voltages; from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL, and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50mA.

Both the inputs and the outputs of the LM111 series can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the μA710 (200ns response time vs 40ns) the devices are also much less prone to spurious oscillations. The LM111 series has the same pin configuration as the μA710 series.

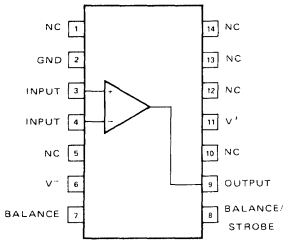
The LH2111 series hybrids are 2 LM111 type comparators in one hermetic package. They feature the same electrical parameters as the single devices.

FEATURES

- **Operates from single 5V supply**
- **Maximum input bias current: 150nA (LM311 - 250nA)**
- **Maximum offset current: 20nA (LM311 - 50nA)**
- **Differential input voltage range: ±30V**
- **Power consumption: 135mW at ±15V**
- **High sensitivity—200V/mV**
- **Military qualification pending**
- **LH2111 offers close thermal tracking**

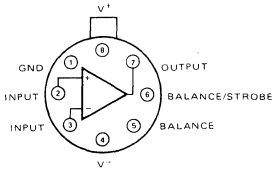
PIN CONFIGURATIONS

F,N-14 PACKAGE



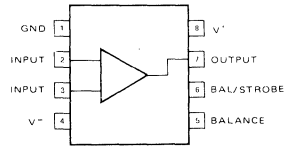
ORDER PART NO.
LM111F/LM211F/LM211N-14
LM311F/LM311N-14

T PACKAGE



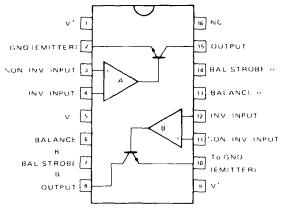
ORDER PART NO.
LM111T/LM211T/LM311T

N PACKAGE



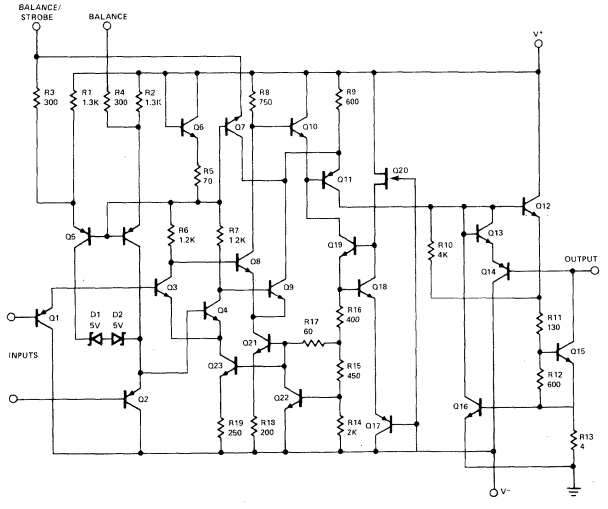
ORDER PART NO.
LM211N/LM311N

F PACKAGE



ORDER PART NO.
LH2111F/LH2211F/LH2311F

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Total supply voltage	36	V
Output to negative supply voltage:		
LM111/LM211, LH2111/LH2211	50	V
LM311, LH2311	40	V
Ground to negative supply voltage	30	V
Differential input voltage	±30	V
Input voltage[1]	±15	V
Power dissipation[2]	500	mW
Output short circuit duration	10	sec
Operating temperature range		
LM111, LH2111	-55 to +125	°C
LM211, LH2211	-25 to +85	°C
LM311, LH2311	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

DC ELECTRICAL CHARACTERISTICS 1,2,3

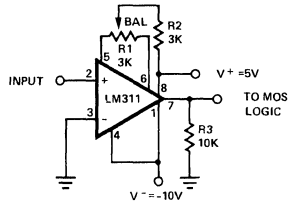
PARAMETER	TEST CONDITIONS	LM111/LM211/LH2111/LH2211			LM311/LH2311			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage[4]	$T_A = 25°C$, $R_S \leq 50k\Omega$		0.7	3.0		2.0	7.5	mV
Input offset current[4]	$T_A = 25°C$		4.0	10		6.0	50	nA
Input bias current	$T_A = 25°C$		60	100		100	250	nA
Voltage gain	$T_A = 25°C$		200			200		V/mV
Response time[5]	$T_A = 25°C$		200			200		ns
Saturation voltage	$V_{IN} \leq -5mV$, $I_{OUT} = 50mA$							
	$T_A = 25°C$		0.75	1.5		0.75	1.5	V
Strobe on current	$T_A = 25°C$		3.0			3.0		mA
Output leakage current	$V_{IN} \geq 5mV$, $V_{OUT} = 35V$							
	$T_A = 25°C$, $I_{STROBE} = 3mA$		0.2	10		0.2	50	nA
Input offset voltage[4]	$R_S \leq 50k\Omega$			4.0			10	mV
Input offset current[4]				20			70	nA
Input bias current				150			300	nA
Input voltage range			±14			±14		V
Saturation voltage	V+ ≥ 4.5V, V- = 0							
	$V_{IN} \leq -6mV$, $I_{SINK} \leq 8mA$		0.23	0.4		0.23	0.4	V
Output leakage current	$V_{IN} \geq 5mV$, $V_{OUT} = 35V$		0.1	0.5				μA
Positive supply current	$T_A = 25°C$		5.1	6.0		5.1	7.5	mA
Negative supply current	$T_A = 25°C$		4.1	5.0		4.1	5.0	mA

NOTES

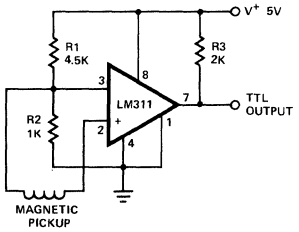
1. This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.
2. The maximum junction temperature of the LM311, LH2311 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, in the N package, a thermal resistance of 162°C/W, and °C/W for the Ceramic package. The maximum junction temperature of the LM111, LH2111 is 150°C, while that of the LM211, LH2111 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient. The thermal resistance of the Cerdip package is 110°C/W, junction to ambient.
3. These specifications apply for $V_S = \pm 15V$ and $0°C < T_A < 70°C$ unless otherwise specified. With the LM211, LH2111 however, all temperature specifications are limited to $-25°C \leq T_A \leq 85°C$ and for the LM111 and LH2111 are limited to $-55°C < T_A < 125°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.
4. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
5. The response time specified (see definitions) is for a 100mV input step with 5mV overdrive.

TYPICAL APPLICATIONS

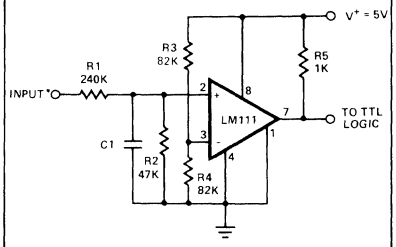
ZERO CROSSING DETECTOR DRIVING MOS LOGIC



DETECTOR FOR MAGNETIC TRANSDUCER



TTL INTERFACE WITH HIGH LEVEL LOGIC



*Values shown are for a 0 to 30V logic swing and a 15V threshold.

†May be added to control speed and reduce susceptability to noise spikes.

LM119/219/319-F,K,N

DESCRIPTION

The LM119 series are precision high speed dual comparators fabricated on a single monolithic chip. They are designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Further, they have higher gain and lower input currents than devices like the μA710. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25mA.

Although designed primarily for applications requiring operation from digital logic supplies, the LM119 series are fully specified for power supplies up to ±15V. It features faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range and low package count make the LM119 much more versatile than older devices like the μA711.

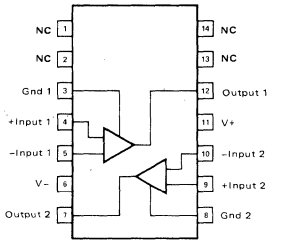
The LM119 is specified from -55°C to +125°C, the LM219 is specified from -25°C to +85°C, and the LM319 is specified from 0°C to +70°C.

FEATURES

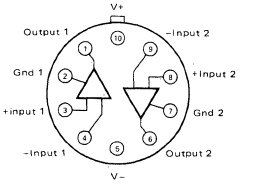
- **Two independent comparators**
- **Operates from a single 5V supply**
- **Typically 80ns response time at ±15V**
- **Minimum fan-out of 3 (each side)**
- **Maximum input current of 1μA over temperature**
- **Inputs and outputs can be isolated from system ground**
- **High common mode slew rate**
- **Mil std 883 A, B, C available**

PIN CONFIGURATIONS

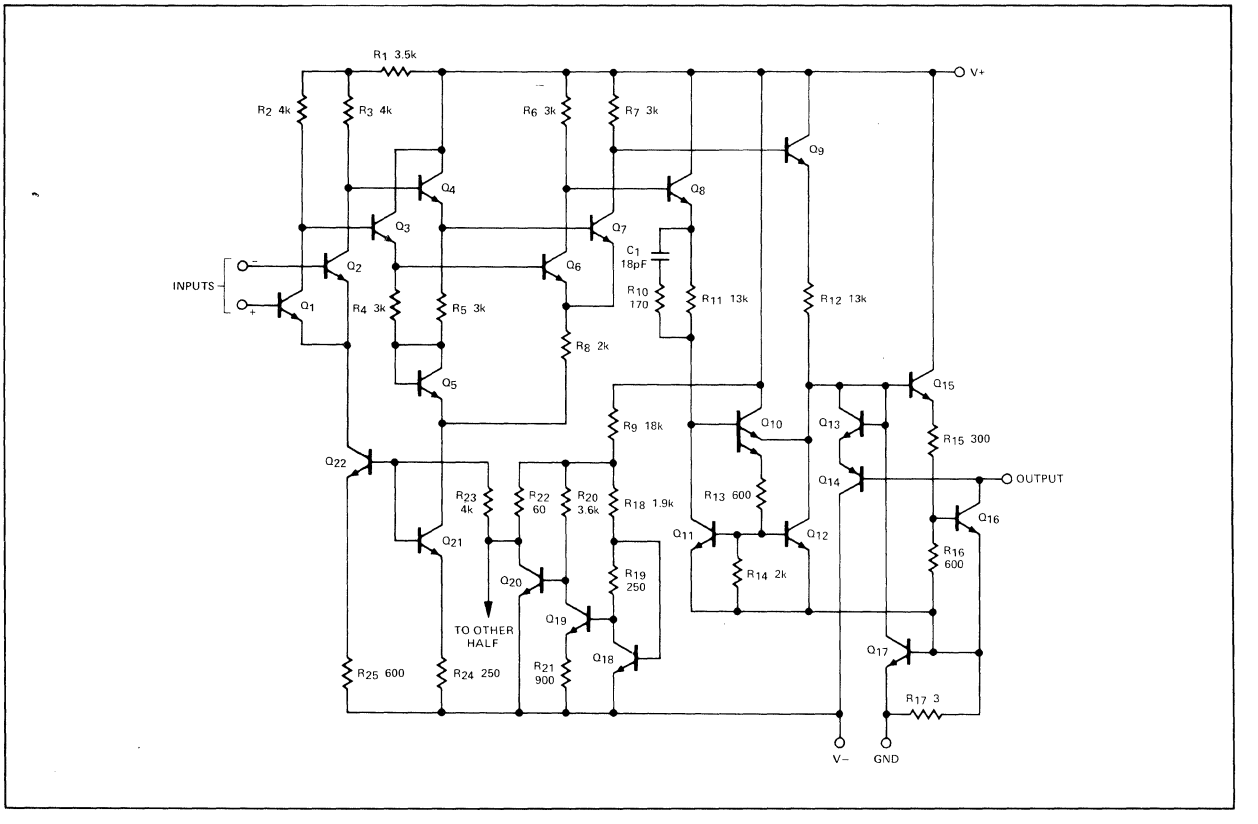
F,N PACKAGE



K PACKAGE



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Total supply voltage	36	V
Output to negative supply voltage	36	V
Ground to negative supply voltage	25	V
Ground to positive supply voltage	18	V
Differential input voltage	±5	V
Input voltage[1]	±15	V
Power dissipation[2]	500	mW
Output short circuit duration	10	s
Operating temperature range		
LM119	-55 to +125	°C
LM219	-25 to +85	°C
LM319	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

NOTES

1. For supply voltages less than ±15V, the absolute maximum rating is equal to the supply voltage.
2. The absolute maximum junction temperature is 150°C. Device dissipation must be derated as follows:
   N/K package—150°C/watt above 75°C
   F package —110°C/watt above 95°C

DC ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, for LM119, $-55°C \le T_A \le 125°C$; LM219, $-25°C \le T_A \le 85°C$; LM319, $0°C \le T_A \le 70°C$; unless otherwise specified.

	PARAMETER	TEST CONDITIONS	LM119/219			LM319			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[1,2]	$R_S \le 5K\Omega$, $T_A = 25°C$		0.7	4.0		2.0	8.0	mV
		Over temp.			7			10	mV
I_{OS}	Input offset current[1,2]	$T_A = 25°C$		30	75		80	200	nA
		Over temp.			100			300	nA
I_B	Input bias current[1]	$T_A = 25°C$		150	500		250	1000	nA
		Over temp.			1000			1200	nA
A_V	Voltage gain	$T_A = 25°C$	10	40		8	40		V/mV
V_{OL}	Saturation voltage	$V_{IN} = 5mV$, $I_{OUT} = 25mA$, $T_A = 25°C$		0.75	1.5				V
		$V_{IN} = 10mV$, $I_{OUT} = 25mA$, $T_A = 25°C$					0.75	1.5	V
		$V^+ \ge 4.5V$, $V^- = 0$							
		$V_{IN} = 6mV$, $I_{OUT} = 3.2mA$							
		$T_A \ge 0°C$		0.23	0.4				V
		$T_A \le 0°C$			0.6				
		$V_{IN} = 10mV$, $I_{OUT} = 3.2mA$					0.3	0.4	V
I_{OH}	Output leakage current	$V^- = 0V$, $V_{IN} = 5mV$							
		$V_{OUT} = 35V$, $T_A = 25°C$		0.2	2				μA
		Over temp.		1	10				μA
		$V^- = 0V$, $V_{IN} = 10mV$							
		$V_{OUT} = 35V$, $T_A = 25°C$					0.2	10	μA
V_{IN}	Input voltage range	$V_S = \pm 15V$		±13			±13		V
		$V^+ = 5V$, $V^- = 0V$	1		3	1		3	V
V_{ID}	Differential input voltage				±5			±5	V
I^+	Positive supply current	$V^+ = 5V$, $V^- = 0V$, $T_A = 25°C$		4.3			4.3		mA
I^+	Positive supply current	$V_S = \pm 15V$, $T_A = 25°C$		8.0	11.5		8.0	12.5	mA
I^-	Negative supply current	$V_S = \pm 15V$, $T_A = 25°C$		3.0	4.5		3.0	5.0	mA

NOTES

1. V_{OS}, I_{OS} and I_B specifications apply for a supply voltage range of $V_S = \pm 15V$ down to a single 5V supply.
2. The offset voltages and offset currents given are the maximum values required to drive the output to within 1 volt of either supply with a 1mA load. Thus these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

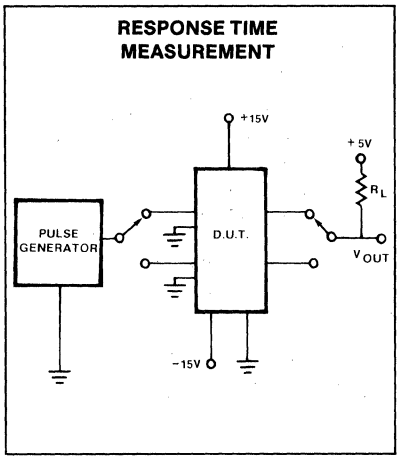
AC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Response time*	$V_S = \pm 15V$, $T_A = 25°C$ $R_L = 500\Omega$ (see test figure)		80		ns

*NOTE

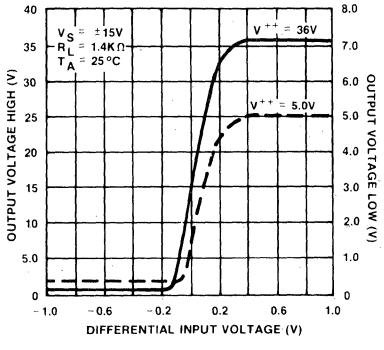
The response time specified is for a 100mV step with 5mV overdrive.

TEST CIRCUIT

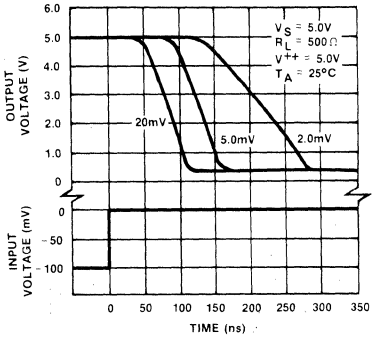


TYPICAL PERFORMANCE CHARACTERISTICS

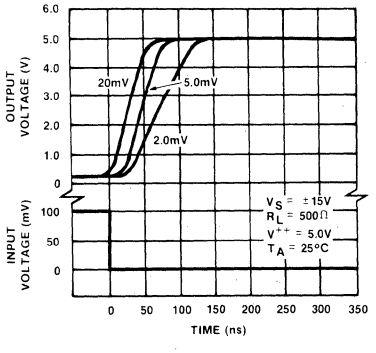
TRANSFER FUNCTION



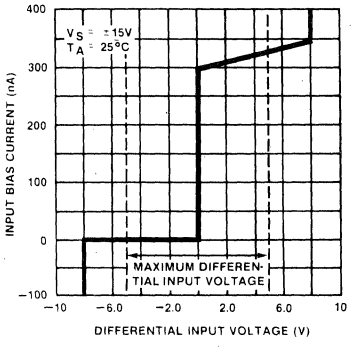
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



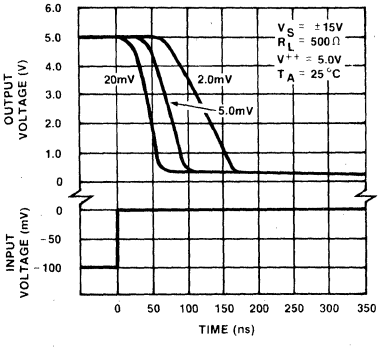
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



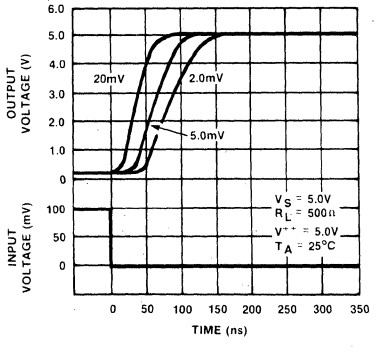
INPUT CHARACTERISTICS



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

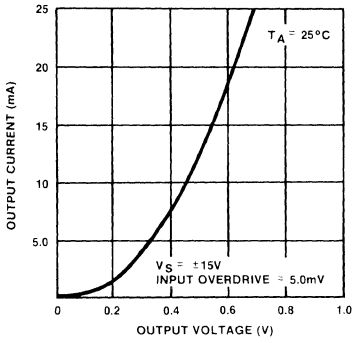


RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

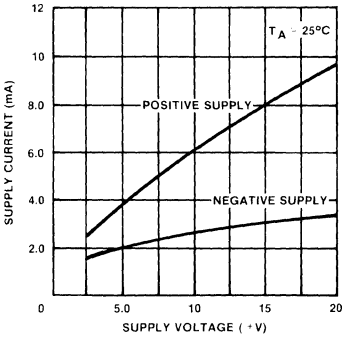


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

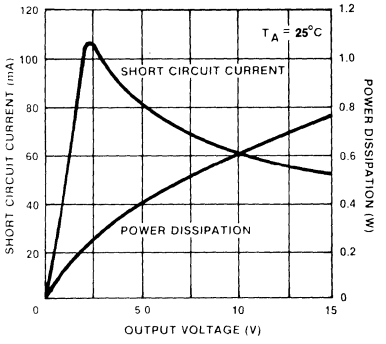
OUTPUT SATURATION VOLTAGE



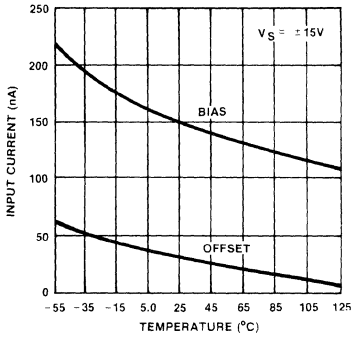
SUPPLY CURRENT



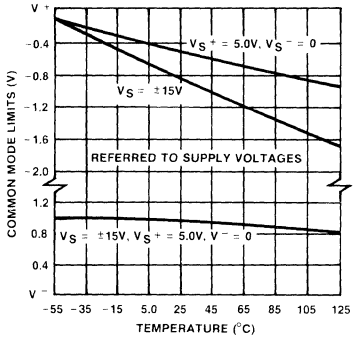
OUTPUT LIMITING CHARACTERISTICS



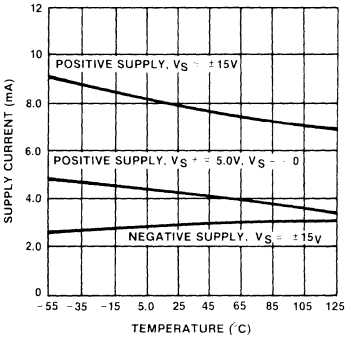
INPUT CURRENTS (LM119/219)



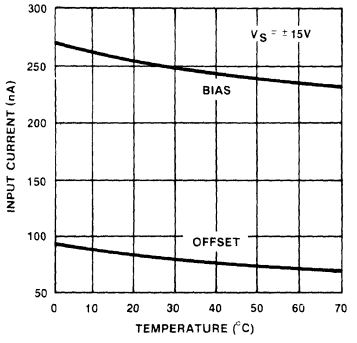
COMMON MODE LIMITS (LM119/219)



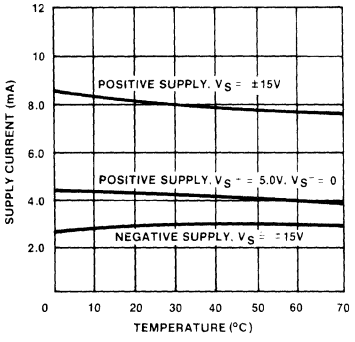
SUPPLY CURRENT (LM119/219)



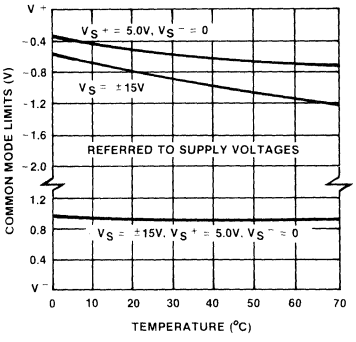
INPUT CURRENTS (LM319)



SUPPLY CURRENTS (LM319)

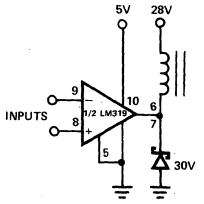


COMMON MODE LIMITS (LM319)

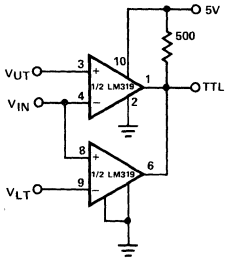


TYPICAL APPLICATIONS

RELAY DRIVER

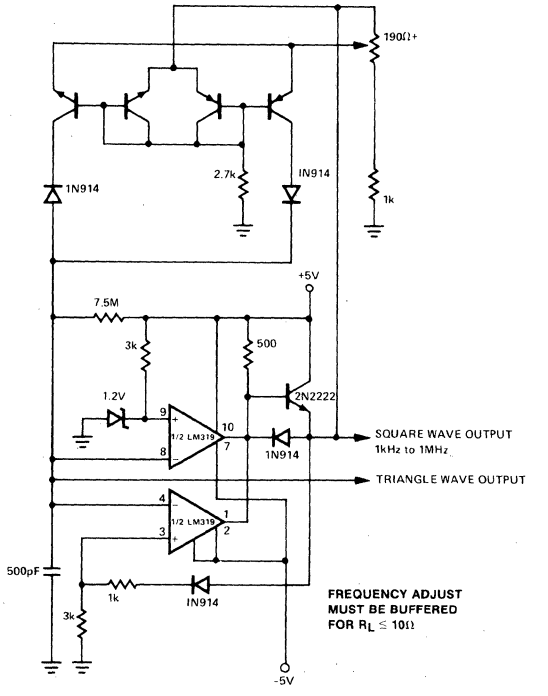


WINDOW DETECTOR



$V_{OUT} = 5V$ for $V_{LT} < V_{IN} < V_{UT}$
$V_{OUT} = 0$ for $V_{IN} < V_{LT}$ or $V_{IN} > V_{UT}$

WIDE RANGE VARIABLE OSCILLATOR



LM139/A/239/A/339/A/2901-F,N • MC3302-N

DESCRIPTION

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2.0mV max for each comparator which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common mode voltage range includes ground, even though operated from a single power supply voltage.

The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM139 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

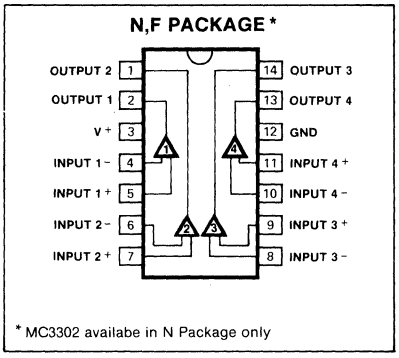
FEATURES

- **Wide single supply voltage range 2.0Vdc to 36Vdc or dual supplies ±1.0Vdc to ±18Vdc**
- **Very low supply current drain (0.8mA) independent of supply voltage (1.0mW/-comparator at 5.0Vdc)**
- **Low input biasing current 25nA**
- **Low input offset currrent ±5nA and offset voltage ±3mV**
- **Input common-mode voltage range includes ground**
- **Differential input voltage range equal to the power supply voltage.**
- **Low output 250mV at 4mA saturation voltage**
- **Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems.**

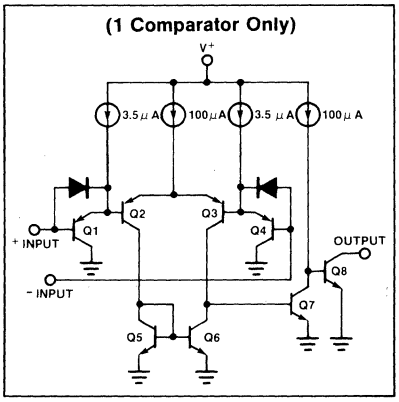
APPLICATIONS

- **A/D converters**
- **Wide range VCO**
- **MOS clock generator**
- **High voltage logic gate**
- **Multivibrators**

PIN CONFIGURATION



EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V_{CC} supply voltage	36 or ±18	Vdc
Differential input voltage	36	Vdc
Input voltage	-0.3 to +36	Vdc
Power dissipation[1]		
Molded DIP	570	mW
CERDIP	900	mW
Output short circuit to ground[2]	Continuous	
Input current (V_{IN} < -0.3Vdc)[3]	50	mA
Operating temperature range		
LM139/139A	-55 to +125	°C
LM239/239A	-25 to +85	°C
LM339/339A	0 to +70	°C
LM2901/MC3302	-40 to +85	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 10 sec.)	300	°C

LM139/A/239/A/339/A/2901-F,N • MC3302-N

DC ELECTRICAL CHARACTERISTICS V+ = 5Vdc, LM139A/LM139: $-55°C \le T_A \le 125°C$ unless otherwise specified
LM239: $-25°C \le T_A \le 85°C$ unless otherwise specified
LM339: $0°C \le T_A \le 70°C$ unless otherwise specified

PARAMETER	TEST CONDITIONS	LM139			LM239/339			LM139A			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS} Input offset voltage[5]	$T_A = 25°C$ Over temp.		±2.0	±5.0 9.0		±2.0	±5.0 9.0		±1.0	±2.0 4.0	mV
V_{CM} Input common mode voltage range[6]	$T_A = 25°C$ Over temp.	0 0		V+-1.5 V+-2.0	0 0		V+-15 V+-20	0 0		V+-1.5 V+-2.0	V
V_{IDR} Differential input voltage[4]	Keep all V_{IN}'s ≥ 0Vdc (or V-if need)			V+			V+			V+	V
I_B Input bias current[7]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25°C$ Over temp.		25	100 300		25	250 400		25	100 300	nA
I_{OS} Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25°C$ Over temp.		±3.0	±25 ±100		±5.0	±50 ±150		±3.0	±25 ±100	nA nA
I_{OL} Output sink current	$V_{IN(-)} \ge 1Vdc$, $V_{IN(+)} = 0$, $V_O \le 1.5Vdc$, $T_A = 25°C$	6.0	16		6.0	16		6.0	16		mA
I_{OH} Output leakage current	$V_{IN(+)} \ge 1Vdc$, $V_{IN(-)} = 0$ $V_O = 5Vdc$, $T_A = 25°C$ $V_O = 30Vdc$, over temp.		0.1	 1.0		0.1	 1.0		0.1	 1.0	nA μA
I_{CC} Supply current[9]	$R_L = \infty$ on comparators, $T_A = 25°C$		0.8	2.0		0.8	2.0		0.8	2.0	mA
A_V Voltage gain	$R_L \ge 15k\Omega$, V+ = 15Vdc	50	200		50	200		50	200		V/mV
V_{OL} Saturation voltage	$V_{IN(-)} \ge 1Vdc$, $V_{IN(+)} = 0$, $I_{SINK} \le 4mA$ $T_A = 25°C$ Over temp.		250	400 700		250	400 700		250	400 700	mV
T_{LSR} Large signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4Vdc$, $V_{RL} = 5Vdc$, $R_L = 5.1k\Omega$, $T_A = 25°C$		300			300			300		ns
T_R Response time[8]	$V_{RL} = 5Vdc$, $R_L = 5.1k\Omega$, $T_A = 25°C$		1.3			1.3			1.3		μs

DC ELECTRICAL CHARACTERTISICS

(Cont'd) V+ = 5Vdc, LM339A: 0°C ≤ T_A ≤ 70°C unless otherwise specified
LM239A: -25°C ≤ T_A ≤ 85°C unless otherwise specified
LM2901/LM3302: -40°C ≤ T_A ≤ 85°C unless otherwise specified

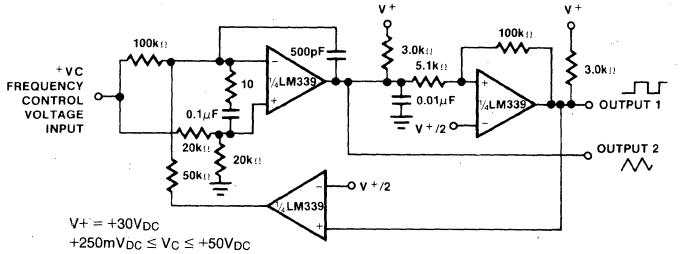
PARAMETER	TEST CONDITIONS	LM239A/339A			LM2901			MC3302			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS} Input offset voltage[5]	T_A = 25°C Over temp.		±1.0	±2.0 ±4.0		±2.0 ±9	±7.0 ±15		±3.0	±20 ±40	mV
V_{CM} Input common mode voltage range[6]	T_A = 25°C Over temp.	0 0		V+-1.5 V+-2.0	0 0		V+-1.5 V+-2.0			V+-1.5 V+-2.0	V
V_{IDR} Differential input voltage[4]	Keep all $V_{IN's} \geq$ 0Vdc (or V-if need)			V+			V+			V+	V
I_B Input bias current[7]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range T_A = 25°C Over temp.		25	250 400		25 200	250 500		25	500 1000	nA
I_{OS} Input offset current	$I_{IN(+)} - I_{IN(-)}$ T_A = 25°C Over temp.		±5.0	±50 ±150		±5 ±50	±50 ±200		±5	±100 ±300	nA nA
I_{OL} Output sink current	$V_{IN(-)} \geq$ 1Vdc, $V_{IN(+)}$ = 0, $V_O \leq$ 1.5Vdc, T_A = 25°C V_O = 800mV, Over temp.	6.0	16		6.0	16		2.0			mA
I_{OH} Output leakage current	$V_{IN(+)} \geq$ 1Vdc, $V_{IN(-)}$ = 0 V_O = 5Vdc, T_A = 25°C V_O = 30Vdc, Over temp.		0.1	 1.0		0.1	 1.0		0.1	 1.0	nA μA
I_{CC} Supply current[9]	R_L = ∞ on comparators, V+ = 5Vdc T_A = 25°C V+ = 30V, T_A = 25°C		0.8	2.0		0.8 1.0	2.0 2.5		0.8	2.0	mA
A_V Voltage gain	$R_L \geq$ 15kΩ, V+ = 15Vdc	50	200		25	100		2	100		V/mV
V_{OL} Saturation voltage	$V_{IN(-)} \geq$ 1Vdc, $V_{IN(+)}$ = 0, $I_{SINK} \leq$ 4mA T_A = 25°C Over temp. I_{SINK} = 2mA, V+ = 5V to 28V, T_A = 25°C		250	400 700		400	400 700		150	400 700	mV
T_{LSR} Large signal response time	V_{IN} = TTL logic swing, V_{REF} = 1.4Vdc, V_{RL} = 5Vdc, R_L = 5.1kΩ, T_A = 25°C		300			300			300		ns
T_R Response time[8]	V_{RL} = 5Vdc, R_L = 5.1kΩ, T_A = 25°C		1.3			1.3			1.3		μs

NOTES

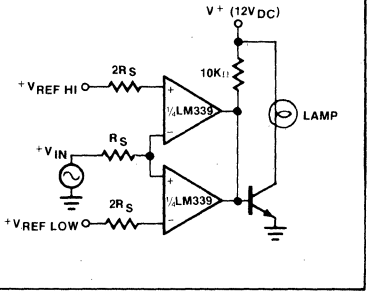
1. For operating at high temperatures, the LM339/339A, LM2901 and MC3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM139/139A/239/239A must be derated on a 150°C maximum junction temperature. The low power dissipation and the "On-Off" characteristics of the outputs keep the chip dissipation very small ($P_D \leq 100mW$), provided the output transistors are allowed to saturate.
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3Vdc.
4. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3Vdc (or 0.3Vdc below the magnitude of the negative power supply, if used).
5. At output switch point, $V_O \cong 1.4Vdc$, $R_S = 0\Omega$ with V+ from 5Vdc to 30Vdc; and over the full input common-mode range (0Vdc to V+ -1.5Vdc).
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ -1.5V, but either or both inputs can go to 30Vdc without damage.
7. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
8. The response time specified is for a 100mV input step with a 5mV overdrive. For larger overdrive signals, 300ns can be obtained, see typical performance characteristics section.
9. The MC3302 has supply current specified with a voltage range of 5 to 28 volts.

TYPICAL APPLICATIONS

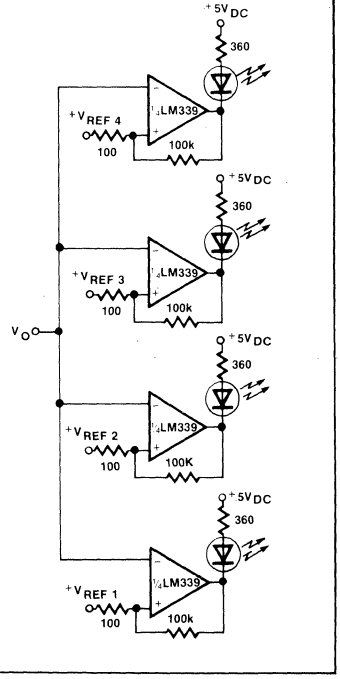
TWO-DECADE HIGH-FREQUENCY VCO



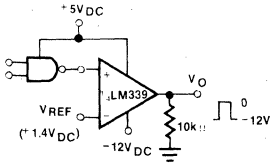
LIMIT COMPARATOR



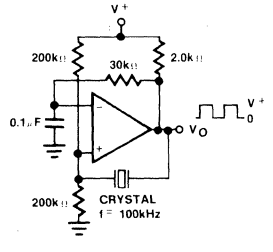
VISIBLE VOLTAGE INDICATOR



TTL TO MOS LOGIC CONVERTER

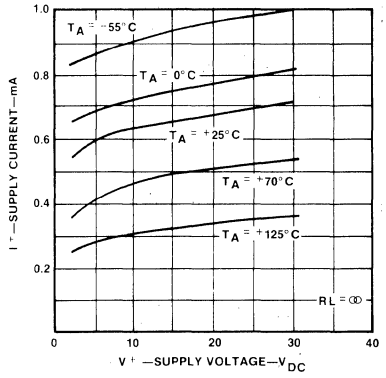


CRYSTAL CONTROLLED OSCILLATOR

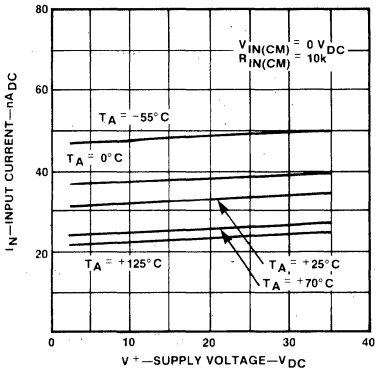


TYPICAL PERFORMANCE CHARACTERISTICS

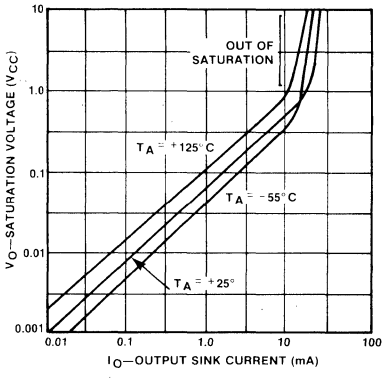
SUPPLY CURRENT



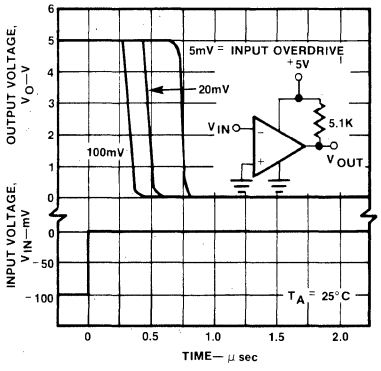
INPUT CURRENT



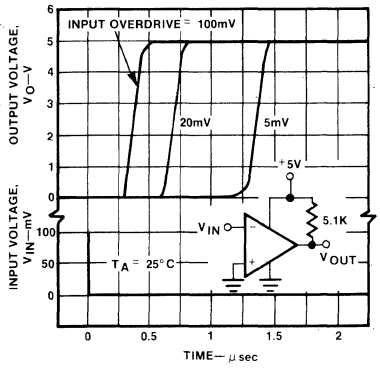
OUTPUT SATURATION VOLTAGE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES— NEGATIVE TRANSITION



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES— POSITIVE TRANSITION



LM193/293/393/193A/293A/393A/2903-N,T

DESCRIPTION

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common mode voltage range includes ground, even though operated from a single power supply voltage.

The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

FEATURES

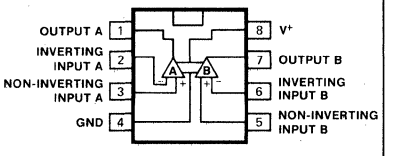
- **Wide single supply voltage range 2.0Vdc to 36Vdc or dual supplies ±1.0Vdc to ±18Vdc**
- **Very low supply current drain (0.8mA) independent of supply voltage (2.0mW/-comparator at 5.0Vdc)**
- **Low input biasing current 25nA**
- **Low input offset current ±5nA and offset voltage ±3mV**
- **Input common-mode voltage range includes ground**
- **Differential input voltage range equal to the power supply voltage.**
- **Low output 250mV at 4mA saturation voltage**
- **Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems.**

APPLICATIONS

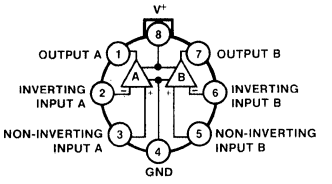
- **A/D converters**
- **Wide range VCO**
- **MOS clock generator**
- **High voltage logic gate**
- **Multivibrators**

PIN CONFIGURATIONS

N PACKAGE

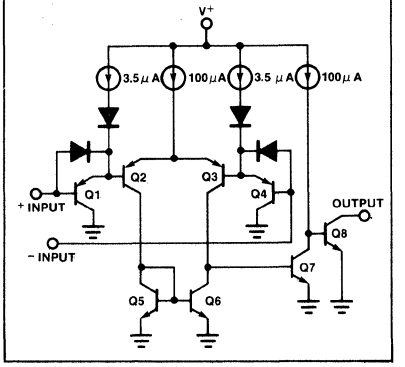


T PACKAGE



EQUIVALENT CIRCUIT

(One Comparator Only)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V_{CC} supply voltage	36 or ±18	Vdc
Differential input voltage	36	Vdc
Input voltage	-0.3 to +36	Vdc
Power dissipation[1]		
Molded DIP	570	mW
Metal can	900	mW
Output short circuit to ground[2]	Continuous	
Input current (V_{IN} < -0.3Vdc)[3]	50	mA
Operating temperature range		
LM193/193A	-55 to +125	°C
LM293/293A	-25 to +85	°C
LM393/393A	0 to +70	°C
LM2903	-40 to +85	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 10 sec.)	300	°C

LM193/293/393/193A/293A/393A/2903-N,T

DC ELECTRICAL CHARACTERISTICS

V+ = 5Vdc, LM193/193A: $-55°C \leq T_A \leq +125°C$ unless otherwise specified.
LM293/293A: $-25°C \leq T_A \leq +85°C$ unless otherwise specified.
LM393/393A: $0°C \leq T_A \leq +70°C$ unless otherwise specified.
LM2903: $-40°C \leq T_A \leq +85°C$ unless otherwise specified.[7]

PARAMETER		TEST CONDITIONS	LM193A			LM293A/393A			LM2903			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[5]	$T_A = 25°C$ Over temp.		±1.0	±2.0 ±4.0		±1.0	±2.0 ±4.0		±2.0 ±9	±7.0 ±15	mV
V_{CM}	Input common mode voltage range[6,10]	$T_A = 25°C$ Over temp.	0 0		V+-1.5 V+-2.0	0 0		V+-1.5 V+-2.0	0 0		V+-1.5 V+-2.0	V
V_{IDR}	Differential input voltage[4]	Keep all V_{IN}'s ≥ 0Vdc (or V-if need)			V+			V+			V+	V
I_B	Input bias current[8]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25°C$ Over temp.		25	100 300		25	250 400		25 200	250 500	nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25°C$ Over temp.		±3.0	±25 ±100		±5.0	±50 ±150		±5 ±50	±50 ±200	nA nA
I_{OL}	Output sink current	$V_{IN(-)} \geq 1Vdc$, $V_{IN(+)} = 0$, $V_O \leq 1.5Vdc$, $T_A = 25°C$	6.0	16		6.0	16		6.0	16		mA
I_{OH}	Output leakage current	$V_{IN(+)} \geq 1Vdc$, $V_{IN(-)} = 0$, $V_O = 30Vdc$ Over temp. $V_O = 5Vdc$, $T_A = 25°C$		0.1	1.0		0.1	1.0		0.1	1.0	μA na
I_{CC}	Supply current	$R_L = \infty$ on both comparators. $T_A = 25°C$ V+ = 30V, over temp.		0.8 1	1 2.5		0.8 1	1 2.5		0.8 1	1 2.5	mA
A_V	Voltage gain	$R_L \geq 15k\Omega$, V+ = 15Vdc	50	200		50	200		25	100		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)} \geq 1Vdc$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4mA$ $T_A = 25°C$ Over temp.		250	400 700		250	400 700		400	400 700	mV
T_{LSR}	Large signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4Vdc$, $V_{RL} = 5Vdc$, $R_L = 5.1k\Omega$, $T_A = 25°C$		300			300			300		ns
T_R	Response time[9]	$V_{RL} = 5Vdc$, $R_L = 5.1k\Omega$, $T_A = 25°C$		1.3			1.3			1.3		μs

LM193/293/393/193A/293A/393A/2903-N,T

DC ELECTRICAL CHARACTERISTICS (Cont'd) V+ = 5Vdc, LM193/193A: $-55°C \le T_A \le +125°C$ unless otherwise specified.
LM293/293A: $-25°C \le T_A \le +85°C$ unless otherwise specified.
LM393/393A: $0°C \le T_A \le +70°C$ unless otherwise specified.
LM2903: $-40°C \le T_A \le +85°C$ unless otherwise specified.[7]

PARAMETER		TEST CONDITIONS	LM193			LM293/393			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[5]	$T_A = 25°C$ Over temp.		±2.0	±5.0 ±9.0		±2.0	±5.0 ±9.0	mV
V_{CM}	Input common mode voltage range[6,10]	$T_A = 25°C$ Over temp.	0 0		V±-1.5 V±-2.0	0 0		V±-1.5 V±-2.0	V
V_{IDR}	Differential input voltage[4]	Keep all $V_{IN's} \ge 0Vdc$ (or V-if need)			V+			V+	V
I_B	Input bias current[8]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25°C$ Over temp.		25	100 300		25	250 400	nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25°C$ Over temp.		±3.0	±25 ±100		±5.0	±50 ±150	nA nA
I_{OL}	Output sink current	$V_{IN(-)} \ge 1Vdc$, $V_{IN(+)} = 0$, $V_O \le 1.5Vdc$, $T_A = 25°C$	6.0	16		6.0	16		mA
I_{OH}	Output leakage current	$V_{IN(+)} \ge 1Vdc$, $V_{IN(-)} = 0$ $V_O = 5Vdc$, $T_A = 25°C$ $V_O = 30Vdc$, over temp.		0.1	 1.0		0.1	 1.0	nA μA
I_{CC}	Supply current	$R_L = \infty$ on both comparators $T_A = 25°C$ V+ = 30V, over temp.		0.8	1 2.5		0.8	1 2.5	mA
A_V	Voltage gain	$R_L \ge 15K\Omega$, V+ = 15Vdc	50	200		50	200		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)} \ge 1Vdc$, $V_{IN(+)} = 0$, $I_{SINK} \le 4mA$ $T_A = 25°C$ Over temp.		250	400 700		250	400 700	mV
T_{LSR}	Large signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4Vdc$, $V_{RL} = 5Vdc$, $R_L = 5.1k\Omega$, $T_A = 25°C$		300			300		ns
T_R	Response time[9]	$V_{RL} = 5Vdc$, $R_L = 5.1k\Omega$, $T_A = 25°C$		1.3			1.3		μs

NOTES

1. For operating at high temperatures, the LM393/393A and LM2903 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM193/193A/293/293A must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "On-Off" characteristics of the outputs keeps the chip dissipation very small ($P_D \le 100mW$), provided the output transistors are allowed to saturate.
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3Vdc.
4. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3Vdc (Vdc below the magnitude of the negative power supply, if used).
5. At output switch point, $V_O \cong 1.4Vdc$, $R_S = 0\Omega$ with V+ from 5Vdc to 30Vdc; and over the full input common-mode range (0Vdc to V+ -1.5Vdc).
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ -1.5V, but either or both inputs can go to 30Vdc without damage.
7. With the LM293/293A, all temperature specifications are limited to $-25°C \le T_A \le +85°C$ and the LM393/393A, all temperature specifications are limited to $0°C \le T_A \le +70°C$. The LM2903 is limited to $-40°C \le T_A \le 85°C$.
8. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
9. The response time specified is for a 100mV input step with a 5mV overdrive. For larger overdrive signals, 300ns can be obtained, see typical performance characteristics section.
10. For input signals that exceed V_{CC}, only the overdriven comparator is affected. With a 5V supply, V_{IN} should be limited to 25V max., and a limiting resistor should be used on all inputs that might exceed the positive supply.

NE521-F,N

FEATURES

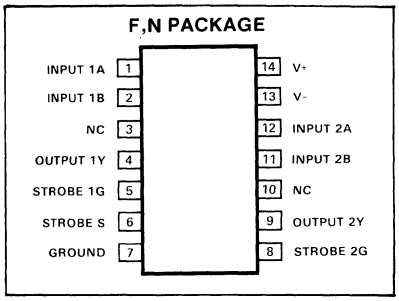
- 12ns maximum guaranteed propagation delay
- 20μA maximum input bias current
- TTL compatible strobes and outputs
- Large common mode input voltage range
- Operates from standard supply voltages
- Military qualifications pending

APPLICATIONS

- MOS memory sense amp
- A-to-D conversion
- High speed line receiver

PIN CONFIGURATION

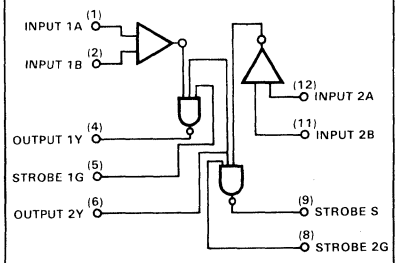
F,N PACKAGE



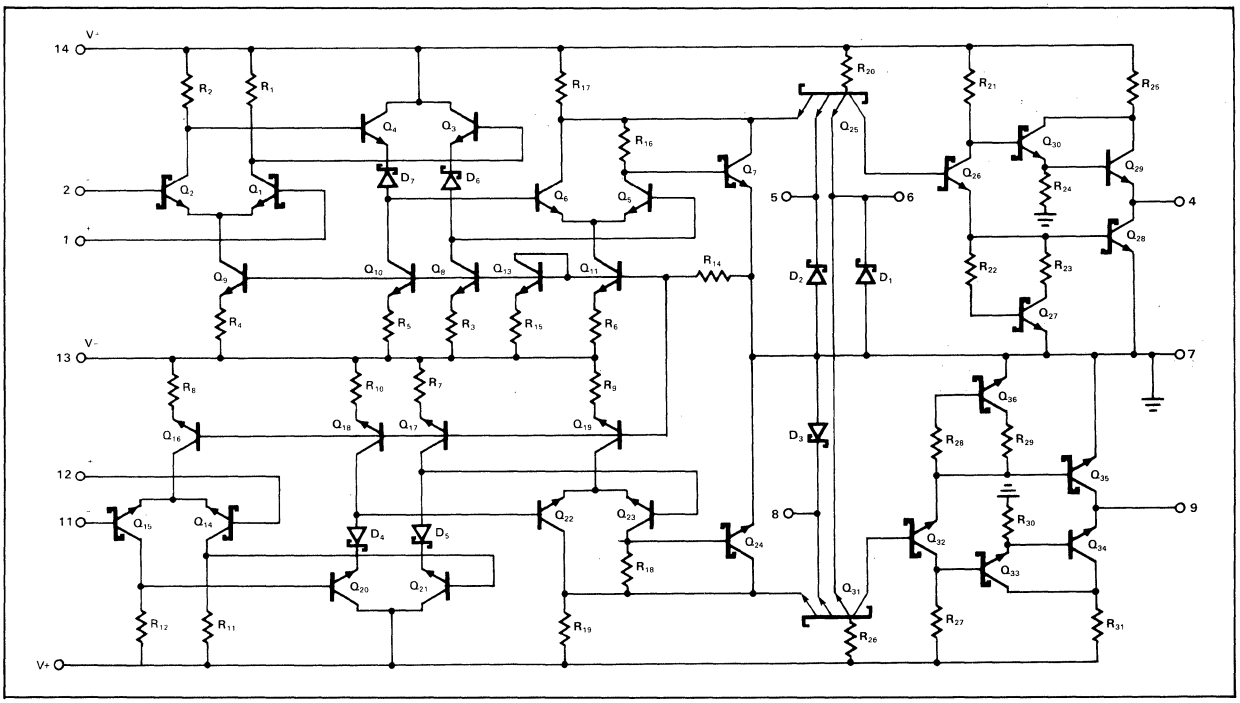
ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
	Supply voltage		V
V+	Positive	+7	
V-	Negative	-7	
V_{IDR}	Differential input voltage	±6	V
V_{IN}	Input voltage		V
	Common mode	±5	
	Strobe/gate	+5.25	
P_D	Power dissipation	600	mW
T_A	Operating temperature range	0 to 70	°C
T_{stg}	Storage temperature range	-65 to +150	°C
	Lead temperature (solder, 60 sec)	+300	°C

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS $V+ = +5V, V- = -5V, T_A = 0$ to 70°C unless otherwise specified

PARAMETER		TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
V_{OS}	Input offset voltage	V+ = +4.75V, V- = -4.75V				mV
	At 25°C			6	7.5	
	Over temperature range				10	
I_{BIAS}	Input bias current	V+ = +5.25V, V- = -5.25V				μA
	At 25°C			7.5	20	
	Over temperature range				40	
I_{OS}	Input offset current	V+ = +5.25V, V- = -5.25V				μA
	At 25°C			1.0	5	
	Over temperature range				12	
V_{CM}	Common mode voltage range	V+ = +4.75V, V- = -4.75V	±3			V
	Input current	V+ = +5.25V, V- = -5.25V				
I_{IH}	High	V_{IH} = 2.7V				
		1G or 2G strobe			50	μA
		Common strobe S			100	μA
I_{IL}	Low	V_{IL} = 0.5V				
		1G or 2G strobe			-2.0	mA
		Common strobe S			-4.0	mA
	Output voltage	$V_{I(S)}$ = 2.0V				V
V_{OH}	High	V+ = +4.75V, V- = -4.75V, I_{LOAD} = -1mA	2.7	3.4		
V_{OL}	Low	V+ = +5.25V, V- = -5.25V, I_{LOAD} = 20mA			0.5	
	Supply voltage					V
V+	Positive		4.75	5.0	5.25	
V-	Negative		-4.75	-5.0	-5.25	
	Supply current	V+ = 5.25V, V- = -5.25V, T_A = 25°C				mA
I_{CC+}	Positive			27	50	
I_{CC-}	Negative			-15	-28	
I_{SC}	Short circuit output current		-40		-100	μA

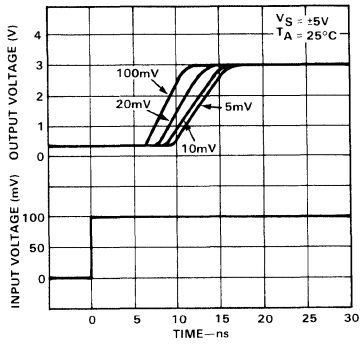
AC ELECTRICAL CHARACTERISTICS $T_A = 25°C, R_L = 280\,\Omega$ C_L = 15pF

PARAMETER		FROM INPUT	TO OUTPUT	LIMITS			UNIT
				Min	Typ	Max	
	Input resistance				4		kΩ
	Input capacitance				3		pF
Large Signal Switching Speed							
	Propagation delay						ns
$t_{PLH(D)}$	Low to high[1]	Amp	Output		8	12	
$t_{PHL(D)}$	High to low[1]	Amp	Output		6	9	
$t_{PLH(S)}$	Low to high[2]	Strobe	Output		4.5	6	
$t_{PHL(S)}$	High to low[2]	Strobe	Output		3.0	4.5	
	Maximum operating frequency			40	55		MHz
Small Signal Switching Speed							
	Propagation delay						ns
PLH(D)	Low to high[3]	Amp	Output		12	18	
PHL(D)	High to low[3]	Amp	Output		10	15	

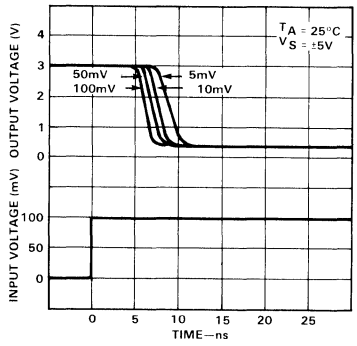
NOTES
1. Response time measured from 0V point of ±100mV p-p 10MHz square wave to the 1.5V point of the output
2. Response time measured from 1.5V point of input to 1.5V point of the output
3. Response time measured from the start of a 100mV input step with 5mV overdrive to the 1.5V point of the output

TYPICAL PERFORMANCE CHARACTERISTICS

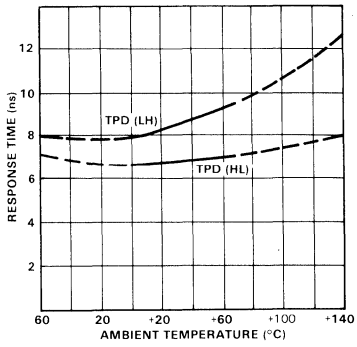
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



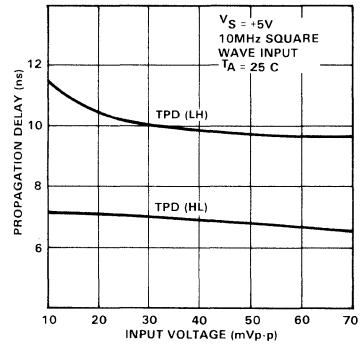
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



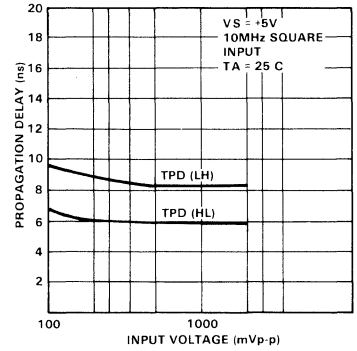
RESPONSE TIME vs TEMPERATURE



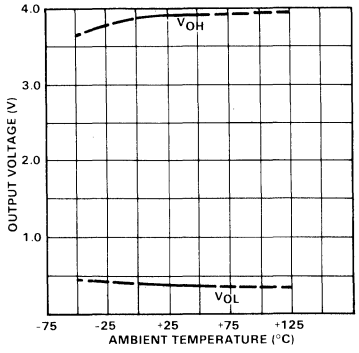
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGE



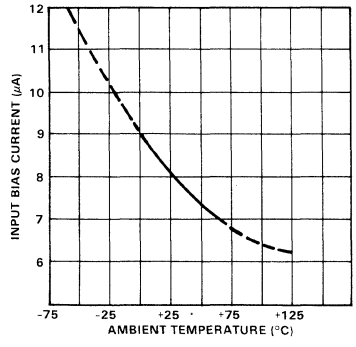
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



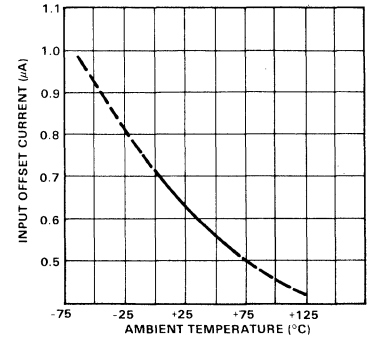
OUTPUT VOLTAGE vs AMBIENT TEMPERATURE



INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE



NE522-F,N

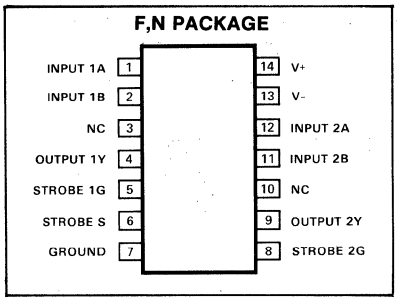
FEATURES

- 15ns maximum guaranteed propagation delay
- 20μA maximum input bias current
- TTL compatible strobes and outputs
- Open collector output for wire-OR'd applications
- Large common mode input voltage range
- Operates from standard supply voltages

APPLICATIONS

- MOS memory sense amp
- A-to-D conversion
- High speed line receiver

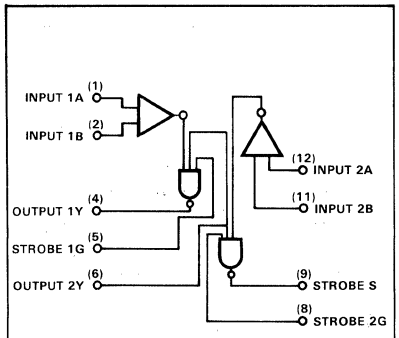
PIN CONFIGURATION



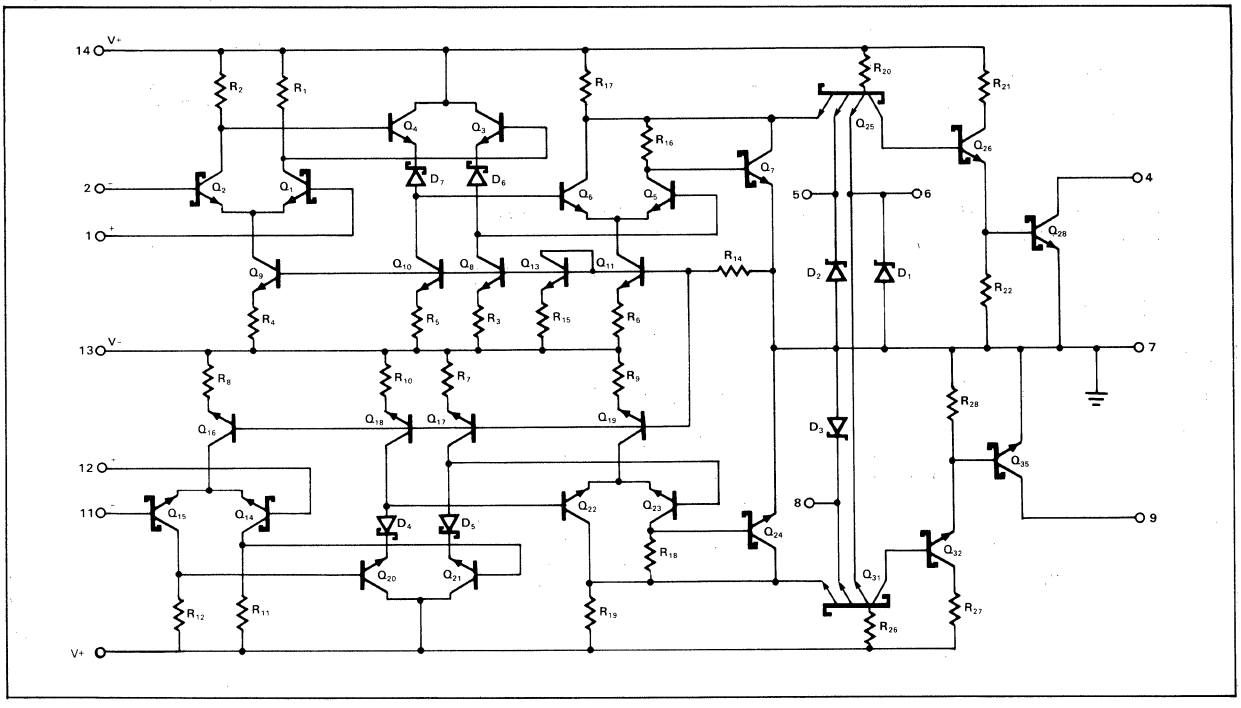
ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
	Supply voltage		V
V+	Positive	+7	
V-	Negative	-7	
V_{IDR}	Differential input voltage	±6	V
V_{IN}	Input voltage		V
	Common mode	±5	
	Strobe/gate	±5.25	
P_D	Power dissipation	600	mW
T_A	Operating temperature range	0 to 70	°C
T_{stg}	Storage temperature range	-65 to +150	°C
	Lead temperature (solder, 60 sec)	+300	°C

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS $V+ = +5V, V- = -5V, T_A = 0$ to 70°C unless otherwise specified

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage	V+ = +4.75V, V- = -4.75V				mV
	At 25°C			6	7.5	
	Over temperature range				10	
I_{BIAS}	Input bias current	V+ = +5.25V, V- = -5.25V				μA
	At 25°C			7.5	20	
	Over temperature range				40	
I_{OS}	Input offset current	V+ = +5.25V, V- = -5.25V				μA
	At 25°C			1.0	5	
	Over temperature range				12	
V_{CM}	Common mode voltage range	V+ = +4.75V, V- = -4.75V	±3			V
	Input current	V+ = +5.25V, V- = -5.25V				
I_{IH}	High	V_{IH} = 2.7V				
		1G or 2G strobe			50	μA
		Common strobe S			100	μA
I_{IL}	Low	V_{IL} = 0.5V				
		1G 2G strobe			-2.0	mA
		Common strobe S			-4.0	mA
	Output voltage					V
V_{OL}	Low	V+ = +5.25V, V- = -5.25V, $V_{I\ (S)}$ = 2.0V			0.5	
	Output current					μA
I_{OH}	High	I_{LOAD} = 20mA, V_{CC+} = +4.75, V_{CC-} = -4.75V, V_{OH} = 5.25V			250	
	Supply voltage					V
V+	Positive		4.75	5.0	5.25	
V-	Negative		-4.75	-5.0	-5.25	
	Supply current	V+ = 5.25V, V- = -5.25V, T_A = 25°C				mA
I_{CC+}	Positive			27	50	
I_{CC-}	Negative			-15	-28	

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C, R_L = 280\Omega, C_L = 15pF$

PARAMETER		FROM INPUT	TO OUTPUT	LIMITS			UNIT
				Min	Typ	Max	
	Input resistance				4		kΩ
	Input capacitance				3		pF
Large Signal Switching Speed							
	Propagation delay						ns
$t_{PLH(D)}$	Low to high[1]	Amp	Output		10	15	
$t_{PHL(D)}$	High to low[1]	Amp	Output		8	12	
$t_{PLH(S)}$	Low to high[2]	Strobe	Output		6	10	
$t_{PHL(S)}$	High to low[2]	Strobe	Output		5	8	
	Maximum operating frequency			25	35		MHz
Small Signal Switching Speed							
	Propagation delay						ns
$t_{PLH(D)}$	Low to high[3]	Amp	Output		17	25	
$t_{PHL(D)}$	High to low[3]	Amp	Output		11	17	

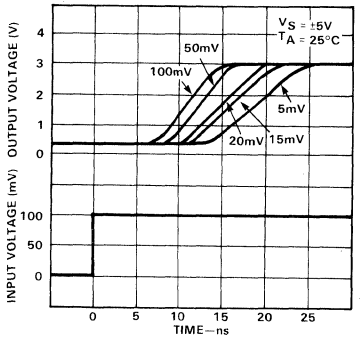
NOTES

1. Response time measured from 0V point of ±100mV p-p 10MHz square wave to the 1.5V point of the output
2. Response time measured from 1.5V point of input to 1.5V point of the output
3. Response time measured from the start of a 100mV input step with 5mV overdrive to the 1.5V point of the output

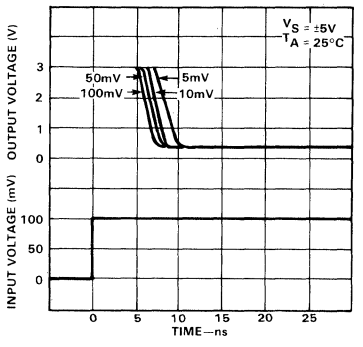
5

TYPICAL PERFORMANCE CHARACTERISTICS

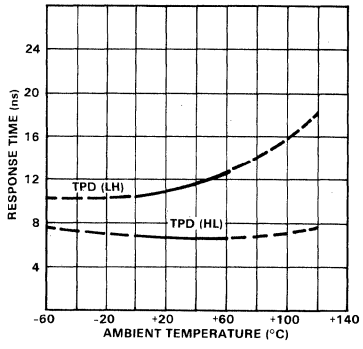
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



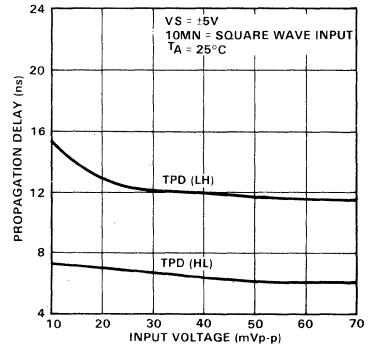
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



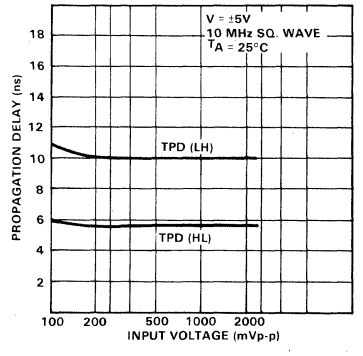
RESPONSE TIME vs TEMPERATURE



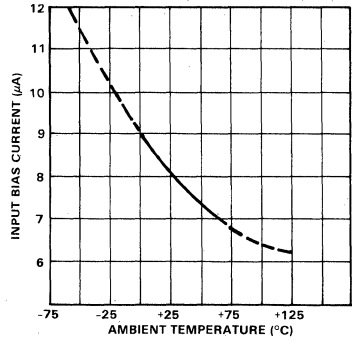
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



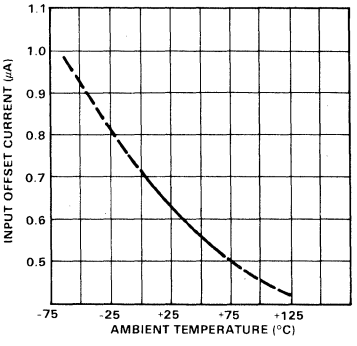
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE



NE/SE527-F,K,N

DESCRIPTION

The SE/NE527 is a high speed analog voltage comparator which, in the first time mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed T²L gates with a precision linear amplifier on a single monolithic chip. The SE/NE527 is similar in design to the Signetics SE/NE529 voltage comparator except that it incorporates a "Emitter Follower" input stage for extremely low input currents. This opens the door to a whole new range of applications for analog voltage comparators.

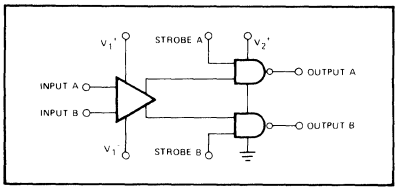
FEATURES

- **15ns propagation delay**
- **Complementary output gates**
- **TTL or ECL compatible outputs**
- **Wide common mode and differential voltage range**
- **Mil std 883A,B,C available**

APPLICATIONS

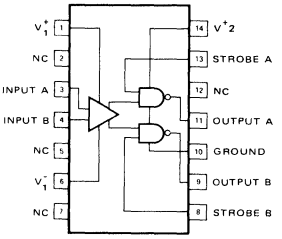
- **A/D conversion**
- **ECL to TTL interface**
- **TTL to ECL interface**
- **Memory sensing**
- **Optical data coupling**

BLOCK DIAGRAM

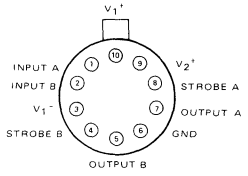


PIN CONFIGURATIONS

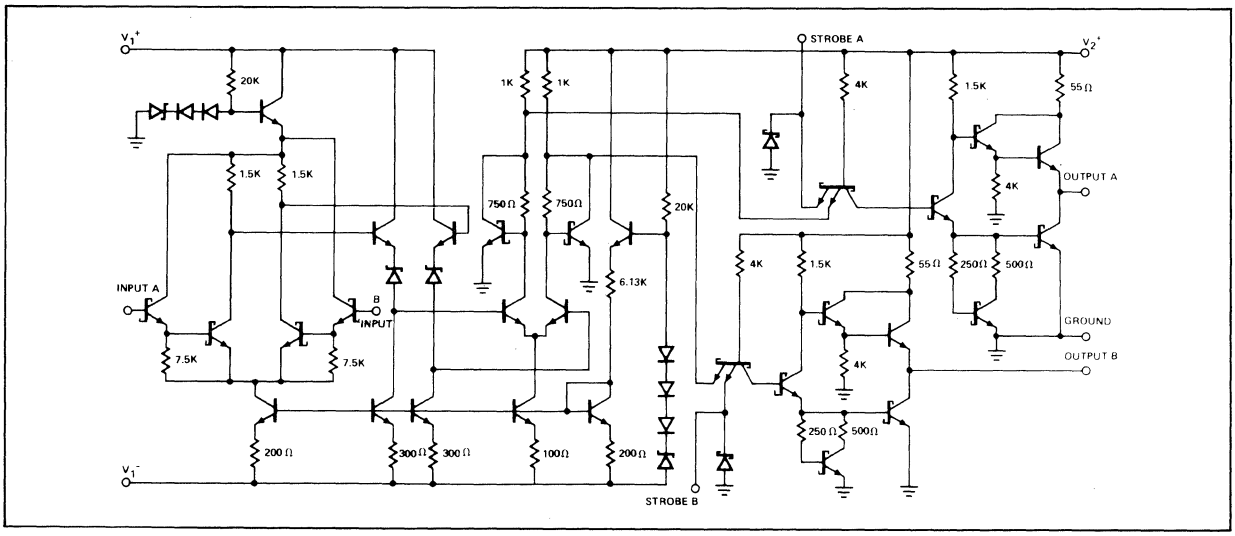
F,N PACKAGE



K PACKAGE



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V1+)	+15	V
Negative supply voltage (V1-)	-15	V
Gate supply voltage (V2+)	+7	V
Output voltage	+15	V
Differential input voltage	±5	V
Input common mode voltage	±6	V
Power dissipation	600	mW
Operating temperature range		
NE527	0 to +70	°C
SE527	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

DC ELECTRICAL CHARACTERISTICS $V_{1^+} = 10V$, $V_{1^-} = -10V$, $V_{2^+} = +5.0V$, $V_{IN} = 0V$*

PARAMETER	TEST CONDITIONS	SE527			NE527			UNIT
		Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS								
Input offset voltage @ 25°C				4			6	mV
Over temperature range				6			10	mV
Input bias current @ 25°C	$V_{1^+} = 10V$, $V_{1^-} = -10V$			2			2	μA
Over temperature range	$V_{IN} = 0V$			4			4	μA
Input offset current @ 25°C	$V_{1^+} = 10V$, $V_{1^-} = -10V$			0.5			0.75	μA
Over temperature range	$V_{IN} = 0V$			1			1	μA
Input impedance	$T_A = 25°C$, f = 1kHz		500			500		kΩ
GATE CHARACTERISTICS								
Output voltage								
"1" State	$V_{2^+} = 4.75V$, $I_{SOURCE} = -1mA$	2.5	3.3		2.7	3.3		V
"0" State	$V_{2^+} = 4.75V$, $I_{SINK} = 10mA$			0.5			0.5	V
Strobe inputs								
"0" Input current	$V_{2^+} = 5.25V$, $V_{STROBE} = 0.5V$			-2			-2	mA
"1" Input current @ 25°C	$V_{2^+} = 5.25V$, $V_{STROBE} = 2.7V$			50			100	μA
Over temperature range	$V_{2^+} = 5.25V$, $V_{STROBE} = 2.7V$			200			200	μA
"0" Input voltage	$V_{2^+} = 4.75V$			0.8			0.8	V
"1" Input voltage	$V_{2^+} = 4.75V$	2.0			2.0			V
Short circuit								
Output current	$V_{2^+} = 5.25V$, $V_{OUT} = 0V$	-18		-70	-18		-70	mA
POWER SUPPLY REQUIREMENTS								
Supply voltage								
V_{1^+}		5		10	5		10	V
V_{1^-}		-6		-10	-6		-10	V
V_{2^+}		4.5	5	5.5	4.75	5	5.25	V
Supply current	$V_{1^+} = 10V$, $V_{1^-} = -10V$							
	$V_{2^+} = 5.25V$							
I_{1^+}	Over temp.			5			5	mA
I_{1^-}	Over temp.			10			10	mA
I_{2^+}	Over temp.			20			20	mA

*NOTE

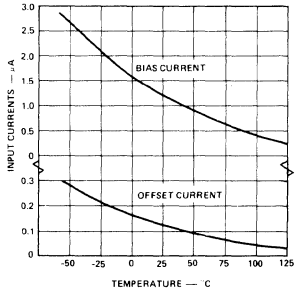
Parameters are guaranteed over the temperature range unless otherwise specified.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

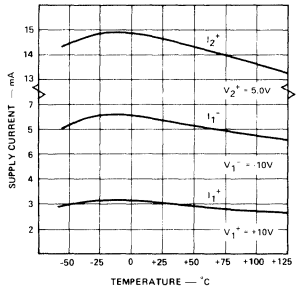
PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Transient response propagation delay time	$V_{IN} = \pm 100mV$ step				
t_{PLH}	$T_A = 25°C$		16	26	ns
t_{PHL}			14	24	ns
Delay between output A and B			2	5	ns
Strobe delay time					
t_{on} Turn-on time			6		ns
t_{off} Turn-off time			6		ns

TYPICAL PERFORMANCE CHARACTERISTICS

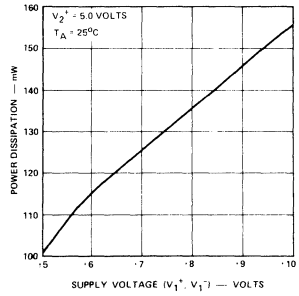
INPUT CURRENTS vs TEMPERATURE



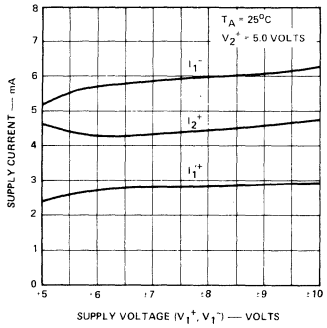
SUPPLY CURRENT vs TEMPERATURE



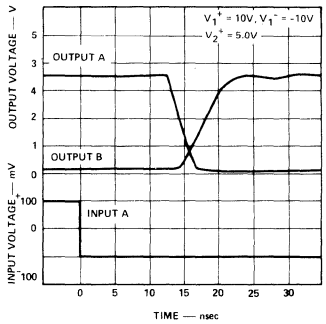
POWER DISSIPATION vs SUPPLY VOLTAGE



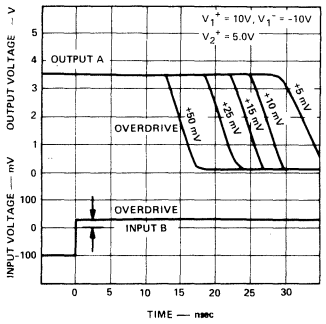
SUPPLY CURRENT vs SUPPLY VOLTAGE



OUTPUT PROPAGATION DELAYS



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



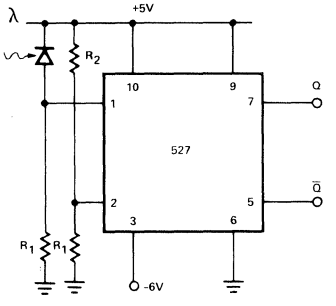
APPLICATIONS

One of the main features of the device is that supply voltages (V1+, V1−) need not be balanced, as indicated in the following diagrams. For proper operation, however, negative supply (V1−) should always be at least six volts more negative than the ground terminal (pin 6). Input Common Mode range should be limited to values of two volts less than the supply voltages (V1+ and V1−) up to a maximum of ±6 volts as supply voltages are increased.

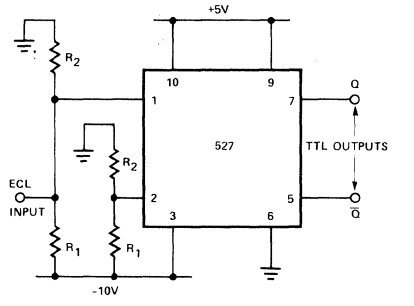
It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

TYPICAL APPLICATIONS

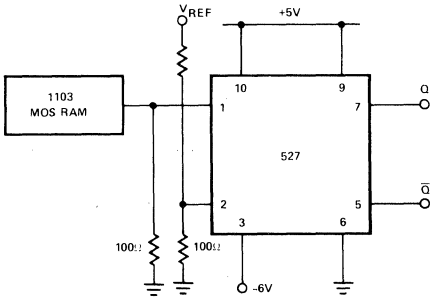
PHOTODIODE DETECTOR



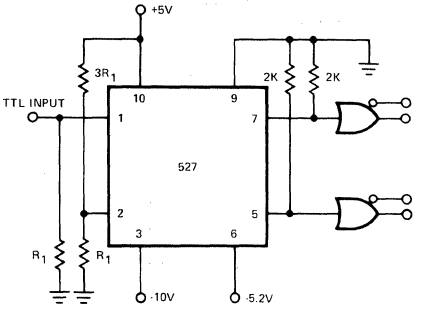
ECL TO TTL INTERFACE



MOS MEMORY SENSE AMP



TTL TO ECL INTERFACE



NE/SE529-F,K,N

DESCRIPTION

The SE/NE529 is a high speed analog voltage comparator which, for the first time mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed T²L gates with a precision linear amplifier on a single monolithic chip.

FEATURES

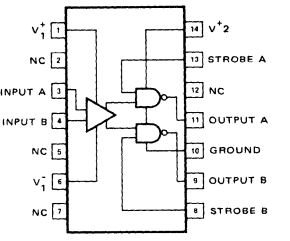
- **10ns propagation delay**
- **Complementary output gates**
- **TTL or ECL compatible outputs**
- **Wide common mode and differential voltage range**

APPLICATIONS

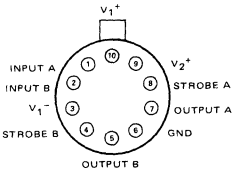
- **A/D conversion**
- **ECL to TTL interface**
- **TTL to ECL interface**
- **Memory sensing**
- **Optical data coupling**
- **Mil std 883A,B,C available**

PIN CONFIGURATION

F,N PACKAGE



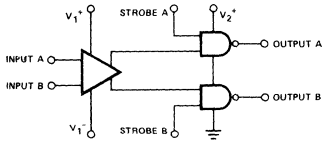
K PACKAGE



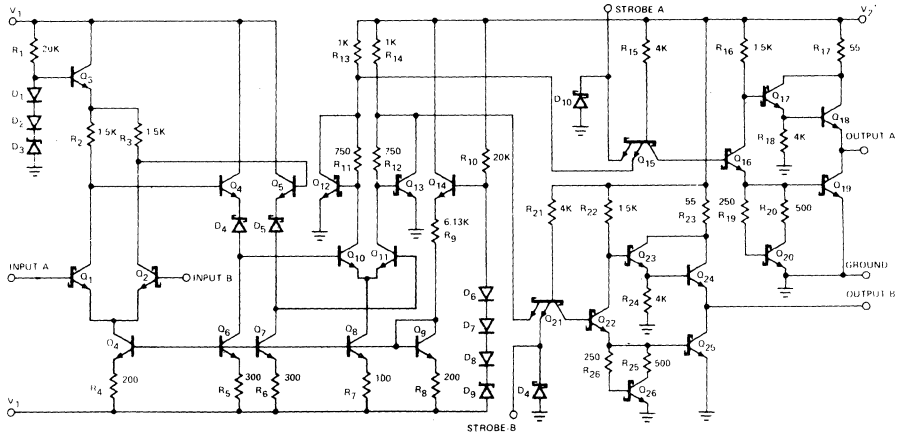
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V1+)	+15	V
Negative supply voltage (V1-)	-15	V
Gate supply voltage (V2+)	+7	V
Output voltage	+15	V
Differential input voltage	±5	V
Input common mode voltage	±6	V
Power dissipation	600	mW
Operating temperature range		
NE529	0 to +70	°C
SE529	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature		
(soldering, 60 sec)	+300	°C

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS

$V_1+ = +10V$, $V_2+ = +5.0V$, $V_1- = -10V$, $V_{IN} = 0V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE529			NE529			UNIT
		Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS								
Input offset voltage @25°C				4			6	mV
Over temperature range				6			10	mV
Input bias current @25°C	$V_1+ = 10V$, $V_1- = -10V$		5	12		5	20	μA
Over temperature range	$V_{IN} = 0V$			36			50	μA
Input offset current @25°C	$V_1+ = 10V$, $V_1- = -10V$		2	3		2	5	μA
Over temperature range	$V_{IN} = 0V$			9			15	μA
Input impedance	$T_A = 25°C$, f = 1kHz		10			10		kΩ
GATE CHARACTERISTICS								
Output voltage								
"1" state	$V_2+ = 4.75V$, $I_{source} = -1mA$	2.5	3.3		2.7	3.3		V
"0" state	$V_2+ = 4.75V$, $I_{sink} = 10mA$			0.5			0.5	V
Strobe inputs								
"0" input current	$V_2+ = 5.25V$, $V_{strobe} = 0.5V$			-2			-2	mA
"1" input current @25°C	$V_2+ = 5.25V$, $V_{strobe} = 2.7V$			50			100	μA
Over temperature range	$V_2+ = 5.25V$, $V_{strobe} = 2.7V$			200			200	μA
"0" input voltage	$V_2+ = 4.75V$			0.8			0.8	V
"1" input voltage	$V_2+ = 4.75V$	2.0			2.0			V
Short circuit								
Output current	$V_2+ = 5.25V$, $V_{OUT} = 0V$	-18		-70	-18		-70	mA
POWER SUPPLY REQUIREMENTS								
Supply voltage								
V_1+		5		10	5		10	V
V_1-		-6		-10	-6		-10	V
V_2+		4.5	5	5.5	4.75	5	5.25	V
Supply current	$V_1+ = 10V$, $V_1- = -10V$							
	$V_2+ = 5.25V$							
I_1+	Over temp.			5			5	mA
I_1-	Over temp.			10			10	mA
I_2+	Over temp.			20			20	mA

AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$

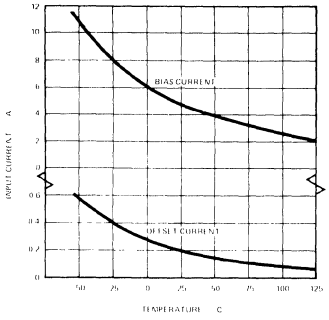
PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Transient response	$V_{IN} = \pm 100mV$ step				
Propagation delay time					
t_{PLH}			12	22	ns
t_{PHL}			10	20	ns
Delay between output A and B			2	5	ns
Strobe delay time					
t_{ON} turn-on time			6		ns
t_{OFF} turn-off time			6		ns

Parameters are guaranteed over the temperature range unless otherwise specified.

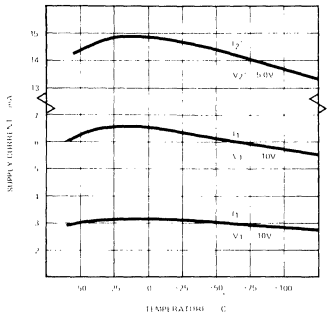
NE/SE529-F,K,N

TYPICAL PERFORMANCE CHARACTERISTICS

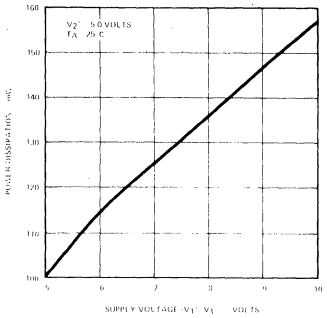
INPUT CURRENTS vs TEMPERATURE



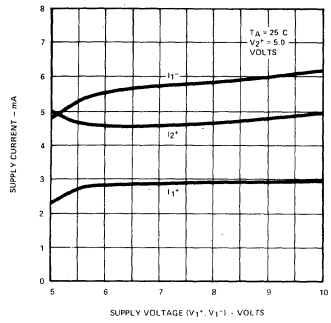
SUPPLY CURRENT vs TEMPERATURE



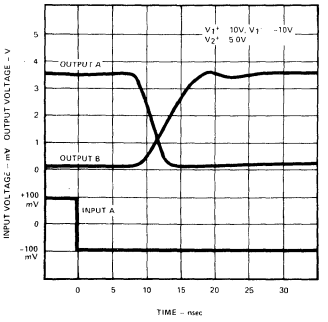
POWER DISSIPATION vs SUPPLY VOLTAGE



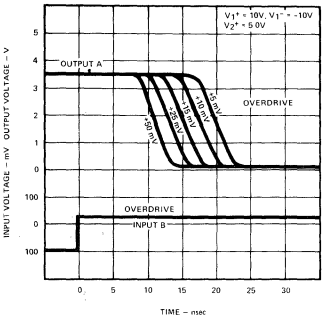
SUPPLY CURRENT vs SUPPLY VOLTAGE



OUTPUT PROPAGATION DELAYS



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



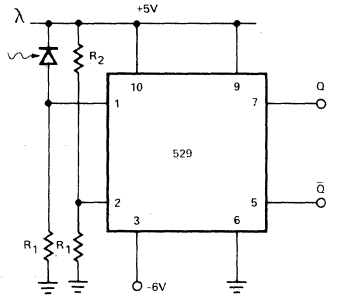
APPLICATIONS

One of the main features of the device is that supply voltages (V1+, V1−) need not be balanced, as indicated in the following diagrams. For proper operation, however, negative supply (V1−) should always be at least five volts more negative than the ground terminal (pin 6). Input Common Mode range should be limited to values of two volts less than the supply voltages (V1+ and V1−) up to a maximum of ±6 volts as supply voltages are increased.

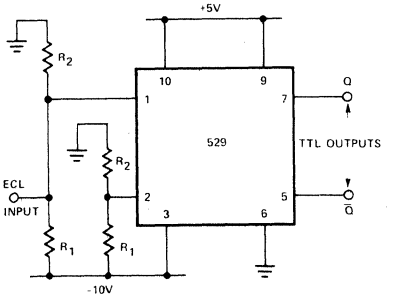
It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

TYPICAL APPLICATIONS

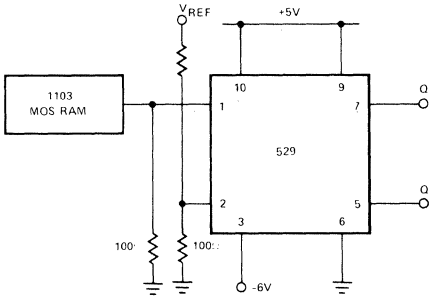
PHOTODIODE DETECTOR



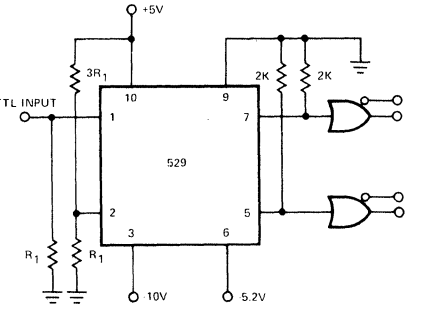
ECL TO TTL INTERFACE



MOS MEMORY SENSE AMP



TTL TO ECL INTERFACE



μA710-F/N/N-14/T

DESCRIPTION

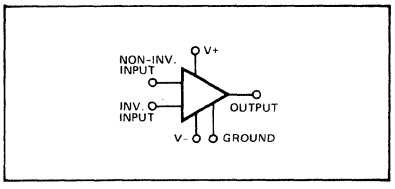
The μA710 is a High Speed Differential Voltage Comparator featuring low offset voltage, high sensitivity and a wide input voltage range. It is ideally suited for use as a pulse height discriminator, an analog comparator or a digital line receiver. The output structure of the μA710 is compatible with DTL, TTL and Utilogic integrated circuits.

The μA710 is specified for operation over the MIL temperature range of -55°C to +125°C. The μA710C is specified for operation over the commercial/industrial temperature range of 0°C to +75°C.

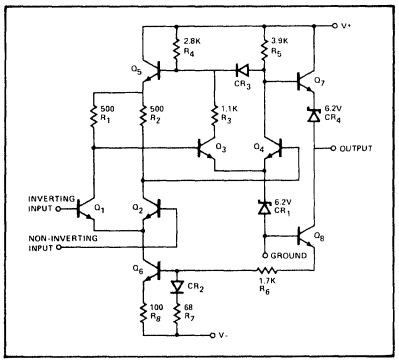
FEATURES

- **Fast response—40ns**
- **High sensitivity—1.7V/mV**
- **Low offset voltage temperature coefficient—3.5μV/°C**
- **High input voltage range—±5.0V**
- **Mil std 883A,B,C available**

BLOCK DIAGRAM

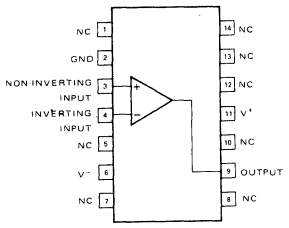


EQUIVALENT SCHEMATIC

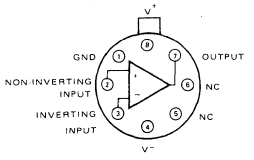


PIN CONFIGURATIONS

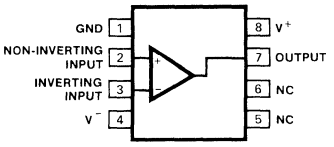
F,N-14 PACKAGE



T PACKAGE



N PACKAGE



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage	+14.0	V
Negative supply voltage	-7.0	V
Peak output current	10	mA
Differential input voltage	±5.0	V
Input voltage	±7.0	V
Internal power dissipation[4]		
TO-99	300	mW
TO-91	200	mW
Operating temperature range		
μA710	-55 to +125	°C
μA710C	0 to +75	°C
Storage temperature rage	-65 to +150	°C
Lead temperature (soldering, 60sec)	300	°C

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, V+ = 12V, V- = 6.0V unless otherwise specified.

PARAMETER	TEST CONDITIONS	μA710			μA710C			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage[3]	$R_S \leq 200\Omega$		0.6	2.0		1.6	5.0	mV
Input offset current[3] Input bias current			0.75 13	3.0 20		1.8 16	5.0 25	μA μA
Voltage gain		1250	1700		1000	1500		
Output resistance Output sink current	$\Delta V_{IN} \geq 5mV$, $V_{OUT} = 0$	2.0	200 2.5		1.6	200		Ω mA
Response time[2] μA710 μA710C	The following specifications apply for: $-55°C \leq T_A \leq +125°C$ $0° \leq T_A \leq +75°C$		40			40		ns
Input offset voltage[3]	$R_S \leq 200\Omega$			3.0			6.5	
Average temperature coefficient of input offset voltage	$R_S = 50\Omega$, $T_A = +25°C$ to $+125°C$ $R_S = 50\Omega$, $T_A = +25°C$ to $-55°C$ $R_S = 50\Omega$, $T_A = 0°C$ to $+75°C$		3.5 2.7	10 10		 5	 20	μV/°C
Input offset current[3]	$T_A = +125°C$ $T_A = -55°C$ $T_A = 0°C$ to $+75°C$		0.25 1.8	3.0 7.0			 7.5	μA μA μA
Average temperature coefficient	$T_A = +25°C$ to $+125°C$		5.0	25				nA/°C
Input offset current	$T_A = +25°C$ to $-55°C$ $T_A = +25°C$ to $+75°C$ $T_A = +25°C$ to $0°C$		15	75		 15 24	 50 100	nA/°C μA/°C μA/°C
Input bias current	$T_A = -55°C$ $T_A = 0°C$		27	45		 25	 40	μA μA
Input common mode voltage range	V- = -7.0V	±5.0			±5.0			V
Common mode rejection ratio Differential input voltage range Voltage gain	$R_S \leq 200\Omega$	80 ±5.0 1000	100		70 ±5.0 800	98		dB
Positive output level Negative output level	$\Delta V_{IN} \geq 5mV$, $0 \leq I_{OUT} \leq 5.0mA$ $\Delta V_{IN} \geq 5mV$	2.5 -1.0	3.2 -0.5	4.0 0	2.5 -1.0	3.2 -0.5	4.0 0	V V
Output sink current	$T_A = +125°C$, $\Delta V_{IN} \geq 5mA$, $V_{OUT} = 0$ $T_A = -55°C$, $\Delta V_{IN} \geq 5mV$, $V_{OUT} = 0$ $T_A = 0°C$ to $+75°C$, $\Delta V_{IN} \geq 5mV$, $V_{OUT} = 0$	0.5 1.0	1.7 2.3		 0.5			mA mA mA
Positive supply current Negative supply current	$V_{OUT} \leq 0$		5.2 4.6	9.0 7.0		5.2 4.6	9.0 7.0	mA mA
Power consumption			90	150		90	150	mW

NOTES

1. All voltages are referenced to ground.
2. The response time specified is measured with a 100mV input step, and a 5mV overdrive.
3. Input Offset Voltage and Input Offset Current are specified for output voltage levels of:

μA710	μA710C
1.8V at -55°C	1.5V at 0°C
1.4V at +25°C	1.4V at +25°C
1.0V at +125°C	1.2V at +75°C

4. Rating applies for temperatures up to:
   μA710 — +125°C
   μA710C — +75°C

μA711-F,K,N

DESCRIPTION

The μA711 High Speed Dual Voltage Comparator features low offset voltage, high sensitivity and a wide input voltage range. It is ideal for use as a bi-directional limit detector in automatic test equipment.

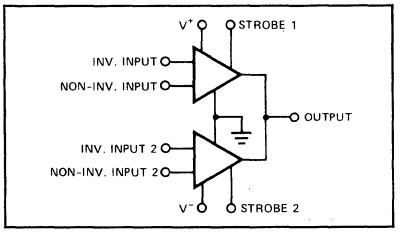
Due to fast response and strobe control capabilities the μA711 performs well as a sense amplifier in core memory systems.

The μA711 is specified over the military temperature range of -55 °C to +125 °C. The μA711C is specified over the commercial/ industrial temperature range of 0 °C to +75 °C.

FEATURES

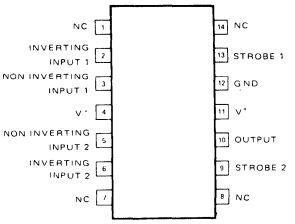
- **Fast response—40ns**
- **High sensitivity—1.5V/mV**
- **Low offset voltage temperature coefficient—5μV/ °C**
- **High input voltage range—±5.0V**
- **Mil std 883A,B,C available**

LOGIC DIAGRAM

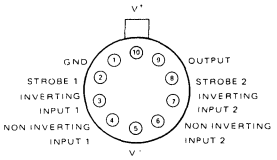


PIN CONFIGURATION

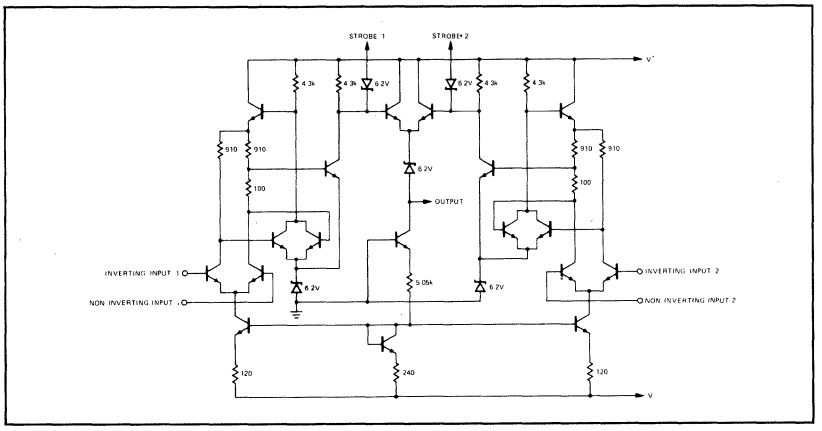
F,N PACKAGE



K PACKAGE



CIRCUIT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage	+14.0	V
Negative supply voltage	-7.0	V
Peak output current	50	mA
Differential input voltage	±5.0	V
Internal power dissipation[4]	300	mW
Operating temperature range		
μA711	-55 to +125	°C
μA711C	0 to +75	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	300	°C

5

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V+ = 12.0V$, $V- = -6.0V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	μA711			μA711C			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage	$V_{OUT} = +1.4V$, $R_S \leq 200\Omega$, $V_{CM} = 0$ $V_{OUT} = +1.4V$, $R_S \leq 200\Omega$		1.0 1.0	3.5 5.0		1.0 1.0	5.0 7.5	mV mV
Input offset current Input bias current	$V_{OUT} = +1.4V$		0.5 25	10.0 75		0.5 25	15.0 100	μA μA
Voltage gain		750	1500		700	1500		
Response time[2] Strobe release time			40 12			40 12		ns ns
Input common mode voltage range Differential input voltage range	$V- = -7.0V$	±5.0 ±5.0			±5.0 ±5.0			V V
Output resistance			200			200		Ω
Positive output level Loaded positive output level	$V_{IN} \geq 10mV$ $V_{IN} \geq 10mV$, $I_O = 5mA$	 2.5	4.5 3.5	5.0	 2.5	4.5 3.5	5.0	V
Negative output level Strobed output level	$V_{IN} \geq 10mV$ $V_{STROBE} < 0.3V$	-1.0 -1.0	-0.5	0 0	-1.0 -1.0	-0.5	0 0	V V
Output sink current	$V_{IN} \geq 10mV$, $V_{OUT} \geq 0$	0.5	0.8		0.5	0.8		mA
Strobe current	$V_{STROBE} = 100mV$		1.2	2.5		1.2	2.5	mA
Positive supply current Negative supply current	$V_{OUT} \leq 0$		8.6 3.9			8.6 3.9		mA mA
Power consumption			130	200		130	230	mW
The following specifications apply over the temperature range of:	$-55°C \leq T_A \leq +125°C$ for the μA711 $0°C \leq T_A \leq +75°C$ for the μA711C							
Input offset voltage[3]	$R_S \leq 200\Omega$, $V_{CM} = 0$ $R_S \leq 200\Omega$			4.5 6.0			6.0 10.0	mV mV
Input offset current[3] Input bias current				20 150			25 150	μA μA
Temperature coefficient of input			5.0			5.0		μV/°C
Offset voltage								
Voltage gain		500			500			

NOTES

1. All voltages are referenced to pin 1.
2. The response time specified is for a 100mV input step, with a 5mV overdrive.
3. The input offset voltage and input offset current are specified for a logic threshold voltage of:

μA711	μA711C
1.8V at -55°C	1.5V at 0°C
1.4V at +25°C	1.4V at +25°C
1.0V at +125°C	1.2V at +75°C

4. Rating applies for temperatures up to: μA711 — +125°C; μA711C — +75°C

SECTION 6
MEMORY INTERFACE

55/75325-F,N

DESCRIPTION

The 55325 and 75325 are monolithic integrated circuit memory drivers with logic inputs and are designed for use with magnetic memories.

The devices contain two 600-milliampere source-switch pairs and two 600-milliampere sink-switch pairs. Source selection is determined by one of two logic inputs, and source turn-on is determined by the source strobe. Likewise, sink selection is determined by one of two logic inputs, and sink turn-on is determined by the sink strobe. This arrangement allows selection of one of the four switches and its subsequent turn-on with minimum time skew of the output current rise.

The 55325 is characterized for operation over the full military temperature range of -55°C to 125°C; the 75325 is characterized for operation from 0°C to 70°C.

When R_{int} and node R are connected together, the amount of base drive available for the source-1 or source-2 output transistor is set internally by a 575-ohm resistor. This method provides adequate base drive for source currents up to 375mA with a V_{CC2} voltage of 15 volts or 600mA with a V_{CC2} voltage of 24 volts.

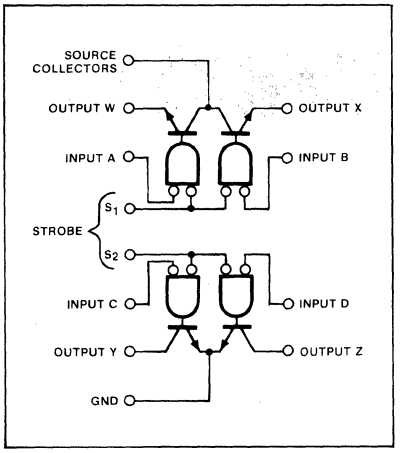
When source currents greater than 375mA are required, it is recommended that a resistor of the appropriate value be connected between V_{CC2} and node R and R_{int} must remain open. By using this method the source base current may usually be regulated within ±5%. An advantage of this method of setting the base drive is that the power dissipated by this resistor is external to the package and allows the integrated circuit to operate at higher source currents for a given junction temperature.

Each sink-output collector has an internal pull-up resistor in parallel with a clamping diode connected to V_{CC2}. This arrangement provides protection from voltage surges associated with switching inductive loads.

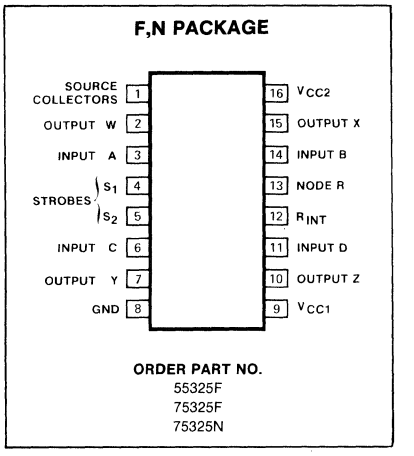
FEATURES

- **600mA output capability**
- **Fast switching times**
- **Output short-circuit protection**
- **Dual sink and dual source outputs**
- **Minimum time skew between address and output current rise**
- **24 volt output capability**
- **Source base drive externally adjustable**
- **TTL or DTL compatibility**
- **Input clamping diodes**

BLOCK DIAGRAM



PIN CONFIGURATION



ORDER PART NO.
55325F
75325F
75325N

TRUTH TABLE

ADDRESS INPUTS				STROBE INPUTS		OUTPUTS			
SOURCE		SINK		SOURCE	SINK	SOURCE		SINK	
A	B	C	D	S1	S2	W	X	Y	Z
L	H	X	X	L	H	ON	OFF	OFF	OFF
H	L	X	X	L	H	OFF	ON	OFF	OFF
X	X	L	H	H	L	OFF	OFF	ON	OFF
X	X	H	L	H	L	OFF	OFF	OFF	ON
X	X	X	X	H	H	OFF	OFF	OFF	OFF
H	H	H	H	X	X	OFF	OFF	OFF	OFF

NOTE

Not more than one output is to be on at any one time.

H = high level, L = low level, X = irrelevant

ABSOLUTE MAXIMUM RATINGS

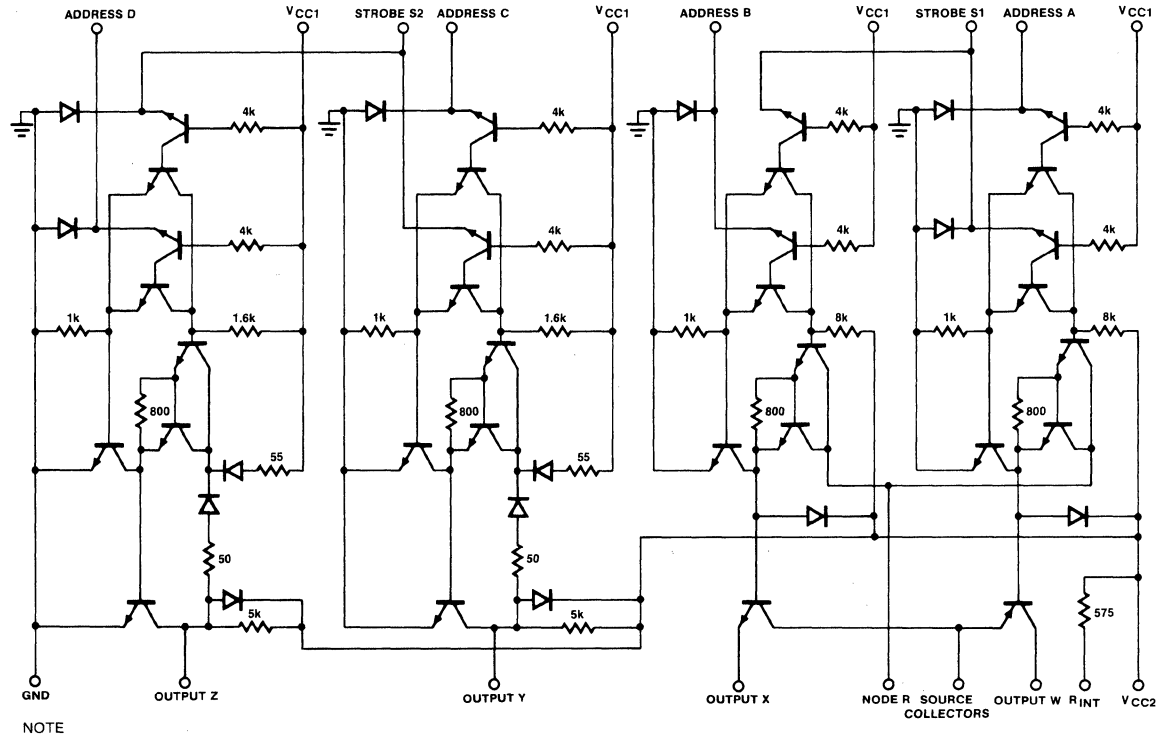
PARAMETER	RATING		UNIT
	55325	75325	
Supply voltage V_{CC1}[1]	7	7	V
Suppy voltage V_{CC2}[2]	25	25	V
Input voltage (any address or strobe input)	5.5	5.5	V
Continuous total dissipation at (or below) 100°C case temperature[2]	1	1	W
Operating free-air temperature range	-55 to +125	0 to +70	°C
Storage temperature range	-65 to +150	-65 to +150	°C
Lead temperature 1/16 inch from case for 60 seconds F package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds N package	260	260	°C

NOTES

1. Voltage values are with respect to network ground terminal
2. For operation above 100°C case temperature, refer to Dissipation Derating Curve, Figure 8. For dissipation ratings in free-air, see Figure 9.

55/75325-F,N

EQUIVALENT SCHEMATIC



NOTE

All resistors values are typical and in ohms.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

PARAMETER			TEST CONDITIONS		55325			75325			UNIT
					Min	Typ	Max	Min	Typ	Max	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage		$V_{CC1} = 4.5V$, $V_{CC2} = 24V$, $I_I = -10mA$, $T_A = 25°C$			-1.3	-1.7		-1.3	-1.7	V
$I_{(off)}$	Source-collectors terminal off-state current		$V_{CC1} = 4.5V$, $V_{CC2} = 24V$	Full range[3] $T_A = 25°C$		 3	500 150		 3	200 200	μA
V_{OH}	High-level sink output voltage		$V_{CC1} = 4.5V$, $V_{CC2} = 24V$, $I_O = 0$		19	23		19	23		V
$V_{(sat)}$	Saturation voltage[2]	Source outputs	$V_{CC1} = 4.5V$, $V_{CC2} = 15V$, $R_L = 24\Omega$, $I_{(source)} \approx -600mA$[4]	Full range[3] $T_A = 25°C$		 0.43	0.9 0.7		 0.43	0.9 0.75	V
		Sink outputs	$V_{CC1} = 4.5V$, $V_{CC2} = 15V$, $R_L = 24\Omega$, $I_{(sink)} \approx 600mA$[4]	Full range[3] $T_A = 25°C$		 0.43	0.9 0.7		 0.43	0.9 0.75	
I_I	Input current at max input voltage	Address inputs Strobe inputs	$V_{CC1} = 5.5V$, $V_{CC2} = 24V$, $V_I = 5.5V$				1 2			1 2	mA
I_{IH}	High-level input current	Address inputs Strobe inputs	$V_{CC1} = 5.5V$, $V_{CC2} = 24V$, $V_I = 2.4V$			3 6	40 80		3 6	40 80	μA
I_{IL}	Low-level input current	Address inputs Strobe inputs	$V_{CC1} = 5.5V$, $V_{CC2} = 24V$, $V_I = 0.4V$			-1 -2	-1.6 -3.2		-1 -2	-1.6 -3.2	mA
$I_{CC(off)}$	Supply current, all sources & sinks off	From V_{CC1} From V_{CC2}	$V_{CC1} = 5.5V$, $V_{CC2} = 24V$, $T_A = 25°C$			14 7.5	22 20		14 7.5	22 20	mA
I_{CC1}	Supply current from V_{CC1}, either sink on		$V_{CC1} = 5.5V$, $V_{CC2} = 24V$, $I_{(sink)} = 50mA$, $T_A = 25°C$			55	70		55	70	mA
I_{CC2}	Supply current from V_{CC2}, either source on		$V_{CC1} = 5.5V$, $V_{CC2} = 24V$, $I_{(source)} = -50mA$, $T_A = 25°C$[4]			32	50		32	50	mA

NOTES

1. Over rated operating free-air temperature range, unless otherwise specified.
2. Not more than one output is to be on at any one time.
3. Full range for 55325 is -55°C to +125°C and for 75325 is 0°C to +70°C.
4. These parameters must be measured using pulse techniques, $t_w = 200\mu s$, duty cycle ≤ 2%.

AC ELECTRICAL CHARACTERISTICS $V_{CC1} = 5V$, $T_A = 25°C$ unless otherwise specified.

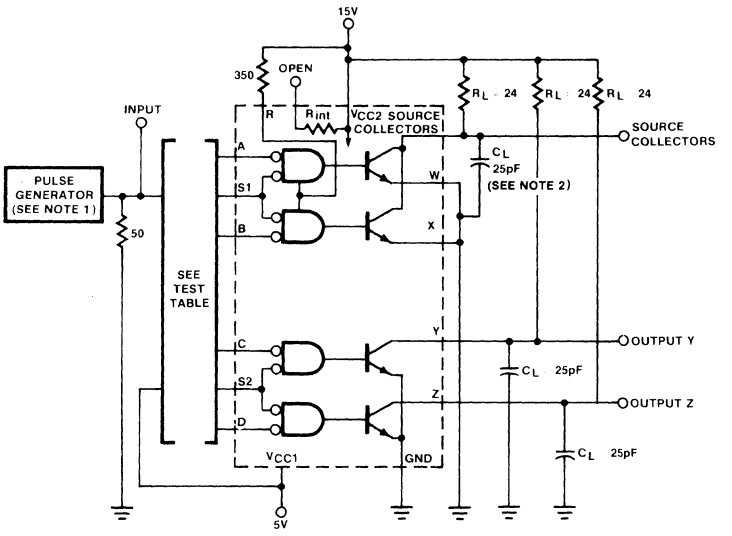
PARAMETER*	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
t_{PLH} t_{PHL}	Source collectors	1	$V_{CC2} = 15V$, $R_L = 24\Omega$ $C_L = 25pF$		25 25	50 50	ns
t_{TLH} t_{THL}	Source outputs	2	$V_{CC2} = 20V$, $R_L = 1k\Omega$ $C_L = 25pF$		55 7		ns
t_{PLH} t_{PHL}	Sink outputs	1	$V_{CC2} = 15V$, $R_L = 24\Omega$ $C_L = 25pF$		20 20	45 45	ns
t_{TLH} t_{THL}	Sink outputs	2	$V_{CC2} = 15V$, $R_L = 24\Omega$ $C_L = 25pF$		7 9	15 20	ns
t_S	Sink outputs	1	$V_{CC2} = 15V$, $R_L = 24\Omega$, $C_L = 25pF$		15	30	ns

NOTE

*t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{TLH} = transition time, low-to-high-level output
t_{THL} = transition time, high-to-low-level output
t_S = storage time

TYPICAL PERFORMANCE CHARACTERISTICS

TEST CIRCUIT



NOTES

All resistors values are typical and in ohms.

1. The pulse generator has the following characteristics: $Z_{OUT} = 50\Omega$, duty cycle $\leq 1\%$.
2. C_L includes probe and jig capacitance.

TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5V
t_{PLH} and t_{PHL}	Source collectors	A and S1	B,C,D and S2
		B and S1	A,C,D and S2
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, and t_S	Sink output Y	C and S2	A,B,D and S1
	Sink output Z	D and S2	A,B,C and S1

VOLTAGE WAVEFORMS

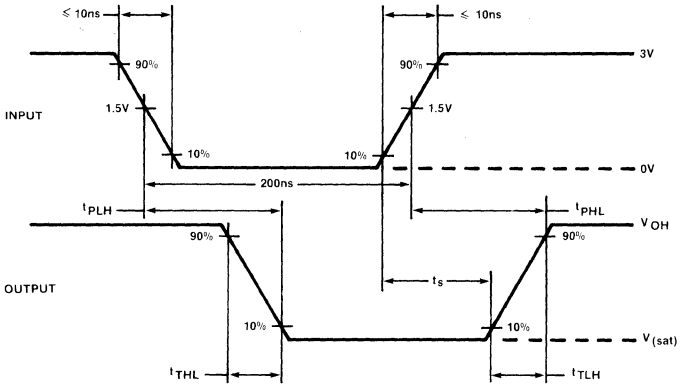
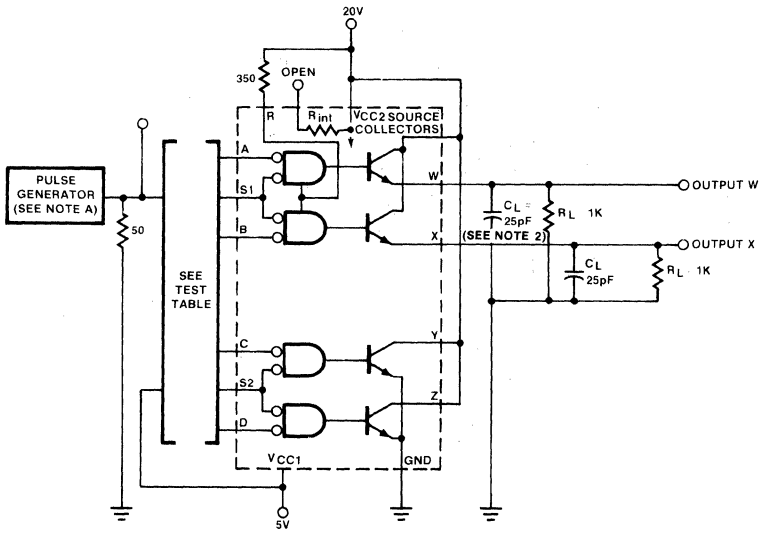


FIGURE 1 SWITCHING TIMES

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



NOTES

All resistors values are typical and in ohms.

1. The pulse generator has the following characteristics. $Z_{OUT} = 50\Omega$, duty cycle $\leq 1\%$.
2. C_L includes probe and jig capacitance.

TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5V
t_{TLH} and t_{THL}	Source output W	A and S1	B,C,D and S2
	Source output X	B and S1	A,B,D and S2

VOLTAGE WAVEFORMS

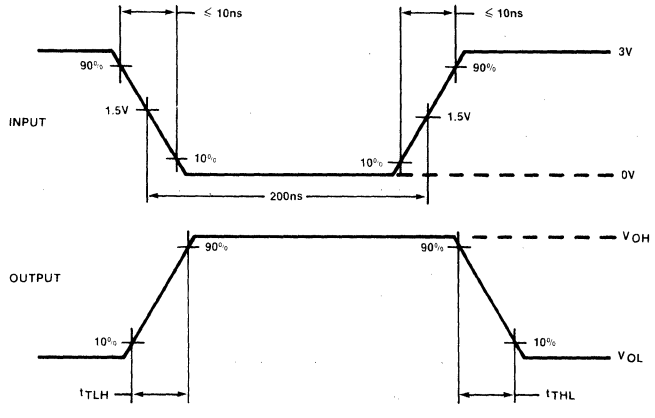


FIGURE 2 TRANSITION TIMES OF SOURCE OUTPUTS

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

OFF-STATE CURRENT INTO SOURCE COLLECTORS vs FREE-AIR TEMPERATURE

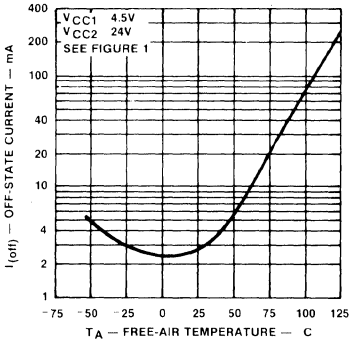


FIGURE 3

HIGH-LEVEL SINK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

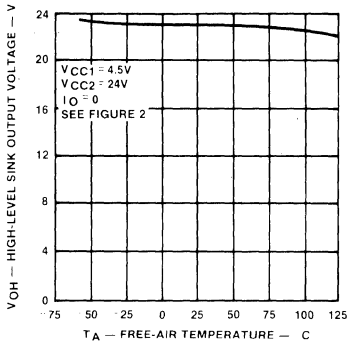


FIGURE 4

SOURCE OR SINK SATURATION VOLTAGE vs SOURCE CURRENT OR SINK CURRENT

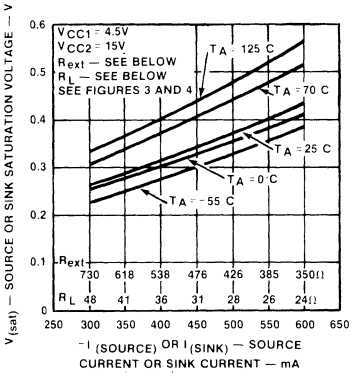


FIGURE 5

SOURCE OR SINK SATURATION VOLTAGE vs FREE-AIR TEMPERATURE

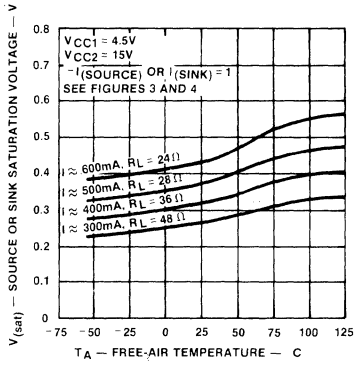


FIGURE 6

SUPPLY CURRENT, ALL SOURCES AND SINKS OFF vs FREE-AIR TEMPERATURES

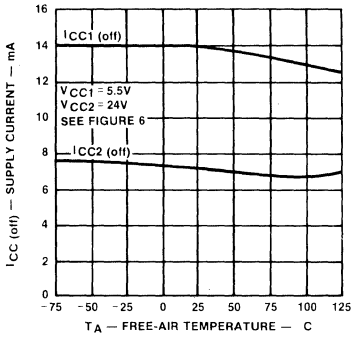


FIGURE 7

CASE TEMPERATURE DISSIPATION DERATING CURVE

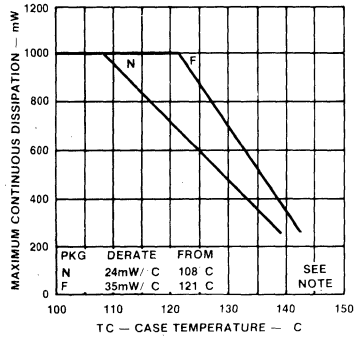


FIGURE 8

FREE-AIR TEMPERATURE DISSIPATION DERATING CURVE

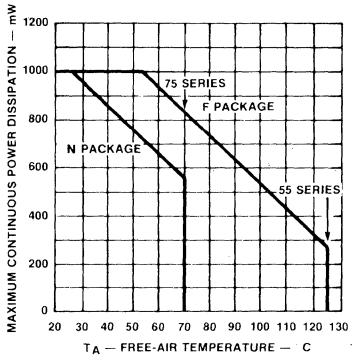


FIGURE 9

NOTE

Rated operating free-air temperature ranges must be observed regardless of heat sinking.

75S207-F,N

DESCRIPTION

The 75S207 is a high speed dual sense amplifier that is functionally equivalent and pin compatible to the SN75207. The improved input sensitivity of ±10mV makes it suitable as a MOS memory sense amplifier which can result in faster memory cycles. The 75S207 features less than 17ns propagation delay without sacrificing input performance characteristics. This is accomplished through the utilization of Schottky technology.

The 75S207 also features STTL compatible output levels with a minimum sink/source capability of 10 Schottky gate loads.

FEATURES

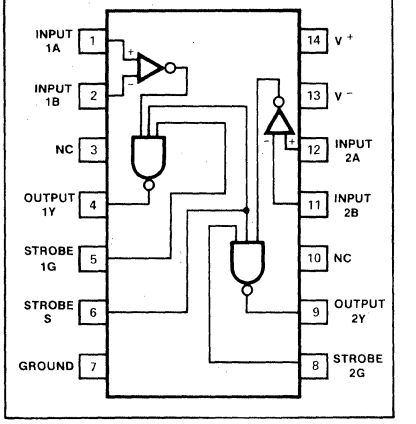
- **Functionally equivalent and pin compatible to SN75207**
- **17ns maximum guaranteed propagation delay**
- **20μA maximum input bias current**
- **STTL compatible strobes and outputs**
- **Large common mode input voltage range**
- **Operates from standard supply voltages**

APPLICATIONS

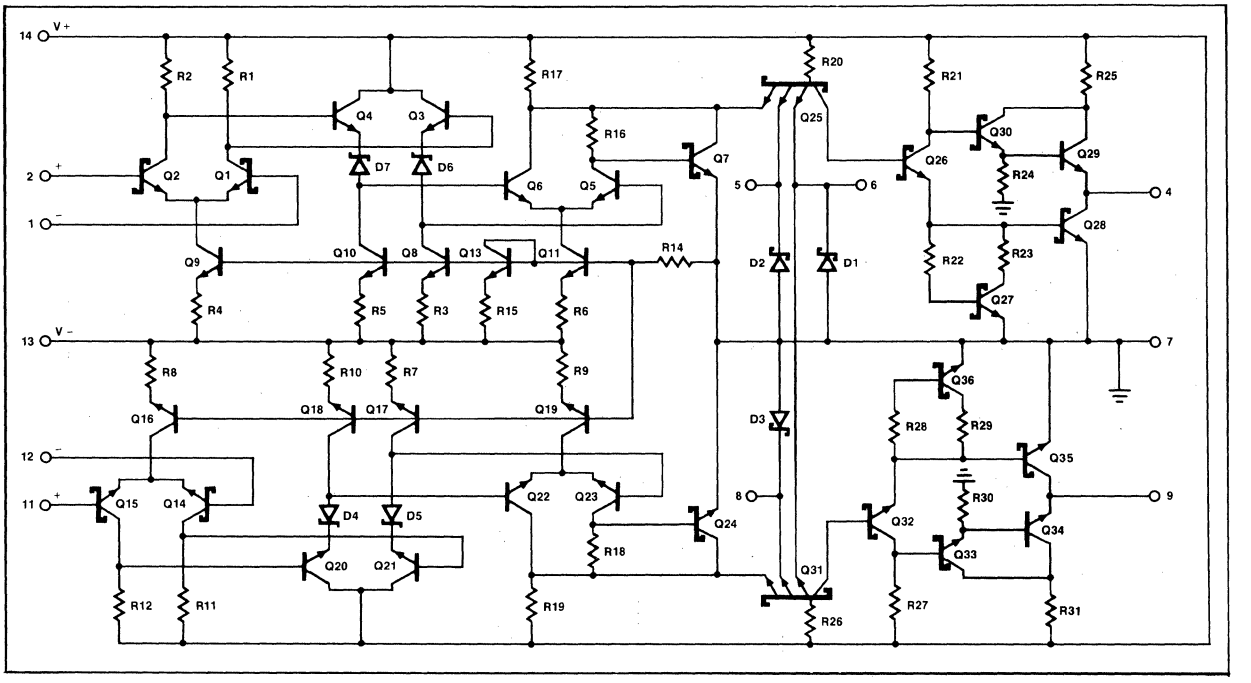
- **MOS memories sense amp**
- **A/D conversion**
- **High speed line receiver**

PIN CONFIGURATION

F,N PACKAGE



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V+)	+7	V
Negative supply voltage (V−)	-7	V
Differential input voltage	±6	V
Common mode input voltage	±5	V
Strobe/gate input voltage	+5.5	V
Power dissipation	600	mW
Operating temperature rnage	0 to 70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 60sec)	+300	°C

DC ELECTRICAL CHARACTERISTICS

$V+ = +5.00$, $V- = -5.00$, $T_A = 0$ to 70°C unless otherwise specified.

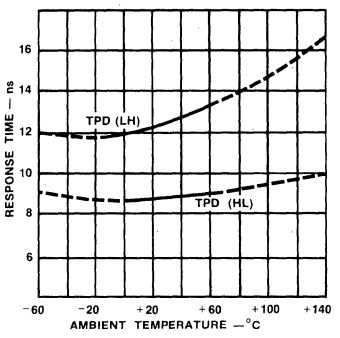
PARAMETER		TEST CONDITIONS	75S207			UNIT
			Min	Typ	Max	
AMPLIFIER INPUT						
	Input offset voltage	V+ = 4.75, V- = -4.75			10	mV
	Input bias current @ 25°C over temp. range	V+ = 5.25, V- = -5.25 V+ = 5.25, V- = -5.25		7.5	20 40	μA μA
	Input offset current @ 25°C over temp. range	V+ = 5.25, V- = -5.25 V+ = 5.25, V- = -5.25		1.0	5 12	μA μA
	Input common mode voltage range Input resistance Input capacitance	V+ = 4.75, V- = -4.75	±3	 4 3	 6	V kΩ pF
	Voltage gain			5		V/mV
SCHOTTKY GATE/OUTPUT						
I_{IH}	High level input current into 1G or 2G strobe	V+ = 5.25, V- = -5.25 V_{IH} = 2.7V V_{IH} = 5.5V			50 1	μA mA
I_{IH}	High level input current into common strobe S	V+ = 5.25, V- = -5.25 V_{IH} = 2.7V V_{IH} = 5.5V			100 2	μA mA
I_{IL}	Low level input current into 1G or 2G	V+ = 5.25, V- = -5.25 V_{IL} = 0.5V			-2.0	mA
I_{IL}	Low level input current into common strobe S	V+ = 5.25, V- = -5.25 V_{IL} = 0.5V			-4.0	mA
V_{OH}	High level output voltage	V+ = 4.75, $V_{I(S)}$ = 2.0V V- = -4.75 I_{LOAD} = -1mA	2.7	3.4		V
V_{OL}	Low level output voltage	V+ = 4.75, V- = -4.75 I_{LOAD} = 20mA $V_{I(S)}$ = 2.0V			0.5	V
POWER SUPPLY REQUIREMENTS						
	Supply voltage V+ V-		 4.75 -4.75	 5.00 -5.00	 5.25 -5.25	 V V
I_{CC}+ I_{CC}-	Supply current	V+ = 5.25V V- = -5.25V T_A = 25°C		20 -11	30 -15	mA mA
I_{OS}	Short circuit output current	V+ = 5.25 V- = -5.25	-40		-100	mA
LARGE SIGNAL SWITCHING SPEED						
$T_pLH(D)$	Low to high propagation delay from amp inputs to output[1]	R_L = 280Ω C_L = 15pF T_A = 25°C		12	17	ns
$T_pHL(D)$	High to low propagation delay from amp inputs to output[1]	R_L = 280Ω C_L = 15pF T_A = 25°C		9	13	ns
$T_pLH(S)$	Low to high propagation delay from strobes input to output[2]	R_L = 280Ω C_L = 15pF T_A = 25°C		4.5	6	ns
$T_pHL(S)$	High to low propagation delay strobe input to output[2]	R_L = 280Ω C_L = 15pF T_A = 25°C		3.0	4.5	ns
	Maximum operating frequency	R_L = 280Ω C_L = 15pF T_A = 25°C	40	55		MHz

NOTES

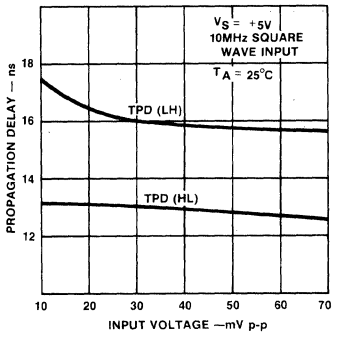
1. Response time measured from 0V point of ±100mV P-P 10MHz square wave to the 1.5 point of the output.
2. Response time measured from 1.5V point of input to 1.5V point of the output.
3. Response time measured from the start of a 100mV input step with 5mV overdrive to the 1.5V point of the output.

TYPICAL PERFORMANCE CHARACTERISTICS

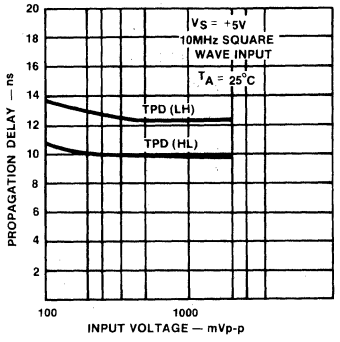
RESPONSE TIME vs TEMPERATURE



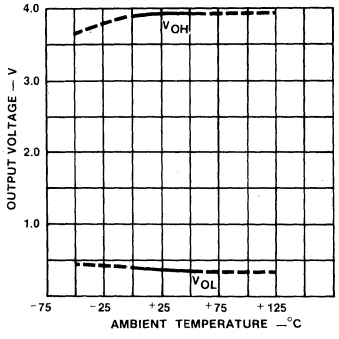
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



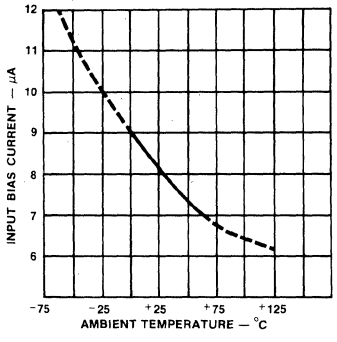
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



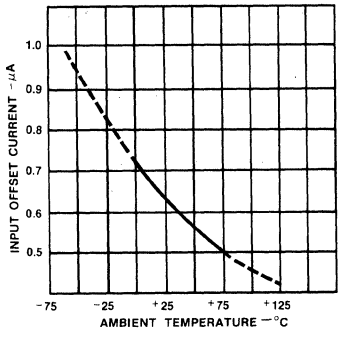
OUTPUT VOLTAGE vs AMBIENT TEMPERATURE



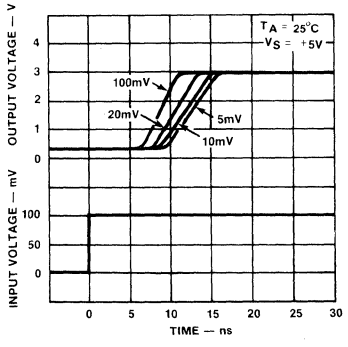
INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



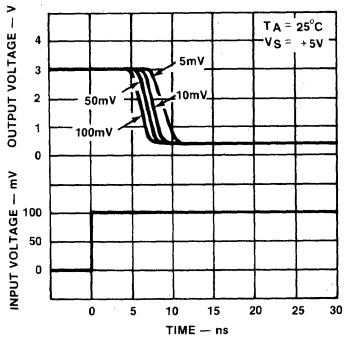
INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



75S208-F,N

DESCRIPTION

The 75S208 is a high speed dual sense amplifier that is functionally equivalent and pin compatible to the SN75208. The improved input sensitivity of ±10mV makes it suitable as a MOS memory sense amplifier which can result in faster memory cycles.

The 75S208 features less than 17ns propagation delay without sacrificing input performance characteristics. This is accomplished through the utilization of Schottky technology. It also features STTL compatible output levels with an open collector configuration for wired-AND logic applications.

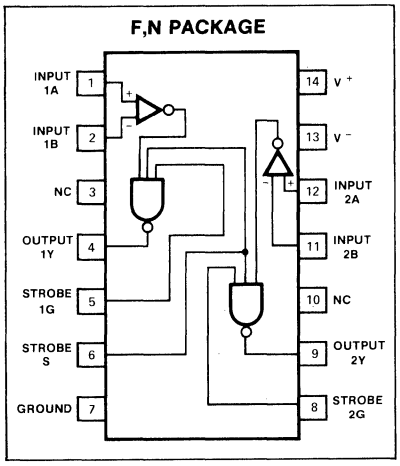
FEATURES

- **Functionally equivalent and pin compatible to 75208**
- **17ns maximum guaranteed propagation delay**
- **20μA maximum input bias current**
- **STTL compatible strobes and outputs**
- **Open collector outputs**
- **Large common mode input voltage range**
- **Operates from standard supply voltages**

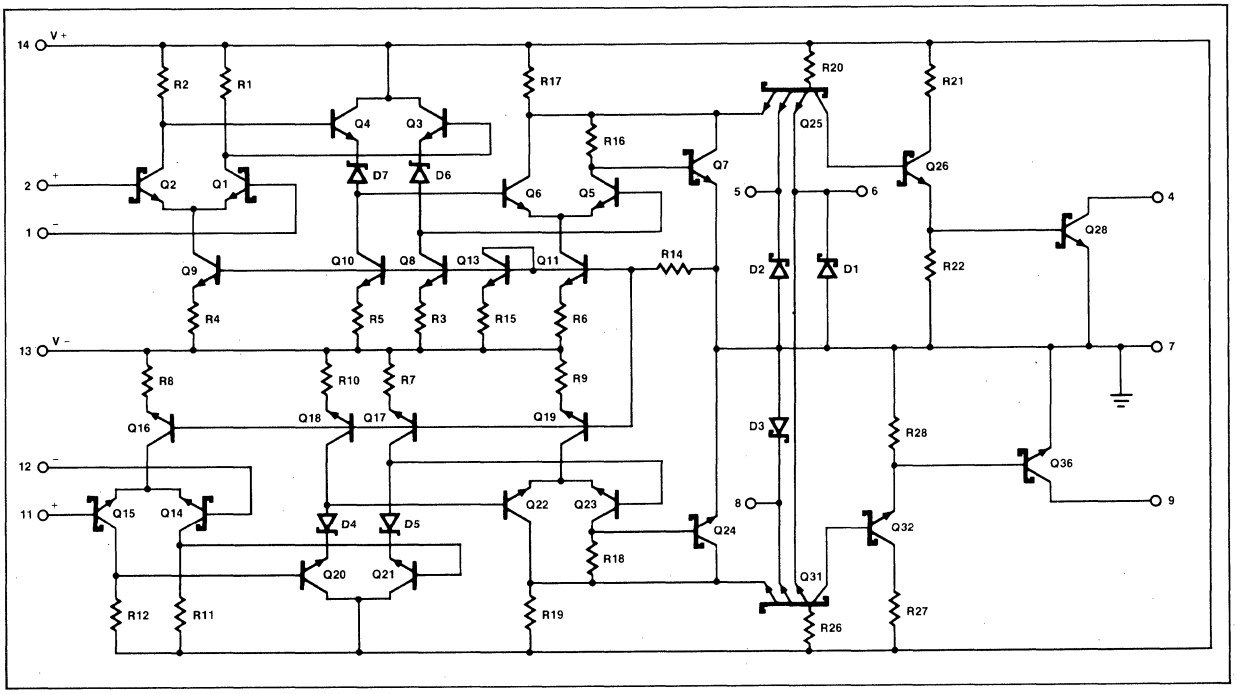
APPLICATIONS

- **MOS memories sense amp**
- **A/D conversion**
- **High speed line receiver**

PIN CONFIGURATION



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V+)	+7	V
Negative supply voltage (V-)	-7	V
Differential input voltage	±6	V
Common mode input voltage	±5	V
Strobe/gate input voltage	+5.5	V
Power dissipation	600	mW
Operating temperature range	0 to + 70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 60sec)	+300	°C

DC ELECTRICAL CHARACTERISTICS

V+ = +5.00, V- = -5.00, T_A = 0 to 70°C unless otherwise specified.

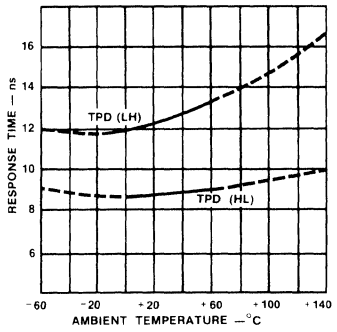
PARAMETER	TEST CONDITIONS	75S208			UNIT
		Min	Typ	Max	
AMPLIFIER INPUT					
Input offset voltage	V+ = 4.75, V- = -4.75			10	mV
Input bias current @ 25°C	V+ = 5.25, V- = -5.25		7.5	20	μA
over temp. range	V+ = 5.25, V- = -5.25			40	μA
Input offset current @ 25°C	V+ = 5.25, V- = -5.25		1.0	5	μA
over temp. range	V+ = 5.25, V- = -5.25			12	μA
Input common mode voltage range	V+ = 4.75, V- = -4.75	±3			V
Input resistance			4		kΩ
Input capacitance			3	6	pF
Voltage gain			5		V/mV
SCHOTTKY GATE/OUTPUT CHARACTERISTICS					
I_{IH} High level input current into 1G or 2G strobe	V+ = 5.25, V- = -5.25 V_{IH} = 2.7V			50	μA
	V_{IH} = 5.5V			1	mA
I_{IH} High level input current into common strobe S	V+ = 5.25, V- = -5.25 V_{IH} = 2.7V			100	μA
	V_{IH} = 5.5V			2	mA
I_{IL} Low level input current into 1G or 2G	V+ = 5.25, V- = -5.25 V_{IL} = 0.5V			-2.0	mA
I_{IL} Low level input current into common strobe S	V+ = 5.25, V- = -5.25 V_{IL} = 0.5V			-4.0	mA
V_{OL} Low level output voltage	V+ = 4.75, $V_{I(S)}$ = 2.0V V- = -4.75 I_{LOAD} = 20mA			0.5	V
I_{OH} High level output voltage	V_{CC}+ = 5.25 V V_{CC}- = -5.25V V_{OH} = 5.25V			250	μA
POWER SUPPLY REQUIREMENTS					
Supply voltage					
V+		4.75	5.00	5.25	V
V-		-4.75	-5.00	-5.25	V
I_{CC}+ Supply current	V+ = 5.25V		20	30	mA
I_{CC}-	V- = -5.25V		-11	-15	mA
	T_A = 25°C				
LARGE SIGNAL SWITCHING SPEED					
$T_pLH(D)$ Low to high propagation delay from amp inputs to output[1]	R_L = 280Ω C_L = 15pF T_A = 25°C		12	17	ns
$T_pHL(D)$ High to low propagation delay from amp inputs to output[1]	R_L = 280Ω C_L = 15pF T_A = 25°C		9	13	ns
$T_pLH(S)$ Low to high propagation delay from strobes input to output[2]	R_L = 280Ω C_L = 15pF T_A = 25°C		6	10	ns
$T_pHL(S)$ High to low propagation delay strobe input to output[2]	R_L = 280Ω C_L = 15pF T_A = 25°C		5	8	ns
Maximum operating frequency	R_L = 280Ω C_L = 15pF T_A = 25°C	25	35		MHz

NOTES

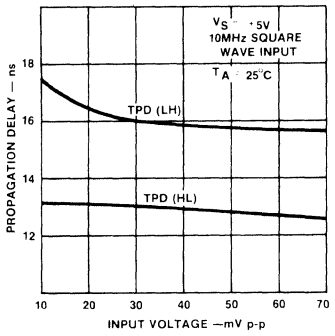
1. Response time measured from 0V point of ±100MHz square wave to the 1.5 point of the output.
2. Response time measured from 1.5V point of input to 1.5V point of the output.
3. Response time measured from the start of a 100mV input step with 5mV overdrive to the 1.5V point of the output.

TYPICAL PERFORMANCE CHARACTERISTICS

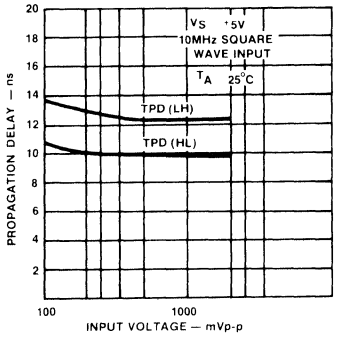
RESPONSE TIME vs TEMPERATURE



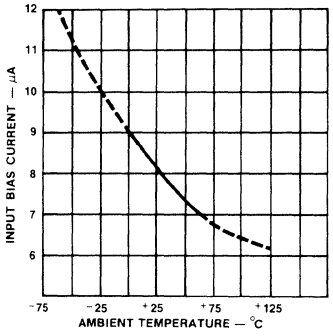
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



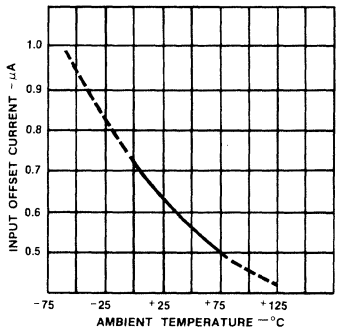
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



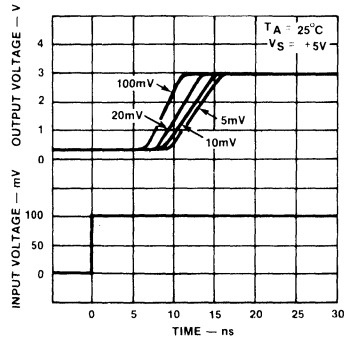
INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



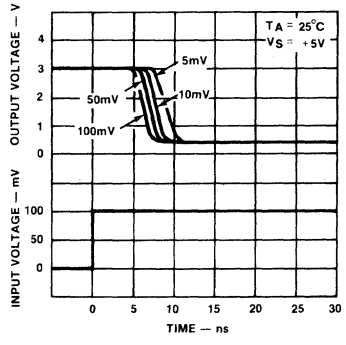
INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



DESCRIPTION

The 7520 series of dual channel sense amplifiers are designed for use with high speed core memory systems. These sense amplifiers detect low level bipolar differential signals from the memory and provide the interface circuitry between the memory element and the logic system. The device outputs are compatible with TTL and DTL logic.

The 7520 circuit may be used to perform the functions of a flip-flop or register which responds to the sense and strobe input conditions.

The 7522 circuit has a high fan-out, single-ended, open-collector output. In addition, it may be used to expand the input capability to a 7520 device, or to perform the wired-AND function.

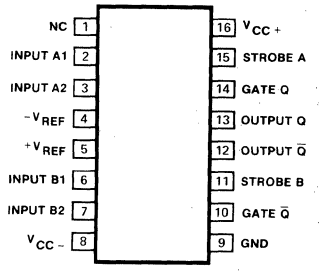
The 7524 circuit provides for independent dual-channel sensing with separate outputs. The 75234 is similar to the 7524, but has an inverted output function. The 75232 is an open-collector version of the 75234. The 7528 circuit is identical in function to the 7524, but has the output of each pre-amplifier stage brought out to test points.

FEATURES

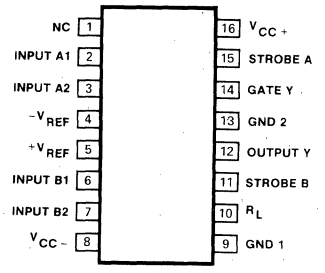
- **High speed—25ns propagation delay**
- **Adjustable input threshold levels**
- **±4mV threshold uncertainty**
- **Wide choice of output functions**
- **High dc noise margin**

PIN CONFIGURATIONS

F,N PACKAGE
7520



F,N PACKAGE
7522



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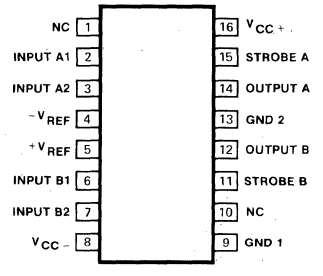
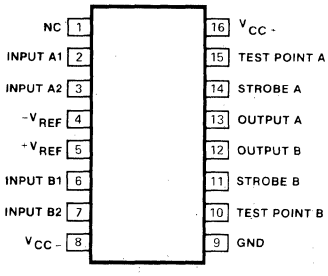
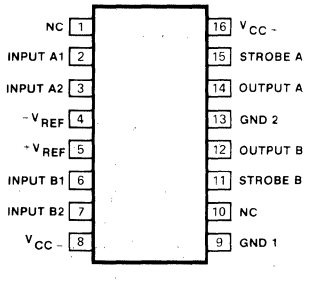


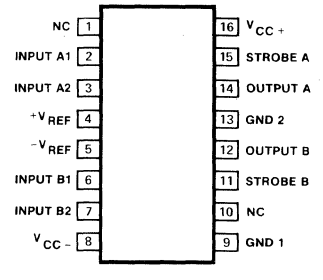
F,N PACKAGE
7528



F,N PACKAGE
75232



F,N PACKAGE
75234

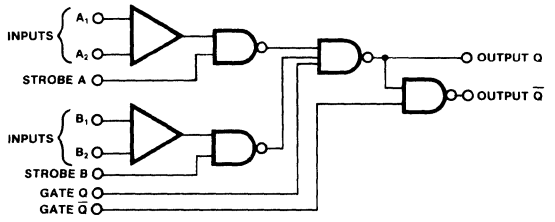


ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC+}	Supply voltage	7	V
V_{CC-}	Supply voltage	-7	V
V_{ID}	Differential input voltage	±5	V
V_{IN}	Input voltage	5.5	V
V_{OUT}	Off-state voltage applied to open-collector outputs	5.5	V
T_A	Operating temperature range	0 to +70	°C
T_{stg}	Storage temperature range	-55 to +150	°C
P_D	Power dissipation	500	mW

BLOCK DIAGRAMS

7520



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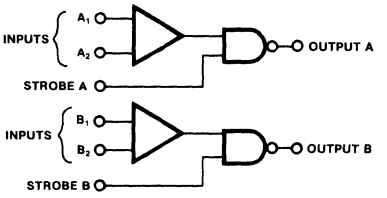

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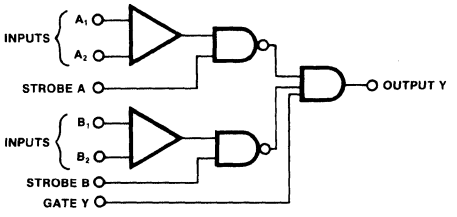

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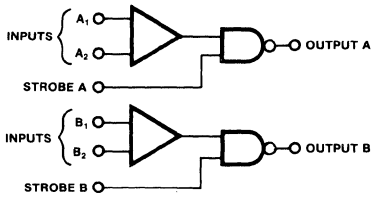

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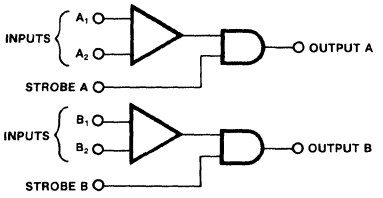

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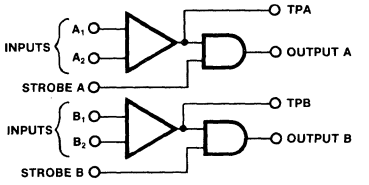
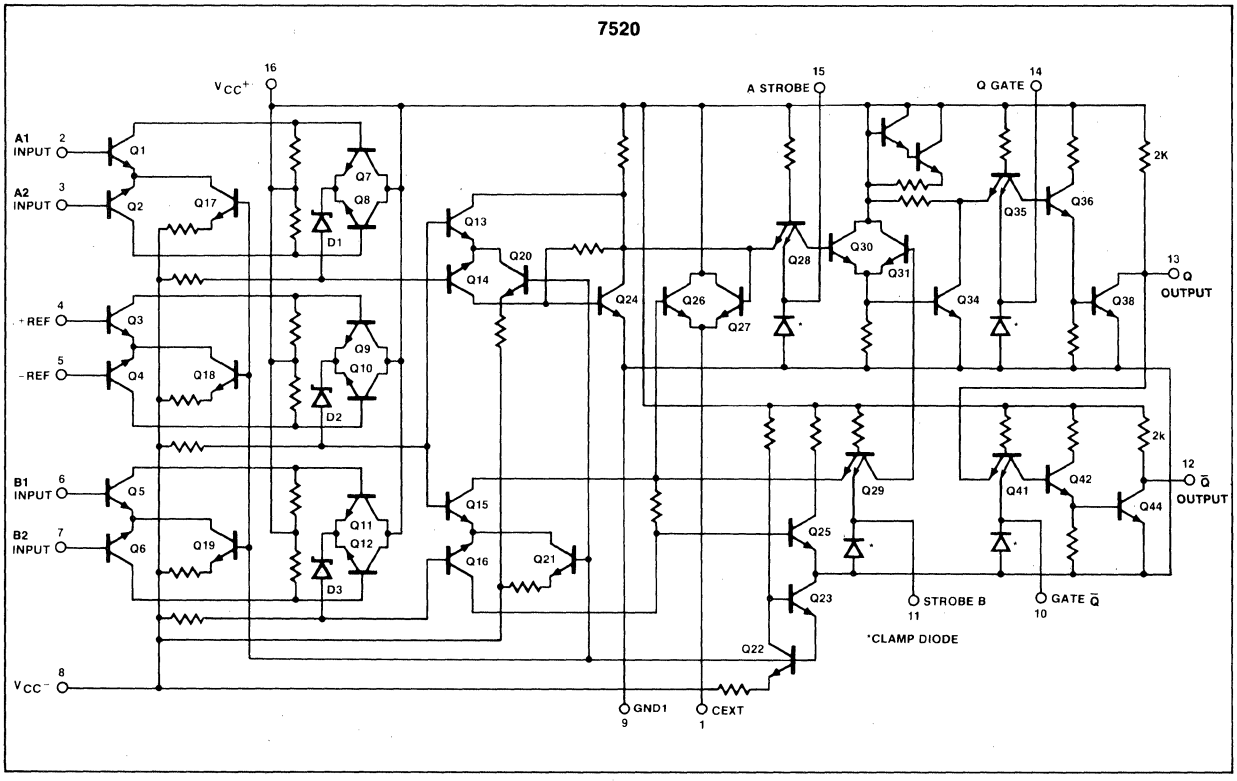


EQUIVALENT SCHEMATICS

7520



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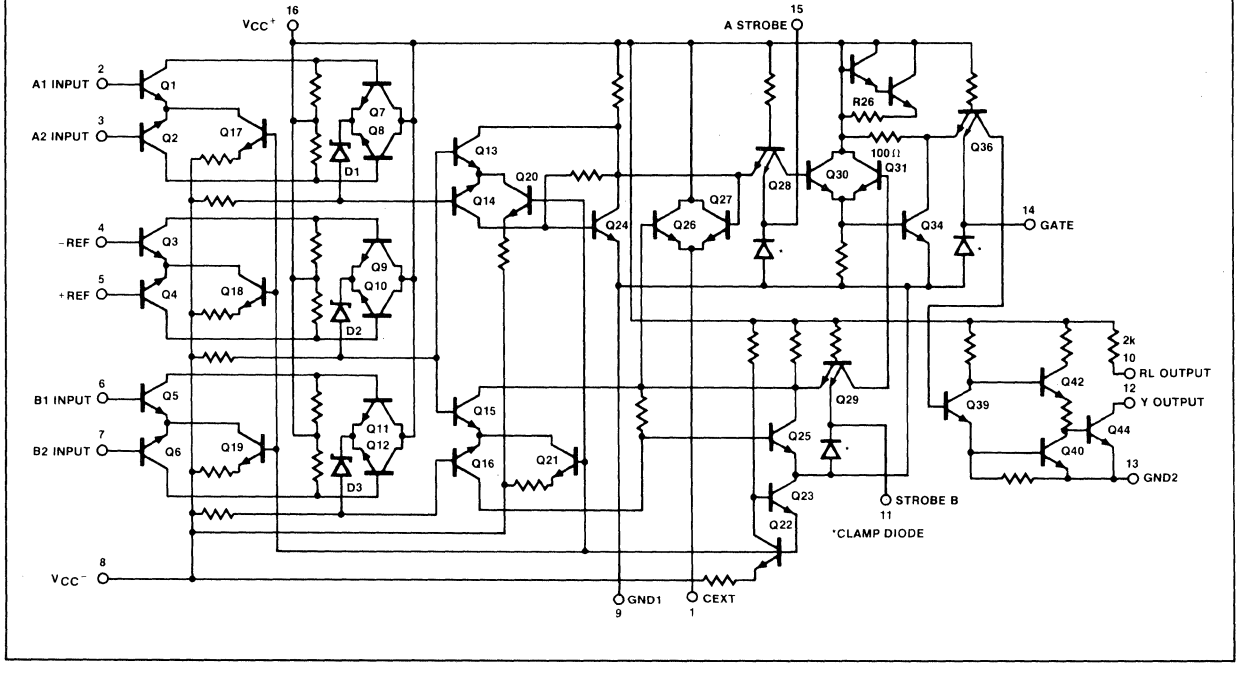
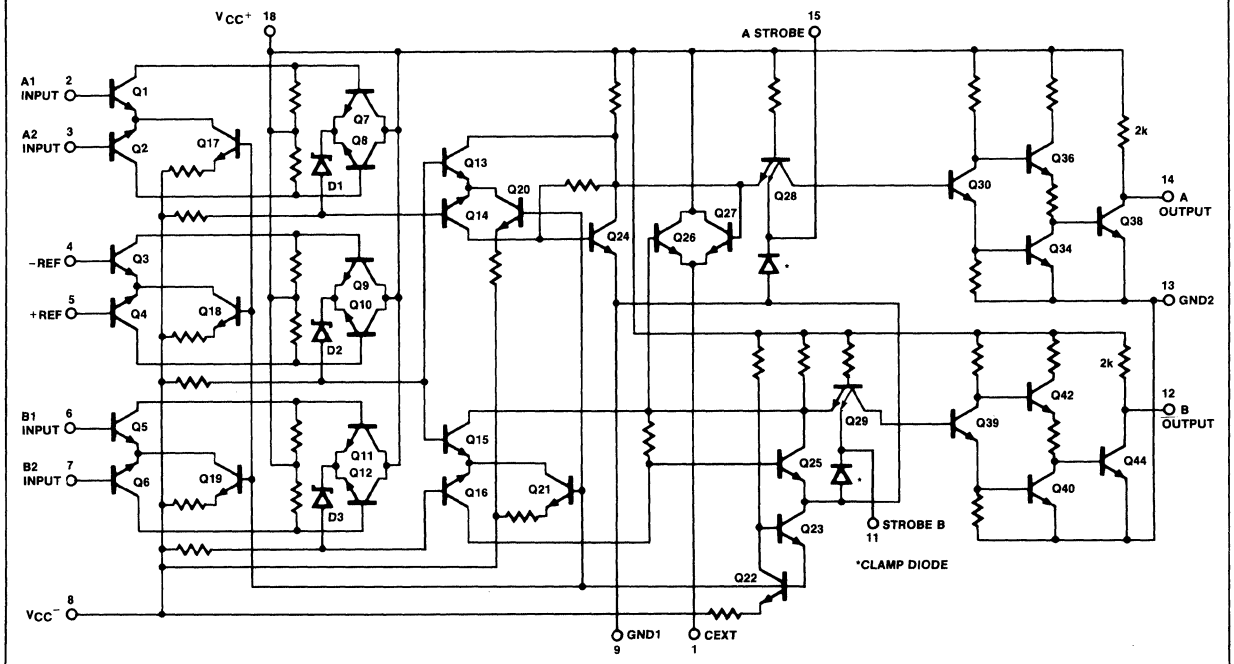


EQUIVALENT SCHEMATICS (Cont'd)

7524



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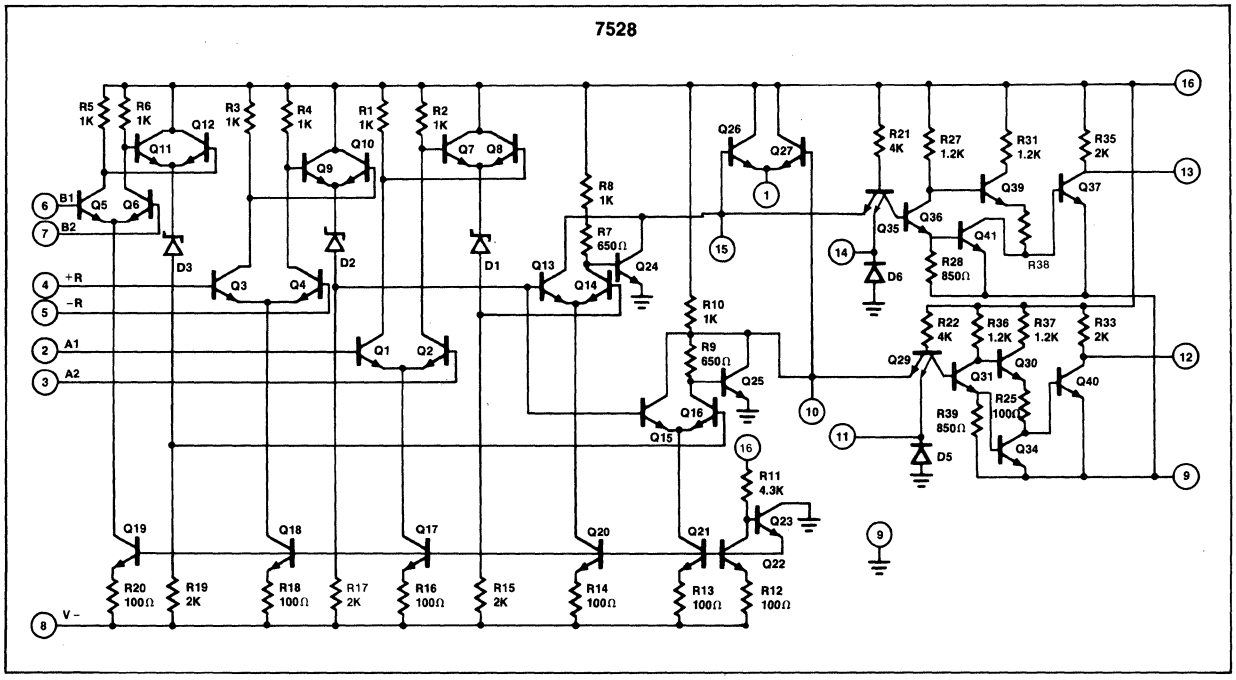
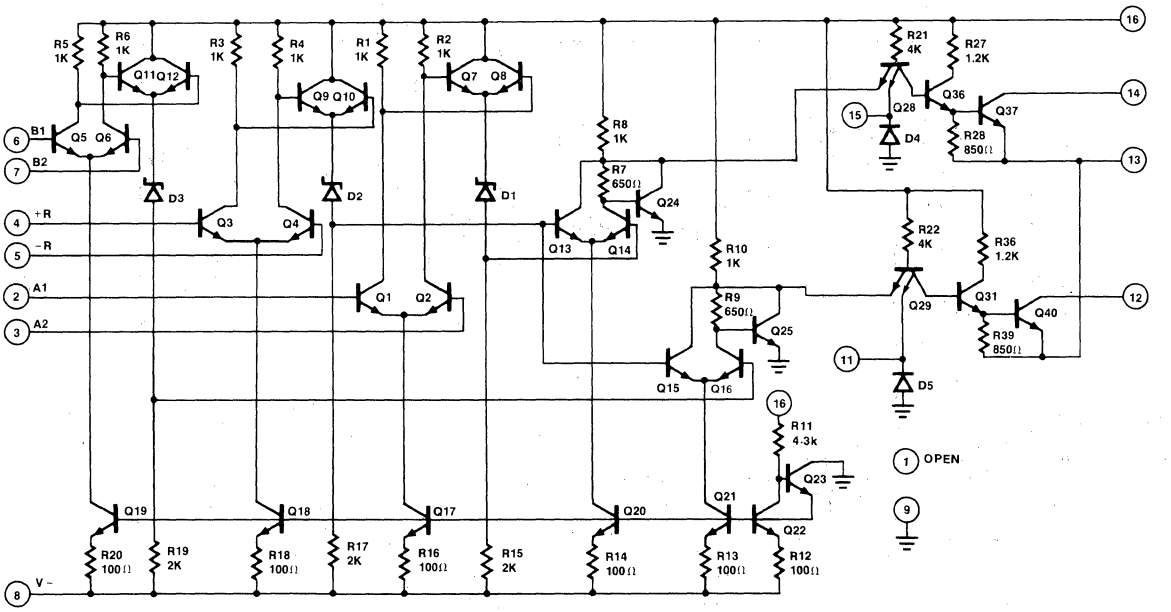


EQUIVALENT SCHEMATICS (Cont'd)

75232



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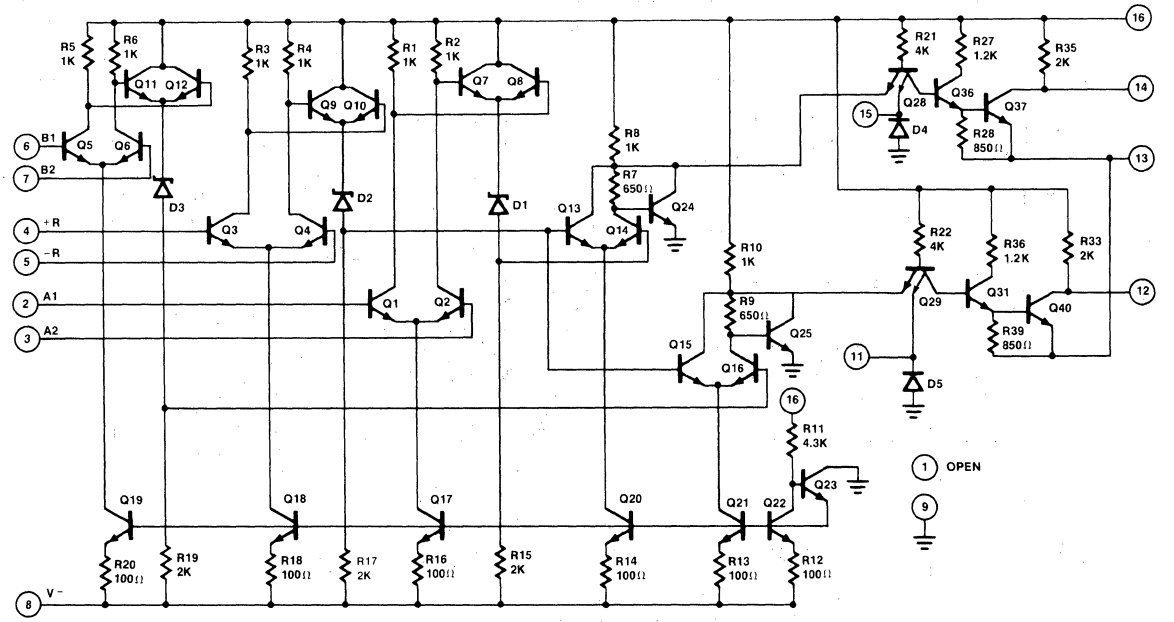


DC ELECTRICAL CHARACTERISTICS

T_A = 0 to70°C, V_{CC+} = 5V, V_{CC-} = -5V unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_T	Differential input threshold voltage	V_{ref} = 15mV V_{ref} = 40mV	11 36	15 40	19 44	mV mV
V_{ICF}	Common-mode input firing voltage	V_{ref} = 40mV, $V_{I(S)} = V_{IH}$ $t_r \leq 15ns$, $t_f \leq 15ns$, $t_w = 50ns$		±2.5		V
I_B	Differential input bias current	V_{CC+} = 5.25V, V_{CC-} = -5.25V V_{ID} = 0		30	75	μA
I_{OS}	Differential input offset current	V_{CC+} = 5.25V, V_{CC-} = -5.25V V_{ID} = 0		0.5		μA
V_{IH} V_{IL}	High level input voltage Low level input voltage		2		 0.8	V V
V_{OH}	High level output voltage	V_{CC+} = 4.75V, V_{CC-} = -4.75V I_{OH} = -400μA, NOT 75232	2.4	4		V
V_{OL}	Low level output voltage	V_{CC+} = 4.75V, V_{CC-} = -4.75V I_{OL} = 16mA		0.25	0.4	V
I_{OH}	High level output current	V_{CC+} = 4.75V, V_{CC-} = -4.75V V_{OH} = 5.25V, 75232 ONLY			250	μA
I_{IH}	High level input current	V_{CC+} = 5.25V, V_{CC-} = -5.25V V_{IH} = 2.4V			40	μA
I_{IL}	Low level input current	V_{CC+} = 5.25V, V_{CC-} = -5.25V V_{IL} = 0.4V		-1.0	-1.6	mA
I_{OS}	Short-circuit output current	V_{CC+} = 5.25V, V_{CC-} = -5.25V NOT Q output (pin 13) on 7520	-2.1		-3.5	mA
I_{OS}	Short-circuit output current	V_{CC+} = 5.25V, V_{CC-} = -5.25V Q output (pin 13) ONLY on 7520	-3		-5	mA
I_{CC+} I_{CC-}	Supply current from V_{CC+} Supply current from V_{CC-}	V_{CC+} = 5.25V, V_{CC-} = -5.25V, T_A = 25°C		27 -15	40 -20	mA mA

AC ELECTRICAL CHARACTERISTICS

PARAMETER		TO	FROM	TEST CONDITIONS	7520			UNIT
					Min	Typ	Max	
$t_{pd(1)}$	DQ	Q output	A1/A2 or B1/B2	C_L = 15pF, R_L = 288Ω		25	40	ns
$t_{pd(0)}$	DQ	Q output	A1/A2 or B1/B2	C_L = 15pF, R_L = 288Ω		20		ns
$t_{pd(1)}$	D$\overline{Q}$	$\overline{Q}$ output	A1/A2 or B1/B2	C_L = 15pF, R_L = 288Ω		30		ns
$t_{pd(0)}$	D$\overline{Q}$	$\overline{Q}$ output	A1/A2 or B1/B2	C_L = 15pF, R_L = 288Ω		35	55	ns
$t_{pd(1)}$	SQ	Q output	Strobe A or B	C_L = 15pF, R_L = 288Ω		15	30	ns
$t_{pd(0)}$	SQ	Q output	Strobe A or B	C_L = 15pF, R_L = 288Ω		20		ns
$t_{pd(1)}$	S$\overline{Q}$	$\overline{Q}$ output	Strobe A or B	C_L = 15pF, R_L = 288Ω		30		ns
$t_{pd(0)}$	S$\overline{Q}$	$\overline{Q}$ output	Strobe A or B	C_L = 15pF, R_L = 288Ω		35	55	ns
$t_{pd(1)}$	G$_Q$Q	Q output	Gate Q	C_L = 15pF, R_L = 288Ω		15	25	ns
$t_{pd(0)}$	G$_Q$Q	Q output	Gate Q	C_L = 15pF, R_L = 288Ω		10		ns
$t_{pd(1)}$	G$_Q$$\overline{Q}$	$\overline{Q}$ output	Gate Q	C_L = 15pF, R_L = 288Ω		15		ns
$t_{pd(0)}$	G$_Q$$\overline{Q}$	$\overline{Q}$ output	Gate Q	C_L = 15pF, R_L = 288Ω		20	30	ns
$t_{pd(1)}$	G$_{\overline{Q}}$$\overline{Q}$	$\overline{Q}$ output	Gate $\overline{Q}$	C_L = 15pF, R_L = 288Ω		15		ns
$t_{pd(0)}$	G$_{\overline{Q}}$$\overline{Q}$	$\overline{Q}$ output	Gate $\overline{Q}$	C_L = 15pF, R_L = 288Ω		10	20	ns

AC ELECTRICAL CHARACTERISTICS

PARAMETER		TO	FROM	TEST CONDITIONS	7522			UNIT
					Min	Typ	Max	
$t_{pd(1)}$	D	Y output	A1/A2 or B1/B2	C_L = 15pF, R_L = 288Ω		20		ns
$t_{pd(0)}$	D	Y output	A1/A2 or B1/B2	C_L = 15pF, R_L = 288Ω		30	45	ns
$t_{pd(1)}$	S	Y output	Strobe A or B	C_L = 15pF, R_L = 288Ω		20		ns
$t_{pd(0)}$	S	Y output	Strobe A or B	C_L = 15pF, R_L = 288Ω		20	40	ns
$t_{pd(1)}$	G	Y output	Gate Y	C_L = 15pF, R_L = 288Ω		10		ns
$t_{pd(0)}$	G	Y output	Gate Y	C_L = 15pF, R_L = 288Ω		15	25	ns

AC ELECTRICAL CHARACTERISTICS

PARAMETER		TO	FROM	TEST CONDITIONS	7524/7528			UNIT
					Min	Typ	Max	
$t_{pd(1)}$	D	Output A or B	A1/A2 or B1/B2	C_L = 15pF, R_L = 288Ω		25	40	ns
$t_{pd(0)}$	D	Output A or B	A1/A2 or B1/B2	C_L = 15pF, R_L = 288Ω		20		ns
$t_{pd(1)}$	S	Output A or B	Strobe A or B	C_L = 15pF, R_L = 288Ω		15	30	ns
$t_{pd(0)}$	S	Output A or B	Strobe A or B	C_L = 15pF, R_L = 288Ω		20		ns

AC ELECTRICAL CHARACTERISTICS

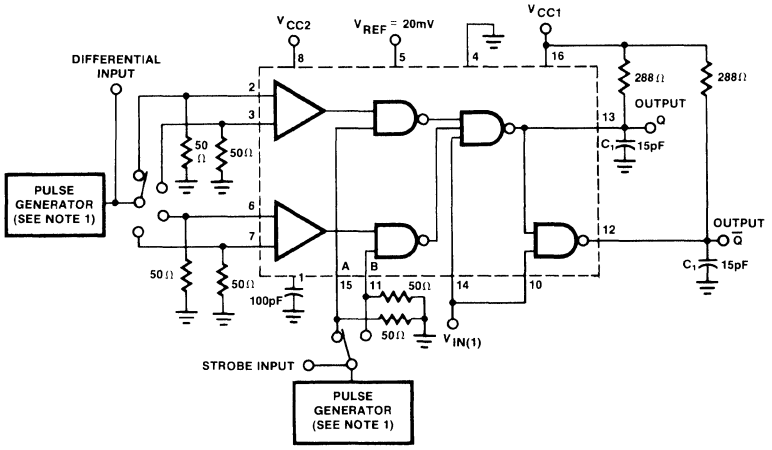
PARAMETER		TO	FROM	TEST CONDITIONS	75232/75234			UNIT
					Min	Typ	Max	
$t_{pd(1)}$	D	Output A or B	A1/A2 or B1/B2	C_L = 15pF, R_L = 288Ω		25		ns
$t_{pd(0)}$	D	Output A or B	A1/A2 or B1/B2	C_L = 15pF, R_L = 288Ω		25	40	ns
$t_{pd(1)}$	S	Output A or B	Strobe A or B	C_L = 15pF, R_L = 288Ω		25		ns
$t_{pd(0)}$	S	Output A or B	Strobe A or B	C_L = 15pF, R_L = 288Ω		15	30	ns

AC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_{orD}	Differential-input overload recovery time	V_{ID} = 2V $t_r = t_f$ = 20ns		20		ns
t_{orC}	Common-mode input overload recovery time	V_{IC} = ±2V $t_r = t_f$ = 20ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

TEST LOAD CIRCUITS—7520

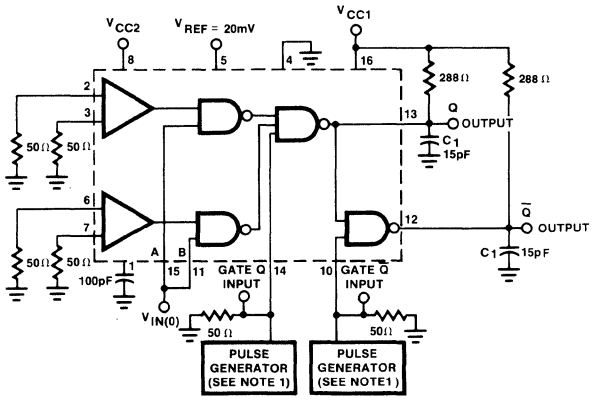
TEST CIRCUIT—DIFFERENTIAL AND STROBE INPUTS TO OUTPUTS



NOTES

1. Pulse generators have the following characteristics: Z_{OUT} = 50Ω, $t_r = t_f$ = 15(±5)ns, t_{p1} = 100ns, t_{p2} = 300ns, and PRR = 1MHz.
2. C_1 includes probe and jig capacitance.

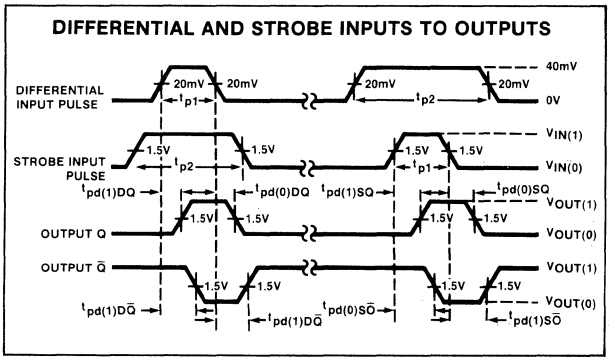
TEST CIRCUIT

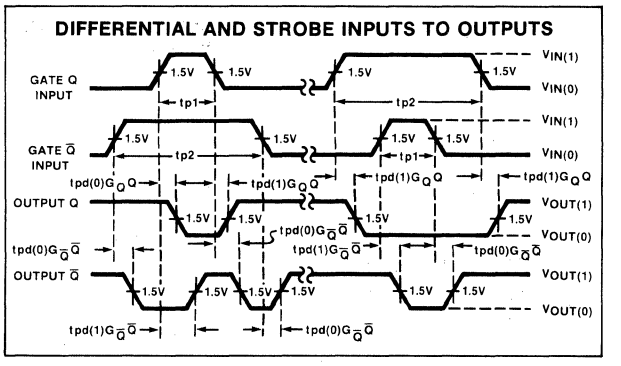


NOTES

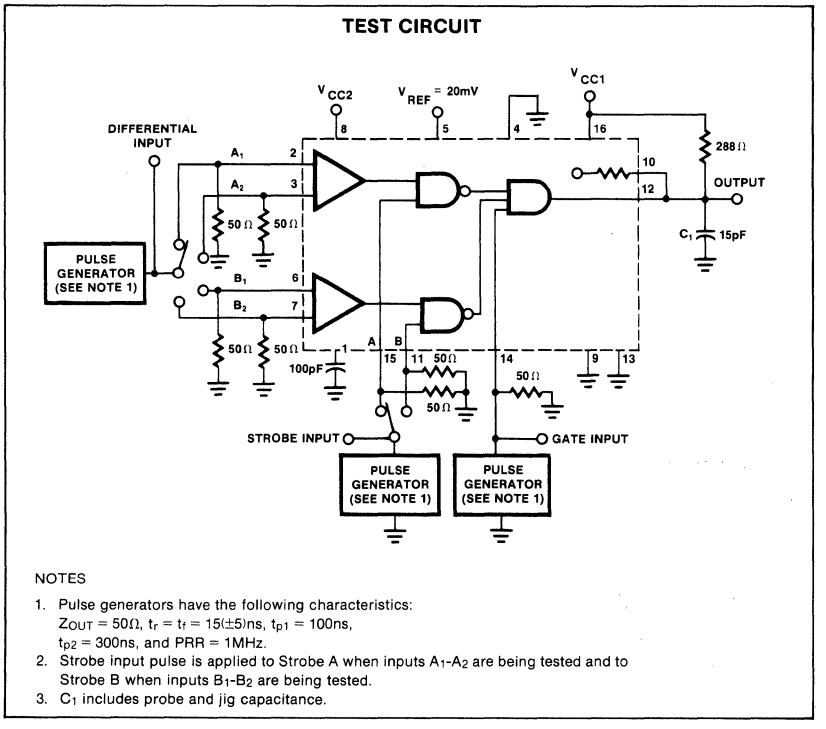
1. Pulse generators have the following characteristics: Z_{OUT} = 50Ω, $t_r = t_f$ = 15(±5)ns, t_{p1} = 100ns, t_{p2} = 300ns, and PRR = 1MHz.
2. C_1 includes probe and jig capacitance.

VOLTAGE WAVEFORMS—7520





TEST LOAD CIRCUIT—7522

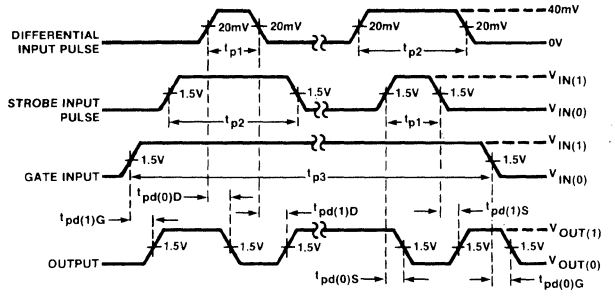


NOTES

1. Pulse generators have the following characteristics: $Z_{OUT} = 50\Omega$, $t_r = t_f = 15(\pm 5)$ns, $t_{p1} = 100$ns, $t_{p2} = 300$ns, and PRR = 1MHz.
2. Strobe input pulse is applied to Strobe A when inputs A_1-A_2 are being tested and to Strobe B when inputs B_1-B_2 are being tested.
3. C_1 includes probe and jig capacitance.

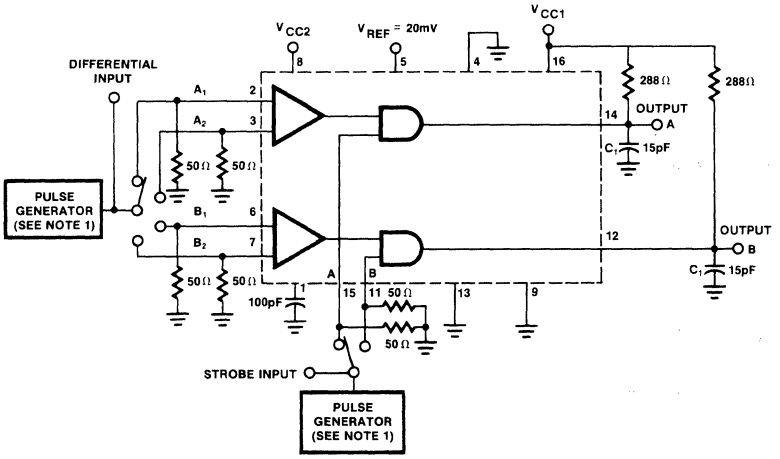
VOLTAGE WAVEFORM—7522

DIFFERENTIAL AND STROBE INPUTS TO OUTPUTS



TEST LOAD CIRCUIT—7524/7528

TEST CIRCUIT

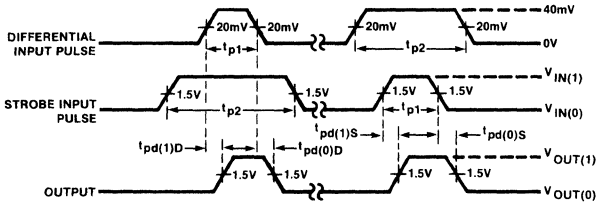


NOTES

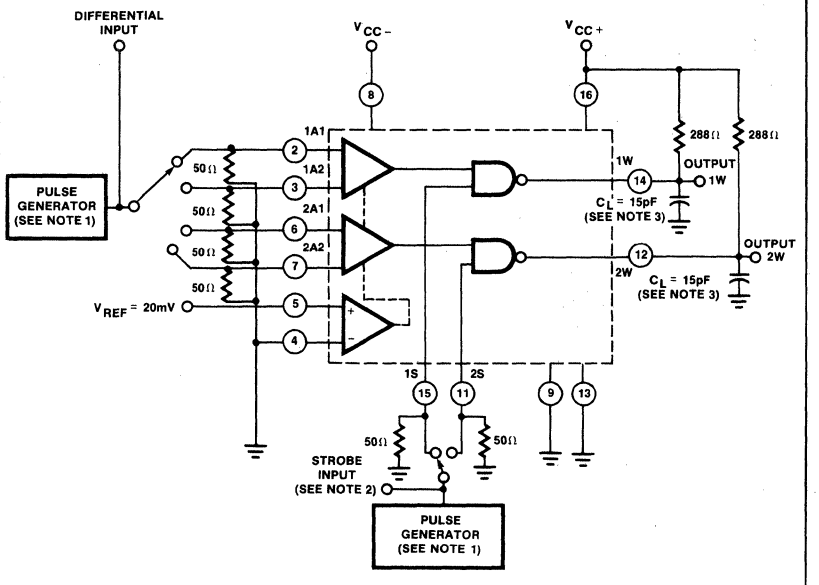
1. Pulse generators have the following characteristics: $Z_{OUT} = 50\Omega$, $t_r = t_f = 15(\pm 5)$ns, $t_{p1} = 100$ns, $t_{p2} = 300$ns, and PRR = 1MHz.
2. Strobe input pulse is applied to Strobe A when inputs A_1-A_2 are being tested and to Strobe B when inputs B_1-B_2 are being tested.
3. C_1 includes probe and jig capacitance.

VOLTAGE WAVEFORM—7524/7528

DIFFERENTIAL AND STROBE INPUTS TO OUTPUTS



TEST LOAD CIRCUIT—75232/75234

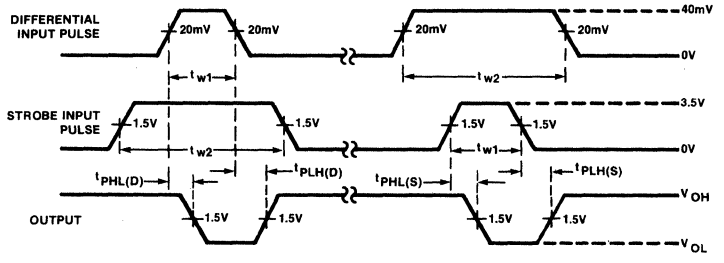


NOTES

1. The pulse generators have the following characteristics: Z_{OUT} = 50Ω, t_r = 15 ± 5ns, t_f = 15 ± 5ns, t_{w1} = 100ns, t_{w2} = 300ns, and PRR = 1MHz.
2. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2A2 are being tested.
3. C_L includes probe and jig capacitance.

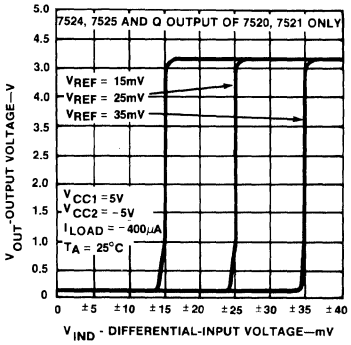
VOLTAGE WAVEFORM—75232/75234

DIFFERENTIAL AND STROBE INPUTS TO OUTPUTS

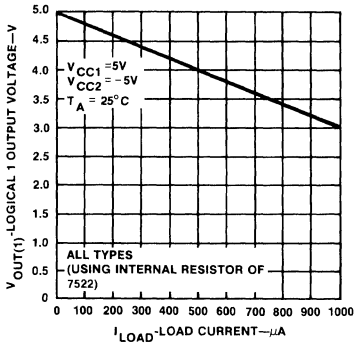


TYPICAL PERFORMANCE CHARACTERISTICS

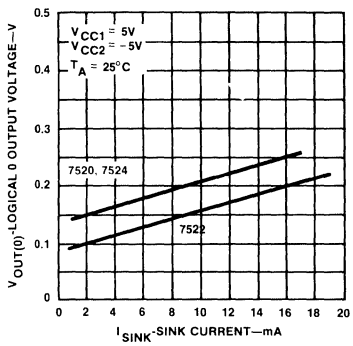
OUTPUT VOLTAGE vs DIFFERENTIAL-INPUT VOLTAGE



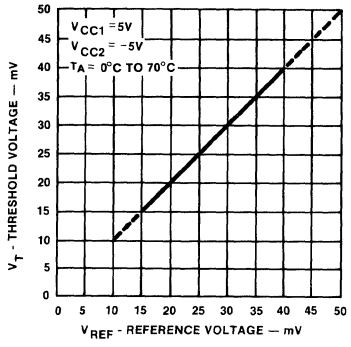
LOGICAL 1 OUTPUT VOLTAGE vs LOAD CURRENT



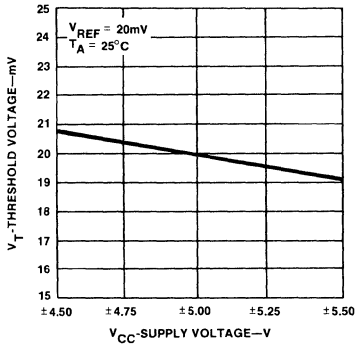
LOGICAL 0 OUTPUT VOLTAGE vs SINK CURRENT



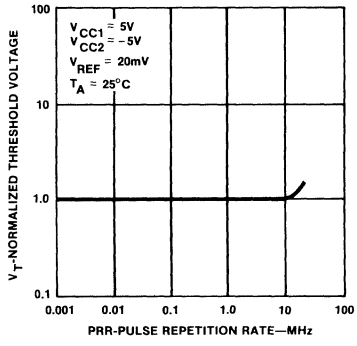
THRESHOLD VOLTAGE vs REFERENCE VOLTAGE



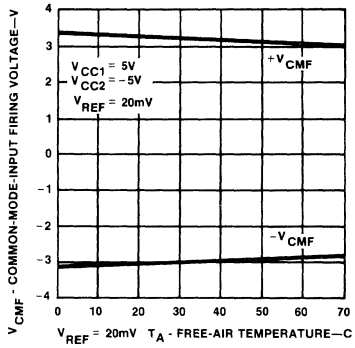
THRESHOLD VOLTAGE vs SUPPLY VOLTAGE



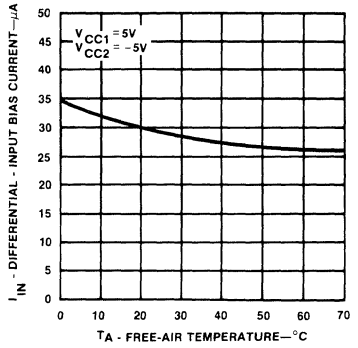
NORMALIZED THRESHOLD VOLTAGE vs PULSE REPETITION RATE



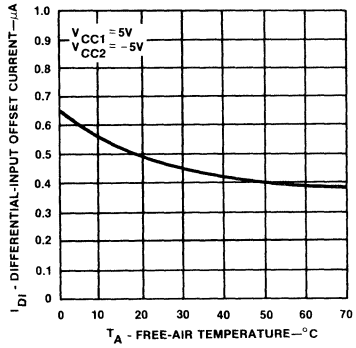
COMMON MODE FIRING VOLTAGE vs FREE-AIR TEMPERATURE



DIFFERENTIAL-INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

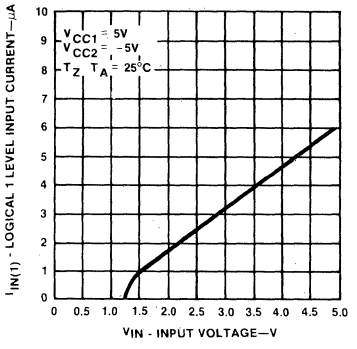


DIFFERENTIAL-INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

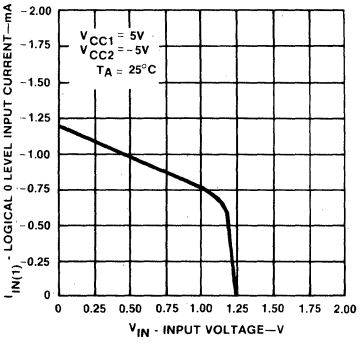


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

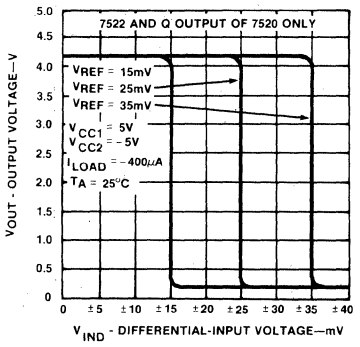
LOGICAL 1 LEVEL INPUT CURRENT vs INPUT VOLTAGE



LOGICAL 0 LEVEL INPUT CURRENT vs INPUT VOLTAGE



OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE



75324-F,N

DESCRIPTION

The 75324 is a monolithic memory driver with decode inputs designed for use with magnetic memories. The device contains two 400mA (source/sink) switch pairs with decoding capability from four address lines. Two address inputs (B and C) are used for mode selection, ie., source or sink. The other two address inputs (A and D) are used for switch-pair selection (output pair Y/Z or W/X).

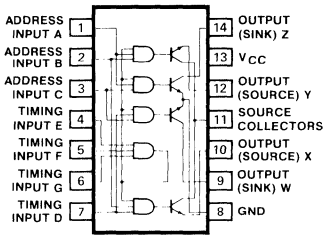
The sink circuit is composed of an inverting switch with a TTL input. The source circuit is an emitter-follower driven from a TTL input.

FEATURES

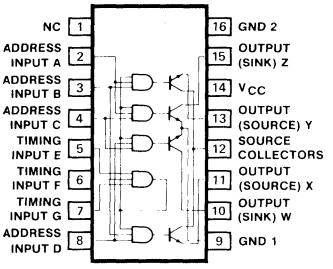
- **400mA output capability**
- **High voltage outputs**
- **Dual sink/source outputs**
- **Internal decoding and timing circuitry**
- **Fast switching times**
- **Output short-circuit protection**

PIN CONFIGURATIONS

N PACKAGE



F PACKAGE



GND 1 and GND 2 are to be used in parallel

ABSOLUTE MAXIMUM RATINGS

Over operating case temperature range unless otherwise specified.

PARAMETER	RATING	UNIT
Supply voltage V_{CC} [1]	17	V
Input voltage[2]	5.5	V
Operating case temperature range	0 to 70	°C
Continuous total power dissipation at (or below) 70°C case temperature	800	mW
Storage temperature range	-65 to +150	°C

NOTES

1. Voltage values are with respect to network ground terminal
2. Input signals must be zero or positive with respect to network ground terminal.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 14V unless otherwise specified.*

	PARAMETER	TEST FIGURE	TEST CONDITIONS	LIMITS Min	LIMITS Typ*	LIMITS Max	UNIT
V_{IH}	High-level input voltage	1		3.5			V
V_{IL}	Low-level input voltage	1				0.8	V
I_{IH}	High-level input current, address inputs	1	V_I = 5V			200	μA
I_{IH}	High-level input current, timing inputs	1	V_I = 5V			100	μA
I_{IL}	Low-level input current, address inputs	1	V_I = 0V			-6	mA
I_{IL}	Low-level input current, timing inputs	1	V_I = 0V			-12	mA
$V_{(SAT)}$	Sink saturation voltage	2	I_{SINK} ≅ 420mA, R_L = 53Ω		0.75	0.85	V
$V_{(SAT)}$	Source saturation voltage	2	I_{SOURCE} ≅ 420mA, R_L = 47.5Ω		0.75	0.85	V
I_{OFF}	Output off-state current	1	V_1 = 0V		125	200	μA
I_{CC}	Supply current, all sources and sinks off	3	V_1 = 0V		12.5	15	mA
I_{CC}	Supply current, either sink selected	4			30	42	mA
I_{CC}	Supply current, either source selected	4			25	35	mA

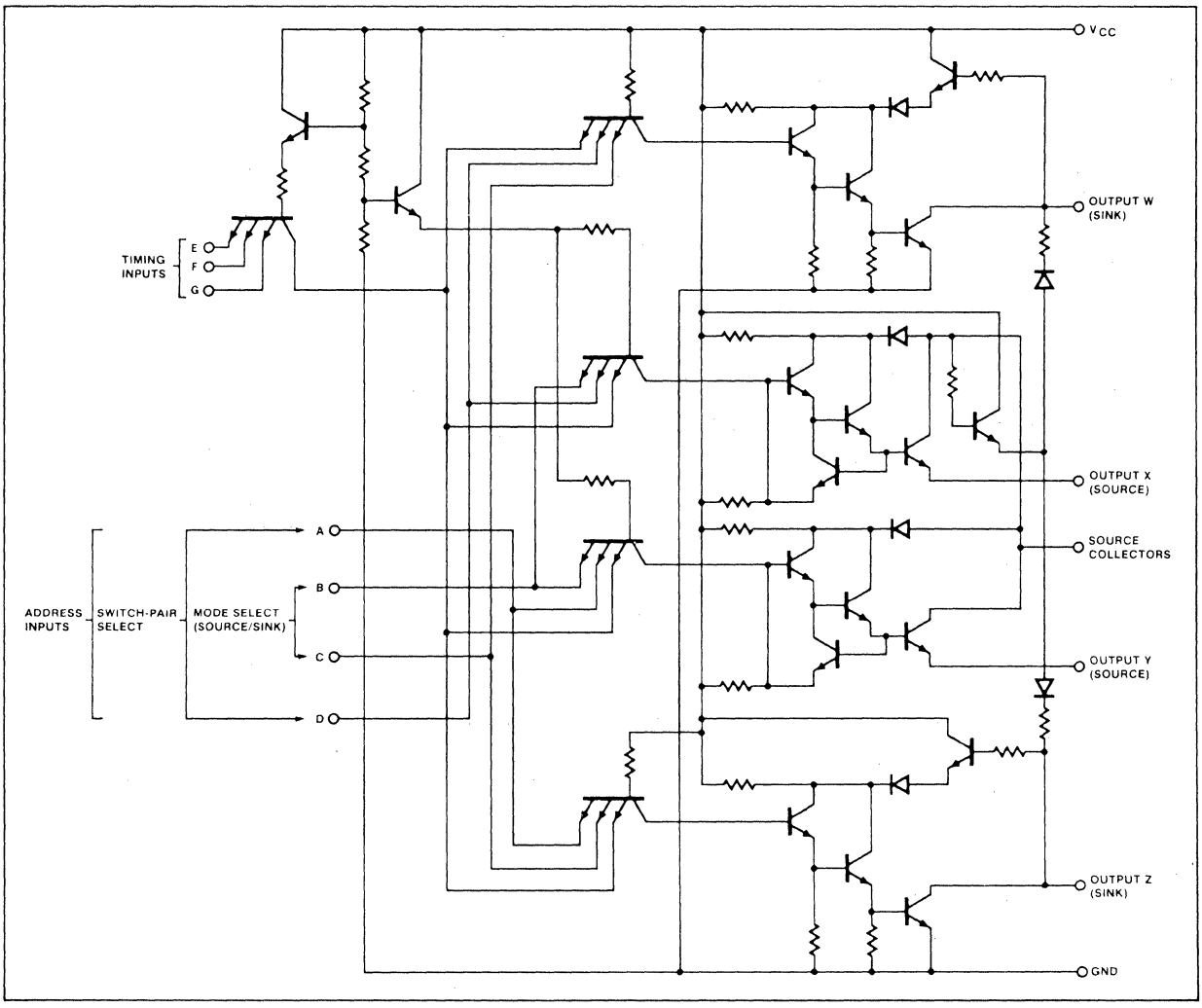
*NOTE

All typical values are at T_A = 25°C.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 14V$ unless otherwise specified.

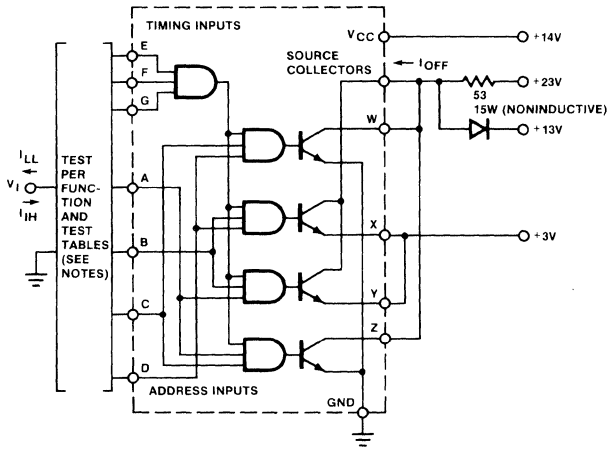
PARAMETER		TEST FIGURE	TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
t_{PLH}	Propagation delay time Low-to-high-level source output	5	$R_{L1} = 53\Omega$ $R_{L2} = 500\Omega$ $C_L = 20pF$			90	ns
t_{PHL}	Propagation delay time High-to-low-level source output	5				50	ns
t_{PLH}	Propagation delay time Low-to-high-level sink output	6	$R_L = 53\Omega$ $C_L = 20pF$			110	ns
t_{PHL}	Propagation delay time High-to-low-level sink output	6				40	ns
t_S	Sink storage time	6				70	ns

EQUIVALENT SCHEMATIC



PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*



V_{IL}, V_{IH}, I_{IL}, I_{IH}, AND I_{OFF}

TEST TABLE FOR I_{IL}

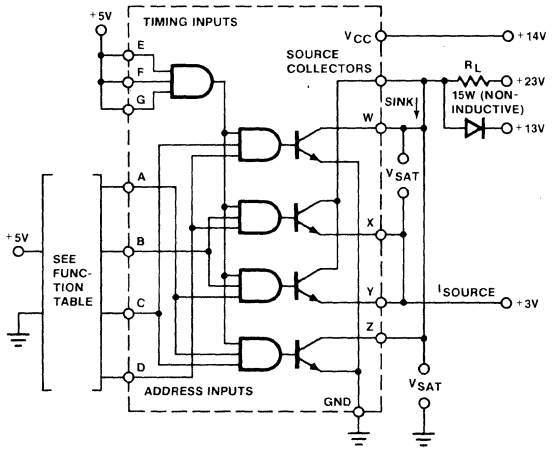
APPLY 3.5V	GROUND	TEST I_{IL}
B,C,E,F, and G	A and D	A
B,C,E,F, and G	A and D	D
A,D,E,F, and G	B and C	B
A,D,E,F, and G	B and C	C
A,B,C,D,F, and G	E	E
A,B,C,D,E, and G	F	F
A,B,C,D,E, and F	G	G

NOTES

1. Check V_{IH} and V_{IL} per Function Table.
2. Measure I_{IL} per Test Table.
3. When measuring I_{IH}, all other inputs are at ground. Each input is tested separately.

Figure 1

$V_{(SAT)}$



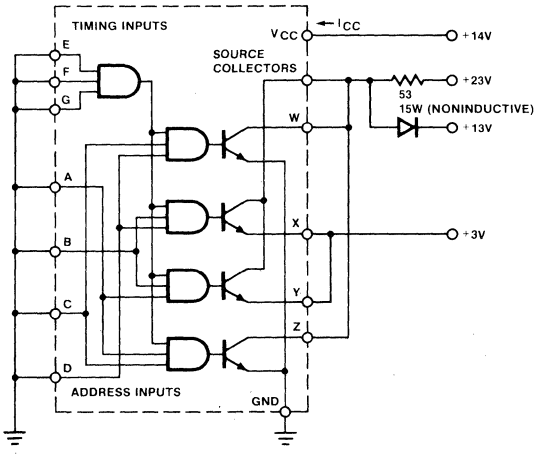
NOTE

This parameter must be using pulse techniques, $t_w = 500ns$, duty cycle $\leq 1\%$.

*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

Figure 2

I_{CC} (ALL OUTPUTS OFF)



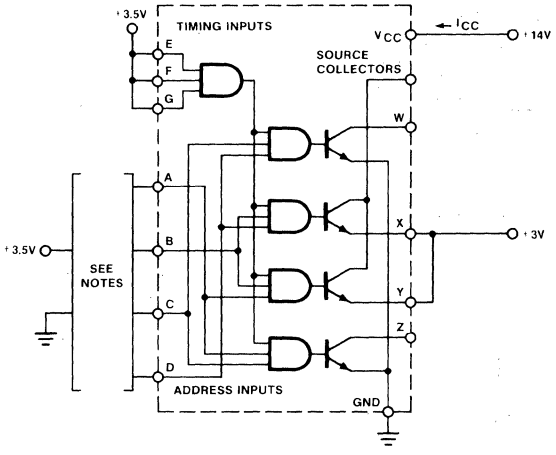
*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

Figure 3

PARAMETER MEASUREMENT INFORMATION (Cont'd)

I_{CC} (ONE OUTPUT ON)

DC TEST CIRCUITS*



NOTES

1. Ground A and B, apply 3.5V to C and D, and measure I_{CC} (output W is on).
2. Ground B and D, apply 3.5V to A and C, and measure I_{CC} (output Z is on).
3. Ground A and C, apply 3.5V to B and D, and measure I_{CC} (output X is on).
4. Ground C and D, apply 3.5V to A and B, and measure I_{CC} (output Y is on).

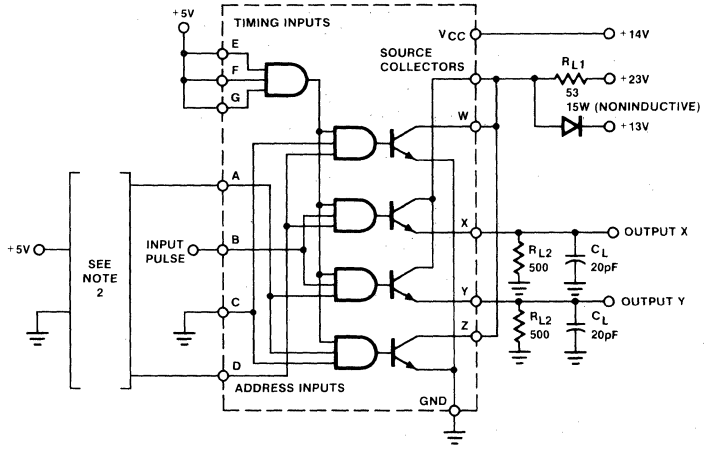
*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

Figure 4

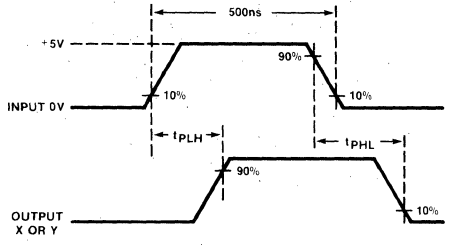
SWITCHING CHARACTERISTICS

SOURCE-OUTPUT SWITCHING TIMES

TEST CIRCUIT



VOLTAGE WAVEFORM



NOTES

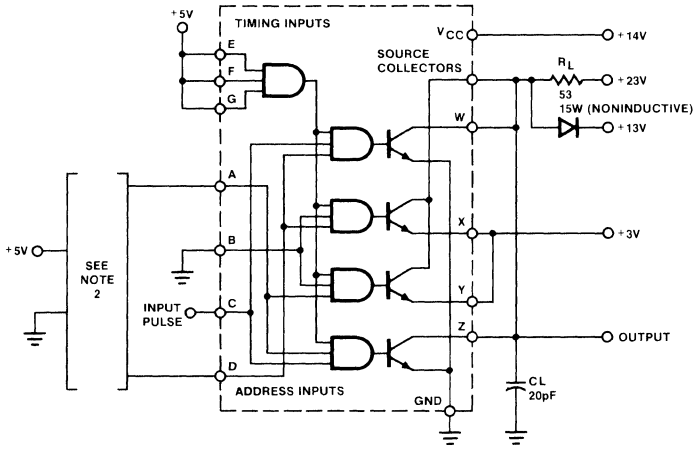
1. The input waveform is supplied by a generator with the following characteristics: $t_r = t_f = 10ns$, duty cycle $\leq 1\%$, and $Z_{OUT} \approx 50\Omega$.
2. When measuring delay times at output X, apply +5V to input D, and ground A. When measuring delay times at output Y, apply +5V to input A, and ground D.
3. C_L includes probe and jig capacitance.
4. Unless otherwise noted all resistors are 0.5W.

Figure 5

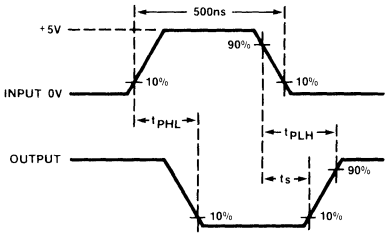
SWITCHING CHARACTERISTICS (Cont'd)

SINK-OUTPUT SWITCHING TIMES

TEST CIRCUIT



VOLTAGE WAVEFORM

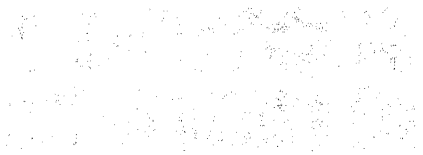


NOTES

1. The input waveform is supplied by a generator with the following characteristics: $t_r \approx t_f \approx 10$ns, duty cycle $\leq 1\%$, and $Z_{OUT} \approx 50$.
2. When measuring delay times at output X, apply +5V to input D, and ground A. When measuring delay times at output Y, apply +5V to input A, and ground D.
3. C_L includes probe and jig capacitance.

Figure 6

SECTION 7
INTERFACE



DS3611/3612/3613/3614-N,T

DESCRIPTION

The DS3611 series of dual peripheral drivers was designed for applications where higher breakdown voltage is required than that provided by the 75451 series.

The pin out for the 3611 series is identical to those of the 75451 through 75454. The 3611 series feature high voltage outputs (80V breakdown in the "off" state) as well as high current (300mA/driver in the on state).

FEATURES

- • **High voltage PNP inputs**
- • **PMOS/CMOS TTL or DTL compatible inputs**
- • **Low input currents**
- **High voltage outputs 80V (off)**
- **High current—300mA/driver (on)**
- **Input clamping diodes**
- **Choice of logic function**
- **DS3611/12/13/14, DS1611/12/13/14**
- **Military qualifications pending**

NOTE

- • **Special Signetics features**

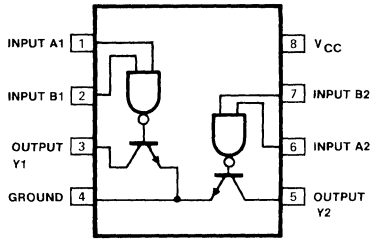
APPLICATIONS

- **Power drivers**
- **Relay drivers**
- **Lamp drivers**
- **Mos drivers**
- **Memory drivers**

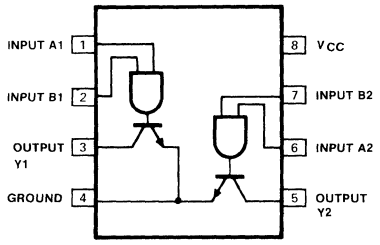
PIN CONFIGURATIONS

N PACKAGE

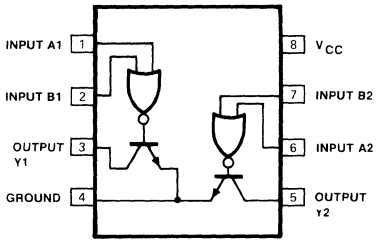
DUAL AND DRIVER
DS3611



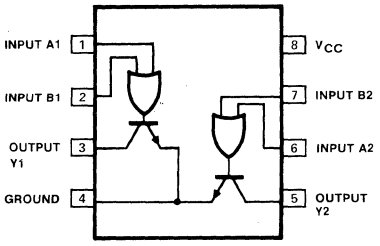
DUAL NAND DRIVER
DS3612



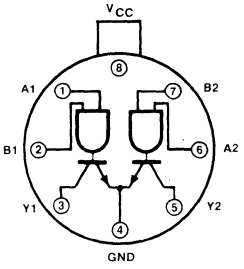
DUAL OR DRIVER
DS3613



DUAL NOR DRIVER
DS3614

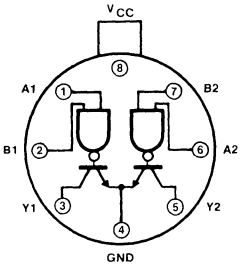


T PACKAGE
DS3611T



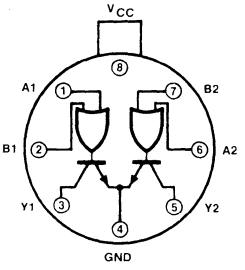
Pin 4 is in electrical contact with the case.

DS3612T



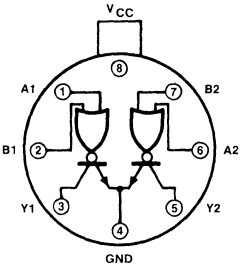
Pin 4 is in electrical contact with the case.

DS3613T



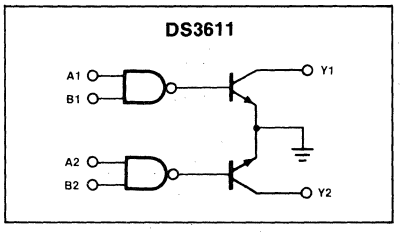
Pin 4 is in electrical contact with the case.

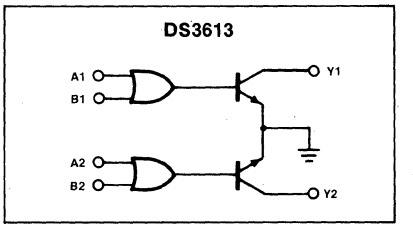
DS3614T

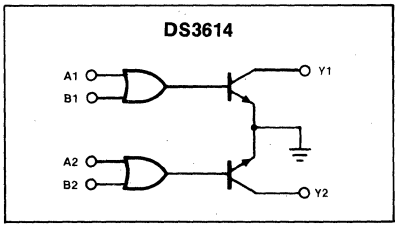


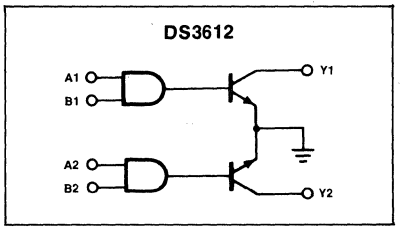
Pin 4 is in electrical contact with the case.

BLOCK DIAGRAMS

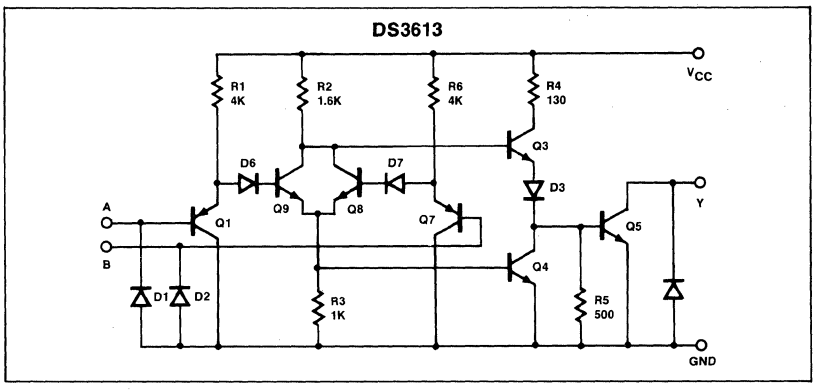


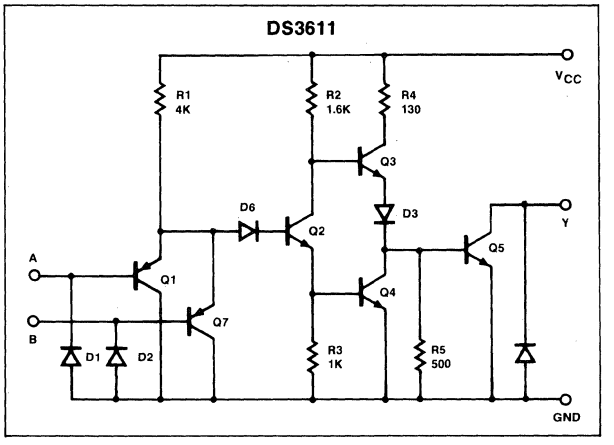


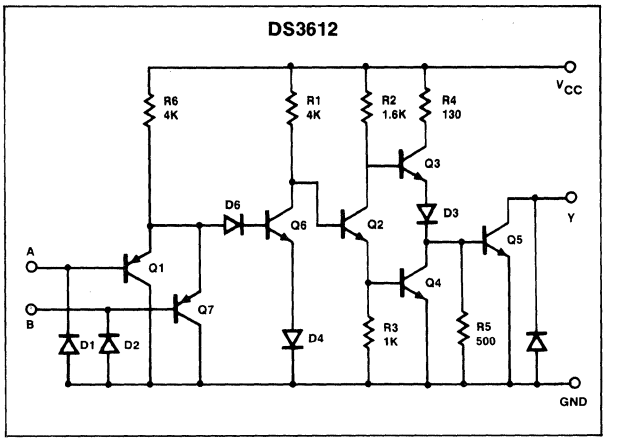


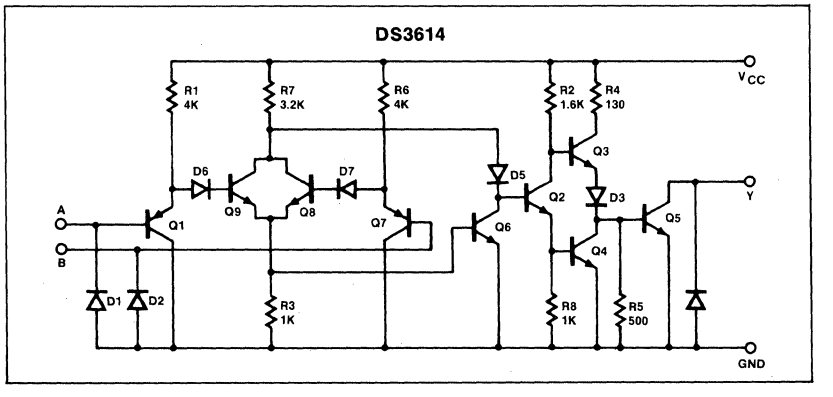


EQUIVALENT SCHEMATICS









NOTE
One circuit only shown

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage		
	continuous	7	V
	momentary (1 second)	15	V
V_{IN}	Input voltage	30	V
V_{OUT}	Output voltage (off state)	80	V
I_{OUT}	Output current (continuous)	300	mA
P_D	Power dissipation*	750	mW
T_A	Operating temperature range	0 to 70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
	Lead temperature (soldering, 10 sec)	300	°C

NOTE

*The maximum, junction temperature is 150°C. Derate at 162°C/Watt above 25°C.

DC ELECTRICAL CHARACTERISTICS

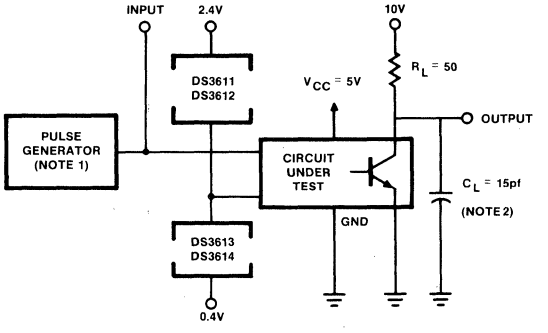
$T_A = 25°C$, $V_{CC} = 5V$, $0°C < T_A < 70°C$ unless otherwise specified.

	PARAMETER	TEST CONDITIONS	DS3611 SERIES			UNIT
			Min	Typ	Max	
V_{IH}	Logical "1" input voltage	$V_{CC} = 4.75V$	2.0			V
V_{IL}	Logical "0" input voltage	$V_{CC} = 4.75V$			0.8	V
V_I	Input clamp voltage	$V_{CC} = 4.75V$, $I_I = -12mA$		-1.2	-1.5	V
I_{IH}	Logical "1" input current	$V_{CC} = 5.25V$, $V_{IN} = 2.4V$			10	μA
		$V_{IN} = 5.5V$		<1	10	μA
		$V_{IN} = 30V$		1	100	μA
I_{IL}	Logical "0" input current	$V_{CC} = 5.25V$, $V_{IN} = 0.4V$		-50	-100	μA
V_{OL}	Output low voltage	$V_{IN} = 0.8V$ (DS3611/3613)				
		$V_{IN} = 2.0V$ (DS3612/3614)				
		$V_{CC} = 4.75V$, $I_{OL} = 100mA$		0.20	0.40	V
		$I_{OL} = 300mA$		0.45	0.70	V
V_{OH}	Output breakdown voltage	$V_{CC} = 5.25V$, $V_{IN} = 2.0V$ (DS3611/3613)				
		$V_{IN} = 0.8V$ (DS3612/3614)	80			V
		$I_{OH} = 100\mu A$				
I_{OH}	Output leakage current	$V_{IN} = 2.0V$ (DS3611/3613)				
		$V_{IN} = 0.8V$ (DS3612/3614)				
		$V_{OUT} = 80V$, $V_{CC} = 5.25V$			100	μA
		V_{CC} = open			100	μA
I_{CCH}	Supply current with outputs high	$V_{CC} = 5.25V$:				
		DS3611 - $V_{IN} = 5V$		5	11	mA
		DS3612 - $V_{IN} = 0V$		8	14	mA
		DS3613 - $V_{IN} = 5V$		8	14	mA
		DS3614 - $V_{IN} = 0V$		10	17	mA
I_{CCL}	Supply current with outputs low	$V_{CC} = 5.25V$:				
		DS3611 - $V_{IN} = 0V$		44	69	mA
		DS3612 - $V_{IN} = 5V$		47	71	mA
		DS3613 - $V_{IN} = 0V$		44	73	mA
		DS3614 - $V_{IN} = 5V$		49	79	mA

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5V, T_A = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	DS3611 SERIES			UNIT
			Min	Typ	Max	
T_{PLH}	Propagation delay time, low-to-high output	$I_O \simeq$ 200mA C_L = 15pf R_L = 50Ω (See test figure)				
		DS3611		130		ns
		DS3612		110		ns
		DS3613		125		ns
		DS3614		220		ns
T_{PHL}	Propagation delay time, high-to-low output					
		DS3611		125		ns
		DS3612		110		ns
		DS3613		125		ns
		DS3614		150		ns

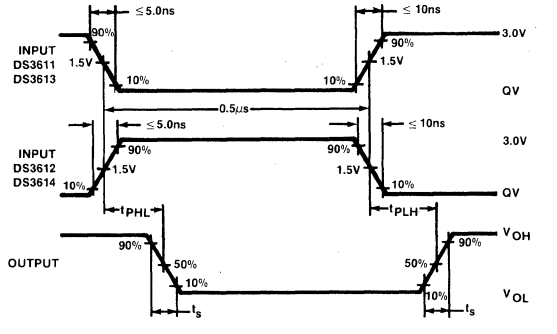
TYPICAL CIRCUIT



NOTES

1. The pulse generator has the following characteristics:
   PRR = 1.0MHz
   Z_{OUT} = 50
2. C_L includes probe and jig capacitances.

TIMING WAVEFORMS



DS7820/8820-F,N

DESCRIPTION

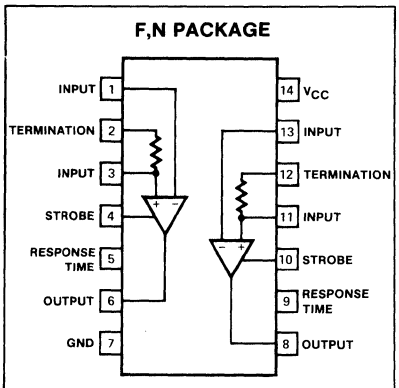
The DS7820, specified from -55°C to 125°C, and the DS8820, specified from 0°C to 70°C, are digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with RTL, DTL or TTL integrated circuits.

The response time can be controlled with an external capacitor to eliminate noise spikes, and the output state is determined for open inputs. Termination resistors for the twisted pair line are also included in the circuit. Both the DS7820 and the DS8820 are specified, worst case, over their full operating temperature range, for ±10-percent supply voltage variations and over the entire input voltage range.

FEATURES

- **Operation from a single +5V logic supply**
- **Input voltage range of ±15V**
- **Independent channel strobing**
- **High input resistance**
- **Fanout of two with DTL or TTL**
- **Output can be wire OR'ed**
- **DS7820 Mil std 883A,B,C available**

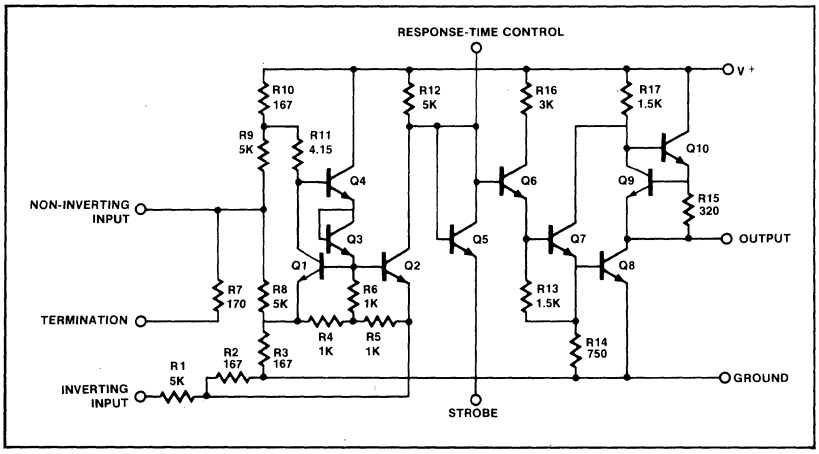
PIN CONFIGURATION



ORDER PART NO.

DS7820N, DS8820N
DS7820F, DS8820F

CIRCUIT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	8.0	V
Input voltage	±20	V
Differential input voltage	±20	V
Strobe voltage	8.0	V
Output sink current	25	mA
Power dissipation	600	mW
Operating temperature range		
DS7820	-55 to +125	°C
DS8820	0 to 70	°C
Lead temperature (soldering, 10sec)	300	°C

NOTE

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

7

DC ELECTRICAL CHARACTERISTICS

Specifications apply for $4.5V \leq V_{CC} \leq 5.5$, $-15V \leq V_{CM} \leq 15V$ and $-55°C \leq T_A \leq +125°C$ for the DS7820 or $0°C \leq T_A \leq +70°C$ for the DS8820 unless otherwise specified. Typical values given are for $V_{CC} = 5.0V$, $T_A = 25°C$ and $V_{CM} = 0V$ unless stated differently.[1,2,3]

PARAMETER		TEST CONDITIONS	DS7820			DS8820			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{TH}	Input threshold	$V_{IN} = 0V$	-0.5	0	0.5	-0.5	0	0.5	V
V_{TH}	Input threshold	$-15V \leq V_{IN} \leq 15V$	-1.0	0	1.0	-1.0	0	1.0	V
V_{OH}	High output level	$I_{OUT} \leq -0.2mA$	2.5		5.5	2.5		5.5	V
V_{OL}	Low output level	$I_{SINK} \leq 3.5mA$	0		0.4	0		0.4	V
$R_{IN}-$	Inverting input resistance		3.6	5.0		3.6	5.0		kΩ
$R_{IN}+$	Noninverting input resistance		1.8	2.5		1.8	2.5		kΩ
R_T	Line termination resistance		120	170	250	120	170	250	Ω
I_{ST}	Strobe current	$V_{Strobe} = 0.4V$		1.0	1.4		1.0	1.4	mA
I_{ST}	Strobe current	$V_{Strobe} = 5.5V$			-5			-5	μA
I_{CC}	Supply current[3]	$V_{IN} = 15V$		3.2	6.0		3.2	6.0	mA
I_{CC}	Supply current[3]	$V_{IN} = 0V$		5.8	10.2		5.8	10.2	mA
I_{CC}	Supply current[3]	$V_{IN} = -15V$		8.3	15.0		8.3	15.0	mA
$I_{IN}+$	Noninverting input current	$V_{IN} = 15V$		3.0	7.0		5.0	7.0	mA
$I_{IN}+$	Noninverting input current	$V_{IN} = 0V$	-1.6	-1.0		-1.6	-1.0		mA
$I_{IN}+$	Noninverting input current	$V_{IN} = -15V$	-9.8	-7.0		-9.8	-7.0		mA
$I_{IN}-$	Inverting input current	$V_{IN} = 15V$		3.0	4.2		3.0	4.2	mA
$I_{IN}-$	Inverting input current	$V_{IN} = 0V$		0	-0.5		0	-0.5	mA
$I_{IN}-$	Inverting input current	$V_{IN} = -15V$	-4.2	-3.0		-4.2	-3.0		mA

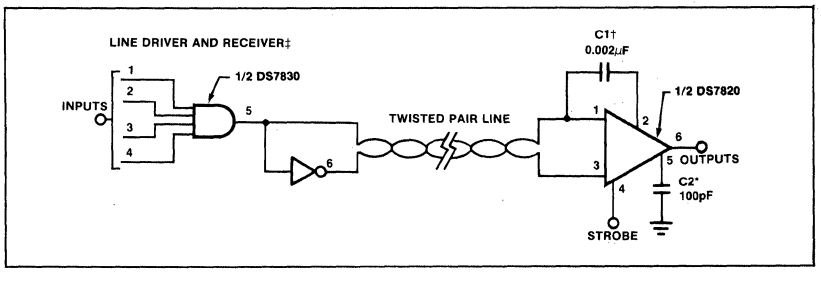
NOTES

1. All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.
2. Only one output at a time should be shorted.
3. The specifications and curves given are for one side only. Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions.

AC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	DS7820			DS8820			UNIT
		Min	Typ	Max	Min	Typ	Max	
T_R Response time	$C_{delay} = 0$		40			40		ns
T_R Response time	$C_{delay} = 100pF$		150			150		ns

DS7820-DS8820 TYPICAL APPLICATION



†Exact value depends on line length
‡V_{CC} is 4.5V to 5.5V for both the DS7820 and DS7830
*Optional to control response time

N/F

DESCRIPTION

The DS7820A and the DS8820A are improved performance digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with RTL, DTL or TTL integrated circuits.

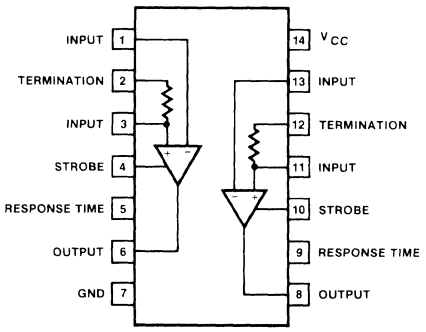
The response time can be controlled with an external capacitor to reject input noise spikes. The output state is a logic "1" for both inputs open. Termination resistors for the twisted pair line are also included in the circuit. Both the DS7820A and the DS8820A are specified, worst case, over their full operating temperature range (-55°C to 125°C and 0°C to 70°C respectively), over the entire input voltage range, for ±10% supply voltage variations.

FEATURES

- **Operation from a single +5V logic supply**
- **Input voltage range of ±15V**
- **Strobe low forces output to "1" state**
- **High input resistance**
- **Fanout of ten with either DTL or TTL integrated circuits**
- **Outputs can be wire OR'ed**
- **Series 54/74 compatible**

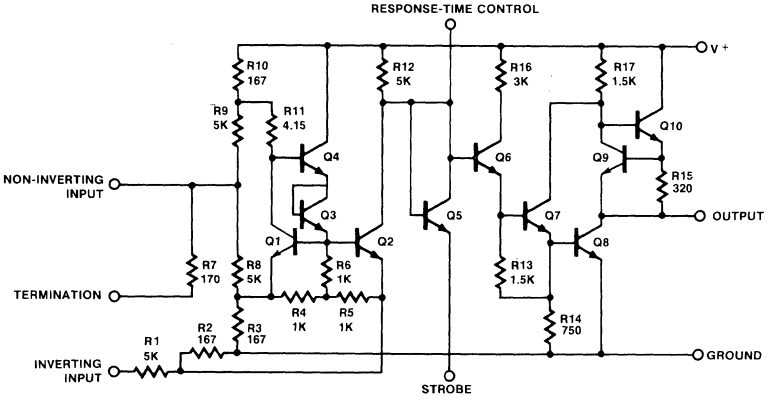
PIN CONFIGURATION

N/F PACKAGE



ORDER PART NO.
DS7820AN, DS7820AF
DS8820AN, DS8820AF

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS*

PARAMETER	RATING	UNIT
Supply voltage	8.0	V
Input voltage	±20	V
Differential input voltage	±20	V
Strobe voltage	8.0	V
Output sink current	50	mA
Power dissipation	600	mW
Operating temperature range		
DS7820A	-55 to +125	°C
DS8820A	0 to +70	°C
Lead temperature (soldering, 60sec)	300	°C

*NOTE

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

7

N/F

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.[1,2,3,4]

PARAMETER		TEST CONDITIONS	DS7820A/DS8820A Min	Typ	Max	UNIT
V_{TH}	Differential threshold voltage	$I_{OUT} = -400\mu A$ $-3V \le V_{CM} \le +3V$ $V_{OUT} \ge 2.5V$ $-15V \le V_{CM} \le +15V$ $I_{OUT} = +16mA$ $-3V \le V_{CM} \le +3V$ $V_{OUT} \le 0.4V$ $-15V \le V_{CM} \le +15V$		0.06 0.06 -0.08 -0.08	0.5 1.0 -0.5 -1.0	V V V V
R_I^-	Inverting input resistance	$-15V \le V_{CM} \le +15V$	3.6	5		kΩ
R_I^+	Non-inverting input resistance	$-15V \le V_{CM} \le +15V$	1.8	2.5		kΩ
R_T	Line termination resistance		120	170	250	Ω
I_I^-	Inverting input current	$V_{CM} = 15V$ $V_{CM} = 0V$ $V_{CM} = -15V$		3.0 0 -3.0	4.2 -0.5 -4.2	mA mA mA
I_I^+	Non-inverting input current	$V_{CM} = 15V$ $V_{CM} = 0V$ $V_{CM} = -15V$		5.0 -1.0 -7.0	7.0 -1.6 -9.8	mA mA mA
I_{CC}	Power supply current	$V_{DIFF} = -1V$, I_{OUT} = Logical "0" $V_{CM} = 15V$ $V_{DIFF} = -1V$, I_{OUT} = Logical "0" $V_{CM} = -15V$ $V_{DIFF} = -0.5V$, $V_{CM} = 0V$		3.9 9.2 6.5	6.0 14.0 10.2	mA mA mA
V_{OH} V_{OL}	Logical "1" output voltage Logical "0" output voltage	$I_{OUT} = -400\mu A$, $V_{DIFF} = 1V$ $I_{OUT} = +16mA$, $V_{DIFF} = -1V$	2.5 0	4.0 0.22	5.5 0.4	V V
V_{SH} V_{SL}	Logical "1" strobe input voltage Logical "0" strobe input voltage	$I_{OUT} = +16mA$, $V_{OUT} \le 0.4V$, $V_{DIFF} = -3V$ $I_{OUT} = -400\mu A$, $V_{OUT} \ge 2.5V$, $V_{DIFF} = -3V$	2.1		 0.9	V V
I_{SH} I_{SL}	Logical "1" strobe input current Logical "0" strobe input current	$V_{STROBE} = 5.5V$, $V_{DIFF} = 3V$ $V_{STROBE} = 0.4V$, $V_{DIFF} = -3V$		0.01 -1.0	5.0 -1.4	μA mA
I_{SC}	Output short circuit current	$I_{OUT} = 0V$, $V_{CC} = 5.5V$, $V_{STROBE} = 0V$	-2.8	-4.5	-6.7	mA

NOTES

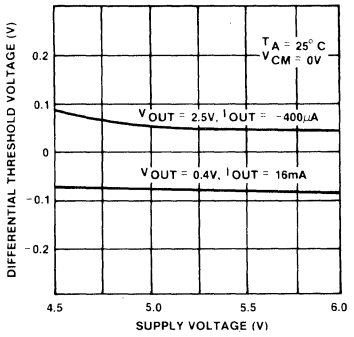
1. These specifications apply for $4.5V \le V_{CC} \le 5.5V$, $-15V \le V_{CM} \le 15V$ and $-55°C \le T_A \le +125°C$ for the DS7820A or $0°C \le T_A \le +70°C$ for the DS8820A unless otherwise specified. Typical values given are for $V_{CC} = 5.0V$, $T_A = 25°C$ and $V_{CM} = 0V$ unless stated differently.
2. All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.
3. Only one output at a time should be shorted.
4. The specifications and curves given are for one side only. Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V$ unless otherwise specified.

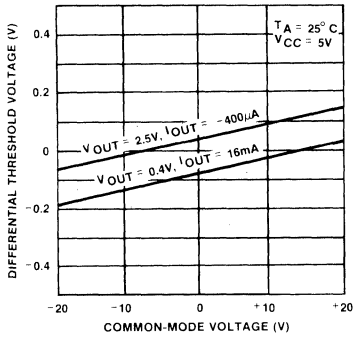
PARAMETER		TEST CONDITIONS	DS7820A/DS8820A Min	Typ	Max	UNIT
t_{PD0}	Propagation delay, differential input to "0" output			30	45	ns
t_{PD1}	Propagation delay, differential input to "1" output			27	40	ns
t_{PD0}	Propagation delay, strobe input to "0" output			16	25	ns
t_{PD1}	Propagation delay, strobe input to "1" output			18	30	ns

TYPICAL PERFORMANCE CHARACTERISTICS

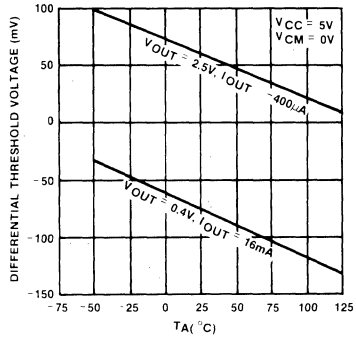
SUPPLY VOLTAGE SENSITIVITY



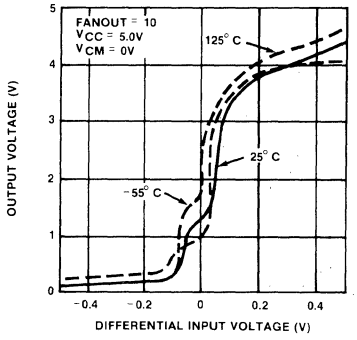
COMMON-MODE VOLTAGE SENSITIVITY



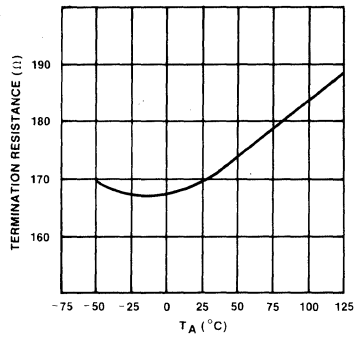
TEMPERATURE SENSITIVITY



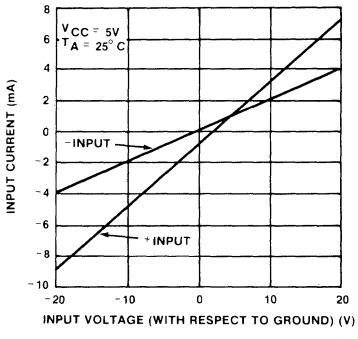
TRANSFER FUNCTION



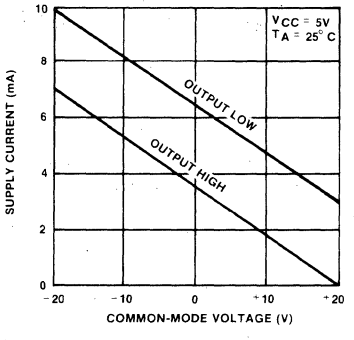
TERMINATION RESISTANCE



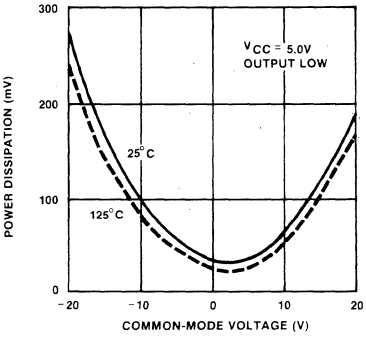
INPUT CHARACTERISTICS



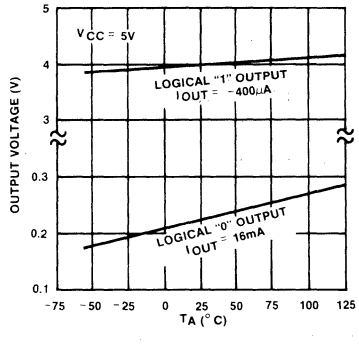
POWER SUPPLY CURRENT



INTERNAL POWER DISSIPATION



OUTPUT VOLTAGE LEVELS



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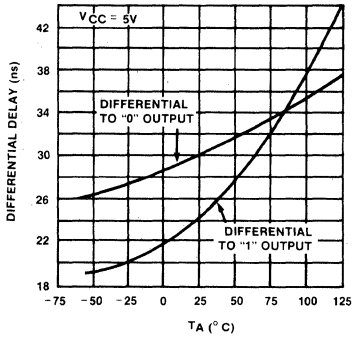
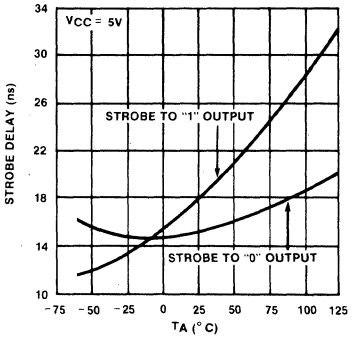
N/F

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

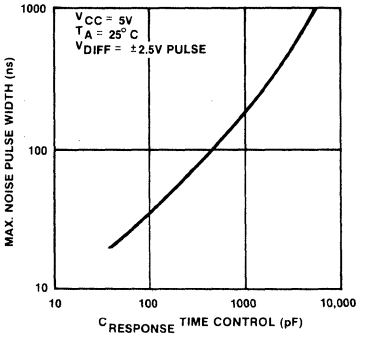
DIFFERENTIAL INPUT DELAYS



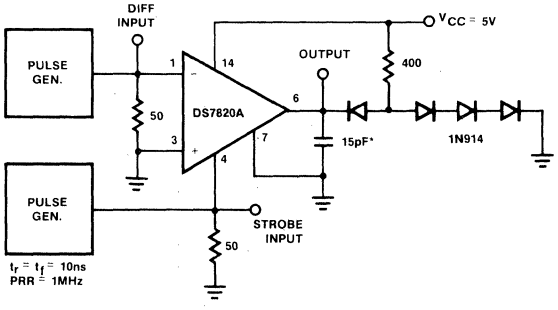
STROBE DELAYS



NOISE REJECTION

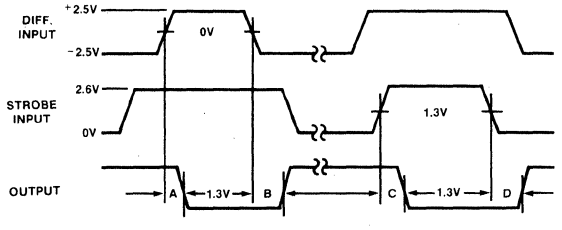


AC TEST CIRCUIT



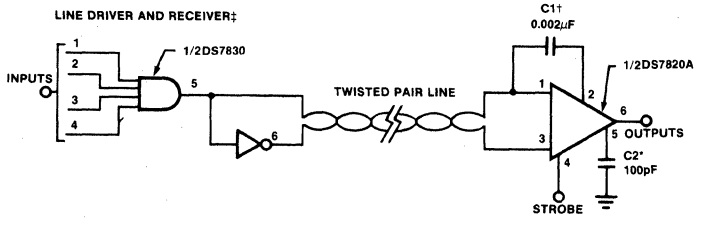
*Includes Jig and Probe

VOLTAGE WAVEFORM



A = Differential input to "0" output
B = Differential input to "1" output
C = Strobe input to "0" output
D = Strobe input to "1" output

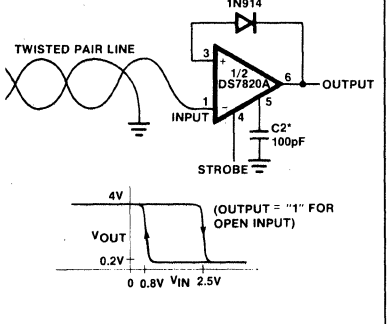
TYPICAL APPLICATIONS



NOTES

†Exact value depends on line length
‡V_{CC} is 4.5V to 5.5V for both the DS7820 and DS7830
*Optional to control response time

SINGLE ENDED (EIA-RS232C) RECEIVER WITH HYSTERESIS



DS7830/8830-F,N

DESCRIPTION

The DS7830/DS8830 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function.

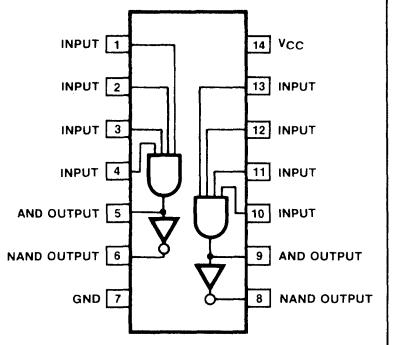
TTL (Transistor-Transistor-Logic) multiple emitter inputs allow this line driver to interface with standard TTL or DTL systems. The differential outputs are balanced and are designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines with characteristic impedances of 50Ω to 500Ω. The differential feature of the output eliminates troublesome ground-loop errors normally associated with single-wire transmissions.

FEATURES

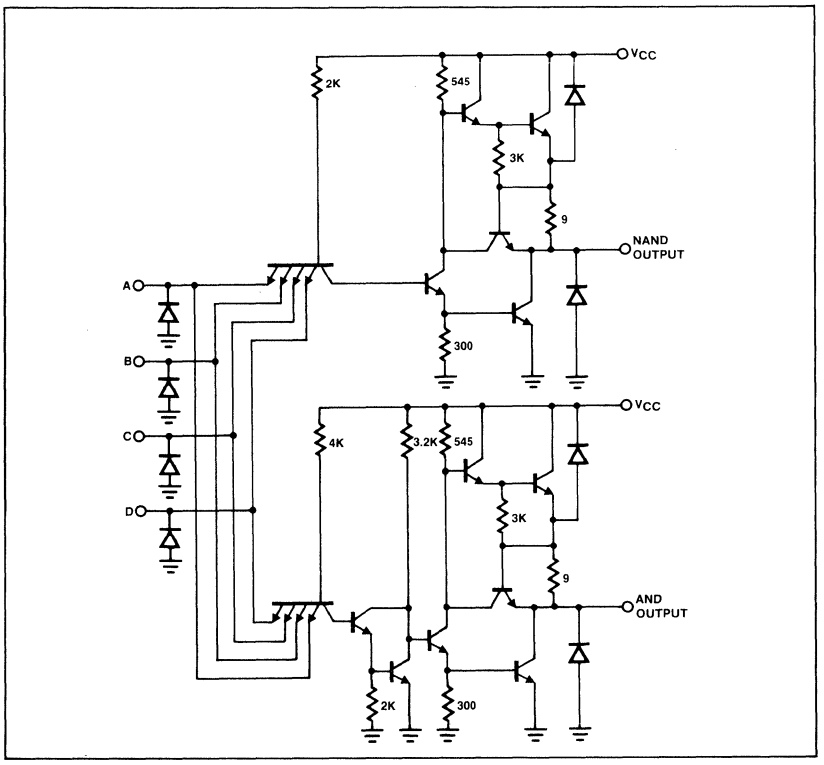
- **Single 5 volt power supply**
- **High speed**
- **Diode protected outputs for termination of positive and negative voltage transients**
- **Diode protected inputs to prevent line ringing**
- **Short circuit protection**
- **DS7830 Mil std 883A,B,C available**

PIN CONFIGURATION

F,N PACKAGE



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V_{CC}	7.0	V
Input voltage	5.5	V
Operating temperature range		
DS7830	-55 to +125	°C
DS8830	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

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DS7830/8830-F,N

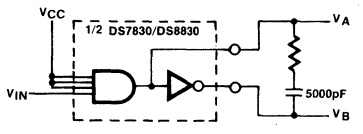
ELECTRICAL CHARACTERISTICS $T_A = 25°C$ $V_{CC} = 5V$ unless otherwise specified.[1,2]

PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
Logical "1" input voltage		2.0			V
Logical "0" input voltage				0.8	V
Logical "1" output voltage	$V_{IN} = 0.8V$ $I_{OUT} = -0.8mA$	2.4			V
Logical "1" output voltage	$V_{IN} = 0.8V$ $I_{OUT} = -40mA$	1.8	2.9		V
Logical "0" output voltage	$V_{IN} = 2.0V$ $I_{OUT} = +32mA$		0.2	0.4	V
Logical "0" output voltage	$V_{IN} = 2.0V$ $I_{OUT} = +40mA$		0.22	0.5	V
Logical "1" input current	$V_{IN} = +2.4V$			120	μA
Logical "1" input current	$V_{IN} = 5.5V$			2	mA
Logical "0" input current	$V_{IN} = 0.4V$			4.8	mA
Output short circuit current[2]	$V_{CC} = 5.0V$	-40	-100	-120	mA
Supply current	$V_{CC} = 5.0V$ $V_{IN} = 5.0V$ (Each driver)		11	18	mA
Propagation delay AND gate $t_{pd}1$	$T_A = 25°C$		8	12	ns
Propagation delay AND gate $t_{pd}0$	$V_{CC} = 5.0V$		11	18	ns
Propagation delay NAND gate $t_{pd}1$	$C_L = 15pF$		8	12	ns
Propagation delay NAND gate $t_{pd}0$	See Figure 1		5	8	ns
Differential delay t_1	Load, 100Ω and 5000pF		12	16	ns
Differential delay t_2	See Figure 2		12	16	ns

NOTES

1. Specifications apply for DS7830 $-55°C \le T_A \le +125°C$, $V_{CC} = +5V \pm 10\%$, DS8830 $0°C \le T_A \le 70°C$, $V_{CC} = +5V \pm 5\%$ unless otherwise specified.
2. Applies for $T_A = +125°C$, only one output at a time to be shorted.

AC TEST CIRCUIT



†V_{CC} is 4.5V to 5.5V for both the DS7820 and DS7830

†Exact value depends on transmission rate

*Optional to control response time

SWITCHING TIME WAVEFORMS

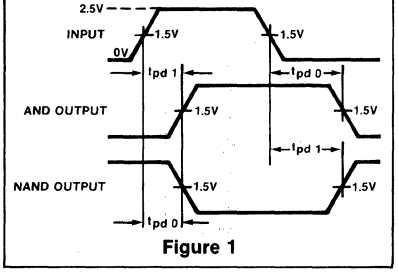


Figure 1

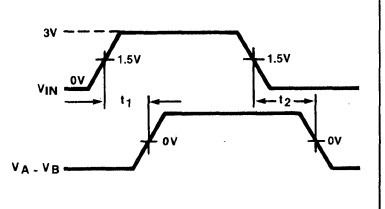
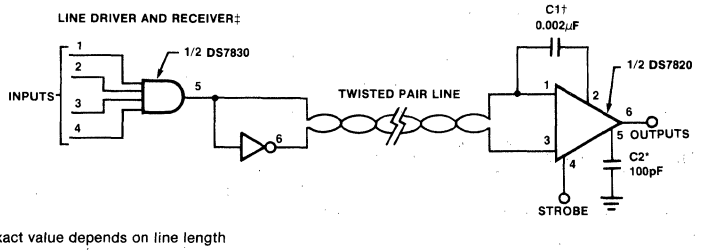


Figure 2

TYPICAL APPLICATION



†Exact value depends on line length

‡V_{CC} is 4.5V to 5.5V for the DS7820 and DS7830

*Optional to control response time

MC1488-F,N

DESCRIPTION

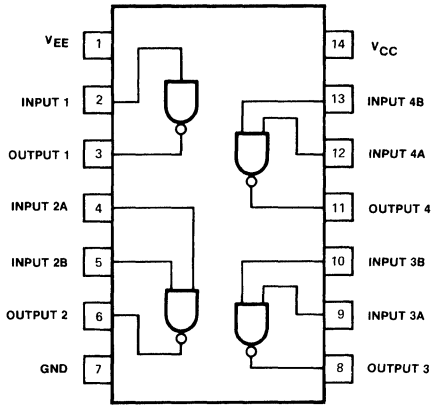
The MC1488 is a quad line driver which converts standard DTL/TTL input logic levels through one stage of inversion to output levels which meet EIA Standard No. RS-232C and CCITT Recommendation V.24.

FEATURES

- **Current limited output: ±10mA Typ**
- **Power-off source impedance: 300Ω Min**
- **Simple slew rate control with external capacitor**
- **Flexible operating supply range**
- **Inputs are DTL/TTL compatible**

PIN CONFIGURATION

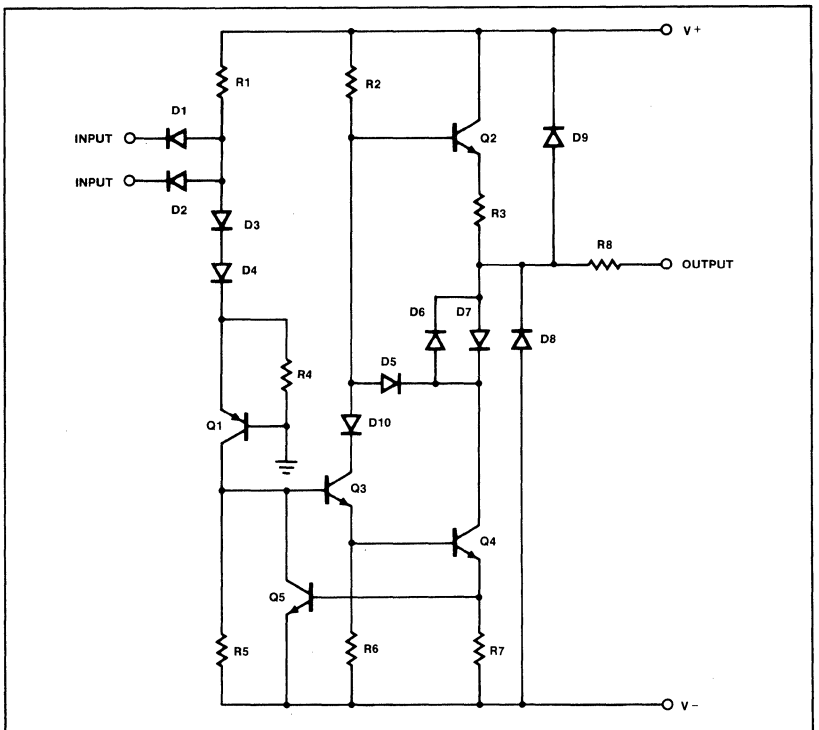
F,N PACKAGE



ORDER PART NO.

MC1488N/F

CIRCUIT SCHEMATIC



1/4 CIRCUIT

MC1488-F,N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage V+	+15	V
V-	-15	V
Input voltage (V_{IN})	$-15 \leq V_{IN} \leq 7.0$	V
Output voltage	±15	V
Power dissipation:		
F package	1000	mW
N package	800	mW
Operating temperature range	0 to +75	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

DC ELECTRICAL CHARACTERISTICS

V+ = +9.0V ± 1%, V- = -9.0V ± 1%, T_A = 0°C to +75°C unless otherwise specified.
All typicals are for V+ = 9.0V, V- = -9.0V, and T_A = 25°C.*

PARAMETER	TEST CONDITIONS		LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
Logic "0" input current	V_{IN} = 0V			-1.0	-1.6	mA
Logic "1" input current	V_{IN} = +5.0V			.005	10.0	μA
High level output voltage	R_L = 3.0kΩ, V_{IN} = 0.8V	V+ = 9.0V, V- = -9.0V	6.0	7.0		V
		V+ = 13.2V, V- = -13.2V	9.0	10.5		V
Low level output voltage	R_L = 3.0kΩ, V_{IN} = 1.9V	V+ = 9.0V, V- = -9.0V	-6.0	-6.8		V
		V+ = 13.2V, V- = -13.2V	-9.0	-10.5		V
High level output Short-circuit current	V_{OUT} = 0V, V_{IN} = 0.8V		-6.0	-10.0	-12.0	mA
Low level output Short-circuit current	V_{OUT} = 0V, V_{IN} = 1.9V		6.0	10.0	12.0	mA
Output resistance	V+ = V- = 0V, V_{OUT} = ±2V		300			Ω
Positive supply current (output open)	V_{IN} = 1.9V	V+ = 9.0V, V- = -9.0V		15.0	20.0	mA
		V+ = 12V, V- = -12V		19.0	25.0	mA
		V+ = 15V, V- = -15V		25.0	34.0	mA
	V_{IN} = 0.8V	V+ = 9.0V, V- = -9.0V		4.5	6.0	mA
		V+ = 12V, V- = -12V		5.5	7.0	mA
		V+ = 15V, V- = -15V		8.0	12.0	mA
Negative supply current (output open)	V_{IN} = 1.9V	V+ = 9.0V, V- = -9.0V		-13.0	-17.0	mA
		V+ = 12V, V- = -12V		-18.0	-23.0	mA
		V+ = 15V, V- = -15V		-25.0	-34.0	mA
	V_{IN} = 0.8V	V+ = 9.0V, V- = -9.0V		-1	-15	μA
		V+ = 12V, V- = -12V		-1	-15	μA
		V+ = 15V, V- = -15V		-.01	-2.5	mA
Power dissipation	V+ = 9.0V, V- = -9.0V			252	333	mW
	V+ = 12V, V- = -12V			444	576	mW
Propagation delay to "1" (t_{pd1})	R_L = 3.0kΩ, C_L = 15pF, T_A = 25°C			275	350	ns
Propagation delay to "0" (t_{pd0})	R_L = 3.0kΩ, C_L = 15pF, T_A = 25°C			70	175	ns
Rise time (t_r)	R_L = 3.0kΩ, C_L = 15pF, T_A = 25°C			75	100	ns
Fall time (t_f)	R_L = 3.0kΩ, C_L = 15pF, T_A = 25°C			40	75	ns

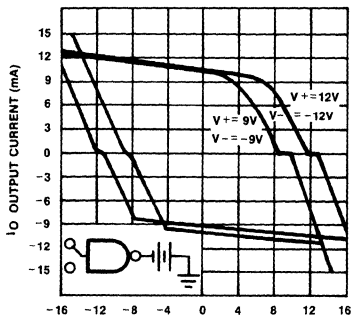
NOTE

*Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.

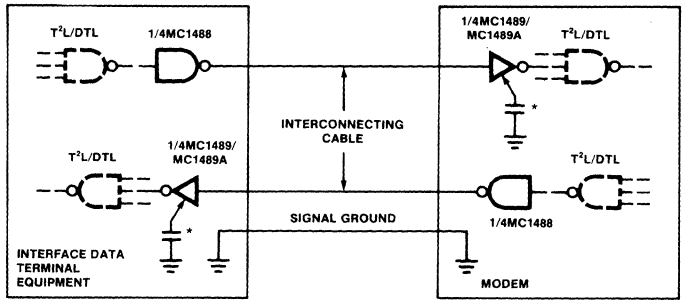
MC1488-F,N

TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT VOLTAGE AND CURRENT-LIMITING CHARACTERISTICS



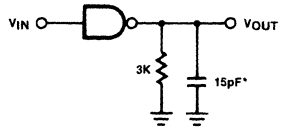
RS232C DATA TRANSMISSION



NOTE

*Optional for noise filtering

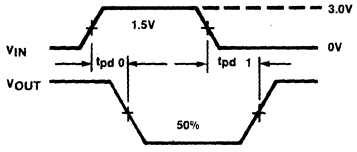
AC LOAD CIRCUIT



NOTE

*C_L includes probe and jig capacitance.

SWITCHING WAVEFORMS



NOTE

t_r and t_f are measured between 10% and 90% of the output waveform

APPLICATIONS

By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current limiting characteristics of the MC1488. For a set slew rate the appropriate capacitor value may be calculated using the following relationship

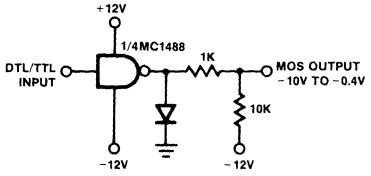
$$C = I_{SC}\,(\Delta T/\Delta V)$$

where C is the required capacitor, I_{SC} is the short circuit current value, and $\Delta V/\Delta T$ is the slew rate.

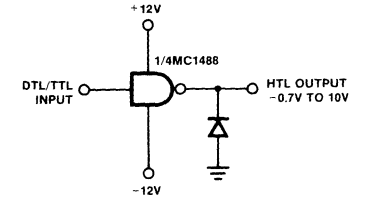
RS232C specifies that the output slew rate must not exceed 30V per microsecond. Using the worst case output short circuit current of 12mA in the above equation, calculations result in a required capacitor of 400pF connected to each output.

TYPICAL APPLICATIONS

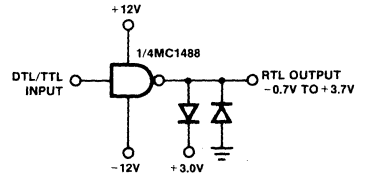
DTL/TTL-TO-MOS TRANSLATOR



DTL/TTL-TO-HTL TRANSLATOR



DTL/TTL-TO-RTL TRANSLATOR



7

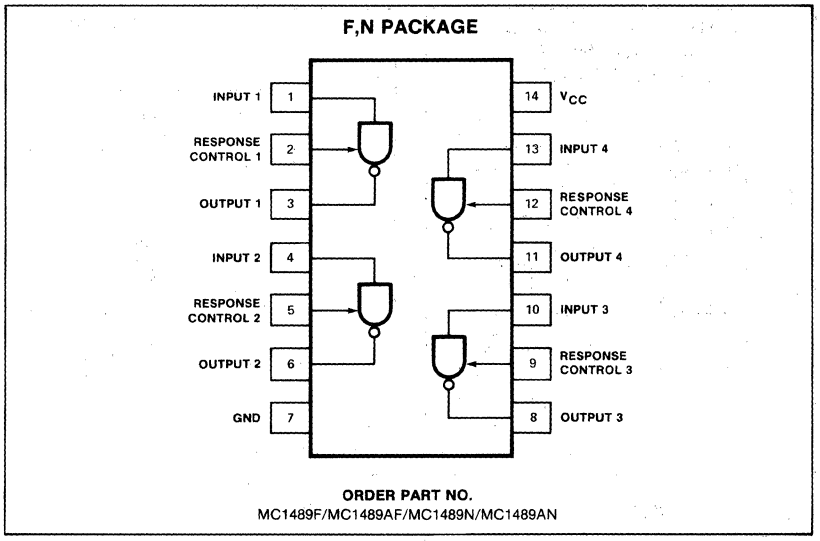
DESCRIPTION

The MC1489/MC1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA standard No. RS232C.

FEATURES

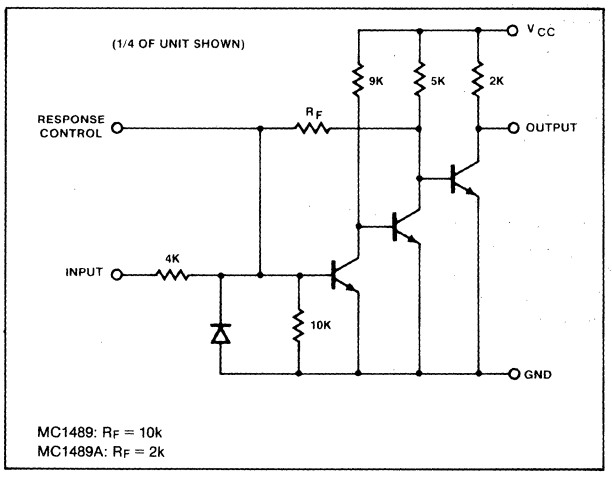
- **Four totally separate receivers per package**
- **Programmable threshold**
- **Built-in input threshold hysteresis**
- **"Fail safe" operating mode**
- **Inputs withstand ±30V**

PIN CONFIGURATION



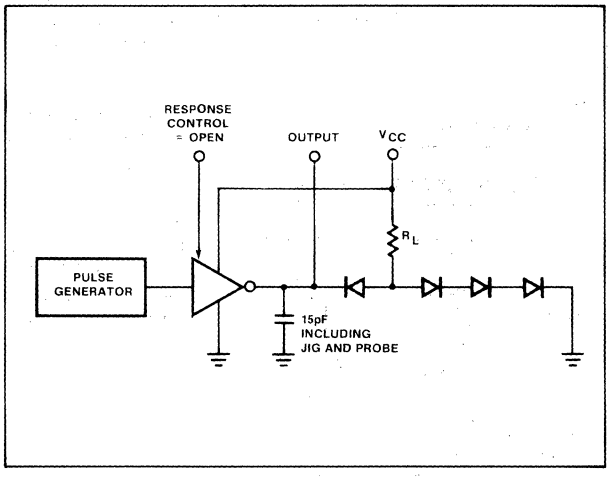
ORDER PART NO.
MC1489F/MC1489AF/MC1489N/MC1489AN

EQUIVALENT SCHEMATIC



MC1489: R_F = 10k
MC1489A: R_F = 2k

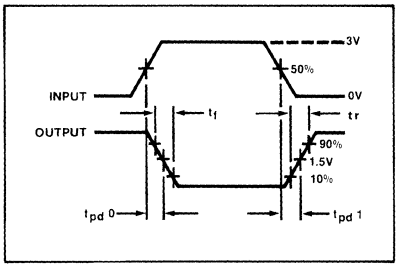
AC TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Power supply voltage	10	V
Input voltage range	±30	V
Output load current	20	mA
Power dissipation:		
F package	1	W
N package	800	mW
Operating temperature range	0 to +75	°C
Storage temperature range	-65 to +150	°C

VOLTAGE WAVEFORMS



DC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ± 1%, 0°C ≤ T_A ≤ +75°C unless otherwise specified.[1,2]

PARAMETER	TEST CONDITIONS	MC1489			MC1489A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input high threshold voltage	T_A = 25°C, V_{OUT} ≤ 0.45V, I_{OUT} = 10mA	1.0		1.5	1.75		2.25	V
Input low threshold voltage	T_A = 25°C, V_{OUT} ≤ 2.5V, I_{OUT} = -0.5mA	0.75		1.25	0.75		1.25	V
	V_{IN} = +25V	+3.6	+5.6	+8.3	+3.6	+5.6	+8.3	mA
	V_{IN} = -25V	-3.6	-5.6	-8.3	-3.6	-5.6	-8.3	
Input current	V_{IN} = +3V	+0.43	+0.53		+0.43	+0.53		mA
	V_{IN} = -3V	-0.43	-0.53		-0.43	-0.53		
Output high voltage	V_{IN} = 0.75V, I_{OUT} = -0.5mA	2.6	3.8	5.0	2.6	3.8	5.0	V
	Input = Open, I_{OUT} = -0.5mA	2.6	3.8	5.0	2.6	3.8	5.0	V
Output low voltage	V_{IN} = 3.0V, I_{OUT} = 10mA		0.33	0.45		0.33	0.45	V
Output short circuit current	V_{IN} = 0.75V		3.0			3.0		mA
Supply current	V_{IN} = 5.0V		20	26		20	26	mA
Power dissipation	V_{IN} = 5.0V		100	130		100	130	mW

NOTES

1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for response control pin = open.

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ± 1%, T_A = 25°C unless otherwise specified.[1,2]

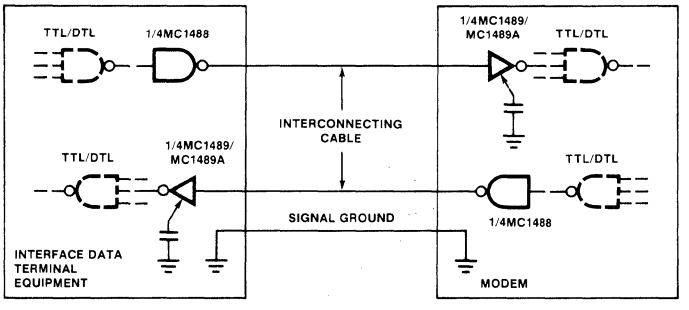
PARAMETER	TEST CONDITIONS	MC1489			MC1489A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input to output "high" Propagation delay (t_{pd1})	R_L = 3.9kΩ (AC test circuit)		25	85		25	85	ns
Input to output "low" Propagation delay (t_{pd0})	R_L = 390Ω (AC test circuit)		20	50		20	50	ns
Output rise time	R_L = 3.9kΩ (AC test circuit)		110	175		110	175	ns
Output fall time	R_L = 390Ω (AC test circuit)		9	20		9	20	ns

NOTES

1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for response control pin = open.

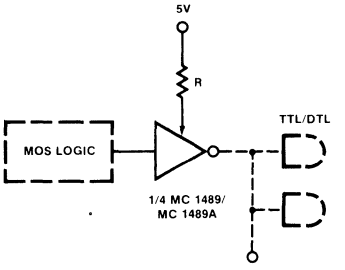
TYPICAL APPLICATIONS

RS232C DATA TRANSMISSION



*Optional for noise filtering

MOS TO TTL/DTL TRANSLATOR



DESCRIPTION

The UDN 5711 series of dual peripheral drivers have high voltage (80V) and high current (300mA) NPN output transistors. In addition an overshoot clamp diode is provided for each output collector for use when switching inductive loads.

A choice of AND, NAND, OR and NOR logic functions comprise the four device types in the series.

In use care must be taken to insure that the absolute maximum junction temperature rating is not exceeded due to excessive power dissipation; particularly when switching capacitive or inductive loads at high frequencies.

FEATURES

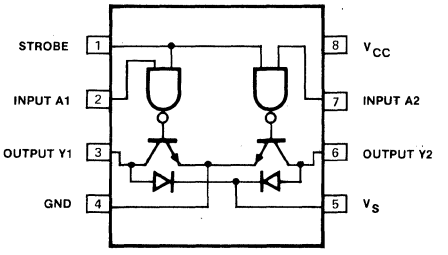
- **Four logic functions**
- **DTL/TTL/PMOS/CMOS compatible inputs**
- **Low input current loading**
- **80V output breakdown**

APPLICATIONS

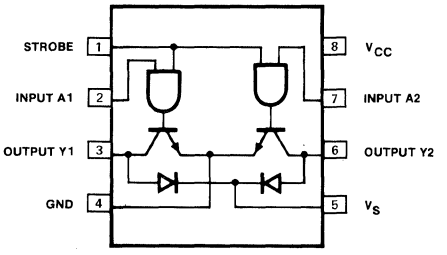
- **Relay drivers**
- **Lamp drivers**
- **LED drivers**
- **High current triac trigger**

PIN CONFIGURATIONS

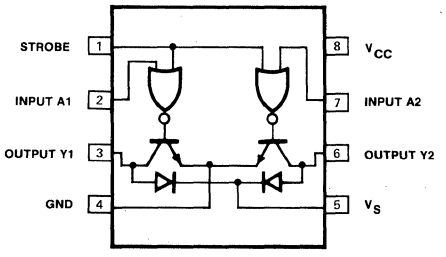
DUAL AND DRIVER
UDN 5711



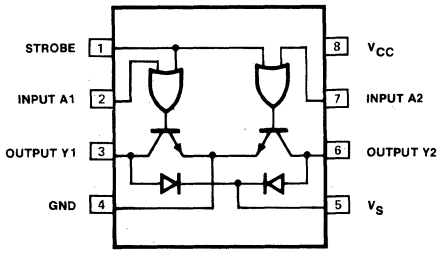
DUAL NAND DRIVER
UDN 5712



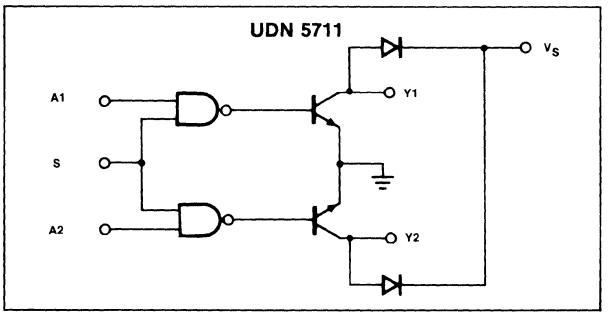
DUAL OR DRIVER
UDN 5713

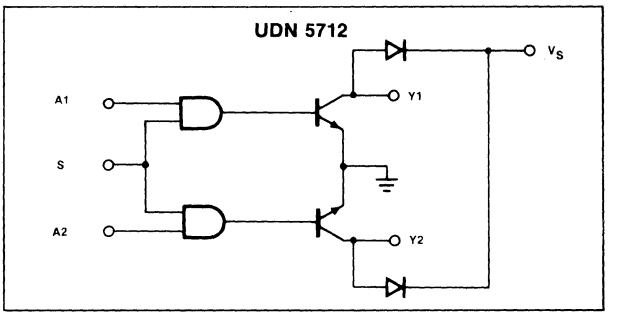


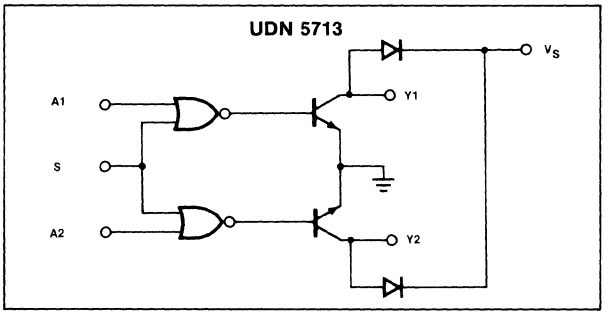
DUAL NOR DRIVER
UDN 5714

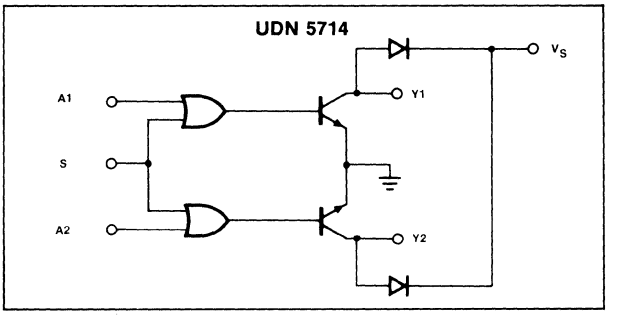


BLOCK DIAGRAMS

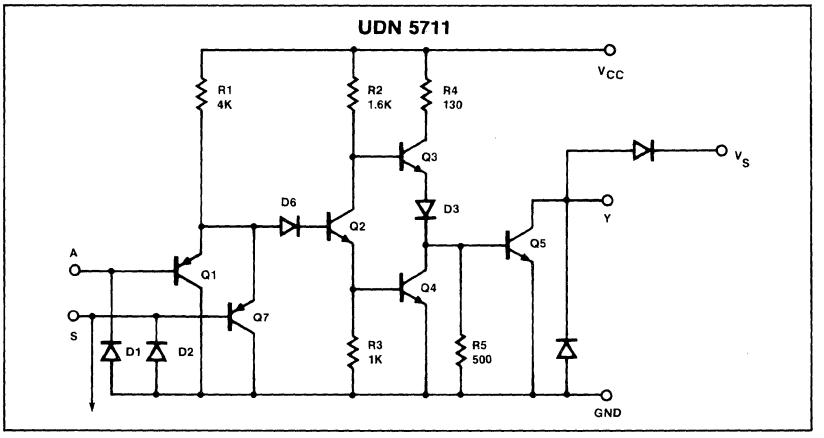


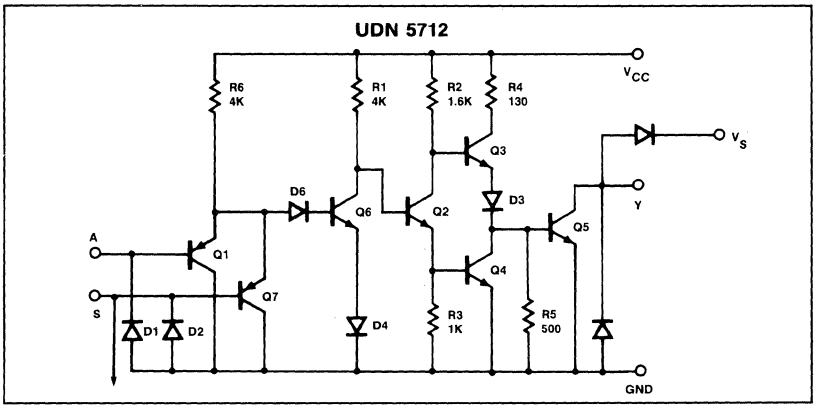




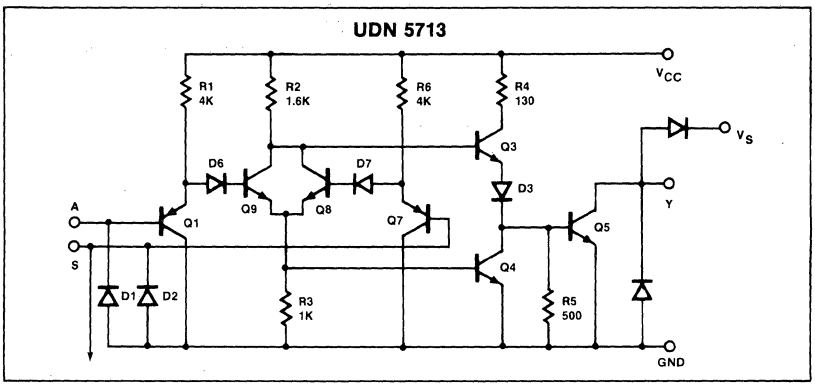


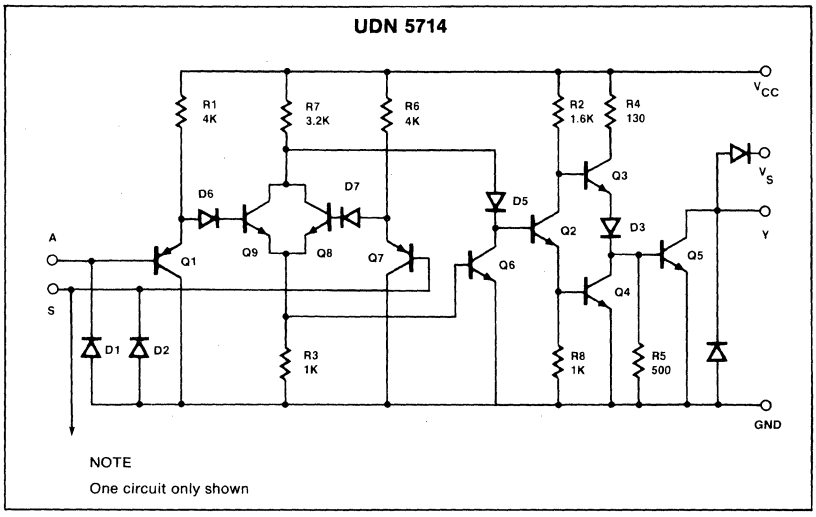
EQUIVALENT CIRCUIT





EQUIVALENT CIRCUIT (Cont'd)





NOTE

One circuit only shown

ABSOLUTE MAXIMUM RATINGS at 25°C unless otherwise stated.

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage		
	Continuous	7	V
	Momentary (1 second)	15	V
V_{IN}	Input voltage	30	V
V_{OUT}	Output voltage (off state)	80	V
I_{OUT}	Output current	600	mA
V_S	Suppression diode reverse voltage	80	V
I_S	Suppression diode forward current	600	mA
P_D	Power dissipation*	750	mW
T_A	Operating temperature range	0 to 70	°C
T_{stg}	Storage temperature range	-65 to 150	°C
	Lead soldering temperature (10 seconds)	300	°C

NOTE

*The maximum junction is 150°C. Derate at 162°C/watt above 25°C.

DC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 85°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage range		4.75	5.00	5.25	V
V_{IH}	Logical "1" input voltage	V_{CC} = 4.75V	2.0			V
V_{IL}	Logical "0" input voltage	V_{CC} = 4.75V			0.8	V
V_I	Input clamp voltage	V_{CC} = 4.75V, T_A = 25°C, I_I = -12mA		-1.2	-1.5	V
I_{IH}	Logical "1" input current except stobe	V_{CC} = 5.25V, V_{IN} = 30V V_{strobe} = 0V		1	10	μA
I_{IH}	Logical "1" input current at strobe	V_{CC} = 5.25V, V_{strobe}= 30V V_{IN} = 0V		2	20	μA
I_{IL}	Logical "0" input current except strobe	V_{CC} = 5.25V, V_{IN} = 0.4V V_{strobe} = 30V		-50	-100	μA
I_{IL}	Logical "0" input current at strobe	V_{CC} = 5.25V, V_{strobe} = 0.4V V_{IN} = 30V		-100	-200	μA
I_{OUT}	Output current	UDN 5711/5713 - V_{IN} = 0.8V UDN 5712/5714 - V_{IN} = 2.0V			300	mA
I_{OH}	Output leakage current	V_{IN} = 2.0V (UDN 5711/5713) V_{IN} = 0.8V (UDN 5712/5714) V_{OH} = 80V, V_{CC} = 5.25V V_{CC} = open			100 100	μA μA
V_{OL}	Output low voltage	V_{IN} = 0.8V (UDN 5711/5713) V_{IN} = 2.0V (UDN 5712/5714) V_{CC} = 4.75V, I_{OL} = 150mA I_{OL} = 300mA		0.35 0.50	0.50 0.70	V V
I_{LD}	Diode leakage current	V_{IN} = 0V (UDN 5711/5713) V_{IN} = 5V (UDN 5712/5714) V_{CC} = 5V, V_{LD} = 80V, T_A = 25°C			200	μA
V_{FD}	Diode forward voltage	I_{FD} = 300mA, T_A = 25°C		1.5	1.75	V
I_{CCH}	Supply current with outputs high	V_{CC} = 5.25V, T_A = 25°C UDN 5711 V_{IN} = 5V UDN 5712 V_{IN} = 0V UDN 5713 V_{IN} = 5V UDN 5714 V_{IN} = 0V		 8 12 8 12	 12 15 13 15	 mA mA mA mA
I_{CCL}	Supply current with outputs low	V_{CC} = 5.25V, T_A = 25°C UDN 5711 V_{IN} = 0V UDN 5712 V_{IN} = 5V UDN 5713 V_{IN} = 0V UDN 5714 V_{IN} = 5V		 35 40 36 40	 49 53 50 50	 mA mA mA mA

AC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
T_{PLH}	Propagation delay time, low-to-high output	V_S = 70V, R_L = 465Ω C_L = 15pF			500	ns
T_{PHL}	Propagation delay time, high-to-low output	V_S = 70V, R_L = 465Ω C_L = 15pF			750	ns

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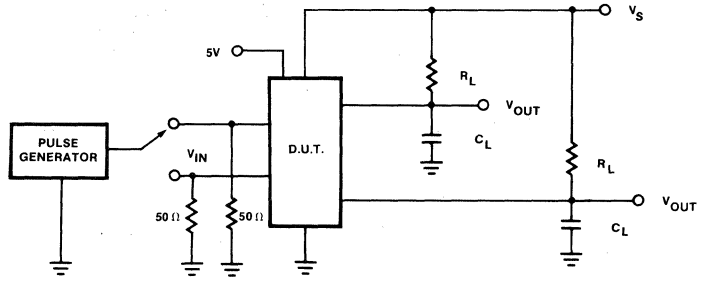
TEST LOAD CIRCUITS

PROPAGATION DELAY MEASUREMENT

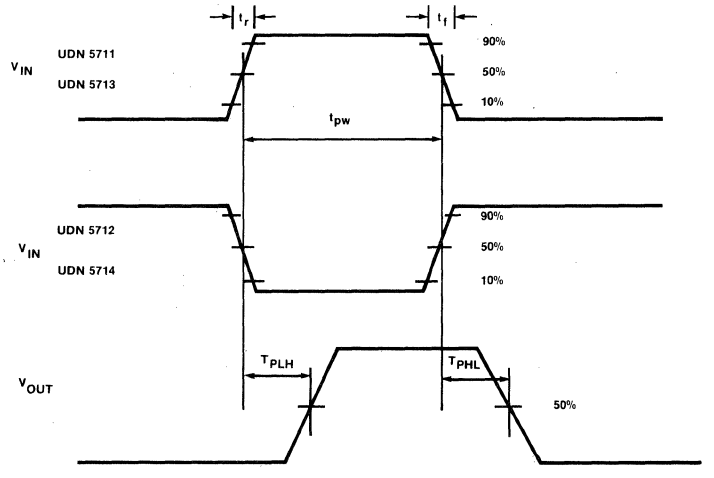


NOTES

1. C_L includes probe and jig capacitances.
2. Unused inputs held at 2.4V.

VOLTAGE WAVEFORMS

PROPAGATION DELAY MEASUREMENT



V_{IL} = 0V
V_{IH} = 3.5V
t_r = 14ns
t_f = 7ns

P_{RR} = 500kHz
T_{PW} = 1μs

75S107-F,N

DESCRIPTION

The 75S107 is a high speed dual line receiver that is functionally equivalent and pin compatible to the SN75107A. If features less than 17ns propagation delay without sacrificing input performance characteristics. This is accomplished through the utilization of Schottky technology.

The 75S107 maintains ±3V common mode voltage range, 7.5mV input offset voltage and 5μA offset current. It also features STTL compatible output levels with a minimum sink/source capability of 10 Schottky gate loads.

FEATURES

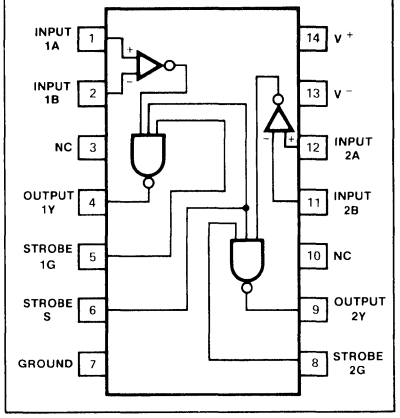
- **Functionally equivalent and pin compatible to SN75107A**
- **17ns maximum guaranteed propagation delay**
- **20μA maximum input bias current**
- **STTL compatible strobes and outputs**
- **Large common mode input voltage range**
- **Operates from standard supply voltages**

APPLICATIONS

- **MOS memory sense amp**
- **A/D conversion**
- **High speed line receiver**

PIN CONFIGURATION

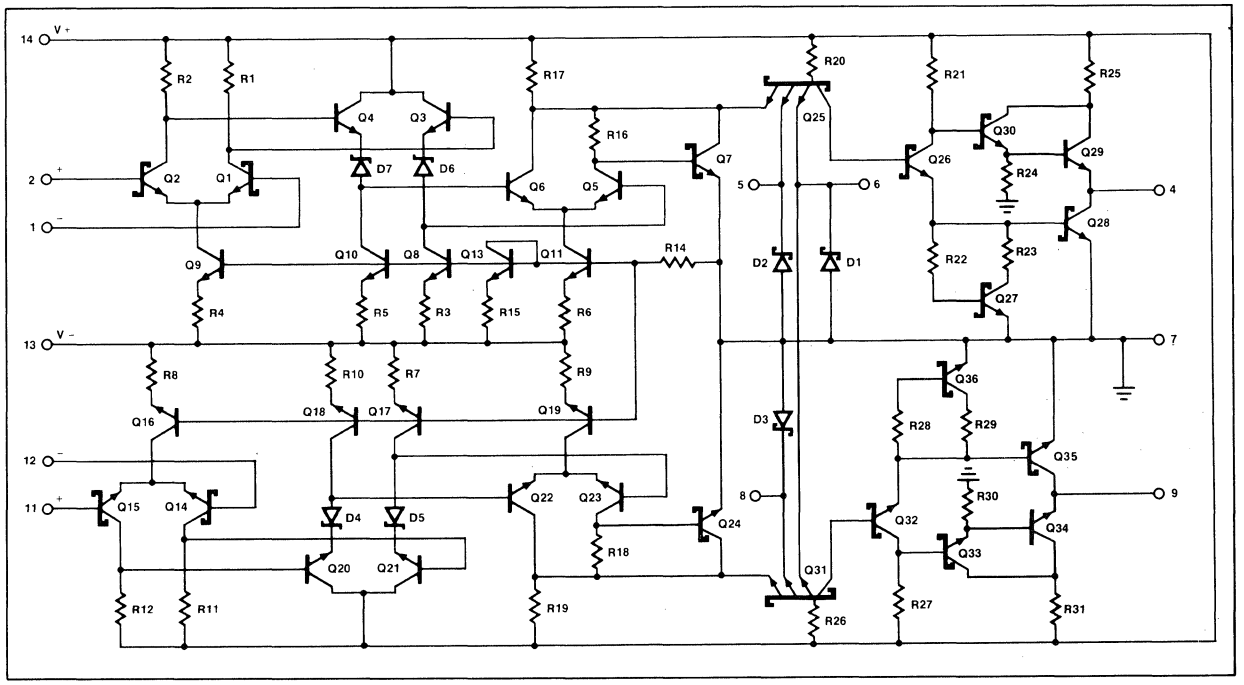
F,N PACKAGE



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V+)	+7	V
Negative supply voltage (V-)	-7	V
Differential input voltage	±6	V
Common mode input voltage	±5	V
Strobe/gate input voltage	+5.5	V
Power dissipation	600	mW
Operating temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 60sec)	+300	°C

EQUIVALENT SCHEMATIC



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ELECTRICAL CHARACTERISTICS T_A = 0 to +70°C, V+ = +5.00, V- = -5.00 unless otherwise specified.

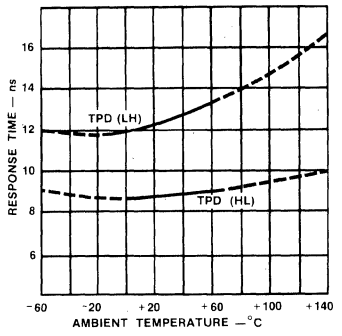
PARAMETER		TEST CONDITIONS	75S107			UNIT
			Min	Typ	Max	
AMPLIFIER INPUT						
	Input offset voltage	V+ = 4.75, V- = -4.75			25	mV
	Input bias current @ 25°C	V+ = 5.25, V- = -5.25		7.5	20	μA
	over temp. range	V+ = 5.25, V- = -5.25			40	μA
	Input offset current @ 25°C	V+ = 5.25, V- = -5.25		1.0	5	μA
	over temp. range	V+ = 5.25, V- = -5.25			12	μA
	Input common mode voltage range	V+ = 4.75, V- = -4.75	±3			V
	Input resistance			4		kΩ
	Input capacitance			3	6	pF
	Voltage gain			5		V/mV
SCHOTTKY GATE/OUTPUT CHARACTERISTICS						
I_{IH}	High level input current into 1G or 2G strobe	V+ = 5.25, V- = -5.25				
		V_{IH} = 2.7V			50	μA
		V_{IH} = 5.5V			1	mA
I_{IH}	High level input current into common strobe S	V+ = 5.25, V- = -5.25				
		V_{IH} = 2.7V			100	μA
		V_{IH} = 5.5V			2	mA
I_{IL}	Low level input current into 1G or 2G	V+ = 5.25, V- = -5.25			-2.0	mA
		V_{IL} = 0.5V				
I_{IL}	Low level input current into common strobe S	V+ = 5.25, V- = -5.25			-4.0	mA
		V_{IL} = 0.5V				
V_{OH}	High level output voltage	V+ = 4.75V, $V_{I(S)}$ = 2.0V	2.7	3.4		V
		V- = -4.75V				
		I_{LOAD} = -1mA				
V_{OL}	Low level output voltage	V+ = 4.75			0.5	V
		V- = -4.75				
		I_{LOAD} = 20mA				
		$V_{I(S)}$ = 2.0V				
POWER SUPPLY REQUIREMENTS						
	Supply voltage					
V+			4.75	5.00	5.25	V
V-			-4.75	-5.00	-5.25	V
I_{CC}+	Supply current	V+ = 5.25V		20	30	mA
I_{CC}-		V- = -5.25V		-11	-15	mA
		T_A = 25°C				
I_{OS}	Short circuit	V+ = +5.25	-40		-100	mA
	output current	V- = -5.25				
LARGE SIGNAL SWITCHING SPEED						
T_pLH (D)	Low to high propagation delay from amp	R_L = 280Ω C_L = 15pF		12	17	ns
	inputs to output[1]	T_A = 25°C				
T_pHL (D)	High to low propagation delay from amps	R_L = 280Ω C_L = 15pF		9	13	ns
	inputs to output[1]	T_A = 25°C				
T_pLH (S)	Low to high propagation delay from strobes	R_L = 280Ω C_L = 15pF		4.5	6	ns
	input to output[2]	T_A = 25°C				
T_pHL (S)	High to low propagation delay strobe	R_L = 280Ω C_L = 15pF		3.0	4.5	ns
	input to output[2]	T_A = 25°C				
	Maximum operating frequency	R_L = 280Ω C_L = 15pF	40	55		MHz
		T_A = 25°C				

NOTES

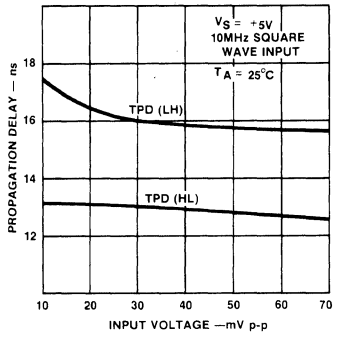
1. Response time measured from 0V point of ±100mV$_{P-P}$ 10MHz square wave to the 1.5 point of the output.
2. Response time measured from 1.5V point to input to 1.5V point of output.
3. Response time measured from the start of a 100mV input step with 5mV overdrive to the 1.5V point of the output.

TYPICAL PERFORMANCE CHARACTERISTICS

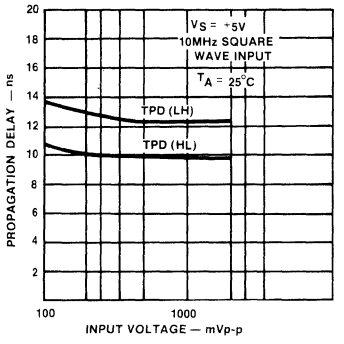
RESPONSE TIME vs TEMPERATURE



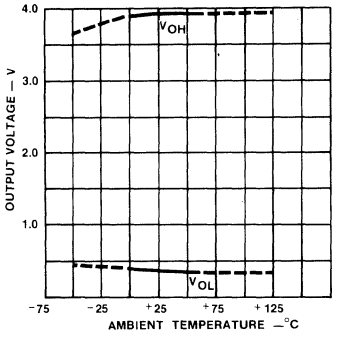
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



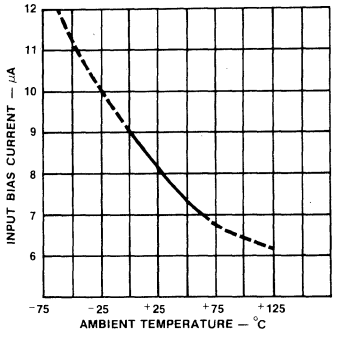
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



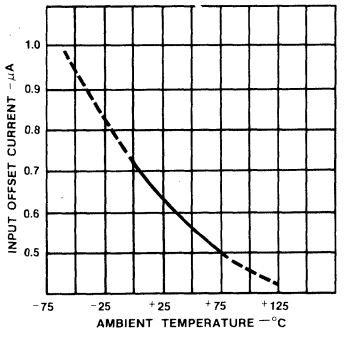
OUTPUT VOLTAGE vs AMBIENT TEMPERATURE



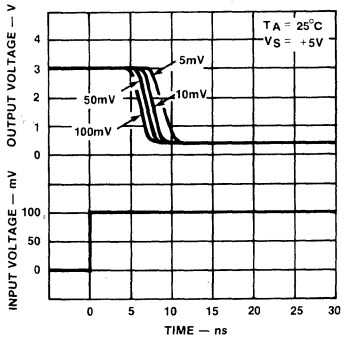
INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



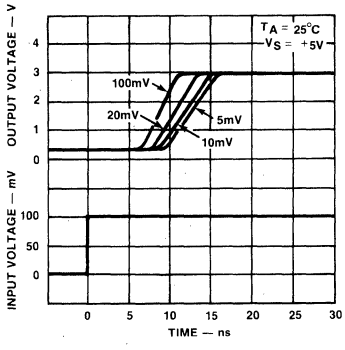
INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



75S108-F,N

DESCRIPTION

The 75S108 is a high speed dual line receiver that is functionally equivalent and pin compatible to the SN75108N. It features less than 17ns propagation delay without sacrificing input performance characteristics. This is accomplished through the utilization of Schottky technology.

The 75S108 maintains ±3V common mode voltage range, 7.5mV input offset voltage and 5μA offset current. It also features STTL compatible output levels with an open collector configuration for wired-AND logic applications.

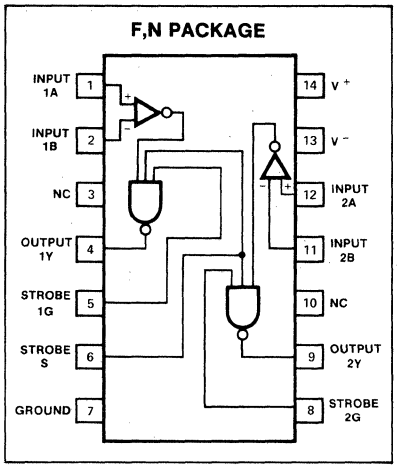
FEATURES

- **Functionally equivalent and pin compatible to SN75108A**
- **17ns maximum guaranteed propagation delay**
- **20μA maximum input bias current**
- **TTL compatible strobes and outputs**
- **Open collector outputs**
- **Large common mode input voltage range**
- **Operates from standard supply voltages**

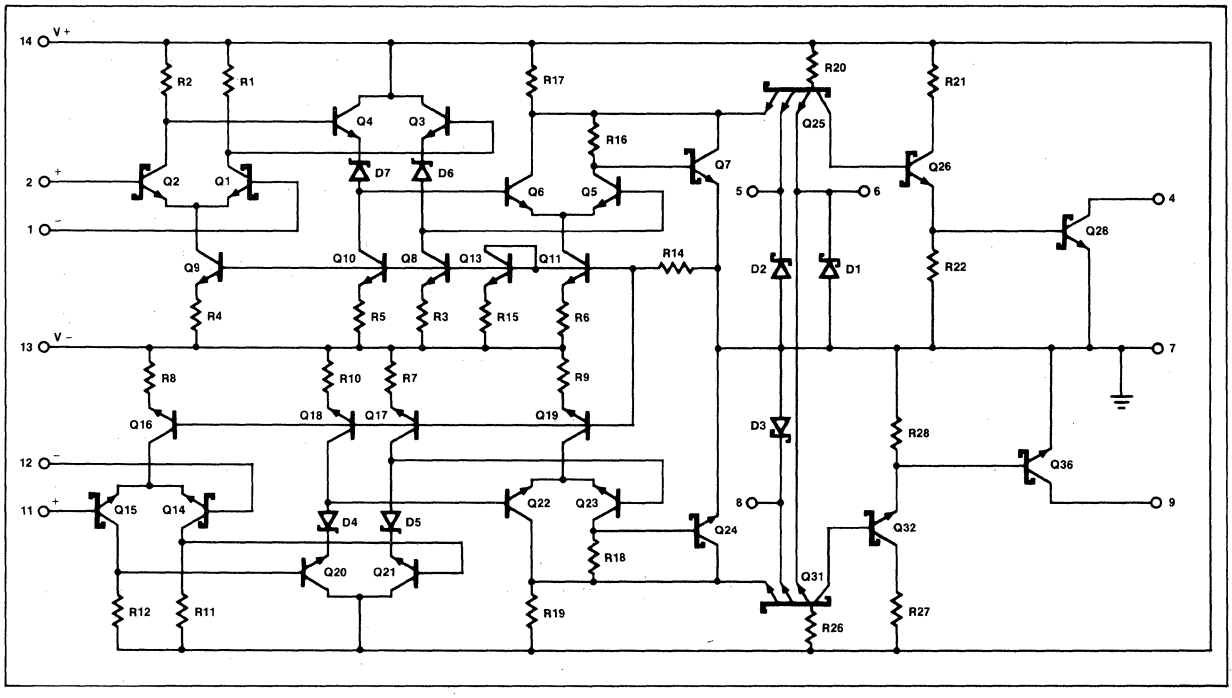
APPLICATIONS

- **High speed line receiver**
- **MOS memory sense amp**
- **A/D conversion**

PIN CONFIGURATION



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V+)	+7	V
Negative supply voltage (V-)	-7	V
Differential input voltage	±6	V
Common mode input voltage	±5	V
Strobe gate input voltage	+5.5	V
Power dissipation	600	mW
Operating temperature range	0 to 70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 60 sec)	+300	°C

75S108-F,N

ELECTRICAL CHARACTERISTICS T_A = 0 to 70°C, V+ = +5.00, V- = -5.00 unless otherwise specified.

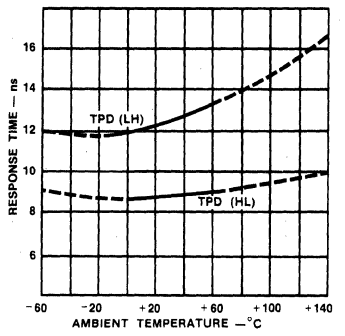
PARAMETER	TEST CONDITIONS	75S108			UNIT
		Min	Typ	Max	
AMPLIFIER INPUT Input offset voltage	V+ = 4.75, V- = -4.75			25	mV
Input bias current @ 25°C over temp range	V+ = 5.25, V- = -5.25 V+ = 5.25, V- = -5.25		7.5	20 40	μA μA
Input offset current @ 25°C over temp range	V+ = 5.25, V- = -5.25 V+ = 5.25, V- = -5.25		1.0	5 12	μA μA
Input common mode voltage range Input resistance Input capacitance	V+ = 4.75, V- = -4.75	±3	 4 3	±3 6	V kΩ pF
Voltage gain			5		V/mV
SCHOTTKY GATE/OUTPUT CHARACTERISTICS I_{IH} High level input current into 1G or 2G strobe	V+ = 5.25, V- = -5.25 V_{IH} = 2.7V V_{IH} = 5.5V			 50 1	 μA mA
I_{IH} High level input current into common strobe S	V+ = 5.25, V- = -5.25 V_{IH} = 2.7V V_{IH} = 5.5V			 100 2	 μA mA
I_{IL} Low level input current into 1G or 2G	V+ = 5.25, V- = -5.25 V_{IL} = 0.5V			-2.0	mA
I_{IL} Low level input current into common strobe S	V+ = 5.25, V- = -5.25 V_{IL} = 0.5V			-4.0	mA
V_{OL} Low level output voltage	V+ = 4.75, $V_{I(S)}$ = 2.0V V- = -4.75 I_{LOAD} = 20mA			0.5	V
I_{OH} High level output current	V_{CC}+ = 5.25V V_{CC}- = -5.25V V_{OH} = 5.25V			250	μA
POWER SUPPLY REQUIREMENTS Supply voltage V+ V-		 4.75 -4.75	 5.00 -5.00	 5.25 -5.25	 V V
Supply current	V+ = 5.25V V- = -5.25V T_A = 25°C				
I_{CC}+ I_{CC}-			20 -11	30 -15	mA mA
LARGE SIGNAL SWITCHING SPEED T_pLH (D) Low to high propagation delay from amp inputs to output[1]	R_L = 280Ω C_L = 15pF T_A = 25°C		12	17	ns
T_pHL (D) High to low propagation delay from amp inputs to output[1]	R_L = 280Ω C_L = 15pF T_A = 25°C		9	13	ns
T_pLH (S) Low to high propagation delay from strobes input to output[2]	R_L = 280Ω C_L = 15pF T_A 25°C		6	10	ns
T_pHL (S) High to low propagation delay strobe input to output[2]	R_L = 280Ω C_L = 15pF T_A = 25°C		5	8	ns
Maximum operating frequency	R_L = 280Ω C_L = 15pF T_A = 25°C	25	35		MHz

NOTES:

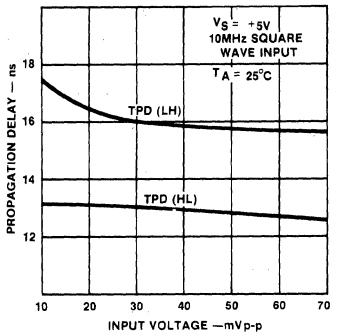
1. Response time measured from 0V point of ±100 mV_{P-P} 10MHz square wave to the 1.5 point of the output.
2. Response time measured from 1.5V point of input to 1.5V point of output.
3. Response time measured from the start of a 100mV input step with 5mV overdrive to the 1.5V point of the output.

TYPICAL PERFORMANCE CHARACTERISTICS

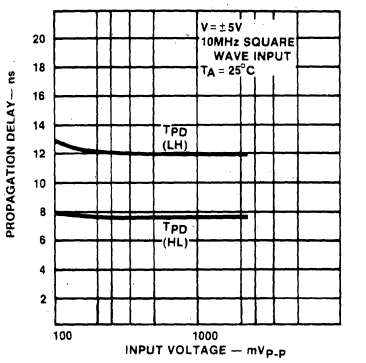
RESPONSE TIME vs TEMPERATURE



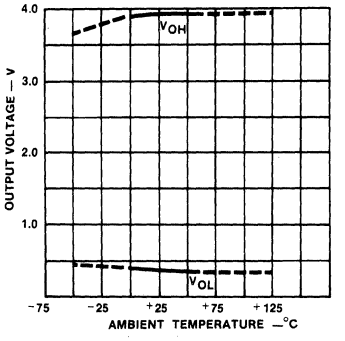
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGE



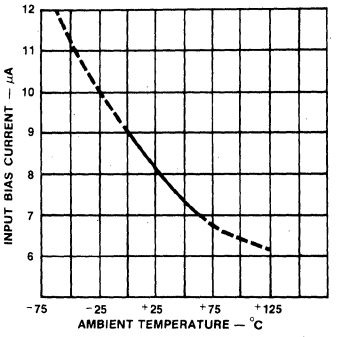
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGE



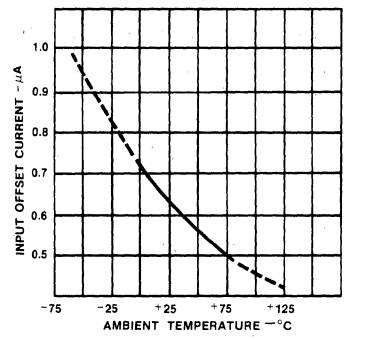
OUTPUT VOLTAGE vs AMBIENT TEMPERATURE



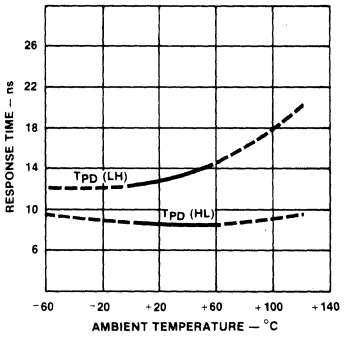
INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



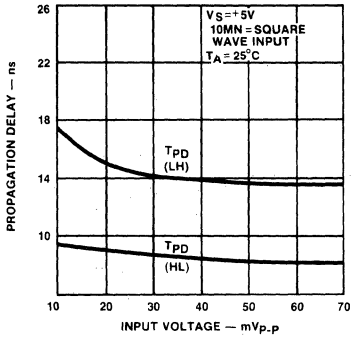
INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE



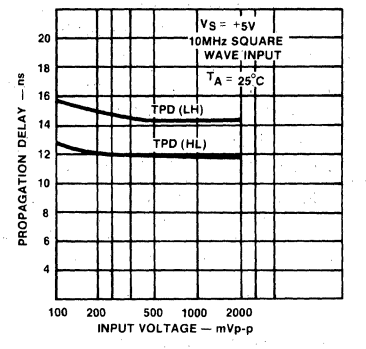
RESPONSE TIME vs TEMPERATURE



PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES

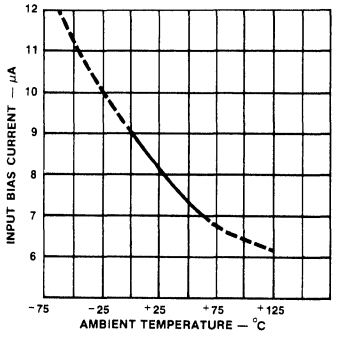


PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES

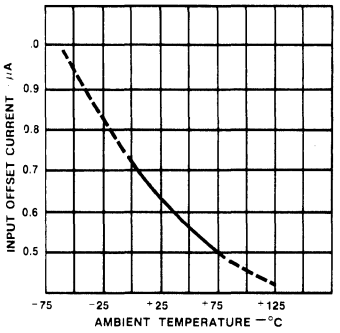


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

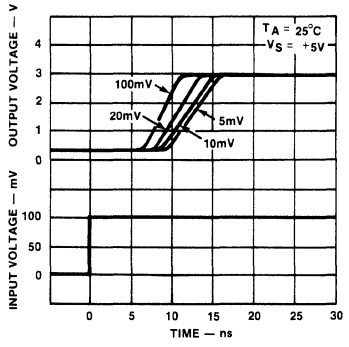
INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



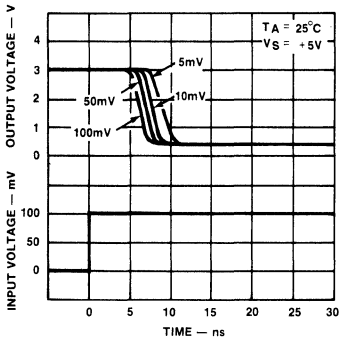
INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



55/75450B-F,N • 55/75451B/2B/3B/4B-N,T

DESCRIPTION

Series 55450B/75450B dual peripheral drivers are a family of versatile devices designed for use in systems that employ TTL or DTL logic. The 55450B/75450B family is functionally interchangeable with and replaces the 75450 family and the 75450A family devices manufactured previously. The speed of the 55450B/75450B family is equal to that of the 75450 family and a test to ensure freedom from latch-up has been added. Diode-clamped inputs simplify circuit design. Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers. Series 55450B drivers are characterized for operation over the full military temperature range of -55°C to 125°C; Series 75450B drivers are characterized for operation from 0°C to 70°C.

The 55450B and 75450B are unique general-purpose devices each featuring two standard Series 54/74 TTL gates and two uncommitted, high-current, high-voltage n-p-n transistors. These devices offer the system designer the flexibility of tailoring the circuit to the application.

The 55451B/75451B, 55452B/75452B, 55453B/75453B, and 55454B/75454B are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic) with the output of the logic gates internally connected to the bases of the n-p-n output transistors.

FEATURES

- **300mA output current capability**
- **High voltage outputs**
- **No output latch up at 20V**
- **High speed switching**
- **Circuit flexibility for varied applications**
- **TTL or DTL compatible diode—clamped inputs**
- **Standard supply voltages**

TRUTH TABLE (55/75450B and 55/75451B)

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

TRUTH TABLE (55/75452B)

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

TRUTH TABLE (55/75453B)

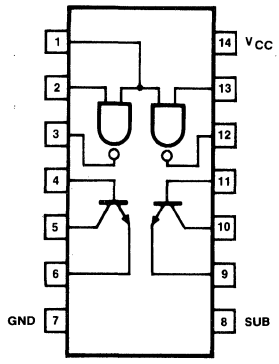
A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

TRUTH TABLE (55/75454B)

A	B	Y
L	L	H (off state)
L	H	L (on state)
H	L	L (on state)
H	H	L (on state)

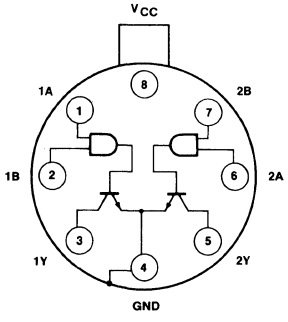
PIN CONFIGURATIONS

F,N PACAGE



ORDER PART NO.
55/775450B

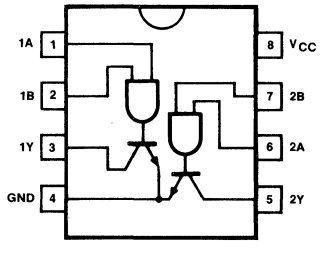
T PACKAGE



Pin 4 is in electrical contact with the case

ORDER PART NO.
55/75451B
55/75452B
55/75453B
55/75454B

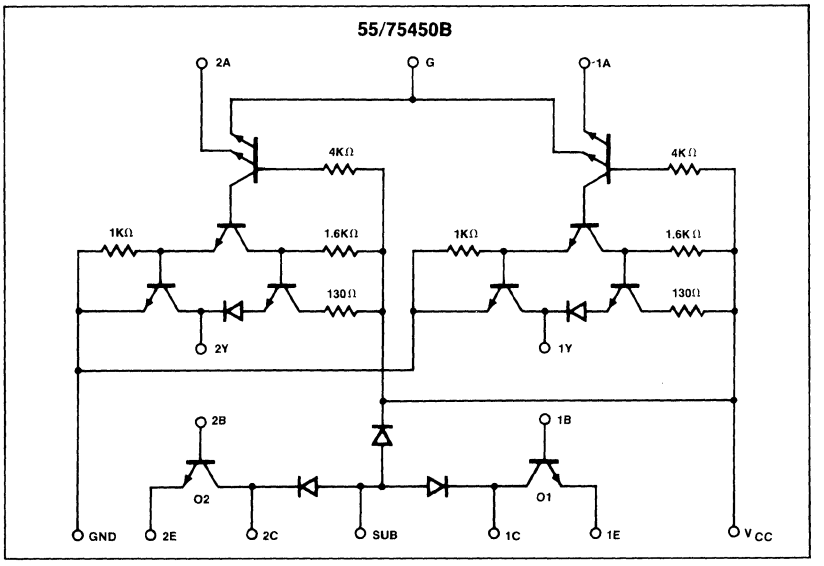
N PACKAGE



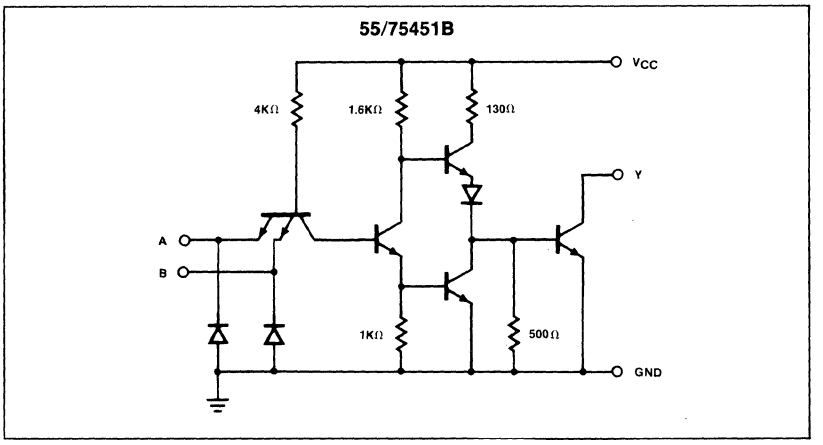
positive logic: Y = AB

EQUIVALENT SCHEMATICS

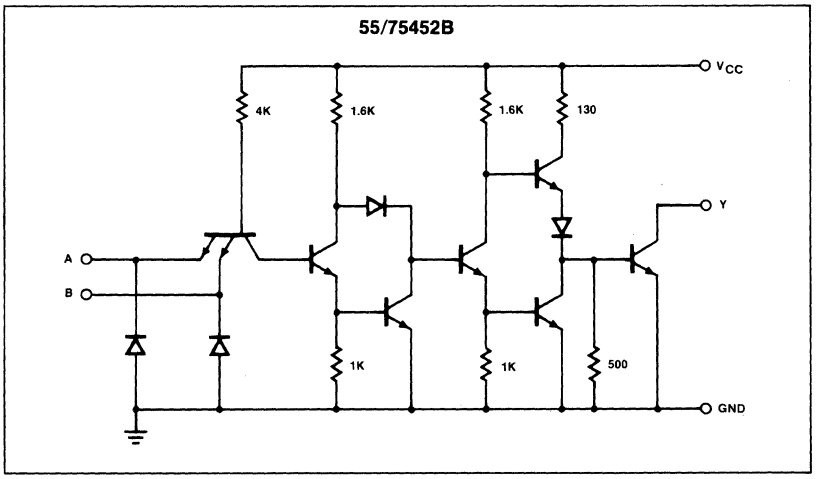
55/75450B



55/75451B

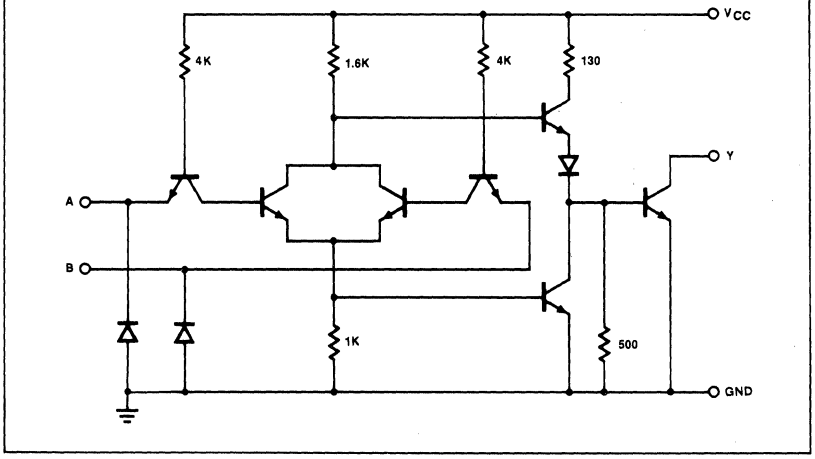


55/75452B

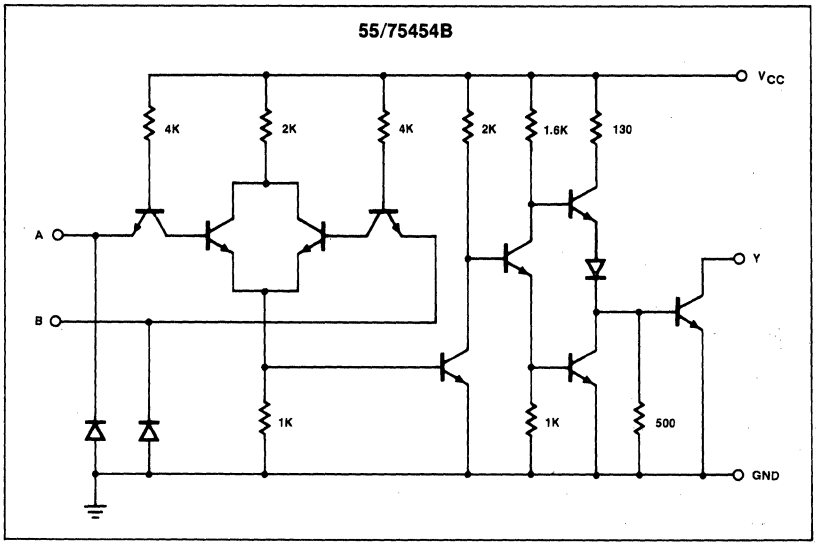


EQUIVALENT SCHEMATICS

55/75453B



55/75454B



ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise specified.

PARAMETER	55450B	75450B	55454B 55453B 55452B 55451B	75454B 75453B 75452B 75451B	UNIT
Supply voltage, V_{CC}[1]	7	7	7	7	V
Input voltage	5.5	5.5	5.5	5.5	V
Interemitter voltage[2]	5.5	5.5	5.5	5.5	V
V_{CC}-to-substrate voltage	35	35			V
Collector-to-substrate voltage	35	35			V
Collector-base voltage	35	35			V
Collector-emitter voltage[3]	30	30			V
Emitter-base voltage	5	5			V
Output voltage[4]			30	30	V
Collector current[5]	300	300			mA
Output current[5]			300	300	mA
Continuous total dissipation at (or below) 25°C free-air temperature[6]	800	800	800	800	mW
Operating free-air temperature range	-55 to 125	0 to 70	-55 to 125	0 to 70	°C
Storage temperature range	-65 to 150	-65 to 150	-65 to 150	-65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds F or T package	300	300	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds N package	260	260	260	260	°C

NOTES

1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transitor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500Ω.
4. This is the maximum voltage which should be applied to any output when it is in the off state.
5. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
6. For operation above 25°C free-air temperature, refer to Dissipation Derating Curve, Figure 20. This rating for the T package requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 95°C/W.

DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5V unless otherwise specified.

PARAMETER		TEST CONDITIONS	55450B			75450B			UNIT
			Min	Typ	Max	Min	Typ	Max	
$V_{(BR)CBO}$	Collector-base breakdown voltage	I_C = 100μA, I_E = 0	35			35			V
$V_{(BR)CER}$	Collector-emitter breakdown voltage	I_C = 100μA, R_{BE} = 500Ω	30			30			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage	I_E = 100μA, I_C = 0	5			5			V
h_{FE}	Static forward current transfer ratio	V_{CE} = 3V, I_C = 100mA	25			25			
h_{FE}	Static forward current transfer ratio	V_{CE} = 3V, I_C = 300mA	30			30			
h_{FE}	Static forward current transfer ratio	V_{CE} = 3V, I_C = 100mA	10						
h_{FE}	Static forward current transfer ratio	V_{CE} = 3V, I_C = 300mA	15						
h_{FE}	Static forward current transfer ratio	V_{CE} = 3V, I_C = 100mA				20			
h_{FE}	Static forward current transfer ratio	V_{CE} = 3V, I_C = 300mA				25			
V_{BE}	Base-emitter voltage	I_B = 10mA, I_C = 100mA		0.85	1.2		0.85	1	V
V_{BE}	Base-emitter voltage	I_B = 30mA, I_C = 300mA		1.05	1.4		1.05	1.2	V
$V_{CE(SAT)}$	Collector-emitter saturation voltage	I_B = 10mA, I_C = 100mA		0.25	0.5		0.25	0.4	V
$V_{CE(SAT)}$	Collector-emitter saturation voltage	I_B = 30mA, I_C = 300mA		0.5	0.8		0.5	0.7	V

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $V_{CC} = 5V$ unless otherwise specified.

PARAMETER			TEST CONDITIONS	55450B			75450B			UNIT
				Min	Typ	Max	Min	Typ	Max	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage		$V_{CC} = 4.5V$ $I_I = -12mA$			1.5				V
V_I	Input clamp voltage		$V_{CC} = 4.75V$ $I_I = -12mA$						1.5	V
V_{OH}	High-level output voltage		$V_{CC} = 4.5V$ $V_{IL} = 0.8V$ $I_{OH} = -400\mu A$	2.4	3.3					V
V_{OH}	High-level output voltage		$V_{CC} = 4.75V$ $V_{IL} = 0.8V$ $I_{OH} = -400\mu A$					2.4	3.3	V
V_{OL}	Low-level output voltage		$V_{CC} = 4.5V$ $V_{IH} = 2V$ $I_{OL} = 16mA$		0.22	0.5				V
V_{OL}	Low-level output voltage		$V_{CC} = 4.75V$ $V_{IH} = 2V$ $I_{OL} = 16mA$					0.22	0.4	V
I_I	Input current at maximum input voltage	InputA	$V_{CC} = 5.5V$ $V_I = 5.5V$			1				mA
		InputG				2				
I_I	Input current at maximum input voltage	InputA	$V_{CC} = 5.25V$ $V_I = 5.5V$						1	mA
		InputG							2	
I_{IH}	High level input current	InputA	$V_{CC} = 5.5V$ $V_I = 2.4V$			40				μA
		InputG				80				
I_{IH}	High level input current	InputA	$V_{CC} = 5.25V$ $V_I = 2.4V$						40	μA
		InputG							80	
I_{IL}	Low-level input current	InputA	$V_{CC} = 5.5V$ $V_I = 0.4V$			-1.6				mA
		InputG				-3.2				
I_{IL}	Low-level input current	InputA	$V_{CC} = 5.25V$ $V_I = 0.4V$						-1.6	mA
		InputG							-3.2	
I_{OS}	Short-circuit output current[2]		$V_{CC} = 5.5V$	-18		-55				mA
I_{OS}	Short-circuit output current[2]		$V_{CC} = 5.25V$				-18		-55	mA
I_{CCH}	Supply current, outputs high		$V_{CC} = 5.5V$ $V_I = 0$		2	4				mA
I_{CCH}	Supply current, outputs high		$V_{CC} = 5.25V$ $V_I = 0$					2	4	mA
I_{CCL}	Supply current, outputs low		$V_{CC} = 5.5V$ $V_I = 5V$		6	11				mA
I_{CCL}	Supply current, outputs low		$V_{CC} = 5.25V$ $V_I = 5V$					6	11	mA

NOTES

1. Electrical characteristics over recommended operating free-air temperature range (unless otherwise specified).
2. Not more than one output should be shorted at a time.

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $V_{CC} = 5V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	55451			75451			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	$V_{CC} = 4.5V$ $I_I = -12mA$			-1.5				V
V_I	Input clamp voltage	$V_{CC} = 4.75V$ $I_I = -12mA$						1.5	
I_{OH}	High-level output current	$V_{CC} = 4.5V$, $V_{IH} = 2V$, $V_{OH} = 30V$			300				μA
I_{OH}	High-level output current	$V_{CC} = 4.75V$, $V_{IH} = 2V$, $V_{OH} = 30V$						100	μA
V_{OL}	Low-level output voltage	$V_{CC} = 4.5V$, $V_{IL} = 0.8V$, $I_{OL} = 100mA$		0.25	0.5				V
		$V_{CC} = 4.5V$, $V_{IL} = 0.8V$, $I_{OL} = 300mA$		0.5	0.8				
V_{OL}	Low-level output voltage	$V_{CC} = 4.75V$, $V_{IL} = 0.8V$, $I_{OL} = 100mA$					0.25	0.4	V
		$V_{CC} = 4.75V$, $V_{IL} = 0.8V$, $I_{OL} = 300mA$					0.5	0.7	
I_I	Input current at maximum input voltage	$V_{CC} = 5.5V$, $V_I = 5.5V$			1				mA
I_I	Input current at maximum input voltage	$V_{CC} = 5.25V$, $V_I = 5.5V$						1	mA
I_{IH}	High level input current	$V_{CC} = 5.5V$, $V_I = 2.4V$			40				mA
I_{IH}	High level input current	$V_{CC} = 5.25V$ $V_I = 2.4V$						40	μA
I_{IL}	Low level input current	$V_{CC} = 5.5V$ $V_I = 0.4V$		-1	-1.6				mA
I_{IL}	Low-level input current	$V_{CC} = 5.25V$ $V_I = 0.4V$					-1	-1.6	mA
I_{CCH}	Supply current, outputs high	$V_{CC} = 5.5V$ $V_I = 5V$		7	11				mA
I_{CCH}	Supply current, outputs high	$V_{CC} = 5.25V$ $V_I = 5V$					7	11	mA
I_{CCL}	Supply current, outputs low	$V_{CC} = 5.5V$ $V_I = 0$		52	65				mA
I_{CCL}	Supply current, outputs low	$V_{CC} = 5.25V$ $V_I = 0$					52	65	mA

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $V_{CC} = 5V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	55452			75452			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	$V_{CC} = 4.5V$ $I_I = -12mA$			-1.5				V
V_I	Input clamp voltage	$V_{CC} = 4.75V$ $I_I = -12mA$						-1.5	
I_{OH}	High-level output current	$V_{CC} = 4.5V$, $V_{IL} = 0.8V$, $V_{OH} = 30V$							μA
I_{OH}	High-level output current	$V_{CC} = 4.75V$, $V_{IL} = 0.8V$, $V_{OH} = 30V$			300			100	μA
V_{OL}	Low-level output voltage	$V_{CC} = 4.5V$, $V_{IH} = 2V$, $I_{OL} = 100mA$		0.25	0.5				V
		$V_{CC} = 4.5V$, $V_{IH} = 2V$, $I_{OL} = 300mA$		0.5	0.8				
V_{OL}	Low-level output voltage	$V_{CC} = 4.75V$, $V_{IH} = 2V$, $I_{OL} = 100mA$					0.25	0.4	V
		$V_{CC} = 4.75V$, $V_{IH} = 2V$, $I_{OL} = 300mA$					0.5	0.7	
I_I	Input current at maximum input voltage	$V_{CC} = 5.5V$, $V_I = 5.5V$			1				mA
I_I	Input current at maximum input voltage	$V_{CC} = 5.25V$, $V_I = 5.5V$						1	mA
I_{IH}	High-level input current	$V_{CC} = 5.5V$, $V_I = 2.4V$			40				μA
I_{IH}	High-level input current	$V_{CC} = 5.25V$, $V_I = 2.4V$						40	μA
I_{IL}	Low-level input current	$V_{CC} = 5.5V$, $V_I = 0.4V$		-1	-1.6				mA
I_{IL}	Low-level input current	$V_{CC} = 5.25V$, $V_I = 0.4V$					-1	-1.6	mA
I_{CCH}	Supply current, outputs high	$V_{CC} = 5.5V$, $V_I = 0V$		11	14				mA
I_{CCH}	Supply current, outputs high	$V_{CC} = 5.25V$, $V_I = 0V$					11	14	mA
I_{CCL}	Supply current, outputs low	$V_{CC} = 5.5V$, $V_I = 5V$		56	71				mA
I_{CCL}	Supply current, outputs low	$V_{CC} = 5.25V$, $V_I = 5V$					56	71	mA

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DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $V_{CC} = 5V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	55453			75453			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	$V_{CC} = 4.5V$ $I_I = -12mA$			-1.5				V
V_I	Input clamp voltage	$V_{CC} = 4.75V$ $I_I = -12mA$						-1.5	
I_{OH}	High-level output current	$V_{CC} = 4.5V$, $V_{IH} = 2V$, $V_{OH} = 30V$			300				μA
I_{OH}	High-level output current	$V_{CC} = 4.75V$, $V_{IH} = 2V$, $V_{OH} = 30V$						100	μA
V_{OL}	Low-level output voltage	$V_{CC} = 4.5V$, $V_{IL} = 0.8V$, $I_{OL} = 100mA$		0.25	0.5				V
		$V_{CC} = 4.5V$, $V_{IL} = 0.8V$, $I_{OL} = 300mA$		0.5	0.8				
V_{OL}	Low-level output voltage	$V_{CC} = 4.75V$, $V_{IL} = 0.8V$, $I_{OL} = 100mA$					0.25	0.4	V
		$V_{CC} = 4.75V$, $V_{IL} = 0.8V$, $I_{OL} = 300mA$					0.5	0.7	
I_I	Input current at maximum input voltage	$V_{CC} = 5.5V$, $V_I = 5.5V$			1				mA
I_I	Input current at maximum input voltage	$V_{CC} = 5.25V$, $V_I = 5.5V$						1	mA
I_{IH}	High-level input current	$V_{CC} = 5.5V$, $V_I = 2.4V$			40				μA
I_{IH}	High-level input current	$V_{CC} = 5.25V$, $V_I = 2.4V$						40	μA
I_{IL}	Low-level input current	$V_{CC} = 5.5V$, $V_I = 0.4V$		-1	-1.6				mA
I_{IL}	Low-level input current	$V_{CC} = 5.25V$, $V_I = 0.4V$					-1	-1.6	mA
I_{CCH}	Supply current, outputs high	$V_{CC} = 5.5V$, $V_I = 5V$		8	11				mA
I_{CCH}	Supply current, outputs high	$V_{CC} = 5.25V$, $V_I = 5V$					8	11	mA
I_{CCL}	Supply current, outputs low	$V_{CC} = 5.5V$, $V_I = 0$		54	68				mA
I_{CCL}	Supply current, outputs low	$V_{CC} = 5.25V$, $V_I = 0$					54	68	mA

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $V_{CC} = 5V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	55454			75454			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	$V_{CC} = 4.5V$ $I_I = -12mA$			-1.5				V
V_I	Input clamp voltage	$V_{CC} = 4.75V$ $I_I = -12mA$						-1.5	
I_{OH}	High-level output current	$V_{CC} = 4.5V$, $V_{IL} = 0.8V$, $V_{OH} = 30V$							μA
I_{OH}	High-level output current	$V_{CC} = 4.75V$, $V_{IL} = 0.8V$, $V_{OH} = 30V$			300			100	
V_{OL}	Low-level output voltage	$V_{CC} = 4.5V$, $V_{IH} = 2V$, $I_{OL} = 100mA$		0.25	0.5				V
		$V_{CC} = 4.5V$, $V_{IH} = 2V$, $I_{OL} = 300mA$		0.5	0.8				V
V_{OL}	Low-level output voltage	$V_{CC} = 4.75V$, $V_{IH} = 2V$, $I_{OL} = 100mA$					0.25	0.4	V
		$V_{CC} = 4.75V$, $V_{IH} = 2V$, $I_{OL} = 300mA$					0.5	0.7	
I_I	Input current at maximum input voltage	$V_{CC} = 5.5V$, $V_I = 5.5V$			1				mA
I_I	Input current at maximum input voltage	$V_{CC} = 5.25V$, $V_I = 5.5V$						1	mA
I_{IH}	High-level input current	$V_{CC} = 5.5V$, $V_I = 2.4V$			40				μA
I_{IH}	High-level input current	$V_{CC} = 5.25V$, $V_I = 2.4V$						40	μA
I_{IL}	Low-level input current	$V_{CC} = 5.5V$, $V_I = 0.4V$		-1	-1.6				mA
I_{IL}	Low-level input current	$V_{CC} = 5.25V$, $V_I = 0.4V$					-1	-1.6	mA
I_{CCH}	Supply current, outputs high	$V_{CC} = 5.5V$, $V_I = 0V$		13	17				mA
I_{CCH}	Supply current, outputs high	$V_{CC} = 5.25V$, $V_I = 0V$					13	17	mA
I_{CCL}	Supply current, outputs low	$V_{CC} = 5.5V$, $V_I = 5V$		61	79				mA
I_{CCL}	Supply current, outputs low	$V_{CC} = 5.25V$, $V_I = 5V$					61	79	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	55/75450B			UNIT
			Min	Typ	Max	
TTL GATES						
t_{PLH}	Propagation delay time, low-to-high output	$C_L = 15pF$, $R_L = 400\Omega$		12	22	ns
t_{PHL}	Propagation delay time, high-to-low level output			8	15	ns
OUTPUT TRANSISTORS						
t_d	Delay time	$I_C = 200mA$, $I_{B(1)} = 20mA$,		8	15	ns
t_r	Rise time	$I_{B(2)} = -40mA$,		12	20	ns
t_s	Storage time	$V_{BE(OFF)} = -1V$, $C_L = 15pF$,		7	15	ns
t_f	Full time	$R_L = 50\Omega$		6	15	ns
GATES AND TRANSISTORS COMBINED						
t_{PLH}	Propagation delay time, low-to-high level output	$I_C \approx 200mA$, $C_L = 15pF$, $R_L = 50\Omega$		20	30	ns
t_{PHL}	Propagation delay time, high-to-low level output			20	30	ns
t_{TLH}	Transition time, low-to-high level output			7	12	ns
t_{THL}	Transition time, high-to-low level output			9	15	ns
V_{OH}	High-level output voltage after switching	$V_S = 20V$, $I_C \approx 300mA$ $R_{BE} = 500\Omega$	V_S-6.5			mV

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	55451/75451			55452/75452			UNIT
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation delay time, low-to-high level output	$I_O \approx 200mA$, $C_L = 15pF$, $R_L = 50\Omega$		18	25		26	35	ns
t_{PHL}	Propagation delay time, high-to-low level output	$I_O \approx 200mA$, $C_L = 15pF$, $R_L = 50\Omega$		18	25		24	35	ns
t_{TLH}	Transition time, low-to-high level output	$I_O \approx 200mA$, $C_L = 15pF$, $R_L = 50\Omega$		5	8		5	8	ns
t_{THL}	Transition time, High-to-low level output	$I_O \approx 200mA$, $C_L = 15pF$, $R_L = 50\Omega$		7	12		7	12	ns
V_{OH}	High-level output voltage after switching	$V_S = 20V$, $I_O \approx 300mA$	V_S-6.5			V_S-6.5			mV

NOTE

Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

AC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $V_{CC} = 5V$ unless otherwise specified.

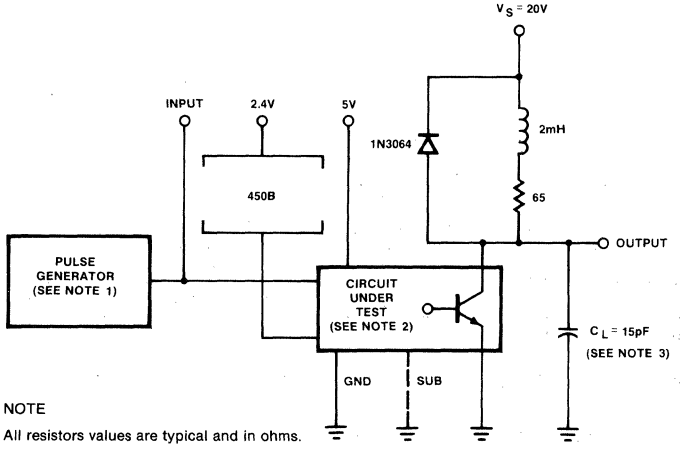
PARAMETER		TEST CONDITIONS	55453/75453			55454/75454			UNIT
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation delay time, low-to-high level output	$I_O \approx 200mA$, $C_L = 15pF$, $R_L = 50\Omega$		18	25		27	35	ns
t_{PHL}	Propagation delay time, high-to-low level output	$I_O \approx 200mA$, $C_L = 15pF$, $R_L = 50\Omega$		16	25		24	35	ns
t_{TLH}	Transition time, low-to-high level output	$I_O \approx 200mA$, $C_L = 15pF$, $R_L = 50\Omega$		5	8		5	8	ns
t_{THL}	Transition time, High-to-low level output	$I_O \approx 200mA$, $C_L = 15pF$, $R_L = 50\Omega$		7	12		7	12	ns
V_{OH}	High-level output voltage after switching	$V_S = 20V$, $I_O \approx 300mA$	V_S-6.5			V_S-6.5			mV

NOTE

Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

LATCH-UP TEST OF COMPLETE DRIVERS

TEST CIRCUIT



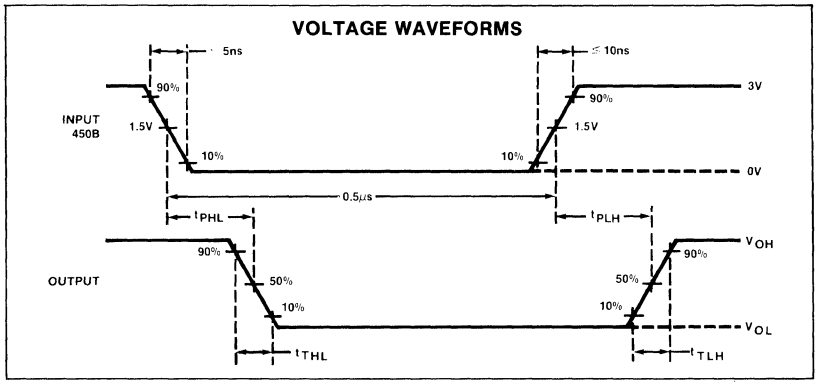
NOTE

All resistors values are typical and in ohms.

NOTES

1. The pulse generator has the following characteristics: PRR = 12.5kHz, $Z_{OUT} = 50\Omega$.
2. When testing 55450B or 75450B, connect output Y to transistor base with a 500-Ω resistor from there to ground, and ground to substrate terminal.
3. C_L includes probe and jig capacitance.

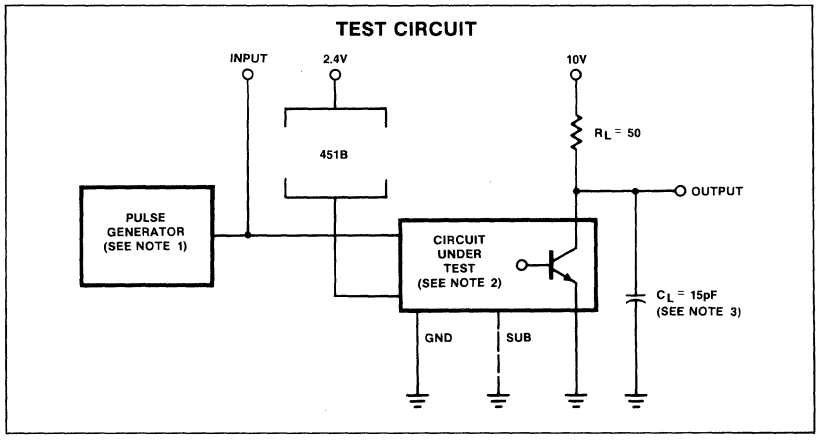
LATCH-UP TEST OF COMPLETE DRIVERS (Cont'd)

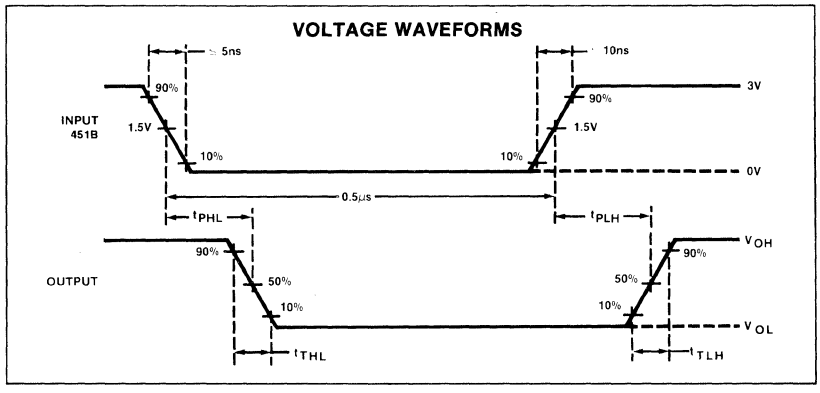


NOTES

1. The pulse generator has the following characteristics: PRR = 12.5kHz, Z_{OUT} = 50Ω.
2. When testing 55450B or 75450B, connect output Y to transistor base with a 500-Ω resistor from there to ground, and ground to substrate terminal.
3. C_L includes probe and jig capacitance.

SWITCHING TIMES OF COMPLETE DRIVERS

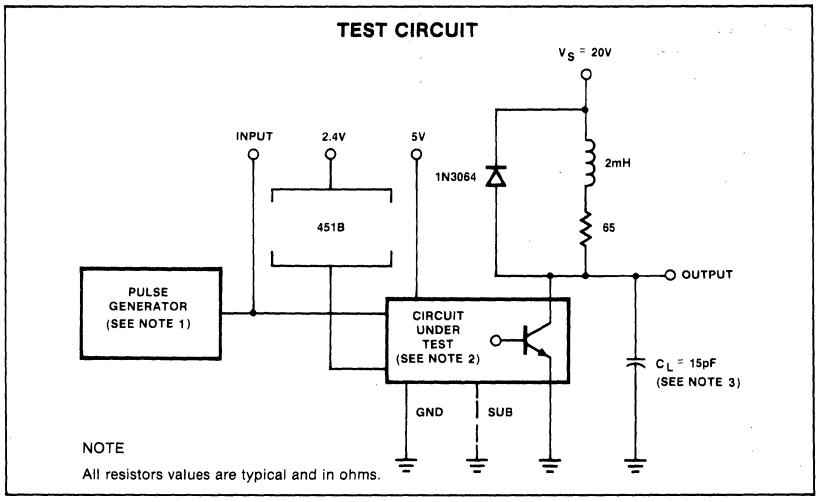


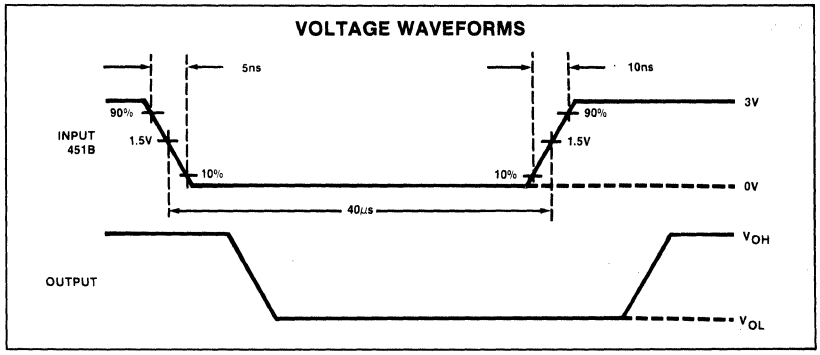


NOTES

1. The pulse generator has the following characteristics: PRR = 1MHz, $Z_{OUT} \approx 50\Omega$.
2. When testing 55451B or 75451B, connect output Y to translator base and ground the substrate terminal.
3. C_L includes probe and jig capacitance.

LATCH-UP TEST OF COMPLETE DRIVERS

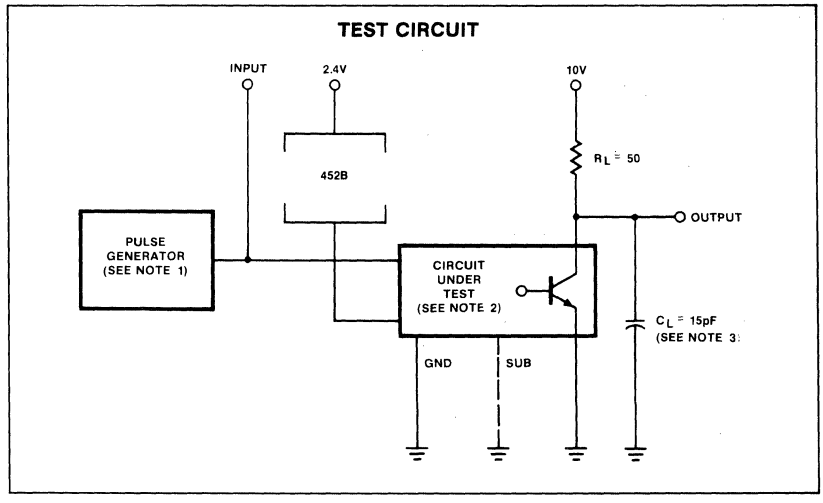




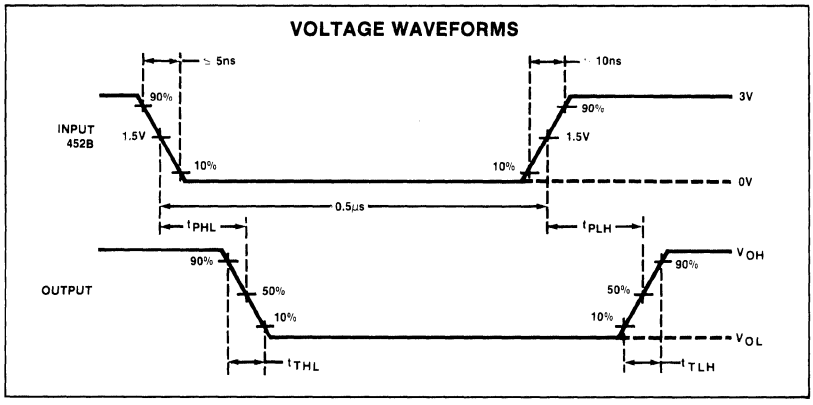
NOTES

1. The pulse generator has the following characteristics: PRR = 12.5kHz, Z_{OUT} = 50Ω.
2. When testing 55451B or 75451B, connect output Y to transistor base with a 500-Ω resistor from there to ground, and ground the substrate terminal.
3. C_L includes probe and jig capacitance.

SWITCHING TIMES OF COMPLETE DRIVERS



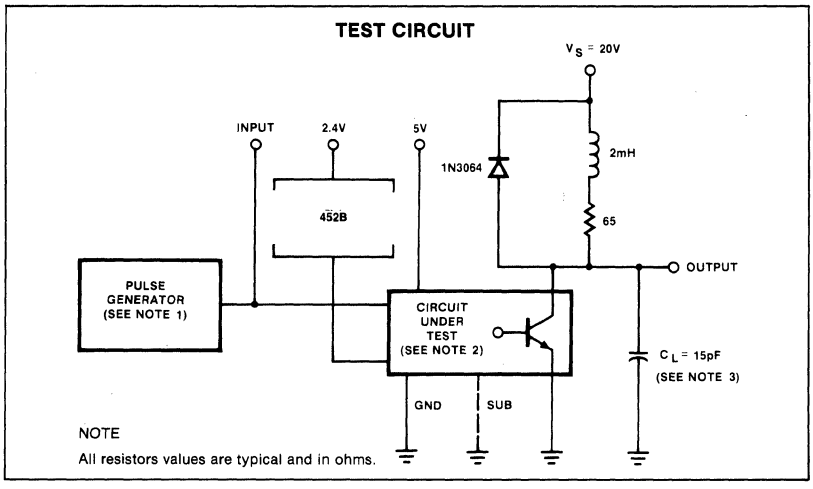
SWITCHING TIMES OF COMPLETE DRIVERS (Cont'd)

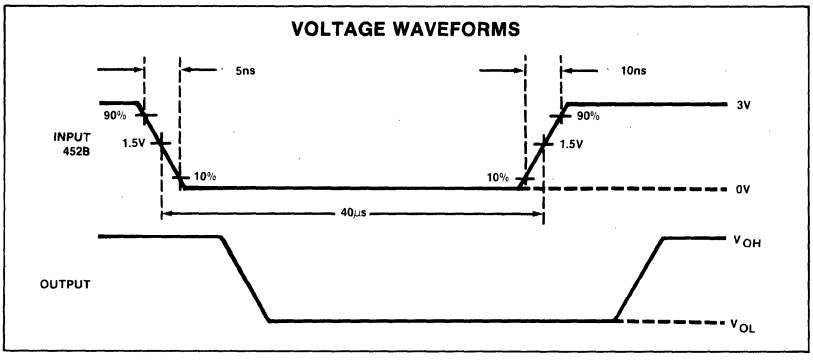


NOTES

1. The pulse generator has the following characteristics: PRR = 1MHz, $Z_{OUT} \approx 50\Omega$.
2. When testing 55452B or 75452B, connect output Y to transistor base and ground the substrate terminal.
3. C_L includes probe and jig capacitance.

LATCH-UP TEST OF COMPLETE DRIVERS

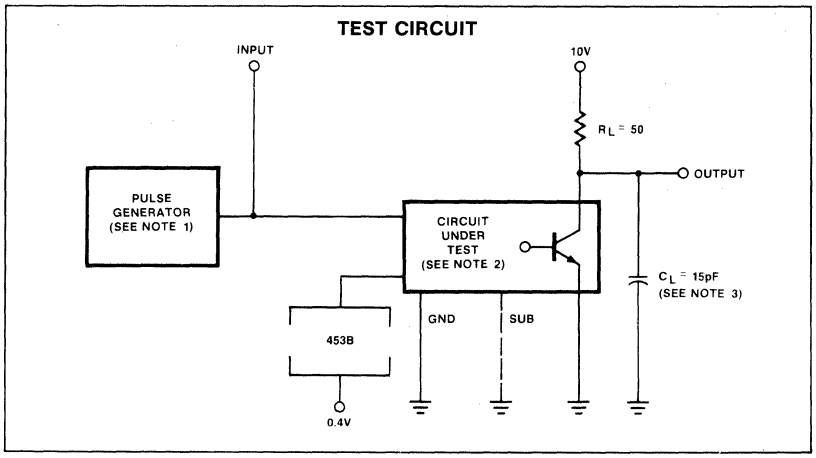


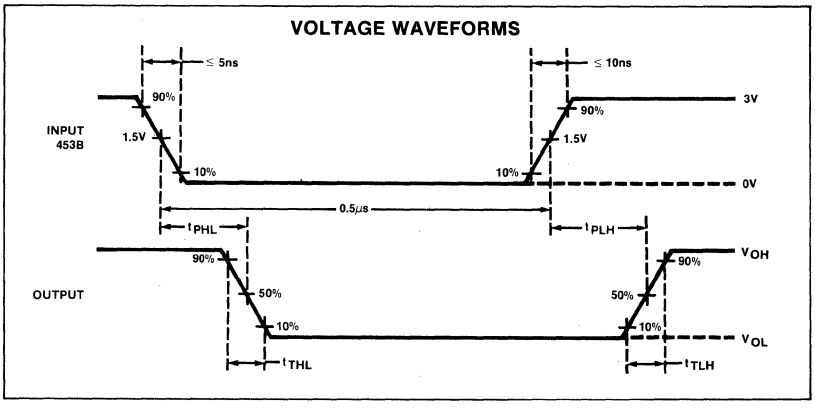


NOTES

1. The pulse generator has the following characteristics: PRR = 12.5kHz, $Z_{OUT} = 50\Omega$.
2. When testing 55452B or 75452B, connect output Y to transistor base with a 500-Ω resistor from there to ground, and ground the substrate terminal.
3. C_L includes probe and jig capacitance.

SWITCHING TIMES OF COMPLETE DRIVERS

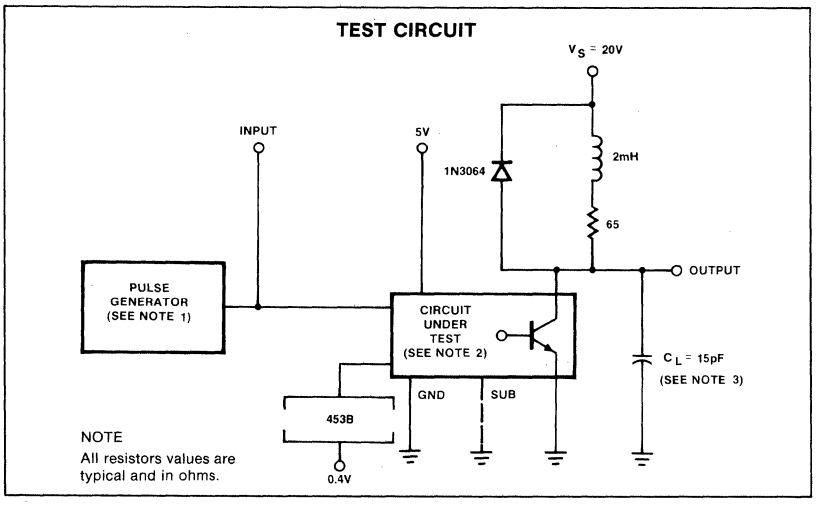




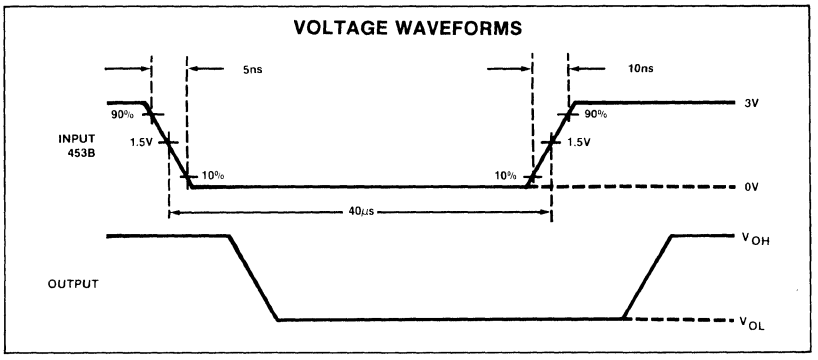
NOTES

1. The pulse generator has the following characteristics: PRR = 1MHz, $Z_{OUT} \approx 50\Omega$.
2. When testing 55453B or 75453B, connect output Y to transistor base and ground the substrate terminal.
3. C_L includes probe and jig capacitance.

LATCH-UP TEST OF COMPLETE DRIVERS



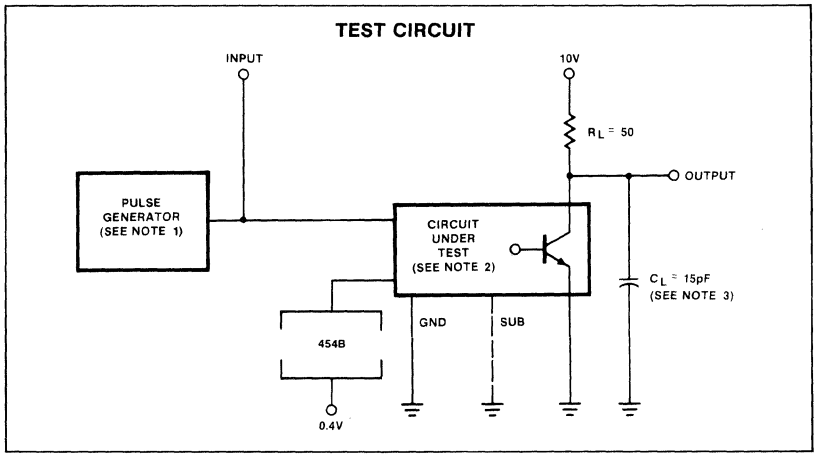
LATCH-UP TEST OF COMPLETE DRIVERS (Cont'd)

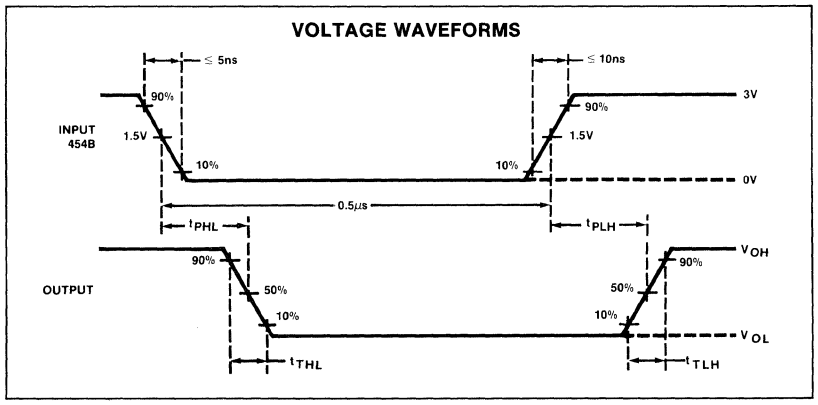


NOTES

1. The pulse generator has the following characteristics: PRR = 12.5kHz, Z_{OUT} = 50Ω.
2. When testing 55453B or 75453B, connect output Y to transistor base with a 500-Ω resistor from there to ground, and ground the substrate terminal.
3. C_L includes probe and jig capacitance.

SWITCHING TIMES OF COMPLETE DRIVERS



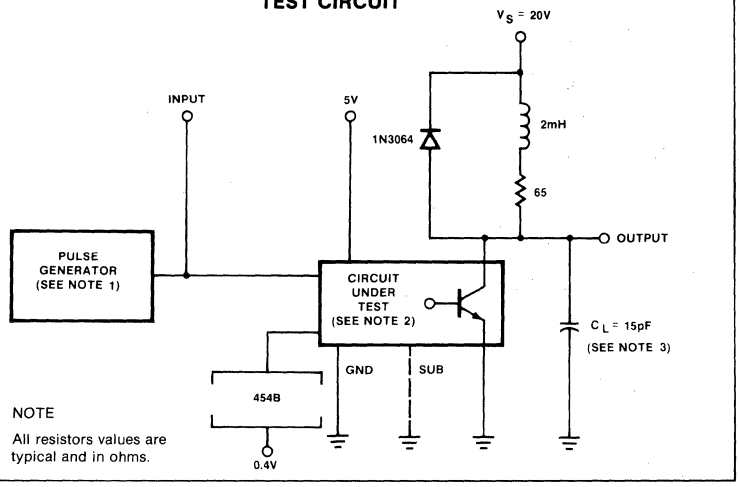


NOTES

1. The pulse generator has the following characteristics: PRR = 1MHz, $Z_{OUT} \approx 50\Omega$.
2. When testing 55454B or 75454B, connect output Y to transistor base and ground the substrate terminal.
3. C_L includes probe and jig capacitance.

LATCH-UP TEST OF COMPLETE DRIVERS

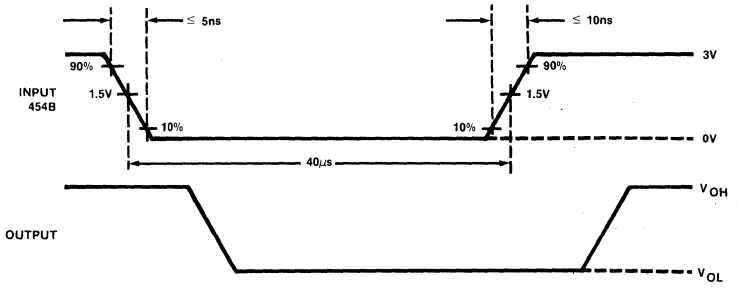
TEST CIRCUIT



NOTE

All resistors values are typical and in ohms.

VOLTAGE WAVEFORMS

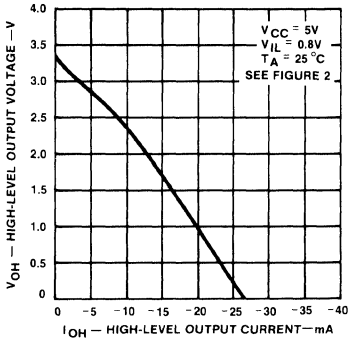


NOTES

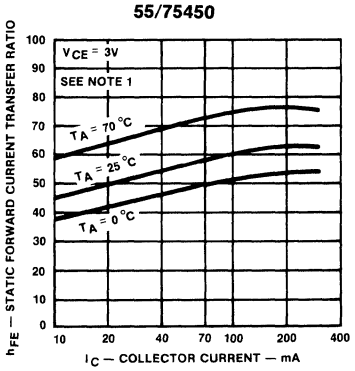
1. The pulse generator has the following characteristics: PRR = 12.5kHz, Z_{OUT} = 50Ω.
2. When testing 55454B or 75454B, connect output Y to transistor base with a 500-Ω resistor from there to ground, and ground the substrate terminal.
3. C_L includes probe and jig capacitance.

TYPICAL PERFORMANCE CHARACTERISTICS

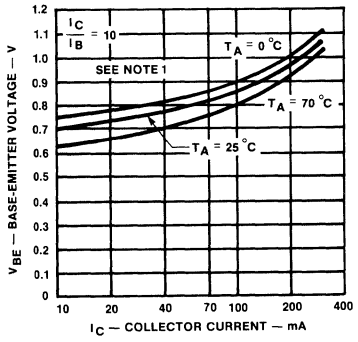
TTL GATE HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT
55/75450



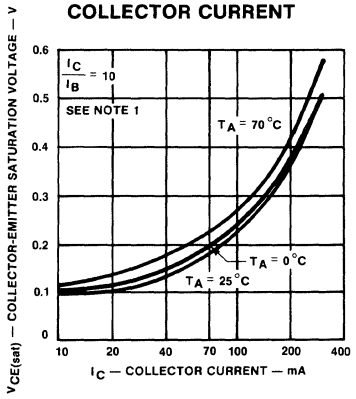
TRANSISTOR STATIC FORWARD CURRENT TRANSFER RATIO vs COLLECTOR CURRENT
55/75450



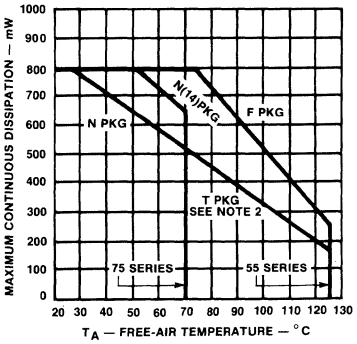
TRANSISTOR BASE-EMITTER VOLTAGE vs COLLECTOR CURRENT
55/75450



TRANSISTOR COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT



DISSIPATION DERATING CURVE



NOTE

1. These parameters must be measured using pulse techniques, tw = 300μs, duty cycle ≤ 2%.
2. This rating for the T Package requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 95°C/W.

SECTION 8
TRANSISTOR ARRAYS

NE5SE510/511-F,N

DESCRIPTION

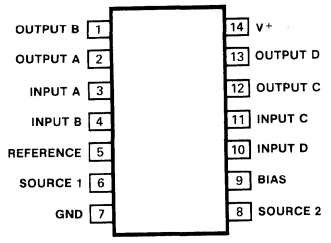
The 510/511 are dual high frequency differential amplifiers with associated constant current sources and biasing elements contained within a silicon monolithic substrate. The large number of accessable internal points allows large flexibility of applications from dc to in excess of 100mhz. Circuit layouts may be either common—common base, cascode or common collector—common base configurations.

FEATURES

- **Low input offset voltage ±2mV**
- **Low input offset current ±3μA**
- **AGC capability**
- **High forward transadmittance**
- **Low feed back capacitance**
- **Single power supply**
- **SE510, SE511 Mil std 883A,B,C available**

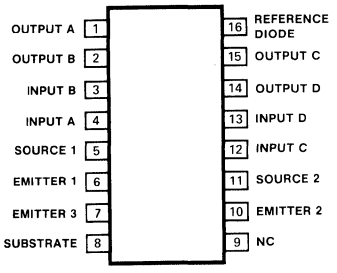
PIN CONFIGURATIONS

510
F,N PACKAGE



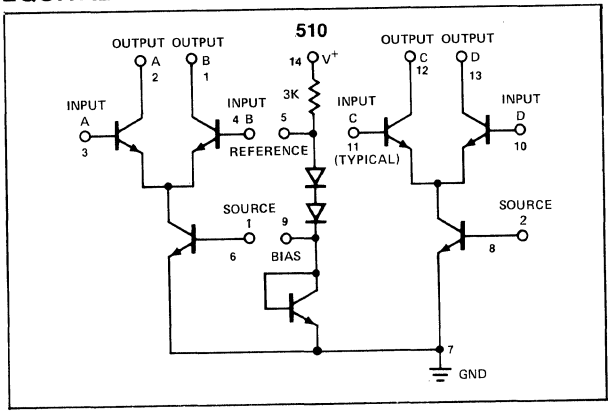
ORDER PART NO.
SE510N, NE510N
SE510F, NE510F

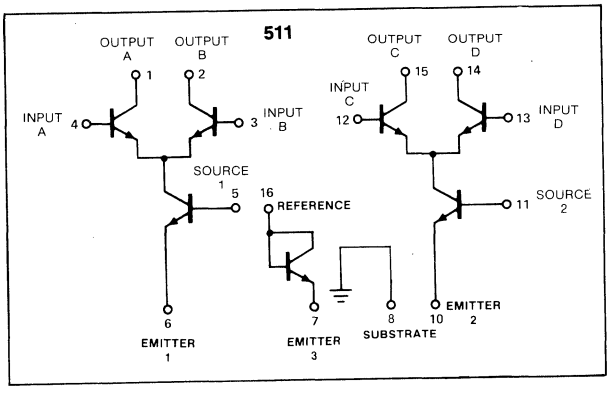
511
F,N PACKAGE



ORDER PART NO.
SE511N, NE511N
SE511F, NE511F

EQUIVALENT SCHEMATICS





ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Applied voltage (V+)	20	V
Differential input voltage	±5	V
Current (all pins)	±15	mA
Storage temperature	-65 to +150	°C
Operating temperature		
SE510N, SE511N	-55 to +125	°C
NE510N, NE511N	0 to +75	°C

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SE510			NE510			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage			0.5	2.0		0.5	3.0	mV
		Over temp.[2]		1.5	3.5		1	4	mV
I_{OS}	Input offset current			2.0	3.5		2.0	6	μA
		Over temp.[2]		2.5	7.5		2.5	9	μA
I_B	Input bias current			8	20		8	25	μA
		Over temp.[2]		16	40		10	40	μA
ΔI_C	Differential collector current per pair	$V_{IN} = 0$, $I_P = 2mA$		45	62.5		45	75	μA
		Over temp.[2], $V_{IN} = 0$, $I_P = 2mA$		50	100		50	100	μA
	Differential source current			30	62.5		30	75	μA
		Over temp.[2]		35	100		35	100	μA
I_{CC}	Total current			11	15		11	15	mA
CMRR	Common mode rejection ratio		60	80		60	80		dB

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SE511			NE511			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage			0.5	2.0		0.5	3.0	mV
		Over temp.[2]		1.5	3.5		1	4	mV
I_{OS}	Input offset current			2	3.5		2	6	μA
		Over temp.[2]		2.5	7.5		2.5	9	μA
I_B	Input bias current			8	20		8	25	μA
		Over temp.[2]		16	40		10	40	μA
ΔI_C	Differential collector current per pair	$V_{IN} = 0$, $I_P = 2mA$		45	62.5		45	75	μA
		Over temp.[2], $V_{IN} = 0$, $I_P = 2mA$		50	100		50	100	μA
	Differential source current			30	62.5		30	75	μA
		Over temp.[2]		35	100		35	100	μA
I_{CC}	Total current			11	15		11	15	mA
CMRR	Common mode rejection ratio		60	80		60	80		dB
G_{22}	Output conductance			0.01			0.01		mmhos
C_{OB}	Output capacitance			2.5			2.5		pF
C_{IB}	Input capacitance			10			10		pF

NOTES

1. Standard test circuit of Figure 1.
2. Operating temperature range:
   SE510/511 -55°C to +125°C
   NE510/511 0°C to +70°C

NE5SE510/511-F,N

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, V+ = 12V unless otherwise specified.

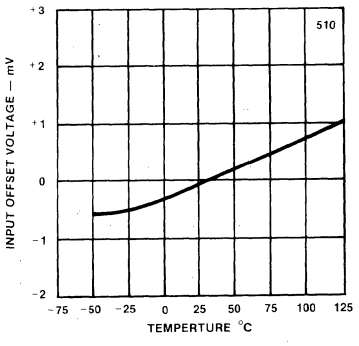
PARAMETER		TEST CONDITIONS	EMITTER COUPLED			CASCODE			UNIT
			Min	Typ	Max	Min	Typ	Max	
$[Re(Y_{11})]$ $[Re(Y_{22})]$	Input conductance[2,3] Output conductance[2,3]			0.7 0.01			3.0 0.01		mmhos mmhos
C_{IB} C_{OB}	Input capacitance[2,3] Output capacitance[2,3] Reverse transfer capacitance[2,3]			4.5 2.5 0.05			10 2.5 0.05		pF pF pF
	Forward transconductance[2,3]			25			90		mmhos

NOTES

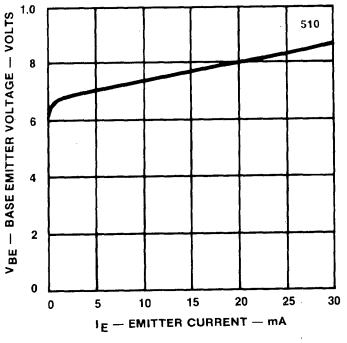
1. Applicable from DC to 10MHz
2. Emitter coupled configuration figure 2
3. Cascode configuration figure 3

TYPICAL PERFORMANCE CHARACTERISTICS

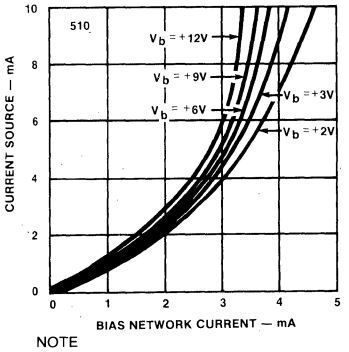
INPUT OFFSET VOLTAGE vs TEMPERATURE



BASE EMITTER VOLTAGE vs EMITTER CURRENT

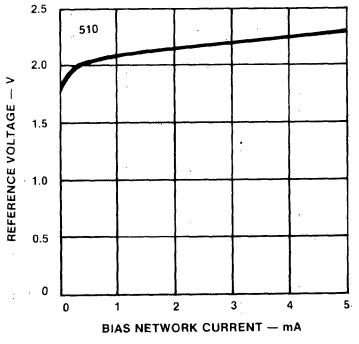


CURRENT SOURCE vs BIAS NETWORK CURRENT

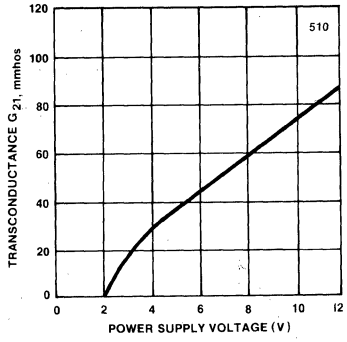


NOTE
V_b is the voltage between the bases of the differential transistors and the emitter of the current source transistor.

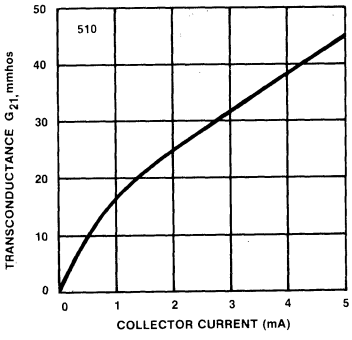
REFERENCE VOLTAGE vs BIAS NETWORK CURRENT



TRANSCONDUCTANCE vs POWER SUPPLY VOLTAGE (Cascode connection)



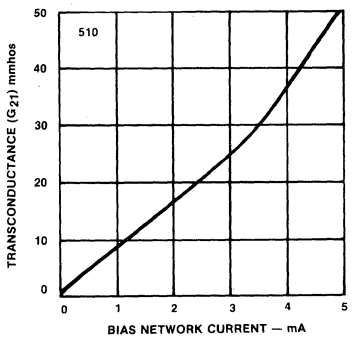
TRANSCONDUCTANCE vs COLLECTOR CURRENT (Emitter coupled)



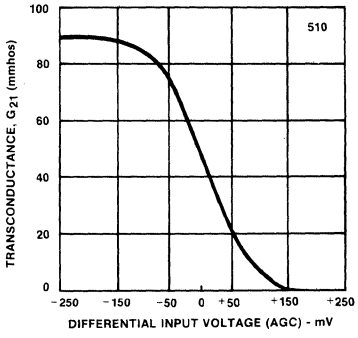
NOTE All characteristics for 25°C unless otherwise specified.

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

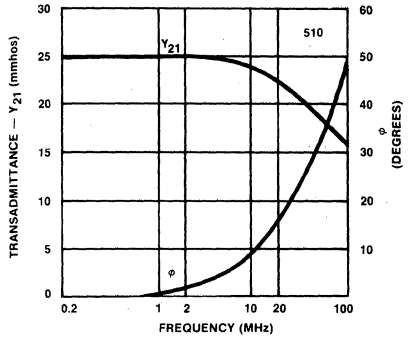
TRANSCONDUCTANCE vs BIAS NETWORK CURRENT (Emitter coupled)



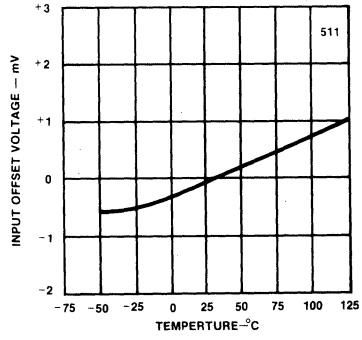
CASCODE TRANSCONDUCTANCE vs DIFFERENTIAL VIN (AGC connection)



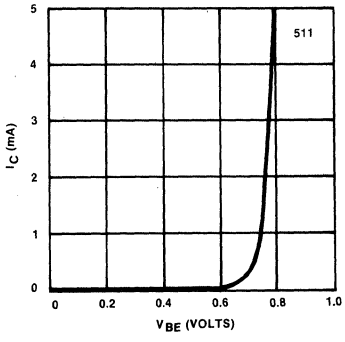
TRANSADMITTANCE vs FREQUENCY (Emitter coupled)



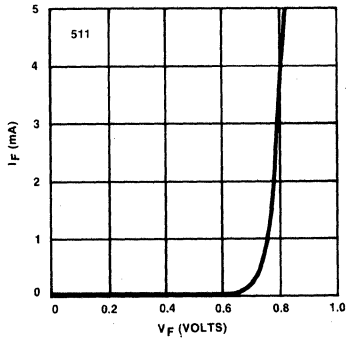
INPUT OFFSET VOLTAGE vs TEMPERATURE



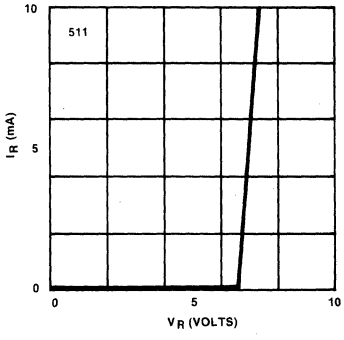
CURRENT SOURCE TRANSISTOR V_{BE} vs I_C



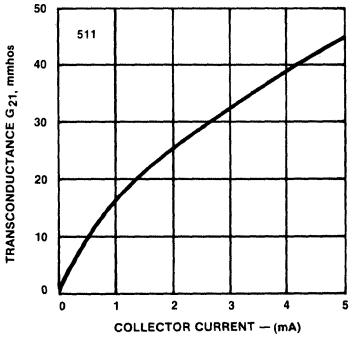
BIAS DIODE FORWARD CHARACTERISTIC V_F vs I_F



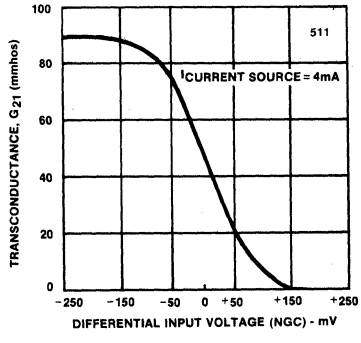
BIAS DIODE REVERSE BREAKDOWN CHARACTERISTIC



TRANSCONDUCTANCE vs COLLECTOR CURRENT (Emitter coupled)



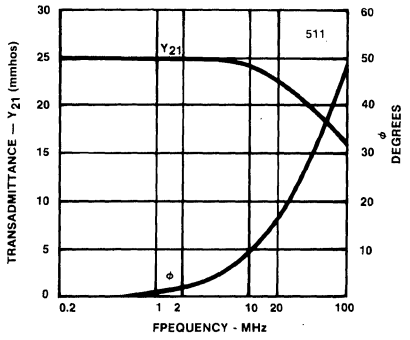
TRANSCONDUCTANCE vs DIFFERENTIAL INPUT VOLTAGE (Cascode)



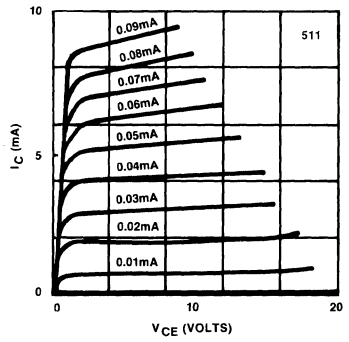
NOTE All characteristics for 25°C unless otherwise specified.

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

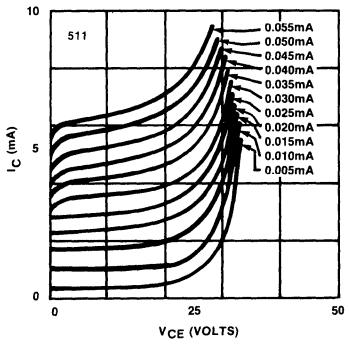
TRANSADMITTANCE vs FREQUENCY (Emitter coupled)



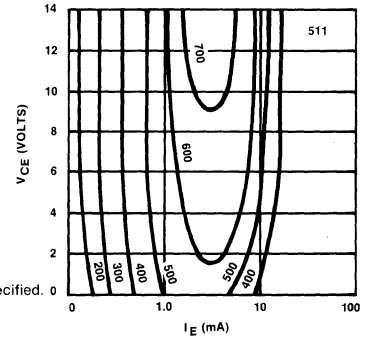
I_C vs V_{CE}



I_C vs V_{CE}

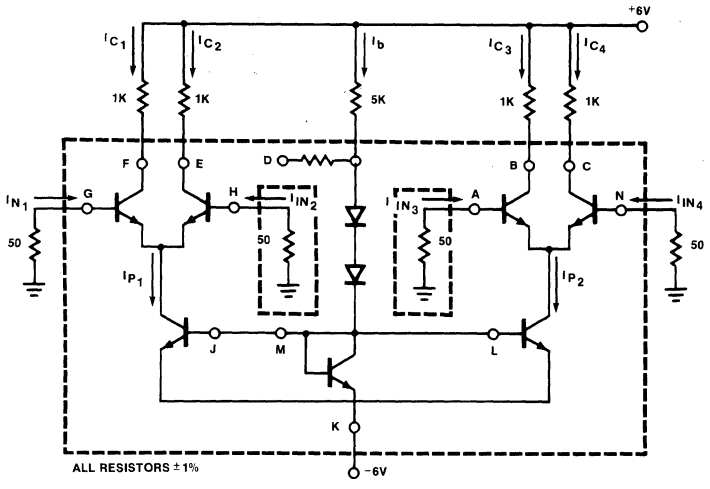


CONSTANT f_t CONTOURS—MHz



NOTE All characteristics for 25°C unless otherwise specified.

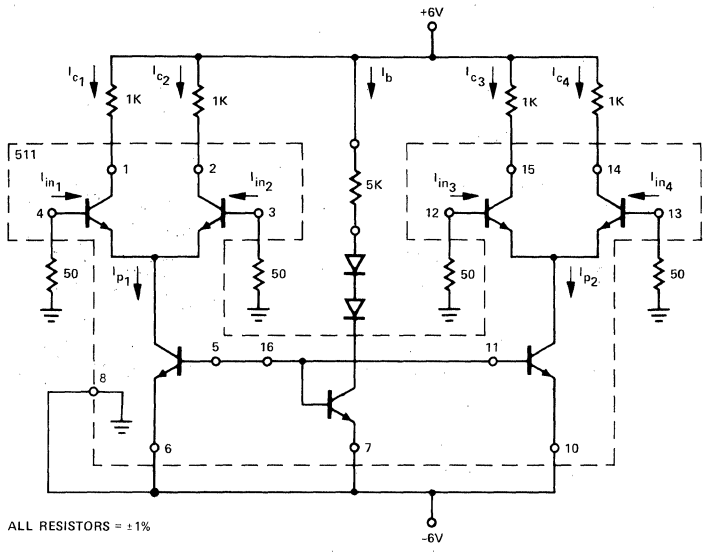
STANDARD TEST CIRCUIT (510)



$\Delta I_{IN} = I_{IN1} - I_{IN2}$
or
$I_{IN3} - I_{IN4}$
$\Delta I_C = I_{C1} - I_{C2}$
or
$I_{C3} - I_{C4}$
$\Delta I_P = I_{P1} - I_{P2}$
$I_{CC} = I_{C1} + I_{C2} + I_{C3} + I_{C4} + I_b$

Figure 1a

STANDARD TEST CIRCUIT (511)



$\Delta I_{IN} = I_{IN1} - I_{IN2}$
or
$I_{IN3} - I_{IN4}$
$\Delta I_C = I_{C1} - I_{C2}$
or
$I_{C3} - I_{C4}$
$\Delta I_P = I_{P1} - I_{P2}$
$I_{CC} = I_{C1} + I_{C2} + I_{C3} + I_{C4} + I_b$

Figure 1b

TEST LOAD CIRCUITS 510, 511

EMITTER COUPLED CONFIGURATION

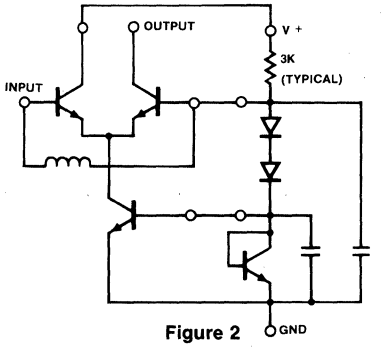


Figure 2

CASCODE CONFIGURATION

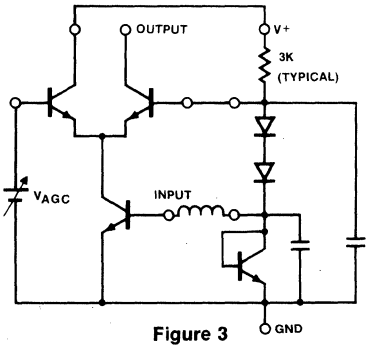


Figure 3

NE5501/5502/5503/5504-N

DESCRIPTION

These high-voltage, high-current Darlington transistor arrays are comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units feature open collector outputs and integral suppression diodes for inductive loads. Peak inrush currents to 600mA are allowable, making them ideal for driving tungsten filament lamps also.

The Type NE5501 is a general-purpose array which may be used with DTL, TTL, PMOS, CMOS, etc. It is pinned with inputs opposite outputs to facilitate ease of circuit board layout and is priced to compete directly with discrete transistor alternatives.

The Type NE5502 was specifically designed for use with 14 to 25V PMOS devices. Each input has a Zener diode and resistor in series in order to limit the input current to a safe value.

The Type NE5503 has a series base resistor to each Darlington pair, and thus allows operation directly with TTL or CMOS operating at a supply voltage of 5V.

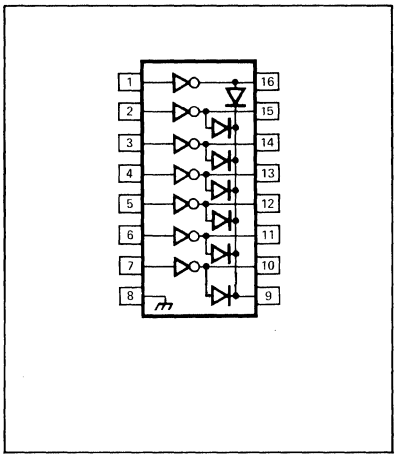
The Type NE5504 has an appropriate series input resistor to allow its operation directly from CMOS or PMOS outputs utilizing supply voltages of 6 to 15V. The required input current is below that of the Type NE5503 while the required input voltage is less than that required by the Type NE5502.

In all cases, the individual Darlington pair collector current rating is 500mA. However, outputs may be paralleled for higher load current capability. All devices are supplied in a 16-pin dual in-line plastic "N" package.

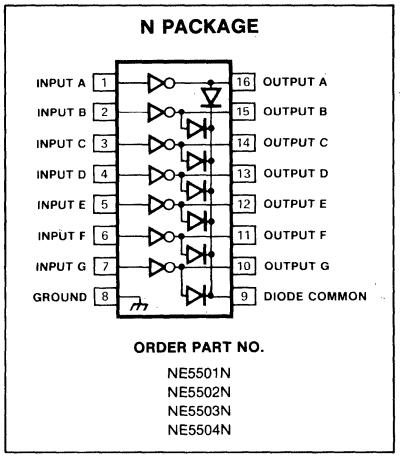
FEATURES

- **Output V_{CEO} > 100V**
- **Peak inrush current 600mA**
- **Protected internally against inductive loads**
- **Open collector topology**
- **Compatible with most logic technologies**

BLOCK DIAGRAM



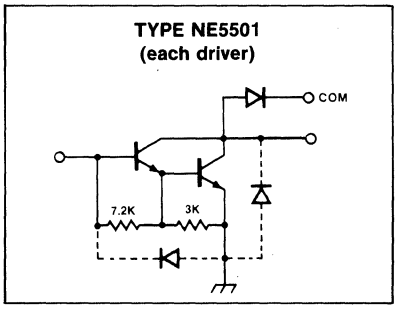
PIN CONFIGURATION

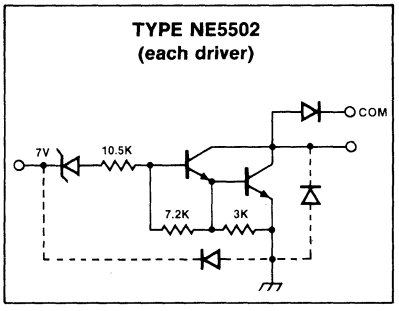


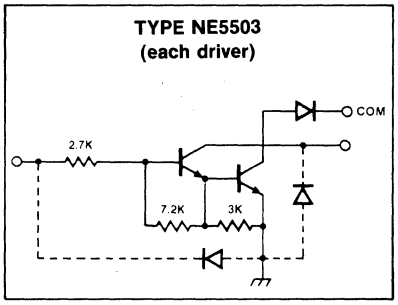
ORDER PART NO.

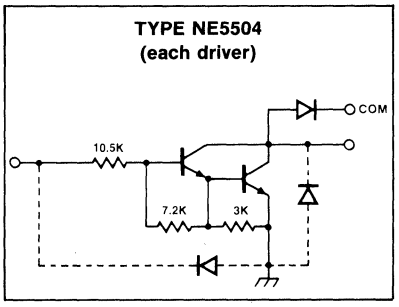
NE5501N
NE5502N
NE5503N
NE5504N

EQUIVALENT SCHEMATICS









ABSOLUTE MAXIMUM RATINGS[1,2]

PARAMETER		RATING	UNIT
V_{CE}	Output breakdown voltage	100	V
V_{IN}	Input voltage (except 5501)	30	V
V_{EBO}	Emitter base voltage	6	V
I_C	Continuous collector current	500	mA
I_B	Continuous base current	25	mA
P_D	Power dissipation	1.3	W
T_A	Ambient temperature	0 to +85	°C
T_{sg}	Storage temperature	-65 to +150	°C

NOTES

1. $T_A = 25°C$
2. Thermal resistivity, θjA, = 95°C/Watt.

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DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.[1,2,3]

PARAMETER		TEST CONDITIONS	NE5501			NE5502			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{CEX}	Output leakage current	$V_{CE} = 100V$, $T_A = 70°C$, Test Fig. 1A		0.1	10		—		μA
		$V_{CE} = 100V$, $T_A = 70°C$, $V_{IN} = 6V$, Test Fig. 1B		—			0.1	10	μA
V_{CESAT}	Collecter emitter saturation voltage	$I_C = 350mA$, $I_B = 500\mu A$, Test Fig. 2		1.6	2.0		1.6	2.0	V
		$I_C = 200mA$, $I_B = 350\mu A$, Test Fig. 2		1.2	1.6		1.2	1.6	V
		$I_C = 100mA$, $I_B = 250\mu A$, Test Fig. 2		1.0	1.4		1.0	1.4	V
I_{IN}	Input current (ON)	$V_{IN} = 17V$, Test Fig. 3		—			0.9	1.45	mA
I_{IN}	Input current (OFF)	$I_C = 500\mu A$, $T_A = 70°C$, Test Fig. 4	50	65		50	65		μA
V_{IN}	Input voltage (ON)	$V_{CE} = 2V$, $I_C = 300mA$, Test Fig. 5		—				13	V
h_{FE}	Forward current gain	$V_{CE} = 2V$, $I_C = 350mA$, Test Fig. 2	1000				—		
I_R	Clamp diode leakage	$V_R = 100V$, Test Fig. 6			10			10	μA
V_F	Clamp diode forward voltage	$I_F = 350mA$, Test Fig. 7		1.6	2.0		1.6	2.0	V

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$ unless otherwise specified.[1,2,3]

PARAMETER		TEST CONDITIONS	NE5503			NE5504			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{CEX}	Output leakage current	$V_{CE} = 100V$, $T_A = 70°C$, Test Fig. 1A		0.1	10		—		μA
		$V_{CE} = 100V$, $T_A = 70°C$, $V_{IN} = 1V$, Test Fig. 1B		—			0.1	10	μA
V_{CESAT}	Collecter emitter saturation voltage	$I_C = 350mA$, $I_B = 500\mu A$, Test Fig. 2		1.6	2.0		1.6	2.0	V
		$I_C = 200mA$, $I_B = 350\mu A$, Test Fig. 2		1.2	1.6		1.2	1.6	V
		$I_C = 100mA$, $I_B = 250\mu A$, Test Fig. 2		1.0	1.4		1.0	1.4	V
I_{IN}	Input current (ON)	$V_{IN} = 3.85V$, Test Fig. 3		1.05	1.65		—		mA
		$V_{IN} = 5V$, Test Fig. 3		—			0.4	0.65	mA
		$V_{IN} = 12V$, Test Fig. 3		—			1.1	1.7	mA
I_{IN}	Input current (OFF)	$I_C = 500\mu A$, $T_A = 70°C$, Test Fig. 4	50	65		50	65		μA
V_{IN}	Input voltage (ON)	$V_{CE} = 2V$, $I_C = 200mA$, Test Fig. 5			2.4		—		V
		$V_{CE} = 2V$, $I_C = 250mA$, Test Fig. 5			2.7		—		V
		$V_{CE} = 2V$, $I_C = 300mA$, Test Fig. 5			3.0		—		V
V_{IN}	Input voltage (ON)	$V_{CE} = 2V$, $I_C = 125mA$, Test Fig. 5						5.0	V
		$V_{CE} = 2V$, $I_C = 200mA$, Test Fig. 5						6.0	V
		$V_{CE} = 2V$, $I_C = 275mA$, Test Fig. 5						7.0	V
		$V_{CE} = 2V$, $I_C = 350mA$, Test Fig. 5						8.0	V
I_R	Clamp diode leakage	$V_R = 100V$, Test Fig. 6			10			10	μA
V_F	Clamp diode forward voltage	$I_F = 350mA$, Test Fig. 7		1.6	2.0		1.6	2.0	V

NOTES

1. All limits stated apply to the complete Darlington series except as specified for a single device type.
2. The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
3. The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

PARAMETER		TO	FROM	TEST CONDITIONS	NE5501			NE5502			UNIT
					Min	Typ	Max	Min	Typ	Max	
C_{IN}	Input capacitance					15	30		15	30	pF
T_{PLH}	Turn on delay	Input	Output	50% E_{IN} to 50% E_{OUT}		1	5		1	5	μs
T_{PHL}	Turn off delay	Input	Output	50% E_{IN} to 50% E_{OUT}		1	5		1	5	μs

AC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$ unless otherwise specified.

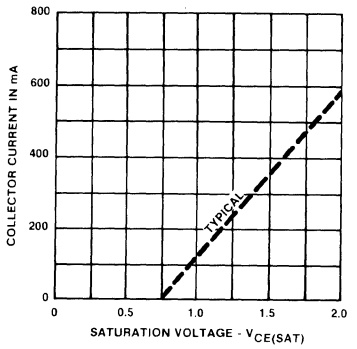
PARAMETER		TO	FROM	TEST CONDITIONS	NE5503			NE5504			UNIT
					Min	Typ	Max	Min	Typ	Max	
C_{IN}	Input capacitance					15	30		15	30	pF
T_{PLH}	Turn on delay	Input	Output	50% E_{IN} to 50% E_{OUT}		1	5		1	5	μs
T_{PHL}	Turn off delay	Input	Output	50% E_{IN} to 50% E_{OUT}		1	5		1	5	μs

NOTES

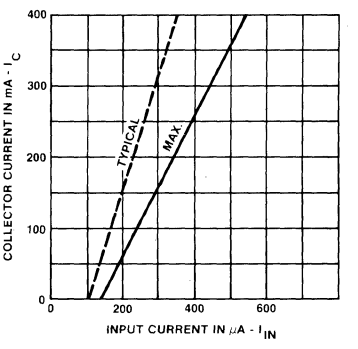
1. All limits stated apply to the complete Darlington series except as specified for a single device type.
2. The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
3. The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

TYPICAL PERFORMANCE CHARACTERISTICS

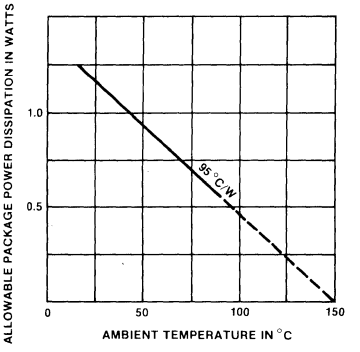
COLLECTOR CURRENT AS A FUNCTION OF SATURATION VOLTAGE



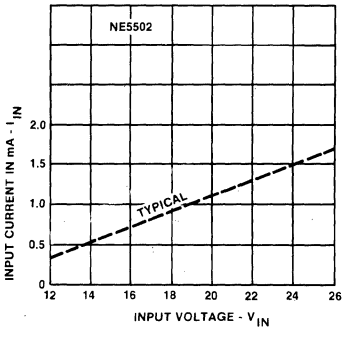
COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT



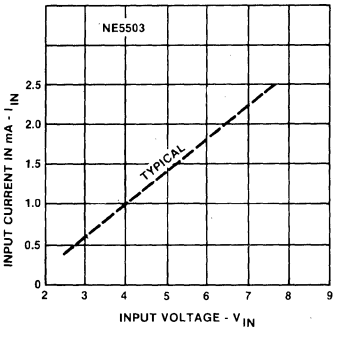
ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



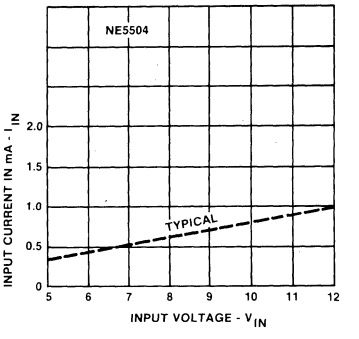
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE FOR TYPE NE5502



INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE FOR TYPE NE5503



INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE FOR TYPE NE5504



TEST LOAD CIRCUITS

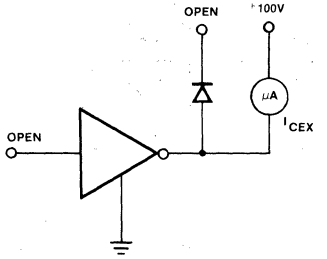


Figure 1A

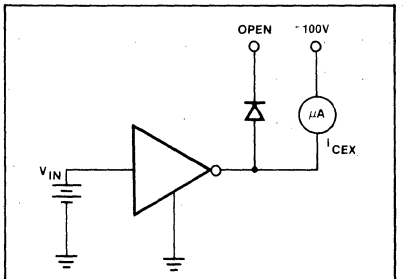


Figure 1B

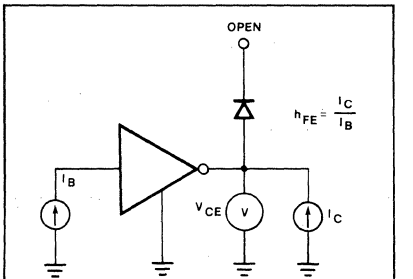


Figure 2

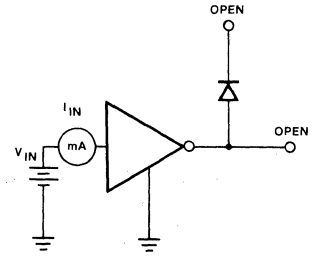


Figure 3

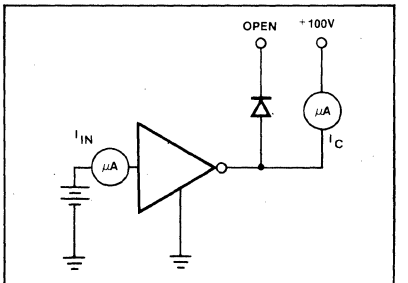


Figure 4

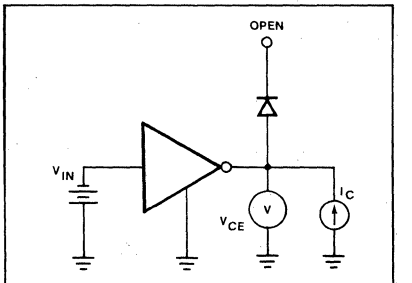


Figure 5

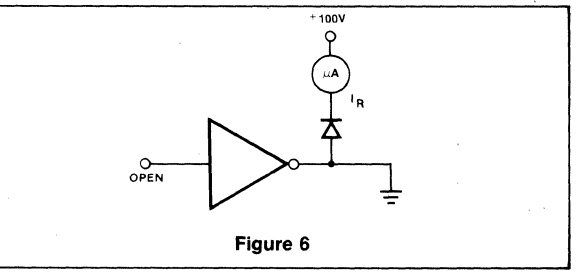


Figure 6

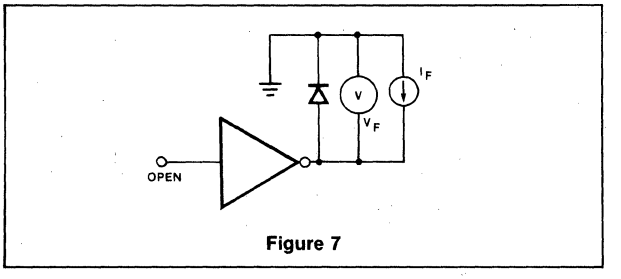
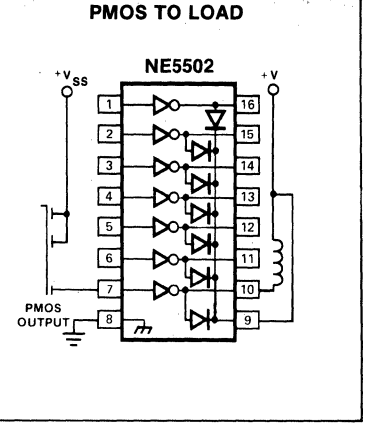
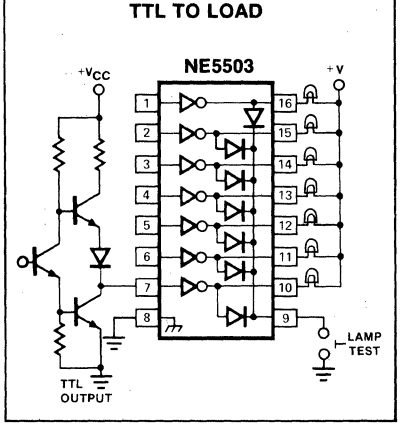
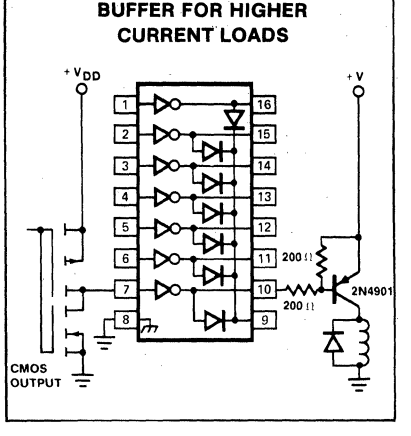


Figure 7

TYPICAL APPLICATIONS







DESCRIPTION

These high-voltage, high-current Darlington transistor arrays are comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units feature open collector outputs and integral suppression diodes for inductive loads. Peak inrush currents to 600mA are allowable, making them ideal for driving tungsten filament lamps also.

The Type ULN-2001 is a general-purpose array which may be used with DTL, TTL, PMOS, CMOS, etc. It is pinned with inputs opposite outputs to facilitate ease of circuit board layout and is priced to compete directly with discrete transistor alternatives.

The Type ULN-2002 was specifically designed for use with 14 to 25V PMOS devices. Each input has a Zener diode and resistor in series in order to limit the input current to a safe value.

The Type ULN-2003 has a series base resistor to each Darlington pair, and thus allows operation directly with TTL or CMOS operating at a supply voltage of 5V.

The Type ULN-2004 has an appropriate series input resistor to allow its operation directly from CMOS or PMOS outputs utilizing supply voltages of 6 to 15V. The required input current is below that of the Type ULN-2003 while the required input voltage is less than that required by the Type ULN-2002.

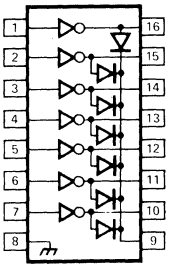
In all cases, the individual Darlington pair collector current rating is 500mA. However, outputs may be paralleled for higher load current capability. All devices are supplied in a 16-pin dual in-line plastic "BA" package.

FEATURES

- **Peak inrush current 600mA**
- **Protected internally against inductive loads**
- **Open collector topology**
- **Compatible with most logic technologies**

PIN CONFIGURATION

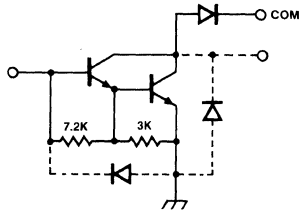
N PACKAGE



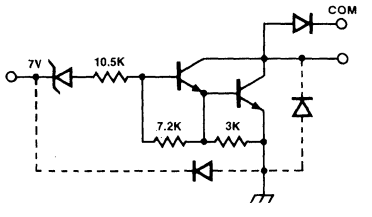
ORDER PART NO.
ULN2001N
ULN2002N
ULN2003N
ULN2004N

EQUIVALENT SCHEMATICS

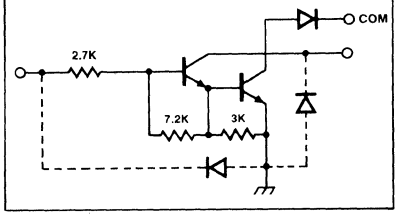
TYPE ULN2001
(each driver)



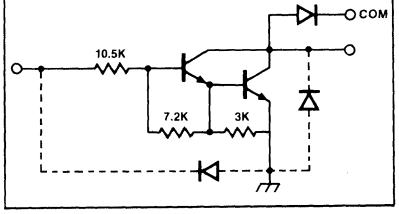
TYPE ULN2002
(each driver)



TYPE ULN2003
(each driver)



TYPE ULN2004
(each driver)



ABSOLUTE MAXIMUM RATINGS

at 25°C Free-Air temperature for any one Darlington pair unless otherwise specified.

PARAMETER		RATING	UNIT
V_{CE}	Output voltage	50	V
V_{IN}	Input voltage	30	V
V_{EBO}	Emitter base voltage	6	V
I_C	Continuous collector current	500	mA
I_B	Continuous base current	25	mA
P_D	Power dissipation	1.3	W
	Derating factor above 25°C	95	°C/W
T_A	Ambient temperature range (operating)	0 to +85	°C
T_S	Storage temperature range	-65 to +150	°C

*NOTE
Under normal operating conditions, these units will sustain 350mA per output with $V_{CE(SAT)}$ = 1.6V at 70°C with a pulse width of 20 ms and a duty cycle of 30%.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.[1,2,3]

PARAMETER		TEST CONDITIONS	Test Fig.	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
I_{CEX}	Output leakage current	$V_{CE} = 50V$, $T_A = 70°C$	1A	—	—	100	μA
	Type ULN-2002	$V_{CE} = 50V$, $T_A = 70°C$, $V_{IN} = 6V$	1B	—	—	500	μA
	Type ULN-2004	$V_{CE} = 50V$, $T_A = 70°C$, $V_{IN} = 1V$	1B	—	—	500	μA
$V_{CE(SAT)}$	Collector-emitter Saturation voltage	$I_C = 350mA$, $I_B = 500\mu A$	2	—	1.25	1.6	V
		$I_C = 200mA$, $I_B = 350\mu A$	2	—	1.1	1.3	V
		$I_C = 100mA$, $I_B = 250\mu A$	2	—	0.9	1.1	V
$I_{IN(ON)}$	Input current						
	Type ULN-2002	$V_{IN} = 17V$	3	—	0.85	1.3	mA
	Type ULN-2003	$V_{IN} = 3.85V$	3	—	0.93	1.35	mA
	Type ULN-2004	$V_{IN} = 5V$	3	—	0.35	0.5	mA
		$V_{IN} = 12V$	3	—	1.0	1.45	mA
$I_{IN(OFF)}$	Input current	$I_C = 500\mu A$, $T_A = 70°C$	4	50	65	—	μA
$V_{IN(ON)}$	Input voltage						
	Type ULN-2002	$V_{CE} = 2V$, $I_C = 300mA$	5	—	—	13	V
	Type ULN-2003	$V_{CE} = 2V$, $I_C = 200mA$	5	—	—	2.4	V
		$V_{CE} = 2V$, $I_C = 250mA$	5	—	—	2.7	V
		$V_{CE} = 2V$, $I_C = 300mA$	5	—	—	3.0	V
	Type ULN-2004	$V_{CE} = 2V$, $I_C = 125mA$	5	—	—	5.0	V
		$V_{CE} = 2V$, $I_C = 200mA$	5	—	—	6.0	V
		$V_{CE} = 2V$, $I_C = 275mA$	5	—	—	7.0	V
		$V_{CE} = 2V$, $I_C = 350mA$	5	—	—	8.0	V
h_{FE}	D-C forward current transfer ratio Type ULN-2001	$V_{CE} = 2V$, $I_C = 350mA$	2	1000		—	—
C_{IN}	Input capacitance		—	—	15	30	pF
I_R	Clamp diode leakage current	$V_R = 50V$	6	—	—	50	μA
V_F	Clamp diode forward voltage	$I_F = 350mA$	7	—	1.7	2	V

NOTES

1. All limits stated apply to the complete Darlington series except as specified for a single device type.
2. The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
3. The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.[1,2,3]

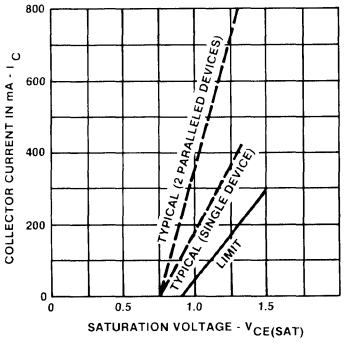
PARAMETER		TEST CONDITIONS	Test Fig.	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
t_{PLH}	Turn-on delay	0.5 E_{IN} to 0.5 E_{OUT}	—	—	1.0	5	μs
t_{PHL}	Turn-off delay	0.5 E_{IN} to 0.5 E_{OUT}	—	—	1.0	5	μs

NOTES

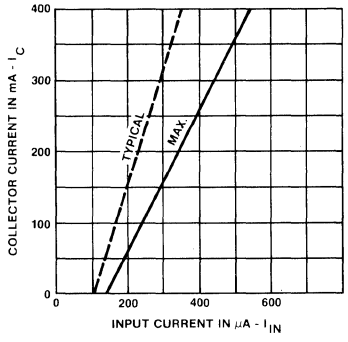
1. All limits stated apply to the complete Darlington series except as specified for a single device type.
2. The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
3. The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

TYPICAL PERFORMANCE CHARACTERISTICS

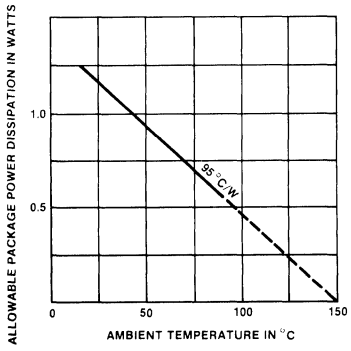
COLLECTOR CURRENT AS A FUNCTION OF SATURATION VOLTAGE



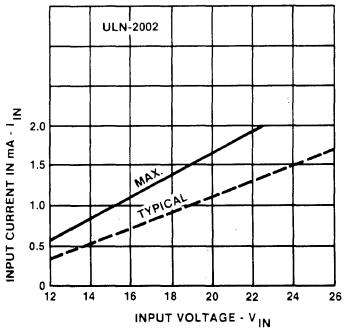
COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT



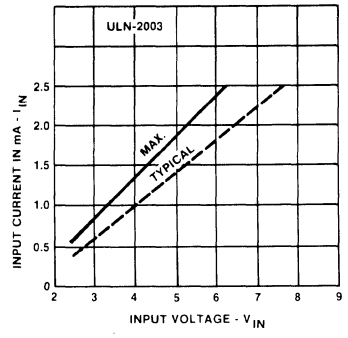
ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



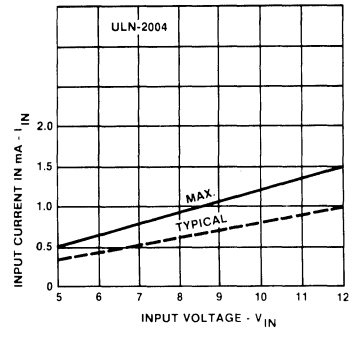
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE FOR TYPE ULN-2002



INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE FOR TYPE ULN-2003



INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE FOR TYPE ULN-2004



TEST FIGURES

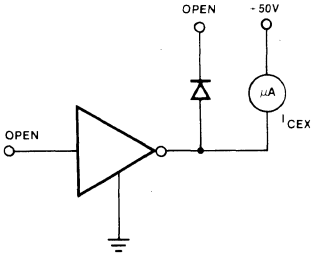


Figure 1A

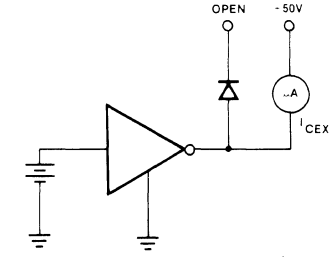


Figure 1B

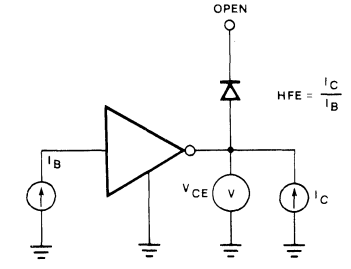


Figure 2

TEST FIGURES (Cont'd)

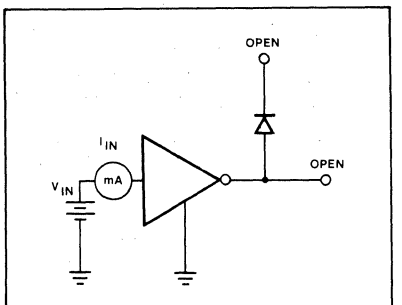


Figure 3

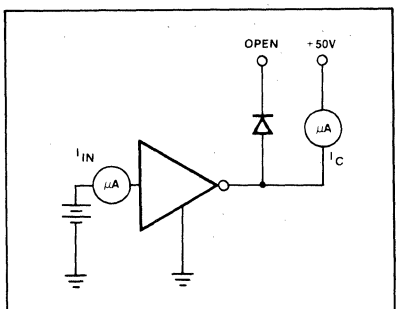


Figure 4

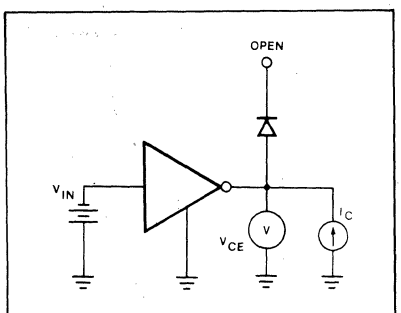


Figure 5

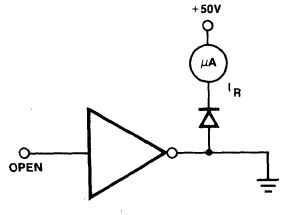


Figure 6

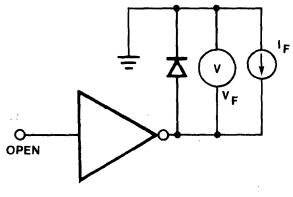
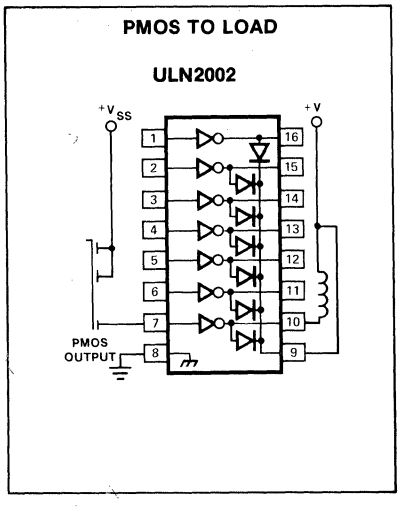
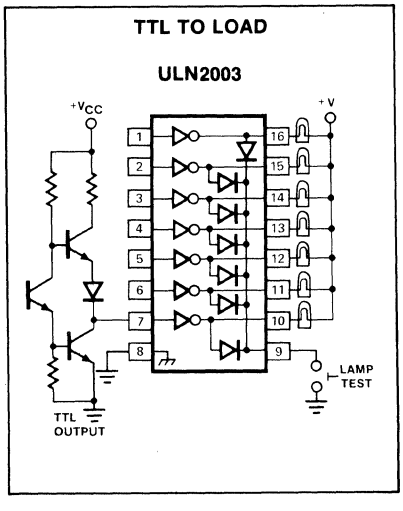
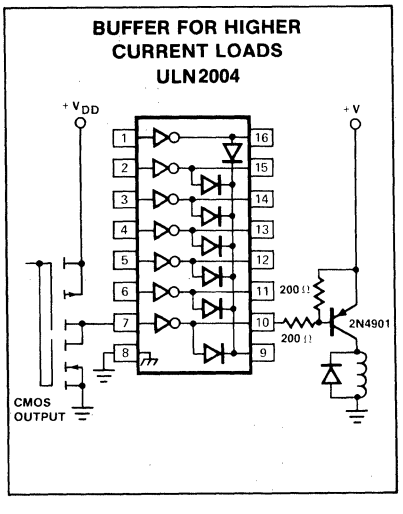


Figure 7

TYPICAL APPLICATIONS







CA3081/3082-N

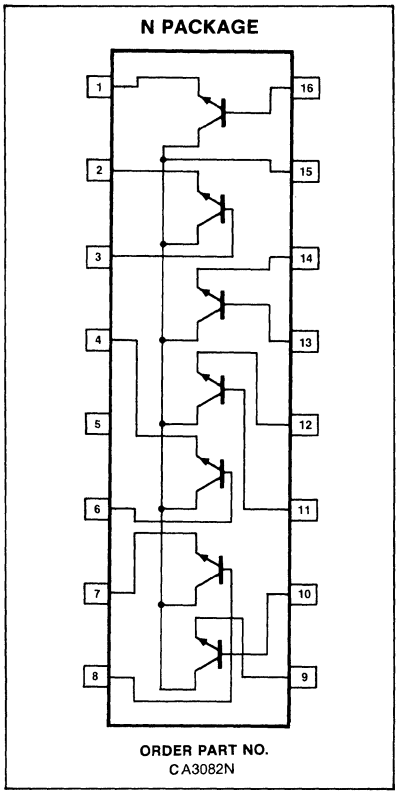
DESCRIPTION

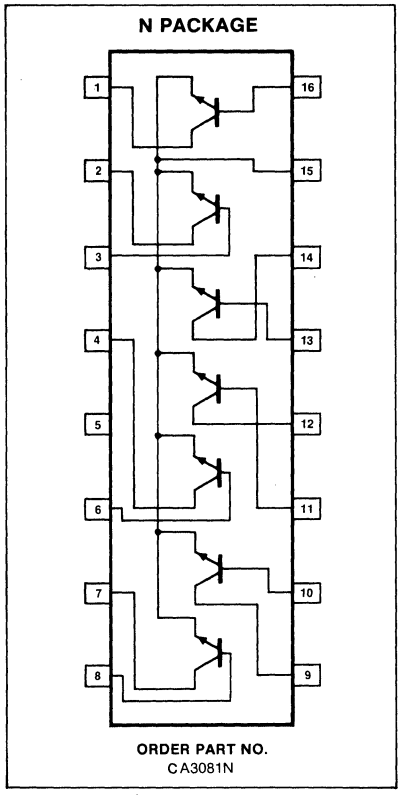
The CA3081 and CA3082 are monolithic integrated circuits each consisting of seven separate npn transistors on a common substrate. The transistors are capable of driving loads up to 100mA. At the same time the transistor geometry used gives maximum current gain at quite low currents, making the devices also suitable for small signal applications. In the CA3081 the transistors are connected in common emitter configuration while in the CA3082 the collectors are common. The transistor arrays are particularly suitable for driving light-emitting diodes and seven-segment displays as well as for general purpose applications.

FEATURES

- **V_{CBO}=50V**
- **V_{CEO}=35V**
- **Collector current 100mA**
- **Common emitter or common collector configuration**

PIN CONFIGURATIONS





ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CEO}	Collector-emitter voltage (open base)	35	V
V_{CBO}	Collector-base voltage (open emitter)	50	V
V_{CSO}	Collector-substrate voltage (open base and emitter)	50	V
V_{EBO}	Emitter-base voltage (open collector)	6	V
I_C	Collector current (dc)	100	mA
I_B	Base current (dc)	20	mA
P	Power dissipation:	500	mW
	any one transistor		
P_{TOT}	total package (see derating curve)	750	mW
T_A	Operating ambient temperature	-40 to +125	°C
T_{stg}	Storage temperature	-50 to +125	°C
T_j	Junction temperature	125	°C
	Lead temperature (10 sec)	300	°C

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	CA3081/3082			UNIT
		Min	Typ	Max	
V_{CEO} Collector-emitter breakdown voltage	$I_C = 1mA$, $I_B = 0$	35			V
V_{CSO} Collector-substrate breakdown voltage	$I_C = 1mA$, $I_B = 0$, $I_E = 0$	50			V
V_{CBO} Collector-base breakdown voltage	$I_C = 10\mu A$, $I_E = 0$	50			V
V_{EBO} Emitter-base breakdown voltage	$I_E = 10\mu A$, $I_C = 0$	6.5	7.0	7.5	V
hfe DC current gain	$I_E = 10\mu A$, $V_{CE} = 5V$ $I_E = 1mA$, $V_{CE} = 5V$ $I_E = 20mA$, $V_{CE} = 5V$	50 50 30		300 300 200	
V_{SAT} Saturation voltage	$I_C = 5mA$, $I_B = .5mA$ $I_C = 50mA$, $I_B = 5mA$		0.2 0.4	0.4 0.8	V V

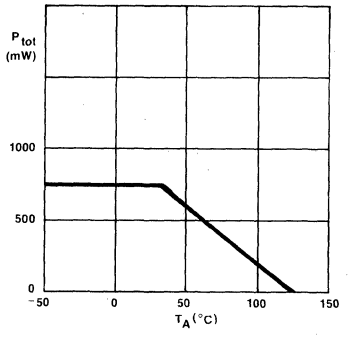
NOTE

As each collector forms a parasitic diode with the substrate, the substrate has to be connected to a voltage which is lower than the lowest collector voltage.

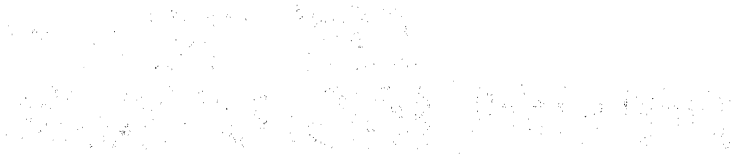
To avoid parasitic coupling between the transistors, the substrate (pin 5) should be connected to signal ground.

TYPICAL PERFORMANCE CHARACTERISTICS

POWER DISSIPATION DERATING CURVE



SECTION 9
PHILIPS INDUSTRIAL



NE502-N

DESCRIPTION

The NE502 is a MOS monolithic integrated circuit, generally intended to delay analogue signals (e.g. delay time = $512/2f_0$).

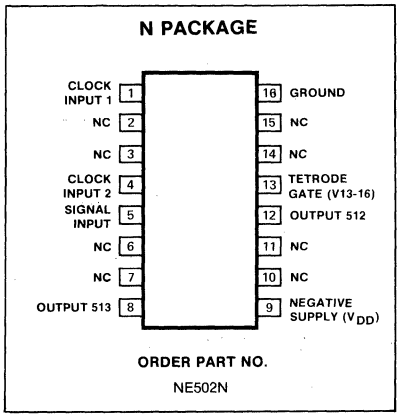
It can be used with clock frequencies in the range 5kHz to 500kHz.

The device contains 512 stages, so the input signal can be delayed from 51.2ms to 0.512ms.

APPLICATIONS

- **Fixed analog delay**
- **V_{ox} control**
- **Equalizing speech delay in PA systems**
- **Vibrato and chorus effects**
- **Reverberation**
- **Variable compression/expansion of speech**
- **Speech scrambling and time scale conversion**

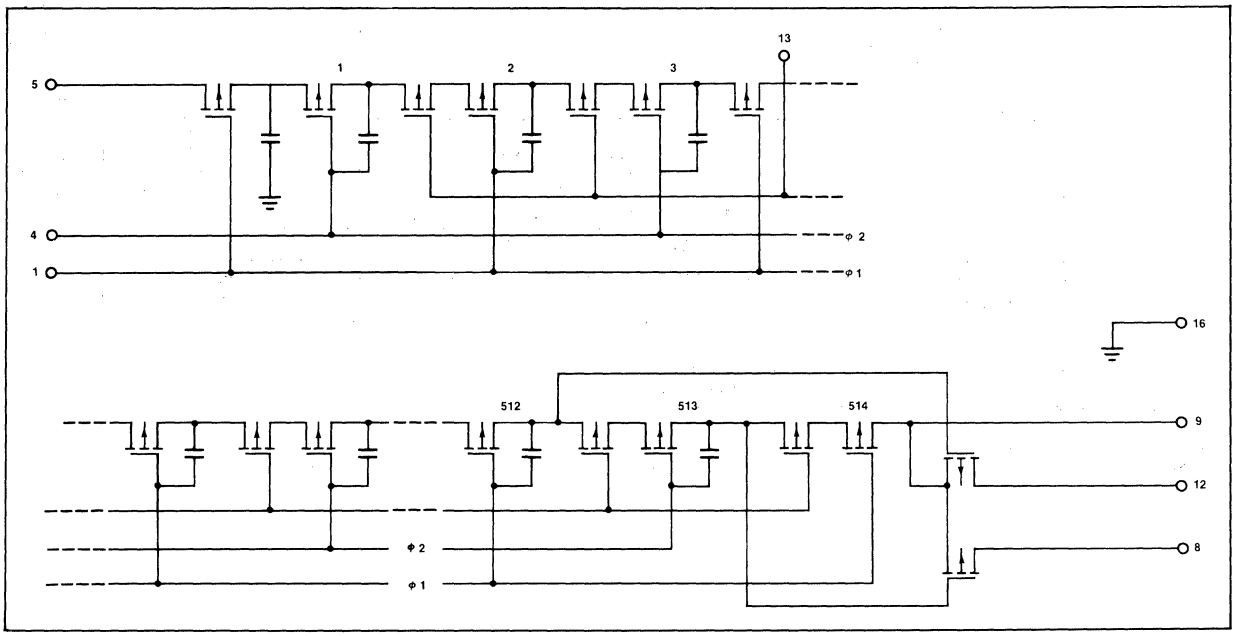
PIN CONFIGURATION



FEATURES

- **5 to 500kHz clock frequency**
- **512 stages**
- **Signal delay of 51.2 to .512ms**
- **Signal frequency to 45kHz**

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
	Voltages*		
V_{9-16}	Supply voltage	0 to -20	V
	Clock input, data input, output voltage and V_{13-16}	0 to -18	V
	Current		
I_8, I_{12}	Output current	0 to +5	mA
	Temperatures		
T_{STG}	Storage temperature	-40 to +150	°C
T_A	Operating ambient temperature	-20 to +85	°C

*NOTE

Though MOS integrated circuits incorporate protection against electrostatic discharge, they can nevertheless be damaged by accidental over-voltages. To be totally safe, it is desirable to take handling precautions into account.

DC ELECTRICAL CHARACTERISTICS

T_A = -20°C to +55°C, V_{DD} = -15V, $V\phi_1 = V\phi_2$ = -15V, V_{13-16} = -14V, R_L = 47kΩ unless otherwise specified.

PARAMETER		TEST CONDITIONS	NE502			UNIT
			Min	Typ	Max	
V_{DD}	Supply voltage[1]		-18		-10	V
I_{DD}	Supply current			.3		mA
$V\phi_{1H}$, $V\phi_{2H}$	Clock voltage high		-1.5		0	V
$V\phi_{1L}$, $V\phi_{2L}$	Clock voltage low[1]		-18	-15	-10	V
V_{IN}	Input voltage	$V_{OUT} \leq$ 1% THD		2.5		Vrms
R_L	Load resistance[1]		10	47		kΩ

AC ELECTRICAL CHARACTERISTICS

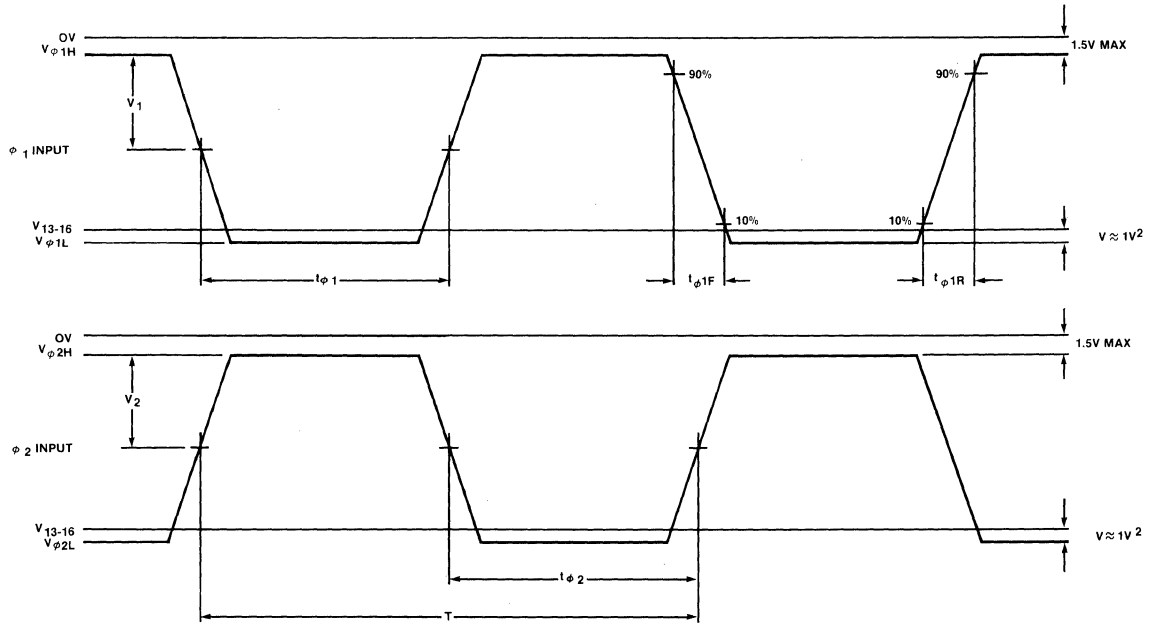
T_A = -20°C to +55°C, V_{DD} = -15V, $V\phi_1 = V\phi_2$ = -15V, V_{13-16} = -14V, R_L = 47kΩ unless otherwise specified.

PARAMETER		TEST CONDITIONS	NE502			UNIT
			Min	Typ	Max	
$f\phi_1$, $f\phi_2$	Clock frequency[2]		5		500	kHz
$T\phi_1$, $T\phi_2$	Clock pulse width[3]				.5	T
$T_r\phi_1$, $T_r\phi_2$	Clock rise time[3]			0.05		T
$T_f\phi_1$, $T_f\phi_2$	Clock fall time[3]			0.05		T
f_S	Signal frequency		0		45	kHz
	Signal attenuation[1]	$f\phi$ = 40kHz, f_S = 1kHz		4	7	dB
	Output signal variation	f_S = 1kHz, V_S = 1Vrms, 5kHz ≤ $f\phi$ ≤ 100kHz		.5	1	dB
	Output signal variation	f_S = 1kHz, V_S = 1Vrms, 100kHz ≤ $f\phi$ ≤ 300kHz		.5	1	dB
ΔV_{OUT}	DC voltage shift	5kHz ≤ $f\phi$ ≤ 300kHz			.5	V
V_N	Noise voltage	$f\phi$ = 100kHz (weighted by "A" curve)		.25		mVrms
S/N	Signal to noise			74		dB

NOTES

1. It is recommended that $V_{13-16} = V\phi_{1L} + 1V = V\phi_{2L} + 1V$; V_{DD} more negative than $V\phi_L$.
2. In theory the clock frequency must be higher than twice the highest signal frequency; in practice $f_S \leq 0.3f\phi$ to $0.5f\phi$ is recommended, depending on the characteristics of the output filter.
3. T = period time = $1/f\phi$. The data on fall and rise times are given to eliminate overlap between the two clock pulses. To be independent of these rise and fall times a clock generator with simple gating can be used. See also pages 5 and 8.

TIMING DIAGRAM

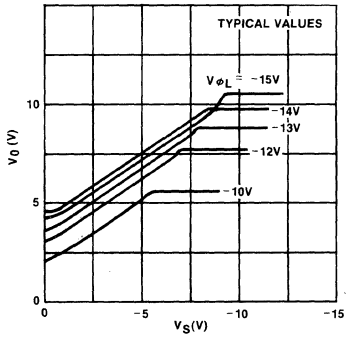


NOTES

1. $|V_1 + V_2| \leq |V\phi_{1L}| = V\phi_{2L}$.
2. For maximum dynamic range adjust V_{13-16} so that $\Delta V = V_{13-16} - V\phi_L \simeq 1V$.

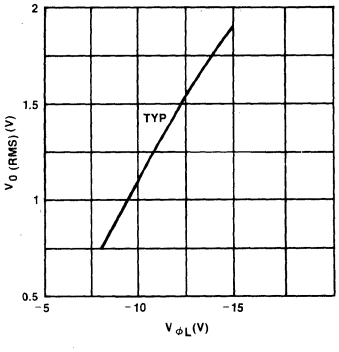
TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT VOLTAGE vs SIGNAL VOLTAGE



V_{DD} = -15V
V_{13-16} = -14V
$V\phi_H$ = 0V
$f\phi$ = 40kHz
R_L = 47kΩ

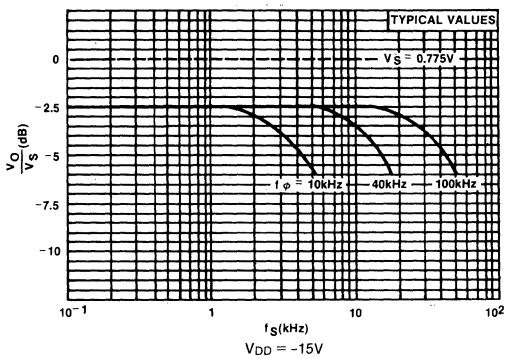
V_{OUT} vs $V_{\phi LOW}$



V_{DD} = -15V
V_{13-16} = -14V
$V\phi_H$ = 0V
$f\phi$ = 40kHz
f_s = 1kHz
R_L = 47kΩ

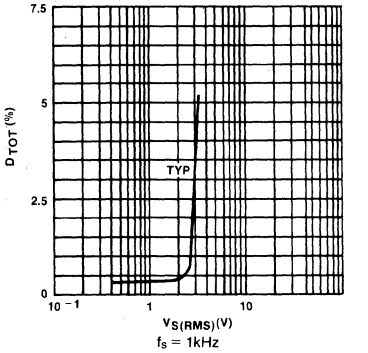
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

OUTPUT ATTENUATION



V_{DD} = -15V
V_{13-16} = -14V
$V\phi$ = 0 to -15V

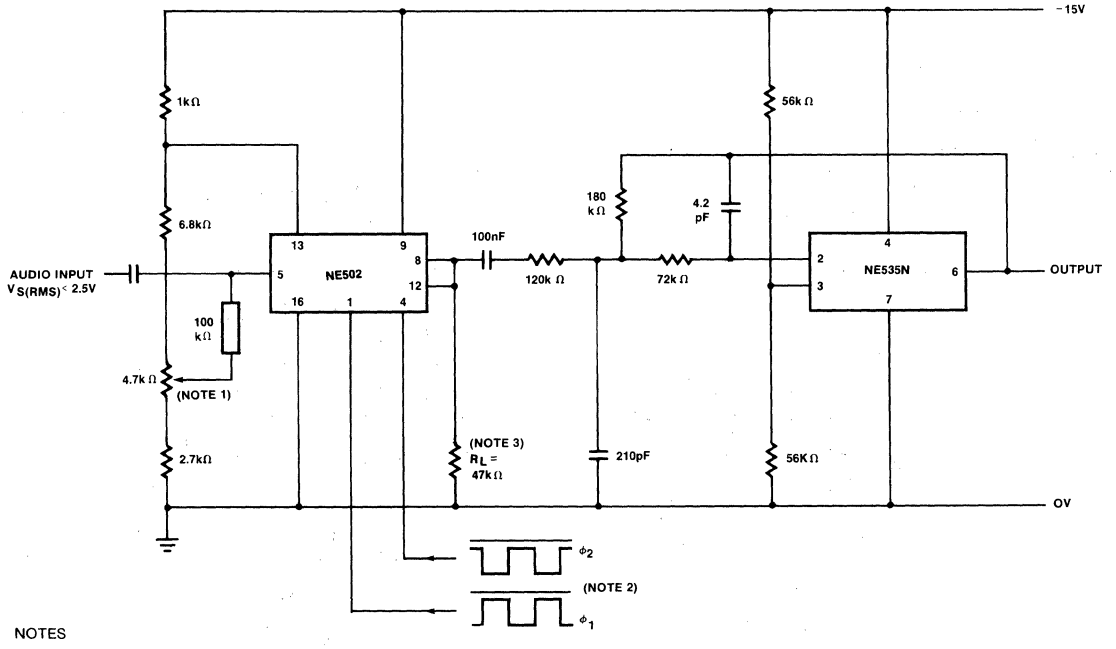
DISTORTION vs INPUT SIGNAL LEVEL



f_s = 1kHz
V_s = -5, 2V
V_{DD} = -15V
V_{13-16} = -14V
$V\phi$ = 0 to -15V
$f\phi$ = 40kHz

TYPICAL APPLICATIONS

SINGLE DELAY LINE CONNECTION

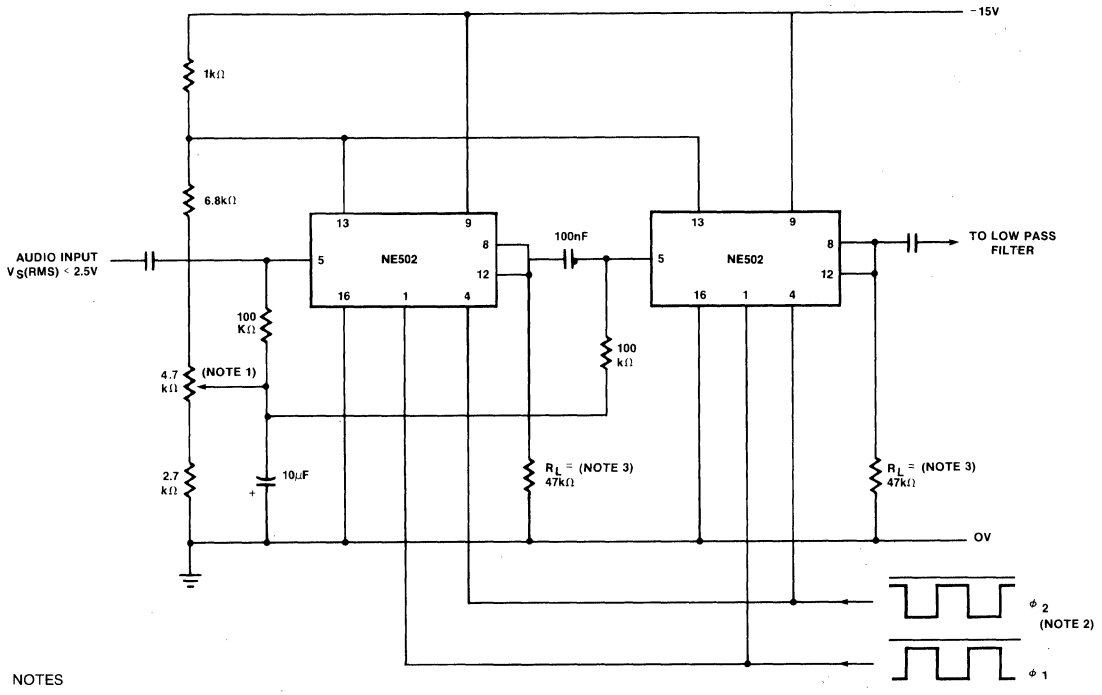


NOTES

1. Adjust dc voltage for class-A operation (≈ 5V).
   Conditions: low pass filter μA741CV (12dB per octave);
   gain = +3.5dB (compensation for line attenuation);
   $f\phi$ = 50kHz (min.);
   cut-off frequency = 15kHz.
2. Clock input voltage amplitude: V_{CL} = -15V.
3. Can be replaced by a current source of 100 to 400μA.

TYPICAL APPLICATIONS (Cont'd)

SERIES CONNECTION OF TWO LINES NE502

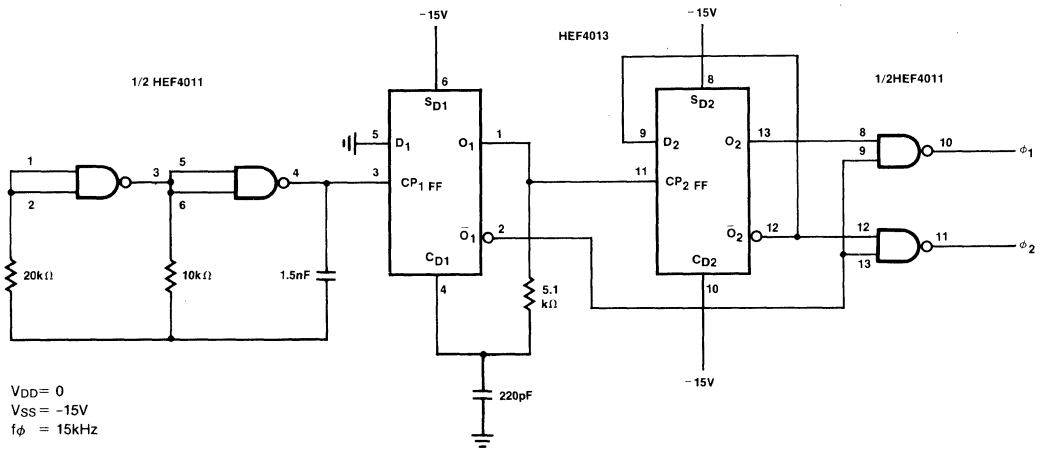


NOTES

1. Adjust dc voltage for class-A operation (≈ 5V).
2. Clock input voltage amplitude: V_{CL} = -15V.
3. Can be replaced by a current source of 100 to 400μA (see also note 1 on page 4).

TYPICAL APPLICATIONS (Cont'd)

CLOCK OSCILLATOR AND DRIVER CIRCUIT WITH ELIMINATION OF OVERLAP (FOR MAX. 6xNE502)



V_{DD} = 0
V_{SS} = -15V
f_ϕ = 15kHz

SAA1027-N

DESCRIPTION

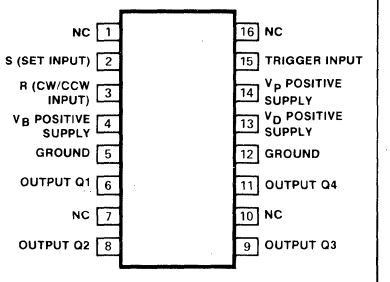
The SAA1027 is intended for driving a four phase two stator stepper motor. The circuit consists of four output stages, a logic part and three input stages. The logic part is driven by three input stages; a trigger input stage, an input stage which can change the switching sequence of the logic part so that the motor can rotate clock wise (CW) or counter clock wise (CCW) and a set input stage to set the four output stages. The three inputs are compatible with high noise immunity logic to ensure proper operation, even in noisy environments. The output can deliver 350mA in each phase. The right switching sequence of the four phases is obtained from the logic part of the circuit. Integrated diodes protect the outputs against transient spikes.

FEATURES

- **CW or CCW rotation**
- **4-phase drive**
- **Few external components**

PIN CONFIGURATION

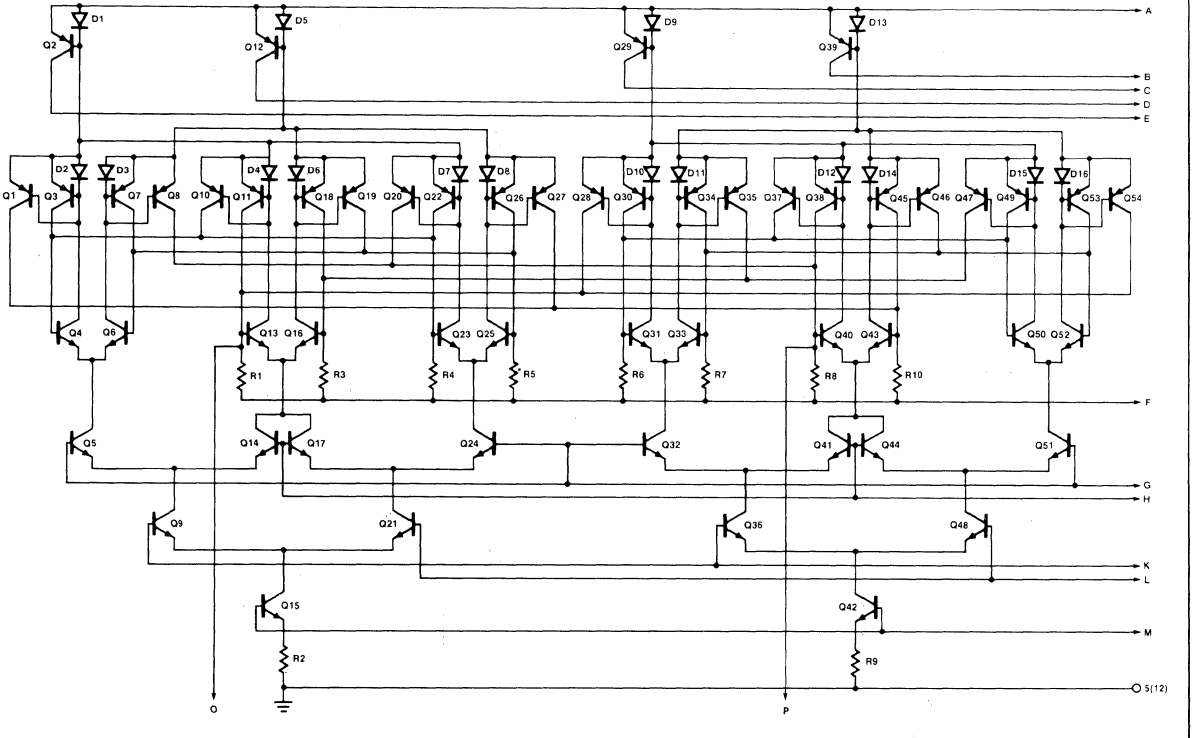
N PACKAGE



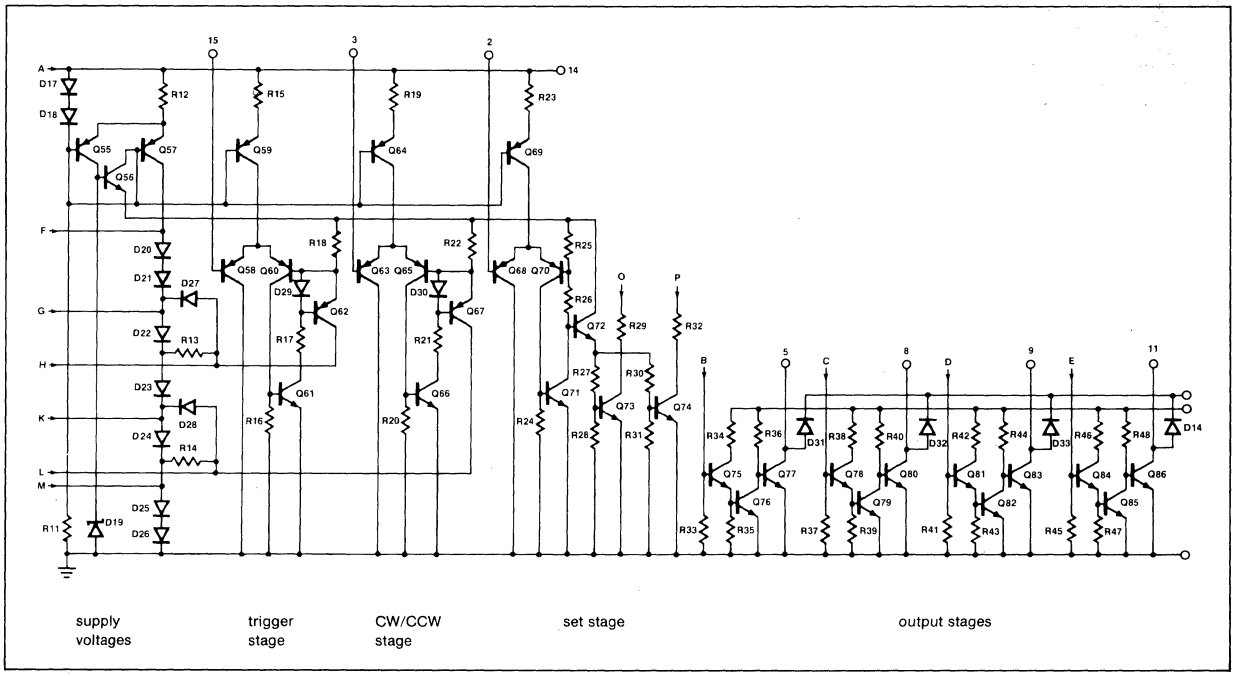
ORDER PART NO.
SAA1027N

EQUIVALENT SCHEMATIC

BI-DIRECTIONAL, 4 POSITION, SYNCHRONOUS COUNTER



EQUIVALENT SCHEMATIC (Cont'd)



ABSOLUTE MAXIMUM RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

	PARAMETER	RATING	UNIT
	VOLTAGES		
V_P	Supply voltage (pin 4, 13, 14)	20	V
V_I	Input voltage; R (pin 3), S (pin 2), T (pin 15)	20	V
	CURRENT		
I_Q	Output current; Q_1 (pin 6), Q_2 (pin 8), Q_3	500	mA
	POWER DISSIPATION	See figure 1	
	TEMPERATURES		
T_{STG}	Storage temperature	-40 to +125	°C
T_A	Operating ambient temperature	-20 to +70	°C
	THERMAL RESISTANCE		
θ_{ja}	From junction to ambient	70	°C/W

*NOTE

Additional power caused by the self-inductance of the motor-coils will be dissipated in the diodes (D31 to D34).

TRUTH TABLE[1,2]

S = H									
R = H					R = L				
T	Q1	Q2	Q3	Q4	T	Q1	Q2	Q3	Q4
0	L	H	L	H	0	L	H	L	H
1	H	L	L	H	1	L	H	H	L
2	H	L	H	L	2	H	L	H	L
3	L	H	H	L	3	H	L	L	H
4	L	H	L	H	4	L	H	L	H

Trigger Conditions(T)

NOTES

1. Direction conditions (R)
   The direction of rotation can be changed at any moment independent of the state of the T and S inputs.
2. Set conditions (S)
   When T is HIGH and S LOW then the outputs are set: $Q_1 = L$, $Q_2 = H$, $Q_3 = L$, $Q_4 = H$.

DC ELECTRICAL CHARACTERISTICS $-20°C \leq T_A \leq 65°$, $V_P = 12V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SAA1027			UNIT
			Min	Typ	Max	
V_P	Supply voltage (pin 14)		9.5	12	18	V
I_P	Supply current	Pin 4 open, without loads, all inputs high	2.0	4.5	6.5	mA
V_{IH}		R, S, T inputs	7.5			V
I_{IH}		R, S, T inputs		1		μA
V_{IL}		R, S, T inputs			4.5	V
I_{IL}		R, S, T inputs		30		μA
V_Q	Supply voltage	Each output stage	1.5	12	18	V
I_Q	Supply current	Each output stage			350	mA
V_{SAT}	Saturation voltage				1	V
	Bias voltage and current	Reference Figure 2.				
	Bias resistor	Reference Figure 3.				
	Bias resistor power dissipation	Reference Figure 4.				
	Device power dissipation	Reference Figure 5.				

TYPICAL PERFORMANCE CHARACTERISTICS

POWER DISSIPATION DERATING CURVE

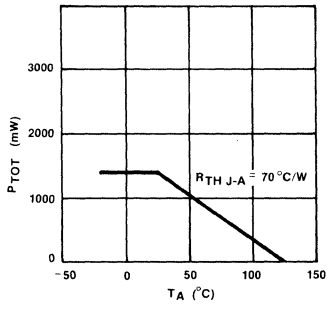


Figure 1

BIAS VOLTAGE AND CURRENT

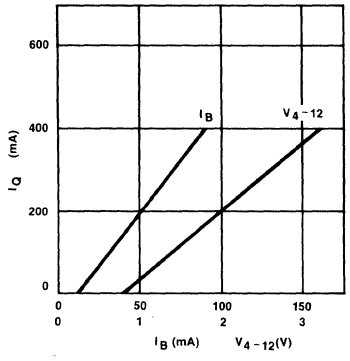


Figure 2

BIAS RESISTOR

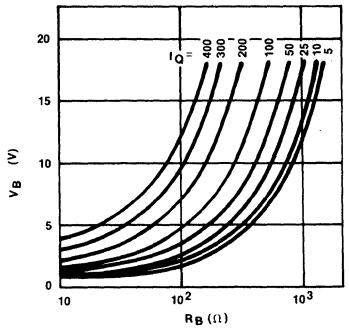


Figure 3

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

BIAS RESISTOR POWER DISSIPATION

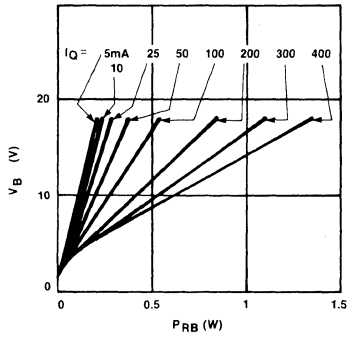


Figure 4

TOTAL DEVICE POWER DISSIPATION

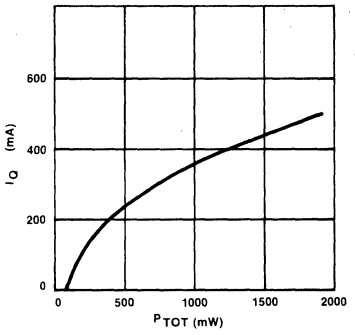


Figure 5

TYPICAL APPLICATIONS

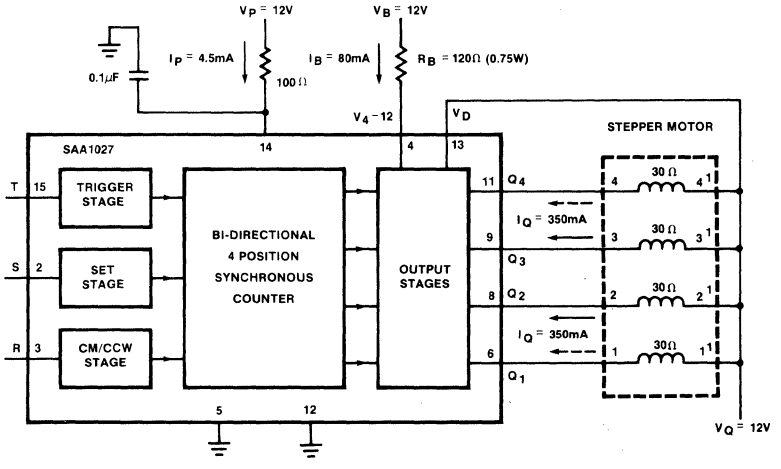


Figure 6

TAA960-K

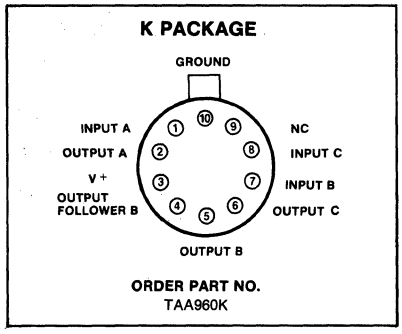
DESCRIPTION

The TAA960 consists of three identical general-purpose amplifiers integrated in a single silicon chip. The amplifiers can be used separately or can be cascaded to give a voltage gain of 117dB. One of the amplifiers has an additional emitter-follower stage. The TAA960 is very suitable for use in an active RC band-pass filter with Q up to 60.

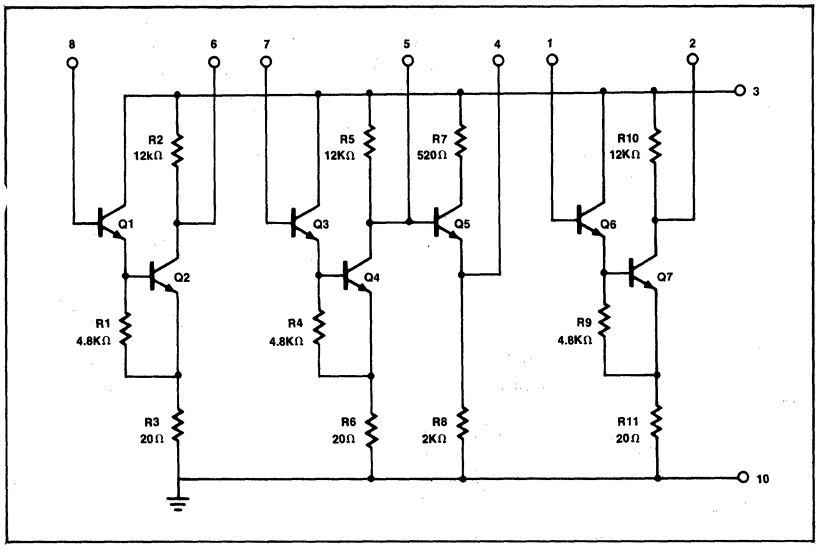
FEATURES

- **Cascade voltage gain of 117dB**
- **Typical Q of 45 in filter**
- **Input resistance > 25K**
- **Triple configuration**
- **Emitter follower output available**

PIN CONFIGURATION



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
	Voltages with respect to pin 10		
V_3	Supply voltage	10	V
V_8, V_7, V_1	Input voltage	4	V
V_6, V_5, V_4, V_2	Output voltage	10	V
I_8, I_7, I_1	Input current	50	μA
P_{TOT}	Total power dissipation	250	mW
T_{STG}	Storage temperature	-65 to +125	°C
T_A	Operating ambient temperature	-55 to +65	°C

NOTES:
1. With lower dc potential on all other terminals.

TAA960-K

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, V+ = 6V unless otherwise specified.

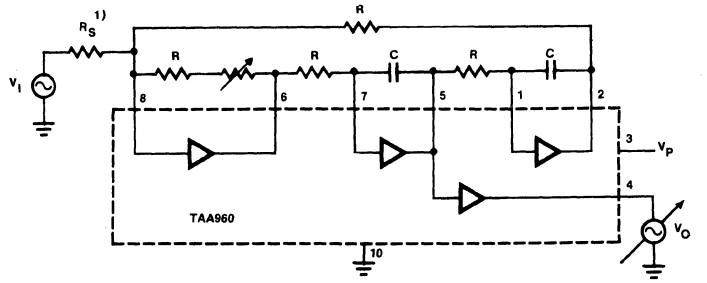
PARAMETER		TEST CONDITIONS	TAA960			UNIT
			Min	Typ	Max	
I_{CC}	Supply current[2]		1.5	2.0	2.5	mA
I_{CC}	Supply current[2]	$V_3 = 10V$	1.5	2.6	3.8	mA
A_{VOL}	Voltage gain (each amplifier)		60	90	150	V/V
R_{IN}	Input resistance		25			kΩ
R_{OUT}	Output resistance	Pins 2, 5 & 6	8	9		kΩ
R_{OUT}	Output resistance	Pin 4	135		750	Ω

NOTES

2. Terminal 8 connected to terminal 6
   Terminal 7 connected to terminal 5
   Terminal 1 connected to terminal 2

TYPICAL APPLICATIONS

ACTIVE RC FILTER FOR FREQUENCIES UP TO 150kHz



R = 10kΩ
This frequency range can be extended to 200kHz if a feed forward capacitor is connected between pin 5 and 8.

f	Frequency	$\frac{1}{2\pi RC}$	
V_P	Supply voltage	6	V
	Filter performance		
Q	at $T_A = 25°C$	40 to 55	
Q	at $T_A = -30$ to $+65°C$	35 to 55	
V_i	Input voltage	400	mV
V_o	Output voltage	400	mV
d_{tot}	Distortion at $V_o = 350mV$	2	%
S/N	S/N ratio at $V_o = 400mV$	50	dB
R_S	Input resistor*	470	kΩ

*NOTE

Value of input resistor to be determined for $\frac{V_o}{V_i}$ = 0.90 to 1.1.

TCA210-N

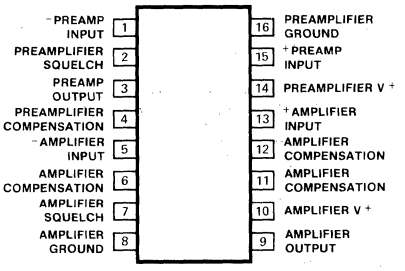
DESCRIPTION

The TCA210 is a monolithic integrated circuit comprising two amplifiers for use in intercoms and other audio systems. The first is a high-grain pre-amplifier with differential input and a class-A output stage which can deliver 2.5mW into an 800Ω load. The second is a power amplifier with a class-B output stage capable of delivering 500mW into a 25Ω load.

Speech rating: up to 800mW can be delivered into a 15Ω load for short periods. When there is no signal, the current consumption is 8mA (typ.). Squelch provision incorporated in both amplifiers can be used to ensure maximum battery life.

PIN CONFIGURATION

N PACKAGE

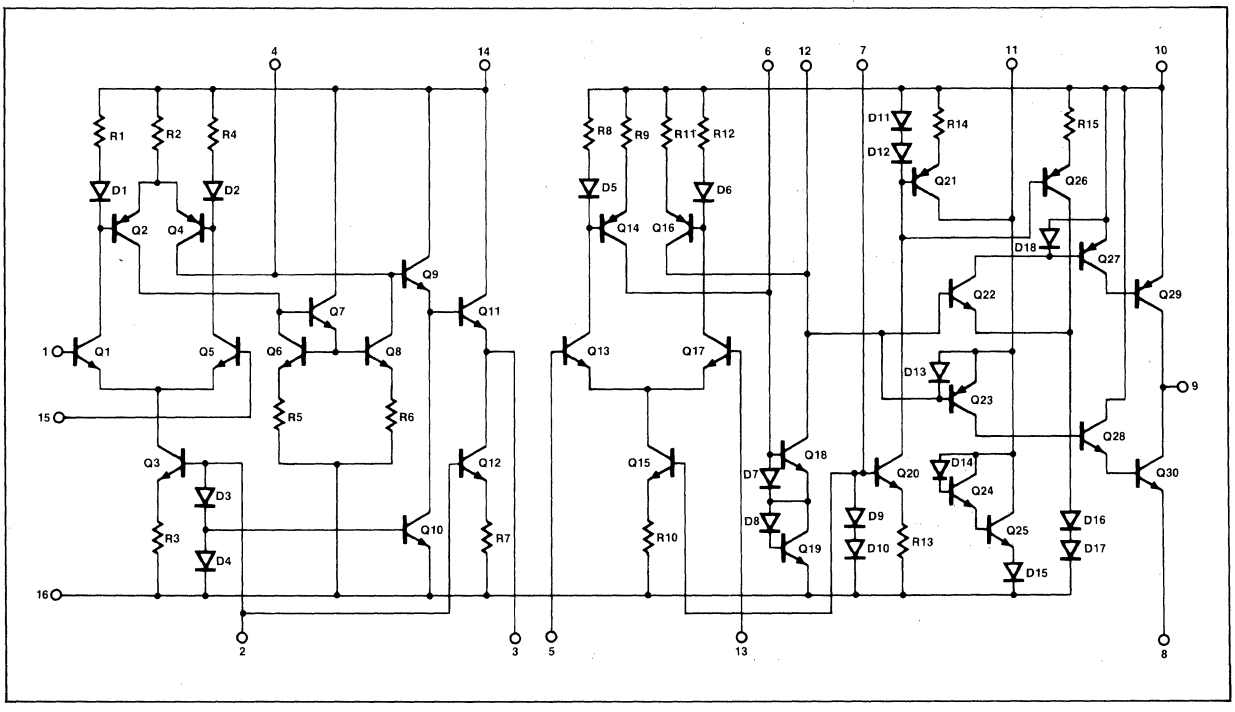


ORDER PART NO.
TCA210N

FEATURES

- **Noise figure < 6dB**
- **Separate supply and ground leads**
- **Preamp open loop gain of 10KV/V**
- **Output amplifier gain of 500V/V**
- **Output power 500mW**

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Voltages		
Pin 8 must be externally connected to pin 16		
Pins 3, 9, 10, 14 with respect to pin 16	17	V
Pins 1, 15, 5, 13 with respect to pin 16	17	V*
Pin 1 with respect to pin 15	±5	V
Pin 5 with respect to pin 13	±5	V
Currents		
Pin 10	550	mA
Pin 9	±550	mA
Pin 8	550	mA
Pin 14	20	mA
Pin 3	±20	mA
Pins 2, 4, 6, 7, 11, 12	5	mA
Pins 1, 15, 5, 13	0,5	mA
Temperatures		
Storage temperature T_{STG}	-55 to +125	°C
Operating ambient temperature (see also graph) T_A	-55 to +125	°C

*NOTE

For a supply voltage less than 14V, the maximum input voltage is equal to the supply voltage.

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V+ = 12 volts unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
I_B	Input bias current	Pins 1 and 15 $1/2(I_1+I_{15})$		2.5		μA
I_{CC}	Supply current	Pin 14		4		μA
I_B	Input bias current	Pin 2		200		μA
I_B	Input bias current	Pins 5 and 13 $1/2(I_5+I_{13})$		2		μA
I_{CC}	Supply current	Pin 10, no signal		4		μA
I_B	Bias current	Pin 7		150		μA
A_{VOL}	Open loop gain (Preamplifier)		65	80		dB
	Output transistor		2.5			mA
Output amplifier						
A_{VOL}	Open loop voltage gain			54		dB
P_{OUT}	Output power			450		mW
Preamplifier						
N_F	Noise figure	R_S = 5KΩ, B_W = 300 to 4KHz		4		dB
B_W	Unity gain bandwidth	6dB/octave compensation		10		MHz
Output amplifier						
T_{HD}	Total distortion	f = 1KHz, P_O = 50mW, R_L = 75Ω		1.5		%

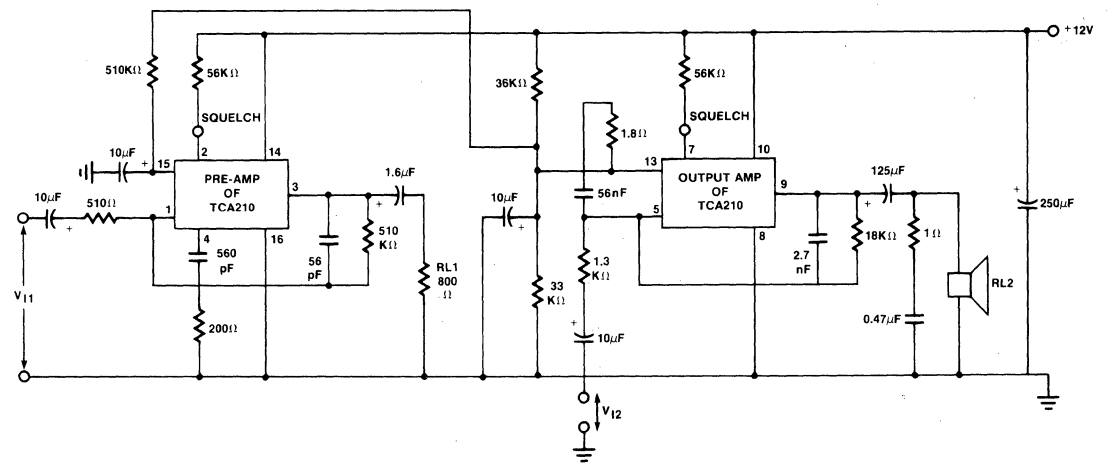
NOTE

V+ = 12 volts, T_A = 25°C unless otherwise specified

TCA210-N

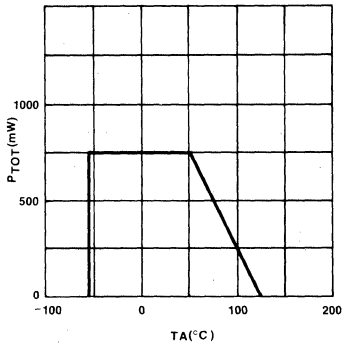
TYPICAL APPLICATION

PRE-AMPLIFIER AND OUTPUT AMPLIFIER FOR INTERCOM SYSTEMS



TYPICAL PERFORMANCE CHARACTERISTICS

TOTAL POWER DISSIPATION



ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_P = 12V$

PARAMETER		LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
PRE-AMPLIFIER					
P_o	Output power at $R_{L1} = 800\Omega$			2, 5	mW
B	Bandwidth (-3dB)			4	kHz
I_{14}	Total current			4, 0	mA
V_{i1}	Input signal			1, 5	mV
$\|Z_i\|$	Input impedance			500	Ω
OUTPUT AMPLIFIER					
P_o	Output power at $R_{L2} = 25\Omega$; $d_{tot} = 5\%$			500	mW
P_o	at $R_{L2} = 15\Omega$; $d_{tot} = 5\%$			800	mW
B	Bandwidth (-3dB)			4	kHz
d_{tot}	Total distortion at $P_o = 50mW$			1, 5	%
V_{i2}	Input signal			260	mV
$\|Z_i\|$	Input impedance			1, 3	kΩ
I_{10}	Total current (dc; no signal; pin 10)			4	mA

TCA580-N

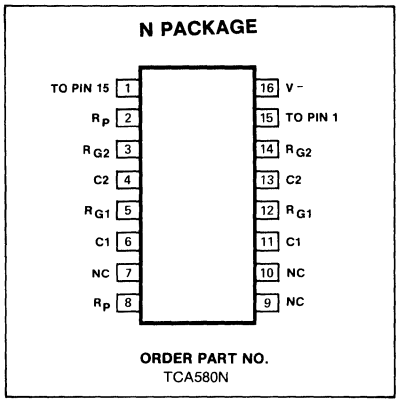
DESCRIPTION

The TCA580 is a monolithic integrated gyrator circuit with floating inputs. It is intended mainly to replace the coils in telephony low-pass filters. The simulated inductance consists of the IC, two resistors R_{g1} and R_{g2} and a capacitor C2. With this configuration, inductances of up to 1MH ± 2% can be achieved.

FEATURES

- **Frequency range dc to 10kHz**
- **Q's of 500 to 5000**
- **Operating temperature range -20 to +70° C**
- **Efficiency of 1.4%**

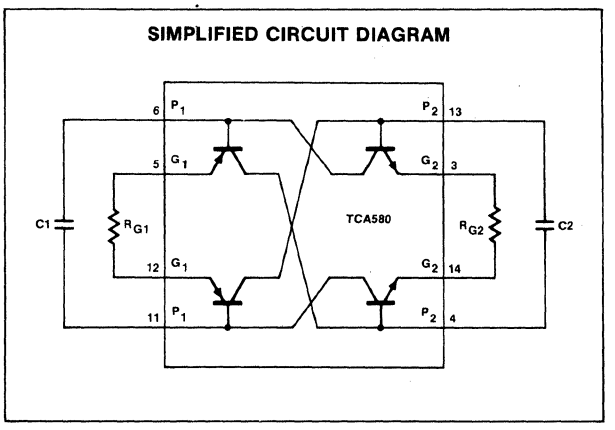
PIN CONFIGURATIONS

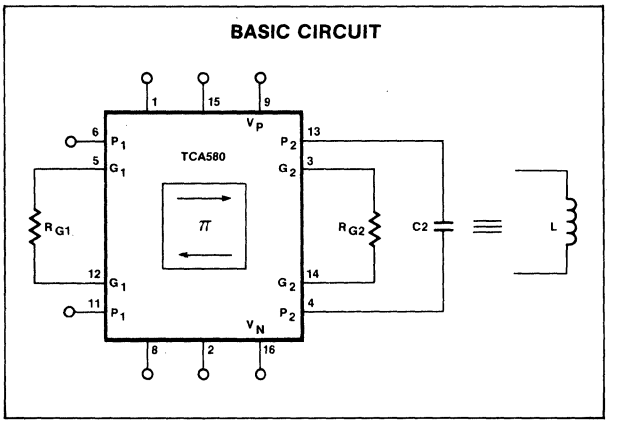


ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V+ to V-	Supply voltages	14	V
$\pm V_{IC}$	Common mode input voltage	14	V
$\pm V_{ID}$	Differential input voltage	14	V
T_{STG}	Storage temperature	-55 to +125	°C
T_{AMB}	Operating ambient temperature	-20 to +70	°C

BLOCK DIAGRAMS



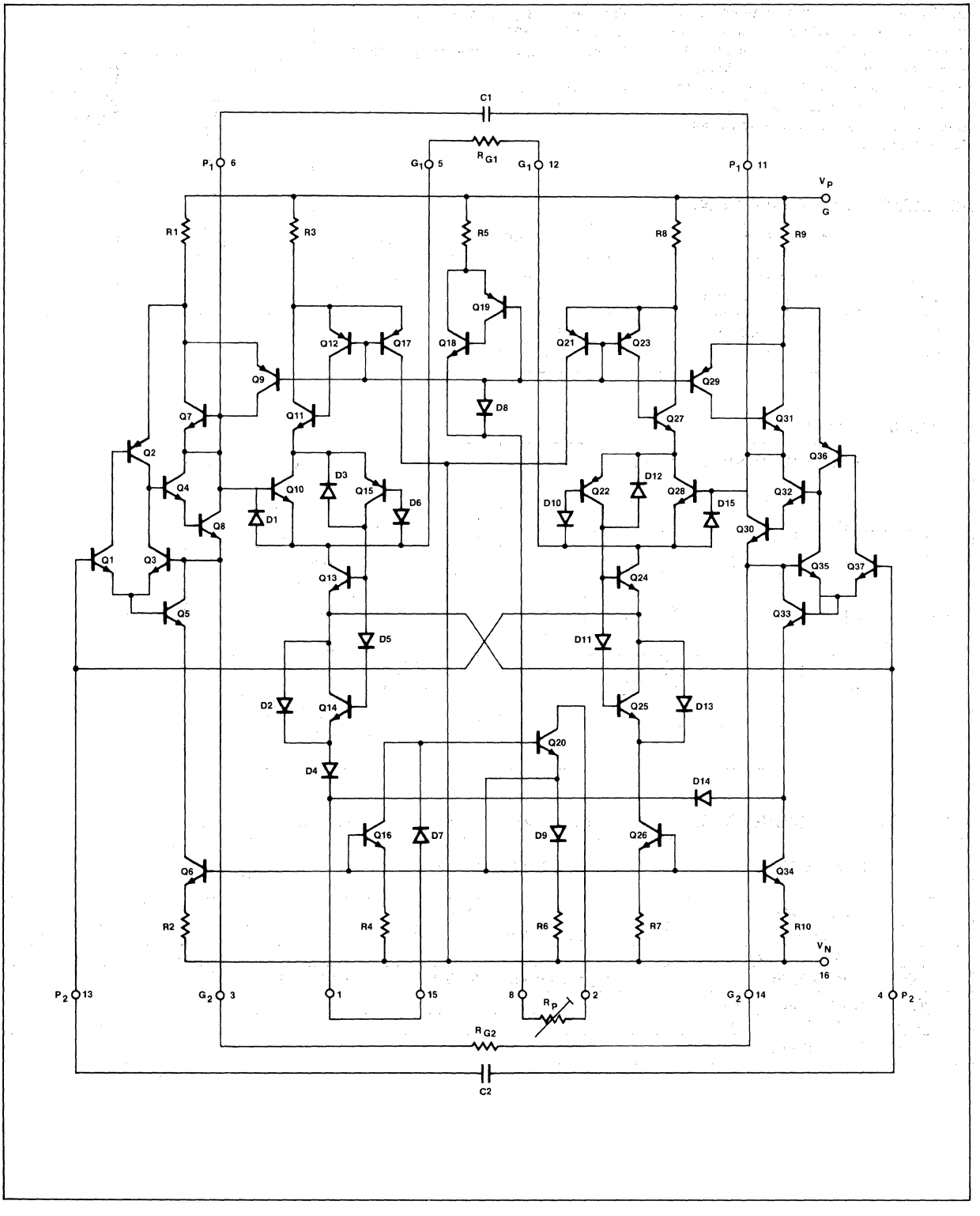


DC ELECTRICAL CHARACTERISTICS

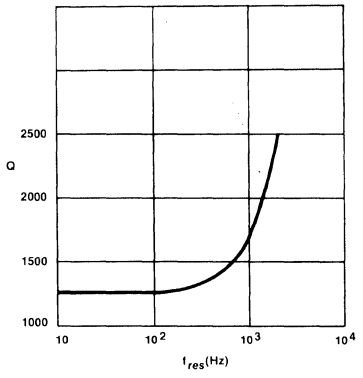
T_A 25°C, V+ = 4.4V, V- = -7.6V unless otherwise specified.

PARAMETER		TEST CONDITIONS	TCA580N			UNIT
			Min	Typ	Max	
I_P	Supply current	R_P = 50kΩ		0.8		mA
n	Efficiency	(Signal Power ÷ Supply Power)		1.4		%
ΔL	Inductor tolerance			±0.2		%
Q	Quality factor	Pin 11 grounded, f = 200Hz, $R_{g1} = R_{g2}$ = 10kΩ	500		5000	
V_{OUT}	Output voltage (peak)				1.6	V
V_{OS}	Input offset voltage				25	mV
I_{OS}	Input offset current				9	μA

EQUIVALENT SCHEMATIC

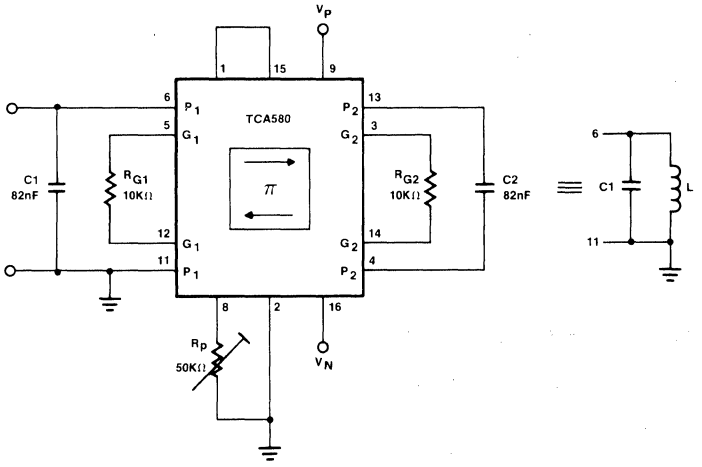


TYPICAL PERFORMANCE CHARACTERISTICS



Quality factor as a function of frequency at pin 11 connected to earth. (See Figure 1).

TYPICAL CONNECTION



The values for L and f_{res} in the circuit above are:

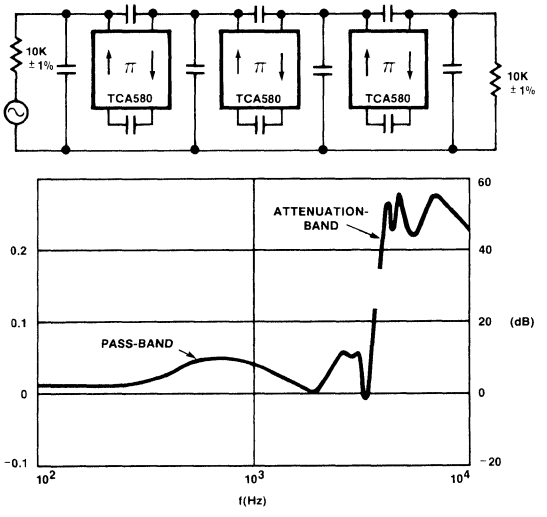
$L = R_{G1} R_{G2} C2 = 8.2H$

$$f_{res} = \frac{1}{2\pi \sqrt{R_{G1} R_{G2} C1 C2}} = 194Hz$$

Figure 1

TYPICAL APPLICATIONS

Circuit and response of a low-pass filter with three TCA580 gyrators.



TCA980-K

DESCRIPTION

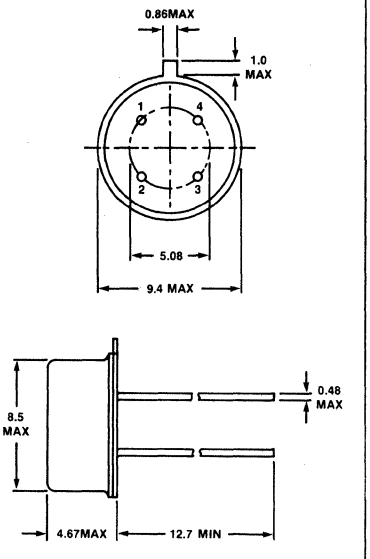
The TCA980 is a monolithic integrated microphone amplifier. It is primarily intended for use with low-impedance microphones in telephone systems. The output of the amplifier is 22mV/μbar when used with a microphone having an impedance of 200Ω and a sensitivity of 100μV/μbar. A capsule assembly containing the TCA980, a low-impedance microphone and a 0.22μF capacitor can directly replace a carbon microphone. The dc supply to the device may be of either polarity.

FEATURES

- **Voltage gain - 220V/V**
- **Noise voltage 1.3mVrms**
- **Single supply operation**

PIN CONFIGURATIONS

K PACKAGE



ORDER PART NO.
TCA980K

ABSOLUTE MAXIMUM RATINGS

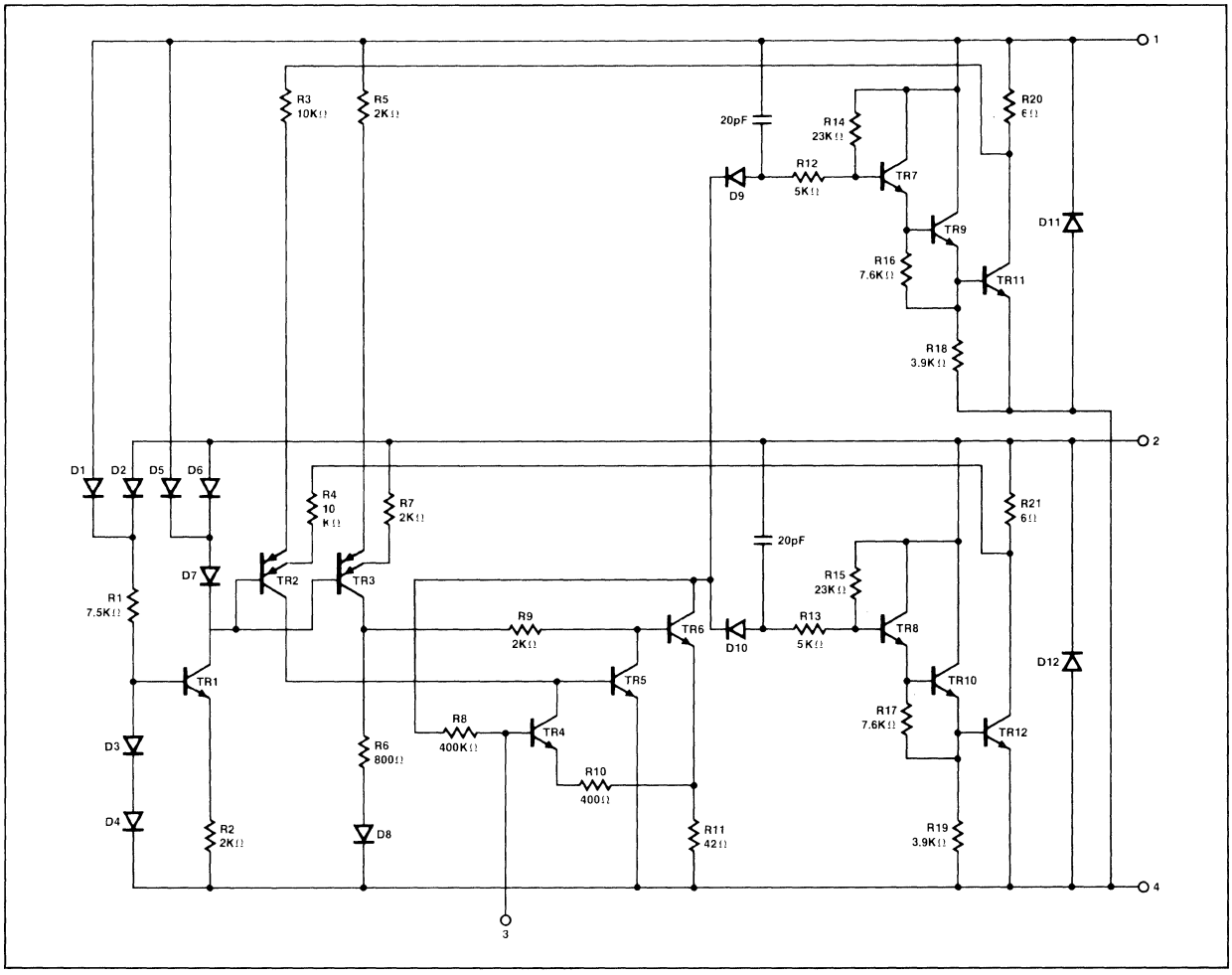
	PARAMETER	RATING	UNIT
$\pm I_2$	Supply current (dc)	100	mA
	Non-repetitive peak current	100	mA(ac)[1]
$+I_3$	Current into pin 3 (dc)	100	μA
	Total power dissipation[2]		
T_{STG}	Storage temperature	-55 to +125	°C
T_A	Ambient temperature	-55 to +125	°C
T_{CR}	Crystal temperature	125	°C
	THERMAL RESISTANCE		
θjC	From crystal to case	65	°C/W
θjA	From crystal to ambient	180	°C/W

NOTES

1. Superimposed on 100mA (dc)
2. See derating curve.

TCA980-K

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, Test Figure 1 unless otherwise specified.

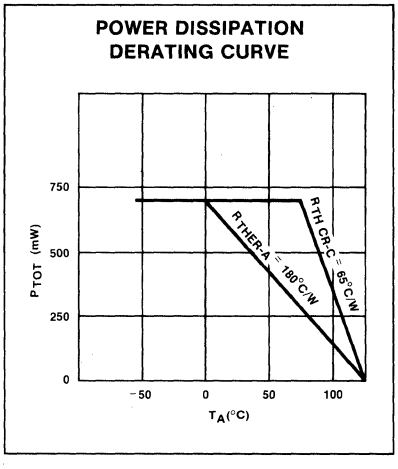
PARAMETER		TEST CONDITIONS	TCA980			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage drop	$\pm I_2 = 10mA$	3.5		5.75	V
		$\pm I_2 = 30mA$	4.45		6.75	V
		$\pm I_2 = 60mA$	5.0		7.8	V

TCA980-K

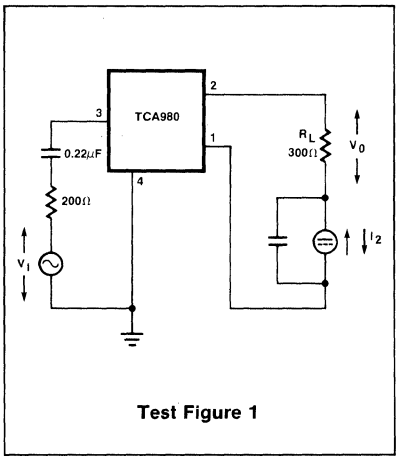
AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, Test Figure 1 unless otherwise specified.

PARAMETER		TEST CONDITIONS	TCA980			UNIT
			Min	Typ	Max	
A_{VOL}	Voltage gain	Test Figure 1, f = 2kHz, $I_2 = \pm 30mA$ Test Figure 1, f = 2kHz, $I_2 = \pm 10mA$	190 160	220	260 260	V/V V/V
ΔA_{VOL}	Voltage gain change	$-20°C \leq T_A \leq 55°C$ $300Hz \leq f \leq 2kHz$		 1	10 3	% dB
V_{OUT}	Output voltage	f = 2kHz, $d_{TOT} < 5\%$ (rms), $I_2 = \pm 10mA$ f = 2kHz, $d_{TOT} < 5\%$ (rms), $I_2 = \pm 30mA$ f = 2kHz, $d_{TOT} < 5\%$ (rms), $I_2 = \pm 60mA$	1 1.35 1	 1.5		V V V
V_N R_{OUT}	Output noise voltage Output impedance	BW = .3kHz to 4kHz f = 2kHz, $I_2 = \pm 30mA$		 150	1.3	mVrms Ω

TYPICAL PERFORMANCE CHARACTERISTICS



TEST LOAD CIRCUITS



Test Figure 1

TDA1024-N

DESCRIPTION

The TDA1024 is a monolithic integrated circuit intended for use in ON/OFF control of triacs in static switching applications. It incorporates zero voltage point triggering to minimize radio interference.

The TDA1024 is mainly intended for applications such as switching resistive loads and replacing mechanical thermostats in, for example:

Central heating installations,
Washing machine heaters,
Water heaters,
Smoothing irons.

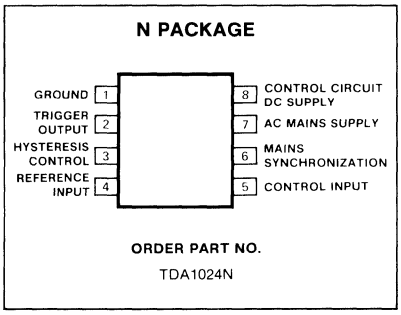
Functions of the TDA1024 are:

1. A comparator with Schmitt-trigger action.
   This circuit compares the control voltage at pin 5 with the reference voltage at pin 4 and switches on when the control voltage exceeds the reference voltage. The hysteresis of the circuit is adjustable between 20mV and 300mV by selection of the value of a resistor connected between pin 3 and pin 1.
2. An input buffer circuit with high input impedance and low output impedance. This circuit presents a low impedance to the comparator input so that the hysteresis of the circuit is independent of variations of the input voltage.
3. A control circuit dc supply which provides a zener-limited nominal 6.5V supply, at a current of up to 30mA, for application to the input bridge.
4. A zero-crossing detector which produces an output when the sinusoidal voltage applied to pin 6 passes through zero; advantage of this mode in minimum radio interference.
5. A control gate which inhibits the output trigger pulse from the TDA1024 unless there are outputs from both zero-crossing detector and comparator.
6. An output stage which delivers a positive-going, mains-synchronized triac trigger pulse whenever the control gate is activated. The output from this stage is current-limited and protected against short-circuit. Since the current and voltage in the load must be in phase for mains-synchronized switching, the applications of the TDA1024 are restricted to the switching of resistive loads.

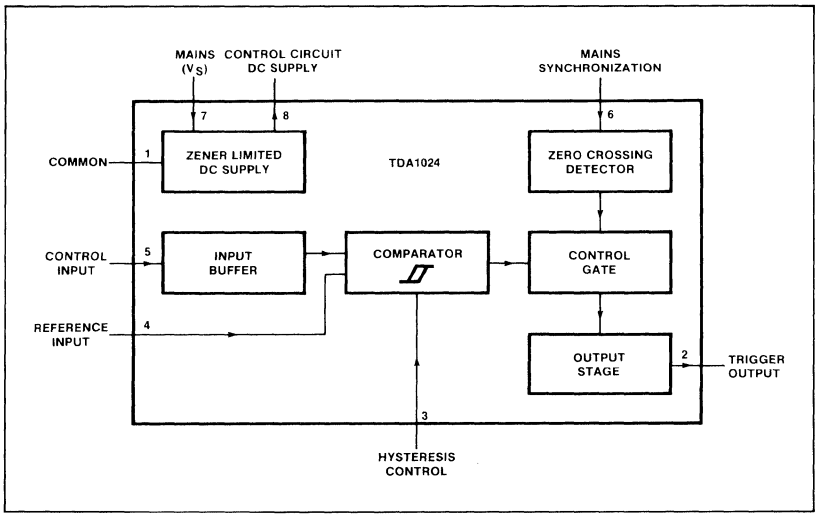
FEATURES

- **Trigger current > 100mA**
- **Supply derived from ac lines**
- **Adjustable hysteresis**
- **Minimum of external components**

PIN CONFIGURATION



BLOCK DIAGRAM

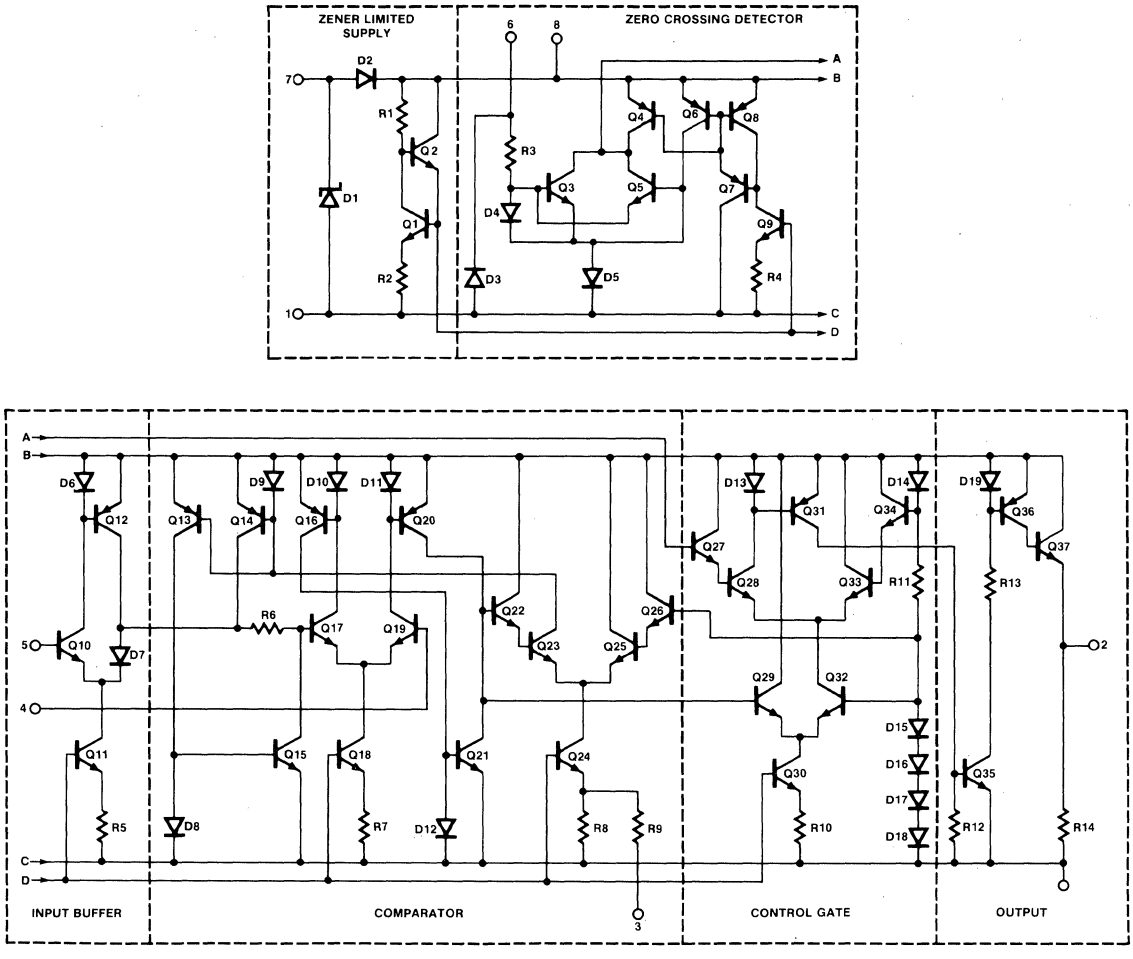


ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (pin 7)	8	V
V_{IN}	Max applied voltage (pin 2, 3, 4, 5 & 8 reference to pin 1)	8	V
I_{CC}	Supply current (pin 7) average	30	mA
I_{CC}	Supply current (pin 7) peak	80	mA
	Max current pins 4, 5, & 6	10	mA
	Non-repetitive peak current (pin 7) $T_p < 50\mu s$	2	A
I_{OUT}	Output current (pin 2) average	30	mA
I_{OUT}	Output current (pin 2) peak $T_p < 300\mu s$	400	mA
T_{SG}	Storage temperature	-55 to +125	°C
T_A	Operating ambient temperature	-20 to +80	°C
P_D	Power dissipation	See derating curve	
	Lead temperature (soldering, 10sec)	300	°C

TDA1024-N

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS

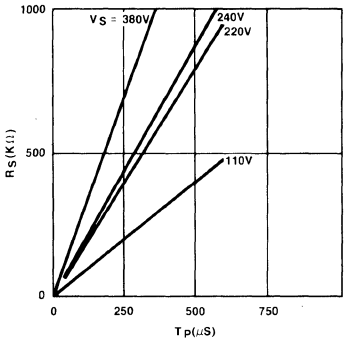
PARAMETER		TEST CONDITIONS	TDA1024			UNIT
			Min	Typ	Max	
	Trigger output					
I_{OUT}	Trigger output current	V_{8-1} = 5.5V	100			mA
V_{2-1}	Trigger output voltage	I_{OUT} =100mA	4			V
	Comparator					
I_4	Input current pin 4	$V_{4-1} > V_{5-1}$			5	μA
I_5	Input current pin 5				5	μA
V_8	Control circuit dc supply (pin 8)	I_7 = 10mA	5.5	6.5	7.5	V
I_{CC}	Supply current	$V_{5-1} > V_{4-1}$, V_{8-1} = 5.5V, pins 2 & 3 open minimum hysteresis			1.8	mA
I_{CC}	Supply current	Pin 2 open, pin 3 = 0V, $V_{5-1} > V_{4-1}$ V_{8-1} = 5.5V maximum hysteresis			3	mA

AC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	TDA1024			UNIT
			Min	Typ	Max	
$T_{TRIGGER}$	Trigger pulse width	I_6 = 1mA, V_{8-1} = 5.5V	130	195	265	μs
ΔV_{5-4}	Comparator hysteresis	Pin 3 open, I_3 = 0	10		30	mV
ΔV_{5-4}	Comparator hysteresis	V_3 = 0		300		mV

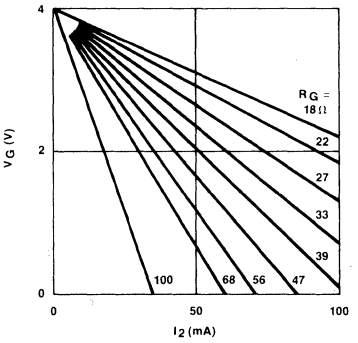
TYPICAL PERFORMANCE CHARACTERISTICS

TRIGGER PULSE WIDTH vs SYNCHRONIZATION RESISTOR



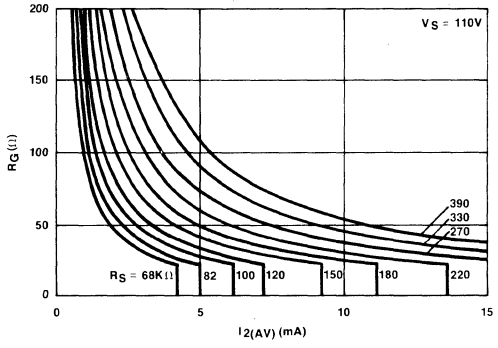
Use Test Circuit CKT 1

OUTPUT CURRENT vs GATE RESISTOR



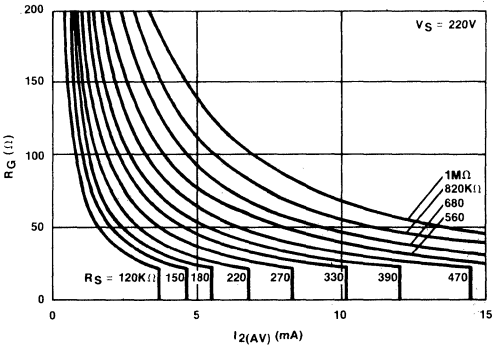
Use Test Circuit CKT 2

AVAILABLE TRIGGER CURRENT



Use Test Circuit 3

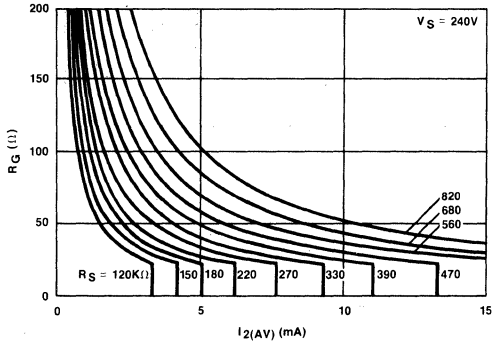
AVAILABLE TRIGGER CURRENT



Use Test Circuit 3

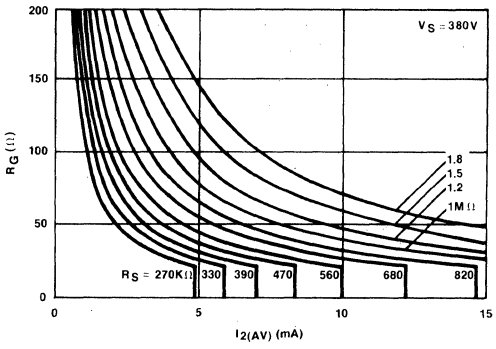
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

AVAILABLE TRIGGER CURRENT



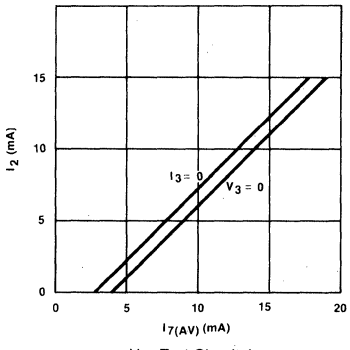
Use Test Circuit 3

AVAILABLE TRIGGER CURRENT



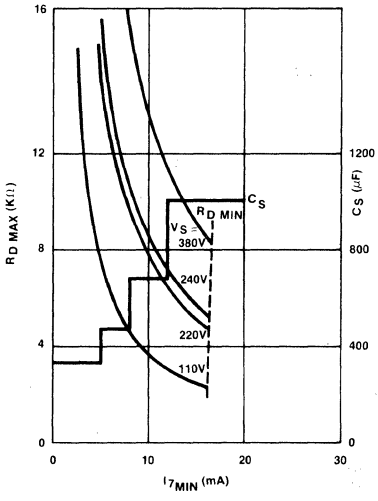
Use Test Circuit 3

MINIMUM REQUIRED SUPPLY CURRENT



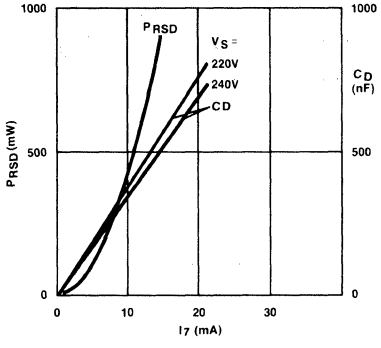
Use Test Circuit 4

MAXIMUM SERIES RESISTANCE AS A FUNCTION OF REQUIRED SUPPLY CURRENT

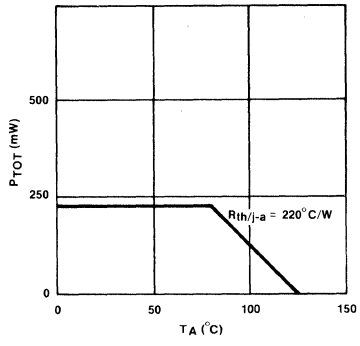


Use Test Circuit 5

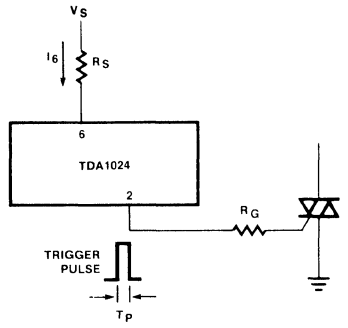
DROPPING RESISTOR POWER DISSIPATION USING DROPPING CAPACITOR



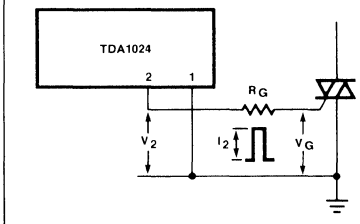
POWER DISSIPATION DERATING CURVE



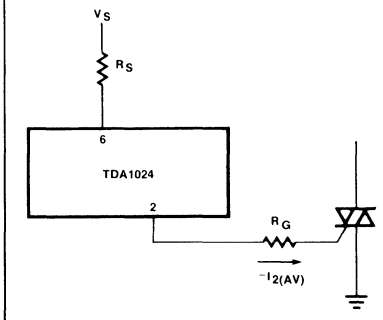
TEST LOAD CIRCUITS



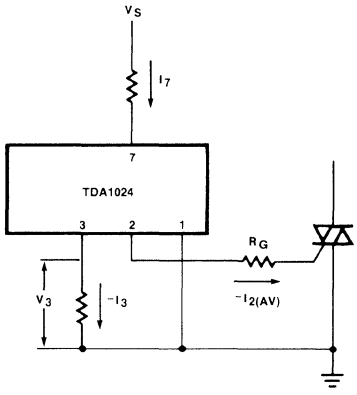
Use Test CKT 1. Synchronization resistor (R_S) value as a function of required trigger pulse width (t_p) with applied mains voltage (V_S) as a parameter.
Tolerance for R_S: ±5%
V_S: ±10%



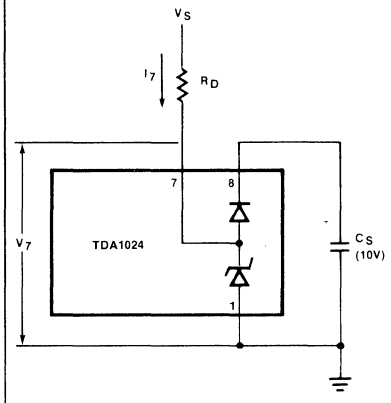
Use Test CKT 2. Gate voltage (V_G) as a function of trigger current (I_2) with gate resistor (R_G) load lines.



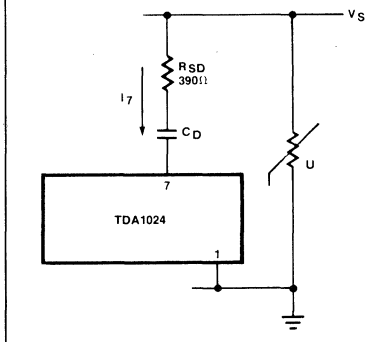
Use Test CKT 3. With the circuit above. They show the maximum average trigger current $I_{2(av)}$ as a function of the value of R_G with the value of R_S as a parameter for V_S = 110V; 220V; 240V; 380V respectively.



Use Test CKT 4. Minimum required supply current (I_7) as a function of maximum average trigger current ($I_{2(av)}$), with hysteresis setting as a parameter.
I_3 = 0; min. hysteresis.
V_3 = 0; max. hysteresis.



Use Test CKT 5. Value of $R_{d\,max}$ as a function of I_{7min} with supply voltage (V_S) as a parameter.
Also shown is the value of the smoothing capacitor (C_S) as a function of I_{7min}.



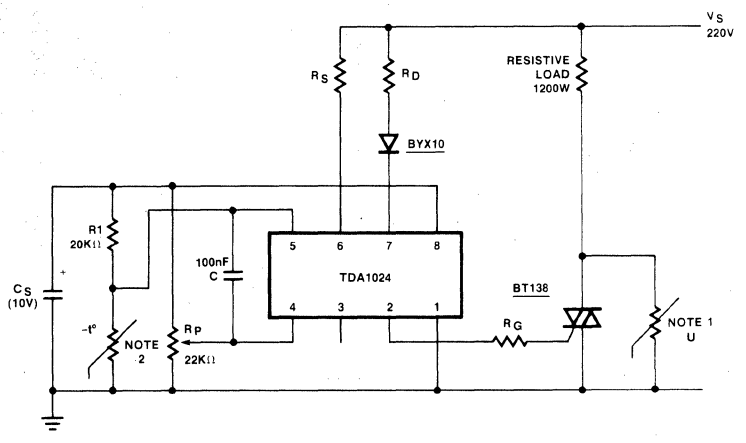
Use Test CKT 6. Using a capacitor for mains supply voltage dropping.

COMPONENT VALUES AND CIRCUIT PARAMETERS

PARAMETER		VALUE		TEST CIRCUIT
		FIG. 1	FIG. 2	
$t_p(\mu s)$	Trigger pulse width	105	105	
$R_S(k\Omega)$	Sync. resistor	180	180	1
$R_G(\Omega)$	Gate resistor	33	33	2
$I_{2(av)}$(mA)	Average gate current	3.7	3.7	3
I_7(mA)	Min. required supply current	6.5	6.5	4
$R_d(k\Omega)$	Mains dropping resistor	10	—	5
$C_s(\mu F)$	Smoothing capacitor	470	470	5
C_d(nF)	Mains dropping capacitor	—	270	6
P_{Rsd}(mW)	Power dissipated by R_{sd}	—	190	6

Design data for the two previous circuits (for other circuits the same sequence of component value selection must be used):
BT138 triac with: V_{GT} = 1.6V at 0°C Mains voltage: V_S = 220V
I_{GT} = 72mA at 0°C Triac load: 1200W
I_L < 60mA

TYPICAL APPLICATIONS

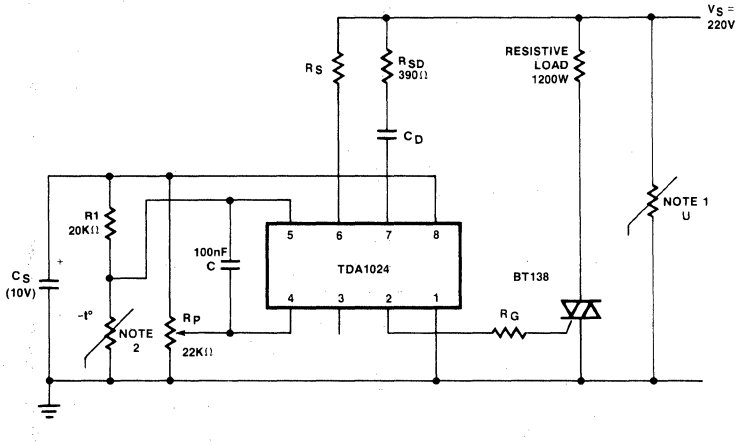


NOTES

1. Spike suppressor (VDR): 350V/1mA (2322 594 13512)
2. $R_{25} = 22k\Omega$

The TDA1024 used in a 1200W thermostat covering the temperature range 5°C to 30°C and designed to minimize the power dissipated by mains dropping resistor R_d by using a rectifier diode.

Figure 1



NOTES

1. Spike suppressor (VDR): 350V/1mA (2322 594 13512)
2. $R_{25} = 22k\Omega$

The TDA1024 used in a 1200W thermostat covering the temperature range 5°C to 30°C and designed to minimize the dissipation in the mains voltage reduction circuit by using capacitor C_d.

Figure 2

TDA1060-N

DESCRIPTION

The TDA1060 is a monolithic integrated circuit intended for the control of switched mode power supplies. It incorporates all the control and protection functions likely to be required in switched mode power supplies for professional equipment.

FEATURES

- **Stabilized power supply**
- **Temperature compensated voltage reference**
- **Sawtooth generator**
- **Pulse width modulator**
- **Remote ON/OFF switching**
- **Current limiting**
- **Low supply voltage protection**
- **Loop fault protection**
- **Demagnetization/over voltage protection**
- **Maximum duty cycle adjustment**
- **External synchronization input**
- **Feed forward**

FUNCTIONAL DESCRIPTION

A. Stabilized Power Supply

The circuit can be fed either by a current source (e.g. connected to the high voltage input of the SMPS via a series resistor), or a voltage source (e.g. a 12V battery). When fed from a 12V supply the maximum current consumption is 10mA.

The stabilized voltage is typically 8.4V and is available on pin 2 for supplying external circuitry. Up to 5mA can be drawn from this supply whereupon the total IC current consumption increases by the same amount. This stabilized supply is protected against short circuits.

B. Reference Voltage Source

The reference voltage for the SMPS is incorporated in the IC. The temperature stability of this reference is ±100ppm/°C maximum.

C. Sawtooth Generator and Feed Forward

The frequency of the sawtooth generator is set by an external resistor (pin 7) and a capacitor (pin 8). The frequency can be determined with the aid of Figure 3. It may be set between 50Hz and 100KHz and is virtually independant of supply voltage.

The upper and lower levels of the sawtooth are fixed by an internal resistor divider. Since these resistors form a bridge configuration with the external voltage divider for the δ-max setting; the accuracy of the δ-max setting is determined by resistor matching rather than by absolute values.

During the flyback of the sawtooth the output pulse is inhibited. This acts as an internal duty cycle limiter. Since the flyback time is 1μs (with 1nF capacity), the maximum duty cycle is limited to 95% at 50KHz.

The frequency of the sawtooth can be synchronized via the TTL-compatible input on pin 9. The synchronizing frequency must be lower than the oscillator free running frequency. When the input on pin 9 is Low the sawtooth generator is stopped, starting again when the input goes High. For free-running operation pin 9 is left dissconnected.

Feed forward can be provided via pin 16 which has the effect of varying the supply voltage of the sawtooth generator with respect to the stabilized voltage. When the voltage on pin 16 increased the upper level of the sawtooth is also increased. Since neither the δ-max voltage level nor the feedback voltage are influenced by the feed forward; the duty cycle reduces. This is a linear function and can therefore compensate for supply voltage variations. If feed forward is not required pin 16 should be connected to pin 12.

D. Feedback Amplifier

The difference between the feedback voltage (pin 3) and the internal reference voltage is amplified in an operational amplifier. The output signal is compared with the sawtooth which has an amplitude of typically 4.5V (without feed forward).

The gain can be controlled by a feedback circuit from the op. amp. output (pin 4). To avoid instability a capacitor should be connected across the op amp (i.e. between pins 3 and 4).

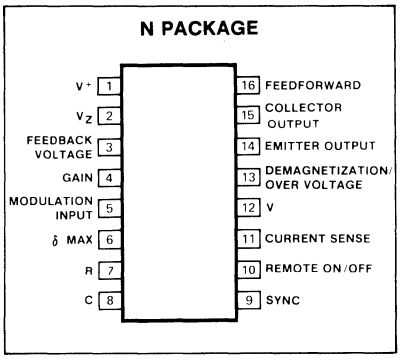
E. Remote ON/OFF

Remote switching can be provided through the TTL-compatible input on pin 10. When this input is Low the circuit is switched off. With the input High the circuit switches on via the slow start procedure.

F. Current Limiter

The current limiter comprises two comparators with trip-on levels of 480mV and 600mV respectively. When the voltage on the current sense input (pin 11) exceeds 480mV, the output pulse is immediately cut off, starting again at the next period. If the voltage exceeds 600mV, the output pulse is inhibited during a certain "dead time", during which the slow start capacitor is unloaded. After this the circuit starts again with slow start.

PIN CONFIGURATION



G. Low Supply Voltage Protection

When the supply voltage is too low (less than Vz + 0.2V) the circuit is automatically switched off. Starting takes place again via the slow start as soon as the supply voltage exceeds this threshold value.

H. Feedback Loop Fault Protection

If the feedback loop is open, the feedback input (pin 3) is pulled high by an internal current source making the duty cycle zero. If the feedback loop is short-circuited, or if the feedback voltage does not exceed 600mV, the δ-max pin is connected to the lower level of the sawtooth by a 1kΩ resistor. This causes a lower δ-max voltage as described in the maximum duty cycle and slow start section.

I. Output

The output circuit comprises a latch and an output transistor. Both collector and emitter of the output transistor are available on pins 15 and 14 respectively. The collector is internally connected to the supply voltage of the integrated circuit by a clamping diode to limit the output voltage in the case of a fault in the external drive circuit of the switching transistor.

J. Demagnetisation/Overvoltage

The demagnetisation/overvoltage input (pin 13) inhibits the output when the voltage at this pin exceeds the trip-on level of 600mV. The combined function can be realized by a zener diode from the output voltage of the SMPS to this pin (e.g. a 5.6 zener in a 5V supply) and the demagnetisation sensor connected also directly to this point.

K. Maximum Duty Cycle and Slow Start

The voltage on pin 6 (δ-max setting) determines the maximum output duty ratio. As explained in section C the δ-max setting accuracy is very good since the voltage at this pin is divided by a resistive divider from the Vz voltage.

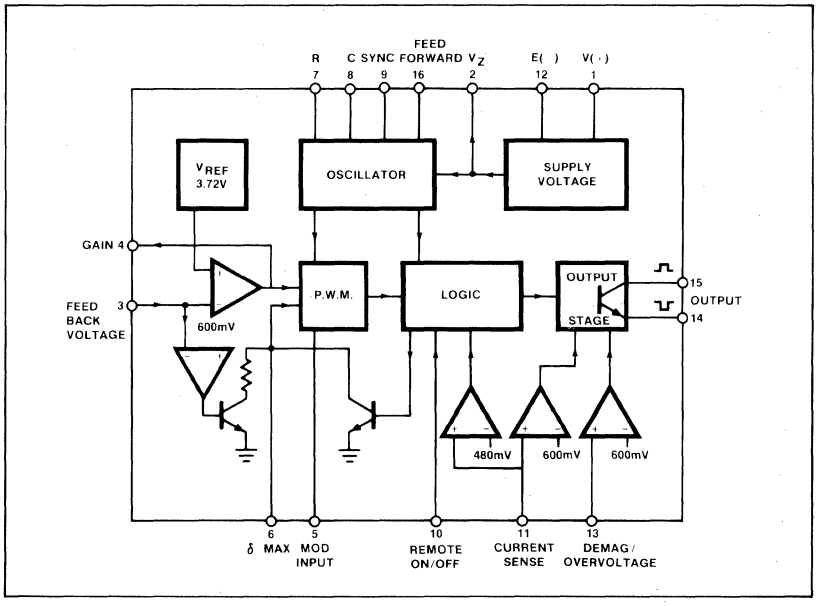
In the event of a loop fault the δ-max pin is connected via an internal 1kΩ resistor to the lower limit of the sawtooth voltage. Thus the δ-max value is decreased to a level determined by the impedance of the δ-max resistive divider to the internal 1kΩ.

The capacitor connected to the δ-max pin, together with the impedance of the resistive divider, determines the time constant for the slow start. For remote ON/OFF or when the current sensing voltage exceeds 600mV, the value of the capacitor determines the dead time of the slow start procedure.

L. Modulation Input

Pin 5 gives an input to the pulse width modulator which may be used for current mode regulation. The duty cycle reduces when the voltage at this point decreases.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING Min	RATING Max	UNIT
V_{CC}	Supply voltage	-0.5	18	V
I_{CC}	Supply current	0	30	mA
	Output current	0	40	mA
	Voltages at the pins with respect to pin 12			
	Feed forward (pin 16)	0	V+	V
	Output emitter (pin 14)	0	5	V
	Output collector (pin 15)	0	V+	V
	All other inputs	0	V_Z	V
	Storage temperature	-25	+125	°C
	Operating temperature	-25	+85	°C

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = 12V$ (VP) unless otherwise specified.[1,2,3,4,5]

PARAMETER			TEST CONDITIONS	TDA1060			UNIT
				Min	Typ	Max	
V_{IN}		Input voltages					
	Pin 1		Current FED I_1 =10mA	20	21	23	V
	Pin 1		Current FED I_1 = 30mA	20	25	30	V
V_Z	Pin 2			7.8	8.4	9.0	V
ΔV_Z/temp.		V_Z drift		-1.3		1.3	mV/°C
	Pin 10	Remote ON/OFF[2]	Circuit ON	2		V_Z	V
	Pin 10	Remote ON/OFF[2]	Circuit OFF	0		0.8	V
	Pin 11	Inhibit	Single pulse inhibit	0.76	0.8	0.84	V_{11}(Start)
	Pin 11	Start	Shutdown/slow start	470	600	720	mV
	Pin 3	Feedback loop protection	Trip on	470	600	700	mV
	Pin 14	Maximum emitter voltage		5			V
	Pin 14-15	Saturation voltage	I_{15} = 40mA			400	mV
	Pin 13	Over voltage input[4]	Trip on level	470	600	720	mV
	Pin 6	δ-max voltage level	Duty cycle = 50% (15-50kHz)	0.38V_Z	0.4V_Z	0.42V_Z	V
	Pin 9	Synchronization input	Sawtooth stopped	0		0.8	V
	Pin 9	Synchronization input	Sawtooth running	2		V_Z	V
V_{REF}	Reference voltage			3.42	3.72	4.03	V
ΔV_{REF}	Temperature coefficient of reference voltage			-100		100	ppm/°C
	Lower sawtooth level				1.1		V
	Upper sawtooth level				5.6		V
V_{PT}	Supply voltage protection		Trip-on level	V_Z+.2		V_Z+1.7	V
ΔV_{PT}	Supply voltage protection Temperature coefficient			-6.5			mV/°C
I_{IN}	Input currents						
	Pin 1	Supply current	Voltage FED	5		10	mA
	Pin 2	Maximum allowable external current drain				5	mA
	Pin 3	Input current			-40		µA
	Pin 10	Sink current[2]	V_{10} = 0			-90	µA
	Pin 11	Input current	V_{11} = 250mV			12	µA
	Pin 15	Available output current		40			mA
I_{IN}		Input currents					
	Pin 13	Input current[4]	V_{13} = 250mV			10	µA
	Pin 6	Input current	V_6 = 1V			20	µA
	Pin 16	Input current				5	µA
	Pin 9	Sink current	V_9 = 0			-90	µA
	Pin 5	Input current	V_5 = 1V			-40	µA
R	Sawtooth resistor value			10		40	kΩ
R	Amplifier resistor value			100			kΩ
A_{VOL}	Amplifier open loop gain				60		dB
	Internal duty cycle limiting		Period time T µs			(T-1)/T	
			c = 1nF			(T-1)/T	
	δ-max setting			0			

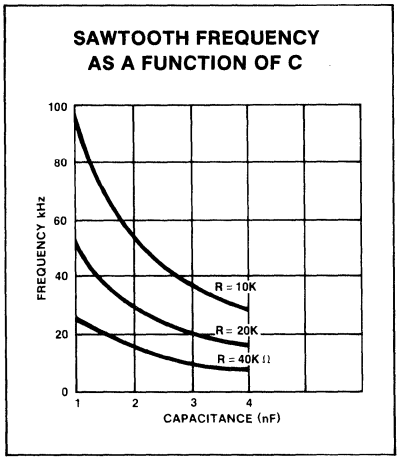
NOTES

1. The remote ON/OFF is not active when this pin is not connected.
2. The synchronization is not active when this pin is not connected.
3. The demagnetisation/overvoltage protection is active when this pin is not connected.
4. The current limiter is active when this pin is not connected.
5. All voltages with respect to pin 9.

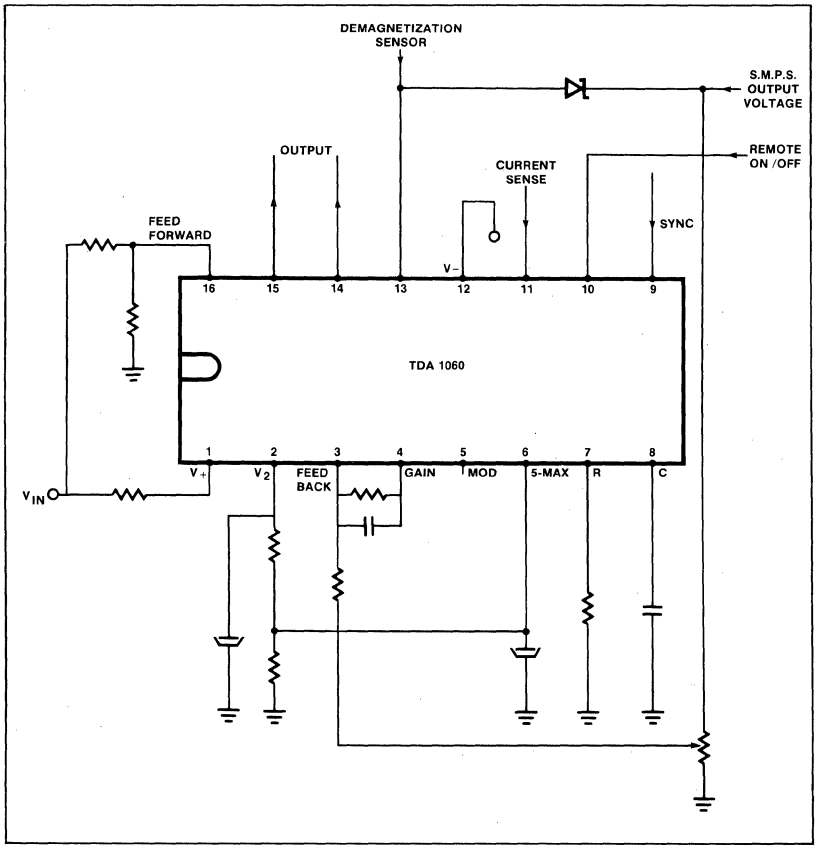
AC ELECTRICAL CHARACTERISTICS

PARAMETER		TO	FROM	TEST CONDITIONS	TDA1060			UNIT
					Min	Typ	Max	
T_D	Delay time	Output	Pin 11	25% overdrive, 40mA output current			0.8	μs
F	Sawtooth frequency range			Figure 3	0.05		100	kHz
$\Delta F/\Delta V$	Frequency drift with supply			8≤ V16 ≤ V+			2.3	%

TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL APPLICATION



SECTION 10
DISPLAY DRIVERS

DESCRIPTION

The DS8880 is a high voltage seven-segment decoder/driver designed to decode BCD and drive gas filled seven-segment display tubes.

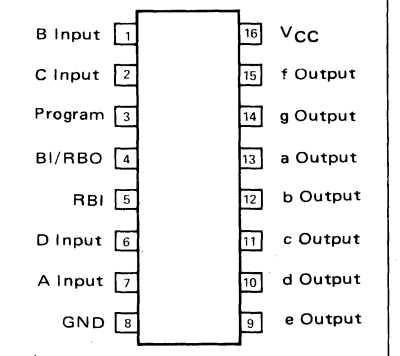
Decoding is performed by a 16X7 read only memory. Thus, for applications desiring other fonts, or applications not using standard BCD inputs, the ROM contents can be altered via metal mask change to produce any seven-segment combination for any 16 binary input combinations.

The output of the ROM is used to drive high voltage constant current sink generators. The current sinks of the DS8880 will withstand 80V output min. while those of DS8880-1 will withstand 100V. The current sinks are ratioed to the B output current as required for even illumination of the segments. Output currents may be varied over a 0.2 to 1.5mA range through use of the external current programming input.

Blanking input provides unconditional blanking of any output display, while the ripple blanking pins allow simple leading or trailing zero blanking.

PIN CONFIGURATION

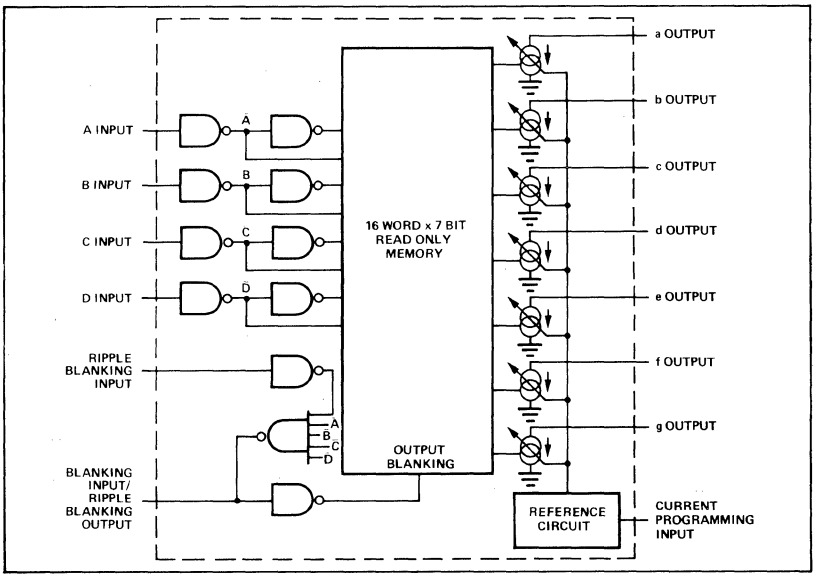
F,N PACKAGE



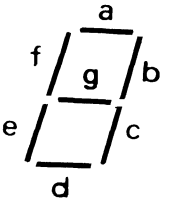
FEATURES

- **Current source outputs**
- **Adjustable output current—0.2 to 1.5mA**
- **High output breakdown voltage—110V TYP**
- **Suitable for multiplex operation**
- **Blanking and ripple blanking provisions**
- **Low fan-in and low power**

LOGIC AND CONNECTION DIAGRAMS



SEGMENT IDENTIFICATION



TRUTH TABLE

DECIMAL OR FUNCTION	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	DISPLAY
0	1	0	0	0	0	1	0	0	0	0	0	0	1	0
1	X	0	0	0	1	1	1	0	0	1	1	1	1	1
2	X	0	0	1	0	1	0	0	1	0	0	1	0	2
3	X	0	0	1	1	1	0	0	0	0	1	1	0	3
4	X	0	1	0	0	1	1	0	0	1	1	0	0	4
5	X	0	1	0	1	1	0	1	0	0	1	0	0	5
6	X	0	1	1	0	1	0	1	0	0	0	0	0	6
7	X	0	1	1	1	1	0	0	0	1	1	1	1	7
8	X	1	0	0	0	1	0	0	0	0	0	0	0	8
9	X	1	0	0	1	1	0	0	0	0	1	0	0	9
10	X	1	0	1	0	1	0	0	0	1	0	0	0	A
11	X	1	0	1	1	1	1	1	0	0	0	0	0	b
12	X	1	1	0	0	1	0	1	1	0	0	0	1	C
13	X	1	1	0	1	1	1	0	0	0	0	1	0	d
14	X	1	1	1	0	1	0	1	1	0	0	0	0	E
15	X	1	1	1	1	1	0	1	1	1	0	0	0	F
BI	X	X	X	X	X	0	1	1	1	1	1	1	1	
RBI	0	0	0	0	0	0	1	1	1	1	1	1	1	

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V_{CC}	7	V
Input voltage		
Except B1	6	V
B1	V_{CC}	
Segment output voltage		
DS8880	80	V
DS8880-1	100	V
Power dissipation*	600	mW
Operating temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10 sec)	300	°C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 5V unless otherwise specified.

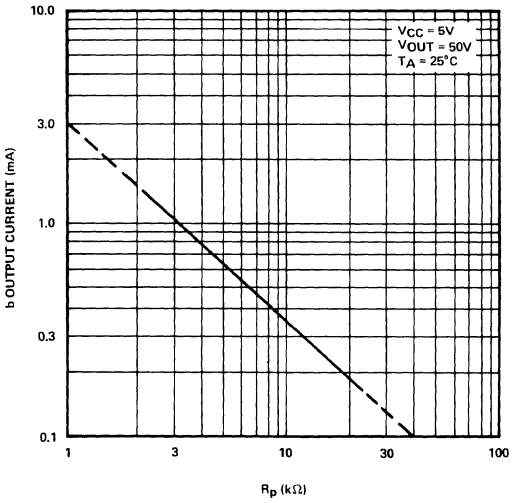
PARAMETER	TEST CONDITIONS	DS8880/8880-1			UNIT
		Min	Typ	Max	
Logic "1" input voltage	V_{CC} = 4.75V	2.0			V
Logic "0" input voltage	V_{CC} = 4.75V			0.8	V
Logic "1" output voltage (RBO)	V_{CC} = 4.75V, I_{OUT} = -200μA	2.4	3.7		V
Logic "0" output voltage (RBO)	V_{CC} = 4.75V, I_{OUT} = 8mA		0.13	0.4	V
Logic "1" input current (except BI)	V_{CC} = 5.25V, V_{IN} = 2.4V		2	15	μA
	V_{CC} = 5.25V, V_{IN} = 5.5V		4	400	μA
Logic "0" input current (except BI)	V_{CC} = 5.25V, V_{IN} = 0.4		-300	-600	μA
Logic "0" input current (BI)	V_{CC} = 5.25V, V_{IN} + 0.4V		-1.2	-2.0	mA
Power supply current	V_{CC} = 5.25V, all inputs = 0V, Rp = 2.2k		27	43	mA
Input diode clamp voltage	V_{CC} = 5V, I_{IN} = -12mA		-0.9	-1.5	V
Segment outputs:					
Outputs a, f, g on current ratio	All outputs = 50V, output b curr. = ref.	0.84	0.93	1.02	mA
Output c on current ratio	All outputs = 50V, output b curr. = ref.	1.12	1.25	1.38	mA
Output d on current ratio	All outputs = 50V, output b curr. = ref.	0.90	1.00	1.10	mA
Output e on current ratio	All outputs = 50V, output b curr. = ref.	0.99	1.10	1.21	mA
Output b on current	V_{CC} = 5V, V_{OUT} b = 50V, Rp = 18.1k	0.15	0.20	0.25	mA
	V_{CC} = 5V, V_{OUT} b = 50V, Rp = 7.03k	0.45	0.50	0.55	mA
	V_{CC} = 5V, V_{OUT} b = 50V, Rp = 3.40k	0.90	1.00	1.10	mA
	V_{CC} = 5V, V_{OUT} b = 50V, Rp = 2.20k	1.35	1.50	1.65	mA
Output saturation voltage	V_{CC} = 4.75V, I_{OUT} = 2mA, Rp = 1k ±5%		0.8	2.5	V
Output leakage current:					
DS8880	V_{OUT} = 75V, BI = 0V		.003	3	μA
DS8880-1	V_{OUT} = 95V, BI = 0V		.005	3	μA
Output breakdown voltage:					
DS8880	I_{OUT} = 250μA, BI = 0V	80	110		V
DS8880-1		100	110		V
Propagation delays:					
BCD input to segment output	V_{CC} = 5V		0.4	10	μs
BI to segment output	V_{CC} = 5V		0.4	10	μs
RBI to segment output	V_{CC} = 5V		0.7	10	μs
RBI to RBO	V_{CC} = 5V		0.4	10	μs

*NOTE

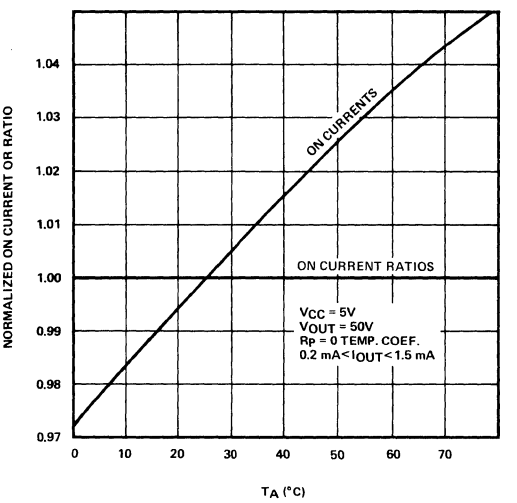
Min/max limits apply across the guaranteed operating temperature range of 0°C to 70°C unless otherwise specified. Positive current is defined as current into the referenced pin.

TYPICAL PERFORMANCE CHARACTERISTICS

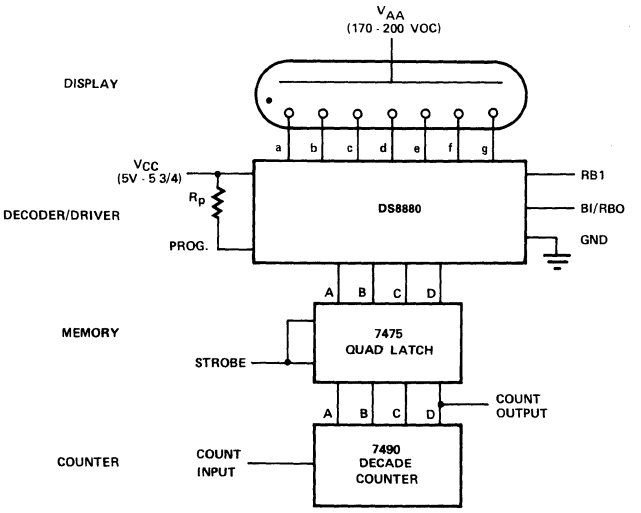
OUTPUT CURRENT PROGRAMMING



ON CURRENTS vs TEMPERATURE



TYPICAL APPLICATION



NE580-F,N

PRELIMINARY SPECIFICATION

Contact factory for product status.

DESCRIPTION

The NE580 is a dual bar-graph logic circuit designed to provide all the functions necessary to drive a gas discharge self-scan ™ bar-graph panel. The NE580 is configured to drive a 201 element bar-graph in either 5 or 6 phase operation. Phase number selection is obtained by applying a logic 0 or 1 level to the phase select pin. 3 phase operation for a 101 element device can be attained by a wire-or connection of adjacent cathode phase outputs.

The device inputs accept an analog voltage in the range 0 to 2.5V and performs an A/D conversion with reference to a fixed input voltage at the reference terminal. On-chip functions include a clock generator, linear ramp generator, control logic and ROM decoding. Output functions comprise 2 anode control lines, 2 overrange indication outputs, 6 cathode phase outputs and 1 cathode reset output. Refer to the system block diagram for clarification.

A minimum of external components are required for the whole conversion and display system shown in the typical application. The NE580 can be expanded to handle more analog channels using external comparators. Either LM393A or LM339A type comparators will function well. A few external low-cost logic packages can in addition provide binary or BCD encoded data to interface with a logic control system.

The device is supplied in a 22-pin plastic molded or ceramic dual-in-line package.

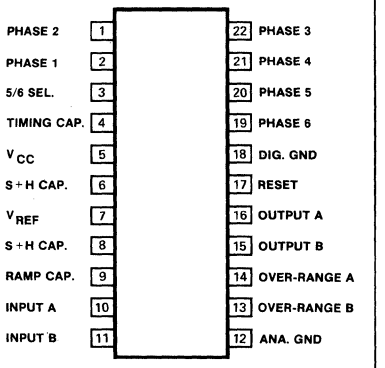
™-self-scan is a trademark of Burroughs Corporation.

FEATURES

- **Dual channel device**
- **Easily expandable to handle more channels.**
- **Single 5 volt supply**
- **3, 5 or 6 phase operation**
- **Can be custom masked for different cathode segment counts, (maximum 240)**
- **Equivalent 8-bit resolution of displayed information.**
- **Overrange indication outputs.**

PIN CONFIGURATION

F,N PACKAGE



ORDERING INFORMATION

Plastic DIL package—NE580N
Cerdip package—NE580F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage, V_{CC}	+7	V
Output voltage (all outputs)	$+V_{CC}$	V
Analog input voltage range	-0.3 to +7	V
Reference voltage input	$+V_{CC}$	V
Phase select input	+5.5	V
Analog/digital ground voltage differential	±0.3	V
Power dissipation		
plastic	500	mW
cerdip*	800	mW
Operating temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Soldering temperature (10sec)	300	°C

*NOTE

The plastic 22 pin package has a thermal impedance θ_{JA} of 120°C/W and the cerdip package, θ_{JA} of 75°C/W. Provided the maximum junction temperature is kept below 150°C then more power may be dissipated to a maximum of 1 watt.

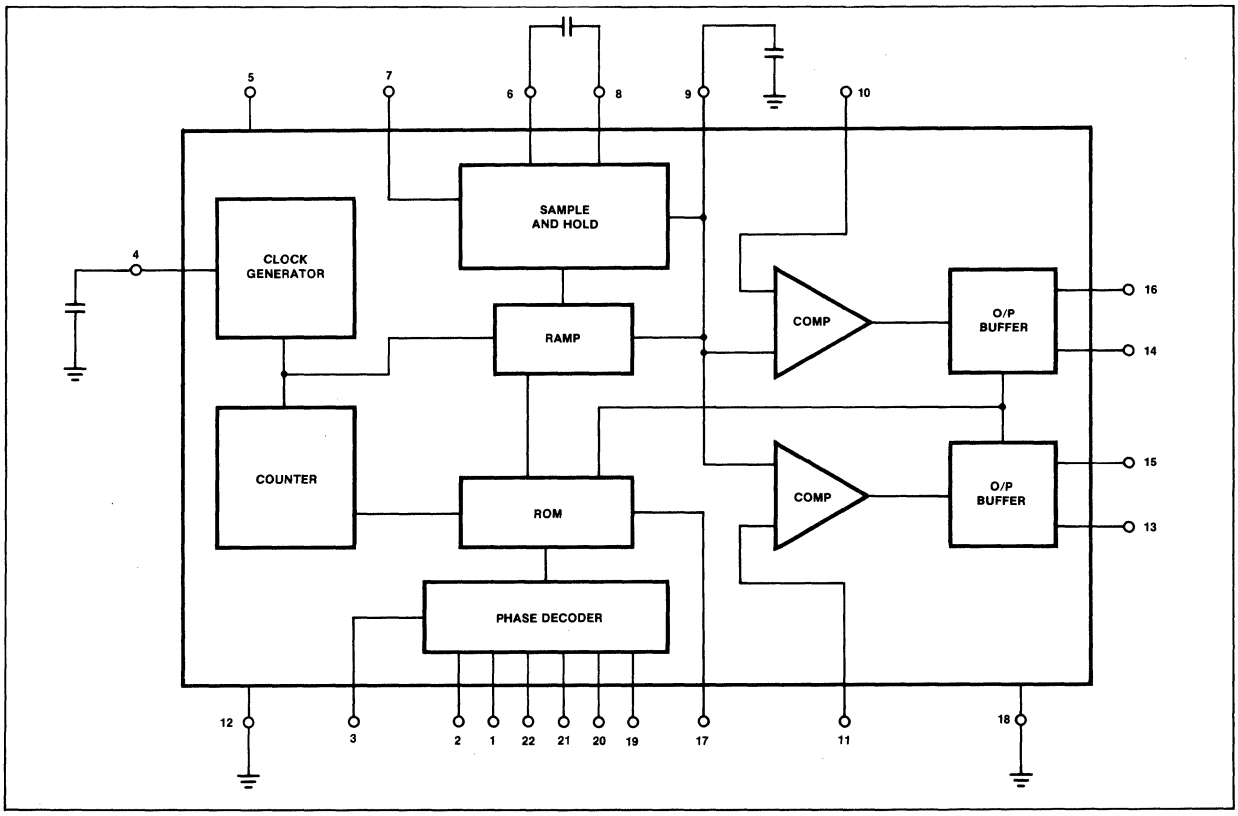
DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V$ unless otherwise specified.

	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Operating supply voltage range		4.75	5.0	5.25	V
V_{IN}	Input voltage range		0		2.5	V
V_{REF}	Applied reference voltage[1]		0		2.5	V
I_{BREF}	Bias current at reference voltage input	$V_{REF} = 2.5V$		500		nA
I_{IB}	Bias current at analog input	$V_{REF} = 2.5V$, $V_{IN} = 0V$		500		nA
$V_{OUT\ (1)}$	All outputs[2]	$I_{OUT} = -500\mu A$		3.5		V
$I_{OUT\ (1)}$	All outputs[2]	$V_{OUT} = 1.5V$		-1.0		mA
$I_{OUT\ (sc)}$	All outputs[2]	$V_{OUT} = 0V$		-1.5		mA
$V_{OUT\ (0)}$	All outputs	$I_{SINK} = 1.6mA$			0.4	V
F_C	Clock generator frequency	Timing capacitor $= .022\mu F$		25		KHz
Accuracy		$2V \leq V_{REF} \leq 2.5V$, $V_{IN} = V_{REF}$		±1		bar
I_{CC}	Supply current			50		mA

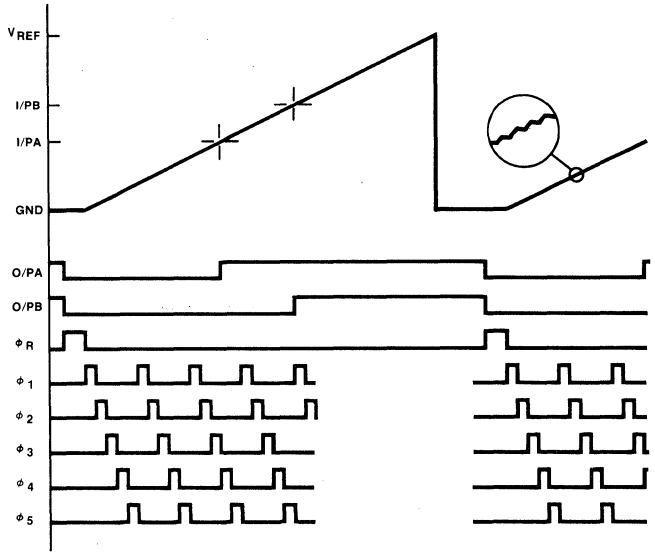
NOTES

1. Displayed accuracy is a function of reference voltage. Values of V_{REF} below 2 volts will impair conversion accuracy.
2. All logic outputs comprise an NPN transistor with 3kΩ pull-up resistor to 5 volts.

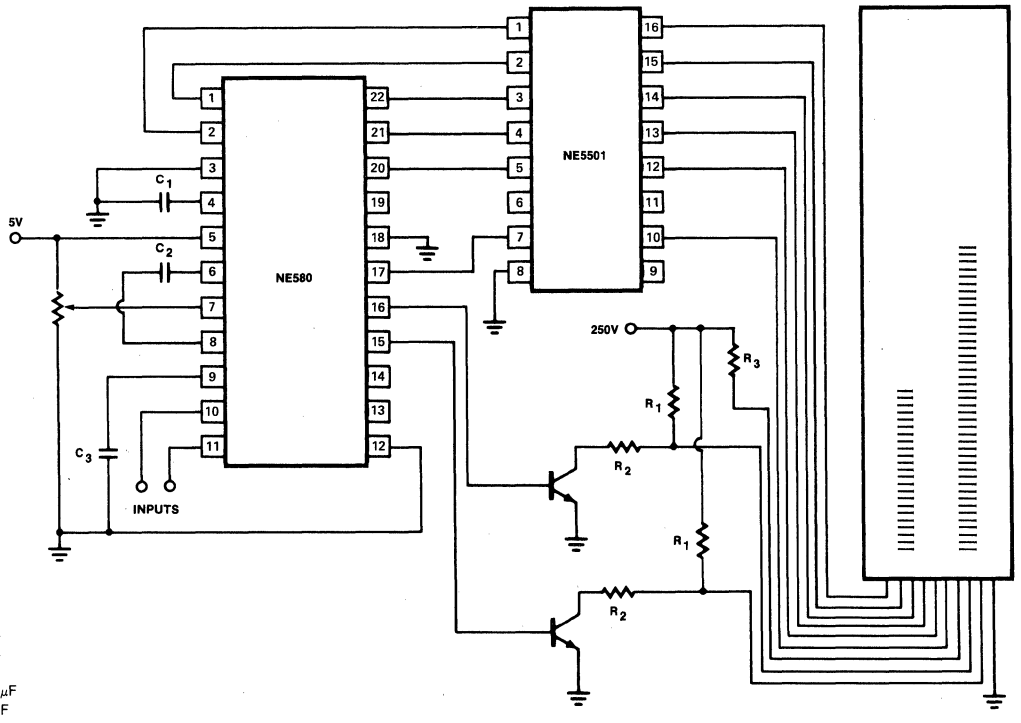
BLOCK DIAGRAM



TIMING DIAGRAM



TYPICAL APPLICATION



NOTES

R_1 = 14KΩ
R_2 = 14KΩ
R_3 = 1MΩ
C_1 = 0.022μF
C_2 = 0.47μF
C_3 = 0.47μF

Schematic shown is for a dual 5 phase 200 element bar-graph.

BAR-GRAPH SYSTEM OPERATION

The bar-graph display is a thick-film planar, gas discharge device. The principal of operation is called self-scan™, in which a neon glow-discharge is propagated from one cathode spot to another under one anode. The bar-graph device appears as a series of cathode bars arranged in a column. A glow discharge is continually propagated along the column from a keep-alive cathode at one end. Provided the scan rate for a whole column is above the eye flicker detection rate, then the glow appears as a continuous column of light.

BAR-GRAPH SIGNAL REQUIREMENTS

The NE580 comprises most of the electronic components necessary to interface an analog voltage level to the bar-graph display. Each column of the display requires an anode control signal and each cathode (usually from 4 to 7 in number) requires an interlaced logic signal of 1/N duty cycle (where N is the number of cathode phases). The pulse width of each cathode signal is of the order of 50 to 100μs. The cathode signals clock continuously throughout the frame period. The anode signal is on only for a proportion of time corresponding to the input voltage.

Thus

$$V_{IN} = V_{REF} \times \frac{T_{AN}}{200}$$

for a 200 element device, where T_{AN} is the number of cathode clock cycles for which the anode is on. Figure 2 illustrates the relative output phasing of the linear ramp cathode and anode lines for 5 phase operation.

CIRCUIT OPERATION

The NE580 provides the circuitry to generate all these signals to the point where they drive the high voltage display elements. An on-chip clock generator drives the master counter and cathode phase generator.

The clock also gates a constant current source which charges the ramp capacitor with a staircase waveform of equal increment steps. These steps correspond to the cathode segments. There are two steps per segment so that the comparison of input voltage with respect to the ramp is made at the mid-point of each segment. The master counter inhibits the current source and discharges the ramp after 200 cathode counts. At the 200th count, the ramp voltage is strobed into a sample-and-hold amplifier. This voltage is compared with the reference voltage and a signal fed back to the ramp constant current source. Hence, the maximum value of the ramp will be adjusted to the same level as the reference voltage.

The anode output goes low at the beginning of each frame and goes high again when the ramp voltage becomes greater than the input voltage. If the ramp reaches full scale before setting the anode output high, then the over-range output goes low and stays low until the end of the next frame if the input signal recovers to an in-range value. A continuing over-range signal will cause the output to go low indefinitely.

Because the ramp is the result of accumulated charge on the integrating capacitor, it is inherently monotonic; thus, each step is greater than the previous one by the expression

$$\Delta V = \frac{\Delta Q}{C}$$

Errors in the ramp can occur due to

1) Starting the ramp from a voltage other than zero. Some capacitors have a time related polarization.
2) Sag in the sampled and hold ramp voltage causing an inconstant charging current.
3) Offset errors in the sample and hold amplifier.
4) Leakage currents into or out of the ramp capacitor.

The zero starting point is achieved by using a very low offset transistor to fully discharge the ramp capacitor to within 1-5mV of ground. The maximum voltage end of the ramp is made stable by using a large value capacitor to overcome the effects of any leakage.

The classical histogram has cells which represent a nominal value plus/minus 1/2 cell width. The NE580 works in the same way. This is realized by having a clock rate which is twice the cathode switching rate, and so the staircase ramp has two steps per cathode dwell time. Each comparison step is made at the nominal cell value plus 1/2 cell, and the anode remains on (anode output low) as long as the ramp voltage is less than the input voltage.

DESCRIPTION

The NE582 is a general interface device comprising a high current output transistor and drive circuitry in each of 6 elements. Each output transistor is individually capable of sinking 400mA with a typical saturation voltage of 0.5V. Input loading is such that direct interfacing with P-MOS, N-MOS, C-MOS or TTL is possible.

The NE582 has applications as a LED display driver, low voltage relay/lamp drivers and many others where high current capability without speed constraints is required.

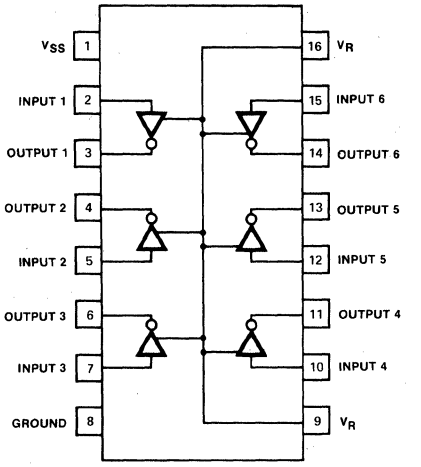
The NE582 is supplied in a 16-pin high dissipation dual-in-line plastic package.

FEATURES

- **Low saturation voltage (typically 0.5V) for minimum power dissipation**
- **High output sink current capability—400mA**
- **Low input current loading for MOS compatibility**
- **Low standby power consumption**
- **Suitable for 3 volt battery operation**
- **Inputs/outputs are compatible with 75494**

PIN CONFIGURATION

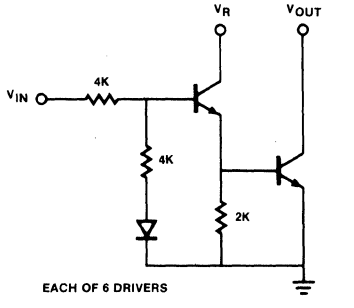
N PACKAGE



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Input voltage range[1]	-12 to V_{SS}	V
Output voltage[2]	10	V
Output to input voltage differential	10	V
Voltage at V_{SS} (pin 1)	10	V
Output current—each output	400	mA
Output current—all outputs	800	mA
Continuous total power dissipation at or below 25°C[3]	800	mW
Current in V_R (pin 9 or 16)	25	mA
Operating free-air temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature 1/16 inch from case for 10sec	260	°C

EQUIVALENT SCHEMATIC



NOTES

1. The inputs are the only pins which may be negative with respect to ground.
2. Voltage values are with respect to ground.
3. Above 25°C, derate power dissipation at 6.25mW/°C.

NE582-N

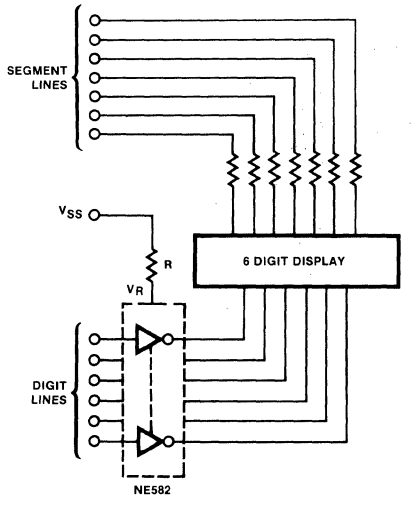
ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $70°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{OL}	Low level output voltage	V_{IN} I_R I_{OL} V mA mA 3 2 20 6.5 12 250 6.5 20 400 R_{IN} = 1K (Series input resistance)		 .025 .320 .500	 .060 .450 .750	 V V V
I_{OH}	High level output current	V_{OH} = 10V, I_{IN} = 40μA V_{OH} = 10V, V_{IN} = 0.5V			400 400	μA μA
I_{IN}	Input current at maximum Input voltage	V_{IN} = 10V, I_{OL} = 20mA, I_R = 2mA		2.2	3.3	mA
V_R I_{SS}	 Current into pin 1	V_{IN} = 6.5V, I_R = 6mA, I_{OL} = 80mA V_{SS} = 10V		.9	1.5 100	V μA

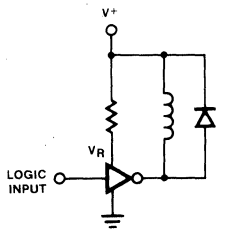
AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Switching characteristics					
T_{PLH}	Propagation delay, low to high level input	R_R = 680Ω R_L = 39Ω C_L = 15pF		300		ns
T_{PHL}	Propagation delay, high to low level input	V_{IH} = 7.5V V_{IL} = 0V $t_r = t_f \leq 10$ns $t_w = 1\mu$s PRR = 100kHz		30		ns

TYPICAL APPLICATION FOR DIGIT DRIVING OF AN LED DISPLAY



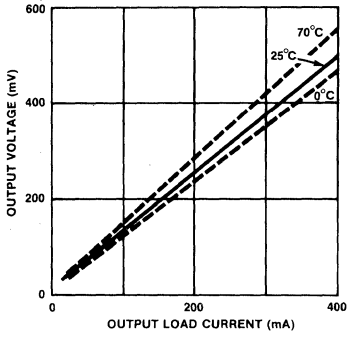
1/6 NE582 AS A RELAY DRIVER



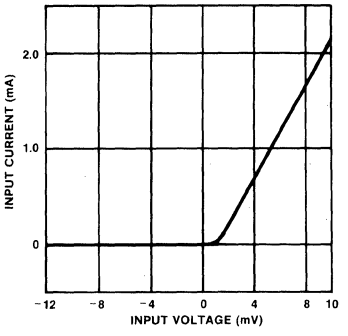
1/6 NE582 AS A RELAY DRIVER

PRELIMINARY SPECIFICATION

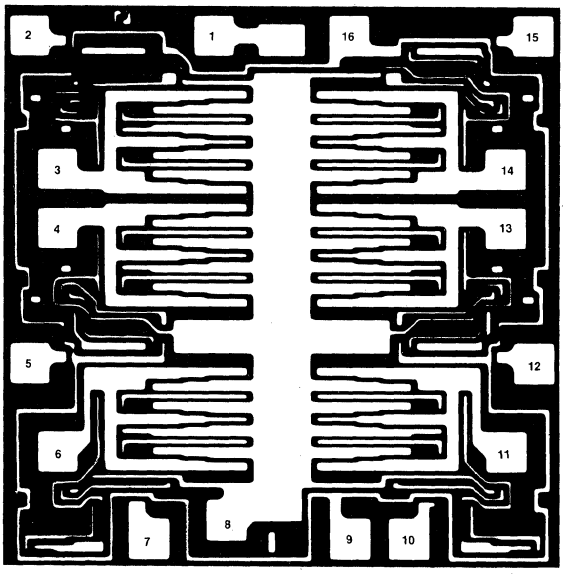
OUTPUT SATURATION VOLTAGE AS A FUNCTION OF OUTPUT LOAD CURRENT, I_R = 25mA V_{IN} = 6.5 VOLTS



INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE, I_R = 25mA, V_{SS} = 10V, T_A = 25°C



CHIP LAYOUT



NE584-F,N

DESCRIPTION

The NE584 is a Cathode Driver for multiplexed, 7-segment gas discharge displays.

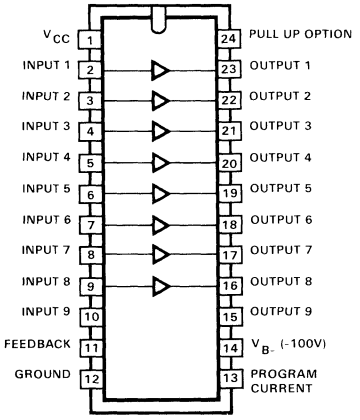
The display segments are driven by floating current sources maintaining uniform brightness across the display panel with a minimum of system components as shown in the Display Drivers illustration. A current feedback circuit is included to adjust the anode voltage steady under optimum load conditions. The maximum voltage ripple is typically held to less than 1V.

FEATURES

- **Capable of driving up to 9 segments**
- **1 external resistor provides for current programming**
- **Minimum component count for system cost effectiveness**
- **Segment current programmability for optimum operation of all character sizes**
- **Internal current limiting protection**
- **Internal feedback network ensures optimum operating conditions**
- **High system reliability**
- **Compatible with MOS and TTL inputs**

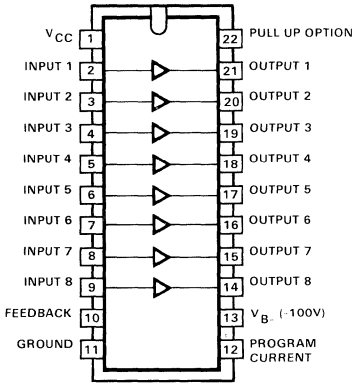
PIN CONFIGURATION

F,N PACKAGE



Order part no. NE584-9

N,F PACKAGE

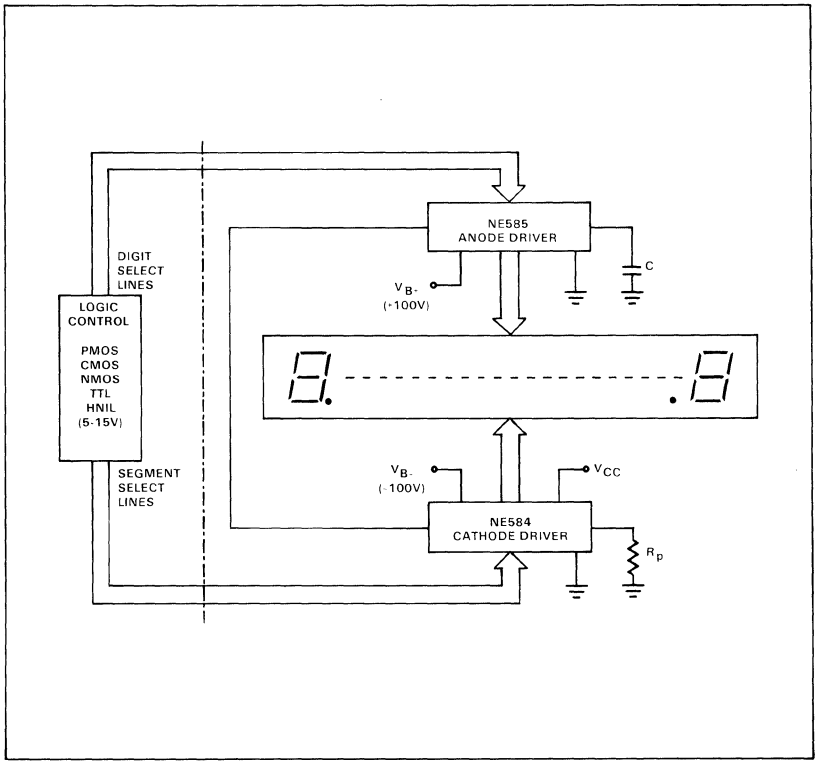


Order part no. NE584-8

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
	Supply voltage		V
V_{B-}	Negative	-110	
V_{CC}	Logic	+15	
V_{IN}	Input voltage	+15	V
I_P	Program current	1	mA
T_J	Junction temperature	150	°C
T_A	Ambient operating temperature range	0 to 70	°C
T_S	Storage temperature range	-65 to 150	°C
T_{sold}	Soldering temperature (10sec)	300	°C
P_D	Power dissipation at 25°C		mW
	Plastic DIP—22 and 24 pin	1000	
	Cerdip—22 and 24 pin	1200	

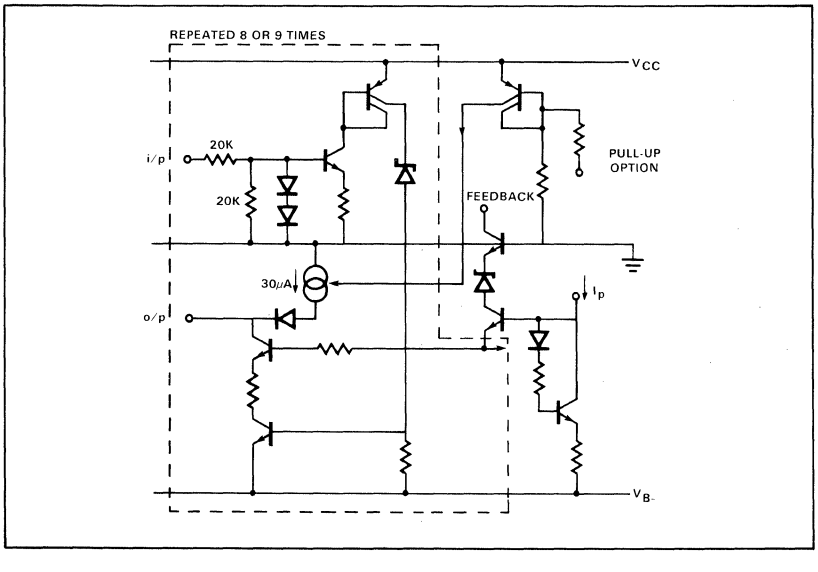
DISPLAY DRIVERS



DC ELECTRICAL CHARACTERISTICS V_{B-} = -100V, V_{CC} = 5 to 15V

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{B-}	Supply voltage	Operating voltage range	-90	-100	-110	V
	Input voltage	For TTL type inputs				V
V_{IH}	High		2.6			
V_{IL}	Low				1.1	
I_I	Input current	V_{IN} = 2.6V		60	200	μA
		V_{IN} = 6V	115	230	460	
		V_{IN} = 15V	340	680	1360	
I_{IH}	High	For MOS type inputs	90			
I_{IL}	Low				5	
	Current ratio between any 2 outputs	T_A = 25°C, I_P = 200 or 600μA	.9	1	1.1	mA
	Output current to program current ratio	I_P = 200 or 600μA				mA
		T_A = 25°C	4.5	5	5.5	
		T_A = 0-70°C	4	5	6	
V_{OUT}	Output voltage					V
	On	I_P = 100μA, I Seg = 450μA		5		
		I_P = 100μA, I Seg = 1μA		1		
		I_P = 600μA, I Seg = 2.7mA		14		
		I_P = 600μA, I Seg = 1μA		3		
	Off	With respect to V_{B-}		V_{B-} + 40		
	On breakdown	I_P = 400μA, I Seg = 3mA		V_{B-} + 55		
	Off breakdown	I Seg = 10μA	90			
	Output leakage current					μA
	Off	I_{OUT} = V_{B-} +90V			10	
I_f	Feedback current	I_P = 200μA, V_{IN} ≥ 3.5V, I Seg = 0				
		1 segment on	140	200	260	μA
		8 segments on	1.1	1.6	2.1	mA
	Propagation delay	C_{OUT} = 15pF		5		μs
	Power supply current	All inputs low, V_{FB} = 15V,				mA
I_{CC}	Logic	I_P = 100μA, V_{CC} = 15V			3	
I_{B-}	Negative			1	2	
	Pull up option current	V_{CC} = 5V. Pin 24 or 22 = 0V		0.6		mA

EQUIVALENT SCHEMATIC



NE585-F,N

DESCRIPTION

The NE585 is an Anode Driver for multiplexed, 7-segment gas discharge displays.

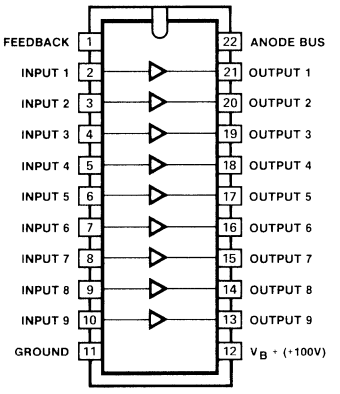
The display segments are driven by floating current sources maintaining uniform brightness across the display panel with a minimum of system components as shown in the Display Drivers illustration. A current feedback circuit is included to adjust the anode voltage steady optimum load conditions. The maximum voltage ripple is typically held to less than 1V.

FEATURES

- **Capable of driving up to 9 digits**
- **Minimum component count for system cost effectiveness**
- **Segment current programmability for optimum operation of all character sizes**
- **Internal current limiting protection**
- **Internal feedback network ensures optimum operating conditions**
- **High system reliability**
- **Compatible with MOS and TTL inputs**

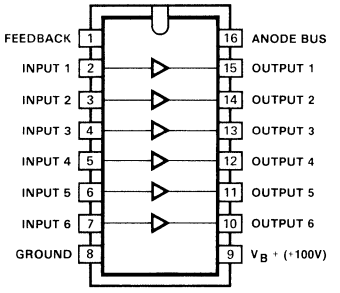
PIN CONFIGURATION

F,N PACKAGE



Order part no. NE585-9

N,F PACKAGE



Order part no. NE585-6

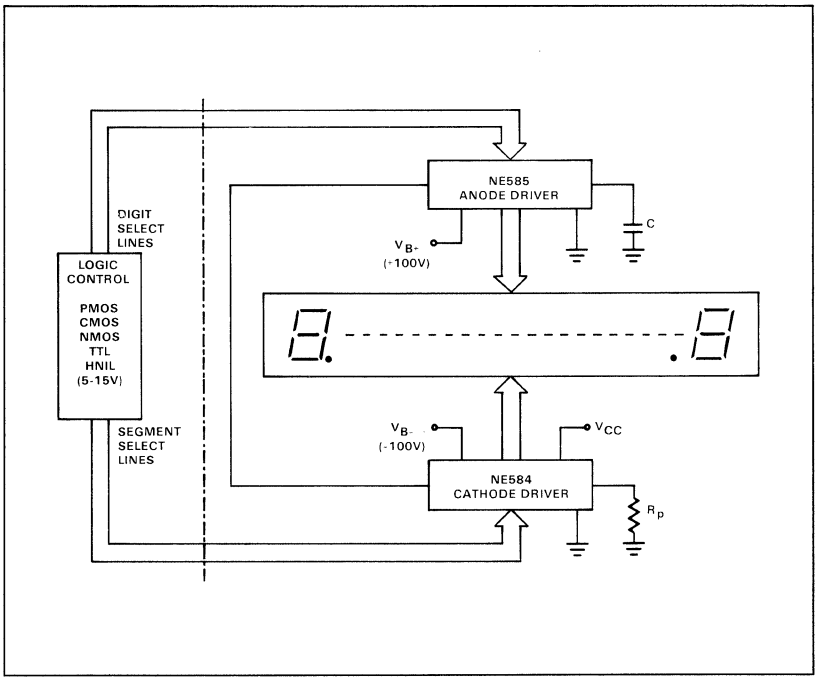
ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{B+}	Positive supply voltage	+110	V
V_A	Anode bus voltage[1]	90 or VB+	V
V_{IN}	Input voltage	+15	V
T_J	Junction temperature	150	°C
T_A	Ambient operating temperature range	0 to 70	°C
T_S	Storage temperature range	-65 to 150	°C
T_{sold}	Soldering temperature (10secs)	300	°C
P_D	Power dissipation at 25°C		mW
	Plastic DIP—16 pin	800	
	Plastic DIP—22 pin	1000	
	Cerdip—16 pin	1000	
	Cerdip—22 pin	1200	

NOTE

Whichever is the lesser of these values is the maximum allowable anode bus voltage

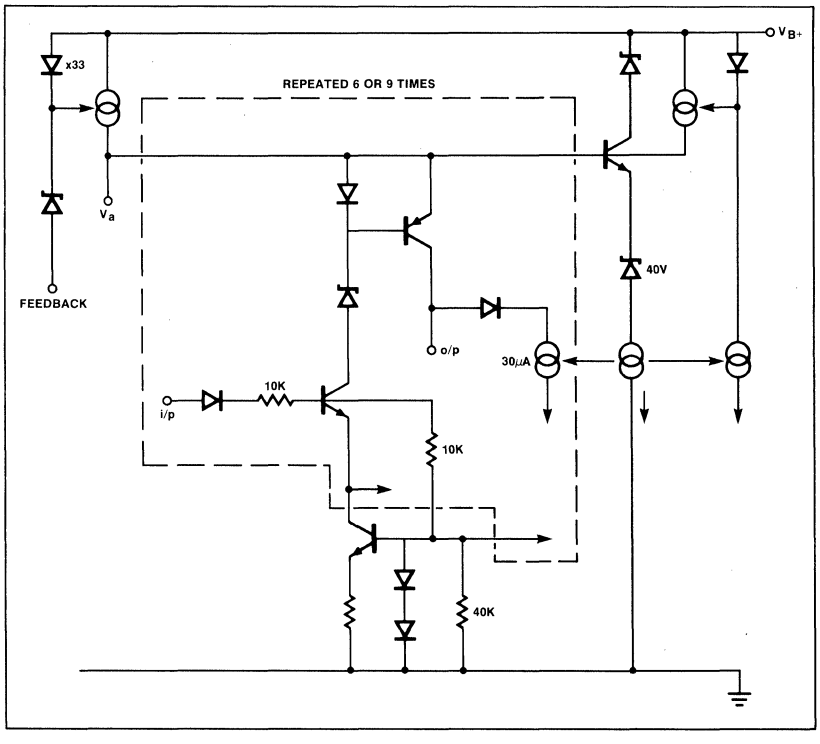
DISPLAY DRIVERS



DC ELECTRICAL CHARACTERISTICS V_{B+} = 100V, V_A = 60V unless otherwise specified

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{B+}	Positive supply voltage	Operating voltage range	90	100	110	V
	Input voltage	For TTL type inputs				V
V_{IH}	High		2.6			
V_{IL}	Low				1.1	
I_I	Input current	V_{IN} = 2.6V		60	200	μA
		V_{IN} = 6V	100	200	400	
		V_{IN} = 15V	325	650	1300	
I_{IH}	High	For MOS type inputs	90			
I_{IL}	Low				5	
	Feedback current gain (= I_A/I_F)	I_F pulse width < 500μs, Duty cycle < 20%				dB
		I_F = 2mA	24	33	40	
		I_F = 200μA	26	33	40	
V_{OUT}	Output voltage	I_{OUT} = -10mA				V
	On				V_A-2	
	Off			V_A-38		
	Breakdown	V_{B+} = 100V, V_A = 90V, I_{OUT} = -100μA	V_A-55			
	Available output current	$V_O = V_A$-5V, V_{IN} = 3.5V		35		mA
	Leakage current					μA
	Output	$V_A - V_{OUT}$ = 50V			-10	
	Input	V_{IN} = 0			-10	
	Propagation delay	C_{OUT} = 15pF		5		μs
I_{B+}	Power supply current	1 input high, All others open		1.6	2.5	mA

EQUIVALENT SCHEMATIC



SECTION II
D/A-A/D CONVERTERS

MC1508-8/MC1408-8/MC1408-7 -F,N

DESCRIPTION

The MC1508/MC1408 series of 8-bit monolithic digital-to-analog converters provide high speed performance with low cost. They are designed for use where the output current is a linear product of an 8-bit digital word and an analog reference voltage.

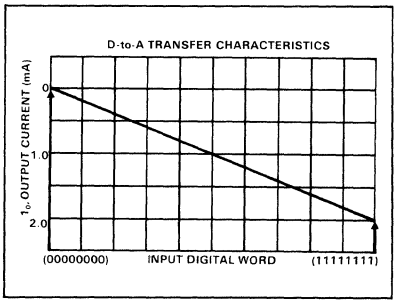
FEATURES

- **Fast settling time—300ns (typ)**
- **Relative accuracy ±0.19% (max error)**
- **Non-inverting digital inputs are TTL and CMOS compatible**
- **High speed multiplying rate 4.0mA/μs (input slew)**
- **Output voltage swing +.5V to -5.0V**
- **Standard supply voltages + 5.0V and -5.0V to -15V**
- **Military qualifications pending**

APPLICATIONS

- **Tracking A-to-D converters**
- **2½-digit panel meters and DVM's**
- **Waveform synthesis**
- **Sample and hold**
- **Peak detector**
- **Programmable gain and attenuation**
- **CRT character generation**
- **Audio digitizing and decoding**
- **Programmable power supplies**
- **Analog-digital multiplication**
- **Digital-digital multiplication**
- **Analog-digital division**
- **Digital addition and subtraction**
- **Speech compression and expansion**
- **Stepping motor drive**

TYPICAL PERFORMANCE CHARACTERISTICS



CIRCUIT DESCRIPTION

The MC1508/MC1408 consists of a reference current amplifier, and R-2R ladder, and 8 high speed current switches. For many applications, only a reference resistor and reference voltage need be added.

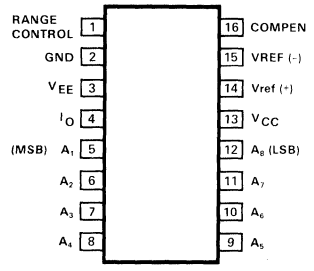
The switches are non-inverting in operation; therefore, a high state on the input turns on the specified output current component.

The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching, and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the switches. Note that there is always a remainder current which is equal to the least significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992mA for a 2.0mA reference amplifier current if the NPN current source pair is perfectly matched.

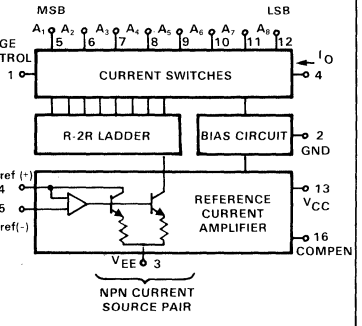
PIN CONFIGURATION

F,N PACKAGE*



*N = Plastic DIP
F = Cerdip

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATNGS

T_A = +25°C unless otherwise specified

PARAMETER		RATING	UNIT
V_{CC}	Power supply voltage		V
V_{EE}	Positive	+5.5	
V_5-V_{12}	Negative	-16.5	
V_O	Digital input voltage	+5.5, 0	V
I_{14}	Applied output voltage	+0.5, -5.2	V
V_{14},V_{15}	Reference current	5.0	mA
	Reference amplifier inputs	V_{CC}, V_{EE}	V
P_D	Power dissipation (package limitation)		mW
	Ceramic package	1000	
	Plastic package	800	
T_A	Operating temperature range		°C
	MC1508	-55 to +125	
	MC1408	0 to +75	
T_{stg}	Storage temperature range	-65 to +70	°C

DC ELECTRICAL CHARACTERISTICS[1]

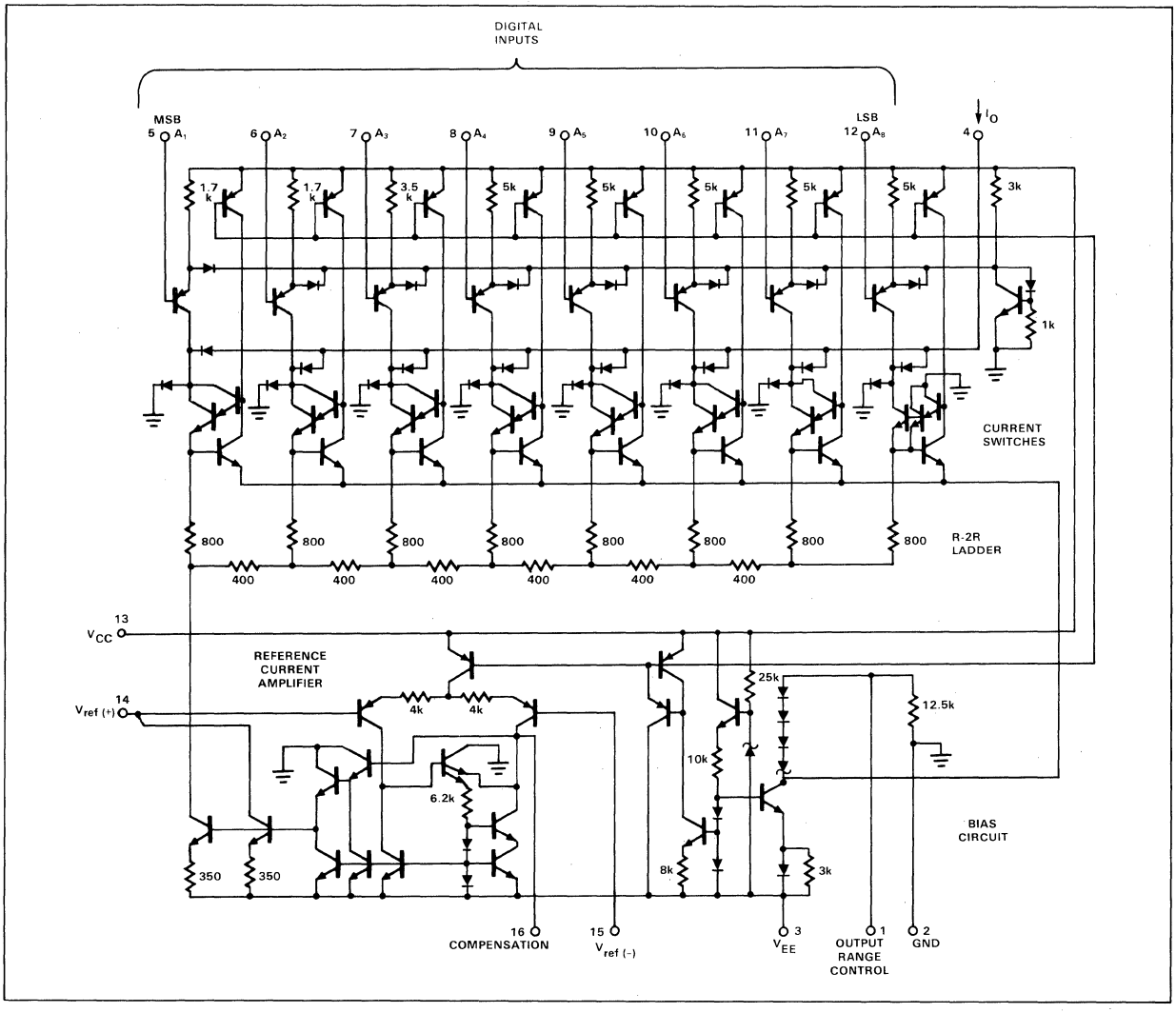
V_{CC} = +5.0Vdc, V_{EE} = -15Vdc, $\frac{V_{ref}}{R_{14}}$ = 2.0mA unless otherwise specified.
MC1508: T_A = -55°C to 125°C. MC1408: T_A = 0°C to 70°C

PARAMETER		TEST CONDITIONS	MC1508-8			MC1408-8			MC1408-7			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
E_r	Relative accuracy	Error relative to full scale I_O, Figure 3			±0.19			±0.19			±0.39	%
t_s	Setting time[1]	To within 1/2 LSB, includes t'PLH, T'A = +25°C, Figure 4		300			300			300		ns
	Propagation delay time											ns
t_{PLH}	Low-to-high	T_A = +25°C, Figure 4		30	100		30	100		30	100	
t_{PHL}	High-to-low											
TCI_O	Output full scale current drift			-20			-20			-20		PPM/°C
	Digital input logic level (MSB)											Vdc
V_{IH}	High	Figure 5	2.0			2.0			2.0			
V_{IL}	Low				0.8			0.8			0.8	
	Digital input current (MSB)	Figure 5										mA
I_{IH}	High	V_{IH} = 5.0V		0	0.04		0	0.04		0	0.04	
I_{IL}	Low	V_{IL} = 0.8V		-0.4	-0.8		-0.4	-0.8		-0.4	-0.8	
I_{15}	Reference input bias current	Pin 15, Figure 5		-1.0	-3.0		-1.0	-3.0		-1.0	-3.0	μA
I_{OR}	Output current range	Figure 5										mA
		V_{EE} = -5.0V	0	2.0	2.1	0	2.0	2.1	0	2.0	2.1	
		V_{EE} = -6.0V to -15V	0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	
I_O	Output current	Figure 5										
		V_{ref} = 2.000V, R14 = 1000Ω	1.9	1.99	2.1	1.9	1.99	2.1	1.9	1.99	2.1	mA
$I_{O(min)}$	Off-state	All bits low		0	4.0		0	4.0		0	4.0	μA
V_O	Output voltage compliance	$E_r \leq 0.19\%$ at T_A = +25°C, Figure 5										Vdc
		V_{EE} = -5V			-0.6, +0.5			-0.6, +0.5			-0.6, +0.5	
		V_{EE} below -10V			-5.0, +0.5			-5.0, +0.5			-5.0, +0.5	
SRI_{ref}	Reference current slew rate	Figure 6		4.0			4.0			4.0		mA/μs
$PSRR_{(-)}$	Output current power supply sensitivity	I_{ref} = 1mA		0.5	2.7		0.5	2.7		0.5	2.7	μA/V
	Power supply current											mA
I_{CC}	Positive	All bits low, Figure 5		+13.5	+22		+13.5	+22		+13.5	+22	
I_{EE}	Negative			-7.5	-13		-7.5	-13		-7.5	-13	
	Power supply voltage range											Vdc
V_{CCR}	Positive	T_A = +25°C, Figure 5	+4.5	+5.0	+5.5	+4.5	+5.0	+5.5	+4.5	+5.0	+5.5	
V_{EER}	Negative		-4.5	-15	-16.5	-4.5	-15	-16.5	-4.5	-15	-16.5	
P_D	Power dissipation	All bits low, Figure 5										mW
		V_{EE} = -5.0Vdc		105	170		105	170		105	170	
		V_{EE} = -15Vdc		190	305		190	305		190	305	
		All bits high, Figure 5										
		V_{EE} = -5.0Vdc		90			90			90		
		V_{EE} = -15Vdc		160			160			160		

NOTES

1. All bits switched

EQUIVALENT CIRCUIT SCHEMATIC



FUNCTIONAL DESCRIPTION

Reference Amplifier Drive and Compensation

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current (I_{14}) must always flow into pin 14 regardless of the setup method or reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 1. The reference voltage source supplies the full current I_{14}. For bipolar reference signals, as in the multiplying mode, R_{15} can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R_{15} with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R_{14} to maintain proper phase margin; for R_{14} values of 1.0, 2.5 and 5.0kΩ, minimum capacitor values are 15, 37, and 75pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

A negative reference voltage may be used if R_{14} is grounded and the reference voltage is applied to R_{15} as shown in Figure 2. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 3.0V above the V_{EE} supply. Bipolar input signals may be handled by connecting R_{14} to a positive reference voltage equal to the peak positive input level at pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0V logic supply is not recommended as a reference voltage. If a well regulated 5.0V supply which drives logic is to be used as the reference, R_{14} should be decoupled by connecting it to +5.0V through another resistor and bypassing the junction of the 2 resistors with 0.1μF to ground. For reference voltages greater than 5.0V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high inpedance such as a transistor current source, none of the above compensation methods apply and

the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage on pin 4 is restricted to a range of -0.6 to +0.5V at -24° C, due to the current switching methods employed in the MC1508/MC1408. When a current switch is turned off, the positive voltage on the output terminal can turn on the output diode and increase the output current level. When a current switch is turned on, the negative output voltage range is restricted. The base of the termination circuit Darlington transistor is 1 diode voltage below ground when pin 1 is grounded, so a negative voltage below ground when pin 1 is grounded, so a negative voltage below the specified safe level will drive the low current device of the Darlington into saturation, decreasing the output current level.

The negative output voltage compliance of the MC1508/MC1408 may be extended to -5.0V by opening the circuit at pin 1. The negative supply voltage must be more negative than -10V. Using a full scale current of 1.992mA and load resistor of 2.5kΩ between pin 4 and ground will yield a voltage output of 256 levels between 0 and -4.980V. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500Ω do not significantly affect performance, but 2.5kΩ load increases worst case settling time to 1.2μs (when all bits are switched on). Refer to the subsequent text section on settling time for more details on output loading.

If a power supply value between -5.0V and -10V is desired, a voltage of between 0 and -5.0V may be applied to pin 1. The value of this voltage will be the maximum allowable negative output swing.

Output Current Range

The output current maximum rating of 4.2mA may be used only for negative supply voltages more negative than -7.0V, due to the increased voltage drop across the 350Ω resistors in the reference current amplifier.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the MC1508/MC1408 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the MC1508/MC1408 has a very low full scale current drift with temperature.

The MC1508/±MC1408 series is guaranteed accurate to within ±1/2 LSB at +25° C at a full scale output current of 1.992mA. This corresponds to a reference amplifier output current drive to the ladder network of 2.0mA, with the loss of 1 LSB = 8.0μA which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in Figure 3. The 12-bit converter is calibrated for a full scale output current of 1.992mA. This is an optional step since the MC1508/MC1408 accuracy is essentially the same between 1.5 and 2.5mA. Then the MC1508/MC1408 circuits' full scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. Sixteen-bit accuracy implies a total error ±1/2 of 1 part in 65,536, or ±0.00076%, which is much more accurate than the ±0.19% specification provided by the MC1508/MC1408.

Multiplying Accuracy

The MC1508/MC1408 may be used in the multiplying mode with 8-bit accuracy when the reference current is varied over a range of 256:1. The major source of error is the bias current of the termination amplifier. Under worst case conditions, these 8 amplifiers can contribute a total of 1.6μA extra current at the output terminal. If the reference current in the multiplying mode ranges from 16μA to 4.0mA, the 1.6μA contributes an error of 0.1 LSB. This is well within 8-bit accuracy.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the MC1508/MC1408 in monotonic for all values of reference current above 0.5mA. The recommended range for operation with a dc reference current is 0.5 to 4.0mA.

Settling Time

The worst case switching condition occurs when all bits are switched on, which corresponds to a low-to-high transition for all bits. This time is typically 300ns for settling to within ±1/2 LSB for 8-bit accuracy and 200ns to 1/2 LSB for 7-bit accuracy. The turnoff is typically under 100ns. These times apply when $R_L \leq 500\Omega$ and C_O 25pF.

The slowest single switch is the least significant bit, which turns on and settles in 250ns and truns off in 80ns. In applications where the D-to-A converter functions in a positive going ramp mode, the worst case switching condition does not occur, and a settling time of less than 300ns may be realized. Bit A7 turns on in 200ns and off in 80ns, while bit A6 turns on in 150ns and off in 80ns.

The test circuit of Figure 4 requires a smaller voltage swing for the current switches due to internal voltage clamping in MC1508/MC1408. A 1.0kΩ load resistor from pin 4 to ground gives a typical settling time of 400ns. Thus, it is voltage swing and not the output R_C time constant that determines settling time for most applications.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

TEST CIRCUITS

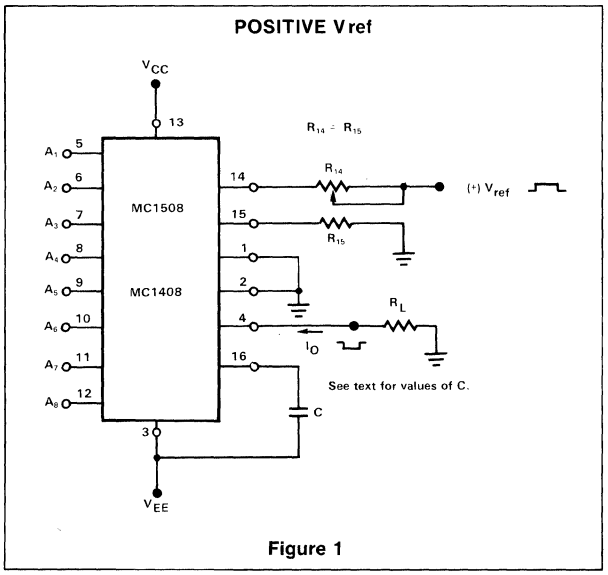


Figure 1

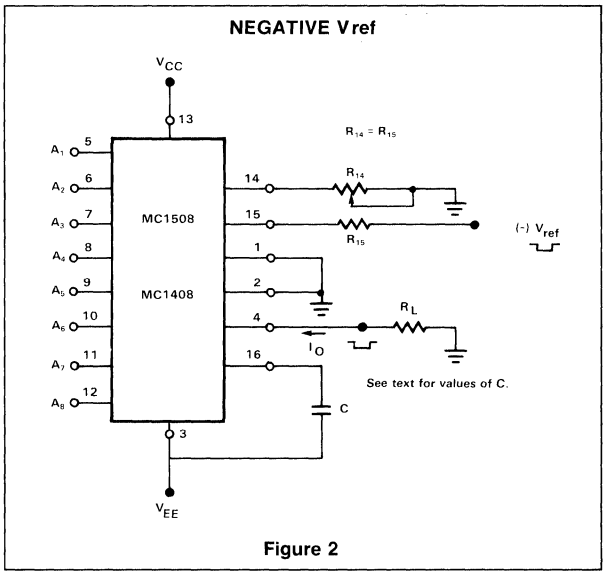


Figure 2

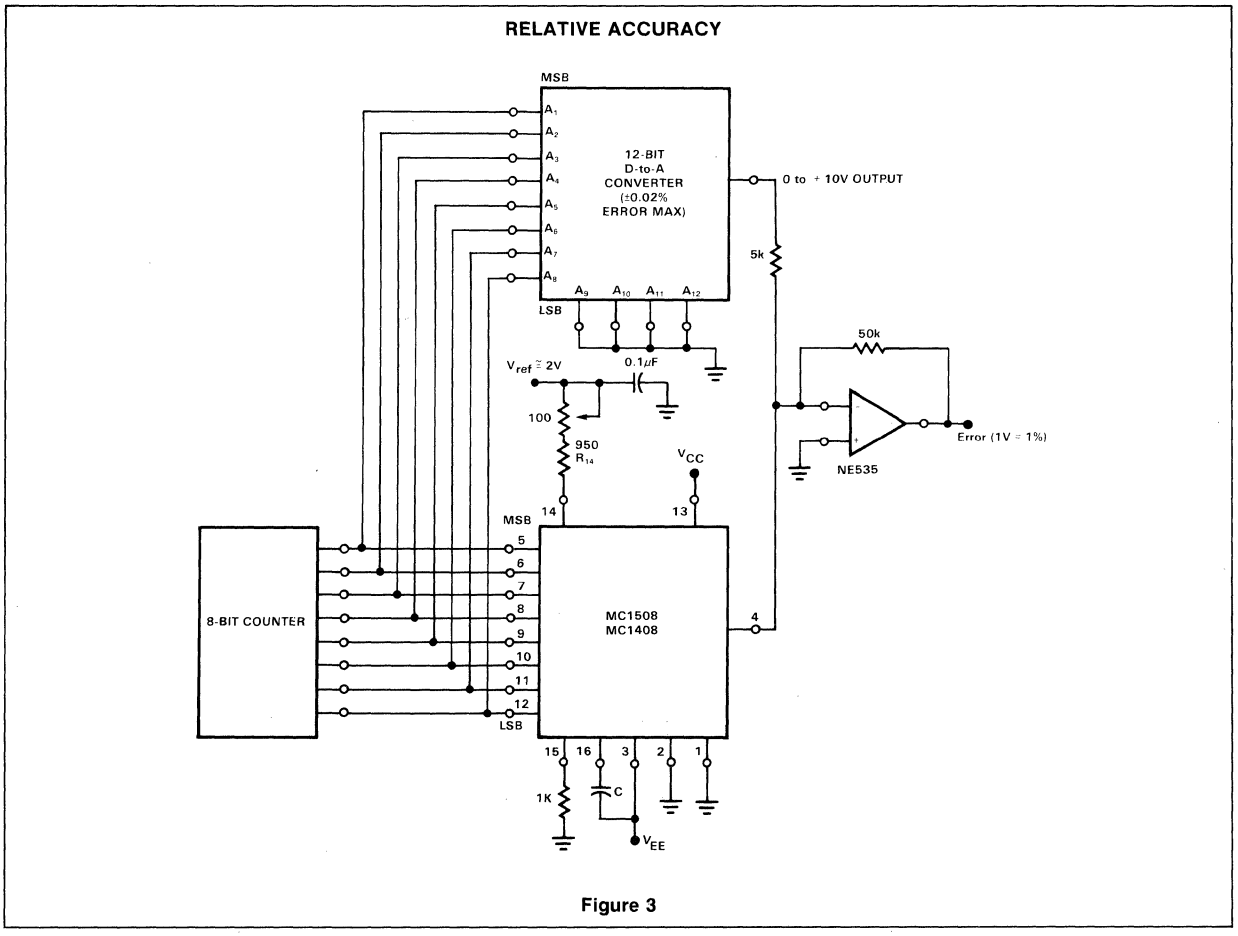


Figure 3

TEST CIRCUITS (Cont'd)

TRANSIENT RESPONSE AND SETTLING TIME

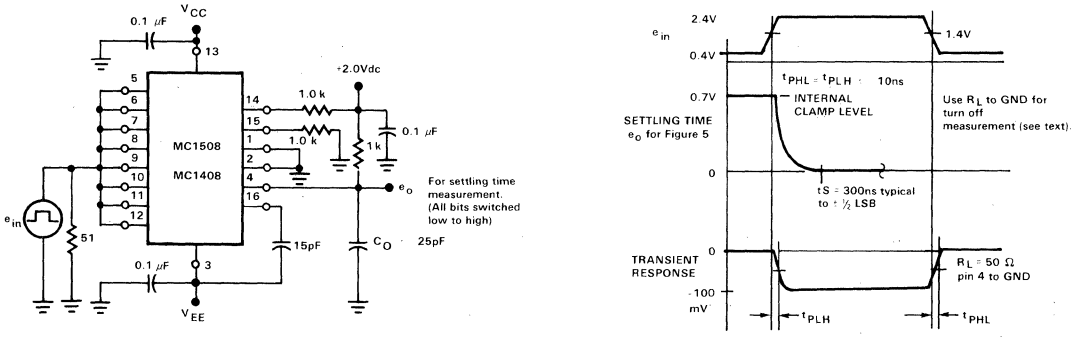
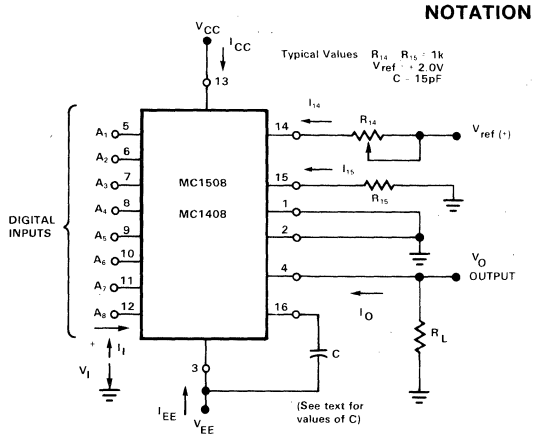


Figure 4

NOTATION DEFINITIONS



V_I and I_I apply to inputs A_1 thru A_8

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left\{\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256}\right\}$$

where $K \cong \frac{V_{ref}}{R_{14}}$

and A_N = "1" if A_N is at high level
A_N = "0" if A_N is at low level

Figure 5

REFERENCE CURRENT SLEW RATE MEASUREMENT

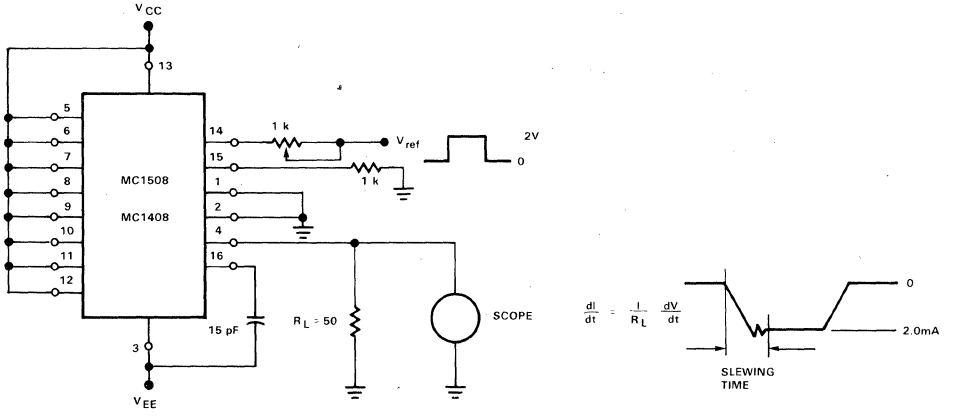


Figure 6

NE5007/5008, SE5008-F,N

DESCRIPTION

The 5007/5008 series of 8-bit monolithic multiplying Digital-to-Analog Converters provide very high speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85ns settling times with very low glitch and at low power consumption. Monotonic multiplying performance is attained over a wide 40 to 1 reference current range. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

Dual complementary outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. True high voltage compliance outputs allow direct output voltage conversion and eliminate output op amps in many applications.

All 5007/5008 series models guarantee full 8-bit monotonicity and linearities as tight as 0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5V to ±18V power supply range, with 33mW power consumption attainable at ±5V supplies.

The compact size and low power consumption make the 5007/5008 attractive for portable and military/aerospace applications.

FEATURES

- **Fast settling output current—85ns**
- **Full scale current prematched to ±1 LSB**
- **Direct interface to TTL, CMOS, ECL, HTL, PMOS**
- **Relative accuracy to 0.1% maximum over temperature range**
- **High output compliance—-10V to +18V**
- **True and complemented outputs**
- **Wide range multiplying capability**
- **Low FS current drift—±10ppm/°C**
- **Wide power supply range—±4.5V to ±18V**
- **Low power consumption—33mW at ±5V**
- **SE5008 military qualifications pending**

APPLICATIONS

- **8-bit, 1μs A-to-D converters**
- **Servo-motor and pen drivers**
- **Waveform generators**
- **Audio encoders and attenuators**
- **Analog meter drivers**
- **Programmable power supplies**
- **CRT display drivers**
- **High speed modems**
- **Other applications where low cost, high speed and complete input/output versatility are required**

ORDERING INFORMATION

RELATIVE ACCURACY	0 to 70°C	-55 to 125°C
0.39% FS	NE5007N NE5007F	-
0.19% FS	NE5008N NE5008F	SE5008F

DEFINITION OF TERMS

Accuracy—The maximum deviation of the Dac output relative to an ideal straight line drawn from zero to full scale; 1 LSB for any bit combination

Differential linearity—The incremental error from an ideal 1 LSB analog output change when the digital input is changed 1 LSB; guaranteed monotonicity requires the differential linearity error be less than 1 LSB and with a tempco of essentially zero

Full scale tempco—The change in Dac full scale current with change in temperature expressed in ppm/°C

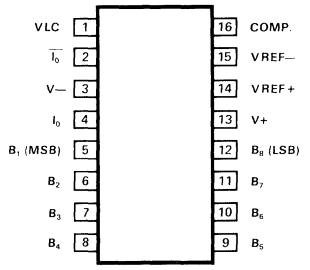
Monotonicity—For a 1 LSB increase of input code, the output either increases or remains the same

Output voltage compliance—The range of allowable voltage levels the output pins can assume without a major effect on circuit performance

Power supply sensitivity—The change in Dac output current with changes in power supply voltage

PIN CONFIGURATION

F,N PACKAGE*



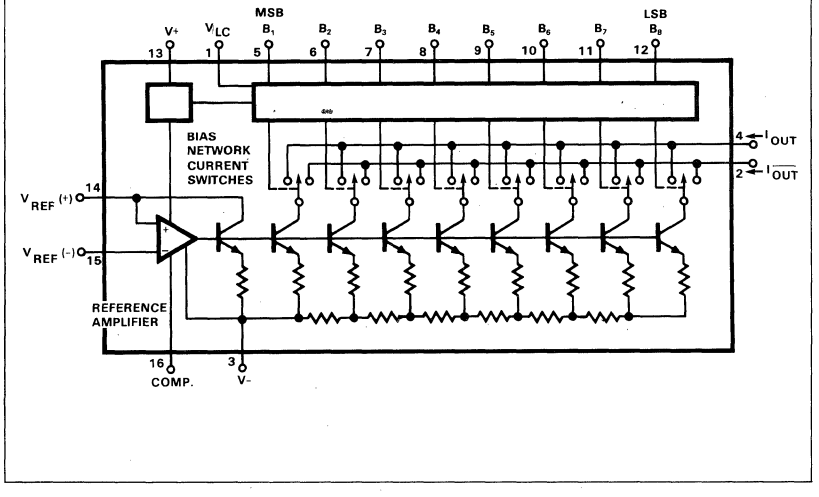
*N = Plastic DIP
F = Cerdip

CROSS REFERENCE

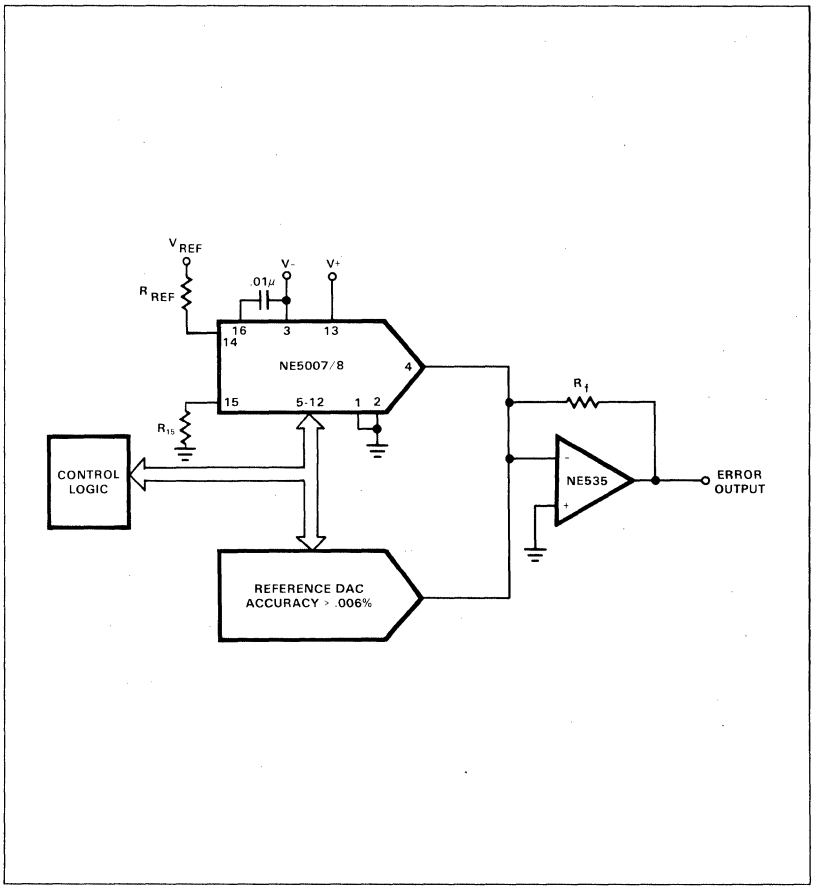
The 5007/5008 series are pin and functionally compatible with the monoDAC-08 series of devices.

PMI	SIGNETICS
monoDAC-08A	SE5009
monoDAC-08	SE5008
monoDAC-08E	NE5008
monoDAC-08C	NE5007

BLOCK DIAGRAM



TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

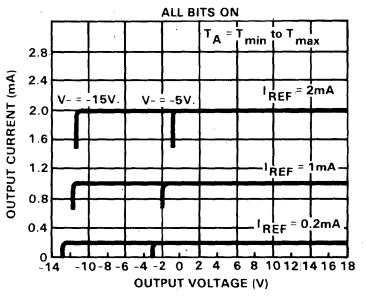
	PARAMETER	RATING	UNIT
T_A	Operating temperature range		°C
	SE5008	-55 to +125	
	NE5007/8	0 to +70	
t_{stg}	Storage temperature	-65 to +150	°C
P_D	Power dissipation	500	mW
	Lead soldering temperature (60sec)	300	°C
	V+ to V- supply	36	V
	Logic inputs	V- to V- plus 36V	
V_{LC}	Logic threshold control	V- to V+	
	Analog current outputs	See output current or output voltage performance curve	
V_{14}, V_{15}	Reference inputs	V- to V+	
V_{14} to V_{15}	Reference input differential voltage	±18	V
I_{14}	Reference input current	5.0	mA

AC ELECTRICAL CHARACTERISTICS V_S = ±15V, I_{REF} = 2.0mA, Output characteristics refer to both IOUT and $\overline{IOUT}$ unless otherwise noted. NE5008: T_A = 0°C to 70°C. SE5008: T_A = -55°C to 125°C.

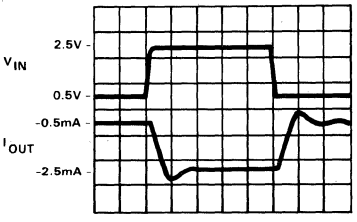
PARAMETER		TEST CONDITIONS	NE5007			NE5008			SE5008[1]			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	8	8	8	Bits
	Relative accuracy	Over temperature range			±0.39			±0.19			±0.19	%FS
t_s	Settling time	To ±½ LSB, all bits switched on or off, T_A=25°C		100			100			100		ns
t_{PLH} t_{PHL}	Propagation delay Low-to-high High-to-low	T_A=25°C, each bit. All bits switched		35			35			35	60	ns
TCI_{FS}	Full scale tempco			±10			±10			±10		ppm/°C
V_{OC}	Output voltage compliance	Full scale current change <½ LSB	-10		+18	-10		+18	-10		+18	V
I_{FS4}	Full scale current	V_{REF}=10.000V, R_{14}, R_{15}=5.000kΩ, T_A=25°C	1.94	1.99	2.04	1.94	1.99	2.04	1.94	1.99	2.04	mA
I_{FSS}	Full scale symmetry	I_{FS4}-I_{FS2}		±2.0	±16		±1.0	±8.0		±1.0	±8.0	μA
I_{ZS}	Zero scale current			0.2	4.0		0.2	2.0		0.2	2.0	μA
I_{FSR}	Output current	V-=-5.0V V-=-7.0V to -18V	0 0	2.0 2.0	2.1 4.2	0 0	2.0 2.0	2.1 4.2	0 0	2.0 2.0	2.1 4.2	mA
V_{IL} V_{IH}	Logic input levels Low High	V_{LC}=0V	 2.0		0.8	 2.0		0.8	 2.0		0.8	V
I_{IL} I_{IH}	Logic input current Low High	V_{LC}=0V V_{IN}=-10V to +0.8V V_{IN}=2.0V to 18V		-2.0 0.002	-10 10		-2.0 0.002	-10 10		-2.0 0.002	-10 10	μA
V_{IS}	Logic input swing	V-=-15V	-10		+18	-10		+18	-10		+18	V
V_{THR}	Logic threshold range	V_S=±15V	-10		+13.5	-10		+13.5	-10		+13.5	V
I_{15}	Reference bias current			-1.0	-3.0		-1.0	-3.0		-1.0	-3.0	μA
dI/dt	Reference input slew rate	Figures 1, 3		8.0			8.0			8.0		mA/μs
$PSSI_{FS+}$ $PSSI_{FS-}$	Power supply sensitivity Positive Negative	I_{REF}=1mA V+=4.5 to 5.5V, V-=-15V; V+=13.5 to 16.5V, V-=-15V V-=-4.5 to -5.5V, V+=+15V; V-=-13.5 to -16.5, V+=+15V		0.0003 0.002	0.01 0.01		0.0003 0.002	0.01 0.01		0.0003 0.002	0.01 0.01	%FS/%VS
I+ I-	Power supply current Positive Negative	V_S=±5V, IREF=1.0mA		2.3 -4.3	3.8 -5.8		2.3 -4.3	3.8 -5.8		2.3 -4.3	3.8 -5.8	mA
I+ I-	Positive Negative	V_S=+5V, -15V, I_{REF}=2.0mA		2.4 -6.4	3.8 -7.8		2.4 -6.4	3.8 -7.8		2.4 -6.4	3.8 -7.8	
I+ I-	Positive Negative	V_S=±15V, I_{REF}=2.0mA		2.5 -6.5	3.8 -7.8		2.5 -6.5	3.8 -7.8		2.5 -6.5	3.8 -7.8	
P_D	Power dissipation	±5V, I_{REF}=1.0mA +5V, -15V, I_{REF}=2.0mA ±15V, I_{REF}=2.0mA		33 108 135	48 136 174		33 108 135	48 136 174		33 108 135	48 136 174	mW

TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)

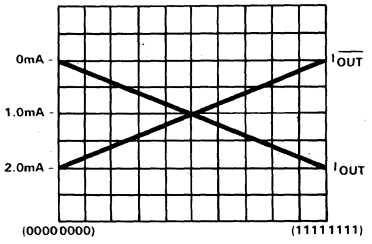


FAST PULSED REFERENCE OPERATION

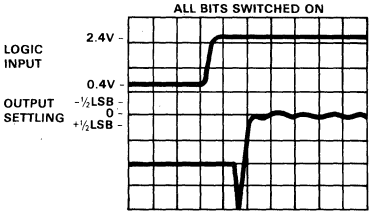


200ns/division
See Figure 1
R_{EQ} = 200Ω, R_L = 100Ω, CC = O

TRUE AND COMPLEMENTARY OUTPUT OPERATION



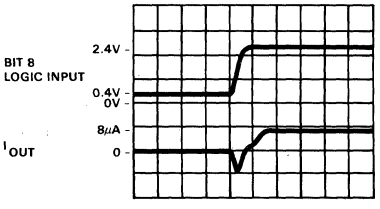
FULL SCALE SETTLING TIME



50ns/division

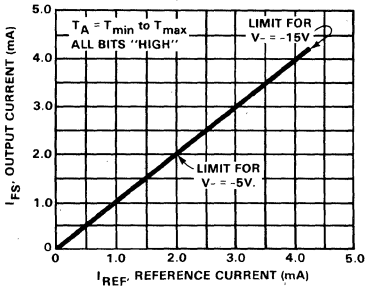
See Figure 8 of application memo for settling time fixture
IFS = 2mA, R_L = 1KΩ, ½ LSB = 4μA

LSB SWITCHING

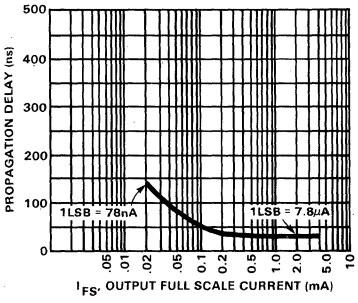


50ns/division

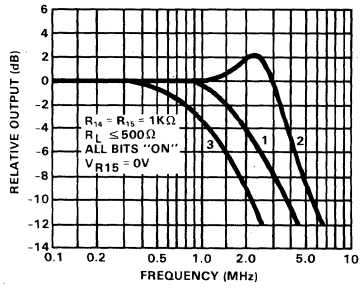
FULL SCALE CURRENT vs REFERENCE CURRENT



LSB PROPAGATION DELAY vs IFS



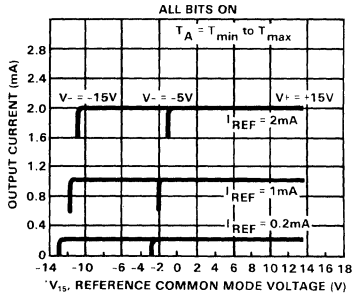
REFERENCE INPUT FREQUENCY RESPONSE



Curve 1: CC = 15pF, V_{IN} = 2.0V p-p centered at +1.0V.
Curve 2: CC = 15pF, V_{IN} = 50mV p-p centered at +200mV.
Curve 3: CC = 0pF, V_{IN} = 100mV p-p centered at 0V and applied thru 50Ω connected to pin 14. +2.0V applied to R_{14}.

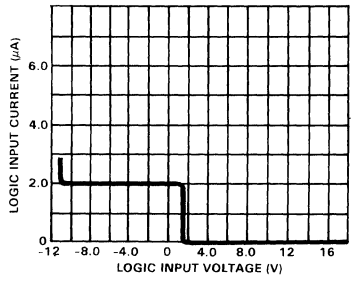
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

REFERENCE AMP COMMON MODE RANGE

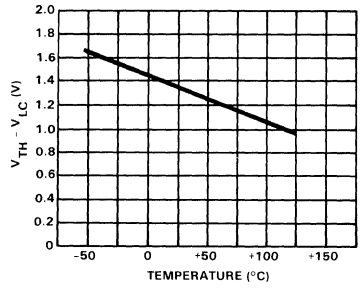


Positive common mode range is always (V+) - 1.5V

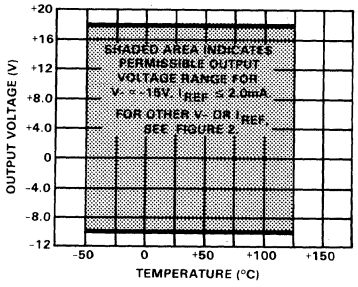
LOGIC INPUT CURRENT vs INPUT VOLTAGE



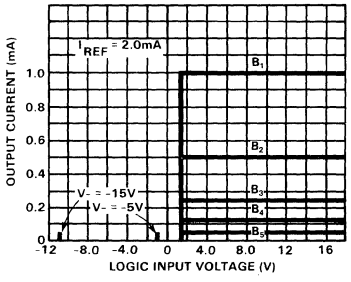
$V_{TH} - V_{LC}$ vs TEMPERATURE



OUTPUT VOLTAGE COMPLIANCE vs TEMPERATURE



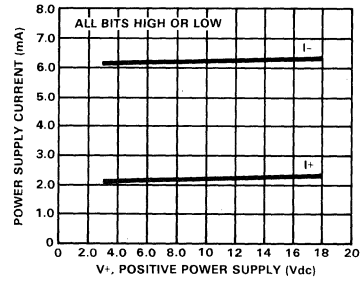
BIT TRANSFER CHARACTERISTICS



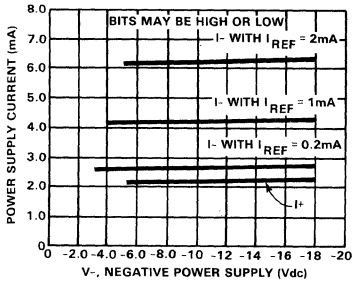
NOTE

B_1 through B_8 have identical transfer characteristics. Bits are fully switched, with less than ½ LSB error, at less than ±100mV from actual threshold. These switching points are guaranteed to lie between 0.8 and 2.0 volts over the operating temperature range (VLC = 0.0V).

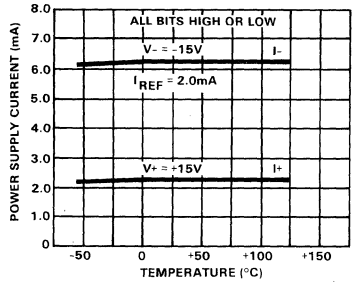
POWER SUPPLY CURRENT vs V+



POWER SUPPLY CURRENT vs V-

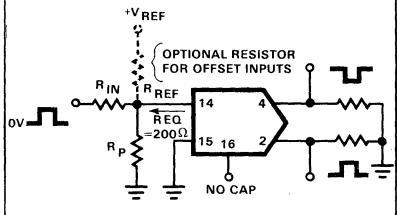


POWER SUPPLY CURRENT vs TEMPERATURE



TYPICAL APPLICATION

PULSED REFERENCE OPERATION



TYPICAL VALUES

R_{IN} = 5K

$+V_{IN}$ = 10V

NE5009-F,N • SE5009-F

DESCRIPTION

The 5009 monolithic 8-bit digital-to-analog converter is an electrical selection of the 5007/8 series of 8-bit D/A converters. Relative accuracy is specified to ±1/4LSB maximum over the operating temperature range. Differential nonlinearity and settling times are also specified to maximum limits.

The device is specifically designed for precision applications in process control and military systems. The SE5009 is specified as equal or superior to the PMI DAC-08A in all respects. Additional relevant testing and application material is shown in the data sheet and application notes for the NE5007/8.

FEATURES

- **Fast settling output current—60ns typical, 135ns maximum**
- **Relative accuracy— ±0.1% maximum**
- **Differential nonlinearity—±0.19% maximum**
- **Low full-scale current drift, ±10 ppm/°C typical**
- **SE5009 military qualifications pending**

APPLICATIONS

- **Fast 8-bit A/D converter**
- **Variable gain amplifiers**
- **Waveform generators**
- **3 digit BCD D/A converter (0.1%)**
- **Programmable power supplies**

DEFINITION OF TERMS

Relative Accuracy—The maximum deviation of the DAC output relative to an ideal straight line drawn from zero to full scale; 1 LSB for any bit combination.

Differential Nonlinearity—The incremental error from an ideal 1 LSB analog output change when the digital input is changed 1 LSB; guaranteed monotonicity requires the differential linearity error be less than 1 LSB and with a tempco of essentially zero.

Full Scale Tempco—The change in DAC full scale current with change in temperature expressed in ppm/°C.

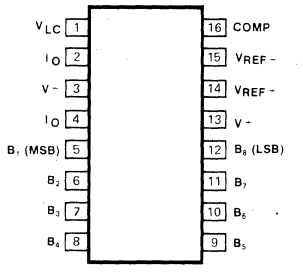
Monotonicity—For a 1 LSB increase of input code, the output either increases or remains the same.

Output Voltage Compliance—The range of allowable voltage levels the output pins can assume without a major effect on circuit performance.

Power Supply Sensitivity—The change in DAC output current with changes in power supply voltage.

PIN CONFIGURATION

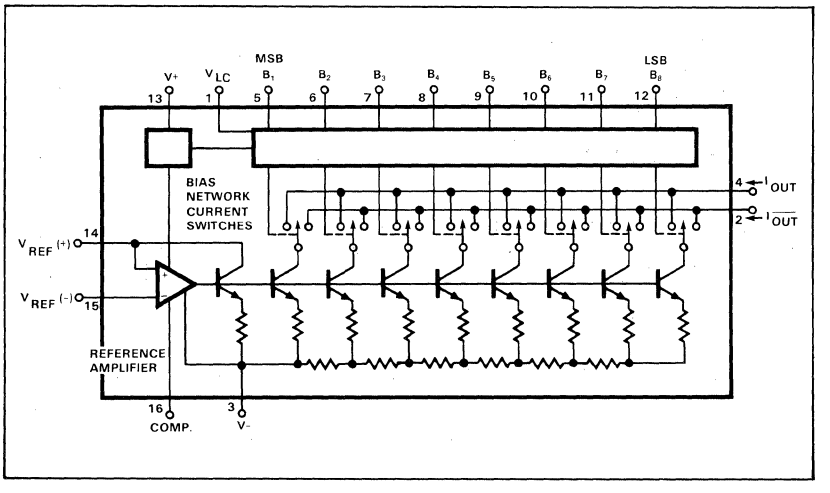
F,N PACKAGE*



NOTE

*SE5009 is in F package only.

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise specified.

PARAMETER	RATING	UNIT
Total supply voltage (V+ - V-)	36	V
Logic input voltage	V- + 36	V
V_{LC} Voltage at pin 1	V- to V+	V
Reference input voltage	V- to V+	V
Reference input differential voltage	±18	V
Reference input current	5.0	mA
Operating temperature range		
SE5009	-55 to +125	°C
NE5009	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead soldering temperature (10sec)	300	°C
Power dissipation*	500	mW

NOTE

*Derate F package at 10mW/°C above 100°C.

DC ELECTRICAL CHARACTERISTICS

These specs apply for $V_S = \pm 15V$, $I_{REF} = 2mA$, T_A for NE5009 0° to 70°C, T_A for SE5009 -55° to +125°C. Output char. for both I_{OUT} and $\overline{I_{OUT}}$.

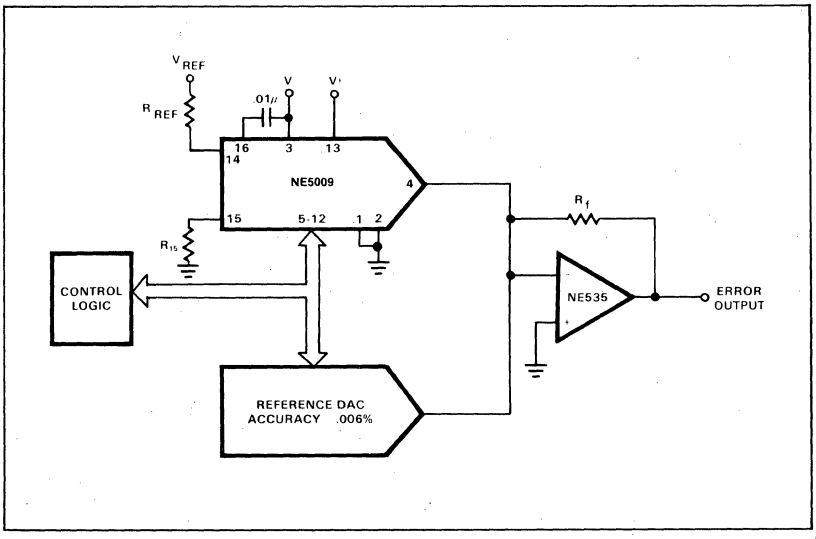
PARAMETER		TEST CONDITIONS	NE5009			SE5009			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	bits
	Monotonicity		8	8	8	8	8	8	bits
	Relative accuracy	Over temperature range			±0.1			±0.1	% FS
	Differential nonlinearity			±0.1	±0.19		±0.1	±0.19	% FS
TCI_{FS}	Full scale tempco			±10	±50		±10	±50	ppm/°C
V_{OC}	Output voltage compliance	Full scale current change < 1/2LSB	-10		+18	-10		+18	V
I_{FS4}	Full scale current	$V_{REF} = 10.000V$, R_{14}·$R_{15} = 5.000k$ $T_A = 25°C$	1.984	1.992	2.000	1.984	1.992	2.000	mA
I_{FSS}	Full scale symmetry	$I_{FS4} - I_{FS2}$		±0.5	±4.0		±0.5	±4.0	μA
I_{ZS}	Zero scale current			0.1	1.0		0.1	1.0	μA
I_{FSR}	Output current range	V- = -5.0V	0	2.0	2.1	0	2.0	2.1	mA
		V- = -7.0V to -18V	0	2.0	4.2	0	2.0	4.2	mA
	Logic input levels								
V_{IL}	Logic "0"	$V_{LC} = 0V$			0.8			0.8	V
V_{IH}	Logic "1"	$V_{LC} = 0V$	2.0			2.0			V
	Logic input current	$V_{LC} = 0V$							
I_{IL}	Logic "0"	$V_{IN} = -10V$ to +0.8V		-2.0	-10		-2.0	-10	μA
I_{IH}	Logic "1"	$V_{IN} = 2.0V$ to 18V		0.002	10		0.002	10	μA
V_{IS}	Logic input swing	V- = -15V	-10		+18	-10		+18	V
V_{THR}	Logic threshold range	$V_S = \pm 15V$	-10		+13.5	-10		+13.5	V
I_{15}	Reference bias current			-1.0	-3.0		-1.0	-3.0	μA
di/dt	Reference input slew rate		4.0	8.0		4.0	8.0		mA/μs
	Power supply sensitivity								
PSSIFS+		$I_{REF} = 1mA$, V- = -15V:							
		V+ = 4.5 to 5.5V		0.0003	0.01		0.0003	0.01	%FS/%VS
		V+ = 13.5 to 16.5V		0.0003	0.01		0.0003	0.01	%FS/%VS
PSSIFS-		$I_{REF} = 1mA$, V+ = +15V:							
		V- = -4.5 to -5.5V		0.0003	0.01		0.0003	0.01	%FS/%VS
		V- = -13.5 to -16.5V		0.0003	0.01		0.0003	0.01	%FS/%VS
	Power supply current	$V_S = \pm 15V$, $I_{REF} = 1.0mA$							
I+				2.3	3.8		2.3	3.8	mA
I-				-4.3	-5.8		-4.3	-5.8	mA
	Power supply current	$V_S = +5V, -15V$; $I_{REF} = 2.0mA$							
I+				2.4	3.8		2.4	3.8	mA
I-				-6.4	-7.8		-6.4	-7.8	mA
	Power supply current	$V_S = \pm 15V$, $I_{REF} = 2.0mA$							
I+				2.5	3.8		2.5	3.8	mA
I-				-6.5	-7.8		-6.5	-7.8	mA
P_D	Power dissipation	±5V, $I_{REF} = 1.0mA$		33	48		33	48	mW
		+5V, -15V, $I_{REF} = 2.0mA$		108	136		108	136	mW
		±15V, $I_{REF} = 2.0mA$		135	174		135	174	mW

AC ELECTRICAL CHARACTERISTICS

These specs apply for $V_S = \pm 15V$, $I_{REF} = 2mA$, Output char. for both I_{OUT} and $\overline{I_{OUT}}$.

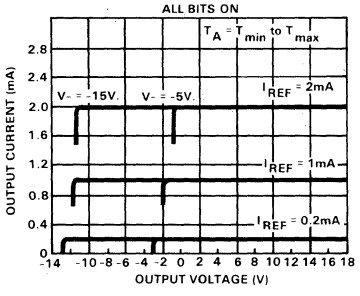
PARAMETER		TEST CONDITIONS	SE/NE5009			UNIT
			Min	Typ	Max	
t_s	Settling time	To $\pm 1/2$LSB all bits switched ON or OFF, $T_A = 25°C$		60	135	ns
	Major carry transition	To 90% complete, $T_A = 25°C$		20		ns
t_{PLH}, t_{PHL}	Propagation delay Each bit	$T_A = 25°C$		35	60	ns
	All bits switched			35	60	ns

TEST CIRCUIT

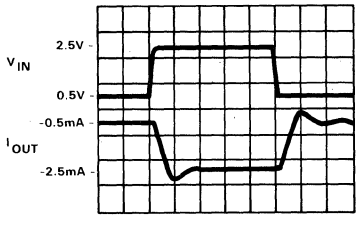


TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)

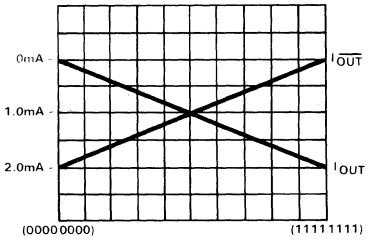


FAST PULSED REFERENCE OPERATION



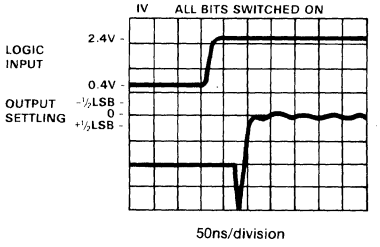
200ns/division
See Figure 1
$R_{EQ} = 200\Omega$, $R_L = 100\Omega$, CC = O

TRUE AND COMPLEMENTARY OUTPUT OPERATION



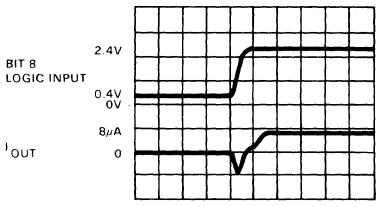
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

FULL SCALE SETTLING TIME

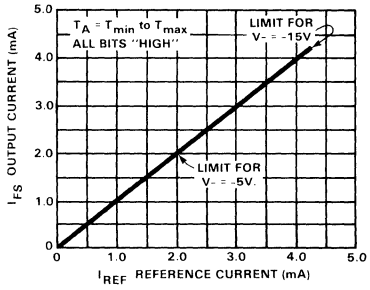


See Figure 13 for settling time fixture

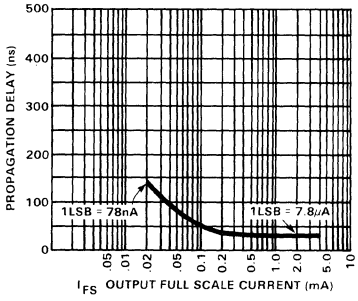
LSB SWITCHING



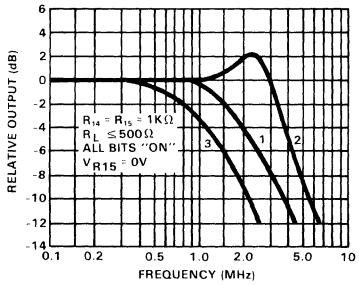
FULL SCALE CURRENT vs REFERENCE CURRENT



LSB PROPAGATION DELAY vs IFS

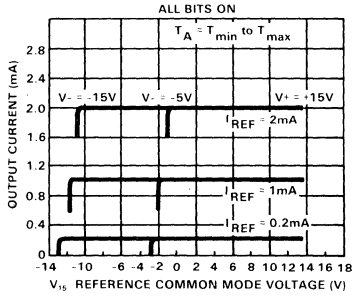


REFERENCE INPUT FREQUENCY RESPONSE



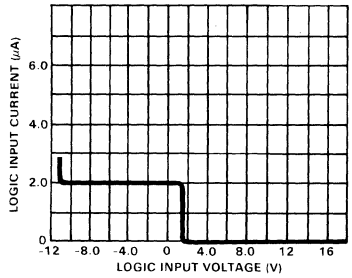
Curve 1:CC = 15pF, V_{IN} = 2.0V p-p centered at +1.0V.
Curve 2:CC = 15pF, V_{IN} = 50mV p-p centered at +200mV.
Curve 3:CC = 0pF, V_{IN} = 100mV p-p centered at 0V and applied thru 50Ω connected to pin 14. +2.0V applied to R_{14}.

REFERENCE AMP COMMON MODE RANGE

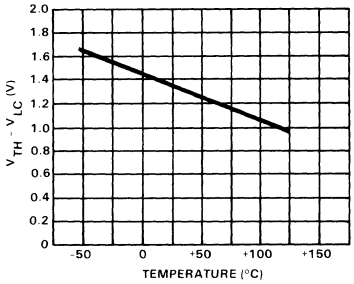


Positive common mode range is always (V+) - 1.5V

LOGIC INPUT CURRENT vs INPUT VOLTAGE

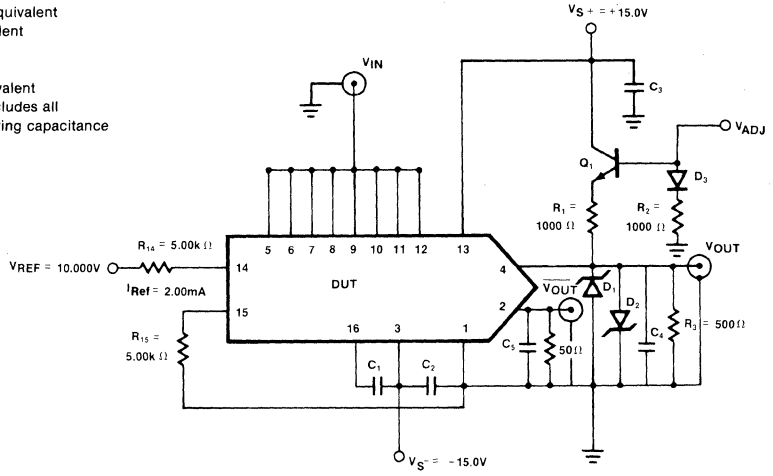


V_{TH}-V_{LC} vs TEMPERATURE

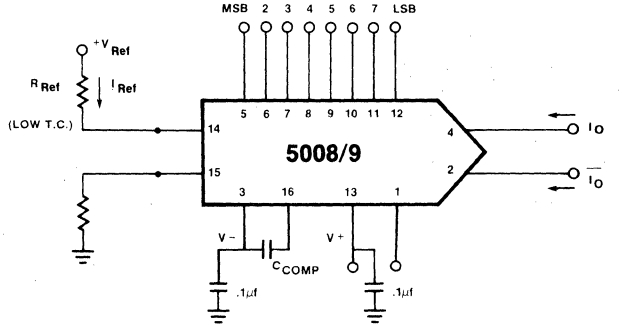


SETTLING TIME AND PROPAGATION DELAY

D_1, D_2 = IN6263 or equivalent
D_3 = IN914 or equivalent
C_1 = 0.01μf
C_2, C_3 = 0.1μf
Q_1 = 2N3904 or equivalent
C_4, C_5 = 15pf and includes all probe and fixturing capacitance

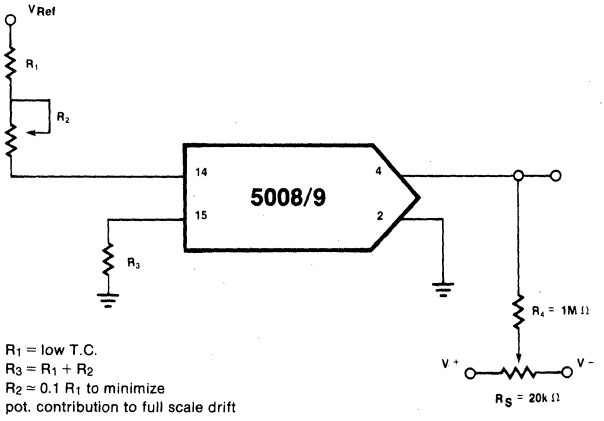


BASIC 5008/5009 CONFIGURATION



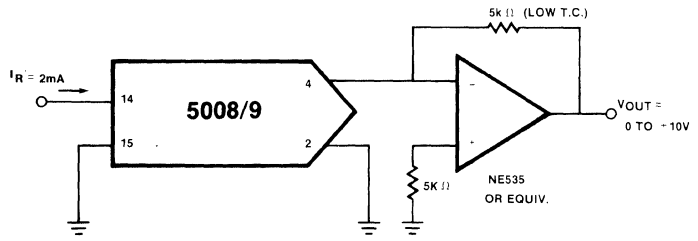
$$I_{FS} \approx \frac{+V_{Ref}}{R_{Ref}} \times \frac{255}{256}\ ;\ I_O + \overline{I}_O = I_{FS} \text{ for all logic states}$$

RECOMMENDED FULL SCALE AND ZERO SCALE ADJ.



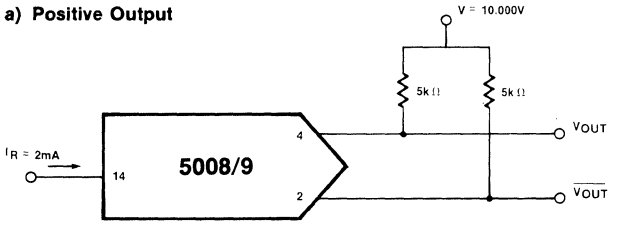
R_1 = low T.C.
$R_3 = R_1 + R_2$
$R_2 \approx 0.1\ R_1$ to minimize pot. contribution to full scale drift

UNIPOLAR VOLTAGE OUTPUT FOR LOW IMPEDANCE OUTPUT

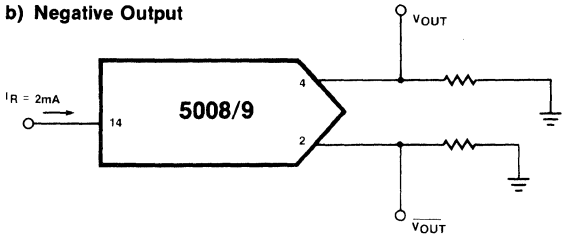


UNIPOLAR VOLT OUTPUT FOR HIGH IMPEDANCE OUTPUT

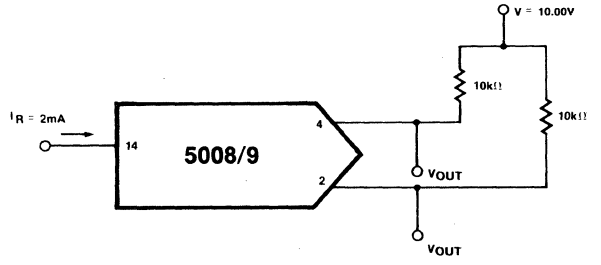
a) Positive Output



b) Negative Output



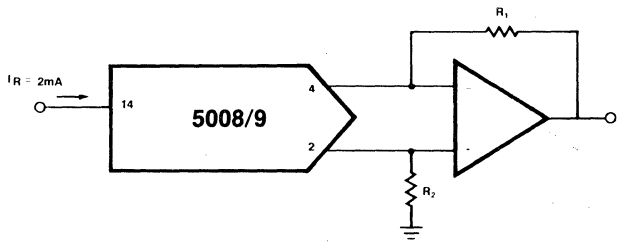
BASIC BIPOLAR OUTPUT OPERATION (OFFSET BINARY)



CODE CHART

	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	V_{OUT}	$\overline{V_{OUT}}$
POS full scale	1	1	1	1	1	1	1	1	-9.920V	+10.000
POS f.s. - 1LSB	1	1	1	1	1	1	1	0	-9.840V	+9.920
+ Zero scale + 1LSB	1	0	0	0	0	0	0	1	-0.080V	+0.160
Zero scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero scale - 1LSB	0	1	1	1	1	1	1	1	0.080	0.000
Neg full scale - 1LSB	0	0	0	0	0	0	0	1	+9.920	-9.840
Neg full scale	0	0	0	0	0	0	0	0	+10.000	-9.920

SYMMETRICAL OFFSET BINARY (BIPOLAR)



V_{OUT} = 0 to ±V*

±V *Range:
±5V for $R_1 = R_2 = 2.5k$
±10V for $R_1 = R_2 = 5.0k$

3 DIGIT BCD CONVERTER

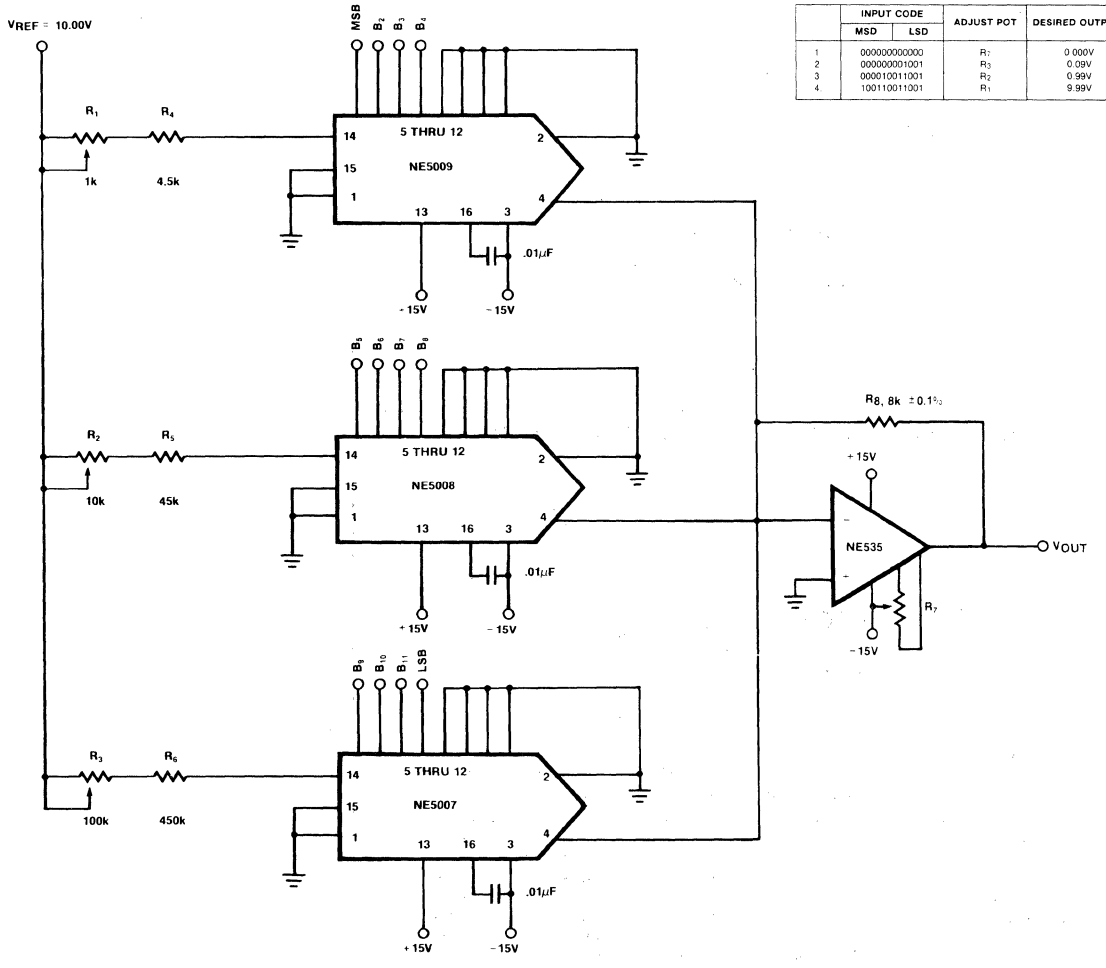
A 3 digit BCD converter, using inexpensive 8-bit binary DACs, can achieve ±0.1% accuracy. The circuit shown in Figure 20 utilizes three DACs, one for each decade, to provide 0 to 999 output steps. DAC 1 contains the first four significant digits controlling the hundreds digit; DAC 2 controls the tens digit and DAC 3 steps 0 to 9. The feedback resistor (R_7) sets the full scale at 9.99V.

The input coding is the popular 8-4-2-1 coding; i.e. the weighting ratios are 8, 4, 2 and 1. The full scale (999) BCD code is input code 100110011001.

Full scale adjustment procedure.

In the sequence below, switch on the following code combinations and adjust the indicated potentiometer for the proper output.

3 DIGIT BCD CONVERTER WITH ±0.1% ACCURACY



	INPUT CODE MSD	INPUT CODE LSD	ADJUST POT	DESIRED OUTPUT
1	000000000000		R_7	0.000V
2	000000001001		R_3	0.09V
3	000010011001		R_2	0.99V
4	100110011001		R_1	9.99V

PRELIMINARY SPECIFICATION

NE5018-F,N

DESCRIPTION

The NE5018 is a complete 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal) and a high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

FEATURES

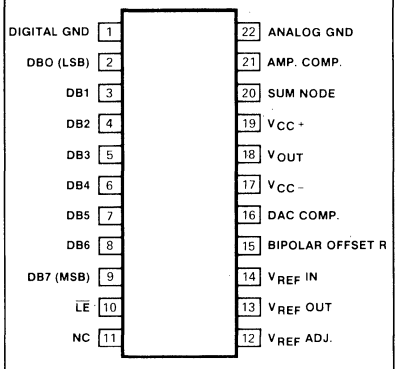
- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Output buffer amplifier**
- **Accurate to ± 1/2 LSB**
- **Monotonic to 8 bits**
- **Amplifier and reference both short-circuit protected**
- **Compatible with 2650, 8080 and many other μP's.**

APPLICATIONS

- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog-digital multiplication**

PIN CONFIGURATION

F,N PACKAGE



SE5018 available in F package only.

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	-18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF}IN$	Voltage at V_{REF} input	12	V
$V_{REF}ADJ$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
I_{REF}	Reference input current	5	mA
P_D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T_A	Operating temperature range		
	SE5018	-55 to +125	°C
	NE5018	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTE

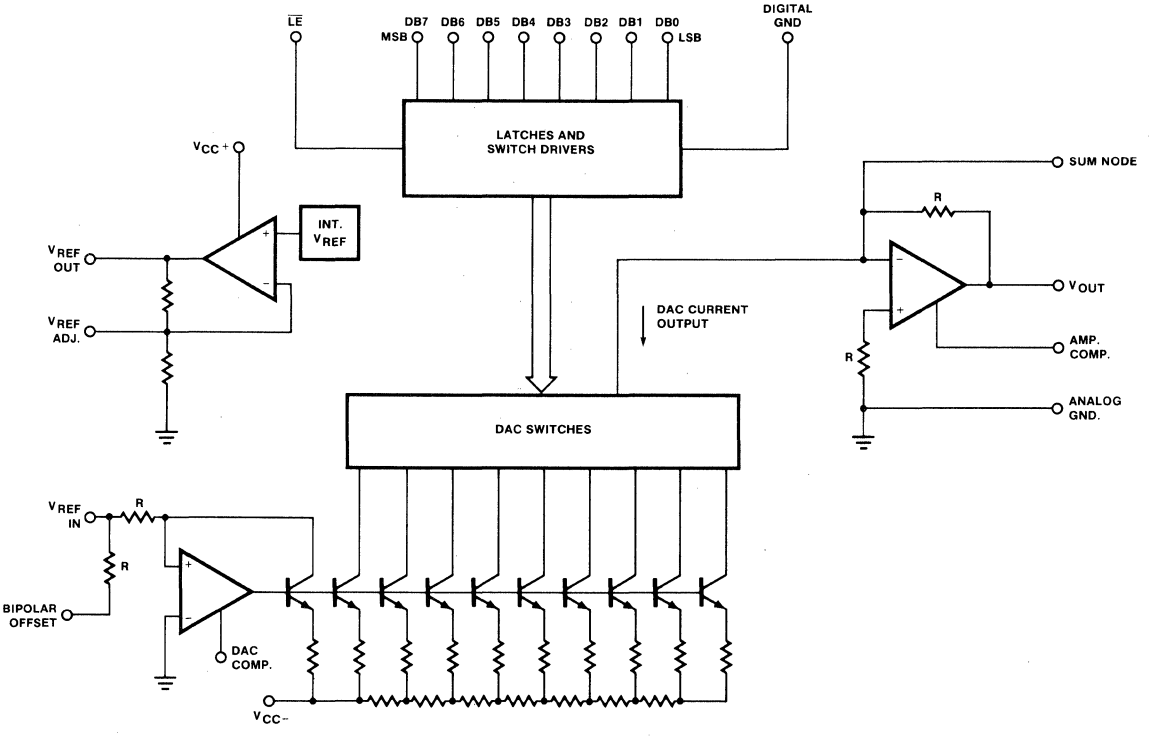
For N package, derate at 120°C/W above 35°C
For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = 15V$, $V_{CC}- = -15V$, SE5018. $-55°C \leq T_A \leq 125°C$, NE5018. $0°C \leq T_A \leq 70°C$ unless otherwise specified.

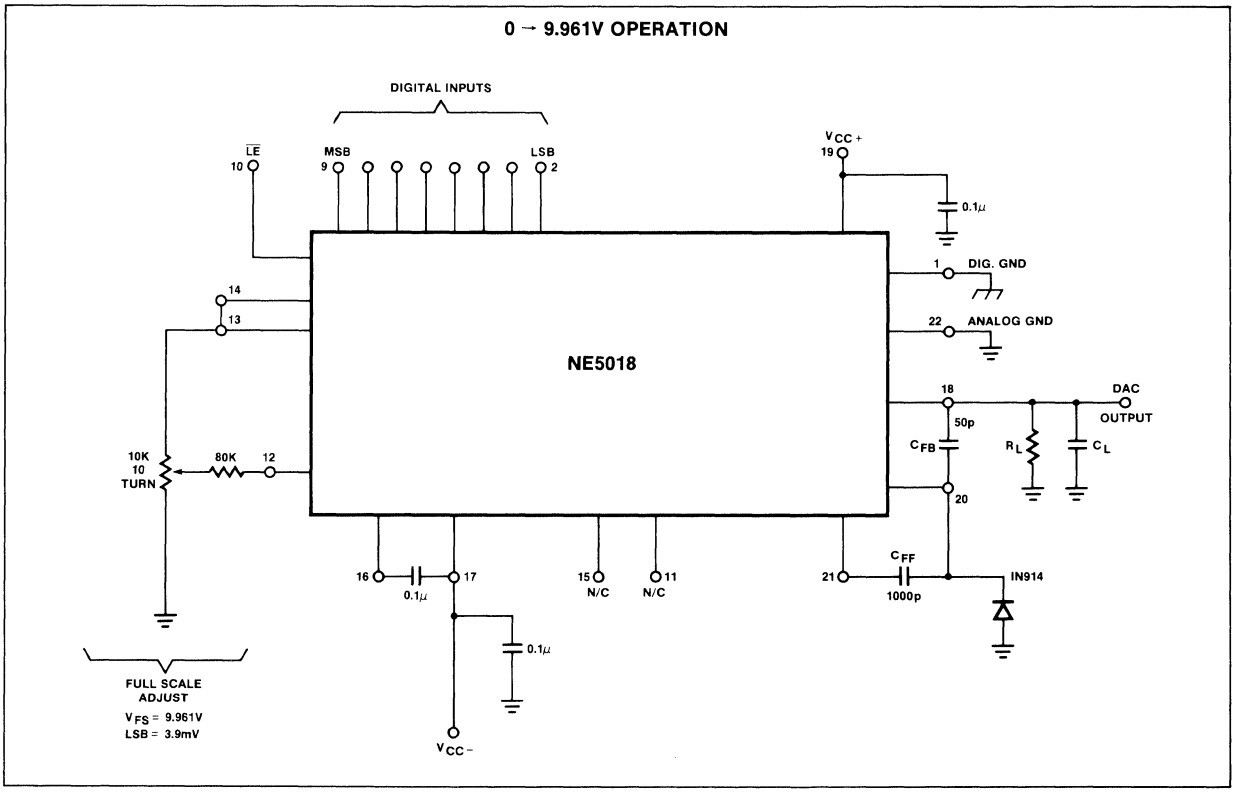
PARAMETER		TEST CONDITIONS	SE5018			NE5018			UNITS
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}+$	Positive supply voltage			15			15		V
$V_{CC}-$	Negative supply voltage			-15			-15		V
	Resolution			8			8		bits
	Relative accuracy				±0.19			±0.19	%
T_S	Settling time	To ± 1/2LSB, 10V step		2			2		μs
PSRR	Power supply Rejection ratio	$V_{CC}+$ +12 to +18V $V_{CC}-$ -12 to -18V		±1			±1		mV/V
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		8			8		mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		-10			-10		mA
$I_{IN}(0)$	Logic "0" input current	$V_{IN} = 0V$		5			5		μA
$V_{IN}(0)$	Logic "0" input voltage				0.8			0.8	V
$V_{IN}(1)$	Logic "1" input voltage		2.0			2.0			V
T_{PWLE}	Latch enable pulse width			400			400		ns

BLOCK DIAGRAM



All R valves equal 5KΩ and are thermally matched.

EQUIVALENT SCHEMATIC



SECTION 12
AUDIO CIRCUITS

LM381/381A-N

DESCRIPTION

The LM381/LM381A is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with individual internal power supply decoupler-regulator, providing 120dB supply rejection and 60dB channel separation. Other outstanding features include high gain (112dB), large output voltage swing (V_{CC} -2V p-p), and wide power bandwidth (75kHz, 20V p-p.). The LM381/LM381A operates from a single supply across the wide range of 9 to 40V.

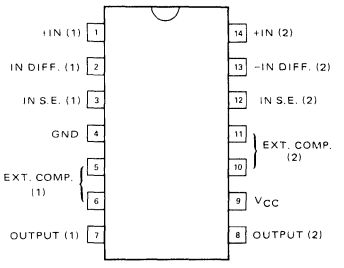
Either differential input or single ended input configurations may be selected. The amplifier is internally compensated with the provision for additional external compensation for narrow band applications.

FEATURES

- **Low noise—.5μV total input noise**
- **High gain—112dB open loop**
- **Single supply operation**
- **Wide supply range 9—40V**
- **Power supply rejection 120dB**
- **Large output voltage swing(V_{CC} -2V p-p)**
- **Wide bandwidth 15MHz unity gain**
- **Power bandwidth 75kHz, 20V p-p**
- **Internally compensated**
- **Short circuit protected**

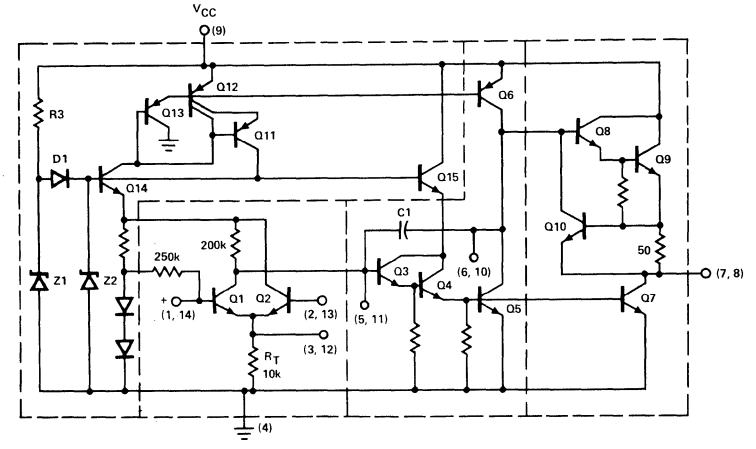
PIN CONFIGURATION

N PACKAGE



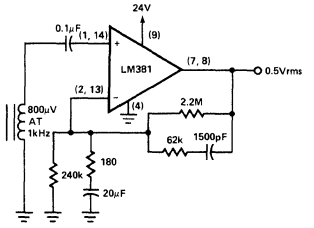
ORDER PART NO.
LM381N LM381AN

EQUIVALENT CIRCUIT



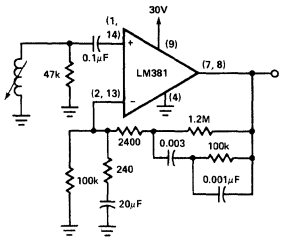
TYPICAL APPLICATIONS

TYPICAL TAPE PLAYBACK AMPLIFIER



NOTE
All resistors standard and are measured in ohms.

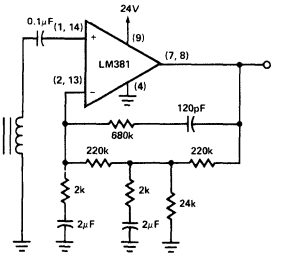
TYPICAL MAGNETIC PHONO PREAMP



NOTE
All resistors standard and are measured in ohms.

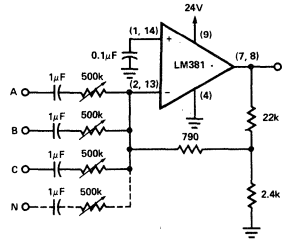
TYPICAL APPLICATIONS

TWO-POLE FAST TURN-ON NAB TAPE PREAMP



NOTE
All resistors standard and are measured in ohms.

AUDIO MIXER



NOTE
All resistors standard and are measured in ohms.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+40	V
Power dissipation	600	mW
Operating temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

12

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 14V unless otherwise specified.

PARAMETER	TEST CONDITIONS	LM381/381A			UNIT
		Min	Typ	Max	
Voltage gain	Open loop (differential input) Open loop (single ended)		160,000 320,000		V/V V/V
Supply current	V_{CC} 9 to 40V, RL = ∞		10		mA
Input resistance	Positive input Negative input		100 200		kΩ kΩ
Input current Output resistance	Negative input Open loop		0.5 150		μA Ω
Output current	Source Sink		8 2		mA mA
Output voltage swing	Peak-to-peak		V_{CC} -2		V

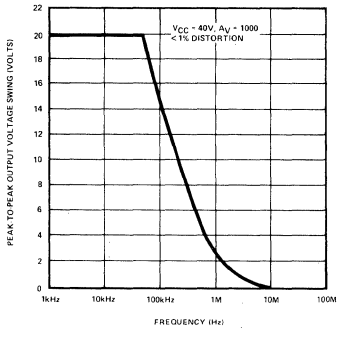
AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 14V unless otherwise specified.

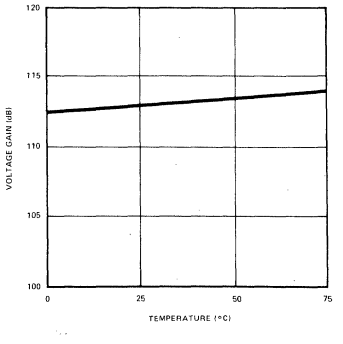
PARAMETER	TEST CONDITIONS	LM381/381A			UNIT
		Min	Typ	Max	
Small signal bandwidth Power bandwidth Maximum input voltage	 20V p-p (V_{CC} = 24V) Linear operation		15 75	 300	MHz kHz mVrms
Supply rejection ratio Channel separation	f = 1kHz f = 1kHz		120 60		dB dB
Total harmonic distortion Total equivalent input noise LM381A LM381	75dB gain, f = 1kHz RS = 600Ω, 100-10,000Hz (single ended input)		0.1 0.5 0.5	 0.7 1.0	% μVrms μVrms
Noise figure	50kΩ,100 - 10,000Hz (Single Ended Input) 10kΩ,100 - 10,000Hz (Single Ended Input) 5kΩ,100 - 10,000Hz (Single Ended Input)		1.0 1.3 1.6		dB dB dB

TYPICAL PERFORMANCE CHARACTERISTICS

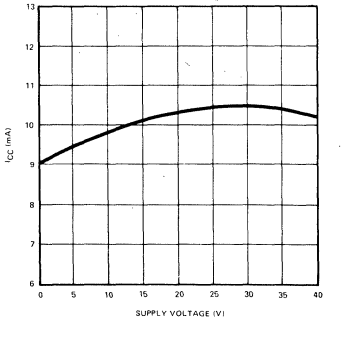
LARGE SIGNAL FREQUENCY RESPONSE



GAIN vs TEMPERATURE

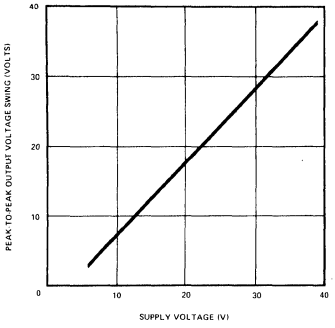


V_{CC} vs I_{CC}

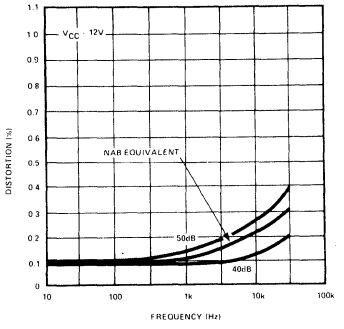


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

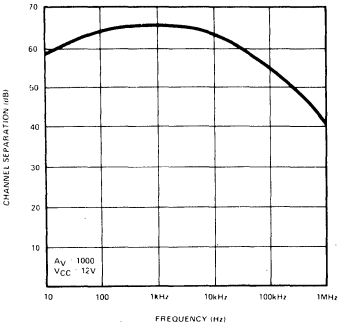
P-P OUTPUT VOLTAGE SWING vs V_{CC}



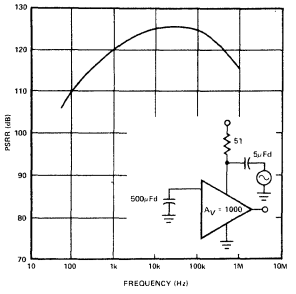
% DISTORTION



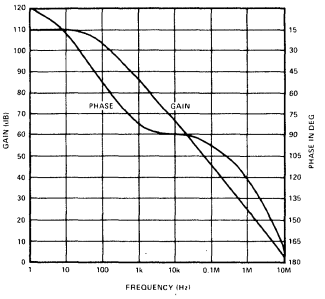
CHANNEL SEPARATION



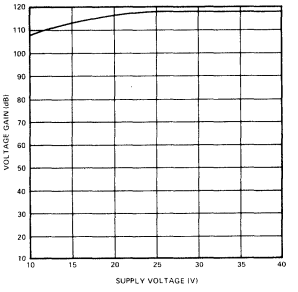
PSRR vs FREQUENCY



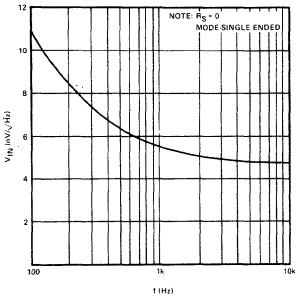
GAIN AND PHASE RESPONSE



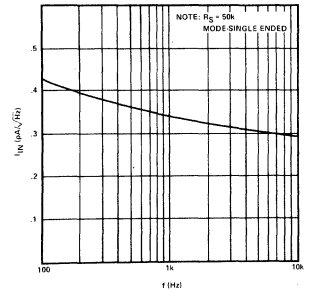
VOLTAGE GAIN vs SUPPLY VOLTAGE



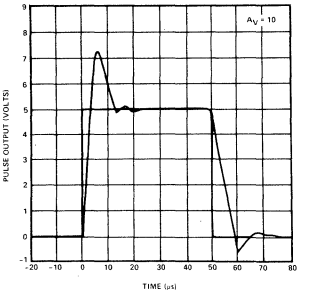
NOISE VOLTAGE vs FREQUENCY



NOISE CURRENT vs FREQUENCY



PULSE RESPONSE



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LM382-N

DESCRIPTION

The LM382 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with individual internal power supply decoupler-regulator, providing 120dB supply rejection and 60dB channel separation. Other outstanding features include high gain (100dB), large output voltage swing (V_{CC} -2V) p-p, and wide power bandwidth (75kHz, 20V p-p). The LM382 operates from a single supply across the wide range of 9 to 40V.

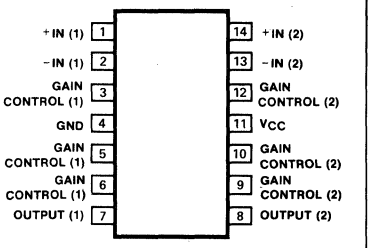
A resistor matrix is provided on the chip to allow the user to select a variety of closed loop gain options and frequency response characteristics such as flat-band, NAB or RIAA equalization. The circuit is supplied in the 14 lead dual-in-line package.

FEATURES

- **Low noise—0.8μV total equivalent input noise**
- **High gain—100dB open loop**
- **Single supply operation**
- **Wide supply range 9 to 40V**
- **Power supply rejection—120dB**
- **Large output voltage swing**
- **Wide bandwidth—15MHz unity gain**
- **Power bandwidth—75kHz, 20V p-p**
- **Internally compensated**
- **Short circuit protected**

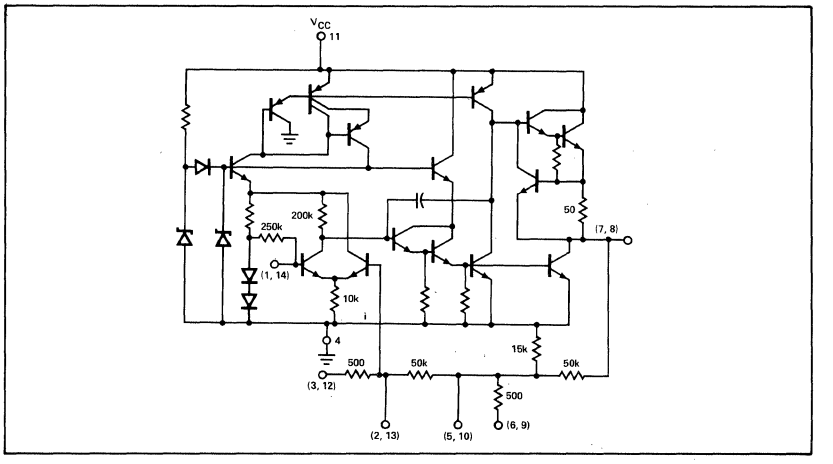
PIN CONFIGURATION

N PACKAGE



ORDER NO.
LM382N

EQUIVALENT SCHEMATIC

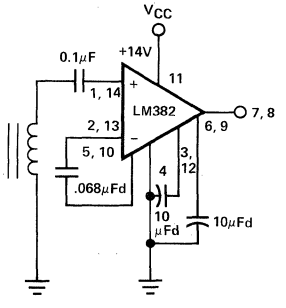


ABSOLUTE MAXIMUM RATINGS

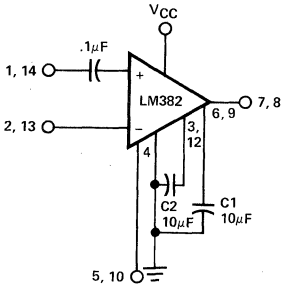
PARAMETER	RATING	UNIT
Supply voltage	+40	V
Power dissipation	600	mW
Operating temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

TYPICAL APPLICATIONS

TAPE PREAMPLIFIER (NAB EQUALIZATION)



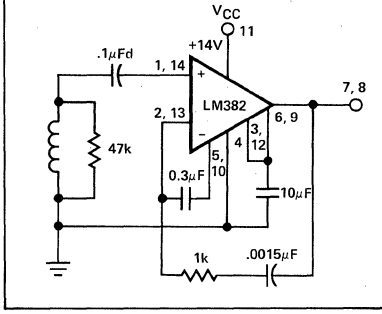
PHONO PREAMP (RIAA EQUALIZATION)



CAPACITOR	GAIN
C1 Only	40dB
C2 Only	55dB
C1 & C2	80dB

TYPICAL APPLICATIONS

FLAT RESPONSE FIXED GAIN CONFIGURATION



LM382-N

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 14V unless otherwise specified.

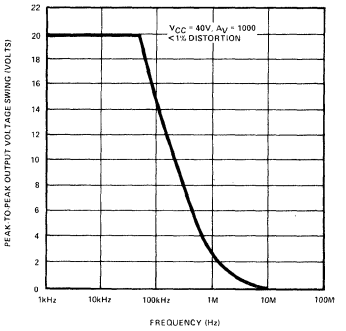
PARAMETER	TEST CONDITIONS	LM382			UNIT
		Min	Typ	Max	
Voltage gain	Open loop (differential input)		100,000		V/V
Supply current	V_{CC} 9 to 40V, $R_L = \infty$		10	16	mA
Input resistance	Positive input		100		kΩ
	Negative input		200		kΩ
Input current	Negative input		0.5		μA
Output resistance	Open loop		150		Ω
Output current	Source		8		mA
	Sink		2		mA
Output voltage swing	Peak-to-peak, R_L = 10k		V_{CC}-2		V

AC ELECTRICAL CHARACTERISTICS

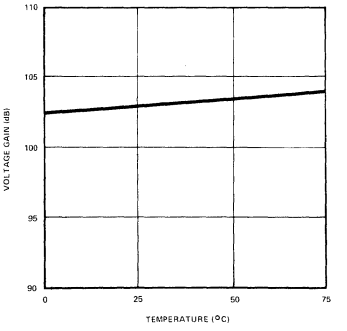
PARAMETER	TEST CONDITIONS	LM382			UNIT
		Min	Typ	Max	
Small signal bandwidth			15		MHz
Power bandwidth	20V p-p (V_{CC} = 24V)		75		kHz
Maximum input voltage	Linear operation			300	mVrms
Supply rejection ratio	f = 1kHz		120		dB
Channel separation	f = 1kHz	40	60		dB
Total harmonic distortion	60dB gain, f = 1kHz		0.1	0.3	%
Total equivalent input noise	R_S = 600Ω, 100-10,000Hz		0.8	1.2	μVrms
Noise figure	50kΩ, 100-10,000Hz		1.0		dB
	10kΩ, 100-10,000Hz		1.6		dB
	5kΩ, 100-10,000Hz		2.6		dB

TYPICAL PERFORMANCE CHARACTERISTICS

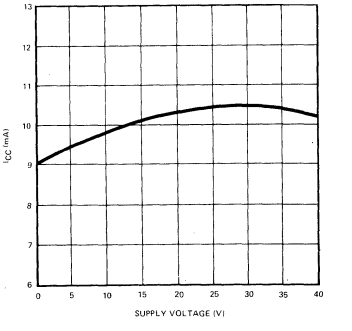
LARGE SIGNAL FREQUENCY RESPONSE



GAIN vs TEMPERATURE



V_{CC} vs I_{CC}



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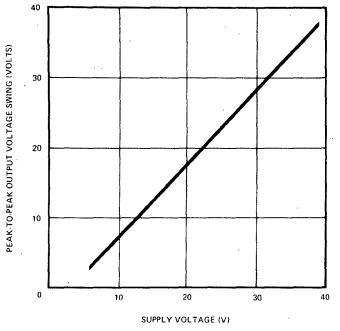
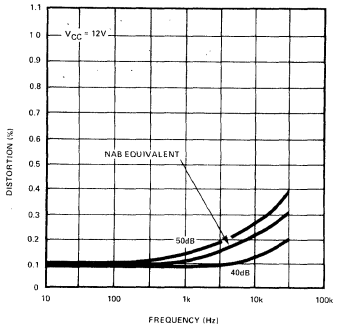
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

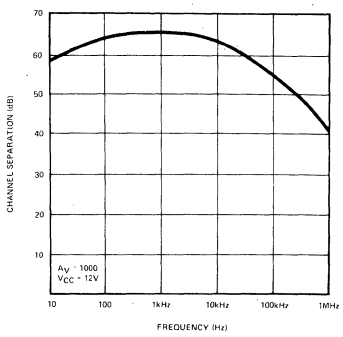
P-P OUTPUT VOLTAGE SWING vs V_{CC}



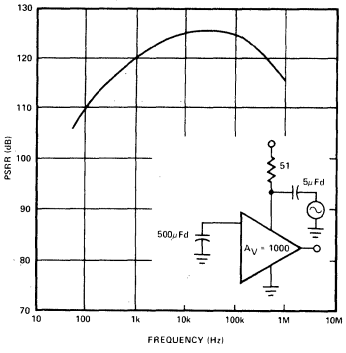
% DISTORTION



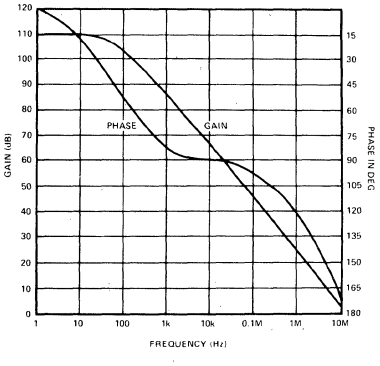
CHANNEL SEPARATION



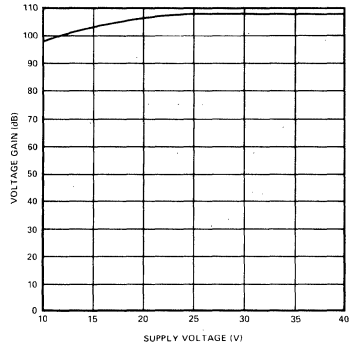
PSRR vs FREQUENCY



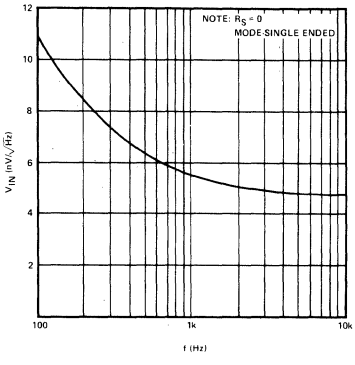
GAIN AND PHASE RESPONSE



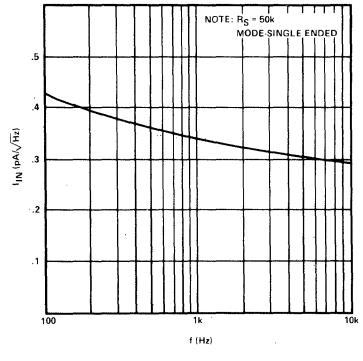
VOLTAGE GAIN vs SUPPLY VOLTAGE



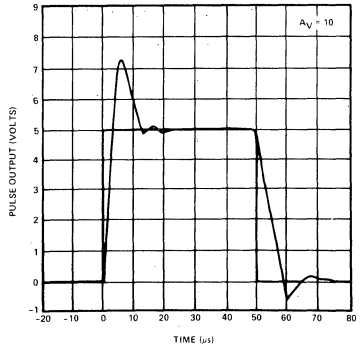
NOISE VOLTAGE vs FREQUENCY



NOISE CURRENT vs FREQUENCY



PULSE RESPONSE



LM387-N

DESCRIPTION

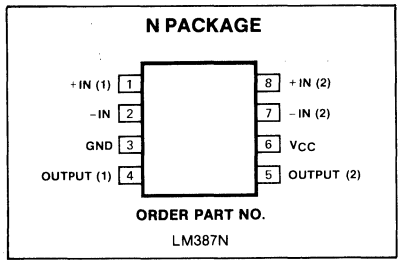
The LM387 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with an internal power supply decoupler-regulator, providing 110dB supply rejection and 60dB channel separation. Other outstanding features include high gain (104dB), large output voltage swing (V_{CC} - 2V p-p), and wide power bandwidth (75kHz, 20V p-p). The LM387 operates from a single supply across the wide range of 9 to 40V.

The amplifiers are internally compensated for all gains greater than 10. The LM387 is available in an 8 lead dual-in-line package.

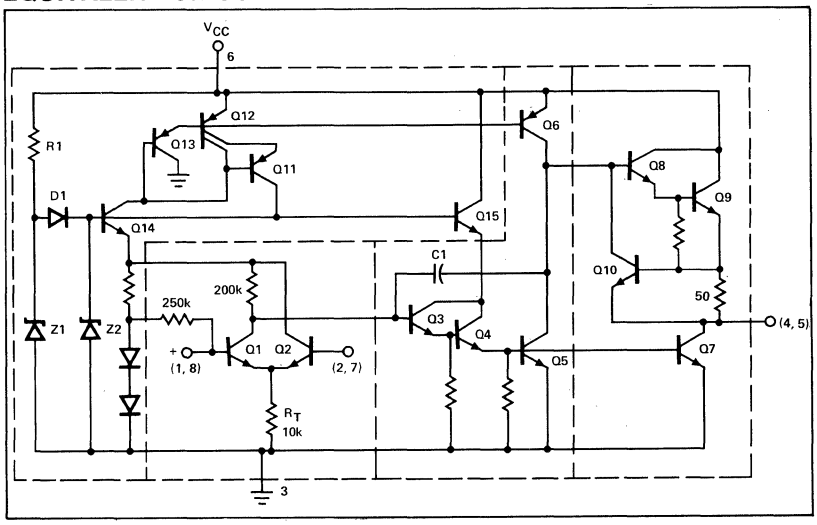
FEATURES

- **Low noise—0.8μV total input noise**
- **High gain—104dB open loop**
- **Single supply operation**
- **Wide supply range 9 to 40V**
- **Power supply rejection—110dB**
- **Large output voltage swing (VCC - 2V p-p)**
- **Wide bandwidth 15MHz unity gain**
- **Power bandwidth 75kHz, 20V p-p**
- **Internally compensated**
- **Short circuit protected**

PIN CONFIGURATION

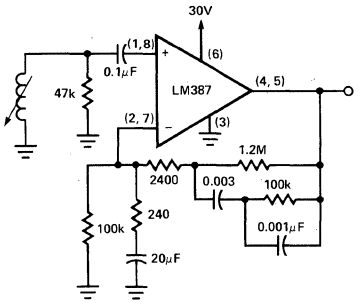


EQUIVALENT CIRCUIT

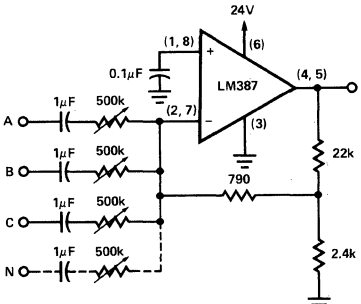


TYPICAL APPLICATIONS

TYPICAL MAGNETIC PHONO PREAMPLIFIER

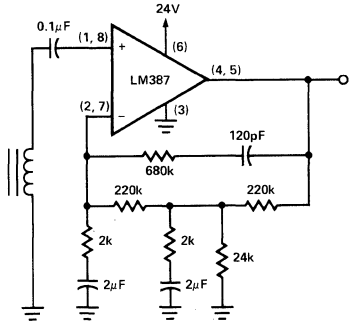


AUDIO MIXER

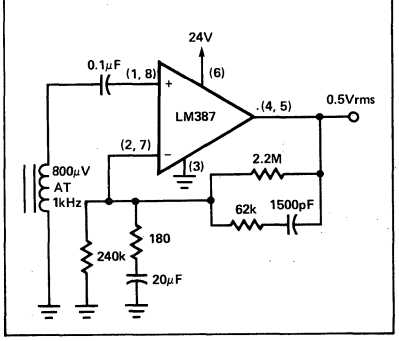


TYPICAL APPLICATIONS

TWO-POLE FAST TURN-ON NAB TAPE PREAMPLIFIER



TYPICAL TAPE PLAYBACK AMPLIFIER



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+40	V
Power dissipation	500	mW
Operating temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

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DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 14V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	LM387			UNIT
		Min	Typ	Max	
Voltage gain	Open loop		160,000		V/V
Supply current	V_{CC} 9 to 40V, $R_L = \infty$		10		mA
Input resistance	Positive input		100		kΩ
	Negative input		200		kΩ
Input current	Negative input		0.5		μA
Output resistance	Open loop		150		Ω
Output current	Source		8		mA
	Sink		2		mA
Output voltage swing	Peak-to-peak		V_{CC}-2		V

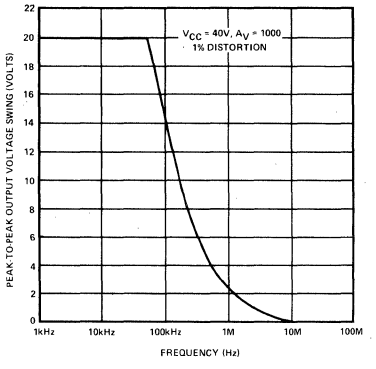
AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 14V$ unless otherwise specified.

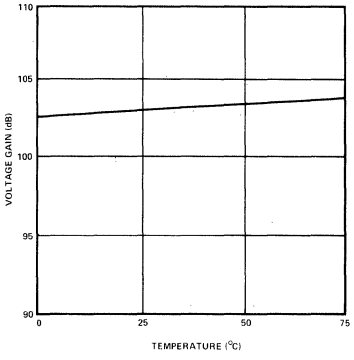
PARAMETER	TEST CONDITIONS	LM387			UNIT
		Min	Typ	Max	
Small signal bandwidth			15		MHz
Power bandwidth	20V p-p ($V_{CC} = 24V$)		75		kHz
Maximum input voltage	Linear operation			300	μVrms
Supply rejection ratio	f = 1kHz		110		dB
Channel separation	f = 1kHz		60		dB
Total harmonic distortion	75dB gain, f = 1kHz		0.1		%
Total equivalent input noise	$R_S = 600Ω$, 100-10,000Hz		0.8	1.4	μVrms
Noise figure	50kΩ, 100-10,000Hz		1.0		dB
	10kΩ, 100-10,000Hz		1.6		dB
	5kΩ, 100-10,000Hz		2.8		dB

TYPICAL PERFORMANCE CHARACTERISTICS

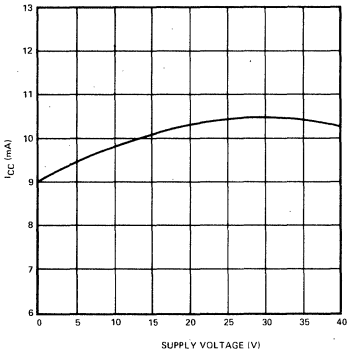
LARGE SIGNAL FREQUENCY RESPONSE



GAIN vs TEMPERATURE

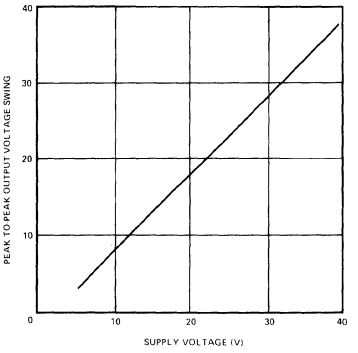


V_{CC} vs I_{CC}

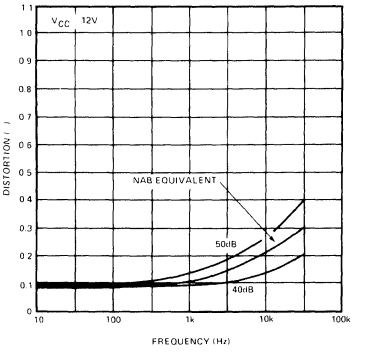


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

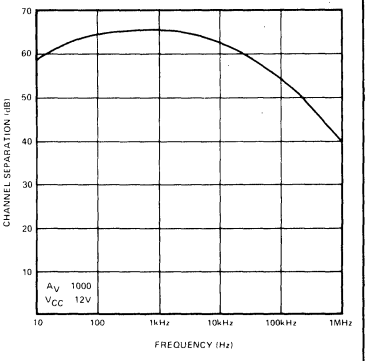
P-P OUTPUT VOLTAGE SWING vs V_{CC}



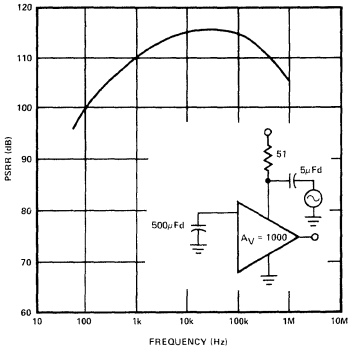
% DISTORTION



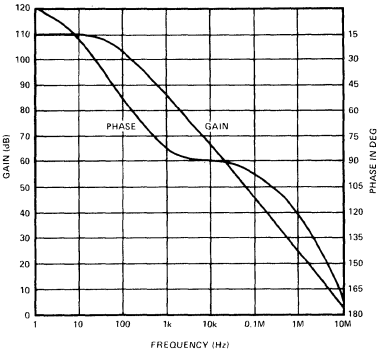
CHANNEL SEPARATION



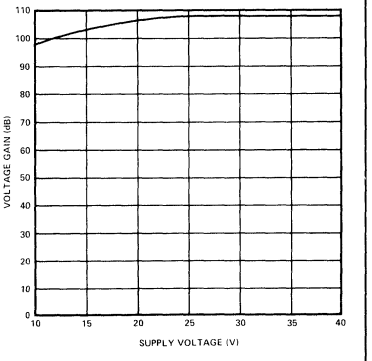
PSRR vs FREQUENCY



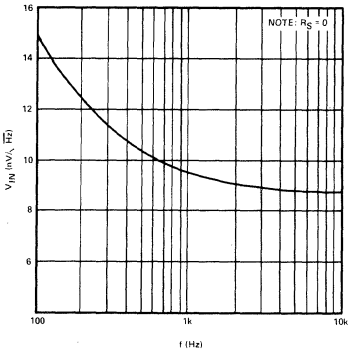
GAIN AND PHASE RESPONSE



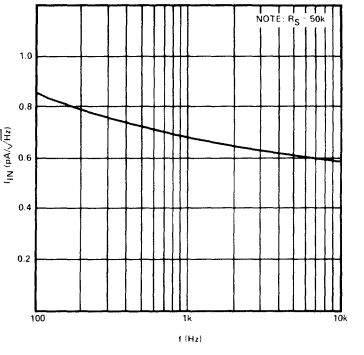
VOLTAGE GAIN vs SUPPLY VOLTAGE



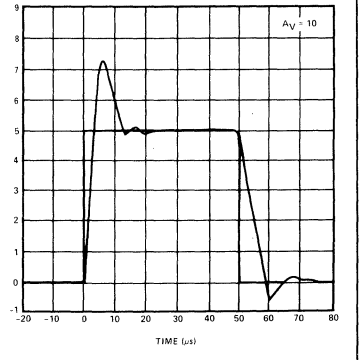
NOISE VOLTAGE vs FREQUENCY



NOISE CURRENT vs FREQUENCY



PULSE RESPONSE



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NE/SE540-L

DESCRIPTION

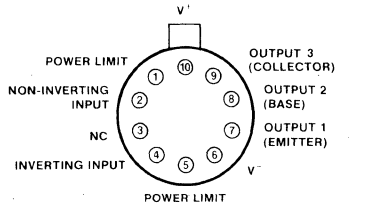
The NE/SE540 is a monolithic, class AB power amplifier designed specifically to drive a pair of complementary output transistors. The device features low standby current yet retains a high output current drive capability with internal current limiting. A wide power bandwidth and excellent linearity make this device ideal for use an audio power amplifier.

FEATURES

- **Internal current limiting**
- **Low standby current**
- **High output current capability**
- **Wide power bandwidth**
- **Low distortion**

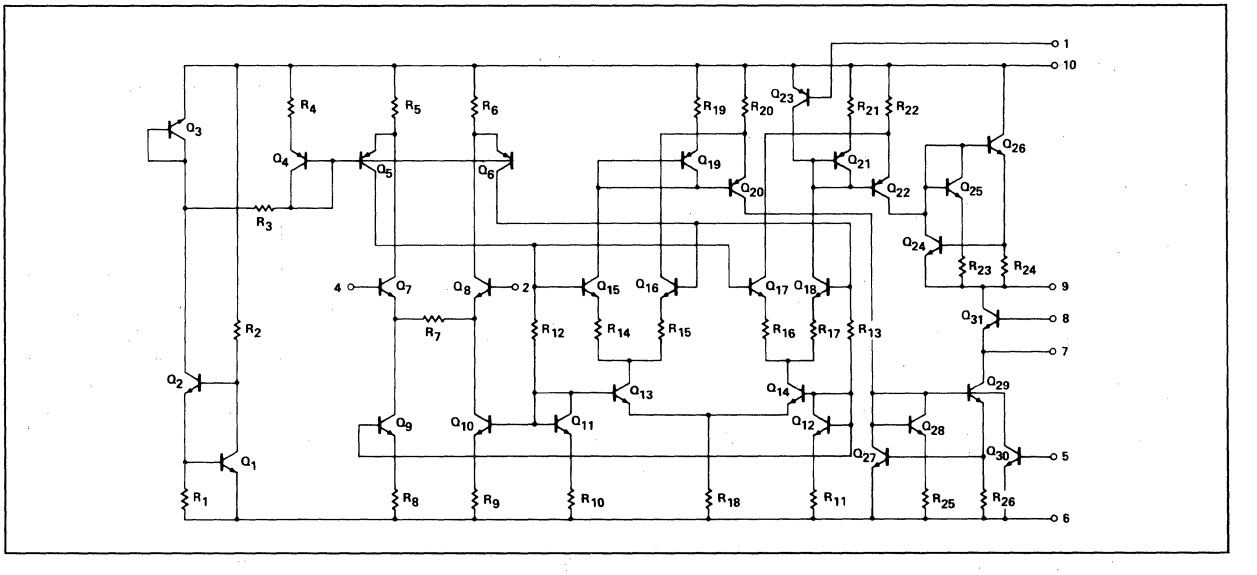
PIN CONFIGURATION

L PACKAGE



ORDER PART NO.
NE540L, SE540L

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE540	±27	V
NE540	±22	V
Operating temperature range		
SE540	-55 to +125	°C
NE540	0 to +70	°C
Storage temperature range	-65 to +150	°C
Output short circuit duration (Not exceeding maximum dissipation.)	Indefinite	

NE/SE540-L

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ and $V_{CC} = \pm 20V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE540			NE540			UNIT
		Min	Typ	Max	Min	Typ	Max	
Operating supply voltage Quiescent current		±5	 13	±25 20	±5	 13	±20 20	V mA
Input offset voltage Input offset current			5 0.3	7 0.7		7 0.5	10 1	mV μA
Input bias current Input impedance			1.5 20	3		2 20	5	μA kΩ
Current gain Gain variation over temperature range	40dB gain	80	100 ±0.1		70	90 ±0.1		dB dB
Power supply rejection ratio Common mode rejection ratio	40dB gain	80	90 110		60	80 90		dB dB
Output drive current		±120	±150		±80	±100		mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ and $V_{CC} = \pm 20V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE540			NE540			UNIT
		Min	Typ	Max	Min	Typ	Max	
Frequency response Distortion	40dB gain ±1dB 40dB gain, Output 3dB below maximum $R_L = 600\Omega$ $R_L = 2k\Omega$		500 0.25 0.06	 0.5 		100 0.5 0.06	 1.0 	kHz %
Equivalent input noise voltage	$R_S = 600\Omega$ 50Hz to 500kHz		 10			 10		 μV
Slew rate	$V_{CC} = \pm 20V$ $V_{OUT} = \pm 15V$		200			200		V/μs

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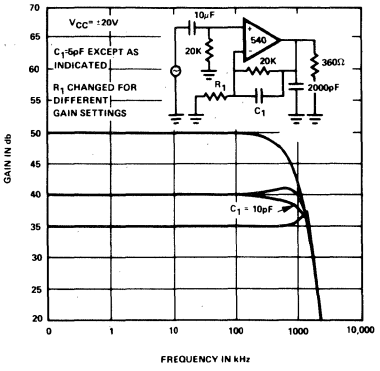
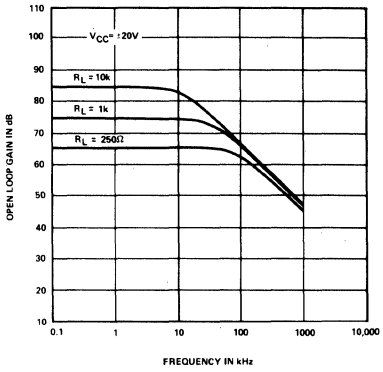
TYPICAL PERFORMANCE CHARACTERISTICS

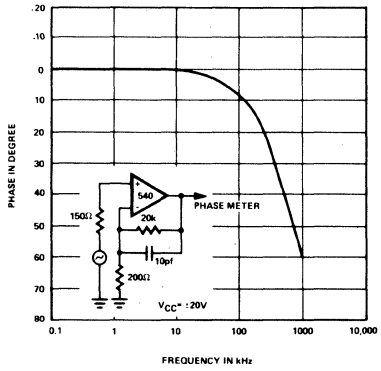
CLOSED LOOP FREQUENCY RESPONSE



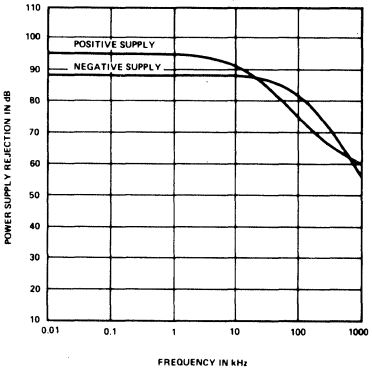
OPEN LOOP GAIN AND FREQUENCY RESPONSE



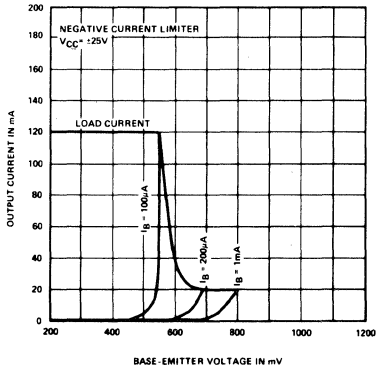
PHASE RESPONSE vs FREQUENCY



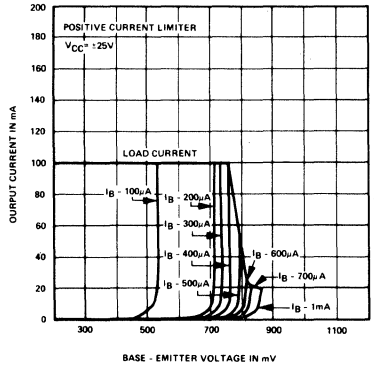
POWER SUPPLY REJECTION vs FREQUENCY



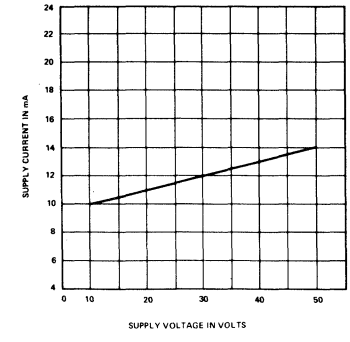
OUTPUT CURRENT vs I_B/V_{BE} OF CURRENT LIMITER



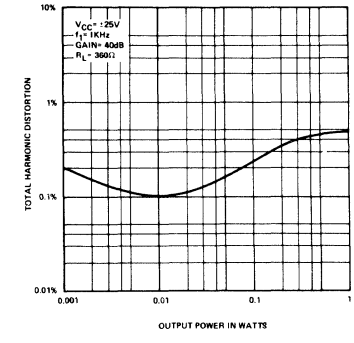
OUTPUT CURRENT vs I_B/V_{BE} OF CURRENT LIMITER



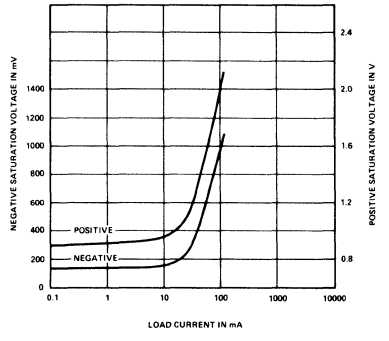
QUIESCENT CURRENT vs SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION vs OUTPUT

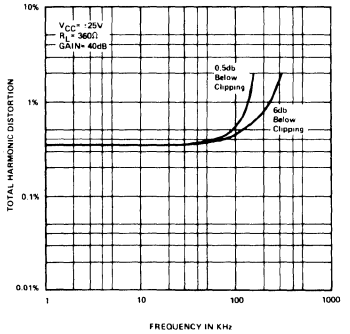


OUTPUT SATURATION VOLTAGE vs LOAD

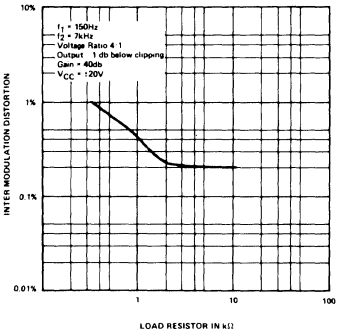


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

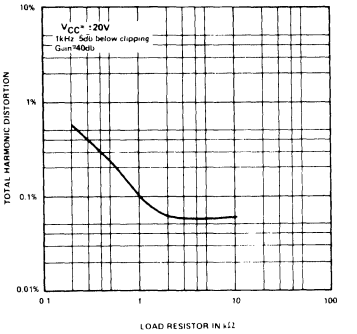
TOTAL HARMONIC DISTORTION vs FREQUENCY



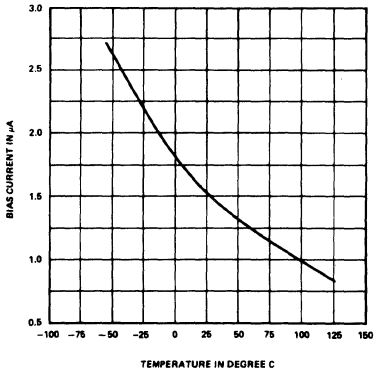
INTERMODULATION DISTORTION vs LOAD



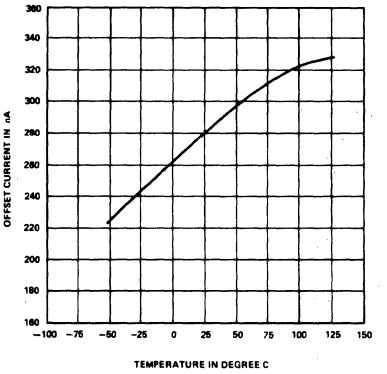
TOTAL HARMONIC DISTORTION vs LOAD



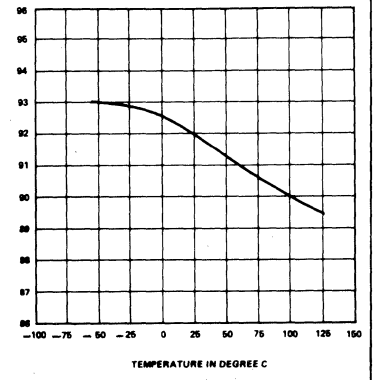
BIAS CURRENT vs TEMPERATURE



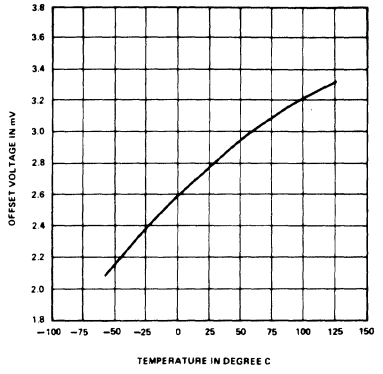
OFFSET CURRENT vs TEMPERATURE



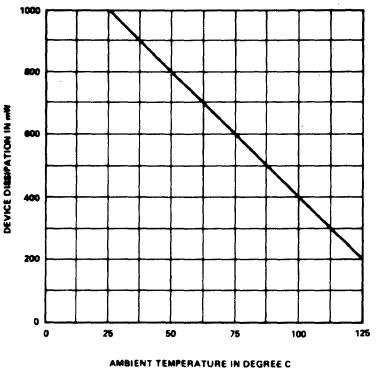
OPEN LOOP GAIN vs TEMPERATURE



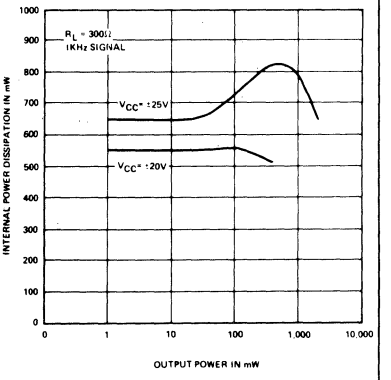
OFFSET VOLTAGE vs TEMPERATURE



MAXIMUM DISSIPATION vs AMBIENT TEMPERATURE



INTERNAL POWER DISSIPATION vs LOAD POWER



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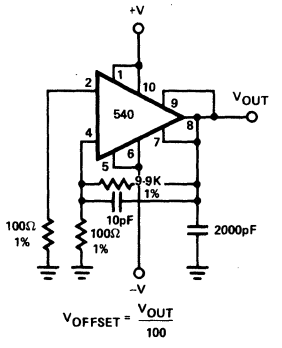
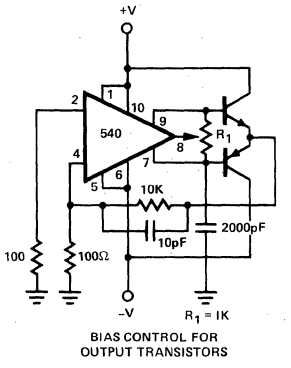
TEST CIRCUITS

OFFSET VOLTAGE MEASUREMENT



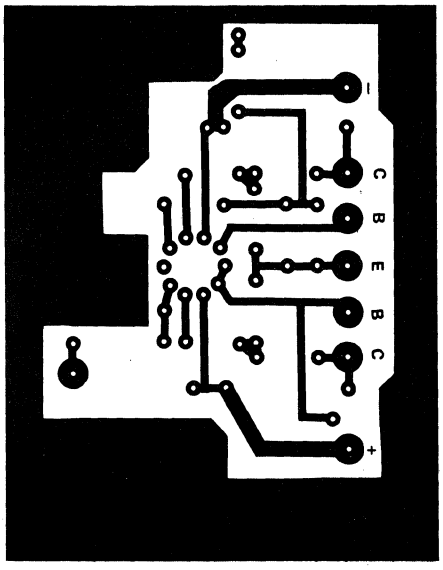
OUTPUT BIAS CONTROL



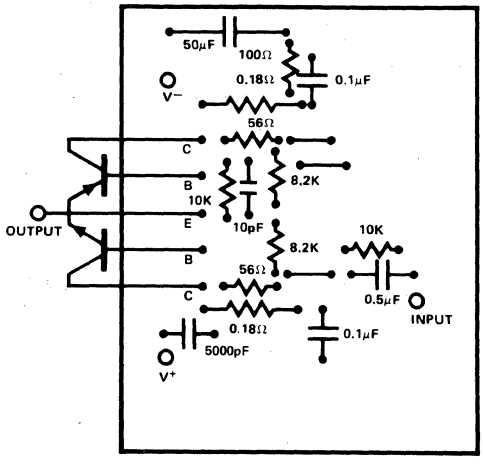
BIAS CONTROL FOR
OUTPUT TRANSISTORS

35 WATT AMPLIFIER

P.C. BOARD LAYOUT
(Bottom View)



PARTS LAYOUT
(Top View)



NE541-PHA

DESCRIPTION

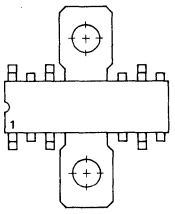
The NE541 is a monolithic, class AB power amplifier designed specifically to drive a pair of complementary output transistors. The device features low standby current yet retains a high output current drive capability with internal current limiting. A wide power bandwidth and excellent linearity make this device ideal for use as an audio power amplifier.

FEATURES

- **Internal current limiting**
- **Low standby current**
- **High output current capability**
- **Wide power bandwidth**
- **Low distortion**

PIN CONFIGURATION

PHA PACKAGE
(Top View)



ORDER PART NO.
NE541 PHA

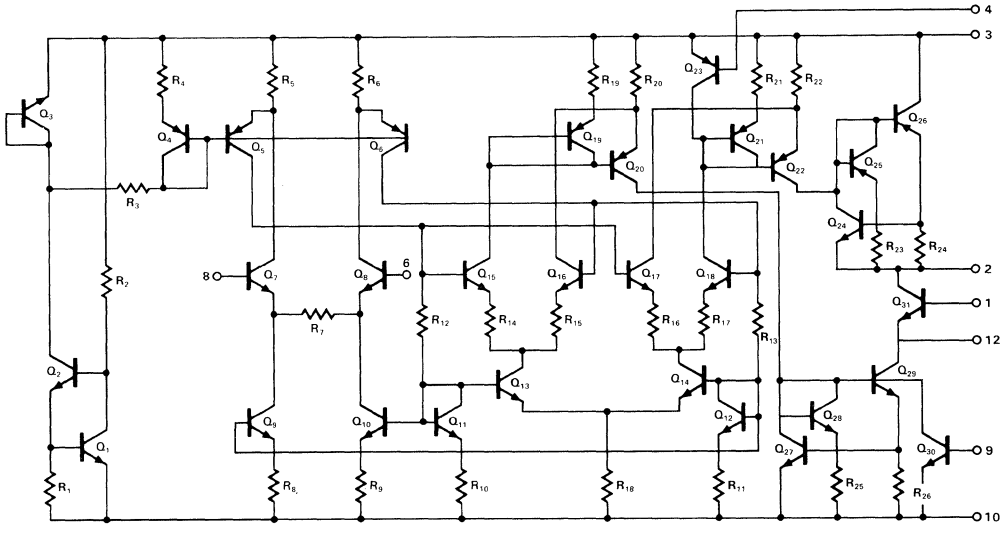
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	±42	V
Operating temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Output short circuit duration (Not exceeding maximum dissipation.)	Indefinite	

PIN DESIGNATION

PIN NO.	NAME AND FUNCTION
1	Output 2 (base)
2	Output 3 (collector)
3	V+
4	Power limit
5	NC
6	Non-inverting input
7	NC
8	Inverting input
9	Power limit
10	V-
11	NC
12	Output 1 (emitter)

BLOCK DIAGRAM



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DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = \pm 40V$ unless otherwise specified.[1]

PARAMETER	TEST CONDITIONS	NE541			UNIT
		Min	Typ	Max	
Operating temperature range Operating supply voltage		0 ±5		+70 ±40	°C V
Quiescent current			14	25	mA
Input offset voltage Input offset current			7 0.5	10 1	mV μA
Input bias current Input impedance	40dB gain		2 20	6	μA kΩ
Current gain Gain variation over temperature range	40dB gain	70	90 ±0.1		dB dB
Power supply rejection ratio Common mode rejection ratio	40dB gain	60	70 90		dB dB
Output drive current		55	80		mA

NOTES

1. Heat sink tab is tied to substrate—do not ground or tie to any voltage.
2. Not exceeding maximum dissipation.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = \pm 40V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	NE541			UNIT
		Min	Typ	Max	
Frequency response Distortion	40dB gain ±1dB 40dB gain, Output 3dB below maximum, $R_L = 600\Omega$		100 0.4	 1.0	kHz %
Equivalent input noise voltage	$R_S = 600\Omega$, 50Hz to 500kHz		10		μV

NE542-N

DESCRIPTION

The NE542 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with individual internal power supply decoupler-regulator, providing 110dB supply rejection and 70dB channel separation. Other outstanding features include high gain (104dB), large output voltage swing (V_{CC} -2Vp-p), and internal compensation to 10dB. The NE542 operates from a single supply across the wide range of 9 to 24V.

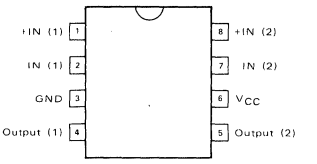
The NE542 is ideal for use in stereo phono, tape, or microphone preamps and other applications requiring low noise amplication of small signals.

FEATURES

- **Low noise—.7μV total input noise**
- **High gain—104dB open loop**
- **Single supply operation**
- **Wide supply range 9 to 24V**
- **Power supply rejection 110dB**
- **Large output voltage swing (V_{CC} -2V p-p)**
- **Wide bandwidth 15MHz unity gain**
- **Power bandwidth 100kHz (15V p-p)**
- **Internally compensated (stable at 10dB)**
- **Short circuit protected**
- **High slew rate 5V/μs**

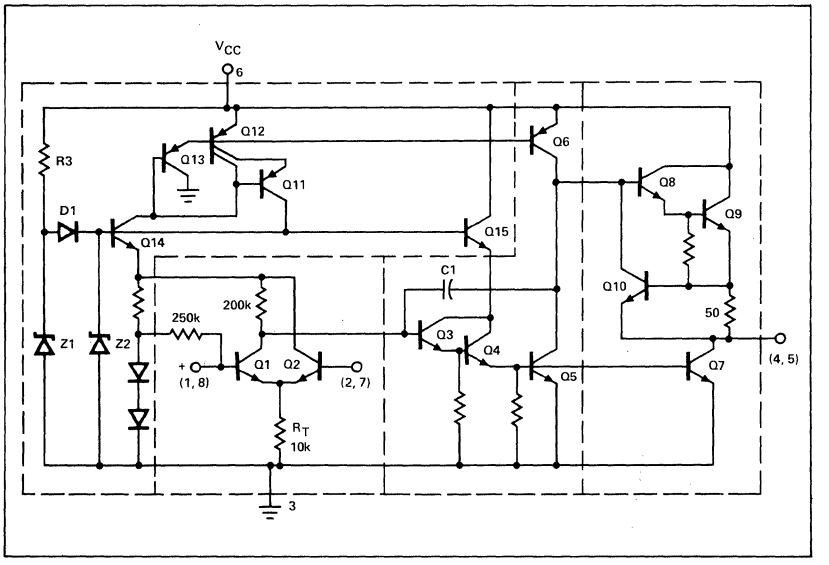
PIN CONFIGURATION

N PACKAGE



ORDER NO.
NE542N

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+24	V
Power dissipation	500	mW
Operating temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 14V$ unless otherwise specified.

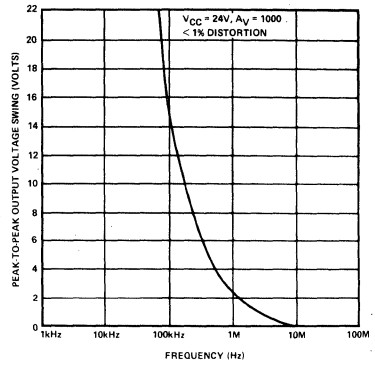
PARAMETER	TEST CONDITIONS	NE542			UNIT
		Min	Typ	Max	
Supply voltage		9		24	V
Supply current	V_{CC} = 9 to 18V, $R_L = \infty$		9	12	mA
Input resistance					
Positive input			100		kΩ
Negative input			200		kΩ
Output resistance	Open loop		150		Ω

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 14V$ unless otherwise specified.

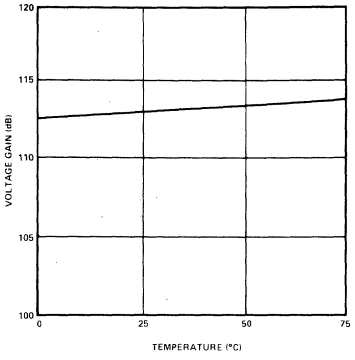
PARAMETER	TEST CONDITIONS	NE542			UNIT
		Min	Typ	Max	
Voltage gain	Open loop		160,000		V/V
Input current Negative input			 .5		 μA
Output current	Source Sink (linear operation)	8 2	14 3		mA mA
Output voltage swing Small signal bandwidth Slew rate Power bandwidth	 15V p-p	V_{CC} -2.5	V_{CC} -2 15 5 100		V MHz V/μs kHz
Maximum input voltage	Linear operation			300	mVrms
Supply rejection ratio Channel separation	f = 60, 120Hz f = 1kHz f = 1kHz		100 110 70		dB dB dB
Total harmonic distortion Total equivalent input Noise	75dB gain, f = 1kHz RS = 600Ω, 100 - 10,000Hz		.1 .7	 1,2	% μVrms
Noise figure	RS = 50kΩ, 10 - 10,000Hz RS = 20kΩ, 10 10,000Hz RS = 10kΩ, 10 - 10,000Hz RS = 5kΩ, 10 - 10,000Hz		1.2 1.2 1.5 2.4		dB dB dB dB

TYPICAL PERFORMANCE CHARACTERISTICS

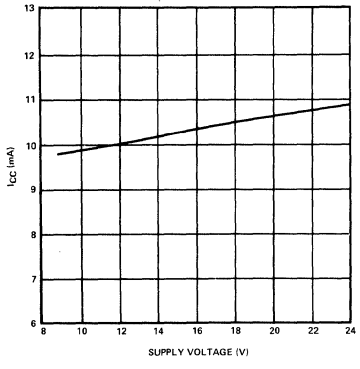
LARGE SIGNAL FREQUENCY RESPONSE



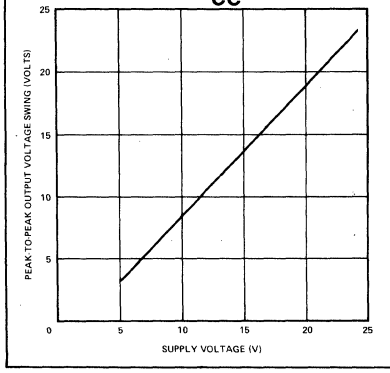
GAIN vs TEMPERATURE



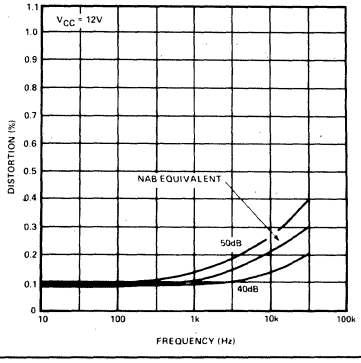
V_{CC} vs I_{CC}



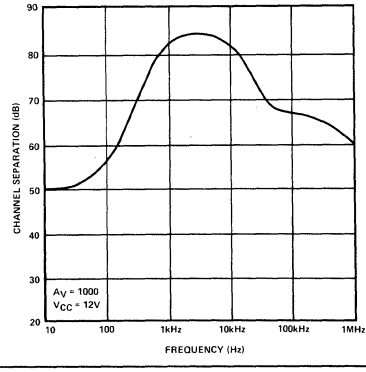
P-P OUTPUT VOLTAGE SWING vs V_{CC}



% DISTORTION

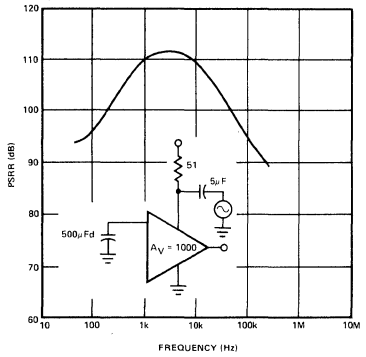


CHANNEL SEPARATION

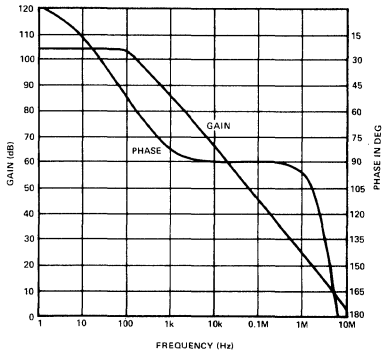


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

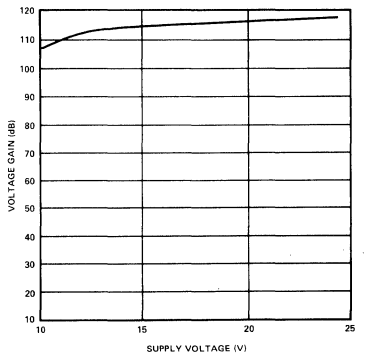
PSRR vs FREQUENCY



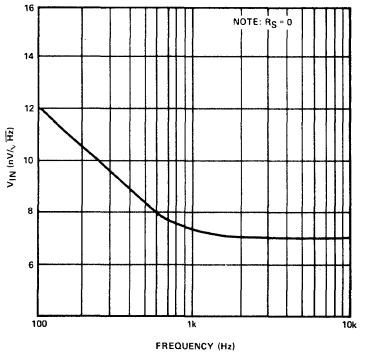
GAIN AND PHASE RESPONSE



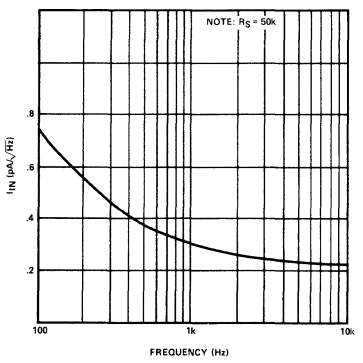
VOLTAGE GAIN vs SUPPLY VOLTAGE



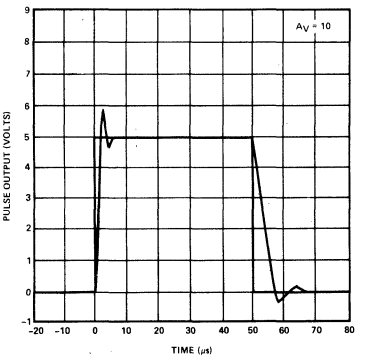
NOISE VOLTAGE vs FREQUENCY



NOISE CURRENT vs FREQUENCY

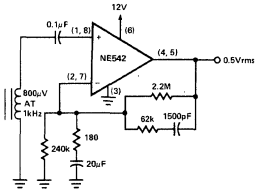


PULSE RESPONSE

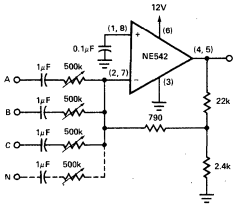


TYPICAL APPLICATIONS

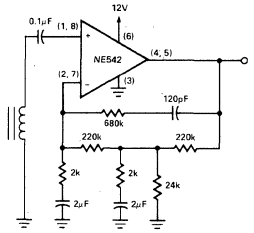
TYPICAL TAPE PLAYBACK AMPLIFIER



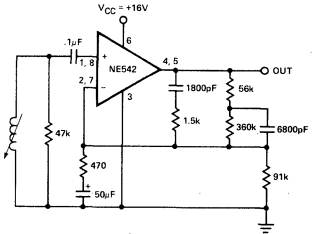
R1AA MAGNETIC PHONO PREAMP



TWO-POLE FAST TURN-ON NAB TAPE PREAMP



AUDIO MIXER



NOTE: All resistors values are typical and in ohms.

DESCRIPTION

The 570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full wave rectifier to detect the average value of the signal; a linerarized, temperature compensated variable gain cell; and an operational amplifier.

The 570/571 is well suited for use in telephone subscriber and trunk carrier systems, communications systems and hi-fi audio systems.

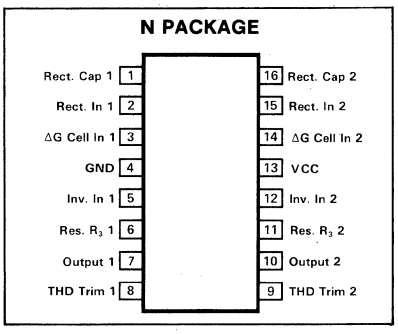
FEATURES

- **Complete compressor and expandor in 1 IC**
- **Temperature compensated**
- **Greater than 110dB dynamic range**
- **Operates down to 6Vdc**
- **System levels adjustable with external components**
- **Distortion may be trimmed out**

APPLICATIONS

- **Telephone trunk compandor—570**
- **Telephone subscriber compandor—571**
- **High level limiter**
- **Low level expandor—noise gate**
- **Dynamic noise reduction systems**
- **Voltage controlled amplifier**
- **Dynamic filters**

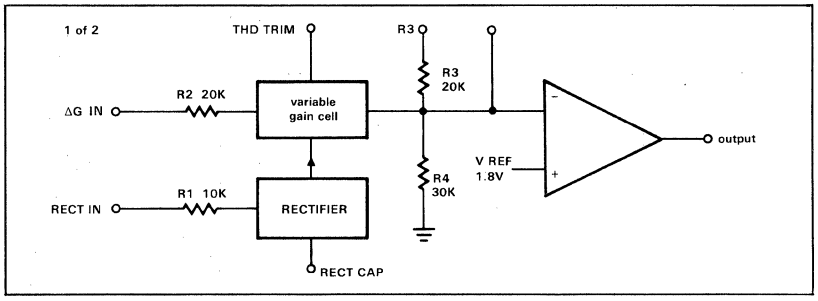
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
	Positive supply		Vdc
	570	24	
	571	18	
T_A	Operating temperature range	-40 to +70	°C
P_D	Power dissipation	400	mW

BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The 570/571 compandor building blocks, as shown in the block diagram, are a full wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively coupled voltage inputs as shown in the following equation. Note that for capacitively coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than .1μA.

$$G \propto \frac{|V_{IN} - V_{REF}|_{ave}}{R_1}$$

or

$$G \propto \frac{|V_{IN}|_{ave}}{R_1}$$

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expandor or compressor application, this would lead to third harmonic distortion, so there is a tradeoff to be made between fast attack and decay times, and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})\ e^{-t/\tau} + G_{final};\quad \tau = 10K \times C_{RECT}$$

The variable gain cell is a current in, current out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the ΔG input to an internal summing node biased at V_{REF}. The following equation applies for capacitively coupled inputs. The output current, I_{OUT}, is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

A compensation scheme built into the ΔG cell compensates for temperature, and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

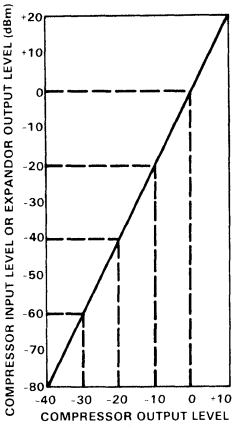
The operational amplifier (which is internally compensated) has the non-inverting input tied to V_{REF}, and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, R_3, is brought out from the summing node and allows compressor or expandor gain to be determined only by internal components. The output stage is capable of ±20mA output current. This allows a +13dBm (3.5V rms) output into a 300Ω load which, with a series resistor and proper transformer, can result in +13dBm with a 600Ω output impedance.

A band gap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and ΔG cell, and a bias current for the ΔG cell. The low tempco of this type of reference provides very stable biasing over a wide temperature range.

The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expandor circuits.

TYPICAL PERFORMANCE CHARACTERISTICS

BASIC INPUT-OUTPUT TRANSFER CURVE



DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 15V$[1]

PARAMETER	TEST CONDITIONS	NE570			NE571			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{CC} Supply voltage		6		24	6		18	V
I_{CC} Supply current	No signal		3.2	4.0				mA
Output current capability		±20						mA
Output slew rate			±.5					V/us
Gain cell distortion[2]	Untrimmed		.3	1.0		.5	2.0	%
	Trimmed		.05			.1		
Resistor tolerance			±5	±15				%
Internal reference voltage		1.7	1.8	1.9	1.65	1.8	1.95	V
Output dc shift[3]	Untrimmed		±20	±50		±30	±100	mV
Expandor output noise	No signal, 20Hz-20kHz		20					μV
			-15					dBRNC
Unity gain level		-1	0	+1	-1.5	0	+1.5	dBm
Gain change[2,4]	-40°C < T < 70°C		±.1	±.3		±.1	±.5	dB
	0°C < T < 70°C		±.1	±.2		±.1	±.4	
Reference drift[4]	-40°C < T < 70°C		+2, -25	-10, -40		+2, -25	+20, -50	mV
	0°C < T < 70°C		±5	±10		±5	±20	
Resistor drift[4]	-40°C < T < 70°C		+8,-0					%
	0°C < T < 70°C		+1,-0					
Tracking error[5]	Rectifier input=							dB
	+6dBm		±.2					
	-10dBm		+.2	-.2,+.4		+.2	-.2,+.5	
	-20dBm		+.2	-.3,+.6		+.2	-.4,+.7	
	-30dBm		+.2	-.5,+1		+.2	-1,+1.5	
	-40dBm		+.2,-.4			+.2,-.4		

NOTES

1. Except where indicated, the 571 specifications are identical to the 570
2. Measured at OdBm
3. Expandor ac input change from no signal to OdBm
4. Relative to value at $T_A = 25°C$
5. Relative to OdBm

SECTION 13
RADIO CIRCUITS

CA3089-N

DESCRIPTION

CA3089 is a monolithic integrated circuit that provides all the functions of a comprehensive FM-IF system. Figure 6 is a block diagram showing the CA3089 features, which include a three-stage FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable features such as delayed AGC for the RF tuner, an AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of +8 to +18 volts.

The CA3089 is ideal for high-fidelity operation. Distortion in a CA3089 FM-IF system is primarily a function of the phase linearity characteristic of the outboard detector coil.

The CA3089 utilizes a 16-lead dual-in-line plastic package and can operate over the ambient temperature range of -40°C to +85°C.

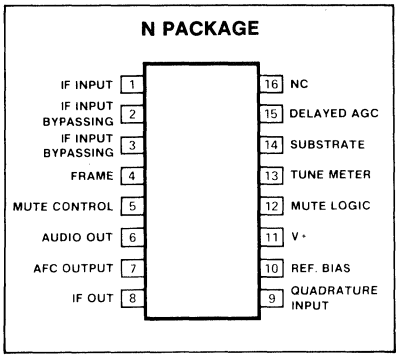
FEATURES

- **Exceptional limiting sensitivity: 10μV typ. at -3dB point**
- **Low distortion: 0.1% typ. (with double-tuned coil)**
- **Single-coil tuning capability**
- **High recovered audio: 400mV typ.**
- **Provides specific signal for control of interchannel muting (squelch)**
- **Provides specific signal for direct drive of a tuning meter**
- **Provides delayed AGC voltage for RF amplifier**
- **Provides a specific circuit for flexible AFC**
- **Internal supply/voltage regulators**

APPLICATIONS

- **High-fidelity FM receivers**
- **Automotive FM receivers**
- **Communications FM receivers**

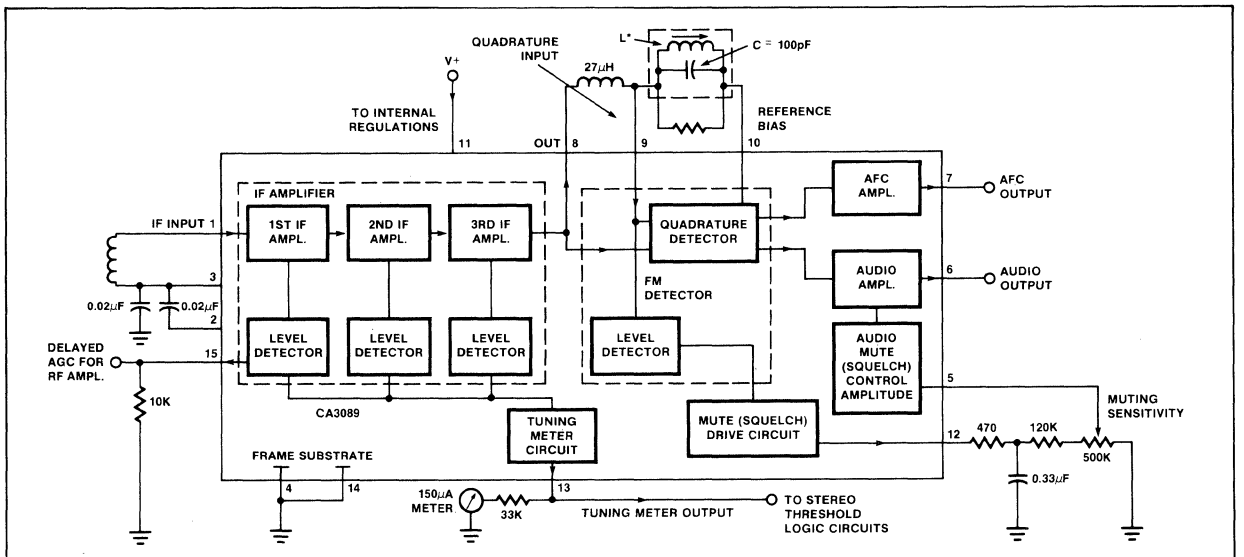
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
DC supply voltage:		
Between terminals 11 and 4	18	V
Between terminals 11 and 14	18	V
DC Current (out of terminal 15)	2	mA
Device dissipation:		
Up to T_A = 60°C	600	mW
Above T_A = 60°C	derate linearly 6.7	mW/°C
Ambient temperature range:		
Operating	-40 to +85	°C
Storage	-65 to +150	°C
Lead temperature (during soldering):		
At distance not less than 1/32" (0.79mm) from case for 10 seconds max.	+265	°C

BLOCK DIAGRAM



NOTE

All resistors values are typical and in ohms.
*L tunes with 100pF (C) at 10.7MHz
Q_O≅ 75 (G.I. EX22741 or equivalent)

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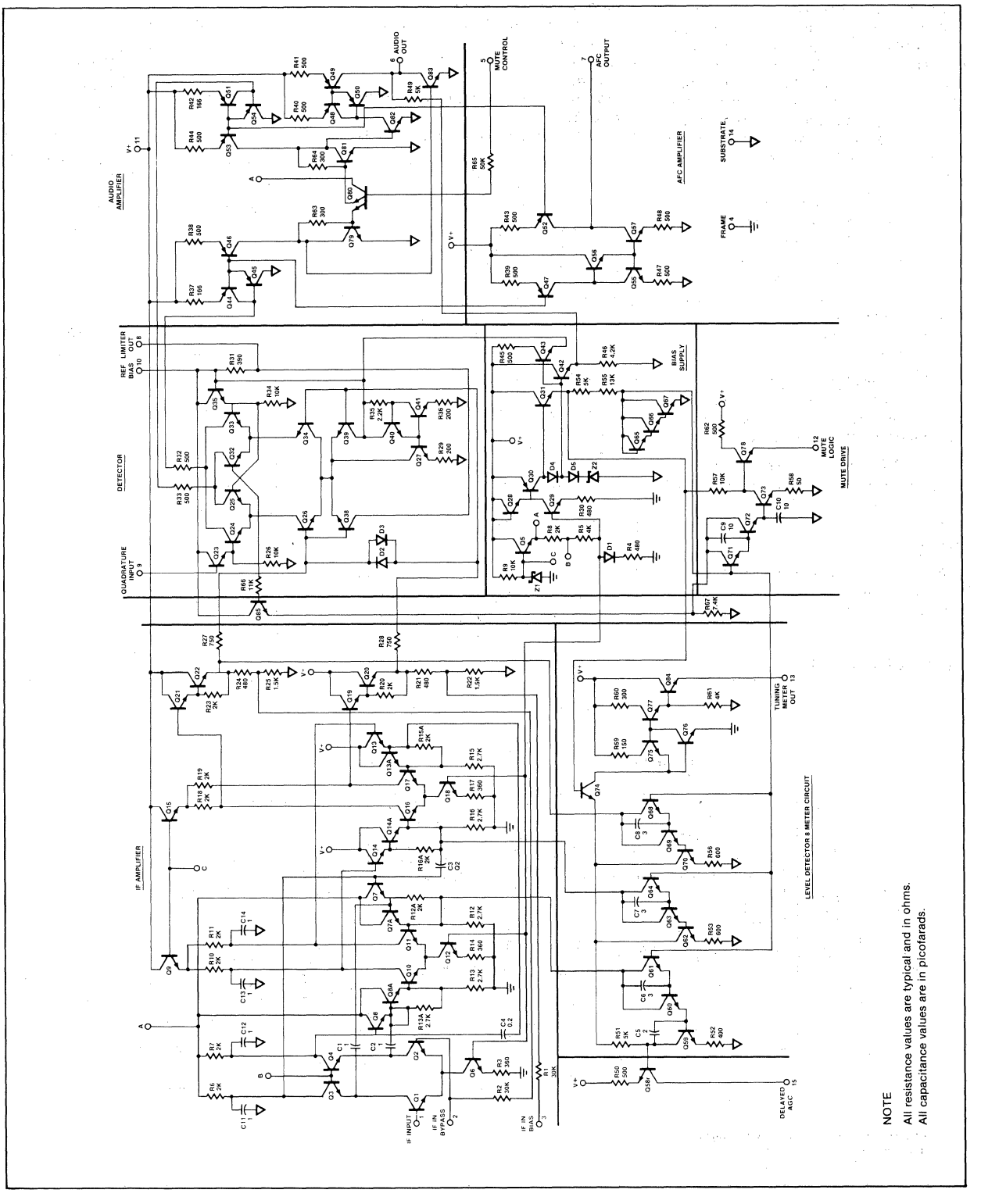
EQUIVALENT SCHEMATIC



NOTE
All resistance values are typical and in ohms.
All capacitance values are in picofarads.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V^+ = 12V$ unless otherwise specified.

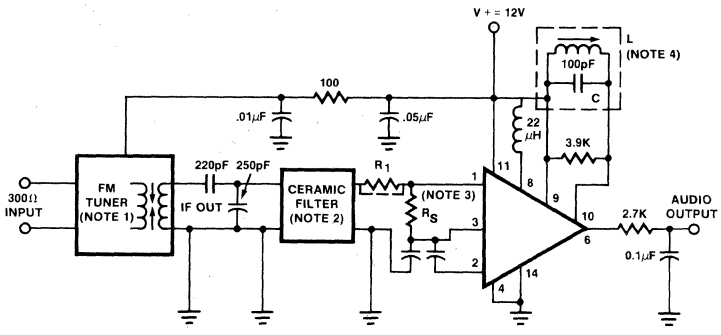
PARAMETER		TEST CONDITIONS	CA3089			UNIT
			Min	Typ	Max	
STATIC (DC) CHARACTERISTICS						
I_{11}	Quiescent circuit current	No signal input, non-muted	16	23	30	mA
DC Voltages:[4]						
V_1	Terminal 1 (IF input)	No signal input, non-muted	1.2	1.9	2.4	V
V_2	Terminal 2 (ac return to input)	No signal input, non-muted	1.2	1.9	2.4	V
V_3	Terminal 3 (dc bias to input)	No signal input, non-muted	1.2	1.9	2.4	V
V_6	Terminal 6 (audio output)	No signal input, non-muted	5.0	5.6	6.0	V
V_7	Terminal 7 (A.F.C.)	No signal input, non-muted	5.0	5.6	6.0	V
V_{10}	Terminal 10 (dc reference)	No signal input, non-muted	5.0	5.6	6.0	V
DYNAMIC CHARACTERISTICS						
$V_{I(lim)}$	Input limiting voltage (-3dB point)[3]			10	25	μV
	AMR AM Rejection (terminal 6)[4]	V_{IN} = 0.1V, F_o = 10.7MHz, f_{mod} = 400Hz, AM Mod = 30%	45	55		dB
V_O	Recovered audio voltage (terminal 6)[3]		300	400	500	mV
Total harmonic distortion:[1]						
THD	Single tuned (terminal 6)[3]			0.5	1.0	%
THD	Double tuned (terminal 6)[4]	f_{mod} = 400Hz, V_{IN} = 0.1		0.1		%
S+N/N	Signal plus noise to noise ratio (terminal 6)[3]	Deviation = ±75kHz	60	67		dB
MU_{IN}	Mute input (terminal 5)	V_5 = 2.5V		70		dB
MU_{OUT}	Mute output (terminal 12)	V_{IN} = 50μV			.5	V
		V_{IN} = 0V	4.0			V
MTR	Meteroutput (terminal 13)	V_{IN} = 0.1V	3.5	4.5		V
		V_{IN} = 500μV	1.0	1.5		V
		V_{IN} = 0V			.7	V
AGC	Delayed AGC (terminal 15)	V_{IN} = 0.1V			.5	V
		V_{IN} = 10μV	4.0	5.0		V
THD	Double tuned (terminal 6)[4]	f_{mod} = 400Hz, V_{IN} = 0.1		0.1		%

NOTES

1. THD characteristics and Audio Level are essentiallly a function of the phase and Q characteristics of the network connected between terminals 8, 9 and 10.
2. Test circuit Figure 1.
3. Test circuit Figure 2.
4. Test circuit Figures 1 and 2.

TEST CIRCUITS

TYPICAL FM TUNER (With a single-tuned detector coil.)



NOTES: All resistors values are typical and in ohms.

1. Waller 4SN3FIC or equivalent
2. Murate SFG 10.7mA or equivalent
3. R_S will affect stability depending on circuit layout. To increase stability R_S is decreased. Range of R_S is 330 to 50Ω, $R_1 + R_S \leq 330\Omega$
4. L tunes with 100pF (C) at 10.7MHz
   Q_O unloaded ≅ 75 (G.I. EX2274I or equivalent)

Performance data at f_o = 98MHz, f_{MOD} = 400Hz, deviation = ±74kHz:

-3dB limiting sensitivity	2μV (antenna level)
20dB quieting sensitivity	1μV (antenna level)
30dB quieting sensitivity	1.5μV (antenna level)

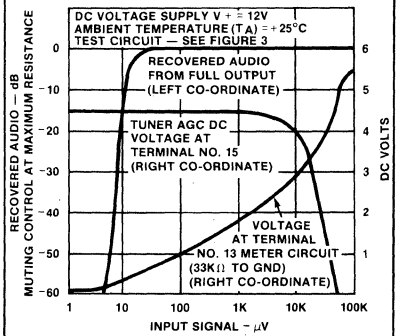
SYSTEM DESIGN CONSIDERATIONS

The CA3089 is a very high gain device and therefore careful consideration must be given to the layout of external components to minimize feedback. The input by-pass capacitors should be located close to the input terminals and the values should not be large nor should the capacitors be of the type which might introduce inductive reactance to the circuit. An example of good by-pass capacitors would be ceramic disc with values in the range of .01 to .05 microfarad.

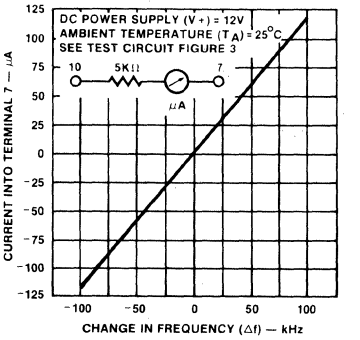
The input impedance of the CA3089 is approximately 10,000 ohms. It is *not* recommended to match this impedance. The value of the input termination resistor should be as low as possible without degrading system operation. The lower the value of this resistor the greater the system stability. An input terminating resistor between 50 and 100 ohms is recommended.

TYPICAL PERFORMANCE CHARACTERISTICS

MUTING ACTION, TUNER AGC
(Tuning meter output as a function of input signal voltage.)

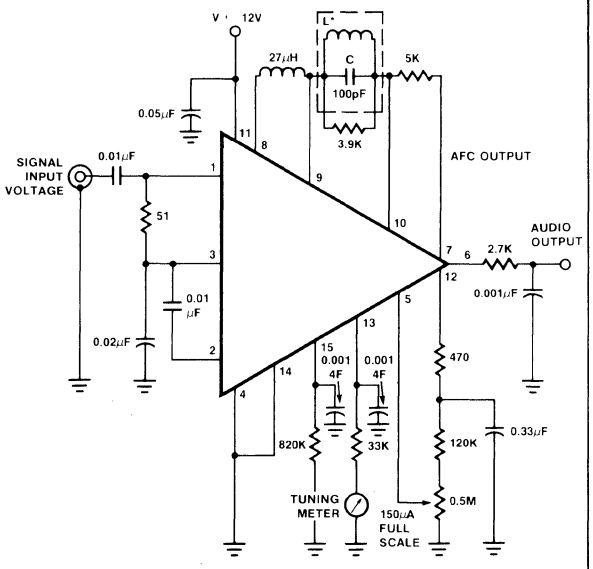


AFC CHARACTERISTICS
(Current at Term. 7 as a function of change in frequency.)



TEST CIRCUITS

TEST CIRCUIT
(Using a single-tuned detector coil.)

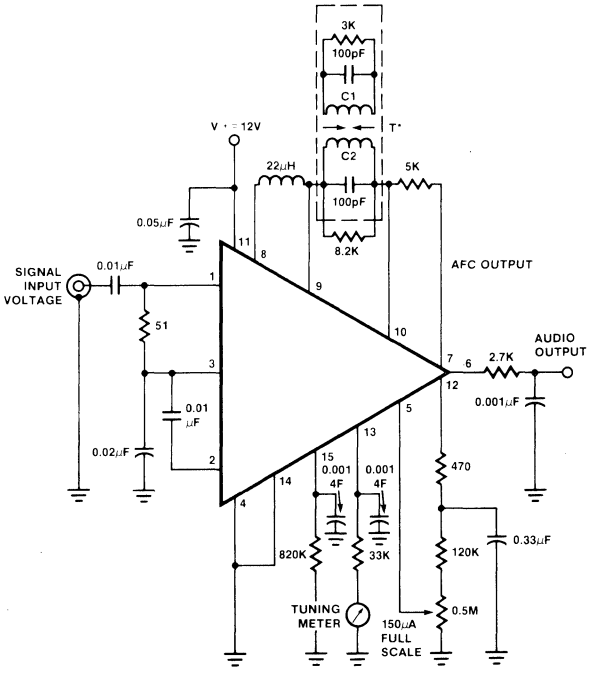


*NOTE

L tunes with 100pF (C) at 10.7MHz.
All resistors values are typical and in ohms.
Q_0 (unloaded) ≅ 75 (G.I. automatic mfg. div. EX22741 or equivalent).

Figure 1

TEST CIRCUIT
(Using a double-tuned detector coil.)



*NOTE: All resistors values are typical and in ohms.

T: Pri. - Q_0 (unloaded) ≅ 75 (tunes with 100pF (C1) 20 † of 34e on 7/32" dia. form)
Sec. - Q_0 (unloaded) ≅ 75 (tunes with 100pF (C2) 20 † of 34e on 7/32" dia. form)
kQ (percent of critical coupling) > 70%
(Adjusted for coil voltage V_C) = 150mV
Above values permit proper operation of mute (squelch) circuit "E" type slugs, spacing 4mm

Figure 2

DESCRIPTION

The 5596 is a monolithic Double-Balanced Modulator/Demodulator designed for use where the output voltage is a product of an input voltage (signal) and a switched function (carrier). The S5596 will operate over the full military temperature range of -55°C to +125°C. The N5596 is intended for applications within the range of 0°C to +70°C.

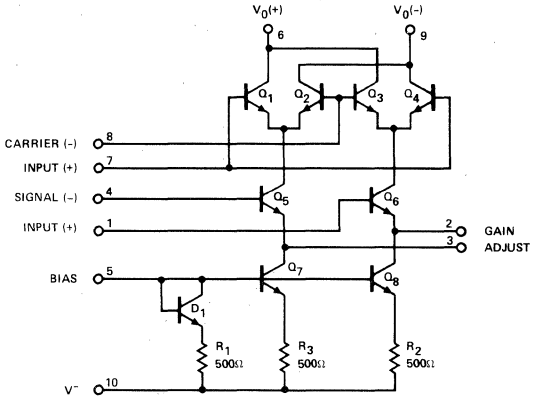
APPLICATIONS

- **Suppressed carrier and amplitude modulation**
- **Synchronous detection**
- **FM detection**
- **Phase detection**
- **Sampling**
- **Single sideband**
- **Frequency doubling**

FEATURES

- **Excellent carrier suppression**
  65dB typ @ 0.5MHz
  50dB typ @ 10MHz
- **Adjustable gain and signal handling**
- **Balanced inputs and outputs**
- **High common-mode rejection—85dB typ**

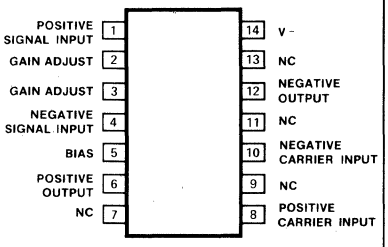
EQUIVALENT SCHEMATIC



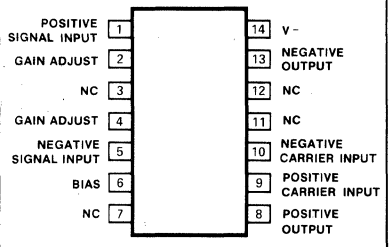
(Pinout for K pkg. shown)

PIN CONFIGURATIONS

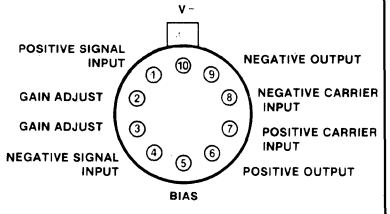
N PACKAGE
MC1496/MC1596



N PACKAGE
5596



K PACKAGE
5596, MC1496, MC1596
(Top View)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Applied voltage[1,2]	30	V
Differential input signal (V_7-V_8)	±5.0	V
Differential input signal (V_4-V_1)	(5 ± I_5 R_e)	V
Input signal (V_2-V_1, V_3-V_4)	5.0	V
Bias current (I_5)	10	mA
Power dissipation (pkg. limitation)		
K package	680	mW
Derate above 25°C	5.4	mW/°C
A package (TO-116)	900	mW
Derate above 25°C	7.2	mW/°C
Operating temperature range	-55 to +125	°C
Storage temperature range	-65 to +150	°C

NOTES

1. Voltage applied between pins 6-7, 8-1, 9-7, 9-8, 7-4, 7-1, 8-4, 6-8, 2-5, 3-5.
2. Pin number references pertain to K package pinout only.

DC ELECTRICAL CHARACTERISTICS

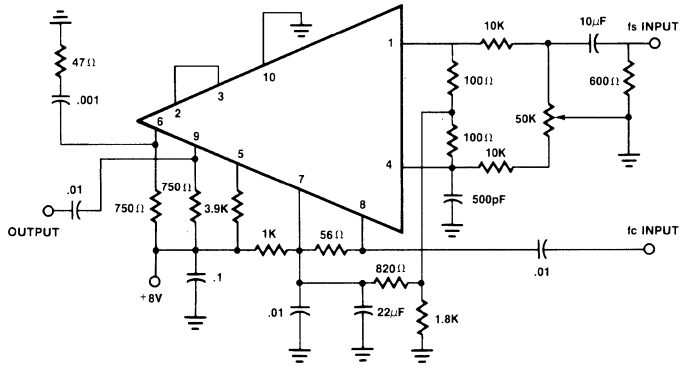
$V^+ = +12Vdc$, $V^- = -9.0Vdc$, $I_5 = 1.0mAdc$, $R_L = 3.9k\Omega$, $R_e = 1.0k\Omega$, $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	MC1596			MC1496/5596			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Single-ended input impedance	Signal port, f = 5.0MHz							
R_{ip}	Parallel input resistance			200			200		kΩ
C_{ip}	Parallel input capacitance			2.0			2.0		pF
	Single-ended output impedance	f = 10MHz							
R_{op}	Parallel output resistance			40			40		kΩ
C_{op}	Parallel output capacitance			5.0			5.0		pF
	Input bias current								μA
I_{bS}	$I_{bS} = \frac{I_1 + I_4}{2}$			12	25		12	30	
I_{bC}	$I_{bS} = \frac{I_7 + I_8}{2}$			12	25		12	30	μA
	Input offset current								μA
I_{ioS}	$I_{ioS} = I_1 - I_4$			0.7	5.0		0.7	7.0	
I_{ioC}	$I_{ioC} = I_7 - I_8$			0.7	5.0		0.7	7.0	μA
T_CI_{io}	Average temperature coefficient of input offset current	$T_A = -55°C$ to $+125°C$		2.0			2.0		nA/°C
	Output offset current								
I_{oo}	$I_6 - I_9$			14	50		15	80	μA
T_CI_{oo}	Average temperature coefficient of output offset current	$T_A = -55°C$ to $+125°C$		90			90		nA/°C
	Common-mode quiescent								
V_o	Output voltage (Pin 6 or Pin 9)			8.0			8.0		Vdc
	Power supply current								mAdc
I_{D+}	$I_6 + I_9$			2.0	3.0		2.0	4.0	
I_{D-}	I_{10}			3.0	4.0		3.0	5.0	
P_D	DC power dissipation			33			33		mW

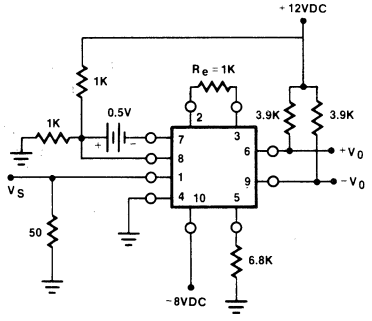
NOTE

Pin number references pertain to K package pinout only.

CARRIER REJECTION AND SUPPRESSION



SIGNAL GAIN AND OUTPUT SWING



AC ELECTRICAL CHARACTERISTICS

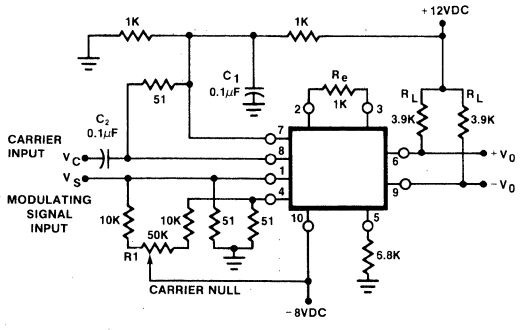
$V^+ = +12Vdc$, $V^- = -9.0Vdc$, $I_5 = 1.0mAdc$, $R_L = 3.9k\Omega$, $R_e = 1.0k\Omega$, $T_A = +25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	MC1596			MC1496/5596			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CFT}	Carrier feedthrough	V_c = 60mVrms sinewave and offset adjusted to zero							
		f_C = 1.0kHz		40			40		μVrms
		f_C = 10MHz		140			140		
		V_c = 300mVp-p squarewave:							
		Offset adjusted to zero f_C = 1.0kHz		0.04	0.2		0.04	0.4	mVrms
		Offset not adjusted f_C = 1.0kHz		20	100		20	200	
V_{CS}	Carrier suppressions	f_S = 10kHz, 300mVrms sinewave							
		f_C = 500kHz, 60mVrms sinewave	50	65		40	65		dB
		f_C = 10MHz, 60mVrms sinewave		50			50		
BW_{3dB}	Transadmittance bandwidth (Magnitude) (R_L = 50Ω)	Carrier input port, V_C = 60mVrms sinewave f_S = 1.0kHz, 300mVrms sinewave		300			300		MHz
		Signal input port, V_S = 300mVrms sinewave $\|V_C\|$ = 0.5Vdc		80			80		MHz
AV_S	Signal gain	V_S = 100mVrms; f = 1.0kHz $\|V_C\|$ = 0.5Vdc	2.5	3.5		2.5	3.5		V/V
CMV	Common-mode input swing	Signal port, f_s = 1.0kHz		5.0			5.0		Vp-p
ACM	Common-mode gain	Signal port, f_S = 1.0kHz $\|V_C\|$ = 0.5Vdc		-85			-85		dB
DV_{OUT}	Differential output voltage swing capability			8.0			8.0		Vp-p

NOTE

Pin number references pertain to K package pinout only.

CARRIER REJECTION AND SUPPRESSION



NE546-N

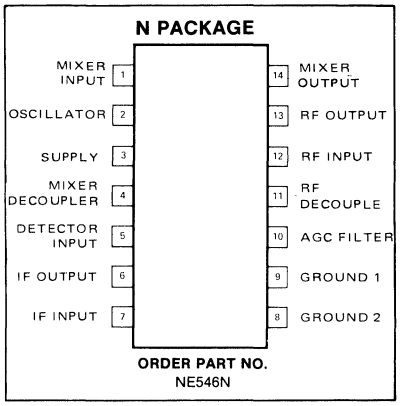
DESCRIPTION

The NE546 is a monolithic integrated circuit that provides an RF amplifier, IF amplifier, mixer, oscillator, AGC detector, and voltage regulator in a single IC. The primary application is super heterodyne AM radio receiver particularly in automobile radios. The NE546 is available in a 14 lead dual inline package.

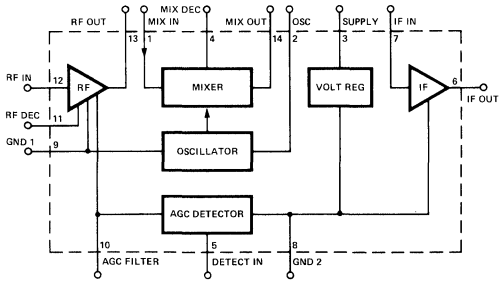
FEATURES

- **Low noise**
- **Build in AGC circuit**
- **Separately accessable amplifiers**
- **Mixer-oscillator stage with internal feedback**
- **High selectivity**
- **High image rejection**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

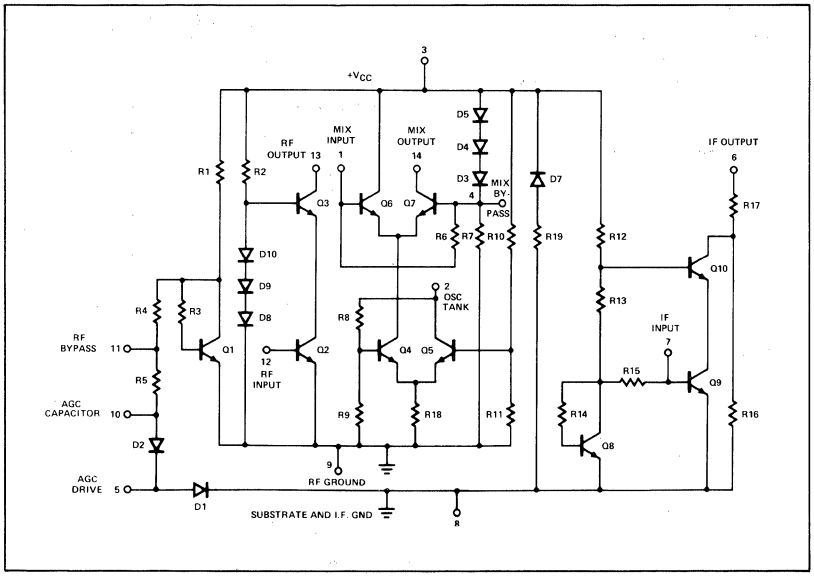
PARAMETER		RATING	UNIT
V_{CC}	Supply voltage pins 3, 13, 14 at pin 6	16	V
DC	Supply voltage (V+)	40	V
DC	Supply current	35	mA
	Internal power dissipation*	750	mW
	Lead temperature	300	°C
	Operating temperature range	-40 to +85	°C
	Storage temperature range	-65 to +150	°C

*NOTE

Rating applies for temperatures up to 55°C.
Derate linearly at 6.67nW/°C above 55°C.

13

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	NE546			UNIT
			Min	Typ	Max	
DC VOLTAGE						
$+V_{CC}$	Supply voltage		9.0		15.0	
$V_{OS}(V_1-V_4)$	Mixer balance			1.0		mV
V_3	Zener voltage: at terminal 5		5.5	6.0	7.0	V
V_5	AGC voltage		0.1	0.25	0.4	V
V_7	Pin 7 voltage		0.55	0.70	0.80	V
V_{12}	Pin 12 voltage		0.6	0.71	0.8	V
V_{13}	Pin 13 voltage			4.0		V
DC CURRENT						
I_{CC}	Supply current		15	18	22	mA
I_2	Oscillator current			1.0		mA
I_3	Zener current		12	14	16	mA
I_6	IF current		3.5	4.3	6	mA
I_{13}	RF current			4.0	5	mA
I_{14}	Mixer current			0.17	0.38	mA
STATIC						
V_6	I.F. breakdown and linearity	Apply 5 volts to pin 6 only. V_{CC} = 0 volts. Measure pin 6.	400	500	600	μA
V_6	I.F. breakdown and linearity	Apply 25 volts to pin 6 only. V_{CC} = 0 volts. Measure pin 6.*	2.0	2.5	3.0	mA

AC ELECTRICAL CHARACTERISTICS

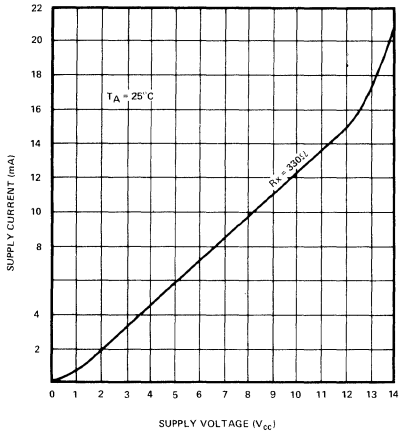
PARAMETER		TEST CONDITIONS	NE546			UNIT
			Min	Typ	Max	
V_{sat}	Saturation	Per sensitivity test interrupting input signal measure output voltage.	500			mV
V_{sen}	Sensitivity	Input signal to dummy antenna at f_{IN} = 1MHz, 30% AM modulation at f_{MOD} = 400Hz, for 11mV output at V_0.		2.5	5	μA
S/N	Signal-to-noise ratio	Ratio of output at V_0 with modulation ON and then OFF, input signal = 100μV, 30% AM modulation at f_{MOD} = 400Hz.	34			dB
Dist.	Overload distortion	Input signal set at 1MHz, 90% AM modulation, distortion at V_0 must be 10%.	100	155	250	mV

NOTE

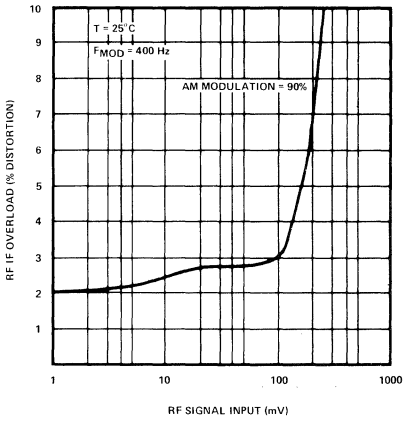
Performance characteristics in circuit of Figure 3.

TYPICAL PERFORMANCE CHARACTERISTICS

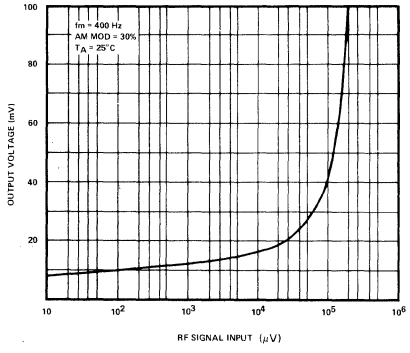
I_{CC} vs V_{CC}



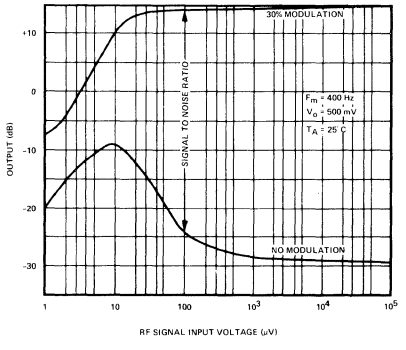
OVERLOAD RESPONSE DISTORTION vs RF INPUT



AGC CURVE



SIGNAL TO NOISE RATIO

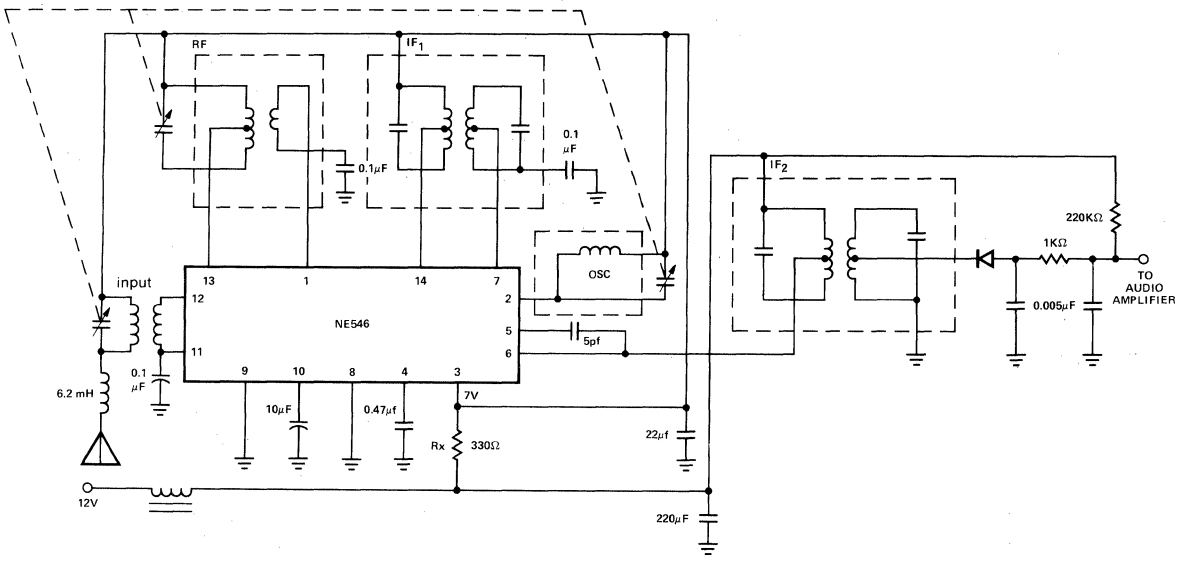


NOTE

Rx is external resistor between pins 3 and V supply.

TYPICAL APPLICATIONS

AM RADIO (Capacitor Tuned)



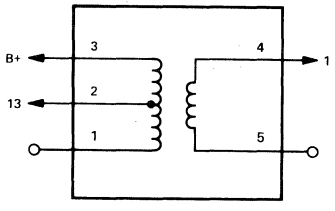
VARIABLE CAPACITOR (Air Varicon)

ANT & RF	13pF ~ 190pF
OSC	12pF ~ 80pF

ANTENNA COIL

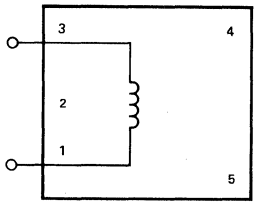
10mm ϕ < 120mm Ferrite Antenna

RF COIL



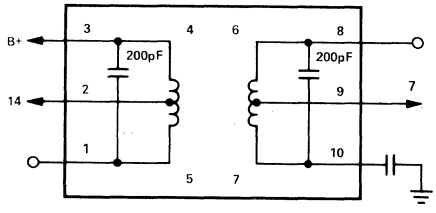
1–2 44 Turns
2–3 81 Turns
4–5 8 Turns

OSC COIL



1–3 95 Turns

1st. IF COIL



2nd. IF COIL

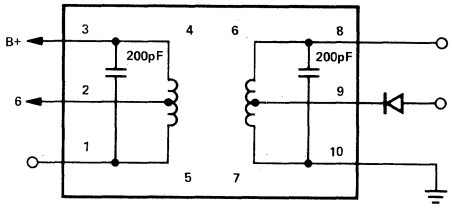


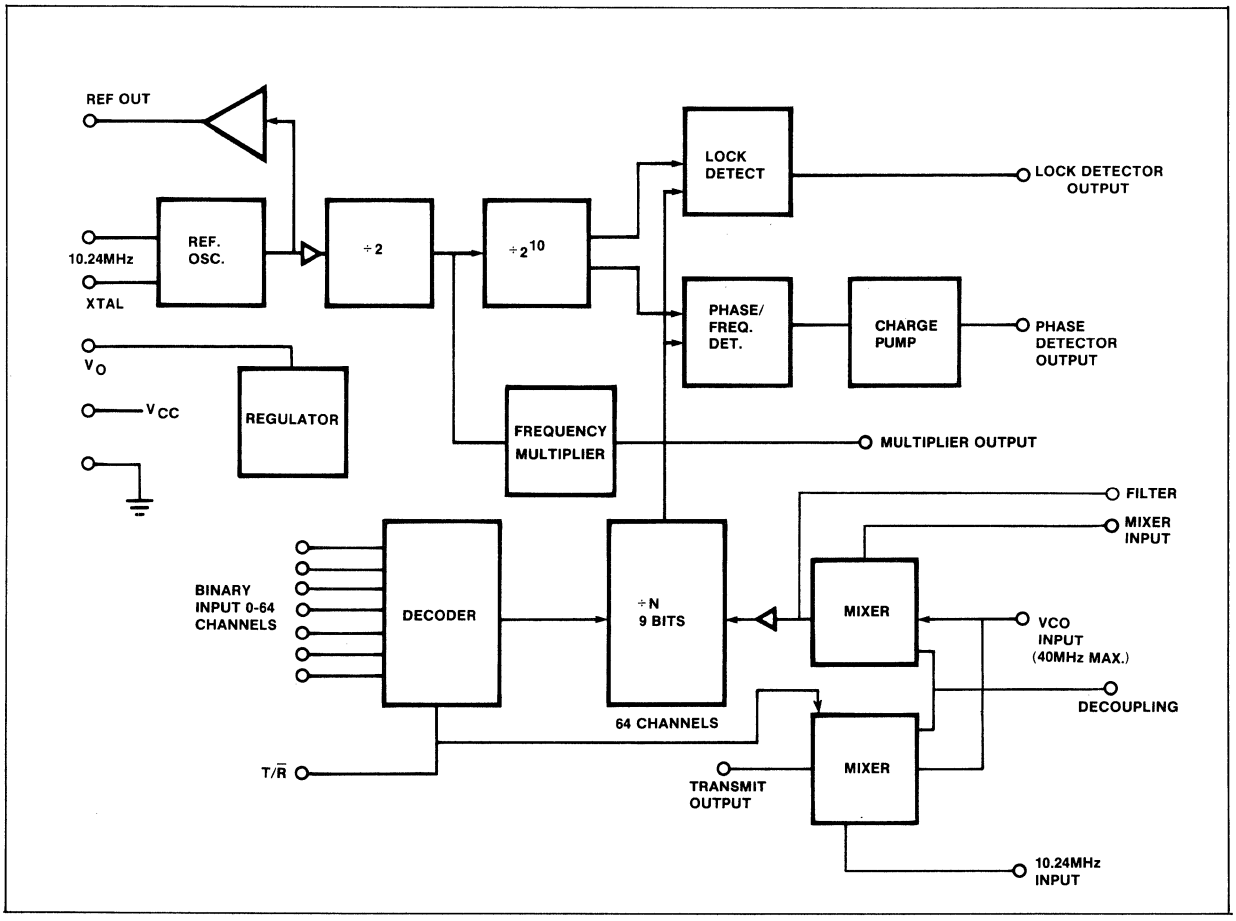
Figure 1

OBJECTIVE SPECIFICATION

FEATURES

- **Single crystal (10.24MHz)**
- **Generates both receive L.O.'s for dual conversion plus transmit frequency**
- **Binary input**
- **ROM programmed**
- **Up to 64 channel capability**
- **High or low side L.O. injection**
- **Wide supply range: 8V → 16V**
- **Single line T/R programming**
- **Regulated 5 volt output (10mA)**
- **Internal transmit squelch**

BLOCK DIAGRAM

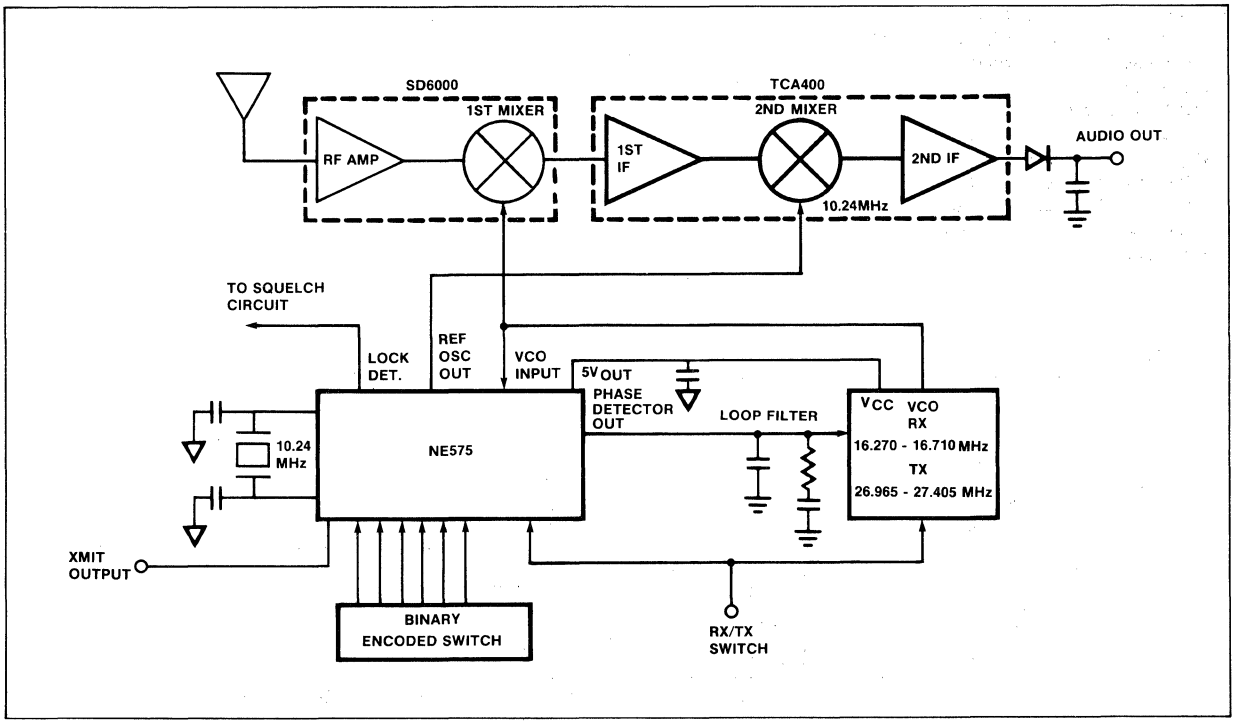


ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Power supply	16	V
Max. VCO input frequency	40	MHz
Reference frequency	10.24	MHz
Logic input current	1	μA

OBJECTIVE SPECIFICATION

TYPICAL APPLICATION



TCA 440-N

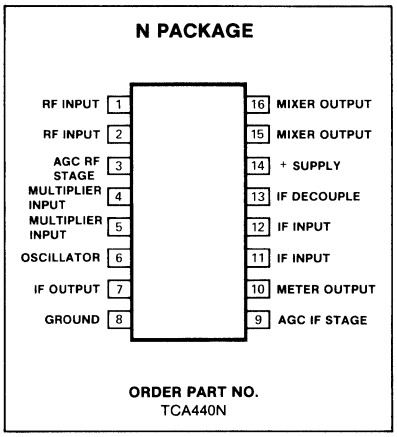
DESCRIPTION

TCA440 is a monolithic IC, especially developed for AM receivers up to 50MHz. It includes a RF stage with AGC, a balanced mixer, separate oscillator and an IF amplifier with AGC. Because of its low current consumption and of its internal stabilization the TCA440 is perfectly suited for battery operated portables, car and home radios.

FEATURES

- **Balanced circuit**
- **Separately controllable prestage**
- **Multiplicative push-pull mixer with separate oscillator**
- **High signal handling capability even with 4.5V supply voltage**
- **100dB feedback control range in 5 stages**
- **Direct connection for tuning meter**
- **Minimum external components**

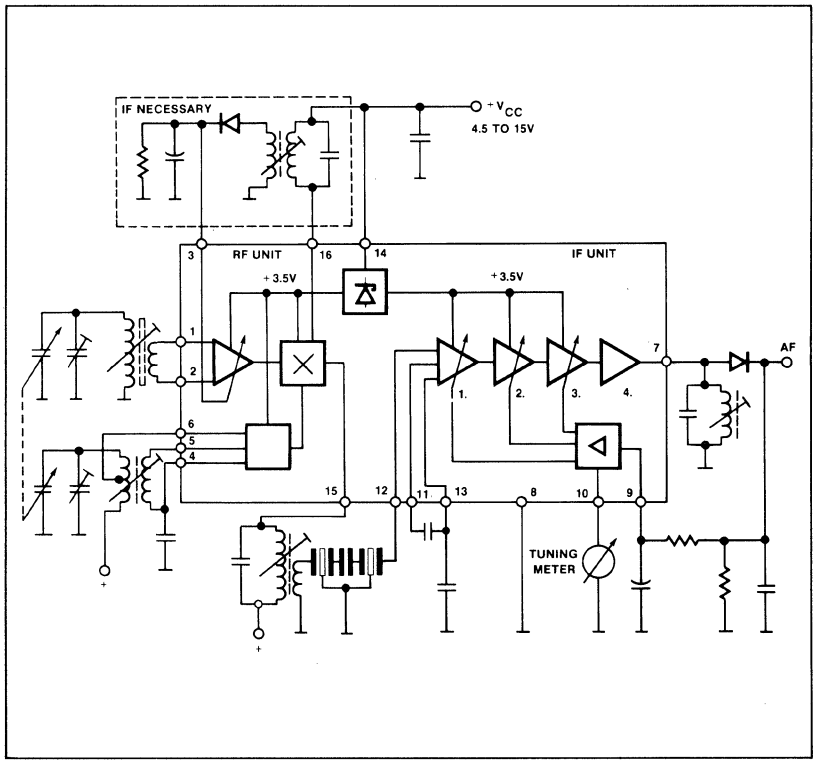
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	15	V
T_{amb}	Ambient temperature in operation	-15 to +80	°C
T_s	Storage temperature	-30 to +125	°C
V_{CC}	Range of operation	4.5 to 15	V

BLOCK DIAGRAM



TUNING METER

Recommended instruments:

or $500\mu A$ ($R_1 = 800k\Omega$)
$300\mu A$ ($R_1 = 1.5k\Omega$)

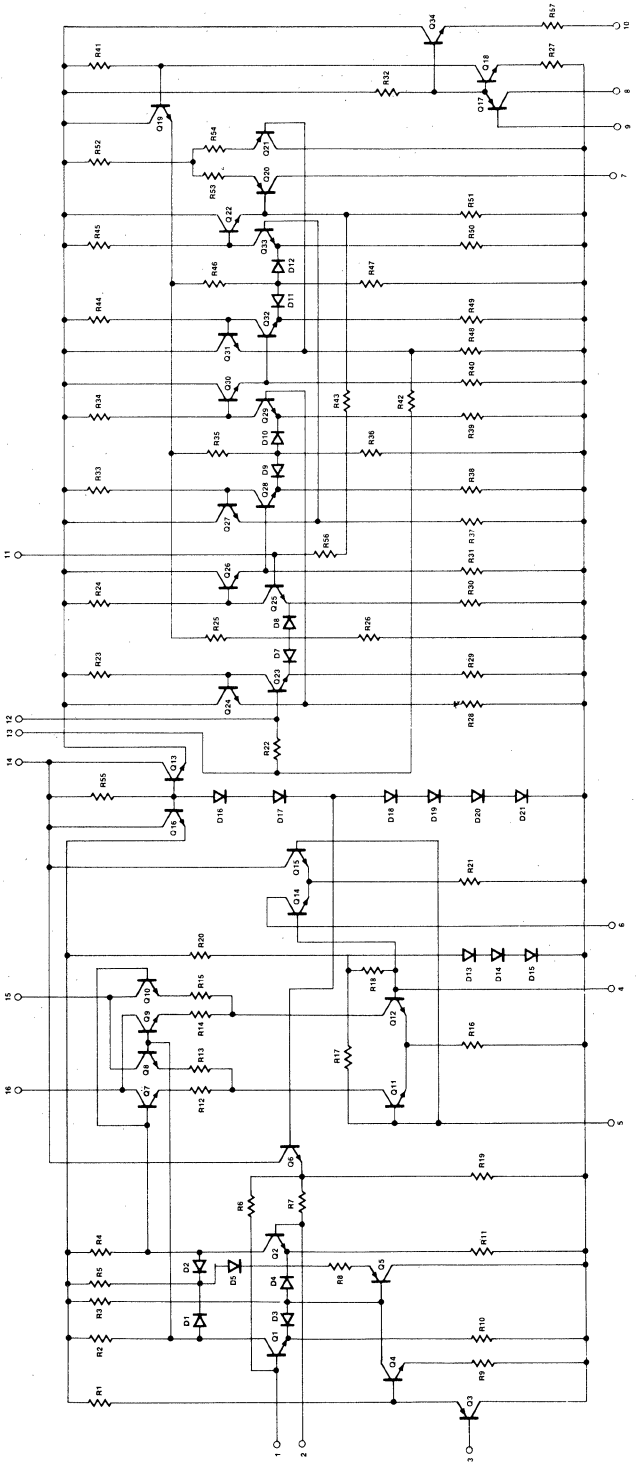
The IC offers at pin 10 a tuning meter voltage of 600 mV_{EMP} max. with a source impedance of approx. 400Ω.

FUNCTION

As pictured in the circuit diagram the TCA440 comprises two control loops independent of each other which control the RF stage and the IF stages. By AGCing the RF stage, excellent signal handling is obtained. A voltage of $2.6V_{pp}$ on the IC input can be handled with very low distortion. The push-pull mixer operates multiplicatively, thereby resulting in few harmonic mixing products and whistling points. The oscillator which is separated from the mixer is also apted excellently for short waves. From the AGC of the RF amplifier a voltage is derived for a tuning meter which can be connected directly to the meter. The symmetric composition of the circuit provides high stability against oscillation and, at the same time, an AGC range of more than 100dB. The bridge circuit of the mixer provides good isolation of the oscillator.

TCA 440-N

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS

V_{CC} = 9V, T_A = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	TCA 440			UNIT
			Min	Typ	Max	
I_{CC}	Total current consumption at:	V_{CC} = 4.5V		7		mA
		V_{CC} = 9V		10.5		mA
		V_{CC} = 15V		12		mA

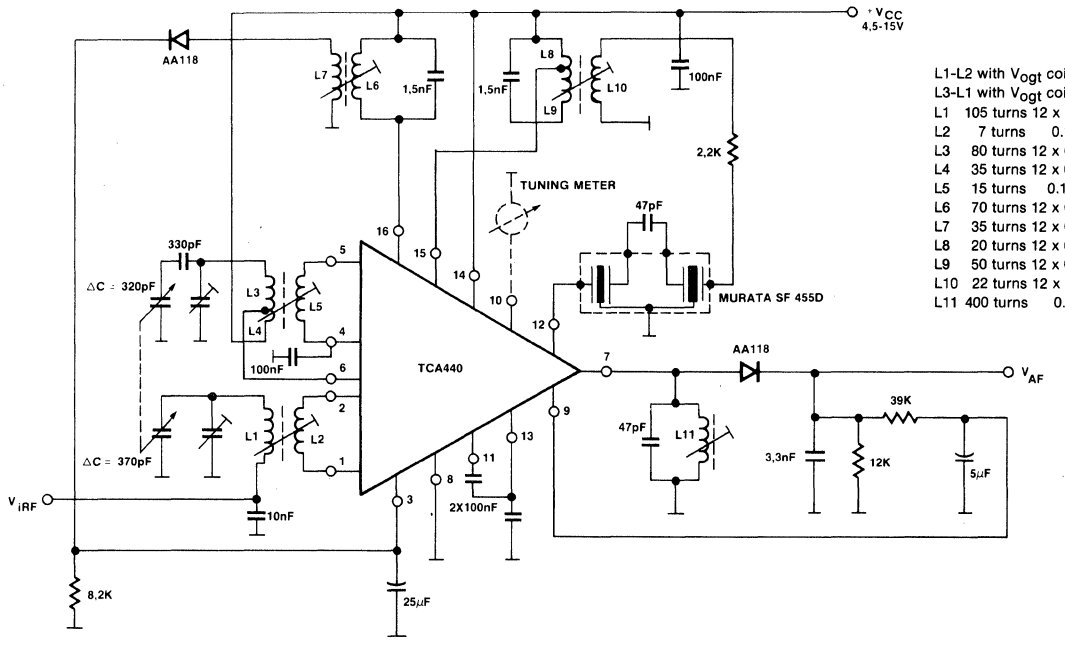
AC ELECTRICAL CHARACTERISTICS

V_{CC} = 9V, T_A = 25°C, f_{IRF} = 600kHz, fmod = 1kHx unless otherwise specified.

PARAMETER		TEST CONDITIONS	TCA 440			UNIT
			Min	Typ	Max	
ΔG_{RF}	RF level deviation for (m = 80%)	ΔV_{AF} = 6dB		65		dB
		ΔV_{AF} = 10dB		80		dB
V_{AFeff}	AF output voltage for V_{IRF} (symm. measured at 1-2)	m = 80% V_{IRF} = 20μV		140		mV
		V_{IRF} = 1mV		260		
		V_{IRF} = 500mV		350		
		m = 30% V_{IRF} = 20μV		50		mV
		V_{IRF} = 1mV		100		
		V_{IRF} = 500mV		130		
V_{IRF}	Input sensitivity (measured at 60Ω, f_{IRF} = 1MHz, m = 30%/0%, R_G = 540Ω)	At signal-to-noise distance				
		$\frac{S+N}{N}$ = 6dB		1		μV
		$\frac{S+N}{N}$ = 26dB		7		μV
		$\frac{S+N}{N}$ = 58dB		1		mV
RF unit						
f_{IRF}	Input frequency range			0 to 50		MHz
f_{IF}	Output frequency	$f_{IF} = f_{OSC} - f_{IRF}$		460		kHz
ΔG_V	Control range			38		dB
V_{IRFpp}	Input voltage	for 600kHz, m = 80%, for Overdrive, k_{AF} = 10%, Symmetrically measured at pins 1 & 2 (mean carrier value)		2.6		Vpp
V_{IRFeff}				.5		V
s_{IF}	IF suppression between 1-2 to 15			20		dB
Z_I	RF input impedance	Asymmetrical coupling at:				
		G_{RFmax}		2/5		kΩ/pF
		G_{RFmin}		2.2/1.5		kΩ/pF
		Symmetrical coupling at:				
		G_{RFmax}		4/5		kΩ/pF
		G_{RFmin}		4.5/1.5		kΩ/pF
Z_{gosc}	Mixer output impedance	Pins 15 or 16		250/4.5		kΩ/pF
IF unit						
f_{IIF}	Input frequency range			0 to 2		MHz
ΔG_V	Control range at 460kHz			62		dB
V_{IFeff}	Input voltage	Mean carrier value at G_{min} for Overdrive (k_{AF} = 10%), measured at Pin 12 (60Ω to ground, f_{IF} = 460kHz, m = 80%, f_{mod} = 1kHz)		200		mV
V_{AFeff}	AF output voltage	V_{IIF} at 60Ω (Pin 12) f_{mod} = 1kHz				
		V_{IF} = 30μV, m = 80%		50		mV
		V_{IF} = 3mV, m = 80%		200		mV
		V_{IF} = 3mV, m = 30%		70		mV
Z_I	IF input impedance	Asymmetrical coupling		3/3		kΩ/pF
Z_g	IF output impedance	Pin 7		200/8		kΩ/pF

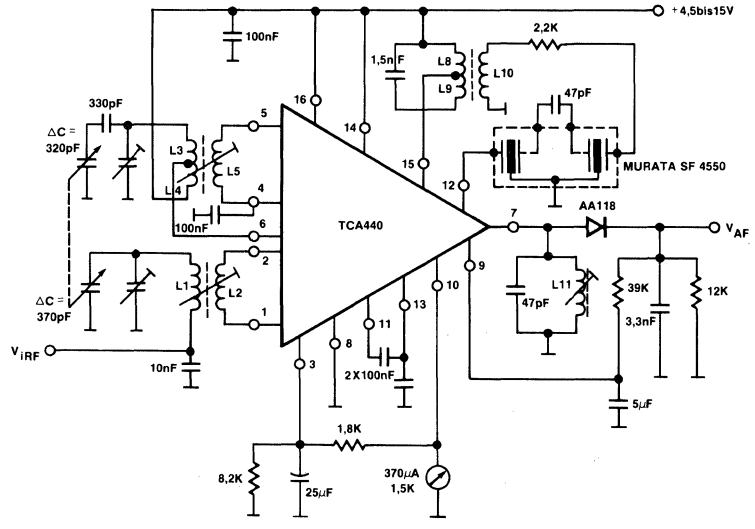
TYPICAL APPLICATIONS

APPLICATION EXAMPLE FOR MW



L1-L2 with V_{ogt} coil set D21-2375.1
L3-L1 with V_{ogt} coil set D41-2519
L1 105 turns 12 x 0.04 CuLS
L2 7 turns 0.10 CuL
L3 80 turns 12 x 0.04 CuLS
L4 35 turns 12 x 0.04 CuLS
L5 15 turns 0.10 CuL
L6 70 turns 12 x 0.04 CuLS
L7 35 turns 12 x 0.04 CuLS
L8 20 turns 12 x 0.04 CuLS
L9 50 turns 12 x 0.04 CuLS
L10 22 turns 12 x 0.04 CuLS
L11 400 turns 0.06 CuL

APPLICATION EXAMPLE FOR MW

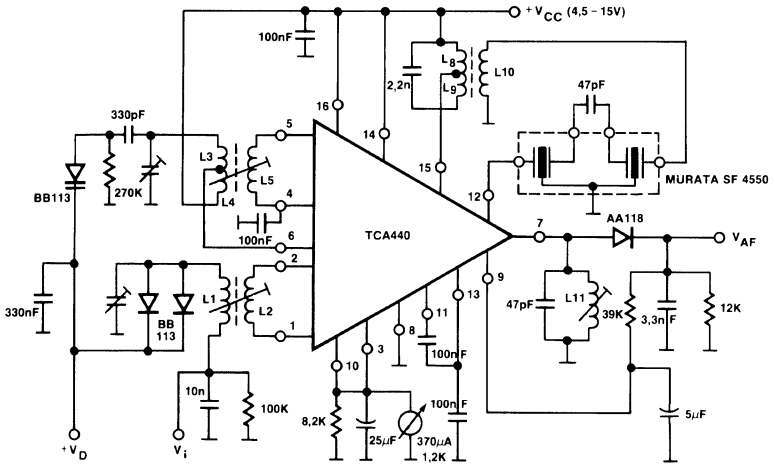


Prestage control is derived from IF control

L1 105 turns 12 x 0.04 CuLS
L2 7 turns 0.10 CuL
L3 80 turns 12 x 0.04 CuLS
L4 35 turns 12 x 0.04 CuLS
L5 15 turns 0.10 CuL
L8 20 turns 12 x 0.04 CuLS
L9 50 turns 12 x 0.04 CuLS
L10 22 turns 12 x 0.04 CuLS
L11 400 turns 0.04 CuL
L1-L2 with V_{ogt} coil set D21-23751
L3-L11 with V_{ogt} coil set D41-2519

TYPICAL APPLICATIONS (Cont'd)

APPLICATION EXAMPLE FOR AM USING VARICAP DIODES BB 113

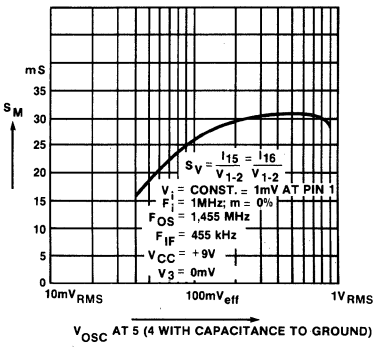


L1 105 turns 12 x 0.04 CuLS
L2 7 turns 0.10 CuL
L3 80 turns 12 x 0.04 CuLS
L4 35 turns 12 x 0.04 CuLS
L5 15 turns 0.10 CuL
L8 20 turns 12 x 0.04 CuLS
L9 50 turns 12 x 0.04 CuLS
L10 22 turns 12 x 0.04 CuLS
L11 400 turns 0.06 CuL

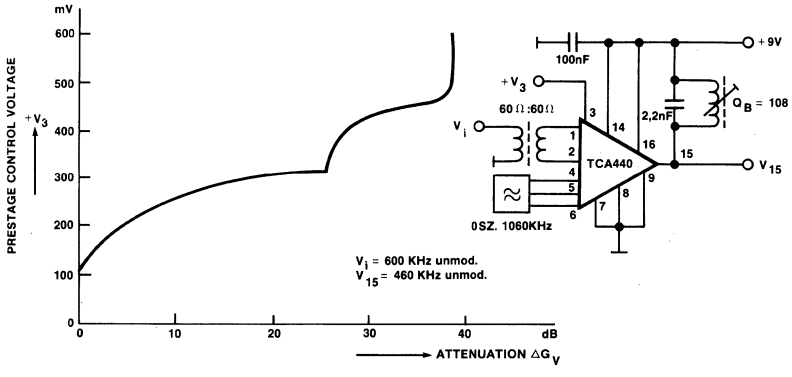
L1-L2 with Vogt coil set D21-23751
L3-L11 with Vogt coil set D41-2519

V_D = 8.5V→f_i = 800kHz
V_D = 30V→f_i = 1620kHz

CONVERSION CONDUCTANCE vs OSCILLATOR VOLTAGE



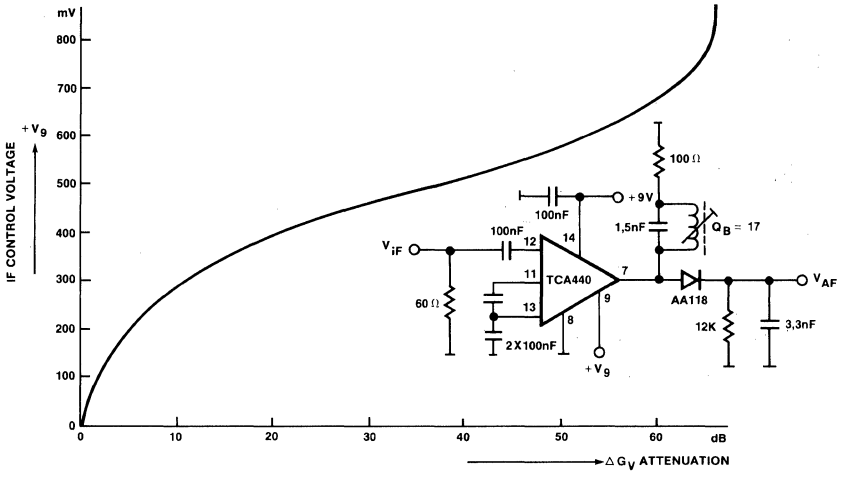
RF STAGE CONTROL



The input is not power matched and can be driven with a higher resistance, V_i is chosen so that a constant V_{15} is obtained ($50mV_{pp}$).

TYPICAL APPLICATIONS (Cont'd)

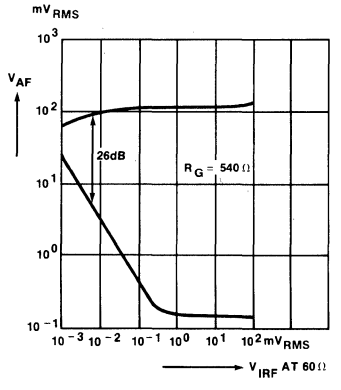
IF CONTROL



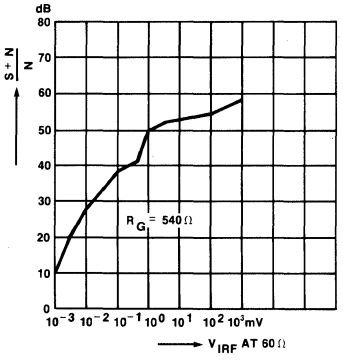
V_{IF} (469kHz; m = 80%; f_{mod} = 1kHz) is chosen so that always a constant V_{AF} is obtained ($200mV_{RMS}$)

TYPICAL PERFORMANCE CHARACTERISTICS

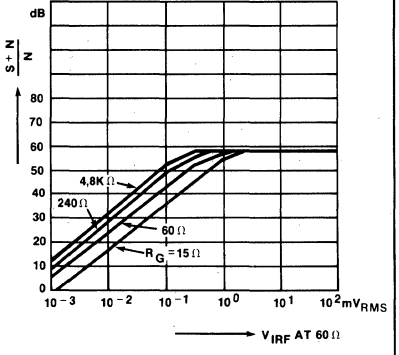
AF OUTPUT VOLTAGE AND NOISE FIGURE vs RF INPUT VOLTAGE (switching position 1)



SIGNAL TO NOISE DISTANCE vs RF INPUT VOLTAGE (switching position 2)

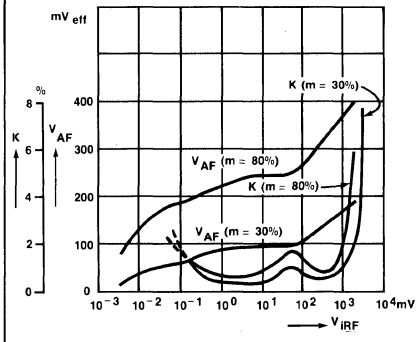


SIGNAL TO NOISE DISTANCE vs RF INPUT VOLTAGE (parameter is generator impedance) (switching position 1)

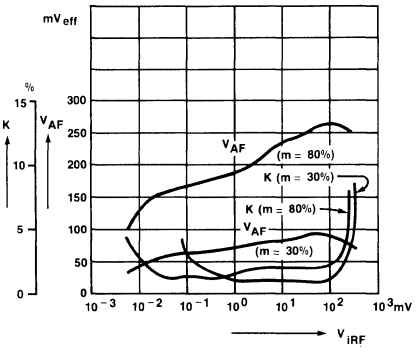


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

TEST FIGURES FOR APPLICATION EXAMPLE FOR MW HARMONIC DISTORTION AND AF OUTPUT VOLTAGE vs RF INPUT VOLTAGE MEASURED SYMMETRICALLY AT PINS 1 AND 2 f_i = 1MHz, f_{mod} = 1kHz, f_{IF} = 455kHz, V_{cc} = 9V



TEST FIGURES FOR APPLICATION EXAMPLE FOR AM USING BB 113 f_i = 1MHz, f_{mod} = 1kHz, f_{IF} = 455 kHz, V_{cc} = 9V, V_{IRF} measured symmetrically at pins 1 and 2

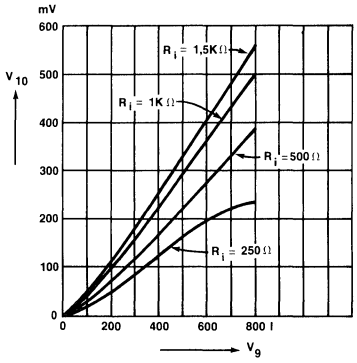


Example for moving coil instruments

R_i for full-scale deflection

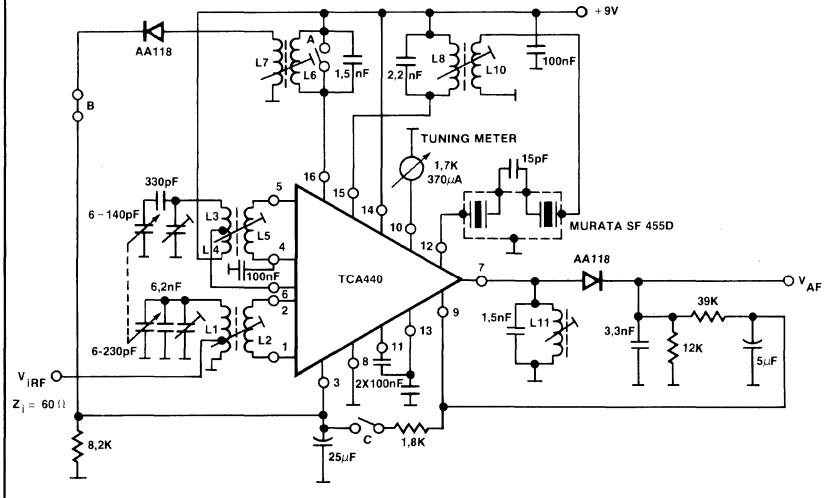
1.5kΩ	100μA
1.5kΩ	170μA
2kΩ	200μA
350Ω	500μA

TUNING METER VOLTAGE vs IF CONTROL VOLTAGE (parameter is impedance of tuning meter)



TEST CIRCUITS

TEST CIRCUIT FOR NOISE FIGURE



L1-L2 M25 pot core
L3-L11 with Vogt coil set D41-2519

L1	2 + 6	turns	6 x 12 x 0.04 CuLS
L2	n		0.15 CuL
L3	90	turns	12 x 0.04 CuLS
L4	35	turns	12 x 0.04 CuLS
L5	15	turns	0.10 CuL
L6	70	turns	12 x 0.04 CuLS
L7	35	turns	12 x 0.04 CuLS
L8	60	turns	12 x 0.04 CuLS
L10	22	turns	12 x 0.04 CuLS
L11	68	turns	0.06 CuL

switch A	switch B	switch C	
off	on	off	separate RF stage control
on	off	on	RF stage control voltage derived from IF control voltage

f_i = 1MHz; m = 30%

n(turns)	$R_{Generator}(\Omega)$
1	15
2	60
4	240
6	540
9	1,2K
12	2,2K
18	4,8K

μA758-N

DESCRIPTION

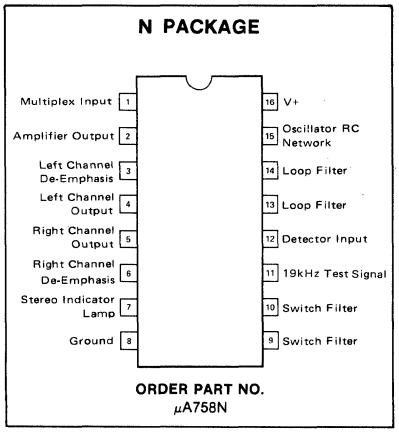
The μA758 is a monolithic phase-locked loop FM stereo multiplex decoder. The device decodes an FM stereo multiplex signal into right and left audio channels while inherently suppressing SCA information when it is contained in the composite input signal. The device includes automatic mono-stereo mode switching and drive for an external lamp to indicate stereo mode operation.

The μA758 operates over a large voltage range and requires a minimum number of external components. A simple setting of an external potentiometer adjusts the oscillator frequency. No coils are required.

FEATURES

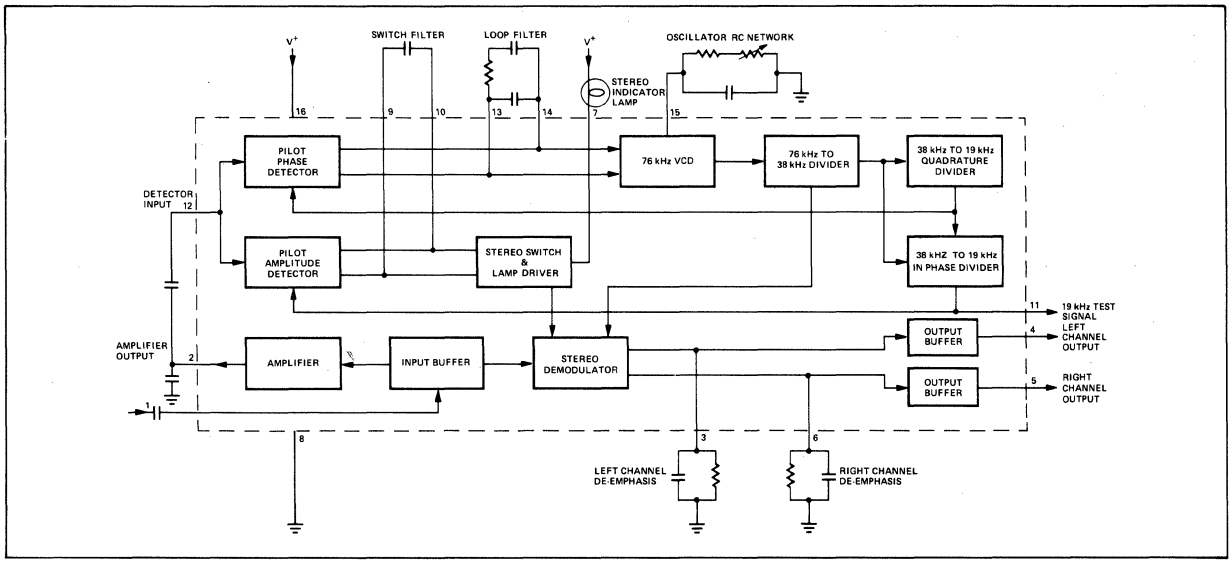
- **45dB channel separation**
- **Automatic stereo/mono switching**
- **70dB SCA rejection**
- **10V to 16V supply range**
- **High impedance input—low impedance output**

PIN CONFIGURATION



ORDER PART NO.
μA758N

BLOCK DIAGRAM

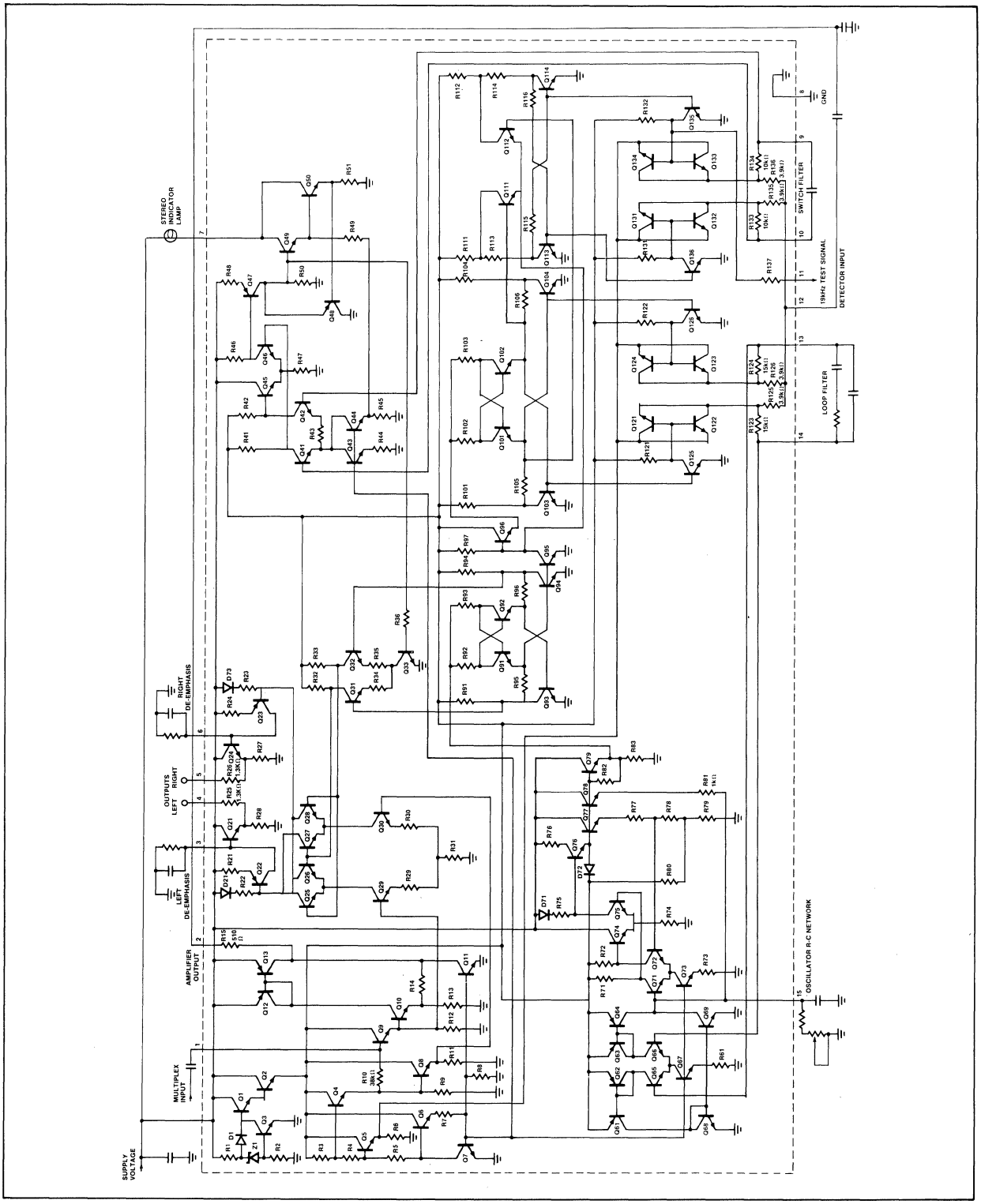


ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+18	V
Supply voltage (≤ 15 seconds)	+22	V
Voltage at lamp driver terminal (Lamp OFF)	+22	V
Internal power dissipation	730	mW
Operating temperature range	-40 to +85	°C
Storage temperature range	-55 to +125	°C
Lead temperature (60sec)	300	°C

μA758-N

EQUIVALENT SCHEMATIC



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μA758-N

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V+ = +12V, 19kHz pilot level = 30mV$_{RMS}$, multiplex signal (L = R, pilot OFF) = 300mV$_{RMS}$, modulation frequency = 400Hz or 1Hz, test circuit 1, unless otherwise specified.

PARAMETER		TEST CONDITIONS	μA758			UNIT
			Min	Typ	Max	
I_{CC}	Supply current	Lamp OFF		26	35	mA
I_L	Maximum available lamp current		75	150		mA
V_7	Voltage at lamp driver terminal	Lamp = 50mA		1.3	1.8	V
r_i	Input resistance		20	35		kΩ
r_o	Output resistance		0.9	1.3	2.0	kΩ

AC ELECTRICAL CHARACTERISTICS

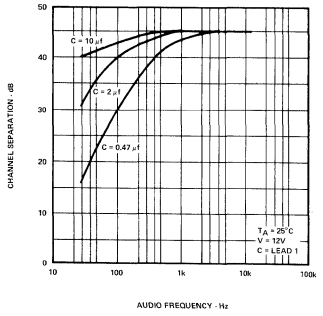
PARAMETER		TEST CONDITIONS	μA758			UNIT
			Min	Typ	Max	
$\Delta(V_4\&V_5)$	DC voltage shift at either output terminal	Stereo to mono operation		30	150	mV
$P_{S.R.R.}$	Power supply ripple rejection	200Hz, 200mV$_{RMS}$	35			dB
SEP	Channel separation	100Hz		40		dB
		400Hz	30	45		dB
		10kHz		45		dB
BAL.	Channel balance			0.3	1.5	dB
A_V	Voltage gain	1kHz	0.5	0.9	1.4	V/V
	Pilot input level	Lamp turn-on		15	22	mV$_{RMS}$
		Lamp turn-off	2.0	7.0		mV$_{RMS}$
	Pilot input level hysteresis	Lamp turn-off to turn-on	3.0	7.0		dB
	Capture range		2.0	4.0	6.0	%
T.H.D.	Total harmonic distortion	Multiplex level = 600mV$_{RMS}$ pilot OFF		0.4	1.0	%
	19kHz rejection		25	35		dB
	38kHz rejection		25	45		dB
	SCA rejection[1]			70		dB
VCO	Tuning resistance[2]		21.0	23.3	25.5	kΩ
VCO	Frequency drift	0°C ≤ T_A ≤ 25°C		+0.1	±2	%
		25°C ≤ T_A ≤ 70°C		-0.4	±2	%

NOTES

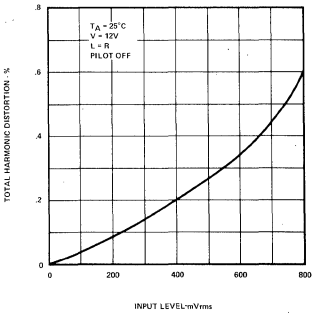
1. Measured with a stereo composite signal consistency of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules on Broadcasting.
2. Total resistance from pin 15 to ground, in test circuit, required to set reference frequency at pin 11 to 19kHz ± 10hz.

TYPICAL PERFORMANCE CHARACTERISTICS

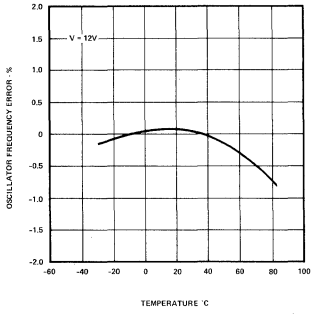
CHANNEL SEPARATION vs AUDIO FREQUENCY



HARMONIC DISTORTION vs INPUT LEVEL

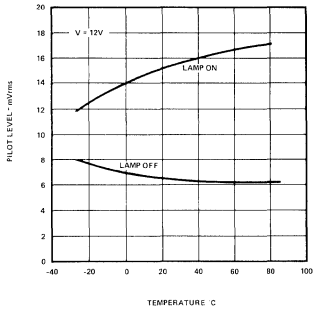


OSCILLATOR FREE RUNNING FREQUENCY ERROR vs AMBIENT TEMPERATURE

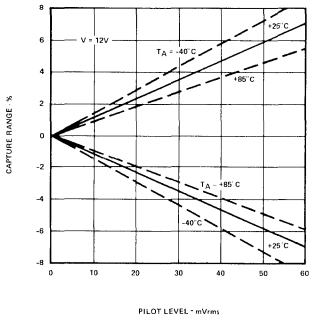


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

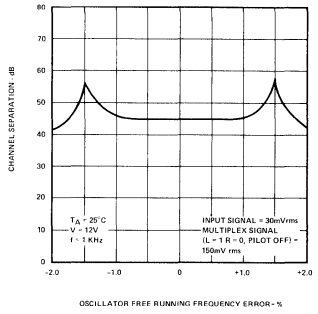
LAMP TURN ON & TURN OFF SENSITIVITY vs AMBIENT TEMPERATURE



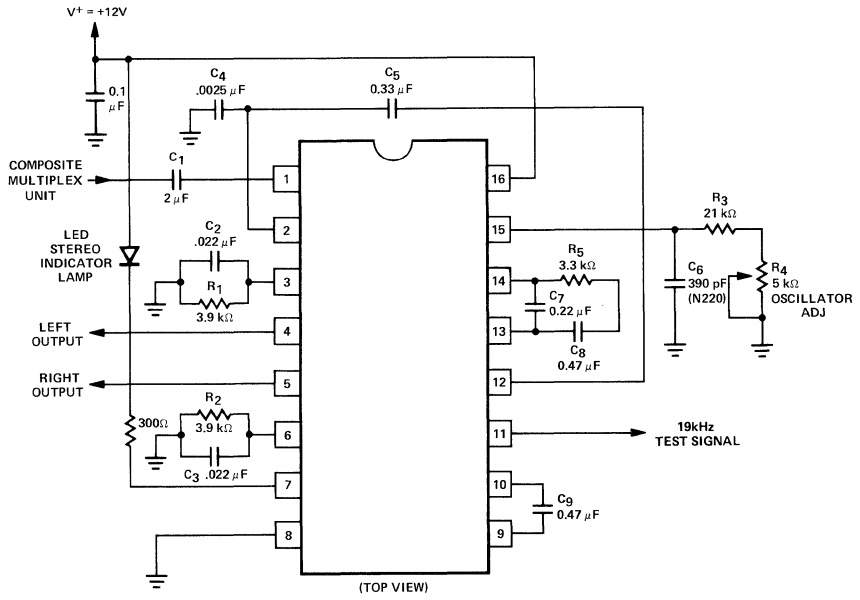
CAPTURE RANGES vs PILOT LEVEL



CHANNEL SEPARATION vs OSCILLATOR FREE RUNNING FREQUENCY ERROR



TEST CIRCUIT AND TYPICAL APPLICATION



NOTE

Tolerance on resistors is ±5% and tolerance on capacitors is ±20% unless otherwise specified. C_1 tolerance = +100%; -20%, C_6 tolerance = ±1% in test circuit and ±5% in typical applications, R_3 tolerance = ±1%, R_4 tolerance = ±10%, R_1 and R_2 tolerances = ±1% in test circuit and ±5% in typical application.

SECTION 14
TV CIRCUITS

MC1327-N

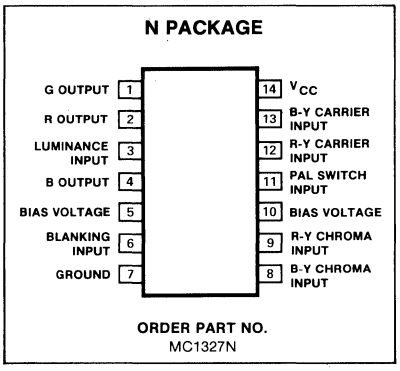
DESCRIPTION

Dual doubly balanced chroma demodulator with RGB matrix, PAL switch, and chroma driver stages. A monolithic device designed for use in solid-state color television receivers.

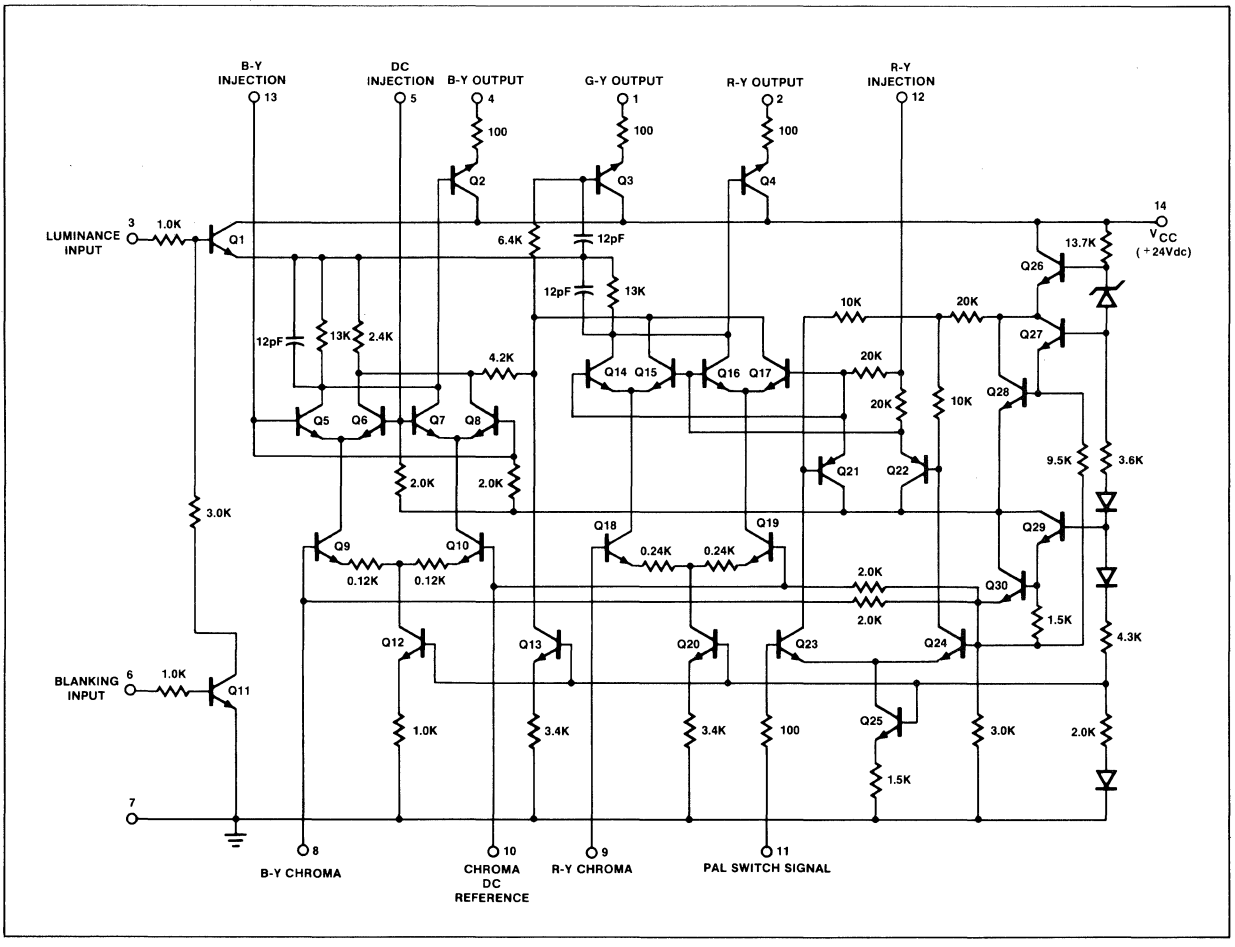
FEATURES

- **Good chroma sensitivity—0.28Vp-p input typical for 5.0Vp-p output**
- **Low differential output dc offset voltage—0.6V maximum**
- **Differential dc temperature stability—0.7mV/°C**
- **High blue output voltage swing—10Vp-p typical**
- **Blanking input provided**
- **Luminance bandwidth greater than 5.0MHz**

PIN CONFIGURATION



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS T_A = +25°C unless otherwise specified.

PARAMETER	RATING	UNIT
Power supply voltage	30	Vdc
Chroma signal input voltage	5.0	Vpk
Reference signal input voltage	5.0	Vpk
Minimum load resistance	3.0	kohms
Luminance input voltage	12	V_{P-P}
Blanking input voltage	7.0	V_{P-P}
Power dissipation (package limitation)		
Plastic packages	625	mW
Derate above T_A = +25°C	5.0	mW/°C
Operating temperature range (ambient)	-20 to +75	°C
Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS T_A = +25°C, V_{CC} = 24Vdc, R_L = 3.3k unless otherwise specified.[1,2]

PARAMETER	TEST CONDITIONS	MC1327			UNIT
		Min	Typ	Max	
Quiescent output voltage[2]		13.2	14.5	15.8	Vdc
Quiescent input current from supply[2]					
	$R_L = \infty$		7.5		mA
	R_L = 3.3kΩ	16	19	26	mA
Reference input dc voltage[2]			6.2		Vdc
Chroma reference input dc voltage			3.4		Vdc
Differential output voltage[1,2]			0.3	0.6	Vdc
	Temperature coefficient (+25°C to +65°C)		0.7		mV/°C
Output voltage[1,2]	Temperature coefficient (+25°C to +65°C)		+0.5	±5.0	mV/°C

NOTES

1. Chroma input signal voltage = 0 and normal reference input signal voltage = 1.0Vp-p
2. Reference Figure 2

AC ELECTRICAL CHARACTERISTICS

T_A = +25°C, V_{CC} = 24Vdc, R_L = 3.3K, reference input voltage = 1.0Vp-p, unless otherwise specified.[1,2,3,4]

PARAMETER	TEST CONDITIONS	MC1327			UNIT
		Min	Typ	Max	
Blue output voltage swing[1,4] Chroma input voltage[2,4]	 B output = 5.0Vp-p	8.0	10 280	 550	Vp-p mVp-p
Luminance input resistance		100			kΩ
Luminance gain from pin 3 to outputs Differential luminance gain, RGB outputs	@ dc @ 5.0MHz, reference at 100kHz @ 5.0MHz		0.95 -1.8 0.3		dB dB dB
Blanking input resistance	1.0Vdc 0Vdc		1.1 75		kΩ kΩ
Detected output voltage (Adjust B output to 5.0Vp-p, luminance voltage = 23V)[4] PAL switch operating voltage range	G output R output 7.8kHz square wave	1.4 2.5 0.3	1.8 2.9	2.2 3.3 3.0	Vp-p Vp-p Vp-p
R-Y output dc offset with PAL switch operation				100	mVdc
Demodulator unbalance voltage	No chroma input voltage and normal reference signal input voltage		200	300	mVp-p
Residual carrier and harmonic output voltage	With input signal voltage, normal reference signal voltage and B output = 5.0Vp-p		0.6	1.0	Vp-p
Reference input resistance Reference input capacitance	Chroma input = 0 Chroma input = 0		2.0 6.0		KΩ pF
Chroma input resistance Chroma input capacitance			2.0 2.0		kΩ pF

NOTE
1. With normal reference input signal voltage, adjust chroma input signal voltage to 1.2Vp-p.
2. With normal reference input signal voltage, adjust chroma input signal voltage until the blue output voltage = 5.0Vp-p.
3. With normal reference input signal voltage, adjust chroma input signal voltage until the blue output voltage = 5.0Vp-p. At this point, the red and green voltages will fall within the specified limits.
4. Reference Figure 3.

TYPICAL APPLICATIONS

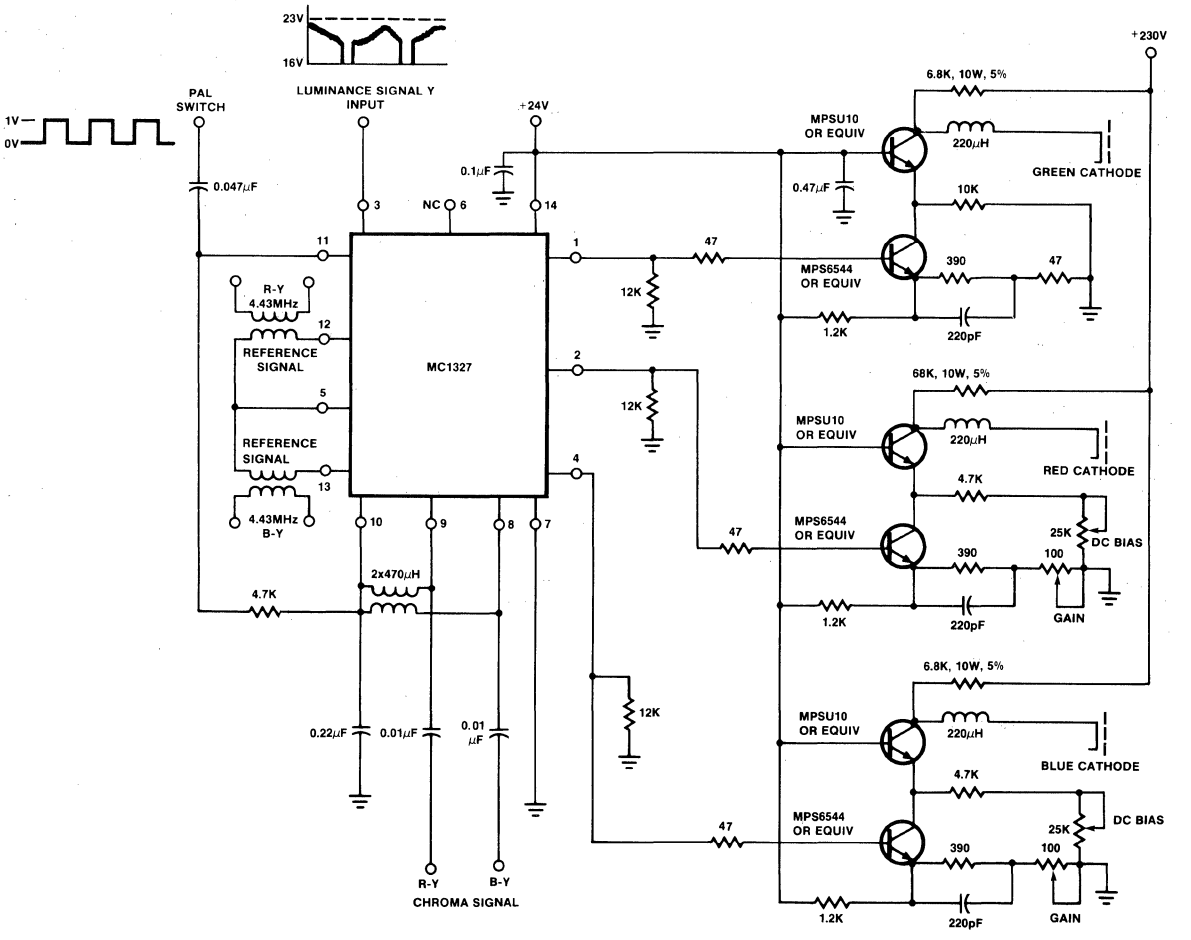
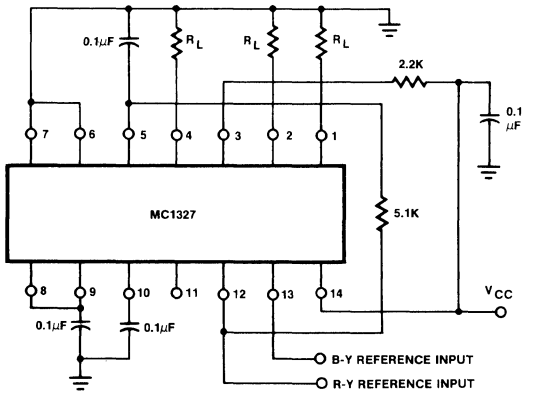


Figure 1

TEST CIRCUITS

DC OUTPUT VOLTAGE TEST CIRCUIT WITH NORMAL REFERENCE INPUT VOLTAGE (B, R, AND G)



(V_{CC} = 24Vdc, R_L = 3.3 kilohms, T_A = +25°C unless otherwise specified.)

Figure 2

DYNAMIC TEST CIRCUIT

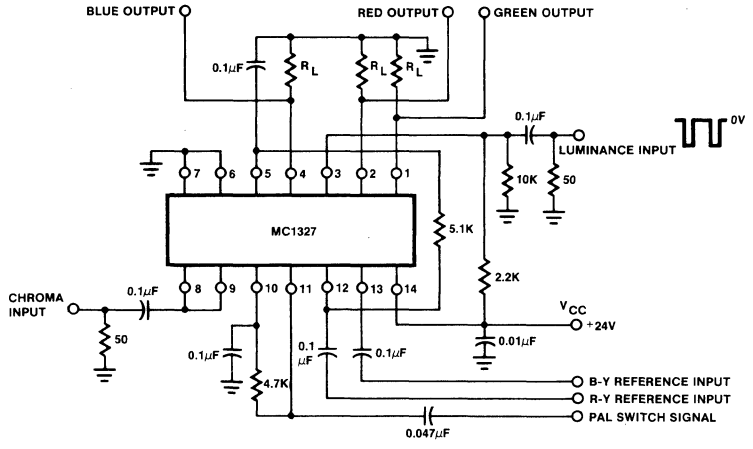


Figure 3

TBA/120S-N

DESCRIPTION

An eight stage amplifier with balanced demodulator for amplifying, limiting and the demodulation of FM signals, specially designed for the sound-IF in TV and RF-IF amplifier in radios. An electronic Volume Control for the audio outputsignal is also provided.

Groups:

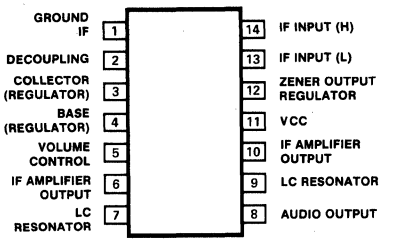
TBA 120 S is delivered in groups:
An attenuation of -30dB of the audio outputsignal requires a resistor from pin 5 to ground as indicated in the table.

Group	2	3	4	5
Value (kΩ)	1.9 to 2.2	2.1 to 2.5	2.4 to 2.9	2.8 to 3.3

For example, devices marked TBA120S-3 indicate group 3.

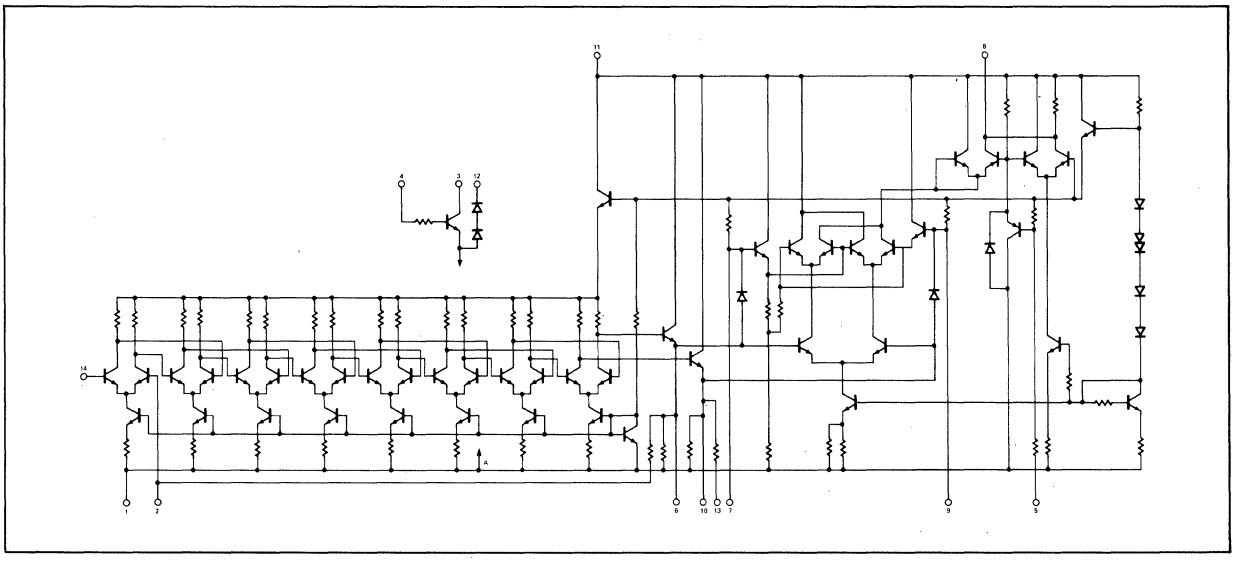
PIN CONFIGURATION

N PACKAGE



ORDER PART NO.
TBA120SN (DIP), TBA120ASN (QUAD-IN-LINE)

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	18	V
Operating temperature range	-15 to +70	°C
Storage temperature	-40 to +125	°C
Power dissipation	400	mW
max 1 minute	500	mW
Supply current	15	mA
max 1 minute	20	mA
Current 13	1	mA
14	1	mA
Operating supply voltage	6 to 18	V
Frequency range	0 to 12	MHz

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 12V; T_{amb} = 25°C)

PARAMETER		TEST CONDITIONS	TBA120S			UNIT
			Min	Typ	Max	
I_{CC}	Total current requirement	$R_5 = \infty$ $R_5 = 0$	10 12	14 16	18 20	mA mA
V_8 V_5	dc-portion of the output signal Voltage	$V_1 = 0$ -1dB down -70dB down		7.3 2.4 1.3	 2.6	V V V

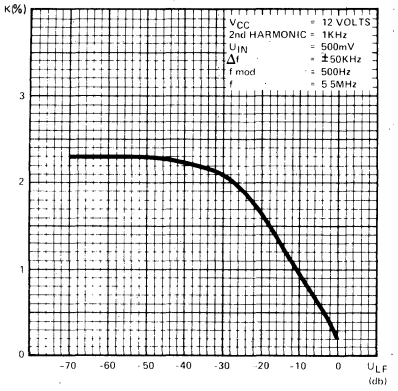
AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 12V unless otherwise specified.

PARAMETER		TEST CONDITIONS	TBA120S			UNIT
			Min	Typ	Max	
G_V	IF-voltage gain V_6/V_{14}	f = 5.5MHz		68		dB
V_{QPP}	IF-output voltage at limiting; each output			250		mV
V_{AFrms}	AF-output voltage	f = 5.5MHz; $\Delta f = \pm 50$kHz; V_I = 10mV; f_{mod} = 1kHz; Q = 45; k = 4% f = 5.5MHz; $\Delta f = \pm 50$kHz; V_I = 10mV; f_{mod} = 1kHz; Q = 20; k = 1%		1.1 0.55		V V
V_{lim}	Input voltage starting limiting	f = 5.5MHz; f = 50kHz; f_{mod} = 1kHz; Q = 45;		30	60	μV
Z_I R_Q	Input impedance Output resistance	f = 5.5MHz Pin 8	15/6	40/4.5 2.6		kΩ/pf kΩ
V_{AFmax} V_{AFmin} a_{AM}	Range of volume control AM-suppression	f = 5.5MHz; f = +50Hz; $V_I = 500\mu$V; f_{mod} = 1kHz; m = 30%	 45	70 55		dB dB
R_5	Potentiometer resistance	-1dB down -70dB down	 1.0	3.7 1.4	4.7	kΩ kΩ
CHARACTERISTICS OF THE AUXILIARY CIRCUIT						
V_{12} R_Z	Z-voltage Z-resistance	I_{12} = 5mA	11.2	12 30	13.2	V Ω
$V_{CEO\ T43}$ h_{FE}	Breakdown voltage Current gain	$I_4 = 0$; $I_3 = 500\mu$A I_3 = 1mA	13 30	 120		 V

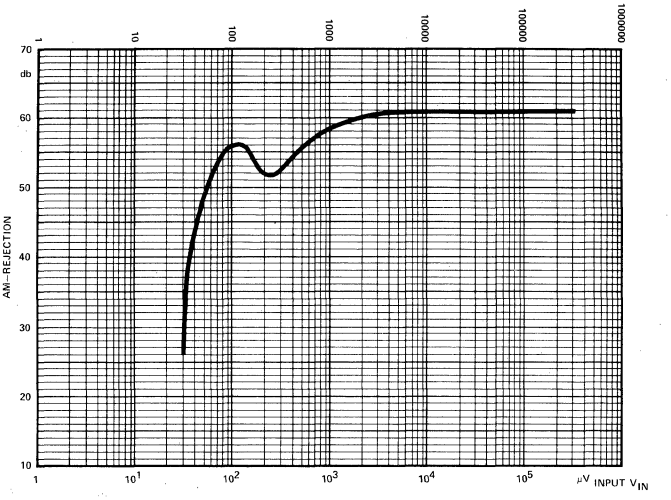
14

TYPICAL PERFORMANCE CHARACTERISTICS

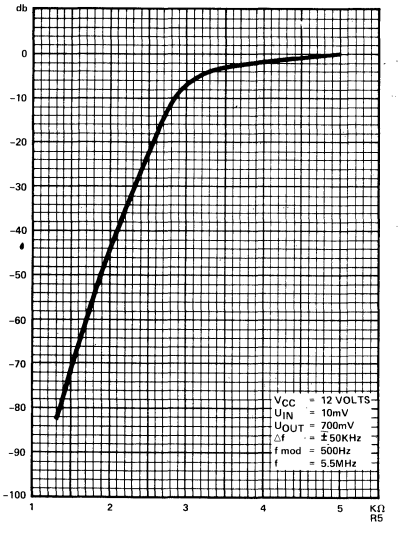
TYPICAL CURVE FROM PRODUCT SELECTION NR3.



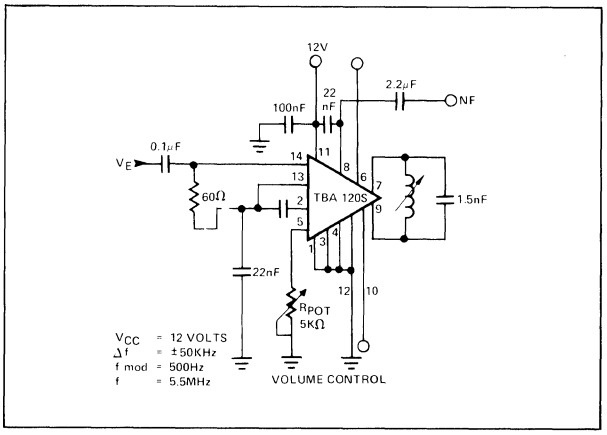
TYPICAL CURVE FROM PRODUCE-REFLECTION NR3.



VOLUME CONTROL SIGNETICS TBA120S



TEST CIRCUIT



FEATURES

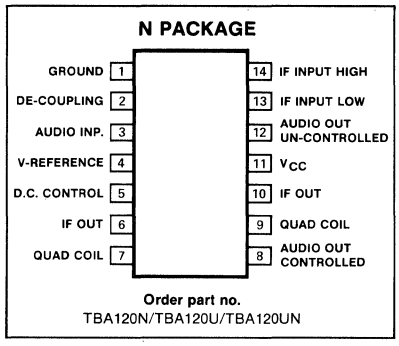
TBA120T

- Input and demondulator are designed for use with ceramic resonators
- Additional output before volume control (constant audio signal) for the connection of headphones and video recorders
- Additional audio input for connection of video recorders (playback)
- Constant audio output voltage between 10 to 18V supply voltage of the same level as TBA120S operating at 15V supply voltage
- Insensitive against hum from the supply voltage therefore very little need for smoothing capacitors
- As there is very little residual IF voltage on the audio output, there is no interference of the video-IF due to harmonics of the sound-IF
- No selection for volume control characteristics is necessary

TBA120U

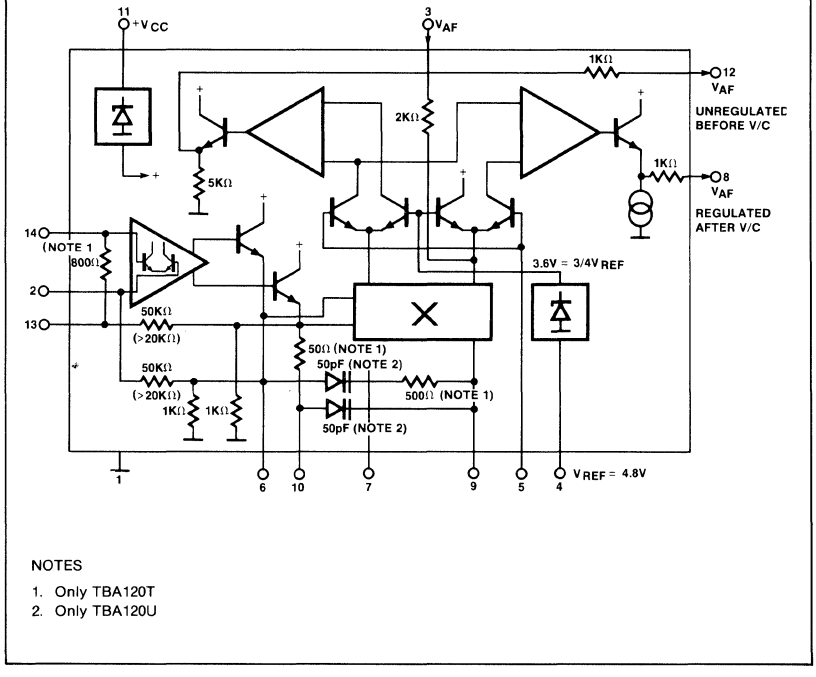
- This circuit incorporates all the advantages of TBA120T but input and demodulator are designed for use in connection with standard LC-circuits

PIN CONFIGURATION



Order part no.
TBA120N/TBA120U/TBA120UN

BLOCK DIAGRAM



NOTES

1. Only TBA120T
2. Only TBA120U

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	18	V
T_A	Ambient temperature in operation	-15 to +70	°C
T_S	Storage temperature	-40 to +125	°C
P_{TOT}	Total power dissipation	400	mW
V_S	Voltage	6	V
I_4	Current	5	mA
R_{13-14}	Ohmic resistance (TBA120U)	≤1	kΩ
R_{THSA}	Thermal resistance (system-air)	≤120	K/W
V_{CC}	Range of operation	10 to 18	V
f	Frequency range	0 to 12	MHz

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 12V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	TBA120T/120U			UNIT
			Min	Typ	Max	
I_{CC}	Total current consumption		9.5	13.5	17.5	mA
V_8	DC level of output signal	$V_i = 0$		4		V
V_{12}		$V_i = 0$		4.9		V
V_4	Stabilized voltage		4.2	4.8	5.3	V

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 12V$ unless otherwise specified.*

PARAMETER		TEST CONDITIONS	TBA120/120U			UNIT
			Min	Typ	Max	
G_V	IF voltage gain	V_6/V_{14} (f_{IF} = 5.5MHz)		68		dB
V_{qpp}	Output voltage with limiting at each output			250		mV
R_{q8}	Output impedance	Pin 8		1.1		kΩ
R_{q12}		Pin 12		1.1		kΩ
R_{13}	Input impedance			2		kΩ
R_{14}	Internal impedance			12		Ω
V_8	Residual IF voltage without deemphasis			20		mV
V_{12}				30		mV
V_8/V_3	AF gain	AF not regulated		7.5		
$V_{AF/8}$	Regulation at certain ratio of divider	R_{4-5} = 5kΩ, R_{5-1} = 13kΩ	20	28	36	dB
$\frac{V_{AFMAX}}{V_{AFMIN}}$	Range of volume control	Referred to pin 8	70	85		dB
R_{4-5}*	Resistance		1		10	kΩ
V_{ilim}	Input voltage for limitation	f_{IF} = 5.5MHz, f = ±50kHz, f_{MOD} = 1kHz		30	60	μV
V_8/V_{11}	Hum suppression			35		dB
V_{12}/V_{11}				30		dB

*NOTE
If dc volume control is not used, pin 4 has to be connected directly to pin 5.

AC ELECTRICAL CHARACTERISTICS TBA120T $T_A = 25°C$, $V_{CC} = 12V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	TBA120T ONLY			UNIT
			Min	Typ	Max	
Z_{IN}	Input impedance	f_{IF} = 5.5MHz		800/5		Ω/pF
a_{AM}	AM suppression	f_{IF} = 5.5MHz, f = ±50kHz, V_I = 500μV, f_{MOD} = 1kHz m = 30%	50	60		dB
V_8	AF output voltage	f_{IF} = 5.5MHz, f = +50kHz, f_{MOD} = 1kHz	650	900		mV
V_{12}			400	650		mV

*NOTE
If dc volume control is not used, pin 4 has to be connected directly to pin 5.

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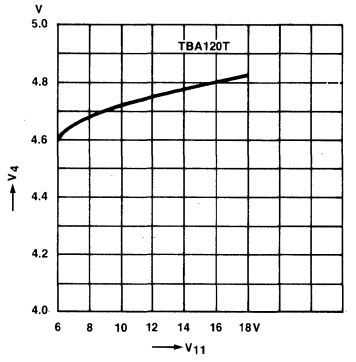
AC ELECTRICAL CHARACTERISTICS TBA120V $T_A = 25°C$, $V_{CC} = 12V$ unless otherwise specified.

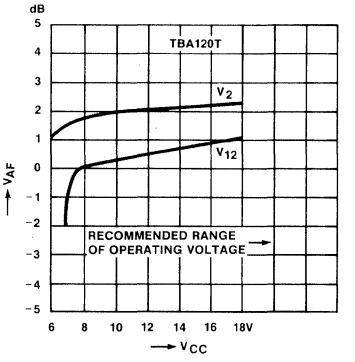
PARAMETER		TEST CONDITIONS	TBA120U ONLY			UNIT
			Min	Typ	Max	
Z_I	Input impedance	$f_{IF} = 5.5MHz$	15/6	40/4.5		kΩ/pF
a_{AM}	AM suppression	$f_{IF} = 5.5MHz$, f = ±50kHz, $V_i = 500\mu V$, $f_{MOD} = 1kHz$, m = 30%	50	60		dB
V_{8eff}	AF output voltage	$f_{IF} = 5.5MHz$, f = ±50kHz, $V_i = 500\mu V$, $f_{MOD} = 1kHz$, $Q_8 \approx 45$, k = 4%	850	1200		mV
V_{12eff}			600	1000		mV
k	Harmonic distortion	$f_{IF} = 5.5MHz$, f = +50kHz, $V_i = 10mV$, $f_{MOD} = 1kHz$, $Q_8 \approx 20$		1		%

TYPICAL PERFORMANCE CHARACTERISTICS

Z VOLTAGE vs SUPPLY VOLTAGE

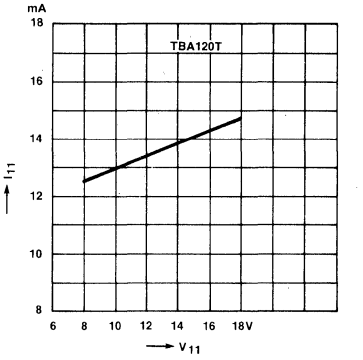


AF OUTPUT VOLTAGE vs SUPPLY VOLTAGE

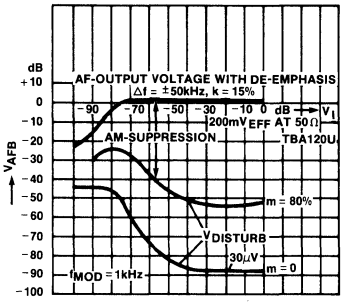


0dB ≙ $770mV_{EFF}$

TOTAL CURRENT CONSUMPTION vs SUPPLY VOLTAGE

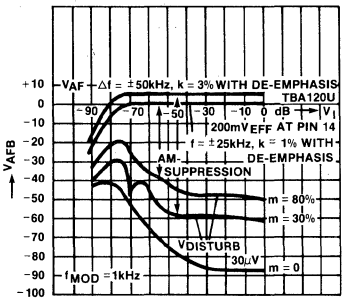


AF OUTPUT VOLTAGE AND DISTURBANCE VOLTAGE vs INPUT VOLTAGE (INPUT WIRED WITH SFE5.5MA/MURATA)



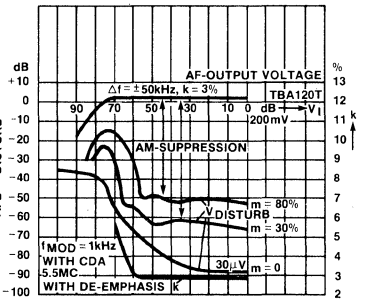
0dB ≙ $770mV_{EFF}$

AF OUTPUT VOLTAGE AND DISTURBANCE VOLTAGE vs INPUT VOLTAGE (INPUT 60Ω IMPEDANCE, BROADBAND)



0dB ≙ $770mV_{EFF}$

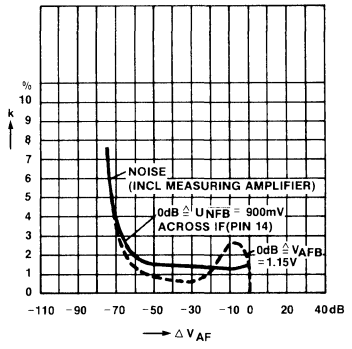
AF OUTPUT VOLTAGE (PIN 8), DISTURBANCE VOLTAGE AND HARMONIC DISTORTION vs INPUT VOLTAGE



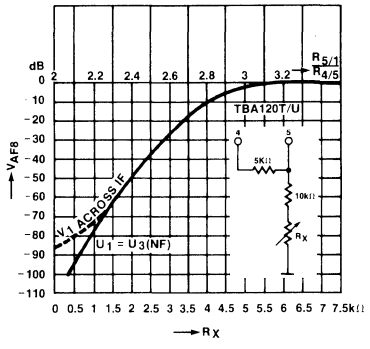
0dB ≙ $770mV_{EFF}$

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

HARMONIC DISTORTION vs VOLUME CONTROL

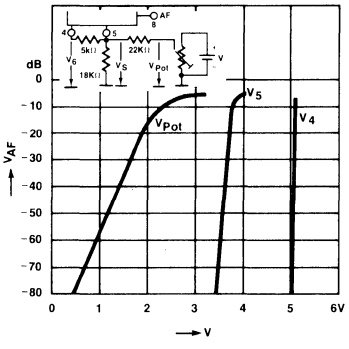


AF OUTPUT VOLTAGE (PIN 8) vs POTENTIOMETER RESISTANCE AND vs RATIO OF RESISTANCES



With electrolytic capacitor 47µF from pin 11 to ground.

AF OUTPUT VOLTAGE (PIN 8) vs VOLTAGE FEEDING INTO PIN 5

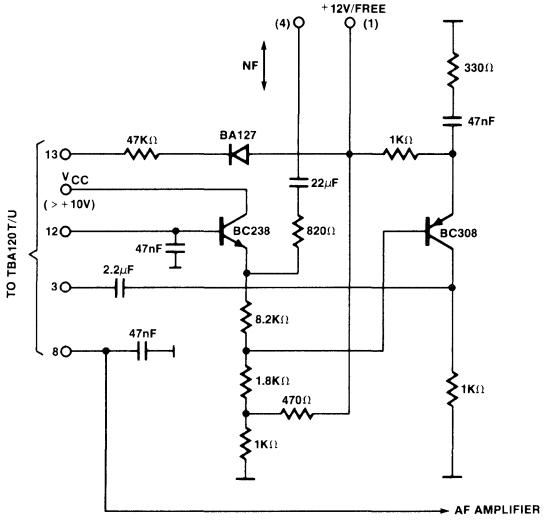


V_{IRF} = 60mV$_{EFF}$, f_{IF} = 5.5MHz, .1f = ±50kHz, f_{MOD} = 1kHz, V_{CC} = 18V

TEST CIRCUITS

CIRCUIT FOR DIRECT CONNECTION TO VIDEO RECORDERS

VIDEO RECORDER



SOCKET (1): Switching voltage: at playback +12V
at input free

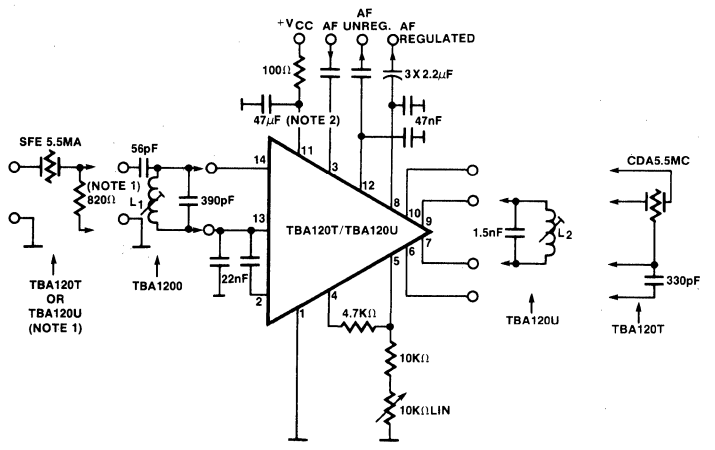
SOCKET (4): Simultaneous in and output for AF

FUNCTION:

When switching voltage applied the emitter follower, BC238, on the output is blocked and the buffer stage, BC308, is switched on. It includes a pre-emphasis to balance the de-emphasis at the AF output. The IF amplifier is put out of the operation by the diode, BA127, and the 47kohm resistor. The remote controllable volume regulator in the TBA120 T/U is used for recording and playback.

TEST CIRCUITS (Con't)

RECOMMENDED APPLICATION CIRCUIT (5.5MHz)



L_1: 20 windings 15 x 0.05 CuLS; $Q_0 \approx 73$
L_2: 9 windings 0.25 CuLS; $Q_0 \approx 40$
Coil Assembly Vogt D41 — 2165 (2438) without gaussion core

NOTES

1. 820 Ohm is no longer necessary for TBA120T, as resistance is integrated.
2. Omitting the electrolytic capacitor 47μF on pin 11 changes volume-control range.

TBA395-N

DESCRIPTION

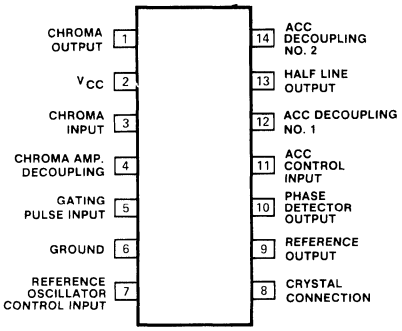
Chrominance combination circuit for use in PAL television receivers.

FEATURES

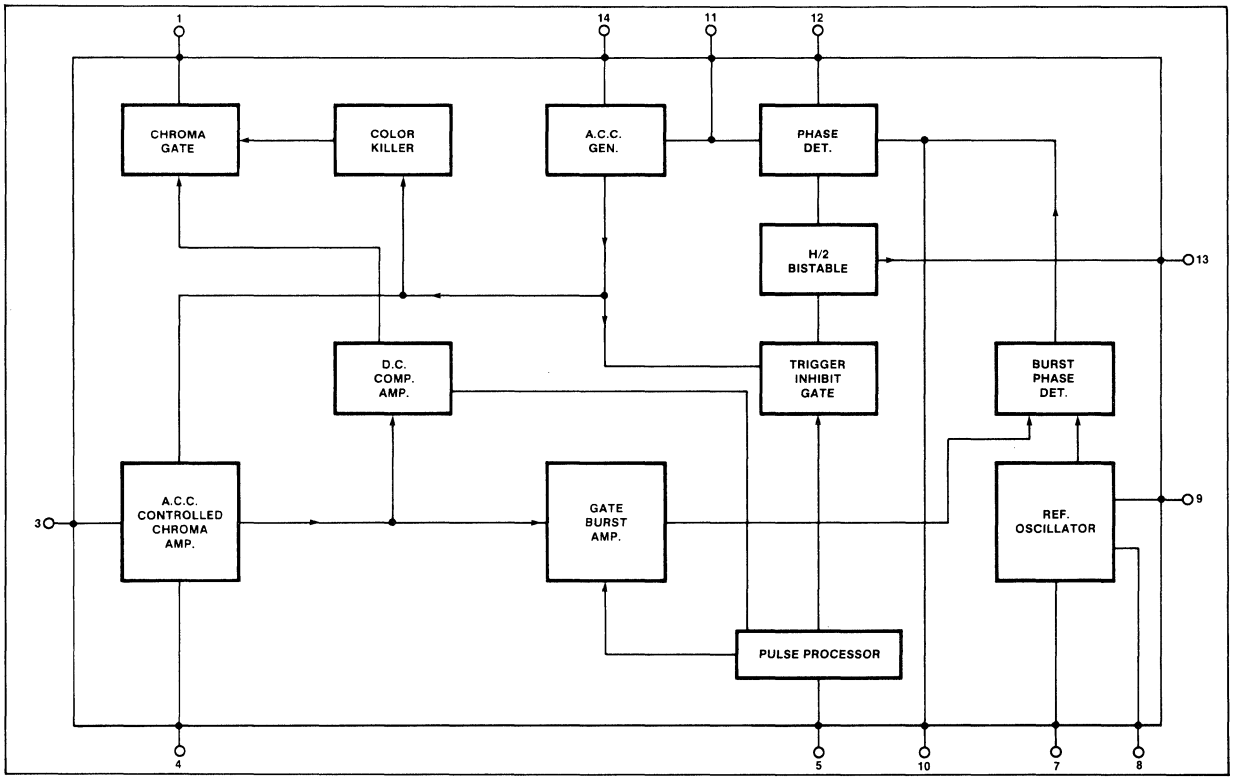
- **Internal supply line stabilization**
- **20dB ACC range—14dB + 6dB**
- **Low external component count**
- **Designed to be used in conjunction with TBA396 and TBA327/MC1327**

PIN CONFIGURATION

N PACKAGE



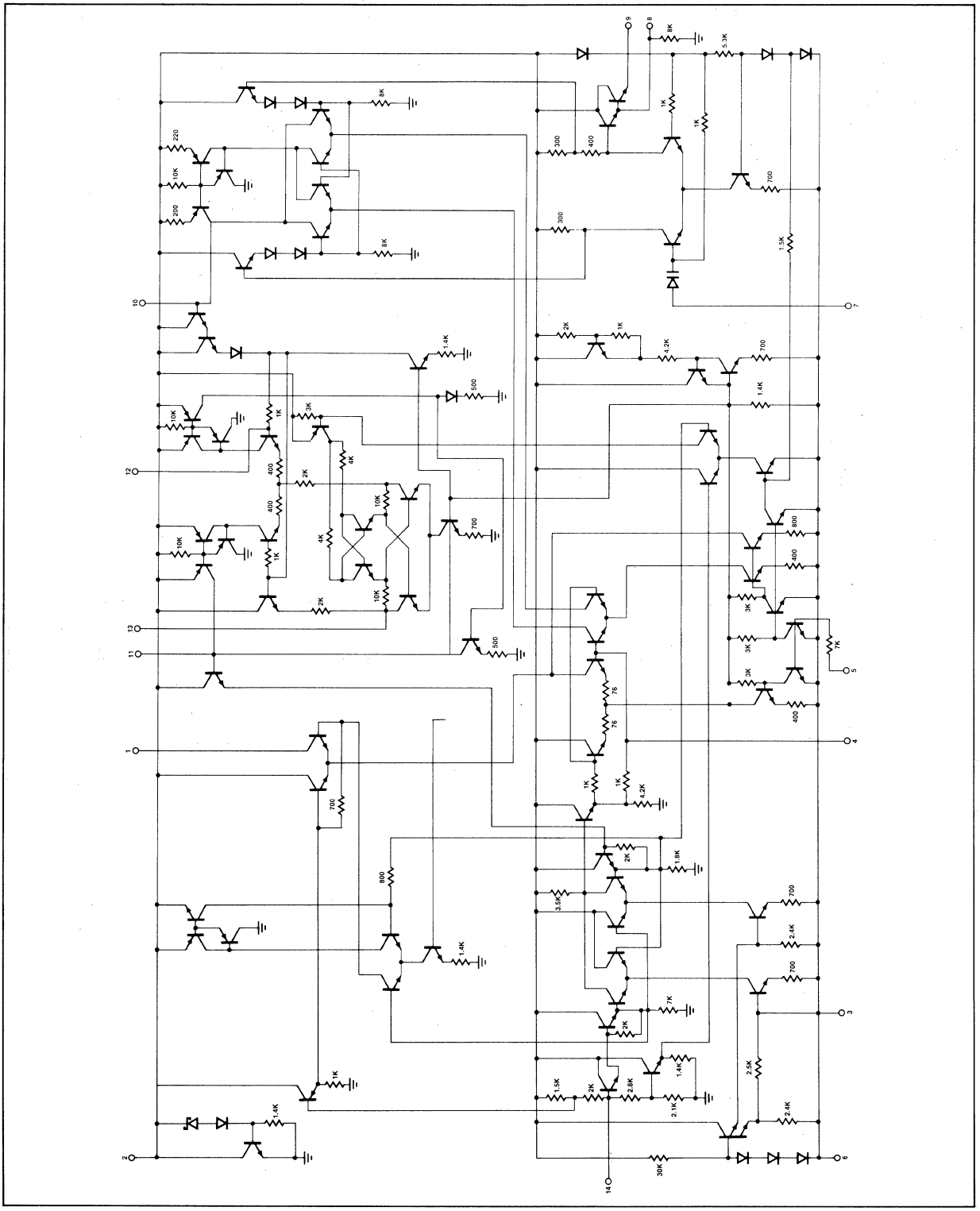
SYSTEM BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Power supply current	60	mA
dc current capability of reference output	4.0	mA
Chrominance input voltage	1.2	Vp-p
Operating temperature range	0 to +70	°C
Power dissipation (package limitation)	625	mW
Derate above T_A = +25°C	5.0	mW/°C
Storage temperature range	-65 to +150	°C

EQUIVALENT SCHEMATIC



TBA395-N

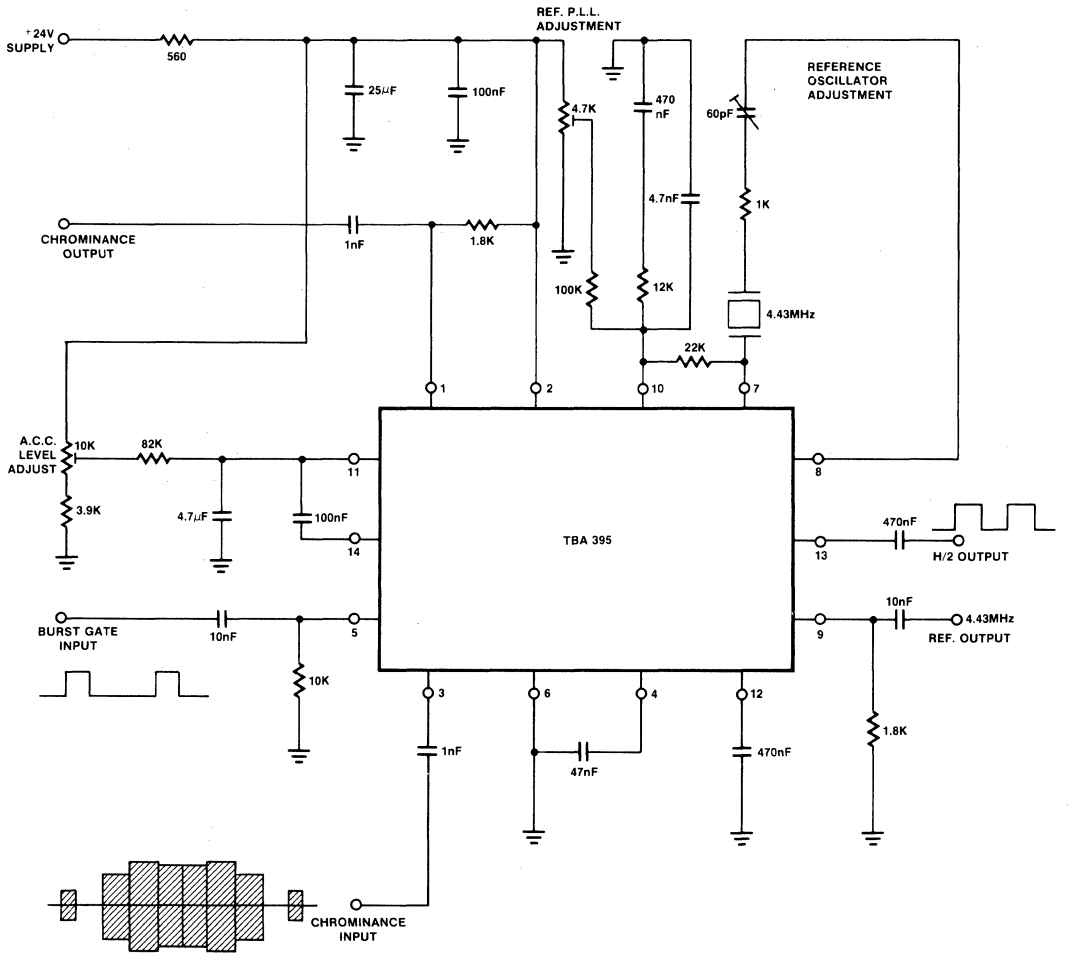
DC ELECTRICAL CHARACTERISTICS $T_A = +25°C$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	TBA395			UNIT
		Min	Typ	Max	
Supply voltage Burst gate operating voltage		7.5 2.0	8.4	9.5 5.0	Vdc V
Chrominance output dc current	Color killer operating Color killer off	 200		4.0	μA μA

AC ELECTRICAL CHARACTERISTICS $T_A = +25°C$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Forward transconductance	Chrominance output load = 560Ω f_{IN} = 4.43MHz	 6.4			 mmho
Chrominance input resistance Reference oscillator pull-in range		2.4 ±250	3.1	4.3	kΩ Hz
Reference output H/2 bistable output		400 1.3	700 1.6	 2.2	mV Vp-p

TYPICAL CIRCUIT CONFIGURATION



SETTING-UP NOTES

For subcarrier oscillator adjustment the chrominance input must be bypassed to ground via a 1nf capacitor. The ACC potentiometer is then set to 1.2 volts below pin 2 voltage using a high input impedance oscilloscope or Voltmeter ($> 10m\Omega$). While the adjustment is made burst gate pulses must be applied to pin 5.

The oscillator free-running frequency can then be adjusted to sub-carrier value $\pm 10Hz$.

The loop will lock if a chrominance signal is re-connected.

With a peak to peak signal of 250mV (100% bars) the output on pin 1 should be adjusted to 400mV peak to peak using the ACC control potentiometer.

APPLICATION NOTES

1. Normal decoupling precautions must be taken. For example pin 2 (8.4 volt circuit supply point) must be decoupled closely to pin 6 (ground) thus preventing sub-carrier components leaking into sensitive areas of the circuit.
2. To prevent the radiation of sub-carrier harmonics, the connection from pin 9 (reference output) and pin 8 (crystal feedback) must be kept as short as possible.
3. The connection from pin 1 (chroma output) should be also as short as possible to prevent capacitive loading of the $1.8k\Omega$ output resistor.

TBA396-N

DESCRIPTION

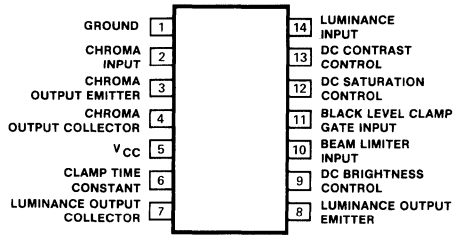
Luminance and chrominance combination circuit designed for use in PAL television receivers.

FEATURES

- **DC control of brightness, contrast and saturation**
- **Tracking of saturation with contrast control changes**
- **Beam current limiting**
- **Black level clamping**
- **Designed to be used in conjunction with TBA395 and TBA327/MC1327**

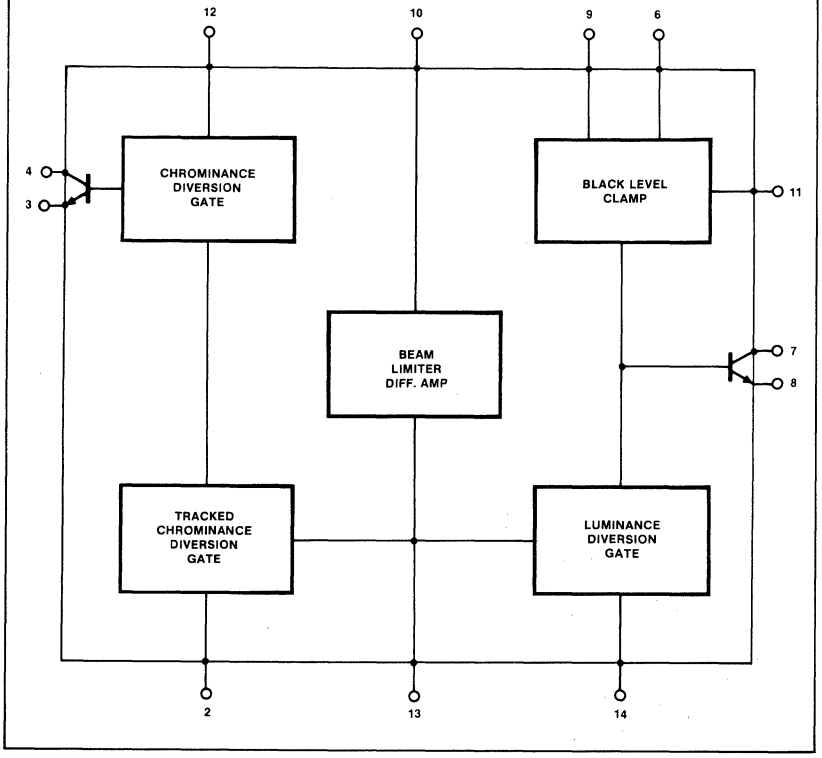
PIN CONFIGURATION

N PACKAGE



ORDER PART NO.
TBA396N

SYSTEM BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS T_A = +25°C unless otherwise specified.

PARAMETER	RATING	UNIT
Supply voltage	20	V
Luminance output collector voltage	30	V
Luminance output emitter current	7.0	mA
Chrominance output emitter current	5.0	mA
Operating temperature range	0 to +70	°C
Power dissipation (package limitation)	625	mW
Derate above T_A = +25°C	5.0	mW/°C
Storage temperature range	-65 to +150	°C

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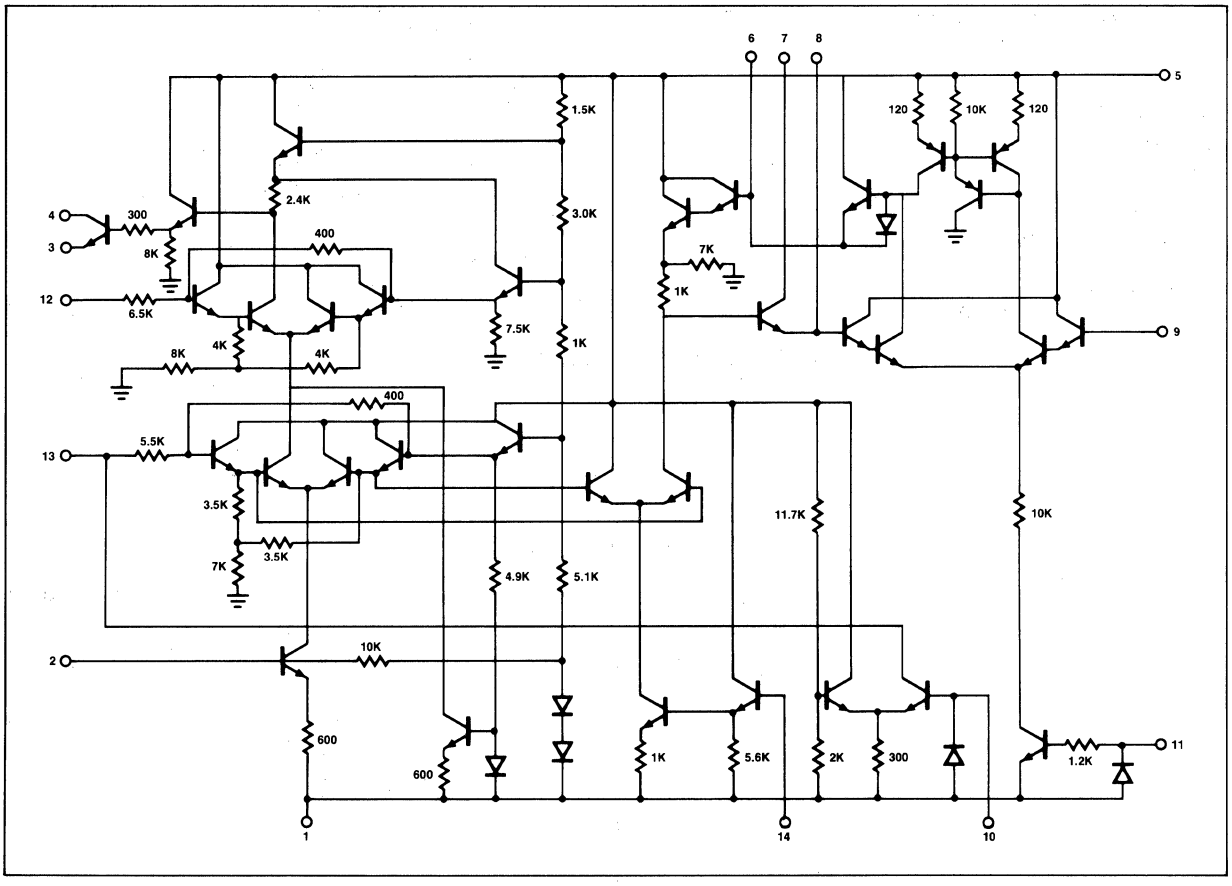
TBA396-N

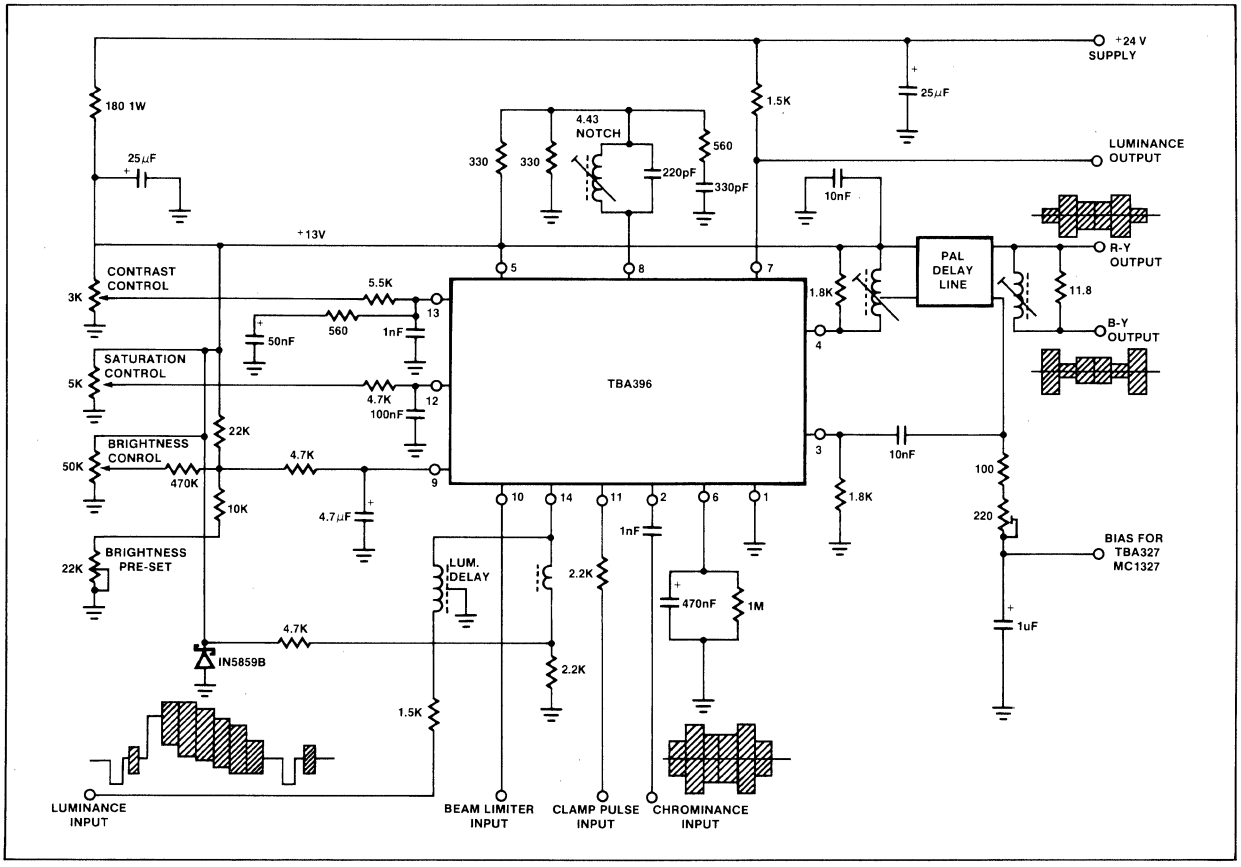
EQUIVALENT SCHEMATIC



GENERAL ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	TBA396			UNIT
		Min	Typ	Max	
Luminance input resistance		100			kΩ
Luminance gain		0.6	1.0	1.2	
Change of black level with contrast and signal changes	Black to white 4μs gating			3.0	%
Black level clamp gating pulse		50		1000	μA
Contrast control range		35			dB
Saturation control range		35			dB
3dB luminance bandwidth	Resistive load		7.5		MHz
Video input aperture		1.4		3.4	V_{p-p}
Chrominance input resistance		5.0			kΩ
Chrominance voltage gain	Resistive load	2.5	3.0	5.0	
Chrominance phase shift with saturation control				±3	%
Chrominance phase shift with contrast control				±3	%
Chrominance/Luminance tracking error with contrast control				±2	dB
Threshold of beam limiter		1.8	2.0	2.2	V

TYPICAL CIRCUIT CONFIGURATION



APPLICATION NOTES

- **The dc controls are relatively insensitive to interference if the decoupling associated with these lines is close to the IC.**
- **Good decoupling is required close to the "cold" end of the PAL delay line driving coil to prevent spurious subcarrier components reaching the IC supply line.**

SETTING UP PROCEDURE

The pre-set brilliance control must be adjusted to give the correct black level of +16.5V at pin 7. If the color demodulator IC TBA327/MC1327 is used to complete the system a voltage of +7.5V at the chroma outputs can be set using the same procedure.

This operation must be performed with the brilliance control at the center of its range.

TBA1440-N

DESCRIPTION

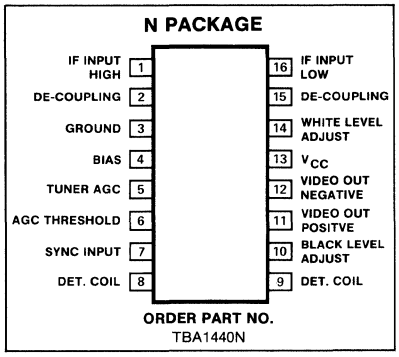
The circuit is a TV-video amplifier-demodulator and consists of:

Three symmetrical IF-broadband-amplifiers with AGC on the first and second stage,
A video balanced-carrier demodulator,
A video pre-amplifier with lowpass-characteristic,
Gated AGC-section for IF-amplifier and a Delayed tuner-AGC-current
TBA1440 is for PNP-type tuner
The AGC-current is high enough to drive pin-diodes

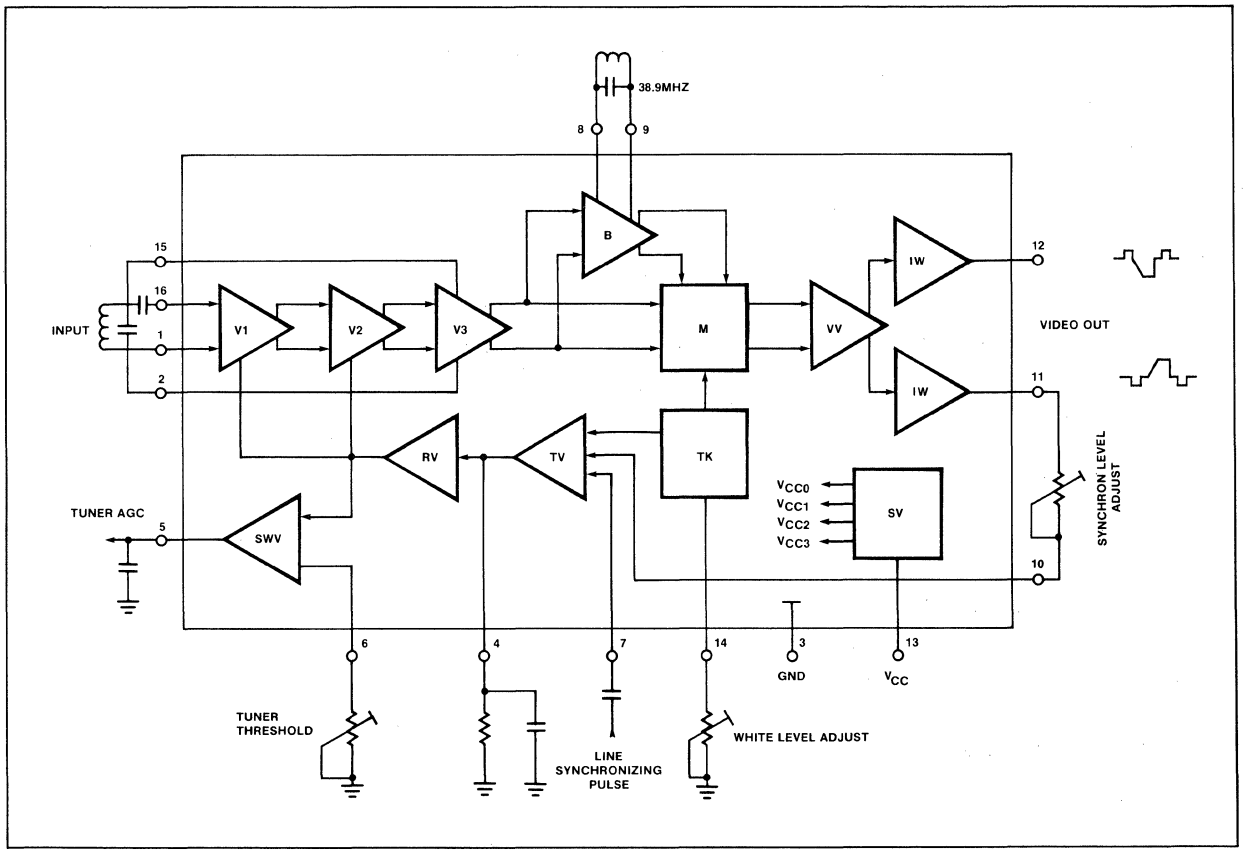
FEATURES

- **High gain—high stability—low noise**
- **Constant input impedance**
- **Output independent of supply-voltage over the operating range**
- **Minimum IF at video-outputs**
- **Fast AGC**
- **Low intermodulation products**
- **Low impedance outputs for positive and negative going video**
- **DC-levels temperature compensated**
- **Adjustable black and white level, each independent from the other**
- **High tuner-AGC current**
- **Adjustable tuner-AGC threshold**

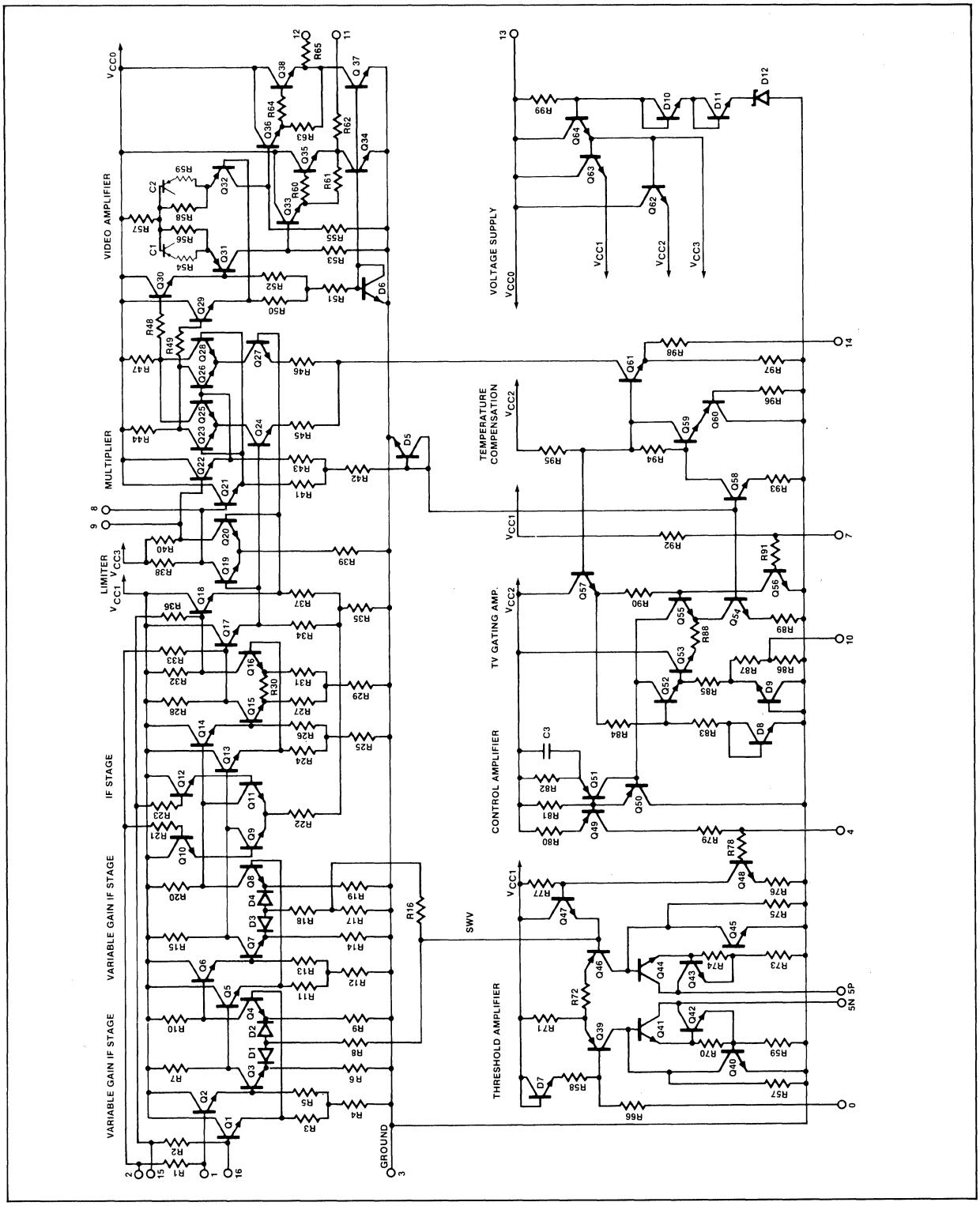
PIN CONFIGURATION



BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Power supply voltage	10.5 to 16	V
Voltage at pin 4	5	V
Voltage at pin 5	16	V
Voltage at pin 14	5	V
Ohmic resistance between pin 8 and pin 9	0 to 20	Ω
Power dissipation		
25°C	1100	mW
70°C	700	mW
Thermal resistance junction to ambient	110	°C/W
Operating temperature range	-25 to +70	°C
Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

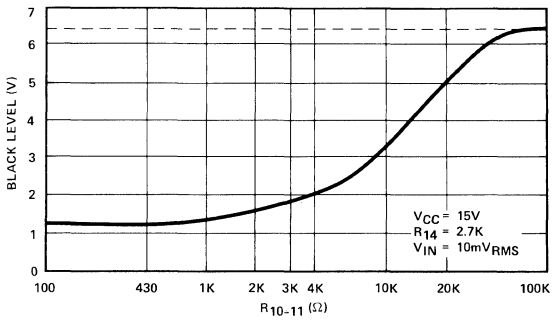
PARAMETER	TEST CONDITIONS	TBA1440			UNIT
		Min	Typ	Max	
V_{CC}		10.5	15	16.5	V
I_{CC}	V_{CC} = 15V		40	45	mA
V_{110}	V_{11} - DC/R_{14} = 0	7.9	8.2	8.5	V
V_{11}	V_{11} - DC/R_{14} = ∞	5.4	5.8	6.2	V
V_{120}	V_{12} - DC/R_{14} = 0	2.4	2.8	3.0	V
V_{12}	V_{12} - DC/R_{14} = ∞	1.25	1.6	1.8	V
THRESHOLD FOR SYNC. LEVEL					
$-V_{10}$	R_{10-11} = 0	0.7	1.0	1.3	V
$-V_7$	Negative gating pulse	0.25	1	7	V
GAIN CONTROL VOLTAGE					
V_{4max}	Gain max		0.5	1	V
V_{4min}	Gain min		1.6	2	V

AC ELECTRICAL CHARACTERISTICS

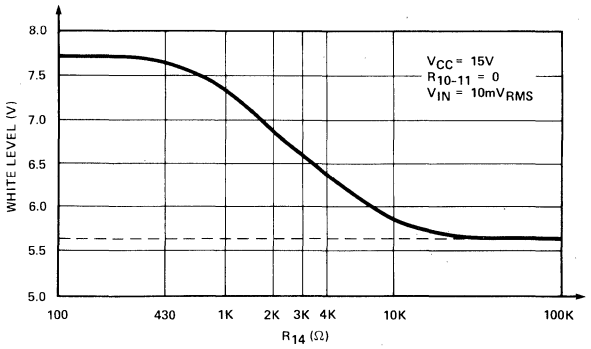
PARAMETER	TEST CONDITIONS	TBA1440			UNIT
		Min	Typ	Max	
MINIMUM INPUT VOLTAGE					
$V_{1/16}$	V_{11} = 3Vpp		500	750	μV
V_{11}	Videoband width (-3dB)	5.5	6	7	MHz
ACC range		50	55		dB
Maximum IF voltage level present at video outputs			60	70	mV
Input impedance	Gain max		1.8		kΩ
			2.0		pF
	Gain min		1.9		kΩ
			1.9		pFΩ

TYPICAL PERFORMANCE CHARACTERISTICS

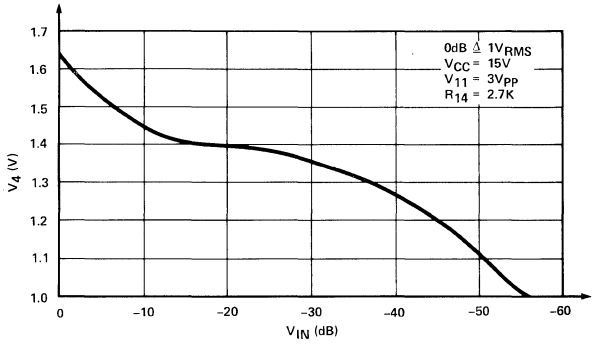
TBA1440
BLACK LEVEL vs R_{10-11}



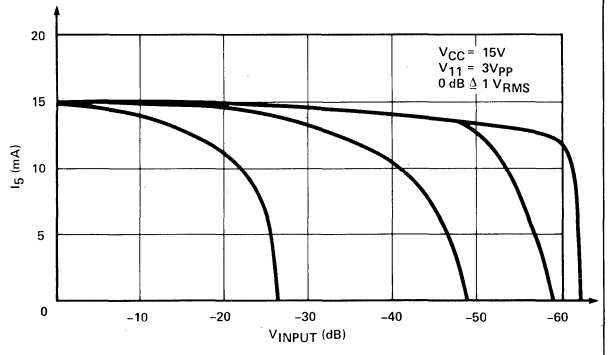
TBA1440
WHITE LEVEL vs R_{14}



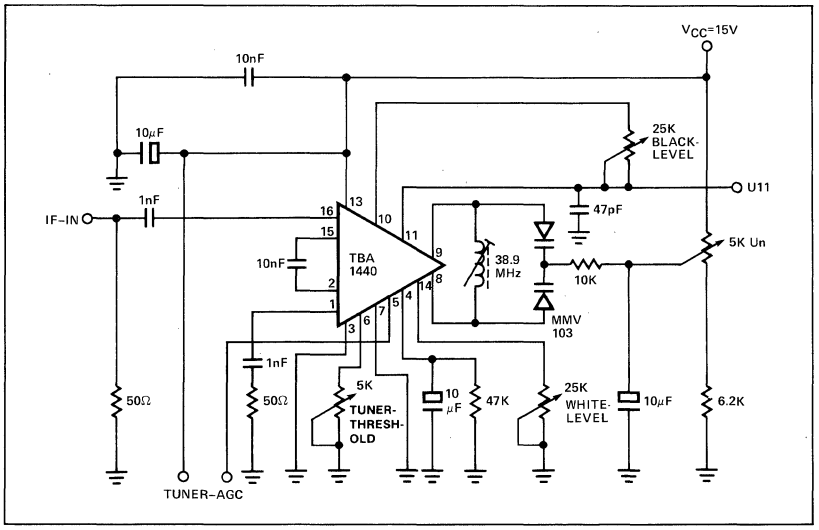
TBA1440
V_4 vs V_{INPUT}



TBA1440
I_5 vs V_{INPUT}



TEST CIRCUIT



TBA1440G/1441-N

DESCRIPTION

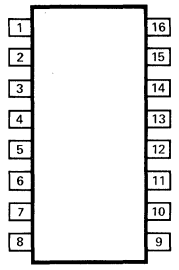
The TBA1440G (for pnp tuner pre-stages) and TBA1441 (for npn tuner pre-stages) have been developed from the TBA440P/N. Their improvements are as follows:

- Reduced residual IF at outputs 11 and 12
- Reduced residual IF at pin 13
- Considerably improved intermodulation distance
- Excellent tuning attitude even with low-ohmic tank circuit at demodulator

The IC's contain a high-amplifying controllable video IF amplifier, a controlled demodulator and two low-resistance video outputs with positive- and negative-going signals as well as the complete keyed control and delayed tuner control.

- Large control range with low noise and wide dynamic range
- High sensitivity
- Controlled demodulator, so minimum 1.07MHz disturbances
- Internal temperature stabilization
- The white levels of the video signals at the positive and negative video output are independent of the operating voltage
- The white and black levels can be adjusted separately

N PACKAGE



ORDER PART NO.
TBA1440GN, TBA1441N

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{13}	Supply voltage	15*	V
V_4	Voltages	5	V
V_5		20	V
V_{14}		5	V
R_{8-9}	Ohmic resistance between pins 8 and 9	≤ 20	Ω
R_{THSA}	Thermal resistance (system-air)	100	K/W
T_J	Junction temperature	150	°C
T_S	Storage temperature	-40 to +125	°C
V_{13}	Supply voltage range	10.5 to 15	V
T_A	Ambient temperature in operation	-25 to +60	°C

*NOTE
Briefly 16.5V

DC ELECTRICAL CHARACTERISTICS

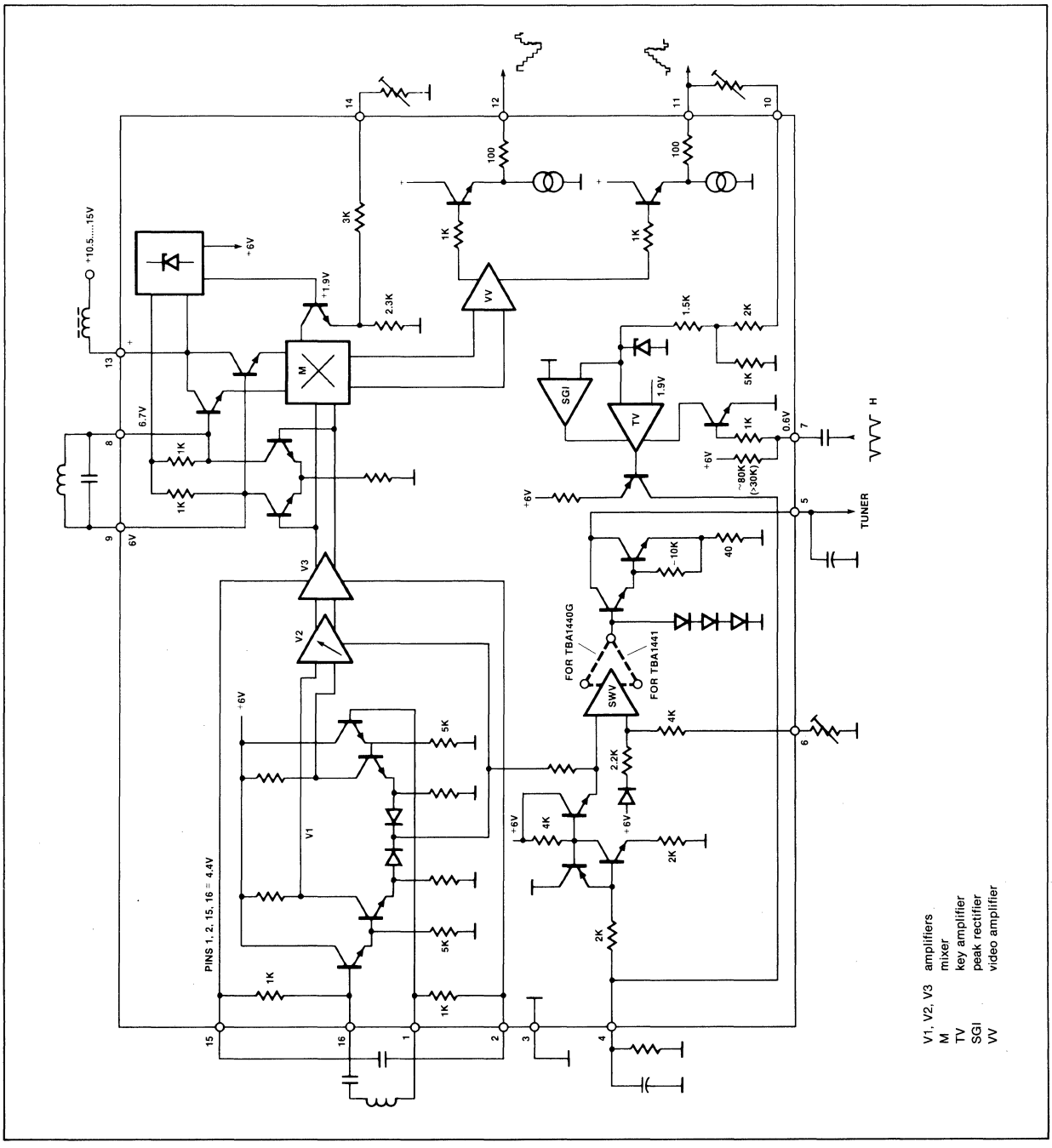
V_{13} = 13V, f_{IIF} = 38.9MHz; T_A = 25°C; all data with reference to ground, unless otherwise specified.

PARAMETER		TEST CONDITIONS	TBA1440G/1441			UNIT
			Min	Typ	Max	
I_{13}	Current consumption	V_{13} = 15V	34	47	60	mA
V_{11}	DC voltage at output 11	V_{13} = 15V; V_1 = 0				
		$R_{14-3} = \infty$		5.5		V
		R_{14-3} = 0		9.6		V
V_{12}	DC voltage at output 12	V_{13} = 15V; V_1 = 0				
		$R_{14-3} = \infty$		1.9		V
		R_{14-3} = 0		3.5		V
$V_{10} = V_{11}$	AGC threshold	V_{10} = sync pulse level for R_{10-11} = 0		1.9		V
V_{11sync}	Sync pulse level with async or without gating pulses	Peak level control		.5		V
V_4	IF control voltage	For max. gain	0		.5	V
		For min. gain	2.5		5	V
$-V_7$	Gating pulse voltage		2		5	V
I_{11}; I_{12}	Output current	To ground			5	mA
		TO $+V_{13}$			-1	mA

NOTES
1. According to test circuit; V_1 = effective sync pulse level at 60Ω.
2. Test level a_{cc} = -3dB
   a_{sc} = -20dB referring to picture carrier.

TBA1440G/1441-N

EQUIVALENT SCHEMATIC



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AC ELECTRICAL CHARACTERISTICS

(V_{13} = 13V; f_{IIF} = 38.9MHz; T_A = 25°C; all data with reference to ground, unless otherwise specified.

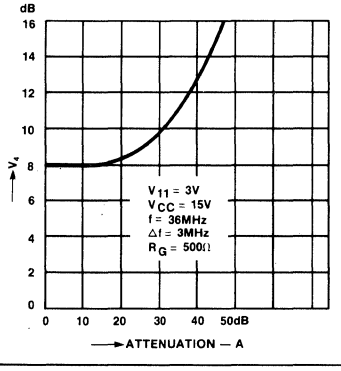
PARAMETER		TEST CONDITIONS	TBA1440G/1441			UNIT
			Min	Typ	Max	
$\Delta V_{11}/\Delta V_{13}$ $\Delta V_{12}/\Delta V_{13}$	White level deviation			100 20		mV/V mV/V
R_{14-3} R_{10-11}	Resistance for ΔV_{11} = 1V Resistance for sync pulse level deviation of 1V			8.5 2.4		kΩ kΩ
I_5	Control current for tuner prestage	V_5 > 2V TBA1440G: 10dB after AGC TBA1441: 10dB previous to AGC	10	15		mA
V_{11}; V_{12}	Residual IF (basic frequency)			10		mV
Z_{1-16}	Input impedance	At max. gain At min. gain		1.8/2 1.9/0		kΩ/pF kΩ/pF
V_1 B_{video}	Input voltage[1] Video band width	V_{11} = $3V_{PP}$ -3dB	70 6	100 7	300	μV MHz
ΔG_v a $Z_{q\ 8-9}$	AGC range Intermodulation with reference color carrier[2] Output impedance			55 45 2/2.5		dB dB kΩ/pF

NOTES

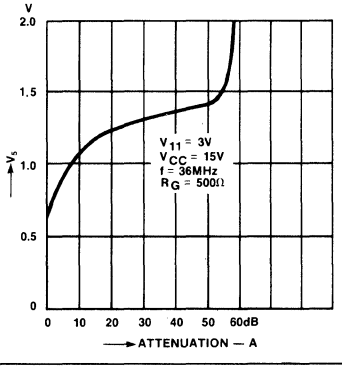
1. According to test circuit; V_1 = effective sync pulse level at 60Ω.
2. Test level a_{cc} = -3dB
   a_{sc} = -20dB referring to picture carrier.

TYPICAL PERFORMANCE CHARACTERISTICS

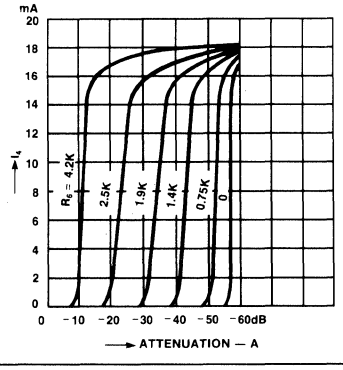
NOISE FIGURE vs ATTENUATION (MEASURED AD VIDEO FREQUENCY)
$-V_{fb}$ = 3V, V_{CC} = 15V, f = 36MHz, Δf = 3MHz, R_G = 500Ω



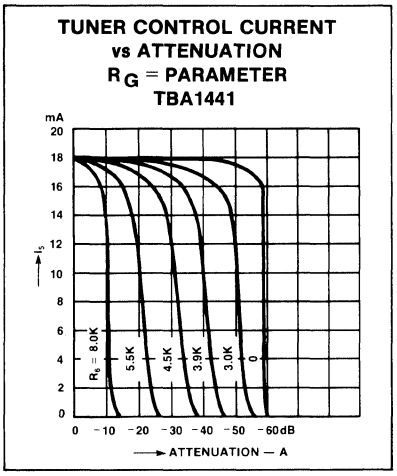
CONTROL VOLTAGE vs ATTENUATION
$-V_{fb}$ = 3V, V_{CC} = 15V, f = 36MHz, R_G = 500Ω



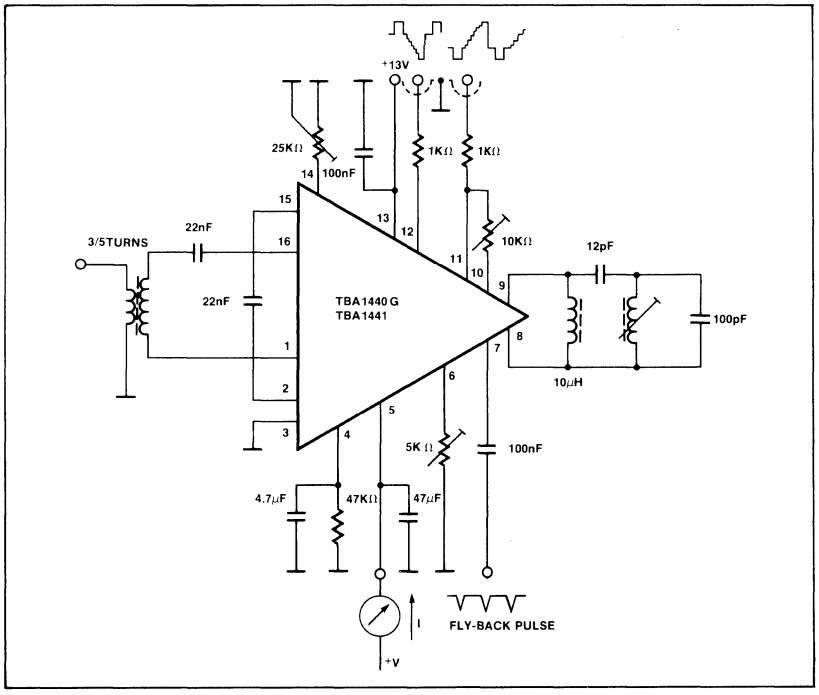
TUNER CONTROL CURRENT vs ATTENUATION R_G = PARAMETER TBA1440G



TYPICAL PERFORMANCE CHARACTERISTICS



TEST CIRCUIT

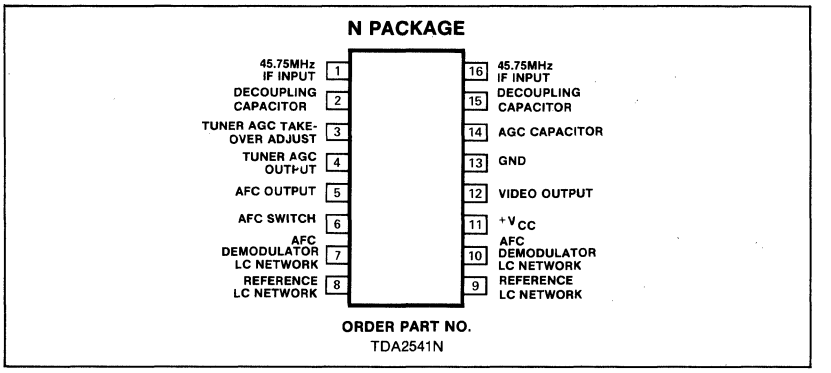


TDA2541-N

FEATURES

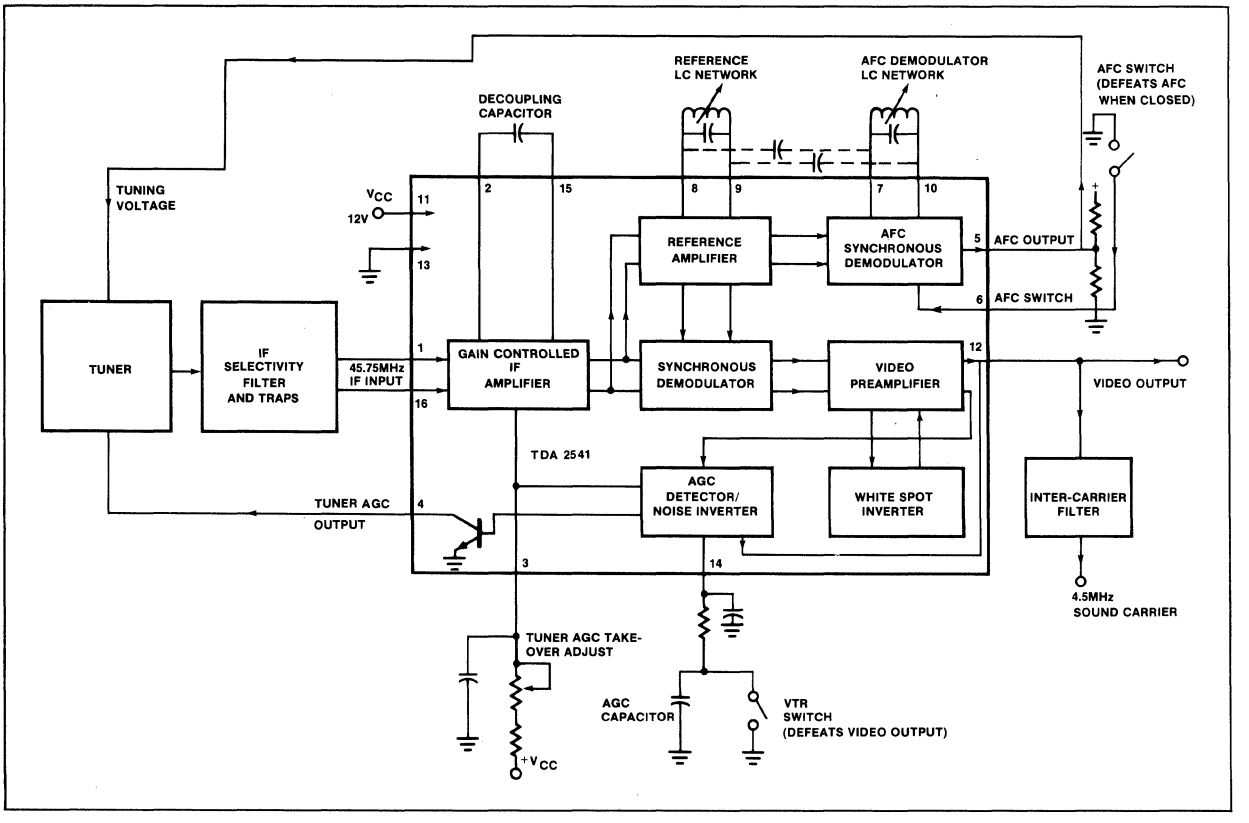
- Performs all video IF functions
- Provides 63dB IF AGC range
- Tuner AGC output
- Black and white noise inverting circuits
- AFC output
- High input sensitivity—100μV typical
- 53dB S/N ratio at 40dB gain control
- Minimal external components and adjustments required
- Switch disabling of video to allow direct video interface with VTR

PIN CONFIGURATION



ORDER PART NO.
TDA2541N

SIMPLIFIED BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage V_{CC}	14	V
Supply current (V_{CC} = 14V)	75	mA
Power dissipation (V_{CC} = 14V)	1.0	W
Operating temperature	0 to +70	°C
Storage temperature	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 12V unless otherwise specified.

PARAMETER		TEST CONDITIONS	TDA 2541			UNIT
			Min	Typ	Max	
I_{CC}	Supply current		37		67	mA
$V_{th(AFC)}$	AFC switched off below			2.5		V
I_5	AFC symmetry	V_i = 0, V_{14} = 0	-40		+40	μA
$V_{th(VTR)}$	VTR switch switches off below			1.1		V
V_{WS}	White spot inverter threshold level			6.6		V
$V_{D(WS)}$	White spot inversion clamping level			4.6		V
V_N	Noise inverter threshold level			1.8		V
$V_{0(N)}$	Noise inversion clamping level			3.8		V
I_4	Tuner AGC output ON current		10			mA
$V_{4(SAT)}$	Tuner AGC output voltage	I_4 = 10mA			300	mV
I_4	Tuner AGC output OFF current				10	μA

AC ELECTRICAL CHARACTERISTICS

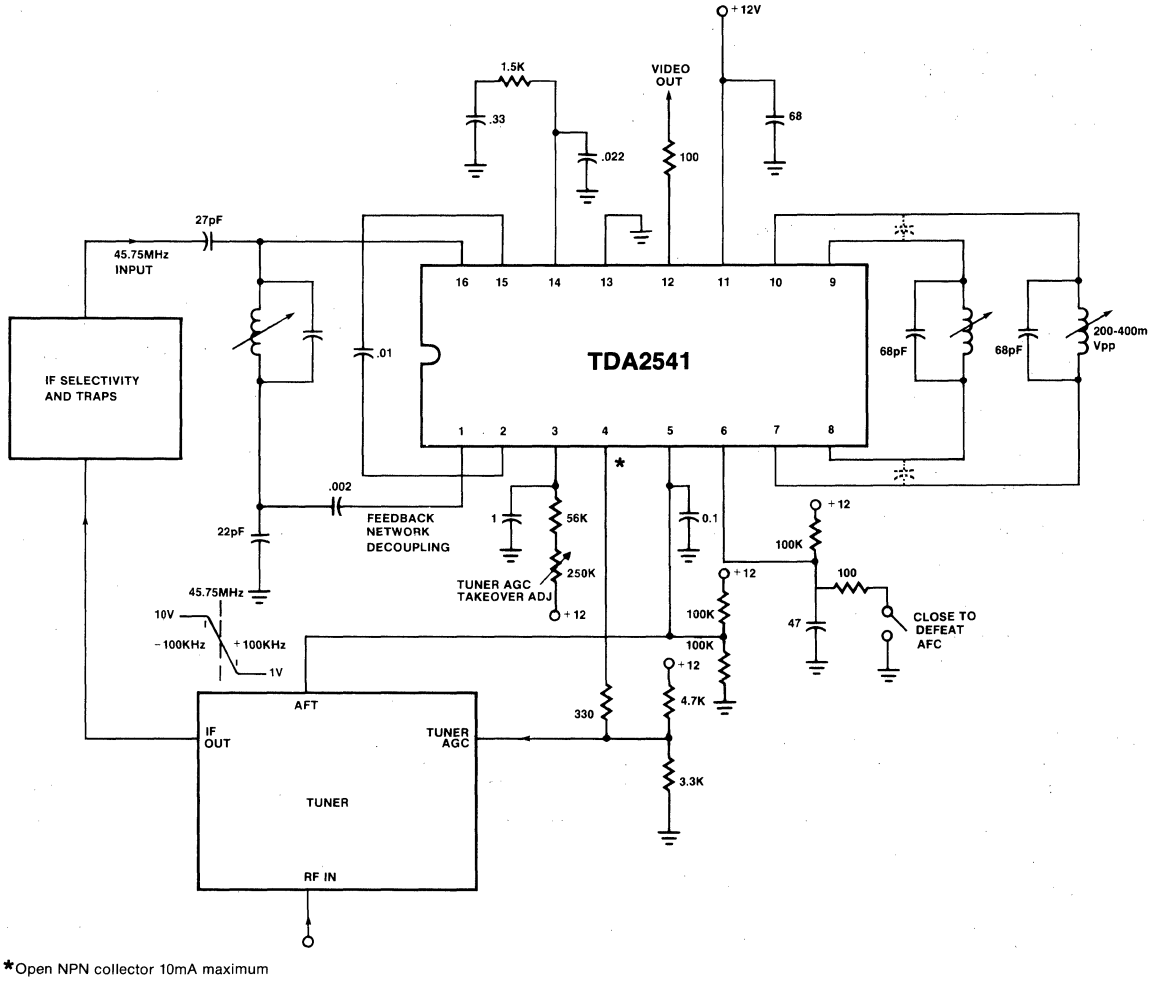
T_A = 25°C, V_{CC} = 12V unless otherwise specified.

PARAMETER		TEST CONDITIONS	TDA 2541			UNIT
			Min	Typ	Max	
V_i	IF input voltage for onset of AGC (f = 45.75MHz)		70	100	140	μV
$V_{o(Z)}$	Zero signal output level		5.7	6	6.3	V
$V_{o(TS)}$	Top sync level		2.9	3	3.2	V
V_5	AFC output voltage swing			10		V
ΔV_i	IF gain control range		50	63		dB
S/N	S/N at V_i = 10mV[1]			58		dB
B	3dB bandwidth of video amplifier			6		MHz
dG	Differential gain[2]			4	10	%
d0	Differential phase[2]			3°	10°	
	Intermodulation (1.1MHz)[3]	1.1MHz blue	46	60		dB
		1.1MHz yellow	46	50		dB
	Intermodulation (3.3MHz)[4]	3.3MHz	46	54		dB
	Carrier signal at video output			4	30	mV
	2nd harmonic of carrier at video output			20		mV
Δf	Change of frequency for 10V AFC swing			100	200	kHz

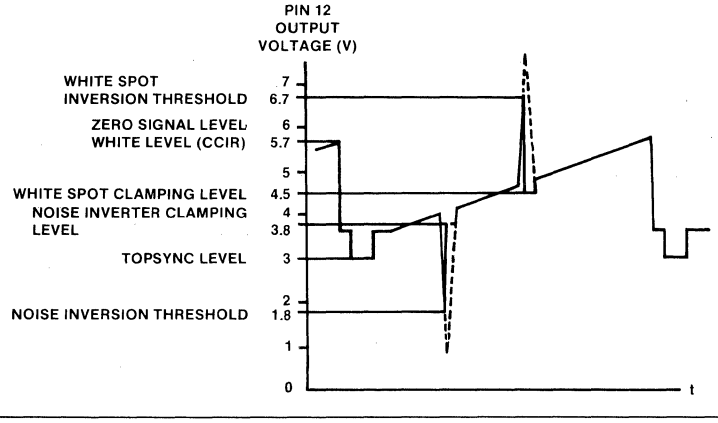
NOTES

1. $S/N = \frac{V_o \text{ black to white}}{V \text{ noise r.m.s. B = 5MHz}}$
2. Measured with the VZM-2 test set-up of Wandel & Goltermann or equivalent. Measured between 10 and 75% of topsync level.
3. Intermodulation 1.1MHz = $20 \log \left(\frac{V_o \text{ B-W}}{V_o \text{ p-p } 1.1\text{MHz}}\right)$ dB = $20 \log \left(\frac{V_o \text{ 4.4MHz}}{V_o \text{ 1.1MHz}}\right) + 3.6$dB
4. Intermodulation 3.3MHz = $20 \log \left(\frac{V_o \text{ 4.4MHz}}{V_o \text{ 3.3MHz}}\right)$ dB

TYPICAL APPLICATION



TDA2541 VIDEO OUTPUT



ULN2211-N

DESCRIPTION

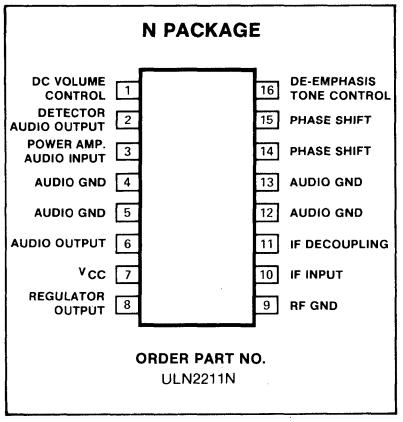
The ULN2211 contains a limiting amplifier, an FM quadrature detector, an electronic gain control stage and a 2-watt audio output stage. It can be used to detect and amplify any FM modulated signal having a 0.1–20MHz carrier frequency.

It is especially recommended as a complete TV sound channel requiring few external components and only one tuning adjustment for the 4.5MHz tank circuit. Provision is made for 6dB/octave de-emphasis and tone control.

FEATURES

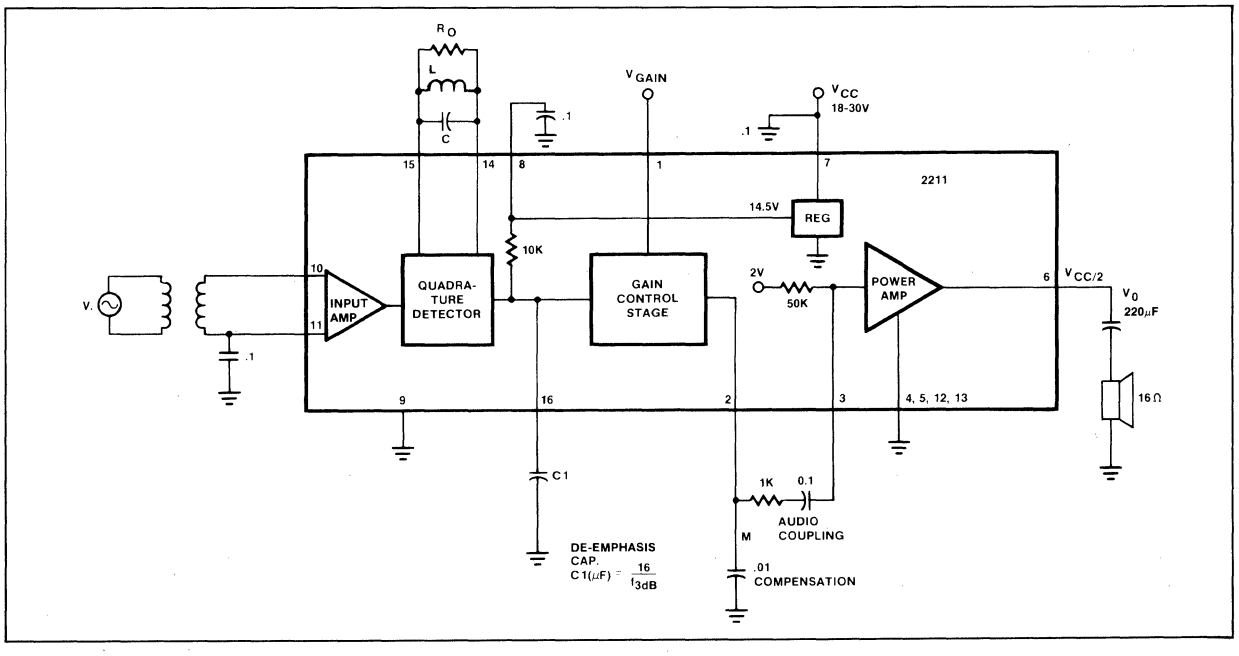
- **2-watt output**
- **DC volume control attenuation, 70dB typ**
- **Limiter gain of 70dB**
- **Limiting threshold typically less than 200μV**
- **Automatic thermal shutdown**
- **Over-current limiting**
- **20dB ripple rejection**
- **Single supply operation (18-30V)**
- **No crossover distortion**

PIN CONFIGURATION



NOTE: Internal power dissipation in watts.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage, V_{CC}	+30	V
Input voltage (pin 10)	+4.0	Vrms
Power consumption (internal)	See Figure 1	
Operating temperature	-25 to +70	°C
Storage temperature	-65 to +150	°C

14

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +24V; f_o= 4.5MHz, Δf = 25kHz, f_m = 400Hz unless otherwise specified.

PARAMETER		TEST CONDITIONS	ULN2211			UNIT
			Min	Typ	Max	
V_{TH}	Recovered audio limiting threshold[1]	Adjust V_1 for V_0 = 5.6V (P_O = 2W)		150	350	μV
AMR	AM rejection[2]	Adjust V_1 for 2W, V_{IN} = 10mV	30	55		dB
V_O	Recovered AF voltage (pin 16)	V_{IN} = 10mV, f = 25kHz	500	800		mVrms
THD_D	Detector output distortion	V_{IN} = 10mV, f = 25kHz		1.0	2.0	%
THD_O	Output distortion	P_O = 2W, R_L = 16		2	10	%
	Playthrough	V_1 = 0		10	15	mVrms
I_{MAX}	Current limit	R_L = 0		800		mA
V_N	Noise	V_{IN} = 0, V_1 = +15V		15	20	mVrms
A_V	Power AMP voltage gain[3]		25	27	29	dB
V_O/V_{CC}	Output tracking (V_6/V_7)	V_{CC} = 18 to 27V		0.5		V/V
Z_{IN}	Audio amp input impedance	f = 1kHz	40	50	60	kΩ

NOTES

1. Measured with output at -3dB, reference V_{IN} = 10mV, Δf = 25kHz
2. $AMR = 20 \log \frac{V_O \text{ (FM, } \Delta f = 7.5\text{kHz)}}{V_O \text{ (AM, 30\%)}}$
3. Set V_O = 1Vrms. $A_V = 20 \log \frac{1}{\text{(V3rms)}}$

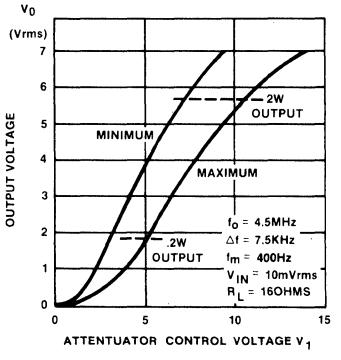
DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +24V unless otherwise specified.

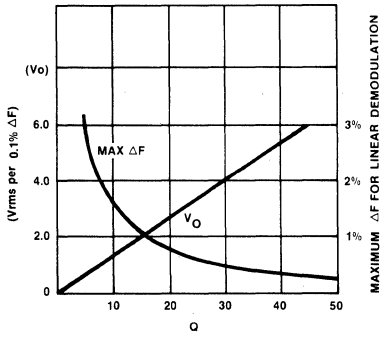
PARAMETER		TEST CONDITIONS	ULN2211			UNIT
			Min	Typ	Max	
I_{CC}	Standby current	V_{IN} = 0	25	45	60	mA
V_6	Terminal voltage		10.5	12.5	14.5	V
V_{10}				1.4		V
V_{11}				1.4		V
V_{14}, V_{15}				4.0		V
V_{16}				8.0		V
V_8			14	14.5	16	V
V_2				10		V
V_3				2.6		V

TYPICAL PERFORMANCE CHARACTERISTICS

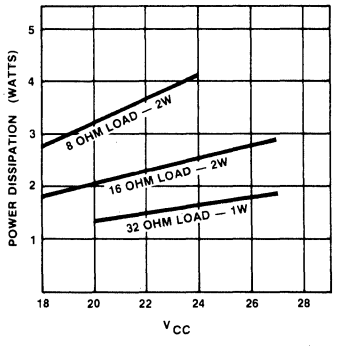
GAIN CONTROL CHARACTERISTIC



OUTPUT VOLTAGE AND LINEAR RANGE vs Q OF DETECTOR COIL



TYPICAL POWER DISSIPATION vs LOAD RESISTANCE AND V_{CC}



MAXIMUM ALLOWABLE POWER DISSIPATION

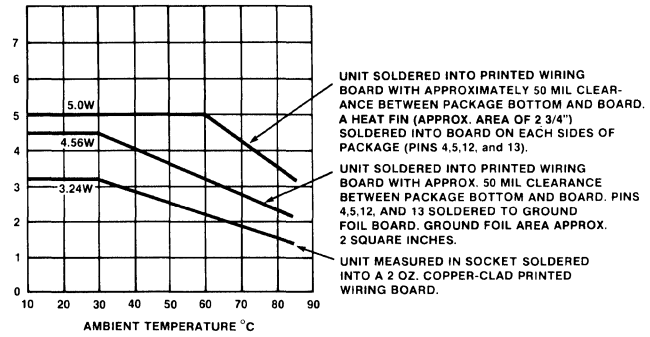


Figure 1

TYPICAL APPLICATION

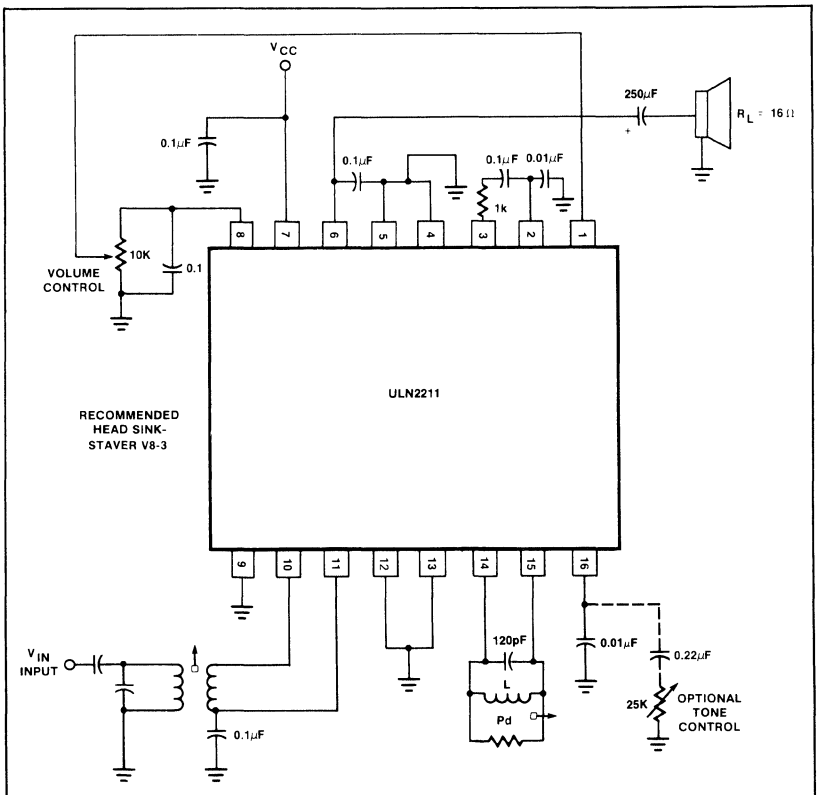


Table 1

f_o	L	R_D
4.5mHz	10-14μH	∞
10./mHz	1-3μH	5K

Figure 2

SECTION 15
GENERAL CONSUMER

NE543-K

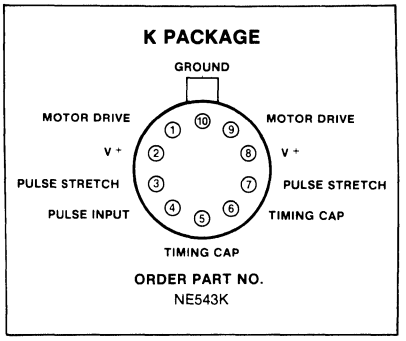
DESCRIPTION

The NE543 is a servo amplifier and pulse-width demodulator with internal motor drive transistors. It is designed for remote control applications in digital proportional systems but can be used in many other closed loop position control applications.

FEATURES

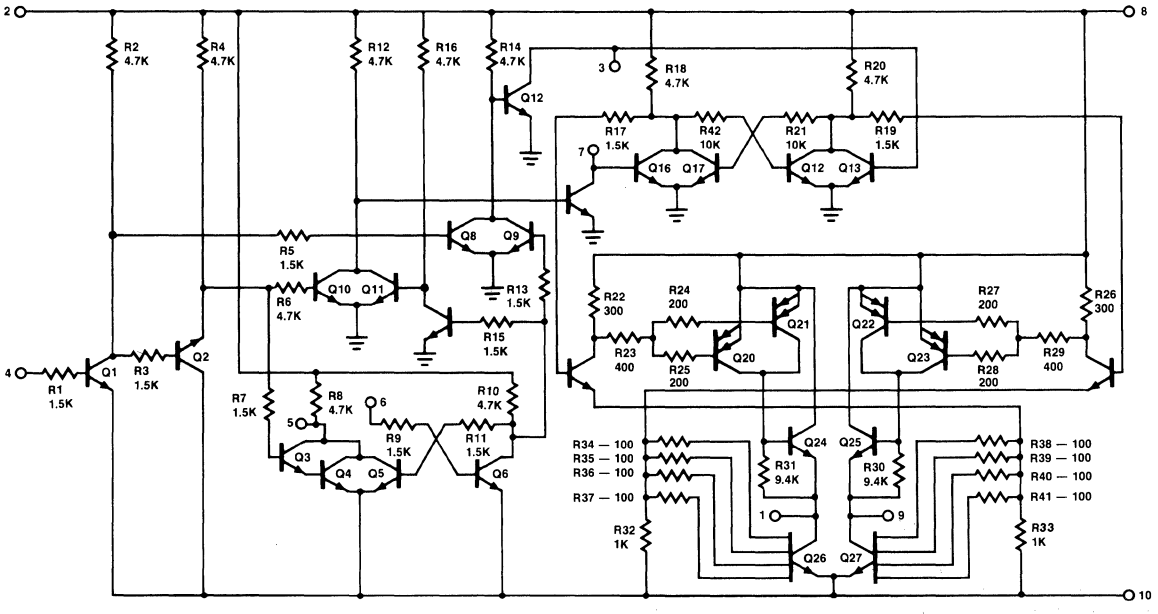
- **450mA load current capability without external power transistors**
- **Bidirectional bridge output with single power supply**
- **Low standby power drain**

PIN CONFIGURATION



ORDER PART NO.
NE543K

EQUIVALENT SCHEMATIC



NOTE

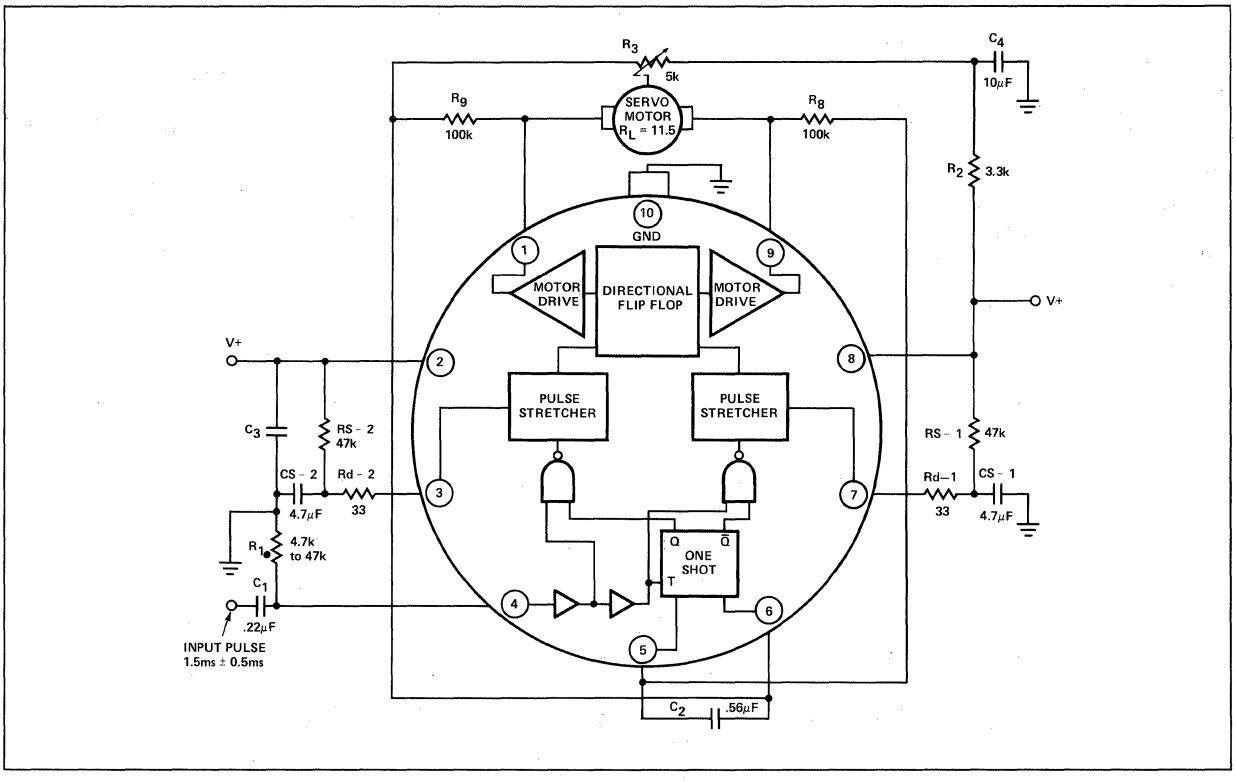
All resistor values are shown in ohms.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	6	V
Power dissipation (T_A = +25°C)	830	mW
Output current (T_A = +25°C)	450	mA

NE543-K

BLOCK DIAGRAM AND TYPICAL CONNECTION



NE543 SERVO DRIVER CONNECTION

The servo driver receives a nominal 1.5ms pulse from the receiver-decoder. The length of the input pulse is compared with an internally generated pulse. If the pulse durations differ by more than an allowed amount (the deadband), a pulse derived from the difference is stretched and applied to the output stage. If the input pulse is shorter, the motor is driven so as to reduce the value of R_3 and, hence, the internal pulse width. If the input pulse is longer, the motor is driven the other way so that R_3 increases and the internal pulse is lengthened. In this way, the control surface position can be made to follow the input pulse. The servo output moves over 100 degrees for pulses between 1 and 2ms. The pulses occur at 16ms intervals.

The internal pulse generator pulse width is determined by C_2 and R_2 in series with R_3. Capacitor C_4 decouples the pulse generator from the supply.

Deadband is controlled by Rd-1 and Rd-2. The 33ohm resistor sets deadband at about 4-5 microseconds (that is, the circuit will not drive the motor until the input pulse is 4 to 5 microseconds different from the internally generated pulse.)

Resistors RS-1 and RS-2 determine the amount of pulse stretching. Capacitors CS-1 and CS-2 are the pulse stretching capacitors. The value is not critical, but if changed RS-1 and RS-2 will have to be changed proportionately.

Resistors R_8 and R_9 are feedback resistors which prevent overshoot by adjusting the closed-loop damping.

Capacitor C_1 is the input coupling capacitor. Resistor R_1 can be any value in the range shown, but noise immunity is improved if it is at the low end of the range. Capacitor C_3 bypasses the power supply at the device.

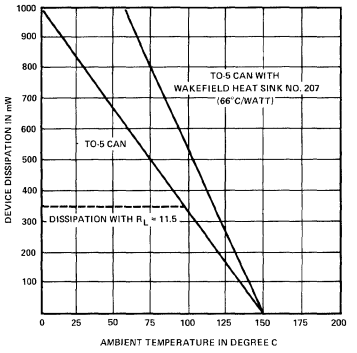
DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V^+ = 4.8V$ unless otherwise specified.

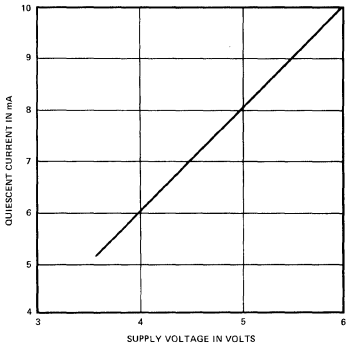
PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Supply voltage		3.6	4.8	6.0	V
Idle current			8.0	10.0	mA
Input bias current			24	50	μA
Input impedance	Pin 4 or pin 6 to ground	1.9	2.4	2.8	kΩ
Output voltage	$V_S = 4.8V$, $R_L = 35\Omega$	3.30	3.75		V
Output current	$V_S = 6.0V$, $R_L = 11.5\Omega$	340	385		mA
	$V_S = 4.8V$, $R_L = 11.5\Omega$	270	280		mA
	$V_S = 3.6V$, $R_L = 11.5\Omega$	185	200		mA
Output impedance		4.0	4.8	5.4	Ω
Power dissipation	Quiescent, $R_L = \infty$		39	48	mW
	$R_L = 11.5\Omega$		350		mW

TYPICAL PERFORMANCE CHARACTERISTICS

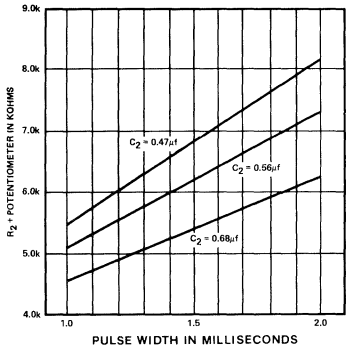
MAXIMUM DISSIPATION vs AMBIENT TEMPERATURE



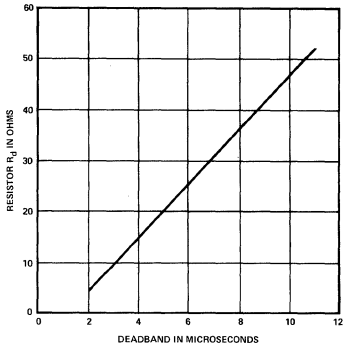
QUIESCENT CURRENT vs SUPPLY VOLTAGE



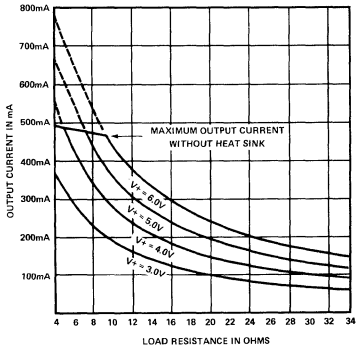
INTERNAL PULSEWIPTH vs R_3 AND C_2



DEADBAND vs RESISTOR R_d

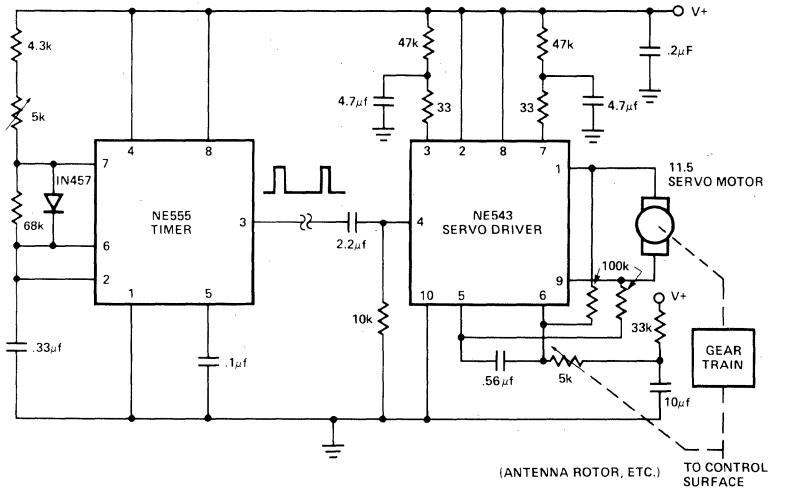


OUTPUT CURRENT vs LOAD RESISTANCE



TYPICAL APPLICATIONS

REMOTE CONTROL SERVO SYSTEM



NE544/644-N,W

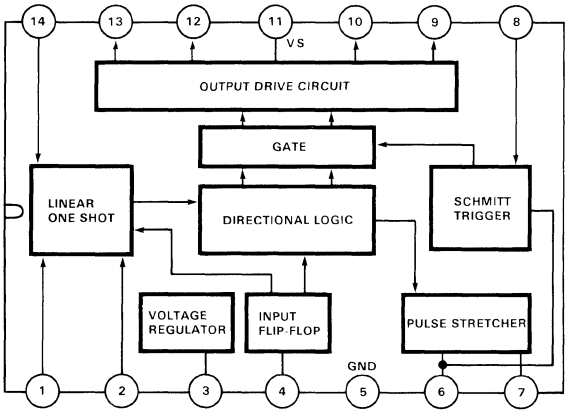
DESCRIPTION

The NE544 is a servo amplifier and pulse-width demodulator with internal motor drive transistors. It is designed for remote control applications in digital proportional systems but can be used in many other closed loop position control applications. It incorporates a linear one shot for improved positional accuracy and outputs for external pnp motor drive transistors.

FEATURES

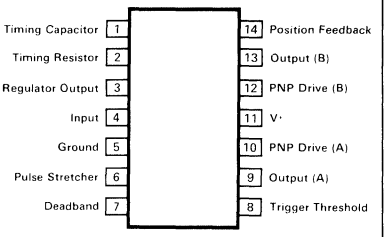
- **500mA load current capability**
- **Bidirectional bridge output with single power supply**
- **Low standby power drain**
- **Adjustable deadband and trigger thresholds**
- **High linearity, 0.5% maximum error**
- **Output drive for external PNP transistors (optional)**
- **Wide supply voltage range**

BLOCK DIAGRAM



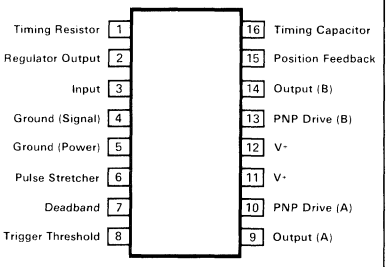
PIN CONFIGURATIONS

N PACKAGE



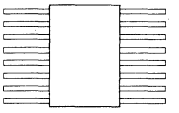
Order part no. NE544N

N PACKAGE



Order part no. NE644N

W PACKAGE*

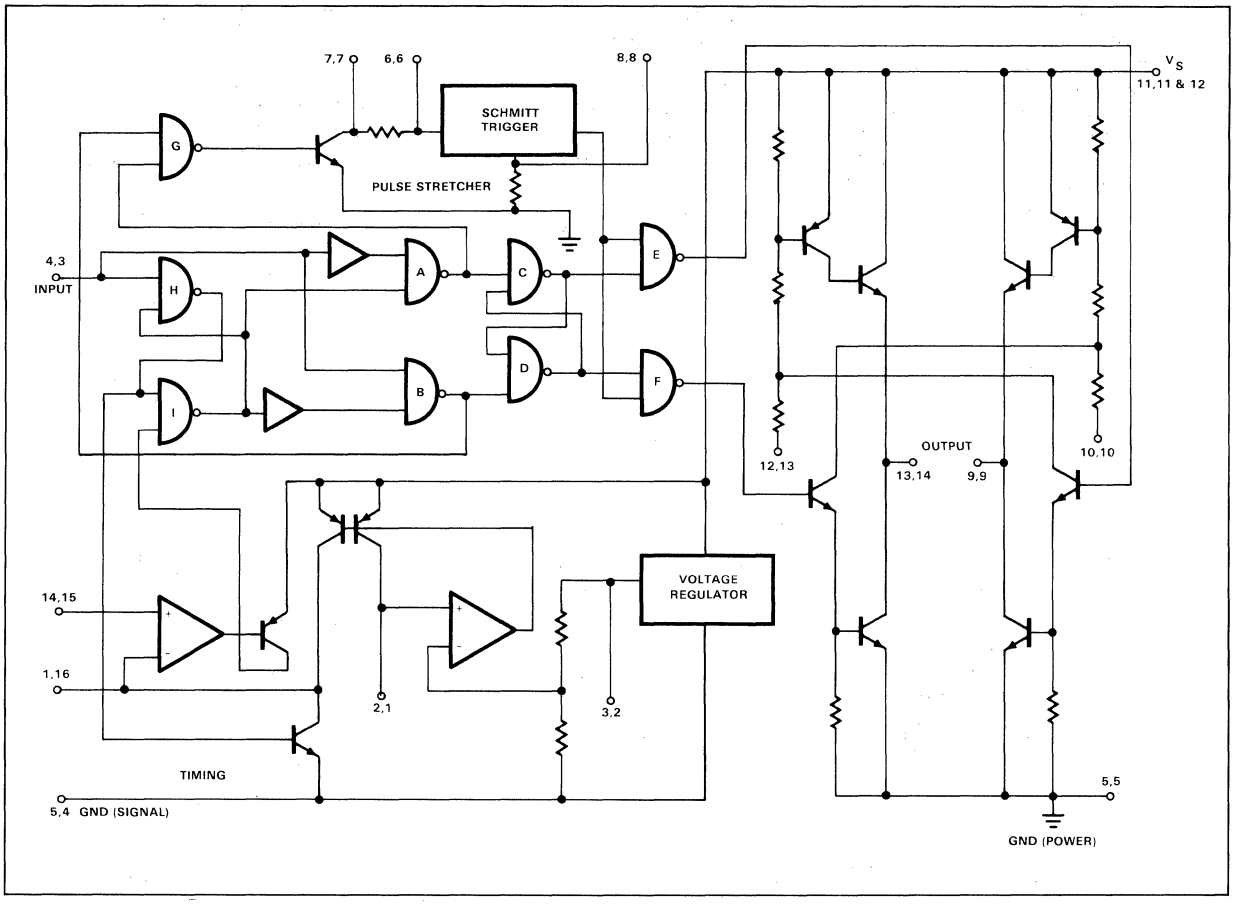


*Pinout same as 644N package
Order part no. NE644W

ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$ unless otherwise specified.

PARAMETER		RATING	UNIT
V+	Supply voltage	6.0	V
I_O	Output current	500	mA
T_A	Operating temperature	-20 to +75	°C
T_{stg}	Storage temperature	-65 to +150	°C

EQUIVALENT CIRCUIT SCHEMATIC



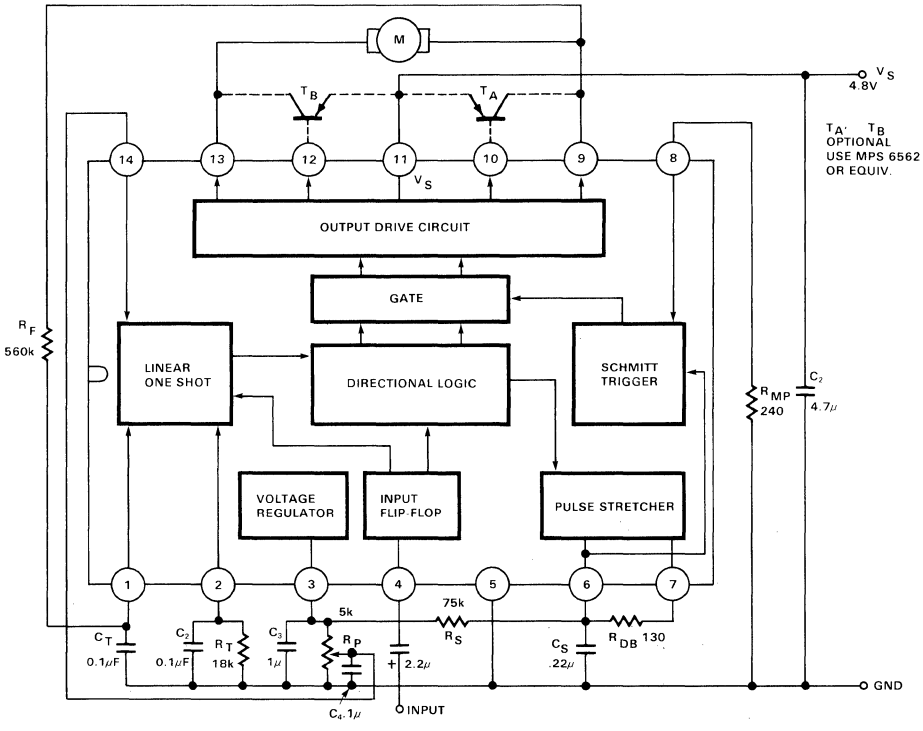
DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = 4.8V$ unless otherwise specified.

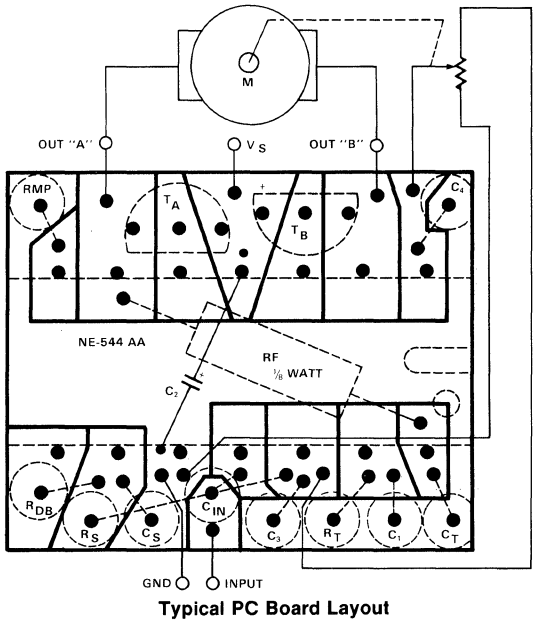
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		3.2	4.8	6	V
I_{CC}	Supply current	Quiescent	4.2	5.5	7.3	mA
V_{TH}	Input threshold					V
	On			1.5		
	Off			1.4		
Z_{IN}	Input resistance			18		kΩ
	Output voltage					V
V_{OL}	Low	Pin 9 or 13, I_L = 400mA		0.3		
V_{OH}	High			3.9		
V_R	Reference voltage		2.4	2.5	2.7	V
PSRR	Power supply rejection	$3.5V \leq V_S \leq 6V$		.01		%/V
	Minimum dead band	RDB = 0		1		μs
	One shot temperature coefficient			.01		%/°C
	Standby power			27		mW
	PNP drive current	Pin 10 and 12		20		mA

NE544/644-N,W

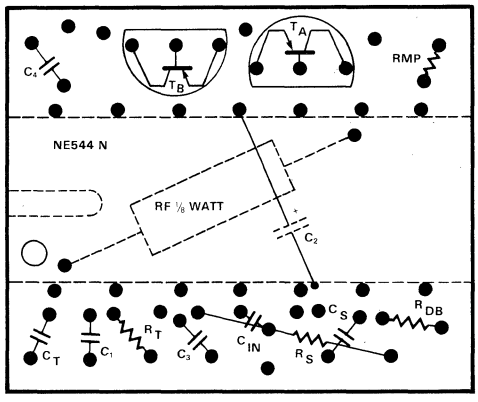
TYPICAL CONNECTION OF NE544N FOR LINEAR ONE SHOT TIMING



PC BOARD—N PACKAGE

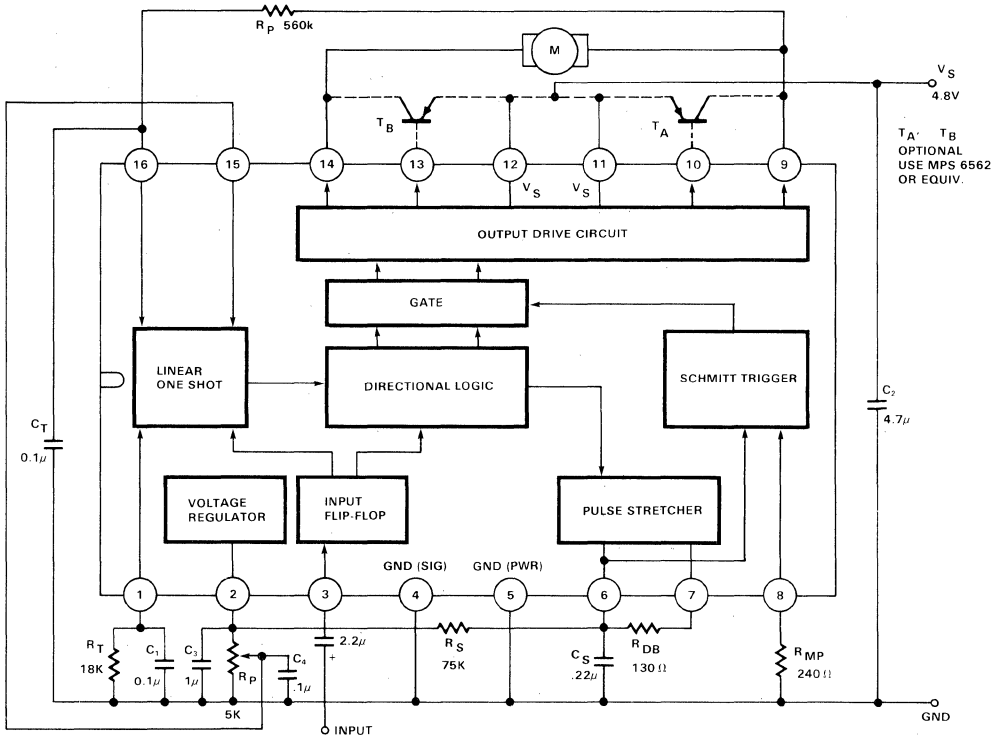


Typical PC Board Layout
Bottom View—4X



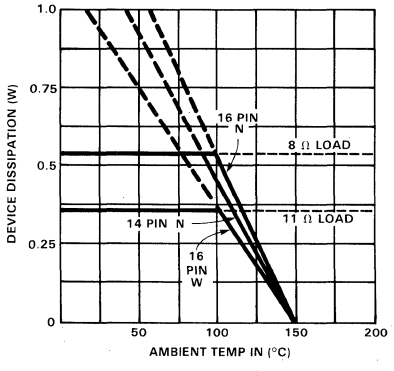
Parts Layout
Top View

TYPICAL CONNECTION OF NE644W AND NE644N FOR LINEAR ONE SHOT TIMING

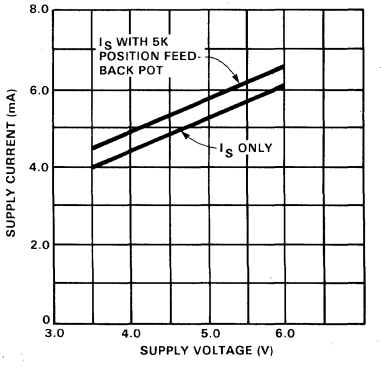


TYPICAL PERFORMANCE CHARACTERISTICS

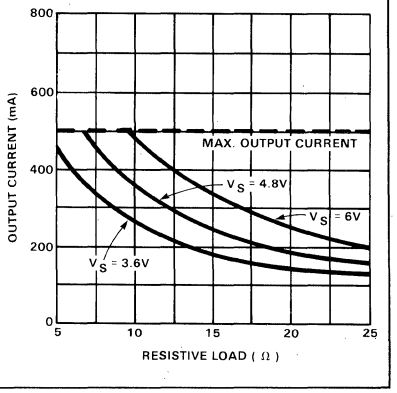
MAXIMUM DISSIPATION vs AMBIENT TEMPERATURE



SUPPLY CURRENT vs SUPPLY VOLTAGE

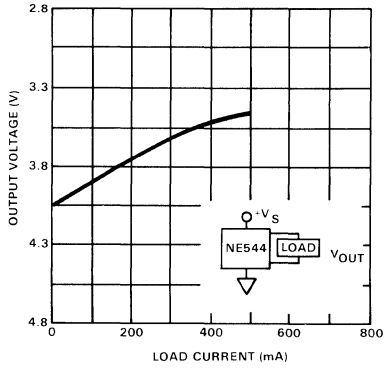


OUTPUT CURRENT vs LOAD RESISTANCE

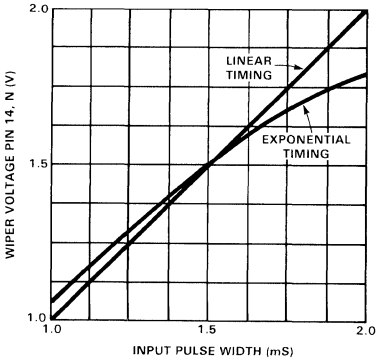


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

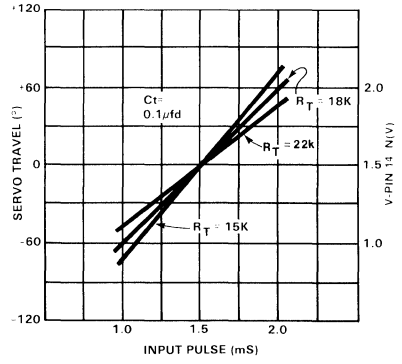
OUTPUT VOLTAGE vs LOAD CURRENT



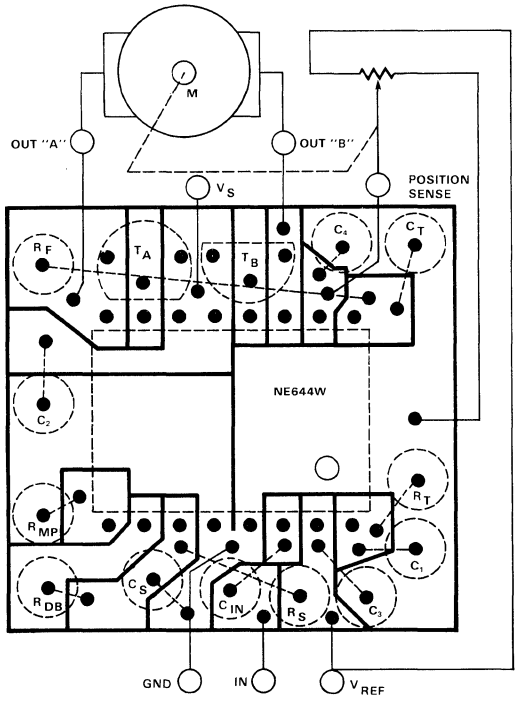
INPUT PULSE WIDTH vs FEEDBACK POT OUTPUT



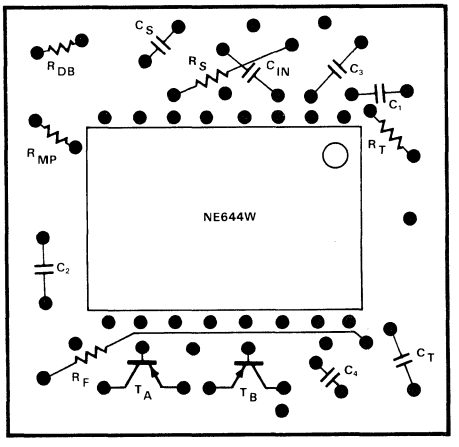
INPUT PULSE vs SERVO TRAVEL



PC BOARD—W PACKAGE



PC Board Layout
Bottom View—4X



Parts Layout
Top View

SECTION 16
PHASE LOCKED LOOPS

NE560-N

DESCRIPTION

The NE560 Phase Locked Loop (PLL) is a monolithic signal conditioner and demodulator system comprising a VCO, Phase Comparator, Amplifier and Low Pass Filter, interconnected as shown in the accompanying block diagram. The center frequency of the PLL is determined by the free running frequency (f_0) of the VCO. This VCO frequency is set by an external capacitor and can be fine tuned by an optional potentiometer. The low pass filter, which determines the capture characteristics of the loop, is formed by the two capacitors and two resistors at the Phase Comparator output.

The PLL system has a set of self biased inputs which can be utilized in either a differential or single ended mode. The VCO output, in differential form, is available for signal conditioning, frequency synchronization, multiplication and division applications. Terminals are provided for optional extended control of the tracking range, VCO frequency, and output dc level.

The monolithic signal conditioner-demodulator system is useful over a wide range of frequencies from less than 1Hz to more than 15MHz with an adjustable tracking range of ±1% to ±15%.

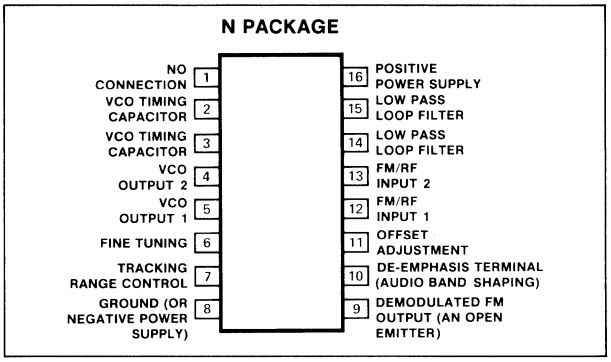
FEATURES

- **FM demodulation without tuned circuits**
- **Narrow bandpass: ± 14% adjustable**
- **Exact frequency duplication in high noise environment**
- **Wide tracking range: ± 15%**
- **High linearity: 1% distortion max**
- **Frequency multiplication and division**

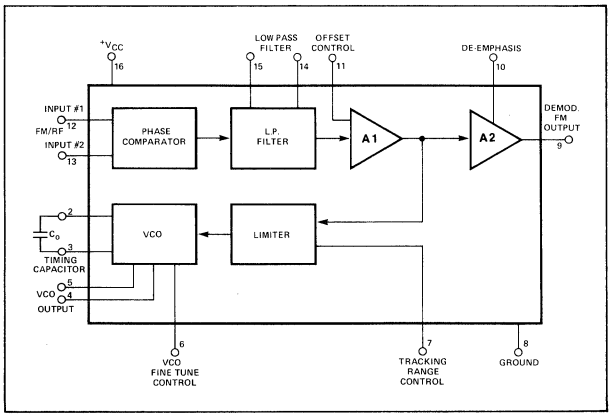
APPLICATIONS

- **Tone decoders**
- **FM IF strips**
- **Telemetry decoders**
- **Data synchronizers**
- **Signal reconstitution**
- **Signal generators**
- **Modems**
- **Tracking filters**
- **SCA receivers**
- **FSK receivers**
- **Wide band high linearity detectors**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Maximum operating voltage	26	V
Input voltage	1	Vrms
Storage temperature	-65 to +150	°C
Operating temperature	0 to +70	°C
Power dissipation	300	mW

NOTE

Limiting values above which serviceability may be impaired.

GENERAL ELECTRICAL CHARACTERISTICS

T_A = 25°C unless otherwise specified.[1]

PARAMETER	TEST CONDITIONS	NE560			UNIT
		Min	Typ	Max	
Lowest practical operating frequency			0.1		Hz
Maximum operating frequency		15	30		MHz
Supply current		7	9	12	mA
Minimum input signal for lock			100		μV
Dynamic range			60		dB
VCO Temp. coefficient[2]	Measured at 2MHz, with both inputs ac grounded.		±0.06	±0.12	%/°C
VCO Supply voltage regulation	Measured at 2MHz		±0.3	±2	%/V
Input resistance			2		kΩ
Input capacitance			4		pF
dc level (pins 14 & 15)		+10.6	+12	+13.4	V
Input dc level (pins 12 & 13)		+2.8	+4	+6.2	V
Output dc level (pin 10)		+12.5	+14	+17	V
(pin 9)		+12	+14	+16	V
Available output swing			4		V_{p-p}
AM rejection[2]		30	40		dB
De-emphasis resistance	Measured at pin 9 (see Figure 1)		8		kΩ

NOTES

1. 15KΩ Pin 9 to GND; input Pin 12 or Pin 13 (ac ground unused input); optional controls not connected; V+ = 18V unless otherwise specified.
2. Acceptance Test Sub Group C.

ELECTRICAL CHARACTERISTICS

FM Applications (see Figure 2)
T_A = 25°C, V+ = 18V unless otherwise specified.[1]

PARAMETER	TEST CONDITIONS	NE560			UNIT
		Min	Typ	Max	
10.7MHz OPERATION—DEVIATION 75kHz, SOURCE IMPEDANCE = 50Ω					
Detection threshold			120	300	μV
Demodulated output amplitude	V_{IN} = 1mVrms, modulation frequency 1kHz	30	60		mV
Distortion[2]	V_{IN} = 1mVrms, modulation frequency 1kHz		0.3	1	%T.H.D.
Signal to noise ratio $(\frac{S+N}{N})$	V_{IN} = 1mVrms, modulation frequency 1kHz		35		dB
4.5MHz OPERATION— DEVIATION = 25kHz, SOURCE IMPEDANCE = 50Ω					
Detection threshold			120	300	μV
Demodulation output amplitude	V_{IN} = 1mVrms, modulation frequency 1kHz	30	60		mV
Distortion[2]	V_{IN} = 1mVrms, modulation frequency 1kHz		0.3	1.0	%T.H.D.
Signal to noise ratio $(\frac{S+N}{N})$	V_{IN} = 1mVrms, modulation frequency 1kHz		35		dB
WIDE DEVIATION—$\Delta F/f_O$ = 5%, f_O = 4.5MHz, DEVIATION = 225kHz @ 1kHz MODULATION RATE					
Detection threshold			1	5	mV
Demodulated output	V_{IN} = 5mVrms	0.2	0.5		Vrms
Distortion[2]	V_{IN} = 5mVrms		0.8		%T.H.D.
Signal to noise ratio $(\frac{S+N}{N})$	V_{IN} = 5mVrms		50		dB

ELECTRICAL CHARACTERISTICS (Cont'd) Tracking Filter (see Figure 3)

$T_A = 25°C$, V+ = 18V unless otherwise specified.[1]

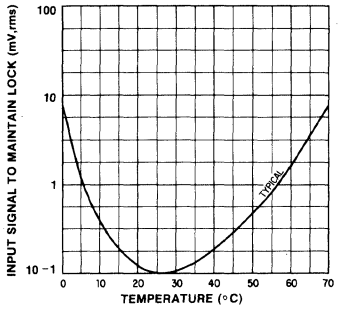
PARAMETER	TEST CONDITIONS	NE560			UNIT
		Min	Typ	Max	
Tracking range	V_{IN} = 5mVrms	±5	±15		% of f_o
Minimum signal to sustain lock	See typical performance characteristics		0.8		mVrms
VCO Output impedance	Measured with high impedance probe with less than 10pF capacitance		1		kΩ
VCO Output swing	with 100kHz sideband separation and 3kHz low pass filter.	0.4	0.6		V_{p-p}
VCO Output dc level	C_1 = .001μF, R_1 = 50Ω		+6.5		V
Side band suppression	Input = 1mV peak for carrier and each sideband.		35		dB

NOTES

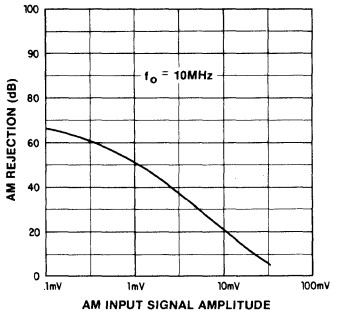
1. 15KΩ Pin 9 to GND; input Pin 12 or 13 (AC ground unused input); optional controls not connected.
2. Acceptance Test Sub Group C.

TYPICAL PERFORMANCE CHARACTERISTICS

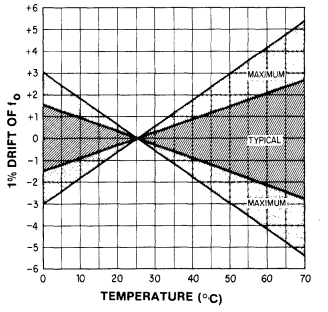
MINIMUM INPUT SIGNAL AMPLITUDE NECESSARY TO MAINTAIN LOCK AS A FUNCTION OF TEMPERATURE WITH $f_{IN} = f_o = 2.0MHz$



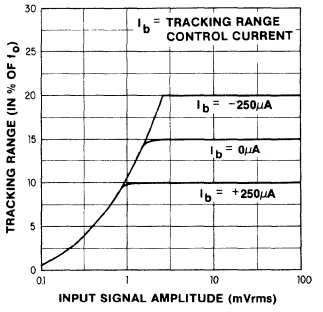
AM REJECTION AS A FUNCTION OF INPUT SIGNAL LEVEL



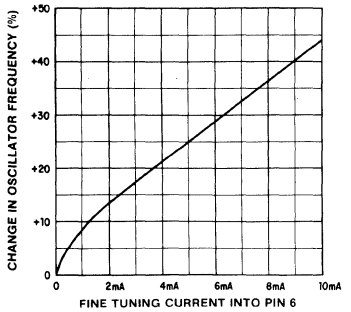
THERMAL DRIFT OF VCO FREE RUNNING FREQUENCY (fo)



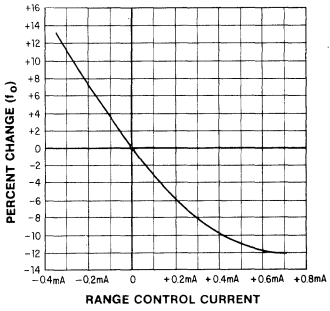
TYPICAL TRACKING RANGE AS A FUNCTION OF INPUT SIGNAL



CHANGE OF FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF FINE TUNING CURRENT

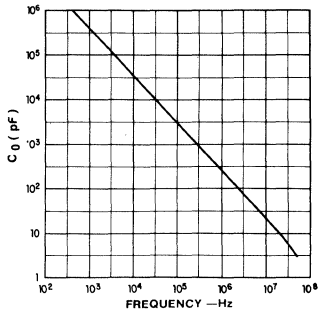


CHANGE OF FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF RANGE CONTROL CURRENT

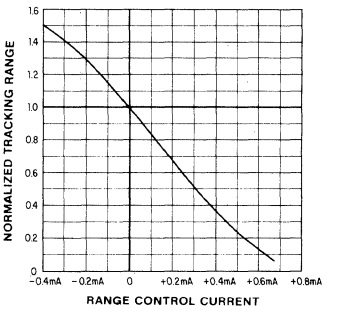


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF VCO TIMING CAPACITANCE



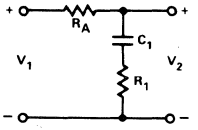
NORMALIZED TRACKING RANGE AS A FUNCTION OF RANGE CONTROL CURRENT



EXTERNAL CONTROLS

1. Loop Low Pass Filter (Pins 14 and 15)

The equivalent circuit for the loop low-pass filter can be represented as:



where R_A (6KΩ) is the effective resistance seen looking into pin 14 or pin 15.

The corresponding filter transfer characteristics are:

$$\frac{V_2}{V_1}(S) = \frac{1 + S\,R_1C_1}{1 + S(R_1 + R_A)C_1}$$

where S is the complex frequency variable.

2. Loop Gain (Threshold) Control

The overall phase locked loop gain can be reduced by connecting a feedback resistor, R_F, across the low-pass filter terminals, pins 14 and 15. This causes the loop gain and the detection sensitivity to decrease by a factor α, ($\alpha < 1$)

where:

$$\alpha = \frac{R_F}{2\,R_A + R_F}$$

Reduction of loop gain may be desirable at high input signal levels (V_{IN} > 30mV) and at high frequencies (f_o > 5MHz) where excessively high loop gain may cause instability.

3. Tracking Range Control (Pin 7)

Any bias current, I_b, injected into the tracking range control reduces the tracking range of the PLL by decreasing the output of the limiter. The variations of the tracking range and the center frequency, as a function of I_b, are shown in the characteristic curves with I_b defined positive going into the tracking range control terminal. This terminal is normally at a dc level of +0.6 volts and presents an impedance of 600Ω.

4. External Fine Tuning (Pin 6)

Any bias current injected into the fine tuning terminal increases the frequency of oscillation, f_o, as shown in the characteristic curves. This current is defined positive into the fine tuning terminal. This terminal is at a typical dc level of +1.3 volts and has a dynamic impedance of 100Ω to ground.

5. Offset Adjustment (Pin 11)

Application of a bias voltage to the offset adjustment terminal modifies the current in the output amplifier, setting the dc level at the output. The effect on the loop is to modify the relationship between the VCO free running frequency and the lock range, allowing the VCO free running frequency to be positioned at different points throughout the lock range.

Nominally this terminal is at +4Vdc and has an input impedance of 3kΩ. The offset adjustment is optional. The characteristics specified correspond to operation of the circuit with this terminal open circuited.

6. De-emphasis Filter (Pin 10)

The de-emphasis terminal is normally used when the PLL is used to demodulate frequency modulated audio signals. In this application, a capacitor from this terminal to ground provides the required de-emphasis. For other applications, this terminal may be used for band shaping the output signal. The 3dB bandwidth of the output amplifier (see Figure 2) is related to the de-emphasis capacitor, C_D, as:

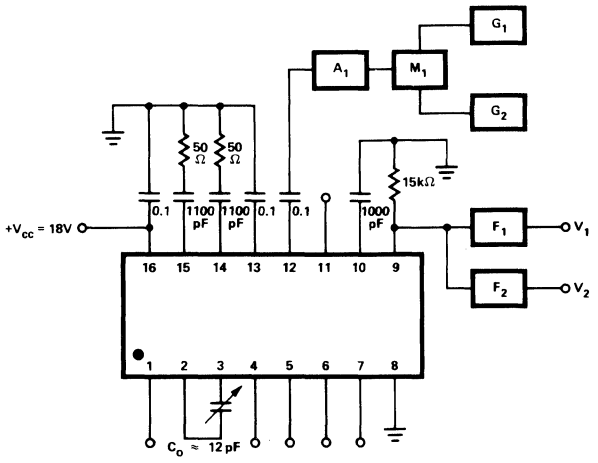
$$f_{3dB} = \frac{1}{2\pi R_D\,C_D}$$

where R_D is the 8000 ohm resistance seen looking into the de-emphasis terminal.

When the PLL system is utilized for signal conditioning, and the loop error voltage is not utilized, the de-emphasis terminal should be ac grounded.

TEST CIRCUITS

AM REJECTION



G_1 = FM Generator with $f_c = f_o \approx 4MHz$, $\Delta f = 40kHz$, $f_{mod} = 1kHz$

G_2 = Audio Generator with $f_A = 400Hz$

M_1 = Balanced Modulator Carrier Supplied by G_1, AM modulation provided by G_2.

A_1 = 50Ω attenuator pad with signal level into pin 12 adjusted to 1mVrms.

F_1 = 1kHz Bandpass filter, Q = 20

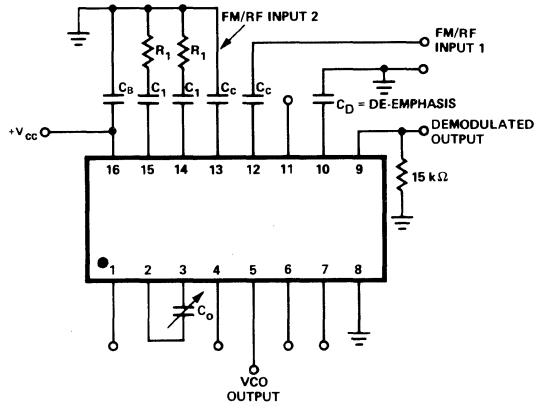
F_2 = 400Hz Bandpass filter with Q = 50, with 1kHz trap.

AMR = $\frac{V_1}{V_2}$ in dB

V_1 and V_2 are rms voltmeter readings.

Figure 1

FM DEMODULATION



C_B = Bypass Capacitor

C_C = Coupling Capacitors

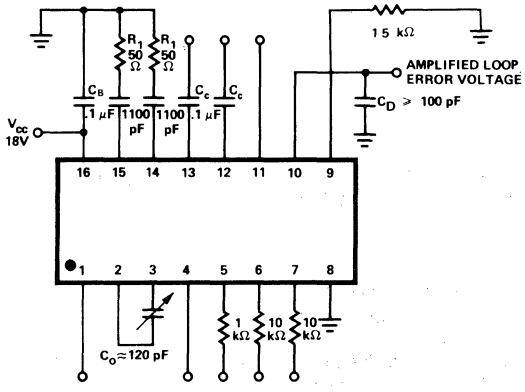
C_1 = Low Pass Filter Capacitors

C_0 = Frequency Determining Capacitor

T_d = De-emphasis time constant = (C_D) (8kΩ)

Figure 2

TRACKING FILTER
f_{IN} = 2MHz



C_C = Coupling Capacitors

C_B = Bypass Capacitor

C_1 = Low Pass Filter Capacitor

C_0 = VCO Frequency Set Capacitor

Figure 3

NE561-N

DESCRIPTION

The NE561 Phase Locked Loop (PLL) is a monolithic signal conditioner, and demodulator system comprising a VCO, Phase Comparator, Amplifier and Low Pass Filter, interconnected as shown in the accompanying block diagram. The center frequency of the PLL is determined by the free running frequency (f_0) of the VCO. This VCO frequency is set by an external capacitor and can be fine tuned by an optional potentiometer. The low pass filter, which determines the capture characteristics of the loop is formed by the two capacitors and two resistors at the Phase Comparator output.

The PLL system has a set of self biased inputs which can be utilized in either a differential or single ended mode. The VCO output is available for signal conditioning, frequency synchronization, multiplication and division applications. Terminals are provided for optional external control of the tracking range, VCO frequency, and output dc level. An analog multiplier block is incorporated into the PLL system to provide frequency selective synchronous AM detection capability.

The monolithic signal conditioner-demodulator system is useful over a wide range of frequencies from less than 1Hz to more than 15 MHz with an adjustable tracking range of ±1% to ±15%.

FEATURES

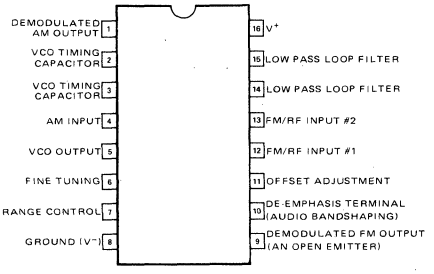
- **FM demodulation without tuned circuits**
- **Synchronous AM detection**
- **Narrow band pass to ±1%**
- **Exact frequency duplication in high noise environment**
- **Adjustable tracking range**
- **Wide tracking range to ±15%**
- **High linearity: 1% distortion max**
- **Frequency multiplication and division through harmonic locking**

APPLICATIONS

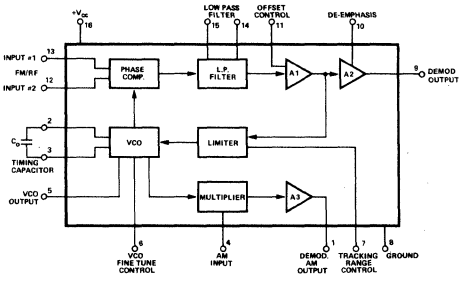
- **Tone decoders AM-FM-IF strips**
- **Telemetry decoders data synchronizers**
- **Signal reconstitution**
- **Signal generators**
- **Modems**
- **Tracking filters**
- **SCA receivers**
- **FSK receivers**
- **Wide bank high linearity detectors**
- **Synchronous detectors**
- **AM receiver**

PIN CONFIGURATION

N PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Maximum operating voltage	26	V
Input voltage	1	Vrms
Storage temperature	-65 to +150	°C
Operating temperature	0 to +70	°C
Power dissipation	300	mW

NE561-N

GENERAL ELECTRICAL CHARACTERISTICS

15kΩ pin 9 to GND; input pin 12 or pin 13 (AC ground unused input); optional controls not connected; $T_A = 25°C$, V+ = 18V unless otherwise specified.

PARAMETER		TEST CONDITIONS	NE561			UNIT
			Min	Typ	Max	
	Lowest practical operating frequency			0.1		Hz
	Maximum operating frequency		15	30		MHz
	Supply current		8	10	13	mA
	Minimum input signal for lock			100		μV
	Dynamic range			60		dB
VCO	Temp. coefficient*	Measured at 2MHz, with both inputs AC grounded		±0.06	±0.12	%/°C
VCO	Supply voltage regulation	Measured at 2MHz		±0.3	±2	%/V
	Input resistance			2		kΩ
	Input capacitance			4		pF
	Input dc level	Measured at pins 12 and 13	+2.8	+4	+6.0	V
		Measured at pins 14 and 15	+10.6	+12	+13.4	V
		Measured at pin 10	+13	+15	+17	V
	Output dc level	Measured at pin 9	+12	+14	+16	V
	Available output swing	Measured at pin 9		4		Vp-p
	AM rejection*	See Figure 3	30	40		dB
	De-emphasis resistance			8		kΩ

*NOTE

Acceptance Test Sub Group C.

ELECTRICAL CHARACTERISTICS

(for tracking filter, Figure 1). 15kΩ pin 9 to GND; input pin 12 or pin 13 (AC ground unused input); optional controls not connected; $T_A = 25°C$, V+ = 18V unless otherwise specified.

PARAMETER		TEST CONDITIONS	NE561			UNIT
			Min	Typ	Max	
	Tracking range	V_{IN} = 5mVrms	±5	±15		% of f_o
	Minimum signal to sustain lock			0.8		mVrms
VCO	Output impedance	Measured with high impedance probe with less than 10pF capacitance with ±100kHz side band separation and 3kHz low pass filter. $C_1 = .001\mu F$, $R_1 = 50\Omega$		1		kΩ
VCO	Output swing		0.4	0.6		Vp-p
VCO	Output dc level			+6.5		V
	Side band suppression	Input = 1mV peak for carrier and each side band		35		dB

ELECTRICAL CHARACTERISTICS

(for FM applications, Figure 2) 15kΩ pin 9 to GND; input pin 12 or 13 (AC ground unused input); optional controls not connected; $T_A = 25°C$, V+ = 18V unless otherwise specified.

PARAMETER	TEST CONDITIONS	NE561			UNIT
		Min	Typ	Max	
10.7MHz OPERATION— DEVIATION = 75kHz, SOURCE IMPEDANCE =50Ω					
Detection threshold			120	300	μV
Demodulated output amplitude	V_{IN} = 1mVrms, modulation frequency 1kHz	30	60		mV
Distortion*	V_{IN} = 1mVrms, modulation frequency 1kHz		.3	1	%T.H.D.
Signal to noise ratio $(\frac{S+N}{N})$	V_{IN} = 1mVrms, modulation frequency 1kHz		35		dB
4.5MHz OPERATION— DEVIATION = 25kHz; SOURCE IMPEDANCE = 50Ω					
Detection threshold			120	300	μV
Demodulation output amplitude	V_{IN} = 1mVrms, modulation frequency 1kHz	30	60		mV
Distortion*	V_{IN} = 1mVrms, modulation frequency 1kHz		0.3	1.0	%T.H.D.
Signal to noise ratio $(\frac{S+N}{N})$	V_{IN} = 1mVrms, modulation frequency 1kHz		35		dB
WIDE DEVIATION— $\Delta f/f_o = 5\%$, $f_o = 4.5$MHz, DEVIATION = 225kHz @ 1kHz MODULATION RATE					
Detection threshold			1	5	mV
Demodulated output	V_{IN} = 5mVrms	0.2	0.5		Vrms
Distortion*	V_{IN} = 5mVrms		0.8		%T.H.D.
Signal to noise ratio $(\frac{S+N}{N})$	V_{IN} = 5mVrms		50		dB

*NOTE

Acceptance Test Sub Group C.

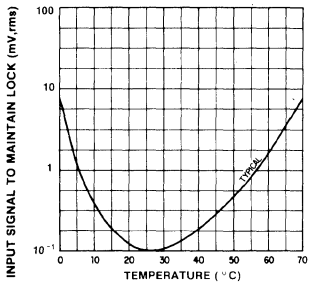
ELECTRICAL CHARACTERISTICS

(for AM synchronous detector, Figure 4). 15kΩ pin 9 to GND; input pin 12 or pin 13 (AC ground unused input); optional controls not connected; $T_A = 25°C$; V+ = 18V unless otherwise specified.

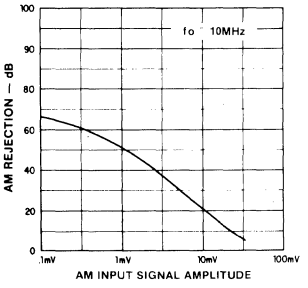
PARAMETER	NE561			UNIT
	Min	Typ	Max	
Input impedance		3		kΩ
Output impedance		8		kΩ
Output dc level	+10	+14	+17	V
AM conversion gain	3	12		dB
Out of band rejection		30		dB
Distortion		1		%T.H.D.

TYPICAL PERFORMANCE CHARACTERISTICS

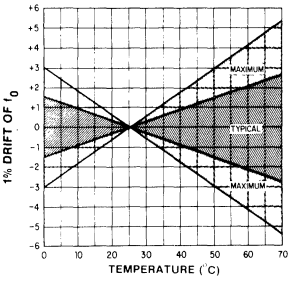
MINIMUM INPUT SIGNAL AMPLITUDE NECESSARY TO MAINTAIN LOCK AS A FUNCTION OF TEMPERATURE WITH $f_{in} = fo = 2.0MHz$



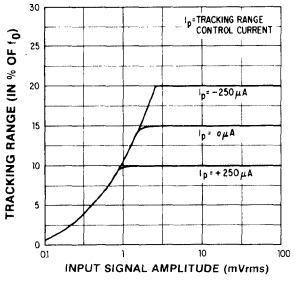
AM REJECTION AS A FUNCTION OF INPUT SIGNAL LEVEL



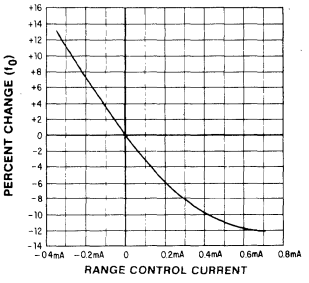
THERMAL DRIFT OF VCO FREE RUNNING FREQUENCY (fo)



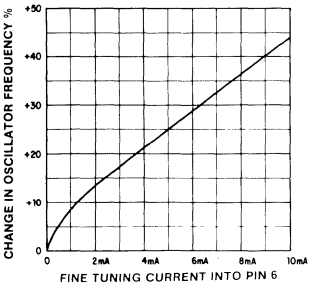
TYPICAL TRACKING RANGE AS A FUNCTION OF INPUT SIGNAL



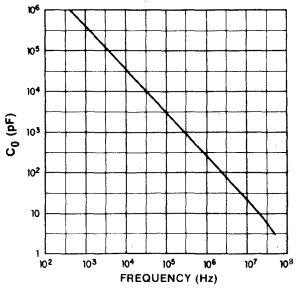
CHANGE OF FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF RANGE CONTROL CURRENT



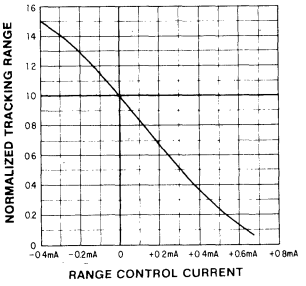
CHANGE OF FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF FINE TUNING CURRENT



FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF VCO TIMING CAPACITANCE



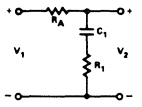
NORMALIZED TRACKING RANGE AS A FUNCTION OF RANGE CONTROL CURRENT



EXTERNAL CONTROLS

Loop Low Pass Filter (Pins 14 and 15)

The equivalent circuit for the loop low-pass filter can be represented as:



where R_A (6KΩ) is the effective resistance seen looking into pin 14 or pin 15.
The corresponding filter transfer characteristics are:

$$\frac{V_2}{V_1}(S) = \frac{1 + S\,R_1\,C_1}{1 + S\,(R_1 + R_A)\,C_1}$$

where S is the complex frequency variable.

Loop Gain (Threshold) Control

The overall phase lock loop gain can be reduced by connecting a feedback resistor, R_f across the low-pass filter terminals, pins 14 and 15. This causes the loop gain and the detection sensitivity to decrease by a factor α, ($\alpha < 1$), where:

$$\alpha = \frac{R_f}{2R_A + R_f}$$

Reduction of loop gain may be desirable at high input signal levels ($V_{IN} > 30mV$) and at high frequencies (fo > 5MHz) where excessively high PLL loop gain may cause instability.

Tracking Range Control (Pin 7)

Any bias current, I_b, injected into the tracking range control, reduces the tracking range of the PLL by decreasing the output of the limiter. The variation of the tracking range and the center frequency, as a function of I_b, are shown in the characteristics curves with I_b defined positive going into the tracking range control terminal. This terminal is normally at a dc level of +0.6 volts and presents an impedance of 600Ω.

External Fine Tuning (Pin 6)

Any bias current injected into the fine tuning terminal increases the frequency of oscillation, fo, as shown in the characteristic curves. This current is defined positive into the fine tuning terminal. This terminal is at a typical dc level of +1.3 volts and has a dynamic impedance of 100Ω to ground.

Offset Adjustment (Pin 11)

Application of a bias voltage to the offset adjustment terminal modifies the current in the output amplifier setting the dc level at the output. The effect on the loop is to modify the relationship between the VCO free running frequency and the lock range, allowing the VCO free running frequency to be positioned at different points throughout the lock range.

Nominally this terminal is at +4Vdc and has an input impedance of 3kΩ. The offset adjustment is optional. The characteristics specified correspond to operation of the circuit with this terminal open circuited.

De-emphasis Filter (Pin 10)

The de-emphasis terminal is normally used when the PLL is used to demodulate frequency modulated audio signals. In this application, a capacitor from this terminal to ground provides the required de-emphasis. For other applications, this terminal may be used for band shaping the output signal. The 3dB bandwidth of the output amplifier (see Figure 2) is related to the de-emphasis capacitor, C_D, as:

$$f_{3dB} = \frac{1}{2\pi R_D\,C_D}$$

where R_D is the 8000 ohm resistance seen looking into the de-emphasis terminal.

When the PLL system is utilized for signal conditioning, and the loop error voltage is not utilized, the de-emphasis terminal should be AC grounded.

AM Post-Detection Filter (Pin 1)

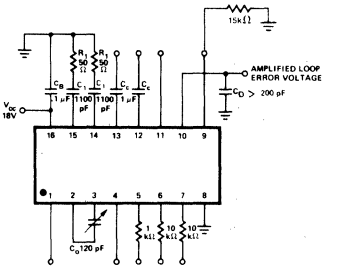
The capacitor Cx connected between Pin 1 and ground serves as low-pass filter for synchronous AM detection with a transfer characteristic, $F_2(S)$, given as:

$$F_2(S) = \frac{1}{1 + SR_x\,C_x}$$

where $R_x = 8k\Omega$ is the resistance seen looking into Pin 1.

TYPICAL TEST CIRCUITS

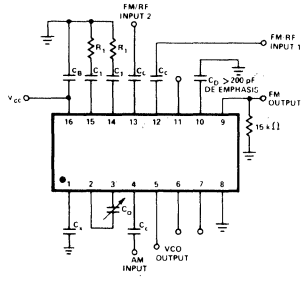
TEST CIRCUIT FOR TRACKING FILTER



C_C = Coupling capacitors
C_B = Bypass capacitor
C_1 = Low pass filter capacitor
C_0 = VCO frequency set capacitor

Figure 1

TEST CIRCUIT FOR FM DEMODULATION

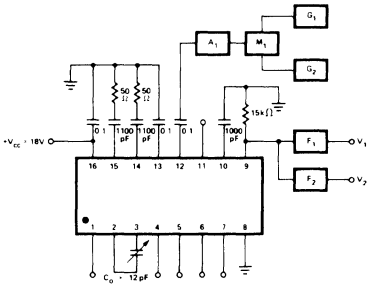


C_B = Bypass capacitor
C_C = Coupling capacitors
C_1 = Low pass filter capacitors
C_0 = Frequency determing capacitors
C_x = AM post detection filter

Figure 2

TYPICAL TEST CIRCUITS (Cont'd)

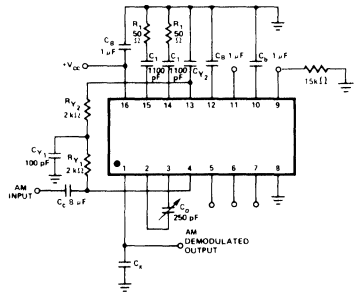
TEST CIRCUIT FOR AM REJECTION



G_1 = FM generator with $f_C = fo \approx 4MHz$
$\Delta f = 40kHz$, $f_{mod} = 1kHz$
G_2 = Audio generator with $f_A = 400kHz$
M_1 = Balanced modulator carrier supplied by G_1
AM modulation provided by G_2
A_1 = 50Ω attenuator pad with signal level into pin 12 adjusted to 1mVrms.
F_1 = 1kHz bandpass filter. Q = 20
F_2 = 400Hz bandpass filter with Q = 50, with 1kHz trap.
AMR = $\frac{V_1}{V_2}$ in dB V_1 and V_2 are rms voltmeter readings.

Figure 3

TEST CIRCUIT FOR AM SYNCHRONOUS DETECTOR



C_B = Bypass capacitor
C_C = Coupling capacitor
$R_{y1}C_{y1} = R_{y2}C_{y2} = \frac{1}{2\pi fo}$
C_x = AM post detection filter

Figure 4

NE562-N

DESCRIPTION

The NE562 Phase Locked Loop (PLL) is a monolithic signal conditioner and demodulator system comprising a VCO, phase comparator, amplifier and low pass filter, interconnected as shown in the accompanying block diagram. The center frequency of the PLL is determined by the free running frequency (f_o) of the VCO. This VCO frequency is set by an external capacitor. The low pass filter, which determines the capture characteristics of the loop, is formed by 2 capacitors and 2 resistors at the phase comparator output.

This PLL has 2 sets of differential inputs, one for the FM/RF input and one for the phase comparator local oscillator input. Both sets of inputs can be used in either a differential or single-ended mode. The FM/RF inputs to the comparator are self-biased. An internally regulated voltage source is provided to bias the phase comparator local oscillator inputs. The VCO output, at high level and in differential form, is available for driving logic circuits in signal conditioning and synchronization, frequency multiplication and division applications. Terminals are also provided for the optional extension of the tracking range.

The monolithic signal conditioner-demodulator system is useful over a wide range of frequencies from less than 1Hz to more than 15MHz with an adjustable tracking range of ±1% to ±15%.

FEATURES

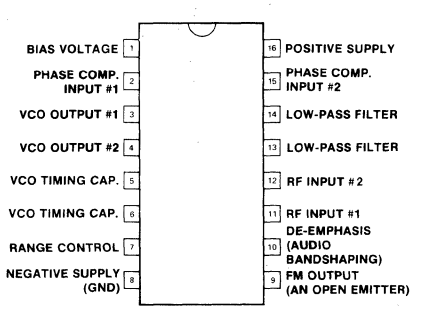
- **Frequency multiplication and division**
- **Signal conditioning and side-band suppression**
- **FM demodulation without tuned circuits**
- **Narrow bandpass to ±1%**
- **Adjustable tracking range to ±15%**
- **Exact frequency duplication in high noise environment**
- **High linearity: 1% distortion maximum at 1% deviation**

APPLICATIONS

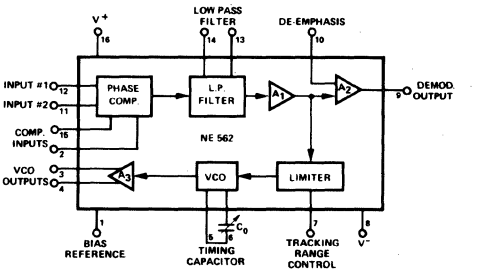
- **Frequency synthesizers**
- **Data synchronizers**
- **Signal conditioning**
- **Tracking filters**
- **Telemetry decoders**
- **Modems**
- **FM IF strips and demodulators**
- **Tone decoders**
- **FSK receivers**
- **Wideband high linearity FM demodulators**

PIN CONFIGURATION

N PACKAGE



BLOCK DIAGRAM

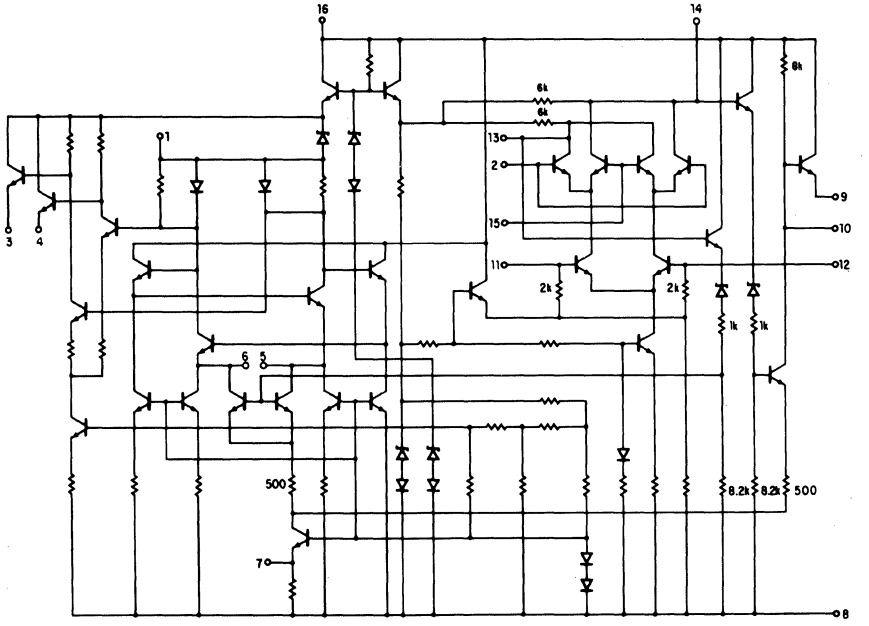


ABSOLUTE MAXIMUM RATINGS (Limiting values above which serviceability may be impaired)

PARAMETER	RATING	UNIT
Maximum operating voltage	30	V
Input voltage	3	Vrms
Storage temperature	-65 to +150	°C
Operating temperature	0 to +70	°C
Power dissipation	300	mW

NE562-N

EQUIVALENT SCHEMATIC



GENERAL ELECTRICAL CHARACTERISTICS

15,000 ohms pin 9 to ground; 12,000 ohms pins 3 and 4 to ground; pins 2 and 15 to pin 1 through 1,000 ohms; input to pin 11 or 12 with unused input at AC ground; range control not connected; $T_A = 25°C$, V+ = 18 volts unless otherwise specified.

PARAMETER	TEST CONDITIONS	NE562			UNIT
		Min	Typ	Max	
Lowest practical operating frequency			0.1		Hz
Maximum operating frequency		15	30		MHz
Supply current		10	12	15	mA
Minimum input signal for lock			200		μV
Dynamic range			80		dB
VCO temp. coefficient*	Measured at 2MHz		±0.06	±0.15	%/°C
VCO supply voltage regulation	Measured at 2MHz		±0.3	±2	%/V
Input resistance			2		kΩ
Input capacitance			4		pF
Input DC level	Measured at pins 11 and 12	+3	+4	+6	V
DC level	Measured at pins 13 and 14	+11	+13	+16	V
Output DC level	Measured at pin 9	+10	+12.5	+15	V
Available output swing	Measured at pin 9		4		Vp-p
AM rejection*		30	40		dB
De-emphasis resistance			8		kΩ
De-emphasis DC level	Measured at pin 10	+11	+14	+16	V
Bias reference	Measured at pin 1	+6.5	+7.5	+8.5	V

*NOTE

Acceptance test Sub Group C.

ELECTRICAL CHARACTERISTICS FOR FM APPLICATIONS

15,000 ohms pin 9 to ground; input to pin 11 or pin 12 (AC ground unused input); range control not connected; T_A = 25°C, V+ = 18 volts unless otherwise specified.

PARAMETER	TEST CONDITIONS	NE562			UNIT
		Min	Typ	Max	
10.7MHz OPERATION—DEVIATION = 75kHz, SOURCE IMPEDANCE = 50Ω					
Detection threshold			200	500	μV
Demodulated output amplitude	V_{IN} = 1mVrms, modulation frequency 1kHz	30	70		mVrms
Distortion*	V_{IN} = 1mVrms, modulation frequency 1kHz		0.5		%T.H.D.
Signal to noise ratio $(\frac{S+N}{N})$	V_{IN} = 1mVrms, modulation frequency 1kHz		35		dB
4.5MHz OPERATION—DEVIATION = 25kHz, SOURCE IMPEDANCE = 50Ω					
Detection threshold			200	500	μV
Demodulated output amplitude	V_{IN} = 1mVrms, modulation frequency 1kHz	30	60		mVrms
Distortion*	V_{IN} = 1mVrms, modulation frequency 1kHz		0.5		%T.H.D.
Signal to noise ratio $(\frac{S+N}{N})$	V_{IN} = 1mVrms, modulation frequency 1kHz		35		dB
WIDE DEVIATION—$\Delta f/f_o$ = 5%, INPUT = 4.5MHz, DEVIATION = 225kHz @ 1kHz MODULATION RATE					
Detection threshold			1	5	μV
Demodulated output	V_{IN} = 5mVrms		1		mVrms
Distortion*	V_{IN} = 5mVrms	0.3	0.8		%T.H.D.
Signal to noise ratio $(\frac{S+N}{N})$	V_{IN} = 5mVrms		50		dB

*NOTE

Acceptance test Sub Group C.

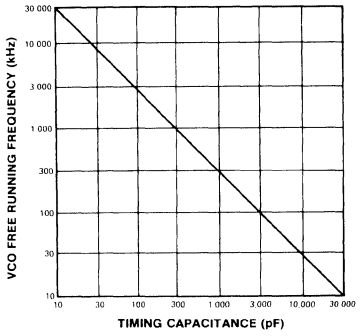
ELECTRICAL CHARACTERISTICS FOR SIGNAL CONDITIONER AND FREQUENCY SYNTHESIS APPLICATIONS

Input to pin 11 or pin 12; AC ground unused input; range control not connected; T_A = 25°C, V+ = 18 volts unless otherwise specified.

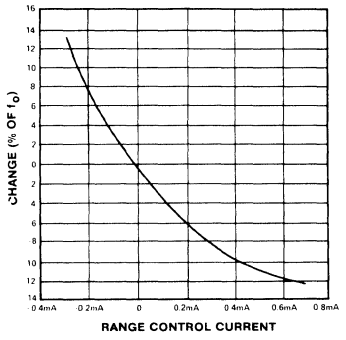
PARAMETER	TEST CONDITIONS	NE562			UNIT
		Min	Typ	Max	
Tracking range	200mVp-p square wave input	±5	±15		% of f_o
Input resistance			2		kΩ
Input capacitance			4		pF
Input DC level			4		V
VCO output impedance			1.3	2.5	kΩ
VCO output swing		3	4.5		Vp-p
VCO output DC level			12		V
VCO signal/noise ratio	Inputs at AC ground		60		dB

TYPICAL PERFORMANCE CHARACTERISTICS

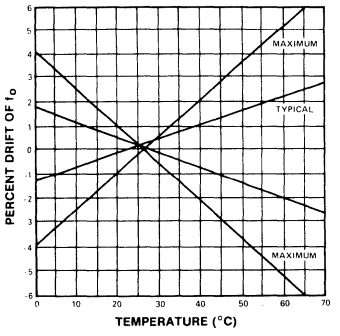
FREE RUNNING VOLTAGE CONTROLLED OSCILLATOR FREQUENCY AS A FUNCTION OF TIMING CAPACITANCE



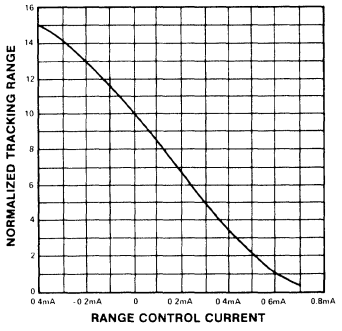
CHANGE OF FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF RANGE CONTROL CURRENT



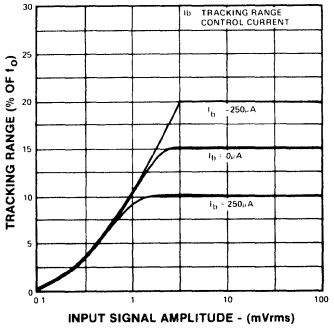
THERMAL DRIFT OF FREE RUNNING FREQUENCY AS A FUNCTION OF TEMPERATURE



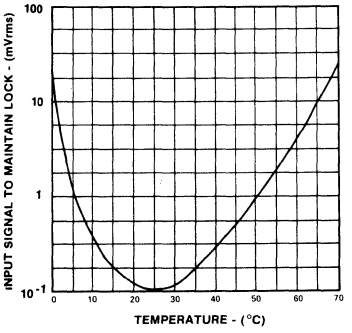
NORMALIZED TRACKING RANGE AS A FUNCTION OF RANGE CONTROL CURRENT



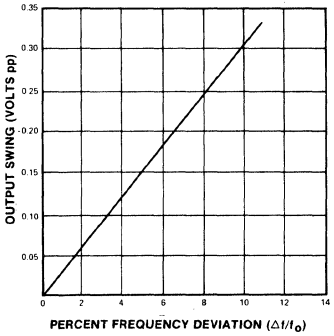
TYPICAL TRACKING RANGE AS A FUNCTION OF INPUT SIGNAL AMPLITUDE



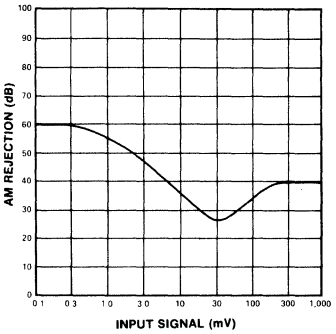
INPUT SIGNAL AMPLITUDE TO MAINTAIN LOCK AS A FUNCTION OF TEMPERATURE ($f_{IN} = f_O = 2.0$ MHz)



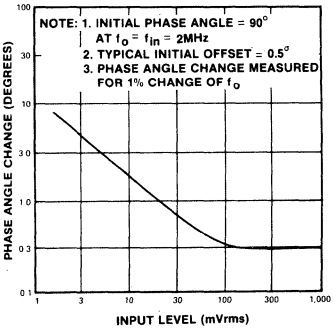
562 PHASE LOCKED LOOP DEMODULATED OUTPUT SWING AS A FUNCTION OF % FM DEVIATION



AM REJECTION AS A FUNCTION OF INPUT SIGNAL LEVEL

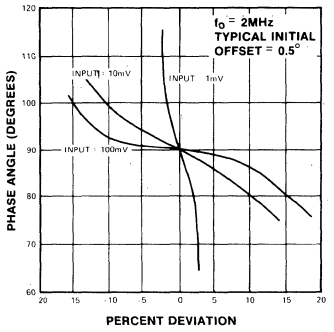


CHANGE IN PHASE ANGLE f_O RELATIVE TO f_{IN}, AS A FUNCTION OF INPUT SIGNAL AMPLITUDE

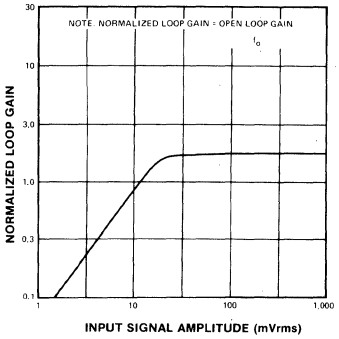


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

VCO OUTPUT PHASE AS A FUNCTION OF PERCENT FREQUENCY DEVIATION

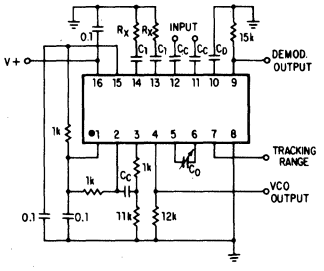


NORMALIZED LOOP GAIN AS A FUNCTION OF INPUT SIGNAL AMPLITUDE



TEST CIRCUITS

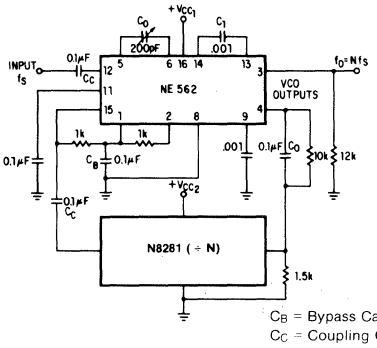
TEST CIRCUIT FOR FM DEMODULATION



C_B = Bypass Capacitor
C_C = Coupling Capacitor
C_1 = Low Pass Filter Capacitor
C_0 = Frequency Capacitor Set

Figure 1

TEST CIRCUIT FOR SIGNAL CONDITIONER AND FREQUENCY SYNTHESIS APPLICATIONS



NOTE: Fanout to divide by N counter is one.

C_B = Bypass Capacitor
C_C = Coupling Capacitor
C_1 = Low Pass Filter Capacitor
C_0 = Frequency Capacitor Set

Figure 2

562 APPLICATIONS INFORMATION

Bias Reference

Pin 1 of the 562 is an internally regulated bias reference voltage supply which should be used as a source of bias current for the phase comparator input terminals, pins 2 and 15. Biasing may be achieved as shown in Figure 3.

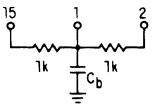


Figure 3

Phase Comparator Loop Inputs

The 562 has an open loop between the VCO and the phase comparator. Once biasing of the comparator is accomplished, as described in Bias Reference above, loop closure can be accomplished by capacitive coupling between either one or both inputs of the phase comparator and the VCO output. A divider or counter may be enclosed in the loop at this point for frequency synthesis applications or a flip-flop may be used to ensure that the output waveform has a 50% duty cycle. If large signal swings, greater than 2 volts, are to be applied to the phase comparator inputs, a limiting resistor should be used in series with the coupling capacitors to ensure that the maximum input voltage rating is not exceeded.

VCO Output

Square wave VCO outputs of both polarities (0° and 180°) buffered by an amplifier are available at pins 3 and 4. For proper operation of the buffer amplifier, pins 3 and 4 must be returned to ground (or the negative supply) through resistors, typically 12,000 ohms. The value of these resistors may be reduced provided that total power dissipated in the 562 does not exceed 300 milliwatts or the total average current in each emitter does not exceed 4mA. The output amplitude is typically 4.5 volts positive with respect to pin 8 (V+ = 12 volts).

VCO Tuning

Setting the free-running frequency of the VCO is accomplished easily with one timing capacitor connected between pins 5 and 6. For the 562 Phase Locked Loop, fine tuning of the free-running frequency may be accomplished in either or both of two ways. The first method uses a trimmer capacitor connected in parallel with the VCO timing capacitor. This is the simplest technique and requires the smallest number of extra components but at the lower frequencies may be difficult to implement. The second technique incorporates two resistors and a voltage source. The resistors are connected between each of the timing capacitor terminals and a voltage source as shown in Figure 4.

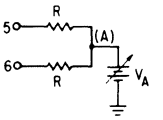


Figure 4

The percent change in the VCO free-running frequency, fo, as a function of the voltage applied to point (A) is shown in the curves of Figure 5. Note that with this fine tuning technique, it is possible to *increase* the VCO free-running frequency to a value greater than possible with just a trimmer capacitor alone. A formula for the approximation of the VCO frequency as a function of the voltage at point (A), the resistance values and the starting frequency, is given below:

$$f = f_o \left[1 - \frac{V_A - 6.4}{1300R}\right]$$

The recommended resistance range of R is 20,000 to 60,000 ohms.

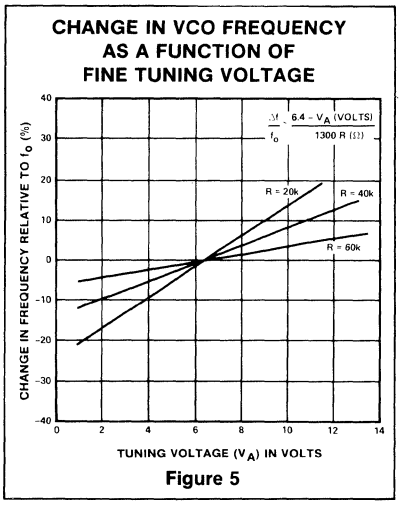


Figure 5

Loop Gain Characteristics

The overall open loop gain of the 562 PLL can be expressed as:

$K_0 = K_1 K_2$

where:

K_0= total open loop gain
K_1= phase comparator and amplifier conversion gain
K_2= VCO conversion gain

The VCO conversion gain, K_2, is the change of VCO frequency per unit of error voltage. In this particular design, it is numerically equal to the VCO frequency, i.e.,

$K_2 = f_o$ Hz/Volt

or

$K_2 = 2\pi f_o$ radians/Volt-second

The phase comparator and amplifier conversion gain, K_1, is proportional to input signal amplitude for low input levels, $V_s \leq$ 40mVrms, and is constant and equal to about 1.5 volts/radian for higher amplitudes. Therefore, K_1 can be approximated as:

$$K_1 \cong \frac{.04\ V_s}{\sqrt{1 + \left(\frac{V_s}{40}\right)^2}}$$

where

V_s = input signal in mVrms.

Signal Input

The input structure is basically differential and may be used in this manner. Biasing is supplied to the input terminals from an internal regulated supply so signal inputs must be capacitively coupled. In most applications where the input is single-ended, the unused input should be AC grounded.

Demodulated Output

Pin 9 is a low impedance output terminal for the loop error voltage. It is at this point that the demodulated FM output is obtained. When used, it must be biased by a resistor to ground (or negative supply), and the resistor value may be adjusted downward provided that the output current does not exceed 5mA or the dissipation in the 562 does not exceed the absolute maximum ratings. When not used, pin 9 may be left open.

De-emphasis Filter

The de-emphasis terminal, pin 10, is normally utilized when the PLL is used to demodulate frequency modulated audio signals. In this application, a capacitor from this terminal to ground provides the required de-emphasis. For other applications it may be used to shape the output response. The 3dB bandwidth of the output amplifier is related to the de-emphasis capacitor, C_D, as:

$$f_{3dB} = \frac{1}{2\pi\ R_D\ C_D}$$

where R_D is the 8000 ohms resistance seen looking into the de-emphasis terminal.

When the PLL system is utilized for applications not requiring the use of the output amplifier, pin 10 should be AC grounded.

562 APPLICATIONS INFORMATION (Cont'd)

Tracking Range Control (Pin 7)

Any bias current, I_b, injected into the tracking range control, reduces the tracking range of the PLL by decreasing the output of the limiter. The variation of the tracking range and the center frequency, as a function of I_b, are shown in the characteristic curves with I_b defined positive going into the tracking range control terminal. This terminal is normally at a DC level of +0.6 volts and presents an impedance of 600Ω.

Low Pass Filter

In most applications, a loop low-pass filter should be connected between pins 13 and 14 and ground. It is used to set the loop response time, controlling the capture range and the rejection of out-of-band information. Four filter configurations and their transfer functions are shown in Figures 6 through 9. For VCO operating frequencies below 5MHz, configurations shown in Figures 6 and 7 may be used. At higher frequencies, configurations shown in Figures 8 and 9 should be used to ensure loop stability. R is the internal resistance seen looking into the low pass filter terminals, Pins 13 and 14 and is nominally 6000 ohms.

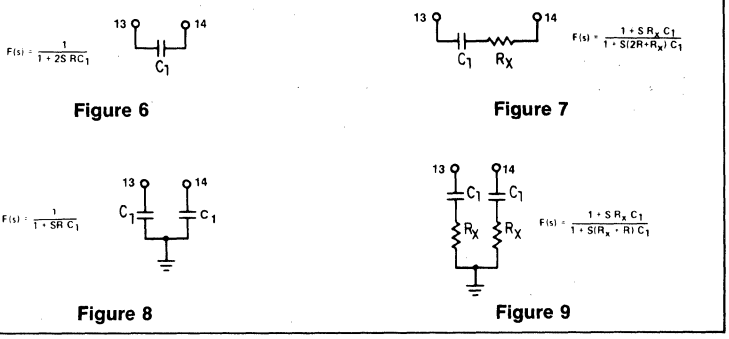


Figure 6

Figure 7

Figure 8

Figure 9

Loop Gain (Threshold) Control

The overall phase locked loop gain can be reduced by connecting a resistor, R_F, across the low-pass filter terminals, pins 13 and 14. This causes the loop gain and the detection sensitivity to decrease by a factor $\alpha, (\alpha < 1)$ where:

$$\alpha = \frac{R_F}{12{,}000 + R_F}$$

Reduction of loop gain may be desirable at operating frequencies greater than 5MHz because, at these frequencies, high loop gain may cause instability.

Static Loop Phase-Error

When the PLL is in lock, the VCO outputs have a nominal ±90° phase shift with respect to the input signal. Due to internal offsets, this nominal angle at perfect lock condition may shift a few degrees, typically ±5°.

NE564-N

DESCRIPTION

The NE564 is a versatile, high frequency Phase Locked Loop designed for operation up to 50MHz. As shown in the block diagram, the NE564 consists of a VCO, limiter, phase comparator, and post detection processor.

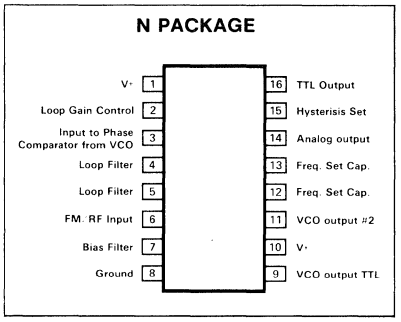
APPLICATIONS

- **High speed modems**
- **FSK receivers and transmitters**
- **Frequency synthesizers**
- **Signal generators**

FEATURES

- **Operation with single 5V supply**
- **TTL compatible inputs and outputs**
- **Operation to 50MHz**
- **Operates as a modulator**
- **External loop gain control**
- **Reduced carrier feedthrough**
- **No elaborate filtering needed in FSK applications**

PIN CONFIGURATION

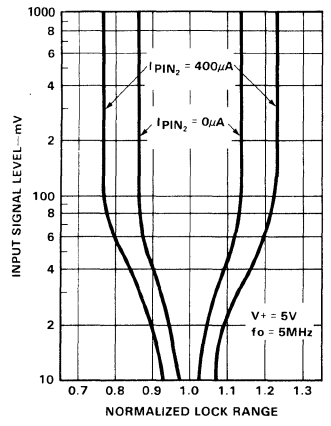


ABSOLUTE MAXIMUM RATINGS

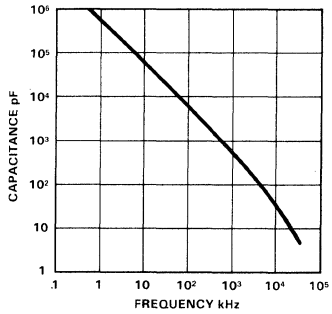
PARAMETER		RATING	UNIT
V+	Supply voltage		V
	Pin 1	14	
	Pin 10	6	
P_D	Power dissipation	400	mW
T_A	Operating temperature	0 to 70	°C
t_{stg}	Storage temperature	-65 to 150	°C

TYPICAL PERFORMANCE CHARACTERISTICS

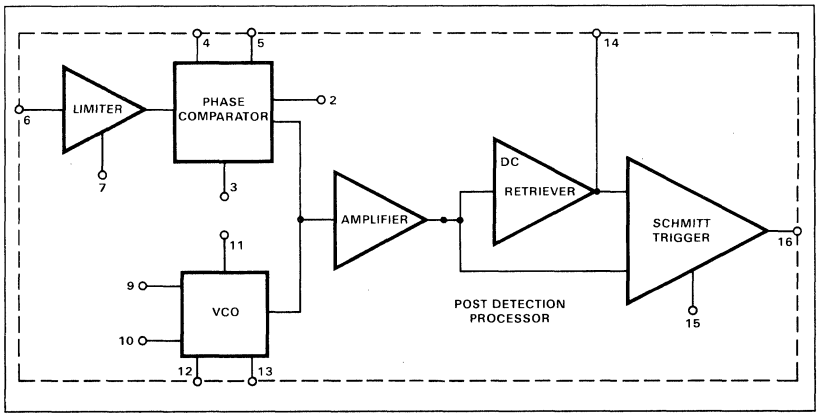
LOCK RANGE vs SIGNAL INPUT



VCO CAPACITOR vs FREQUENCY



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The NE564 is a monolithic phase locked loop with a post detection processor. The use of Schottky clamped transistors and optimized device geometries extends the frequency of operation to 50MHz. In addition to the classical PLL applications, the NE564 can be used as a modulator with a controllable frequency deviation.

The output voltage of the PLL can be written as shown in the following equation:

Equation 1

$$V_O = \frac{(f_{in} - f_o)}{K_{VCO}}$$

K_{VCO} = conversion gain of the VCO
f_{in} = frequency of the input signal
f_o = free running frequency of the VCO

The process of recovering FSK signals involves the conversion of the PLL output into digital, logic compatible signals. For high data rates, a considerable amount of carrier

DC ELECTRICAL CHARACTERISTICS V+ = 5V, T_A = 25°C unless otherwise specified

	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Lock range	T_A = 25°C, I_2 = 400μA	25	40		%
f_o	Frequency of operation of VCO		45	50		MHz
	Frequency drift with temperature	T_A = 0°C to 70°C, f_o = 5MHz		400	850	ppm/°C
	Frequency change with supply voltage	V+ = 4.5V to 5.5V		3	6	%/V
	Demodulated output voltage	± 1% input deviation	10	14		mVrms
		± 10% input deviation, f_o = 5MHz	100	140		
	Output voltage linearity			3		%
	Signal to noise ratio			40		dB
	AM rejection			35		dB
I_{CC}	Supply current	5V		30	40	mA
I_{LC}	Leakage current	Pin 9		1	10	μA
	Output current	Pin 9			6	mA
V+	Supply voltage	Pin 1	4.5		12	V
		Pin 10	4.5		5.5	

will be present at the output due to the the use of complicated filters, a comparator with hysterisis or Schmitt trigger is required. With the conversion gain of the VCO fixed, the output voltage as given by Equation 1 varies according to the frequency deviation of f_{in} from f_o. Since this differs from system to system, it is necessary that the hysterisis of the Schmitt trigger be capable of being changed, so that it can be optimized for a particular system. This is accomplished in the 564 by varying the voltage at pin 15 which results in a change of the hysterisis of the Schmitt trigger.

For FSK signals, an important factor to be considered is the drift in the free running frequency of the VCO itself. If this changes due to temperature, according to Equation 1 it will lead to a change in the dc levels of the PLL output, and consequently to errors in the digital output signal. This is especially true for narrow band signals where the deviation in f_{in} itself may be less than the change in f_o due to temperature. This effect can be eliminated if the dc or average value of the signal is retrieved and used as the reference to the comparator. In this manner, variations in the dc levels of the PLL output do not affect the FSK output.

VCO Section

Due to its inherent high frequency performance, an emitter coupled oscillator is used in the VCO. In the circuit, shown in the equivalent schematic, transistors Q_{21} and Q_{23} with current sources Q_{25}-Q_{26} form the basic oscillator. The free running frequency of the oscillator is shown in the following equation:

Equation 2

$$f_o = \frac{1}{16R_cC_1}$$

R_c = R_{19} = R_{20}
C_1 = frequency setting external capacitor

Variation of V_d changes the frequency of the oscillator. As indicated by Equation 2, the frequency of the oscillator has a negative temperature coefficient due to the positive temperature coefficient of the monolithic resistor. To compensate for this, a current I_R with negative temperature coefficient is introduced to achieve a low frequency drift with temperature.

Phase Comparator Section

The phase comparator consists of a double balanced modulator with a limiter amplifier to improve AM rejection. Schottky clamped vertical PNPs are used to obtain TTL level inputs. The loop gain can be varied changing the current in Q_4 and Q_{15} which effectively changes the gain of the differential amplifiers. This can be accomplished by introducing a current at pin 2.

Post Detection Processor Section

The post detection processor consists of a unity gain transconductance amplifier and comparator. The amplifier can be used as a dc retriever for demodulation of FSK signals, and as a post detection filter for linear FM demodulation. The comparator has adjustable hysterisis so that phase jitter in the output signal can be eliminated.

As shown in the equivalent schematic, the dc retriever is formed by the transconductance amplifier Q_{42}-Q_{43} with a capacitor at the output (pin 14). This forms an integrator whose output voltage is shown in the following equation:

Equation 3

$$V_0 = \frac{g_m}{C_2}\int V_{in}\,dt$$

g_m = transconductance of the amplifier
C_2 = capacitor at the output (pin 14)
V_{in} = signal voltage at amplifier input

With proper selection of C_2, the integrator time constant can be varied so that the output voltage is the dc or average value of the input signal for use in FSK, or as a post detection filter in linear demodulation.

The comparator with hysterisis is made up of Q_{49}-Q_{50} with positive feedback being provided by Q_{47}-Q_{48}. The hysterisis is varied by changing the current in Q_{52} with a resulting variation in the loop gain of the comparator. This method of hysterisis control, which is a dc control, provides symmetric variation around the nominal value.

Design Formula

Free running frequency of VCO is shown by the following equation:

Equation 4

$$f_O = \frac{1}{16 R_C C_1} \text{ in Hz}$$

$R_C = 100\,\Omega$

C_1 = external cap in farads

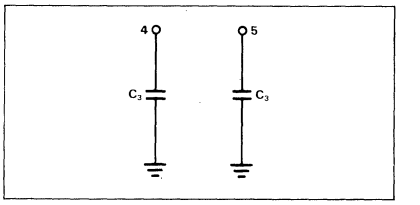
The loop filter diagram shown is explained by the following equation:

Equation 5

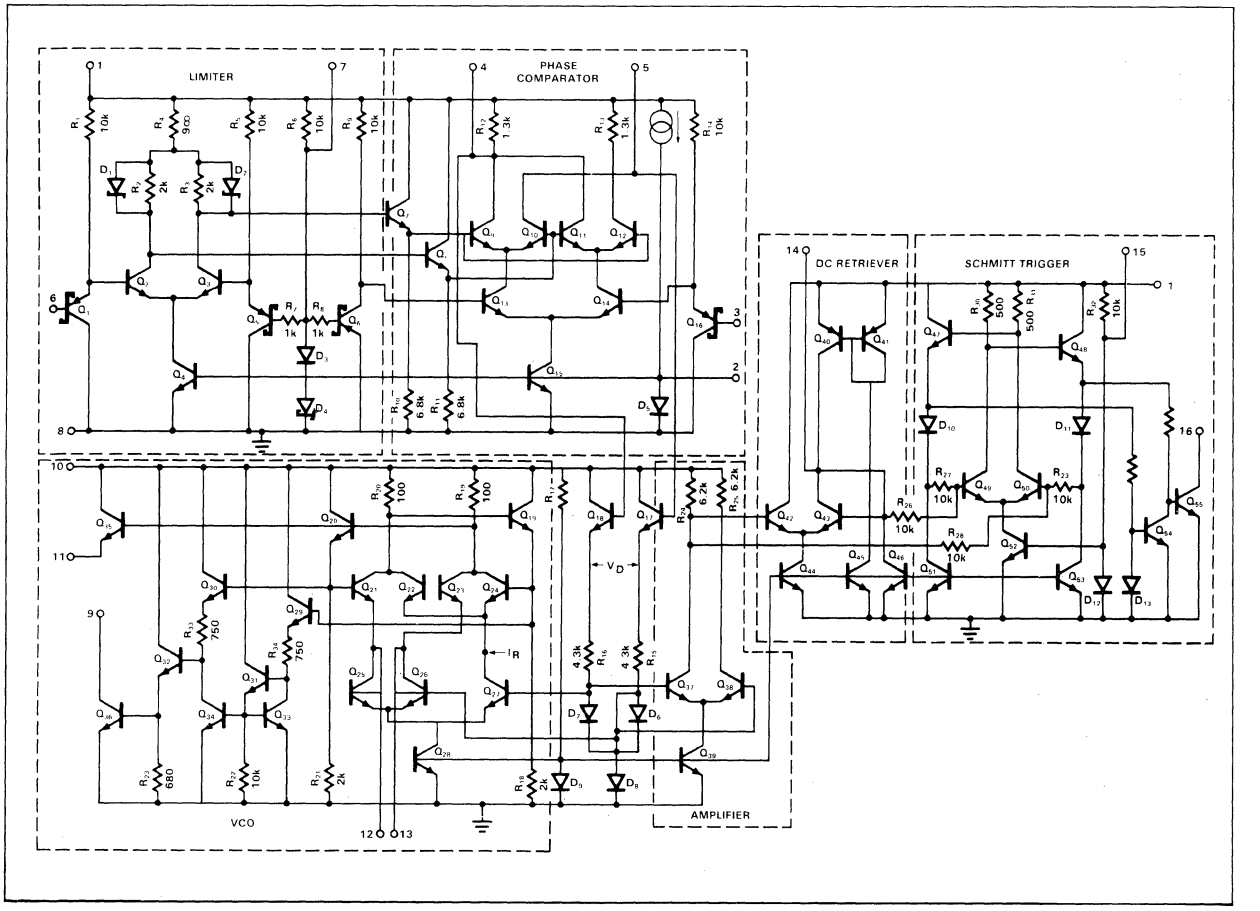
$$F(s) = \frac{1}{1 + sRC_3}$$

$R = R_{12} = R_{13} = 1.3\text{k}\,\Omega$

LOOP FILTER



EQUIVALENT SCHEMATIC



DESCRIPTION

The SE/NE565 Phase-Locked Loop (PLL) is a self-contained, adaptable filter and demodulator for the frequency range from 0.001Hz to 500kHz. The circuit comprises a voltage-controlled oscillator of exceptional stability and linearity, a phase comparator, an amplifier and a low-pass filter as shown in the block diagram. The center frequency of the PLL is determined by the free-running frequency of the VCO; this frequency can be adjusted externally with a resistor or a capacitor. The low-pass filter, which determines the capture characteristics of the loop, is formed by an internal resistor and an external capacitor.

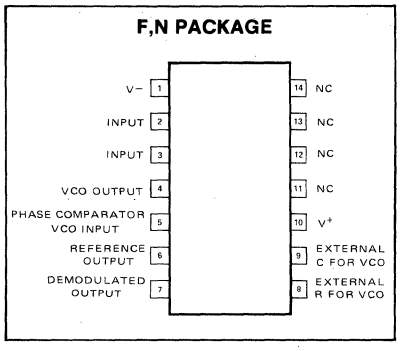
FEATURES

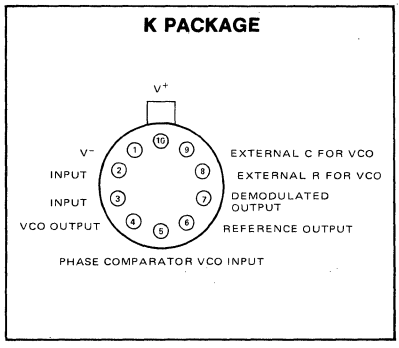
- **Highly stable center frequency (200ppm/°C typ.)**
- **Wide operating voltage range (±6 to ±12 volts)**
- **Highly linear demodulated output (0.2% typ.)**
- **Center frequency programming by means of a resistor or capacitor, voltage or current**
- **TTL and DTL compatible square-wave output; loop can be opened to insert digital frequency divider**
- **Highly linear triangle wave output**
- **Reference output for connection of comparator in frequency discriminator**
- **Bandwidth adjustable from < ±1% to > ±60%**
- **Frequency adjustable over 10 to 1 range with same capacitor**

APPLICATIONS

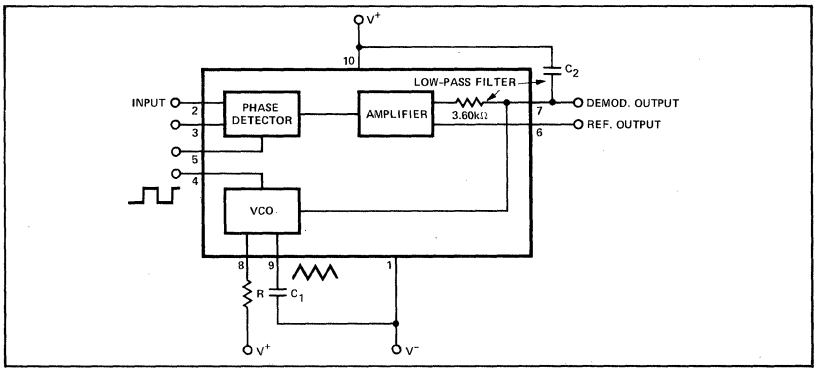
- **Frequency shift keying**
- **Modems**
- **Telemetry receivers**
- **Tone decoders**
- **SCA receivers**
- **Wideband FM discriminators**
- **Data synchronizers**
- **Tracking filters**
- **Signal restoration**
- **Frequency multiplication & division**

PIN CONFIGURATIONS

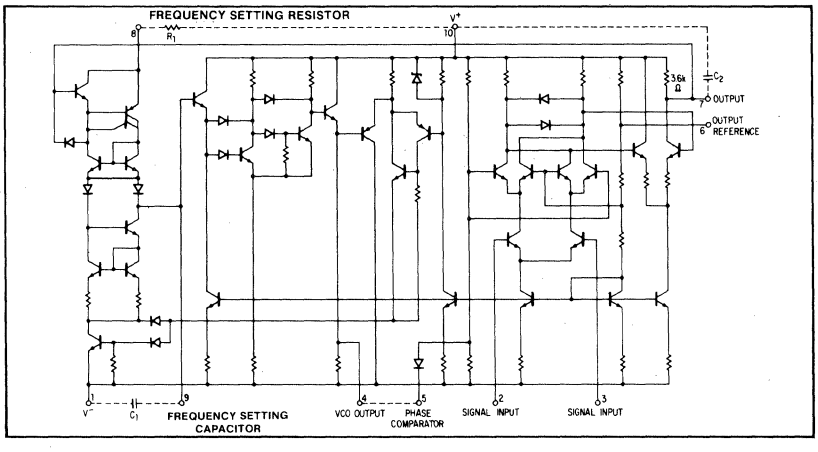




BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise specified.

PARAMETER	RATING	UNIT
Maximum operating voltage	26	V
Input voltage	3	Vp-p
Storage temperature	-65 to +150	°C
Operating temperature range		
NE565	0 to +70	°C
SE565	-55 to +125	°C
Power dissipation	300	mW

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = \pm 6V$ unless otherwise specified.

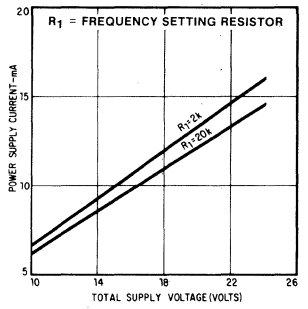
PARAMETER	TEST CONDITIONS	SE565			NE565			UNIT
		Min	Typ	Max	Min	Typ	Max	
SUPPLY REQUIREMENTS								
Supply voltage		±6		±12	±6		±12	V
Supply current			8	12.5		8	12.5	mA
INPUT CHARACTERISTICS								
Input impedance[1]		7	10		5	10		kΩ
Input level required for tracking	f_o = 50kHz, ±10% frequency deviation	10	1		10	1		mVrms
VCO CHARACTERISTICS								
Center frequency								
Maximum value	C_1 = 2.7pF	300	500			500		kHz
Distribution[2]	Distribution taken about f_o = 50kHz, R_1 = 5.0kΩ, C_1 = 1200pF	-10	0	+10	-30	0	+30	%
Drift with temperature	f_o = 50kHz		200	525		300		ppm/°C
Drift with supply voltage	f_o = 50kHz, V_{CC} = ±6 to ±7 volts		0.1	1.0		0.2	1.5	%/V
Triangle wave								
Output voltage level		1.9	0		1.9	0		V
Amplitude			2.4	3		2.4	3	Vp-p
Linearity			0.2			0.5		%
Square wave								
Logical "1" output voltage	f_o = 50kHz	+4.9	+5.2		+4.9	+5.2		V
Logical "0" output voltage	f_o = 50kHz		-0.2	+0.2		-0.2	+0.2	V
Duty cycle	f_o = 50kHz	45	50	55	40	50	60	%
Rise time			20	100		20		ns
Fall time			50	200		50		ns
Output current (sink)		0.6	1		0.6	1		mA
Output current (source)		5	10		5	10		mA
DEMODULATED OUTPUT CHARACTERISTICS								
Output voltage level	Measured at pin 7	4.25	4.5	4.75	4.0	4.5	5.0	V
Maximum voltage swing[3]			2			2		Vp-p
Output voltage swing	±10% frequency deviation	250	300		200	300		mVp-p
Total harmonic distortion			0.2	0.75		0.4	1.5	%
Output impedance[4]			3.6			3.6		kΩ
Offset voltage (V6-V7)			30	100		50	200	mV
Offset voltage vs temperature (drift)			50			100		μV/°C
AM rejection		30	40			40		dB

NOTES

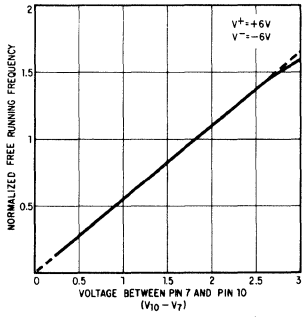
1. Both input terminals (pins 2 and 3) must receive identical dc bias. This bias may range from 0 volts to -4 volts.
2. The external resistance for frequency adjustment (R1) must have a value between 2kΩ and 20kΩ.
3. Output voltage swings negative as input frequency increases.
4. Output not buffered.

TYPICAL PERFORMANCE CHARACTERISTICS

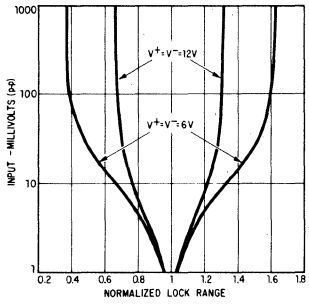
POWER SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



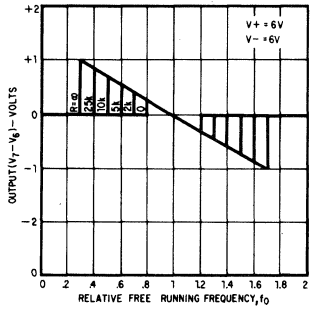
VCO CONVERSION GAIN



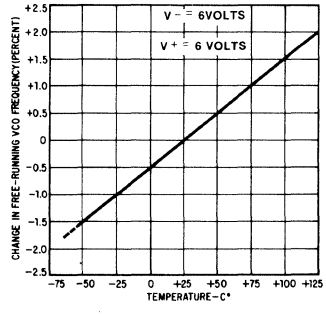
LOCK RANGE AS A FUNCTION OF INPUT VOLTAGE



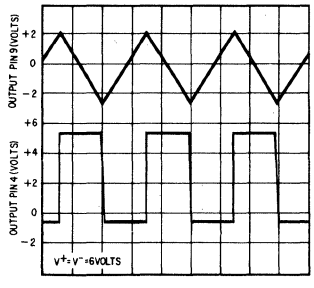
LOCK RANGE AS A FUNCTION OF GAIN SETTING RESISTANCE (PIN 6-7)



CHANGE IN FREE-RNNING VCO FREQUENCY AS A FUNCTION OF TEMPERATURE



VCO OUTPUT WAVEFORM



DESIGN FORMULAS (See Figure 1)

Free-running frequency of VCO: $f_o \simeq \frac{1.2}{4R_1C_1}$ in Hz

Lock-range: $f_L = \pm \frac{8f_o}{V_{CC}}$ in Hz

Capture-range: $f_C \simeq \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{\tau}}$

where $\tau = (3.6X10^3) \times C_2$

TYPICAL APPLICATIONS

FM Demodulation

The 565 Phase Locked Loop is a general purpose circuit designed for highly linear FM demodulation. During lock, the average dc level of the phase comparator output signal is directly proportional to the frequency of the input signal. As the input frequency shifts, it is this output signal which causes the VCO to shift its frequency to match that of the input. Consequently, the linearity of the phase comparator output with frequency is determined by the voltage-to-frequency transfer function of the VCO.

Because of its unique and highly linear VCO, the 565 PLL can lock to and track an input signal over a very wide bandwidth (typically ±60%) with very high linearity (typically, within 0.5%).

A typical connection diagram is shown in Figure 1. The VCO free-running frequency is given approximately by

$f_o = \frac{1.2}{4R_1C_1}$ and should be adjusted to be at the center of the input signal frequency range. C1 can be any value, but R1 should be within the range of 2000 to 20,000 ohms with an optimum value on the order of 4000 ohms. The source can be direct coupled if the dc resistances seen from pins 2 and 3 are equal and there is no dc voltage difference between the pins. A short between pins 4 and 5 connects the VCO to the phase comparator. Pin 6 provides a dc reference voltage that is close to the dc potential of the demodulated output (pin 7). Thus, if a resistance is connected between pins 6 and 7, the gain of the output stage can be reduced with little change in the dc voltage level at the output. This allows the lock range to be decreased with little change in the free-running frequency. In this manner the lock range can be decreased from ±60% of f_o to approximately ±20% of f_o (at ±6V).

A small capacitor (typically 0.001 μF) should be connected between pins 7 and 8 to eliminate possible oscillation in the control current source.

A single-pole loop filter is formed by the capacitor C2, connected between pin 7 and the positive supply, and an internal resistance of approximately 3600 ohms.

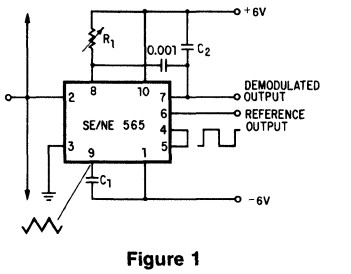


Figure 1

Frequency Shift Keying (FSK)

FSK refers to data transmission by means of a carrier which is shifted between two preset frequencies. This frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the "0" and "1" states (commonly called space and mark) of the binary data signal.

A simple scheme using the 565 to receive FSK signals of 1070Hz and 1270Hz is shown in Figure 2. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output.

The loop filter capacitor C2 is chosen smaller than usual to eliminate overshoot on the output pulse, and a three-stage RC ladder filter is used to remove the carrier component from the output. The band edge of the ladder filter is chosen to be approximately half way between the maximum keying rate (in this case 300 baud or 150Hz) and twice the input frequency (approximately 2200Hz). The output signal can now be made logic compatible by connecting a voltage comparator between the output and pin 6 of the loop. The free-running frequency is adjusted with R1 so as to result in a slightly-positive voltage at the output with f_{IN} = 1070Hz.

The input connection is typical for cases where a dc voltage is present at the source and therefore a direct connection is not desirable. Both input terminals are returned to ground with identical resistors (in this case, the values are chosen to effect a 600-ohm input impedance).

Frequency Multiplication

There are two methods by which frequency multiplication can be achieved using the 565:

1. Locking to a harmonic of the input signal.
2. Inclusion of a digital frequency divider or counter in the loop between the VCO and phase comparator.

The first method is the simplest, and can be achieved by setting the free-running frequency of the VCO to a multiple of the input frequency. A limitation of this scheme is that the lock range decreases as successively higher and weaker harmonics are used for locking. If the input frequency is to be constant with little tracking required, the loop can generally be locked to any one of the first 5 harmonics. For higher orders of multiplication, or for cases where a large lock range is desired, the second scheme is more desirable. An example of this might be a case where the input signal varies over a wide frequency range and a large multiple of the input frequency is required.

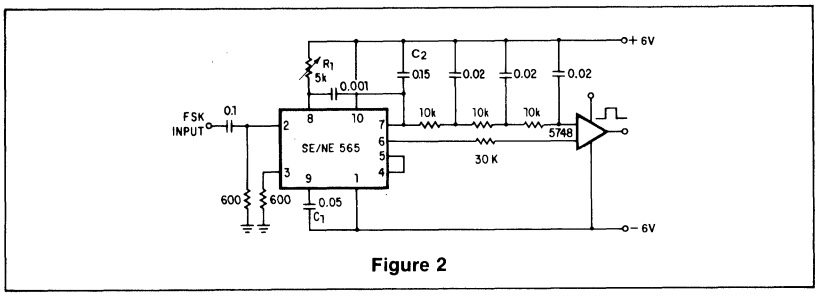


Figure 2

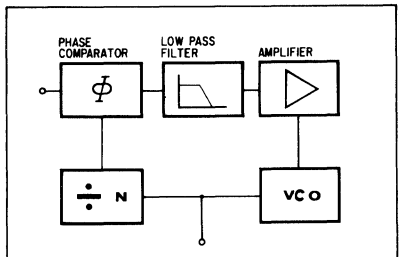


Figure 3

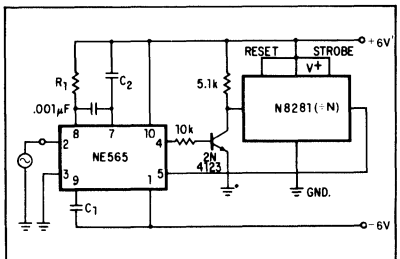


Figure 4

A block diagram of the second scheme is shown in Figure 3. Here the loop is broken between the VCO and the phase comparator, and a frequency divider is inserted. The fundamental of the divided VCO frequency is locked to the input frequency in this case, so that the VCO is actually running at a multiple of the input frequency. The amount of multiplication is determined by the frequency divider. A typical connection scheme is shown in Figure 4. To set up the circuit, the frequency limits of the input signal must be determined. The free-running frequency of the VCO is then adjusted by means of R1 and C1 (as discussed under FM demodulation) so that the output frequency of the divider is midway between the input frequency limits. The filter capacitor, C2, should be large enough to eliminate variations in the demodulated output voltage (at pin 7), in order to stabilize the VCO frequency. The output can now be taken as the VCO squarewave output, and its fundamental will be the desired multiple of the input frequency (f_{IN}) as long as the loop is in lock.

SCA (Background Music) Decoder

Some FM stations are authorized by the FCC to broadcast uninterrupted background music for commerical use. To do this a frequency modulated subcarrier of 67kHz is used. The frequency is chosen so as not to interfere with the normal stereo or monaural program; in addition, the level of the subcarrier is only 10% of the amplitude of the combined signal.

The SCA signal can be filtered out and demodulated with the NE565 Phase Locked Loop without the use of any resonant circuits. A connection diagram is shown in Figure 5. This circuit also serves as an example of operation from a single power supply.

A resistive voltage divider is used to establish a bias voltage for the input (pins 2 and 3). The demodulated (multiplex) FM signal is fed to the input through a two-stage high-pass filter, both to effect capacitive coupling and to attenuate the strong signal of the regular channel. A total signal amplitude, between 80mV and 300mV, is required at the input. Its source should have an impedance of less than 10,000 ohms.

The Phase Locked Loop is tuned to 67kHz with a 5000 ohm potentiometer; only approximate tuning is required, since the loop will seek the signal.

The demodulated output (pin 7) passes through a three-stage low-pass filter to provide de-emphasis and attenuate the high-frequency noise which often accompanies SCA transmission. Note that no capacitor is provided directly at pin 7; thus, the circuit is operating as a first-order loop. The demodulated output signal is in the order of 50mV and the frequency response extends to 7kHz.

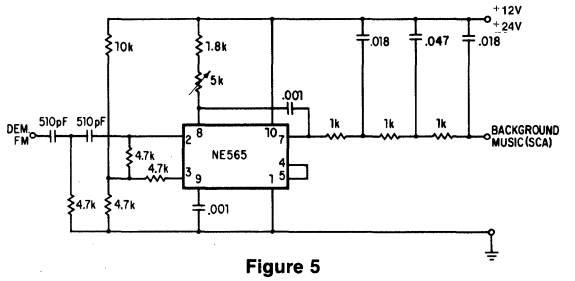

+12V
+24V
10k
1.8k
5k
.001
.018
.047
.018
DEM FM
510pF
510pF
2
8
10
7
1k
1k
1k
BACKGROUND MUSIC (SCA)
4.7k
4.7k
NE565
3
9
4
5
1
4.7k
4.7k
.001

Figure 5

NE/SE566-F,N,T

DESCRIPTION

The SE/NE 566 Function Generator is a voltage controlled oscillator of exceptional linearity with buffered square wave and triangle wave outputs.The frequency of oscillation is determined by an external resistor and capacitor and the voltage applied to the control terminal. The oscillator can be programmed over a ten to one frequency range by proper selection of an external resistance and modulated over a ten to one range by the control voltage, with exceptional linearity.

FEATURES

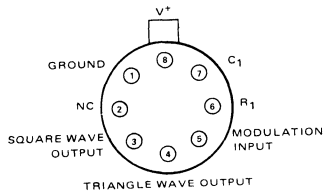
- **Wide range of operating voltage (up to 24 volts)**
- **High linearity of modulation**
- **Highly stable center frequency (200 ppm/°C typical)**
- **Highly linear triangle wave output**
- **Frequency programming by means of a resistor or capacitor, voltage or current**
- **Frequency adjustable over 10 to 1 range with same capacitor**

APPLICATIONS

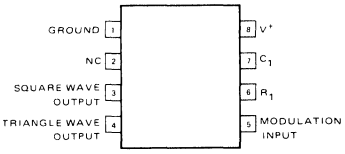
- **Tone generators**
- **Frequency shift keying**
- **FM modulators**
- **Clock generators**
- **Signal generators**
- **Function generators**

PIN CONFIGURATIONS

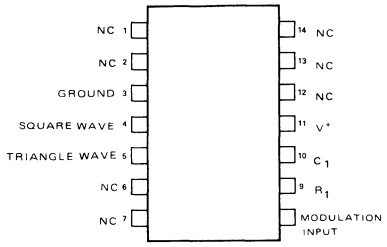
T PACKAGE



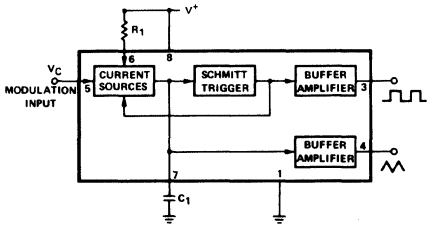
N PACKAGE



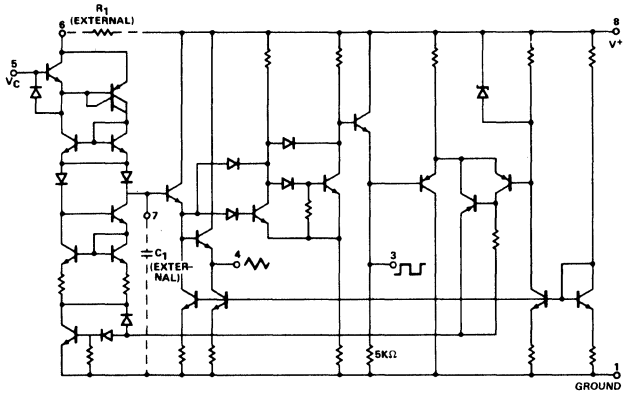
F PACKAGE



BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Maximum operating voltage	26	V
Input voltage	3	V_{P-P}
Storage temperature	-65 to +150	°C
Operating temperature range		
NE566	0 to +70	°C
SE566	-55 to +125	°C
Power dissipation	300	mW

NE/SE566-F,N,T

ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = 12V$ unless otherwise specified.

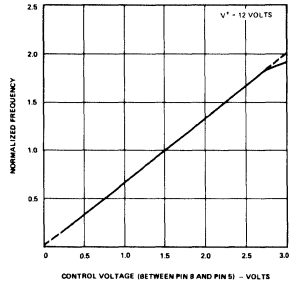
PARAMETER	SE566			NE566			UNIT
	Min	Typ	Max	Min	Typ	Max	
GENERAL							
Operating temperature range	-55		125	0		70	°C
Operating supply voltage			24			24	V
Operating supply current		7	12.5		7	12.5	mA
VCO[1]							
Maximum operating frequency		1			1		MHz
Frequency drift with temperature		200			300		ppm/°C
Frequency drift with supply voltage		1			2		%/V
Control terminal input impedance[2]		1			1		MΩ
FM distortion (±10% deviation)		0.2	0.75		0.4	1.5	%
Maximum sweep rate		1			1		MHz
Sweep range		10:1			10:1		
OUTPUT							
Triangle wave output							
Impedance		50			50		Ω
Voltage	1.9	2.4		1.9	2.4		Vpp
Linearity		0.2			0.5		%
Square wave input							
Impedance		50			50		Ω
Voltage	5	5.4		5	5.4		Vpp
Duty Cycle	45	50	55	40	50	60	%
Rise time		20			20		ns
Fall Time		50			50		ns

NOTES

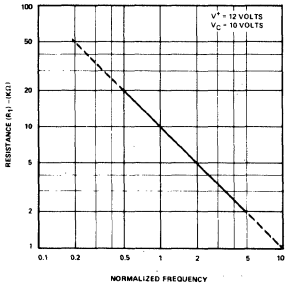
1. The external resistance for frequency adjustment (R_1) must have a value between 2kΩ and 20KΩ.
2. The bias voltage (V_C) applied to the control terminal (pin 5) should be in the range $3/4V^+ \leq V_C \leq V^+$.

TYPICAL PERFORMANCE CHARACTERISTICS

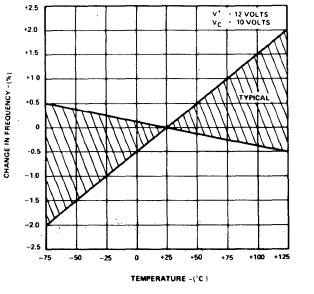
NORMALIZED FREQUENCY AS A FUNCTION OF CONTROL VOLTAGE



NORMALIZED FREQUENCY AS A FUNCTION OF RESISTANCE (R1)

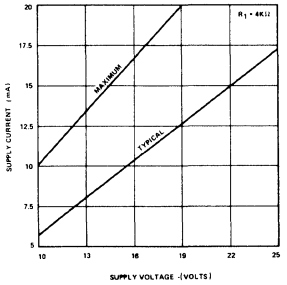


CHANGE IN FREQUENCY AS A FUNCTION OF TEMPERATURE

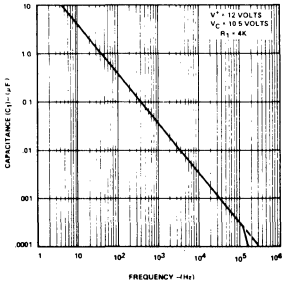


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

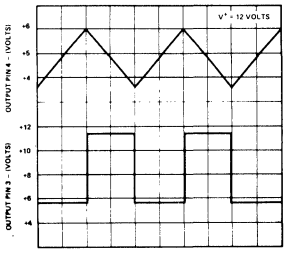
POWER SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



FREQUENCY AS A FUNCTION OF CAPACITANCE (C1)



VCO OUTPUT WAVEFORMS



OPERATING INSTRUCTIONS

The SE/NE 566 Function Generator is a general purpose voltage controlled oscillator designed for highly linear frequency modulation. The circuit provides simultaneous square wave and triangle wave outputs at frequencies up to 1MHz. A typical connection diagram is shown in Figure 1. The control terminal (pin 5) must be biased externally with a voltage (V_C) in the range

$$3/4\ V^+ \leq V_C \leq V^+$$

where V_{CC} is the total supply voltage. In Figure 1, the control voltage is set by the voltage divider formed with R_2 and R_3. The modulating signal is then ac coupled with the capacitor C_2. The modulating signal can be direct coupled as well, if the appropriate dc bias voltage is applied to the control terminal. The frequency is given approximately by

$$f_o \simeq \frac{2[(V^+) - (V_C)]}{R_1 C_1 V^+}$$

and R_1 should be in the range $2k\Omega < R_1 < 20k\Omega$.

A small capacitor (typically $0.001\mu f$) should be connected between pins 5 and 6 to eliminate possible oscillation in the control current source.

If the VCO is to be used to drive standard logic circuitry, it may be desirable to use a dual supply of ±5 volts as shown in Figure 2. In this case the square wave output has the proper dc levels for logic circuitry. RTL can be driven directly from pin 3. For DTL or T²L gates, which require a current sink of more than 1mA, it is usually necessary to connect a $5k\Omega$ resistor between pin 3 and negative supply. This increases the current sinking capability to 2mA. The third type of interface shown uses a saturated transistor between the 566 and the logic circuitry. This scheme is used primarily for T²L circuitry which requires a fast fall time (<50ns) and a large current sinking capability.

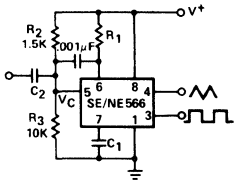


FIGURE 1

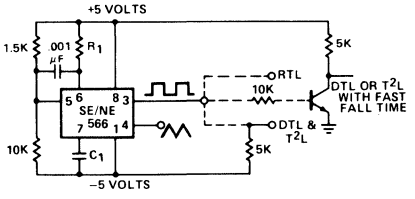


FIGURE 2

NE/SE567-F,N,T

DESCRIPTION

The SE/NE567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth center frequency, and output delay are independently determined by means of four external components.

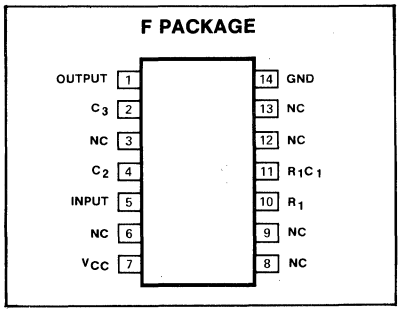
FEATURES

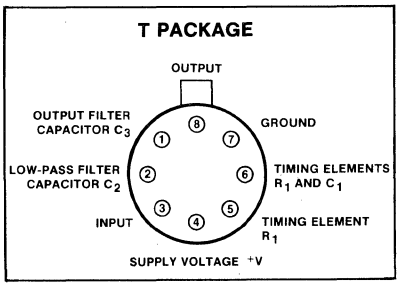
- **Wide frequency range (.01Hz to 500kHz)**
- **High stability of center frequency**
- **Independently controllable bandwidth (up to 14 percent)**
- **High out-band signal and noise rejection**
- **Logic-compatible output with 100mA current sinking capability**
- **Inherent immunity to false signals**
- **Frequency adjustment over a 20 to 1 range with an external resistor**
- **Military processing available**

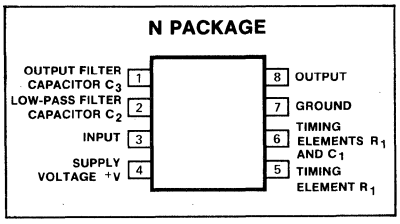
APPLICATIONS

- **Touch Tone® decoding**
- **Carrier current remote controls**
- **Ultrasonic controls (remote TV, etc.)**
- **Communications paging**
- **Frequency monitoring and control**
- **Wireless intercom**
- **Precision oscillator**

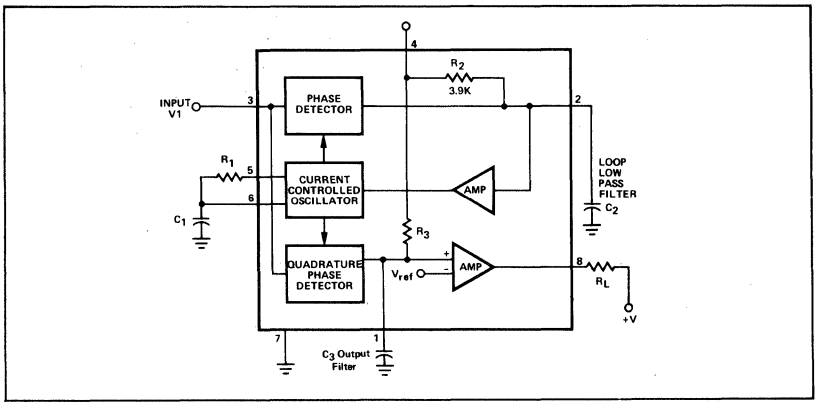
PIN CONFIGURATIONS







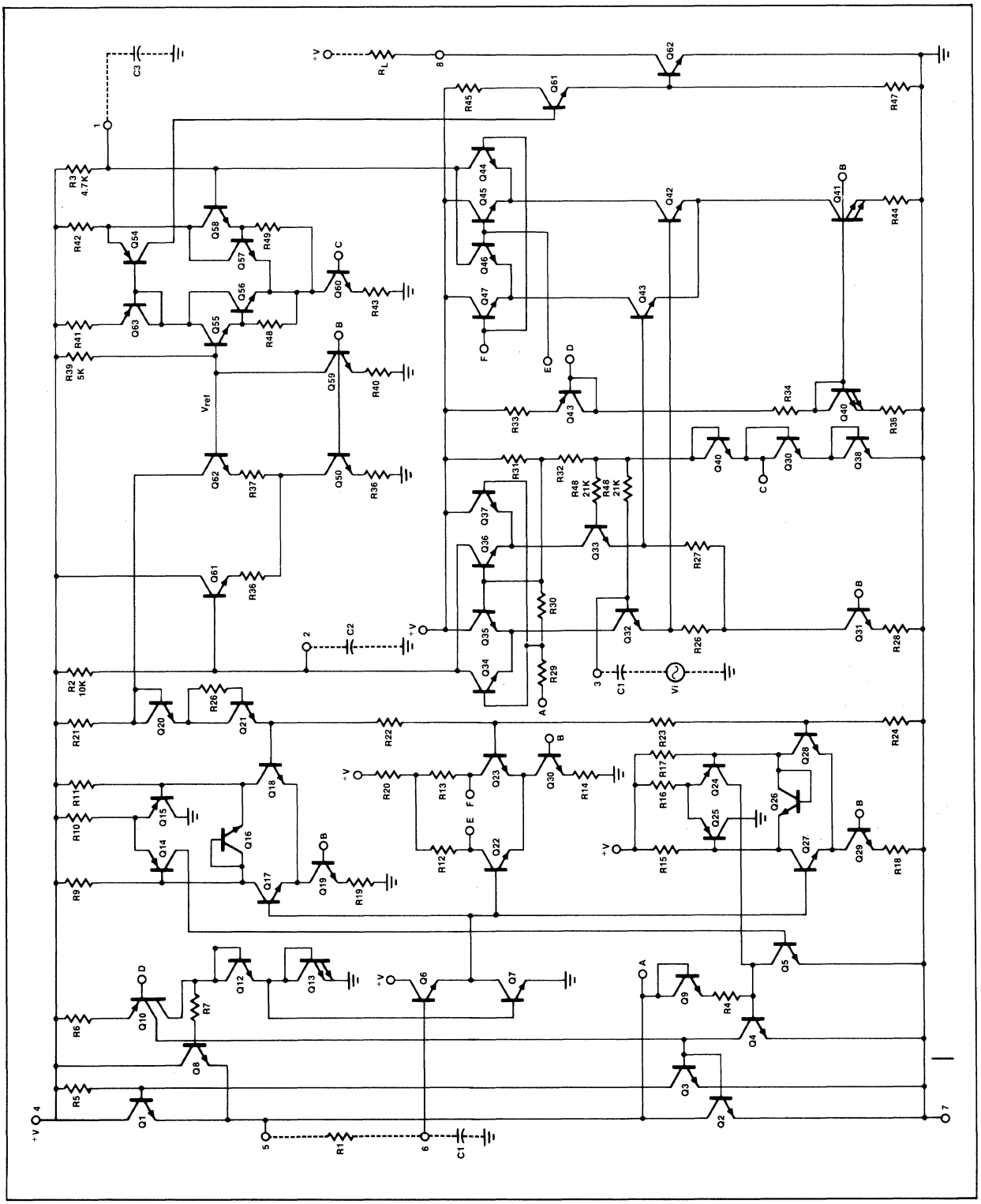
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Operating temperature		
NE567	0 to +70	°C
SE567	-55 to +125	°C
Operating voltage	10	V
Positive voltage at input	0.5 + Vs	V
Negative voltage at input	-10	Vdc
Output voltage (collector of output transistor)	15	Vdc
Storage temperature	-65 to +150	°C
Power dissipation	300	mW

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS (V+ = 5.0V; T_A = 25°C unless otherwise specified.)

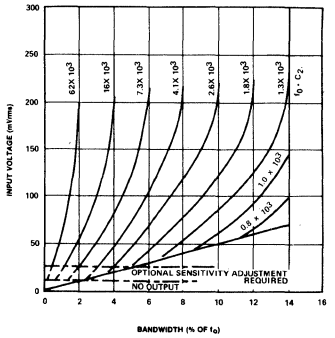
PARAMETER	TEST CONDITIONS	SE567			NE567			UNIT
		Min	Typ	Max	Min	Typ	Max	
CENTER FREQUENCY[1]								
Highest center frequency (f_o)		100	500		100	500		kHz
Center frequency stability[2]	-55 to +125°C		35±140			35±140		ppm/°C
	0 to +70°C		35±60			35±60		ppm/°C
Center frequency shift with supply voltage	f_o = 100kHz		0.5	1		0.7	2	%/V
DETECTION BANDWIDTH								
Largest detection bandwidth	f_o = 100kHz	12	14	16	10	14	18	% of f_o
Largest detection bandwidth skew			1	2		2	3	% of f_o
Largest detection bandwidth—variation with temperature	V_i = 300mVrms		±0.1			±0.1		%/°C
Largest detection bandwidth—variation with supply voltage	V_i = 300mVrms		±2			±2		%/V
INPUT								
Input resistance			20			20		kΩ
Smallest detectable input voltage (V_i)	I_L = 100mA, $f_i = f_o$		20	25		20	25	mVrms
Largest no-output input voltage	I_L = 100mA, $f_i = f_o$	10	15		10	15		mVrms
Greatest simultaneous outband signal to inband signal ratio			+6			+6		dB
Minimum input signal to wideband noise ratio	B_n = 140kHz		-6			-6		dB
OUTPUT								
Fastest on-off cycling rate			f_o/20			f_o/20		
"1" output leakage current			0.01	25		0.01	25	A
"0" output voltage	I_L = 30mA		0.2	0.4		0.2	0.4	V
	I_L = 100mA		0.6	1.0		0.6	1.0	V
Output fall time[3]	R_L = 50Ω		30			30		ns
Output rise time[3]	R_L = 50Ω		150			150		ns
GENERAL								
Operating voltage range		4.75		9.0	4.75		9.0	V
Supply current quiescent			6	8		7	10	mA
Supply current—activated	R_L = 20kΩ		11	13		12	15	mA
Quiescent power dissipation			30			35		mW

NOTES

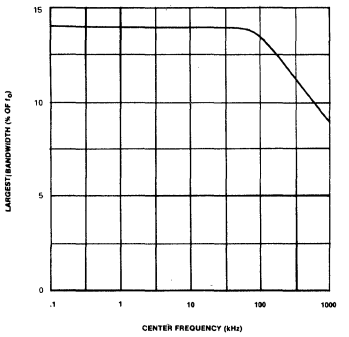
1. Frequency determining resistor R_1 should be between 1 and 20kΩ.
2. Applicable over 4.75 to 5.75 volts. See graphs for more detailed information.
3. Pin 8 to Pin 1 feedback R_L network selected to eliminate pulsing during turn-on and turn-off.

TYPICAL PERFORMANCE CHARACTERISTICS

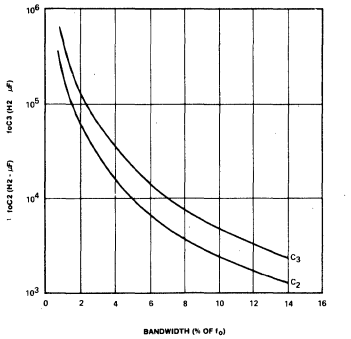
BANDWIDTH vs INPUT SIGNAL AMPLITUDE



LARGEST DETECTION BANDWIDTH vs OPERATING FREQUENCY

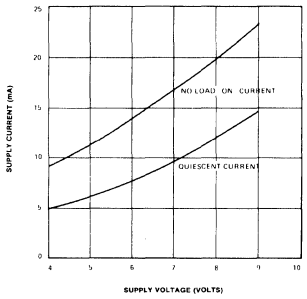


DETECTION BANDWIDTH AS A FUNCTION OF C_2 and C_3

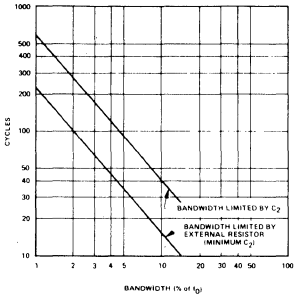


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

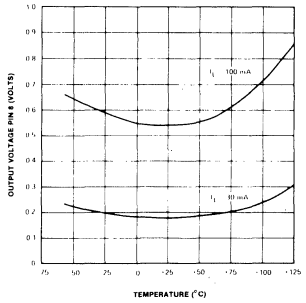
TYPICAL SUPPLY CURRENT vs SUPPLY VOLTAGE



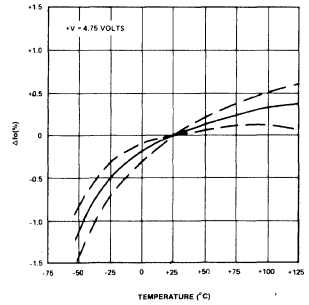
GREATEST NUMBER OF CYCLES BEFORE OUTPUT



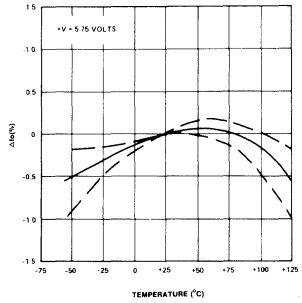
TYPICAL OUTPUT VOLTAGE vs TEMPERATURE



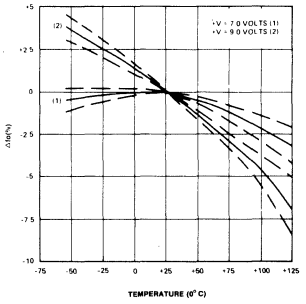
TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)



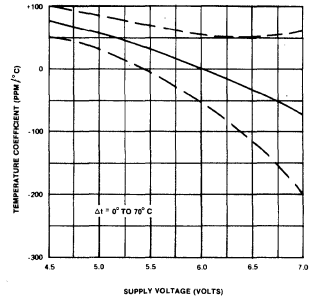
TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)



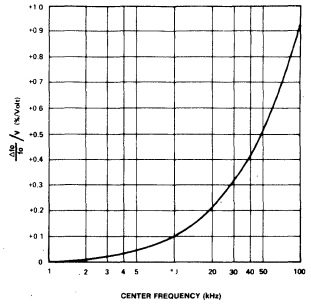
TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)



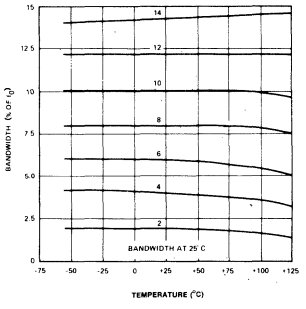
CENTER FREQUENCY TEMPERATURE COEFFICIENT (MEAN AND S.D.)



CENTER FREQUENCY SHIFT WITH SUPPLY VOLTAGE CHANGE vs OPERATING FREQUENCY



TYPICAL BANDWIDTH VARIATION WITH TEMPERATURE



DESIGN FORMULAS

$$f_0 \approx \frac{1.1}{R_1 C_1}$$

$$BW \approx 1070\sqrt{\frac{V_i}{f_0 C_2}} \text{ in \% of } f_0,\ V_i \leq 200\text{mVrms}$$

Where

V_i = Input Voltage (Vrms)
C_2 = Low-Pass Filter Capacitor (μF)

PHASE LOCKED LOOP TERMINOLOGY CENTER FREQUENCY (fo)

The free-running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

Detection Bandwidth (BW)

The frequency range, centered about f_0, within which an input signal above the threshold voltage (typically 20mVrms) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

Lock Range

The largest frequency range within which an input signal above the threshold voltage will hold a logical zero state on the output.

Detection Band Skew

A measure of how well the detection band is centered about the center frequency, f_0. The skew is defined as $(f_{max} + f_{min} - 2f_0)/2f_0$ where fmax and fmin are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

OPERATING INSTRUCTIONS

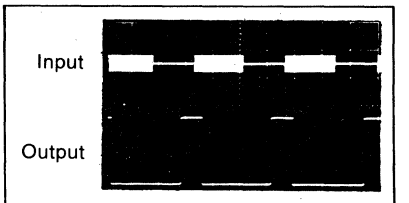
Figure 1 shows a typical connection diagram for the 567. For most applications, the following three-step procedure will be sufficient for choosing the external components R_1, C_1, C_2 and C_3.

1. Select R_1 and C_1 for the desired center frequency. For best temperature stability, R_1 should be between 2K and 20K ohm, and the combined temperature coefficient of the R_1C_1 product should have sufficient stability over the projected temperature range to meet the necessary requirements.

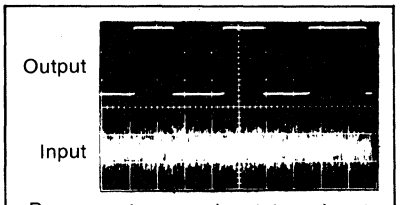
2. Select the low pass capacitor, C_2, by referring to the Bandwidth versus Input Signal Amplitude graph. If the input amplitude variation is known, the appropriate value of f_0C_2 necessary to give the desired bandwidth may be found. Conversely, an area of operation may be selected on this graph and the input level and C_2 may be adjusted accordingly. For example, constant bandwidth operation requires that input amplitude be above 200mVrms. The bandwidth, as noted on the graph, is then controlled solely by the f_0C_2 product (f_0 (Hz), C_2 (μ fd)).

3. The value of C_3 is generally non-critical. C_3 sets the band edge of a low pass filter which attenuates frequencies outside the detection band to elminate spurious outputs. If C_3 is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If C_3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage on C_3 passes the threshold voltage. (Such delay may be desirable to avoid spurious outputs due to translent frequencies.) A typical minimum value for C_3 is $2C_2$.

TYPICAL RESPONSE



Response to 100mVrms tone burst.
R_L = 100 ohms.



Response to same input tone burst with wideband noise.
$\frac{S}{N}$ = -6db R_L = 100 ohms
Noise Bandwidth = 140Hz

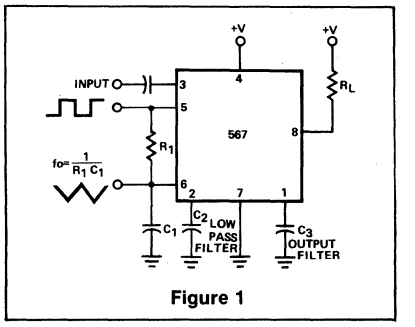


Figure 1

AVAILABLE OUTPUTS (Figure 2)

The primary output is the uncommitted output transistor collector, pin 8. When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0 volt (typically 0.6V) at full output current (100mA). The voltage at pin 2 is the phase detector output which is a linear function of frequency over the range of 0.95 to 1.05 f_0 with a slope of about 20mV per percent of frequency deviation. The average voltage at pin 1 is, during lock, a function of the inband input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave output of magnitude $(+V - 2V_{be}) \approx (+V - 1.4V)$ having a dc average of +V/2. A 1kΩ load may be driven from pin 5. Pin 6 is an exponential triangle of 1 volt peak-to-peak with an average dc level of +V/2. Only high impedance loads may be connected to pin 6 without affecting the CCO duty cycle or temperature stability.

OPERATING PRECAUTIONS

A brief review of the following precautions will help the user achieve the high level of performance of which the 567 is capable.

1. Operation in the high input level mode (above 200mV) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the in-band signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at $f_0/3$, $f_0/5$, etc.

2. The 567 will lock onto signals near $(2n + 1)\ f_0$, and will give an output for signals near $(4n + 1)\ f_0$ where $n = 0, 1, 2$, etc. Thus, signals at $5f_0$ and $9f_0$ can cause an unwanted output. If such signals are anticipated, they should be attenuated before reaching the 567 input.

3. Maximum immunity from noise and out-band signals is afforded in the low input level (below 200mVrms) and reduced bandwidth operating mode. However, decreased loop damping causes the worse-case lock-up time to increase, as shown by the Greatest Number of Cycles Before Output vs Bandwidth graph.

4. Due to the high switching speeds (20ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. The power supply should be adequately bypassed close to the 567 with a 0.01μF or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and

unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply or increasing the supply filter capacitor.

SPEED OF OPERATION

Minimum lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, maximum operating speed is obtained when C_2 is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away form the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock-up transient is at its worst and the theoretical minimum lock-up time is not achievable. We must simply wait for the transient to die out.

The following expressions give the values of C_2 and C_3 which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $f_o/10$ baud.

$$C_2 = \frac{130}{f_o}\ \mu F$$

$$C_3 = \frac{260}{f_o}\ \mu F$$

In cases where turn-off time can be sacrificed to achieve fast turn-on, the optional sensitivity adjustment circuit can be used to move the quiescent C_3 voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.

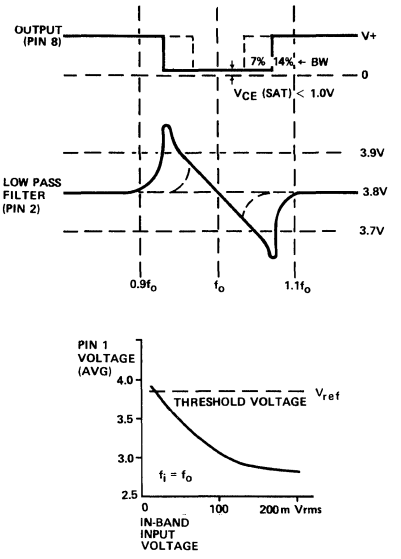


Figure 2

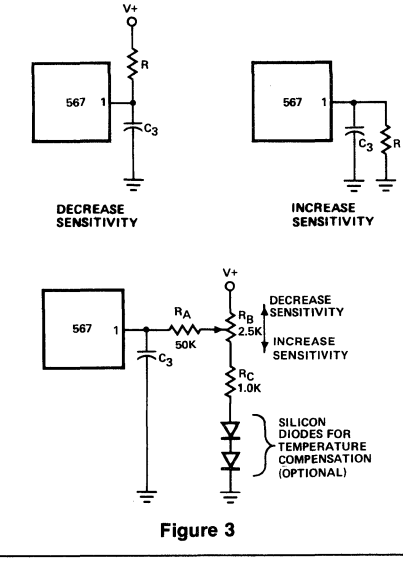


Figure 3

OPTIONAL CONTROLS (Figure 3)

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will be greatly facilitated if full advantage is taken of the added control possibilities available through the use of additional external components. In the diagrams given, typical values are suggested where applicable. For best results the resistors used, except where noted, should have the same temperature coefficient. Ideally, silicon diodes would be low-resistivity types, such as forward-biased transistor base-emmiter junctions. However, ordinary low-voltage diodes should be adequate for most applications.

SENSITIVITY ADJUSTMENT

(Figure 3)

When operated as a very narrow band detector (less than 8 percent), both C_2 and C_3 are made quite large in order to improve noise and outband signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to terminal 1. Under this condition, the 567 will also give an output for lower-level signals (10mV or lower).

By adding current to terminal 1, the output stage is biased further away from the threshold voltage. This is most useful when, to obtain maximum operating speed, C_2 and C_3 are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the outband beat notes do not feed through to the output stage. Since the input level must be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in-band harmonics (of lower frequency signals) is also improved.

CHATTER PREVENTION (Figure 4)

Chatter occurs in the output stage when C_3 is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognize the chatter as a series of outputs. By feeding the output stage output back to its input (pin 1) the chatter can be eliminated. Three schemes for doing this are given in Figure 4. All operate by feeding the first output step (either on or off) back to the input, pushing the input past the threshold until the transient conditions are over. It is only necessary to assure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can always be eliminated by making C_3 large, the feedback circuit will enable faster operation of the 567 by allowing C_3 to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.

DETECTION BAND CENTERING (OR SKEW) ADJUSTMENT

(Figure 5)

When it is desired to alter the location of the detection band (corresponding to the loop capture range) within the lock range, the

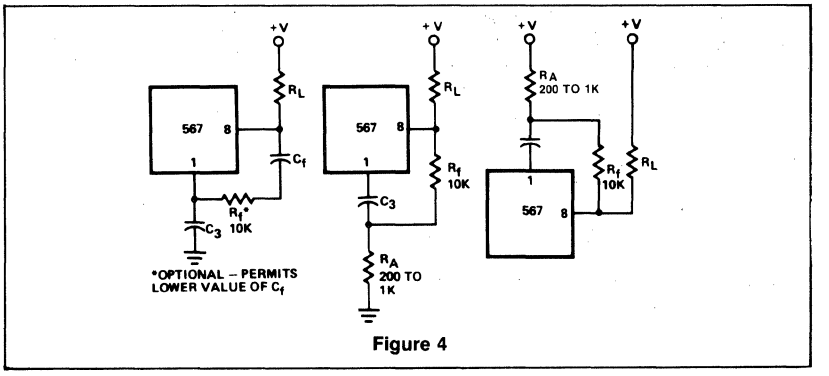


Figure 4

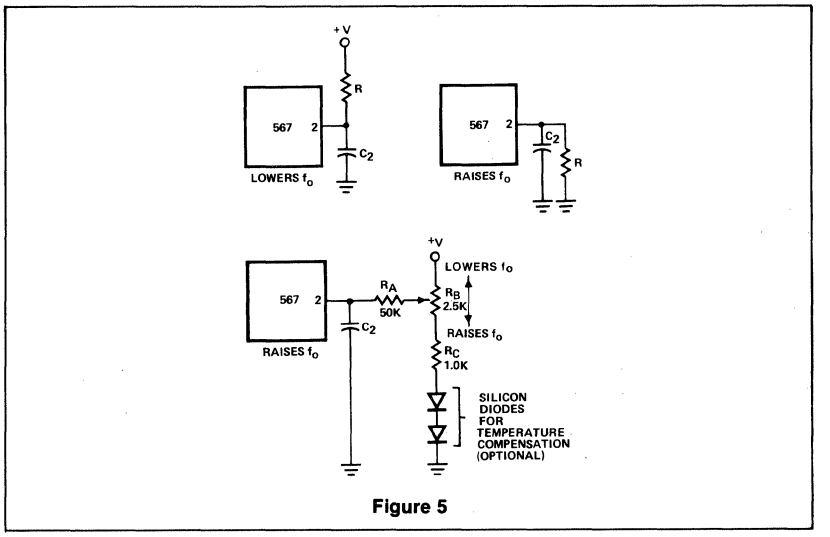


Figure 5

circuits shown above can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the center frequency. Since R_B also alters the duty cycle slightly, this method may be used to obtain a precise duty cycle when the 567 is used as an oscillator.

ALTERNATE METHOD OF BANDWIDTH REDUCTION

(Figure 6)

Although a large value of C_2 will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve damping and permit faster operation under narrow-band conditions. Note that the reduced impedance level at terminal 2 will require that a larger value of C_2 be used for a given filter cutoff frequency. If more than three 567s are to be used, the network of R_B and R_C can be eliminated and the R_A resistors connected together. A capacitor between this junction and ground may be required to shunt high frequency components.

OUTPUT LATCHING (Figure 7)

To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between pins 8 and 1). Pin 1 is pulled up to unlatch the output stage.

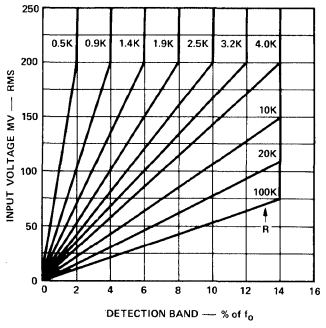
REDUCTION OF C1 VALUE

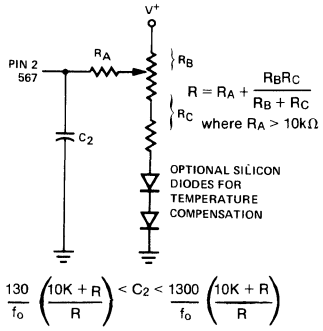
(Figure 8)

For precision very low-frequency applications, where the value of C_1 becomes large, an overall cost savings may be achieved by inserting a voltage follower between the R_1 C_1 junction and pin 6, so as to allow a higher value of R_1 and a lower value of C_1 for a given frequency.

PROGRAMMING

To change the center frequency, the value of R_1 can be changed with a mechanical or solid state switch, or additional C_1 capacitors may be added by grounding them through saturating npn transistors.





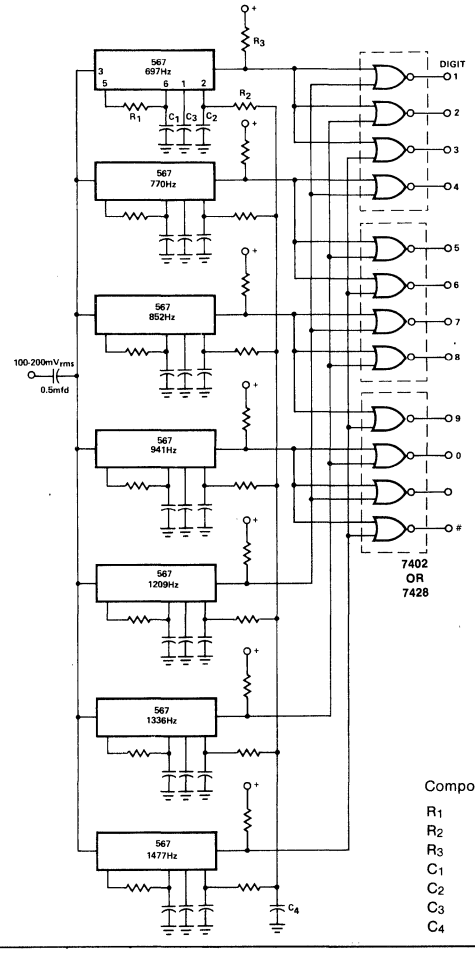
NOTE

Adjust control for symmetry of detection band edges about f_o.

Figure 6

TYPICAL APPLICATIONS

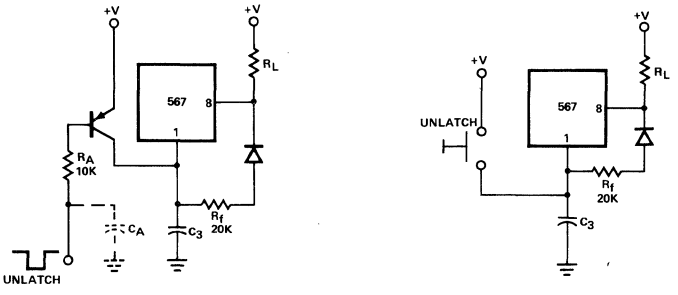
TOUCH-TONE® DECODER



Component values (Typical)

R_1	6.8 to 15K ohm
R_2	4.7K ohm
R_3	20K ohm
C_1	0.10mfd
C_2	1.0mfd 5V
C_3	2.2mfd 6V
C_4	250 μF 6V

OUTPUT LATCHING



C_A prevents latch-up when power supply is turned on.

Figure 7

PRECISION VLF

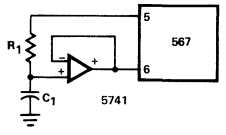
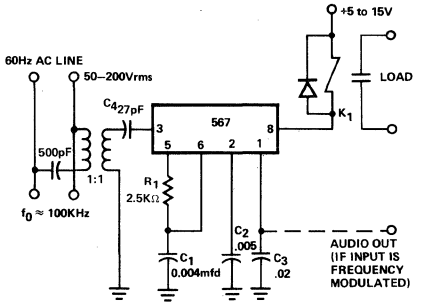


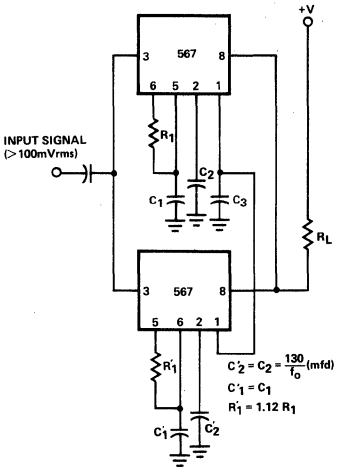
Figure 8

TYPICAL APPLICATIONS (Cont'd)

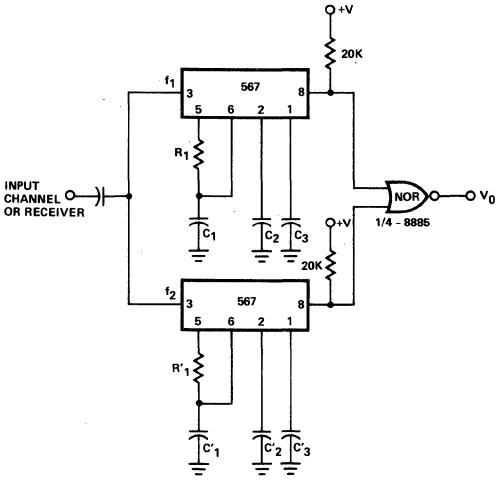
CARRIER-CURRENT REMOTE CONTROL OR INTERCOM



24% BANDWIDTH TONE DECODER

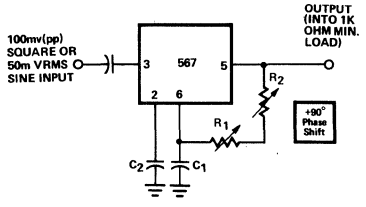


DUAL-TONE DECODER



1. Resistor and capacitor values chosen for desired frequencies and bandwidth.
2. If C_3 is made large so as to delay turn-on of the top 567, decoding of sequential (f_1 f_2) tones is possible.

0° to 180° PHASE SHIFTER

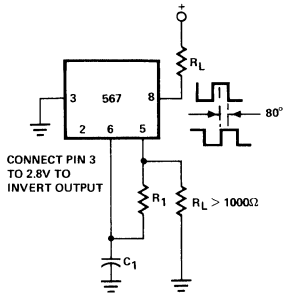


$R_2 \approx R_1/5$

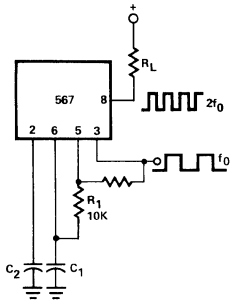
Adjust R_1 so that $\phi = 90°$ with control midway

TYPICAL APPLICATIONS (Cont'd)

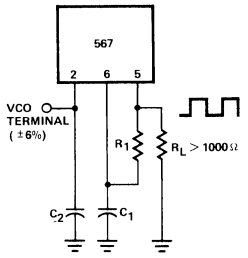
OSCILLATOR WITH QUADRATURE OUTPUT



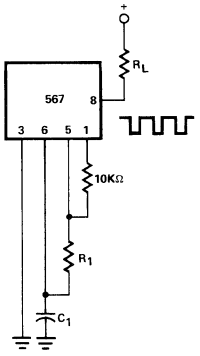
OSCILLATOR WITH DOUBLE FREQUENCY OUTPUT



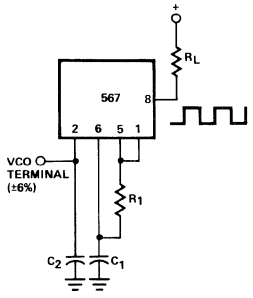
PRECISION OSCILLATOR WITH 20ns SWITCHING



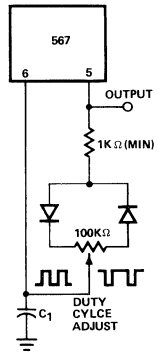
PULSE GENERATOR WITH 25% DUTY CYCLE



PRECISION OSCILLATOR TO SWITCH 100ma LOADS



PULSE GENERATOR



NOTE

Application information available on request.

SECTION 17
NEW PRODUCTS

HIGH SLEW RATE OPERATIONAL AMPLIFIER — NE/SE530/5530

PRELIMINARY SPECIFICATION

NE/SE530-N,T • NE/SE5530-N,T

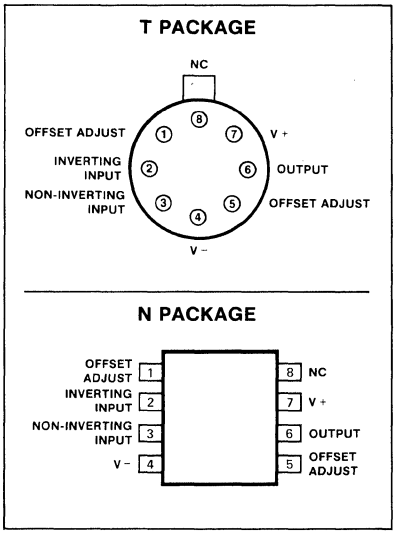
DESCRIPTION

The NE/SE530 and NE/SE5530 are new generation high slew rate operational amplifiers featuring 3MHz bandwidths and improved input parameters. The 530 is a single amplifier while the 5530 is a dual configuration. Both products will have industry standard pinouts.

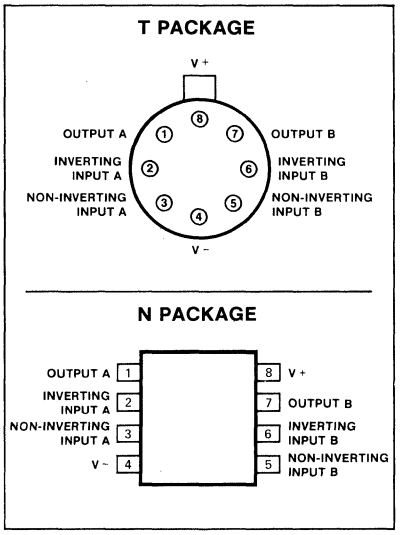
FEATURES

- **Output swing (±5v supplies) 8 volts p-p typical**
- **High slew rate 35V/μs@ unity gain inverting typical**
- **Settling time (to 0.1%) 1μs typical**
- **Low offset voltage 2mVmax**
- **Low bias current 60nAmax**
- **Wide bandwidth 3MHz typical**
- **Low current drain 2mA typical/amplifier**

PIN CONFIGURATIONS (530)



PIN CONFIGURATIONS (5530)

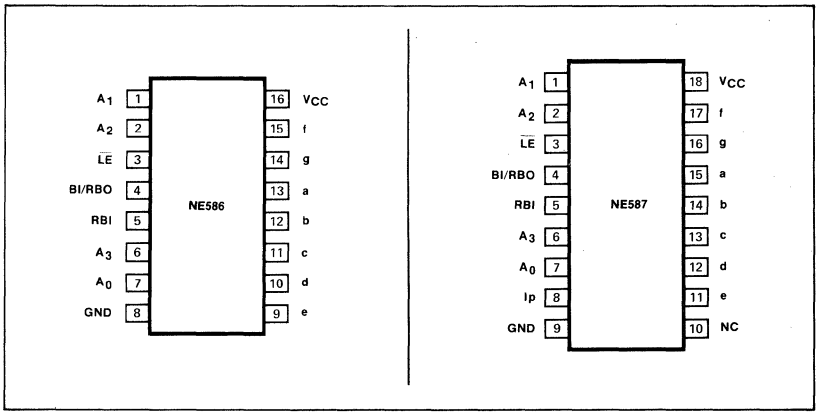


LED DISPLAY DRIVERS — NE586/587

DESCRIPTION

The NE586 and 587 are latch/decoder/drivers for 7-segment LED displays. Both devices have constant current outputs, the NE586 being a fixed 25mA/segment drive capability, and the NE587, variable between 5 and 50mA/segment. On the NE587 the current is set with a single external resistor. The data (BCD) inputs and $\overline{LE}$ (latch enable) function are low loading so that the devices are compatible with any data bus system.

PIN CONFIGURATION



ADDRESSABLE PERIPHERAL DRIVERS — NE590/NE591

PRELIMINARY SPECIFICATION

DESCRIPTION

The NE590/NE591 addressable peripheral drivers are high current latched drivers, similar in function to the 9334 address decoder. The device has 8 darlington power outputs, each capable of 250mA load current. The outputs are turned on or off by respectively loading a logic "1" or logic "0" into the device data input. The required output is defined by a 3 bit address. The device must be enabled by a $\overline{CE}$ input line which also serves the function of further address decoding. A common clear input, $\overline{CLR}$, turns all outputs off when a logic "0" is applied.

The NE590 has 8 open collector darlington outputs which sink current to ground. The device is packaged in a 16 pin molded or cerdip package.

The NE591 has 8 open emitter darlington outputs which source current to an external load from a common collector line, V_S. The V_S line need not necessarily be the same as the 5 volt V_{CC} supply. The device is packaged in an 18 pin molded or cerdip package.

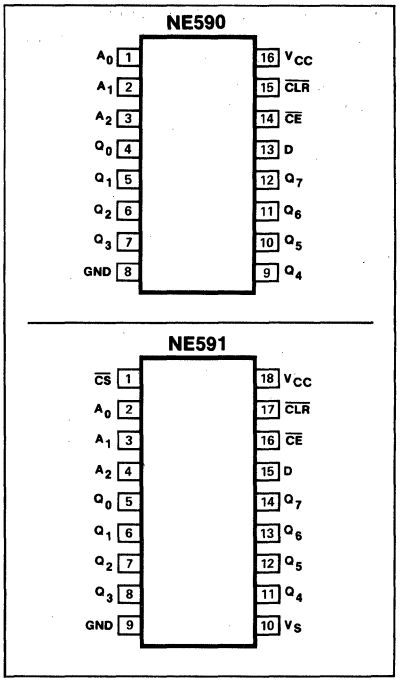
FEATURES

- **8 high current outputs**
- **Low-loading bus compatible inputs**
- **Power-on clear ensures safe operation**
- **NE590 will operate in addressable or demultiplex mode**
- **Allows random (addressed) data entry**
- **Easily expandable**
- **NE590 is pin compatible with 9334.**

APPLICATIONS

- **Relay driver**
- **Indicator lamp driver**
- **Triac trigger**
- **LED display digit driver**
- **Stepper motor driver**

PIN CONFIGURATIONS

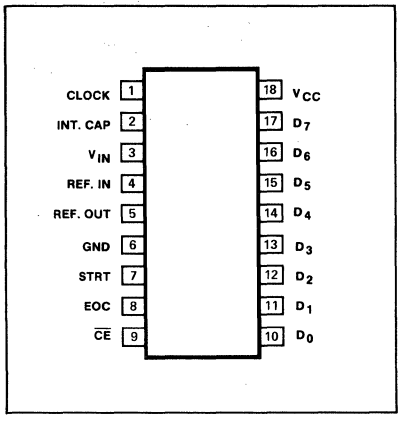


8-BIT ANALOG-TO-DIGITAL CONVERTER — NE5030

DESCRIPTION

The NE5030 is an 8-bit A-to-D converter employing the triple-slope technique of conversion. The device includes a voltage reference and clock generator and so constitutes the total conversion system with a minimum of components. Conversion time is approximately 10mS; voltage requirement is a single 5V supply and the data outputs are tri-state bus compatible.

PIN CONFIGURATION



APPLICATIONS

SECTION 18
ANALOG IC PROCESSING

INTRODUCTION

Integrated circuits are divided into three general categories: (1) linear, (2) digital, and (3) MOS. Distinctly different design and process techniques are used for each type. The main difference between linear processes and other IC processes is their diversity. While digital circuits are commonly restricted to low voltage switching, linear circuits may be fabricated with anything from switching to linear characteristics, high or low voltages, high or low frequency, or any combination of these properties. To cope with this range of applications, the following processes are frequently used:

Epitaxial— 0.25 ohm-cm gold doped and non-gold doped
0.5 ohm-cm gold doped
1.0 ohm-cm Schottky and non-Schottky
2.5 ohm-cm
5.0 ohm-cm

Dielectric— 2 to 15 ohm-cm

All epitaxial processes are similar. The main difference is the resistivity of the deposited epitaxial layer in which the components are formed. This provides the means of selecting higher breakdown voltages or lower saturations by merely selecting an epitaxial resistivity.

For instance, the 5 ohm-cm process is used for operational amplifiers and regulators because it gives the 50V LV_{ceo} transistor breakdowns required. Since the phase lock loops need only 20V, and lower saturation voltages are desirable, the 2.5 ohm-cm process is used for their fabrication.

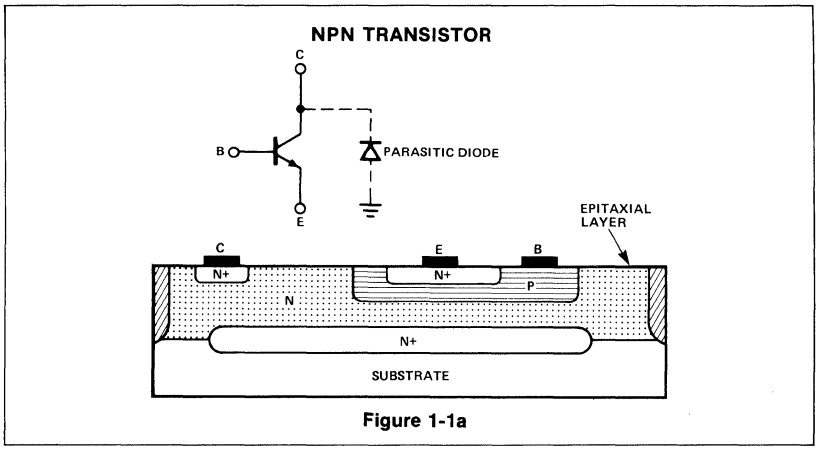


Figure 1-1a

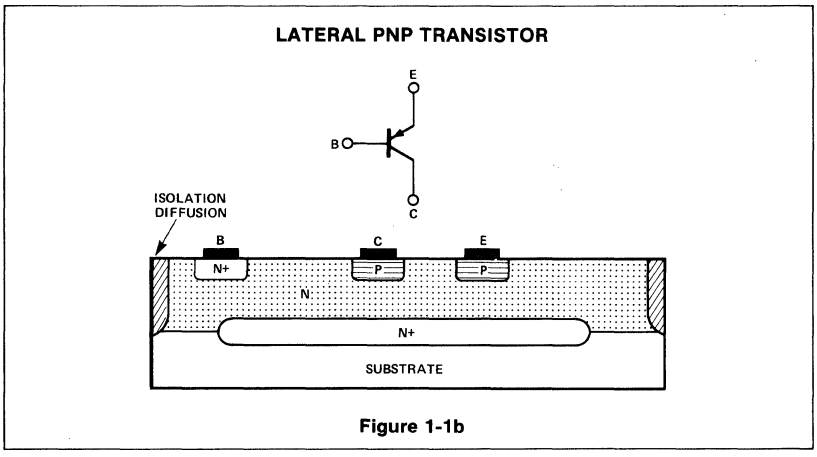


Figure 1-1b

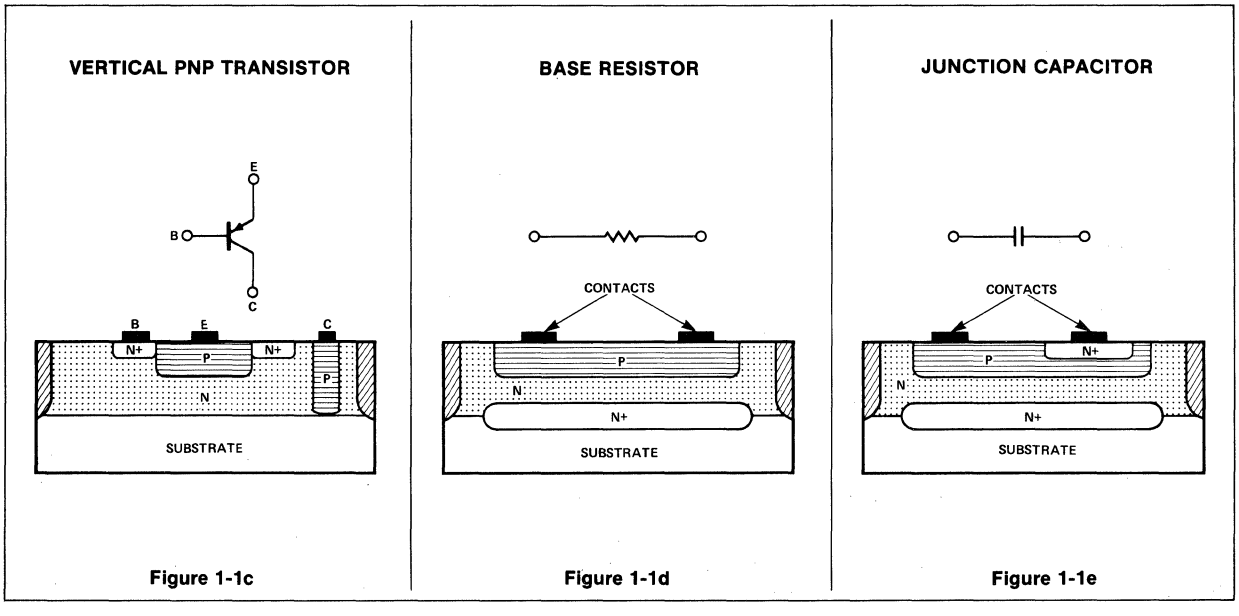


Figure 1-1c **Figure 1-1d** **Figure 1-1e**

Transistor breakdown is not the only consideration in choosing a process. In products where fast switching is required, either the gold doped or Schottky processes are used. Gold doping is used where medium and high current operation is involved. Schottky technology is desired where lower currents or high transistor breakdowns are needed in addition to speed. Dielectric isolation is used where breakdown voltages must be in excess of 50 volts.

COMPONENTS

The components commonly formed in linear integrated circuits by junction isolation are drawn in cross section in Figure 1-1. Parasitic components are also shown in the equivalent schematics. These parasitics can occasionally cause "sneak" paths or fault conditions in the circuit.

TRANSISTORS

It is instructive to compare, in a general manner, discrete transistors with those manufactured in integrated circuits. The most important differences for npn transistors are the parasitic substrate transistor and the top contact collector, as seen in Figure 1-2.

The magnitude of the parasitic pnp beta depends upon the process and geometry used, but it ranges from about five for high-resistivity processes to very much less than one for gold doped processes. The parasitic pnp only becomes active when the npn transistor goes into saturation. Normally such effects are not important, but in some circuit configurations latching effects may be observed. That is, a positive feedback path may be established which is self-sustaining. Alternately, or perhaps coincidentally, this path may cause high currents to flow. These potential problems are easily avoided with judicious layout procedures.

The effect of the top contact is to increase the saturation resistance. In small signal devices this is not significant, but at higher currents (around 50. mA) this becomes an economic factor as the die arc must be increased and yields drop. This resistance is lowered by means of the N+ buried layer seen in the cross sections of Figure 1-1.

The normal npn transistor beta for linear devices ranges up to 250. Occasionally "super beta" transistors are needed with betas as high as 2000. The processing steps involved are the same as for regular transistors except for a longer emitter diffusion time which gives a very narrow base width and high beta. Care must be exercised in this sequence to make super beta and regular npn devices at the same time.

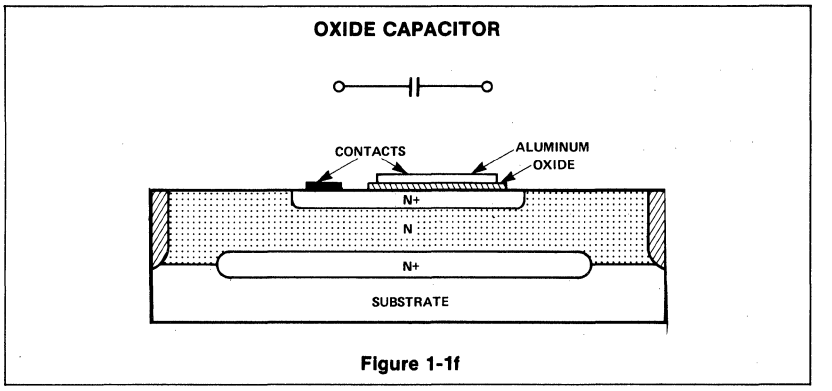


Figure 1-1f

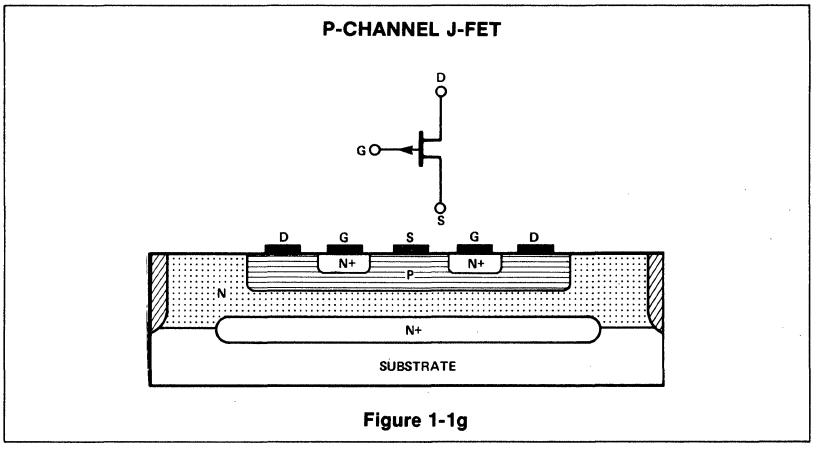


Figure 1-1g

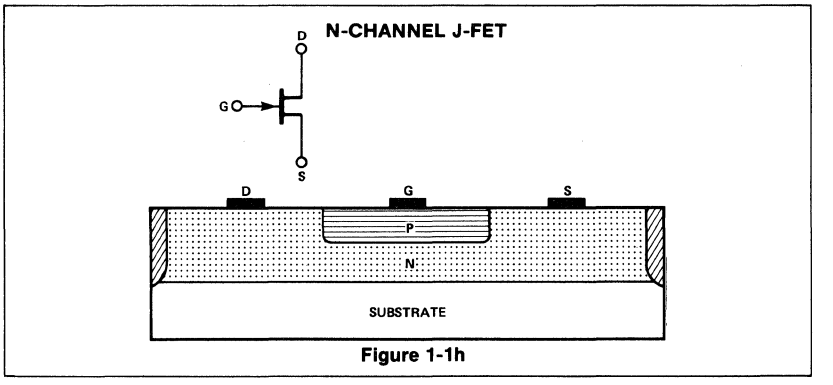


Figure 1-1h

The pnp transistors in monolithic form, both lateral and vertical, differ from discrete pnps. The names 'lateral' and 'vertical' are derived from the mode of transistor action that occurs in the two components. Referring to Figure 1-1B it can be seen that current flows laterally from emitter to collector through the N-epitaxial area. The presence of the buried layer diffusion reduces to a comparatively low level, the collection by the isolation area. It is not eliminated entirely, however, which gives rise to the parasitic diode shown in Figure 1-3.

The vertical pnp is similarly constructed but in this case the buried layer diffusion is omitted resulting in the isolation diffusion acting as the collector. The vertical current flow in this device gives rise to its name.

Frequency response is the primary difference between these devices. The lateral pnp is restricted to frequencies below 1 to 2 MHz while the vertical pnp upper range is around

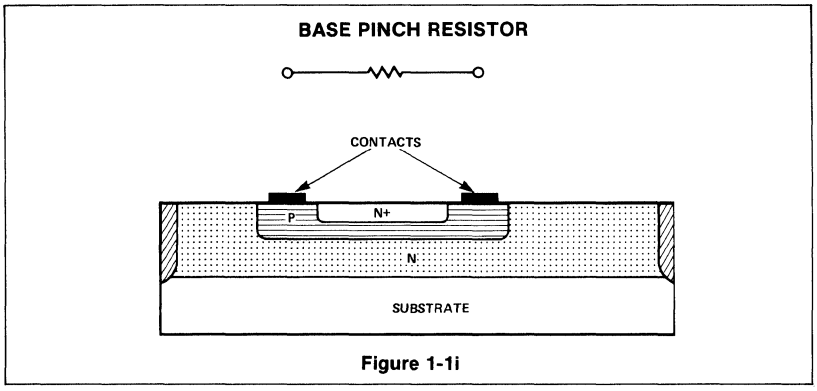


Figure 1-1i

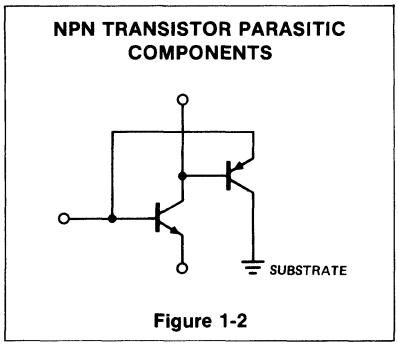


Figure 1-2

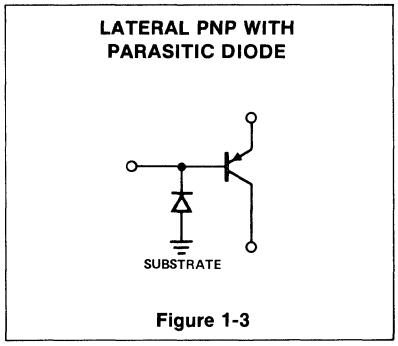


Figure 1-3

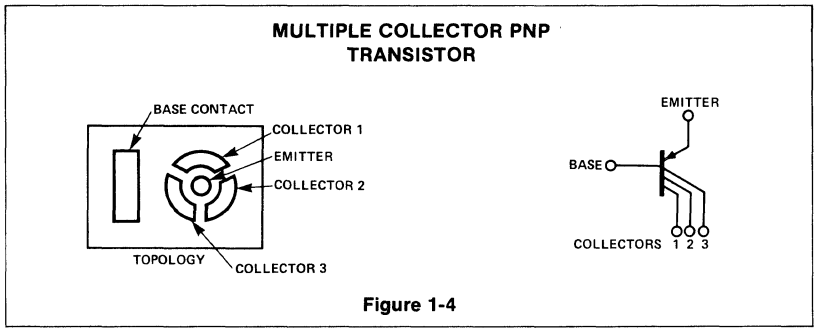


Figure 1-4

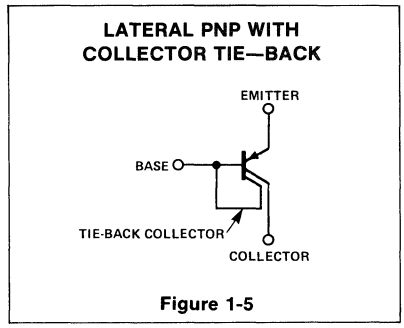


Figure 1-5

10 to 20 MHz. Another important feature of the lateral pnp is its comparatively low beta range and the low current at which beta peaks. In addition, the lateral pnp collector can be split to give multiple collector devices as shown in Figure 1-4.

This configuration can be used to give fairly precise values of beta by tying one of the collectors to the base. Figure 1-5 illustrates the tie back method used.

Recent process development allows the addition of Schottky barrier devices to monolithic design (see Figure 1-6). The advantage is very fast switching circuits without gold doping. With this technique, the properties of non-gold doped devices are maintained while switching speeds are greatly improved. This is very desirable in devices containing both analog and digital circuitry such as voltage comparators.

RESISTORS

Resistors can be made from any of the n or p type layers. In practice the base and emitter diffusions are generally used. At times the "epilayer" (the bulk material) in the dielectric isolation process is also used. The required characteristics of the resistor determine the material or processes used. The most commonly used is the base diffused resistor. Size is scaled for the value desired. Base pinch resistors are used where high values are required and the limitations of accuracy and breakdown are not a problem. Emitter resistors are useful where low value, temperature insensitive resistors are needed. This diffusion is also often used as a "cross-under," that is, a low resistance connecting path. This can simplify layout design considerably.

A new development in resistors that will offer great flexibility in design is the use of ion implantation. With this technique, resistivities orders of magnitude higher and temperature coefficients orders of magnitude lower than base diffused resistors are possible. We can expect to see this technology used extensively in high voltage circuits, low power circuits and in complex linear functions where die areas would otherwise be excessive.

JUNCTION FIELD EFFECT TRANSISTORS

The n-channel FET is fabricated in the epitaxial layers and is obtained by pinching-off the epi with isolation diffusion. Because of this construction, the nomenclature FET is something of a misnomer since the gate is not available as an input. Its usefulness is as a bias circuit starting element. It is much smaller in area than an equivalent value resistor and has a sufficiently high breakdown voltage for this purpose.

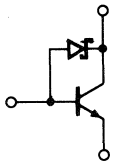
The p-channel FET is a more useful general purpose device. Its most important limitation is the breakdown voltage which is restricted to about 5 volts. Processing of both field effect and super beta transistors is similar. Changes in the regular process flows is necessary for both devices.

CAPACITORS

Capacitors are made by using the capacitance associated with the various junctions or by forming a thin silicon dioxide layer between two plates. The plates are formed by aluminum metalization and low resistivity emitter diffusion.

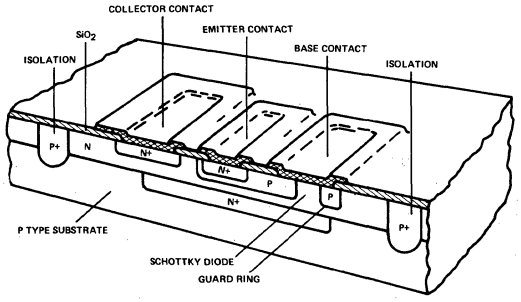
A number of problems are associated with junction capacitors. They have low breakdowns for reasonable capacitance per unit area, the capacitors formed are polarized,

SCHOTTKY DIODE



SCHEMATIC

Figure 1-6a



CROSS-SECTION

Figure 1-6b

and they have high leakage currents. Oxide capacitors are free from these problems but the capacitance per unit area is comparatively low. Junction capacitors are used primarily where decoupling capacitors are needed, while oxide capacitors are used where high quality is needed.

OTHER DEVICES

There are a number of other components such as SCR, SCS and Zener diodes that are available coincidentally with the components discussed above. The Zener diodes available are the emitter base junction and the emitter-isolation junction. Other junctions have breakdowns that are high and variable so they are seldom used.

OXIDE CAPACITOR CONSTRUCTION

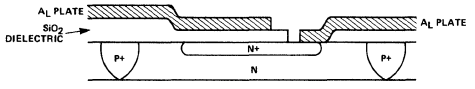


Figure 1-7

SECTION 19
ANALOG IC DESIGN TECHNIQUES

INTRODUCTION

The components available for linear ICs were reviewed in Section 1. From that discussion it was clear that many differences exist between IC components and those available to discrete circuit design. These differences may be conveniently summarized as:

A. Limited resistor accuracy and values
B. Lack of integrated inductance
C. Small integrated capacitance values
D. Poor PNP transistor performance
E. Limited power dissipation

On the other hand, linear IC designs have the advantages of excellent component matching, both active and passive; and the accessibility of a great number of active components.

To cope with the limitations of monolithic circuitry, designers have evolved special techniques and practices, a number of which are detailed in this section.

BIAS CIRCUITRY

In discrete designs the bias circuitry is accomplished by high value resistor networks. In linear designs this is impractical because of the die area required. The alternative is to use an n-channel FET as shown in Figure 2-1.

SIMPLE BIAS CIRCUIT

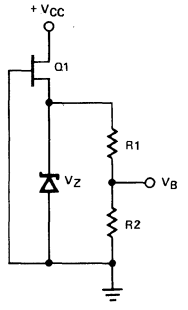


Figure 2-1

Zener V_Z is fed current by FET Q1. The required bias voltage is then developed by the resistor divider R1 and R2. This simple technique can be elaborated upon if temperature compensation is required. By adding transistor Q2 shown in Figure 2-2, the positive temperature coefficient of the zener diode is offset by the negative one of the forward biased emitter-base diode.

More elaborate schemes, which include the maintenance of constant currents in the

TEMPERATURE COMPENSATED BIAS NETWORK

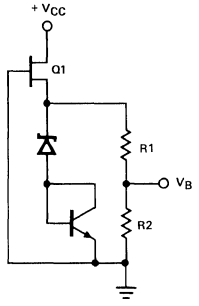


Figure 2-2

diodes, buffering the load from the source, and adjusting the composite temperature coefficient to zero, are commonly found where accurate references are required.

Current sources as well as voltage sources can be easily obtained using similar circuitry. Both npn and pnp type current sources are depicted by Figure 2-3.

NPN AND PNP CURRENT SOURCES

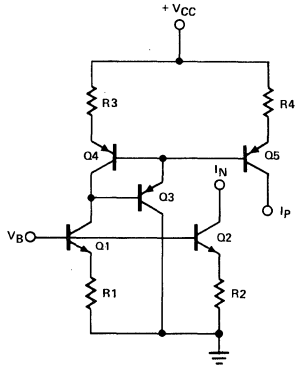


Figure 2-3

Assuming Q1-Q2 and Q4-Q5 are well matched and of the same geometries it can be shown that :

$$I_{NPN} = \frac{V_B - V_{BE}}{R2} \quad \text{and} \quad I_{PNP} = \left[\frac{V_B - V_{BE}}{R1}\right] \frac{R3}{R4}$$

These equations demonstrate that the circuit currents can be made independent of external supply voltages and temperature fluctuations. Circuits such as these are used extensively in modern operational amplifiers such as the 531 and 536, where their presence assures that such parameters as voltage gain and offset voltage remain constant with temperature and supply voltage variations.

The preceding circuits are valuable for high and medium values of current. Low current values are better developed by the popular circuit of Figure 2-4.

LOW VALUE CURRENT SOURCE

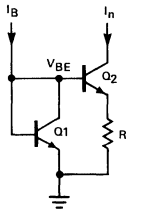


Figure 2-4

If the geometries of Q1 and Q2 are identical, the following equations hold:

$$V_{BE1} = V_{BE2} + I_N R$$

$$V_{BE1} = \frac{kT}{q} \ln\left(\frac{I_B}{I_S}\right)$$

$$V_{BE2} = \frac{kT}{q} \ln\left(\frac{I_N}{I_S}\right)$$

$$I_N R = \frac{kT}{q} \ln\left(\frac{I_B}{I_N}\right)$$

Where the subscripts refer to their respective transistors, beta is high, and other symbols have their standard meaning.

This is a transcendental equation which is represented graphically by Figure 2-5.

CURRENT SOURCE FAMILY CURVES

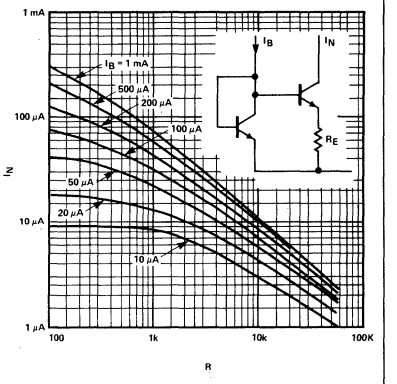


Figure 2-5

As can be seen, it becomes possible to obtain very low currents with reasonable values of resistance. This circuit is used in the 592 where I_{bias} is set by a single resistor and the valve of the operating power supplies.

This principle may be extended to provide a particularly useful voltage reference. The circuit of Figure 2-6 illustrates how this is done.

NON ZENER VOLTAGE REFERENCE

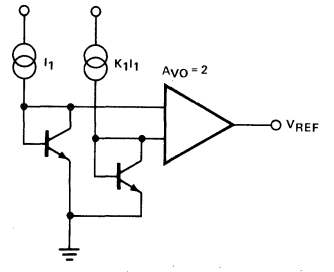


Figure 2-6

From the same considerations as before, the reference voltage can be shown to be:

$$V_{Ref} = K_2 \frac{kT}{q} I_n K_1$$

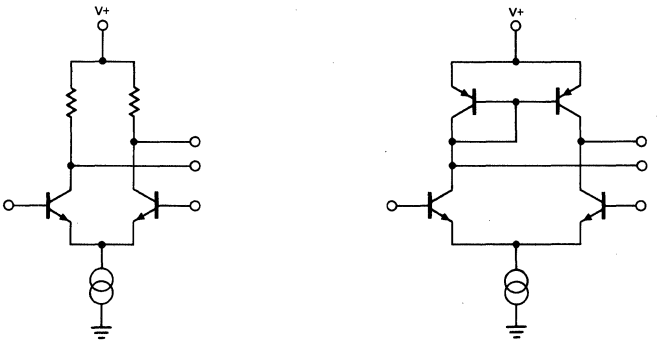
There are a number of interesting and useful properties of this circuit. Compared with a Zener reference, it is much less noisy and can be used at lower supply voltages. With judicious circuit implementation, the voltage can be controlled to about ±10% and low temperature coefficients can be achieved.

CURRENT SOURCE LOADS

Using current sources for load resistors is another technique exploited in linear integrated circuit designs. The schematics of Figure 2-7 show how this may be done. The circuit shown is the simple differential amplifier. Figure 2-7a gives a conventional circuit while Figure 2-7b is an I.C. implementation using pnp current sources.

The value of the current source as a collector load lies in its equivalancy of an extremely high resistance while occupying a very small die area. High stage gains are thus obtained in a minimum of space. Other advantages of the current source include linearity of gain versus output swing (because gain is independent of current), and large output swing capabilities. The active load circuit also has the feature of summing the gain from both output sides. The disadvantages of the circuit in Figure 2-7b are that the noise in the pnp's is summed into the npn input noise, and the self-biasing scheme used in Figure 2-7b can introduce some added offset current if the pnp betas are low because pnps run at different current levels. A change in the circuit which avoids this problem is shown in Figure 2-8.

DIFFERENTIAL AMPLIFIER



Conventional Design Current Source Loads

Figure 2-7a **Figure 2-7b**

IMPROVED DIFFERENTIAL AMPLIFIER

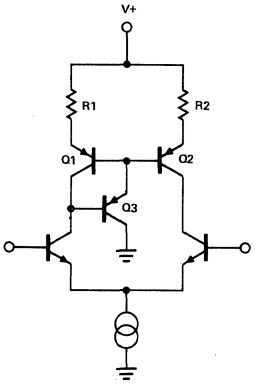


Figure 2-8

The current imbalance between Q1 and Q2 is now only:

$$I_{B3} = \frac{2I_{C1}}{\beta_1 \beta_3}$$

Where I_{B3} is Q3 base current
I_{C1} is Q1 collector current
and β_1 and β_3 are betas of Q1 and Q3 respectively. This imbalance is now negligible. Resistors have also been added to the pnp emitters to increase the output impedance and, therefore, the gain.

Use of the pnp as a collector load can be extended by using multiple collector pnps as indicated in Figure 2-9.

MULTIPLE COLLECTOR TRANSISTOR LOADS

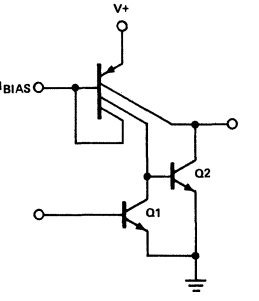


Figure 2-9

This circuit could give a voltage gain of many millions, which for linear amplification would be generally impractical due to clipping. A practical realization would incorporate feedback to define gain, as shown in Figure 2-10, where the voltage gain is given by the ratio:

$$A_V = \frac{R_F}{R_E}$$

LEVEL SHIFTING

The necessity for level shifting arises from two general requirements:

A. Level interfacing from input to output
B. Maintaining voltages across transistor collector-base junctions to avoid clipping.

The latter situation can be seen in the circuit of Figure 2-10, where the voltage across Q1 is limited to a V_{BE} minus an IR drop which limits the voltage swing at the output. Discrete designers overcome this problem with a liberal use of coupling and decoupling capacitators which are not available to linear I.C. designers, unless incorporated externally.

AMPLIFIER STAGE WITH FIXED GAIN

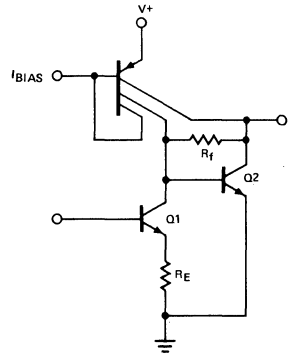


Figure 2-10

Resistive level shifting is one method used in integrated circuitry. Figure 2-11 illustrates the actual and equivalent networks.

The DC voltage is level shifted down from point A to point B through resistor R1 by the current of Q2. The circuit AC performance can be analyzed by the equivalent circuit of Figure 2-11b with the gain of the circuit being given by:

$$A_1 = \frac{Z_2}{Z_1 Z_2}$$

Where

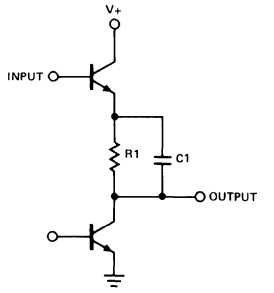
$$Z_1 = \frac{R1}{1 + j\omega R1C1} \text{ and } Z2 = \frac{R2}{1 + j\omega R2C2}$$

Maximum gain and broad bandwidth are dependent upon the following relationships:

R2 >> R1 and C1 >>C2

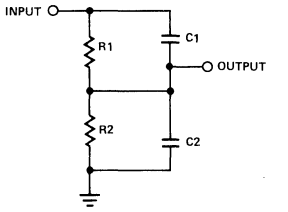
These conditions can generally be met since the output can be fed into an emitter follower with high input resistance and low input capacitance. R2 and C2 values would be in the 5 megohm and 0.5 pF range respectively. These values place workable values of R1 and C1 at 10-20Kohms and 15-30pF respectively. Lower values of R1 consume excessive current while lower values of C1 degrade the 50MHz frequency performance.

RESISTIVE LEVEL SHIFTING



Actual Circuit

Figure 2-11a



Equivalent Circuit

Figure 2-11b

The disadvantages of this circuit include:

A. Large die area for R1 and C1
B. Limited voltage range
C. Power consumption without gain

A level shifter which overcomes these problems is the zener diode. A reverse biased transistor emitter base junction, giving a voltage drop of 6 to 7 volts, is commonly used for the zener since the voltage is in the range generally required.

ZENER DIODE LEVEL SHIFTING

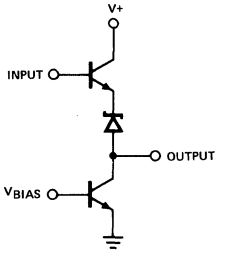


Figure 2-12

Multiples of this value can be gained by cascading more diodes. The benefits of this method are speed and small die area, while disadvantages include inflexibility to power supplies and high noise. These drawbacks restrict the use of this method to switching circuits such as comparators and sense amplifiers.

A combination of these two methods provides a circuit which provides a variable level shift. The zener of Figure 2-13 produces a constant voltage drop which is modified by resistors R1 and R2. Input to output voltage is given by:

$$V = \left(1 + \frac{R1}{R2}\right)(V_2 = V_{BE})$$

VARIABLE LEVEL SHIFT

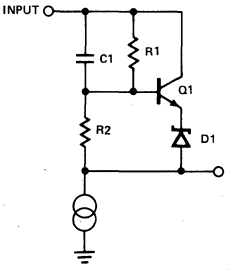


Figure 2-13

The most universally used level shifting technique however, uses the pnp transistor. The circuit of Figure 2-10 has been redrawn to include pnp level shifters in Figure 2-14.

LEVEL SHIFT WITH PNP TRANSISTORS

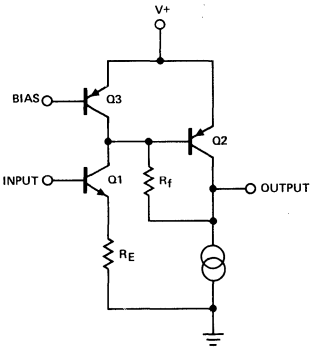


Figure 2-14

Transistors Q3 and Q4 are current source loads as described earlier. With the addition of Q2 the level shifting has been accomplished across the gain stage itself. The primary advantages are a large voltage range and power supply insensitivity. Voltage ranges up to the breakdown of the transistor are available with the additional advantage of voltage gain for the current consumed. Although not a problem in audio and low frequency systems, the disadvantage of the pnp level shifter is lack of frequency response above 1MHz.

OUTPUT STAGES

The design techniques for driven stages used in linear integrated circuits differ little from those of conventional designs. In cases where the power required is small, the conventional class A emitter follower is generally used as shown in Figure 2-15a.

The integrated form may vary in that R_E is generally replaced by a current source in the interest of smaller die size.

Where both sink and source drive capabilities are required, the nnp-pnp arrangement is used. As shown in Figure 2-16a driver Q1 feeds output transistors Q2 and Q3.

Diodes D1 and D2 are used to bias the output transistors into slight quiescent conduction. Temperature variations make current control difficult with this method and thermal runaway can result. The circuit of Figure 2-16b is much better from this standpoint since the current through Q4 and, therefore, the voltage across Q4 and Q5 can be controlled fairly well. By adjusting the value of R2 the current flowing through Q2 and Q3 is likewise controlled. A further advantage of this scheme is that Q4, Q5 and R2 can be placed in the same isolation tub.

An alternative to the use of the vertical pnp is the compound npn-pnp circuit of Figure 2-17. Keeping in mind the poor frequency and phase response of the lateral pnp, the loop formed from Q3 and Q6 has the potential danger of instability, however.

CLASS A EMITTER FOLLOWER

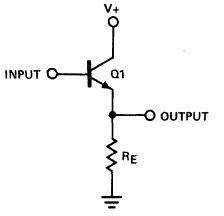


Figure 2-15a

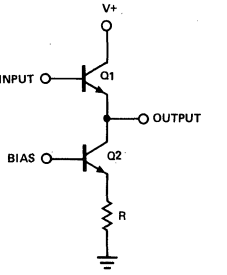
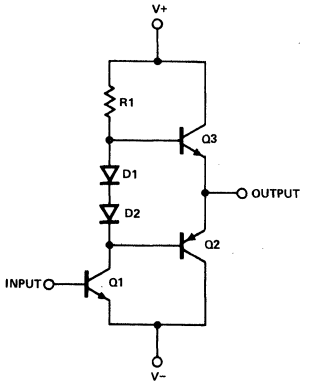


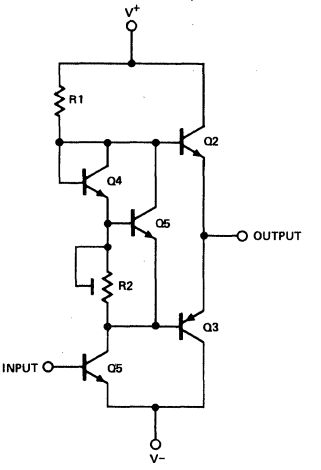
Figure 2-15b

COMPLEMENTARY OUTPUT STRUCTURE



With Diode Biasing

Figure 2-16a



Transistor Biasing

Figure 2-16b

OUTPUT PROTECTION

Output stages are commonly protected so that the maximum current available does not damage the device. A circuit achieving this is shown in Figure 2-18.

As the output current increases the voltage drop across R1 rises sufficiently to turn on Q1, which in turn removes some base drive from Q3. The output current is thus limited to the value specified by the IR drop of R1. Currents in the negative direction are likewise limited by R2 and Q2 acting upon Q4.

LATERAL PNP COMPLEMENTARY OUTPUT STAGE

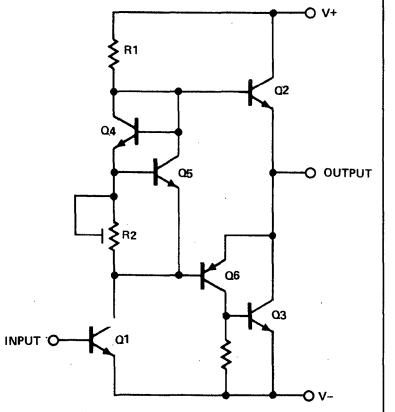


Figure 2-17

COMPLEMENTARY OUTPUT STAGE WITH SHORT CIRCUIT PROTECTION

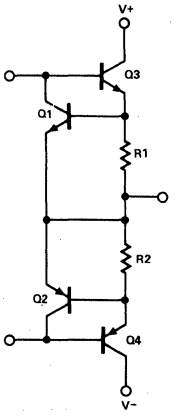


Figure 2-18

Often times the current handled by Q4 is large. If this is the case, the base drive at Q4 must be large to overcome low beta in the pnp. Hence Q2 must handle large currents to effect output protection. For this reason negative current limiting is often installed at earlier stages of a design so that smaller Q2 collector currents are required to control the output.

REACTIVE COMPONENT SIMULATION

Earlier in this chapter component limitations of linear IC design were discussed. These limitations restricted the values of resistance and capacitance in addition to the non existence of the inductor for linear design. Techniques circumventing the resistor limitations, such as current source loads, have been covered. Methods of multiplying capacitance and simulating inductance have also been developed for use in linear IC design.

In both cases the general method is to incorporate the oxide capacitors available into an active feedback configuration to synthesize the desired impedance.

Capacitive multiplication is done using the circuit of Figure 2-19. The effective capacitance is given by the relationship:

$$C_{eff} = C\left(\frac{R1}{R3}\right)$$

Values of resistance for R1 should be as high as possible since the impedance appears in series with the effective capacitance.

CAPACITANCE MULTIPLIER

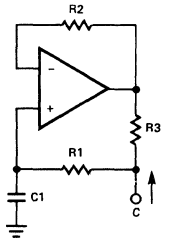


Figure 2-19

Virtual inductors can be synthesized from active devices as well. With a constant current excitation, the voltage dropped across an inductance increases with frequency. Thus an active device whose output increases with frequency can be characterized as an inductance. The circuit of Figure 2-20 yields such a response with the effective inductance being equal to:

$$L = R_1R_2C$$

SIMULATED INDUCTOR

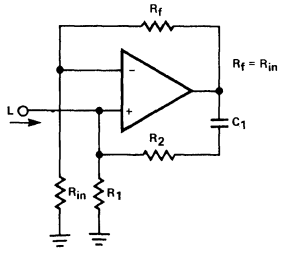


Figure 2-20

The Q of this inductance depends upon R1 being equal to R2. At this point the Q of the inductor is maximum. At the same time, however, the positive and negative feedback paths of the amplifier are equal leading to the distinct possibility of oscillation at high frequencies. R1 should therefore always be slightly smaller than R2 to assure stable operation.

LAYOUT CONSIDERATIONS

Of paramount importance to the layout of a linear circuit is the chip size. Every possible effort is made to reduce chip size for economic reasons.

In general, the transition of a circuit design to a layout of its monolithic form is by way of design rules which give the minimum and maximum spacing between oxide openings of both the same and other diffusions. These rules take into account various process parameters and tolerances. Besides these general rules there are some particular considerations.

First is optimization of matching between similar components. This is accomplished by placing components as close as possible so that the differences due to microvariations are minimized. In the case of transistors this means placing them in adjacent isolation tubs. For resistors this means running them parallel with identical numbers of corners and with identical end-contacts.

Another consideration is component matching in the presence of thermal transients. This is a common problem with operational amplifiers where thermal transients of the output transistors can reflect back to the input transistors. A layout that could exhibit this effect is shown in Figure 2-21.

As the output drives the load the power dissipation from output transistors Q3 and Q4 cause thermal gradients across the die. Transistors Q1 and Q2 receive a thermally generated voltage difference of 2mV per degree centigrade. Since operational amplifiers such as the 531 have voltage gains in excess of 100dB, the voltage need only be 20-200μV to produce output saturation.

The layout example of Figure 2-21 would generate large offset voltages as well as make accurate gain measurements impossible. The modifications required to eliminate temperature variations have been illustrated in Figure 2-22. Here the power dissipating elements are situated on the die center line. All temperature sensitive elements, such as Q1 and Q2, are placed symmetrically about the center line.

CHIP LAYOUT WITH THERMAL SYMMETRY

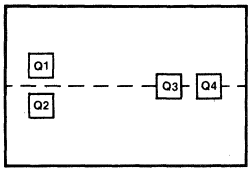


Figure 2-22

POOR THERMAL LAYOUT

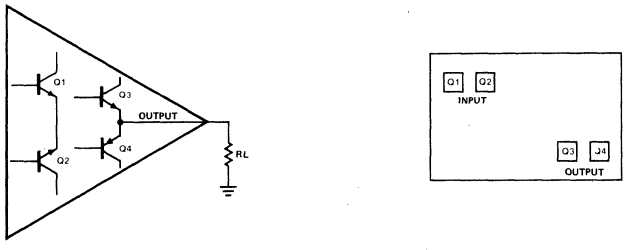


Figure 2-21

Die layout is also important with respect to ground current feedback. A good example occurs when both digital and linear circuitry appear on the same chip, as with sense amplifiers.

A functional block diagram of the sense amplifier with parasitic resistances R1 and R2 is shown in Figure 2-23. Resistors R1 and R2 represent the impedance of the die metalization.

PARASITIC RESISTANCE IN GROUND LINES

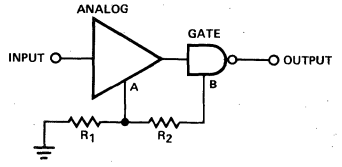


Figure 2-23

When the TTL gate output switches large ground currents occur on the gate ground leads. This transient current flows through R1 and R2, raising the voltage at points A and B. These potentials can cause positive (or negative) feedback which can alter the ideal transfer curve of Figure 2-24a to that of Figure 2-24b. Both discontinuities and hysteresis are evident.

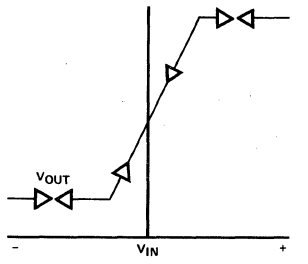
The improved method of grounding is illustrated in Figure 2-25. Ground paths have been arranged so that currents sum only at the common ground pad of the die. In addition, ground metalization has been widened to reduce metal resistance.

As stated earlier, minimizing die area is important. One of the ways this can be done is by placing many components in a single isolation area. There are dangers in doing this however, due to the presence of parasitic components. To illustrate, the emitter follower circuit of Figure 2-26 will be used.

To save space both components are diffused in the same isolation tub as shown by Figure 2-27. The transistor collector contact serves the dual role of collector contact and reverse biasing of the resistor as required. Danger arises as the transistor current increases.

The voltage drop in the N-epi region becomes larger, eventually forward biasing part of the resistor. The circuit of Figure 2-28 applies should forward biasing occur, adding a parasitic pnp transistor between the resistor and the npn transistor base. If the beta is high enough a regenerative loop occurs causing latch up. The solution lies in locating the resistor out of the transistor current path.

SENSE AMPLIFIER TRANSFER CURVE



Ideal

Figure 2-24a

HYSTERESIS DUE TO GROUND CURRENTS

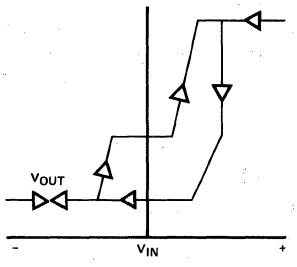


Figure 2-24b

IMPROVED SENSE AMPLIFIER LAYOUT

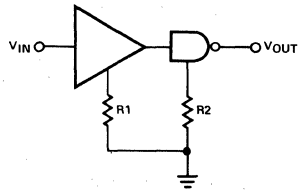


Figure 2-25

EMITTER FOLLOWER CIRCUIT

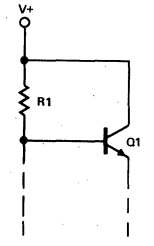


Figure 2-26

CROSS SECTIONAL OF EMITTER FOLLOWER CIRCUIT

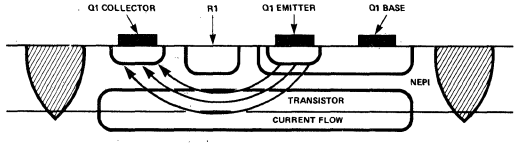


Figure 2-27

Summary:

The preceding two chapters have been devoted to a basic treatise of linear design and processing techniques. Although severely limited in depth, the knowledge presented should provide a great deal of insight into understanding linear circuits, their capabilities and limitations.

EMITTER WITH PARASITIC PNP TRANSISTOR

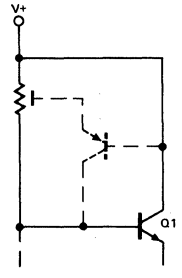


Figure 2-28

SECTION 20
OPERATIONAL AMPLIFIERS

INTRODUCTION

The operational amplifier was first introduced in the early 1940's. Primary usage of these vacuum tube forerunners of the ideal gain block was in computational circuits. They were fed back in such a way as to accomplish addition, subtraction, and other mathematical functions.

Expensive and extremely bulky, the operational amplifier found limited use until new technology brought about the integrated version, solving both size and cost drawbacks.

Volumes upon volumes have been and could be written on the subject of op amps. In the interest of brevity this chapter will cover the basic op amp as it is defined along with test methods and suggestive applications. Also, included is a basic coverage of the feedback theory from which all configurations can be analyzed.

THE PERFECT AMPLIFIER

The ideal operational amplifier possesses several unique characteristics. Since the device will be used as a gain block, the ideal amplifier should have infinite gain. By definition also, the gain block should have an infinite input impedance in order not to draw any power from the driving source. Additionally, the output impedance would be zero in order to supply infinite current to the load being driven. These ideal definitions are illustrated by the ideal amplifier model of Figure 3-1.

IDEAL OPERATIONAL AMPLIFIER

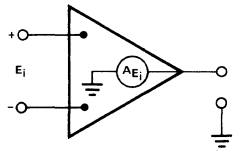


Figure 3-1

Further desirable attributes would include infinite bandwidth, zero offset voltage, and complete insensitivity to temperature, power supply variations, and common mode input signals.

Keeping these parameters in mind, further contemplation produces two very powerful analysis tools. Since the input impedance is infinite, there will be no current flowing at the amplifier input nodes. In addition, when feedback is employed the differential input voltage reduces to zero. These two statements are used universally as beginning points for any network analysis and will be explored in detail later on.

THE PRACTICAL AMPLIFIER

Tremendous strides have been made by modern technology with respect to the ideal amplifier. Integrated circuits are coming closer and closer to the ideal gain block. Input bias currents for instance are in the 5pA range for FET input amplifiers while offset voltages have been reduced to less than 1mV in many cases.

Any device has limitations however, and the integrated circuit is no exception. Modern op amps have both voltage and current limitations. Peak to peak output voltage, for instance, is generally limited to one or two base-emitter voltage drops below the supply voltage while output current is internally limited to approximately 25mA. Other limitations such as bandwidth and slew rates are also present, although each generation of devices improves over the previous one.

DEFINITION OF TERMS

Earlier the ideal operational amplifier was defined. No circuit is ideal of course so practical realizations contain some sources of error. Most sources of error are very small and therefore can usually be ignored. It should be noted that some applications require special attention to specific sources of error.

Before the internal circuitry of the op amp is further explored it would be beneficial to define those parameters commonly referenced.

INPUT OFFSET VOLTAGE

Ideal amplifiers produce 0 volts out for 0 volts input. But, since the practical case is not perfect, there will appear a small dc voltage at the output even though no differential voltage is applied. This dc voltage is called the input offset voltage, with the majority of its magnitude being generated by the differential input stage pictured in Figure 3-2.

An operational amplifier's performance is in large part dependent upon the first stage. It is the very high gain of the first stage that amplifies small signal levels to drive remaining circuitry. Coincidentally, the input current, a function of beta, must be as small as possible. Collector current levels are thus made very low in the input stage in order to gain low bias currents. It is this input stage also which determines dc parameters such as offset voltage since the amplified output of this stage is of sufficient voltage levels to eclipse most subsequent error terms added by the remaining circuitry. Under balanced conditions the collector currents of Q1 and Q2 are perfectly matched, hence we may say:

DIFFERENTIAL INPUT STAGE

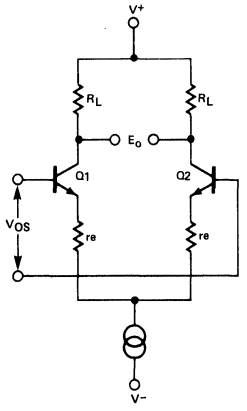


Figure 3-2

$$E_{OS} = I_{C2}R_L - I_{C1}R_L = 0$$

In practice small differences in geometries of the base emitter regions of Q1 and Q2 will cause E_{OS} not to equal 0. Thus, for balance to be restored a small dc voltage must be added to one V_{BE} or

$$V_{OS} = V_{BE1} - V_{BE2}$$

where the V_{BE} of the transistor is found by

$$V_{BE} = \frac{kT}{q} \ln\left(\frac{I_E}{I_S}\right)$$

Reference is made to the input when talking of offset voltage. Thus, the classic definition of input offset voltage is 'that differential dc voltage required between inputs of an amplifier to force its output to zero volts.'

Offset voltage becomes a very useful quantity for the designer because many other sources of error can be expressed in terms of V_{OS}. For instance, the error contribution of input bias current can be expressed as offset voltages appearing across the input resistors.

INPUT OFFSET VOLTAGE DRIFT

Another related parameter to offset voltage is V_{OS} drift with temperature. Present day amplifiers usually possess V_{OS} drift levels in the range of 5μV to 40μV per degree C. The magnitude of V_{OS} drift is directly related to the initial offset voltage at room temperature. Amplifiers exhibiting larger initial offset voltages will also possess higher drift rates with temperature. A rule of thumb often applied is that the drift per degree C will be 3.3μV for each millivolt of initial offset. Thus, for tighter control of thermal drift, a low offset amplifier would be selected.

INPUT BIAS CURRENT

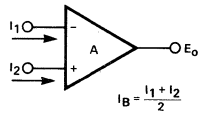


Figure 3-3

INPUT BIAS CURRENT

Again referring to Figure 3-2, it is apparent that the input pins of this op amp are base inputs. They must, therefore, possess a dc current path to ground in order for the input to function. Input bias current, then is 'the dc current required by the inputs of the amplifier to properly drive the first stage.'

The magnitude of I_{bias} is calculated as the average of both currents flowing into the inputs and is calculated from

$$I_B = \frac{I_1 + I_2}{2}$$

Bias current requirements are made as small as possible by using high beta input transistors and very low collector currents in the first stage. The trade-off for bias current is lower stage gain due to low collector current levels and lower slew rates. The effect upon slew rate is covered in detail under the compensation section.

INPUT OFFSET CURRENT

The ideal case of the differential amplifier and its associated bias current does not possess an input offset current. Circuit realizations always have a small difference in bias currents from one input to the other, however. This difference is called the input offset current. Actual magnitudes of offset current are usually at least an order of magnitude below the bias current. For many applications this offset may be ignored but very high gain, high input impedance amplifiers should possess as little I_{os} as possible because the difference in currents flowing across large impedances develops substantial offset voltages. Output voltage offset due to I_{os} can be calculated by

$$V_{out} = A_{cl}(I_{os}R_s)$$

Hence, high gain and high input impedances magnify directly to the output, the error created by offset current. Circuits capable of nulling the input voltage and current errors are available and will be covered later in this chapter.

INPUT OFFSET CURRENT DRIFT

Of considerable importance is the temperature coefficient of input offset current. Even though the effects of offset are nulled at room temperature, the output will drift due to changes in offset current over temperature. Many popular models now include a typical specification for I_{os} drift with values ranging in the .5nA per degree C area. Obviously those applications requiring low input offset currents also require low drift with temperature.

INPUT IMPEDANCE

Differential and common mode impedances looking into the input are often specified for integrated op amps. The differential impedance is the total resistance looking from one input to the other while common mode is the common impedance as measured to ground. Differential impedances are calculated by measuring the change of bias current caused by a change in the input voltage.

COMMON MODE RANGE

All input structures have limitations as to the range of voltages over which they will operate properly. This range of voltages impressed upon *both inputs* which will not cause the output to misbehave is called the common mode range. Most amplifiers possess common mode ranges of ±12 volts with supplies of ±15 volts.

COMMON MODE REJECTION RATIO

The ideal operational amplifier should have no gain for an input signal common to both inputs. Practical amplifiers do have some gain to common mode signals. The classic definition for common mode rejection ratio of an amplifier is the ratio the differential signal gain to the common mode signal gain expressed in dB as shown in equation 3-6a.

$$CMRR(dB) = 20 \log \frac{e_o/e_i}{e_o/e_{cm}}$$

The measurement CMRR as in 3-6a requires 2 sets of measurements. However note that if e_o in equation 3-6a is held constant, CMRR becomes:

$$CMRR(dB) = 20 \log \frac{e_{cm}}{e_i} \Big/ e_o = K$$

A new alternate definition of CMRR based on 3-6b is the ratio of the change of input offset voltage to the input common made voltage change producing it.

EFFECTS OF CMRR ON VOLTAGE FOLLOWER

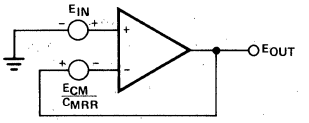


Figure 3-4

Figure 3-4 illustrates the application of the equivalent common mode error generator to the voltage follower circuit. The gain of the voltage follower with error contributions caused by both finite gain and finite common mode rejection ratio is shown in equation 3-7.

$$\frac{e_o}{e_{in}} = \frac{1 \pm 1/CMRR}{1+1/A}$$

AC PARAMETERS

Parameter definition has up to this point, been dealing primarily with dc quantities of voltages, currents, etc. Several important ac or frequency dependent parameters will now be discussed.

An ideal gain block was defined earlier as one which would provide infinite gain and bandwidth. Real circuits approximate infinite open loop gain with low frequency gains in excess of 100dB. The very high gains achieved with present designs are possible only by cascading stages. Although providing very high open loop gain the cascading of stages results in the need for frequency compensation in closed loop configurations and reduces the open loop.

LARGE SIGNAL BANDWIDTH

The large signal or power bandwidth of an amplifier refers to its ability to provide its maximum output voltage swing with increasing frequency. At some frequency the output will become slew rate limited and the output will begin to degrade. This point is defined by

$$F_{PL} = \frac{\text{Slew Rate}}{2\pi \cdot E_{out}}$$

where F_{PL} is the upper power bandwidth frequency and E_{out} is the peak output swing of the amplifier.

SLEW RATE

The maximum rate of change of the output in response to a step input signal is termed a slew rate. Deviation from the ideal is caused by the limitation in frequency response of the amplifier stages and the phase compensation technique used. Summing node and amplifier output capacitances must be kept to a minimum to guarantee getting the maximum slew rate of the operational amplifier. Circuit board layout must also be of high frequency quality. Power supplies should be adequately bypassed at the pins, with both low and high frequency components to avoid possible ringing. A selection of a proper capacitor in parallel with the feedback resistor may be necessary. Too small a value could result in excessive ringing and too large a value will decrease

frequency response. In general, the worst case slew rate is in the unity gain noninverting mode. Specifications of slew rate should always reflect this worst case condition with the maximum required compensation network.

AMPLIFIER SLEW RATE LIMITATIONS

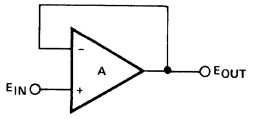


Figure 3-5a

AMPLIFIER SLEW RATE LIMITATIONS

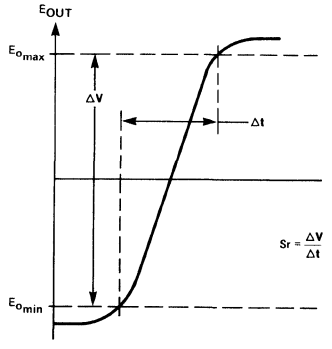


Figure 3-5b

FREQUENCY RESPONSE

Distributed capacitances and transit times in semiconductors cause an upper frequency limit or pole for each and every gain stage. Monolithic pnp transistors used for level shifting possess poor upper frequency characteristics and cascaded gain stages, used to approach the highest gain, subtract from the maximum frequency response. As shown in Figure 3-6 the open loop frequency response of most op amps crosses unity gain at 10MHz. Closed loop response is unstable without compensation however, so typical unity gain frequencies are readjusted to approximately 1MHz by the effects of phase compensation.

From Figure 3-6 it is also apparent that an amplifier has a trade off between gain and bandwidth. Higher gains are achieved at the expense of bandwidth. This trade off is a constant figure called the gain bandwidth product.

TEST METHODS

Product testing of all integrated circuits is

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

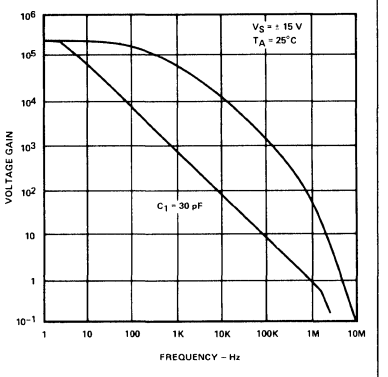


Figure 3-6

very rapid using state of the art automatic test equipment. Large computer controlled test decks test all data sheet limits in a matter of milliseconds. Each parameter is tested in a specific circuit configuration defined by the test hardware.

A typical simplified op amp test configuration is depicted by Figure 3-9. Units may be classed in several categories according to selected parameters. Even failures may be classified categorically depending upon their mode of failure.

Figures 3-7, 3-8, 3-10, and 3-11 illustrate the general test set ups commonly used to measure CMRR, average bias current, offset voltage and current and open loop gain respectively. In general the following parameters are tested under the following conditions.

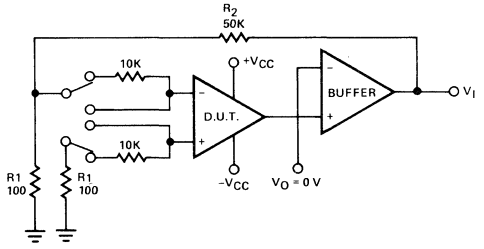
COMMON MODE REJECTION

The test set-up for CMRR is given in Figure 3-7. Resistor values are chosen to provide sufficient sensitivity and accuracy for the device type being tested and the voltage measuring equipment being used.

The positive common mode input voltage within the range V_{CM1} is algebraically subtracted from all supply voltages and from V_O. Then V_I is measured. The most negative common mode voltge within the range, V_{CM2}, is then subtracted from all the supply voltages and V_O, and V_I is again measured. Then

$$CMRR = (R1 + R2)/R1\,|(V_{CM1} - V_{CM2})/V_{11} - V_{12}$$

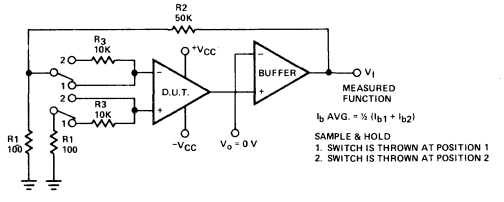
CIRCUIT DIAGRAM USED FOR CMRR MEASUREMENT



All resistor values are in ohms.

Figure 3-7

CIRCUIT DIAGRAM USED FOR AVERAGE BIAS CURRENT MEASUREMENT



All resistor values are in ohms.

Figure 3-8

A TYPICAL OP AMP TEST CIRCUIT (SIMPLIFIED)

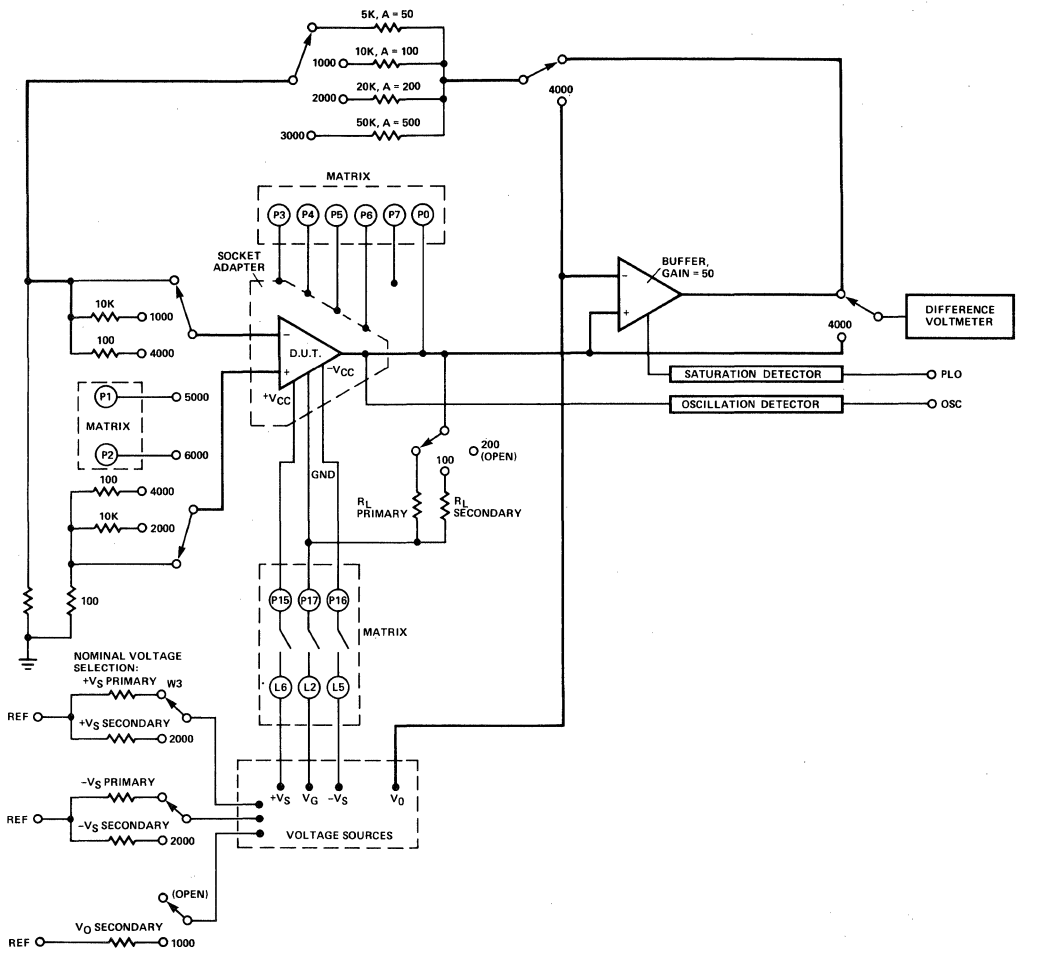
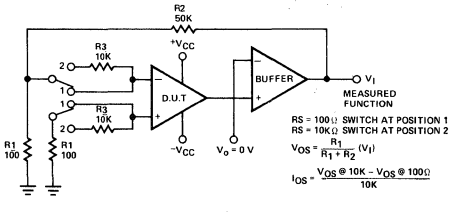


Figure 3-9

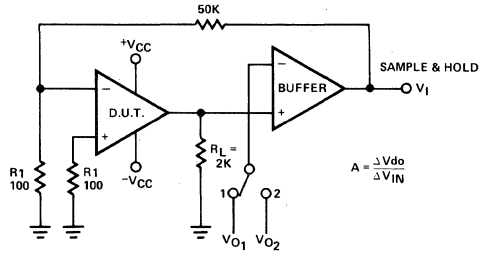
CIRCUIT DIAGRAM USED FOR OFFSET VOLTAGE AND OFFSET CURRENT



All resistor values are in ohms.

Figure 3-10

CIRCUIT DIAGRAM USED FOR LARGE-SIGNAL OPEN LOOP GAIN MEASUREMENT



All resistor values are in ohms.

Figure 3-11

This operation is equivalent to swinging both inputs over the full common mode range, and holding the output voltage constant, but it makes the V_I measurement much simpler.

BIAS CURRENT

Bias current is measured in the configuration of Figure 3-8.

With switches at position 1 and $V_O = 0$ volts, measure V_I1. Move switches to position 2 and again measure V_I2. Calculate I_{BIAS} (average), by

$$I_{B1} = \frac{R1}{R1 + R2}\left(\frac{V_I}{R3}\right)$$

$$I_{B2} = \frac{R1}{R1 + R2}\left(\frac{V_I}{R3}\right)$$

$$I_{BIAS\ (avg)} = \frac{I_{B1} + I_{B2}}{2} = \frac{R1}{R1 + R2}\,\frac{V_{I1} - V_{I2}}{2R3}$$

OFFSET VOLTAGE

Figure 3-10 is used for both offset voltage and current. With V_O at 0 volts and the switches selecting the source impedance, the offset voltage is measured at V_I and is equal to

$$V_{os} = \frac{R1V_I}{R1 + R2}$$

OFFSET CURRENT

Offset current is measured by calculation of offset voltage change with a change in source impedance. With switches in position 1, measure V_{I2}. Calculate the contribution of I_{os} by

$$I_{os} = \frac{V_{I2}\text{-}V_{I1}}{R3}$$

SIGNAL GAIN

The signal gain of operational amplifiers is most commonly specified for the full output swing.

This is referred to as large signal voltage gain and can be measured by the circuit of Figure 3-11. Usually specified under a specific load determined by R_L, a signal equal to the maximum swing of the output voltage is applied to V_O in both positive and negative directions. V_{I1} and V_{I2} are measured values of V_I and and V_O = maximum positive and maximum negative signals respectively. The gain of the device under test then becomes

$$A_{VO} = \left(\frac{R1 + R2}{R1}\right)\left(\frac{V_{O1} - V_{O2}}{V_{I1} - V_{I2}}\right)$$

SLEW RATE

Many other parameters are checked automatically by similar means. Only the most important ones have been covered here. Of great interest to the designer are other parameters which do not necessarily carry minimum or maximum limits. One such parameter is slew rate. The configuration used to measure slew rate depends upon the intended application. Worst case conditions arise in the unity gain non-inverting mode.

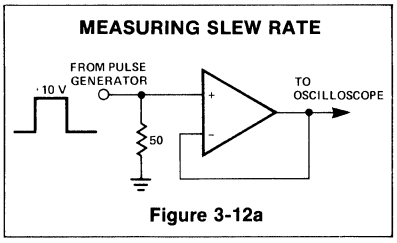


Figure 3-12a

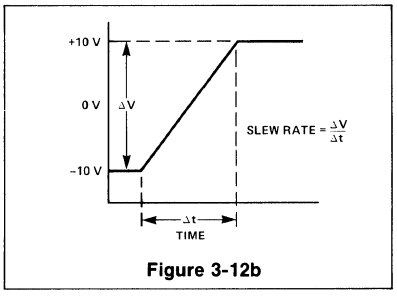


Figure 3-12b

Figure 3-12 shows a typical bench set up for measuring the response of the output to a step input. The input step frequency should be of a frequency low enough for the output of the op amp to have sufficient time to slew from limit to limit. In addition, V_{in} must be less than absolute maximum input voltage and the wave form should have good rise and fall times. The slew rate is then calculated from the slope of the output voltage versus time or

$$S_R = \frac{V_{out}}{T} \quad \text{in volts/}\mu s$$

OP AMP CURVE TRACER

Two of the most important parameters of linear integrated circuits having differential inputs are voltage gain and input offset voltage. These parameters may be read directly from a plot of the transfer characteristic of the device. This memo will describe a very simple curve tracer which, when used with an oscilloscope, will display the transfer characteristic of most Signetics linear devices.

Figure 3-13 shows the transfer characteristic of a typical linear device, the Signetics 531. Note that the unit saturates at approximately +12 and -12 volts and exhibits a linear transfer characteristic between -10 and +10 volts.

From the slope of this linear portion of the transfer characteristic, and from the point

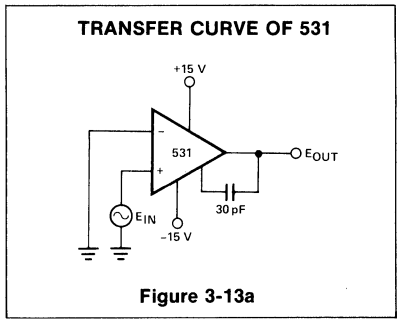


Figure 3-13a

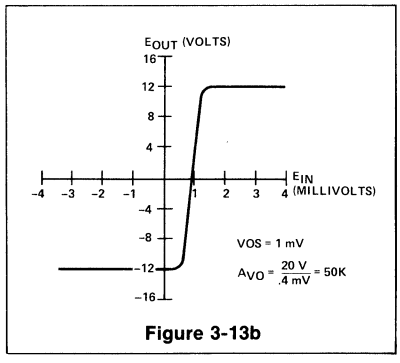


Figure 3-13b

where it crosses the e_{in} axis, the voltage gain and offset voltage may be determined. It can be seen that the voltage gain of the device under test, (D.U.T.), is 50,000 and its input offset voltage is 1.0mV.

A simple circuit to display the curves of Figure 3-13 on an oscilloscope is shown in Figure 3-14. A 60Hz, 44Vp-p sinewave is applied to the horizontal input of oscilloscope and an attenuated version of the sinewave is applied to the input of the D.U.T.

The output of the D.U.T. drives the vertical input of the scope. For providing V+and V– to the D.U.T., the tester uses two simple adjustable regulators, both current limited at 25mA. Input drive to the D.U.T. may be selected by means of S-2 as shown.

To use the curve tracer, first preset the V+ and V– supplies with an accurate meter. The supply voltages are somewhat dependent on ac line regulation and should be checked periodically. The horizontal gain of the scope may be set to give a convenient readout of the peak-to-peak D.U.T. input signal corresponding to the setting of S-2. As some devices have two outputs, a second output line (vertical 2) has been provided for these devices. The transfer function of such devices will be inverted to that of Figure 3-13 of course.

CURVE TRACER SCHEMATIC

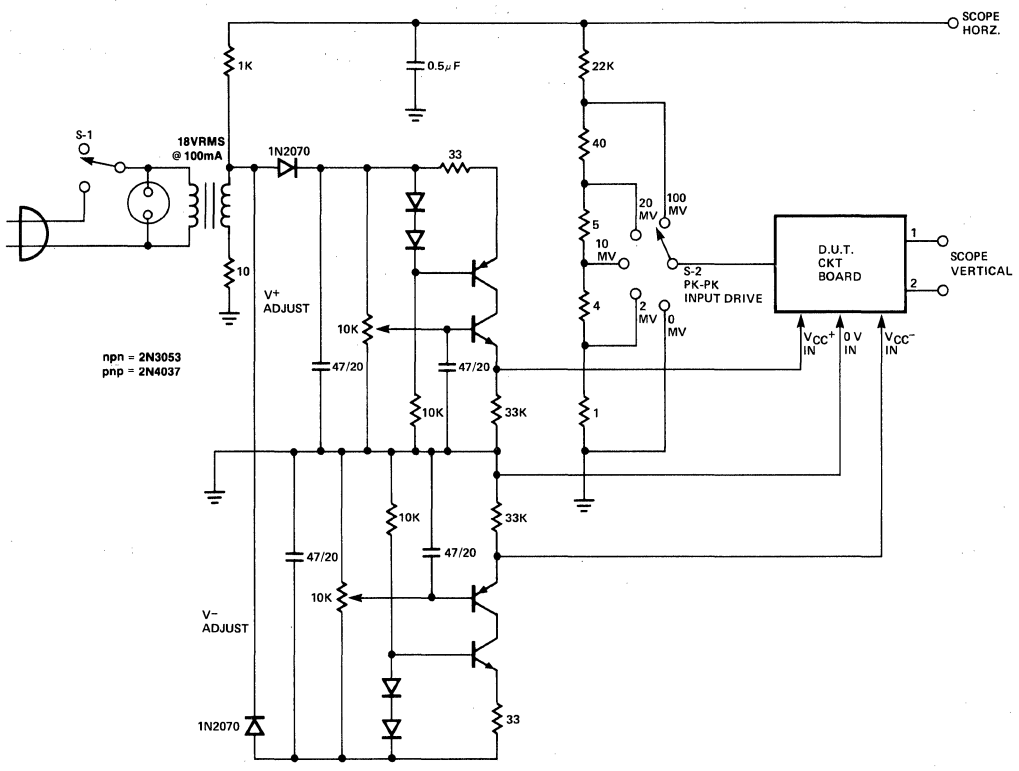


Figure 3-14

Simplicity and low cost are the two major attributes of this tester. It is not intended to perform highly rigorous tests for all devices. It is, however, a reasonably accurate means of determining the gains and offset voltages of most amplifiers. It will in addition, indicate the transfer curves of comparators and sense amplifiers with equivalent accuracies.

AMPLIFIER DESIGN

Linear operational amplifier IC's were introduced soon after the appearance of the first digital integrated circuits. The performance of these early devices, however, left much to be desired until the introduction of the 709 device. Even with its lack of short circuit protection and its complicated compensation requirements, the 709 gained real acceptance for the IC op amp. The 709 was designed using a three stage approach requiring both input and output stage compensation. In addition the output stage was not short circuit proof and the input stage latched up under certain conditions, requiring external protection.

Much better designs soon were introduced. Among the contenders were the 741, 748, 101, and 107 devices. All were general purpose devices with single capacitor compensation, (some were internally compensated), and all heralded input and output overstress protection. The basic design has two gain stages. By rolling off the frequency response of one of these, (the second stage), so that the overall gain is unity at a frequency below the point where excess phase becomes significant, the device can be stabilized for all feedback configurations. Further, by making the first stage a voltage to current converter, with a small g_m and the second stage a current to voltage converter with a high r_m, the second stage can be rolled off at 6dB octave with a small value capacitor in the order of 30pF, which can then be built into the device itself. This concept is shown in Figure 3-15.

BASIC TWO STAGE OP AMP DESIGN

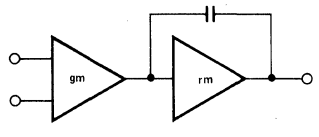


Figure 3-15

The frequency and phase response of the pnp devices in the first stage dictate a roll off in the second stage to give a loop gain of unity at about 1.0MHz. For the unity gain feedback configuration, this implies an open loop gain of unity at this frequency. The capacitor C_c controls this parameter by looking much smaller than r_m at frequencies above a few cycles, giving a clean 6dB/octave roll off over 5 decades.

The overall gain at frequencies where the impedance of C_c dominates r_m is given by

$$A_V(\omega) = \frac{qI_{S1}}{4KT} \cdot \frac{1}{\omega Cc}$$

Substituting the value given above, we find that a capacitance of $C_c = 30pF$ gives a unity

SCHEMATIC OF 536

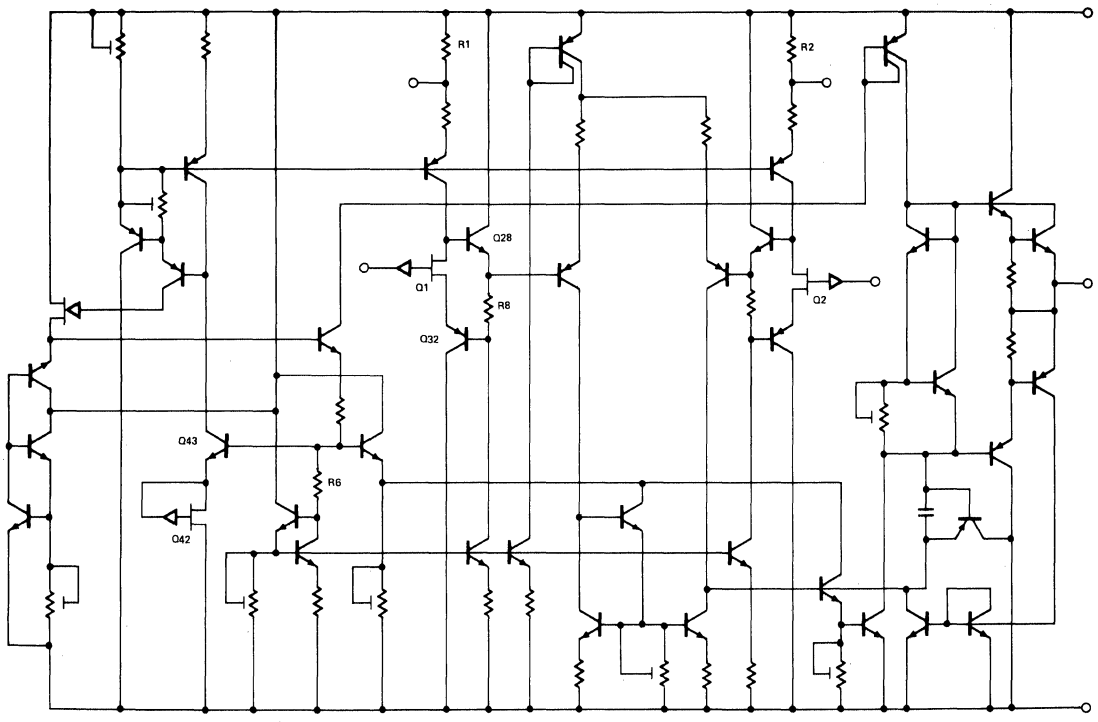


Figure 3-16

gain frequency of about 1.0MHz.

First stage large signal current also defines the slew rate for a specific compensation technique. It is this current which must charge and discharge the C_C by the expression

$$S_R = \frac{dV}{dT} = \frac{I_{LS}}{C_C}$$

where I_{LS} is the largest signal current of the input stage. Obviously, the slew rate can be improved by increasing the first stage collector current. This would, however, reflect directly upon the bias current by increasing it.

Two serious limitations, then, of these devices for diverse applications are input bias current and slew rate. Both may be overcome with small changes of the input structure to yield higher performance devices.

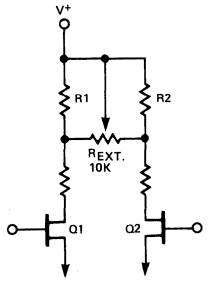
Reducing the input bias current becomes a matter of raising the transistor beta of the first stage. Several current designs boasting very low input currents use what is termed super beta input devices. These transistors have betas of 1,500 to 7,000. Bias currents under 2nA can be achieved in this way. Even though the B_{VCEO} of such transistors can be as low as 1 volt, the lower breakdowns are accounted for in the input stage by rearranging the bias technique. Bandwidths and slew rates suffer only slightly as a result of the lower current levels.

Further reduction in room temperature input bias current can be achieved by the use of FET input devices. A, (slightly simplified), schematic of the 536 FET input op amp is given in Figure 3-16.

The majority of the 741 circuitry is preserved with the appropriate input and bias structural changes made to incorporate the junction FETs. The biasing of Q1 and Q2 is chosen to minimize offset voltage and drift. The voltage across Q1 is controlled by Q28, Q32, and R8 which is the same as that across R6 via Q42 and Q43. The operating points of Q1 and Q2 are closely controlled by the I_{DSS} of Q42 via their respective current sources. Offset adjustment is accomplished by trimming the values of R1 and R2 externally to equalize the currents through Q1 and Q2. Figure 3-17 illustrates the technique required.

FET input structures of this type can provide input bias, (gate leakage), currents on the order of 5pA at room temperature. However, unlike the input bias currents of bipolar devices, the input bias current changes rapidly with temperature, doubling in value for every 10° C rise in temperature. For high temperatures the bias current of FETs becomes only about 4 times lower than super beta structures.

OFFSET VOLTAGE ADJUSTMENT OF THE 536



All resistor values are in ohms.

Figure 3-17

The 536 offers the advantages of very high input impedance and higher slew rate. The increase in slew rates for the 536 is about 6 times that of a 741.

The second limitation of 101—741 devices is slew rate. As previously mentioned, the rate of change is dictated by the compensation capacitance as charged by the large signal current of the first stage. By altering the large signal gm of the first stage as depicted by Figure 3-18, the slew rate can be dramatically increased.

The additional current supplied during large signal swings by current source I4 causes the first stage transfer function to change as shown in Figure 3-19. The compensation capacitor is returned to the output of the 531 structure because the output driving source must be capable of supplying the increased current to charge the capacitor.

Large signal bandwidths with this input structure will be essentially the same as the small signal response. Full bandwidth possibilities of this configuration are still limited by the beta and f_t of the lateral pnp devices used for collector loads in the first stage. Even so, the slew rate of the 531 and 538 is a factor of 40 better than general purpose devices.

INPUT STRUCTURE OF 531

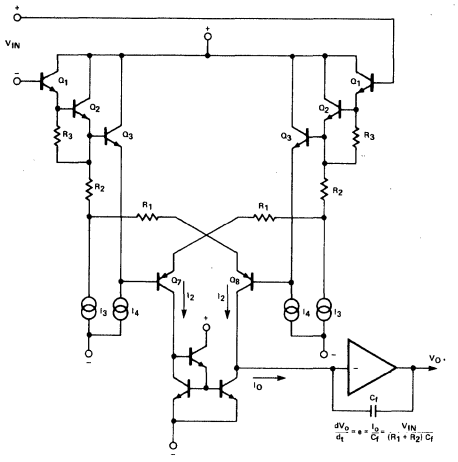


Figure 3-18

VOLTAGE/CURRENT CURVES OF FIRST STAGE

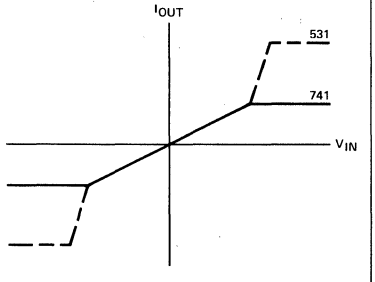


Figure 3-19

BASIC FEEDBACK THEORY

At the beginning of this chapter the ideal op amp was defined. The ideal parameters are never fully realized but they present a very convenient method for the preliminary analysis of circuitry. So important are these ideal definitions that they are repeated here. The ideal amplifier possesses:

1. Infinite gain
2. Infinite input impedance
3. Infinite bandwidth
4. Zero output impedance

From these definitions two important theorems are developed:

1. No current flows into or out of the input terminals.
2. When negative feedback is applied the differential input voltage is reduced to zero.

Keeping these rules in mind, the basic concept of feedback can be explored.

VOLTAGE FOLLOWER

Perhaps the most often used and simplest circuit is that of a voltage follower. The circuit of Figure 3-20 illustrates the simplicity.

VOLTAGE FOLLOWER

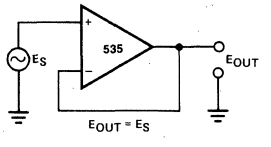


Figure 3-20

Applying the zero differential input theorem the voltages of pins 2 and 3 are equal and since pins 2 and 6 are tied together, their voltage is equal; hence, $E_{out} = E_{in}$. Trivial to analyze, the circuit nevertheless does illustrate the power of the zero differential voltage theorem. Because the input impedance is multiplied and the output impedance divided by the loop gain the voltage follower is extremely useful for buffering voltage sources and for impedance transformation.

NON-INVERTING AMPLIFIER

Only slightly more complicated is the non-inverting amplifier of Figure 3-21.

NON-INVERTING AMPLIFIER

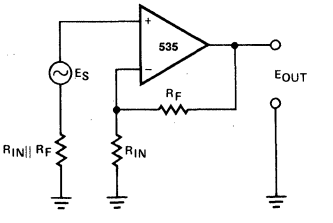


Figure 3-21

The voltage appearing at the inverting input is defined by

$$E2 = \frac{E_{out} \bullet R_{in}}{R_F + R_{in}}$$

Since the differential voltage is zero, E2 = E3, and the output voltage becomes

$$E_{out} = E_S \left(1 + \frac{R_F}{R_{in}}\right)$$

It should be noted that as long as the gain of the closed loop is small compared to open loop gain, the output will be accurate, but as the closed loop gain approaches the open loop value more error will be introduced.

The signal source is shown in Figure 3-21 in

series with a resistor equal in size to the parallel combination of R_{in} and R_F. This is desirable because the voltage drops due to bias currents to the inputs are equal and cancel out even over temperature. Thus overall performance is much improved.

INVERTING AMPLIFIER

By slightly rearranging the circuit of Figure 3-21, the non-inverting amplifier is changed to an inverting amplifier. The circuit gain is found by applying both theorems; hence, the voltage at the inverting input is 0 and no current flows into the input. Thus the following relationships hold.

$$\frac{E_{in}}{R_{in}} + \frac{E_o}{R_F} = 0$$

Solving for the output E_o

$$E_o = -E_{in}\frac{R_F}{R_{in}}$$

INVERTING AMPLIFIER

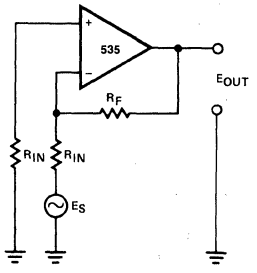


Figure 3-22

As opposed to the non-inverting circuits the input impedance of the inverting amplifier is not infinite but becomes essentially equal to R_{in}. This circuit has found widespread acceptance because of the ease with which input impedance and gain can be controlled to advantage, as in the case of the summing amplifier.

COMPENSATION

Present day operational amplifiers are comprised of multiple stages, each of which has a 3dB point or pole associated with it. Referring to Figure 3-23, the 3dB break points of a two stage amplifier are approximated by the Bode plot.

As with any feedback loop, the op amp must be protected from phase shifts in excess of 360°. A steady 180° phase shift is developed by the amplifier from output to inverting input. In addition the sum of all additional shifts due to amplifier poles or feedback component poles will cause the necessary additional 180° to sustain oscillation if the

FREQUENCY COMPENSATION

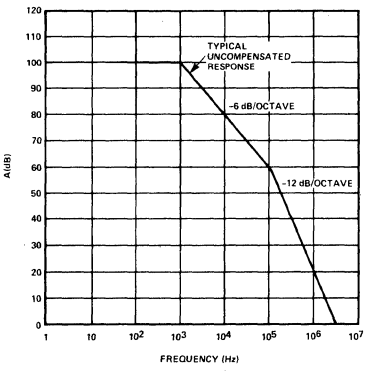


Figure 3-23

gain of the amplifier is greater than one for the frequency at which the 180° phase shift is reached. By adding poles and zeros to the amplifier response externally, the phase shift can be controlled to insure stability.

Many op amps now include internal compensation. These are single capacitors of 30pF typically and the amplifier will remain stable for all gains. However, since they are unconditionally stable, the compensation is larger than required for most applications. The resultant loss of bandwidth and slew rate may be acceptable in the general case but selection of an externally compensated device can add a great deal to the amplifier response if the compensation is handled properly.

In order to fully develop the point at which instability occurs a fuller understanding of phase response is necessary.

The diagram of Figure 3-24 depicts the phase shift of a single pole. Note that at the pole position the phase shift is 45° and that phase shift becomes 0° for a decade below the pole and -90° for a decade above the pole location. This is a Bode approximation which possesses a 5.7° error at 0° and 90° but this error is usually considered small enough to be ignored. The single pole produces a maximum of 90° phase shift and also produces a frequency roll off of 20dB per decade. The addition of the second pole of Figure 3-25 produces an additional 90° phase shift and increases the role off slope to -40dB per decade.

At this point phase shift could exceed 180° because unity gain is reached causing instability. For gain levels equal to A1 or $|1/\beta|$, the phase shift is only 90° and the amplifier is stable. However, the gain of A2 the phase shift is 180° and the loop is unstable. Gains in between A1 and A2 are

SINGLE POLE AMPLITUDE AND PHASE RESPONSE

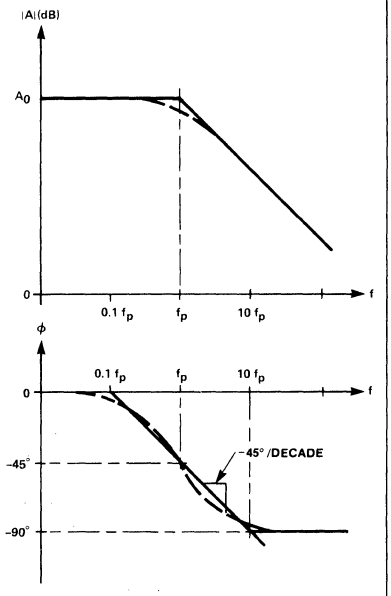


Figure 3-24

TWO POLE CLOSED LOOP RESPONSE

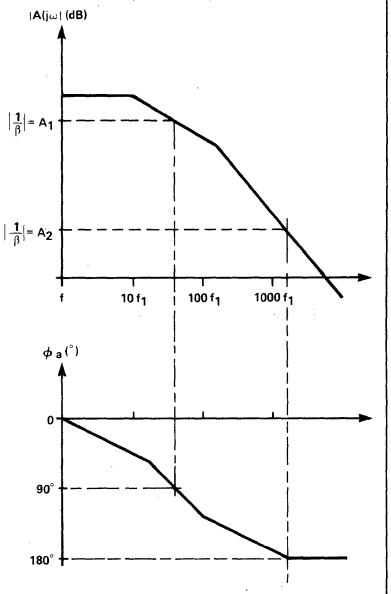


Figure 3-25

marginally stable. However, as shown in Figure 3-26 the phase shift as it approaches 180° causes increasing frequency peaking and overshoot until sustained oscillations occur.

FREQUENCY PEAKING DUE TO INSUFFICIENT PHASE MARGIN

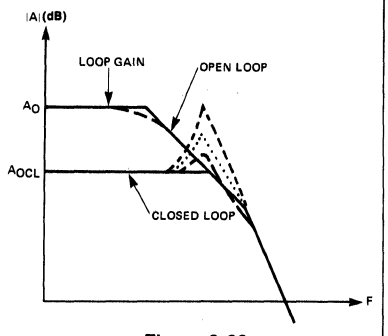


Figure 3-26

It is generally accepted in the interest of minimized frequency peaking to limit the phase shift of the amplifier to 135° or a phase margin of 45°. At this margin the second order response of the system is critically damped and oscillation is prevented.

Referring to Figure 3-27, the required compensation can be determined. Given the open loop response of the amplifier, the desired gain is plotted until it intercepts the open loop curve as shown.

FREQUENCY COMPENSATION

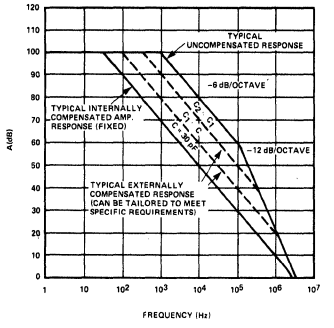


Figure 3-27

The phase shift for minimum peaking is 135°. Remembering that phase shift is 45° at the frequency pole the example of Figure 3-27 will be unstable at gains less than 20dB where phase shift exceeds 180°, and will possess excessive overshoot and ringing at gains less than 60dB where phase shift exceeds 135°. Thus, the desired compensation will move the second pole of the amplifier out in frequency until the closed loop gain intersects the open loop response before the second break of the amplifier occurs. Selecting only enough compensation to do the job assures the maximum bandwidths and slew rates of the amplifier. Additional in-depth information on compensation can be found in the reference material.

FEED FORWARD COMPENSATION

External compensation has been shown to improve amplifier bandwidth over internal compensation in the preceding section. Additional bandwidth can be realized if feed forward compensation is used. Bandwidth is limited in monolithic design by the poor frequency response of the pnp level shifters of the first stage.

TECHNIQUE OF FEED FORWARD AROUND 1st STAGE

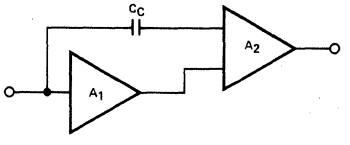


Figure 3-28a

FREQUENCY RESPONSE WITH FEED FORWARD COMPENSATION

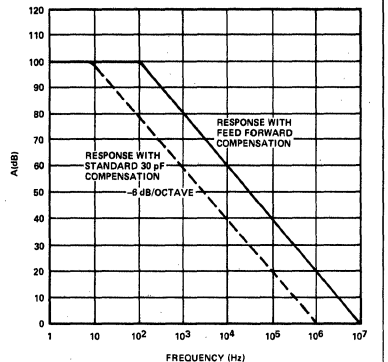
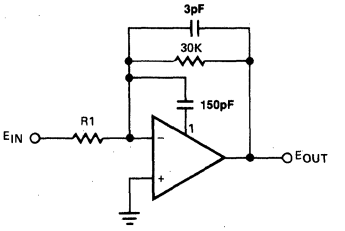


Figure 3-28b

FEED FORWARD COMPENSATION OF LM301



All resistor values are in ohms.

Figure 3-28c

The concept of feed forward compensation bypasses the input stage at high frequencies driving the higher frequency second stage directly as pictured by Figure 3-28a. The Bode plot of Figure 3-28b shows the additional response added by the feed forward technique used in Figure 3-28c. The response of the original amplifier requires less compensation at lower frequencies allowing an order of magnitude improvement in bandwidth. The typical feed forward network for the LM301 is shown in Figure 3-28c with its Bode plot in Figure 3-28b. Standard compensation and feed forward are both plotted to illustrate the bandwidth improvement. Unfortunately, the use of feed forward compensation is restricted to the inverting amplifier mode.

REFERENCES

1. *OPERATIONAL AMPLIFIERS-Design & Applications*, Jerald Graeme and Gene Tobey, McGraw Hill Book Company.

APPLICATIONS

Volumes upon volumes have been written describing circuits based on the operational amplifier. Space prohibits a lengthy discussion of each application. Rather the following pages are intended as a reference point from which one can digress to achieve a specific response. The most important things to remember were brought out in the basic feedback theory section. No application of op amps need be terribly difficult if the summing point restraints are remembered and applied.

VOLTAGE FOLLOWER

The basic configuration in Figure 3-29 has a gain of 1 with extremely high input impedance. Setting the feedback resistor equal to the source impedance will cancel the effects of bias current if desired.

VOLTAGE FOLLOWER

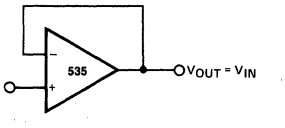


Figure 3-29

However, for most applications a direct connection from output to input will suffice. Errors arise from offset voltage, common mode rejection ratio and gain. The circuit can be used with any op amp with the required unity gain compensation, if it is required.

INVERTING AMPLIFIER

With the inverting amplifier of Figure 3-30 the gain can be set to any desired value defined by R2 divided by R1. Input impedance is defined by the value of R1, and R3 should equal the parallel combination of R1 and R2 to cancel the effect of bias current. Offset voltage, offset current, and gain contribute most of the errors. The ground may be set anywhere within the common mode range and any op amp will provide satisfactory response.

NON-INVERTING AMPLIFIER

Gain for the non-inverting amplifier is defined by the sum of R1 and R2 divided by R1.

The amplifier does not phase invert and possesses high input impedance. Again the impedances of the two inputs should be equal to reduce offsets due to bias currents.

INVERTING AMPLIFIER

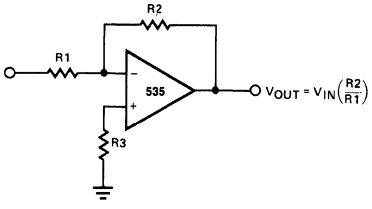


Figure 3-30

NON-INVERTING AMPLIFIER

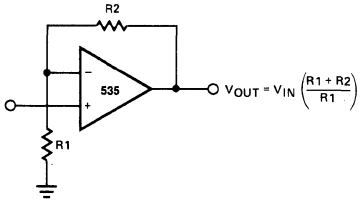


Figure 3-31

CURRENT TO VOLTAGE CONVERTER

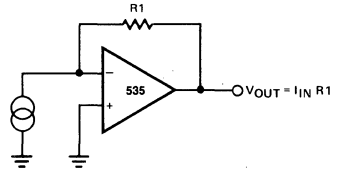


Figure 3-32

DIFFERENTIAL AMPLIFIER

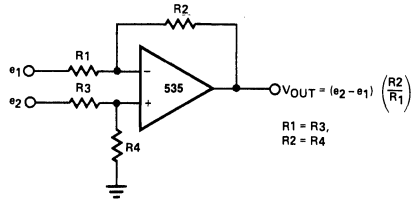


Figure 3-33

SUMMING AMPLIFIER

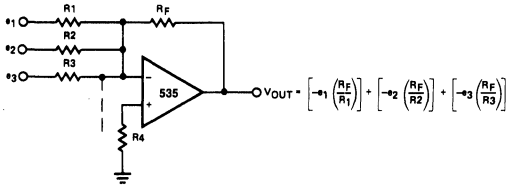


Figure 3-34

CURRENT TO VOLTAGE CONVERTER

The transfer function of the current to voltage converter is

$$V_{out} = R1 I_{in}$$

Evaluation of the circuit depends upon the virtual ground theorem developed earlier. The current flowing into the input must be the same as that flowing across R1, hence, the output voltage is the IR drop of R1.

Limitations of course are output saturation voltage and output current capability. The inputs may be biased anywhere within the common mode range.

DIFFERENTIAL AMPLIFIER

This circuit of Figure 3-33 has a gain with respect to differential signals of R2/R1.

The common mode rejection is dominated by the accuracy of the resistors. Other errors arise from the offset voltage, input offset current, gain and common mode rejection. The circuit can be used with any op amp discussed in this chapter with the proper compensation.

SUMMING AMPLIFIER

The summing amplifier is a variation of the inverting amplifier. The output is the sum of the input voltages, each being weighed by—R_F/R_{in}.

The value of R4 may be chosen to cancel the effects of bias current and is selected equal to the parallel combination of RF and all the input resistors.

INTEGRATOR

Integration can be performed with a variation of the inverting amplifier by replacing the feedback resistor with a capacitance. The transfer function is defined by

$$V_{out} = -\frac{1}{RC}\int_0^t V_{in} \bullet dt$$

The gain of the circuit falls at 6dB per octave over the range in which strays and leakages are small.

INTEGRATOR

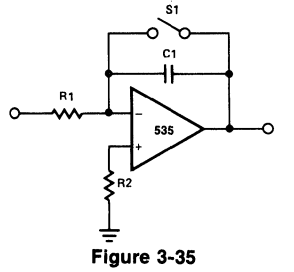


Figure 3-35

Since the gain at dc is very high a method for resetting initial conditions is necessary. Switch S1 removes the charge on the capacitor. A relay of FET may be used in the practical circuit. Bias and offset currents and offset voltage should be low in such an application.

DIFFERENTIATOR

The differentiator of Figure 3-36 is another variation of the inverting amplifier. The gain increases at 6dB per octave until it intersects the amplifier open loop gain, then decreases because of the amplifier bandwidth. This characteristic can lead to instability and high frequency noise sensitivity.

DIFFERENTIATOR

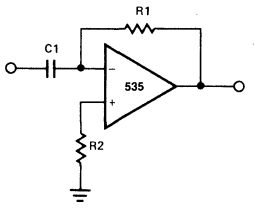


Figure 3-36

A more practical circuit is shown in Figure 3-37. The gain has been reduced by R3 and the high frequency gain reduced by C2 allowing better phase control and less high frequency noise. Compensation should be for unity gain.

PRACTICAL DIFFERENTIATOR

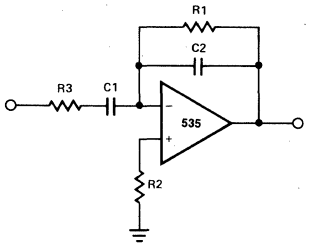


Figure 3-37

AUDIO CIRCUITS

Many audio circuits involve carefully tailored frequency responses. Pre-emphasis is used in all recording mediums to reduce noise and produce flat frequency response. The most often used de-emphasis curves for broadcast and home entertainment systems are shown in Figure 3-38. Operational amplifiers are well suited to these applications because of their high gain and easily tailored frequency response.

RIAA PREAMP

The preamplifier for phono equalization is shown in Figure 3-39, along with the theoretical and actual circuit response.

RIAA EQUALIZATION

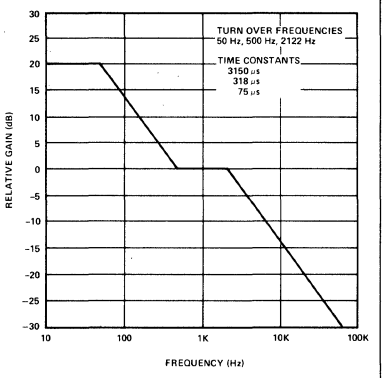


Figure 3-38a

NAB STANDARD PLAYBACK 7 1/2 IPS

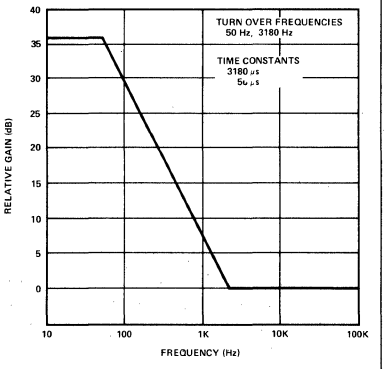


Figure 3-38b

3.75 IPS TAPE EQUALIZATION

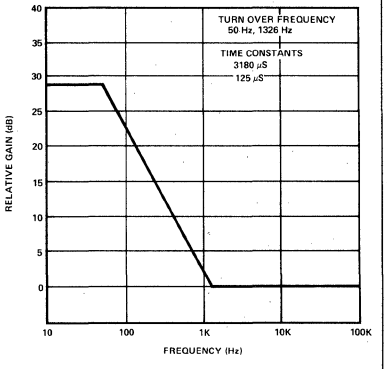


Figure 3-38c

BASE TREBLE CONTROL CURVE

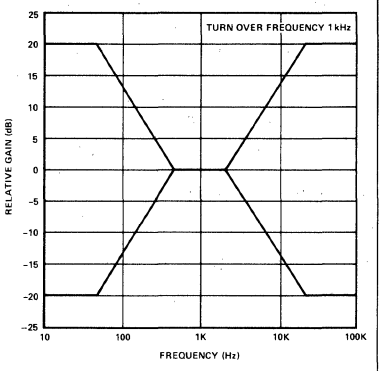


Figure 3-38d

STANDARD FM BROADCAST EQUALIZATION

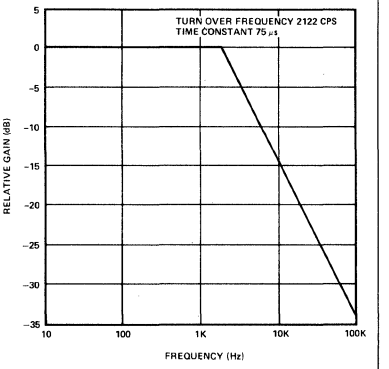


Figure 3-38e

Low frequency boost is provided by the inductance of the magnetic cartridge with the RC network providing the necessary break points to approximate the theoretical RIAA curve.

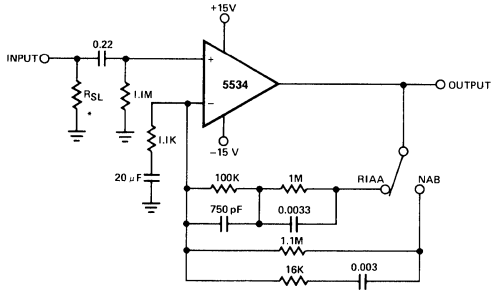
RUMBLE FILTER

Following the amplifier stage, rumble and scratch filters are often used to improve overall quality. Such a filter designed with op amps uses the 2 pole Butterworth approach and features switchable break points. With the circuit of Figure 3-40 any degree of filtering from fairly sharp to none at all is switch selectable.

TONE CONTROL

Tone control of audio systems involves altering the flat response in order to attain more low frequencies or more high ones dependent upon listener preference. The

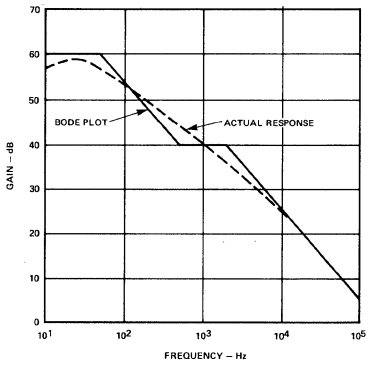
PREAMPLIFIER—RIAA/NAB COMPENSATION



*Select to provide specified transducer loading.
Output Noise ≈ 0.8mV rms (with input shorted)

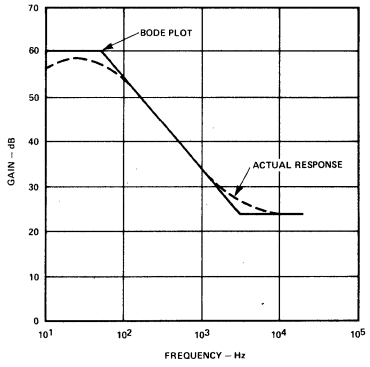
All resistor values are in ohms.

Figure 3-39a



Bode Plot of RIAA Equalization and the response realized in an actual circuit using the 531.

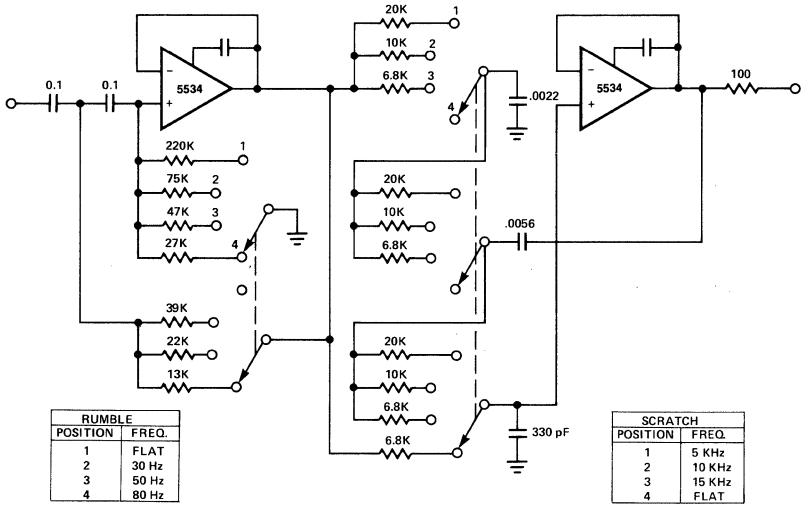
Figure 3-39b



Bode Plot of NAB Equalization and the response realized in the actual circuit using the 531.

Figure 3-39c

RUMBLE/SCRATCH FILTER



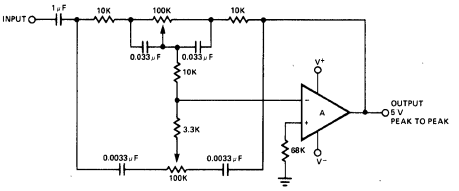
RUMBLE	
POSITION	FREQ.
1	FLAT
2	30 Hz
3	50 Hz
4	80 Hz

SCRATCH	
POSITION	FREQ.
1	5 KHz
2	10 KHz
3	15 KHz
4	FLAT

All resistor values are in ohms.

Figure 3-40

TONE CONTROL CIRCUIT FOR OPERATIONAL AMPLIFIERS



All resistor values are in ohms.

NOTES
1. Amplifier A may be a 531 or 301. Frequency compensation, as for unity gain non-inverting amplifiers, must be used.
2. Turn-over frequency—1kHz.
3. Bass boost +20dB at 20Hz, bass cut -20dB at 20Hz, treble boost +19dB at 20kHz, treble cut -19dB at 20kHz.

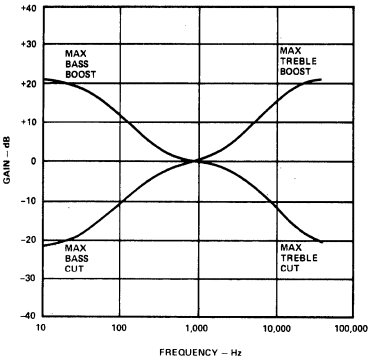
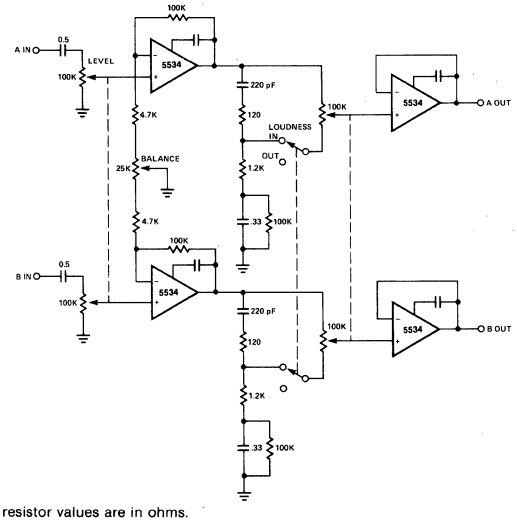


Figure 3-41

BALANCE AMPLIFIER WITH LOUDNESS CONTROL



All resistor values are in ohms.

Figure 3-42

circuit of Figure 3-41 provides 20dB of bass or treble boost or cut as set by the variable resistance. The actual response of the circuit is shown also.

BALANCE AND LOUDNESS AMPLIFIER

Figure 3-42 shows a combination of balance and loudness controls. Due to the non-linearity of the human hearing system the low frequencies must be boosted at low listening levels. Balance, level and loudness controls provide all the listening controls to produce the desired music response.

VOLTMETER

Figure 3-43 shows a high impedance voltmeter, using the 536 op amp as a non-inverting amplifier. The ranges, up to 10V full scale, have extremely high input impedance, (up to $5X10^8\Omega$), with a guard terminal available. The 30V and 100V scales have 30 and $100M\Omega$ input impedance. The input is protected against input overvoltage by the diodes, but the meter cannot be subjected to more than 50% overload.

CAPACITANCE MULTIPLIER

The circuit in Figure 3-44 can be used to simulate large capacitances using small value components. With the values shown and C = $10\mu F$, and effective capacitance of $10,000\mu F$ was obtained. The Q available is limited by the effective series resistance. So R1 should be as large as practical.

SIMULATED INDUCTOR

With a constant current exitation, the voltage dropped across an inductance increases with frequency. Thus, an active device whose output increases with frequency can be characterized as an inductance. The circuit of Figure 3-45 yields such a response with the effective inductance being equal to:

$$L = R1R2C$$

The Q of this inductance depends upon R1 being equal to R2. At the same time, however, the positive and negative feedback paths of the amplifier are equal leading to the distinct possibility of instability at high frequencies. R1 should therefore always be slightly smaller than R2 to assure stable operation.

POWER AMPLIFIER

For most applications, the available power from op amps is sufficient. There are times when more power handling capability is necessary. A simple power booster capable of driving moderate loads is offered in Figure 3-46.

The circuit as shown uses a 741 device. Other amplifiers may be substituted only if

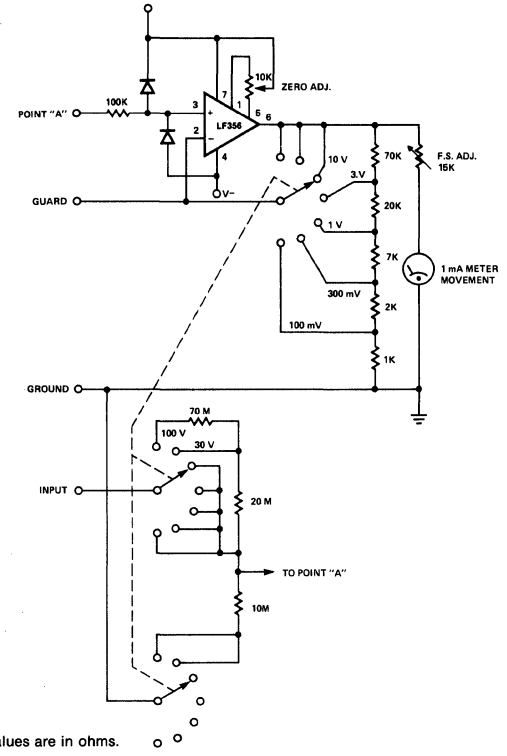


Figure 3-43

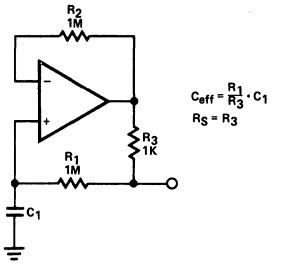


Figure 3-44

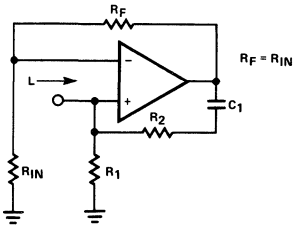


Figure 3-45

R1 values are changed because of the ICC current required by the amplifier. R1 should be calculated from the expression

$$R1 = \frac{600mV}{ICC}$$

VOLTAGE-TO-CURRENT CONVERTERS

A simple voltage-to-current converter is shown in Figure 3-47 The current out is $I_{out} \simeq V_{in}/R$. For negative currents, a pnp can be used and for better accuracy, a Darlington pair can be substituted for the transistor. With careful design, this circuit can be used to control currents of many amps. Unity gain compensation is necessary.

The circuit in Figure 3-48 has a different input and will produce either polarity of output current. The main disadvantages are the error current flowing in R2, and the limited current available.

ACTIVE CLAMP LIMITING AMPLIFIER

The modified inverting amplifier in Figure 3-49 uses an active clamp to limit the output swing with precision. Allowance must be made for the Vbe of the transistors. The swing is limited by the base-emitter breakdown of the transistors. A simple circuit uses two back-to-back zener diodes across the feedback resistor, but tends to give less precise limiting and cannot be easily controlled.

ABSOLUTE VALUE AMPLIFIER

The circuit in Figure 3-50 generates a positive output voltage for either polarity of input. For positive signals, it acts as an non-inverting amplifier and for negative signals, as an inverting amplifier. The accuracy is poor for input voltages under 1V, but for less stringent applications, it can be effective.

HALF WAVE RECTIFIER

Figure 3-51 provides a circuit for accurate half wave rectification of the incoming signal. For positive signals, the gain is 0, for negative signals, the gain is -1. By reversing both diodes, the polarity can be inverted. This circuit provides an accurate output, but the output impedance differs for the two input polarities and buffering may be needed. The output must slew through two diode drops when the input polarity reverses. This limits the accuracy for 741 type devices above 300Hz. The 535 device will work up to 10kHz with less than 5% distortion.

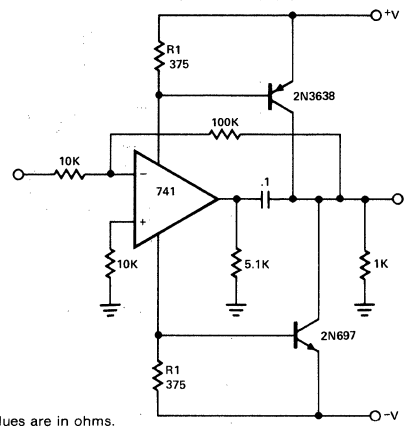
PRECISION FULL WAVE RECTIFIER

The circuit in Figure 3-52 provides accurate full wave rectification. The output impedance is low for both input polarities, and the errors are small at all signal levels. Note that the output will not sink heavy currents, except a small amount through the 10kΩ resistors. Therefore, the load applied should be referenced to ground or a negative voltage. Reversal of all diode polarities will reverse the polarity of the output. Since the outputs of the amplifiers must slew through two diode drops when the input polarity changes, 741 type devices give 5% distortion at about 300Hz. The 535 device will give under 5% distortion up to 10kHz in this circuit.

CYCLIC A TO D CONVERTER

One interesting, but, much ignored A/D converter is the cyclic converter. This consists of a chain of identical stages, each of which senses the polarity of the input. The stage then subtracts V_{ref} from the input and doubles the remainder if the polarity

POWER BOOSTER



All resistor values are in ohms.

Figure 3-46

VOLTAGE TO CURRENT CONVERTERS

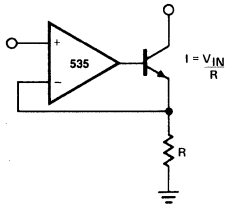


Figure 3-47

VOLTAGE TO CURRENT CONVERTER

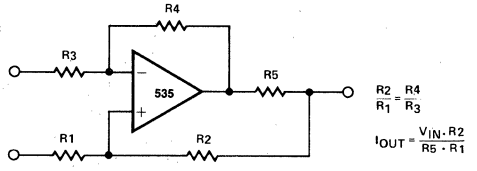


Figure 3-48

ACTIVE CLAMP LIMITING AMPLIFIER

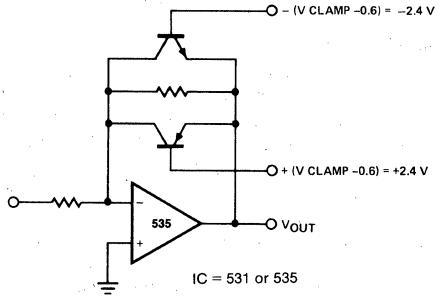


Figure 3-49

was correct. In Figure 3-53 the signal is full wave rectified and the remainder of $V_{in} - V_{ref}$ is doubled. A chain of these stages gives the gray code equivalent of the input voltage in digitized form related to the magnitude of V_{ref}. Possessing high potential accuracy, the circuit using 531 devices settles in 5μs.

LOGARITHMIC AMPLIFIER

Converting an input voltage to its log equivalent is very useful in computational circuits since two inputs can be multiplied simply by adding their logarithms. The log transfer curve of a V_{BE} junction is used in Figure 3-54 to achieve the transfer function. The 15.7kohm resistor and 1kohm thermistor provide a temperature compensated scale factor of 1 volt per decade of input voltage. Low input current devices such as the LF356 should be used for best results.

TRIANGLE AND SQUARE WAVE GENERATOR

The circuit in Figure 3-55 will generate precision triangle and square waves. The output amplitude of the square wave is set by the output swing of the op amp A - 1 and R1/R2 sets the triangle amplitude. The frequency of oscillation in either case is

$$f = \frac{1}{4RC} \cdot \frac{R2}{R1}$$

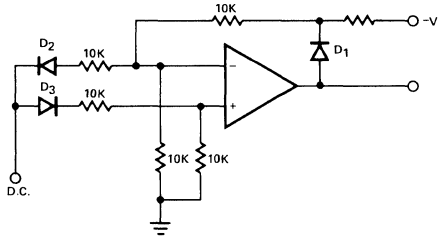
The square wave will maintain 50% duty cycle even if the amplitude of the oscillation is not symmetrical.

The use of the 531 in this circuit will allow good square waves to be generated to quite high frequencies. Since the amplifier A1 runs open loop, there is no need for compensation. The triangle-generating amplifier must be compensated. The 5558 device can be used as well, except for the lower frequency response.

TWO-PHASE SINE WAVE OSCILLATOR

This circuit uses a 2-pole pass Butterworth filter, followed by a phase shifting single pole stage, fed back through a voltage limiter to achieve sine and cosine outputs. The values shown using 741 amplifiers give about 1.5% distortion at the sine output and about 3% distortion at the cosine output. By careful trimming of C_G and/or the limiting network, better distortion figures are possible. The component values shown give a frequency of oscillation of about 2kHz. The values can be readily selected for other frequencies. The 531 should be used at higher frequencies to reduce distortion due to slew limiting.

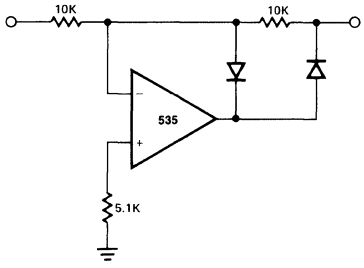
ABSOLUTE VALUE AMPLIFIER



All resistor values are in ohms.

Figure 3-50

HALF WAVE RECTIFIER



All resistor values are in ohms.

Figure 3-51

PRECISION FULL WAVE RECTIFIER

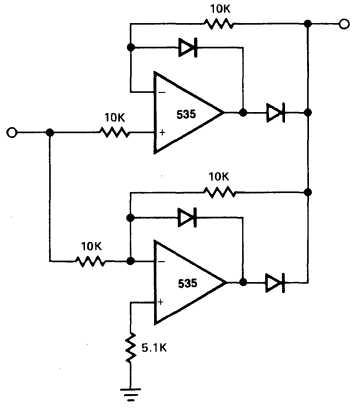


Figure 3-52

FAST SAMPLE AND HOLD CIRCUIT

This circuit, (referring to Figure 3-57), depends upon the high slew rate of the 531. The operation begins as a strobe pulse developed from a logic input at IC2 turns on jFET Q1. This completes the feedback loop to IC1 and Q1 and Q2. This forces the capacitor C1 to charge to a voltage equal to the input voltage plus the gate to source offest voltage of the MOS transistor Q2. At the end of the strobe time, the loop is broken and this voltage is held by capacitor C1 until the time of the next strobe pulse. Using the MOSFET in this way minimizes greatly any drift or offset and results in a tracking accuracy of better than .01%. The 536 could be used as a buffer amplifier instead, with some loss of speed.

With the components shown, a 15μs strobe pulse was used and the decay of the output voltage between samplings was measured at less than 1mV per second.

VOLTAGE COMPARATOR

Inexpensive voltage comparators with only modest parameters are often needed. The op amp is often used in this configuration because the high gain provides good selectivity. Figure 3-58 shows a circuit usable with most any op amp. The zener is selected for the output voltage required (5.1 volt for TTL), and the resistor provides some current protection to the op amp output structure. V_{ref} can be any voltage within the wide common mode range of the amplifier—another advantage of using op amps for comparators. If the LM101A devices is used as depicted by Figure 3-59 the clamp diode may be connected to the compensation point directly. Clamping the voltage at this point does not require a series resistor because of the internal circuitry of the LM101A.

VOLTAGE AND CURRENT OFFSET ADJUSTMENTS

Many IC amplifiers include the necessary pin connections to provide external offset adjustments. Many times however, it becomes necessary to select a device not possessing external adjustments. Figures 3-60, 3-61, and 3-62 suggest some possible arrangements for offset voltage adjust and bias current nulling circuitry. The circuitry of Figure 3-62 provides sufficient current into the input to cancel the bias current requirement. Although more simplified arrangements are possible the addition of Q2 and Q3 provide a fixed current level to Q1, thus, bias cancellation can be provided without regard to input voltage level.

CYCLIC A TO D CONVERTER

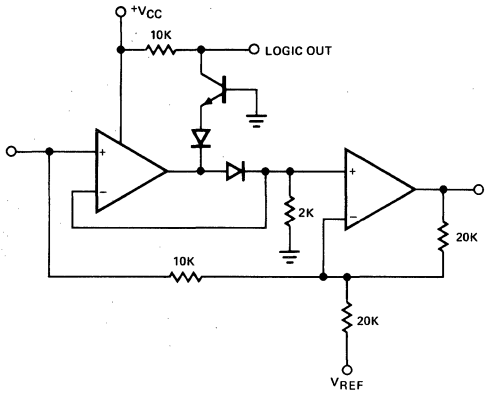


Figure 3-53a

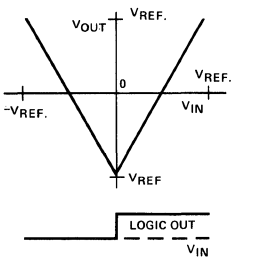
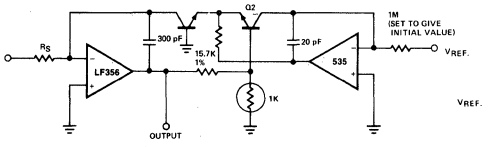


Figure 3-53b

LOGARITHMIC AMPLIFIER



All resistor values are in ohms.

Figure 3-54

TRIANGLE AND SQUARE WAVE GENERATOR

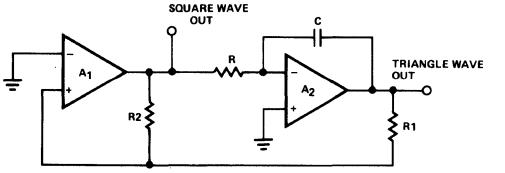
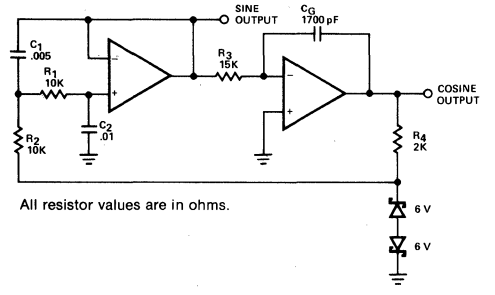


Figure 3-55

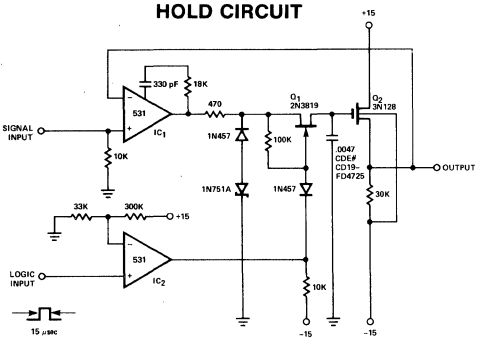
TWO-PHASE SINE WAVE OSCILLATOR



All resistor values are in ohms.

Figure 3-56

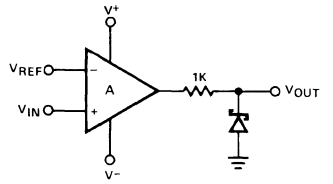
FAST SAMPLE AND HOLD CIRCUIT



All resistor values are in ohms.

Figure 3-57

VOLTAGE COMPARATOR



All resistor values are in ohms.

Figure 3-58

VOLTAGE COMPARATOR

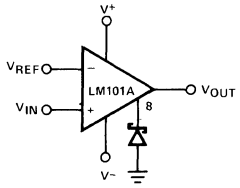
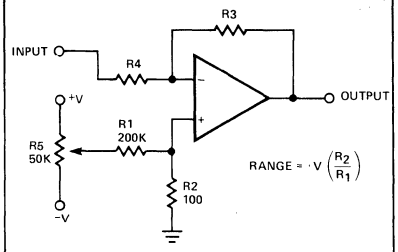


Figure 3-59

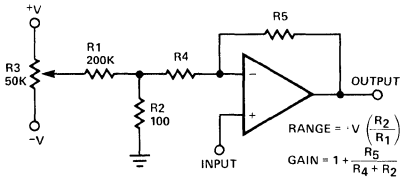
UNIVERSAL OFFSET NULL FOR INVERTING AMPLIFIERS



All resistor values are in ohms.

Figure 3-60

UNIVERSAL OFFSET NULL FOR NONINVERTING AMPLIFIERS



All resistor values are in ohms.

Figure 3-61

BIAS CURRENT COMPENSATION

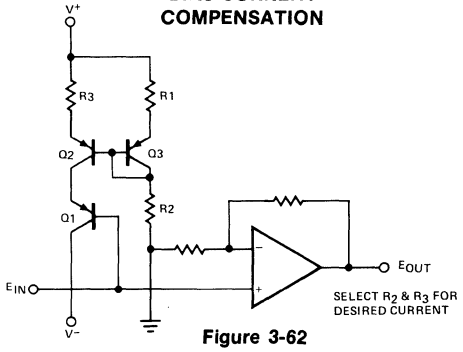


Figure 3-62

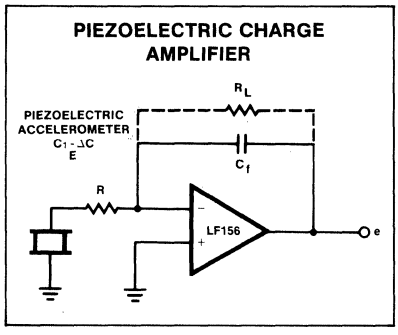
THE LF 156, IMPROVED FET OP AMP

Introduction

Advanced analog processing at Signetics has led to the improved jFET input op amp. The LF156 incorporates well-matched, high-voltage jFET's on the same chip with bipolar transistors. The design gives low voltage and current noise and a low I/f noise corner. Specific applications which can utilize the advanced characteristics of the LF156 follow:

Applications

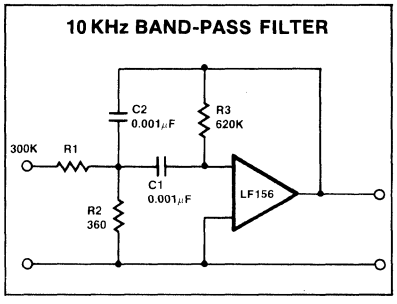
A change in capacitance must cause a change in charge, and that charge is displaced into the summing point, which must be balanced by an equivalent displacement of charge across the feedback capacitor, C_f, caused in turn by a change in the output voltage e. This circuit has the desirable property of being virtually independent of shunt capacitance across the

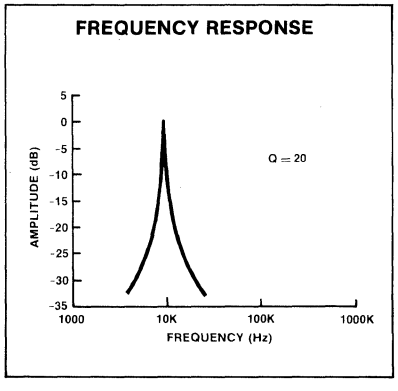


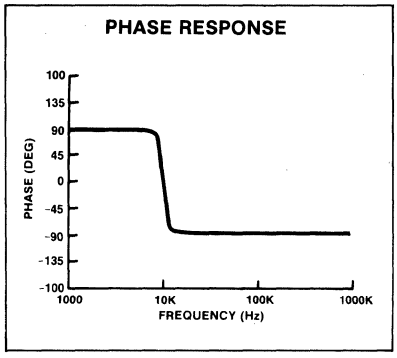
input, since such capacitance is connected from the summing point to ground, and has across it only the residual null voltage, which should be negligibly low. This independence of input capacitance permits the use of long shielded cables between the transducer and the amp, without significantly affecting accuracy. Leakage resistance in parallel with C_f must be deliberately sustained, in order to prevent the amplifier output from drifting to saturation. The sensitivity is inversely proportional to the value of C_f.

The smallest value of C_f that will be large compared to "strays" will yield the highest predictable sensitivity. At the lowest frequency, Xc must be small compared to R_L and the op amp's offset current is sufficiently small to prevent saturation with the required value of R.

Another application for which the LF156 is well suited is the high frequency, high impedance active filter. An example follows:





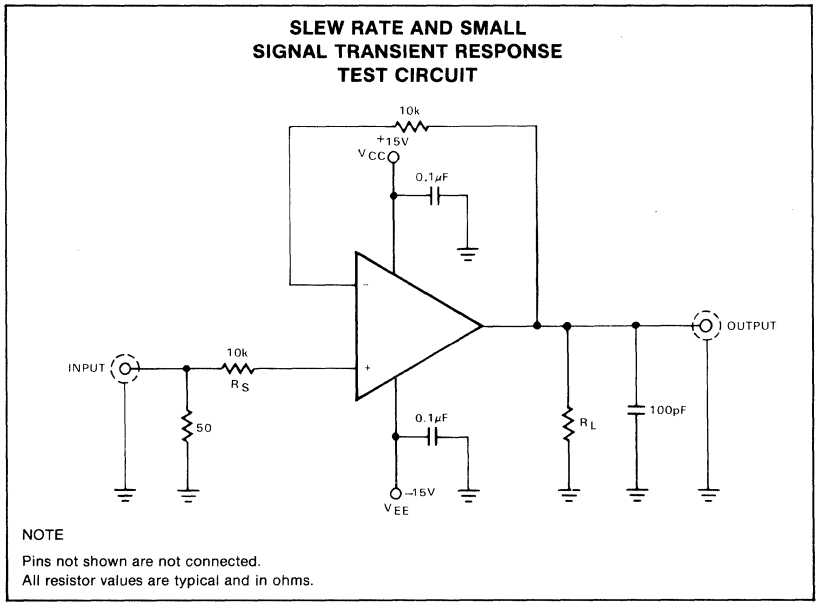


Other applications for the LF156 include: high impedance buffers, wideband low noise low drift amplifiers, precision high speed integrators, sample and hold circuits and fast D/A and A/D converters.

SE/NE535, OP AMP APPLICATIONS

Introduction

The 535 is a new generation monolithic op amp which features improved input characteristics. The device is compensated to unity gain and has a minimum guaranteed unity gain slew rate of 10V/μs. This is achieved by employing a clamped super beta input stage which has lower input bias current.



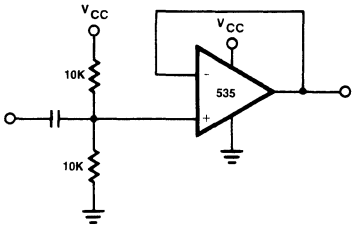
Applications

These improved parameters can be put to good use in applications such as sample and hold circuits which require low input current and in voltage follower circuits which require high slew rates. The circuit that follows will yield maximum small signal transient response and slew rate for the 535 at unity gain.

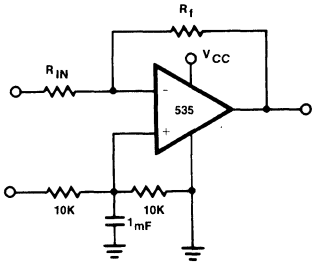
It is always good practice in designing a system to use dual tracking regulators such as the Signetics 5554 to power the dual supply op amps. This will guarantee the positive and negative supply voltage will be equal during power up. With the 535, it is possible to degrade the input circuit characteristics by not applying the power supplies simultaneously. The 535 is capable of directly replacing the 741 with higher input resistance which will improve such designed as active filters, sample and hold, as well as voltage followers.

The SE/NE535 can be used either with single or split power supplies.

VOLTAGE FOLLOWER WITH SINGLE POWER SOURCE



INVERTING AMP WITH SINGLE POWER SUPPLY



SE/NE538 APP. NOTE

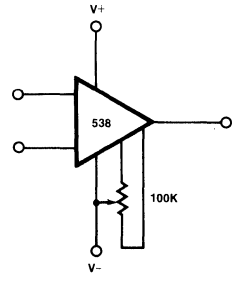
Introduction

The Signetics SE/NE538 is the undercompensated version of the SE/NE535. The 538 has a typical slew rate of 50V/μs and a gain bandwidth product of 6MHz.

The internal frequency compensation is designed for a minimum inverting gain of 4 and a minimum non-inverting gain of 5. Below these gains the 538 will be unstable and the 535 should be used.

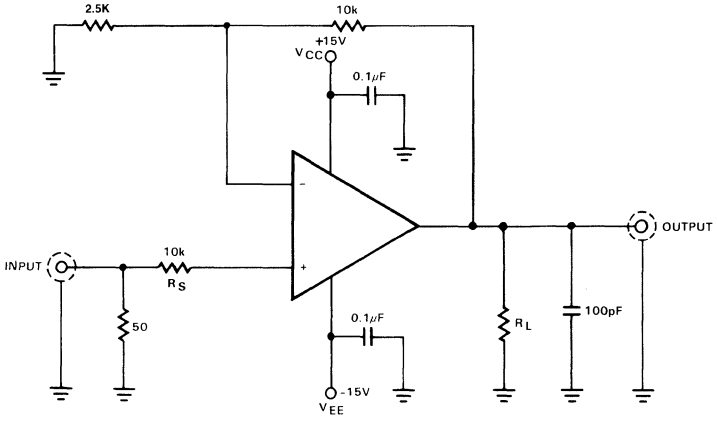
The higher slew rate of the 538 has made this device quite appealing for high speed designs and the fact that it has a standard pinout will allow it to be used to upgrade existing sytems that now use the μA741 or μA748.

OFFSET ADJUST CIRCUIT



Applications

SLEW RATE AND SMALL SIGNAL TRANSIENT RESPONSE TEST CIRCUIT



NOTE:
Pins not shown are not connected.
All resistor values are typical and in ohms.

SECTION 21
VOLTAGE REGULATORS

INTRODUCTION

The wide use of integrated circuits in systems has frequently led to the power supply and regulator portions taking a disproportionate share of the volume of the system. The introduction of flexible, high performance regulator ICs such as the 550 has made it possible for a designer to produce a highly regulated power supply in a small space with greatly reduced design effort.

The objective of a voltage regulator is to provide a constant output voltage independent of input supply voltage, output load current, and temperature. In general, it is desirable that the regulator should limit its own dissipation and its output current so that fault conditions and overload will not damage the regulator or the load.

Supply regulators contain four basic elements: a reference source, an error detector, a control device, and protection circuitry. For the devices discussed here, the reference source is a constant voltage, the control device is a pass transistor, and the protection is primarily by current limiting.

Because the application of voltage regulators depends a great deal upon the internal workings of the integrated circuit, a brief discussion of the design is included before actual applications are presented.

A schematic of the 550 is present in Figure 4-1. For the sake of brevity this discussion will deal with the 550 but in most cases will apply also to the μA723 device.

THE REFERENCE SOURCE

The 550 reference voltage is developed across the zener diode D2. The voltage is temperature compensated by the base-emitter drops in Q4, Q5 and Q6, in combination with the resistance divider R2—R6. The voltage appearing at the emitter of Q5 has a temperature coefficient of approximately +7mV/°C while that at the base of Q6 is approximately -2.3mV/°C. Thus, by choosing the appropriate tap on the resistor R2—R6, it is possible to obtain a zero temperature coeffient. Naturally, the actual value of the temperature coefficient will fluctuate from unit to unit, but accurate compensation is easier to achieve here than with other methods. The effective impedance at this point is predominantly the parallel impedance of R2 and R6, increased by the diode impedances, and is typically 2k ohms.

The reference circuit as it stands is not self starting, necessitating the addition of FET Q1, D1, D4, and D5. When there is no current in D2, Q1 will feed current through D4 and D5 into the base of Q4, thus starting the current sources. When these are operating, D1 drops approximately the same voltage as D2, so D5 has no voltage across it and it no longer affects the reference circuit. The current through Q1 drives the base of Q17, with D1 and D4 providing the correct bias point for the proper operation of Q4 and Q5.

ERROR AMPLIFIER

The error amplifier in the 550 is a differential amplifier composed of Q11 and Q12, with biasing provided by Q7, Q8, Q9, Q10 and Q13. Q7 and Q8 act as equal current sources, driven by Q2, with R4 and R5 improving the balance and output impedance characteristics. The current from Q7 is inverted in Q10 and Q13. Q13 has twice the area of Q10, so the current sink Q13 is twice the value of the source Q7 and Q8. Q9 eliminnates the error term caused by the basic currents of Q12 and Q13. Thus, the sum of the emitter currents of Q4 and Q12 is twice the current in source Q8. In balance, the current flow into the base of Q14 can be neglected, so the collector current of Q12 is equal to the current from Q8. Ignoring the base current of Q12, the emitter current of Q12 is half the collector current of Q13, so Q11 must carry the remainder. Hence, the currents in Q11 and Q12 are equally matched at balance, or no error condition. An unbalanced condition where the base of

550 REGULATOR SCHEMATIC

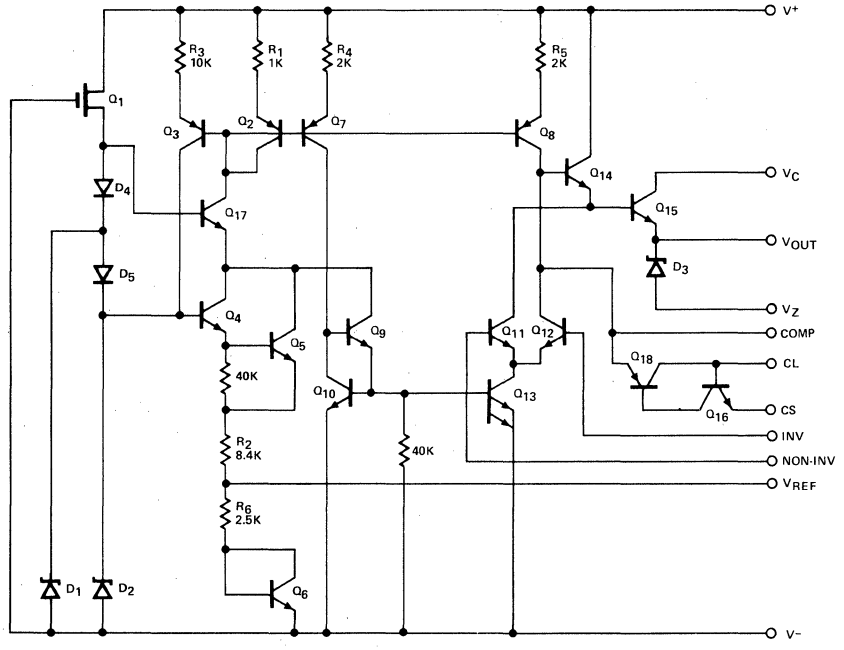


Figure 4-1

BASIC REGULATOR CONFIGURATION

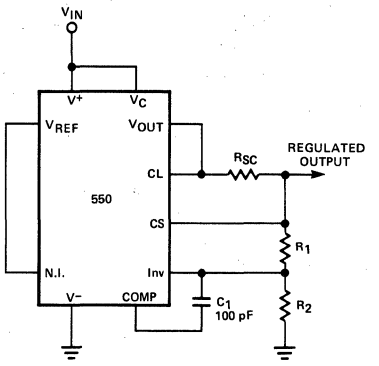


Figure 4-2a

CURRENT LIMITING CURVES

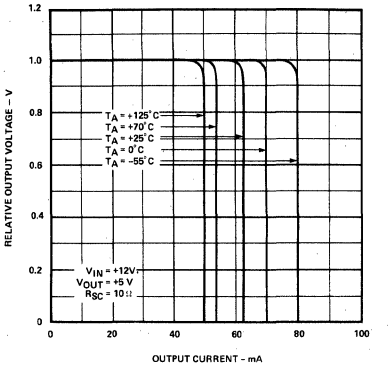


Figure 4-2b

Q11 is more positive (negative) than that of Q12 will lead to an increase (decrease) of current in Q11, a decrease (increase) of current in Q12, and a rise (fall) of the voltage at the base of Q14 and Q15. Thus, a positive voltage change on the base of Q11 will lead to a higher current from V_{OUT}, the emitter of Q15. The effect of voltage changes on the base of Q12 is, of course, the opposite. The voltage gain of the error amplifier is given by

(Equation 4-1)

$$AV \cong \frac{RC}{2r_e} = \frac{R_{C12}/\,/R_{C8}}{2kT/qI_E}$$

This is typically 5000 at room temperature, rising a little at low temperature, and falling slightly at high temperature. High frequency stability is ensured by connecting a capacitor from the compensation pin to the inverting input, giving the amplifier a 6dB/octave roll off. In this manner, external pass elements with arbitrary phase characteristics at high frequency can still be compensated for by rolling off the amplifier.

The error voltage is derived by resistor division of the output voltage. Since the error amplifier inputs will seek a balance between them, the output voltage will attain a value equal to the reference voltage multiplied by the amplifier gain.

The collector voltage of Q12 is set by the nearly constant output voltage. Power supply rejection of the amplifier may be improved by taking the collector of Q11 to the constant voltage of Q14 also.

The availability of both the inverting and non-inverting inputs to the error amplifier allows the regulator to be used in a wide variety of applications.

In some applications where the output is fed back to the non-inverting input, a non-destructive latch-up can occur in Q11. By feeding current into the compensation pin through a diode this phenomenon can be avoided. Those applications requiring the additional diode are shown with the necessary connections.

CONTROL DEVICE

The control element is formed by the pass transistor Darlington pair Q14—Q15. The ultimate current capability of this pair is very high, but the usable current is restricted by packaging and assembly limitations to about 200mA. In general, power dissipation factors lead to more severe limitations, and applications requiring currents in excess of 50mA are best handled with external pass transistors. To this end, the collector of Q15 is brought out separately, allowing an extended range of pass transistor connections to be utilized. These are discussed in the applications sections.

PROTECTION CIRCUITRY

Up to this point the design discussions have applied both to the 550 and μA723 devices. The short circuit protection sections differ slightly. Therefore, the following discussion will not necessarily apply to the μA723.

Isolating the regulator from the load during periods of overload is the function of Q16 and Q18. These two transistors are arranged to form an SCS device.

Figure 4-2 shows the basic positive voltage regulator configuration. The sense resistor RSC is connected between emitter and base of Q16. When load current increases to such a value as to turn on Q16 the SCS device turns on removing the 120μA base drive provided by Q8 to Q14, thus isolating the load.

After the SCS turns on, Q16 need only provide the small base current required by Q18 to sustain current limiting. The current at which current limiting occurs is given by:

(Equation 4-2)

$$I_{SC} = \frac{V_{sense}}{RSC}$$

where Isc is the short circuit current and V_{sense} is the V_{BE} of Q16.

Since the V_{BE} of Q16 falls with increasing temperature the short circuit also falls, a desirable trait.

The advantage of incorporating the SCS device for current limiting lies in foldback limiting the output. That is, the output current under overload conditions drops to a value far below the peak load current capability. This is essential in high current regulators to protect the regulator from excessive power dissipation. The technique of foldback limiting and the resultant locus are illustrated by Figure 4-3. In normal operation of the circuit no current is sourced, but when shut down, a current

(Equation 4-3)

$$I_{CL} \cong I_{Q8} \bullet h_{FEL} / (1+h_{FEL})$$

is sourced. Bypassing this current through a resistor R_{FB} as in Figure 4-3, a portion, ($I_{CL}R_{FB}$), of the V_{sense} shutdown voltage can be generated regardless of current in R_{SC}, once the device is shut down.

Thus, when Q16 — Q18 are conducting the major portion of IQ8, the shutdown condi-

FOLD BACK CURRENT LIMITING

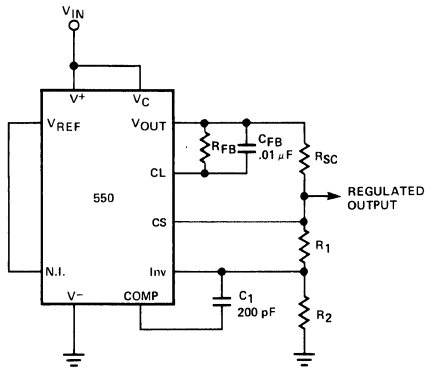


Figure 4-3a

FOLDBACK CURRENT LIMITED OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

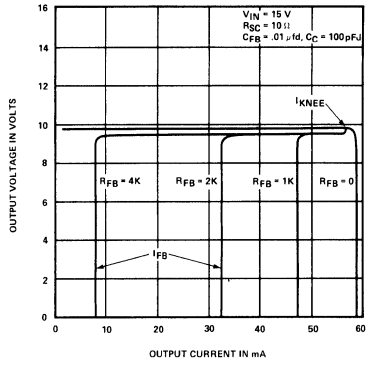


Figure 4-3b

tion changes from equation 4-3 to, (ignoring small terms),

(Equation 4-4)

$$I_{SC}R_{SC} + I_{CL} \bullet R_{FB} = V_{sense}$$

Thus, the actual short circuit current can be much less than the peak load current given by equation 4-2. The load current-voltage characteristics of Figure 4-3 are shown in the curve for various values of R_{FB}.

Since the input impedance of the C_L terminal is negative over some range of voltages, it is normally necessary to by-pass R_{FB} with a capacitor to maintain stability if operation in this range is desired. A value of 0.01μF is generally satisfactory.

By increasing R_{FB} to such a value that $R_{FB} \bullet I_{CL} > V_{sense}$, the circuit will shut down completely under overload, and not come back into operation unless the voltage between the C_L and C_S terminals is reduced below V_{sense} by some external means. In general, this is most useful in remote shutdown applications discussed later.

The final feature available in the dual in-line package versions of the 550 and the μA723 is the zener diode D3 between V_{OUT} and V_Z, (the V_Z output is not available in the L package since there are insufficient pins). This diode is useful in certain applications such as negative regulators, where it is desirable for the output of the amplifier to be level shifted to a point more negative that V_{out} is permitted to go (+2V referred to V-). The Zener voltage is typically 6.4V. The use of this feature is discussed in the next section.

APPLICATIONS

Designing basic voltage regulators with high performance IC regulators is relatively straightforward. Each functional block of the regulator should be considered as to its contribution to the system. Basic regulation of an output voltage is achieved by multiplying a reference voltage by the gain of an amplifier. Thus, the error amplifier may be treated as an operational amplifier where the 'virtual ground' and 'zero differential voltage' statements developed in section three apply. The reference voltage is applied to the positive input and a sample of the output voltage is fed back to the negative input via a resistor divider network. Since the junction of R1 and R2 in Figure 4-3 will equal the reference voltage (zero differential rule), the output will be set by the ratio of the resistors. Specifically the output voltage becomes:

(Equation 4-5)

$$V_{OUT} = V_{REF}\frac{R1 + R2}{R2}$$

Each input to the error amplifier requires a small bias current of typically 1μA. Since these currents will be flowing through the input impedances to the amplifier it is possible to generate an error voltage if the impedances to the amplifier are not equal. In addition temperature changes will cause fluctuations in bias current causing the output voltage to drift. Thus, the final design should provide a match of the input impedances both to improve accuracy and temperature stability of the output voltage. The effective impedance of the internal reference voltage of the 550 is 2kohm. Therefore for best temperature stability the parallel combination of R1 and R2 should be 2kohm.

(Equation 4-6)

$$R_S = 2k = \frac{R1 \bullet R2}{R1 + R2}$$

The design of the regulator should satisfy both equation 4-5 and equation 4-6 simultaneously. Solving both leads to equations 4-7 and 4-8 which express the resistor values as a function of output voltage.

(Equation 4-7)

$$R2 = \frac{2000V_{OUT}}{V_{OUT}\text{-}V_{REF}} \text{ OHMS}$$

(Equation 4-8)

$$R1 = \frac{2000V_{OUT}}{V_{REF}} \text{ OHMS}$$

Having determined the required resistor values, the designer may find that they are not readily available in standard values and some adjustments are necessary. Such changes should maintain the ratio:

(Equation 4-9)

$$\frac{V_{OUT}}{V_{IN}} = \frac{R1 + R2}{R2}$$

The reference voltage of the 550 is 1.63 volts typically, with a spread of 1.53 volts minimum to 1.73 volts maximum. This variation from unit to unit may require that some portion of R1 or R2 be made adjustable for exact output voltage trimming.

PASS TRANSISTOR CIRCUITS

The next major subject concerns the use of external pass transistor options. These can readily extend the usable output current range of the regulator to many amps and reduce power dissipation in the IC as well. In this way, thermal effects, (discussed later in detail), are minimized.

The simplest circuit is that shown in Figure 4-4. Here, the internal Darlington pass transistor configuration is extended to a triplet by the external npn transistor. For further extension, this external device can be a Darlington, extending the string to a quad.

USE OF EXTERNAL NPN PASS TRANSISTOR

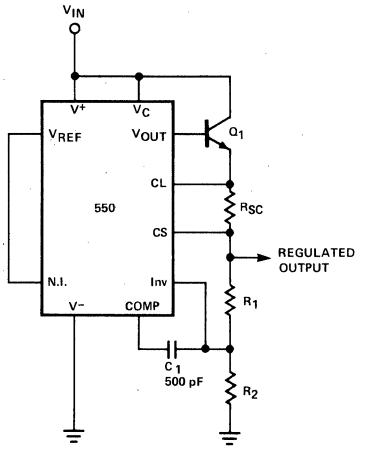
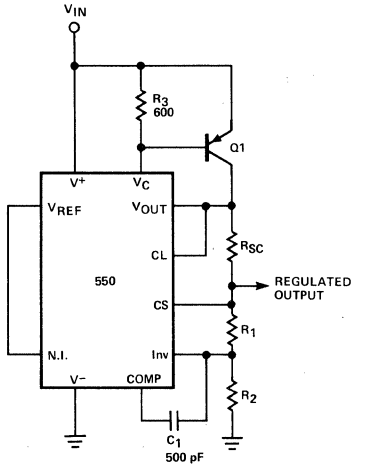


Figure 4-4

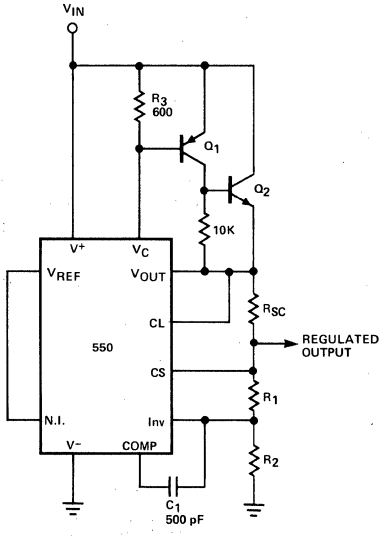
USE OF PNP PASS TRANSISTOR



ALL RESISTOR VALUES ARE IN OHMS

Figure 4-5

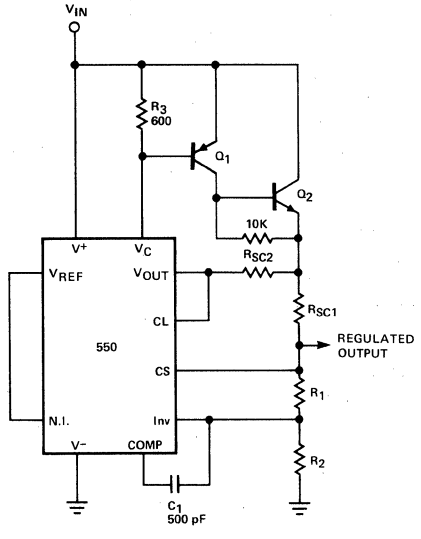
USE OF PNP-NPN PASS TRANSISTOR



ALL RESISTOR VALUES ARE IN OHMS

Figure 4-6

OVERLOAD PROTECTION OF THE INTEGRATED CIRCUIT AND THE PASS TRANSISTORS



All resistor values are in ohms

Figure 4-7

This arrangement has the merit of economy, since npn power transistors are generally cheaper than pnp, but has the disadvantage that the minimum differential voltage between input and output is increased by the V_{BE}s of the external transistors. The load regulation is also somewhat degraded since the error amplifier gain is finite and the V_{BE} drops of the external transistors is a function of load current.

An alternative circuit avoiding the disadvantages mentioned above is shown in Figure 4-5. This circuit uses the pnp transistor whose base drive is obtained from the V_C terminal.

The resistor R3 is used to ensure Q1 turns off under no load conditions, avoiding the excessive buildup of leakage current that can sometimes occur at high temperature. The effect of Q1 is to multiply the h_{FE} of the output transistor in the IC, without increasing the V_{BE}, hence this circuit optimizes the load regulation also. Once again, this device

can be replaced by a Darlington pair, but the V_{BE} buildup begins to affect the differential voltage limit. The best arrangement is that shown in Figure 4-6. The npn pass transistor is driven from a pnp device to enhance beta. Thus, large output currents are gained without sacrificing minimum input to output voltage differential.

The short circuit and overload protection techniques discussed later can all be applied to these pass transistor circuits. The currents can be scaled by altering the value of R_{SC}.

This will protect the entire regulator against overload but will not protect the IC from pass transistor failure. The limit is set at several amperes — enough to destroy the IC — should the transistor fail. Protection from such failure can be provided by the circuit of Figure 4-7.

R_{SC1} performs the main short circuit protection, but R_{SC2} limits the IC output current to a safe value if the pass transistors fail. The normal voltage drop in R_{SC2} should be small compared with the voltage drop in R_{SC1}. This circuit may be modified to include all the protection techniques discussed next.

OVERLOAD PROTECTION

The simple short circuit protection arrangement of Figure 4-2A gives the typical output characteristic illustrated in 4-2B. This shows the variation of limit current with temperature and the sharp knee between the constant voltage and constant current regions. Adequate for most applications, this method has the benefit of simplicity. The value of the short circuit resistor R_{SC} is given by:

(Equation 4-10)

$$I_{SC} \simeq \frac{V_{sense}}{R_{SC}}$$

Many variations of the basic circuit exist. Since the regulator is shut down when the voltage difference between C_L and C_S reaches V_{sense}, a set of resistors to achieve limiting or a locus other than that given by equation 4-10 can be chosen. For instance, it might be beneficial to limit one supply to a lower current level than another.

The arrangement of Figure 4-8 produces a limit relationship

(Equation 4-11)

$$I_{L1}R_{SC1} + I_{L2}(R_{SC1} + R_{SC2}) < V_{sense}$$

This allows a higher limit on output 1 [V_{sense}/R_{SC1} if $I_{L2}=0$] than on output 2 [$V_{sense}/R_{SC1} + R_{SC2}$) if $I_{L1} = 0$], but protects both outputs to less than these limits if the other is carrying current. The price paid is that only one output can be well regulated. The other output has an effective output impedance derived from the R_{SC}'s. If output 1 is stabilized (by tying R1 to it), then the output impedance of output 2 will be R_{SC2} higher; if output 2 is stabilized, then output 1 has a low output impedance, but a high mutual impedance from the load current I_{L2}.

In general, any linear combination of load currents and input or output voltages can be used to set the overload operating conditions. In extreme cases the use of an op-amp summing amplifier to drive C_L or C_S could be considered. However, the simple limit scheme depicted in Figures 4-2 and 4-3 is adequate to cover most cases.

FOLD BACK CURRENT LIMITING

The primary limitation on the use of the simple protection of Figure 4-2 arises from the power dissipation under short circuit conditions. The power dissipation allowed depends on the package type. For simplicity, we will discuss the L package (10 lead T05) values, but the other package limits can be substituted readily. At ambient temperatures below 30°C, this limit is 800mW, giving a junction-to-ambient temperature difference in the neighborhood of 120°C. Above this temperature, derating at 6.8mW/°C, we find at an ambient of 50°C, 680mW, at 75°C, 510mW, at 100°C, 300mW, and at 125°C, 170mW.

Clearly, under short circuit output conditions, the dissipation becomes the product of the full input voltage and the short circuit current. Consider a device with $20V_{IN}$, $15V_{OUT}$, and 60mA current limit, operating at ambient temperature of $T_A = 25°C$. The standby current will be assumed to be 2mA or a dissipation of 40mW. The pass transistor dissipation just before overload is 5V at 60mA, or 300mW, for a total of 340mW, well within ratings. But under short circuit conditions, the initial pass transistor dissipation is 20V at 60mA, or 1.2W (a total of 1.24W), in excess of the allowed ratings. If the 340mW

MODIFIED SHORT CIRCUIT PROTECTION

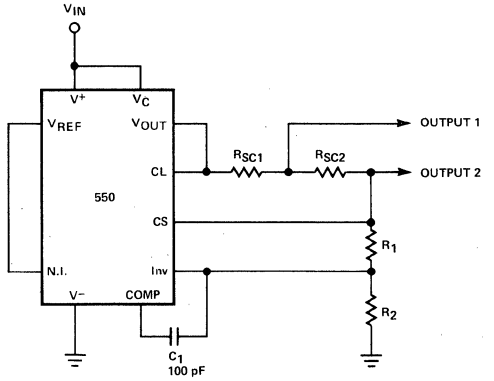
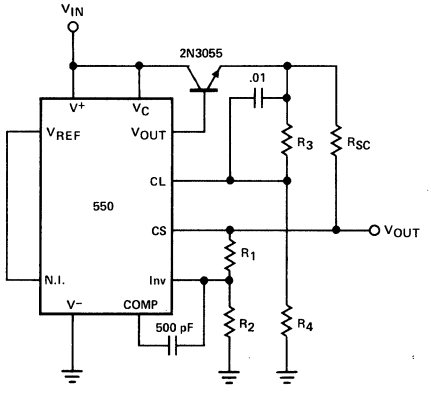


Figure 4-8

SCHEMATIC OF 10 VOLT-1 AMP REGULATOR



$$I_{KNEE} = \frac{V_{OUT}R_3 + (V_{SENSE} - I_{CL}R_3)(R_3 + R_4)}{R_4 R_{SC}}$$

$$I_{SC} = \frac{(R_3 + R_4)(V_{SENSE} - I_{CL}R_3)}{R_{SC}R_4}$$

Figure 4-9a

FOLD BACK LIMITING OF 10 VOLT-1 AMP REGULATOR

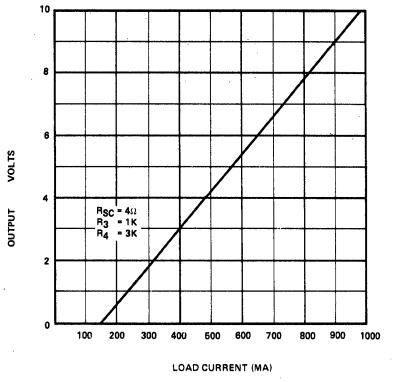


Figure 4-9b

REMOTE SHUTDOWN REGULATOR

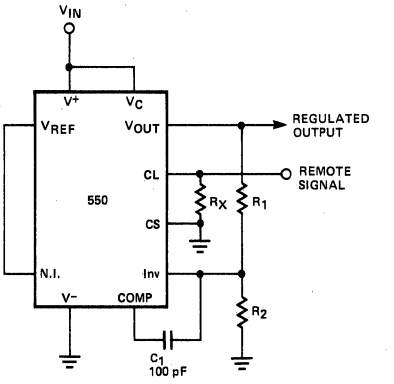


Figure 4-10

REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING

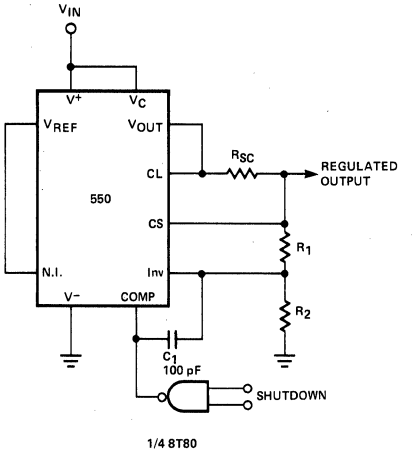


Figure 4-11

dissipation is maintained to reach equilibrium, the junction temperature will rise to about 75°C, and the short circuit current will fall to about 52mA, so the short circuit dissipation is then 1.08W, still in excess of ratings. Eventually, the junction temperature will reach 150°C, where the short circuit current will be about 37mA, and the total dissipation about 800mW, just acceptable at an ambient temperature of 25°C. High ambient temperature will degrade the situation. Taking a worst case situation, with V_{IN} = 40V, T_A = 125°C, and I standby=2.0mA, the allowable package dissipation is 170mW, of which 80mW is taken by standby current, leaving 90mW for the pass device. Thus, the short circuit current must not exceed 2.2mA. However, with V_{OUT} at 35V, the allowable output current is 18mA. The same problem arises in circuits using pass transistors, except that the dissipation is transferred to the pass transistor itself.

The solution to this problem is found in foldback current limiting circuits. The 550 device is particularly well suited to this type of circuit. The basic 550 foldback circuit is shown in Figure 4-3. The internal operation of this circuit was described earlier and will not be repeated here. The current that can be drawn without significant drop in V_{OUT} called the knee current, (I_{knee}), can be considerably greater than the short-circuited output current, in this case called the foldback current, I_{SC}. The equations controlling the currents are, for I_{knee},

(Equation 4-12)

$$I_{knee} = V_{sense}/R_{SC}$$

and for I_{SC},

(Equation 4-13)

$$I_{SC} = (V_{sense} - I_{CL}R_{FB})/R_{SC}$$
$$= (V_{sense} - R_{FB} \bullet 125\mu A)/R_{SC}$$

where I_{CL} is 125μA.

The primary disadvantage of this scheme is that for certain load lines the circuit will not start. Large capacitive loads may trigger the fold back circuit causing the regulator to prematurely shut down. Momentary overloads such as start up may have to be tolerated in this case by shorting out R_{SC} until the capacitance has charged. The advantage of this circuit is that the dissipation under all types of overload is markedly reduced and by careful design, the knee current can be set at the dissipation limit value without exceeding this limit under overload.

An alternative circuit, with advantages and disadvantages of its own, is shown in Figure 4-9. This circuit can be used with the 550 and the μA723 devices, and is basically a variant of the "linear combination of voltage and current" type.

Here, the combination is of load current and output voltage, such that

(Equation 4-14)

$$V_{sense} = \left[V_{OUT} + I_{knee} \bullet R_{SC}\right]\left[\frac{R4}{R3+R4}\right] - V_{OUT} + I_{cl}R3$$

(where $I_{cl} \approx 125\mu A$ for the 550)

Solving for I_{knee} we find

(Equation 4-15)

$$I_{knee} = \frac{(R3 + R4)(V_{sense} - I_{cl}R3) + V_{OUT}R3}{R_{SC}R4}$$

The short circuit current is less than the full load or "knee" current and is described by

(Equation 4-16)

$$I_{sc} = \frac{(R3 + R4)(V_{sense} - I_{cl}R3)}{R_{SC}R4}$$

The parallel combination of R3 and R4 form a feedback resistor so the impedance should be less than 1 kohm. Values larger than 1 kohm cause the inherent foldback characteristic of the 550 to latch back before assuming the linear load line of Figure 4-9.

Ignoring small quantities the resistor values of R3 and R4 are selected from the ratio

(Equation 4-17)

$$\frac{R4}{R3} = \frac{(V_{OUT}\, I_{sc})}{V_{sense}(I_{knee} - I_{sc})} - 1$$

A design example is included here to illustrate the design procedure.

Design Example
18 Volt Input
10 Volts Output @ 1 Amp
Foldback Current Limiting

Step 1 Compute minimum I short circuit with I_{knee} = 1 amp by

$$\frac{I_{sc}}{I_{knee}} > \frac{2V_{sense}}{V_{sense} + V_{OUT}} > \frac{1.2}{10.6} > 113mA$$

Step 2 Select I_{sc} at 150mA

Step 3 Calculate R3/R4 ratio by

$$\frac{R4}{R3} = \frac{V_{OUT}(I_{sc})}{V_{sense}(I_{knee} - I_{sc})} - 1$$

$$= \frac{(10)(150)}{.6\,(.850)} - 1 = 2.94$$

Step 4 Because R3 in parallel with R4 must be less than 1 kohm select R3 at 1k. Thus, R4 becomes 2.94K. Rounding to standard values select R3 = 1K and R4 = 3K.

Step 5 Calculate R_{sc} by

$$R_{sc} = \frac{(R3 + R4)(V_{sense} - I_{cl}R3) + V_{OUT}R3}{I_{knee}R4}$$

$$= \frac{(4)(.475) + 10}{3} = 3.96\Omega$$

Step 6 Select standard value of R_{sc} = 4 ohms

Step 7 Recalculate I_{knee} using the selected standard values.

$$I_{knee} = \frac{(R3 + R4)(V_{sense} - I_{cl}R3) + V_{OUT}R3}{R_{SC}R4}$$

$$= \frac{(4)(.475) + 10}{4.3} = .991 \text{ amp}$$

Step 8 Recalculate I_{sc} using selected values

$$I_{sc} = \frac{(R3 + R4)(V_{sense} - I_{cl}R3)}{R_{SC}R4}$$

$$= \frac{(4)(.475)}{12} = 158mA$$

Figure 4-9a illustrates the final regulator arrangement with the shut down locus given by Figure 4-9b. Excellent alignment of calculated and measured results was obtained. The foldback characteristic is of the type shown in Figure 4-9b and should be contrasted with that of Figure 4-3.

Two distinct disadvantages of this circuit are readily apparent. First, the voltage drop across R_{sc} becomes large and adds directly to the minimum differential voltage required between V_{IN} and V_{OUT}. This in turn causes excessive power consumption in the regulator since the power dissipated by the pass transistor is equal to the input-output voltage differential multiplied by the peak load current.

Secondly, since R_{sc} is larger than normal, and must handle all load current, its wattage must be increased. It should be noted that load regulation will be adversely affected as well.

With these disadvantages in mind, large peak current regulators are usually best protected by the foldback characteristic shown by Figure 4-3. This circuit is advantageous because R_{sc} is small and therefore affects load regulation to a smaller degree and the latch back characteristic instantly switches the regulator from an overload condition back into one of safe power dissipation.

REMOTE SHUTDOWN

Quite often, especially in large systems, a circuit failure or alarm may be required to remove power from the main system. Remote control of the 550 is relatively easy as shown in Figure 4-10. A current injected into R_x sufficient to develop V_{sense} across R_x will shut down the regulator.

Note that for the 550 if $I_{cl} \bullet R_x$ is greater than V_{sense} ($I_{cl} = 125\mu A$), the regulator will latch in the shut down mode until R_x is sufficiently reduced. This action can be beneficial in avoiding the requirement for an external latch should the initial remote command be removed when the supply shuts down. Use of this technique will be discussed in more detail later.

A remote control circuit which retains any of the current limiting protection schemes so far discussed and adds control via a standard TTL logic level is shown in Figure 4-11. The gate listed in the figure is a suitable open collector gate with high voltage breakdown.

Selection of any other open collector gate should be based upon a breakdown at least 2 volts higher than the maximum V_{OUT} and with output leakage well below 50μA.

Naturally, no gate inputs or other loads should be tied to the line, but any number of gates meeting the above needs in total may be used in a wired-OR configuration. Tri-state outputs may not be used. Note that if the normal V_{OUT} is high, the load capacitance may be discharged through the reverse emitter base diodes of the pass transistors and the gate. This current can be limited by a series resistor not to exceed 2 kohms. Remote shut down is especially useful to ensure turn off of multiple supplies if any one supply becomes overloaded.

A schematic showing one possible technique for doing this is shown in Figure 4-12, where the use of open collector AND gates gives a simple logic structure. The diodes are not needed for supplies not exceeding the V_{CC} logic level, and it has been assumed that each supply has a load adequate to turn on the gate input.

The string may be reset by shutting down the V_{CC} supply to the gates, which must be separate from the string of controlled supplies.

Another circuit technique giving linked shutdown of regulators is given in the Non-Basic Configurations Section, (Figures 4-17 and 4-18).

Figure 4-13 shows another use of the latch capability of the 550 regulator in a remote latching shutdown regulator. The circuit is operated by TTL gates, with separate inputs for shutdown and unlatch (or reset). In normal operation, the shutdown line is high, so the output of the shutdown gate is low, and regardless of the state of the unlatch gate, V_{OUT} is set at the normal level.

If the unlatch input is low, and the shutdown input goes low, the CL input will be pulled up by R3 (and R4 if needed), the regulator will shut down, and the current sourced from the CL terminal will latch the regulator shutdown, even after the shutdown line goes high again, while the unlatch input remains low. When the unlatch line goes high, the sourced current is taken through

REMOTE SLAVING OF MULTIPLE SUPPLIES

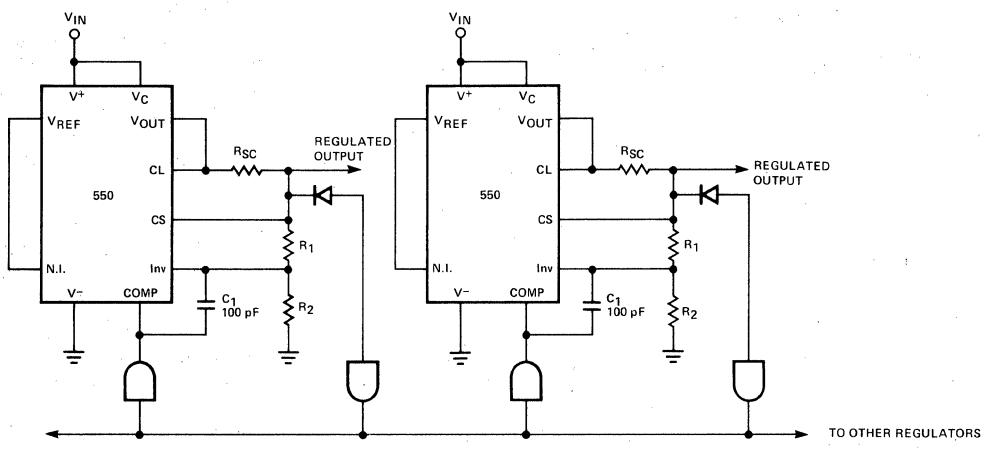
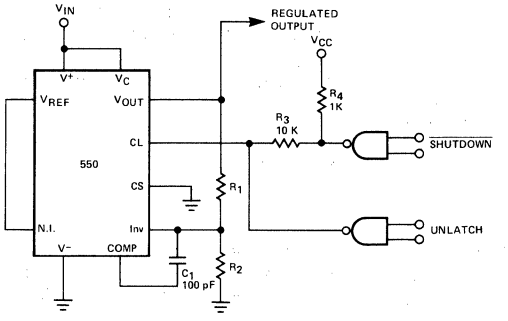


Figure 4-12

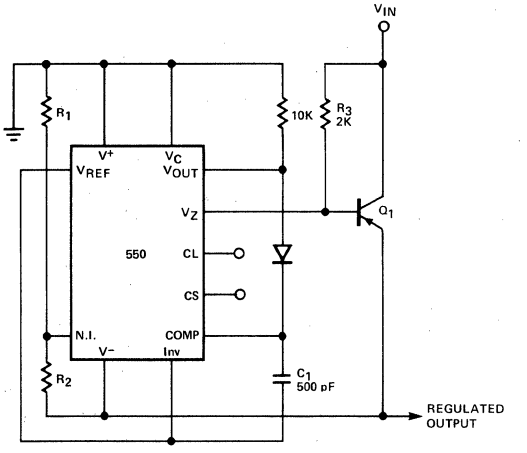
LATCHING REMOTE SHUTDOWN REGULATOR



All resistor values are in ohms

Figure 4-13

BASIC NEGATIVE REGULATOR



$$V_{OUT} = -V_{REF} \times \frac{R1 + R2}{R2}$$

$$\frac{R1 \times R2}{R1 + R2} = 2k\Omega \text{ for minimum temperature drift}$$

All resistor values are in ohms

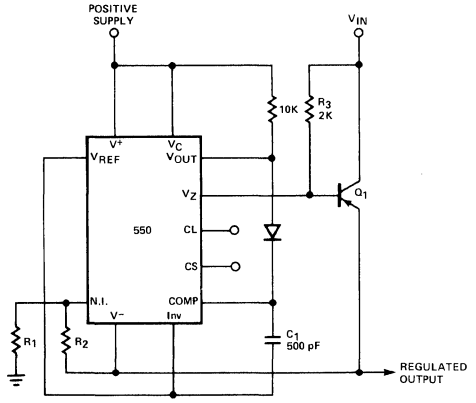
Figure 4-14

the unlatched gate, the CL terminal drops below V_{sense}, and the regulator resets. The figure lists some suitable gates, but any open collector gate can be used for the unlatch gate, and any gate at all for the shutdown gate. If an active pullup gate is used in the latter position, R4 may be omitted. Using 8T90 gates, a pulse width into the shutdown input of 50ns was found adequate to ensure latched shutdown, although the regulator output in the configuration tested did not decay fully until more than 1μs after the pulse. Since this circuit uses the internal shutdown components, additional short circuit protection would require an external transistor, connected to the compensation terminal. This basic arrangement can also be used with MOS logic driving the C_L input, although diode gating will normally be needed to ensure correct operation.

NON-BASIC CONFIGURATIONS

All the circuits discussed so far have been variations on the basic positive voltage regulator. There are many other circuit configurations that can be used, however, including negative voltage regulators, floating regulators (for voltages exceeding the maximum voltage ratings) and switching regulators for highly efficient regulation. Many of

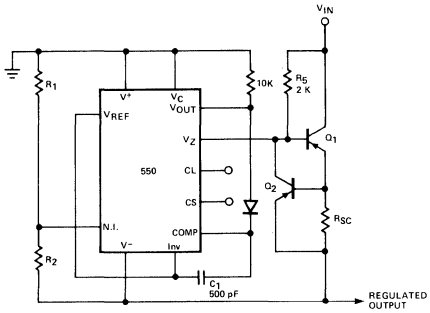
NEGATIVE REGULATOR (LESS THAN -8.5 VOLTS)



All resistor values are in ohms

Figure 4-15

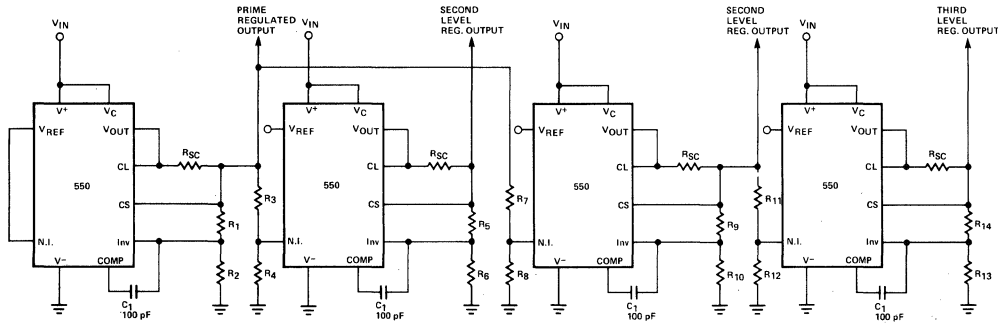
PROVIDING NEGATIVE REGULATOR OVERLOAD PROTECTION



All resistor values are in ohms

Figure 4-16

CASCADING REGULATORS



All resistor values are in ohms

Figure 4-17

the pass transistor and overload protection circuits discussed in the previous section are applicable to these configurations also.

NEGATIVE REGULATORS

The basic negative voltage regulator circuits are shown in Figure 4-14.

Note that for units not having the V_Z terminal (those in 10 pin packages) an external 6.2V Zener can be used.

The inverting and non-inverting input connections are reversed, and the pass transistor Q1 acts as a level shifted emitter follower from V_{OUT} to drive the output. The regulator is driven from its own output, so the line regulation is excellent, the load regulation is controlled by the h_{FE} of Q1 and the load regulation of the IC. R3 must be of sufficient value to drive the maximum load current through Q1 at the minimum input voltage, and large enough not to draw more than 10mA through the internal Zener (the V_Z terminal) at minimum load and maximum V_{IN}. This places a lower limit on the h_{FE} of Q1, which for large currents may need to be a Darlington pair or equivalent.

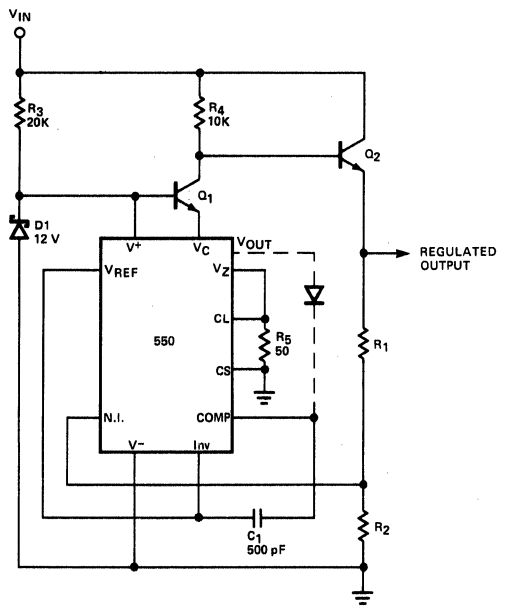
The supply voltage for the regulator is derived from the output voltage. For this reason the output voltage available is limited to values more negative than -8.5 volts.

A circuit such as in Figure 4-15 overcomes this limitation but assumes the presence of a positive supply. This is usually acceptable since the majority of negative regulator requirements arise from the need for symmetrical positive and negative voltages.

The diode and resistor frequently shown in negative regulator applications is necessary to avoid a possible forward base-collector bias on Q12 of Figure 4-1. Should forward base-collector bias occur, the regulator will latch up preventing regulation at initial power up. The diode can be a small signal type with a forward current of 100μA. Diode current flows only during initial turn on and sees approximately two volts reverse bias under normal operation. The resistor should be of sufficient value to allow approximately 100μA to flow into the V_{OUT} terminal.

Short circuit protection of negative regula-

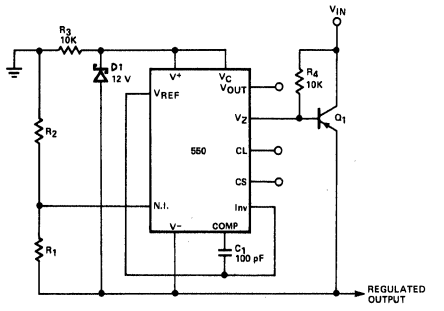
POSITIVE FLOATING REGULATOR



All resistor values are in ohms

Figure 4-18

NEGATIVE FLOATING REGULATOR



All resistor values are in ohms

Figure 4-19

BASIC SWITCHING REGULATOR

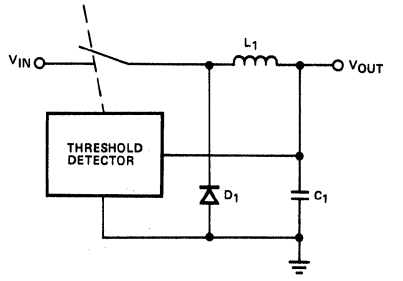


Figure 4-20

tors cannot be implemented with the circuits previously described because of the inversion of the error amplifier inputs.

Protection can be provided with the addition of a transistor as illustrated by Figure 4-16. Note that the saturation voltage of Q2 at the maximum current through R5 must be less than the V_{BE} of Q1. Other components are not critical.

FLOATING REGULATORS

So far only output voltages less than the 40 volt maximum ratings of the 550 have been covered. The maximum voltage limitation can be overcome by using floating regulator techniques.

The limits on V_{IN} can be overcome by using a preregulator to feed the V+ and V_C lines, but the V_{OUT} limitation requires greater sophistication. The circuits of Figures 4-18 and 4-19 show two techniques that can be used to give output voltages well outside the range of the IC device.

In both circuits, R3 and CR1 provide a low voltage supply to preregulate the input voltage to a level within the IC ratings. The circuits of Figure 4-18 connects the internal pass transistor in the grounded emitter configuration through the 6.2 volt zener V_Z with overload protection provided by R5. Cascaded into the pass transistor is the high voltage transistor Q1 which provides level translation and voltage control to Q2, the pass transistor.

Short circuit protection can be arranged by removing base drive from Q2 is desired.

SWITCHING REGULATORS

Up to this point only series dissipative regulators have been discussed. All circuits presented thus far have the disadvantage of low efficiency. By definition these regulators must dissipate the power difference between input and output voltage and the load current such that

(Equation 4-18)

$$P_D = I_L (V_{IN} - V_{OUT})$$

This is in addition to the standby power dissipation of the regulator circuit itself. Thus, it becomes prohibitive in terms of efficiency to build a dissipative regulator with high output currents and high input to output voltage differentials. These parameters are best implemented with a switching type regulator taking advantage of the very high efficiency of such a circuit. By using the switching technique the power transistor requirements and its associated heat sink size can be greatly reduced.

Switching regulators consist of a switch S, a level detector, and an LC network L1, C1 as depicted in Figure 4-20. The cycle begins when switch S is closed causing a nearly linear current to build up through L1. This current, less the load current, charges C1 until the upper threshold of the detector is reached.

At this point S1 is opened and D1 forward conducts eventually discharging C1 through L1 to the lower threshold limit at which time S1 closes, restarting the sequence. A sketch of the basic waveforms is shown in Figure 4-21 for two different duty cycles. The output voltage is a function of the duty cycle of the switching waveform.

SWITCHING REGULATOR WAVEFORMS

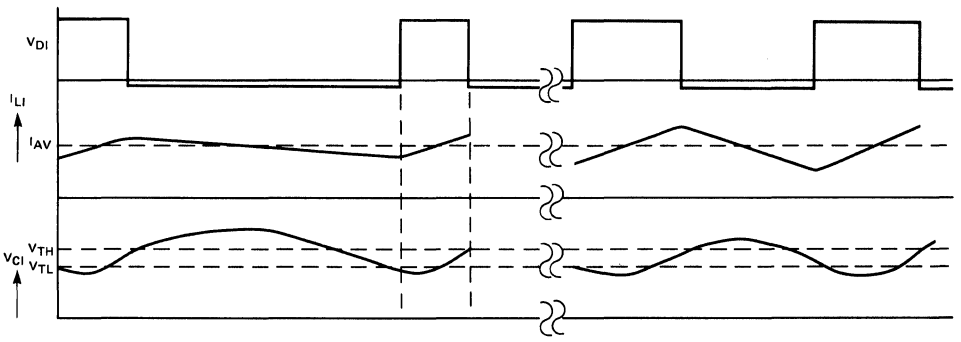


Figure 4-21

Therefore, regulation can be achieved if the duty cycle is made variable as is the case with switching regulators. The detailed theory and design of switching regulators is complex, but the basic operation makes the following assumptions:

1. Operating frequency well above resonant frequency of L and C.
2. Harmonics of input square wave are attenuated.
3. Phase shift of lowest frequency is 180°.

The last assumption provides the minimum output ripple at close to the hysteresis limits of the threshold control device.

The frequency of operation is a function of load levels, input voltage levels, and threshold levels. Although it is possible to synchronize the switching frequency with an external source, the electrical interference problem usually requires that the regulator be well shielded. The choice of operating frequency is in general a compromise between the inductor size becoming prohibitive at low frequencies, and switching losses in D1 and S1 becoming excessive at high frequencies. Values between 10 and 25kHz are normally satisfactory. Note that the load current flows as a dc current through L1, and that the peak current I_{MAX} can be quite a bit more than that. The inductor should not saturate at that level, or the frequency will increase abruptly, the efficiency will fall rapidly, and potential disaster will ensue. The diode and switch must also handle I_{MAX}. There is a considerable high frequency ripple current in C1 of $\mp (I_{max} - I_{out})$. The component used must be capable of handling that current.

A circuit realization for Figure 4-20 is shown in Figure 4-22. The switch S1 is replaced by a Darlington pnp pair Q1 and Q2 and the threshold detector by the 550 device, driving Q1 and Q2 from the V_C pin.

The peak driving current through the 550 is set by R_{SC}. This does not, of course, protect the whole regulator, just the 550 itself. The threshold values are set by V_{REF} in combination with R1 and R2, and the threshold hysteresis is controlled by R3 and the internal impedance of V_{REF} (about 2kΩ), as derived from the voltage across D1. The capacitor across R1 reduces the ripple on the output by increasing the feedback at ripple frequencies. Diode D2 prevents the possibility of initial latchup in the 550. A similar circuit can be used for the μA723, if a resistor of 1—2kΩ is included between V_{REF} and the junction of R3 and the non-inverting input, and the values of R1 and R2 are modified to suit the different V_{REF} value.

The component values may be chosen by the following algorithm, which is approximate:

Neglecting switching transients,

$$V_{OUT} = t_{ON} f V_{IN}$$

where t_{ON} is the time S1 is on, and f is the frequency of operation, so having chosen f for some V_{IN}, and knowing V_{OUT}.

(Equation 4-19)

$$t_{ON} = \frac{V_{OUT}}{V_{IN}}\left(\frac{1}{f}\right) \text{ and } t_{OFF} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right)\left(\frac{1}{f}\right)$$

The current in L1 increases almost linearly during t_{ON}, so we may find L1 from I_{OUT}, I_{MAX}, and t_{ON}, or t_{OFF}

(Equation 4-20)

$$L_1 = \frac{(V_{IN} - V_{OUT})(t_{ON})}{2(I_{MAX} - I_{OUT})} = \frac{V_{OUT}\, t_{OFF}}{2(I_{MAX} - I_{OUT})}$$

The output ripple is derived from the difference between IL1 and I_{OUT} charging C1, so for a given output ripple ΔV_{OUT}, we can write

(Equation 4-21)

$$C_1 = \frac{I_{MAX} - I_{OUT}}{4f\Delta V_{OUT}} = \frac{V_{IN} - V_{OUT}}{8L1f^2V_{IN}} \cdot \left(\frac{V_{OUT}}{\Delta V_{OUT}}\right)$$

Note that if we put

$$\frac{V_{IN} - V_{OUT}}{V_{IN}} \simeq 1$$

we find

(Equation 4-22)

$$f \simeq \frac{1}{(8L1C1)1/2} \cdot \left(\frac{\Delta V_{OUT}}{\Delta V_{OUT}}\right)^{1/2}$$

The values of L1 and C1 also control the load transient response. The voltage overshoot for a load decrease of ΔI_{OUT} is

(Equation 4-23a)

$$\Delta V_{OUT} = \left(\frac{\Delta I_{OUT} t_r}{2C1}\right) = \left(\frac{\Delta I_{OUT2}}{V_{OUT}}\right)\left(\frac{L1}{C1}\right)$$

where the recovery time

(Equation 4-23b)

$$t_r = 2L1\left(\frac{\Delta I_{OUT}}{V_{OUT}}\right)$$

and for a load increase of ΔI_{OUT} is

(Equation 4-23c)

$$\Delta V_{OUT} = \frac{\Delta I_{OUT} t_r}{2C1} = \left(\frac{\Delta I_{OUT2}}{V_{IN} - V_{OUT}}\right)\left(\frac{L1}{C1}\right)$$

and

(Equation 4-23d)

$$t_r = 2L1\left(\frac{\Delta I_{OUT}}{V_{IN} - V_{OUT}}\right)$$

The exact frequency of oscillation and, in fact, the functionality of the circuit depends upon the parasitic components. From the preceding equations it follows that the circuit as shown will not sustain oscillation. Fortunately the imperfections of components comes to the rescue and the circuit is restored to operation by the parasitic elements indicated in Figure 4-23. The most

important of these is the series resistance of C1, R_C.

The effective series resistance of the inductor R_L also contributes, and the storage in diode D1 adds a small step. These contributions are indicated in the waveforms of Figure 4-24. All generate a difference in V_{OUT} at the two switching points, which of course must correspond to the hysteresis in the threshold detector. Acting in the opposite direction are the delay, and the rise and fall times in the switch.

Considering first the effect of R_C, we may write at once (even through we don't know the value of R_C),

(Equation 4-24)

$$V_{T/R_C} = 2(I_{MAX} - I_{OUT})\,R_C$$

Substituting into equations 4-18 and 4-19, we obtain

(Equation 4-25)

$$f = \frac{V_{OUT}}{V_{IN}}\left(\frac{1}{t_{ON}}\right) = \frac{V_{OUT}}{V_T}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)\frac{R_C}{2L1}$$

The easiest way to establish the effect of R_L is to assess the phase change for the first harmonic of the waveform on V_{D1}. This procedure is at best approximate, but except for extreme duty cycles, the higher harmonics at the input are smaller than the first. Since the attenuation of L and C is at 12dB per octave, the influence on the answer obtained of these harmonics is small. It is convenient to treat the switching delays in S1 as a phase change at the same point.

This total phase change can then be written

(Equation 4-26)

$$\Theta \simeq \frac{R_L}{2\pi fL1} - 2\pi f t_s$$

where

$$t_s = \frac{1}{2}\,(t_r + t_f)$$

This leads to a threshold voltage difference at the switching points (assuming the phase change is small) of

(Equation 4-27)

$$V_T|R_L = \Delta V_{OUT}\sin(\pi f\, t_{ON})\left[\frac{RL}{2\pi fL1} - 2\pi f\, t_s\right]$$

$$= V_{OUT}\sin\left(\frac{\pi V_{OUT}}{V_{IN}}\right)\left[\frac{R_L}{2\pi f\, L1} - 2\pi f\, t_s\right]$$

The stored charge in the transistor forming S1 is primarily introduced by the threshold detector, and its removal can be included in the fall time t_f accounted for in equation 4-26. The charge removal from the diode is performed by S1, which passes a current surge when switching on. This current does not pass through L1 and has no influence on the remainder of the circuit. However, the charge needed to turn the diode on is provided by the current in L1. The voltage impulse needed to do this gives a current step in I_{L1} given by

$$I = \frac{Q_D R_D}{L1}$$

where Q_D is the stored charge, and R_D is the effective series impedance of the diode.

SELF OSCILLATING SWITCHING REGULATOR

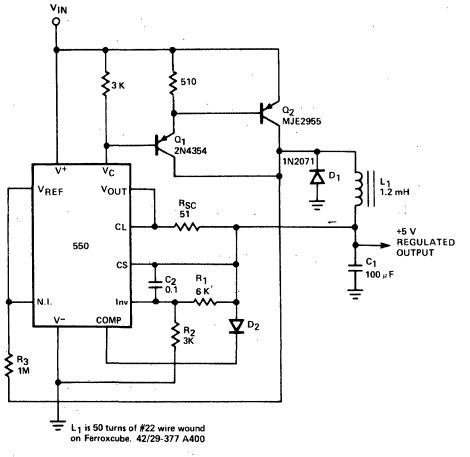


Figure 4-22

PARASITIC COMPONENTS

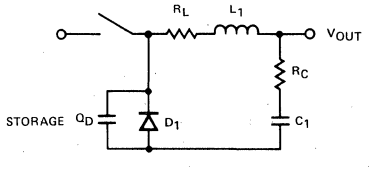


Figure 4-23

CONTRIBUTIONS OF PARASITIC ELEMENTS

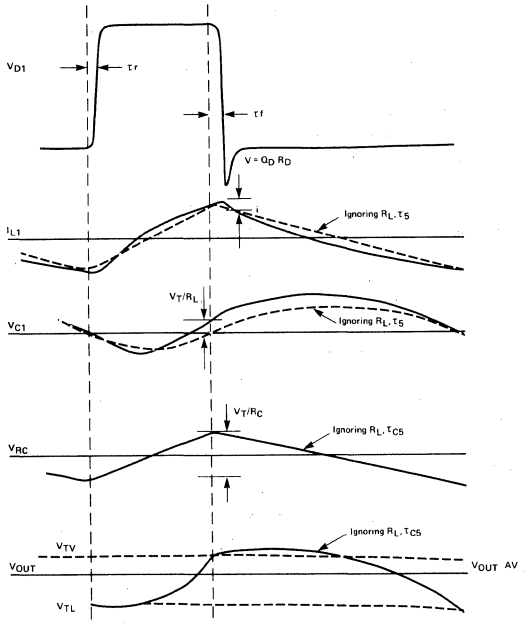


Figure 4-24

This leads to an effective V_T of approximately

(Equation 4-28)

$$V_T|_{Q_D} = \left(\frac{Q_D R_D}{2L1C1}\right)\left(\frac{V_{OUT}}{V_{IN}}\right) t_{ON}$$

The waveforms resulting from these various terms are sketched in Figure 4-24.

Note that in the circuit of Figure 4-22, the value of V_T at which the circuit operates is a function of V_{IN}, so the frequency may be approximated by

(Equation 4-29)

$$f \simeq \left(\frac{R_S}{R_{INT}}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)\left(\frac{R_C}{2L1}\right)$$

where R_{INT} is the internal reference impedance, about 2KΩ.

As a function of V_{IN}, we can see that f will be low for both high and low values of V_{IN} and it will go through a maximum to the point near where $V_{IN} \approx 2\ V_{out}$.

The value of R_C can be estimated from equation 4-28 and gives a value of 0.35 to 0.4Ω. Since the performance of the circuit depends to some extent on the effective series impedance of C1, which may not be sufficiently well controlled for some applications, it may be worthwhile to place a small value resistor in series with C1 to reduce circuit to circuit variation.

In applications where the frequency of operation is important (such as EMI supression), the regulator may be locked to an external signal by means of the circuit of Figure 4-25.

The incoming signal is converted to a triangle wave by R3 and C3, and added to the reference voltage. If the drive signal is already a triangle wave, (derived from pin 4 of a 566 oscillator) C3 can be omitted, and R3 increased to about 100KΩ. The amplitude of the triangle wave at the reference pin must exceed the amplitude of the ripple on V_{OUT}, (50mV is suitable for normal use). The duty cycle of the switching pulse is controlled by the relative values of V_{OUT} and the (referred) V_{REF} with impressed triangle, thus ensuring the required regulation. The remainder of the circuit operates as precisely as before. Note that neither switching point is controlled in phase relative to the controlling waveform. Thus, spikes from other controlled regulators could cause false switching if inadequately shielded from each other. The line regulation is closely related to the amplitude of the triangle wave. The gain of the amplifier is adequate to give sharp switching transitions, even without explicit positive feedback.

A negative switching regulator may be constructed similarly, as shown in Figure 4-26. The same basic restrictions apply here as in the simple negative regulator of Figure 4-14, the output voltage must be at least -8.5V unless a positive supply is available. The basic operation is the same as before. An alternative negative switching regulator is shown in Figure 4-27. This circuit always needs a positive supply.

All these regulators suffer from a lack of short circuit protection. The difficulty in providing protection is that the regulator must continue to switch. If it does not, the switching transistors will become pass transistors with an extreme increase in dissipation!

SYNCHRONIZED SWITCHING REGULATOR

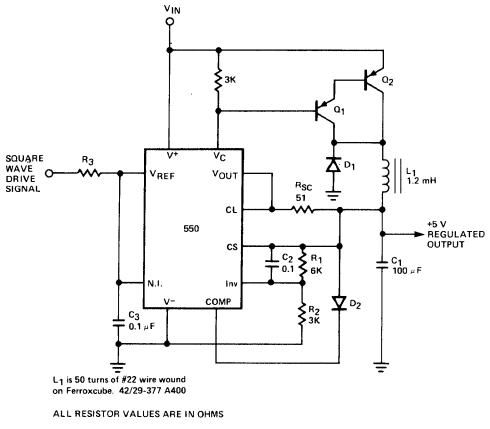


Figure 4-25

NEGATIVE SWITCHING REGULATOR

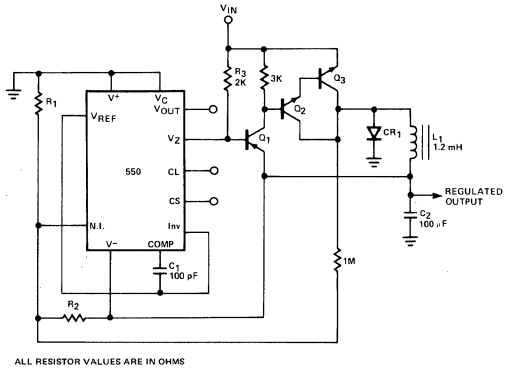


Figure 4-26

SWITCHING REGULATOR (LESS THAN -8.5 VOLTS)

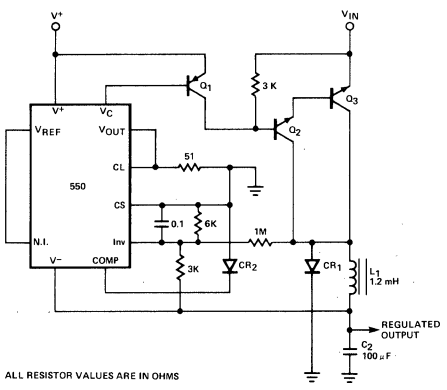


Figure 4-27

SHORT CIRCUIT PROTECTION

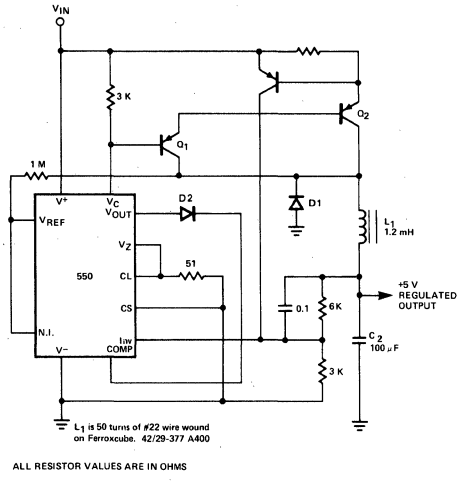


Figure 4-28

SENSING INDUCTOR CURRENT

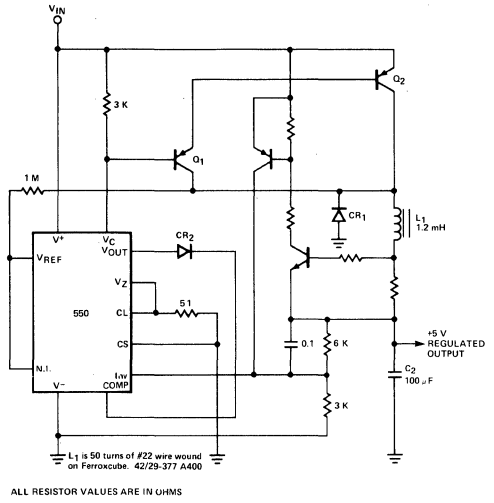


Figure 4-29

REDUCING REGULATOR NOISE

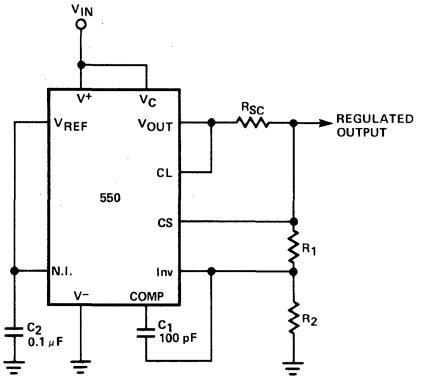


Figure 4-30a

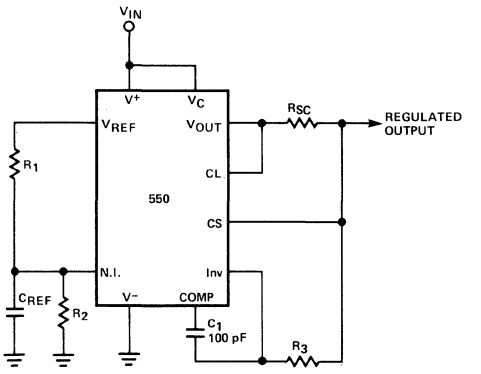


Figure 4-30b

In general, the best way to arrange for continued switching is to modify the voltage feedback to the amplifier in order to effectively maintain V_{REF} at the comparison point even in shutdown. This can be achieved simply by sensing the current in the switching transistor, as shown in Figure 4-28.

This has a disadvantage in that the current surge when the transistor switches the diode off must be allowed for, and the limit point is somewhat dependent on duty cycle. A better arrangement is shown in Figure 4-29. This needs more external transistors, but gives much better control since the current through the inductor is sensed.

The current derived is used to raise the apparent output voltage as seen at the inverting input. Since the amplifier will not work with V_{OUT} at ground, the V_Z output is tied to ground. The V_Z output can be tied to V_{OUT}, avoiding the waste of that current, if the input-output differential is large enough. Note that this technique can be applied to the negative regulator shown in Figure 4-27, (provided V+ is more than 8.5V), but not to that of Figure 4-26.

Since the dissipation in the switching devices is not very dependent on either V_{IN} or V_{OUT}, the elaborate protection schemes devised for the pass transistor case are not really applicable here. For applications where the ripple, transient and regulation performance of the switching regulators are unacceptable, a combination of a switching regulator which gives highly efficient preregulation for a static regulator may provide a satisfactory solution.

NOISE, TEMPERATURE EFFECTS, AND TRANSIENT RESPONSE

An almost inherent property of reverse biased junctions of the emitter base type is voltage noise at breakdown as a result of so-called microplasmas. The noise arises as a

result of space-charge induced instability of the breakdown of localized minor imperfections and irregularities. The inherently clean and defect free processing used for integrated circuits reduces this effect to a minimum, but the statistical inevitabilities of diffusion processes have sufficient irregularity to lead to some small noise generation. The characteristic noise pattern is displayed as step-function current change as each microplasma switches on and off. Each microplasma switches at roughly constant voltages, leading to approximately constant voltage transitions.

Since the reference voltage for the 550 is derived from the breakdown of the emitter-base junction, this noise will appear at the reference terminal. Transformed by the internal network between the zener diode and the reference terminal, this is the major component of noise in the regulator. For applications where the noise level could be troublesome, it can be reduced by putting a low pass filter between the zener and the amplifier input. The low frequency component of the noise is quite small. Since the internal reference impedance of the 550 is 2KΩ, placing a capacitor between V_{REF} and ground will generally be all that is required.

In circuits where the reference is divided down, the divider impedance provides some effective series resistance, but in other applications better results may be obtained by the use of a simple series RC network. Suitable circuits are shown in Figures 4-30a and 4-30b.

The line and load regulation performance discussed in previous sections and presented in the data sheets are all values defined and measured under such conditions that the die temperature is constant. The circuit dissipation is changed by changes in input line voltage and load current. Therefore, the consequent changes in die temperature, which primarily affects the reference voltage, must be accounted for separately. The temperature effects are certainly not negligible in many applications.

A regulator operating at $10V_{in}$ and $5V_{out}$ with a load current that steps from 1mA to 50mA will have a short time (1-10msec) output voltage change of typically under 3mV. The dissipation increases, however, by 250mW, leading to a temperature rise of about 25°C at the die. With temperature coefficient of 0.005%/°C, this leads to an output voltage change of 6mV, twice the short time value. If the input voltage had been higher, say 15V, the same load step would eventually result in about four times the voltage change, though the short term change would not be affected significantly.

The effects of transient line and load changes are primarily concerned with the impulse response of the amplifier, which in turn depends on the compensation and external connections involved in the particular circuit being used. Typical transient responses for simple configurations are given for the 550 in Figure 4-31.

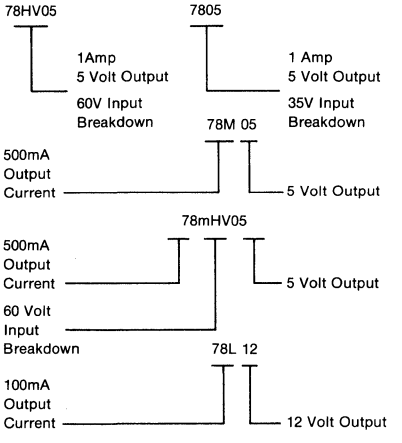
There are three effects to be considered, then, upon imposition of a line or load step to a regulator circuit; the initial reaction is controlled by the transient response. After a few microseconds, the transient dies away and the response becomes the data sheet defined regulation. After a time of many tens of milliseconds, the changing die temperature begins to take effect. After perhaps one minute, the die temperature stabilizes and no further changes occur. As mentioned above, each of these effects is effectively separate, and should be allowed for separately.

3 TERMINAL REGULATORS

Introduction

The μA7800 and 78HV00 series regulators are monolithic three terminal devices intended for fixed voltage outputs. Since no external elements are required they are excellent candidates for PC card and subsystem regulation. With the use of these devices much system crosstalk and power supply distributed noise can be eliminated.

These devices are available in 5, 6, 8, 12, 15, 18 and 24 volts, positive or negative, with 3 output current ratings. The voltage and power output ranges are designated as follows:



TRANSIENT RESPONSE

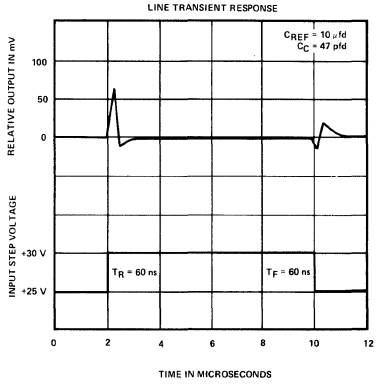


Figure 4-31a

TRANSIENT RESPONSE

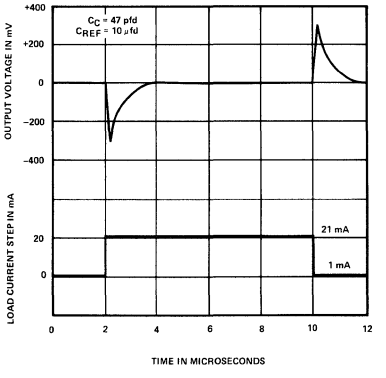


Figure 4-31b

SERIES PACKAGE	7800 TO-3	7800C TO-3	7800C TO-220	78MOO TO-39	78MOOC TO-39	78MOOC TO-220	UNIT
Maximum junction temperature, T_J(MAX)	150	125	125	175	175	125	°C
Minimum ambient temperature, T_J(MIN)	-55	0	0	-55	0	0	°C
Thermal resistance junction-to-case, Θ_{JC}	4	4	4	20	20	5	°C/W
Thermal resistance junction-to-case, Θ_{JA}	35	35	50	150	150	50	°C/W
Maximum allowable dissipation, P_D(MAX)	15	15	15	5	5	5	W

Figure 4-32

The μA78HV00 has a unique process which gives an input breakdown voltage greater than 60 volts. Standard operating conditions allow the input voltage to be as high as 48 volts continuous. Transients and momentary inputs may be as high as 60 volts without damaging the regulator. Under these high input conditions, the regulator may go into current limiting or thermal shutdown.

Voltages other than those listed are also available upon special order.

Applications

As with any voltage distribution system, effort should be expended to keep the output impedance of three terminal regulators as low as possible.

Possessing 20 to 30 milliohms output impedance at low frequencies, the regulator's output impedance will increase with frequency. This becomes significant, especially in TTL systems, where current impulses from the logic are in the Megahertz regions. Thus it becomes necessary to bypass the supply lines for high frequencies to insure stability and error free operation. The best technique for achieving low impedance at all frequencies is to use a large tantalum (10-47μfd) in parallel with small (0.01μfd) disc ceramics. In systems where fairly large printed circuit boards are used, the disc ceramics should be disbursed upon the board to neutralize the trace inductance. No other stabilization techniques should be required.

Thermal Limitations

The maximum allowable junction temperature and the ambient temperature expected determine whether a heat sink will be required for a particular regulator application.

As seen from the derating curves of Figure 4-32 the maximum no heat sink power dissipation allowable for the TO-3 is 3 watts and for the TO-220 is 2 watts. Above 25°C this must be derated according to the relationship

(Equation 4-30)

$$\frac{TJ\ (MAX) - T_A}{\Theta_{JA}}$$

Figure 4-32 summarizes the maximum junction temperature and thermal resistivities of the TO-3 and TO-220 packages. The power dissipation qualities of heat sinks are usually well established by the manufacturer. Since the common terminal of these devices is common they may be bolted directly to the chassis, using the surface area as the heat sink.

Figure 4-33 provides a selection chart which relates surface area of the chassis material to the thermal resistivity. It should be noted that the surface area refers to both sides of the material.

In order to find a thermal resistivity scribe a vertical line from the surface area across the appropriate material.

Heat Sinks

As a further aid in determining which package/heat sink combination is best suited to a given application, the following nomograph (Figure 4-35) solves for Θ_{JA} from basic current, input/output voltage differential and ambient temperature information. The package thermal resistances have been superimposed on the Θ_{JA} line E. If the required Θ_{JA} is less than Θ_{JC} for a package, then that package cannot be considered. Even if an infinite heat sink were possible, the junction temperature would exceed 125°C. If the required Θ_{JA} is greater than Θ_{JA} for a package, that package may be used without a heat sink. In all other cases a package/heat sink combination is necessary. Subtract Θ_{JC} for the preferred package from the required Θ_{JA} to arrive at the necessary heat sink thermal resistance Θ_{HS}.

To use the nomograph, select the maximum load current on Line A and the maximum input/output voltage differential on Line D. The line joining these points intersects Line B at a point representing the maximum

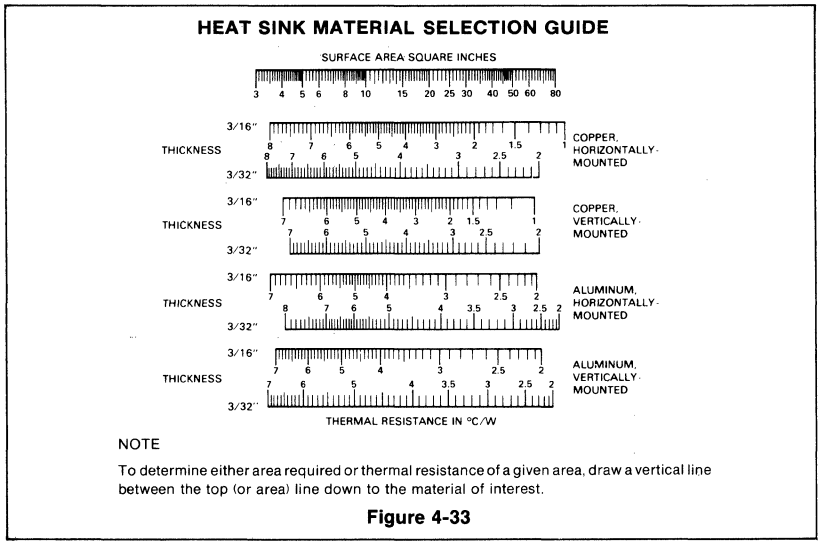


Figure 4-33

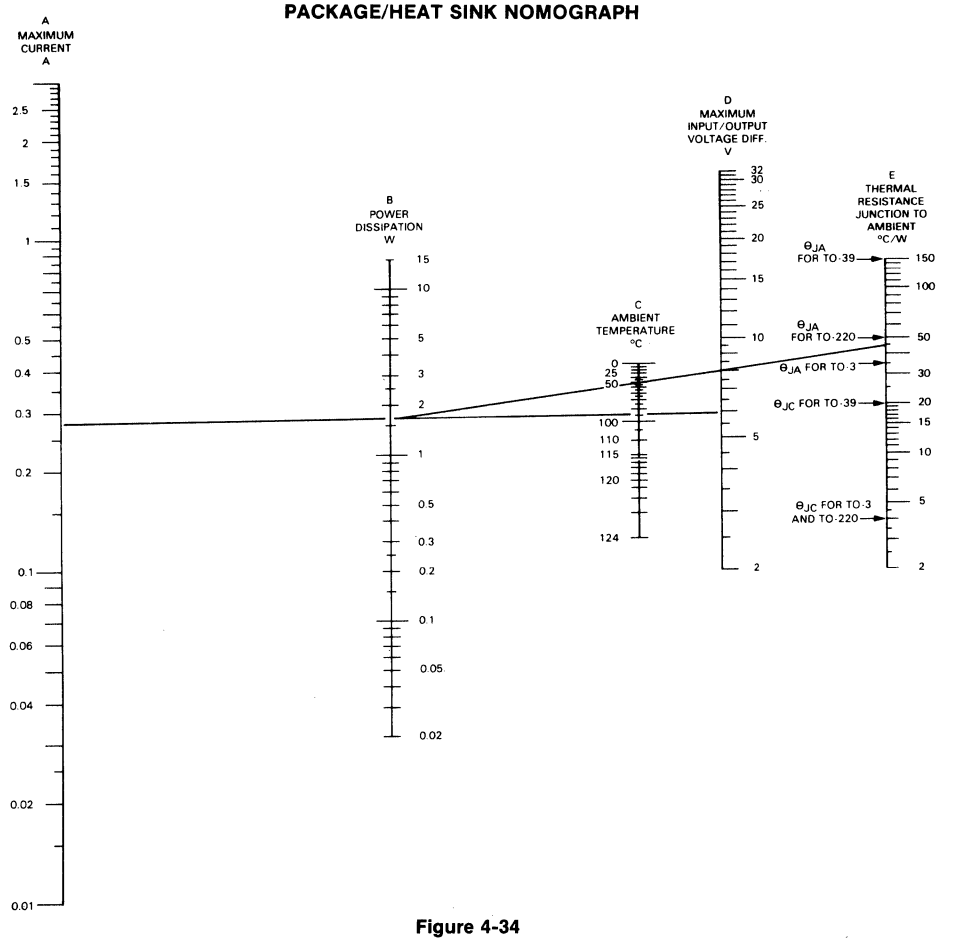


Figure 4-34

power dissipation. Join this Line B intersection to a point on Line C representing the maximum expected ambient temperature. Extend this line so it intersects Line E. The Line E intersection represents the total junction-to-ambient thermal resistance required for the particular application. If the Line E intersection falls above the junction-to-ambient thermal resistance, Θ_{JA}, no heat sink is required.

To determine the thermal resistance of a heat sink, subtract the junction-to-case thermal resistance, Θ_{JC}, of the selected package from the Line E intersection.

- For TO-39, subtract 20°C/W
- For TO-3, subtract 4°C/W
- For TO-220, subtract 4°C/W

Example:

Choose a regulator to supply 275mA (max) with an input/output voltage differential of 6V (max) at an ambient temperature of 50°C (max). Join the 275mA point on Line A to the 6V point on Line D. The intersection with Line B gives a power dissipation of 1.7W. Join 1.7W to the 50°C point on Line C and extrapolate to an intersection with Line E. This gives a total junction-to-ambient thermal resistance requirement of 45°C/W. The regulator package choices are

- A TO-39 package with a heat sink of 25°C/W thermal resistance (subtract 20°C/W Θ_{JC}).
- A TO-220 package with a heat sink of 41°C/W thermal resistance (subtract 4°C/W Θ_{JC}).
- A TO-3 package with no heat sink (45°C/W falls above Θ_{JA} for the TO-3).

Additional Applications Ideas

The versatility of the 7800 family of regulators may be increased beyond the basic 3-terminal use by the addition of external components. The following applications contain circuits which cover the range of 0.5V to 30V output, and output currents in excess of 10A. Note that apart from power considerations the 7800 and 78M00 devices are interchangeable in all applications.

Fixed Output Regulator

In this basic application of Figure 4-35, the last two digits of the device code specify the nominal output voltage. The insulating washer normally used when heat-sinking a power transistor may be omitted when mounting the regulator since the case of the device is at ground potential. This is true unless circulating ground currents are a problem.

Current Regulator

The circuit shown in Figure 4-36 supplies a regulated current to a load, its value being determined by an external resistor. The minimum input/output differential in this application is (minimum regulator input/output differential voltage) + (maximum

BASIC FIXED OUTPUT REGULATOR

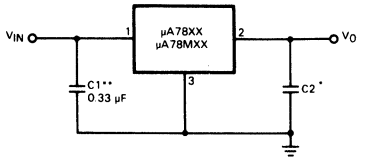
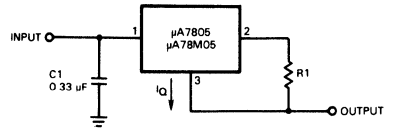


Figure 4-35

BASIC CURRENT REGULATOR



$$\text{Output Current} = \left(\frac{5.0\ V}{R1}\right) + I_Q$$

Figure 4-36

HIGH CURRENT REGULATORS

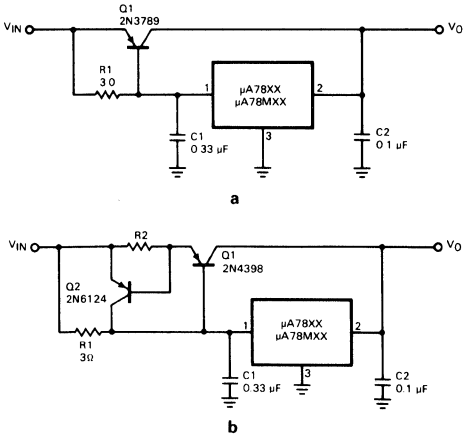


Figure 4-37

VARIABLE OUTPUT REGULATOR

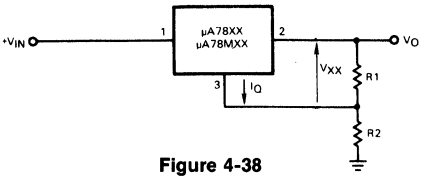


Figure 4-38

SWITCHING REGULATOR

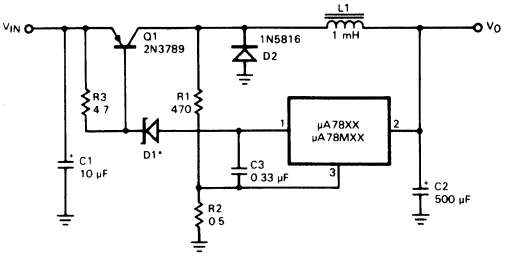


Figure 4-39

regulator output voltage). For currents up to 1A 0° C to 70° C, this voltage is typically 2.2V + 5.25V, or 7.45V.

High Current Voltage Regulators

Currents in excess of the output capabilities of the basic regulator can be obtained with the circuit shown in Figure 4-37. The value of R1 determines the point at which Q1 begins to conduct and hence bypasses the regulator. This supply can be protected against a short circuit load by adding a short circuit sense resistor, R2, and a pnp transistor Q2. In this circuit Q2 must be able to handle the short circuit current of the regulator, since when Q1 is bypassed, the regulator goes into its short-circuit mode.

Variable Output Voltage Regulators

In Figure 4-38 a voltage pedestal is developed across R2, which is then added to the normal regulated output V_{XX}, such that

$$V_O = V_{XX}\left(1+\frac{R2}{R1}\right)+I_QR2$$

The current through R1 should be set much higher than the quiescent current I_Q to minimize the effects of the change in I_Q which occurs with a change in V_{IN}.

Switching Regulators

A switching regulator may be used in those cases where the dissipation of a linear regulator is excessive. Figure 4-39 shows that when power is first applied, current flows through R3 and the 7800 device to the output. As soon as the current generates a voltage drop sufficient to forward bias Q1's base-emitter junction, Q1 is driven toward saturation. The increase in voltage at the collector applies power through L1 to the load and provides positive feedback through R1 and R2 to assure a full switching action. As the output voltage approaches the sum of the 7800 regulated output plus the voltage developed across R2, current flow through the 7800 decreases

Input voltages in excess of the maximum input voltage rating of the regulator may be commodated by the inclusion of a voltage dropping Zener (D1). This reduces the voltage appearing across leads 1 and 3 of the 7800 to an acceptable level.

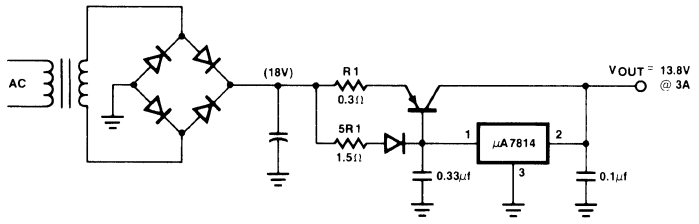
When the base current drops below the level required to keep Q1 in saturation, the collector voltage starts to decrease and the positive feedback loop completes the switching action.

μA7814

There is a sufficient requirement for a power supply output voltage of 13.8 volts. Therefore, Signetics Analog now offers the μA7814 type 1 amp three terminal regulator with 13.8 volts nominal output.

One of the main requirements for this 13.8 volt regulator is for AC line operation of automotive type equipment. With the increase in the number of CB sets and the servicing required on CB, AM/FM stereo radio, the battery substitution power supply is becoming more prevalent. Another major need for battery substitution power supplies is in the home operation of the portable automotive equipment. The portable CB can be removed from the vehicle to prevent theft and also utilized in the home with a

BATTERY SUBSTITUTION POWER SUPPLY

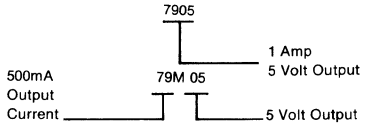


battery substitution power supply using the μA7814.

NEGATIVE REGULATORS

Introduction

The μA79 series regulators are monolithic three terminal devices intended for negative fixed voltage outputs. They are an excellent choice for PC card and subsystem regulation due to their self-contained simplicity. These devices are available in negative 5, 6, 8, 12, 15, 18 and 24 volts. The voltage and power output ranges are designated as follows:



Voltages other than those listed are also available upon special order.

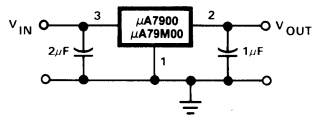
Applications

As with the μA78 voltage regulators, effort should be made to keep the output impedance as low as possible. This is accomplished with bypass on the supply lines for high frequencies to insure stability and error-free operation. Use a large tantalum (10-47μfd) in parallel with a small (.01μfd) disc ceramic. Output bypass capacitors will improve the transient response of the regulator. A good high frequency ceramic or tantalum of 1μf will generally suffice. Keep lead lengths as short as possible.

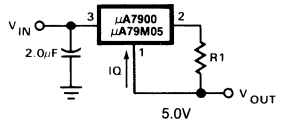
All of the applications for Signetics positive regulators can be used with the negative regulators. The polarities are inversed, the sense diode is reversed and the pnp's are replaced with NPN transistors. Specific circuit configurations follow:

TYPICAL APPLICATIONS μA79XX SERIES

FIXED OUTPUT REGULATOR

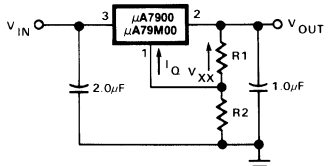


BASIC CURRENT REGULATOR



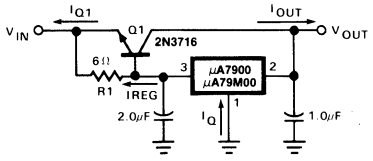
$$\text{Output current} = \frac{5.0V}{R1} + I_Q$$

VARIABLE OUTPUT VOLTAGE REGULATOR



$$|V_{OUT}| = V_{XX}\left(1 + \frac{R2}{R1}\right) + I_Q R2$$

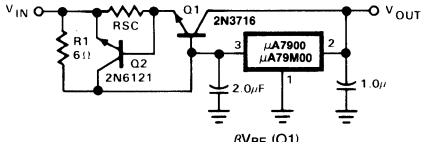
HIGH CURRENT VOLTAGE REGULATOR



$$R1 = \frac{V_{BE(Q1)}}{I_{REG}} = \frac{\beta V_{BE}\,(Q1)}{I_{REQ(MAX)}\,(\beta + 1) - I_{OUT(MAX)}}$$

$$I_{Q1} = \beta(Q1)\, I_{REG}$$

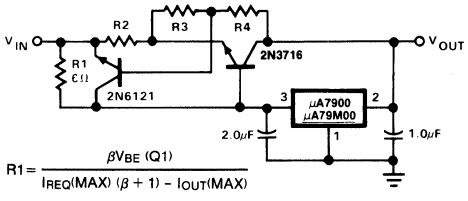
HIGH OUTPUT CURRENT, SHORT CIRCUIT PROTECTED



$$R1 = \frac{\beta V_{BE}\,(Q1)}{I_{REQ(MAX)}\,(\beta + 1) - I_{OUT(MAX)}}$$

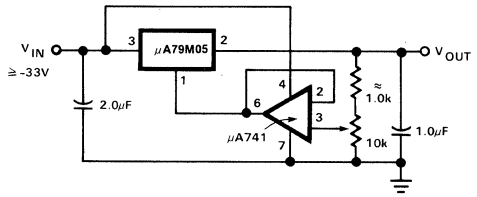
$$R_{SC} = \frac{V_{BE(Q2)}}{I_{SC}}$$

HIGH OUTPUT CURRENT, FOLDBACK CURRENT LIMITED

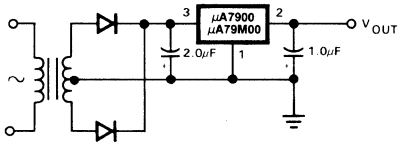


$$R1 = \frac{\beta V_{BE}\,(Q1)}{I_{REQ(MAX)}\,(\beta + 1) - I_{OUT(MAX)}}$$

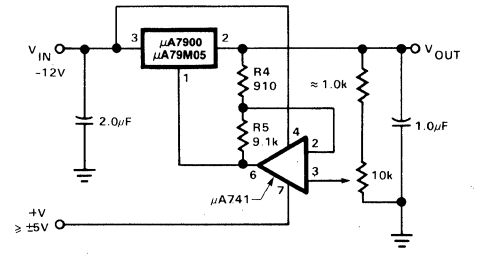
VARIABLE OUTPUT VOLTAGE, -30V TO -7V



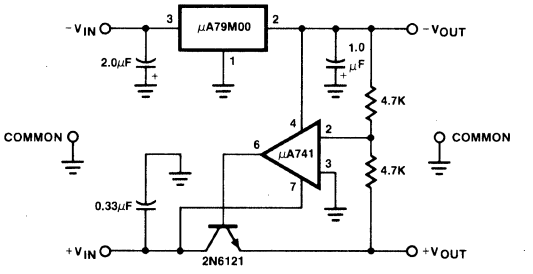
NEGATIVE OUTPUT VOLTAGE CIRCUIT



VARIABLE OUTPUT VOLTAGE, -0.5V TO -10V



POSITIVE AND NEGATIVE TRACKING VOLTAGE REGULATOR



PROGRAMMABLE REGULATORS

Introduction

The μA78G and μA79G are positive and negative programmable regulators respectively. They are identical to their μA78 and μA79 counterparts with the exception to the reference to the error amplifier being brought out and the voltage determining divider being supplied by the circuit designer rather than internal to the regulator. The voltage may be adjusted over the range of 5 to 30V for the μA78G and μA79G from -30 to -2.2 volts. They have the same inherent feature that other devices in the series have.

Applications

The basic programmable voltage regulator circuits and design considerations follow.

DESIGN CONSIDERATIONS

The 78G and 79G adjustable voltage regulators have an output voltage which varies from $V_{CONTROL}$ to typically $V_{IN} - 2V$ by $V_{OUT} = V_{CONTROL} \frac{(R1 + R2)}{R2}$. The nominal reference in the 78G is 5.0V and 79G is -2.23V. If we allow 1.0mA to flow in the control string to eliminate bias current effects, we can make R2 = 5kΩ in the 78G. The output voltage is then: $V_{OUT} = (R1 + R2)$ V, where R1 and R2 are in kΩs.

Example: If R2 = 5kΩ and R1 = 10kΩ then V_{OUT} = 15V nominal, for the 78G; R2 = 2.2kΩ and R1 = 12.8kΩ then V_{OUT} = -15.2V typical, for the 79G.

By proper wiring of the feedback resistors, load regulation of the devices can be improved significantly.

Both 78G and 79G regulators have thermal overload protection from excessive power, internal short circuit protection which limits each circuit's maximum current, and output transistor safe area protection for reducing the output current as the voltage across each pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

	TYP	MAX	TYP	MAX
Package	θ_{JC}	θ_{JC}	θ_{JA}	θ_{JA}
POWER TAB	7.5°C/W	11°C/W	75°C/W	80°C/W
TO-3	4.0°C/W	6°C/W	44°C/W	47°C/W

$P_D (MAX) = \frac{T_J(MAX) - T_A}{\theta_{JC} + \theta_{CA}}$ or $\frac{T_J (MAX) - T_A}{\theta_{JA}}$.

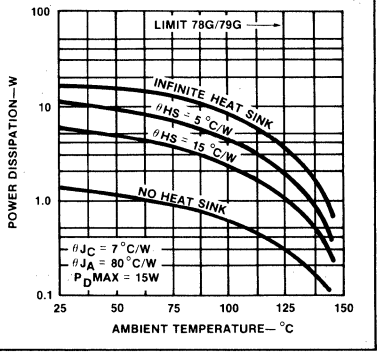
(Without a heat sink)

$\theta_{CA} = \theta_{CS} + \theta_{SA}$

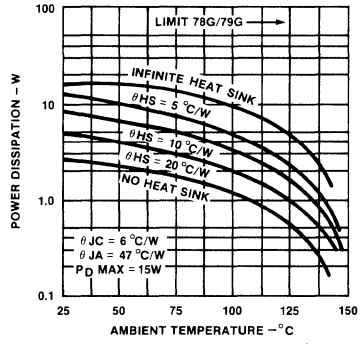
Solving for T_J: $T_J = T_A + P_D (\theta_{JC} + \theta_{CA})$ or $T_A + P_D\theta_{JA}$ (Without heat sink)

Where T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{J-A} = Junction to ambient thermal resistance
θ_{JC} = Junction to case thermal resistance
θ_{CA} = Case to ambient thermal resistance
θ_{CS} = Case to heat sink resistance
θ_{SA} = Heat sink to ambient thermal resistance

μA78G AND μA79G POWER TAB (U1) PACKAGE WORST CASE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

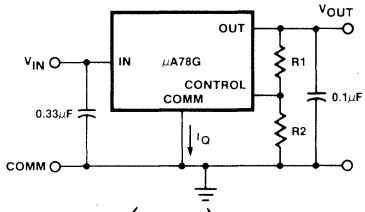


μA78G AND μA79G TO-3 PACKAGE WORST CASE POWER DISSIPATION vs AMBIENT TEMPERATURE



TEST LOAD CIRCUITS

μA78G TEST CIRCUIT 1

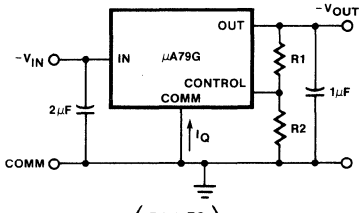


$$V_{OUT} = \left(\frac{R1 + R2}{R2}\right) V_{CONTROL}$$

$V_{CONTROL}$ Nominal = 5V

Recommended R2 current ≈ 1mA
∴R2 = 5kΩ (78G)
R2 = 2.2kΩ (79G)

μA79G TEST CIRCUIT 2



$$V_{OUT} = \left(\frac{R1 + R2}{R2}\right) V_{CONTROL}$$

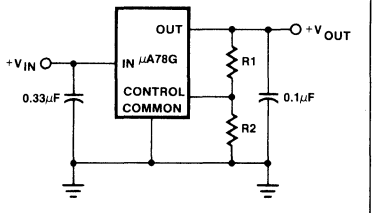
$V_{CONTROL}$ Nominal = –2.23V

Recommended R2 current ≈ 1mA
∴R2 = 5kΩ (78G)
R2 = 2.2kΩ (79G)

TYPICAL APPLICATIONS FOR μA78G

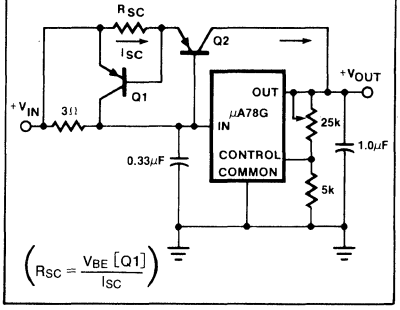
In many μA78G applications, compensation capacitors may not be required. However, for stable operation of the regulator over all input voltage and output current ranges, bypassing of the input and output (0.33μF and 0.1μF, respectively) is recommended. Input bypassing is necessary if the regulator is located far from the filter capacitor of the power supply. Bypassing the output will improve the transient response of the regulator.

BASIC POSITIVE REGULATOR



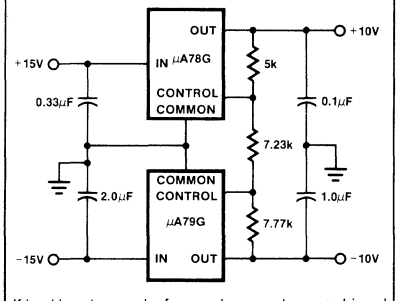
$$V_{OUT} = V_{CONT}\left(\frac{R1 + R2}{R2}\right)$$

POSITIVE HIGH CURRENT SHORT CIRCUIT PROTECTED REGULATOR



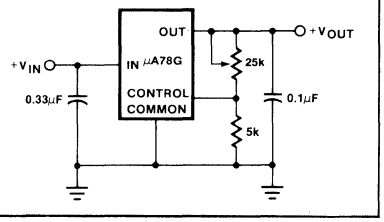
$$\left(R_{SC} = \frac{V_{BE}\,[Q1]}{I_{SC}}\right)$$

± 10V, 1.0A DUAL TRACKING REGULATOR

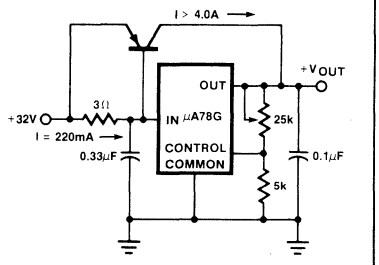


If load is not ground referenced, connect reverse biased diodes from outputs to ground.

POSITIVE 5 TO 30V ADJUSTABLE REGULATOR

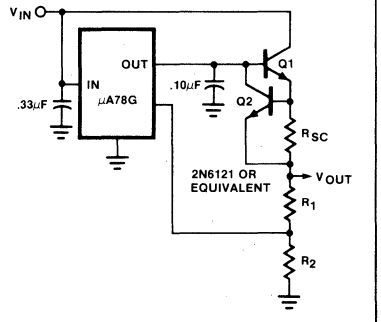


POSITIVE 5 TO 30V ADJUSTABLE REGULATOR I_{OUT} > 5.0A

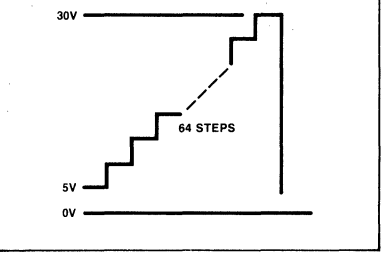


NOTE: External series pass device is not short circuit protected.

POSITIVE HIGH CURRENT SHORT CIRCUIT PROTECTED REGULATOR

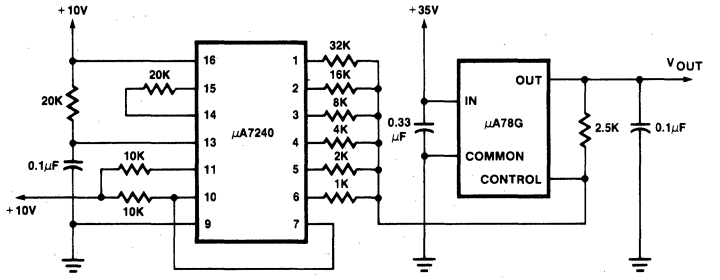


OUTPUT WAVEFORM

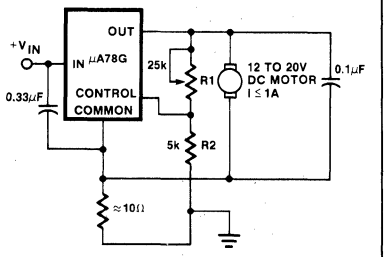


TYPICAL APPLICATIONS FOR μA78G (Cont'd)

PROGRAMMABLE SUPPLY



MOTOR SPEED CONTROL



Use flyback diode across motor if necessary.

NE/SE5554 DUAL TRACKING REGULATOR

The Signetics NE/SE5554 is a monolithic dual tracking regulator designed for use where dual supplies must track with close tolerances. It was designed with ease of production and high performance in mind. The intent was to supply a product which has performance surpassing its intended need and no additional features.

The device is composed of a negative, zener referenced regulator with an inverting amplifier-follower. The zener regulator has a zener controlled current source and a forward biased diode for temp. compensation. This classical reference was used for one main reason . . . simplicity. The main justification to use this is the devices intended use. Considering 4 basic contributors to output voltage change, (1) Line regulation, (2) Load regulation, (3) Temperature Coefficient, (4) Popcorn noise, all of these, and combinations of them, are small considering the uses this device is intended for:

1. Op-Amp Supplies
2. Sense-Amp Supplies
3. Analog Signal Processors (Driver-Gates, Mpx, etc.)
4. MOS-LSI Systems
5. Communications Circuits

These applications all have excellent power supply rejection or limited need for very close control of slight variations on supply lines. In short, it is an attempt to supply a customer with a device designed for his uses, but not costing money for features he doesn't need.

Both actual regulators are differential amplifiers followed by a gain stage followed by a Darlington with current limit. The negative regulator is the complement of the positive with the exception that the output stage is a compound PNP. The 5554 is essentially a dual 78M regulator.

The voltage dividers around the zener set the actual reference at 5 volts and allow positive and negative output voltages to be programmed conveniently. The various resistor values available with metal mask options, allow many different output voltage options as well as externally controlling output voltages by programming resistors to +Vout, -Vout, control and null.

The output current limit of 200mA was chosen as a compromise. The 100mA limit of the 78LXX Family is only marginally useful for many systems, where 0.5 amp is too much dissipation for two regulators in a TO-5 package thus, the 200mA limit.

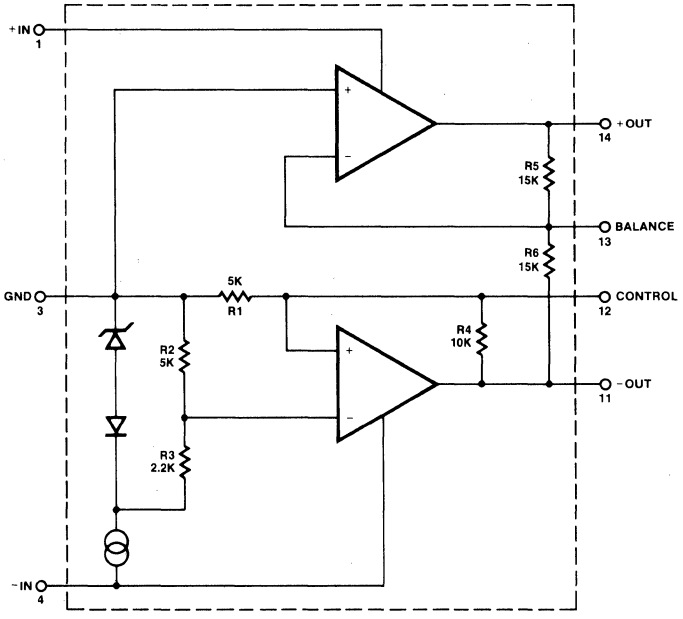
The regulators were designed to be on-chip compensated so external capacitors are not needed. This is a great advantage as most of the currently available devices require 10μf output capacitors or other cumbersome externally compensation.

The performance expectations reflect the intended use:

VOUT	Tolerance	5%
VOUT	Regulation (Load & Line)	1%
VOUT	Temp. Coefficient	65PPM/°C
VOUT	Noise	100μVRMS 10Hz - 10kHz

The intended use being power supplies, not reference supplies. Most devices these regulators would be driving have excellent

NE/SE5554 DUAL TRACKING REGULATOR EQUIVALENT CIRCUIT



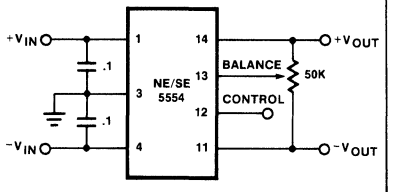
power supply rejection, such as operational amplifiers, Analog switches, MOS logic, communication circuits, and will not be adversely affected by the output voltage tolerances, including noise and temperature coefficient.

The initial output voltages of the 5554 will track exactly but the absolute pos voltage will be different from the absolute neg voltage. This is due to small process variations in the internal balance resistors.

NE/SE5554 DUAL TRACKING REGULATOR APPLICATION NOTE

For most applications, this difference is of no concern. For those applications where exact positive and negative voltages are necessary external balance potentiometer may be added as shown.

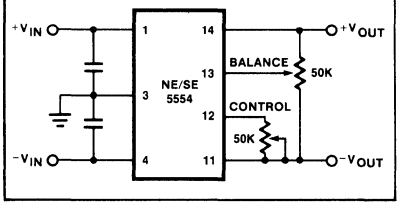
BALANCED DUAL TRACKING REGULATOR



This output balance control may be used to change the positive regulated voltage from about 0.2 volts to ≥ 16 volts without changing the negative regulated voltage.

To change the negative regulator voltage from its fixed value it is necessary to use the control function. With zero resistance between the control pin and $-V_{OUT}$, the output will be ±5.0 volts. Increasing the resistance to 50K will give full output. This control, in conjunction with the balance, can give output voltage of ±5V to about $\pm V_{IN}$ - 3 volts.

VARIABLE OUTPUT TRACKING REGULATOR

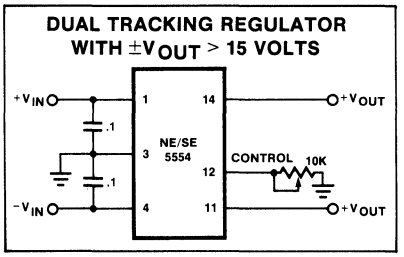


In order to prevent instability in this circuit when the control resistance approaches zero ohms, it is necessary to use a filter capacitor on $-V_{OUT}$ of 0.1μf or larger to ground. A 10μf from $+V_{OUT}$ and $-V_{OUT}$ to ground will improve transient response, where this is of concern.

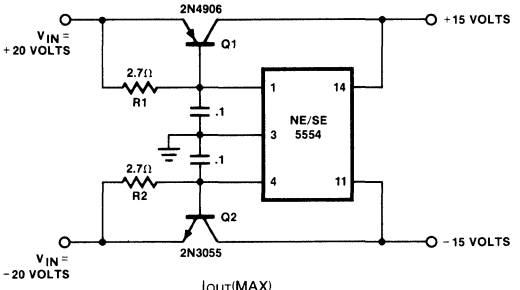
Increasing output above ±15 volts on NE/SE5554

To increase the regulated output above ±15 volts, it is necessary to trim the op amp negative input reference resistor (R_1 in the NE/SE5554 equivalent circuit).

DUAL TRACKING REGULATOR WITH $\pm V_{OUT}$ > 15 VOLTS



HIGH CURRENT DUAL TRACKING REGULATOR



$$\beta(Q) \geq \frac{I_{OUT(MAX)}}{I_{REQ(MAX)}}$$

$$R1 = R2 = \frac{\beta V_{BE}}{I_{REG(MAX)}\,(\beta + 1) - I_{OUT(MAX)}}$$

SECTION 22
INTERFACE CIRCUITS

INTRODUCTION

Large systems are comprised of many different subsystems, all of which must interface to complete the system. All types of circuits, including linear, digital and discrete are often used in the subsystems.

Interface circuits provide the necessary function of tying the parts of a system together. These circuits are usually not purely linear or digital but contain both types of circuit functions. For instance, sense amplifiers are designed for interface between low level memory outputs and bipolar levels, while differential comparators are designed for interface between analog systems and TTL/DTL systems. In general, this section will cover such devices as comparators, sense amplifiers, line drivers/receivers, and display drivers.

CONVERTERS

Digital computers, digital communications, digital instruments and displays have created a demand for low cost reliable converters. Key factors in this demand are:

- The need to communicate with digital computers for processing and storage of analog signals.
- Severe limitations encountered in reliable analog data transmission over any considerable distance.
- The need for more easily readable displays.

General application areas for converters include: Data processing, data transmission, graphics and displays, audio systems, control systems and arithmetic operations.

Specific Applications

Test Systems

- Transistor tester (Force I_B and I_C)
- Resistor matching (Use both outputs)
- Programmable power supplies
- Programmable pulse generators
- Programmable current source
- Function generators (ROM drive)

Arithmetic Operations

- Analog division by a digital word
- Analog quotient of 2 digital words
- Analog product of 2 digital words—squaring
- Addition and subtraction with analog output
- Magnitude comparison of 2 digital words
- Digital quotient of 2 analog variables
- Arithmetic operations with words from different logic families

Graphics and Displays

- Polar to rectangular conversion
- CRT character generation
- Chart recorder driver
- CRT display driver

Data Transmission

- Modern transmitter
- Differential line driver
- Party line multiplexing of analog signals
- Multi-level 2-wire data transmission
- Secure communications (constant power dissipation)

Control Systems

- Reference level generator for setpoint controllers
- Positive peak detector
- Negative peak detector
- Disc drive head positioner
- Microfilm head positioner

Audio Systems

- Digital AVC and reverberation
- Music distribution
- Organ tone generator
- Audio tracking A/D
- Speech compression and expansion
- Audio digitizing and decoding

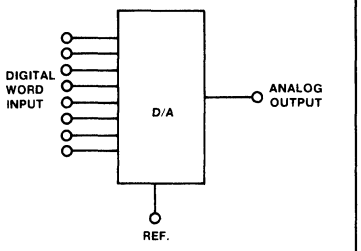
D/A CONVERTERS

D/A converters perform the function of converting a digitally coded signal input into an analog signal output (See Figure 5-1). D/A converters are useful in systems requiring analog signals derived from digital data.

DAC Building Blocks

The actual implementation of a D/A system contains four separate parts: A reference quantity; a set of binary switches to simulate binary coefficients $B_1 \ldots B_N$; a weighting network; and an output summing means.

CONVERSION OF A DIGITALLY CODED SIGNAL INPUT INTO AN ANALOG SIGNAL OUTPUT



Output = Ref. x digital word

$$\text{Output} = \text{Ref.} \times \left(\frac{B_1}{2} + \frac{B_2}{4} + \ldots + \frac{B_N}{2^N}\right)$$

Figure 5-1

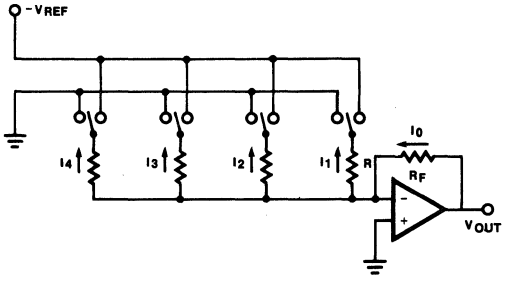
Binary-Weighted Ladder Employing Voltage Switching

The disadvantages of a binary-weighted ladder employing voltage switching include: A wide range of resistor values which are used in weighting the network; and nodal capacitances which are charged/discharged during conversion. See Figure 5-2.

R-2R Ladder Network Employing Current Switching

The advantages of this type of network include: No need for a wide range of resistor

BINARY-WEIGHTED LADDER EMPLOYING VOLTAGE SWITCHING



$$V_{OUT} = \frac{R_F}{R} V_{REF} \times \left(b_1 + \frac{b_2}{2} + \frac{b_4}{4} + \frac{b_8}{8}\right)$$

Figure 5-2

values; and current switching eliminates transients in nodal parasite capacitances. See Figure 5-3.

KEY SPECIFICATIONS

Speed

The conversion process should represent the input signal with the highest fidelity and minimal lag in time (Real time applications).

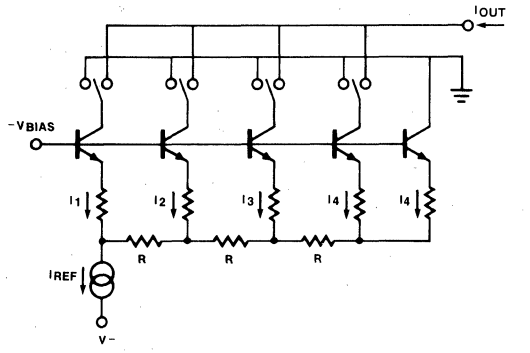
Settling Time

Settling time is a measure of a converter's speed and is defined as the elapsed time after a code transition for DAC output to reach final value within specified limits, usually ±1/2 L.S.B. See Figure 5-5.

Errors

Offset Error —The output voltage of DAC with zero code input. Offset can and usually is trimmed to zero with an offset zero adjust potentiometer. See Figure 5-6.

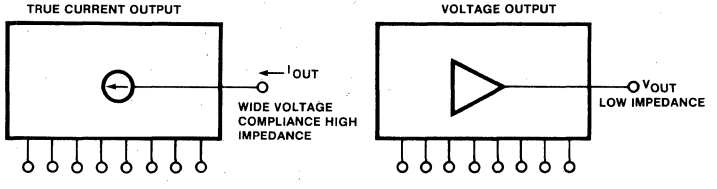
R-2R LADDER NETWORK EMPLOYING CURRENT SWITCHING



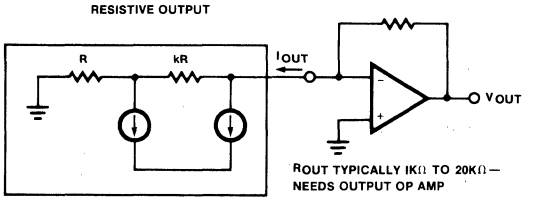
$$I_{OUT} = I_{REF} \times \left(\frac{b_1}{2} + \frac{b_2}{4} + \frac{b_3}{8} + \frac{b_4}{8} \right)$$

Figure 5-3

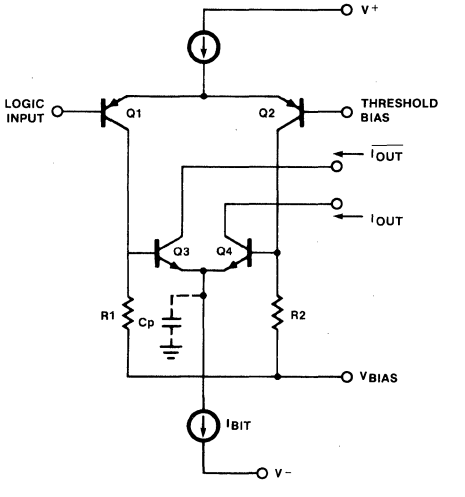
DAC OUTPUT TYPES



a. True Current Output/Voltage Output



b. Resistive Output



c. Complementary High Compliance Current Switch

Figure 5-4

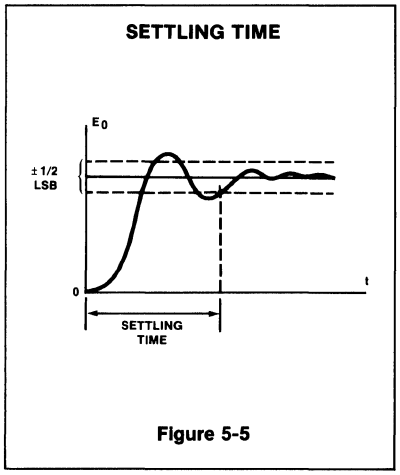


Figure 5-5

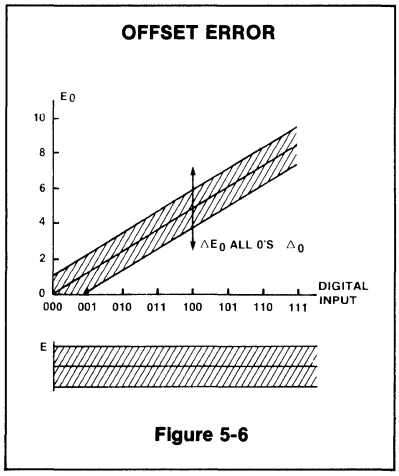


Figure 5-6

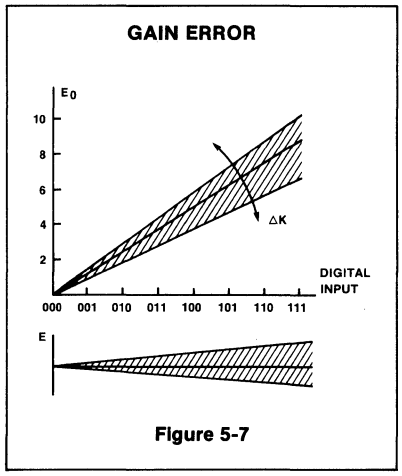


Figure 5-7

Gain Error — Deviation in output voltage from correct level when the input calls for a full scale output. This error may be trimmed to zero. See Figure 5-7.

Relative Accuracy — The maximum deviation of the DAC output relative to an ideal straight line drawn from zero to full scale (1 L.S.B.). See Figure 5-8.

Differential Non-Linearity — Incremental error from any ideal L.S.B. analog output change when the digital input is changed (1 L.S.B.). See Figure 5-9.

Monotonicity — As the input code is incremented from one code to the next in sequence, the analog output will either increase or remain constant. See Figure 5-10.

Stability

Stability is a measure of the independence of converter parameters with respect to variations in external conditions such as temperature and supply voltage.

Temperature Coefficient — The effects of temperature changes of the output. Specified as %F.S. change.

Supply Rejection — Ability to resist changes in the output with supply changes, specified as % full scale change.

PARAMETER	MC1406/7/8	NE5008	NE5009	UNITS
Resolution	8	8	8	Bits
Relative accuracy	.78/.39/.19	0.19	0.1	%
Settling time	300	85	60	ns

Table 5-1
D/A CONVERTER COMPARISON

5007/5008 DAC

Reference Amplifier Setup

The 5007/5008 is a multiplying D-to-A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full scale output current is a

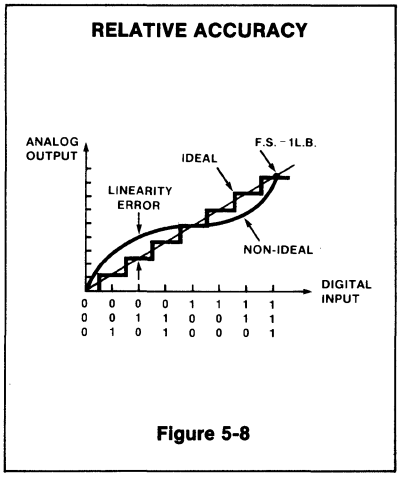


Figure 5-8

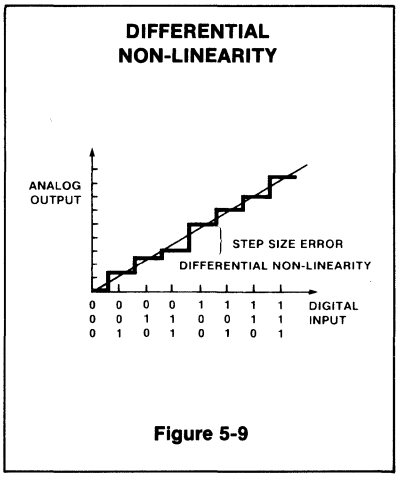


Figure 5-9

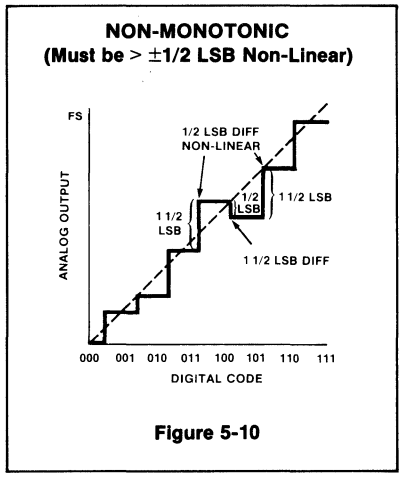


Figure 5-10

linear function of the reference current and is given by this equation where $I_{REF} = I_{14}$.

$$I_{FS} = \frac{255}{256} \bullet I_{REF}$$

In positive reference applications shown in Figure 5-11, an external positive reference voltage forces current through R14 into the V_{REF} (+) terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to V_{REF} (–) at pin 15, shown in Figure 5-12. Reference current flows from ground through R14 into V_{REF} (+) as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier R15 (nominally equal to R14) is used to cancel bias current errors. R15 may be eliminated with only a minor increase in error.

Bipolar references may be accommodated by offsetting V_{REF} or pin 15 as shown in Figure 5-13. The negative common mode range of the reference amplifier is given by the following equation. The positive common mode range is V+ less 1.5V.

$$V_{CM-} = V- + (I_{REF} \bullet 1k\Omega) + 2.5V$$

When a dc reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference R14 should be split into 2 resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications, a + 10.0V reference is recommended for optimum full scale temperature coefficient performance. This will minimize the contributions of reference amplifier V_{OS} and TCV_{OS}. For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R14, or by using a potentiometer for R14. An improved method of full scale trimming which eliminates potentiometer T.C. effects is shown in Figure 5-14.

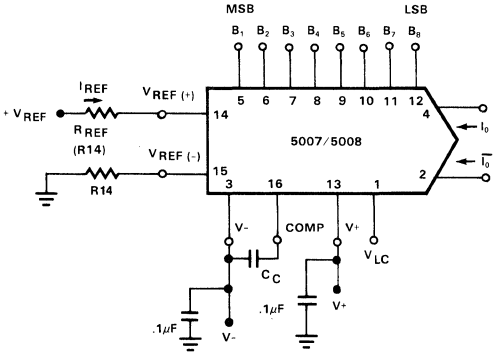
Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common mode range. The recommended range for operation with a dc reference current is +0.2mA to +4.0mA.

The reference amplifier must be compensated by using a capacitor from pin 16 to V–. For fixed reference operation, a 0.01μF capacitor is recommended. For variable reference applications, see section entitled Reference Amplifier Compensation for Multiplying Applications.

Multiplying Operation

The 5007/5008 provides excellent multiplying performance with an extremely linear

BASIC POSITIVE REFERENCE OPERATION

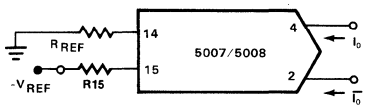


$$I_{FS} \approx +\frac{V_{REF}}{R_{REF}} \times \frac{255}{256} I_O + \overline{I_O} = I_{FS} \text{ for all logic states}$$

For fixed reference, TTL operation typical values are:
V_{REF} = +10,000V, R_{REF} = 5,000Ω R15 ≈ R_{REF},
C_C = 0.01μF, V_{LC} = 0V (ground)

Figure 5-11

BASIC NEGATIVE REFERENCE OPERATION

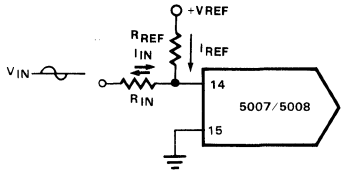


$$I_{FS} = \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

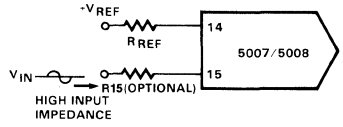
R_{REF} sets I_{FS}, R15 is for bias current cancellation.

Figure 5-12

ACCOMMODATING BIPOLAR REFERENCES



$I_{REF} \geq$ Peak Negative Swing of I_{IN}



+V_{REF} must be above Peak Positive Swing of V_{IN}

Figure 5-13

RECOMMENDED FULL SCALE ADJUSTMENT CIRCUIT

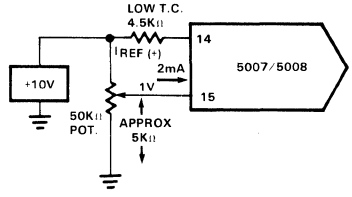


Figure 5-14

relationship between I_{FS} and I_{REF} over a range of 4mA to 4μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 4.0mA. Consult the factory for devices selected for monotonic operation over wider I_{REF} ranges. For better multiplying accuracy see the 5009 data sheet.

Reference Amplifier Compensation for Multiplying Applications

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V-. The value of this capacitor depends on the impedance presented to pin 14. For R14 values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 15, 37 and 75pF. Larger values of R14 require proportionately increased values of C_C for proper phase margin.

PULSED REFERENCE OPERATION

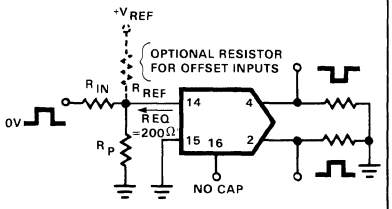


Figure 5-15

For fastest multiplying response, low values of R14 enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the preceding values will suffice and the amplifier must be heavily compensated, which will decrease overall bandwidth and slew rate. For R14 = 1kΩ and C_C = 15pF, the reference amplifier slews at 4mA/μs enabling a transition from I_{REF} = 0 to I_{REF} = 2mA in 500ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme shown in Figure 5-15. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full scale transition (0 to 2mA) occurs in 120ns when the equivalent impedance at pin 14 is 200Ω and C_C = 0. This yields a reference slew rate of 16mA/μs, which is relatively independent of R_{IN} and V_{IN} values.

V_{TH} - V_{LC} vs TEMPERATURE

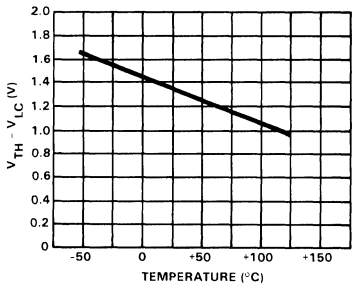


Figure 5-16

Logic Inputs

The 5007/5008 design incorporates a logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2μA logic input current and completely adjustable logic threshold voltage. For V- = -15V, the logic inputs may swing between -10V and +18V. This enables direct interface with +15V CMOS logic, even when the 5007/5008 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by this equation.

$$V- + (I_{REF} \bullet 1k\Omega) + 2.5V$$

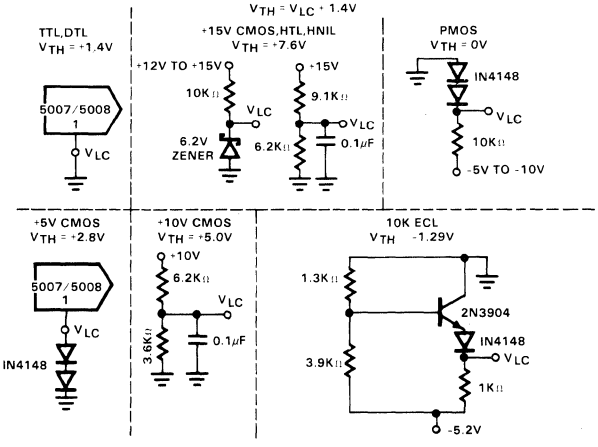
The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control in (pin 1, V_{LC}). Figure 5-16 shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4 above V_{LC}. For TTL and DTL interface, simply ground pin 1. When interfacing ECL, an I_{REF} = 1mA is recommended. For interfacing other logic families, see Figure 5-17. For general setup of the logic control circuit, it should be noted that pin 1 may source up to 200μA. External circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1kΩ divider, for example, it should be bypassed to ground by a 0.01μF capacitor.

Analog Output Currents

Both true and complemented output sink currents are provided, where $I_O + \overline{I_O} = I_{FS}$. Current appears at the true output when a 1 is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a positive logic D-to-A converter. When a 0 is

INTERFACING WITH VARIOUS LOGIC FAMILIES



NOTE

Do not exceed negative logic input range of DAC

Figure 5-17

applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases I_O as in a negative or inverted logic D-to-A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS}. Do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V- and is independent of the positive supply. Negative compliance is given by this equation.

$$V- + (I_{REF} \bullet 1k\Omega) + 2.5V$$

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

Power Supplies

The 5007/5008 operate over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5V or less, $I_{REF} \leq 1mA$ is recommended.

Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range. Consult the various figures for guidance. For example, operation at -4.5V with I_{REF} = 2mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible; however, at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the 5007/5008 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be useful to insure logic swings, etc., remain between acceptable limits.

Power consumption may be calculated by this equation.

$$P_D = (I+)(V+) + (I+)(V-) + (2I_{REF})(V-)$$

A useful feature of the 5007/5008 design is that supply current is constant and independent of input logic states. This is useful in cryptographic applications and further serves to reduce the size of the power supply bypass capacitors.

Temperature Performance

The linearity and monotonicity specifications of the 5007/5008 are guaranteed to apply over the entire rated operating temperature range. Full scale output current drift is low, typically ±10ppm/°C, with zero scale output current and drift essentially negligible compared to 1/2 LSB.

Full scale output drift performance will be best with +10.0V references, as V_{OS} and TCV_{OS} of the reference amplifier will be very small compared to 10.0V. The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full scale drift. Settling times of the 5007/5008 decrease approximately 10% at -55°C and an increase of about 15% at +125°C is typical.

Settling Time

The 5007/5008 is capable of extremely fast settling times (typically 85ns at I_{REF} = 2.0mA). Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35ns for each of the 8 bits. Settling time to within 1/2 LSB of the LSB is therefore 35ns, with each progressively larger bit taking successively longer. The MSB settles in 85ns, thus determining the overall settling time of 85ns. Settling to 6-bit accuracy requires about 65 to 70ns. The output capacitance of the 5007/5008 including the package is approximately 15pF. Therefore the output RC time constant dominates settling time if RL > 500Ω.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 1.0mA, with gradual increases for lower I_{REF} values. The principal advantage of higher I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±4μA. Therefore a 1kΩ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture of Figure 5-18 uses a cascode design to permit driving a 1kΩ load with less than 5pF of parasitic capacitance at the measurement node. At I_{REF} values of less than 1.0mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 01111111 to 10000000

SETTLING TIME MEASUREMENT

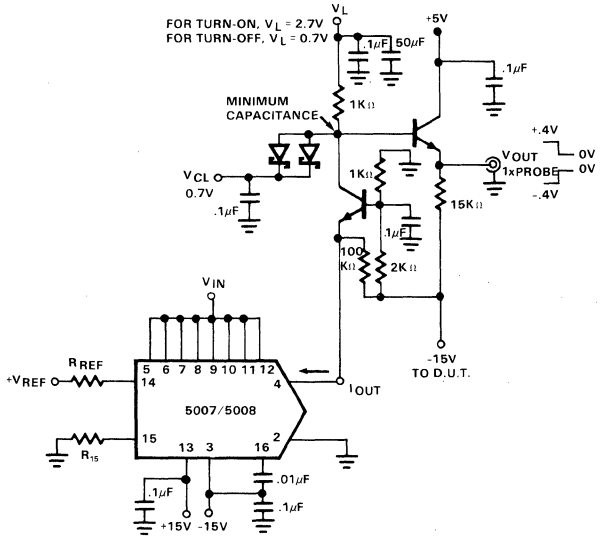


Figure 5-18

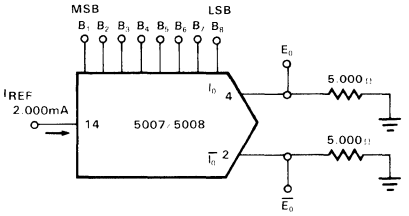
provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value; thus, settling time may be observed at lower values of I_{REF}.

The 5007/5008 switching transients or glitches are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is dependent of input logic states. 0.1μF capacitors at the supply pins provide full transient performance.

TYPICAL APPLICATIONS

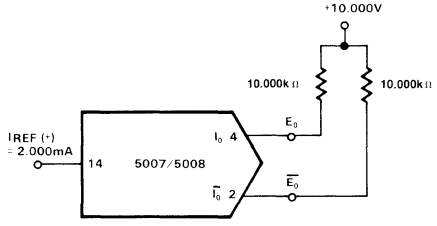
BASIC UNIPOLAR NEGATIVE OPERATION



	B1	B2	B3	B4	B5	B6	B7	B8	I_OmA	$\bar{I}_O$mA	E_O	$\bar{E}_O$
Full scale	1	1	1	1	1	1	1	1	1.992	000	-9.960	.000
Full scale - LSB	1	1	1	1	1	1	1	0	1.984	.008	-9.920	-.040
Half scale + LSB	1	0	0	0	0	0	0	1	1.008	.984	-5.040	-4.920
Half scale	1	0	0	0	0	0	0	0	1.000	.992	-5.000	-4.960
Half scale - LSB	0	1	1	1	1	1	1	1	.992	1.000	-4.960	-5.000
Zero scale + LSB	0	0	0	0	0	0	0	1	.008	1.984	-.040	-9.920
Zero scale	0	0	0	0	0	0	0	0	.000	1.992	.000	-9.960

Figure 5-19

BASIC BIPOLAR OUTPUT OPERATION

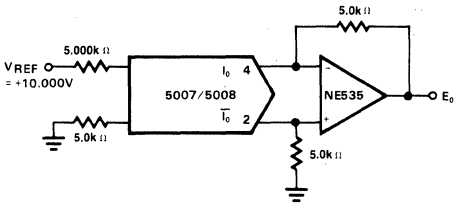


	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\bar{E}_O$
POS full scale	1	1	1	1	1	1	1	1	-9.920	+10.000
POS full scale - LSB	1	1	1	1	1	1	1	0	-9.840	+9.920
Zero scale + LSB	1	0	0	0	0	0	0	1	-0.080	+0.160
Zero scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero scale - LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg full scale + LSB	0	0	0	0	0	0	0	1	+9.920	-9.840
Neg full scale	0	0	0	0	0	0	0	0	+10.000	-9.920

Figure 5-20

TYPICAL APPLICATIONS (Cont'd)

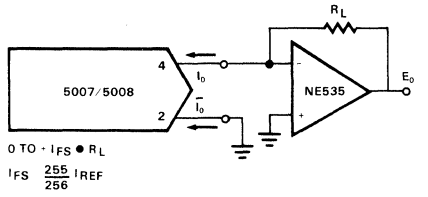
SYMMETRICAL OFFSET BINARY OPERATION



	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	E_O
POS full scale	1	1	1	1	1	1	1	1	+9.920
POS full scale - LSB	1	1	1	1	1	1	1	0	+9.840
(+) Zero scale	1	0	0	0	0	0	0	0	+0.040
(–) Zero scale	0	1	1	1	1	1	1	1	-0.040
Neg full scale + LSB	0	0	0	0	0	0	0	1	-9.840
Neg full scale	0	0	0	0	0	0	0	0	-9.920

Figure 5-21

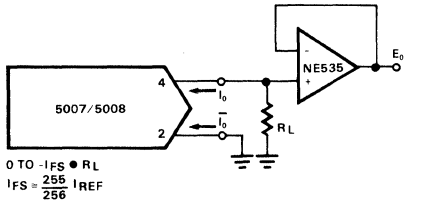
POSITIVE LOW IMPEDANCE OUTPUT OPERATION



For complementary output (operation as negative logic DAC), connect inverting input of OP-amp to I_O (pin 2), connect I_O (pin 4) to ground.

Figure 5-22

NEGATIVE LOW IMPEDANCE OUTPUT OPERATION



For complementary output (operation as a negative logic DAC), connect non-inverting input of OP-amp to I_O (pin 2); connect I_O (pin 4) to ground.

Figure 5-23

LOW COST 8-BIT 1 MICROSECOND A-TO-D CONVERTER

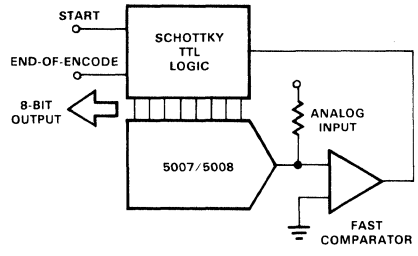
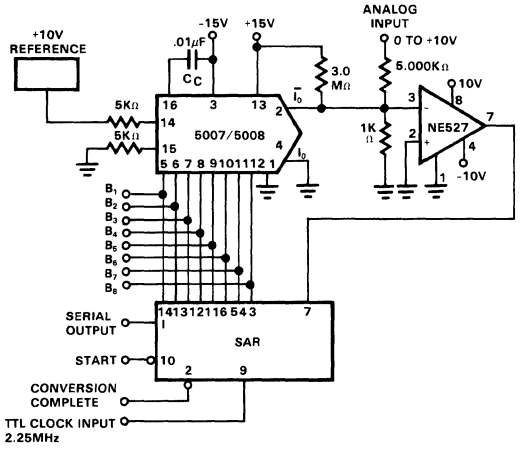


Figure 5-24

3 IC LOW COST A-TO-D CONVERTER

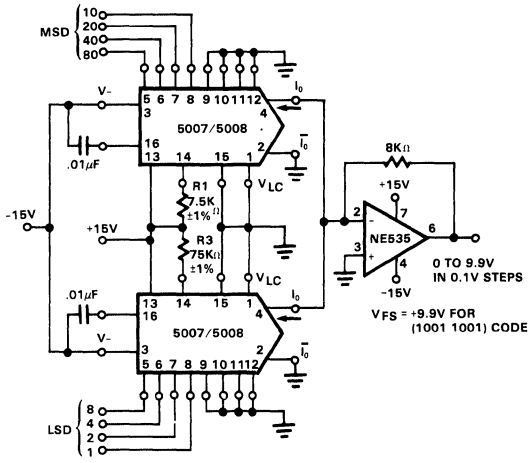


NOTE

Connect "start" to "conversion complete" for continuous conversions.

Figure 5-25

LOW COST 2-DIGIT BCD DAC

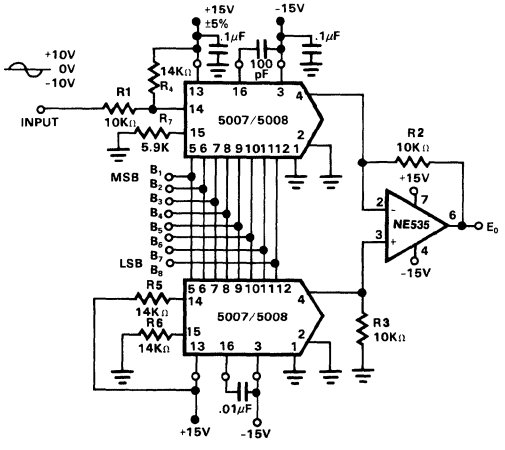


NOTE

Output is directly proportional to positive power supply.

Figure 5-26

DC-COUPLED DIGITAL ATTENUATOR/ PROGRAMMABLE GAIN AMPLIFIER



Bipolar input offset binary output } Performs 2 quadrant multiplications—AC input controls output polarity.

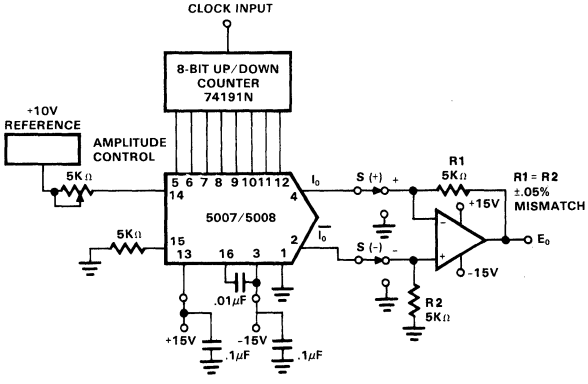
NOTES

1. R1 = R2 = R3
2. R4 = R5
3. E_O DC to 20KHz = ±5V
4. E_O DC to 10KHz = ±10V

Figure 5-27

HIGH SPEED WAVEFORM GENERATOR

OUTPUT TYPE (EO)	SWITCH S(+)	CONDITIONS S(-)
Unipolar positive	+	GND
Unipolar negative	GND	-
Bipolar	+	-



NOTES

1. Bipolar output is symmetrical around zero, adjustable peak to peak amplitude.
2. For triangle wave, count up to full, reverse and count down.
3. For positive-going sawtooth, count up to full, clear, repeat.
4. For negative-going sawtooth, count down, clear, repeat.
5. For other waveforms, use a ROM programmed with the desired function.

Figure 5-28

A/D CONVERTER CIRCUITS

Conversion schemes usually fall into one of two categories:

D/A Feedback A/D Converters

a. Digital ramp (Counting)
b. Tracking (Up-down)
c. Successive approximation*

Integrating A/D Converters

a. Single slope
b. Double slope
c. Triple slope*

Indirect Schemes

Feedback Methods

- Very fast
- Accurate
- Good differential linearity
- Constant conversion time

Integrating Methods

- Slow conversion time
- Accurate
- Excellent differential linearity
- Excellent rejection of high frequency noise
- Fixed averaging period, but variable conversion time

CONSIDERATIONS FOR A/D CONVERTERS

- Analog input signal range and resolution required
- Linearity requirement and stability
- Conversion speed required
- Monotonicity requirement: Can missing codes be tolerated?
- Character of input signal: Is it noisy, sampled, filtered, slowly varying?
- Transfer characteristics (Type of coding)

A/D CONVERTER TERMS

Resolution

Resolution is the input change required to increment the output between the two adjacent codes. This term also refers to the number of bits in the output word and; hence, the number of discrete output codes the input analog signal can be broken into. Expressed in "bits" resolution.

Transfer Characteristic

The Transfer Characteristic is the relationship of the output digital word (code) to the input analog signal, i.e., Binary, BCD.

Conversion Speed

The Conversion Speed is the speed at which an ADC can make repetitive data conversions.

Quantizing Error

Quantizing Error is an inherent error in the conversion process due to finite resolution (discrete output). See Figure 5-29.

Offset Error

An Offset Error is shown in Figure 5-30.

Gain Error

A Gain Error is shown in Figure 5-31.

Relative Accuracy

Relative Accuracy is the deviation of an actual bit transition from the ideal transition value at any level over the range of the ADC (% F.S.). See Figure 5-32.

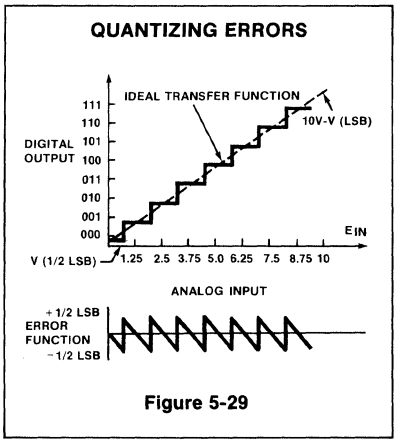


Figure 5-29

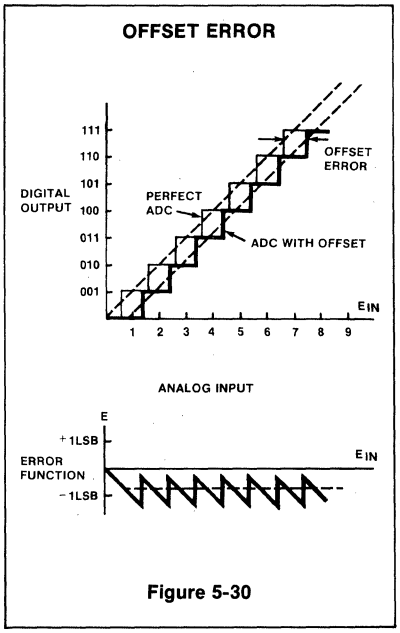


Figure 5-30

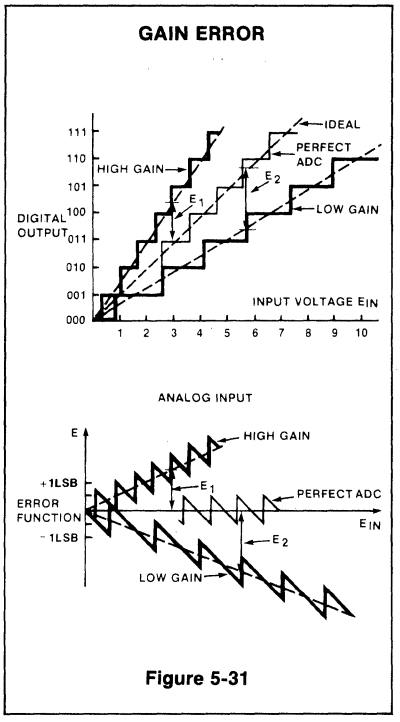


Figure 5-31

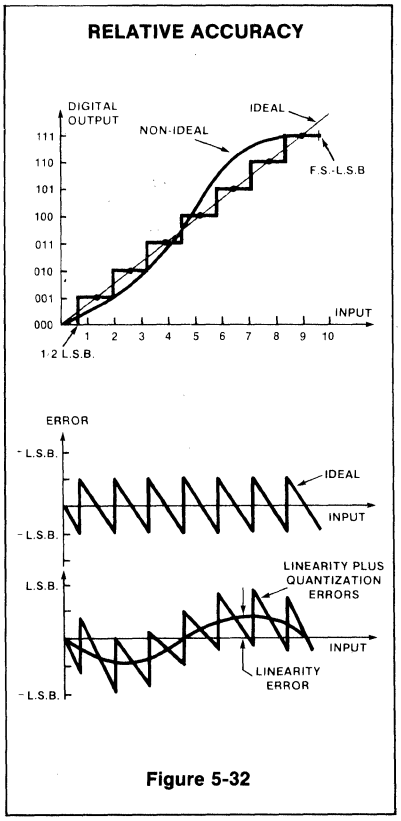


Figure 5-32

Hysteresis Error

A Hysteresis Error is the code transition voltage dependence relative to the direction from which the transition is approached.

Monotonicity

Monotonicity is when the output code either increases or remains the same for increasing analog input signals. The opposite is true in the reverse direction.

Missing Codes

A Missing Code is a code combination that is skipped. See Figure 5-33.

*Converter schemes used at Signetics

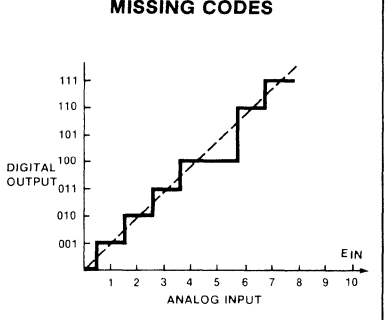


Figure 5-33

INTRODUCTION

The advent of MSI digital logic has made feasible the digital display at a reasonable cost with virtually all instrumentation now taking that course. The key features of digital displays are ease of readability and high reliability.

SEVEN SEGMENT DISPLAYS

Seven segment displays are used for many types of applications. These applications include:

Instruments (Industrial)

- Voltmeters
- Frequency Counters
- Digital Thermometers
- Medical Equipment
- Process Control Equipment
- Avionic Displays

EDP and Minicomputer

- POS Terminals
- Calculators
- Misc. EDP Peripheral Equipment, e.g., Tape Drivers
- Accounting Machines

Consumer

- Automotive—Dashboard Indicators
- Appliances—Ranges, Clocks
- Audio—Digital Tuning
- Games

The most popular and commonly used of the various display technologies are:

- Liquid Crystal Displays (LCD)
- Light-Emitting Diodes (LED)
- Gas-Discharge
- Fluorescent
- Incandescent

The choice of which technology to be used is often dictated by the system constraints, such as:

- Cost
- Size
- Readability (Ambient light)
- Operating Temperature Range
- Reliability
- Power and Supply Limitations
- Ability to be Multiplexed

LIGHT-EMITTING DIODES (LEDs)

LED displays have taken over an appreciable part of the display market, primarily due to:

- High Reliability
- Long Life
- Fast Response Time
- Low Operating Voltage
- Ease in Interfacing

GAS DISCHARGE DISPLAYS

Gas discharge displays have several advantages over LEDs, LCDs and other displays in the applications area. These advantages are generally in products where performance, rather than cost, is of prime importance. These advantages include:

- Larger Digits
- Increased Readability in Bright, Ambient Light
- High Reliability
- Operation in Wide Temperature Extremes

Applications for Gas Discharge Displays

Automotive Industry

- Operating temperature range (-40°F to +120°F)
- LCDs—Freeze at lower temperature
- LEDs—Poor efficiencies at high temperature

Avionics

- Visibility
- LCDs—Difficult to multiplex (Poor response)
  Poor operating temperature range
  Need direct light
- LEDs—Poor visibility in bright light

Games

- Size and Brightness
- LCDs—Poor viewing angle
- LEDs—Not bright enough

NE580 BAR GRAPH DRIVER

Bar-graph System Operation

The bar-graph display is a thick-film planar, gas discharge device. The principal of operation is called self-scan™, in which a neon glow-discharge is propagated from one cathode spot to another under one anode. The bar-graph device appears as a series of cathode bars arranged in a column. A glow discharge is continually propagated along the column from a keep-alive cathode at one end. Provided the scan rate for a whole column is above the eye flicker detection rate, then the glow appears as a continuous column of light.

Bar-graph Signal Requirements

The NE580 comprises most of the electronic components necessary to interface an analog voltage level to the bar-graph display. Each column of the display requires an anode control signal and each cathode (usually from 4 to 7 in number) requires an interlaced logic signal of 1/N duty cycle (where N is the number of cathode phases). The pulse width of each cathode signal is of the order of 50 to 100μs. The cathode signals clock continuously throughout the frame period. The anode signal is on only for a proportion of time corresponding to the input voltage.

$$\text{Thus} \quad V_{IN} = V_{REF} \times \frac{T_{AN}}{200}$$

for a 200 element device, where T_{AN} is the number of cathode clock cycles for which the anode is on Figure 5-35 illustrates the relative output phasing of the linear ramp cathode and anode lines for 5 phase operation.

Circuit Operation

The NE580 provides the circuitry to generate all these signals to the point where they drive the high voltage display elements. An on-chip clock generator drives the master counter and cathode phase generator.

The clock also gates a constant current source which charges the ramp capacitor with a staircase waveform of equal increment steps. These steps correspond to the cathode segments. There are two steps per

BLOCK DIAGRAM

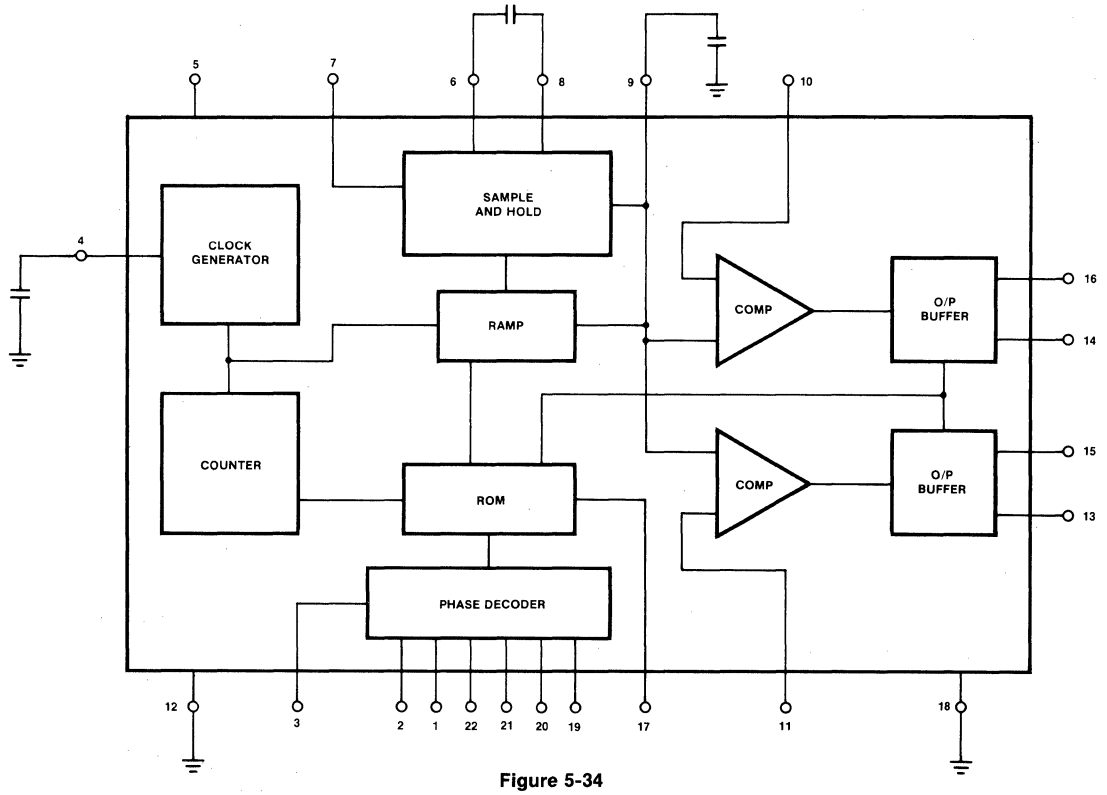


Figure 5-34

RELATIVE OUTPUT PHASING

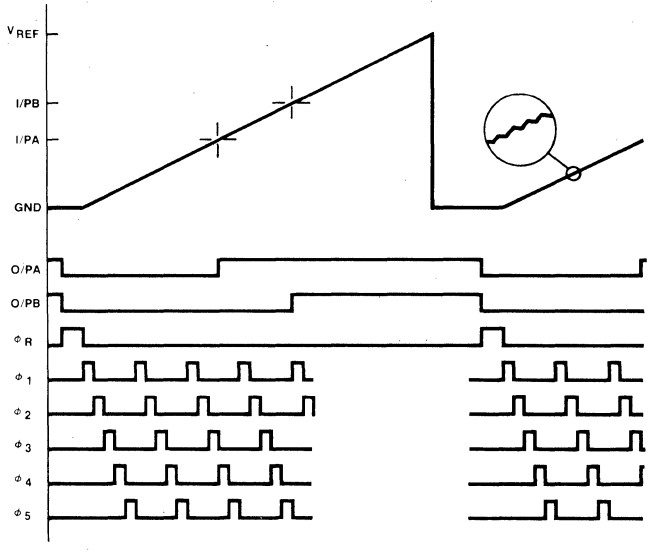
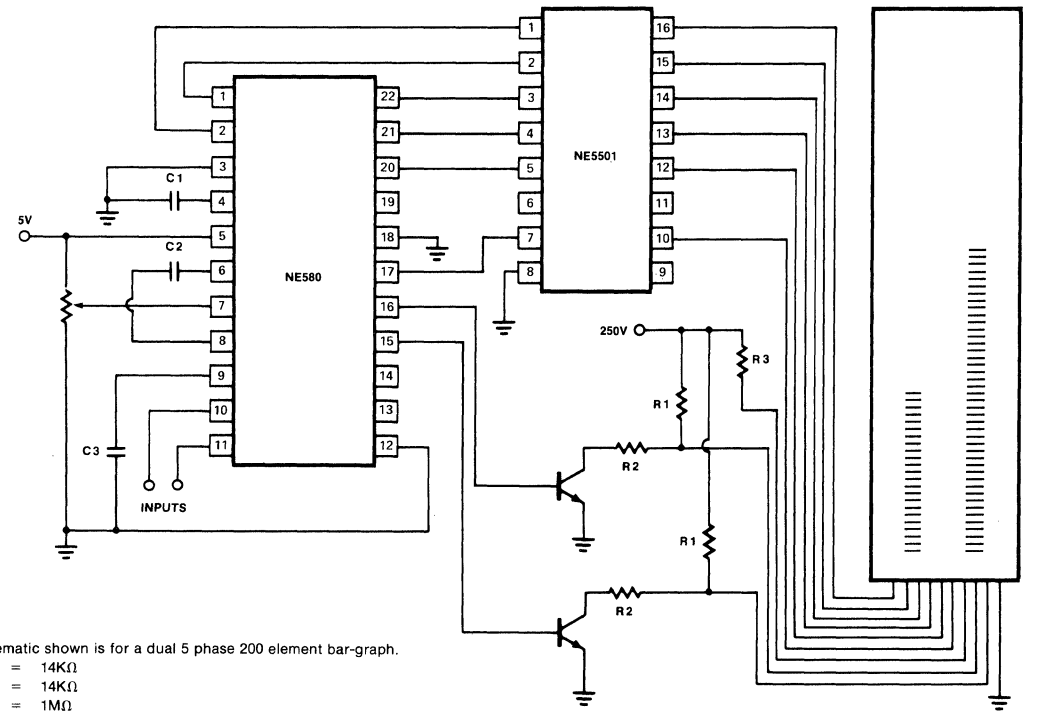


Figure 5-35

APPLICATION



NOTES

1. Schematic shown is for a dual 5 phase 200 element bar-graph.
2. R1 = 14KΩ
   R2 = 14KΩ
   R3 = 1MΩ
   C1 = 0.022μF
   C2 = 0.47μF
   C3 = 0.47μF

Figure 5-36

segment so that the comparison of input voltage with respect to the ramp is made at the mid-point of each segment. The master counter inhibits the current source and discharges the ramp after 200 cathode counts. At the 200th count, the ramp voltage is strobed into a sample-and-hold amplifier. This voltage is compared with the reference voltage and a signal fed back to the ramp constant current source. Hence, the maximum value of the ramp will be adjusted to the same level as the reference voltage.

NE584/585 GAS DISCHARGE DISPLAY DRIVERS

Introduction

The NE584 and NE585 Gas Discharge Display Drivers find wide application in driving displays such as Burroughs Panaplex II, Cherry Plasma-Lux, Beckman SP, etc. They feature high reliability, simplicity in interfacing, programmable segment current, and internal feedback. External components required include a resistor used in programming the segment currents, and a capacitor used in limiting anode bus voltage variations. The purpose of this application note is to supply the designer with the information necessary to design systems based on these drivers.

Selection of Program Current Resistor

The NE584, available in either an eight or nine channel unit, drives the cathodes of the displays. Segment drive current, a factor in determining the brightness of the display, is set on all channel outputs simultaneously by selection of a single resistor.

Currents may be programmed up to 3mA (in the internal feedback mode) and up to 5mA (when using external feedback or no feedback). Component values may be selected using Figure 5-37.

Selection of Feedback Capacitor

The NE584 and NE585 may be operated with or without feedback. The feedback mode may be controlled internally or externally. When using external feedback current, capabilities of the drivers are extended as a result of eliminating the power dissipation in the internal feedback network which is a current limiting factor. Also certain system timing conditions may make it necessary to operate in this mode because of improper feedback operation. Operating in the feedback mode offers consistency of operation under conditions such as supply voltage variations, temperature variations blanked leading zeros, variations in display panel ionization voltage, component tolerances, etc.

When operating in the feedback mode, a capacitor is required to limit variations on the anode bus. This prevents the cathode

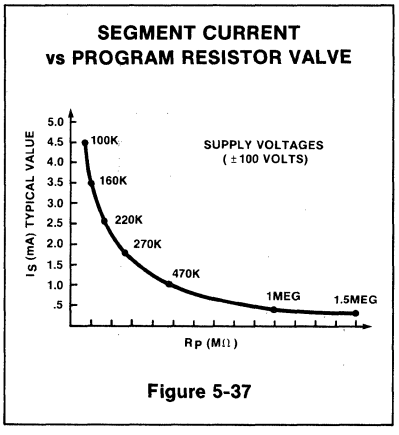


Figure 5-37

output from going into saturation causing feedback current to flow and anode bus voltages to be higher than required. Selection of this capacitor is mainly determined by the cathode pulse width and by the segment currents and may be selected using Figure 5-38.

Interface Considerations
Input Requirements

Driver inputs may be directly interfaced with TTL, MOS, and C-MOS logic families. Each of these logic families will provide enough drive to fully enable the driver outputs.

Unused inputs should not be grounded. They should be left open to prevent loading of selected inputs.

Single Supply Operation

Because of the increased external component count, single supply operation is usually not recommended. If it is necessary to operate in this mode, all voltage levels must be shifted by 1/2 the supply voltage. For example:

PIN	Split Supply ±100 volts	Single Supply +200 volts
V_1	5 to 15 volts	105 to 115 volts
V_2	-100 volts	0 volts
V_3	+100 volts	+200 volts
GND	0 volts	+100 volts

The input levels must also be shifted. One method of accomplishing this is shown in Figure 5-39.

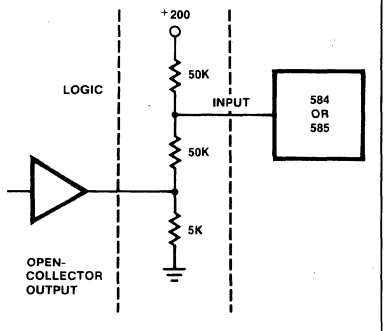


Figure 5-39

Pull-Up Option

When operating the drivers at fast scanning rates, the turn-off time of the display may become a limiting factor. This may become noticeable when operating with a 5 volt supply (V_1).

The pull-up option is provided on the segment driver and is used to decrease turn-off delays by allowing charge to be removed more quickly from the cathodes and from stray capacitance. This is accomplished by grounding this pin, which increases the drive current to the pull-up network.

Cathode Pull-Up Resistors

When driving long cables, it is helpful, as with all drivers, to add an external pull-up resistor from the output of the cathode driver to ground. The value of this resistor is in the range of 1 Meg, placed close to the display, and allows charge to be removed more rapidly from both the display and from the cable.

Timing Considerations and Feedback

A number of system requirements and panel parameters must be considered in making a decision as to what constraints should be imposed on cathode and anode signals and on selecting the frame rate. The two driver modes of operation require different timing constraints—each mode offering its own unique advantages. Feedback Mode-Variations in both ionization voltages from panel-to-panel as well as from digit-to-digit within the same panel and in the supply voltages, make it advantageous to float the anode bus and make it self compensating for such variations. This is accomplished by the use of a current feedback scheme and imposes constraints on both the duration and relative timing of the driver input signals.

The feedback scheme is relatively simple—whenever an input is applied to the cathode driver and the display has not yet ionized the coincidence of this condition is sensed by the cathode driver and a current pulse is sent along the feedback link to the digit driver. The amplitude of this pulse is proportional to the program current and to the number of segment inputs selected. Its duration is equal to the ionization time or to the duration of the segment pulse input—the shorter of the two. This current pulse is sensed by the digit driver, amplified, and is used to charge the feedback capacitor. This results in an increase in the voltage level of the anode bus.

Once the display is ionized, a current must be supplied by the anode bus for the duration of the cathode input. The cathode driver, which functions as a constant current sink, senses this current and terminates the feedback current pulse. Once feedback current has ceased, the feedback capacitor begins to discharge lowering the anode bus voltage. The average voltage level on the anode bus is stabilized when the charge entering the anode bus during the ionization time equals the charge leaving the bus during on-time of the display, cathode pulse duration minus the ionization time. This level is defined by the supply voltage and display panel parameters and is self compensating since the anode bus voltage is directly related to the ionization time and the ionization time inversely related to the anode bus voltage.

The following constraints are unique to the feedback mode of operation.

1-a A digit input should always be selected before or at the same time that one or more segment inputs are selected and remain on for the duration of the segment inputs or longer.

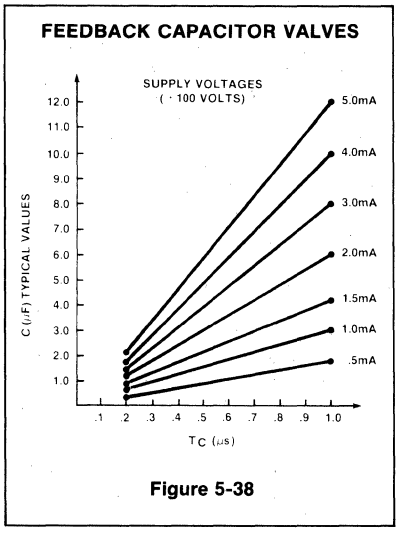
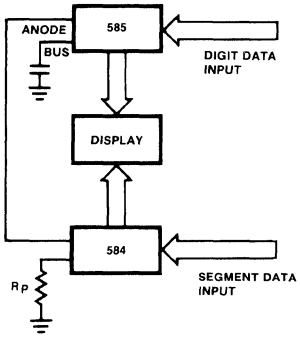


Figure 5-38

TYPICAL APPLICATIONS

FEEDBACK MODE

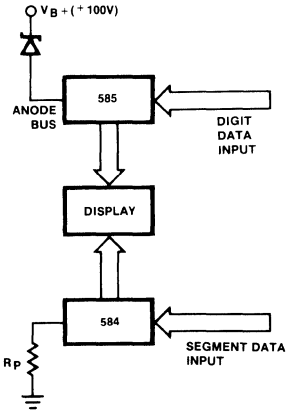


NOTES

(a) Feedback pins connected together.
(b) Segment current set by R_P and limited to 3mA.
(c) Capacitor connected to anode bus to provide feedback.

Figure 5-40

NON-FEEDBACK MODE

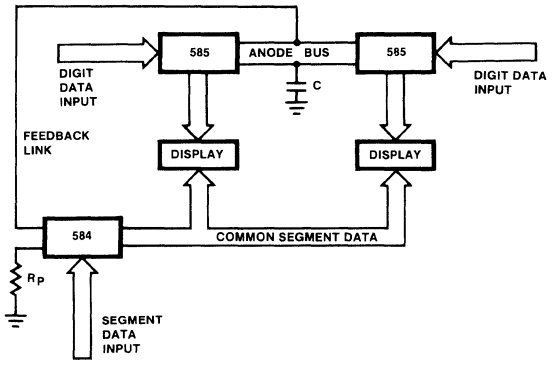


NOTES

(a) Feedback pins left open.
(b) Segment current set by R_P and limited to 5mA.
(c) Anode bus connectd to V_3 supply (+100 volts) through zener diode (15-20 volt range) and maintains anode bus at a constant voltage.

Figure 5-41

MULTIPLE ANODE DRIVER SINGLE CATHODE DRIVER

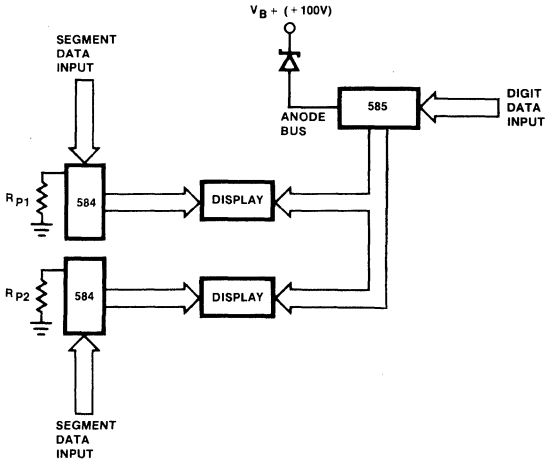


NOTES

(a) Digits are multiplexed (only one digit on at any given time).
(b) Feedback pins are connected together.
(c) Anode bus pins are connected together and a single feedback capacitor used.
(d) Max segment current should be limited to 5mA.
(e) If displays with different parameters are used, it may be necessary to operate the system in the non-feedback mode. This may be accomplished by leaving all feedback pins open connecting the anode bus pins together and connecting a single zener diode of the proper power and current rating to the $-V_3$(+100 volts) supply.

Figure 5-42

MULTIPLE ANODE DRIVER SINGLE CATHODE DRIVER CONFIGURATION



NOTES

(a) Displays are multiplexed in parallel. (Each anode driver output selects two digits—one from each display).
(b) Segment currents may be set independently by R_{P1} and R_{P2} and the total should not exceed 5mA.
(c) All feedback pins are left open.
(d) Anode bus pin connected to the V_3 supply (+100V) through a zener diode 20 volt (15-20 volt range) and maintains a constant voltage as the anode voltage.

Figure 5-43

1-b Blanking should be accomplished by inhibiting segment inputs or both segment and digit inputs.

2. For large cathode pulse widths combined with high segment currents, it is recommended that the non-feedback mode be used a result of limitations on the magnitude of the feedback current and on power dissipation. If any of the constraints are not met, then the non-feedback mode of operation should be used.

The following constraints are common to both modes of operation.

1. Adequate blanking should be used when scanning digits sequentially to inhibit adjacent digit arcing. Interlacing of digits may be used to eliminate the necessity for such blanking, but this in many cases will require a greater amount of hardware. Typical blanking time would range between 10-20% of total digit time.

2. Minimum pulse widths for the segment inputs should be typically greater than 200μs so that variations in ionization time do not cause brightness variations in displays.

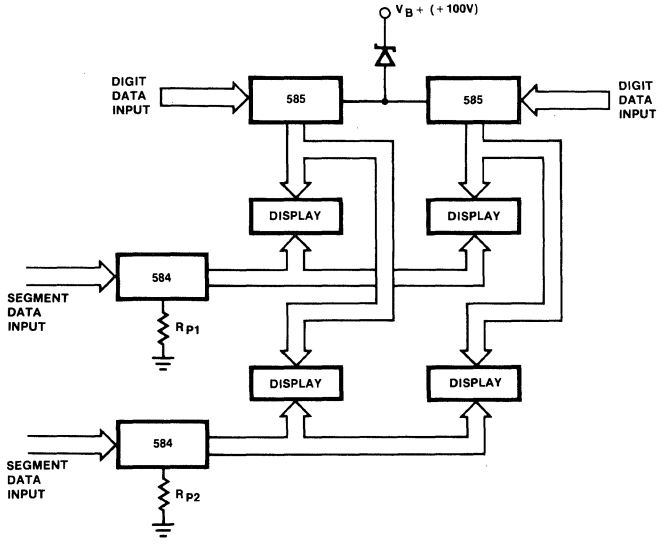
3. Scanning rate should be greater than 50Hz to prevent flickering of display.

4. Brightness of the display is directly proportional to the segment current level and to the cathode input pulse width. Typically, the brightness may be varied over a 3:1 range by variation of segment current and over a 10:1 range by variation of cathode pulse width. Both ranges are dependent on display parameters.

CONCLUSION

The switching of the high voltages necessary for display panels has long presented difficulties to the semiconductor industry—particularly to the IC manufacturers. Signetics now makes available a driver set capable of switching these high voltages with high reliability and ease in interfacing. Flexibility in configuring systems and small external component count, together with internal feedback and programmable segment current capabilities is why Signetics drivers find such wide applications in terminals, calculators, clocks, electronic games, instrument, cash registers, and medical equipment.

MULTIPLE ANODE AND CATHODE DRIVER CONFIGURATION



NOTES

(a) Extension to the concepts presented in Figure 5-42 and 5-43. Non-feedback mode employed.

(b) Segment currents independently set and their sum limited to 5mA.

Figure 5-44

APPENDIX A

DRIVER-INTERCONNECTION DIAGRAM

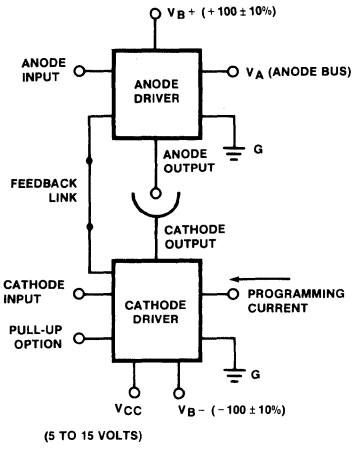


Figure 5-46

APPENDIX B

NE584/585 Digital Clock Application

The system operates in the non-feedback mode. A 15V zener diode maintains the anode bus at +85 volts which allows for variations in display panel ionization voltage. Display segment current is programmed by R1 and is set at 5mA to allow maximum brightness. No other external components are required for interfacing.

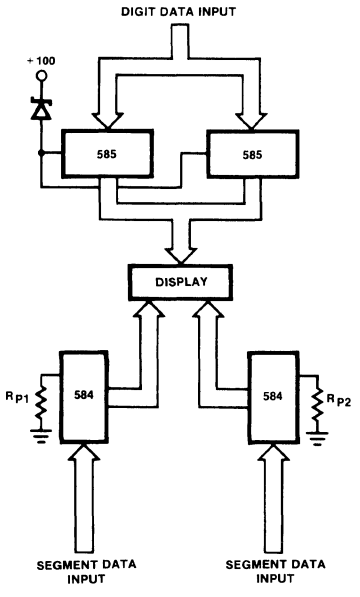
DESCRIPTION OF OPERATION

A three position brightness control is provided as well as a blanking switch. When in the blanking mode of operation the clock operates in a normal manner, but the display is blanked. Controls are provided for setting the time. The hours digit will be advanced by depressing S2. Minutes may be advanced in ten minute increments by depressing S3 and in one minute increments by depressing S2 and S3 simultaneously. A count inhibit switch is also provided which will allow setting of seconds.

A snooze alarm feature may be added by adding additional switches which allow the following pins in the Mostek chip to be connected to +15 volts. Pin (12) alarm enable, Pin (15) alarm set, Pin (11) snooze. In the alarm set mode the alarm time is displayed and may be set. The snooze feature will temporarily turn off an activated alarm for ten minutes.

An output tone, available at Pin (13), is in the range between 400-600Hz and when buffered is used to drive a speaker.

PARALLEL INPUT DIGIT DRIVER OUTPUTS



NOTES

(a) Corresponding inputs and outputs on each digit driver are connected together directly.
(b) Non-feedback mode is used.
(c) Max segment current should be limited to 5mA on each cathode driver and digit current limited to 60mA where $I_D = \Sigma I_S$.
(d) Separate zener diodes may be used to decrease power ratings, but a single diode may also be used and the anode bus pins tied together.
(e) Extended current capability of the 585 is increased to 60mA.

Figure 5-45

COMPARATORS

Voltage comparators are high gain differential input—logic output devices. They are specifically designed for open loop operation with a minimum of delay time. Although variations of the comparator are used in a host of applications, all uses depend upon the basic transfer function of Figure 5-49. As shown device operation is simply a change of output voltage dependent upon whether the signal input is above or below the threshold input. The threshold in this example is 0 volts.

Comparator inputs are customarily marked with plus or minus signs to indicate their polarity. For example the circuit of Figure 5-50 produces a logic 1 level when the non-inverting input is more positive than the reference voltage.

DEFINITIONS

Many similarities exist between operational amplifiers and the amplifier section of voltage comparators. In fact op amps can be used to implement the comparator function at low frequencies.

Thus, the characteristic definitions presented here are similar to those reviewed for op amps in Section 3.

Input Offset Voltage

As with operational amplifiers the non-ideal comparator possesses some offset voltage. The definition differs slightly in that the output structure of comparators is digital rather than linear. Hence, input offset voltage is defined for comparators as the dc voltage required at the input to force the output to the logic threshold of ensuing devices (1.2 volts for TTL).

Input Offset Current

Imbalances of input bias current arise from small variances of the junction geometry of the differential input amplifier. As for op amps, the imbalance is referred to as input offset current.

Bias Current

As with op amps the input structure of comparators is usually a differential bipolar stage. Hence, the average input current required defines bias current.

Common Mode Range

When specifying voltage comparators one of the key parameters is common mode range, which is defined as the range of voltages over which both inputs can be varied simultaneously without abnormal output voltage transitions. This parameter must be kept uppermost in the designer's mind because the reference and signal voltages become common mode signals at threshold. All ranges of input signals thus must be within the common mode range of the input amplifier.

Voltage Gain

Specifications of voltage gain refer to the overall gain of the device, the bulk of which occurs in the amplifier section.

In general higher gains would be advantageous for resolving smaller input signals. Of course the propagation delay suffers due to the more severe saturation of the transistors. Typical gains for TTL output devices are set for 5000 volts per volt. This gain provides 5 volts of output swing with 1mV

DRIVER INTERFACING

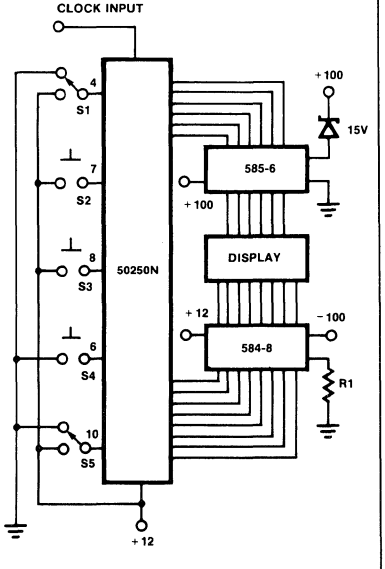


Figure 5-47

POWER SUPPLY DIAGRAM

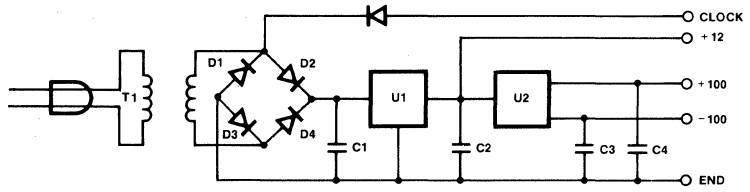


Figure 5-48

input signal change for reasonable accuracy but does not contribute severely to the overload recovery delay.

Propagation Delay

Voltage comparisons of analog signals with a reference voltage usually require that the operation take as little time as possible. Long delays in the comparator cause a pulse position error at the output since the analog signal in the meantime has changed value. At low frequencies the delay is of small consequence but at higher frequencies, transit time becomes intolerable. Design of voltage comparator devices includes as a prime goal, the minimizing of transit times.

Propagation delay testing is done under worst case conditions. The recovery from saturation varies depending upon the initial state of the amplifier and the overdrive. Worst case conditions begin applying a 100mV signal on the reference terminal. With no signal applied the amplifier is in saturation in one direction. A step input pulse on the signal line of 100mV $\pm$ V_{OS} will bring the amplifier to a threshold level. Propagation delay at this point is undefined since the output has not switched.

To attain output switching a small overdrive is necessary. Propagation delay is tested in a configuration such as Figure 5-51. The input is a step function of 100mV plus a specified excess or overdrive signal. This causes the amplifier to be exercised from saturation in one direction to saturation in the other for worst case propagation delay. Note that larger overdrive improves delay time as can be seen in Figure 5-52. An overdrive of 5mV causes 12ns delay, whereas a 100mV overdrive improves transit time to only 6ns.

526 TRANSFER FUNCTION

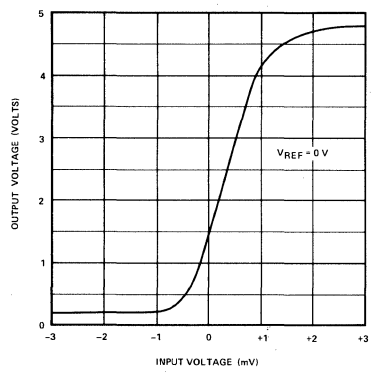


Figure 5-49

BASIC COMPARATOR CIRCUIT

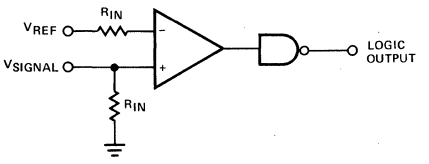


Figure 5-50

If the measurement were made without initial saturation (less than 100mV V threshold) the delay time would be smaller, due to the smaller storage times of unsaturated transistors.

STATE-OF-THE-ART

Comparator design has always been optimized for four basic parameters. They are:

1. High Speed
2. Wide Input Voltage Range
3. Low Input Current
4. Good Resolution

Unfortunately these four parameters are not compatible. For instance gain and input current can be improved by using thinner diffusions for higher beta, but only at the expense of input voltage range. Higher gain also means higher saturation for an increase in delay time. So it becomes obvious that comparators such as the 526 were designed with the best compromises in mind using standard processing.

One method of improving overall response adds gold doping to the processing flow. The gold dopant causes a decrease in minority carrier lifetime which aids the recombination process and shortens the saturation recovery time. Unfortunately the transistor beta is adversely affected by gold causing slightly higher bias and offset currents.

PROPAGATION DELAY TEST SETUP

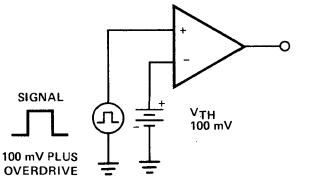


Figure 5-51

It was not until the advent of the Schottky clamp that a vast improvement in speed without input degradation was possible. A very familiar term in the semiconductor industry, the Schottky barrier diode's (SBD) location is illustrated in Figure 5-53.

The Schottky clamped transistor is formed by parallelling the Schottky diode with the base-collector junction of the npn transistor. Without the clamp, as base drive is increased the collector voltage falls until hard saturation occurs. At this point the collector voltage is very near the emitter

RESPONSE TIME FOR NE/SE521 COMPARATOR FOR VARIOUS INPUT OVERDRIVES

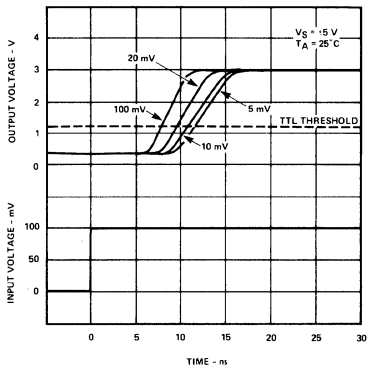


Figure 5-52

voltage, and stored charges in the junctions causes slow recovery from saturation after base drive has been removed. The forward voltage drop of the Schottky diode is 0.4 volts—less than the forward drop of silicon diodes. This difference in forward drop is used by placing the diode across the transistor base-collector junction. The Schottky diode becomes forward biased when the collector voltage falls 0.4 volts below the base voltage. Excess base drive is then shunted into the collector circuit prohibiting the transistor from reaching classic saturation. With almost no stored charge in either the SBD or the transistor, there is a large reduction in storage time. Thus, transistor switching time is significantly reduced.

A cross sectional area of the Schottky diode is shown in Figure 5-54.

SCHOTTKY CLAMPED TRANSISTOR

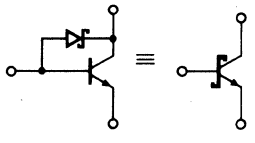


Figure 5-53

SCHOTTKY CLAMPED TRANSISTOR GEOMETRY

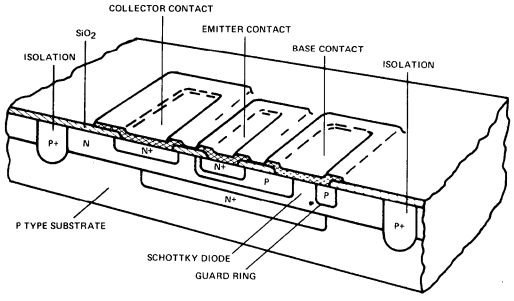


Figure 5-54

COMPARING THE COMPARATORS

Presently available comparator ICs range from the ultra fast 521 to the general purpose comparator fashioned from an inexpensive op amp. Selection of the device depends upon the application in which it will be used. Often times speed of conversion is of primary importance to minimize pulse position errors of high frequency signals. At other times the parameters are much less stringent allowing the use of a general purpose comparator.

A handy reference guide to the major parameters is summarized in Table 5-3. At a glance the necessary parameters can be chosen to select the proper device.

521/522 Comparators

A general description of the comparator devices is included here to familiarize the user with available devices and their advantages.

Processed with state-of-the-art Schottky barrier diodes the 521/522 series devices provide good input characteristics while providing the fastest analog to TTL conversion to date. Total delay from input to output is typically 6ns with a guaranteed speed of 12ns. Additional features of this device include the dual configuration and individual output strobes to simplify system logic. The 522, although sacrificing some speed, features open collector outputs for party line or wired-OR configurations for additional system flexibility.

Device	Propagation Delay (ns)	Vos (mV)	Ios (μA)	Ibias (μA)	Gain	CMR (V)	Benefits
521	12	7.5	5	20	5000	±3	Dual, very fast, standard supplies, TTL compatible, individual & common strobe.
522	15	7.5	5	20	5000	±3	Same as 521 plus open collector outputs for additional decoding.
526	48	5	5	35	—	+4.2 -3.2	General purpose, ±5V supplies, strobe, separate amplifier output, large common mode range.
527	26	6	0.75	2	5000	±6	Fast, very low input current, differential outputs, flexible surplus wide common mode range.
529	22	6	5	20	5000	±6	Same as 527 but with faster response.

NOTE Parameters are based on min/max limits at 25°C as defined in the individual data sheet.

Table 5-3 COMPARATOR SELECTION GUIDE

526 Comparator

The 526 is a medium speed analog comparator intended for applications where rapid recovery from common mode or differential overdrive is necessary. The circuit consists of a medium gain differential amplifier and high speed TTL gate. Compatible with all TTL logic families, the 526 provides independent amplifier and gate outputs and operates from standard ±5 volt supplies.

If desired more than one gate may be driven from the 526 amplifier output. Should this be necessary, a 5k ohm pull down resistor from the amplifier output to V- should be added to increase the sink current capability as shown in Figure 5-55. More than one amplifier may also be tied together for system flexibility. This configuration produces the logic NOR of 2 analog signals at the output of the gate.

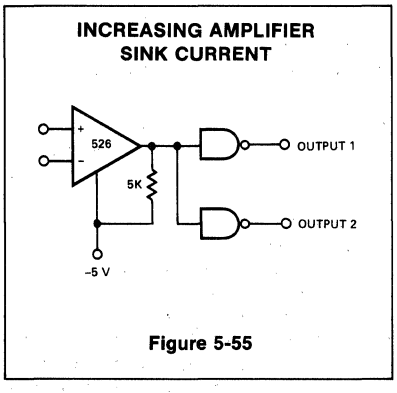


Figure 5-55

527 Comparator

Featuring darlington inputs for very low bias current, the 527 is generically related to the 529 comparator. Emitter follower inputs to the differential amplifier are used to trade better input parameters for slightly less speed. As Table 5-3 shows, a factor of 10 improvement in I_{BIAS} is gained with an increase of propagation delay of only 4ns maximum.

529 Comparator

Second in speed only to the 521 device, the 529 is also manufactured using Schottky technology. Although a few nano seconds slower than the 521, the 529 features variable supplies from ±5 to ±10 volts with a high common mode range of ±6 volts. Both the 527 and 529 Schottky comparators boast complimentary logic outputs with output A being in phase with input A. In addition the supplies of both the 527 and 529 may be non-symmetrical to produce a desired shift in the common mode range. This technique is illustrated by the ECL to TTL and TTL to ECL translators of Figures 5-65 and 5-66 respectively. The only major requirement of the supplies is that the negative supply be at least 5 volts more negative than the ground terminal of the gate. This is necessary to insure that the internal bias arrangement has sufficient voltage to operate normally.

APPLICATIONS

Today's state-of-the-art ultra-high speed comparators are capable of making logic decisions in less than 10 nano seconds. They are easily applied and possess good input and power supply noise rejection. As with all linear ICs however, some preliminary steps should be taken in their use.

General Precautions

Layout

The comparator is capable of resolving submillivolt signals. To prevent unwanted signals from appearing at signal ports, good physical layout is required. For any high speed design, ground planes should be used to guard against ground loops and other sources of spurious signals. At high frequencies hidden signal paths become dominant. Of a particular nuisance is distributed capacitance. If care is not taken to isolate output from input, distributed capacitance can couple a few millivolts into the input, causing oscillation.

Another source of spurious signal is ground current. Input structures are relatively high impedance while the gate structures of comparators run with large signal and ground currents. If this gate ground current is allowed to pass near the input signal path, the small impedances of the ground circuit will cause millivolt changes in reference or signal voltages producing errors, sustained oscillation, or ringing. A ground plane arranged such that output currents do not flow near input areas is highly recommended.

Power Supplies

Another general precaution that should always be exercised is power supply bypassing. As mentioned the name of the game is speed. Very high speed gates are used to produce the desired output logic levels. Maximizing response speed also requires higher current levels, giving rise to power supply noise. For this reason good power supply by-passing is always mandatory very close to the device itself. A tantalum capacitor of 1 to 10μF in parallel with 500 to 1000pF will prove effective in most cases. Lead lengths should be as short as physically possible to preserve low impedances at high frequency.

Unused Inputs

Some currently available comparators such as the 521 and 522 are dual devices. Most often both sections of these devices will be utilized. Should a system utilize one device, the unused inputs should be biased in a known condition. The high gain-bandwidth may otherwise cause oscillations in the unused comparator section. A low impedance should be provided from both unused inputs to ground. A resistor of relatively high impedance may then be used to supply a differential input on the order of 100mV to insure the comparator assumes a known state.

If the inverting input is tied to the positive differential voltage the gate output will be low. The strobe inputs then provide a means of utilizing the Schottky gate for other system logic functions.

Common Mode Signals

As defined previously manufacturers specify the maximum voltage range over which the inputs may be taken. In addition the maximum differential voltage that may be safely applied to the inputs is specified. In the case of the 529 comparator the differential voltage is restricted to less than ±5 volts, with a common mode of ±6 volts. That these two quantities interact cannot be overlooked during application. For instance with both inputs at ±4 volts the common mode restriction is satisfied. If V ref is now left at +4 volts the signal input may not be taken below ground more than 1 volt because the differential signal becomes 5 volts.

It is important to observe this maximum rating since exceeding the differential input voltage limit and drawing excessive current in breaking down the emitter-base junctions of the input transistors could cause gross degradation in the input offset current and bias current parameters.

Exceeding the absolute maximum positive input voltage limit of the device will saturate the input transistor and possibly cause damage through excessive current. However, even if the current is limited to a reasonable value so that the device is not damaged, erratic operation can result.

Input Impedance

The differential bias and offset currents of comparators are minimized by design. As was pointed out for op amps, the input resistance seen by both inputs should be equal. This reduces to a minimum the contribution of offset current to threshold error. Unbalanced input impedance also adds to the offset error due to the difference in voltage drop across the input resistances.

BASIC APPLICATIONS

The basic comparator circuit and its transfer function were presented by Figures 5-49 and 5-50.

When the input exceeds the reference voltage, the output switches either positive or negative, depending on how the inputs are connected.

The vast majority of specific applications involve only the basic configuration with a change of reference voltage. A to D converters are realized by applying the signal to one terminal and the voltage derived from a ladder network to the other. Limit detectors are likewise made from only the very basic circuit. Both are only a small deviation from the basic level detector.

Hysteresis

Normally saturated high or low, the amplifiers used in voltage comparators are seldom held in their threshold region.

They possess high gain-bandwidth products and are not compensated to preserve switching speed. Therefore if the compared voltages remain at or near the threshold for long periods of time, the comparator may oscillate or respond to noise pulses. For instance this is a common problem with successive approximation D/A converters where the differential voltage seen by the comparator becomes successively smaller until noise signals cause indecision. To avoid this oscillation in the linear range, hysteresis can be employed from output to input. Figure 5-56 defines the arrangement. Both positive and negative feedback is provided by R_{IN} and R_f.

Hysteresis occurs because a small portion of the "one" level output voltage is fed back in phase and added to the input signal. This feedback aids the signal in crossing the threshold. When the signal returns to the threshold, the positive feedback must be overcome by the signal before switching can occur. The switching process is then assured and oscillations cannot occur. The threshold "dead zone" created by this method, illustrated in Figure 5-57, prevents output chatter with signals having slow and erratic zero crossings.

LEVEL DETECTOR WITH HYSTERESIS

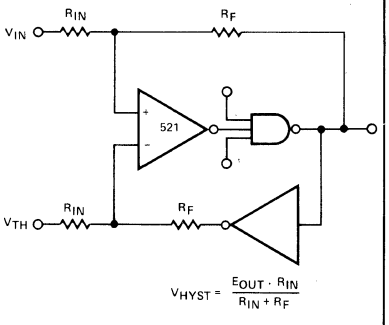


Figure 5-56

0 VOLT LEVEL DETECTOR WITH ± 10mV HYSTERESIS

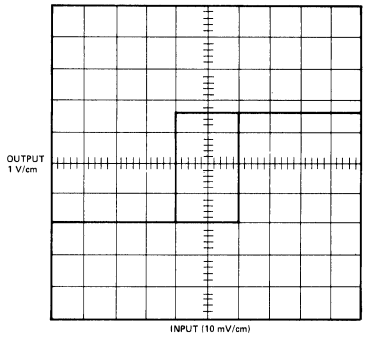


Figure 5-57

As shown in Figure 5-56 the voltage feedback is calculated from the expression:

$$V_{HYST} = \frac{E_{OUT} \bullet R_{IN}}{R_{IN} + R_f}$$

where E_{OUT} is the gate output voltage. The hysteresis voltage is bounded by the common mode range and the ability of the gate to source the current required by the feedback network. If symmetrical hysteresis is desired an additional inverting gate is required if the comparator does not have differential outputs. The 527 and 529 devices provide inverted signals from differential outputs while the 521, 522 and 526 devices will require the inverter. Care should be taken in the selection of the inverter that propagation delay is minimum especially for very high speed comparators such as the 521.

Line Receiver

Retrieving signals which have been transmitted over long cables in the presence of high electrical noise is a perfect application for differential comparators. Such systems as automated production lines and large computer systems must transmit high frequency digital signals over long distances. If the twisted pair of the system is driven differentially from ground, the signals can be reclaimed easily via a differential line receiver.

Since the electrical noise imposed upon a pair of wires takes the form of a common mode signal, the very high common mode rejection of the 521/522 makes the unit ideal for differential line receivers. Figure 5-58 depicts the simple schematic arrangement. The 521 is used as a differential amplifier having a logic level output. Because common mode signals are rejected, noise on the cable disappears and only the desired differential signal remains. Figure 5-59 illustrates the 521 response to the 200mV peak to peak 10MHz differential signal. In Figure 5-60 the same signal has been buried in 5 volts peak to peak of 1MHz common mode "noise."

As shown the circuit suffers no degradation of signal. If desired several 522 comparators may be "wire OR'd," or a latch output can be accomplished as shown.

The 521 and 529 comparators have the advantage of wider bandwidth to permit higher data rates. Where speed is slower the 526 comparator will also provide the excellent common mode rejection needed for line receiving.

Double Ended Limit Detector

Many system designs require that it be known when a signal level lies between two limits. This function is easily accomplished with a single 522 package. The schematic and transfer curve of the circuit is shown in Figure 5-61.

Each half of the 522 is referenced to the desired upper or lower voltage limit producing the desired transfer curve shown. Taking advantage of the dual configuration and the open collectors of the 522 minimize external components and connections.

Crystal Oscillator

Any device with a reasonable gain can be made to oscillate by applying positive feedback in controlled amounts. The 521 will lend itself to crystal control easily, provided the crystal is used in its fundamental mode. Figure 5-62 shows a typical oscillator circuit.

The crystal is operated in its series resonant mode, providing the necessary feedback through the capacitor to the input of the 521. The resistor R_{adj} is used to control the amount of feedback for symmetry. Oscillations will start whenever a circuit disturbance such as turning on the power supplies occurs. The 521 will oscillate up to 70MHz. However, crystals with frequencies

LINE RECEIVER

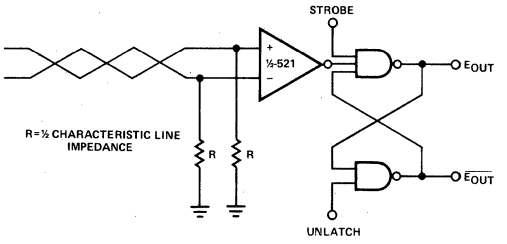


Figure 5-58

LINE RECEIVER RESPONSE

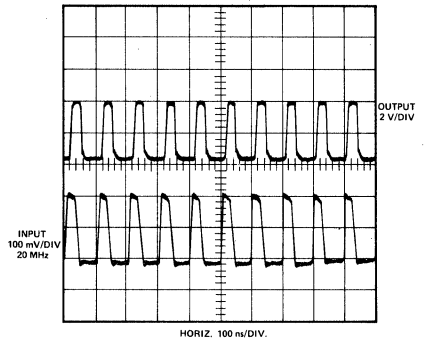


Figure 5-59

DOUBLE ENDED LIMIT DETECTOR

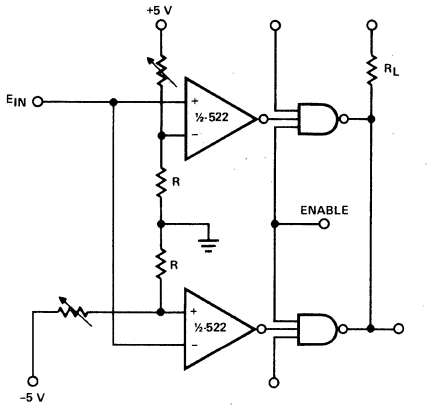


Figure 5-61a

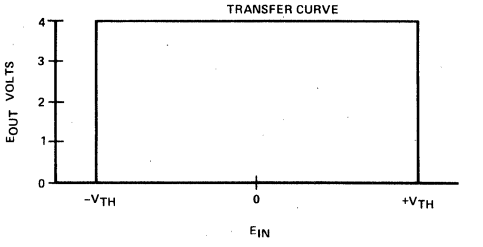


Figure 5-61b

RESPONSE DURING COMMON MODE NOISE

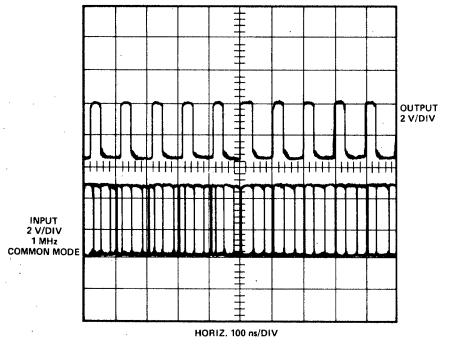


Figure 5-60

CRYSTAL OSCILLATOR

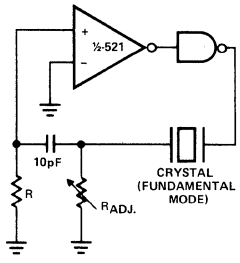


Figure 5-62

higher than about 20MHz are usually operated in one of their overtones. To build an oscillator for a specific overtone requires tuned circuits in addition to the crystal to provide the necessary mode suppression. If the spurious modes are not tuned out the crystal will oscillate at the fundamental frequency. Higher frequency oscillators could be realized using input and output mode suppression or tuning. The 522 is especially desirable since the bare collector topology allows the output to be collector tuned readily.

Analog to Digital Converter

There are many types of A to D converter designs, each having its own merits. However, where speed of conversion is of prime interest the multi-threshold conversion type is used exclusively. It is apparent from Figure 5-63 that the conversion speed of this design is the sum of the delay through the comparator and the decoding gates.

The sacrifices which must be made to obtain speed are the number of components, bit accuracy and cost. The number of comparators needed for an N-bit converter is 2^{n-1}. Although the 521 provides two comparators per package, the length of parallel converters is usually limited to less than 4 bits. Accuracy of multi-threshold A-D converters also suffers since the integrity of each bit is dependent upon comparator threshold accuracy.

The implementation of a 3-bit parallel A-D converter is shown in Figure 5-64 with a 3-bit digital equivalent of an analog input shown in Figure 5-63.

Reference voltages for each bit are developed from a precision resistor ladder network. Values of R and 2R are chosen so that the threshold is one half of the least significant bit. This assures maximum accuracy of ±1/2 bit.

It is apparent from the schematic that the individual strobe line and duality features of the 521 have greatly reduced the cost and complexity of the design. The speed of the converter is graphically illustrated by the photo of Figure 5-63. All 3-bit outputs have settled and are true a mere 15ns after the input step of 3 volts has arrived. The output is usually strobed into a register only after a certain time has elapsed to insure that all data has arrived.

Logic Interface

During the design of the 527 and 529 devices, particular attention was paid to the biasing network so that balanced supplies need not be provided. For example, if the "ground" terminal is set at -5.2 volts and the other supplies are adjusted accordingly, the output logic 1 state will be at -1.5 volts and logic 0 will be at -5.0 volts. With this freedom of power supply voltage, the user may adjust the output swings to match the desired logic levels even if that logic is other than TTL levels.

ECL to TTL Interface

Emitter coupled logic is becoming very popular due to its speed. Systems are often built around standard TTL logic with those portions requiring higher speed being implemented with emitter coupled logic. As

PARALLEL A-D RESPONSE

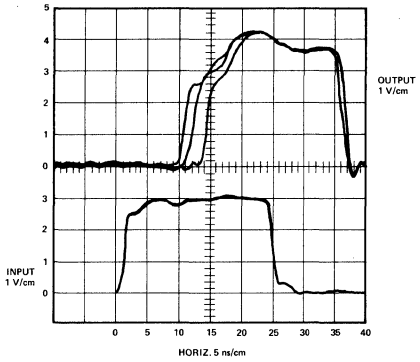


Figure 5-63

3-BIT PARALLEL A-D CONVERTER

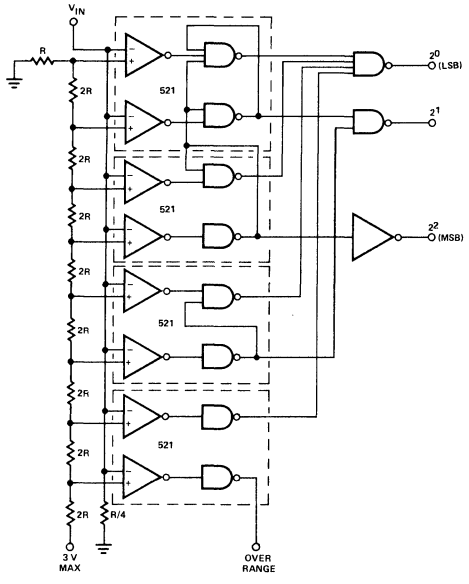


Figure 5-64

soon as such a decision is made the problem of interfacing TTL to ECL logic levels is encountered. The standard logic output swings of ECL are -0.8V to -1.8V at room temperatures. Converting these signals to TTL levels is accomplished simply by using the basic voltage comparator circuit with slight modifications. Figure 5-65 reveals that the power supplies have been shifted in order to shift the common mode range more negative. This insures that the common mode range is not exceeded by the logic inputs. Since ECL is extremely fast the 529 is usually selected because of its superior speed so that a minimum of time is lost in translation.

TTL to ECL

Operating in the reverse, TTL levels can also be converted to ECL levels by the 529. Again the 529 is selected as the fastest converter with the necessary power supply flexibility to accomplish the level shifting with a minimum of effort and cost.

A check of output voltage for the 529 reveals that the voltage is slightly less than required by the ECL logic for fast switching. R2 and the diode of Figure 5-66 raises the gate supply voltage and therefore the 529 output voltage by 0.7V sufficient to guarantee fast switching of the translator. Resistive pull up from the 529 output to V_{CC} can also be used with the gate supply grounded. This method is dependent upon RC time constants of distributed capacitance and is therefore much slower.

Photo Diode Detector

Responding to the presence or absence of light, the photo diode increases or decreases the current through it. Detecting the changes becomes a matter of converting light and dark currents to voltage across a resistor as shown in Figure 5-67. R1 is selected to be large enough to generate detectable differences between light and dark conditions. Once the signal levels are defined by R1 and the diode characteristics, the average between light and dark signals is used for V reference and is produced by the resistive divider consisting of R1 and R2. The comparator then produces an output dependent upon the presence or absence of light upon the diode.

SENSE AMPLIFIERS

Closely related to the comparator is the sense amplifier. Signals derived from the many sources such as transducers and core memories are not of sufficient amplitude to be compatible with subsequent logic. It then becomes necessary to amplify and convert the signal to TTL levels, which is the responsibility of the sense amplifier.

As an example, the 1103 MOS RAM output is of the bare drain variety. Hence the output of the memory takes the form of a current for a one level with zero current for a zero level.

It remains, then, for the user to convert these currents to TTL levels. A terminating resistor from the drain to ground provides a voltage output proportional to the current and the resistor size. Larger signals can be produced by larger resistors; but in practice resistors larger than 1k ohm are avoided because of increasing access time. Distributed capacitance forms a time constant with this output resistance causing slow rise and fall times when the resistor is large, adding to the access time.

Virtually any voltage comparator or sense amplifier can be used. Since total time is the sum of all delays, the sense amplifier is most often the fastest available. Signetics comparators 521 and 522 are ideal in this application because of low input offset voltages and very fast response. Using these Schottky clamped comparators significantly reduces the total cycle time of the memory.

Design of the sense amplifier network depends upon the 1103 used (1103 or 1103-1) and the input characteristics. Two sense amplifiers will be discussed in this application, the 521/522 and the 75107/75108. Both sets of devices are very similar in operation with basic differences in input parameters

ECL TO TTL TRANSLATOR

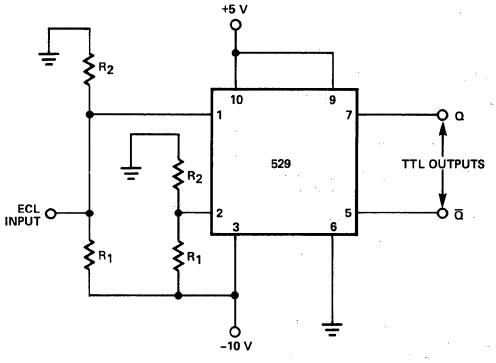


Figure 5-65

TTL TO ECL TRANSLATOR

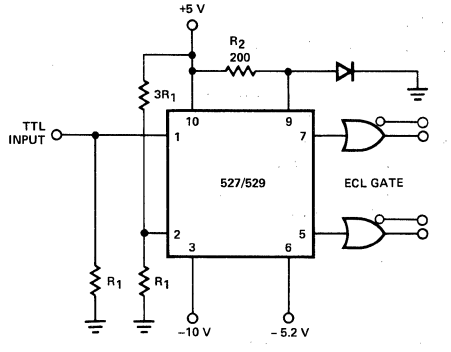


Figure 5-66

and speed. The significiant specifications are given in Table 5-4.

DEVICE	V_{OS} (mV)	I_B (μA)	V_{IN} (MIN) (mV)	SPEED (NS) (V_{IN}=100mV)	GAIN
521	10	40	15	12	5000
522	10	40	15	15	5000
75107	-	75	25	25	-
75108	-	75	25	25	-

Table 5-4 IMPORTANT SENSE AMPLIFIER PARAMETERS

Consideration must first be given to the differential input voltage requirements of the sense amplifier. The required reference voltage is calculated from the relationship:

$$V_{ref} \leq (I_1 - I_B)\, R1 - V_{diff}$$

Where I_1 is the 1103 output current, I_B is sense amplifier bias current and V_{diff} is minimum differential voltage to switch the sense amplifier.

Thus, referring to Figure 5-68, the calculation for the 522 and the 1103-1 becomes:

$$V_{ref} \leq (900\mu A - 40\mu A)\, R - 15mV$$

Hence V_{ref} must be less than 71mV for a 100 ohm resistor. Values of R1 can be selected from 100 to 1000 ohms. Resistor values less than 100 ohms do not produce sufficient voltage swings while values over 1k ohm tend to generate excessive noise from capacitively coupled signals.

In large systems noise coupled into the sense lines by stray capacitance can be very troublesome. Judicious layout patterns with sense lines being as short as possible will help, but large memories can still be difficult to control. One method of eliminating noise is to use a balanced sense line as shown in Figure 5-69.

PHOTO DIODE DETECTOR

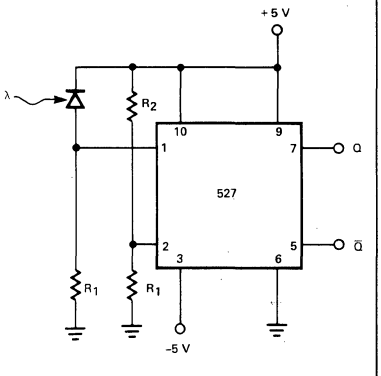
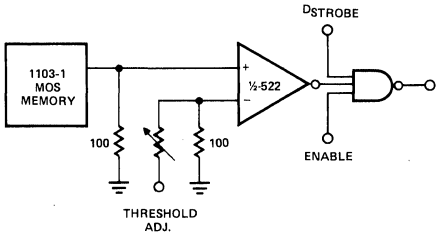


Figure 5-67

1103 MEMORY SENSE AMPLIFIER



All resistor values are in ohms.

Figure 5-68

During layout a dummy line is run parallel to the actual sense line in as close proximity as possible. One end is connected to the sense amplifier at the V_{ref} point while the other end is left open. The normal sense line is connected as usual. Electrical noise imposed upon the pair of sense lines takes the form of a common mode signal and will be rejected by the sense amplifier. Signal currents in the sense line, on the other hand, form differential signals at the sense amp causing the output to switch.

Core Memory Sense Amps

The core memory is another device requiring a sense amplifier.

Figure 5-70 shows a simplified block diagram of memory organization in a computer. The appropriate command to the address register selects the appropriate x and y address lines. Two wires are threaded through each core. One is common to all cores in that column arranging a matrix in which any x-address line and any y-address line has only one core in common.

Both reading and writing are accomplished by driving current through the wires linking the cores. If this current exceeds a minimum value I_m, the core is reset to zero. Therefore, by driving $I_m/2$ through one of the x-address lines and through one of the y-address lines, any one core may be reset. Only the core common to both lines will receive the sum of the currents and will be reset. The rest of the cores receive $I_m/2$ and will be only half-selected. For a core to be set to the "1" state, the current is reversed in the two selecting wires.

A sense line linking all the cores in the plane together couples the read data out of the array. In order to read a specific core, a "0" is first written into that core. If its initial state was at "1", it is reset, generating a pulse on the sense line. If the core is in "0" state, no signal results.

The high currents used in core memory generate a good deal of noise. The sense amplifier used must be able to detect the difference between the disturbed one voltage, without responding to undesired signals. The threshold voltages of the sense amplifier should be adjusted to approximately the mid-point between the sum of the disturbed zero voltages and the minimum disturbed one voltage as defined in Figure 5-71.

The region on either side of the threshold voltage in which the sense amplifier cannot detect the difference between a 0 and a 1 is called the uncertainty region. This region is the sum of the varition of the input threshold voltage and the differential offset voltage and must be less than the voltage difference between ones and zeros generated by the memory core.

Signetics series N7520 Dual Core Memory Sense Amplifiers, successfully solve the basic sense amplifier problems: It provides a stable narrow input threshold, an adjustable reference and output logic functions to fulfill the several variations required in different core memory systems.

The N7520 series uses the "true comparator" technique to achieve superior amplifier threshold performance. A unique circuit design of the internal logic guarantees the fastest possible propagation. Series N7520 is pin compatible with other 7520 series and offers the user these advantages:

BALANCED SENSE LINE TO REDUCE NOISE

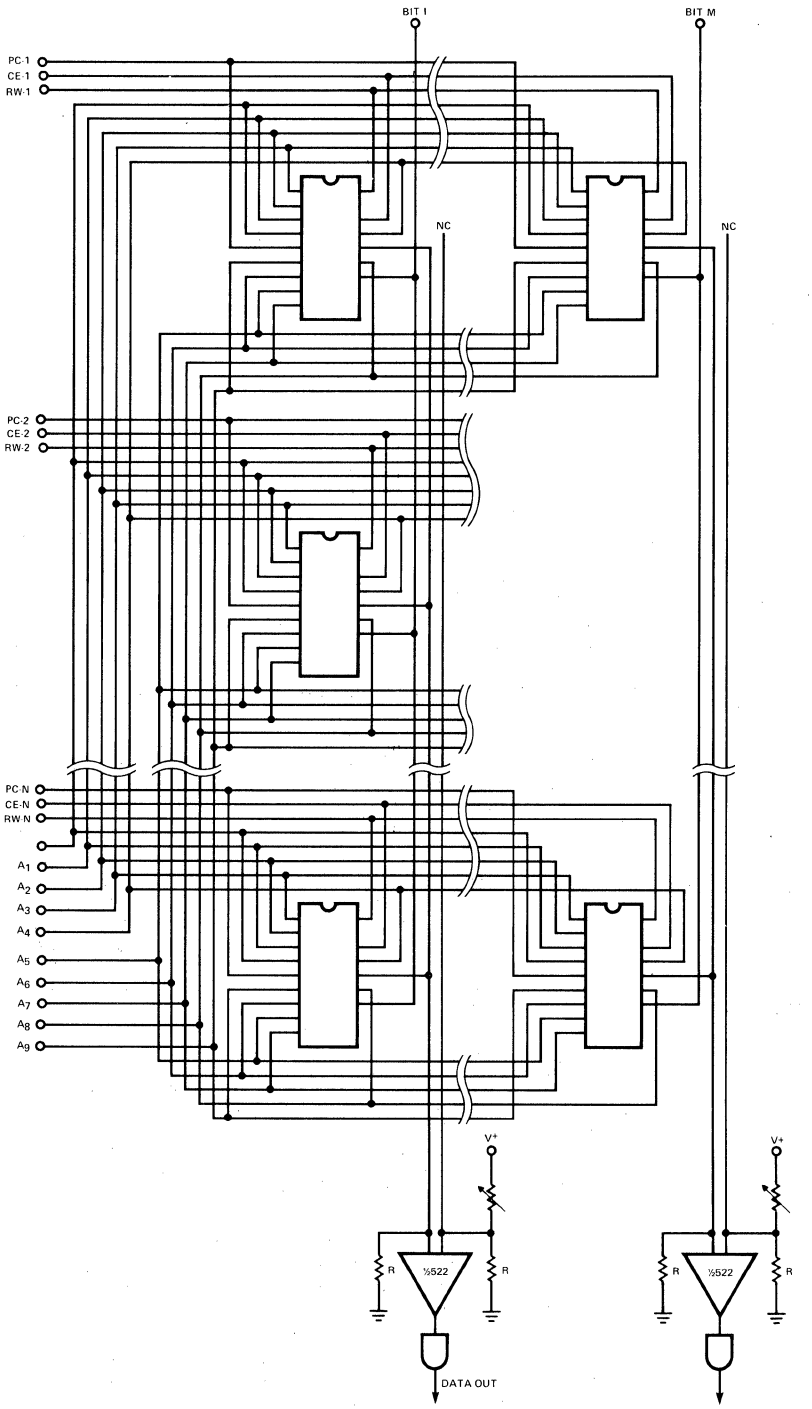


Figure 5-69

TYPICAL DIGITAL COMPUTER MEMORY ORGANIZATION

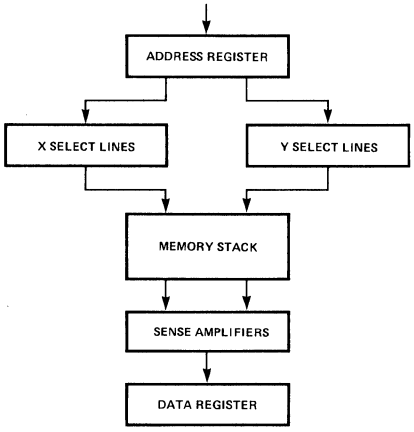


Figure 5-70

TYPICAL CORE DISTURBED ZERO AND DISTURBED ONE SIGNALS

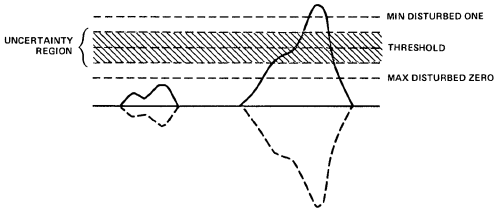


Figure 5-71

a. True Comparator technique guarantees that narrow input threshold devices can be built in volume production.
b. An external capacitor is not required for stability. True Comparator technique allows use of simple single stage preamp.
c. Clamp diodes are provided at all gate and strobe inputs.

Figure 5-72 illustrates the necessary connections to utilize the 7524 sense amplifier. The reference voltage against which the sense voltage is compared is derived via the resistor divider network from the 5 volt supply. Other connections are straight forward and for the most part self explanatory.

Care should be exercised in the board layout to minimize stray coupling of signals. Of extreme importance to the device, the reference voltage must be kept as clean as possible. For instance, ground currents from the gate structure should not be allowed to pass near the reference terminals before finding system ground. Small voltages generated by this current can cause reference instability. Oscillations and general poor performance can also occur if proper techniques are not used in layout.

55/75325 MEMORY DRIVERS TYPICAL APPLICATIONS

Balanced Bipolar Logic Line Driver

The circuit shown in Figure 5-73 converts standard TTL logic to bipolar logic. Bipolar logic is primarily used in transmitting data or clock pulses over long lines. This line-driver may be operated from a single 5 volt supply; however; the output drive may be increased by raising the supply voltage to the source collectors. The circuit features a tri-state output which is off during the absence of data, thus not dissipating high power. It provides a balanced drive circuit giving maximum noise immunity when used with the proper line receiver. Large drive levels can be used to further increase noise immunity. The circuit is capable of driving twisted-pair lines of several miles in length or low-impedance coaxial lines.

In memory-drive applications the 75325 (or for full-temperature operation, the 55325) can be connected in any of several ways. Typically, however, sources and sinks are arranged in pairs from which many drive-lines branch off as shown in Figure 5-74. Here each drive-line is served by a unique combination of two source/sink pairs so that a selection matrix is formed. To select drive-line 13, 75154 No. 1 must be set to 3 (with mode select high), enabling source X of 75325 No. 2 to drive lines 12 through 15, and 74154 No. 2 must be set to 2, providing a sink at Y of 75325 No. 4 for drive-line 13 only. Alternatively, to drive current in drive-line 13 in the opposite direction, only the mode-select voltage would be changed from high to low. The size of such a matrix is limited only by the number of drive-lines that a source/sink pair can serve. This number in turn depends on the capacitive and inductive load that each drive-line of the particular system imposes on the driver. A 256-drive-line selection matrix is shown in Figure 5-75. These 256 drive-lines are sufficient to serve $(256/2)^2 = 16{,}384$ individual cores.

External Resistor Calculation

A typical magnetic-memory word-drive requirement is shown in Figure 5-76. A source-output transistor of one 75325 delivers load current (I_L). The sink-output transistor of another 75325 sinks this current.

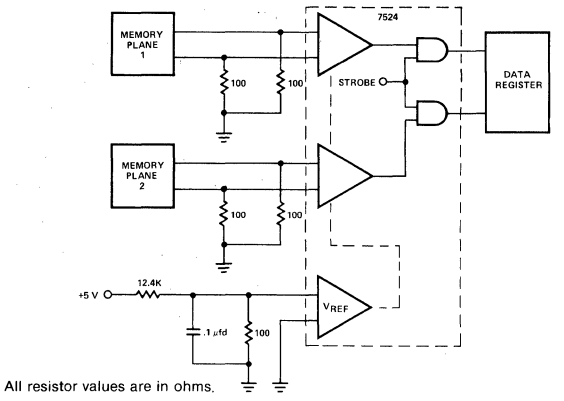
The value of the external pull-up resistor (R_{ext}) for a particular memory application may be determined using the following equation:

$$R_{ext} = \frac{16\,(V_{CC2(min)} - V_S - 2.2)}{I_L - 1.6\,(V_{CC2(min)} - V_S - 2.9)}$$

(Equation 1)

where: R_{ext} is in kΩ,
$V_{CC2(min)}$ is the lowest expected value of V_{CC2} in volts,
V_S is the source output voltage in volts with respect to ground,
I_L is in mA.

TYPICAL SENSE AMPLIFIER HOOK UP USING 7524



All resistor values are in ohms.

Figure 5-72

The power dissipated in resistor R_{ext} during the load current pulse duration is calculated using Equation 2,

$$P_{Rext} \approx \frac{I_L}{16}[V_{CC2(min)} - V_S - 2] \qquad \text{(Equation 2)}$$

where: P_{Rext} is in mW.

After solving for R_{ext}, the magnitude of the source collector current (I_{CS}) is determined from Equation 3,

$$I_{CS} \approx 0.94\ I_L \qquad \text{(Equation 3)}$$

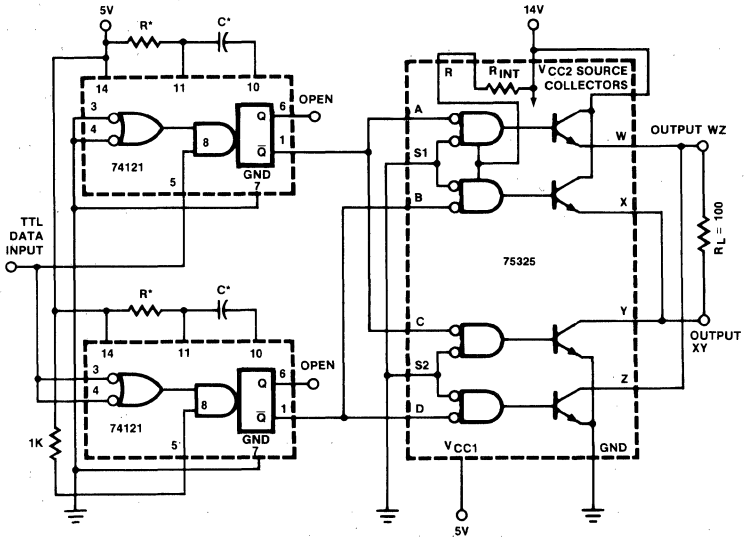
where: I_{CS} is in mA.

As an example, let $V_{CC2(min)} = 20V$ and $V_L = 3V$ while I_L of 500mA flows.

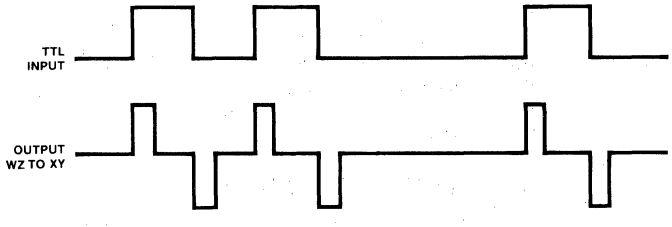
Using Equation 1,

$$R_{ext} = \frac{16\ (20 - 3 - 2.2)}{500 - 1.6\ (20 - 3 - 2.9)} = 0.5k\Omega$$

BALANCED BIPOLAR LOGIC LINE DRIVER



a. Test Circuit

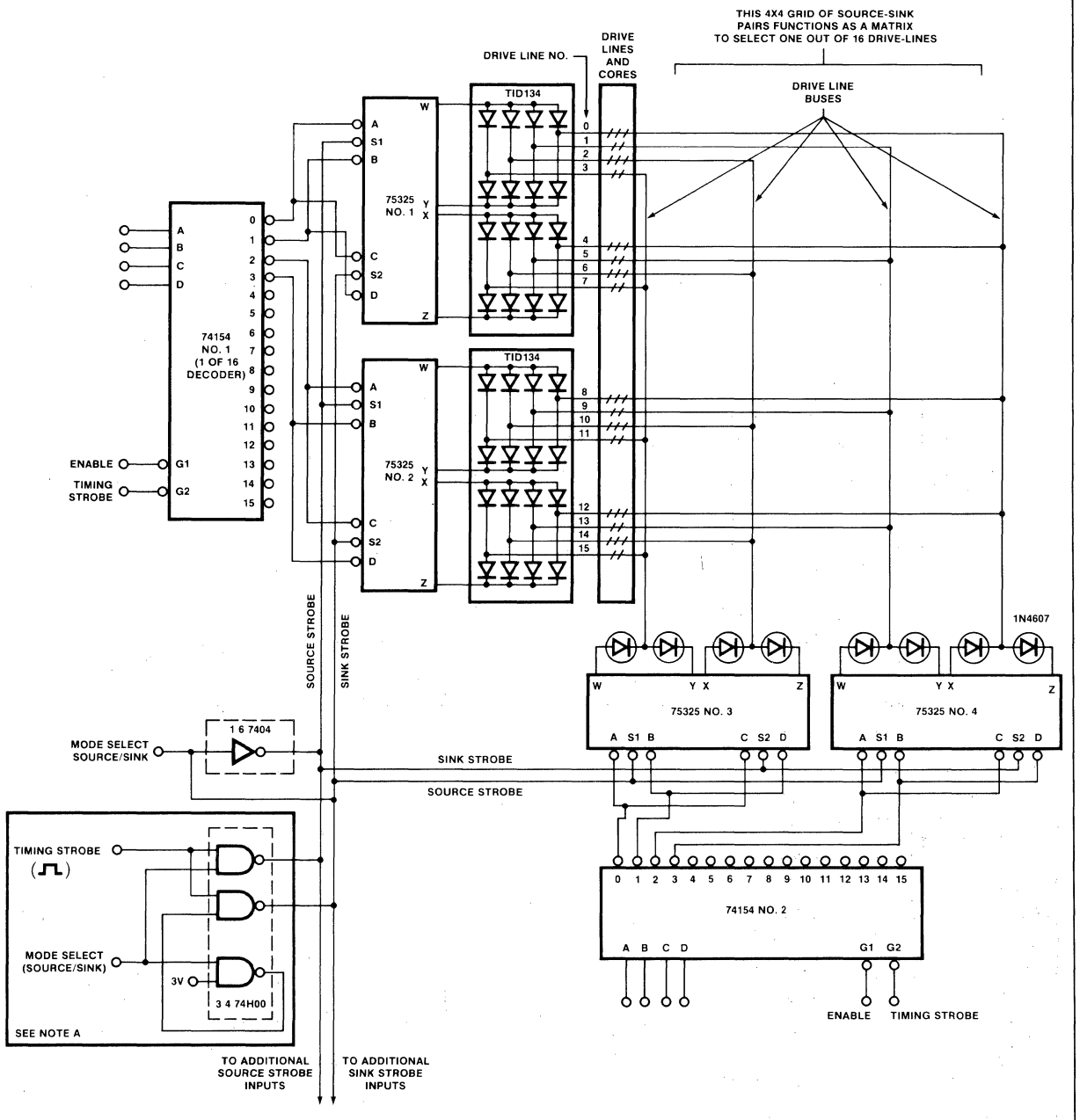


b. Voltage Waveforms

All resistors values are typical and in ohms.
*R and C are adjusted to give the desired bipolar output pulse width.

Figure 5-73

75325 USED AS A MEMORY DRIVER TO SELECT ONE OF SIXTEEN DRIVE LINES



NOTE A This optional mode select and timing strobe technique can be used in place of the 7440 mode select and 74154 timing strobe when minimum time skew is desired.

Figure 5-74

75325 SERVING 256 DRIVE LINES IN A MAGNETIC MEMORY

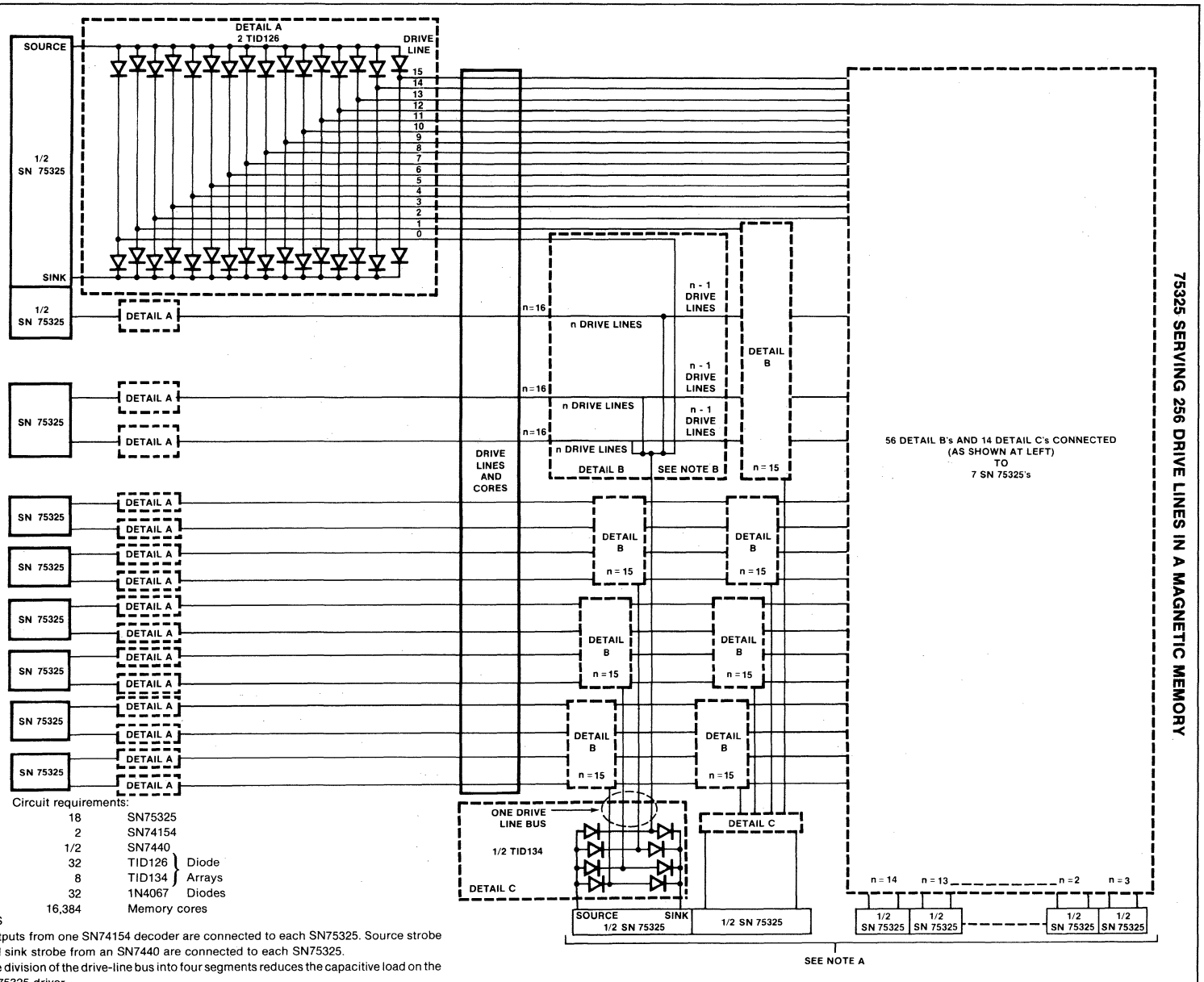


Figure 5-75

Circuit requirements:

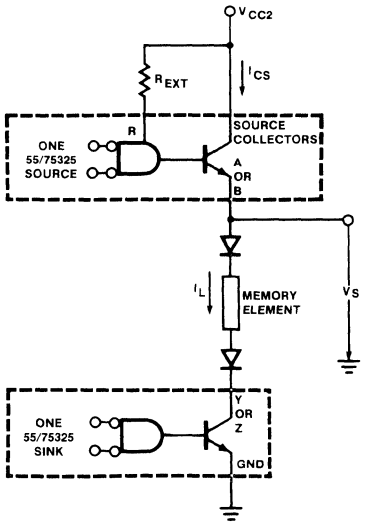
18	SN75325
2	SN74154
1/2	SN7440
32	TID126 } Diode
8	TID134 } Arrays
32	1N4067 Diodes
16,384	Memory cores

NOTES

A. Outputs from one SN74154 decoder are connected to each SN75325. Source strobe and sink strobe from an SN7440 are connected to each SN75325.

B. The division of the drive-line bus into four segments reduces the capacitive load on the SN75325 driver.

TYPICAL MAGNETIC MEMORY WORD DRIVE REQUIREMENT



NOTE

A. For clarity, partial logic diagrams of two 75325's are shown.
B. Source and sink shown are in different packages.

Figure 5-76

and from Equation 2,

$$P_{Rext} \approx \frac{500}{16} (20 - 3 - 2) \approx 470mW$$

The amount of the memory system current source (I_{CS}) from Equation 3 is:

$$I_{CS} \approx 0.94\ (500) \approx 470mA$$

In this example the regulated source-output transistor base current through the external pull-up resistor (R_{ext}) and the source gate is approximately 30mA. This current and I_{CS} comprise I_L.

VIDEO AMPLIFIER PRODUCTS

592 Video Amplifier

The 592 is a two stage differential output, wideband video amplifier with voltage gains as high as 400 and bandwidths up to 120MHz.

Three basic gain options are provided. Fixed gains of 400 and 100 result from shorting together gain select pins G_{1A} — G_{1B} and G_{2A}—G_{2B} respectively. As shown by Figure 5-78 the emitter circuits of the differential pair return thru independent current sources. This topology allows no gain in the input stage if all gain select pins are left open. Thus the third gain option of tying an external resistance across the gain select pins allows the user to select any desired gain from 0 to 400 volts per volt. The advantages of this configuration will be covered in greater detail under the filter application section.

Three factors should be pointed out at this time:

1. The gains specified are differential. Single ended gains are one half the stated value.
2. The circuit 3dB bandwidths are a function of and are inversely proportional to the gain settings.
3. The differential input impedance is an inverse function of the gain setting.

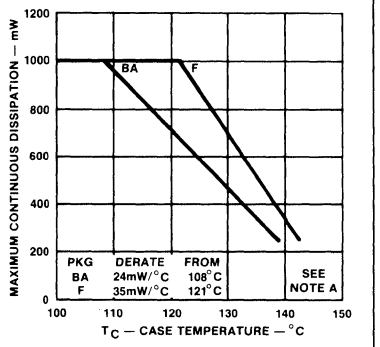
In applications where the signal source is a transformer or magnetic transducer the input bias current required by the 592 may be passed directly thru the source to ground. Where capacitive coupling is to be used, the base inputs must be returned to ground through a resistor to provide a dc path for the bias current.

Due to offset currents, the selection of the input bias resistors is a compromise. To reduce the loading on the source, the resistors should be large, but to minimize the output dc offset, they should be small — ideally 0 ohms. Their maximum value is set by the maximum allowable output offset and may be determined as follows:

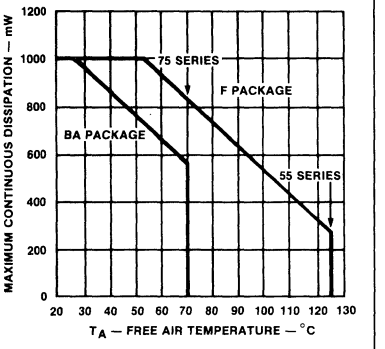
1. Define the allowable output offset (assume 1.5V).
2. Subtract the maximum 592 output offset (from the data sheet). This gives the output offset allowed as a function of input offset currents (1.5V — 1.0V = 0.5V).
3. Divide by the circuit gain (assume 100). This refers the output offset to the input.

THERMAL INFORMATION

CASE TEMPERATURE DISSIPATION DERATING CURVE



FREE-AIR TEMPERATURE DISSIPATION DERATING CURVE



NOTE A rated operating free add temperature ranges must be observed regardless of heat sinking.

Figure 5-77

PARAMETER	501	592	733
BANDWIDTH (MH_Z)	150	120	120
GAIN	6, 10, 20, 50	0,100,400	10,100,400
R_{IN} (K)	1	4-30	4-250
V_{PP} (VOLTS)	3.5	4.0	4.0

Table 5-5 VIDEO AMPLIFIER COMPARISON FILE

4. The maximum input resistor size is:

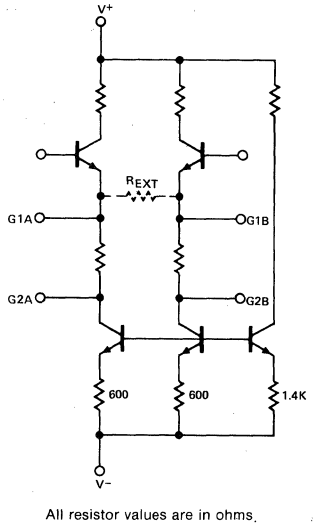
$$R_{MAX} = \frac{\text{Input Offset Voltage}}{\text{Max Input Offset Current}}$$

$$\frac{.005V}{3\mu A}$$

$$= 1.67k\Omega$$

Of paramount importance during the design of the 592 device was bandwidth. In a monolithic device, this precludes the use of pnp transistors and standard level shifting techniques used in lower frequency devices. Thus without the aid of level shifting the output common mode voltage present on the 592 is typically 2.9 volts. Most applications, therefore, require capacitive coupling to the load. An exception to the rule is a differential amplifier with an input common mode range greater than +2.9V as shown in Figure 5-79. In this circuit, the 592 drives a 511B transistor array connected as a differential cascode amplifier. This amplifier is capable of differential output voltages of 48V peak-to-peak with a 3dB bandwidth of approximately 10MHz (depending on the capacitive load). For optimum operation, R1 is set for a no signal level of +18V. The emitter resistors, R_E, were selected to give the cascode amplifier a differential gain of 10. The gain of the composite amplifier is adjusted at the gain selected point of the 592.

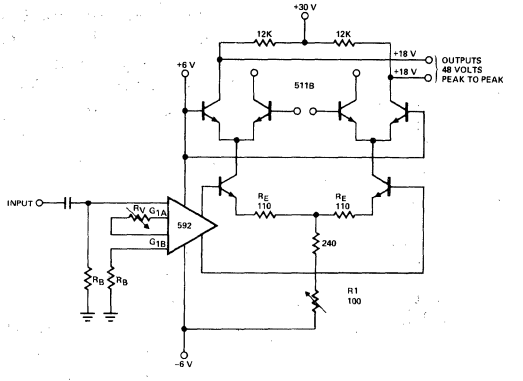
592 INPUT STRUCTURE



All resistor values are in ohms.

Figure 5-78

VIDEO AMPLIFIER WITH HIGH LEVEL DIFFERENTIAL OUTPUT



All resistor values are in ohms.

Figure 5-79

Filters

As mentioned earlier, the emitter circuit of the 592 includes two current sources. Since the stage gain is calculated by dividing the collector load impedance by the emitter impedance, the high impedance contributed by the current sources causes the stage gain to be zero with all gain select pins open. As shown by the gain vs. frequency graph of Figure 5-80 the overall gain at low frequencies is a negative 48dB.

Higher frequencies cause higher gain due to distributed parasitic capacitive reactance. This reactance in the first stage emitter circuit causes increasing stage gain until at 10MHz the gain is 0dB or unity.

Referring to Figure 5-81, the impedance seen looking across the emitter structure includes small r_e of each transistor.

Any calculations of impedance networks across the emitters then must include this quantity. The collector current level is approximately 2mA causing the quantity of 2 r_e to be approximately 32 ohms. Overall device gain is thus given by

$$\frac{V_O(S)}{V_{IN}(S)} = \frac{1.4 \times 10^4}{Z_{(S)} + 32}$$

where $Z_{(S)}$ can be a resistance or a reactive impedance. Table 5-6 summarizes the possible configurations to produce low, high, and bandpass filters. The emitter impedance is made to vary as a function of frequency by using capacitors or inductors to alter the frequency response. Included also in Table 5-6 is the gain calculation to determine the voltage gain as a function of frequency.

Differentiation

With the addition of a capacitor across the gain select terminals the 592 becomes a differentiator. The primary advantage of using the emitter circuit to accomplish differentiation is the retention of the high common mode noise rejection. Disc file playback systems rely heavily upon this common mode rejection for proper operation.

Disc file Decoding

In recovering data from disc or drum files, several steps must be taken to pre-condition the linear data. The NE592 video amplifier, coupled with the 8T20 bi-directional one-shot, provides all the signal conditioning necessary for phase encoded data.

When data is recorded on a disc, drum or tape system, the readback will be a Gaussian shaped pulse with the peak of the pulse corresponding to the actual recorded transition point. This readback signal is usually 500μV p-p to 3mV p-p for oxide coated disc files and 1 to 20mV p-p for nickel-cobalt disc files. In order to accurately reproduce the data stream originally written on the disc memory, the time of peak point of the Gaussian readback signal must be determined.

The classical approach to peak-time determination is to differentiate the input signal. Differentiation results in a voltage proportional to the slope of the input signal. The zero-crossing point of the differentiator, therefore, will occur when the input signal is at a peak. Using a zero-crossing detector and one-shot, therefore, results in pulses occurring at the input peak points.

VOLTAGE GAIN AS A FUNCTION OF FREQUENCY (ALL GAIN SELECT PINS OPEN)

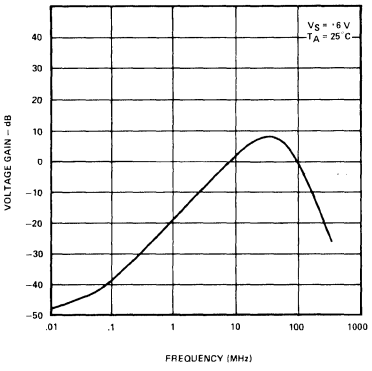


Figure 5-80

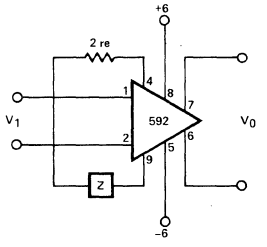
Z NETWORK	FILTER TYPE	V_0 (s) TRANSFER V_1 (s) FUNCTION
R L	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
R C	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
R L C	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/L\, s + 1/LC}\right]$
R L C	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

NOTE: In the networks above, the R value used is assumed to include 2 r_e, or approximately, 32 ohms.

Table 5-6 FILTER NETWORKS

A circuit which provides the preconditioning described above is shown in Figure 5-83. Readback data is applied directly to the input of the first 592. This amplifier functions as a wideband ac coupled amplifier with a gain of 100. The NE592 is excellent for this use because of its high phase linearity, high grain and ability to directly couple the unit with the readback head. By direct coupling of readback head to amplifier, no matched terminating resistors are required and the excellent common mode rejection ratio of the amplifier is preserved. DC components are also rejected because the 592 has no gain at dc due to the capacitance across the gain select terminals.

BASIC GAIN CONFIGURATION



$$\frac{V_0(s)}{V_1(s)} = \frac{1.4 \times 10^4}{Z(s) + 2re} = \frac{1.4 \times 10^4}{Z(s) + 32}$$

Figure 5-81

The output of the first stage amplifier is routed to a linear phase shift low pass filter. The filter is a single stage constant K filter, with a characteristic impedance of 200Ω. Calculations for the filter are as follows:

$L = 2R/\omega c$ Where R = characteristic impedance (ohms)

$C = 1/\omega c$ ωc = cutoff frequency (radians/sec)

The second 592 is utilized as a low noise differentiator/amplifier stage. The 592 is excellent in this application because it allows differentiation with excellent common mode noise rejection.

The output of the differentiator/amplifier is connected to the 8T20 bi-directional monostable unit to provide the proper pulses at the zero-crossing points of the differentiator.

The circuit in Figure 5-83 was tested with an input signal approximating that of a readback signal. The results are shown in Figure 5-85.

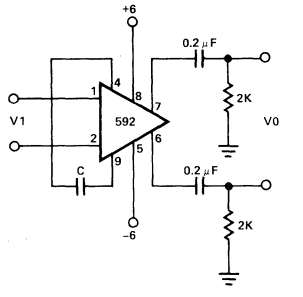
Automatic Gain Control

The 592 can also be connected in conjunction with a MC1496 balanced modulator to form an excellent automatic gain control system. With the circuit of Figure 5-84, the signal is fed to the signal input of the MC1496 and RC coupled to the 592. Unbalancing the carrier input of the MC1496 causes the signal to pass thru unattenuated. Rectifying and filtering one of the 592 outputs produces a dc signal which is proportional to the ac signal amplitude. After filtering this control signal is applied to the MC1496 causing its gain to change.

LINE DRIVERS AND RECEIVERS

Many types of line drivers and receivers are available today. Each device has been designed to meet specific criteria. For instance, the device may be extremely wide band or be intended for use in party line systems. Some include built in hysteresis in the receiver while others do not.

DIFFERENTIAL WITH HIGH COMMON MODE NOISE REJECTION



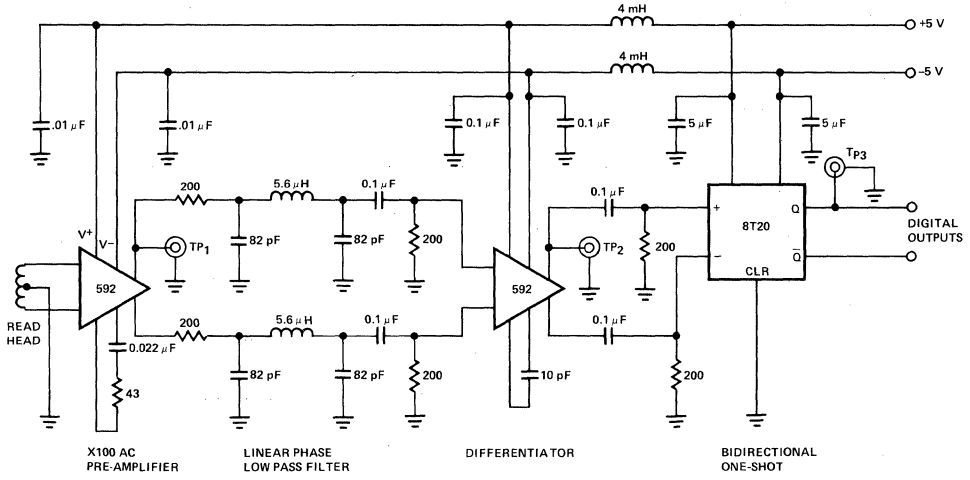
For frequency $F_1 << 1/2\ \pi(32)C$

$V_0 \cong 1.4 \times 10^4 C \frac{dvi}{dT}$

All resistor values are in ohms.

Figure 5-82

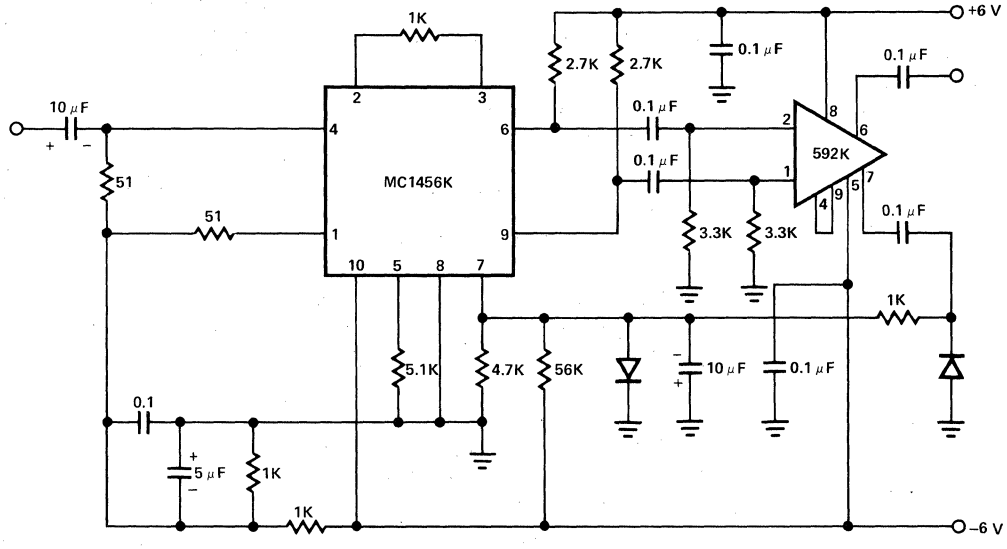
5MHz PHASE—ENCODED DATA READ CIRCUITRY



All resistor values are in ohms.

Figure 5-83

WIDE BAND AGC AMPLIFIER



All resistor values are in ohms.

Figure 5-84

The EIA Standard

The Electronic Industries Association has produced a set of specifications dealing with the transmission of data between data terminal and communications equipment. This is EIA Standard RS-232-C and delineates much information about signal levels and hardware configurations in data systems.

MC1488/1489

As line driver and receiver the MC1488 and MC1489 meet or exceed the RS-232 specification.

Standard RS-232 defines the voltage level as being from 5 to 15 volts with positive voltage representing a logic 0. The MC1488 meets these requirements when loaded with resistors from 3k to 7k ohms.

TEST RESULTS

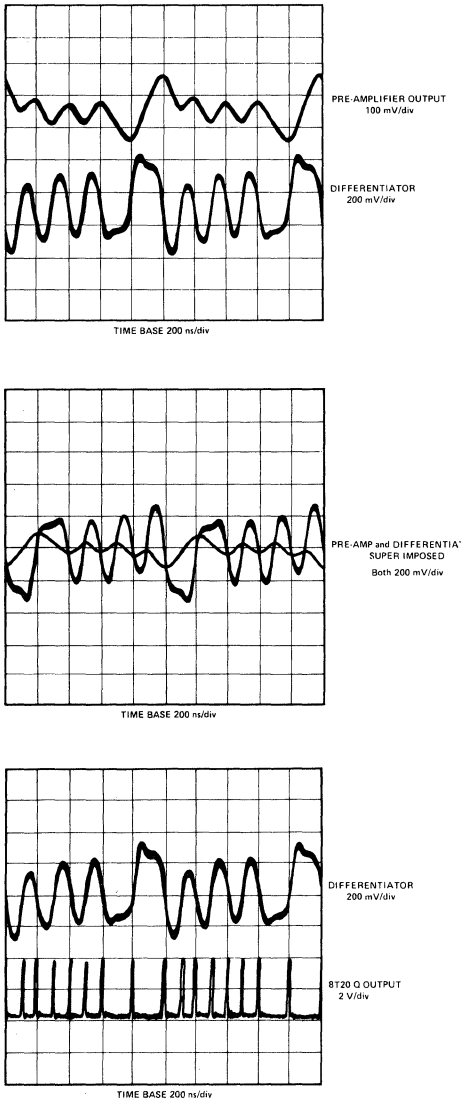


Figure 5-85

Output slew rates are limited by RS-232 to 30 volts per microsecond. To accomplish this specification the MC1488 is loaded at its output by capacitance as shown by the typical hookup diagram of Figure 5-86. A graph of slew rate vs output capacitance is given in Figure 5-87. For the standard 30V/μs a capacitance of 300pF is selected.

The short circuit current charges the capacitance with the relationship.

$$C = \frac{I_{SC}\Delta T}{\Delta V}$$

The EIA standard also states that output shorts to any other conductor of the cable must not damage the driver. Thus the MC1488 is designed such that the output will withstand shorts to other conductors indefinitely even if these conductors are at worst case voltage levels. In addition to output protection the MC1488 includes a 300 ohm resistor to ensure that the output impedance of the driver will be at least 300 ohms even if the power supply is turned off. In cases where power supply malfunction produces a low impedance to ground, the 300 ohm resistors are shorted to ground also. Output shorts then can cause excessive power dissipation. Preventing such a case from happening, series diodes should be included in both supply lines as pictured in Figure 5-88.

The companion receiver MC1489 is also designed to meet RS-232 specifications for receivers. It must detect a voltage from ±3 to ±25 volts as logic signals but cannot generate a differential voltage of greater than 2 volts should its inputs become open circuited. Noise and spurious signals are rejected by incorporating positive feedback internally to produce hysteresis. Featured also in the receiver is an external response node so that the threshold may be externally varied to fit the application. Figure 5-89 shows the shift in high and low trip points as a function of the programming resistance.

PERIPHERAL DRIVERS

Peripheral drivers are general purpose interface devices which interface between logic and devices requiring high current.

Application Areas

POWER SWITCHING
- Relay Drivers
- Electromechanical Controls
- SCR or TRIAC Gates

LAMP DRIVERS
- Pilot Lamps
- Intensity Control

TYPICAL LINE DRIVER-RECEIVER APPLICATION

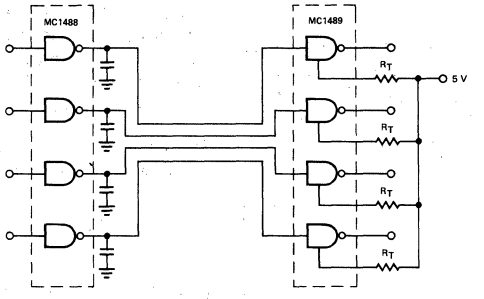


Figure 5-86

OUTPUT SLEW RATE vs. LOAD CAPACITANCE

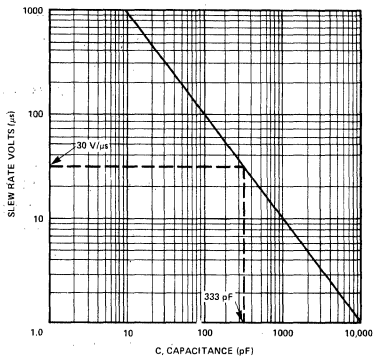


Figure 5-87

PROTECTION FROM POWER SUPPLY MALFUNCTION

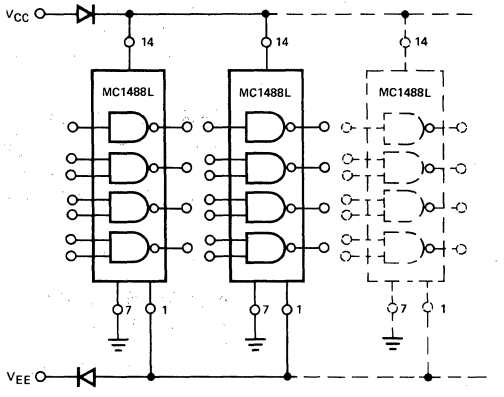


Figure 5-88

LEVEL SHIFTERS
- TTL-to-MOS
- MOS-to-TTL

SIGNAL COMPARISON
- In-Phase Logic Detector

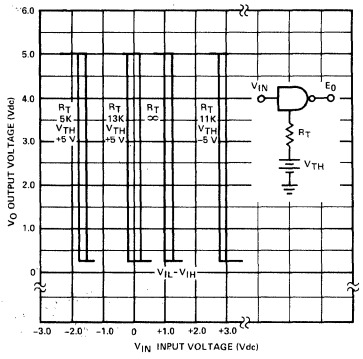
SIGNAL GENERATION
- Square Wave Generator

TIMING
- Dual Channel One Shot
- Two Phase MOS Clock Driver

Basic Requirements for a Peripheral Driver

- Input Logic Compatibility
- High Output Current/High Voltage Compliance

HYSTERESIS AS A FUNCTION OF PROGRAMMING RESISTANCE



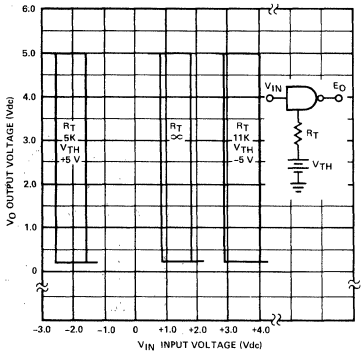


Figure 5-89

PERIPHERAL DRIVER

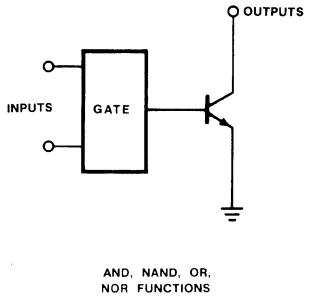


Figure 5-90

- High Speed
- Application Versatility

Other Requirements Include:

- Compatability with popular supply voltages
- Medium to high power capability
- Economical packaging
- Good pin arrangement

A peripheral driver has two basic building blocks:

(See Figure 5-90)

1. TTL gate
2. Discrete transistor with good output drive capabilities

DARLINGTON TRANSISTOR ARRAYS

Darlington Transistor Arrays are high voltage, high current arrays comprised of seven silicon npn Darlington pairs on a common monolithic substrate.

ULN 2001 Series

The ULN 2001 Series features

- General purpose (DTL, TTL, PMOS, CMOS)
- High current: 500mA continuous
- High voltage: VCE = 50V
- Output suppression diodes
- Fast switching: 1μs typ.
  5μs max.
- Open collector outputs

NE 5501 Series

The NE 5501 Series features are the same as the ULN 2001 Series with the following exceptions:

- High voltage: VCE = 90V
- High current: 350mA continuous

DEVICE	FEATURES
75450B 75451B 75452B DS3611 DS3612 DS3613 DS3614 UDN5711 UDN5712 UDN5713 UDN5714	30 volt breakdown, 24-35ns switching, choise of logic function, 300mA output 80 volt breakdown 100-300ns switching speed, 300mA output Same as DS3611 series with the addition of output suppression diodes
ULN2001 ULN2002 ULN2003 ULN2004	General purpose Darlington NPN Transistor arrays 50 volt breakdown 500mA output Output suppression diodes
NE5501 NE5502 NE5503 NE5504	Same as ULN 2001 series except for 90 volt breakdown, and 350mA output

TABLE 5-7 PERIPHERAL DRIVER PRODUCTS

Typical Applications

P-MOS TO LOAD ULN 2002

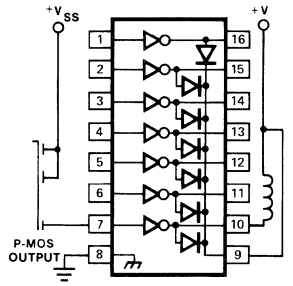


Figure 5-91

TTL TO LOAD ULN 2003

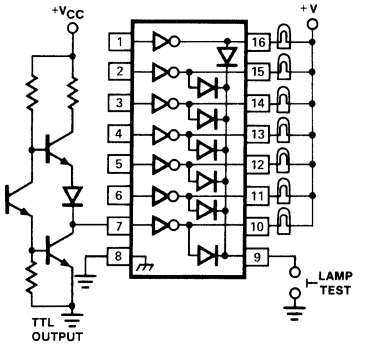


Figure 5-92

BUFFER FOR HIGHER CURRENT LOADS ULN2004

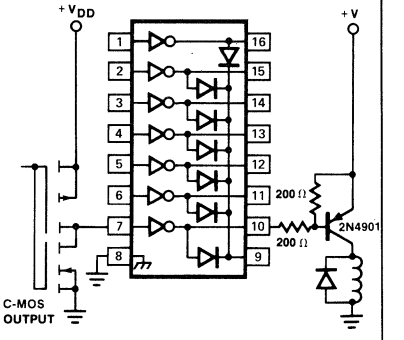


Figure 5-93

SECTION 23
TIMERS

INTRODUCTION

In mid 1972, Signetics introduced the 555 timer, a unique functional building block that has enjoyed unprecedented popularity. The timer's success can be attributed to several inherent characteristics foremost of which are versatility, stability and low cost. There can be no doubt that the 555 timer has altered the course of the electronics industry with an impact not unlike that of the I.C. operational amplifier.

The simplicity of the timer in conjunction with its ability to produce long time delays in a variety of applications has lured many designers from mechanical timers, op amps, and various discrete circuits into the ever increasing ranks of timer users.

DESCRIPTION

The 555 timer consists of two voltage comparators, a bistable flip-flop, a discharge transistor, and a resistor divider network. To understand the basic concept of the timer let's first examine the timer in block form as in Figure 6-1.

555/556 TIMER FUNCTIONAL BLOCK DIAGRAM

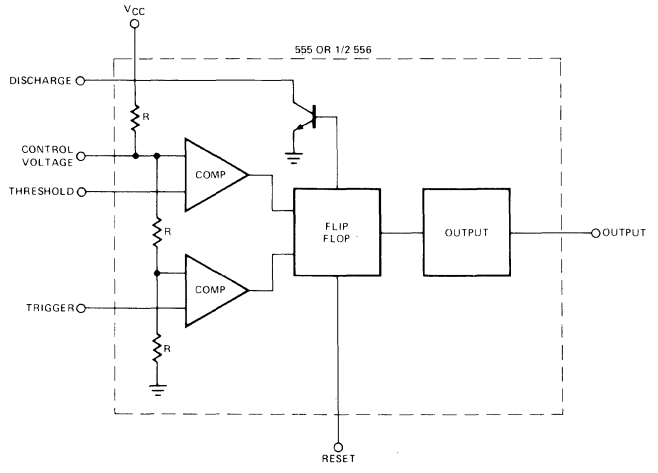


Figure 6-1

The resistive divider network is used to set the comparator levels. Since all three resistors are of equal value, the threshold comparator is referenced internally at 2/3 of supply voltage level and the trigger comparator is referenced at 1/3 of supply voltage. The outputs of the comparators are tied to the bistable flip-flop. When the trigger voltage is moved below 1/3 of the supply, the comparator changes state and sets the flip-flop driving the output to a high state. The threshold pin normally monitors the capacitor voltage of the RC timing network When the capacitor voltage exceeds 2/3 of the supply, the threshold comparator resets the flip-flop which in turn drives the output to a low state. When the output is in a low state, the discharge transistor is "on", hereby discharging the external timing capacitor. Once the capacitor is discharged, the timer will await another trigger pulse, the timing cycle having been completed.

The 555 and its complement, the 556 Dual Timer, exhibit a typical initial timing accuracy of 1% with a 50ppm/°C timing drift with temperature. To operate the timer as a one shot, only two external components are necessary; resistance & capacitance. For an oscillator, only one additional resistor is necessary. By proper selection of external components, oscillating frequencies from one cycle per half hour to 500KHz can be realized. Duty cycles can be adjusted from less than one percent to 99 percent over the frequency spectrum. Voltage control of timing and oscillation functions is also available,

Timer Circuitry

The timer is comprised of five distinct circuits; two voltage comparators, a resistive voltage divider reference, a bistable flip-flop, a discharge transistor, and an output stage that is the "totem pole" design for sink or source capability. Q_{10} - Q_{13} comprise a Darlington differential pair which serves as a trigger comparator. Starting with a positive voltage on the trigger; Q_{10} and Q_{11} turn on when the voltage at pin 2 is moved below one third of the supply voltage. The voltage level is derived from a resistive divider chain consisting of R_7, R_8 and R_9. All three resistors are of equal value (5K ohms). At fifteen volts supply, the triggering level would be five volts. When Q_{10} and Q_{11} turn on, they provide a base drive for Q_{15}, turning it on. Q_{16} and Q_{17} form a bistable flip-flop. When Q_{15} is saturated, Q_{16} is 'off' and Q_{17} is saturated. Q_{16} and Q_{17} will remain in these states even if the trigger is removed and Q_{15} is turned 'off'. While Q_{17} is saturated, Q_{20} and Q_{14} are turned off.

The output structure of the timer is a "totem pole"design, with Q_{22} and Q_{24} being large geometry transistors capable of providing 200mA with a fifteen volt supply. While Q_{20} is 'off', base drive is provided for Q_{22} by Q_{21}, thus providing a high output.

For the duration that the output is in a high state, the discharge transistor is 'off'. Since the collector of Q_{14} is typically connected to the external timing capacitor, C, while Q_{14} is off the timing capacitor now can charge thru the timing resistor, R_A.

The capacitor voltage is monitored by the threshold comparator (Q_1 - Q_4) which is a Darlington differential pair. When the capacitor voltage reaches two thirds of the supply voltage, the current is directed from Q_3 and Q_4 thru Q_1 and Q_2. Amplification of the current change is provided by Q_5 and Q_6. Q_5 - Q_6 and Q_7 - Q_8 comprise a diode-biased amplifier. The amplified current change from Q_6 now provides a base drive for Q_{16} which is part of the bistable flip-flop to change states. In doing so, the output is driven "low", and Q_{14} the discharge transistor is turned "on" shorting the timing capacitor to ground.

The discussion to this point has only encompassed the most fundamental of the timer's operating modes and circuitry. Several points of the circuit are brought out to the real world which allow the timer to function in a variety of modes. It is important; more than that, it is essential that one understands all the variations possible in order to utilize this device to its fullest extent.

SCHEMATIC 555 OR 1/2 556 DUAL TIMER

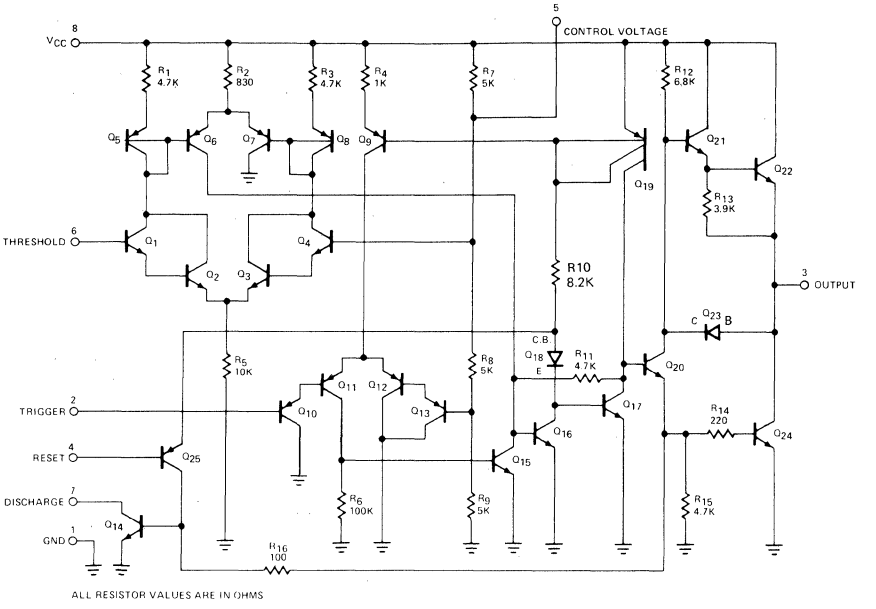


Figure 6-2

Reset Function

Regressing to the trigger mode, it should be noted that once the device has triggered and the bistable flip-flop set, continued triggering will not interfere with the timing cycle. However, there may come a time when it is necessary to interrupt or halt a timing cycle. This is the function that the reset accomplishes.

In the normal operating mode the reset transistor, Q_{25}, is off with its base held high. When the base of Q_{25} is grounded, it turns on, providing base drive to Q_{14}, turning it on. This discharges the timing capacitor, resets the flip-flop at Q_{17}, and drives the output low. The reset overrides all other functions within the timer.

Trigger Requirements

Due to the nature of the trigger circuitry, the timer will trigger on the negative going edge of the input pulse. For the device to time out properly, it is necessary that the trigger voltage level be returned to some voltage greater than one third of the supply before the time out period. This can be achieved by making either the trigger pulse sufficiently short or by AC coupling into the trigger. By AC coupling the trigger, see Figure 3, a short negative going pulse is achieved when the trigger signal goes to ground. AC coupling is most frequently used in conjunction with a switch or a signal that goes to ground which initiates the timing cycle. Should the trigger be held low, without AC coupling, for a longer duration than the timing cycle the output will remain in a high state for the duration of the low trigger signal, without regard to the threshold comparator state. This is due to the predominance of Q_{15} on the base of Q_{16}, controlling the state of the bistable flip-flop. When the trigger signal then returns to a high level, the output will fall immediately. Thus, the output signal will follow the trigger signal in this case.

Control Voltage

One additional point of significance, the control voltage, is brought out on the timer. As mentioned earlier, both the trigger comparator, Q_{10} - Q_{13}, and the threshold comparator, Q_1 - Q_4, are referenced to an internal resistor divider network, R_7, R_8, R_9. This network establishes the nominal two thirds of supply voltage (Vcc) trip point for the threshold comparator and one third of

AC COUPLING OF THE TRIGGER PULSE

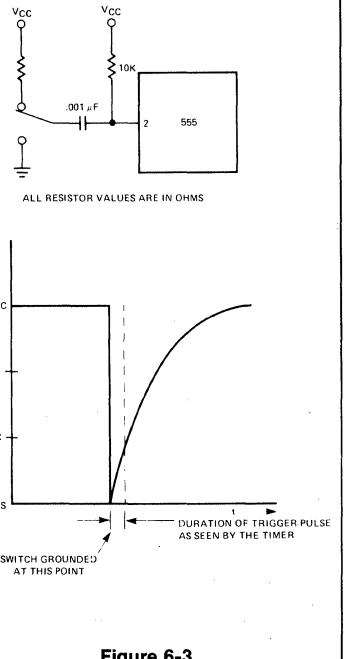


Figure 6-3

Vcc for the trigger comparator. The two thirds point at the junction of R_7, R_8 and the base of Q_4 is brought out. By imposing a voltage at this point, the comparator reference levels may be shifted either higher or lower than the nominal levels of one third and two thirds of the supply voltage. Varying the voltage at this point will vary the timing. This feature of the timer opens a multitude of application possibilities such as using the timer as a voltage controlled oscillator, pulse width modulator, etc. For applications where the control voltage function is not used, it is strongly recommended that a bypass capacitor (.01μF) be place across the control voltage pin and ground. This will increase the noise immunity of the timer to high frequency trash which may monitor the threshold levels causing timing error.

Monostable Operation

The timer lends itself to three basic operating modes:

1. Monostable (one shot)
2. Astable (oscillatory)
3. Time delay

By utilizing any one or combination of basic operating modes and suitable variations it is possible to utilize the timer in a myriad of applications. The applications are limited only to the imagination of the designer.

One of the simplest and most widely used operating modes of the timer is the monostable (one shot). This configuration requires only two external components for operation (See Figure 6-4). The sequence of events starts when a voltage below one third Vcc is sensed by the trigger comparator. The trigger is normally applied in the form of a short negative going pulse. On the negative going edge of the pulse, the device triggers, the output goes high and the discharge transistor turns off. Note that prior to the input pulse, the discharge transistor is on, shorting the timing capacitor to ground. At this point the timing capacitor, C, starts charging thru the timing resistor, R. The voltage on the capacitor increases exponentially with a time constant T = RC. Ignoring capacitor leakage, the capacitor will reach the two thirds Vcc level in 1.1 time constants or

$$T = 1.1\ RC$$

where T is in seconds; R is in ohms and; C is in Farads. This voltage level trips the threshold comparator, which in turn drives the output low and turns on the discharge transistor. The transistor discharges the capacitor, C, rapidly. The timer has completed its cycle and will now await another trigger pulse.

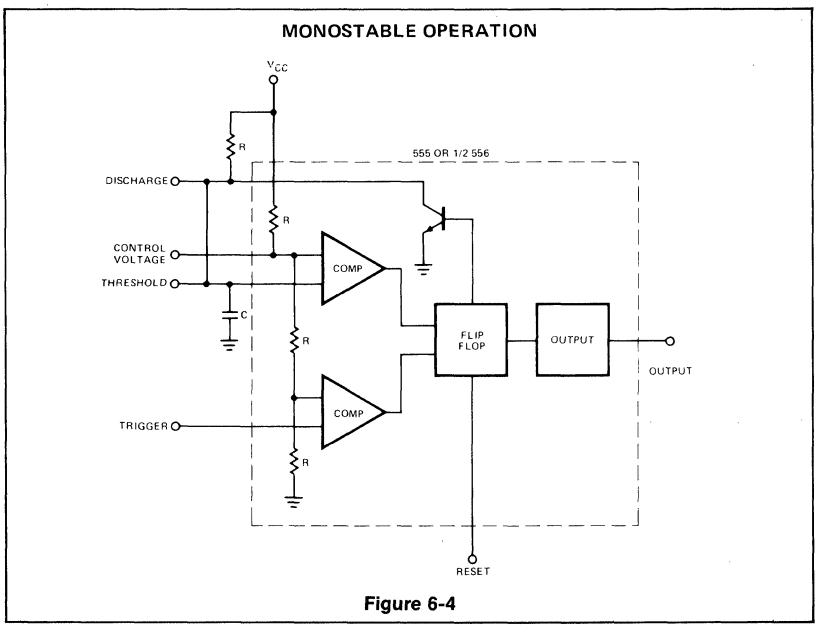


Figure 6-4

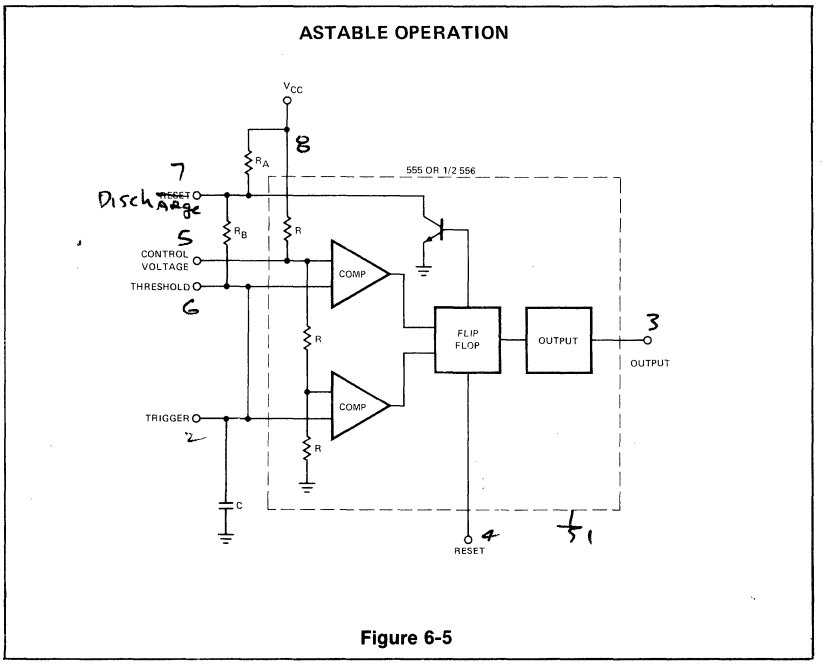


Figure 6-5

Astable Operation

In the astable (free run) mode, only one additional component, Rb is necessary. The trigger is now tied to the threshold pin. At power up, the capacitor is discharged, holding the trigger low. This triggers the timer, which establishes the capacitor charge path thru R_A and R_B. When the capacitor reaches the threshold level of 2/3 Vcc, the output drops low and the discharge transistor turns on.

$R = \frac{T}{1.1C}$

The timing capacitor now discharges thru R_B. When the capacitor voltage drops to 1/3 Vcc, the trigger comparator trips, automatically retriggering the timer, creating an oscillator whose frequency is given by:

$$f = \frac{1.49}{(R_A + 2R_B)\ C}$$

Selecting the ratios or R_A and R_B varies the duty cycle accordingly. Lo and behold, we have a problem. If a duty cycle of less than fifty percent is required, then what? Even if $R_A = 0$, the charge time cannot be made smaller than the discharge time because the charge path is $R_A + R_B$ while the discharge path is R_B alone. In this case it becomes necessary to insert a diode in parallel with R_B, cathode toward the timing capacitor. Another diode is desireable, but not mandatory, this one in series with R_B, cathode away from the timing capacitor. Now the charge path becomes R_A, thru the parallel diode into C. Discharge is thru the series diode and R_B to the discharge transistor. This scheme will afford a duty cycle range from less than 5% to greater than 95%. It should be noted that for reliable operation a minimum value of 3KΩ for R_B is recommended to assure that oscillation begins.

METHOD OF ACHIEVING DUTY CYCLES LESS THAN 50%

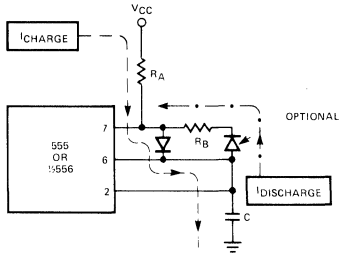


Figure 6-6

Time Delay

In this third basic operating mode, we aim to accomplish something a little different from monostable operation. In the monostable mode, when a trigger was applied, the output immediately changed to the high state, timed out, and returned to its pre-trigger low state. in the time delay mode, we require the output not to change state upon triggering, but at some precalculated time after trigger is received.

TIME DELAY OPERATION

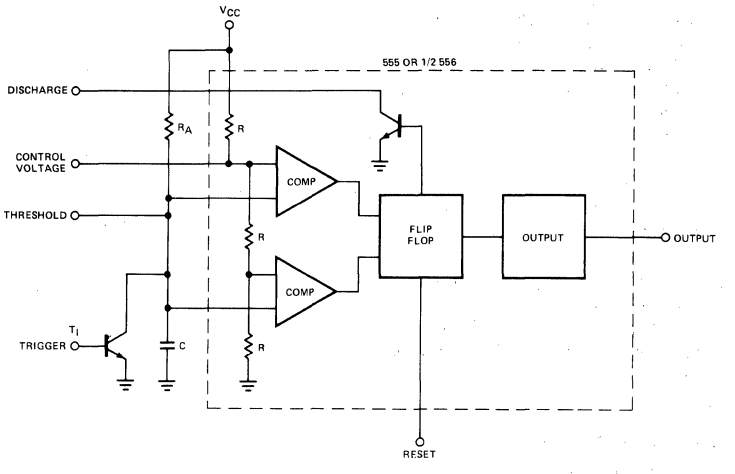


Figure 6-7

The threshold and trigger are tied together monitoring the capacitor voltage. The discharge function is not used. The operation sequence begins as transistor (T_1) is turned on, keeping the capacitor grounded. The trigger sees a low state and forces the timer output high. When the transistor is turned off the capacitor commences its charge cycle. When the capacitor reaches the threshold level, then and only then does the output change from its normally high state to the low state. The output will remain low until T_1 is again turned on.

GENERAL DESIGN CONSIDERATIONS

The timer will operate over a guaranteed voltage range of 4.5 volts to 15 volts DC, with 16 VDC being the absolute max. rating. Most of the devices, however, will operate at voltage levels as low as 3 VDC. The timing interval is independent of supply voltage since the charge rate and threshold level of the comparator are both directly proportional to supply. The supply volatage may be provided by any number of sources: however, several precautions should be taken. The most important, the one which provides the most headaches if not practiced, is good power supply filtering and adequate bypassing. Ripple on the supply line can cause loss of timing accuracy. The threshold level shifts causing a change of charging current. This will cause a timing error for that cycle.

Due to the nature of the output structure, a high power totem pole design, the output of the timer can exhibit large current spikes on the supply line. Bypassing is necessary to eliminate this phenomenon. A capacitor across the Vcc and ground, ideally, directly across the device is necessary. The size of capacitor will depend on the specific application. Values of capacitance from .01μF to 10μF are not uncommon. Note that the bypass capacitor would be as close to the device as physically possible.

Selecting External Components

In selecting the timing resistor and capacitor, there are several considerations to be taken into account.

Stable external components are necessary for the RC network if good timing accuracy is to be maintained. The timing resistor(s) should be of the metal film variety if timing accuracy and repeatability are important design criteria. The timer exhibits a typical initial accuracy of one percent. That is, with any one RC network, from timer to timer only one percent change is to be expected. Most of the initial timing error (i.e. deviation from the formula) is due to inaccuracies of external components. Resistors range from their rated values by .01% to 10 and 20 percent. Capacitors may have a 5 to 10 percent deviation from rated capacity. Therefore, in a

system where timing is critical, an adjustable timing resistor or precision components are necessary. For best results, a good quality trim pot, placed in series with the largest feasible resistance will allow for best adjustability and performance.

The timing capacitor should be a high quality, stable component with very low leakage characteristics. *Under no circumstances should ceramic disc capacitors be used in the timing network!* Ceramic disc capacitors are not sufficiently stable in capacitance to operate properly in an RC mode. Several acceptable capacitor types are: silver mica, mylar, polycarbonate, polystyrene, tantulum or similar types.

The timer typically exhibits a small negative temperature coefficient (50ppm/°C). If timer accuracy over temperature is a consideration, timing components with a small positive temperature coefficient should be chosen. This combination will tend to cancel timing drift due to temperature.

In selecting the values for the timing resistors and capacitor, several points should be considered. A minimum value of threshold current is necessary to trip the threshold comparator. This value is .25μA. To calculate the maximum value of resistance, keep in mind that at the time the threshold current is required, the voltage potential on the threshold pin is two thirds of supply. Therefore:

$$V\text{potential} = V_{CC} - V\text{capacitor}$$

$$V\text{potential} = V_{CC} - 2/3\ V_{CC} = 1/3\ V_{CC}$$

Maximum resistance is then defined as

$$R_{max} = \frac{V_{CC} - V_{cap}}{I_{thresh}}$$

Example: $V_{CC} = 15V$

$$R_{max} = \frac{15 - 10}{.25\ (10{-}6)} = 20M\Omega$$

$V_{CC} = 5V$

$$R_{max} = \frac{5 - 3.33}{.25\ (10{-}6)} \qquad 6.6M\Omega$$

NOTE: If using a large value of timing resistor, be certain that the capacitor leakage is significantly lower than the charging current available to minimize timing error.

On the other end of the spectrum, there are certain minimum values of resistance that should be observed. The discharge transistor, Q_{14}, is current limited at 35mA to 55mA internally. Thus, at the current limiting values, Q_{14}, establishes high saturation voltages. When examining the currents at Q_{14}, remember that the transistor, when turned on will be carrying two current loads. The first being the constant current thru timing resistor, R_A. The second will be the varying discharge current from the timing capacitor. To provide best operation the current contributed by the R_A path should be minimized so that the majority of discharge current can be used to reset the capacitor voltage. Hence it is recommended that a 5K ohm value be the minimum feasible value for R_A. This does not mean lower values cannot be used successfully in certain applications. Yet there are extreme cases that should be avoided if at all possible.

Capacitor size has not proven to be a legitimate design criteria. Values ranging from picofarads to greater than one thousand microfarads have been used successfully. One precaution need be utilized though. (It should be a cardinal rule that applies to the usage of all I C's.) Make certain that the package power dissipation is not exceeded. With extremely large capacitor values, a maximum duty cycle which allows some cooling time for the discharge transistor, may be necessary.

The most important characteristic of the capacitor should be as low a leakage as possible. Obviously any leakage will subtract from the charge count causing the calculated time to be longer than anticipated.

Control Voltage

Regressing momentarily, we recall that the control voltage pin is connected directly to the threshold comparator at the junction of R_7, or R_8. The combination of R_7, R_8 and R_9 comprise the resistive voltage divider network that establishes the nominal 1/3 Vcc trigger comparator level (junction R_8, R_9) and the 2/3 Vcc level for the threshold comparator (junction R_7, R_8).

For most applications, the control voltage function is not used and therefore is bypassed to ground with a small capacitor for noise filtering. The control voltage function, in other applications becomes an integral part of the design. By imposing a voltage at this pin, it becomes possible to vary the threshold comparator "set" level above or below the 2/3 Vcc nominal, hereby varying the timing. In the monostable mode, the control voltage may be varied from 45 percent to 90 percent of Vcc. The 45 to 90 percent figure is not firm, but only an indication to a safe usage. Control voltage levels below and above those stated have been used successfully in some applications.

In the oscillatory (free run) mode, the control voltage limitations are from 1.7 volts to Vcc. These values should be heeded for reliable operation. Keep in mind that in this mode the trigger level is also important. When the control voltage raises the threshold comparator level it also raise the trigger comparator level by one half that amount due to R_8 and R_9 of Figure 2. As a voltage controlled oscillator, one can expect ±25% around center frequency (f_o) to be virtually linear with a normal RC timing circuit. For wider linear variations around F_o it may be desireable to replace the charging resistor with a constant current source. In this manner the exponential charging characteristics of the classical configuration will be altered to linear charge time.

Reset Control

The only remaining function now is the reset. As mentioned earlier, the reset, when taken to ground, inhibits all device functioning. The output is driven low, the bistable flip-flop is reset, and the timing capacitor is discharged. In the astable (oscillatory) mode, the reset can be used to gate the oscillator. In the monostable it can be used as a timing abort to either interrupt a timing sequence or establish a standby mode (i.e. — device off during power up). It can also be used in conjunction with the trigger pin to establish a positive edge triggered circuit as opposed to the normal negative edge trigger mode. One thing to keep in mind when using the reset function is that the reset voltage (switching) point is between 0.4V and 1.0V (min/max). Therefore, if used in conjunction with the trigger, the device will be out of the reset mode prior to reaching 1 volt. At that point the trigger is in the "turn on" region, below 1/3 Vcc. This will cause the device to trigger immediately, effectively triggering on the positive going edge if a pulse is applied to pins 4 and 2 simultaneously.

FREQUENTLY ASKED APPLICATIONS QUESTIONS

The following is a harvest of various maladies, exceptions, and idiosyncracies that may exhibit themselves from time

to time in various applications. Rather than cast aspersions, a quick review of this list may uncover a solution to the problem at hand.

1. In the oscillator mode when reset is released the *first time constant* is approximately *twice as long as the rest.* Why?

   Answer: In the oscillator mode the capacitor voltage fluctuates between 1/3 and 2/3 of the supply voltage. When reset is pulled down the capacitor discharges completely. Thus for the first cycle it must charge from ground to 2/3 Vcc which takes twice as long.

2. What is *maximum frequency of oscillations?*

   Answer: Most devices will oscillate about 1M Hz. However, in the interest of temperature stability one should operate only up to about 500kHz.

3. What is *temperature drift* for *oscillator mode?*

   Answer: Temperature drift of oscillator mode is 3 times that of one shot mode due to addition of second voltage comparator. Frequency always increases with an increasing temperature. Therefore it is possible to partially offset this drift with an offsetting temperature coefficient in the external resistor/capacitor combination.

4. Oscillator exhibits spurious *oscillations on cross over points.* Why?

   Answer: The 555 can oscillate due to feedback from power supply. Always bypass with sufficient capacitance close to the device for all applications.

5. Trying to drive a *relay* but 555 *hangs up.* How come?

   Answer: Inductive feedback. A clamp diode across the coil prevents the coil from driving pin 3 below a negative .6 volts. This negative voltage is sufficient in some cases to cause the timer to malfunction. The solution is to drive the relay through a diode thus preventing pin 3 from ever seeing a negative voltage.

6. Double triggering of the TTL loads sometimes occurs. Why?

   Answer: Due to the high current capability and fast rise and fall times of the output a totem pole structure different from the TTL classical structure was used. Near TTL threshold this output exhibits a cross over distortion which may double trigger logic. A 1000 pF capacitor from the output to ground will eliminate any false triggering.

7. What is the longest time I can get out of the timer?

   Answer: Times exceeding an hour are possible, but not always practical. Large capacitors with low leakage specs are quite expensive. It becomes cheaper to use a countdown scheme (see Figure 15) at some point dependent on required accuracy. Normally 20 to 30 min. is the longest feasible time.

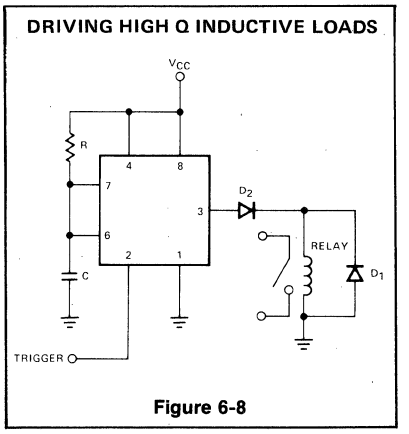
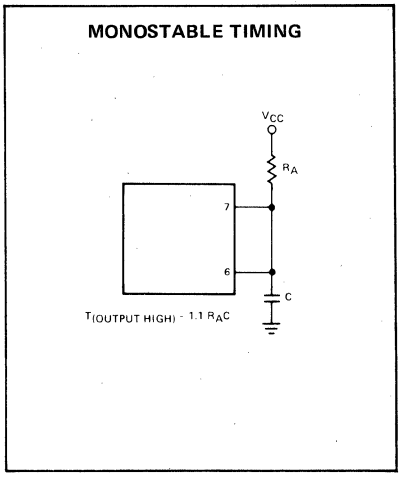
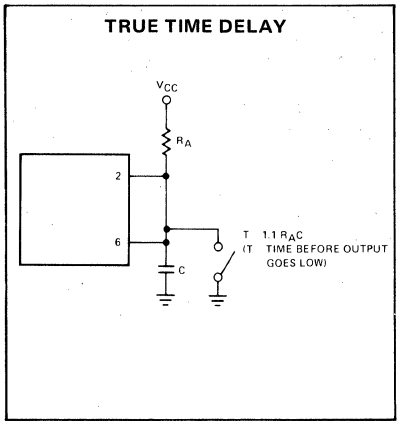


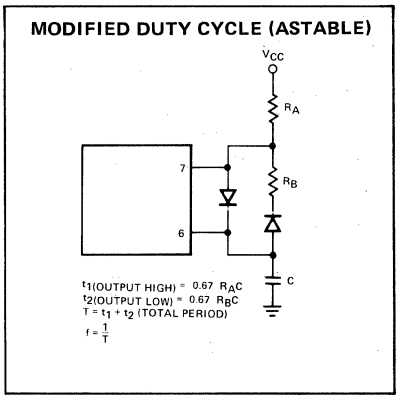
Figure 6-8

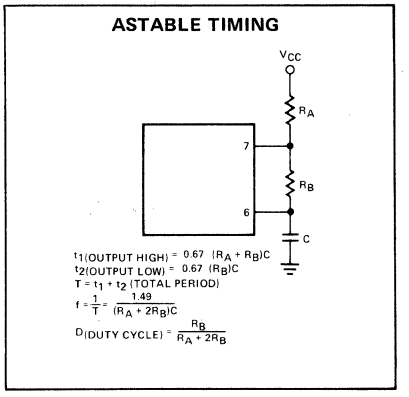
DESIGN FORMULAS

Before entering the section on specific applications it is advantageous to review the timing formulas. The formulas given here apply to the 555 and 556 devices.









APPLICATIONS

The timer since introduction has spurred the imagination of thousands. Thus the ways in which this device has been used are far too numerous to present each one. A review of the basic operation and basic modes has previously been given. Presented here are some ingenious applications devised by our applications engineers and by some of our customers.

Missing Pulse Detector

Using the circuit of Figure 6-9a, the timing cycle is continuously reset by the input pulse train. A change in frequency, or a missing pulse, allows completion of the timing cycle which causes a change in the output level. For this application, the time delay should be set to be slightly longer than the normal time between pulses. Figure 6-9b shows the actual waveforms seen in this mode of operation.

SCHEMATIC DIAGRAM

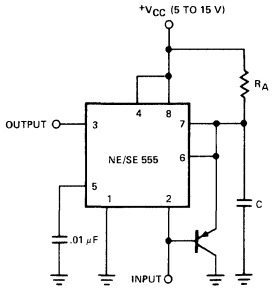


Figure 6-9a

EXPECTED WAVE FORMS

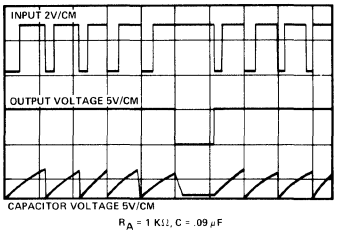


Figure 6-9b

If the input frequency is known, the timer can easily be used as a frequency divider by adjusting the length of the timing cycle.

Frequency Divider

SCHEMATIC DIAGRAM

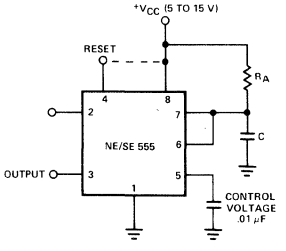


Figure 6-10a

EXPECTED WAVE FORMS

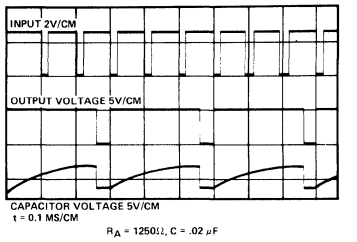


Figure 6-10b

Figure 6-10b shows the waveforms of the timer in Figure 6-10a when used as a divide by three circuit. This application makes use of the fact that this circuit cannot be retriggered during the timing cycle.

Pulse Width Modulation (PWM)

In this application, the timer is connected in the monostable mode as shown in Figure 6-11a. The circuit is triggered with a continuous pulse train and the threshold voltage is modulated by the signal applied to the control voltage terminal (pin 5). This has the effect of modulating the pulse width as the control voltage varies. Figure 6-11b shows the actual waveform generated with this circuit.

DEVICE SCHEMATIC

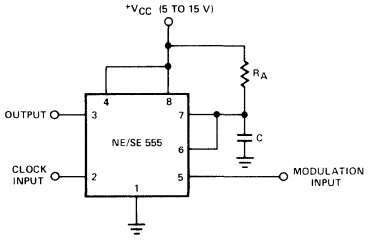


Figure 6-11a

EXPECTED WAVE FORMS

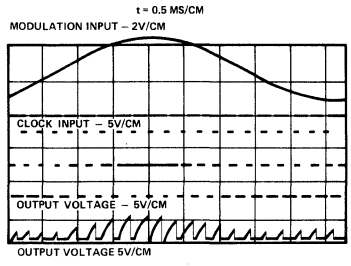


Figure 6-11b

Pulse Position Modulation (PPM)

This application uses the timer connected for astable (free-running) operation, Figure 6-12a, with a modulating signal again applied to the control voltage terminal. Now the pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. Figure 6-12b shows the waveform generated for triangle wave modulation signal.

SCHEMATIC DIAGRAMS

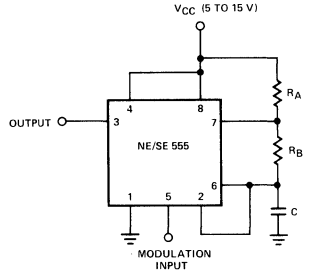


Figure 6-12a

EXPECTED WAVE FORMS

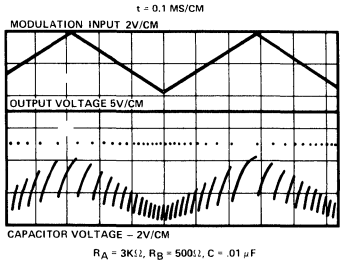


Figure 6-12b

TONE BURST GENERATOR

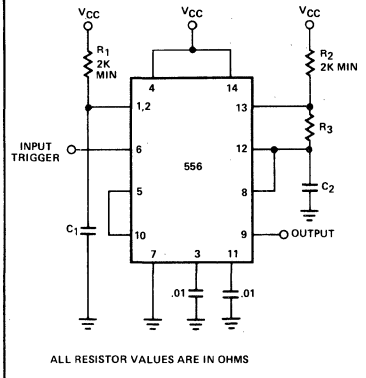


Figure 6-13

Tone Burst Generator

The 556 Dual Timer makes an excellent tone burst generator. The first half is connected as a one shot and the second half as an oscillator. (Figure 6-13)

The pulse established by the one shot turns on the oscillator allowing a burst to be generated.

Sequential Timing

One feature of the dual timer is that by utilizing both halves it is possible to obtain sequential timing. By connecting the output of the first half to the input of the second half via a .001μfd coupling capacitor sequential timing may be obtained. Delay t_1 is determined by the first half and t_2 by the second half delay. (Figure 6-14)

The first half of the timer is started by momentarily connecting pin 6 to ground. When it is timed out (determined by $1.1R_1C_1$) the second half begins. Its duration is determined by $1.1R_2C_2$.

SEQUENTIAL TIMER

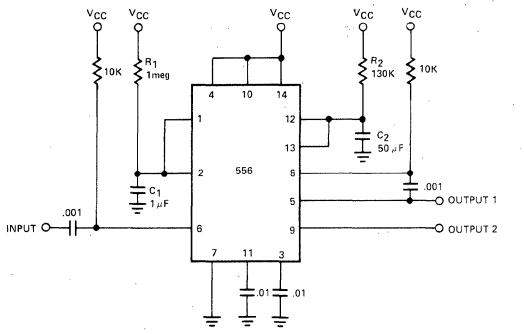


Figure 6-14

METHOD OF ACHIEVING LONG TIME DELAYS

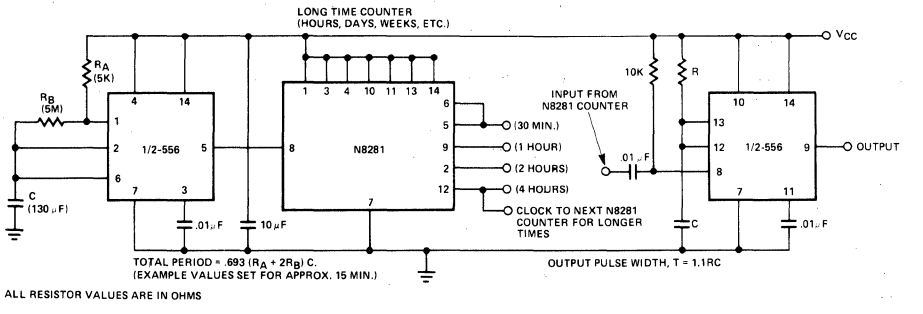


Figure 6-15

Long Time Delays

In the 556 timer the timing is a function of the charging rate of the external capacitor. For long time delays expensive capacitors with extremely low leakage are required. the practicality of the components involved limits the time between pulses to something in the neighborhood of twenty minutes.

To achieve longer time periods both halves may be connected in tandem with a "divide-by" network in between.

The first timer section operates in an oscillatory mode with a period of $1/f_o$. This signal is then applied to a "Divide-by-N" network to give an output with the period of N/f_o. This can then be used to trigger the second half of the 556. The total time is now a function of N and f_o (Figure 6-15).

Auto Burglar Alarm

This circuit utilizes the time delay mode of operation. When the arm/disarm switch is opened (normally closed) the exit timer starts its timing cycle. Pin 5 will go low after the exit time lapse to energize the alarm circuit. Door switches, when closed will keep the PNP transistor of: by keeping pin 9 high. When any door switch is opened, after a delay, the transistor will turn on sounding horn of the arm/disarm switch is not closed within the delay time (Figure 6-16).

Speed Warning Device (1)

Utilizing the "missing pulse detector" concept, a speed warning device, such as depicted, becomes a simple and inexpensive circuit (Figure 6-17a).

Car Tachometer (1)

The timer receives pulses from the distributor points. Meter M receives a calibrated current thru R6 when the timer output is high. After time out the meter receives no current for that part of the duty cycle. Integration of the variable duty cycle by the meter movement provides a visible indication of engine speed (Figure 6-18).

BURGLAR ALARM CIRCUIT

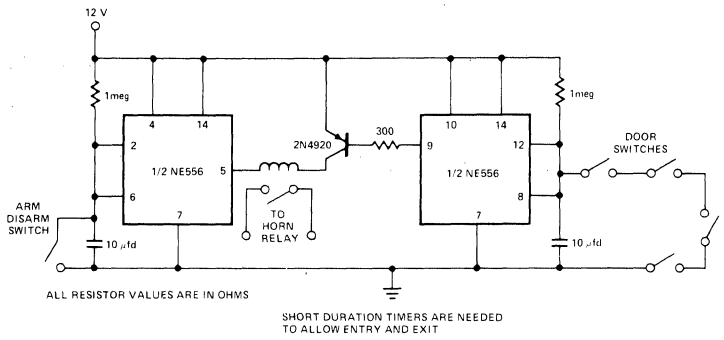


Figure 6-16

SCHEMATIC OF SPEED WARNING DEVICE

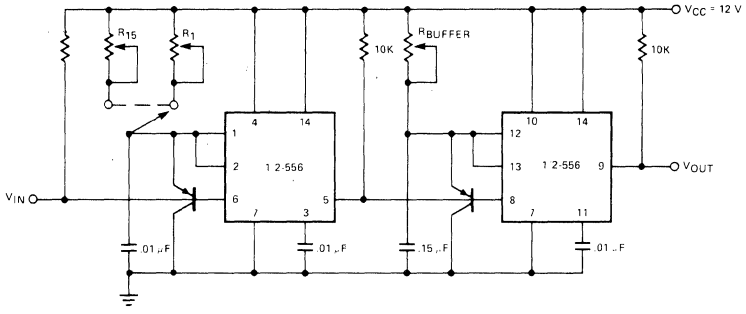


Figure 6-17a

OPERATING WAVE FORMS OF SPEED WARNING DEVICE

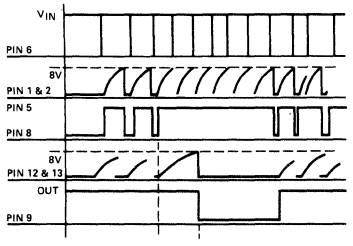


Figure 6-17b

TACHOMETER

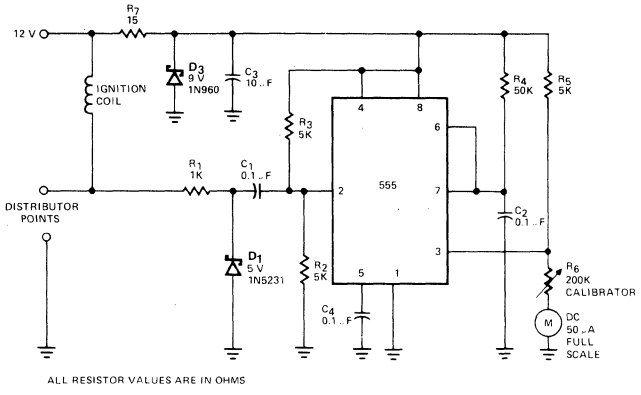


Figure 6-18

Oscilloscope Triggered Sweep

The 555 timer holds down the cost of adding a triggered sweep to an economy oscilloscope. The circuit's input op amp triggers the timer, setting its flip-flop and cutting off its discharge transistor so that capacitor C can charge. When capacitor voltage reaches the timer's control voltage (0.33Vcc), the flip-flop resets and the transistor conducts, discharging the capacitor (Figure 6-19).

Square Wave Tone Burst Generator (4)

Depressing the pushbutton provides square-wave tone bursts whose duration depends on the duration for which the voltage at pin 4 exceeds a threshold. Components R_1, R_2 and C_1 causes the astable action of the timer IC (Figure 6-20).

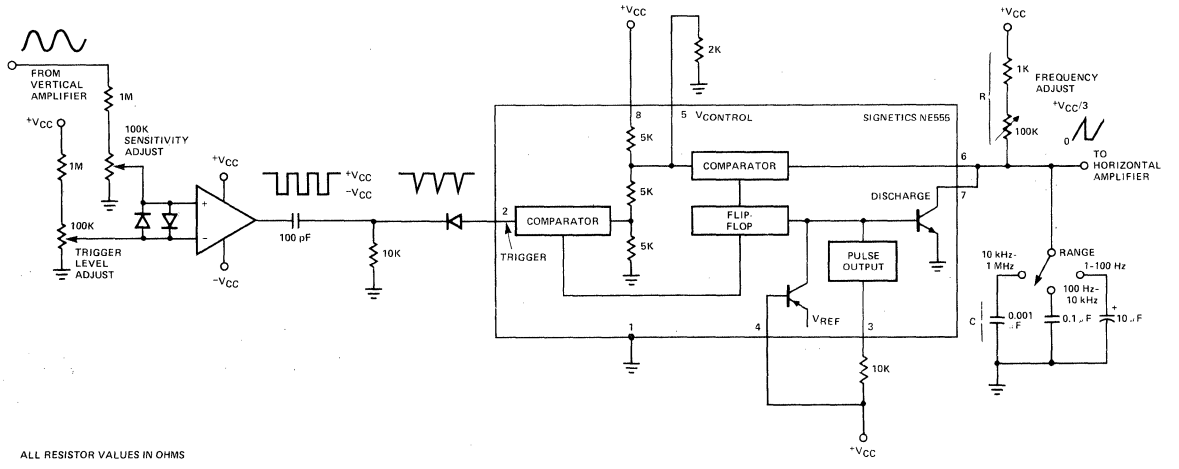
Regulated DC-to-DC Converter (2)

Regulated DC to DC converter produces 15V DC outputs from a +5V DC input. Line and load regulation is 0.1% (Figure 6-21).

Voltage to Pulse Duration Converter (1)

Voltage levels can be converted to pulse durations by combining an op amp and a timer IC. Accuracies to better than 1% can be obtained with this circuit (a) and the output signals (b) still retain the original frequency, independent of the input voltage (Figure 6-22).

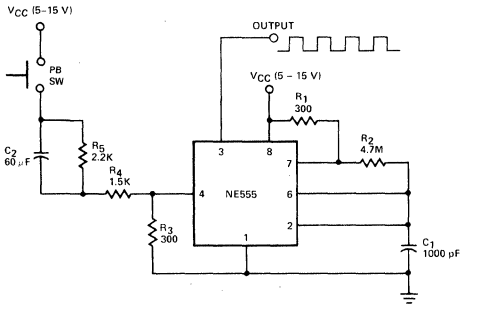
SCHEMATIC OF TRIGGERED SWEEP



ALL RESISTOR VALUES IN OHMS

Figure 6-19

SQUARE WAVE TONE BURST GENERATOR



ALL RESISTOR VALUES IN OHMS

Figure 6-20

REGULATED DC TO DC CONVERTER

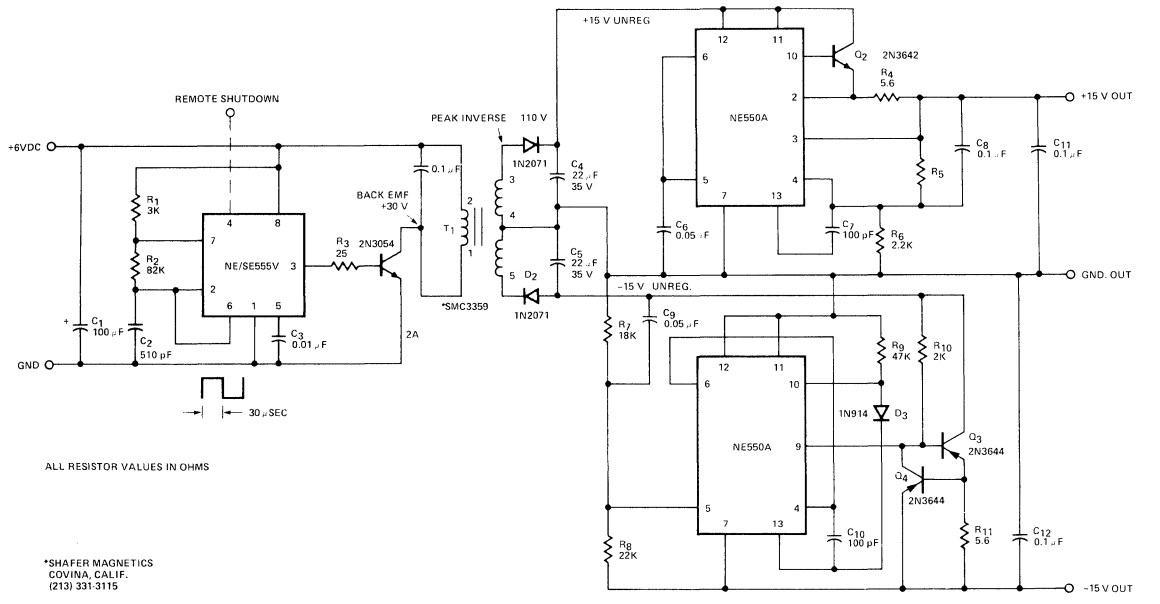


Figure 6-21

VOLTAGE-TO-PULSE-DURATION CONVERTER

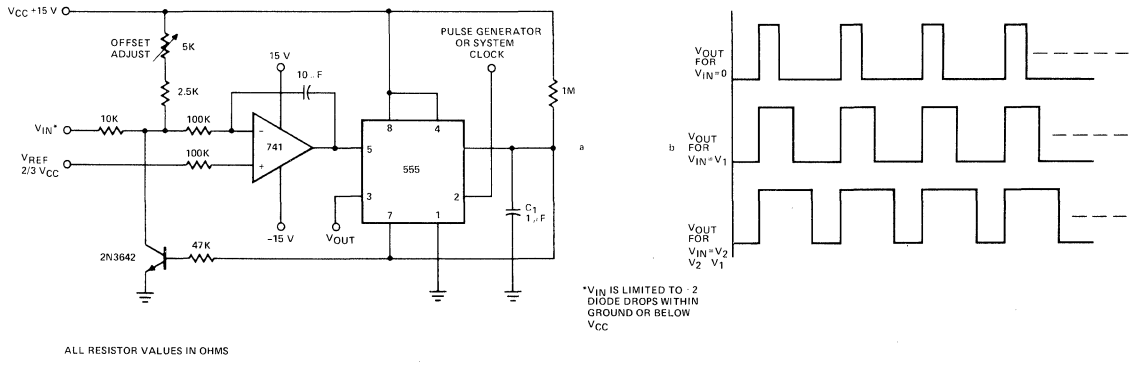


Figure 6-22

Servo System Controller (1)

To remoteley control a servo motor, the 555 needs only six extra components (Figure 6-23).

Stimulus Isolator (5)

Stimulus isolator uses a photo-SCR and a toroid for shaping pulses of up to 200V at 200μA (Figure 6-24).

Voltage to Frequency Converter (0.2% Accuracy) (6)

Linear voltage-to-frequency converter (a) achieves good linearity over the 0 to −10V. Its mirror image (b) provides the same linearity over the 0-to+10V range but is not DTL/TTL compatible (Figure 6-25a & b.)

SERVO SYSTEM CONTROLLER

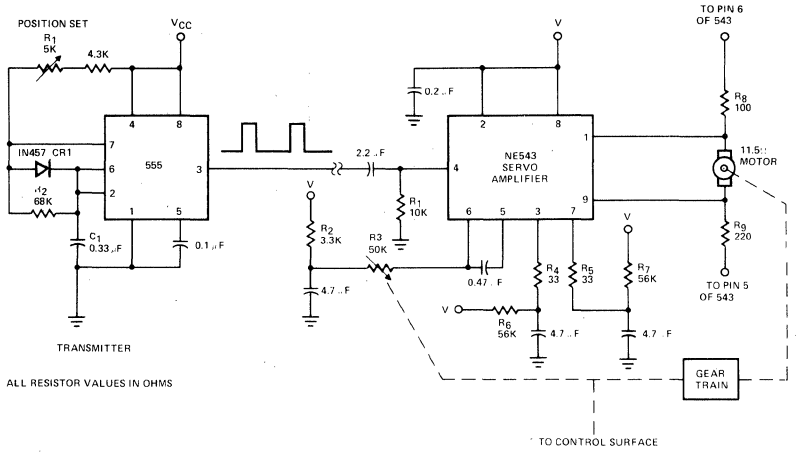


Figure 6-23

STIMULUS ISOLATOR

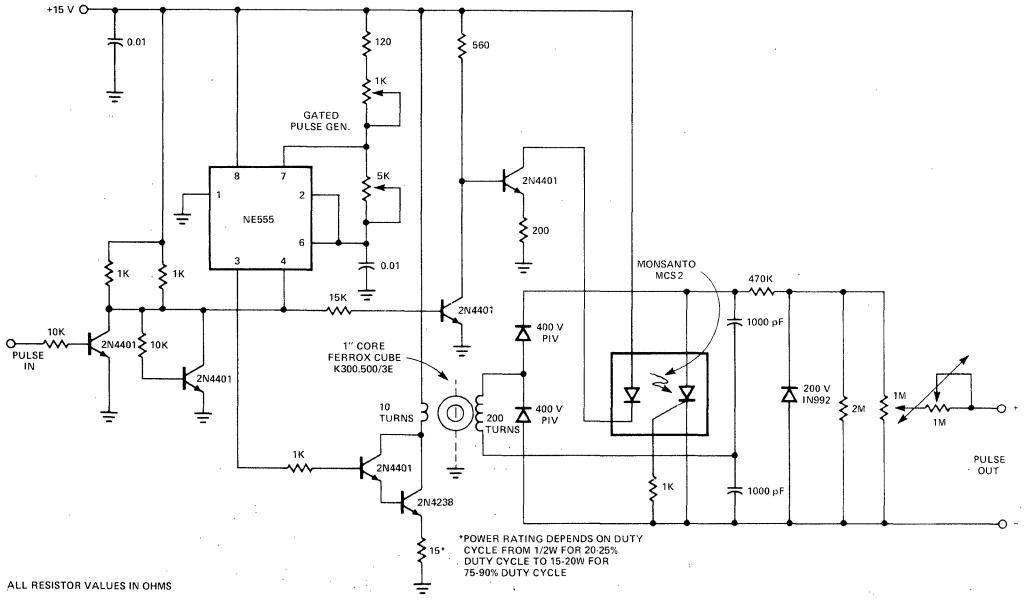


Figure 6-24

VOLTAGE-TO-FREQUENCY CONVERTER (0.2% ACCURACY)

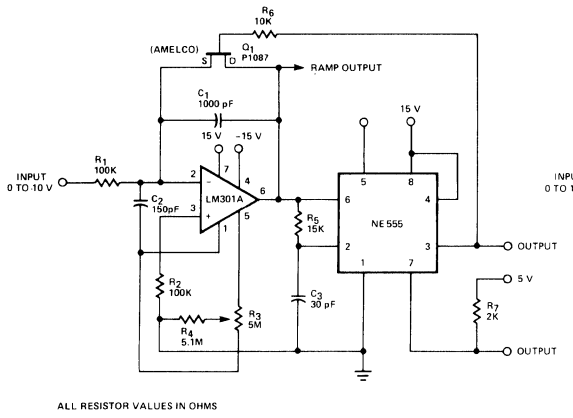


Figure 6-25a

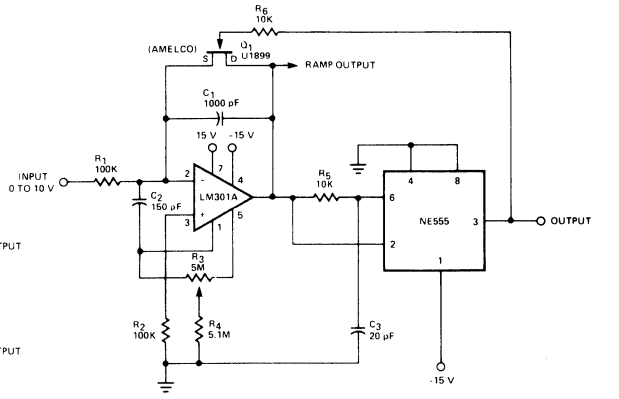


Figure 6-25b

Positive to Negative Converter (7)

Transformerless dc-dc converter derives a negative supply voltage from a positive. As a bonus the circuit also generates a clock signal.

The negative output voltage tracks the dc input voltage linearity (a), but its magnitude is about 3V lower, Application of a 500Ω load, (b), causes 10% change from the no-load value (Figure 6-26a, b, & c).

POSITIVE TO NEGATIVE CONVERTER

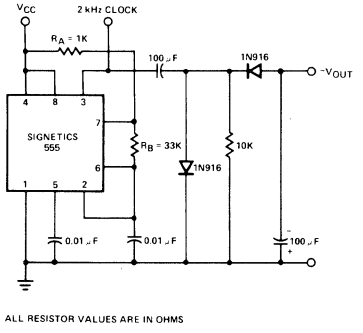


Figure 6-26a

Auto Burglar Alarm (8)

Timer A produces a safegaurd delay, allowing driver to disarm alarm and eliminating vulnerable outside control switch. The SCR prevents timer A from triggering timer B, unless timer B is triggered by strategically located sensor switches (Figure 6-27).

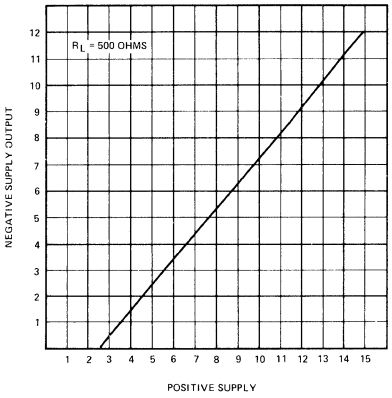


Figure 6-26b

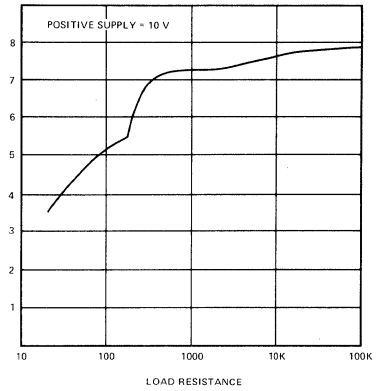


Figure 6-26c

Cable Tester (9)

Compact tester checks cables for open-cicuit or short-circuit conditions. A differential transistor pair at one end of each cable line remains balanced as long as the same clock pulse - generated by the timer IC - appears at both ends of the line. A clock pulse just at the clock end of the line lights green light-emitting diode, and a clock pulse only at the other end lights a red LED (Figure 6-28).

Low Cost Line Receiver (10)

The timer makes an excellent line receiver for control applications involving relatively slow electro-mechanical devices. It can work without special drivers over single unshielded lines (Figure 6-29).

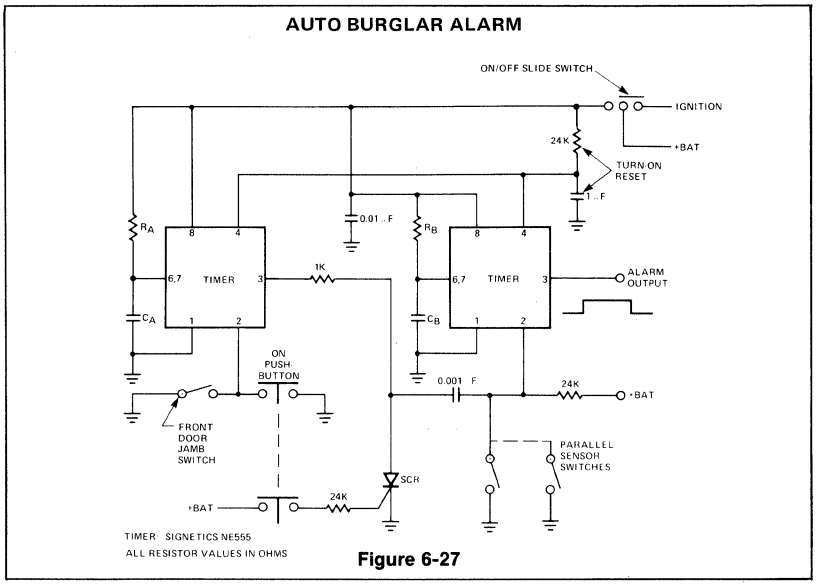


Figure 6-27

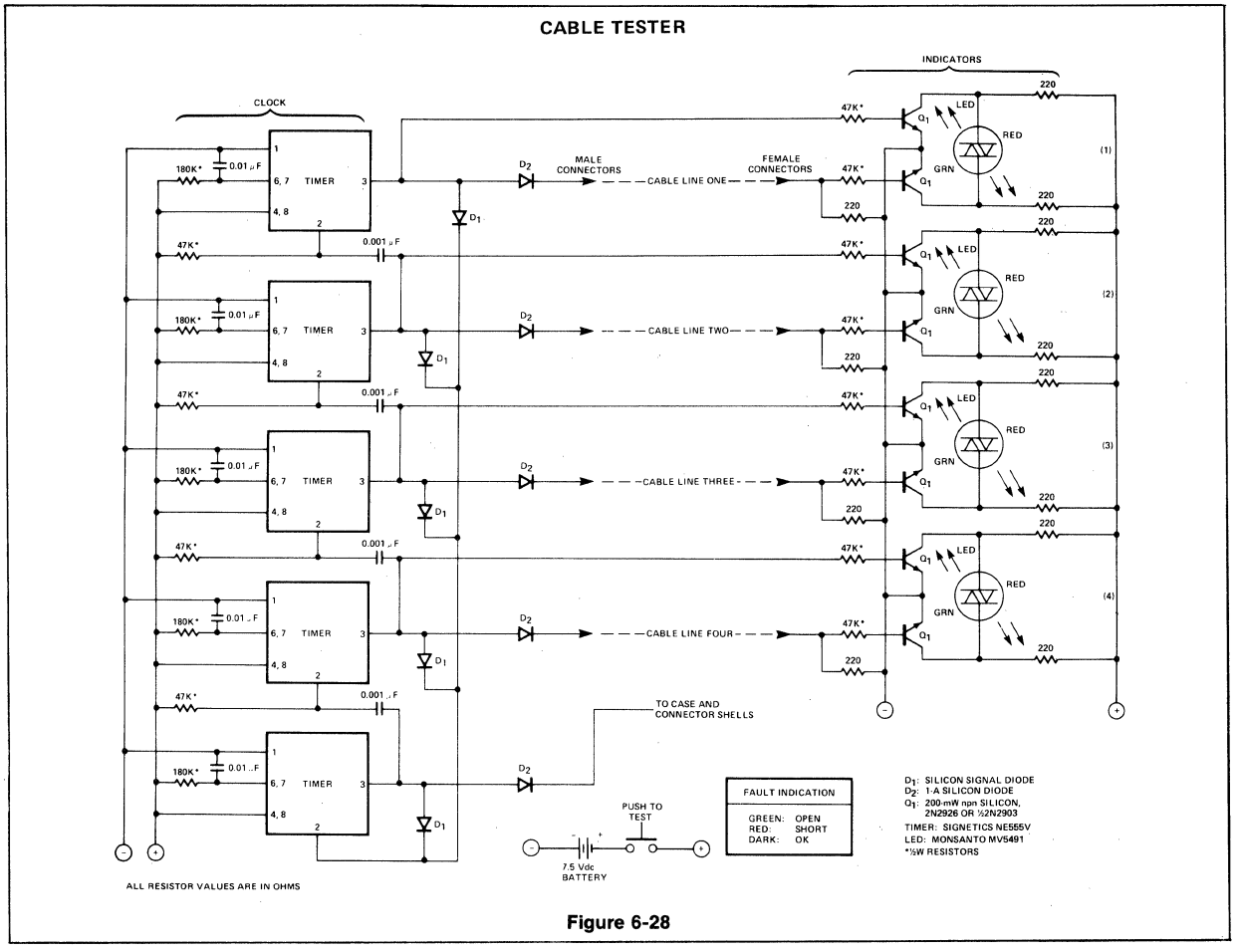
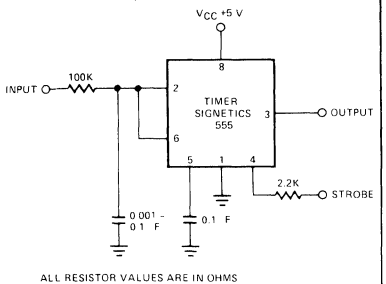


Figure 6-28

LOW COST LINE RECEIVER



ALL RESISTOR VALUES ARE IN OHMS

Figure 6-29

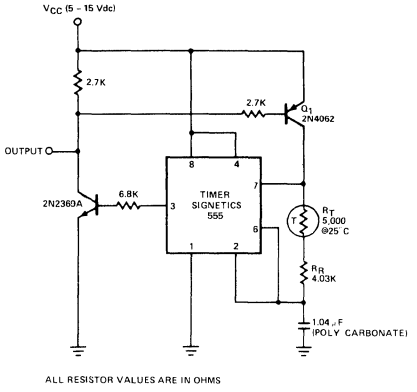
Temperature Control (11)

A couple of transistors and thermistor in the charging network of the 555-type timer enable this device to sense temperature and produce a corresponding frequency output. The circuit is accurate to within ±1 Hertz over a 78°F temperature range (Figure 6-30a & b).

Automobile Voltage Regulator (12)

Monolithic 555-type timer is the heart of this simple automobile voltage regulator. When the timer is off so that its output (pin 3) is low, the power Darlington transistor pair is off. If battery voltage becomes too low (less than 14.4 volts in this case), the timer turns on and the Darlington pair conducts (Figure 6-31).

TEMPERATURE CONTROL



ALL RESISTOR VALUES ARE IN OHMS

Figure 6-30a

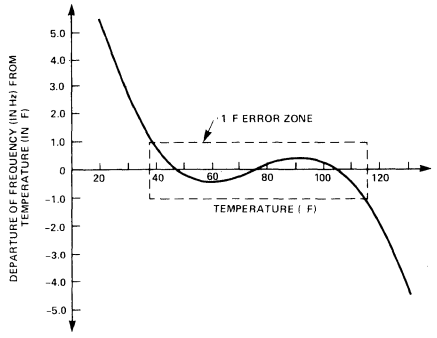
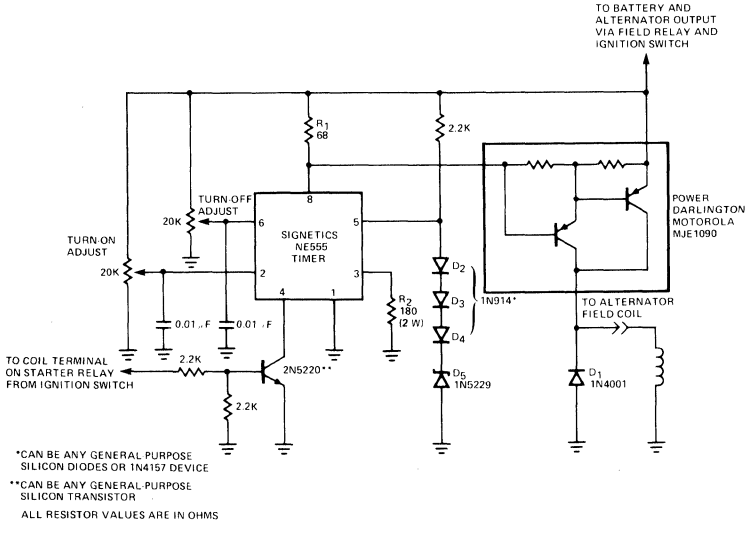


Figure 6-30b

AUTOMOBILE VOLTAGE REGULATOR



*CAN BE ANY GENERAL PURPOSE SILICON DIODES OR 1N4157 DEVICE

**CAN BE ANY GENERAL-PURPOSE SILICON TRANSISTOR

ALL RESISTOR VALUES ARE IN OHMS

Figure 6-31

Switching Regulator (13)

The basic regulator of Figure 6-32 is shown here with its associated timing and pulse generating circuitry. The block diagram illustrates how the over-all regulator works. The multivibrator determines switching frequency, and the error amplifier adjusts the pulse width of the modulator to maintain output voltage at the desired level. The output resistor divider provides the sensing voltage. (Figure 6-35)

DC-to-DC Converter (14)

DC TO DC CONVERTER

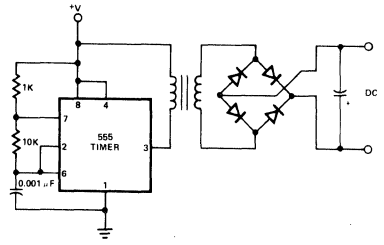


Figure 6-32

Ramp Generator (14)

RAMP GENERATOR

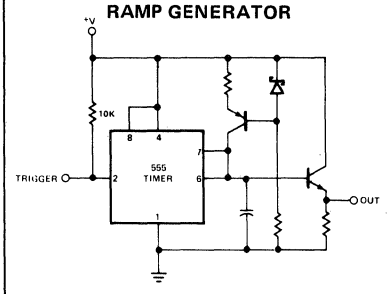


Figure 6-33

Audio Oscillator (14)

AUDIO OSCILLATOR

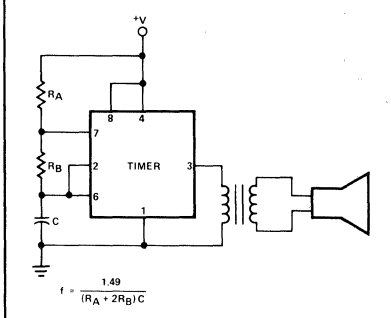


Figure 6-34

SWITCHING REGULATOR

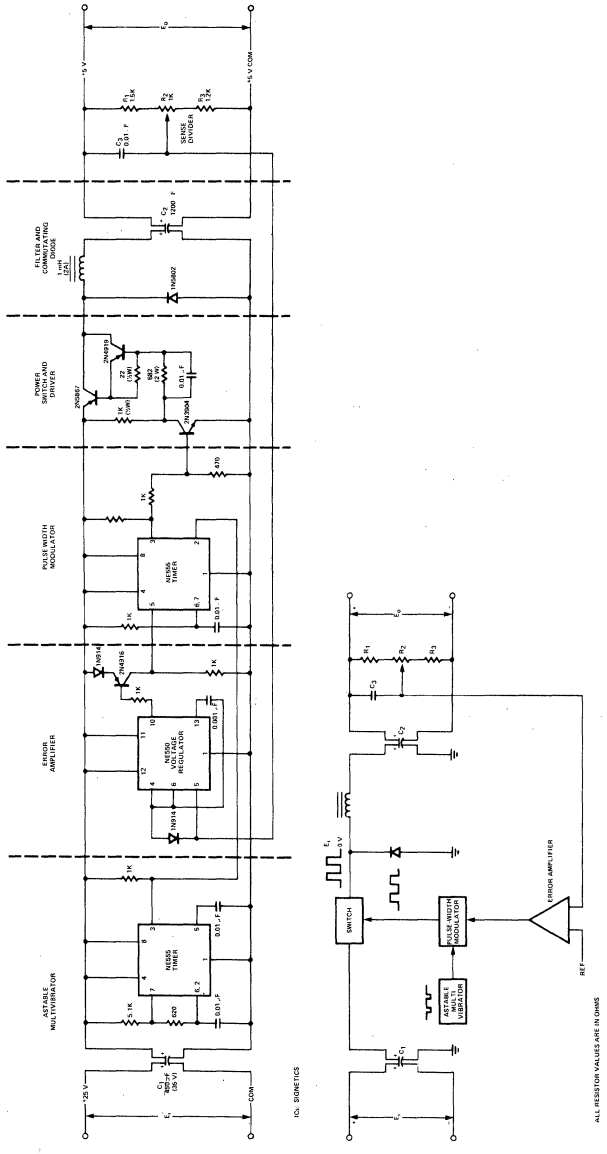


Figure 6-35

Low Power Monostable Operation

In battery operated equipment where load current is a significant factor figure 36 can deliver 555 monostable operation at low standby power. This circuit interfaces directly with CMOS 4000 series and 74L00 series. During the monostable time, the current drawn is 4.5mA for T = 1.1RC. The rest of the time the current drawn is less than 50μA. Circuit submitted by Karl Imhof, Executone Inc., Long Island City, NY.

In other low power operations of the timer where Vcc is removed until timing is needed, it is necessary to consider the output load. If the output is driving the base of a PNP transistor, for example, and its power is not removed, it will sink current into pin 3 to ground and use excessive power. Therefore, when driving these types of loads, one should recall this internal sinking path of the timer.

LOW POWER MONOSTABLE

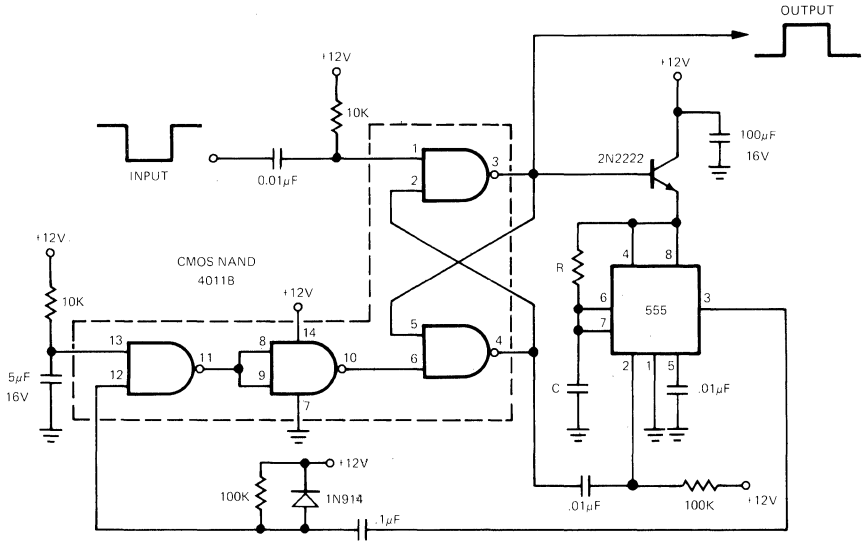


Figure 6-36

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4. **"Get Square Wave Tone Bursts With a Single Timer IC"**, Sol Black, *Electronic Design*, September 1973, pp. 148.
5. **"Toroid and Photo-SCR Prevent Ground Loops in High Isolation Biologicical Pulser"**, Joseph Sonsino, *Electronic Design*, June 21, 1973, pp. 128.
6. **"Voltage to Frequency Converter Constructed With Few Components is Accurate to 0.2%"**, Chaim Klement, *Electronic Design*, June 21, 1973, pp. 124.
7. **" Positive Voltage Changed into Negative And No Transformer is Required"**, Bert Pearl, *Electronic Design*, May 24, 1973, pp. 164.
8. **"Pair of IC Timers Sounds Auto Burglar Alarm"**, Michael Harvey, *Electronics*, June 21, 1973, pp. 131.
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10. **"IC Timer Can Function As Low Cost Line Receiver"**, John Pate, *Electronics*, June 21, 1973, pp. 132.
11. **"IC Timer Plus Thermister Can Control Temperature"**, Donald Dekold, *Electronics*, June 21, 1973, pp. 132.
12. **"IC Timer Makes Economical Automobile Voltage Regulator"**, T. J. Fusar, *Electronics*, February 21, 1974, pp. 100.
13. **"Switching Regulators, The Efficient Way to Power"**, Robert Olla, *Electronics*, August 16, 1973, pp. 94-95.
14. **"Put The IC Timer To Work in A Myriad Of Ways"**, Eugene Hnatek, *EDN*, March 5, 1973, pp. 54-58.

INTRODUCTION

The 558/559 are monolithic Quad Timers designed to be used in the timing range from a few microseconds to a few hours. Four entirely independent timing functions can be acheived, using a timing resistor and capacitor for each section. Two sections of the quad may be interconnected for astable operation. All four sections may be used together, in tandem, for sequential timing applications up to several hours. No coupling capacitors are required when connecting the output of one timer section to the input of the next.

FEATURES

- **100mA OUTPUT CURRENT PER SECTION**
- **EDGE TRIGGERED (NO COUPLING CAPACITOR)**
- **OUTPUT INDEPENDENT OF TRIGGER CONDITIONS**
- **WIDE SUPPLY VOLTAGE RANGE 4.5V TO 16V**
- **TIMER INTERVALS FROM MICROSECONDS TO HOURS**
- **TIME PERIOD EQUALS RC**

CIRCUIT OPERATIONS

In the one shot mode of operation, it is necessary to supply a minimum of two external components, the resistor and capacitor for timing. The time period is equal to the product of R and C. An output load must be present to complete the circuit due to the output structure of the 558/559.

For astable operation, it is desireable to cross couple two devices from the 558/559 Quad. The outputs are direct coupled to the opposite trigger input. The duty cycle can be set by ratio of R_1C_1 to R_2C_2 from close to zero to almost 100%. An astable circuit using one timer is shown on page 13.

OUTPUT STRUCTURE 558

The 558 structure is open collector which requires a pull-up resistor to Vcc and is capable of sinking 100mA per unit but not to exceed the power dissipation and junction temperature rating of the die and package. The output is normally low and is switched high when triggered.

OUTPUT STRUCTURE 559

The 559 output is normally low and off. It sources up to 100mA from a Darlington emitter follower when switched on. A pull down resistor to ground is required.

RESET

A reset function has been made available to reset all sections simultaneously to an output low state. During reset the trigger is disabled. After reset is finished, the trigger voltage must be taken high and then low to implement triggering.

The reset voltage must be brought below 0.8V to insure reset.

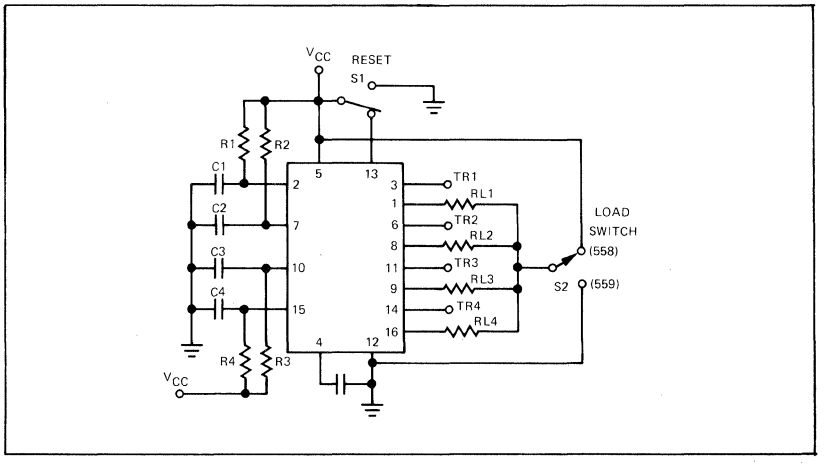
THE CONTROL VOLTAGE

The control voltage is also made available on the 558/559 timers. This allows the threshold voltage to be modulated, therefore controlling the output pulse width and duty cycle with an external control voltage. The range of this control voltage is from about 0.5V to Vcc minus 1 volt. This will give a cycle time variation of about 50:1. In a sequential timer with voltage controlled cycle time, the timing periods remain proportional over the adjustment range.

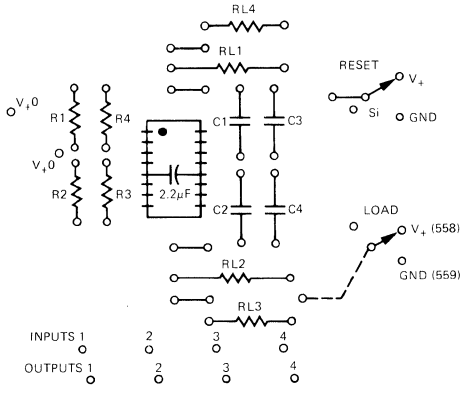
TEST BOARD FOR 558/559

The circuit layout can be used to test and characterize the 558 or 559 timer. S_2 is used to connect the loads to either Vcc or ground. The main precaution, in layout of the 558 and 559 circuits, is the path of the discharge current from the timing capacitor to ground (pin 12). The path must be direct to pin 12 and not on the ground buss. This is to prevent voltage spikes on the ground buss return due to current switching transient. It is also wise to use good power supply bypassing when large currents are being switched.

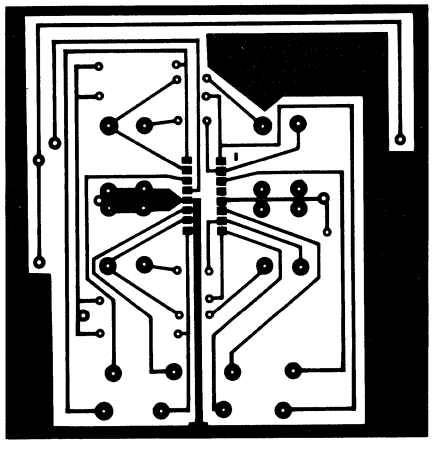
558/559 TEST CIRCUIT



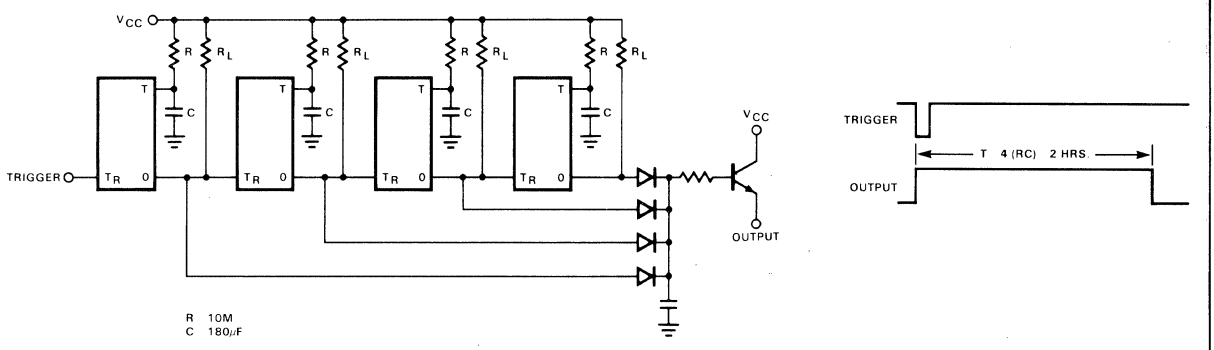
558/559 TEST BOARD LAYOUT



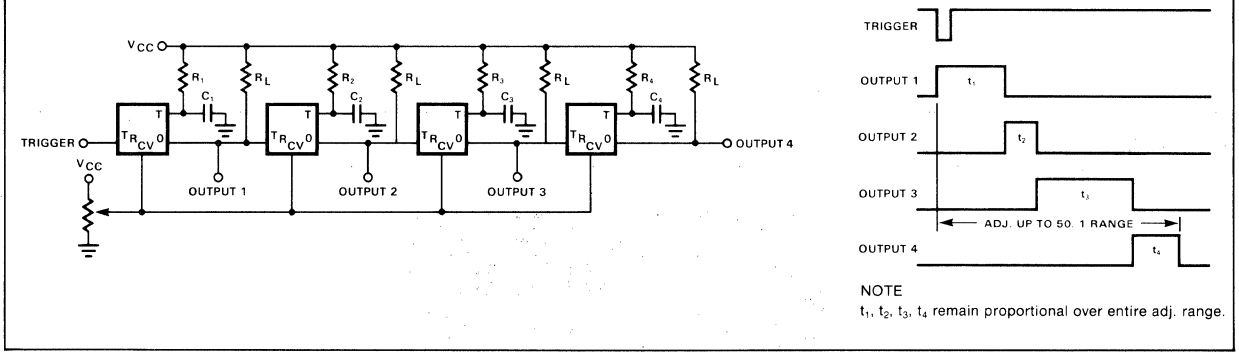
FOIL SIDE



558 TWO HOUR TIMER

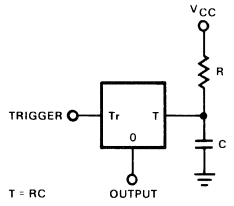


558 SEQUENTIAL TIMER WITH VOLTAGE CONTROLLED CYCLE TIME (50:1 RANGE)

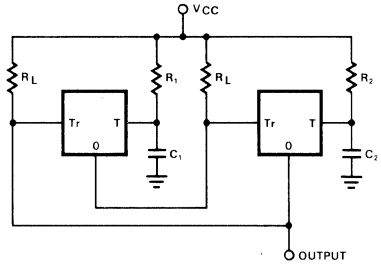


NOTE
t_1, t_2, t_3, t_4 remain proportional over entire adj. range.

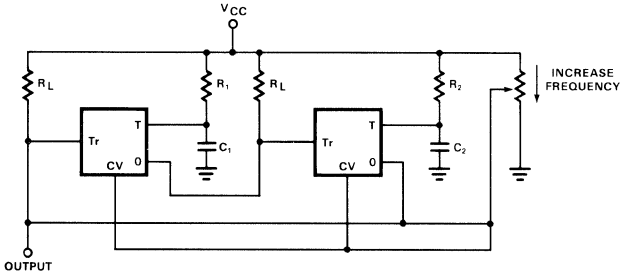
MONOSTABLE OPERATION (ONE SHOT)



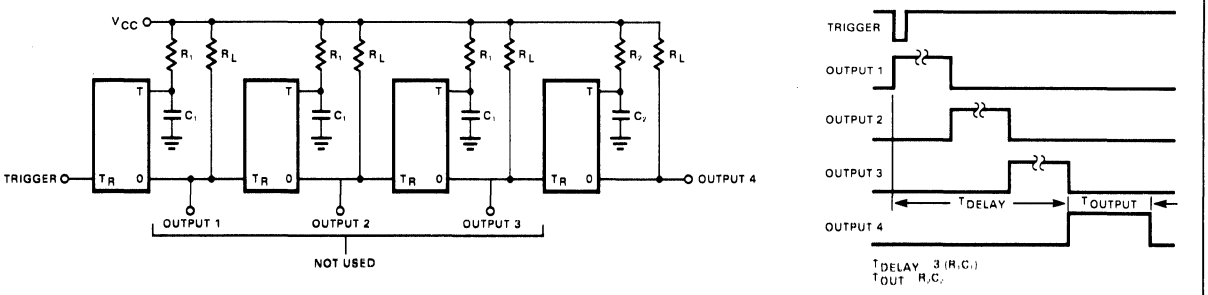
558 ASTABLE OPERATION (OSCILLATOR)



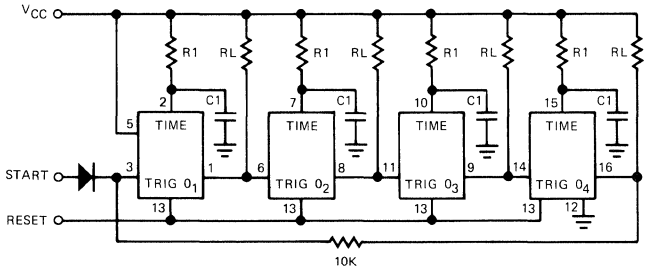
558 VARIABLE FREQUENCY OSCILLATOR WITH FIXED DUTY CYCLE



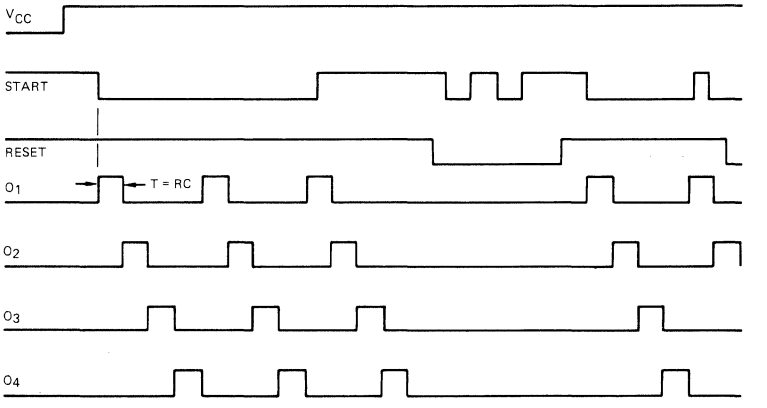
558 LONG-TIME DELAY



558 RING COUNTER

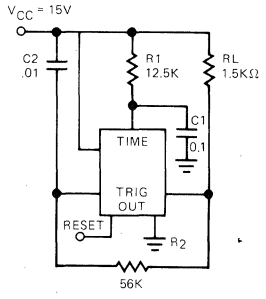


EXPECTED WAVEFORMS



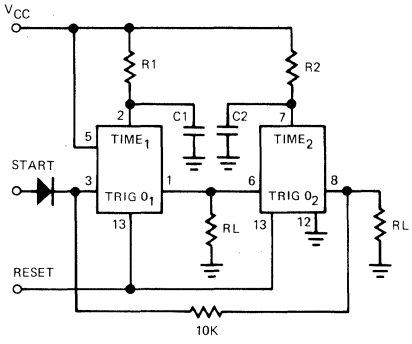
APPLICATIONS

NE558 400 Hz SQUARE WAVE OSCILLATOR

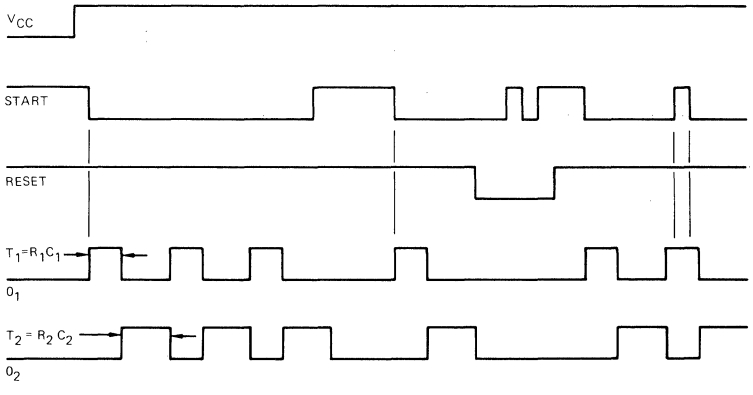


A single section of the Quad time may be used as a non precision oscillator. The values given are for oscillation at about 400Hz. $T_1 \approx R_1 C_1$ and $T_2 \approx 2.25\ R_2\ C_2$ for Vcc of 15 volts. The frequency of oscillation is subject to the changes in Vcc.

559 ASTABLE OPERATION



EXPECTED WAVEFORMS



SECTION 24
COMMUNICATIONS CIRCUITS

INTRODUCTION

The following chapter will cover those devices which can be referred to as communications circuits. Such devices as balanced modulators, RF/IF amplifiers, and video amplifiers are included. Many other devices such as the ULN2111 partially fit the communication heading but also fit the consumer category since they are intended primarily for the home entertainment market. These devices will be covered in detail in the consumer section.

RF/IF AMPLIFIERS

Ideally, semiconductor devices for use in the RF amplifiers should have a high forward transconductance and a low reverse transadmittance, that is, low feedback capacitance. A single transistor may have a high transconductance, but it will also have high reverse transadmittance, making it difficult to fully utilize its high tranconductance in a tuned amplifier.

DIFFERENTIAL AMPLIFIER

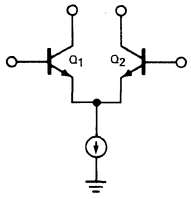


Figure 7-1

There are two multiple transistor circuit configurations available that allow the reduction of the reverse transadmittance. The first circuit, Figure 7-1, is basically a differential amplifier with a high impedance emitter coupling circuit (a current generator). Rearranging the circuit and adding a source, load, and ground result in the circuit of Figure 7-2. The input stage is common collector and the output stage is common base. Therefore, the currents in the collector to base capacitance of the input stage are completely isolated from the input stage. The reverse transadmittance then consists primarily of the stray capacitive reactance occurring in the package in which the device is encased. Figure 7-3 shows the circuit with suitable biasing applied.

The second circuit, Figure 7-4, is a series transistor connection. When a source and loading are incorporated, it is apparent that this is a common emitter-common base connection, commonly called a "cascode" circuit. Again, as in the circuit of Figure 7-3, the currents in the collector to base capacitance of the output stage are completely isolated from the input circuitry. The currents in the collector to base capacitance of the input stage do not flow directly to ground as in the circuit of Figure 7-3 and some feedback does occur. However, it is negligible because the collector of the first stage is heavily loaded by the emitter of the second stage. Therefore, very little feedback voltage may be developed across it. Figure 7-6 shows the circuit as it might be used. It has a gain capability greater than the circuit of Figure 7-3.

REARRANGEMENT SHOWING COMMON COLLECTOR-COMMON BASE STAGES

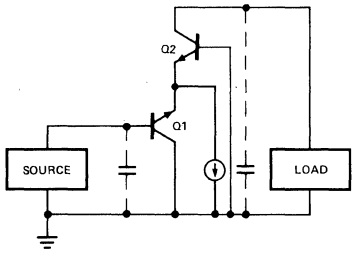


Figure 7-2

COMMON COLLECTOR-COMMON BASE STAGE WITH BIASING

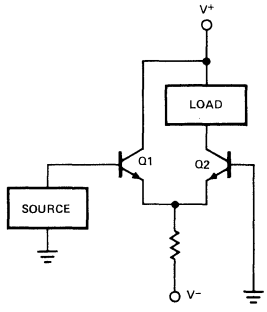


Figure 7-3

COMMON EMITTER-COMMON BASE AMPLIFIER

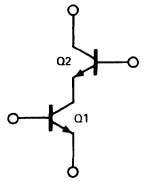


Figure 7-4

REARRANGEMENT SHOWING LOADS AND PARASITIC ELEMENTS

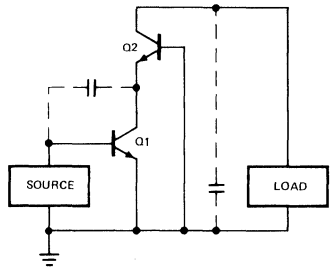


Figure 7-5

In most RF/IF amplifiers, the circuit designer wishes to operate from a single power supply. To permit this method of operation, a bias must be supplied for the bases of transistors Q1 and Q2.

This bias is obtained by inserting two more diodes, CR1 and CR2, in a series with the bias current resistor R, of Figure 7-7. Two diodes are used to ensure that if either of the transistors, Q1 or Q2, should become saturated the voltage cannot fall low enough to disturb the operation of the current generator.

COMMON EMITTER-COMMON BASE AMPLIFIER WITH BIASING

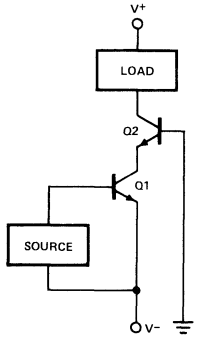


Figure 7-6

ADDITIONAL BIASING TECHNIQUE

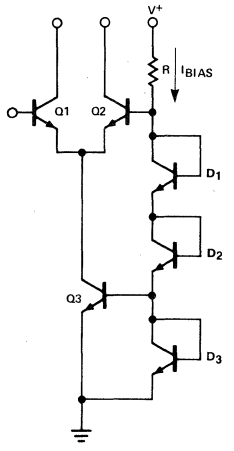


Figure 7-7

DC AND LOW FREQUENCY PARAMETERS

PARAMETER	CC-CB		CE-CB		Unit
	V^+ = 6 V	V^+ = 12 V	V^+ = 6 V	V^+ = 12 V	
Bias Network Current	1.5	3.2	1.5	3.2	mA
Quiescent Input Current	25	50	50	100	μA
Quiescent Output Current	0.6	1.4	1.2	2.8	mA
Input Conductance (Y_{11})	0.25	0.4	1.0	2.0	mmho
Output Conductance (Y_{22})	0.01	0.01	0.01	0.01	mmho
Input Capacitance	4.0	4.5	8	10	pF
Output Capacitance	3.0	2.5	3.0	2.5	pF
Feedback Capacitance	0.1	0.1	0.1	0.1	pF
Forward Transconductance (Y_{21})	11	21	45	75	mmho

Table 7-1

The final circuit design is shown in Figure 7-8. The transistors used are of small geometry and have an F_T of about 700MHz.

As shown the 510 and 511 configurations are quite similar. The emitters of the current sources are brought out for the 511 so that degeneration may be introduced for better signal handling capability and linearity.

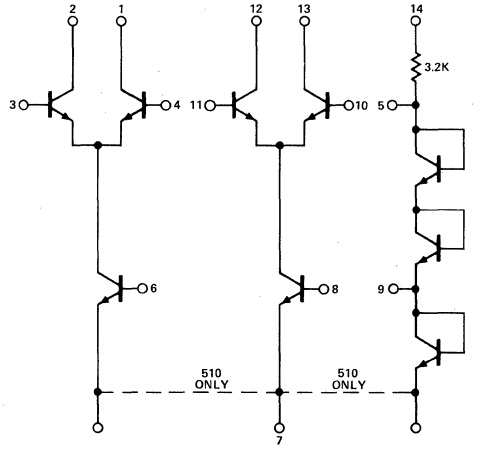
CIRCUIT CHARACTERIZATION

The circuit is characterized with "Y" parameters as is common with RF amplifiers used in the frequency range for which this device was designed. Table 7-1 is a summary of the low frequency "Y" parameters of the circuit. The real part of all the parameters remains nearly constant until the operating frequency exceeds 10MHz, at which time input and output conductances start to rise and the forward transconductance starts to fall.

The reverse transconductance of both the common emitter/common base and common base/common collector configurations is extremely small, the real part being negligible while the imaginary part corresponds to a capacitance of less than 0.1 pico Farad.

Table 7-1 shows that the forward transconductance, Y21, of both configurations is a function of power supply voltage. A plot of Y21 versus bias network current for the common collector—common base configuration, Figure 7-9, shows that the Y21 is directly proportional to the bias current. A plot of Y21 versus differential input voltage of the common emitter—common collector configuration, Figure 7-10, shows that Y21 may be controlled by changing differential input voltage. These circuit characteristics allow the application of automatic gain control to RF amplifiers made from either circuit configuration.

FINAL CIRCUIT CONFIGURATION OF 510/511



All resistor values are in ohms

Figure 7-8

CIRCUIT BIASING

Since this circuit is completely devoid of resistors and bias networks, their selection

TRANSCONDUCTANCE vs BIAS CURRENT

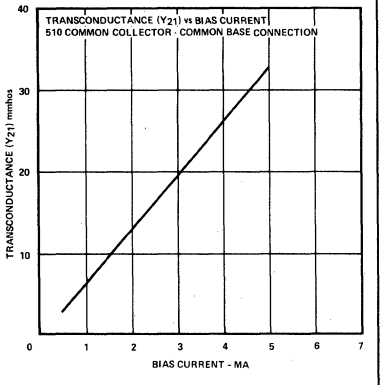


Figure 7-9

TRANSCONDUCTANCE vs CONTROL VOLTAGE

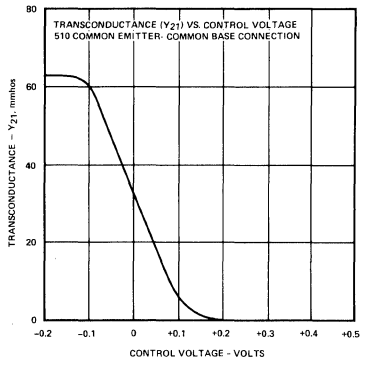


Figure 7-10

is at the discretion of the user. This allows the circuit designer complete freedom of choice in operating parameters and transistor interconnections. His only constraints are the absolute maximum ratings of the device; for example, applied voltage, current, junction temperature, etc.

A typical bias connection, option No. 1, is given in Figure 7-11. Operating currents are determined by the voltage between the base of the transistors Q1 and Q2 and V-, and resistors R1 and R2. The voltage for the bases of Q1 and Q2 is obtained from the temperature compensated voltage divider consisting of R3, R4, and diode CR1. Including CR1 in the bias network compensates for the temperature coefficient of the base-emitter voltage of Q1 and Q2. The current in the voltage divider should be approximately 75% of the emitter current of Q1 and Q2. Should it become necessary for the collector currents of Q1 and Q2 to be unequal but of the same order of magnitude, then it is suggested that the voltage divider current be selected as the average of the emitter currents. A design example is as follows:

1. Assume operating currents of 2mA for I_{C1} and I_{C2}.
2. Assume V- is at ground and V+ at +12 volts.
3. Assume that the design requires that resistors R1 and R2 be 1000ohms.
4. Calculate the voltage at the emitters and the bases of Q1 and Q2.

$V_{E1} = V_{E2} = I_{C1} \times R_I = 1000\Omega \times 2mA = +2V$

$V_{B1} = V_{B2} = V_{E1} + V_{BE} = +2V + 0.7V$

$= +2.7V\ (T_a = 25°\ C)$

BIAS CIRCUIT-OPTION 1

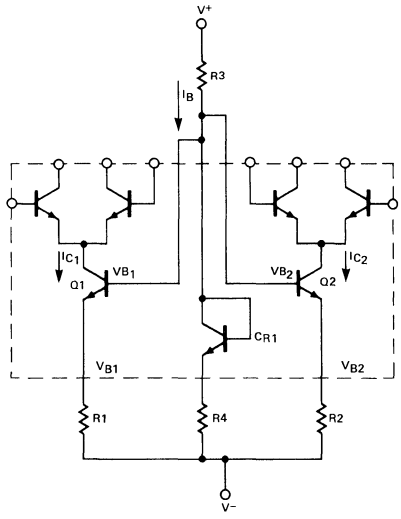


Figure 7-11

5. Calculate bias network current.

$I_B = 0.75I_{C1}$, $I_{C2} = 0.75 \times 2mA = 1.5mA$

6. Calculate bias resistors.

$$R1 = \frac{V_{E1}}{I_B} = \frac{2V}{1.5mA} = 1.33k;$$

$$R3 = \frac{V^+ - V_{B1}}{I_B} = \frac{12 - 2.7}{1.5} = 6.2k$$

The bias diode is formed from a planar type transistor which has had its collector and base connected together. It may be operated in either the forward mode or in the reverse breakdown region as a 6.8V Zener diode. When used as a Zener diode, the operating current should be kept less than 10mA.

Figure 7-12, option No. 2, shows utilization of the diode in this mode to develop a third

BIAS CIRCUIT-OPTION 2

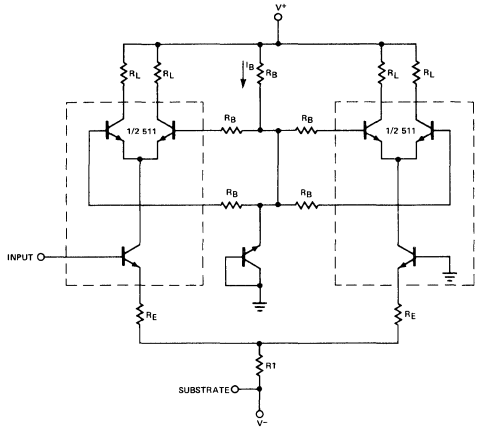


Figure 7-12

power supply required to bias the bases of the emitter-coupled transistors.

The selection of the load for these circuits is entirely application oriented. If it is to be resistive, its magnitude will be a function of the following amplifier requirements:

1. Output Voltage Swing
2. Voltage Gain
3. Bandwidth

In most applications, the load should be selected to ensure that the transistors do not saturate for the largest positive common mode input voltage.

DIFFERENTIAL AMPLIFIERS

Differential amplifiers are the easiest circuits to design. The following parameters must be considered in their design:

1. Voltage Gain
2. Output Swing
3. Input Resistance
4. Bandwidth

It may be possible to design a one-stage amplifier with all of these parameters optimized but it is highly unlikely. Usually the designs are a compromise of these parameters. For example, several cascaded stages may be required to obtain the desired gain. The gain and the output swing may have to be compromised so the required input resistance and bandwidth may be obtained.

Until bandwidths of greater than 10MHz are required, the bandwidth of the amplifier is determined solely by the RC time constant consisting of the load resistance and load capacitance, be it a discrete capacitor, stray capacitance to ground, or collector to base capacitance (Figure 7-2, 7-5). The 3dB bandwidth is determined from the following equation:

$$F_{3dB} = \frac{1}{6.28\ R_L C_L}$$

When R_L = total load resistance and
C_L = total load capacitance

The single-ended output voltage gain (A_V) of the circuit may be calculated from the product of the transconductance (g_m) and load resistance (R_L).

$$A_V = g_m R_L$$

The transconductance of the 511 may be determined for any collector current from a curve on the data sheet entitled Transconductance vs. Collector Current (Emitter-Coupled).

A second method of calculating the gain of a single-ended output differential amplifier uses the relationship between the load resistance and the resistance in the emitter circuit. Figure 7-14 shows this type of amplifier. The gain is approximated by the ratio of the load resistance to the total resistance in the emitter circuit.

The resistance in the emitter circuit consists of the emitter contact and bulk resistance, R_E and the diffusion resistance, r_e. For the 510/511, R_E is approximately 3 ohms per transistor and r_e is given by the following equation:

$$r_e = \frac{kT}{qI_e}$$

which reduces to:

$$r_e = \frac{26mV}{I_e}$$

at 25° C and for emitter currents in milliamperes.

The circuit gain measured from the differential input to one output becomes:

$$A_V = \frac{R_L}{2R_E + 2r_e} = \frac{R_L}{2\left(3 + \frac{26 \times 10^{-3}}{I_E}\right)}$$

For differential output, the differential gain is twice the single-ended output gain. The input resistance of the differential amplifier in Figure 7-14 may be approximated by the following equation:

$$R_{in} = h_{FE}(2R_E + 2r_e)$$

In utilizing this equation, the designer should be cognizant of the fact that the h_{FE} and r_e will change as a function of temperature and emitter current. The h_{FE} is typically 125 for collector currents of 1mA (at 25° C). The output swing capability is determined by the power supply voltage available. The maximum power supply voltage is determined by the absolute maximum ratings of the collector to base voltage of the differential transistors. It is this voltage which sets the maximum peak-to-peak swing for non-inductive loads. To maximize the output swing, the collector current is set so that the quiescent output voltage is one-half of the positive supply voltage. A circuit example is Figure 7-15. If, however, the input signal is differential in nature with a common mode

BASIC DIFFERENTIAL AMPLIFIER

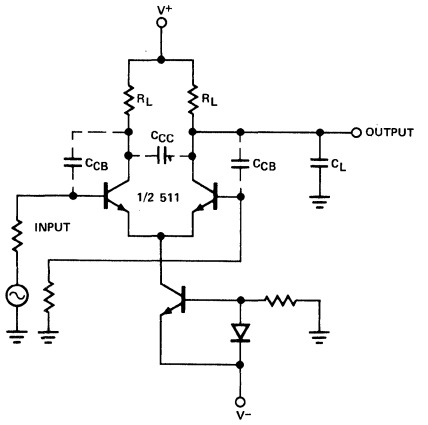


Figure 7-13

DIFFERENTIAL GAIN CALCULATIONS

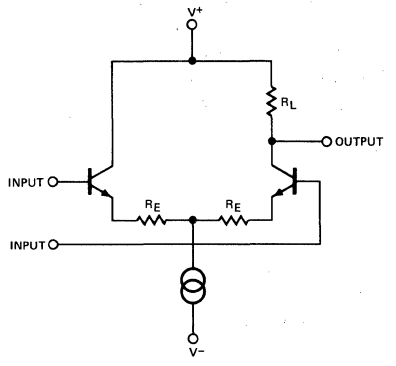


Figure 7-14

DIFFERENTIAL AMPLIFIER COLLECTOR OPERATING POINT

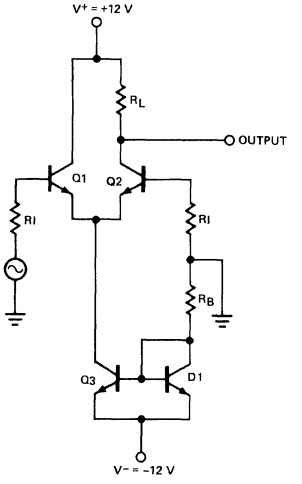


Figure 7-15

DIFFERENTIAL AMPLIFIER WITH COMMON MODE INPUT SIGNAL

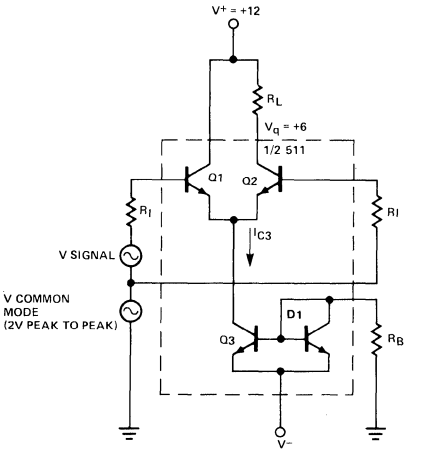


Figure 7-16

signal relative to ground, the collector operating point must be made more positive to allow for the common mode input signal if nonsymmetrical distortion is to be eliminated. For example, if the input signal is 10mV peak-to-peak riding a 2V common mode signal, the collector operating point must be raised according to the following equation:

$$V_O = \frac{V^+ + V_{cm}}{2}$$

When $V^+ = 12V$, $V_O = 7V$

The circuit of Figure 7-16 is a differential amplifier designed using the following design criteria.

Circuit Design Example: Differential Input, Single-Ended Output Amplifier

Goals:
1. Gain = 100
2. Output Swing = 10V peak-to-peak
3. Common Mode Range = ±1V
4. Input Resistance = 5000Ω

Assumptions:
1. $h_{FE} = 125$
2. Ambient Temperature (T_a) = 25° C

Solution:
1. The input resistance of a differential amplifier is set by the emitter currents of the transistors. Therefore, in order to obtain the required amplifier input resistance, the emitter currents must be determined first.

a. Find r_e:

$$R_{in} = h_{FE}(2R_E + 2r_e)$$

$$r_e = \frac{R_{in}}{2h_{FE}} - R_E = \frac{5000}{2 \times 125} - 3\Omega$$

$$r_e = 17\Omega$$

b. Determine required emitter current to give desired r_e:

$$I_e = \frac{26}{r_e} \text{ mA at } 25^\circ C$$

$$I_e = \frac{26}{17} = 1.53mA$$

c. Once the emitter currents have been obtained, the collector currents (I_C) are easily found:

$$I_C = I_e - I_b = I_e - \frac{I_e}{h_{FE}}$$

$$I_C = 1.53 - \frac{1.53}{125}$$

for all practical purposes

$$I_C \approx 1.5mA$$

2. At this point the emitter currents have been selected to provide the required input resistance and the collector currents have been found. It is now necessary to determine the load resistance that will provide the desired gain.

The voltage gain

$$(A_V) = \frac{R_L}{2R_E + 2r_e} \text{ or}$$

$$R_L = 2A_V(R_E + r_e)$$

$$= 2 \times 100 (3 + 17)$$

$$= 4000\Omega$$

3. Having determined the load resistance, we next determine the collector operating point, V_q.

$$v_q = V^+ - I_C R_L$$

when $V^+ = 12V$

$$v_q = 12 - 4000 \times 1.5 \times 10^{-3}$$

$$= +6V$$

4. The requirement for output swing is 10V peak-to-peak or the output collector must swing ±5V from its operating point. The collector will swing +6V ±5V or from +1V to +11V.

5. The positive common mode range (CMR) is determined by the most negative excursion of the output collector and will be +1V. The negative common mode range is a function of the negative power supply and is limited by the V_{be}'s of the input stage and the saturation voltage of the current source. A "rule of thumb" for determining the saturation voltage of the current source is to assume that it is equal to the V_{be} of the transistors. The negative common mode range is then:

Negative CMR = $V^- + 2V_{be}$

The V_{be}'s of the 511 are 0.8V or less, therefore:

Negative CMR = $V^- + 1.6V$.

For the design example, a negative CMR of -1V may be obtained with a negative power supply of -2.6V.

V^- = Negative CMR -1.6V

= -1V -1.6V

= -2.6V

Increasing the negative supply voltage, while staying within the ratings will allow a greater negative CMR to be achieved.

6. The current in the current source transistor, Q3, is set by the resistance of R_B and the magnitude of the negative power supply. For the 511, the best current stability is obtained when the bias current in the resistor R_B is 75% of the required current source current.

$$R_B = \frac{V^- - V_{be}}{0.75I_{c3}} = \frac{V^- - V_{be}}{1.5I_e}$$

For the design example where $V^+ = 12V$.

$$R_B = \frac{12 - 0.8}{1.5 \times 1.5 \times 10^{-3}}$$

$R_B \cong 5000\Omega$

CASCODE RF/IF AMPLIFIER (CE-CB)

The cascode configuration will be used where the maximum gain is required and where there is no requirement for symmetrical limiting. The circuit of Figure 7-17 is typical. For frequencies below 10Mhz, no particular precautions need to be taken to design a stable amplifier, other than the usual efforts to isolate the output from the input. Because of the excellent input to output isolation and because the gain control voltage has little effect on the input or output parameters, it is not necessary to mismatch the interstage transformers to ensure a stable amplifier that shows no appreciable change in the bandwidth characteristics as the gain is adjusted by the automatic gain control voltage.

Circuit Design Example: Cascode Amplifier (Figure 7-18)

Goals:

1. Output Voltage Swing (V_o) = 12V peak-to-peak
2. Voltage Gain ≥ 10.
3. Bandwidth ≥ 2MHz (with 20pF capacitive load).

Assumptions:

1. Assume high h_{FE}'s (typically 125)
2. $T_a = 25°$ C

Solution:

1. Determine the maximum load resistance. It is a function of required bandwidth.

$$R_L = \frac{1}{2\pi fC} = \frac{1}{2\pi \times 2 \times 10^6 \times 20 \times 10^{-12}}$$

$R_L = 4.03k$

If 5% resistors are used, a 3.6kΩ is the largest standard value which will ensure that the required minimum bandwidth will be obtained.

2. Determine the required Power Supply Voltage (V^+):

$V^+ \geq$ Sum of the voltage at the base of the common base transistor (Q2) and the output swing, V_o. The bias voltage at the base of Q2 is set by the reverse breakdown voltage of the 511 bias diode which is used as a Zener diode in this example.

$V^+ \geq 6.8V + 12V = 18.8V$

To allow for power supply fluctuations and measurement tolerances, use $V^+ = 20V$.

3. Determine the output collector current:

$$I_C = \frac{V^+ - V_q}{R_L}$$

where: V_q is the quiescent dc output level.

CE-CB CASCODE AMPLIFIER

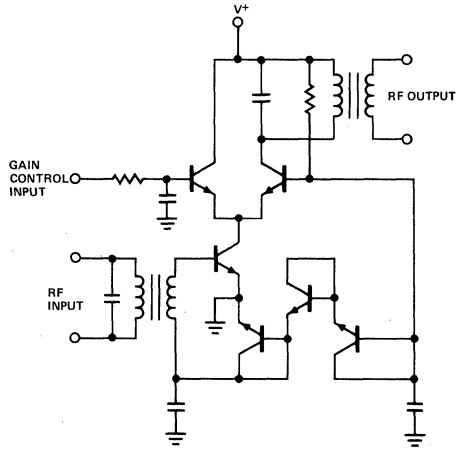
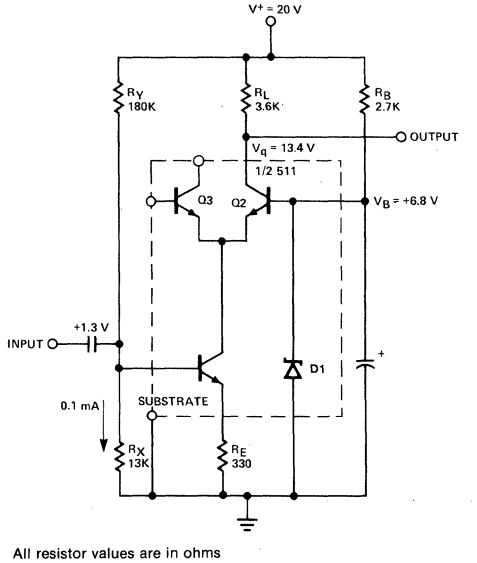


Figure 7-17

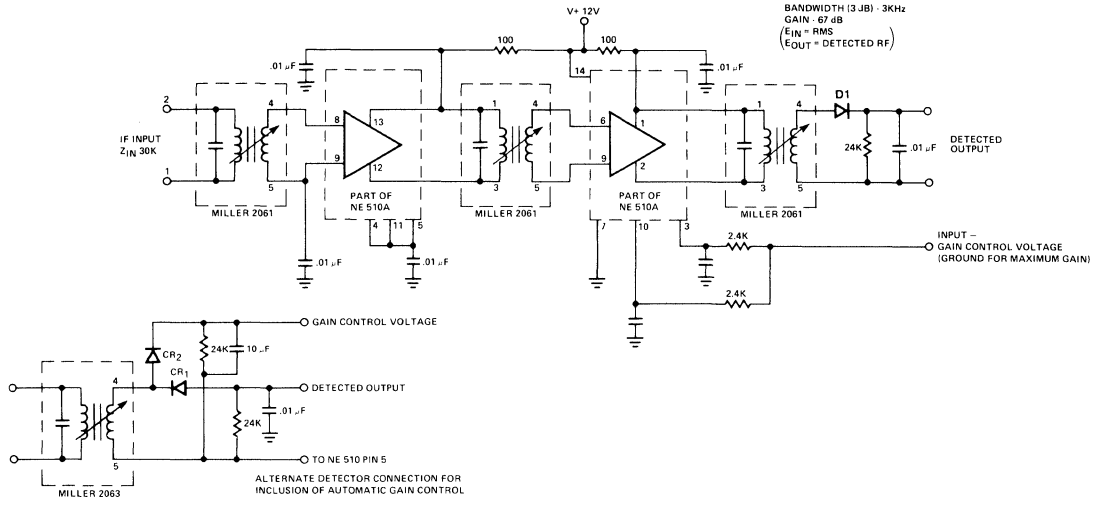
CASCODE AMPLIFIER



All resistor values are in ohms

Figure 7-18

455KHz IF AMPLIFIER
(CASCODE CONNECTION)



All resistor values are in ohms

Figure 7-19

V_q = Power supply voltage minus one-half the possible output swing

$$V_q = V^+ - \left[\frac{V^+ - V_b}{2}\right] = 13.4V$$

therefore:

$$I_C = \frac{20V - 13.4V}{3600\Omega} = 1.83A$$

4. Determine the resistance of R_E:

   The voltage gain of the circuit is a function of the ratio of the load resistance to the resistance in the emitter circuit.

$$\text{Circuit Gain} = \frac{R_L}{R_E + r_e + r_c}$$

where: r_e is the diffusion resistance and is

$$\frac{26mV}{1.83mA}$$

$r_e = 14.2\Omega$, $T_a = 25°C$

r_c is the emitter contact resistance and is 3Ω.

Substituting in the circuit gain equation from above:

$$10 = \frac{3600}{R_E + 14.2 + 3}$$

$R_E = 360 - 17.2 = 343\Omega$.

5. Select the bias network resistors:
   a. The 511 data sheet shows that the bias diode, when operated in the reverse breakdown region, has a low dynamic resistance for currents up to 10mA. The bias current was arbitrarily set at 5mA, this being a point halfway between the knee of the curve and the 10mA limit.
   b. R_X and R_Y are selected to apply the appropriate bias at the base of Q1. This voltage is determined by the level which must appear across R_E to obtain the desired operating current and the base emitter voltage of Q1. In the example, the base voltage of Q1 is +1.3V. The voltage divider resistor is selected to provide this voltage when the input bias current is 10μA.

In the design, a number of approximations were made. In all but the most critical applications, this design technique will prove quite adequate.

An expansion of the cascode amplifier is the 455KHz IF strip shown in Figure 7-19.

This amplifier has been designed using "off the shelf" IF transformers. The circuit was built using the NE510 in a 14 dual in-line plastic package. The resulting amplifier has a voltage gain of 66dB when the gain control input is grounded. Gain, in this instance, is defined as a ratio of dc output voltage at the detector to RMS input voltage. Figure 7-20 is a curve of the gain versus gain control voltage. At the maximum gain setting, the input was set so that there was no output clipping and the dc output voltage was plus 2 volts.

10.7MHz LIMITING IF AMPLIFIER

An RF amplifier, using the NE510 in the common collector—common base configuration, is shown in Figure 7-21. Although the common collector/common base circuit has a lower gain than the common emitter/common collector configuration, it will prove extremely useful when a limiting amplifier is required. When it is operated in this configuration, an input level of 0.3 volts peak-to-peak will cause the maximum realizable output swing, and no further increase in the input signal level will affect the output. In addition, selecting the load impedance so that the output transistor can never saturate will ensure a limiter design having excellent characteristics with a minimum of phase distortion.

Figure 7-22 is a schematic of the IF amplifier using the circuit of Figure 7-21. The intent of the design is to demonstrate the device characteristics and the ease with which the circuit was designed and constructed. The IF frequency used in commercial FM broadcast receivers (10.7MHz) was selected for the IF frequency for this amplifier so that there would be a basis for comparison.

GAIN vs. CONTROL VOLTAGE

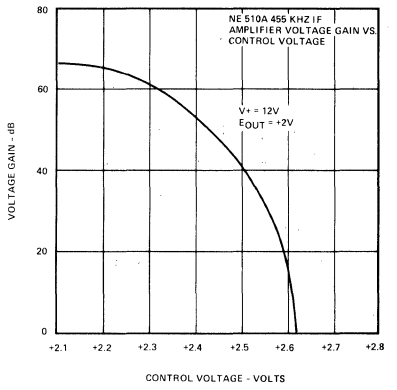


Figure 7-20

**COMMON COLLECTOR—
COMMON BASE
R.F. AMPLIFIER**

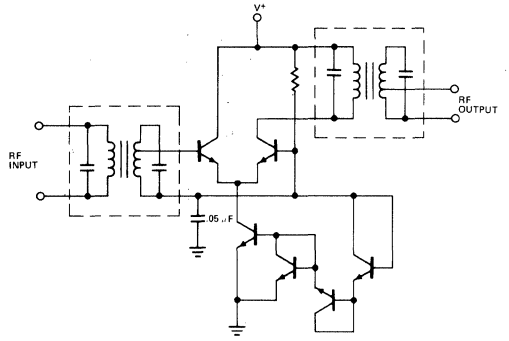


Figure 7-21

When the design was initiated, checking the Y parameters for 10.7MHz showed very little deviation from the dc and low frequency parameters. Since the feedback capacitance was very small, it was decided to use low frequency design techniques and not attempt to mismatch the coupling circuits. It was felt that if the design were made in this manner, and no instability problems occurred, the usefulness of the circuit would be proved. A typical commercial 10.7MHz IF amplifier has a 3dB bandwidth of 250 to 300KHz. It was decided to design this amplifier for 300KHz bandwidth. The bandwidths of the individual transformers in this design were selected using the equation: Amplifier Bandwidth (3dB) = Transformer Bandwidth (3dB) X $\sqrt{2^{1/n}-1}$ where "n" is the number of transformers. In our case, n = 3 and $\sqrt{2^{1/n}-1}$ = 0.5. Therefore, each transformer must have a bandwidth of 600KHz. In order to have transformers critically coupled and have a minimum saddle, the primary to secondary winding space is quite large, precluding the use of subminiature transformers for this first design. It was decided to use dual cup core transformers of the type used for many years in vacuum tube IF amplifiers. Winding data for the coils is given in Figure 7-22. The transformers used were taken from an old receiver and all the windings stripped and rewound. The transformers had a capacitance of about 12 picofarads in the base, so an additional 39 picofarads were added to the transformer externally to obtain the desired tuning capacitance.

The final amplifier designed had the desired bandwidth of 300KHz and full limiting was obtained with an input voltage at 70 microvolts RMS. No circuit prmblems appeared and tuning was not critical.

10.7MHz LIMITING IF AMPLIFIER

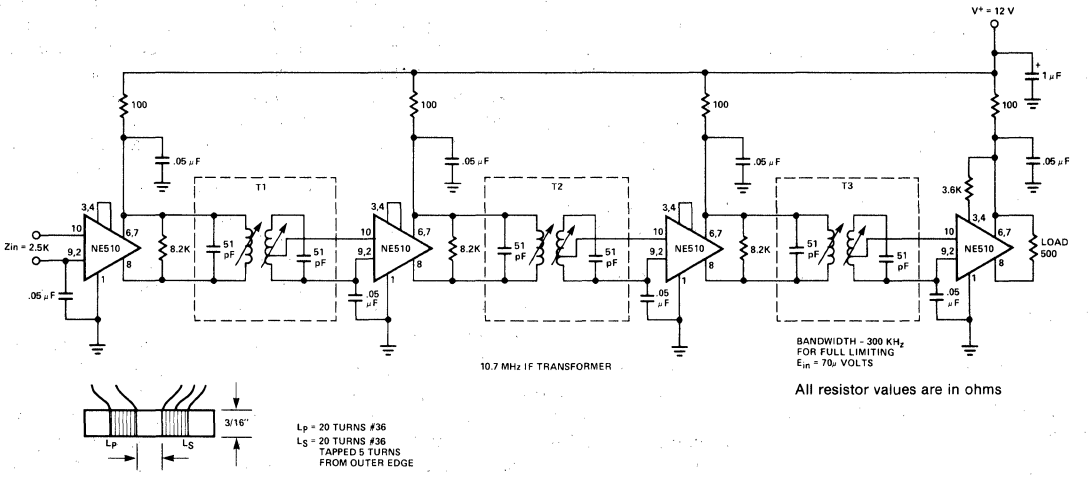


Figure 7-22

60MHz BAND PASS AMPLIFIER

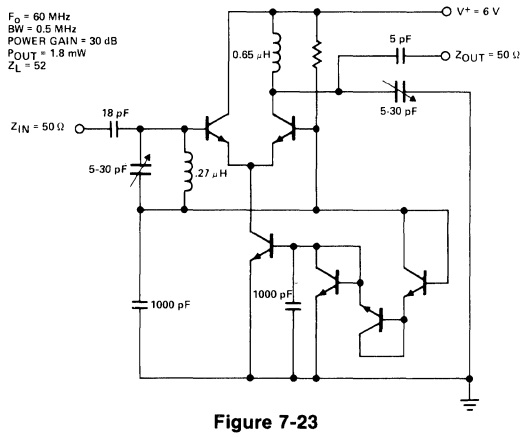
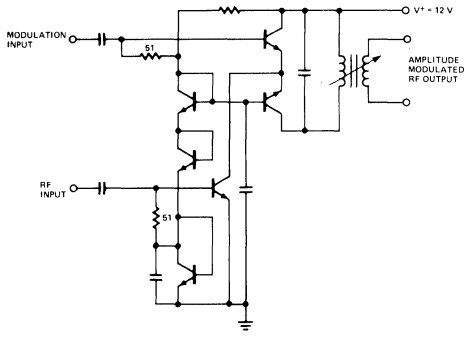


Figure 7-23

510 MODULATOR



All resistor values are in ohms

Figure 7-24

NARROW BAND 60MHz RF AMPLIFIER

The NE510/511 may be used for narrow band amplifiers with center frequencies well above 100MHz. As an example, an amplifier in the common collector—common base configuration, Figure 7-23, was designed with the following design objectives:

a. Power Gain—maximize
b. Center frequency—60MHz
c. Bandwidth (3dB)—0.5MHz
d. Power supply—+6 volts
e. Input impedance—50 ohms
f. Output impedance—50 ohms

The Y parameters for 60MHz, as read from the curves in the Appendix, are as follows:

$Y_{11} = 0.36 + j1.5 = 1.54 \angle 76.5°$
$Y_{22} = .03 + j1.1 = 1.1 \angle 88.5°$
$Y_{21} = 3.6 + j9.9 = 10.5 \angle 160°$
$Y_{12} = j0.02 = 0.02 \angle -90°$

With the help of the Linvill technique input and output networks to achieve maximum power gain were calculated. The bandwidth of the amplifier is determined by the output network, since the input network has a relatively broad bandwidth.

The following parameters were measured on a breadboard amplifier:

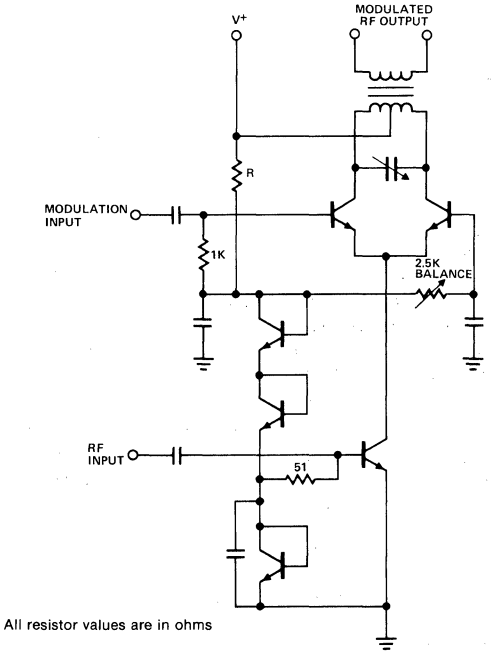
1) power gain—30dB
2) bandwidth (3dB)—0.5MHz
3) noise figure—7dB
4) maximum output swing—300 millivolts RMS across 50 ohms

Because of the very small feedback capacitance of the amplifier, tuning is easily accomplished and input adjustments have very little effect on the output impedance matching and vice versa.

MODULATORS

Returning to the curve of transadmittance of the 510 versus the differential input voltage, Figure 7-10, it may be seen that if a modulating signal instead of an AGC voltage is applied to the control input, the transconductance of the output transistor and the output current vary in a like manner. Figure 7-24 is a modulator circuit. This circuit has been operated with a carrier frequency of 50MHz and a modulating bandwidth of 4MHz. A modification of the circuit of 7-24 is the balanced modulator circuit of Figure 7-25. The constant current generator is modulated by the RF input. When the balance

BALANCED MODULATOR (SUPPRESSED CARRIER)



All resistor values are in ohms

Figure 7-25

FREQUENCY CONVERTER

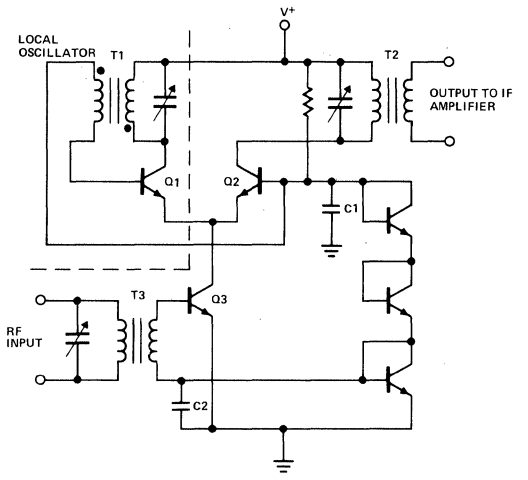
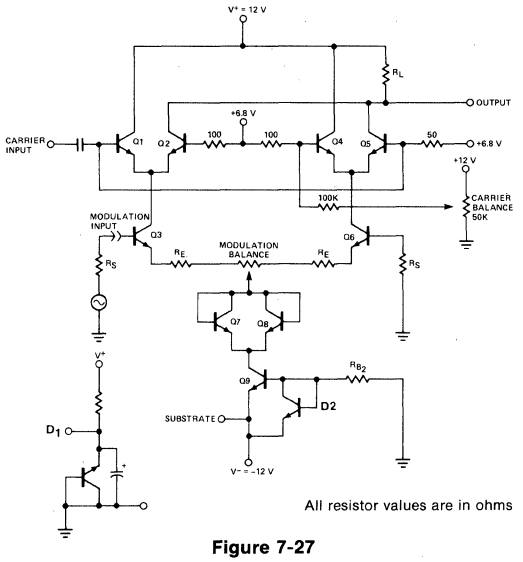


Figure 7-26

DOUBLY BALANCED MODULATOR



All resistor values are in ohms

Figure 7-27

resistor is properly adjusted and with no modulation input, no carrier will be present at the output. When a modulation signal is impressed, the collector RF currents of the differential pair of transistors will be unbalanced and a RF signal will be present at the output, the phase of which will depend upon whether the modulation input is positive or negative.

RF OSCILLATOR/CONVERTER

The 510/511 may be used as an RF oscillator/converter, Figure 7-26, to frequencies as high as 100MHz. Transistor Q1 in conjunction with a tuned transformer T1 constitutes a variable frequency oscillator of the Hartley type. The base of transistor Q1 is biased through the secondary of transformer T1. Transistor Q3 has its current modulated by the incoming signal from the transformer T3 and obtains its bias through the secondary of T3. T2 is a transformer turned to filter out all but the desired IF frequency. Transistor Q2 acts as a common base, tuned IF amplifier.

Conversion is accomplished in the nonlinear operating region of the base emitter junction of transistors Q1 and Q2. When there is no input signal to transistor Q3, only harmonics of the local oscillator fundamental frequency are generated and no signal can appear at the output because of tuned filter transformer T2. When the current in transistor Q3 is modified by the incoming signal, beat frequencies are generated between the local oscillator frequency and the incoming signal frequencies and their sum and difference frequencies appear in the currents of transistor Q2. Transformer T2 selects the desired sum or difference frequency for amplification in an IF amplifier.

DOUBLY BALANCED MODULATOR

The 511 is ideally suited for application as a doubly balanced modulator. A circuit of this type provides double sideband suppressed carrier amplitude modulation. Its output consists of the sum and difference frequencies of the two input signals and their related harmonics. For example, when the inputs are a carrier (f_c) and a modulating signal (f_m) the major output is as follows:

$$f_{out} = k(f_c - f_m) + k(f_c + f_m)$$

The output will also contain small amounts of the carrier, modulating signal and their harmonics. However, when the circuit is properly balanced, their effects are minimal.

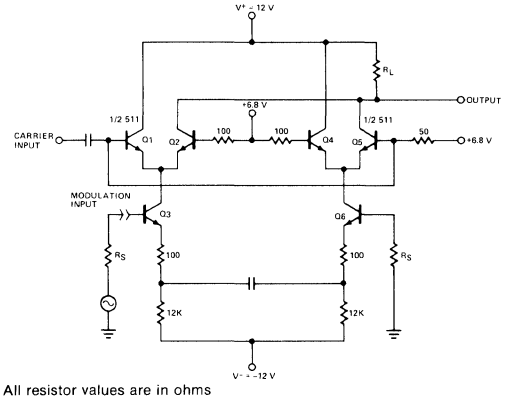
A circuit example is given in Figure 7-27. The design was done for operation with ±12V power supplies with the modulation input referenced to ground to permit direct coupling of the modulation signal for the best low frequency response. If the power supplies are not suitable for some applications, the input signal coupling techniques may be altered; capacitive coupling employed, and power supplies modified. For example, the negative supply input may be grounded, the modulation input may be capacitively coupled and biased at +4V leaving the remainder of the circuit configuration unchanged. The lower half of a 511 is merely a current source. It may be replaced with a current source constructed from a discrete transistor or if differential modulation input is available, a resistor.

R_E and the modulation balance potentiometer are selected to provide the desired dynamic range capabilities of the modulation input. The voltage developed by the emitter currents across the two R_E's and the modulation balance potentiometer should be approximately equal to the modulating signal peak-to-peak amplitude minus 100mV. Modulating signals exceeding this level will cause distortion. The modulation balance potentiometer is adjusted for minimum modulation signal in the output. In addition to this potentiometer, a carrier balance potentiometer is shown. It should be adjusted to minimize the presence of the carrier in the output. The circuit of Figure 7-28 is a variation of the circuit for Figure 7-27. It eliminates all potentiometers. Carrier and modulation feedthough will not be as small as the circuit of Figure 2-27, but will be quite useful where circuit adjustments must be kept at a minimum. The capacitor between the emitters of Q2 and Q6 should be selected to have a low reactance at the lowest modulating frequency.

DEMODULATOR

The 511 may be used in demodulator applications also. As an example, the FM stereo demodulator circuit of Figure 7-29 is pre-

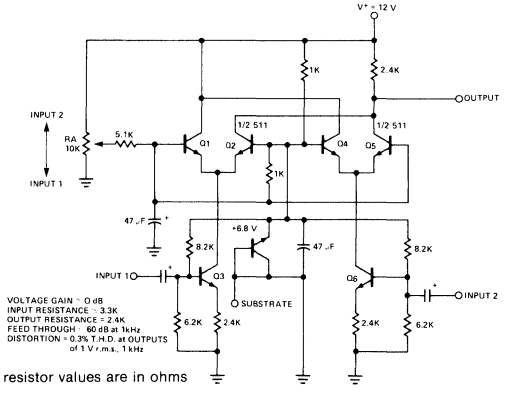
DOUBLY BALANCED MODULATOR, SELF-BALANCING



All resistor values are in ohms

Figure 7-28

ISOLATION AMPLIFIER WITH REMOTELY SELECTED INPUTS AND REMOTELY CONTROLLED GAIN



All resistor values are in ohms

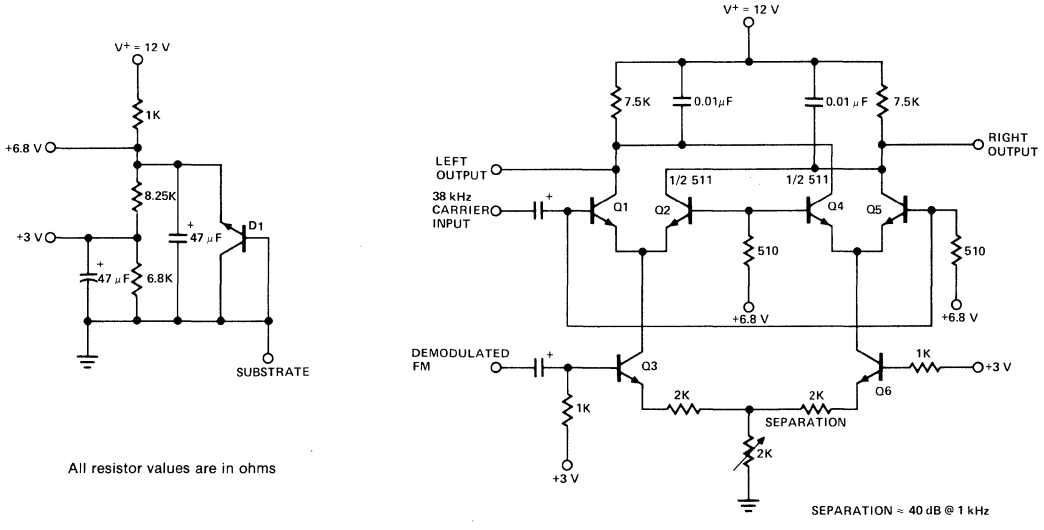
Figure 7-30

sented. The demodulator FM information is applied to the base of Q3. The collector current of Q3 is switched alternately, by the 38KHz sub-carrier local oscillator, from the left output load to the right output load. Transistors Q4 and Q5 are driven out of phase with transistors Q1 and Q2 from the 38KHz local oscillator so as to cancel the 38KHz component in the outputs. The separation is optimized by applying a small portion of the input signal to the emitter Q6 to cancel unwanted out-of-channel information. For maximum separation, the 38KHz sub-carrier local oscillator signal should have a minimum second harmonic content. Ideally its waveform should be square with a 50% duty cycle and have an amplitude of approximately 1V peak-to-peak.

Although doubly balanced modulators are not normally used for audio applications, this type of circuit with a few minor modifications may prove extremely useful. The isolation amplifier with remotely selected inputs is shown in Figure 7-30. The level adjust/mixing control (R_A) may be located in a far location and the distance is limited only by the noise (60Hz) which may be picked up. Feedthrough from the OFF channel is negligible. Bandwidth is limited only by the capacitive load on the output.

Applications occasionally arise where it is required to select, with a logic signal, one of

STEREO DEMODULATOR



All resistor values are in ohms

Figure 7-29

two inputs to an analog system; for example, sense amplifiers for magnetic tape or disc readout or other memory systems. The circuit of Figure 7-31 illustrates a 511 application which will perform this function. Differential input transistor pairs, Q1 and Q2 or Q4 and Q5 are selected by turning on current source transistor Q3 or Q6. The bias diode of the 511 is used in its reverse breakdown mode to couple the logic input signal through a standard gate to the level of the current source bases in such a manner that the level at the base of Q3 swings through the fixed voltage level present at the base of Q6 when the logic input goes from a "O" to a "1."

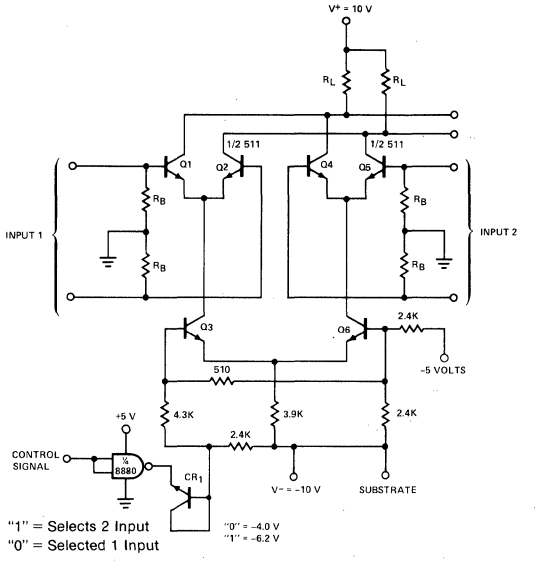
DIGITAL TO ANALOG CONVERTER

The 511, an extremely versatile device, is readily connected as a dual switched current source. When a number of 511's are connected as current sources, with each current properly scaled, a digital to analog converter may be constructed, as in Figure 7-32. The currents are scaled such that:

$$I_n = \frac{I_1}{2^{n-1}}$$

and are summed in a very low impedance provided by the virtual ground present at the inverting input of the operational amplifier.

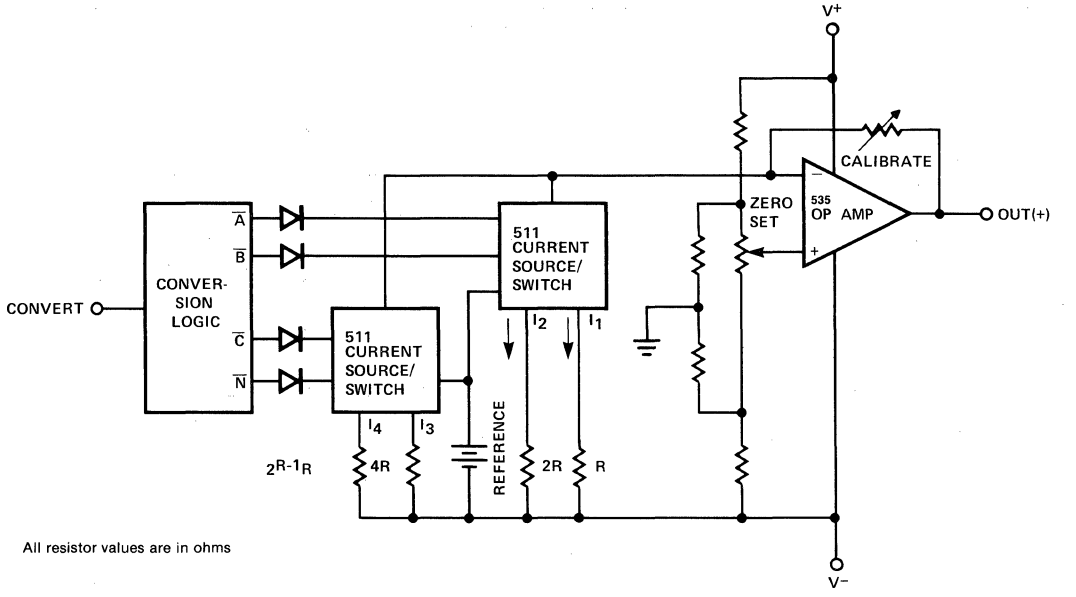
2-INPUT, DIGITALLY SELECTED DIFFERENTIAL PREAMPLIFIER



All resistor values are in ohms

Figure 7-31

BLOCK DIAGRAM—D/A CONVERTER (4-BIT—16 LEVEL)



All resistor values are in ohms

Figure 7-32

DETAIL OF CURRENT SOURCE SWITCH FOR DIGITAL TO ANALOG CONVERTER

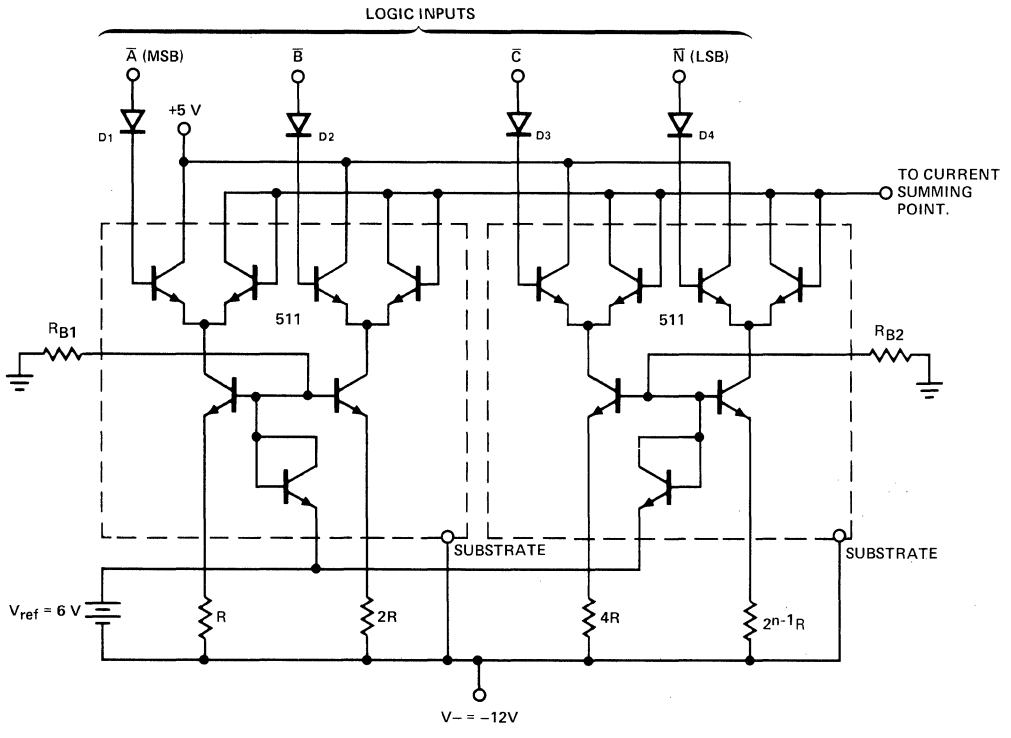


Figure 7-33

The sum of the currents at the input of the operational amplifier is presented at its output as a positive voltage proportional to the input current. The type of conversion, successive approximation or ripple counter, etc., is controlled by the conversion logic. $\bar{A}$ is the most significant bit (MSB) and $\bar{N}$ is the least significant bit (LSB). The calibrate potentiometer is adjusted for the desired maximum output when all of the current switches are ON. The zero set is adjusted for a zero output level when all of the current sources are turned off.

The detail of the current switches is shown in Figure 7-33. The diodes CR1 through CR4 are necessary to ensure that the current switches may be adequately driven by typical DTL/TTL gates. The bias resistors, R_b, are selected to provide a current in the bias compensating diodes equal to 75% of the current in the most significant of the two current sources of each 511.

ANALOG MULTIPLEXER

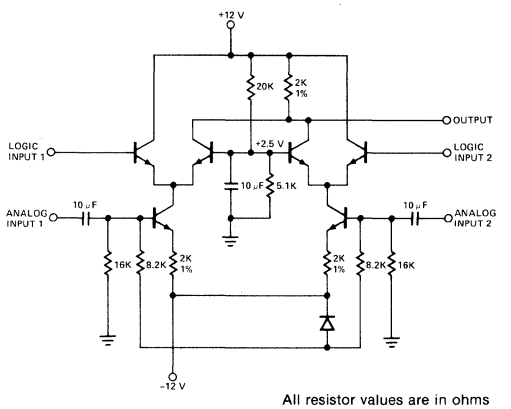
Many applications arise where digitally controlled analog switching is required. The circuit of Figure 7-34 illustrates a design using an integrated circuit which is capable of selecting one of two analog signals by digital means. The 511 is connected such that a logical "0", at the control input, permits the associated analog input signal to appear at the common collector resistor while the other analog input signal is rejected. The block diagram of Figure 7-35 shows the connection of four of the circuits of Figure 7-34 to form an eight channel analog multiplex switch. A Signetics 8250, binary to octal decoder, is used to convert a three line binary address to a one of eight signal and present a logic "0" to the appropriate 511 switch. The channel capability may be increased by the use of additional 511's and 8250's with the D (inhibit) input of the 8250's being used to control the groups of eight.

Analog signals of up to 200KHz may be switched without amplitude degradation. The bandwidth may be extended to 2MHz when the collector load resistor is replaced with the input of a common base amplifier, Figure 7-36, thereby reducing the effects of the total parasitic circuit capacitances when many collectors are connected in parallel.

For critical applications, the binary information should be applied to the 8250 inputs simultaneously. For applications where a 50 to 100 nanosecond switching transient may be tolerated in the output, the 8250 inputs may be derived from ripple through counters. In order to eliminate gain differences, from input to input, and minimize the dc shift at the output, the bias and emitter resistors should be matched at 1% or better.

The circuits presented in this memo are but a few of the many possible. The component values shown are not necessarily optimum and should be modified to fit each specific

ANALOG SWITCH



All resistor values are in ohms

Figure 7-34

application. In the application of the 511, the user is cautioned to maintain short leads and maintain input/output isolation as the circuit transistors have gains in excess of unity at frequencies as high as 500MHz. The user should also note that the isolation contact substrate *must* always be connected to the most negative point of the circuit. Further information is presented in the Appendix.

BALANCED MODULATOR

The MC1496 is a monolithic transistor array arranged as a balanced modulator-demodulator. The device takes advantage of the excellent matching qualities of monolithic devices to provide superior carrier and signal rejection. Carrier suppressions of 50dB at 10MHz are typical with no external balancing networks required.

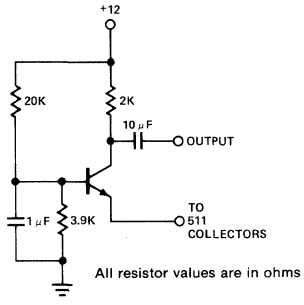
Applications include AM and suppressed carrier modulators, AM and FM demodulators, and phase detectors.

THEORY OF OPERATION

As Figure 7-37 suggests the topography includes three differential amplifiers. Internal connections are made such that the output becomes a product of the two input signals V_C and V_S.

To accomplish this the differential pairs Q1-Q2 and Q3-Q4, with their cross coupled collectors, are driven into saturation by the zero crossings of the carrier signal V_C. With

COMMON BASE AMPLIFIER



All resistor values are in ohms

Figure 7-36

ANALOG MULTIPLEXER

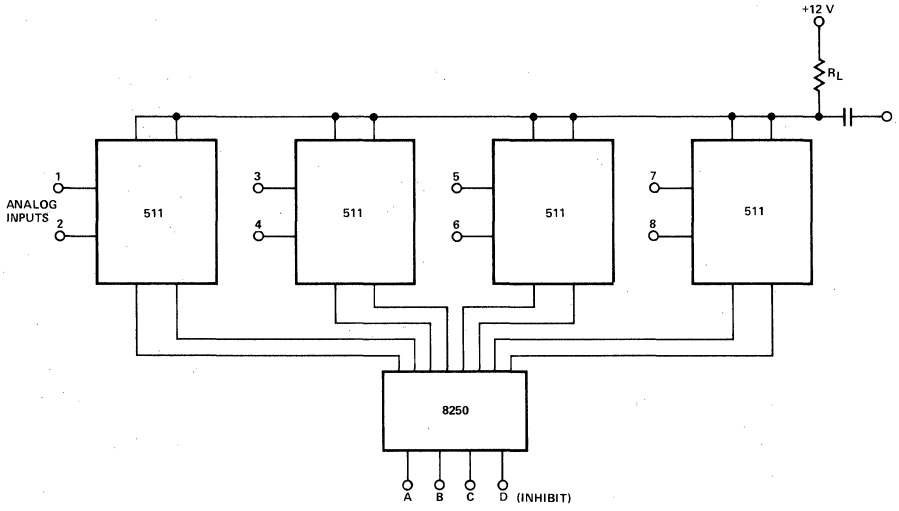
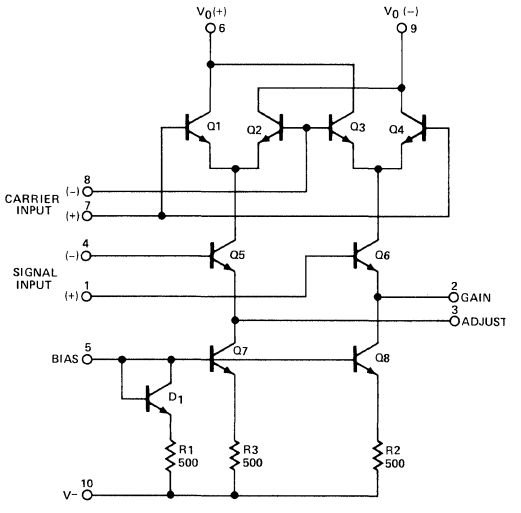


Figure 7-35

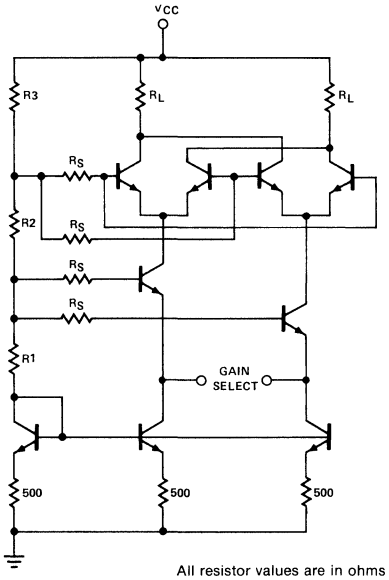
BALANCED MODULATOR SCHEMATIC



All resistor values are in ohms

Figure 7-37

SINGLE SUPPLY BIASING



All resistor values are in ohms

Figure 7-38

a low level signal, V_S, driving the third differential amplifier Q5-Q6, the output voltage will be a full wave multiplication of V_C and V_S. Thus for sine wave signals, V_{out} becomes:

$$V_{out} = E_x E_y [\cos(\omega_x + \omega_y)\, t + \cos(\omega_x - \omega_y)\, t]$$

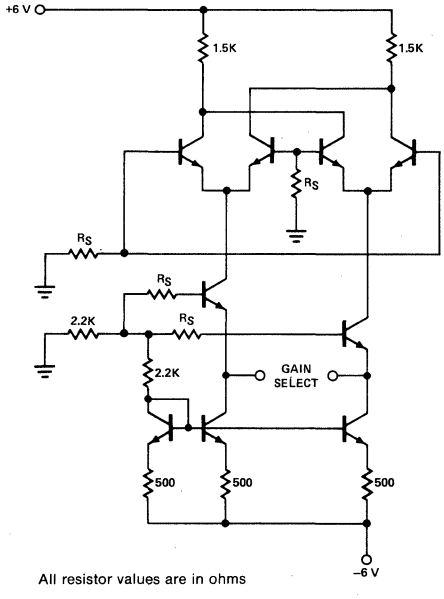
From equation 7-21 the output voltage will contain the sum and difference frequencies of the two original signals. In addition, with the carrier input ports being driven into saturation, the output will contain the odd harmonics of the carrier signals.

BIASING

Since the MC1496 was intended for a multitude of different functions as well as a myriad of supply voltages, the biasing techniques are specified by the individual application. This allows the user complete freedom to choose gain, current levels, and power supplies. The device can be operated with single ended or dual supplies.

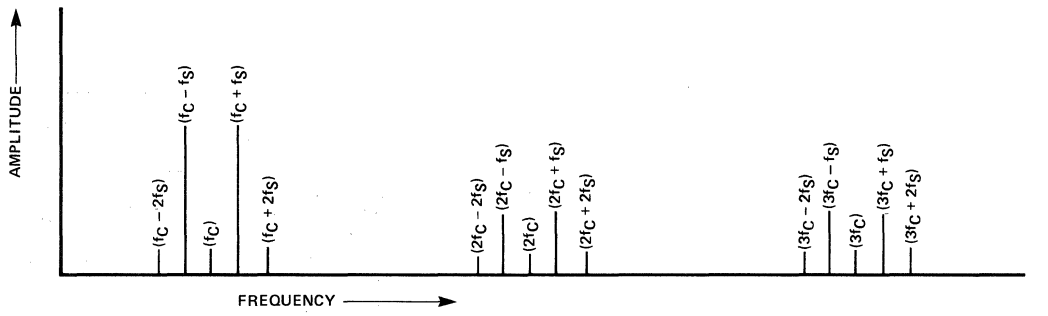
Internally provided with the device are two current sources driven by a temperature compensated bias network. Since the transistor geometries are the same and since V_{BE} matching in monolithic devices is excellent, the currents through Q7 and Q8 will be identical to the current set at pin 5. Figure 7-38 and 7-39 illustrate typical biasing arrangements from split and single ended supplies respectively.

DUAL SUPPLY BIASING



All resistor values are in ohms

Figure 7-39



f_C Carrier Fundamental
f_S Modulating Signal
$f_C \pm f_S$ Fundamental Carrier Sidebands
$f_C \pm nf_S$ Fundamental Carrier Sideband Harmonics
nf_C Carrier Harmonics
$nf_C \pm nf_S$ Carrier Harmonic Sidebands

Figure 7-40

Of primary interest in beginning the bias circuitry design is relating available power supplies and desired output voltages to device requirements with a minimum of external components.

The transistors are connected in a cascode fashion. Therefore sufficient collector voltage must be supplied to avoid saturation if linear operation is to be achieved. Voltages greater than 2 volts is sufficient in most applications.

Biasing is achieved with simple resistor divider networks as shown in Figure 7-39. This configuration assumes the presence of symmetrical supplies. Explaining the dc biasing technique is probably best accomplished by an example. Thus, the initial assumptions and criteria are set forth:

1. Output swing greater than 4 volts p-p.
2. Positive and negative supplies of 6 volts are available.
3. Collector current is 2mA. It should be noted here that the collector output current is equal to the current set in the current sources.

As a matter of convenience the carrier signal ports are referenced to ground. If desired the modulation signal ports could be ground referenced with slight changes in the bias arrangement. With the carrier inputs at dc ground, the quiescent operating point of the outputs should be at one half the total positive voltage or 3 volts for this case. Thus a collector load resistor is selected which drops 3 volts at 2mA or 1.5k ohm. A quick check at this point reveals that with these loads and current levels the peak to peak output swing will be greater than 4 volts. It remains to set the current source level and proper biasing of the signal ports.

The voltage at pin 5 is expressed by

$V_{bias} = V_{BE} = 500 \times I_S$

where I_S is the current set in the current sources.

For the example V_{BE} is 700mV at room temperature and the bias voltage at pin 5 becomes 1.7 volts. Because of the cascode configuration both the collectors of the current sources and the collectors of the signal transistors must have some voltage to operate properly. Hence the remaining voltage of the negative supply (-6v + 1.7v = -4.3v) is split between these transistors by biasing the signal transistor bases at -2.15 volts.

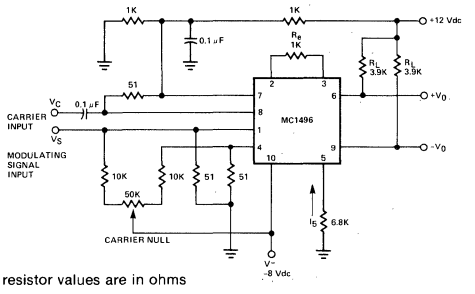
Countless other bias arrangements can be used with other power supply voltages. The important thing to remember is that sufficient dc voltage is applied to each bias point to avoid collector saturation over the expected signal wings.

BALANCED MODULATOR

In the primary application of balanced modulation, generation of double sideband suppressed carrier modulation is accomplished. Due to the balance of both modulation and carrier inputs the output, as mentioned, contains the sum and difference frequencies while attentuating the fundamentals. Upper and lower sideband signals are the strongest signals present with harmonic sidebands being of diminishing amplitudes as characterized by Figure 7-40.

Gain of the 1496 is set by including emitter degeneration resistance located as R_E in Figure 7-41. Degeneration also allows the

DOUBLE SIDEBAND SUPPRESSED CARRIER MODULATOR



All resistor values are in ohms

Figure 7-41

maximum signal level of the modulation to be increased. In general linear response defines the maximum input signal as

$V_S \leq I5 \bullet R_E$ (Peak)

and the gain is given by

$$A_{vs} = \frac{R_L}{R_E + 2r_e}$$

This approximation is good for high levels of carrier signals. Table 7-2 summarizes the gain for different carrier signals.

As seen from Table 7-2 the output spectrum suffers an amplitude increase of undesired sideband signals when either the modulation or carrier signals are high. Indeed the modulation level can be increased if R_E is increased without significant consequence. However, large carrier signals cause odd harmonic sidebands (Figure 7-40) to increase. At the same time, due to imperfections of the carrier waveforms and small imbalances of the device, the second harmonic rejection will be seriously degraded. Output filtering is often used with high carrier levels to remove all but the desired sideband. The filter removes unwanted signals while the high carrier level guards against amplitude variations and maximizes gain. Broadband modulators, without benefit of filters, are implemented using low carrier and modulation signals to maximize linearity and minimize spurious sidebands.

CARRIER INPUT SIGNAL (V_C)	APPROXIMATE VOLTAGE GAIN	OUTPUT SIGNAL FREQUENCY(S)
Low-level dc	$\frac{R_L V_C}{2(R_E + 2r_E)\left(\frac{KT}{q}\right)}$	f_M
High-level dc	$\frac{R_L}{R + 2r_e}$	f_M
Low-level ac	$\frac{R_L V_C(rms)}{2\sqrt{2}\left(\frac{KT}{q}\right)(R_E + 2r_e)}$	$f_C \pm f_M$
High-level ac	$\frac{0.637R_L}{R_E + 2r_e}$	$f_C \pm f_M$, $3f_C \pm f_M$, $5f_C \pm f_M$....

Table 7-2 VOLTAGE GAIN & OUTPUT SPECTRUM vs INPUT SIGNAL

AM MODULATOR

The basic current of Figure 7-41 allows no carrier to be present in the output. By adding offset to the carrier differential pairs, controlled amounts of carrier appear at the output whose amplitude becomes a function of the modulation signal or AM modulation. As shown the carrier null circuit is changed from Figure 7-41 to have a wider range so that wider control is achieved. All connections are shown in Figure 7-42.

AM DEMODULATION

As pointed out in equation 7-21, the output of the balanced mixer is a cosine function of the angle between signal and carrier inputs. Further, if the carrier input is driven hard enough to provide a switching action the output becomes a function of the input amplitude. Thus the output amplitude is maximum when there is 0° phase difference as shown in Figure 7-43.

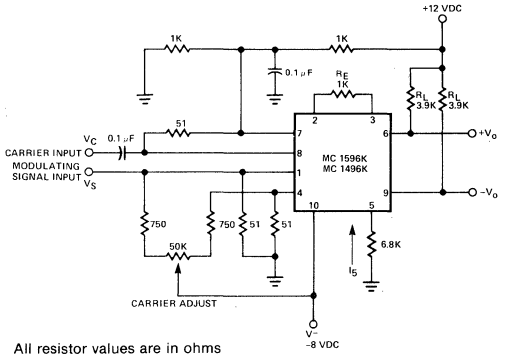
Amplifying and limiting of the AM carrier is accomplished by the ULN2209. Providing 55dB of gain, the 2209 also provides symmetrical limiting above 400μ volts. The limited carrier is then applied to the detector at the carrier ports to provide the desired switching function. The signal is then demodulated by the syncronous AM demodulator (1496) where the carrier frequency is attenuated due to the balanced nature of the device. Care must be taken not to overdrive the signal input so that distortion does not appear in the recovered audio. Maximum conversion gain is reached when the carrier signals are in phase as indicated by the phase-gain relationship drawn in Figure 7-43. Output filtering will also be necessary to remove high frequency sum components of the carrier from the audio signal.

PHASE DETECTOR

The versatility of the balanced modulator or multiplier also allows the device to be used as a phase detector. As mentioned the output of the detector contains a term related to the cosine of the phase angle. Two signals of equal frequency are applied to the inputs as per Figure 7-44. The frequencies are multiplied together producing the sum and difference frequencies. Equal frequencies cause the difference component to become dc while the undesired sum component is filtered out. The dc component is related to the phase angle by the graph of Figure 7-45. At 90 degrees the cosine becomes zero, while being at maximum positive or maximum negative at 0° and 180° respectively.

The advantage of using the balanced modulator over other types of phase comparators is the excellent linearity of conversion. This configuration also provides a conversion

AM MODULATOR



All resistor values are in ohms

Figure 7-42

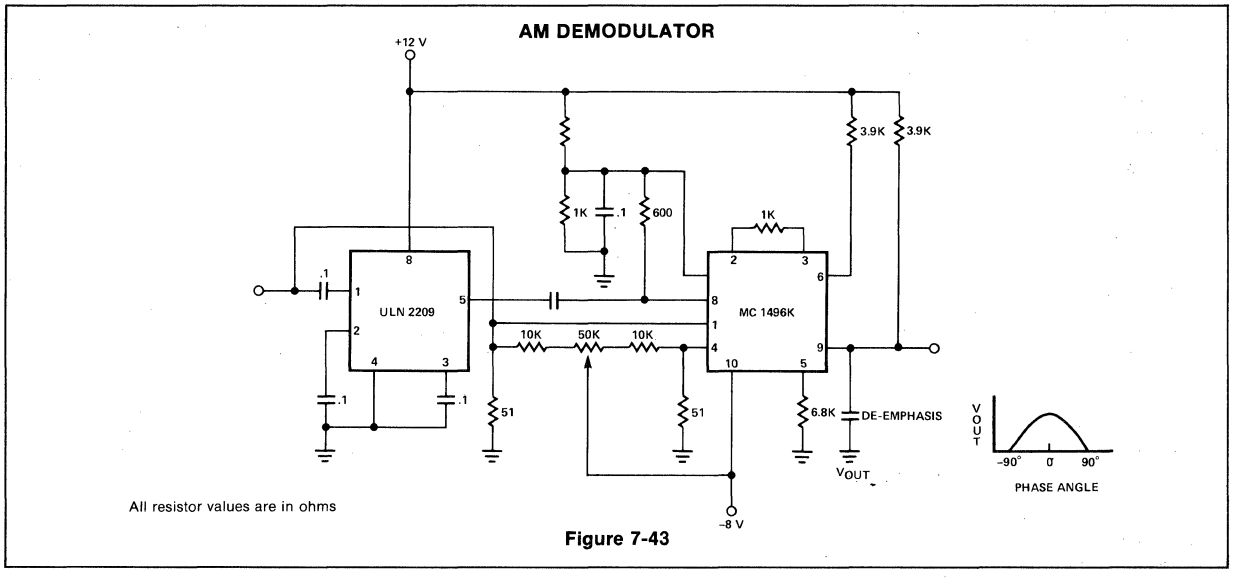


Figure 7-43

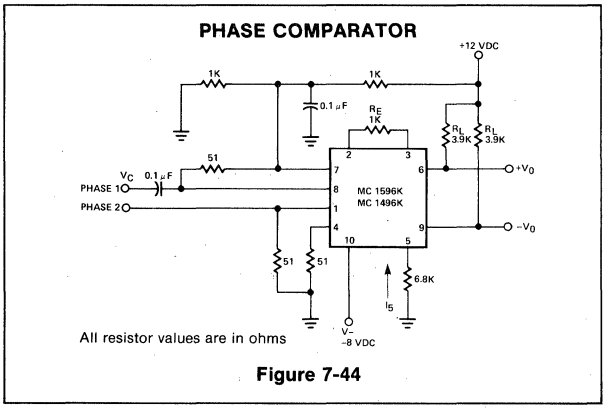


Figure 7-44

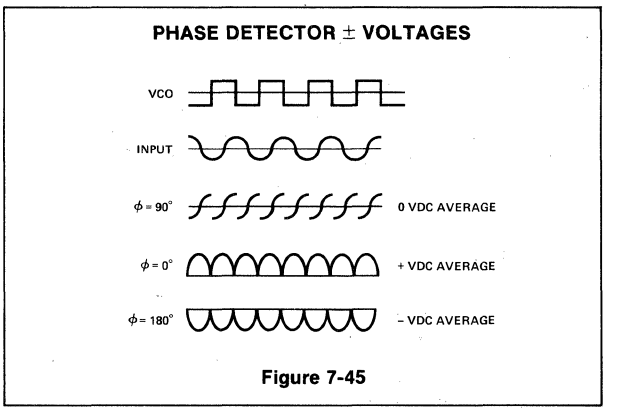


Figure 7-45

gain rather than a loss for greater resolution. Used in conjunction with a phase locked loop for instance, the balanced modulator provides a very low distortion FM demodulator.

FREQUENCY DOUBLER

Very similar to the phase detector of Figure 7-44, a frequency doubler schematic is shown in Figure 7-46. Departure from Figure 7-44 is primarily the removal of the low pass filter. The output then contains the sum component which is twice the frequency of the input since both input signals are the same frequency.

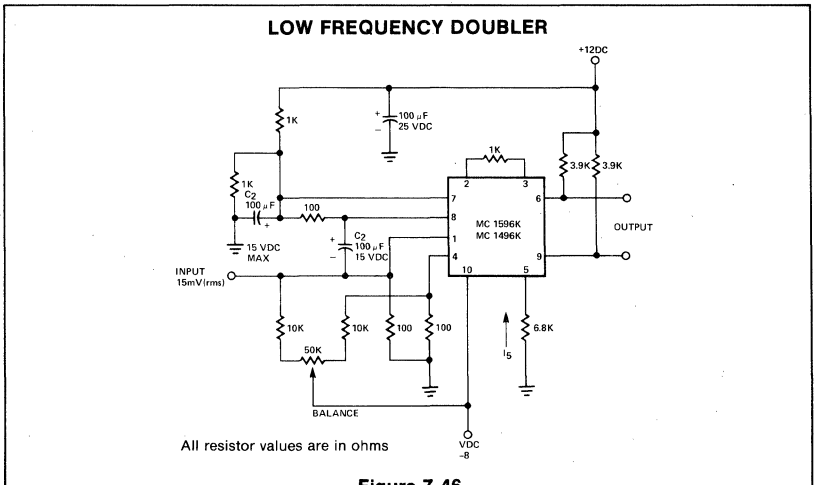


Figure 7-46

SECTION 25
CONSUMER CIRCUITS

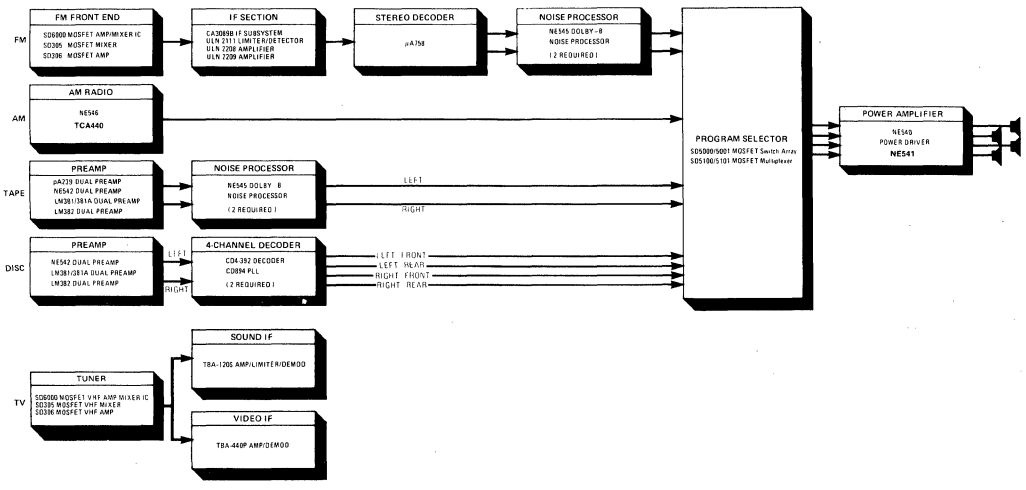


Figure 8-1

INTRODUCTION

The ever increasing voracity of the consumer electronics marketplace has led to a host of integrated circuits which replace discrete devices and simplify the old methods of doing things. For instance home entertainment systems now enjoy the use of integrated power amplifiers, pre-amplifiers, and IF systems on a single chip. More recent advancements have added the Dolby circuit and the CD-4 four channel stereo decoder in monolithic form. The following chapter will cover in detail the numerous benefits of using the new generation of consumer I.C.'s.

POWER AMPLIFICATION

Optimized for high quality and low distortion the 540 power driver is designed to drive a pair of complementary output transistors.

It features low standby current, 100mA output capability, low bias current, external current and power limiting, wide power bandwidth and a power supply operating range from ±5V to ±25V.

The 540 power driver is in essence a transconductance amplifier with an extremely linear output current swing of ±100mA with a transconductance of 3.3 Amps/Volt. The input stage converts the differential input voltage into current and the remaining circuitry is basically a current amplifier in a class B configuration. Operating in class B allows the device to drive large currents with a minimum of internal power dissipation while using current gain rather than voltage gain increases bandwidth.

COMPENSATION

Most designs utilizing the 540 should be limited to gains higher than 40dB for simplicity of compensation. At this gain level a simple capacitance to ground and a small lead network in the feedback path provide excellent stability and wide bandwidth.

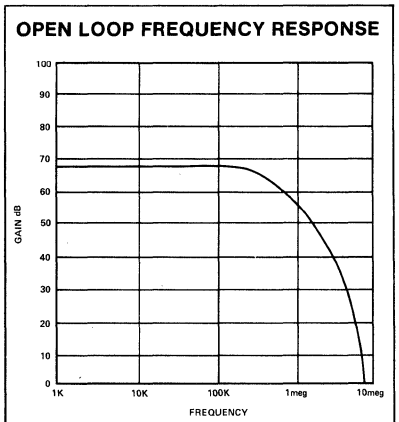


Figure 8-2

Because the 540 does possess many op amp features the compensation techniques for lower gains are also of interest. In order to simplify the precedure the current gain or transconductance is related to voltage gain. The output impedance of the 540 is 5kohms in parallel with 100pF. Therefore, the equivalent open loop voltage gain is equal to (Equation 8-1)

$$A_O = S_m \times R_O = 3.3 \times 5 \times 10^3 = 16.5k$$

The frequency response is given in Figure 8-2. Two methods of compensation can be used although one method allows only the inverting configuration. Figure 8-3 shows the lower gain configurations, which is valid for both inverting or noninverting configurations. As shown, by increasing the load capacitance the amplifier becomes more stable. Table 8-1 relates the necessary compensation capacitance to the required gain. Changes in bandwidth and slew rate are also given.

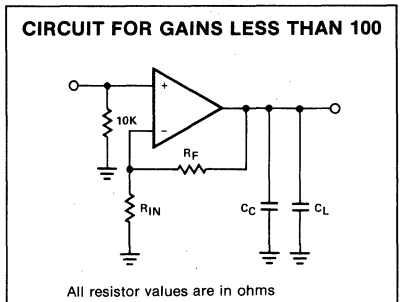


Figure 8-3

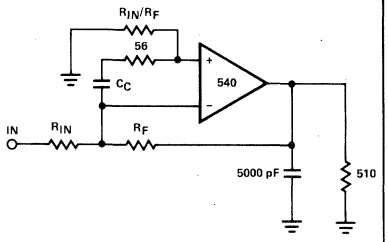
A_{CL}	GBP. (MHz)	SLEW RATE (V/μs)	POWER BAND-WIDTH (KHz)	C_L[1] (μF)	C_L (pF)
2	1	0.3	4.8	0.5	50,000
5	2.5	0.75	12	0.2	20,000
10	5	1.5	24	0.1	10,000
50	25	7.5	120	0.02	2,000
100	50	15	240	0.01	1,000
200	100	30	480	0.005	500

Table 8-1 540 Gain/Bandwidth Relationships

For closed loop gains of 2 the 540 has characteristics similar to the 741 with the exception of ±100mA output capability and little parametric change with capacitance loads up to 50,000pF. Such applications as coaxial line drivers and capacitance bridge drivers come to mind immediately and benefit greatly from this feature.

Another method of compensation applies only to the inverting amplifier configuration as illustrated by Figure 8-4. By placing high frequency attenuation across the input terminals the loop gain is reduced sufficiently to avoid oscillations even at unity gain.

ALTERNATE METHOD OF INPUT COMPENSATION



All resistor values are in ohms

Figure 8-4

Since signal levels are low at these points the slew rate and associated bandwidth are very good as illustrated by the Bode plots of Figure 8-5. The peaking exhibited by the gain of 100 configuration is less than 2dB while the 3dB bandwidth is 850kHz. More severe peaking is exhibited by the unity gain amplifier suggesting that the overall phase shift is increasing, but the 3dB bandwidth is over 2MHz.

FREQUENCY RESPONSE

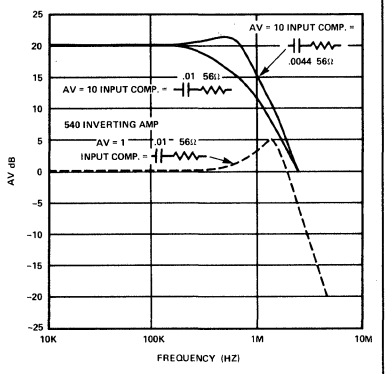


Figure 8-5

Gain settings other than those shown require increasing values of capacitance as the gain approaches 0. The approximate values can be calculated from the expression

(Equation 8-2)

$$C = \frac{0.01\mu Fd}{R_F \text{ (kohms)}} \ \mu Fd$$

where R_{series} = 56ohms and R_F is expressed in kohms.

Although 56 ohms was found to be adequate in most cases, slightly less resistance may be beneficial at unity gain while higher values will be satisfactory at higher gains. The formula of Equation 8-2 is only approximate and will depend upon the series resistance used and the capacitance loading present at the amplifier output.

POWER OUTPUT STAGES

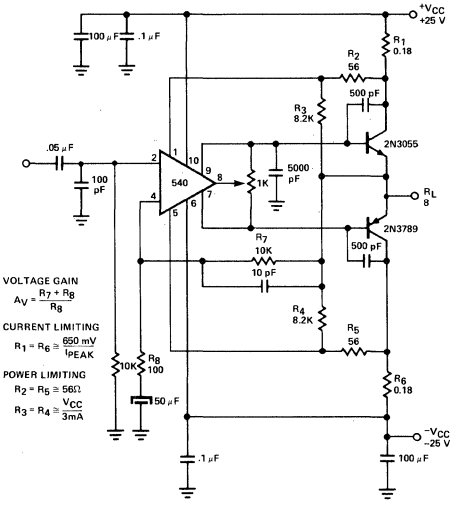
The 540 was designed specifically to drive complementary output transistors for very high output currents. Figure 8-6 illustrates the necessary connections with Figure 8-7 providing a printed circuit pattern and loading diagram.

As shown, typical operational amplifier feedback techniques are used to set the ac gain at the desired point (40dB in this case). Resistor R8 is returned to ground thru a 50μfd capacitor.

At low frequencies the capacitive reactance becomes large causing the amplifier gain to roll off to unity at dc. This is done to prevent dc voltages such as offset voltage from becoming amplified to the level where they might be detrimental to the speaker system.

The selection of power transistors is dictated primarily by the output current capability of the 540 which is ±100mA. Total harmonic distortion is a direct function of output current also. As seen from the distortion curves in the data sheet the reflected impedance from the emitter followers seen by the 540 should be as high as possible if minimum harmonic and intermodulation distortion is to be realized. Transistor types having betas greater than 50 at 3 amps of current are excellent choices. Such transistor types as the 2N3055, or the 2N5877 npn types and the 2N3789 or 2N5879 pnp types are good choices because their betas are specified at 4 amps and they are relatively inexpensive.

35 WATT POWER AMPLIFIER

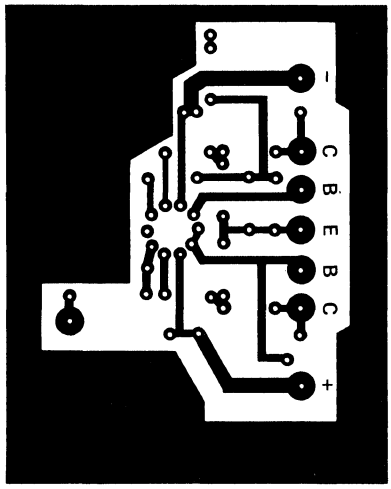


All resistor values are in ohms.

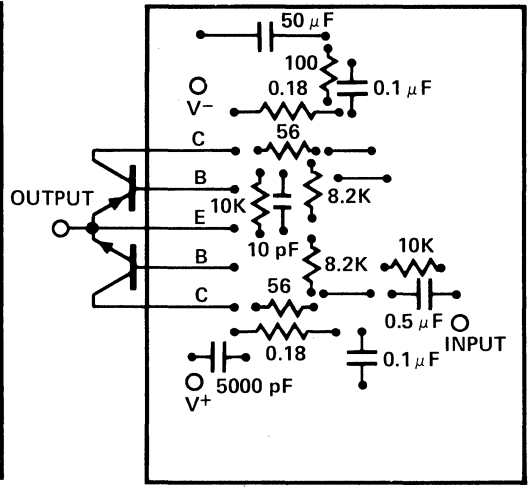
Figure 8-6

PRINTED CIRCUIT BOARD FOR 35 WATT AMP

P.C. BOARD LAYOUT
(Bottom View)



PARTS LAYOUT
(Top View)



All resistor values are in ohms

Figure 8-7

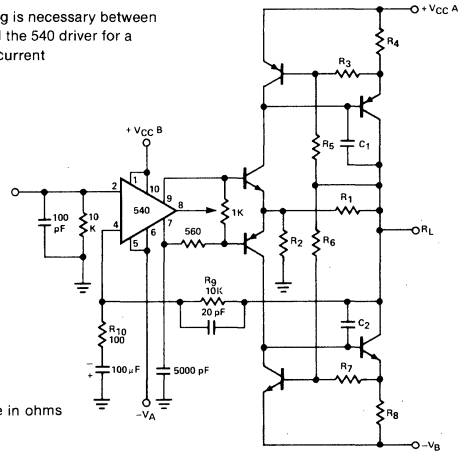
At high frequencies additional phase shifts up to 90 degrees can be contributed by the output transistors. Total phase margin in these cases reduces to less than 45 degrees which can cause instability. Miller capacitors of 500pF should be added from base to collector as shown in Figure 8-6. Close physical leads should be incorporated to assure low lead inductance.

POWER LIMITING

Power limiting is achieved by placing a resistor network around the output stage as shown in Figure 8-6. R1 and R6 are current sensing resistors with R3 and R4 being voltage sensing resistors. It is the purpose of R2 and R5 to establish a voltage just below the V_{BE} of the current limiter transistor. Only a small additional current through the output devices is necessary to increase the voltage drop sufficiently to activate the current limiters. However, as long as a load is present at the output, the voltage across resistors R3 and R4 will be reduced proportionally to the voltage developed across the load resistor allowing higher currents to be developed only under safe load limits. Typical V_{BE}/I_B curves for the limiter devices can be found in the data sheet. Power dissipation internally to the 540 can become quite high. Especially with maximum power supply voltages it is a good idea to use a clip on heat sink. For example at ±25 volts the device quiescent current is 20mA maximum. Therefore internal dissipation is 1W—in excess of package ratings without the use of a clip on radiator.

75 WATT RMS POWER AMPLIFIER

Close thermal coupling is necessary between output transistors and the 540 driver for a controlled quiescent current



All resistor values are in ohms

$\frac{R1}{R2} = \frac{V_{CCA}}{V_{CCB}}$

Current limiting

$R4 = R6 = \frac{750mV}{I_{PEAK}}$

Power limiting $= \frac{R5}{2R_3} = \frac{R_L}{R4}$ and $\frac{R6}{2R7} = \frac{R_L}{R8}$

Voltage across R_e, R7 ≈ 300 TO 400mv
I R5, R6 ≈ 4mA

AC gain minimum $= \frac{R9 + R10}{R10} \times \frac{R1}{R2}$

C1, C2 = 100 - 1000pF

Figure 8-8

HIGH POWER AMPLIFIER

Figure 8-8 shows a hook-up of the 540 driving an output stage capable of swinging 95 volts peak-to-peak. Given a 16ohm load the output rms power is then greater than 72W.

The extended voltage range is achieved by driving the load from a high current output stage which has voltage gain and which is operating from a higher supply voltage. Q1 and Q2 provide current and power limiting for the output stage. Output stage gain is

calculated from the ratio of R1 and R2 such that

(Equation 8-3)

$$R1 = \frac{V_{OUT\ (MAX)}}{V_{OUT(540)}} \cdot R2$$

This voltage gain is sufficient to amplify the peak 540 output voltage (which depends upon the 540 supply voltage) to the maximum possible output voltage (dependent upon output stage supplies).

Current limiting levels are described by

(Equation 8-4)

$$R4 = R8 = \frac{750\ mV}{I_{PEAK}}$$

By establishing a voltage and current combination to generate the necessary turn on voltage, power limiting is achieved. Power limiting is fixed by the relationship

(Equation 8-5)

$$\frac{R5}{2R3} = \frac{R_L}{R4} \text{ and } \frac{R6}{2R7} = \frac{R_L}{R8}$$

When defining values of R3, R5, R6 and R7 the current should be approximately 4mA. This allows sufficient base drive to Q1, and Q2 to assure that full limiting takes place.

The output voltage is defined as 0 volts when the bias current is calculated. Thus for a 50 volt supply the current becomes

(Equation 8-6)

$$I_B = \frac{V_{SUPPLY}}{R3 + R5} = \frac{50}{12k + 56} = 4.16mA$$

A voltage due to this current is developed across resistors R3 and R7. This voltage must be less than 750mV and is usually selected to be between 300 and 400mV. As long as the normal load is seen by the amplifier the voltage across the load subtracts from the current limiter V_{BE} voltage. This increases the output current of the amplifier until peak current is reached at full output voltage corresponding to full power.

SINGLE SUPPLY AMPLIFIERS

When one polarity supply is all that is available, the 540 can be rebiased to perform normally. For instance the 12 volt supply found in automobiles is used by the circuit of Figure 8-9. For proper operation the 540 differential inputs must see bipolar supplies. To achieve this the inputs are returned to one half of the available supply or 6 volts. All circuitry is otherwise basic with the exception of the load. The amplifier output will be 6 volts dc since the amplifier has a dc gain of one. The load must be ac coupled in order to block this voltage from the speaker. The supply current of the 540 is sensed with a 39ohm resistor for output transistor drive. This method assures that the maximum output swing is equal to the supply voltage less only the saturation voltage of the output transistors. The maximum drive current for the output devices is established by the 56ohm resistor in series with 50μFd capacitor from the 540 output to ground. The 560ohm resistor in parallel with 5000pF provides an output voltage reference as well as high frequency stabilization.

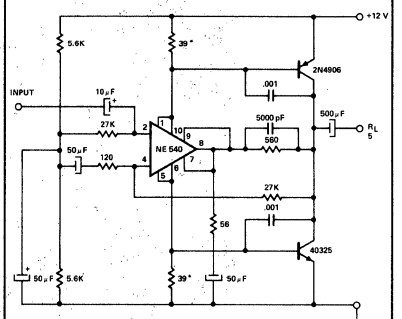
HAMMER DRIVER

The 540 can also be used as a driver for relays, solenoids, motors, or any other mechanical devices. Figure 8-10 demonstrates some typical connections. The load can either be push pull or (as in the conventional hook-up) single ended. In the push pull connection the load is driven in either the positive, negative, or both arms of the output. Depending on the input pulse polarity, either output can be selected. In addition, the output can be gated off by applying a voltage via a current limiting resistor to either pin 5 or 6 between pins 1 and 10.

The current required for these limiters is approximately 1mA for pin 1 and 100μA for pin 5.

In such applications the required input signal is defined by the maximum load voltage divided by the closed loop gain.

CAR RADIO AMPLIFIER

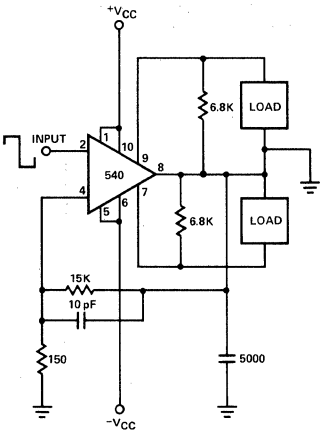


All resistor values are in ohms.

*Select for minimum crossover distortion

Figure 8-9

RELAY-SOLENOID DRIVER



All resistor values are in ohms

Figure 8-10a

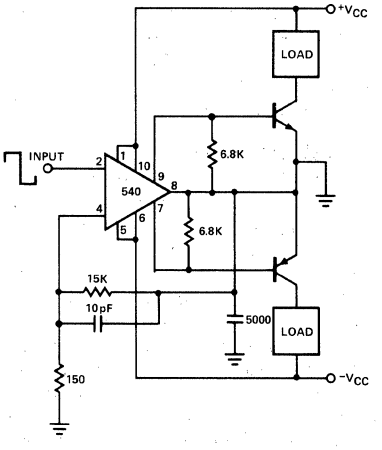


Figure 8-10b

DESCRIPTION

The NE541 High Voltage Power Amplifier has been designed primarily for use with audio equipment. Figure 8-11 shows the typical circuit configuration for evaluation of the following parameters.

The amplifier is basically a class AB1 type giving very high current gain (typically 90dB or better within the audio frequency spectrum of 20Hz to 20kHz). The high gain of the amplifier permits relatively small signal levels from a preamp stage to be used. If the amp stage uses a large feedback factor, the linearity of the preamp can be improved. The NE541 should operate with closed loop gains of 30dB or higher to permit wide band operation with relatively high capacitive loads at its output. Therefore, a preamp whose output is 200-300mVrms will result in output levels of 10-20Vrms from the NE541.

The NE541 always requires some capacitance on its output. The device has been designed with some positive feedback which aids in the high slew rate and high gain capability. The output capacitance maintains the stability of the device.

The NE541 has built-in short circuit protection. A sensing resistor in series with the output drivers turns on a base current shunt when the output current goes too high. This limit is set to approximately 100mA typically, but will have variations due to processing and manufacturing tolerances. In addition to the built-in short circuit protection, the current can be limited by use of external circuitry as shown in Figure 8-12.

The wide band operation of the device as seen in Figure 8-13 plus the nominal low offset voltages inherent to the amplifier (V_{OS} and I_{OS}) will permit the usage of the device in several other areas, such as instrumentation amplifiers, servo drivers and power regulators.

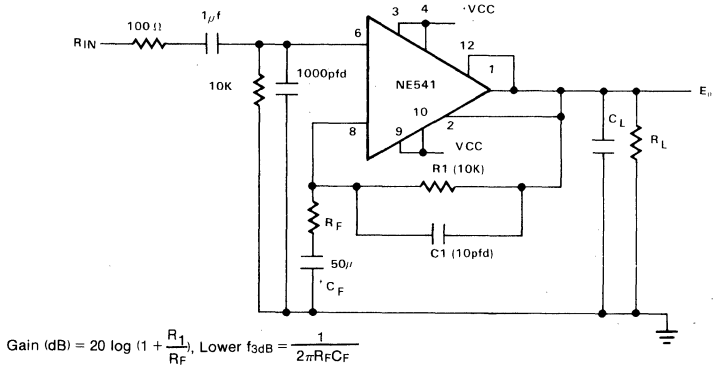
Several input configurations can be incorporated to add either bass or treble boost to the system. These configurations should be evaluated by the designer to best fit his needs. For high power systems additional speaker compensation can be included.

FM DETECTOR—LIMITER

The ULN2111 was designed primarily for FM and TV sound IF applications. This circuit is comprised of a three stage limiting amplifier with a voltage gain of 60dB and a balanced quadrature phase detector as shown in Figure 8-17.

Comprised of three identical differential amplifier stages, the amplifier—limiter is directly coupled thru emitter followers. The direct coupling is possible by using an

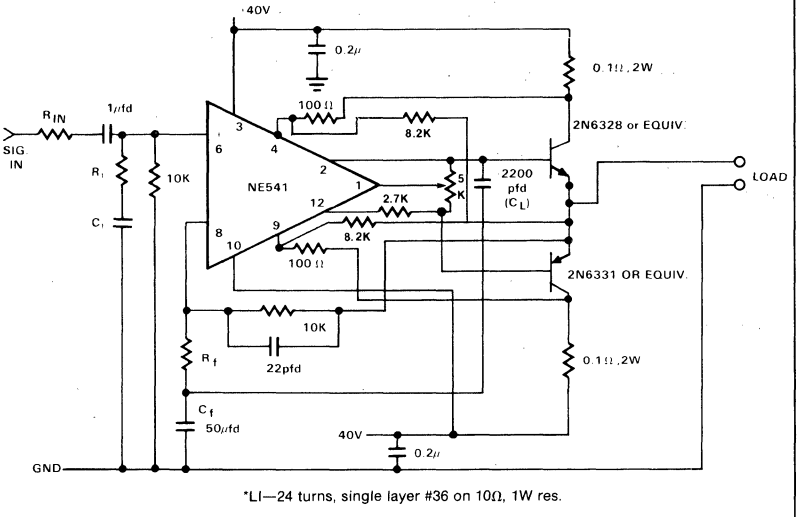
TYPICAL CIRCUIT CONFIGURATION



Gain (dB) = 20 log $(1 + \frac{R_1}{R_F})$, Lower $f_{3dB} = \frac{1}{2\pi R_F C_F}$

Figure 8-11

75 WATT AMPLIFIER WITH EXTERNAL CURRENT LIMITING



*LI—24 turns, single layer #36 on 10Ω, 1W res.

Figure 8-12

GAIN PHASE vs FREQUENCY

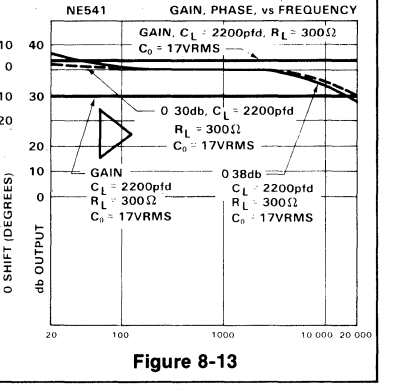


Figure 8-13

BASIC OPERATING EQUATIONS

Lower 3dB

$$f = \frac{0.16}{R_f C_f}$$

Bass Emphasis

$$e_{in\ pin\ 6} = \frac{10k}{R_{in}}\left(\frac{1 + S1}{1 + S2}\right)$$

where: $S1 = jwC1R1$

$S_2 = jwC1\ (R1 + R2)$

Amplifier Gain (Midband)

$$A_{CL} = 20 \log_{10} \frac{10k + R_f}{R_f}\ R_f \text{ in } k\Omega$$

Loop gain ≈ 90dB - A_{CL}

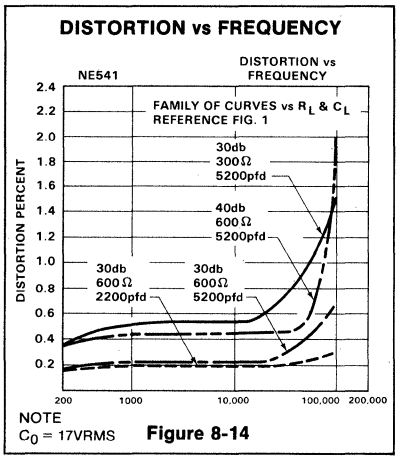


Figure 8-14

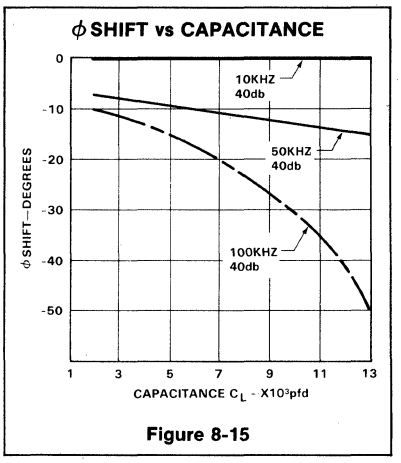


Figure 8-15

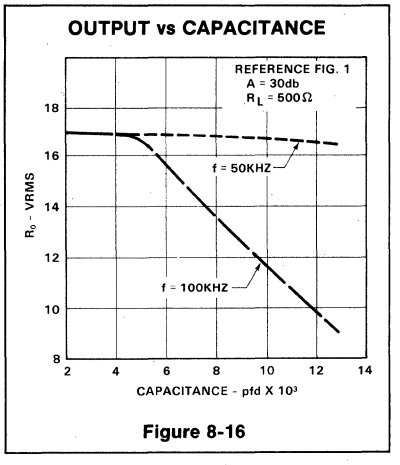


Figure 8-16

internally generated voltage reference formed by a series diode string, dc level shifting between stages, and overall dc negative feedback.

To provide for flexibility in the driving of different phase-shift networks, two limiter outputs are available. One provides the fully limited output voltage of 1.4V peak to peak which is applied directly to the coincidence detector. A second low voltage output supplies the same signal at an attenuation of -20dB.

FM detection is accomplished with the balanced product detector shown in Figure 8-18. As has been pointed out in the phase detector discussions of chapter 7 the balanced product detector produces an output dependent upon the phase of the two input signals. By phase shifting, with a simple LC network, one signal from the other by 90°, the carrier signal becomes non-existent and the audio modulation is recovered. For any level of the inputs V1 and V2 of Figure 8-18 the output voltage becomes

(Equation 8-7)

$$Vo = \frac{V_R}{t}\int_o^t U1\,(t)\,U2\,(t)\,dt$$

(Equation 8-8)

where

$$U_1 = \tanh\frac{V1\,(t)}{2kT/q}$$

(Equation 8-9)

$$U2 = \tanh\frac{V2\,(t)}{2kT/q}$$

(Equation 8-10)

and

$$V_R = \frac{I_O R}{2}$$

Equation 8-7 shows that the output is proportional to the product of the two input functions U(t).

The U function accounts for any symmetrical limiting in the base-emitter junctions and can be approximated for linear opera-

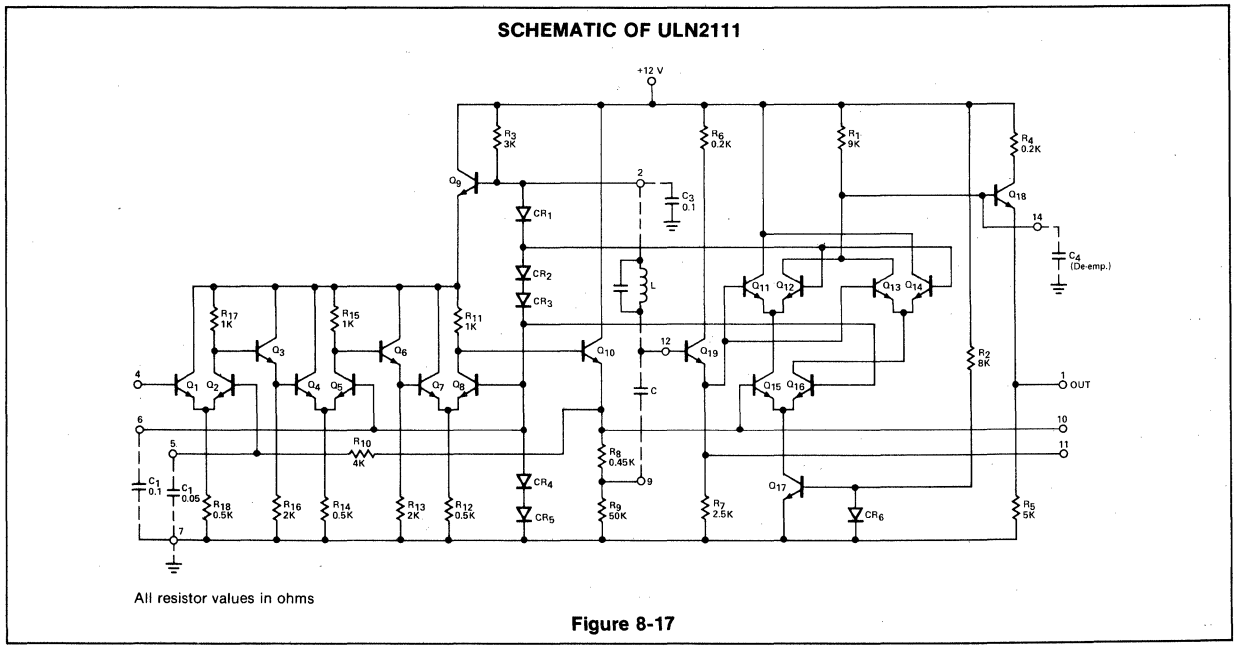


Figure 8-17

MONOLITHIC MULTIPLIER BLOCK

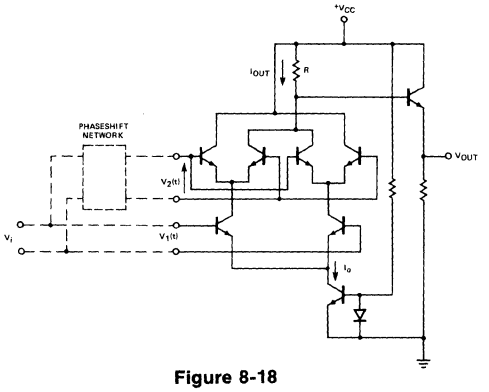


Figure 8-18

tion and hard-limiting by the input voltage itself or by switching function, respectively.

There are two modes of operation: high level switching and low level switching. The frequency-transfer characteristics for each operating mode are given by:

(Equation 8-11)

$$\frac{V_o}{V_R} = \frac{2}{\pi} \arctan a \text{ (high level)}$$

(Equation 8-12)

$$\frac{V_o}{V_R} = \frac{2}{a}\left(\frac{|V1|_o}{2kT/q}\right)\frac{a}{1+a^2} \text{ (low level)}$$

(Equation 8-13)

where

$A = 2Q\frac{\Delta F}{F_o}$ = normalized frequency deviation

and

$|V1|_o$ is the magnitude of V1 at the center frequency.

Equation 8-17 and 8-18 are plotted in Figure 8-19. For low level operation, the amplitude of the bell-shaped response of the tuned circuit provides the response fall-off on either side of the center frequency, and the familiar S-shaped transfer function is obtained. The peak-to-peak separation of the source is directly related to the 3dB bandwidth of the tuned circuit. For high-level operation and within a large range of frequency deviations, the amplitude response of the network transfer function is eliminated, and the response is directly that of the phase-shift properties of the LC network.

The conversion efficiency, V_F defined as the slope of the transfer characteristic at the center frequency, can be shown to be:

(Equation 8-14)

$$V_F = \left(\frac{d\,Vo}{d\,a}\right)_{a=0} = \frac{2}{\pi} V_R \tanh\frac{|V1|_o}{2kT/q}$$

Figure 8-20 shows the measured values of the conversion efficiency as a function of the magnitude of the driving voltage V1, at the center frequency 4.5MHz.

DEFINITIONS

In order to properly utilize the design advantages offered by the ULN2111 it is necessary to clarify those quantities used in design evaluations.

Center Frequency—the fm modulated carrier frequency designated by f_o.

Frequency Deviation—the amount of frequency change of the carrier designated Δf

Network Selectivity—the Q of the tuned circuit used for phase shifting ($Q = \frac{fo}{BW}$ and should be greater than 10)

Conversion Efficiency—the slope of the fm "S" curve specified by $(dV_{OUT}/d\theta) = $ VOLTS per radian.

Normalized Deviation—For simple LC networks the quantity $2Q\frac{\Delta F}{fo}$ is designated by the letter a.

GENERAL CONSIDERATIONS

The ULN2111 is very versatile and easy to use. Only a few general requirements are needed.

1. As with any integrated circuit, especially those operating at high frequencies, the power supply at pin 13 should be bypassed with a ceramic disc of the 05.μfd value range.
2. Amplifier gain is 60dB at high frequencies. This can be troublesome unless good high frequency layout techniques are practiced. Ground planes are very helpful and physical separation of inputs and outputs is mandatory.
3. A dc path less than 300Ω should be provided between pins 4 and 6.
4. Decoupling capacitor leads at pins 5, 6, and 12 should be as short as possible.
5. The maximum ac load current can be increased by adding an external resistor between pins 1 and 7. The minimum value for this resistor is 800Ω, giving a minimum load current of 4mA RMS.
6. A dc path less than 100Ω shall be provided between pins 2 and 12. No other biasing provisions are required.

CALCULATED TRANSFER CHARACTERISTICS FOR HIGH AND LOW LEVEL CASES

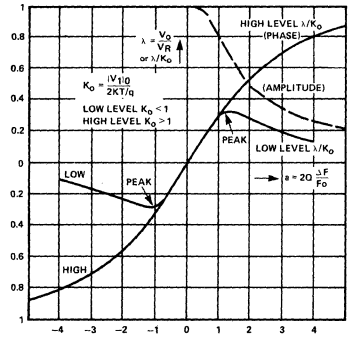


Figure 8-19

MEASURED CONVERSION EFFICIENCY OF THE MONOLITHIC FM DETECTOR

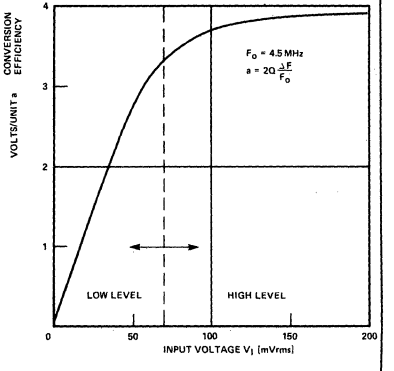


Figure 8-20

PERFORMANCE

In an FM detector and limiter, the major figures of merit include recovered audio amplitude, dynamic range, and total harmonic distortion.

Audio recovery is affected primarily by the resonant LC network and the injection level at the detector input.

To obtain a proper value for audio recovery, specific characteristics of the S curve are recommended. A choice of slope of the S curve gives a specified value for dV/dF, which is the basic expression of audio recovery. A choice of a peak-to-peak separation desired and a choice of peak-to-peak voltage required at the nodes of the S curve determine the Q of the LC resonant network and injection level.

The peak-to-peak separation is usually defined by the service for which the system is intended. This value is 550kHz for FM and 150kHz for TV. An approximation of the circuit Q can be made by the equation:

(Equation 8-15)

$$Q = \frac{F_o}{\Delta f}$$

where f_o is the center frequency and Δf is the 3dB attenuation bandwidth. For TV service, the value of circuit Q is approximately

$$Q = \frac{4.5X10^6}{150X10^3} = 30$$

Although the desired circuit Q is fairly low (indicating a high-L network), it is desirable to use a high-C network. The input to the detector introduces some variable capacitance. This can be minimized through the use of at least 100pF as the C part of the resonant circuit. Inductor choice, along with this capacitance value, yields a network with a Q somewhat higher than desired. This can be reduced by using a paralleled resistor across the network.

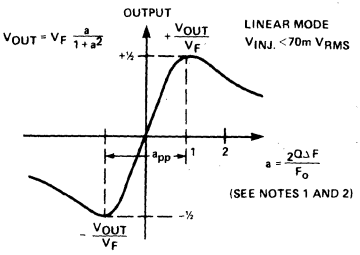
Figure 8-21 shows the transfer characteristic for a simple LC network, while Figure 8-22 shows the ULN2111 FM Detector and Limiter used for TV interfacing.

Typical driving capabilities of the ULN2111 at 4.5MHz are shown in Figure 8-23.

ULN2111A Driving Capabilities at f_o = 4.5MHz

Fig.	$R_L(\Omega)$	Δf = 7.5kHz	Δf = 24kHz	Remarks
A	2000	220	650	No Clipping
B	200	130	400	No Clipping
C	200	220	650	Clipping at V_o = 500Vrms

TRANSFER CHARACTERISTICS FOR A SIMPLE LC NETWORK



OUTPUT = f (NORMALIZED DEVIATION)
(The units along the vertical axis are arbitrary units.)

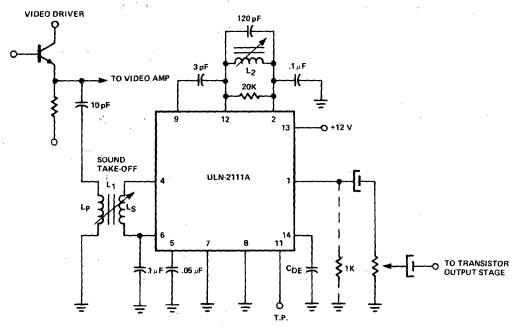
Linear mode: Operation of the FM detector with no limiting after the phase shift network.

NOTES

1. V_F defines the slope of the FM transfer characteristic, at origin:
   $V_f = \frac{dV_{out}}{da}$ at a = 0
   V_F is primarily a function of bias current in the detector and injection voltage.
   V_F will decrease with decreasing V_{CC} or V_{inj}.
2. a = normalized frequency deviation:
   $A = \frac{20\Delta F}{F_o}$
   a = 1 for peak deviation

Figure 8-21

TV INTERFACING



All resistor values are in ohms

Figure 8-22

ULN2111A DRIVING CAPABILITIES AT f_o = 4.5 MHz

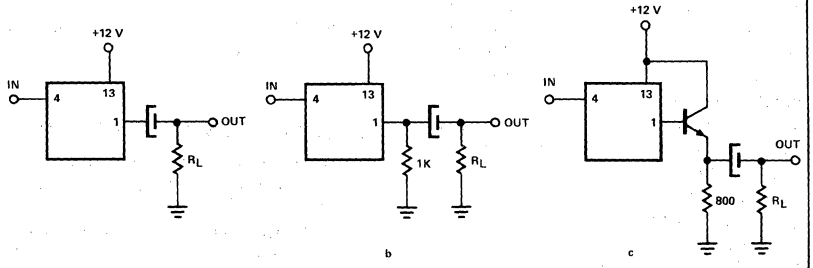


Fig.	R_L (Ω)	Δf = 7.5 kHz	Δf = 24 kHz	Remarks
A	2000	220	650	No Clipping
B	200	130	400	No Clipping
C	200	220	650	Clipping at V_o = 500 mV rms

All resistor values are in ohms

Figure 8-23

The final component required is a small decoupling capacitor placed between the network and the low amplifier output. To insure linear detector operation, the reactance of this capacitor should be substantially large, as compared to the impedance of the tuned circuit at resonance.

The voltage developed across the simple tank circuit is applied to the other two balanced gates of the coincidence detector through emitter follower Q1,which provides a capability for monitoring the LC network tuning without any appreciable loading effects. It also reduces, to a great degree, the capacitance reflected to a tuned circuit, leading to a negligible shift in the tuning as a function of incoming signal strength.

When designing the LC network it is necessary to provide the following requirements:

1. Capacitively drive the network from low impedance (pins 9 or 10).
2. Pins 2 and 12 should see a dc path less than 100 ohms.
3. The required V_2 (Figure 8-18) must be supplied at pin 12 by the network.
4. The phase of the network at fo must be $\pi/2$ or an odd multiple thereof.
5. To minimize output distortion a maximum normalized deviation (a) of less than .3 should be used.

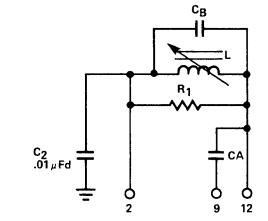
Figure 8-24 gives the recommended networks for use at 10.7MHz and 4.5MHz.

	COMPONENT VALUE	
	TV 4.5MHz	Fm 10.7MHz
L Inductance	7-14μH	1.5-3μH
L Nominal Q (unloaded)	50	50
L DC Resistance	50Ω	50Ω
C_A	3pF	4.7pF
C_B	120pF	120pF
R1	20k	3.0K
Network Q	30	20

The other factor governing audio output is the injection value at the input to the detector. The optimum value is 60mVrms at the resonant frequency of the network. Figure 8-20 shows a normalized plot of V_{inj} as a function of V_f, where V_f represents a normalized output for any single LC network. Note that the output (V_f) has a linear relationship to V_{inj} up to approximately 50mV. Above this value, the function breaks into a curve, then flattens out, indicating that the detector is in a switching mode.

Figures 8-25 and 8-26 demonstrate the detector operation in the linear (low injection) mode and the switching (high injection) mode. Note that in the linear mode, a greater portion of the S curve is linear, thus producing lower distortion than in the switching mode. For best operation, the low injection mode is recommended where V_{inj} is set as high as possible. The optimum injection value is 60mVrms.

TYPICAL PHASE SHIFT NETWORKS



	COMPONENT VALUE	
	TV 4.5 MHz	FM 10.7 MHz
L INDUCTANCE	7-14 μH	1.5 – 3μH
L NOMINAL Q (UNLOADED)	50	50
L DC RESISTANCE	50Ω	50Ω
C_A	3pF	4.7pF
C_B	120pF	120pF
R_1	20K	3.0K
NETWORK Q	30	20

Figure 8-24

FM TRANSFER CHARACTERISTICS LOW Vij OPERATION

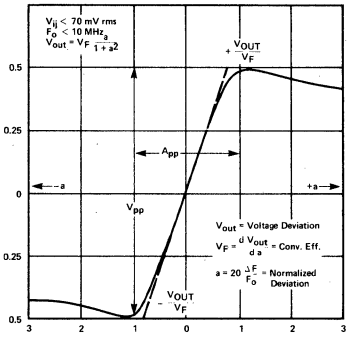


Figure 8-25

FM TRANSFER CHARACTERISTICS HIGH Vij OPERATION

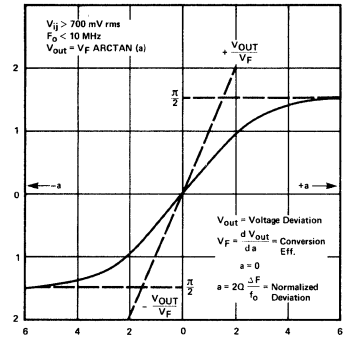


Figure 8-26

Introduction

The phase locked loop (PLL) has been used for many years in consumer equipment. Due to the nature of FM STEREO MULTIPLEX SYSTEMS, where prime importance is the channel separation, discrete systems lacked the tracking ability over wide temperature and voltage ranges to be done economically.

The development of the monolithic PLL and improvements in IC processing has made the Phase Locked Loop FM Stereo Multiplexer Decoder a reality.

Major Advantages

The economic advantages in using the PLL multiplex decoding system are not only cost reduction, by eliminating peripheral components, but the man hour cost reduction by eliminating turning coils, thereby eliminating tedious alignment procedures.

The cost advantages are extremely signifcant and are in addition to the following:

- 45 dB Channel Separation
- Automatic Stereo/Mono Switching
- Stereo Indicator Lamp Driver With Current Limiting
- High Impedance Input—Low Impedance Outputs
- 70dB SCA Rejection (Subsidiary Carrier Authorization)
- One Adjustment for Complete Alignment
- 10V to 16V Supply Voltage Range

FM Stereo Multiplex Subcarrier and Pilot

The two (2) basic signals differentiating an FM stereo multiplex signal from an FM monaural signal are the 19kHz pilot and the 38kHz subcarrier. The frequency and phase relationship of these signals is well defined.

Earlier systems had to reconstruct the 38kHz subcarrier by using the 19kHz pilot. This system required frequency multipliers and selective filters (coils). Since maximum channel separation is directly related to proper phasing, alignment procedures were extremely critical and therefore expensive. In addition, long term stability and performance were degraded due to component aging, and temperature.

Use of the PLL as the multiplex decoder eliminated these short comings since the phase accuracy of the 38kHz signal is limited only by the loop gain of the system and the free running oscillator stability. Both of these parameters are easily controlled, providing easy, rapid adjustment and excellent long term stability.

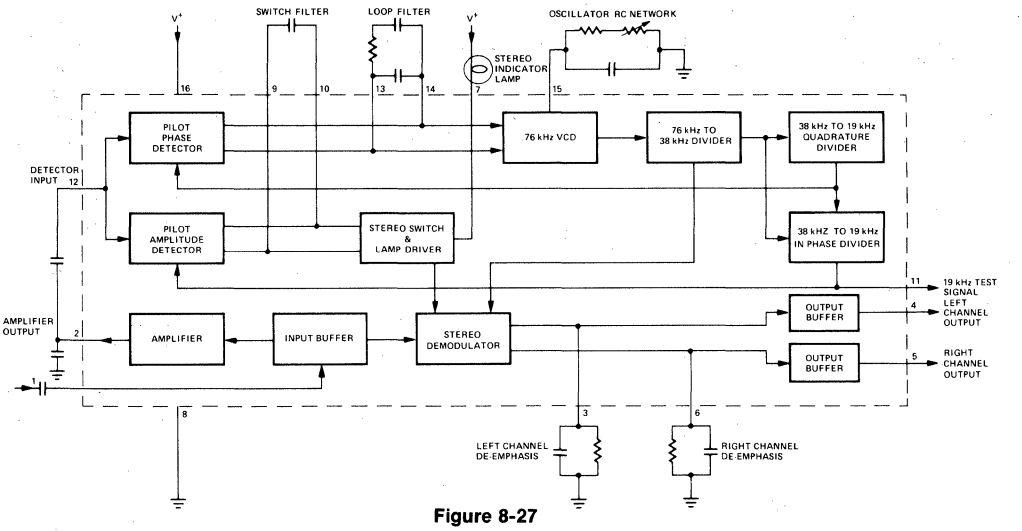


Figure 8-27

General Description

The μA758 is a monolithic Phase Locked Loop FM Stereo Multiplex decoder using the 16-LEAD Dip AA Package. This integrated circuit decodes an FM Stereo Multiplex Signal into Right and Left audio channels while inherently suppressing SCA information when it is contained in the composite input signal. Internal functions include automatic mono-stereo mode switching and drive for an external lamp to indicate stereo mode operation.

The μA758 operates over a wide supply voltage range and uses a low number of external components. It has only one control to adjust a potentiometer to set oscillator frequency. No external coils are required. The μA758 is suitable for all line-operated and automotive FM Stereo Receivers.

Referencing Figure 8-27

The upper row of blocks comprises the PLL which regenerates the 38kHz subcarrier, necessary for multiplex signal demodulation. The basic 76kHz generator is voltage controlled, and is divided by 2 to insure a 50% duty cycle 38kHz internally generated signal. This symmetry is necessary for maximum left/right channel separation and SCA rejection (band centered at 67kHz). Dividing the 38kHz by 2 generates the 19kHz signal necessary to lock on to the incoming pilot signal. A second 19kHz signal is generated which is in quadrature to the first internally generated 19kHz signal and in phase with the pilot. This second 19kHz is mixed in a quadrature (synchronous) phase detector to operate the stereo switch and lamp driver circuitry.

When a stereo signal is present, the stereo switch enables the stereo demodulator and when a stereo signal is not present the demodulator is disabled allowing the system to reach optimum noise performance.

Functional Operation

To aid in understanding the system operation, the μA758 equivalent circuit has been broken down into subsections as follows. Reference Figure 8-28.

I Buffer Amplifier and Bias Supplies
II Demodulator
III Stereo Switch and Lamp Driver
IV Voltage Controlled Oscillator
V Frequency Dividers
VI Pilot Phase and Amplitude Defectors

SIGNETICS LINEAR INTEGRATED CIRCUITS • μA758
Equivalent Circuit

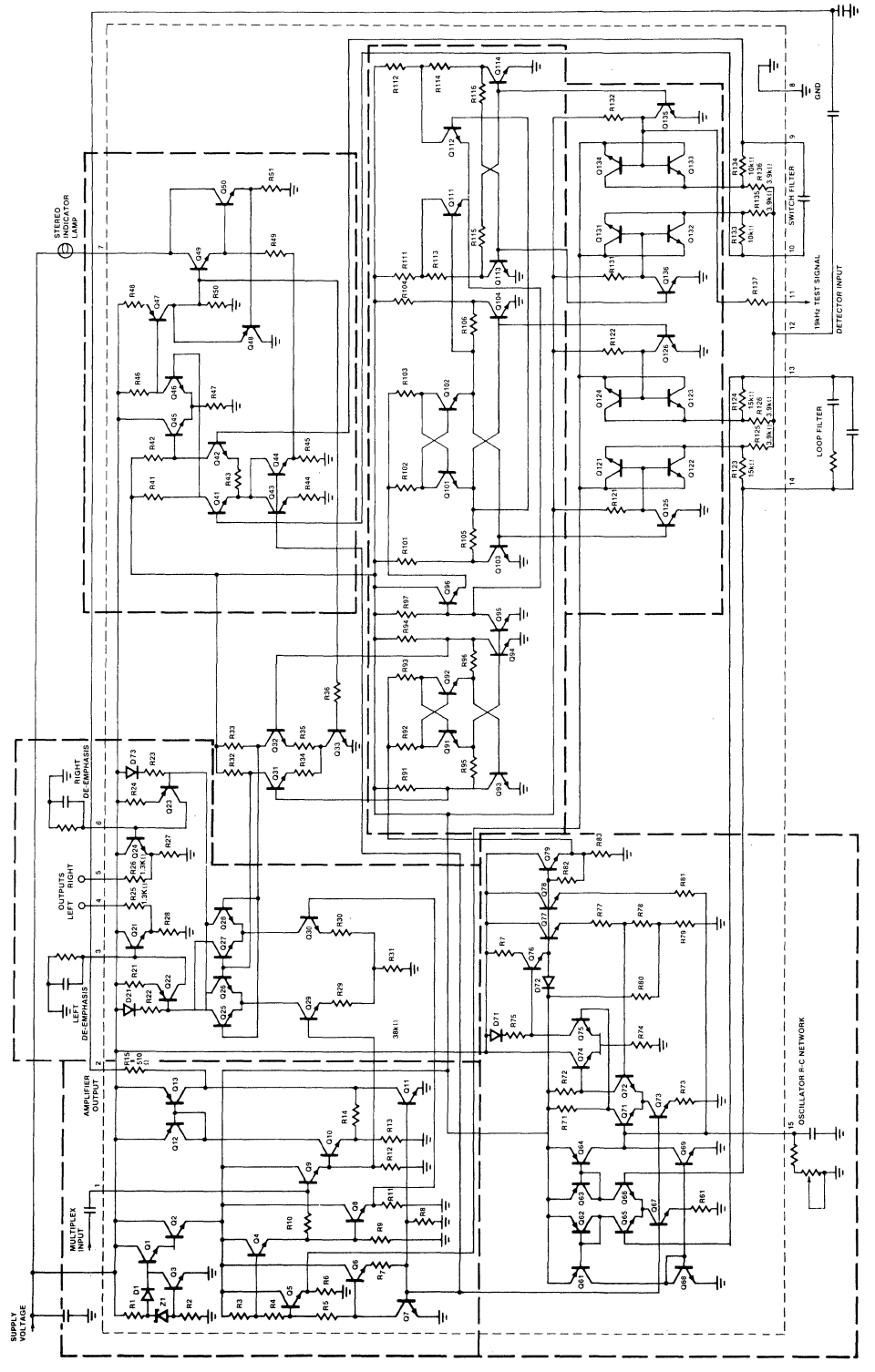


Figure 8-28

I Buffer Amplifier and Bias Supplies (Figure 8-29)

The zener diode Z, and its associated transistors generate a 6V internal voltage reference source. From this 6V reference, additional bias levels are established via resistors R3, R4, and R5. In addition transistor Q7 acts as the control source for several current mirrors; Q11 in the Buffer Amplifier, Q43 and Q44 in the Stereo Switch and Lamp Driver (III) and Q67 and Q73 in the Voltage Controlled Oscillator (IV).

The input Buffer Amplifier (Q8, Q9) level shifts the composite multiplex input signal to 2 levels each in phase with each other.

Transistors Q10 - Q13 amplify this same signal by the ratio of:

$$A = \frac{R_{14}}{R_{13}}$$

This amplified signal, the gain of which is independent of supply voltage variation, is fed to the Pilot Phase and Amplitude Detectors (VI).

II Demodulator (Figure 8-30)

The basic demodulator, Q25 - Q30, is a fully balanced detector similar to standard phase locked loop types. The addition of resistors R29, R30, and R31 introduces a small offset to allow a small multiplex signal in the collector of Q30. This signal compensates the cross talk components inherent to the synchronous switching demodulation process.

Switching to the left and right channels is accomplished through Q25 and Q26 when the 38kHz drive is present at their bases. This occurs when Q33 is "ON." When Q33 is off, a dc bias is placed at the bases of Q25 and Q26 through resistors R32 and R33, this automatically converts the system to monophonic operation.

Supply voltage rejection is accomplished at the demodulator outputs by converting the audio to current supplies in Q23 and Q24. The voltage developed across pnp transistors is

$V_e = (V^+ + v_{mod}) - (V_{be} + V_{D1} + [R22\ i_{ac}] + v_{mod})$

where V_{be} = base-emitter voltage across Q22 and Q23

V_{mod} = modulation on the power line

V_{D1} = diode drop in D21

$(R22)i_{ac}$ = voltage drop due to current in the demodulator

Simplifying the above reduces to

(Equation 8-16)

$$V_e = V^+ - (V_{be} + V_{D1} + R22\ i_{ac})$$

The output voltage developed is

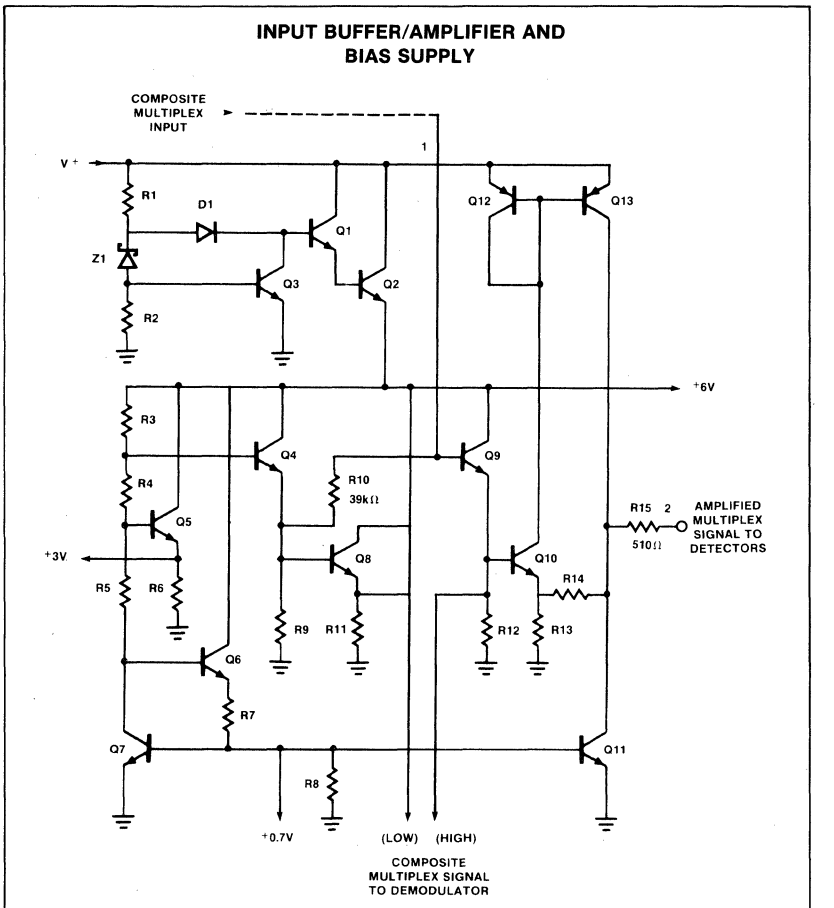


Figure 8-29

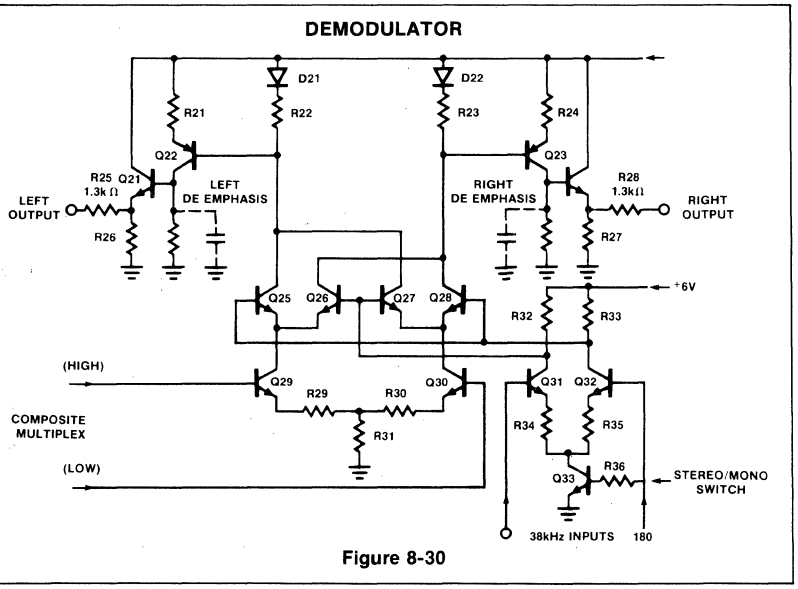


Figure 8-30

(Equation 8-17)

$$V_{out} = \left(\frac{V_e}{R21}\right) R_{ext}$$

where R_{ext} = external resistor

The output voltage at pins 4 and 5 are provided through 1.3k resistors driven by Emitter Followers Q21 and Q24.

III Stereo Switch and Lamp Driver (Figure 8-31)

The pilot amplitude detector differential voltage is sensed by the differential amplifier Q41 and Q42. This pair in conjunction with their load resistors (R41, R42) control amplifiers Q45, Q46. Positive feedback action is achieved through Q47, R50, Q50 and R46 (which turns off Q44).

The turn on threshold is the differential input voltage required to overcome the offset voltage in R43 times the current summation of I_{R44} and I_{R45}. When the lamp is ON, Q44 is off and the differential voltage across R43 is reduced by the amount (I_{R45} x R_{43}), which means a lower turn off voltage is required. This voltage difference is referred to as the switch hysteresis.

Transistors Q48 senses the current across R51 which therefore controls the maximum current in the Stereo Indicator Lamp.

(Equation 8-18)

$$I_{max} = \frac{V_{be\ Q48}}{R151}$$

IV Voltage Controlled Oscillator (Figure 8-32)

The basic oscillator Q71 - Q79 is an RC relaxation type which generates a positive low duty cycle, 76kHz output. The frequency is established by equations 8-19 and 8-20.

The control voltage from the phase detector into the transconductance amplifier Q61 - Q69 converts the differential error to a bidirectional single ended current drive to the oscillator.

Voltage on the capacitor is compared with the set voltages by the differential input stage Q71, Q72. This feeds Q74, Q75. The output of Q75 drives a PNP inverter, Q76, (whose action eliminates power supply modulation as described in the demodulator section of this note), when these set limits are reached the direction of charge reverses.

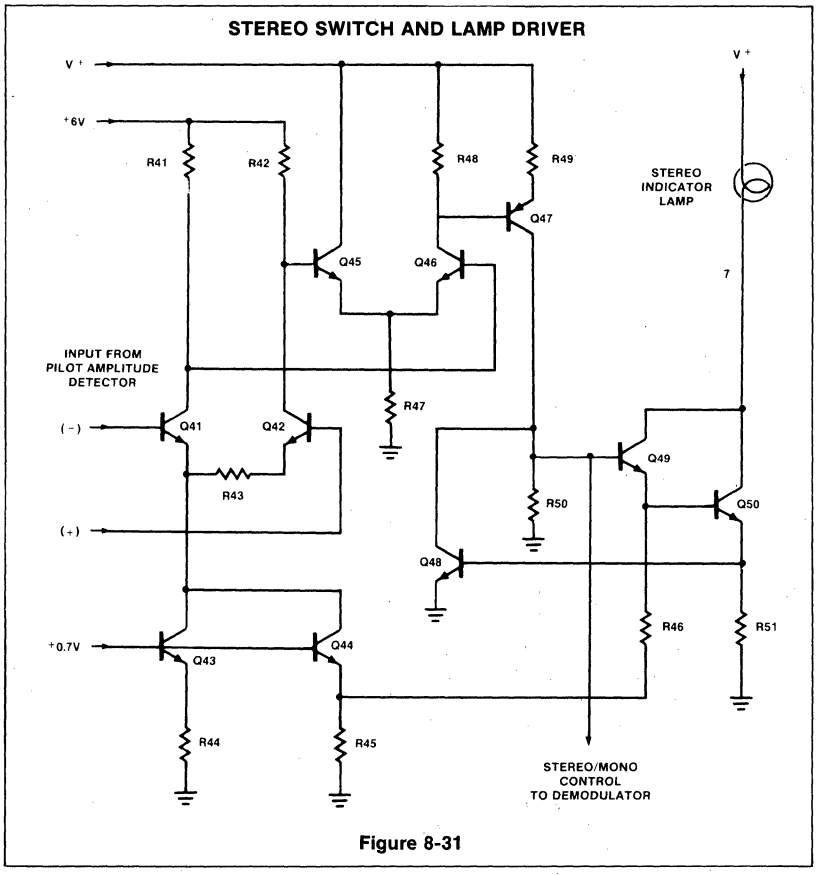


Figure 8-31

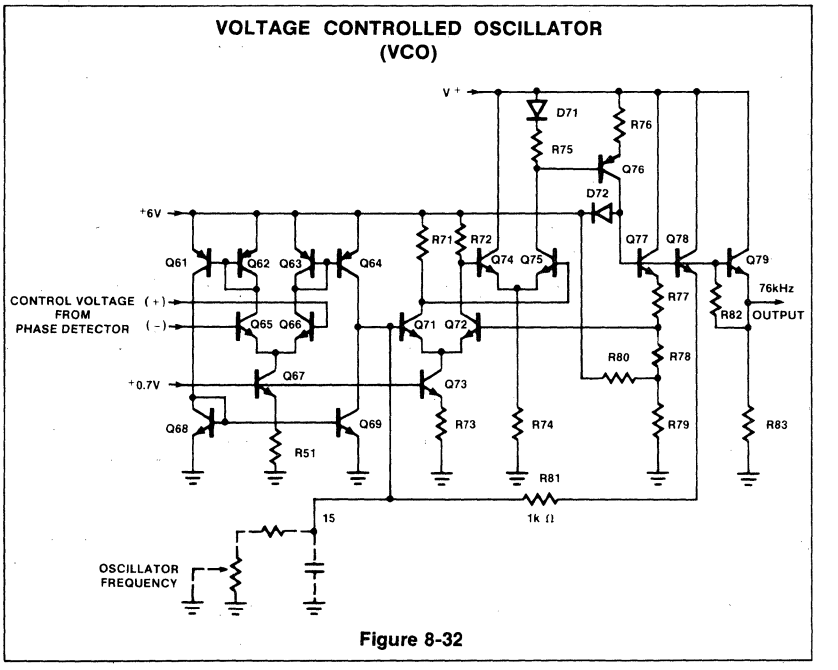


Figure 8-32

Lower set voltage is set by R79, R80, and the regulated 6V supply. The upper set voltage (V_H) involves two (2) additional resistors R77 and R78 and is established when Q76 turns on Q77. Both set levels are referenced to the regulated 6V supply and are therefore dependent only on resistor ratios. (Proper design layout should also eliminate temperature variations.)

Capacitor charging is through Q78 and R8 and discharging through the external fixed resistor.

Equations 8-19 and 8-20 of Figure 8-33 are first order expressions for the change and discharge periods.

Q79 supplies a positive output pulse necessary to operate the 38kHz dividers.

V Frequency Dividers (Figure 8-34)

Transistors Q91 through Q94 form a simple divide-by-two circuit which converts the pulse output from the 76kHz oscillator to a 38kHz square wave (reference 5).

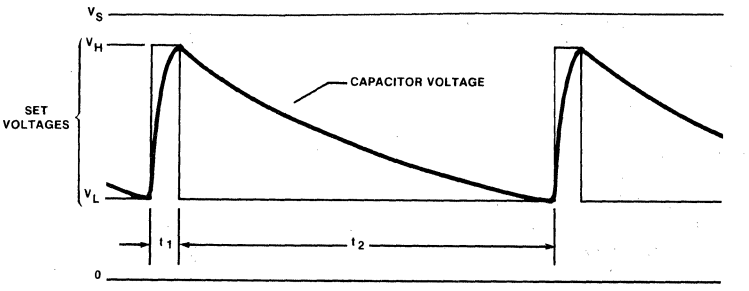
The divider changes state during the positive excursion of the input pulse supplied from the emitter of Q79 in the oscillator. Initially, when the input is low, Q91 and Q92 are OFF and we may arbitrarily assume Q93 is ON and Q94 is OFF.

As the potential on the input rises, Q91 starts conduction before Q92 because the emitter of Q91 is at a lower potential than the emitter of Q92. (The emitter of Q91 is connected through R95 to the collector of Q93 which is in saturation, whereas the emitter of Q92 is at the $V_{BE(ON)}$ potential of Q93). Since Q91 is ON, the current from both R92 and R93 flows through the emitter of Q91 into R95. As this current increases, the rising voltage at the emitter of Q91 turns Q94 ON which removes base drive to Q93 and turns it OFF, thus producing a change of state in the divider. Even though the relative potentials at the emitters of Q91 and Q92 are now reversed, current continues to flow in Q91 for the duration of the positive input because Q92 is held OFF by Q91. When the input returns to a low potential, Q91 turns OFF. The divider remains in its present state until driven by the next positive going input.

Oppositely phased 38kHz outputs to the demodulator are taken from the collectors of Q93 and Q94. Transistors Q95 and Q96 are used to drive the two 38kHz dividers.

The 38kHz Quadrature Divider has an identical configuration to the 76kHz divider. A change of state occurs with each positive excursion of the 38kHz input signal from the emitter of Q96.

OSCILLATOR WAVEFORMS



Basic timing equations:

(Equation 8-19)

$$t1 = R81\ C\ 1n\ \frac{V_S - V_L}{V_S - V_H}$$

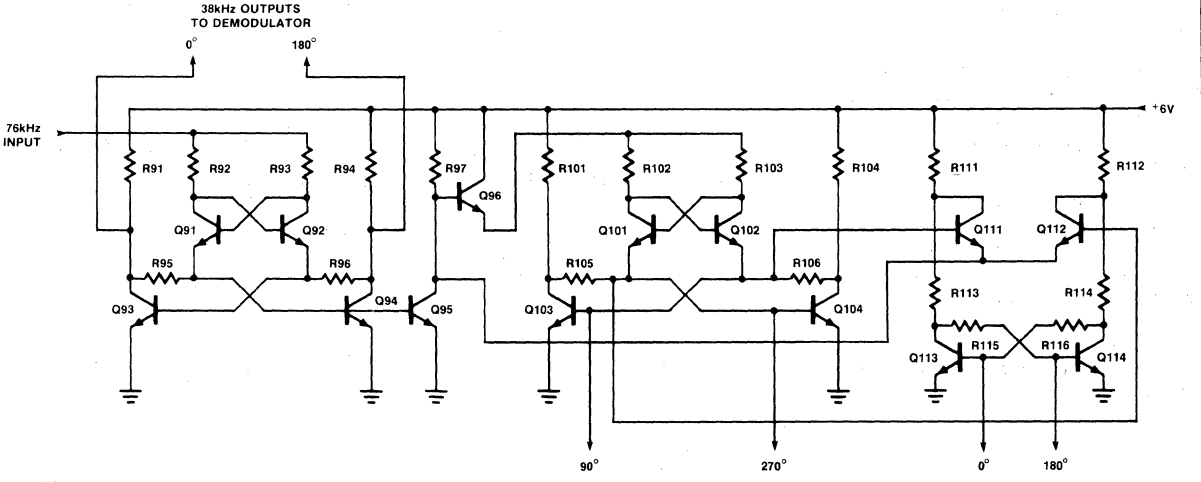
(Equation 8-20)

$$t2 = RC\ 1n\ \frac{V_H}{V_L}$$

where R and C are external components on Lead 15, R81 is on the chip, and V_H and V_L are set voltages which are a fixed percentage of V_S, the internally regulated 6 Volt supply.

Figure 8-33

FREQUENCY DIVIDERS



19kHz outputs to pilot amplitude and phase detectors.

Figure 8-34

The 38kHz In-Phase divider contains a bistable pair, Q113 and Q114, steered by inputs into Q111 and Q112, (a 38kHz input from the collector of Q95, and 19kHz inputs from the bases of Q103 and Q104). If the 19kHz input to the base of Q111 is high when the 76kHz divider turns Q95 ON, Q111 conducts and removes drive to Q114, changing the state of the bistable pair, Q113 and Q114. The bistable remains in this state until the next 38kHz turn on of Q95 which, this time, turns Q112 ON, removes drive to Q113 and resets the bistable pair. The resulting 19kHz output from Q113 and Q114 is at 90 degrees to the Quadrature Divider output with no ambiguity in phasing.

Pilot Phase and Amplitude Detectors

The pilot phase detector and pilot amplitude detector as shown in Figure 8-35 are synchronous, balanced chopper types which develop differential output signals across external filters. Back-to-back NPN transistor pairs are used for each switch to insure minimum drop regardless of signal polarity without reliance on inverse NPN beta characteristics.

The chopper transistors (Q121 through Q124), in the phase detector are driven from the 38kHz Quadrature Divider through transistors Q125 and Q126. The input signal is supplied from lead 12 through resistors R125 and R126. A differential output is developed across the loop filter, comprised of resistors R123 and R124 and the external R-C network between leads 13 and 14.

The pilot amplitude detector (Q131 through Q136), has an identical configuration to the phase detector. Since it operates with drive which is in phase with the pilot signal (90 degrees from the drive to the phase detector), its output is proportional to the amplitude of the pilot component of the multiplex signal. The differential output at leads 9 and 10 is filtered by the external capacitor on these two leads.

A reference 19kHz square wave signal is taken from the collector of drive transistor Q136 through resistor R137 to lead 11. It has the same phasing as the pilot contained in the multiplex input signal.

STEREO PREAMPLIFIERS

Introduction

Stereo preamplifiers have come into greater and greater demand with the increased usage of tape recorders. With stereophonic recording systems, the need increased to have multiple devices in the same package to insure greater thermal tracking and packing density, without sacrificing performance.

PILOT PHASE AND AMPLITUDE DETECTORS

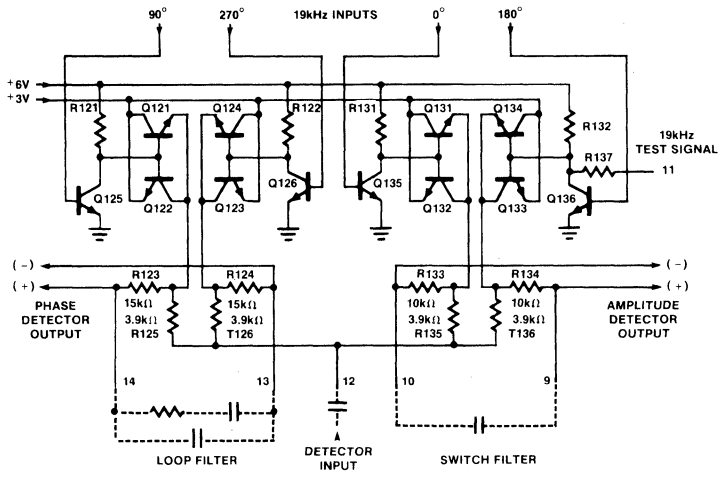
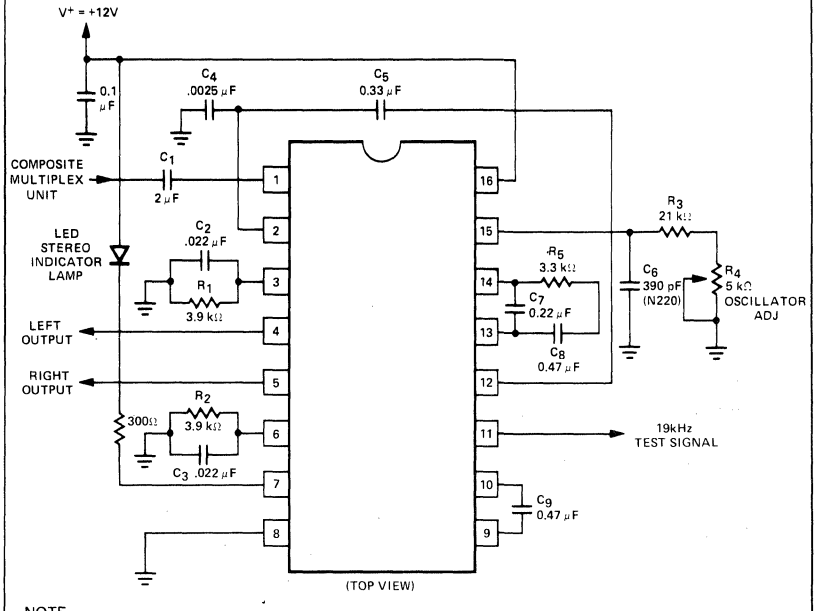


Figure 8-35

TEST CIRCUIT 1 AND TYPICAL APPLICATION

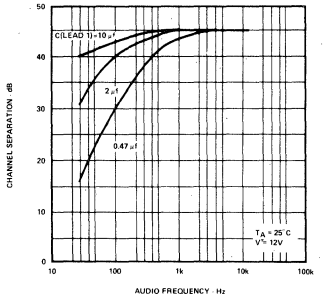


NOTE

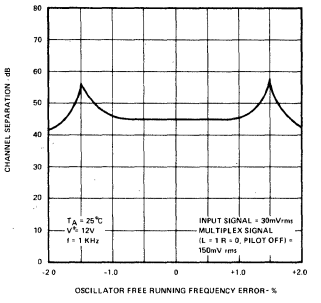
Tolerance on resistors is ±5% and tolerance on capacitors is ±20% unless otherwise specified.
C1 Tolerance = + 100%, −20%
C6 Tolerance = ±1% in test circuit and ±5% in typical application
R3 Tolerance = ±1%
R4 Tolerance = ±10%
R1 and R2 Tolerances = ±1% in test circuit and ±5% in typical application.

TYPICAL PERFORMANCE CURVES FOR 758C
(Test Circuit 1 unless Otherwise Specified)

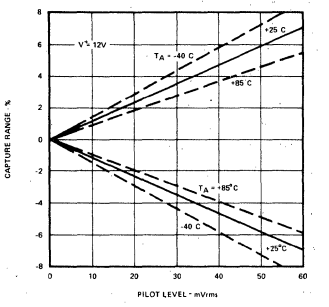
CHANNEL SEPARATION AS A FUNCTION OF AUDIO FREQUENCY



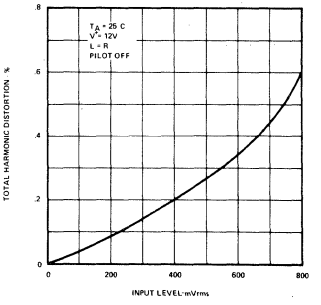
CHANNEL SEPARATION AS A FUNCTION OF OSCILLATOR FREE RUNNING FREQUENCY ERROR



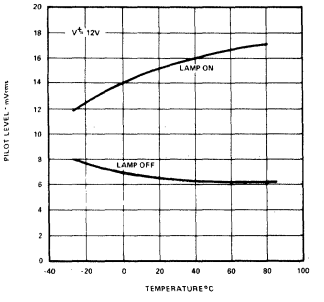
CAPTURE RANGE AS A FUNCTION OF PILOT LEVEL



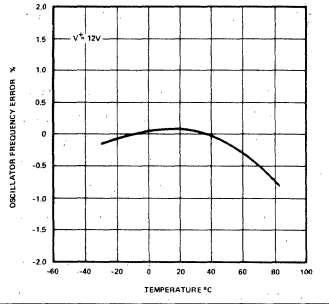
TOTAL HARMONIC DISTORTION AS A FUNCTION OF INPUT LEVEL



LAMP TURN ON AND TURN OFF SENSITIVITY AS A FUNCTION OF AMBIENT TEMPERATURE



OSCILLATOR FREE RUNNING FREQUENCY ERROR AS A FUNCTION OF AMBIENT TEMPERATURE



The NE542, LM381, LM382, LM387 all qualify as low noise dual preamplifiers. The LM381 and LM382 are 14 pin dual in line devices, while the NE542 and LM387 are 8 pin dual in line devices.

All of the above devices have greater than 100dB open loop gain and (15-20) MHz gain bandwidth products. In selecting the proper "low noise" preamplifier several factors must be considered.

I Frequency shaping characteristic required.
II Closed loop response with respect to a system reference level.
III Response of the record/playback head.
IV System distortion requirements.
V Response of the tape used.

The following will deal with items I, II, IV.

When approaching the design criteria of Item 2, the designer should be concerned with the open loop device characteristics. These characteristcs will aid in determining the maximum boost available, knowing that a specific loop gain (open loop gain minus closed loop gain) will be necessary to keep the system distortion low and maintain the output impedance of the "low noise" preamplifier constant over the required operating frequency range.

EQUALIZATION CRITERIA

RIAA Equalization

Recording music in the medium of plastic discs is similar to that of magnetic tape in that neither system exhibits a linear amplitude vs frequency response. Compensation is therefore necessary with records as it was with tape. The standard equalization is known as the RIAA curve and is shown in Figure 8-36, with its corner or turn over frequencies.

Many phono cartridges do not require preamplification. The ceramic and crystal types produce voltage larger than 100mV. Magnetic types, however, produce small voltages in the neighborhood of 5mV and require preamplification.

STANDARD RIAA EQUALIZATION CURVE

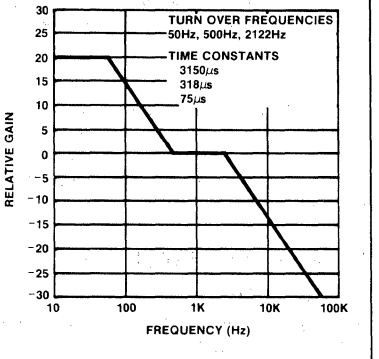


Figure 8-36

RIAA standards call for a maximum recording velocity of 21cm/sec for stereo discs. This worst case velocity describes a bound for the preamplifier gain because the input signal at this velocity is maximum. The maximum undistorted output voltage of the PA239 is 1.25 volts rms. This voltage divided by the output voltage of the cartridge at 21cm/sec velocity defines the highest gain permissible without distortion. This maximum is assumed to be 40dB at 1kHz for the following example. As seen from Figure 8-36, the RIAA curve accounts for 20dB base boost from 50Hz to 500Hz and 20dB of treble out from 2122Hz to 21kHz.

NAB TAPE EQUALIZATION

Recording and playback characteristics of magnetic tape and record/playback heads are not flat but exhibit a loss at high frequencies and a boost at lower frequencies. To obtain an overall flat frequency response and improved signal to noise ratio, the audio signals are equalized by boosting the higher frequencies in amplitude before recording. Playback amplifiers must exhibit bass boost to remove the effects of pre-emphasis for an overall flat response.

Known as the NAB equalization curve, the standard deemphasis employs attenuation from the turnover frequency of 50Hz to the turnover frequency of 3180Hz for 7 1/2 Ips recording. The slower recording speed of 3.75 Ips employs turnover frequencies of 50Hz and 1326Hz. These curves are shown in Figure 8-37. A reference level of 800μV head sensitivity at 1kHz is also used by the NAB.

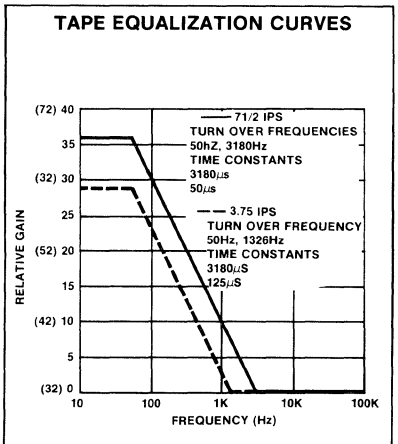


Figure 8-37

STEREO PREAMPLIFICATION

The voltage level appearing at the output of tape playback heads and some phono cartridges are too small to be useful without a large amount of low noise preamplification. In addition to providing low noise amplification, the preamplifier should possess enough open loop gain so that the RIAA and NAB equalization curves can be produced in the feedback networks of the amplifier.

The following paragraphs describe the characteristics and applications of the 542, LM381/382 and the PA239. These devices provide a matched pair of amplifiers which have been specifically designed to minimize amplifier noise and maximize signal to noise ratio.

542 DEVICE DESCRIPTION

The NE542 is a dual low noise amplifier with 104dB open loop gain produced by two stages of voltage gain followed by one stage of current gain.

In the design of low noise devices special attention must be focused on the input stage. If differential topography is used, the stage should be designed so that one of the differential transistors is turned off. This reduces the noise contribution by a factor of 1.4 since only one transistor is producing noise. Current sources and mirrors cannot be used for biasing loads because active elements will contribute more noise.

Implementing these observations, the first gain stage of the 542 is pictured with the complete schematic by Figure 8-38.

Although the differential input configuration degrades the noise performance slightly, using differential inputs has the advantages of higher input impedance, allowing smaller capacitors and larger resistors to be used to achieve the RIAA and NAB curves.

The second stage is a common-emitter amplifier (Q5) with a current source load (Q6). The Darlington emitter-follower Q3-Q4 provides level shifting and current gain to the common-emitter stage (Q5) and the output current sink (Q7). The voltage gain of the second stage is approximately 2000 making the total gain of the amplifier typically 160,000 in the differential input configuration.

The preamplifier is internally compensated with the pole-splitting capacitor, C1. This compensates to unity gain at 15MHz. The compensation is adequate to preserve stability to a closed loop gain of 10.

BIASING

The non-inverting input has been internally biased from a 1.4 Volt internal voltage source. Following the zero differential rule of amplifiers, the output voltage will be set by the resistor feedback network (R4 and R5) of Figure 8-39.

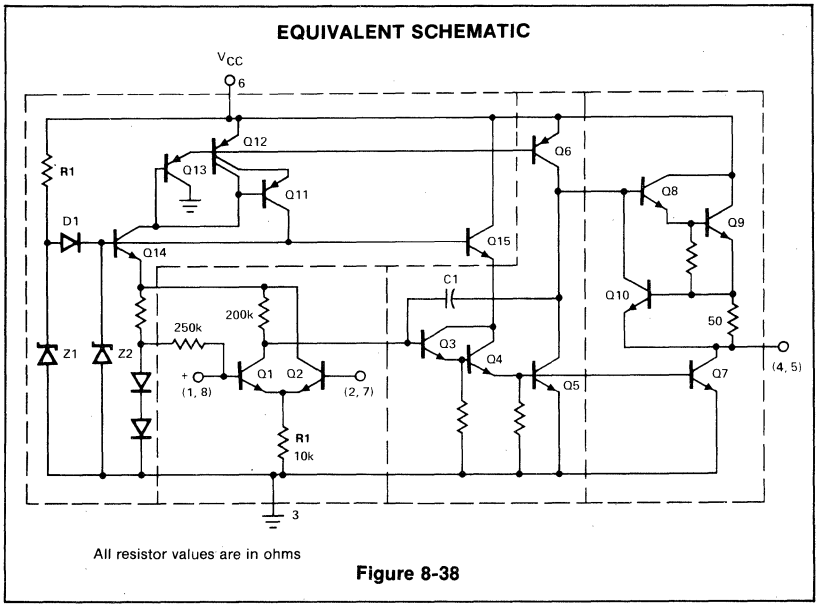
The base of Q2 requires 0.5μA bias current. Hence R5 should pass 5μA minimum for stability, for an output dc voltage of $\frac{V_{CC}}{2}$ the values of R4 and R5 are:

(Equation 8-19)

$$R5 = \frac{2\ V_{BE}}{10\ I_B} = 240K\ \text{Max.}$$

(Equation 8-20)

$$R4 = \left(\frac{V_{CC}}{2.8 - 1}\right) R5$$



All resistor values are in ohms

Figure 8-38

DC amplifier gain is defined by the ratio of R4 and R5. Open loop ac gain can be regained by adding a shunt capacitor across R5. The low frequency 3dB corner is then defined by the capacitor-resistor break point.

LM381/382 Device Description

To achieve low noise performance, special consideration must be taken in the design of the input stage. First, the input should be capable of being operated single ended; since both transistors contribute noise in a differential stage degrading input noise by the factor $\sqrt{2}$.

Secondly, both the load and biasing elements must be resistive; since active components would each contribute as much noise at the input device.

The basic input stage, Figure 8-40, can operate as a differential or single ended amplifier. For optimum noise performance Q2 is turned OFF and feedback is brought to the emitter Q1.

In applications where noise is less critical, Q1 and Q2 can be used in the differential configuration. This has the advantage of higher impedance at the feedback summing point, allowing the use of larger resistors and smaller capacitors in the one control and equalization networks.

The schematic diagram of Figure 8-40 is divided into the first and second voltage gain stages, the current gain stage, and the bias regulator.

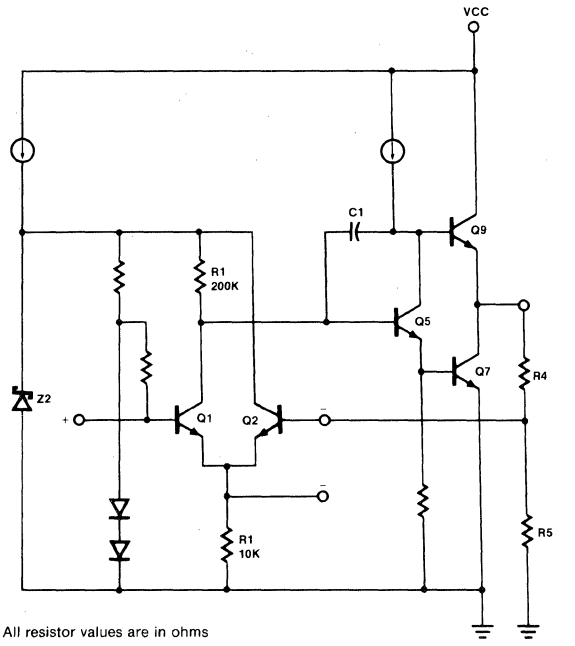
The second stage is a common-emitter amplifier (Q5) with a current source load (Q6). The Darlington emitter-follower Q3-Q4 provides level shifting and current gain to the common-emitter stage (Q5) and the output current sink (Q7). The voltage gain of the second stage is approximately 2000. making the total gain of the amplifier typically 160,000 in the differential input configuration.

The preamplifier is internally compensated with the pole-splitting capacitor, C1. This compensates to unity gain at 15MHz. The compensation is adequate to preserve stability to a closed loop gain of 10. Compensation for unity gain closure may be provided with the addition of an external capacitor in parallel with C1.

Three basic compensation schemes are possible for this amplifier; first stage pole, second stage pole and pole-splitting. First stage compensation will cause an increase in high frequency noise because the first stage gain is reduced, allowing the second stage to contribute noise. Second stage compensation causes poor slew rate (power bandwidth) because the capacitor must swing the full output voltage. Pole-splitting overcomes both these deficiencies and has the advantage that a small monolithic compensation capacitor can be used.

The output stage is a Darlington emitter-follower (Q8, Q9) with an active current sink (Q7). Transistor Q10 provides short-circuit protection by limiting the output to 12mA.

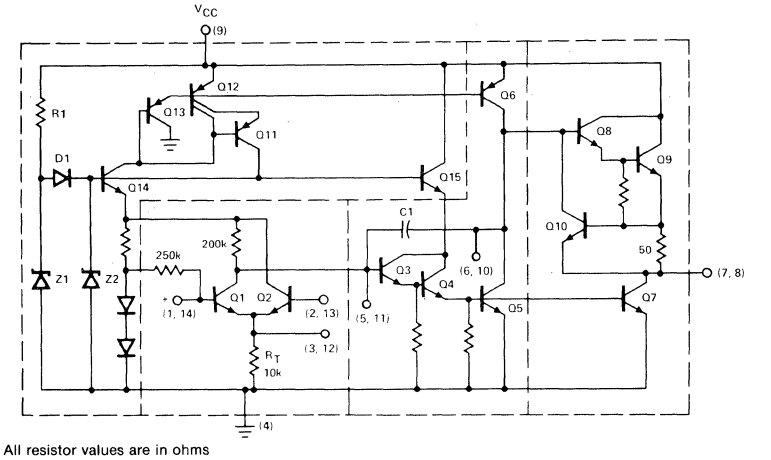
DIFFERENTIAL INPUT BIASING



All resistor values are in ohms

Figure 8-39

LM381 SCHEMATIC DIAGRAM



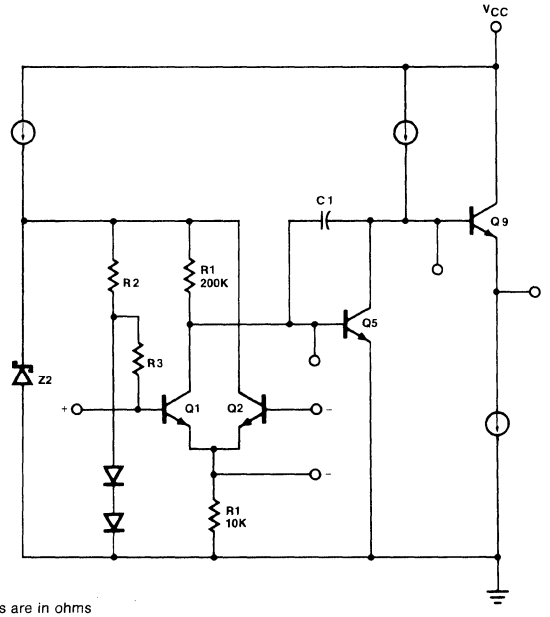
All resistor values are in ohms

Figure 8-40

Biasing

Figure 8-41 shows an ac equivalent circuit of the LM381. The non-inverting input, Q1, is referenced to a voltage source two V_{BE} above ground. The output quiescent point is established by negative dc feedback

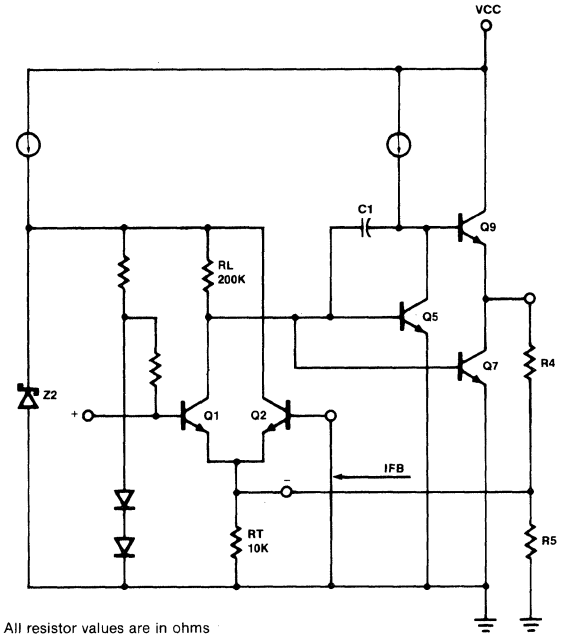
AC EQUIVALENT CIRCUIT



All resistor values are in ohms

Figure 8-41

SINGLE ENDED INPUT BIASING



All resistor values are in ohms

Figure 8-42

through external divider R4/R5 (Figure 8-39).

For bias stability, the current through R5 is made ten times the input current of Q2 (≈0.5μA). Then, for the differential input, resistors R5 and R4 are:

(Equation 8-21)

$$R5 = \frac{2V_{BE}}{10\ I_{Q2}} = \frac{1.2}{5 \times 10^{6}} = 240k\Omega \text{ MAX.}$$

(Equation 8-22)

$$R4 = \left(\frac{V_{CC} - 1}{2.4}\right) R5$$

When using the single ended input, Q2 is turned OFF and dc feedback is brought to the emitter of Q1 (Figure 8-41). The impedance of the feedback summing point is now two orders of the magnitude lower than the base of Q2 (≈ 10kΩ).

Therefore, to preserve bias stability, the impedance of the feedback network must be decreased. In keeping with reasonable resistance values, the impedance of the feedback voltage source can be 1/5 the summing point impedance.

The feedback current is less than 100μA worst case. Therefore, for single ended input, resistors R5 and R4 are:

(Equation 8-23)

$$R5 = \frac{V_{BE}}{5\ I_{FB}} = \frac{0.6}{5 \times 10^{4}} = 1200\Omega\text{MAX.}$$

(Equation 8-24)

$$R4 = \left(\frac{V_{CC} - 1}{1.2}\right) R5$$

The circuits of Figures 8-39 and 8-42 have an ac and dc gain equal to the ratio R4/R5. To open the ac gain, capacitor C2 is used to shunt R5 (Figure 8-43). The ac gain now approaches open loop. The low frequency 3dB corner, f_o, is given by:

(Equation 8-25)

$$f_o = \frac{A_0}{2\pi C2R4} \quad \text{where: } A_0 \text{ open loop gain}$$

LM381 OPEN LOOP CONFIGURATION

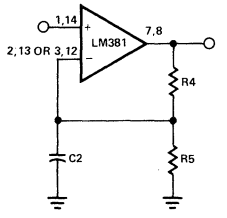


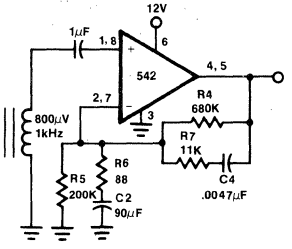
Figure 8-43

NAB Tape Preamplifier

Design of a preamplifier begins by determining the gain and output signal amplitudes in reference to the standard 800μV input signal level. For the following design example, we will use the 542 to achieve a 100mV output level at 1kHz following the 7-1/2 Ips NAB equalization curve. The graph of Figure 8-37 has been calibrated both in absolute gain for this example and relative gain for general use.

From the given parameters, the closed loop gain becomes 32dB at the highest frequency of interest. The NAB response is achieved by adding frequency selective ac feedback as depicted by Figure 8-44. Resistors R4 and R5 select the dc gain as defined by Equations 8-19 and 8-20. Placing a value of 200K upon R5, Equation 8-20 yields a value of 680K ohms.

NAB RESPONSE AMPLIFIER



All resistor values are in ohms

Figure 8-44

The lower corner frequency is determined next by the reactance of C4 and R4 such that:

(Equation 8-26)

$$f_1 = \frac{.159}{C4\ R4}$$

Solving for C4 yields a value of .0047μfd.

The upper corner frequency, f_2, is similarly fixed by the reactance of C4 and R7.

(Equation 8-27)

$$f_2 = \frac{.159}{C4\ R7}$$

Then solving Equation 8-27 for R7 defines a value of 11k ohms.

Midband gain is now fixed by the relationship.

(Equation 8-28)

$$A = \frac{R6 + R7}{R6}$$

Solving for the 1kHz gain of 42dB using 11k for R7 yields a value of 88 ohms for R6. The final calculation of the low frequency cut off of the preamp determines the size of C2.

(Equation 8-29)

$$C2 = \frac{.159}{f_{CUTOFF}\ R6}$$

Typical Applications

In addition to the previous detailed design examples, the following general amplifier configurations (see Figures 8-45 through 8-55) are presented. The choise of design and the device used is a function of the desired complicity and overall performance.

FLAT RESPONSE TAPE AMPLIFIER

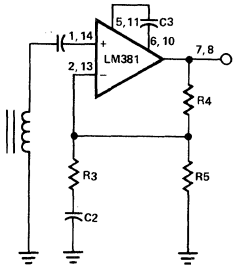


Figure 8-45

TWO-POLE FAST TURN-ON NAB TYPE PREAMP

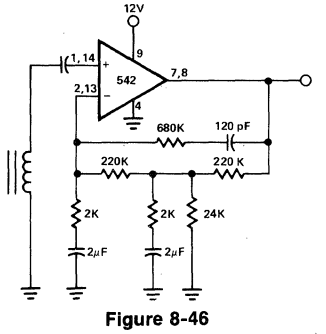
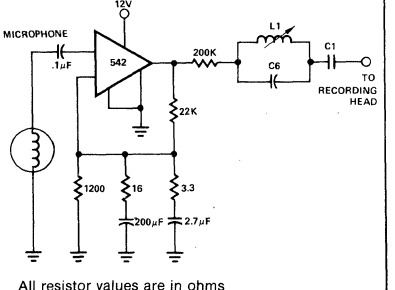


Figure 8-46

TYPICAL NAB RECORD PREAMPLIFIER



All resistor values are in ohms

Figure 8-47

TYPICAL TAPE PLAYBACK AMPLIFIER

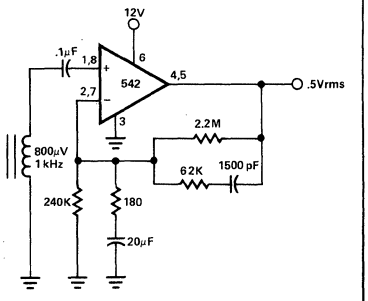
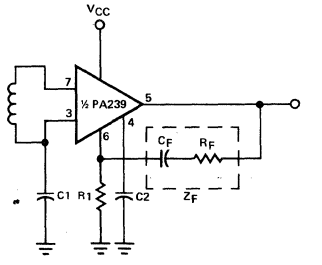


Figure 8-48

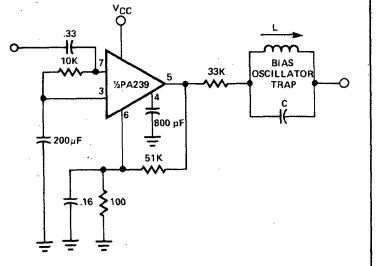
TAPE PREAMPLIFIER



	C2	CF	RF	R1
7-1/2 IPS	750pF	.033	1.5K	22Ω
3-3/4 IPS	750pF	.047	2.4K	33Ω

Figure 8-49

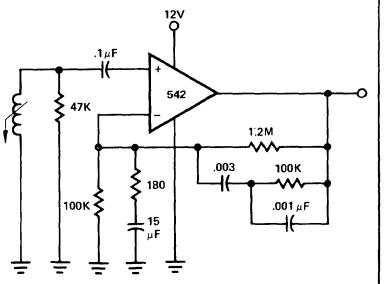
TYPICAL NAB RECORD PREAMPLIFIER



All resistor values in ohms

Figure 8-50

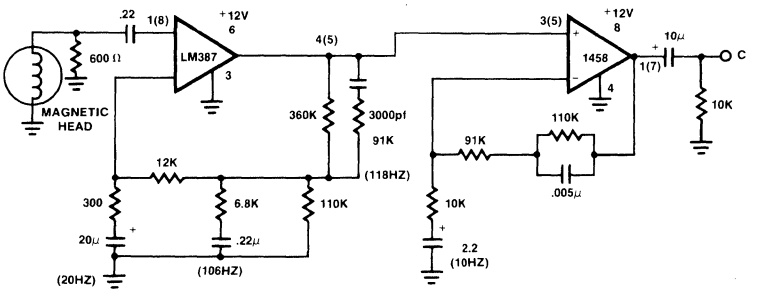
TYPICAL RIAA PREAMPLIFIERS



All resistor values are in ohms

Figure 8-51

CASSETTE PREAMPLIFIER SINGLE CHANNEL



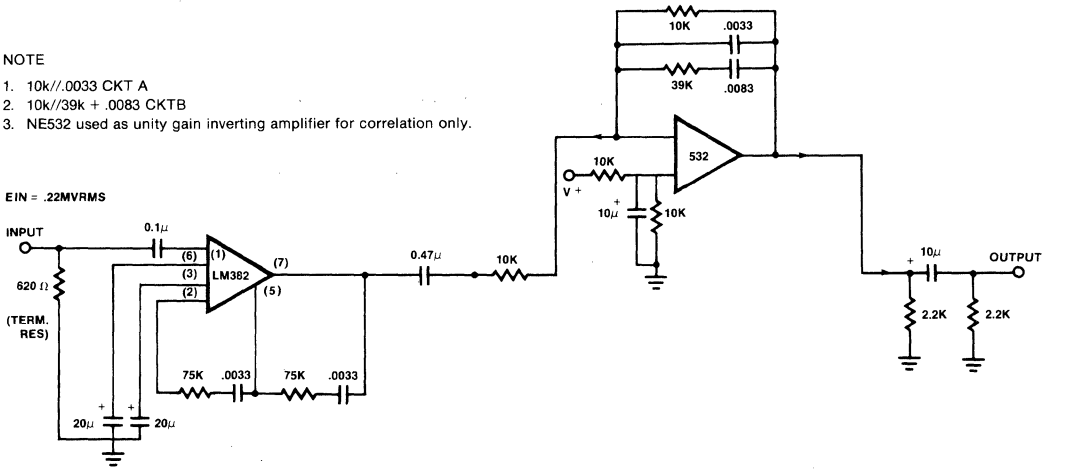
*600Ω resistor used as a terminator when using a voltage generator instead of the magnetic head.

Figure 8-52

CASSETTE PREAMPLIFIER USING LM382 and NE532

NOTE

1. 10k//.0033 CKT A
2. 10k//39k + .0083 CKTB
3. NE532 used as unity gain inverting amplifier for correlation only.



FREQ	GAIN(dB) CKT A	φ (deg) CKT A	GAIN(dB) CKT B	φ (deg) CKT B
20Hz	+68	-15	+68	
40Hz	+76.1	-76	+76	-77
80Hz	+79.4	-135	+79.3	-134
100Hz	+79.8	-147	+79.7	-148
200Hz	+79.7	-187	+79.5	+177
400Hz	+77.6	+157	+76.9	+155
800Hz	+74.6	+144	+73.3	+149
1kHz	+73.9	+144	+72.4	+150
2kHz	+71.8	+134	+70.6	+152
4kHz	+69.2	+110	+69.4	+145
8kHz	+63.9	+76	+67.4	+132
10kHz	+61.5	+65	+66.5	+126
20kHz	+54	-4.0	+62.2	+107

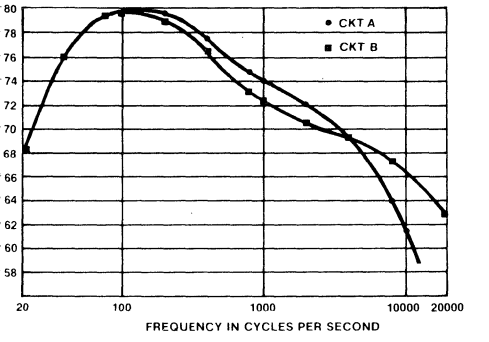
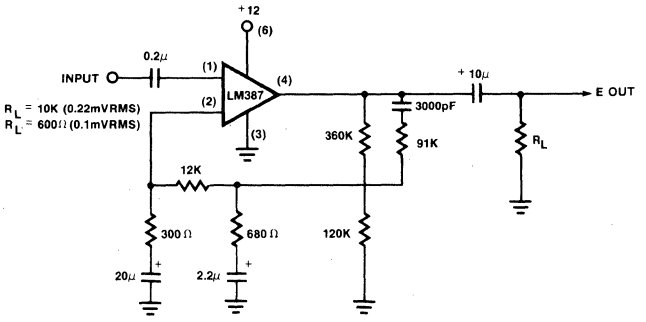


Figure 8-53

CASSETTE PREAMP USING LM387



FREQ	GAIN DB RL = 10K	φ deg	GAIN dB RL = 600	φ deg
20	69		64	
40	76.3		72.4	+115
80	80.4		77.8	+46.3
100	81		78.4	+33
200	80.2		77.8	-0.3
400	77.2		74.9	-18
800	74.8		72.4	-19.8
1kHz	74.2		72.1	-19.3
2kHz	73.3		71.1	-20.4
4kHz	72.3		70	-29.4
8kHz	70.1		68	-44.6
10kHz	69.1		67	-51.1
20kHz	65		62.4	-67.7

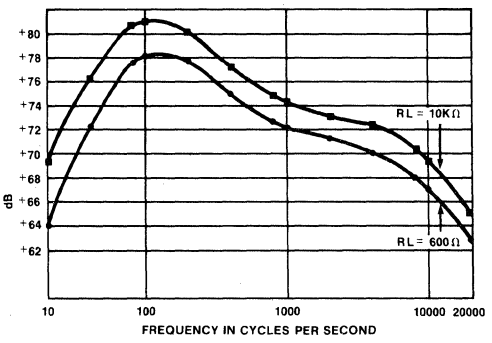
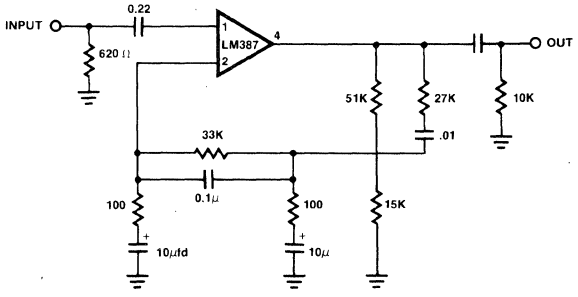


Figure 8-54

CASSETTE PREAMPLIFIER WITH MODIFIED NAB



FREQ	GAIN dB
20	79.8db
40	83
80	82.5
100	82
200	76.5
400	68
800	60
1kHz	57.7
2kHz	51.8
4kHz	48.8
8kHz	47.3
10kHz	47
12kHz	47

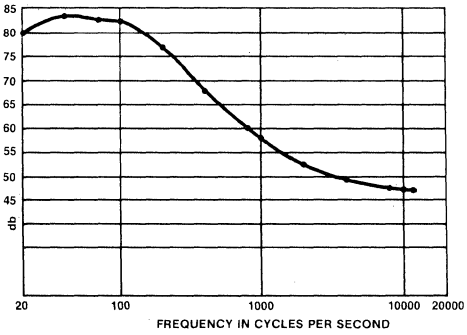


Figure 8-55

CONSTANT FLUX RESPONSE

Equalization criteria discussed earlier has made reference to RIAA Equalization for plastic discs (records) and for NAB Equalization for magnetic tapes. The NAB characterization should be carried further to discuss the Constant Flux Response.

The earlier discussion encompassed the voltage gain (in dB) vs frequency response of NAB amplifiers. In this section we will deal with the Constant Flux Response.

The Constant Flux Response accounts for the frequency characteristics of the record/playback heads of the tape (or cassette) machine employed and the effects of tape speed on Standard NAB Constant Flux Response.

Figure 8-56 indicates the circuitry for using two (2) IC's for a NAB response amplifier. Specific care should be taken to terminate the input *only* when using a voltmeter. When using the magnetic head, the terminating resistor should be removed.

NAB CONSTANT FLUX RESPONSE FOR IDEAL REPRODUCE AMPLIFIER

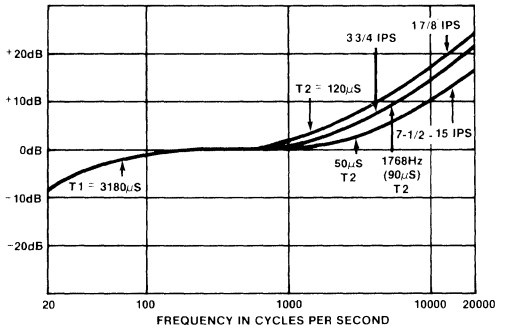


Figure 8-56

Frequency	Response	Frequency	Response
20Hz	-8.6dB	1.5kHz	+0.9dB
25	7.0	2	1.45
30	5.8	2.5	2.1
40	4.1	3	2.75
50	3.0	4	4.1
60	2.3	5	5.4
70	1.8	6	6.6
75	1.6	7	7.7
80	1.4	7.5	8.2
90	1.2	8	8.6
100	1.0	9	9.5
150	0.45	10	10.35
200	0.2	11	11.1
250	0.1	12	11.8
300	-0.1	13	12.5
400	±0	14	13.1
500	+0.1	15	13.6
600	0.1	16	14.2
700	0.2	17	14.7
750	0.2	18	15.2
800	0.2	19	15.6
900	0.3	20	+16.1
1kHz	+0.4dB		

NOTES
Reproducer amplifier output for a constant flux in the core of an ideal reproducing head.
NAB Standard reproducing characteristics for 1 7/8 and 3 3/4 ips tape speeds.

Table 8-2

Frequency	Response	Frequency	Response
20Hz	-8.8dB	1.5kHz	+2.2dB
25	7.2	2	3.4
30	5.9	2.5	4.6
40	4.2	3	5.7
50	3.2	4	7.7
60	2.4	5	9.4
70	1.9	6	10.8
75	1.7	7	12.1
80	1.6	7.5	12.6
90	1.3	8	13.2
100	1.1	9	14.15
150	0.6	10	15.0
200	0.4	11	15.8
250	0.2	12	16.6
300	0.15	13	17.2
400	±0	14	17.9
500	+0.1	15	18.5
600	0.3	16	19.0
700	0.5	17	19.6
750	0.55	18	20.0
800	0.6	19	20.5
900	0.8	20	+21.0
1kHz	+1.0dB		

NOTES
Reproducer amplifier output for a constant flux in the core of an ideal reproducing head.
NAB Standard reproducing characteristic for 7 1/2 and 15-ips tape speeds.

Table 8-3

NAB Standards

According to the NAB Standard, an ideal magnetic reproducing system consists of an ideal reproducing head, lossless magnetic ring, head gaps are short and straight, long wave length flux paths so controlled that no low frequency contours are present and head material losses are negligible. The system employs a reproducing amplifier whose voltage conforms to the frequency response of Fig. 8-55 with a constant flux vs frequency in the head core. Because of several reasons, the flux in the core of an ideal head is not necessarily the same as the surface flux on the tape. Since most of the above effects are not easily measured, the NAB Standard is based on an ideal head-core flux, rather than surface induction.

The voltage vs frequency curve is to be uniform with frequency except where modified by the equalization time constants T1 & T2. The curve expressed in decibels is:

(Equation 8-30)

$$N_{dB} = 20 \log 10\ WT1^{*} \sqrt{\frac{1 + (WT2)^2}{1 + (WT1)^2}}$$

where $W = 2\pi f$, with f in Hz.

T1 & T2 are time constants given below:

Tape Speed	T1	T2
15 ips**	3180μsec	50 - μsec
7.5 ips	3180μsec	50 - μsec
3.75 ips	3180μsec	90 - μsec
1.875 ips	3180μsec	90 - μsec

Head Gap Losses:

The approximate head-gap losses vs frequency may be calculated using the expression:

(Equation 8-31)

$$\text{Gap loss} = -20 \log 10 \frac{\text{Sin } (180^{\circ}\ d/\lambda)}{\pi d/\lambda}$$

where,

d = the null wavelength,
λ = the wavelength of the frequency at which the gap is calculated.

Null wavelength is determined by finding the recorded wavelength at which the reproducing-head output voltage reaches a distinct minimum of at least 20dB below maximum output. This measurement may be made using speeds of one-half and one-quarter the normal speed, using a tuned-voltmeter with no greater than one-third octave bandwidth. To reach a 20-dB null, the head gap edges must be sharp, straight, and parallel.

NOTES

*WT is:
ω = Omega
τ = Tau
** ips = inches per second

CASSETTE PREAMP LM387-1458
CONSTANT FLUX RESPONSE

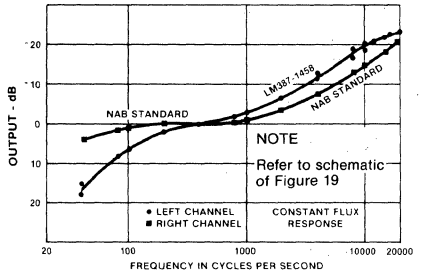
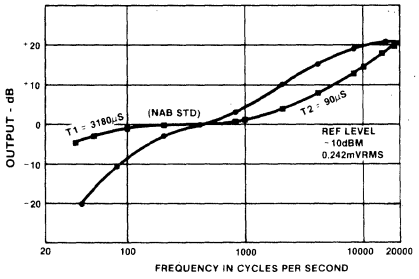


Figure 8-57

TAPE PREAMP LM387
CONSTANT FLUX RESPONSE

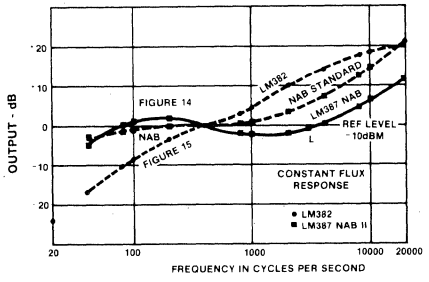


NOTE

Refer to schematic of Figure 13

Figure 8-58

CASSETTE PREAMP LM382 & LM387 (NAB)
CONSTANT FLUX RESPONSE



NOTE

Refer to schematic of Figure 14 & 15

Figure 8-59

CASSETTE PREAMPS COMPARATIVE CONSTANT FLUX RESPONSE

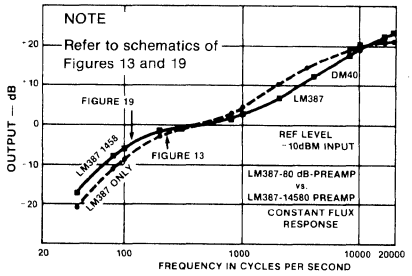


Figure 8-60

FILTER BANDWIDTH			1Vrms		2Vrms		THD + NOISE
			THD				
$f_{(Hz)}$	$f_{L\ (Hz)}$	$f_{H\ (Hz)}$	Left %	Right %	Left %	Right %	No Pre-filter
							Signal 1Vrms
500	400	2500	.28	.28	.29	.27	2.5%
1k	900	4k	.28	.26	.32	.28	2.5%
10k	9900	40k	1.3	1.4	.68	.7	2.4%

Test Conditions: V_{CC} = 12V

ST1700A THD Analyser oscillator signal coupled to reproduce head through constant flux loop. Output signal fed back to ST1700 through Kronhite 3203 filter.

Table 8-4 CASSETTE PREAMP 'THD' MEASUREMENTS WITH REPRO *HEAD*

Freq (Hz)	Output		
	Left dBM	Right dBM	
20		-35	
40	-27.5	-26	
80	-18	-18	
100	-16	-16	
200	-12	-12	
400	-10	-10.5	
800	-8	-8	
1k	-7	-7	"0" dB reference level @ -10dBm
2k	-2.5	-2.2	
4k	+2	+3.2	
8k	+8	+9	
10k	+9.5	+10.8	
12k	+11.2	+11.8	
14k	+12	+12.3	
16k	+12.6	+12.5	
20k	+13	+13	

Test Conditions:

HP651A Test Oscillator 600ohm output coupled through constant flux loop to reproduce head. Output recorded from preamp across 10k load ac. V.M.

Table 8-5 CASSETTE PREAMP CONSTANT FLUX RESPONSE

Freq. Hz	125μVrms (-76dBm) input		245μVrms (-70dBm) input	
	Left %	Right %	Left %	Right %
100	.37	.5	.47	.7
500	.35	.35	.19	.23
1k	.42	.43	.22	.23
5k	.54	.54	.26	.28
10k	.73	.75	.37	.38

Figure 8-63

Test Conditions:

Preamp input terminated in 600Ω. Signal fed from ST1700A Analyser to input.

THD measured at output across 10kΩ load.

Table 8-6 'THD' MEASUREMENT

INTEGRATED CIRCUITS FOR CITIZENS BAND TRANSCEIVERS

Introduction

Recent advancements in integrated circuits have made it possible to greatly simplify the design of citizens band transceivers. A complete multi-channel radio can be built using integrated circuits for all the required functions with the exception of the RF power output stage. A simplified block diagram of such a transceiver is shown in Figure 8-64.

This applications report will further describe a typical version of such a transceiver using several newly developed integrated circuits.

The growing popularity of CB radio is making it necessary to improve the performance characteristics of the CB receiver. The crowded channel and noise problems inherent in this type of communication system demand high performance system design. A dual conversion receiver is desirable to aid in meeting this goal.

RF AMPLIFIER/1ST MIXER

The RF amplifier and 1st mixer used in this radio are implemented using an SD6000. The SD6000 is a dual enhancement mode MOSFET integrated RF amplifier/mixer intended for use up to 150MHz. The advantages of using MOSFETs in receiver "front end" designs have been realized for several years by manufacturers of FM and television tuners. Using a linear device such as a MOSFET, it is possible to achieve improvements in cross-modulation, intermodulation distortion and in general a much wider dynamic range than possible using conventional bipolar transistors.

INTEGRATED CIRCUIT CITIZENS BAND TRANSCEIVER

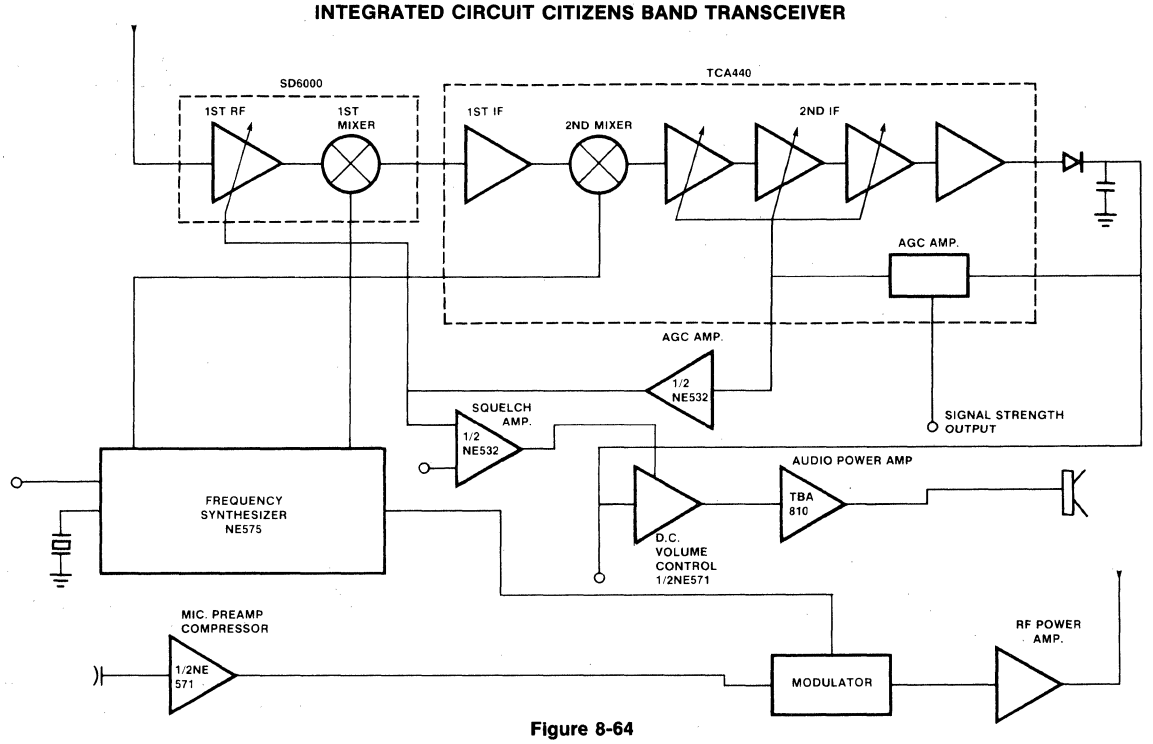


Figure 8-64

The SD6000 is ideally suited for this application for several reasons. The RF section is essentially a low noise, high gain dual gate MOSFET. The relatively high input impedance of this device makes it convenient to use high Q tuned circuits which reduce the possibility of out of band spurious responses. The AGC range of the RF amplifier is greater than 50dB at 27MHz and because of the low parasitic capacitances associated with this device there is no skewing of the center frequency of the tuned circuits as a function of AGC voltages. The RF amplifier input circuit can be roughly approximated as shown below in Figure 8-65.

RF AMPLIFIER INPUT CIRCUIT

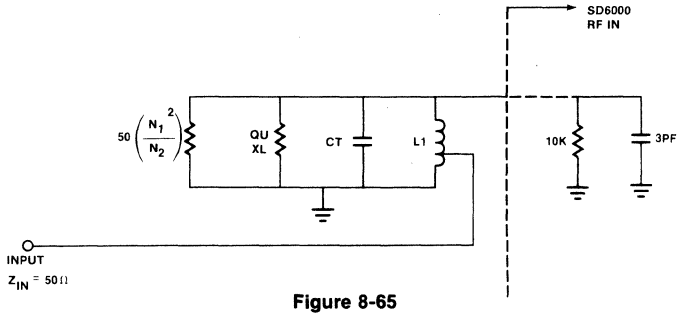


Figure 8-65

L1 consists of 24 turns of #32 wire tapped 4 turns from the ground side on a Micro-Metals T44-10 core. This gives an inductance of 1.6μh (X_C = 270Ω @ 27MHz) and an unloaded Q of 150.

The input circuit can be further simplified as shown in Figure 8-66.

INPUT CIRCUIT SIMPLIFIED

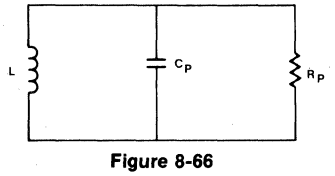


Figure 8-66

C_P is made up of the D-MOS input, and a fixed parallel capacitor. The required C_P is given by

$$C_P = \frac{1}{w^2 L}$$

C_P at 27MHz is therefore equal to 22pf. A portion of C_P is made tunable in this design. This would not be necessary in a design using a slug tuned inductor. It should be noted that the position of the tap is such that the reflected antenna impedance does not match the RF amplifier input impedance. This was done intentionally to improve the large signal (2Vrms) handling capability of this receiver. The MOS front end has sufficient gain to compensate for this loss.

The bandwidth of the RF input circuit can be found knowing the total parallel resistance (R_P) and parallel capacitance

$$BW_{-3dB} = \frac{1}{2\pi RC}$$

At 27MHz the RF input bandwidth is approximately 4MHz. In a more optimum design this could be made narrower by tapping the input coil closer to ground.

The design of the RF output circuit is very similar to that of the input. The only difference is a different value of fixed capacitance to take into account the RF amplifier output and mixer input capacitance.

Dual gate Signetics D-MOS transistors are exceptionally stable RF devices because of their low feedback capacitance (typically .02pf). This makes it possible to achieve high gain without the need for neutralization. Low feedback is also the reason for a wide dynamic AGC range.

The second dual gate MOSFET is the SD6000 which is designed for mixer applications. It is a relatively large geometry device with a wide square law region. This design overcomes the bias problems inherent in most MOSFETs when used as mixers. In other MOSFETs biasing in the square law region is only possible over a narrow range of drain current. In the SD6000 mixer the conversion gain is essentially constant from 5 to 10mA drain current thus simplifying the bias circuit design.

The 1st oscillator is injected into gate 2 and the RF signal into gate 1. Injecting the oscillator into gate 2 provides the highest isolation between the oscillator and RF input. This isolation is important to prevent radiation of the oscillator signal through the receiver antenna.

The mixer is biased to operate in the most linear portion of the forward transconductance curves. Figures 8-67 and 8-68 show the transconductance curves for the SD6000 are linear in a relatively wide operating region. Non-linearities in these curves indicate that third order (and higher) terms would be present if the device was biased in these regions. These higher order terms contribute only to undesired responses. As the transconductance curves become linear, the higher order terms disappear and conversion gain increases. Figure 8-67 shows that the gate 1 transconductance curves is almost a straight line for gate 2 bias voltage between 2.0 and 6.0 volts. Figure 8-68 shows a linear region for gate 2 transconductance with gate 1 bias from 2.5 to 3.5 volts.

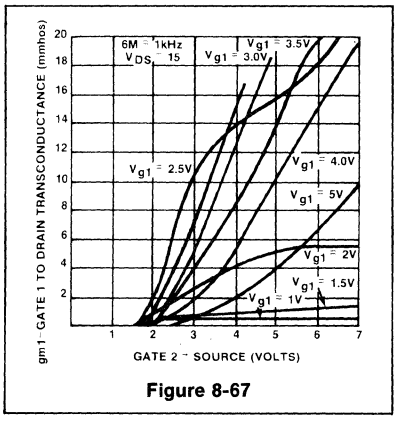


Figure 8-67

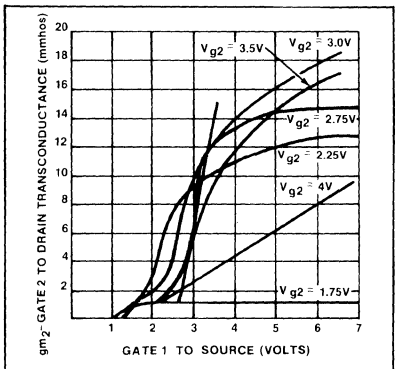


Figure 8-68

By definition the transconductance, gm is the partial derivative of drain current, i_d, with respect to the input voltage e_s. The total drain current of the mixer can be expressed by

$$i_d = gm1\ V_{g1} + gm2\ V_{g2}$$

where gm1 = transconductance gate 1 to drain.
gm2 = tranconductance gate 2 to drain.

From Figure 8-67 the gate 1 tranconductance, gm1 can be expressed as:

$$gm1 = -17.6 + 8.2\ (V_{g2} + V_{g2})\ \text{(mmhos)}$$

for V_{g2} = 2V to 6V

From Figure 8-68 we get the following expression for gm2

$$gm2 = -23.7 + 10.2\ (V_{g1} + V_{g1})\ \text{(mmhos)}$$

for V_{g1} = 2.5V to 3.5V

If the dc bias points are chosen, for example V_{g1} = 3.5 and V_{g2} = 3.5, the following expressions are derived from gm1 and gm2 using the previous equations

$$gm1 = 11.1 + 8.2\ V_{g2}\ \text{(mmhos)}$$

$$gm2 = 8.9 + 10.2\ V_{g1}\ \text{(mmhos)}$$

Substituting these equations into the expression for the total drain current, i_d, we get

$$i_d = 11.1\ V_{g1} + 8.9\ V_{g2} + 18.4\ V_{g1}\ V_{g2}$$

The last term in this equation is the one that will contain the IF frequency we desire. If we let V_{g1} and V_{g2} equal a sinusoidal voltage, V_{g1} is the input signal voltage and V_{g2} is the local oscillator, we obtain

$$V_{g1} = E_s \sin \omega_{LO} + \omega_s t$$

$$V_{g2} = E_{LO} \sin \omega_{LO} t$$

Substituting V_{g1} and V_{g2} into the equation for i_d gives

$$i_d = 18.4\ E_S\ E_{LO}\ 1/2 \cos (\omega_{LO} + \omega_s)t + 1/2 \cos (\omega_{LO} - \omega_s)t$$

The $(\omega_{LO} - \omega_s)$ term is the 10.7MHz IF we want. Dividing both sides of the equation by E_s we obtain

$$\frac{i_d}{E_s} = gm_c = 9.2\ E_{LO}\ \text{(peak)}$$

$$= 13\ E_{LO}\ \text{(rms) mmhos}$$

This exercise shows that relatively high conversion gains can be achieved using the SD6000. It can be seen that the conversion transconductance will also be a function of the local oscillator level.

In actual practice, good performance can be achieved with both gates biased at the same dc voltage. The bias voltage is chosen to give a drain current of 5 to 10mA.

For bias stability, some form of dc feedback should be incorporated to reduce the drain current variations that would occur in production where variations in the device threshold voltages will be encountered. In the SD6000, the mixer and RF amplifier substrates and RF amplifier source are connected internally so precautions must be taken to assure that the RF amplifier source voltage is less than or equal to the mixer source voltage. In this design the RF amplifier source is grounded so it can never be positive with respect to the mixer source. Figure 8-69 shows a simplified bias circuit of the RF amplifier.

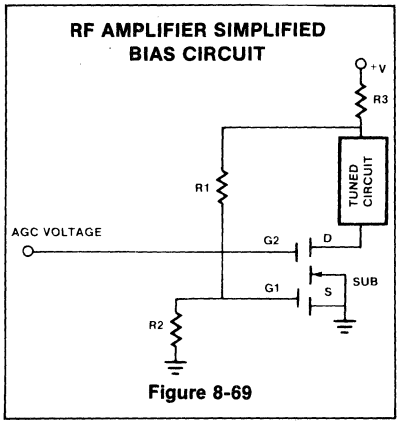


Figure 8-69

This bias circuit provides dc feedback without using a source resistor. R3 is made large enough so that there is a significant voltage drop across it with normal operating drain current (10-15mA). This voltage drop means a lower drain to source voltage (V_{DS}). A lower V_{DS} does not affect the RF amplifier gain since the transconductance is constant with V_{DS} from 5 to 20 volts. If variations in threshold voltage were to cause a higher drain current, the voltage drop across R3 would increase thereby decreasing the gate 1 voltage derived from R1 and R2. This decreased gate 1 voltage tends to decrease

the drain current and will result in a stable operating point.

The mixer is biased using the same technique with the addition of a bypassed source resistor to provide even greater stability.

The mixer output is coupled through a 10.7MHz IF transformer to a 10.7MHz crystal filter. The output of the filter is terminated with a 2.2k resistor in parallel with the TCA440 input (2K/5pf).

1st IF/2nd Mixer/2n IF

A block diagram of the TCA440 is shown in Figure 8-70.

This integrated circuit is intended for AM receivers up to 50MHz. It has several features making it well suited for citizens band receiver applications. The RF stage (in this case the 1st IF) is a differential amplifier with an AGC control range of approximately 38dB. Its output is internally coupled to a mulitplicative push-pull mixer (balanced). This mixer produces few harmonics and provides suppression of the RF and oscillator frequencies. The internal oscillator frequency is fixed at 10.245MHz by a parallel resonant crystal. This gives a mixer output frequency of 455kHz for the 2nd IF.

The mixer output is filtered by a single tuned IF transformer, ceramic filter, and a second single tuned transformer and applied to the 4 stage 2nd IF amplifier in the TCA440. This 2nd IF has an AGC control range of 62dB. The two independent AGC control loops in the TCA440 provide a very wide operating dynamic range (100dB). Although a 455kHz 2nd IF frequency is used in this design, the TCA440 IF stages will operate from 0 to 2MHz.

Audio Processing

The circuit shown in Figure 8-71 shows how the NE571 may be used as a dc volume control. The frequency response of the circuit is approximately 300Hz to 3kHz and the dynamic control range is greater than 60dB. Figure 8-72 shows the dc control voltage vs gain.

The output of the NE571 dc volume control drives a TBA810S audio power amplifier. The TBA 810 provides a 6 watt (@ 14.4V 4Ω) output with low harmonic and cross-over distortion. In addition, the circuit has a thermal limiting circuit which simplifies the heat sink design.

Frequency Synthesizer

The purpose of the frequency synthesizer is to provide the necessary signals to drive the receiver's first mixer, second mixer, and transmitter power amplifier. In a 40 channel, dual conversion CB transceiver, it is necessary to generate 81 discrete frequencies. By using phase locked loop frequency synthesis, this can be accomplished using only one crystal.

The SM5104/5/7/9 is a "first generation" C-MOS integrated circuit synthesizer. A block diagram of the SM5104 is shown in Figure 8-73.

This circuit operates from a single power supply using low power CMOS technology. It contains a reference oscillator, a 2^8 or 2^9 divider chain, a binary input programmable divider, and phase detector circuits.

There are several ways this circuit can be used in the transceivers. The methods described here will be limited to dual conversion systems using 10.695MHz 1st IF and 455kHz 2nd IF. These frequencies were

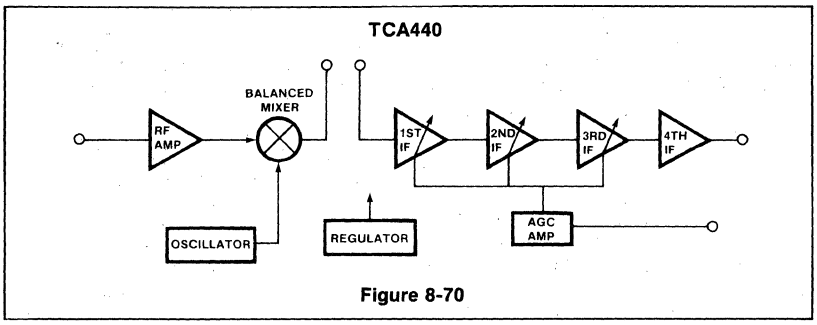


Figure 8-70

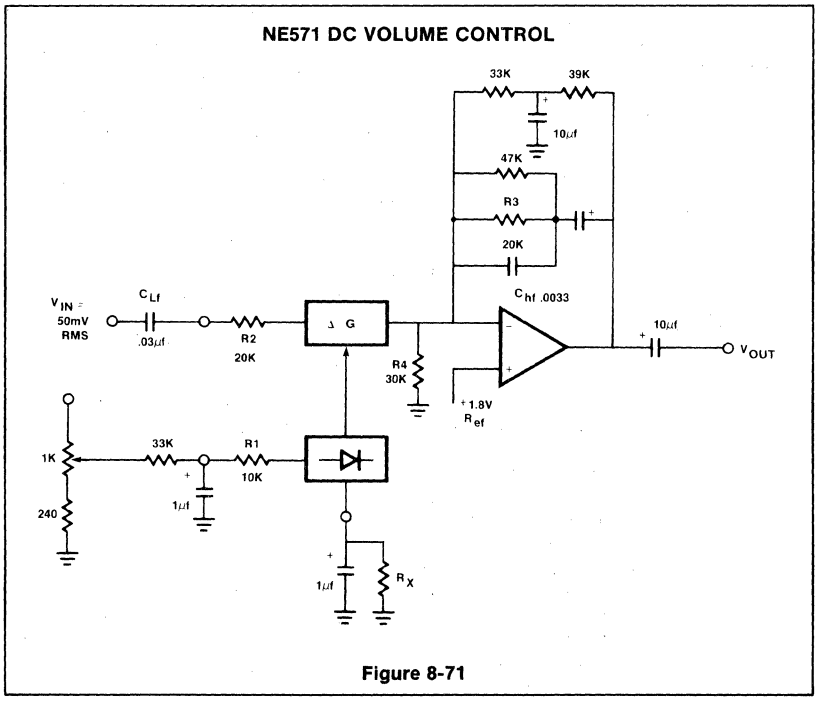


Figure 8-71

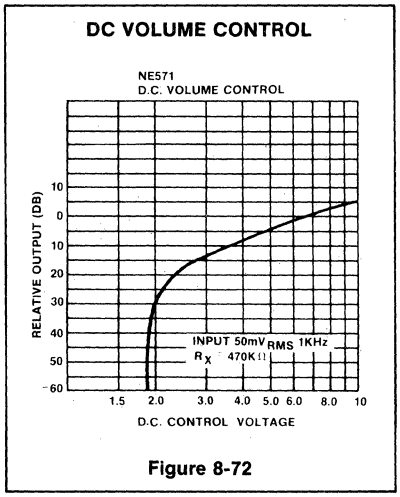


Figure 8-72

chosen because low cost filters are readily available. A simplified block diagram of a CB transceiver is shown in Figure 8-74.

The basic frequency synthesizer using a PLL is shown in Figure 8-74.

In this circuit, the output frequency is an integer multiple of the reference frequency. ($f_{out} = N f_{ref}$). This is the simplest form the loop can assume but in most cases, not the most practical. The major problem with this type of PLL is that the programmable counters must operate at the output frequency (in the CB case, up to 27MHz). There are several commonly used methods to lower the frequency into the programmable counter.

Frequency synthesis by prescaling is shown in Figure 8-76.

In this system, the frequency into the programmable counter is lowered by a factor of P. The disadvantage of this system is that the reference frequency must also be prescaled by the factor P. This lowers the "effective" reference frequency and slows the loop response.

Frequency synthesis by 2 modulus prescaling solves the problem of high programmable divider frequency and slow loop response but requires more complex logic in addition to a high frequency 2 modulus divider. The cost of this system is slightly greater than that of Figure 8-76 but the performance is equal to that of Figure 8-75. A block diagram of this system is shown in Figure 8-77.

The most common synthesizer configuration used in CB transceivers is prescaling by mixing down. This method is shown below in Figure 8-78.

This system offers the optimum performance but requires a second stable frequency source for mixing down. This system can be easily implemented using the SM5104. The system block diagram is shown in Figure 8-79.

This is a practical circuit configuration but has several minor disadvantages. The major problems are that it requires four external active tuned circuits, the x3 multiplier, offset mixer, transmit offset oscillator and mixer. It also requires the use of 2 crystals. Despite these drawbacks, this general configuration is widely used in currently available CB transceivers.

With the introduction of "second generation" synthesizers such as the NE575, many of the previously described shortcomings are resolved. The NE575 will generate the required frequencies for a dual or single conversion CB transceiver using only one crystal. Figure 8-80 shows the functional block diagram of the NE575.

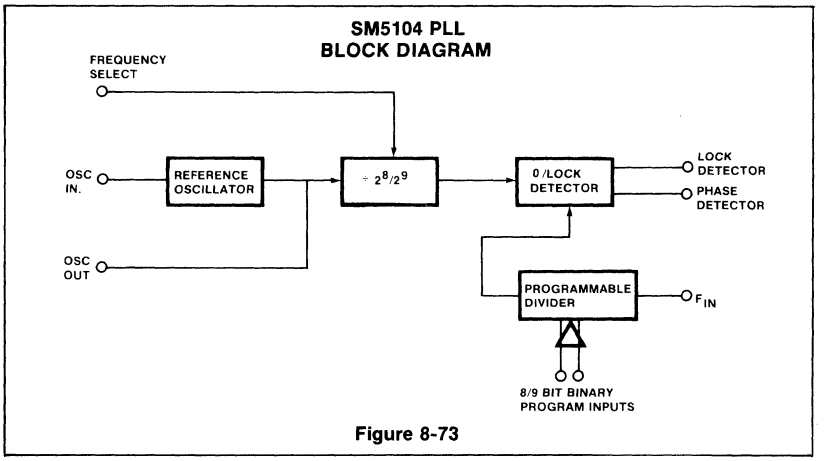


Figure 8-73

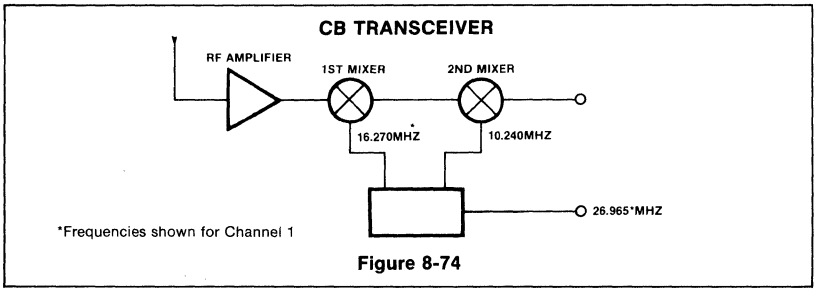


Figure 8-74

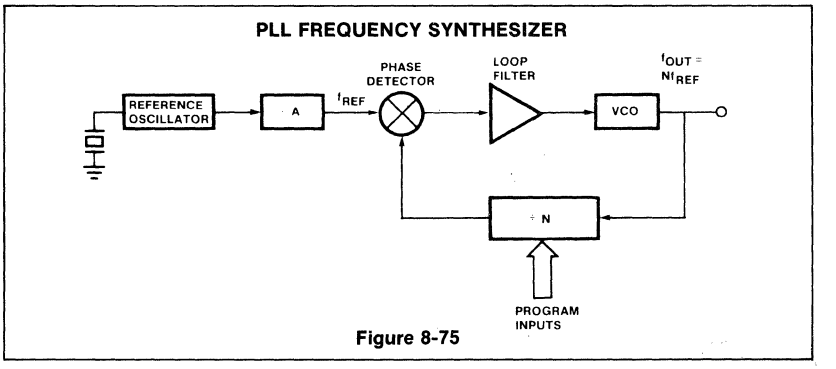


Figure 8-75

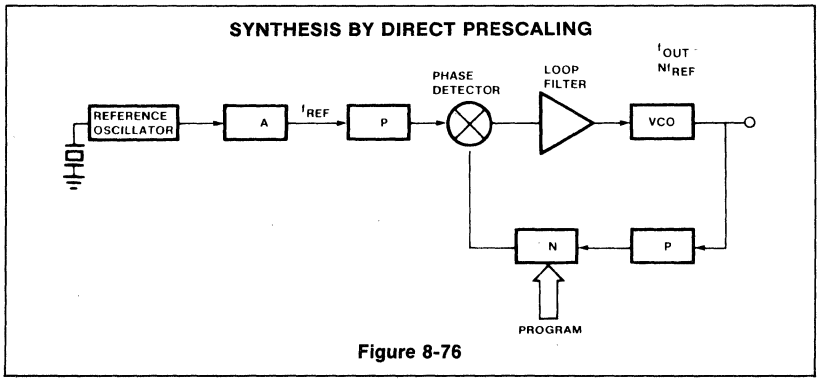


Figure 8-76

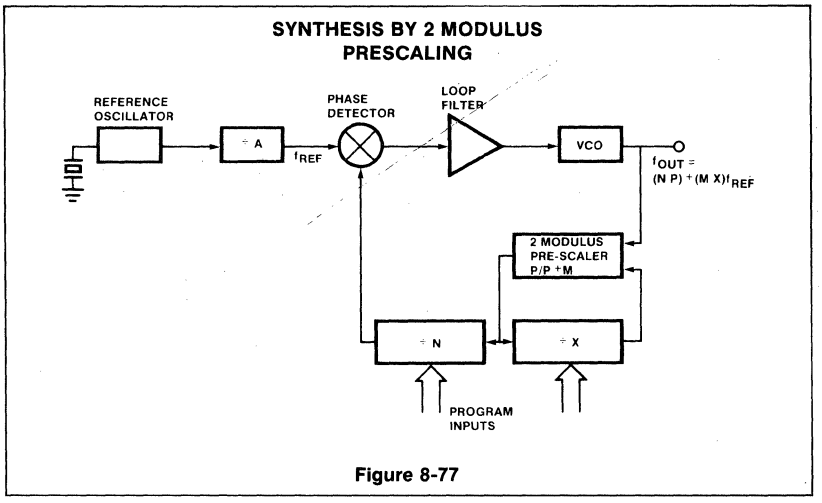


Figure 8-77

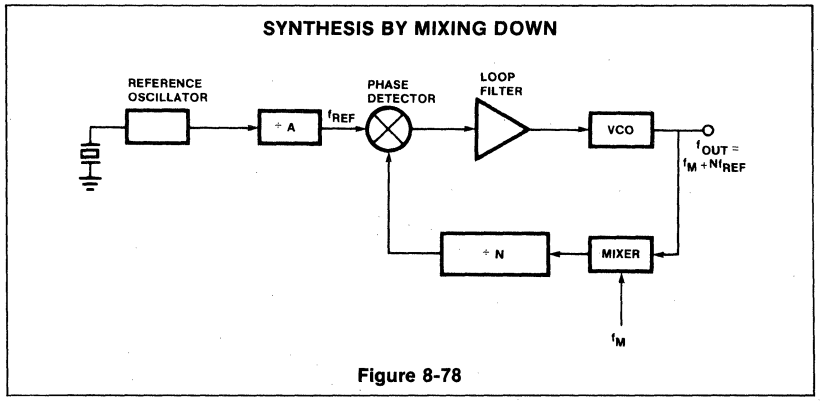


Figure 8-78

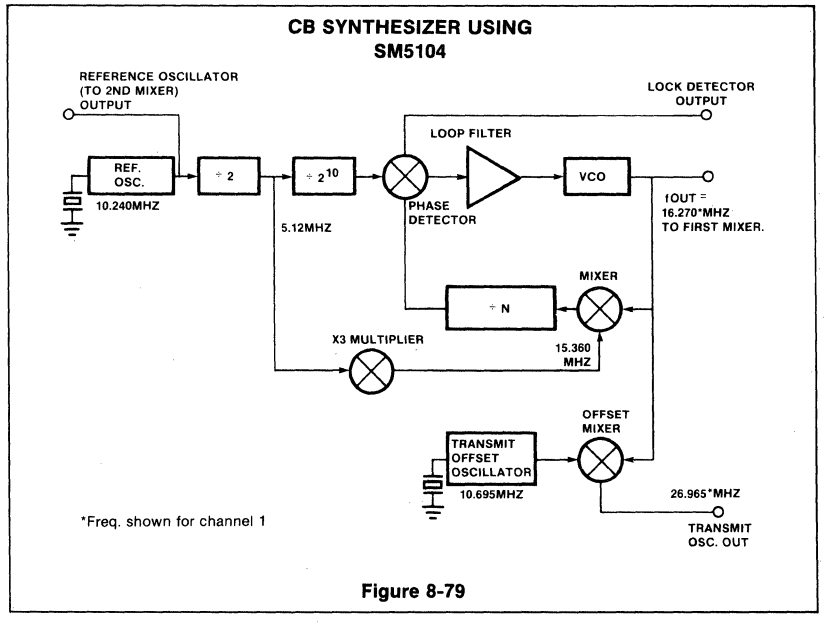


Figure 8-79

Audio Compressor

The purpose of the transmit audio compressor is to amplify the signal from the microphone to the level required to drive the modulator. It also provides an automatic level control (ALC) circuit. The ALC circuit has a transfer function which makes its output voltage constant with a wide range of input levels. It is generally desirable to have an audio compressor which provides an output level which drives the modulator to close to 100% modulation with very low input levels and does not exceed 100% with large inputs.

There are two major overmodulation problems that show up in many CB transceivers currently available. One is the audio compressor's ability to handle a wide dynamic range of microphone input levels. The current popularity of "power mics" makes it necessary for the compressor to limit the modulation index to less than 100% with very large inputs. The second overmodulation problem that may arise relates to the audio compressor's attach time. Active compressor circuits take a finite time to respond to a sudden change in input level.

The NE571 provides an economical solution to the above mentioned problems. Figure 8-81 shows how this ALC circuit may be implemented.

The gain of this circuit is

$$K = \frac{R1\ R2\ I_B}{2R3\ V_{IN}\ (AVG)} \text{ where } I3 = 140\mu A$$

and $\frac{V_{IN}}{V_{IN}\ (AVG)} = \frac{\pi}{2\sqrt{2}}$ for sinc waves

R_X is included to limit the maximum gain of the compressor. This is to prevent high modulation levels at very low input levels (such as background noise). The maximum gain

$$K_{max} = \frac{\frac{R1 + R_X}{1.8} \times R2 \times I_B}{2R3}$$

The output voltage may be set to the desired level

$$V_{out} = \frac{R1\ R2\ I_B}{2R3} \frac{V_{IN}}{V_{IN}\ (AVG)}$$

The other important design equations for this circuit are:

I ALC time constant (τ = R1 x C_{Rect})

II Distortion = $\frac{.1\mu f}{C_{Rect}} \times \frac{1KHz}{freq} \times 2\%$

III $V_{out}\ (dc) = \left[1 + \frac{R_{dc1} + R_{dc2}}{R4}\right] 1.8V$

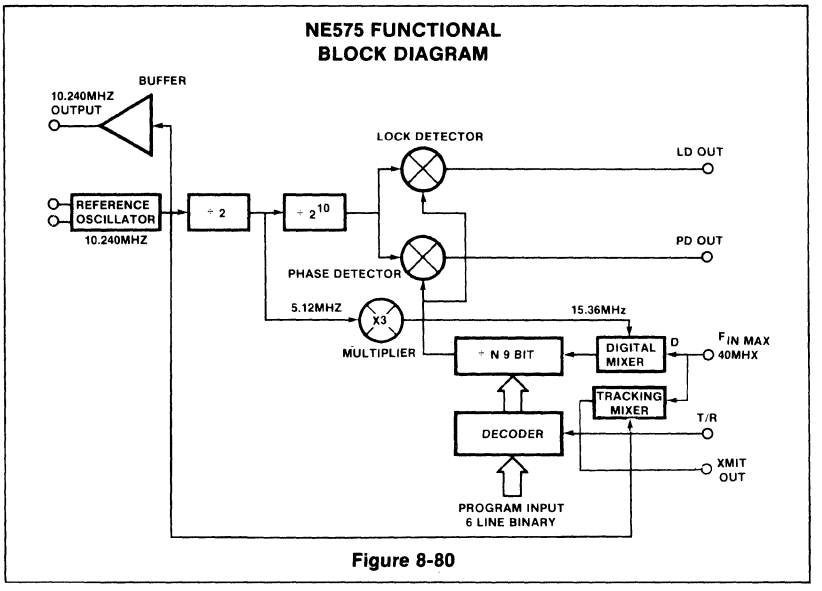


Figure 8-80

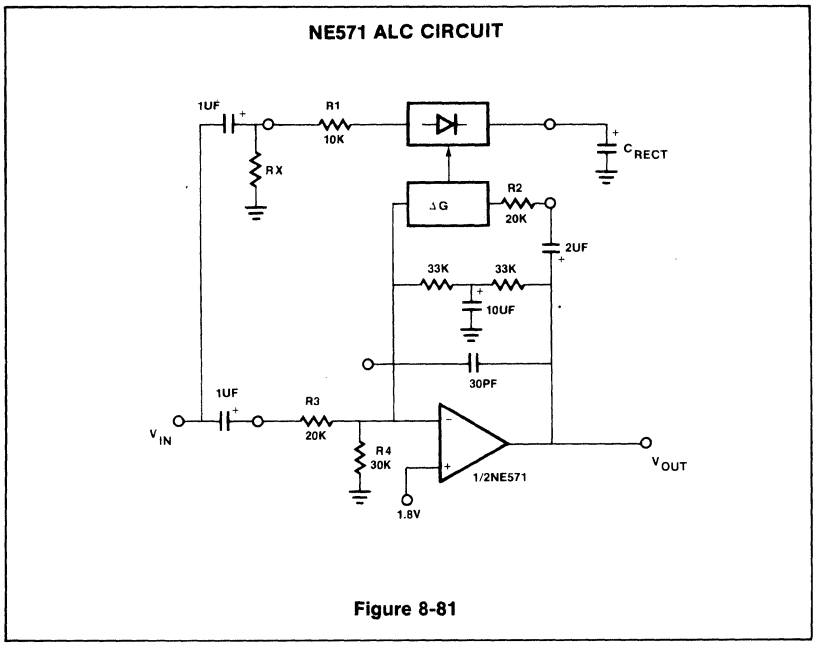


Figure 8-81

Transmit RF

Development work is currently taking place to try and solve some of the typical problems encountered in the RF section of CB transceivers. The major emphasis is towards reducing the cost of the output circuitry (elimination of the modulation transformer) and reduce spurious outputs.

The transmit oscillator signal, generated by the PLL, will drive a low level FET modulator. The modulator output then drives a linear RF power amplifier. The RF power amplifier will be implemented using a power D-MOS FET. The advantages of a MOSFET power amplifier are high transconductance, no thermal run-away, no second breakdown, and reduction in harmonic output.

Detailed information on this section of the CB transceiver will be made available as soon as the development work is completed.

CITIZENS' BAND RECEIVER
TCA440/SD6000

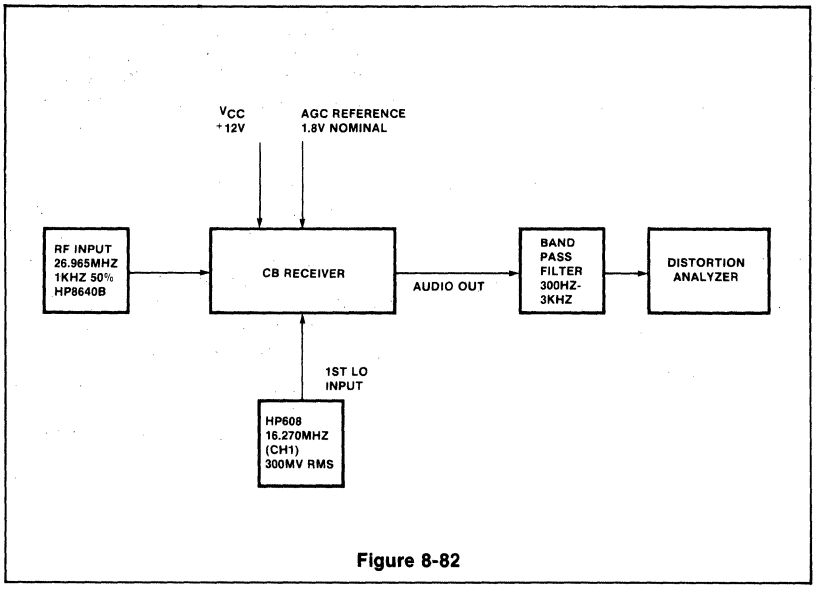


Figure 8-82

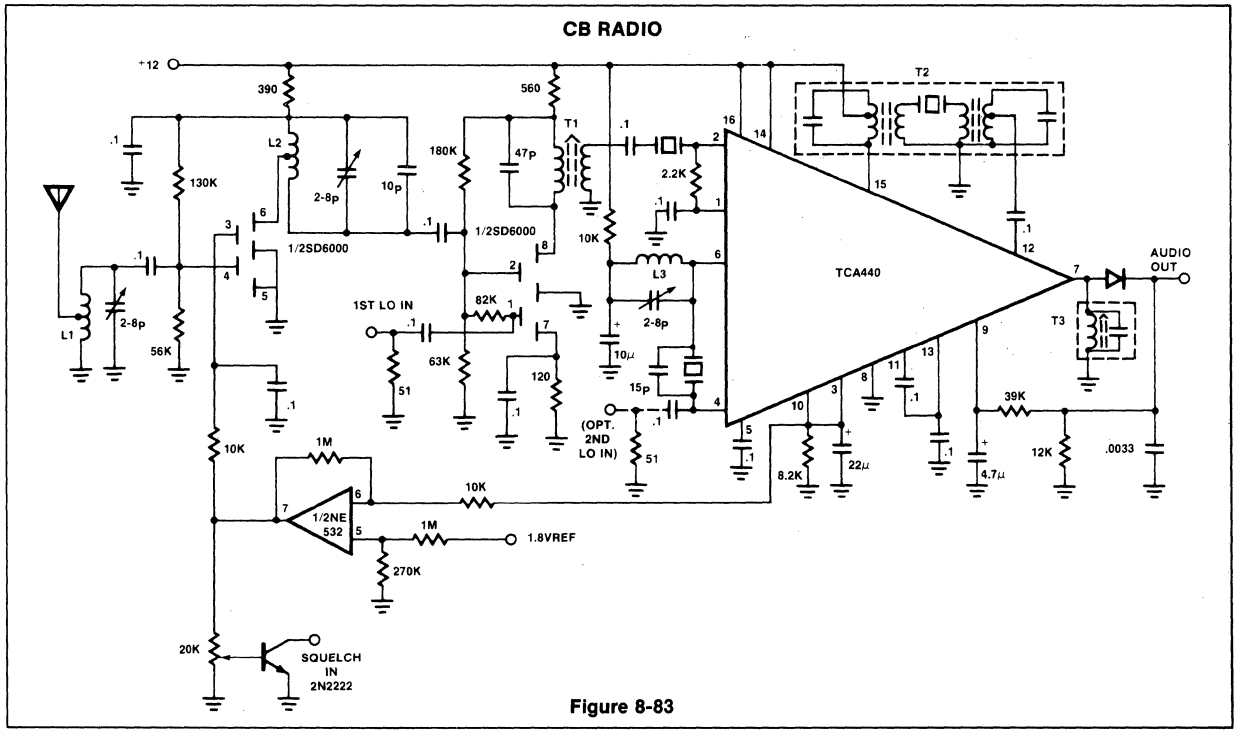


Figure 8-83

RF INPUT vs S + N, THD, AUDIO
CB RECEIVER TCA440/SD600
RF INPUT 26.965MHz 1KHz 50%MOD

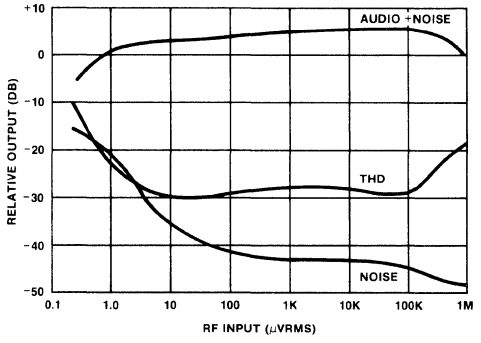


Figure 8-84

AGC vs RF INPUT
CB RECEIVER TCA440/SD600
RF INPUT 26.965MHz 1KHz 50%MOD

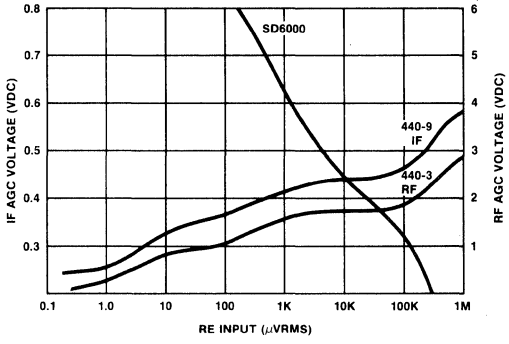
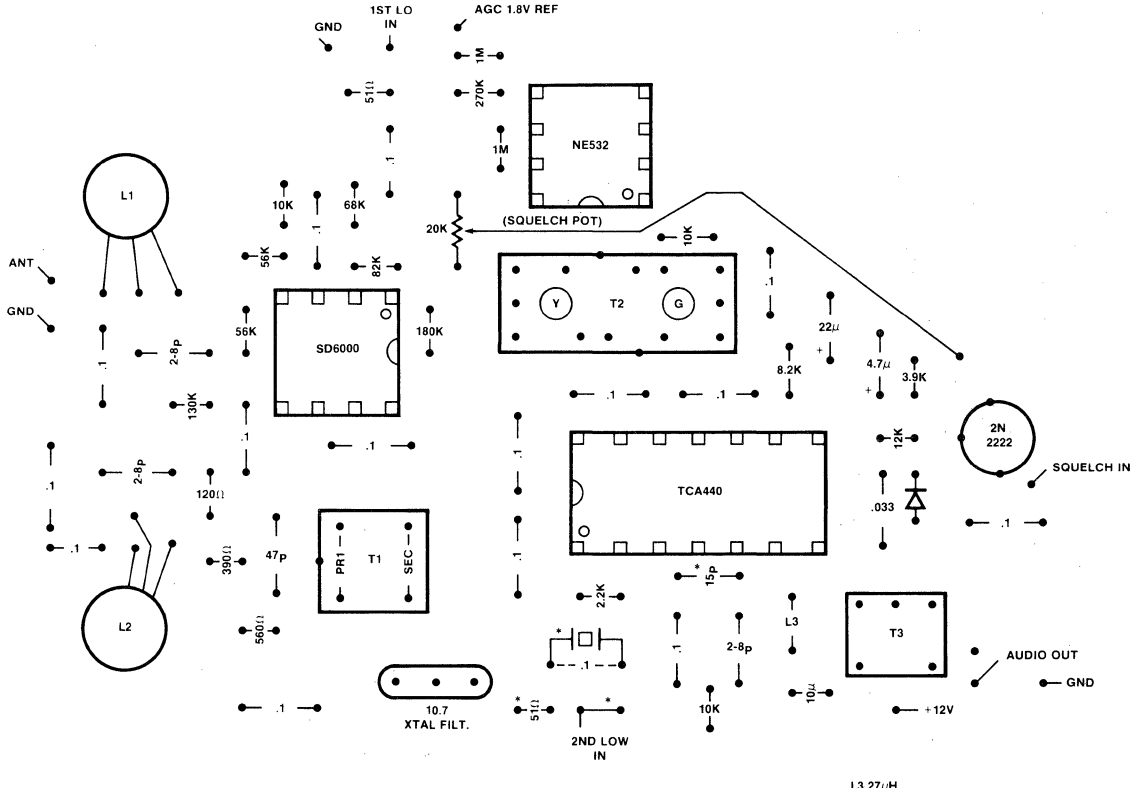


Figure 8-85

CB RADIO



L1 24T #26 on T44-10 core, tap 3T from GND
L2 24T #26 on T44-10 core, tap 6T from +V
T1 533-3652-03 Camrion, green core
PR1 30T #26, sec 8T #26
T2 Toko CFT 006H 455kHz
T3 Toko A2549

*15p, XTAL, & jumper wire with 51Ω omitted makes optional built in OSC. (See schematic)

Figure 8-86

INTRODUCTION

Much interest has been expressed in high performance electronic gain control circuits. For non-critical applications, an integrated circuit operational transconductance amplifier can be used, but when high performance is required, one has to resort to complex discrete circuitry with many expensive, well matched components. This paper describes a new integrated circuit, the NE570 Compandor, which offers a pair of high performance gain control circuits featuring low distortion (<.1%), high signal to noise ratio (90dB), and wide dynamic range (110dB).

CIRCUIT BACKGROUND

The NE570 Compandor was specifically designed to satisfy the requirements of the telephone system. When several telephone channels are multiplexed onto a common line, the resulting signal to noise ratio is poor and companding is used to allow a wider dynamic range to be passed through the channel. Figure 8-89 graphically shows what a compandor can do for the signal to noise ratio of a restricted dynamic range channel. The input level range of +20 to -80dB is shown undergoing a 2 to 1 compression where a 2dB input level change is compressed into a 1dB output level change by the compressor. The original 100dB of dynamic range is thus compressed to a 50dB range for transmission through a restricted dynamic range channel. A complementary expansion on the receiving end restores the original signal levels and reduces the channel noise by as much as 45dB.

The significant circuits in a compressor or expandor are the rectifier and the gain control element. The phone system requires a simple full wave averaging rectifier with good accuracy, since the rectifier accuracy determines the (input) output level tracking accuracy. The gain cell determines the distortion and noise characteristics, and the phone system specifications here are very loose. These specs could have been met with a simple operational transconductance multiplier, or OTA, but the gain of an OTA is proportional to temperature and this is very undesirable. Therefore, a linearized transconductance multiplier was designed which is insensitive to temperature and offers low noise and low distortion performance. It is hoped that these features will make the circuit as widely used in audio systems as it will be in telecommunications systems.

BASIC CIRCUIT HOOKUP AND OPERATION

Figure 8-90 shows the block diagram of one half of the chip (there are two identical channels on the I.C.). The full wave averaging rectifier provides a gain control current, I_G, for the variable gain (ΔG) cell. The output of the ΔG cell is a current which is fed to the summing node of the operational amplifier. Resistors are provided to establish circuit gain and set the output dc bias.

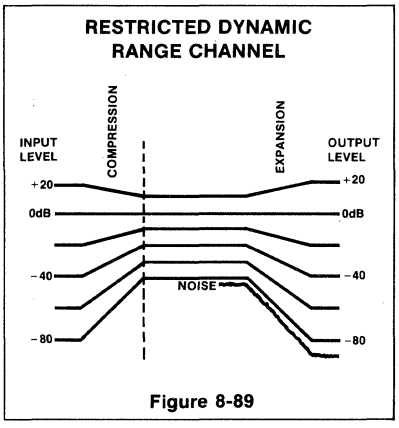


Figure 8-89

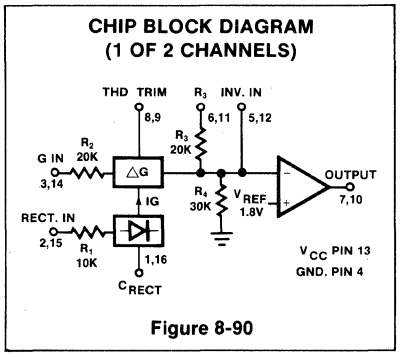


Figure 8-90

The circuit is intended for use in single power supply systems, so the internal summing nodes must be biased at some voltage above ground. An internal band gap voltage reference provides a very stable, low noise 1.8 volt reference denoted V_{ref}. The non-inverting input of the op amp is tied to V_{ref}, and the summing nodes of the rectifier and ΔG cell (located, at the right, of R_1 and R_2) have the same potential. The THD trim pin is also at the V_{ref} potential.

Figure 8-91 shows how the circuit is hooked up to realize an expandor. The input signal, V_{in}, is applied to the inputs of both the rectifier and the ΔG cell. When the input signal drops by 6dB, the gain control current will drop by a factor of 2, and so the gain will drop 6dB. The output level at V_{out} will thus drop 12dB, giving us the desired 2 to 1 expansion.

Figure 8-92 shows the hookup for a compressor. This is essentially an expandor placed in the feedback loop of the op amp. The ΔG cell is set up to provide ac feedback only, so a separate dc feedback loop is provided by the two R_{dc} and C_{dc}. The values of R_{dc} will determine the dc bias at the output of the op amp. The output will bias to:

$$V_{out}\,dc = 1 + \frac{R_{dc1}+R_{dc2}}{R_4} V_{ref} = \left(1 + \frac{R_{dc\ tot}}{30K}\right) 1.8V$$

The output of the expandor will bias up to:

$$V_{out}\,dc = 1 + \frac{R_3}{R_4} V_{ref} = \left(1 + \frac{20K}{30K}\right) 1.8V = 3.0V$$

The output will bias to 3.0V when the internal resistors are used. External resistors may be placed in series with R_3, (which will affect the gain), or in parallel with R_4 to raise the dc bias to any desired value.

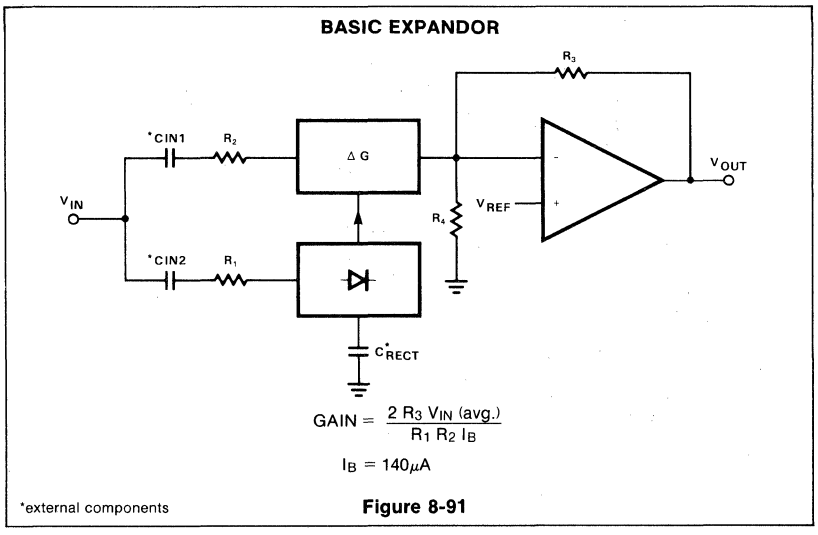
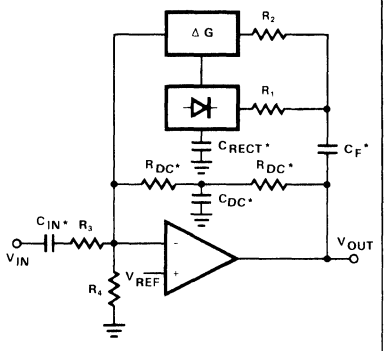


Figure 8-91

BASIC COMPRESSOR



$$GAIN = \left(\frac{R_1 R_2 I_B}{2 R_3 V_{IN\ (avg.)}}\right)^{1/2}$$

$I_B = 140\mu A$

*external components

Figure 8-92

CIRCUIT DETAILS-RECTIFIER

Figure 8-93 shows the concept behind the full wave averaging rectifier. The input current to the summing node of the op amp, V_{in}/R_1, is supplied by the output of the op amp. If we can mirror the op amp output current into a unipolar current, we will have an ideal rectifier. The output current is averaged by R_5, Cr, which set the averaging time constant, and then mirrored with a gain of 2 to become I_G, the gain control current.

RECTIFIER CONCEPT

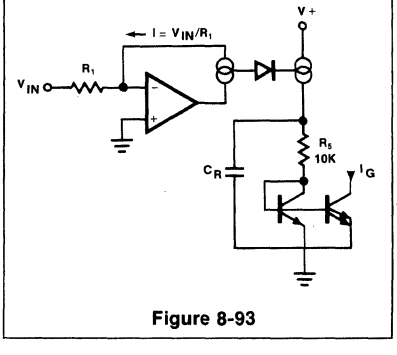
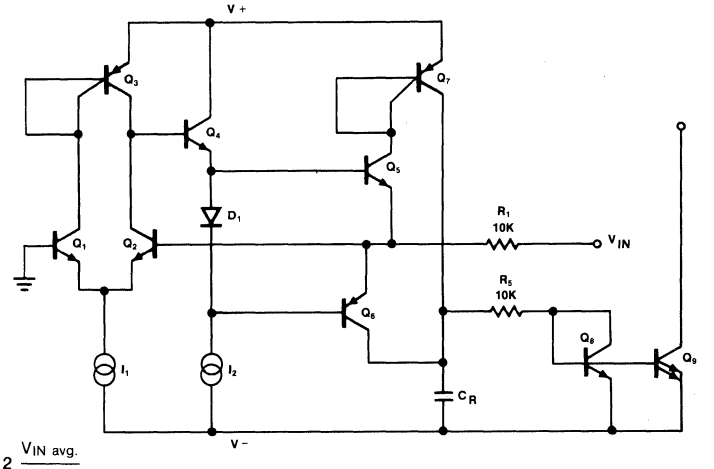


Figure 8-93

Figure 8-94 shows the rectifier circuit in more detail. The op amp is a one stage op amp, biased so that only one output device is on at a time. The non-inverting input, (the base of Q_1), which is shown grounded, is actually tied to the internal 1.8V V_{ref}. The inverting input is tied to the op amp output, (the emitters of Q_5 and Q_6), and the input summing resistor R_1. The single diode between the bases of Q_5 and Q_6 assures that only one device is on at a time. To detect the output current of the op amp, we simply use the collector currents of the output devices Q_5 and Q_6. Q_6 will conduct when the input swings positive and Q_5 conducts when the input swings negative. The collector currents will be in error by the α of Q_5 or Q_6 on negative or positive signal swings, respectively. IC's such as this have typical npn β's of 200 and pnp β's of 40. The α's of .995 and .975 will produce errors of .5% on negative swings and 2.5% on positive swings. The 1.5% average of these errors yields a mere -13dB gain error.

SIMPLIFIED RECTIFIER SCHEMATIC



$I_G = 2\ \frac{V_{IN\ avg.}}{R1}$

Figure 8-94

At very low input signal levels the bias current of Q_2, (typically 50nA), will become significant as it must be supplied by Q_5. Another low level error can be caused by dc coupling into the rectifier. If an offset voltage exists between the V_{in} input pin and the base of Q_2, an error current of V_{os}/R_1 will be generated. A mere 1mv of offset will cause an input current of 100nA which will produce twice the error of the input bias current. For highest accuracy, the rectifier should be coupled into capacitively. At high input levels the β of the pnp Q_6 will begin to suffer, and there will be an increasing error until the circuit saturates. Saturation can be avoided by limiting the current into the rectifier input to 250μA. If necessary, an external resistor may be placed in series with R_1 to limit the current to this value. Figure 8-95 shows the rectifier accuracy vs input level at a frequency of 1kHz.

At very high frequencies, the response of the rectifier will fall off. The rolloff will be more pronounced at lower input levels due to the increasing amount of gain required to switch between Q_5 or Q_6 conducting. The rectifier frequency response for input levels of 0dBm, -20dBm, and -40dBm is shown in Figure 8-96 The response at all three levels is flat to well above the audio range.

RECTIFIER ACCURACY

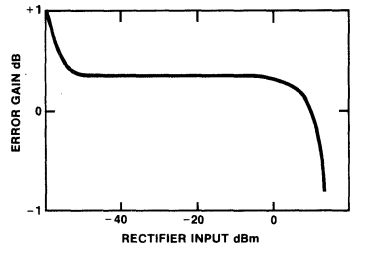


Figure 8-95

RECTIFIER FREQUENCY RESPONSE vs INPUT LEVEL

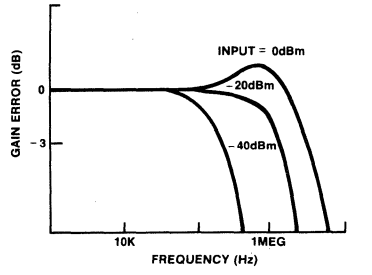


Figure 8-96

VARIABLE GAIN CELL

Figure 8-97 is a diagram of the variable gain cell. This is a linearized two quadrant transconductance multiplier[1,2]. Q_1, Q_2 and the op amp provide a predistorted drive signal for the gain control pair, Q_3, Q_4. The gain is controlled by I_G and a current mirror provides the output current.

The op amp maintains the base and collector of Q_1 at ground potential (V_{ref}) by controlling the base of Q_2. The input current I_{in} (= V_{in}/R_2) is thus forced to flow through Q_1 along with the current I_1, so $I_{C1} = I_1 + I_{in}$. Since I_2 has been set at twice the value of I_1, the current through Q_2 is $I_2-(I_1+I_{in}) = I_1-I_{in} = I_{C2}$. The op amp has thus forced a linear current swing between Q_1 and Q_2, by providing the proper drive to the base of Q_2. This drive signal will be linear for small signals, but very non-linear for large signals, since it is compensating for the non-linearity of the differential pair Q_1, Q_2 under large signal conditions.

The key to the circuit is that this same predistorted drive signal is applied to the gain control pair Q_3 and Q_4. When two differential pairs of transistors have the same signal applied, their collector current ratios will be identical, regardless of the magnitude of the currents. This gives us:

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{C4}}{I_{C3}} = \frac{I_1+I_{in}}{I_1-I_{in}}$$

plus the relationships $I_G = I_{C3} = I_{C4}$ and $I_{out} = I_{C4}-I_{C3}$ will yield the multiplier transfer function,

$$I_{out} = \frac{I_G}{I_1} I_{in} = \frac{V_{in}}{R_2} \frac{I_G}{I_1}$$

this equation is linear and temperature insensitive, but it assumes ideal transistors.

If the transistors are not perfectly matched, a parabolic, non-linearity is generated, which results in 2nd harmonic distortion. Figure 8-98 gives an indication of the magnitude of the distortion caused by a given input level and offset voltage. The distortion is linearly proportional to the magnitude of the offset and the input level. Saturation of the gain cell occurs at a +8dBm level. At a nominal operating level of 0dBm, a 1mv offset will yield .34% of second harmonic distortion. Most circuits are somewhat better than this, which means our overall offsets are typically about 1/2mv. The distortion is not affected by the magnitude of the gain control current, and it does not increase as the gain is changed. This second harmonic distortion could be eliminated by making perfect transistors, but since that would be difficult, we have had to resort to other methods. A trim pin has been provided to allow trimming of the internal offsets to zero, which effectively eliminated second harmonic distortion. Figure 8-99 shows the simple trim network required.

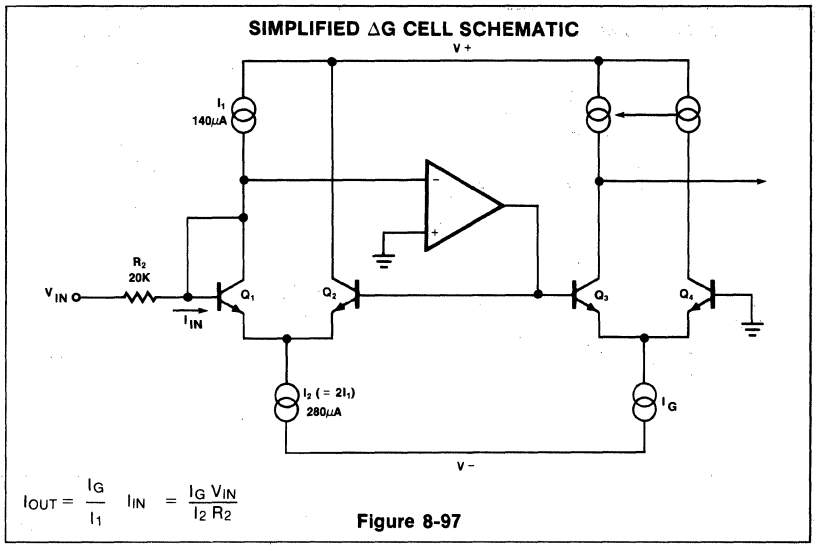


Figure 8-97

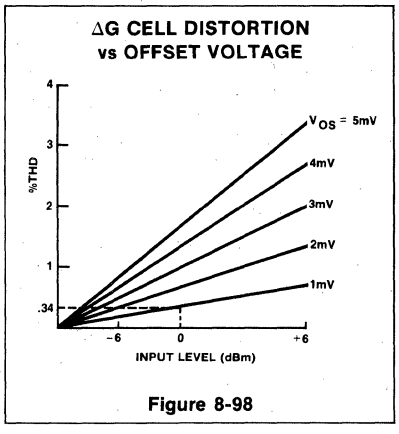


Figure 8-98

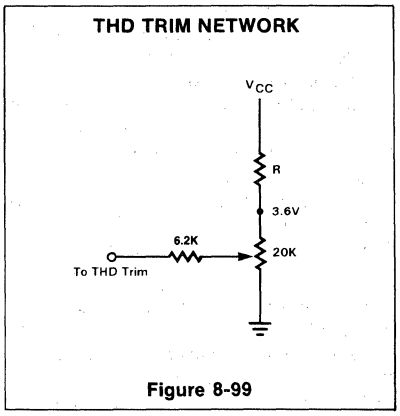


Figure 8-99

Figure 8-100 shows the noise performance of the ΔG cell. The maximum output level before clipping occurs in the gain cell is plotted along with the output noise in a 20kHz bandwidth. Note that the noise drops as the gain is reduced for the first 20dB of gain reduction. At high gains, the signal to noise ratio is 90dB, and the total dynamic range from maximum signal to minimum noise is 110dB.

Control signal feed-through is generated in the gain cell by imperfect device matching and mismatches in the current sources I_1 and I_2. When no input signal is present, changing I_G will cause a small output signal. The distortion trim is effective in nulling out any control signal feed-through, but in general, the null for minimum feed-through will be different than the null in distortion. The control signal feed-through can be trimmed independently of distortion by tying a current source to the ΔG input pin. This effectively trims I_1. Figure 8-101 shows such a trim network.

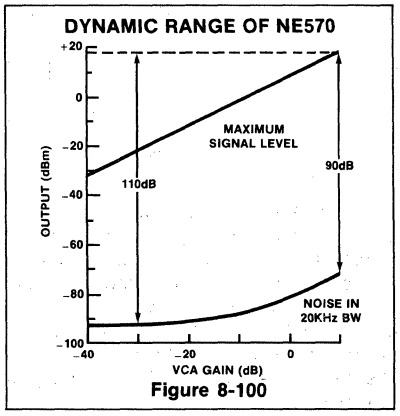


Figure 8-100

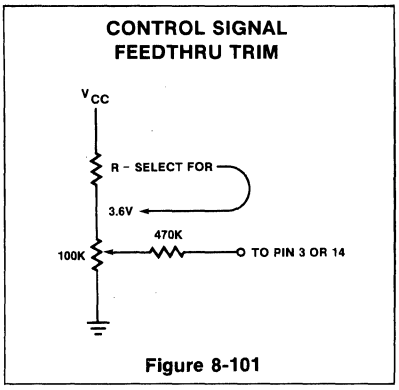


Figure 8-101

OPERATIONAL AMPLIFIER

The main op amp shown in the chip block diagram is equivalent to a 741 with a 1MHz bandwidth. Figure 8-102 shows the basic circuit. Split collectors are used in the input pair to reduce g_m, so that a small compensation capacitor of just 10pf may be used. The output stage, although capable of output currents in excess of 20mA., is biased for a low quiescent current to conserve power. When driving heavy loads, this leads to a small amount of crossover distortion.

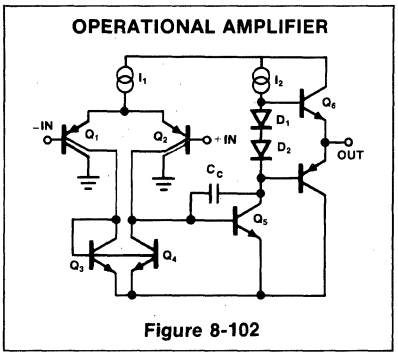


Figure 8-102

RESISTORS

Inspection of the gain equations in Figure 8-91 and 8-92 will show that the basic compressor and expandor circuit gains may be set entirely by resistor ratios and the internal voltage reference. Thus, any form of resistors that match well would suffice for these simple hookups, and absolute accuracy and temperature coefficient would be of no importance. However, as one starts to modify the gain equation with external resistors, the internal resistor accuracy and tempco become very significant. Figure 8-103 shows the effects of the temperature on the diffused resistors which are normally used in integrated circuits, and the ion implanted resistors which are used in this circuit. Over the critical 0°C to 70°C temperature range, there is a 10 to 1 improvement in drift from a 5% charge for the diffused resistors, to a .5% change for the implemented resistors. The implanted resistors have another advantage in that they can be made 1/7 the size of the diffused resistors due to the higher resistivity. This saves a significant amount of chip area.

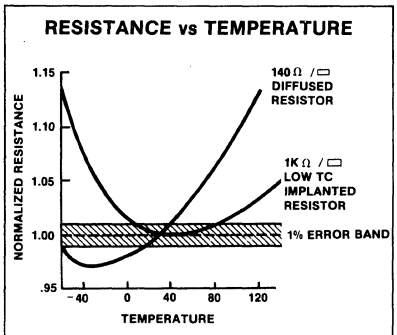


Figure 8-103

APPLICATIONS

The following circuits will illustrate some of the wide variety of applications for the NE570.

BASIC EXPANDOR

Figure 8-104 shows how the circuit would be hooked up for use as an expandor. Both the rectifier and the ΔG cell inputs are tied to V_{in} so that the gain is proportional to the average value of (V_{in}). Thus, when V_{in} falls 6dB, the gain drops 6dB and the output drops 12dB. The exact expression for the gain is

$$\text{Gain exp.} = \frac{2\,R_3\,V_{in}\,(ave)}{R_1\,R_2\,I_B}\;;\; I_B = 140\mu A$$

The maximum input that can be handled by the circuit in Figure 8-104 is a peak of 3V. The rectifier input current can be as large as $I = 3V/R_1 = 3V/10K = 300\mu A$. The ΔG cell input current should be limited to $I = 2.8V/R_2 = 2.8V/20K = 140\mu A$. If it is necessary to handle larger input voltages than 0 ± 2.8V pk, external resistors should be placed in series with R_1 and R_2 to limit the input current to the above values.

Figure 8-104 shows a pair of input capacitors C_{in1} and C_{in2}. It is not necessary to use both capacitors if low level tracking accuracy is not important. If R_1 and R_2 are tied together and share a common capacitor, a small current will flow between the ΔG cell summing node and the rectifier summing node due to offset voltages. This current will produce an error in the gain control signal at low levels, degrading tracking accuracy.

The output of the expandor is biased up to 3V by the dc gain provided by R_3, R_4. The output will bias up to

$$V_{out}\,dc = \left(1 + \frac{R_3}{R_4}\right) \quad V_{ref}$$

For supply voltages higher than 6V, R_4 can be shunted with an external resistor to bias the output up to $^1/_2V_{CC}$.

Note that it is possible to externally increase R_1, R_2, and R_3, and to decrease R_3 and R_4. This allows a great deal of flexibility in setting up system levels. If larger input signals are to be handled, R_1 and R_2 may be increased; if a larger output is required, R_3 may be increased. To obtain the largest dynamic range out of this circuit, the rectifier input should always be as large as possible (subject to the ±300μA peak current restriction).

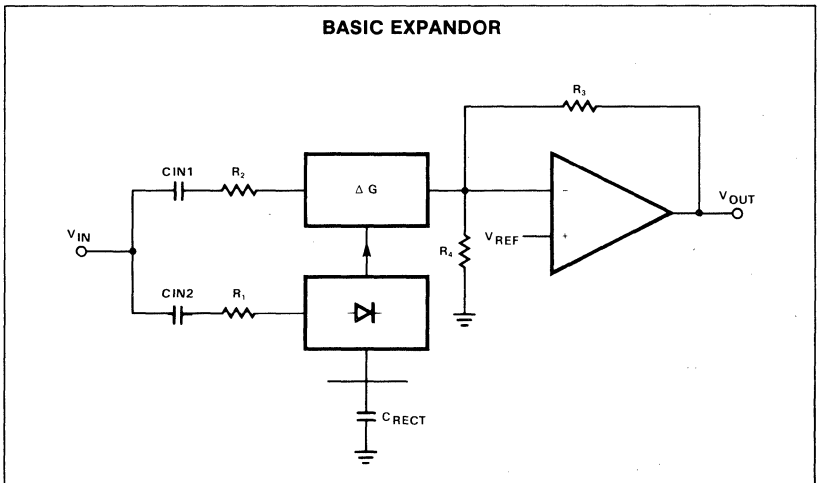


Figure 8-104

BASIC COMPRESSOR

Figure 8-105 shows how to use the NE570/571 as a compressor. It functions as an expandor in the feedback loop of an op amp. If the input rises 6dB, the output can rise only 3dB. The 3dB increase in output level produces a 3dB increase in the gain in the ΔG cell, yielding a 6dB increase in feedback current to the summing node. Exact expression for gain is

$$\text{Gain (comp.)} = \left[\frac{R_1 R_2 I_B}{2 R_3 V_{in}\,(ave)}\right]^{1/2}$$

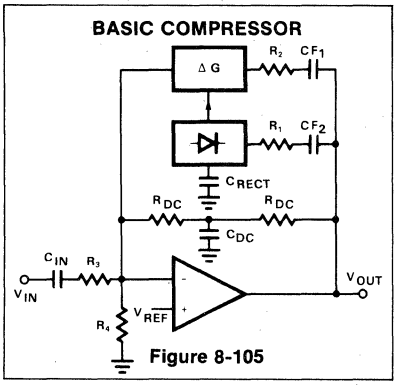


Figure 8-105

The same restrictions for the rectifier and ΔG cell maximum input current still hold, which place a limit on the maximum compressor output. As in the expandor, the rectifier and ΔG cell inputs could be made common to save a capacitor, but low level tracking accuracy would suffer. Since there is no dc feedback path around the op amp through the ΔG cell, one must be provided externally. The pair of resistors R_{dc} and the capacitor C_{dc} must be provided. The op amp output will bias up to

$$V_{out}\,dc = \left(1 + \frac{2\,R_{dc}}{R_4}\right) V_{ref}$$

For the largest dynamic range, the compressor output should be as large as possible so that the rectifier input is as large as possible (subject to the ±300μA peak current restriction). If the input signal is small, a large output can be produced by reducing R_3 with the attendant decrease in input impedance, or by increasing R_1 or R_2. It would be best to increase R_2 rather than R_1 so that the rectifier input current is not reduced.

DISTORTION TRIM

Distortion can be produced by voltage offsets in the ΔG cell. The distortion is mainly even harmonics, and drops with decreasing input signal. (Input signal meaning the current into the ΔG cell.) The THD trim terminal provides a means for trimming out the offset voltages and thus trimming out the distortion. The circuit shown in Figure 8-106 is suitable, as would be any other capable of delivering ±30μA into 100Ω resistor tied to 1.8V.

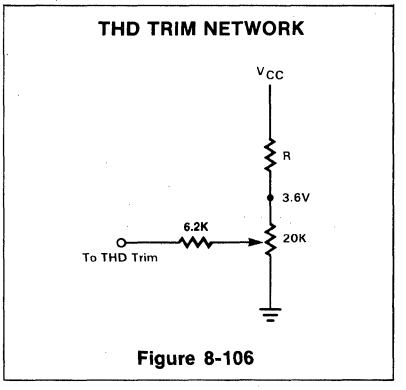


Figure 8-106

LOW LEVEL MISTRACKING

The compandor will follow a 2 to 1 tracking ratio down to very low levels. The rectifier is responsible for errors in gain, and it is the rectifier input bias current of <100na that produces errors at low levels. The magnitude of the error can be estimated. For a full scale rectifier input signal of ±200μA, the average input current will be 127μA. When the input signal level drops to a 1μA average, the bias current will produce a 10% or 1dB error in gain. This will occur at 42dB below the maximum input level.

It is possible to deviate from the 2 to 1 transfer characteristic at low levels as shown in the circuit of Figure 8-107. Either R_a or R_b, (but not both), is required. The voltage on C_{rect} is $2xV_{be}$ plus V_{in} ave. For low level inputs V_{in} ave is negligible, so we can assume 1.3V as the bias on C_{rect}. If R_a is placed from C_{rect} to gnd we will bleed off a current $I = 1.3V/R_a$. If the rectifier average input current is less than this value, there will be no gain control input to the ΔG cell, so that its gain will be zero and the expandor output will be zero. As the input level is raised, the input current will exceed $1.3V/R_a$ and the expandor output will become active. For large input signals, R_a will have little effect. The result of this is that we will deviate from the 2 to 1 expansion, present at high levels, to an infinite expansion at low levels where the output shuts off completely. Figure 8-108 shows some examples of tracking curves which can be obtained. Complementary curves would be obtained for a compressor, where at low level signals the result would be infinite compression. The bleed current through R_a will be a function of temperature because of the two V_{be} drops, so the low level tracking will drift with temperature. If a negative supply is available, it would be desirable to tie R_a to that, rather than ground, and to increase its value accordingly. The bleed current will then be less sensitive to the V_{be} temperature drift.

R_b will supply an extra current to the rectifier equal to $(V_{CC} - 1.3V)/R_b$. In this case, the expandor transfer characteristic will deviate towards 1 to 1 at low levels. At low levels the expandor gain will stop dropping and the expansion will cease. In a compressor this would lead to a lack of compression at low levels. Figure 8-109 shows some typical transfer curves. An R_b value of approximately 2.5Meg would trim the low level tracking so as to match the Bell system N2 trunk compandor characteristic.

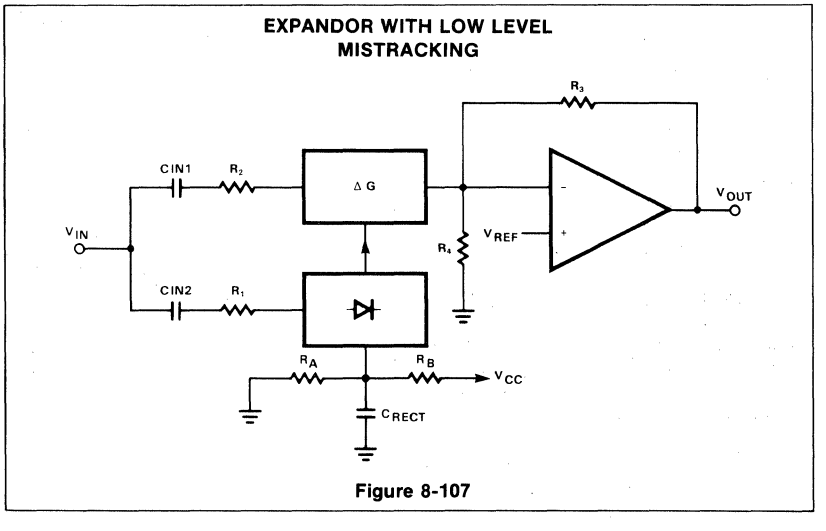


Figure 8-107

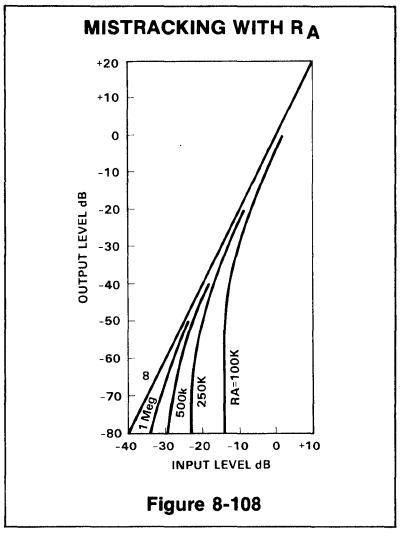


Figure 8-108

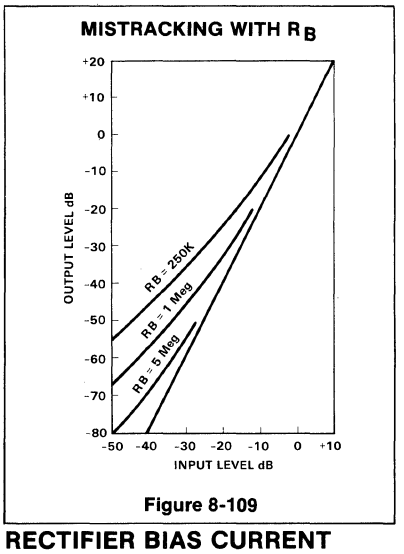


Figure 8-109

RECTIFIER BIAS CURRENT CANCELLATION

The rectifier has an input bias current of between 50 and 100nA. This limits the dynamic range of the rectifier to about 60dB. It also limits the amount of attenuation of the ΔG cell. The rectifier dynamic range may be increased by about 20dB by the bias current trim network shown in Figure 8-110 Figure 8-111 shows the rectifier performance with and without current cancellation.

ATTACK AND DECAY TIME

The attack and decay times of the compandor are determined by the rectifier filter time constant 10KxC$_{rect}$. Figure 8-112 shows how the gain will change when the input signal undergoes a 10, 20, or 30dB change in level.

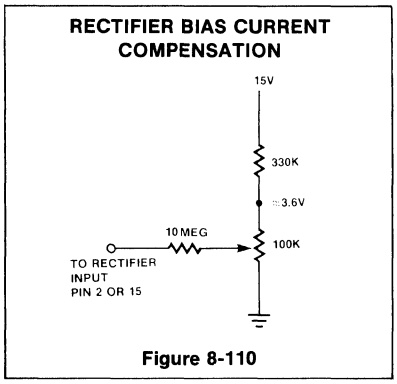


Figure 8-110

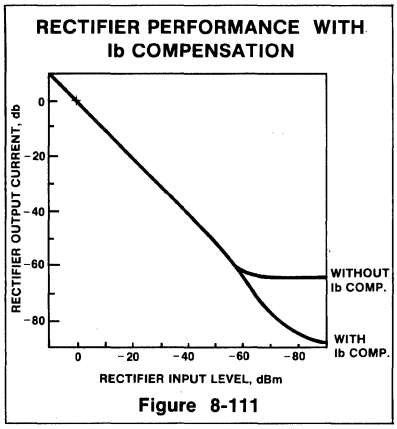


Figure 8-111

The attack time is much faster than the decay, which is desirable in most applications. Figure 8-113 shows the compressor attack envelope for a +12dB step in input level. The initial output level of 1 unit instantaneously rises to 4 units, and then starts to fall towards its final value of 2 units. The CCITT recommendation on attack and decay times for telephone system compandors, defines the attack time as when the envelope has fallen to a level of 3 units, corresponding to t = .15 in the figure. The CCITT recommends an attack time of 3± 2ms, which suggests an RC product of 20ms. Figure 8-114 shows the compressor output envelope when the input level is suddenly reduced 12dB. The output, initially at a level of 4 units, drops 12dB to 1 unit and then rises to its final value of 2 units. The CCITT defines release time as when the output has risen to 1.5 units, and suggests a value of 13.5 ± 9ms. This corresponds to t = .675 in the figure, which gain suggests a 20ms RC product. Since R_1 = 10K, the CCITT recommendations will be met if C$_{rect}$ = 2μf.

There is a trade off between fast response and low distortion. If a small C$_{rect}$ is used to get very fast attack and decay, some ripple will appear on the gain control line and produce distortion. As a rule, a 1μf C$_{rect}$ will produce .2% distortion at 1kHz. The distortion is inversely proportional to both frequency and capacitance. Thus, for telephone applications where C$_{rect}$ = 2μf, the ripple would cause .1% distortion at 1kHz and .33% at 300hz. The low frequency distortion generated by a compressor would be cancelled (or undistorted) by an expandor, providing that they have the same value of C$_{rect}$.

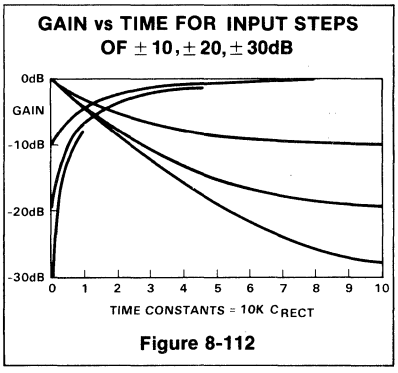


Figure 8-112

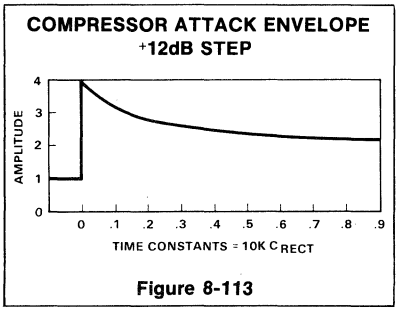


Figure 8-113

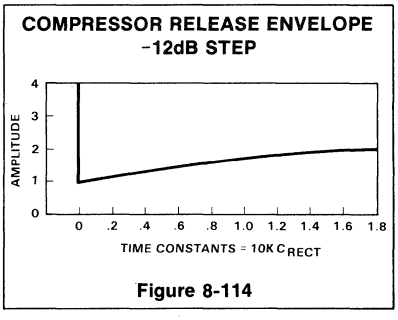


Figure 8-114

FAST ATTACK, SLOW RELEASE HARD LIMITER

The NE570/571 can be easily used to make an excellent limiter. Figure 8-115 shows a typical circuit which requires 1/2 of an NE570/571, 1/2 of an LM339 quad comparator, and a pnp transistor. For small signals, the ΔG cell is nearly off, and the circuit runs at unity gain as set by R_8, R_7. When the output signal tries to exceed a + or - 1 volt peak, a comparator threshold is exceeded. The pnp is turned on and rapidly charges C_4 which activates the ΔG cell. Negative feedback through the ΔG cell reduces the gain, and the output signal level. The attack time is set by the RC product of R_{18} and C_4, and the release time is determined by C_4 and the internal rectifier resistor, which is 10K. The circuit shown attacks in less than 1ms and has a release time constant of 100ms. R_9 trickles about .7μA through the rectifier to prevent C_4 from becoming completely discharged. The gain cell is activated when the voltage on pin 1 or 16 exceeds two diode drops. If C_4 were allowed to completely discharge, there would be a slight delay before it recharged to > 1.2V and activated limiting action.

A stereo limiter can be built out of 1 NE570/571, 1 LM339 and two pnp transistors. The resistor networks R_{12}, R_{13} and R_{14}, R_{15}, which set the limiting thresholds, could be common between channels. To gang the stereo channels together (limiting in one channel will produce a corresponding gain change in the second channel to maintain the balance of the stereo image), then pins 1 and 16 should be jumpered together. The outputs of all 4 comparators may then be tied together, and only one pnp transistor and one capacitor C_4 need be used. The release time will then be the product 5K×C_4 since two channels are being supplied current from C_4.

USE OF EXTERNAL OP AMP

The operational amplifiers in the NE570/571 is not adequate for some applications. The slew rate, bandwidth, noise, and output drive capability can limit performance in many systems. For best performance, an external op amp can be used. The external op amp may be powered by bipolar supplies for a larger output swing.

Figure 8-116 shows how an external op amp may be connected. The non-inverting input must be biased at about 1.8V. This is easily accomplished by tying it to either pin 8 or 9, the THD trim pins, since these pins sit at 1.8V. An optional RC decoupling network is shown which will filter out the noise from the NE570/571 reference (typically about 10μV in 20kHz BW). The inverting input of the external op amp is tied to the inverting input of the internal op amp. The output of the external op amp is then used, with the internal op amp output left to float. If the external op amp is used single supply, (+V_{CC} and ground), it must have an input common mode range down to less than 1.8V.

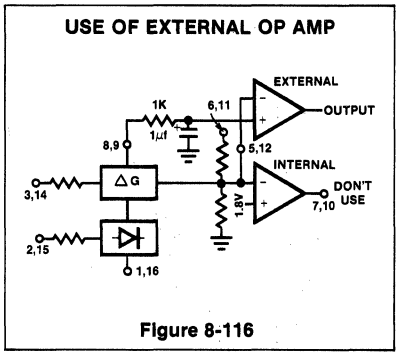
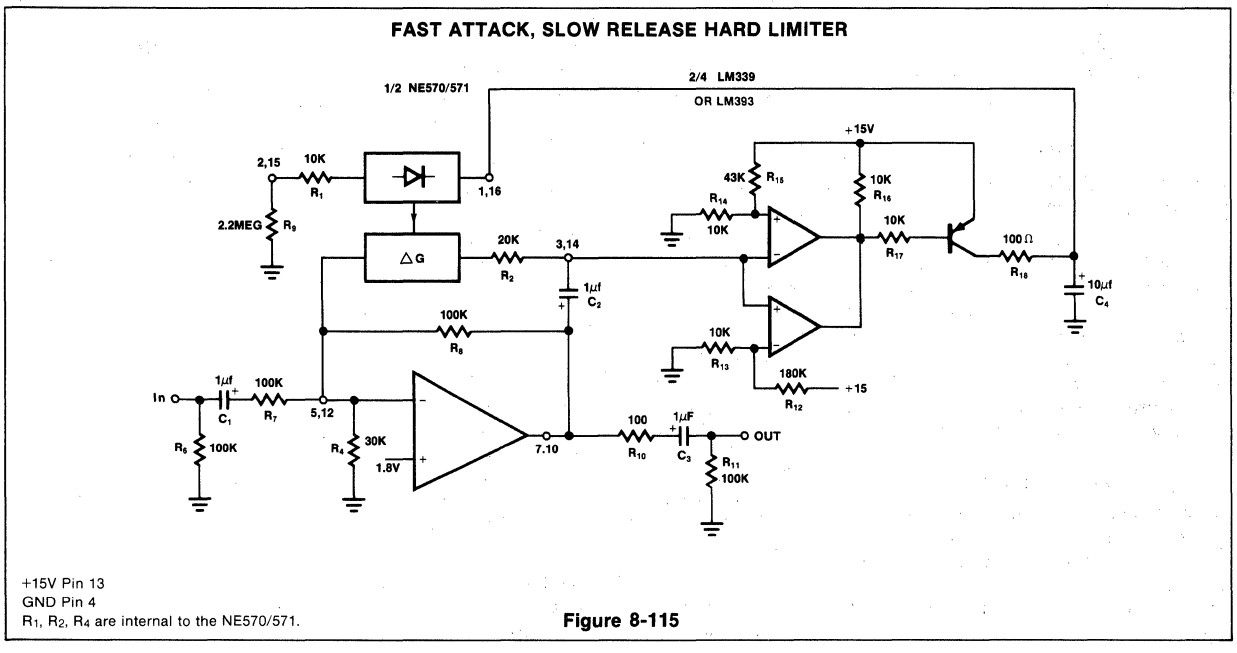


Figure 8-116

N2 COMPANDOR

There are four primary considerations involved in the application of the NE570/571 in an N2 compandor. These are matching of input and output levels, accurate 600Ω input and output impedances, conformance to the Bell system low level tracking curve, and proper attack and release times.

Figure 8-117 shows the implementation of an N2 compressor. The input level of .245V rms is stepped up to 1.41Vrms by the 600Ω: 20KΩ matching transformer. The 20K input resistor properly terminates the transformer. An internal 20KΩ resistor (R_3) is provided, but for accurate impedance termination an external resistor should be used. The output impedance is provided by the 4K output resistor and the 4KΩ: 600Ω output transformer. The .275V RMS output level



+15V Pin 13
GND Pin 4
R_1, R_2, R_4 are internal to the NE570/571.

Figure 8-115

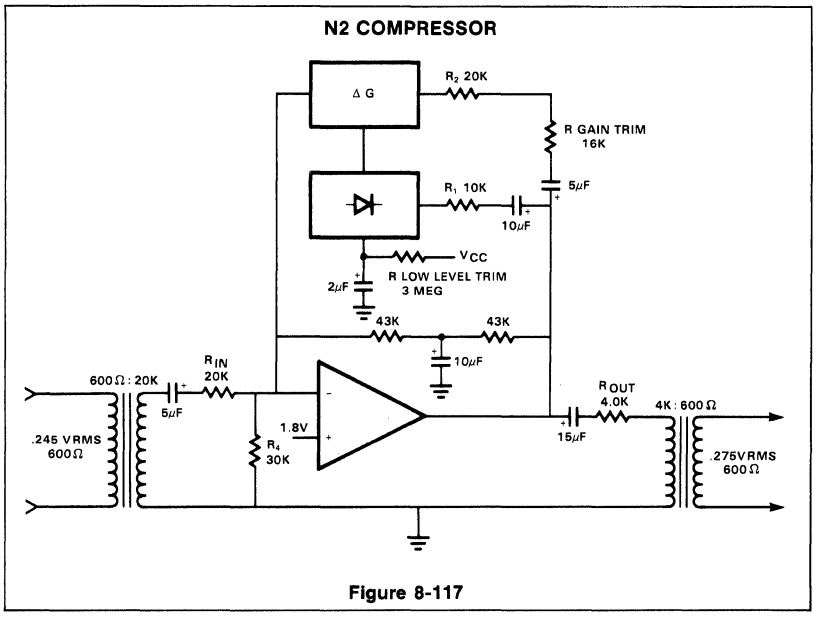


Figure 8-117

requires a 1.41V op amp output level. This can be provided by increasing the value of R_2 with an external resistor, which can be selected to fine trim the gain. A rearrangement of the compressor gain equation (6) allows us to determine the value for R_2.

$$R_2 = \frac{\text{Gain}^2\, R_3\, V_{in\ ave}}{R_1\, I_B} = \frac{1^2 \text{ X } 2 \text{ X } 20\text{K X } 1.27}{10\text{K X } 140\mu\text{A}}$$

$$= 36.3\text{K}$$

The external resistance required will thus be 36.3K - 20K = 16.3K.

The Bell compatible low level tracking characteristic is provided by the low level trim resistor from C_{rect} to V_{CC}. As shown in Figure 9-108 this will skew the system to a 1:1 transfer characteristic at low levels. The 2μf rectifier capacitor provides attack and release times of 3ms and 13.5ms respectively, as shown in Figures 8-97 and 8-98. The R-C-R network around the op amp provides dc feedback to bias the output at dc.

An N2 expandor is shown in Figure 8-118. The input level of 3.27Vrms is stepped down to 1.33V by the 600Ω: 100Ω transformer, which is terminated with a 100Ω resistor for accurate impedance matching. The output impedance is accurately set by the 150Ω output resistor and the 150Ω: 600Ω output transformer. With this configuration the 3.46V transformer output requires a 3.46V op amp output. To obtain this output level, it is necessary to increase the value of R_3 with an external trim resistor. The new value of R_3 can be found with the expandor gain equation.

$$R_3 = \frac{R_1\, R_2\, I_B\, \text{Gain}}{2\, V_{in\ ave}} = \frac{10\text{K X } 20\text{K X } 140\mu\text{A X } 2.6}{2 \text{ X } 1.20}$$

$$= 30.3\text{K}$$

An external addition to R_3 of 10K is required, and this value can be selected to accurately set the high level gain.

A low level trim resistor from C_{rect} to V_{CC} of about 3Meg provides matching of the Bell low level tracking curve, and the 2μf value of C_{rect} provides the proper attack and release times. A 16K resistor from the summing node to ground biases the output to $7V_{dc}$.

VOLTAGE CONTROLLED ATTENUATOR

The variable gain cell in the NE570/571 may be used as the heart of a high quality voltage controlled amplifier (VCA). Figure 8-119 shows a typical circuit which uses an external op amp for better performance, and an exponential converter to get a control characteristic of -6dB/V. Trim networks are shown to null out distortion and dc shift, and to fine trim gain to 0dB with zero volts of control voltage.

Op amp A_2 and transistors Q_1 and Q_2 form the exponential converter generating an exponential gain control current, which is fed into the rectifier. A reference current of 150μA, (15V and R_{20} = 100K), is attenuated a factor of two (6dB) for every volt increase in

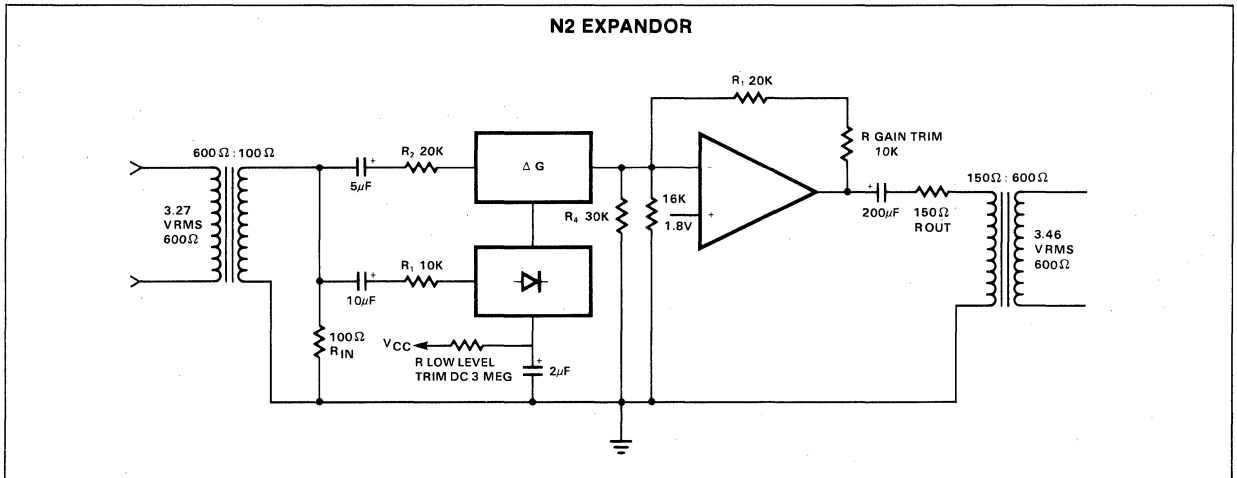


Figure 8-118

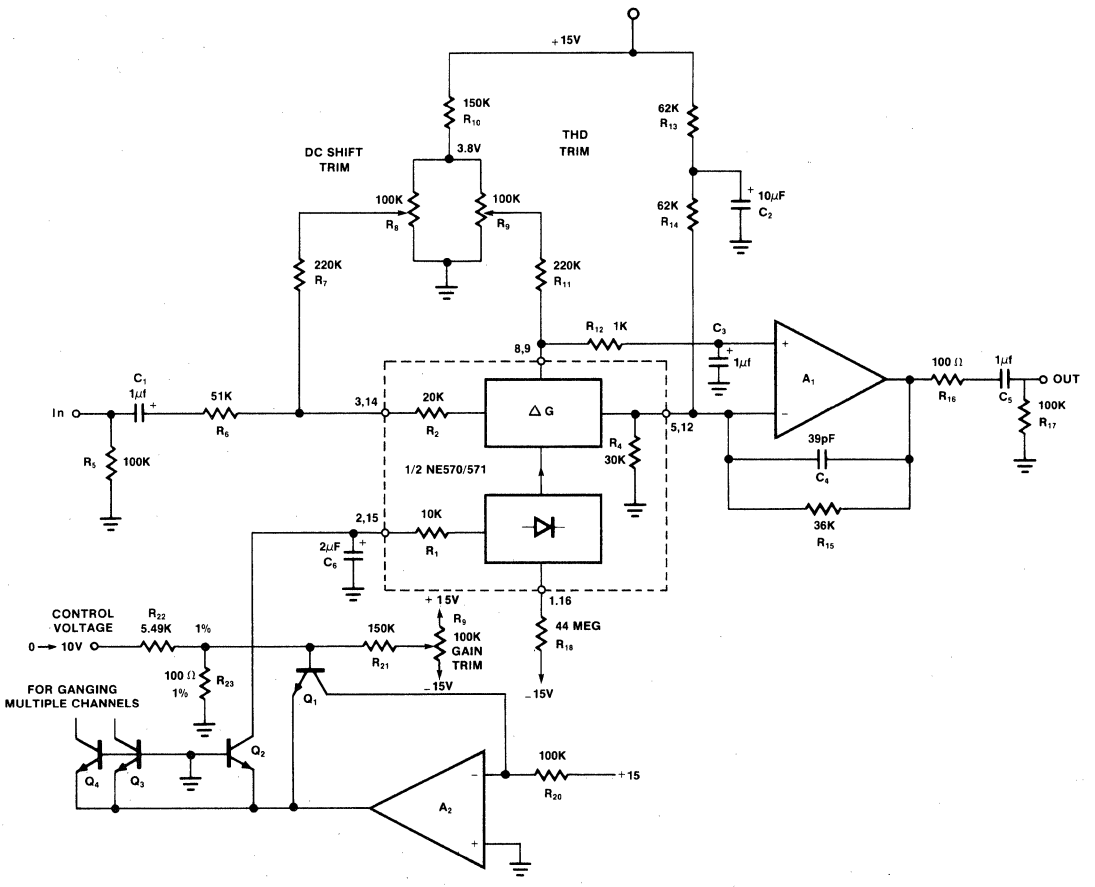


Figure 8-119

the control voltage. Capacitor C_6 slows down gain changes to a 20ms time constant (C_6 x R_1) so that an abrupt change in the control voltage will produce a smooth sounding gain change. R_{18} assures that for large control voltages the circuit will go to full attenuation. The rectifier bias current would normally limit the gain reduction to about 70dB. R_{18} draws excess current out of the rectifier. After approximately 50dB of attenuation at a -6dB/V slope, the slope steepens and attenuation becomes much more rapid until the circuit totally shuts off at about 9 volts of control voltage. A_1 should be a low noise high slew rate op amp. R_{13} and R_{14} establish approximately a zero volt bias at A_1's output.

With a zero volt control voltage, R_{19} should be adjusted for 0dB gain. At 1V (-6dB gain) R_9 should be adjusted for minimum distortion with a large (+10dBm) input signal. The output dc bias (A_1 output) should be measured at full attenuation (+10V control voltage) and then R_8 is adjusted to give the same value at 0dB gain. Properly adjusted, the circuit will give typically less than .1% distortion at any gain with a dc output voltage variation of only a few millivolts. The clipping level (140μA into pin 3, 14) is ±10V peak. A signal to noise ratio of 90dB can be obtained.

If several VCA's must track each other, a common exponential converter can be used. Transistors can simply be added in parallel with Q_2 to control the other channels. The transistors should be maintained at the same temperature for best tracking.

AUTOMATIC LEVEL CONTROL

The NE570 can be used to make a very high performance ALC as shown in Figure 8-120. This circuit hookup is very similar to the basic compressor shown in Figure 8-105, except that the rectifier input is tied to the input rather than the output. This makes gain inversely proportional to input level so that a 20dB drop in input level will produce a 20dB increase in gain. The output will remain fixed at a constant level. As shown, the circuit will maintain an output level of ±1dbm for an input range of +14 to -43dbm at 1khz. Additional external components will allow the output level to be adjusted. Some relevant design equations are:

$$\text{Output level} = \frac{R_1 R_2 I_B}{2 R_3}\left(\frac{V_{in}}{V_{in(avg)}}\right);\ I_B = 140\mu A$$

$$\text{Gain} = \frac{R_1 R_2 I_B}{2 R_3 V_{in\ (avg)}} \quad \text{where}$$

$$\frac{V_{IN}}{V_{IN(avg)}} = \frac{\pi}{2\sqrt{2}} = 1.11 \text{ (for sine wave)}$$

If ALC action at very low input levels is not desired, the addition of resistor R_X will limit the maximum gain of the circuit.

$$\text{Gain max.} = \frac{\frac{R_1 + R_X}{1.8V} \times R_2 \times I_B}{2\,R_3}$$

The time constant of the circuit is determined by the rectifier capacitor, C_{rect}, and an internal 10K resistor.

$$\tau = 10K\ C_{rect}$$

Response time can be made faster at the expense of distortion. Distortion can be approximated by the equation.

$$THD = \left(\frac{1\mu f}{C_{rect}}\right)\left(\frac{1KHz}{freq.}\right) \times .2\%$$

VARIABLE SLOPE COMPRESSOR-EXPANDOR

Compression and expansion ratios other than 2:1 can be achieved by the circuit shown in Figure 8-121. Rotation of the dual potentiometer causes the circuit hookup to change from a basic compressor to a basic expandor. In the center of rotation, the circuit is 1:1, has neither compression or expansion. The (input) output transfer characteristic is thus continuously variable from 2:1 compression, through 1:1, up to 1:2 expansion. If a fixed compression or expansion ratio is desired, proper selection of fixed resistors can be used instead of the potentiometer. The optional threshold resistor will make the compression or expansion ratio deviate towards 1:1 at low levels. A wide variety of (input) output characteristics can be created with this circuit, some of which are shown in Figure 8-122.

HI FI COMPANDOR

The NE570 can be used to construct a high performance compandor suitable for use with music. This type of system can be used for noise reduction in tape recorders, transmission systems, bucket brigade delay lines, and digital audio systems. The circuits to be described contain features which improve performance, but are not required for all applications.

A major problem with the simple NE570 compressor (Figure 8-105) is the limited op amp gain at high frequencies. For weak input signals, the compressor circuit operates at high gain and the 570 op amp simply runs out of loop gain. Another problem with the 570 op amp is its limited slew rate of about .6v/μs. This is a limitation of the expandor, since the expandor is more likely to produce large output signals than a compressor.

AUTOMATIC LEVEL CONTROL

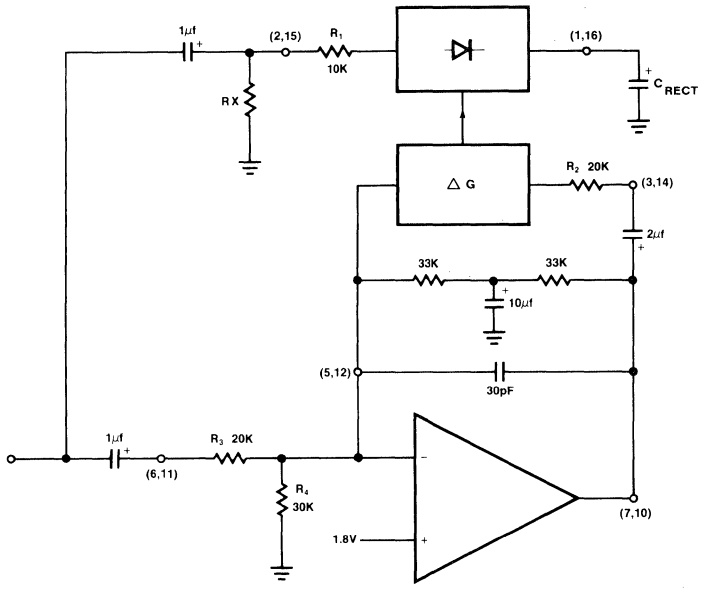


Figure 8-120

VARIABLE SLOPE COMPRESSOR-EXPANDOR

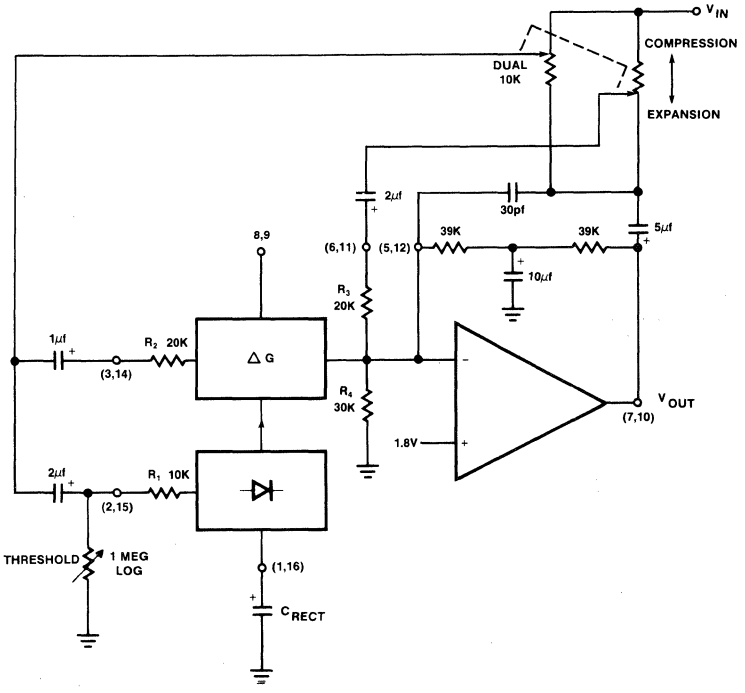


Figure 8-121

TYPICAL INPUT-OUTPUT TRACKING CURVES OF VARIABLE RATIO COMPRESSOR-EXPANDOR

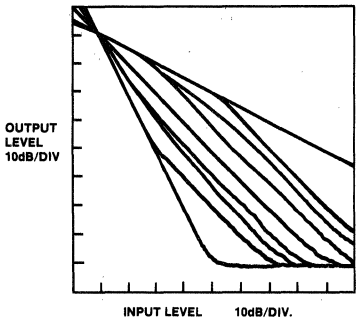


Figure 8-122

Figure 8-123 is a circuit for a high fidelity compressor which uses an external op amp and has a high gain and wide bandwidth. An input compensation network is required for stability.

Another feature of the circuit in Figure 8-123 is that the rectifier capacitor (C_9) is not grounded, but is tied to the output of an op amp circuit. This circuit, built around an LM324, speeds up the compressor attack time at low signal levels. The response times of the simple expandor and compressor (Figures 8-104 and 8-105) become longer at low signal levels. The time constant is not simply $10K \times C_{rect}$, but is really

$$\left(10K + 2\left(\frac{.026V}{I_{rect}}\right)\right) \times C_{rect}.$$

When the rectifier input level drops from 0dBm to -30dBm, the time constant increases from $10.7K \times C_{rect}$ to $32.6K \times C_{rect}$. In systems where there is unity gain between the compressor and expandor, this will cause no overall error. Gain or loss between the compressor and expandor will be a mistracking of low signal dynamics. The circuit with the LM324 will greatly reduce this problem for systems which cannot guarantee the unity gain.

When a compressor is operating at high gain, (small input signal), and is suddenly hit with a signal, it will overload until it can reduce its gain. Overloaded the output will attempt to swing rail to rail. This compressor is limited to approximately a 7V peak to peak output swing by the brute force clamp diodes D_3 and D_4. The diodes cannot be placed in the feedback loop because their capacitance would limit high frequency gain. The purpose of limiting the output swing is to avoid overloading any succeeding circuit such as a tape recorder input.

HI-FI COMPRESSOR WITH PRE-EMPHASIS

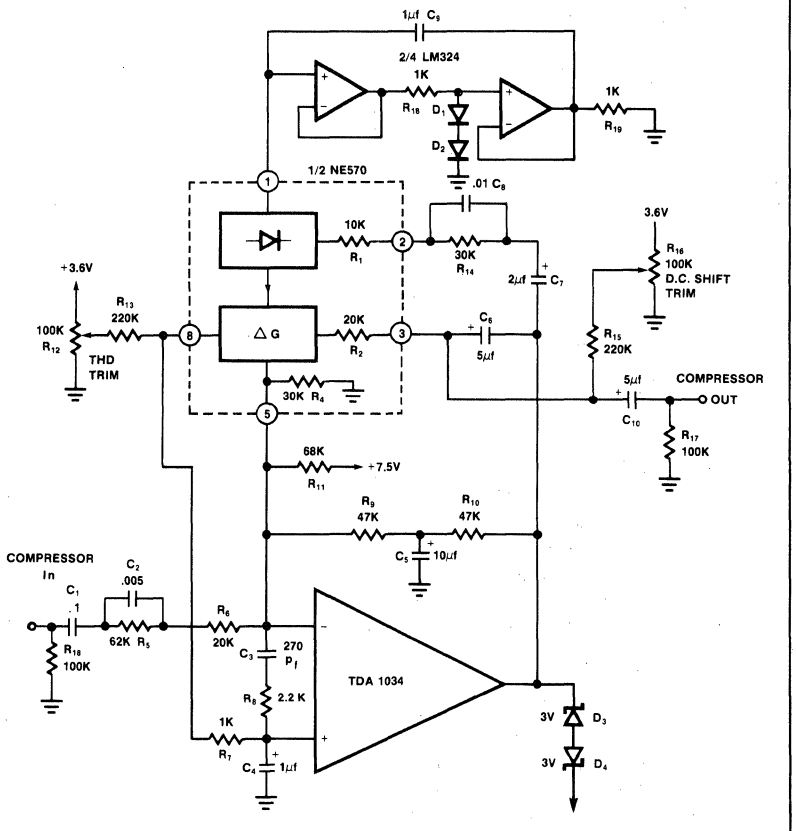


Figure 8-123

The time it takes for the compressor to recover from overload is determined by the rectifier capacitor C_9. A smaller capacitor will allow faster response to transients, but will produce more low frequency third harmonic distortion due to gain modulation. A value of 1 µf seems to be a good compromise value and yields good subjective results. Of course, the expandor should have exactly the same value rectifier capacitor for proper transient response. Systems which have good low frequency amplitude and phase response can use compandors with smaller rectifier capacitors, since the third harmonic distortion which is generated by the compressor will be undistorted by the expandor.

Simple compandor systems are subject to a problem known as breathing. As the system is changing gain, the change in the background noise level can sometimes be heard. The compressor in Figure 8-123 contains a high frequency pre-emphasis circuit (C_2, R_5 and C_8, R_{14}), which helps solve this problem. Matching de-emphasis on the expandor is required. More complex designs could make the pre-emphasis variable and further reduce breathing.

The expandor to complement the compressor is shown in Figure 8-124. Here an external op amp is used for high slew rate. Both the compressor and expandor have unity gain levels of 0dBm. Trim networks are shown for distortion (THD) and dc shift. The distortion trim should be done first, with an input of 0dBm at 10kHz. The dc shift should be adjusted for minimum envelope bounce with tone bursts. When applied to consumer tape recorders, the subjective performance of this system is excellent.

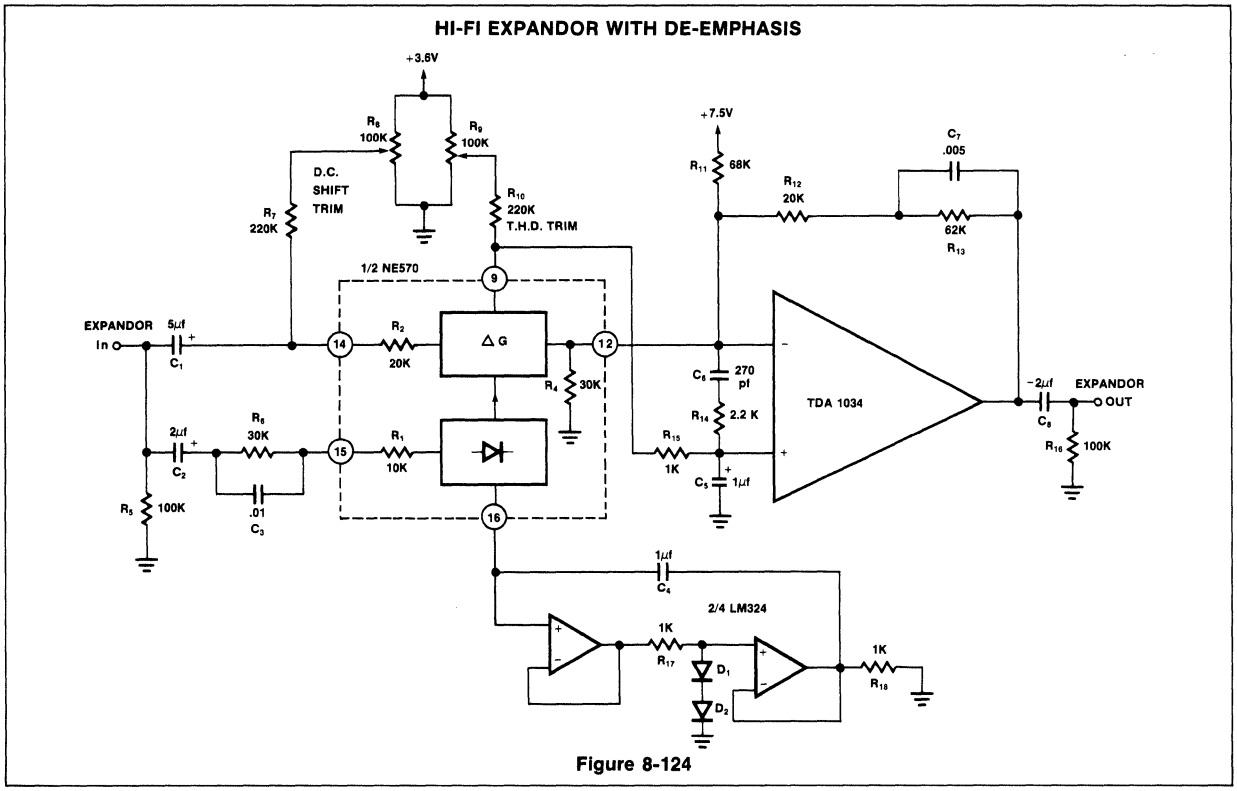


Figure 8-124

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SECTION 26
PHASE LOCKED LOOPS

INTRODUCTION

Phase Locked Loop (PLLs) are a new class of monolithic circuits developed by Signetics, but they are based on frequency feedback technology which dates back 40 years.

A phase locked loop is basically an electronic servo loop consisting of a phase detector, a low pass filter and a voltage controlled oscillator. Its controlled oscillator phase makes it capable of locking or synchronizing with an incoming signal. If the phase changes, indicating the incoming frequency is changing , the phase detector output voltage increases or decreases just enough to keep the oscillator frequency the same as the incoming frequency, preserving the locked condition. Thus, the average voltage applied to the controlled oscillator is a function of the frequency of the incoming signal. In fact, the low pass filter voltage *is* the demodulated output when the incoming signal is frequency modulated (provided the controlled oscillator has linear voltage-to-frequency transfer characteristic). The synchronous reception of radio signals using PLL techniques was described (Ref. 1) in the early thirties. You may have heard of the "homodyne" receiver.

The first widespread use of the phase lock, however, was in TV receivers to synchronize the horizontal and vertical sweep oscillators to the transmitted sync pulses. Lately, narrowband phase locked receivers have proved to be of considerable benefit in tracking weak satellite signals because of their superior noise immunity. Applicaitons such as these were implemented primarily in discrete component form and involved considerable complexity even after the advent of transistors. This complexity made PLL techniques impractical or uneconomical in the majority of systems.

The development of complete, single-chip phase locked loops has changed this situation considerably. Now, a single packaged device with a few external components will offer the user all the benefits of phase locked loop operation, including independent center frequency and bandwidth adjustment, high noise immunity, high selectivity, high frequency operation and center frequency tuning by means of a single external component.

Signetics makes three basic classes of single-chip PLL circuits: the general purpose PLL, the PLL with an added multiplier and the PLL tone decoder.

The 560N, 562N and 565 are general purpose phase locked loops containing an oscillator, phase detector and amplifier. When locked to an incoming signal, they provide two outputs: a voltage proportional to the frequency of the incoming signal (FM output) and the square wave oscillator output which, during lock, is equal to the incoming frequency. All general purpose devices are optimized to provide a linear frequency-to-voltage transfer characteristic.

The 561N contains a complete PLL as those above, plus the additional multiplier or quadrature phase detector required for AM demodulation. In addition to the standard FM and oscillator outputs, it also provides an output voltage which is proportional to the amplitude of the incoming signal (AM output). The 561N is opitmized for highly linear FM and AM demodulation.

The 567 is a special purpose phase locked loop intended solely for use as a tone decoder. It contains a complete PLL including oscillator, phase detector and amplifier as well as a quadrature phase detector or multiplier. If the signal amplitude at the locked frequency is above a minimal value, the driver amplifier turns on, driving a load as much as 200mA. It, thus, gives an output whenever an inband tone is present. The 567 is optimized for both center frequency and bandwidth stability.

The 566 is not a phase locked loop, but a precision voltage-controllable waveform generator derived from the oscillator of the 565 general purpose loop. Because of its similarity to the 565 and because it lends itself well to use in, and in conjunction with, phased locked loops, it has been included in this section.

Table 9-1 summarizes the characteristics of Signetics phase locked loop products.

A considerable quantity of detailed specifications and publications information for these products is included in the Linear Spec. Handbook. Because many readers are likely to be unfamiliar with the terminology and operating characteristics of phase locked loops, a glossary of terms and a general explanation of PLL principles are included here with a detailed discussion of the action of the individual loop elements.

The tradeoff and setup section will assist the reader in some of the considerations involved in selecting and applying the loop products to meet system requirements. A brief summary of measurement techniques has been presented to aid the user in achieving his performance goals.

Detailed descriptions have been provided for each of the loop products. The user can supplement the suggested connection diagrams with his own schemes.

Perhaps the best way to become familiar with the many uses of phase locked loops is to actually study the various application circuits provided. These circuits have been drawn from many sources—textbooks, users, Signetics' applications engineers and the 1970 Signetics—EDN Phase Locked Loop contest. Every effort has been made to provide usable, workable circuits which may be copied directly or used as jumping-off points for other imaginative applications.

The section on interfacing will aid the user in driving different forms of logic from PLL outputs and the section on expanding loop capabilities will show how to achieve improved performance in certain difficult applications.

PHASED LOCKED LOOP TERMINOLOGY

The following is a brief glossary of terms encountered in PLL literature.

Capture Range ($2\omega_C$)—Although the loop will remain in lock throughout its lock range, it may not be able to acquire lock at the tracking range extremes. The range over which the loop *can* acquire lock is termed capture range. The capture range is sometimes called the *Lock-in Range.* (The latter refers to how close a signal must be to the center frequency before acquisition can occur. It is thus one-half the capture range of ω_C.)

Current Controlled Oscillator (CCO)—An oscillator similar to a VCO in which the frequency is determined by an applied current.

Damping Factor (ζ)—The standard damping constant of a second order feedback system. In the case of the PLL, it refers to the ability of the loop to respond quickly to an input frequency step without excessive overshoot.

Free-Running Frequency (f_o, ω_o)—Also called the *Center Frequency,* this is the frequency at which the loop VCO operates when not locked to an input signal. The same symbols (f_o, ω_o) used for the free-running frequency are commonly used for the general oscillator frequency. It is usually clear which is meant from the context.

Lock Range ($2\omega_L$)—The range of input frequencies over which the loop will remain in lock. It is also called the *Tracking Range* or *Hold-In Range.* (The latter refers to how far the loop frequency can be deviated from the center frequency and is one-half the lock range or ω_L.)

Loop Gain (K_v)—The product of the dc gains of all the loop elements, in units of $(sec)^{-1}$.

USER'S QUICK-LOOK GUIDE TO SIGNETICS PLLs

	UPPER FREQUENCY (MHz)	MAXIMUM LOCK RANGE (%f_o)	FM DISTORTION	OUTPUT SWING ±5% DEVIATION (volts p-p)	CENTER FREQUENCY STABILITY (ppm/°C)	FREQUENCY DRIFT WITH SUPPLY VOLTAGE (%/volt)	INPUT RESISTANCE	AM OUTPUT AVAILABLE	TYPICAL SUPPLY CURRENT (mA)	SUPPLY VOLTAGE RANGE (volts)
NE560	30	40%	.3%	1	±600	.3	2K**	No	9	+16 to +26
NE561	30	40%	.3%	1	±600	.3	2K**	Yes	10	+16 to +26
NE562	30	40%	.5%	1	±600	.3	2K**	No	12	+16 to +30
NE564	50	40%	.5%	.1	±400	.3	3K	No	30	+4.5 to +12
NE565	.5	120%	.2%	.15	±200	.16	5K	No	8	± 5 to ±12
SE565	.5	120%	.2%	.15	±100	.08	5K	No	8	± 5 to ±12
NE567	.5	14%	5%*	.20	35±60	.7	20K**	Yes*	7	± 4.5 to +9
SE567	.5	14%	5%*	.20	35±60	.5	20K**	Yes*	6	+ 4.5 to +9
NE566	.5		.2%	30%/V***	±200	.16			7	+10 to +26
SE566	.5		.2%	30%/V***	±100	.08			7	+10 to +26

* The 567 AM and FM outputs are available, but are not optimized for linear demodulation.
** Input biased internally.
*** Figure shown is VCO gain in percent deviation per volt.

Table 9-1

Loop Noise Bandwidth (B_L)—A loop property related to damping and natural frequency which describes the effective bandwidth of the received signal. Noise and signal components outside this band are greatly attenuated.

Low Pass Filter (LPF)—A low pass filter in the loop which permits only dc and low frequency voltages to travel around the loop. It controls the capture range and the noise and out-band signal rejection characteristics.

Natural Frequency (ω_n)—The characteristic frequency of the loop, determined mathematically by the final pole positions in the complex plane. May be determined experimentally as the modulation frequency for which an underdamped loop gives the maximum output and at which phase error swing is the greatest.

Phase Detector Gain Factor (K_d)—The conversion factor between the phase detector output voltage and the phase difference between input and VCO signals in volts/radian. At low input signal amplitudes, the gain is also a function of input level.

Phase Detector (PD)—A circuit which compares the input and VCO signals and produces an error voltage which is dependent upon their relative phase difference. This error corrects the VCO frequency during tracking. Also called *Phase Comparator. A Multiplier* or *Mixer* is often used as a phase detector.

Quadrature Phase Detector (QPD)—A phase detector operated in quadrature (90° out of phase) with the loop phase detector. It is used primarily for AM demodulation and lock detection.

BLOCK DIAGRAM OF PHASE LOCKED LOOP

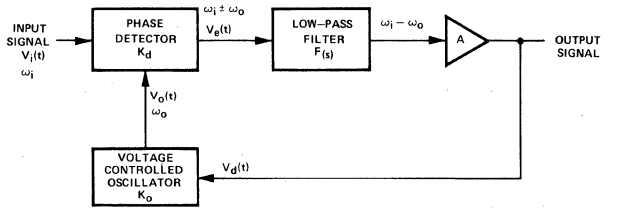


Figure 9-1

VCO Conversion Gain (K_o)—The conversion factor between VCO frequency and control voltage in radians/second/volt.

Voltage Controlled Oscillator (VCO)—An oscillator whose frequency is determined by an applied control voltage.

THE PHASE LOCKED LOOP PRINCIPLE

The phase locked loop is a feedback system comprised of a phase comparator, a low pass filter and an error amplifier in the forward signal path and a voltage-controlled oscillator (VCO) in the feedback path. The block diagram of a basic PLL system is shown in Figure 9-1. Detailed analysis of the PLL as a feedback control system has been discussed in the literature (Ref. 2). Perhaps the single most important point to realize when designing with the PLL is that it is a feedback system and, hence, is characterized mathematically by the same equations that apply to other, more conventional feedback systems. The parameters in the equations are somewhat different, however, since the feedback error signal in the phase locked system is a phase rather than a current or voltage signal, as is usually the case in conventional feedback systems.

Loop Operation

A rigorous mathematical analysis of the system is quite cumbersome and will not be repeated here. However, from a qualitative point of view, the basic principle of PLL operation can be briefly explained as follows: With no signal input applied to the system, the error voltage V_d is equal to zero. The VCO operates at a set frequency ω_o, which is known as the free-running frequency. If an output signal is applied to the system. the phase comparator compares the phase and the frequency of the input with the VCO frequency and generates an error voltage $V_e(t)$ that is related to the phase and the frequency difference between the two signals. This error voltage is then filtered, amplified and applied to the control terminal of the VCO. In this manner, the control voltage $V_d(t)$ forces the VCO fre-

quency to vary in a direction that reduces the frequency difference between f_o and the input signal. If the input frequency ω_i is sufficiently close to ω_o, the feedback nature of the PLL causes the VCO to synchronize or lock with the incoming signal. Once in lock, the VCO frequency is identical to the input signal except for a finite phase difference. This net phase difference θ_o is necessary to generate the corrective error voltage V_d to shift the VCO frequency from its free-running value to the input signal frequency ω_i and, thus, keep the PLL in lock. This self-correcting ability of the system also allows the PLL to track the frequency changes of the input signal once it is locked. The range of frequencies over which the PLL can maintain lock with an input signal is defined as the "lock range" of the system. The band of frequencies over which the PLL can acquire lock with an incoming signal is known as the "capture range" of the system and is never greater than the "lock range."

Another means of describing the operation of the PLL is to observe that the phase comparator is in actuality a multipler circuit that mixes the input signal with the VCO signal. This mix produces the sum and difference frequencies $\omega_i \pm \omega_o$ shown in Figure 9-1. When the loop is in lock, the VCO duplicates the input frequency so that the difference frequency component $(\omega_i - \omega_o)$ is zero; hence, the output of the phase comparator contains a dc component. The low pass filter removes the sum frequency component $(\omega_i = \omega_o)$ but passes the dc component which is then amplified and fed back to the VCO. Notice that when the loop is in lock, the difference frequency component is always dc, so the lock range is independent of the band edge of the low pass filter.

Lock and Capture

Consider now the case where the loop is not yet in lock. The phase comparator again mixes the input and VCO signals to produce sum and difference frequency components. Now, however, the difference component may fall outside the band edge of the low pass filter and be removed along with the sum frequency component. If this is the case, no information is transmitted around the loop and the VCO remains at its initial free-running frequency. As the input frequency approaches that of VCO, the frequency of the difference component decreases and approaches the band edge of the low pass filter. Now some of the difference component is passed, which tends to drive the VCO towards the frequency of the input signal. This, in turn, decreases the frequency of the difference component and allows more information to be transmitted through the low pass filter to the VCO. This is essentially a positive feedback mechanism which causes the VCO to snap into lock with the input signal. With this mechanism in mind, the term "capture range" can again be defined as *the frequency range centered about the VCO initial free-running frequency over which the loop can acquire lock with the input signal.* The capture range is a measure of how close the input signal must be in frequency to that of the VCO to acquire lock. The "capture range" can assume any value within the lock range and depends primarily upon the band edge of the low pass filter together with the closed loop gain of the system. It is this signal capturing phenomenon which gives the loop its frequency selective properties.

It is important to distinguish the "capture range" from the "lock range" which can, again, be defined as *the frequency range usually centered about the VCO initial free running frequency over which the loop can track the input signal once lock has been achieved.*

When the loop is in lock, the difference frequency component on the output of the phase comparator (error voltage) is dc and will always be passed by the low pass filter. Thus, the lock range is limited by the range of error voltage that can be generated and the corresponding VCO frequency deviation produced. The lock range is essentially a dc parameter and is not affected by the band edge of the low pass filter.

The Capture Transient

The capture process is highly complex and does not lend itself to simple mathematical analysis. However, a qualitative description of the capture mechanism may be given as follows: Since frequency is the time derivative of phase, the frequency and the phase errors in the loop can be related as

$$\Delta\omega = \frac{d\theta_o}{dt} \qquad \text{(Equation 9-1)}$$

where $\Delta\omega$ is the instantaneous frequency separation between the signal and VCO frequencies and θ_o is the phase difference between the input signal and VCO signals.

If the feedback loop of the PLL was opened, say between the low pass filter and the VCO control input, then for a given condition of ω_o and ω_i the phase comparator output would be a sinusoidal beat note at a fixed frequency $\Delta\omega$. If ω_i and ω_o were sufficiently close in frequency, this beat note would appear at the filter output with negligible attenuation. Now suppose that the feedback loop is closed by connecting the low pass filter output to the VCO control terminal. The VCO frequency will be modulated by the beat note. When this happens, $\Delta\omega$ itself will become a function of time. If during this modulation process, the VCO frequency moves closer to ω_i (i.e., decreasing $\Delta\omega$), then $d\theta_o/d_t$ decreases and the output of the phase comparator becomes a slowly varying function of time. Similarly, if the VCO is modulated away from ω_i, $d\theta/d_t$ increases and the error voltage becomes a rapidly varying function of time. Under this condition the beat note waveform no longer looks sinusoidal; it looks like a series of aperiodic cusps, depicted schematically in Figure 9-2a. Because of its asymmetry, the beat note waveform contains a finite dc component that pushes the average value of the VCO toward ω_i, thus increasing $\Delta\omega$. In this manner, the beat note frequency rapidly decreases toward zero, the VCO frequency drifts toward ω_i and the lock is established. When the system is in lock, $\Delta\omega$ is equal to zero and only a steady-state dc error voltage remains.

Figure 9-2b displays an oscillogram of the loop error voltage V_d in an actual PLL system during the capture process. Note that as lock is approached, $\Delta\omega$ is reduced, the low pass filter attenuation becomes less and the amplitude of the beat note increases.

The total time taken by the PLL to establish lock is called the pull-in time. Pull-in time depends on the initial frequency and phase differences between the two signals as well as on the overall loop gain and the low pass filter bandwidth. Under certain conditions, the pull-in time may be shorter than the period of the beat note and the loop can lock without an oscillatory error transient.

A specific case to illustrate this is shown in Figure 9-3. The 565 PLL is shown acquiring lock within the first cycle of the input signal. The PLL was able to capture in this short time because it was operated as a first order loop (no low pass filter) and the input tone-burst frequency was within its lock and capture range.

Effect of the Low Pass Filter

In the operation of the loop, the loop pass filter serves a dual function: First, by attenuating the high frequency error components at the output of the phase comparator, it enhances the inteference-rejection characteristics; second, it provides a short-term memory for the PLL and ensures a rapid recapture of the signal if the system is thrown out of lock due to a noise transient. The low pass filter bandwidth has the following effects on system performance:

ASYNCHRONOUS ERROR BEAT FREQUENCY DURING THE CAPTURE PROCESS

Figure 9-2a

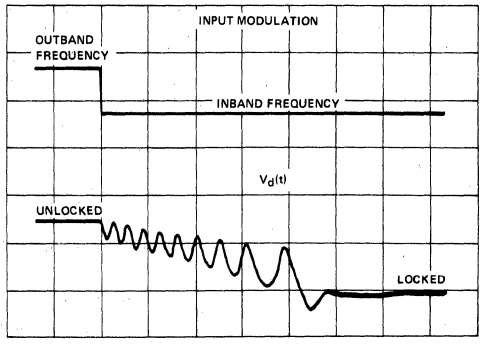


Figure 9-2b

FAST CAPTURE EXHIBITED BY FIRST ORDER LOOP

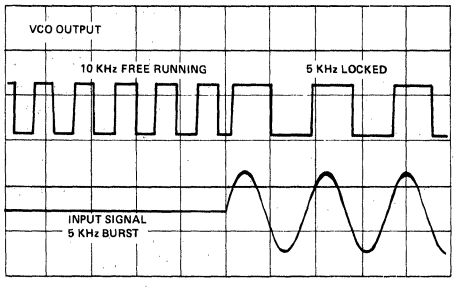


Figure 9-3

LINEARIZED MODEL OF THE PLL AS A NEGATIVE FEEDBACK SYSTEM

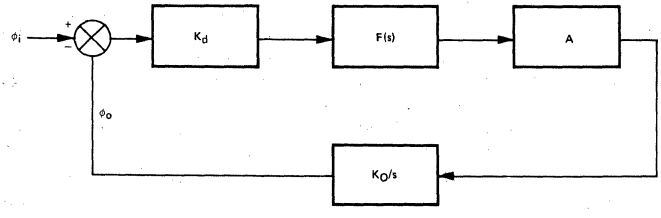


Figure 9-4

a. The capture process becomes slower, and the pull-in time increases.
b. The capture range decreases.
c. Interference-rejection properties of the PLL improve since the error voltage caused by an interfering frequency is attenuated further by the low pass filter.
d. The transient responce of the loop (the response of the PLL to sudden changes of the input frequency within the capture range) becomes undamped.

The last effect also produces a practical limitation on the low pass loop filter bandwidth and roll-off characteristics from a stability standpoint. These points will be explained further in the following analysis.

Linear Analysis for Lock Condition—Frequency Tracking

When the PLL is in lock, the non-linear capture transients are no longer present. Therefore, under lock condition, the PLL can often be approximated as a linear control system (see Figure 9-4) and can be analyzed using Laplace transform techniques. In this case, it is convenient to use the net phase error in the loop ($\theta_s - \theta_o$) as the system variable. Each of the gain terms associated with the blocks can be defined as follows:

K_d = conversion gain of phase detector (volt/rad)

F(s) = transfer characteristic of low pass filter

A = amplifier voltage gain

$K\theta$ = VCO conversion gain (rad/sec/volt)

Note that, since the VCO converts a voltage to a frequency and since phase is the integral of frequency, the VCO functions as an integrator in the feedback loop.

The open loop transfer function for the PLL can be written as

(Equation 9-2)

$$T(s) = \frac{K_V F(s)}{s}$$

where K_V is the total loop gain, i.e., $K_V = K_O K_d A$. Using the linear feedback analysis techniques, the closed loop transfer characteristics H(s) can be related to the open loop performance as

(Equation 9-3)

$$H(s) = \frac{T(s)}{1 + T(s)}$$

and the roots of the characteristic system polynomial can be readily determined by root locus techniques.

From these equations, it is apparent that the transient performance and frequency re-

sponse of the loop is heavily dependent upon the choice of filter and its corresponding transfer characteristic, F(s).

The simplest case is that of the first order loop where F(s) = 1 (no filter). The closed loop transfer function then becomes

(Equation 9-4)

$$T(s) = \frac{K_V}{s + K_V}$$

This transfer function gives the root locus as a function of the total loop gain K_V and the corresponding frequency response shown in Figure 9-5a. The open loop pole at the origin is due to the integrating action of the VCO. Note that the frequency response is actually the amplitude of the difference frequency component versus modulating frequency when the PLL is used to track a frequency modulated input signal. Since there is no low pass filter in this case, sum frequency components are also present on the phase detector output and must be filtered outside of the loop if the difference frequency component (demodulated FM) is to be measured.

With the addition of a single pole low pass filter F(s) of the form

(Equation 9-5)

$$F(s) = \frac{1}{1 + \tau_1 s}$$

where $\tau_1 = R1C$, the PLL becomes a second order system with the root locus shown in Figure 9-5b. Here, we again have an open loop pole at the origin because of the integrating action of the VCO and another open loop pole at a position equal to $-1/\tau_1$ where τ_1 is the time constant of the low pass filter.

One can make the following observations from the root locus characteristics of Figure 9-5b.

a. As the loop gain K_V increases for a given choice of τ_1, the imaginary part of the closed loop poles increase; thus, the natural frequency of the loop increases and the loop becomes more and more undamped.
b. If the filter time constant is increased, the real part of the closed loop poles becomes smaller and the damping is reduced.

As in any practical feedback system, excess shifts or non-dominant poles associated with the blocks within the PLL can cause the root loci to bend toward the right half plane as shown by the dashed line in Figure 9-5b. This is likely to happen if either the loop gain or the filter time constant is too large and may cause the loop to break into sustained oscillations.

ROOT LOCUS AND FREQUENCY RESPONSE PLOTS OF FIRST AND SECOND ORDER LOOPS

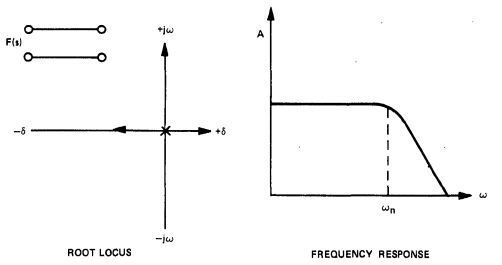


Figure 9-5a

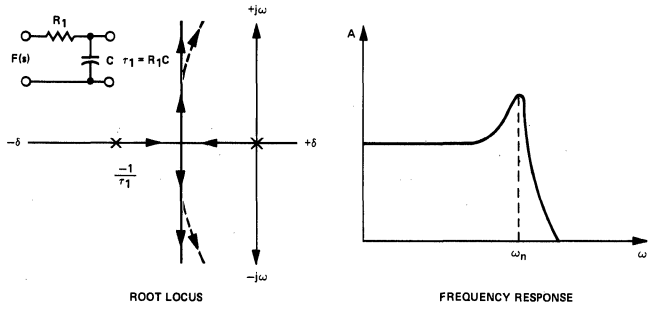


Figure 9-5b

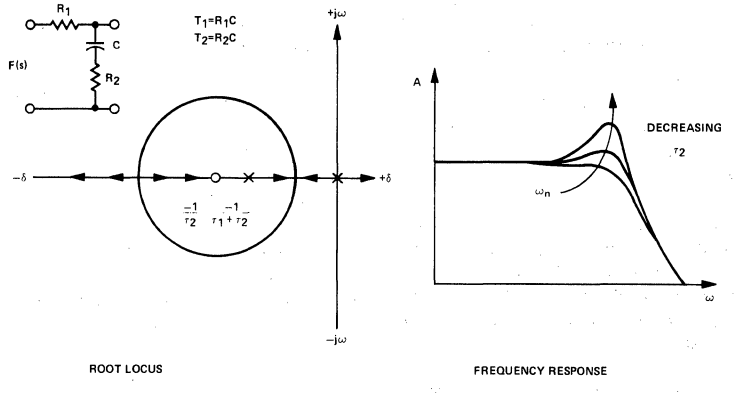


Figure 9-5c

The stability problem can be eliminated by using a lag-lead type of filter, as indicated in Figure 9-5c. This type of filter has a transfer function

(Equation 9-6)

$$F(s) = \frac{1 + \tau_2 s}{1 + (\tau_1 + \tau_2)s}$$

where $\tau_2 = R2C$ and $\tau_1 = R1C$. By the proper choice of R2, this type of filter confines the root locus to the left half plane and ensures stability. The lag-lead filter gives a frequency response dependent on the damping, which can now be controlled by the proper adjustment of τ_1 and τ_2. In practice, this type of filter is important because it allows the loop to be used with a response between that of the first and second order loops and it provides an additional control over the loop transient response. If R2 = 0, the loop

behaves as a second order loop and if R2 = ∞, the loop behaves as a first order loop due to a pole-zero cancellation. Note, however, that as first order operation is approached, the noise bandwidth increases and interference rejection decreases since the high frequency error components in the loop are now attenuated to a lesser degree.

In terms of the basic gain expressions in the system, the lock range of the PLL ω_L can be shown to be numerically equal to the dc loop gain

(Equation 9-7)

$$2\omega_L = 4\pi f_L = 2K_v$$

Since the capture range ω_C denotes a transient condition, it is not as readily derived as the lock range. However, an approximate expression for the capture range can be written as

(Equation 9-8)

$$2\omega_C = 4\pi f_C \simeq 2K_v \bullet F(j\omega_C)$$

where $F(j\omega_C)$ is the low pass filter amplitude response at $\omega = \omega_L$. Note that at all times the capture range is smaller than the lock range. If the simple lag filter of Figure 9-5b is used, the capture range equation can be approximated as

(Equation 9-9)

$$2\omega_C \simeq 2\sqrt{\frac{\omega_L}{\tau_1}}\sqrt{\frac{K_v}{\tau_1}}$$

Thus, the capture range increased as the low pass filter time constant is decreased, whereas the lock range is unaffected by the filter and is determined solely by the loop gain.

Figure 9-6 shows the typical frequency-to-voltage transfer characterisitcs of the PLL. The input is assumed to be a sine wave whose frequency is swept slowly over a broad frequency range. The vertical scale is the corresponding loop error voltage. In Figure 9-6a, the input frequency is being gradually increased. The loop does not respond to the signal until it reaches frequency ω_1, corresponding to the lower edge of the capture range. Then, the loop suddenly locks on the input and causes a negative jump of the loop error voltage. Next, V_d varies with frequency with a slope equal to the reciprocal of VCO gain ($1/K_o$) and goes through zero as $\omega_i = \omega_o$. The loop tracks the input until the input frequency reaches ω_2, corresponding to the upper edge of the lock range. The PLL then loses lock and the error voltage drops to zero. If the input frequency is swept slowly back now, the cycle repeats itself, but it is inverted, as shown in Figure 9-6b. The loop recaptures the signal at ω_3 and tracks it down to ω_4. The total capture and lock ranges of the system are:

TYPICAL PLL FREQUENCY- TO-VOLTAGE TRANSFER CHARACTERISTICS FOR INPUT FREQUENCY INCREASING AND DECREASING

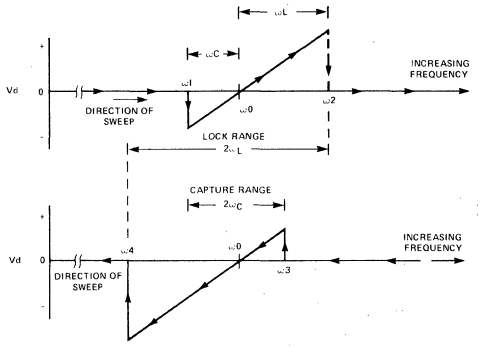


Figure 9-6

(Equation 9-10)

$$2\omega_C = \omega_3 - \omega_1 \text{ and } 2\omega_L = \omega_2 - \omega_4$$

Note that, as indicated by the transfer characteristics of Figure 9-6, the PLL system has an inherent selectivity about the center frequency set by the VCO free-running frequency ω_o. It will respond only to the input signal frequencies that are separated from ω_o by less than ω_C or ω_L, depending on whether the loop starts with or without an initial lock condition. The linearity of the frequency-to-voltage conversion characteristics for the PLL is determined solely by the VCO conversion gain. Therefore, in most PLL applications, the VCO is required to have a highly linear voltage-to-frequency transfer characteristic.

PHASE LOCKED LOOP BUILDING BLOCKS

Voltage Controlled Oscillator

Since three different forms of VCO have been used in the Signetics PLL series, the VCO details will not be discussed until the individual loops are described. However, a few general comments about VCOs are in order.

When the PLL is locked to a signal, the VCO voltage is a function of the frequency of the input signal. Since the VCO control voltage is the demodulated output during FM demodulation, it is important that the VCO voltage-to-frequency characteristic be linear so that the output is not distorted. Over the linear range of the VCO, the conversion gain is given by K_o (in radian/sec/volt).

(Equation 9-11)

$$K_o = \frac{\Delta\omega_o}{\Delta V_o}$$

Since the output voltage is the VCO voltage, we can get the loop output voltage as

(Equation 9-12)

$$\Delta V_o = \frac{\Delta\omega_o}{K_o}$$

The gain K_o can be found from the data sheet by taking the change in VCO control voltage for a given percentage frequency deviation and multiplying by the center frequency. When the VCO voltage is changed, the frequency change is virtually instantaneous.

Phase Detector

All Signetics phase locked loops use the same form of phase detector—often called the doubly-balanced multiplier or mixer. Such a circuit is shown in Figure 9-7.

The input stage formed by transistors Q1 and Q2 may be viewed as a differential amplifier which has a collector resistance R_c and whose differential gain at balance is the ratio of R_c to the emitter resistance r_e of Q1 and Q2.

(Equation 9-13)

$$A_d = \frac{R_C}{r_e} = \frac{R_C}{\frac{0.026}{I_e/2}} = \frac{R_C}{0.0131_e}$$

The switching stage formed by Q3 - Q6 is switched on and off by the VCO square wave. Since the collector current swing of Q2 is the negative of the collector current swing of Q1, the switching action has the effect of multiplying the differential stage output first by +1 and then by -1. That is, when the base of Q4 is positive, R_{C2} receives I1 and when the base of Q6 is positive, R_{C2} receives I2 = I1. Since we have called this a multiplier, let us perform the multiplication to gain further insight into the action of the phase detector.

Suppose we have an input signal which consists of two added components: a component at frequency ω_i which is close to the free-running frequency and a component at frequency ω_k which may be at any frequency. The input signal is

(Equation 9-14)

$$V_i + V_k = V_i \sin(\omega_i t + \theta_i) + V_k \sin(\omega_k t + \theta_k)$$

where θ_i and θ_k are the phase in relation to the VCO signal. The unity square wave developed in the multiplier by the VCO signal is

(Equation 9-15)

$$\frac{4}{\pi(2n+1)} \sin\left[(2n+1)\omega_o t\right]$$

where ω_o is the VCO frequency. Multiplying the two terms, using the appropriate trigonometric relationship and inserting the differential stage gain A_d, we get

(Equation 9-16)

$$V_d = \frac{2A_d}{\pi}\left[\sum_{n=0}^{\infty}\frac{V_i}{(2n+1)}\cos\left[(2n+1)\omega_o t - \omega_i t - \theta_i\right]\right.$$
$$-\sum_{n=0}^{\infty}\frac{V_i}{(2n+1)}\cos\left[(2n+1)\omega_o t + \omega_i t + \theta_i\right]$$
$$+\sum_{n=0}^{\infty}\frac{V_k}{(2n+1)}\cos\left[(2n+1)\omega_o t - \omega_k t - \theta_k\right]$$
$$\left.-\sum_{n=0}^{\infty}\frac{V_k}{(2n+1)}\cos\left[(2n+1)\omega_o t + \omega_k t + \theta_k\right]\right]$$

Assuming the V_k is zero, temporarily, if ω_i is close to ω_o, the first term (n = 0) has a low frequency difference frequency component. This is the beat frequency component that feeds around the loop and causes lock up by modulating the VCO. As ω_o is driven closer to ω_i, this difference component becomes lower and lower in frequency until $\omega_o = \omega_i$ and lock is achieved. The first term then becomes

(Equation 9-17)

$$\frac{2A_d V_i}{\pi}\cos\theta_i$$

which is the usual phase detector formula showing the dc component of the phase detector during lock. This component must equal the voltage necessary to keep the VCO at ω_o. it is possible for ω_o to equal ω_i momentarily during the lock up process and, yet, for the phase to be incorrect so that ω_o passes through ω_i without the lock being achieved. This explains why lock is usually not achieved instantaneously, even when $\omega_i = \omega_o$ at t = 0.

INTEGRATED PHASE DETECTOR

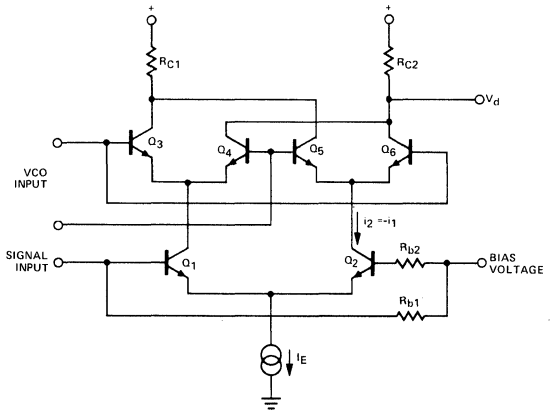


Figure 9-7

If $n \neq 0$ in the first term, the loop can lock when $\omega_i = (2n+1)\omega_o$, giving the dc phase detector component

(Equation 9-18)

$$\frac{2A_d V_i}{\pi(2n+1)}\cos\theta_i$$

showing that the loop can lock odd harmonics of the center frequency. The (2n + 1) term in the denominator shows that the phase detector output is lower for harmonic lock, which explains why the lock range decreases as higher and higher odd harmonics are used to achieve lock.

Note also that the phase detector during lock is (assuming A_d is constant) also a function of the input amplitude V_i. Thus, for a given dc phase detector output V_d, an input amplitude decrease must be accompanied by a phase change. Since the loop can remain locked only for θ_i between 0 and 180°, the lower V_i becomes, the more reduced is the lock range.

Going to the second term, we note that during lock the lowest possible frequency is $\omega_o + \omega_i = 2\omega_i$. A sum frequency component is always present at the phase detector output. This component is usually greatly attenuated by the low pass filter capacitor connected to the phase detector output. However, when rapid tracking is required (as with high-speed FM detection or FSK-frequency shift keying), the requirement for a relatively high frequency cutoff in the low pass filter may leave this component unattenuated to the extent that it interferes with detection. At the very least, additional filtering may be required to remove this component. Components caused by $n \neq 0$ in the second term are both attenuated and of much higher frequency, so they may be neglected.

Suppose that we have other frequencies represented by V_k present. What is their effect for $V_k \neq 0$?

The third term shows that V_k introduces another difference frequency component. Obviously, if ω_k is close to ω_i, it can interfere with the locking process since it may form a beat frequency of the same magnitude as the desired locking beat frequency. Suppose lock has been achieved, however, so that $\omega_o = \omega_i$. In order for lock to be maintained, the average phase detector output must be constant. If $\omega_o = \omega_k$ is relatively low in frequency, the phase θ_i must change to compensate for this beat frequency. Broadly speaking, any signal in addition to the signal to which the loop is locked causes a phase variation. Usually this is negligible since ω_k is often far removed from ω_i. However, it has been stated that the phase θ_i can move only between 0 and 180°. Suppose the phase limit has been reached and V_k appears. Since it cannot be compensated for, it will drive the loop out of lock. This explains why extraneous signals can result in a decrease in the lock range. If V_k is assumed to be an instantaneous noise component, the same effect occurs. When the full swing of the loop is being utilized, noise will decrease the lock or tracking range. We can reduce this effect by decreasing the cutoff frequency of the low pass filter so that the $\omega_o - \omega_k$ is attentuated to a greater extent, which illustrates that noise immunity and out-

band frequency rejection is improved (at the expense of capture range since $\omega_o - \omega_i$ is likewise attenuated) when the low pass filter capacitor is large.

The third term can have a dc component when ω_k is an odd harmonic of the locked frequency so that $(2n+1)(\omega_o - \omega_i)$ is zero and θ_k makes its appearance. This will have an effect on θ_i which will change the θ_i versus frequency ω_i. This is most noticeable when the waveform of the incoming signal is, for example, a square wave. The θ_k term will combine with the θ_i term so that the phase is a linear function of input frequency. Other waveforms will give different phase versus frequency functions. When the input amplitude V_i is large and the loop gain is large, the phase will be close to 90° throughout the range of VCO swing, so this effect is often unnoticed.

The fourth term is of little consequence except that if ω_k approaches zero, the phase detector output will have a component at the locked frequency ω_o at the output. For example, a dc offset at the input differential stage will appear as a square wave of fundamental ω_o at the phase detector output. This is usually small and well attenuated by the low pass filter. Since many out-band signals or noise components may be present, many V_k terms may be combining to influence locking and phase during lock. Fortunately, we need only worry about those close to the locked frequency.

The quadrature phase detector action is exactly the same except that its output is proportional to the sine of the phase angle. When the phase θ_i is 90°, the quadrature phase detector output is then at its maximum, which explains why it makes a useful lock or amplitude detector. The output of the quadrature phase detector is given by:

$$V_q = \frac{2A_qV_i}{\pi} \sin \theta_i \qquad \text{(Equation 9-19)}$$

where V_i is the constant or modulated AM signal and $\theta_i \approx 90°$ in most cases so that sine $\theta_i = 1$ and

$$V_q = \frac{2A_qV_i}{\pi} \qquad \text{(Equation 9-20)}$$

This is the demodulation principle of the autodyne receiver and the basis for the 567 tone decoder operation.

FUNCTIONAL APPLICATIONS

Low Pass Filter

The simplest type of low pass filter for the second order loop is a single pole RC type shown in Figure 9-5b. In all Signetics' loops, the resistor is internal and the capacitor is external. The inside resistor greatly improves the center frequency stability of the loop with temperature variations. Fortunately, the capture range and loop damping are related to the square root of this internal resistor value, so variations in its absolute value have little effect on loop performance. The nominal value of the internal resistor for each loop is given in the circuit diagrams of the detailed circuit descriptions in this chapter. The typical tolerance on these integrated resistors is ±20%.

As a functional building block, the phase locked loop is suitable for a wide variety of frequency related applications. These applications generally fall into one or more of the following categories:

a. FM demodulation
b. Frequency synthesizing
c. Frequency synchronization
d. Signal conditioning
e. AM demodulation

FM Demodulation

If the PLL is locked to a frequency modulated (FM) signal, the VCO tracks the instantaneous frequency of the input signal. The filtered error voltage, which forces the VCO to maintain lock with the input signal then becomes the demodulated FM output. The linearity of this demodulated signal depends solely on the linearity of the VCO control-voltage-to-frequency transfer characteristic.

It should be noted that since the PLL is in lock during the FM demodulation process, the response is linear and can be readily predicted from a root locus plot.

FM demodulation applications are numerous; however, some of the more popular are:

BROADCAST FM DETECTION

Here, the PLL can be used as a complete IF strip, limiter and FM detector which may be used for detecting either wide or narrow band FM signals with greater linearity than can be obtained by other means. For frequencies within the range of the VCO, the PLL functions as a self contained receiver since it combines the functions of frequency selectivity and demodulation. One increasingly popular use of the PLL is in scanning-receivers where a number of broadcast channels may be sequentially monitored by simply varying the VCO free-running frequency.

FM TELEMETRY

This application involves demodulation of a frequency modulated subcarrier of the main channel. A popular example here is the use of the PLL to recover the SCA (storecast music) signal from the combined signal of many commercial FM broadcast stations. The SCA signal is a 67kHz frequency modulated subcarrier which puts it above the frequency spectrum of the normal stereo or monaural FM program material. By connecting the circuit of Figure 9-8 to a point between the FM discriminator and the de-emphasis filter of a commercial band (home) FM receiver and tuning the receiver to a station which broadcasts an SCA signal, one can obtain hours of commercial free background music.

FREQUENCY SHIFT KEYING (FSK)

This refers to what is essentially digital frequency modulation. FSK is a means for transmitting digital information by a carrier which is shifted between two discrete frequencies. In this case, the two discrete frequencies correspond to a digital "1" and a digital "0," respectively. When the PLL is locked to a FSK signal, the demodulated output (error voltage) shifts between two discrete voltage levels, corresponding to the demodulated binary output. FSK techniques are often used in modems (modulator-demodulators), intended for transmitting data over telephone lines.

SCA DECODER

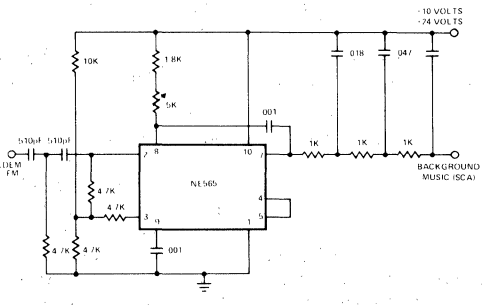


Figure 9-8

FREQUENCY SYNTHESIZER

Frequency Multiplication can be achieved with the PLL in two ways:

a. Locking to a harmonic of the input signal
b. Insertion of a counter (digital frequency divider) in the loop

Harmonic locking is the simplest and can usually be achieved by setting the VCO free-running frequency to a multiple of the input frequency and allowing the PLL to lock. A limitation on this scheme, however, is that the lock range decreases as successively higher and weaker harmonics are used for locking. This limits the practical harmonic locking range to multiples of approximately less than ten. For larger multiples, the second scheme is more desirable.

A block diagram of the second scheme is shown in Figure 9-9. Here, the loop is broken between the VCO and the phase comparator and a counter is inserted. In this case, the fundamental of the *divided* VCO frequency is locked to the input frequency so that the VCO is actually running at a multiple of the input frequency. The amount of multiplication is determined by the counter. An obvious practical application of this multiplication property, is the use of the PLL in wide range frequency synthesizers.

In frequency multiplication applications it is important to take into account that the phase comparator is actually a mixer and that its output contains sum and difference frequency components. The difference frequency component is dc and is the error voltage which drives the VCO to keep the PLL in lock. The sum frequency components (of which the fundamental is twice the frequency of the input signal) if not well filtered, will induce incidental FM on the VCO output. This occurs because the VCO is running at many times the frequency of the input signal and the sum frequency component which appears on the control voltage to the VCO causes a periodic variation of its frequency about the desired multiple. For frequency multiplication it is generally necessary to filter quite heavily to remove this sum frequency component. The tradeoff, of course, is a reduced capture range and a more underdamped loop transient response.

For the case of frequency fractionalization, both harmonic locking and frequency countdown could be used to generate, for instance, a frequency exactly 16/3 the input. In this case, the circuit of Figure 9-10 could be used with the initial VCO frequency set to approximately 16/3 the expected input frequency. The counter then divides the VCO frequency by 16, and the input is locked to the 3rd harmonic of the counter output. Now the output can be taken as the VCO output and it will be exactly 16/3 of the input frequency as long as the loop is in lock.

Frequency translation can be achieved by adding a mixer and a low pass filter stage to the basic PLL as shown in Figure 9-11. With this system the PLL can be used to translate the frequency of a highly stable but fixed-frequency reference oscillator by a small amount in frequency.

In this case, the reference input f_r and the VCO output f_o are applied to the inputs of

BLOCK DIAGRAM OF FREQUENCY SYNTHESIZER USING FREQUENCY DIVIDER

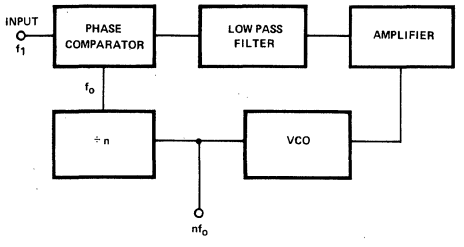


Figure 9-9

IMPLEMENTATION OF FREQUENCY SYNTHESIZER (565)

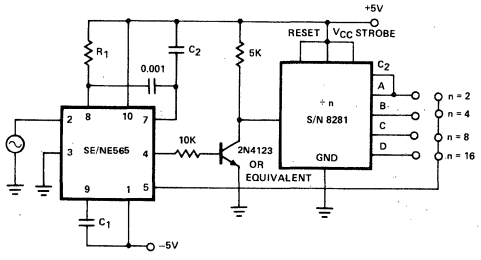


Figure 9-10

FREQUENCY TRANSLATION OR "OFFSET" LOOP

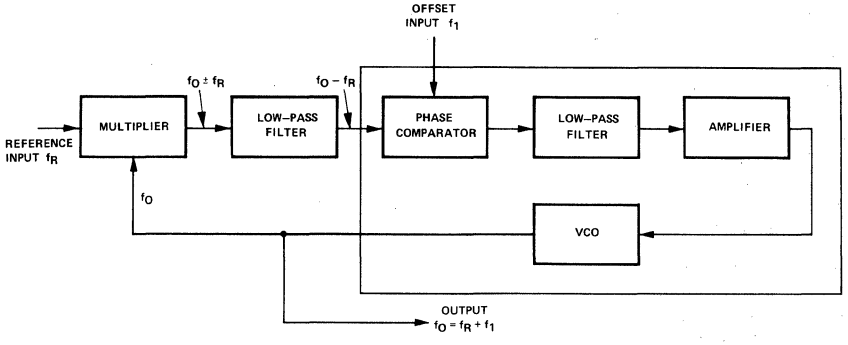


Figure 9-11

the mixer stage. The mixer output is made up of the sum and the difference components of f_r and f_o. The sum component is filtered by the first low pass filter. The translation or offset frequency f_1 is applied to the phase comparator along with the $f_r - f_o$ component of the mixer output. When the system is in lock, the two inputs of the phase comparator are at identical frequency, that is,

(Equation 9-21)

$$f_o - f_R = f_1 \text{ or } f_o = f_R + f_1$$

Frequency Synchronization

Using the phase locked loop system, the frequency of the less precise VCO can be phase locked with a low level but highly stable reference signal. Thus, the VCO output reproduces the reference signal frequency at the same per-unit accuracy, but at a much higher power level. In some applications, the synchronizing signal can be in the form of a low duty cycle burst at a specific frequency. Then, the PLL can be used to regenerate a coherent CW reference frequency locking onto this short synchronizing pulse. A typical example of such an application is seen in the phase locked chroma-reference generators of color television receivers.

In digital systems, the PLL can be used for a variety of synchronization functions. For example, two system clocks can be phase locked to each other such that one can function as a back up for the other; or PLLs can be used in synchronizing disk or tape drive mechanisms in information storage and retrieval systems. In pulse-code modulation (PCM) telemetry receivers or in repeater systems, the PLL is used for bit synchronization.

Other popular applications include locking to WWVB to generate an inexpensive laboratory frequency standard and synchronizing tape speed for playback of a tape recorded at an irregular speed.

Signal Conditioning

By proper choice of the VCO free-running frequency, the PLL can be made to lock to any one of a number of signals present at the input. Hence, the VCO output reproduces the frequency of the desired signal, while greatly attenuating the undesired frequencies of sidebands present at the input.

If the loop bandwidth is sufficiently narrow, the signal-to-noise ratio at the VCO output can be much better than that at the input. Thus, the PLL can be used as a noise filter for regenerating weak signals buried in noise.

AM Demodulation

AM demodulation may be achieved with PLL by the scheme shown in Figure 9-12. In this mode of operation, the PLL functions as a synchronous AM detector. The PLL locks on the carrier of the AM signal so that the VCO output has the same frequency as that of the carrier but no amplitude modulation. The demodulated AM is then obtained by multiplying the VCO signal with the modulated input signal and filtering the output to remove all but the difference frequency component. It may be recalled from the initial discussion that when the frequency of the input signal is identical to the free-running frequency of the VCO, the loop goes into lock with these signals 90° out of phase. If the input is now shifted 90° so that it is in phase with the VCO signal and the two signals are mixed in a second phase comparator, the average dc value (difference frequency component) of the phase comparator output will be directly proportional to the amplitude of the input signal.

The PLL still exhibits the same capture range phenomena discussed earlier so that the loop has an inherent high degree of selectivity centered about the free-running VCO frequency. Because this method is essentially a coherent detection technique which involves averaging of the two compared signals, it offers a higher degree of noise immunity than can be obtained with conventional peak-detector-type AM demodulators.

GENERAL LOOP SETUP AND TRADEOFFS

In a given application, maximum PLL effectiveness can be achieved if the user understands the tradeoffs which can be made. Generally speaking, the user is free to select the frequency, tracking or lock range, capture range and input amplitude.

Center Frequency Selection

Setting the center frequency is accomplished by selecting one or two external components. The center frequency is usually set in the center of the expected input frequency range. Since the loop's ability to capture is a function of the *difference* between the incoming and free-running frequencies, the band edges of the capture range are *always* an equal distance (in Hz) from the center frequency. Typically, the lock range is also centered about the free-running frequency. Occasionally, the center frequency is chosen to be offset from the incoming so that detection or tracking range is limited on one side. This permits rejection of an adjacent higher or lower frequency signal without paying the penalty for narrow band operation (reduced tracking speed).

All of Signetics' loops use a multiplier in which the input signal is multiplied by a unity square wave at the VCO frequency. The odd harmonics present in the square wave permit the loop to lock to input signals at these odd harmonics. Thus, the center frequency may be set to, say, 1/3 or 1/5 of the input signal. The tracking range, however, will be considerably reduced as the higher harmonics are utilized.

The foregoing phase detector discussion would suggest that the PLL cannot lock to subharmonics because the phase detector cannot produce a dc component if ω_i is less than ω_o.

The loop can lock to both odd harmonic and subharmonic signals in practice because such signals often contain harmonic components at f_o. For example, a square wave of fundamental $f_o/3$ will have a substantial component at f_o to which the loop can lock. Even a pure sine wave input signal can be used for harmonic locking if the PLL input stage is overdriven (the resultant internal limiting generates harmonic frequencies). Locking to even harmonics or subharmonics is the least satisfactory since the input or VCO signal must contain second harmonic distortion. If locking to even harmonics is desired, the duty cycle of the input and VCO signals must be shifted away from the sym-

COHERENT AMPLITUDE-MODULATION DETECTION USING A PHASE-LOCKED LOOP

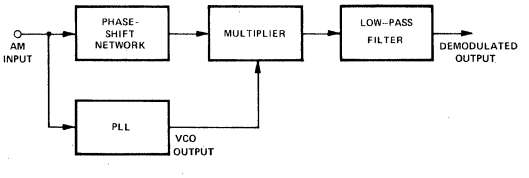


Figure 9-12

metrical to generate substantial even harmonic content.

In evaluating the loop for a potential application, it is best to actually compute the magnitude of the expected signal component nearest f_o. This magnitude can be used to estimate the capture and lock range.

All of Signetics' loops are stabilized against center frequency drift due to power supply variations. Both the 565 and the 567 are temperature compensated over the entire military temperature range (-55 to +125° C). To benefit from this inherent stability, however, the user must provide equally stable (or better) external components. For maximum cost effectiveness in some noncritical applications, the user may wish to trade some stability for lower cost external components.

Tracking or Lock Range Control

Two things limit the lock or tracking range. First, any VCO can only swing so far; if the input signal frequency goes beyond this limit, lock will be lost. Second, the voltage developed by the phase detector is proportional to the product of *both* the phase and the amplitude of the in-band component to which the loop is locked. If the signal amplitude decreases, the phase difference between the signal and the VCO must increase in order to maintain the same output voltage and, hence, the same frequency deviation. It often happens with low input amplitudes that even the full ±90° phase range of the phase detector cannot generate enough voltage to allow tracking wide deviations. When this occurs, the effective lock range is reduced. We must, therefore, give up some tracking capability and accept greater phase errors if the input signal is weak. Conversely, a strong input signal will allow us to use the entire VCO swing capability and keep the VCO phase (referred to the input signal) very close to 90° throughout the range. Note that tracking range does not depend on the low pass filter. However, if a low pass filter *is* in the loop, it will have the effect of limiting the maximum *rate* at which tracking can occur. Obviously, the LPF capacitor voltage cannot change instantly, so lock may be lost when large enough step changes occur. Between the constant frequency input and the step-change frequency input is some limiting frequency slew rate at which lock is just barely maintained. When tracking at this rate, the phase difference is at its limit of 0 or 180°. It can be seen that if the LPF cutoff frequency is low, the loop will be unable to track as fast as if the LPF cutoff frequency is higher. Thus, when maximum tracking rate is needed, the LPF should have a high cutoff frequency. However, a high cutoff frequency LPF will attenuate the sum frequencies to a lesser extent so that our output contains a significant and often bothersome signal at twice the input frequency. (Remember that the multiplier forms both the sum and difference frequencies. During lock, the difference frequency is zero, but the sum frequency of twice the locked frequency is still present.) This sum frequency component can then be filtered out with an external low pass filter.

Capture Range Control

There are two main reasons for making the low pass filter time constant large. First, a large time constant provides an increased memory effect in the loop so that it remains at or near the operating frequency during momentary fading or loss of signal. Second, the large time constant integrates the phase detector output so that increased immunity to noise and out-band signals is obtained.

Besides the lower tracking rates attendant to large loop filters, other penalties must be paid for the benefits gained. The capture range is reduced and the capture transient becomes longer. Reduction of capture range occurs because the loop must utilize the magnitude of the difference frequency component at the phase detector to drive the VCO towards the input frequency. If the LPF cutoff frequency is low, the difference component amplitude is reduced and the loop cannot swing as far. Thus, the capture range is reduced.

Choice of Input Level

Whenever amplitude limiting of the in-band signal occurs, whether in the loop input stages or prior to the input, the tracking (lock) and capture range becomes independent of signal amplitude.

Better noise and out-band signal immunity is achieved when the input levels are below the limiting threshold since the input stage is in its linear region and the creation of cross-modulation components is reduced. Higher input levels will allow somewhat faster operation due to greater phase detector gain and will result in a lock range which becomes constant with amplitude as the phase detector gain becomes constant. Also, high input levels will result in a linear phase versus frequency characteristic.

Lock-Up Time and Tracking Speed Control

In tracking applications, lock-up time is normally of little consequence, but occasions do arise when it is desirable to keep lock-up time short to minimize data loss when noise or extraneous signals drive the loop out of lock. Lock-up time is of great importance in tone decoder type applications. Tracking speed is important if the loop is used to demodulate an FM signal. Although the following discussion dwells largely on lock-up time, the same comments apply to tracking speed.

No simple expression is available which adequately describes the acquisition or lock-up time. This may be appreciated when we review the following factors which influence lock-up time.

a. Input phase
b. Low pass filter characteristic
c. Loop damping
d. Deviation of input frequency from center frequency
e. In-band input amplitude
f. Out-band signals and noise
g. Center frequency

Fortunately, it is usually sufficient to know how we can improve the lock-up time and what we must tradeoff to get faster lock-up. Suppose we have set up a loop or tone decoder and find that occasionally the lock-up transient is too long. What can be done to improve the situation—keeping in mind the factors that influence lock?

a. Initial phase relationship between incoming signal and VCO — This is the greatest single factor influencing the lock time. If the initial phase is wrong, it first drives the VCO frequency *away* from the input frequency so that the VCO frequency must walk back on the beat notes. Figure 9-13 gives a typical distribution of lock-up times with the input pulse initiated at random phase. The only way to overcome this variation is to send phase information all the time so that a favorable phase relationship is guaranteed at t = 0. For example, a number of PLLs or tone decoders may be weakly locked to low amplitude harmonics of pulse train and the transmitted tone phase-related to the same pulse train. Usually, however, the incoming phase cannot be controlled.
b. Low pass filter — The larger the low pass filter time constant, the longer will be the lock-up time. We can reduce lock-up time by decreasing the filter time constant, but in doing so, we sacrifice some of the noise immunity and out-band signal rejection which caused us to use a large filter in the first place. We must also accept a sum frequency (twice the VCO frequency) component at the low pass filter and greater phase jitter resulting from out-band signals and noise. In the case of the tone decoder (where control of the capture range is required since it specified the device bandwidth) a lower value of low pass capacitor automatically increases the bandwidth. We gain speed

only at the expense of added bandwidth.

c. Loop damping—Loop damping for a simple time constant low pass filter is:

(Equation 9-22)

$$\zeta = \frac{1}{2}\sqrt{\frac{1}{\tau k_V}}$$

Damping can be increased not only by reducing τ, as discussed above, but also by reducing the loop gain K_V. By using the loop gain reduction to control bandwidth or capture and lock range, we achieve better damping for narrow bandwidth operation. The penalty for this damping is that more phase detector output is required for a given deviation so that phase errors are greater and noise immunity is reduced. Also, more input drive may be required for a given deviation.

d. Input frequency deviation from free-running frequency—Naturally, the further an applied input signal is from the free-running frequency of the loop, the longer it will take the loop to reach that frequency due to the charging time of the low pass filter capacitor. Usually, however, the effect of this frequency deviation is small compared to the variation resulting from the initial phase uncertainty. Where loop damping is very low, however, it may be predominant.

e. In-band input amplitude—Since input amplitude is one factor in the phase detector gain K_d and since K_d is a factor in the loop gain K_v, damping is also a function of input amplitude. When the input amplitude is low, the lock-up time may be limited by the rate at which the low pass capacitor can charge with the reduced phase detector output (see d above).

f. Out-band signals and noise—Low levels of extraneous signals and noise have very little effect on the lock-up time, neither improving or degrading it. However, large levels may overdrive the loop input stage so that limiting occurs, at which point the in-band signal starts to be suppressed. The lower effective input level can cause the lock-up time to increase, as discussed in e above.

g. Center frequency—Since lock-up time can be described in terms of the number of cycles to lock, fastest lock-up is achieved at higher frequencies. Thus, whenever a system can be operated at a higher frequency, lock will typically take place faster. Also, in systems where different frequencies are being detected, the higher frequencies *on the average* will be detected before the lower frequencies. However, because of the wide variation due to initial phase, the reverse may be true for any single trial.

PLL MEASUREMENT TECHNIQUES

This section deals with user measurements of PLL operation. The techniques suggested are meant to help the user in evaluating the performance of his PLL during the initial setup period as well as to point out some pitfalls that may obscure loop evaluation. Recognizing that the user's test equipment may be limited, we have stressed the techniques which require a minimum of standard test items.

Center Frequency

Center frequency measurements are easily made by connecting a frequency counter or oscilloscope to the VCO output of the loop. The loop should be connected in its final configuration with the chosen values of input, bypass and low pass filter capacitors. No input signal should be present. As the center frequency is read out, it can be adjusted to the desired value by the adjustment means selected for the particular loop. It is important not to make the frequency measurement directly at the timing capacitor unless the capacity added by the measurement probe is much less than the timing capacitor value since the probe capacity will then cause a frequency error.

When the frequency measurement is to be converted to a dc voltage for production readout or automated testing, a calibrated phase locked loop can be used as a frequency meter (see Applications Section).

Capture and Lock Range

Figure 9-14a shows a typical measurement setup for capture and lock range measurements. The signal input from a variable frequency oscillator is swept linearly through the frequency range of interest and the loop FM output is displayed on a scope or (at lower frequencies) X-Y recorder. The sweep voltage is applied to the X axis.

Figure 9-14b shows the type of trace which results. The lock range (also called hold-in or tracking range) is given by the outer lines on the trace, which are formed as the incoming frequency sweeps *away* from the center frequency. The inner trace, formed as the frequency sweeps *toward* the center frequency, designates the capture range. Linearity of the VCO is revealed by the straightness of the trace portion within the lock range. The slope ($\Delta f/\Delta V$) is the gain or conversion factor for the VCO.

By using the sweep technique, the effect on center frequency, capture range and lock range of the input amplitude, supply voltage, low pass filter and temperature can be examined.

Because of the lock-up time duration and variation, the sweep frequency must be very much lower than the center frequency, especially when the capture range is below 10% of center frequency. Otherwise, the *apparent* capture and lock range will be a function of sweep frequency. It is best to start sweeping as slow as possible and, if desired, increase the rate until capture range begins to show an apparent reduction—indicating that the sweep is too fast. Typical sweep frequencies are in the range of 1/1000 to 1/100,000 of the center frequency. In the case of the 561 and 567, the quadrature detector output may be similarly displayed on the Y axis, as shown in Figure 9-15, showing the output level

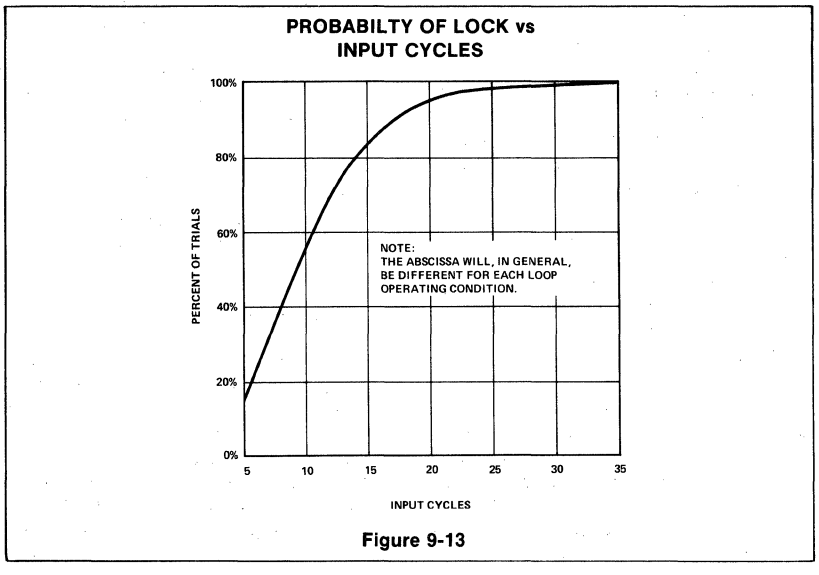


Figure 9-13

CAPTURE AND LOCK RANGE MEASUREMENT SETUP

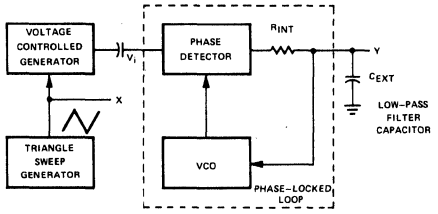


Figure 9-14a

CAPTURE AND LOCK RANGE OSCILLOGRAM

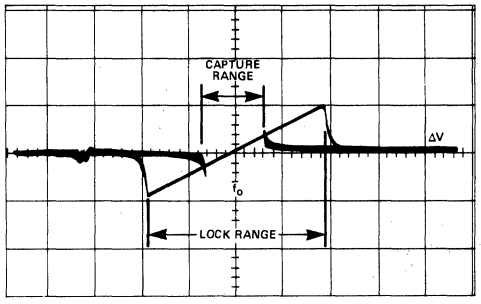


Figure 9-14b

versus frequency for one value of input amplitude.

Capture and lock range measurements may also be made by sweeping the generator manually through the band of interest. Sweeping must be done very slowly as the edges of the capture range are approached (sweeping toward center frequency) or the lock-up transient delay will cause an error in reading the band edge. Frequency should be read from the generator rather than the loop VCO because the VCO frequency gyrates wildly around the center frequency just before and after lock. Lock and unlock can be readily detected by simultaneously monitoring the input and VCO signals, the dc voltage at the low pass filter or the ac beat frequency components at the low pass filter. The latter are greatly reduced during lock as opposed to frequencies just outside of lock.

PHASE DETECTOR OUTPUTS vs FREQUENCY

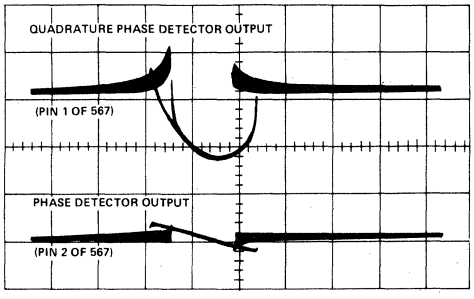


Figure 9-15

FM and AM Demodulation Distortion

These measurements are quite straightforward. The loop is simply setup for FM or AM (561 or 567) detection and the test signal is applied to the input. A spectrum analyzer or distortion analyzer (HP 333A) can be used to measure distortion at the FM or AM output.

For FM demodulation, the input signal amplitude must be large enough so that lock is not lost at the frequency extremes. The data sheets give the lock (or tracking) range as a function of input signal and the optional range control adjustments. Due to the inherent linearity of the VCOs, it makes little difference whether the FM carrier is at the free-running frequency or offset slightly as long as the tracking range limits are not exceeded.

The faster the FM modulation in relation to the center frequency, the lower the value of the capacitor in the low pass filter must be for satisfactory tracking. As this value decreases, however, it attentuates the sum frequency component of the phase detector output less. The demodulated signal will appear to have greater distortion unless this component is filtered out before the distortion is measured. The same comment applies to the measurement of AM distortion on the 561.

When AM distortion is being measured, the carrier frequency offset becomes more important. The lowest absolute value of carrier voltage at the modulation valleys must be high enough to maintain lock at the frequency deviation present. Otherwise, lock will periodically be lost and the distortion will be unreasonable. For example, the typical tracking range as a function of input signal graph in the 561 data sheet gives a total 3% tracking range at 0.3mVrms input. Thus, for a carrier deviation of 1.5%, the carrier must not drop below 0.3Vrms in the modulation valleys. Naturally, the AM amplitude must not be too high or the AM information will be suppressed.

Natural Frequency (ω_n)

Expressions for the natural frequency in terms of the loop gains and filter parameters are given in Table 9-2.

Expressions for ω_n and ζ in Second Order Loop

The natural frequency (ω_n) of a loop in its final circuit configuration can be measured by applying a frequency modulated signal of the desired amplitude to the loop (Table 9-2 shows that the natural frequency is a function of K_d, in turn a function of input amplitude). As the modulation frequency (ω_m) is increased, the phase relationship between the modulation and recovered sine wave will go through 90° at $S_m = \omega_n$ and the output amplitude will peak.

Damping (ζ)

As shown in Table 9-2 in the discussion on low pass filter, damping is a function of K_o, K_d and the low pass filter. Since K_o and k_d are

functions of center frequency and input amplitude, respectively, damping is highly dependent on the particular operating condition of the loop. Damping estimates for the desired operating condition can be made by applying an input signal which is frequency modulated within the lock range by a square wave. The low pass filter voltage is then monitored on an oscilloscope which is synchronized to the modulating waveform, as shown in Figure 9-16. Figure 9-17 shows typical waveforms displayed. The loop damping can be estimated by comparing the number and magnitude of the overshoots with the graph of Figure 9-18, which gives the transient phase error due to a step in input frequency.

Another way of estimating damping is to make use of the frequency response plot measured for the natural frequency (ω_n) measurement. For low damping constants, the frequency response measurement peak will be a strong function of damping. For high damping constants, the 3dB-down point will give the damping. Table 9-3 gives the approximate relationship.

EXPRESSIONS FOR ω_n and ζ IN SECOND ORDER LOOP

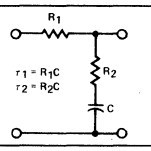
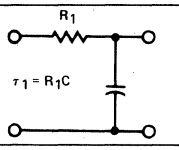
LOOP FILTER TYPE	
	
NATURAL FREQUENCY ω_n	
$\sqrt{\frac{K_o K_d}{\tau_1 + \tau_2}}$	$\sqrt{\frac{K_o K_d}{\tau_1}}$
DAMPING ζ	
$1/2\ \omega_n\ (\tau_2 + \frac{1}{K_o K_d})$	$\frac{\omega_n}{2K_o K_d}$

Table 9-2

MEASUREMENT SETUP FOR DISPLAY OF LOOP TRANSIENT RESPONSE

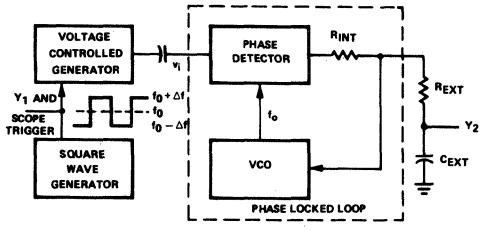
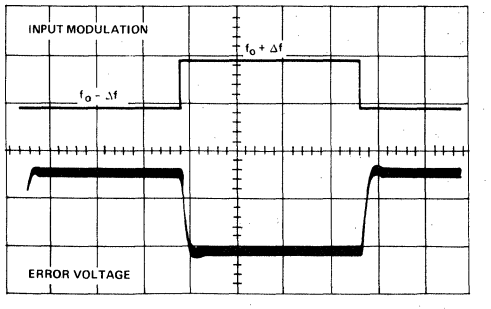


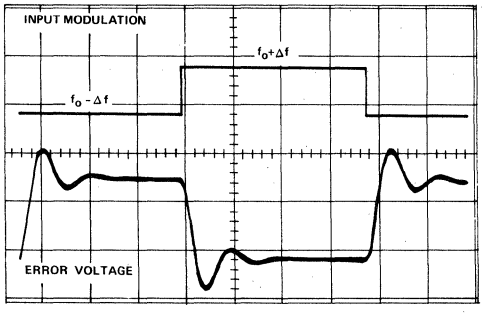
Figure 9-16

CRITICALLY DAMPED $\zeta \approx 1$



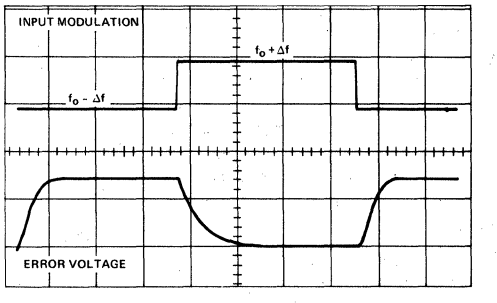
[$C_{ext} = C_{crit}, R_{ext} = 0$] **Figure 9-17b**

UNDERDAMPED $\zeta \approx .5$



[$C_{ext} > C_{crit}, R_{ext} = 0$] **Figure 9-17a**

OVERDAMPED $\zeta \approx 10$



[$C_{ext} < C_{crit}, R_{ext} > 0$] **Figure 9-17c**

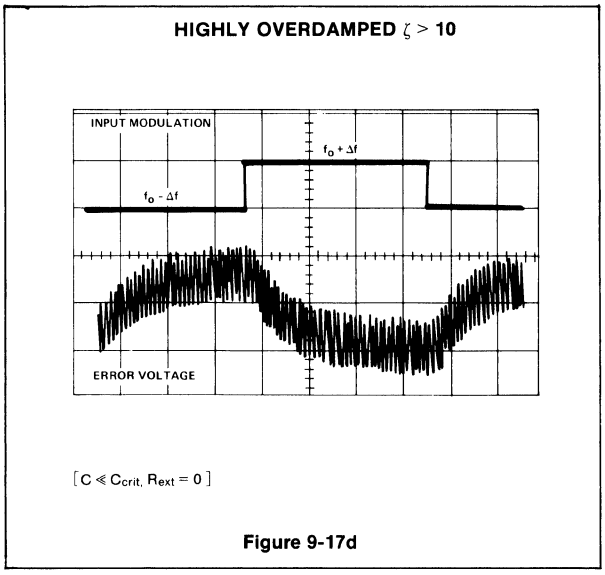


Figure 9-17d

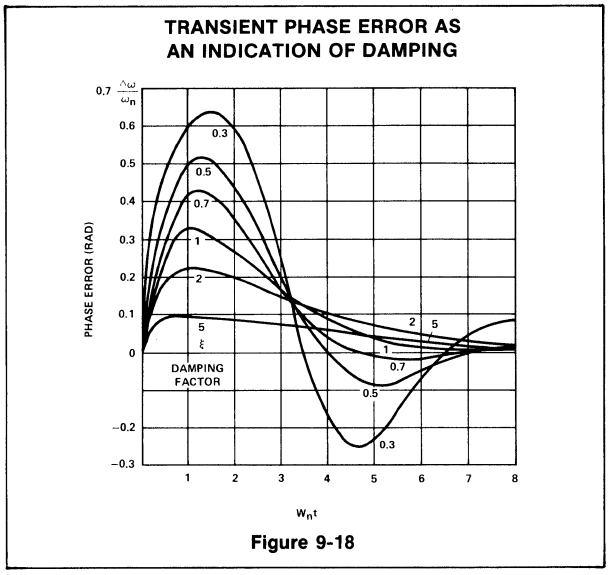


Figure 9-18

ESTIMATING DAMPING FROM MODULATING FREQUENCY (ω_m) RESPONSE

ζ	PEAK AMPLITUDE / LOW FREQUENCY AMPLITUDE	ω − 3dB / ωn
.3	6.0dB	1.8
.5	3.2dB	2.1
.7	2.2dB	2.5
1.0	1.3dB	4.3
5.0	.5dB	10

Table 9-3

Noise Effects

The effect of input noise on loop operation is very difficult to predict. Briefly, the input noise components near the center frequency are converted to phase noise. When the phase noise becomes so great that the ±90° permissible phase variation is exceeded, the loop drops out of lock or fails to acquire lock. The best technique is to actually apply the anticipated noise amplitude and bandwidth to the input and then perform the capture and lock range measurements as well as perform operating tests with the anticipated input level and modulation deviations. By including a small safety factor in the loop design to compensate for small processing variations, satisfactory operation can be assured.

Simplified Measurement Equipment

The majority of the PLL tests described can be done with a signal generator, a scope and a frequency counter. Most laboratories have these. A low-cost digital voltmeter will facilitate accurate measurement of the VCO conversion gain. Where the need for a FM generator arises, it may be met in most cases by the VCO of a Signetics PLL. (See the applications in this section.) Any of the loops may be set up to operate as a VCO by simply applying the modulating voltage to the low pass filter terminal(s). The resulting generator may be checked for linearity by using the counter to check frequency as a function of modulating voltage. Since the VCOs may be modulated right down to dc, the calibration may be done in steps. Moreover, Gardner* shows how loop measurements may be made by applying a *constant* frequency to the loop input and the modulating signal to the low pass filter terminal to simulate the effect of a FM input so that a FM generator may be omitted for many measurements.

*See references

SIGNETICS MONOLITHIC PHASE LOCKED LOOPS

Detailed Description of 560N, 561N and 562N, 564N

The 560N, 561N and 562N phase locked loops are all derived from the same monolithic die with different metal interconnections. Each device contains the same VCO, phase detector and voltage regulator stage and, hence, the basic loop parameters are the same for all three circuits.

The 560N is the most fundamental of the three circuits, having a block diagram equivalent to that shown in Figure 9-1. The actual circuit diagram is shown in Figure 9-19.

The VCO is a high frequency emitter-coupled multivibrator formed by transistors Q11-Q14. It operates from a regulated 7.7V supply formed by 6.3V supply formed by Zener diode CR1 (a reverse-biased base-emitter junction) in series with the 14V regulated supply. The VCO frequency is thus immune from supply voltages variations. Four constant current sources formed by Q20, Q21, Q23, Q24, and biased by CR6 and CR7, supply operating current for the VCO. Voltage control of the frequency is achieved by a differential amplifier, Q22 and Q25. As the base voltage of Q22 increases with respect to the base voltage of Q25, additional current is supplied to the emitters of Q12 and Q13, increasing the charge and discharge current of the timing capacitor C_o, increasing the VCO frequency. Reducing the base voltage of Q22 with respect to Q25 similarly reduces the VCO frequency. Two Zener diodes and two transistors, CR4, CR5, Q5 and Q10, respectively, provide level shifting which allows the VCO to be driven by the outputs of the phase detector.

The phase detector is a doubly-balanced multiplier formed by transistors Q6-Q9, Q17 and Q18. Signal input is made to the lower stage, biased at about 4V by means of 2kΩ base resistors. The upper stage is biased and driven directly by the VCO output taken from the collector resistors of Q12 and Q13. A differential output signal is available between the collectors of Q6 (and Q8) and Q7 (and Q9). An external network, together with the 6k collector resistors, comprises the low pass filter. The phase detector is operated from regulated 14V appearing at the emitter of Q27. A resistor in the collector of Q25 can be shunted with an external capacitor to

SCHEMATIC DIAGRAM OF 560N

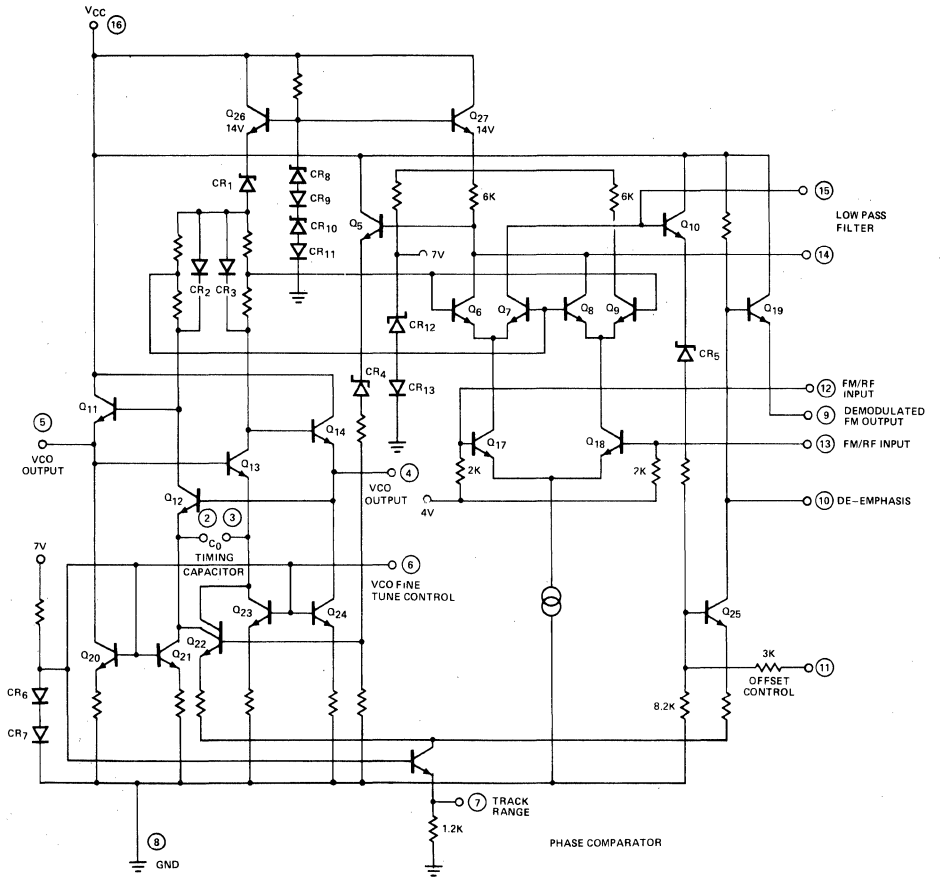


Figure 9-19

form a de-emphasis filter. The de-emphasized signal is buffered by emitter follower Q19 before being brought out.

The Track Range input, pin 7 on all three loops, allows the user to control the total current flowing through the frequency controlling differential amplifier Q22, Q25. This is done by controlling effective emitter resistance of Q29, the current source for Q22, Q25. Current may be added or subtracted at pin 7 to, respectively, reduce or increase the tracking range.

The 561, shown in Figure 9-20, contains all of the circuitry of the 560 and in addition, has a quadrature phase comparator. This enables it to be used as a synchronous AM detector. The quadrature phase detector consists of transistors Q1-Q4 and Q15, Q16 which are biased and driven in the same manner as the loop phase detector. However, the quadrature detector input is single ended rather than differential (as the loop phase detector input) and the external 90° phase shift network is required to provide the proper phase relations. The demodulated AM output is brought out at pin 1.

The 562, shown in Figure 9-21, is basically the same as the 560 except that the loop is broken between the VCO and phase comparator. This allows a counter to be inserted in the loop for frequency multiplication applications. Transistors Q1-Q4 provide low impedance differential VCO outputs (pins 3 and 4), and the upper stage phase detector inputs are brought out of the package (pins 2 and 15). A bias voltage is brought out through pin 1 to provide a convenient bias level for the upper stage of the phase detector.

Interfacing

Connection of the Signetics 560N and 561N phase locked loops to external input and output circuitry is readily accomplished; however, as with any electrical system, there are voltage, current and impedance limitations that must be considered.

The inputs of the phase comparators in the 560N, 561N and 562N and the AM detector in the 561N are biased internally from a +4 volt supply; therefore, the input signals must be capacitively coupled to the PLL to avoid interfering with this bias. These coupling capacitors should be selected to give negligible phase shift at the input frequency and impedance of the PLL. (The capacitive impedance at the operating frequency should be as small as possible, compared to the input resistance of the PLL.)

The input resistance of the phase comparator is 2000Ω single-ended, and 4000Ω when differentially connected. The input resistance of the AM detector is 3000Ω. The signal input to the phase comparator may be ap-

SCHEMATIC DIAGRAM OF 561N

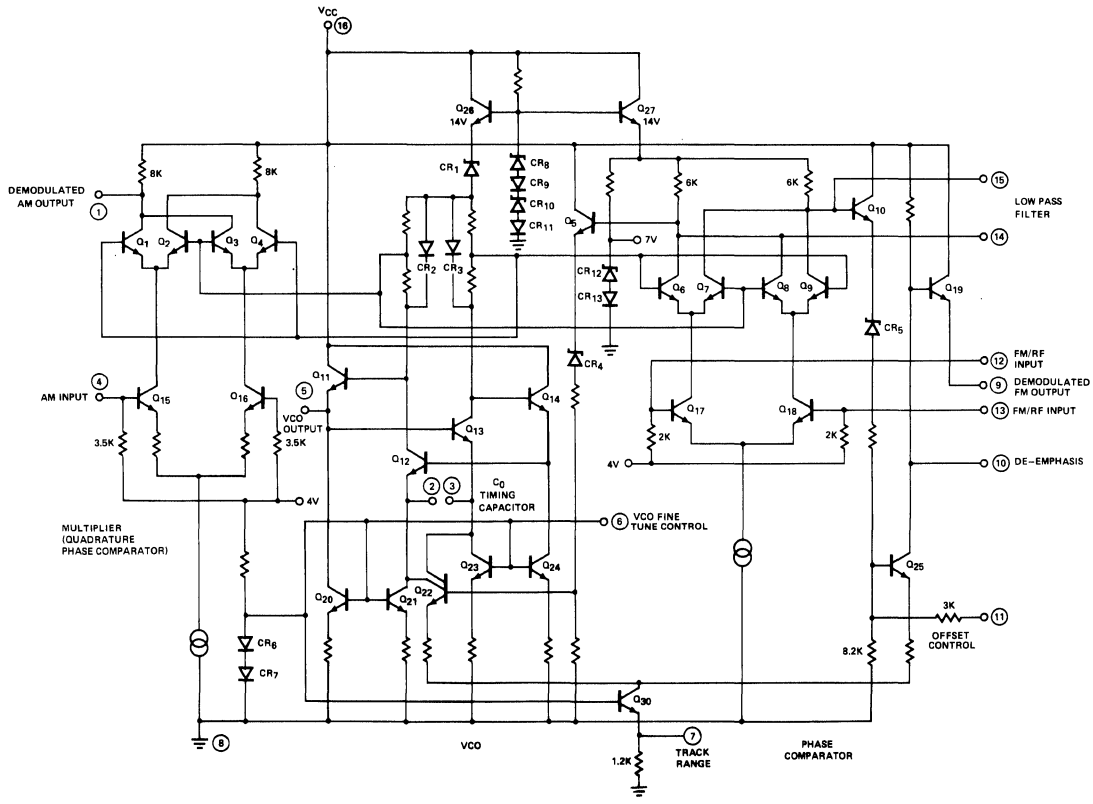


Figure 9-20

plied differentially if there is a common mode noise problem; however, in most applications, a single-ended input will be satisfactory. When inputs are not used differentially, the unused input may be ac-coupled to ground to double the phase detector gain at low input amplitudes.

The amplitude of the input signal should be adjusted to give optimum results with the PLL. Signals of less than 0.2mVrms may have an unsatisfactory signal-to-noise ratio; signals exceeding 25mVrms will have reduced AM rejection (less than 30dB). The AM detector will handle input signals up to 200mV peak-to-peak without excessive distortion, and will handle up to 2V peak-to-peak where distortion is not a factor.

Interfacing of the available outputs is best described by referring to the following diagrams. Figure 9-22 shows the PLL VCO output as a clock circuit for logic pulse synchronization. Figures 9-22a and 9-22b show the 560N and 561N, respectively, connected directly to the clock circuit; however, this configuration may be limited by low voltage and the possibility of too large a capacitive load swamping the oscillator. Figures 9-22c and 9-22d show the PLL clock output for the 560N and 561N, respectively, using the μA710 Voltage Comparator as a buffer amplifier to provide an output voltage swing suitable for driving logic circuits. The power supply for circuits utilizing the μA710 is split (+12 and -6V dc).

In Figure 9-23a the 560N is a FM demodulator used for the detection of audio information on frequency modulated carriers. Since the lower frequency limit of this type of information is approximately 1Hz, capacitive coupling may be used. However, in some applications where carrier shifts occur at an extremely slow rate, direct coupling from the output to load is necessary. Figure 9-23b shows an alternative FM detector output configuration which should be used if a different output is desirable. In this case, the output is removed at pins 14 and 15. These pins are the terminals of the low pass filter and are in the line containing the demodulated signal. The signal level (single-ended) is about one-sixth of that at pin 9 so that additional amplification may be required.

Additional receiving modes are illustrated in Figure 9-24 for the 561N only. Figure 9-24a shows the 561N output when used as an AM detector; note the straight capacitive coupling. Figure 9-24b shows the 561N used as a continuous wave detector. Since this version of the circuit is for the detection of CW or AM signals, external circuitry must be incorporated for use with CW inputs. With a CW input applied, there will be a dc shift at the output of the AM detector, pin 1. This shift is small compared to the no signal dc level and may be difficult to detect in relation to power supply voltage changes. Therefore, a reference must be generated to track any power supply voltage variations and to compensate for internal PLL thermal drift. This is best accompanied by simulating a portion of the PLL internal structure.

SCHEMATIC DIAGRAM OF 562N

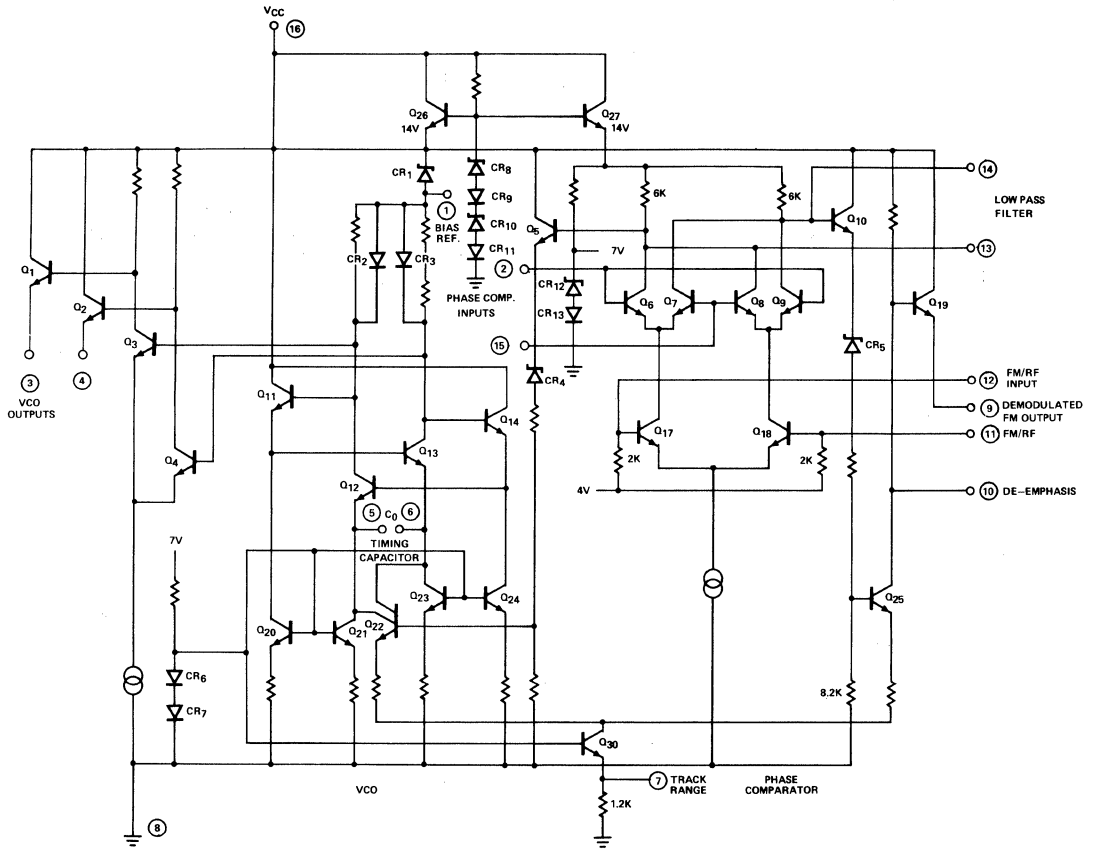


Figure 9-21

The 2N3565 npn transistor is used as a constant-current source. Its reference voltage is obtained from an internal PLL bias source at pins 12 and 13, with the current level established by the 6.8k resistor. The 6.2k resistor and the 2.5k potentiometer simulate the PLL output resistance. The differential amplifier, composed of two 2N3638 pnp transistors, amplifies the dc output and allows it to drive a npn transistor referenced to ground. This type of circuit may also be used as a tone detector or to sense that the PLL is locked to an incoming signal.

The 562 phase locked loop is especially designed for utilizing the output of the VCO. In this configuration, an amplifier-buffer has been added to the VCO to provide differential square wave outputs with a 4.5V amplitude (see block diagram Figure 9-25). This facilitates the utilization of the frequency stabilized VCO as a timing or clocking signal. The outputs (pins 3 and 4) are emitter-followers and have no internal load resistors; therefore, external 3k to 12kΩ load resistors are required.

It is essential that the resistance from each pin to ground be equal in order to maintain output waveform symmetry and to minimize frequency drift. When locking the VCO output to the phase comparator (pins 3 to 2 for single-ended connection), capacitive coupling should be used. If a signal exceeding 2V is to be applied, a 1kΩ resistor should be placed in series with the coupling capacitor. This resistor may be part of the load resistance of 12kΩ, by using two resistors (1k and 11k) to form the VCO load, as shown in Figure 9-26.

The output from the VCO is a minimum of 3V peak-to-peak, but has an average level of 12Vdc; that is, it oscillates from 10.5 to 13.5V. To utilize this output with logic circuits, some means of voltage level shifting must be used. Figures 9-27 and 9-28 show two methods of accomplishing level shifting. These circuits will operate satisfactorily to 20MHz.

The phase comparator inputs of the 562N (pins 2 and 15) must be biased by connecting a 1kΩ resistor from each pin to the 8V bias supply available at pin 1. Pin 1 should be capacitively bypassed to ground. The inputs to the phase comparator should be capacitively coupled.

VCO INPUT INTERFACING

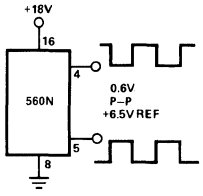


Figure 9-22a

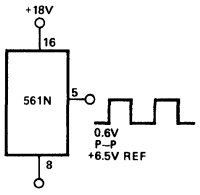


Figure 9-22b

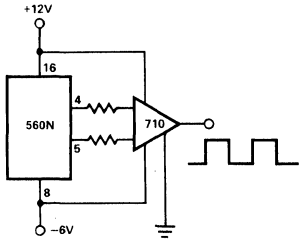


Figure 9-22c

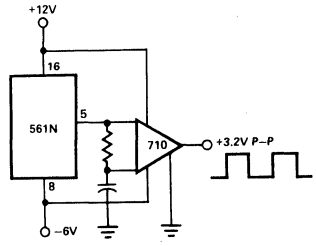


Figure 9-22d

FM DETECTOR INTERFACING

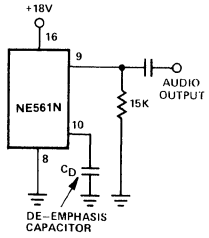


Figure 9-23a

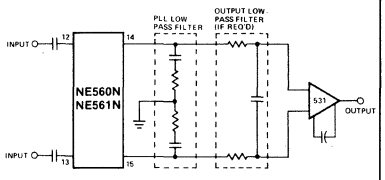


Figure 9-23b

DETECTOR INTERFACING (NE561N ONLY)

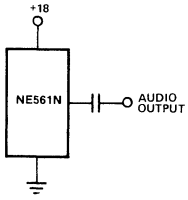


Figure 9-24a

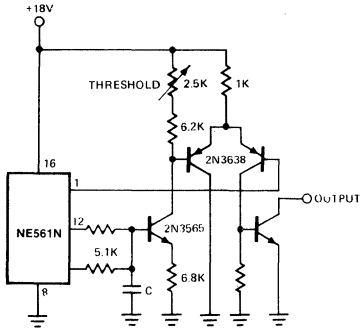


Figure 9-24b

ATTENUATING INPUT TO 562N PHASE DETECTOR

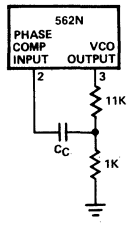


Figure 9-26

LEVEL SHIFTING 562N VCO INPUT FOR DRIVING LOGIC

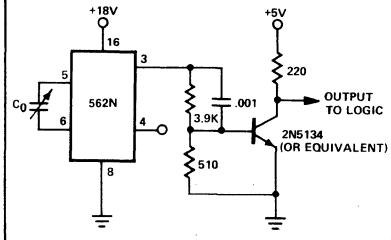


Figure 9-27

BLOCK DIAGRAM OF 562N

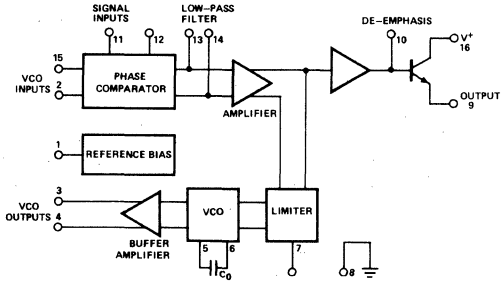


Figure 9-25

LEVEL SHIFTING 562N VCO OUTPUT FOR DRIVING LOGIC

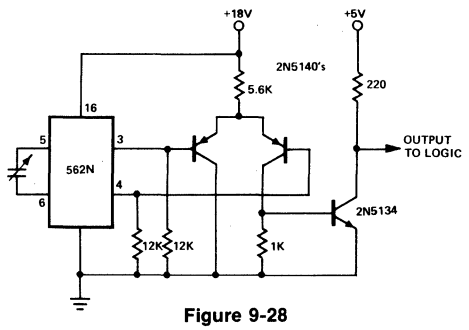


Figure 9-28

FUNCTIONAL DESCRIPTION

The NE564 is a monolithic phase locked loop with a post detection processor. The equivalent circuit of the NE564 is shown in Figure 9-28a. The use of Schottky clamped transistors and optimized device geometries extends the frequency of operation to 50MHz. In addition to the classical PLL applications, the NE564 can be used as a modulator with a controllable frequency deviation.

The output voltage of the PLL can be written as shown in the following equation:

(Equation 9-23)

$$v_o = \frac{(f_{in} - f_o)}{K_{vco}}$$

K_{vco}= conversion gain of the VCO
f_{in} = frequency of the input signal
f_o = free running frequency of the VCO

The process of recovering FSK signals involves the conversion of the PLL output into digital, logic compatible signals. For high data rates, a considerable amount of carrier will be present at the output due to the use of complicated filters, a comparator with hysteresis or Schmitt trigger is required. With the conversion gain of the VCO fixed, the output voltage as given by Equation 9-23 varies according to the frequency deviation of f_{in} from f_o. Since this differs from system to system, it is necessary that the hysteresis of the Schmitt trigger be capable of being changed, so that it can be optimized for a particular system. This is accomplished in the 564 by varying the voltage at pin 15 which results in a change of the hysteresis of the Schmitt trigger.

For FSK signals, an important factor to be considered is the drift in the free running frequency of the VCO itself. If this changes due to temperature, according to Equation 9-23 it will lead to a change in the dc levels of the PLL output, and consequently to errors in the digital output signal. This is especially true for narrow band signals where the deviation in f_{in} itself may be less than the change in f_o due to temperature. This effect can be eliminated if the dc or average value of the signal is retrieved and used as the reference to the comparator. In this manner, variations in the dc levels of the PLL output do not affect the FSK output.

VCO Section

Due to its inherent high frequency performance, an emitter coupled oscillator is used in the VCO. In the circuit, shown in the equivalent schematic, transistors Q21 and Q23 with current sources Q25 - Q26 form the basic oscillator. The free running frequency of the oscillator is shown in the following equation:

(Equation 9-24)

$$f_o = \frac{1}{16R_cC1}$$

R_c = R19 = R20
C1= frequency setting external capacitor

Variation of V_d changes the frequency of the oscillator. As indicated by Equation 9-24, the frequency of the oscillator has a negative temperature coefficient due to the positive temperature coefficient of the monolithic resistor. To compensate for this, a current I_R with negative temperature coefficient is introduced to achieve a low frequency drift with temperature.

Phase Comparator Section

The phase comparator consists of a double balanced modulator with a limiter amplifier to improve AM rejection. Schottky clamped vertical PNPs are used to obtain TTL level inputs. The loop gain can be varied changing the current Q4 and Q15 which effectively changes the gain of the differential amplifiers. This can be accomplished by introducing a current at pin 2.

Post Detection Processor Section

The post detection processor consists of a unity gain transconductance amplifier and comparator. The amplifier can be used as a dc retriever for demodulation of FSK signals, and as a post detection filter for linear FM demodulation. The comparator has adjustable hysteresis so that phase jitter in the output signal can be eliminated.

As shown in the equivalent schematic, the dc retriever is formed by the transconductance amplifier Q42 - Q43 with a capacitor at the output (pin 14). This forms an integrator whose output voltage is shown in the following equation:

(Equation 9-25)

$$V_o = \frac{gm}{C2}\int V_{IN}\,dt$$

gm= transconductance of the amplifier
C2= capacitor at the output (pin 14)
V_{IN}= signal voltage at amplifier input

With proper selection of C2, the integrator time constant can be varied so that the output voltage is the dc or average value of the input signal for use in FSK, or as a post detection filter in linear demodulation.

The comparator with hysteresis is made up of Q49 - Q50 with positive feedback being provided by Q47 - Q48. The hysteresis is varied by changing the current in Q52 with a resulting variation in the loop gain of the comparator. This method of hysteresis control, which is a dc control, provides symmetric variation around the nominal value.

Design Formula

Free running frequency of VCO is shown by the following equation:

(Equation 9-26)

$$f_o = \frac{1}{16R_cC1} \text{ in Hz}$$

$R_c = 100\Omega$
C1= external cap in farads

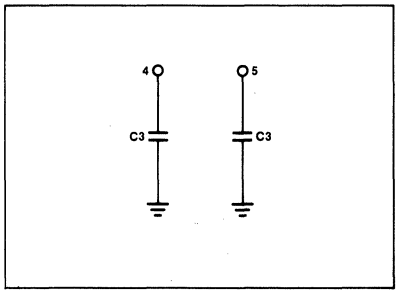
The loop filter diagram shown is explained by the following equation:

(Equation 9-27)

$$F(s) = \frac{1}{1 + sRC3}$$

$R = R12 + R13 + 1.3k\Omega$

LOOP FILTER



FM DEMODULATOR

The NE564 can be used as an FM demodulator. The connections for operation at 5V and 12V are shown in Figures 9-29 and 9-30 respectively. The input signal is ac coupled with the output signal being extracted at pin 14. Loop filtering is provided by the capacitors at pins 4 and 5 with additional filtering being provided by the capacitor at pin 14. Since the conversion gain of the VCO is not very high, to obtain sufficient demodulated output signal the frequency deviation in the input signal should be fairly high (1% or higher).

FM DEMODULATOR WITH TTL COMPATIBLE OUTPUT SIGNAL

An FM demodulator with the output signal being a TTL signal can be obtained from the NE564 by connecting it as shown in Figure 9-31. This operation requires the use of the dc retriever, the capacitance for which is connected at pin 14. The hysteresis of the Schmitt trigger can be adjusted by connecting a potentiometer at pin 15. The output signal appears at pin 16, which requires an external resistor. If necessary, the duty cycle of the output signal can be adjusted by applying a voltage at pin 14 (around 2.5V) and varying it. The connection for a similar application appears in Figure 9-32.

EQUIVALENT CIRCUIT - NE564 — 50MHz PLL

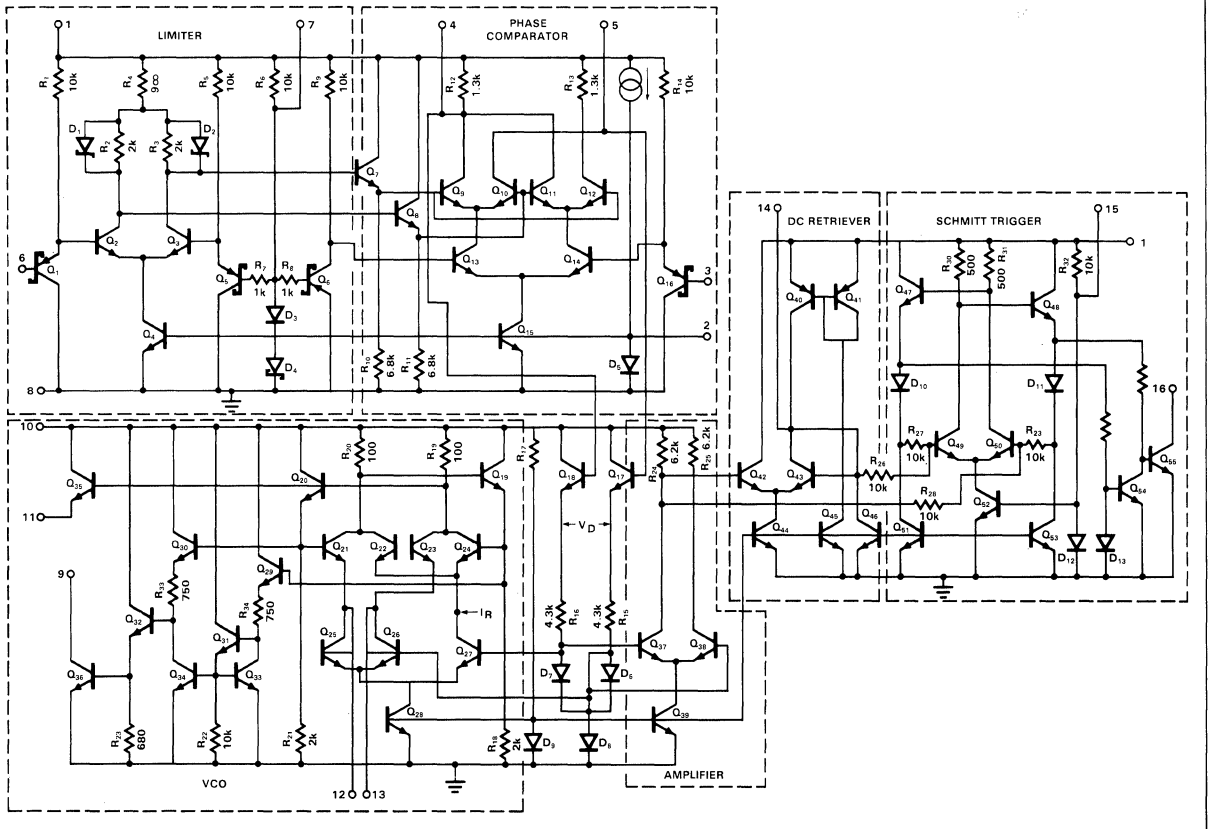


Figure 9-28a

GATED PLL DEMODULATOR

The lock range adjust pin of the NE564 can be used to gate the PLL when it is operating in the demodulator mode. The circuit is connected as shown in Figure 9-33. The gating voltage which can be a TTL signal is applied to pin 2. When this voltage is high, the loop is in lock and the demodulated output signal appears at pin 16. When the input to pin 2 is low, the loop is out of lock and the VCO will be at its center frequency. It is also possible to use pin 2 to adjust the loop gain so that a large capture range and small lock range can be obtained.

MODULATION TECHNIQUES

The NE564 phase locked loop can be modulated at either the loop filter ports (pins 4 and 5) or the input port (pin 6) as shown in Figure 9-34. The approximate modulation frequency can be determined from the frequency conversion gain curve shown in Figure 9-35. This curve will be appropriate for signals injected into pins 4 and 5.

FREQUENCY SYNTHESIS

Frequency multiplication can be achieved with the NE564 with the insertion of a counter (digital frequency divider) in the loop. A block diagram is shown in Figure 9-36 and the associated performance characteristic curve in Figure 9-35. Here the loop is broken between the VCO and the phase comparator and a counter is inserted. In this case, the fundamental of the divided VCO frequency is locked to the input frequency so that the VCO is actually running at a multiple of the input frequency. The amount of multiplication is determined by the counter. An obvious practical application of this multiplication property is the use of the NE564 in wide range frequency synthesizers.

FM DEMODULATOR AT 5V

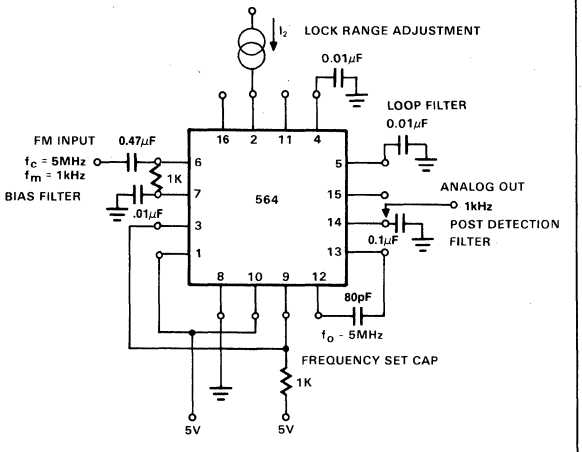


Figure 9-29

FM DEMODULATOR AT 12V

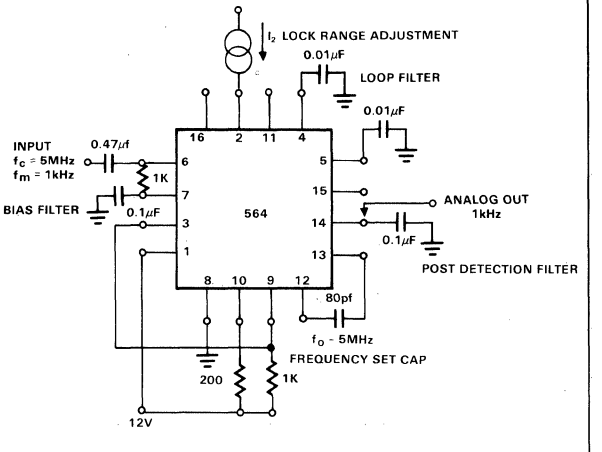


Figure 9-30

FM DEMODULATOR WITH TTL COMPATIBLE DEMODULATED OUTPUT SIGNAL

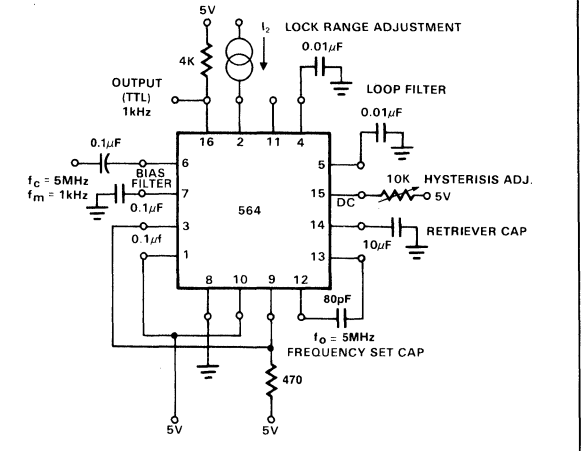


Figure 9-31

12V DEMODULATOR WITH DIGITAL OUTPUT

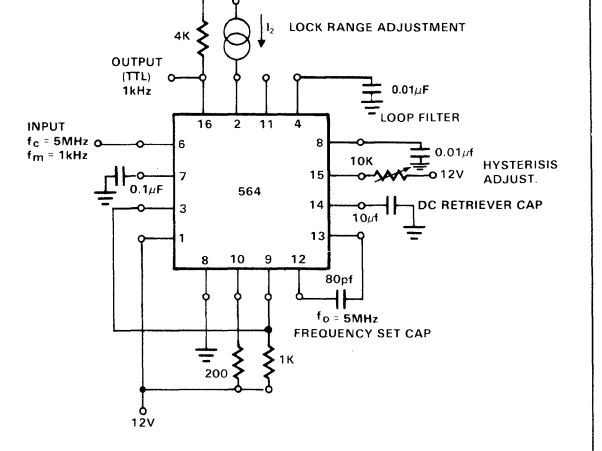
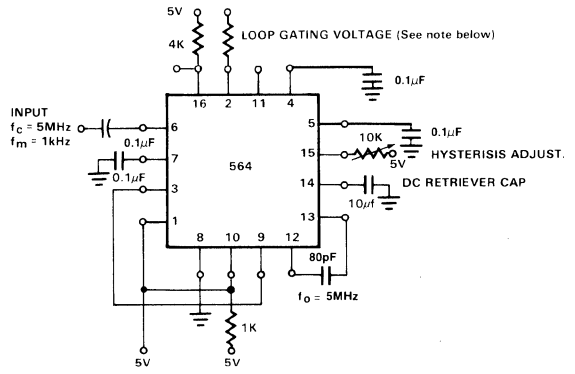


Figure 9-32

GATED PLL DEMODULATOR



NOTE

When the input to pin 2 is high (TTL level), the loop is in lock and the demodulated output at pin 16 is present. When the input to pin 2 is low (TTL level) the loop is out of lock with the VCO at its center frequency.

Figure 9-33

MODULATOR

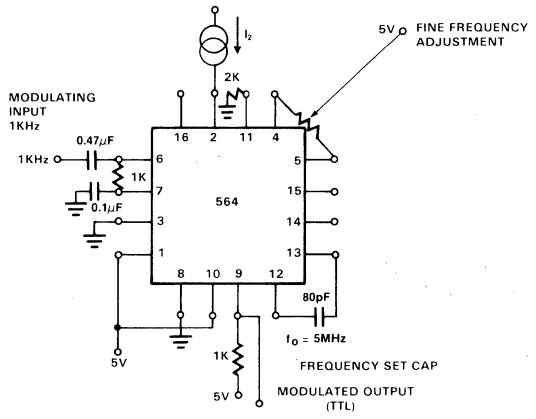


Figure 9-34

VCO CONVERSION GAIN

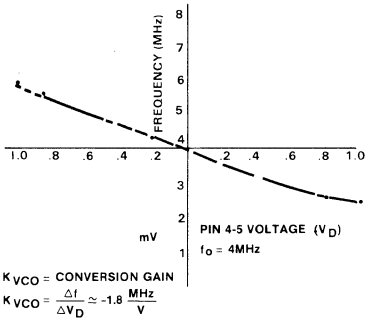


Figure 9-35

FREQUENCY SYNTHESIZER

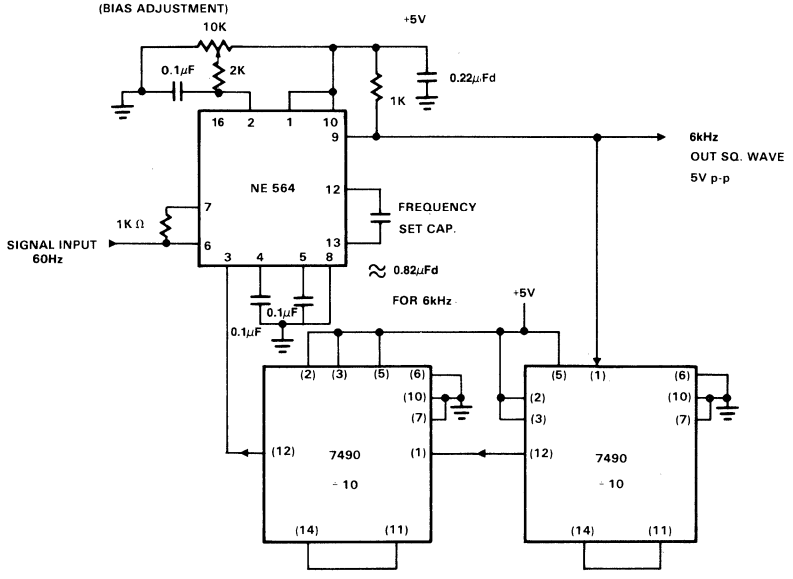


Figure 9-36

In frequency multiplication applications it is important to take into account that the phase comparator is actually a mixer and that its output contains sum and difference frequency components. The difference frequency component is dc and is the error voltage which drives the VCO to keep the NE564 in lock. The sum frequency components (of which the fundamental is twice the frequency of the input signal) if not well filtered, will induce incidental FM on the VCO output. This occurs because the VCO is running at many times the frequency of the input signal and the sum frequency component which appears on the control voltage to the VCO causes a periodic variation of its frequency about the desired multiple. For frequency multiplication it is generally necessary to filter quite heavily to remove this sum frequency component. The tradeoff, of course, is a reduced capture range and a more underdamped loop transient response.

DETAILED DESCRIPTION OF 565

The 565 is a general purpose PLL designed to operate at frequencies below 1MHz. Functionally, the circuit is similar to the 562 in that the loop is broken between the VCO and phase comparator to allow the insertion of a counter for frequency multiplication applications. With the 565, it is also possible to break the loop between the output of the phase comparator and the control terminal of the VCO to allow additional stages of gain or filtering. This is described later in this section.

The VCO is made up of a precision current source and a non-saturating Schmitt trigger. In operation, the current source alternately charges and discharges an external timing capacitor between two switching levels of the Schmitt trigger, which in turn controls the direction of current generated by the current source.

A simplified diagram of the VCO is shown in Figure 9-37. I_1 is the charging current created by the application of the control voltage V_C. In the initial state, Q3 is off and the current I_1 charges capacitor C1 through the diode D2. When the voltage on C1 reaches the upper triggering threshold, the Schmitt trigger changes state and activates the transistor Q3. This provides a current sink and essentially grounds the emitters of Q1 and Q2 to become reverse biased. The charging current I_1 now flows through D1, Q1 and Q3 to ground. Since the base-emitter voltage of Q2 is the same as that of Q1, an equal current flows through Q2. This discharges the capacitor C1 until the lower triggering threshold is reached at which point the cycle repeats itself. Because the capacitor C1 is charged and discharged with the constant current I_1, the VCO produces a triangle wave form as well as the square wave output of the Schmitt trigger.

The actual circuit is shown in Figure 9-38. Transistors Q1-Q7 and diodes D1-D3 form the precision current source. The base of Q1 is the control voltage input to the VCO. This voltage is transferred to pin 8 where it is applied across the external resistor R1. This develops a current through R1 which enters pin 8 and becomes the charging current for the VCO. With the exception of the negligible Q1 base current, all the current that enters pin 8, appears at the anodes of diodes D2 and D3. When Q8 (controlled by the Schmitt trigger) is on, D3 is reverse biased and all the current flows through D2 to the duplicating current source Q5-Q7, R2-R3 and appears as the capacitor discharge current at the collector of Q5. When Q8 is off, the duplicating current source Q5-Q7, R2-R3 floats and the charging current passes through D3 to charge C1.

SIMPLIFIED DIAGRAM OF 565 VCO

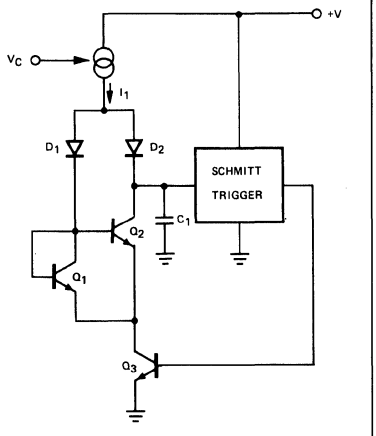


Figure 9-37

The Schmitt trigger (Q11, Q12) is driven from the capacitor triangle wave form by the emitter follower Q9. Diodes D6-D9 prevent saturation of Q11 and Q12, enhancing the switching speed. The Schmitt trigger output

SCHEMATIC DIAGRAM OF 565

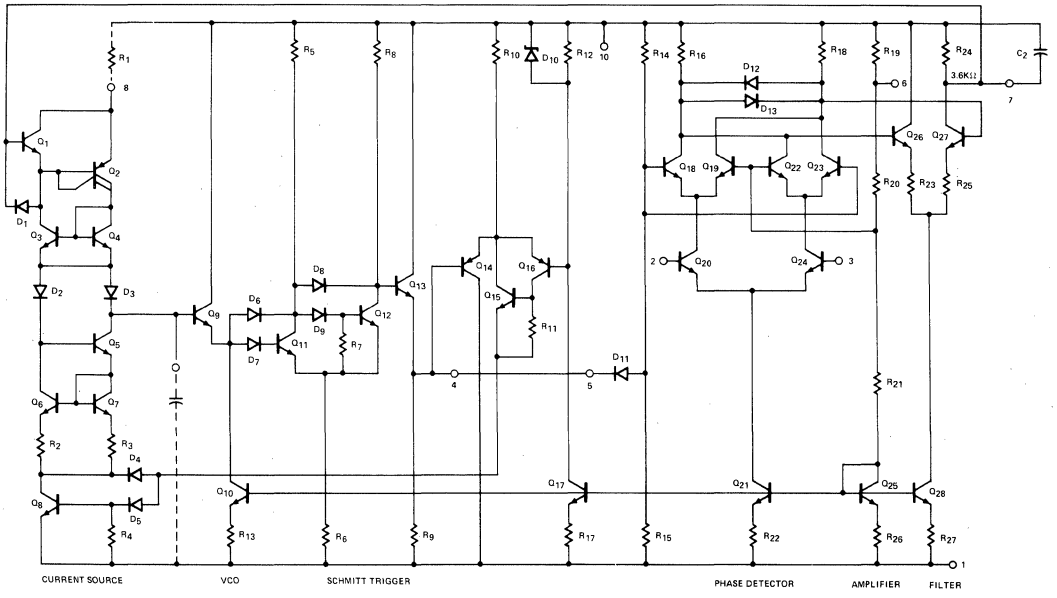


Figure 9-38

is buffered by emitter follower Q13 and is brought out to pin 4, and is also connected back to the current source by the differential amplifier (Q14-Q16).

When operated from dual symmetrical supplies, the square wave on pin 4 will swing between a low level of slightly (0.2V) below ground to a high level of one diode voltage drop (0.7V) below positive supply. The triangle wave form on pin 9 is approximately centered between positive and negative supply and has an amplitude of 2V with supply voltages of ±5V. The amplitude of the triangle waveform is directly proportional to the supply voltages.

The phase detector is again of the doubly-balanced modulator type. Transistors Q20 and Q24 form the signal input stage, and must be biased externally. If dual symmetrical supplies are used, it is simplest to bias Q20 and Q24 through external resistors to ground. The switching stage Q18, Q19, Q22 and Q23 is driven from the Schmitt trigger via pin 5 and D11. Diodes D12 and D13 limit the phase detector output, and differential amplifier Q26 and Q27 provides increased loop gain.

The loop low pass filter is formed with an external capacitor (connected to pin 7) and the collector resistance R24 (typically 3.6kΩ). The voltage on pin 7 becomes the error voltage which is then connected back to the control voltage terminal of the VCO (base of Q1). Pin 6 is connected to a tap on the bias resistor string and provides a reference voltage which is normally equal to the output voltage on pin 7. This allows differential stages to be both biased and driven by connecting them to pins 6 and 7.

The free-running center frequency of the 565 is adjusted by means of R1 and C1 and is given approximately by

(Equation 9-28)

$$f_o \approx \frac{1.2}{4R1C1}$$

When the phase comparator is in the limiting mode (Vin≥ 200mVp-p), the lock range can be calculated from the expression:

(Equation 9-29)

$$2\omega_L = 2K_oK_dA\theta_d$$

where K_o is the VCO conversion gain, K_d is the phase detector gain factor, A is the amplifier gain and θ_d is the maximum phase error over which the loop can remain in lock.

(Equation 9-30)

$$K_o = \frac{50f_o}{V_{cc}} \text{ radians/sec/volt}$$

(where f_o is the free-running frequency of the VCO and V_{cc} is the total supply voltage applied to the circuit.)

(Equation 9-31)

$$K_d = \frac{1.4}{\pi} \text{ volts/radian}$$

$$A = 1.4$$

$$\theta_d = \frac{\pi}{2} \text{ radians}$$

The lock range for the 565 then becomes:

(Equation 9-32)

$$f_L \cong \frac{\omega_L}{2\pi} \cong \frac{8f_o}{V_{cc}} \text{ Hz}$$

to each side of the center frequency, or a total range of:

(Equation 9-33)

$$2f_L \cong \frac{16f_o}{V_{cc}} \text{ Hz}$$

The capture range, over which the loop can acquire lock with the input signal is given approximately by: (Equation 9-34)

$$2\omega_C \cong 2\sqrt{\frac{\omega_L}{\tau}}$$

where ω_L is the one-sided lock range

$$\omega_L = 2\pi f_L$$

and τ is the time constant of the loop filter

$$\tau = RC_2$$

with R = 3.6KΩ.

This can be written as:

(Equation 9-35)

$$f_c \cong \pm\frac{1}{2\pi}\sqrt{\frac{2\pi f_L}{\tau}} = \pm\frac{1}{2\pi}\sqrt{\frac{32\pi f_o}{V_{cc}\tau}}$$

to each side of the center frequency of a total capture range of:

(Equation 9-36)

$$f_C \cong \frac{1}{\pi}\sqrt{\frac{32\pi f_O}{\tau V_{CC}}}$$

This approximation works well for narrow capture ranges ($f_c = 1/3f_L$) but becomes too large as the limiting case is approached ($f_c = f_L$).

DETAILED DESCRIPTION OF 566

The 566 is the voltage controlled oscillator portion of the 565. The basic die is the same as that of the 565; modified metalization is used to bring out only the VCO. The 566 circuit diagram is shown in Figure 9-39. Transistor Q18 has been a buffered triangle waveform output. (The triangle waveform is available at capacitor C1 also, but any current drawn from pin 7 will alter the duty cycle and frequency.) The square wave output is available from Q19 by pin 4. The circuit will operate at frequencies up to 1MHz and may be programmed by the voltage applied on the control terminal (pin 5), current injected into pin 6 or the value of the external resistor and capacitor (R1 and C1).

DETAILED DESCRIPTION OF 567

The 567 is a PLL designed specifically for frequency sensing or tone decoding. Like the 561, the 567 has a controlled oscillator, a phase detector and a second auxiliary or quadrature phase detector. In addition, however, it contains a power output stage which is driven directly by the quadrature phase detector output. During lock, the quadrature phase detector drives the output stage on, so the device functions as a tone decoder or frequency relay. The tone decoder center frequency and bandwidth are specified by the center frequency and capture range of the loop portion. Since a tone decoder, by definition, responds to a stable frequency, the lock or tracking range is relatively unimportant except as it limits the maximum attainable capture range.

The current controlled oscillator is shown in simplified form in Figure 9-40. It provides both a square wave output and a quadrature output. The control current I_c sweeps the oscillator ±7% of the center frequency, which is set by external components R1 and C1. It operates as follows:

Transistors Q1 through Q6 form a flip-flop which can switch pin 5 between V_{be} and $V+ - V_{be}$. Thus, the R1C1 network is driven from a square wave of $V+ - 2V_{be}$ peak-to-peak volts. On the positive portion of the square wave, C1 is charged through R1 until V_1 is reached. A comparator circuit driven from C1 at pin 6 then supplies a pulse which resets the flip-flop so that pin 5 switches to V_{be} and C1 is discharged until V_2 is reached. A second comparator then supplies a pulse which sets the flip-flop and C1 resumes charging.

The total swing of the capacitor voltage, as determined by the comparator sensing voltages, is

(Equation 9-37)

$$V_1 - V_2 = (V+ - 2V_{be})\frac{R22 + R23}{R21 + R22 + R23 + R23 + R24}$$

$$= K\,(V+ - 2V_{be})$$

Due to the excellent matching of integrated resistors, the resistor ratio K may be considered constant. Figure 9-41 shows the pin 5 and pin 6 voltages during operation. It is obvious from the proportion that $t_1 + t_2$ is independent of the magnitude of V+ and dependent only on the time constant R1C1 of the external components. Moreover, if $(V_1 + V_2)/2 = V^+/2$, then $t_1 = t_2$ and the duty cycle is 50%. Note that the triangular waveform is phase shifted from the square wave. A differential stage (Q22 and Q23) amplifies

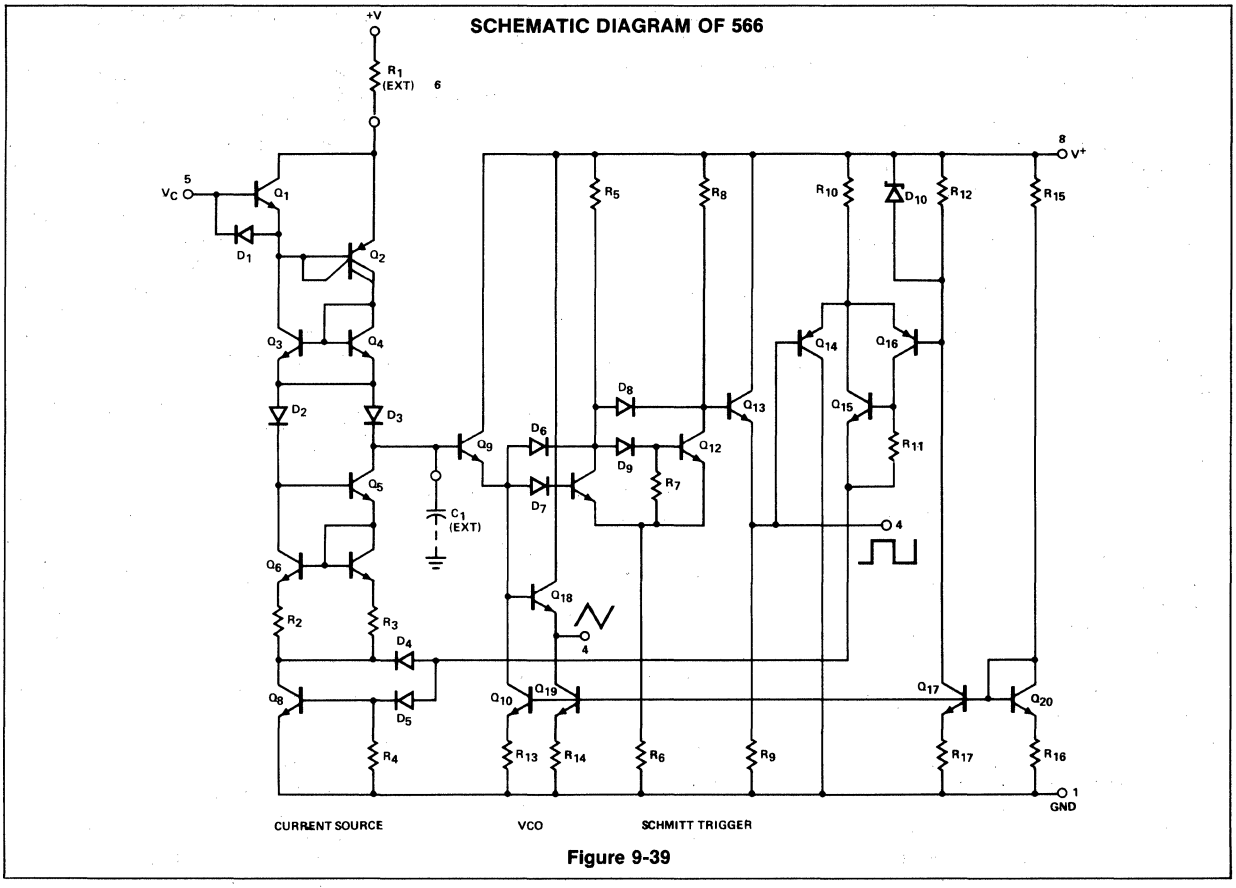


Figure 9-39

the triangular wave with respect to (V_1 and V_2)/2 to provide the quadrature output. (Due to the exponential distortion of the triangle wave, the quadrature output is actually phase shifted about 80°, but no operating compromises result from this slight deviation from true quadrature.)

One source of error in this oscillator scheme is current drawn by the comparators from the R1C1 mode. An emitter follower, therefore, is inserted at X to minimize this drain and Q21 placed in series with Q20 to drop the comparator sensing voltage one V_{be} to compensate for the V_{be} drop in the emitter follower.

LOOP GAIN CONSTANTS (K_o, K_d)

Table 9-4 gives the gain constants (K_o, K_d) for the Signetics' loops. The values given are for the standard connection with no gain reduction or tracking adjustment components connected. The dc amplifier gain A has been included in either the K_o or K_d value, depending on which side of the low pass filter terminals the gain is present. This

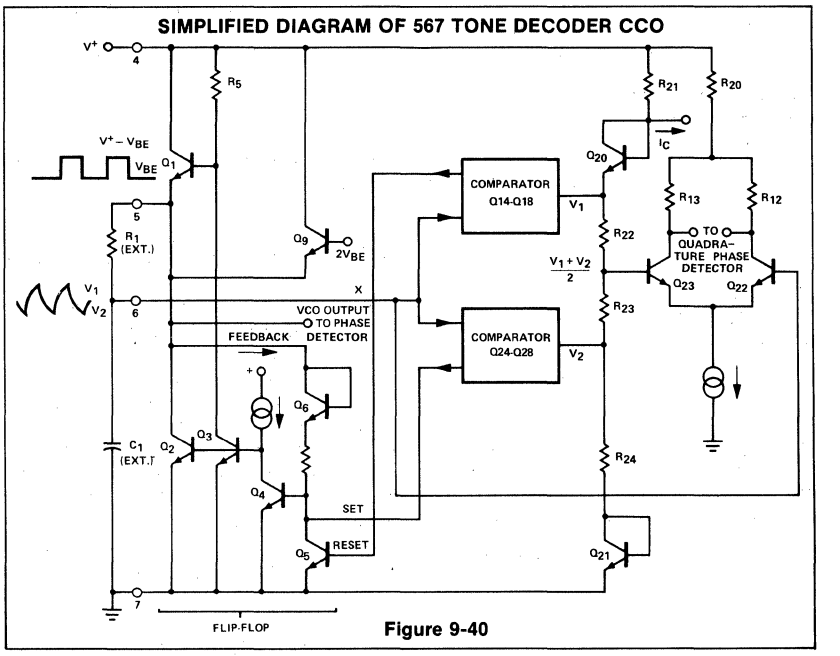


Figure 9-40

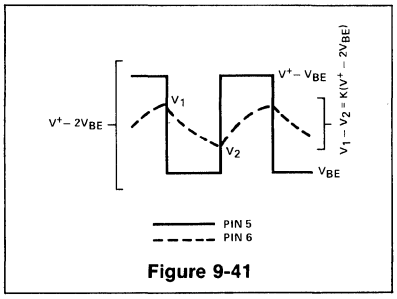


Figure 9-41

causes no hardship in calculations since the loop gain K_v becomes simply K_oK_d.

In order to insure that the square wave drops quickly and accurately to V_{be}, an active clamp scheme is applied to the collector of Q2. The base of Q9 is held at $2V_{be}$ so that as Q2 is turned on by its base current, its collector is held at V_{be}. Because Q2 and Q3 have the same geometry and their base-emitter voltages are the same, the maximum Q2 current when clamped is essentially the same as the collector current of Q3 (as limited by R5). The flip-flop was optimized for maximum switching speed to reduce frequency drift due to switching speed variations.

Current control of the frequency is achieved by making R21 somewhat less than R24 and restoring the proper voltage for 50% duty cycle by drawing I_c of 100μA for the R21, Q20 junction. When I_c is then varied between 0 and 200μA, the frequency changes by ±7%. Because of the slight shift in the voltage levels V_1 and V_2 with I_c, the square wave duty cycle changes from about 47% to about 53% over the control range. To avoid drift of center frequency with temperature and supply voltage changes when

$I_c \neq O$, I_c is also made a function of $V + -2V_{be}$.

The CCO circuit is shown in the tone decoder schematic diagram, Figure 9-42.

A doubly-balanced multiplier formed by Q32 through Q37 (Figure 9-42) functions as the phase detector. The input signal is applied to the base of Q32. Transistors Q34-Q37 are driven by a square wave taken from the CCO at the collector of Q2. Phase detector input bias is provided by three diodes, Q38 through Q40, connected in series, assuring good bias voltage matching from run to run. Emitter resistors R26 and R27, in addition to providing the necessary dynamic range at the input, help stabilize the gain over the wide temperature range.

The loop dc amplifier is formed by Q51 and Q52. Having a current gain of 8, it permits even a small phase detector output to drive the CCO the full ±7%. Therefore, full detection bandwidth can be obtained for any in-band input signal greater than about 70mVrms. However, the main purpose of high loop gain in the tone decoder is to keep the locked phase as close to $\pi/2$ as possible for all but the smallest input levels since this greatly facilitates operation of the quadrature lock detector. Emitter resistors R36 and R37 help to stabilize the gain over the required temperature range. Another function of the dc amplifier is to allow a higher impedance level at the low pass filter terminal (pin 2) so that a smaller capacitor can be used for a given loop cutoff frequency. Once again, emitter resistors help stabilize the loop gain over the temperature range.

The quadrature phase detector (QPD), formed by a second doubly-balanced multiplier Q42-Q47, is driven from the quadrature output (E, F, in Figure 9-47) of the CCO. The signal input comes from the emitters of the input transistors Q32 and Q33.

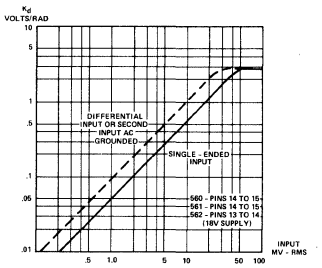
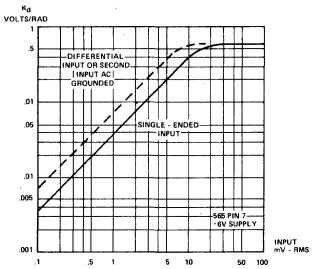
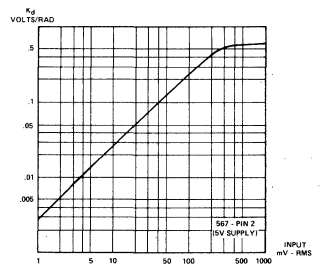
The output stage, Q53 through Q62, compares the average QPD current in the low pass output filter R3C3 with a temperature compensated current in R39 (forming the threshold voltage V_t).

Since R3 is slightly lower in value than R39, the output stage is normally off. When the lock and the QPD current I_q occurs, pin 1 voltage drops below the threshold voltage V_t and the output stage is energized.

The uncommitted collector (pin 8) of the power npn output transistor can drive both 100—200mA loads and logic elements, including TTL.

Table 9-4

PLL GAIN CONSTANTS* K_oK_d ($K_v = K_oK_d$)

	560B, 561B, 562B	565	
K_o	$0.32\omega_o \frac{\text{rad.}}{\text{sec-volt}}$ Single-Ended Input to VCO $0.64\omega_o \frac{\text{rad.}}{\text{sec-volt}}$ Differential Input to VCO	$\frac{8.0\ \omega_o}{\text{Total Supply Voltage}}$ $= 0.67\ \omega_o \frac{\text{rad.}}{\text{sec-volt}}$ at ± 6 volts	$0.44\omega_o \frac{\text{rad.}}{\text{sec-volt}}$
K_d			

*The dc amplifier gain A has been included in K_o or K_d, depending on which side of the LPF terminals the amplifier is located.

SCHEMATIC DIAGRAM OF 567

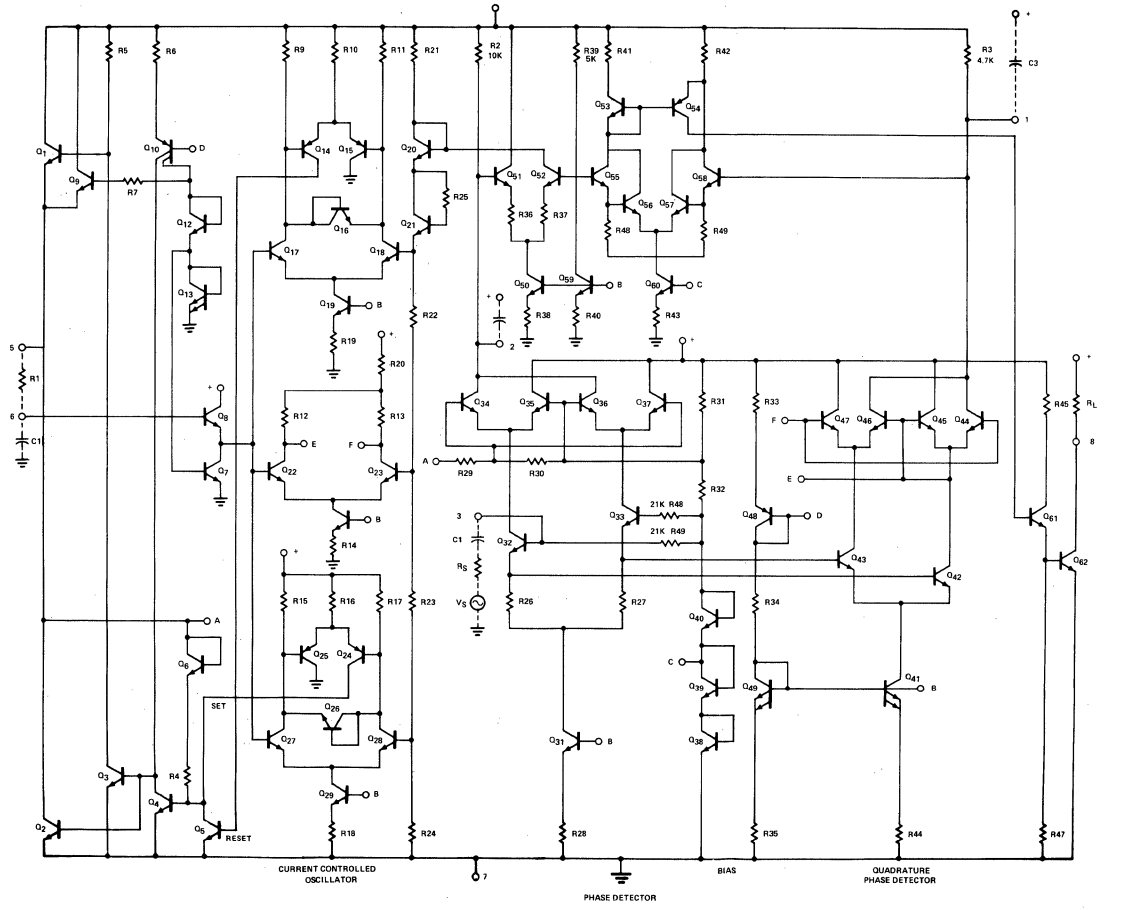


Figure 9-42

EXPANDING LOOP CAPABILITY

Low Pass Filter Circuits (560N, 561N and 562N)

The low pass filters used with the 560N, 561N and 562N are externally adjusted to provide the desired operational characteristics. To select the most appropriate type of filter and component values, a basic understanding of filter operation is required.

A FM signal to be demodulated is matched in the phase comparator with the voltage controlled oscillator signal, which is tuned to the FM center frequency. Any resulting phase difference between these two signals is the demodulated FM signal. This demodulated signal is normally at frequencies between dc and upper audio frequencies.

The choice of low pass filter response gives a degree of design freedom in determining the capture range or selectivity of the loop. The attenuation of the high frequency error components at the output of the phase detector enhances the interference rejection characteristics of the loop. The filter also provides a short-term memory for the PLL that ensures rapid recapture of the signal if the system is thrown out of lock due to noise transient.

To ensure absolute closed loop stability at all signal levels within the dynamic range of the loop, the open loop PLL is required to have no more than 12dB per octave high frequency roll-off.

The capacitor in each filter circuit shown in Figure 9-43 will provide 6dB per octave roll-off at the first break point—the desired bandwidth frequency. The resistor R_X shown in filters (c) and (d) is used to break the response up at high frequencies to ensure 6dB per octave roll-off at the loop unity gain frequency. R_X is typically between 50 and 200Ω.

Calculations of values for low pass filters shown can be made using the complex second-degree transfer function equations given, or approximated using the equation:

(Equation 9-38)

$C1 = \frac{26.60}{f}$ mfd for filters (a) and (c), and the equation:

$C1 = \frac{13.30}{f}$ mfd for filters (b) and (d) where f is the desired first break frequency in Hz.

At frequencies greater than 5MHz where the loop may be prone to instability, filters (C) and (D) should be used. For operation at low frequencies, a simple type (b) lag filter with no added resistance is usually sufficient.

LOW PASS FILTER CONFIGURATIONS

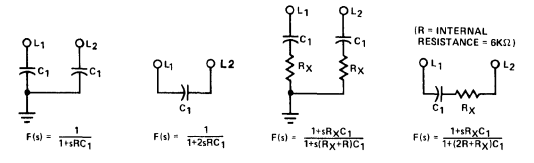


Figure 9-43

NARROW BANDWIDTH FM DEMODULATOR

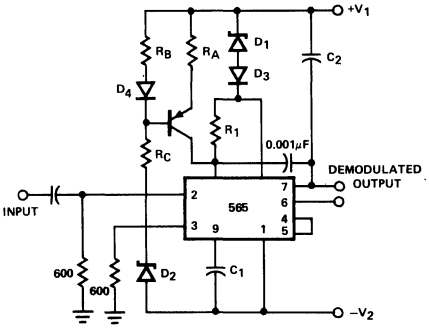


Figure 9-45

OPERATING FREQUENCY EXTENSION FOR 560N, 561N and 562N

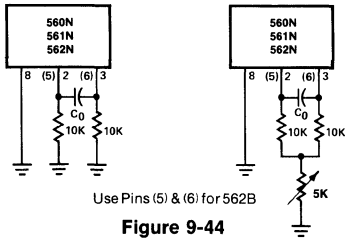


Figure 9-44

Operating Frequency Extension to 60MHz (560N, 561N, 562N)

The frequency range of the 560N, 561N and 562N phase locked loops may be extended to 60MHz by the addition of two 10kΩ resistors from the timing capacitor terminals to the negative power supply as shown in Figure 9-44. The inclusion of a 5kΩ potentiometer between these 10kΩ resistors and the negative supply provides a simple method of fine tuning.

Increased Loop Output Voltage For Small Frequency Deviations (565)

For applications where both a narrow lock range and a large output voltage swing are required, it is necessary to inject a constant current into pin 8 and increase the value of R1. One scheme for this is shown in Figure 9-45. The basis for this scheme is the fact that the output voltage controls only the current through R1 while the current through Q1 remains constant. Thus, if most of the charging current is due to Q1, the total current can be varied only a small amount due to the small change in current through R1. Consequently, the VCO can track the input signal over a small frequency range yet the output voltage of the loop (control voltage of the VCO) will swing its maximum value.

Diode D1 is a Zener diode, used to allow a larger voltage drop across R_A than would otherwise be available. D4 is a diode which should be matched to the emitter-base junction of Q1 for temperature stability. In addition, D1 and D2 should have the same breakdown voltages and D3 and D4 should be similar so that the voltage seen across R_B and R_C is the same as that seen across pins 10 and 1 of the phased locked loop. This causes the frequency of the loop to be insensitive to power supply variations. The center frequency can be found by:

(Equation 9-39)

$$f_o \simeq \frac{2R_B}{(R_B + R_C)R_A C1} + \frac{1}{4R1C1} \text{ Hz}$$

and the total lock range is given by:

(Equation 9-40)

$$2\Delta f_L \simeq \frac{22.4V_D(R_B + R_C)R_A f_o}{(|V_1|+|V_2|-V_Z-V_D)(8R_BR1+R_A[R_B+R_C])} \text{ Hz}$$

where:

V_D = forward biased diode voltage ≈ 0.7V
V_Z = Zener diode breakdown voltage
V_1 = positive supply voltage
V_2 = negative supply voltage
f_o = free-running VCO center frequency

When the output excursion at pin 7 need be only a volt or so, diodes D1 , D2 and D3 may be replaced by short circuits.

The value of R1 can be selected to give a prescribed output voltage for a given frequency deviation.

(Equation 9-41)

$$R1 = \frac{R_A(R_B + R_C)f_o}{R_B(|V_1| + |V_2| - 0.7)\Delta f}$$

where f_o is the center frequency and Δf is the desired frequency deviation per volt of output.

In most instances, R_B and R_A are chosen to be equal so that the voltage drop across them is about 200mV. For the best temperature stability, diode D1 should be a base-collector shorted transistor of the same type as Q1.

Expanded Lock Range (565)

When the 565 is connected normally, feedback to the VCO from the phase detector is internal. That is, an amplifier makes the pin 8 voltage track the pin 7 (phase detector output) voltage. Since the capacitor C1 charge current is determined by the current through resistance R1, the frequency is a function of the voltage at pin 8. It is possible, however, to bypass and swamp the internal loop amplifier so that the current into pin 8 is no longer a function of the pin 8 voltage but only of the pin 7 voltage. This makes a greater charge-discharge current variation possible, allowing a greater lock range. Figure 9-46 shows such a circuit in which the μA741 operational amplifier is set for a differential gain of 5, feeding current to pin 8 through the 33k resistor (simulating a current source). Not only is the tracking range greatly expanded, but the output voltage as a function of frequency is five times greater than normal. In setting up such a circuit, the user should keep in mind that for best frequency stability, the charge-discharge current should be in the range of 50 to 1500μA which also specifies the pin 8 input current range, showing that a ratio of upper to lower lock extremes of about 30 can be achieved.

EXPANDED LOCK RANGE CONFIGURATION FOR 565

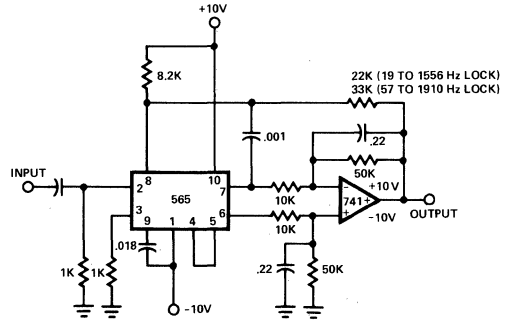


Figure 9-46

INCREASED LOOP GAIN AND LOCK RANGE FOR 565

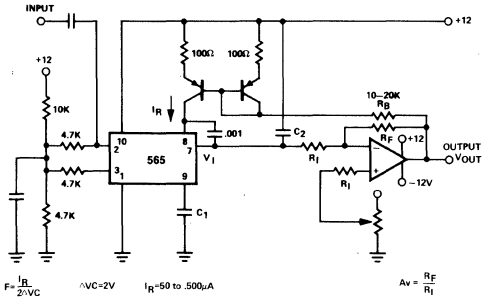


Figure 9-47

Breaking the Internal Feedback Loop (565)

Many times it would be advantageous to be able to break the feedback connection between the output (pin 7) and the voltage control terminal (Q1) of the VCO. This can be easily done once it is seen that it is the *current* into pin 8 which controls the VCO frequency. If the external resistor R1 is replaced with a current source, such as in Figure 9-47, we have effectively broken the internal voltage feedback connection. The current flowing into pin 8 is now independent of the voltage on pin 8. The output voltage (on pin 7) can now be amplified or filtered and used to drive the current source by a scheme such as that shown in Figure 9-47. This scheme allows the addition of enough gain for the loop to stay in lock over a 100:1 frequency range, or conversely, to stay in lock with a precise phase difference (between input and VCO signals) which is almost independent of frequency variation. Adjustment of the voltage to the non-inverting input of the op amp, together with a large enough loop gain allows the phase difference to be set at a constant value between 0° and 180°. In addition, it is now possible to do special filtering to improve the performance in certain applications. For instance, in frequency multiplication applications it may be desirable to include a notch filter tuned to the sum frequency component to minimize incidental FM without excessive reduction of capture range.

Breaking the Internal Feedback Loop (560, 561, 562)

The internal control voltage feedback loop can also be easily broken on the 560, 561 and 562. The key in this case is to bias the range control terminal (pin 7) to +2V which turns off the controlled current source. Now the phase comparator output voltage will have no effect on the charging current which sets the VCO frequency. Now an external feedback loop can be built with the desired transfer function. Figure 9-48 shows a practical application of this principle. The control voltage is taken from across the low pass filter terminals, amplified, and used to add or subtract current into the timing capacitor nodes.

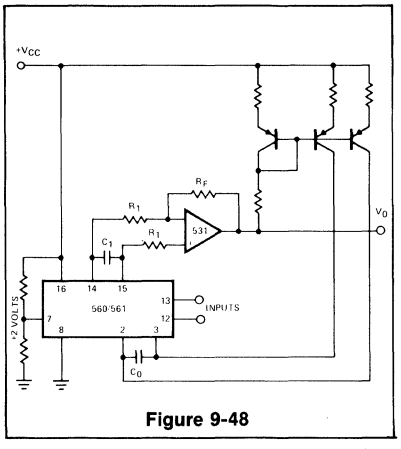


Figure 9-48

Minimizing Tone Decoder Response Time

The 567 Tone Decoder is a specialized loop which can be set up to respond to a given tone (constant frequency) within its bandwidth. The center frequency is set by a resistor R1 and capacitor C1 which determine the free-running frequency. The bandwidth is controlled by the low-pass filter capacitor C2. A third capacitor C3 integrates the output of the quadrature phase detector (QPD) so that the dc lock-indicating component can switch the power output stage on when lock is present. The 567 is optimized for stability and predictability of center frequency and bandwidth.

Two events must occur before an output is given. First, the loop portion of the 567 must achieve lock. Second, the output capacitor C3 must charge sufficiently to activate the output stage. For minimum response time, these events must be as brief as possible.

As previously discussed, the lock time of a loop can be minimized by reducing the response time of the low pass filter. Thus, C2 must be as small as possible. However, C2 also controls the bandwidth. Therefore, the response time is an inverse function of bandwidth as shown by Figure 9-49, reprinted from the 567 data sheet. The upper curve denotes the expected worst-case response time when the bandwidth is controlled solely by C2 and the input amplitude is 200mVrms or greater. The response time is given in cycles of center frequency. For example, a 2% bandwidth at a center frequency of 1000 cycles can require as long as 280 cycles (280ms) to lock when the initial phase relationship is at its worst. Figure 9-50 gives a typical distribution of response time versus input phase. Note that, assuming random initial input phase, only 30/180 = 1/6 of the time will the lock-up time be longer than half the worst case lock-up time. Figure 9-51 shows some actual measurements of lock-up time for a set-up having a worst case lock-up time of 27 cycles and a best-case lock-up time of four input cycles.

The lower curve on the graph shows the worst-case lock-up time when the loop gain is reduced as a means of reducing the bandwidth (see data sheet, Alternate Method of Bandwidth Reduction). The value of C2 required for this minimum response time is

(Equation 9-42)

$$C_2' = \frac{130}{f_o}\left[\frac{10k - R_A}{R_A}\right] \mu F$$

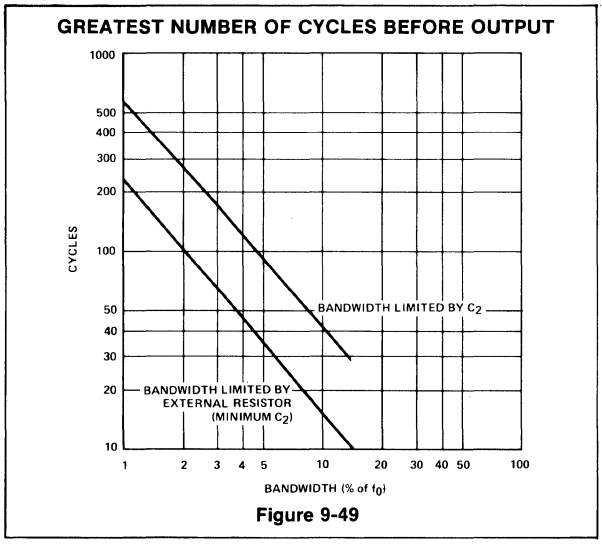


Figure 9-49

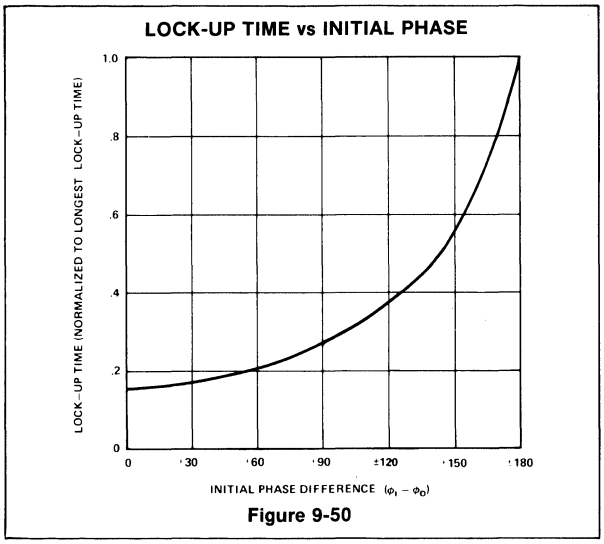


Figure 9-50

It is important to note that noise immunity and rejection of out-band tones suffer somewhat when this minimum value (C2) of C2 is used so that response time is gained at their expense. Except at very low input levels, input amplitude has only a minor effect on the lock-up time—usually negligible in comparison to the variation caused by input phase.

Lock-up transients can be displayed on a two-channel scope with ease. Figure 9-52 shows the display which results. The top trace shows the square wave which either gates the input generator signal off and on (or shifts the frequency in and out of the band if you have a generator which has a frequency control input only). The lower trace shows the voltage at pin 2, the low pass filter voltage. The input frequency is offset slightly from the center frequency so that the locked and unlocked voltage are different. It is apparent that, while the C2 decay during unlock is always the same, the lock transient is different each time. This is because the turn-on repetition rate is such that a different initial phase relationship occurs with each appearance of the in-band signal. It is tempting to adjust the repetition rate so that a fast, constant lock-up transient is displayed. However, in doing so a favorable initial phase is created that is not present in actual operation. On the contrary, it is most realistic to adjust the repetition rate so that the longest lock-up time is displayed, such as the fifth lock transient shows. Once this display is achieved, the effect of various adjustments in C2 or input amplitude is seen. However, *the repetition rate must be readjusted for worst-case lock-up after each change.*

Once lock is achieved, the quadrature phase detector output at pin 1 is integrated by C3 to extract the dc component. As C3 charges from its quiescent value V_q (see Figure 9-53) to its final value (V_q—ΔV), it passes through the output stage threshold, turning it on. The total voltage change is a function of input amplitude. Since the unadjusted V_q is very close (within 50mV) to V_t, the output stage turns on very soon after lock. Only a small fraction of the output stage time constant (τ = 4700C3) expires before V_t is crossed so that C3 does not greatly influence the response time. However, as shown in Figure 9-53a, the turn-off

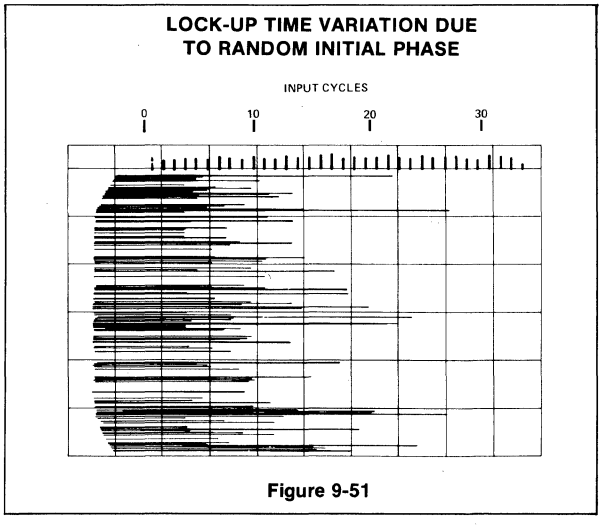


Figure 9-51

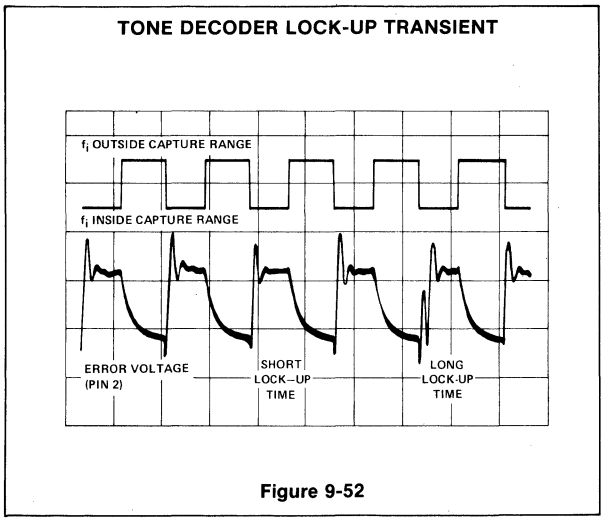


Figure 9-52

delay time can be quite long when C3 is large. Figure 9-53b shows how desensitizing the output stage by connecting a high-value resistor between pin 1 and pin 4 (plus supply) can equalize the turn-on and turn-off time. If turn-off delay is important in the overall response time, then desensitizing can reduce the total delay.

But why not make C3 very small so that these delays can be totally neglected? The problem here is that the QPD output has a large twice-center-frequency component that must be filtered out. Also, noise, outband signals and difference frequencies formed by close out-band frequencies beating with the VCO frequency appear at the QPD output. All these must be attenuated by C3 or the output stage will chatter on and off as the threshold is approached. The more noisy the input signal and the larger the near-band signals, the greater C3 must be to reject them. Thus, there is a complicated relationship between the input spectrum and the size of C3. What must be done, then, is to make C3 more than sufficient for proper operation (no false outputs or missed signals) under actual operating conditions and then reduce its value in small steps until either the required response time is obtained or operation becomes unsatisfactory.

In setting up the tone decoder for maximum speed, it is best to proceed as follows:

a. After the center frequency has been set, adjust C2 to give the desired bandwidth or, if the graph of response time in cycles (Figure 9-51) suggests that worst-case lock-up time will be too long, incorporate the loop gain reduction scheme as an alternate means of bandwidth reduction. (See data sheet.)
b. Check lock-up time by observing the waveform at pin 2 while pulsing the input signal on and off (or in and out of the band when a FM generator is used). Adjust repetition rate to reveal worst lock-up time.
c. Starting with a large value of C3 (say 10 C2), reduce it as much as possible in steps while monitoring the output to be certain that no false outputs or missed signals occur. The full input spectrum should be used for this test. Ignore brief transients or chatter during turn-on and turn-off as they can be eliminated with the chatter prevention feedback technique described in the data sheet.
d. Use the desensitizing technique, also described in the data sheet, to balance turn-on and turn-off delay.
e. Apply the chatter prevention technique to clean up the output.

If this procedure results in a worst-case response time that is too slow, the following suggestions may be considered:

a. Relax the bandwidth requirement.
b. Operate the entire system at higher frequency when this option is available.
c. Use two tone decoders operating at slightly different frequencies and OR the outputs. This will reduce the statistical occurrence of the worst-case lock-up time so that excessive lock-up time occurs. For example, if the lock-up time is marginal 10% of the time with one unit, it will drop to 1% with two units.
d. Control the in-band input amplitude to stabilize the bandwidth, set up two tone decoders for maximum bandwidth and overlap the detection bands to make the desired frequency range equal to the overlap. Since both tone decoders are on only when a tone appears within the overlap range, the outputs can be ANDed to provide the desired selectivity.
e. If the system design permits, send the tone to be detected continuously at a low level (say 25mVrms) to keep the loop in lock at all times. The output stage, slightly desensitized, can then be gated on as required by increasing the signal amplitude during the on time. Naturally, the signal phase should be maintained as the amplitude is changed. This scheme is extremely fast, allowing repetition rates as fast as 1/3 to 1/2 the center frequency when C3 is small. This is equivalent to ASK (amplitude shift keying).

EFFECT OF THRESHOLD VOLTAGE (Vt) ADJUSTMENT ON THE TONE DECODER TURN-ON AND TURN-OFF DELAY

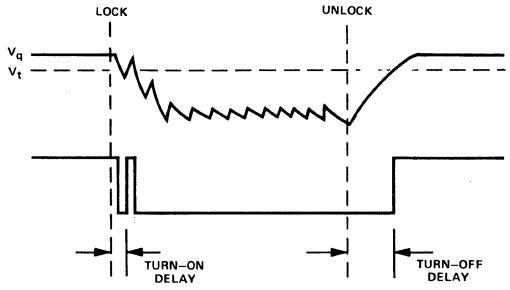


Figure 9-53a

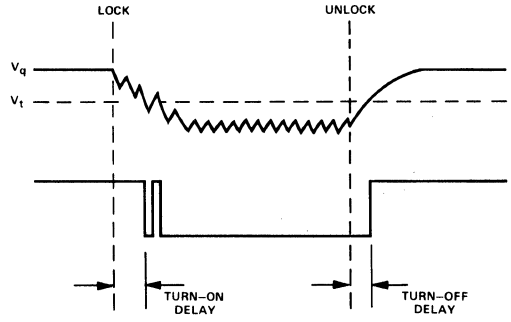


Figure 9-53b

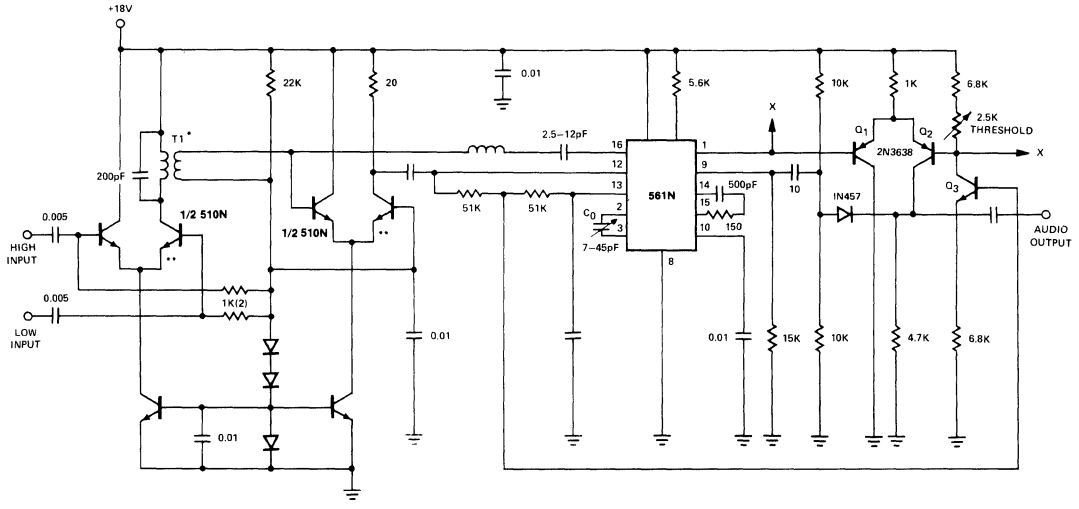
FM IF Amplifier/Demodulator With Muting (561N)

In this application, the loop portion of the 561N operates in the usual manner for FM demodulation. To introduce muting (squelch) the synchronous AM detector portion of the PLL is used to detect the presence of an input signal and to open a muting gate. Figure 9-54 shows a typical circuit incorporating the muting feature.

The input section of the circuit is a broadband, amplifier-limiter. The tuned LC network at the AM input, pin 4, is adjusted to provide a 90° phase shift at the IF frequency. This network is adjusted for maximum output at pin 1, demodulated AM output, with a carrier applied, at the IF frequency.

Three transistors at the right of the diagram (Q1, Q2 and Q3) and the 1N457 diode form

TYPICAL FM IF AMPLIFIER/ DEMODULATOR WITH MUTING



* T1:20 Turns Biflar No. 36 Wire on 1/2-Watt Resistor Body (For 10.7 MHz)
** Part of NE510N

Figure 9-54

the muting gate. Gating is accomplished by applying the demodulated FM output through the 1N457 diode and by biasing the diode on and off as follows: During periods with no input applied, Q1 is shut off and Q2 conducts. Therefore, the diode is effectively back biased since its anode potential developed by the 10k resistors across the power supply is approximately +13.5V. When an input is applied to the circuit, Q1 is turned on and Q2 shuts off, reducing its collector potential below 9V. Thus, the diode is forward biased and the demodulated IF output is gated through to the circuit output.

Muting threshold adjustment is accomplished using the 2.5k potentiometer. Transistor Q3 is used as a bias generator for the differential pair, Q1 and Q2. In turn, the bias of Q3 is obtained from internal PLL bias points at pins 12 and 13. Thus, the muting gate will track the PLL over wide temperature variations.

FM Demodulator (560N)

When used as a FM demodulator, the 560N phase locked loop requires selection of external components and/or circuits to create the desired response. The areas to be considered are:

a. Input signal conditioning
b. Tuning—VCO frequency
c. Low pass filter selection/gain adjustment
d. Output swing
e. Tracking range adjustment
f. De-emphasis network selection

Figure 9-55 illustrates schematically a typical FM demodulator with IF amplifier and limiter using the 560N PLL. The amplitude of the input signal has a pronounced effect on the operation. For the tracking range to be constant, the input signal level should be greater than 2mVrms. In addition, AM rejection diminishes at higher signal levels and drops to less than 20dB for signals greater than 30mV. If either the tracking range or AM rejection is critical, the input signal should be conditioned to be in the 2 to 10mV range, using either a limiter or a combination limiter-amplifier. This circuit should limit at the smallest input voltage that is expected.

The PLL is tuned by adjusting the VCO to the center frequency of the FM signal. This is accomplished by connecting a capacitor across pins 2 and 3. The capacitor value is determined using the equation $C_o \approx 300/f_o$, pF where f_o, the free-running VCO frequency, is in MHz. The exact value is not important as the internal resistors are only within ±10% of nominal value and fine tuning is normally required. Fine tuning may be accomplished by using a trimmer capacitor in parallel with C_o or by using a potentiometer connected across the power supply with the rotor connected to pin 6 through a 200Ω current limiting resistor.

The dc gain of the loop, which sets the lock range and threshold sensitivity, can be controlled by the placement of a resistance between pins 14 and 15, the low pass filter terminals. A low pass filter connected to these terminals controls the capture range or selectivity of the loop. In basic terms, it may be said that the low pass filter sets the bandwidth of the demodulated information which will be obtained. For most applications, a single capacitor connected between pins 14 and 15 will provide the required filtering. The capacitance value required can be approximated as follows:

(Equation 9-43)

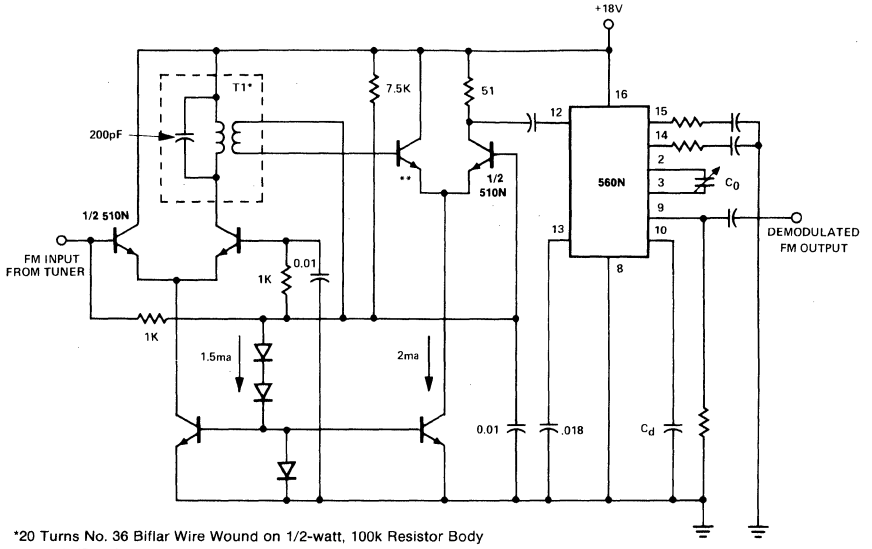
$$C \approx \frac{13.30}{f} \text{ mfd}$$

where f is the desired bandwidth in Hz. For example, if the desired information bandwidth is 15kHz, the required low pass filter capacitance will be:

(Equation 9-44)

$$C \approx \frac{13.30}{15000} = 885\text{pF}$$

TYPICAL FM DEMODULATOR WITH IF AMPLIFIER AND LIMITER USING THE 560N



*20 Turns No. 36 Biflar Wire Wound on 1/2-watt, 100k Resistor Body
**Part of NE501N

Figure 9-55

The output swing is a function of the frequency deviation of the incoming signal, and is approximately 0.3Vp-p for ±1% deviation. For example, a standard 10.7MHz IF frequency has a deviation of ±75kHz; therefore, the percentage deviation equals

$$\frac{\pm 0.75 \times 100}{10.7} = \pm 0.7\%$$

and the output voltage will be

$$0.3\text{V p-p} \times \frac{.7\%}{1\%} = .21\text{V p-p},$$

or 74mVrms for 100% modulation.

The de-emphasis network requires an external capacitor from pin 10 to ground. This capacitor C_d and the 8000Ω internal resistance should produce a time constant of approximately 75μs for standard FM broadcast demodulation. The value of the de-emphasis capacitor for this application is determined by the following formula:

$$C_d = \frac{75 \times 10^{-6}}{8000} = 0.0094\text{mfd}$$

For most applications, a 0.01mfd value would be satisfactory since the manufacturing tolerance of the resistor is on the order of 20%.

Phase Locked AM Receiver (561N)

The Signetics 561N can be used as an AM detector/receiver. AM detection is accomplished as illustrated in the block diagram of Figure 9-56a. The phase locked loop is locked to the signal carrier frequency and its VCO output is used to provide the local oscillator signal for the product detector or synchronous demodulator. The PLL locks to its input signal with a constant 90° phase error. The amplitude of the signal at the output of the product detector is a function of the phase relationship of the carrier of the incoming signal and the local oscillator; it will be a maximum when the carrier and local oscillator are in phase or 180° out of phase and a minimum when they are in quadrature. It is, therefore, necessary to add a 90° phase shift network in the system to compensate for the normal PLL phase shift. The 561 is designed for this to be incorporated between the signal input and the input to the phase comparator input, pin 12 or pin 13.

Connection as an AM detector/receiver is given in Figure 9-56b. The bypass and coupling capacitors should be selected for low impedance at the operating frequency. C_o is selected to make the VCO oscillate at the frequency to be received and C_x is selected, in conjunction with the output resistance (8000Ω) and the load resistance, to roll off the audio output for the desired bandwidth.

PHASE LOCKED AM RECEIVER

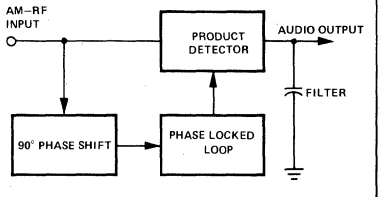


Figure 9-56a

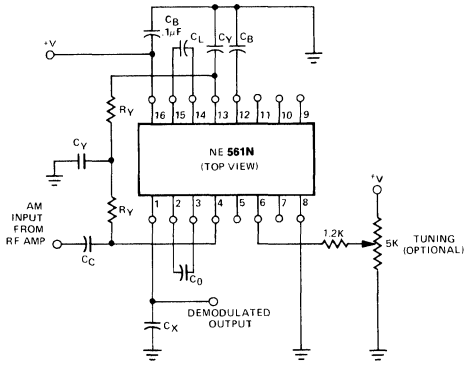
The phase shift network may be determined from the following equations:

(Equation 9-45)

$$C_y = \frac{1.3 \times 10^{-4}}{f_c}\ \text{pF}$$

where f_c is the carrier frequency of the signal to be received and $R_y = 3000\Omega$. A receiver for standard AM reception is easily constructed using the circuit of Figure 9-56b. Its operating range will be from 550kHz to 1.6MHz. All bypass and coupling capacitors are 0.1mfd. C_y is selected using a frequency which is the geometric mean of the limits of the frequencies which are to be received.

PHASE LOCKED AM RECEIVER



C_B = Bypass Capacitor
C_C = Coupling Capacitor

Figure 9-56b

(Equation 9-46)

$f_c = \sqrt{f_{hi} f_{lo}} = 1.6 \times 0.55 = .94\text{MHz}$

then:

$$C_y = \frac{1.3 \times 10^{-4}}{.94 \times 10^{-6}} = 135\text{pF}$$

The low pass filter for the loop, C_L, is not critical for no information is being derived directly from the loop error signal and one need only be assured of stable loop operation. A .01mfd capacitor was found to be adequate.

Tuning may be accomplished in several ways. The simplest method uses a variable capacitor as C_o. It should be trimmed so that when set for minimum capacitance, the VCO frequency is approximately 1.6MHz. The capacitance used may be obtained from the following formula:

$$C_o \approx \frac{300\text{pF}}{f_o} \quad \text{where } f_o \text{ is in MHz.}$$

Application of this formula shows that the minimum capacitance should be about 180pF and the maximum capacitance should be 550pF. A second tuning method utilizes the fine tuning input, pin 6. When current is inserted or removed from this pin, the VCO frequency will change, thereby tuning the receiver. Select C_o, when the current at pin 6 is zero, to make the VCO operate at the mean frequency used in the phase shift network calculation (940kHz). The complete standard AM broadcast band may now be tuned with one potentiometer. The resistor in series with the arm of the potentiometer is selected to give the desired tuning range and will be about 1200Ω when an 18V power supply is used.

For operation, this receiver requires an antenna and a good grounding system. Operation may be improved by including a broadband untuned RF amplifier, but care should be used to ensure that the phase locked loop is not overdriven, e.g. input signals should be kept less than 0.5Vrms.

IF STAGE WITH AGC AND AM/FM DETECTION (561N)

The circuit shown in Figure 9-57 is basically an IF strip at 10.7MHz employing a buffer amplifier, two stages of gain, two ganged stages of AGC and an AGC summing amplifier. A single 561N PLL serves as both the AM and FM detector. Input sensitivity to insure lockup for either AM or FM demodulation is approximately 10μV. The input level to the 561N is held level at 305mVp-p during input amplitude excursion from 10μV to 120mVp-p. Potentiometer R_{AGC} is adjusted at no input for a quiescent dc voltage (pin 6 of amplifier μA741) of -90mV. This presets the MC1496 multipliers at a maximum gain condition. The gain is slowly reduced as the RF input level rises and full AGC action begins.

The bandwidth of linear demodulation of AM is 1Hz to 4.5Hz and of FM is 1Hz to 36kHz.

IF gain adjustment can be provided with the installation of a potentiometer between pins 4 and 9 of either (or both) of the μA733, a zero ohm setting insuring maximum gain.

The addition of a conventional converter front-end and audio driver stages completes the circuitry for a receiver.

Translation Loop for Precise FM (561N, 562N)

A translation loop mixes the output of two oscillators and produces a signal whose frequency is equal to the sum or difference of the two. In the most useful application of this circuit, one oscillator is a precise crystal-controlled oscillator and the second is a low frequency voltage-controlled oscillator so that the loop output is a FM signal whose center frequency is slightly offset from the crystal oscillator frequency. Since the offset oscillator supplies only a small percentage of the final output frequency, it need not be as precise as the crystal oscillator.

Such a loop is shown in Figure 9-58a. The VCO is driven until the filtered low frequency component of the PD2 output is equal to the offset frequency f_m. When this occurs, lockup is achieved and the VCO output is either $f_R + f_m$ or $f_R - f_m$. By adjusting the VCO free-running slightly above f_m, the latter case can be eliminated. If f_m is frequency modulated, then the output will also be frequency modulated since it has the same absolute deviation.

Figure 9-58b shows a translation loop made from a 561N and 562N. It is designed to produce a 4.5MHz signal with a deviation of ±25kHz. The 561N serves as the VCO and PD1; the 562N serves as the crystal oscillator and PD2. A 4.400MHz crystal controls the reference frequency f_R. The offset frequency f_m is 100kHz frequency modulated ±25kHz at a modulation frequency of 400Hz. The accuracy of the output frequency is that of the reference oscillator plus that of the offset oscillator; since f_m is a small percentage (2%) of f_R, its stability can be considerably less than that of the crystal oscillator. In this case, f_m can be provided by a 566 VCO modulated, if desired, by a second 566. (The triangle wave 566 output results in a constant df/dt.)

Special layout precautions are required to be sure that no high frequency coupling occurs via grounds or power supply lines. The circuit is adjusted by trimming the 562 VCO trimmer capacitor until the beat note present at test point 1 has the same frequency as f_m throughout the deviation range (f_m can be deviated by hand or very slowly, say, at a 1Hz rate, to observe that the beat note does not break up during sweep. If the beat note is lost at either extreme, adjust the VCO trimmer. If the full deviation cannot be obtained, decrease the 562 low pass filter capacitor slightly. Connect a counter to the output to be sure the loop is locked to $f_R + f_m$ and not $f_R - f_m$ (unless the latter is desired).

IF GAIN STAGE WITH AGC AND AM/FM DETECTION

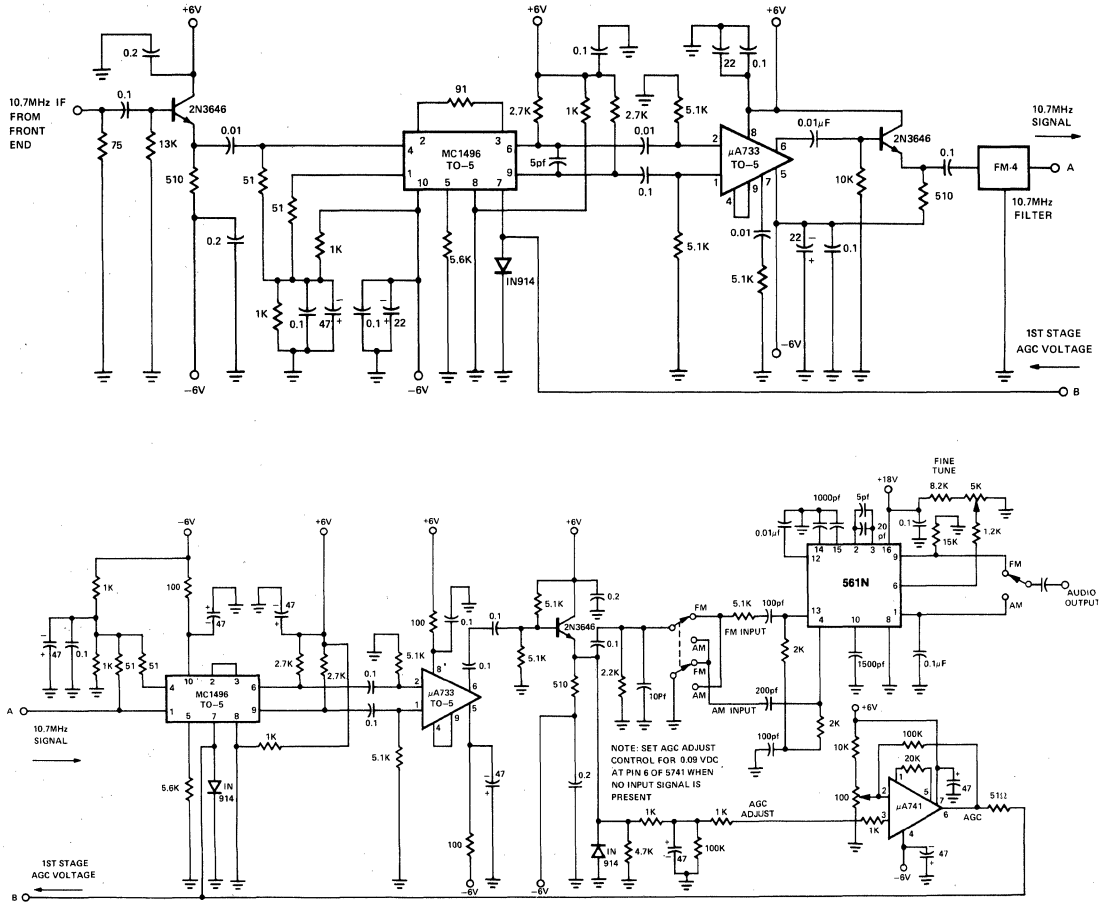


Figure 9-57

Naturally, the component values given may be altered for other applications. Note that as f_m is made a smaller and smaller percentage of the total output frequency, it becomes difficult to prevent locking in the $f_R - f_m$ mode since the 562 lock range will likely include both $f_R - f_m$ and $f_R + f_m$. However, if f_m is made too large a portion of the output frequency, then overall stability suffers unless f_m is also quite precise.

Phase Locked FSK Demodulators (560N, 565)

FSK refers to data transmission by means of a carrier which is shifted between two preset frequencies. This frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the "0" and "1" states (commonly called space and mark) of the binary data signal.

TRANSLATION LOOP FOR PRECISION TV INTERMEDIATE—FREQUENCY FM GENERATOR

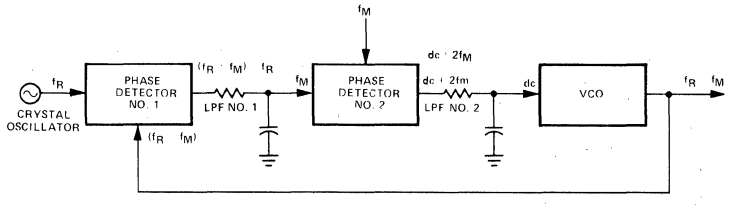


Figure 9-58a

The 560N phase locked loop can be used as a receiving converter to demodulate FSK audio tones and to provide a shifting dc voltage to initiate mark or space code elements. The PLL can replace the bulky audio filters and undependable relay circuits previously used for this application. Connection of the 560N PLL as a FSK demodulator is illustrated in Figure 9-59.

The system functions by locking-on and tracking the output frequency of the receiver. The demodulator frequency shift appears at pin 9 as a direct-current voltage of

TRANSLATION LOOP FOR PRECISION TV INTERMEDIATE—FREQUENCY FM GENERATOR

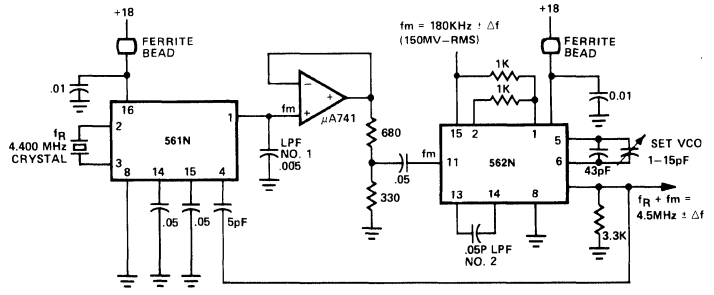


Figure 9-58b

FSK DEMODULATOR USING 560N

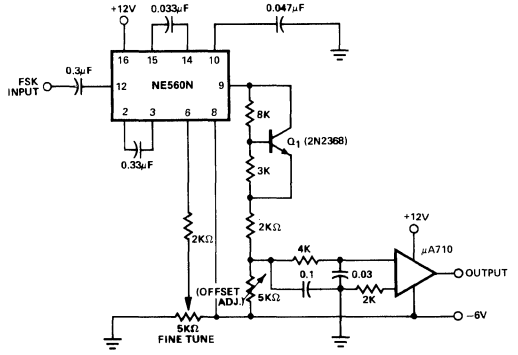


Figure 9-59

about 60mV amplitude and must be amplified and signal-conditioned to interface with the printer. The input voltage at pin 12 should be from 30mV to 2V peak-to-peak, square or sine wave. Pin 10, the de-emphasis terminal, is used for band-shaping. The capacitor connected between this terminal and ground bypasses unwanted high frequency noise to ground. Pin 9 is the output (approximately 60mVdc) which is amplified, conditioned and fed to a voltage comparator amplifier (μA710) to provide the proper voltages for interfacing with the printer. This specific circuit was designed to match the Bell 103C and 103D Data Phones. When modifying this circuit to accommodate other systems, maintain the resistance to ground from pin 9 at approximately 15KΩ. Pins 3 and 2 are the connections for the external capacitor that determine the free-running frequency of the VCO. The 0.33μF value indicated provides a VCO frequency, f_o, of approximately 1060Hz. The value of the timing capacitor can be calculated by use of the following equation:

(Equation 9-48)

$$C_o = \frac{300pF}{f_o} \quad \text{where } f_o \text{ is in hertz.}$$

The output has a swing of 2V peak-to-peak, over a 0 to 600 baud input FSK rate, with less than 10% jitter at the comparator output. The circuit is operative over a temperature range of 0° to 75°C with a total drift of approximately 100mV over the temperature range.

A simple scheme using the 565 to receive FSK signals of 1070Hz and 1270Hz is shown in Figure 9-60. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output.

The loop filter capacitor C2 is chosen to set the proper overshoot on the output and a three-stage RC ladder filter is used to remove the sum frequency component. The band edge of the ladder filter is chosen to be approximately half-way between the maximum keying rate (300 baud or bits per second, or 150Hz) and twice the input frequency (about 2200Hz). The free-running frequency should be adjusted (with R1) so that the dc voltage level at the output is the same as that at pin 6 of the loop. The output signal can now be made logic compatible by connecting a voltage comparator between the output and pin 6.

The input connection is typical for cases where a dc voltage is present at the source and, therefore, a direct connection is not desirable. Both input terminals are returned to ground with identical resistors (in this case, the values are chosen to achieve a 600Ω input impedance).

A more sophisticated approach primarily useful for narrow frequency deviations is shown in Figure 9-61. Here, a constant current is injected into pin 8 by means of transistor Q1. This has the effect of decreasing the lock range and increasing the output voltage sensitivity to the input frequency shift. The basis for this scheme is the fact that the output voltage (control voltage for VCO) controls only the current through R1, while the current through Q1 remains constant. Thus, if most of the capacitor charging current is due to Q1, the current variation due to R1 will be a small percentage of the total charging current and, consequently, the total frequency deviation of the VCO will be limited to a small percentage of the center frequency. A 0.25mfd loop filter capacitor gives approximately 30% overshoot on the output pulse, as seen in the accompanying photographs.

FSK DECODER USING THE 565

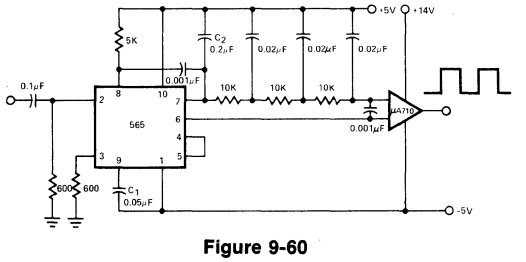


Figure 9-60

FSK DECODER WITH EXPANDED 565 OUTPUT VOLTAGE RANGE

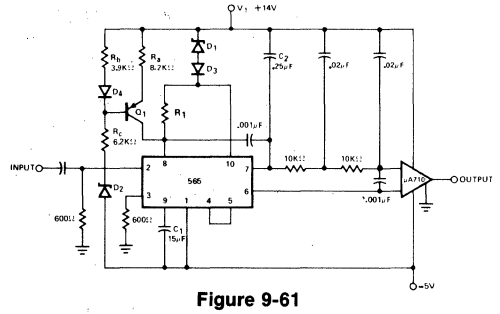


Figure 9-61

100 BAUD FSK DECODING

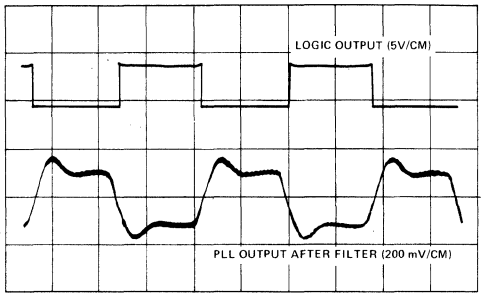


Figure 9-62a

200 BAUD FSK DECODING

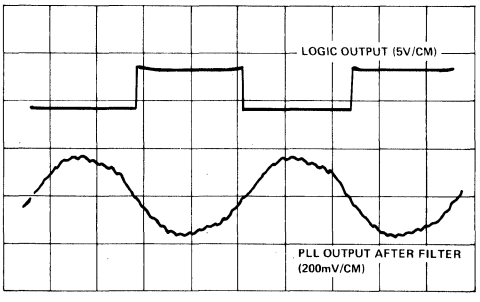


Figure 9-62b

300 BAUD FSK DECODING

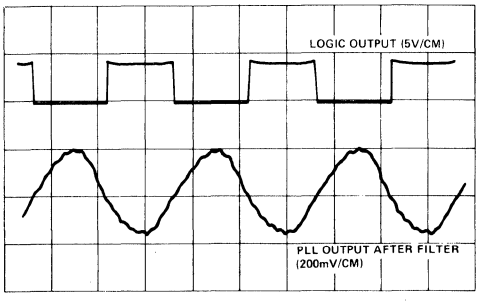


Figure 9-62c

The output is then filtered with a two-stage RC ladder filter with a band edge chosen to be approximately 800Hz (approximately half-way between the maximum keying rate of 150Hz and twice the carrier frequency). The number of stages on the filter can be more or less depending on the degree of uncertainty allowable in the comparator output pulse. Two small capacitors (typically 0.001mfd) are connected between pins 8 and 7 of the 565 and across the input of the comparator to avoid possible oscillation problems.

For best operation, the free-running VCO frequency should be adjusted so that the output voltage (corresponding to the input frequencies of 1070Hz and 1270Hz swings equally to both sides of the reference voltage at pin 6. This can be easily done by adjusting the center frequency of the VCO so that the output signal of the μA710 comparator has a 50% duty cycle. It is usually necessary to decouple pin 6 with a large capacitor connected to the positive supply in order to obtain a stable reference voltage for the μA710 comparator.

Figure 9-62 shows the output of the μA710 comparator and the output of the 565 phase locked loop after the filter at rates of 100, 200 and 300 baud, respectively.

Analog Light-Coupled Isolators (565, 567)

The analog isolator shown in Figure 9-63a is basically a FM transmission system with light as the transmission medium. Because of the high degree of electrical isolation achieved, low-level signals may be transmitted without interference by great potential difference between the sending and receiving circuits. The transmitter is a 565 used as a VCO with the input applied to the VCO terminal 7. Since the light emitting diode is driven from the 565 VCO output, the LED flashes at a rate proportional to the input voltage. The receiver is a photo transistor which drives an amplifier having sufficient gain to apply a 200mV peak-to-peak signal to the input of the receiving 565, which then acts as a FM detector with the output appearing at pin 7. Since the output has a twice carrier frequency ripple, it is best to keep the carrier frequency as high as possible (say, 100 times the highest modulation frequency). Because of the excellent temperature stability of the 565, drift is minimal even when dc levels are being transmitted. If operation to dc is not required, the output of the receiver can be capacitively coupled to the next stage. Also, a 566 can be used as the transmitter.

Figure 9-63b shows that the 567 may be used in the same manner when operation from 5V supplies is required. Here, the output stage of the 567 is used to drive the LED directly. When the free-running frequency of the receiving 567 is the same as that of the transmitting 567, the non-linearity of the two controlled oscillator transfer functions cancel so that highly linear information transfer results.

Figure 9-64 is an oscillogram of the input and output of the Figure 9-63a circuit. The output can easily be filtered to remove the sum frequency component.

PHASE MODULATORS

If a phase locked loop is locked onto a signal at the center frequency, the phase of the VCO will be 90° with respect to the input signal. If a current is injected into the VCO terminal (the low pass filter output), the phase will shift sufficiently to develop an opposing average current out of the phase detector so that the VCO voltage is constant

LIGHT—COUPLED ANALOG ISOLATORS

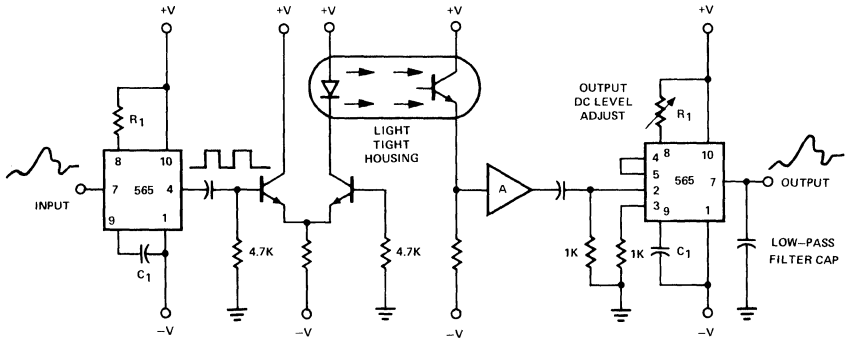


Figure 9-63a

LIGHT—COUPLED ANALOG ISOLATORS

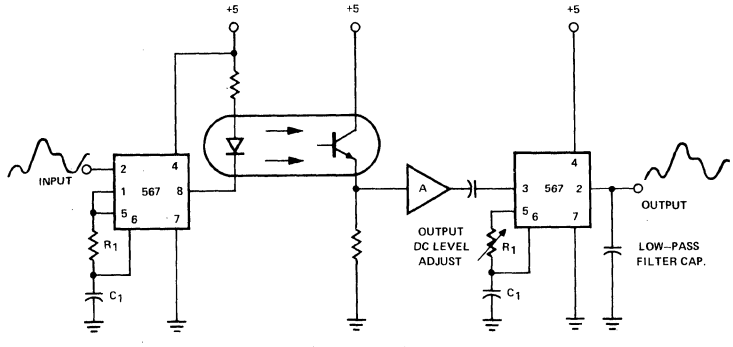


Figure 9-63b

and lock is maintained. When the input signal amplitude is low enough so that the loop frequency swing is limited by the phase detector output rather than the VCO swing, the phase can be modulated over the full range of 0 to 180°. If the input signal is a square wave, the phase will be a linear function of the injected current.

A block diagram of the phase modulator is given in Figure 9-65a. The conversion factor K is a function of which loop is used, as well as the input square wave amplitude. Figure 9-65b shows an implementation of this circuit using the 567.

WAVEFORMS OF LIGHT-COUPLED ANALOG ISOLATOR (CIRCUIT A)

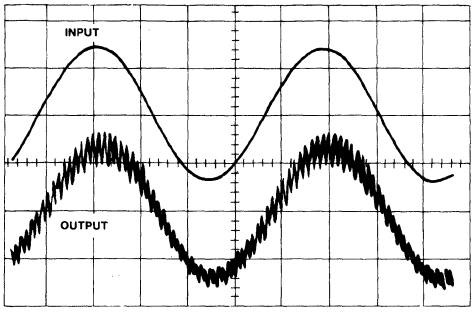


Figure 9-64

PHASE MODULATION USING THE PLL

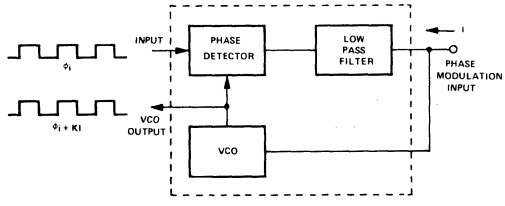


Figure 9-65a

PHASE MODULATION USING THE PLL

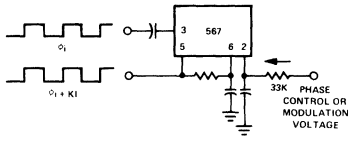


Figure 9-65b

Dual Tone Decoders (567)

Two integrated tone decoders can be connected (as shown in Figure 9-66a) to permit decoding of simultaneous or sequential tones. Both units must be on before an output is given. R1C1 and R1C1 are chosen, respectively, for tones 1 and 2. If sequential tones (1 followed by 2) are to be decoded, then C3 is made very large to delay turn off of unit 1 until unit 2 has turned on and the NOR gate is activated. Note that the wrong sequence (2 followed by 1) will not provide an output since unit 2 will turn off before unit 1 comes on. Figure 9-66b shows a circuit variation which eliminates the NOR gate. The output is taken from unit 2, but the unit 2 output stage is biased off by R2 and CR1 until activated by tone 1. A further variation is given in Figure 9-66c. Here, unit 2 is turned on by the unit 1 output when tone 1 appears, reducing the standby power to half. Thus, when unit 2 is on, tone 1 is or was present. If tone 2 is now present, unit 2 comes on also and an output is given. Since a transient output pulse may appear during unit 1 turn-on, even if tone 2 is not present, the load must be slow in response to avoid a false output due to tone 1 alone.

High Speed, Narrow Band Tone Decoder

The circuit of Figure 9-66a may be used to obtain a fast, narrow band tone decoder. The detection bandwidth is achieved by overlapping the detection bands of the two tone decoders. Thus, only a tone within the overlap portion will result in an output. The input amplitude should be greater than 70mVrms at all times to prevent detection band shrinkage and C2 should be between $130/f_o$ and $1300/f_o$ mfd where f_o is the nominal detection frequency. The small value of C2 allows operation at the maximum speed so that worst-case output delay is only about 14 cycles.

Touch-Tone® Decoder (567)

Touch-Tone® decoding is of great interest since all sorts of remote control applications are possible if you make use of the encoder (the push-button dial) that will ultimately be part of every phone. A low cost decoder can be made as shown in Figure 9-67. Seven 567 tone decoders, their inputs connected in common to a phone line or acoustical coupler, drive three integrated NOR gate packages. Each tone decoder is tuned, by means of R1 and C1, to one of the seven tones. The R2 resistor reduces the bandwidth to about 8% at 100mV and 5% at 50mVrms. Capacitor C4 decouples the seven units. If you are willing to settle for a somewhat slower response at low input voltage (50 to 100mVrms), the bandwidth can be controlled in the normal manner by selecting C2, thereby eliminating the seven R2 resistors and C4.

The only unusual feature of this circuit is the means of bandwidth reduction using the R2 resistors. In the Alternate Method of Bandwidth Reduction, Figure 9-68, an external resistor R_A can be used to reduce the loop gain and, therefore, the bandwidth. Resistor R2 serves the same function as R_A except that instead of going to a voltage divider for dc bias it goes to a common point with the six other R2 resistors. In effect, the five 567s which are not being activated during the decoding process serve as bias voltage sources for the R2 resistors of the two 567s which are being activitated. Capacitor C4 decouples the ac currents at the common point.

Figure 9-67 shows several additions to the "normal" method of tone decoding. The reduced capture time (shown dotted around the 697Hz decoders) and reduced unlock time (shown with the 1477Hz decoder) can be added to allow greater response time to the decoder at the expense of additional components. The addition of resistor R2 can be of greater advantage when selected such that the bandwidth of each decoder can be individually adjusted.

DETECTION OF TWO SIMULTANEOUS OR SEQUENTIAL TONES

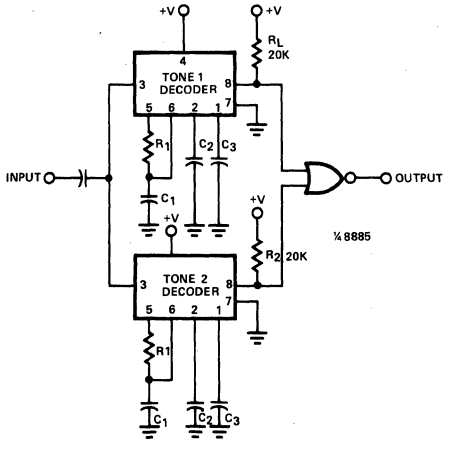


Figure 9-66a

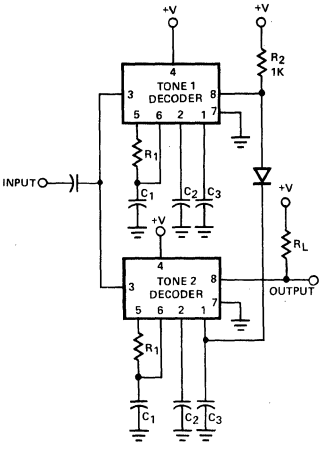


Figure 9-66b

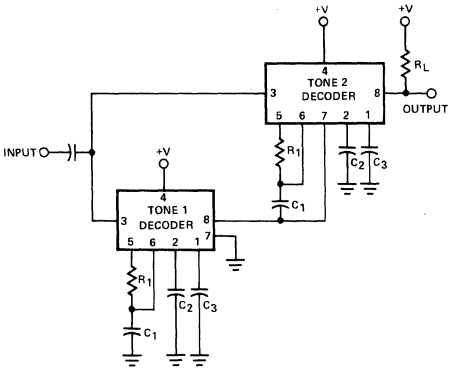


Figure 9-66c

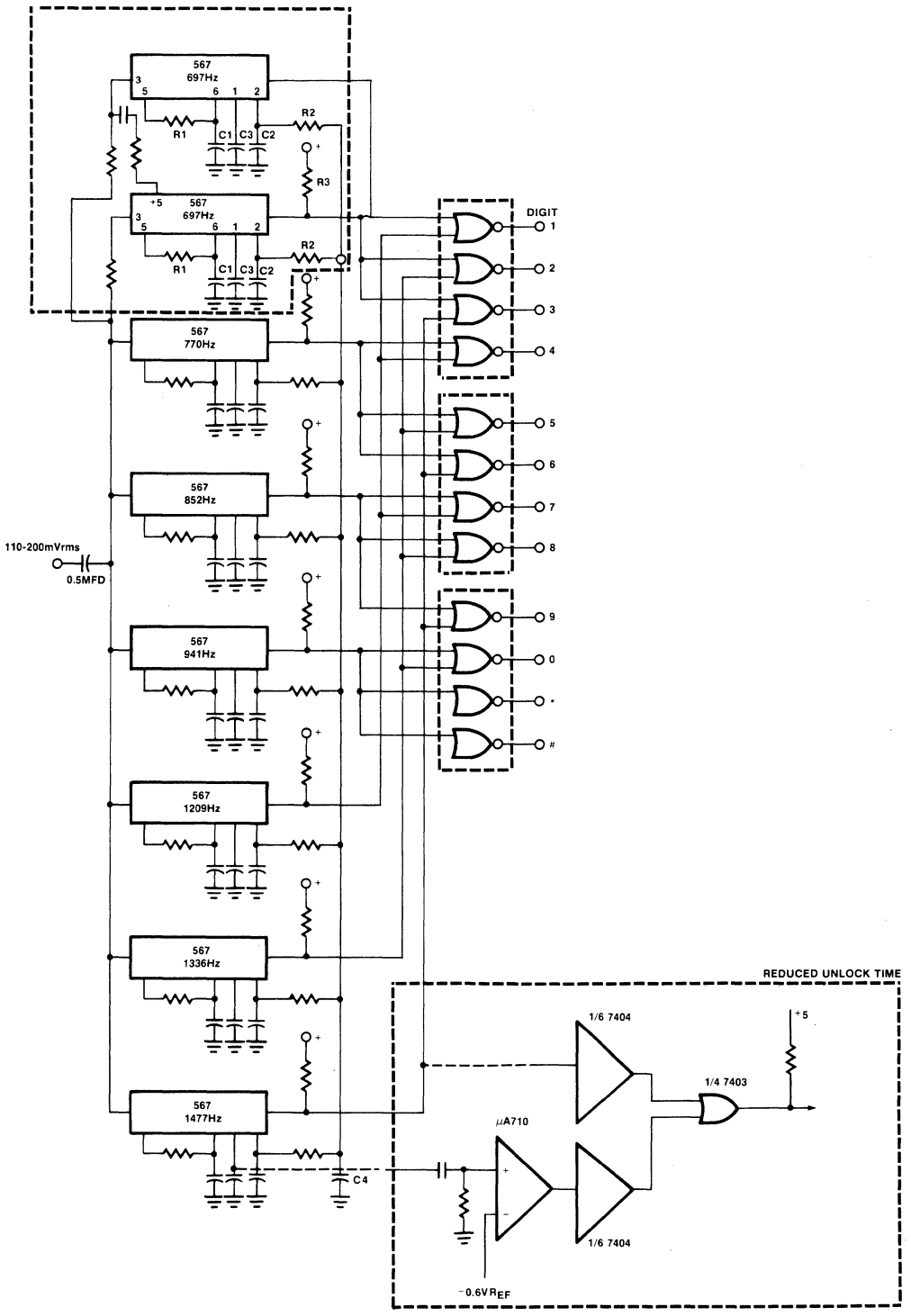
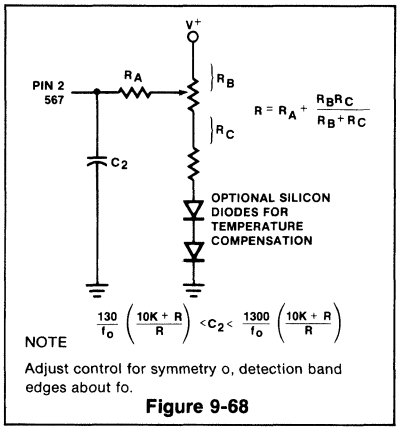

REDUCED CAPTURE TIME MODULE
567
697Hz
R1
R2
C1
C3
C2
R3
+5
567
697Hz
567
770Hz
567
852Hz
567
941Hz
567
1209Hz
567
1336Hz
567
1477Hz
DIGIT
1
2
3
4
5
6
7
8
9
0
*
#
110-200mVrms
0.5MFD
C4
REDUCED UNLOCK TIME
1/6 7404
1/4 7403
μA710
1/6 7404
+5
-0.6VREF

Figure 9-67



NOTE

Adjust control for symmetry o, detection band edges about fo.

Figure 9-68

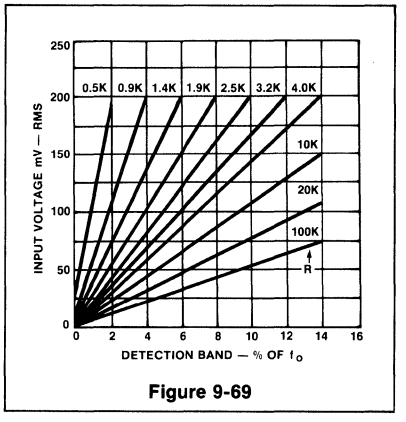


Figure 9-69

The curve in Figure 9-69 indicates that in order to obtain more control of the decoder the resistor R2 should be less than 10K.

The reduced capture time technique is described below.

Typical capture time for a phase lock loop can be as long as 10 cycles of incoming signal. For a frequency of 697Hz (low tone of a touch tone system) this ends up in a delay time of up to 15 milliseconds. Lower frequencies result in much longer delays. In order to relieve these extended delays and to use external components (loop filter and low pass filter) which more closely match the design criteria, a system such as shown in Figure 9-67 is used.

The output of one of the tone decoders is phase shifted by 90 degrees at the given tone and fed into the second tone decoder. This forces the second tone decoder VCO to be phase shifted 90 degrees from the reference signal. The incoming signal is then fed to both devices. The maximum phase shift of the signal will be 45 degrees resulting in a 6dB reduction in capture time.

The approach can be further expanded if a third device is used, with each loop phase shifted 30 degrees from each other.

Improved noise immunity can be achieved by adding resistors across pins 1 and 4. A 50kΩ resistor will improve the noise threshold by approximately 2-3dB. In effect the sensitivity of the system is reduced.

Latch up circuity is included in this set up. The outputs of each device are wire "OR" together.

Reduced Release Time

Due to the nature of the output filter capacitor and the internal resistor, the decode unlatch time can be as long as 40ms. This time can be reduced to less than 1/4 of a cycle of the incoming tone by incorporating the circuitry shown in Figure 9-67. The output of the 567 is "added" together along with the output of a comparator. The comparator is triggered by the output of the 567 filter section. This output responds (within 1 cycle) of the incoming signal. The net result is the increased unlatch time of the decoder.

Low Cost Frequency Indicator (567)

Figure 9-70 shows how two tone decoders set up with overlapping detection bands can be used for a go/no-go frequency meter. Unit 1 is set 6% above the desired sensing frequency and unit 2 is set 6% below the desired frequency. Now, if the incoming frequency is within 13% of the desired frequency, either unit 1 or unit 2 will give an output. If both units are on, it means that the incoming frequency is within 1% of the desired frequency. Three light bulbs and a transistor allow low cost read-out.

CRYSTAL-STABILIZED PHASE LOCKED LOOP

Figure 9-71a shows the 560N connected as a tracking filter for signals near 10MHz. The crystal keeps the free-running frequency at the desired value. Figure 9-71b gives the lock and capture range as a function of input amplitude. An emitter follower has been added to the normal VCO output to prevent pulling the loop off frequency.

FREQUENCY METER WITH LOW-COST LAMP READOUT

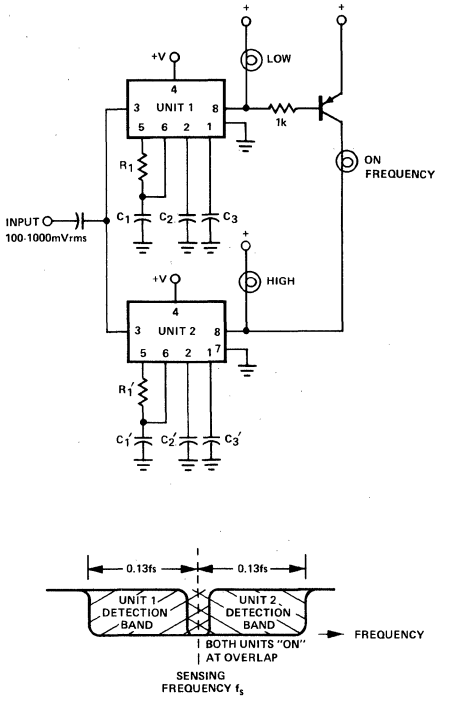


FIGURE 9-70

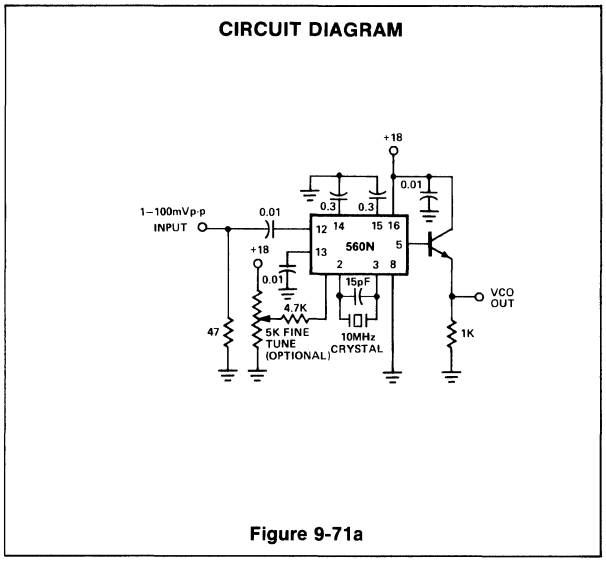


Figure 9-71a

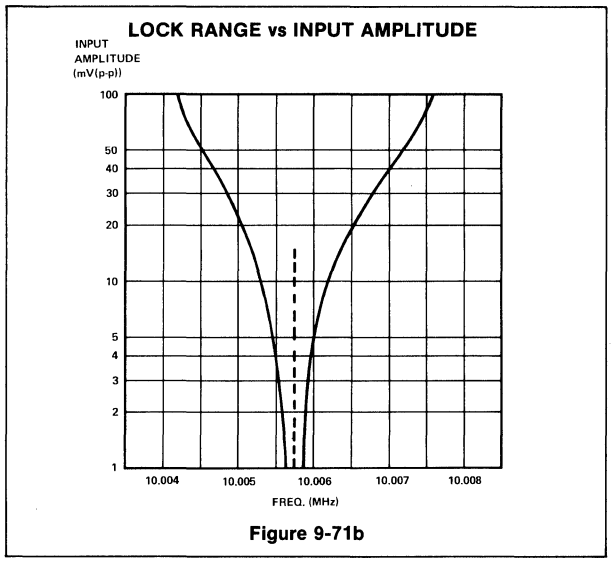


Figure 9-71b

Ramp Generators (566)

Figure 9-72 shows how the 566 can be wired as a positive or negative ramp generator. In the positive ramp generator, the external transistor driven by the pin 3 output rapidly discharges C1 at the end of the charging period so that charging can resume instantaneously. The pnp transistor likewise rapidly charges the timing capacitor C1 at the end of the discharge period. Because the circuits are reset so quickly, the temperature stability of the ramp generator is excellent. The period τ is $1/2f_O$ where f_O is the 566 free-running frequency in normal operation. Therefore,

(Equation 9-49)

$$\tau = \frac{1}{2f_O} = \frac{R_T C1 V+}{5(V+ - V_C)}$$

where V_C is the bias voltage at pin 5 and R_T is the total resistance between pin 6 and V+. Note that a short pulse is available at pin 3. (Placing collector resistance in series with the external transistor collector will lengthen the pulse.)

Sawtooth and Pulse Generator (566)

Figure 9-73 shows how pin 3 output can be used to provide different charge and discharge currents for C1 so that a sawtooth output is available at pin 4 and a pulse at pin 3. The pnp transistor should be well saturated to preserve good temperature stability. The charge and discharge times may be estimated by using the formula

(Equation 9-50)

$$\tau = \frac{R_T C1 V+}{5(V+ - V_C)}$$

where R_T is the combined resistance between pin 6 and V+ for the interval considered.

Triangle-To-Sine Converters

Conversion of triangular wave shapes to sinusoids is usually accomplished by diode-resistor shaping networks, which accurately reconstruct the sine wave segment by segment. Two simpler and less costly methods may be used to shape the triangle waveform of the 566 into a sinusoid with less than 2% distortion.

The first scheme (Figure 9-74a) uses the nonlinear I_{DS}—V_{DS} transfer characteristic of a p-channel junction FET to shape the triangle waveform. The second scheme (Figure 9-74b) uses the non-linear emitter

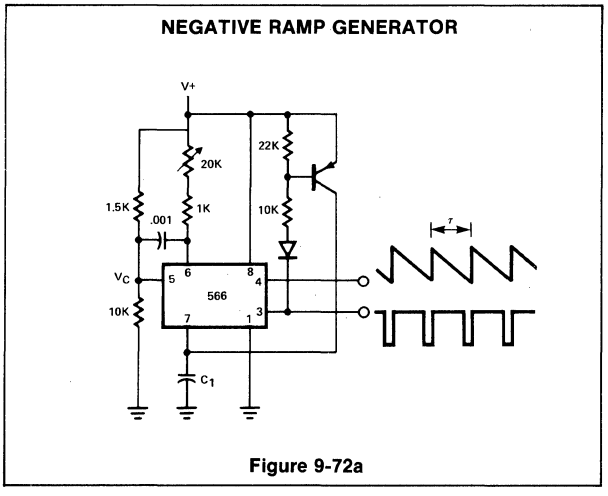


Figure 9-72a

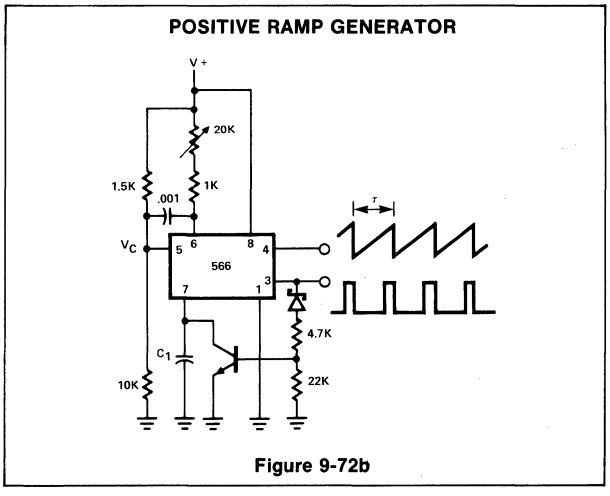


Figure 9-72b

POSITIVE SAWTOOTH AND PULSE GENERATOR

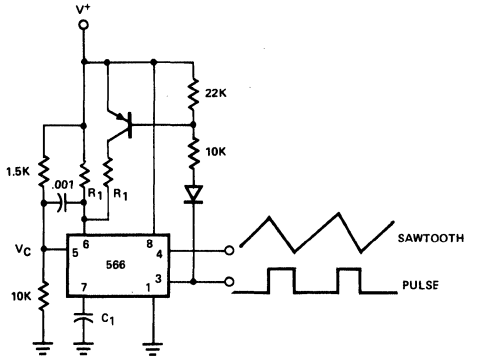


Figure 9-73a

NEGATIVE SAWTOOTH AND PULSE GENERATOR

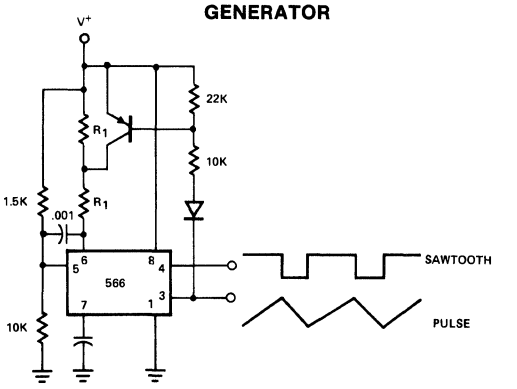


Figure 9-73b

FET TRIANGLE-TO-SINE CONVERTER

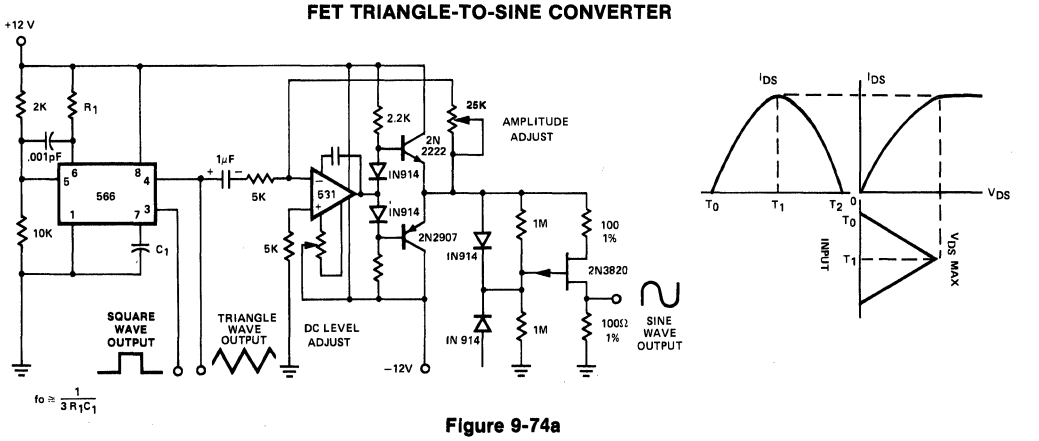


Figure 9-74a

base junction characteristic of the 511N for shaping.

In both cases, the amplitude of the triangle waveform is critical and must be carefully adjusted to achieve a low distortion sinusoidal output. Naturally, where additional waveform accuracy is needed, the diode-resistor shaping scheme can be applied to the 566 with excellent results since it has very good output amplitude stability when operated from a regulated supply.

Single Tone Burst Generator (566)

Figure 9-75 is a tone burst generator which supplies a tone for one-half second after the power supply is activated; its intended use is as a communications network alert signal. Cessation of the tone is accomplished by the SCR, which shunts the timing capacitor C1 charge current when activated. The SCR is gated on when C2 charges up to the gate voltage, which occurs in 0.5 seconds. Since only 70μA are available for triggering, the SCR must be sensitive enough to trigger at this level. The triggering current can be increased, of course, by reducing R2 (and increasing C2 to keep the same time constant). If the tone duration must be constant under widely varying supply voltage conditions, the optional Zener diode regulator circuit can be added, along with the new value for R2, R2 = 82K.

If the SCR is replaced by a npn transistor, the tone can be switched on and off at will at the transistor base terminal.

Low Frequency FM Generators (566)

Figures 9-76 and 9-77 show FM generators for low frequency (less than 0.5mHz center frequency) applications. Each uses a 566 function generator as a modulation generator and a second 566 as the carrier generator.

Capacitor C1 selects the modulation frequency adjustment range and C1 selects the center frequency. Capacitor C2 is a coupling capacitor which only needs to be large enough to avoid distorting the modulating waveform.

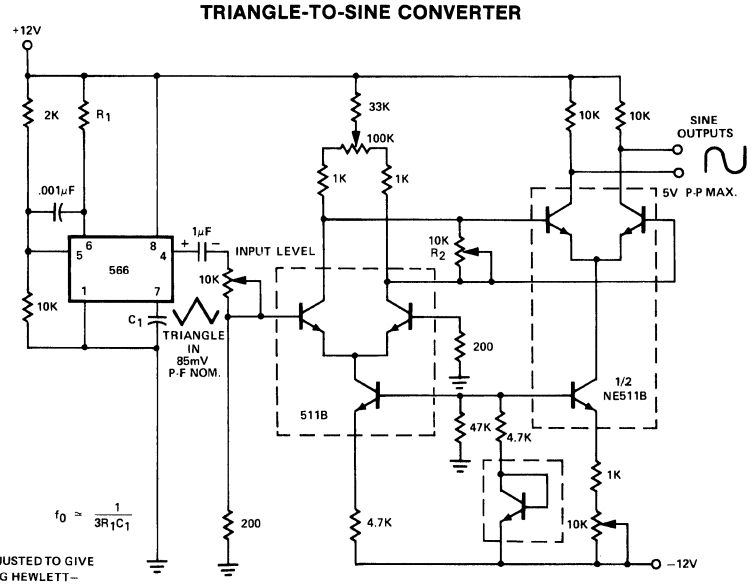
If a frequency sweep in only one direction is required, the 566 ramp generators given in this section may be used to drive the carrier generator.

Radio Frequency FM Generators (566, 560N)

Figure 9-78 shows how a 560N may be used as a FM generator with modulation supplied by a 566 function generator. Capacitor C1 is chosen to give the desired modulation range, C2 is large enough for undistorted coupling and C3 with its trimmer specifies the center frequency. The VCO output may be taken differentially or single ended.

A 561N or 562N with appropriate pin numbering changes may also be used in this application. If a sweep generator is desired, the 566 may be connected as a ramp generator (described elsewhere in this chapter).

TRIANGLE-TO-SINE CONVERTER



R1, R2, AND INPUT LEVEL MAY BE ADJUSTED TO GIVE LESS THAN 2% T.H.D. AT OUTPUT USING HEWLETT-PACKARD 333A DIST. ANALYZER.

Figure 9-74b

SINGLE BURST TONE GENERATOR

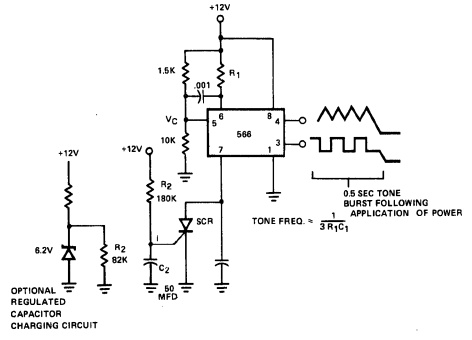


Figure 9-75

FREQUENCY MODULATED GENERATOR FOR SMALL DEVIATIONS (TO ±20%)

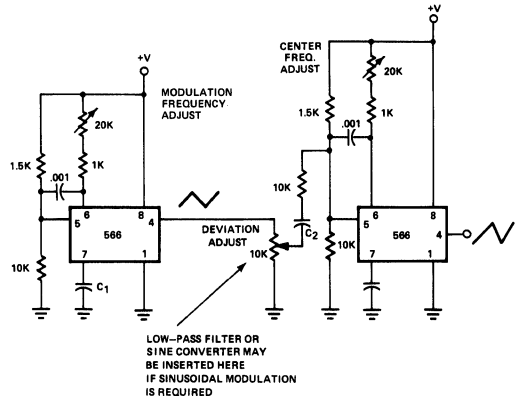


Figure 9-76

Precision Power Inverter (566, 540)

Figure 9-79 shows a precision 12Vdc to 115 Vac 100W inverter. Its triangular output is derived from the 566 function generator, providing a high degree of frequency stability (±.02%° C). The 540 power driver is used to drive the power output stage. Because of third harmonic attenuation in the transformer, the output is very close to a pure 60Hz sine wave.

DESIGN IDEAS FOR USING PHASE LOCKED LOOPS

The following design ideas were drawn mainly from the Signetics-EDN Phase Locked Loop Contest. These circuits should be viewed as design suggestions only since Signetics has not verified their operating characteristics. In all cases, however, the principle of operation appears to be sound.

Quotation marks indicate quotes taken directly from the contest entry.

Aircraft VHF Omnidirectional Range (VOR) Receiver

Herbert F. Kraemer of Minneapolis, Minnesota, submitted the winning contest entry which uses one phase locked loop (562) as an AM detector, a second loop (565) as an

FREQUENCY MODULATED GENERATOR FOR LARGE DEVIATIONS (TO ±100%)

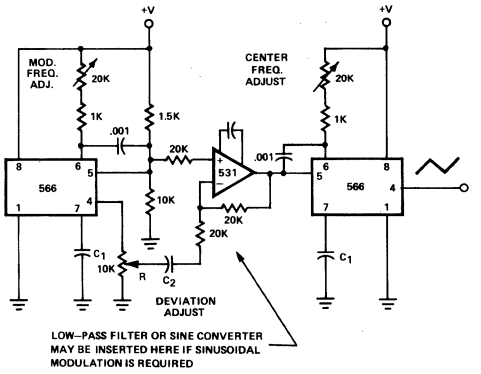


Figure 9-77

RF-FM GENERATOR

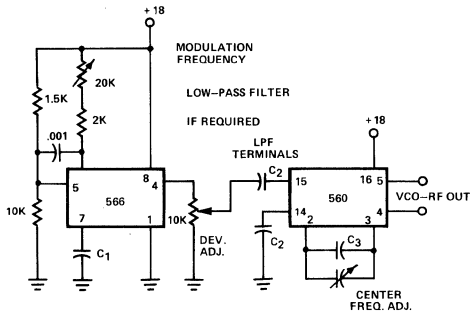


Figure 9-78

PRECISION 100 WATT POWER INVERTER

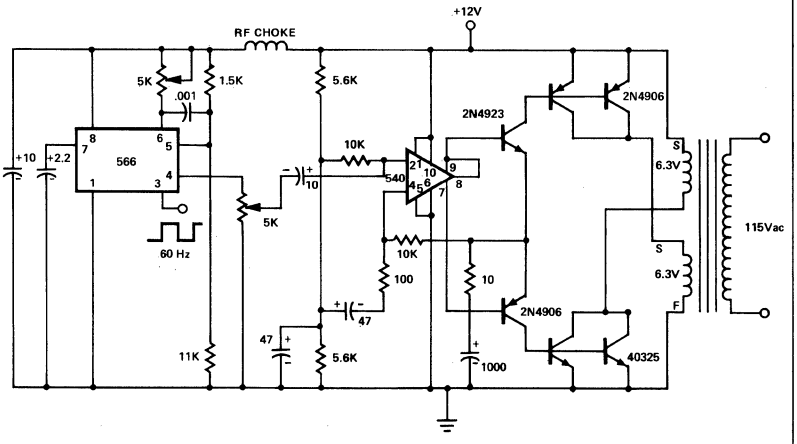


Figure 9-79

FM detector and a third loop (565) as a self-biased phase detector.

"The circuit is a new type of VOR (VHF omnidirectional range) receiver used in air navigation to determine an airplane's angular bearing with respect to a VOR transmitter located on the ground. The principles of the circuit allow any desired increase in accuracy, as compared to current units, with potential cost savings.

"A VOR station transmits in the VHF band (108—117.9MHz). Two signals are transmitted on the same carrier, i.e.,

1. A 30Hz reference signal which frequency modulates an audio frequency subcarrier of 9960Hz. This subcarrier then amplitude modulates the VHF carrier.
2. A 30Hz directional signal which amplitude modulates the VHF carrier.

"The latter signal varies in phase with respeat to the reference, depending on the bearing of the VOR station and the receiver. Both signals are in phase when the receiver is north of the transmitter and 180 degrees out of phase when the receiver is south.

"Current VOR receivers are specified to be accurate within a 1-2 degree bearing, but many pilots accept 4 degree errors. The major design problem is to produce a receiver which will measure phase differences to an accuracy of about 1 degree, throughout the entire 360 degree range."

Although analog quarter-square multipliers can be built to an accuracy of 0.01%, the simpler analog phase detectors are only accurate to 3-4°. This circuit uses the NE562 PLL to frequency multiply the two 30Hz signals, producing 60 and 120Hz signals. A digital method combines these signals, thereby dividing the entire range of bearings into eight 45° sectors. One of eight lights on the display will light, showing the pilot his approximate bearing. An analog method is then used to further determine the phase difference and the bearing within the given 45° sector. Extending the principle further, sectors of 22 1/2° could be used for improved accuracy.

This VOR receiver does not have the conventional to-from switch since it indicates directly throughout the entire 360° range. Confusion of 180° in bearing (going the wrong way) is impossible with this receiver.

System Description (References to Block Number—Figure 9-80)

Block 1. This is a standard VHF tuner.

Block 2. The NE561 is used for IF and AM detection.

Block 3. A low pass filter removes the 9960Hz subcarrier. It appears that a zero crossing detector is not needed to shape the input signal to the NE562.

Block 4. Frequency multiplier.

Block 5. High pass filter.

Block 6. FM detection of 30Hz signal.

Block 7. A calibration adjustment to compensate for any phase shifts throughout the circuit. A gain may be needed since the FM detector output is low.

Block 8. Another frequency multiplier.

Block 9. Standard ripple flip-flops for divide-by-two.

Block 10. A null principle is normally used in a VOR receiver so that the pilot can fly along a predetermined course, nulling the needle by turning his plane. To insure that the needle always reacts in the same direction for a given direction of error, even sectors are treated differently than odd sectors. The phase comparison is made with respect to C for *odd* sectors, and with respect to $\overline{C}$ for *even* sectors.

Block 11. "At the desired null, the two signals must be 90 degrees out of phase to obtain a zero output from the phase detector. Some gain may be needed to compensate for the losses in Block 10.

Block 12. The phase detector portion of the NE565 only is used. The VCO part is unused but may be valuable in certain types of special displays.
An alternate form of analog phase detector might be an AND gate followed by a standard duty cycle integrator, such as used on dwell meters.

Block 13. The digital signals from the flip-flops are decoded with AND gates to indicate the sector corresponding to the phase lag between the two 30Hz signals."

Speech Privacy Circuit (Speech Scrambler)

The second place entry was that of David M. Alexander of Austin, Texas. His application for the loop was a voice scrambler-unscrambler for private communications.

"This circuit utilizes the principles of frequency inversion and masking to render speech unintelligible to listeners not possessing a similar unit. A synchronization signal is generated as part of the scrambled signal which phase locks the decoding carrier oscillator to the coding oscillator and thus guarantees minimum distortion in the unscrambled speech. This synch signal also increases the security close to the inversion point where they are displaced only slightly from their original values.

"In operation, a single circuit serves as both scrambler and unscrambler at one end of a two-way communications link. It is switched from the receive mode to the transmit mode by a multipole relay controlled by the push-to-talk switch on the system microphone or handset.

"As can be seen by the diagram (Figure 9-81), the major components of the system

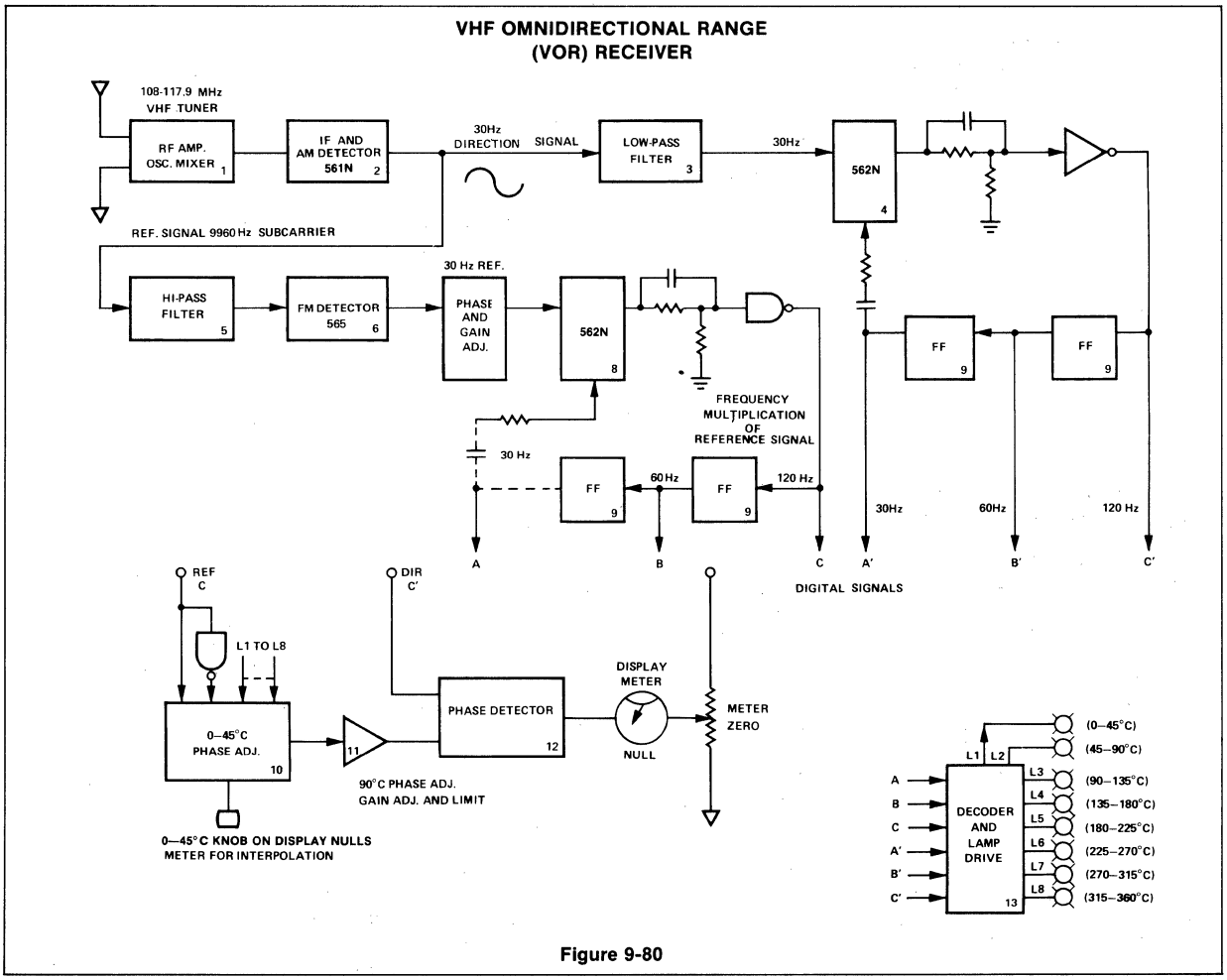


Figure 9-80

SIMPLIFIED DIAGRAM OF VOICE SCRAMBLER

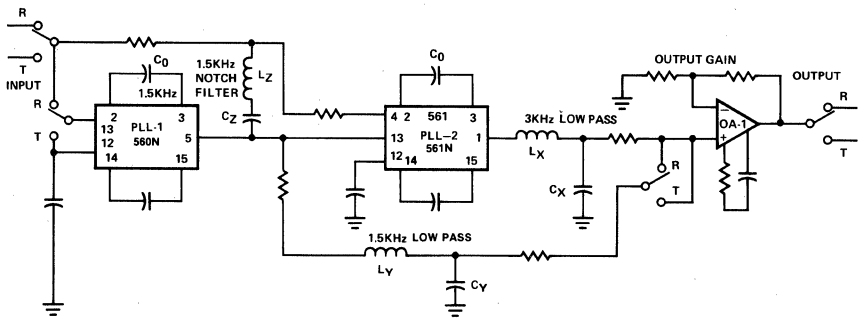


Figure 9-81

are the synch oscillator PLL-1 (NE560N), the carrier oscillator-modulator PLL-2 (NE561N) and the mixer-gain stage OA-1 (μA709).

"In the transmit mode, PLL-1 is adjusted to free-run at the inversion frequency (1.5kHz), or 1/2 the desired carrier frequency. PLL-2 is phase locked to this oscillator and operates on its second harmonic frequency (3kHz). The audio to be scrambled is applied to the input of the multiplier of PLL-2. This produces the sum and difference products of the input audio and the encoding carrier. The sum product is filtered out by the low pass filter (Lx-Cx), leaving only the difference product. This product consists of the original audio signal with the frequency components inverted about 1/2 the carrier frequency, or 1.5kHz. The square wave output of the oscillator of PLL-1 is low pass filtered by network Ly-Cy to produce a sine wave sync signal which is mixed with the inverted speech by OA-1 to produce the final scrambled signal.

"In the receive mode, PLL-1 is phase locked to the 1.5kHz synch and masking signal and acts as a signal conditioner for this signal. PLL-2 doubles this frequency to produce the decoding carrier. The scrambled signal is notch-filtered by network Lz-Cz to remove the 1.5kHz sync and masking signal and the resultant inverted audio applied to the multiplier of PLL-2. Here it is re-inverted in a manner similar to that of the transmit mode. The resultant unscrambled audio is amplified in OA-1 for output to further system audio stages."

[Note: It is suggested that the 1.5kHz "sync and masking" signal be changed to 1.0kHz, since PLL-2 (free-running at 3kHz) will lock to the third harmonic of the 1kHz square wave from the PLL-1 more readily than to the small second harmonic of the 1.5kHz signal. It may then be desirable to disconnect the notch filter during transmission. Of course, the filters may be implemented using active filter techniques.]

Precision Programmable Time Delay Generator

Sam Butt of Gaithersburg, Maryland, submitted the third place entry. This circuit provides both a pulse and a high frequency output at some time t_d after an input pulse is received. The interval t_d is programmable in 10 steps by means of a digital output switch.

Figure 9-82 shows the circuit in simplified form. It works as follows:

The 562 VCO is set so that its center frequency is at a point slightly above (say 10.5MHz) the window of the 10MHz band pass filter (BPF). Thus, no rf appears at the output. When a pulse is received at the input, the flip-flop is set so as to actuate one input A of the N8880A NAND gate.

The other side of the NAND gate B receives a signal which occurs at the rate of f_r/M where M is set by the binary-output switch. The output of the NAND gate begins to drive the N8291A binary ripple counter which is connected to the divide-by-N circuit in the loop feedback path. When 10 counts have been registered, the divide-by-N counter is putting out $f_o/10$ or (in the assumed case) 1.05 MHz. Since the phase comparator now sees two frequencies very close together, the loop locks up and $f_o = 10f_r$. Since f_r is 1MHz, the VCO operates at 10 MHz rf which the band pass filter passes to the output. This rf is detected and used to reset the input flip-flop and the counter in preparation for the next input pulse. The duration of the rf output is determined mainly by the detector time constant. The duration of the output pulse, which begins when the rf detector actuates the one-shot, is determined by the one-shot time constant.

(Equation 9-51)

$$\text{The delay time is } t_d = \frac{NM}{f_r}$$

where M is settable between 1 and 10 using the digital switch.

Metal Detector Using PLL as a Frequency Meter (565)

The metal detector shown in Figure 9-83 was submitted to the Signetics-EDN Phase Locked Loop Contest by Jim Blecksmith of Irvine, California. It incorporates a 565 as a frequency meter which indicates the frequency change in a Colpitts oscillator whose tank coil approaches a metal object. The loop output voltage at pin 7 is compared with the reference voltage at pin 6 and the difference amplified by meter amplifier Q4, Q5.

To increase the loop output (pin 7) to about 0.5V per percent of frequency deviation, a current source (Q2, Q3) is used to supply most of the capacitor (2.5mA) charge and discharge current at pin 8. The 20k resistor connected to pin 8 changes the charge and discharge current by 0.5V/20kΩ = 0.25mA or about 1% per 0.5V. Since the voltage at pins 8 and 7 track, the loop output voltage is also 0.5V per percent deviation. (This technique of increasing loop output swing for small frequency deviations is discussed in the Expanding Loop capability section of this chapter.)

Increasing oscillator frequency, as indicated by a rising meter indication, results when the search coil is brought near a nonferrous metal object. Reduced oscillator

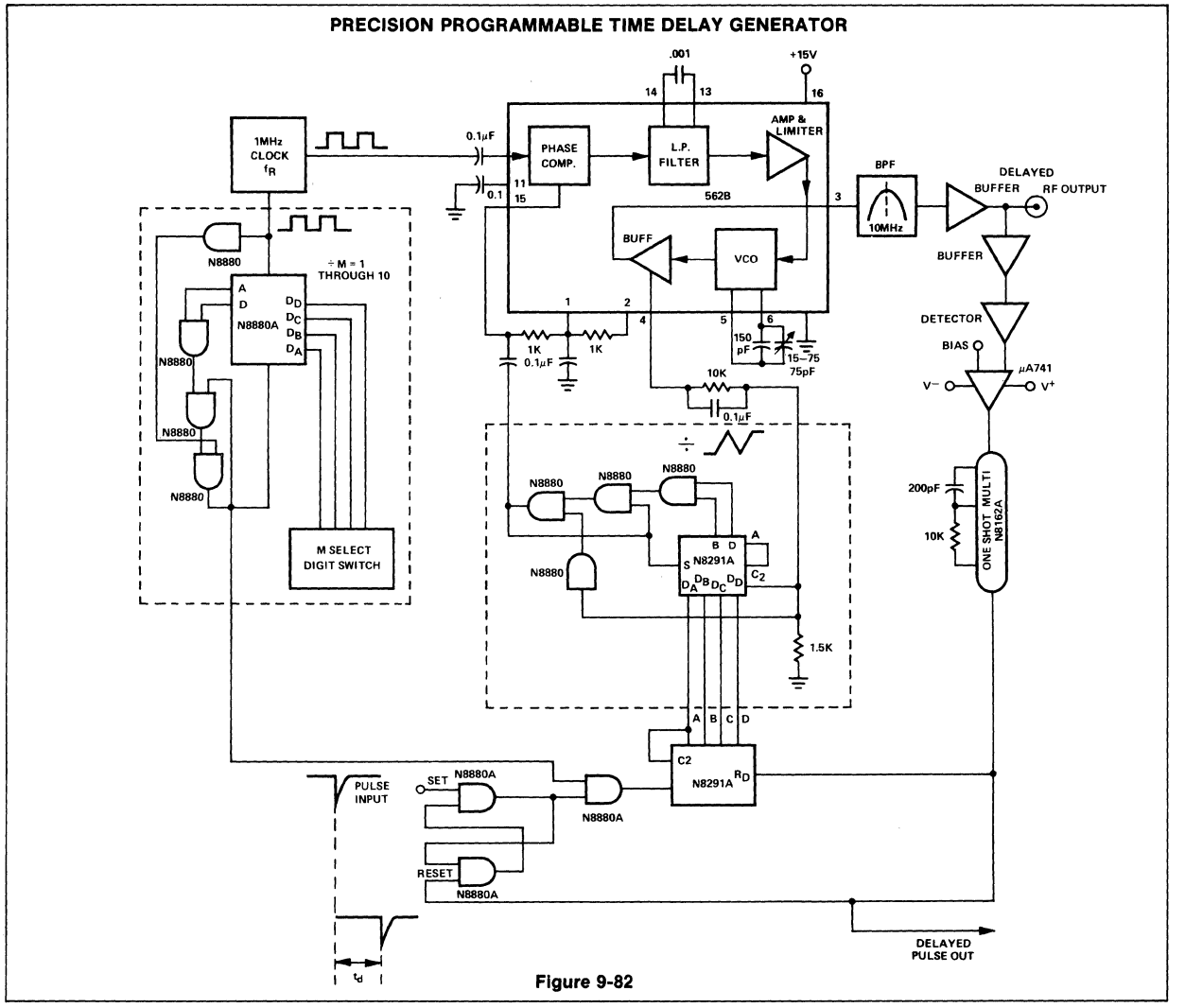


Figure 9-82

frequency, as indicated by a dropping meter reading, results from the search coil being brought near a ferrous object.

Programmed Phase or Frequency Shift

Howard E. Clupper of Chadds Ford, Pennsylvania, submitted the following circuit in which "a digital phase shifter is inserted in the loop between the VCO and the phase comparator. The phase shift is programmed by sequentially selecting the ring counter by means of the multiplexer and up-down counter.

"As shown in Figure 9-84, the eight ring counter outputs are separated by 45°, which is within the lock-in range of the loop. Output 1 is constrained to follow the phase shift introduced and may be used, for example, to drive a synchronous motor above or below its normal speed, while still maintaining reference with the input. This is accomplished by monitoring the contents of the up-down counter (which may be any length). As long as the counter does not overflow, the motor may be advanced or retarded in any manner and then returned to the original relationship with respect to the 60Hz reference input by running the U/D counter to the initial value.

"For higher frequency outputs, a divide-by-N counter may be added in the normal manner and the output taken directly from the VCO at output 2.

"Operation in this mode would provide means to generate a precisely controlled FM signal of any arbitrary center frequency depending upon the frequency of the reference input and the value of N."

The 565 may be used in this circuit in place of the 562 for lower frequency applications (less than 500kHz).

FSK Data Converter For Cassette Recorder

A circuit scheme which allows an ordinary reel or cassette tape recorder to be used as a digital data recorder was submitted by Daniel Chin of Burlington, Massachusetts.

"The circuit design allows any single-track audio tape recorder with frequency response to 7kHz to be used as a digital

PHASE LOCK LOOP METAL DETECTOR

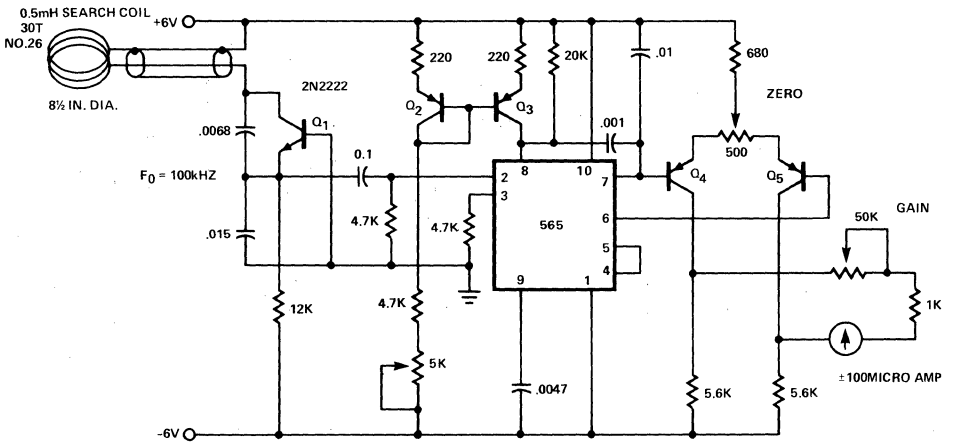


Figure 9-83

PROGRAMMED PHASE OR FREQUENCY SHIFTER

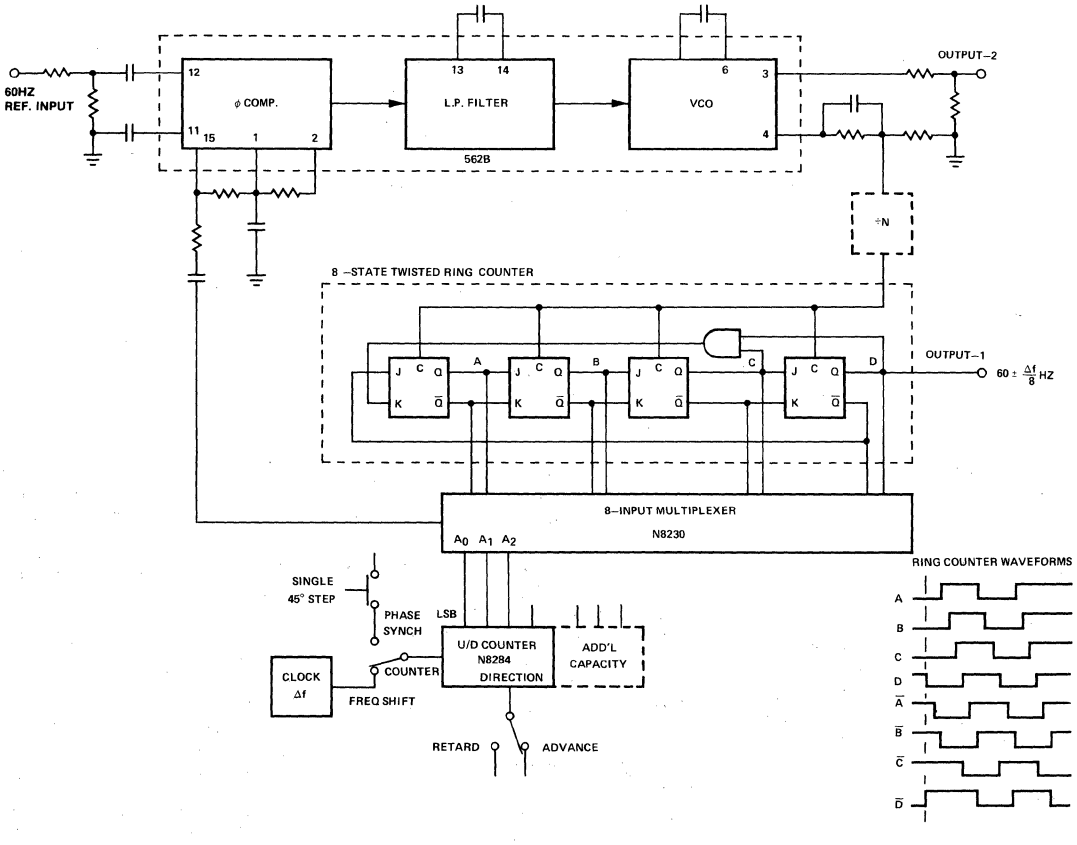


Figure 9-84

recorder for many non-critical applications. This application provides a complete data recording system using two recorded frequencies on a single track. The two frequencies are obtained from two synchronized NE565s. Detection of the recorded frequencies requires a third NE565. A fourth circuit is used to generate and synchronize the system clock. The advantages obtained by using these techniques are elimination of the need for:

1. A timing channel to strobe off the data, or
2. A third frequency for null, while using the other two frequencies for 1 and 0.

"This implementation, therefore, is one of the simplest ways to get a digital recording system on an audio recorder. It is shown in block diagram form in Figure 9-85.

"The parameters chosen for the circuit design allow a digital recording bit rate of 800Hz or 100 8-bit characters per second. Though 100 characters per second is less than the 300-character-per-second speed of a high-speed paper tape reader, the low cost of this circuitry combined with the audio tape recorder should make this system very attractive from a cost performance viewpoint. This is especially true when compared with the normal Teletype speed of 10 characters per second.

"The circuits will also work with the readily available low cost cassette recorders now available, which make compact as well as low cost information storage. A FSK system of recording is used, which allows the voice recording and reproduction electronics of the recorder to be unmodified for use in recording digital information. The retained electronics may also be used to record voice message identification of the various sections of the tape.

"The intended use of this circuit is to convert an audio recorder for minicomputer written for engineering design applications. Such an application requires good information storage and retrieval over a wide range of storage time. Redundancy may be incorporated by using a two-channel recorder (stereo) and a FSK detector per channel. The outputs of the two detectors could then be ORed digitally to recover recorded 1s and, thus, give a safeguard against dropouts.

Circuit Description

"Four NE565s are used in three circuits to achieve the design. These are:

BLOCK DIAGRAM OF PLL CASSETTE RECORDER

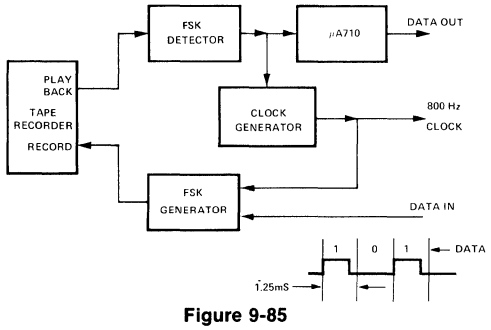


Figure 9-85

CASSETTE RECORDER FSK DETECTOR, CLOCK GENERATOR AND FSK GENERATOR

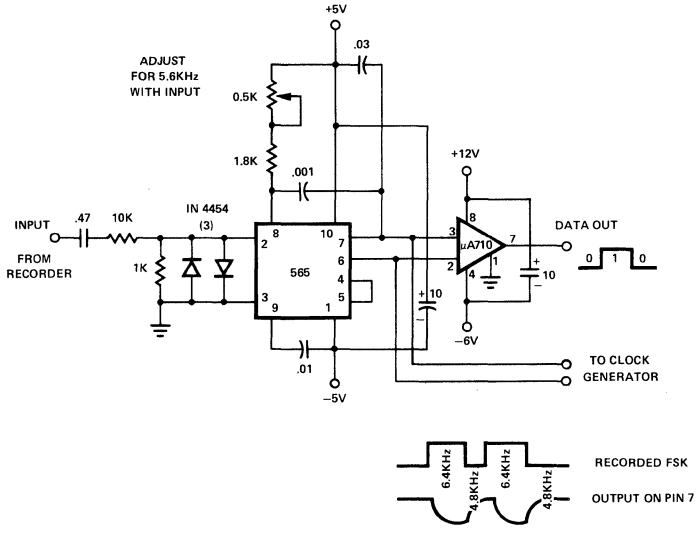


Figure 9-86a

"The FSK detector (Figure 9-86a) is used to detect 6.4kHz for a 1 and 4.8kHz for a 0. The data output is taken from a μA711 connected to pins 7 and 6 of the NE565. The recording method used is RZ FSK, which means that a zero is recorded as 4.8kHz for the entire bit period and one is recorded as 6.4kHz for about 60 percent of the period and 4.8kHz for the remaining 40 percent of the period. This 60 percent bit duty cycle insures that the clock will synchronize with a negative transition during the time that a 1 should be detected.

"The clock generator (Figure 9-86b) is used to derive the 800Hz with no input. When the data pulses are extracted from the recorded data, the clock is synchronized to the data. The design allows up to 7 zeros in succession without causing the clock to go out of synchronization. This condition is easily met if odd parity is used to record the 8-bit characters. (One of the 8 bits is a parity bit and, thus, one bit out of 8 is always a one.)

"The FSK generator (Figure 9-86c) provides the FSK signal for recording on tape. It consists of 2 oscillators locked to the basic 800Hz system clock but oscillating at 6.4kHz and 4.8kHz. The incoming data to be recorded selects either oscillator as the frequency to be recorded. Harmonic suppression of the square wave output is taken care of automatically by the high frequency roll off characteristic of the tape recorder."

CLOCK GENERATOR

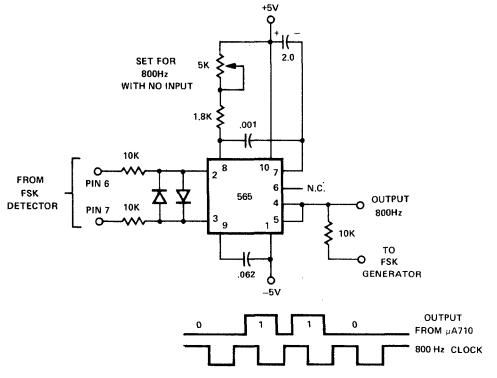


Figure 9-86b

FSK GENERATOR

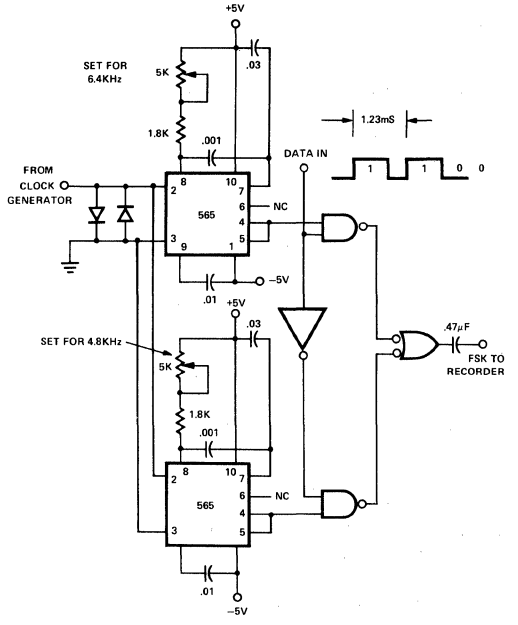


Figure 9-86c

Tape Recorder Flutter Meter

Using the 561 as a flutter meter for tape recorders was suggested by Ronald Blair of Houston, Texas. His circuit is given in Figure 9-87.

"The Signetics PLL 561N is used to detect the frequency variations of the playback 3kHz tone. The VCO frequency is set to a nominal 3kHz by C_O and fine tuning trimmer. The demodulated output is ac coupled to a high input impedance amplifier. An oscilloscope can be used to measure peak deviations and a true RMS voltmeter is used to make RMS flutter readings. Note: Waveform is complex and averaging or peak reading meters will not give true readings.

"The output may be calibrated by feeding in a 3kHz tone from an oscillator and offsetting the frequency by 1% and measuring the output level shift. Good recorders have RMS flutter of less than 0.1%. The output can be filtered to study selected frequency bands.

"Speed variations in the movement of tape across the heads in a 4 tape recorder cause the playback frequency to vary from the original signal being recorded. These speed variations are caused by mechanical problems associated with the tape drive and tape guidance mechanisms. The variation in frequency of the playback signal is called flutter and is generally measured over a frequency range of 0.5Hz + 0.200Hz.

"Test tapes with low recorded flutter variations are available to test playback mechanisms. These tapes are standardized at 3kHz. With the systems equipped with record heads, a 3kHz can be recorded for analysis."

[Note: A 565 may be used in place of the 561N since the frequency is quite low.]

FLUTTER METER USING 561N

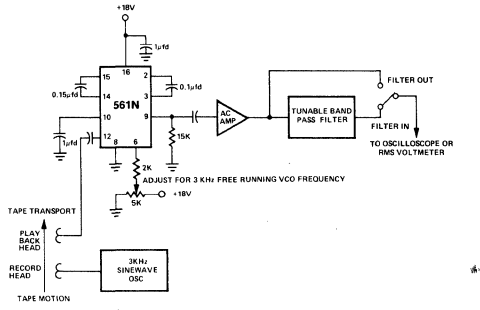


Figure 9-87

SECTION 27
APPENDICES

INCHES			DECIMAL EQUIVALENT	MILLIMETER EQUIVALENT
1/64			.0156	0.397
	1/32		.0313	0.794
3/64			.0469	1.191
		1/16	.0625	1.588
5/64			.0781	1.985
	3/32		.0938	2.381
7/64			.1094	2.778
		1/8	.1250	3.175
9/64			.1406	3.572
	5/32		.1563	3.969
11/64			.1719	4.366
		3/16	.1875	4.762
13/64			.2031	5.159
	7/32		.2188	5.556
15/64			.2344	5.953
		1/4	.2500	6.350
17/64			.2656	6.747
	9/32		.2813	7.144
19/64			.2969	7.541
		5/16	.3125	7.937
21/64			.3281	8.334
	11/32		.3438	8.731
23/64			.3594	9.128
		3/8	.3750	9.525
25/64			.3906	9.922
	13/32		.4063	10.319
27/64			.4219	10.716
		7/16	.4375	11.112
29/64			.4531	11.509
	15/32		.4688	11.906
31/64			.4844	12.303
		1/2	.5000	12.700
33/64			.5156	13.097
	17/32		.5313	13.494
35/64			.5469	13.891
		9/16	.5625	14.287
37/64			.5781	14.684
	19/32		.5938	15.081
39/64			.6094	15.478
		5/8	.6250	15.875
41/64			.6406	16.272
	21/32		.6563	16.669
43/64			.6719	17.067
		11/16	.6875	17.463
45/64			.7031	17.860
	23/32		.7188	18.238
47/64			.7344	18.635
		3/4	.7500	19.049
49/64			.7656	19.446
	25/32		.7813	19.842
51/64			.7969	20.239
		13/16	.8125	20.636
53/64			.8281	21.033
	27/32		.8438	21.430
55/64			.8594	21.827
		7/8	.8750	22.224
57/64			.8906	22.621
	29/32		.9063	23.018
59/64			.9219	23.415
		15/16	.9375	23.812
61/64			.9531	24.209
	31/32		.9688	24.606
63/64			.9844	25.004
		1.0	1.0000	25.400

MATHEMATICAL CONSTANTS

$\pi = 3.14$

$2\pi = 6.28$

$(2\pi)^2 = 39.5$

$4\pi = 12.6$

$\pi^2 = 9.87$

$\frac{\pi}{2} = 1.57$

$\frac{1}{\pi} = 0.318$

$\frac{1}{2\pi} = 0.159$

$\frac{1}{\pi^2} = 0.101$

$\frac{1}{\sqrt{\pi}} = 0.564$

$\sqrt{\pi} = 1.77$

$\sqrt{\frac{\pi}{2}} = 1.25$

$\sqrt{2} = 1.41$

$\sqrt{3} = 1.73$

$\frac{1}{\sqrt{2}} = 0.707$

$\frac{1}{\sqrt{3}} = 0.577$

$\log \pi = 0.497$

$\log \frac{\pi}{2} = 0.196$

$\log \pi^2 = 0.994$

$\log \sqrt{\pi} = 0.248$

TEMPERATURE CONVERSION TABLE

°C	°F	°C	°F	°C	°F	°C	°F
−100	−148	+ 60	+140	+220	+428	+380	+716
− 95	−139	+ 65	+149	+225	+437	+385	+725
− 90	−130	+ 70	+158	+230	+446	+390	+734
− 85	−121	+ 75	+167	+235	+455	+395	+743
− 80	−112	+ 80	+176	+240	+464	+400	+752
− 75	−103	+ 85	+185	+245	+473	+405	+761
− 70	− 94	+ 90	+194	+250	+482	+410	+770
− 65	− 85	+ 95	+203	+255	+491	+415	+779
− 60	− 76	+100	+212	+260	+500	+420	+788
− 55	− 67	+105	+221	+265	+509	+425	+797
− 50	− 58	+110	+230	+270	+518	+430	+806
− 45	− 49	+115	+239	+275	+527	+435	+815
− 40	− 40	+120	+248	+280	+536	+440	+824
− 35	− 31	+125	+257	+285	+545	+445	+833
− 30	− 22	+130	+266	+290	+554	+450	+842
− 25	− 13	+135	+275	+295	+563	+455	+851
− 20	− 4	+140	+284	+300	+572	+460	+860
− 15	+ 5	+145	+293	+305	+581	+465	+869
− 10	+ 14	+150	+302	+310	+590	+470	+878
− 5	+ 23	+155	+311	+315	+599	+475	+887
0	+ 32	+160	+320	+320	+608	+480	+896
+ 5	+ 41	+165	+329	+325	+617	+485	+905
+ 10	+ 50	+170	+338	+330	+626	+490	+914
+ 15	+ 59	+175	+347	+335	+635	+495	+923
+ 20	+ 68	+180	+356	+340	+644	+500	+932
+ 25	+ 77	+185	+365	+345	+653	+505	+941
+ 30	+ 86	+190	+374	+350	+662	+510	+950
+ 35	+ 95	+195	+383	+355	+671	+515	+959
+ 40	+104	+200	+392	+360	+680	+520	+968
+ 45	+113	+205	+401	+365	+689	+525	+977
+ 50	+122	+210	+410	+370	+698	+530	+986
+ 55	+131	+215	+419	+375	+707	+535	+995

REACTANCE CHART

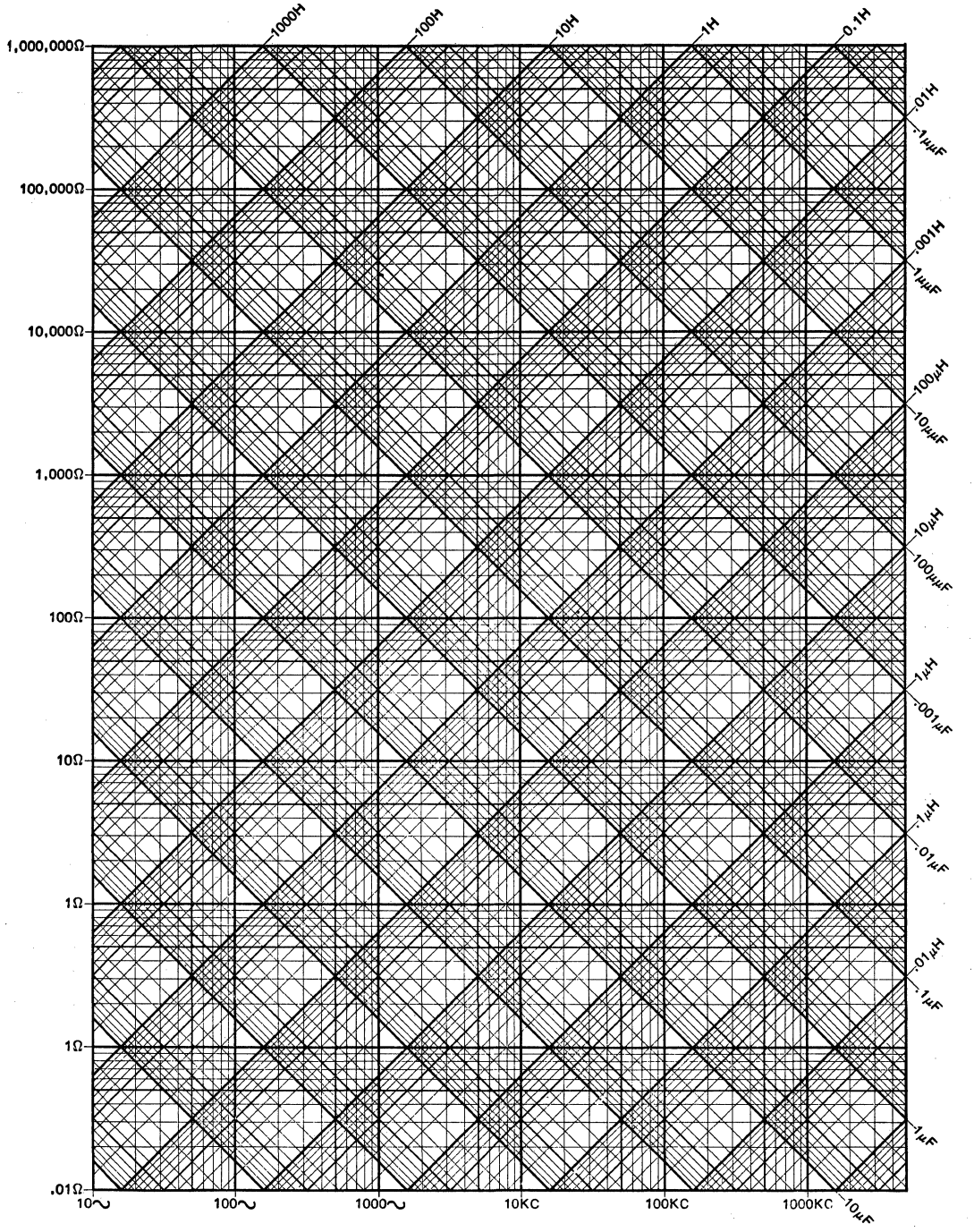
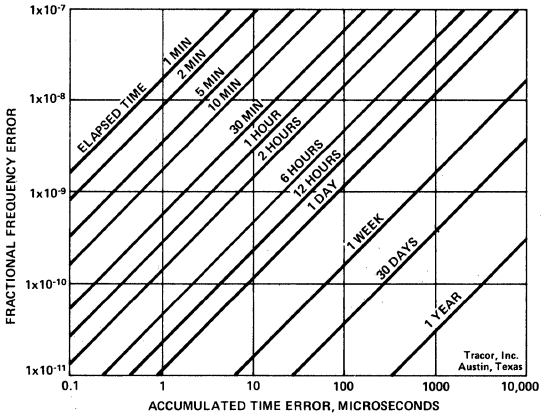


TABLE OF DECIBELS

DECIBEL (Voltage)	LOSS	GAIN	DECIBEL (Power)
.0	1.0000	1.000	.0
.1	.9886	1.012	.05
.2	.9772	1.023	.10
.3	.9661	1.035	.15
.4	.9550	1.047	.20
.5	.9441	1.059	.25
.6	.9333	1.072	.30
.7	.9226	1.084	.35
.8	.9120	1.096	.40
.9	.9016	1.109	.45
1.0	**.8913**	**1.122**	**.50**
.1	.8810	1.135	.55
.2	.8710	1.148	.60
.3	.8610	1.161	.65
.4	.8511	1.175	.70
.5	.8414	1.189	.75
.6	.8318	1.202	.80
.7	.8222	1.216	.85
.8	.8128	1.230	.90
.9	.8035	1.245	.95
2.0	**.7943**	**1.259**	**1.00**
.1	.7852	1.274	.05
.2	.7762	1.288	.10
.3	.7674	1.303	.15
.4	.7586	1.318	.20
.5	.7499	1.334	.25
.6	.7413	1.349	.30
.7	.7328	1.365	.35
.8	.7244	1.380	.40
.9	.7161	1.396	.45
3.0	**.7079**	**1.413**	**.50**
.1	.6998	1.429	.55
.2	.6918	1.445	.60
.3	.6839	1.462	.65
.4	.6761	1.479	.70
.5	.6683	1.496	.75
.6	.6607	1.514	.80
.7	.6531	1.531	.85
.8	.6457	1.549	.90
.9	.6383	1.567	.95
4.0	**.6310**	**1.585**	**2.00**
.1	.6237	1.603	.05
.2	.6166	1.622	.10
.3	.6095	1.641	.15
.4	.6026	1.660	.20
.5	.5957	1.679	.25
.6	.5888	1.698	.30
.7	.5821	1.718	.35
.8	.5754	1.738	.40
.9	.5689	1.758	.45
5.0	**.5623**	**1.778**	**.50**
.1	.5559	1.799	.55
.2	.5495	1.820	.60
.3	.5433	1.841	.65
.4	.5370	1.862	.70
.5	.5309	1.884	.75
.6	.5248	1.905	.80
.7	.5188	1.928	.85
.8	.5129	1.950	.90
.9	.5070	1.972	.95
6.0	**.5012**	**1.995**	**3.00**
.1	.4955	2.018	.05
.2	.4898	2.042	.10
.3	.4842	2.065	.15
.4	.4786	2.089	.20
.5	.4732	2.113	.25
.6	.4677	2.138	.30
.7	.4624	2.163	.35
.8	.4571	2.188	.40
.9	.4519	2.213	.45
7.0	**.4467**	**2.239**	**.50**
.1	.4416	2.265	.55
.2	.4365	2.291	.60
.3	.4315	2.317	.65
.4	.4266	2.344	.70
.5	.4217	2.371	.75
.6	.4169	2.399	.80
.7	.4121	2.427	.85
.8	.4074	2.455	.90
.9	.4027	2.483	.95
8.0	**.3981**	**2.512**	**4.00**
.1	.3936	2.541	.05
.2	.3890	2.570	.10
.3	.3846	2.600	.15
.4	.3802	2.630	.20
.5	.3758	2.661	.25
.6	.3715	2.692	.30
.7	.3673	2.723	.35
.8	.3631	2.754	.40
.9	.3589	2.786	.45
9.0	**.3548**	**2.818**	**.50**
.1	.3508	2.851	.55
.2	.3467	2.884	.60
.3	.3428	2.917	.65
.4	.3388	2.951	.70
.5	.3350	2.985	.75
.6	.3311	3.020	.80
.7	.3273	3.055	.85
.8	.3236	3.090	.90
.9	.3199	3.126	.95
10.0	**.3162**	**3.162**	**5.00**
.1	.3126	3.199	.05
.2	.3090	3.236	.10
.3	.3055	3.273	.15
.4	.3020	3.311	.20
.5	.2985	3.350	.25
.6	.2951	3.388	.30
.7	.2917	3.428	.35
.8	.2884	3.467	.40
.9	.2851	3.508	.45
11.0	**.2818**	**3.548**	**.50**
.1	.2786	3.589	.55
.2	.2754	3.631	.60
.3	.2723	3.673	.65
.4	.2692	3.715	.70
.5	.2661	3.758	.75
.6	.2630	3.802	.80
.7	.2600	3.846	.85
.8	.2570	3.890	.90
.9	.2541	3.936	.95
12.0	**.2512**	**3.981**	**6.00**
.1	.2483	4.027	.05
.2	.2455	4.074	.10
.3	.2427	4.121	.15
.4	.2399	4.169	.20
.5	.2371	4.217	.25
.6	.2344	4.266	.30
.7	.2317	4.315	.35
.8	.2291	4.365	.40
.9	.2265	4.416	.45
13.0	**.2239**	**4.467**	**.50**
.1	.2213	4.519	.55
.2	.2188	4.571	.60
.3	.2163	4.624	.65
.4	.2138	4.677	.70
.5	.2113	4.732	.75
.6	.2089	4.786	.80
.7	.2065	4.842	.85
.8	.2042	4.898	.90
.9	.2018	4.955	.95
14.0	**.1995**	**5.012**	**7.00**
.1	.1972	5.070	.05
.2	.1950	5.129	.10
.3	.1928	5.188	.15
.4	.1905	5.248	.20
.5	.1884	5.309	.25
.6	.1862	5.370	.30
.7	.1841	5.433	.35
.8	.1820	5.495	.40
.9	.1799	5.559	.45
15.0	**.1778**	**5.623**	**.50**
.1	.1758	5.689	.55
.2	.1738	5.754	.60
.3	.1718	5.821	.65
.4	.1698	5.888	.70
.5	.1679	5.957	.75
.6	.1660	6.026	.80
.7	.1641	6.095	.85
.8	.1622	6.166	.90
.9	.1603	6.237	.95
16.0	**.1585**	**6.310**	**8.00**
.1	.1567	6.383	.05
.2	.1549	6.457	.10
.3	.1531	6.531	.15
.4	.1514	6.607	.20
.5	.1496	6.683	.25
.6	.1479	6.761	.30
.7	.1462	6.839	.35
.8	.1445	6.918	.40
.9	.1429	6.998	.45
17.0	**.1413**	**7.079**	**.50**
.1	.1396	7.161	.55
.2	.1380	7.244	.60
.3	.1365	7.328	.65
.4	.1349	7.413	.70
.5	.1334	7.499	.75
.6	.1318	7.586	.80
.7	.1303	7.674	.85
.8	.1288	7.762	.90
.9	.1274	7.852	.95
18.0	**.1259**	**7.943**	**9.00**
.1	.1245	8.035	.05
.2	.1230	8.128	.10
.3	.1216	8.222	.15
.4	.1202	8.318	.20
.5	.1189	8.414	.25
.6	.1175	8.511	.30
.7	.1161	8.610	.35
.8	.1148	8.710	.40
.9	.1135	8.811	.45
19.0	**.1122**	**8.913**	**.50**
.1	.1109	9.016	.55
.2	.1096	9.120	.60
.3	.1084	9.226	.65
.4	.1072	9.333	.70
.5	.1059	9.441	.75
.6	.1047	9.550	.80
.7	.1035	9.661	.85
.8	.1023	9.772	.90
.9	.1012	9.886	.95

DECIBEL (Voltage)	LOSS	GAIN	DECIBEL (Power)
20.0	**.1000**	**10.00**	**10.00**
	Use the same numbers as 0-20 dB, but shift point one step to the left. Thus since 10dB = .3162 30dB = .03162	Use the same numbers as 0-20 dB, but shift point one step to the right. Thus since 10dB = 3.162 30dB = 31.62	This column repeats every 10dB instead of every 20dB
40.0	**.01**	**100**	**20.00**
	Use the same numbers as 0-20 dB, but shift point two steps to the left. Thus since 10dB = .3162 50dB = .003162	Use the same numbers as 0-20 dB, but shift point two steps to the right. Thus since 10dB = 3.162 50db = 316.2	This column repeats every 10dB instead of every 20dB
60.0	**.001**	**1,000**	**30.00**
	Use the same numbers as 0-20dB, but shift point three steps to the left. Thus since 10dB = .3162 70dB = .0003162	Use the same numbers as 0-20 dB, but shift point three steps to the right. Thus since 10dB = 3.162 70dB = 3162.	This column repeats every 10dB instead of every 20dB
80.0	**.0001**	**10,000**	**40.00**
	Use the same numbers as 0-20 dB, but shift point four steps to the left. Thus since 10dB = .3162 90dB = .00003162	Use the same numbers as 0-20dB, but shift point four steps to the right. Thus since 10dB = 3.162 90dB = 31620.	This column repeats every 10dB instead of every 20dB.
100.0	**.00001**	**100,000**	**50.00**

FREQUENCY CONVERSION FACTORS



Frequency Conversion Factors

1 min=60 sec=6×10^7 μsec
1 hr.=3600 sec=3.6×10^9 μsec
1 day=8.64×10^4 sec=8.64×10^{10} μsec
1 microsecond/min=1.667×10^{-8}
1 microsecond/hr.=2.78×10^{-10}
1 microsecond/day=1.16×10^{-11}

Fractional frequency error, $\frac{\Delta f}{f}$ =

$$\frac{\text{difference in microseconds}}{\text{elapsed time in seconds}} \times 10^{-6}$$

MILITARY

The Signetics Mil 38510/883 Program is organized to provide a broad selection of processing options, structured around the most commonly requested customer flows. The program is designed to provide our customers:

- Standard processing flows to help minimize the need for custom specs.
- Cost savings realized by using standard processing flows in lieu of custom flows.
- Better delivery lead times by minimizing spec negotiation time, plus allows customers to buy product off-the-shelf or in various stages of production rather than waiting for devices started specifically to custom specs.

The following explains the different processing options available to you. Special device marking clearly distinguishes the type of screening performed. Refer to Tables 1 and 2.

	JB	JBX	RBX	RB	S
	JAN Qualified	JAN Processed	JAN Rel	/883	Mil Temp
54/54H	X	X	X	X	X
54LS	X	X	X	X	X
54S	X	X	X	X	X
82/8T	X	X	X	X	X
93XX	X	X	X	X	X
96XX	—	—	X	X	X
Linear	Planned	X	X	X	X
Bipolar Memory	Planned	—	X	X	X
Microprocessor	—	—	X	X	X

Table 1 MILITARY SUMMARY

JAN CASE OUTLINE AND LEAD FINISH	SIGNETICS MILITARY PACKAGE TYPES				
			Dual-In-Line		
	8-Pin	10-Pin	14-Pin	16-Pin	24-Pin
CB	—	—	F	—	—
EB	—	—	—	F	—
JB	—	—	—	—	I/F*
DB	—	—	W	—	—
FB	—	—	—	W	—
ZC	—	—	—	—	Q
GC	T	—	—	—	—
IC	—	K	—	—	—

*The gold plated versions of these packages will be available for a limited time.
All products listed in the Military section are also available in Die form.

Table 2 MILITARY PACKAGE AVAILABILITY

JAN QUALIFIED (JB)

JAN Qualified product is designed to give you the optimum in quality and reliability. The JAN processing level is offered as the result of the government's product standardization programs, and is monitored by the Defense Electronic Supply Center (DESC), through the use of industry-wide procedures and specifications.

JAN Qualified products are manufactured, processed and tested in a government certified facility to Mil-M 38510, and appropriate device slash sheet specifications. Design documentation, lot sampling plans, electrical test data and qualification data for each specific part type has been approved by the Defense Electronic Supply Center (DESC) and products appear on the DESC Qualified Products List (QPL-38510).

Group B testing, per Mil-Std-883 Method 5005, is performed on each six weeks of production on each slash sheet for each package type. Group C, per Mil-Std-883 Method 5005, is performed every ninety days for each microcircuit group. Group D testing, per Mil-Std-883 Method 5005, is performed every six months for each package type.

In addition to the common specs used throughout the industry for processing and testing, JAN Qualified products also possess a requirement for a standard marking used throughout the IC industry.

JAN PROCESSING (JBX)

This option is extremely useful when the reliability and screening of a JAN device is required, however, Signetics is not listed on the QPL for the product needed. Processing is performed to Mil-Std-883 Method 5004, and product is 100% electrically tested to the appropriate JAN slash sheet.

Group B, C and D data for JAN processed and the other military processing levels which follow, consist of Group B, C and D testing performed per Mil-Std-883 Method 5005, in accordance with the Signetics Military Data Program.

JAN REL (RBX)

Processing to this option is ideal when no JAN slash sheets are released on devices required. Product is processed to Mil-Std-883 Method 5004, and is 100% electrically tested to industry data sheets.

/883B (RB)

This is a lower priced version of the JAN Rel option described above. Processing is identical with the only exceptions being the dc electrical testing over the temperature range and ac electrical testing at room temperature are performed as a part of Group A instead of 100%.

MIL TEMP/883C (S/RC)

If you need a Military temp. range device, but do not require all the high reliability screening performed in the other processing options, our Mil-Temp. product is ideal. Mil-Temp. parts are the standard full Mil-Temperature range product guaranteed to a 1% AQL to the Signetics data sheet parameters.

MILITARY GENERIC DATA

Signetics has a new program for those customers who require quality conformance data on their products. This program allows our customers to obtain reliability information without the necessity of running Groups B, C and D inspections for their particular purchase order. It provides for the customer something that has not been readily available before in the semiconductor industry in that all Military Generic Data is controlled and audited by both Government Inspection in the case of JAN data and Signetics Quality Assurance.

Signetics Military Generic Data is compiled by the Military Products Division based on data from 1) JAN quality conformance lots, and 2) Data generated by quality conformance lots run for other reliability programs. Refer to Table 3.

A Military Generic family is defined as consisting of die function and package type families.

Military Generic Data

- Allows our customers to qualify Signetics products based on existing quality conformance data performed at Signetics.
- Allows our customers to reduce costs and improve deliveries.
- Provides assurance that all Signetics die function families and packages meet Mil-M-38510 and customer reliability requirements.
- Provides an attributes summary to the customer backed by lot identity and traceability.

QUALIFIED SUB-GROUPS	QUALIFIES	OPTION 1	OPTION 2
A	Electrical Test	See NOTE 1	See NOTE 1
B	Package—Same package construction and lead finish.	Data selected from devices manufactured within 6 weeks of the manufacturing period on the same production line through final seal.	Data selected from devices manufactured within 24 weeks of manufacturing period.
C	Die/Process—Devices representing the same process families.	Data selected from representative devices from the same microcircuit group and sealed within 12 weeks of the manufacturing period.	Data selected from the representative devices from the same microcircuit group and sealed within 48 weeks of the manufacturing period.
D	Package—Same package construction and lead finish.	Data selected from the devices representing the same package construction and lead finish manufactured within the 24 weeks of manufacturing period. If specific data not available, Option 2 will be supplied.	Data selected from the devices representing the same package construction and lead finish manufactured within the 52 weeks of manufacturing period.

NOTE
1. Group A is performed on each lot or sublot of Signetics devices.

Table 3 DEFINITION AND QUALIFYING MANUFACTURING PERIODS FOR GENERIC DATA

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS					
			CLASS A	JAN Qualified (JB)	JAN Processed (JBX)	JAN Rel (RBX)	/883B (RB)	/883C (RC)
General Mil-M-38510 1. Pre-Certification A. Product Assurance Program Plan B. Manufacturer's Certification	The manufacturer shall establish and implement a Products Assurance Program Plan and provide for a manufacturer survey by the qualifying activity, Para. 3.4.1.1	—	X	X	N/A	N/A	N/A	N/A
2. Certification	Received after manufacturer has completed a successful survey, Para. 3.4.1.2	—	X	X	N/A	N/A	N/A	N/A
3. Device Qualification	Device qualification shall consist of subjecting the desired device to groups A, B, C & D of method 5005 to tightened LTPD, Para. 3.4.1.2	—	X	X	N/A	N/A	N/A	N/A
4. Traceability	Traceability maintained back to a production lot Para. 3.4.6	—	X	X	X	X	X	X
5. Country of Origin	Devices must be manufactured, assembled, and tested within the U.S. or its territories, Para. 3.2.1	—	X	X	N/A	N/A	N/A	N/A
Screening Per Method 5004 of Mil-Std-883								
6. Internal Visual (Precap)	2010, Cond. A or B	100%	XA	XB	XB	XB	XB	XB
7. Stabilization Bake	1008, Cond. C Min; (24 Hrs @ 150°C)	100%	X	X	X	X	X	X
8. Temperature Cycling* *For Class B and C devices thermal shock may be substituted, 1011, Cond. A; (15 cycles, 0° to +100°C)	1010, Cond. C; (10 cycles, -65°C to +150°C)	100%	X	X	X	X	X	X
9. Constant Acceleration	2001, Cond. E; (30_{kg} in YI Plane)	100%	X	X	X	X	X	X
10. Visual Inspection	There is no test method for this screen; it is intended only for the removal of "Catastrophic Failures" defined as "Missing Leads, Broken Packages or Lids Off."	100%	X	X	X	X	X	X
11. Seal (Hermeticity)	1014							
A. Fine	Cond. A or B (5.0 X 10^{-8}CC/Sec)	100%	X	X	X	X	X	X
B. Gross	Cond. C2 Min.	100%	X	X	X	X	X	X
12. Interim Electricals (Pre Burn-In)	Per applicable device specification	100% Optional	100% Read & Record	Slash Sheet	Slash Sheet	Data Sheet	Data Sheet	N/A
13. Burn-In	1015, Cond. as specified (160 hrs. Min. at 125°C)	100%	100% 240 hrs.	X	X	X	X	N/A
14. Final Electricals	Per applicable Device Specification	100%	100% Read & Record	Slash Sheet	Slash Sheet	Data Sheet	Data Sheet	Data Sheet
A. Static Tests @ 25°C	Sub Group 1		X	X	X	X	X	X
B. Static Tests @ +125°C	Sub Group 2		X	X	X	X	N/A	N/A
C. Static Tests @ -55°C	Sub Group 3		X	X	X	X	N/A	N/A

Table 4 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD CLASS B PRODUCTS

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS					
			CLASS A	JAN Qualified (JB)	JAN Processed (JBX)	JAN Rel (RBX)	/883B (RB)	/883C (RC)
D. Dynamic Test @ 25°C	Sub Group 4 for (Linear Product Mainly)		X	X	X	X	X	X
E. Functional Test @ 25°C	Sub Group 7		X	X	X	X	X	X
F. Switching Test @ 25°C	Sub Group 9		X	X	X	X	N/A	N/A
15. Percent Defective allowable (PDA)	A PDA of 10% is a normal requirement applied against the static tests @ 25°C (A-1). This is controlled by the slash sheets for JB & JBX products. For RBX & RB 10% is standard.	10%	5%	X	X	X	X	N/A
16. Marking	Fungus Inhibiting Paint	100%	As Req'd	JM38510/ XXXX Slash Sheet #	M38510/ XXXX Slash Sheet #	M38510/ SXXXX Sig. Basic #	SXXXX/ 883B Sig. Basic #	SXXXX/ 883C Sig. Basic #
17. X-Ray	2012		100%	N/A	N/A	N/A	N/A	N/A
18. External Visual	2009	100%	X	X	X	X	X	X
Quality Conformance Inspection per Method 5005 of Mil-Std-883								
19. Group A	Electrical Tests-Final Electricals (#14 above) repeated on a sample basis. (Sub Groups 1 thru 12 as specified.)	Each Lot	X	X	X	X	X	X
20. Group B	Package functional and constructional related test I.E. package dimensions, resistance to solvents, internal visual & mechanical, bond strength & solderability.	Every 6 week per microcircuit group	X	X	Generic Data Available			
21. Group C	Die related tests I.E. 1,000 hr. operating life, temperature cycling, & constant acceleration.	Every 3 months per package type	X	X	Generic Data Available			
22. Group D	Package related tests I.E. physical dimensions, lead fatigue, thermal shock, temperature cycle, moisture resistance, mechanical shock, vibration variable frequency constant acceleration, & salt atmosphere.	Every 6 months per package type	X	X	Generic Data Available			

Table 4 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD CLASS B PRODUCTS (Cont'd)

LOGIC—5400 SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL*		JAN PROC-ESSED		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK	DIP	FLATPACK
5400	Quad 2-Input NAND Gate	/00104	1	1	F	W	F	W
5401	Quad 2-Input NAND Gate with o/c	/00107	1	1	F	W	F	W
5402	Quad 2-Input NOR Gate	/00401	1	1	F	W	F	W
5403	Quad 2-Input NAND Gate with o/c	/00109	1	1	F	*	F	—
5404	Hex Inverter	/00105	1	1	F	W	F	W
5405	Hex Inverter with o/c	/00108	1	1	F	W	F	W
5406	Hex Inverter w/Buffer/Driver with o/c	/00801	—	—	F	W	F	W
5407	Hex Buffer/Driver with o/c	/00803	—	—	F	W	F	W
5408	Quad 2-Input AND Gate	/01601	1	1	F	W	F	W
5409	Quad 2-Input AND Gate with o/c	/01602	1	1	F	W	F	W
5410	Triple 3-Input NAND Gate	/00103	1	1	F	W	F	W
5411	Triple 3-Input NAND Gate	—	—	—	—	—	F	W
5412	Triple 3-Input NAND Gate wih o/c	/00106	—	—	—	—	F	W
5413	Dual NAND Schmitt Trigger	/15101	*	*	F	W	F	W
5414	Hex Schmitt Trigger	/15102	*	*	F	W	F	W
5416	Hex Inverter Buffer/Driver with o/c	/00802	—	—	F	W	F	W
5417	Hex Buffer/Driver with o/c	/00804	—	—	F	W	F	W
5420	Dual 4-Input NAND Gate	/00102	1	1	F	W	F	W
5421	Dual 4-Input AND Gate	—	—	—	—	—	F	W
5426	Quad 2-Input NAND Gate with o/c	/00805	1	—	F	—	F	—
5427	Triple 3-Input NOR Gate	/00404	*	*	F	W	F	W
5428	Quad 2-Input NOR Buffer	/16201	—	—	—	—	F	W
5430	8-Input NAND Gate	/00101	1	1	F	W	F	W
5432	Quad 2-Input OR Gate	/16101	*	*	—	—	F	W
5433	Quad 2-Input NOR Buffer with o/c	—	—	—	—	—	F	W
5437	Quad 2-Input NAND Buffer	/00302	1	1	F	W	F	W
5438	Quad 2-Input NAND Buffer with o/c	/00303	1	1	F	W	F	W
5439	Quad 2-Input NAND Buffer	—	—	—	—	—	F	W
5440	Dual 4-Input NAND Buffer	/00301	1	1	F	W	F	W
5442	BCD-to-Decimal Decoder	/01001	1	1	F	W	F	W
5443	Excess 3-to-Decimal Decoder	/01002	1	1	F	W	F	W
5444	Excess 3-Gray-to-Decimal Decoder	/01003	1	1	F	W	F	W
5445	BCD-to-Decimal Decoder/Driver with o/c	/01004	—	—	F	W	F	W
5446A	BCD-to-7 Segment Decoder/ Driver	/01006	—	—	F	W	F	W
5447A	BCD-to-7 Segment Decoder/ Driver	/01007	—	—	F	W	F	W
5448	BCD-to-7 Segment Decoder/ Driver	/01008	—	—	F	W	F	W
5450	Expandable Dual 2-Wide 2-Input A01	/00501	1	1	F	W	F	W
5451	Dual 2-Wide 2-Input A01 Gate	/00502	1	1	F	W	F	W
5453	4-Wide 2-Input A01 Gate (Expandable)	/00503	1	1	F	W	F	W
5454	4-Wide 2-Input A01 Gate	/00504	1	1	F	W	F	W
5455	2-Wide 4-Input A01 Gate	/04005	—	—	—	—	—	—

NOTE

Per QPL 38510-28 dated 1 Apr. 1977
1 = Level 1 Qualification
2 = Level 2 Qualification
* = In process

LOGIC—5400 SERIES (Cont'd)

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL*		JAN PROC-ESSED		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK	DIP	FLATPACK
5460	Dual 4-Input Expander	—	—	—	—	—	F	W
5470	J-K Flip-Flop	/00206	1	1	F	W	F	W
5472	J-K Master-Slave Flip-Flop	/00201	1	1	F	W	F	W
5473	Dual J-K Master-Slave Flip-Flop	/00202	1	1	F	W	F	W
5474	Dual D-Type Edge-Triggered Flip-Flop	/00205	1	1	F	W	F	W
5475	Quad Bistable Latch	/01501	1	1	F	W	F	W
5476	Dual J-K Master-Slave Flip-Flop	/00204	1	1	F	W	F	W
5477	Quad Bistable Latch	/01502	—	1	—	W	—	W
5480	Gated Full Adder	—	—	—	—	—	F	W
5483	4-Bit Binary Full Adder	/00602	1	1	F	W	F	W
5485	4-Bit Magnitude Comparator	/15001	1	1	F	W	F	W
5486	Quad 2-Input Exclusive-OR Gate	/00701	1	1	F	W	F	W
5490	Decade Counter	/01307	*	*	F	W	F	W
5491	8-Bit Shift Register	—	—	—	—	—	F	W
5492	Divide-by-Twelve Counter	/01301	1	1	F	W	F	W
5493	4-Bit Binary Counter	/01302	1	1	F	W	F	W
5494	4-Bit Shift Register (PISO)	—	—	—	—	—	F	W
5495	4-Bit Left-Right Shift Register	/00901	1	—	F	—	F	W
5496	5-Bit Shift Register	/00902	1	1	F	W	F	W
54100	4-Bit Bistable Latch (Dual)	—	—	—	—	—	F	W
54107	Dual J-K Master-Slave Flip-Flop	/00203	1	—	F	—	F	—
54109	Dual J-K Positive Edge-Triggered Flip-Flop	—	—	—	—	—	F	W
54116	Dual 4-Bit Latch with Clear	/01503	2	—	I	—	I	—
54121	Monostable Multivibrator	/01201	1	1	F	W	F	W
54122	Retriggerable Monostable Multivibrator	/01202	—	—	—	—	—	—
54123	Retriggerable Monostable Multivibrator	/01203	1	1	F	W	F	W
54125	Quad Bus Buffer Gate w/Tri-State Outputs	/15301	2	2	F	W	F	W
54126	Quad Bus Buffer Gate w/Tri-State Outputs	/15302	2	2	F	W	F	W
54128	Quad 2-Input NOR Buffer	—	—	—	—	—	F	W
54132	Quad Schmitt Trigger	/15103	*	*	F	W	F	W
54145	BCD-to-Decimal Decoder/Driver with o/c	/01005	—	—	F	W	F	W
54147	10-Line to 4-Line Priority Encoder	/15601	*	*	F	W	F	W
54148	8-Line to 3-Line Priority Encoder	/15602	*	*	F	W	F	W
54150	16-Line to 1-Line Mux	/01401	2	—	I	—	I	—
54151	8-Line to 1-Line Mux	/01406	2	2	F	W	F	W
54152	8-Line to 1-Line Mux	—	—	—	—	—	F	W
54153	Dual 4-Line to 1-Line Mux	/01403	2	2	F	W	F	W
54154	4-Line to 16-Line Decoder/ Demux	/15201	*	—	I	—	I	Q
54155	Dual 2-Line to 4-Line Decoder/Demux	/15202	2	2	F	W	F	W
54156	Dual 2-Line to 4-Line Decoder/Demux	/15203	2	2	F	W	F	W
54157	Quad 2-Input Data Selector (non-inv.)	/01405	1	1	F	W	F	W
54158	Quad 2-Input Data Selector (inv.)	—	—	—	—	—	F	W
54160	Synchronous 4-Bit Decade Counter	/01303	1	1	F	W	F	W

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LOGIC—5400 SERIES (Cont'd)

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		JAN PROC-ESSED		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK	DIP	FLATPACK
54161	Synchronous 4-Bit Binary Counter	/01306	1	1	F	W	F	W
54162	Synchronous 4-Bit Decade Counter	/01305	1	1	F	W	F	W
54163	Synchronous 4-Bit Binary Counter	/01304	1	1	F	W	F	W
54164	8-Bit Parallel-Out Serial Shift Register	/00903	1	—	F	—	F	—
54165	Parallel-Load 8-Bit Shift Register	/00904	*	*	F	W	F	W
			—	—	—	—	F	W
54166	8-Bit Shift Register	—	—	—	—	—	F	—
54170	4X4 Register File	/01801						
54174	Hex D-Type Flip-Flop with Clear	/01701	1	1	F	W	F	W
54175	Quad D-Type Edge-Triggered Flip-Flop	/01702	1	1	F	W	F	W
54180	8-Bit Odd/Even Parity Checker	/01901	—	2	F	W	F	W
54181	4-Bit Arithmetic Logic Unit	/01101	1	—	I	—	I	—
54182	Look-Ahead Carry Generator	/01102	1	1	F	W	F	W
54190	Synchronous Up/Down Counter (BCD)	—	—	—	—	—	*	*
54191	Synchronous Up/Down Counter (Binary)	—	—	—	—	—	*	*
54192	Synchronous Decade Up/Down Counter	/01308	*	*	F	W	F	W
54193	Synchronous 4-Bit Binary Up/Down Counter	/01309	*	*	F	W	F	W
54194	4-Bit Bidirectional Universal Shift Register	/00905	*	*	F	W	F	W
54195	4-Bit Parallel-Access Shift Register	/00906	*	*	F	W	F	W
54198	8-Bit Shift Register	—	—	—	—	—	I	Q
54199	8-Bit Shift Register	—	—	—	—	—	—	—
54221	Dual Monostable Multivibrator	—	—	—	—	—	F	W
54279	Quad S-R Latch	—	—	—	—	—	F	W
54298	Quad 2-Input Mux with Storage	—	—	—	—	—	F	W
54365	Hex Buffer w/Common Enable (3-State)	/16301	*	*	*	*	*	*
54366	Hex Buffer w/Common Enable (3-State)	/16302	*	*	*	*	F	W
54367	Hex Buffer, 4-Bit and 2-Bit (3-State)	/16303	*	*	*	*	F	W
54368	Hex Buffer, 4-Bit and 2-Bit (3-State)	/16304	*	*	*	*	F	W

NOTE

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* = In process

LOGIC—54H SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		JAN PROC-ESSED		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK	DIP	FLATPACK
54H00	Quad 2-Input NAND Gate	/02304	1	1	F	W	F	W
54H01	Quad 2-Input NAND Gate with o/c	/02306	1	1	F	W	F	W
54H04	Hex Inverter	/02305	1	1	F	W	F	W
54H05	Hex Inverter with o/c	—	—	—	—	—	F	W
54H08	Quad 2-Input AND Gate	/15501	2	—	F	—	F	W
54H10	Triple 3-Input NAND Gate	/02303	1	1	F	W	F	W
54H11	Triple 3-Input NAND Gate	/15502	2	—	F	—	F	W
54H20	Dual 4-Input NAND Gate	/02302	1	1	F	W	F	W
54H21	Dual 4-Input AND Gate	/15503	2	—	F	—	F	W
54H22	Dual 4-Input NAND Gate with o/c	/02307	1	—	F	W	F	W
54H30	8-Input NAND Gate	/02301	1	1	F	W	F	W
54H40	Dual 4-Input NAND Buffer	/02401	1	1	F	W	F	W
54H50	Expandable Dual 2-Wide 2-Input A01	/04001	1	1	F	W	F	W
54H51	Dual 2-Wide 2-Input A01 Gate	/04002	1	1	F	W	F	W
54H52	Expandable 4-Wide 2-2-2-3 Input AND-OR Gate	—	—	—	—	—	F	W
54H53	4-Wide 2-Input A01 Gate (Expandable)	/04003	1	1	F	W	F	W
54H54	4-Wide 2-Input A01 Gate	/04004	1	1	F	W	F	W
54H55	2-Wide 2-Input A01 Gate	/04005	1	1	F	W	F	W
54H60	Dual 4-Input Expander	—	—	—	—	—	F	W
54H61	Triple 3-Input Expander	—	—	—	—	—	F	W
54H62	3-2-2-3 Input AND-OR Expander	—	—	—	—	—	F	W
54H71	J-K Master-Slave Flip-Flop with AND-OR Inputs	—	—	—	—	—	F	W
54H72	J-K Master-Slave Flip-Flop	/02201	1	1	F	W	F	W
54H73	Dual J-K Master-Slave Flip-Flop	/02202	1	1	F	W	F	W
54H74	Dual D-Type Edge-Triggered Flip-Flop	/02203	1	1	F	W	F	W
54H76	Dual J-K Master-Slave Flip-Flop	/02204	1	1	F	W	F	W
54H101	J-K Negative Edge-Triggered Flip-Flop	/02205	1	1	F	W	F	W
54H102	J-K Negative Edge-Triggered Flip-Flop	—	—	—	—	—	F	W
54H103	Dual J-K Negative Edge-Triggered Flip-Flop	/02206	1	1	F	W	F	W
54H106	Dual J-K Negative Edge-Triggered Flip-Flop	—	—	—	—	—	F	W
54H108	Dual J-K Negative Edge-Triggered Flip-Flop	—	—	—	—	—	F	—

NOTE

Per QPL 38510-28 dated 1 April 1977.
1 = Level 1 Qualification
2 = Level 2 Qualification

LOGIC—54LS SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		JAN PROCESSED		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK	DIP	FLATPACK
54LS00	Quad 2-Input NAND Gate	/30001	2	2	F	W	F	W
54LS01	Quad 2-Input NAND Gate with o/c	—	—	—	F	W	F	W
54LS02	Quad 2-Input NOR Gate	/30301	2	2	F	W	F	W
54LS03	Quad 2-Input NAND Gate with o/c	/30002	1	1	F	W	F	W
54LS04	Hex Inverter	/30003	1	1	F	W	F	W
54LS05	Hex Inverter with o/c	/30004	1	1	F	W	F	W
54LS08	Quad 2-Input AND Gate	/31004	2	2	F	W	F	W
54LS09	Quad 2-Input AND Gate with o/c	—	—	—	—	—	F	W
54LS10	Triple 3-Input NAND Gate	/30005	1	1	F	W	F	W
54LS11	Triple 3-Input NAND Gate	/31001	2	2	F	W	F	W
54LS12	Triple 3-Input NAND Gate with o/c	/30006	1	1	F	W	F	W
54LS13	Dual NAND Schmitt Trigger	/31301	*	*	F	W	F	W
54LS14	Hex Schmitt Trigger	/31302	*	*	F	W	F	W
54LS15	Triple 3-Input AND Gate with o/c	/31002	2	2	F	W	F	W
54LS20	Dual 4-Input NAND Gate	/30007	1	1	F	W	F	W
54LS21	Dual 4-Input AND Gate	/31003	2	2	F	W	F	W
54LS22	Dual 4-Input NAND Gate with o/c	/30008	1	1	F	W	F	W
54LS26	Quad 2-Input NAND Gate with o/c	/32101	*	*	F	W	F	W
54LS27	Triple 3-Input NOR Gate	/30302	2	2	F	W	F	W
54LS28	Quad 2-Input NOR Buffer	/30204	*	*	F	W	F	W
54LS30	8-Input NAND Gate	/30009	2	2	F	W	F	W
54LS32	Quad 2-Input OR Gate	/30501	2	2	F	W	F	W
54LS33	Quad 2-Input NOR Buffer with o/c	—	—	—	—	—	F	W
54LS37	Quad 2-Input NAND Buffer	/30202	2	2	F	W	F	W
54LS38	Quad 2-Input NAND Buffer with o/c	/30203	*	*	F	W	F	W
54LS40	Dual 4-Input NAND Buffer	/30201	2	2	F	W	F	W
54LS42	BCD-to-Decimal Decoder	/30703	*	*	*	*	F	W
54LS51	Dual 2-Wide 2-Input A01 Gate	/03401	2	2	F	W	F	W
54LS54	4-Wide 2-Input A01 Gate	/30402	2	2	F	W	F	W
54LS55	2-Wide 4-Input A01 Gate	—	—	—	—	—	F	W
54LS73	Dual J-K Master-Slave Flip-Flop	/30101	—	—	—	—	F	W
54LS74	Dual D-Type Edge-Triggered Flip-Flop	/30102	*	*	F	W	F	W
54LS75	Quad Bistable Latch	—	—	—	F	W	F	W
54LS76	Dual J-K Master-Slave Flip-Flop	/30110	*	*	F	W	F	W
54LS78	Quad Bistable Latch	—	—	—	—	—	F	W
54LS83A	4-Bit Binary Full Adder	/31201	*	*	F	W	F	W
54LS85	4-Bit Magnitude Comparator	/31101	*	*	F	W	F	W
54LS86	Quad 2-Input Exclusive-OR Gate	/30502	*	*	F	W	F	W
54LS90	Decade Counter	/31501	*	*	F	W	F	W
54LS92	Divide-by-Twelve Counter	/31510	*	*	F	W	F	W
54LS93	4-Bit Binary Counter	/31502	*	*	F	W	F	W
54LS95	4-Bit Left-Right Shift Register	/30603	*	*	F	W	F	W
54LS96	5-Bit Shift Register	/30604	*	*	F	W	F	W

NOTE

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LOGIC—54LS SERIES (Cont'd)

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		JAN PROC-ESSED		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK	DIP	FLATPACK
54LS107	Dual J-K Master-Slave Flip-Flop	/30108	*	*	F	W	F	W
54LS109	Dual J-K Positive Edge-Triggered Flip-Flop	/30109	*	*	F	W	F	W
54LS112	Dual J-K Negative Edge-Triggered Flip-Flop	/30103	*	*	F	W	F	W
54LS113	Dual J-K Negative Edge-Triggered Flip-Flop	/30104	*	*	F	W	F	W
54LS114	Dual J-K Negative Edge-Triggered Flip-Flop	/30105	*	*	F	W	F	W
54LS122	Retriggerable Monostable Multivibrator	/31403	—	—	—	—	—	—
54LS125	Quad Bus Buffer Gate w/Tri-State Outputs	/32301	*	*	*	*	F	W
54LS126	Quad Bus Buffer Gate w/Tri-State Outputs	/32302	*	*	*	*	F	W
54LS132	Quad Schmitt Trigger	/31303	*	*	F	W	F	W
54LS136	Quad Exclusive-OR with o/c	—	—	—			F	W
54LS138	3-to-8 Line Decoder/Demux	/30701	*	*	*	*	F	W
54LS139	Dual 2-to-4 Line Decoder/ Demux	/30702	*	*	*	*	F	W
54LS145	BCD to Decimal Decoder/Dye	—	—	—	—	—	F	W
54LS151	8-Line to 1-Line Mux	/30901	*	*	*	*	*	*
54LS153	Dual 4-Line to 1-Line Mux	/30902	*	*	F	W	F	W
54LS154	4-Line to 16-Line Decoder/ Demux	—	—	—	—	—	I	Q
54LS155	Dual 2-Line to 4-Line Decoder/Demux	—	—	—	—	—	F	W
54LS157	Quad 2-Input Data Selector (non-inv.)	/30903	*	*	F	W	F	W
54LS158	Quad 2-Input Data Selector (inv.)	/30904	*	*	F	W	F	W
54LS160	Synchronous 4-Bit Decade Counter	/31503	*	*	*	*	F	W
54LS161	Synchronous 4-Bit Binary Counter	/31504	*	*	F	W	F	W
54LS162	Synchronous 4-Bit Decade Counter	/31511	*	*	*	*	F	W
54LS163	Synchronous 4-Bit Binary Counter	/31512	*	*	*	*	F	W
54LS164	8-Bit Parallel-Out Serial Shift Register	/30605	*	*	F	W	F	W
54LS170	4X4 Register File	—	—	—	—	—	F	W
54LS173	Quad D-Type Flip-Flop (Tri-State) (8T10)	—	—	—	—	—	F	W
54LS174	Hex D-Type Flip-Flop with Clear	/30106	*	*	F	W	F	W
54LS175	Quad D-Type Edge-Triggered Flip-Flop	/30107	*	*	F	W	F	W
54LS181	4-Bit Arithmetic Logic Unit	/03801	2	—	I	—	I	Q
54LS190	Synchronous Up/Down Counter (BCD)	/31513	*	*	F	W	F	W
54LS191	Synchronous Up/Down Counter (Binary)	/31509	*	*	F	W	F	W

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LOGIC—54LS SERIES (Cont'd)

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		JAN PROC-ESSED		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK	DIP	FLATPACK
54LS192	Synchronous Decade Up/Down Counter	/31507	*	*	F	W	F	W
54LS193	Synchronous 4-Bit Binary Up/Down Counter	/31508	*	*	F	W	F	W
54LS194	4-Bit Bidirectional Universal Shift Register	/30601	*	*	*	*	*	*
54LS195	4-Bit Parallel-Access Shift Register	/30602	*	*	*	*	*	*
54LS196	Presettable Decade Counter/ Latch (8290)	/31601	*	*	*	*	*	*
54LS197	Presettable Binary Counter/ Latch (8291)	/31602	*	*	*	*	*	*
54LS221	Dual Monostable Multivibrator	/31402	*	*	*	*	*	*
54LS251	Data Selector/Mux with 3-State Outputs	/30905	*	*	*	*	*	*
54LS253	Dual 4-Line to 1-Line Data Selector/Mux	/30908	*	*	F	W	F	W
54LS257	Quad 2-Line to 1-Line Data Selector/Mux	/30906	*	*	F	W	F	W
54LS258	Quad 2-Line to 1-Line Data Selector/Mux	/30907	*	*	*	*	F	W
54LS260	Dual 5-Input NOR Gate	—	—	—	—	—	F	W
54LS261	2X4 Parallel Binary Multiplier	—	—	—	—	—	F	W
54LS266	Quad Exclusive-NOR Gate	/30303	2	2	F	W	F	W
54LS279	Quad S-R Latch	—	—	—	—	—	F	W
54LS280	9-Bit Odd/Even Parity Generator/Checker	—	—	—	—	—	*	*
54LS283	4-Bit Adder	/31202	*	*	*	*	F	W
54LS290	Decade Counter	/32003	*	*	F	W	F	W
54LS293	4-Bit Binary Counter	/32004	*	*	F	W	F	W
54LS295A	4-Bit Right-Shift Left-Shift Register	/30606	*	*	*	*	F	W
54LS298	Quad 2-Input Mux with Storage	—	—	—	—	—	F	W
54LS365	Hex Buffer w/Common Enable (3-State)	/32201	*	*	*	*	F	W
54LS366	Hex Buffer w/Common Enable (3-State)	/32202	*	*	*	*	F	W
54LS367	Hex Buffer, 4-Bit and 2-Bit (3-State)	/32203	*	*	*	*	F	W
54LS368	Hex Buffer, 4-Bit and 2-Bit (3-State)	/32204	*	*	*	*	F	W
54LS375	Quad Latch	—	—	—	—	—	F	W
54LS386	Exclusive-OR Gate	—	—	—	—	—	F	W
54LS395	4-Bit Cascadeable Shift Register (3-State)	/30607	*	*	*	*	F	W
54LS445	BCD to Decimal Decoder/Dye	—	—	—	—	—	F	W
54LS670	4X4 Register File (Tri-State)	—	—	—	—	—	F	W

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LOGIC—54S SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		JAN PROC-ESSED		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK	DIP	FLATPACK
54S00	Quad 2-Input NAND Gate	/07001	1	1	F	W	F	W
54S02	Quad 2-Input NOR Gate	/07301	2	2	F	W	F	W
54S03	Quad 2-Input NAND Gate with o/c	/07002	2	2	F	W	F	W
54S04	Hex Inverter	/07003	1	1	F	W	F	W
54S05	Hex Inverter with o/c	/07004	1	1	F	W	F	W
54S08	Quad 2-Input AND Gate	/08003	*	*	F	W	F	W
54S09	Quad 2-Input AND Gate with o/c	/08004	—	—	—	—	F	W
54S10	Triple 3-Input NAND Gate	/07005	2	2	F	W	F	W
54S11	Triple 3-Input NAND Gate	/08001	2	2	F	W	F	W
54S15	Triple 3-Input AND Gate with o/c	/08002	2	2	F	W	F	W
54S20	Dual 4-Input NAND Gate	/07006	2	2	F	W	F	W
54S22	Dual 4-Input NAND Gate with o/c	/07007	1	1	F	W	F	W
54S30	8-Input NAND Gate	/07008	—	—	—	—	—	—
54S32	Quad 2-Input OR Gate	—	—	—	—	—	F	W
54S40	Dual 4-Input NAND Buffer	/07201	2	2	F	W	F	W
54S51	Dual 2-Wide 2-Input A01 Gate	/07401	2	2	F	W	F	W
54S64	4-2-3-2 Input A01 Gate	/07402	2	2	F	W	F	W
54S65	4-2-3-2 Input A01 Gate	/07403	2	2	F	W	F	W
54S74	Dual D-Type Edge-Triggered Flip-Flop	/07101	2	2	F	W	F	W
54S85	4-Bit Magnitude Comparator	/08201	*	—	F	—	F	—
54S86	Quad 2-Input Exclusive-OR Gate	/07501	2	2	F	W	F	W
54S112	Dual J-K Negative Edge-Triggered Flip-Flop	/07102	—	—	—	—	F	W
54S113	Dual J-K Negative Edge-Triggered Flip-Flop	/07103	—	—	—	—	F	W
54S114	Dual J-K Negative Edge-Triggered Flip-Flop	/07104	—	—	—	—	F	W
54S133	13-Input NAND Gate	/07009	2	2	F	W	F	W
54S134	12-Input NAND Gate w/Tri-State Outputs	/07010	2	2	F	W	F	W
54S135	Quad Exclusive-OR/NOR Gate	/07502	—	—	—	—	—	—
54S138	3-to-8 Line Decoder/Demux	/07701	—	—	—	—	—	—
54S139	Dual 2-to-4 Line Decoder/ Demux	/07702	—	—	—	—	F	W
54S140	Dual 4-Input NAND Line Driver	/08101	2	2	F	W	F	W
54S151	8-Line to 1-Line Mux	/07901	2	2	F	W	F	W
54S153	Dual 4-Line to 1-Line Mux	/07902	2	2	F	W	F	W
54S157	Quad 2-Input Data Selector (non.inv.)	/07903	2	2	F	W	F	W
54S158	Quad 2-Input Data Selector (inv.)	/07904	*	*	F	W	F	W
54S174	Hex D-Type Flip-Flop with Clear	/07106	—	—	—	—	*	*
54S175	Quad D-Type Edge-Triggered Flip-Flop	/07105	—	—	—	—	*	*
54S181	4-Bit Arithmetic Logic Unit	/07801	*	—	I	—	I	*
54S182	Look-Ahead Carry Generator	/07802	—	—	—	—	*	*
54S194	4-Bit Bidirectional Universal Shift Register	/07601	—	—	—	—	—	—
54S195	4-Bit Parallel-Access Shift Register	/07602	—	—	—	—	—	—

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LOGIC—54S SERIES (Cont'd)

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		JAN PROC-ESSED		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK	DIP	FLATPACK
54S251	Data Selector/Mux with 3-State Outputs	/08905	—	—	—	—	—	—
54S253	Dual 4-Line to 1-Line Data Selector/Mux	—	—	—	—	—	F	W
54S257	Quad 2-Line to 1-Line Data Selector/Mux	/07906	—	—	—	—	—	—
54S258	Quad 2-Lint to 1-Line Data Selector/Mux	/07907	—	—	—	—	—	—
54S260	Dual 5-Input NOR Gate	—	—	—	—	—	F	W
54S280	9-Bit Odd/Even Parity Generator/Checker	/07703	—	—	—	—	—	—
54S350	4/6 Bit Shifter-Tri-State	—	—	—	—	—	F	—

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LOGIC—8200/9300/9600 SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUALIFIED*		JAN PROCESSED		MIL REL/883 MIL TEMP	
			Dip	Flat Pack	Dip	Flat Pack	Dip	Flat Pack
8200	Dual 5-Bit Buffer Register	—	—	—	—	—	I	Q
8201	Dual 5-Bit Buffer Register with D Inputs	—		—	—	—	I	Q
8202	10-Bit Buffer Register	—	—	—	—	—	I	Q
8203	10-Bit Buffer Register with D Inputs	—	—	—	—	—	I	Q
8230	8-Input Digital Multiplexer	/01402	*	*	F	W	F	W
8231	8-Input Digital Multiplexer	—	—	—	—	—	F	W
8232	8-Input Digital Multiplexer	—	—	—	—	—	F	W
8233	2-Input 4-Bit Digital Multiplexer	—	—	—	—	—	F	W
8234	2-Input 4-Bit Digital Multiplexer		—	—	—	—	F	W
8235	2-Input 4-Bit Digital Multiplexer	—	—	—	—	—	F	W
8241	Quad Exclusive-OR Gate	—	—	—	—	—	F	W
8242	Quad Exclusive-NOR Gate	—	—	—	—	—	F	W
8243	8-Bit Position Scaler	—	—	—	—	—	I	Q
8250	Binary-to-Octal Decoder	/15204	2	2	F	W	F	W
8251	BCD-to-Decimal Decoder	/15205	2	2	F	W	F	W
8252	BCD-to-Decimal Decoder	/15206	2	2	F	W	F	W
8260	Arithmetic Logic Unit	—	—	—	—	—	I	Q
8261	Fast Carry Extender	—	—	—	—	—	F	W
8262	9-Bit Parity Generator and Checker	—	—	—	—	—	F	W
8263	3-Input 4-Bit Digital Multiplexer	—	—	—	—	—	I	Q
8264	3-Input 4-Bit Digital Multiplexer		—	—	—	—	I	Q
8266	2-Input 4-Bit Digital Multiplexer	—	—	—	—	—	F	W
8267	2-Input 4-Bit Digital Multiplexer	—	—	—	—	—	F	W
8268	Gated Full Adder	—	—	—	—	—	F	Q
8269	4-Bit Comparator	—	—	—	—	—	F	W
8270	4-Bit Shift Register	—	—	—	—	—	F	W
8271	4-Bit Shift Register	—	—	—	—	—	F	W
8273	10-Bit Serial-In, Parallel-Out Shift Register	—	—	—	—	—	F	W
8274	10-Bit Parallel-In, Serial-Out Shift Register	—	—	—	—	—	F	W
8275	Quad Bistable Latch	—	—	—	—	—	F	W
8276	8-Bit Serial Shift Register	—	—	—	—	—	F	—
8277	Dual 8-Bit Shift Register	—	—	—	—	—	F	—
8280	Presettable Decade Counter	—	—	—	—	—	F	W
8281	Presettable Binary Counter	—	—	—	—	—	F	W
8284	Binary Up/Down Counter	—	—	—	—	—	F	W
8285	Decade Up/Down Counter	—	—	—	—	—	F	W
8288	Divide-by-Twelve Counter	—	—	—	—	—	F	W
8290	Presettable High Speed Decade Counter	—	—	—	—	—	F	W
8291	Presettable High Speed Binary Counter	—	—	—	—	—	F	W
8292	Presettable Low Power Decade Counter	—	—	—	—	—	F	W
8293	Presettable Low Power Binary Counter	—	—	—	—	—	F	W
9300	4-Bit Shift Register	/15901	*	*	F	W	F	W
9301	BCD to Decimal Decoder	/15206	2	2	F	W	F	W
9308	Dual 4-Bit Latch w/Clear	—	—	—	—	—	I	Q
9309	Dual 4-Input Multiplexer	/01404	I	I	F	W	F	W
9310	4-Bit Decade Counter	—	—	—	—	—	F	W
9312	8-Input Digital Multiplexer	/01402	*	*	F	W	F	W
9316	4-Bit Binary Counter	—	—	—	—	—	F	W
9322	Data Selector-Multiplexer	—	—	—	—	—	F	W
9324	5-Bit Comparator	/15002	*	*	F	WF	W	—
9334	8-Bit Addressable Latch	/16001	—	—	—	—	F	W
9602	Dual Monostable Multivibrator	—	*	*	F	W	F	W

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LOGIC—8T INTERFACE SERIES

DEVICE	DESCRIPTION	JAN M38510 SHEET	MIL REL/883 MIL TEMP	
			Dip	Flat Pack
8T04	7-Segment Decoder Display Driver (Active-Low Outputs)	—	F	W
8T05	7-Segment Decoder Display Driver (Active-Hi Outputs)	—	F	W
8T06	7-Segment Decoder Display Driver (Active-Low Outputs)	—	F	W
8T09	Quad Bus Driver with Tri-State Outputs	—	F	W
8T10	Quad D-Type Bus Latch (Tri-State)	—	F	W
8T13	Dual Line Driver	—	F	W
8T14	Triple Line Receiver/Schmitt Trigger	—	F	W
8T18	Dual 2-Input NAND (High Voltage to TTL Interface)	—	F	W
8T20	Bidirectional Monostable Multivibrator (Diff. Input)	—	*	*
8T22	Retriggerable Monostable Multivibrator (54122/9601)	—	F	W
8T26A	Quad Bus Driver/Receiver (Tri-State Outputs)	—	F	W
8T28	Quad Non-Inverting Bus Driver/Receiver (Tri-State Outputs)	—	F	W
8T31	8-Bit Bidirectional I/O Port	—	*	*
8T32	Programmable 8-Bit, I/O Port (3-State)	—	I	*
8T33	Programmable 8-Bit, I/O Port (Open Collector)	—	I	*
8T35	Asynchronous Programmable 8-Bit I/O Port (Open Collector)	—	I	*
8T37	Hex Bus Receiver with Hysteresis—Schmitt Trigger (DM8837)		F	W
8T38	Quad Bus Transceiver (Open Collector) (DM8838)	—	F	W
8T80	Quad 2-Input NAND Gate (High Voltage)	—	F	W
8T90	Hex Inverter (High Voltage)	—	F	W
8T95	High Speed Hex Buffers/Inverters (74365/DM8095)	—	F	W
8T96	High Speed Hex Buffers/Inverters (74366/DM8096)	—	F	W
8T97	High Speed Hex Buffers/Inverters (74367/DM8097)		F	W
8T98	High Speed Hex Buffers/Inverters (74368/DM8098)		F	W

* = Qualification planned

BIPOLAR MEMORIES CROSS REFERENCE

DEVICE	ORGANIZATION	PACKAGE*		FAIRCHILD	HARRIS	MMI	INTERSIL	AMD	TI
PROMs									
82S23	32X8	F	R	—	7602-2	5330	5600	27S08	54S188
82S115	512X8	I	R	—	7644-2	—	—	—	
82S123	32X8	F	R	—	7603-2	5331	5610	27S09	54S288
82S126	256X4	F	R	93416	7610-2	5300	5603	27S10	54S387
82S129	256X4	F	R	93426	7611-2	5301	5623	27S11	54S287
82S130	512X4	F	R	93436	7620-2	5305	5604	—	—
82S131	512X4	F	R	93446	7621-2	5306	5624	—	—
82S136	1024X4	F,I	R	93443	7642-2	5352	5606	—	—
82S137	1024X4	F,I	R	93453	7643-2	5353	5626	—	—
82S140	512X8	I	R	93438	7640-2	5340	5606	—	—
82S141	512X8	I	R	93448	7641-2	5341	5625	—	—
82S180	1024X8	I	R	—	—	5380	—	—	—
82S181	1024X8	I	R	—	—	5381	—	—	—
82S184	2048X4	I	R	—	—	—	—	—	—
82S185	2048X4	I	R	—	—	—	—	—	—
FPLAs									
82S100	16X48X8	I	R	93459	—	82S100	—	27S100	—
82S101	16X48X8	I	R	93458	—	82S101	—	27S101	—
PLAs									
82S200	16X48X8	I	R	—	—	—	—	—	—
82S201	16X48X8	!	R	—	—	—	—	—	—
RAMs									
54S89	16X4	F	R	—	—	—	—	—	5489
54S189	16X4	F	R	—	—	—	—	—	54189
54S200	256X1	F	R	—	—	—	—	—	54S200
54S201	256X1	F	R	—	—	—	—	—	54S201
54S301	256X1	F	R	—	—	—	—	—	54S301
82S09	64X9	I	R	93419	—	—	—	—	—
82S10	1024X1	F,I	R	93415	—	—	55S08	2952	—
82S11	1024X1	F,I	R	93425	—	—	55S18	2953	—
82S16	256X1	F	R	93421	—	5531	5523	2700	—
82S17	256X1	F	R	93411	—	5530	5533	2701	—
82S25	16X4	F	R	93403	0064	5560	5501	3101	—
ROMs									
82S15	512X8								
82S223	32X8								
82S224	32X8								
82S226	256X4								
82S229	256X4								
82S230	512X4								
82S231	512X4								
82S280	1024X8								
82S281	1024X8								

*NOTE

R = BeO Flat Pack
F = Cerdip
I = Ceramic DIP

LINEAR MIL REL/883 MIL TEMP.

DEVICE	DESCRIPTION	PACKAGE	
	COMPARATORS		
SE521	Dual Comparator	F	
SE526	Analog Voltage Comparator	F	K
SE527	Analog Voltage Comparator	F	K
SE529	Analog Voltage Comparator	F	K
LH2111	Dual Comparator	F	
LM111	Comparator	F	T
LM119	Dual Comparator	F	K
LM139	Quad Comparator	F	
LM193/193A	Dual Comparator		T
μA710	Differential Voltage Comparator	F	T
μA711	Comparator	F	K
	DIFFERENTIAL AMPLIFIERS		
SE510	Dual Differential Amplifier	F	
SE511	Dual Differential Amplifier	F	
SE515	Differential Amplifier	F	K
μA733	Video Amplifier	F	K
	OPERATIONAL AMPLIFIERS		
LF155/156	FET Op Amp	T	
LH2101A	Dual Op Amp	F	
LH2108A	Dual Op Amp	F	
LM101	High Perf. Op Amp	F	T
LM101A	High Perf. Op Amp	F	T
LM107	General Purpose Op Amp	F	F
LM108	Precision Op Amp	F	T
LM108A	Precision Op Amp	F	T
LM124	Quad Op Amp	F	
LM158	Dual Op Amp		T
MC1556	Op Amp	F	T
MC1558	Dual Op Amp	F	T
SE532	Dual Op Amp	—	T
SE535	Hi Slew Rate Op Amp	T	
SE538	Hi Slew Rate Op Amp	T	
μA709	Op Amp	F	T
μA709A	Op Amp	F	T
μA741	General Purpose Op Amp	F	T
μA747	Dual Op Amp	F	K
μA748	General Purpose Op Amp	F	T

DEVICE	DESCRIPTION	PACKAGE	
	PHASE LOCKED LOOPS		
SE567	Tone Decoder P11	F	T
	LINE RECEIVERS		
DM7820	Dual Differential Line Receiver	F	
DM7830	Dual Differential Line Receiver	F	
	TIMERS		
SE555	Timer	F	T
SE556	Dual Timer	F	
SE558/9	Quad Timer	F	
	VOLTAGE REGULATORS		
LM109	5 Volt Regulator	DA	
SE5554	Dual Track Reg	F	
78XX (7)	Positive Reg	DA	
79XX (7)	Negative Reg	DA	
79MXX (7)	Med Power Reg	DB	
μA723	Precision Voltage Regulator	F	L
	DRIVERS		
DS1611-1614	Peripheral Drivers		T
	D/A		
MC1508-8	8-Bit D/A	F	
SE5008	8-Bit D/A	F	
SE5009	8-Bit D/A	F	

BIPOLAR MICROPROCESSORS

PRODUCT	DESCRIPTION	AVAILABILITY	
		Dip	Flat Pack
3001	Microprogram Control Unit	I	R
3002	Central Processing Element (2-bit slice)	I	R
8X300	Interpreter/Microcontroller	I	*
2901-1	Central Processing Element (4-bit slice)	*	*

*Under development

MICROPROCESSOR SUPPORT CIRCUITS

PRODUCT	DESCRIPTION	AVAILABILITY	
		Dip	Flatpack
LOGIC			
54123	Retriggerable Monostable Multivibrator	F	W
54180	8-Bit Odd/Even Parity Checker	F	W
54298	Quad 2-Input Mux with Storage	F	W
54S182	Look-Ahead Carry Generator	*	*
54S194	4-Bit Bidirectional Shift Register	*	*
54S195	4-Bit Parallel Access Shift Register	*	*
54LS365	High Speed Hex Tri-State Buffer	F	*
54LS366	High Speed Hex Tri-State Buffer	F	*
54LS367	High Speed Hex Tri-State Buffer	F	*
54LS368	High Speed Hex Tri-State Buffer	F	*
8262	9-Bit Parity Generator Checker	F	W
8281	Presettable Binary Counter	F	W
8291	Presettable High Speed Binary Counter	F	W
9602	Dual Monostable Multivibrator	F	W
INTERFACE			
8T09	Quad Bus Driver with Tri-State Output	F	W
8T10	Quad D-Type Bus Latch (Tri-State Outputs)	F	W
8T13	Dual Line Driver	F	W
8T14	Triple Line Receiver/Schmitt Trigger	F	W
8T26A	Quad Bus Driver/Receiver (Tri-State)	F	W
8T28	Quad Bus Non-Inverting Driver/Receiver (Tri-State)	F	W
8T32	Programmable 8-Bit I/O Port (3-State)	I	*
8T33	Programmable 8-Bit I/O Port (Open Collector)	I	*
8T35	Asynchronous Programmable 8-Bit I/O Port (Open Collector)	I	*
8T95	High Speed Hex Buffer (Tri-State)	F	*
8T96	High Speed Hex Inverter (Tri-State)	F	*
8T97	High Speed Hex Buffer (Tri-State)	F	*
8T98	High Speed Hex Inverter (Tri-State)	F	*

*Under development

PACKAGES

INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings.

General

1. Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).
2. Lead spacing shall be measured within this zone.
   a. Shoulder and lead tip dimensions are to centerline of leads.
3. Tolerances non-cumulative
4. Thermal resistance values are determined by utilizing the linear temperature dependence of the forward voltage drop across the substrate diode in a digital device to monitor the junction temperature rise during known power application across VCC and ground. The values are based upon 120 mils square die for plastic packages and a 90 mils square die in the smallest available cavity for hermetic packages. All units were solder mounted to P.C. boards, with standard stand-off, for measurement.

Plastic Only

5. Lead material: Alloy 42 or equivalent, solder dipped.
6. Body material: Plastic
7. Round hole in top corner denotes lead No. 1.
8. Body dimensions do not include molding flash.

Hermetic Only

9. Lead material
   a. Alloy 52—gold plated, or solder dipped.
   b. ASTM alloy F-15 (KOVAR) or equivalent—gold plated, tin plated, or solder dipped.
   c. ASTM alloy F-30 (Alloy 42) or equivalent—tin plated.
   d. ASTM alloy F-15 (KOVAR) or equivalent—gold plated.
   e. ASTM alloy F-15 (KOVAR) or equivalent—tin plated.
10. Body Material
   a. 1010 Steel—nickel plated or tin plate over nickel.
   b. Eyelet, ASTM alloy F-15 or equivalent—gold or tin plated.
   c. Eyelet, ASTM alloy F-15 or equivalent—gold or tin plated, glass body.
   d. Ceramic with glass seal at leads.
   e. BeO ceramic with glass seal at leads.
   f. Ceramic with ASTM alloy F-15 or equivalent.
11. Lid Material
   a. 1010 steel, nickel plated, or tin-plate over nickel, weld seal.
   b. Nickel or tin plated nickel, weld seal.
   c. Ceramic, glass seal.
   d. ASTM alloy F-15 or equivalent, gold plated.
   e. BeO Ceramic with glass seal.
   f. Translucent $A1_2O_3$, glass seal.

PLASTIC PACKAGES

NO. OF LEADS	PACKAGE CODE	θ_{ja}/θ_{jc} (°C/W)	DESCRIPTION[1]	PAGE
Standard Dual-in-Line				
8	NE	162/65		3
14	NH	150/65	TO-116/MO-001	3
16	NJ	137/53	MO-001	3
18	NK	135/53		3
20	NL	135/53		3
22	NM	120/53		3
24	NN	116/53	MO-015	4
28	NQ	116/53	MO-015	4
40	NW[3]	110/50	MO-015	4
Power Dual-in-Line				
14	NHA[2]	95/33	Butterfly	3
16	NJA[2]	95/33	Butterfly	3
18	NKA[2,3]	90/26	Butterfly	3
20	NLA[2,3]	90/26	Butterfly	3
24	NNA[2]	60/23	Butterfly	4
28	NQA[2]	56/21	Butterfly	4
Power				
3	S	200/70	TO-92	5
3	U	75/3	TO-220	5
3 + GND	GB[3]	95/15	Single-in-Line (SIL)	5
4 + GND	GC[3]	95/15	Single-in-Line (SIL)	5
12 + GND	PH/PHA[3]	95/15	Batwing	5

12. Signetics symbol, angle cut, or lead tab denotes Lead No. 1.
13. Recommended minimum offset before lead bend.
14. Maximum glass climb .010 inches.
15. Maximum glass climb or lid skew is .010 inches.
16. Typical four places.
17. Dimension also applies to seating plane.

HERMETIC PACKAGES

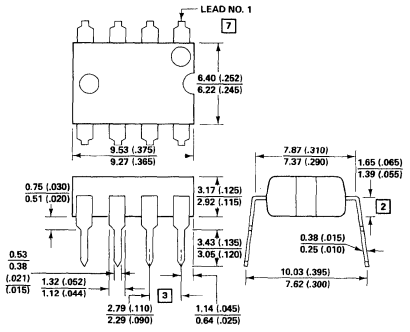
NO. OF LEADS	PACKAGE CODE	θ_{ja}/θ_{jc} (°C/W)	DESCRIPTION[1]	PAGE
Metal Headers				
2	DA	TBD	TO-3 Solid Header	6
3	DB	TBD	TO-39 Solid Header, Short Can	6
4	DC	TBD	TO-72 Solid Header	6
4	DE	TBD	TO-72 Glass Filled Header	6
8	T	150/25	TO-99 Header (.200 Dia.)	7
10	K	150/25	TO-100 Header, Short Can	7
10	L	150/25	TO-100 Header, Tall Can	7
Flat Packs				
10	WF	240/50	Flat Ceramic	8
14	WH	205/50	Flat Ceramic	8
16	WJ	200/50	Flat Ceramic	8
24	WN	155/40	Flat Ceramic	8
16	RJ/RJA	133/30	Flat Ceramic, BeO	8
18	RKA[3]	TBD	Flat Ceramic, BeO	—
24	RNA	TBD	Flat Ceramic, BeO	8
28	RQA	TBD	Flat Ceramic, BeO	9
40	RWA	TBD	Flat Ceramic, BeO	9
10	QF	230/55	Flat Ceramic	9
14	QH	185/45	Flat Ceramic	9
16	QJ	170/45	Flat Ceramic	9
24	QN	155/44	Flat Ceramic	9
10	QFA	230/55	Flat Ceramic Laminate	10
14	QHA	185/45	Flat Ceramic Laminate	10
16	QJA	170/45	Flat Ceramic Laminate	10
24	QNA	155/44	Flat Ceramic Laminate	10
Cerdip Family				
14	FH	110/30	Dual in-Line Ceramic	11
16	FJ	100/30	Dual-in-Line Ceramic	11
18	FK	93/27	Dual-in-Line Ceramic	11
22	FM	75/27	Dual-in-Line Ceramic	11
24	FN	60/26	Dual-in-Line Ceramic	11
Laminated Ceramic, Side Brazed Lead				
8	IEA	100/30	Dip Laminate	12
14	IHA	95/25	Dip Laminate	12
16	IJA	90/25	Dip Laminate	12
18	IKA	88/25	Dip Laminate	12
22	IMA	80/25	Dip Laminate	12
24	INC/IND	65/25	Dip Laminate	12
28	IQA	60/25	Dip Laminate	13
40	IWA	55/25	Dip Laminate	13
50	IZA	TBD	Dip Laminate	13

NOTES

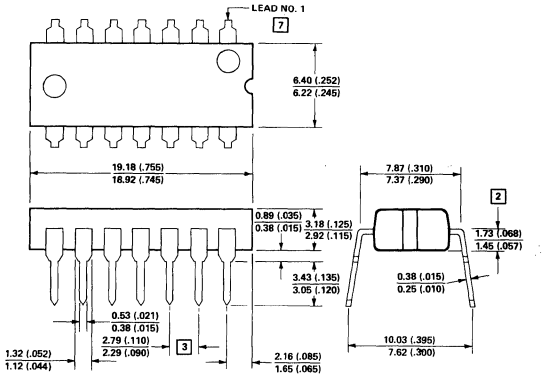
1. Dual-in-Line packages unless otherwise described
2. Package outline is the same as corresponding standard Dual-in-Line package with identical number of leads
3. Package not yet available, scheduled for 1977 release

PLASTIC: Standard and Power Dual-In-Line

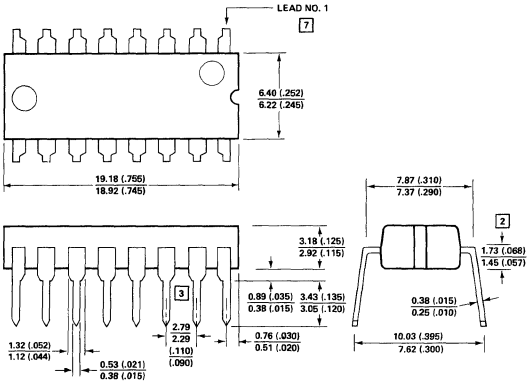
NE Package



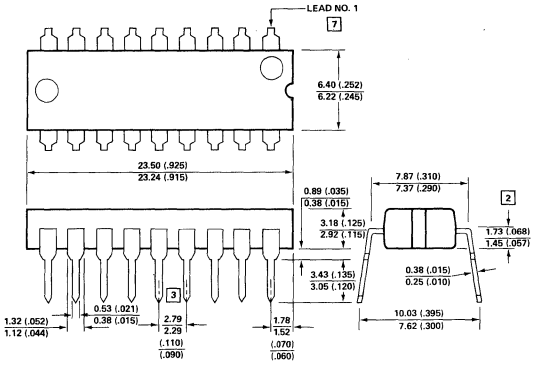
NH Package and NHA Package



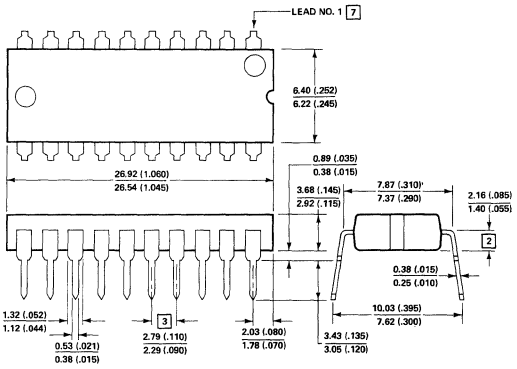
NJ Package and NJA Package



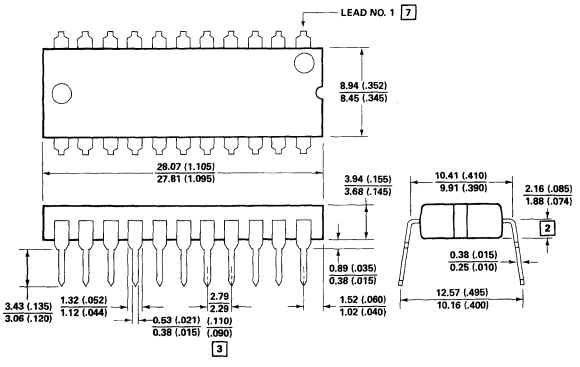
NK Package and NKA Package



NL Package and NLA Package

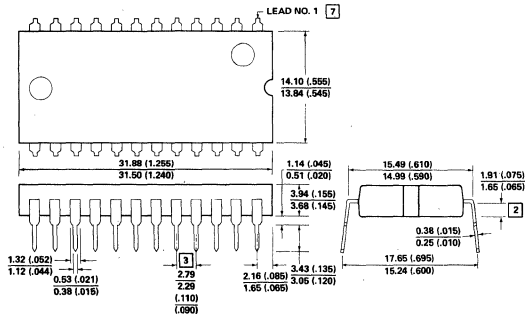


NM Package

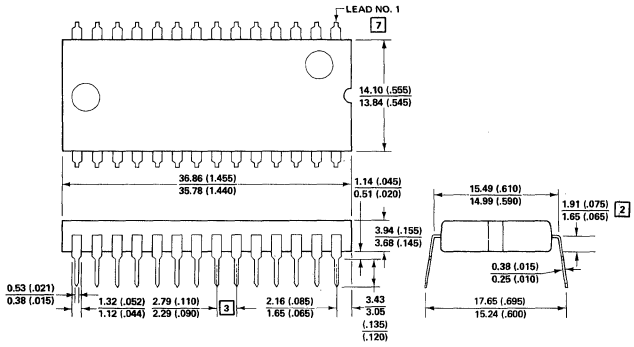


PLASTIC: Standard and Power Dual-In-Line (cont'd.)

NN Package and NNA Package



NQ Package and NQA Package

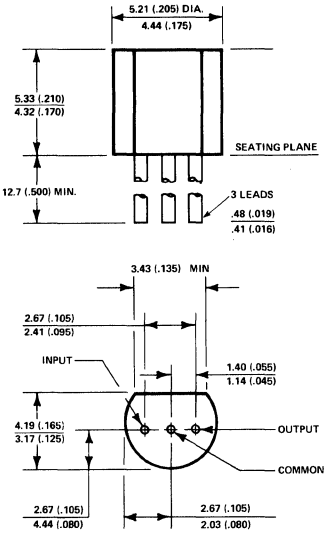


NW Package

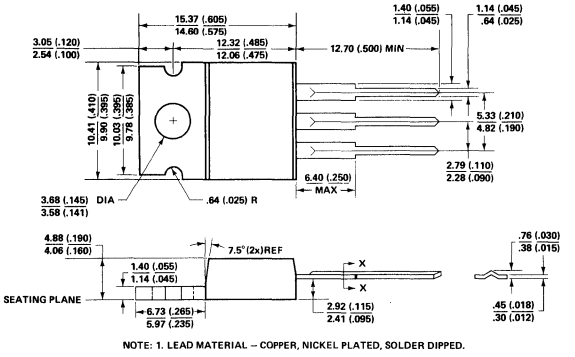
Package not yet available
Scheduled for 1977 release

PLASTIC: Power (Not Dual-In-Line)

S Package



U Package



NOTE: 1. LEAD MATERIAL – COPPER, NICKEL PLATED, SOLDER DIPPED.

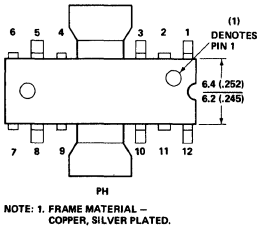
GB Package

Package not yet available
Scheduled for 1977 release

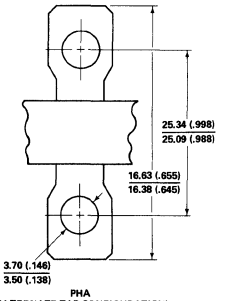
GC Package

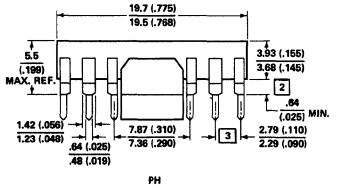
Package not yet available
Scheduled for 1977 release

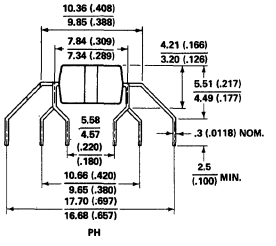
PH/PHA Package



NOTE: 1. FRAME MATERIAL – COPPER, SILVER PLATED.

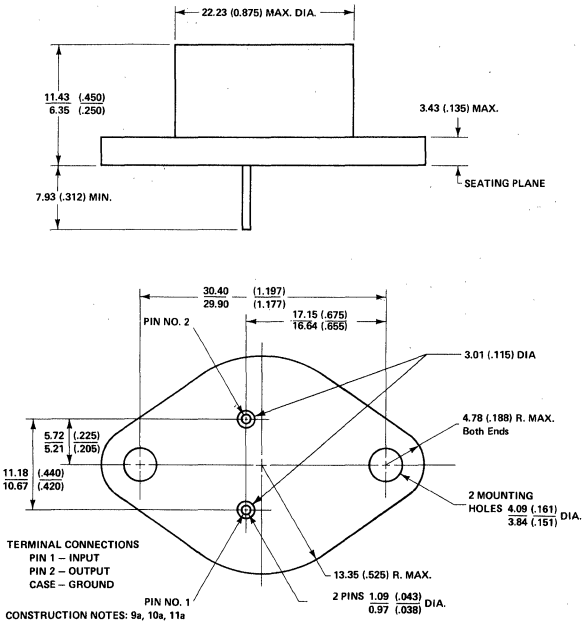






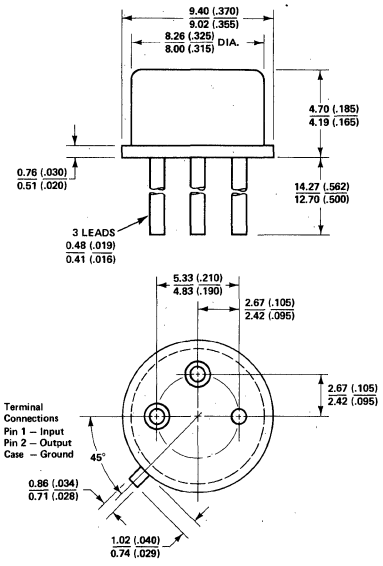
HERMETIC: Metal Headers

DA Package



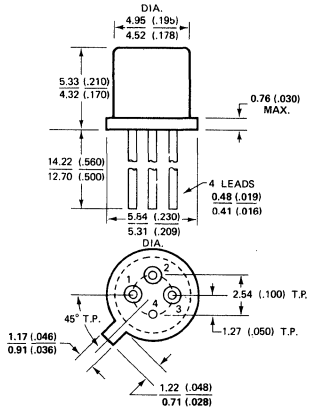
CONSTRUCTION NOTES: 9a, 10a, 11a

DB Package



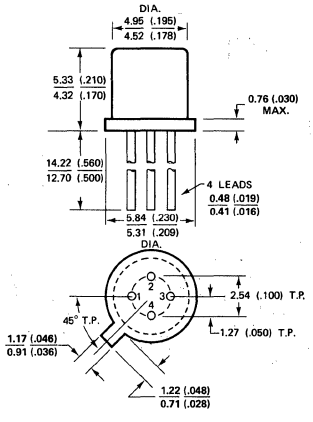
CONSTRUCTION NOTES: 9b, 10b, 11b

DC Package



CONSTRUCTION NOTES: 9b, 10b, 11b

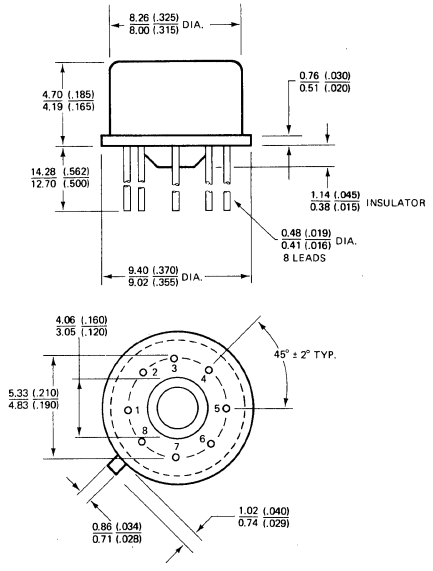
DE Package



CONSTRUCTION NOTES: 9b, 10c, 11b

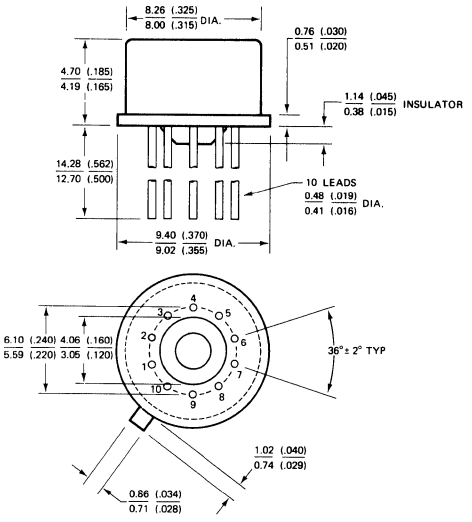
HERMETIC: Metal Headers (cont'd.)

T Package



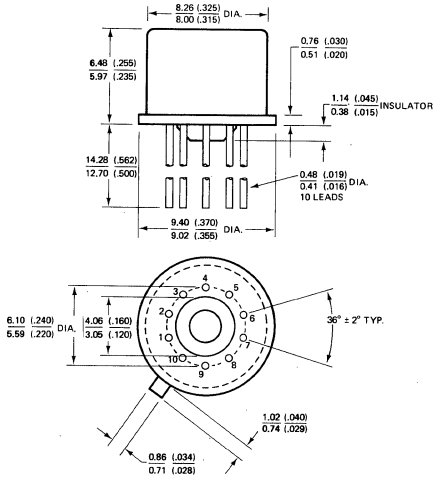
CONSTRUCTION NOTES: 9b, 10c, 11b

K Package



CONSTRUCTION NOTES: 9b, 10c, 11b

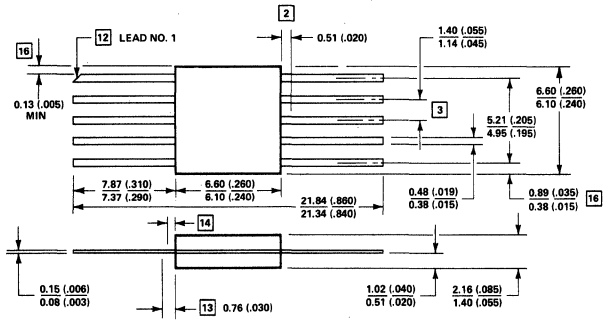
L Package



CONSTRUCTION NOTES: 9b, 10c, 11b

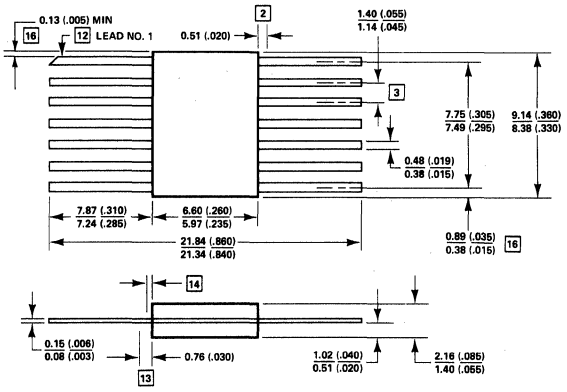
HERMETIC: Flat Packs

WF Package



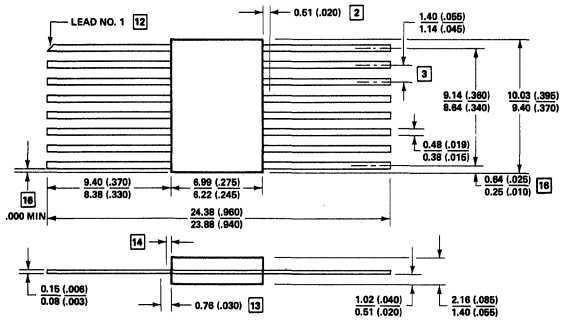
CONSTRUCTION NOTES: 9c, 10d, 11c

WH Package



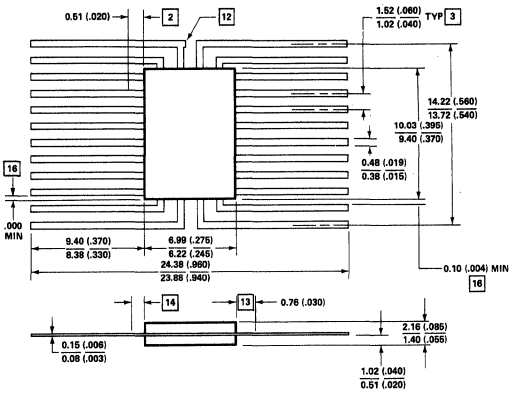
CONSTRUCTION NOTES: 9c, 10d, 11c

WJ Package



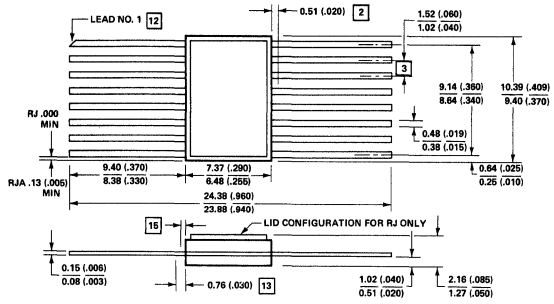
CONSTRUCTION NOTES: 9c, 10d, 11c

WN Package



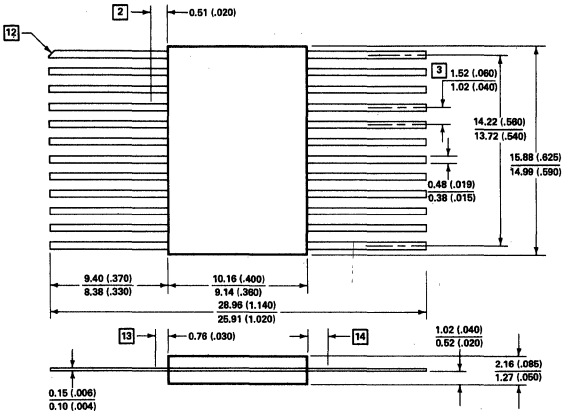
CONSTRUCTION NOTES: 9c, 10d, 11c

RJ and RJA Package



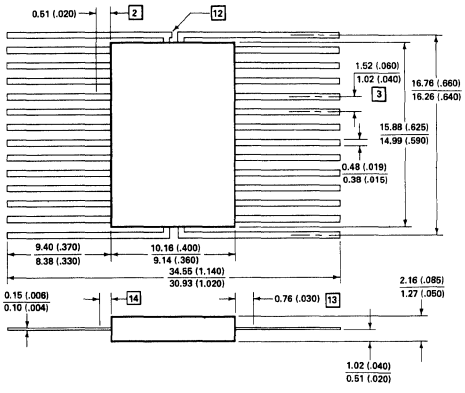
RJA CONSTRUCTION NOTES: 9c, 10e, 11e
RJ CONSTRUCTION NOTES: 9d, 10e, 11d

RNA Package



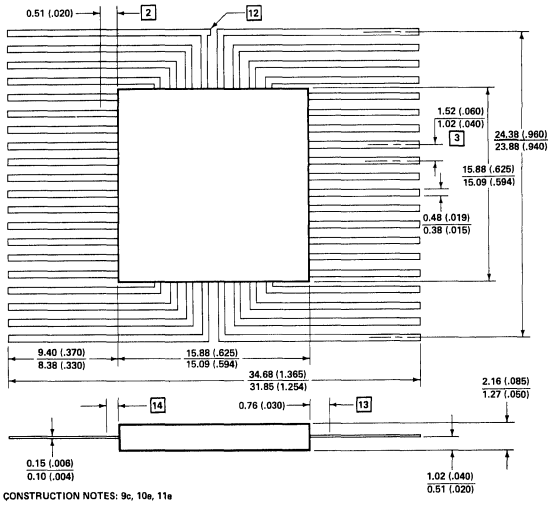
HERMETIC: Flat Packs (cont'd.)

RQA Package



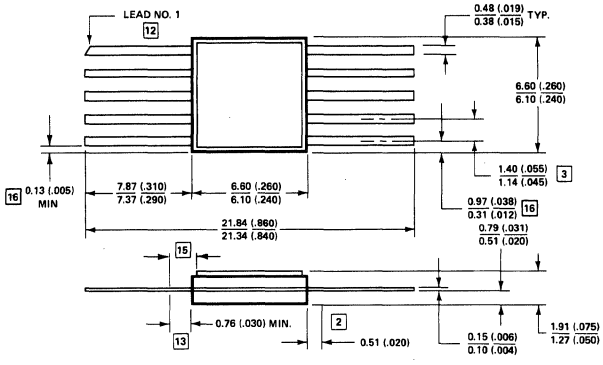
CONSTRUCTION NOTES: 9c, 10e, 11e

RWA Package



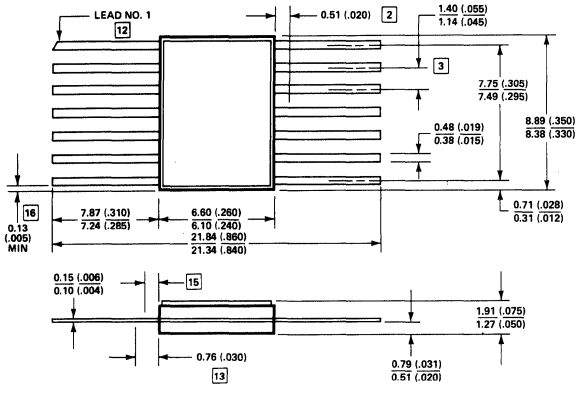
CONSTRUCTION NOTES: 9c, 10e, 11e

QF Package



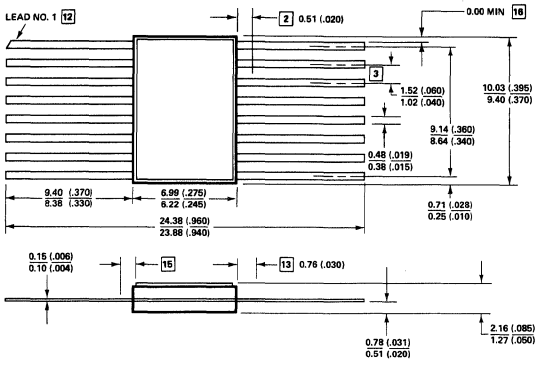
CONSTRUCTION NOTES: 9d, 10d, 11c

QH Package



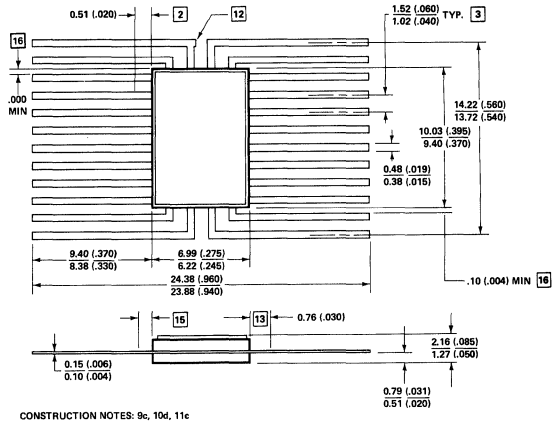
CONSTRUCTION NOTES: 9d, 10d, 11c

QJ Package



CONSTRUCTION NOTES: 9d, 10d, 11c

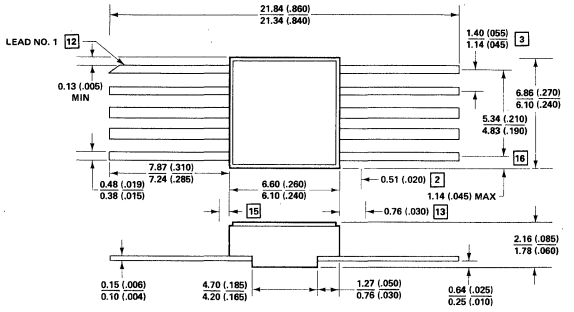
QN Package



CONSTRUCTION NOTES: 9c, 10d, 11c

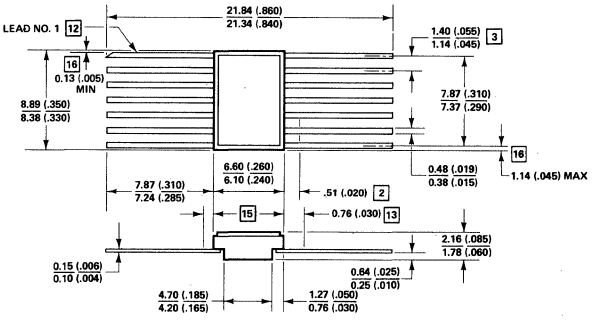
HERMETIC: Flat Packs (cont'd.)

QFA Package



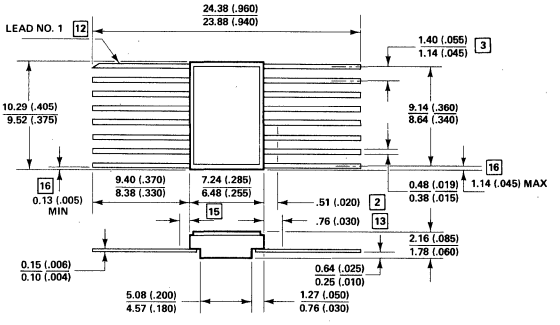
CONSTRUCTION NOTES: 9d, 10f, 11c

QHA Package



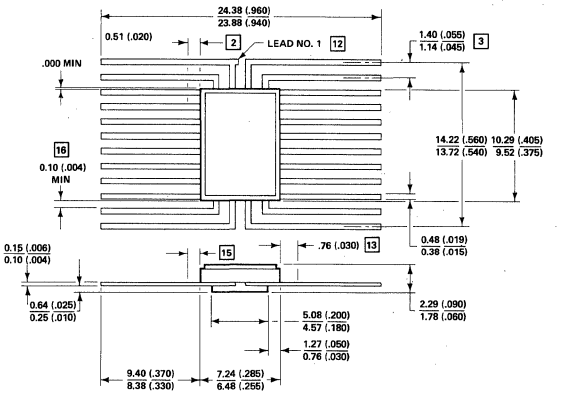
CONSTRUCTION NOTES: 9d, 10f, 11c

QJA Package



CONSTRUCTION NOTES: 9d, 10f, 11c

QNA Package



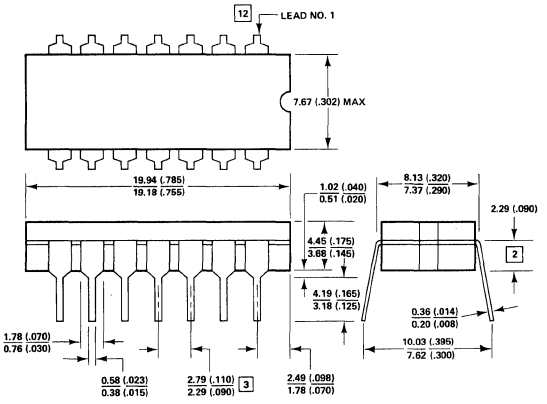
CONSTRUCTION NOTES: 9d, 10f, 11c

RKA Package

Package not yet available
Scheduled for 1977 release

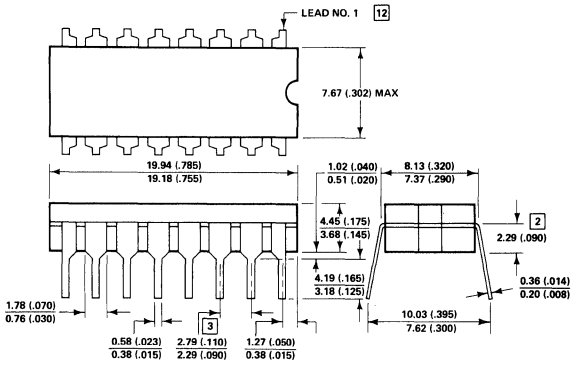
HERMETIC: Cerdip

FH Package



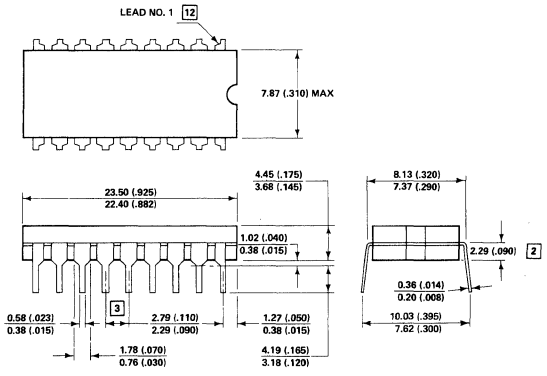
CONSTRUCTION NOTES: 9c, 10d, 11c

FJ Package



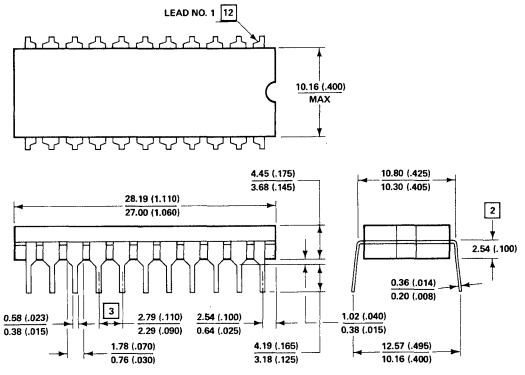
CONSTRUCTION NOTES: 9c, 10d, 11c

FK Package



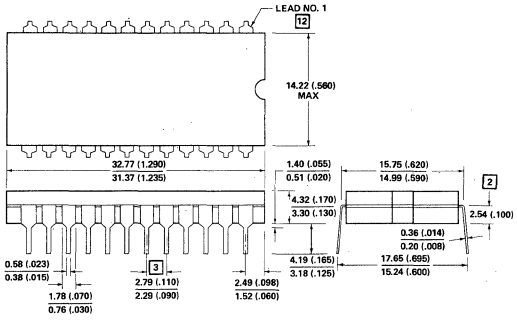
CONSTRUCTION NOTES: 9c, 10d, 11c

FM Package



CONSTRUCTION NOTES: 9c, 10d, 11c

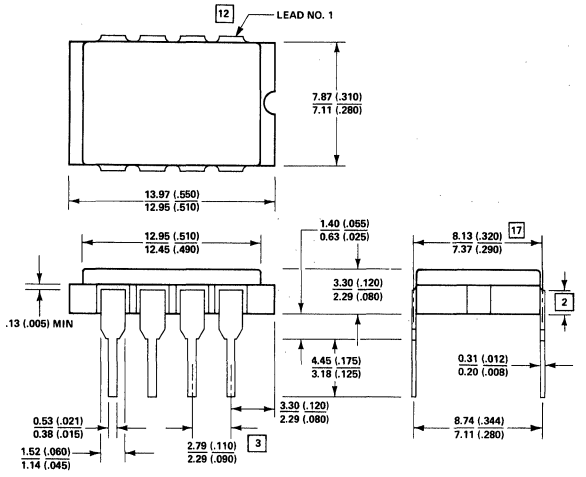
FN Package



CONSTRUCTION NOTES: 9c, 10d, 11c

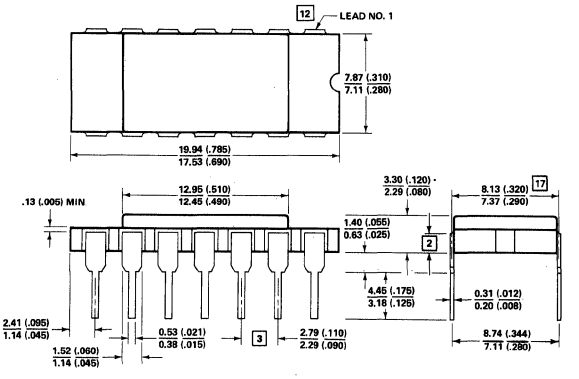
HERMETIC: Laminated Ceramic, Side Brazed Lead

IEA Package



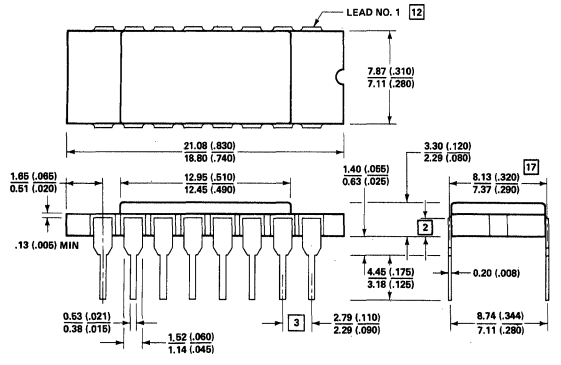
CONSTRUCTION NOTES: 9e, 10f, 11c

IHA Package



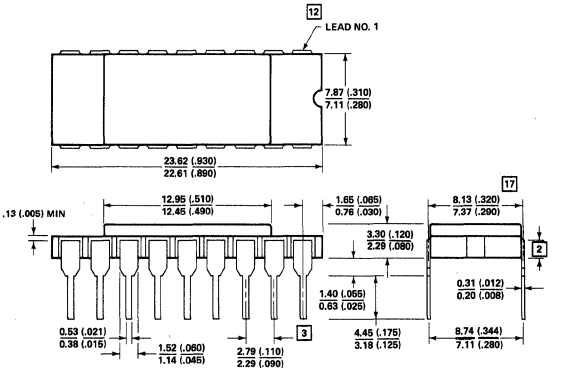
CONSTRUCTION NOTES: 9e, 10f, 11c

IJA Package



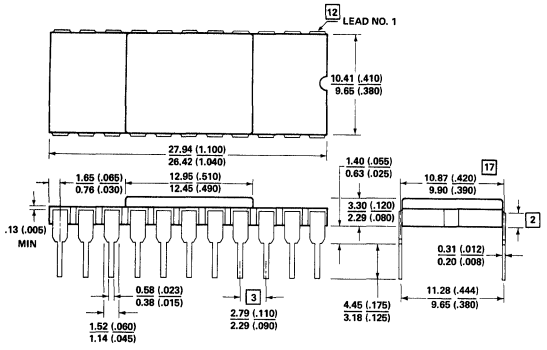
CONSTRUCTION NOTES: 9e, 10f, 11c

IKA Package



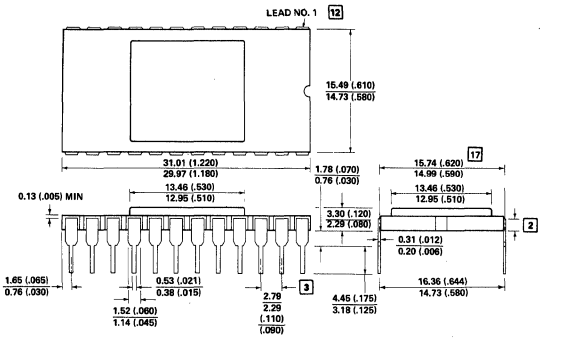
CONSTRUCTION NOTES: 9e, 10f, 11c

IMA Package



CONSTRUCTION NOTES: 9e, 10f, 11c

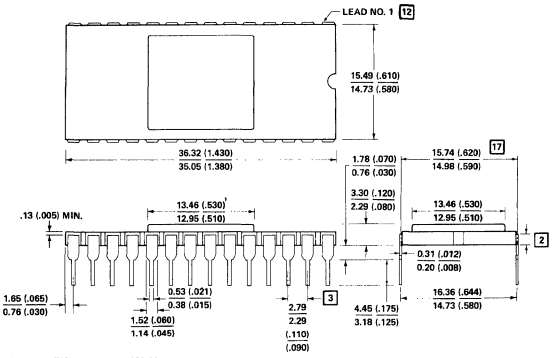
INC Package and IND Package



CONSTRUCTION NOTES: 9e, 10f, 11c, 11f (IND)

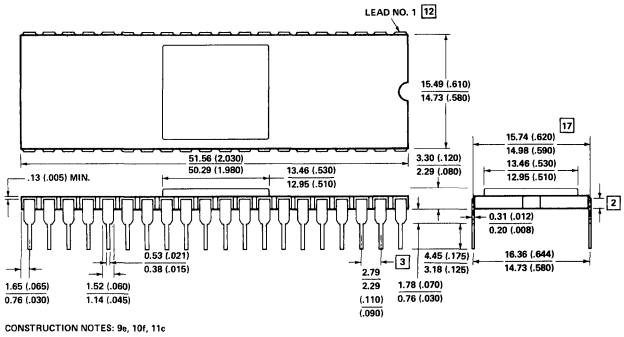
HERMETIC: Laminated Ceramic, Side Brazed Lead (cont'd.)

IQA Package



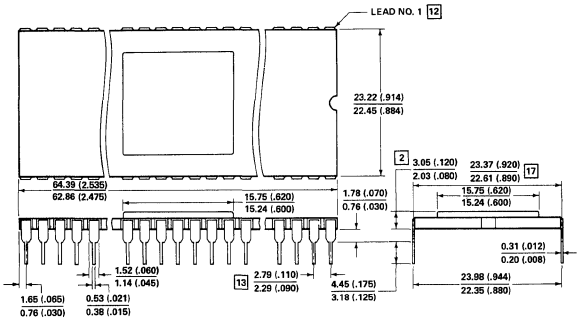
CONSTRUCTION NOTES: 9e, 10f, 11c

IWA Package



CONSTRUCTION NOTES: 9e, 10f, 11c

IZA Package



CONSTRUCTION NOTES: 9e, 10f, 11c

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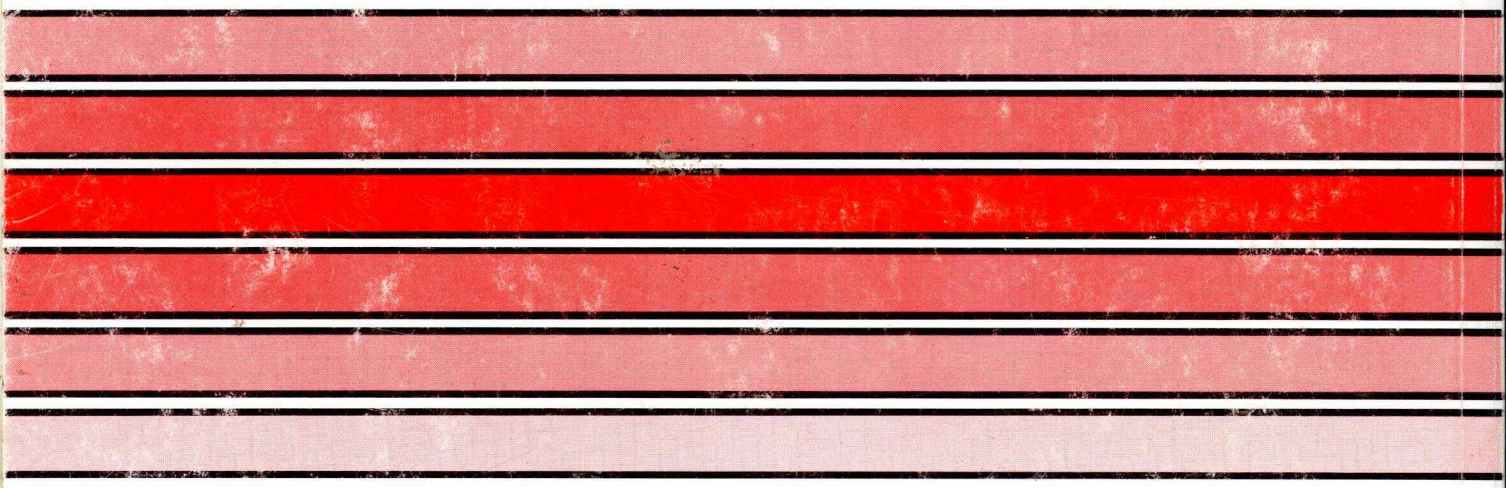

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