SILICON GENERAL

Silicon General Semiconductors

Product Catalog

1990/1991

Product Catalog

SILICON GENERAL

Solutions for Data Conversion and Power Management

THE SILICON GENERAL COMMITMENT

Silicon General Semiconductors has been recognized for many years as a leading supplier of linear power management IC's, providing proprietary semiconductors for regulators, pulse width modulators, servo and other drivers, read/write circuitry, and operational amplifiers. Our roots in power IC technology have led us naturally into the interface area, and CMOS now plays an important role in our product strategy, along with our historically recognized bipolar capability. Our CMOS products, while not represented in this catalog, serve a variety of interface applications and are available on a custom basis.

Silicon General believes a focused product and marketing strategy is best for our chosen marketing base, as well as our customers. We concentrate our resources on serving applications in the Military, Radiation Hard, Industrial Power Supplies, Computer Storage, and Automotive markets. This focused strategy has allowed us to become the leading supplier to our customers in some of these areas, and we continue to increase our penetration in the others.

Silicon General has been certified by DESC to manufacture microcircuits in conformance with MIL-M-38510, Class B. Certification has also been extended to manufacture devices to MIL-S-19500, JAN, JANTX, and JANTXV. Several devices have been qualified with a growing list of QPL items planned in the future. Many OEM customers have approved Silicon General to manufacture and process devices to their demanding Class S requirements.

We are committed to providing quality products to our customers, on schedule. All our products, whether industrial or military, are processed in the same qualified bipolar fabrication facility. Fab equipment includes the use of projection aligners, dry etch equipment, and ion implantation. Statistical process control is in place and used in daily operations.

Silicon General's offshore and US assembly capability, in combination with one of the broadest package offerings in the industry, provides further flexibility in satisfying the needs of our customers.

We are also committed to providing better technical solutions to your applications problems, and particularly endeavor to provide custom capability wherever practical. Design, product, and applications engineering teams are available in more than one geographical area.

Silicon General supplies the leaders in each of our chosen market areas, and we pride ourselves in this regard. We are a team dedicated to meeting our commitments, and we are a company who values partnership relations with its customers.

We thank you for considering Silicon General as a supplier to your company.

Signed,

Charles C. Thompson
President

PRODUCT STATUS DEFINITIONS

The following definitions are used in this catalog to describe the current product production status. Silicon General reserves the right to make changes without further notice to any product to improve reliability, function or design.

Future Product Release -
Product is either currently under design or in the conceptual stage, and characteristics are for information only.

Advanced Data Sheet -
Product design has been completed and parameters are under evaluation. Data described are design goals, and final device specifications are subject to change.

(No Definition Noted) -
Product is in full production.

IDENTIFICATION OF OFF-SHORE ASSEMBLY LOCATIONS

Silicon General utilizes several off-shore locations to perform assembly and environmental screening operations. This assembly site is identified on the device or unit packaging label according to the following codes:

Country	Preferred Abbreviations	Limited Space Abbreviations
Korea	KOR	A
Philippines	PHIL	S or T
Thailand	THAI	B
U.S.A.	USA	G

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SILICON GENERAL

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LINEAR INTEGRATED CIRCUITS

CHERRY

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CH1526	SG1526
CS365	SG3172
CS1524	SG1524
CS1524A	SG1524B
CS1525A	SG1525A
CS1527A	SG1527A
CS1842	SG1842
CS1843	SG1843
CS2524	SG2524
CS2525A	SG2525A
CS2526	SG2526
CS2527A	SG2527A
CS3717A	SG3718

LINEAR TECH

P/N	SG REPLACE
LM101A	SG101A
LM107	SG107
LM111	SG111
LM117	SG117
LM117A	SG117A
LM123	SG123
LM137	SG137
LM138	SG138
LM150	SG150
LM301A	SG301A
LM307A	SG307
LM311	SG311
LM317	SG317
LM317A	SG317A
LM323	SG323
LM337	SG337
LM338	SG338
LM350	SG350
LT123A	SG123A
LT137A	SG137A
LT138A	SG138A
LT150A	SG150A
LT1524	SG1524
LT1525A	SG1525A
LT1526	SG1526
LT1527A	SG1527A
LT1842	SG1842
LT1843	SG1843
LT2524	SG2524
LT2524A	SG2524B
LT2526	SG2526
LT323A	SG323A
LT337A	SG337A
LT338A	SG338A
LT350A	SG350A
LT3524	SG3524
LT3525A	SG3525A
LT3526	SG3526
LT3527A	SG3527A
SG1524	SG1524
SG1525A	SG1525A
SG1527A	SG1527A
SG2524	SG2524
SG3524	SG3524
SG3525A	SG3525A
SG3527A	SG3527A
UC1846	SG1846
UC1847	SG1847
UC3846	SG3846
UC3847	SG3847

MOTOROLA

P/N	SG REPLACE
LM101A	SG101A
LM109	SG109
LM111	SG111
LM117	SG117
LM123	SG123
LM124	SG124
LM137	SG137
LM140-12	SG140-12
LM140-15	SG140-15
LM140-18	SG140-18
LM140-24	SG140-24
LM150	SG150
LM201	SG201
LM201A	SG201A
LM204	SG204
LM205	SG205
LM208	SG209
LM211	SG211
LM217	SG217
LM223	SG223
LM224	SG224
LM237	SG237
LM250	SG250
LM301A	SG301A
LM305	SG305
LM309	SG309
LM311	SG311
LM317	SG317
LM323	SG323
LM337	SG337
LM340-05	SG340-05
LM340-12	SG340-12
LM340-15	SG340-15
LM340-18	SG340-18
LM340-20	SG340-20
LM340-24	SG340-24
LM350	SG350
LM350-08	SG340-08
MAD1103C	SG5772J
MAD1103F	SG5772F
MAD1103P	SG5772N
MAD1104C	SG5774J
MAD1104F	SG5774F
MAD1104P	SG5774N
MAD1108C	SG6101J
MAD1108F	SG6101F
MAD1108P	SG6101N
MC1403	SG3503
MC1411	SG2001
MC1412	SG2002
MC1413	SG2003
MC1416	SG2004
MC1436	SG1436
MC1468	SG1468
MC1489A	SG1489A
MC1495	SG1495
MC1496	SG1496
MC1503	SG1503
MC1536	SG1536
MC1568	SG1568
MC1595	SG1595
MC1596	SG1596
MC1723	SG723
MC1741	SG741
MC1741S	SG741C
MC1748	SG201
MC7805	SG7805
MC7805A	SG7805A
MC7805AC	SG7805AC
MC7805C	SG7805C
MC7806	SG7806
MC7806A	SG7806A
MC7806AC	SG7806AC
MC7806C	SG7806C
MC7808	SG7808
MC7808A	SG7808A
MC7808C	SG7808C
MC7812	SG7812
MC7812A	SG7812A
MC7812AC	SG7812AC
MC7812C	SG7812C
MC7815	SG7815
MC7815A	SG7815A
MC7815AC	SG7815AC
MC7815C	SG7815C
MC7820	SG7820
MC7820A	SG7820A
MC7820AC	SG7820AC
MC7820C	SG7820C
MC7824	SG7824
MC7824A	SG7824A
MC7824AC	SG7824AC
MC7824C	SG7824C
MC7905	SG7905
MC7905A	SG7905A
MC7905AC	SG7905AC
MC7905C	SG7905C
MC7905.2	SG7905.2
MC7905.2A	SG7905.2A
MC7905.2AC	SG7905.2AC
MC7905.2C	SG7905.2C
MC7908	SG7908
MC7908A	SG7908A
MC7908AC	SG7908AC
MC7908C	SG7908C
MC7912	SG7912
MC7912A	SG7912A
MC7912AC	SG7912AC
MC7912C	SG7912C
MC7915	SG7915
MC7915A	SG7915A
MC7915AC	SG7915AC
MC7915C	SG7915C
MC7918	SG7918
MC7918A	SG7918A
MC7918AC	SG7918AC
MC7918C	SG7918C
MC7920	SG7920
MC7920A	SG7920A
MC7920AC	SG7920AC
MC7920C	SG7920C
SG1525A	SG1525A
SG1526	SG1526
SG1527A	SG1527A
SG2525A	SG2525A
SG2526	SG2526
SG2527A	SG2527A
SG3525A	SG3525A
SG3526	SG3526
ULN2003	SG2003C
ULN2004	SG2004C
ULN2064	SG2064
ULN2065	SG2065
ULN2066	SG2066
ULN2067	SG2067
ULN2068	SG2068
ULN2069	SG2069
ULN2074	SG2074

NATIONAL

P/N	SG REPLACE
DS55325	SG55325
DS55451	SG55451
DS55452	SG55452
DS55453	SG55453
DS55454	SG55454
DS55461	SG55461
DS55462	SG55462
DS55463	SG55463
DS55464	SG55464
DS55470	SG55470
DS55471	SG55471
FSA1410M	SG5770T
FSA1411M	SG5768T
FSA2002M	SG5768F
FSA2003M	SG5770F
FSA2500M	SG5772F
FSA2501M	SG5772J
FSA2501P	SG5772N
FSA2503M	SG5774J
FSA2503P	SG5774N
FSA2504M	SG5774F
FSA2509M	SG5774AJ
FSA2509P	SG5774AN
FSA2510M	SG5772AJ
FSA2510P	SG5772AN
FSA2563M	SG5768AJ
FSA2563P	SG5768AN
FSA2564M	SG5770AJ
FSA2564P	SG5770AN
FSA2565M	SG25768J
FSA2566M	SG25770J
FSA2619M	SG6101AJ
FSA2619P	SG6101AN
FSA2620M	SG6100AJ
FSA2620P	SG6100AN
FSA2621M	SG6100AF
FSA2719M	SG6101J
FSA2719P	SG6101N
FSA2720M	SG6100J
FSA2720P	SG6100N
FSA2721M	SG6100F
LM103-1.8	SG103-1.8
LM103-2.7	SG103-2.7
LM103-4.8	SG103-4.8
LM104A	SG104
LM105A	SG105
LM109	SG109
LM117	SG117
LM120-05	SG120-05
LM120-08	SG120-08
LM120-12	SG120-12
LM120-15	SG120-15
LM120-18	SG120-18
LM120-20	SG120-20
LM120-5.2	SG120-5.2
LM123	SG123
LM137	SG137
LM138	SG138
LM140-05	SG140-05
LM140-06	SG140-06
LM140-08	SG140-08
LM140-12	SG140-12
LM140-15	SG140-15
LM140-18	SG140-18
LM140-20	SG140-20
LM143	SG143
LM150	SG150
LM1524	SG1524
LM204	SG204
LM205	SG205
LM207	SG207
LM209	SG209
LM217	SG217
LM220-05	SG220-05
LM220-08	SG220-08
LM220-12	SG220-12
LM220-15	SG220-15
LM220-5.2	SG220-5.2
LM237	SG237
LM238	SG238
LM238A	SG238A
LM240-05	SG240-05
LM240-06	SG240-06
LM240-08	SG240-08
LM240-12	SG240-12
LM240-15	SG240-15
LM240-18	SG240-18
LM250	SG250
LM250A	SG250A
LM2524	SG2524
LM304	SG304
LM305	SG305
LM305A	SG305A
LM309	SG309
LM317	SG317
LM320-05	SG320-05
LM320-08	SG320-08
LM320-12	SG320-12
LM320-15	SG320-15
LM320-18	SG320-18
LM320-20	SG320-20
LM320-5.2	SG320-5.2
LM323	SG323
LM337	SG337
LM338	SG338
LM340-05	SG340-05
LM340-08	SG340-08
LM340-12	SG340-12
LM340-15	SG340-15
LM340-18	SG340-18
LM340-20	SG340-20
LM343	SG343
LM350	SG350
LM3524	SG3524
LM723	SG723
LM723C	SG723C
LM2935	SG29055
LM2985	SG29085
MAD1105	SG5768
MAD1106	SG5770
MAD1107	SG5774
MAD1109	SG6100
UA101A	SG101A
UA105	SG105
UA109	SG109
UA111	SG111
UA117	SG117
UA124	SG124
UA1489	SG1468
UA1489A	SG1489A
UA1524	SG1524
UA201	SG201
UA209	SG209
UA224	SG224
UA238	SG238
UA2524	SG2524
UA301A	SG301A
UA305	SG305
UA305A	SG305A
UA3086	SG3821
UA309	SG309
UA311	SG311
UA317	SG317
UA324	SG324
UA338	SG338
UA350	SG350
UA3524	SG3524
UA55450	SG55450B
UA55452	SG55452B
UA55462	SG55462
UA75450	SG75450B
UA75451	SG75451B
UA75452	SG75452B
UA75453	SG75453B
UA75461	SG75461
UA75462	SG75462
UA7805-C	SG7805C
UA7805-C2	SG7805AC
UA7805-M	SG7805
UA7806-C	SG7806C
UA7806-C2	SG7806AC
UA7806-M	SG7806
UA7808-C	SG7808C
UA7808-C2	SG7808AC
UA7808-M	SG7808
UA7812-C	SG7812C
UA7812-C2	SG7812AC
UA7812-M	SG7812
UA7815-C	SG7815C
UA7815-C2	SG7815AC
UA7815-M	SG7815
UA7820-C	SG7820C
UA7820-C2	SG7820AC
UA7820-M	SG7820
UA7824-C	SG7824C
UA7824-C2	SG7824AC
UA7824-M	SG7824
UA7905-C	SG7905C
UA7905-M	SG7905

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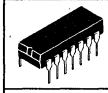
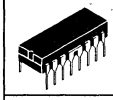
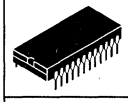
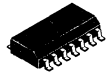
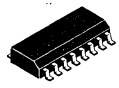
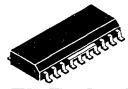
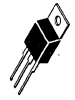
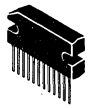
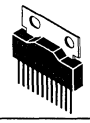
P/N	SG REPLACE
NATIONAL	
UA7908-C	SG7908C
UA7908-M	SG7908
UA7912-C	SG7912C
UA7912-M	SG7912
UA7915-C	SG7915C
UA7915-M	SG7915
UA796	SG1596
UA9665	SG2001
UA9666	SG2002
UA9667	SG2003
1N5768	1N5768
1N5770	1N5770
1N5772	1N5772
SGS	
L165	SG3173
L201	SG2021C
L202	SG2022C
L203	SG2023C
L204	SG2024C
L272	SG3272
L601	SG2821
L602	SG2822
L603	SG2823
L604	SG2824
L2722	SG3272
L2726	SG3272
L7805	SG7805
L7805C	SG7805C
L7806	SG7806
L7806C	SG7806C
L7808	SG7808
L7808A	SG7808C
L7812	SG7812
L7812C	SG7812C
L7815	SG7815
L7815C	SG7815C
L7820	SG7820
L7820C	SG7820C
L7824	SG7824
L7824C	SG7824C
L7905	SG7905
L7905C	SG7905C
L7905.2	SG7905.2
L7905.2C	SG7905.2C
L7908	SG7908
L7908C	SG7908C
L7912	SG7912
L7912C	SG7912C
L7915	SG7915
L7915C	SG7915C
L7918	SG7918
L7918C	SG7918C
L7920	SG7920
L7920C	SG7920C
LM123	SG123
LM217	SG217
LM223	SG223
LM317	SG317
LM323	SG323
LM324	SG324
LM324A	SG324A
LM723	SG723
LM741	SG741
LM741C	SG741C
LS101A	SG101A
LS204	SG204
ULN2001A	SG2001C
ULN2002A	SG2002C
ULN2003A	SG2003C
ULN2004A	SG2004C
ULN2064B	SG2064
ULN2065B	SG2065
ULN2066B	SG2066
ULN2067B	SG2067
ULN2068B	SG2068
ULN2069B	SG2069
ULN2070B	SG2070
ULN2071B	SG2071
ULN2074B	SG2074
ULN2075B	SG2075
ULN2076B	SG2076
ULN2077B	SG2077
ULN2801A	SG2801
ULN2802A	SG2802
ULN2803A	SG2803
ULN2804A	SG2804
SPRAGUE	
UDN2935	SG3635
ULN2001	SG2001C
ULN2002	SG2002C
ULN2003	SG2003C
ULN2004	SG2004C
ULN2011	SG2011C
ULN2012	SG2012C
ULN2013	SG2013C
ULN2014	SG2014C
ULN2021	SG2021C
ULN2022	SG2022C
ULN2023	SG2023C
ULN2024	SG2024C
ULN2045	SG3821
ULN2064	SG2064
ULN2065	SG2065
ULN2066	SG2066
ULN2067	SG2067
ULN2068	SG2068
ULN2069	SG2069
ULN2070	SG2070
ULN2071	SG2071
ULN2074	SG2074
ULN2075	SG2075
ULN2076	SG2076
ULN2077	SG2077
ULN3751	SG3173
ULN8124	SG3524
ULN8125A	SG3525A
ULN8126	SG3526
ULN8127A	SG3527A
ULQ8124	SG2524
ULQ8125A	SG2525A
ULQ8126	SG2526
ULQ8127A	SG2527A
ULS2001	SG2001
ULS2002	SG2002
ULS2003	SG2003
ULS2004	SG2004
ULS2011	SG2011
ULS2012	SG2012
ULS2013	SG2013
ULS2014	SG2014
ULS2021	SG2021
ULS2022	SG2022
ULS2023	SG2023
ULS2024	SG2024
ULS2801	SG2801A
ULS2802	SG2802A
ULS2803	SG2803A
ULS2803	SG2813A
ULS2804	SG2804A
ULS2811	SG2811A
ULS2812	SG2812A
ULS2814	SG2814A
ULS2821	SG2821A
ULS2822	SG2822A
ULS2823	SG2823A
ULS2824	SG2824A
ULS8124	SG1524
ULS8125A	SG1525A
ULS8126H	SG1526
ULS8127A	SG1527A
TEXAS INSTRUMENTS	
TL040	SG040
LM101A	SG101A
LM107	SG107
LM111	SG111
LM137	SG137
LM207	SG207
LM211	SG211
LM217	SG217
LM237	SG237
SG1524	SG1524
SG2524	SG2524
SN55189	SG1468
SN55189A	SG1489A
SN75064	SG2064
SN75065	SG2065
SN75066	SG2066
SN75067	SG2067
SN75068	SG2068
SN75069	SG2069
SN75074	SG2074
SN75075	SG2075
SN75188	SG75188
SN75189	SG1468
SN75189A	SG1489A
SN75234	SG75234
SN7524	SG7524
SN75325	SG75325
SN75326	SG75326
SN75327	SG75327
SN75430	SG75430
SN75431	SG75431
SN75432	SG75432
SN75433	SG75433
SN75434	SG75434
SN75450B	SG75450B
SN75451B	SG75451B
SN75452B	SG75452B
SN75453B	SG75453B
SN75454B	SG75454B
SN75460	SG75460
SN75461	SG75461
SN75462	SG75462
SN75463	SG75463
SN75464	SG75464
SN75470	SG75470
SN75471	SG75471
SN75472	SG75472
SN75473	SG75473
SN75474	SG75474
SNJ55188	SG1488
SNJ55189	SG1489
SNJ55189A	SG1489A
SNJ55234	SG55234
SNJ55234	SG55234A
SNJ55236	SG55236
SNJ55236	SG55236A
SNJ5524	SG5524
SNJ55325	SG55325
SNJ55326	SG55326
SNJ5534	SG5534
SNJ55450B	SG55450B
SNJ55451B	SG55451B
SNJ55452B	SG55452B
SNJ55453B	SG55453B
SNJ55454B	SG55454B
SNJ55460	SG55460
SNJ55461	SG55461
SNJ55462	SG55462
SNJ55463	SG55463
SNJ55464	SG55464
SNJ55470	SG55470
SNJ55471	SG55471
SNJ55472	SG55472
SNJ55473	SG55473
SNJ55474	SG55474
TL111	SG111
TL117	SG117
TL1525A	SG1525A
TL1527A	SG1527A
TL2525A	SG2525A
TL2527A	SG2527A
UNITRODE	
PIC600	SM600
PIC601	SM601
PIC602	SM602
PIC610	SM610
PIC611	SM611
PIC612	SM612
PIC625	SM625
PIC626	SM626
PIC627	SM627
PIC635	SM635
PIC636	SM636
PIC637	SM637
PIC645	SM645
PIC646	SM646
PIC647	SM647
PIC655	SM655
PIC656	SM656
PIC657	SM657
PIC7501	SM600B
PIC7502	SM601B
PIC7503	SM602B
PIC7504	SM610B
PIC7505	SM611B
PIC7506	SM612B
PIC7507	SM625B
PIC7508	SM626B
PIC7509	SM627B
PIC7510	SM635B
PIC7511	SM636B
PIC7512	SM637B
PIC7513	SM645B
PIC7514	SM646B
PIC7515	SM647B
PIC7516	SM655B
PIC7517	SM656B
PIC7518	SM657B
PIC7519	SM600A
PIC7520	SM601A
PIC7521	SM602A
PIC7522	SM610A
PIC7523	SM611A
PIC7524	SM612A
PIC7525	SM625A
PIC7526	SM626A
PIC7527	SM627A
PIC7528	SM635A
PIC7529	SM636A
PIC7530	SM637A
PIC7531	SM645A
PIC7532	SM646A
PIC7533	SM647A
PIC7534	SM655A
PIC7535	SM656A
PIC7535	SM657A
UC117	SG117
UC120-05	SG120-05
UC120-12	SG120-12
UC120-15	SG120-15
UC137	SG137
UC140-05	SG140-05
UC140-12	SG140-12
UC140-15	SG140-15
UC150	SG150
UC1524	SG1524
UC1524A	SG1524B
UC1525A	SG1525A
UC1526	SG1526
UC1526A	SG1526B
UC1527A	SG1527A
UC1543	SG1543
UC1825	SG1825
UC1544	SG1544
UC1840	SG1840
UC1842	SG1842
UC1843	SG1843
UC1844	SG1844
UC1845	SG1845
UC1846	SG1846
UC1847	SG1847
UC217	SG217
UC237	SG237
UC250	SG250
UC2524	SG2524
UC2524A	SG2524B
UC2525A	SG2525A
UC2526	SG2526
UC2526A	SG2526B
UC2527A	SG2527A
UC2540	SG2540
UC2543	SG2543
UC2544	SG2544
UC2825	SG2825
UC2840	SG2840
UC2842	SG2842
UC2843	SG2843
UC2844	SG2844
UC2845	SG3845
UC2846	SG2846
UC2847	SG2847
UC317	SG317
UC320-05	SG320-05
UC320-12	SG320-12
UC320-15	SG320-15
UC337	SG337
UC340-05	SG340-05
UC340-12	SG340-12
UC340-15	SG340-15
UC350	SG350
UC3524	SG3524
UC3525A	SG3525A
UC3526	SG3526
UC3526A	SG3526B
UC3527A	SG3527A
UC3543	SG3543
UC3544	SG3544
UC3717	SG3718
UC3825	SG3825
UC3840	SG3840
UC3842	SG3842
UC3843	SG3843
UC3844	SG3844
UC3845	SG3845
UC3846	SG3846
UC3847	SG3847
UC7805	SG7805
UC7805A	SG7805A
UC7805AC	SG7805AC
UC7805C	SG7805C
UC7812	SG7812
UC7812A	SG7812A
UC7812AC	SG7812AC
UC7812C	SG7812C
UC7815	SG7815
UC7815A	SG7815A
UC7815AC	SG7815AC
UC7815C	SG7815C
UC7905	SG7905
UC7905A	SG7905A
UC7905AC	SG7905AC
UC7905C	SG7905C
UC7912	SG7912
UC7912A	SG7912A
UC7912AC	SG7912AC
UC7912C	SG7912C
UC7915	SG7915
UC7915A	SG7915A
UC7915AC	SG7915AC
UC7915C	SG7915C

SILICON GENERAL

INDUSTRY PACKAGE CROSS-REFERENCE

		Silicon General	Cherry	Linear Tech	Motorola	NSC	Signetics	Sprague	Texas Instruments	Unitrode
PLASTIC DUAL-IN-LINE (DIP)										
	8 - Pin	M	N	N8	P1		N	M	P	N
	14, 16, 18, 20, 22, & 24 - Pin	N	N	N	P2		N	A	N	N
	16 - Pin (Batwing)	W						B		
	24 & 28 - Pin (Wide)	N					N	A	NF	N
PLASTIC SMALL OUTLINE (S.O.I.C.)										
	8 - Pin	DM		S	D	M	D	L	D	
	14 & 16 - Pin	D		S	D	M	D	L	D	D
	16, 18, & 20 - Pin	DW		S	D	WN	DW	LW		D
	20 - Pin (Batwing)	DWW						LB		
PLASTIC (POWER)										
	3 & 5 - Pin (TO-220)	P		T	T	T	U	Z	KC	T
	3 - Pin (TO-247)	V		P						
	12 - Pin (SIP)	S								
	12 - Pin (SIP)	ST						W		

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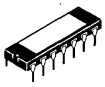
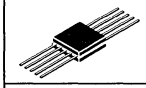
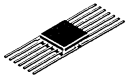
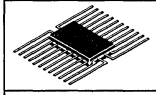
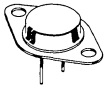
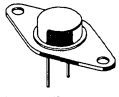
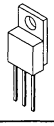
INDUSTRY PACKAGE CROSS-REFERENCE

	Silicon General	Cherry	Linear Tech	Motorola	NSC	Signetics	Sprague	Texas Instruments	Unitrode
PLASTIC LEADED CHIP CARRIER									
 20 & 28 - Pin (PLCC)	Q				V		EP	FN	Q
CERAMIC DUAL-IN-LINE									
 8 - Pin	Y	J	J8	U	J	FE		JG	J
 14, 16 (TO-116), & 18 - Pin	J	J	J	L	J	F	R	J	J
CERAMIC SIDE BRAZED (DIP)									
 14, 16, & 18 - Pin	H		D	L	D		H	JD	
CERAMIC FLAT PACK (CERPAC)									
 10, 16, & 20 - Pin	F		J		F			U, W	
 14 - Pin	F				F			W	
 24 - Pin	F				F			W	
CERAMIC LEADLESS CHIP CARRIER									
 20 - Pin (LCC)	L		L		E	G	EK	FK	L
METAL CANS									
 3 (TO-39), 8 (TO-99), 10 (TO-96, TO-100), & 12 (TO-101) - Pin	T		H	G, H	H	H			H
 3 - Pin (TO-3)	K		K	K	K		V		K
 3, 5, & 9 - Pin (TO-66)	R			R					
HERMETIC TO-257									
 3 - Pin	G, IG								

PRODUCT IDENTIFICATION

LINEAR INTEGRATED CIRCUITS

XX	XXXXX	XX	XXX	XXXXX	
SG	55325		J	883B	- Example
SG	7805	AC	R		- Example
SM	645		K		- Example

PRODUCT

SG - Linear Integrated Circuit
SM - Thick Film Hybrid (See next page)

GENERIC PART NUMBER

See data sheets or price sheet for individual descriptions and temperature ranges.

ELECTRICAL GRADES (optional)

A or B - Improved Performance
C - Commercial Temp Range

PROCESSING LEVEL (optional)

(SPS No.) - 4 or 5 digit in-house number for Spec. Control Drawings
883 - MIL-STD-883
Class B
Class S
JAN - MIL-M-38510 (Integrated Circuits)
SMD - Standardized Military Drawing (DESC)
JAN - MIL-S-19500 (Descrete Components)

PACKAGE OPTIONS

M - 8 PIN DIL Plastic
N - 14,16,18,20,22,24,28,40 PIN DIL Plastic
W - 16 PIN Batwing DIL Plastic
D - 14, 16, PIN DIL S.O.I.C. Plastic
DM - 8 PIN DIL S.O.I.C. Plastic
DW - 16, 18, 20 PIN DIL S.O.I.C. Plastic (wide body)
DWW - 20 PIN Batwing DIL S.O.I.C. Plastic
P - 3, 5 PIN TO-220 Plastic
V - 3 PIN TO-247 SIP Plastic
S - 12 PIN SIP Plastic
ST - 12 PIN SIP Plastic (Metal Tab)
Q - 20, 28 PIN Leaded Chip Carrier - Plastic (PLCC)
Y - 8 PIN DIL Ceramic
J - 14, 16, 18 PIN DIL Ceramic
H - 14, 16, 18 PIN DIL Ceramic Side Brazed
F - 10, 14, 16, 20, 24 PIN DIL Ceramic (CERPAC)
L - 20 PIN Leadless Chip Carrier - Ceramic (LCC)
Z - 2 PIN TO-46 Metal Can
Z - 3 PIN TO-52 Metal Can
T - 3, 8, 10, 12 PIN TO-5 Metal Can
K - 3, 4 PIN TO-3 Metal Can
R - 3, 4, 5, 9 PIN TO-66 Metal Can
G - 3, 5 PIN TO-257 (non-isolated hermetic TO-220)
IG - 3, 5 PIN TO-257 (isolated hermetic TO-220)

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PRODUCT IDENTIFICATION

POWER HYBRID CIRCUITS

SM	XXX	XX	X	X	XXXXX	
SM	600			R		- Example
SM	625	HR		R		- Example
SM	645	HR	1	K	12345	- Example

PRODUCT

SM - Thick Film Hybrid

GENERIC PART NUMBER

See data sheets or price sheet for individual descriptions and temperature ranges.

SPECIAL SCREENING

4 or 5 digit in - house number for Spec. Control Drawings.

PACKAGE DESIGNATOR

R - Metal Can TO-66
K - Metal Can TO-3

PARTICLE CONTROL
(Available only with HR construction)

(blank) - Standard
1 - PIND Test
2 - Conformal Coating

CONSTRUCTION / SCREENING

(blank) - Commercial construction, no burn-in
HR - High reliability construction, Burn-in HTRB 160 Hours

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From its beginning in 1969, Silicon General has been committed to excellence in the manufacture of Linear Integrated Circuits.

Over the years, innovative design and the dedication to high quality manufacturing principles has seen the product line expand in scope and grow in customer acceptance.

Silicon General is committed to the concept that the ultimate quality of a device is determined by the company's exacting design and manufactuing process controls. The Statistical Process Control program (SPC) at Silicon General is in effect and has a high management directive to continue to improve. Our dedication to a zero defects program, through process control, has largely been realized through the Total Quality Management concept currently in place.

We understand that satisfaction to the customer is achieved by delivering a high quality product on time. Silicon General assures this through close customer working relationships and a dedication to personal service.

QUALITY ASSURANCE MANAGER

SCREENING PROCEDURES FOR LINEAR INTEGRATED CIRCUITS

Silicon General manufactures hermetic products to the three standard levels of quality assurance processing outlined below. In addition, the company's unique flexibility allows ready accommodations to special customer requirements. The following Class S and Class B screening procedures are in compliance to MIL-M-38510 and all methods are as detailed in MIL-STD-883.

Screen	MIL-M-38510, Class S Method	Reqm't	MIL-M-38510, Class B Method	Reqm't	Standard Product Method	Reqm't
Wafer Lot Acceptance	5007	Sample	N/A		N/A	
Non-Destructive Bond Pull	2023	100%	N/A		N/A	
Internal Visual (Pre-Cap)	2010, Condition A	100%	2010, Condition B	100%	Commercial Visual	100%
Stabilization Bake	1008, Condition C 24 Hours @ 150°C	100%	1008, Condition C 24 Hours @ 150°C	100%	1008, Condition C 24 Hours @ 150°C	Optional
Temperature Cycling	1010, Condition C 10 Cycles, -65°C to +150°C	100%	1010, Condition C 10 Cycles, -65°C to +150°C	100%	1010, Condition C 10 Cycles, -65°C to +150°C	Optional
Constant Acceleration	2001, Applicable Condition per Package Type	100%	2001, Applicable Condition per Package Type	100%	2001, Applicable Condition per Package Type	Optional
Particle Impact Noise Detection (PIND)	2020, Condition A		N/A		N/A	
Hermeticity (Seal) a) Fine Leak b) Gross Leak	 1014, Condition B 5 x 10^{-8} atm-cc/sec 1014, Condition C1	 100% 100%	 1014, Condition B 5 x 10^{-8} atm-cc/sec 1014, Condition C1	 100% 100%	 1014, Condition B 5 x 10^{-8} atm-cc/sec 1014, Condition C1	 Sample Sample
Pre-Burn-in Electrical Test	Per Applicable Device Spec. Unit Serialization as required		Per Applicable Device Spec.		Per Applicable Device Spec.	
Burn-in Test	1015, Dynamic 240 Hours @ 125°C Minimum (Note: An additional 72 Hrs HTRB burn-in and interim electrical test as required)	100%	1015, Static or Dynamic 160 Hours @ 125°C Minimum or equivalent	100%	N/A	
Final Electrical Test a) DC @ 25°C b) DC @ Max. and Min. Rated Temp. c) Dynamic @25°C d) Functional @25°C	Per Applicable Device Spec.	 100% 100% 100% 100%	Per Applicable Device Spec.	 100% 100% 100% 100%	Per Applicable Device Spec.	 100% Sample 100% 100%
Hermeticity (Seal) a) Fine Leak b) Gross Leak	 1014, Condition B 5 x 10^{-8} atm-cc/sec 1014, Condition C1	 100% 100%	 N/A N/A		 N/A N/A	
Radiography	Method 2012	100%	N/A		N/A	
External Visual	Method 2009	100%	Method 2009	100%	Method 2009	100%
Quality Conformance Testing Group A Groups B, C (Class B only), D	5005 DC, AC Parameters 5005 Paragraph	 +25°C +125°C -55°C 3.5	5005 DC, AC Parameters 5005 Paragraph	 +25°C +125°C -55°C 3.5	DC, AC Parameters	+25°C

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SCREENING PROCEDURES FOR HIGH RELIABILITY POWER HYBRID CIRCUITS

Screen	Method - MIL-STD-883	Requirement	Comments
Internal Visual (Pre-Cap)	2017, Condition B	100%	
Conformal Coating	SG Internal Spec.	(optional)	Per Applicable Device Specification
Stabilization Bake	1008, Condition C 24 Hours @ 150°C	100%	
Temperature Cycling	1010, Condition C 10 Cycles, -65°C to +150°C	100%	
Constant Acceleration	2001, Condition B 20,000 g, Y_1 orientation (R - Pkg.) 5,000 g, Y_1 orientation (K - Pkg.)	100%	
Particle Impact Noise Detection (PIND)	2020, Condition B	(optional)	
Hermeticity (Seal) a) Fine Leak b) Gross Leak	 1014, Condition B 5 x 10^{-8} atm-cc/sec 1014, Condition C1	 100% 100%	
Functional Test		100%	Per Applicable Device Specification
Pre-Burn-in Electrical Test	Per Applicable Device Specification	100%	Unit Serialization as required
Burn-in Test	1015, Static Condition A (HTRB) 160 Hours	100%	Consult Factory for Other Screening Procedures
Final Electrical Test a) DC @ 25°C b) DC @ Max. and Min. Rated Temp. c) Dynamic @25°C d) Functional @25°C e) AC @ 25°C	Per Applicable Device Specification	 100% 100% 100% 100% 100%	
Hermeticity (Seal) a) Fine Leak b) Gross Leak	 1014, Condition B 5 x 10^{-8} atm-cc/sec 1014, Condition C1	 100% 100%	
External Visual	Method 2009	100%	
Quality Conformance Testing Group A Groups B, C, D	5008 DC, AC Parameters Sample Testing	 +25°C +125°C -55°C 	 Subgroups 1, 4, 7, 9 Subgroups 2, 8, 10 Subgroups 3, 8, 11

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JANTX & JANTXV SCREENING PROCEDURES FOR MIL-S-19500/474 DIODE ARRAYS

Screen	Method - MIL-STD-750	Requirement	Comments
Internal Visual (Pre-Cap)	MIL-STD-883 Method 2010 Cond. B	JANTXV only	Specified in MIL-S-19500/474
Stabilization Bake	1032 24 Hours @ 200°C	100%	
Temperature Cycling	1051 20 Cycles, -65°C to +175°C	100%	
Constant Acceleration	2006 20,000 g, Y_1 orientation	100%	
Hermeticity (Seal) a) Fine Leak b) Gross Leak	1071	 100% 100%	
Pre-Burn-in Electrical Test	Per Applicable Device Specification	100%	
Burn-in Test	1038 72 Hours @ 150°C	100%	As specified in MIL-S-19500/474
Final Electrical Test a) DC @ 25°C b) DC @ Max. and Min. Rated Temp. c) Delta Measurements	Per Applicable Device Specification	 100% 100% 100%	
Quality Conformance Testing Group A	External Visual DC, AC Parameters	 +25°C +150°C -55°C	Subgroup 1 Subgroups 2, 4, 6, 7 Subgroup 3 Subgroup 3
Groups B & C	Sample Testing		

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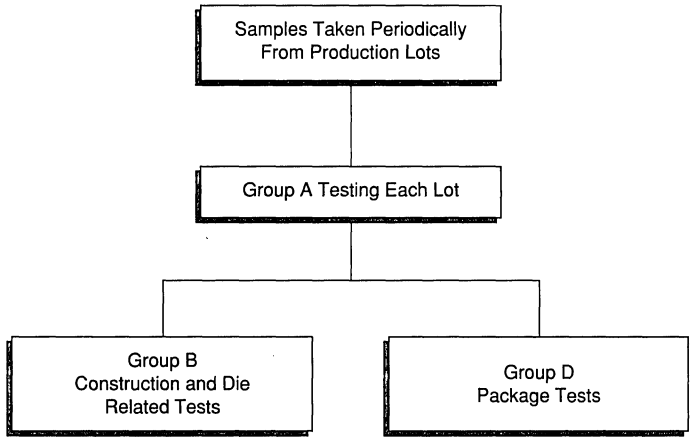
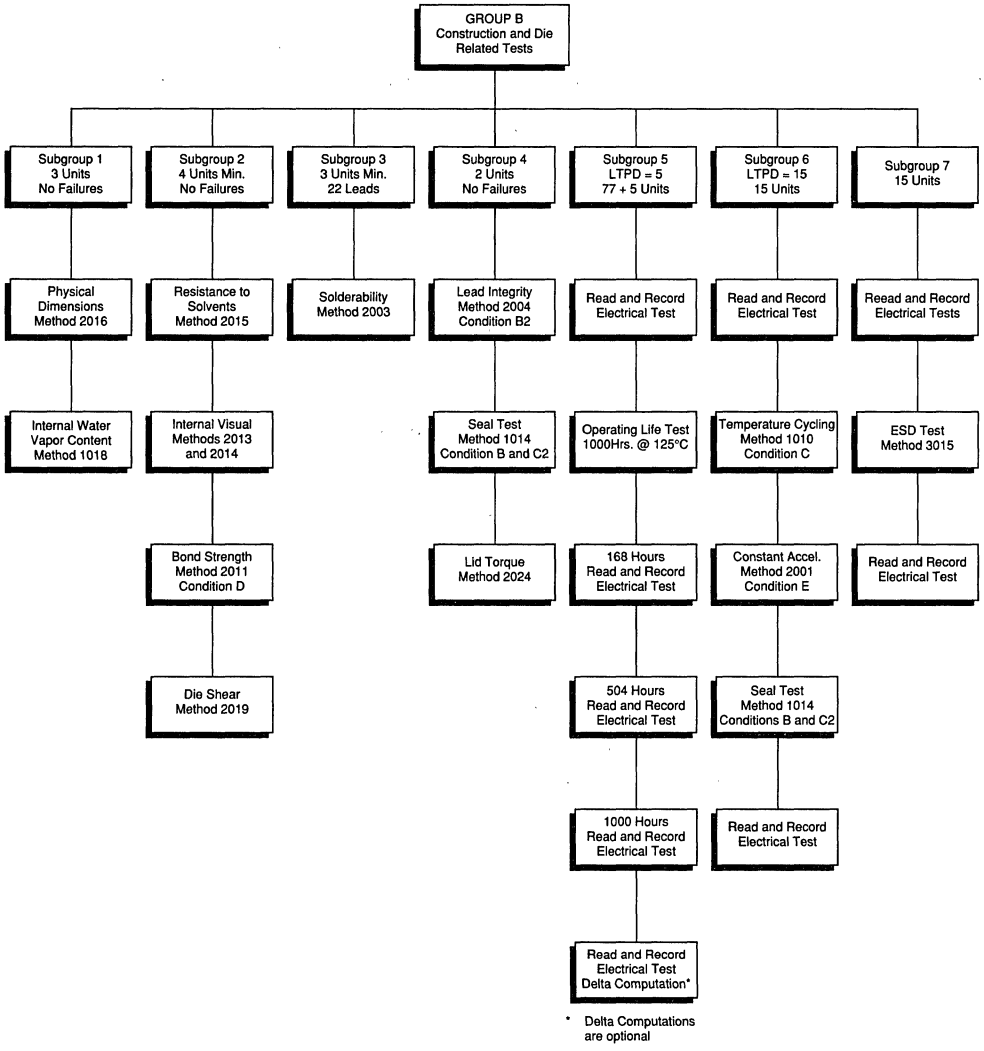
QUALITY CONFORMANCE INSPECTION (Q.C.I.)

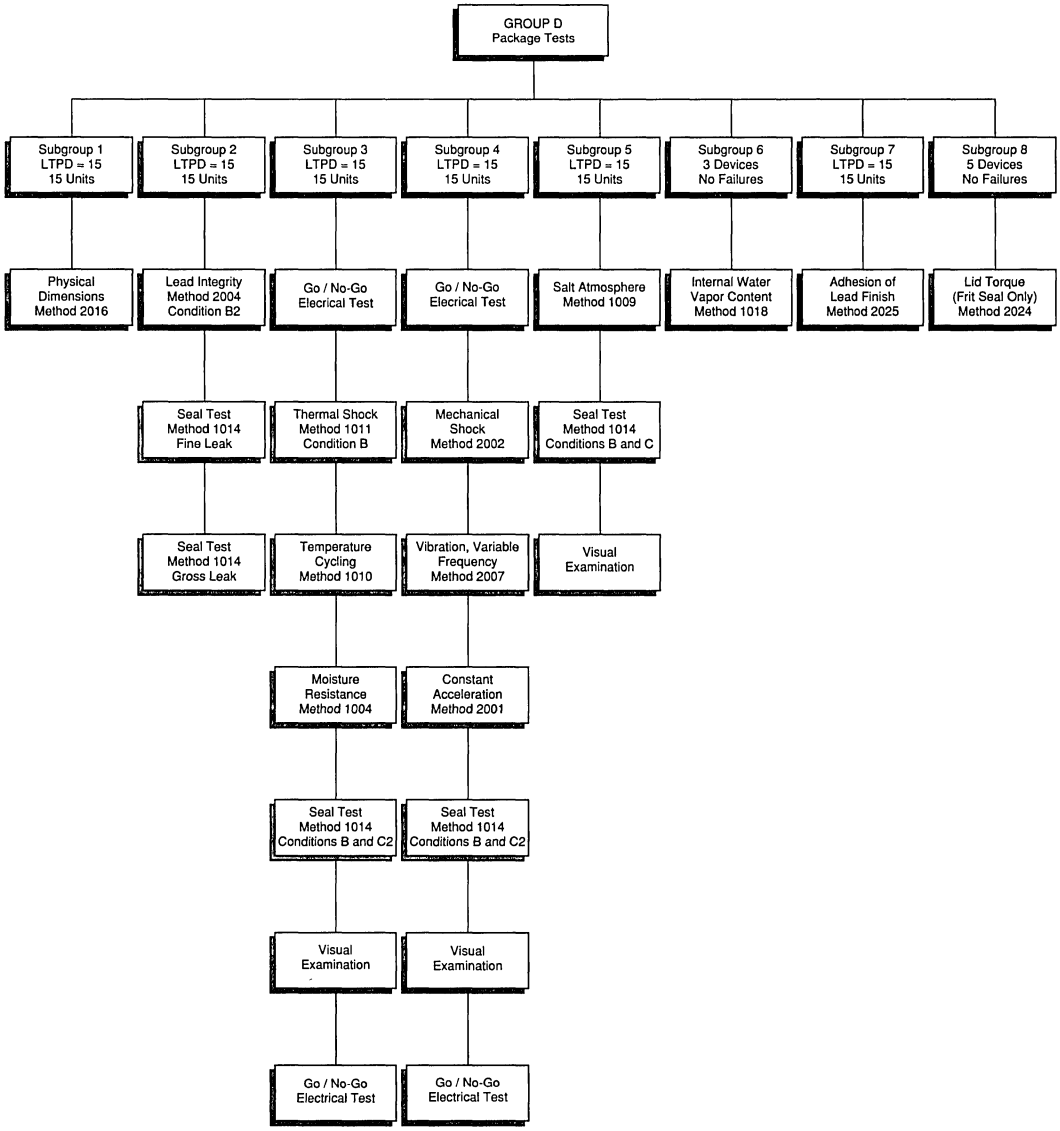
The following Group B and D tests are performed on a periodic basis or when specified by the customer. This testing is in compliance to MIL-M-38510 as detailed in MIL-STD-883, Method 5005.



Group B

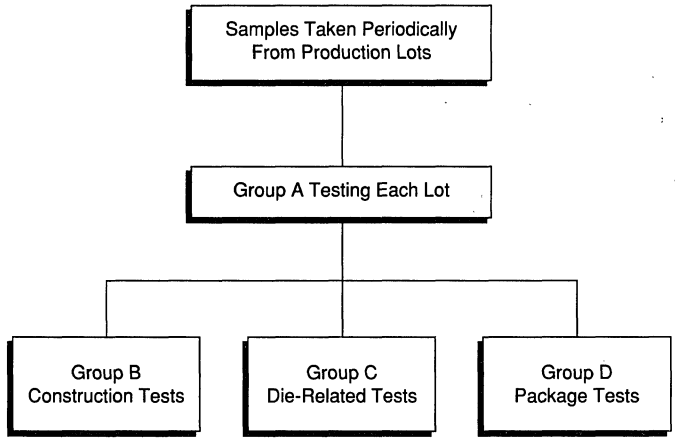

GROUP B
Construction and Die
Related Tests
Subgroup 1
3 Units
No Failures
Subgroup 2
4 Units Min.
No Failures
Subgroup 3
3 Units Min.
22 Leads
Subgroup 4
2 Units
No Failures
Subgroup 5
LTPD = 5
77 + 5 Units
Subgroup 6
LTPD = 15
15 Units
Subgroup 7
15 Units
Physical
Dimensions
Method 2016
Resistance to
Solvents
Method 2015
Solderability
Method 2003
Lead Integrity
Method 2004
Condition B2
Read and Record
Electrical Test
Read and Record
Electrical Test
Reead and Record
Electrical Tests
Internal Water
Vapor Content
Method 1018
Internal Visual
Methods 2013
and 2014
Seal Test
Method 1014
Condition B and C2
Operating Life Test
1000Hrs. @ 125°C
Temperature Cycling
Method 1010
Condition C
ESD Test
Method 3015
Bond Strength
Method 2011
Condition D
Lid Torque
Method 2024
168 Hours
Read and Record
Electrical Test
Constant Accel.
Method 2001
Condition E
Read and Record
Electrical Test
Die Shear
Method 2019
504 Hours
Read and Record
Electrical Test
Seal Test
Method 1014
Conditions B and C2
1000 Hours
Read and Record
Electrical Test
Read and Record
Electrical Test
Read and Record
Electrical Test
Delta Computation*
* Delta Computations
are optional

Group D

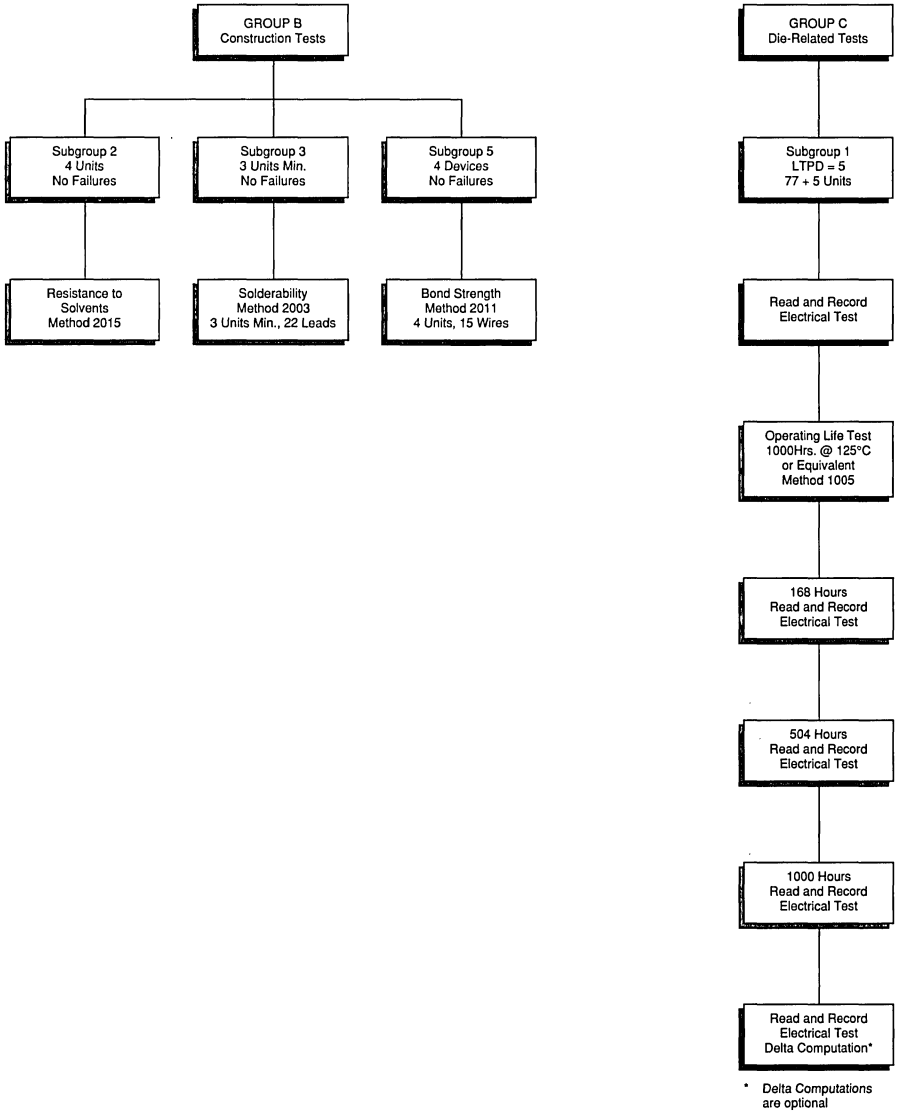

GROUP D
Package Tests
Subgroup 1
LTPD = 15
15 Units
Subgroup 2
LTPD = 15
15 Units
Subgroup 3
LTPD = 15
15 Units
Subgroup 4
LTPD = 15
15 Units
Subgroup 5
LTPD = 15
15 Units
Subgroup 6
3 Devices
No Failures
Subgroup 7
LTPD = 15
15 Units
Subgroup 8
5 Devices
No Failures
Physical Dimensions Method 2016
Lead Integrity Method 2004 Condition B2
Go / No-Go Elecrical Test
Go / No-Go Elecrical Test
Salt Atmosphere Method 1009
Internal Water Vapor Content Method 1018
Adhesion of Lead Finish Method 2025
Lid Torque (Frit Seal Only) Method 2024
Seal Test Method 1014 Fine Leak
Thermal Shock Method 1011 Condition B
Mechanical Shock Method 2002
Seal Test Method 1014 Conditions B and C
Seal Test Method 1014 Gross Leak
Temperature Cycling Method 1010
Vibration, Variable Frequency Method 2007
Visual Examination
Moisture Resistance Method 1004
Constant Acceleration Method 2001
Seal Test Method 1014 Conditions B and C2
Seal Test Method 1014 Conditions B and C2
Visual Examination
Visual Examination
Go / No-Go Electrical Test
Go / No-Go Electrical Test

QUALITY CONFORMANCE INSPECTION (Q.C.I.)

The following Group B, C and D tests are performed on a periodic basis or when specified by the customer. This testing is in compliance to MIL-M-38510 as detailed in MIL-STD-883, Method 5005.

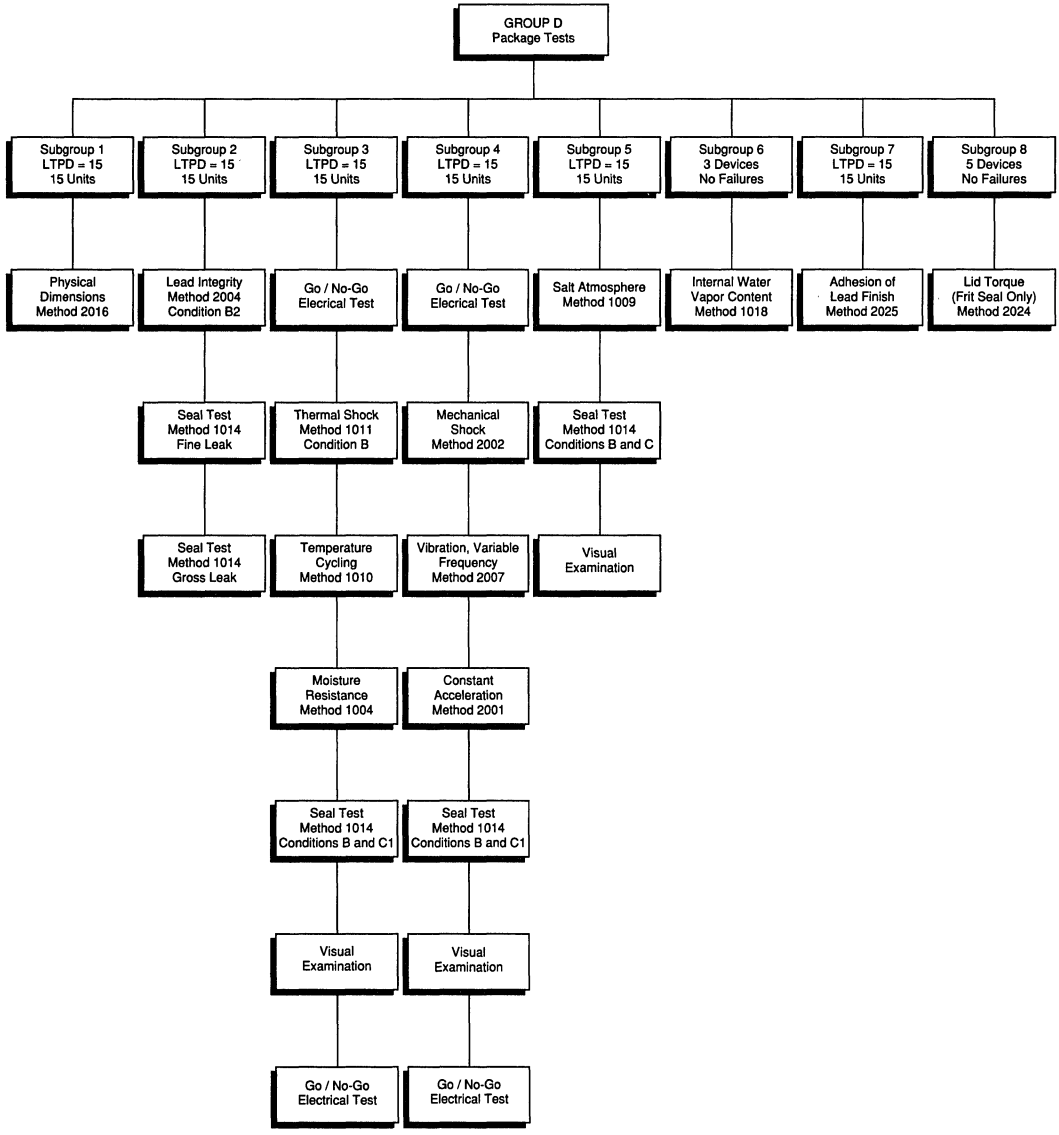


Groups B and C



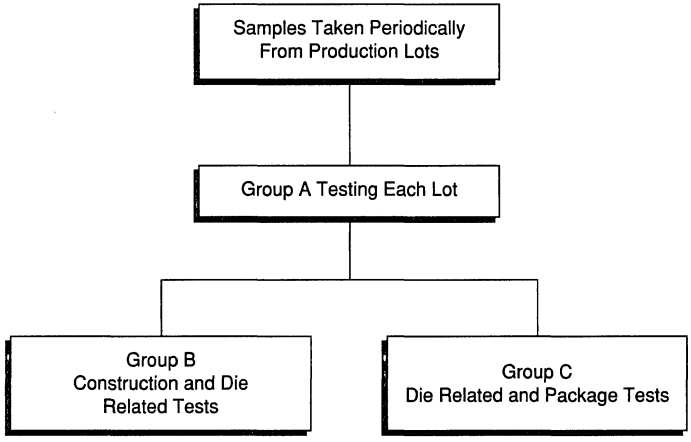
* Delta Computations are optional

Group D

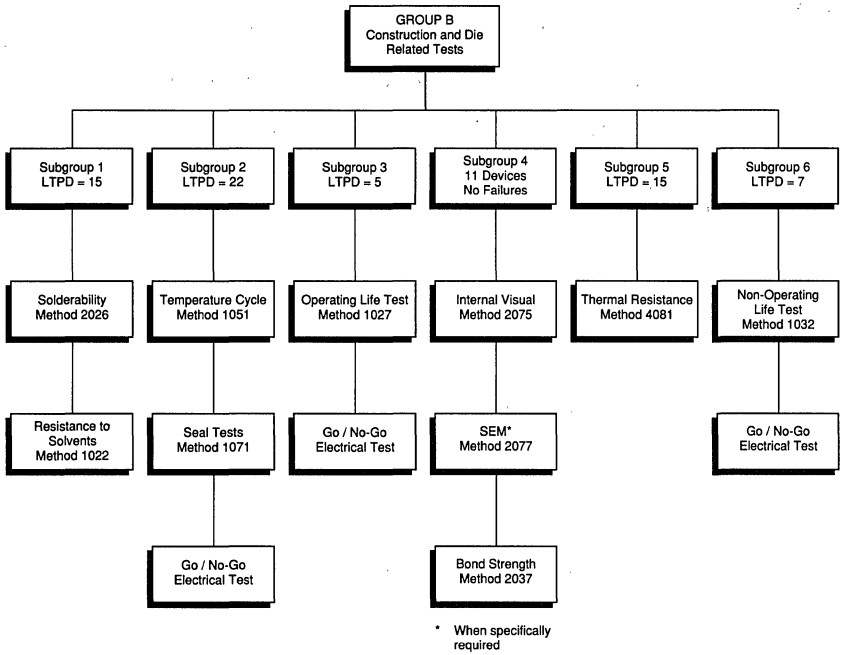

GROUP D
Package Tests
Subgroup 1
LTPD = 15
15 Units
Subgroup 2
LTPD = 15
15 Units
Subgroup 3
LTPD = 15
15 Units
Subgroup 4
LTPD = 15
15 Units
Subgroup 5
LTPD = 15
15 Units
Subgroup 6
3 Devices
No Failures
Subgroup 7
LTPD = 15
15 Units
Subgroup 8
5 Devices
No Failures
Physical Dimensions Method 2016
Lead Integrity Method 2004 Condition B2
Go / No-Go Elecrical Test
Go / No-Go Elecrical Test
Salt Atmosphere Method 1009
Internal Water Vapor Content Method 1018
Adhesion of Lead Finish Method 2025
Lid Torque (Frit Seal Only) Method 2024
Seal Test Method 1014 Fine Leak
Thermal Shock Method 1011 Condition B
Mechanical Shock Method 2002
Seal Test Method 1014 Conditions B and C
Seal Test Method 1014 Gross Leak
Temperature Cycling Method 1010
Vibration, Variable Frequency Method 2007
Visual Examination
Moisture Resistance Method 1004
Constant Acceleration Method 2001
Seal Test Method 1014 Conditions B and C1
Seal Test Method 1014 Conditions B and C1
Visual Examination
Visual Examination
Go / No-Go Electrical Test
Go / No-Go Electrical Test

QUALITY CONFORMANCE INSPECTION

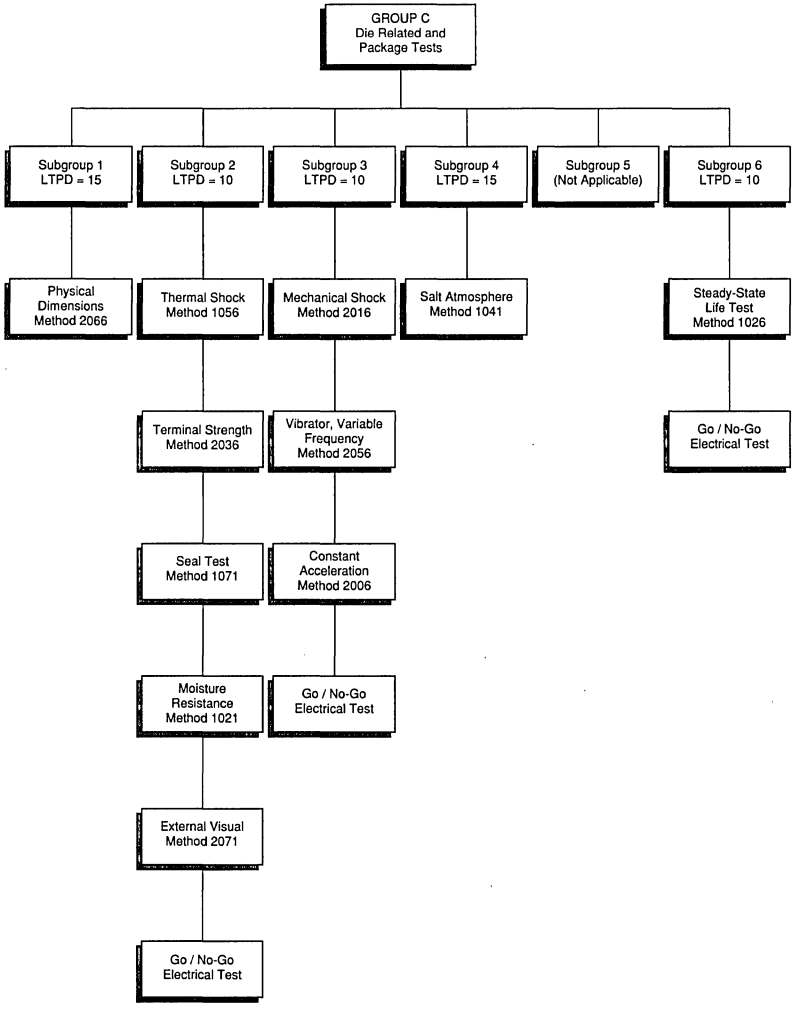
The following Group B and C tests are performed on a periodic basis or when specified by the customer. This testing is in compliance to MIL-S-19500 Class B quality is shown below.



Group B


GROUP B
Construction and Die
Related Tests
Subgroup 1
LTPD = 15
Subgroup 2
LTPD = 22
Subgroup 3
LTPD = 5
Subgroup 4
11 Devices
No Failures
Subgroup 5
LTPD = 15
Subgroup 6
LTPD = 7
Solderability
Method 2026
Temperature Cycle
Method 1051
Operating Life Test
Method 1027
Internal Visual
Method 2075
Thermal Resistance
Method 4081
Non-Operating
Life Test
Method 1032
Resistance to
Solvents
Method 1022
Seal Tests
Method 1071
Go / No-Go
Electrical Test
SEM*
Method 2077
Go / No-Go
Electrical Test
Go / No-Go
Electrical Test
Bond Strength
Method 2037
* When specifically
required

Group C


GROUP C
Die Related and
Package Tests
Subgroup 1
LTPD = 15
Subgroup 2
LTPD = 10
Subgroup 3
LTPD = 10
Subgroup 4
LTPD = 15
Subgroup 5
(Not Applicable)
Subgroup 6
LTPD = 10
Physical
Dimensions
Method 2066
Thermal Shock
Method 1056
Mechanical Shock
Method 2016
Salt Atmosphere
Method 1041
Steady-State
Life Test
Method 1026
Terminal Strength
Method 2036
Vibrator, Variable
Frequency
Method 2056
Go / No-Go
Electrical Test
Seal Test
Method 1071
Constant
Acceleration
Method 2006
Moisture
Resistance
Method 1021
Go / No-Go
Electrical Test
External Visual
Method 2071
Go / No-Go
Electrical Test

MILITARY PRODUCTS

PROCESS CAPABLILITIES

Silicon General offers a variety of design, test and processing capabilities that specialize in meeting the specific requirements of the military customer.

This commitment to the military marketplace has led Silicon General to staff and operate a fully certified MIL-M-38510 as well as MIL–S–19500 facility. This unique combination encompassing both discrete and microcircuit components solutions has proven valuable in solving the miitary customers needs.

The JAN market has become a vital part of our business and Silicon General has introduced a broad offering of components to support it. In addition to our current list of QPL devices we have developed an extensive list of products scheduled for future JAN qualification. These products will help to support the military's thrust for product standardization. Silicon General believes that this understanding of severe environment components has improved the quality of our entire product offering.

SILICON GENERAL SPECIFICATION PROGRAMS

- MIL-M-38510 - JAN
- MIL-S-19500 - JAN, TX, TXV
- DESC Drawings
- MIL - STD - 883
- MIL - STD - 750
- Source Control Drawings

ADDITIONAL - HIGH RELIABILITY OPTIONS

In addition to the process capabilities required by our military certification, we also offer the following process options for our space level and Ultra-High Reliability applications.

- PIND Testing
- X - Ray
- Radiation Testing
- SEM Analysis and Wafer Lot Acceptance
- Customer Source Inspection Program
- Custom Data Capability

This combination of small company customer service philosophy with large company capability has enabled Silicon General to become a key supplier in a broad range of High Reliability programs.

Contact Silicon General for a current listing of our JAN QPL and DESC DWG qualifications.

CUSTOM AND SEMI-CUSTOM INTEGRATED CIRCUITS

INTRODUCTION

Silicon General offers a wide range of full custom and semi-custom integrated circuits processed in a MIL-M-38510 and MIL-S-19500 certified facility.

CUSTOM CIRCUIT TECHNOLOGY

Full custom ICs are unique circuit topologies defined by the end user. By contrast, semi-custom ICs are circuit modifications and extrapolations of existing Silicon General devices. This might be as simple as unique electrical test programs or special packaging or as extensive as actually altering the original circuit design.

Silicon General has several circuit technologies to chose from in the design of a custom or semi-custom I.C. This choice can be defined by the end user or recommended by Silicon General. These technologies are shown in Table 1.

TABLE 1 - CUSTOM CIRCUIT TECHNOLOGIES

- Bipolar
- Gold - doped Bipolar
- CMOS
- Hybrids
- Silicon - on - Insulator

CUSTOM CIRCUIT CAPABILITY

The important characteristics for each of the technologies mentioned above in Table 1 are listed in the following section. These characteristics provide only a baseline as new processing modules are continually being developed. Please consult the factory for the latest innovations being made.

Bipolar

The details in Table 2 show the characteristics of the various junction isolated bipolar processes used at Silicon General.

TABLE 2 - BIPOLAR PROCESS CAPABILITIES

Process	F_T	Min. HFE	Min. V_{CBO}	Min. V_{CEO}	Current Rating	Double Layer Metal	Schottky	Gold Doping	Implant Resistor	Polysilicon Resistor
12V	1GHz	50	25V	14V	100mA	Yes	Yes	No	Yes	No
20V	600MHz	50	40V	20V	5A	Yes	Yes	Yes	Yes	Yes
40V	400MHz	50	60V	40V	5A	Yes	Yes	Yes	Yes	Yes
60V	250MHz	50	80V	60V	5A	No	No	Yes	Yes	Yes
Discrete	N/A	50	150V	100V	30A	No	No	Yes	N/A	N/A

Along with the broad bipolar processing capabilities, Silicon General offers proven building blocks with extensive reliability histories and known levels of operational performance. These blocks can be used as is or modified to accomodate an end users needs. Table 3 details the building blocks used extensively on Silicon General standard and custom/semi-custom circuits.

TABLE 3 - IC BUILDING BLOCKS

- Pulse Width Modulation techniques for switching power supplies and motor control applications
- Bandgap voltage references (tolerance < 1%)
- Oscillators
- Low dropout output stages (e.g. dropout <1V at 750mA)
- Various comparators and op-amps
- Full Logic
  - Gates, Flip Flops, Schmitt Triggers etc.
  - TTL, Schottky TTL, EFL, ECL, I^2L
  - Gate Delays ≥ 3nsec
- Discrete Transistor / Diode Arrays
- High Current, High Voltage Power Stages

CUSTOM CIRCUIT CAPABILITY (continued)

CMOS

Silicon General has in-house capability to develop Standard Cell or full custom CMOS I.C.'s. These I.C.'s are then processed at qualified outside foundries. This CMOS capability combined with the broad bipolar background enable Silicon General to aid in the partitioning of many end users applications. Current CMOS capabilities are listed in Table 4.

TABLE 4 - CMOS CAPABILITIES

- Geometries from 2.0μm to 1.2μm
- Standard Cell Library that includes:
  - 7400 SSI/MSI Logic Family
  - Static RAM to 64K
- CAD tools available:
  - Auto Place and Route (Standard Cell and Block)
  - Schematic Capture
  - Schematic Simulation
  - Layout vs. Schematic Checking (LVS)
  - Design Rule Checking (DRC)
  - Electrical Rule Checking (ERC)

Hybrid

A long history exists in the design and manufacture of thick film hybrids for the military, automotive, and commercial markets. For those applications where a single monolithic approach is not attainable Silicon General can combine a standard, custom or semi-custom I.C. with other components into a cost-effective, size efficient hybrid. Current thick film hybrid capabilities are listed in Table 5.

TABLE 5 - HYBRID CAPABILITIES

- Surface Mount or Chip and Wire technologies
- Custom Hybrid Packaging for both low and high power applications
- Full Military Processing
- Laser trimmed resistors:
  - 0.5% absolute value
  - 0.2% matching
- Conformal Coating

Silicon on Insulator (SOI)

Currently under development is a proprietary state of the art SOI process designed specifically to improve the radiation hardening capability of Military I.C.'s produced at Silicon General. First product introduction will occur in 1989. The details of this process are shown on page 3-18. Target characteristics are listed in Table 6.

TABLE 6 - SOI CHARACTERISTICS

- Transistor isolation to 750V
- Minimum V_{CBO} = 130V, V_{CEO} = 80V
- Maximum Current Rating to 5A
- Dual Layer metal, Schottky, and gold doping capability
- F_T up to 6GHz
- Implant and Polysilicon resistors

PACKAGING ALTERNATIVES

Packaging alternatives are presented in Table 7. These range from the more common DIP to newer packages like the hermetic TO-220 and full custom packages. Trade-offs can be made concerning power handling capability, size, hermeticity and cost. The θ_{JC} and θ_{JA} values and package dimensions are given for most of these packages in Section 11 of this catalog. Silicon General product engineers are well equipped to assist in selecting the best package for your particular requirements.

TABLE 7 - PACKAGING ALTERNATIVES

- Ceramic and plastic dual in line
- Ceramic and plastic leadless and leaded chip carriers (J-lead available)
- Ceramic flatpacks
- Plastic S.O.I.C.
- Metal Can (TO-3, TO-5, TO-39, TO-46, TO-52, TO-66, TO-99)
- Hermetic TO-220 and plastic TO-220 outline package
- Power SIP
- Custom hermetic and plastic packages

CUSTOM CIRCUIT PROCESSING LEVELS

Silicon General's custom circuit experience is extensive. We have produced custom ICs for some of the most demanding environments, both military and commercial. Our custom circuits can be found on satellites, radar systems, gyroscopes, automobiles, missile systems, disc drives and catalog power supplies.

Table 8 contains a partial list of the processing levels available for custom circuits. This flexibility in processing combined with a MIL-M-38510, MIL-S-19500 approved facility results in a custom circuit supplier able to handle virtually all special program and end-user requirements.

TABLE 8 - CUSTOM CIRCUIT PROCESSING LEVELS

- MIL - STD - 883
  - Class B
  - Class S
- MIL - STD - 750
  - JAN
  - JANTX
  - JANTXV
- Die processing; MIL - STD - 883, Level B, Level S
- Military (-55°C to 125°C)
- Automotive (-40°C to 125°C)
- Industrial (-25°C to 85°C)
- Commercial (0°C to 70°C)
- Extended temperature range
- Wafer traceability, wafer lot acceptance, SEM
- Special processing (end user defined)

CONCLUSION

Silicon General is committed to building long-term customer relationships. To be a valued supplier; we must provide, on time, a quality product, which meets not only the customer specification but the device application as well. Our military certified facility and production capability, both military and commercial, define Silicon General as a custom IC supplier able to support virtually any end-user requirement.

Silicon General has the production resources, technical expertise and commitment to quality to provide a TOTAL SERVICE (end-user defined) custom integrated circuit program.

RADIATION HARDENED INTEGRATED CIRCUITS

INTRODUCTION

After successfully participating in most of the strategic military and space programs of the last two decades, Silicon General is focusing its efforts in these areas by forming a division that will design and produce RADIATION HARDENED linear integrated circuits. The RAD HARD IC TECHNOLOGIES Division, in conjunction with Silicon General's established Level "S" and custom processing programs, will be able to better serve the needs of today's demanding space and military programs by providing radiation hardened custom and standard linear ICs.

RAD HARD TECHNOLOGY

The RAD HARD IC TECHNOLOGIES Division begins the design of a radiation hardened device by studying the customer's radiation and electrical performance requirements to determine required device geometries and radiation hardening techniques. Circuit simulations are used to verify device performance; prototypes are provided to the customer to verify system performance. In this way Silicon General reduces the risk of a radiation or electrical specification issue when the final product is delivered. Many factors are considered but the major areas of concern when designing a device for specific radiation performance are the device electrical design, circuit layout and fabrication processes. Listed below are some of the techniques used by Silicon General.

DESIGN / LAYOUT CONSIDERATIONS

- Beta degradation tolerant electrical design ensures the system designer worst case electrical specification after the radiation event.
- Photocurrent compensation is used to minimize the circuit upset during a radiation event.
- In junction isolated devices, NPN and PNP transistors are spaced for maximum radiation tolerance.

FABRICATION PROCESSES

- The key fabrication process used at Silicon General for radiation hardening is a propretary process called *TISER* (See figure 1). The acronym stands for Trench Isolated Selective Epi Regrowth. It is a Silicon On Insulator process that offers many advantages over older isolation techniques, such as Dielectric Isolation. *TISER* is used in any circuit design requiring low photo current generation or latch-up free operating during a Gamma Dot event.

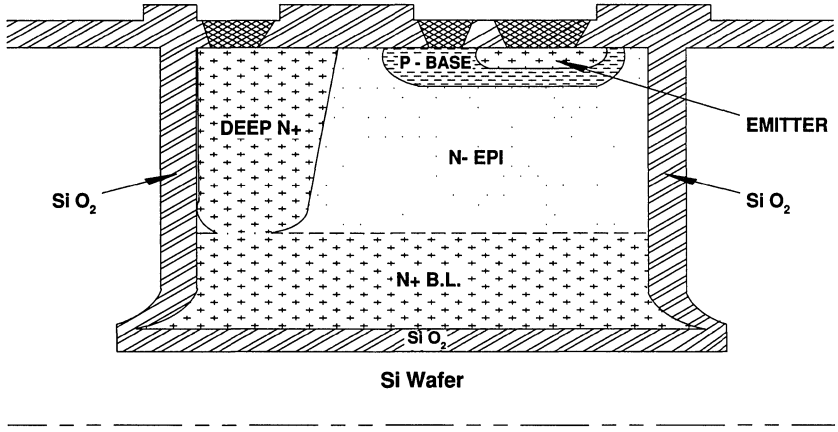


Figure 1. NPN Transistor

- Buried zener references are used instead of surface zeners to minimize the effect of surface charge build-up.
- Other fabrication processes, such as Submetal Nitride Passivation, Double diffused PNP transistors, and Oxide Isolated resistors, are also used.

In addition to custom radiation hardened designs, Silicon General plans to introduce a line of rad hard "industry standard" linear devices, e.g., LM117, LM137, ... Please call Silicon General or your local Silicon General representative for more information.

January 1990

SILICON GENERAL

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LINEAR INTEGRATED CIRCUITS

SELECTION GUIDE
POWER SUPPLY CIRCUITS

SWITCHING REGULATOR CONTROL IC's

DEVICE TYPE	Voltage Reference ± 4%	Voltage Reference ± 1%	Soft Start	PWM Latch	Under-Voltage Lockout	Pulse-by-Pulse Current Limiting	Shutdown Terminal	Output Transistor Rating (Vce, Peak Current)	Feed Forward	Maximum Frequency Oscillator	Uncommitted Outputs	Number of Outputs	Totem Pole Outputs	Separate Oscillator Sync Terminal	Adjustable Deadtime Control	Double Pulse Suppression	Low Current Start Up	Maximum Duty Cycle per Output	Packages
PERFORMANCE CHARACTERISTICS																			
Voltage Mode PWM																			
SG1524/2524/3524	•						•	40V 100mA		300KHz	•	2		•				<50%	J, N, D, F, L
SG1524B/2524B/3524B		•		•	•	•	•	60V 200mA		500KHz	•	2		•		•		<50%	J, N, DW, F, L
SG1525A/2525A/3525A		•	•	•	•		•	35V		500KHz		2	•	•	•			<50%	J, N, DW, F, L
SG1527A/2527A/3527A		•	•	•	•		•	0.4A					•	•	•				
SG1526/2526/3526		•	•	•	•	•	•	35V 0.4A		400KHz		2	•	•	•	•		<50%	J, N, DW, F, L
SG1526B/2526B/3526B		•	•	•	•	•	•	35V 0.4A		550KHz		2	•	•	•	•		<50%	J, N, DW, F, L
SG1529/2529/3529		•		•	•	•	•	60V 200mA	•	500KHz	•	2		•		•		<50%	J, N, DW
SG1840/2840/3840		•	•	•	•	•	•	30V 400mA	•	500KHz	•	1			•	N/A	•	<100%	J, N, DW
Current Mode PWM																			
SG1528/2528/3528		•	•	•	•	•		22V	•	3MHz		1	•	•		N/A	•	<50%	J, N, DW
SG1530/2530/3530		•	•	•	•	•		3A					•	•			•	<100%	
SG1825/2825/3825		•	•	•	•	•	•	30V 1.5A	•	2MHz		2	•	•	•	•	•	<50%	J, N, DW, F, L, Q
SG1842/2842/3842		•		•	•	•		30V	•	500KHz		1	•		•	N/A	•	<100%	J, N, Y, M, D, F, L
SG1843/2843/3843		•		•	•	•		1A	•				•		•		•		
SG1844/2844/3844		•		•	•	•			•				•		•		•	<50%	J, N, Y, M, D
SG1845/2845/3845		•		•	•	•			•				•		•		•		
SG1846/2846/3846		•	•	•	•	•	•	40V	•	500KHz		2	•	•	•	•		<50%	J, N, DW, F, L
SG1847/2847/3847		•	•	•	•	•	•	500mA	•				•	•	•	•			

November 1988

POWER SUPPLY SUPPORT FUNCTIONS

Device Type	Description	Key Features	Packages
SG1540/2540/3540	Off- line start up controller. Minimizes the cost and complexity of auxillary power supply.	• Eliminates bulky 50/60Hz transformer. • Minimizes high voltage bleeder current. • Usable with primary or secondary PWM contol. • Programmable start up voltage. • Programmable over voltage latch.	Y, M, DW, F
SG3561	Power factor controller	• Micro-power start-up mode • Low operating current consumption • Internal 5% reference • Totem pole output stage • Automatic current limiting of Boost stage • 8-pin DIP plastic package	Y, M
SG1542/2542/3542	Over/under voltage protection circuit	• Operation from 4.5V to 40V • Useful for either over- or under-voltage sensing • Built-in input hysterisis • Zero to 35V sensing capability • Programmable time delay • SCR "Crowbar" drive of 200mA • Remote activation capability • 2.6V 1% reference available	J, N, D, F
SG3523A/3523 SG3423A/3423	Over voltage protection circuit	• Operation from 4.5V to 40V • Highly accurate sensing threshold • Built-in input hysteresis • Programmable time delay • SCR "Crowbar" drive of 200mA • Remote activation capability	Y, M
SG1543/2543/3543 SG1544/2544/3544	Power supply supervisory circuit. Monitors and controls power supply output.	• Over-voltage, under-voltage, and current sensing circuits are all included • Programmable time delays • Internal 1% accurate reference available • Open collector outputs • Remote activation capability • SCR "Crowbar" drive of 300mA • Optional over voltage latch • Uncommited comparator • Inputs for low voltage sensing (SG1544 series only)	J, N, DW, F, L
SG1548/2548/3548	Quad power fault monitor. Monitors and controls four power supply outputs.	• Over-voltage and under-voltage sensing on four power supply outputs • Programmable time delay • Internal 1% accurate reference available • Open collector outputs. • Adjustable fault window • On-chip inverting op-amp for negative voltage • Additional input for AC line monitoring	J, N, DW, L

December 1989

POWER SUPPLY SUPPORT FUNCTIONS

Device Type	Description	Key Features	Packages
SG1549/2549/2549	Current sense latch. Monitors power supply output current.	• Current sense latching circuitry • Separate terminals for high and low common mode input sensing • Automatic reset from PWM clock • Complementary outputs available • Low propagation delays (180ns)	Y, M
SG1557/2557/3557 SG1559/2559/3559 SG1560/2560/3560	Low cost MAG-AMP controller. Controller for magnetic amplifiers or secondary side control applications.	• Lower cost than combined comparable discrete parts • Two independent op-amps (1557/59 series) • Two uncommited open collector comparators (1557/59 series) • ±2% voltage reference over line, load and temperature • Low input voltage operation • 13V zener for pre-regulating $+V_{IN}$ (1557/59 series) • Internal 100mV offset voltage built in one of the comparators (1559 series only)	J, N, Y, M, DW
SG1626/2626/3626 SG1644/2644/3644 SG1627/2627/3627 SG1629/2629/3629	High speed driver (Inv.) High speed driver (N.I.) Dual uncommited output driver Bipolar driver	SEE POWER DRIVER AND INTERFACE SECTION	
SG103/203/303 SG1503/2503/3503	Voltage reference Voltage reference	SEE OTHER LINEAR CIRCUITS SECTION	

SELECTION GUIDE
POWER SUPPLY CIRCUITS

VOLTAGE REGULATORS

Device Type	PERFORMANCE CHARACTERISTICS								
	Output Current	Polarity	Fixed	Adjustable	Dual	Low Dropout	Max. Input Voltage	Output Voltage (V)	Package
SG138/138A	5A	Positive		•			35V	1.2V to 38V	K (TO-3)
SG150	3A	Positive		•			35V	1.2V to 33V	K (TO-3), P (TO-220)
SG117/117A	1.5A	Positive		•			35V	1.2V to 37V	K (TO-3), R (TO-66),
SG117HV/117AHV				•			60V	1.2V to 57V	P (TO-220),
SG140		Positive	•				35V	5, 6, 8, 12, 15,	G (Hermetic TO-220),
SG7800			•					18, 20, 24	IG (Hermetic TO-220)
SG109		Positive	•				35V	5V	
SG137/137A		Negative		•			35V	-1.2V to -37V	
SG137HV				•			60V	-1.2V to -57V	
SG120		Negative	•				35V	-5, -5.2, -8, -12,	
SG7900/7900A			•					-15 -18, -20	
SG29055/55A*	0.75A	Positive	•		•	•	26V	5V, 5V	P (TO-220)
SG29085/85A*		Positive	•		•	•	26V	8V, 5V	
SG29125/125A*		Positive	•		•	•	26V	12V, 5V	
SG117/117A	0.5A	Positive		•			35V	1.2V to 37V	T (TO-39)
SG117HV/117AHV				•			60V	1.2V to 57V	
SG7800/7800A		Positive	•				35V	5, 6, 8, 12, 15,	
								18, 20, 24	
SG109		Positive	•				35V	5V	
SG137/137A		Negative		•			35V	-1.2V to -37V	
SG137HV				•			60V	-1.2V to -57V	
SG120		Negative	•				35V	-5, -5.2, -8, -12,	
SG7900/7900A			•					-15, -18, -20	
SG1532	0.1A	Positive		•			50V	2V to 38V	J, N, T (TO-96)
SG723		Positive		•			50V	2V to 38V	
SG1501A		Negative/ Positive	•		•		±35V	±15V	J, N, T (TO-100)
SG1502		Negative/ Positive		•	•		±30V	±10V to ±28V	J, N
SG1568		Positive/ Negative	•		•		±30V	±15V	J, N, T (TO-100) R (TO-66)
SG105	0.02A	Positive		•			50V	4.5V to 40V	J, N, T (TO-99)
SG104		Negative		•			-50V	-0.015V to -40V	T (TO-100)

* See Automotive Section

December 1989

SWITCHING REGULATOR OUTPUT STAGE

Device Type	PERFORMANCE CHARACTERISTICS									
	Peak Output Current	Polarity	Input/Output Voltage (V)	Rise Time (ns)		Fall Time (ns)		On-State Voltage		Packages
				Voltage	Current	Voltage	Current	Transistor	Diode	
SM645	20A	Positive	60	60	150	175	300	1.5V @ 7A	1.25V @ 7A	K (TO-3)
SM646			80							
SM647			100							
SM655		Negative	60	60	175	300	300			
SM656			80							
SM657			100							
SM625	15A	Positive	60	60	150	175	300	1.5V @ 7A	1.25V @ 7A	R (TO-66) Isolated
SM626			80							
SM627			100							
SM635		Negative	60	60	175	300	300			
SM636			80							
SM637			100							
SM660	10A	Positive	60	60	150	175	300	1.5V @ 5A	1.25V @ 5A	R (TO-66) Isolated
SM661			80							
SM662			100							
SM670		Negative	60	60	175	300	300			
SM671			80							
SM672			100							
SM600	5A	Positive	60	50	75	75	150	1.5V @ 2A	1.0V @ 2A	R (TO-66) Isolated
SM601			80							
SM602			100							
SM610		Negative	60	50	75	75	150			
SM611			80							
SM612			100							

November 1988

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

NEGATIVE VOLTAGE REGULATOR

DESCRIPTION

This circuit is a negative voltage regulator designed for both linear and switching applications. It is a complement of the SG100/200/300, SG105/205/305 and SG723/723C intended for systems requiring regulated negative voltages having a common ground with the unregulated supply. With an input voltage rating of up to 50 volts, this device will deliver load currents to 25 milliamps. Adding external transistors will increase the current capability to greater than 10amps and further improve regulation.

The SG104 will operate over the full military ambient temperature range of -55°C to +125°C. The SG204 operates over the temperature range of -25°C to 85°C while the SG304 is designed for commercial applications of 0°C to 70°C.

FEATURES

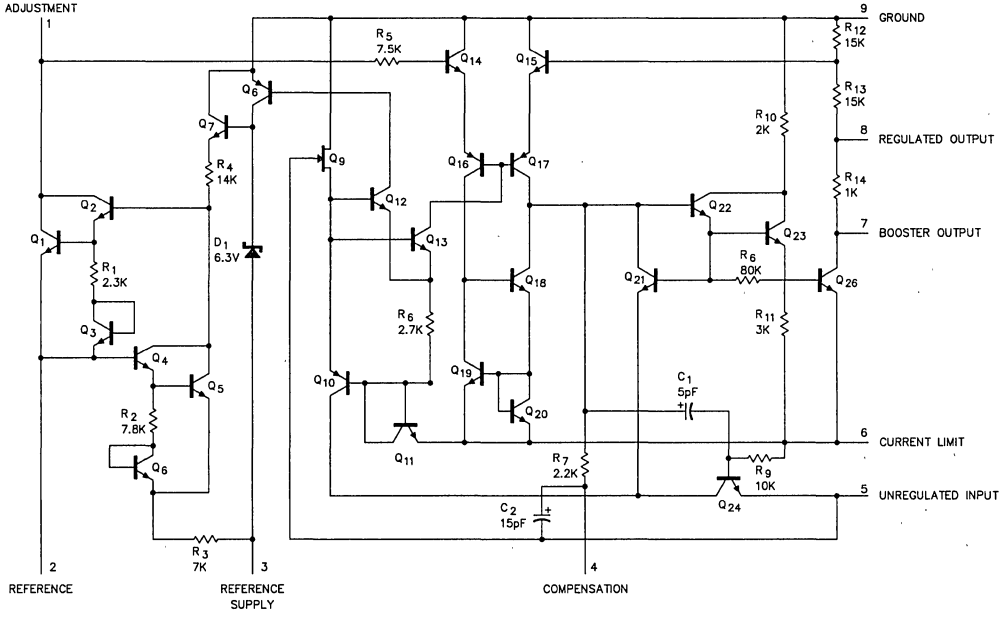
- **Output voltage adjustable from 15mV to 40V**
- **1mV regulation no load to full load**
- **0.01%/V lin regulation**
- **1% maximum temperature variation**

HIGH RELIABILITY FEATURES - SG104

- **Available to MIL-STD-883B**
- **SG level "S" processing available**

4

BLOCK DIAGRAM



April 1990

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage
- SG104, SG204 ..... 50V
- SG304 ..... 40V

Input - Output Voltage Differential
- SG104, SG204 ..... 50V
- SG304 ..... 40V

Operating Junction Temperature
- Hermetic (T-Package) ..... 150°C

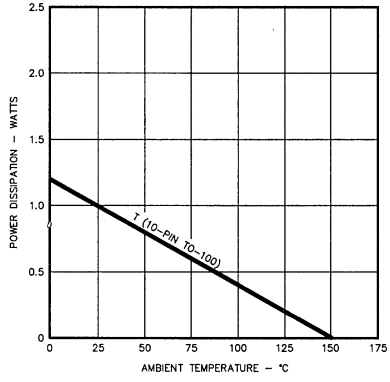
Power Dissipation 500mW

Storage Temperature Range ..... -65°C to 150°C

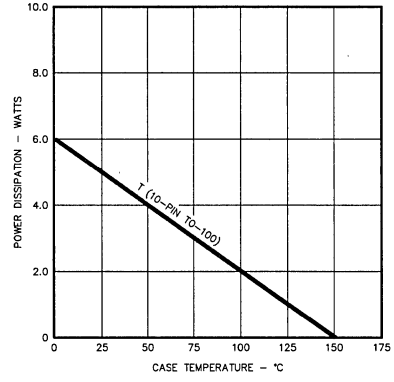
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Voltage
- SG104, SG204 ..... 8V to 48V
- SG304 ..... 8V to 38V

Input - Output Voltage Differential
- SG104, SG204 ..... 4V to 47V
- SG304 ..... 4V to 37V

Operating Ambient Temperature Range
- SG104 ..... -55°C to 125°C
- SG204 ..... -25°C to 85°C
- SG304 ..... 0°C to 70°C

Note 2: Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG104 with -55°C ≤ T_A ≤ 125°C, SG204 with -55°C ≤ T_A ≤ 125°C, SG304 with -55°C ≤ T_A ≤ 70°C. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG104/204			SG304			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Voltage Range		-50		-8	-40		-8	V
Output Voltage Range		-40		-0.015	-30		-0.035	V
Output - Input Voltage	I_O = 20mA	2.0		50	2.0		40	V
Differential (Note 2)	I_O = 5mA	0.5		50	0.5		40	V
Load Regulation (Note 3)	0 ≤ I_O ≤ 20mA, R_{SC} = 15Ω		1	5		1	5	mV
Line Regulation (Note 4)	V_{OUT} ≤ -5V, ΔV_{IN} = 0.1 V_{IN}		0.056	0.1		0.056	0.1	%
Ripple Rejection	$C_{PIN1 - PIN9}$ = 10μF, f = 120Hz							
	V_{IN} < -15V		0.2	0.5		0.2	0.5	mV/V
	-7V ≥ V_{IN} ≥ -15V		0.5	1.0		0.5	1.0	mV/V

Note 2. When external booster transistors are used, the minimum output-input voltage differential is increased, in the worst case, by approximately 1 volt.

Note 3. The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.

Note 4. With zero output, the DC line regulation is determined from the ripple rejection. Hence, with output voltages between 0 volts and -5volts, a DC output variation, determined from the ripple rejection, must be added to find the worst-case line regulation.

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG104/204			SG304			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage Scale Factor	$R_{PIN2-PIN3}$ = 2.4k	1.8	2.0	2.2	1.8	2.0	2.2	V/KΩ
Temperature Stability	$V_O \leq$ -1V		0.3	1.0		0.3	1.0	%
Output Noise Voltage	10Hz ≤ f ≤ 10KHz							
	$V_O \leq$ -5V, $C_{PIN1-PIN9}$ = 0		0.007			0.007		%
	$C_{PIN1-PIN9}$ = 10μF		15			15		μV
Standby Current Drain	I_L = 5mA, V_O = 0		1.7	2.5		1.7	2.5	mA
	V_O = -30V					3.6	5.0	mA
	V_O = -40V		3.6	5.0				mA
Long Term Stability	$V_O \leq$ -1V		0.1	1.0		0.1	1.0	%

APPLICATION CIRCUITS

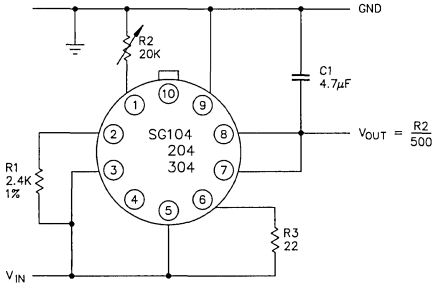


FIGURE 1 - BASIC NEGATIVE REGULATOR CIRCUIT

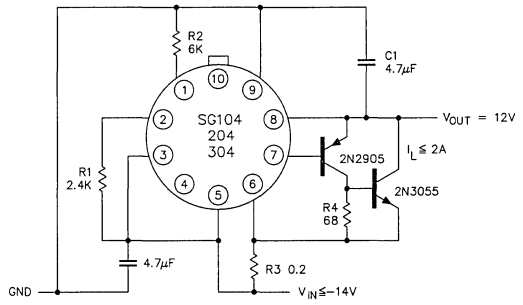
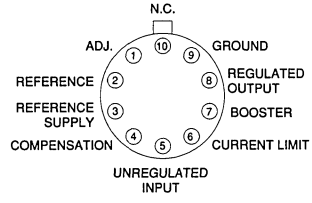


FIGURE 1 - HIGH CURRENT REGULATOR CIRCUIT

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
10-PIN TO-100 METAL CAN T-PACKAGE	SG104T/883B	-55°C to 125°C	
	SG104T	-55°C to 125°C	
	SG204T	-25°C to 85°C	
	SG304T	0°C to 70°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

POSITIVE VOLTAGE REGULATOR

DESCRIPTION

This circuit is a positive voltage regulator designed for both linear and switching applications. Inherent component tracking of the monolithic integrated circuit process provides a high degree of stability and accuracy in addition to fast response to both line and load transients. With an input voltage rating of up to 50V, this device will deliver load currents of 20mA (45mA with 305A). Adding external transistors will increase the current capability to greater than 10amps and further improve regulation.

FEATURES

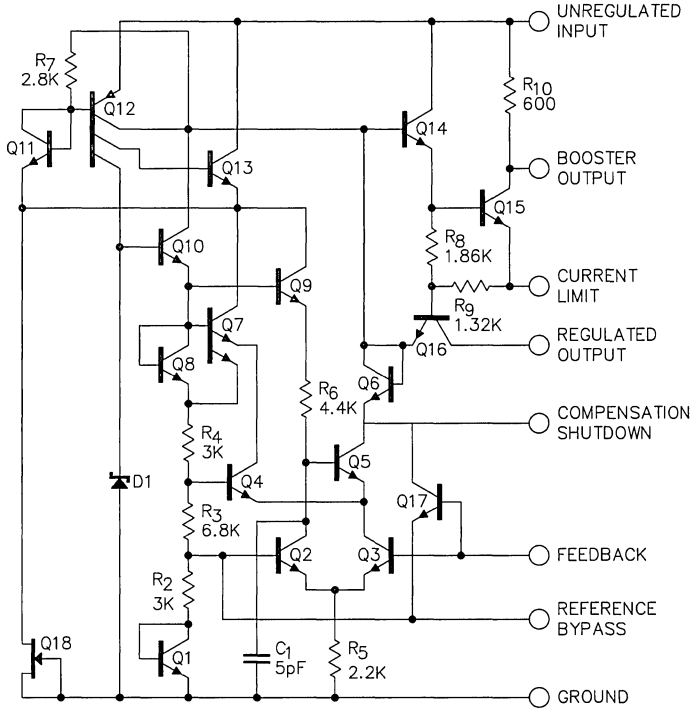
- **Output voltage adjustable from 4.5V to 40V**
- **Load regulation better than 0.01%/mA**
- **Line regulation better than 0.06%/V**
- **Ripple rejection of 0.01%/V**
- **1.0% maximum temperature variation**

HIGH RELIABILITY FEATURES - SG105

- **Available to MIL-STD-883B**
- **SG level "S" processing available**

4

BLOCK DIAGRAM



April 1990

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage
- SG105 ..... 50V
- SG205 ..... 50V
- SG305 ..... 40V
- SG305A 50V

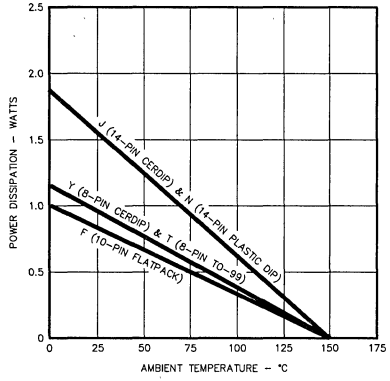
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Input - Output Voltage Differential
- SG105 ..... 30V
- SG205 ..... 30V
- SG305 ..... 30V
- SG305A 30V

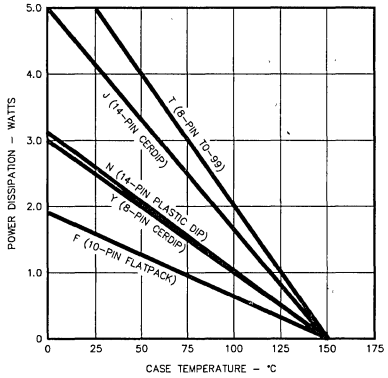
Operating Junction Temperatures
- Hermetic (T, J, F, Y-Packages) ..... 150°C
- Plastic (N-Packages) ..... 150°C

Note 1. Values beyond which damage may occur.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Voltage
- SG105, SG205, SG305A ..... 10V to 48V
- SG305 ..... 10V to 38V

Input - Output Voltage Differential
- SG105, SG205, SG305, SG305A ..... 5V to 28V

Operating Ambient Temperature Range
- SG105 ..... -55°C to 125°C
- SG205 ..... -25°C to 85°C
- SG305, SG305A ..... 0°C to 70°C

Note 2: Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG105 with -55°C ≤ T_A ≤ 125°C, SG205 with -25°C ≤ T_A ≤ 85°C, and SG305 with 0°C ≤ T_A ≤ 70°C. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG105/205			SG305			SG305A			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Voltage Range		8.5		50	8.0		40	8.5		50	V
Output Voltage Range		4.5		40	4.5		30	4.5		40	V
Input/Output Differential		3.0		30	3.0		30	3.0		30	V
Load Regulation (Note 4)	I_L < 12mA, R_{SC} = 10Ω			0.1			0.1			0.2	%
Line Regulation	V_{IN} - V_{OUT} ≤ 5V			0.06			0.06			0.06	%/V
	V_{IN} - V_{OUT} > 5V			0.03			0.03			0.03	%/V
Ripple Feed	C_{REF} = 10μF, f = 120Hz			0.01			0.01		0.003		%/V
Temperature Stability (Note 3)				1.0			1.0			1.0	%
Output Noise Voltage	10Hz ≤ f ≤ 10KHz, C_{REF} = 0		0.005			0.005			0.005		%
Feedback Sense Voltage		1.55	1.7	1.85	1.55	1.7	1.85	1.55		1.85	V
Standby Current Drain				2.0			2.0			2.0	mA
Load Current		0			0			0			mA
Long Term Stability (Note 3)			0.1	1.0		0.1	1.0		0.1	1.0	%

Note 3. This test is guaranteed but not tested.
Note 4. Applies for constant junction temperature.

CHARACTERISTIC CURVES (continued)

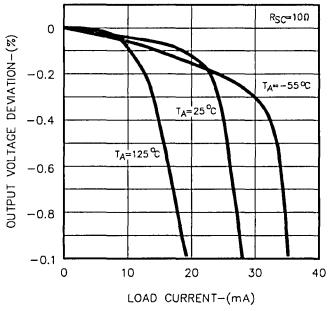


FIGURE 1.
LOAD REGULATION

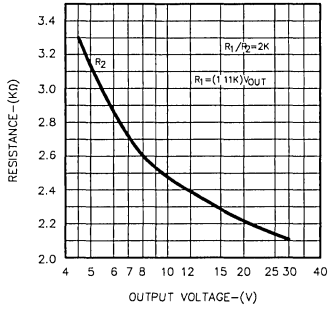


FIGURE 2.
OPTIMUM DIVIDER RESISTOR VALUES

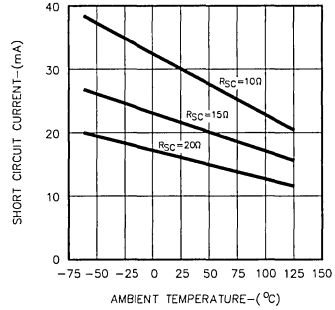


FIGURE 3.
CURRENT LIMITNG

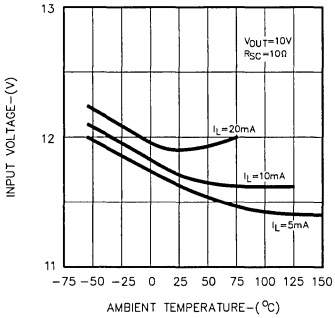


FIGURE 4.
DROPOUT VOLTAGE

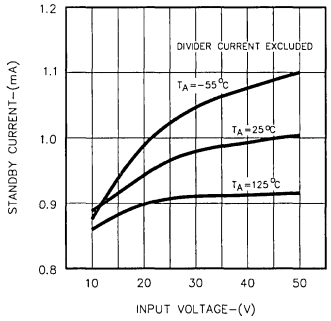


FIGURE 5.
STANDBY CURRENT DRAIN

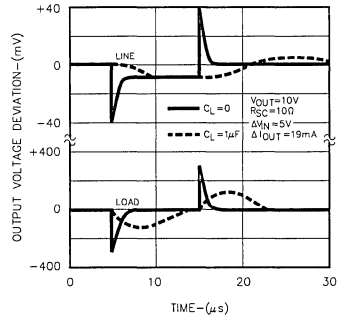


FIGURE 6.
TRANSIENT RESPONSE

APPLICATION CIRCUITS

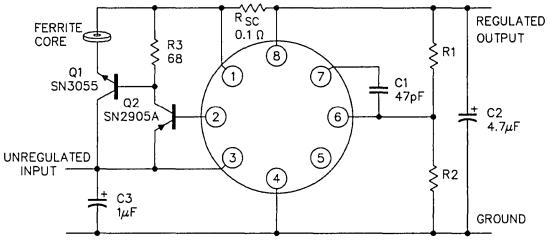


FIGURE 7 - REGULATOR CONNECTED FOR 2 AMP OUTPUT

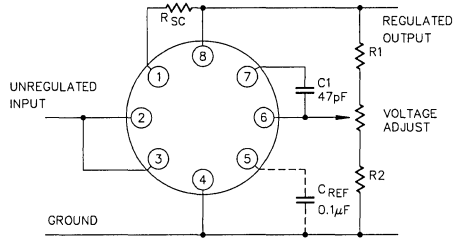
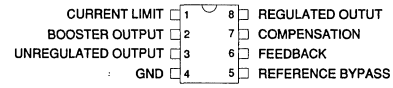
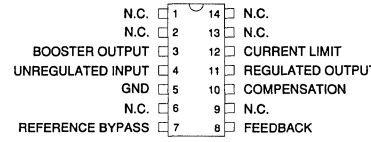
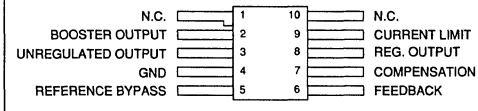
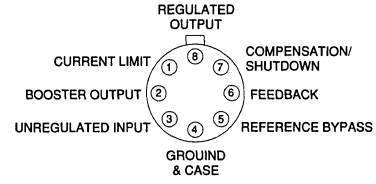


FIGURE 8 - BASIC REGULATOR CIRCUIT

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
8-PIN CERAMIC DIP Y - PACKAGE	SG105Y/883B SG105Y SG205Y SG305Y SG305AY	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C 0°C to 70°C	
14-PIN CERAMIC DIP J - PACKAGE	SG105J/883B SG105J SG205J SG305J SG305AJ	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C 0°C to 70°C	
14-PIN PLASTIC DIP N - PACKAGE	SG205N SG305N SG305AN	-25°C to 85°C 0°C to 70°C 0°C to 70°C	
10-PIN CERAMIC FLATPACK F - PACKAGE	SG105F/883B SG105F	-55°C to 125°C -55°C to 125°C	
8-PIN TO-99 METAL CAN T-PACKAGE	SG105T/883B SG105T SG205T SG305T SG305AT	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C 0°C to 70°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

5 -VOLT FIXED VOLTAGE REGULATORS

DESCRIPTION

The SG109/SG309 is a completely self-contained 5V regulator. Designed to provide local regualtion at currents up to 1A for digital logic cards, this device is available in the hermetic TO-3, TO-66, TO-39 and hermetic and plastic TO-220.

A major feature of the SG109's design is its built-in protective features which make it essentially blowout proof. These consist of both current limiting to control the peak currents and thermal shutdown to protect against excessive power dissipation. With the only added component being a possible need for an input bypass capacitor, this regulator becomes extremely easy to apply. Utilizing an improved Bandgap reference design, problems have been eliminated that are normally associated with the zener diode references, such as drift in output voltage and large changes in the line and load regulation.

FEATURES

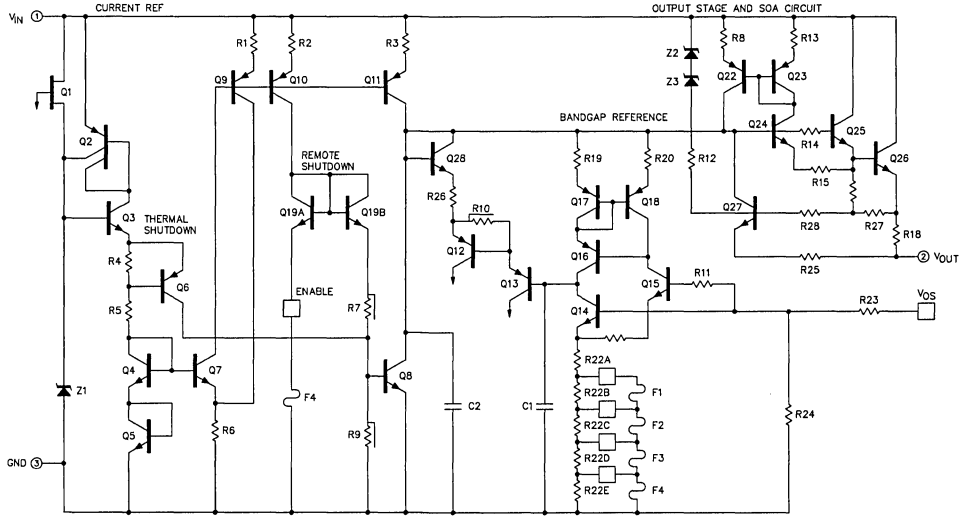
- **Fully compatible with TTL and DTL**
- **Output current in excess of 1A**
- **Internal thermal overload protection**
- **No additional external components**
- **Bandgap reference voltage**
- **Foldback current limiting**

HIGH RELIABILITY FEATURES-SG109

- **Available to MIL-STD-883**
- **MIL - M38510 / 10701BXA - JAN109T**
- **Radiation data available**
- **SG level "S" processing available**

4

SCHEMATIC



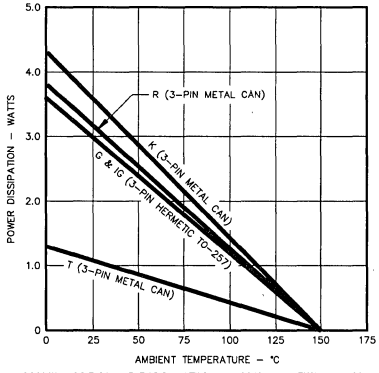
ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage 35V
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... -65°C to 150°C

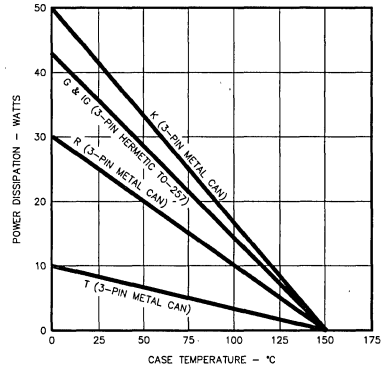
Operating Junction Temperature
Hermetic (K, R, T, G, IG-Packages) ..... 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Voltage Range ..... 7.0V to 25V

Operating Junction Temperature Range
SG109 ..... -55°C to 150°C
SG309 ..... 0°C to 125°C

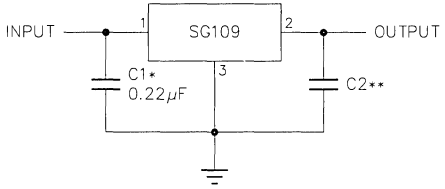
Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG109 with -55°C ≤ T_A ≤ 150°C, SG309 with 0°C ≤ T_A ≤ 125°C, and for V_{IN} = 10V, I_{OUT} = 500mA (K, R, G, and IG -Power Packages-) and I_{OUT} = 100mA (T-package). Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG109			SG309			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_A = 25°C	4.7	5.05	5.3	4.8	5.05	5.2	V
Line Regulation	V_{IN} = 7.1V to 25V, T_A = 25°C		4.0	50		4.0	50	mV
Load Regulation	T_A = 25°C							
	Power Pkgs: I_{OUT} = 5mA to 1.5A		15	100		15	100	mV
	T-package: I_{OUT} =5mA to 500mA		15	50		15	50	mV
Total Output Voltage Tolerance	V_{IN}= 7.4V to 25V							
	Power Pkgs: I_{OUT} = 5mA to 1.0A, P ≤ 20W	4.6	5.0	5.4	4.75	5.00	5.25	V
	T-package: I_{OUT} =5mA to 200mA, P ≤ 20W	4.6	5.0	5.4	4/75	5.00	5.25	V
Quiescent Current	V_{IN} = 7.4V to 25V			10			10	mA
Quiescent Current Change	With Line : V_{IN} = 7.4V to 25V			0.5			0.5	mA
	With Load: Power Pkgs: I_{OUT} = 5mA to 1.0A			0.8			0.8	mA
	T-package: I_{OUT} =5mA to 200mA			0.8			0.8	mA
Output Noise Voltage	f = 10Hz to 100KHz, T_A = 25°C		40			40		µV
Long Term Stability			10			20		mV
Ripple Rejection	T_A = 25°C	50			50			dB

APPLICATION CIRCUITS



* REQUIRED IF REGULATOR IS AN APPRECIABLE DISTANCE FROM POWER SUPPLY FILTER

** ALTHOUGH NO OUTPUT CAPACITOR IS NEEDED FOR STABILITY IT DOES IMPROVE TRANSIENT RESPONSE.

FIGURE 1 - FIXED 5V REGULATOR

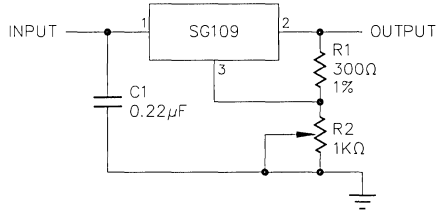
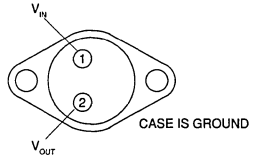
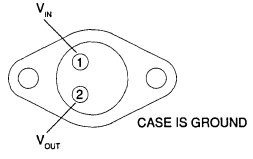
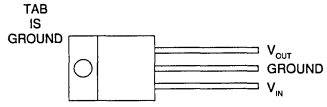
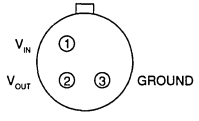


FIGURE 2 - ADJUSTABLE OUTPUT REGULATOR

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
3-TERMINAL TO-3 METAL CAN K-PACKAGE	SG109K/883B SG109K SG309K	-55°C to 125°C -55°C to 125°C 0°C to 70°C	
3-TERMINAL TO-66 METAL CAN R-PACKAGE	SG109R/883B SG109R SG309R	-55°C to 125°C -55°C to 125°C 0°C to 70°C	
3-PIN HERMETIC TO-257 G-PACKAGE (Non-Isolated) 3-PIN HERMETIC TO-257 IG-PACKAGE (Isolated)	SG109G/883B SG109G SG109IG/883B SG109IG	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C	
3-PIN TO-39 METAL CAN T-PACKAGE	SG109T/883B SG109T SG309T	-55°C to 125°C -55°C to 125°C 0°C to 70°C	

Note 1. Contact factory for JAN and DESC product availability.
2. All parts are viewed from the top.
3. Product is also available in leadless chip carrier (LCC) and hermetic flat pack (F). Contact factory for price and availability.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SG117A/SG217A/SG317A
SG117/SG217/SG317

1.5 AMP THREE TERMINAL ADJUSTABLE VOLTAGE REGULATOR

DESCRIPTION

The SG117A Series are 3-terminal positive adjustable voltage regulators which offer improved performance over the original 117 design. A major feature of the SG117A is reference voltage tolerance guaranteed within ± 1%, allowing an overall power supply tolerance to be better than 3% using inexpensive 1% resistors. Line and load regulation performance has been improved as well. Additionally, the SG117A reference voltage is guaranteed not to exceed 2% when operating over the full load, line and power dissipation conditions. The SG117A adjustable regulators offer an improved solution for all positive voltage regulator requirements with load currents up to 1.5A.

FEATURES

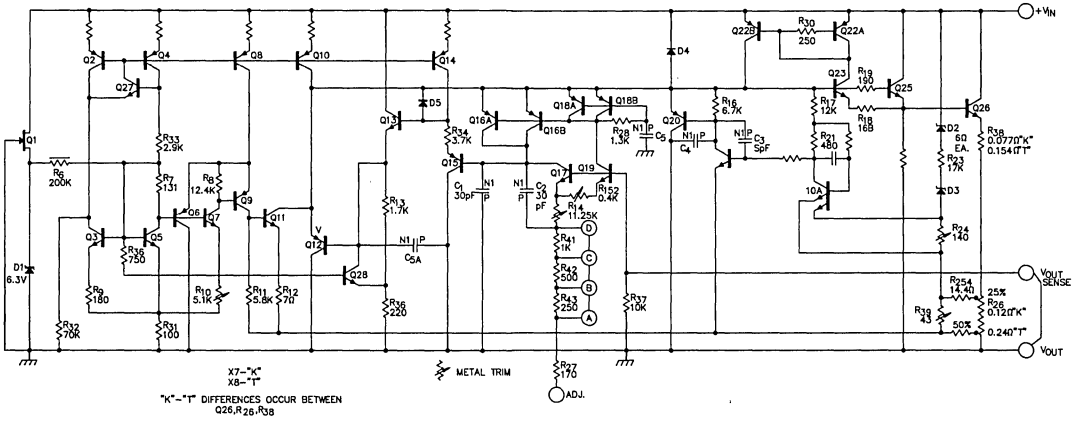
- **1% output voltage tolerance**
- **0.01%/V line regulation**
- **0.3% load regulation**
- **Min. 1.5A output current**
- **Available in hermetic TO-220**

HIGH RELIABILITY FEATURES-SG117A/SG117

- **Available to MIL-STD-883 and DESC SMD**
- **MIL-M38510/11704BYA - JAN117K**
- **MIL-M38510/11704BXA - JAN117T**
- **SG level "S" processing available**

4

SCHEMATIC DIAGRAM



April 1990

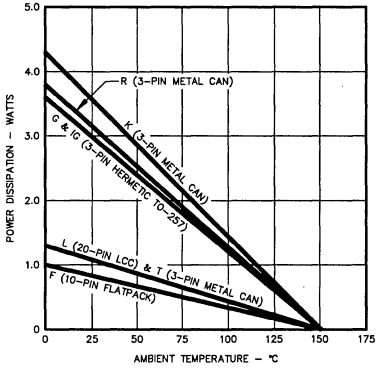
ABSOLUTE MAXIMUM RATINGS (Note 1)

Power Dissipation ..... Internally Limited
Input to Output Voltage Differential 40V
Storage Temperature Range ..... -65°C to 150°C

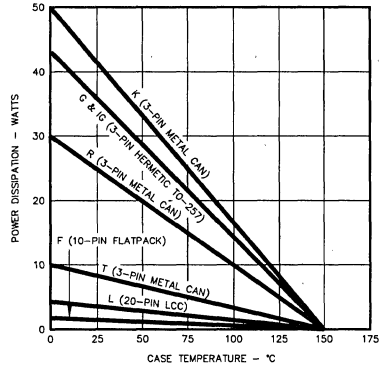
Operating Junction Temperature
Hermetic (K, R, T, F, L, G, IG-Packages) ..... 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2 & 3)

Input Voltage Range ..... (V_{OUT} + 3.5V) to 37V

Operating Junction Temperature Range
SG117A/SG117 ..... -55°C to 150°C
SG217A/SG217 ..... -25°C to 150°C
SG317A/SG317 ..... 0°C to 125°C

Note 2. Range over which the device is functional.
Note 3. These ratings are applicable for junction temperatures of less than 150°C.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over full operating ambient temperatures for SG117A/SG117 with -55°C ≤ T_A ≤ 125°C, SG217A/SG217 with -25°C ≤ T_A ≤ 150°C, SG 317A/SG317 with 0°C ≤ T_A ≤ 125°C, V_{IN} - V_{OUT} = 5.0V , and for I_{OUT} = 500mA (K, R, G and IG), and I_{OUT} = 100mA (T, F and L packages). Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the T, F, and L packages, and 20W for the K, R, G, and IG packages. I_{MAX} is 1.5A for the K, R, G, and IG packages and 500mA for the T, F, and L packages. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG117A/SG217A			SG117/SG217			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Voltage	I_{OUT} = 10mA T_A = 25°C	1.238	1.250	1.262				V
	3V ≤ (V_{IN} - V_{OUT}) ≤ 40V, P ≤ P_{MAX}, 10mA ≤ I_{OUT} ≤ I_{MAX}	1.225	1.250	1.270	1.20	1.25	1.30	V
Line Regulation (Note 4)	3V ≤ (V_{IN} - V_{OUT}) ≤ 40V, I_L = 10mA							
	T_A = 25°C		0.005	0.01		0.01	0.02	%/V
	T_A = T_{MIN} to T_{MAX}		0.01	0.02		0.02	0.05	%/V
Load Regulation (Note 4)	10mA ≤ I_{OUT} ≤ I_{MAX}							
	V_{OUT} ≤ 5V, T_A = 25°C		5	15		5	15	mV
	V_{OUT} ≥ 5V, T_A = 25°C		0.1	0.3		0.1	0.3	%
	V_{OUT} ≤ 5V		20	50		20	50	mV
	V_{OUT} ≥ 5V		0.3	1		0.3	1	%
Thermal Regulation (Note 5)	T_A = 25°C, 20ms pulse		0.002	0.02		0.03	0.07	%/W
Ripple Rejection	V_{OUT} = 10V, f =120Hz							
	C_{ADJ} = 1µF, T_A = 25°C		65			65		dB
	C_{ADJ} = 10µF	66	80		66	80		dB
Adjust Pin Current			50	100		50	100	µA
Adjust Pin Current Change	10mA ≤ I_{OUT} ≤ I_{MAX}, 2.5V ≤ (V_{IN} - V_{OUT}) ≤ 40V		0.2	5		0.2	5	µA

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG117A/SG217A			SG117/SG217			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Minimum Load Current	$(V_{IN} - V_{OUT}) = 40V$		3.5	5		3.5	5	mA
Current Limit	$(V_{IN} - V_{OUT}) \leq 15V$							
	K, P, R, G, IG Packages	1.5	2.2		1.5	2.2		A
	T, L, F Package	0.5	0.8		0.5	0.8		A
	$(V_{IN} - V_{OUT}) = 40V$, $T_J = 25°C$							
	K, P, R, G, IG Packages	0.3	0.4		0.3	0.4		A
	T, L, F Packages	0.15	0.2		0.15	0.2		A
Temperature Stability (Note 5)			1	2		1		%
Long Term Stability (Note 5)	$T_A = 125°C$, 1000 Hours		0.3	1		0.3	1	%
RMS Output Noise (% of V_{OUT})	$T_A = 25°C$, $10Hz \leq f \leq 10$ KHz (Note 5)		0.001			0.001		%

Parameter	Test Conditions	SG317A			SG317			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Voltage	$I_{OUT} = 10mA$ $T_A = 25°C$	1.238	1.250	1.262				V
	$3V \leq (V_{IN} - V_{OUT}) \leq 40V$, $P \leq P_{MAX}$,							
	$10mA \leq I_{OUT} \leq I_{MAX}$	1.225	1.250	1.270	1.20	1.25	1.30	V
Line Regulation (Note 4)	$3V \leq (V_{IN} - V_{OUT}) \leq 40V$, $I_L = 10mA$							
	$T_A = 25°C$		0.005	0.01		0.01	0.04	%/V
	$T_A = T_{MIN}$ to T_{MAX}		0.01	0.02		0.02	0.07	%/V
Load Regulation (Note 4)	$10mA \leq I_{OUT} \leq I_{MAX}$							
	$V_{OUT} \leq 5V$, $T_A = 25°C$		5	25		5	25	mV
	$V_{OUT} \geq 5V$, $T_A = 25°C$		0.1	0.5		0.1	0.5	%
	$V_{OUT} \leq 5V$		20	50		20	70	mV
	$V_{OUT} \geq 5V$		0.3	1		0.3	1.5	%
Thermal Regulation (Note 5)	$T_A = 25°C$, 20ms pulse		0.002	0.02		0.03	0.07	%/W
Ripple Rejection	$V_{OUT} = 10V$, f =120Hz							
	$C_{ADJ} = 1\mu F$, $T_A = 25°C$		65			65		dB
	$C_{ADJ} = 10\mu F$	66	80		66	80		dB
Adjust Pin Current	$T_A = 25°C$		50	100		50	100	µA
Adjust Pin Current Change	$10mA \leq I_{OUT} \leq I_{MAX}$, $2.5V \leq (V_{IN} - V_{OUT}) \leq 40V$		0.2	5		0.2	5	µA
Minimum Load Current	$(V_{IN} - V_{OUT}) = 40V$		3.5	10		3.5	10	mA
Current Limit	$(V_{IN} - V_{OUT}) \leq 15V$							
	K, P, R, G, IG Packages	1.5	2.2		1.5	2.2		A
	T, L, F Packages	0.5	0.8		0.5	0.8		A
	$(V_{IN} - V_{OUT}) = 40V$, $T_J = 25°C$							
	K, P, R, G, IG Packages	0.15	0.4		0.15	0.4		A
	T, L, F Packages	.075	0.2		.075	0.2		A
Temperature Stability (Note 5)			1	2		1		%
Long Term Stability (Note 5)	$T_A = 125°C$		0.3	1		0.3	1	%
RMS Output Noise (% of V_{OUT})	$T_A = 25°C$, $10Hz \leq f \leq 10KHz$ (Note 5)		0.001			0.001		%

Note 4. Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

Note 5. These parameters, although guaranteed, are not tested in production.

4

CHARACTERISTIC CURVES

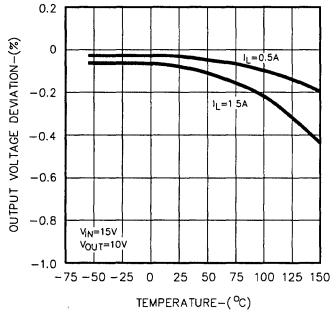


FIGURE 1.
OUTPUT VOLTAGE DEVIATION VS. TEMPERATURE

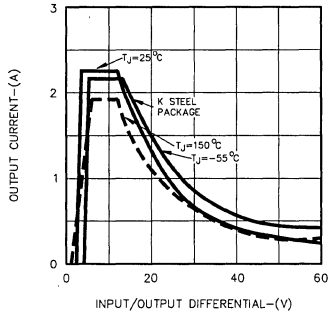


FIGURE 2.
OUTPUT CURRENT VS. INPUT/OUTPUT DIFFERENTIAL

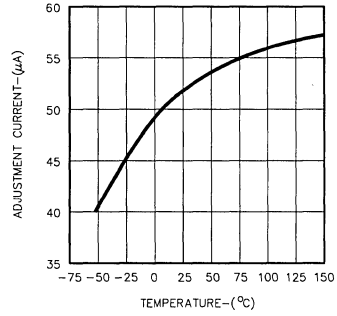


FIGURE 3.
ADJUSTMENT CURRENT VS. TEMPERATURE

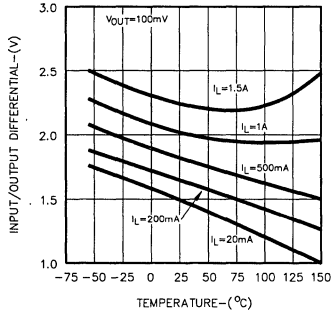


FIGURE 4.
INPUT/OUTPUT DIFFERENTIAL VS. TEMPERATURE

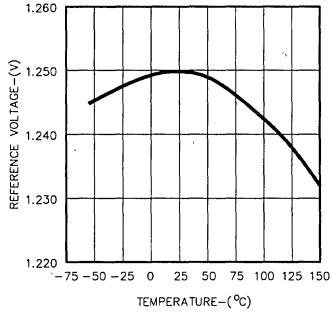


FIGURE 5.
REFERENCE VOLTAGE VS. TEMPERATURE

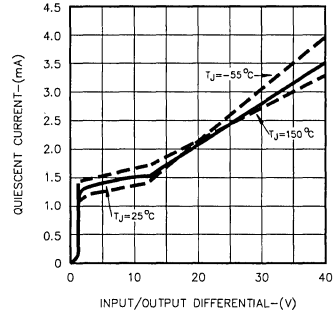


FIGURE 6.
QUIESCENT CURRENT VS. INPUT/OUTPUT DIFFERENTIAL

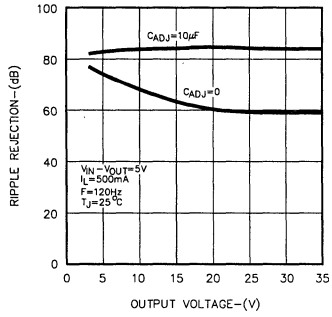


FIGURE 7.
RIPPLE REJECTION VS. OUTPUT VOLTAGE

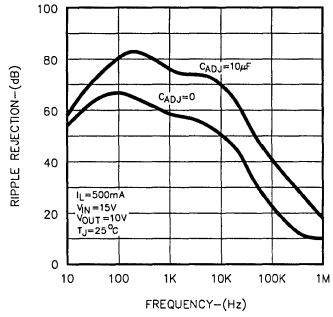


FIGURE 8.
RIPPLE REJECTION VS. FREQUENCY

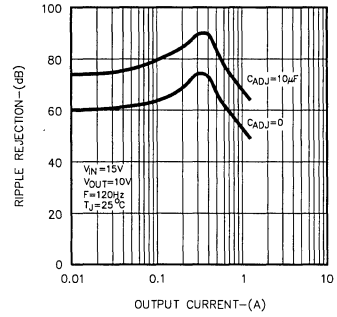


FIGURE 9.
RIPPLE REJECTION VS. OUTPUT CURRENT

CHARACTERISTIC CURVES (continued)

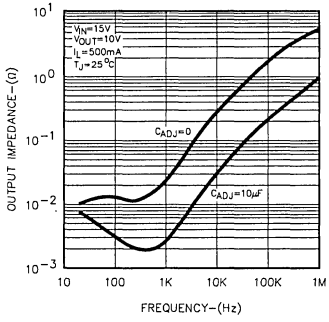


FIGURE 10.
OUTPUT IMPEDANCE VS. FEQUENCY

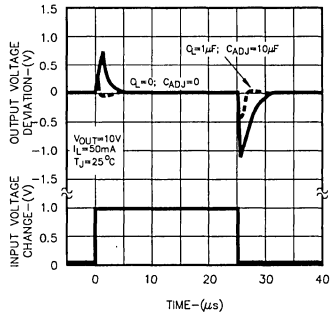


FIGURE 11.
LINE TRANSIENT RESPONSE

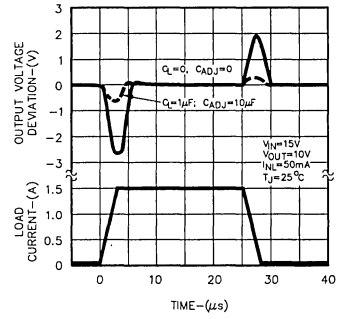


FIGURE 12.
LOAD TRANSIENT RESPONSE

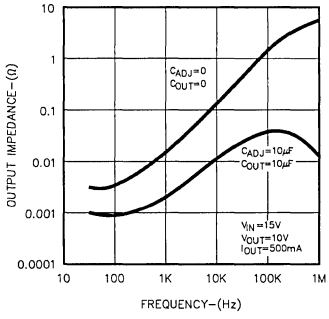


FIGURE 13.
OUTPUT IMPEDANCE VS. FREQUENCY

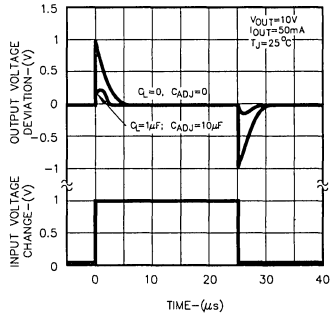


FIGURE 14.
LINE TRANSIENT RESPONSE

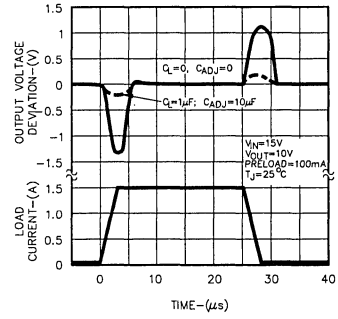


FIGURE 15.
LOAD TRANSIENT RESPONSE

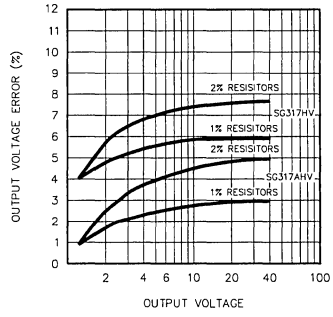
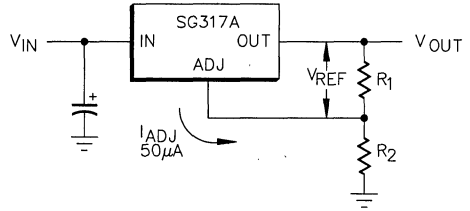


FIGURE 16.
OUTPUT VOLTAGE ERROR

APPLICATION INFORMATION

GENERAL

The SG117A develops a 1.25V reference voltage between the output and the adjustable terminal (see Figure 1). By placing a resistor, R_1 between these two terminals, a constant current is caused to flow through R_1 and down through R_2 to set the overall output voltage, Normally this current is the specified minimum load current of 5mA or 10mA.



$$V_{OUT} = V_{REF}\left(1+\frac{R_2}{R_1}\right)+I_{ADJ}R_2$$

FIGURE 17 - BASIC REGULATOR CIRCUIT

Because I_{ADJ} is very small and constant when compared with the current through R_1, it represents a small error and can usually be ignored.

It is easily seen from the above equation, that even if the resistors were of exact value, the accuracy of the output is limited by the accuracy of V_{REF}. Earlier adjustable regulators had a reference tolerance of ±4%. This tolerance is dangerously close to the ±5% supply tolerance required in many logic and analog systems. Further, many 1% resistors can drift 0.01%°C adding another 1% to the output voltage tolerance.

For example, using 2% resistors and ±4% tolerance for VREF, calculations will show that the expected range of a 5V regulator design would be $4.66V \le V_{OUT} \le 5.36V$ or approximately ±7%. If the same example were used for a 15V regulator, the expected tolerance would be ±8%. With these results most applications require some method of trimming, usually a trim pot. This solution is expensive and not conducive to volume production.

One of the enhancements of Silicon General's adjustable regulators over existing devices is tightened initial tolerance. This allows relatively inexpensive 1% or 2% film resistors to be used for R_1 and R_2 while setting output voltage within an acceptable tolerance range.

With a guaranteed 1% reference, a 5V power supply design, using ±2% resistors, would have a worse case manufacturing tolerance of ±4%. If 1% resistors were used, the tolerance would drop to ±2.5%. A plot of the worst case output voltage tolerance as a function of resistor tolerance is shown on the front page.

For convenience, a table of standard 1% resistor values is shown below.

Table of ½% and 1% Standard Resistance Values

1.00	1.47	2.15	3.16	4.64	6.81
1.02	1.50	2.21	3.24	4.75	6.98
1.05	1.54	2.26	3.32	4.87	7.15
1.07	1.58	2.32	3.40	4.99	7.32
1.10	1.62	2.37	3.48	5.11	7.50
1.13	1.65	2.43	3.57	5.23	7.68
1.15	1.69	2.49	3.65	5.36	7.87
1.18	1.74	2.55	3.74	5.49	8.06
1.21	1.78	2.61	3.83	5.62	8.25
1.24	1.82	2.67	3.92	5.76	8.45
1.27	1.87	2.74	4.02	5.90	8.66
1.30	1.91	2.80	4.12	6.04	8.87
1.33	1.96	2.87	4.22	6.19	9.09
1.37	2.00	2.94	4.32	6.34	9.31
1.40	2.05	3.01	4.42	6.49	9.53
1.43	2.10	3.09	4.53	6.65	9.76

Standard Resistance Values are obtained from the Decade Table by multiplying by multiples of 10. As an example:1.21 can represent 1.21Ω, 12.1Ω, 121Ω, 1.21KΩ etc.

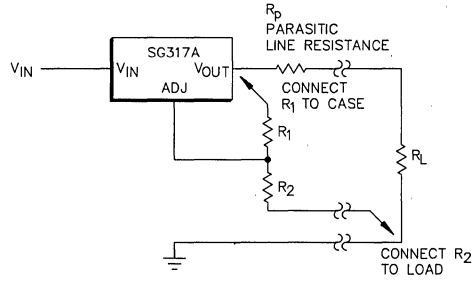
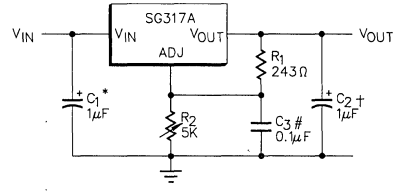


FIGURE 18 - CONNECTIONS FOR BEST LOAD REGULATION



+ Optional—improves transient response

$V_{OUT} = 1.25V\left(1+\frac{R_2}{R_1}\right)$

* Needed if device is far from filter capacitors

\# Needed if load current is mechanically switched

FIGURE 19 - 1.2V-25V ADJUSTABLE REGULATOR

APPLICATION INFORMATION (continued)

BYPASS CAPACITORS

Input bypassing using a 1μF tantalum or 25μF electrolytic is recommended when the input filter capacitors are more than 5 inches from the device. A 0.1μF bypass capacitor on the ADJUST pin is required if the load current varies by more than 1A/μsec. Improved ripple rejection (80dB) can be accomplished by adding a 10μF capacitor from the adjust pin to ground. For improved AC transient response and to prevent the possibility of oscillation due to unknown reactive load, a 1μF capacitor is also recommended at the output. Because of their low impedance at high frequencies, the best type of capacitor to use is solid tantalum.

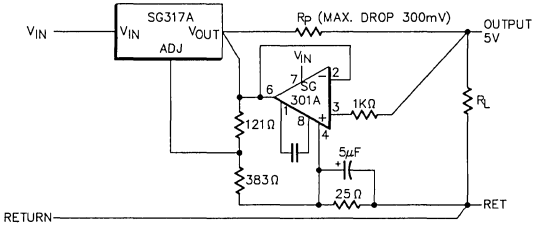
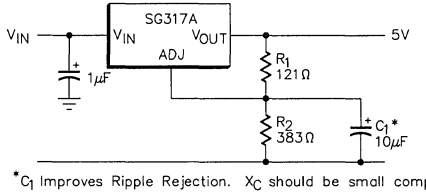


FIGURE 20 - REMOTE SENSING



*C_1 Improves Ripple Rejection. X_C should be small compared to R_2.

FIGURE 21 - IMPROVING RIPPLE REJECTION

LOAD REGULATION

Because the SG117A is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the wire connecting the regulator to the load. For the data sheet specification, regulation is measured at the bottom of the package. Negative side sensing is a true Kelvin connection, with the bottom of the output divider returned to the negative side of the load. Although it may not be immediately obvious, best load regulation is obtained when the top of the divider is connected directly to the case, not to the load. This is illustrated in Figure 18. If R_1 were connected to the load, the effective resistance between the regulator and the load would be

$$R_P X \left(\frac{R_2 + R_1}{R_1}\right), R_P = \text{Parasitic Line Resistance.}$$

Connected as shown, R_P is not multiplied by the divider ratio. R_P is about 0.004Ω per foot using 16 gauge wire. This translates to 4mV/ft. at 1A load current, so it is important to keep the positive lead between regulator and load as short as possible.

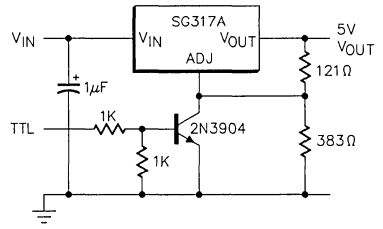


FIGURE 22 - 5V REGULATOR WITH SHUT DOWN

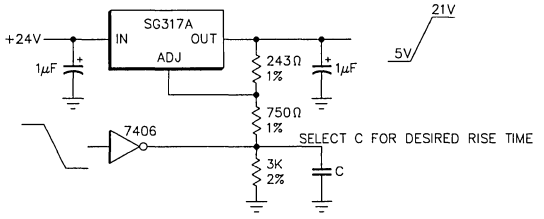


FIGURE 23 - 21V PROGRAMMING SUPPLY FOR UV PROM/EEPROM

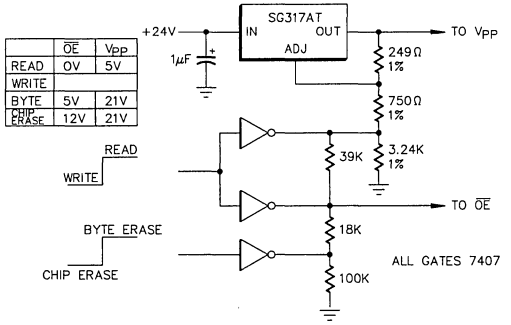


FIGURE 24 - 2816 EEPROM SUPPLY PROGRAMMER FOR READ/WRITE CONTROL

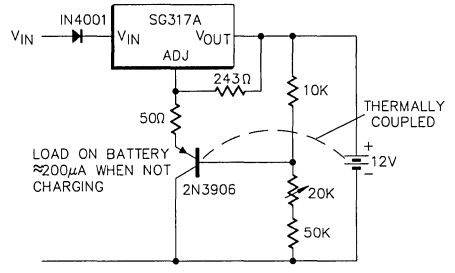
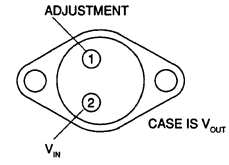
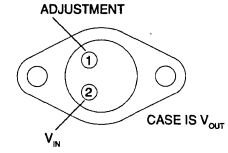
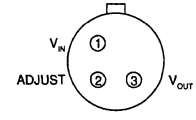
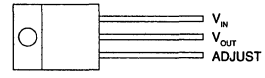
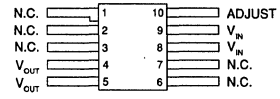
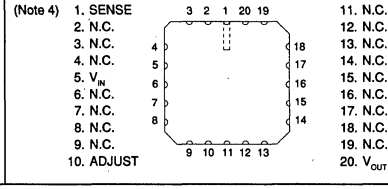


FIGURE 25 - TEMPERATURE COMPENSATED LEAD ACID BATTERY CHARGER

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
3-TERMINAL TO-3 METAL CAN K-PACKAGE	SG117AK/883B SG117AK SG217AK SG317AK SG117K/883B SG117K SG217K SG317K	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C -55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
3-TERMINAL TO-66 METAL CAN R-PACKAGE	SG117AR/883B SG117AR SG217AR SG317AR SG117R/883B SG117R SG217R SG317R	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C -55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
3-PIN TO-39 METAL CAN T-PACKAGE	SG117AT/883B SG117AT SG217AT SG317AT SG117T/883B SG117T SG217T SG317T	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C -55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
3-PIN HERMETIC TO-257 G-PACKAGE (Non-Isolated) 3-PIN HERMETIC TO-257 IG-PACKAGE (Isolated)	SG117AG/883B SG117AG SG117G/883B SG117G SG117AIG/883B SG117AIG SG117IG/883B SG117IG	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C	
10-PIN CERAMIC FLAT PACK F - PACKAGE	SG117AF/883B SG117AF SG117F/883B SG117F	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C	(Note 3) 
20-PIN CERAMIC (LCC) LEADLESS CHIP CARRIER L- PACKAGE	SG117AL/883B SG117AL SG117L/883B SG117L	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C	(Note 4) 

Note 1. Contact factory for JAN and DESC product availability.
2. All parts are viewed from the top.
3. Both inputs and outputs must be externally connected together at the device terminals.
4. For normal operation the SENSE pin must be externally connected to the load.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SG117AHV/SG217AHV/SG317AHV
SG117HV/SG217HV/SG317HV

1.5 AMP THREE TERMINAL ADJUSTABLE VOLTAGE REGULATOR

DESCRIPTION

The SG117AHV Series are 3-terminal positive adjustable voltage regulators which offer improved performance over earlier devices. A major feature of the SG117AHV is the output voltage tolerance is guaranteed at a maximum of ± 1%, allowing an overall power supply tolerance to be better than 3 % using inexpensive 1 % resistors. Line and load regulation performance has been improved as well. Additionally, the SG117AHV reference voltage is guaranteed not to exceed 2% when operating over the full load, line and power dissipation conditions. The SG117AHV adjustable regulators offer an improved solution for all positive voltage regulator requirements with load currents up to 1.5 amps.

For application information and characteristic curves see SG117A/117 data sheet.

FEATURES

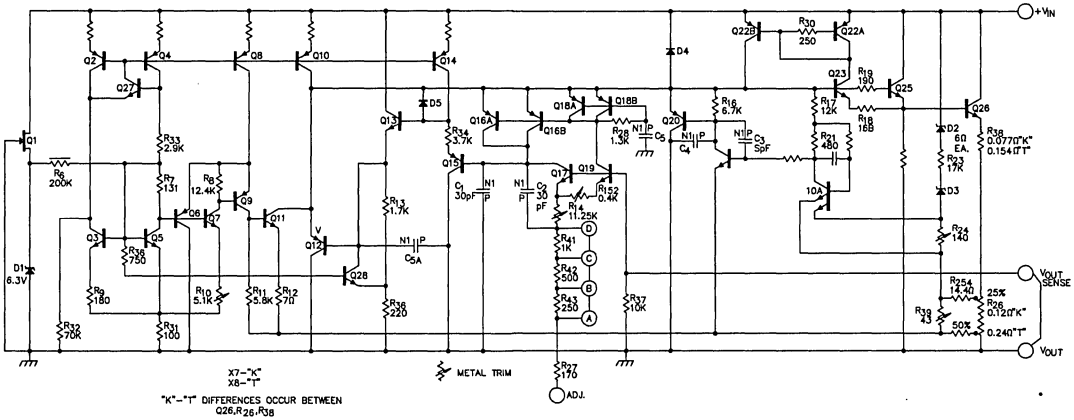
- **1 % output voltage tolerance**
- **0.01%/V line regulation**
- **0.3% load regulation**
- **Min. 1.5A output current**
- **Available in hermetic TO-220**

HIGH RELIABILITY FEATURES -SG117AHV/SG117HV

- **Available to MIL-STD-883**
- **SG level "S" processing available**

4

SCHEMATIC DIAGRAM



April 1990

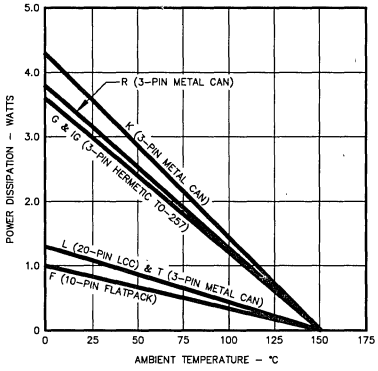
ABSOLUTE MAXIMUM RATINGS (Note 1)

Power Dissipation ..... Internally Limited
Input to Output Voltage Differential 60V
Storage Temperature Range ..... -65°C to 150°C

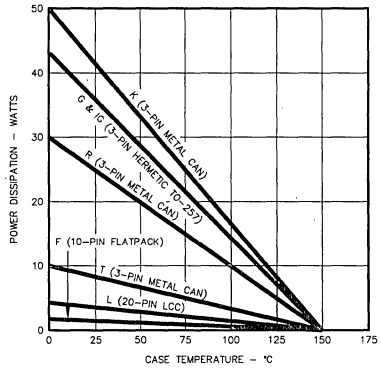
Operating Junction Temperature
Hermetic (K, R, T, F, L, G, IG-Packages) ..... 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2 & 3)

Input Voltage Range ..... (V_{OUT} + 3.5V) to 57V

Operating Junction Temperature Range
SG117AHV/SG117HV ..... -55°C to 150°C
SG217AHV/SG217HV ..... -25°C to 150°C
SG317AHV/SG317HV ..... 0°C to 125°C

Note 2. Range over which the device is functional.
Note 3. These ratings are applicable for junction temperatures of less than 150°C.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over full operating ambient temperatures for SG117AHV/SG117HV with -55°C ≤ T_A ≤ 150°C, SG217AHV/SG217HV with -25°C ≤ T_A ≤ 150°C, SG 317AHV/SG317HV with 0°C ≤ T_A ≤ 125°C, V_{IN} - V_{OUT} = 5.0V , and for I_{OUT} = 500mA (K, R, G and IG), and I_{OUT} = 100mA (T, F, and L packages). Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the T, F, and L packages, and 20W for the K, R, G, and IG packages. I_{MAX} is 1.5A for the K, R, G, and IG packages and 500mA for the T, F, and L packages. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG117AHV/ SG217AHV			SG117HV/ SG217HV			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Voltage	I_{OUT} = 10mA T_A = 25°C	1.238	1.250	1.262				V
	3V ≤ (V_{IN} - V_{OUT}) ≤ 60V, P ≤ P_{MAX}, 10mA ≤ I_{OUT} ≤ I_{MAX}	1.225	1.250	1.270	1.20	1.25	1.30	V
Line Regulation (Note 4)	3V ≤ (V_{IN} - V_{OUT}) ≤ 60V, I_L = 10mA							
	T_A = 25°C		0.005	0.01		0.01	0.02	%/V
	T_A = T_{MIN} to T_{MAX}		0.01	0.02		0.02	0.05	%/V
Load Regulation (Note 4)	10mA ≤ I_{OUT} ≤ I_{MAX}							
	V_{OUT} ≤ 5V, T_A = 25°C		5	15		5	15	mV
	V_{OUT} ≥ 5V, T_A = 25°C		0.1	0.3		0.1	0.3	%
	V_{OUT} ≤ 5V		20	50		20	50	mV
	V_{OUT} ≥ 5V		0.3	1		0.3	1	%
Thermal Regulation (Note 5)	T_A = 25°C, 20msec pulse		0.002	0.02		0.03	0.07	%/W
Ripple Rejection	V_{OUT} = 10V, f =120Hz							
	C_{ADJ} = 1µF, T_A = 25°C		65			65		dB
	C_{ADJ} = 10µF	66	80		66	80		dB
Adjust Pin Current	T_A = 25°C		50	100		50	100	µA
Adjust Pin Current Change	10mA ≤ I_{OUT} ≤ I_{MAX}, 2.5V ≤ (V_{IN} - V_{OUT}) ≤ 60V		0.2	5		0.2	5	µA

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG117AHV/ SG217AHV			SG117HV/ SG217HV			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Minimum Load Current	$(V_{IN} - V_{OUT}) = 60V$		3.5	7		3.5	7	mA
Current Limit	$(V_{IN} - V_{OUT}) \leq 15V$							
	K, P, R, G, IG Packages	1.5	2.2		1.5	2.2		A
	T, L, F Package	0.5	0.8		0.5	0.8		A
	$(V_{IN} - V_{OUT}) = 60V$, $T_J = 25°C$							
	K, P, R, G, IG Packages		0.1			0.1		A
	T, L, F Packages		0.03			0.03		A
Temperature Stability (Note 5)			1	2		1		%
Long Term Stability (Note 5)	$T_A = 125°C$, 1000 Hours		0.3	1		0.3	1	%
RMS Output Noise (% of V_{OUT})	$T_A = 25°C$, $10Hz \leq f \leq 10$ KHz (Note 5)		0.001			0.001		%

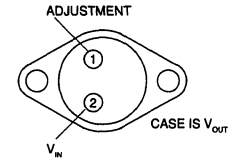
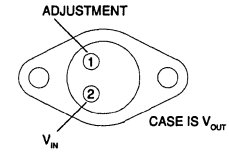
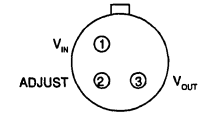
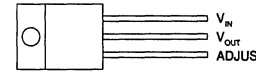
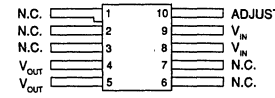
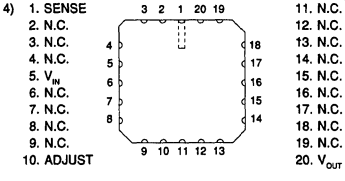
Parameter	Test Conditions	SG317AHV			SG317HV			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Voltage	$I_{OUT} = 10mA$ $T_A = 25°C$	1.238	1.250	1.262				V
	$3V \leq (V_{IN} - V_{OUT}) \leq 60V$, $P \leq P_{MAX}$,							
	$10mA \leq I_{OUT} \leq I_{MAX}$	1.225	1.250	1.270	1.20	1.25	1.30	V
Line Regulation (Note 4)	$3V \leq (V_{IN} - V_{OUT}) \leq 60V$, $I_L = 10mA$							
	$T_A = 25°C$		0.005	0.01		0.01	0.04	%/V
	$T_A = T_{MIN}$ to T_{MAX}		0.01	0.02		0.02	0.07	%/V
Load Regulation (Note 4)	$10mA \leq I_{OUT} \leq I_{MAX}$							
	$V_{OUT} \leq 5V$, $T_A = 25°C$		5	25		5	25	mV
	$V_{OUT} \geq 5V$, $T_A = 25°C$		0.1	0.5		0.1	0.5	%
	$V_{OUT} \leq 5V$		20	50		20	70	mV
	$V_{OUT} \geq 5V$		0.3	1		0.3	1.5	%
Thermal Regulation (Note 5)	$T_A = 25°C$, 20ms pulse		0.002	0.02		0.04	0.07	%/W
Ripple Rejection	$V_{OUT} = 10V$, f =120Hz							
	$C_{ADJ} = 1\mu F$, $T_A = 25°C$		65			65		dB
	$C_{ADJ} = 10\mu F$	66	80		66	80		dB
Adjust Pin Current	$T_A = 25°C$		50	100		50	100	µA
Adjust Pin Current Change	$10mA \leq I_{OUT} \leq I_{MAX}$, $2.5V \leq (V_{IN} - V_{OUT}) \leq 60V$		0.2	5		0.2	5	µA
Minimum Load Current	$(V_{IN} - V_{OUT}) = 60V$		3.5	12		3.5	12	mA
Current Limit	$(V_{IN} - V_{OUT}) \leq 15V$							
	K, P, R, G, IG Packages	1.5	2.2		1.5	2.2		A
	T, L, F Packages	0.5	0.8		0.5	0.8		A
	$(V_{IN} - V_{OUT}) = 60V$, $T_J = 25°C$							
	K, P, R, G, IG Packages		0.1			0.4		A
	T, L, F Packages		0.03			0.03		A
Temperature Stability (Note 5)			1	2		1		%
Long Term Stability (Note 5)	$T_A = 125°C$		0.3	1		0.3	1	%
RMS Output Noise (% of V_{OUT})	$T_A = 25°C$, $10Hz \leq f \leq 10KHz$ (Note 5)		0.001			0.001		%

Note 4. Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

Note 5. These parameters, although guaranteed, are not tested in production.

4

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
3-TERMINAL TO-3 METAL CAN K-PACKAGE	SG117AHVK/883B SG117AHVK SG217AHVK SG317AHVK SG117HVK/883B SG117HVK SG217HVK SG317HVK	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C -55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
3-TERMINAL TO-66 METAL CAN R-PACKAGE	SG117AHVR/883B SG117AHVR SG217AHVR SG317AHVR SG117HVR/883B SG117HVR SG217HVR SG317HVR	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C -55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
3-PIN TO-39 METAL CAN T-PACKAGE	SG117AHVT/883B SG117AHVT SG217AHVT SG317AHVT SG117HVT/883B SG117HVT SG217HVT SG317HVT	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C -55°C to 125C -55°C to 125°C -25°C to 85C 0°C to 70°C	
3-PIN HERMETIC TO-257 G-PACKAGE (Non-Isolated) 3-PIN HERMETIC TO-257 IG-PACKAGE (Isolated)	SG117AHVG/883B SG117AHVG SG117HVG/883B SG117HVG SG117AHVIG/883B SG117AHVIG SG117HVIG/883B SG117HVIG	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C	
10-PIN CERAMIC FLAT PACK F - PACKAGE	SG117AHVF/883B SG117AHVF SG117HVF/883B SG117HVF	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C	(Note 3) 
20-PIN CERAMIC (LCC) LEADLESS CHIP CARRIER L- PACKAGE	SG117AHVL/883B SG117AHVL SG117HVL/883B SG117HVL	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C	(Note 4) 

Note 1. Contact factory for JAN and DESC product availability.
2. All parts are viewed from the top.
3. Both inputs and outputs must be externally connected together at the device terminals.
4. For normal operation the SENSE pin must be externally connected to the load.

NEGATIVE FIXED VOLTAGE REGULATOR

DESCRIPTION

The SG120/320 series of negative regulators offer self-contained, fixed-voltage capability with up to 1.5A of load current. With a variety of output voltages and four package options this regulator series is an optimum complement to the SG7800A/ 7800/120/320 line of three terminal regulators.

All protective features of thermal shutdown, current limiting, and safe-area control have been designed into these units and since these regulators require only a single output capacitor or a capacitor and 5mA minimum load for satisfactory performance, ease of application is assured.

Although designed as fixed-voltage regulators, the output voltage can be increased through the use of a simple voltage divider. The low quiescent drain current of the device insures good regulation when this method is used, especially for the SG120 series. Utilizing an improved Bandgap reference design, problems have been eliminated that are normally associated with the zener diode references, such as drift in output voltage and large changes in the line and load regulation

These devices are available in TO-257 (hermetically sealed TO-220), both isolated and non-isolated), TO-3, TO-39 and TO-66 power packages as well as the plastic commercial power TO-220 package.

FEATURES

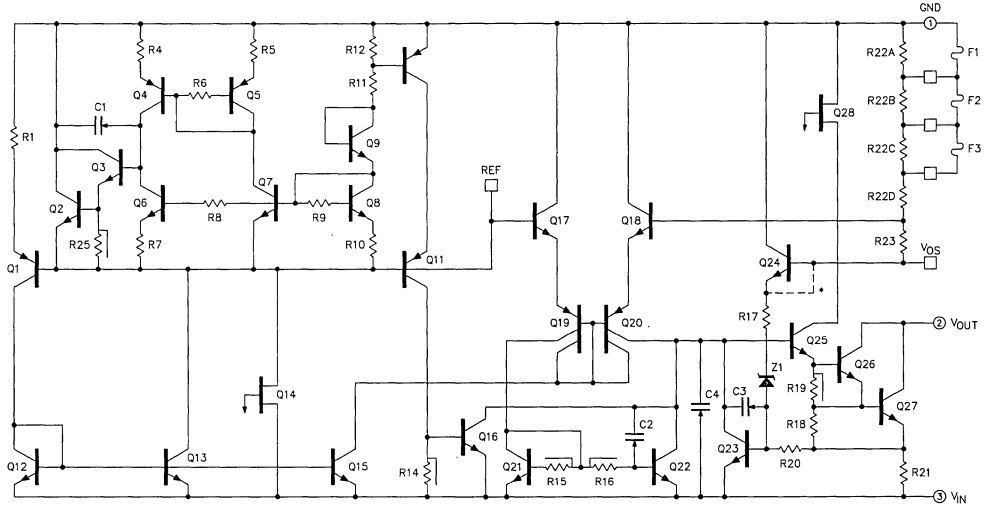
- **Output current to 1.5A**
- **Excellent line and load regulation**
- **Foldback current limiting**
- **Thermal overload protection**
- **Voltages available: -5V, -5.2V, -8V, -12V, -15V, -18V, -20V**
- **Contact factory for other voltage options**

HIGH RELIABILITY FEATURES - SG120

- ♦ **Available to MIL-STD - 883**
- ♦ **Radiation data available**
- ♦ **SG level "S" processing available**

4

SCHEMATIC DIAGRAM



* WIRE EXISTS IF 120 TYPE DEVICE.
WIRE DOES NOT EXIST IF 7900 TYPE DEVICE.
SELECTABLE BY EMITTER OPTION.

ABSOLUTE MAXIMUM RATINGS (Note 1)

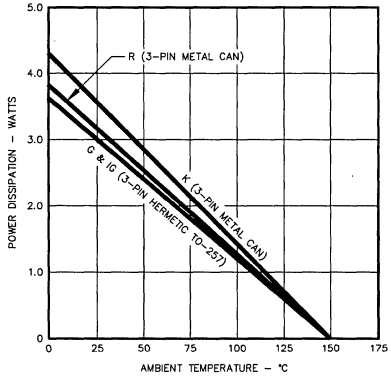
Device Output Voltage	Input Voltage	Input Voltage Differential (Output shorted to ground)
-5V	-35V	35V
-5.2V	-35V	35V
-8V	-35V	35V
-12V	-35V	35V
-15V	-40V	35V
-18V	-40V	35V
-20V	-40V	35V

Operating Junction Temperature
Hermetic (K, R, G, IG - Packages) ..... 150°C

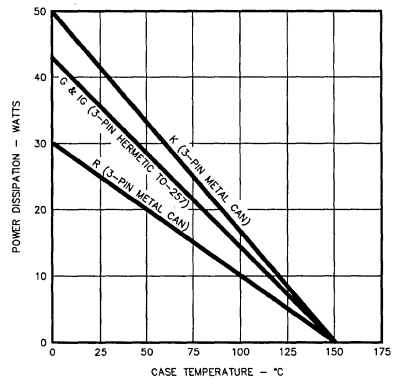
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Values beyond which damage may occur.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Operating Junction Temperature Range:
SG120 ..... -55°C to 150°C
SG320 ..... 0°C to 125°C

Note 2. Range over which the device is functional.

CHARACTERISTIC CURVES

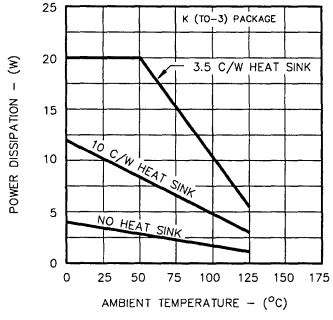


FIGURE 1.
MAXIMUM AVERAGE POWER DISSIPATION

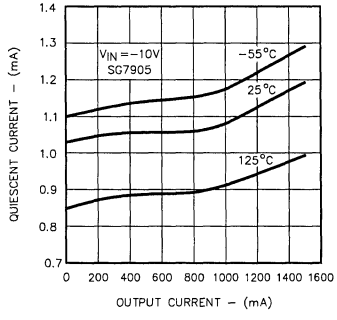


FIGURE 2.
QUIESCENT CURRENT VS. LOAD

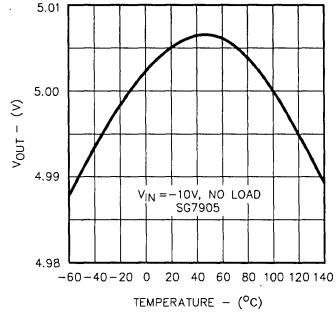


FIGURE 3.
TEMPERATURE COEFFICIENT

CHARACTERISTIC CURVES (continued)

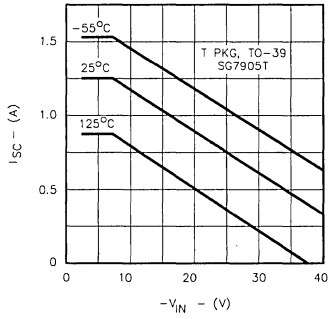


FIGURE 4.
SHORTCIRCUIT CURRENT VS. V_{IN}

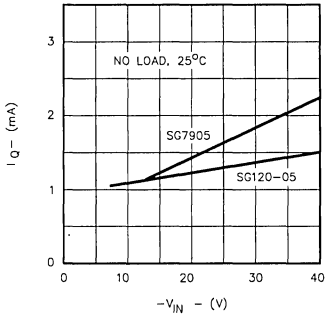


FIGURE 5.
QUIESCENT CURRENT VS. V_{IN}

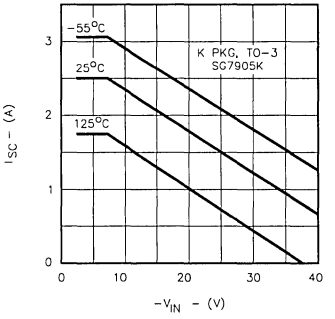


FIGURE 6.
SHORT CIRCUIT CURRENT VS. V_{IN}

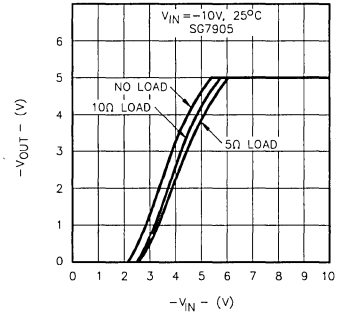


FIGURE 7.
DROPOUT CHARACTERISTICS

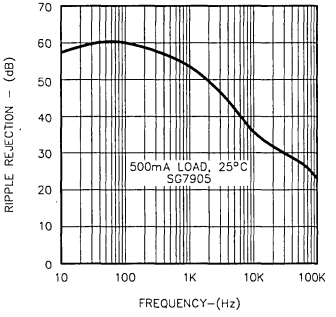


FIGURE 8.
RIPPLE REJECTION VS. FREQUENCY

APPLICATIONS

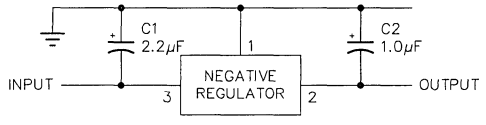


FIGURE 9 - FIXED OUTPUT REGULATOR

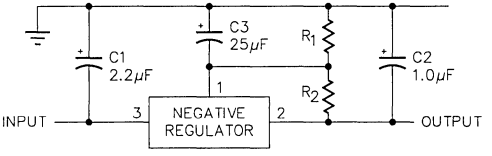


FIGURE 10 - CIRCUIT FOR INCREASING OUTPUT VOLTAGE

NOTE: 1. C1 is required only if regulator is separated from rectifier filter.
2. Both C1 and C2 should be low E.S.R. types such as solid tantalum. If aluminum electrolitics are used, at least 10 times values shown should be selected.
3. If large output capacities are used, the regulators must be protected from momentary input shorts. A high current diode

NOTE: C3 optional for improved transient response and ripple rejec-

$$V_{OUT} = V\,(REGULATOR)\frac{R_1 + R_2}{R_1} \qquad R_2 = \frac{V(REG)}{15mA}$$

ELECTRICAL SPECIFICATIONS (Note 1)

SG120-05/SG320-05

(Unless otherwise specified, these specifications apply over full operating ambient temperatures for SG120-05 with $-55°C \le T_A \le 150°C$, SG320-05 with $0°C \le T_A \le 125°C$, and $V_{IN} = -10V$, $I_O = 5mA$, $C_{IN} = 2\mu F$, $C_{OUT} = 1.0\mu F$. Low duty cycle pulse testing techniques are used which maintains junction and case temperature equal to the ambient temperature.)

Parameter	Test Conditions	SG120-05			SG320-05			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	$T_J = 25°C$	-4.9	-5.0	-5.1	-4.8	-5.0	-5.2	V
Line Regulation (Note 1)	$V_{IN} = -7V$ to $-25V$, $T_J = 25°C$		10	25		10	40	mV
Load Regulation (Note 1)	Power Pkgs: $I_O = 5mA$ to $1.5A$, $T_J = 25°C$		50	75		60	100	mV
	T - Pkg: $I_O = 5mA$ to $500mA$, $T_J = 25°C$		30	50		30	50	mV
Total Output Voltage	$V_{IN} = -7.5V$ to $-25V$							
Tolerance	Power Pkgs: $I_O = 5mA$ to $1.5A$, $P \le 20W$	-4.8	-5.0	-5.2	-4.75	-5.00	-5.25	V
	T - Pkg: $I_O = 5mA$ to $500mA$, $P \le 2W$	-4.8	-5.0	-5.2	-4.75	-5.00	-5.25	V
Quiescent Current	$V_{IN} = -7V$ to $-25V$			2			2	mA
Quiescent Current Change	With Line: $V_{IN} = -7V$ to $-25V$, $T_J = 25°C$			0.4			0.4	mA
	With Load: $T_J = 25°C$							
	Power Pkgs: $I_O = 5mA$ to $1.5A$			0.4			0.4	mA
	T - Pkg: $I_O = 5mA$ to $500mA$			0.4			0.4	mA
Dropout Voltage	$\Delta V_O = 100mV$, $T_J = 25°C$							
	Power Pkgs: $I_O = 1.0A$, T - Pkg: $I_O = 500mA$		1.1	2.3		1.1	2.3	V
Peak Output Current	Power Pkgs: $T_J = 25°C$	1.5		3.3	1.5		3.3	A
	T - Pkg: $T_J = 25°C$	0.5		1.4			1.4	A
Short Circuit Current	Power Pkgs: $V_{IN} = -35V$, $T_J = 25°C$			1.2			1.2	A
	T - Pkg: $V_{IN} = -35V$, $T_J = 25°C$			0.6			0.6	A
Ripple Rejection	$\Delta V_{IN} = 10V$, $f = 120Hz$, $T_J = 25°C$	54			54			dB
Output Noise Voltage (rms)	$f = 10Hz$ to $100KHz$ (Note 2)		25	80		25	80	μV/V
Long Term Stability	1000hrs. at $T_J = 125°C$		20			20		mV
Thermal Shutdown	$I_O = 5mA$		175			175		°C

SG120-5.2/SG320-5.2

(Unless otherwise specified, these specifications apply over full operating ambient temperatures for SG120-5.2 with $-55°C \le T_A \le 150°C$, SG320-5.2 with $0°C \le T_A \le 125°C$, and $V_{IN} = -10V$, $I_O = 5mA$, $C_{IN} = 2\mu F$, $C_{OUT} = 1.0\mu F$. Low duty cycle pulse testing techniques are used which maintains junction and case temperature equal to the ambient temperature.)

Parameter	Test Conditions	SG120-5.2			SG320-5.2			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	$T_J = 25°C$	-5.1	-5.2	-5.3	-5.0	-5.2	-5.4	V
Line Regulation (Note 1)	$V_{IN} = -7.2V$ to $-25V$, $T_J = 25°C$		15	25		10	40	mV
Load Regulation (Note 1)	Power Pkgs: $I_O = 5mA$ to $1.5A$, $T_J = 25°C$		50	75		60	100	mV
	T - Pkg: $I_O = 5mA$ to $500mA$, $T_J = 25°C$		30	50		30	50	mV
Total Output Voltage	$V_{IN} = -7.7V$ to $-25V$							
Tolerance	Power Pkgs: $I_O = 5mA$ to $1.5A$, $P \le 20W$	-5.0	-5.2	-5.4	-4.95	-5.20	-5.45	V
	T - Pkg: $I_O = 5mA$ to $500mA$, $P \le 2W$	-5.0	-5.2	-5.4	-4.95	-5.20	-5.45	V
Quiescent Current	$V_{IN} = -7.2V$ to $-25V$			2			2	mA
Quiescent Current Change	With Line: $V_{IN} = -7.2V$ to $-25V$, $T_J = 25°C$			0.4			0.4	mA
	With Load: $T_J = 25°C$							
	Power Pkgs: $I_O = 5mA$ to $1.5A$			0.4			0.4	mA
	T - Pkg: $I_O = 5mA$ to $500mA$			0.4			0.4	mA
Dropout Voltage	$\Delta V_O = 100mV$, $T_J = 25°C$							
	Power Pkgs: $I_O = 1.5A$, T - Pkg: $I_O = 500mA$		1.1	2.3		1.1	2.3	V
Peak Output Current	Power Pkgs: $T_J = 25°C$	1.5		3.3	1.5		3.3	A
	T - Pkg: $T_J = 25°C$	0.5		1.4	0.5		1.4	A
Short Circuit Current	Power Pkgs: $V_{IN} = -35V$, $T_J = 25°C$			1.2			1.2	A
	T - Pkg: $V_{IN} = -35V$, $T_J = 25°C$			0.6			0.6	A
Ripple Rejection	$\Delta V_{IN} = 10V$, $f = 120Hz$, $T_J = 25°C$	54			54			dB
Output Noise Voltage (rms)	$f = 10Hz$ to $100KHz$ (Note 2)		25	80		25	80	μV/V
Long Term Stability	1000hrs. at $T_J = 125°C$		20			20		mV
Thermal Shutdown	$I_O = 5mA$		175			175		°C

Note 1. All regulation tests are made at constant junction temperature with low duty cycle testing.
2. This test is guaranteed but is not tested in production.

ELECTRICAL SPECIFICATIONS (Note 1)

SG120-08/SG320-08

(Unless otherwise specified, these specifications apply over full operating ambient temperatures for SG120-08 with -55°C ≤ T_A ≤ 150°C, SG320-08 with 0°C ≤ T_A ≤ 125°C, and V_{IN} = -14V, I_O = 5mA, C_{IN} = 1.0µF, C_{OUT} = 1.0µF. Low duty cycle pulse testing techniques are used which maintains junction and case temperature equal to the ambient temperature.)

Parameter	Test Conditions	SG120-8			SG320-8			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	-7.8	-8.0	-8.2	-7.7	-8.0	-8.3	V
Line Regulation (Note 1)	V_{IN} = -10.5V to -25V, T_J = 25°C		10	25		10	40	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		20	80		20	100	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		10	25		10	40	mV
Total Output Voltage	V_{IN} = -10.5V to -25V							
Tolerance	Power Pkgs: I_O = 5mA to 1.5A, P ≤ 20W	-7.65	-8.00	-8.35	-7.6	-8.0	-8.4	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	-7.65	-8.00	-8.35	-7.6	-8.0	-8.4	V
Quiescent Current	V_{IN} = -10.5V to -25V			2			2	mA
Quiescent Current Change	With Line: V_{IN} = -10.5V to -25V, T_J = 25°C			0.4			0.4	mA
	With Load: T_J = 25°C							
	Power Pkgs: I_O = 5mA to 1.5A			0.4			0.4	mA
	T - Pkg: I_O = 5mA to 500mA			0.4			0.4	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		1.1	2.3		1.1	2.3	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5		3.3	1.5		3.3	A
	T - Pkg: T_J = 25°C	0.5		1.4	0.5		1.4	A
Short Circuit Current	Power Pkgs: V_{IN} = -35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = -35V, T_J = 25°C			0.6			0.6	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	54			54			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)		25	80		25	80	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		32			32		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

SG120-12/SG320-12

(Unless otherwise specified, these specifications apply over full operating ambient temperatures for SG120-12 with -55°C ≤ T_A ≤ 150°C, SG320-12 with 0°C ≤ T_A ≤ 125°C, and V_{IN} = -17V, I_O = 5mA, C_{IN} = 2.0µF, C_{OUT} = 1.0µF. Low duty cycle pulse testing techniques are used which maintains junction and case temperature equal to the ambient temperature.)

Parameter	Test Conditions	SG120-12			SG320-12			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	-11.7	-12.0	-12.3	-11.6	-12.0	-12.4	V
Line Regulation (Note 1)	V_{IN} = -14V to -32V, T_J = 25°C		4	10		4	20	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.0A, T_J = 25°C		30	80		30	80	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		10	25		10	40	mV
Total Output Voltage	V_{IN} = -14.5V to -32V							
Tolerance	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	-11.5	-12.0	-12.5	-11.4	-12.0	-12.4	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	-11.5	-12.0	-12.5	-11.4	-12.0	-12.4	V
Quiescent Current	V_{IN} = -14V to -32V		2	4		2	4	mA
Quiescent Current Change	With Line: V_{IN} = -14V to -32V, T_J = 25°C			0.4			0.4	mA
	With Load: T_J = 25°C							
	Power Pkgs: I_O = 5mA to 1.0A			0.4			0.4	mA
	T - Pkg: I_O = 5mA to 500mA			0.4			0.4	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		1.1	2.3		1.1	2.3	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5		3.3	1.5		3.3	A
	T - Pkg: T_J = 25°C	0.5		1.4	0.5		1.4	A
Short Circuit Current	Power Pkgs: V_{IN} = -35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = -35V, T_J = 25°C			0.6			0.6	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	56			56			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)		25	80		25	80	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		48			48		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

Note 1. All regulation tests are made at constant junction temperature with low duty cycle testing.
2. This test is guaranteed but is not tested in production.

ELECTRICAL SPECIFICATIONS (Note 1)

SG120-15/SG320-15

(Unless otherwise specified, these specifications apply over full operating ambient temperatures for SG120-15 with -55°C ≤ T_A ≤ 150°C, SG320-15 with 0°C ≤ T_A ≤ 125°C, and V_{IN} = -20V, I_O = 5mA, C_{IN} = 2.0µF, C_{OUT} = 1.0µF. Low duty cycle pulse testing techniques are used which maintains junction and case temperature equal to the ambient temperature.)

Parameter	Test Conditions	SG120-15			SG320-15			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	-14.7	-15.0	-15.3	-14.6	-15.0	-15.4	V
Line Regulation (Note 1)	V_{IN} = -17V to -35V, T_J = 25°C		5	10		5	20	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.0A, T_J = 25°C		30	80		30	80	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		10	25		10	40	mV
Total Output Voltage	V_{IN} = -17.5V to -35V							
Tolerance	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	-14.5	-15.0	-15.5	-14.4	-15.0	-15.6	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	-14.5	-15.0	-15.5	-14.4	-15.0	-15.6	V
Quiescent Current	V_{IN} = -17V to -35V		2	4		2	4	mA
Quiescent Current Change	With Line: V_{IN} = -17V to -35V, T_J = 25°C			0.4			0.4	mA
	With Load: T_J = 25°C							
	Power Pkgs: I_O = 5mA to 1.0A			0.4			0.4	mA
	T - Pkg: I_O = 5mA to 500mA			0.4			0.4	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		1.1	2.3		1.1	2.3	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5		3.3	1.5		3.3	A
	T - Pkg: T_J = 25°C	0.5		1.4	0.5		1.4	A
Short Circuit Current	Power Pkgs: V_{IN} = -35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = -35V, T_J = 25°C			0.6			0.6	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	56			56			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)		25	80		25	80	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		60			60		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

SG120-18/SG320-18

(Unless otherwise specified, these specifications apply over full operating ambient temperatures for SG120-18 with -55°C ≤ T_A ≤ 150°C, SG320-18 with 0°C ≤ T_A ≤ 125°C, and V_{IN} = -27V, I_O = 5mA, C_{IN} = 2.0µF, C_{OUT} = 1.0µF. Low duty cycle pulse testing techniques are used which maintains junction and case temperature equal to the ambient temperature.)

Parameter	Test Conditions	SG120-18			SG320-18			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	-17.6	-18.0	-18.4	-17.4	-18.0	-18.6	V
Line Regulation (Note 1)	V_{IN} = -21V to -33V, T_J = 25°C		5	10		5	20	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.0A, T_J = 25°C		30	80		30	80	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		10	25		10	40	mV
Total Output Voltage	V_{IN} = -22V to -33V							
Tolerance	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	-17.4	-18.0	-18.6	-17.1	-18.0	-18.9	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	-17.4	-18.0	-18.6	-17.1	-18.0	-18.9	V
Quiescent Current	V_{IN} = -21V to -33V		2	4		2	4	mA
Quiescent Current Change	With Line: V_{IN} = -21V to -33V, T_J = 25°C			0.4			0.4	mA
	With Load: T_J = 25°C							
	Power Pkgs: I_O = 5mA to 1.0A			0.4			0.4	mA
	T - Pkg: I_O = 5mA to 500mA			0.4			0.4	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		1.1	2.3		1.1	2.3	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5		3.3	1.5		3.3	A
	T - Pkg: T_J = 25°C	0.5		1.4	0.5		1.4	A
Short Circuit Current	Power Pkgs: V_{IN} = -35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = -35V, T_J = 25°C			0.6			0.6	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	56			56			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)		25			80		µV/V
Long Term Stability	1000hrs. at T_J = 125°C		72			72		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

Note 1. All regulation tests are made at constant junction temperature with low duty cycle testing.
2. This test is guaranteed but is not tested in production.

ELECTRICAL SPECIFICATIONS (Note 1)

SG120-20/SG320-20

(Unless otherwise specified, these specifications apply over full operating ambient temperatures for SG120-20 with $-55°C \le T_A \le 150°C$, SG320-20 with $0°C \le T_A \le 125°C$, and $V_{IN} = -29V$, $I_O = 5mA$, $C_{IN} = 2.0\mu F$, $C_{OUT} = 1.0\mu F$. Low duty cycle pulse testing techniques are used which maintains junction and case temperature equal to the ambient temperature.)

Parameter	Test Conditions	SG120-20			SG320-20			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	$T_J = 25°C$	-19.5	-20.0	-20.5	-19.2	-20.0	-20.8	V
Line Regulation (Note 1)	$V_{IN} = -23V$ to $-35V$, $T_J = 25°C$		5	10		5	20	mV
Load Regulation (Note 1)	Power Pkgs: $I_O = 5mA$ to $1.0A$, $T_J = 25°C$		30	80		30	80	mV
	T - Pkg: $I_O = 5mA$ to $500mA$, $T_J = 25°C$		10	25		10	25	mV
Total Output Voltage	$V_{IN} = -24V$ to $-35V$							
Tolerance	Power Pkgs: $I_O = 5mA$ to $1.0A$, $P \le 20W$	-19.3	-20.0	-20.7	-19.0	-20.0	-21.0	V
	T - Pkg: $I_O = 5mA$ to $500mA$, $P \le 2W$	-19.3	-20.0	-20.7	-19.0	-20.0	-21.0	V
Quiescent Current	$V_{IN} = -23V$ to $-35V$		2	4		2	4	mA
Quiescent Current Change	With Line: $V_{IN} = -23V$ to $-35V$, $T_J = 25°C$			0.4			0.4	mA
	With Load: $T_J = 25°C$							
	Power Pkgs: $I_O = 5mA$ to $1.0A$			0.4			0.4	mA
	T - Pkg: $I_O = 5mA$ to $500mA$			0.4			0.4	mA
Dropout Voltage	$\Delta V_O = 100mV$, $T_J = 25°C$							
	Power Pkgs: $I_O = 1.0A$, T - Pkg: $I_O = 500mA$		1.1	2.3		1.1	2.3	V
Peak Output Current	Power Pkgs: $T_J = 25°C$	1.5		3.3	1.5		3.3	A
	T - Pkg: $T_J = 25°C$	0.5		1.4	0.5		1.4	A
Short Circuit Current	Power Pkgs: $V_{IN} = -35V$, $T_J = 25°C$			1.2			1.2	A
	T - Pkg: $V_{IN} = -35V$, $T_J = 25°C$			0.6			0.6	A
Ripple Rejection	$\Delta V_{IN} = 10V$, $f = 120Hz$, $T_J = 25°C$	56			56			dB
Output Noise Voltage (rms)	$f = 10Hz$ to $100KHz$ (Note 2)		25	80		25	80	μV/V
Long Term Stability	1000hrs. at $T_J = 125°C$		80			80		mV
Thermal Shutdown	$I_O = 5mA$		175			175		°C

Note 1. All regulation tests are made at constant junction temperature with low duty cycle testing.
2. This test is guaranteed but is not tested in production.

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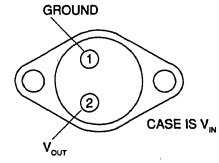
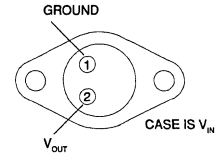
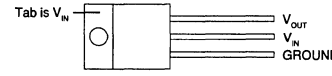
CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
3-TERMINAL TO-3 METAL CAN K-PACKAGE	SG120-XXK/883B SG120-XXK SG320-XXK	-55°C to 125°C -55°C to 125°C 0°C to 70°C	
3-TERMINAL TO-66 METAL CAN R-PACKAGE	SG120-XXR/883B SG120-XXR SG320-XXR	-55°C to 125°C -55°C to 125°C 0°C to 70°C	
3-PIN HERMETIC TO-257 G-PACKAGE (Non-Isolated) 3-PIN HERMETIC TO-257 IG-PACKAGE (Isolated)	SG120-XXG/883B SG120-XXG SG120-XXIG/883B SG120-XXIG	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availability.
2. All parts are viewed from the top.
3. "XX" to be replaced by output voltage of specific fixed regulator.
4. Some products will be available in leadless chip carrier (LCC) and hermetic flat pack (F). Consult factory for price and availability

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SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SG137A/SG237A/SG337A
SG137/SG237/SG337

1.5 AMP NEGATIVE ADJUSTABLE REGULATOR

DESCRIPTION

The SG137A family of negative adjustable regulators will deliver up to 1.5A output current over an output voltage range of -1.2V to -37V. Silicon General has made significant improvements in these regulators compared to previous devices, such as better line and load regulation, and a maximum output voltage error of 1%. The SG137 family uses the same chip design and guarantees maximum output voltage error of ±2%.

Every effort has been made to make these devices easy to use and difficult to damage. Internal current and power limiting coupled with true thermal limiting prevents device damage due to overloads or shorts even if the regulator is not fastened to a heat sink.

The SG137A/137 family of products are ideal complements to the SG117A/117 adjustable positive regulators.

FEATURES

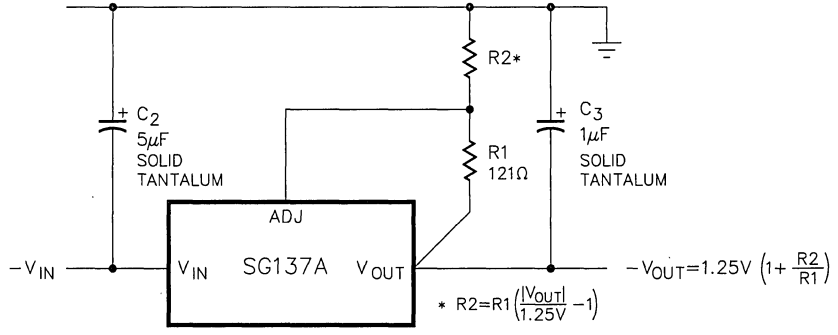
- **1 % output voltage tolerance**
- **0.01%/V line regulation**
- **0.5% load regulation**
- **0.02%/W thermal regulation**
- **Available in hermetic TO-220**

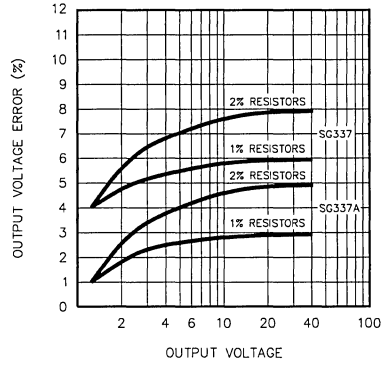
HIGH RELIABILITY FEATURES -SG137A/SG137

- **Available to MIL-STD-883 and DESC SMD**
- **Scheduled for MIL-M38510 QPL listing**
- **SG level "S" processing available**

4

BLOCK DIAGRAM





April 1990

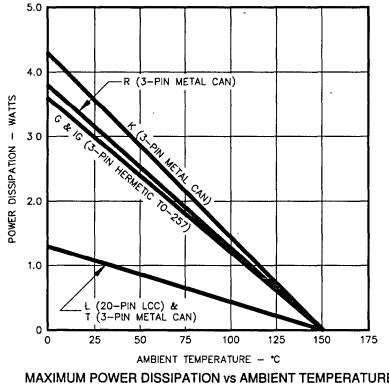
ABSOLUTE MAXIMUM RATINGS (Note 1)

Power Dissipation ..... Internally Limited
Input to Output Voltage Differential 40V
Storage Temperature Range ..... -65°C to 150°C

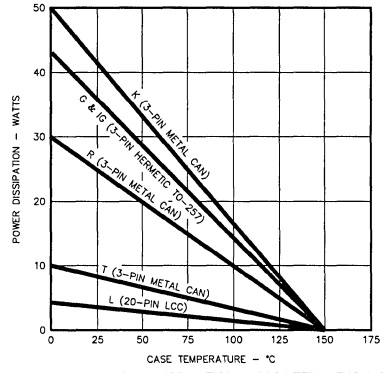
Operating Junction Temperature
Hermetic (K, R, T, L, G, IG-Packages) ..... 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2 & 3)

Input Voltage Range ..... $-(V_{OUT} + 3.5V)$ to -36V

Operating Junction Temperature Range
SG137A/SG137 ..... -55°C to 150°C
SG237A/SG237 ..... -25°C to 150°C
SG337A/SG337 ..... 0°C to 125°C

Note 2. Range over which the device is functional.
Note 3. These ratings are applicable for junction temperatures of less than 135°C.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over full operating ambient temperatures for SG137A/SG137 with $-55°C \le T_A \le 150°C$, SG237A/SG237 with $-25°C \le T_A \le 150°C$, SG337A/SG337 with $0°C \le T_A \le 125°C$, $|V_{IN} - V_{OUT}| = 5.0V$, and for $I_{OUT} = 500mA$ (K, R, G, and IG power packages) and $I_{OUT} = 100mA$ (T, F, and L packages). Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the T, F and L packages, and 20W for the K, R, G, and IG packages. I_{MAX} is 1.5A for the K, R, G, and IG packages and 0.5A for the T, F and L packages. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG137A/SG237A			SG137/SG237			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Voltage	$I_{OUT} = 10mA$, $T_A = 25°C$	-1.238	-1.250	-1.262	-1.225	-1.250	-1.275	V
	$3V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$, $10mA \le I_{OUT} \le I_{MAX}$	-1.220	-1.250	-1.280	-1.200	-1.250	-1.300	V
Line Regulation (Note 4)	$3V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$, $I_{OUT} \le I_{MAX}$ $T_A = 25°C$		0.005	0.01		0.01	0.02	%/V
Load Regulation (Note 4)	$10mA \le I_{OUT} \le I_{MAX}$							
	$\lvert V_{OUT} \rvert \le 5V$, $T_A = 25°C$		5	25		15	25	mV
	$\lvert V_{OUT} \rvert \ge 5V$, $T_A = 25°C$		0.1	0.5		0.3	0.5	%
	$\lvert V_{OUT} \rvert \le 5V$		10	50		20	50	mV
	$\lvert V_{OUT} \rvert \ge 5V$		0.2	1.0		0.3	1.0	%
Thermal Regulation (Note 5)	$T_A = 25°C$, 10ms pulse		0.002	0.02		0.002	0.02	%/W
Ripple Rejection	$V_{OUT} = -10V$, f =120Hz							
	$C_{ADJ} = 0$, $T_A = 25°C$	60	66		60			dB
	$C_{ADJ} = 10\mu F$	70	80		66	77		dB
Adjust Pin Current	$T_A = 25°C$		65	100		65	100	µA
Adjust Pin Current Change	$3V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$		1.0	5		2	5	µA
	$10mA \le I_{OUT} \le I_{MAX}$		0.2	2		0.5	5	µA

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG137A/SG237A			SG137/SG237			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Minimum Load Current	$\|V_{IN} - V_{OUT}\| \le 40V$		2.5	5.0		2.5	5.0	mA
	$\|V_{IN} - V_{OUT}\| \le 10V$		1.2	3		1.2	3.0	mA
Current Limit	$\|V_{IN} - V_{OUT}\| \le 15V$							
	K, P, R, G, IG Packages	1.5	2.2	3.2	1.5	2.2		A
	T, L, Packages	0.5	0.8	1.5	0.5	0.8		A
	$\|V_{IN} - V_{OUT}\| \le 40V$, $T_J = 25°C$							
	K, P, R, G, IG Packages	0.24	0.4	1.0	0.24	0.4		A
	T, L, Packages	0.15	0.25	0.5	0.15	0.25		A
Temperature Stability (Note 5)			0.6	1.5		0.6		%
Long Term Stability (Note 5)	$T_A = 125°C$, 1000 Hours		0.3	1.0		0.3	1.0	%
RMS Output Noise (% of V_{OUT})	$T_A = 25°C$, $10Hz \le f \le 10$ KHz (Note 5)		0.003			0.003		%

Parameter	Test Conditions	SG337A			SG337			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Voltage	$I_{OUT} = 10mA$, $T_A = 25°C$	-1.238	-1.250	-1.262	-1.213	-1.250	-1.287	V
	$3V \le \|V_{IN} - V_{OUT}\| \le 40V$, $10mA \le I_{OUT} \le I_{MAX}$	-1.220	-1.250	-1.280	-1.200	-1.250	-1.300	V
Line Regulation (Note 4)	$3V \le \|V_{IN} - V_{OUT}\| \le 40V$, $I_{OUT} \le I_{MAX}$							
	$T_A = 25°C$		0.005	0.01		0.01	0.04	%/V
Load Regulation (Note 4)	$10mA \le I_{OUT} \le I_{MAX}$							
	$\|V_{OUT}\| \le 5V$, $T_A = 25°C$		5	25		15	50	mV
	$\|V_{OUT}\| \ge 5V$, $T_A = 25°C$		0.1	0.5		0.3	1.0	%
	$\|V_{OUT}\| \le 5V$		10	50		20	70	mV
	$\|V_{OUT}\| \ge 5V$		0.2	1.0		0.3	1.5	%
Thermal Regulation (Note 5)	$T_A = 25°C$, 10ms pulse		0.002	0.02		0.003	0.04	%/W
Ripple Rejection	$V_{OUT} = -10V$, f =120Hz							
	$C_{ADJ} = 0$, $T_A = 25°C$	60	66			60		dB
	$C_{ADJ} = 10\mu F$	70	80		66	77		dB
Adjust Pin Current	$T_A = 25°C$		65	100		65	100	µA
Adjust Pin Current Change	$3V \le \|V_{IN} - V_{OUT}\| \le 40V$		1.0	5		2	5	µA
	$10mA \le I_{OUT} \le I_{MAX}$		0.2	2		0.5	5	µA
Minimum Load Current	$\|V_{IN} - V_{OUT}\| \le 40V$		2.5	5		2.5	10	mA
	$\|V_{IN} - V_{OUT}\| \le 10V$		1.2	3		1	6	mA
Current Limit	$\|V_{IN} - V_{OUT}\| \le 15V$							
	K, P, R, G, IG-Packages	1.5	2.2	3.5	1.5	2.2		A
	T, L-Packages	0.5	0.8	1.5	0.5	0.8		A
	$\|V_{IN} - V_{OUT}\| \le 40V$, $T_J = 25°C$							
	K, P, R, G, IG- Packages	0.24	0.5	1.0	0.15	0.4		A
	T, L-Packages	0.15	0.25	0.5	0.10	0.17		A
Temperature Stability (Note 5)			0.6	1.5		0.6		%
Long Term Stability (Note 5)	$T_A = 125°C$, 1000hr		0.3	1.0		0.3	1.0	%
RMS Output Noise (% of V_{OUT})	$T_A = 25°C$, $10Hz \le f \le 10KHz$ (Note 5)		0.003			0.003		%

Note 4. Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

Note 5. These parameters, although guaranteed, are not tested in production.

4

CHARACTERISTIC CURVES

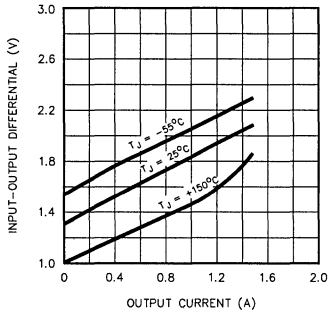


FIGURE 1.
INPUT/OUTPUT DIFFERENTIAL
VS. OUTPUT CURRENT

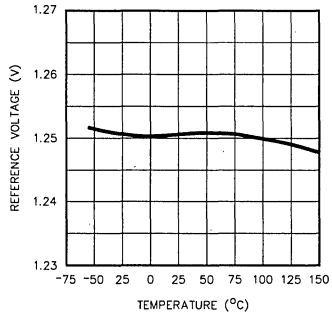


FIGURE 2.
REFERENCE VOLTAGE VS. TEMPERATURE

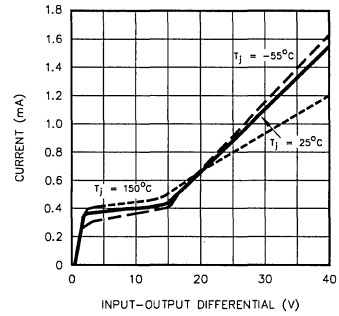


FIGURE 3.
CURRENT VS. INPUT/OUTPUT DIFFERENTIAL

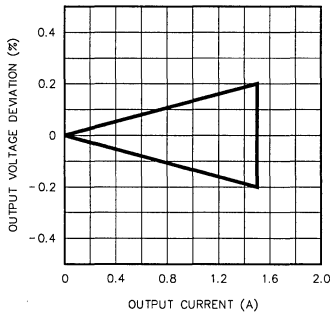


FIGURE 4. *
OUTPUT VOLTAGE DEVIATION
VS. OUTPUT CURRENT

* The SG137A has load regulation compensation which makes the typical unit read close to zero. This band represents the typical production spread.

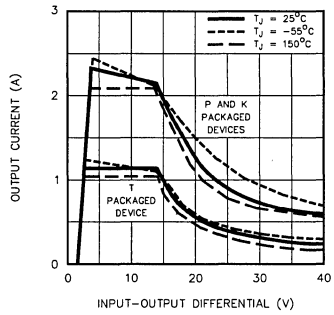


FIGURE 5.
INPUT/OUTPUT DIFFERENTIAL
VS. OUTPUT CURRENT

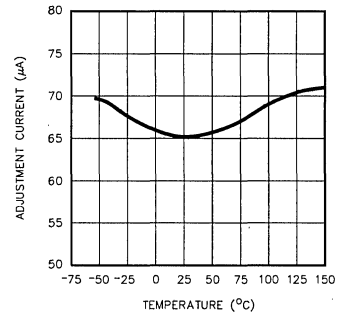


FIGURE 6.
ADJUSTMENT CURRENT VS. TEMPERATURE

APPLICATION INFORMATION

OUTPUT VOLTAGE

The output voltage is determined by two external resistors, R_1 & R_2(see Figure 7).

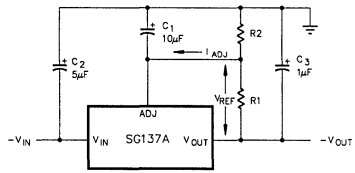


FIGURE 7

The exact formula for the output voltage is:

$$V_{OUT} = V_{REF}\left(\frac{R_2 + R_1}{R_1}\right) + I_{ADJ}(R_2)$$

Where: V_{REF} =Reference Voltage, I_{ADJ} = Adjustment Pin Current. In most applications, the second term is small enough to be ignored, typically about 0.5% of V_{OUT}. In more critical applications, the exact formula should be used, with I_{ADJ} equal to 65µA. Solving for R_2 yields:

$$R_2 = \frac{V_{OUT} - V_{REF}}{\frac{V_{REF}}{R_1} + I_{ADJ}}$$

Smaller values of R_1 and R_2 will reduce the influence of I_{ADJ} on the output voltage, but the no-load current drain on the regulator will be increased. Typical values for R_1 are between 100Ω and 300Ω, giving 12.5 mA and 4.2mA no-load current respectively. There is an additional consideration in selecting R_1 the minimum load current specification of the regulator. The operating current of the

APPLICATION INFORMATION (continued)

SG137A flows from input to output. If this current is not absorbed by the load, the output of the regulator will rise above the regulated value. The current drawn by R_1 and R_2 is normally high enough to absorb the current, but care must be taken in no–load situations where R_1 and R_2 have high values. The maximum value for the operating current, which must be absorbed, is 5mA for the SG137A, If input-output voltage differential is less than 10V, the operating current that must be absorbed drops to 3mA.

EXAMPLES:

1. A precision 10V regulator to supply up to 1Amp load current.

   a. Select $R_1 = 100\Omega$ to minimize effect of I_{ADJ}

   b. Calculate $R_2 = \frac{V_{OUT} - V_{REF}}{(V_{REF}/R_1) + I_{ADJ}} = \frac{10V - 1.25V}{(1.25V/100\Omega) + 65\mu A} = 704\Omega$

2. A 15V regulator to run off batteries and supply 50mA. V_{IN} MAX = 25V

   a. To minimize battery drain, select R_1 as high as possible

   $$R_1 = \frac{1.25V}{3mA} = 417\Omega, \text{ use } 404\Omega, 1\%$$

TYPICAL APPLICATIONS

The output stability, load regulation, line regulation, thermal regulation, temperature drift, long term drift, and noise, can be improved by a factor of 6.6 over the standard regulator configuration. This assumes a zener whose drift and noise is considerably better than the regulator itself. The LM329B has 20PPM/°C maximum drift and about 10 times lower noise than the regulator.

In the application shown Figure 8, regulators #2 to #N will track regulator #1 to within ±24mV initially, and to ±60mV over all load, line, and temperature conditions. If any regulator output is shorted to ground, all other outputs will drop to -2V. Load regulation of regulators #2 to #N will be improved by $V_{OUT}/1.25V$ compared to a standard regulator, so regulator #1 should be the one which has the lowest load current.

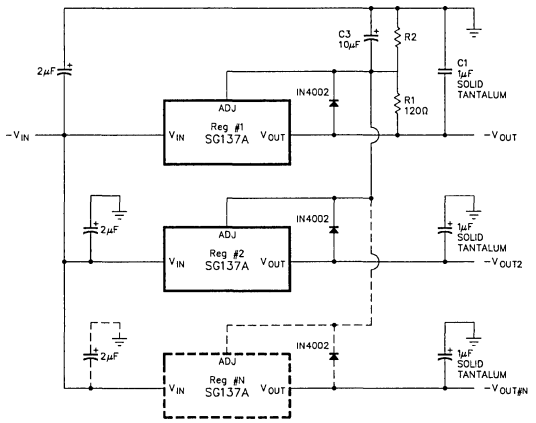


FIGURE 8 - MULTIPLE TRACKING REGULATORS

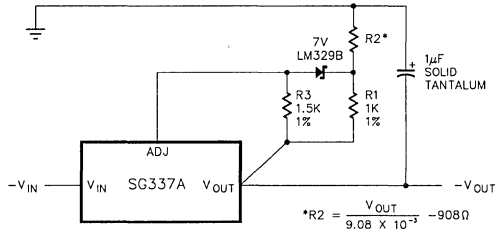


FIGURE 9 - HIGH STABILITY REGULATOR

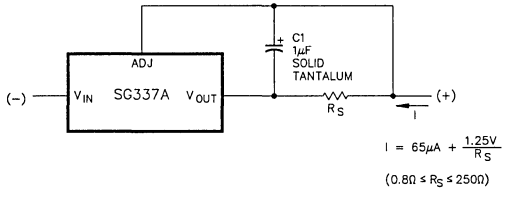


FIGURE 10 - CURRENT REGULATOR

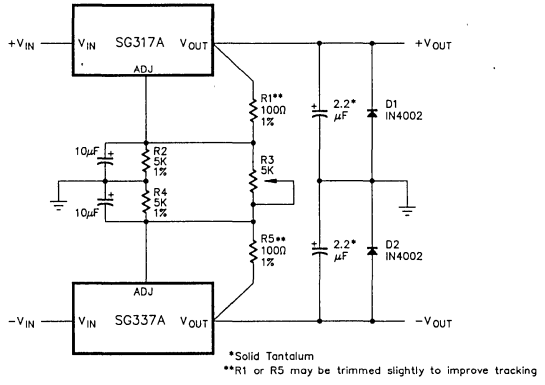
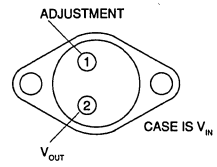
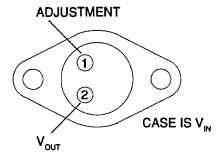
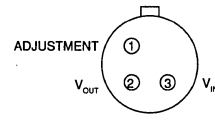
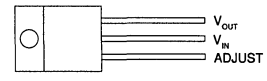
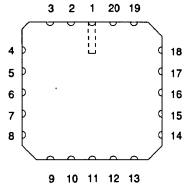


FIGURE 11 - DUAL TRACKING SUPPLY ±1.25V to ±20V

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
3-TERMINAL TO-3 METAL CAN K-PACKAGE	SG137AK/883B SG137AK SG237AK SG337AK SG137K/883B SG137K SG237K SG337K	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70C -55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
3-TERMINAL TO-66 METAL CAN R-PACKAGE	SG137AR/883B SG137AR SG237AR SG337AR SG137R/883B SG137R SG237R SG337R	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C -55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
3-PIN TO-39 METAL CAN T-PACKAGE	SG137AT/883B SG137AT SG237AT SG337AT SG137T/883B SG137T SG237T SG337T	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C -55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
3-PIN HERMETIC TO-257 G-PACKAGE (Non-Isolated) 3-PIN HERMETIC TO-257 IG-PACKAGE (Isolated)	SG137AG/883B SG137AG SG137G/883B SG137G SG137AIG/883B SG137AIG SG137IG/883B SG137IG	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C	
20-PIN CERAMIC (LCC) LEADLESS CHIP CARRIER L- PACKAGE	SG137AL/883B SG137AL SG137L/883B SG137L	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C	(Note 4) 1. V_{OUT} 2. V_{OUT} 3. N.C. 4. N.C. 5. N.C. 6. N.C. 7. N.C. 8. N.C. 9. N.C. 10. N.C.  11. V_{IN} 12. N.C. 13. N.C. 14. N.C. 15. N.C. 16. ADJUST 17. N.C. 18. N.C. 19. N.C. 20. N.C.

Note 1. Contact factory for JAN and DESC product availability.
2. All parts are viewed from the top.
3. Product is also available in flatpack. Consult factory for price and delivery.
4. Both outputs must be externally connected together at the device terminals.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SG138A/SG238A/SG338A
SG138/SG238/SG338

5 AMP POSITIVE ADJUSTABLE VOLTAGE REGLATOR

DESCRIPTION

The SG138A series are 3-terminal positive adjustable voltage regulators capable of supplying in excess of 5A over a 1.25V to 32V output voltage range. These regulators are exceptionally easy to use, requiring only two external resistors to program the output voltage. In addition, a major feature of the "A" version device is the initial output voltage tolerance which is guaranteed to be within ±1% at room temperature. Over full operating conditions, including load, line, and power dissipation, the reference is guaranteed not to very more than 2%.

A novel characteristic of the SG138A series is its new current limit circuitry, which allows transient load currents of up to 12A to be safely delivered to the load without additional protection schemes.

The SG138A is an improved version of the popular LM138, and utilizes advanced circuit design, device layout, and processing techniques in order to provide superior performance and reliability.

FEATURES

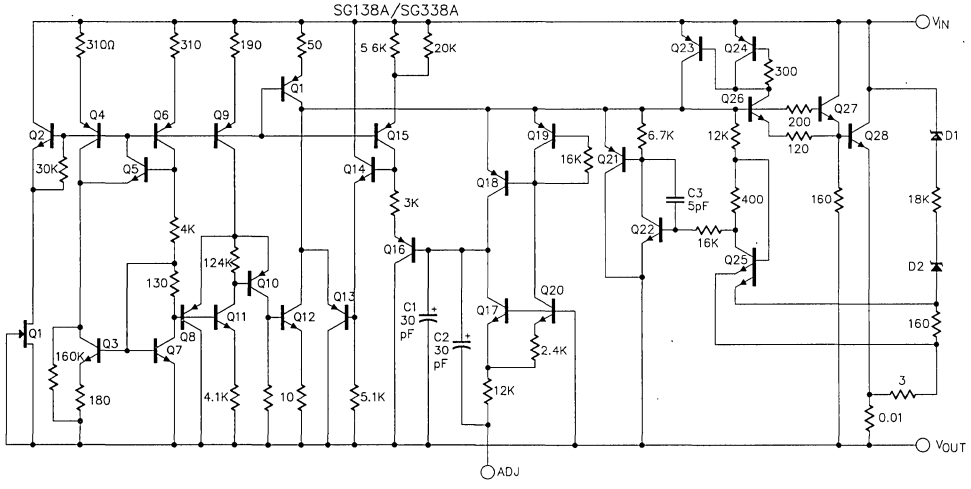
- **Guaranteed 5A output current**
- **Guaranteed 1% output voltage tolerance**
- **Guaranteed 0.3 % load regulation**
- **Guaranteed 0.01% line regulation**
- **Low TC internal current limit**
- **Thermal overload protection**
- **Improved output transistor safe operating area compensation**
- **Output adjustable from 1.25V to 32V**
- **Paralleling regulators for higher output current**

HIGH RELIABILITY FEATURES -SG138A/SG138

- **Available to MIL-STD-883**
- **SG level "S" processing available**

4

SCHEMATIC



April 1990

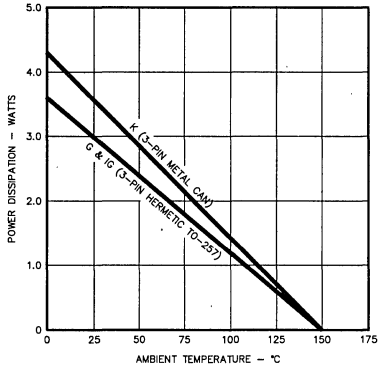
ABSOLUTE MAXIMUM RATINGS (Note 1)

Power Dissipation ..... Internally Limited
Input to Output Voltage Differential 35V
Storage Temperature Range ..... -65°C to 150°C

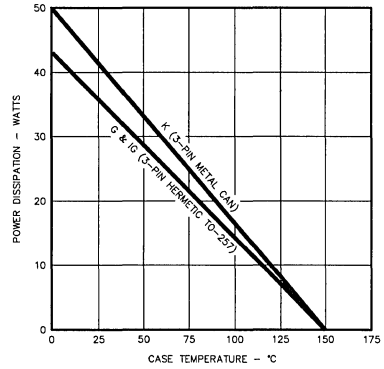
Operating Junction Temperature
Hermetic (K, G, IG-Packages) ..... 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Input to Output Voltage Differential ..... 3V to 35V

Operating Junction Temperature Range
SG138A/SG138 ..... -55°C to 150°C
SG238A/SG238 ..... -25°C to 150°C
SG338A/SG338 ..... 0°C to 125°C

Note 2: Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over full operating ambient temperatures for SG138A/SG138 with $-55°C \le T_A \le 150°C$, SG238A/SG238 with $-25°C \le T_A \le 150°C$, SG338A/SG338 with $0°C \le T_A \le 125°C$, $V_{IN} - V_{OUT} = 5.0V$, $I_{OUT} = 2.5mA$. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG138A/SG238A			SG138/SG238			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Voltage	$I_{OUT} = 10mA$ $T_A = 25°C$	1.238	1.250	1.262				V
	$3V \le (V_{IN} - V_{OUT}) \le 35V$							
	$10mA \le I_{OUT} \le 5A$, $P \le 50W$	1.225	1.250	1.270	1.19	1.24	1.29	V
Line Regulation	$3V \le (V_{IN} - V_{OUT}) \le 35V$, (Note 3)							
	$T_A = 25°C$		0.005	0.01		0.005	0.01	%/V
	$T_A = T_{MIN}$ to T_{MAX}		0.02	0.04		0.02	0.04	%/V
Load Regulation	$10mA \le I_{OUT} \le 5A$, (Note 3)							
	$V_{OUT} \le 5V$, $T_A = 25°C$		5	15		5	15	mV
	$V_{OUT} \ge 5V$, $T_A = 25°C$		0.1	0.3		0.1	0.3	%
	$V_{OUT} \le 5V$		20	30		20	30	mV
	$V_{OUT} \ge 5V$		0.3	0.6		0.3	0.6	%
Thermal Regulation	$T_A = 25°C$, 20msec pulse		0.002	0.01		0.002	0.01	%/W
Ripple Rejection	$V_{OUT} = 10V$, f =120Hz							
	$C_{ADJ} = 0$		60			60		dB
	$C_{ADJ} = 10\mu F$	60	75		60	75		dB
Adjust Pin Current			45	100		45	100	µA
Adjust Pin Current Change	$10mA \le I_{OUT} \le 5A$, $3V \le (V_{IN} - V_{OUT}) \le 35V$		0.2	5		0.2	5	µA

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG138A/SG238A			SG138/SG238			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Minimum Load Current	$(V_{IN} - V_{OUT}) = 35V$		3.5	5		3.5	5	mA
Current Limit	$(V_{IN} - V_{OUT}) \leq 10V$							
	DC	5	8		5	8		A
	0.5ms peak	7	12		7	12		A
	$(V_{IN} - V_{OUT}) = 30V$, $T_J = 25°C$		1			1		A
Temperature Stability			1	2		1		%
Long Term Stability	$T_A = 125°C$, 1000 Hours		0.3	1		0.3	1	%
RMS Output Noise (% of V_{OUT})	$T_A = 25°C$, 10Hz ≤ f ≤ 10 KHz		0.001			0.003		%
Thermal Resistance	Junction to case			1			1	°C/W

Parameter	Test Conditions	SG338A			SG338			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Voltage	$I_{OUT} = 10mA$ $T_A = 25°C$	1.238	1.250	1.262				V
	$3V \leq (V_{IN} - V_{OUT}) \leq 35V$							
	$10mA \leq I_{OUT} \leq 5A$, $P \leq 50W$	1.225	1.250	1.270	1.19	1.24	1.29	V
Line Regulation	$3V \leq (V_{IN} - V_{OUT}) \leq 35V$, (Note 3)							
	$T_A = 25°C$		0.005	0.01		0.005	0.03	%/V
	$T_A = T_{MIN}$ to T_{MAX}		0.02	0.04		0.02	0.06	%/V
Load Regulation	$10mA \leq I_{OUT} \leq 5A$, (Note 3)							
	$V_{OUT} \leq 5V$, $T_A = 25°C$		5	15		5	25	mV
	$V_{OUT} \geq 5V$, $T_A = 25°C$		0.1	0.3		0.1	0.5	%
	$V_{OUT} \leq 5V$		20	30		20	50	mV
	$V_{OUT} \geq 5V$		0.3	0.6		0.3	1	%
Thermal Regulation	$T_A = 25°C$, 20msec pulse		0.002	0.02		0.002	0.02	%/W
Ripple Rejection	$V_{OUT} = 10V$, f =120Hz							
	$C_{ADJ} = 0$		60			60		dB
	$C_{ADJ} = 10\mu F$	60	75		60	75		dB
Adjust Pin Current			45	100		45	100	µA
Adjust Pin Current Change	$10mA \leq I_{OUT} \leq 5A$, $3V \leq (V_{IN} - V_{OUT}) \leq 35V$		0.2	5		0.2	5	µA
Minimum Load Current	$(V_{IN} - V_{OUT}) = 35V$		3.5	10		3.5	10	mA
Current Limit	$(V_{IN} - V_{OUT}) \leq 10V$							
	DC	5	8		5	8		A
	0.5ms peak	7	12		7	12		A
	$(V_{IN} - V_{OUT}) = 30V$, $T_J = 25°C$		1			1		A
Temperature Stability			1	2		1		%
Long Term Stability	$T_A = 125°C$, 1000 Hours		0.3	1		0.3	1	%
RMS Output Noise (% of V_{OUT})	$T_A = 25°C$, 10Hz ≤ f ≤ 10 KHz		0.001			0.003		%
Thermal Resistance	Junction to case			1			1	°C/W

Note 3: See thermal regulation specifications for changes in output voltage due to heating effects. Load and line regulation are measured at a constant junction temperature by low duty cycle pulse testing.

4

CHARACTERISTIC CURVES

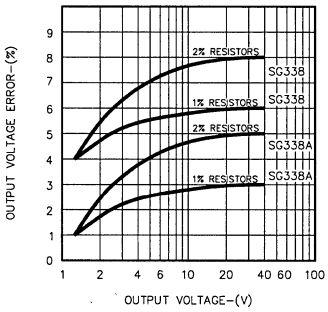


FIGURE 1.
OUTPUT VOLTAGE ERROR VS. OUTPUT VOLTAGE

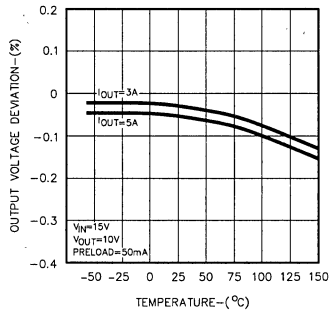


FIGURE 2.
LOAD REGULATION VS. TEMPERATURE

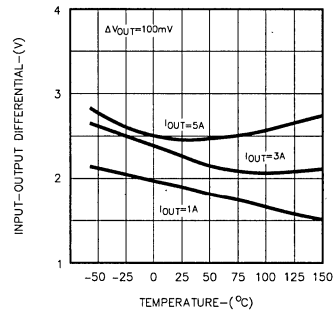


FIGURE 3.
DROPOUT VOLTAGE VS. TEMPERATURE

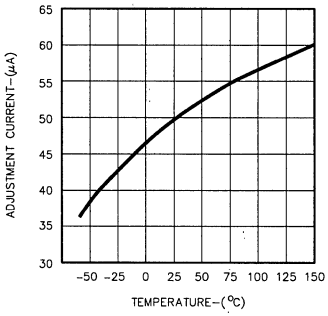


FIGURE 4.
ADJUSTMENT CURRENT VS. TEMPERATURE

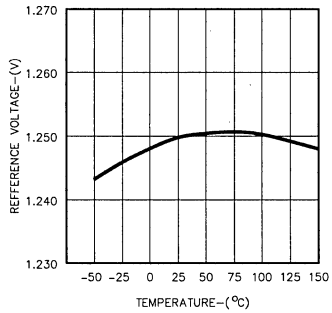


FIGURE 5.
TEMPERATURE STABILITY

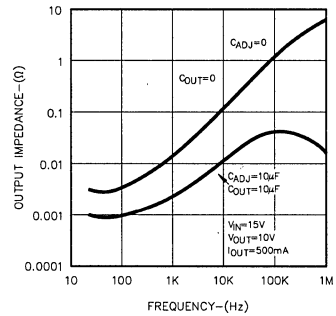


FIGURE 6.
OUTPUT IMPEDANCE VS. FREQUENCY

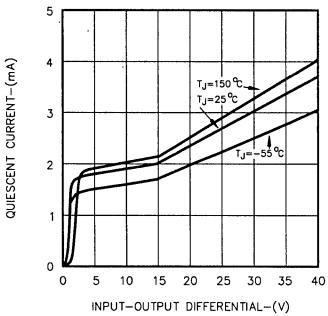


FIGURE 7.
MINIMUM OPERATING CURRENT VS. INPUT - OUTPUT DIFFERENTIAL

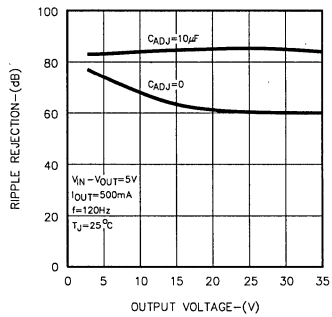


FIGURE 8.
RIPPLE REJECTION VS. OUTPUT VOLTAGE

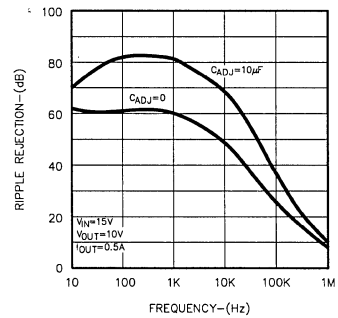


FIGURE 9.
RIPPLE REJECTION VS. FREQUENCY

CHARACTERISTIC CURVES (continued)

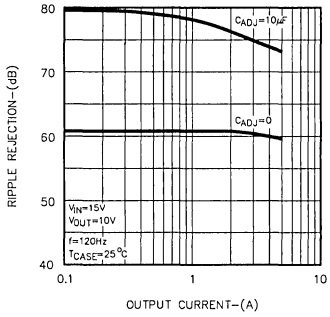


FIGURE 10.
RIPPLE REJECTION

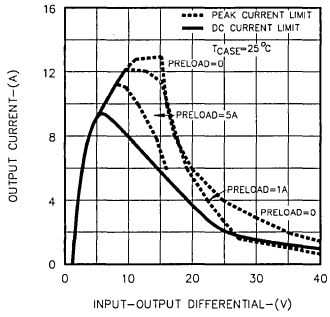


FIGURE 11.
CURRENT LIMIT VS. INPUT - OUTPUT DIFFERENTIAL

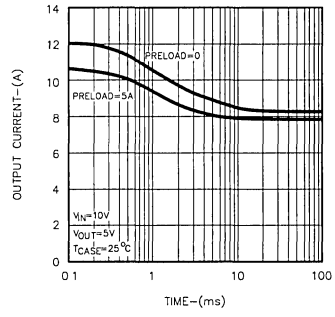


FIGURE 12.
CURRENT LIMIT VS. PERIOD

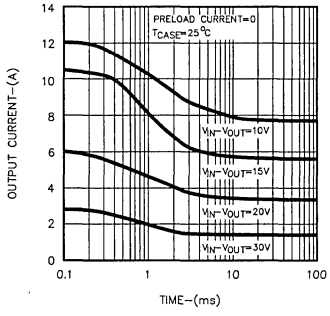


FIGURE 13.
CURRENT LIMIT VS. PERIOD

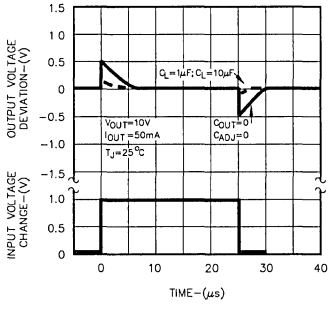


FIGURE 14.
LINE TRANSIENT RESPONSE VS. PERIOD

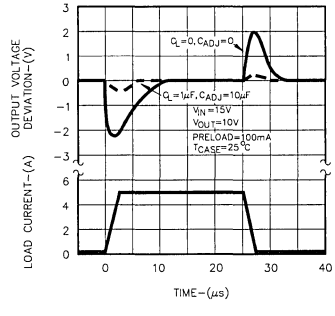


FIGURE 15.
LOAD TRANSIENT RESPONSE VS. PERIOD

APPLICATION INFORMATION

GENERAL

The SG138A develops a 1.25V reference voltage between the output and the adjustable terminal (see Figure 1). By placing a resistor, R1, between these two terminals, a constant current is caused to flow through R1 and down through R2 to set the overall output voltage. Normally this current is the specified minimum load current of 5mA or 10mA. Because I_{ADJ} is very small and constant when compared with the current through R1, it represents a small error and can usually be ignored. It is easily seen from the output voltage equation, that even if the resistors were of exact value, the accuracy of the output is limited by the accuracy of V_{REF}. Earlier adjustable regulators had a reference tolerance of ±4% which is dangerously close to the ±5% supply tolerance required in many logic and analog systems. Further, even 1% resistors can drift 0.01%/°C, adding additional error to the output voltage tolerance.

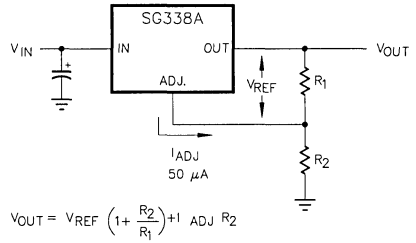


FIGURE 16 - BASIC ADJUSTABLE REGULATOR

APPLICATION INFORMATION (continued)

For example, using 2% resistors and ±4% tolerance for V_{REF}, calculations will show that the expected range of a 5V regulator design would be $4.66V \leq V_{OUT} \leq 5.36V$ or approximately ±7%. If the same example were used for a 15V regulator, the expected tolerance would be ±8%. With these results most applications required some method of trimming, usually a trim pot. This solution is both expensive and not conducive to volume production

One of the enhancements of Silicon General's adjustable regulators over existing devices is the tightened initial tolerance of V_{REF}. This allows relatively inexpensive 1% or 2% film resistors to be used to R1 and R2 to set the output voltage within an acceptable tolerance.

With a guaranteed 1% reference, a 5V power supply design, using ±2% resistors, would have a worst case manufacturing tolerance of ±4%. If 1% resistors are used, the tolerance will drop to ±2.5%. A plot of the worst case output voltage tolerance as a function of resistor tolerance is shown on the front page.

For convenience, a table of standard 1% resistor values is shown below.

Table of ½% and 1% Standard Resistance Values

1.00	1.47	2.15	3.16	4.64	6.81
1.02	1.50	2.21	3.24	4.75	6.98
1.05	1.54	2.26	3.32	4.87	7.15
1.07	1.58	2.32	3.40	4.99	7.32
1.10	1.62	2.37	3.48	5.11	7.50
1.13	1.65	2.43	3.57	5.23	7.68
1.15	1.69	2.49	3.65	5.36	7.87
1.18	1.74	2.55	3.74	5.49	8.06
1.21	1.78	2.61	3.83	5.62	8.25
1.24	1.82	2.67	3.92	5.76	8.45
1.27	1.87	2.74	4.02	5.90	8.66
1.30	1.91	2.80	4.12	6.04	8.87
1.33	1.96	2.87	4.22	6.19	9.09
1.37	2.00	2.94	4.32	6.34	9.31
1.40	2.05	3.01	4.42	6.49	9.53
1.43	2.10	3.09	4.53	6.65	9.76

Standard Resistance Values are obtained from the Decade Table by multiplying by multiples of 10. As an example:1.21 can represent 1.21Ω, 12.1Ω, 121Ω, 1.21KΩ etc.

BYPASS CAPACITORS

Input bypassing using a 1µF tantalum or 25µF electrolytic is recommended when the input filter capacitors are more than 5 inches from the device. Improved ripple rejection (80dB) can be accomplished by adding a 10µF capacitor from the adjust pin to ground. Increasing the size of the capacitor to 20µF will help ripple rejection at low output voltage since the reactance of this capacitor should be small compared to the voltage setting resistor, R2. For improved AC transient response and to prevent the possibility of oscillation due to unknown reactive load, a 1µF capacitor is also recommended at the output. Because of their low impedance at high frequencies, the best type of capacitor to use is solid tantalum.

PROTECTION DIODES

The SG138A/338A do not require a protection diode from the adjustment terminal to the output (see Figure17). Improved internal circuitry eliminates the need for this diode when the adjustment pin is bypassed with a capacitor to improve ripple rejection.If a very large output capacitor is used, such as a 100µF shown in Figure 2, the regulator could be damaged or destroyed if the input is accidentally shorted to ground or crowbarred, due to the output capacitor discharging into the output terminal of the regulator. To prevent this, a diode D1 as shown, is recommended to safely discharge the capacitor.

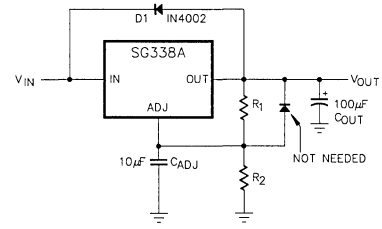


FIGURE 17 - REMOVING PROTECTION DIODE

LOAD REGULATION

Because the SG138A is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the wire connecting the regulator to the load. The data sheet specification for load regulation is measured at the bottom of the package. Negative side sensing is a true Kelvin connection, with the bottom of the output divider returned to the negative side of the load. Although it may not be immediately obvious, best load regulation is obtained when the top of the resistor divider, (R1), is connected directly to the case not to the load. This is illustrated in Figure 18. If R1 were connected to the load, the effective resistance between the regulator and the load would be

$$R_P X \left(\frac{R2 + R1}{R1}\right), R_P = \text{Parasitic Line Resistance.}$$

Connected as shown, R_P is not multiplied by the divider ratio. R_P is about 0.004Ω per foot using 16 gauge wire. This translates to 4mV/ft at 1A load current, so it is important to keep the positive lead between regulator and load as short as possible, and use large wire or PC board traces.

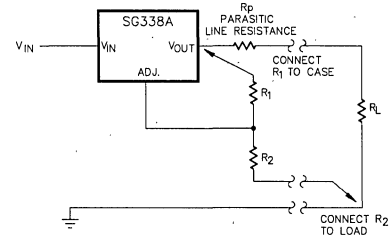


FIGURE 18 - CONNECTIONS FOR BEST LOAD REGULATION

TYPICAL APPLICATIONS

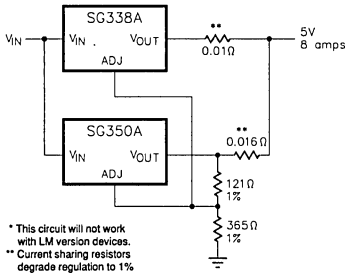


FIGURE 19 - PARALLEL REGULATORS FOR HIGHER CURRENT

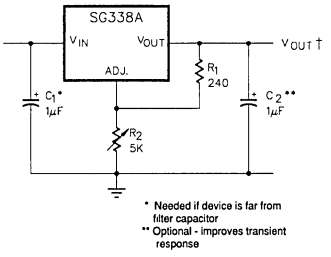


FIGURE 20 - 1.2V - 25V ADJUSTABLE REGULATOR

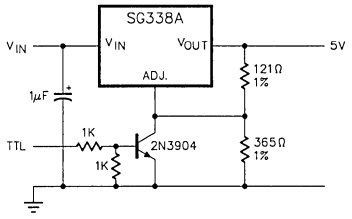


FIGURE 21 - 5V REGULATOR WITH SHUT DOWN

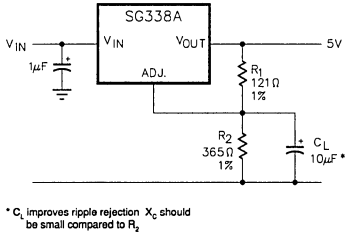


FIGURE 22 - IMPROVING RIPPLE REJECTION

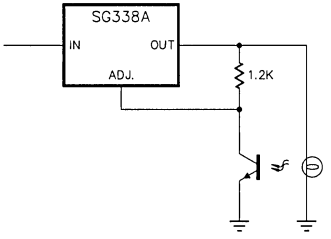


FIGURE 23 - AUTOMATIC LIGHT CONTROL

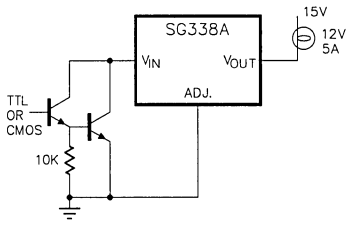


FIGURE 24 - PROTECTED HIGH CURRENT LAMP DRIVER

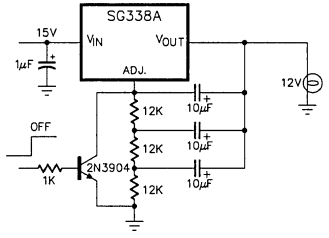


FIGURE 25 - LAMP FLASHER

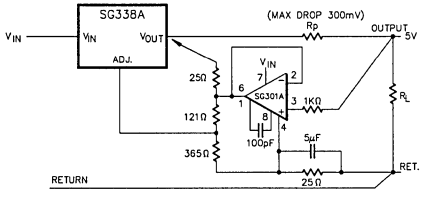


FIGURE 26 - REMOTE SENSING

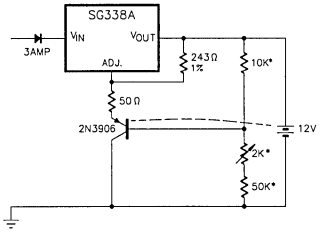
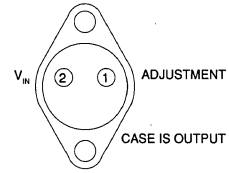
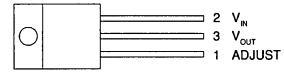


FIGURE 27 - TEMPERATURE COMPENSATED LEAD ACID BATTERY CHARGER

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
3-PIN METAL CAN K-PACKAGE	SG138AK/883B SG138AK SG238AK SG338AK SG138K/883B SG138K SG238K SG338K	-55°C to 150°C -55°C to 150°C -25°C to 150°C 0°C to 125°C -55°C to 150°C -55°C to 150°C -25°C to 150°C 0°C to 125°C	
3-PIN HERMETIC TO-257 G-PACKAGE (non-Isolated) 3-PIN HERMETIC TO-257 IG-PACKAGE (Isolated)	SG138AG/883B SG138AG SG138G/883B SG138G SG138AIG/883B SG138AIG SG138IG/883B SG138IG	-55°C to 150°C -55°C to 150°C -55°C to 150°C -55°C to 150°C -55°C to 150°C -55°C to 150°C -55°C to 150°C -55°C to 150°C	

Note 1. Contact factory for JAN and DESC product availability.
2. All parts are viewed from the top.

SG140A/SG340A
SG140/SG340

POSITIVE FIXED VOLTAGE REGULATOR

DESCRIPTION

The SG140A/140 series of positive regulators offer self contained, fixed-voltage capability with up to 1.5A of load current and input voltage up to 50V (SG140A series only).

These units feature a unique on-chip trimming system to set the output voltages to within ±1.5% of nominal on the SG140A series, ±2.0% on the SG140 series, and ±4.0% on the SG340 series. The SG140A versions also offer much improved line and load regulation characteristics. Utilizing an improved Bandgap reference design, problems have been eliminated that are normally associated with the Zener Diode references, such as drift in output voltage and large changes in the line and load regulation.

All protective features of thermal shutdown, current limiting, and safe-area control have been designed into these units and since these regulators require only a small output capacitor for satisfactory performance, ease of application is assured.

Although designed as fixed-voltage regulators, the output voltage can be increased through the use of a simple voltage divider. The low quiescent drain current of the device insures good regulation when this method is used.

Product is available in hermetically sealed TO-220 (both isolated and non-isolated), TO-3 and TO-66 power packages.

FEATURES

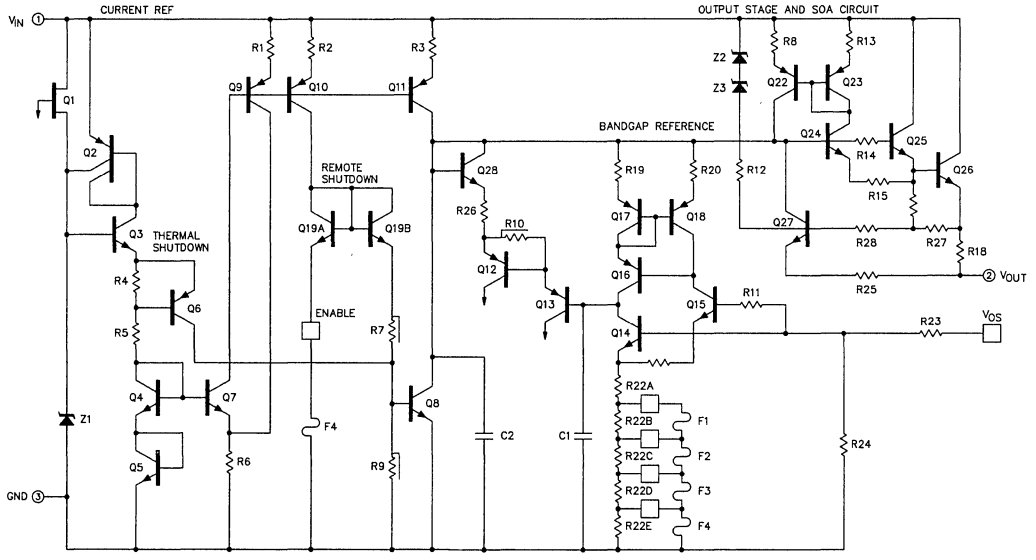
- **Output voltage set internally to ±1.5% on SG140A**
- **Input voltage reange to 50V max. on SG140A**
- **Two volt input-output differential**
- **Bandgap reference voltage**
- **Excellent line and load regulation**
- **Foldback current limiting**
- **Thermal overload protection**
- **Voltages available - 5V, 6V, 8V, 12V,15V,18V, 24V**

HIGH RELIABILITY FEATURES - SG140A/140

- **Available to MIL-STD - 883**
- **Radiation data available**
- **SG level "S" processing available**

4

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

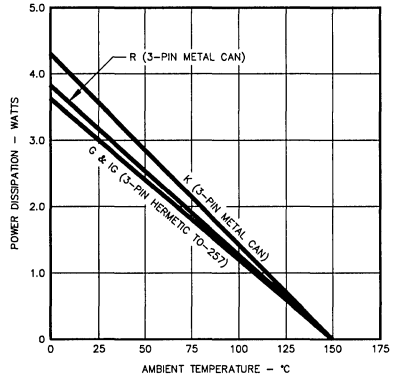
Device Output Voltage	Input Voltage	Input Voltage (transient) (Note 3)	Input Voltage Differential (Output shorted to ground)
5V	35V	50V	35V
6V	35V	50V	35V
8V	35V	50V	35V
12V	35V	50V	35V
15V	35V	50V	35V
18V	35V	50V	35V
24V	40V	50V	35V

Operating Junction Temperature
Hermetic (K, R, G, IG - Packages) ..... 150°C

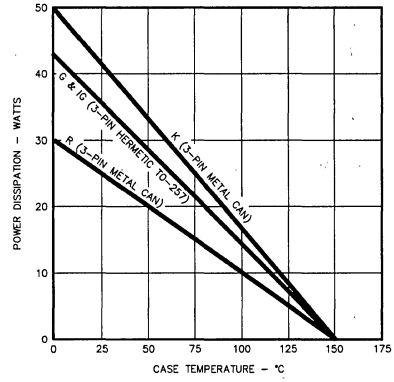
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Values beyond which damage may occur.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Operating Junction Temperature Range:
SG140A/140 ..... -55°C to 150°C
SG340A/340 ..... 0°C to 125°C

Note 2. Range over which the device is functional.

CHARACTERISTIC CURVES

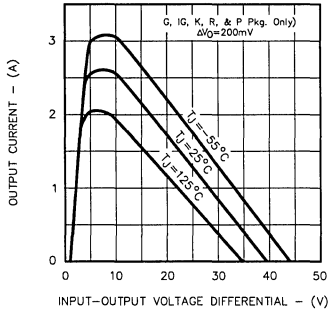


FIGURE 1.
PEAK OUTPUT CURRENT
VS. INPUT - OUTPUT DIFFERENTIAL

Note 3. Operation at high input voltages is dependent upon load current. When load current is less than 5mA, output will rise out of regulation as input-oiutput differential icreases beyond 30V. Note also from Figure 1, that maximum load current is reduced at high voltages. The 50V input rating of the SG140A series refers to ability to withstnd high line or transient conditions without damage. Since the regulator's maximum current capability is reduced, the output may fall out of regulation at high input voltages under nominal loading.

CHARACTERISTIC CURVES (continued)

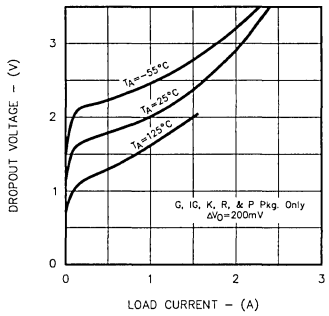


FIGURE 2.
MINIMUM INPUT - OUTPUT VOLTAGE
VS. LOAD CURRENT

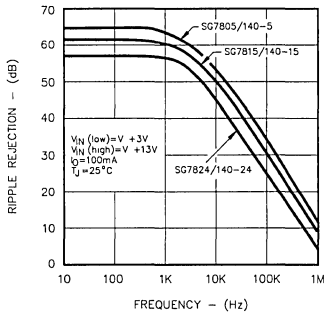


FIGURE 3.
RIPPLE REJECTION VS. FREQUENCY

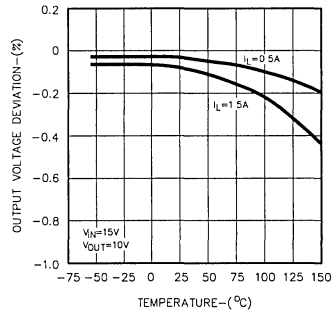
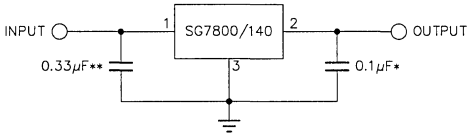


FIGURE 4.
TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE

APPLICATIONS



* INCREASING VALUE OF OUTPUT CAPACITOR IMPROVES SYSTEM TRANSIENT RESPONSE

** REQUIRED ONLY IF REGULATOR IS LOCATED AN APPRECIABLE DISTANCE FROM POWER SUPPLY FILTER

FIGURE 5 - FIXED OUITPUT REGULATOR

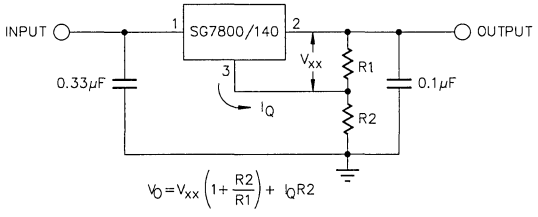


FIGURE 6 - CIRCUIT FOR INCREASING OUITPUT VOLTAGE

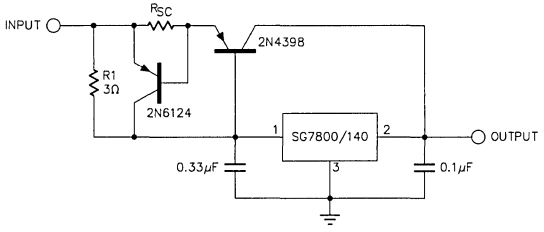


FIGURE 7 - HIGH OUTPUT CIRRENT, SHORT CIRCUIT PROTECTED

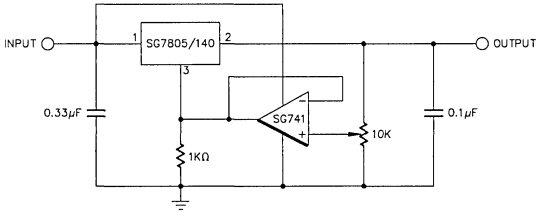


FIGURE 8 - ADJUTABLE OUITPUT REGULATOR, 7V to 30V

ELECTRICAL SPECIFICATIONS (Note 1)

SG140A - 5/SG340A - 5

(Unless otherwise specified, these specifications apply over full operating ambient temperatures for SG140A-05 with -55°C ≤ T_A ≤ 150°C, SG340A-05 with 0°C ≤ T_A ≤ 125°C, and V_{IN} = 10V, I_O = 1.0A, C_{IN} = 0. 33µF, C_{OUT} = 0.1µF and are applicable for the K, R, G, and IG - Power package - only. Low duty cycle pulse testing techniques are used which maintains junction and case temperature equal to the ambient temperature.)

Parameter	Test Conditions	SG140A-5			SG340A-5			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	I_O = 5mA to 1.0A, T_J = 25°C	4.9	5.0	5.1	4.9	5.0	5.1	V
Line Regulation (Note 1)	V_{IN} = 7.5V to 20V, I_O = 500mA			10			10	mV
	V_{IN} = 7.5V to 20V, T_J = 25°C		3	10		3	10	mV
	V_{IN} = 7.5V to 20V			12			12	mV
	V_{IN} = 8V to 12V, T_J = 25°C			4			4	mV
Load Regulation (Note 1)	I_O = 5mA to 1.0A			25			25	mV
	I_O = 5mA to 1.5A, T_J = 25°C		10	25		10	25	mV
	I_O = 250mA to 750mA, T_J = 25°C			15			15	mV
Total Output Voltage Tolerance	V_{IN} = 7.5V to 20V, I_O = 5mA to 1.0A, P ≤ 15W	4.8	5.0	5.2	4.8	5.0	5.2	V
Quiescent Current	Over Temperature Range			6.5			6.5	mA
	T_J = 25°C			6			6	mA
Quiescent Current Change	With Line: V_{IN} = 7.5V to 25V, I_O = 500mA			0.8			0.8	mA
	V_{IN} = 7.5V to 20V, I_O = 1A, T_J = 25°C			0.8			0.8	mA
	With Load: I_O = 5mA to 1.0A			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, I_O = 1A, T_J = 25°C		2	2.5		2	2.5	V
Peak Output Current	T_J = 25°C		2.4			2.4		A
Short Circuit Current	T_J = 25°C		2.1			2.1		A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	68			68			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)			40			40	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		20			20		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

SG140 - 5/SG340 - 5

(Unless otherwise specified, these specifications apply over full operating ambient temperatures for SG140-05 with -55°C ≤ T_A ≤ 150°C, SG340-05 with 0°C ≤ T_A ≤ 125°C, and V_{IN} = 10V, I_O = 500mA, C_{IN} = 0. 33µF, C_{OUT} = 0.1µF and are applicable for the K, R, G, and IG - Power package - only. Low duty cycle pulse testing techniques are used which maintains junction and case temperature equal to the ambient temperature.)

Parameter	Test Conditions	SG140-5			SG340-5			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	I_O = 5mA to 1.0A, T_J = 25°C	4.8	5.0	5.2	4.8	5.0	5.2	V
Line Regulation (Note 1)	V_{IN} = 8V to 20V			50			50	mV
	V_{IN} = 7V to 25V, T_J = 25°C			50			50	mV
	V_{IN} = 8V to 12V, I_O = 1.0A			25			25	mV
	V_{IN} = 7.3V to 20V, I_O = 1.0A, T_J = 25°C			50			50	mV
Load Regulation (Note 1)	I_O = 5mA to 1.0A			50			50	mV
	I_O = 5mA to 1.5A, T_J = 25°C			50			50	mV
	I_O = 250mA to 750mA, T_J = 25°C			25			25	mV
Total Output Voltage Tolerance	V_{IN} = 8V to 20V, I_O = 5mA to 1.0A, P ≤ 15W	4.75	5.00	5.25	4.75	5.00	5.25	V
Quiescent Current	I_O = 1.0A			7			8.5	mA
	T_J = 25°C			6			8	mA
Quiescent Current Change	With Line: V_{IN} = 8V to 25V			0.8			1.0	mA
	V_{IN} = 8V to 20V, I_O = 1A, T_J = 25°C			0.8			1.0	mA
	With Load: I_O = 5mA to 1.0A			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, I_O = 1A, T_J = 25°C		2	2.5		2	2.5	V
Peak Output Current	T_J = 25°C		2.4			2.4		A
Short Circuit Current	T_J = 25°C		2.1			2.1		A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	68			62			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)			40			40	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		20			20		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

Note 1. All regulation tests are made at constant junction temperature with low duty cycle testing.
2. This test is guaranteed but is not tested in production.

ELECTRICAL SPECIFICATIONS (Note 1)

SG140 - 6/SG340 - 6

(Unless otherwise specified, these specifications apply over full operating ambient temperatures for SG140-06 with -55°C ≤ T_A ≤ 150°C, SG340-06 with 0°C ≤ T_A ≤ 125°C, and V_{IN} = 11V, I_O = 500mA, C_{IN} = 0. 33µF, C_{OUT} = 0.1µF and are applicable for the K, R, G, and IG - Power package - only. Low duty cycle pulse testing techniques are used which maintains junction and case temperature equal to the ambient temperature.)

Parameter	Test Conditions	SG140 - 6			SG340 - 6			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	I_O = 5mA to 1.0A, T_J = 25°C	5.75	6.00	6.25	5.75	6.00	6.25	V
Line Regulation (Note 1)	V_{IN} = 9V to 21V			60			60	mV
	V_{IN} = 8V to 25V, T_J = 25°C			60			60	mV
	V_{IN} = 9V to 13V, I_O= 1.0 A			30			30	mV
	V_{IN} = 8.3V to 21V, I_O= 1.0 A, T_J = 25°C			60			60	mV
Load Regulation (Note 1)	I_O = 5mA to 1.0A			60			60	mV
	I_O = 5mA to 1.5A, T_J = 25°C			60			60	mV
	I_O = 250mA to 750mA, T_J = 25°C			30			30	mV
Total Output Voltage Tolerance	V_{IN} = 9V to 21V, I_O = 5mA to 1.0A, P ≤ 15W	5.7	6.0	6.3	5.7	6.0	6.3	V
Quiescent Current	I_O= 1.0 A			7			8.5	mA
	T_J= 25°C			6			8	mA
Quiescent Current Change	With Line: V_{IN} = 9V to 25V			0.8			1.0	mA
	V_{IN} = 9V to 21V, I_O = 1A, T_J = 25°C			0.8			1.0	mA
	With Load: I_O = 5mA to 1.0A			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, I_O = 1A, T_J = 25°C		2	2.5		2	2.5	V
Peak Output Current	T_J = 25°C		2.4			2.4		A
Short Circuit Current	T_J = 25°C		2.1			2.1		A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	65			59			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)			40			40	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		24			24		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

SG140 - 8/SG340 - 8

(Unless otherwise specified, these specifications apply over full operating ambient temperatures for SG140-08 with -55°C ≤ T_A ≤ 150°C, SG340-08 with 0°C ≤ T_A ≤ 125°C, and V_{IN} = 14V, I_O = 500mA, C_{IN} = 0. 33µF, C_{OUT} = 0.1µF and are applicable for the K, R, G, and IG - Power package - only. Low duty cycle pulse testing techniques are used which maintains junction and case temperature equal to the ambient temperature.)

Parameter	Test Conditions	SG140 - 8			SG340 - 8			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	I_O = 5mA to 1.0A, T_J = 25°C	7.7	8.0	8.3	7.7	8.0	8.3	V
Line Regulation (Note 1)	V_{IN} = 11V to 23V			80			80	mV
	V_{IN} = 10.5V to 25V, T_J = 25°C			80			80	mV
	V_{IN} = 11V to 17V, I_O = 1.0A			40			40	mV
	V_{IN} = 10.5V to 23V, I_O = 1.0A, T_J = 25°C			80			80	mV
Load Regulation (Note 1)	I_O = 5mA to 1.0A			80			80	mV
	I_O = 5mA to 1.5A, T_J = 25°C			80			80	mV
	I_O = 250mA to 750mA, T_J = 25°C			40			40	mV
Total Output Voltage Tolerance	V_{IN} = 11.5V to 23V, I_O = 5mA to 1.0A, P ≤ 15W	7.6	8.0	8.4	7.6	8.0	8.4	V
Quiescent Current	I_O = 1.0A			7			8.5	mA
	T_J = 25°C			6			8	mA
Quiescent Current Change	With Line: V_{IN} = 11.5V to 25V			0.8			1.0	mA
	V_{IN} = 11.5V to 23V, I_O = 1A, T_J = 25°C			0.8			1.0	mA
	With Load: I_O = 5mA to 1.0A			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, I_O = 1A, T_J = 25°C		2	2.5		2	2.5	V
Peak Output Current	T_J = 25°C		2.4			2.4		A
Short Circuit Current	T_J = 25°C		2.1			2.1		A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	62			56			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)			40			40	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		32			32		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

Note 1. All regulation tests are made at constant junction temperature with low duty cycle testing.
2. This test is guaranteed but is not tested in production.

ELECTRICAL SPECIFICATIONS (Note 1)

SG140 A - 12/SG340A - 12

(Unless otherwise specified, these specifications apply over full operating ambient temperatures for SG140A -12 with -55°C ≤ T_A ≤ 150°C, SG340A-12 with 0°C ≤ T_A ≤ 125°C, and V_{IN} = 19V, I_O = 1.0A, C_{IN} = 0. 33µF, C_{OUT} = 0.1µF and are applicable for the K, R, G, and IG - Power package - only. Low duty cycle pulse testing techniques are used which maintains junction and case temperature equal to the ambient temperature.)

Parameter	Test Conditions	SG140A - 12			SG340A - 12			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	I_O = 5mA to 1.0A, T_J = 25°C	11.75	12.00	12.25	11.75	12.00	12.25	V
Line Regulation (Note 1)	V_{IN} = 14.8V to 27V, I_O = 500mA			18			18	mV
	V_{IN} = 14.5V to 27V, T_J = 25°C		4	18		4	18	mV
	V_{IN} = 16V to 22V			30			30	mV
	V_{IN} = 16V to 22V, T_J = 25°C			9			9	mV
Load Regulation (Note 1)	I_O = 5mA to 1.0A			60			60	mV
	I_O = 5mA to 1.5A, T_J = 25°C			32			32	mV
	I_O = 250mA to 750mA, T_J = 25°C			19			19	mV
Total Output Voltage Tolerance	V_{IN} = 14.8V to 27V, I_O = 5mA to 1.0A, P ≤ 15W	11.5	12.0	12.5	11.5	12.0	12.5	V
Quiescent Current	Over Temperature Range			6.5			6.5	mA
	T_J = 25°C			6			6	mA
Quiescent Current Change	With Line: V_{IN} = 15V to 30V, I_O = 500mA			0.8			0.8	mA
	V_{IN} = 14.8V to 27V, I_O = 1A, T_J = 25°C			0.8			0.8	mA
	With Load: I_O = 5mA to 1.0A			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, I_O = 1A, T_J = 25°C		2	2.5		2	2.5	V
Peak Output Current	T_J = 25°C		2.4			2.4		A
Short Circuit Current	T_J = 25°C		2.1			2.1		A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	61			61			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)			40			40	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		48			48		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

SG140 - 12/SG340 - 12

(Unless otherwise specified, these specifications apply over full operating ambient temperatures for SG140-12 with -55°C ≤ T_A ≤ 150°C, SG340-12 with 0°C ≤ T_A ≤ 125°C, and V_{IN} = 19V, I_O = 500mA, C_{IN} = 0. 33µF, C_{OUT} = 0.1µF and are applicable for the K, R, G, and IG - Power package - only. Low duty cycle pulse testing techniques are used which maintains junction and case temperature equal to the ambient temperature.)

Parameter	Test Conditions	SG140 - 12			SG340 - 12			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	I_O = 5mA to 1.0A, T_J = 25°C	11.5	12.0	12.5	11.5	12.0	12.5	V
Line Regulation (Note 1)	V_{IN} = 15V to 27V			120			120	mV
	V_{IN} = 14.5V to 30V, T_J = 25°C			120			120	mV
	V_{IN} = 16V to 22V, I_O = 1.0A			60			60	mV
	V_{IN} = 14.6V to 27V, I_O = 1.0A, T_J = 25°C			120			120	mV
Load Regulation (Note 1)	I_O = 5mA to 1.0A			120			120	mV
	I_O = 5mA to 1.5A, T_J = 25°C			120			120	mV
	I_O = 250mA to 750mA, T_J = 25°C			60			60	mV
Total Output Voltage Tolerance	V_{IN} = 14.5V to 27V, I_O = 5mA to 1.0A, P ≤ 15W	11.4	12.0	12.6	11.4	12.0	12.6	V
Quiescent Current	I_O = 1.0A			7			8.5	mA
	T_J = 25°C			6			8	mA
Quiescent Current Change	With Line: V_{IN} = 15V to 30V			0.8			1.0	mA
	V_{IN} = 14.5V to 27V, I_O = 1A, T_J = 25°C			0.8			1.0	mA
	With Load: I_O = 5mA to 1.0A			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, I_O = 1A, T_J = 25°C		2	2.5		2	2.5	V
Peak Output Current	T_J = 25°C		2.4			2.4		A
Short Circuit Current	T_J = 25°C		2.1			2.1		A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	61			55			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)			40			40	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		48			48		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

Note 1. All regulation tests are made at constant junction temperature with low duty cycle testing.
2. This test is guaranteed but is not tested in production.

ELECTRICAL SPECIFICATIONS (Note 1)

SG140 A - 15/SG340A - 15

(Unless otherwise specified, these specifications apply over full operating ambient temperatures for SG140A-15 with -55°C ≤ T_A ≤ 150°C, SG340A-15 with 0°C ≤ T_A ≤ 125°C, and V_{IN} = 23V, I_O = 1.0A, C_{IN} = 0. 33µF, C_{OUT} = 0.1µF and are applicable for the K, R, G, and IG - Power package - only. Low duty cycle pulse testing techniques are used which maintains junction and case temperature equal to the ambient temperature.)

Parameter	Test Conditions	SG140A - 15			SG340A - 15			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	I_O = 5mA to 1.0A, T_J = 25°C	14.7	15.0	15.3	14.7	15.0	15.3	V
Line Regulation (Note 1)	V_{IN} = 17.9V to 30V, I_O = 500mA			22			22	mV
	V_{IN} = 17.5V to 30V, T_J = 25°C			22			22	mV
	V_{IN} = 20V to 26V			30			30	mV
	V_{IN} = 20V to 26V, T_J = 25°C			10			10	mV
Load Regulation (Note 1)	I_O = 5mA to 1.0A			75			75	mV
	I_O = 5mA to 1.5A, T_J = 25°C			35			35	mV
	I_O = 250mA to 750mA, T_J = 25°C			21			21	mV
Total Output Voltage Tolerance	V_{IN} = 17.9V to 30V, I_O = 5mA to 1.0A, P ≤ 15W	14.4	15.0	15.6	14.4	15.0	15.6	V
Quiescent Current	Over Temperature Range			6.5			6.5	mA
	T_J = 25°C			6			6	mA
Quiescent Current Change	With Line: V_{IN} = 17.9V to 30V, I_O = 500mA			0.8			0.8	mA
	V_{IN} = 17.9V to 30V, I_O = 1A, T_J = 25°C			0.8			0.8	mA
	With Load: I_O = 5mA to 1.0A			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, I_O = 1A, T_J = 25°C		2	2.5		2	2.5	V
Peak Output Current	T_J = 25°C		2.4			2.4		A
Short Circuit Current	T_J = 25°C		2.1			2.1		A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	60			60			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)			40			40	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		60			60		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

SG140 - 15/SG340 - 15

(Unless otherwise specified, these specifications apply over full operating ambient temperatures for SG140-15 with -55°C ≤ T_A ≤ 150°C, SG340-15 with 0°C ≤ T_A ≤ 125°C, and V_{IN} = 23V, I_O = 500mA, C_{IN} = 0. 33µF, C_{OUT} = 0.1µF and are applicable for the K, R, G, and IG - Power package - only. Low duty cycle pulse testing techniques are used which maintains junction and case temperature equal to the ambient temperature.)

Parameter	Test Conditions	SG140 - 15			SG340 - 15			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	I_O = 5mA to 1.0A, T_J = 25°C	14.4	15.0	15.6	14.4	15.0	15.6	V
Line Regulation (Note 1)	V_{IN} = 18.5V to 30V			150			150	mV
	V_{IN} = 17.5V to 30V, T_J = 25°C			150			150	mV
	V_{IN} = 20V to 26V, I_O = 1.0A			75			75	mV
	V_{IN} = 17.7V to 30V, I_O = 1.0A, T_J = 25°C			150			150	mV
Load Regulation (Note 1)	I_O = 5mA to 1.0A			150			150	mV
	I_O = 5mA to 1.5A, T_J = 25°C			150			150	mV
	I_O = 250mA to 750mA, T_J = 25°C			75			75	mV
Total Output Voltage Tolerance	V_{IN} = 17.5V to 30V, I_O = 5mA to 1.0A, P ≤ 15W	14.25	15.00	15.75	14.25	15.00	15.75	V
Quiescent Current	I_O = 1.0A			7			8.5	mA
	T_J = 25°C			6			8	mA
Quiescent Current Change	With Line: V_{IN} = 18.5V to 30V			0.8			1.0	mA
	V_{IN} = 18.5V to 30V, I_O = 1A, T_J = 25°C			0.8			1.0	mA
	With Load: I_O = 5mA to 1.0A			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, I_O = 1A, T_J = 25°C		2	2.5		2	2.5	V
Peak Output Current	T_J = 25°C		2.4			2.4		A
Short Circuit Current	T_J = 25°C		2.1			2.1		A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	60			54			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)			40			40	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		60			60		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

Note 1. All regulation tests are made at constant junction temperature with low duty cycle testing.
2. This test is guaranteed but is not tested in production.

ELECTRICAL SPECIFICATIONS (Note 1)

SG140 - 18/SG340 - 18

(Unless otherwise specified, these specifications apply over full operating ambient temperatures for SG140-18 with -55°C ≤ T_A ≤ 150°C, SG340-18 with 0°C ≤ T_A ≤ 125°C, and V_{IN} = 27V, I_O = 500mA, C_{IN} = 0. 33µF, C_{OUT} = 0.1µF and are applicable for the K, R, G, and IG - Power package - only. Low duty cycle pulse testing techniques are used which maintains junction and case temperature equal to the ambient temperature.)

Parameter	Test Conditions	SG140 - 18			SG340 - 18			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	I_O = 5mA to 1.0A, T_J = 25°C	17.3	18.0	18.7	17.3	18.0	18.7	V
Line Regulation (Note 1)	V_{IN} = 21.5V to 33V			180			180	mV
	V_{IN} = 21V to 33V, T_J = 25°C			180			180	mV
	V_{IN} = 24V to 30V, I_O = 1.0A			90			90	mV
	V_{IN} = 21V to 30V, I_O = 1.0A, T_J = 25°C			180			180	mV
Load Regulation (Note 1)	I_O = 5mA to 1.0A			180			180	mV
	I_O = 5mA to 1.5A, T_J = 25°C			180			180	mV
	I_O = 250mA to 750mA, T_J = 25°C			90			90	mV
Total Output Voltage Tolerance	V_{IN} = 21V to 33V, I_O = 5mA to 1.0A, P ≤ 15W	17.1	18.0	18.9	17.1	18.0	18.9	V
Quiescent Current	I_O = 1A			7			8.5	mA
	T_J = 25°C			6			8	mA
Quiescent Current Change	With Line: V_{IN} = 21V to 33V			0.8			1.0	mA
	V_{IN} = 21V to 33V, I_O = 1A, T_J = 25°C			0.8			1.0	mA
	With Load: I_O = 5mA to 1.0A			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, I_O = 1A, T_J = 25°C		2	2.5		2	2.5	V
Peak Output Current	T_J = 25°C		2.4			2.4		A
Short Circuit Current	T_J = 25°C		2.1			2.1		A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	59			53			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)			40			40	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		72			72		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

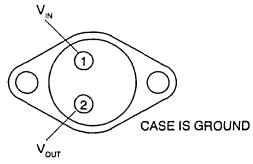
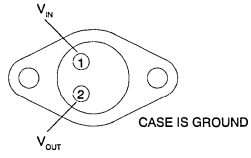
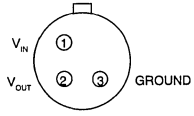
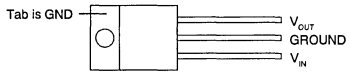
SG140 - 24/SG340 - 24

(Unless otherwise specified, these specifications apply over full operating ambient temperatures for SG140-24 with -55°C ≤ T_A ≤ 150°C, SG340-24 with 0°C ≤ T_A ≤ 125°C, and V_{IN} = 33V, I_O = 500mA, C_{IN} = 0. 33µF, C_{OUT} = 0.1µF and are applicable for the K, R, G, and IG - Power package - only. Low duty cycle pulse testing techniques are used which maintains junction and case temperature equal to the ambient temperature.)

Parameter	Test Conditions	SG140 - 24			SG340 - 24			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	I_O = 5mA to 1.0A, T_J = 25°C	23	24	25	23	24	25	V
Line Regulation (Note 1)	V_{IN} = 28V to 38V			240			240	mV
	V_{IN} = 27V to 38V, T_J = 25°C			240			240	mV
	V_{IN} = 30V to 36V, I_O = 1.0A			120			120	mV
	V_{IN} = 27.1V to 35V, I_O = 1.0A, T_J = 25°C			240			240	mV
Load Regulation (Note 1)	I_O = 5mA to 1.0A			240			240	mV
	I_O = 5mA to 1.5A, T_J = 25°C			240			240	mV
	I_O = 250mA to 750mA, T_J = 25°C			120			120	mV
Total Output Voltage Tolerance	V_{IN} = 27V to 38V, I_O = 5mA to 1.0A, P ≤ 15W	22.8	24.0	25.2	22.8	24.0	25.2	V
Quiescent Current	I_O = 1.0A			7			8.5	mA
	T_J = 25°C			6			8	mA
Quiescent Current Change	With Line: V_{IN} = 27V to 38V			0.8			1.0	mA
	V_{IN} = 28V to 38V, I_O = 1A, T_J = 25°C			0.8			1.0	mA
	With Load: I_O = 5mA to 1.0A			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, I_O = 1A, T_J = 25°C		2	2.5		2	2.5	V
Peak Output Current	T_J = 25°C		2.4			2.4		A
Short Circuit Current	T_J = 25°C		2.1			2.1		A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	56			50			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)			40			40	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		96			96		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

Note 1. All regulation tests are made at constant junction temperature with low duty cycle testing.
2. This test is guaranteed but is not tested in production.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
3-TERMINAL TO-3 METAL CAN K-PACKAGE	SG140A-XXK/883B SG140A-XXK SG240A-XXK SG340A-XXK SG140-XXK/883B SG140-XXK SG240-XXK SG340-XXK	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70C -55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
3-TERMINAL TO-66 METAL CAN R-PACKAGE	SG140A-XXR/883B SG140A-XXR SG240A-XXR SG340A-XXR SG140-XXR/883B SG140-XXR SG240-XXR SG340-XXR	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C -55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
3-PIN TO-39 METAL CAN T-PACKAGE	SG140A-XXT/883B SG140A-XXT SG340A-XXT SG140-XXT/883B SG140-XXT SG340-XXT	-55°C to 125°C -55°C to 125°C 0°C to 70°C -55°C to 125°C -55°C to 125°C 0°C to 70°C	
3-PIN HERMETIC TO-257 G-PACKAGE (Non-Isolated) 3-PIN HERMETIC TO-257 IG-PACKAGE (Isolated)	SG140A-XXG/883B SG140A-XXG SG140-XXG/883B SG140-XXG SG140A-XXIG/883B SG140A-XXIG SG140-XXIG/883B SG140-XXIG	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availability.
2. All parts are viewed from the top.
3. "XX" to be replaced by output voltage of specific fixed regulator.
4. Some products will be available in leadless chip carrier (LCC) and hermetic flat pack (F). Consult factory for price and availability

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SG150A/SG250A/SG350A
SG150/SG250/SG350

3 AMP POSITIVE ADJUSTABLE REGULATOR

DESCRIPTION

The SG150/150A series are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 3A over a 1.2V to 33V output range. They are exceptionally easy to use and require only 2 external resistors to set the output voltage. The SG150/150A series offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe operating area protection.

Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded.

Supplies needing electronic shutdown can be achieved by clamping the adjustment terminal to ground, which programs the output to 1.2V where most loads draw little current. Reference voltage, which is trimmed to be within ±1% at room temperature, is guaranteed to be within ±2% over all operating conditions for the "A" version and ±4% for the standard version. They are packaged in the hermetic TO-3 and TO-220 (Isolated and Non-Isolated).

FEATURES

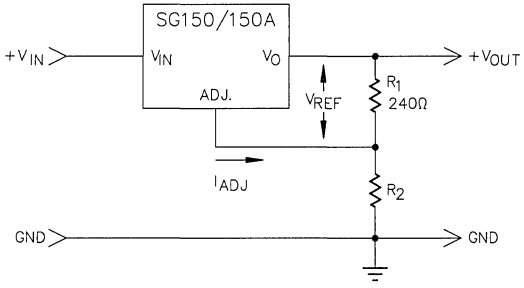
- **Trimmed ±1% reference voltage**
- **Adjustable output down to 1.2V**
- **Guaranteed 3A output current**
- **Line Regulation typically 0.1%**
- **Guaranteed thermal regulation**
- **Current limit constant with temperature**
- **86 dB ripple rejection**
- **Standard 3-lead transistor package**

HIGH RELIABILITY FEATURES - SG150A / SG150

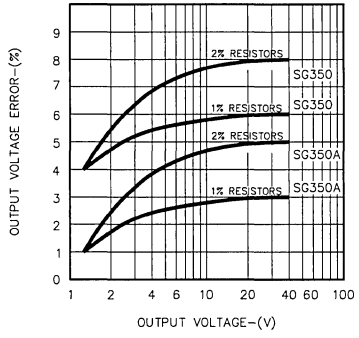
- **Available to MIL-STD-883 AND DESC SMD**
- **SG level "S" processing available**

4

PRECISION REGULATOR



OUTPUT VOLTAGE ERROR



April 1990

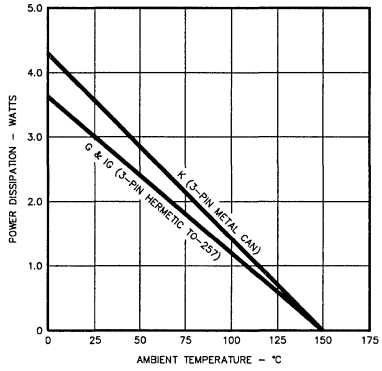
ABSOLUTE MAXIMUM RATINGS (Note 1)

Power Dissipation ..... Internally Limited
Input-Output Voltage Differential 35V
Storage Temperature Range ..... -65°C to 150°C

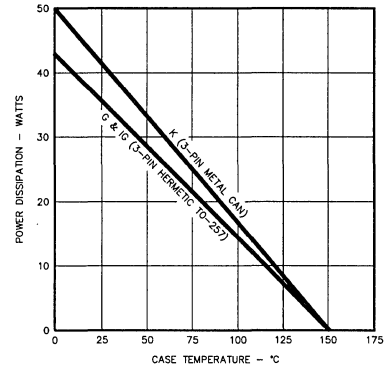
Operating Junction Temperature
Hermetic (K, G, IG-Packages) ..... 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Voltage Range ..... 3.0V to 30V

Operation Junction Temperature Range
SG150A/150 ..... -55°C to 150°C
SG250A/250 ..... -25°C to 150°C
SG350A/350 ..... 0°C to 125°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG150A/SG150 with $-55°C \le T_A \le 150°C$, SG250A/SG250 with $-25°C \le T_A \le 150°C$, SG350A/SG350 with $0°C \le T_A \le 125°C$ and $V_{IN} - V_{OUT} = 5V$, and $I_{OUT} = 1.5A$. Specifications are applicable for power dissipations up to 30W for the K package. Power dissipation is guaranteed at these values up to 15V input-output differential. Above 15V input-output differential power dissipation is limited by device internal protections circuitry. Low duty cycle pulse testing techniques are used which maintains junction and case temperature equal to the ambient temperature.)

Parameter	Test Conditions	SG150A/SG250A			SG150			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Voltage	I_{OUT} = 10mA T_J = 25°C	1.238	1.250	1.262				V
	3V ≤ (V_{IN} - V_{OUT}) ≤ 35V, P ≤ 30W, 10mA ≤ I_{OUT} ≤ 3A	1.225	1.250	1.270	1.20	1.25	1.30	V
Line Regulation	3V ≤ (V_{IN} - V_{OUT}) ≤ 35V, I_L = 10mA, T_A = 25°C		0.02	0.05		0.02	0.05	%/V
			0.005	0.01		0.005	0.01	%/V
Load Regulation (Note 3)	10mA ≤ I_{OUT} ≤ 3A							
	V_{OUT} ≤ 5V, T_A = 25°C		5	15		5	15	mV
	V_{OUT} ≥ 5V, T_A = 25°C		0.1	0.3		0.1	0.3	%
	V_{OUT} ≤ 5V		15	50		20	50	mV
	V_{OUT} ≥ 5V		0.3	1		0.3	1	%
Thermal Regulation	T_A = 25°C, 20ms pulse		0.002	0.01		0.002	0.01	%/W
Ripple Rejection	V_{OUT} = 10V, f =120Hz							
	C_{ADJ} = 0		65			65		dB
	C_{ADJ} = 10µF	66	86		66	86		dB
Adjust Pin Current			50	100		50	100	µA
Adjust Pin Current Change	10mA ≤ I_L ≤ 3A, 3V ≤ (V_{IN} - V_{OUT}) ≤ 35V		0.2	5		0.2	5	µA
Minimum Load Current	(V_{IN} - V_{OUT}) = 35V		3.5	5		3.5	5	mA
Current Limit	(V_{IN} - V_{OUT}) ≤ 10V	3	4.5		3	4.5		A
	(V_{IN} - V_{OUT}) = 30V	0.3	1		0.3	1		A

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG150A/SG250A			SG150			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Temperature Stability (Note 4)			1	2		1		%
Long Term Stability (Note 4)	T_A = 125°C		0.3	1		0.3	1	%
RMS Output Noise (% of V_{OUT})	T_A = 25°C, 10Hz ≤ f ≤ 10KHz		0.001			0.001		%

Parameter	Test Conditions	SG350A			SG350			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Voltage	I_{OUT} = 10mA T_J = 25°C	1.238	1.250	1.262				V
	3V ≤ (V_{IN} - V_{OUT}) ≤ 35V, P ≤ 30W,							
	10mA ≤ I_{OUT} ≤ 3A	1.225	1.250	1.270	1.20	1.25	1.30	V
Line Regulation	3V ≤ (V_{IN} - V_{OUT}) ≤ 35V, I_L = 10mA		0.02	0.05		0.02	0.07	%/V
	T_A = 25°C		0.005	0.01		0.005	0.03	%/V
Load Regulation (Note 3)	10mA ≤ I_{OUT} ≤ 3A							
	V_{OUT} ≤ 5V, T_A = 25°C		5	15		5	25	mV
	V_{OUT} ≥ 5V, T_A = 25°C		0.1	0.3		0.1	0.5	%
	V_{OUT} ≤ 5V		15	50		20	70	mV
	V_{OUT} ≥ 5V		0.3	1		0.3	1.5	%
Thermal Regulation	T_A = 25°C, 20ms pulse		0.002	0.01		0.002	0.03	%/W
Ripple Rejection	V_{OUT} = 10V, f =120Hz							
	C_{ADJ} = 0		65			65		dB
	C_{ADJ} = 10µF	66	86		66	86		dB
Adjust Pin Current			50	100		50	100	µA
Adjust Pin Current Change	10mA ≤ I_L ≤ 3A, 3V ≤ (V_{IN} - V_{OUT}) ≤ 35V		0.2	5		0.2	5	µA
Minimum Load Current	(V_{IN} - V_{OUT}) = 35V		3.5	10		3.5	10	mA
Current Limit	(V_{IN} - V_{OUT}) ≤ 10V	3	4.5		3	4.5		A
	(V_{IN} - V_{OUT}) = 30V	0.25	1		0.25	1		A
Temperature Stability (Note 4)			1	2		1		%
Long Term Stability (Note 4)	T_A = 125°C		0.3	1		0.3	1	%
RMS Output Noise (% of V_{OUT})	T_A = 25°C, 10Hz ≤ f ≤ 10KHz		0.001			0.001		%

Note 3. Regulation is measured at a constant T_A. Changes in output due to heating must be taken into account seperately. Pulse testing with low duty cycle is used.

Note 4. These parameters, although guaranteed are not tested in production.

APPLICATIONS INFORMATION

GENERAL

The SG150A develops a 1.25V reference voltage between the output and the adjustable terminal (see Figure 1). By placing a resistor, R_1, between these two terminals, a constant current is caused to flow through R_1 and down through R_2 to set the overall output voltage. Normally this current is the specified minimum load current of 5mA or 10mA.

Because I_{ADJ} is a very small and constant when compared with the current through R_1, it represents a small error and can usually be ignored. It is easily seen from the equation, that even if the resistors were of exact value, the accuracy of the output is limited by the accuracy of V_{REF}. Earlier adjustable regulators had a reference tolerance of ±4% which is dangerously close to the ±5% supply tolerance required in many logic and analog systems. Further, even 1% resistors can drift 0.01%/°C, adding additional error to the output voltage tolerance.

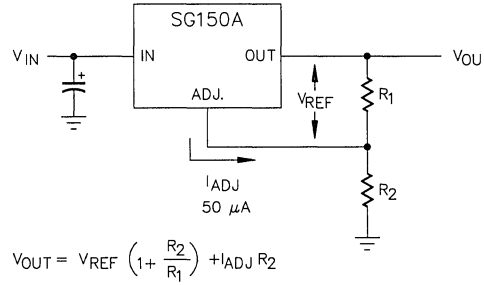


FIGURE 1 - BASIC ADJUSTABLE REGULATOR

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APPLICATIONS INFORMATION

BYPASS CAPACITORS

Input bypassing using a 1μF tantalum or 25μF electrolytic is recommended when the input filter capacitors are more than 5 inches from the device. Improved ripple rejection (80dB) can be accomplished by adding a 10μF capacitor from the adjust pin to ground. Increasing the size of the capacitor to 20μF will help ripple rejection at low output voltage since the reactance of this capacitor should be small compared to the voltage setting resistor, R_2. For improved AC transient response and to prevent the possibility of oscillation due to unknown reactive load, a 1μF capacitor is also recommended at the output. Because of their low impedance at high frequencies, the best type of capacitor to use is solid tantalum.

LOAD REGULATION

Because the SG150A is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the wire connecting the regulator to the load. The data sheet specification for load regulation is measured at the bottom of the package. Negative side sensing is a true Kelvin connection, with the bottom of the output divider returned to the negative side of the load. Although it may not be immediately obvious, best load regulation is obtained when the top of the resistor divider (R_2) is connected directly to the case, not the load.

This is illustrated in Figure 2. If R_1 were connected to the load, the effective resistance between the regulator and the load would be:

$$R_P \times \left(\frac{R_2 + R_1}{R_1}\right), \quad R_P = \text{Parasitic Line Resistance.}$$

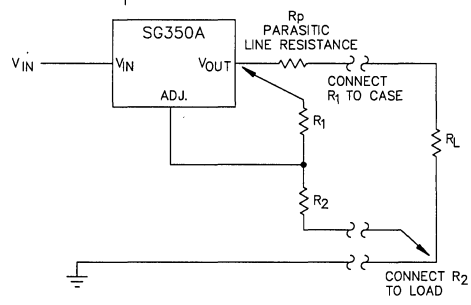


FIGURE 2 - CONNECTIONS FOR BEST LOAD REGULATION

Connected as shown, Rp is not multiplied by the divider ratio. Rp is about 0.004Ω per foot using 16 gauge wire. This translates to 4mV/ft. at a 1A load current, so it is important to keep the positive lead between regulator and load as short as possible, and use large wire or PC board traces.

TYPICAL APPLICATIONS

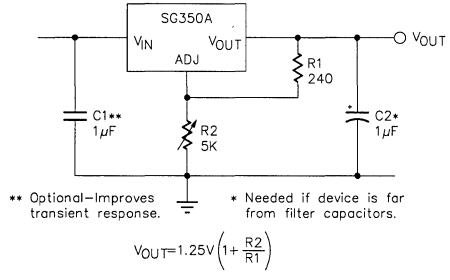


FIGURE 3 - 1.2V - 25V ADJUSTABLE REGULATOR

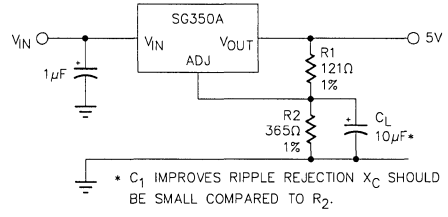


FIGURE 4 - IMPROVING RIPPLE REJECTION

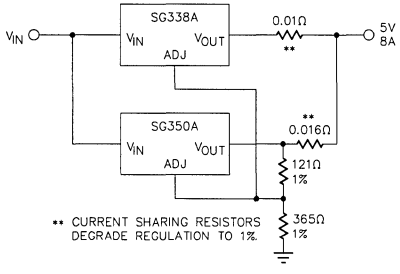


FIGURE 5 - PARALLEL REGULATORS FOR HIGHER CURRENT
(This circuit will not work with LM version devices.)

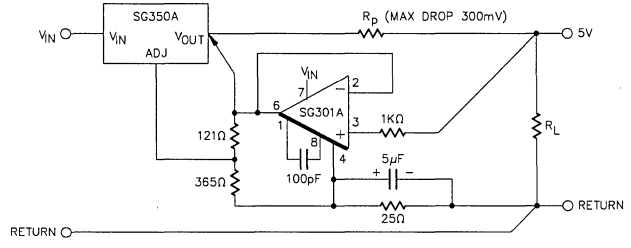


FIGURE 6 - REMOTE SENSING

TYPICAL APPLICATIONS (continued)

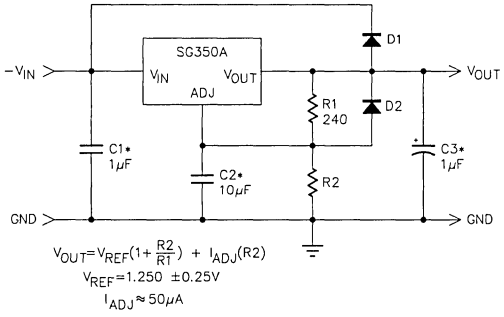


FIGURE 7 - BASIC REGULATOR WITH CAPACITORS* FOR INCREASED PERFORMANCE

* No external capacitors are required with the SG150A/150 but in some application, performance may be improved with added capacitance as follows:

C1. An input capacitor at 0.1μF will protect against problems when high impedance is present. The device can be more sensitive to input impedance when output or adjustment capacitors are used.

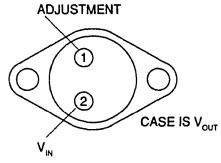
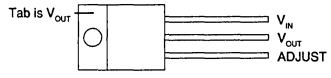
C2. Bypassing the adjustment terminal to ground with a 10μF capacitor will improve the ripple rejection by about 15dB.

C3. A 1μF tantalum capacitors on the output will improve transient response and keep the regulator from ringing due to tight capacitive loading.

In addition to external capacitors, it is sometimes good practice to add protection diodes D1 and D2 if there is a chance that a capacitor may discharge through the regulator IC.

Diode D1 protects against C3 with an input short.
Diode D2 protects against C2 with an output short.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
3-TERMINAL TO-3 METAL CAN K-PACKAGE	SG150AK/883B SG150AK SG250AK SG350AK SG150K/883B SG150K SG250K SG350K	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70C -55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
3-PIN HERMETIC TO-257 G-PACKAGE (Non-Isolated) 3-PIN HERMETIC TO-257 IG-PACKAGE (Isolated)	SG150AG/883B SG150AG SG150G/883B SG150G SG150AIG/883B SG150AIG SG150IG/883B SG150IG	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availability.
2. All parts are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

PRECISION VOLTAGE REGULATOR

DESCRIPTION

This monolithic voltage regulator is designed for use with either positive or negative supplies as a series, shunt, switching, or floating regulator with currents up to 150mA. Higher current requirements may be accommodated through the use of external NPN or PNP power transistors. This device consists of a temperature compensated reference amplifier, error amplifier, power series pass transistor, current limit, and remote shutdown circuitry.

The SG723 will operate over the full military ambient temperature range of -55°C to 125°C while the SG723C is designed for commercial applications of 0°C to 70°C.

FEATURES

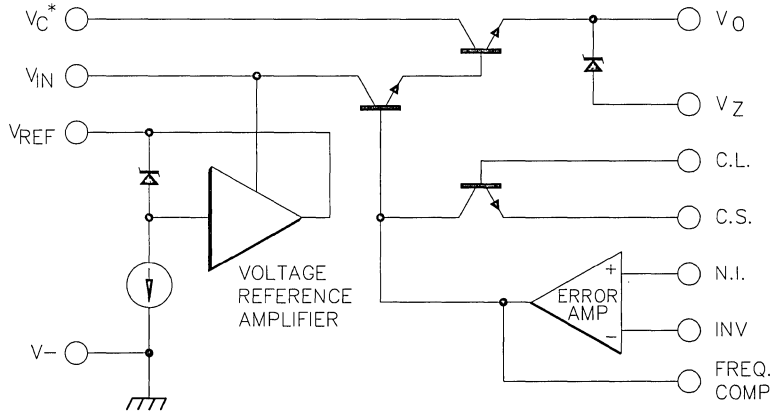
- **Positive or negative supply operation**
- **Series, shunt, switching or floating operation**
- **Low line and load regulation**
- **Output adjustable from 2V to 37V**
- **Output current to 150 mA**
- **Low standby current drain**
- **0.002%/°C average temperature variation**

HIGH RELIABILITY FEATURES - SG723

- **Available to MIL-STD-883 and DESC SMD**
- **MIL-M38510/10201BHA - JAN 723F**
- **MIL-M38510/10201BIA - JAN 723T**
- **MIL-M38510/10201BCA - JAN723J**
- **Radiation data available**
- **SG level "S" processing available**

4

BLOCK DIAGRAM



* V_C IS INTERNALLY CONNECTED TO V_{IN} FOR T PACKAGE.

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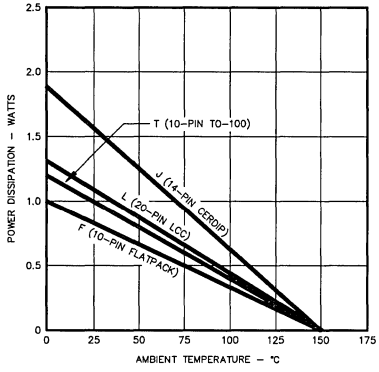
ABSOLUTE MAXIMUM RATINGS (Note 1)

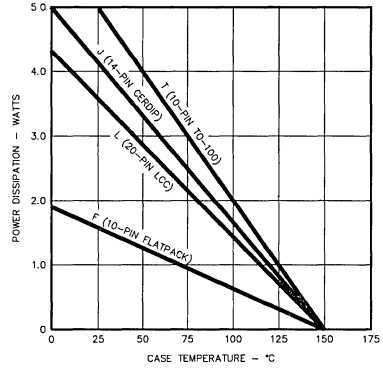
Pulse (50 ms) Input Voltage from V_{IN} to V- 50V
Continuous Input Voltage from V_{IN} to V- 40V
Input to Output Voltage Differential 40V
Maximum Output Current 150mA
Current from V_Z (J-Package only)..... 25 mA
Current from V_{REF}..... 15mA
Operating Junction Temperature
Hermetic (T, J, F, L-Packages)..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Voltage Range ..... (V_{OUT} +4.5V) to 38 V
Output Current Range ..... 5mA to 45mA
Reference Current..... 5mA
Zener Current (J-Package only)..... 5mA
Operating Ambient Temperature Range
SG723 ..... -55°C to 125°C
SG723C ..... 0°C to 70°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply for the operating ambient temperature of T_A = 25°C, V_{IN} = V_C = 12V, V- = 0V, V_{OUT} = 5V, I_L = 1 mA, R_{SC} = 0Ω, C_1 = 100pF, and divider impedance as seen by error amplifier ≤ 10KΩ. Low duty cycle pulse testing echniques are used which maintains junction and case temperatures equeal to the ambient temperature.)

Parameter	Test Conditions	SG723			SG723C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Voltage Range		9.5		40	9.5		40	V
Output Voltage Range		2.0		37	2.0		37	V
Input to Output Differential		3.0		38	3.0		38	V
Line Regulation (Note 3)	V_{IN} = 12V to 15V		0.01	0.1		0.01	0.1	$\%V_{OUT}$
	$T_A = T_{MIN}$ to T_{MAX}			0.3			0.3	$\%V_{OUT}$
	V_{IN} = 12V to 40V		0.02	0.2		0.1	0.5	$\%V_{OUT}$
Load Regulation (Note 3)	I_L = 1 to 50 mA		0.03	0.15		0.03	0.2	$\%V_{OUT}$
	$T_A = T_{MIN}$ to T_{MAX}			0.6			0.6	$\%V_{OUT}$
Ripple Rejection	f = 50 Hz to 10KHz							
	C_{REF} = 0		74			74		dB
	C_{REF} = 5μF		86			86		dB
Temperature Stability (Note 4)	$T_A = T_{MIN}$ to T_{MAX}		0.002	0.015		0.003	0.015	%/°C
Short Circuit Current Limit	R_{SC} = 10Ω		65			65		mA
Reference Voltage		6.95	7.15	7.35	6.80	7.15	7.50	V
Output Noise Voltage	BW = 100Hz to 10KHz							
	C_{REF} = 0		20			20		μV_{rms}
	C_{REF} = 5μF		2.5			2.5		μV_{rms}
Standby Current Drain	I_L = 0, V_{IN} = 30V		2.3	3.5		2.3	4.0	mA
Long Term Stability			0.1			0.1		%/Khr

Note 3. Applies for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

Note 4. These parameters, although guaranteed, are not tested in production.

CHARACTERISTIC CURVES

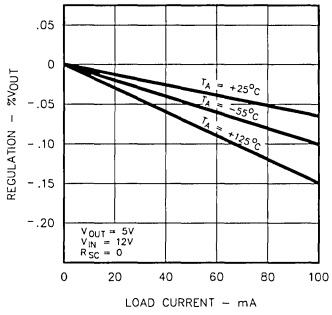


FIGURE 1.
LOAD REGULATION

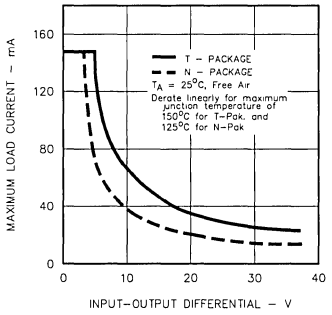


FIGURE 2.
MAXIMUM LOAD CURRENT

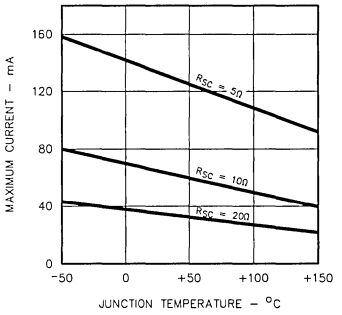


FIGURE 3.
CURRENT LIMITING CHARACTERISTICS

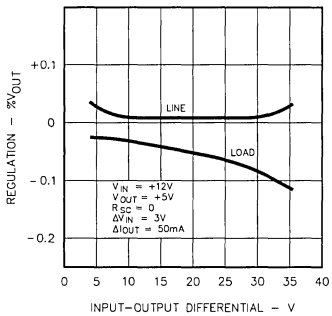


FIGURE 4.
REGULATION VS. INPUT-OUTPUT VOLTAGE REGULATION

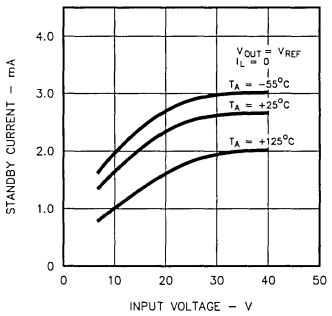


FIGURE 5.
STANDBY CURRENT DRAIN

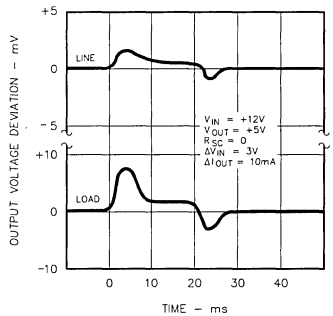


FIGURE 6.
TRANSIENT RESPONSE

APPLICATION INFORMATION

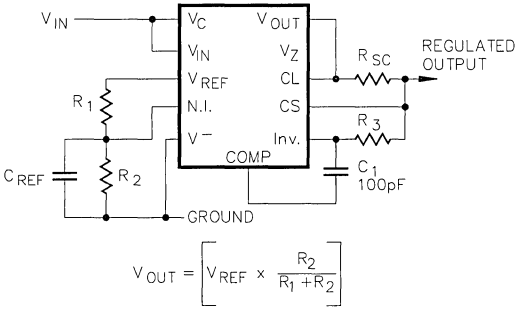


FIGURE 7 - BASIC LOW VOLTAGE REGULATOR
V_{OUT} = 2V TO 7 V

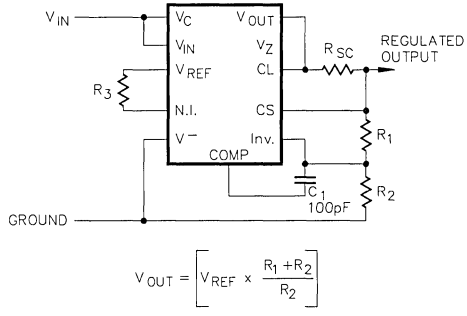
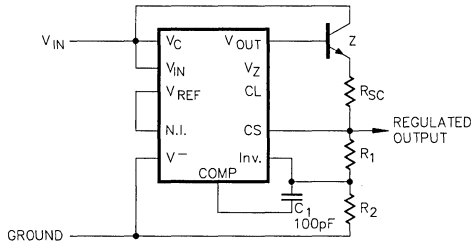


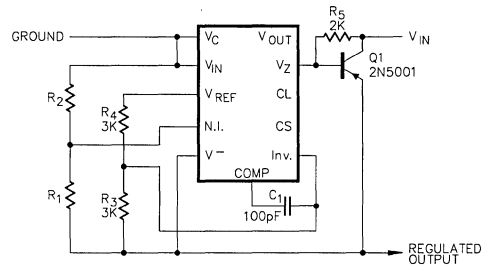
FIGURE 8 - BASIC HIGH VOLTAGE REGULATOR
V_{OUT} = 7V TO 37 V

APPLICATION INFORMATION (continued)



$$V_{OUT} = \left[V_{REF} \times \frac{R_1 + R_2}{R_2} \right]$$

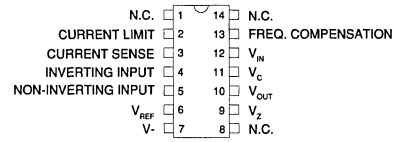
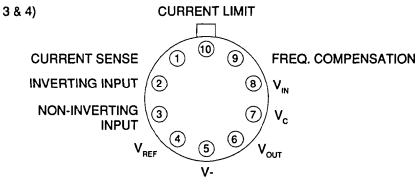
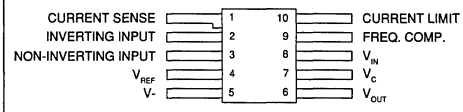
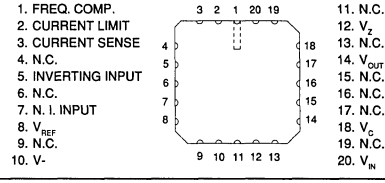
FIGURE 9 - HIGH CURRENT REGULATOR
EXTERNAL NPN TRANSISTOR I_L = 1.0A



$$V_{OUT} = \left[\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1} \right] ; R_3 = R_4$$

FIGURE 10 - NEGATIVE VOLTAGE REGULATOR

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN CERAMIC DIP J - PACKAGE	SG723J/883B SG723J SG723CJ	-55°C to 125°C -55°C to 125°C 0°C to 70°C	
10-PIN METAL CAN T - PACKAGE	SG723T/883B SG723T SG723CT	-55°C to 125°C -55°C to 125°C 0°C to 70°C	
10-PIN CERAMIC FLAT PACK F - PACKAGE	SG723F/883B SG723F	-55°C to 125°C -55°C to 125°C	
20-PIN CERAMIC LEADLESS CHIP CARRIER L- PACKAGE	SG723L/883B SG723L	-55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

Note 3. V_z output is not available in T, F-packages.
4. Pin 5 is connected to case.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

DUAL VOLTAGE TRACKING REGULATOR

DESCRIPTION

This circuit is a dual polarity tracking regulator designed to provide balanced positive and negative output voltages at currents up to 100mA. It is internally set for positive and negative 15 volt outputs but a single external adjustment can be used to change both outputs simultaneously from 10 to 23 volts. This device can be used with input voltages of up to ±35 volts and also has provision for adjustable current limiting, and utilization at currents in excess of two amps with the aid of external power transistors. A built-in sensing circuit monitors junction temperature and shuts down the regulator above 170°C eliminating the user's need for concern about power dissipation under short circuit conditions. The SG1501A will operate over the military ambient temperature range of -55°C to 125°C, while the SG2501A, SG3501A, and SG4501 are designed for commercial applications of 0°C to 70°C.

FEATURES

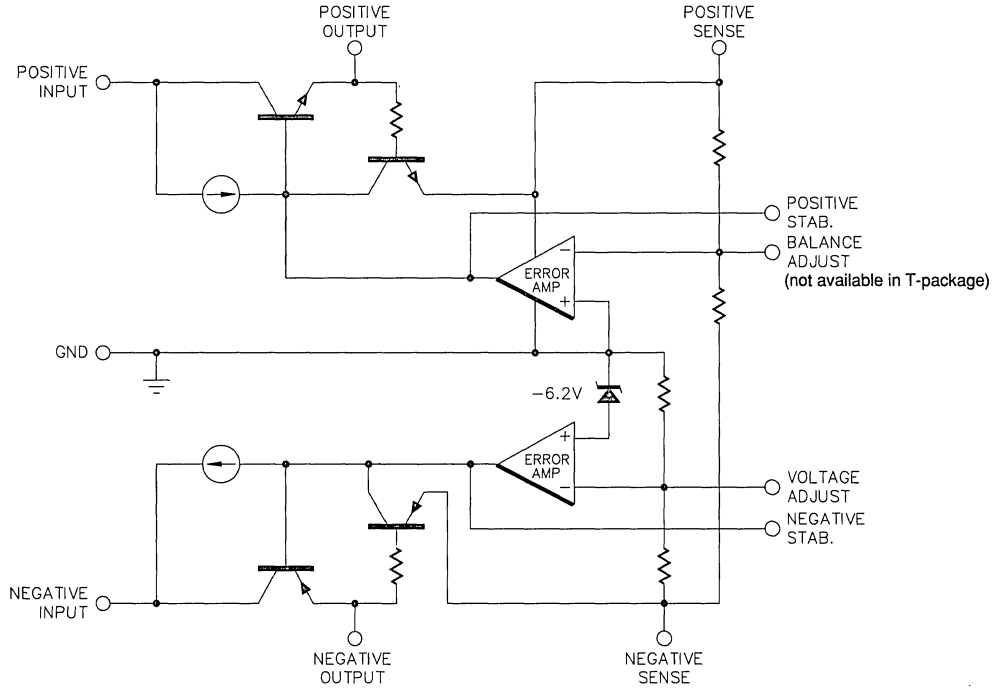
- **±15V tracking outputs**
- **Output currents to 100mA**
- **Internal thermal shutdown protection**
- **Precision line and load regulation**
- **1% maximum temperature variation**
- **Adjustable current limit**
- **±35V inputs**
- **Output adjustable from ±10V to ±23V**

HIGH RELIABILITY FEATURES - SG1501A

- **Available to MIL-STD-883**
- **SG level "S" processing available**

4

BLOCK DIAGRAM



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See Application Notes for additional information.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage from V+ to V-
- SG1501A, SG2501A 70V
- SG3501A, SG4501 ..... 60V

Maximum Load Current 100mA

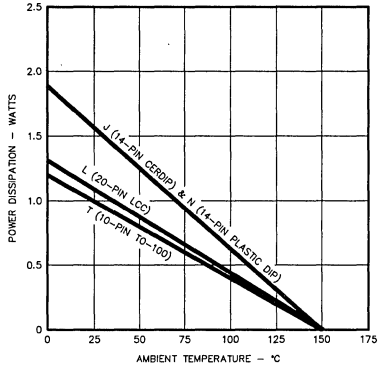
Operating Junction Temperature
- Hermetic (J, T, L - Packages) ..... 150°C
- Plastic (N - Packages) ..... 150°C

Storage Temperature Range ..... -65°C to 150°C

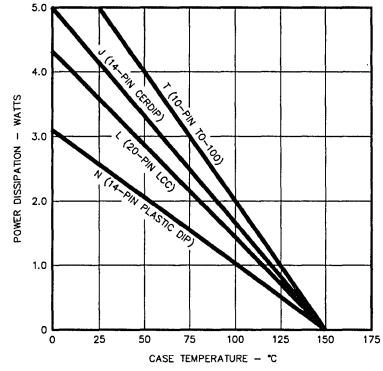
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Voltage from V+ to V-
- SG1501A, SG2501A 60V
- SG3501A, 4501 ..... 50V

Output Current ..... 0 to 50mA

Input - Output Differential (minimum) 4V

Operating Ambient Temperature Range (T_J)
- SG1501A ..... -55°C to 125°C
- SG2501A, SG3501A, SG4501 ..... 0°C to 70°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise stated, these specifications apply for the operating ambient temperature of T_A = 25°C, V_{IN} = ±20V, V_{OUT} = ±15V, I_L = 0, R_{SC} = 0Ω, C_1 = C_2 = 0.01µF, C_3 = C_4 = 1.0µF, and VOLTAGE ADJUSTMENT pin open. All specifications apply to both positive and negative sides of the regulator, either singly or together. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1501A/2501A			SG3501A			SG4501			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage		14.8	15	15.2	14.5	15	15.5	14.25		15.75	V
Input Voltage				±35			±30			±30	V
Input - Output Differential	R_{SC} = 0, I_L = 50mA	2			2			2			V
Output Voltage Balance			50	150		50	300		50	300	mV
Line Regulation	V_{IN} = 17V to V_{MAX}, T_A = T_{MIN} to T_{MAX}		4	20		4	20		4	20	mV
Load Regulation	I_L = 0mA to 50mA, T_A = T_{MIN} to T_{MAX}		5	30		5	30		5	30	mV
Output Voltage Range	Voltage adjust circuit	10		23	10		23	10		23	V
Input Voltage Range	10V Output	12		35	12		30	12		30	V
Ripple Rejection	f = 120Hz		75			75			75		dB
Temperature Stability (Note 3)	T_A = T_{MIN} to T_{MAX}		0.3	1.0		0.3	1.0		0.3	1.0	%
Short Circuit Current Limit	R_{SC} = 10Ω		60			60			60		mA
Output Noise Voltage	BW = 100Hz to 10KHz		50			50			50		μV_{rms}
Positive Standby Current	I_L = 0		2	4		2	4		2	4	mA
Negative Standby Current	I_L = 0		3	5		3	5		3	5	mA
Long Term Stability			0.1			0.1			0.1		%/KHr

Note 3. These parameters, although guaranteed, are not tested in production.

CHARACTERISTIC CURVES

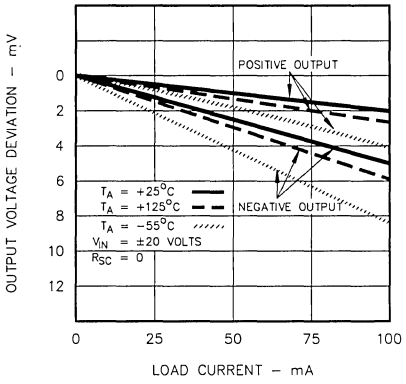


FIGURE 1.
LOAD REGULATION

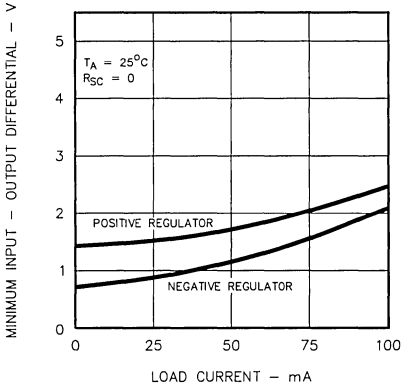


FIGURE 2.
REGULATOR DROPOUT VOLTAGE

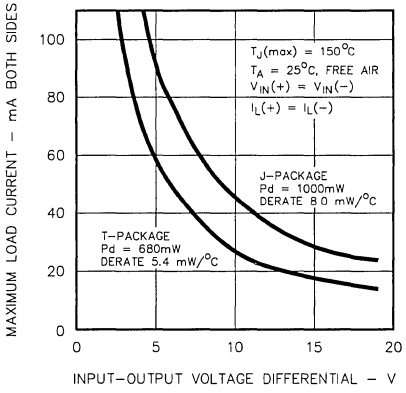


FIGURE 3.
MAXIMUM CURRENT CAPABILITY

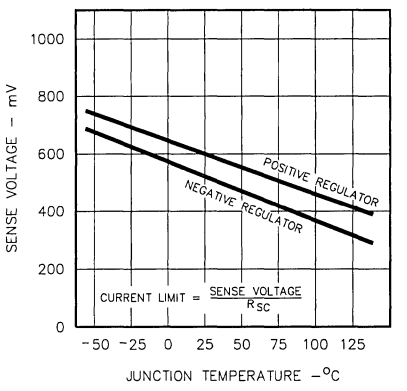


FIGURE 4.
CURRENT LIMITING CHARACTERISTICS

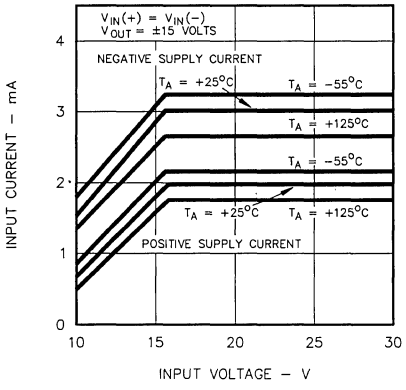


FIGURE 5.
STANDBY CURRENT DRAIN

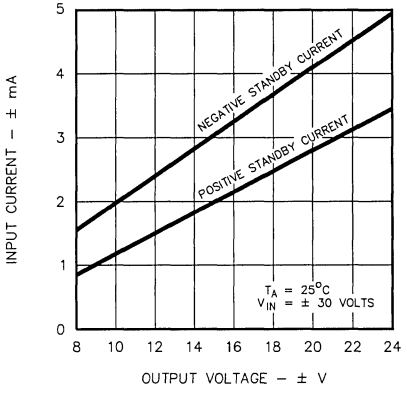


FIGURE 6.
STANDBY CURRENT DRAIN

CHARACTERISTIC CURVES

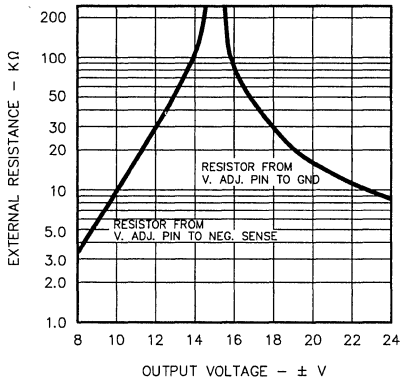


FIGURE 7.
EXTERNAL PARALLEL RESISTOR REQUIRED FOR VOLTAGES OTHER THAN ±15 VOLTS

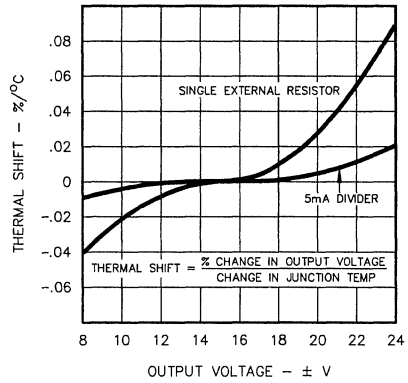


FIGURE 8.
TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE

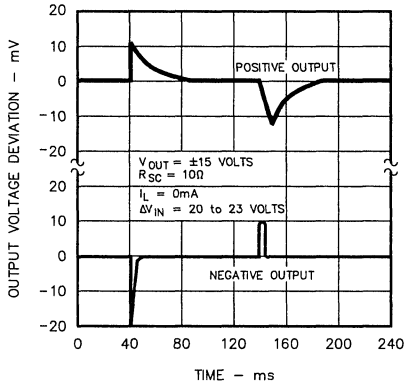


FIGURE 9.
LINE TRANSIENT RESPONSE

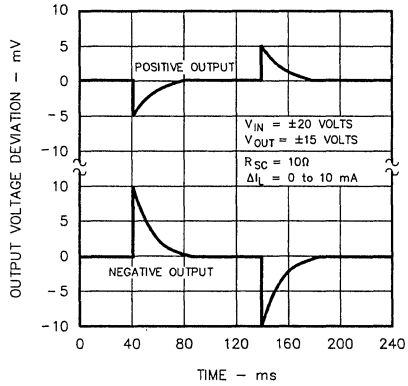


FIGURE 10.
LOAD TRANSIENT RESPONSE

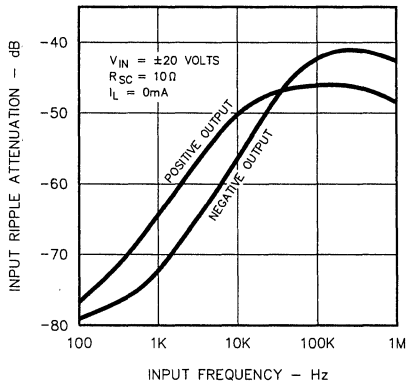


FIGURE 11.
RIPPLE REJECTION

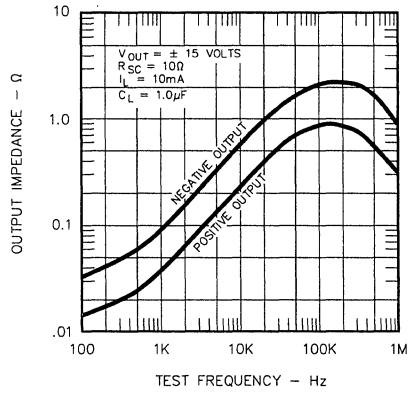


FIGURE 12.
OUTPUT IMPEDANCE

TYPICAL APPLICATIONS

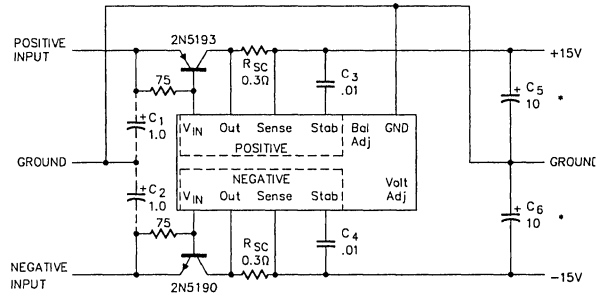


FIGURE 13 - HIGH CURRENT CONFIGURATION, ONE AMP OUTPUT

For full power output, the external transistors must be mounted on adequate heat sinks. Selection of power transistors may be made on the basis of current and voltage capability with low-frequency devices preferred to minimize the risk of oscillation. In this circuit, the value of Rsc is selected in order to protect the pass transistors rather than the IC. C1 and C2 are only necessary if high line impedance is present.

4

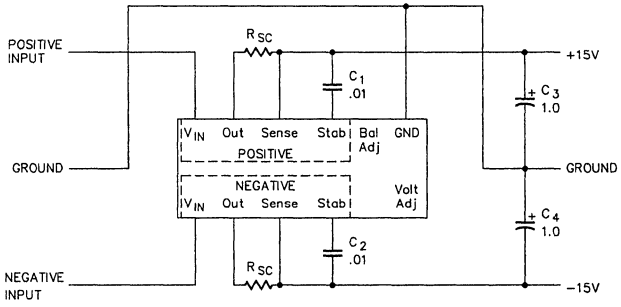


FIGURE 14 - BASIC ±15 V, 50mA REGULATOR

Additional reduction in output noise voltage may be achieved with larger values for C1 and C2 although there is some loss in frequency response. C3 and C4 may also be increased to improve load transient characteristics. Note that the case is common to $-V_{IN}$, not ground.

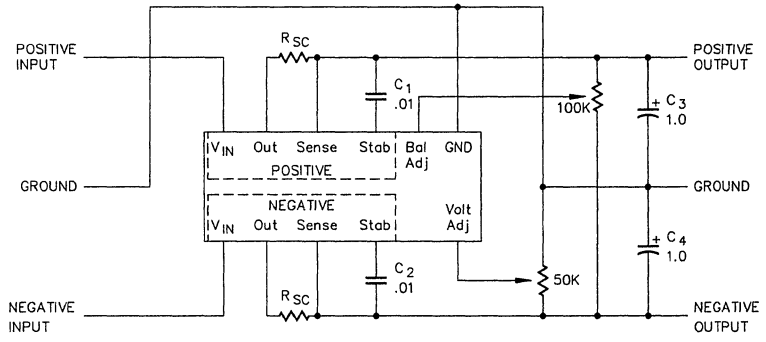


FIGURE 15 - ADJUSTMENT OF VOLTAGE LEVELS

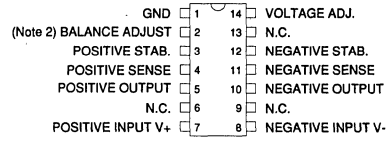
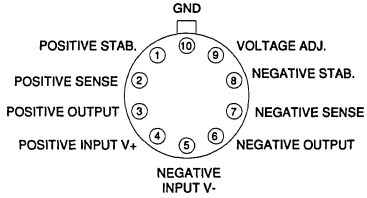
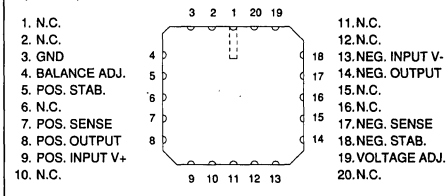
Greater resolution may be achieved by padding each of the potentiometer with fixed resistors. Also, a single resistor, rather than a divider, may be used when adjustment in only one direction is required, but some degradation in temperature coefficient results (see temperature coefficient of output voltage curve).

APPLICATION NOTE

Although the SG1501A series contains thermal limiting circuitry, the maximum current must still be controlled to allow time for this protection to react. Therefore, without external pass transistors, the minimum value for R_{SC} is three ohms. R_{SC} can, of course, have a larger value in order to protect a load.

Under some conditions, a low-level oscillation may be present on the negative side when the device goes into current limiting. Should this be a problem, it may be eliminated by by-passing R_{SC} with a capacitor whose value is such that the time constant, R_{SC} C, is equal to 10 x 10^{-6} second. This capacitor, as well as the output capacitors, C3 and C4, must be low ESR types such as solid tantalum.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Note Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN CERAMIC DIP J - PACKAGE	SG1501AJ/883B SG1501AJ SG2501AJ SG3501AJ SG4501T	-55°C to 125°C -55°C to 125°C 0°C to 70°C 0°C to 70°C 0°C to 70°C	
14-PIN PLASTIC DIP N - PACKAGE	SG2501AN SG3501AN SG4501N	0°C to 70°C 0°C to 70°C 0°C to 70°C	
10-PIN TO-100 METAL CAN T-PACKAGE	SG1501AT/883B SG1501AT SG2501AT SG3501AT SG4501T	-55°C to 125°C -55°C to 125°C 0°C to 70°C 0°C to 70°C 0°C to 70°C	
20-PIN CERAMIC LEADLESS CHIP CARRIER L - PACKAGE	SG1501AL/883B SG1501AL	-55°C to 125°C -55°C to 125°C	(Note 3) 

Note 1. All packages are viewed from the top.
Note 2. The Balance Adjust function is not available in the "T" package.
Note 3. The Negative Input (V-) pin is internally connected to the case.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

ADJUSTABLE DUAL VOLTAGE REGULATOR

DESCRIPTION

This circuit is identical to the SG1501 series of dual polarity tracking regulators except that the internal voltage setting resistors are not included and the current limit inputs have been disconnected from the pass transistors. While this circuit does require external divider resistors, maximum versatility of offered in adjusting the output voltage levels, and additional current-limit inputs ease the application of fold-back current limiting. In all other respects, this circuit performs as the SG1501.

FEATURES

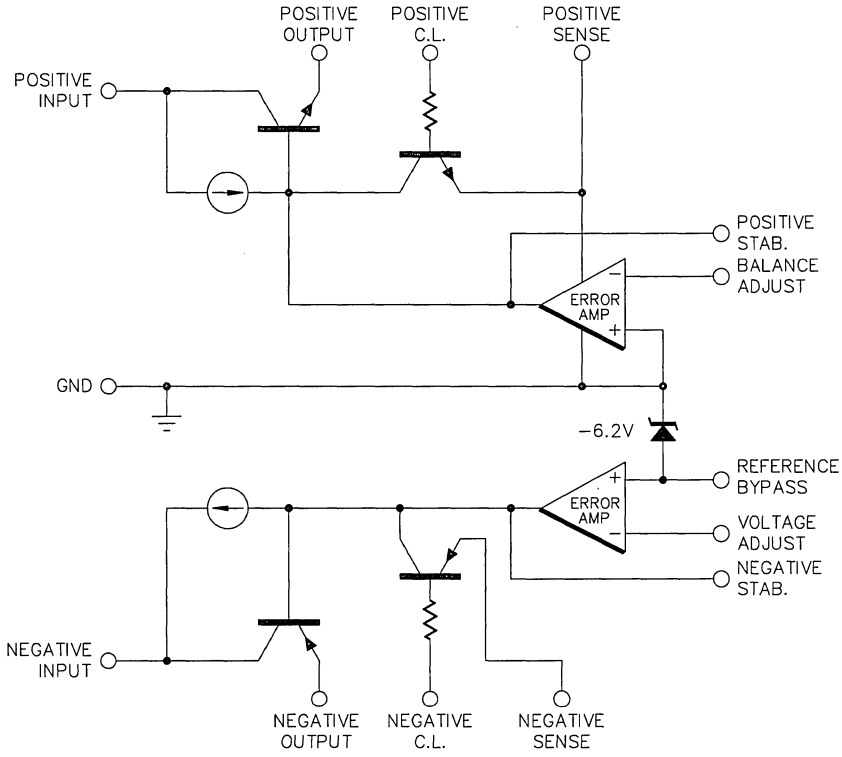
- **Positive and negative output voltage independently adjustable from 10V to 28V**
- **Output currents to 100mA**
- **Line and load regulation of 0.1%**
- **1% maximum temperature variation**
- **Standby current drain only 3mA**
- **Internal thermal shutdown protection**

HIGH RELIABILITY FEATURES - SG1502

- **Available to MIL-STD-883**
- **SG level "S" processing available**

4

BLOCK DIAGRAM



April 1990

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage from V+ to V-
- SG1502, SG2502 ..... 60V
- SG3502 ..... 50V

Maximum Load Current 100mA

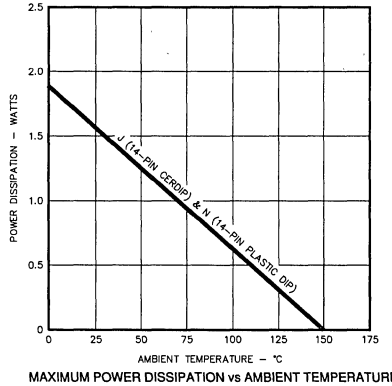
Operating Junction Temperature
- Hermetic (J Package) ..... 150°C
- Plastic (N Package) ..... 150°C

Storage Temperature Range ..... -65°C to 150°C

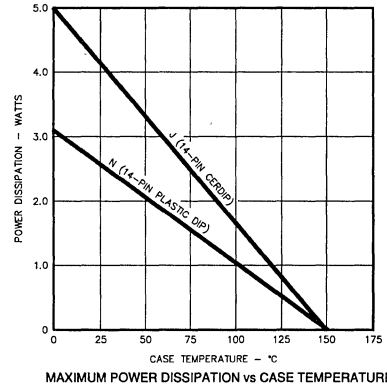
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Voltage from V+ to V-
- SG1502, SG2502 ..... 50V
- SG3502 ..... 40V

Output Current ..... 0 to 50mA

Input - Output Differential (minimum) 4V

Operating Ambient Temperature Range (T_A)
- SG1502 ..... -55°C to 125°C
- SG2502, SG3502 ..... 0°C to 70°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise stated, these specifications apply for the operating ambient termperature of T_A = 25°C, V_{IN} = ±20V, V_{OUT} = ±15V, I_L = 0, R_{SC} = 0Ω, $C_1 = C_2$ = 0.01µF, and $C_3 = C_4$ = 1.0µF. All specifications apply to both positive and negative sides of the regulator, either singly or together. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1502/2502			SG3502			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Voltage Range		12		30	12		25	V
Output Voltage Range		10		28	10		23	V
Input - Output Differential		2			2			V
Line Regulation	ΔV_{IN} = 10V		0.02	0.1		0.02	0.1	$\%V_{OUT}$
	$T_A = T_{MIN}$ to T_{MAX}		0.04	0.2		0.04	0.2	$\%V_{OUT}$
Load Regulation	I_L = 0mA to 50mA		0.02	0.1		0.02	0.1	$\%V_{OUT}$
	$T_A = T_{MIN}$ to T_{MAX}		0.03	0.3		0.02	0.3	$\%V_{OUT}$
Temperature Stability (Note 3)	$T_A = T_{MIN}$ to T_{MAX}		0.3	1.0		0.3	1.0	$\%V_{OUT}$
Current Limit Sense Voltage			0.6			0.6		V
Reference Voltage		6.3		6.6	6.2		6.8	V
Ripple Rejection	f = 120Hz		75			75		dB
Output Noise Voltage	BW = 100Hz to 10KHz		50			50		μV_{rms}
Positive Standby Current	Divider 1 = 0.5mA (Note 4)		2	3		2	3	mA
Negative Standby Current	Divider 1 = 0.5mA (Note 4)		3	4		3	4	mA
Long Term Stability			0.1			0.1		%/KHr

Note 3. These parameters, although guaranteed, they are not tested in production.
Note 4. "Divider 1" refers to R_1 , R_2 resistor divider. (See Figure 7)

CHARACTERISTIC CURVES

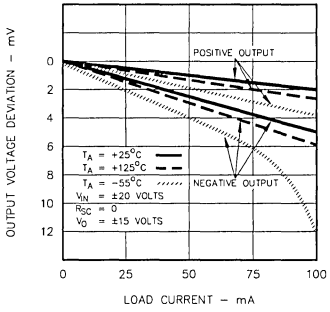


FIGURE 1.
LOAD REGULATION

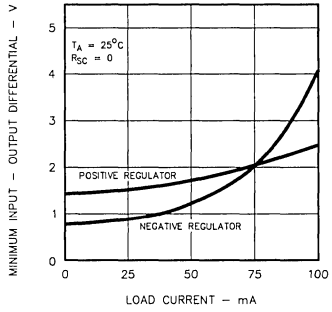


FIGURE 2.
REGULATOR DROPOUT VOLTAGE

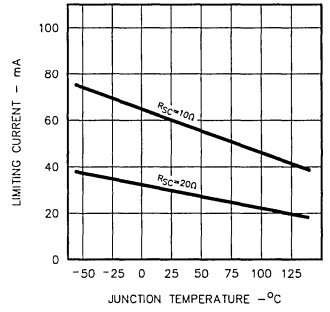


FIGURE 3.
CURRENT LIMITING CHARACTERISTICS

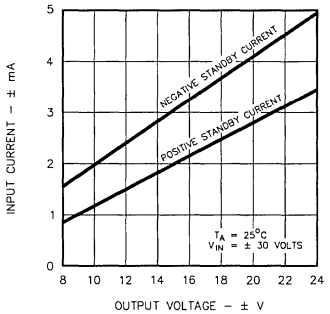


FIGURE 4.
STANDBY CURRENT DRAIN

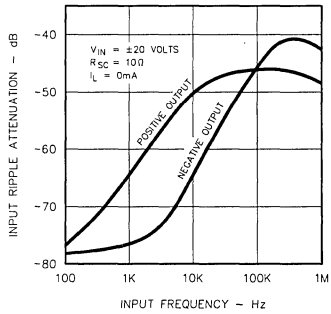


FIGURE 5.
RIPPLE REJECTION

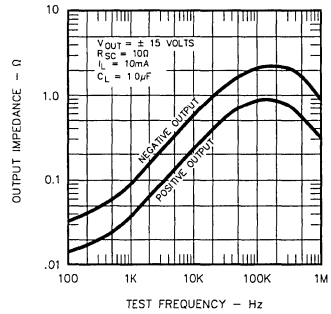
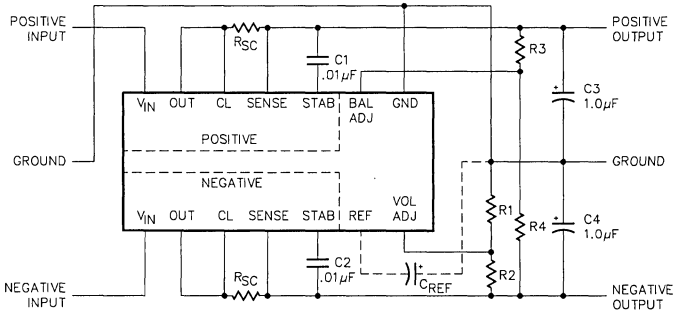


FIGURE 6.
OUTPUT IMPEDANCE

TYPICAL APPLICATIONS



NEGATIVE $V_O = \frac{6.2(R1+R2)}{R1}$, POSITIVE $V_O = \frac{R3}{R4}$ NEGATIVE V_O

FIGURE 7 - BASIC REGULATOR CIRCUIT

For best temperature performance, the parallel impedance of R1 and R2 should be 6.3K ohm while that of R3 and R4 should be 10 K. Increasing the value of C1 and C2 will reduce the frequency response while transient response may be improved by increasing C3 and C4. For very low-noise applications, a 4.7μF capacitor for C_{REF} may be added. R_{SC} is selected such that a sense voltage of 0.6 volts (at T_J = 25°C) is developed at the maximum load current desired.

TYPICAL APPLICATIONS (continued)

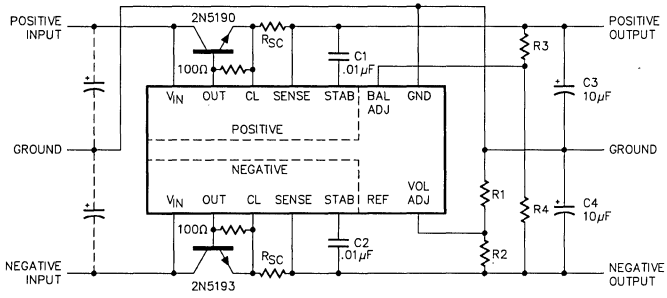


FIGURE 8 - HIGH CURRENT CONFIGURATION

Power transistors should be selected on the basis of current and voltage requirements with low-frequency devices preferred to minimize the risk of oscillation. Input capacitors (0.1μF to 1.0μF) may be required if the circuit is located remote from the power supply filter. The common-collector configuration here has the advantage of allowing the use of separate collector voltages for the pass transistors but the common-emitter configuration shown below may also be used. In fact, one configuration on the positive side and the other on the negative side will allow the use of all NPN or all PNP power transistors.

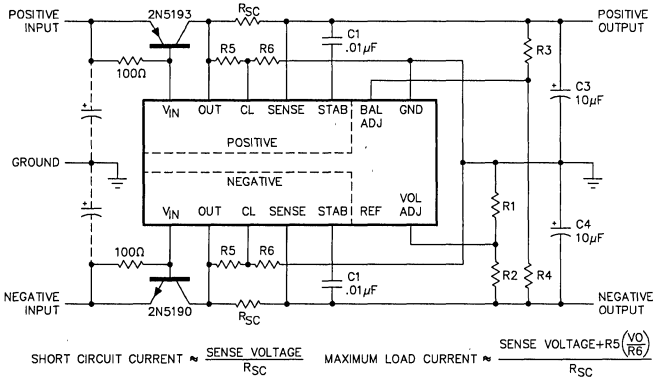
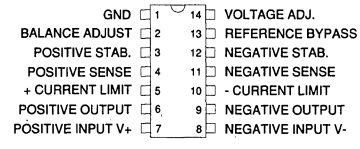


FIGURE 9 - FOLDBACK CURRENT LIMITING

The use of R5 and R6 to provide fold-back current limiting is possible with either common-emitter or common-collector configurations. The values for R5 and R6 are determined by an iterative solution of the equations shown with the trade-off being that a greater amount of fold-back requires a larger voltage drop a cross R_{SC}. Note that in the common-emitter configuration, the 100Ω base - to emitter resistors must provide a path for the regulator stand-by current and should not be increased in value.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Note Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN CERAMIC DIP J - PACKAGE	SG1502J/883B SG1502J SG2502J SG3502J	-55°C to 125°C -55°C to 125°C 0°C to 70°C 0°C to 70°C	
14-PIN PLASTIC DIP N - PACKAGE	SG2502N SG3502N	0°C to 70°C 0°C to 70°C	



Note 1. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

REGULATING PULSE WIDTH MODULATOR

DESCRIPTION

This monolithic integrated circuit contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual-in-line package is the voltage reference, error amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches and current limiting and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer coupled DC to DC converters, transformerless voltage doublers and polarity converters, as well as other power applications. The SG1524 is specified for operation over the full military ambient temperature range of -55°C to +125°C, the SG2524 for -25°C to +85°C, and the SG3524 is designed for commercial applications of 0°C to +70°C.

FEATURES

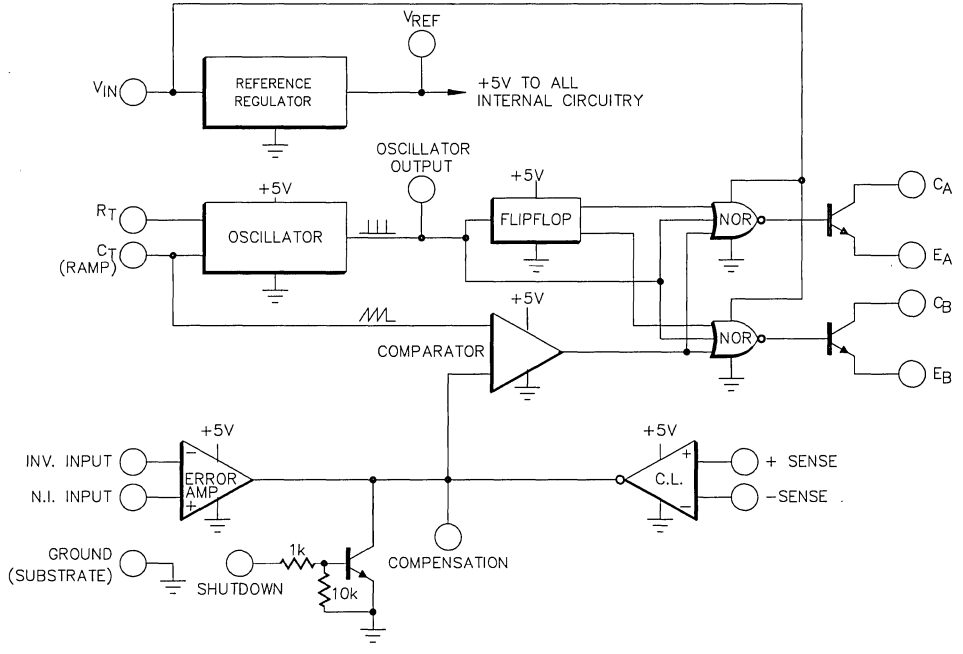
- **8V to 40V operation**
- **5V reference**
- **Reference line and load regulation of 0.4%**
- **Reference temperature coefficient < ± 1%**
- **100Hz to 300KHz oscillator range**
- **Excellent external sync capability**
- **Dual 50mA output transistors**
- **Current limit circuitry**
- **Complete PWM power control circuitry**
- **Single ended or push-pull outputs**
- **Total supply current less than 10mA**

HIGH RELIABILITY FEATURES - SG1524

- **Available to MIL-STD-883B and DESC SMD**
- **MIL-M-38510/12601BEA - JAN1524J**
- **Radiation data available**
- **SG level "S" processing available**

4

BLOCK DIAGRAM



April 1990

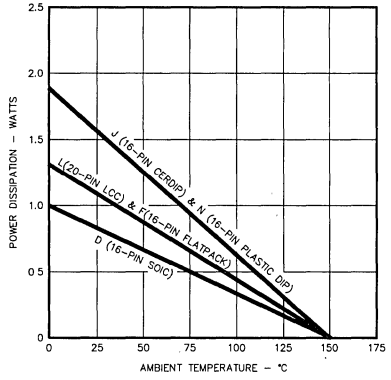
See Application Notes for additional information.

ABSOLUTE MAXIMUM RATINGS (Note 1)

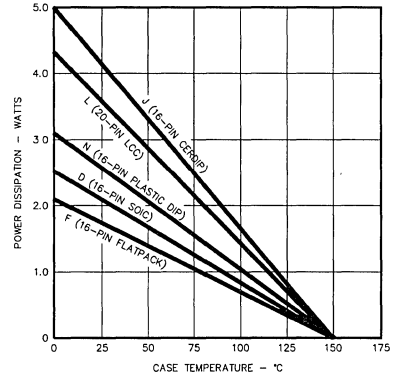
Input Voltage ($+V_{IN}$) 42V
Collector Voltage 40V
Logic Inputs ..... -0.3V to 5.5V
Current Limit Sense Inputs ..... -0.3V to 0.3V
Output Current (each transistor) 100mA
Reference Load Current 50mA
Oscillator Charging Current 5mA
Operating Junction Temperature
Hermetic (J, F, L Packages) ..... 150°C
Plastic (N, DW Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1. Values beyond which damage may occur.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Voltage ($+V_{IN}$) ..... 8V to 40V
Collector Voltage ..... 0V to 40V
Error Amp Common Mode Range ..... 1.8V to 3.4V
Current Limit Sense Common Mode Range ..... -0.3V to 0.3V
Output Current (each transistor) ..... 0 to 50mA
Reference Load Current ..... 0 to 20mA
Oscillator Charging Current ..... 30µA to 2mA
Oscillator Frequency Range ..... 100Hz to 300KHz
Oscillator Timing Resistor (R_T) ..... 1.8KΩ to 100KΩ
Oscillator Timing Capacitor (C_T) ..... 1nF to 1.0µF
Operating Ambient Temperature Range
SG1524 ..... -55°C to 125°C
SG2524 ..... -25°C to 85°C
SG3524 ..... 0°C to 70°C

Note 2: Range over which the device is functional and parameter limits are guaranteed.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1524 with $-55°C \le T_A \le 125°C$, SG2524 with $-25°C \le T_A \le 85°C$, SG3524 with $0°C \le T_A \le 70°C$, and $+V_{IN} = 20V$. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1524/2524			SG3524			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Section (Note 3)								
Output Voltage	$T_J = 25°C$	4.80	5.00	5.20	4.60	5.00	5.40	V
Line Regulation	$V_{IN} = 8V$ to 40V			20			30	mV
Load Regulation	$I_L = 0$ to 20mA			50			50	mV
Temperature Stability (Note 7)	Over Operating Temperature Range			50			50	mV
Total Output Voltage Range (Note 7)	Over Line, Load and Temperature	4.80		5.20	4.60		5.40	V
Short Circuit Current	$V_{REF} = 0V$	25	50	150	25	50	150	mA

Note 3. $I_L = 0mA$

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1524/2524			SG3524			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Oscillator Section (Note 4)								
Initial Accuracy	T_J = 25°C	36	40	44	36	40	44	KHz
	MIN ≤ T_J ≤ MAX	34		46	34		46	KHz
Voltage Stability	V_{IN} = 8V to 40V		0.1	1		0.1	1	%
Maximum Frequency	R_T = 2KΩ, C_T = 1nF	200	400		200	400		KHz
Sawtooth Peak Voltage	V_{IN} = 40V	3		3.8	3		3.8	V
Sawtooth Valley Voltage	V_{IN} = 8V	0.6	1	1.2	0.6	1	1.2	V
Clock Amplitude		3.2			3.2			V
Clock Pulse Width		0.3		1.5	0.3		1.5	µs
Error Amplifier Section (Note 5)								
Input Offset Voltage	R_S ≤ 2KΩ		0.5	5		2	10	mV
Input Bias Current			1	10		1	10	µA
Input Offset Current				1			2	µA
DC Open Loop Gain	R_L ≥10MΩ, T_J = 25°C	72			60			dB
Output Low Level	$V_{PIN\,1}$ - $V_{PIN\,2}$ ≥ 150mV		0.2	0.5		0.2	0.5	V
Output High Level	$V_{PIN\,2}$ - $V_{PIN\,1}$ ≥150mV	3.8	4.2		3.8	4.2		V
Common Mode Rejection	V_{CM} = 1.8V to 3.4V	70						dB
Supply Voltage Rejection	V_{IN} = 8V to 40V	55						dB
Gain-Bandwidth Product (Note 7)	T_J = 25°C	1	2		1	2		MHz
P.W.M. Comparator (Note 4)								
Minimum Duty Cycle	V_{COMP} = 0.5V			0			0	%
Maximum Duty Cycle	V_{COMP} = 3.6V	45	49		45	49		%
Current Limit Amplifier Section (Note 6)								
Sense Voltage	T_J = 25°C	190	200	210	180	200	220	mV
Input Bias Current				200			200	µA
Shutdown Section								
Threshold Voltage	T_J = 25°C	0.5	0.8	1.2	0.5	0.8	1.2	V
	MIN ≤ T_J ≤ MAX	0.2		1.8	0.2		1.8	V
Output Section (each transistor)								
Collector Leakage Current	V_{CE} = 40V			50			50	µA
Collector Saturation Voltage	I_C = 50mA			2			2	V
Emitter Output Voltage	I_E = 50mA	17			17			V
Collector Voltage Rise Time	R_C = 2KΩ			0.4			0.4	µs
Collector Voltage Fall Time	R_C = 2KΩ			0.2			0.2	µs
Power Consumption								
Standby Current	V_{IN} = 40V		7	10		7	10	mA

Note 4. F_{OSC} = 40KHz (R_T = 2.9KΩ, C_T = .01µF)
Note 5. V_{CM} = 2.5V
Note 6. V_{CM} = 0V
Note 7. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

APPLICATION NOTES

OSCILLATOR

The oscillator in the SG1524 uses an external resistor R_T to establish a constant charging current into an external capacitor C_T. While this uses more current than a series-connected RC, it provides a linear ramp voltage at C_T which is used as a time-dependent reference for the PWM comparator. The charging current is equal to $3.6V/R_T$, and should be restricted to between 30µA and 2mA. The equivalent range for R_T is 1.8K to 100K.

The range of values for C_T also has limits, as the discharge time of C_T determines the pulse width of the oscillator output pulse. The pulse is used (among other things) as a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. This output deadtime relationship is shown in Figure 1. A pulse width below 0.35 microseconds may cause failure of the internal flip-flop to toggle. This restricts the minimum value of C_T to 1000pF. (Note: Although the oscillator output is a convenient oscilloscope sync input, the probe capacitance will increase the pulse width and decrease the oscillator frequency slightly.) Obviously, the upper limit to the pulse width is determined by the modulation range required in the power supply at the chosen switching frequency. Practical values of C_T fall between 1000pF and 0.1µF, although successful 120 Hz oscillators have been implemented with values up to 5µF and a series surge limit resistor of 100 ohms.

The oscillator frequency is approximately $1/R_T \cdot C_T$; where R is in ohms, C is in microfarads, and the frequency is in Megahertz. For greater accuracy, the chart in Figure 2 may be used for a wide range of operating frequencies.

Note that for buck regulator topologies, the two outputs can be wire-ORed for an effective 0-90% duty cycle range. With this connection, the output frequency is the same as the oscillator frequency. For push-pull applications, the outputs are used separately; the flip-flop limits the duty cycle range at each output to 0-45%, and the effective switching frequency at the transformer is 1/2 the oscillator frequency.

If it is desired to synchronize the SG1524 to an external clock, a positive pulse may be applied to the clock pin. The oscillator should be programmed with R_T and C_T values that cause it to free-run at 90% of the external sync frequency. A sync pulse with a maximum logic 0 of +0.3 volts and a minimum logic 1 of +2.4 volts applied to Pin 3 will lock the oscillator to the external source. The minimum sync pulsewidth should be 200 nanoseconds, and the maximum is determined by the required deadtime. The clock pin should never be driven more negative than -0.3 volts, nor more positive than +5.0 volts. The nominal resistance to ground is 3.2K at the clock pin, ±25% over temperature.

If two or more SG1524s must be synchronized together, program one master unit with R_T and C_T for the desired frequency. Leave the R_T pins on the slaves open, connect the C_T pins to the C_T of the master, and connect the clock pins to the clock pin of the master. Since C_T is a high-impedance node, this sync technique works best when all devices are close together.

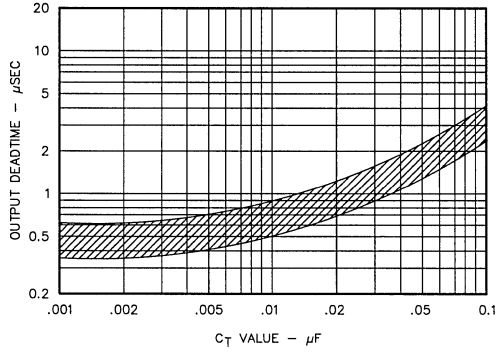


FIGURE 1 - OUTPUT STAGE DEADTIME VS. C_T

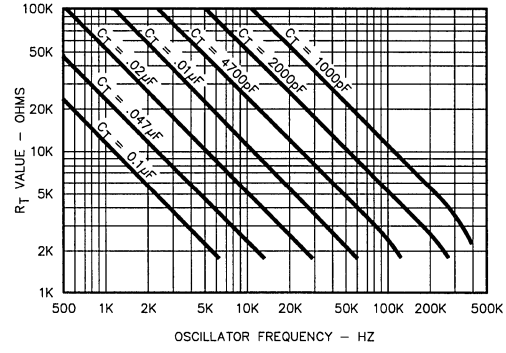


FIGURE 2 - OSCILLATOR FREQUENCY VS. R_T AND C_T

APPLICATION NOTES (continued)

CURRENT LIMITING

The current limiting circuitry of the SG1524 is shown in Figure 3. By matching the base-emitter voltages of Q1 and Q2, and assuming a negligible voltage drop across R1:

$$\text{C.L. Threshold} = V_{BE}(Q1) + I_1 \bullet R_2 - V_{BE}(Q2) = I_1 \bullet R_2$$
$$\sim 200 \text{ mV}$$

Although this circuit provides a relatively small threshold with a negligible temperature coefficient, there are some limitations to its use because of its simplicity.

The most important of these is the limited common-mode voltage range: ±0.3 volts around ground. This requires sensing in the ground or return line of the power supply. Also precautions should be taken to not turn on the parasitic substrate diode of the integrated circuit, even under transient conditions. A Schottky clamp diode at Pin 5 may be required in some configurations to achieve this.

A second factor to consider is that the response time is relatively slow. The current limit amplifier is internally compensated by R_1, C_1, and Q1, resulting in a roll-off pole at approximately 300 Hz. A third factor to consider is the bias current of the C.L. Sense pins. A constant current of approximately 150µA flows out of Pin 4, and a variable current with a range of 0-150µA flows out of Pin 5. As a result, the equivalent source impedance seen by the current sense pins should be less than 50 ohms to keep the threshold error less than 5%.

Since the gain of this circuit is relatively low (42 dB), there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, threshold is defined as the input voltage required to get 25% duty cycle (+2 volts at the error amplifier output) with the error amplifier signaling maximum duty cycle.

APPLICATION NOTE: If the current limit function is not used on the SG1524, the common-mode voltage range restriction requires both current sense pins to be grounded.

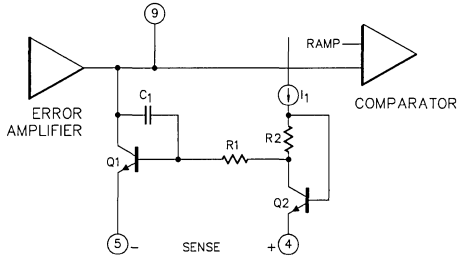
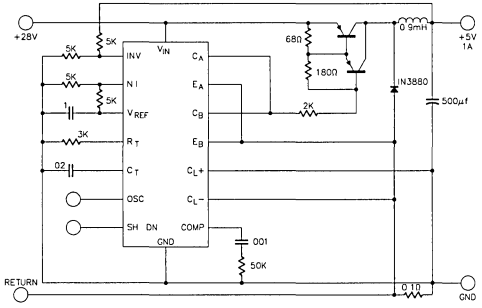
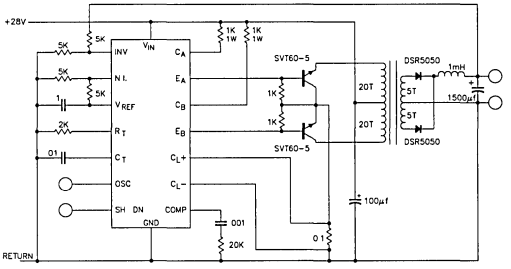


FIGURE 3 - CURRENT LIMITING CIRCUITRY OF THE SG1524

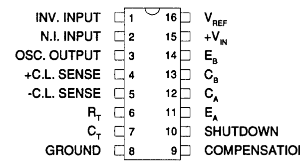
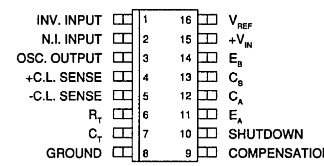
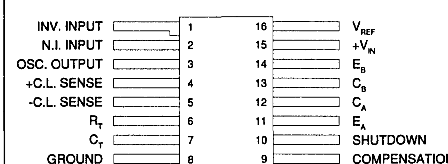
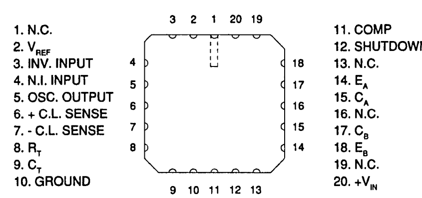


In this conventional single-ended regulator circuit, the two outputs of the SG1524 are connected in parallel for effective 0 - 90% duty-cycle modulation. The use of an output inductor requires and R-C phase compensation network for loop stability.



Push-pull outputs are used in this transformer-coupled DC-DC regulating converter. Note that the oscillator must be set at twice the desired output frequency as the SG1524's internal flip-flop divides the frequency by 2 as it switches the P.W.M. signal from one output to the other. Current limiting is done here in the primary so that the pulse width will be reduced should transformer saturation occur.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG1524J/883B SG1524J SG2524J SG3524J	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
16-PIN PLASTIC DIP N - PACKAGE	SG2524N SG3524N	-25°C to 85°C 0°C to 70°C	
16-PIN NARROW BODY PLASTIC S.O.I.C. D - PACKAGE	SG2524D SG3524D	-25°C to 85°C 0°C to 70°C	
16-PIN CERAMIC FLAT PACK F - PACKAGE	SG1524F/883B SG1524F	-55°C to 125°C -55°C to 125°C	
20-PIN CERAMIC LEADLESS CHIP CARRIER L- PACKAGE	SG1524L/883B SG1524L	-55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

REGULATING PULSE WIDTH MODULATOR

DESCRIPTION

The SG1524B is a pulse width modulator for switching power supplies which features improved performance over industry standards like the SG1524. A direct pin-for-pin replacement for the earlier device, it combines advanced processing techniques and circuit design to provide improved reference accuracy, and extended common mode range at the error amplifier and current limit inputs. A DC-coupled flip-flop eliminates triggering and glitch problems, and a PWM data latch prevents edge oscillations. The circuit incorporates true digital shutdown for high speed response, while an undervoltage lockout circuit prevents spurious outputs when the supply voltage is too low for stable operation. Full double-pulse suppression logic insures alternating output pulses when the Shutdown pin is used for pulse-by-pulse current limiting. The SG1524B is specified for operation over the full military ambient temperature range of -55°C to 125°C. The SG2524B is characterized for the industrial range of -25°C to 85°C, and the SG3524B is designed for the commercial range of 0°C to 70°C.

FEATURES

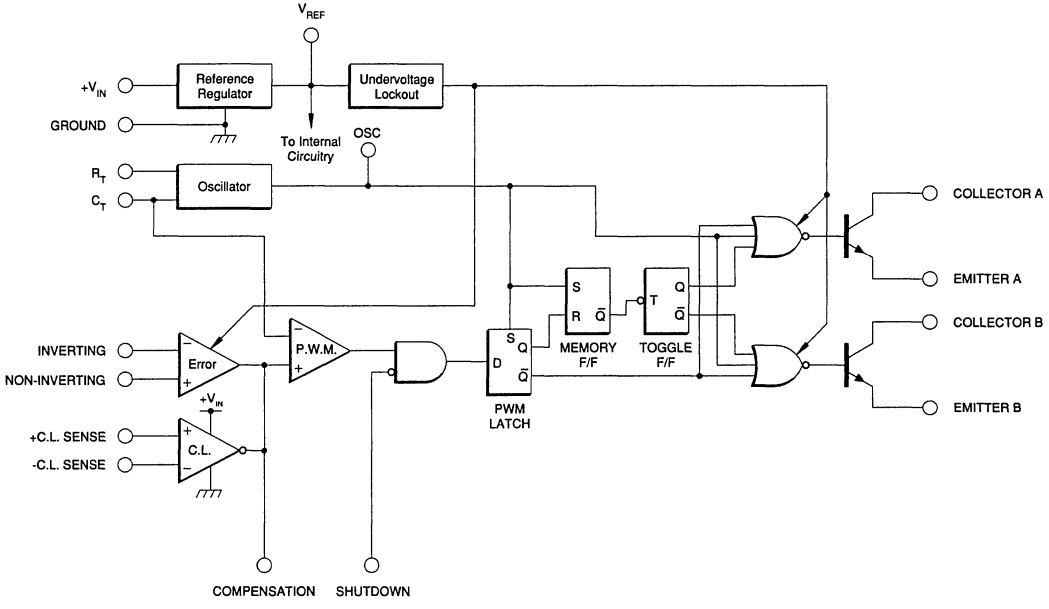
- **7V to 40V operation**
- **5V reference trimmed to ±1%**
- **100Hz to 400KHz oscillator range**
- **Excellent external sync capability**
- **Dual 100mA output transistors**
- **Wide current limit common mode range**
- **DC-coupled toggle flip-flop**
- **PWM data latch**
- **Undervoltage lockout**
- **Full double-pulse suppression logic**
- **60V output collectors**

HIGH RELIABILITY FEATURES - SG1524B

- **Available to MIL-STD-883 and DESC SMD**
- **Scheduled for MIL-M-38510 QPL listing**
- **Radiation data available**
- **SG level "S" processing available**

4

DESCRIPTION

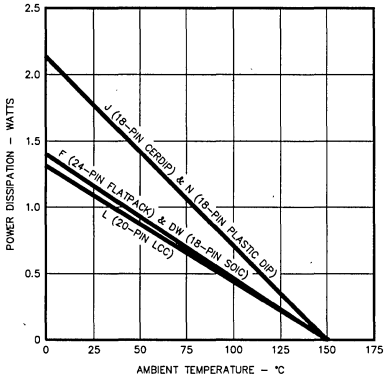


ABSOLUTE MAXIMUM RATINGS (Note 1)

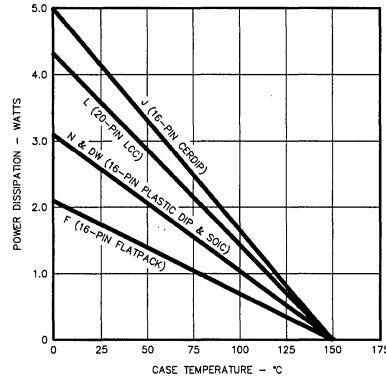
Input Voltage ($+V_{IN}$) 42V
Collector Voltage 60V
Logic Inputs ..... -0.3V to 5.5V
Current Limit Sense Inputs ..... -0.3V to V_{IN}
Output Current (each transistor) 200mA
Reference Load Current 50mA
Oscillator Charging Current 5mA
Operating Junction Temperature
Hermetic (J, F, L Packages) ..... 150°C
Plastic (N, DW Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1. Values beyond which damage may occur.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Voltage ($+V_{IN}$) ..... 7V to 40V
Collector Voltage ..... 0V to 60V
Error Amp Common Mode Range ..... 2.3V to V_{REF}
Current Limit Sense Common Mode Range ..... 0V to V_{IN}-2.5V
Output Current (each transistor) ..... 0 to 100mA
Reference Load Current ..... 0 to 20mA
Oscillator Charging Current ..... 25µA to 1.8mA
Oscillator Frequency Range ..... 100Hz to 400KHz
Oscillator Timing Resistor (R_T) ..... 2KΩ to 150KΩ
Oscillator Timing Capacitor (C_T) ..... 1nF to 0.1µF
Operating Ambient Temperature Range
SG1524B ..... -55°C to 125°C
SG2524B ..... -25°C to 85°C
SG3524B ..... 0°C to 70°C

Note 2: Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1524B with $-55°C \le T_A \le 125°C$, SG2524B with $-25°C \le T_A \le 85°C$, SG3524B with $0°C \le T_A \le 70°C$, and $+V_{IN} = 20V$. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1524B/2524B			SG3524B			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Section (Note 3)								
Output Voltage	$T_J = 25°C$	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	$V_{IN} = 7V$ to 40V		3	20		3	30	mV
Load Regulation	$I_L = 0$ to 20mA		5	30		5	50	mV
Temperature Stability (Note 7)	Over Operating Temperature Range		15	50		15	50	mV
Total Output Voltage Range	Over Line, Load and Temperature	4.90		5.10	4.80		5.20	V
Short Circuit Current	$V_{REF} = 0V$	25	50	120	25	50	120	mA
Undervoltage Lockout Section								
Threshold Voltage		4.3	4.5	4.7	4.3	4.5	4.7	V

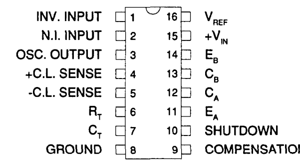
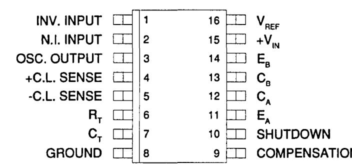
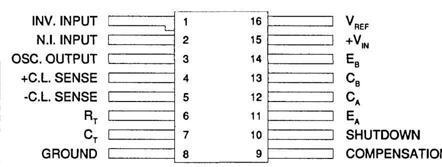
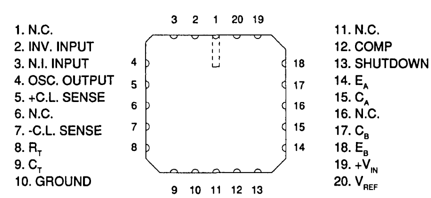
Note 3. $I_L = 0mA$

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1524B/2524B			SG3524B			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Oscillator Section (Note 4)								
Initial Accuracy	T_J = 25°C	42	45	48	40	45	50	KHz
Voltage Stability	V_{IN} = 7V to 40V		0.1	1		0.1	1	%
Temperature Stability (Note 9)	Over Operating Range		1	2		1	2	%
Minimum Frequency	R_T = 150KΩ, C_T = 0.1μF		50	140		50	120	Hz
Maximum Frequency	R_T = 2KΩ, C_T = 470pF	400	600		400	600		KHz
Sawtooth Peak Voltage	V_{IN} = 40V		3.5	3.9		3.5	3.9	V
Sawtooth Valley Voltage	V_{IN} = 7V	0.6	1		0.6	1		V
Clock Amplitude		3.0	4.0		3.0	4.0		V
Clock Pulse Width		0.2	0.5	1.2	0.2	0.5	1.2	μs
Error Amplifier Section (Note 5)								
Input Offset Voltage	$R_S \leq$ 2KΩ		0.5	5		2	10	mV
Input Bias Current			1	5		1	10	μA
Input Offset Current				1			1	μA
DC Open Loop Gain	$R_L \geq$10MΩ	60	78		60	78		dB
Output Low Level	I_{SINK} = 100μA; $V_{PIN\,1}$ - $V_{PIN\,2} \geq$ 150mV		0.2	0.5		0.2	0.5	V
Output High Level	I_{SOURCE} = 100μA; $V_{PIN\,2}$ - $V_{PIN\,1} \geq$ 150mV	3.8	4.2		3.8	4.2		V
Common Mode Rejection	V_{CM} = 2.3V to V_{REF}	70	90		70	90		dB
Supply Voltage Rejection	V_{IN} = 7V to 40V	76	100		76	100		dB
Gain-Bandwidth Product (Note 7)	T_J = 25°C	1	2		1	2		MHz
P.W.M. Comparator (Note 4)								
Minimum Duty Cycle	V_{COMP} = 0.5V			0			0	%
Maximum Duty Cycle	V_{COMP} = 3.9V	45	49		45	49		%
Current Limit Amplifier Section (Note 6)								
Sense Voltage		180	200	220	170	200	230	mV
Input Bias Current			-3	-10		-3	-10	μA
Shutdown Input Section								
HIGH Input Voltage		2.0			2.0			V
HIGH Input Current	$V_{SHUTDOWN}$ = 5.0V		0.1	1		0.1	1	mA
LOW Input Voltage				0.6			0.6	V
Output Section (each transistor)								
Collector Leakage Current	V_{CE} = 60V			50			50	μA
Collector Saturation Voltage	I_C = 10mA		0.2	0.4		0.2	0.4	V
	I_C = 100mA		1.0	2.0		1.0	2.0	V
Emitter Output Voltage	I_E = 10mA	17.5	19		17.5	19		V
	I_E = 100mA	17	18		17	18		V
Emitter Voltage Rise Time (Note 7)	R_E = 2KΩ, T_A = 25°C		0.2	0.5		0.2	0.5	μs
Collector Voltage Fall Time	R_C = 2KΩ, T_A = 25°C		0.1	0.2		0.1	0.2	μs
Power Consumption								
Standby Current	V_{IN} = 40V, $V_{SHUTDOWN}$ = 2.0V		5	12		5	12	mA

Note 4. F_{OSC} = 43KHz (R_T = 2700Ω, C_T = .01μF)
Note 5. V_{CM} = 2.3V to V_{REF}
Note 6. V_{CM} = 0V to 17.5V
Note 7. These parameters, although guaranteed over the recommended operating conditions, are not tested in production.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG1524BJ/883B SG1524BJ SG2524BJ SG3524BJ	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
16-PIN PLASTIC DIP N - PACKAGE	SG2524BN SG3524BN	-25°C to 85°C 0°C to 70°C	
16-PIN WIDE BODY PLASTIC S.O.I.C. DW - PACKAGE	SG2524BDW SG3524BDW	-25°C to 85°C 0°C to 70°C	
16-PIN CERAMIC FLAT PACK F - PACKAGE	SG1524BF/883B SG1524BF	-55°C to 125°C -55°C to 125°C	
20-PIN CERAMIC LEADLESS CHIP CARRIER L- PACKAGE	SG1524BL/883B SG1524BL	-55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SG1525A/SG2525A/SG3525A
SG1527A/SG2527A/SG3527A

REGULATING PULSE WIDTH MODULATOR

DESCRIPTION

The SG1525A/1527A series of pulse width modulator integrated circuits are designed to offer improved performance and lower external parts count when used to implement all types of switching power supplies. The on-chip +5.1 volt reference is trimmed to ±1% initial accuracy and the input common-mode range of the error amplifier includes the reference voltage, eliminating external potentiometers and divider resistors. A Sync input to the oscillator allows multiple units to be slaved together, or a single unit to be synchronized to an external system clock. A single resistor between the C_T pin and the Discharge pin provides a wide range of deadtime adjustment. These devices also feature built-in soft-start circuitry with only a timing capacitor required externally. A Shutdown pin controls both the soft-start circuitry and the output stages, providing instantaneous turn-off with soft-start recycle for slow turn-on. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for input voltages less than that required for normal operation. Another unique feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200mA. The SG1525A output stage features NOR logic, giving a LOW output for an OFF state. The SG1527A utilizes OR logic which results in a HIGH output level when OFF.

FEATURES

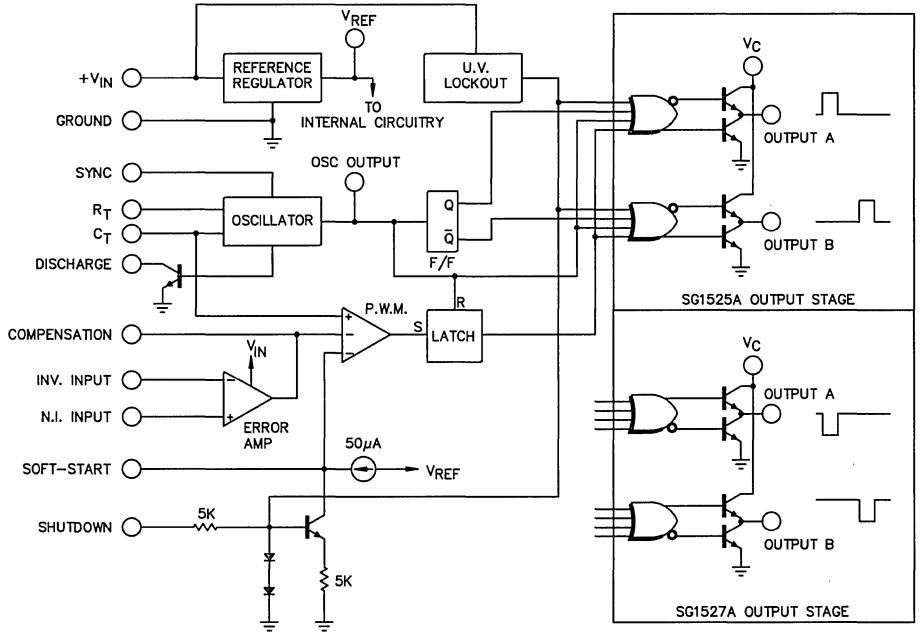
- **8V to 35V operation**
- **5.1V reference trimmed to ±1%**
- **100Hz to 500KHz oscillator range**
- **Separate oscillator sync terminal**
- **Adjustable deadtime control**
- **Internal soft-start**
- **Input undervoltage lockout**
- **Latching P.W.M. to prevent multiple pulses**
- **Dual source/sink output drivers**

HIGH RELIABILITY FEATURES - SG1525A, SG1527A

- **Available to MIL-STD-883B**
- **MIL-M38510/12602BEA - JAN1525AJ**
- **MIL-M38510/12604BEA - JAN1527AJ**
- **Radiation data available**
- **SG level "S" processing available**

4

BLOCK DIAGRAM



April 1990

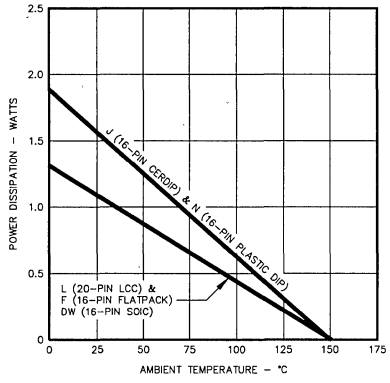
See Application Notes for additional information.

ABSOLUTE MAXIMUM RATINGS (Note 1)

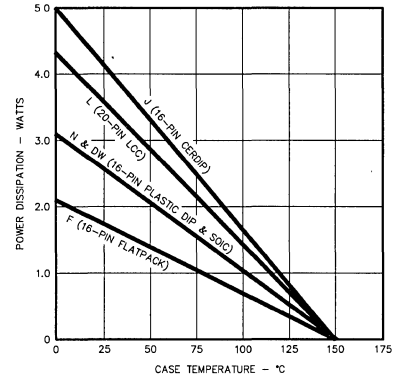
Supply Voltage ($+V_{IN}$) 40V
Collector Supply Voltage (V_C) 40V
Logic Inputs ..... -0.3V to 5.5V
Analog Inputs ..... -0.3V to V_{IN}
Output Current, Source or Sink 500mA
Reference Load Current 50mA
Oscillator Charging Current 5mA
Operating Junction Temperature Range
Hermetic (J, F, L Packages) ..... 150°C
Plastic (N, DW Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1. Values beyond which damage may occur.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Voltage ($+V_{IN}$) ..... 8V to 35V
Collector Voltage (V_C) ..... 4.5V to 35V
Sink/Source Load Current (steady state) ..... 0 to 100mA
Sink/Source Load Current (peak) ..... 0 to 400mA
Reference Load Current ..... 0 to 20mA
Oscillator Frequency Range ..... 100Hz to 350KHz
Oscillator Timing Resistor (R_T) ..... 2KΩ to 150KΩ
Deadtime Resistor Range (R_D) ..... 0Ω to 500Ω
Oscillator Timing Capacitor (C_T) ..... 0.001µF to 0.1µF
Operating Ambient Temperature Range
SG1525A/SG1527A ..... -55°C to 125°C
SG2525A/SG2527A ..... -25°C to 85°C
SG3525A/SG3527A ..... 0°C to 70°C

Note 2: Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1525A/SG1527A with $-55°C \le T_A \le 125°C$, SG2525A/SG2527A with $-25°C \le T_A \le 85°C$, SG3525A/SG3527A with $0°C \le T_A \le 70°C$, and $+V_{IN} = 20V$. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Section								
Output Voltage	$T_J = 25°C$	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	$V_{IN} = 8V$ to 35V		10	30		10	30	mV
Load Regulation	$I_L = 0$ to 20mA		20	50		20	50	mV
Temperature Stability (Note 3)	Over Operating Temperature Range		20	50		20	50	mV
Total Output Voltage Range (Note 3)	Over Line, Load and Temperature	5.00		5.20	4.95		5.25	V
Short Circuit Current	$V_{REF} = 0V$, $T_J = 25°C$		80	100		80	100	mA
Output Noise Voltage (Note 3)	$10Hz \le f \le 10KHz$, $T_J = 25°C$		40	200		40	200	µVrms
Long Term Stability (Note 3)	$T_J = 125°C$		20	50		20	50	mV/khr

Note 3. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
Note 4. $F_{OSC} = 40KHz$ ($R_T = 3.6K\Omega$, $C_T = 0.01\mu F$, $R_D = 0\Omega$)
Note 5. Applies to SG1525A/2525A/3525A only, due to polarity of output pulses.

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Oscillator Section (Note 4)								
Initial Accuracy	T_J = 25°C	37.6	40	42.4	37.6	40	42.4	KHz
Voltage Stability	V_{IN} = 8V to 35V		±0.3	±1		±1	±2	%
Temperature Stability (Note 3)	MIN ≤ T_J ≤ MAX		±3	±6		±3	±6	%
Minimum Frequency (Note 3)	R_T = 150KΩ, C_T = .01µF			150			150	Hz
Maximum Frequency (Note 3)	R_T = 2KΩ, C_T = 1nF	350			350			KHz
Current Mirror	I_{RT} = 2mA	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude		3.0	3.5		3.0	3.5		V
Clock Width	T_J = 25°C	0.3	0.5	1.0	0.3	0.5	1.0	µs
Sync Threshold		1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current	Sync Voltage = 3.5V		1.0	2.5		1.0	2.5	mA
Error Amplifier Section (V_{CM} = 5.1V)								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	10		1	10	µA
Input Offset Current				1			1	µA
DC Open Loop Gain	R_L ≥10MΩ, T_J = 25°C	60	75		60	75		dB
Gain-Bandwidth Product (Note 3)	A_V = 0dB, T_J = 25°C	1	2		1	2		MHz
Output Low Level			0.2	0.5		0.2	0.5	V
Output High Level		3.8	5.6		3.8	5.6		V
Common Mode Rejection	V_{CM} = 1.5V to 5.2V	60	75		60	75		dB
Supply Voltage Rejection	V_{IN} = 8V to 35V	50	60		50	60		dB
P.W.M. Comparator Section								
Minimum Duty Cycle	V_{COMP} = 0.6V			0			0	%
Maximum Duty Cycle	V_{COMP} = 3.6V	45	49		45	49		%
Input Threshold (Note 4)	Zero Duty Cycle	0.6	0.9		0.6	0.9		V
	Maximum Duty Cycle		3.3	3.6		3.3	3.6	V
Input Bias Current			.05	2.0		.05	2.0	µA
Soft-Start Section								
Soft Start Current	$V_{SHUTDOWN}$ = 0V	25	50	80	25	50	80	µA
Soft Start Voltage	$V_{SHUTDOWN}$ = 2V		0.4	0.6		0.4	0.6	V
Shutdown Input Current	$V_{SHUTDOWN}$ = 2.5V		0.4	1.0		0.4	1.0	mA
Output Drivers Section (each transistor, V_C = 20V)								
Output High Level	I_{SOURCE} = 20mA	18	19		18	19		V
	I_{SOURCE} = 100mA	17	18		17	18		V
Output Low Level	I_{SINK} = 20mA		0.2	0.4		0.2	0.4	V
	I_{SINK} = 100mA		1.0	2.2		1.0	2.2	V
Undervoltage Lockout	V_{COMP} and V_{SS} = High	6	7	8	6	7	8	V
Collector Leakage (Note 5)	V_C = 35V			200			200	µA
Rise Time	C_L = 1nF, T_J = 25°C		100	600		100	600	ns
Fall Time	C_L = 1nF, T_J = 25°C		50	300		50	300	ns
Shutdown Delay (Note 3)	V_{SD} = 3V, C_S = 0, T_J = 25°C		0.2	0.5		0.2	0.5	µs
Total Standby Current								
Standby Current	V_{IN} = 35V		14	20		14	20	mA

4

OSCILLATOR SECTION

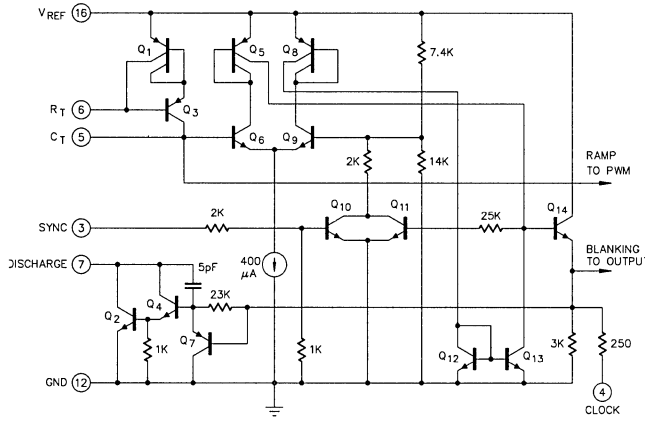


FIGURE 1 - OSCILLATOR SCHEMATIC

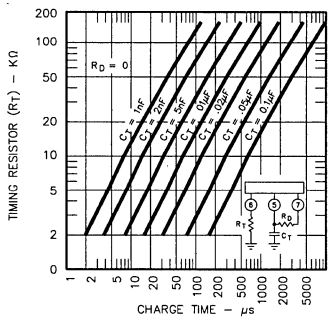


FIGURE 2 - OSCILLATOR CHARGE TIME VS. R_T AND C_T

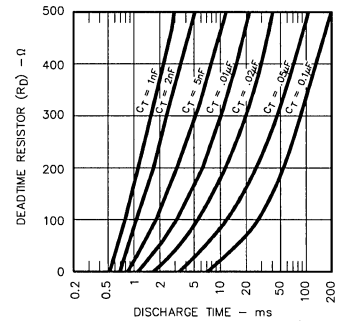


FIGURE 3 - OSCILLATOR DISCHARGE TIME VS. R_D AND C_T

ERROR AMPLIFIER SECTION

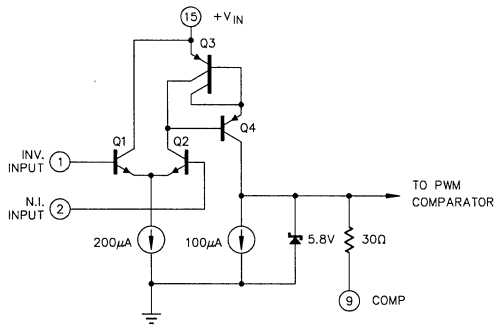


FIGURE 4 - ERROR AMPLIFIER

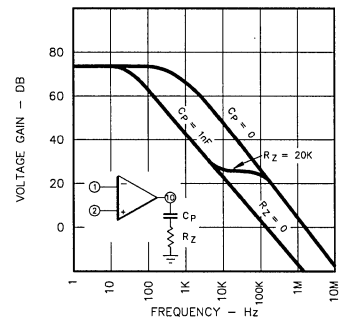


FIGURE 5 - ERROR AMPLIFIER OPEN-LOOP FREQUENCY RESPONSE

OUTPUT SECTION

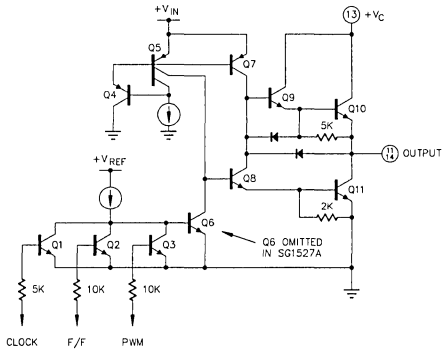


FIGURE 6 -OUTPUT CIRCUIT (½ Circuit Shown)

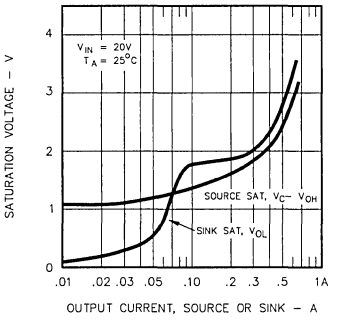
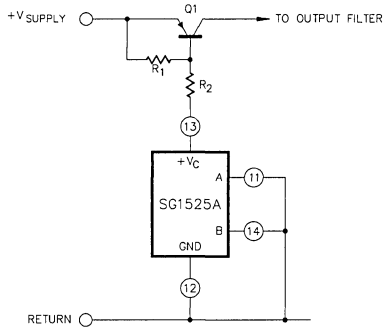
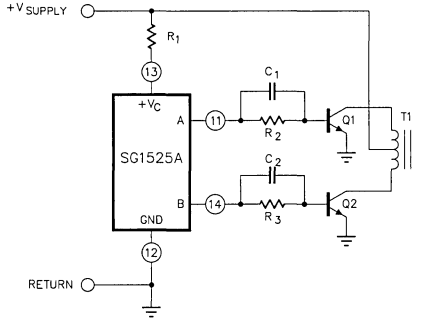


FIGURE 7 - OUTPUT SATURATION CHARACTERISTICS

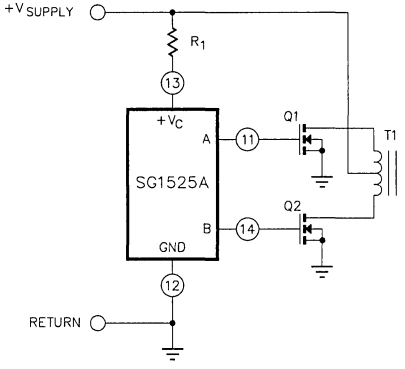
APPLICATION INFORMATION



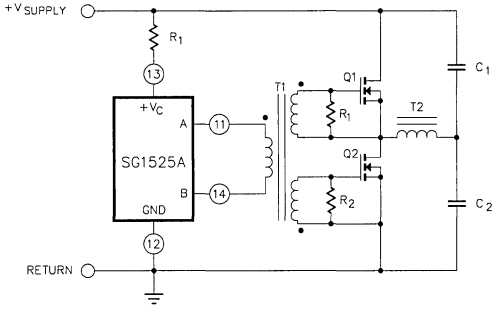
For single-ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.



In conventional push-pull bipolar designs, forward base drive is controlled by R_1 - R_3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C_1 and C_2.



The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.



Low power transformers can be driven directly by the SG1525A. Automatic reset occurs during deadtime, when both ends of the primary winding are switched to ground.

APPLICATION INFORMATION (continued)

SHUTDOWN OPTIONS

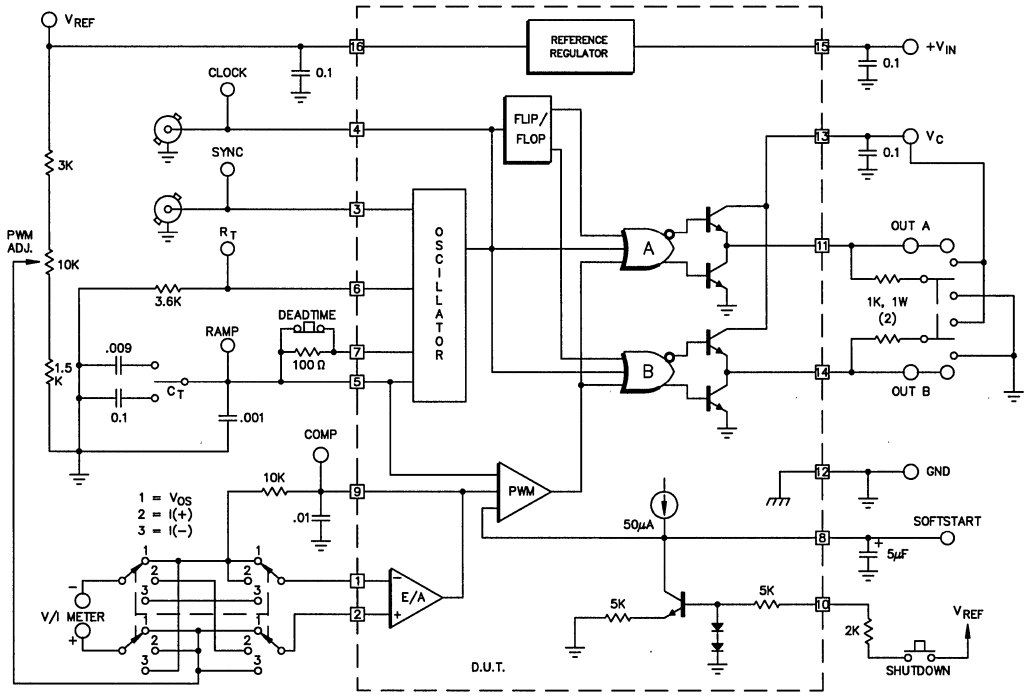
1. Use an external transistor or open-collector comparator to pull down on the Comp terminal. This will set the PWM latch turning off both outputs. If the shutdown signal is momentary, pulse-by-pulse protection can be accomplished as the PWM latch will be reset with each clock pulse.

2. The same results can be accomplished by pulling down on the Soft-Start terminal with the difference that on this pin, shutdown will not affect the amplifier compensation network but must discharge any Soft-Start capacitor.

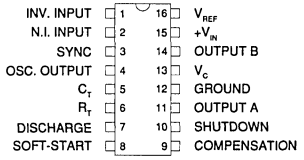
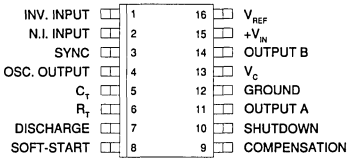
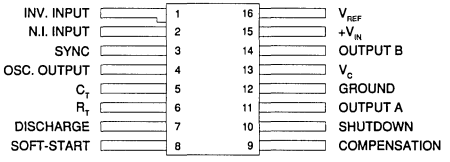
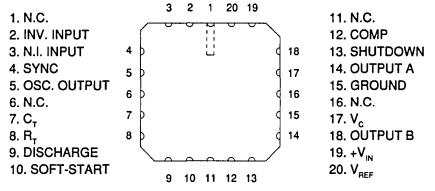
3. Apply a positive-going signal to the Shutdown terminal. This will provide most rapid shutdown of the outputs but will not immediately set the PWM latch if there is a Soft-Start capacitor. This capacitor will discharge but with a current of approximately twice the charging current.

4. The shutdown terminal can be used to set the PWM latch on a pulse-by-pulse basis if there is no external capacitance on Soft-Start terminal. Slow turn-on may still be accomplished by applying an external capacitor, blocking diode, and charging resistor to the comp terminal. (See SG1524 Application Note).

SG1525A/1527A LAB TEST FIXTURE



CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG1525AJ/883B SG1525AJ SG2525AJ SG3525AJ SG1527AJ/883B SG1527AJ SG2527AJ SG3527AJ	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C -55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
16-PIN PLASTIC DIP N - PACKAGE	SG2525AN SG3525AN SG2527AN SG3527AN	-25°C to 85°C 0°C to 70°C -25°C to 85°C 0°C to 70°C	
16-PIN WIDE BODY PLASTIC S.O.I.C. DW - PACKAGE	SG2525ADW SG3525ADW SG2527ADW SG3527ADW	-25°C to 85°C 0°C to 70°C -25°C to 85°C 0°C to 70°C	
16-PIN CERAMIC FLAT PACK F - PACKAGE	SG1525AF/883B SG1525AF SG1527AF/883B SG1527AF	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C	
20-PIN CERAMIC LEADLESS CHIP CARRIER L- PACKAGE	SG1525AL/883B SG1525AL SG1527AL/883B SG1527AL	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

REGULATING PULSE WIDTH MODULATOR

DESCRIPTION

The SG1526 is a high performance monolithic pulse width modulator circuit designed for fixed-frequency switching regulators and other power control applications. Included in an 18-pin dual-in-line package are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and steering logic, and two low impedance power drivers. Also included are protective features such as soft-start and undervoltage lockout, digital current limiting, double pulse inhibit, a data latch for single pulse metering, adjustable deadtime, and provision for symmetry correction inputs. For ease of interface, all digital control ports are TTL and B-series CMOS compatible. Active LOW logic design allows wired-OR connections for maximum flexibility. This versatile device can be used to implement single-ended or push-pull switching regulators of either polarity, both transformerless and transformer coupled. The SG1526 is characterized for operation over the full military ambient junction temperature range of -55°C to +150°C. The SG2526 is characterized for operation from -25°C to +150°C, and the SG3526 is characterized for operation from 0°C to +125°C.

FEATURES

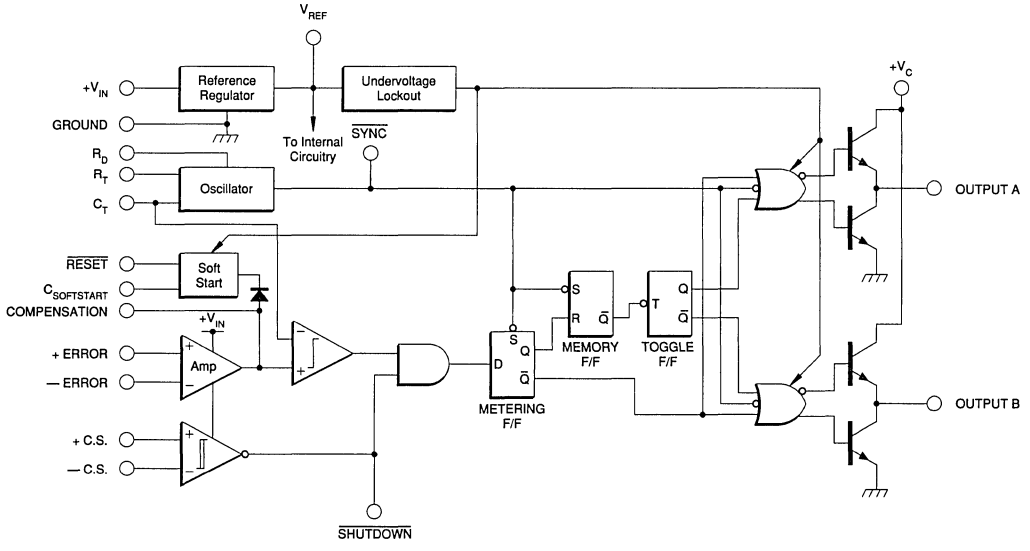
- **8 to 35 volt operation**
- **5V reference trimmed to ±1%**
- **1Hz to 350KHz oscillator range**
- **Dual 100mA source/sink outputs**
- **Digital current limiting**
- **Double pulse suppression**
- **Programmable deadtime**
- **Undervoltage lockout**
- **Single pulse metering**
- **Programmable soft-start**
- **Wide current limit common mode range**
- **TTL/CMOS compatible logic ports**
- **Symmetry correction capability**
- **Guaranteed 6 unit synchronization**

HIGH RELIABILITY FEATURES - SG1526

- **Available to MIL-STD-883B and DESC SMD**
- **Radiation data available**
- **SG level "S"processing available**

4

BLOCK DIAGRAM



April 1990

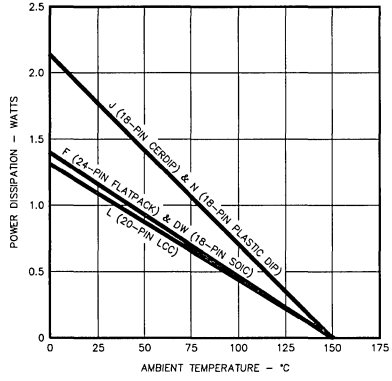
See Application Notes for addition information.

ABSOLUTE MAXIMUM RATINGS

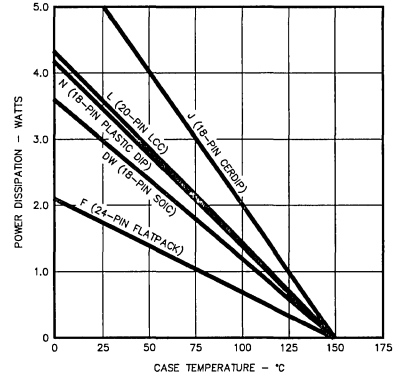
Input Voltage (V_{IN}) 40V
Collector Supply Voltage (V_C) 40V
Logic Inputs ..... -0.3V to 5.5V
Analog Inputs ..... -0.3V to V_{IN}
Source/Sink Load Current (each output) 200mA
Reference Load Current 50mA
Logic Sink Current 15mA
Operating Junction Temperature
Hermetic (J, F, L Packages) ..... 150°C
Plastic (N, DW Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Voltage ..... 8V to 35V
Collector Supply Voltage ..... 4.5V to 35V
Sink/Source Load Current (each output) ..... 0 to 100mA
Reference Load Current ..... 0 to 20mA
Oscillator Frequency Range ..... 1Hz to 350KHz
Oscillator Timing Resistor ..... 2KΩ to 150KΩ
Oscillator Timing Capacitor ..... 1nF to 20μF
Available Deadtime Range at 40KHz ..... 3% to 50%
Operating Ambient Temperature Range:
SG1526 ..... -55°C to 125°C
SG2526 ..... -25°C to 85°C
SG3526 ..... 0°C to 70°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1526 with -55°C ≤ T_A ≤ 125°C, SG2526 with -25°C ≤ T_A ≤ 85°C, SG3526 with 0°C ≤ T_A ≤ 70°C, and V_{IN} = 15V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1526/2526			SG3526			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Section (Note 3)								
Output Voltage	T_J = 25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	V_{IN} = 8 to 35V		10	30		10	30	mV
Load Regulation	I_L = 0 to 20mA		10	30		10	50	mV
Temperature Stability (Note 9)	Over Operating T_J		15	50		15	50	mV
Total Output Voltage Range (Note 9)	Over Recommended Operating Conditions	4.90	5.00	5.10	4.85	5.00	5.15	V
Short Circuit Current	V_{REF} = 0V		50	125		50	125	mA
Undervoltage Lockout Section								
$\overline{\text{RESET}}$ Output Voltage	V_{REF} = 3.8V		0.2	0.4		0.2	0.4	V
$\overline{\text{RESET}}$ Output Voltage	V_{REF} = 4.8V	2.4	4.8		2.4	4.8		V

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1526/2526			SG3526			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Oscillator Section (Note 4)								
Initial Accuracy	T_J = 25°C		±3	±8		±3	±8	%
Voltage Stability	V_{IN} = 8 to 35V		0.5	1.0		0.5	1.0	%
Temperature Stability (Note 9)	Over Operating T_J		7	10		5	10	%
Minimum Frequency (Note 9)	R_T = 150KΩ, C_T = 20µF			1.0			1.0	Hz
Maximum Frequency	R_T = 2KΩ, C_T = 1.0nF	350			350			KHz
Sawtooth Peak Voltage	V_{IN} = 35V		3.0	3.5		3.0	3.5	V
Sawtooth Valley Voltage	V_{IN} = 8V	0.5	1.0		0.5	1.0		V
Error Amplifier Section (Note 5)								
Input Offset Voltage	R_S ≤ 2KΩ		2	5		2	10	mV
Input Bias Current			-350	-1000		-350	-2000	nA
Input Offset Current			35	100		35	200	nA
DC Open Loop Gain	R_L ≥ 10MΩ, T_J = 25°C	64	72		60	72		dB
High Output Voltage	V_{PIN1} - V_{PIN2} ≥ 150mV, I_{SOURCE} = 100µA	3.6	4.2		3.6	4.2		V
Low Output Voltage	V_{PIN2} - V_{PIN1} ≥ 150mV, I_{SINK} = 100µA		0.2	0.4		0.2	0.4	V
Common Mode Rejection	R_S ≤ 2KΩ	70	94		70	94		dB
Supply Voltage Rejection	V_{IN} = 8V to 35V	66	80		66	80		dB
PWM Comparator Section (Note 4)								
Minimum Duty Cycle	$V_{COMPENSATION}$ = 0.4V			0			0	%
Maximum Duty Cycle	$V_{COMPENSATION}$ = 3.6V	45	49		45	49		%
Digital Ports (SYNC, SHUTDOWN, and RESET)								
HIGH Output Voltage	I_{SOURCE} = 40µA	2.4	4		2.4	4		V
LOW Output Voltage	I_{SINK} = 3.6mA		0.2	0.4		0.2	0.4	V
HIGH Input Current	V_{IH} = 2.4V		-125	-300		-125	-300	µA
LOW Input Current	V_{IL} = 0.4V		-225	-500		-225	-500	µA
Current Limit Comparator Section (Note 6)								
Sense Voltage	R_S ≤ 50Ω, T_J = 25°C	90	100	110	80	100	120	mV
Input Bias Current			-3	-10		-3	-10	µA
Soft-Start Section								
Error Clamp Voltage	$\overline{RESET}$ = 0.4V		0.1	0.4		0.1	0.4	V
C_S Charging Current	$\overline{RESET}$ = 2.4V	50	100	200	50	100	200	µA
Output Drivers (each output) (Note 7)								
HIGH Output Voltage	I_{SOURCE} = 20mA	12.5	13.5		12.5	13.5		V
	I_{SOURCE} = 100mA	12	13		12	13		V
LOW Output Voltage	I_{SINK} = 20mA		0.2	0.3		0.2	0.3	V
	I_{SINK} = 100mA		1.2	2		1.2	2	V
Collector Leakage	V_C = 40V		50	150		50	150	µA
Rise Time	C_L = 1000pF		0.3	0.6		0.3	0.6	µs
Fall Time	C_L = 1000pF		0.1	0.2		0.1	0.2	µs
Power Consumption Section (Note 8)								
Standby Current	$\overline{SHUTDOWN}$ = 0.4V		18	30		18	30	mA

Note 3. I_L = 0mA
Note 4. F_{OSC} = 40KHz (R_T = 4.12KΩ ±1%, C_T = .01µF ±1%, R_D = 0Ω)
Note 5. V_{CM} = 0 to 5.2V
Note 6. V_{CM} = 0 to 12V
Note 7. V_C = 15V
Note 8. V_{IN} = 35V
Note 9. These parameters, although guaranteed over the recommended operating conditions, are not tested in production.

4

CHARACTERISTIC CURVES

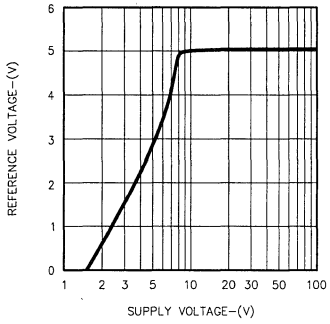


FIGURE 1.
REFERENCE VOLTAGE VS. SUPPLY VOLTAGE

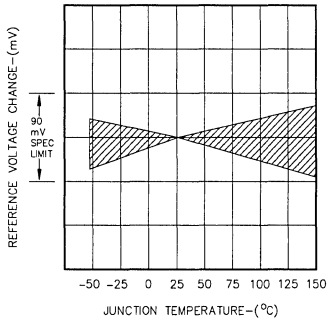


FIGURE 2.
REFERENCE TEMPERATURE STABILITY

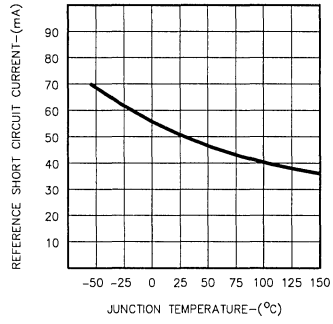


FIGURE 3.
REFERENCE SHORT CIRCUIT CURRENT

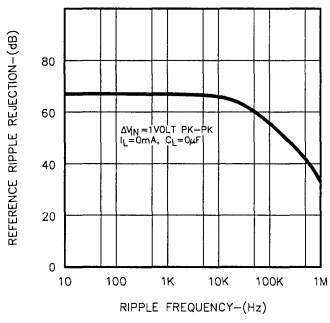


FIGURE 4.
REFERENCE RIPPLE REJECTION

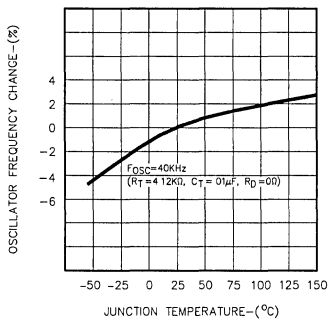


FIGURE 5.
OSCILLATOR FREQUENCY TEMPERATURE STABILITY

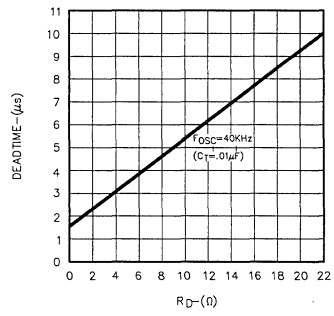


FIGURE 6.
OUTPUT DRIVER DEADTIME VS. R_D VALUE

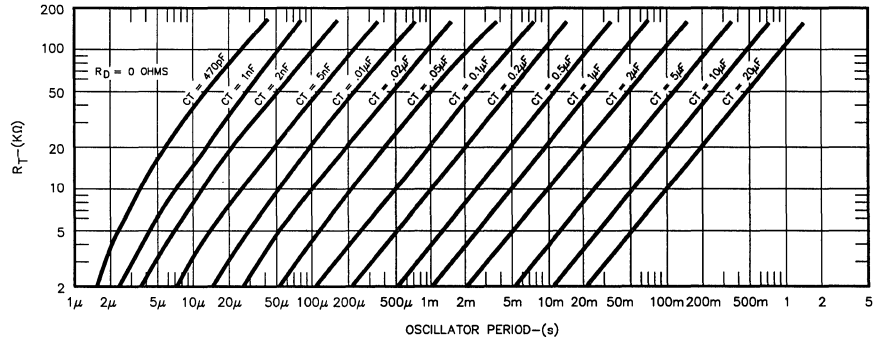


FIGURE 7.
OSCILLATOR PERIOD VS. R_T AND C_T

CHARACTERISTIC CURVES (continued)

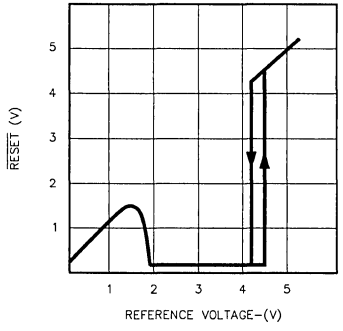


FIGURE 8.
UNDERVOLTAGE LOCKOUT CHARACTERISTIC

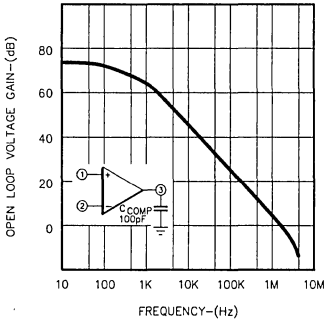


FIGURE 9.
ERROR AMPLIFIER OPEN LOOP GAIN VS. FREQUENCY

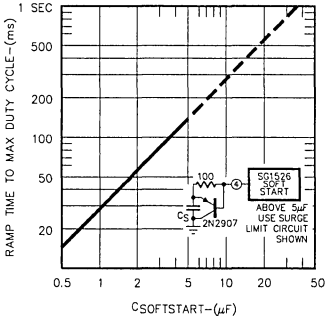


FIGURE 10.
SOFTSTART TIME CONSTANT VS. C_S

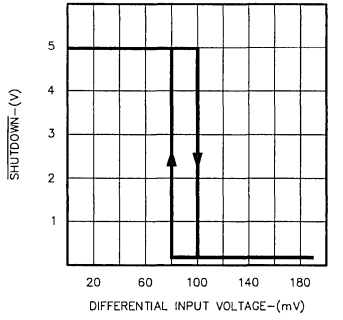


FIGURE 11.
CURRENT LIMIT TRANSFER FUNCTION

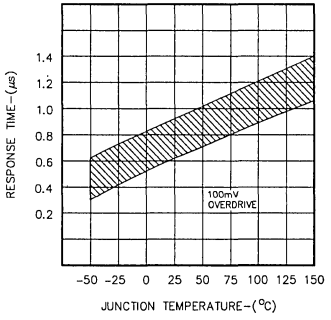


FIGURE 12.
COMPARATOR INPUT TO DRIVER OUTPUT DELAY

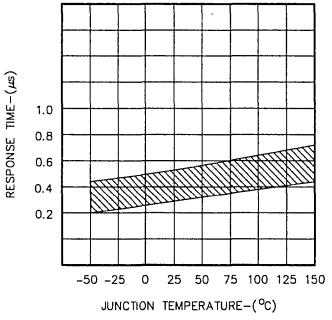


FIGURE 13.
SHUTDOWN INPUT TO DRIVER OUTPUT DELAY

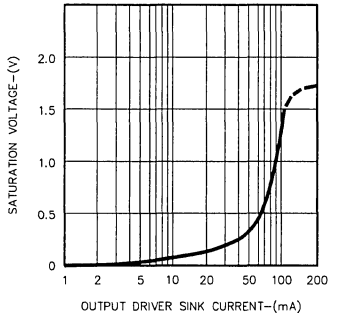


FIGURE 14.
OUTPUT DRIVER SATURATION VOLTAGE VS. I_{SINK}

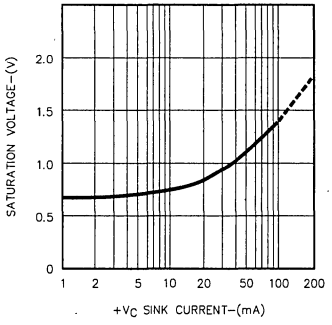


FIGURE 15.
OUTPUT SUPPLY SATURATION VOLTAGE VS. I_{SINK}

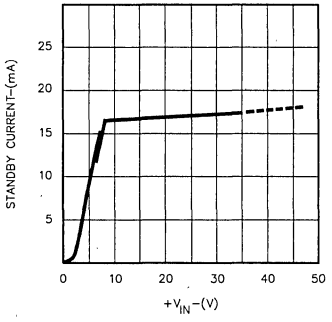


FIGURE 16.
STANDBY CURRENT VS. SUPPLY VOLTAGE

APPLICATION INFORMATION

VOLTAGE REFERENCE

The reference regulator of the SG1526 is based on a temperature compensated zener diode. The circuitry is fully active at supply voltages above +8 volts., and provides up to 20mA of load current to external circuitry at +5.0 volts. In systems where additional current is required, an external PNP transistor can be used to boost the available current. A rugged low frequency audio-type transistor should be used, and lead lengths between the PWM and transistor should be as short as possible to minimize the risk of oscillations. Even so, some types of transistors may require collector-base capacitance for stability. Up to 1amp of load current can be obtained with excellent regulation if the device selected maintains high current gain.

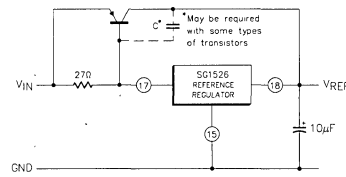


FIGURE 17.
EXTENDING REFERENCE OUTPUT CURRENT

UNDERVOLTAGE LOCKOUT

The undervoltage lockout circuit protects the SG1526 and the power devices it controls from inadequate supply voltage. If $+V_{IN}$ is too low, the circuit disables the output drivers and holds the $\overline{RESET}$ pin LOW. This prevents spurious output pulses while the control circuitry is stabilizing, and holds the soft-start timing capacitor in a discharged state.

The circuit consists of a +1.2 volt bandgap reference and comparator circuit which is active when the reference voltage has risen to $3V_{BE}$ or 1.8 volts at 25°C. When the reference voltage rises to approximately +4.4 volts, the circuit enables the output drivers and releases the $\overline{RESET}$ pin, allowing a normal soft-start. The comparator has 200mV of hysteresis to minimize oscillation at the trip point. When $+V_{IN}$ to the PWM is removed and the reference drops to +4.2 volts, the undervoltage circuit pulls $\overline{RESET}$ LOW again. The soft-start capacitor is immediately discharged, and the PWM is ready for another soft-start cycle.

The SG1526 can operate from a +5 volt supply by connecting the V_{REF} pin to the $+V_{IN}$ pin and maintaining the supply between +4.8 and +5.2 volts.

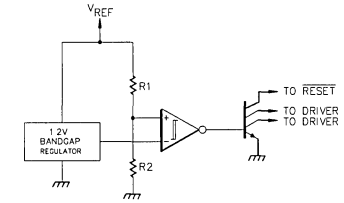


FIGURE 18.
SIMPLIFIED UNDERVOLTAGE LOCKOUT

SOFT-START CIRCUIT

The soft-start circuit protects the power transistors and rectifier diodes from high current surges during power supply turn-on. When supply voltage is first applied to the SG1526, the undervoltage lockout circuit holds $\overline{RESET}$ LOW with Q3. Q1 is turned on, which holds the soft-start capacitor voltage at zero. The second collector of Q1 clamps the output error amplifier to ground, guaranteeing zero duty cycle at the driver outputs. When the supply voltage reaches normal operating range, $\overline{RESET}$ will go HIGH. Q1 turns off, allowing the internal 100μA current source to charge C_S. Q2 clamps the error amplifier output to $1V_{BE}$ above the voltage on C_S. As the soft-start voltage ramps up to +5 volts, the duty cycle of the PWM linearly increases to whatever value the voltage regulation loop requires for an error null. Figure 10 gives the timing relationship between C_S and ramp time to 100% duty cycle.

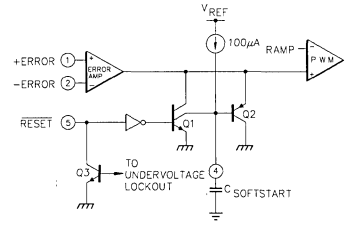


FIGURE 19.
SOFT-START CIRCUIT SCHEMATIC

DIGITAL CONTROL PORTS

The three digital control ports of the SG1526 are bi-directional. Each pin can drive TTL and 5 volt CMOS logic directly, up to a fan-out of 10 low-power Schottky gates. Each pin can also be directly driven by open-collector voltage comparators; fan-in is equivalent to 1 low-power Schottky gate. Each port is normally HIGH; the pin is pulled LOW to activate the particular function. Driving $\overline{SYNC}$ LOW initiates a discharge cycle in the oscillator. Pulling $\overline{SHUTDOWN}$ LOW immediately inhibits all PWM output pulses. Holding $\overline{RESET}$ LOW discharges the soft-start capacitor. The logic threshold is +1.1 volts at 25°C. Noise immunity can be gained at the expense of fan-out with an external 2K pullup resistor to +5 volts.

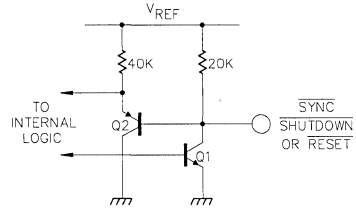


FIGURE 20.
DIGITAL CONTROL PORT SCHEMATIC

APPLICATION INFORMATION (continued)

OSCILLATOR

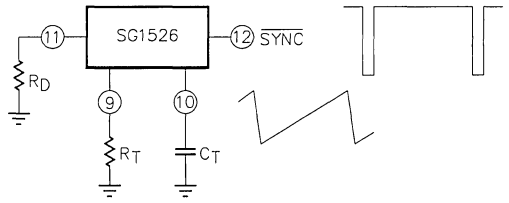


FIGURE 21 - OSCILLATOR CONNECTIONS AND WAVEFORMS

The oscillator is programmed for frequency and deadtime with three components: R_T, C_T, and R_D. Two waveforms are generated: a sawtooth waveform at pin 10 for pulse width modulation, and a logic clock at pin 12. The following procedure is recommended for choosing timing values:

1. With $R_D = 0\Omega$ (pin 11 shorted to ground) select values for R_T and C_T from Figure 7 to give the desired oscillator period. Remember that the frequency at each driver output is half the oscillator frequency, and the frequency at the $+V_C$ terminal is the same as the oscillator frequency.
2. If more dead time is required, select a larger value of R_D using Figure 6 as a guide. At 40kHz dead time increases by 400nSec/ohm.
3. Increasing the dead time will cause the oscillator frequency to decrease slightly. Go back and decrease the value of R_T slightly to bring the frequency back to the nominal design value.

The SG1526 can be synchronized to an external logic clock by programming the oscillator to free-run at a frequency 10% slower than the sync frequency. A periodic LOW logic pulse approximately 0.5µSec wide at the $\overline{SYNC}$ pin will then lock the oscillator to the external frequency.

Multiple devices can be synchronized together by programming one master unit for the desired frequency, and then sharing its sawtooth and clock waveforms with the slave units. All C_T terminals are connected to the C_T pin of the master, and all SYNC terminals are likewise connected to the $\overline{SYNC}$ pin of the master. Slave R_T terminals should not be left open nor should they be tied to the +5V reference; at least 50K should be connected to each pin. Slave R_D terminals may be either left open or grounded.

ERROR AMPLIFIER

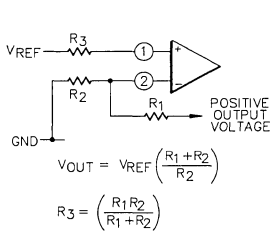


FIGURE 22A

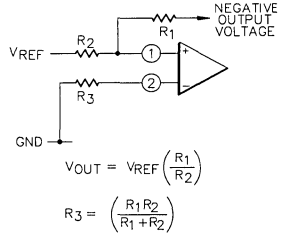


FIGURE 22B

ERROR AMPLIFIER CONNECTIONS

The error amplifier is a transconductance design, with an output impedance of 2 megohms and an effective output capacitance of 100 pF. Since all voltage gain takes place at the output pin, the open-loop gain can be shaped with shunt reactance to ground. For unity gain stability the amplifier requires an additional external 100 pF to ground, resulting in an open-loop pole at 400 Hz.

The input connections to the error amplifier are determined by the polarity of the switching supply output voltage. For positive supplies, the common-mode voltage is +5.0 volts and the feedback connections in Figure 22A are used. With negative supplies, the common-mode voltage is ground and the feedback divider is connected between the negative output and the +5.0 volt reference voltage, as shown in Figure 22B.

APPLICATION INFORMATION (continued)

OUTPUT DRIVERS

The totem-pole output drivers of the SG1526 are designed to source and sink 100mA continuously and 200mA peak. Loads can be driven either from the output pins 13 and 16, or from the $+V_C$ pin, as required. Curves for the saturation voltage at these outputs as a function of load current are found in Figures 14 and 15.

Since the bottom transistor of the totem-pole is allowed to saturate, there is a momentary conduction path from the $+V_C$ terminal to ground during switching. To limit the resulting current spikes a small resistor in series with pin 14 is always recommended. The resistor value is determined by the driver supply voltage, and should be chosen for 200mA peak currents, as shown in Figure 25.

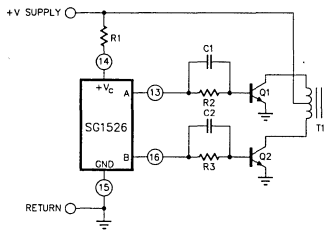


FIGURE 23.
PUSH-PULL CONFIGURATION

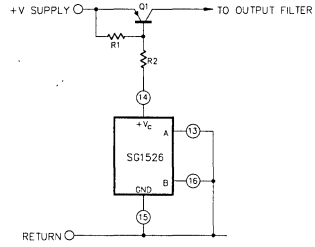


FIGURE 24.
SINGLE-ENDED CONFIGURATION

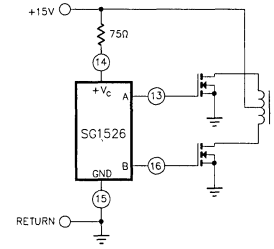
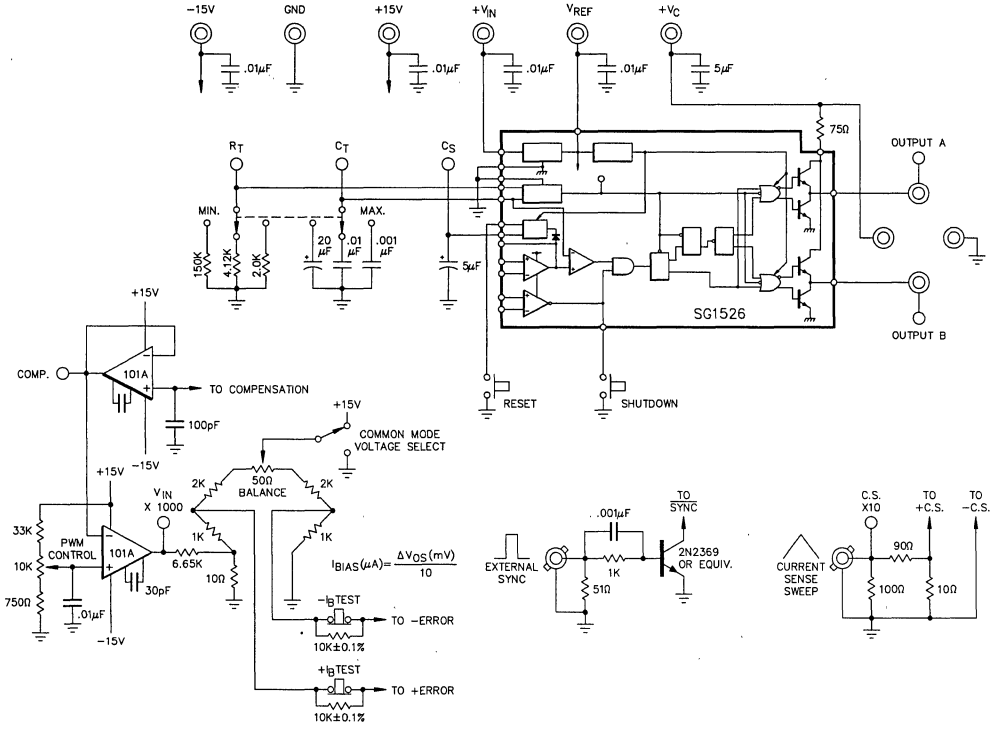
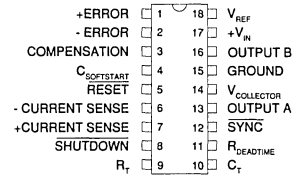
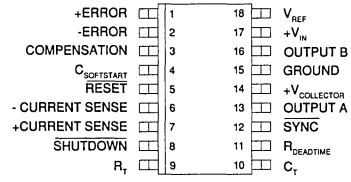
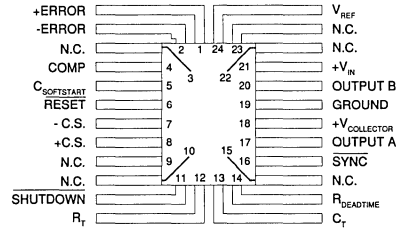
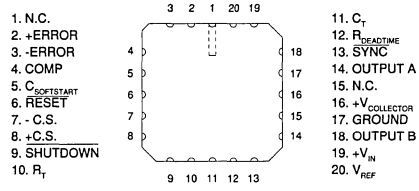


FIGURE 25.
DRIVING N-CHANNEL POWER MOSFETS

SG1526 LAB TEST FIXTURE



CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
18-PIN CERAMIC DIP J - PACKAGE	SG1526J/883B SG1526J SG2526J SG3526J	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
18-PIN PLASTIC DIP N - PACKAGE	SG2526N SG3526N	-25°C to 85°C 0°C to 70°C	
18-PIN WIDE BODY PLASTIC S.O.I.C. DW - PACKAGE	SG2526DW SG3526DW	-25°C to 85°C 0°C to 70°C	
24-PIN CERAMIC FLAT PACK F - PACKAGE	SG1526F/883B SG1526F	-55°C to 125°C -55°C to 125°C	
20-PIN CERAMIC LEADLESS CHIP CARRIER L- PACKAGE	SG1526L/883B SG1526L	-55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availability.
2. All parts are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

REGULATING PULSE WIDTH MODULATOR

DESCRIPTION

The SG1526B is a high-performance pulse width modulator for switching power supplies which offers improved functional and electrical characteristics over the industry-standard SG1526. A direct pin-for-pin replacement for the earlier device with all its features, it incorporates the following enhancements: a bandgap reference circuit for improved regulation and drift characteristics, improved undervoltage lockout, lower temperature coefficients on oscillator frequency and current-sense threshold, tighter tolerance on softstart time, much faster $\overline{\text{SHUTDOWN}}$ response, improved double-pulse supperession logic for higher speed operation, and an improved output driver design with low shoot-through current, and faster rise and fall times. This versatile device can be used to implement single-ended or push-pull switching regulators of either polarity, both transformer-less and transformer-coupled. The SG1526B is specified for operation over the full military ambient temperature range of -55°C to 150°C. The SG2526B is characterized for the industrial range of -25°C to 150°C, and the SG3526B is designed for the commercial range of 0°C to 125°C.

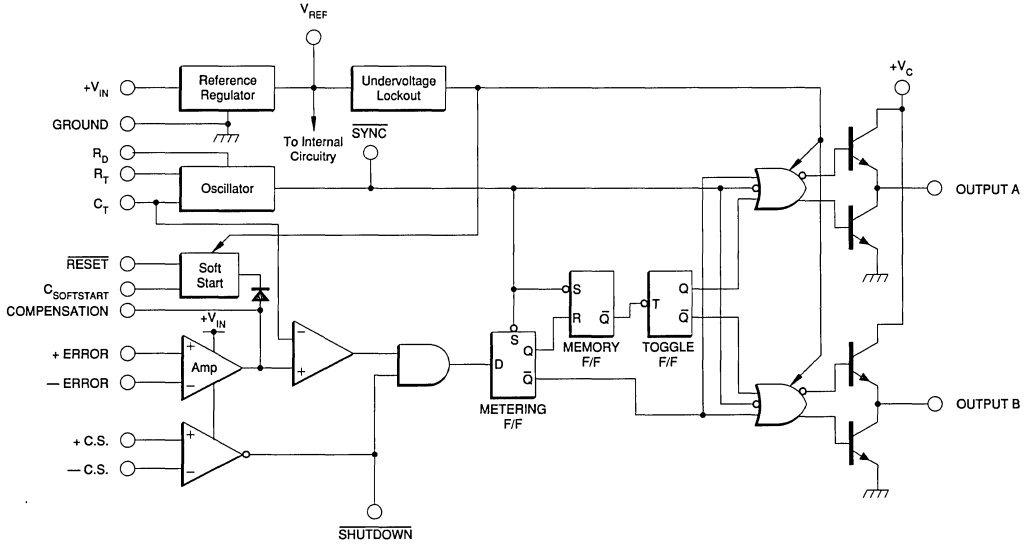
FEATURES

- **8 to 35 volt operation**
- **5V low drift 1% bandgap reference**
- **1Hz to 500KHz oscillator range**
- **Dual 100mA source/sink**
- **Digital current limiting**
- **Double pulse suppression**
- **Programmable deadtime**
- **Improved undervoltage lockout**
- **Single pulse metering**
- **Programmable soft-start**
- **Wide current limit common mode range**
- **TTL/CMOS compatible logic ports**
- **Symmetry correction capability**
- **Guaranteed 6 unit synchronization**
- **Shoot thru currents less than 100mA**
- **Improved shutdown delay**
- **Improved rise and fall time**

HIGH RELIABILITY FEATURES - SG1526B

- **Available to MIL-STD-883**
- **MIL-M38510/12603BVA - JAN1526BJ**
- **Radiation data available**
- **SG level "S" processing available**

BLOCK DIAGRAM



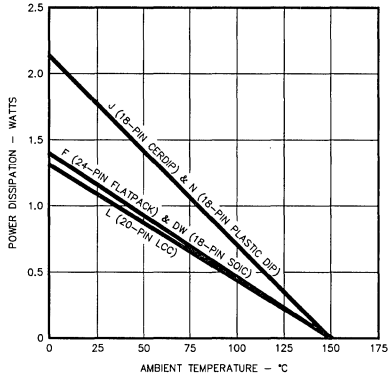
April 1990

ABSOLUTE MAXIMUM RATINGS (Note 1)

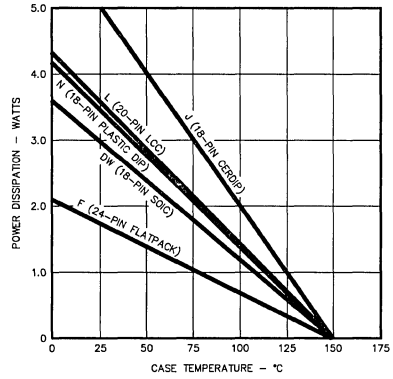
Input Voltage (V_{IN}) 40V
Collector Supply Voltage (V_C) 40V
Logic Inputs ..... -0.3V to 5.5V
Analog Inputs ..... -0.3V to V_{IN}
Source/Sink Load Current (each output) 200mA
Reference Load Current 50mA
Logic Sink Current 15mA
Operating Junction Temperature
Hermetic (J, F, L Packages) ..... 150°C
Plastic (N, DW Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Voltage ..... 8V to 35V
Collector Supply Voltage ..... 4.5V to 35V
Sink/Source Load Current (each output) ..... 0 to 100mA
Reference Load Current ..... 0 to 20mA
Oscillator Frequency Range ..... 1Hz to 500KHz
Oscillator Timing Resistor ..... 2KΩ to 150KΩ
Oscillator Timing Capacitor ..... 470pF to 20μF
Available Deadtime Range at 40KHz ..... 5% to 50%
Operating Junction Temperature Range:
SG1526B ..... -55°C to 125°C
SG2526B ..... -25°C to 85°C
SG3526B ..... 0°C to 70°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1526B with -55°C ≤ T_A ≤ 125°C, SG2526B with -25°C ≤ T_A ≤ 85°C, SG3526B with 0°C ≤ T_A ≤ 70°C, and V_{IN} = 15V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1526B/2526B			SG3526B			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Section (Note 3)								
Output Voltage	T_J = 25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	V_{IN} = 8 to 35V		7	10		10	20	mV
Load Regulation	I_L = 0 to 20mA		10	20		10	25	mV
Temperature Stability (Note 9)	Over Operating T_J		15	50		15	50	mV
Total Output Voltage Range (Note 9)		4.90	5.00	5.10	4.85	5.00	5.15	V
Short Circuit Current	V_{REF} = 0V	25	50	125	25	50	125	mA
Undervoltage Lockout Section								
$\overline{\text{RESET}}$ Output Voltage	V_{REF} = 3.8V		0.2	0.4		0.2	0.4	V
$\overline{\text{RESET}}$ Output Voltage	V_{REF} = 4.8V	2.4	4.8		2.4	4.8		V

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1526B/2526B			SG3526B			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Oscillator Section (Note 4)								
Initial Accuracy	T_J = 25°C		±3	±8		±3	±8	%
Voltage Stability	V_{IN} = 8 to 35V		0.5	1.0		0.5	1.0	%
Temperature Stability (Note 9)	Over Operating T_J		7	10		3	5	%
Minimum Frequency (Note 9)	R_T = 150KΩ, C_T = 20µF			1.0			1.0	Hz
Maximum Frequency	R_T = 2KΩ, C_T = 470pF	500			500			KHz
Sawtooth Peak Voltage	V_{IN} = 35V	2.5	3.0	3.5	2.5	3.0	3.5	V
Sawtooth Valley Voltage	V_{IN} = 8V	0.5	1.0	1.1	0.5	1.0	1.1	V
$\overline{SYNC}$ Pulse Width	R_L = 2.0KΩ to V_{REF}		1.0	2		1.0	2	µs
Error Amplifier Section (Note 5)								
Input Offset Voltage	R_S ≤ 2KΩ		2	5		2	10	mV
Input Bias Current			-350	-1000		-350	-2000	nA
Input Offset Current			35	100		35	200	nA
DC Open Loop Gain	R_L ≥ 10MΩ	64	72		60	72		dB
High Output Voltage	V_{PIN1} - V_{PIN2} ≥ 150mV, I_{SOURCE} = 100µA	3.6	4.2		3.6	4.2		V
Low Output Voltage	V_{PIN2} - V_{PIN1} ≥ 150mV, I_{SINK} = 100µA		0.2	0.4		0.2	0.4	V
Common Mode Rejection	R_S ≤ 2KΩ	70	94		70	94		dB
Supply Voltage Rejection	V_{IN} = 8V to 35V	66	80		66	80		dB
PWM Comparator Section (Note 4)								
Minimum Duty Cycle	$V_{COMPENSATION}$ = 0.4V			0			0	%
Maximum Duty Cycle	$V_{COMPENSATION}$ = 3.6V	45	49		45	49		%
Digital Ports ($\overline{SYNC}$, $\overline{SHUTDOWN}$, and $\overline{RESET}$)								
HIGH Output Voltage	I_{SOURCE} = 40µA	2.4	4		2.4	4		V
LOW Output Voltage	I_{SINK} = 3.6mA		0.2	0.4		0.2	0.4	V
HIGH Input Current	V_{IH} = 2.4V		-125	-200		-125	-200	µA
LOW Input Current	V_{IL} = 0.4V		-225	-360		-225	-360	µA
$\overline{SHUTDOWN}$ Delay to Output	(Note9)			200			200	ns
Current Limit Comparator Section (Note 6)								
Sense Voltage	R_S ≤ 50Ω	90	100	110	80	100	120	mV
Input Bias Current			-3	-10		-3	-10	µA
Delay to Output (Note 9)				400			400	ns
Soft-Start Section								
Error Clamp Voltage	$\overline{RESET}$ = 0.4V		0.1	0.4.		0.1	0.4.	V
C_S Charging Current	$\overline{RESET}$ = 2.4V	50	100	150	50	100	150	µA
Output Drivers (each output) (Note 7)								
HIGH Output Voltage	I_{SOURCE} = 20mA	12.5	13.5		12.5	13.5		V
	I_{SOURCE} = 100mA	12	13		12	13		V
LOW Output Voltage	I_{SINK} = 20mA		0.2	0.3		0.2	0.3	V
	I_{SINK} = 100mA		1.2	2		1.2	2	V
Collector Leakage	V_C = 40V		50	150		50	150	µA
Rise Time	C_L = 1000pF		0.3	0.4		0.3	0.4	µs
Fall Time	C_L = 1000pF		0.1	0.15		0.1	0.15	µs
Power Consumption Section (Note 8)								
Standby Current	$\overline{SHUTDOWN}$ = 0.4V		18	30		18	30	mA

Note 3. I_L = 0mA
Note 4. F_{OSC} = 40KHz (R_T = 4.12KΩ ±1%, C_T = .01µF ±1%, R_D = 0Ω)
Note 5. V_{CM} = 0 to 5.2V
Note 6. V_{CM} = 0 to 12V
Note 7. V_C = 15V
Note 8. V_{IN} = 35V
Note 9. These parameters, although guaranteed over the recommended operating conditions, are not tested in production.

CHARACTERISTIC CURVES

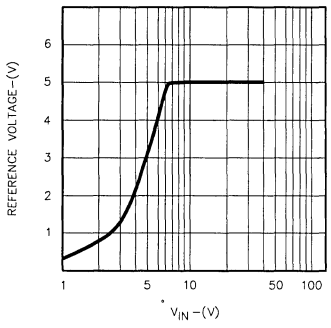


FIGURE 1.
REFERENCE VOLTAGE VS. SUPPLY VOLTAGE

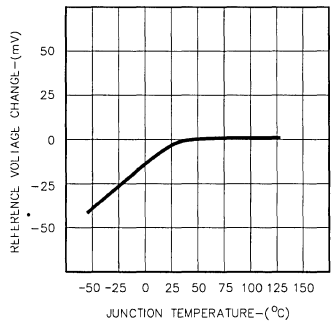


FIGURE 2.
REFERENCE TEMPERATURE STABILITY

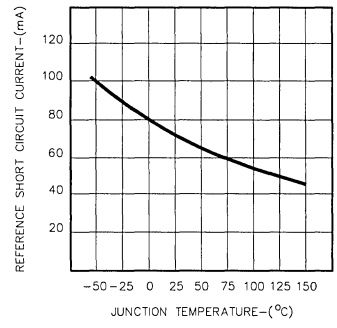


FIGURE 3.
REFERENCE SHORT CIRCUIT

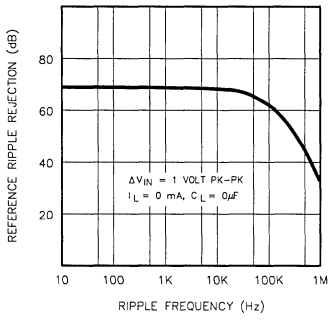


FIGURE 4.
REFERENCE RIPPLE REJECTION

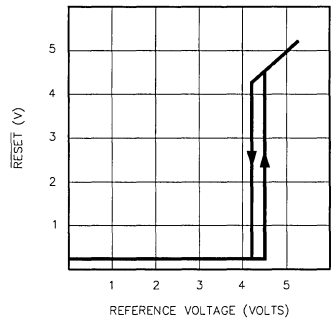


FIGURE 5.
UNDER VOLTAGE LOCKOUT

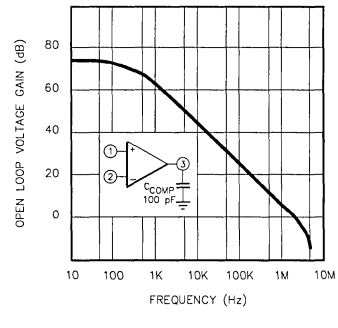


FIGURE 6.
ERROR AMPLIFIER OPEN LOOP GAIN
VS. FREQUENCY

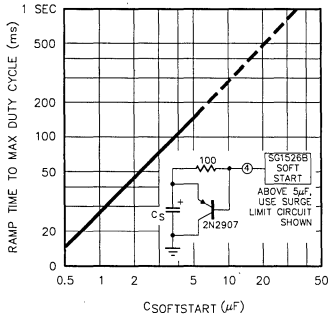


FIGURE 7.
SOFTSTART TIME CONSTANT VS. C_S

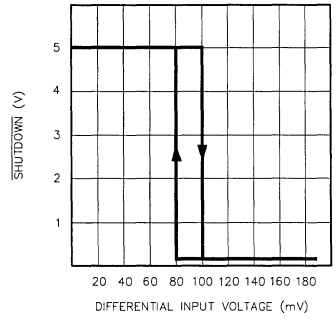


FIGURE 8.
CURRENT LIMIT TRANSFER FUNCTION

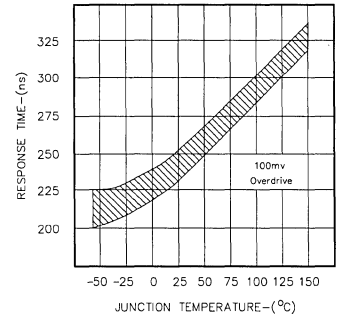


FIGURE 9.
COMPARATOR INPUT TO DRIVER OUTPUT DELAY

CHARACTERISTIC CURVES (continued)

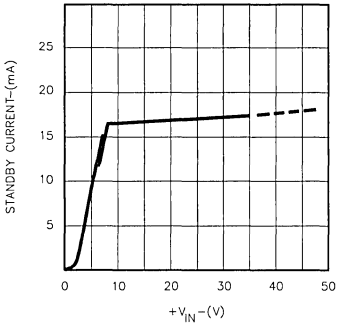


FIGURE 10.
STANDBY CURRENT VS. SUPPLY VOLTAGE

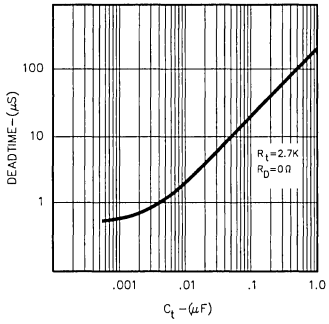


FIGURE 11.
OUTPUT DRIVER DEADTIME VS. C_T VALUE

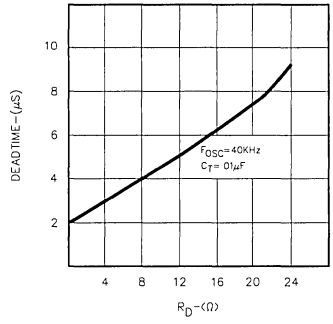


FIGURE 12.
OUTPUT DRIVER DEADTIME VS. R_D VALUE

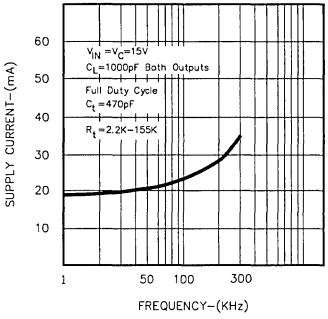


FIGURE 13.
SUPPLY CURRENT VS. OUTPUT FREQUENCY

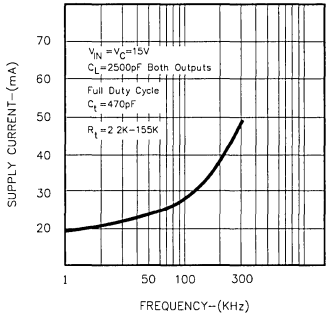


FIGURE 14.
SUPPLY CURRENT VS. OUTPUT FREQUENCY

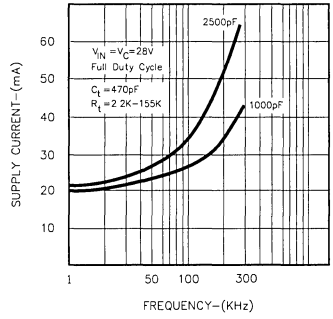


FIGURE 15.
SUPPLY CURRENT VS. OUTPUT FREQUENCY

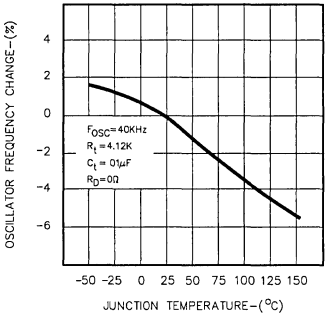


FIGURE 16.
OSCILLATOR FREQUENCY
TEMPERATURE STABILITY

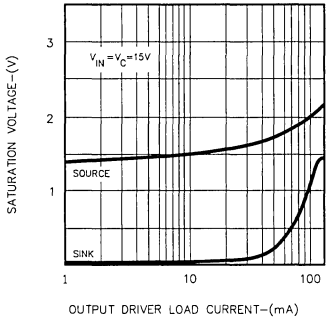


FIGURE 17.
OUTPUT DRIVER SATURATION VOLTAGE

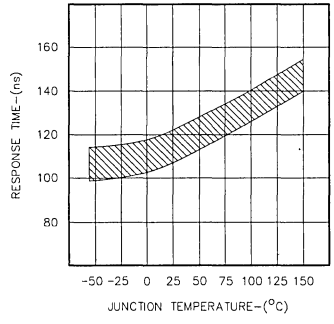


FIGURE 18.
SHUTDOWN INPUT TO DRIVER OUTPUT DELAY

CHARACTERISTIC CURVES (continued)

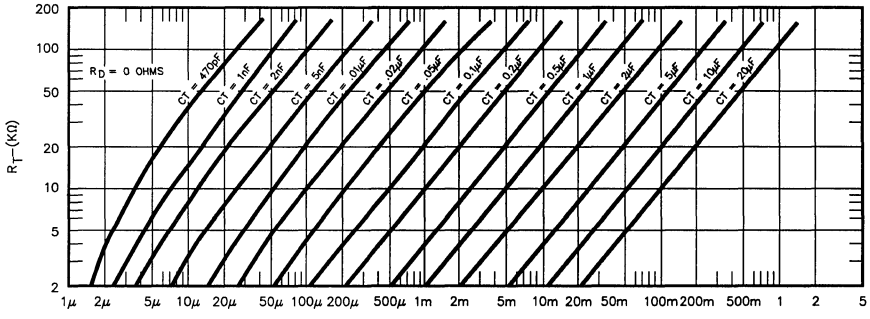


FIGURE 19.
OSCILLATOR PERIOD VS. R_T AND C_T

APPLICATION INFORMATION

VOLTAGE REFERENCE

The reference regulator of the SG1526B is a "band-gap" type; that is, the precision +5 volt output is derived from the very predictable base-emitter voltage of an NPN transistor. Since this is a sub-surface phenomenon, the resulting output exhibits excellent stability compared to earlier surface-breakdown zener designs.

The reference output is stabilized at input voltages as low as +8 volts, and can provide up to 20mA of load current to external circuitry. An external PNP transistor can be used to boost the available current to many hundreds of mA. A rugged low-frequency audio-type transistor should be used, and lead lengths between the PWM and transistor should be as short as possible to minimize the risk of oscillation.

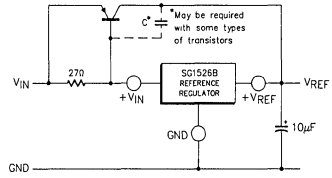


FIGURE 20.
EXTENDING REFERENCE OUTPUT CURRENT

UNDERVOLTAGE LOCKOUT

The undervoltage lockout circuit protects the SG1526B and the power devices it controls from inadequate supply voltage. If $+V_{IN}$ is too low, the circuit disables the output drivers and holds the $\overline{\text{RESET}}$ pin LOW. This prevents spurious output pulses while the control circuitry is stabilizing, and holds the soft-start timing capacitor in a discharged state.

The circuit consists of a merged bandgap reference and comparator circuit which is active when the reference voltage has risen to $2V_{BE}$ or 1.2 volts at 25°C. When the reference voltage rises to approximately +4.4 volts, the circuit enables the output drivers and releases the $\overline{\text{RESET}}$ pin, allowing a normal softstart. The comparator has 200mV of hysteresis to minimize oscillation at the trip point. When $+V_{IN}$ to the PWM is removed and the reference drops to +4.2 volts, the undervoltage circuit pulls $\overline{\text{RESET}}$ LOW again. The soft-start capacitor is immediately discharged, and the PWM is ready for another soft-start cycle.

The SG1526B can operate from a +5 volt supply regulated to within ±4% by connecting the V_{REF} pin to the $+V_{IN}$ pin.

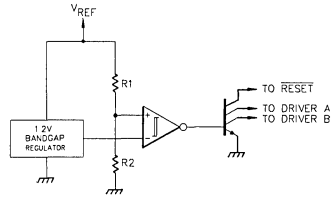


FIGURE 21.
SIMPLIFIED UNDERVOLTAGE LOCKOUT

SOFT-START CIRCUIT

The soft-start circuit protects the power transistors and rectifier diodes from high current surges during power supply turn-on. When supply voltage is first applied to the SG1526B, the undervoltage lockout circuit holds $\overline{\text{RESET}}$ LOW with Q3. Q1 is turned on, which holds the soft-start capacitor voltage at zero. The second collector of Q1 clamps the output of the error amplifier to ground, guaranteeing zero duty cycle at the driver outputs. When the supply voltage reaches normal operating range, $\overline{\text{RESET}}$ will go HIGH. Q1 turns off, allowing the internal 100μA current source to charge C_S. Q2 clamps the error amplifier output to 1.0 V_{BE} above the voltage on C_S. As the soft-start voltage ramps up to +5 volts, the duty cycle of the PWM linearly increases to whatever value the voltage regulation loop requires for an error null. Figure 7 gives the timing relationship between C_S ramp time to 100% duty cycle.

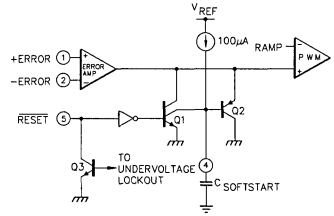


FIGURE 22.
SOFT-START CIRCUIT SCHEMATIC

APPLICATION INFORMATION (continued)

DIGITAL CONTROL PORTS

The three digital control ports of the SG1526B are bi-directional. Each pin can drive TTL and 5 volt CMOS logic directly, up to a fan-out of 10 low-power Schottky gates. Each pin can also be directly driven by open-collector TTL, open-drain CMOS, and open-collector voltage comparators, fan-in is equivalent to 1 low-power Schottky gate. Each port is normally HIGH; the pin is pulled LOW to activate the particular function. Driving $\overline{\text{SYNC}}$ LOW initiates a discharge cycle in the oscillator. Pulling SHUTDOWN LOW immediately inhibits all PWM output pulses. Holding $\overline{\text{RESET}}$ LOW discharges the soft-start capacitor. The logic threshold is +1.1 volts at +25°C. Noise immunity can be gained at the expense of fan-out with an external 2K pull-up resistor to +5 volts.

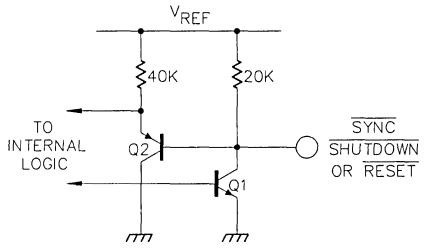


FIGURE 23
DIGITAL CONTROL PORT SCHEMATIC

OSCILLATOR

The oscillator is programmed for frequency and dead time with three components: R_T C_T, and R_D. Two waveforms are generated: a sawtooth waveform at pin 10 for pulse width modulation, and a logic clock at pin 12. The following procedure is recommended for choosing timing values:

1. With $R_D = 0\Omega$ (pin 11 shorted to ground) select values for R_T and C_T from Figure 19 to give the desired oscillator period. Remember that the frequency at each driver output is half the oscillator frequency, and the frequency at the $+V_C$ terminal is the same as the oscillator frequency.
2. If more dead time is required, select a larger value of R_D using Figure 14 as a guide. At 40 KHz dead time increases by 300 ns/Ω.
3. Increasing the dead time will cause the oscillator frequency to decrease slightly. Go back and decrease the value of R_T slightly to bring the frequency back to the nominal design value.

The SG1526B can be synchronized to an external logic clock by programming the oscillator to free-run at a frequency 10% slower than the sync frequency. A periodic LOW logic pulse approximately 0.5 µSec wide at the $\overline{\text{SYNC}}$ pin will then lock the oscillator to the external frequency.

Multiple devices can be synchronized together by programming one master unit for the desired frequency, and then sharing its sawtooth and clock waveforms with the slave units. All C_T terminals are connected to the C_T pin of the master, and all $\overline{\text{SYNC}}$ terminals are likewise connected to the $\overline{\text{SYNC}}$ pin of the master. Slave R_T terminals should not be left open; at least 50K should be connected from each pin to ground. Slave R_D terminals may be either left open or grounded.

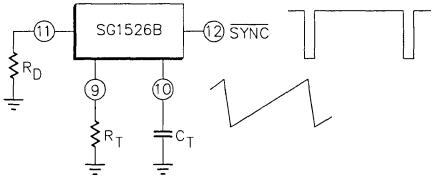


FIGURE 24.
OSCILLATOR CONNECTIONS ANDD WAVEFORMS

ERROR AMPLIFIER

The error amplifier is a transconductance design, with an output impedance of 2 megohms. Since all voltage gain takes place at the output pin, the open-loop gain/frequency characteristics can be controlled with shunt reactance to ground. When compensated for unity-gain stability with 100 pF, the amplifier has an open-loop pole at 400 Hz.

The input connections to the error amplifier and determined by the polarity of the switching supply output voltage. For positive supplies, the common-mode voltage is +5.0 volts and the feedback connections in Figure 25A are used. With negative supplies, the common-mode voltage is ground and the feedback divider is connected between the negative output and the +5.0 volt reference voltage, as shown in Figure 25B.

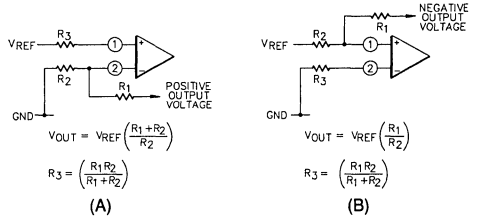


FIGURE 25.
ERROR AMPLIFIER CONNECTIONS

APPLICATION INFORMATION (continued)

OUTPUT DRIVERS

The totem-pole output drivers of the SG1526B are designed to source and sink 100mA continuously and 200mA peak. Loads can be driven either from the output pins 13 and 16, or from the $+V_C$ pin, as required. Curves for the saturation voltage at these outputs as a function of load current are found in Figure 17.

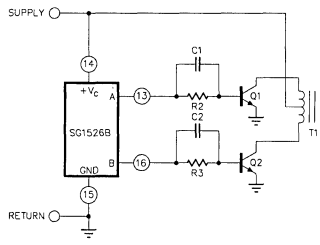


FIGURE 26.
PUSH-PULL CONFIGURATION

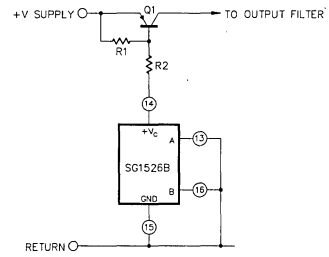


FIGURE 27.
SINGLE-ENDED CONFIGURATION

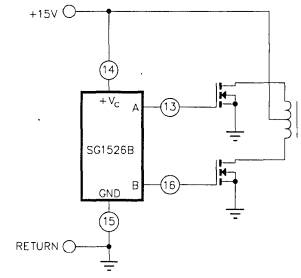
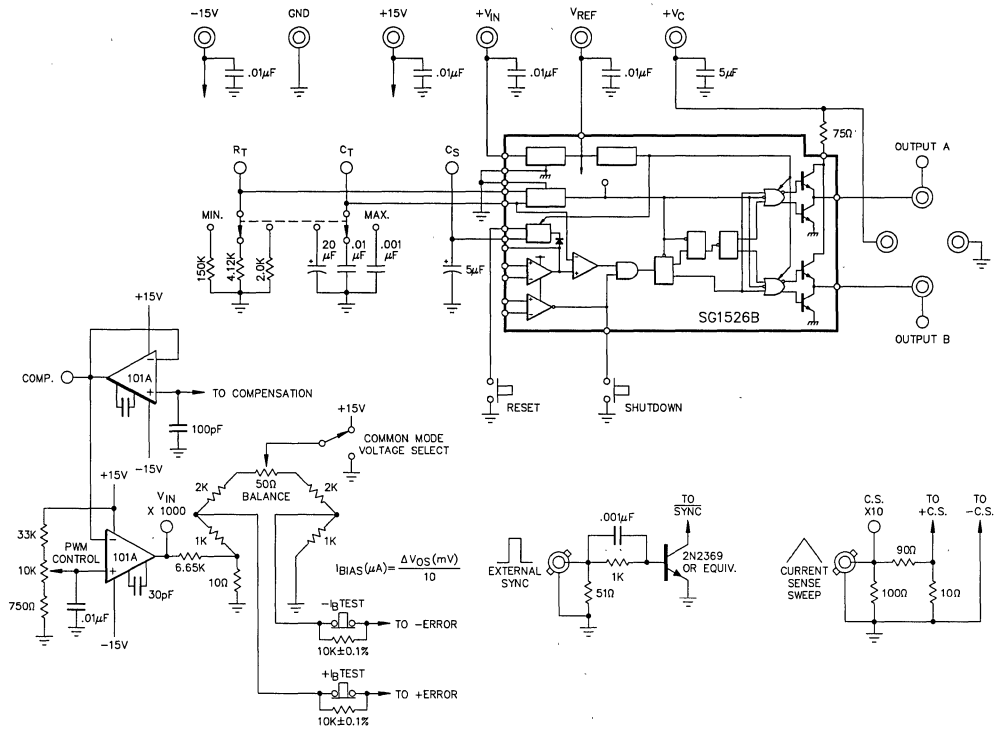
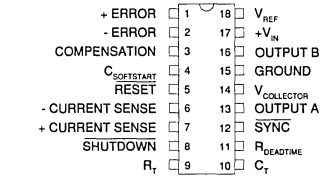
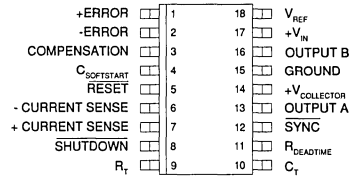
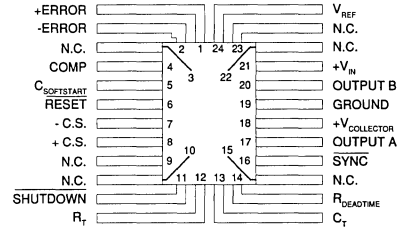
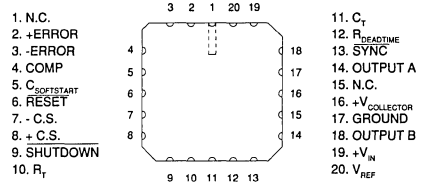


FIGURE 28.
DRIVING N-CHANNEL POWER MOSFETS

SG1526B LAB TEST FIXTURE



CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
18-PIN CERAMIC DIP J - PACKAGE	SG1526BJ/883B SG1526BJ SG2526BJ SG3526BJ	-55°C to 125°C -55°C to 125°C -55°C to 125°C 0°C to 70°C	
18-PIN PLASTIC DIP N - PACKAGE	SG2526BN SG3526BN	-25°C to 85°C 0°C to 70°C	
18-PIN WIDE BODY PLASTIC S.O.I.C. DW - PACKAGE	SG2526BDW SG3526BDW	-25°C to 85°C 0°C to 70°C	
24-PIN CERAMIC FLAT PACK F - PACKAGE	SG1526BF/883B SG1526BF	-55°C to 125°C -55°C to 125°C	
20-PIN CERAMIC LEADLESS CHIP CARRIER L- PACKAGE	SG1526BL/883B SG1526BL	-55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availability.
2. All parts are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SG1528/SG2528/SG3528
SG1530/SG2530/SG3530

FUTURE PRODUCT RELEASE

HIGH SPEED CURRENT MODE PWM CONTROLLER

DESCRIPTION

The SG1528/30 family of single-ended pulse width modulators are optimized for high frequency, current mode control of switching power supply applications. The control architecture also allows its use as a uni-directional motor speed controller. The circuit features internally preset start-up and run voltage thresholds compatible with power N-channel MOSFETs. A precision low-drift bandgap reference exhibits excellent long-term stability. Both the voltage error amp and current amp are wideband operational amplifiers for high speed performance and maximum applications flexibility. A high peak-current totem-pole output driver permits direct drive of the power switch. The difference between these two series of controllers is the maximum duty cycle range of the output stage. The SG1530 family can operate to duty cycles approaching 100%, where they are mainly used in non-isolated DC-DC converters whereas the 1528 series has a duty cycle range of zero to <50%, optimized for isolated, primary-side control of switching power supplies. The SG1528/1530 is specified for operation over the full military ambient temperature range of -55°C to 125°C. The SG2528/2530 is characterized for the industrial range of -25°C to 85°C, and the SG3528/3530 is designed for the commercial range of 0°C to 70°C.

FEATURES

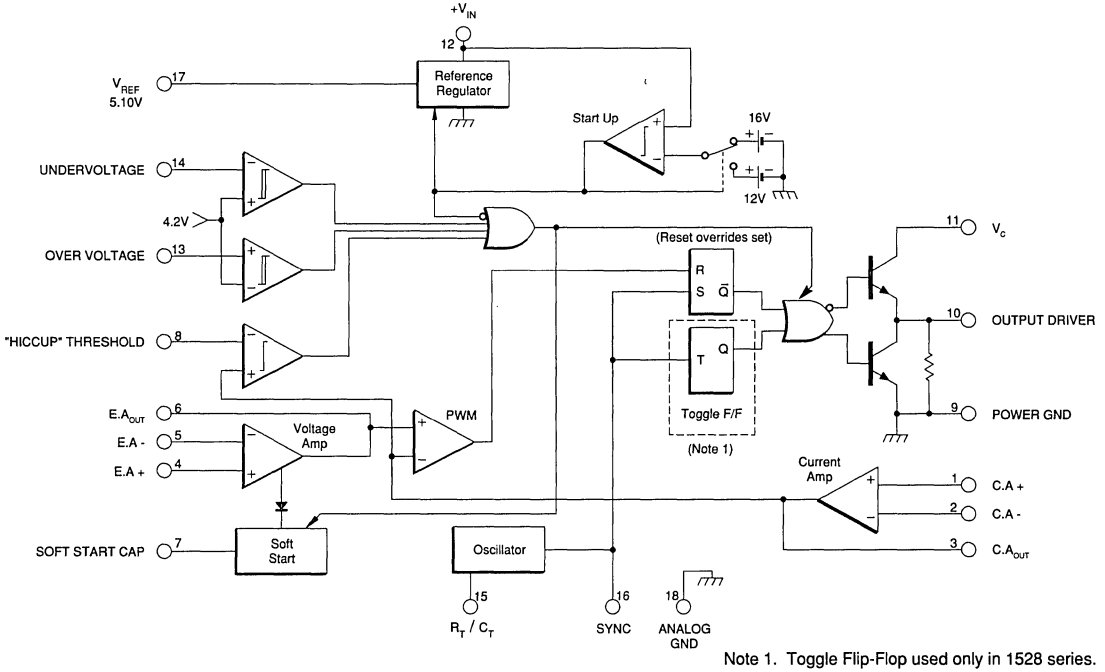
- **Current mode or voltage mode control**
- **Micropower start-up mode (0.6mA max.)**
- **±1% Low-drift reference**
- **Wideband voltage error amp (6MHz typ.)**
- **Wideband current differential amp (12MHz typ.)**
- **Output Frequencies to 2MHz**
- **Programmable DC Bus O.V. and U.V. sense**
- **High speed shutdown**
- **Soft start**
- **Full fault suppression logic**
- **2A peak output current drive**
- **Output driver rise and fall time less than 30ns**
- **Ideal for using with SENSFETS**

HIGH RELIABILITY FEATURES - SG1528/SG1530

- **Available to MIL-STD-883**
- **SG level "S" processing available**

4

BLOCK DIAGRAM



Note 1. Toggle Flip-Flop used only in 1528 series.

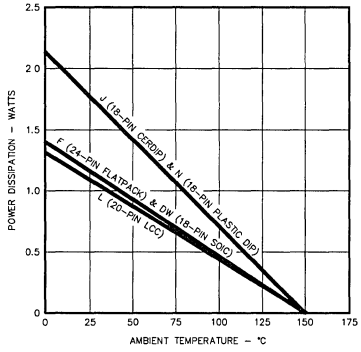
April 1990

ABSOLUTE MAXIMUM RATINGS (Note 2)

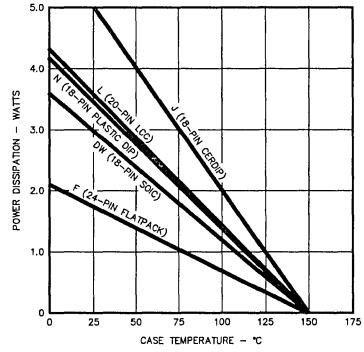
Supply Voltage (V_{IN}, V_C) 22V
Analog Inputs (ERR, CUR, OV, UV) ..... -0.3V to V_{IN}
Logic Inputs (SYNC) ..... -0.3V to 5.5V
Source / Sink Load Current (continuous) 0.5A
Source / Sink Load Current Peak (200ns) 3A
Reference Load Current 50mA
Soft Start Discharge Current 50mA
Sync Output Source Current 5mA
Error Amplifier Output Current 5mA
Current Sense Amplifier Output Current 5mA
Oscillator Discharging Current 5mA
Operating Junction Temperature
Hermetic (J, F, L Packages) ..... 150°C
Plastic (N, DW Packages) ..... 150°C
Storage Temperature ..... -65°C to 150°C

Note 2. Values beyond which damage may occur.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 3. Range over which the device is functional.)

Collector Voltage ..... 4.5V to 20V
Supply Voltage Range ..... 13V to 20V
Source / Sink Output Current (continuous) 0.3A
Source / Sink Output Current Peak (200ns) 1.5A
Reference Load Current ..... 0 to 10mA
Oscillator Frequency Range ..... 1KHz to 1.5MHz
Oscillator Timing Resistor (R_T) ..... 1KΩ to TBD
Oscillator Timing Capacitor (C_T) ..... 500pF to 0.1μF
Operating Ambient Temperature Range
SG1528 ..... -55°C to 125°C
SG2528 ..... -25°C to 85°C
SG3528 ..... 0°C to 70°C

ELECTRICAL SPECIFICATIONS (Note 4)

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1528/SG1530 with $-55°C \le T_A \le 125°C$, SG2528/SG2530 with $-25°C \le T_A \le 85°C$, SG3528/SG3530 with $0°C \le T_A \le 70°C$, and $V_{IN} = V_C = 15V$ (Note 5). Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1528/2528 SG1530/2530			SG3528 SG3530			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Section								
Output Voltage	$T_J = 25°C$, $I_O = 1mA$	5.05	5.10	5.15	5.05	5.10	5.15	V
Line Regulation	$V_{IN} = 13V$ to 20V		3	15		3	15	mV
Load Regulation	$I_L = 1$ to 10mA		2	15		2	15	mV
Temperature Stability (Note 6)			20	40		20	40	mV
Total Output Variation	Line, Load and Temp	5.0		5.2	5.0		5.2	V
Output Noise Voltage (Note 6)	$T_J = 25°C$, 10Hz < f < 10KHz		100			100		μV/rms
Long-Term Stablility (Note 6, 7)	$T_J = 125°C$, 1000Hrs		5	25		5	25	mV
Short Circuit Output Current	$V_{REF} = 0V$	15	50	100	15	50	100	mA
Oscillator Section (Note 8)								
Initial Accuracy	$T_J = 25°C$, $C_{SYNC} \le 10pF$	0.9	1.0	1.1	0.9	1.0	1.1	MHz
Voltage Stability	$V_{IN} = 13V$ to 20V			±0.5			±0.5	%
Temperature Stability	Over Operating Range		±4	±8		±4	±8	%
Minimum Frequency	R_T = TBD ; C_T = TBD		0.5	1.0		0.5	1.0	KHz
Maximum Frequency	R_T = TBD ; C_T = TBD	2	3		2	3		MHz
Ramp Peak Voltage			3.8			3.8		V

ELECTRICAL SPECIFICATIONS (continued)

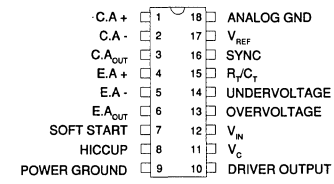
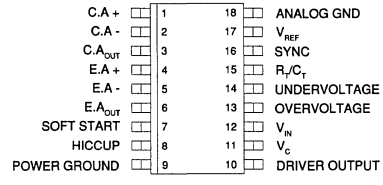
Parameter	Test Conditions	SG1528/2528 SG1530/2530			SG3528 SG3530			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Oscillator Section (Note 8)								
Ramp Valley Voltage			2.8			2.8		V
Ramp Valley to Peak Amplitude		0.9	1.0	1.1	0.9	1.0	1.1	V
Sync Output High Level	T_J = 25°C, I_{SYNC} = 1mA	4.2	4.35	4.5	4.2	4.35	4.5	V
Sync Output Low Level	T_J = 25°C, I_{SYNC} = 1mA	3.35	3.55	3.75	3.35	3.55	3.75	V
Sync Input High Level (Note 6)	T_J = 25°C	4.25			4.25			V
Sync Input Low Level (Note 6)	T_J = 25°C			3.6			3.6	V
Sync Input Current, High & Low	(Note 6)		1	2		1	2	mA
Sync Output Pulse	$C_{CLK} \leq$ 10pF, I_{SYNC} = 0mA	200	275	350	200	275	350	ns
Error Amplifier Section (E.A) (Note 9)								
Input Offset Voltage	$R_S \leq 100\Omega$, $E.A_{OUT}$ = 2.5V			5			5	mV
Input Bias Current	V_{CM} = 2.5V			15			15	µA
Input Offset Current	V_{CM} = 2.5V			2.5			2.5	µA
Common Mode Range		1.7		7	1.7		7	V
Open Loop Gain	V_{CM} = 2.5V, Output Volt. 1 to 2.5V, R_L = 10K	60	64		60	64		dB
Unity Gain Bandwidth (Note 6)	A_{VOL} = 0dB	4	6		4	6		MHz
Output Voltage Slew Rate (Note 6)	See Figure TBD	5	10		5	10		V/µs
CMRR	V_{CM} = 1.7V to 7V	75	100		75	100		dB
PSRR	V_{IN} = 13V to 20V	90			90			dB
Output Sink Current	$E.A_{OUT}$ = 2V, ΔV = 150mV	0.4	0.7		0.4	0.7		mA
Output Source Current	$E.A_{OUT}$ = 2V, ΔV = 150mV	3	6		3	6		mA
Output High Level	R_L = 10K	2.6	2.8	3.8	2.6	2.8	3.8	V
Output Low Level	R_L = 10K		0.1	0.3		0.1	0.3	V
Current Sense Amplifier (C.A) Section (Note 10)								
Input Offset Voltage	$R_{CM} \leq 10\Omega$, $C.A_{OUT}$ = 2.5V, V_{CM} = 1.5V		2.5	5		2.5	5	mV
Input Bias Current	V_{CM} = 0.1V		200	500		200	500	µA
Input Offset Current	V_{CM} = 0.1V			50			50	µA
Common Mode Range		0.1		7	0.1		7	V
Open Loop Gain	V_{CM} = 1.5V, Output Voltage 1 to 2.5V, R_L = 5K	60	64		60	64		dB
Unity Gain Bandwidth (Note 6)	A_{VOL} = 0dB	8	12		8	12		MHz
Output Voltage Slew Rate (Note 6)	See Figure TBD	10	20		10	20		V/µs
CMRR	V_{CM} = 0.1V to 7V, $C.A_{OUT}$ = 2.5V	75	100		75	100		dB
PSRR	V_{IN} = 13V to 20V, V_{CM} = 0.1	90			90			dB
Output Sink Current	$C.A_{OUT}$ = 2V, V_{CM} = 2.5V, ΔV = 75mV	0.5	1.33		0.5	1.33		mA
Output Source Current	$C.A_{OUT}$ = 2V, V_{CM} = 2.5V, ΔV = 75mV	5	10		5	10		mA
Delay to Output (Note 6)	$C.A_{OUT}$ = 0.5V to 2V, $E.A_{OUT}$ = 1.5V			80			80	ns
Output High Level	R_L = 5K	2.7	3.5		2.7	3.5		V
Output Low Level	R_L = 5K		0.2	0.4		0.2	0.4	V
"Hiccup" Section								
Input Offset Voltage	$R_S \leq 10\Omega$, V_{CM} = 1.7V to 2.5V			10			10	mV
Input Bias Current	$C.A_{OUT}$ = 2.5V, V_{HICCUP} = 1.7V to 3.5V			10			10	µA
Common Mode Range		1.7		3.5	1.7		3.5	V
Delay to Output (Note 6)	$C.A_{OUT}$ = 2.2V, V_{HICCUP} = 2V, $E.A_{OUT}$ = 2.5V		60	650		60	650	ns
Overvoltage/Undervoltage Section								
Overvoltage Threshold Voltage	I_{REF} = 1mA	4.0	4.2	4.4	4.0	4.2	4.4	V
Overvoltage Hysteresis	I_{REF} = 1mA	350	450	550	350	450	550	mV
Undervoltage Threshold Voltage	I_{REF} = 1mA	4.0	4.2	4.4	4.0	4.2	4.4	V
Undervoltage Hysteresis	I_{REF} = 1mA	660	830	1000	660	830	1000	mV
Delay to Output (Note 6)	O.V. = V_{REF} + 0.2V		550	800		550	800	ns
O.V. Input Bias Current	O.V. Input = 10V		2	6		2	6	µA
U.V. Input Bias Current	U.V. Input = 10V		2	6		2	6	µA

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1528/2528 SG1530/2530			SG3528 SG3530			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Section								
Collector Leakage Current	V_C = 20V, Output off			0.5			0.5	mA
Output High Level	I_{SOURCE} = 50mA	13	13.5		13	13.5		V
	I_{SOURCE} = 200mA	12.5	13.5		12.5	13.5		V
Output Low Level	I_{SINK} = 50mA		0.3	0.5		0.3	0.5	V
	I_{SINK} = 200mA		1	2		1	2	V
Maximum Duty Cycle (Note 8)	$E.A_{OUT}$ = 2V, $C.A_{OUT}$ = 1.5V	45	48	51	45	48	51	%
Zero Duty Cycle	$E.A_{OUT}$ = 0.5V, $C.A_{OUT}$ = 0.6V			0			0	%
Rise Time (Note 6)	C_L = 1nF		25	50		25	50	ns
Fall Time (Note 6)	C_L = 1nF		20	50		20	50	ns
Bleeding Resistor	Tristate Output, V_{IN} = 11V (Note 6)	10		60	10		60	KΩ
Cross Conduction Current (Note 6)	C_L = 1nF		6	60		6	60	nJ/Hz
Start Up Section								
Start Up Voltage		15.5	16	16.5	15.5	16	16.5	V
Start Up Current	V_{IN} = Start-Up Threshold		350	600		350	600	µA
Shut Down Voltage		11.5	12	12.5	11.5	12	12.5	V
Delay to Output on Shut Down	Output Low, V_{IN} = 11V (Note 6)		150	300		150	300	ns
Soft-Start Section								
Soft Start Charging Current	$V_{SOFTSTART}$ = 0.5V, V_{HICCUP} = 4V	35	45	55	35	45	55	µA
Soft Start Discharge Current	$V_{SOFTSTART}$ = 11V, V_{IN} = 11V	30			30			mA
Soft Start Discharge Voltage	$I_{DISCHARGE}$ = 30mA			2			2	V
Power Consumption Section								
Total Supply Current	f_O = 200KHz, C_L = 1000pF		35	50		35	50	mA
Standby Current	$V_{U.V}$ = 3.5V			20			20	mA

Note 4. Performance data described herein represent design goals. Final device specifications are subject to change.
Note 5. Adjust V_{IN} above the start threshold before setting it to 15V.
Note 6. This parameter, although guaranteed, is not tested in production.
Note 7. This parameter is non-accumulative, and represents the random fluctuation of the reference voltage within some error band when observed over any 1000 hour period of time.
Note 8. F_{OSC} = 1MHz (R_T = TBD , C_T = TBD)
Note 9. C.A - = 1.1V, C.A + = 1V
Note 10. E.A - = 2.5V, E.A + = 2.4V

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
18-PIN CERAMIC DIP J - PACKAGE	SG1528J/883B	-55°C to 125°C	
	SG1528J	-55°C to 125°C	
	SG2528J	-25°C to 85°C	
	SG3528J	0°C to 70°C	
	SG1530J/883B	-55°C to 125°C	
	SG1530J	-55°C to 125°C	
	SG2530J	-25°C to 85°C	
	SG3530J	0°C to 70°C	
18-PIN WIDE BODY PLASTIC S.O.I.C. DW - PACKAGE	SG2528DW	-25°C to 85°C	
	SG3528DW	0°C to 70°C	
	SG2530DW	-25°C to 85°C	
	SG3530DW	0°C to 70°C	

Notes: 1. Contact factory for JAN and DESC product availability.
2. All parts are viewed from the top.
3. Product is also available in leadless chip carrier (LCC) and 24-pin hermetic flat pack (F). Contact factory for price and availability.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

REGULATING PULSE WIDTH MODULATOR

DESCRIPTION

The SG1529 series of pulse width modulator integrated circuits are designed to provide all the operational features of the SG1524B series with the added advantage of an uncommitted input to the PWM comparator. This allows the device to be used in Feed-Forward regulation schemes to achieve better line regulation as well as improved dynamic response. A 5V bandgap reference trimmed to ±1% tolerance, an error amplifier, and a current limit comparator with a high common mode range are included in the I.C.

A DC coupled flip-flop eliminates triggering and glitch problems, and a PWM data latch prevents edge oscillations. The circuit incorporates true digital shutdown for high speed response while an undervoltage lockout circuit prevents spurious outputs when the supply voltage is too low for stable operation. Full double-pulse suppression logic insures alternating output pulses when the Shutdown pin is used for pulse-by-pulse current limiting. The SG1529 is specified for operation over the full military ambient temperature range of -55°C to 125°C. The SG2529 is characterized for the industrial range of -25°C to 85°C and the SG3529 is designed for the commercial range of 0°C to 70°C.

FEATURES

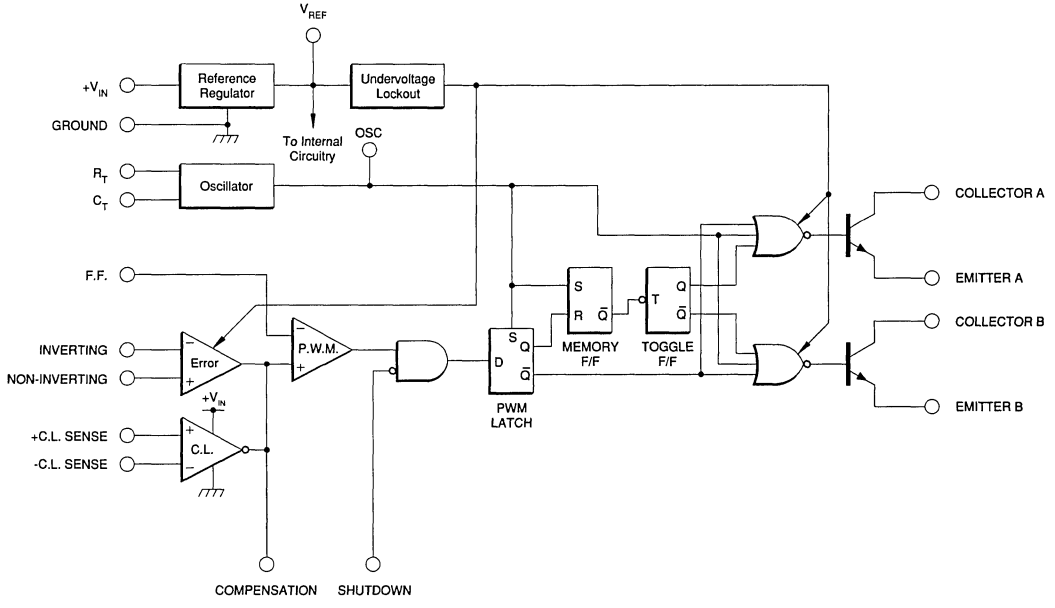
- **Feed forward capability**
- **7V to 40V operation**
- **5V reference trimmed to ±1%**
- **100Hz to 400KHz oscillator range**
- **Excellent external sync capability**
- **Dual 100mA output transistors**
- **Wide current limit common mode range**
- **DC-coupled toggle flip-flop**
- **PWM data latch**
- **Undervoltage lockout**
- **Full double-pulse suppression logic**
- **60V output collectors**

HIGH RELIABILITY FEATURES - SG1529

- **Available to MIL-STD-883**
- **SG level "S" processing available**

4

BLOCK DIAGRAM



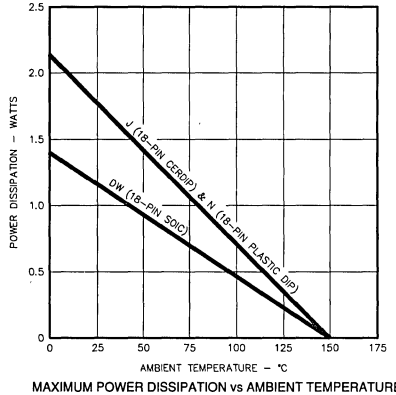
April 1990

ABSOLUTE MAXIMUM RATINGS (Note 1)

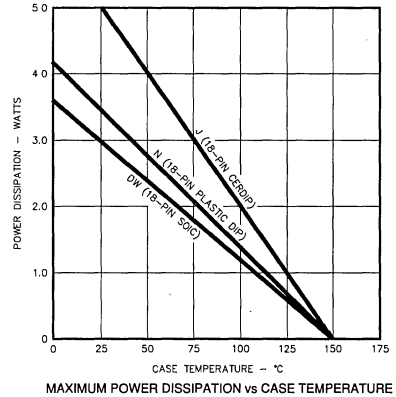
Input Voltage ($+V_{IN}$) 42V
Collector Voltage 60V
Logic Inputs ..... -0.3V to 5.5V
Current Limit Sense Inputs ..... -0.3V to V_{IN}
Output Current (each transistor) 200mA
Reference Load Current 50mA
Oscillator Charging Current 5mA
Operating Junction Temperature
Hermetic (J Package) ..... 150°C
Plastic (N, DW Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1. Values beyond which damage may occur.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Voltage ($+V_{IN}$) ..... 7V to 40V
Collector Voltage ..... 0V to 60V
Error Amp Common Mode Range ..... 2.3V to V_{REF}
Current Limit Sense Common Mode Range ..... 0V to V_{IN}-2.5V
Output Current (each transistor) ..... 0 to 100mA
Reference Load Current ..... 0 to 20mA
Oscillator Charging Current ..... 25µA to 1.8mA
Oscillator Frequency Range ..... 100Hz to 400KHz
Oscillator Timing Resistor (R_T) ..... 2KΩ to 150KΩ
Oscillator Timing Capacitor (C_T) ..... 1nF to 0.1µF
Operating Ambient Temperature Range
SG1529 ..... -55°C to 125°C
SG2529 ..... -25°C to 85°C
SG3529 ..... 0°C to 70°C

Note 2: Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1529 with $-55°C \le T_A \le 125°C$, SG2529 with $-25°C \le T_A \le 85°C$, SG3529 with $0°C \le T_A \le 70°C$, and $+V_{IN} = 20V$. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1529/2529			SG3529			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Section (Note 3)								
Output Voltage	$T_J = 25°C$	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	$V_{IN} = 7V$ to 40V		3	20		3	30	mV
Load Regulation	$I_L = 0$ to 20mA		5	30		5	50	mV
Temperature Stability (Note 7)	Over Operating Temperature Range		15	50		15	50	mV
Total Output Voltage Range	Over Line, Load and Temperature	4.90		5.10	4.80		5.20	V
Short Circuit Current	$V_{REF} = 0V$	25	50	120	25	50	120	mA
Undervoltage Lockout Section								
Threshold Voltage		4.3	4.5	4.7	4.3	4.5	4.7	V

Note 3. $I_L = 0mA$

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1529/2529			SG3529			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Oscillator Section (Note 4)								
Initial Accuracy	T_J = 25°C	42	45	48	40	45	50	KHz
Voltage Stability	V_{IN} = 7V to 40V		±0.1	±1		±0.1	±1	%
Temperature Stability (Note 7)	Over Operating Range		±1	±2		±1	±2	%
Minimum Frequency	R_T = 150KΩ, C_T = 0.1μF		50	140		50	120	Hz
Maximum Frequency	R_T = 2KΩ, C_T = 470pF	400	600		400	600		KHz
Sawtooth Peak Voltage	V_{IN} = 40V		3.5	3.9		3.5	3.9	V
Sawtooth Valley Voltage	V_{IN} = 7V	0.6	1		0.6	1		V
Clock Amplitude		3.0	4.0		3.0	4.0		V
Clock Pulse Width		0.2	0.5	1.2	0.2	0.5	1.2	μs
Error Amplifier Section (Note 5)								
Input Offset Voltage	$R_S \leq$ 2KΩ		0.5	5		2	10	mV
Input Bias Current			1	5		1	10	μA
Input Offset Current				1			1	μA
DC Open Loop Gain	$R_L \geq$ 10MΩ	60	78		60	78		dB
Output Low Level	I_{SINK} = 100μA; $V_{PIN\,1} - V_{PIN\,2} \geq$ 150mV		0.2	0.5		0.2	0.5	V
Output High Level	I_{SOURCE} = 100μA; $V_{PIN\,2} - V_{PIN\,1} \geq$ 150mV	3.8	4.2		3.8	4.2		V
Common Mode Rejection	V_{CM} = 2.3V to V_{REF}	70	90		70	90		dB
Supply Voltage Rejection	V_{IN} = 7V to 40V	76	100		76	100		dB
Gain-Bandwidth Product (Note 7)	T_J = 25°C	1	2		1	2		MHz
P.W.M. Comparator (Note 4)								
Minimum Duty Cycle	V_{COMP} = 0.5V (Note 8)			0			0	%
Maximum Duty Cycle	V_{COMP} = 3.9V (Note 8)	45	49		45	49		%
Input Bias Current	V_{FF} = 0.5V to 3.9V			2			2	μA
Current Limit Amplifier Section (Note 6)								
Sense Voltage		180	200	220	170	200	230	mV
Input Bias Current			-3	-10		-3	-10	μA
Shutdown Input Section (Note 6)								
HIGH Input Voltage		2.0			2.0			V
HIGH Input Current	$V_{SHUTDOWN}$ = 5.0V		0.1	1		0.1	1	mA
LOW Input Voltage				0.6			0.6	V
Output Section (each transistor)								
Collector Leakage Current	V_{CE} = 60V			50			50	μA
Collector Saturation Voltage	I_C = 10mA		0.2	0.4		0.2	0.4	V
	I_C = 100mA		1.0	2.0		1.0	2.0	V
Emitter Output Voltage	I_E = 10mA	17.5	19		17.5	19		V
	I_E = 100mA	17	18		17	18		V
Emitter Voltage Rise Time (Note 7)	R_E = 2KΩ, T_A = 25°C		0.2	0.5		0.2	0.5	μs
Collector Voltage Fall Time	R_C = 2KΩ, T_A = 25°C		0.1	0.2		0.1	0.2	μs
Power Consumption								
Standby Current	V_{IN} = 40V, $V_{SHUTDOWN}$ = 2.0V		5	12		5	12	mA

Note 4. F_{OSC} = 43KHz (R_T = 2700Ω, C_T = .01μF)
Note 5. V_{CM} = 2.3V to V_{REF}
Note 6. V_{CM} = 0V to 17.5V
Note 7. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
Note 8. C_T connected to FF.

4

APPLICATION CIRCUITS

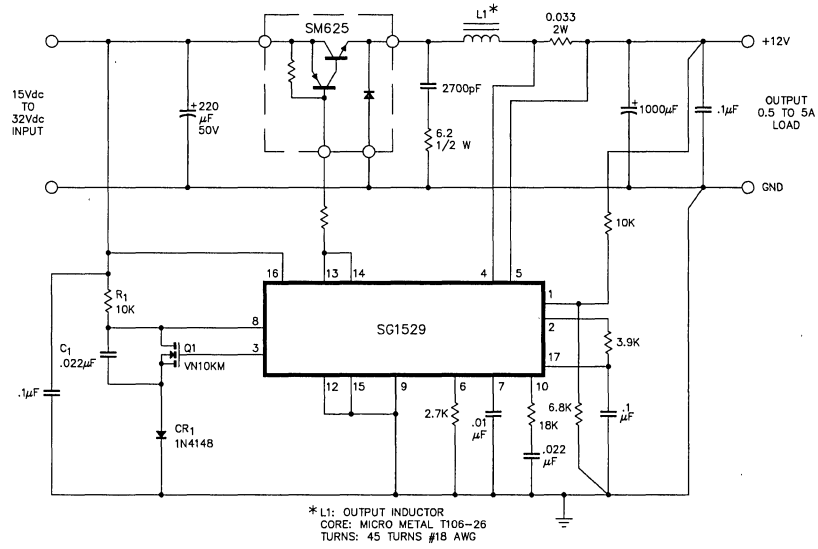
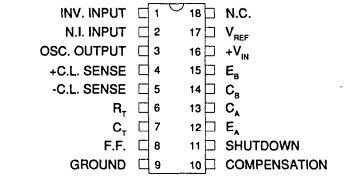
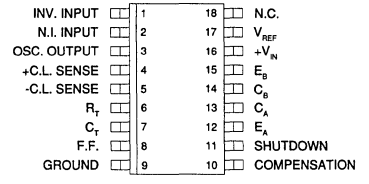


FIGURE 1 - 60V STEP DOWN BUCK CONVERTER

The above schematic describes a 60W step down (Buck) converter where feed forward feature is obtained by generating a ramp with external components R1, C1 and Q1. The slope of the ramp changes with the change in input voltage, which causes the duty cycle to adjust much faster than the conventional fixed slope ramp method resulting in a better line transient response. Rectifier CR1 is used to offset the ramp.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
18-PIN CERAMIC DIP J - PACKAGE	SG1529J/883B SG1529J SG2529J SG3529J	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
18-PIN PLASTIC DIP N - PACKAGE	SG2529N SG3529N	-25°C to 85°C 0°C to 70°C	
18-PIN WIDE BODY PLASTIC S.O.I.C. DW - PACKAGE	SG2529DW SG3529DW	-25°C to 85°C 0°C to 70°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

PRECISION GENERAL-PURPOSE REGULATOR

DESCRIPTION

This monolithic integrated circuit is a versatile, general-purpose voltage regulator designed as a substantially improved replacement for the popular SG723 device. The SG1532 series regulators retain all the versatility of the SG723 but have the added benefits of operation with input voltages as low as 4.5 volts and as high as 50 volts; a low noise, low voltage reference; temperature compensated, low threshold current limiting; and protective circuits which include thermal shutdown and independent current limiting of both the reference and output voltages. A separate remote shutdown terminal is included. In the dual-in-line package an open collector output is available for low input-output differential applications.

These devices are available in both hermetic 14-pin cerdip and 10-pin TO-96 packages. In the T-package, these units are interchangeable with the LAS-1000 and LAS-1100 regulators. The SG1532 is rated for operation over the ambient temperature range of -55°C to 125°C while the SG2532 and SG3532 are intended for industrial applications of 0°C to 70°C.

FEATURES

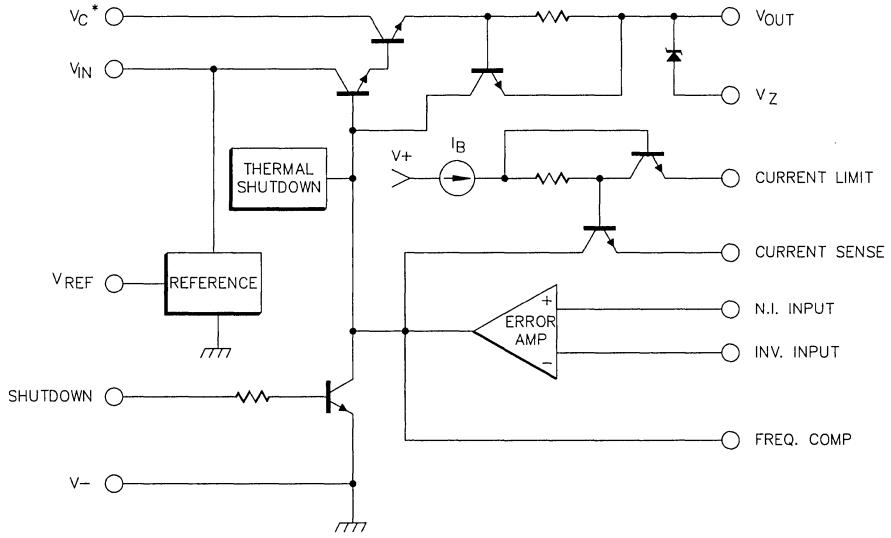
- **Input voltage range of 4.5V to 50V**
- **2.5V low noise reference**
- **Independent shutdown terminal**
- **Improved line and load regulation**
- **80mV current limit sense voltage**
- **Fully protected including thermal shutdown**
- **Useful output current to 150mA**

HIGH RELIABILITY FEATURES -SG1532

- **Available to MIL-STD-883**
- **SG level "S" processing available**

4

BLOCK DIAGRAM



* V_C IS INTERNALLY CONNECTED TO V_{IN} FOR T PACKAGE

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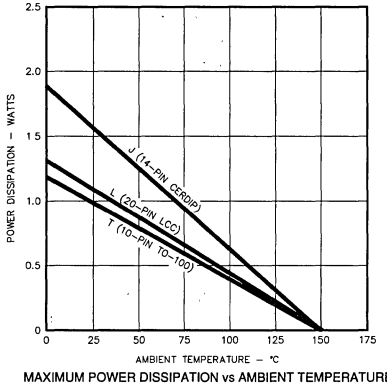
ABSOLUTE MAXIMUM RATINGS (Note 1)

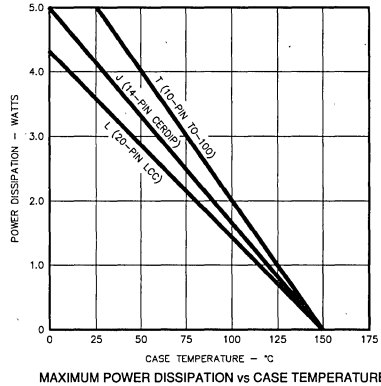
Pulse (50 ms) Input Voltage from V_{IN} to V- 50V
Continuous Input Voltage from V_{IN} to V- 40V
Input to Output Voltage Differential 40V
Maximum Output Current 250mA
Current from V_Z (J, L-Package only) 100mA
Current from V_{REF} 25mA
Operating Junction Temperature
Hermetic (T, J, L-Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Voltage Range
SG1532/SG2532 ..... 5V to 45V
SG3532 ..... 5V to 36V
Output Current Range ..... 1mA to 100mA
Reference Current 5mA
Zener Current (J & L-Packages only) 20mA
Operating Ambient Temperature Range
SG1532 ..... -55°C to 125°C
SG2532/SG3532 ..... 0°C to 70°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1532 with $-55°C \le T_A \le 125°C$, SG2532 with $0°C \le T_A \le 70°C$, SG3532 with $0°C \le T_A \le 70°C$, $V_{IN} = 10V$, $V_{OUT} = 5V$, and $I_{OUT} = 1mA$. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1532/SG2532			SG3532			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Voltage Range	$T_A = 25°C$	4.5		50	4.5		40	V
		4.7		50	4.7		40	V
Output Voltage Range		2.0		38	2.0		38	V
Max Output Current	$R_{SC} = 0$, $V_{OUT} = 0$, $T_A = 25°C$		175	250		175	250	mA
Min (V_{IN} - V_{OUT})	$I_{OUT} = 100mA$, $T_A = 25°C$		1.7	2.0		1.7	2.0	V
Reference Voltage	$T_A = 25°C$	2.40	2.50	2.60	2.40	2.50	2.60	V
		2.35		2.65	2.35		2.65	V
Temperature Stability (Note 4)			0.005	0.015		0.005	0.015	%/°C
Ref Short Circuit Current	$V_{REF} = 0$, $T_A = 25°C$		15	25		15	25	mA
Line Regulation (Note 3)	$8V \le V_{IN} \le 40V$		0.005	0.01		0.005	0.02	%/V
	$8V \le V_{IN} \le 20V$, $I_{OUT} = 25mA$		0.01	0.02		0.01	0.03	%/V
Load Regulation (Note 3)	$1mA \le I_{OUT} \le 25mA$		0.002	0.004		0.002	0.004	%/mA
	$1mA \le I_{OUT} \le 100mA$		0.002	0.005		0.002	0.005	%/mA
Current Limit Sense Voltage	$R_{SC} = 100\Omega$, $V_{OUT} = 0V$	0.06	0.08	0.10	0.06	0.08	0.10	V
Shutdown Voltage Threshold		0.40	0.70	1.0	0.40	0.70	1.0	V
Shutdown Source Current	V_{OUT} = high	100	200	300	100	200	300	µA
Zener Voltage	$I_{OUT} = 10mA$, (J and L-Packages only)	6.0	6.4	7.2	6.0	6.4	7.2	V
Standby Current	$V_{IN} = 40V$		2.5	3.5		2.5	3.5	mA
Error Amplifier Offset Voltage			2.0	10		2.0	15	mV
Error Amplifier Input Bias Current			4.0	15		4.0	20	µA

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1532/SG2532			SG3532			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Open Loop Gain	T_A = 25°C	66	68		60	68		dB
Ripple Rejection	f = 120Hz, T_A = 25°C		66			66		dB
Output Noise	10Hz ≤ f ≤ 100KHz, T_A = 25°C		50			50		μV_{RMS}
Long Term Stability (Note 4)	V_{IN} = 30V, T_A = 125°C		0.3	1.0		0.3	1.0	%/Khr
Thermal Shutdown			175			175		°C

Note 3. Applies for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.
Note 4. These parameters, although guaranteed, are not tested in production.

CHARACTERISTIC CURVES

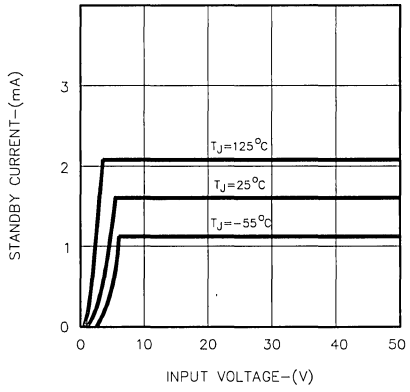


FIGURE 1.
STANDBY CURRENT

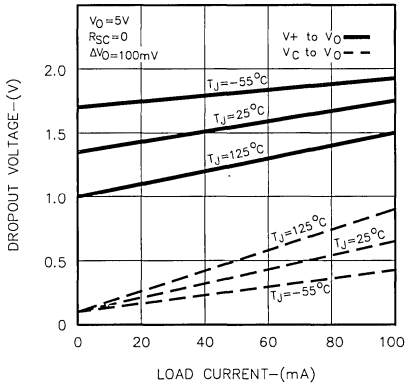


FIGURE 2.
MINIMUM INPUT-OUTPUT VOLTAGE

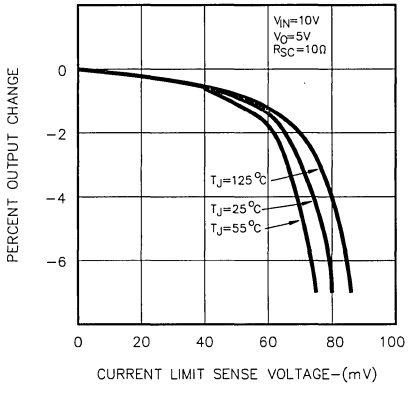


FIGURE 3.
CURRENT LIMITING

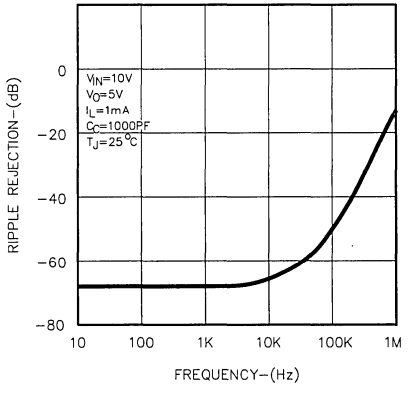


FIGURE 4.
RIPPLE REJECTION

CHARACTERISTIC CURVES (continued)

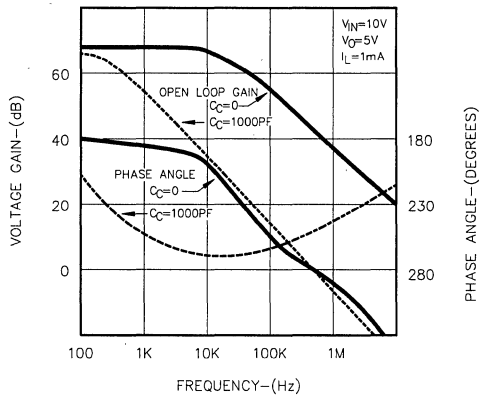


FIGURE 5.
FREQUENCY RESPONSE

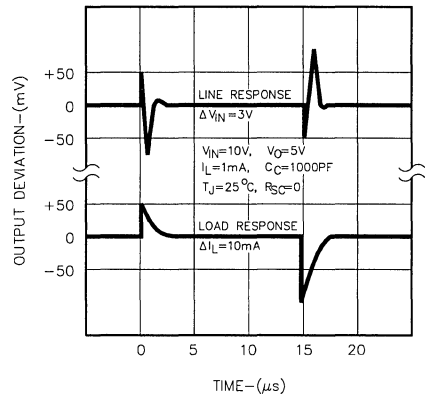


FIGURE 6.
TRANSIENT RESPONSE

APPLICATION INFORMATION

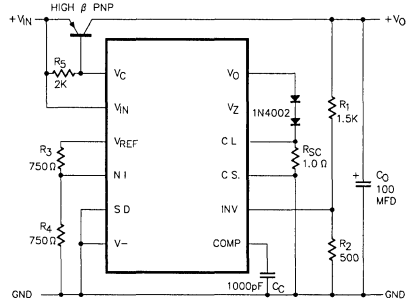


FIGURE 7 - 90% EFFICIENT LINEAR REGULATOR

Output Voltage = 5V
Min (V_{IN}-V_{OUT}) at 2A = 0.4V
Load Reg 0-2A = 20mV

Max Output Current = 3A
Line Reg 6-30V = 10 mV

Notes:

For output voltages above 8V and load currents which allow PNP base current to be limited to 25mA, the internal zener may be used, eliminating the need for the two external diodes and the divider on V_{REF}.

R_{SC} can be eliminated if the 200mA current limit on V_{OUT} is adequate. Overall current limiting is dependent upon PNP Beta. For greater accuracy, load currrent may be sensed in the ground line.

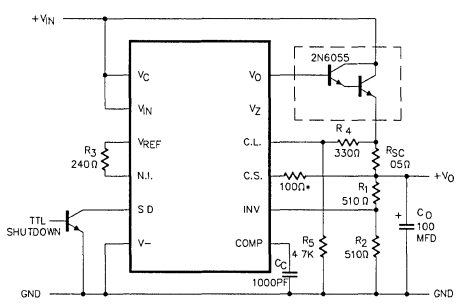


FIGURE 8 - HIGH CURRENT REGULATOR WITH FOLDBACK CURRENT LIMITING AND REMOTE SHUTDOWN

Output Voltage = 5V
Max Output Current = 8A
Min V_{IN} at No Load = 6.9V
Min V_{IN} at 5A = 8.2V

Line Reg 10-30V = 3mV
Load Reg 0-5A = 17mV
Short Circuit Current = 1.8A

Note:

* 100Ω surge limiting resistor should be used for output voltages above 8V.

APPLICATION INFORMATION

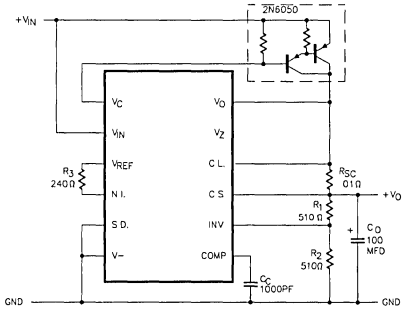


FIGURE 9 - HIGH EFFICIENCY LOW VOLTAGE REGULATOR

Output Voltage = 5V
Max Output Current = 9A
Min V_{IN} at 5A = 7.0V

Line Reg 7-20V = 10mV
Load Reg 0-5A = 25mV
Constant Current Limiting

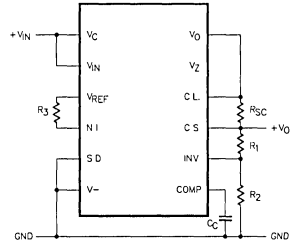


FIGURE 10 - BASIC LOW CURRENT REGULATOR

$V_{OUT} = V_{REF}\left(1 + \frac{R_1}{R_2}\right)$

$I_{SC} = \frac{\text{Sense Voltage}}{R_{SC}}$

$C_C = 1000\ pF$

$I_{OUT} \leq 100mA$

$R_3 = \frac{R_1 R_2}{R_1 + R_2}$

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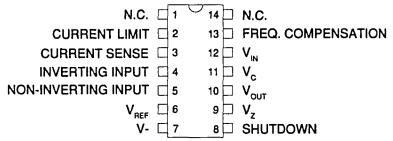
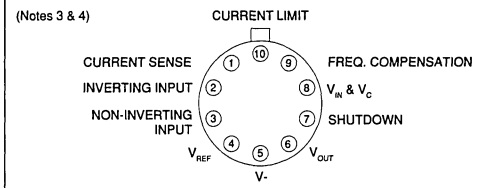
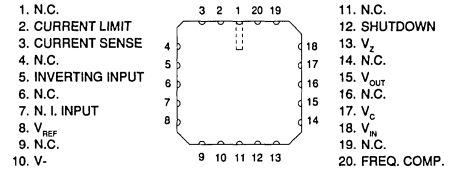
CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN CERAMIC DIP J - PACKAGE	SG1532J/883B SG1532J SG2532J SG3532J	-55°C to 125°C -55°C to 125°C 0°C to 70°C 0°C to 70°C	
10-PIN METAL CAN T - PACKAGE	SG1532T/883B SG1532T SG2532T SG3532T	-55°C to 125°C -55°C to 125°C 0°C to 70°C 0°C to 70°C	
20-PIN CERAMIC LEADLESS CHIP CARRIER L- PACKAGE	SG1532L/883B SG1532L	-55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

Note 3. V_Z output is not available in T-package.
4. Pin 5 is connected to case.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

OFF-LINE START-UP CONTROLLER

DESCRIPTION

The SG1540 is an integrated circuit designed to efficiently provide start-up power from a high-voltage DC bus to a PWM control circuit in a switching power supply. When used on the primary side, it reduces start-up current to less than 1mA and allows any standard PWM control circuit to be used as a primary-side controller. When used to power a controller on the secondary side, it efficiently eliminates the need for a heavy 50/60Hz line transformer with its associated low frequency magnetic fields.

The circuit consists of three sections: a micropower bandgap comparator/power switch referenced to 2.5 volts which isolates the start-up capacitor from its load; a high frequency square-wave oscillator with 200mA totem-pole output for driving an isolation transformer; and a second bandgap comparator with latching crowbar to protect against overvoltage faults while starting or running.

The SG1540 is specified for operation over the full military ambient temperature range of -55°C to 125°C. The SG2540 is characterized for the industrial range of -25°C to 85°C, and the SG3540 is designed for the commercial range of 0°C to 70°C.

FEATURES

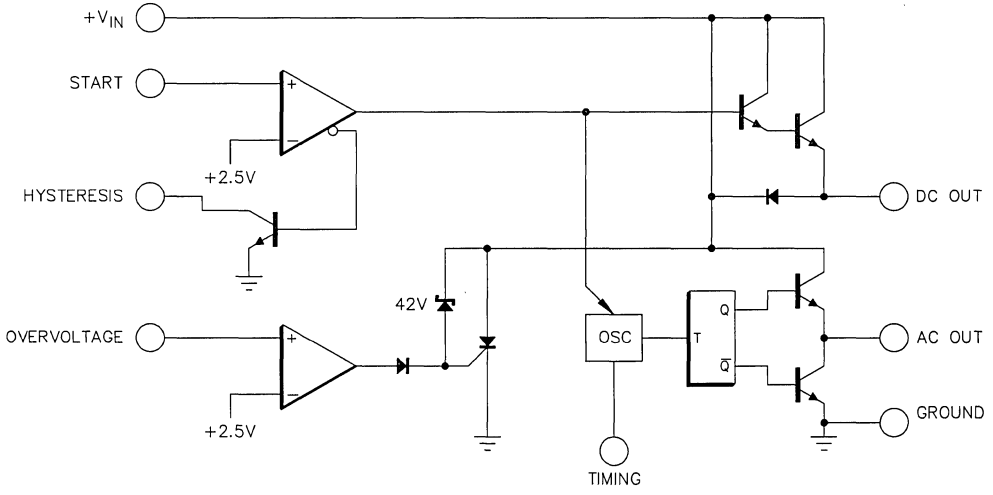
- **Useable with primary and secondary side PWM controllers**
- **Micropower comparator / switch**
  - **Internal 2.5V bandgap reference**
  - **50mA power switch**
- **Squarewave oscillator**
  - **500Hz to 200KHz operation**
  - **200mA totem pole outputs**
- **Eliminates bulky, expensive 50/60 Hz transformer**
- **Minimizes high voltage bleeder current**
- **Programmable start-up voltage and hysteresis**
- **Internal and programmable overvoltage crowbar latch**
- **Available in 8 pin DIP, 10 pin flat pack, and 16 pin widebody SOIC**

HIGH RELIABILITY FEATURES - SG1540

- **Available to MIL-STD - 883**
- **SG level "S" processing available**

4

BLOCK DIAGRAM



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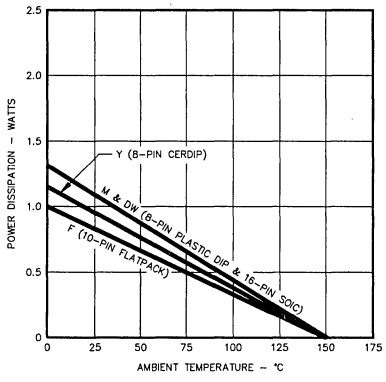
See Application Notes for additional information.

ABSOLUTE MAXIMUM RATINGS (Note 1)

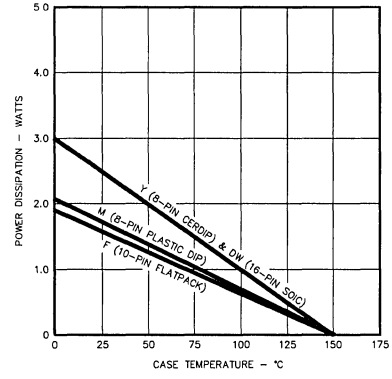
Supply Voltage ($+V_{IN}$) ..... +37V
DC Output Current, Continuous (V_{OUT}) 100mA
AC Output Current, Continuous 200mA
Analog Inputs (Start and Overvoltage) ..... -0.3V to 6.0V
Analog Input Currents (V>8V) 10mA
Overvoltage Crowbar Current, Continuous 50mA
Overvoltage Crowbar Energy (½CV²) 8mJ
Operating Junction Temperature
Hermetic (Y Package) ..... 150°C
Plastic (M, DW Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Values beyond which damage may occur.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage Range ..... 7V to 35V
DC Output Current, Continuous ..... 0 to 50mA
AC Output Current, Continuous ..... 0 to 100 mA
Oscillator Frequency Range ..... 1KHz to 400KHz
Timing Resistor Range ..... 2KΩ to 150KΩ
Timing Capacitor Range ..... 1nF to 20µF
Operating Ambient Temperature Range
SG1540 ..... -55°C to 125°C
SG2540 ..... -25°C to 85°C
SG3540 ..... 0°C to 70°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1540 with $-55°C \le T_A \le 125°C$, SG2540 with $-25°C \le T_A \le 85°C$, SG3540 with $0°C \le T_A \le 70°C$, and $+V_{IN} = 15V$. A 0.1µF high frequency bypass capacitor is recommended on V_{IN}. Low duty cycle testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1540/2540/3540 Min.	Typ.	Max.	Units
Start-up Section					
Start Current I_{CC}	V_{START} = 0 to 2.37V		0.2	0.4	mA
Operating Current	$V_{TIMING} = +V_{IN}$; V_{OUT} Open		0.3	0.6	mA
	F_{OSC} = 50KHz, V_{OUT} and AC $_{OUT}$ Open		3	6	mA
Start Threshold		2.37	2.50	2.63	V
Start Bias Current	$V_{PIN\,1}$ = 0 to 5V		0.1	1	µA
Start Clamp Voltage	$I_{PIN\,1}$ = 1mA	6	7	8	V
Hysteresis ON Voltage	$I_{PIN\,4}$ = 100µA		0.1	0.2	V
DC Output Section					
V_{OUT} Voltage	I_{SOURCE} = 10mA	12.5	13.5		V
	I_{SOURCE} = 50mA	12.0	13.0		V
Short Circuit Current	V_{OUT} = 0V	50	100	225	mA

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1540/2540/3540 Min.	Typ.	Max.	Units
Oscillator Section (Note 3)					
Initial Accuracy	T_J = 25°C	46	50	54	KHz
Voltage Stability	$+V_{IN}$ = 12 to 18V		5	12	%
Temperature Stability (Note 4)			2	5	%
Oscillator Minimum Frequency	R_T = 17.8K, C_T = .068µF			1	KHz
Oscillator Maximum Frequency	R_T = 1.5K, C_T = 470pF	400			KHz
AC Output Section					
HIGH Output Voltage	I_{SOURCE} = 20mA	12.5	13.5		V
	I_{SOURCE} = 100mA	12.0	13.0		V
LOW Output Voltage	I_{SINK} = 20mA		0.2	0.3	V
	I_{SINK} = 100mA		1.2	2.0	V
Squarewave Duty Cycle		45	50	55	%
AC Output Risetime	C_L = 1000pF		0.3	0.6	µS
AC Output Falltime	C_L = 1000pF		0.1	0.2	µS
Overvoltage Crowbar Section					
Overvoltage Threshold		2.37	2.50	2.63	V
Overvoltage Bias Current	$V_{O.V.}$ = 0 to 2.37V		0.1	1	µA
Overvoltage Clamp Voltage	$I_{O.V.}$ = 1mA	6	7	8	V
$+V_{IN}$ Overvoltage Threshold		37	42	44	V
SCR ON Voltage	I_{VIN} = 35mA		9	12	V
SCR Holding Current	$V_{O.V.}$ = 0	0.15	0.35	0.55	mA

Note 3. F_{OSC} = 50KHz, R_T = 3.48K C_T = 4.7nF unless otherwise specified.
Note 4. These parameters, although guaranteed, are not tested in production.

CHARACTERISTIC CURVES

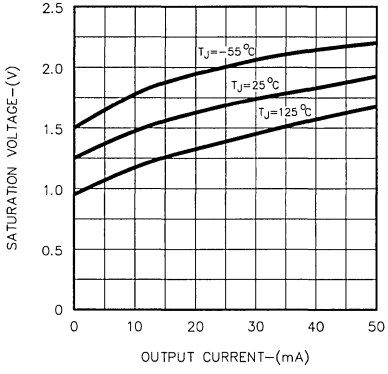


FIGURE 1 - SATURATION VOLTAGE (DC OUT PIN) VS. OUTPUT CURRENT

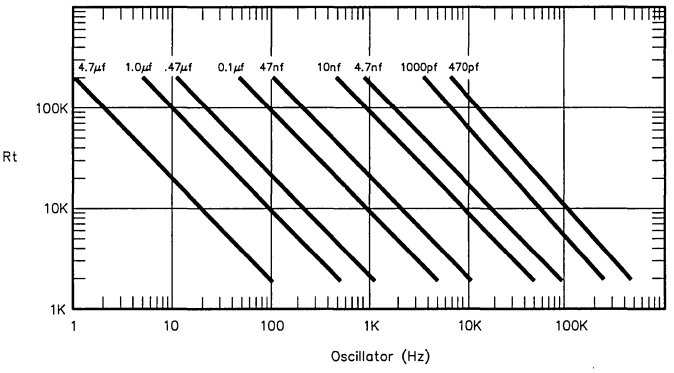


FIGURE 2 - OSCILLATOR FREQUENCY VS. R_T AND C_T

4

APPLICATION INFORMATION

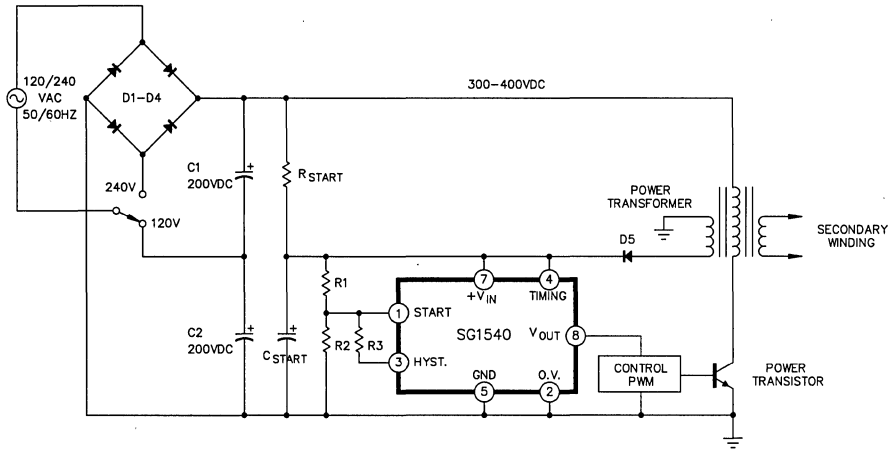


FIGURE 3 - EFFICIENT PRIMARY SIDE START-UP

PRIMARY SIDE START-UP

When the design goal is efficient start-up for a control PWM referenced to the primary side of the power transformer, the configuration in Figure 3 is recommended. An energy storage capacitor C_{START} is trickle-charged from the 300-400 Volt DC bus by resistor R_{START}. The value of R_{START} is chosen to provide a constant 1mA charging current, allowing the use of a ½ watt resistor. As the voltage on C_{START} ramps up from zero, the only load current is the standby current of the SG1540 and that of the divider network R1-R3. (Connecting the TIMING pin to $+V_{IN}$ disables the internal power oscillator and forces the circuitry into a micropower standby model. Since the input bias current at the START pin is 1µA maximum, a divider current of 100µA is adequate).

When the voltage at the START pin reaches +2.5 Volts, the hysteresis transistor turns off, overdriving the START pin. The V_{OUT} pin is switched to the HIGH state, providing power to the PWM control circuit. As energy flows out of the START capacitor, its voltage decays; but it remains connected to the PWM circuit until the dropout voltage is reached ($V_{START} - V_{HYSTERESIS}$). The bootstrap winding on the power transformer and rectifier diode D5 prevent this from happening. As the PWM control circuit becomes active, the power transistor begins to switch, providing operating current to the PWM circuit through the SG1540.

RESISTOR CALCULATIONS

Given that V_{START} and $V_{DROPOUT}$ have been chosen, and that the divider current at start-up is 100µA, then the values for R1 through R3 are calculated as follows:

1. For simplification, let $X = \frac{V_{START} - 2.5}{2.5}$ and $Y = \frac{V_{DROPOUT} - 2.5}{2.5}$

2. Then, $R1 = 2.5 \times 10^4 * X$ [1]
   $R2 = R1/Y$ [2]
   and $R3 = \frac{R1 * R2}{X * R2 - R1}$ [3]

DESIGN EXAMPLE

Suppose we have a power MOSFET device, and so want to start at +18 volts and drop out at +12 volts.

Then $X = 6.20$
and $Y = 3.80$

Therefore $R1 = 2.5 \times 10^4 * 6.2 = 155K$ (Choose 150K)
$R2 = 1.5 \times 10^5 / 3.8 = 39.5K$ (Choose 39K)

$$R3 = \frac{1.5 \times 10^5 * 3.9 \times 10^4}{6.2 * 3.9 \times 10^4 - 1.5 \times 10^5} = 63.7K$$ (Choose 62K)

APPLICATIONS INFORMATION (continued)

The voltage waveform at $+V_{IN}$ is shown in Figure 4 with these resistor values and with C_{START} = 3µF. Notice that two tries are required before the +15 volt bootstrap winding becomes active.

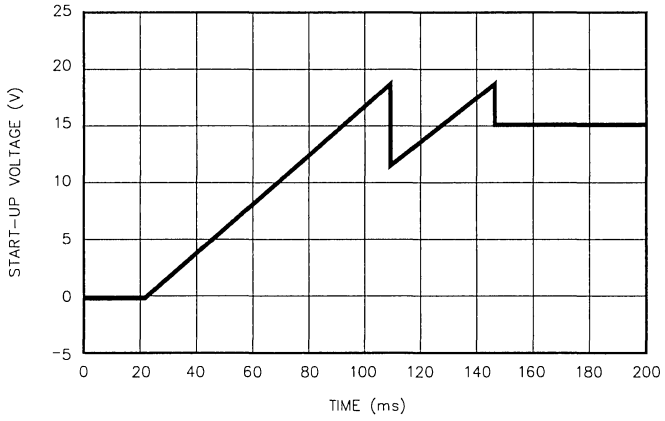


FIGURE 4 - STARTUP VOLTAGE WAVEFORM

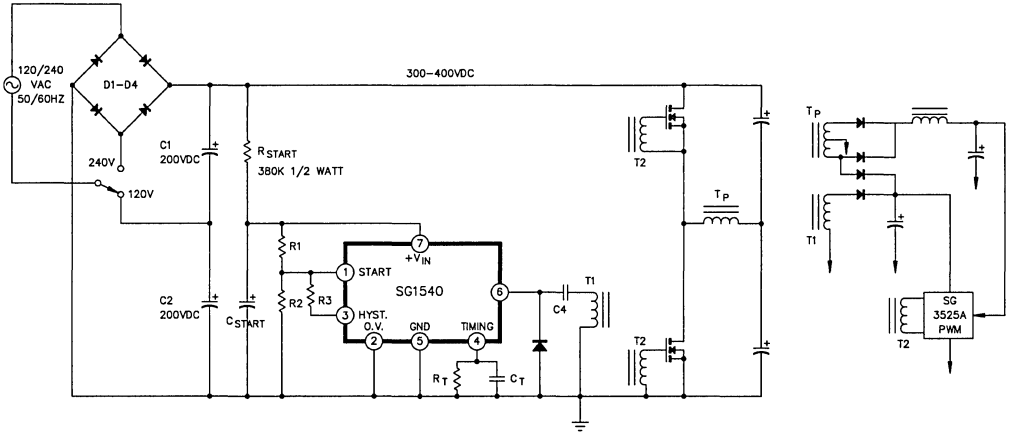
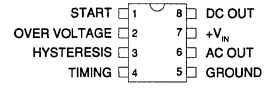
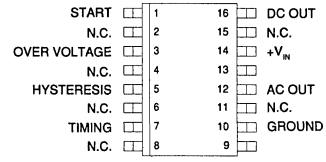
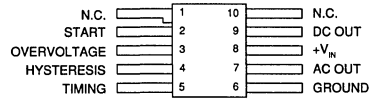


FIGURE 5 - SECONDARY-SIDE START-UP WITHOUT A LINE TRANSFORMER

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
8-PIN CERAMIC DIP Y - PACKAGE	SG1540Y/883B SG1540Y SG2540Y SG3540Y	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
8-PIN PLASTIC DIP M - PACKAGE	SG2540M SG3540M	-25°C to 85°C 0°C to 70°C	
16-PIN WIDE BODY PLASTIC S.O.I.C. DW - PACKAGE	SG2540DW SG3540DW	-25°C to 85°C 0°C to 70°C	
10-PIN HERMETIC FLAT PACK F - PACKAGE	SG1540F/883B SG1540F	-55°C to 125°C -55°C to 125°C	

Notes: 1. Contact factory for JAN and DESC part availability.
2. All parts are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

VOLTAGE SENSING CIRCUIT

DESCRIPTION

This monolithic integrated circuit provides the control functions necessary to protect sensitive electronic circuitry from over-voltage transients or the effects of voltage regulator failure. It is designed for use with an external SCR "crowbar" for immediate shutdown of the power supply, but additionally provides logic level outputs for regulator turn-off and/or operator or system out-of-tolerance indication.

This device contains an accurate, stable 2.6 volt reference which allows the sensing threshold to be set predictably without the need for potentiometers. Uncommitted availability of both polarity inputs to the sensing comparator allows a wide flexibility of use including the ability to sense voltages less than the reference voltage. An external capacitor can be used to program an accurate time delay between fault occurrence and crowbar triggering, but this delay may be bypassed by inputing at the Sense 2 terminal or by using the remote activation capability.

For additional circuit functions, see SG1543 data sheet.

FEATURES

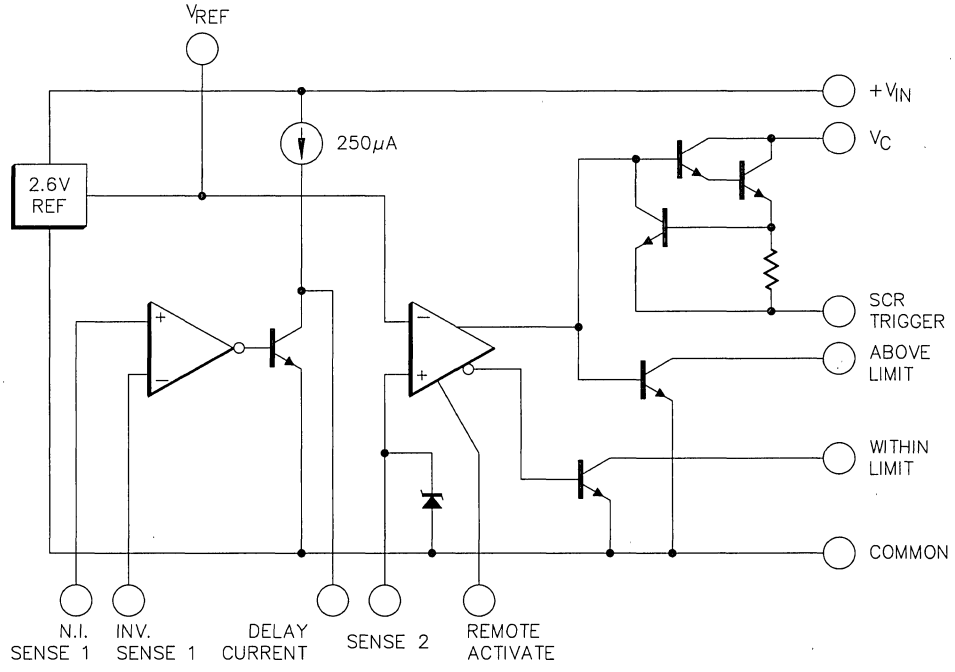
- **Operation from 4.5V to 40V**
- **Useful for either over- or under-voltage sensing**
- **Sensing threshold accurate to ±2%**
- **Built-in input hysterisis**
- **Zero to 35V sensing capability**
- **Programmable time delay**
- **SCR "Crowbar" drive of 200mA**
- **Remote activation capability**
- **2.6V 1% reference available**

HIGH RELIABILITY FEATURES -SG1542

- **Available to MIL-STD-883B**
- **SG level "S" processing available**

4

BLOCK DIAGRAM

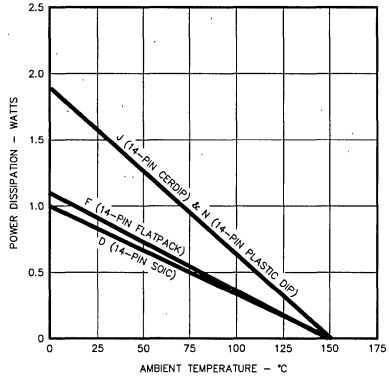


ABSOLUTE MAXIMUM RATINGS (Note 1)

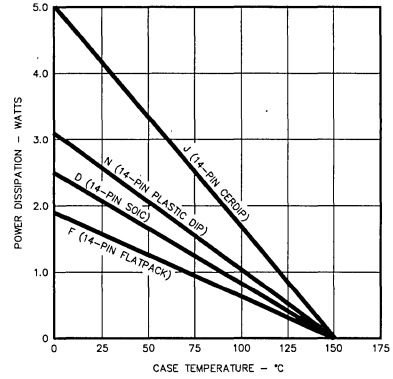
Input Supply Voltage ($+V_{IN}$) 40V
Collector Supply Voltage, V_C 40V
Sense Voltage (1) ..... $+V_{IN}$
Sense Voltage (2) 6.5V
Remote Activation Input Voltage 7.0V
SCR Trigger Current (Note 2) 300mA
Limit Indicators Output Voltage 40V
Limit Indicators Output Sink Current 50mA
Operating Junction Termperature
Hermetic (J, F Packages) ..... 150°C
Plastic (N, D Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C

Note 1. Values beyond which damage may occur.
Note 2. At higher input voltages, a dissipation limiting resistor, R_G, is required. See Figure 1.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 3)

Input Supply Voltage ($+V_{IN}$) ..... 4.7V to 40V
Sense Voltage (1)
Common Mode Input Range ..... 0V to ($+V_{IN}$) -3V
Sense Voltage (2) ..... 0 to 5.5V
Reference Load Current ..... 0 to 10mA
Indicator Output Voltage ..... 4.7V to 40V
Indicator Output Current ..... 0 to 10mA
Delay Timing Capacitor (Note 4) ..... 0 to 1µF
Operating Ambient Temperature Range
SG1542 ..... -55°C to 125°C
SG2542 ..... -25°C to 85°C
SG3542 ..... 0°C to 70°C

Note 3. Range over which the device is functional and parameter limits are guaranteed.
Note 4. Larger value capacitor may be used with peak current limiting. See Figure 5.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1542 with $-55°C \le T_A \le 125°C$, SG2542 with $-25°C \le T_A \le 85°C$, SG3542 with $0°C \le T_A \le 70°C$, and $+V_{IN}$ = 10V. Low duty cycle testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1542/2542			SG3542			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Section								
Input Voltage Range	T_J = 25°C to T_{MAX}	4.5		40	4.5		40	V
	T_{MIN} to T_{MAX}	4.7		40	4.7		40	V
Supply Current	$+V_{IN}$ = 40V, Outputs open		5	7		5	10	mA
Reference Section								
Reference Voltage	T_J = 25°C	2.58	2.60	2.62	2.55	2.60	2.65	V
	Over Operating Temperature Range	2.55		2.65	2.50		2.70	V
Line Regulation	$+V_{IN}$ = 5 to 40V		1	5		1	5	mV
Load Regulation	I_{REF} = 0 to 10mA		1	15		1	15	mV
Short Circuit Current	V_{REF} = 0V		15	40		15	40	mA
Temperature Stability			0.005			0.005		%/°C

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1542/2542			SG3542			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Comparator Section								
Sense 1 Offset Voltage	SENSE 1 (+) rising, SENSE 1 INV. = 2.6V	-20	0	20	-20	0	20	mV
Input Hysteresis			25			25		mV
Sense 1 Common Mode		0		(V_{IN})-3	0		(V_{IN})-3	V
Sense 1 Bias Current			-0.3	-1.5		-0.3	-1.5	µA
Sense 2 Threshold		2.50	2.60	2.70	2.50	2.60	2.70	V
Sense 2 Bias Current			1.0	10		1.0	10	µA
Delay Current		200	250	350	200	250	350	µA
Limit Indicators V_{SAT}	I_L = 10mA		0.2	0.5		0.2	0.5	V
Limit Indicators Leakage	V_{IND} = 40V		0.01	1.0		0.01	1.0	µA
Propagation Delay	T_O Ind., T_J = 25°C		500			500		ns
	T_O Trigger, T_J = 25°C		500			500		ns
SCR Trigger Section								
Remote Activation Current			120	220		120	220	µA
Remote Activation Threshold		0.8	1.0	2.0	0.8	1.0	2.0	V
Peak Output Current	V_C = 5V, R_G = 0, V_O = 0	100	200	600	100	200	600	mA
Peak Output Voltage	I_O = 100mA	V_{IN}-2.5	V_{IN}-1.6		V_{IN}-2.5	V_{IN}-1.6		V
Output Off Voltage	+V_{IN} = 40V, R_L = 1KΩ			0.1			0.1	V
Output Current Rise Time	R_L = 50Ω, T_J = 25°C		400			400		mA/µs

CHARACTERISTIC CURVES

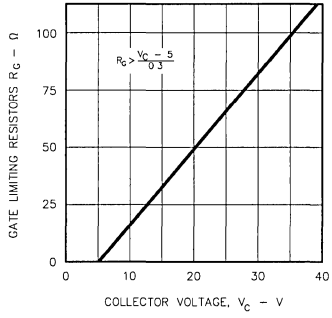


FIGURE 1 - MINIMUM GATE CURRENT LIMITING RESISTANCE

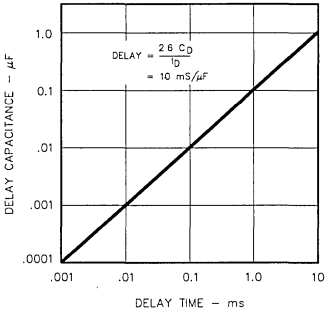
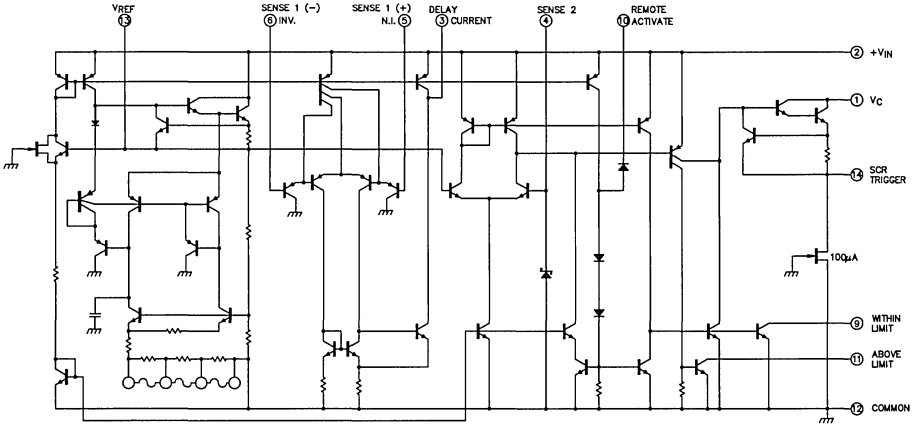


FIGURE 2 - ACTIVATION DELAY VS. CAPACITOR VALUE

SIMPLIFIED SCHEMATIC DIAGRAM - FIGURE 3



APPLICATION INFORMATION (continued)

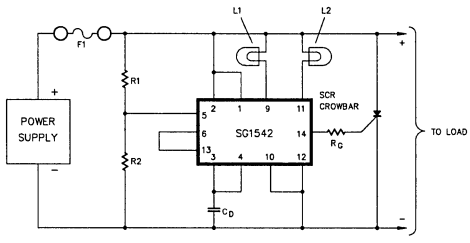


FIGURE 4 - BASIC OVER-VOLTAGE PROTECTION CIRCUIT CONFIGURATION

F_1 = Only necessary if power supply is not current limited

$V_{TRIP} = \left[\frac{2.6V\ (R_1 + R_2)}{R_2}\right]$, $R_2 \leq 100k\Omega$

$t_D = 10^4\ C_D$

$R_G > \frac{V_C - 5}{0.3}$

L_1, L_2 = Indicator selected for max. current ≈ 10mA @ V_{TRIP}

SCR = Selected for max. peak current capability

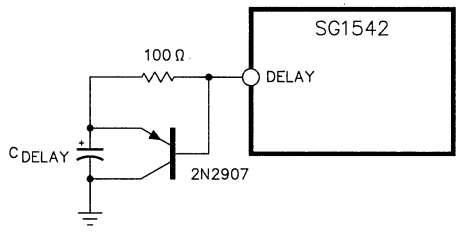


FIGURE 5 - SURGE LIMIT CIRCUIT FOR LARGE DELAY CAPACITORS

The 100 ohm resistor limits the peak discharge current into the SG1542 while the external PNP transistor provides a high peak-current discharge path for the delay capacitor.

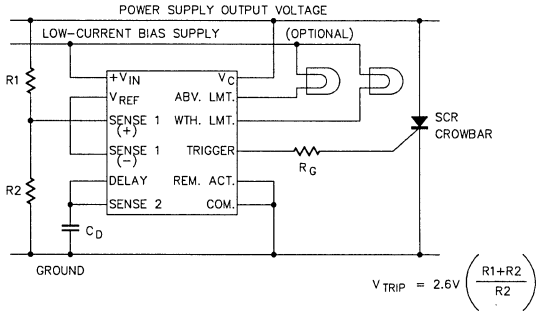


FIGURE 6 - OVER-VOLTAGE SENSING FOR VOLTAGES ABOVE 2.6 VOLTS

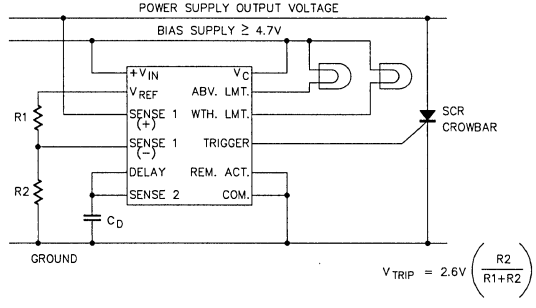


FIGURE 7 - OVER-VOLTAGE SENSING FOR VOLTAGES LESS THAN 2.6 VOLTS

APPLICATION INFORMATION (continued)

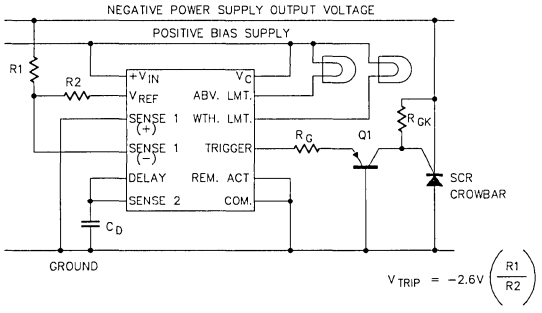


FIGURE 8 - OVER-VOLTAGE SENSING FOR NEGATIVE OUTPUT VOLTAGES *

* Without a positive bias supply, the basic OVP circuit on page 3 can be used equally well with either positive or negative voltages.

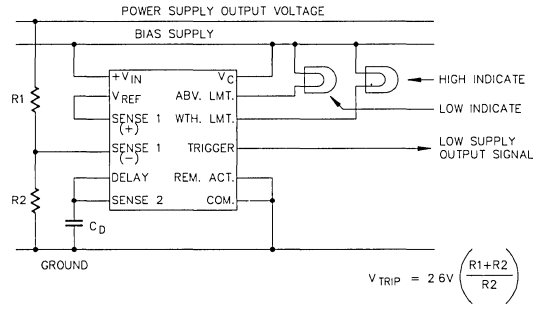


FIGURE 9 - UNDER-VOLTAGE SENSING

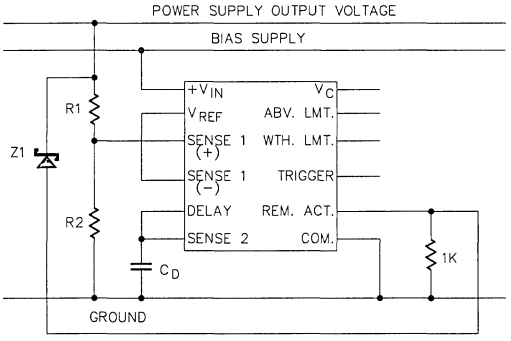


FIGURE 10 - DELAYED THRESHOLD SENSE PLUS IMMEDIATE TRIP FOR HIGH OVER-VOLTAGE

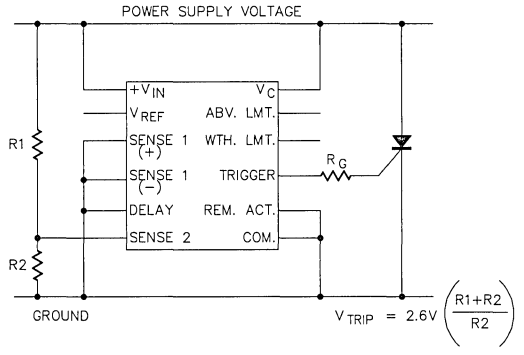


FIGURE 11 - OVER-VOLTAGE SENSING WITH MINIMUM TIME DELAY

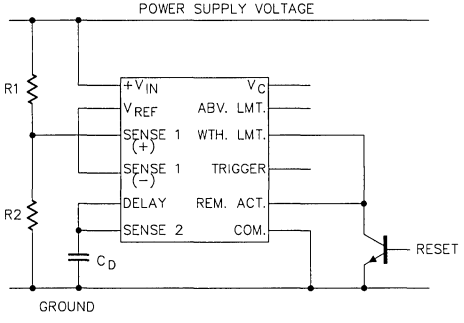


FIGURE 12 - OVER-VOLTAGE LATCH WITH RESET

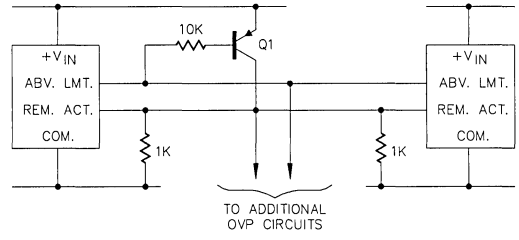
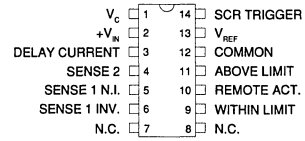
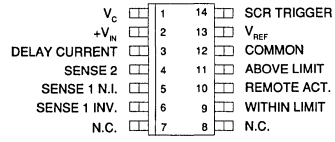
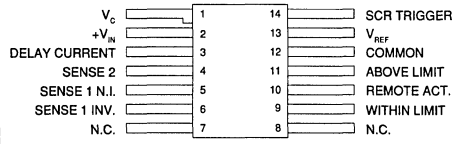


FIGURE 13 - INTERCONNECTING MULTIPLE SG1542's

Q1 must provide >2mA for each OVP circuit. With this arrangement, activation of any circuit will activate all. For a master-slave relationship, the WITHIN LIMIT terminal of the master may be directly connected to the REMOTE ACTIVATE terminals of all the slaves.

4

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN CERAMIC DIP J - PACKAGE	SG1542J/883B SG1542J SG2542J SG3542J	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
14-PIN PLASTIC DIP N - PACKAGE	SG2542N SG3542N	-25°C to 85°C 0°C to 70°C	
14-PIN PLASTIC S.O.I.C. D - PACKAGE	SG2542D SG3542D	-25°C to 85°C 0°C to 70°C	
14-PIN CERAMIC FLATPACK F - PACKAGE (Note 3)	SG1542F/883B SG1542F	-55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.
3. Contact factory for product availability.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

POWER SUPPLY OUTPUT SUPERVISORY CIRCUIT

DESCRIPTION

This monolithic integrated circuit contains all the functions necessary to monitor and control the output of a sophisticated power supply system. Over-voltage (O.V.) sensing with provision to trigger an external SCR "crowbar" shutdown; an under-voltage (U.V.) circuit which can be used to monitor either the output or to sample the input line voltage; and a third op amp/comparator usable for current sensing (C.L.) are all included in this IC, together with an independent, accurate reference generator.

Both over and under-voltage sensing circuits can be externally programmed for minimum time duration of fault before triggering. All functions contain open collector outputs which can be used independently or wire-ORed together; and although the SCR trigger is directly connected only to the over-voltage sensing circuit, it may be optionally activated by any of the other outputs, or from an external signal. The O.V. circuit also includes an optional latch and external reset capability.

The current sense circuit may be used with external compensation as a linear amplifier or as a high gain comparator. Although nominally set for zero input offset, a fixed threshold may be added with an external resistor. Instead of current limiting, this circuit may also be used as an additional voltage monitor.

The reference generator circuit is internally trimmed to eliminate the need for external potentiometers and the entire circuit may be powered directly from either the output being monitored or from a separate bias voltage.

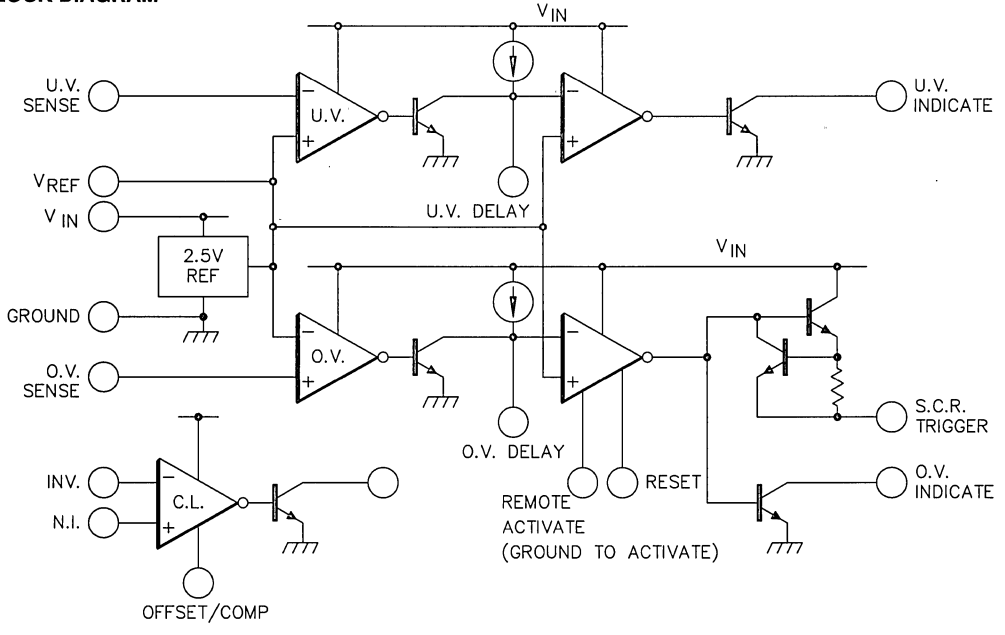
FEATURES

- **Over-voltage, under-voltage, and current sensing circuits all included**
- **Reference voltage trimmed to 1% accuracy**
- **SCR "Crowbar" drive of 300mA**
- **Programmable time delays**
- **Open-collector outputs and remote activation capability**
- **Total standby current less than 10mA**

HIGH RELIABILITY FEATURES - SG1543

- **Available to MIL-STD-883 and DESC SMD**
- **SG level "S" processing available**

BLOCK DIAGRAM



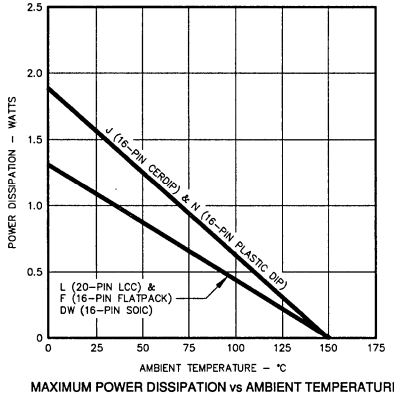
See Application Notes for additional information.

ABSOLUTE MAXIMUM RATINGS (Note 1)

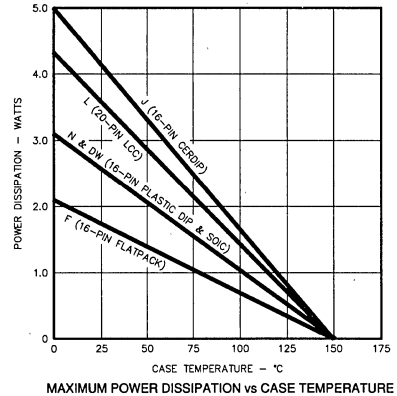
Input Supply Voltage ($+V_{IN}$) 40V
Sense Inputs ..... $+V_{IN}$
SCR Trigger Current (Note 2) 300mA
Indicator Output Voltage 40V
Indicator Output Sink Current 50mA
Operating Junction Temperature
Hermetic (J, F, L Packages) ..... 150°C
Plastic (N, DW Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C

Note 1. Values beyond which damage may occur.
Note 2. At higher input voltages, a dissipation limiting resistor, R_G, is required. See Figure 1.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 3)

Input Supply Voltage ($+V_{IN}$) ..... 4.7V to 40V
Current Limit Common Mode
Input Voltage Range ..... 0V to $+V_{IN}$ -3V
Reference Load Current ..... 0 to 10mA
Indicator Output Voltage ..... 4.7V to 40V
Indicator Output Current ..... 0 to 10mA
Delay Timing Capcitor (Note 4) ..... 0 to 1µF
Operating Ambient Temperature Range
SG1543 ..... -55°C to 125°C
SG2543 ..... -25°C to 85°C
SG3543 ..... 0°C to 70°C

Note 3: Range over which the device is functional.
Note 4. Larger value capacitor may be used with peak current limiting. See Figure 7.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1543 with -55°C ≤ T_A ≤ 125°C, SG2543 with -25°C ≤ T_A ≤ 85°C, SG3543 with 0°C ≤ T_A ≤ 70°C, and $+V_{IN}$ = 10V. Indicator outputs have 2KΩ pull-up resistor. Low duty cycle testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1543/2543			SG3543			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Section								
Input Voltage Range	T_J = 25°C to T_{MAX}	4.5		40	4.5		40	V
		4.7		40	4.7		40	V
Supply Current	$+V_{IN}$ = 40V, Outputs open, T_J = 25°C		7	10		7	10	mA
Reference Section								
Output Voltage	T_J = 25°C	2.48	2.50	2.52	2.45	2.50	2.55	V
		2.45		2.55	2.40		2.60	V
Line Regulation	$+V_{IN}$ = 5 to 30V		1	5		1	5	mV
Load Regulation	I_{REF} = 0 to 10mA		1	10		1	10	mV
Short Circuit Current	V_{REF} = 0V	12	25	40	12	25	40	mA
Temperature Stability			.005			.005		%/°C

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1543/2543			SG3543			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Comparator Section								
Input Threshold (Note 5)	T_J = 25°C	2.45	2.50	2.55	2.40	2.50	2.60	V
		2.40		2.60	2.35		2.65	V
Input Hysteresis			25			25		mV
Input Bias Current	Sense input = 0V		0.3	1.0		0.3	1.0	µA
Delay Saturation			0.2	0.5		0.2	0.5	V
Delay High Level			6	8		6	8	V
Delay Charging Current	V_D = 0V	200	250	300	200	250	300	µA
Indicate Saturation	I_L = 10mA		0.2	0.5		0.2	0.5	V
Indicate Leakage	V_{IND} = 40V		.01	1.0		0.1	1.0	µA
Propagation Delay	$V_{O.V.\ INPUT}$ = 2.7V, $V_{U.V.\ INPUT}$ = 2.3V, T_J = 25°C							
	C_D = 0		400			400		ns
	C_D = 1µF		10			10		ms
SCR Trigger Section								
Peak Output Current	$+V_{IN}$ = 5V, R_G = 0, V_O = 0	100	200	400	100	200	400	mA
Peak Output Voltage	$+V_{IN}$ = 15V, I_O = 100mA	12	13		12	13		V
Output Off Voltage	$+V_{IN}$ = 40V, R_L = 1KΩ		0	0.1		0	0.1	V
Remote Activate Current	REM. ACT. pin = Gnd		0.4	0.8		0.4	0.8	mA
Remote Activate Voltage	REM. ACT pin open		2	6		2	6	V
Reset Current	RESET pin = Gnd, REM. ACT. = Gnd		0.4	0.8		0.4	0.8	mA
Reset Voltage	RESET pin open, REM. ACT. = Gnd		2	6		2	6	V
Output Current Rise Time	R_L = 50Ω, T_J = 25°C, C_D = 0		400			400		mA/µs
Prop. Delay from REM. ACT. Pin	$V_{REM.\ ACT.}$ = 0.4V		300			300		ns
Prop. Delay fom O.V. INPUT Pin	$V_{O.V.\ INPUT}$ = 2.7V		500			500		ns
Current Limit Section								
Input Voltage Range		0		V_{IN}-3V	0		V_{IN}-3V	V
Input Bias Current	OFFSET/COMP pin open, V_{CM} = 0V		0.3	1.0		0.3	1.0	µA
Input Offset Voltage	OFFSET/COMP pin open, V_{CM} = 0V		0	10		0	15	mV
	10kΩ from OFFSET/COMP pin to Gnd	80	100	120	70	100	130	mV
CMRR	0 ≤ V_{CM} ≤ 12V, V_{IN} = 15V	60	70		60	70		dB
AVOL	OFFSET/COMP pin open, V_{CM} = 0V	72	80		72	80		dB
Output Saturation	I_L = 10mA		0.2	0.5		0.2	0.5	V
Output Leakage	V_{IND} = 40V		.01	1.0		.01	1.0	µA
Small Signal Bandwidth	A_V = 0dB, T_J = 25°C		5			5		MHz
Propagation Delay	$V_{OVERDRIVE}$ = 100mV, T_J = 25°C		200			200		ns

Note 5. Input voltage rising on O.V. Input and falling on U.V. Input.

CHARACTERISTIC CURVES

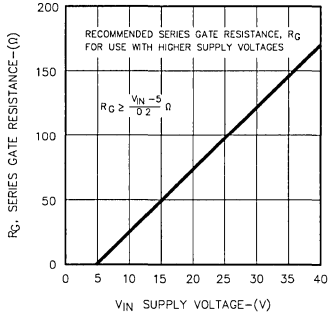


FIGURE 1.
SCR TRIGGER POWER LIMITING

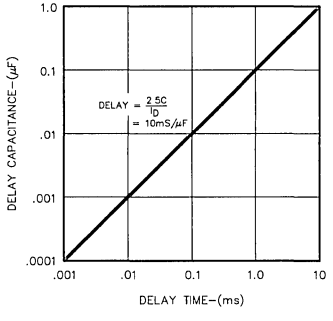


FIGURE 2.
ACTIVATION DELAY VS. CAPACITOR VALUE

CHARACTERISTIC CURVES (continued)

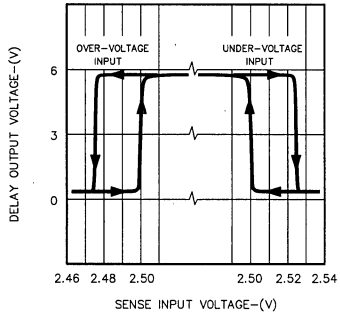


FIGURE 3.
COMPARATOR INPUT HYSTERESIS

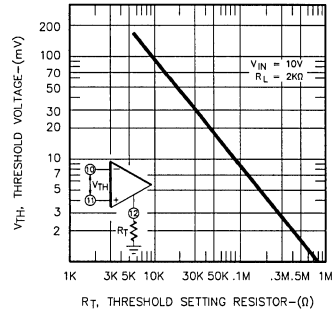


FIGURE 4.
CURRENT LIMIT INPUT THRESHOLD

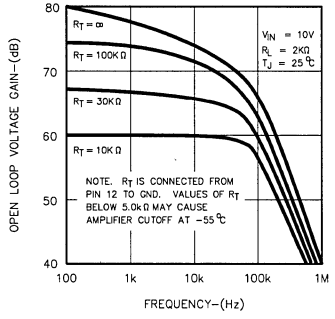


FIGURE 5.
CURRENT LIMIT AMPLIFIER GAIN

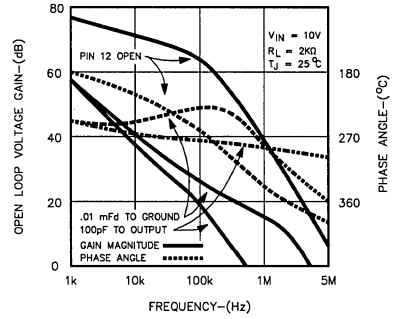


FIGURE 6.
CURRENT LIMIT AMPLIFIER FREQUENCY RESPONSE

APPLICATION INFORMATION

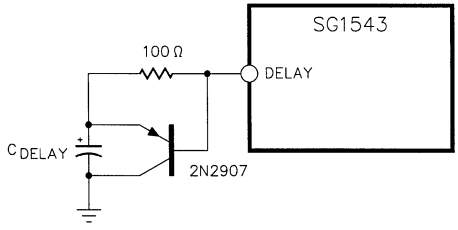


FIGURE 7 - SURGE LIMIT CIRCUIT FOR LARGE DELAY CAPACITORS

The 100 ohm resistor limits the peak discharge current into the SG1543 while the external PNP transistor provides a high peak-current discharge path for the delay capacitor.

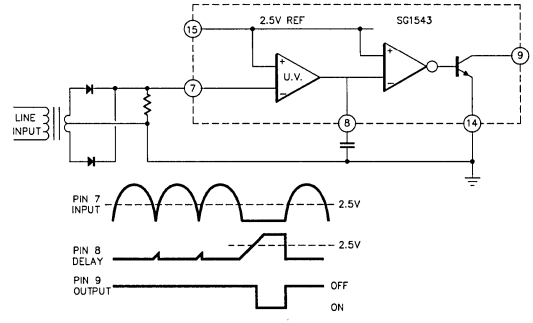


FIGURE 8 - INPUT LINE MONITOR

APPLICATION INFORMATION (continued)

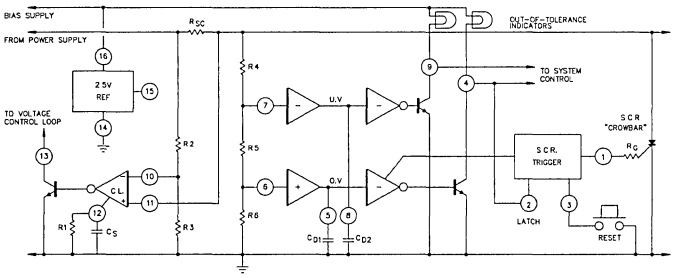


FIGURE 9 - TYPICAL APPLICATION CIRCUIT

The values for the external components are determined as follows:

Current limit input threshold, $V_{TH} \approx \frac{1000}{R_1}$

C_S is determined by the current loop dynamics

Peak current to load, $I_P \approx \frac{V_{TH}}{R_{SC}} + \frac{V_O}{R_{SC}}\left(\frac{R_2}{R_2+R_3}\right)$

Short circuit current, $I_{SC} = \frac{V_{TH}}{R_{SC}}$

Low output voltage limit, V_O (Low) $= \frac{2.5\,(R_4+R_5+R_6)}{R_5+R_6}$

High output voltage limit, V_O (High) $= \frac{2.5\,(R_4+R_5+R_6)}{R_6}$

Voltage sensing delay, $t_D = 10{,}000\ C_D$

SCR trigger power limiting resistor, $R_G > \frac{V_{IN} - 5}{0.2}$

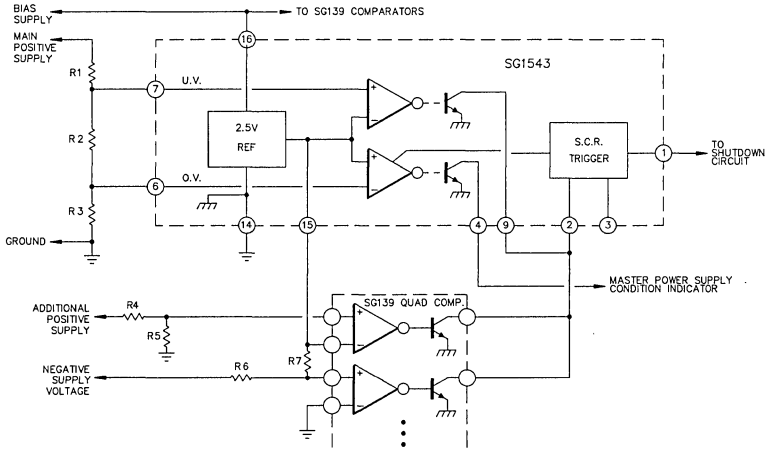


FIGURE 10 - SENSING MULTIPLE SUPPLY VOLTAGES

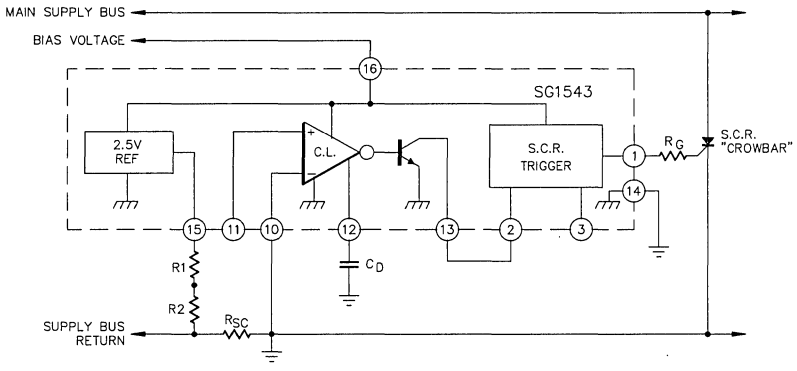
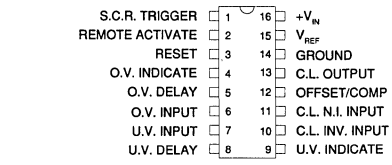
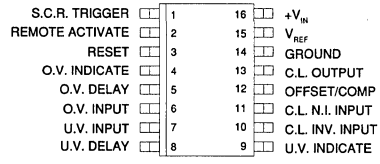
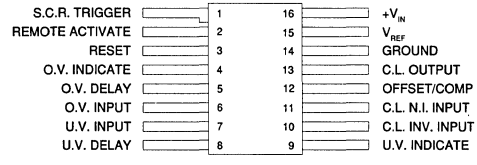
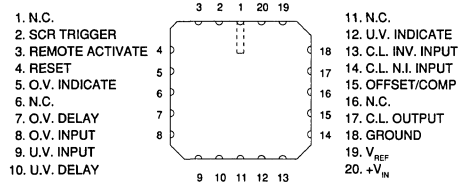


FIGURE 11 - OVERCURRENT SHUTDOWN

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG1543J/883B SG1543J SG2543J SG3543J	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
16-PIN PLASTIC DIP N - PACKAGE	SG2543N SG3543N	-25°C to 85°C 0°C to 70°C	
16-PIN WIDE BODY PLASTIC S.O.I.C. DW - PACKAGE	SG2543DW SG3543DW	-25°C to 85°C 0°C to 70°C	
16-PIN CERAMIC FLAT PACK F - PACKAGE (Note 3)	SG1543F/883B SG1543F	-55°C to 125°C -55°C to 125°C	
20-PIN CERAMIC LEADLESS CHIP CARRIER L- PACKAGE (Note 3)	SG1543L/883B SG1543L	-55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.
3. Consult factory for product availability.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

LOW-VOLTAGE SUPERVISORY CIRCUIT

DESCRIPTION

This device was designed to provide all the operational features of the SG1543/2543/3543 devices but with the added advantage of uncommitted inputs to the voltage sensing comparators. This allows monitoring of voltage levels less than 2.5 volts by dividing down the internal reference supply.

In all other respects, the SG1544 series is identical to the SG1543 series. These monolithic devices contain all the functions necessary to monitor and control the output of a sophisticated power supply system. Over-voltage sensing with provision to trigger an external SCR "crowbar" shutdown; an under-voltage circuit which can be used to monitor either the output or sample the input line voltage; and a third op amp/comparator usable for current sensing are all included in this IC, together with an independent, accurate reference generator.

The voltage-sensing input comparators are identical and can be used with threshold levels from zero volts to (V_{IN} - 3V). Each has approximately 25mv of hysteresis which is offset so the switching differential threshold is zero on the non-inverting input for rising levels and zero on the inverting input for falling signals. All other operating characteristics are as described in the SG1543 data sheet and application note.

FEATURES

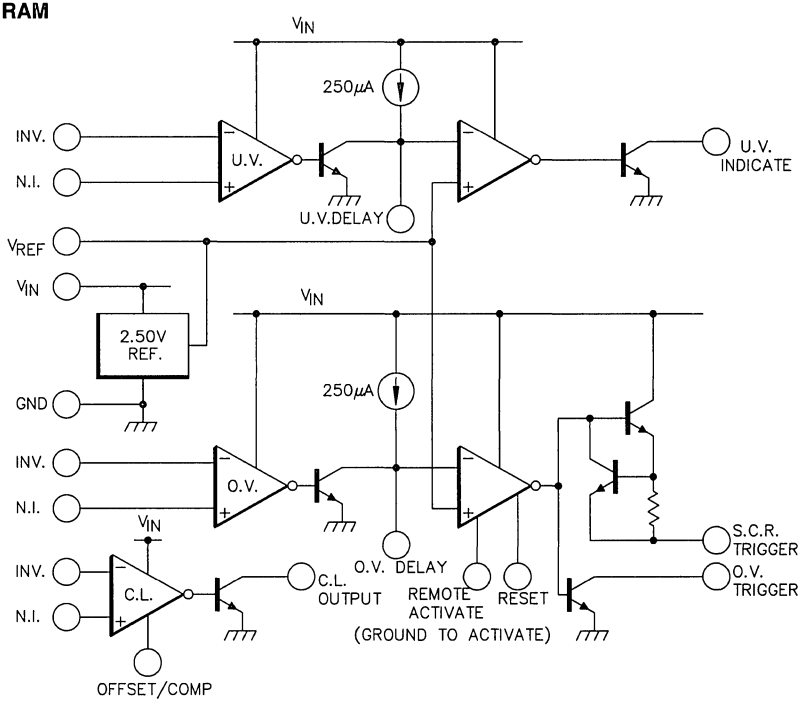
- **Uncommitted comparator inputs for wide input flexibility**
- **Common-Mode range from zero to near supply voltage**
- **Reference voltage trimmed to 1% accuracy**
- **Over-voltage, under-voltage, and current sensing circuits all included**
- **SCR "Crowbar" drive of 300mA**
- **Programmable time delays**
- **Open-collector outputs and remote activation capability**
- **Total standby current less than 10mA**

HIGH RELIABILITY FEATURES - SG1544

- **Available to MIL-STD-883 and DESC SMD**
- **SG level "S" processing available**

4

BLOCK DIAGRAM



April 1990

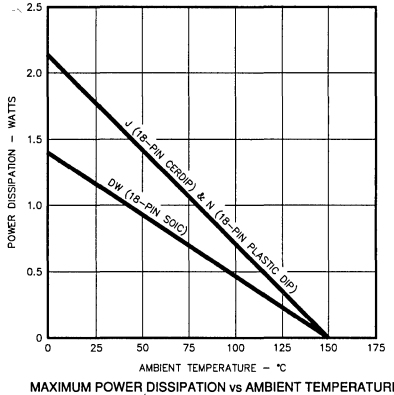
See Application Notes for additional information.

ABSOLUTE MAXIMUM RATINGS (Note 1)

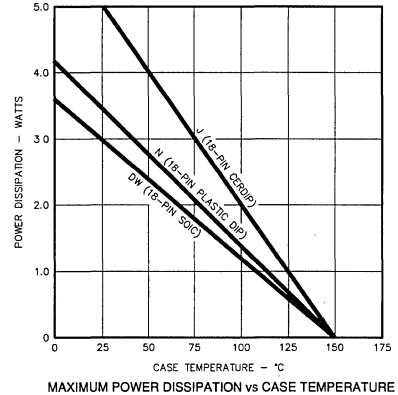
Input Supply Voltage ($+V_{IN}$) 40V
Sense Inputs ..... $+V_{IN}$
SCR Trigger Current (Note 2) 300mA
Indicator Output Voltage 40V
Indicator Output Sink Current 50mA
Operating Junction Temperature
Hermetic (J Package) ..... 150°C
Plasitc (N, DW Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C

Note 1. Values beyond which damage may occur.
Note 2. At higher input voltages, a dissipation limiting resistor, R_G, is required. See Figure 1.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 3)

Input Supply Voltage ($+V_{IN}$) ..... 4.7V to 40V
Current Limit Common Mode
Input Voltage Range ..... 0V to $+V_{IN}$ -3V
Reference Load Current ..... 0 to 10mA
Indicator Output Voltage ..... 4.7V to 40V
Indicator Output Current ..... 0 to 10mA
Delay Timing Capcitor (Note 4) ..... 0 to 1µF
Operating Ambient Temperature Range
SG1544 ..... -55°C to 125°C
SG2544 ..... -25°C to 85°C
SG3544 ..... 0°C to 70°C

Note 3: Range over which the device is functional.
Note 4. Larger value capacitor may be used with peak current limiting. See Figure 1.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1544 with $-55°C \le T_A \le 125°C$, SG2544 with $-25°C \le T_A \le 85°C$, SG3544 with $0°C \le T_A \le 70°C$, and $+V_{IN}$ = 10V. Indicator outputs have 2kΩ pull-up resistors. All electrical ratings and specifications are tested with the inverting over-voltage input and the non-inverting under-voltage input externally connected to the 2.5V reference. Low duty cycle testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1544/2544			SG3544			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Section								
Input Voltage Range	T_J = 25°C to T_{MAX}	4.5		40	4.5		40	V
		4.7		40	4.7		40	V
Supply Current	$+V_{IN}$ = 40V, Outputs open		7	10		7	10	mA
Reference Section								
Output Voltage	T_J = 25°C	2.48	2.50	2.52	2.45	2.50	2.55	V
		2.45		2.55	2.40		2.60	V
Line Regulation	$+V_{IN}$ = 5 to 30V		1	5		1	5	mV
Load Regulation	I_{REF} = 0 to 10mA		1	10		1	10	mV
Short Circuit Current	V_{REF} = 0V	12	25	40	12	25	40	mA
Temperature Stability			.005			.005		%/°C

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1544/2544			SG3544			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Comparator Section								
Input Threshold (Note 5)	T_J = 25°C	2.45	2.50	2.55	2.40	2.50	2.60	V
		2.40		2.60	2.35		2.65	V
Input Hysteresis			25			25		mV
Input Bias Current	Sense input = 0V		0.3	1.0		0.3	1.0	µA
Delay Saturation			0.2	0.5		0.2	0.5	V
Delay High Level			6	8		6	8	V
Delay Charging Current	V_D = 0V	200	250	300	200	250	300	µA
Indicate Saturation	I_L = 10mA		0.2	0.5		0.2	0.5	V
Indicate Leakage	V_{IND} = 40V		.01	1.0		0.1	1.0	µA
Propagation Delay	$V_{O.V.\ N\ I.\ IN}$ = 2.7V, $V_{U.V.\ INV.\ IN}$ = 2.3V, T_J = 25°C							
	C_D = 0		400			400		ns
	C_D = 1µF		10			10		ms
SCR Trigger Section								
Peak Output Current	$+V_{IN}$ = 5V, R_G = 0, V_O = 0	100	200	400	100	200	400	mA
Peak Output Voltage	$+V_{IN}$ = 15V, I_O = 100mA	12	13		12	13		V
Output Off Voltage	$+V_{IN}$ = 40V, R_L = 1KΩ		0	0.1		0	0.1	V
Remote Activate Current	REM. ACT. pin = Gnd		0.4	0.8		0.4	0.8	mA
Remote Activate Voltage	REM. ACT pin open		2	6		2	6	V
Reset Current	RESET pin = Gnd, REM. ACT. = Gnd		0.4	0.8		0.4	0.8	mA
Reset Voltage	RESET pin open, REM. ACT. = Gnd		2	6		2	6	V
Output Current Rise Time	R_L = 50Ω, T_J = 25°C, C_D = 0		400			400		mA/µs
Prop. Delay from REM. ACT. Pin	$V_{REM.\ ACT.}$ = 0.4V		300			300		ns
Prop. Delay fom O.V. N.I. IN Pin	$V_{O.V.\ N.I.\ INPUT}$ = 2.7V		500			500		ns
Current Limit Section								
Input Voltage Range		0		V_{IN}-3V	0		V_{IN}-3V	V
Input Bias Current	OFFSET/COMP pin open, V_{CM} = 0V		0.3	1.0		0.3	1.0	µA
Input Offset Voltage	OFFSET/COMP pin open, V_{CM} = 0V		0	10		0	15	mV
	10Ω from OFFSET/COMP pin to Gnd, T_J = 25°C	80	100	120	70	100	130	mV
CMRR	$0 \le V_{CM} \le 12V$, V_{IN} = 15V	60	70		60	70		dB
AVOL	OFFSET/COMP pin open, V_{CM} = 0V	72	80		72	80		dB
Output Saturation	I_L = 10mA		0.2	0.5		0.2	0.5	V
Output Leakage	V_{IND} = 40V		.01	1.0		.01	1.0	µA
Small Signal Bandwidth	A_V = 0dB, T_J = 25°C		5			5		MHz
Propagation Delay	$V_{OVERDRIVE}$ = 100mV, T_J = 25°C		200			200		ns

Note 5. Input voltage rising on O.V. N.I. INPUT and falling on U.V. INV. INPUT.

APPLICATION INFORMATION

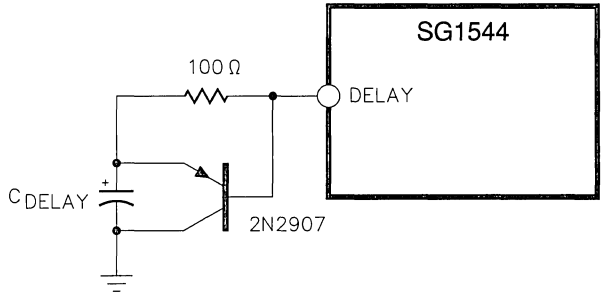
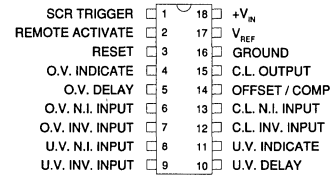
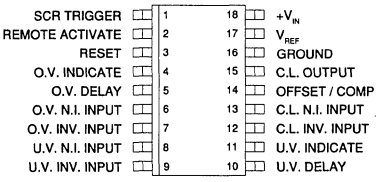


FIGURE 1 - SURGE LIMIT CIRCUIT FOR LARGE DELAY CAPACITORS

The 100 ohm resistor limits the peak discharge current into the SG1544 while the external PNP transistor provides a high peak-current discharge path for the delay capacitor.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
18-PIN CERAMIC DIP J - PACKAGE	SG1544J/883B SG1544J SG2544J SG3544J	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
18-PIN PLASTIC DIP N - PACKAGE	SG2544N SG3544N	-25°C to 85°C 0°C to 70°C	
18-PIN WIDE BODY PLASTIC S.O.I.C. DW - PACKAGE	SG2544DW SG3544DW	-25°C to 85°C 0°C to 70°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

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SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

QUAD POWER FAULT MONITOR

DESCRIPTION

The SG1548 is an integrated circuit capable of monitoring up to four positive DC supply voltages simultaneously for overvoltage and undervoltage fault conditions. An on-chip inverting op amp also allows monitoring one negative DC voltage. The fault tolerance window is accurately programmable from ±5% to ±40% using a simple divider network on the 2.5V reference. A single external capacitor sets the fault indication delay, eliminating false outputs due to switching noise, logic transition current spikes, and short-term AC line interruptions. An additional comparator referenced to 2.5V allows the AC line to be monitored for undervoltage conditions or for generation of a line clock. The comparator can also be used for programmable undervoltage lockout in a switching power supply. Uncommitted collector and emitter outputs permit both inverting and non-inverting operation. External availability of the precision 2.5V reference and open-collector logic outputs permit expansion to monitor additional voltage using available open-collector quad comparators.

FEATURES

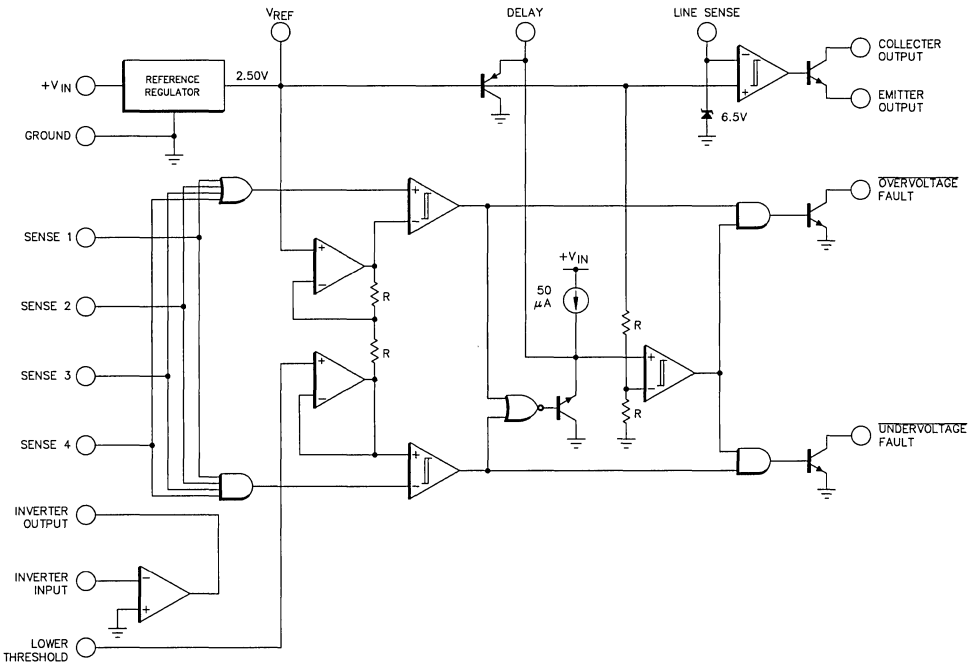
- **Monitors four DC voltages and the AC line**
- **Precision 2.5V ±1% low-drift reference**
- **Fault tolerance adjustable from ±5% to ±40%**
- **±3% trip threshold tolerance over temperature**
- **Separate 10mA, 40V overvoltage, undervoltage and AC line fault outputs**
- **Fault delay programmable with a single capacitor**
- **30mV comparator hysteresis to prevent oscillations**
- **On-chip inverting op amp for negative voltage**
- **Open-collector output logic or expandability**
- **Operation from 4.5V to 40V supply**

HIGH RELIABILITY FEATURES - SG1548

- **Available to MIL-STD-883**
- **Radiation data available**
- **SG level "S" processing available**

4

BLOCK DIAGRAM



April 1990

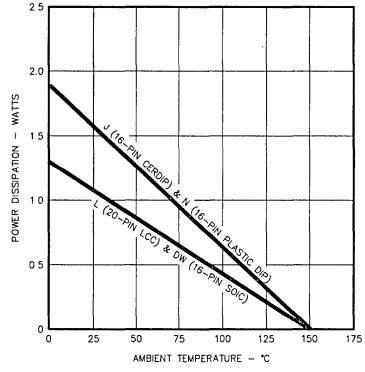
See Application Notes for additional information.

ABSOLUTE MAXIMUM RATINGS (Note 1)

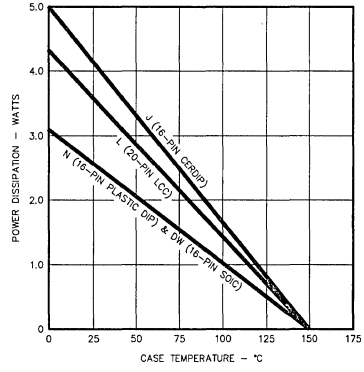
Supply Voltage ($+V_{IN}$) 40V
Fault Output Collector Voltage 40V
Sense Input Voltage Range ..... -0.3V to 6.0V
Fault Output Sink Current 20mA
Line Sense Input Current ..... ±1mA
Inverting Op Amp Input Current ..... -5mA
Inverting Op Amp Output Current 25mA
Operating Junction Temperature
  Hermetic (J, L Packages) ..... 150°C
  Plastic (N, DW Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature ..... 300°C

Note 1. Values beyond which damage may occur.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage Range
  ±25% Maximum Fault Window (Note 3) ..... 4.5V to 35V
  ±40% Maximum Fault Window ..... 5.0V to 35V
Lower Threshold Input Range ..... 1.5V to 2.45V
Fault Tolerance Window Range ..... ±5% to ±40%
Fault Output Sink Current Range ..... 0 to 10mA
Line Sense Output Current Range ..... 0 to 10mA
Voltage Reference Output Current ..... 0 to 10mA
Operating Ambient Temperature Range
  SG1548 ..... -55°C to 125°C
  SG2548 ..... -25°C to 85°C
  SG3548 ..... 0°C to 70°C

Note 2. Range over which the device is functional.

Note 3. Limited by inverter amplifier positive swing at -55°C.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1548 with $-55°C \le T_A \le 125°C$, SG2548 with $-25°C \le T_A \le 85°C$, SG3548 with $0°C \le T_A \le 70°C$, and $+V_{IN} = 15V$. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1548/2548			SG3548			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Section								
Supply Current	$+V_{IN} = 40V$		4.8	10		4.8	10	mA
Reference Section (Note 4)								
Output Voltage	$T_J = 25°C$	2.475	2.500	2.525	2.475	2.500	2.525	V
	Over Temperature	2.450		2.550	2.450		2.550	V
Line Regulation	$+V_{IN} = 4.5V$ to 35V		1	5		1	5	mV
Load Regulation	$I_L = 0$ to 10mA		3	10		3	10	mV
Short Circuit Current	$V_{REF} = 0V$	10	25	40	10	25	40	mA
Fault Window Generator Section								
Input Bias Current	$V_{PIN\ 1} = 1.5V$ to 2.45V		-0.4	-2.0		-0.4	-2.0	µA
DC Sense Inputs Section								
Overvoltage Threshold	$V_{PIN\ 1} = 0.95 \times V_{REF}$	2.547	2.625	2.704	2.547	2.625	2.704	V
	$V_{PIN\ 1} = 0.60 \times V_{REF}$	3.396	3.500	3.606	3.396	3.500	3.606	V
Undervoltage Threshold	$V_{PIN\ 1} = 0.95 \times V_{REF}$	2.304	2.375	2.447	2.304	2.375	2.447	V
	$V_{PIN\ 1} = 0.60 \times V_{REF}$	1.455	1.500	1.545	1.455	1.500	1.545	V
Input Bias Current	$V_{SENSE} = 1.5V$ to 3.5V		±0.6	±2.0		±0.6	±2.0	µA
Threshold Supply Rejection	$+V_{IN} = 4.5V$ to 35V	60	100		60	100		dB

Note 4. $I_L = 0mA$

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1548/2548			SG3548			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Fault Delay Section								
Comparator Threshold		1.200	1.250	1.300	1.200	1.250	1.300	V
Comparator Hysteresis			25			25		mV
Delay Charging Current	$V_{PIN\ 8}$ = 0V	32.5	50	67.5	32.5	50	67.5	µA
On Saturation Voltage	$I_{PIN\ 8}$ = 0mA		0.1	0.2		0.1	0.2	V
OFF Clamp Voltage	$I_{PIN\ 8}$ = 0mA		+3.2	+3.6		+3.2	+3.6	V
Inverting Op Amp Section (Note 5)								
Input Offset Voltage			2	15		2	15	mV
Input Bias Current			-0.3	-1.0		-0.3	-1.0	µA
Output High Voltage	I_{SOURCE} = 5mA	3.2	3.5		3.2	3.5		V
Output Low Voltage	I_{SINK} = 5mA		1.0	1.9		1.0	1.9	V
Large Signal Voltage Gain	R_L = 10K	72	100		72	100		dB
Output Source Current		5	15	25	5	15	25	mA
Power Supply Rejection Ratio	$+V_{IN}$ = 4.5V to 35V	72	100		72	100		dB
AC Line Sense Section								
Comparator Threshold	$V_{PIN\ 5}$ = Low to High	2.440	2.500	2.560	2.440	2.500	2.560	V
Comparator Hysteresis			25			25		mV
Input Bias Current	$V_{PIN\ 5}$ = 2.5V		1	2		1	2	µA
Collector Leakage Current	V_{CE} = 40V		1	10		1	10	µA
Collector Saturation Voltage	I_C = 10mA		0.2	0.5		0.2	0.5	V
Emitter Output Voltage	I_E = 10mA	12	13		12	13		V
Diode Clamp Voltage	$I_{PIN\ 5}$ = 1mA	6.0		7.5	6.0		7.5	V
	$I_{PIN\ 5}$ = -1mA	-0.3		-1.0	-0.3		-1.0	V
Fault Logic Outputs (Each output)								
Collector Leakage Current	V_C = 40V		1	10		1	10	µA
Collector Saturation Voltage	I_C = 10mA		0.2	0.5		0.2	0.5	V

Note 5. $+V_{IN}$ = 4.5V.

APPLICATION INFORMATION

SETTING THE FAULT TOLERANCE WINDOW

The fault tolerance window is set by applying a voltage less than the +2.50Vreference to the Lower Threshold input (Pin 1). The voltage is obtained by a resistor divider from the reference (Pin 3) to ground. If ±5% tolerance is desired, then 95% of the reference (+2.375V) is applied to Pin 1. If ±40% is wanted, then 60% of the reference (+1.50V) is applied. In the example on the back page, the tolerance is ±5%. The nominal overvoltage and undervoltage thresholds are centered about the reference at +2.625V and +2.375V (+2.500V ±0.125V).

SCALING THE MONITORED SUPPLY VOLTAGES

Each positive voltage to be monitored is divided down to +2.50V with a resistor network and connected to one of the Sense inputs. Unused Sense inputs should be connected to the reference. This will not increase the bias current. A variation of the monitored voltages out of the programmed tolerance range will cause the appropriate overvoltage or undervoltage fault output to switch LOW. The effective tolerance on any input may be broadened with an additional resistor to the voltage reference. The example on the back page shows a ±10% tolerance on the +5Vsupply although the SG1548 is programmed for a ±5% tolerance. The procedure for calculating the resistor value is found in the SG1548 Application Note.

MONITORING A NEGATIVE VOLTAGE

A negative voltage can be converted to a positive one and simultaneously scaled to +2.50V by using the internal operational amplifier as an inverter. Only an input resistor and feedback resistor are required.

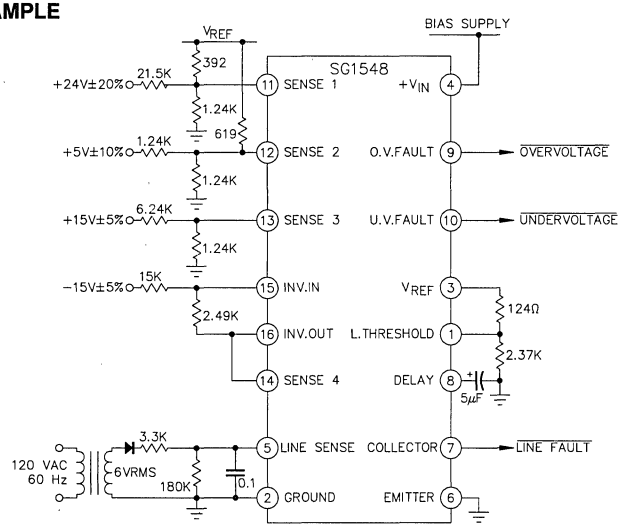
SETTING THE FAULT DELAY

A single capacitor at the Delay pin sets the time an out-of-tolerance fault must persist before a fault is actually declared. This feature allows switching noise on the supplies to be rejected. The delay time is given by: Delay = 25ms/µF .

AC LINE MONITORING

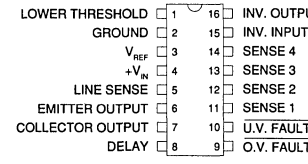
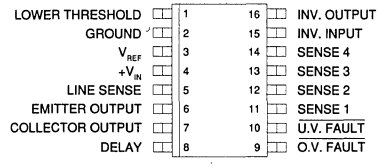
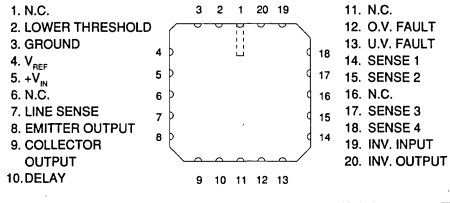
The AC line voltage can be monitored for single-cycle dropouts with the few components shown in the example. A half-wave rectifier charges the capacitor on positive line cycles. After the positive peak and during the negative line cycle the capacitor discharges from a fixed voltage controlled by the internal Zener diode. If a positive cycle is missing, the capacitor discharges to below the +2.5V trip point of the comparator, causing the output transistor to turn on.

APPLICATION EXAMPLE



In this example, the SG1548 simultaneously monitors four DC voltages: +5V, +24V, and ±15V. Three different fault tolerances are programmed: ±5% on the two 15V supplies, ±10% on the +5V supply, and ±20% on the +24V supply. The 5µF delay capacitor provides 125 milliseconds of fault delay.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG1548J/883B SG1548J SG2548J SG3548J	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
16-PIN PLASTIC DIP N - PACKAGE	SG2548N SG3548N	-25°C to 85°C 0°C to 70°C	
16-PIN WIDE BODY PLASTIC S.O.I.C. DW - PACKAGE	SG2548DW SG3548DW	-25°C to 85°C 0°C to 70°C	
20-PIN CERAMIC (LCC) LEADLESS CHIP CARRIER L- PACKAGE	SG1548L/883B SG1548L	-55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availability.
2. All parts are viewed from the top.

SG1549/SG2549/SG3549

CURRENT SENSE LATCH

DESCRIPTION

This monolithic integrated circuit is an analog latch device with digital reset. It was specifically designed to provide pulse-by-pulse current limiting for switch-mode power supply systems, but many other application are also feasible. Its function is to provide a latching switch action upon sensing an input threshold voltage, with reset accomplished by an external clock signal. This device can be interfaced directly with many kinds of pulse width modulating control IC's, including the SG1524, SG1525A and SG1527A.

The input threshold for the latch circuit is 100mV, which can be referenced either to ground or to a wide-ranging positive voltage. There are high and low-going output signals available, and both the supply voltage and clock signal can be taken directly from an associated PWM control chip.

With delays in the range of 200 nanoseconds, this latch circuit is ideal for fast reaction sensing to provide overall current limiting, short circuit protection, or transformer saturation control.

FEATURES

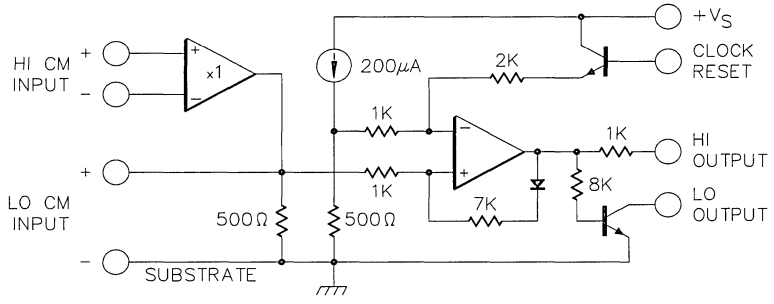
- **Current sensing with 100mV threshold**
- **Common-mode input at ground or to 40V**
- **Complementary outputs**
- **Automatic reset from PWM clock**
- **180ns delay**
- **Interface direct to SG1524, SG1525A, SG1527A**

HIGH RELIABILITY FEATURES - SG1549

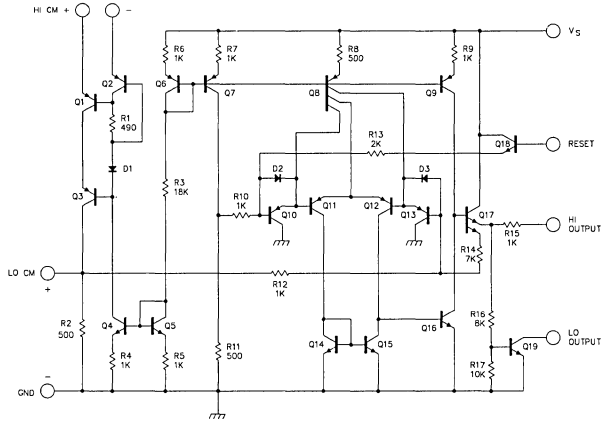
- **Available to MIL-STD-883**
- **SG level "S" processing available**
- **Radiation data available**

4

BLOCK DIAGRAM



SCHEMATIC



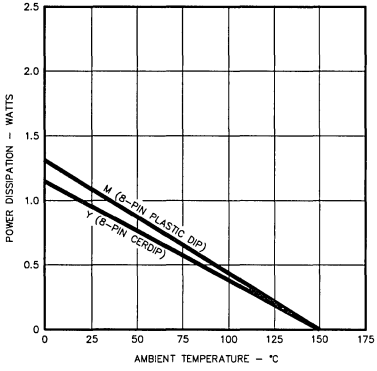
ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage, V_S 25V
HI CM Input Voltage 40V
LO Output "off" Voltage 40V
LO Output "on" current 25mA

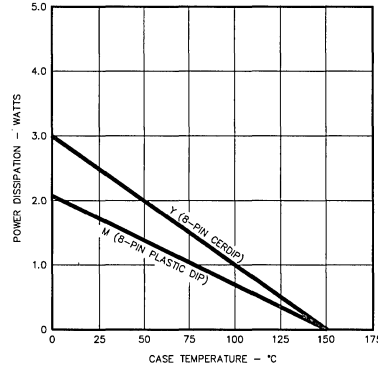
Operating Junction Temperature
Hermetic (Y Package) ..... 150°C
Plastic (N Package) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C

Note 1. Values beyond which damage may occur.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Supply Voltage, V_S 5.0V
HI CM Input Voltage ..... 2V to 40V
LO Output "off" Voltage ..... 5V to 40V
LO Output "on" Current ..... 0 to 10mA
Reset LO Voltage ..... 0V to 0.8V

Reset HI Voltage ..... 2.5V to 5.0V
Operating Ambient Temperature Range
SG1549Y ..... -55°C to 125°C
SG2549Y or M ..... -25°C to 85°C
SG3549Y or M ..... 0°C to 70°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1549 with $-55°C \le T_A \le 125°C$, SG2549 with $-25°C \le T_A \le 85°C$, SG3549 with $0°C \le T_A \le 70°C$, and $V_S = 5V$. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1549/2549			SG3549			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Section								
Supply Current	$V_{PIN\ 8} = 5V$		2	3		2	5	mA
	$V_{PIN\ 8} = 20V$		10	15		10	15	mA
LO CM Input Section (Note 3)								
Threshold Voltage	Pin 1 & 2 shorted, $T_A = 25°C$	80	100	120	80	100	120	mV
	pin 1 & 2 shorted	70	100	130	70	100	130	mV
Input Impedance	$V_{PIN\ 3} = 50mV$, $T_A = 25°C$	400	500	600	400	500	600	Ω
	$V_{PIN\ 3} = 50mV$	300	500	700	300	500	700	Ω
HI CM Input Section (Note 3)								
Threshold Voltage	$V_{CM} = 2V$, Pin 3 open, $T_A = 25°C$	80	100	120	80	100	120	mV
	$V_{CM} = 40V$, Pin 3 open, $T_A = 25°C$	80	100	120	80	100	120	mV
	$V_{CM} = 2V$, Pin 3 open	70	100	130	70	100	130	mV
	$V_{CM} = 40V$, Pin 3 open	70	100	130	70	100	130	mV
Input Current	$V_{PIN\ 1} = V_{PIN\ 2} = 40V$		200	300		200	300	µA
Clock Reset Section								
Min. Trigger Voltage			2.0	2.5		2.0	2.5	V
Input Current	$V_{PIN\ 7} = 4V$		20	40		20	40	µA

Note 3. Input threshold voltages and supply current are directly proportional to supply voltage, V_S.

ELECTRICAL SPECIFICATIONS

(V_S = 5V, and over recomended operating temperature, unless otherwise specified.)

Parameter	Test Conditions	SG1549/2549			SG3549			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
HI Output Section								
Off Voltage			0	0.1		0	0.1	V
On Voltage	I_L = 1mA	2.8	3.2		2.8	3.2		V
LO Output								
Off Leakage	$V_{PIN\ 5}$ = 40V		.01	1.0		.01	1.0	µA
On Voltage	I_L = 5mA		.3	0.5		.3	0.5	V

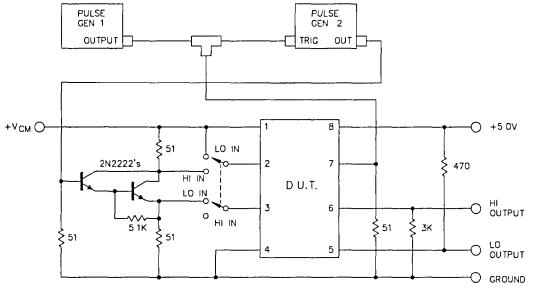
TYPICAL SWITCHING CHARACTERISTICS (Note 4)

(V_S = 5V, T_A = 25°C)

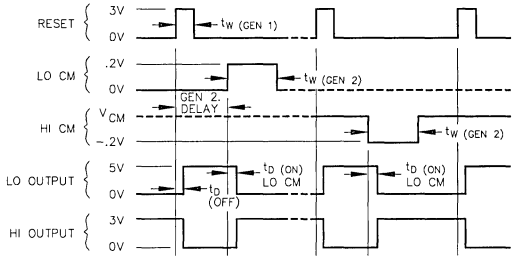
Parameter	Test Conditions	SG1549 Series			Units
		Min.	Typ.	Max.	
Reset Minimum Pulse Width (T_{W1})	Amplitude = 3.0V		150	300	ns
Delay from Reset to LO Output ($T_{D(OFF)}$)	R_L = 470Ω to V_S		300	600	ns
LO Input Minimum Pulse Width (T_{W2})	LO CM Amplitude = 200mV		50	300	ns
Delay from LO Input to LO Output ($T_{D(ON)}$)	LO CM Amplitude = 200mV, R_L = 470Ω to V_S		180	360	ns
Delay from HI Input to LO Output ($T_{D(ON)}$)	Amplitude = 200mV, V_{CM} = 5V		300	900	ns
Delay from HI Output to LO Output	LO CM Input = 200mV		30	60	ns

Note 4: These parameters, although guaranteed, are not tested in production.

DYNAMIC TEST CIRCUIT



SWITCHING WAVEFORMS



APPLICATION NOTES

HIGH LINE SENSING - The SG1549 will provide current sensing in the positive supply line in the typical SG1524 single-ended switching regulator application shown in Figure 1. The HI CM sense circuitry can be used with input voltages between 2 and 40 volts.

A value for R_{SC} is determined by dividing the 100mV input threshold by the peak current desired. High-frequency noise, or switching transients, can usually be eliminated by a small capacitor between pins 3 and 4.

Current control may be accomplished by either the HI OUTPUT pin connected to the SG1524's Shutdown pin, or the LO OUTPUT pin connected directly to the Compensation Terminal. In either case, activation of the current sense latch will tend to discharge the compensation capacitor, C_C, which may cause slow recovery from pulse limiting. If this feature is desired, the LO OUTPUT pin may be used to discharge a soft-start network instead of coupling directly to the SG1524. If it is not desired, the use of a small value of C_C, and perhaps a diode across R_C, will enhance recovery.

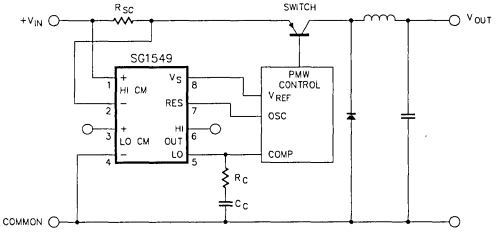


FIGURE 1 — HIGH LINE SENSING WITH THE SG1549 IN CONJUNCTION WITH AN SG1524 PWM CONTROL IC

APPLICATION NOTES (continued)

Another method of introducing the current shutdown signal is shown in Figure 2 where the SG1524 is used to activate a constant drive current to the high-current switch, in this case an SM600. The 2N2222 forms a constant current generator when driven from the SG1524's 5.0 volt reference through a 1K resistor. This transistor is then switched off by the LO OUTPUT transistor in the SG1549, achieving the fastest response to the output of the regulator.

LOW LINE SENSING - In many types of feed-forward or push-pull converters, current protection may be provided by sensing in an emitter resistor referenced to ground on the primary side of an output transformer. The fast-reacting SG1549 can easily sense secondary overload as reflected back to the primary and, additionally, provide protection from unbalanced transformer saturation.

When using the LO CM inputs, the HI CM inputs should be shorted together. While the LO CM inputs may be connected directly across a sense resistor, R_{SC}, a small low-pass filter as shown in Figure 3 is often required to eliminate high frequency transients. It must be remembered that the 500Ω input impedance at the LO CM terminals will cause the use of R1 to increase the effective threshold; however, this also offers the possibility of an easily adjustable threshold by incorporating a potentiometer at the input.

Coupling the output signal from the SG1549 to the control chip may be done in several ways including the use of either the Compensation or Shutdown pins on the SG1524 as described earlier.

Another convenient way to tie the output of the SG1549 into the PWM control in higher power applications is by using the SG1627 Dual Interface Driver and connecting the LO OUTPUT terminal of the Sg1549 directly to the two Non-Inverting inputs of the SG1627 as shown in Figure 4.

And finally, keep in mind that the LO OUTPUT terminal of the SG1549 will easily drive most high-speed optical couplers should some type of isolation between current sense and shutdown control be required.

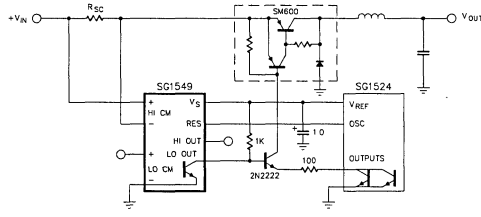


FIGURE 2 — CURRENT CONTROL FOR A BUCK REGULATOR WITH CONSTANT DRIVE CURRENT

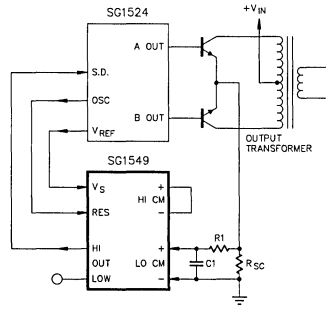


FIGURE 3 — A PUSH-PULL CONVERTER WITH LOW-LINE EMITTER CURRENT SENSING

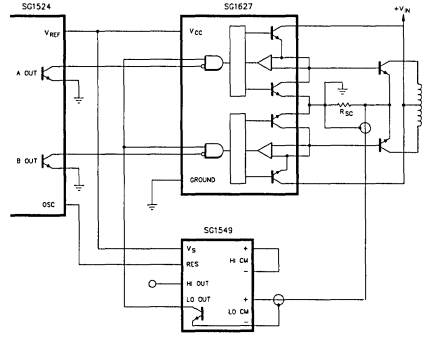


FIGURE 4 — POWER BOOST AND CURRENT CONTROL WITH THE SG1627

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
8-PIN CERAMIC DIP Y - PACKAGE	SG1549Y/883B SG1549Y SG2549Y SG3549Y	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	+ HI CM INPUT 1 — 8 +V_S — HI CM INPUT 2 — 7 CLOCK RESET + LO CM INPUT 3 — 6 HI OUTPUT — LO CM INPUT 4 — 5 LO OUTPUT
8-PIN PLASTIC DIP M - PACKAGE	SG2549M SG3549M	-25°C to 85°C 0°C to 70°C	

Note 1. Contact factory for JAN and DESC product availability.
2. All parts are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SG1557/SG2557/SG3557
SG1559/SG2559/SG3559
SG1560/SG2560/SG3560

FUTURE PRODUCT RELEASE

MAG AMP CONTROLLER

DESCRIPTION

The SG1557, SG1559, and SG1560 family of integrated circuits has been designed to incorporate some of the most commonly used analog functions in one dual in-line package. It includes a 1.25V ±1% band gap reference, guaranteed to operate as low as 4.5V over the entire temperature range. Two independent operational amplifiers with electrical characteristics similar to the industry standard LM324, as well as two uncommited, open collector comparators similar to LM139 are included in the I.C. This product line provides all the necessary control functions required for magnetic amplifier regulators where they are ideal choices as secondary side regulators requiring high current and high efficiency. It can also be used in power supply applications where PWM is on the primary side and the reference and error amp needs to be on the secondary side to maintain input/output isolation.

FEATURES

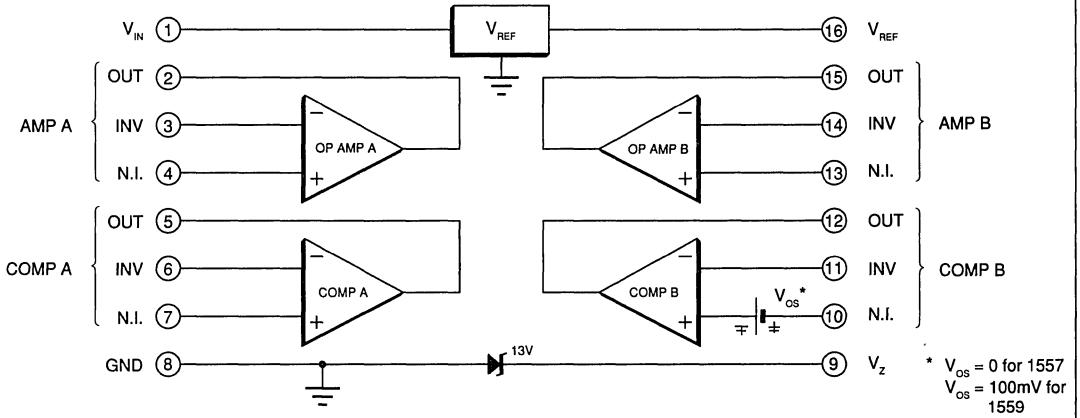
- **Low cost**
- **Two independent op amps**
- **Two uncommited open collector comparators**
- **4.5V to 40V input voltage operation over temperature (SG1557 and SG1559 only)**
- **±2% voltage reference over load, line and temperature**
- **13V zener for pre-regulating $+V_{IN}$ (SG1557 and SG1559 only)**
- **Available in SOIC package**

HIGH RELIABILITY FEATURES - SG1557/SG1559/SG1560

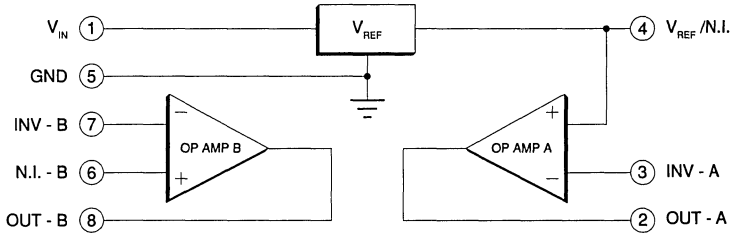
♦ **Available to MIL-STD-883**

4

BLOCK DIAGRAM



1557/1559



1560

April 1990

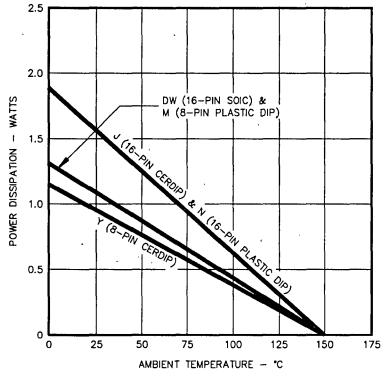
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V_{CC}) 42V
Amplifier Input Voltage ..... -0.3V to V_{CC}
Amplifier Output Current 30mA
Reference Load Current 30mA
Zener Current 25mA

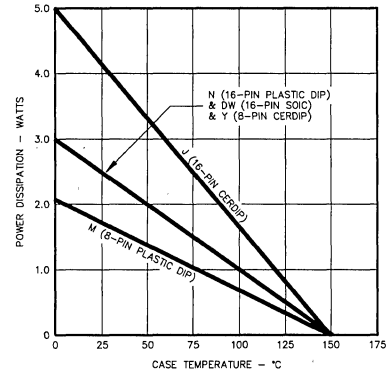
Operating Junction Temperature
Hermetic (J, Y-Packages) ..... 150°C
Plastic (N, M, DW-Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device. All voltages are with respect to ground. All currents are positive into the specified terminal.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage (V_{CC}) 35v
Amplifier Input Voltage ..... 0 to V_{CC}-2
Amplifier Output Current 15mA
Reference Load 15mA
Zener Current 15mA

Operating Ambient Temperature Range
SG1557, 1559, 1560 ..... -55°C to 125°C
SG2557, 2559, 2560 ..... -25°C to 85°C
SG3557, 3559, 3560 ..... 0°C to 70°C

Note 2: Range over which the device is functional.

ELECTRICAL SPECIFICATIONS *

(Unless otherwise specified, these specfiications apply over the operating ambient temperatures for SG1557/1559/1560 with -55°C ≤ T_A ≤ 125°C, SG2557/2559/2560 with -25°C ≤ T_A ≤ 85°C, SG3557/3559/3560 with 0°C ≤ T_A ≤ 70°C, and V_{CC} = 15V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1557/2557/3557 SG1559/2559/3559 SG1560/2560/3560			Units
		Min.	Typ.	Max.	
Reference Section					
Output Voltage	T_J = 25°C	1.237	1.250	1.263	V
Temperature Stability		-13		13	mV
Line Regulation	V_{IN} = 4.5V to 40V, T_J = 25°C	-13		13	mV
Load Regulation	I_{REF} = 0 to 15mA, T_J = 25°C	-13		13	mV
Total Output Voltage Range		1.225		1.275	V
Short Circuit Current	V_{REF} = 0V			100	mA

* NOTE: Performance data described herein represent design goals. Final device specifications are subject to change.

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1557/2557/3557 SG1559/2559/3559 SG1560/2560/3560			Units
		Min.	Typ.	Max.	
Op-Amp Section					
Input Offset Voltage		-10		10	mV
Input Bias Current				-1000	nA
Input Offset Current				-200	nA
Input Common Mode Range		0		V_{cc}-2	V
Open Loop Voltage Gain		80			dB
Unity Gain Bandwidth			1		MHz
Common Mode Rejection Ratio			70		dB
Power Supply Rejection Ratio		65			dB
Output Voltage Level - High	R_L = 2KΩ to GND	V_{cc}-1.5			V
Output Voltage Level - Low	R_L = 2KΩ to V_{CC}			1.2	V
Output Short-circuit Current			30		mA
Slew Rate	A_V = 1, V_{IN} = 2V to 12V		0.5		V/µs
Comparator Section (Applies to SG1557 and SG1559 family only)					
Input Offset Voltage (1557 only)				10	mV
Input Offset Voltage (1559 only)		95	100	110	mV
Input Bias Current	T_J = 25°C			1000	nA
Input Offset Current				200	nA
Input Common Mode Range		-0.5		V_{cc}-2	V
Output Sink Current	V_O = 1.5V	6			mA
Output Saturation Voltage	I_O = 4mA			400	mV
Input-Output Propagation Delay	$V_{N.I.}$ = 1.4V, V_{INV} = 0.7V to 2V			1000	ns
Open Loop Voltage Gain		80			dB
Other Parameters					
Supply Voltage		4.5		40	V
Supply Current				7	mA
Zener Voltage	(1mA to 20mA)	12.4	13.4	14.4	V
Zener Current		1		20	mA

4

APPLICATION INFORMATION

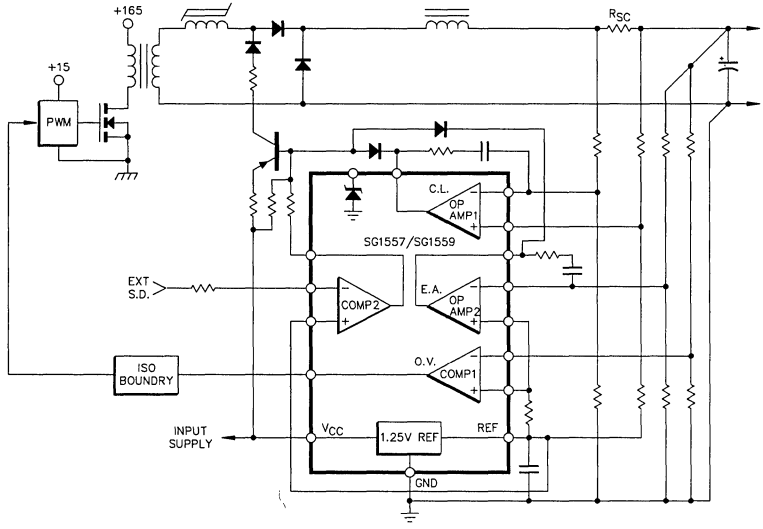


FIGURE 1 - MAGNETIC AMPLIFIER

Magnetic amplifiers are ideal choices where high current, high efficiency secondary regulation is required. Figure 1 shows the application of SG1557 and SG1559 in this Mag-Amp regulator.

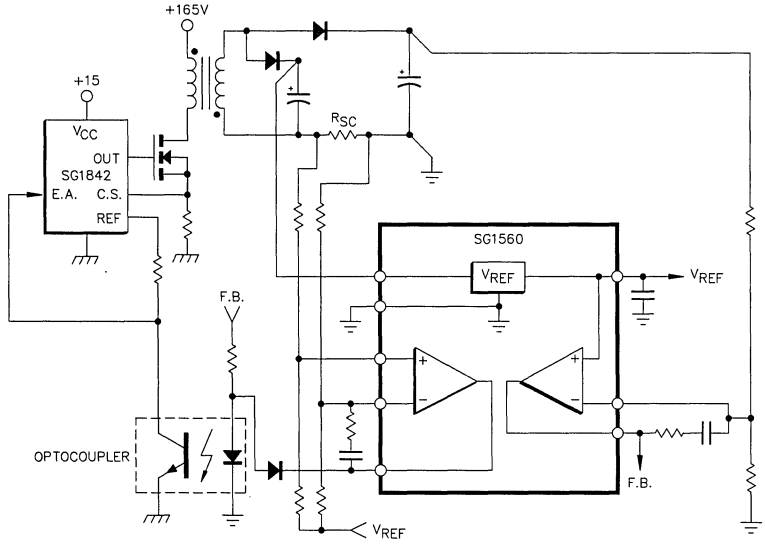
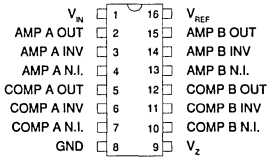
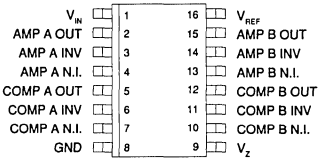
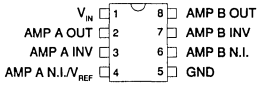


FIGURE 2 - FLYBACK POWER SUPPLY

SG1560 is an ideal choice for the applications where the PWM is in the primary side. Figure 2 shows the application of this device in this flyback power supply using SG1842 as the PWM.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG1557J/883B	-55°C to 125°C	
	SG1557J	-55°C to 125°C	
	SG2557J	-25°C to 85°C	
	SG3557J	0°C to 70°C	
	SG1559J/883B	-55°C to 125°C	
	SG1559J	-55°C to 125°C	
	SG2559J	-25°C to 85°C	
	SG3559J	0°C to 70°C	
16-PIN PLASTIC DIP N - PACKAGE	SG2557N	-25°C to 85°C	
	SG3557N	0°C to 70°C	
	SG2559N	-25°C to 85°C	
	SG3559N	0°C to 70°C	
16-PIN WIDE BODY PLASTIC S.O.I.C. DW - PACKAGE	SG2557DW	-25°C to 85°C	
	SG3557DW	0°C to 70°C	
	SG2559DW	-25°C to 85°C	
	SG3559DW	0°C to 70°C	
8-PIN CERAMIC DIP Y - PACKAGE	SG1560Y/883B	-55°C to 125°C	
	SG1560Y	-55°C to 125°C	
	SG2560Y	-55°C to 125°C	
	SG3560Y	-55°C to 125°C	
8-PIN PLASTIC DIP M - PACKAGE	SG2560M	-25°C to 85°C	
	SG3560M	0°C to 70°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.
3. Consult factory for product availability.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

DUAL-POLARITY TRACKING REGULATORS

DESCRIPTION

The SG1568/SG1468 is a dual-polarity tracking regulator designed to provide balanced positive and negative output voltages at currents to 100mA. The device is set internally for ±15V outputs but a single external adjustment can be used to change both outputs simultaneously from 9V to 20V. Input voltages up to ±30V can be used and there is provision for adjustable current limiting.

FEATURES

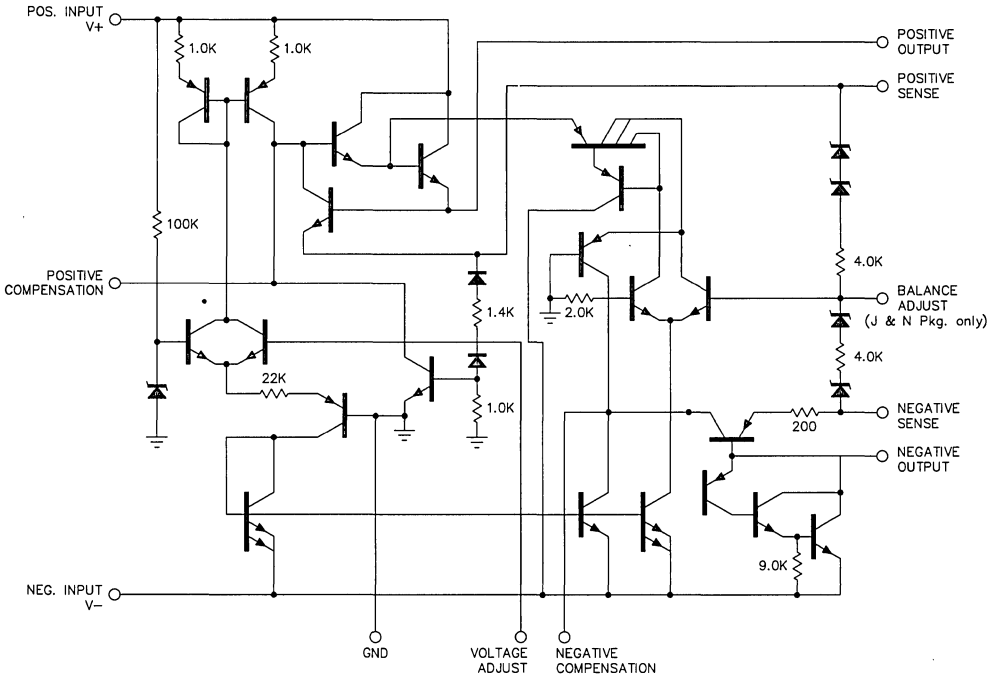
- **Outputs balanced to within 1% (SG1568)**
- **Line and load regulation of 0.06%**
- **1% maximum output variation due to temperature changes**
- **Standby current drain of 3.0mA**
- **Remote sensing provisions**

HIGH RELIABILITY FEATURES - SG1568

- **Available to MIL-STD-883**
- **SG level "S" processing available**

4

BLOCK DIAGRAM



April 1990

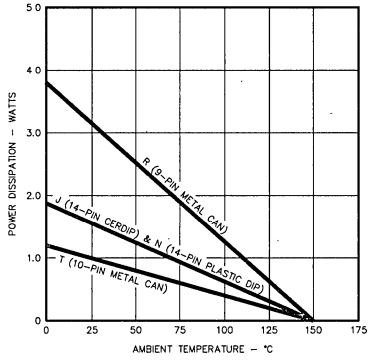
ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage 30V
Peak Load Current 100mA
Minimum Short-Circuit Resistance 4.0Ω

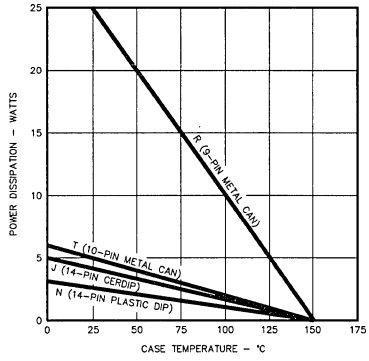
Note 1. Exceeding these ratings could cause damage to the device.

Operating Junction Temperature
Hermetic (J, T, R-Packages) ..... 150°C
Plastic (N-Package) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Voltage ..... 7.0V to 30V

Note 2. Range over which the device is functional.

Operating Ambient Temperature
SG1568 ..... -55°C to 125°C
SG1468 ..... 0°C to 70°C

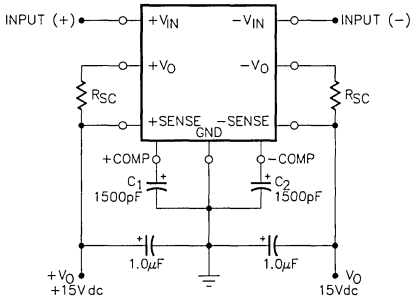
ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply for the operating ambient temperature T_A = 25°C, V_{CC} = 20V, V_{EE} = 20V, $C_1 = C_2$ = 1500pF, $C_3 = C_4$ = 1.0µF, $+I_L = -I_L = 0$, and R_{SC} = 4.0Ω for both positive and negative inputs. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1568			SG1468			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage		14.5		15.5	14.5		15.5	V
Input Voltage				30			30	V
Input-Output Voltage Differential				2.0			2.0	V
Output Voltage Balance				±150			±300	mV
Line Regulation Voltage	V_{IN} = 18V to 30V			10			10	mV
	$T_A = T_{MIN}$ to T_{MAX}			20			20	mV
Load RegulationVoltage (Note 3)	I_L = 0 to 50 mA			10			10	mV
	$T_A = T_{MIN}$ to T_{MAX}			30			30	mV
Output Voltage Range		9.0		20	9.0		20	V
Ripple Rejection	f = 120Hz		75			75		dB
Output Voltage Temperature Stability (Note 4)	$T_A = T_{MIN}$ to T_{MAX}			1.0			1.0	%
Short Circuit Current Limit	R_{SC} = 10Ω		60			60		mA
Output Noise Voltage	BW = 100Hz to 10KHz		100			100		µV(rms)
Positive Standby Current	V_{IN} = 30V			4.0			4.0	mA
Negative Standby Current	V_{IN} = -30V			3.0			3.0	mA
Long Term Stability			0.2			0.2		%/Khr

Note 3. Applies for constant junction temperature.
Note 4. This parameter, although guaranteed, is not tested in production.

APPLICATION INFORMATION



C1 and C2 should be located as close to the device as possible. A 0.1μF ceramic capacitor may be required on the input lines if the device is located an appreciable distance from the rectifier filter capacitors.

C3 and C4 may be increased to improve load transient response and to reduce the output noise voltage. At low temperature operation it may be necessary to bypass C4 with a 0.1μF ceramic disc capacitor.

FIGURE 1 - BASIC 50mA REGULATOR

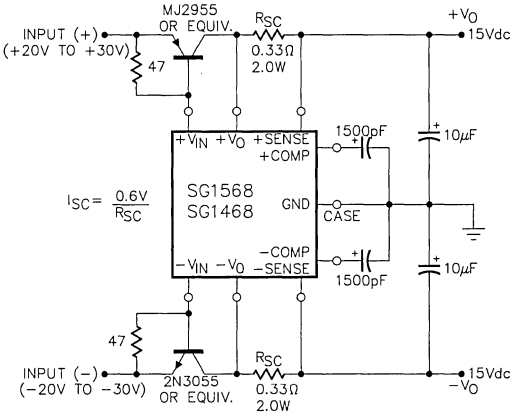
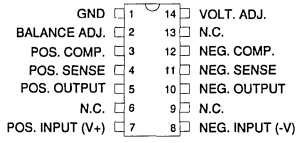
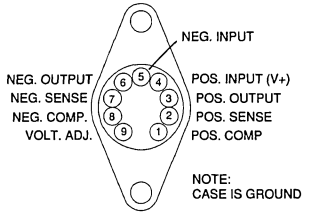
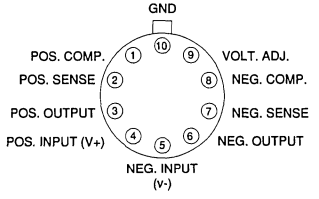


FIGURE 2 - 1.5A REGULATOR
SHORT CIRCUIT PROTECTED, WITH PROPER HEATSINKING

4

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN CERAMIC DIP J - PACKAGE	SG1568J/883B SG1568J SG1468J	-55°C to 125°C -55°C to 125°C 0°C to 70°C	
14-PIN PLASTIC DIP N - PACKAGE	SG1468N	0°C to 70°C	
9-PIN METAL CAN R - PACKAGE	SG1568R/883B SG1568R SG1568R SG1468R	-55°C to 125°C -55°C to 125°C 0°C to 70°C 0°C to 70°C	
10-PIN METAL CAN T - PACKAGE	SG1568T/883B SG1568T SG1568T SG1468T	-55°C to 125°C -55°C to 125°C 0°C to 70°C 0°C to 70°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

HIGH-SPEED CURRENT-MODE PWM

DESCRIPTION

The SG1825 is a high-performance pulse width modulator optimized for high frequency current-mode power supplies. Included in the controller are a precision voltage reference, micropower start-up circuitry, soft-start, high-frequency oscillator, wideband error amplifier, fast current-limit comparator, full double-pulse suppression logic, and dual totem-pole output drivers. Innovative circuit design and an advanced linear Schottky process result in very short propagation delays through the current limit comparator, logic, and output drivers. This device can be used to implement either current-mode or voltage-mode switching power supplies. It also is useful as a series-resonant controller to frequencies beyond 1MHz. The SG1825 is specified for operation over the full military ambient temperature range of -55°C to 150°C. The SG2825 is characterized for the industrial range of -25°C to 150°C, and the SG3825 is selected for the commercial range of 0°C to 125°C.

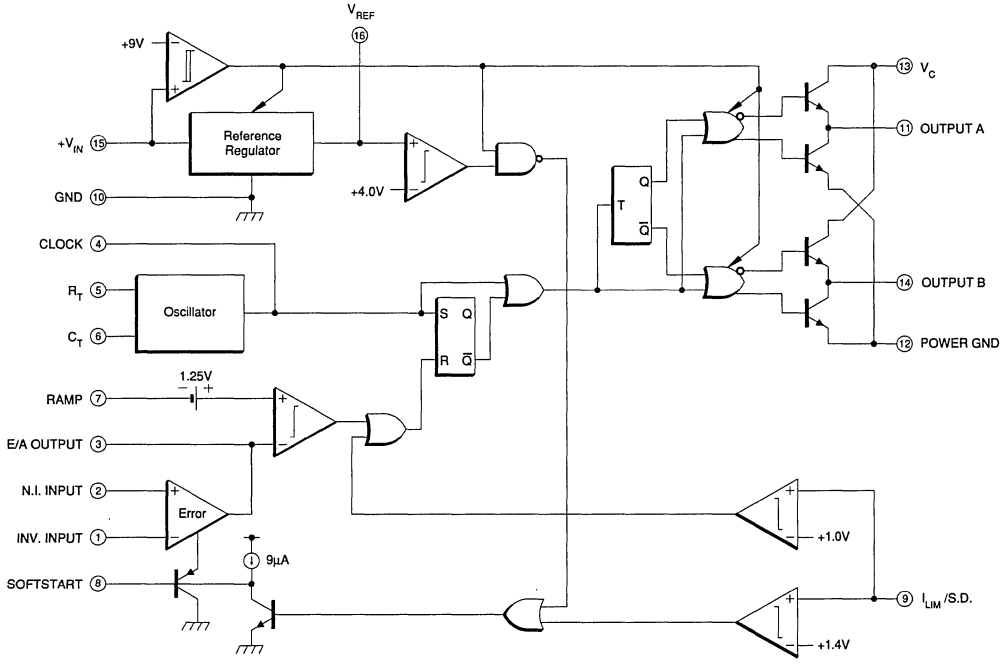
FEATURES

- **10 to 30 volt operation**
- **5.1V reference trimmed to ±1%**
- **2MHz oscillator capability**
- **80ns prop delay to outputs**
- **1.5A peak totem-pole drivers**
- **2mA max start-up current**
- **U.V. lockout with hysteresis**
- **No output driver "float"**
- **Programmable soft start**
- **Double-pulse suppression logic**
- **Wideband low-impedance error amp**
- **Current-mode or voltage-mode control**
- **Wide choice of high frequency packages**

HIGH RELIABILITY FEATURES - SG1825

- **Available to MIL-STD-883B**
- **Scheduled for MIL-M-38510 QPL listing**
- **SG level "S" processing available**

BLOCK DIAGRAM

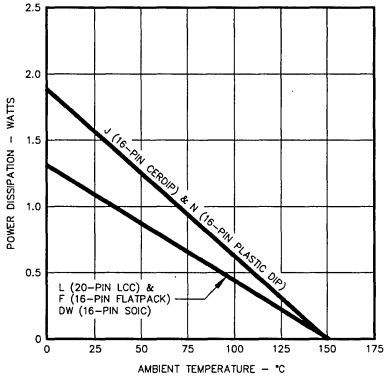


ABSOLUTE MAXIMUM RATINGS (Note 1)

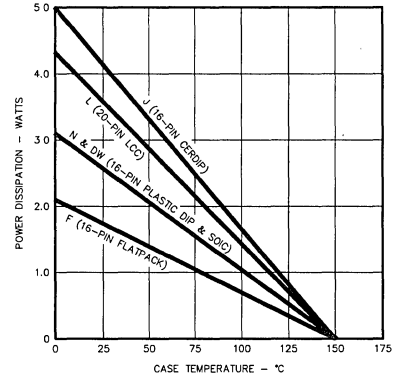
Input Voltage (V_{IN} and V_C) 30V
Analog Inputs:
  Error Amplifier and Ramp ..... -0.3V to 7.0V
  Soft Start and I_{LIM}/S.D. ..... -0.3V to 6.0V
Digital Input (Clock) ..... 1.5V to 6.0V
Driver Outputs ..... -0.3V to V_C+1.5V
Source / Sink Output Current (each output):
  Continuous 0.5A
  Pulse, 500ns 2.0A
Soft Start Sink Current 20mA
Clock Output Current 5mA
Error Amplifier Output Current 5mA
Oscillator Charging Current 5mA
Operating Junction Temperature:
  Hermetic (F, J, L Packages) ..... 150°C
  Plastic (DW, N Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (soldering, 10 seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage Range ..... 10V to 30V
Voltage Amp Common Mode Range ..... 1.5V to 5.5V
Ramp Input Voltage Range ..... 0V to 5.0V
Current Limit / Shutdown Voltage Range ..... 0V to 4.0V
Source / Sink Output Current
  Continuous 200mA
  Pulse, 500ns 1.0A
Voltage Reference Output Current ..... 1 mA to 10mA
Oscillator Frequency Range ..... 4KHz to 1.5MHz
Oscillator Charging Current ..... 30µA to 3mA
Oscillator Timing Resistor (R_T) ..... 1KΩ to 100KΩ
Oscillator Timing Capacitor (C_T) ..... 470pF to .01µF
Operating Ambient Temperature Range:
  SG1825 ..... -55°C to 125°C
  SG2825 ..... -25°C to 85°C
  SG3825 ..... 0°C to 70°C

Note 2. Range over which the device is functional and parameter limits are guaranteed.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1825 with -55°C ≤ T_A ≤ 125°C, SG2825 with -25°C ≤ T_A ≤ 85°C, SG3825 with 0°C ≤ T_A ≤ 70°C, and V_{IN} = V_C = 15V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1825/2825			SG3825			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Section								
Output Voltage	T_J = 25°C, I_L = 1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	V_{IN} = 10 to 30V		2	20		2	20	mV
Load Regulation	I_L = 1 to 10mA		5	20		5	20	mV
Temperature Stability (Note 3)	Over Operating Temperature		0.2	0.4		0.2	0.4	mV/°C
Total Output Range (Note 3)	Over Line, Load, and Temperature	5.00		5.20	4.95		5.25	V
Output Noise Voltage (Note 3)	f = 10Hz to 10KHz, I_L = 0mA		50	200		50		μV_{RMS}
Long Term Stability (Notes 3 & 4)	T_J = 125°C, t = 1000hrs		5	25		5	25	mV
Short Circuit Current	V_{REF} = 0V	-15	-50	-100	-15	-50	-100	mA

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1825/2825			SG3825			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Oscillator Section (Note 5)								
Initial Accuracy	T_J = 25°C, $C_{CLK} \leq$ 10pF	360	400	440	360	400	440	KHz
Voltage Stability	V_{IN} = 10 to 30V		0.2	2		0.2	2	%
Temperature Stability (Note 3)	Over Rated Operating Temperature		5	8		5	8	%
Total Frequency Limits (Note 3)	Over Line and Temperature	340		460	340		460	KHz
Minimum Frequency	R_T = 100KΩ, C_T = .01µF			4			4	KHz
Maximum Frequency	R_T = 1KΩ, C_T = 470pF	1.5			1.5			MHz
Clock High Level	I_{CLK} = -1mA	3.9	4.5		3.9	4.5		V
Clock Low Level	I_{CLK} = -1mA		2.3	2.9		2.3	2.9	V
Ramp Peak Voltage		2.6	2.8	3.0	2.6	2.8	3.0	V
Ramp Valley Voltage		0.6	0.9	1.1	0.6	0.9	1.1	V
Valley-to-Peak Amplitude		1.6	1.8	2.1	1.6	1.8	2.1	V
Error Amplifier Section (Note 6)								
Input Offset Voltage	$R_S \leq$ 2KΩ, V_{ERROR} = 2.5V			10			15	mV
Input Bias Current	V_{ERROR} = 2.5V		0.6	3		0.6	3	µA
Input Offset Current	V_{ERROR} = 2.5V		0.1	1		0.1	1	µA
DC Open Loop Gain	V_{ERROR} = 1 to 4V	60	95		60	95		dB
Common Mode Rejection	Over Rated Voltage Range, V_{ERROR} = 2.5V	75	95		75	95		dB
Power Supply Rejection	V_{IN} = 10V to 30V, V_{ERROR} = 2.5V	85	110		85	110		dB
Output Sink Current	V_{ERROR} = 1V	1	2.5		1	2.5		mA
Output Source Current	V_{ERROR} = 4V	-0.5	-1.3		-0.5	-1.3		mA
Output High Voltage	I_{ERROR} = -0.5mA	4.0	4.7	5.0	4.0	4.7	5.0	V
Output Low Voltage	I_{ERROR} = 1mA	0	0.5	1.0	0	0.5	1.0	V
Unity Gain Bandwidth (Note 3)	A_{VOL} = 0dB	3	5.5		3	5.5		MHz
Slew Rate (Note 3)	A_{VCL} = 1, V_O = 2V to 4V	6	12		6	12		V/µs
PWM Comparator Section (Note 5 & 7)								
Ramp Input Bias Current			-1	-5		-1	-5	µA
Minimum Duty Cycle	V_{ERROR} = 1V			0			0	%
Maximum Duty Cycle (Note 8)	V_{ERROR} = 4V	85			85			%
Zero Duty Cycle Threshold		1.1	1.25		1.1	1.25		V
Delay to Driver Output (Note 3)	V_{RAMP} = 0 to 2V, V_{ERROR} = 2V		80	100		80	100	ns
SoftStart Section								
C_{SS} Charge Current	$V_{SOFTSTART}$ = 0.5V	3	9	20	3	9	20	µA
C_{SS} Discharge Current	$V_{SOFTSTART}$ = 1.0V	1			1			mA
Current Limit / Shutdown Section (Note 9)								
I_{LIM} Input Bias Current				±10			±10	µA
Current Limit Threshold		0.9	1.0	1.1	0.9	1.0	1.1	V
Shutdown Threshold		1.25	1.40	1.55	1.25	1.40	1.55	V
Delay to Driver Output (Note 3)	$V_{SHUTDOWN}$ = 0V to 1.2V		80	100		80	100	ns
Output Drivers (each output)								
Output Low Level	I_{SINK} = 20mA		0.25	0.40		0.25	0.40	V
	I_{SINK} = 200mA		1.2	2.2		1.2	2.2	V
Output High Level	I_{SOURCE} = 20mA	13.0	13.5		13.0	13.5		V
	I_{SOURCE} = 200mA	12.0	13.0		12.0	13.0		V
V_C Standby Current	V_C = 30V		150	500		150	500	µA
Output Rise / Fall Time (Note 3)	C_L = 1000pF		30	60		30	60	ns
Undervoltage Lockout Section								
Start Threshold Voltage		8.8	9.2	9.6	8.8	9.2	9.6	V
UV Lockout Hysteresis		0.4	0.8	1.2	0.4	0.8	1.2	V
Supply Current Section (Note 5)								
Start Up Current	V_{IN} = 8V		1.1	2.5		1.1	2.5	mA
Operating Current	V_{INV} , V_{RAMP} , $V(I_{LIM}/S.D.)$ = 0V, $V_{N.I.}$ = 1V		22	33		22	33	mA

Note 3. This parameter is guaranteed by design and process control, but is not 100% tested in production.
Note 4. This parameter is non-accumulative, and represents the random fluctuation of the reference voltage within some error band when observed over any 1000 hour period of time.
Note 5. F_{OSC} = 400KHz (R_T = 3.65KΩ, C_T = 1.0nF)
Note 6. V_{CM} = 1.5V to 5.5V.
Note 7. V_{RAMP} = 0V, unless otherwise specified.
Note 8. 100% duty cycle is defined as a pulsewidth equal to one oscillator period.
Note 9. $V(I_{LIM}$/SHUTDOWN) = 0V to 4.0V, unless otherwise specified.

CHARACTERISTIC CURVES

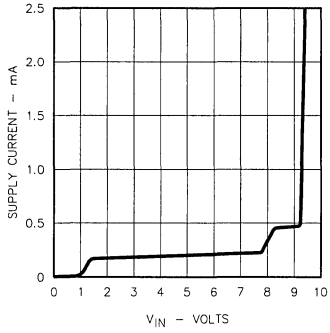


FIGURE 1.
SUPPLY CURRENT VS. V_{IN}

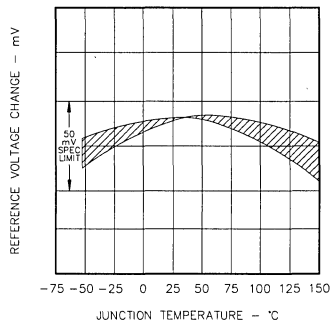


FIGURE 2.
REFERENCE TEMPERATURE STABILITY

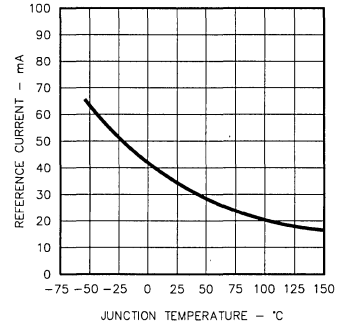


FIGURE 3.
REFERENCE SHORT CIRCUIT CURRENT

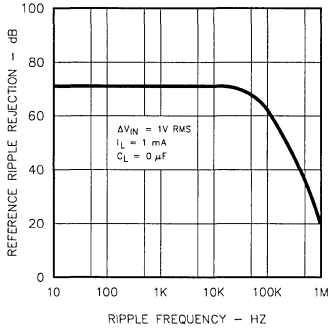


FIGURE 4.
REFERENCE RIPPLE REJECTION

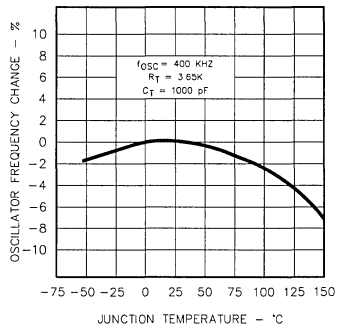


FIGURE 5.
OSCILLATOR TEMPERATURE STABILITY

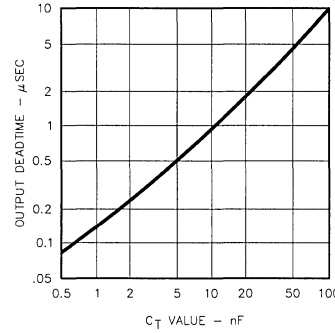


FIGURE 6.
OUTPUT DEADTIME VS. C_T VALUE

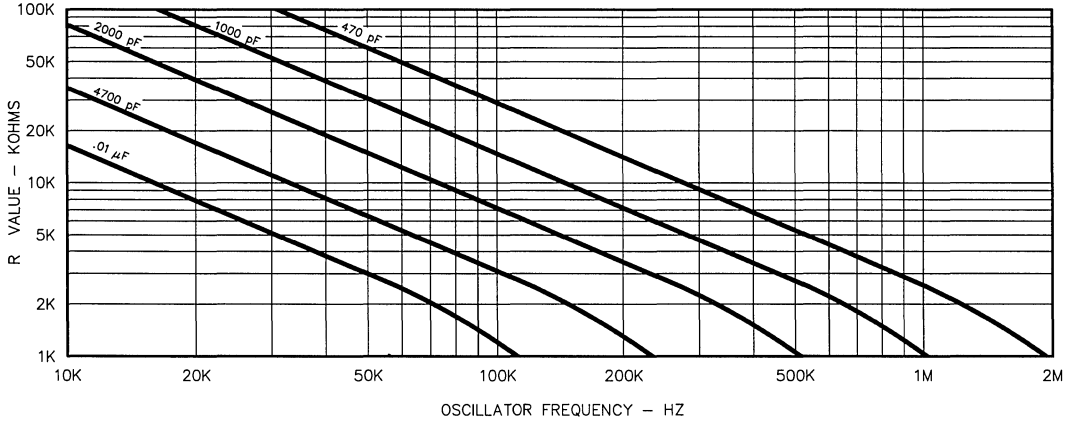


FIGURE 7.
OSCILLATOR FREQUENCY VS. R_T AND C_T

CHARACTERISTIC CURVES

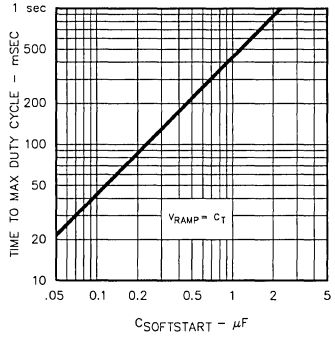


FIGURE 8.
SOFTSTART TIME VS. C_S VALUE

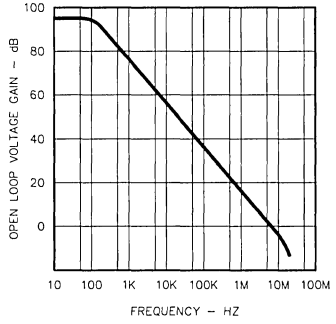


FIGURE 9.
ERROR AMP OPEN LOOP GAIN

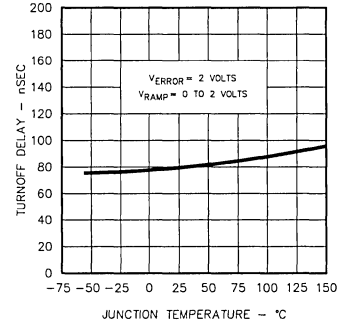


FIGURE 10.
RAMP INPUT TO DRIVER OUTPUT DELAY

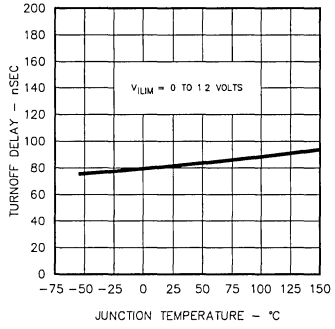


FIGURE 11.
I_{LIMIT} INPUT TO DRIVER OUTPUT DELAY

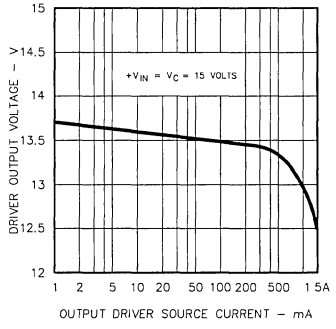


FIGURE 12.
OUTPUT DRIVER HIGH VOLTAGE VS. I_{SOURCE}

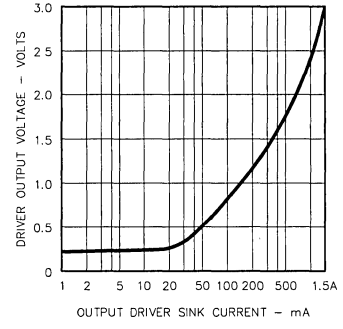


FIGURE 13.
OUTPUT DRIVER LOW VOLTAGE VS. I_{SINK}

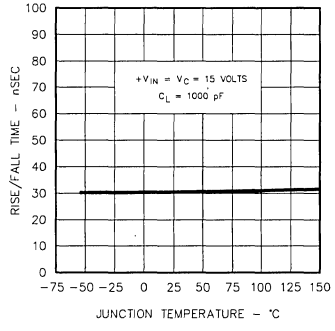


FIGURE 14.
OUTPUT RISE/FALL TIME VS. TEMPERATURE

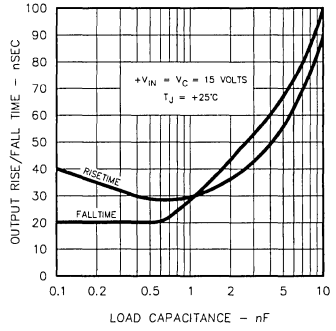


FIGURE 15.
OUTPUT RISE/FALL TIME VS. LOAD CAPACITANCE

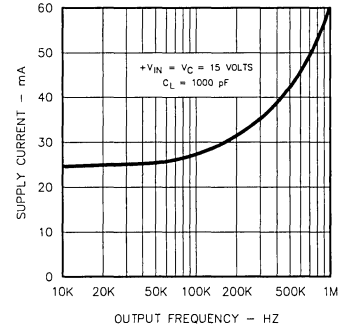


FIGURE 16.
SUPPLY CURRENT VS. OUTPUT FREQUENCY

APPLICATION INFORMATION

HIGH-SPEED LAYOUT AND BYPASSING

The SG1825, like all high-speed circuits, requires extra attention to external conductor and component layout to minimize undesired inductive and capacitive effects. All lead lengths must be as short as possible. The best printed circuit board choice would be a four-layer design, with the two internal planes supplying power and ground. Signal interconnects should be placed on the outside, giving a conductor-over-ground-plane (microstrip) configuration. A two-sided pc board with one side dedicated as a ground plane is next best, and requires careful component placement by a skilled pc designer.

Two supply bypass capacitors should be employed: a low-inductance 0.1 µF ceramic within 0.25 inches of the $+V_{IN}$ pin for high frequencies, and a 1 to 5 µF solid tantalum within 0.5 inches of the V_C pin to provide an energy reservoir for the high peak output currents. A low-inductance .01 µF bypass for the reference output is also recommended.

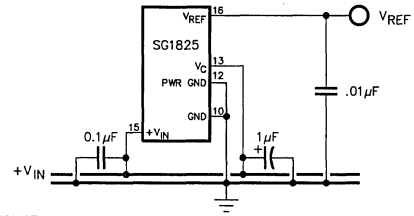


FIGURE 17.
HIGH SPEED LAYOUT AND BYPASSING

MICROPOWER STARTUP

Since the SG1825 draws less than 2.5 mA of supply current before turning on, a low power bleeder resistor from the rectified AC line supply is all that is required for startup. A start capacitor, C_S, is charged with the excess current from the bleeder resistor. When the turn-on threshold voltage is reached, the PWM circuit becomes active, energizing the power transistors. The additional operating current required by the PWM is then provided by a bootstrap winding on the main high-frequency power transformer.

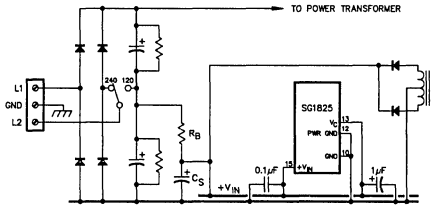


FIGURE 18.
MICROPOWER STARTUP

SOFTSTART CIRCUIT

The Softstart pin of the SG1825 is held low when either the chip is in the micropower mode, or when a voltage greater than +1.4 volts is present at the $I_{LIM/S.D.}$ pin. The maximum positive swing of the voltage error amplifier is clamped to the Softstart pin voltage, providing a ramp-up of peak charging currents in the power semiconductors at turn-on.

In some cases, the duration of the Shutdown signal can be too short to fully discharge the softstart capacitor. The illustrated resistor/discrete PNP transistor configuration can be used to shorten the discharge time by a factor of 50 or more. When the internal discharge transistor in the SG1825 turns on, current will flow through surge limit resistor R1. As the resistor drop approaches 0.6 volts, the external PNP turns on, providing a low resistance discharge path for the energy in the softstart capacitor. The capacitor will be rapidly discharged to +0.7 volts, which corresponds to zero duty cycle in the pulse width modulator.

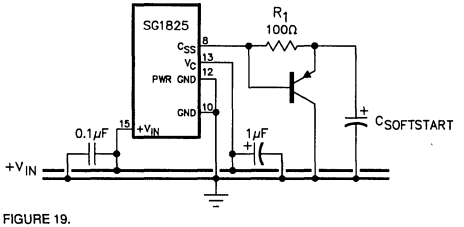


FIGURE 19.
SOFTSTART FAST RESET

FREQUENCY SYNCHRONIZATION

Two or three SG1825 oscillators may be locked together with the interconnection scheme shown, if the devices are within an inch or so of each other. A master unit is programmed for desired frequency with R_T and C_T as usual. The oscillators in the slave units are disabled by grounding C_T and by connecting R_T to V_{REF}. The logic in the slave units is locked to the clock of the master with the wire-OR connection shown.

Many SG1825s can be locked to a master system clock by wiring the oscillators as slave units, and distributing the master clock to each using a tree-fanout geometry.

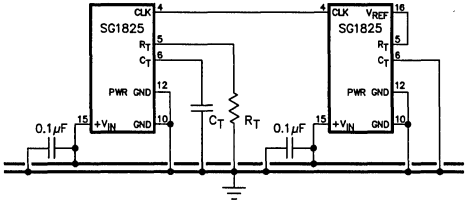


FIGURE 20.
OSCILLATOR SYNCHRONIZATION

APPLICATION INFORMATION

OSCILLATOR

The oscillator frequency is programmed by external timing components R_T and C_T. A nominal +3.0 volts appears at the R_T pin. The current flowing through R_T is mirrored internally with a 1:1 ratio. This causes an identical current to flow out the C_T pin, charging the timing capacitor and generating a linear ramp. When the upper threshold of +2.8 volts is reached, a discharge network reduces the ramp voltage to +1.0, where a new charge cycle begins.

The Clock output pin is LOW (+2.3 volts) during the charge cycle, and HIGH (+4.5 volts) during the discharge cycle. The Clock pin is driven by an NPN emitter follower, and so can be wire-ORed. Each Clock pin can drive a 1 mA load. Since the internal current-source pulldown is approximately 400 µA, the DC fan-out to other SG1825 Clock pins is at least two.

The type of capacitor selected for C_T is very important. At high frequencies, non-ideal characteristics such as effective series resistance (ESR), effective series inductance (ESL), dielectric loss and dielectric absorption all affect frequency accuracy and stability. RF capacitors such as silver mica, glass, polystyrene, or COG ceramics are recommended. Avoid high-K ceramics, which work best in DC bypass applications.

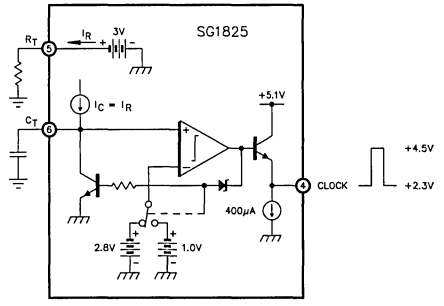


FIGURE 21.
OSCILLATOR FUNCTIONAL DIAGRAM

ERROR AMPLIFIER

The voltage error amplifier is a true operational amplifier with low-impedance output, and can be gain-stabilized using conventional feedback techniques. The typical DC open-loop gain is 95 dB, with a single low-frequency pole at 100 Hz.

The input connections to the error amplifier are determined by the polarity of the power supply output voltage. For positive supplies, the common-mode voltage is +5.1 volts and the feedback connections in Figure A are used. With negative outputs, the common-mode voltage is half the reference, and the feedback divider is connected between the negative output and the +5.1 volt reference as shown in Figure B.

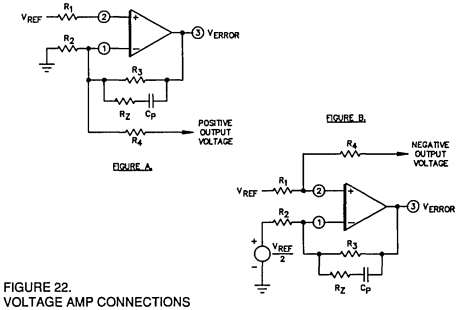


FIGURE 22.
VOLTAGE AMP CONNECTIONS

OUTPUT DRIVERS

The output drivers are designed to provide up to 1.5 Amps peak output current. To minimize ringing on the output waveform, which can be destructive to both the power MOSFET and the PWM chip, the series inductance seen by the drivers should be as low as possible.

One solution is to keep the distance between the PWM and MOSFET gate as short as possible, and to use carbon composition series damping resistors. A Faraday shield to intercept radiated EMI from the power transistors is usually required with this choice.

A second approach is to place the MOSFETs some distance from the PWM chip, and use a series-terminated transmission line to preserve drive pulse fidelity. This will minimize noise radiated back to the sensitive analog circuitry of the SG1825. A Faraday shield may also be required.

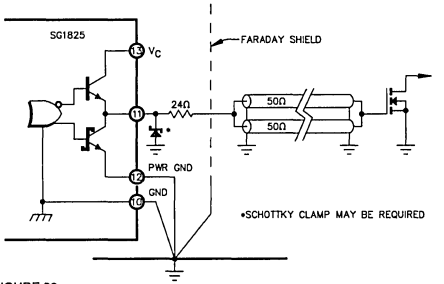
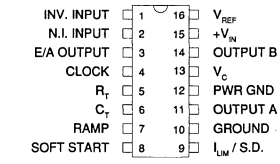
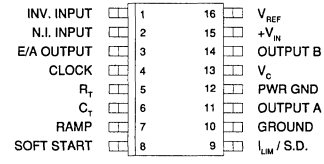
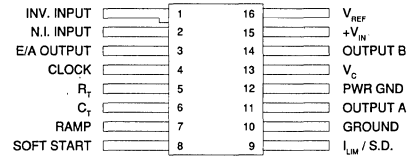
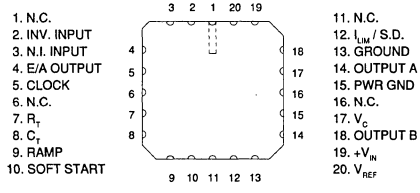
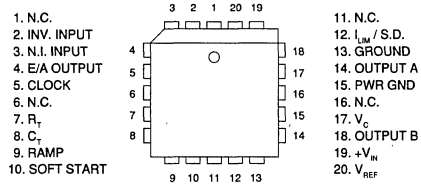


FIGURE 23.
DRIVING SHIELDED CABLE

If the drivers are connected to an isolation transformer, or if kickback through C_{GD} of the MOSFET is severe, clamp diodes may be required. 1 Amp peak Schottky diodes will limit undershoot to less than -0.3 volts.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG1825J/883B SG1825J SG2825J SG3825J	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
16-PIN PLASTIC DIP N - PACKAGE	SG2825N SG3825N	-25°C to 85°C 0°C to 70°C	
16-PIN WIDE BODY PLASTIC S.O.I.C. DW - PACKAGE	SG2825DW SG3825DW	-25°C to 85°C 0°C to 70°C	
16-PIN CERAMIC FLAT PACK F - PACKAGE (Note 3)	SG1825F/883B SG1825F	-55°C to 125°C -55°C to 125°C	
20-PIN CERAMIC LEADLESS CHIP CARRIER L- PACKAGE (Note 3)	SG1825L/883B SG1825L	-55°C to 125°C -55°C to 125°C	
20-PIN PLASTIC LEADED CHIP CARRIER Q- PACKAGE (Note 3)	SG2825Q SG3825Q	-25°C to 85°C 0°C to 70°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.
3. Contact factory for package availabiility

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

PROGRAMMABLE, OFF-LINE, PWM CONTROLLER

DESCRIPTION

Although containing most of the features required by all types of switching power supply controllers, the SG1840 family has been optimized for highly-efficient boot-strapped primary-side operation in forward or flyback power converters. Two important features for this mode are a starting circuit which requires little current from the second operation over a wide input voltage range.

In addition to startup and normal regulating PWM functions, these devices offer a built-in protection from over-voltage, under-voltage, and over-current fault conditions. This monitoring circuitry contains the added features that any fault will initiate a complete shutdown with provisions for either latch-off or automatic restart. In the latch-off mode, the controller may be started and stopped with external pulsed or steady-state commands.

Other performance features of these devices include a 1% accurate reference, provision for slow-turn-on and duty-cycle limiting, and high-speed pulse-by-pulse current limiting in addition to current fault shutdown.

The SG1840 PWM output stage includes a latch to insure only a single pulse per period and is designed to optimize the turn off of an external switching device by conducting during the "OFF" time with a capability for both high peak current and low saturation voltage. These devices are available in an 18-pin dual-in-line plastic or ceramic package.

The SG1840 is characterised for operation over the full military ambient temperature range or -55°C to 125°C. The SG2840 and SG3840 are designed for operation from -25°C to 85°C and 0°C to 70°C, respectively.

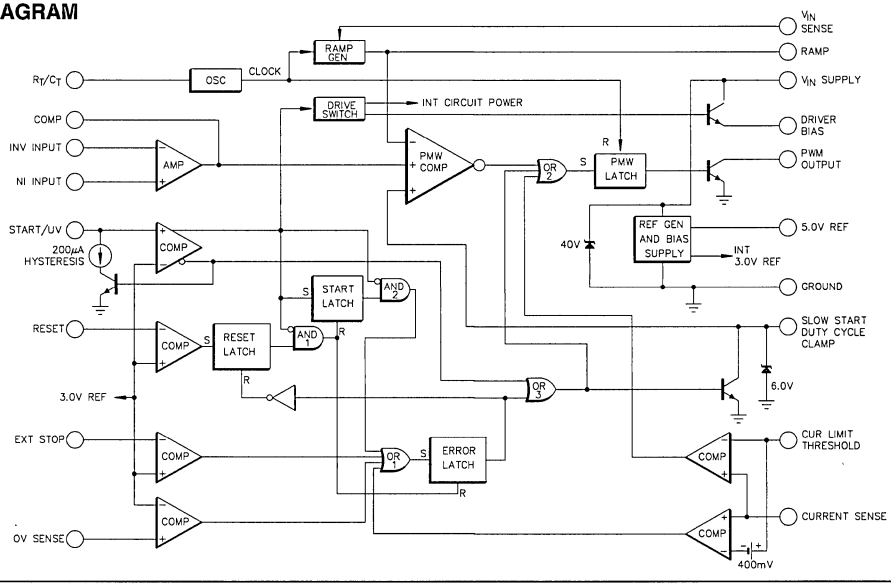
FEATURES

- **All control, driving, monitoring, and protection functions included**
- **High Frequency Initial Accuracy**
- **Low-current, Off-line start circuit**
- **Feed-forward line regulation over 4 to 1 input range**
- **PWM latch for single pulse per period**
- **Pulse-by-pulse current limiting plus shutdown for over-current fault**
- **No start-up or shutdown transients**
- **Slow turn-on and maximum duty-cycle clamp**
- **Shutdown upon over- or under-voltage sensing**
- **Latch off or continuous retry after fault**
- **Remote, pulse-commandable start/stop**
- **PWM output switch usable to 1A peak current**
- **1% reference accuracy**
- **500kHz operation**
- **70dB PSRR**
- **Linear frequency response**

HIGH RELIABILITY FEATURES-SG1840

- **Available to MIL-STD-883**
- **SG Level "S" processing available**

BLOCK DIAGRAM



April 1990

ABSOLUTE MAXIMUM RATINGS (Note 1)

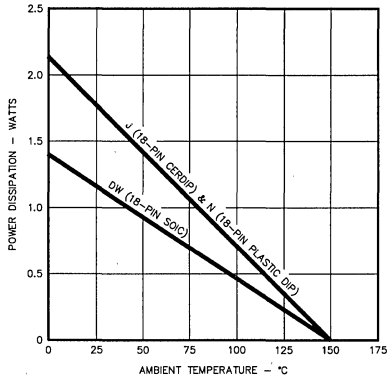
Supply Voltage (+ V_{IN})
- Voltage Driven 32V
- Current Driven (self-limiting) 100mA

PWM Output Voltage (Pin 12) 40V
PWM Output Current (continuous) 400mA
PWM Output Peak Energy Discharge ..... 20µ Joules
Driver Bias Current (Pin 14) ..... -200mA
Reference Output Current (Pin 16) ..... -50mA
Slow-start Sink Current (Pin 8)..... 20 mA
+ V_{IN} Sense Current (Pin 11) 10mA
Current Limit Inputs (Pins 6 & 7) ..... -0.5V to 5.5V
Comparator Inputs (Pins 2,3,4,5,17,18) ..... -0.3V to V_{IN}
Operating Junction Temperature
- Hermetic (J package)..... 150°C
- Plastic (N, DW packages)..... 150°C

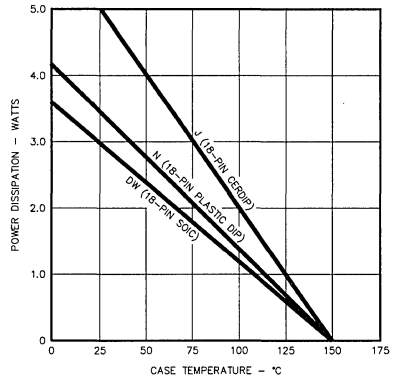
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Values beyond which damage may occur.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage Range ..... 8V to 30V
Error Amp Common Mode Range ..... 1.5V to 5.5V
PWM Output Current (continuous) ..... 0 to 200mA
Driver Bias Output Current ..... 0 to 50mA
Reference Load Current ..... 0 to 20mA
+ V_{IN} Sense Current Range ..... 10µA to 1.0mA
Ramp Generator Capacitor Range ..... 620pF to 0.1µF
Oscillator Frequency Range .....100Hz to 500KHz
Oscillator Timing Resistor (R_T) ..... 1KΩ to 100KΩ
Oscillator Timing Capacitor (C_T) ..... 620pF to 0.1µF
Operating Ambient Temperature Range:
- SG1840 ..... -55°C to 125°C
- SG2840 ..... -25°C to 85°C
- SG3840 ..... 0°C to 70°C

Note 2. Range over which the device is functional and parameter limits are guaranteed.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1840 with -55°C ≤ T_A ≤ 125°C, SG2840 with -25°C ≤ T_A ≤ 85°C, SG3840 with 0°C ≤ T_A ≤ 70°C, V_{IN} = 20V. R_T = 20KΩ, C_T = 0.001µF, C_R = 0.001µF, and Current Limit Threshhold = 200mV. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1840/2840			SG3840			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Power Inputs Section								
Start-Up Current	V_{IN} = 30V, Pin 2 = 2.5V, T_J = 25°C		5	7		5	7	mA
Start-Up Current T.C. (Note 3)	V_{IN} = 30V, Pin 2 = 2.5V		-0.1	-0.2		-0.1	-0.2	%/°C
Operating Current	V_{IN} = 30V, Pin 2 = 3.5V	5	10	15	5	10	15	mA
Supply OV Clamp	I_{IN} = 20mA	33	40	45	33	40	48	V
Reference Section								
Reference Voltage	T_J = 25°C	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation	V_{IN} = 8 to 30V		10	15		10	20	mV
Load Regulation	I_L = 0 to 20mA		10	20		10	30	mV
Temperature Coefficient (Note 3)	Over operating temperature range			±0.4			±0.4	mV/°C
Short Circuit Current	V_{REF} = 0, T_J = 25°C		-80	-100		-80	-100	mA

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1840/2840			SG3840			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Oscillator Section								
Nominal Frequency	T_J= 25°C	47	50	53	45	50	55	KHz
H.F. Initial Accuracy (Note 3)	R_T = 3KΩ, C_T = 910pF	270	300	330	270	300	330	KHz
Voltage Stability	V_{IN} = 8 to 30V		0.5	1		0.5	1	%
Temperature Coefficient (Note 3)	Over operating temperature range			±.08			±.08	%/°C
Maximum Frequency	R_T = 2KΩ, C_T = 620pF	500			500			KHz
Ramp Generator Section								
Ramp Current, Minimum	I_{SENSE} = -10µA		-11	-14		-11	-14	µA
Ramp Current, Maximum	I_{SENSE} = 1.0mA	-0.9	-0.95		-0.9	-0.95		mA
Ramp Valley		0.3	0.5		0.3	0.5		V
Ramp Peak	Clamping Level	3.9	4.2	4.5	3.9	4.2	4.5	V
Error Amplifier Section								
Input Offset Voltage	V_{CM} = 5.0V		0.5	5		2	10	mV
Input Bias Current			0.5	2		1	5	µA
Input Offset Current				0.5			0.5	µA
Open Loop Gain	ΔV_O = 1 to 3V	60	66		60	66		dB
Output Swing (Max. Output ≤ Ramp Peak - 100mV)	Minimum Total Range	0.3		3.5	0.3		3.5	V
CMRR	V_{CM} = 1.5 to 5.5V	70	80		70	80		dB
PSRR	V_{IN} = 8 to 30V	70	90		70	90		dB
Short Circuit Current	V_{COMP} = 0V		-4	-10		-4	-10	mA
Gain Bandwidth (Note 3)	T_J = 25°C, A_{VOL} = 0dB	1	2		1	2		MHz
Slew Rate (Note 3)	T_J = 25°C, A_{VCL} = 0dB		0.8			0.8		V/µs
PWM Section								
Continuous Duty Cycle Range (other than zero) (Note 3)	Minimum Total Continuous Range, Ramp Peak < 4.2V	5		95	5		95	%
Output Saturation	I_{OUT} = 20mA		0.2	0.4		0.2	0.4	V
	I_{OUT} = 200mA		1.7	2.2		1.7	2.2	V
Output Leakage	V_{OUT} = 40V		0.1	10		0.1	10	µA
Comparator Delay (Note 3)	Pin 8 to Pin 12		300	500		300	500	ns
	T_J = 25°C, R_L = 1kΩ							
Sequencing Functions Section								
Comparator Thresholds	Pins 2, 3, 4, 5	2.8	3.0	3.2	2.8	3.0	3.2	V
Input Bias Current	Pins 3, 4, 5 = 0V		-1.0	-3.0		-1.0	-3.0	µA
Start/UV Hysteresis Current	Pin 2 = 2.5V	150	200	250	150	200	250	µA
Input Leakage	Input V = 20V		0.1	10		0.1	10	µA
Driver Bias Saturation Voltage	I_B = -50mA		2	3		2	3	V
Driver Bias Leakage	V_B = 0V		-0.1	-10		-0.1	-10	µA
Slow-Start Saturation	I_S = 2mA		0.2	0.5		0.2	0.5	V
Slow-Start Leakage	V_S = 4.5V		0.1	2.0		0.1	2.0	µA
Current Control Section								
Current Limit Offset			0	5		0	10	mV
Current Shutdown Offset		370	400	430	360	400	440	mV
Input Bias Current	Pin 7 = 0V		-2	-5		-2	-5	µA
Common Mode Range (Note 3)		-0.4		3.0	-0.4		3.0	V
Current Limit Delay (Note 3)	T_J = 25°C, Pin 7 to 12, R_L = 1k		200	400		200	400	ns

Note 3. These parameters, although guaranteed over the recommended operating condition, are not 100% tested in production.

CHARACTERISTIC CURVES

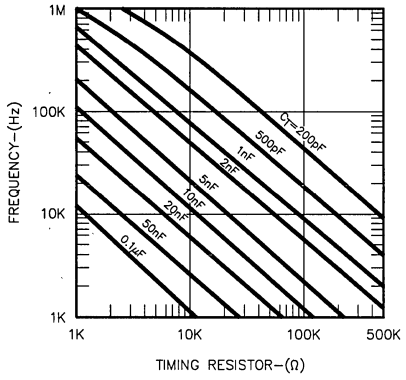


FIGURE 1.
OSCILLATOR FREQUENCY

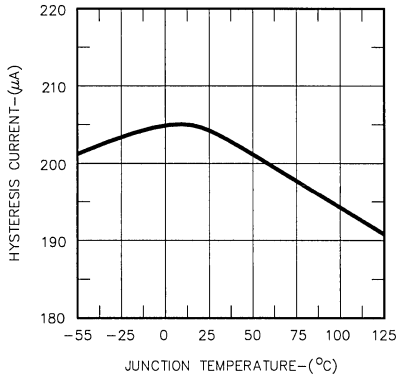


FIGURE 2.
START/U.V. HYSTERESIS CURRENT VS.
JUNCTION TEMPERATURE

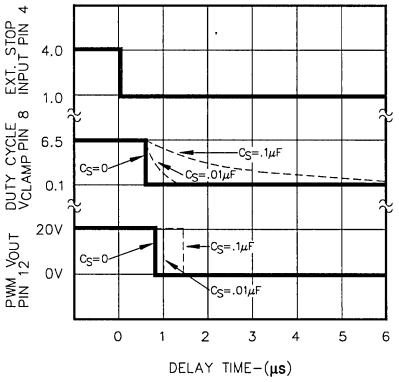


FIGURE 3.
SHUTDOWN TIMING

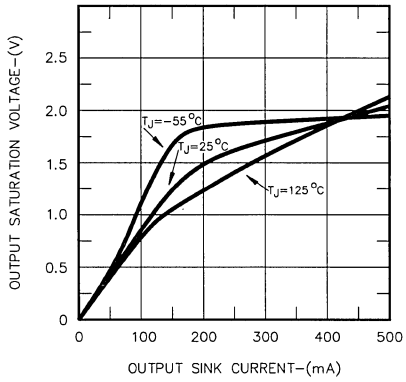


FIGURE 4.
PWM OUTPUT SATURATION VOLTAGE
VS. SINK CURRENT

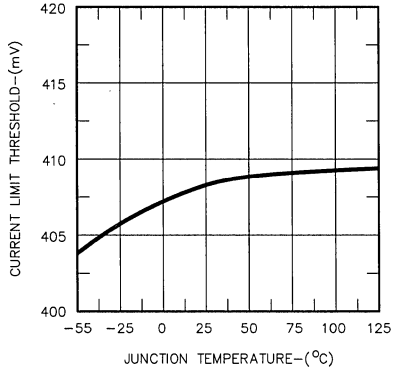
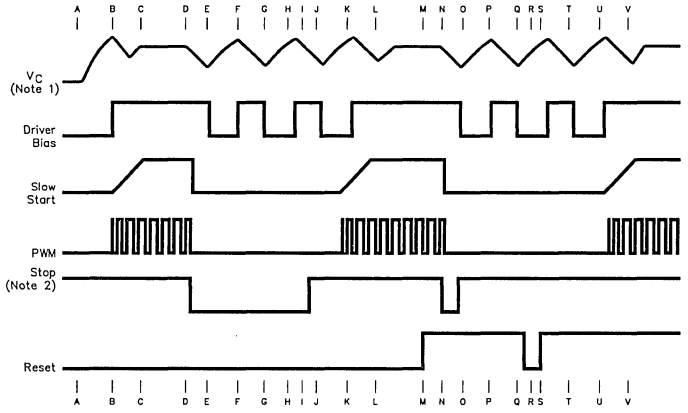


FIGURE 5.
CURRENT LIMIT VS. JUNCTION TEMPERATURE

SG1840 POWER SEQUENCING FUNCTIONS

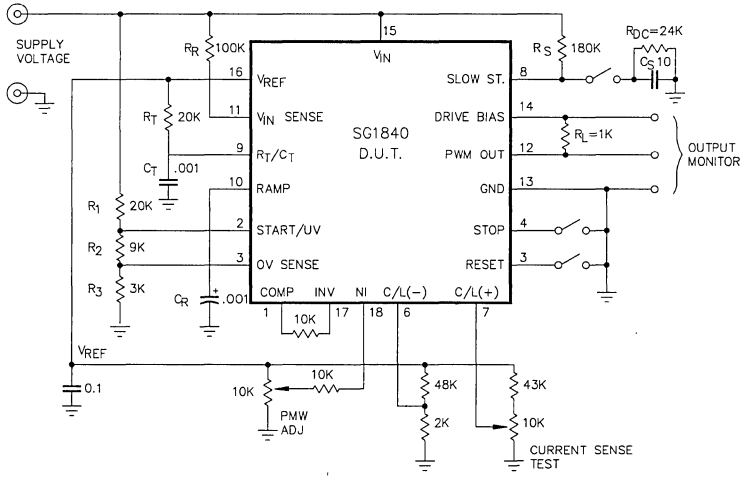


Note 1. V_C represents an analog of the output voltage generated by a primary-referenced secondary winding on the power transformer. It is the voltage monitored by the start/UV comparator and, in most cases, is the supply voltage, V_{IN}, for the SG1840.

Note 2. Although input to External Stop, Pin 4, is shown, results are the same for any fault input which sets the Error Latch.

TIME	EVENT
A	Initial turn-on. V_C rises with light load
B	Start threshold. Driver Bias Loads V_C
C	Operating PWM regulates V_C
D	Stop input sets Error Latch turning off PWM
E	UV low threshold. Error Latch remains set
F	Start turns on Driver Bias but Error Latch still set
G, H	V_C and Driver Bias continue to cycle
I	Stop command removed
J	Error Latch reset at UV low threshold
K	Start threshold now removes slow-start clamp
L	Return to normal run state
M	Reset Latch set signal removed
N	Error Latch set with momentary fault
O	Error Latch does not reset as Reset Latch is reset
P, Q	V_C and Driver Bias recycle with no turn-on
R	Reset Latch set is set with momentary Reset signal
S	V_C must complete cycle to turn-on
T	Start and Error Latches reset
U	Normal start initiated
V	Return to normal run state

OPEN LOOP TEST CIRCUIT



$$\text{Nominal Frequency} = \frac{1}{R_T C_T} = 50\text{KHz}$$

$$\text{Start Voltage} = 3\left(\frac{R_1+R_2+R_3}{R_2+R_3}\right)+0.2R_1 = 12\text{V}$$

$$\text{UV Fault Voltage} = 3\left(\frac{R_1+R_2+R_3}{R_2+R_3}\right) = 8\text{V}$$

$$\text{OV Fault Voltage} = 3\left(\frac{R_1+R_2+R_3}{R_2+R_3}\right) = 32\text{V}$$

Current Limit = 200mV

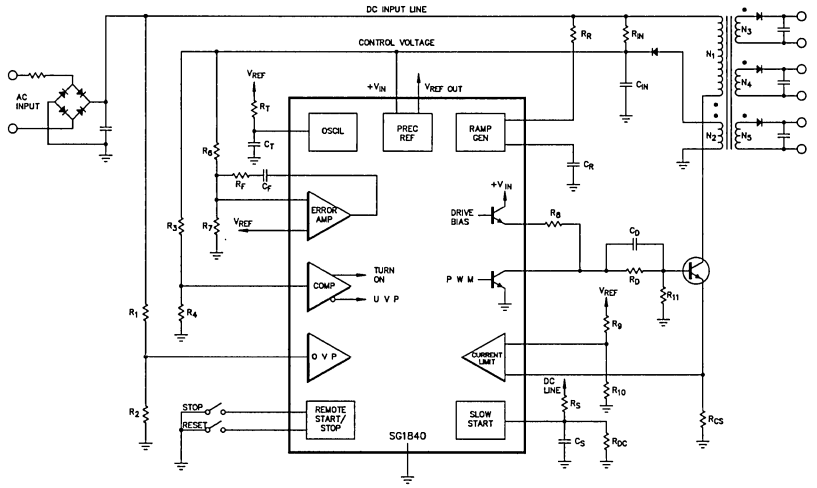
Current Fault Voltage = 600mV

Duty Cycle = 50%

FUNCTIONAL DESCRIPTION

PWM Control	
1. Oscillator	Generates a fixed-frequency internal clock from an external R_T and C_T. Frequency = $\frac{1}{R_T C_T}$
2. Ramp Generator	Develops a linear ramp with a slope defined externally by $\frac{dv}{dt} = \frac{\text{sense voltage}}{R_R C_R}$ C_R is normally selected $\leq C_R$ and its value will have some effect upon valley voltage. C_R terminal can be used as an input port for current mode control.
3. Error Amplifier	Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance; unity-gain stable.
4. Reference Generator	Precision 5.0V for internal and external usage to 50mA. Tracking 3.0V reference for internal usage only with nominal accuracy of ±2%. 40V clamp zener for chip 0V protection. 100mA maximum current.
5. PWM Comparator	Generates output pulse which starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs.
6. PWM Latch	Terminates the PWM output pulse when set by inputs from either the PWM comparator, the pulse-by-pulse current limit comparator, or the error latch. Resets with each internal clock pulse.
7. PWM Output Switch	Transistor capable of sinking current to ground which is off during the PWM on-time and turns on to terminate the power pulse. Current capacity is 400mA saturated with peak capacitance discharge in excess of one amp.
Sequencing Functions	
1. Start/UV Sense	This comparator performs three functions— With an increasing voltage, it generates a turn-on signal at a start threshold. With a decreasing voltage, it generates a UV fault signal at a lower level separated by a 200µA hysteresis current. At the UV threshold, it also resets the Error Latch if the Reset Latch has been set.
2. Drive Switch	Disables most of the chip to hold internal current consumption low, and Driver Bias OFF, until input voltage reaches start threshold.
3. Driver Bias	Supplies drive current to external power switch to provide turn-on bias.
4. Slow Start	Clamps low to hold PWM OFF. Upon release, rises with rate controlled by $R_S C_S$ for slow increase of output pulse width. Also used to clamp maximum duty cycle with divider R_S R_{DC}.
5. Start Latch	Keeps low input voltage at initial turn-on from being defined as a UV fault. Sets at start level to monitor for UV fault.
6. Reset Latch	When reset, this latch insures no reset signal to either Start or Error latches so that first fault will lock the PWM off. When set, this latch resets the Start and Error latches at the UV low threshold, allowing a restart.
Protection Functions	
1. Error Latch	When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset. Inputs to Error Latch are: a. UV low (after turn-on) b. OV high c. Stop low d. Current Sense 400mV over threshold Error Latch resets at UV threshold if Reset Latch is set.
2. Current Limiting	Differential input comparator terminates individual output pulses each time sense voltage rises above threshold. When sense voltage rises to 400mV above threshold, a shutdown signal is sent to Error Latch.

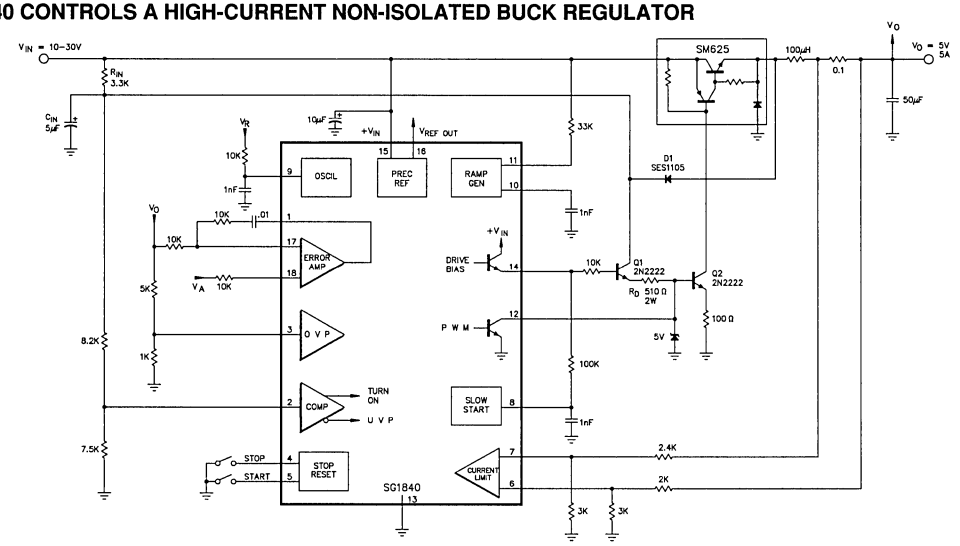
SG1840 PROGRAMMABLE PWM CONTROLLER IN A SIMPLIFIED FLYBACK REGULATOR



In this application, complete control is maintained on the primary side. Control power is provided by R_{IN} and C_{IN} during start-up, and by a primary-referenced low voltage winding, N2, for efficient operation after start. The error amplifier loop is closed to regulate the DC voltage from N2 with other outputs following through their magnetic coupling - a task made even easier with the SG1840's feed-forward line regulation.

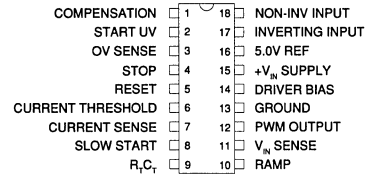
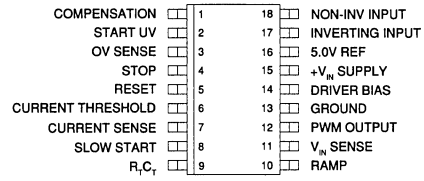
Not shown are protective snubbers or additional interface circuitry which may be required by the choice of the high-voltage switch, Qs, or the application.

SG1840 CONTROLS A HIGH-CURRENT NON-ISOLATED BUCK REGULATOR



Although primarily intended for transformer-coupled power systems, the SG1840's advantages of feed-forward for high ripple-rejection, a fully contained fault monitoring system and remote start/stop capability make it worth considering for other types of regulators. Since the fault logic within the SG1840 requires recycling the voltage sensed by the Start/UV Comparator to reset the error latch, a need for automatic restart must be addressed in a manner similar to that shown. In this simple, non-isolated, buck regulator, diode D1 provides a low-impedence bootstrapped drive power source after start-up is achieved through R_{IN} and C_{IN}. When a fault shutdown terminates switching action, the loading of Q1 and R_d will lower the voltage on pin 2 to effect an automatic re-start attempt which will continuously recycle until the fault is removed.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
18-PIN CERAMIC DIP J - PACKAGE	SG1840J/883B SG1840J SG2840J SG3840J	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
18-PIN PLASTIC DIP N - PACKAGE	SG2840N SG3840N	-25°C to 85°C 0°C to 70°C	
18-PIN WIDE BODY PLASTIC S.O.I.C. DW - PACKAGE	SG2840DW SG3840DW	-25°C to 85°C 0°C to 70°C	

Note 1. Contact factory for JAN and DESC product availibility.
2. All parts are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SG1842/2842/3842
SG1843/2843/3843

CURRENT-MODE PWM CONTROLLER

DESCRIPTION

The SG1842/43 family of control IC's provides all the necessary features to implement off-line fixed frequency, current mode switching power supplies with a minimum number of external components. Current mode architecture demonstrates improved line regulation, improved load regulation, pulse-by-pulse current limiting and inherent protection of the power supply output switch.

The bandgap reference is trimmed to ±1% over temperature. Oscillator discharge current is trimmed to less than ±10%. The SG1842/43 has under-voltage lockout, current limiting circuitry and start-up current of less than 1 mA.

The totem pole output is optimized to drive the gate of a power MOSFET. The output is low in the off state to provide direct interface to an N channel device.

The SG1842/43 is specified for operation over the full military ambient temperature range of -55°C to 125°C. The SG2842/43 is specified for the industrial range of -25°C to 85°C, and the SG3842/43 is designed for the commercial range of 0°C to 70°C.

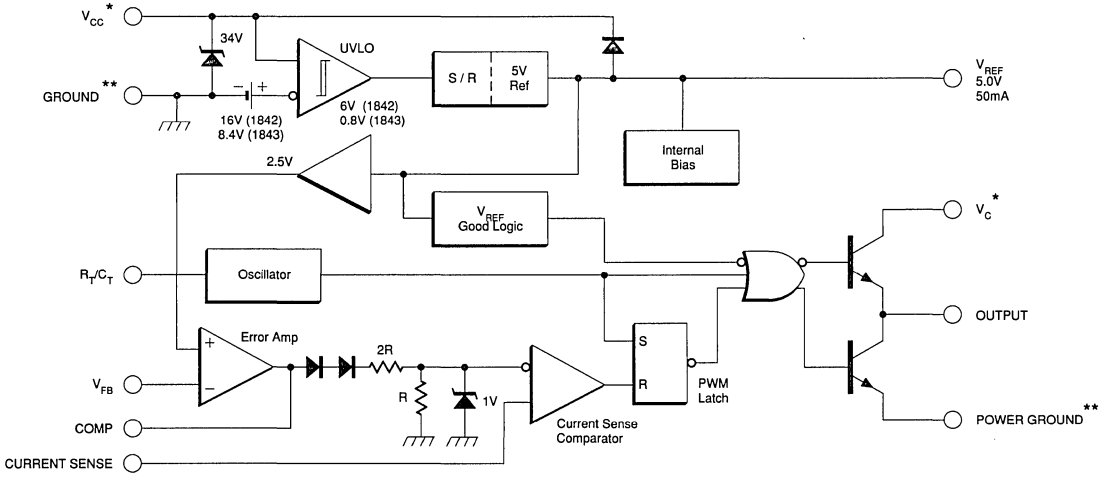
FEATURES

- **Optimized for off-line control**
- **Low start-up current (<1mA)**
- **Automatic feed forward compensation**
- **Trimmed oscillator discharge current**
- **Pulse-by-pulse current limiting**
- **Enhanced load response characteristics**
- **Under-voltage lockout with 6V hysteresis (SG1842 only)**
- **Double pulse suppression**
- **High current totem pole output (1Amp peak)**
- **Internally trimmed bandgap reference**
- **500 KHz operation**
- **Undervoltage lockout**
  SG1842 — 16 volts
  SG1843 — 8.4 volts
- **Low shoot-through current < 75mA over temperature**

HIGH RELIABILITY FEATURES - SG1842/ 1843

- **Available to MIL-STD-883 and DESC SMD**
- **Scheduled for MIL-M38510 QPL listing**
- **Radiation data available**
- **SG level "S" processing available**

BLOCK DIAGRAM



* - V_{CC} and V_C are internally connected for 8 pin packages.

** - POWER GROUND and GROUND are internally connected for 8 pin packages.

April 1990

See Application Notes for additional information.

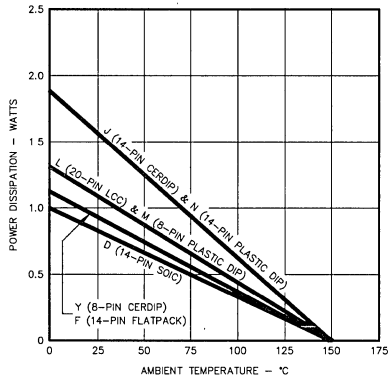
ABSOLUTE MAXIMUM RATINGS (Notes 1 & 2)

Supply Voltage (I_{CC} < 30mA) ..... Self-limiting
Supply Voltage (Low Impedence Source) 30V
Output Current (peak) ..... ±1A
Output Current (continuous) 350mA
Output Energy (Capacitive Load) 5µJ
Analog Inputs (Pin 2, Pin 3) ..... -0.3V to 6.3V

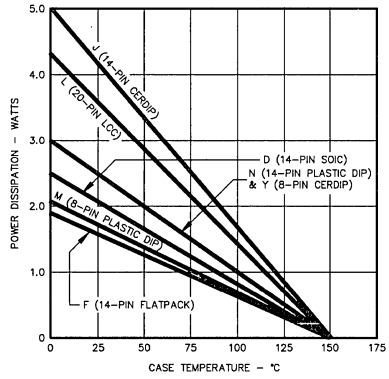
Error Amp Output Sink Current 10mA
Operating Junction Temperature
Hermetic (J, Y, F - Packages) ..... 150°C
Plastic (N, M, D - Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.
Note 2. All voltages are with respect to Pin 5. All currents are positive into the specified terminal.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 3)

Supply Voltage Range 30V
Output Current (peak) ..... ±1A
Output Current (continuous) 200mA
Analog Inputs (Pin 2, Pin 3) ..... 0V to 2.6V
Error Amp Output Sink Current 5mA
Oscillator Frequency Range ..... 100Hz to 500KHz

Oscillator Timing Resistor (R_T) ..... $520\Omega \le R_T \le 150k\Omega$
Oscillator Timing Capacitor (C_T) ..... $1000pF \le C_T \le 1\mu F$
Operating Ambient Temperature Range:
SG1842/43 ..... -55°C to 125°C
SG2842/43 ..... -25°C to 85°C
SG3842/43 ..... 0°C to 70°C

Note 3. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1842/SG1843 with $-55°C \le T_A \le 125°C$, SG2842/SG2843 with $-25°C \le T_A \le 85°C$, SG3842/SG3843 with $0°C \le T_A \le 70°C$, V_{CC} = 15V (Note 7), R_T = 10KΩ, and C_T = 3.3nF. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1842/43			SG2842/43			SG3842/43			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Section											
Output Voltage	T_J = 25°C, I_O = 1mA	4.95	5.00	5.05	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	$12V \le V_{IN} \le 25V$		6	20		6	20		6	20	mV
Load Regulation	$1 \le I_O \le 20mA$		6	25		6	25		6	25	mV
Temp. Stability (Note 4)			0.2	0.4		.02	0.4		0.2	0.4	mV/°C
Total Output Variation (Note 4)	Line, Load , Temp.	4.90		5.10	4.90		5.10	4.82		5.18	V
Output Noise Voltage (Note 4)	$10Hz \le f \le 10kHz$, T_J = 25°C		50			50			50		µV
Long Term Stability (Note 4)	T_A = 125°C, 1000 Hrs.		5	25		5	25		5	25	mV
Output Short Circuit		-30	-100	-180	-30	-100	-180	-30	-100	-180	mA
Oscillator Section											
Initial Accuracy	T_J = 25°C	47	52	57	47	52	57	47	52	57	kHz
Voltage Stability	$12 \le V_{CC} \le 25V$		.02	1		0.2	1		0.2	1	%
Temp. Stability (Note 4)	$T_{MIN} \le T_A \le T_{MAX}$		5			5			5		%
Amplitude	$V_{RT/CT}$ (peak to peak)		1.7			1.7			1.7		V
Discharge Current	T_J = 25°C	7.8	8.3	8.8	7.5	8.4	9.3	7.5	8.4	9.3	mA
	$T_{MIN} \le T_A \le T_{MAX}$	7.0		9.0	7.2		9.5	7.2		9.5	mA

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1842/43			SG2842/43			SG3842/43			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Error Amp Section											
Input Voltage	V_{COMP} = 2.5V	2.45	2.50	2.55	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current			-0.3	-1		-0.3	1		-0.3	-2	µA
Open Loop Gain (A_{VOL})	$2 \le V_O \le 4V$	65	90		65	90		65	90		dB
Unity Gain Bandwidth (Note 4)		0.7	1		0.7	1		0.7	1		MHz
PSRR	$12 \le V_{CC} \le 25V$	60	70		60	70		60	70		dB
Output Sink Current	V_{VFB} = 2.7V, V_{COMP} = 1.1V	2	6		2	6		2	6		mA
Output Source Current	V_{VFB} = 2.3V, V_{COMP} = 5V	-0.5	-0.8		-0.5	-0.8		-0.5	-0.8		mA
V_{OUT} High	V_{VFB} = 2.3V, R_L = 15K to gnd	5	6		5	6		5	6		V
V_{OUT} Low	V_{VFB} = 2.7V, R_L = 15K to V_{REF}		0.7	1.1		0.7	1.1		0.7	1.1	V
Current Sense Section											
Gain (Notes 5 & 6)		2.85	3	3.15	2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal (Note 5)	V_{COMP} = 5V	0.9	1	1.1	0.9	1	1.1	0.9	1	1.1	V
PSRR (Note 5)	$12 \le V_{CC} \le 25V$		70			70			70		dB
Input Bias Current			-2	-10		-2	-10		-2	-10	µA
Delay to Output (Note 4)			150	300		150	300		150	300	ns
Output Section											
Output Low Level	I_{SINK} = 20mA		0.1	0.4		0.1	0.4		0.1	0.4	V
	I_{SINK} = 200mA		1.5	2.2		1.5	2.2		1.5	2.2	V
Output High Level	I_{SOURCE} = 20mA	13	13.5		13	13.5		13	13.5		V
	I_{SOURCE} = 200mA	12	13.5		12	13.5		12	13.5		V
Rise Time	T_J = 25°C, C_L = 1nF		50	150		50	150		50	150	ns
Fall Time	T_J = 25°C, C_L = 1nF		50	150		50	150		50	150	ns
Under-Voltage Lockout Section											
Start Threshold (1842)		15	16	17	15	16	17	14.5	16	17.5	V
Min. Operating Voltage (1842)	After Turn On	9	10	11	9	10	11	8.5	10	11.5	V
Start Threshold (1843)		7.8	8.4	9.0	7.8	8.4	9.0	7.8	8.4	9.0	V
Min. Operating Voltage (1843)	After Turn On	7.0	7.6	8.2	7.0	7.6	8.2	7.0	7.6	8.2	V
PWM Section											
Max. Duty Cycle		93	95	100	90	95	100	90	95	100	%
Min. Duty Cycle				0			0			0	%
Power Consumption Section											
Start-Up Current			0.5	1		0.5	1		0.5	1	mA
Operating Supply Current	V_{VFB} = V_{ISENSE} = 0V		11	17		11	17		11	17	mA
V_{CC} Zener Voltage	I_{CC} = 25mA		34			34			34		V

Notes: 4. These parameters, although guaranteed, are not 100% tested in production.

5. Parameter measured at trip point of latch with V_{VFB} = 0.

6. Gain defined as: $A = \frac{\Delta V_{COMP}}{\Delta V_{ISENSE}}$; $0 \le V_{ISENSE} \le 0.8V$.

7. Adjust V_{CC} above the start threshold before setting at 15V.

CHARACTERISTIC CURVES

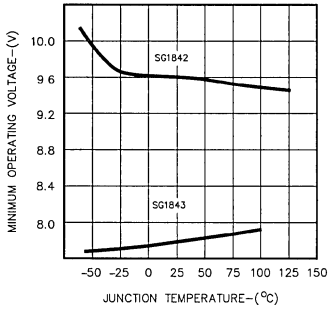


FIGURE 1.
DROPOUT VOLTAGE VS. TEMPERATURE

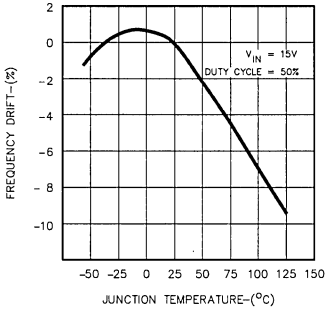


FIGURE 2.
OSCILLATOR TEMPERATURE STABILITY

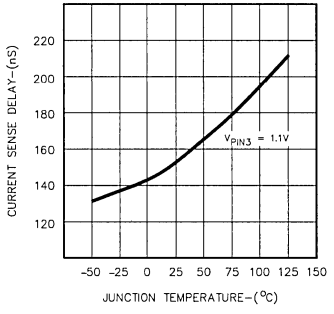


FIGURE 3.
CURRENT SENSE TO OUTPUT DELAY VS. TEMP.

CHARACTERISTIC CURVES (continued)

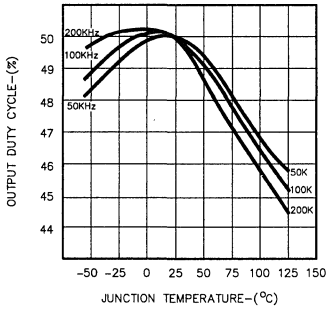


FIGURE 4.
OUTPUT DUTY CYCLE VS. TEMPERATURE

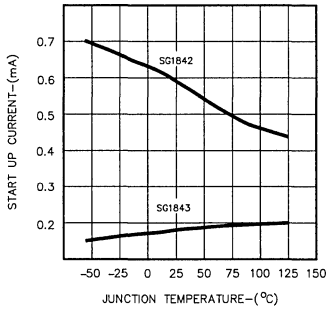


FIGURE 5.
START-UP CURRENT VS. TEMPERATURE

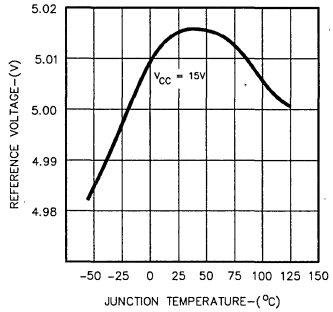


FIGURE 6.
REFERENCE VOLTAGE VS. TEMPERATURE

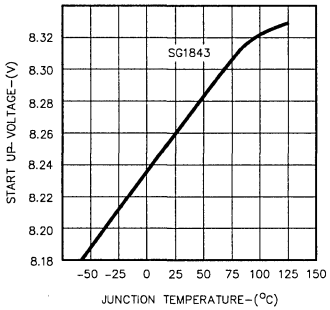


FIGURE 7.
START-UP VOLTAGE THRESHOLD
VS. TEMPERATURE

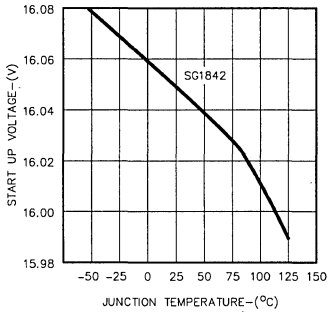


FIGURE 8.
START-UP VOLTAGE THRESHOLD
VS. TEMPERATURE

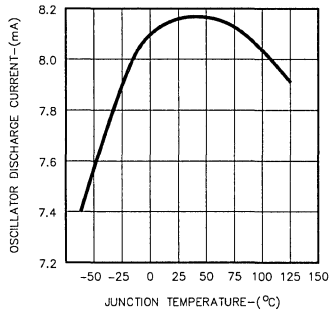


FIGURE 9.
OSCILLATOR DISCHARGE CURRENT
VS. TEMPERATURE

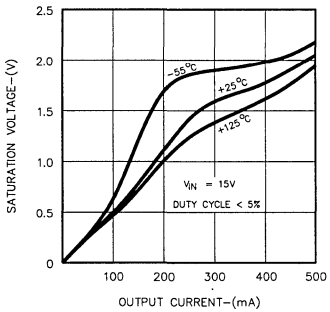


FIGURE 10.
OUTPUT SATURATION VOLTAGE VS. OUTPUT
CURRENT AND TEMPERATURE
(SINK TRANSISTOR)

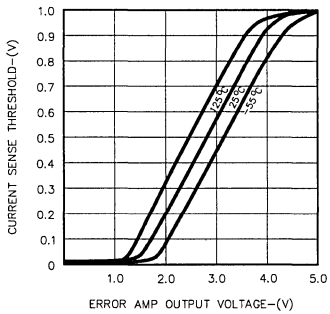


FIGURE 11.
CURRENT SENSE THRESHOLD VS. ERROR
AMPLIFIER OUTPUT

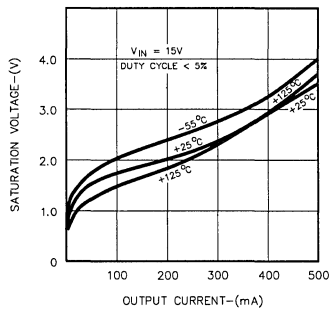


FIGURE 12.
OUTPUT SATURATION VOLTAGE VS. OUTPUT
CURRENT AND TEMPERATURE
(SOURCE TRANSISTOR)

APPLICATION INFORMATION

OSCILLATOR:

The oscillator of the 1842/43 family of PWM's is designed such that many values of R_T & C_T will give the same oscillator frequency, but only one combination will yield a specific duty cycle at a given frequency.

A set of formulas are given to determine the values of R_T & C_T for a given frequency and maximum duty cycle. (Note: These formulas are less accurate for smaller duty cycles or higher frequencies. This will require trimming of R_T or C_T to correct for this error.)

GIVEN: Frequency ≡ f
Maximum Duty Cycle ≡ D_m

CALCULATE:

$$R_T = 267 \left[\frac{(1.76)^{1/D_m} - 1}{(1.76)^{(1-D_m)/D_m} - 1} \right] \quad (\Omega)$$

where $.3 < D_m < .95$

$$C_T = \frac{1.86 \times D_m}{f \times R_T} \quad (\mu F)$$

EXAMPLE:

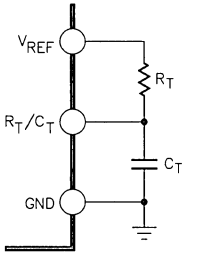
A Flyback power supply requires a maximum of 45% duty-cycle at a switching frequency of 50KHz. What are the values of R_T and C_T?

GIVEN: f = 50KHz
$D_m = 0.45$

CALCULATE: $R_T = 267 \left[\frac{(1.76)^{1/.045} - 1}{(1.76)^{.55/.45} - 1} \right] = 674\Omega$

$$C_T = \frac{1.86 \times .45}{50000 \times 674} = .025\mu F$$

For Duty-Cycles above 95% use:



$$F \approx \frac{1.86}{R_T C_T} \quad \text{WHERE } R_T \geq 5K\Omega$$

FIGURE 13 — OSCILLATOR TIMING CIRCUIT

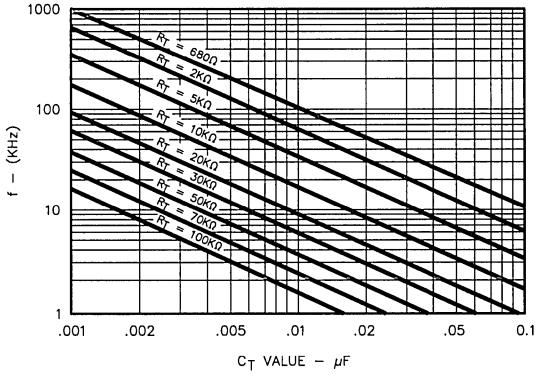


FIGURE 14 — OSCILLATOR FREQUENCY VS. R_T FOR VARIOUS C_T

APPLICATION CIRCUITS (Note 8)

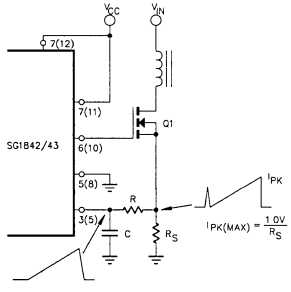


FIGURE 15 — CURRENT SENSE SPIKE SUPPRESSION

The RC low pass filter will eliminate the leading edge current spike caused by parasitics of Power MOSFET.

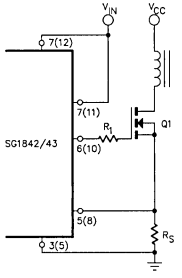


FIGURE 16 — MOSFET PARASITIC OSCILLATIONS

A resistor (R_1) in series with the MOSFET gate will reduce overshoot & ringing caused by the MOSFET input capacitance and any inductance in series with the gate drive. (Note: It is very important to have a low inductance ground path to insure correct operation of the I.C. This can be done by making the ground paths as short and as wide as possible.)

APPLICATION CIRCUITS (continued)

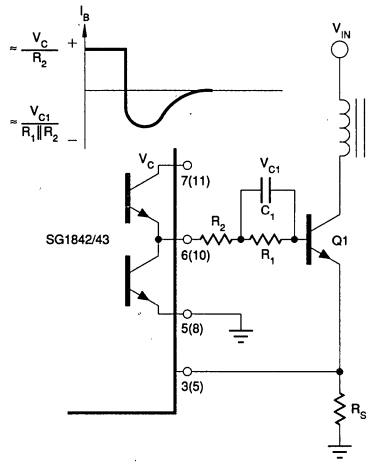


FIGURE 17 — BIPOLAR TRANSISTOR DRIVE

The 1842/43 output stage can provide negative base current to remove base charge of power transistor (Q_1) for faster turn off. This is accomplished by adding a capacitor (C_1) in parallel with a resistor (R_1). The resistor (R_1) is to limit the base current during turn on.

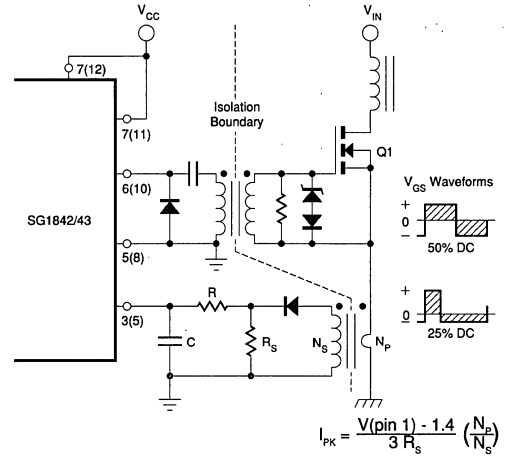


FIGURE 18 — ISOLATED MOSFET DRIVE

Current transformers can be used where isolation is required between PWM and Primary ground. A drive transformer is then necessary to interface the PWM output with the MOSFET.

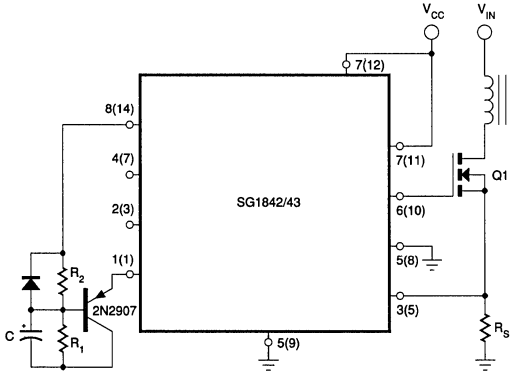


FIGURE 19 — ADJUSTABLE BUFFERED REDUCTION OF CLAMP LEVEL WITH SOFT-START

Soft start and adjustable peak current can be done with the external circuitry shown above.

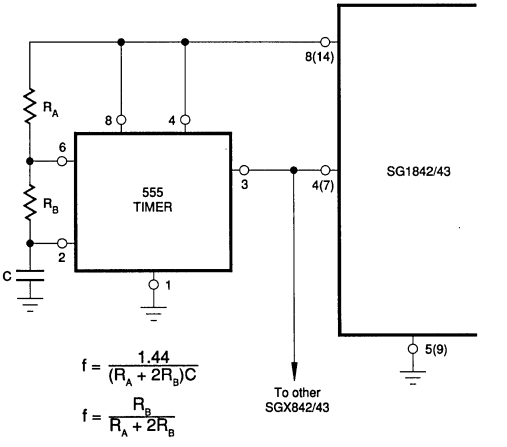


FIGURE 20 — EXTERNAL DUTY CYCLE CLAMP AND MULTI-UNIT SYNCHRONIZATION

Precision duty cycle limiting as well as synchronizing several 1842/43's is possible with the above circuitry.

APPLICATION CIRCUITS (continued)

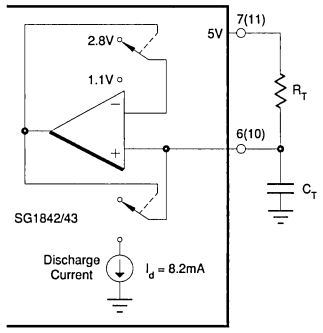


FIGURE 21 — OSCILLATOR CONNECTION

The oscillator is programmed by the values selected for the timing components R_T and C_T. Refer to application information for calculation of the component values.

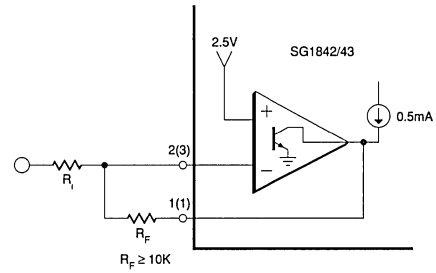


FIGURE 22 — ERROR AMPLIFIER CONNECTION

Error amplifier is capable of sourcing and sinking current up to 0.5mA.

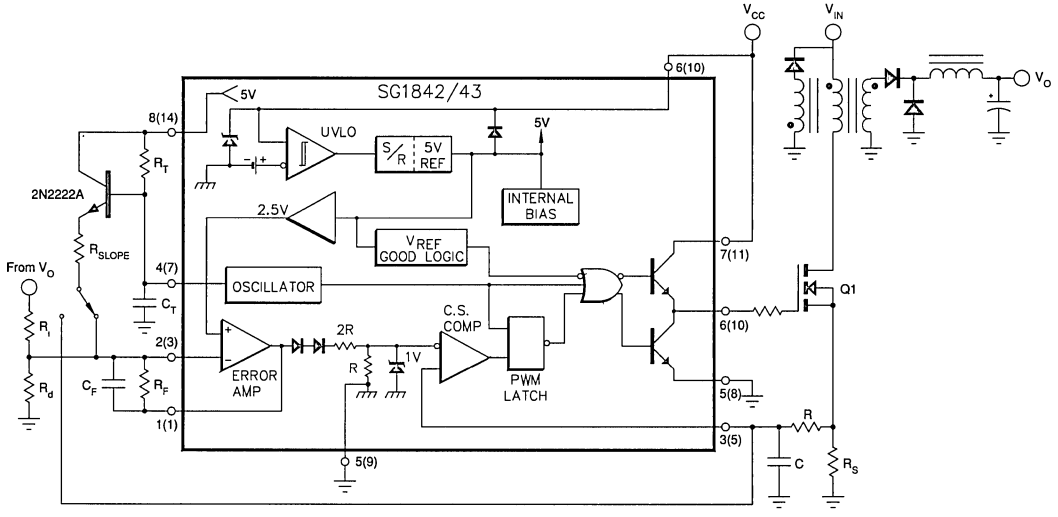


FIGURE 23 — SLOPE COMPENSATION

Due to inherent instability of current mode converters running above 50% duty cycle, a slope compensation should be added to either current sense pin or the error amplifier. Figure 23 shows a typical slope compensation technique.

APPLICATION CIRCUITS (continued)

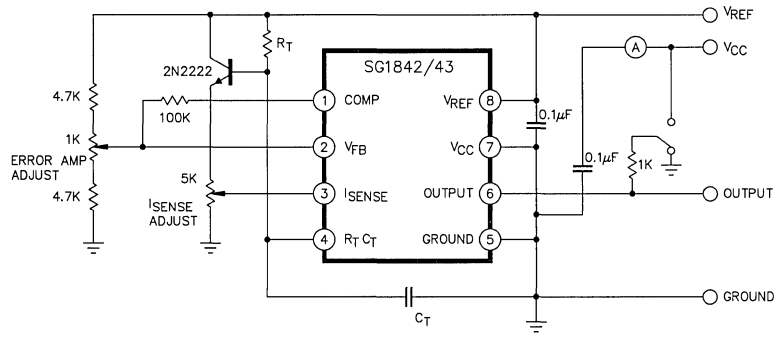


FIGURE 24 — OPEN LOOP LABORATORY FIXTURE

High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and ypass capacitors should be connected to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

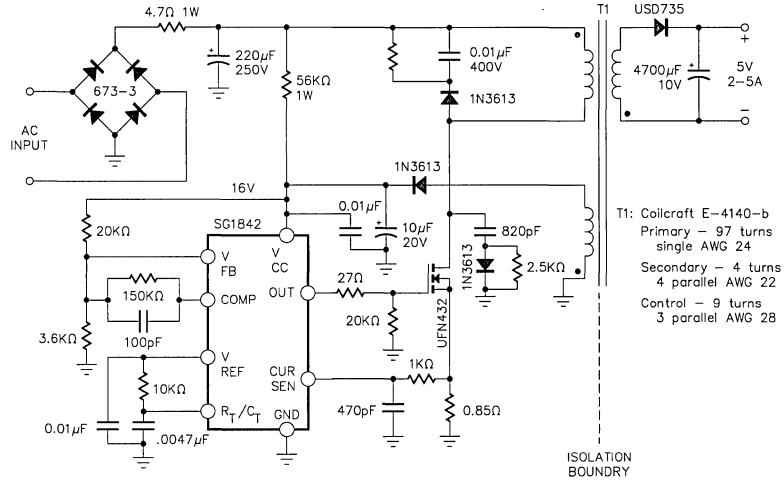


FIGURE 25 — OFF-LINE FLYBACK REGULATOR

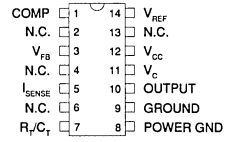
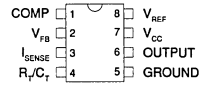
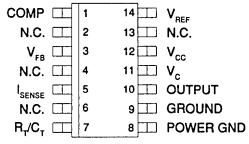
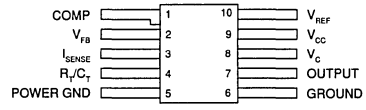
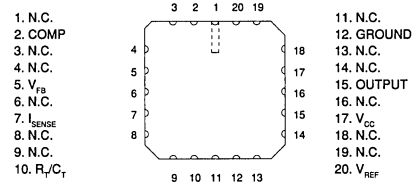
SPECIFICATIONS

Input line voltage:	90VAC to 130VAC
Input frequency:	50 or 60Hz
Switching frequency:	40KHz ±10%
Output power:	25W maximum
Output voltage:	5V +5%
Output current:	2 to 5A
Line regulation:	0.01%/V
Load regulation:	8%/A*
Efficiency @ 25 Watts,	
V_{IN} = 90VAC:	70%
V_{IN} = 130VAC:	65%
Output short-circuit current:	2.5Amp average

* This circuit uses a low-cost feedback scheme in which the DC voltage developed from the primary-side control winding is sensed by the SG1842 error amplifier. Load regulation is therefore dependent on the coupling between secondary and control windings, and on transformer leakage inductance.

Note 8. Pin numbers referenced are for 8 pin package and pin numbers in parenthesis are for 14 pin packages.

CONNECTION DIAGRAM & ORDERING INFORMATION (See notes below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN CERAMIC DIP J - PACKAGE	SG1842J/883B SG1842J SG2842J SG3842J SG1843J/883B SG1843J SG2843J SG3843J	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C -55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
14-PIN PLASTIC DIP N - PACKAGE	SG2842N SG3842N SG2843N SG3843N	-25°C to 85°C 0°C to 70°C -25°C to 85°C 0°C to 70°C	
8-PIN CERAMIC DIP Y - PACKAGE	SG1842Y/883B SG1842Y SG2842Y SG3842Y SG1843Y/883B SG1843Y SG2843Y SG3843Y	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C -55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
8-PIN PLASTIC DIP M - PACKAGE	SG2842M SG3842M SG2843M SG3843M	-25°C to 85°C 0°C to 70°C -25°C to 85°C 0°C to 70°C	
14-PIN PLASTIC S.O.I.C. D - PACKAGE	SG2842D SG3842D SG2843D SG3843D	-25°C to 85°C 0°C to 70°C -25°C to 85°C 0°C to 70°C	
10-PIN CERAMIC FLAT PACK F - PACKAGE	SG1842F/883B SG1842F SG1843F/883B SG1843F	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C	
20-PIN CERAMIC LEADLESS CHIP CARRIER L- PACKAGE	SG1842L/883B SG1842L SG1843L/883B SG1843L	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availability.
2. All packages are viewed from the top.

SG1844/2844/3844
SG1845/2845/3845

CURRENT-MODE PWM CONTROLLER

DESCRIPTION

The SG1844/45 family of control IC's provides all the necessary features to implement off-line fixed frequency, current mode switching power supplies with a minimum number of external components. Current mode architecture demonstrates improved line regulation, improved load regulation, pulse-by-pulse current limiting and inherent protection of the power supply output switch.

The bandgap reference is trimmed to ±1% over temperature. Oscillator discharge current is trimmed to less than ±10%. The SG1844/45 has undervoltage lockout, current limiting circuitry and start-up current of less than 1 mA.

The totem pole output is optimized to drive the gate of a power MOSFET. The output is low in the off state to provide direct interface to an N channel device.

Both operate up to a maximum duty cycle range of zero to < 50% due to an internal toggle flip flop which blanks the output off every other clock cycle.

The SG1844/45 is specified for operation over the full military ambient temperature range of -55°C to 125°C. The SG2844/45 is specified for the industrial range of -25°C to 85°C, and the SG3844/45 is designed for the commercial range of 0°C to 70°C.

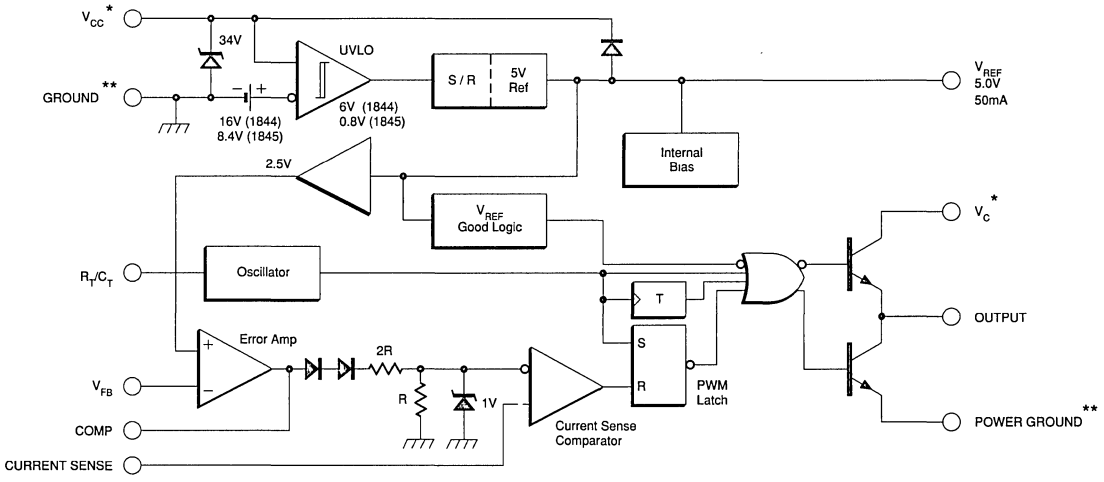
FEATURES

- **Optimized for off-line control**
- **Low start-up current (<1mA)**
- **Automatic feed forward compensation**
- **Trimmed oscillator discharge current**
- **Pulse-by-pulse current limiting**
- **Enhanced load response characteristics**
- **Under-voltage lockout with 6V hysteresis (SG1844 only)**
- **Double pulse suppression**
- **High current totem pole output**
- **Internally trimmed bandgap reference**
- **500KHz operation**
- **Undervoltage lockout**
  SG1844 — 16 volts
  SG1845 — 8.4 volts
- **Low shoot-through current < 75mA over temperature**

HIGH RELIABILITY FEATURES - SG1844/SG1845

- **Available to MIL-STD-883**
- **SG level "S" processing available**

BLOCK DIAGRAM



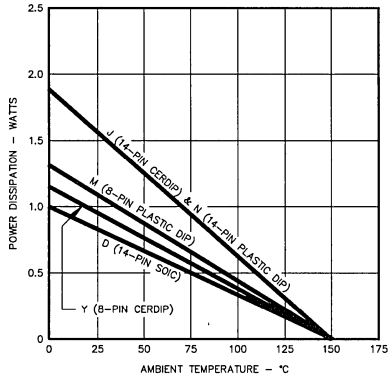
* - V_{CC} and V_C are internally connected for 8 pin packages.
** - POWER GROUND and GROUND are internally connected for 8 pin packages.

ABSOLUTE MAXIMUM RATINGS (Note 1 & 2)

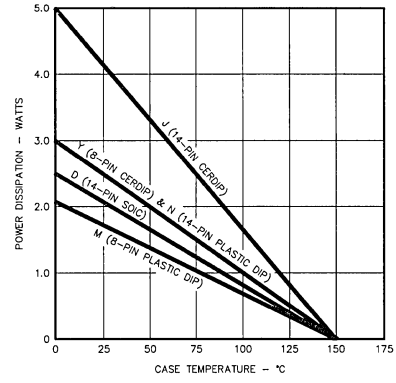
Supply Voltage (I_{CC} < 30mA) ..... Self-limiting
Supply Voltage (Low Impedence Source) 30V
Output Current (peak) ..... ±1A
Output Current (continuous) 350mA
Output Energy (Capacitive Load) 5µJ
Analog Inputs (Pin 2, Pin 3) ..... -0.3V to 6.3V
Error Amp Output Sink Current 10mA
Operating Junction Temperature
Hermetic (J, Y Packages) ..... 150°C
Plastic (N, M, D Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Values beyond which damage may occur.
Note 2. All voltages are with respect to Pin 5. All currents are positive into the specified terminal.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage Range 30V
Output Current (peak) ..... ±1A
Output Current (continuous) 200mA
Analog Inputs (Pin 2, Pin 3) ..... 0V to 2.6V
Error Amp Output Sink Current 5mA
Oscillator Frequency Range ..... 100Hz to 500KHz
Oscillator Timing Resistor (R_T) ..... $520\Omega \le R_T \le 150k\Omega$
Oscillator Timing Capacitor (C_T) ..... $1000pF \le C_T \le 1\mu F$
Operating Ambient Temperature Range:
SG1844/45 ..... -55°C to 125°C
SG2844/45 ..... -25°C to 85°C
SG3844/45 ..... 0°C to 70°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1844/SG1845 with $-55°C \le T_A \le 125°C$, SG2844/SG2845 with $-25°C \le T_A \le 85°C$, SG3844/SG3845 with $0°C \le T_A \le 70°C$, V_{CC} = 15V (Note 6), R_T = 10KΩ, and C_T = 3.3nF. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1844/45			SG2844/45			SG3844/45			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Section											
Output Voltage	T_J = 25°C, I_O = 1mA	4.95	5.00	5.05	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	$12 \le V_{IN} \le 25V$		6	20		6	20		6	20	mV
Load Regulation	$1 \le I_O \le 20mA$		6	25		6	25		6	25	mV
Temp. Stability (Note 3)			0.2	0.4		.02	0.4		0.2	0.4	mV/°C
Total Output Variation (Note 3)	Line, Load , Temp.	4.90		5.10	4.90		5.10	4.82		5.18	V
Output Noise Voltage (Note 3)	10Hz ≤ f ≤ 10kHz, T_j = 25°C		50			50			50		µV
Long Term Stability (Note 3)	T_A = 125°C, 1000 Hrs.		5	25		5	25		5	25	mV
Output Short Circuit		-30	-100	-180	-30	-100	-180	-30	-100	-180	mA
Oscillator Section											
Initial Accuracy (Note 7)	T_J = 25°C	47	52	57	47	52	57	47	52	57	kHz
Voltage Stability	$12V \le V_{CC} \le 25V$		.02	1		0.2	1		0.2	1	%
Temp. Stability (Note 3)	$T_{MIN} \le T_A \le T_{MAX}$		5			5			5		%
Amplitude	$V_{RT/CT}$ (peak to peak)		1.7			1.7			1.7		V
Discharge Current	T_J = 25°C	7.8	8.3	9.1	7.5	8.4	9.3	7.5	8.4	9.3	mA
	$T_{MIN} < T_A < T_{MAX}$	6.8		9.3	7.2		9.5	7.2		9.5	mA

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1844/45			SG2844/45			SG3844/45			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Error Amp Section											
Input Voltage	V_{COMP} = 2.5V	2.45	2.50	2.55	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current			-0.3	-1		-0.3	1		-0.3	-2	µA
Open Loop Gain (A_{VOL})	$2 \le V_O \le 4V$	65	90		65	90		65	90		dB
Unity Gain Bandwidth (Note 3)		0.7	1		0.7	1		0.7	1		MHz
PSRR	$12 \le V_{CC} \le 25V$	60	70		60	70		60	70		dB
Output Sink Current	V_{VFB} = 2.7V, V_{COMP} = 1.1V	2	6		2	6		2	6		mA
Output Source Current	V_{VFB} = 2.3V, V_{COMP} = 5V	-0.5	-0.8		-0.5	-0.8		-0.5	-0.8		mA
V_{OUT} High	V_{VFB} = 2.3V, R_L = 15K to gnd	5	6		5	6		5	6		V
V_{OUT} Low	V_{VFB} = 2.7V, R_L = 15K to V_{REF}		0.7	1.1		0.7	1.1		0.7	1.1	V
Current Sense Section											
Gain (Notes 4 & 5)		2.85	3	3.15	2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal (Note 4)	V_{COMP} = 5V	0.9	1	1.1	0.9	1	1.1	0.9	1	1.1	V
PSRR (Note 4)	$12V \le V_{CC} \le 25V$		70			70			70		dB
Input Bias Current			-2	-10		-2	-10		-2	-10	µA
Delay to Output (Note 3)			150	300		150	300		150	300	ns
Output Section											
Output Low Level	I_{SINK} = 20mA		0.1	0.4		0.1	0.4		0.1	0.4	V
	I_{SINK} = 200mA		1.5	2.2		1.5	2.2		1.5	2.2	V
Output High Level	I_{SOURCE} = 20mA	13	13.5		13	13.5		13	13.5		V
	I_{SOURCE} = 200mA	12	13.5		12	13.5		12	13.5		V
Rise Time (Note 3)	T_J = 25°C, C_L = 1nF		50	150		50	150		50	150	ns
Fall Time (Note 3)	T_J = 25°C, C_L = 1nF		50	150		50	150		50	150	ns
Under-Voltage Lockout Section											
Start Threshold (1844)		15	16	17	15	16	17	14.5	16	17.5	V
Min. Operating Voltage (1844)	After Turn On	9	10	11	9	10	11	8.5	10	11.5	V
Start Threshold (1845)		7.8	8.4	9.0	7.8	8.4	9.0	7.8	8.4	9.0	V
Min. Operating Voltage (1845)	After Turn On	7.0	7.6	8.2	7.0	7.6	8.2	7.0	7.6	8.2	V
PWM Section											
Max. Duty Cycle		46	48	50	46	48	50	46	48	50	%
Min. Duty Cycle				0			0			0	%
Power Consumption Section											
Start-Up Current			0.5	1		0.5	1		0.5	1	mA
Operating Supply Current	V_{VFB} = V_{ISENSE} = 0V		11	17		11	17		11	17	mA
V_{CC} Zener Voltage	I_{CC} = 25mA		34			34			34		V

Notes: 3. These parameters, although guaranteed, are not 100% tested in production.

4. Parameter measured at trip point of latch with V_{VFB} = 0.

5. Gain defined as: $A = \frac{\Delta V_{COMP}}{\Delta V_{ISENSE}}$; $0 \le V_{ISENSE} \le 0.8V$.

6. Adjust V_{CC} above the start threshold before setting at 15V.

7. Output frequency equals one half of oscillator frequency.

CHARACTERISTIC CURVES

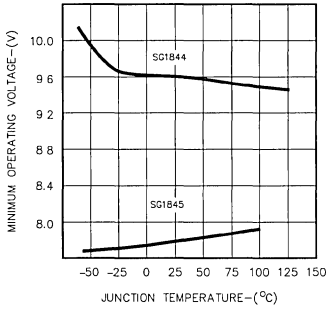


FIGURE 1.
DROPOUT VOLTAGE VS. TEMPERATURE

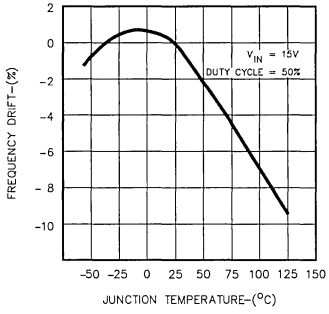


FIGURE 2.
OSCILLATOR TEMPERATURE STABILITY

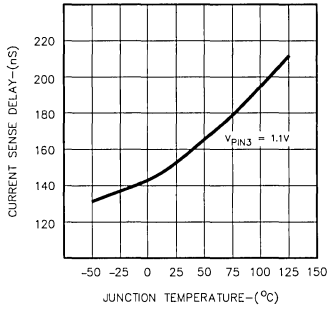


FIGURE 3.
CURRENT SENSE TO OUTPUT DELAY VS. TEMP.

CHARACTERISTIC CURVES (continued)

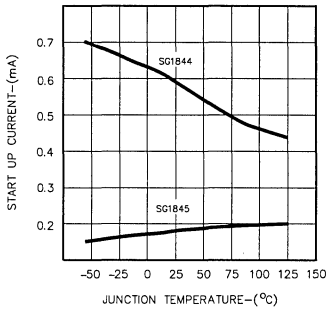


FIGURE 4.
START-UP CURRENT VS. TEMPERATURE

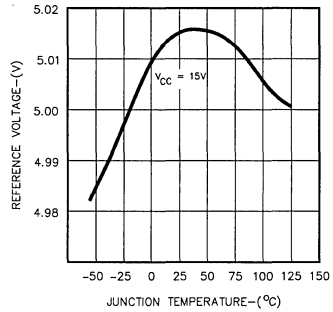


FIGURE 5.
REFERENCE VOLTAGE VS. TEMPERATURE

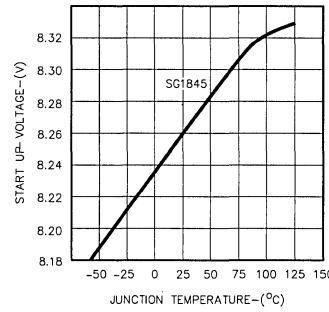


FIGURE 6.
START-UP VOLTAGE THRESHOLD
VS. TEMPERATURE

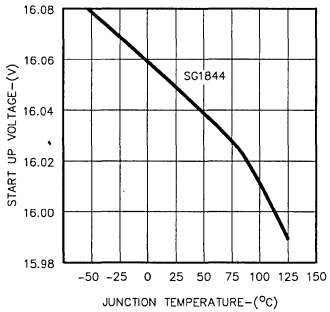


FIGURE 7.
START-UP VOLTAGE THRESHOLD
VS. TEMPERATURE

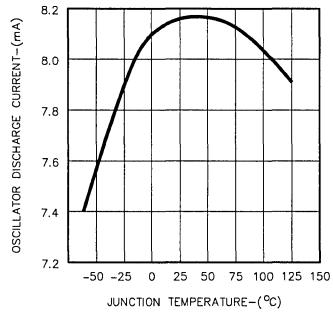


FIGURE 8.
OSCILLATOR DISCHARGE CURRENT
VS. TEMPERATURE

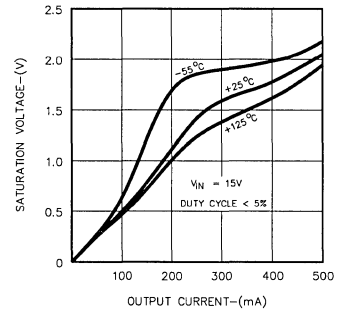


FIGURE 9.
OUTPUT SATURATION VOLTAGE VS. OUTPUT
CURRENT AND TEMPERATURE
(SINK TRANSISTOR)

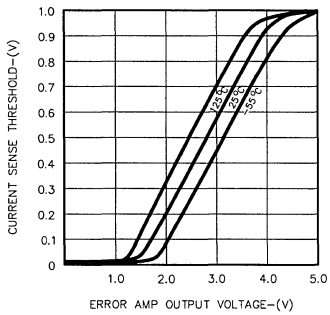


FIGURE 10.
CURRENT SENSE THRESHOLD VS. ERROR
AMPLIFIER OUTPUT

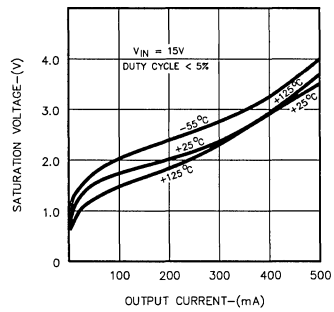
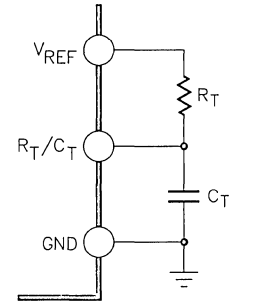


FIGURE 11.
OUTPUT SATURATION VOLTAGE VS. OUTPUT
CURRENT AND TEMPERATURE
(SOURCE TRANSISTOR)

APPLICATION INFORMATION

OSCILLATOR

The oscillator of the SG1844/45 PWM's is programmed by the external timing components (R_T , C_T) as shown in Figure 13.



$$F \approx \frac{1.86}{R_T C_T} \quad \text{WHERE } R_T \geq 5K\Omega$$

FIGURE 12 - OSCILLATOR TIMING CIRCUIT

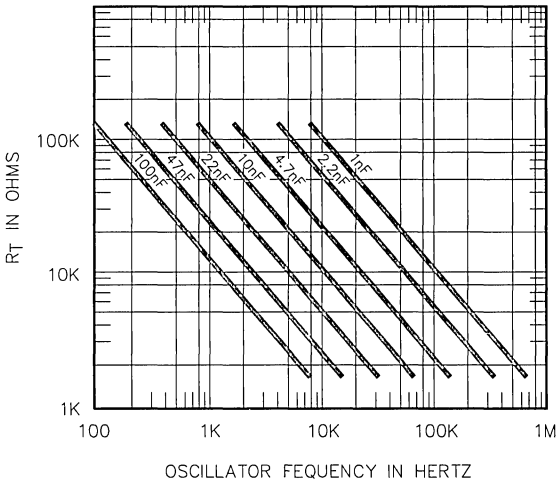


FIGURE 13 - OSCILLATOR FREQUENCY VS. R_T FOR VARIOUS C_T

APPLICATION CIRCUITS (Note 8)

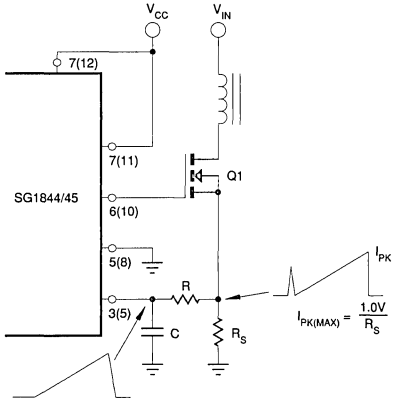


FIGURE 14 — CURRENT SENSE SPIKE SUPPRESSION

The RC low pass filter will eliminate the leading edge current spike caused by parasitics of Power MOSFET.

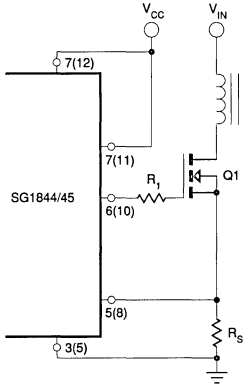


FIGURE 15 — MOSFET PARASITIC OSCILLATIONS

A resistor (R_1) in series with the MOSFET gate will reduce overshoot & ringing caused by the MOSFET input capacitance and any inductance in series with the gate drive. (Note: It is very important to have a low inductance ground path to insure correct operation of the I.C. This can be done by making the ground paths as short and as wide as possible.)

APPLICATION CIRCUITS (continued)

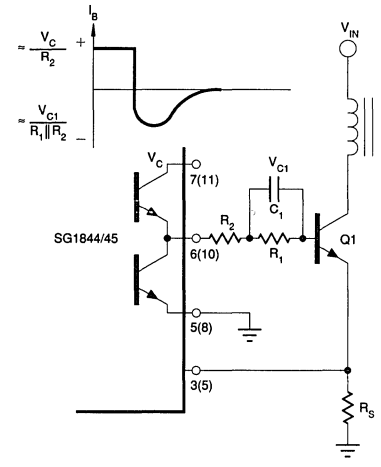


FIGURE 16 — BIPOLAR TRANSISTOR DRIVE

The 1844/45 output stage can provide negative base current to remove base charge of power transistor (Q_1) for faster turn off. This is accomplished by adding a capacitor (C_1) in parallel with a resistor (R_1). The resistor (R_1) is to limit the base current during turn on.

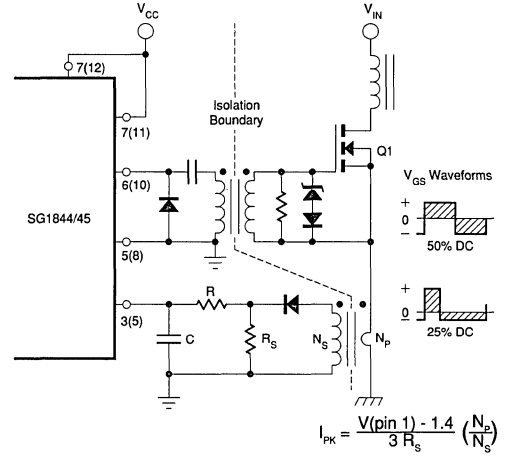


FIGURE 17 — ISOLATED MOSFET DRIVE

Current transformers can be used where isolation is required between PWM and Primary ground. A drive transformer is then necessary to interface the PWM output with the MOSFET.

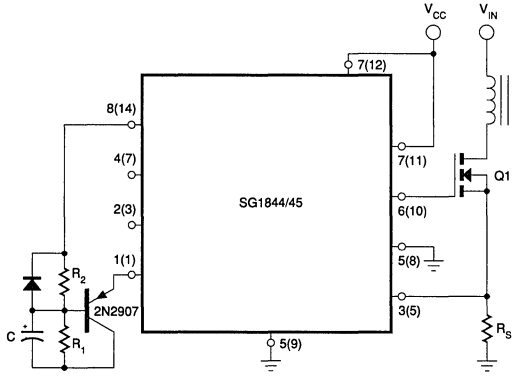


FIGURE 18 — ADJUSTABLE BUFFERED REDUCTION OF CLAMP LEVEL WITH SOFT-START

Soft start and adjustable peak current can be done with the external circuitry shown above.

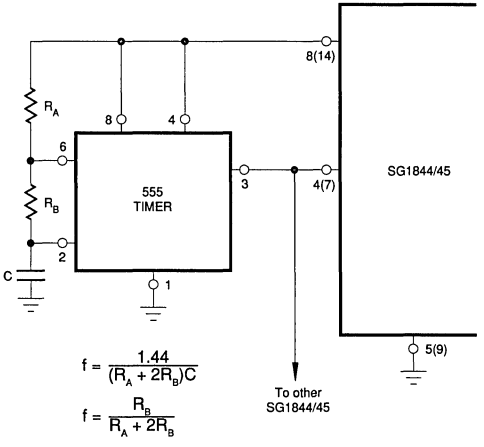


FIGURE 19 — EXTERNAL DUTY CYCLE CLAMP AND MULTI-UNIT SYNCHRONIZATION

Precision duty cycle limiting for a duty cycle of <50%, as well as synchronizing several 1844/45's is possible with the above circuitry.

APPLICATION CIRCUITS (continued)

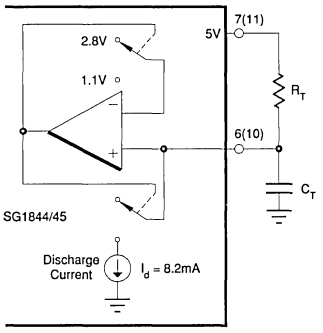


FIGURE 20 — OSCILLATOR CONNECTION

The oscillator is programmed by the values selected for the timing components R_T and C_T. Refer to application information for calculation of the component values.

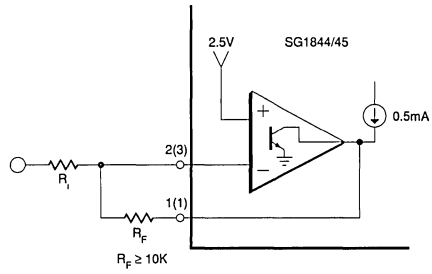
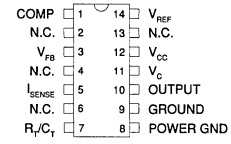
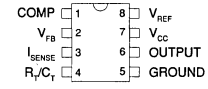
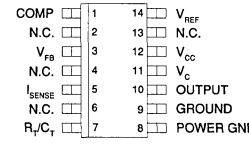


FIGURE 21 — ERROR AMPLIFIER CONNECTION

Error amplifier is capable of sourcing and sinking current up to 0.5mA.

Note 8. Pin numbers referenced are for 8 pin packages and pin numbers in parenthesis are for 14 pin packages.

CONNECTION DIAGRAM & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN CERAMIC DIP J - PACKAGE	SG1844J/883B	-55°C to 125°C	
	SG1844J	-55°C to 125°C	
	SG2844J	-25°C to 85°C	
	SG3844J	0°C to 70°C	
	SG1845J/883B	-55°C to 125°C	
	SG1845J	-55°C to 125°C	
	SG2845J	-25°C to 85°C	
	SG3845J	0°C to 70°C	
14-PIN PLASTIC DIP N - PACKAGE	SG2844N	-25°C to 85°C	
	SG3844N	0°C to 70°C	
	SG2845N	-25°C to 85°C	
	SG3845N	0°C to 70°C	
8-PIN CERAMIC DIP Y - PACKAGE	SG1844Y/883B	-55°C to 125°C	
	SG1844Y	-55°C to 125°C	
	SG2844Y	-25°C to 85°C	
	SG3844Y	0°C to 70°C	
	SG1845Y/883B	-55°C to 125°C	
	SG1845Y	-55°C to 125°C	
	SG2845Y	-25°C to 85°C	
	SG3845Y	0°C to 70°C	
8-PIN PLASTIC DIP M - PACKAGE	SG2844M	-25°C to 85°C	
	SG3844M	0°C to 70°C	
	SG2845M	-25°C to 85°C	
	SG3845M	0°C to 70°C	
14-PIN PLASTIC S.O.I.C. D - PACKAGE	SG2844D	-25°C to 85°C	
	SG3844D	0°C to 70°C	
	SG2845D	-25°C to 85°C	
	SG3845D	0°C to 70°C	

Note: 1. Contat factory for JAN and DESC product availability.
2. All parts are viewed from the top.
3. Product is also available in flat pack and leadless chip carrier. Consult factory for price and delivery.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SG1846/SG2846/SG3846
SG1847/SG2847/SG3847

CURRENT MODE PWM CONTROLLER

DESCRIPTION

The SG1846/1847 family of control ICs provides all of the necessary features to implement fixed frequency, current mode control schemes while maintaining a minimum external parts count. The superior performance of this technique can be measured in improved line regulation, enhanced load response characteristics, and a simpler, easier-to-design control loop. Topological advantages include inherent pulse-by-pulse current limiting capability, automatic symmetry correction for push-pull converters, and the ability to parallel "power modules" while maintaining equal current sharing.

Protection circuitry includes built-in under-voltage lockout and programmable current limit in addition to soft start capability. A shutdown function is also available which can initiate either a complete shutdown with automatic restart or latch the supply off.

Other features include fully latched operation, double pulse suppression, deadtime adjust capability, and a ±1% trimmed bandgap reference.

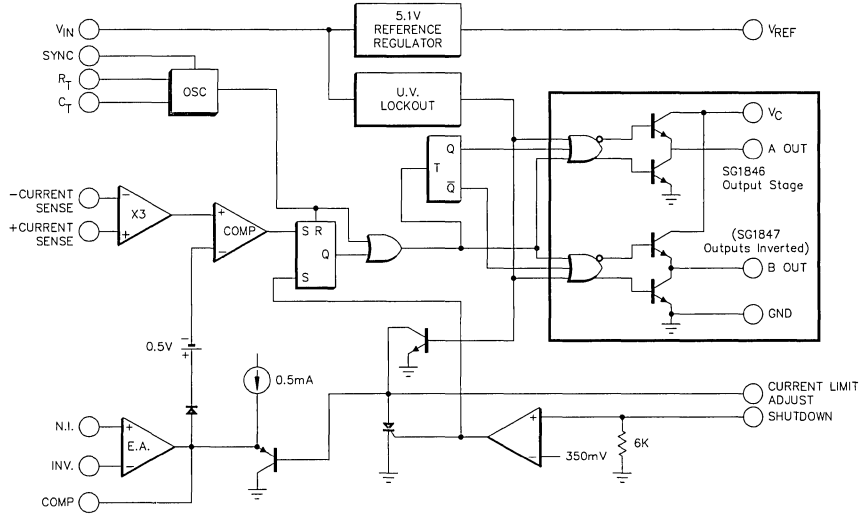
FEATURES

- **Automatic feed forward compensation**
- **Programmable pulse by pulse current limiting**
- **Automatic symmetry correction in push-pull configuration**
- **Enhanced load response characteristics**
- **Parallel operation capability for modular power systems**
- **Differential current sense amplifier with wide common mode range**
- **Double pulse suppression**
- **200mA totem-pole outputs**
- **± 1% bandgap reference**
- **Under-voltage lockout**
- **Soft-start capability**
- **Shutdown capability**
- **500KHz operation**

HIGH RELIABILITY FEATURES - SG1846/47

- **Available to MIL-STD - 883**
- **Radiation data available**
- **SG level "S" processing available**

BLOCK DIAGRAM



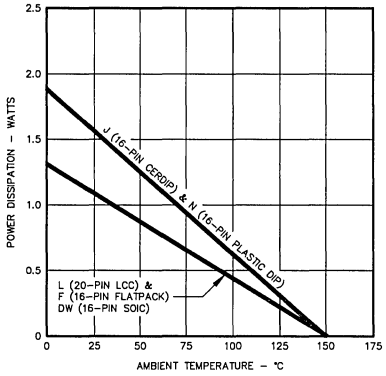
April 1990

ABSOLUTE MAXIMUM RATINGS (Note 1 and 2)

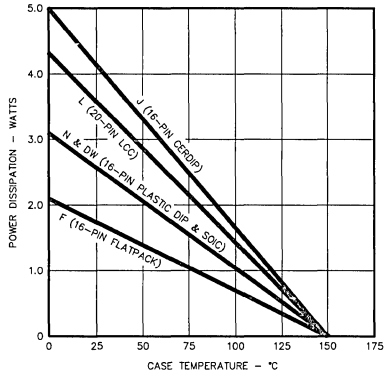
Supply Voltage ($+V_{IN}$) 40V
Collector Supply Voltage(V_C) 40V
Analog Inputs (Pins 3, 4, 5, 6, & 16) ..... -0.3V to $+V_{IN}$
Logic Input ..... -0.3V to 5.5V
Soure/Sink Load current (continuous) 200mA
Source/Sink Load Current (peak, 200ns) 500mA
Reference Load Current 30mA
Soft Start Sink Current 50mA
Sync Output Current 5mA
Error Amplifier Output Current 5mA
Oscillator Charging current (Pin 9) 5mA
Operating Junction Temperature
Hermetic (J, L, F Packages) ..... 150°C
Plastic (N, DW Package) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Values beyond which damage may occur.
Note 2. Pin numbers refer to ceramic J package.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 3)

Supply Voltage Range ..... 8V to 40V
Collector Supply Voltage Range ..... 4.5V to 40V
Source/Sink Output Current (continuous) 100mA
Source/Sink Output Current (peak 200ns) 200mA
Reference Load Current ..... 0 to 10mA
Oscillator Frequency Range ..... 1KHz to 500KHz
Oscillator Timing Resistor (R_T) ..... 2KΩ to 100KΩ
Oscillator Timing Capacitor (C_T) ..... 1000 pF to 0.1μF
Operating Ambient Temperature Range
SG1846/1847 ..... -55°C to 125°C
SG2846/2847 ..... -25°C to 85°C
SG3846/3847 ..... 0°C to 70°C

Note 3. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1846/SG1847 with $-55°C \le T_A \le 125°C$, SG2846/SG2847 with $-25°C \le T_A \le 85°C$, SG3846/SG3847 with $0°C \le T_A \le 70°C$, $+V_{IN} = 15V$. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1846/47 SG2846/47			SG3846/47			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Section								
Output Voltage	$T_J = 25°C$, $I_O = 1mA$	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	$V_{IN} = 8V$ to 40V		5	20		5	20	mV
Load Regulation	$I_L = 1mA$ to 10mA		3	15		3	15	mV
Temperature Stability (Note 4)			0.4			0.4		mV/°C
Total Output Variation (Note 4)	Line, Load and Temperature	5.00		5.20	4.95		5.25	V
Output Noise Voltage (Note 4)	$10Hz \le f \le 10KHz$. $T_J = 25°C$		100			100		μV
Long Term Stability (Note 4)	$T_J = 125°C$, 1000Hrs.		5			5		mV
Short Circuit Output Current	$V_{REF} = 0V$	-10	-45		-10	-45		mA

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1846/47 SG2846/47			SG3846/47			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Oscillator Section (Note 9)								
Initial Accuracy	T_J = 25°C	39	43	47	39	43	47	KHz
Voltage Stability	V_{IN} = 8V to 40V		1	2		1	2	%
Temperature Stability (Note 4)	Over Operating Range		1			1		%
Sync Output High Level		3.9	4.35		3.9	4.35		V
Sync Output Low Level			2.3	2.5		2.3	2.5	V
Sync Input High Level	Pin 8 = 0V	3.9			3.9			V
Sync Input Low Level	Pin 8 = 0V			2.5			2.5	V
Sync Input Current	Sync Voltage = 5.25V, Pin 8 = 0V		1.2	1.5		1.2	1.5	mA
Error Amp Section								
Input Offset Voltage			0.5	5		0.5	10	mV
Input Bias Current			-0.6	-1		-0.6	-2	µA
Input Offset Current			40	250		40	250	nA
Common Mode Range	V_{IN} = 8V to 40V	0		V_{IN}-2V	0		V_{IN}-2V	V
Open Loop Voltage Gain	V_O = 1.2V to 3V, V_{CM} = 2V	80	105		80	105		dB
Unity Gain Bandwidth (Note 4)	T_J = 25°C	0.7	1.0		0.7	1.0		MHz
CMRR	V_{CM} = 0V to 38V, V_{IN} = 40V	75	100		75	100		dB
PSRR	V_{IN} = 8V to 40V	80	105		80	105		dB
Output Sink Current	V_{ID} = - 15mV to -5V, $V_{PIN\,7}$ = 1.2V	2	6		2	6		mA
Output Source Current	V_{ID} = 15mV to 5V, $V_{PIN\,7}$ = 2.5V	-0.4	-0.5		-0.4	-0.5		mA
High Level Output Voltage	R_L = 15KΩ (Pin 7)	4.3	4.6		4.3	4.6		V
Low Level Output Voltage	R_L = 15KΩ (Pin 7)		0.7	1		0.7	1	V
Current Sense Amplifier Section								
Amplifier Gain (Notes 5 & 6)	$V_{PIN\,3}$ = 0V, Pin 1 Open	2.5	2.75	3.0	2.5	2.75	3.0	V
Maximum Differential (Note 6)	Pin 1 Open R_L = 15KΩ (Pin 7)							
Input Signal ($V_{PIN\,4}$ - $V_{PIN\,3}$)(Note 5)		1.1	1.2		1.1	1.2		V
Input Offset Voltage (Note 5)	$V_{PIN\,1}$ = 0.5V, Pin 7 Open		5	25		5	25	mV
CMRR	V_{CM} = 1V to 12V	60	83		60	83		dB
PSRR	V_{IN} = 8V to 40V	60	84		60	84		dB
Input Bias Current (Note 5)	$V_{PIN\,1}$ = 0.5V, Pin 7 Open		-2.5	-10		-2.5	-10	µA
Input Offset Current (Note 5)	$V_{PIN\,1}$ = 0.5V, Pin 7 Open		0.08	1		0.08	1	µA
Input Common Mode Range		0		V_{IN}-3	0		V_{IN}-3	V
Delay to Outputs (Note 4)	T_J = 25°C		200	500		200	500	ns
Current Limit Adjust Section								
Current Limit Offset Voltage (Note 5)	$V_{PIN\,3}$ = 0, $V_{PIN\,4}$ = 0V, Pin 7 Open	0.45	0.5	0.55	0.45	0.5	0.55	V
Input Bias Current	$V_{PIN\,5}$ = V_{REF}, $V_{PIN\,6}$ = 0V		-10	-30		-10	-30	µA
Shutdown Terminal Section								
Threshold Voltage		250	350	400	250	350	400	mV
Input Voltage Range		0		V_{IN}	0		V_{IN}	V
Minimum Latching Current ($I_{PIN\,1}$) (Note 7)		3.0	1.5		3.0	1.5		mA
Maximum Non-Latching Current ($I_{PIN\,1}$) (Note 8)			1.5	0.8		1.5	0.8	mA
Delay to Outputs (Note 4)	T_J = 25°C		300	600		300	600	ns
Output Section								
Collector Emitter Voltage		40			40			V
Collector Leakage Current	V_C = 40V			200			200	µA
Output Low Level	I_{SINK} = 20mA		0.1	0.4		0.1	0.4	V
	I_{SINK} = 100mA		0.4	2.1		0.4	2.1	V
Output High Level	I_{SOURCE} = 20mA	13	13.5		13	13.5		V
	I_{SOURCE} = 100mA	12	13.5		12	13.5		V
Rise Time (Note 4)	C_L = 1nF, T_J = 25°C		50	300		50	300	ns
Fall Time (Note 4)	C_L = 1nF, T_J = 25°C		50	300		50	300	ns

4

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1846/47 SG2846/47			SG3846/47			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Under-Voltage Lockout Section								
Start-Up Threshold			7.7	8.0		7.7	8.0	V
Threshold Hysteresis			0.75			0.75		V
Total Standby Current								
Supply Current			17	21		17	21	mA

Note 4. These parameters although guaranteed over the recommended operating conditions, are not tested in production.

Note 5. Parameter measured at trip point of latch with $V_{PIN\,5} = V_{REF}$, $V_{PIN\,6} = 0V$.

Note 6. Amplifier gain defined as : $G = \frac{\Delta V_{PIN\,7}}{\Delta V_{PIN\,4}}$; $V_{PIN\,4} = 0V$ to $1.0V$

Note 7. Current into Pin 1 guaranteed to latch circuit in shutdown state.

Note 8. Current into Pin 1 guaranteed not to latch circuit in shutdown state.

Note 9. $R_T = 10K\Omega$, $C_T = 4.7nF$

CHARACTERISTIC CURVES

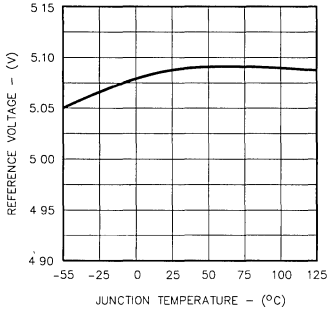


FIGURE 1.
REFERENCE VOLTAGE VS. TEMPERATURE

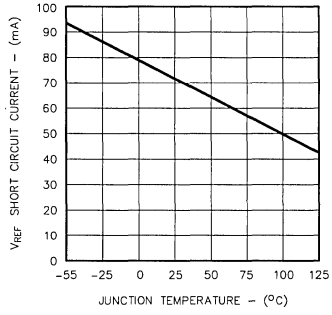


FIGURE 2.
V_{REF} SHORT CIRCUIT CURRENT VS. TEMPERATURE

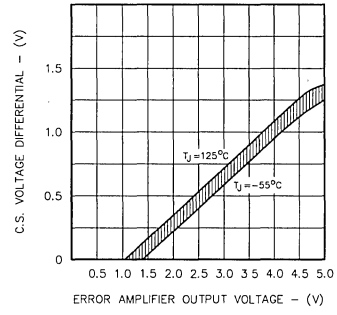


FIGURE 3.
CURRENT SENSE THRESHOLD
VS. ERROR AMPLIFIER OUTPUT

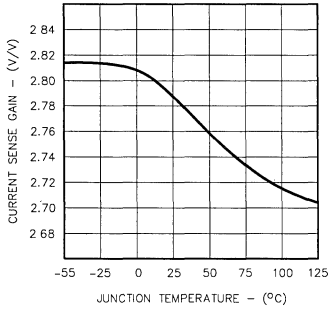


FIGURE 4.
CURRENT SENSE GAIN VS. TEMPERATURE

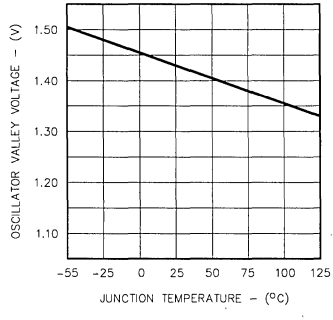


FIGURE 5.
OSCILLATOR VALLEY VOLTAGE VS. TEMPERATURE

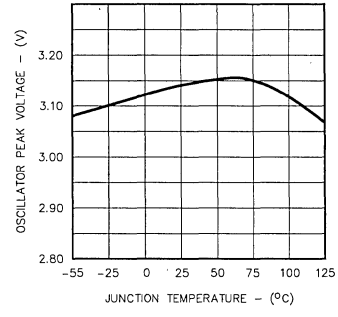


FIGURE 6.
OSCILLATOR PEAK VOLTAGE VS. TEMPERATURE

CHARACTERISTIC CURVES (continued)

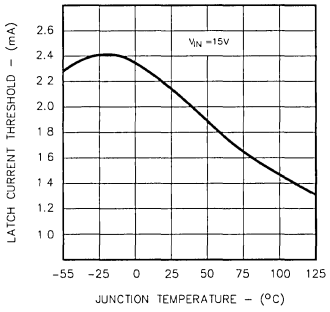


FIGURE 7.
MINIMUM SCR LATCH CURRENT

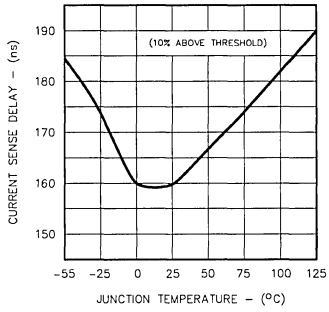


FIGURE 8.
CURRENT SENSE DELAY VS. TEMPERATURE

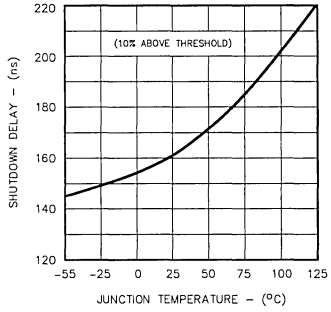


FIGURE 9.
SHUTDOWN DELAY TO OUTPUT VS. TEMPERATURE

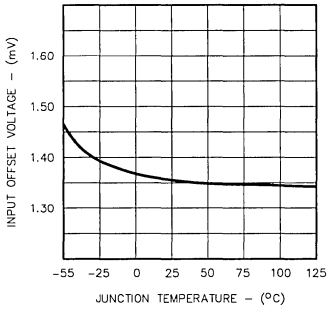


FIGURE 10.
ERROR AMPLIFIER INPUT OFFSET VOLTAGE
VS. TEMPERATURE

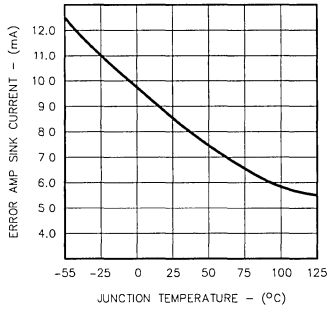


FIGURE 11.
ERROR AMP SINK CURRENT VS. TEMPERATURE

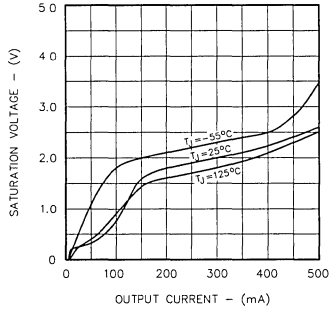


FIGURE 12.
OUTPUT TRANSISTOR SATURATION VOLTAGE
VS. OUTPUT CURRENT (SINK TRANSISTOR)

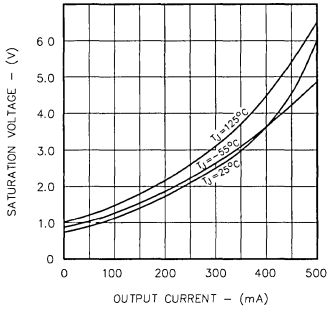


FIGURE 13.
OUTPUT TRANSISTOR SATURATION VOLTAGE
VS. OUTPUT CURRENT (SOURCE TRANSISTOR)

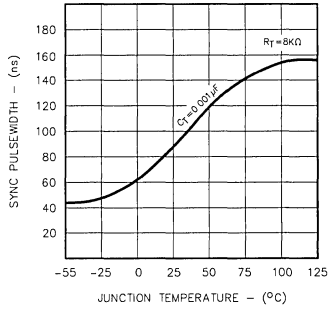


FIGURE 14.
SYNC PULSEWIDTH VS. TEMPERATURE

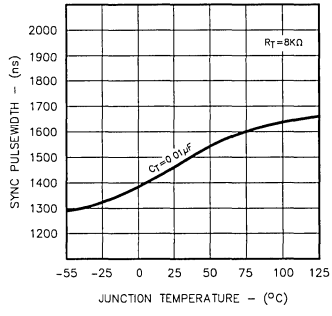


FIGURE 15.
SYNC PULSEWIDTH VS. TEMPERATURE

CHARACTERISTIC CURVES (continued)

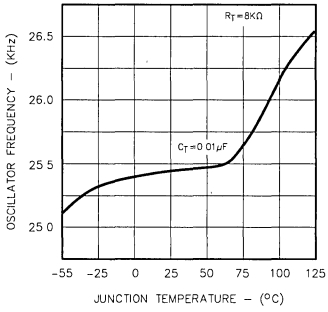


FIGURE 16.
OSCILLATOR FREQUENCY VS. TEMPERATURE

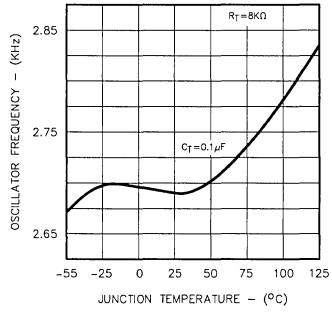


FIGURE 17.
OSCILLATOR FREQUENCY VS. TEMPERATURE

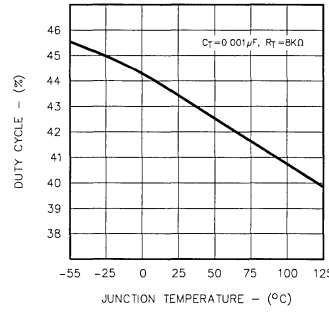


FIGURE 18.
DUTY CYCLE VS. TEMPERATURE

APPLICATION INFORMATION

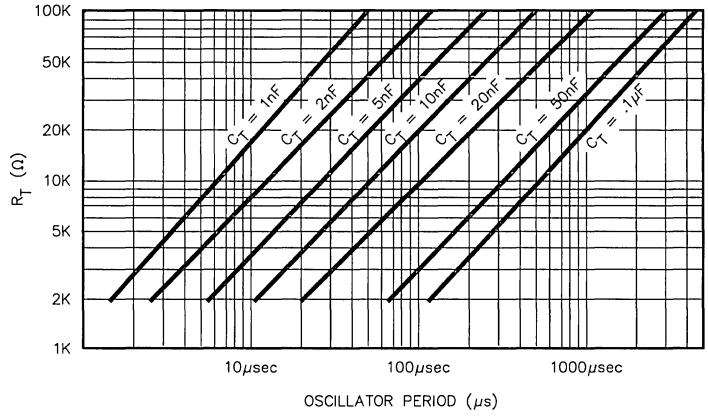
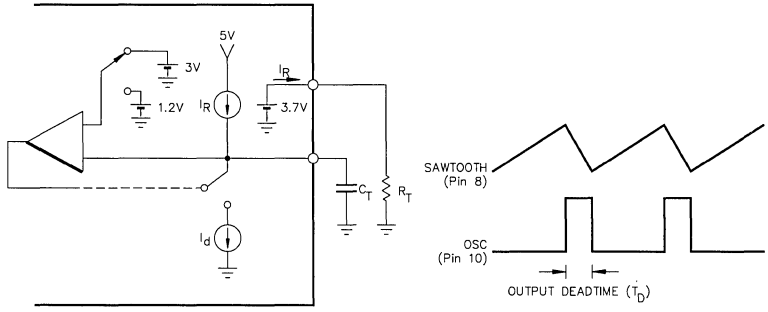


FIGURE 19- OSCILLATOR FREQUENCY CURVES



Oscillator frequency is approximated by the formula: $f_T \approx \frac{2.2}{R_T C_T}$

FIGURE 20 - OSCILLATOR CIRCUIT

APPLICATION INFORMATION (continued)

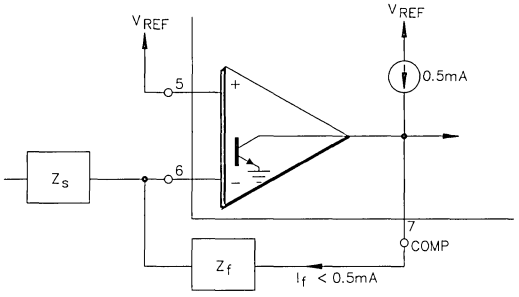


FIGURE 21 - ERROR AMP OUTPUT CONFIGURATION
(Error amplifier can source up to 0.5mA)

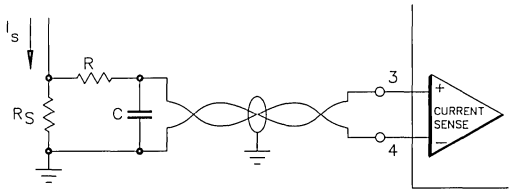


FIGURE 22 - CURRENT SENSE AMPCONNECTIONS

A small RC filter may be required in some applications to reduce switch transients. Differential input allows remote, noise free switching.

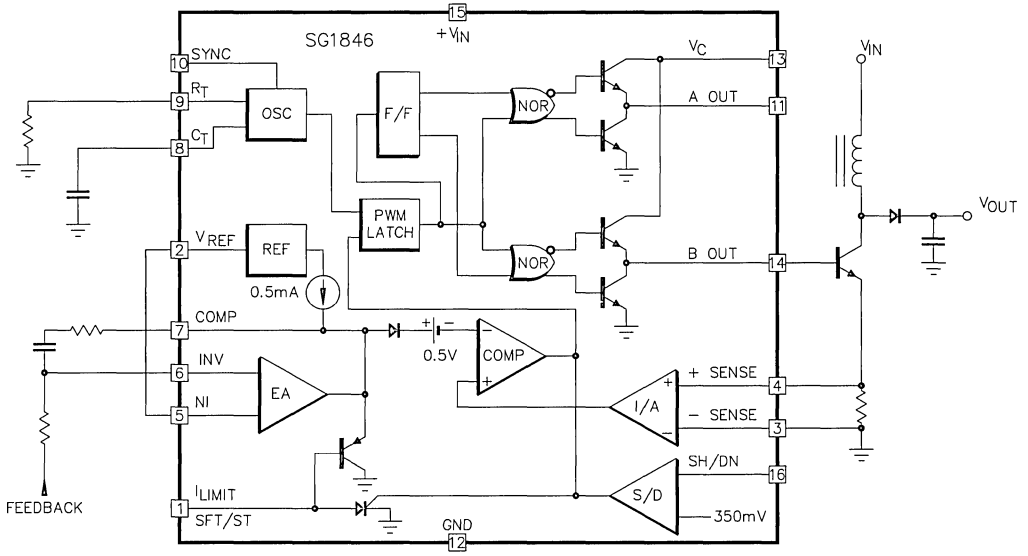


FIGURE 23 - SINGLE ENDED BOOST CONFIGURATION

APPLICATIONS INFORMATION (continued)

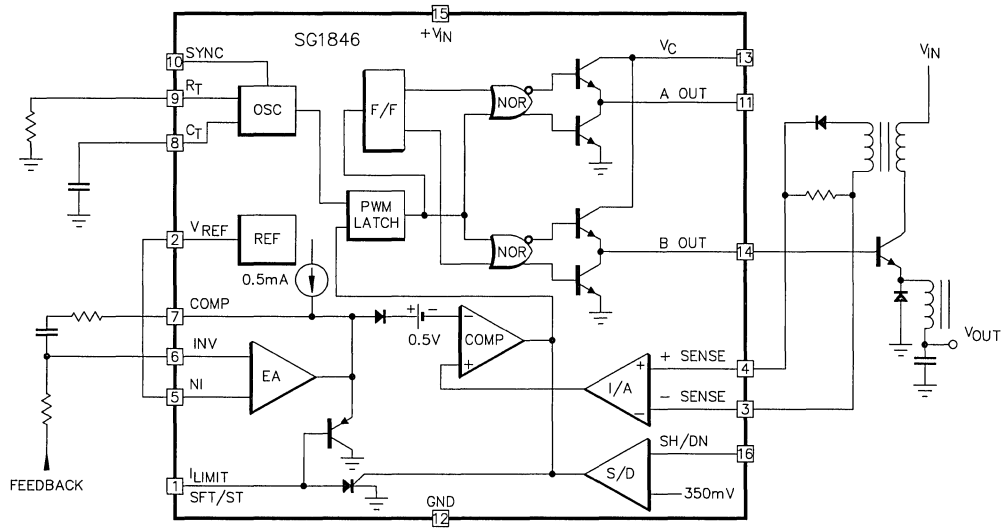


FIGURE 24 - BUCK CONVERTER WITH CURRENT SENSE WINDING

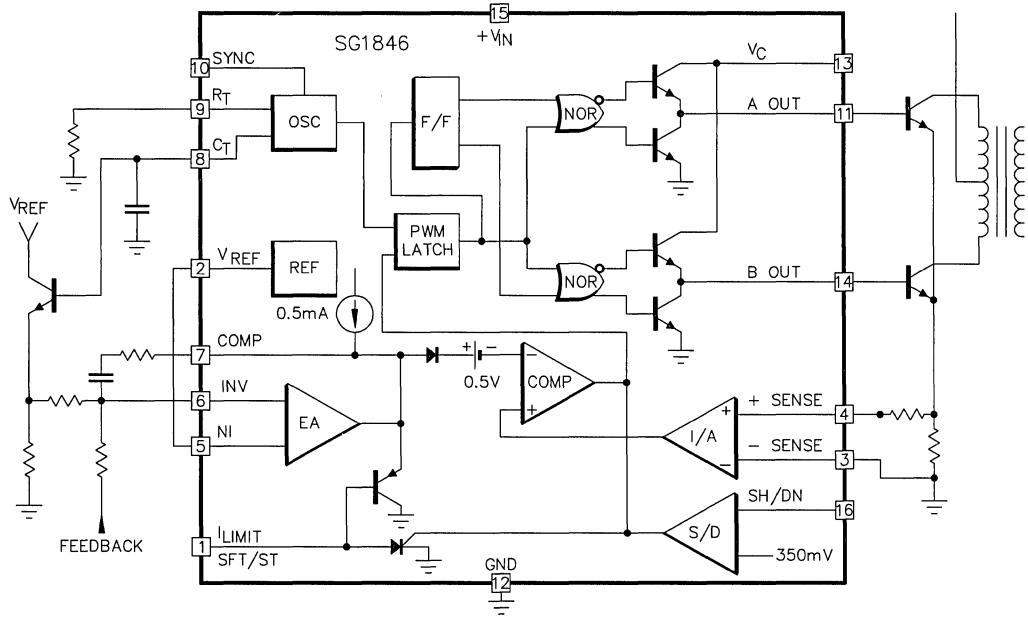
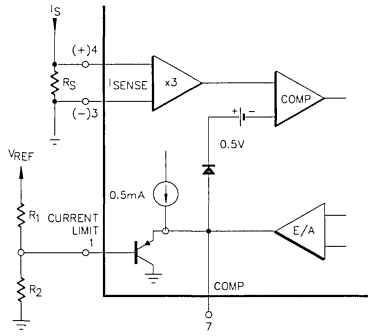


FIGURE 25 - PUSH/PULL CONVERTER WITH SLOPE COMPENSATION

APPLICATIONS INFORMATION (continued)



Peak Current (I_S) is determined by the formula: $I_S = \frac{\frac{R_2 V_{REF}}{R_1 + R_2} - 0.5}{3R_S}$

FIGURE 26 - PULSE BY PULSE CURRENT LIMITING

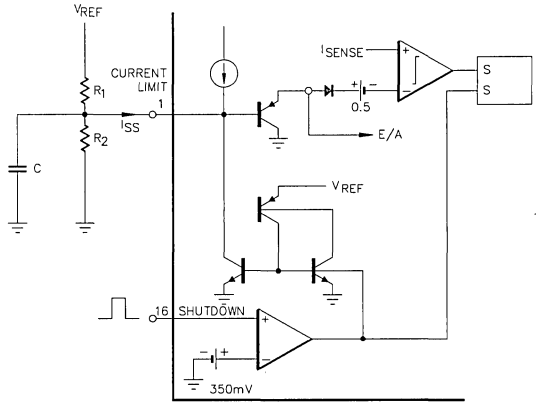
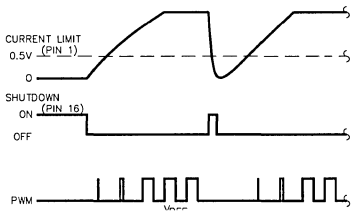
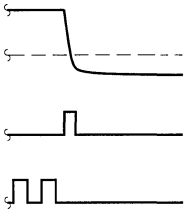


FIGURE 27 - SOFT START AND SHUTDOWN/RESTART FUNCTIONS



$\frac{V_{REF}}{R_1} < 0.8mA$

FIGURE 28 - SHUTDOWN WITH AUTO-RESTART



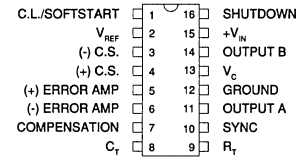
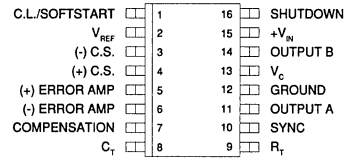
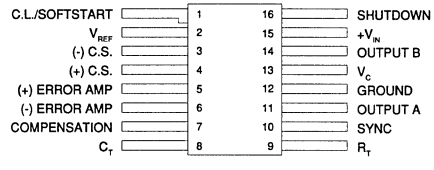
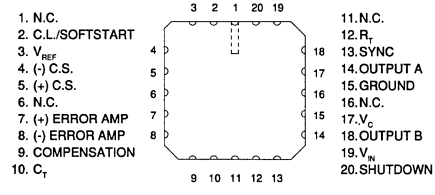
$\frac{V_{REF}}{R_1} > 3mA$ (LATCHED OFF)

FIGURE 29 - SHUTDOWN WITHOUT AUTO-RESTART (LATCHED)

If $\frac{V_{REF}}{R_1} < 0.8mA$ the shutdown latch will commutate when $I_{SS} < 0.8mA$ and a restart cycle will be initiated.

If $\frac{V_{REF}}{R_1} > 3mA$ the device will latch off until power is recycled.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG1846J/883B SG1846J SG2846J SG3846J SG1847J/883B SG1847J SG2847J SG3847J	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C -55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
16-PIN PLASTIC DIP N - PACKAGE	SG2846N SG3846N SG2847N SG3847N	-25°C to 85°C 0°C to 70°C -25°C to 85°C 0°C to 70°C	
16-PIN WIDEBODY PLASTIC S.O.I.C DW - PACKAGE	SG2846DW SG3846DW SG2847DW SG3847DW	-25°C to 85°C 0°C to 70°C -25°C to 85°C 0°C to 70°C	
16-PIN CERAMIC FLAT PACK F - PACKAGE (Note 3)	SG1846F/883B SG1846F SG1847F/883B SG1847F	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C	
20-PIN CERAMIC LEADLESS CHIP CARRIER L - PACKAGE (Note 3)	SG1846L/883B SG1846L SG1847L/883B SG1847L	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C	

Notes:
1. Contact factory for JAN and DESC part availability.
2. All parts are viewed from the top.
3. Consult factory for product availability.

SG3523/SG3423
SG3523A/SG3423A

OVER-VOLTAGE SENSING CIRCUIT

DESCRIPTION

This monolithic integrated circuit provides the control functions necessary to protect sensitive electronic circuitry from over-voltage transients or the effects of voltage regulator failure. It is designed for use with an external SCR "crowbar" for immediate shutdown of the power supply, but additionally provides logic level outputs for regulator turn-off and / or operator or system out-of-tolerance indication.

This device contains an accurate, stable 2.6V reference which allows the sensing threshold to be set predictably without the need for potentiometers. An external capacitor can be used to program an accurate time delay between fault occurence and crowbar triggering, but this delay may be bypassed by inputing at the Sense 2 terminal or by using the remote activation capability.

For additional circuit functions, see SG1542 and SG1543 data sheets.

FEATURES

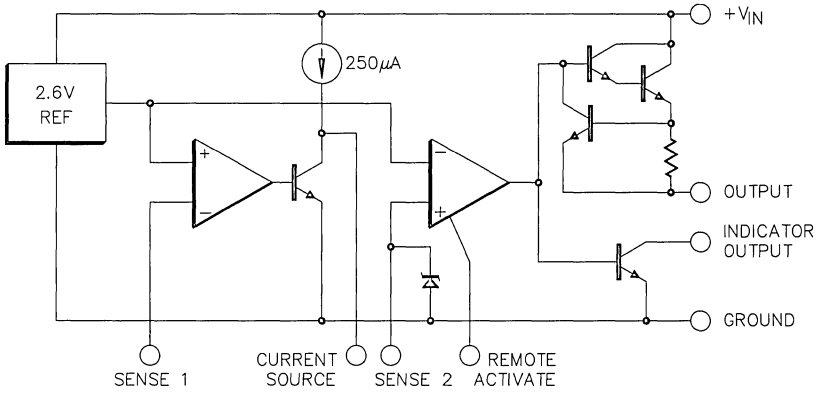
- **Operation from 4.5V to 40V**
- **Highly accurate sensing threshold**
- **Built-in input hysteresis**
- **Programmable time delay**
- **SCR "Crowbar" drive of 200mA**
- **Remote activation capability**

HIGH RELIABILITY FEATURES
- SG3523/SG3523A

- **Available to MIL-STD-883B**
- **SG level "S" processing available**

4

BLOCK DIAGRAM



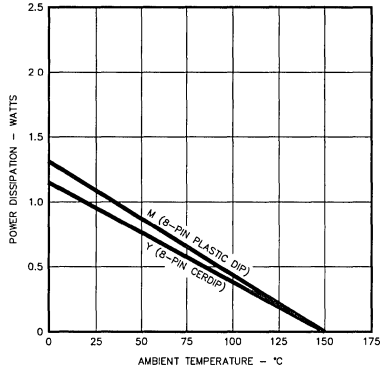
ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage (V_{IN}) 40V
Sense Voltage (1) Input Range ..... V_{IN}
Sense Voltage (2) Input Range 6.5V
Reference Load Current 10mA
Indicator Output Voltage 40V

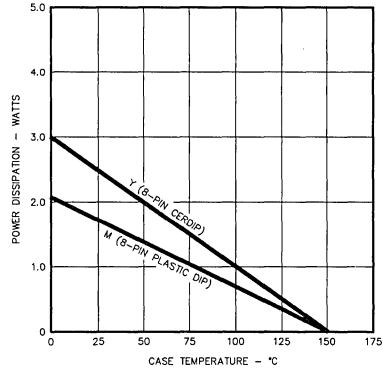
Note 1. Values beyond which damage may occur.

Indicator Output Current 50mA
Operating Junction Temperatures
Hermetic (Y-Packages) ..... 150°C
Plastic (M-Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 3)

Input Supply Voltage (V_{IN}) ..... 4.7V to 40V
Sense Voltage (1) Input Range ..... 0V to V_{IN} -3V
Sense Voltage (2) Input Range ..... 0V to 5.5V
Reference Load Current ..... 0mA to 10mA
Indicator Output Voltage ..... 4.7V to 40V

Indicator Output Current ..... 0mA to 10mA
Delay Timing Capacitor (Note 2) ..... 0μF to 1μF
Operating Ambient Temperature Range
SG3523/3523A ..... -55°C to 125°C
SG3423/3423A ..... 0°C to 70°C

Note 2. Larger value capacitor may be used with peak current limiting. See Figure 1.

Note 3. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG3523/SG3523A with -55°C ≤ T_A ≤ 125°C, SG3423/SG3423A with 0°C ≤ T_A ≤ 70°C, and V_{IN} = 10V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG3523A			SG3423A			SG3423/SG3523			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Voltage Range	T_A = 25°C to T_{MAX}	4.5		40	4.5		40	4.5		40	V
	T_A = T_{MIN} to T_{MAX}	4,7		40	4.7		40	4.7		40	V
Supply Current			5	7		5	7		5	10	mA
Sense Threshold	T_J = 25°C	2.55	2.60	2.65	2.50	2.60	2.70	2.45	2.60	2.75	V
	T_A = T_{MIN} to T_{MAX}	2.50		2.70	2.45		2.75	2.35		2.85	V
Input Hyteresis	Sense 1 only		25			25			25		mV
Input Bias Current	Sense 1		-0.3	-1.0		-0.3	-1.0		-0.3		μA
	Sense 2		+5	+10		+5	+10		+5		μA
Delay Current		200	250	350	200	250	350	150	250	350	μA
Remote Activation Input Current	$V_{PIN\ 5}$ = 2.0V		5	40		5	40		5	40	μA
	$V_{PIN\ 5}$ = 0.8V		-120	-250		-120	-250		-120	-250	μA
Output Voltage	I_O = 100mA	V_{IN}-2.5	V_{IN}-1.6		V_{IN}-2.5	V_{IN}-1.6		V_{IN}-2.5	V_{IN}-1.6		V
Peak Output Current	V_{IN} = 5V, V_O = 0V	100	200	600	100	200	600		200		mA
Output Off Voltage	V_{IN} = 40V		0	0.1		0	0.1		0		V
Indicator Saturation Voltage	I_L = -1.6mA		0.1			0.1			0.1		V
	I_L = -10mA		0.2	0.5		0.2	0.5		0.4		V
Indicator Leakage	$V_{PIN\ 6}$ = 40V		0.1	1.0		0.1	1.0		0.1	1.0	μA
Propagation Delay to Output	T_J = 25°C, Sense 1		1.0			1.0			1.0		μs
	T_J = 25°C, Sense 2		0.5			0.5			0.5		μs
Output Current Rise Time	T_J = 25°C		400			400			400		mA/μs

APPLICATION INFORMATION

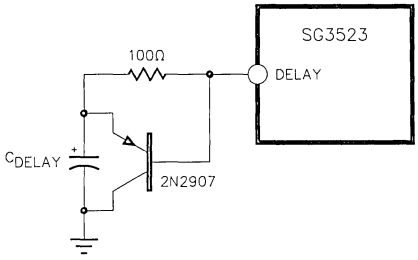
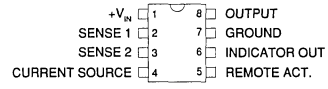


FIGURE 1 - SURGE LIMIT CIRCUIT FOR LARGE DELAY CAPACITORS

The 100Ω resistor limits the peak discharge current into the SG3523 while the external PNP transistor provides a high peak-current discharge path for the delay capacitor.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
8-PIN CERAMIC DIP Y - PACKAGE	SG3523AY/883B SG3523AY SG3523Y/883B SG3523Y SG3423AY SG3423Y	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C 0°C to 70°C 0°C to 70°C	
8-PIN PLASTIC DIP M - PACKAGE	SG3423AM SG3423M	0°C to 70°C 0°C to 70°C	

Note 1. All packages are viewed from the top.

SG7800A/SG7800AC
SG7800/SG7800C

POSITIVE FIXED VOLTAGE REGULATOR

DESCRIPTION

The SG7800A/SG7800 series of positive regulators offer self contained, fixed-voltage capability with up to 1.5A of load current and input voltage up to 50V (SG7800A series only). These units feature a unique on-chip trimming system to set the output voltages to within ±1.5% of nominal on the SG7800A series, ±2.0% on the SG7800 series, and ±4.0% on the SG7800C/340 series. The SG7800A versions also offer much improved line and load regulation characteristics. Utilizing an improved Bandgap reference design, problems have been eliminated that are normally associated with the Zener diode references, such as drift in output voltage and large changes in the line and load regulation.

All protective features of thermal shutdown, current limiting, and safe-area control have been designed into these units and since these regulators require only a small output capacitor for satisfactory performance, ease of application is assured.

Although designed as fixed-voltage regulators, the output voltage can be increased through the use of a simple voltage divider. The low quiescent drain current of the device insures good regulation when this method is used.

Product is available in hermetically sealed TO-257 (both isolated and non-isolated), TO-3, TO39 and TO-66 power packages.

FEATURES

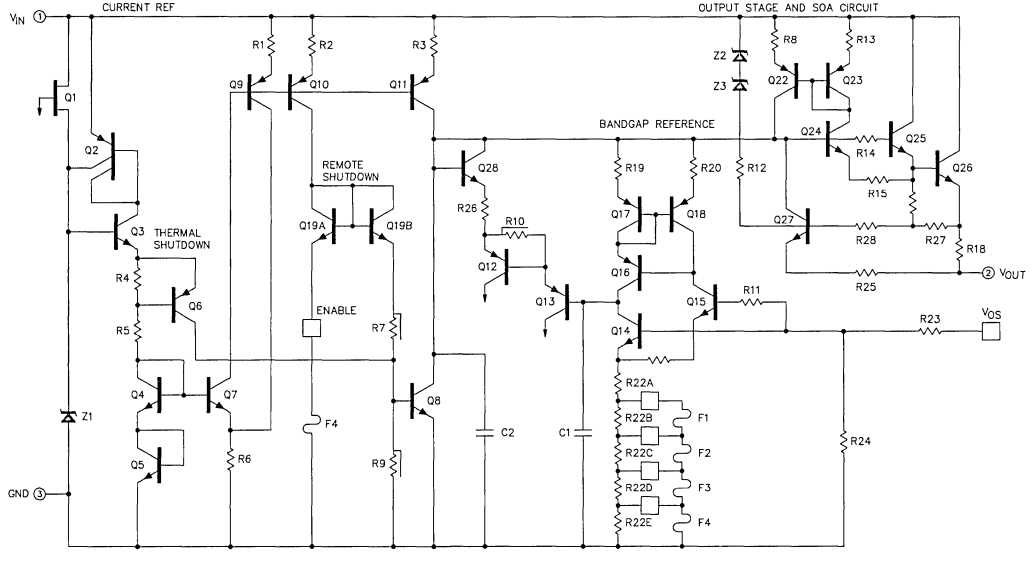
- **Output voltage set internally to ±1.5% on SG7800A**
- **Input voltage range to 50V max. on SG7800A**
- **Two volt input-output differential**
- **Excellent line and load regulation**
- **Foldback current limiting**
- **Thermal overload protection**
- **Voltages available - 5V, 6V, 8V, 12V, 15V, 18V, 20V, 24V**

HIGH RELIABILITY FEATURES - SG7800A/7800

- **Available to MIL-STD - 883**
- **MIL-M38510/10702BXA - JAN7805T**
- **MIL-M38510/10703BXA - JAN7812T**
- **MIL-M38510/10704BXA - JAN7815T**
- **MIL-M38510/10706BYA - JAN7805K**
- **MIL-M38510/10707BYA - JAN7812K**
- **MIL-M38510/10708BYA - JAN7815K**
- **Radiation data available**
- **SG level "S" processing available**

4

SCHEMATIC DIAGRAM



April 1990

ABSOLUTE MAXIMUM RATINGS (Note 1)

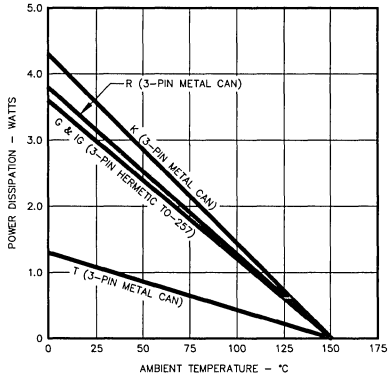
Device Output Voltage	Input Voltage	Input Voltage (transient) (Note 3)	Input Voltage Differential (Output shorted to ground)
5V	35V	50V	35V
6V	35V	50V	35V
8V	35V	50V	35V
12V	35V	50V	35V
15V	35V	50V	35V
18V	35V	50V	35V
20V	35V	50V	35V
24V	40V	50V	35V

Operating Junction Temperature
Hermetic (K, R, T, G, IG - Packages) ..... 150°C

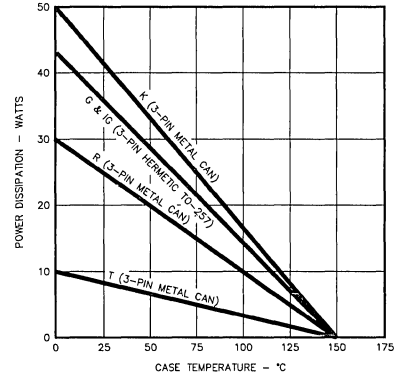
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Values beyond which damage may occur.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Operating Junction Temperature Range:
SG7800 ..... -55°C to 150°C
SG7800C ..... 0°C to 125°C

Note 2. Range over which the device is functional.

CHARACTERISTIC CURVES

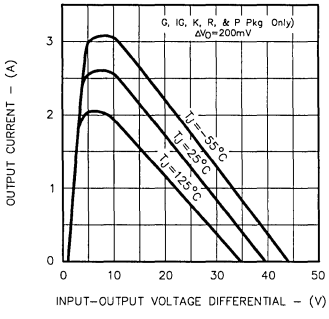


FIGURE 1.
PEAK OUTPUT CURRENT
VS. INPUT - OUTPUT DIFFERENTIAL

Note 3. Operation at high input voltages is dependent upon load current. When load current is less than 5mA, output will rise out of regulation as input-oiutput differential icreases beyond 30V. Note also from Figure 1, that maximum load current is reduced at high voltages. The 50V input rating of the SG140A series refers to ability to withstnd high line or transient conditions without damage. Since the regulator's maximum current capability is reduced, the output may fall out of regulation at high input voltages under nominal loading.

CHARACTERISTIC CURVES (continued)

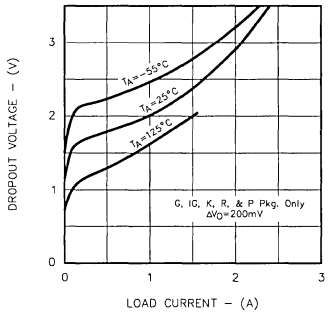


FIGURE 2.
MINIMUM INPUT - OUTPUT VOLTAGE
VS. LOAD CURRENT

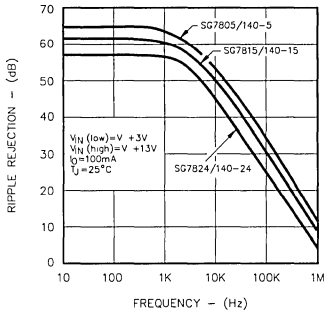


FIGURE 3.
RIPPLE REJECTION VS. FREQUENCY

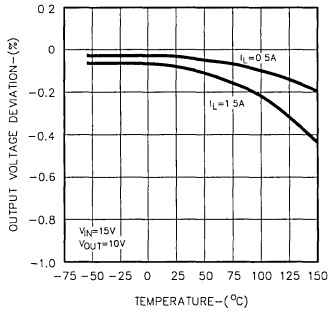
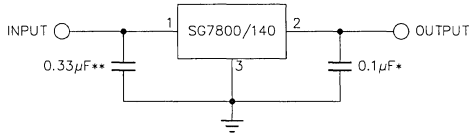


FIGURE 4.
TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE

APPLICATIONS



* INCREASING VALUE OF OUTPUT CAPACITOR IMPROVES SYSTEM TRANSIENT RESPONSE

** REQUIRED ONLY IF REGULATOR IS LOCATED AN APPRECIABLE DISTANCE FROM POWER SUPPLY FILTER

FIGURE 5 - FIXED OUITPUT REGULATOR

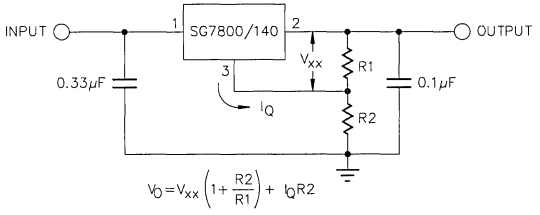


FIGURE 6 - CIRCUIT FOR INCREASING OUITPUT VOLTAGE

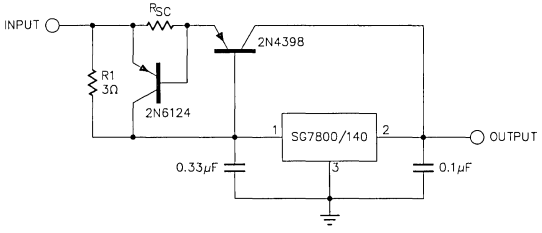


FIGURE 7 - HIGH OUTPUT CIRRENT, SHORT CIRCUIT PROTECTED

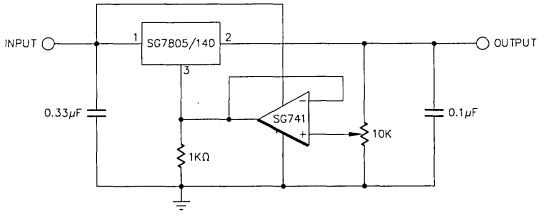


FIGURE 8 - ADJUTABLE OUITPUT REGULATOR, 7V to 30V

ELECTRICAL SPECIFICATIONS (Note 1)

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG7805A/SG7805 with -55°C ≤ T_A ≤ 150°C, SG7805AC/SG7805C with 0°C ≤ T_A ≤ 125°C, V_{IN} = 10V, I_O = 500mA for the K, R, G and IG -Power Packages-, I_O = 100mA for the T package, C_{IN} = 0.33μF, and C_{OUT} = 0.1μF. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperatire.)

SG7805A/SG7805

Parameter	Test Conditions	SG7805A			SG7805			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	4.92	5.00	5.08	4.80	5.00	5.20	V
Line Regulation (Note 1)	V_{IN} = 7.5V to 20V, T_J = 25°C		5	25		5	50	mV
	V_{IN} = 8V to 12V, T_J = 25°C		2	12		2	25	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		15	50		15	50	mV
	I_O = 250mA to 750mA, T_J = 25°C		5	25		5	25	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		5	25		20	100	mV
Total Output Voltage	V_{IN} =8V to 20V							
Tolerance	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	4.85	5.00	5.15	4.65	5.00	5.35	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	4.85	5.00	5.15	4.65	5.00	5.35	V
Quiescent Current	Over Temperature Range			7			7	mA
	T_J = 25°C		4	6		4	6	mA
Quiescent Current Change	With Line: V_{IN} = 8V to 25V			0.8			0.8	mA
	With Load: I_O = 5mA to 1.0A (Power Pkgs.)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		2	2.5		2	2.5	V
Peak Output Current	Power Pkgs: V_{IN} = 10V, T_J = 25°C	1.5	2.0	3.3	1.5	2.0	3.3	A
	T - Pkg: V_{IN} = 10V, T_J = 25°C	0.5	1.0	2.0	0.5	1.0	2.0	A
Short Circuit Current	Power Pkgs: V_{IN} = 35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = 35V, T_J = 25°C			0.7			0.7	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	68			68			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)			40			40	μV/V
Long Term Stability	1000hrs. at T_J = 125°C		20			20		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

SG7805AC/SG7805C

Parameter	Test Conditions	SG7805AC			SG7805C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	4.92	5.00	5.08	4.80	5.00	5.20	V
Line Regulation (Note 1)	V_{IN} = 7.5V to 20V, T_J = 25°C		5	50		5	100	mV
	V_{IN} = 8V to 12V, T_J = 25°C		2	25		4	50	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C			50			100	mV
	I_O = 250mA to 750mA, T_J = 25°C		5	25		10	50	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C			25			100	mV
Total Output Voltage	V_{IN} = 8V to 20V							
Tolerance	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	4.85	5.00	5.15	4.75	5.00	5.25	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	4.85	5.00	5.15	4.75	5.00	5.25	V
Quiescent Current	Over Temperature Range			7			8.5	mA
	T_J = 25°C		4	6		4	8	mA
Quiescent Current Change	With Line: V_{IN} = 8V to 25V			1.0			1.3	mA
	With Load: I_O = 5mA to 1.0A (Power Pkgs.)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		2	2.5		2	2.5	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5	2.0	3.3	1.5	2.0	3.3	A
	T - Pkg: T_J = 25°C	0.5	1.0	2.0	0.5	1.0	2.0	A
Short Circuit Current	Power Pkgs: V_{IN} = 35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = 35V, T_J = 25°C			0.7			0.7	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	68			62			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)			40			40	μV/V
Long Term Stability	1000hrs. at T_J = 125°C		20			20		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

Note 1. All regulation tests are made at constant junction temperature with low duty cycle testing.
2. This test is guaranteed but is not tested in production.

ELECTRICAL SPECIFICATIONS (Note 1)

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG7806A/SG7806 with -55°C ≤ T_A ≤ 150°C, SG7806AC/SG7806C with 0°C ≤ T_A ≤ 125°C, V_{IN} = 11V, I_O = 500mA for the K, R, G and IG -Power Packages-, I_O = 100mA for the T package, C_{IN} = 0.33µF, and C_{OUT} = 0.1µF. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperatire.)

SG7806A/SG7806

Parameter	Test Conditions	SG7606A			SG7806			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	5.9	6.0	6.1	5.75	6.00	6.25	V
Line Regulation (Note 1)	V_{IN} = 8.5V to 25V, T_J = 25°C		6	30		6	60	mV
	V_{IN} = 9V to 13V, T_J = 25°C		3	15		3	30	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		20	60		20	60	mV
	I_O = 250mA to 750mA, T_J = 25°C		6	30		6	30	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C			30			30	mV
Total Output Voltage Tolerance	V_{IN} = 9V to 21V							
	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	5.82	6.00	6.18	5.65	6.00	6.35	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	5.82	6.00	6.18	5.65	6.00	6.35	V
Quiescent Current	Over Temperature Range			7			7	mA
	T_J = 25°C		4	6		4	6	mA
Quiescent Current Change	With Line: V_{IN} = 8V to 25V			0.8			0.8	mA
	With Load: I_O = 5mA to 1.0A (Power Pkgs.)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		2	2.5		2	2.5	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5	2.0	3.3	1.5	2.0	3.3	A
	T - Pkg: T_J = 25°C	0.5	1.0	1.7	0.5	1.0	1.7	A
Short Circuit Current	Power Pkgs: V_{IN} = 35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = 35V, T_J = 25°C			0.7			0.7	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	65			65			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)			40			40	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		24			24		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

SG7806AC/SG7806C

Parameter	Test Conditions	SG7806AC			SG7806C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	5.9	6.0	6.1	5.75	6.00	6.25	V
Line Regulation (Note 1)	V_{IN} = 8.5V to 25V, T_J = 25°C		6	60		12	120	mV
	V_{IN} = 9V to 13V, T_J = 25°C		3	30		6	60	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		15	60		25	120	mV
	I_O = 250mA to 750mA, T_J = 25°C		5	30		10	60	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C			30			60	mV
Total Output Voltage Tolerance	V_{IN} = 9V to 21V							
	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	5.82	6.00	6.18	5.7	6.0	6.3	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	5.82	6.00	6.18	5.7	6.0	6.3	V
Quiescent Current	Over Temperature Range			7			8.5	mA
	T_J = 25°C		4	6		4	8	mA
Quiescent Current Change	With Line: V_{IN} = 8V to 25V			1.0			1.3	mA
	With Load: I_O = 5mA to 1.0A (Power Pkgs.)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		2	2.5		2	2.5	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5	2.0	3.3	1.5	2.0	3.3	A
	T - Pkg: T_J = 25°C	0.5	1.0	1.7	0.5	1.0	1.7	A
Short Circuit Current	Power Pkgs: V_{IN} = 35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = 35V, T_J = 25°C			0.7			0.7	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	62			59			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)			40			40	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		24			24		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

Note 1. All regulation tests are made at constant junction temperature with low duty cycle testing.
2. This test is guaranteed but is not tested in production.

ELECTRICAL SPECIFICATIONS (Note 1)

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG7808A/SG7808 with -55°C ≤ T_A ≤ 150°C, SG7808AC/SG7808C with 0°C ≤ T_A ≤ 125°C, V_{IN} = 14V, I_O = 500mA for the K, R, G and IG -Power Packages-, I_O = 100mA for the T package, C_{IN} = 0.33µF, and C_{OUT} = 0.1µF. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperatire.)

SG7808A/SG7808

Parameter	Test Conditions	SG7808A			SG7808			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	7.88	8.00	8.12	7.7	8.00	8.3	V
Line Regulation (Note 1)	V_{IN} = 10.5V to 25V, T_J = 25°C		8	40		8	80	mV
	V_{IN} = 11V to 17V, T_J = 25°C		4	20		4	40	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		24	70		24	80	mV
	I_O = 250mA to 750mA, T_J = 25°C		8	35		8	40	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		8	35		8	40	mV
Total Output Voltage	V_{IN} = 11.5V to 23V							
Tolerance	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	7.76	8.00	8.24	7.6	8	8.4	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	7.76	8.00	8.24	7.6	8	8.4	V
Quiescent Current	Over Temperature Range			7			7	mA
	T_J = 25°C		4	6		4	6	mA
Quiescent Current Change	With Line: V_{IN} = 11.5V to 25V			0.8			0.8	mA
	With Load: I_O = 5mA to 1.0A (Power Pkgs.)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		2	2.5		2	2.5	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5	2.0	3.3	1.5	2.0	3.3	A
	T - Pkg: T_J = 25°C	0.5	1.0	1.7	0.5	1.0	1.7	A
Short Circuit Current	Power Pkgs: V_{IN} = 35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = 10V, T_J = 25°C			0.7			0.7	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	62			62			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)							µV/V
Long Term Stability	1000hrs. at T_J = 125°C		32			32		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

SG7808AC/SG7808C

Parameter	Test Conditions	SG7808AC			SG7808C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	7.88	8.00	8.12	7.7	8.0	8.3	V
Line Regulation (Note 1)	V_{IN} = 10.5V to 25V, T_J = 25°C		8	80		16	160	mV
	V_{IN} = 11V to 17V, T_J = 25°C		4	40		8	80	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		24	80		40	160	mV
	I_O = 250mA to 750mA, T_J = 25°C		8	40		16	80	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		8	40		16	80	mV
Total Output Voltage	V_{IN} = 11.5V to 23V							
Tolerance	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	7.76	8.00	8.24	7.6	8.0	8.4	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	7.76	8.00	8.24	7.6	8.0	8.4	V
Quiescent Current	Over Temperature Range			7			8.5	mA
	T_J = 25°C		4	6		4	8	mA
Quiescent Current Change	With Line: V_{IN} = 11.5V to 25V			1.0			1.0	mA
	With Load: I_O = 5mA to 1.0A (Power Pkgs.)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		2	2.5		2	2.5	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5	2.0	3.3	1.5	2.0	3.3	A
	T - Pkg: T_J = 25°C	0.5	1.0	1.7	0.5	1.0	1.7	A
Short Circuit Current	Power Pkgs: V_{IN} = 35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = 35V, T_J = 25°C			0.7			0.7	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	62			55			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)			40			40	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		32			32		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

Note 1. All regulation tests are made at constant junction temperature with low duty cycle testing.
2. This test is guaranteed but is not tested in production.

ELECTRICAL SPECIFICATIONS (Note 1)

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG7812A/SG7812 with -55°C ≤ T_A ≤ 150°C, SG7812AC/SG7812C with 0°C ≤ T_A ≤ 125°C, V_{IN} = 19V, I_O = 500mA for the K, R, G and IG -Power Packages-, I_O = 100mA for the T package, C_{IN} = 0.33µF, and C_{OUT} = 0.1µF. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperatire.)

SG7812A/SG7812

Parameter	Test Conditions	SG7812A			SG7812			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	11.8	12.0	12.2	11.5	12.0	12.5	V
Line Regulation (Note 1)	V_{IN} = 14.5V to 30V, T_J = 25°C		12	60		12	120	mV
	V_{IN} = 16V to 22V, T_J = 25°C		6	30		6	60	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		28	80		28	120	mV
	I_O = 250mA to 750mA, T_J = 25°C		10	40		10	60	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		10	40		10	60	mV
Total Output Voltage Tolerance	V_{IN} = 15.5V to 27V							
	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	11.7	12.0	12.3	11.4	12.0	12.6	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	11.7	12.0	12.3	11.4	12.0	12.6	V
Quiescent Current	Over Temperature Range			7			7	mA
	T_J = 25°C		4	6		4	6	mA
Quiescent Current Change	With Line: V_{IN} = 15V to 30V			0.8			0.8	mA
	With Load: I_O = 5mA to 1.0A (Power Pkgs.)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		2	2.5		2	2.5	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5	2.0	3.3	1.5	2.0	3.3	A
	T - Pkg: T_J = 25°C	0.5	1.0	1.7	0.5	1.0	1.7	A
Short Circuit Current	Power Pkgs: V_{IN} = 35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = 35V, T_J = 25°C			0.7			0.7	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	61			61			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)			40			40	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		48			48		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

SG7812AC/SG7812C

Parameter	Test Conditions	SG7812AC			SG7812C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	11.8	12.0	12.2	11.5	12.0	12.5	V
Line Regulation (Note 1)	V_{IN} = 14.5V to 30V, T_J = 25°C		12	120		240	240	mV
	V_{IN} = 16V to 22V, T_J = 25°C		6	60		12	120	mV
Load Regulation (Note1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		28	120		80	240	mV
	I_O = 250mA to 750mA, T_J = 25°C		10	60		24	120	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		10	60		24	120	mV
Total Output Voltage Tolerance	V_{IN} = 15.5V to 27V							
	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	11.7	12.0	12.3	11.4	12.0	12.6	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	11.7	12.0	12.3	11.4	12.0	12.6	V
Quiescent Current	Over Temperature Range			7			8.5	mA
	T_J = 25°C		4	6		4	8	mA
Quiescent Current Change	With Line: V_{IN} = 15V to 30V			1.0			1.0	mA
	With Load: I_O = 5mA to 1.0A (Power Pkgs.)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		2	2.5		2	2.5	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5	2.0	3.3	1.5	2.0	3.3	A
	T - Pkg: T_J = 25°C	0.5	1.0	1.7	0.5	1.0	1.7	A
Short Circuit Current	Power Pkgs: V_{IN} = 35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = 35V, T_J = 25°C			0.7			0.7	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	61			55			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)			40			40	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		48			48		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

Note 1. All regulation tests are made at constant junction temperature with low duty cycle testing.
2. This test is guaranteed but is not tested in production.

ELECTRICAL SPECIFICATIONS (Note 1)

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG7815A/SG7815 with -55°C ≤ T_A ≤ 150°C, SG7815AC/SG7815C with 0°C ≤ T_A ≤ 125°C, V_{IN} = 23V, I_O = 500mA for the K, R, G and IG -Power Packages-, I_O = 100mA for the T package, C_{IN} = 0.33µF, and C_{OUT} = 0.1µF. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperatire.)

SG7815A/SG7815

Parameter	Test Conditions	SG7815A			SG7815			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	14.8	15.0	15.2	14.4	15.0	15.6	V
Line Regulation (Note 1)	V_{IN} = 17.5V to 30V, T_J = 25°C		15	75		15	150	mV
	V_{IN} = 20V to 26V, T_J = 25°C		8	40		8	75	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		30	100		30	150	mV
	I_O = 250mA to 750mA, T_J = 25°C		12	50		12	75	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		12	50		12	75	mV
Total Output Voltage Tolerance	V_{IN} = 18.5V to 30V							
	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	14.6	15.0	15.4	14.3	15.0	15.7	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	14.6	15.0	15.4	14.3	15.0	15.7	V
Quiescent Current	Over Temperature Range			7			7	mA
	T_J = 25°C		4	6		4	6	mA
Quiescent Current Change	With Line: V_{IN} = 18.5V to 30V			0.8			0.8	mA
	With Load: I_O = 5mA to 1.0A (Power Pkgs.)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		2	2.5		2	2.5	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5	2.2	3.3	1.5	2.2	3.3	A
	T - Pkg: T_J = 25°C	0.5	0.9	1.7	0.5	0.9	1.7	A
Short Circuit Current	Power Pkgs: V_{IN} = 35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = 35V, T_J = 25°C			0.7			0.7	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	60			60			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)			40			40	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		60			60		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

SG7815AC/SG7815C

Parameter	Test Conditions	SG7815AC			SG7815C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	14.8	15.0	15.2	14.4	15.0	15.6	V
Line Regulation (Note 1)	V_{IN} = 17.5V to 30V, T_J = 25°C		15	150		30	300	mV
	V_{IN} = 20V to 26V, T_J = 25°C		8	75		15	150	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		30	150		100	300	mV
	I_O = 250mA to 750mA, T_J = 25°C		12	75		30	150	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		12	75		30	150	mV
Total Output Voltage Tolerance	V_{IN} = 13.5V to 30V							
	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	14.6	15.0	15.4	14.3	15.0	15.7	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	14.6	15.0	15.4	14.3	15.0	15.7	V
Quiescent Current	Over Temperature Range			7			8.5	mA
	T_J = 25°C		4	6		4	8	mA
Quiescent Current Change	With Line: V_{IN} = 18.5V to 30V			1.0			1.0	mA
	With Load: I_O = 5mA to 1.0A (Power Pkgs.)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		2	2.5		2	2.5	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5	2.2	3.3	1.5	2.2	3.3	A
	T - Pkg: T_J = 25°C	0.5	0.9	1.7	0.5	0.9	1.7	A
Short Circuit Current	Power Pkgs: V_{IN} = 35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = 35V, T_J = 25°C			0.7			0.7	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	60			60			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)			40			40	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		60			60		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

Note 1. All regulation tests are made at constant junction temperature with low duty cycle testing.
2. This test is guaranteed but is not tested in production.

ELECTRICAL SPECIFICATIONS (Note 1)

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG7818A/SG7818 with -55°C ≤ T_A ≤ 150°C, SG7818AC/SG7818C with 0°C ≤ T_A ≤ 125°C, V_{IN} = 27V, I_O = 500mA for the K, R, G and IG -Power Packages-, I_O = 100mA for the T package, C_{IN} = 0.33μF, and C_{OUT} = 0.1μF. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperatire.)

SG7818A/SG7818

Parameter	Test Conditions	SG7818A			SG7818			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	17.7	18.0	18.3	17.3	18.0	18.7	V
Line Regulation (Note 1)	V_{IN} = 21V to 33V, T_J = 25°C		20	90		20	180	mV
	V_{IN} = 24V to 30V, T_J = 25°C		10	45		10	90	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		40	120		40	180	mV
	I_O = 250mA to 750mA, T_J = 25°C		15	60		15	90	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		15	60		15	90	mV
Total Output Voltage Tolerance	V_{IN} = 22V to 33V							
	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	17.5	18.0	18.5	17.1	18.0	18.9	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	17.5	18.0	18.5	17.1	18.0	18.9	V
Quiescent Current	Over Temperature Range			7			7	mA
	T_J = 25°C		4	6		4	6	mA
Quiescent Current Change	With Line: V_{IN} = 28V to 38V			0.8			0.8	mA
	With Load: I_O = 5mA to 1.0A (Power Pkgs.)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		2	2.5		2	2.5	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5	2.2	3.3	1.5	2.2	3.3	A
	T - Pkg: T_J = 25°C	0.5	0.9	1.7	0.5	0.9	1.7	A
Short Circuit Current	Power Pkgs: V_{IN} = 35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = 35V, T_J = 25°C			0.7			0.7	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	59			59			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)			40			40	μV/V
Long Term Stability	1000hrs. at T_J = 125°C		72			72		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

SG7818AC/SG7818C

Parameter	Test Conditions	SG7818AC			SG7818C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	17.7	18.0	18.3	17.3	18.0	18.7	V
Line Regulation (Note 1)	V_{IN} = 21V to 33V, T_J = 25°C		20	180		40	360	mV
	V_{IN} = 24V to 30V, T_J = 25°C		10	90		20	180	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		40	180		120	360	mV
	I_O = 250mA to 750mA, T_J = 25°C		15	90		40	180	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		15	90		40	180	mV
Total Output Voltage Tolerance	V_{IN} = 22V to 33V							
	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	17.5	18.0	18.5	17.1	18.0	18.9	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	17.5	18.0	18.5	17.1	18.0	18.9	V
Quiescent Current	Over Temperature Range			7			8.5	mA
	T_J = 25°C		4	6		4	8	mA
Quiescent Current Change	With Line: V_{IN} = 28V to 38V			1.0			1.0	mA
	With Load: I_O = 5mA to 1.0A (Power Pkgs.)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		2	2.5		2	2.5	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5	2.2	3.3	1.5	2.2	3.3	A
	T - Pkg: T_J = 25°C	0.5	0.9	1.7	0.5	0.9	1.7	A
Short Circuit Current	Power Pkgs: V_{IN} = 35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = 35V, T_J = 25°C			0.7			0.7	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	59			59			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)							μV/V
Long Term Stability	1000hrs. at T_J = 125°C		72			72		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

Note 1. All regulation tests are made at constant junction temperature with low duty cycle testing.
2. This test is guaranteed but is not tested in production.

ELECTRICAL SPECIFICATIONS (Note 1)

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG7820A/SG7820 with -55°C ≤ T_A ≤ 150°C, SG7820AC/SG7820C with 0°C ≤ T_A ≤ 125°C, V_{IN} = 29V, I_O = 500mA for the K, R, G and IG -Power Packages-, I_O = 100mA for the T package, C_{IN} = 0.33μF, and C_{OUT} = 0.1μF. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperatire.)

SG7820A/SG7820

Parameter	Test Conditions	SG7820A			SG7820			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	19.7	20.0	20.3	19.2	20.0	20.8	V
Line Regulation (Note 1)	V_{IN} = 27V to 35V, T_J = 25°C		22	100		22	200	mV
	V_{IN} = 26V to 32V, T_J = 25°C		12	50		12	100	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		45	140		45	200	mV
	I_O = 250mA to 750mA, T_J = 25°C		20	70		20	100	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		20	70		20	100	mV
Total Output Voltage	V_{IN} = 24V to 35V							
Tolerance	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	19.4	20.0	20.6	19.0	20.0	21.0	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	19.4	20.0	20.6	19.0	20.0	21.0	V
Quiescent Current	Over Temperature Range			7			7	mA
	T_J = 25°C		4	6		4	6	mA
Quiescent Current Change	With Line: V_{IN} = 24V to 35V			0.8			0.8	mA
	With Load: I_O = 5mA to 1.0A (Power Pkgs.)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		2	2.5		2	2.5	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5	2.2	3.3	1.5	2.2	3.3	A
	T - Pkg: T_J = 25°C	0.5	0.9	1.7	0.5	0.9	1.7	A
Short Circuit Current	Power Pkgs: V_{IN} = 35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = 35V, T_J = 25°C			0.7			0.7	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	58			58			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)			40			40	μV/V
Long Term Stability	1000hrs. at T_J = 125°C		96			96		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

SG7820AC/SG7820C

Parameter	Test Conditions	SG7820AC			SG7820C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	19.7	20.0	20.3	19.2	20.0	20.8	V
Line Regulation (Note 1)	V_{IN} = 27V to 35V, T_J = 25°C		22	200		44	400	mV
	V_{IN} = 26V to 32V, T_J = 25°C		12	100		24	200	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		45	200		150	400	mV
	I_O = 250mA to 750mA, T_J = 25°C		20	100		50	200	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		20	100		50	200	mV
Total Output Voltage	V_{IN} = 24V to 35V							
Tolerance	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	19.4	20.0	20.6	19.0	20.0	21.0	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	19.4	20.0	20.6	19.0	20.0	21.0	V
Quiescent Current	Over Temperature Range			7			8.5	mA
	T_J = 25°C		4	6		4	8	mA
Quiescent Current Change	With Line: V_{IN} = 24V to 35V			1.0			1.0	mA
	With Load: I_O = 5mA to 1.0A (Power Pkgs.)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		2	2.5		2	2.5	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5	2.2	3.3	1.5	2.2	3.3	A
	T - Pkg: T_J = 25°C	0.5	0.9	1.7	0.5	0.9	1.7	A
Short Circuit Current	Power Pkgs: V_{IN} = 35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = 35V, T_J = 25°C			0.7			0.7	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	58			58			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)			40			40	μV/V
Long Term Stability	1000hrs. at T_J = 125°C		96			96		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

Note 1. All regulation tests are made at constant junction temperature with low duty cycle testing.
2. This test is guaranteed but is not tested in production.

ELECTRICAL SPECIFICATIONS (Note 1)

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG7824A/SG7824 with -55°C ≤ T_A ≤ 150°C, SG7824AC/SG7824C with 0°C ≤ T_A ≤ 125°C, V_{IN} = 32V, I_O = 500mA for the K, R, G and IG -Power Packages-, I_O = 100mA for the T package, C_{IN} = 0.33µF, and C_{OUT} = 0.1µF. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperatire.)

SG7824A/SG7824

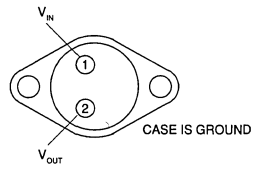
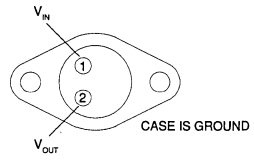
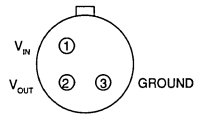
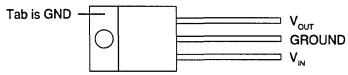
Parameter	Test Conditions	SG7824A			SG7824			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	23.6	24.0	24.4	23.0	24.0	25.0	V
Line Regulation (Note 1)	V_{IN} = 27V to 38V, T_J = 25°C		25	120		50	240	mV
	V_{IN} = 30V to 36V, T_J = 25°C		14	60		28	120	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		50	160		180	240	mV
	I_O = 250mA to 750mA, T_J = 25°C		25	80		70	120	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		25	80		25	120	mV
Total Output Voltage Tolerance	V_{IN} = 28V to 38V							
	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	23.3	24.0	24.7	22.8	24.0	25.2	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	23.3	24.0	24.7	22.8	24.0	25.2	V
Quiescent Current	Over Temperature Range			7			7	mA
	T_J = 25°C		4	6		4	6	mA
Quiescent Current Change	With Line: V_{IN} = 28V to 38V			0.8			0.8	mA
	With Load: I_O = 5mA to 1.0A (Power Pkgs.)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		2	2.5		2	2.5	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5	2.2	3.3	1.5	2.2	3.3	A
	T - Pkg: T_J = 25°C	0.5	0.9	1.7	0.5	0.9	1.7	A
Short Circuit Current	Power Pkgs: V_{IN} = 35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = 35V, T_J = 25°C			0.7			0.7	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	56			56			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)			40			40	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		96			96		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

SG7824AC/SG7824C

Parameter	Test Conditions	SG7824AC			SG7824C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	23.6	24.0	24.4	23.0	24.0	25.0	V
Line Regulation (Note 1)	V_{IN} = 27V to 38V, T_J = 25°C		25	240		50	480	mV
	V_{IN} = 30V to 36V, T_J = 25°C		14	120		28	240	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		50	240		180	480	mV
	I_O = 250mA to 750mA, T_J = 25°C		25	120		70	240	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		25	120		25	240	mV
Total Output Voltage Tolerance	V_{IN} = 28V to 38V							
	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	23.3	24.0	24.7	22.8	24.0	25.2	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	23.3	24.0	24.7	22.8	24.0	25.2	V
Quiescent Current	Over Temperature Range			7			8.5	mA
	T_J = 25°C		4	6		4	8	mA
Quiescent Current Change	With Line: V_{IN} = 28V to 38V			1.0			1.0	mA
	With Load: I_O = 5mA to 1.0A (Power Pkgs.)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		2	2.5		2	2.5	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5	2.2	3.3	1.5	2.2	3.3	A
	T - Pkg: T_J = 25°C	0.7	0.9	1.7	0.7	0.9	1.7	A
Short Circuit Current	Power Pkgs: V_{IN} = 35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = 35V, T_J = 25°C			0.7			0.7	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	56			56			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)			40			40	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		96			96		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

Note 1. All regulation tests are made at constant junction temperature with low duty cycle testing.
2. This test is guaranteed but is not tested in production.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
3-TERMINAL TO-3 METAL CAN K-PACKAGE	SG78XXAK/883B SG78XXAK SG78XXACK SG78XXK/883B SG78XXK SG78XXK	-55°C to 125°C -55°C to 125°C 0°C to 70C -55°C to 125°C -55°C to 125°C 0°C to 70°C	
3-TERMINAL TO-66 METAL CAN R-PACKAGE	SG78XXAR/883B SG78XXAR SG78XXACR SG78XXR/883B SG78XXR SG78XXCR	-55°C to 125°C -55°C to 125°C 0°C to 70°C -55°C to 125°C -55°C to 125°C 0°C to 70°C	
3-PIN TO-39 METAL CAN T-PACKAGE	SG78XXAT/883B SG78XXAT SG78XXACT SG78XXT/883B SG78XXT SG78XXCT	-55°C to 125°C -55°C to 125°C 0°C to 70°C -55°C to 125°C -55°C to 125°C 0°C to 70°C	
3-PIN HERMETIC TO-257 G-PACKAGE (Non-Isolated) 3-PIN HERMETIC TO-257 IG-PACKAGE (Isolated)	SG78XXAG/883B SG78XXAG SG78XXG/883B SG78XXG SG78XXAIG/883B SG78XXAIG SG78XXIG/883B SG78XXIG	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availability.
2. All parts are viewed from the top.
3. "XX" to be replaced by output voltage of specific fixed regulator.
4. Some products will be available in leadless chip carrier (LCC) and hermetic flat pack (F). Consult factory for price and availability

SG7900A/SG7900AC
SG7900/SG7900C

NEGATIVE FIXED VOLTAGE REGULATOR

DESCRIPTION

The SG7900A/SG7900 series of negative regulators offer self-contained, fixed-voltage capability with up to 1.5A of load current. With a variety of output voltages and four package options this regulator series is an optimum complement to the SG7800A/SG7800, SG140/SG340 line of three terminal regulators.

These units feature a unique band gap reference which allows the SG7900A series to be specified with an output voltage tolerance of ±1.5%. The SG7900A versions also offer much improved line regulation characteristics.

All protective features of thermal shutdown, current limiting, and safe-area control have been designed into these units and since these regulators require only a single output capacitor (SG7900 series) or a capacitor and 5mA minimum load (SG120 series) for satisfactory performance, ease of application is assured.

Although designed as fixed-voltage regulators, the output voltage can be increased through the use of a simple voltage divider. The low quiescent drain current of the device insures good regulation when this method is used, especially for the SG120 series.

These devices are available in hermetically sealed TO-257 (both isolated and non-isolated), TO-3, TO-39 and TO-66 power packages.

FEATURES

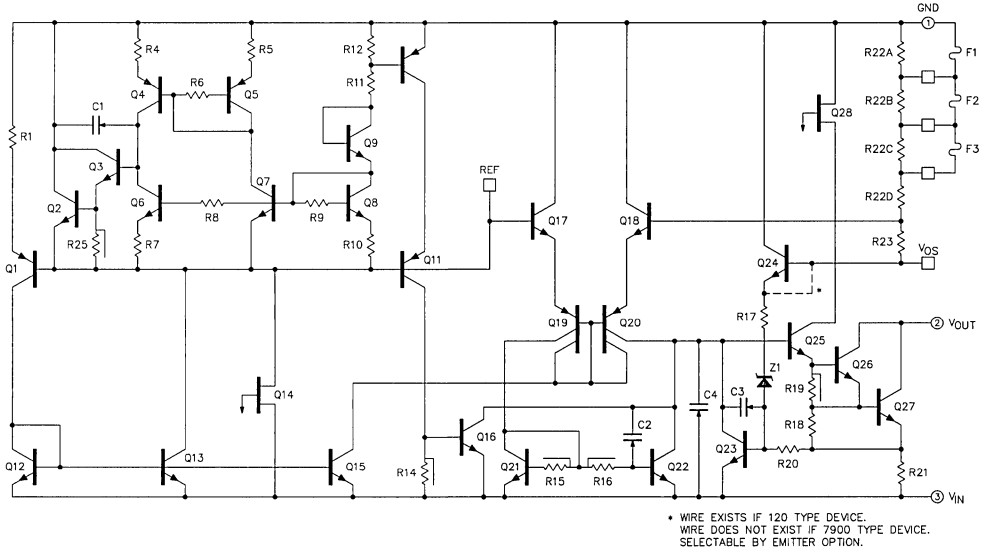
- **Output voltage set internally to ±1.5% on SG7900A**
- **Output current to 1.5A**
- **Excellent line and load regulation**
- **Foldback current limiting**
- **Thermal overload protection**
- **Voltages available: -5V, -5.2V, -8V, -12V, -15V, -18V, -20V**
- **Contact factory for other voltage options**

HIGH RELIABILITY FEATURES - SG7900A/SG7900

- **Available to MIL-STD - 883**
- **MIL-M38510/11501BXA - JAN7905T**
- **MIL-M38510/11505BYA - JAN7905K**
- **MIL-M38510/11506BYA - JAN7912K**
- **MIL-M38510/11507BYA - JAN7915K**
- **Scheduled for MIL-M-38510 QPL listing**
- **Radiation data available**
- **SG level "S" processing available**

4

SCHEMATIC DIAGRAM



April 1990

ABSOLUTE MAXIMUM RATINGS (Note 1)

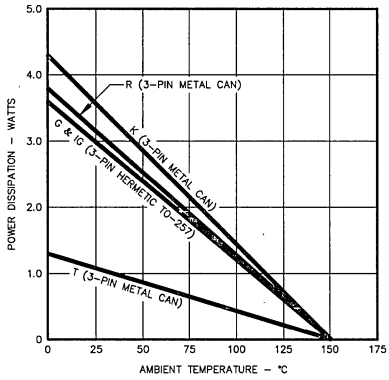
Device Output Voltage	Input Voltage	Input Voltage Differential (Output shorted to ground)
-5V	-35V	35V
-5.2V	-35V	35V
-8V	-35V	35V
-12V	-35V	35V
-15V	-40V	35V
-18V	-40V	35V
-20V	-40V	35V

Operating Junction Temperature
Hermetic (K, R, T, G, IG - Packages) ..... 150°C

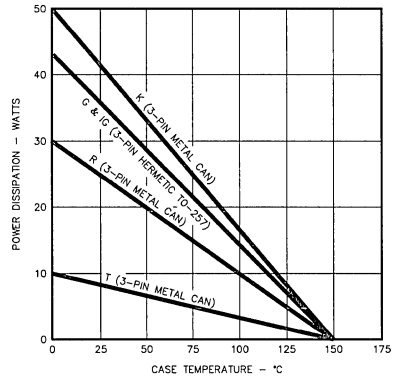
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Values beyond which damage may occur.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Operating Junction Temperature Range:
SG7900A/7900 ..... -55°C to 150°C
SG7900AC/7900C ..... 0°C to 125°C

Note 2. Range over which the device is functional.

CHARACTERISTIC CURVES

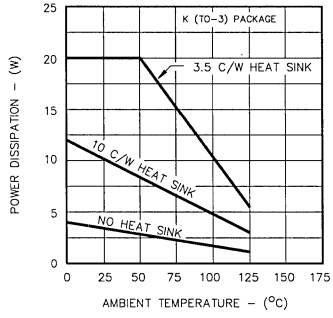


FIGURE 1.
MAXIMUM AVERAGE POWER DISSIPATION

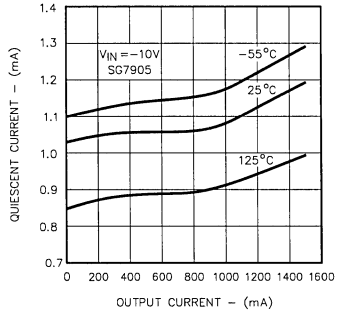


FIGURE 2.
QUIESCENT CURRENT VS. LOAD

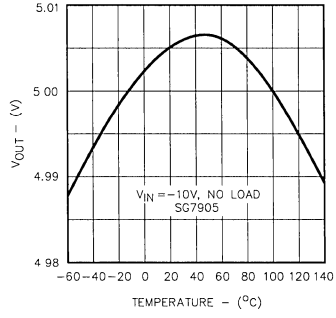


FIGURE 3.
TEMPERATURE COEFFICIENT

CHARACTERISTIC CURVES (continued)

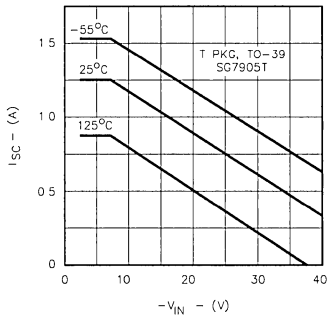


FIGURE 4.
SHORTCIRCUIT CURRENT VS. V_{IN}

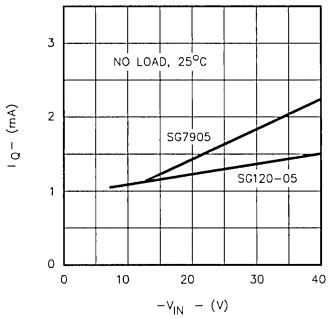


FIGURE 5.
QUIESCENT CURRENT VS. V_{IN}

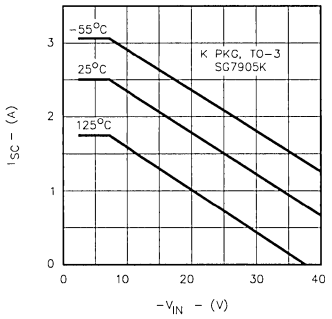


FIGURE 6.
SHORT CIRCUIT CURRENT VS. V_{IN}

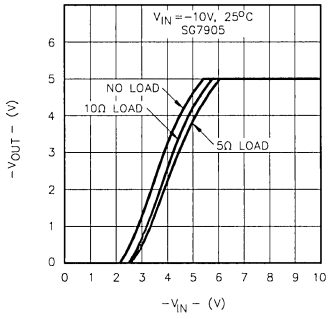


FIGURE 7.
DROPOUT CHARACTERISTICS

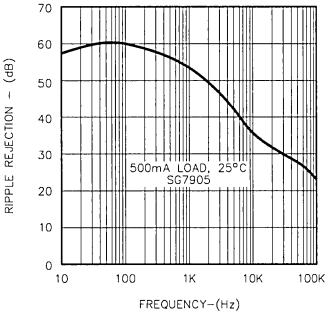


FIGURE 8.
RIPPLE REJECTION VS. FREQUENCY

APPLICATIONS

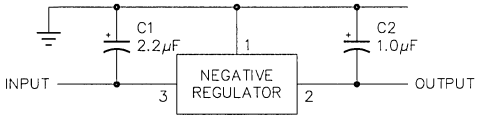


FIGURE 9 - FIXED OUTPUT REGULATOR

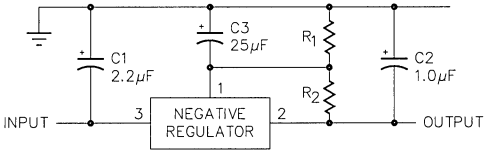


FIGURE 10 - CIRCUIT FOR INCREASING OUTPUT VOLTAGE

NOTE: 1. C1 is required only if regulator is separated from rectifier filter.
2. Both C1 and C2 should be low E.S.R. types such as solid tantalum. If aluminum electrolitics are used, at least 10 times values shown should be selected.
3. If large output capacities are used, the regulators must be protected from momentary input shorts. A high current diode

NOTE: C3 optional for improved transient response and ripple rejec-

$$V_{OUT} = V\,(REGULATOR)\frac{R_1 + R_2}{R_1} \qquad R_2 = \frac{V(REG)}{15mA}$$

ELECTRICAL SPECIFICATIONS (Note 1)

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG7905A/SG7905 with -55°C ≤ T_A ≤ 150°C, SG7905AC/SG7905C with 0°C ≤ T_A ≤ 125°C, V_{IN} = -10V, I_O = 500mA for the K, R, G and IG -Power Packages-, I_O = 100mA for the T package, C_{IN} = 2µF, and C_{OUT} = 1.0µF. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

SG7905A/SG7905

Parameter	Test Conditions	SG7905A			SG7905			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	-4.92	-5.00	-5.08	-4.8	-5.0	-5.2	V
Line Regulation (Note 1)	V_{IN} = -7.5V to -25V, T_J = 25°C		5	25		3	50	mV
	V_{IN} = -8V to -12V, T_J = 25°C		3	12		1	25	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		15	75		15	100	mV
	I_O = 250mA to 750mA, T_J = 25°C		15	25		15	25	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		5	30		5	100	mV
Total Output Voltage Tolerance	V_{IN} = -8V to -20V							
	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	-4.85	-5.00	-5.15	-4.70	-5.00	-5.30	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	-4.85	-5.00	-5.15	-4.70	-5.00	-5.30	V
Quiescent Current	Over Temperature Range			2.5			2.5	mA
	T_J = 25°C			2.0			2.0	mA
Quiescent Current Change	with Line: V_{IN} = -8V to -25V			1.3			1.3	mA
	with Load: I_O = 5mA to 1.0A (Power Packages)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		1.1	2.3		1.1	2.3	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5		3.3	1.5		3.3	A
	T - Pkg: T_J = 25°C	0.5		1.4	0.5		1.4	A
Short Circuit Current	Power Pkgs: V_{IN} = -35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = -35V, T_J = 25°C			0.6			0.6	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	54			54			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)		25	80		25	80	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		20			20		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

SG7905AC/SG7905C

Parameter	Test Conditions	SG7905AC			SG7905C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	-4.92	-5.00	-5.08	-4.8	-5.0	-5.2	V
Line Regulation (Note 1)	V_{IN} = -7.5V to -25V, T_J = 25°C		5	40		3	100	mV
	V_{IN} = -8V to -12V, T_J = 25°C		3	25		1	50	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		15	75		15	100	mV
	I_O = 250mA to 750mA, T_J = 25°C		5	50		5	50	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		5	50		15	100	mV
Total Output Voltage Tolerance	V_{IN} = -8V to -20V							
	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	-4.85	-5.00	-5.15	-4.75	-5.00	-5.25	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	-4.85	-5.00	-5.15	-4.75	-5.00	-5.25	V
Quiescent Current	Over Temperature Range			2.5			3.0	mA
	T_J = 25°C			2.0			2.0	mA
Quiescent Current Change	with Line: V_{IN} = -8V to -25V			1.3			1.3	mA
	with Load: I_O = 5mA to 1.0A (Power Packages)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		1.1	2.3		1.1	2.3	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5		3.3	1.5		3.3	A
	T - Pkg: T_J = 25°C	0.5		1.4	0.5		1.4	A
Short Circuit Current	Power Pkgs: V_{IN} = -35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = -35V, T_J = 25°C			0.6			0.6	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	54			54			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)		25	80		25	80	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		20			20		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

Note 1. All regulation tests are made at constant junction temperature with low duty cycle testing.
2. This test is guaranteed but is not tested in production.

ELECTRICAL SPECIFICATIONS (Note 1)

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG7905.2A/7905.2 with -55°C ≤ T_A ≤ 150°C, SG7905.2AC/7905.2C with 0°C ≤ T_A ≤ 125°C, V_{IN} = -10V, I_O = 500mA for the K, R, G and IG -Power Packages-, I_O = 100mA for the T package, C_{IN} = 2µF, and C_{OUT} = 1.0µF. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

SG7905.2A/SG7905.2

Parameter	Test Conditions	SG7905.2A			SG7905.2			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	-5.12	-5.20	-5.28	-5.0	-5.2	-5.4	V
Line Regulation (Note 1)	V_{IN} = -7.7V to -25V, T_J = 25°C		5	25		5	50	mV
	V_{IN} = -8V to -12V, T_J = 25°C		3	15		3	25	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		15	75		15	100	mV
	I_O = 250mA to 750mA, T_J = 25°C		5	25		5	30	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		5	30		5	100	mV
Total Output Voltage Tolerance	V_{IN} = -8.2V to -20V							
	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	-5.05	-5.20	-5.35	-4.90	-5.20	-5.50	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	-5.05	-5.20	-5.35	-4.90	-5.20	-5.50	V
Quiescent Current	Over Temperature Range			2.5			2.5	mA
	T_J = 25°C			2.0			2.0	mA
Quiescent Current Change	with Line: V_{IN} = -8.2V to -25V			1.3			1.3	mA
	with Load: I_O = 5mA to 1.0A (Power Packages)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		1.1	2.3		1.1	2.3	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5		3.3	1.5		3.3	A
	T - Pkg: T_J = 25°C	0.5		1.4	0.5		1.4	A
Short Circuit Current	Power Pkgs: V_{IN} = -35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = -35V, T_J = 25°C			0.6			0.6	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	54			54			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)		25	80		25	80	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		24			24		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

SG7905.2AC/SG7905.2C

Parameter	Test Conditions	SG7905.2AC			SG7905.2C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	-5.12	-5.20	-5.28	-5.0	-5.2	-5.4	V
Line Regulation (Note 1)	V_{IN} = -7.7V to -25V, T_J = 25°C		5	40		10	50	mV
	V_{IN} = -8V to -12V, T_J = 25°C		3	25		5	25	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		15	75		15	100	mV
	I_O = 250mA to 750mA, T_J = 25°C		5	50		5	50	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		5	50		5	100	mV
Total Output Voltage Tolerance	V_{IN} = -8.2V to -20V							
	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	-5.05	-5.20	-5.35	-4.95	-5.20	-5.45	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	-5.05	-5.20	-5.35	-4.95	-5.20	-5.45	V
Quiescent Current	Over Temperature Range			2.5			3.1	mA
	T_J = 25°C			2.0			2.0	mA
Quiescent Current Change	with Line: V_{IN} = -8.2V to -20V			1.3			1.3	mA
	with Load: I_O = 5mA to 1.0A (Power Packages)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		1.1	2.3		1.1	2.3	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5		3.3	1.5		3.3	A
	T - Pkg: T_J = 25°C	0.5		1.4	0.5		1.4	A
Short Circuit Current	Power Pkgs: V_{IN} = -35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = -35V, T_J = 25°C			0.6			0.6	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	54			54			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)		25	80		25	80	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		24			24		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

Note 1. All regulation tests are made at constant junction temperature with low duty cycle testing.
2. This test is guaranteed but is not tested in production.

ELECTRICAL SPECIFICATIONS (Note 1)

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG7908A/SG7908 with -55°C ≤ T_A ≤ 150°C, SG7908AC/SG7908C with 0°C ≤ T_A ≤ 125°C, V_{IN} = -14V, I_O = 500mA for the K, R, G and IG -Power Packages-, I_O = 100mA for the T package, C_{IN} = 2µF, and C_{OUT} = 1.0µF. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

SG7908A/SG7908

Parameter	Test Conditions	SG7908A			SG7908			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	-7.88	-8.00	-8.12	-7.7	-8.0	-8.3	V
Line Regulation (Note 1)	V_{IN} = -10.5V to -25V, T_J = 25°C		6	40		6	80	mV
	V_{IN} = -11V to -17V, T_J = 25°C		2	20		2	40	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		12	80		12	100	mV
	I_O = 250mA to 750mA, T_J = 25°C		4	30		4	40	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		10	30		10	160	mV
Total Output Voltage Tolerance	V_{IN} = -11.5V to -23V							
	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	-7.76	-8.00	-8.24	-7.6	-8.0	-8.4	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	-7.76	-8.00	-8.24	-7.6	-8.0	-8.4	V
Quiescent Current	Over Temperature Range			2.5			2.5	mA
	T_J = 25°C			2.0			2.0	mA
Quiescent Current Change	with Line: V_{IN} = -11.5V to -25V			1.0			1.0	mA
	with Load: I_O = 5mA to 1.0A (Power Packages)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		1.1	2.3		1.1	2.3	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5		3.3	1.5		3.3	A
	T - Pkg: T_J = 25°C	0.5		1.4	0.5		1.4	A
Short Circuit Current	Power Pkgs: V_{IN} = -35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = -35V, T_J = 25°C			0.6			0.6	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	54			54			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)		25	80		25	80	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		32			32		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

SG7908AC/SG7908C

Parameter	Test Conditions	SG7908AC			SG7908C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	-7.88	-8.00	-8.12	-7.7	-8.0	-8.3	V
Line Regulation (Note 1)	V_{IN} = -10.5V to -25V, T_J = 25°C		6	40		6	160	mV
	V_{IN} = -11V to -17V, T_J = 25°C		4	25		2	80	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		12	100		12	160	mV
	I_O = 250mA to 750mA, T_J = 25°C		10	50		4	80	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		10	40		10	160	mV
Total Output Voltage Tolerance	V_{IN} = -11.5V to -23V							
	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	-7.76	-8.00	-8.24	-7.6	-8.0	-8.4	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	-7.76	-8.00	-8.24	-7.6	-8.0	-8.4	V
Quiescent Current	Over Temperature Range			2.5			3.0	mA
	T_J = 25°C			2.0			2.0	mA
Quiescent Current Change	with Line: V_{IN} = -11.5V to -25V			1.0			1.0	mA
	with Load: I_O = 5mA to 1.0A (Power Packages)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		1.1	2.3		1.1	2.3	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5		3.3	1.5		3.3	A
	T - Pkg: T_J = 25°C	0.5		1.4	0.5		1.4	A
Short Circuit Current	Power Pkgs: V_{IN} = -35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = -35V, T_J = 25°C			0.6			0.6	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	54			54			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)		25	80		25	80	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		32			32		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

Note 1. All regulation tests are made at constant junction temperature with low duty cycle testing.
2. This test is guaranteed but is not tested in production.

ELECTRICAL SPECIFICATIONS (Note 1)

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG7912A/SG7912 with -55°C ≤ T_A ≤ 150°C, SG7912AC/SG7912C with 0°C ≤ T_A ≤ 125°C, V_{IN} = -19V, I_O = 500mA for the K, R, G and IG -Power Packages-, I_O = 100mA for the T package, C_{IN} = 2µF, and C_{OUT} = 1.0µF. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

SG7912A/SG7912

Parameter	Test Conditions	SG7912A			SG7912			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	-11.8	-12.0	-12.2	-11.5	-12.0	-12.5	V
Line Regulation (Note 1)	V_{IN} = -14.5V to -30V, T_J = 25°C		4	60		10	120	mV
	V_{IN} = -16V to -22V, T_J = 25°C		3	30		3	60	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		20	90		12	120	mV
	I_O = 250mA to 750mA, T_J = 25°C		10	40		4	60	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		10	40		10	240	mV
Total Output Voltage Tolerance	V_{IN} = -14.5V to -27V							
	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	-11.7	-12.0	-12.3	-11.4	-12.0	-12.6	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	-11.7	-12.0	-12.3	-11.4	-12.0	-12.6	V
Quiescent Current	Over Temperature Range			4			4	mA
	T_J = 25°C			3			3	mA
Quiescent Current Change	with Line: V_{IN} = -14.5V to -30V			1.0			1.0	mA
	with Load: I_O = 5mA to 1.0A (Power Packages)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		1.1	2.3		1.1	2.3	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5		3.3	1.5		3.3	A
	T - Pkg: T_J = 25°C	0.5		1.4	0.5		1.4	A
Short Circuit Current	Power Pkgs: V_{IN} = -35V, T_J = 25°C			1.2			0.2	A
	T - Pkg: V_{IN} = -35V, T_J = 25°C			0.6			0.6	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	54			54			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)		25	80		25	80	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		60			60		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

SG7912AC/SG7912C

Parameter	Test Conditions	SG7912AC			SG7912C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	-11.8	-12.0	-12.2	-11.5	-12.0	-12.5	V
Line Regulation (Note 1)	V_{IN} = -14.5V to -30V, T_J = 25°C		4	70		10	240	mV
	V_{IN} = -16V to -22V, T_J = 25°C		3	40		3	120	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		20	100		12	240	mV
	I_O = 250mA to 750mA, T_J = 25°C		10	50		4	120	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		10	50		10	240	mV
Total Output Voltage Tolerance	V_{IN} = -14.5V to -27V							
	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	-11.7	-12.0	-12.3	-11.4	-12.0	-12.6	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	-11.7	-12.0	-12.3	-11.4	-12.0	-12.6	V
Quiescent Current	Over Temperature Range			4			4	mA
	T_J = 25°C			3			3	mA
Quiescent Current Change	with Line: V_{IN} = -14.5V to -30V			1.0			1.0	mA
	with Load: I_O = 5mA to 1.0A (Power Packages)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		1.1	2.3		1.1	2.3	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5		3.3	1.5		3.3	A
	T - Pkg: T_J = 25°C	0.5		1.4	0.5		1.4	A
Short Circuit Current	Power Pkgs: V_{IN} = -35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = -35V, T_J = 25°C			0.6			0.6	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	54			54			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)		25	80		25	80	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		60			60		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

Note 1. All regulation tests are made at constant junction temperature with low duty cycle testing.
2. This test is guaranteed but is not tested in production.

ELECTRICAL SPECIFICATIONS (Note 1)

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG7915A/SG7915 with -55°C ≤ T_A ≤ 150°C, SG7915AC/SG7915C with 0°C ≤ T_A ≤ 125°C, V_{IN} = -23V, I_O = 500mA for the K, R, G and IG -Power Packages-, I_O = 100mA for the T package, C_{IN} = 2µF, and C_{OUT} = 1.0µF. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

SG7915A/SG7915

Parameter	Test Conditions	SG7915A			SG7915			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	-14.8	-15.0	-15.2	-14.4	-15.0	-15.6	V
Line Regulation (Note 1)	V_{IN} = -17.5V to -30V, T_J = 25°C		5	75		11	150	mV
	V_{IN} = -20V to -25V, T_J = 25°C		3	40		3	75	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		30	100		12	150	mV
	I_O = 250mA to 750mA, T_J = 25°C		4	50		4	75	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		10	50		10	240	mV
Total Output Voltage Tolerance	V_{IN} = -18.5V to -30V							
	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	-14.6	-15.0	-15.4	-14.25	-15.00	-15.75	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	-14.6	-15.0	-15.4	-14.25	-15.00	-15.75	V
Quiescent Current	Over Temperature Range			4			4	mA
	T_J = 25°C			3			3	mA
Quiescent Current Change	with Line: V_{IN} = -18.5V to -30V			1.0			1.0	mA
	with Load: I_O = 5mA to 1.0A (Power Packages)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		1.1	2.3		1.1	2.3	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5		3.3	1.5		3.3	A
	T - Pkg: T_J = 25°C	0.5		1.4	0.5		1.4	A
Short Circuit Current	Power Pkgs: V_{IN} = -35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = -35V, T_J = 25°C			0.6			0.6	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	54			54			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)		25	80		25	80	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		60			60		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

SG7915AC/SG7915C

Parameter	Test Conditions	SG7915AC			SG7915C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	-14.8	-15.0	-15.2	-14.4	-15.0	-15.6	V
Line Regulation (Note 1)	V_{IN} = -17.5V to -30V, T_J = 25°C		5	90		12	300	mV
	V_{IN} = -20V to -25V, T_J = 25°C		4	50		3	150	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		30	130		12	300	mV
	I_O = 250mA to 750mA, T_J = 25°C		4	60		4	150	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		10	60		10	240	mV
Total Output Voltage Tolerance	V_{IN} = -18.5V to -30V							
	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	-14.6	-15.0	-15.4	-14.25	-15.00	-15.75	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	-14.6	-15.0	-15.4	-14.25	-15.00	-15.75	V
Quiescent Current	Over Temperature Range			4			4	mA
	T_J = 25°C			3			3	mA
Quiescent Current Change	with Line: V_{IN} = -18.5V to -30V			1.0			1.0	mA
	with Load: I_O = 5mA to 1.0A (Power Packages)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		1.1	2.3		1.1	2.3	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5		3.3	1.5		3.3	A
	T - Pkg: T_J = 25°C	0.5		1.4	0.5		1.4	A
Short Circuit Current	Power Pkgs: V_{IN} = -35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = -35V, T_J = 25°C			0.6			0.6	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	54			54			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)		25	80		25	80	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		60			60		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

Note 1. All regulation tests are made at constant junction temperature with low duty cycle testing.
2. This test is guaranteed but is not tested in production.

ELECTRICAL SPECIFICATIONS (Note 1)

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG7918A/SG7918 with -55°C ≤ T_A ≤ 150°C, SG7918AC/SG7918C with 0°C ≤ T_A ≤ 125°C, V_{IN} = -27V, I_O = 500mA for the K, R, G and IG -Power Packages-, I_O = 100mA for the T package, C_{IN} = 2µF, and C_{OUT} = 1.0µF. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

SG7918A/SG7918

Parameter	Test Conditions	SG7918A			SG7918			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	-17.7	-18.0	-18.3	-17.3	-18.0	-18.7	V
Line Regulation (Note 1)	V_{IN} = -21V to -33V, T_J = 25°C		5	90		6	180	mV
	V_{IN} = -24V to -30V, T_J = 25°C		3	50		3	75	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		30	120		12	180	mV
	I_O = 250mA to 750mA, T_J = 25°C		4	60		4	90	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		10	60		10	240	mV
Total Output Voltage Tolerance	V_{IN} = -22V to -33V							
	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	-17.5	-18.0	-18.5	-17.1	-18.0	-18.9	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	-17.5	-18.0	-18.5	-17.1	-18.0	-18.9	V
Quiescent Current	Over Temperature Range			4			4	mA
	T_J = 25°C			3			3	mA
Quiescent Current Change	with Line: V_{IN} = -21V to -33V			1.0			1.0	mA
	with Load: I_O = 5mA to 1.0A (Power Packages)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		1.1	2.3		1.1	2.3	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5		3.3	1.5		3.3	A
	T - Pkg: T_J = 25°C	0.5		1.4	0.5		1.4	A
Short Circuit Current	Power Pkgs: V_{IN} = -35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = -35V, T_J = 25°C			0.6			0.6	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	54			54			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)		25	80		25	80	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		72			72		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

SG7918AC/SG7918C

Parameter	Test Conditions	SG7918AC			SG7918C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	-17.7	-18.0	-18.3	-17.4	-18.0	-18.6	V
Line Regulation (Note 1)	V_{IN} = -21V to -33V, T_J = 25°C		5	100		12	300	mV
	V_{IN} = -24V to -30V, T_J = 25°C		4	60		3	150	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		30	130		12	360	mV
	I_O = 250mA to 750mA, T_J = 25°C		4	70		4	180	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		10	70		10	300	mV
Total Output Voltage Tolerance	V_{IN} = -22V to -33V							
	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	-17.5	-18.0	-18.5	-17.1	-18.0	-18.9	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	-17.5	-18.0	-18.5	-17.1	-18.0	-18.9	V
Quiescent Current	Over Temperature Range			4			4	mA
	T_J = 25°C			3			3	mA
Quiescent Current Change	with Line: V_{IN} = -21V to -33V			1.0			1.0	mA
	with Load: I_O = 5mA to 1.0A (Power Packages)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		1.1	2.3		1.1	2.3	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5		3.3	1.5		3.3	A
	T - Pkg: T_J = 25°C	0.5		1.4	0.5		1.4	A
Short Circuit Current	Power Pkgs: V_{IN} = -35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = -35V, T_J = 25°C			0.6			0.6	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	54			54			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)		25	80		25	80	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		72			72		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

Note 1. All regulation tests are made at constant junction temperature with low duty cycle testing.
2. This test is guaranteed but is not tested in production.

ELECTRICAL SPECIFICATIONS (Note 1)

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG7920A/SG7920 with -55°C ≤ T_A ≤ 150°C, SG7920AC/SG7920C with 0°C ≤ T_A ≤ 125°C, V_{IN} = -29V, I_O = 500mA for the K, R, G and IG -Power Packages-, I_O = 100mA for the T package, C_{IN} = 2µF, and C_{OUT} = 1.0µF. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

SG7920A/SG7920

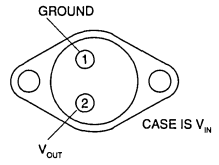
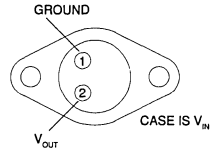
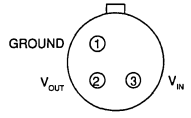
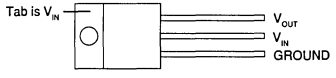
Parameter	Test Conditions	SG7920A			SG7920			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	-19.7	-20.0	-20.3	-19.2	-20.0	-20.8	V
Line Regulation (Note 1)	V_{IN} = -23V to -35V, T_J = 25°C		5	100		11	150	mV
	V_{IN} = -26V to -32V, T_J = 25°C		4	60		3	75	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		30	120		12	200	mV
	I_O = 250mA to 750mA, T_J = 25°C		4	70		4	100	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		10	70		10	240	mV
Total Output Voltage Tolerance	V_{IN} = -24V to -35V							
	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	-19.4	-20.0	-20.6	-19.0	-20.0	-21.0	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	-19.4	-20.0	-20.6	-19.0	-20.0	-21.0	V
Quiescent Current	Over Temperature Range			4			4	mA
	T_J = 25°C			3			3	mA
Quiescent Current Change	with Line: V_{IN} = -24V to -35V			1.0			1.0	mA
	with Load: I_O = 5mA to 1.0A (Power Packages)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		1.1	2.3		1.1	2.3	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5		3.3	1.5		3.3	A
	T - Pkg: T_J = 25°C	0.5		1.4	0.5		1.4	A
Short Circuit Current	Power Pkgs: V_{IN} = -35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = -35V, T_J = 25°C			0.6			0.6	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	54			54			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)		25	80		25	80	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		80			80		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

SG7920AC/SG7920C

Parameter	Test Conditions	SG7920AC			SG7920C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_J = 25°C	-19.7	-20.0	-20.3	-19.2	-20.0	-20.8	V
Line Regulation (Note 1)	V_{IN} = -23V to -35V, T_J = 25°C		6	120		11	300	mV
	V_{IN} = -26V to -32V, T_J = 25°C		4	70		3	150	mV
Load Regulation (Note 1)	Power Pkgs: I_O = 5mA to 1.5A, T_J = 25°C		30	140		12	400	mV
	I_O = 250mA to 750mA, T_J = 25°C		4	80		10	200	mV
	T - Pkg: I_O = 5mA to 500mA, T_J = 25°C		10	80		10	300	mV
Total Output Voltage Tolerance	V_{IN} = -24V to -35V							
	Power Pkgs: I_O = 5mA to 1.0A, P ≤ 20W	-19.4	-20.0	-20.6	-19.0	-20.0	-21.0	V
	T - Pkg: I_O = 5mA to 500mA, P ≤ 2W	-19.4	-20.0	-20.6	-19.0	-20.0	-21.0	V
Quiescent Current	Over Temperature Range			4			4	mA
	T_J = 25°C			3			3	mA
Quiescent Current Change	with Line: V_{IN} = -24V to -35V			1.0			1.0	mA
	with Load: I_O = 5mA to 1.0A (Power Packages)			0.5			0.5	mA
	I_O = 5mA to 500mA (T)			0.5			0.5	mA
Dropout Voltage	ΔV_O = 100mV, T_J = 25°C							
	Power Pkgs: I_O = 1.0A, T - Pkg: I_O = 500mA		1.1	2.3		1.1	2.3	V
Peak Output Current	Power Pkgs: T_J = 25°C	1.5		3.3	1.5		3.3	A
	T - Pkg: T_J = 25°C	0.5		1.4	0.5		1.4	A
Short Circuit Current	Power Pkgs: V_{IN} = -35V, T_J = 25°C			1.2			1.2	A
	T - Pkg: V_{IN} = -35V, T_J = 25°C			0.6			0.6	A
Ripple Rejection	ΔV_{IN} = 10V, f = 120Hz, T_J = 25°C	54			54			dB
Output Noise Voltage (rms)	f = 10Hz to 100KHz (Note 2)		25	80		25	80	µV/V
Long Term Stability	1000hrs. at T_J = 125°C		80			80		mV
Thermal Shutdown	I_O = 5mA		175			175		°C

Note 1. All regulation tests are made at constant junction temperature with low duty cycle testing.
2. This test is guaranteed but is not tested in production.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
3-TERMINAL TO-3 METAL CAN K-PACKAGE	SG79XXAK/883B SG79XXAK SG79XXACK SG79XXK/883B SG79XXK SG79XXK	-55°C to 125°C -55°C to 125°C 0°C to 70C -55°C to 125°C -55°C to 125°C 0°C to 70°C	
3-TERMINAL TO-66 METAL CAN R-PACKAGE	SG79XXAR/883B SG79XXAR SG79XXACR SG79XXR/883B SG79XXR SG79XXCR	-55°C to 125°C -55°C to 125°C 0°C to 70°C -55°C to 125°C -55°C to 125°C 0°C to 70°C	
3-PIN TO-39 METAL CAN T-PACKAGE	SG79XXAT/883B SG79XXAT SG79XXACT SG79XXT/883B SG79XXT SG79XXCT	-55°C to 125°C -55°C to 125°C 0°C to 70°C -55°C to 125°C -55°C to 125°C 0°C to 70°C	
3-PIN HERMETIC TO-257 G-PACKAGE (Non-Isolated) 3-PIN HERMETIC TO-257 IG-PACKAGE (Isolated)	SG79XXAG/883B SG79XXAG SG79XXG/883B SG79XXG SG79XXAIG/883B SG79XXAIG SG79XXIG/883B SG79XXIG	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availability.
2. All parts are viewed from the top.
3. "XX" to be replaced by output voltage of specific fixed regulator.
4. Some products will be available in leadless chip carrier (LCC) and hermetic flat pack (F). Consult factory for price and availability

SM600/SM601/SM602/SM610/SM611/SM612

SWITCHING REGULATOR POWER OUTPUT STAGES

DESCRIPTION

The SM600/601/602 and SM610/611/612 series of Power Output Stages are especially designed to be driven with standard PWM integrated circuits to form an efficient switching power supply. The SM600, SM601 and SM602 are optimized for non-isolated Buck and Buck-Boost application, where SM610, SM611 and SM612 are best suited for DC-DC Boost type applications as well as negative output Buck Converters. The hybrid circuit construction utilizes thick film resistors on a beryllia substrate for maximum thermal conductivity and resultant low thermal impedance. All of the active elements in the hybrid are fully passivated.

FEATURES

- **Equivalent to the Unitrode PIC 600, 601, 602, 610, 611, 612**
- **5A current capability**
- **Designed and characterized for switching regulator applications such as Buck, Boost, and Buck-Boost type**
- **Cost saving design reduces size, improves efficiency, reduces noise and RFI**
- **High operating efficiency at 2A typical performance -**
  Rise and fall time < 75ns
  Efficiency > 85%
- **Electrically isolated, 4-pin, TO-66 hermetic case**

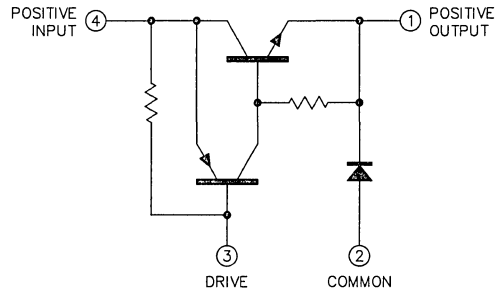
HIGH RELIABILITY FEATURES

- **Available with high reliability processing**

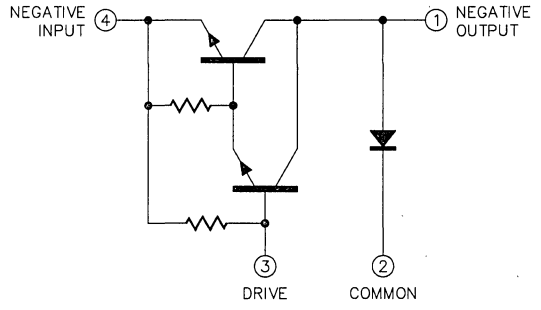
4

FUNCTIONAL DIAGRAM

SM600/SM601/SM602



SM610/SM611/SM612



ABSOLUTE MAXIMUM RATINGS (Note 1)

	SM600	SM601	SM602	SM610	SM611	SM612
Input Voltage, V_{4-2}	60V	80V	100V	-60V	-80V	-100V
Output Voltage, V_{1-2}	60V	80V	100V	-60V	-80V	-100V
Drive Input Reverse Voltage, V_{3-4}	5V	5V	5V	-5V	-5V	-5V
Output Current, I_1	5A	5A	5A	-5A	-5A	-5A
Drive Current, I_3	-0.2A	-0.2A	-0.2A	0.2A	0.2A	0.2A

Thermal Resistance
- Power Switch, θ_{J-C} ..... 4.0°C/W
- Commutating Diode ..... 4.0°C/W
- Case to Ambient, θ_{C-A} ..... 60.0°C/W

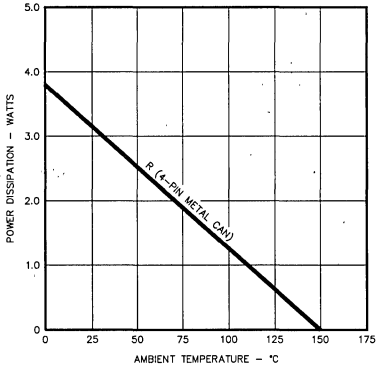
Operating Junction Temperature
- Hermetic (R Package) ..... 150°C

Storage Temperature Range ..... -65°C to 150°C

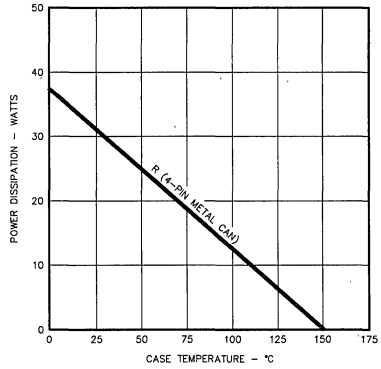
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

	SM600	SM601	SM602	SM610	SM611	SM612
Input Voltage, V_{4-2}	50V	70V	90V	-50V	-70V	-90V
Output Voltage, V_{1-2}	50V	70V	90V	-50V	-70V	-90V
Drive Input Reverse Voltage, V_{3-4}	3V	3V	3V	-3V	-3V	-3V
Output Current, I_1	4A	4A	4A	-4A	-4A	-4A
Drive Current, I_3	-0.1A	-0.1A	-0.1A	0.1A	0.1A	0.1A

Operating Ambient Temperature Range
- SM6XXR ..... 0°C to 70°C
- SM6XXHRR ..... -55°C to 125°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply for the operating ambient temperature of T_A = 25°C.. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG600/601/602			SG610/611/612			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
On-State Voltage (Note 3)	I_4 = 2A(-2A), I_3 = -20mA (20mA)		1.0	1.5		-1.0	-1.5	V
	I_4 = 5A(-5A), I_3 = -20mA (20mA)		2.5	3.5		-2.5	-3.5	V
Diode Forward Voltage (Note 3)	I_4 = 2A(-2A)		0.8	1.0		-0.8	-1.0	V
	I_4 = 5A(-5A)		1.0	1.5		-1.0	-1.5	V
Off-State Current	V_4 = Rated input voltage		0.1	10		-0.1	-10	µA
	V_4 = Rated input voltage, T_A = 125°C		10			-10		µA
Diode Reverse Current	V_1 = Rated output voltage		1.0	10		-1.0	-10	µA
	V_1 = Rated output voltage, T_A = 125°C		500			-500		µA

Note 3. Pulse test: Duration = 300µs, Duty Cycle ≤ 2%.

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG600/601/602			SG610/611/612			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Dynamic Characteristics (See Figures 1 & 2) (Notes 4 & 5)								
Current Delay Time			20	40		20	40	ns
Current Rise Time			50	75		50	75	ns
Voltage Rise Time			30	50		30	50	ns
Voltage Storage Time			450			450		ns
Voltage Fall Time			50	75		50	75	ns
Current Fall Time			70	150		70	150	ns
Efficiency (Note 5)			85			85		%

AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS (Note 6)

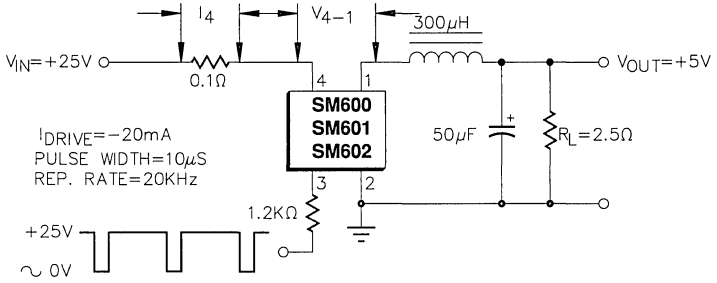


FIGURE 1 - SM600/601/602 SWITCHING SPEED CIRCUIT

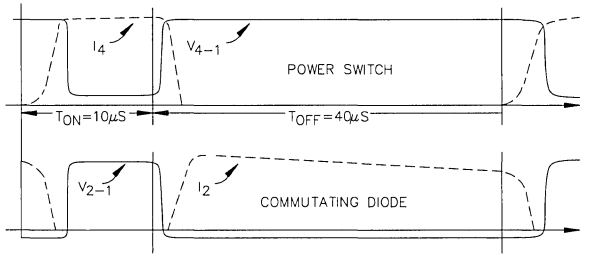


FIGURE 2 - SM600/601/602 SWITCHING WAVEFORMS

Note 4. In switching an inductive load, the current will lead the voltage on turn-on and lag the voltage on turn-off (see Figure 2). Therefore, Voltage Delay Time (t_{pv}) $\cong t_{ri} + t_n$ and Current Storage Time (t_{si}) $\cong t_{sv} + t_{fv}$.

Note 5. The efficiency is a measure of internal power losses and is equal to Output Power divided by Input Power. The switching speed circuit of Figure 1, in which the efficiency measured, is represenative of typical operating conditions for the SM600 series switching regulators.

Note 6. SM610/611/612 Test Circuit and waveforms are identical but of opposite polarity (V_{IN} = -25V, V_{OUT} = -5V, I_{DRIVE} = +20mA).

APPLICATION CIRCUITS

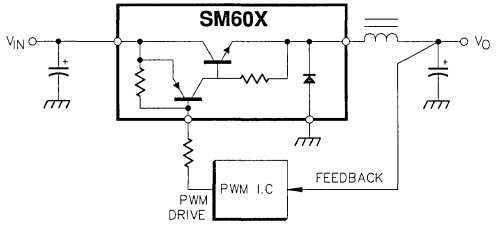


FIGURE 3 - STEP DOWN (BUCK) CONVERTER

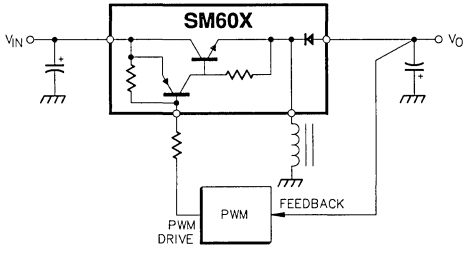


FIGURE 4 - NEGATIVE OUTPUT DOWN/UP (BUCK-BOOST) CONVERTER

APPLICATION CIRCUITS (continued)

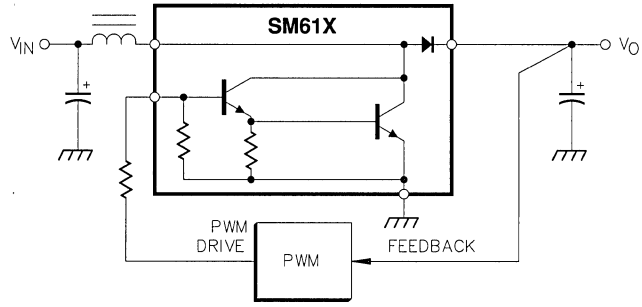
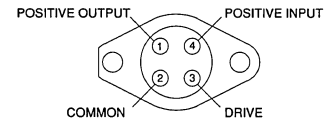
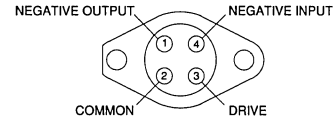


FIGURE 5 - STEP UP (BOOST) CONVERTER

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Note Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
4-PIN TO-66 METAL CAN R - PACKAGE	SM600R SM600HRR SM601R SM601HRR SM602R SM602HRR	0°C to 70°C -55°C to 125°C 0°C to 70°C -55°C to 125°C 0°C to 70°C -55°C to 125°C	
	SM610R SM610HRR SM611R SM611HRR SM612R SM612HRR	0°C to 70°C -55°C to 125°C 0°C to 70°C -55°C to 125°C 0°C to 70°C -55°C to 125°C	

Note 1. All packages are viewed from the top.
2. Case is electrically isolated.
3. Consult factory for additional screening available.

SM625/SM626/SM627/SM635/SM636/SM637

SWITCHING REGULATOR POWER OUTPUT STAGES

DESCRIPTION

The SM625/626/627 and SM635/636/637 series of Power Output Stages are especially designed to be driven with standard PWM integrated circuits to form an efficient switching power supply. The SM625, SM626 and SM627 are optimized for non-isolated Buck and Buck-Boost application, where SM635, SM636 and SM637 are best suited for DC-DC Boost type applications as well as negative output Buck Converters. The hybrid circuit construction utilizes thick film resistors on a beryllia substrate for maximum thermal conductivity and resultant low thermal impedance. All of the active elements in the hybrid are fully passivated.

FEATURES

- **Equivalent to the Unitrode PIC 625, 626, 627, 635, 636, 637**
- **15A current capability**
- **Designed and characterized for switching regulator applications such as Buck, Boost, and Buck-Boost type**
- **Cost saving design reduces size, improves efficiency, reduces noise and RFI**
- **High operating frequency (to > 100KHz) results in smaller inductor-capacitor filter and improved power supply response time**
- **High operating efficiency at 7A typical performance -**
  Rise and fall time < 300ns
  Efficiency > 85%
- **Electrically isolated, 4-pin, TO-66 hermetic case**

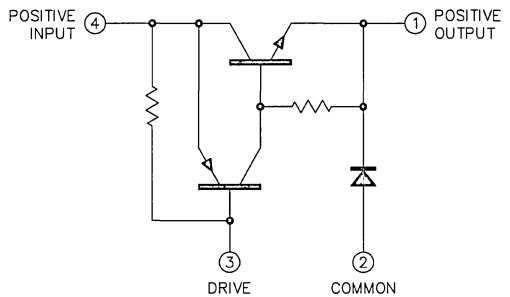
HIGH RELIABILITY FEATURES

- **Available with high reliability processing**

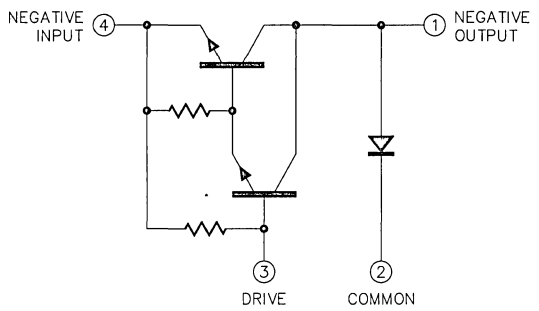
4

FUNCTIONAL DIAGRAM

SM625/SM626/SM627



SM635/SM636/SM637



April 1990

ABSOLUTE MAXIMUM RATINGS (Note 1)

	SM625	SM626	SM627	SM635	SM636	SM637
Input Voltage, V_{4-2}	60V	80V	100V	-60V	-80V	-100V
Output Voltage, V_{1-2}	60V	80V	100V	-60V	-80V	-100V
Drive Input Reverse Voltage, V_{3-4}	5V	5V	5V	-5V	-5V	-5V
Output Current, I_1	15A	15A	15A	-15A	-15A	-15A
Drive Current, I_3	-0.4A	-0.4A	-0.4A	0.4A	0.4A	0.4A

Thermal Resistance
- Power Switch, θ_{J-C} ..... 4.0°C/W
- Commutating Diode ..... 4.0°C/W
- Case to Ambient, θ_{C-A} ..... 60.0°C/W

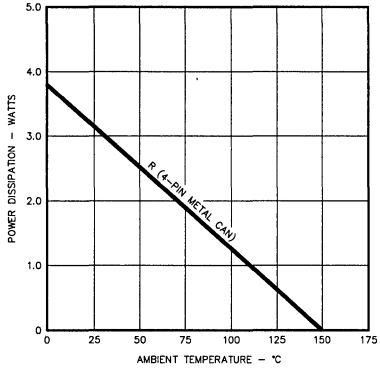
Operating Junction Temperature
- Hermetic (R Package) ..... 150°C

Storage Temperature Range ..... -65°C to 150°C

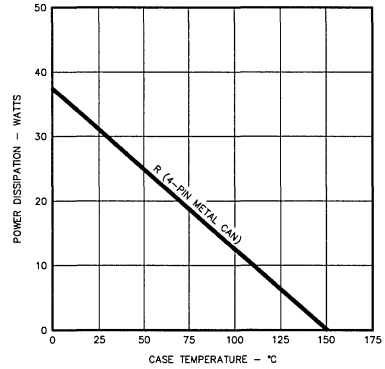
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

	SM625	SM626	SM627	SM635	SM636	SM637
Input Voltage, V_{4-2}	50V	70V	90V	-50V	-70V	-90V
Output Voltage, V_{1-2}	50V	70V	90V	-50V	-70V	-90V
Drive Input Reverse Voltage, V_{3-4}	4V	4V	4V	-4V	-4V	-4V
Output Current, I_1	13A	13A	13A	-13A	-13A	-13A
Drive Current, I_3	-0.3A	-0.3A	-0.3A	0.3A	0.3A	0.3A

Operating Ambient Temperature Range
- SM6XXR ..... 0°C to 70°C
- SM6XXHRR ..... -55°C to 125°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply for the operating ambient temperature of T_A = 25°C. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG625/626/627			SG635/636/637			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
On-State Voltage (Note 3)	I_4 = 7A(-7A), I_3 = -30mA (30mA)		1.0	1.5		-1.0	-1.5	V
	I_4 = 15A(-15A), I_3 = -30mA (30mA)		2.5	3.5		-2.5	-3.5	V
Diode Forward Voltage (Note 3)	I_4 = 7A(-7A)		0.85	1.25		-0.85	-1.25	V
	I_4 = 15A(-15A)		0.95	1.75		-0.95	-1.75	V
Off-State Current	V_4 = Rated input voltage		0.1	10		-0.1	-10	µA
	V_4 = Rated input voltage, T_A = 125°C		10			-10		µA
Diode Reverse Current	V_1 = Rated output voltage		1.0	10		-1.0	-10	µA
	V_1 = Rated output voltage, T_A = 125°C		500			-500		µA

Note 3. Pulse test: Duration = 300µs, Duty Cycle ≤ 2%.

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG625/626/627			SG635/636/637			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Dynamic Characteristics (See Figures 1 & 2) (Notes 4 & 5)								
Current Delay Time			35	60		35	60	ns
Current Rise Time			65	150		65	175	ns
Voltage Rise Time			40	60		40	60	ns
Voltage Storage Time			700			700		ns
Voltage Fall Time			70	175		100	300	ns
Current Fall Time			175	300		175	300	ns
Efficiency (Note 5)			85			85		%

AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS (Note 6)

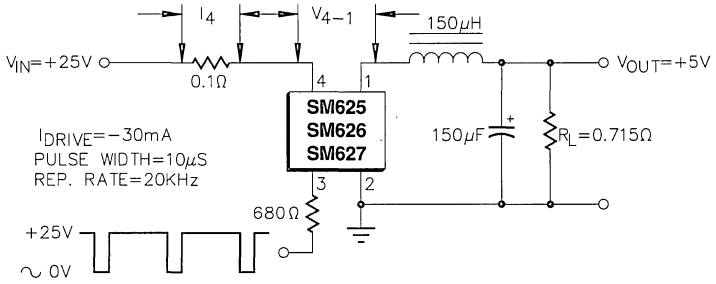


FIGURE 1 - SM625/626/627 SWITCHING SPEED CIRCUIT

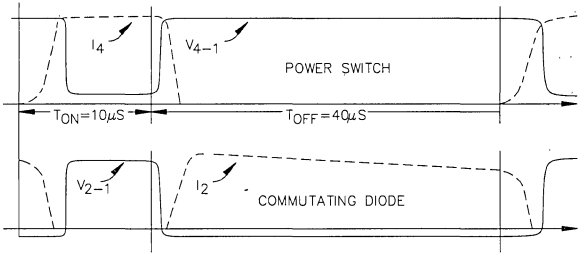


FIGURE 2 - SM625/626/627 SWITCHING WAVEFORMS

Note 4. In switching an inductive load, the current will lead the voltage on turn-on and lag the voltage on turn-off (see Figure 2). Therefore, Voltage Delay Time (t_{DV}) $\equiv t_{di} + t_n$ and Current Storage Time (t_{si}) $\equiv t_{sv} + t_{fv}$.

Note 5. The efficiency is a measure of internal power losses and is equal to Output Power divided by Input Power. The switching speed circuit of Figure 1, in which the efficiency measured, is represenative of typical operating conditions for the SM600 series switching regulators.

Note 6. SM635/636/637 Test Circuit and waveforms are identical but of opposite polarity (V_{IN} = -25V, V_{OUT} = -5V, I_{DRIVE} = +30mA).

APPLICATION CIRCUITS

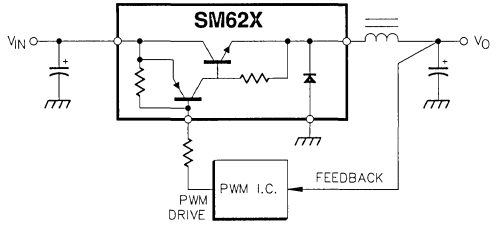


FIGURE 3 - STEP DOWN (BUCK) CONVERTER

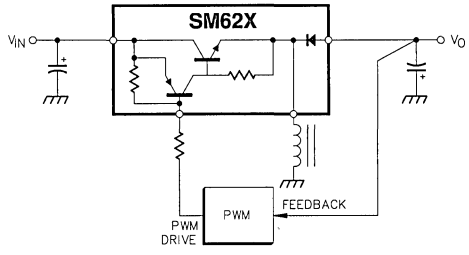


FIGURE 4 - NEGATIVE OUTPUT DOWN/UP (BUCK-BOOST) CONVERTER

APPLICATION CIRCUITS (continued)

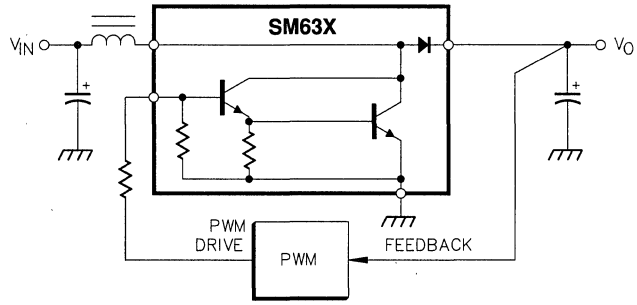
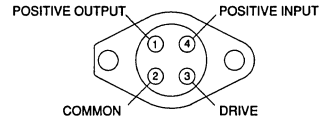
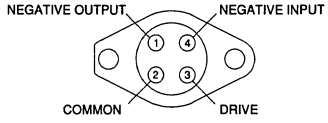


FIGURE 5 - STEP UP (BOOST) CONVERTER

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Note Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
4-PIN TO-66 METAL CAN R - PACKAGE	SM625R SM625HRR SM626R SM626HRR SM627R SM627HRR	0°C to 70°C -55°C to 125°C 0°C to 70°C -55°C to 125°C 0°C to 70°C -55°C to 125°C	
	SM635R SM635HRR SM636R SM636HRR SM637R SM637HRR	0°C to 70°C -55°C to 125°C 0°C to 70°C -55°C to 125°C 0°C to 70°C -55°C to 125°C	

Note 1. All packages are viewed from the top.
2. Case is electrically isolated.
3. Contact factory for additional screening available.

SM645/SM646/SM647/SM655/SM656/SM657

SWITCHING REGULATOR POWER OUTPUT STAGES

DESCRIPTION

The SM645/646/647 and SM655/656/657 series of Power Output Stages are especially designed to be driven with standard PWM integrated circuits to form an efficient switching power supply. The SM645, SM646 and SM647 are optimized for non-isolated Buck and Buck-Boost application, where SM655, SM656 and SM657 are best suited for DC-DC Boost type applications as well as negative output Buck Converters. The hybrid circuit construction utilizes thick film resistors on a beryllia substrate for maximum thermal conductivity and resultant low thermal impedance. All of the active elements in the hybrid are fully passivated.

FEATURES

- **Equivalent to the Unitrode PIC 645, 646, 647, 655, 656, 657**
- **15A current capability**
- **Cost saving design reduces size, improves efficiency, reduces noise and RFI**
- **High operating frequency (to > 100KHz) results in smaller inductor-capacitor filter and improved power supply response time**
- **High operating efficiency at 7A typical performance - Rise and fall time < 300ns Efficiency > 85%**

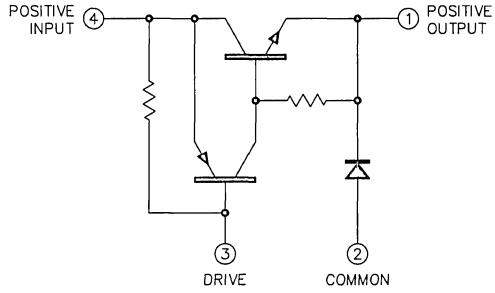
HIGH RELIABILITY FEATURES

- **Available with high reliability processing**

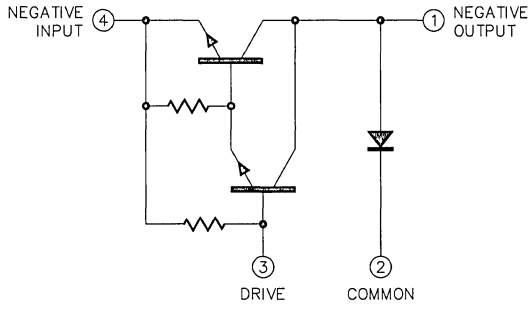
4

FUNCTIONAL DIAGRAM

SM645/SM646/SM647



SM655/SM656/SM657



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ABSOLUTE MAXIMUM RATINGS (Note 1)

	SM645	SM646	SM647	SM655	SM656	SM657
Input Voltage, V_{4-2}	60V	80V	100V	-60V	-80V	-100V
Output Voltage, V_{1-2}	60v	80v	100V	-60v	-80v	-100V
Drive Input Reverse Voltage, V_{3-4}	5V	5V	5V	-5V	-5V	-5V
Continuous Output Current, I_1	15A	15A	15A	-15A	-15A	-15A
Peak Output Current	20A	20A	20A	-20A	-20A	-20A
Drive Current, I_3	-0.4A	-0.4A	-0.4A	0.4A	0.4A	0.4A

Thermal Resistance
- Power Switch, θ_{J-C} ..... 2.0°C/W
- Commutating Diode ..... 2.0°C/W
- Case to Ambient, θ_{C-A} ..... 30.0°C/W

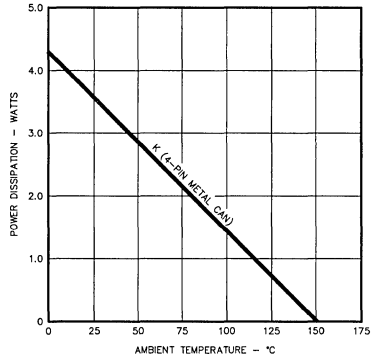
Operating Junction Temperature
- Hermetic (K Package) ..... 150°C

Storage Temperature Range ..... -65°C to 150°C

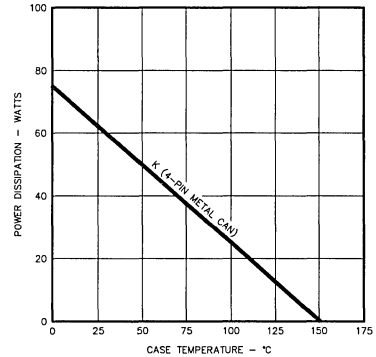
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

	SM645	SM646	SM647	SM655	SM656	SM657
Input Voltage, V_{4-2}	50V	70V	90V	-50V	-70V	-90V
Output Voltage, V_{1-2}	50v	70v	90V	-50v	-70v	-90V
Drive Input Reverse Voltage, V_{3-4}	4V	4V	4V	-4V	-4V	-4V
Output Current, I_1	13A	13A	13A	-13A	-13A	-13A
Drive Current, I_3	-0.3A	-0.3A	-0.3A	0.3A	0.3A	0.3A

Operating Ambient Temperature Range
- SM6XXK ..... 0°C to 70°C
- SM6XXHRK ..... -55°C to 125°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply for the operating ambient temperature of T_A = 25°C. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG645/646/647			SG655/656/657			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
On-State Voltage (Note 3)	I_4 = 7A(-7A), I_3 = -30mA(30mA)		1.0	1.5		-1.0	-1.5	V
	I_4 = 15A(-15A), I_3 = -30mA(30mA)		2.5	3.5		-2.5	-3.5	V
Diode Forward Voltage (Note 3)	I_4 = 7A(-7A)		0.85	1.25		-0.85	-1.25	V
	I_4 = 15A(-15A)		0.95	1.75		-0.95	-1.75	V
Off-State Current	V_4 = Rated input voltage		0.1	10		-0.1	-10	µA
	V_4 = Rated input voltage, T_A = 125°C		10			-10		µA
Diode Reverse Current	V_1 = Rated output voltage		1.0	10		-1.0	-10	µA
	V_1 = Rated output voltage, T_A = 125°C		500			-500		µA

Note 3. Pulse test: Duration = 300µs, Duty Cycle ≤ 2%.

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG645/646/647			SG655/656/657			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Dynamic Characteristics (See Figures 1 & 2) (Notes 4 & 5)								
Current Delay Time			35	60		35	60	ns
Current Rise Time			65	150		65	175	ns
Voltage Rise Time			40	60		40	60	ns
Voltage Storage Time			700			700		ns
Voltage Fall Time			70	175		100	300	ns
Current Fall Time			175	300		175	300	ns
Efficiency (Note 5)			85			85		%

AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS (Note 6)

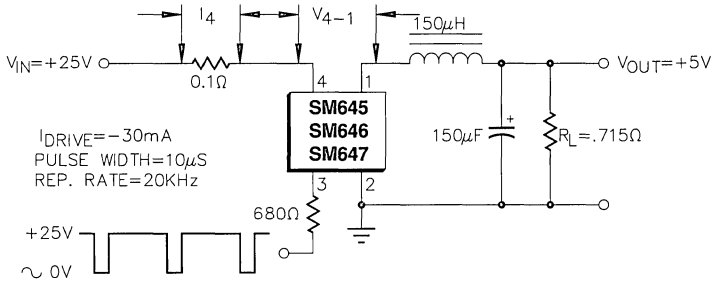


FIGURE 1 - SM645/646/647 SWITCHING SPEED CIRCUIT

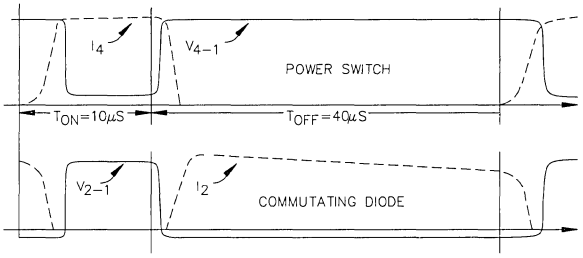


FIGURE 2 - SM645/646/647 SWITCHING WAVEFORMS

Note 4. In switching an inductive load, the current will lead the voltage on turn-on and lag the voltage on turn-off (see Figure 2). Therefore, Voltage Delay Time (t_{DV}) $\cong t_{di} + t_{fi}$ and Current Storage Time (t_{si}) $\cong t_{sv} + t_{fv}$.

Note 5. The efficiency is a measure of internal power losses and is equal to Output Power divided by Input Power. The switching speed circuit of Figure 1, in which the efficiency measured, is represenative of typical operating conditions for the SM600 series switching regulators.

Note 6. SM655/656/657 Test Circuit and waveforms are identical but of opposite polarity (V_{IN} = -25V, V_{OUT} = -5V, I_{DRIVE} = +30mA).

APPLICATION CIRCUITS

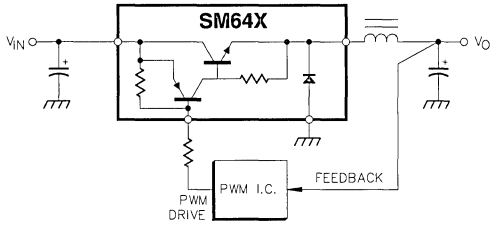


FIGURE 3 - STEP DOWN (BUCK) CONVERTER

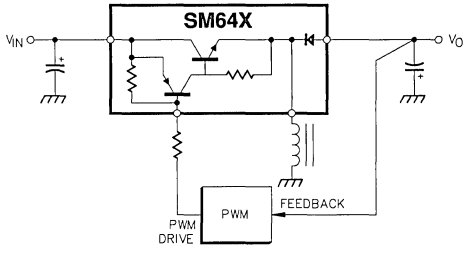


FIGURE 4 - NEGATIVE OUTPUT DOWN/UP (BUCK-BOOST) CONVERTER

APPLICATION CIRCUITS (continued)

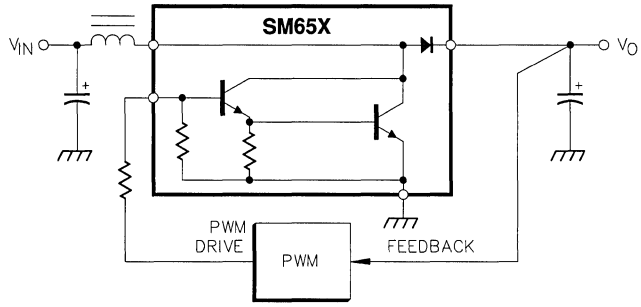
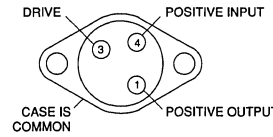
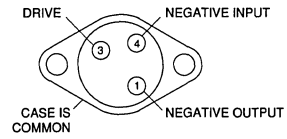


FIGURE 5 - STEP UP (BOOST) CONVERTER

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Note Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
4-TERMINAL TO-3 METAL CAN K - PACKAGE	SM645K SM645HRK SM646K SM646HRK SM647K SM647HRK	0°C to 70°C -55°C to 125°C 0°C to 70°C -55°C to 125°C 0°C to 70°C -55°C to 125°C	
	SM655K SM655HRK SM656K SM656HRK SM657K SM657HRK	0°C to 70°C -55°C to 125°C 0°C to 70°C -55°C to 125°C 0°C to 70°C -55°C to 125°C	

Note 1. All packages are viewed from the top.
2. Consult factory for additional screening available.

SM660/SM661/SM662/SM670/SM671/SM672

SWITCHING REGULATOR POWER OUTPUT STAGES

DESCRIPTION

The SM660/661/662 and SM670/671/672 series of Power Output Stages are especially designed to be driven with standard PWM integrated circuits to form an efficient switching power supply. The SM660, SM661 and SM662 are optimized for non-isolated Buck and Buck-Boost application, where SM670, SM671 and SM672 are best suited for DC-DC Boost type applications as well as negative output Buck Converters. The hybrid circuit construction utilizes thick film resistors on a beryllia substrate for maximum thermal conductivity and resultant low thermal impedance. All of the active elements in the hybrid are fully passivated.

FEATURES

- **Equivalent to the Unitrode PIC 660, 661, 662, 670, 671, 672**
- **10A current capability**
- **Designed and characterized for switching regulator applications such as Buck, Boost, and Buck-Boost type**
- **Cost saving design reduces size, improves efficiency, reduces noise and RFI**
- **High operating frequency (to > 100KHz) results in smaller inductor-capacitor filter and improved power supply response time**
- **High operating efficiency at 7A typical performance -**
  Rise and fall time < 300ns
  Efficiency > 85%
- **Electrically isolated, 4-pin, TO-66 hermetic case**

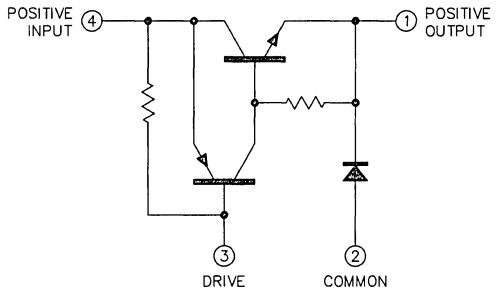
HIGH RELIABILITY FEATURES

- **Available with high reliability processing**

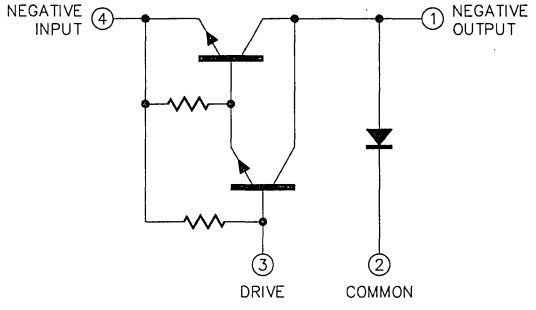
4

FUNCTIONAL DIAGRAM

SM660/SM661/SM662



SM670/SM671/SM672



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ABSOLUTE MAXIMUM RATINGS (Note 1)

	SM660	SM661	SM662	SM670	SM671	SM672
Input Voltage, V_{4-2}	60V	80V	100V	-60V	-80V	-100V
Output Voltage, V_{1-2}	60V	80V	100V	-60V	-80V	-100V
Drive Input Reverse Voltage, V_{3-4}	5V	5V	5V	-5V	-5V	-5V
Output Current, I_1	10A	10A	10A	-10A	-10A	-10A
Drive Current, I_3	-0.4A	-0.4A	-0.4A	0.4A	0.4A	0.4A

Thermal Resistance
- Power Switch, θ_{J-C} ..... 4.0°C/W
- Commutating Diode ..... 4.0°C/W
- Case to Ambient, θ_{C-A} ..... 60.0°C/W

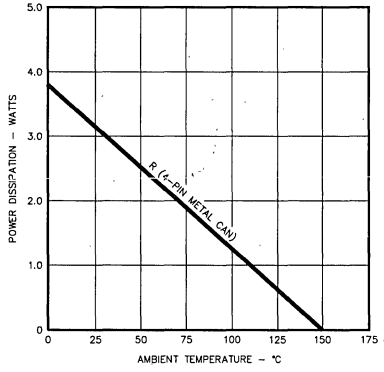
Operating Junction Temperature
- Hermetic (R Package) ..... 150°C

Storage Temperature Range ..... -65°C to 150°C

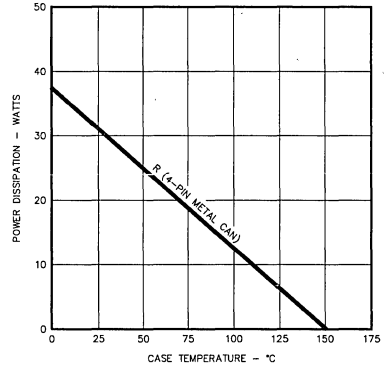
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

	SM660	SM661	SM662	SM660	SM661	SM662
Input Voltage, V_{4-2}	50V	70V	90V	-50V	-70V	-90V
Output Voltage, V_{1-2}	50V	70V	90V	-50V	-70V	-90V
Drive Input Reverse Voltage, V_{3-4}	4V	4V	4V	-4V	-4V	-4V
Output Current, I_1	9A	9A	9A	-9A	-9A	-9A
Drive Current, I_3	-0.3A	-0.3A	-0.3A	0.3A	0.3A	0.3A

Operating Ambient Temperature Range
- SM6XXR ..... 0°C to 70°C
- SM6XXHRK ..... -55°C to 125°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply for the operating ambient temperature of T_A = 25°C. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG660/661/662			SG670/671/672			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
On-State Voltage (Note 3)	I_4 = 5A(-5A), I_3 = -30mA(30mA)		1.0	1.5		-10	-1.5	V
	I_4 = 10A(-10A), I_3 = -30mA(30mA)		2.5	3.5		-2.5	-3.5	V
Diode Forward Voltage (Note 3)	I_4 = 5A(-5A)		0.85	1.25		-0.85	-1.25	V
	I_4 = 10A(-10A)		0.95	1.75		-0.95	-1.75	V
Off-State Current	V_4 = Rated input voltage		0.1	10		-0.1	-10	µA
	V_4 = Rated input voltage, T_A = 125°C		10			-10		µA
Diode Reverse Current	V_1 = Rated output voltage		1.0	10		-1.0	-10	µA
	V_1 = Rated output voltage, T_A = 125°C		500			-500		µA

Note 3. Pulse test: Duration = 300µs, Duty Cycle ≤ 2%.

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG660/661/662			SG670/671/672			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Dynamic Characteristics (See Figures 1 & 2) (Notes 4 & 5)								
Current Delay Time			35	60		35	60	ns
Current Rise Time			65	150		65	175	ns
Voltage Rise Time			40	60		40	60	ns
Voltage Storage Time			700			700		ns
Voltage Fall Time			70	175		100	300	ns
Current Fall Time			175	300		175	300	ns
Efficiency (Note 5)			85			85		%

AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS (Note 6)

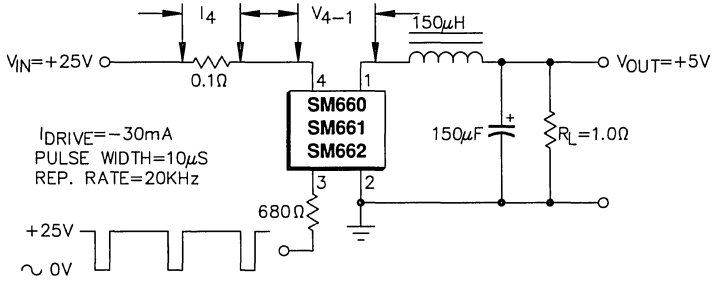


FIGURE 1 - SM660/661/662 SWITCHING SPEED CIRCUIT

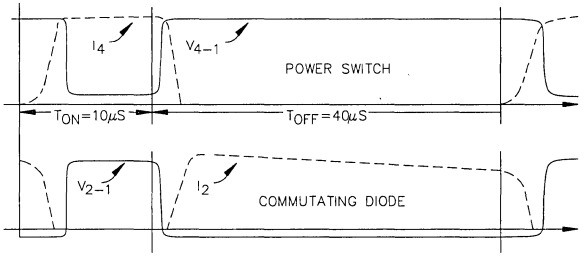


FIGURE 2 - SM660/661/662 SWITCHING WAVEFORMS

Note 4. In switching an inductive load, the current will lead the voltage on turn-on and lag the voltage on turn-off (see Figure 2). Therefore, Voltage Delay Time (t_{DV}) ≅ $t_d + t_n$ and Current Storage Time (t_{si}) ≅ $t_{sv} + t_{fv}$.

Note 5. The efficiency is a measure of internal power losses and is equal to Output Power divided by Input Power. The switching speed circuit of Figure 1, in which the efficiency measured, is represenative of typical operating conditions for the SM600 series switching regulators.

Note 6. SM670/671/672 Test Circuit and waveforms are identical but of opposite polarity (V_{IN} = -25V, V_{OUT} = -5V, I_{DRIVE} = +30mA).

APPLICATION CIRCUITS

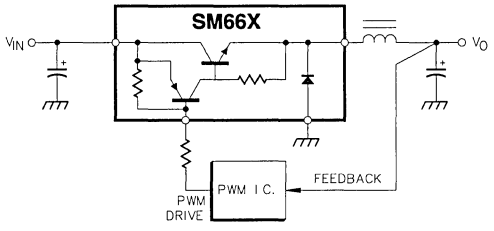


FIGURE 3 - STEP DOWN (BUCK) CONVERTER

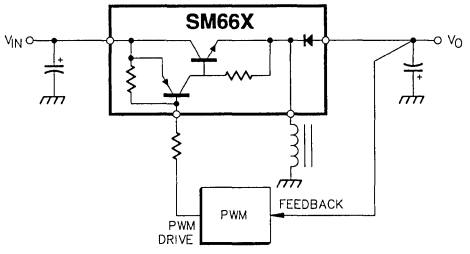


FIGURE 4 - NEGATIVE OUTPUT DOWN/UP (BUCK-BOOST) CONVERTER

APPLICATION CIRCUITS (continued)

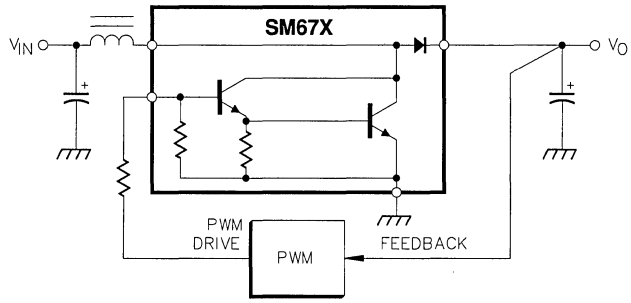
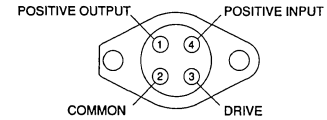
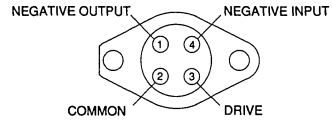


FIGURE 5 - STEP UP (BOOST) CONVERTER

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Note Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
4-PIN TO-66 METAL CAN R - PACKAGE	SM660R SM660HRR SM661R SM661HRR SM662R SM662HRR	0°C to 70°C -55°C to 125°C 0°C to 70°C -55°C to 125°C 0°C to 70°C -55°C to 125°C	
	SM670R SM670HRR SM671R SM671HRR SM672R SM672HRR	0°C to 70°C -55°C to 125°C 0°C to 70°C -55°C to 125°C 0°C to 70°C -55°C to 125°C	

Note 1. All packages are viewed from the top.
2. Case is electrically isolated.
3. Consult factory for additional screening available.

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SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SELECTION GUIDE
MOTION CONTROL CIRCUITS

Device Type	Description	Typ. Application	$I_{O(PK)}$	$I_{O(CONT)}$	$V_{C(MAX)}$	$V_{CC(MAX)}$	Key Features	Pkgs.
SG1635/3635 SG1635A/3635A SG1650/3650	Half-bridge driver	• DC motor drivers • Stepper motor drive	5A	2A	35V 40V	35V 40V	• Single totem-pole output • Internal clamp diodes • Built-in thermal protection • TTL input compatibility	R, P
SG3645	Quad power driver	• DC motor drivers • Stepper motor drive • Lamp driver • Relay driver	3.5A	2.5A	60V	40V	• Four open collector outputs • Internal clamp diodes • Thermal shutdown protection • TTL input compatibility • Common enable pin	W, DWW
SG3663	Dual solenoid motor driver	• DC motor drivers • Stepper motor drive • Solenoid motor drive	3.5A	3.0A	50V	50V	• Dual uncommited totem pole outputs • Internal clamp diodes • Thermal shutdown protection • Current sense comparator with variable threshold and hysteresis • Chop or non-chop load current control	S, ST
SG3700	Dual hammer driver	• DC motor drivers • Hammer coil drive in high speed printers	1.5A	0.9A	5.25V	40V	• Dual open collector outputs • Internal clamp diodes • Thermal shutdown protection • Internal op-amp to regulate output current • Adjustable output current control • Thermal shutdown indicator • Logic control of input data	N
SG1731/2731/3731	DC motor pulse-width modulator	• DC motor control • Electronic micro-stepping of stepper motors	400mA	200mA	±25V (50V)	±18V (36V)	• Dual uncommited totem pole outputs • Maximum frequency to 350KHz • Adjustable deadband operation • High slew rate op-amp • Digital $\overline{\text{SHUTDOWN}}$ input	J, N
SG3718	Sepper motor driver	• Stepper motors	1.5A	1.2A	5.5V	45V	• Full-step, Half-step, Micro-set capability • Wide range of motor supply voltge • Built-in fast commutating diodes • Output stage shoot-through protection • Thermal shutdown protection • Low saturation output stage • Designed for unstabilized motor supply	W, DWW, Q
SG1173/2173/3173 SG3172 SG3272	Power op-amp	• Linear DC motor	5A 3A 1.5A	3.5A 2A 1A	50V 18V 18V		SEE OP-AMP SECTION	
SG2000/2800 Series	Darlington arrays	• Logic to power interface • Lamp driver • Motor driver	0.6A	0.5A	50V & 95V		SEE POWER DRIVER & INTERFACE SECTION	
SG2064 thru 2077	Quad power Darlington arrays	• Relays • Solenoids • DC and stepper motor driver • Display driver	1.75A	1.5A	50V & 80V		SEE POWER DRIVER SECTION	

November 1988

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SG1635A/SG3635A
SG1635/SG3635
SG1650/SG3650

2A, HALF-BRIDGE DRIVER

DESCRIPTION

The SG1635 and SG1650 are monolithic integrated circuits designed to interface low-level logic signals with high-current, inductive, or capacitive loads. These devices are particularly adept at high-speed pulse width modulation for motor drives or Class D audio amplifiers, and when used in pairs, they can provide full bridge drive for bi-directional control.

With TTL-compatible units, these devices will either source or sink up to 5A of peak current with interlock protection to insure that source and sink cannot be on simultaneously. Additional protection is provided by thermal shutdown of the source output if the chip temperature rises above 160°C. High speed internal commutating diodes are also included.

FEATURES

- **Source or sink 5A peak**
- **Half-bridge with internal diodes**
- **TTL input compatibility**
- **Either dual- or tri-state output**
- **Direct PWM motor drive from microprocessor**
- **Built-in thermal protection**
- **SG3635P replaces UDN2935Z**
  SG3650P replaces UDN2950Z and SN75605

HIGH RELIABILITY FEATURES - SG1635A/SG1635/SG1650

- ◊ **Available to MIL-STD-883**
- ◊ **SG level "S" processing available**

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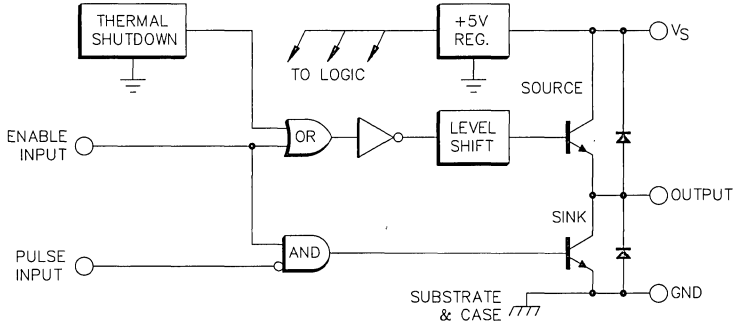
BLOCK DIAGRAM - SG1635/1635A/3635/3635A

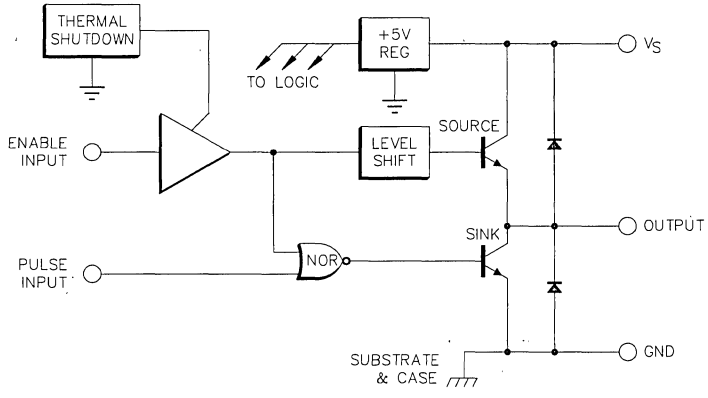


TRUTH TABLE

Enable	Pulse	Output
0	0	High
0	1	High
1	0	Low
1	1	Off - High Z

1 = Open or High

BLOCK DIAGRAM - SG1650/3650



TRUTH TABLE

Enable	Pulse	Output
0	0	Low
0	1	Off - High Z
1	0	Low
1	1	High

1 = Open or High

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See Application Notes for additional information.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V_S)
- SG1635/SG3635, SG1650/SG3650 ..... 40V
- SG1635A/SG3635A 45V

Input Voltage
- Enable and Pulse 7V

Source/Sink Output Current
- Contiuous 3A
- Peak 5A

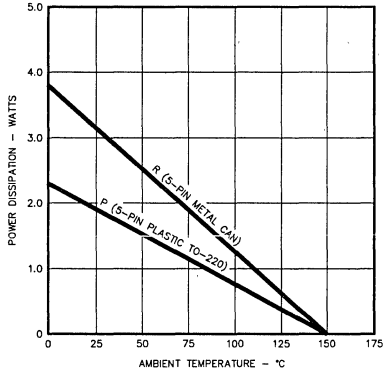
Operating Junction Temperature
- Hermetic (R - Package) ..... 150°C
- Plastic (P - Package) ..... 150°C

Storage Temperature Range ..... -65°C to 150°C

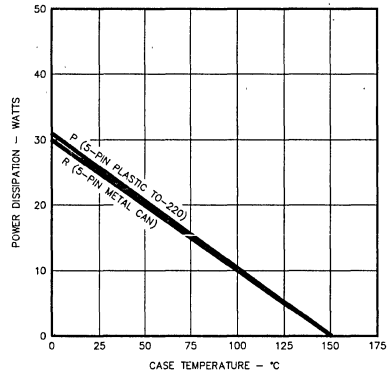
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Values beyond which damage may occur.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage (V_S)
- SG1635/SG3635, SG1650/SG3650 ..... 8V to 35V
- SG1635A/SG3635A ..... 8V to 40V

Source/Sink Output Current
- Continuous 2A
- Peak 3A

Operating Ambient Temperature Range
- SG1635/SG1635A, SG1650 ..... -55°C to 125°C
- SG3635/SG3635A, SG3650 ..... 0°C to 70°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

SG1635/SG1635A and SG3635/SG3635A

(Unless otherwise specified, these specfiications apply over the operating ambient temperatures for SG1635/SG1635A with -55°C ≤ T_A ≤ 125°C, SG3635/SG3635A with 0°C ≤ T_A ≤ 70°C, and +V_S = 24V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1635/1635A SG3635/3635A			Units
		Min.	Typ.	Max.	
Static Characteristics					
Logic 1 Input Voltage		2.0			V
Logic 0 Input Voltage				0.8	V
Input High Current	V_{PULSE} = V_{ENABLE} = 4.5V			200	µA
Input Low Current	V_{PULSE} = V_{ENABLE} = 0V			-3.2	mA
Output Leakage	V_{PULSE} = V_{ENABLE} = 2.0V				
	V_{OUT} = 24V			500	mA
	V_{OUT} = 0V			40	mA
Source Saturation Voltage	V_{PULSE} = 2.0V, V_{ENABLE} = 0.8V, I_{OUT} = -2A		2.0	3.0	V
Sink Saturation Voltage	V_{PULSE} = 0.8V, V_{ENABLE} = 2.0V, I_{OUT} = 2A		2.0	3.0	V
Diode Forward Voltage	I_{DIODE} = ±2A		2.0	3.0	V
Supply Current	V_S = 35V (SG1635/3635); V_S = 40V (SG1635A/3635A)				
	V_{PULSE} = 2.0V, V_{ENABLE} = 0.8V			25	mA
	V_{PULSE} = 0.8V, V_{ENABLE} = 2.0V			70	mA

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Definition	SG1635/1635A SG3635/3635A Min.	Typ.	Max.	Units
Dynamic Characteristics (Notes 3 and 4)					
Pulse Propagation Delay	Turn-On Delay (TPDHL)		50		ns
	Turn-Off Delay (TPDLH)		100		ns
Pulse Transition Time	Turn-On (TPTHL)		200		ns
	Turn-Off (TPTLH)		200		ns
Enable Propagation Delay	Turn-On Delay (TEDLH)		200		ns
	Turn-Off Delay (TEDHL)		100		ns
Enable Transition Time	Turn-On (TETLH)		100		ns
	Turn-Off (TETHL)		100		ns

Note 3. T_J = 25°C.
Note 4. Although these parameters are guaranteed, they are not tested in production.

SG1650/SG3650

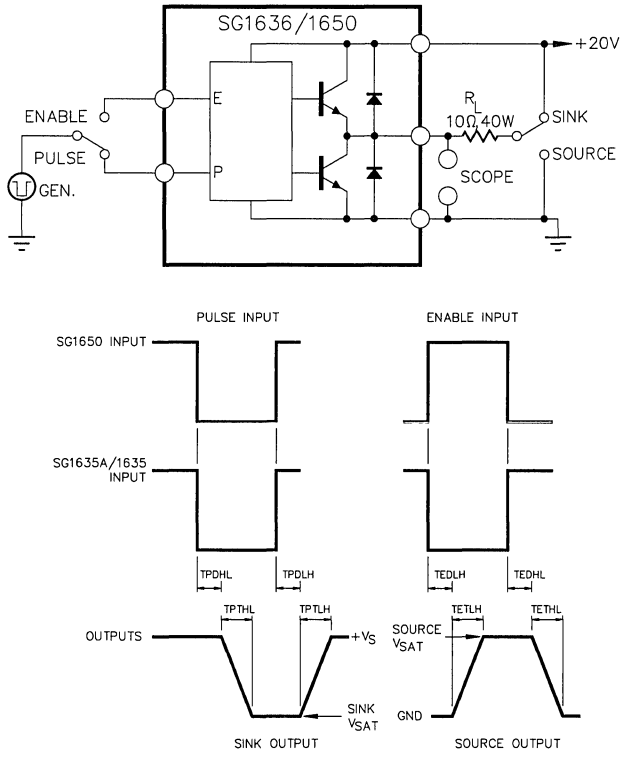
(Unless otherwise specified, these specfiications apply over the operating ambient temperatures for SG1650 with -55°C ≤ T_A ≤ 125°C, SG3650 with 0°C ≤ T_A ≤ 70°C, and +V_S = 24V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1650 SG3650 Min.	Typ.	Max.	Units
Static Characteristics					
Logic 1 Input Voltage		2.0			V
Logic 0 Input Voltage				0.8	V
Input High Current	$V_{PULSE} = V_{ENABLE} = 4.5V$			200	µA
Input Low Current	$V_{PULSE} = V_{ENABLE} = 0V$			-3.2	mA
Output Leakage	$V_{PULSE} = 2.0V$, $V_{ENABLE} = 0.8V$				
	$V_{OUT} = 24V$			500	µA
	$V_{OUT} = 0V$			40	mA
Source Saturation Voltage	$V_{ENABLE} = 0.8V$, $I_{OUT} = -2A$		2.0	3.0	V
Sink Saturation Voltage	$V_{PULSE} = V_{ENABLE} = 0.8V$, $I_{OUT} = 2A$		2.0	3.0	V
Diode Forward Voltage	$I_{DIODE} = \pm 2A$		2.0	3.0	V
Supply Current	V_S = 35V				
	$V_{PULSE} = 2.0V$, $V_{ENABLE} = 0.8V$			25	mA
	$V_{PULSE} = 0.8V$, $V_{ENABLE} = 2.0V$			70	mA

Parameter	Definition	SG1635/1635A SG3635/3635A Min.	Typ.	Max.	Units
Dynamic Characteristics (Notes 5 and 6)					
Pulse Propagation Delay	Turn-On Delay (TPDHL)		300		ns
	Turn-Off Delay (TPDLH)		300		ns
Enable Propagation Delay	Turn-On Delay (TEDLH)		1		µs
	Turn-Off Delay (TEDHL)		1		µs

Note 5. T_J = 25°C.
Note 6. Although these parameters are guaranteed, they are not tested in production.

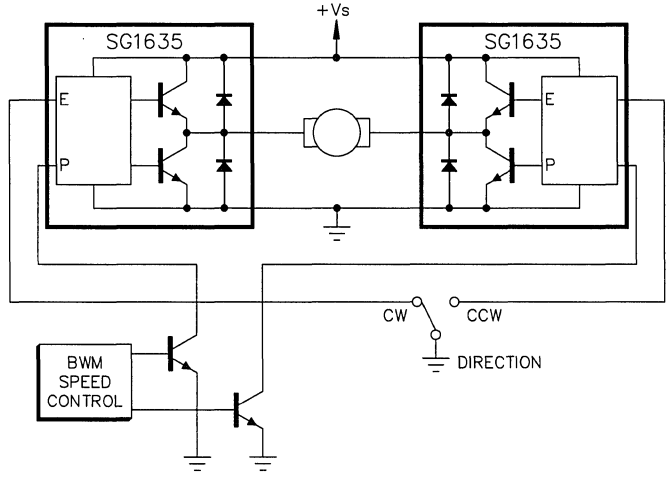
AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS - FIGURE 1



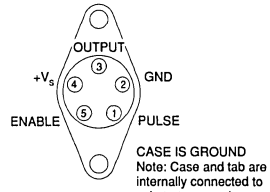
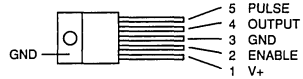
APPLICATION INFORMATION

TYPICAL MOTOR DRIVE APPLICATION

Two SG1635's form a full bridge motor drive circuit with the appropriate Enable Input, determining motor direction, and a PWM signal into the Pulse Inputs, determining speed. Because of the internal Enable interlock, both Pulse Inputs may be connected together to a single-ended PWM



CONNECTION DIAGRAMS/ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
5-PIN TO-66 METAL CAN R - PACKAGE	SG1635AR/883B SG1635AR SG3635AR SG1635R/883B SG1635R SG3635R SG1650R/883B SG1650R SG3650R	-55°C to 125°C -55°C to 125°C 0°C to 70°C -55°C to 125°C -55°C to 125°C 0°C to 70°C -55°C to 125°C -55°C to 125°C 0°C to 70°C	 CASE IS GROUND Note: Case and tab are internally connected to substrate ground.
5-PIN TO-220 PLASTIC P - PACKAGE	SG3635AP SG3635P SG3650P	0°C to 70°C 0°C to 70°C 0°C to 70°C	 Case + Tab are internally connected

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Notes: 1. Contact factory for JAN and DESC part availability.
2. All parts are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

DC MOTOR PULSE WIDTH MODULATOR

DESCRIPTION

The SG1731 is a pulse width modulator circuit designed specifically for DC motor control. It provides a bi-directional pulse train output in response to the magnitude and polarity of an analog error signal input. The device is useful as the control element in motor-driven servo systems for precision positioning and speed control, as well as in audio modulators and amplifiers using carrier frequencies to 350 KHz.

The circuit contains a triangle waveform oscillator, a wideband operational amplifier for error voltage generation, a summing/scaling network for level-shifting the triangle waveform, externally programmable PWM comparators and dual ±100mA, ±22V totem pole drivers with commutation diodes for full bridge output. A $\overline{\text{SHUTDOWN}}$ terminal forces the drivers into a floating high-impedance state when driven LOW. Supply voltage to the control circuitry and to the output drivers may be from either dual positive and negative supplies, or single-ended.

FEATURES

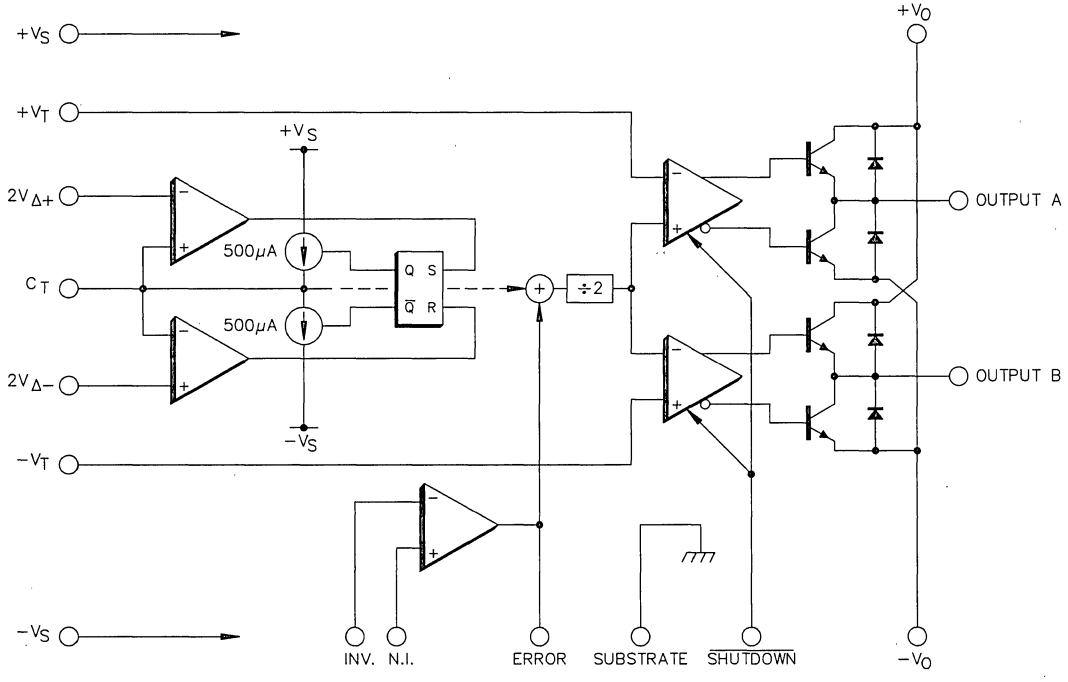
- **±3.5V to ±15V control supply**
- **±2.5V to ±22V driver supply**
- **Dual 100mA source/sink output drivers**
- **5KHz to 350KHz oscillator range**
- **High slew rate error amplifier**
- **Adjustable deadband operation**
- **Digital $\overline{\text{SHUTDOWN}}$ input**

HIGH RELIABILITY FEATURES - SG1731

- **Available to MIL-STD-883**
- **SG level "S" processing available**

5

BLOCK DIAGRAM



April 1990

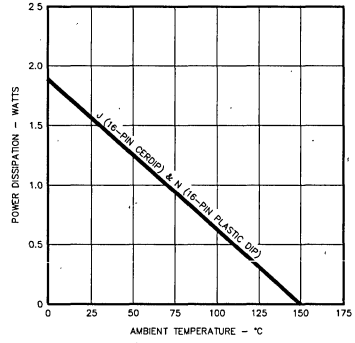
See Application Notes for additional information.

ABSOLUTE MAXIMUM RATINGS (Note1)

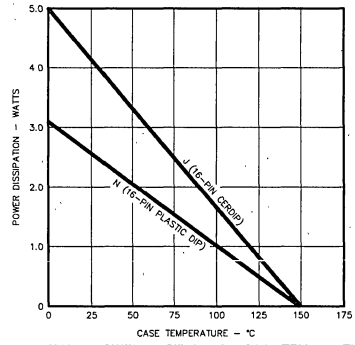
Supply Voltage ($\pm V_S$) ..... ±18V
Analog Inputs ..... $\pm V_S$
Digital Inputs ($\overline{SHUTDOWN}$) ..... $-V_S$-0.3V to $-V_S$+18V
Output Driver Supply Voltage ($\pm V_O$) ..... ±25V
Source/Sink Output Current (continuous) 200mA
Source/Sink Output Current (peak, 500ns) 400mA
Note 1. Values beyond which damage may occur.

Output Driver Diode Current (continuous) 200mA
Output Driver Diode Current (peak, 500ns) 400mA
Operating Junction Temperature
Hermetic (J - Package) ..... 150°C
Plastic (N - Package) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage Range ($\pm V_S$) ..... ±3.5V to ±15V
Error Amp Common-Mode Range ..... $-V_S$ + 3V to V_S - 3V
Output Driver Supply Voltage Range ..... ±2.5V to ±22V
Source/Sink Output Current (continuous) 100mA
Source/Sink Output Current (peak, 500ns) 200mA
Output Driver Diode Current (continuous) 100mA
Output Driver Diode Current (peak, 500ns) 200mA

Oscillator Frequency Range ..... 10Hz to 350KHz
Oscillator Voltage (Peak-to-Peak) ..... 1V to 10V
Oscillator Timing Capacitor (C_T) ..... 200pF to 2.5µF
Operating Ambient Temperature Range
SG1731 ..... -55°C to 125°C
SG2731 ..... -25°C to 85°C
SG3731 ..... 0°C to 70°C

Note 2. Range over which the device is functional and parameter limits are guaranteed.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specfiications apply over the operating ambient temperatures for SG1731 with -55°C ≤ T_A ≤ 125°C, SG2731 with -25°C ≤ T_A ≤ 85°C, SG3731 with 0°C ≤ T_A ≤ 70°C, V_S = ±15V, and V_O = ±22V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1731/2731/3731			Units
		Min.	Typ.	Max.	
Oscillator Section					
C_T Charging Current	T_A = 25°C	450	500	550	µA
	$T_A = T_{MIN}$ to T_{MAX}	400		600	µA
2V∆± Input Bias Current	V_{CM} = ±5V			-20	µA
Initial Oscillator Frequency	C_T = 1000pF, 2V∆± = ±5V, T_A = 25°C	22.5	25.0	27.5	KHz
Temperature Stability (Note 3)	C_T = 1000pF, 2V∆± = ±5V			10	%
Error Amplifier Section (Note 5)					
Input Offset Voltage				10	mV
Input Bias Current				3	µA
Input Offset Current				600	nA
Open Loop Voltage Gain	R_L = 2KΩ	70			dB
Output Voltage Swing	R_L = 2KΩ	±10			V
Common-Mode Rejection Ratio		70			dB
Slew Rate (Notes 3 and 4)	T_A = 25°C	5	10		V/µs
Unity Gain Bandwidth (Notes 3 and 4)	T_A = 25°C	0.7	1		MHz
PWM Comparators					
Input Bias Current	$\pm V_T$ = ±3V			6	µA

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1731/2731/3731 Min.	Typ.	Max.	Units
SHUTDOWN Section					
Logic Threshold	$-V_S$ = -3.5V to -15V	$-V_S$+0.8		$-V_S$+2.0	V
SHUTDOWN HIGH Current	$V_{\overline{SHUTDOWN}} = -V_S$+2.4V			400	µA
SHUTDOWN LOW Current	$V_{\overline{SHUTDOWN}} = -V_S$			-1.0	mA
Output Drivers (Each Output)					
HIGH Output Voltage	I_{SOURCE} = 20mA	19.2			V
	I_{SOURCE} = 100mA	19.0			V
LOW Output Voltage	I_{SINK} = 20mA			-19.2	V
	I_{SINK} = 100mA			-19.0	V
Driver Risetime	C_L = 1000pF			300	ns
Driver Falltime	C_L = 1000pF			300	ns
Total Supply Current					
V_S Supply Current	$V_{\overline{SHUTDOWN}} = -V_S$ + 0.8V			14	mA
V_O Supply Current	$V_{\overline{SHUTDOWN}} = -V_S$ + 0.8V			6	mA

Note 3. These parameters, although guaranteed, are not tested in production.
Note 4. Unity Gain Inverting 10KΩ Feedback Resistance.
Note 5. V_{CM} = ±12V.

APPLICATION INFORMATION

SUPPLY VOLTAGE

The SG1731 requires a supply voltage for the control circuitry (V_S) and for the power output drivers (V_O). Each supply may be either balanced positive and negative with respect to ground, or single-ended. The only restrictions are:

1. The voltage between $+V_S$ and $-V_S$ must be at least 7.0V; but no more than 44V.
2. The voltage between $+V_O$ and $-V_O$ must be at least 5.0V; but no more than 44V.
3. $+V_O$ must be at least 5V more positive than $-V_S$. This eliminates the combination of a single-ended positive control supply with a single-ended negative driver supply.

SUBSTRATE CONNECTION

The substrate connection (Pin 10) must always be connected to either $-V_S$ or $-V_O$, whichever is more negative. The substrate must also be well bypassed to ground with a high quality capacitor.

OSCILLATOR

The triangle oscillator consists of two voltage comparators, a set/reset flip-flop, a bi-directional 500µA current source, and an external timing capacitor C_T. A positive reference voltage (2VΔ+) applied to Pin 2 determines the positive peak value of the triangle, and a negative reference voltage (2VΔ-) at Pin 7 sets the negative peak value of the triangle waveform.
Since the value of the internal current source is fixed at a nominal ±500µA, the oscillator period is a function of the selected peak-to-peak voltage excursion and the value of C_T. The theoretical expression for the oscillator period is:

$$T_{OSC} = \frac{2C_T\,dV}{5 \times 10^{-4}} \qquad \text{(Eq.1)}$$

where C_T is the timing capacitor in Farads and dV is V_{OSC} in Volts peak-to-peak.

As a design aid, the solutions to Equation 1 over the recommended range of T_{OSC} and V_{OSC} are given in graphic form in Figure 1. The lower limit on T_{OSC} is 1.85µs, corresponding to a maximum frequency of 350 KHz. The maximum value of V_{OSC}, (2VΔ+) - (2VΔ-), is 10V peak-to-peak for linear waveforms.

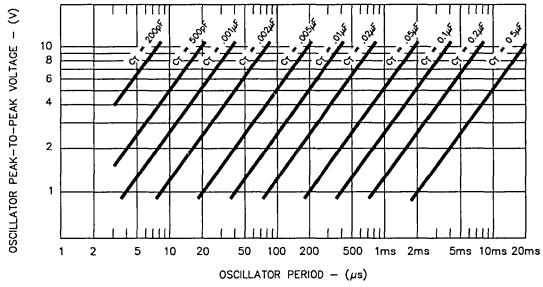


FIGURE 1 - SG1731 OSCILLATOR PERIOD VS. V_{OSC} AND C_T

ERROR AMPLIFIER

The error amplifier of the SG1731 is a conventional internally-compensated operational amplifier with low output impedance. All of the usual feedback and frequency compensation techniques may be use to control the closed-loop gain characteristics. The control supply voltage $\pm V_S$ will determine the input common mode range and output voltage swing; both will extend to within 3V of the V_S supply.

PULSE WIDTH MODULATION

Pulse width modulation occurs by comparing the triangle waveform to a fixed upper ($+V_T$) and lower ($-V_T$) threshold voltage. A crossing above the upper threshold causes Output A to switch to the HIGH state, and a crossing below the lower

APPLICATION INFORMATION (continued)

threshold causes Output B to switch to the HIGH state. If $\pm V_S$ is less than ±8V then $\pm V_T$ can be obtained with resistors from $\pm V_S$. If $\pm V_S$ is greater than ±8V use zeners.

Threshold crossings are generated by shifting the triangle waveform up and down with the error voltage (Pin 5). A positive error voltage will result in a pulse width modulated output at Driver A (Pin 13). Similarly, a negative error voltage produces a pulse train at Driver B (Pin 12). Figure 2 illustrates this process for the case where $V\Delta+$ is greater than V_T.

It is important to note that the triangle shifting circuit also attenuates the waveform seen at C_T by a factor of 2. This results in a waveform at the PWM comparators with a positive peak of $V\Delta+$ and a negative peak of $V\Delta-$, and must be taken into account when selecting the values for $+V_T$ and $-V_T$.

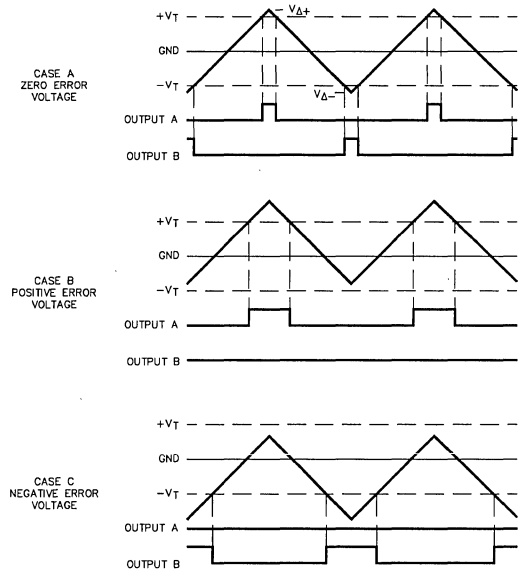


FIGURE 2 - PULSE WIDTH MODULATION WITH NO DEADBAND

APPLICATION CIRCUITS

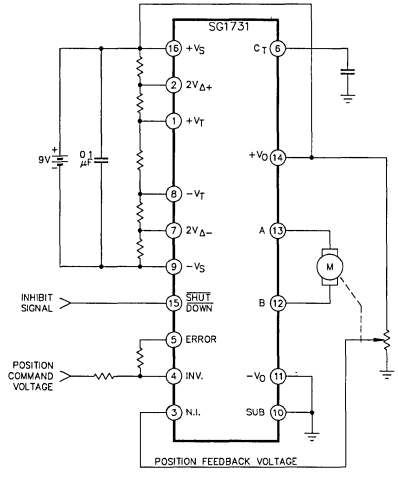


FIGURE 3

In this simple battery-powered position servo, the control supply and driver supply are both single-ended positive with respect to ground.

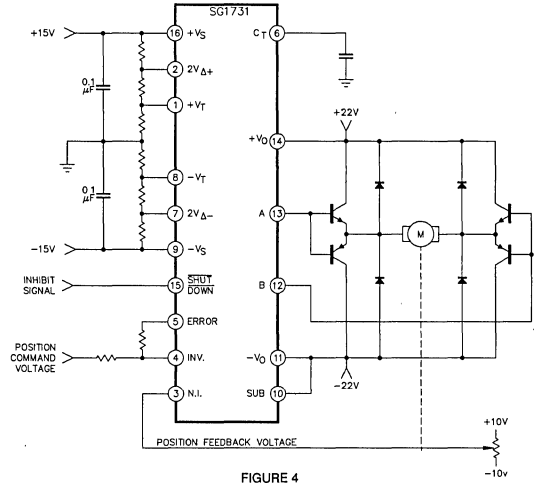


FIGURE 4

A high torque position servo is obtained by buffering the output drivers to obtain higher output current.

APPLICATION CIRCUITS

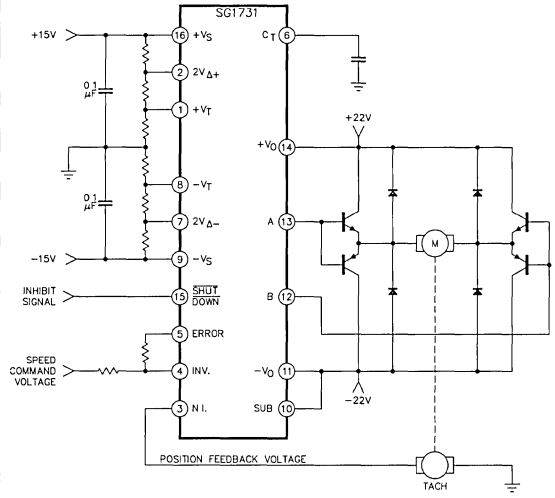


FIGURE 5

Bi-directional speed control results when the feedback voltage transducer is a tachometer.

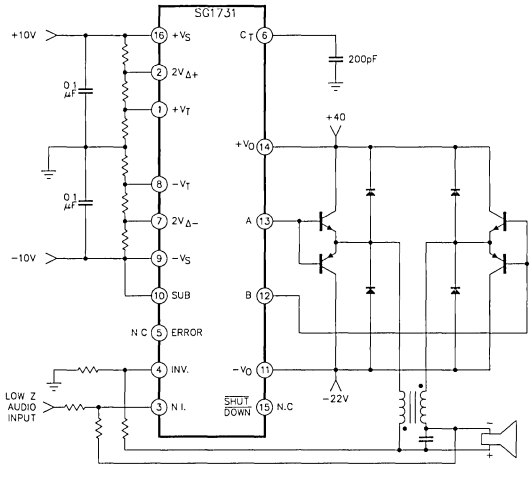


FIGURE 6

The two-quadrant transfer function of the SG1731 is ideal for pulse width modulated audio power amplifiers.

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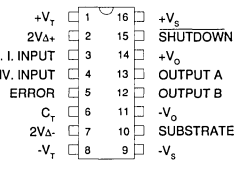
CONNECTION DIAGRAMS & ORDERING INFORMATION (See Note Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG1731J/883B SG1731J SG2731J SG3731J	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 65°C	
16-PIN PLASTIC DIP N - PACKAGE	SG2731N SG3731N	-25°C to 85°C 0°C to 65°C	



Note 1. All packages are viewed from the top.
Note 2. Contact factory for flatpack and leadless chip carrier availability.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

QUAD 2.5 AMP POWER DRIVER

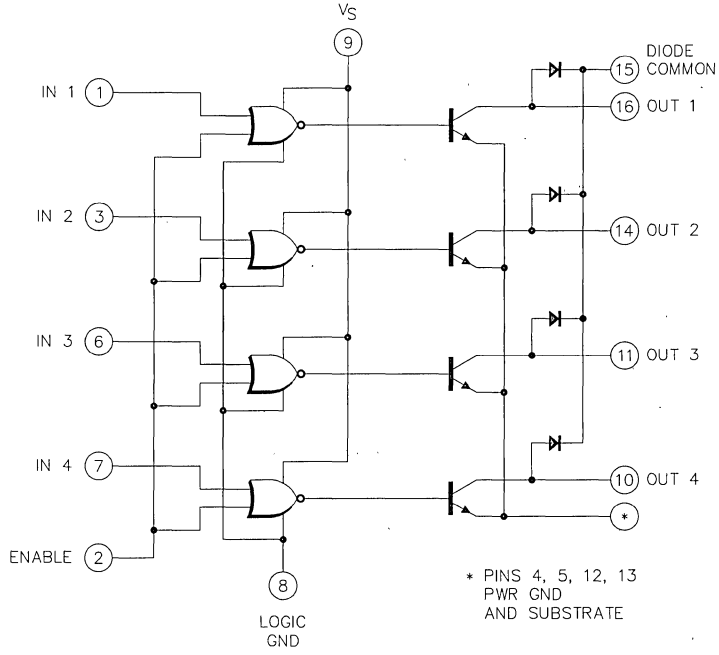
DESCRIPTION

The SG3645 is a quad high voltage, high current driver, ideal for driving stepper motors. Each channel consists of TTL compatible inputs and open collector-Darlington outputs with integral transient suppression diodes. A common enable is provided to disable or enable all four outputs simultaneously. The output stages are capable of sinking 2.5 Amps with breakdown voltages in excess of 60 volts. Thermal shutdown is provided to disable the outputs if excessive die heating occurs. The SG3645 is specified for operation over the ambient temperature range of 0°C to 125°C and is available in the thermally efficient plastic Batwing package.

FEATURES

- **Peak output currents to 3.5A**
- **Output voltages to 60V**
- **Integral clamp diodes**
- **Common enable pin**
- **TTL compatible inputs**
- **Thermal shutdown protection**
- **Available in 16 pin Batwing DIP and a 20 pin Batwing SOIC**

BLOCK DIAGRAM



TRUTH TABLE

INPUT	ENABLE	OUTPUT
L	L	ON
L	H	OFF
H	L	OFF
H	H	OFF

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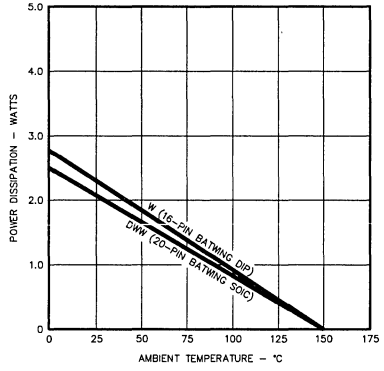
ABSOLUTE MAXIMUM RATINGS (Note 1)

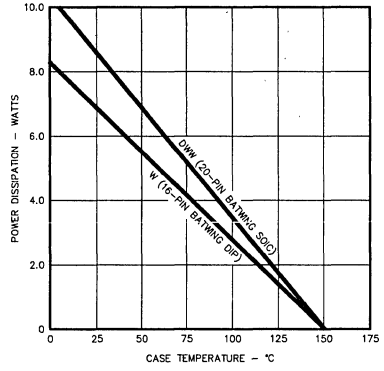
Output Voltage 70V
Output Current (Each Output)
  Continuous (Note 2) 3.0A
  Peak (1% Duty Cycle, t_{ON} = 10ms) 4.0A
Supply Voltage (V_S) 25V
Logic Input Voltage 7V
Logic Supply to Substrate Voltage 40V
Operating Junction Temperature
  Plastic (W, DWW-Package) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device. All currents are positive into the specified terminal.
Note 2. Maximum continuous output current is limited by the thermal resistance of the package-heat sink combination.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 3)

Supply Voltage (V_S) ..... 4.5V to 20V
Output Voltage 60V
Logic Supply to Substrate Voltage 25V
Output Current (Each Output)
  Continuous 2.5A
  Peak (1% Duty Cycle, t_{ON} = 10ms) 3.5A
Operating Ambient Temperature Range
  SG3645 ..... 0°C to 125°C

Note 3. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS (Static and Dynamic)

(Unless otherwise specified, these specifications apply for the operating ambient temperatures for SG3645 with 0°C ≤ T_J ≤ 125°C and V_S = 5V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.) (Note 4)

Parameter	Test Conditions	SG3645 Min.	SG3645 Typ.	SG3645 Max.	Units
Logic 1 Input Voltage (V_{IH})		2			V
Logic 0 Input Voltage (V_{IL})				0.8	V
Supply Current (I_S - OFF)	$V_{IN} = V_{EN}$ = 5V, V_S = 20V		8	15	mA
(I_S - ON)	$V_{IN} = V_{EN}$ = 0V, V_S = 20V		21	35	mA
Input High Current ($I_{IN(H)}$)	V_{IN} = 5V; V_S = 20V			10	µA
($I_{EN(H)}$)	V_{EN} = 5V; V_S = 20V			10	µA
Input Low Current ($I_{IN(L)}$)	V_{IN} = 0V; V_S = 20V		-50	-250	µA
($I_{EN(L)}$)	V_{EN} = 0V; V_S = 20V		-70	-250	µA
Output Saturation Voltage (V_{SAT})	$V_{IN} = V_{EN}$ = 0.8V; V_S = 4.5V				
(Note 5)	I_{OUT} = 1.5A		1.2	1.75	V
	I_{OUT} = 2.5A		1.8	2.65	V
Output Leakage Current (I_{CEX})	(Per Truth Table) V_S = 20V; V_{CEX} = 60V				
	T_J = 25°C			25	µA
	T_J = 0°C to 125°C			250	µA
Diode Forward Voltage (V_F)	I_F = 1.5A		1.5	2.1	V
(Note 5)	I_F = 2.5A		1.8	2.65	V

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG3645 Min.	SG3645 Typ.	SG3645 Max.	Units
Diode Leakage Current (I_R)	V_R = 60V				
	T_J = 25°C			25	µA
	T_J = 125°C			250	µA
Input/Enable, Turn-on Delay (t_{ON}) (Note 6)	T_J = 25°C; V_S = 5V, I_{OUT} = 1.5A, V_{OUT} = 45V, Duty Cycle = 10%		500	1500	ns
Input/Enable, Turn-off Delay (t_{OFF}) (Note 6)	T_J = 25°C; V_S = 5V, I_{OUT} = 1.5A, V_{OUT} = 45V, Duty Cycle = 10%		500	1500	ns
Thermal Shutdown (T_{TH}) (Note 6)	Measured at Junction Temperature	125	150		°C

Note 4. Although device performance is guaranteed over the recommended junction temperature range, testing is not performed at the temperature extremes.
Note 5. These parameters are tested using pulse techniques to minimize device heating.
Note 6. These parameters, although guaranteed over the recommended operating conditions, are not tested in production.

CHARACTERISTIC CURVES

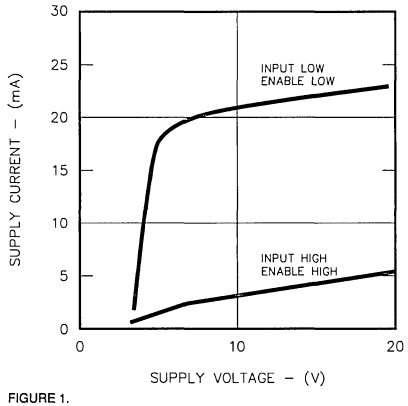


FIGURE 1.
SUPPLY CURRENT

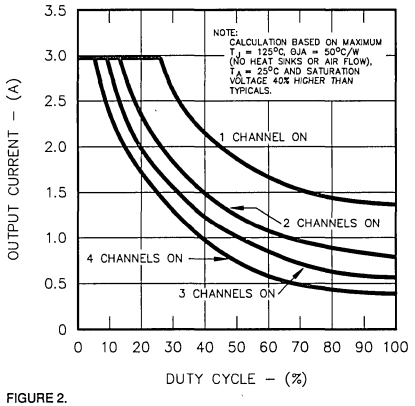


FIGURE 2.
RECOMMENDED MAXIMUM PEAK CURRENT
VS. DUTY CYCLE

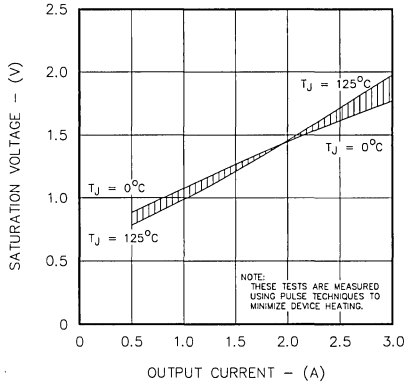


FIGURE 3.
SATURATION VOLTAGE VS. OUTPUT CURRENT

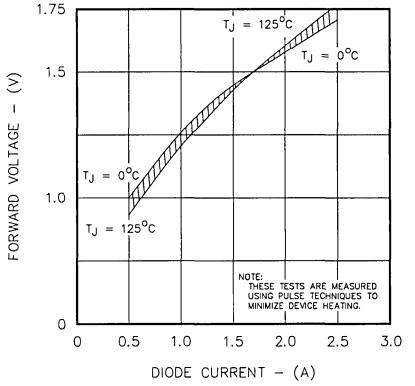


FIGURE 4.
DIODE FORWARD VOLTAGE VS. DIODE CURRENT

APPLICATION CIRCUITS

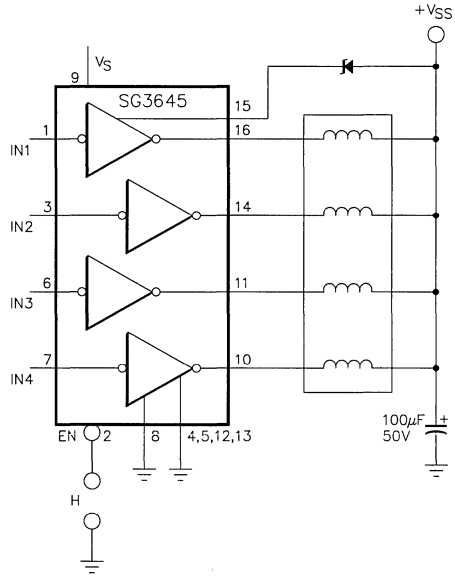
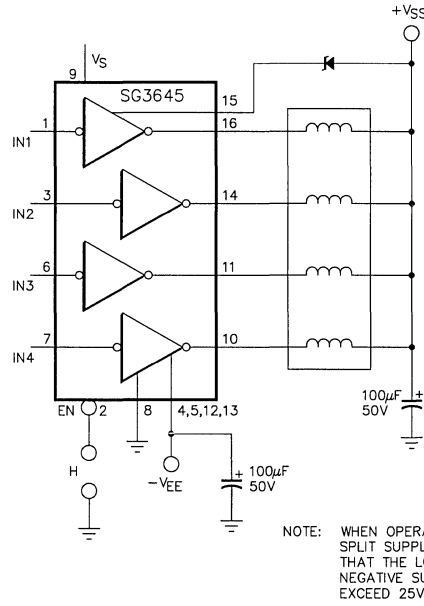


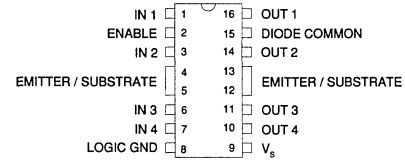
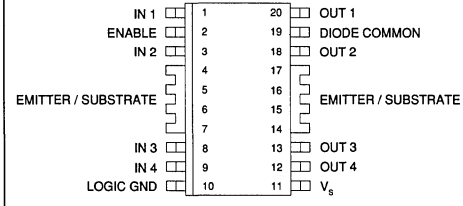
FIGURE 5 - POSITIVE SUPPLY



NOTE: WHEN OPERATING USING A SPLIT SUPPLY, INSURE THAT THE LOGIC GROUND TO NEGATIVE SUPPLY DOES NOT EXCEED 25V.

FIGURE 6 - SPLIT SUPPLY

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Note Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN PLASTIC BATWING W - PACKAGE	SG3645W	0°C to 70°C	
20-PIN PLASTIC BATWING S.O.I.C. DWW - PACKAGE	SG3645DWW	0°C to 70°C	

Note 1. All parts are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

DUAL SOLENOID / MOTOR DRIVER

DESCRIPTION

The SG3663 is a dual high-voltage, high-current monolithic I.C. recommended for driving solenoids and stepper motors. Each output stage contains sink/source drivers rated to ±3.5A peak currents with breakdowns in excess of 50V. Internal suppression diodes provide protection when switching inductive loads. The output stage can be configured to drive two separate loads or a single load in an H-bridge configuration.

The SG3663 offers load current control through the implementation of an internal current sense comparator to control the high side driver. Peak and average currents are set by controlling the threshold voltage on the sense comparator. A mode select pin determines if the SG3663 is operating in the chop or non-chop mode.

The SG3663 is available in two types of power SIP and is rated to junction temperatures of 0°C to 125°C.

FEATURES

- **Dual outputs rated at ±3.5A peak current**
- **Chop or non-chop load current control**
- **Current sense comparator with variable threshold and hysteresis**
- **Internal clamp diodes for transient suppression**
- **Single supply operation (8V to 50V)**
- **Thermal shutdown protection**
- **Available in two different power SIP's rated at θ_{JC} < 2°C/W**

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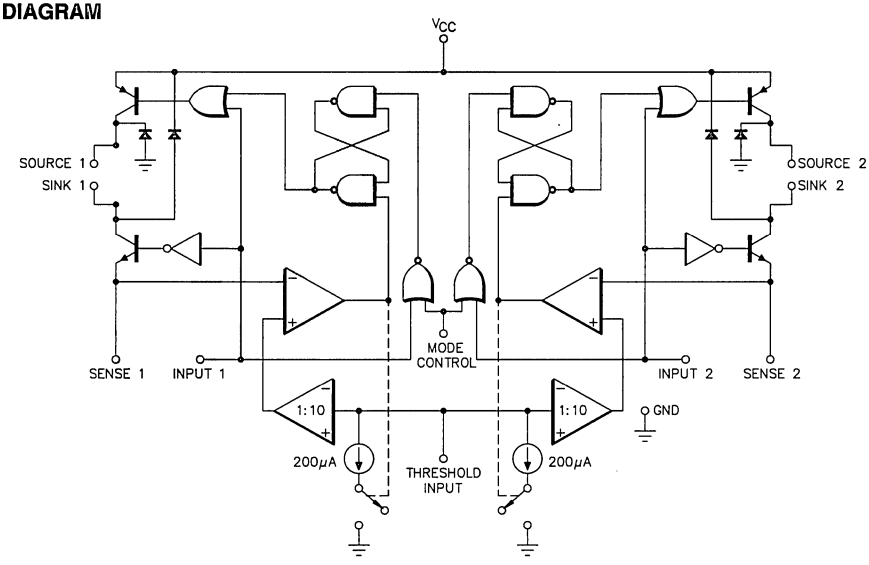
BLOCK DIAGRAM



TRUTH TABLE

INPUT	MODE CONTROL	V_{SENSE}	SOURCE DRIVER	SINK DRIVER
0	0 (Non-chop)	< V_{TH} /10	ON	ON
0	0 (Non-chop)	> V_{TH} /10	OFF	ON
0	1 (Chop)	< V_{TH} /10	ON	ON
0	1 (Chop)	> V_{TH} /10	OFF	ON
1	DC	DC	OFF	OFF

DC = Don't care

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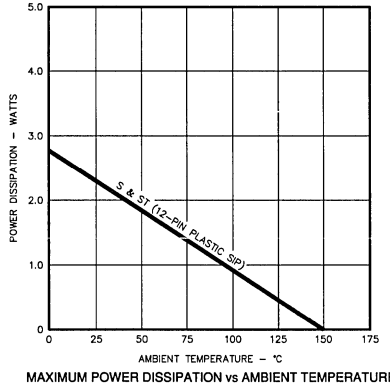
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V_{CC}) 55V
Logic Input Voltage 7V
Threshold Input Voltage (V_{TH}) 5V
Source/Sink Output Current (Each Output):
  Continuous ..... ±3.5A
  Peak ..... ±4.4A

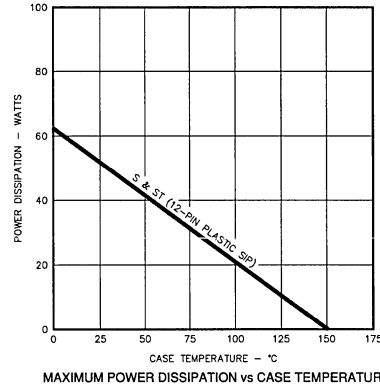
Operating Junction Temperature ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device. All currents are positive into the specified terminal.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage (V_{CC}) ..... 8V to 50V
Source/Sink Output Current (Each Output):
  Continuous ..... ±3.0A
  Peak ..... ±3.5A

Threshold Input Voltage (V_{TH}) ..... 0.6V to 5.0V
Ambient Temperature Range (T_A) ..... 0°C to 70°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply for the operating ambient temperature of T_A = 25°C, V_{CC} = 50V, and R_{SENSE} = 0.1Ω. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG3663			Units
		Min.	Typ.	Max.	
Supply Current ($I_{CC(ON)}$)	$V_{IN} = V_{MODE} = 0V$, $I_{OUT} = 0A$		12	25	mA
($I_{CC(OFF)}$)	$V_{IN} = V_{MODE} = 2.7V$		12	25	mA
Logic 1 Input Voltage (V_{IH})	Input / Mode Control	2.0			V
Logic 0 Input Voltage (V_{IL})	Input / Mode Control			0.8	V
Logic 1 Input Current (I_{IH})	$V_{IN} = V_{MODE} = 2.4V$			100	µA
Logic 0 Input Current (I_{IL})	$V_{IN} = V_{MODE} = 0.4V$			-1.0	mA
Threshold Input Current (I_{THH})	V_{TH} = 0.6V to 5.0V, $V_{TH} \geq V_{SENSE}$ x 10			-100	µA
Threshold Hysteresis Current (I_{HYS})	V_{TH} = 0.6V to 5.0V, $V_{TH} \geq V_{SENSE}$ x 10	140	200	260	µA
Source Output Saturation Voltage	$V_{IN} = 0V$, $I_{OUT} = -2A$		1.85	2.2	V
(V_{SAT}) (Note 3)	$V_{IN} = 0V$, $I_{OUT} = -3.5A$		2.0	2.6	V
Sink Output Saturation Voltage	$V_{IN} = 0V$, $I_{OUT} = 2A$		1.3	1.8	V
(V_{SAT}) (Note 3)	$V_{IN} = 0V$, $I_{OUT} = 3.5A$		2.1	2.6	V
Source/Sink Leakage Current (I_{CEX})	$V_{IN} = 2.4V$, $V_{SOURCE} = 0V$			100	µA
	$V_{IN} = 2.4V$, $V_{SINK} = 50V$			100	µA
Source Diode Forward Voltage (V_F)	$V_{IN} = 2.4V$, $I_{SOURCE} = -2A$		-1.2	-1.6	V
	$V_{IN} = 2.4V$, $I_{SOURCE} = -3.5A$		-1.4	-2.0	V

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG3663 Min.	SG3663 Typ.	SG3663 Max.	Units
Sink Diode Forward Voltage (V_F)	V_{IN} = 2.4V, I_{SINK} = 2A		1.75	2.2	V
	V_{IN} = 2.4V, I_{SINK} = 3.5A		2.3	2.8	V
Diode Leakage Current (I_R)	V_{IN} = 2.4V, V_{SOURCE} = 50V			100	µA
	V_{IN} = 2.4V, V_{SOURCE} = 0V			100	µA
Output Current Regulation (I_{REG})	V_{TH} = 2.0V to 3.6V	-5		5	%
	V_{TH} = 1.0V to 2.0V	-10		10	%
	V_{TH} = 0.6V to 1.0V	-25		25	%
Propagation Delay (Note 4) (T_{PLH})	50% V_{IN} to 50% V_{OUT}			2.5	µs
(T_{PHL})	I_{OUT} = 2A (resistive)			3.0	µs
Thermal Shutdown (T_{TH})			160		°C

Note 3. These parameters are tested using pulse techniques to minimize device heating.
Note 4. These parameters are guaranteed by design but not 100% tested in production.

CHARACTERISTIC CURVES

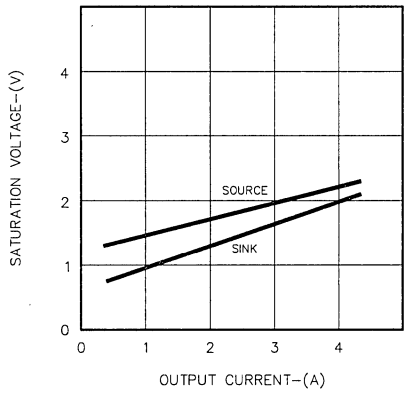


FIGURE 1.
OUTPUT SATURATION VOLTAGE
VS. OUTPUT CURRENT

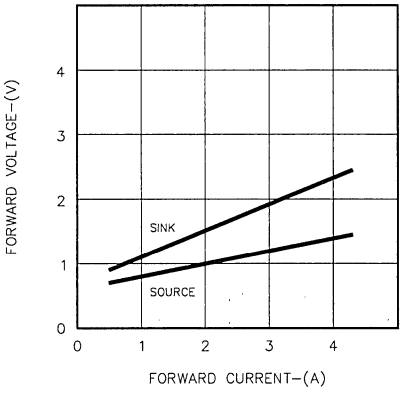


FIGURE 2.
DIODE FORWARD VOLTAGE
VS. FORWARD CURRENT

APPLICATION NOTES

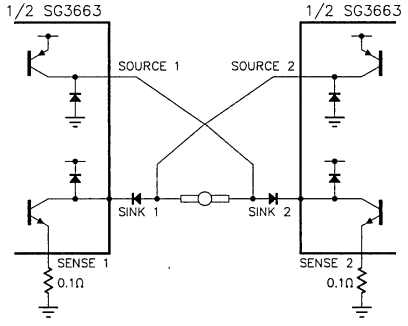


FIGURE 3 - H-BRIDGE CONFIGURATION

1. When using the SG3663 in an H-bridge configuration, external diodes must be used. These diodes must be high speed with voltage ratings above 70V and capable of handling 5A. Care should also be taken not to simultaneously turn on both inputs.

2. PC Board layout - The output current is controlled by both the voltage of the Sense pin and the sense resistor. Because of the large currents and low resistance, it is critical to have extremely good PC board layout to reduce parasitic wiring resistances which could add to the sense resistor and reduce the output current.

3. Decoupling of the V_{CC} supply with a 10µF electrolytic is recommended.

FUNCTIONAL DESCRIPTION

NON-CHOP MODE

A logic "0" applied to the Mode Control pin will cause the SG3663 to operate in the non-chop mode. If a logic "0" then appears on the Input pin, both the sink and source transistors will turn-on causing the load current to rise according to:

$$V_{CC} - V_{SAT1} - V_{SAT2} - L\frac{d_i}{d_t} - IR_{SENSE} = 0$$

solving for I(t)

$$1) \qquad I(t) = \frac{V_{CC} - V_{SAT1} - V_{SAT2}}{R_{SENSE}} (1 - e^{-(R/L)t})$$

for I(t=0) = 0A

This current will rise exponentially until it reaches a peak value described in Equation 2.

$$2) \qquad I_{PEAK} = \frac{V_{TH} / 10}{R_{SENSE}}$$

The comparator then trips, setting the latch and turning off the source transistor.

Since the source transistor has been disabled and the coil current cannot change instantaneously the current flow will be through D2 and will exponentially decay per the following:

$$3) \qquad I(t) = - I_{PEAK} e^{-(R/L)(t - T)}$$

The load current will decay to "0" unless the latch is reset by pulling the input high and then low again to activate the source driver.

When the input goes high both the sink and source turn off and the current path is through D2, L, and D1. Figure 5 is a graphical representation of the above discussion.

CHOP MODE (Note: Only one section can be used at one time.)

A logic signal "1" on the Mode Control pin will cause the SG3663 to operate in the chop mode. As in the non-chop mode a logic "0" on the Input pin will cause the sink and source transistor to turn on with Equation 4 describing the current in the load.

$$4) \qquad I(t) = \frac{V_{CC} - V_{SAT1} - V_{SAT2}}{R_{SENSE}} (1 - e^{-(R/L)t})$$

Once I_{PEAK} is reached the source transistor turns-off and a current source ($I_{HYS} \approx +200\mu A$) is activated on the threshold pin. This current source lowers the effective threshold voltage by an amount determined by a resistor value R_{HYS}. The load current will decay until the new threshold is reached at which time the source transistor is activated and the threshold is restored to its original value by turning off the current source. The output current will rise again until the original peak value has been reached. This chopping action will continue until the Input pin is taken high causing the load current to decay to 0A. Figure 6 is a graphical representation of the chop-mode action.

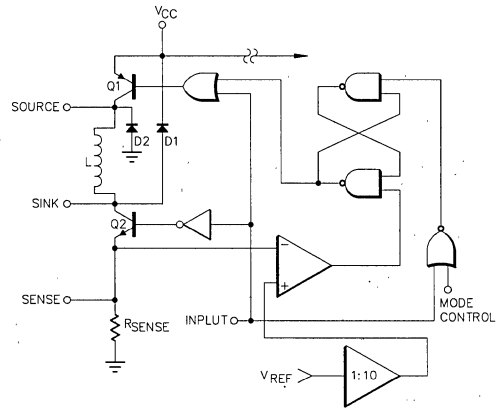


FIGURE 4 - TYPICAL APPLICATION IN NON-CHOP MODE (Refer to Figures 4 & 5)

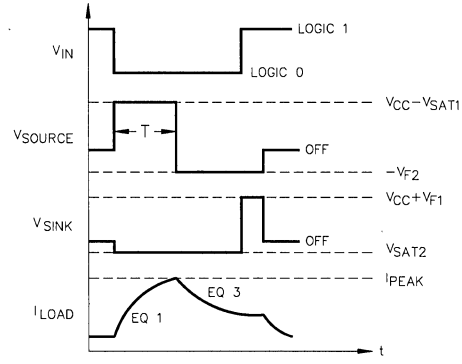


FIGURE 5 - NON-CHOP MODE

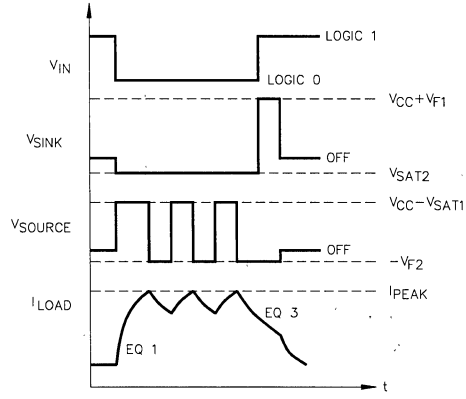


FIGURE 6 - CHOP MODE (Refer to Figure 4)

DESIGN EXAMPLES - CHOP MODE (Refer to Figure 4)

Example 1 -
Desired: 3.0A Peak, 20KHz Chop Frequency
Given: V_{CC} = 50V, L = 2mH, R_{SENSE} = 0.1Ω

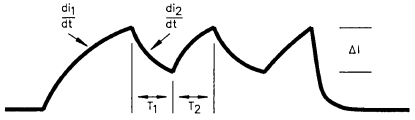


FIGURE 7.

1) $V_{SENSE} = (3.0A) \times (0.1\Omega) = 300mV$

$V_{TH} = 300mV \times 10 = 3V$

2) $T = T_1 + T_2 = \frac{1}{20KHz}$

$V = L\frac{d_{i1}}{d_t}$ $\qquad$ $V = L\frac{d_{i2}}{d_t}$

$\frac{d_{i1}}{d_t} = \frac{V_{CC} - V_{SAT1} - V_{SAT2}}{L}$ $\qquad$ $\frac{d_{i2}}{d_t} = \frac{-V_{SAT2} - V_{P2}}{L}$

$= \frac{50V - 2.0V - 2.0V}{2mH}$ $\qquad$ $= \frac{-2.0V - 2.0V}{2mH}$

$= 23A/ms$ $\qquad$ $= -2.0A/ms$

$\therefore T \cong \frac{\Delta I}{23A/ms} + \frac{\Delta I}{2.0A/ms}$

$\Delta I \cong \frac{\frac{1}{20KHz}}{(\frac{1}{2.0} + \frac{1}{23}) \times 10^{-3}} = 92mA$

3) $\%\ HYS = \frac{\Delta I}{I_{PEAK}}$

$= \frac{0.092A}{3A}$

$= 3\%$

4) $\Delta V_{TH} = (3\%)\ (3V)$

$= 90mV$

5) $R_{HYS} = \frac{\Delta V_{TH}}{200\mu A}$

$= \frac{90mV}{200\mu A}$

$= 450\Omega$

Example 2 -
A voltage divider on the reference supply can be used to establish the necessary peak and hysterisis current.

Desired: 3.0A Peak, 10% Hysterisis Current
Given: V_{REF} = 5.0V, R_{SENSE} = 0.1Ω

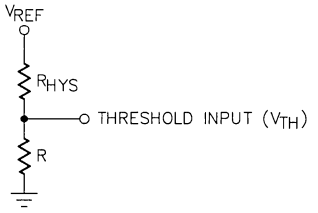


FIGURE 8.

$R_{HYS} = \frac{V_{REF} \times \%\ Hysterisis}{200\mu A}$

$R = \frac{R_{HYS} \times V_{TH}\ (peak)}{V_{REF} - V_{TH}\ (peak)}$

$R = \frac{R_{HYS}\ (I_{PEAK} \times R_{SENSE} \times 10)}{V_{REF} - (I_{PEAK} \times R_{SENSE} \times 10)}$

$\therefore R_{HYS} = \frac{5.0V \times 10\%}{200\mu A}$

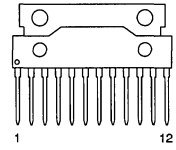
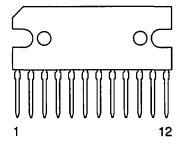
$= 2.5K\Omega$

$R = \frac{2.5K\Omega\ (3.0A \times 0.1\Omega \times 10)}{5.0V - (3.0A \times 0.1\Omega \times 10)}$

$= 3.75K\Omega$

5

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
12-PIN PLASTIC SIP ST - PACKAGE	SG3663ST	0°C to 70°C	 1. GROUND 2. IN 1 3. SENSE 1 4. SINK 1 5. SOURCE 1 6. THRESHOLD INPUT 7. V_{CC} 8. SOURCE 2 9. SINK 2 10. SENSE 2 11. IN 2 12. MODE CONTROL
12-PIN PLASTIC SIP S - PACKAGE	SG3663S	0°C to 70°C	 1. GROUND 2. IN 1 3. SENSE 1 4. SINK 1 5. SOURCE 1 6. THRESHOLD INPUT 7. V_{CC} 8. SOURCE 2 9. SINK 2 10. SENSE 2 11. IN 2 12. MODE CONTROL

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

DUAL HAMMER DRIVER

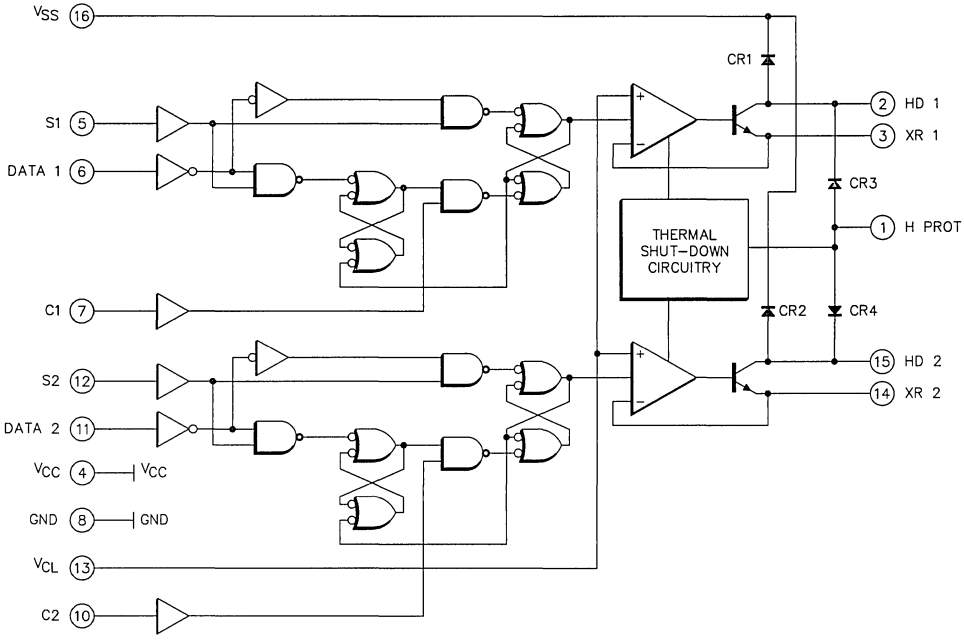
DESCRIPTION

The SG3700 is a monolithic integrated circuit that will provide up to 900mA of current to each output. An external sense resistor and an external reference control voltage is required for programming the output current to the desired value. On-chip TTL-compatible logic is provided for timing of the output current pulse duration.

FEATURES

- **Output current to 900mA**
- **Output voltage to 40V**
- **Built-in clamp diodes**
- **Thermal protection**
- **Logic control of pulse duration**

BLOCK DIAGRAM



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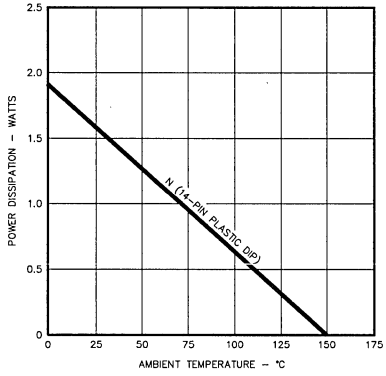
ABSOLUTE MAXIMUM RATINGS (Note 1)

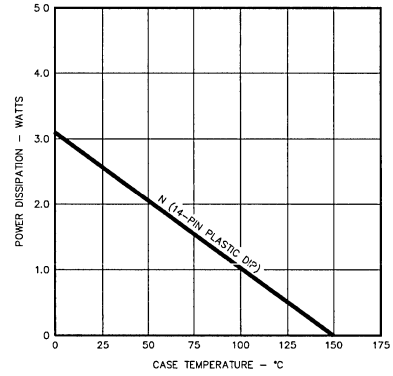
Driver Supply Voltage (V_{SS}) 42V
TTL Supply Voltage (V_{CC}) 7V
TTL Logic Input Voltage With Respect To Ground (V_{IN}) 5.5V
Output Current, Each Driver 1A
Control Voltage (V_{CL}) 2V
V_{HPROT} ..... V_{SS}
Operating Junction Temperature
Plastic (N- Package) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Values beyond which damage may occur.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Driver Supply Voltage (V_{SS}) 40V
TTL Supply Voltage (V_{CC}) ..... 4.75V to 5.25V
Control Voltage (V_{CL}) (On State) ..... 1.2V to 1.8V
Control Voltage (V_{CL}) (Off State) ..... 0V to 0.4V
Output Current, Continuous 900mA
Operating Ambient Temperature Range
SG3700 ..... 0°C to 70°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specfiications apply over the operating ambient temperatures for SG3700 with $0°C \le T_A \le 70°C$. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG3700			Units
		Min.	Typ.	Max.	
Logic Section					
Low Level Input Voltage(V_{IL}) (All Inputs)				0.8	V
Low Level Input Current (I_{IL}) (All Inputs)	V_{CC} = 5.25V, V_{IN} = 0.4V			-1.6	mA
High Level Input Voltage (V_{IH}) (All Inputs)		2.0			V
High Level Input Current (I_{IH}) (All Inputs)	V_{CC} = 5.25V, V_{IN} = 2.4V			40	µA
	V_{CC} = 5.25V, V_{IN} = 5.5V			1.0	mA
Input Clamp Voltage (V_{IK})	V_{CC} = 4.75V, I_{IN} = 12mA			-1.5	V
Control Section					
Control Voltage Input Current (I_{CL})	V_{CC} = 0V to 1.8V		-0.2	-1.0	µA
Protection Section					
HPROT Output Voltage, Low State (Thermal Shutdown) (V_{HPROT})	I_{HPROT} = 1.5mA			2.0	V
HPROT Leakage to Ground (I_{HPROT})	V_{HPROT} = 0V, V_{SS} = 40V			-100	µA
HPROT Leakage from V_{SS} (I_{HPROT})	V_{HPROT} = V_{SS} = V_{HD} = 40V, V_{CC} = 5V			5	µA

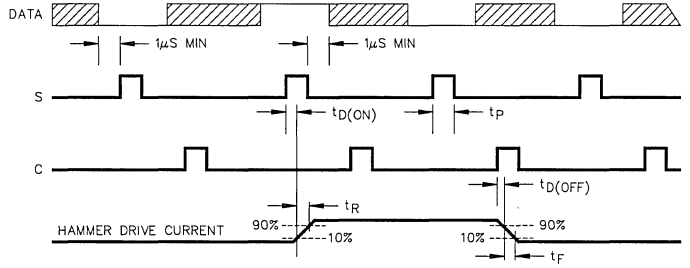
ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG3700 Min.	SG3700 Typ.	SG3700 Max.	Units
Output Section					
Output Transistor Saturation Voltage ($V_{CE(SAT)}$)	I_C = 900mA, V_{CL} = 1.2V to 1.8V			1.5	V
Output Current Low, Off State (I_{OL})	V_{SS} = V_{HD} = 40V			1.0	mA
XR_1, XR_2 Voltage, On State (V_{XR})	Driver on, V_{CL} = 1.2V to 1.8V, T_A =25°C	$0.97V_{CL}$	V_{CL}	$1.03V_{CL}$	V
XR_1, XR_2 Voltage, Off State (V_{XR}) (Note 3)	Driver on, V_{CL} = 0V			450	mV
Forward Voltage (CR_1, CR_2) (V_F)	I_F = 900mA			3.0	V
Forward Voltage (CR_3, CR_4) (V_F)	I_F = 1mA			1.0	V
Leakage Current (CR_1, CR_2) (I_R)	V_{SS} = 40V, V_{HD} = 0V			100	µA
Supply Section					
Total Supply Current (I_{CC})	Outputs in Off State, Logic Inputs Low		50	70	mA

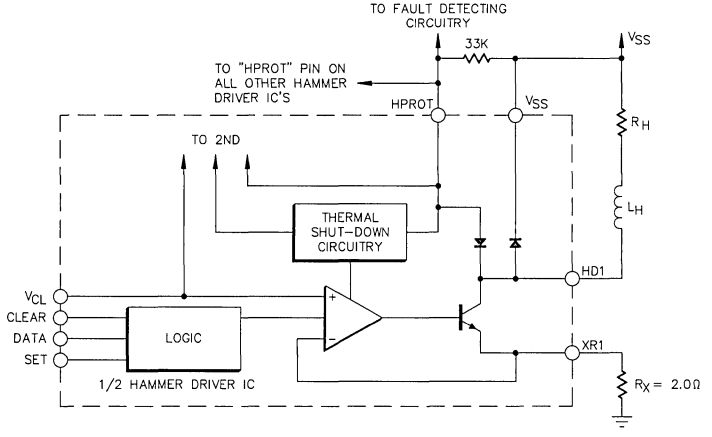
Parameter	Test Conditions	SG3700 Min.	SG3700 Typ.	SG3700 Max.	Units
Dynamic Characteristics (V_{SS} = 40V, R_X = 2Ω, R_H = 32Ω, L_H = 0 and T_A = 25°C)					
Pulse Width, S & C Inputs (t_P)	See Figure 1	1			µs
Hammer Drive Current Turn-on Delay ($t_{D(ON)}$)			3		µs
Hammer Drive Current Turn-off Delay ($t_{D(OFF)}$)			3		µs
Hammer Drive Rise Time (t_R)			30		µs
Hammer Drive Fall Time (t_F)			30		µs

Note 3. V_{XR} voltage in off-state shall not exceed specified value when V_{CC} is changed from +5V to 0V.

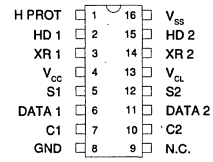
SWITCHING WAVEFORM AND TIMING DIAGRAM - FIGURE 1



TYPICAL APPLICATION



CONNECTION DIAGRAMS & ORDERING INFORMATION (See Note Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN PLASTIC DIP N - PACKAGE	SG3700N	0°C to 70°C	

Note: 1. All parts are viewed from the top.

SG3718
ADVANCED DATA SHEET

STEPPER MOTOR DRIVER

DESCRIPTION

The SG3718 is a monolithic integrated circuit intended to drive one phase winding of a bipolar stepper motor with chopper control of the phase current.

Current levels may be selected in three steps by means of two logic inputs which selects one of the three current comparators. Each comparator is set to a different threshold level with the divider network off of the reference input. A monostable programmed by an external RC network sets the current decay time to control the average current in the winding. A seperate logic input controls the direction of current flow. The output section features an H-bridge with four fast recovery commutating diodes for current recirculation. An external connection to the lower emitters is available for insertion of a sensing resistor.

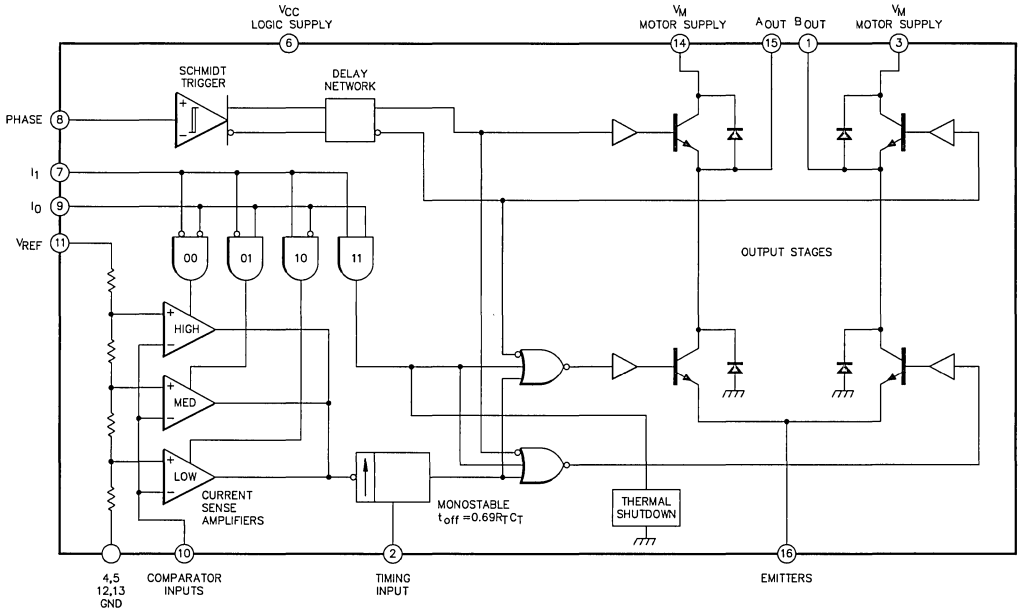
The SG3718 is available in 16 pin plastic batwing, 20 pin batwing S.O.I.C. and 28 pin PLCC packages.

FEATURES

- **Pin to pin compatible with all industry standard 3717s / 3718s**
- **Full-step, half-step and micro-step capability**
- **Bipolar output current up to 1.5A**
- **Wide range of motor supply voltage 10-46V**
- **Built-in fast recovery commutating diodes**
- **Current levels selected in steps or varied continuously**
- **Output stage shoot-through protection**
- **Thermal shutdown protection**
- **Low saturation output stage**
- **Designed for unstabilized motor supply**

5

BLOCK DIAGRAM (Pin numbers are for plastic batwing W - Pkg only.)



TRUTH TABLE

Input 0 (I_0)	Input 1 (I_1)	Mode
H	H	No current
L	H	Low current
H	L	Medium current
L	L	High current

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ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltages
- Logic Supply, V_{CC} ..... 0V to 7V
- Output Supply, V_M ..... 0V to 50V

Input Voltage
- Logic Inputs ..... -0.3V to 6V
- Analog Input ..... -0.3V to V_{CC}
- Reference Input ..... -0.3V to15V

Input Currents
- Logic Inputs ..... -10mA
- Analog Inputs ..... -10mA

Output Current ..... ±1.5A

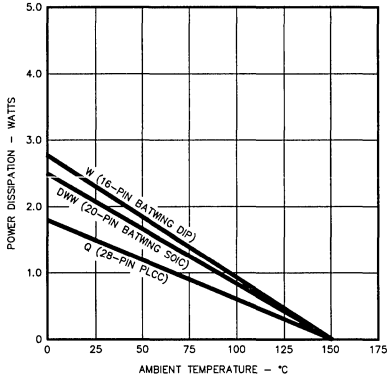
Operating Junction Temperature
- Plastic (W, DWW, Q Packages) .....125°C

Storage Temperature Range ..... -65°C to 150°C

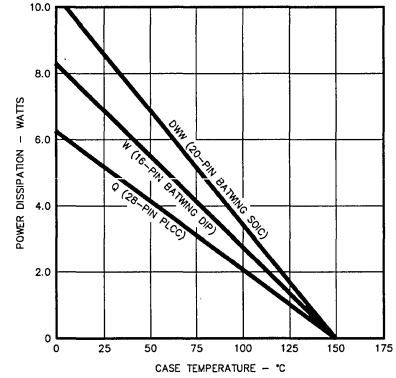
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1. Values beyond which damage may occur. All voltages are measured with respect to ground, and all currents are defined as positive flowing into the device (unless otherwise specified).

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage
- Logic Supply, V_{CC} ..... 4.5V to 5.5V
- Output Supply, V_M .....10V to 45V

Output Current ..... ±20mA to ±1.2A

Logic Input Rise Times ..... < 2µsec

Logic Input Fall Times ..... < 2µsec

Operating Ambient Temperature Range
- SG3718 ..... 0°C to 70°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specfiications apply over the operating ambient temperatures for SG3718 with $0°C \le T_A \le 70°C$, $10V < V_M < 45V$, $4.5V < V_{CC} < 5.5V$, and $V_R = 5V$ (Refer to the test circuit, Figure 1). Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG3718 Min.	SG3718 Typ.	SG3718 Max.	Units
Bias Supply					
Logic Supply Current, I_{CC}			9	30	mA
Total Power Consumption (Note 3)					
Total Power Dissipation	$I_M = 0.5A$, $f_s = 30KHz$, $V_M = 36V$		1.4	1.7	W
	$I_M = 0.8A$, $f_s = 30KHz$, $V_M = 36V$		2.8	3.3	W
	$I_M = 1A$, $f_s = 30KHz$, $V_M = 36V$		3.1	3.8	W
Thermal Shutdown Temperature	Self heating	150		190	°C
Logic Inputs					
Logic Input Low Voltage				0.8	V
Logic Input High Voltage		2			V
Logic Low Voltage Input Current	$V_I = 0.4V$	-400			µA
High Voltage Input Current	$V_I = 2.4V$			20	µA
Reference Input Current	$V_R = 5V$		0.4	1.0	mA

Note 3. These parameters, although guaranteed, are not tested in production.

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG3718 Min.	SG3718 Typ.	SG3718 Max.	Units
Comparators					
Low Threshold Voltage	V_R = 5V, I_0 = L, I_1 = H	65	80	90	mV
Medium Threshold Voltage	V_R = 5V, I_0 = H, I_1 = L	230	250	270	mV
High Threshold Voltage	V_R = 5V, I_0 = L, I_1 = L	390	420	440	mV
Input Current		-20		+20	µA
Cutoff Time, T_{OFF}	R_T = 56KΩ, C_T = 820pF, V_M = 10V, T_{ON} > 5µsec	25	30	35	µs
Turn Off Delay, T_D	T_A = 25°C, dv_C / dt > 50mV/µsec			2	µs
Source Diode - Transistor Pair					
Saturation Voltage, V_{SAT}	I_M = -0.5A, (See Figure 2)		1.05	1.2	V
	I_M = -0.8A		1.2	1.4	V
	I_M = -1A		1.3	1.5	V
Leakage Current	V_M = 40V, I_0 = H, I_1 = H			100	µA
Diode Forward Voltage, V_F	I_M = -0.5A		1.1	1.5	V
	I_M = -0.8A		1.2	1.45	V
	I_M = -1A		1.3	1.6	V
Sink Diode - Transistor Pair					
Saturation Voltage, V_{SAT}	I_M = 0.5A		1.0	1.2	V
	I_M = 0.8A		1.0	1.25	V
	I_M = 1A		1.2	1.3	V
Leakage Current	V_M = 40V, I_0 = H, I_1 = H			100	µA
Diode Forward Voltage, V_F	I_M = 0.5A		1.1	1.5	V
	I_M = 0.8A		1.3	1.7	V
	I_M = 1A		1.1	2.0	V

PIN DESCRIPTION

Pin Name	Description
OUTPUT B (B_{OUT})	Output connection (with OUTPUT A). The output stage is a "H" bridge formed by four transistors and four diodes suitable for switching applications.
PULSE TIME (TIMING)	A parallel RC network connected to this pin sets the OFF time of the lower power transistors. The pulse generator is a monostable triggered by the rising edge of the output of the comparators (T_{OFF} = 0.69 R_TC_T).
SUPPLY VOLTAGE B (V_M)	Supply voltage input for output stage
GROUND	Ground connection. This will provide good heat conduction from die to printed circuit copper.
LOGIC SUPPLY (V_{CC})	Supply voltage input for logic circuitry.
PHASE	This TTL-compatible logic input sets the direction of current flow through the load. A high level causes current to flow from OUTPUT A (source) to OUTPUT B (sink). A schmitt trigger on this input provides good noise immunity and delay circuit prevents output stage short circuits during switching.

Pin Name	Description
INPUT 1 (I_1)	This pin and INPUT 0 are logic inputs which select the outputs of the three comparators to set the current level. Current also depends on the sensing resistor and reference voltage. See truth table.
INPUT 0 (I_0)	See INPUT 1.
COMPARATOR INPUT (CURRENT)	Input connected to the three comparators. The voltage across the sense resistor is fed back to this input through the low pass filter R_CC_C . The lower transistor are disabled when the sense voltage exceeds the reference voltage of the selected comparator. When this occurs the current decays for a time set by R_TC_T , T_{OFF} = 0.69 R_TC_T .
REFERENCE (V_R)	A voltage applied to this pin sets the reference voltage of the three comparators, this determining the output current (also thus depending on R_S and the two inputs INPUT 0 and INPUT 1).
OUTPUT A (A_{OUT})	See OUTPUT B pin.
SENSE RESISTOR (EMITTERS)	Connection to lower emitters of output stage for insertion of a current sense resistor.

5

TEST CIRCUIT & TYPICAL WAVEFORMS

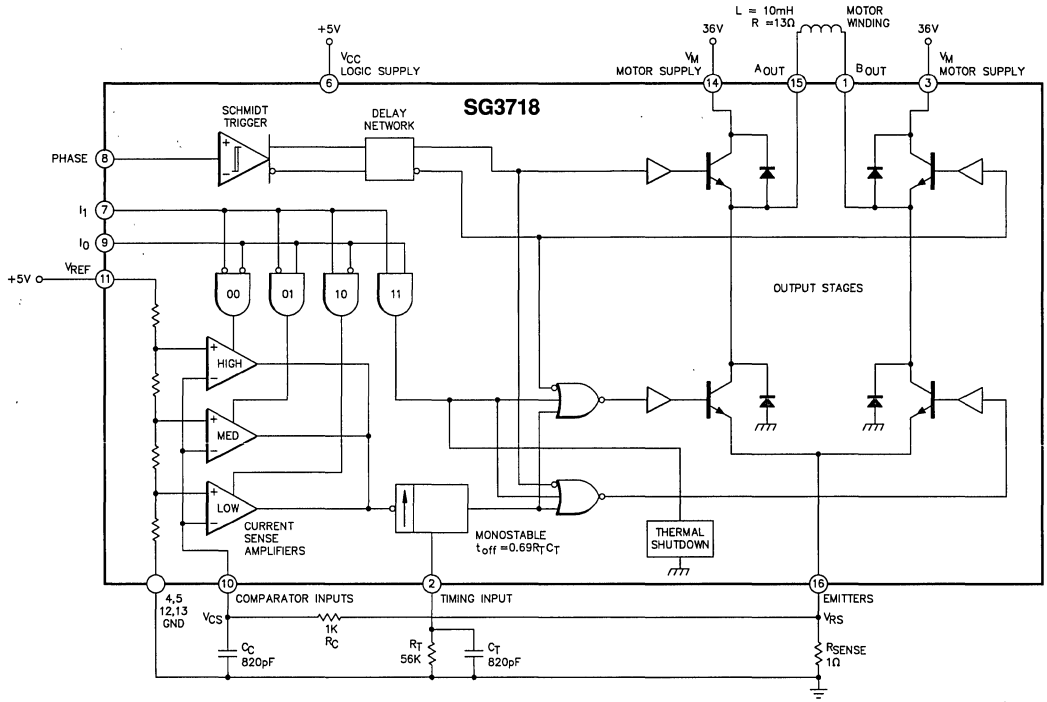


FIGURE 1 - SG3718 TEST CIRCUIT (Pin numbers are for plastic batwing W-pkg only)

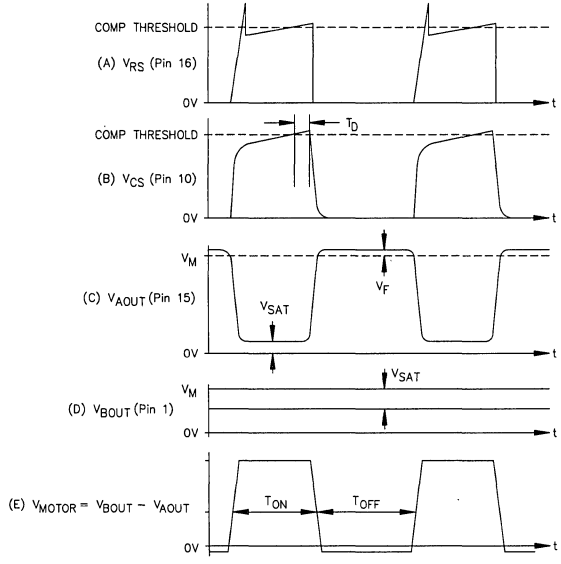
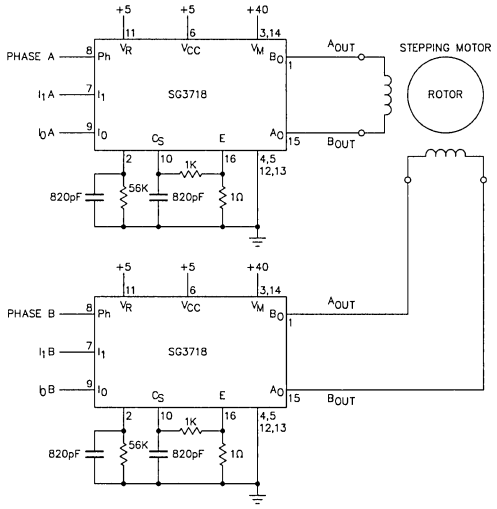


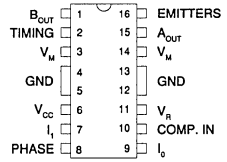
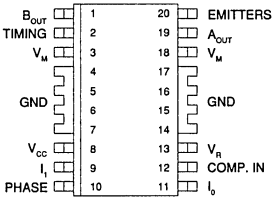
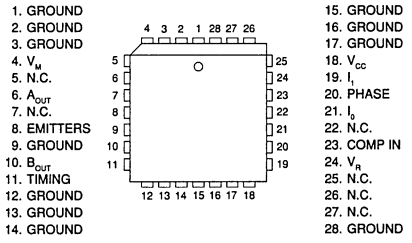
FIGURE 2 - TYPICAL WAVEFORMS WHEN PHASE INPUT IS LOW
(Pin numbers are for plastic batwing W-pkg only)

TYPICAL APPLICATION



(Pin numbers are for plastic batwing W-pkg only)

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN PLASTIC BATWING W - PACKAGE	SG3718W	0°C to 70°C	
20-PIN PLASTIC BATWING S.O.I.C DWW - PACKAGE	SG3718DWW	0°C to 70°C	
28-PIN PLASTIC LEADED CHIP CARRIER (PLCC) Q - PACKAGE	SG3718Q 0°C to 70°C		

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

SILICON GENERAL

THUMB INDEX

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SELECTION GUIDE
POWER DRIVERS & INTERFACE CIRCUITS

POWER DRIVERS

Device Type	Description	Typ. Application	$I_{O(PK)}$	$I_{O(CONT)}$	$V_{C(MAX)}$	$V_{CC(MAX)}$	Key Features	Pkgs.
SG1635/2635/3635 SG1635A/2635A/3635A	Half-bridge driver	• DC motor drivers • Stepper motor drive	5A	2A	35V 40V	35V 40V	SEE MOTION CONTROL CIRCUITS	
SG2000 Series	Darlington arrays	• Logic to power interface • Lamp driver • Motor driver	0.6A	0.5A	50V 95V*		• Seven open collector Darlington arrays • Internal clamp diodes • High speed switching • Closely matched parameters	J, N, DW, L
SG2800 Series	Darlington arrays	• Logic to power interface • Lamp driver • Motor driver		0.5A	50V 95V*		• Eight open collector Darlington arrays • Internal clamp diodes • High speed switching • Closely matched parameters	J, L
SG2064 thru SG2077	Quad power Darlington arrays	• Relays • Solenoids • DC and stepping motors • Display drivers	1.75A	1.5A	50V 80V**		• Four open collector Darlington arrays • Internal clamp diodes • 1.5V max. saturation at 1.5A • Low internal parasitics	J, W
SG3645	Quad power driver	• Stepper motor drive • DC motor drive • Lamp driver • Relay driver	3.5A	2.5A	60V	40V	SEE MOTION CONTROL CIRCUITS	
SG3663	Dual solenoid motor driver	• DC motor drivers • Stepper motor drive • Solenoid motor drive	3.5A	3.0A	50V	50V	SEE MOTION CONTROL CIRCUITS	
SG3700	Dual hammer driver	• DC motor drivers • Hammer coil drive in high speed printers	1.5A	0.9A	5.25V	40V	SEE MOTION CONTROL CIRCUITS	

* - SG2021 thru SG2025 only
SG2821 thru SG2824 only
** - For SG2065, 2067, 2069, 2071, 2075, 2077 only.

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LINEAR INTEGRATED CIRCUITS

SELECTION GUIDE
POWER DRIVERS & INTERFACE CIRCUITS

INTERFACE CIRCUITS

Device Type	Description	Typ. Application	$I_{O(PK)}$	$I_{O(CONT)}$	V_C	V_{CC}	Key Features	Pkgs.
SG1488	Quad line-driver	• Data communication interface	10mA	10mA	±12V		• Conformance with specifications of EIA standard No. RS-232C • Current limited outputs • Power-off source impedance 300Ω minimum • Slew rate control with external capacitor • Inputs compatile with DTL and TTL logic	J
SG1489/SG1489A	Quad line receiver	• Data communicaton interface	20mA	10mA	10V		• Conformance with specifications of EIA standard No. RS-232C • Input resistance -3KΩ TO 7KΩ • Input threshold hysteresis built in • Logic threshold shifting • Input noise filtering	J
SG1626/2626/3626 SG1644/2644/3644	Dual high speed driver Inv. (1626 series) N.I. (1644 series)	• Driving power MOSFETs • Driving high capacitive loads • Low voltage motor drive	3A	0.2A	22V	22V	• Dual totem pole outputs • High speed Schottky logic • Frequencies beyong 1MHz • TTL input compatibility • Rise and fall times less than 25ns • Propagation delays less than 20ns • Efficient operation at high frequency	Y,M,J,W, T, R
SG1627/2627/3627	Dual high current output driver	• Driving bipolar or MOSFETs • Low current DC motor drive	1A	0.5A	30V	30V	• Dual uncommited totem-pole outputs • Constant current drive capability • Inverting and N.I. inputs • 2V threshold for high noise immunity • Full cmpatibility with 1524 outputs	J, N
SG1629/2629/3629	Floating switch driver	• Driving high speed bipolar power transistors	2A	0.5A	20V	20V	• Single uncommited outputs • Self generating positive and negative currents • Floating operation • Baker clamp input for non-saturated switching • Provisions for source and sink gating	T, R
SG5792	Quad pin diode driver	• Phase shifters • Attenuators	0.5A	0.3A	50V	6V	• Four independent pin drivers • Shorted diode protection • TTL input compatible	J
SG5793	Quad pin diode driver	• Phase shifters • Attenuators	0.2A	0.1A	-55V	7V	• Four independent pin drivers • HCMOS compatible • Output monitor pin for each output	J

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LINEAR INTEGRATED CIRCUITS

SELECTION GUIDE
POWER DRIVERS & INTERFACE CIRCUITS

PERIPHERAL DRIVERS

Device Type	Description	Typ. Application	$I_{O(PK)}$	$I_{O(CONT)}$	V_C	V_{CC}	Key Features	Pkgs.
SG508	Quad high voltage NAND driver	• Lamp drivers • Relay driver	0.5A	0.25A	100V	7V	• Four NAND gates with open collector outputs • Pinning compatible with 54/74 logic series • Inputs compatible with DTL/TTL	H
SG55325 SG55326 SG55327	Memory driver	• Core memory drivers • Relay drivers • Lamp drivers	0.75A	0.6A	25V	7V & 25V	SEE CORE MEMORY CIRCUITS	
SG55450B/75450B	Dual peripheral positive AND driver	• High speed logic buffers • Relay drivers • Lamp drivers • Memory drivers • Line drivers	0.4A	0.3A	35V	7V	• Two NAND gates and two uncommited NPN transistors • High speed switching • TTL or DTL compatible diode-clamped inputs • Can be configured as an AND gate (common emitter configuration) or as a NAND gate (emitter follower configuration)	J, L
SG55460/75460					40V			
SG55470/75470					70V			
SG55451B/75451B	Dual peripheral positive AND driver	• High speed logic buffers • Relay drivers • Lamp drivers • Memory drivers • Line drivers	0.4A	0.3A	30V	7V	• Two AND gates with open collector outputs • High speed switching • TTL or DTL compatible diode-clamped inputs	Y, L
SG55461/75461					35V			
SG55471/75471					70V			
SG55452B/75452B	Dual peripheral positive NAND driver	• High speed logic buffers • Relay drivers • Lamp drivers • Memory drivers • Line drivers	0.4A	0.3A	30V	7V	• Two NAND gates with open collector outputs • High speed switching • TTL or DTL compatible diode-clamped inputs	Y, L
SG55462/75462					35V			
SG55472/75472					70V			
SG55453B/75453B	Dual peripheral positive OR driver	• High speed logic buffers • Relay drivers • Lamp drivers • Memory drivers • Line drivers	0.4A	0.3A	30V	7V	• Two OR gates with open collector outputs • High speed switching • TTL or DTL compatible diode-clamped inputs	Y, L
SG55463/75463					35V			
SG55473/75473					70V			
SG55454B/75454B	Dual peripheral positive NOR driver	• High speed logic buffers • Relay drivers • Lamp drivers • Memory drivers • Line drivers	0.4A	0.3A	30V	7V	• Two NOR gates with open collector outputs • High speed switching • TTL or DTL compatible diode-clamped inputs	Y, L
SG55464/75464					35V			
SG55474/75474					70V			

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SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

QUAD-NAND DRIVER

DESCRIPTION

The SG508 is a Quad 2-Input NAND Driver with outputs capable of sustaining 100V breakdown voltage. Each TTL-compatible NAND gate controls a 500mA output sink transistor. This combination of a TTL–compatible gate with high current output driver allows the designer to interface low-level logic circuits to power loads. It is also ideal for sense circuit applications.

The high breakdown voltage and current sink capabilities of these devices make them the perfect choice for driving incandescent lamps, relays and other peripheral devices.

The SG508 driver is a direct replacement for the Sprague UHD508 and is available in the side-brazed hermetic package (H-package). The SG508 Quad NAND driver is characterized for operation over the full military ambient temperature range of -55°C to 125°C and can be ordered in custom or other high-reliability screening flows.

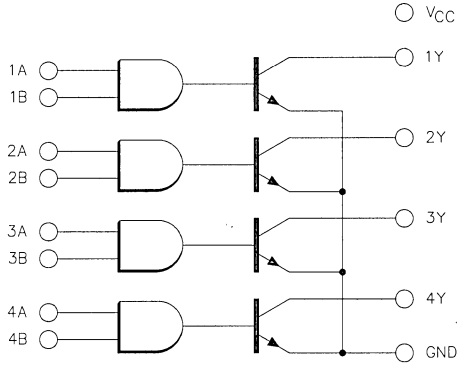
FEATURES

- **Quad drivers with TTL-compatible logic**
- **500mA output sink current**
- **100V output breakdown voltage**

HIGH RELIABILITY FEATURES - SG508

- **Available to MIL-STD-883 and DESC SMD**
- **SG level "S" processing available**

BLOCK DIAGRAM



FUNCTION TABLE (each driver)

A	B	Y
L	L	H (off-state)
L	H	H (off-state)
H	L	H (off-state)
H	H	L(on-state)

H = High Level, L = Low Level

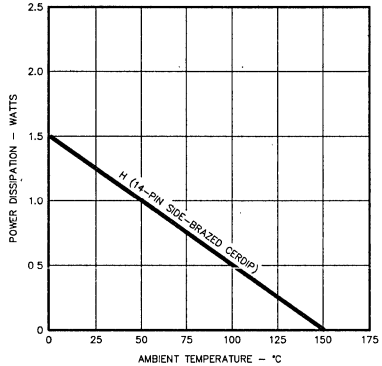
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V_{CC}) ..... 7.0V DC
Input Voltage ..... 5.5V DC
Output Off-State Voltage ..... 100V DC
Output On-State Current 500mA

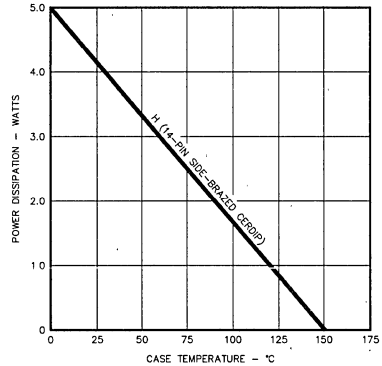
Operating Junction Temperature
Hermetic (H-package) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device. All currents are positive into the specified terminal.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage (V_{CC}) ..... 4.5V to 5.5V
Maximum Current Into Any Output (On-State) 250mA
Minimum High Level Input Voltage (V_{IH}) 2.0V

Maximum Low Level Input Voltage (V_{IL}) 0.8V
Operating Ambient Temperature Range (T_J)
SG508 ..... -55°C to 125°C

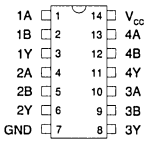
Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise stated, these specifications apply over the operating ambient temperatures for SG 508 with $-55°C \le T_A \le 125°C$. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG508			Units
		Min.	Typ.	Max.	
Input Current High ($I_{IN(1)}$)	Other input = 0V				
	Driven input = 2.4V			40	µA
	Driven input = 5.5V			1000	µA
Input Current Low ($I_{IN(0)}$)	Other input = 4.5V, Driven input = 0.4V, V_{CC} = 5.5V, V_{OUT} = 100V			-800	µA
Output Reverse Current (I_{OFF})	Other input = V_{CC}, Driven input = 0.8V, V_{CC} = 4.5V			100	µA
Output Voltage Low (V_{ON})	V_{CC} = 4.5V, All inputs = 2.0V				
	$-55°C \le T_A < 25°C$, Output = 150mA			0.5	V
	$-55°C \le T_A < 25°C$, Output = 250mA			0.7	V
	T_A = 125°C, Output = 150mA			0.6	V
	T_A = 125°C, Output = 250mA			0.8	V
Level Supply Current, High ($I_{CC(1)}$)	T_A = 25°C, V_{CC} = 5.5V, All Inputs = 0V			30	mA
Level Supply Current, Low ($I_{CC(0)}$)	T_A = 25°C, V_{CC} = 5.5V, All Inputs = 5.0V			106	mA
Propagation Delay Time	V_S = 100V, C_L = 15pF, V_{CC} = 5.0V, R_L = 670Ω				
Turn-on ($t_{PD\ ON}$)				500	ns
Turn-off ($t_{PD\ OFF}$)				750	ns

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN SIDE-BRAZED DIP H - PACKAGE	SG508H/883B SG508H	-55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

QUAD RS-232C LINE DRIVER

DESCRIPTION

The SG1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with specifications of EIA standard No. RS-232C.

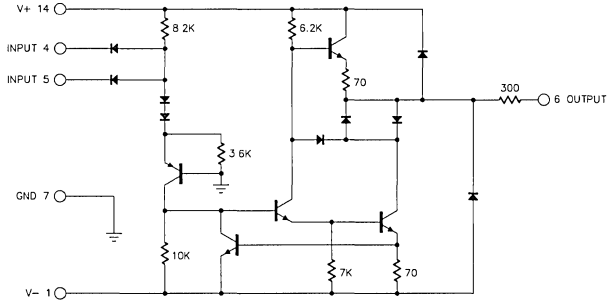
FEATURES

- **Current limited output 10mA typical**
- **Power-Off source impedance 300Ω minimum**
- **Simple slew rate control with external capacitor**
- **Flexible operating supply range**
- **Compatible with all DTL and TTL logic families**

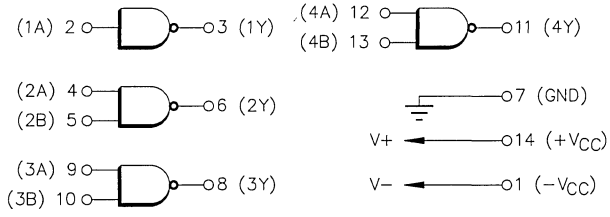
HIGH RELIABILITY FEATURES - SG1488

- **Available to MIL-STD-883**
- **SG level "S" processing available**

CIRCUIT SCHEMATIC (¼ Circuit Shown)



LOGIC DIAGRAM



POSITIVE LOGIC: $Y=\overline{AB}$

FUNCTION TABLE

INPUTS		OUTPUT
A	S	Y
H	H	L
L	X	H
X	L	H

H = high level, L = low level,
X = irrelevant

April 1990

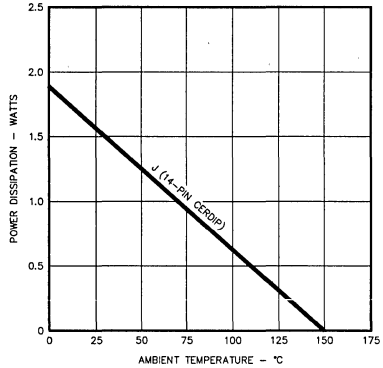
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±15V
Input Signal Voltage ..... -15V ≤ V_{IN} ≤ 7.0V
Output Signal Voltage ..... ±15V

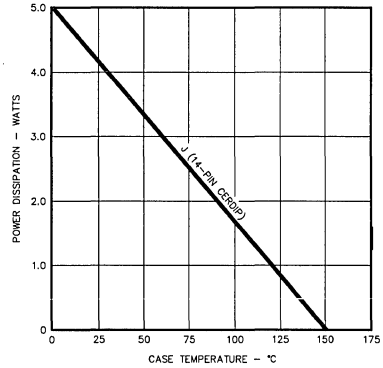
Operating Junction Temperature
Hermetic (J-Package) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage ..... ±12V
Input Signal Voltage ..... V- to 5V

Operating Ambient Temperature Range
SG1488 ..... 0°C to 75°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over full operating ambient temperatures for SG1488 with 0°C ≤ T_A ≤ 75°C, V+ = 9.0V ±1%, and V- = -9.0V ±1%. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

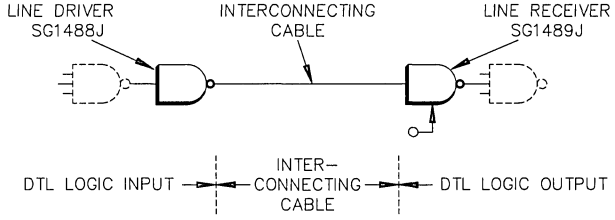
Parameter	Test Conditions	SG1488			Units
		Min.	Typ.	Max.	
Static Characteristics					
Forward Input Current	V_{IN} = 0V		1.0	1.6	mA
Reverse Input Current	V_{IN} = 5.0V			10	µA
Output Voltage High	V_{IN} = 0.8V, R_L = 3.0KΩ, V+ = 9.0V, V- = -9.0V	6.0	7.0		V
	V_{IN} = 0.8V, R_L = 3.0KΩ, V+ = 13.2V, V- = -13.2V	9.0	10.5		V
Output Voltage Low	V_{IN} = 1.9V, R_L = 3.0KΩ, V+ = 9.0V, V- = -9.0V	-6.0	-7.0		V
	V_{IN} = 1.9V, R_L = 3.0KΩ, V+ = 13.2V, V- = -13.2V	-9.0	-10.5		V
Positive Output Short-Circuit Current (Note 3)		6.0	10	12	mA
Negative Output Short–Circuit Current (Note 3)		-6.0	-10	-12	mA
Output Resistance (Note 4)	V+ = V- = 0V, $\|V_{OUT}\|$ = ±2.0V	300			Ω
Positive Supply Current	R_L = ∞				
	V_{IN} = 0.8V, V+ = 9.0V		4.5	6.0	mA
	V_{IN} = 1.9V, V+ = 9.0V		15	20	mA
	V_{IN} = 0.8V, V+ = 12V		5.5	7.0	mA
	V_{IN} = 1.9V, V+ = 12V		19	25	mA
	V_{IN} = 0.8V, V+ = 15V			12	mA
	V_{IN} = 1.9V, V+ = 15V			34	mA
Negative Supply Current	R_L = ∞				
	V_{IN} = 0.8V, V- = -9.0V			-15	mA
	V_{IN} = 1.9V, V- = -9.0V		-13	-17	mA
	V_{IN} = 0.8V, V- = -12V			-15	mA
	V_{IN} = 1.9V, V- = -12V		-18	-23	mA
	V_{IN} = 0.8V, V- = -15V			-2.5	mA
	V_{IN} = 1.9V, V- = -15V				mA

ELECTRICAL SPECIFICATIONS (continued)

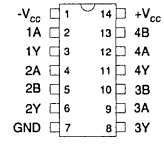
Parameter	Test Conditions	SG1488 Min.	SG1488 Typ.	SG1488 Max.	Units
Static Characteristics (continued)					
Power Dissipation	V+ = 9.0V, V- = -9.0V			333	mW
	V+ = 12V, V- = -12V			576	mW
Dynamic Characteristics (Note 4)					
Propagation Delay Time High-Low (TPHL)	Z_L = 3.0KΩ, C_L = 15pF, T_A = 25°C		150	200	ns
Fall Time (TTHL)	Z_L = 3.0KΩ, C_L = 15pF, T_A = 25°C		45	75	ns
Propagation Delay Time Low-High (TPLH)	Z_L = 3.0KΩ, C_L = 15pF, T_A = 25°C		110	175	ns
Rise Time (TTLH)	Z_L = 3.0KΩ, C_L = 15pF, T_A = 25°C		55	100	ns

Note 3. Maximum power dissipation may be exceeded if all outputs are shorted simultaneously.
Note 4. These parameters are not tested in production.

TYPICAL APPLICATION



CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN CERAMIC DIP J - PACKAGE	SG1488J/883B SG1488J	0°C to 75°C 0°C to 75°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

QUAD RS-232C LINE RECEIVERS

DESCRIPTION

The SG1489/SG1489A monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with specifications of EIA Standard No. RS-232C.

FEATURES

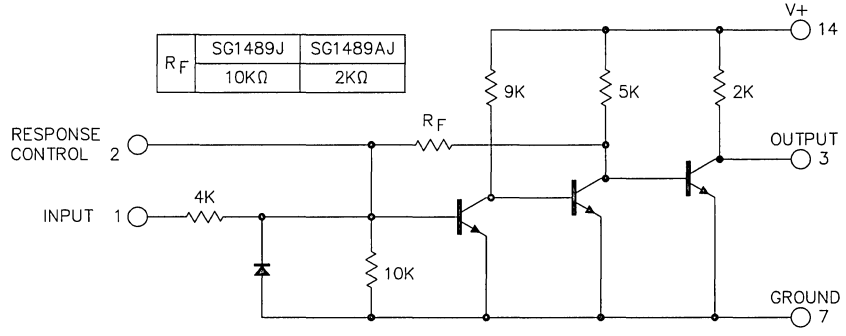
- **Input resistance 3.0KΩ to 7.0KΩ**
- **Input signal range ±30V**
- **Input threshold hysteresis built in**
- **Response control**
  - **Logic threshold shifting**
  - **Input noise filtering**

HIGH RELIABILITY FEATURES - SG1489/1489A

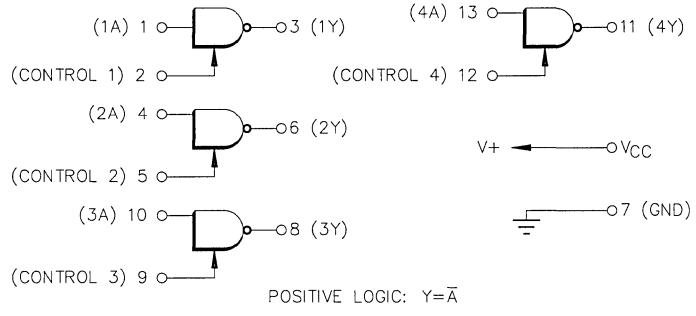
- ♦ **Available to MIL-STD-883**
- ♦ **SG level "S" processing available**

CIRCUIT SCHEMATIC (1/4 Circuit Shown)

R_F	SG1489J	SG1489AJ
	10KΩ	2KΩ



LOGIC DIAGRAM



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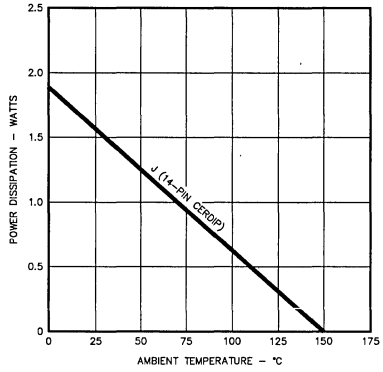
ABSOLUTE MAXIMUM RATINGS (Note 1)

Power Supply Voltage 10V
Input Signal Range ..... ±30V
Output Load Current 20mA

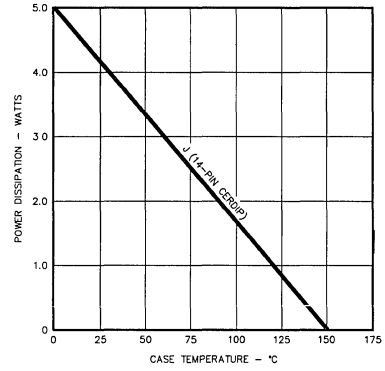
Operating Junction Temperature
Hermetic (J-Package) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage 9V
Input Signal Range ..... ±25V

Operating Ambient Temperature Range
SG1489/SG1489A ..... 0°C to 75°C

Note 2. Range over which the device is functional.

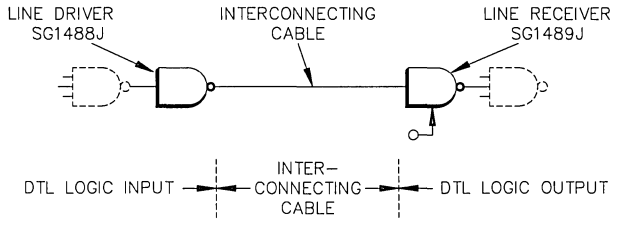
ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over full operating ambient temperatures for SG1489/SG1489A with $0°C \le T_A \le 75°C$, V+ = 5.0V ±1%. The RESPONSE CONTROL pin is open. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

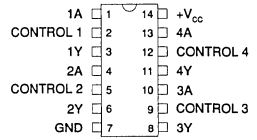
Parameter	Test Conditions	SG1489			SG1489A			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Static Characteristics								
Positive Input Current	V_{IN} = 25V	3.6		8.3	3.6		8.3	mA
	V_{IN} = 3.0V	0.43			0.43			mA
Negative Input Current	V_{IN} = -25V	-3.6		-8.3	-3.8		8.3	V
	V_{IN} = -3.0V	-0.43			-0.43			V
Input Turn-On Threshold Voltage	$V_{OL} \le 0.45V$, T_A = 25°C	1.0		1.5	1.75	1.95	2.25	V
Input Turn-Off Threshold Voltage	$V_{OH} \ge 2.5V$, I_L = –0.5mA, T_A = 25°C	0.75		1.25	0.75	0.8	1.25	V
Output Voltage High	V_{IN} = 0.75V, I_L = -0.5mA	2.6	4.0	5.0	2.6	4.0	5.0	V
	Input open circuit, I_L = -0.5mA	2.6	4.0	5.0	2.6	4.0	5.0	V
Output Voltage Low	V_{IN} = 3.0V, I_L = 10mA		0.2	0.45		0.2	0.45	V
Output Short-Circuit Current			3.0			3.0		mA
Power Supply Current	V_{IN} = 5.0V		20	26		20	26	mA
Power Dissipation	V_{IN} = 5.0V		100	130		100	130	mW
Dynamic Characteristics (Note 3)								
Propagation Delay Time High-Low (TPHL)	R_L = 3.9KΩ, T_A = 25°C		25	85		25	85	ns
Fall Time (TTHL)	R_L = 3.9KΩ, T_A = 25°C		120	175		120	175	ns
Propagation Delay Time Low-High (TPLH)	R_L = 390Ω, T_A = 25°C		25	50		25	50	ns
Rise Time (TTLH)	R_L = 390Ω, T_A = 25°C		10	20		10	20	ns

Note 3. These parameters, although guaranteed, are not tested in production.

TYPICAL APPLICATION



CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN CERAMIC DIP J - PACKAGE	SG1489AJ/883B SG1489AJ SG1489J/883B SG1489J	0°C to 75°C 0°C to 75°C 0°C to 75°C 0°C to 75°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

DUAL HIGH SPEED DRIVER

DESCRIPTION

The SG1626, 2626, 3626 is a dual inverting monolithic high speed driver that is pin for pin compatible with the DS0026, TSC426 and ICL7667. This device utilizes high voltage Schottky logic to convert TTL signals to high speed outputs up to 18V. The totem pole outputs have 3A peak current capability, which enables them to drive 1000pF loads in typically less than 25ns. These speeds make it ideal for driving power MOSFETs and other large capacitive loads requiring high speed switching.

In addition to the standard packages, Silicon General offers the 16 pin Batwing (W-package) and 16 pin S.O.I.C. (DW-package) for commercial and industrial applications and the Hermetic TO-66 (R-package) for military use. These packages offer improved thermal performance for applications requiring high frequencies and/or high peak currents.

FEATURES

- **Pin for pin compatible with DS0026, TSC426 and ICL7667.**
- **Totem pole outputs with 3.0A peak current capability.**
- **Supply voltage to 22V.**
- **Rise and fall times less than 25ns.**
- **Propagation delays less than 20ns.**
- **Inverting high-speed high-voltage Schottky logic.**
- **Efficient operation at high frequency.**
- **Available in:**
  - **8 Pin Plastic and Ceramic DIP**
  - **14 Pin Ceramic DIP**
  - **16 Pin Batwing DIP**
  - **16 Pin Plastic S.O.I.C.**
  - **TO-99**
  - **TO-66**

HIGH RELIABILITY FEATURES - SG1626

- ♦ **Available to MIL-STD-883**
- ♦ **Radiation data available**
- ♦ **SG level"S" processing available**

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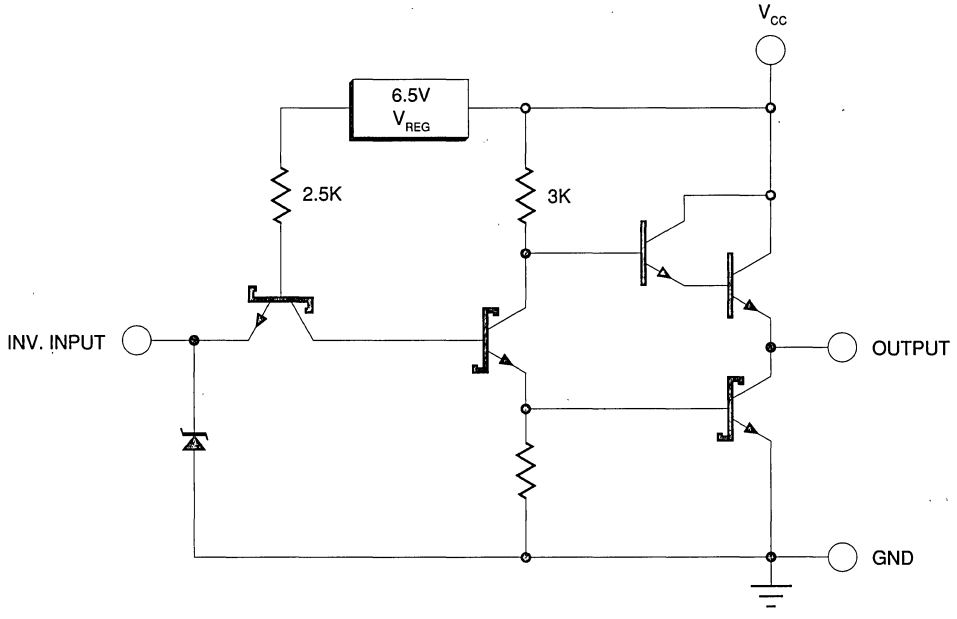
EQUIVALENT CIRCUIT SCHEMATIC



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See Application Notes for additional information.

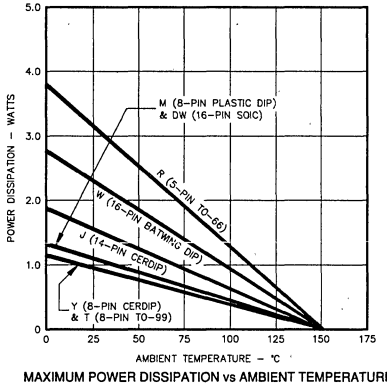
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V_{CC}) 22V
Logic Input Voltage 7V
Source/Sink Output Current (Each Output)
  Continuous ..... ±0.5A
  Pulse, 500ns ..... ±3.0A

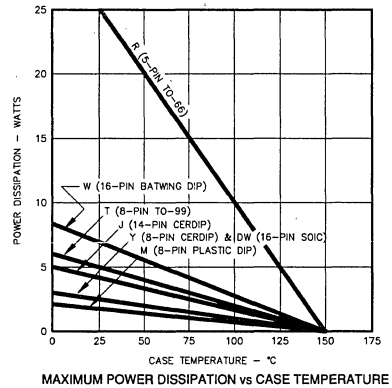
Operating Junction Temperature
  Hermetic (J, T, Y, R-Packages) ..... 150°C
  Plastic (M, DW, W-Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device. All voltages are with respect to ground. All currents are positive into the specified terminal.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage (V_{CC}) ..... 4.5V to 20V (Note 3)
Frequency Range ..... DC to 1.5MHz
Peak Pulse Current ..... ±3A
Logic Input Voltage ..... -0.5 to 5.5V

Operating Ambient Temperature Range (T_J)
  SG1626 ..... -55°C to 125°C
  SG2626 ..... -25°C to 85°C
  SG3626 ..... 0°C to 70°C

Note 2. Range over which the device is functional.
Note 3. AC performance has been optimized for V_{CC} = 8V to 20V.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1626 with -55°C ≤ T_A ≤ 125°C, SG2626 with -25°C ≤ T_A ≤ 85°C, SG3626 with 0°C ≤ T_A ≤ 70°C, and V_{CC} = 20V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1626/2626/3626			Units
		Min.	Typ.	Max.	
Static Characteristics					
Logic 1 Input Voltage		2.0			V
Logic 0 Input Voltage				0.7	V
Input High Current	V_{IN} = 2.4V			200	µA
Input High Current	V_{IN} = 5.5V			1.0	mA
Input Low Current	V_{IN} = 0V			-4	mA
Input Clamp Voltage	I_{IN} = -10mA			-1.5	V
Output High Voltage (Note 4)	I_{OUT} = -200mA	V_{CC}-3			V
Output Low Voltage (Note 4)	I_{OUT} = 200mA			1.0	V
Supply Current Outputs Low	V_{IN} = 2.4V (both inputs)		18	27	mA
Supply Current Outputs High	V_{IN} = 0V (both inputs)		7.5	12	mA

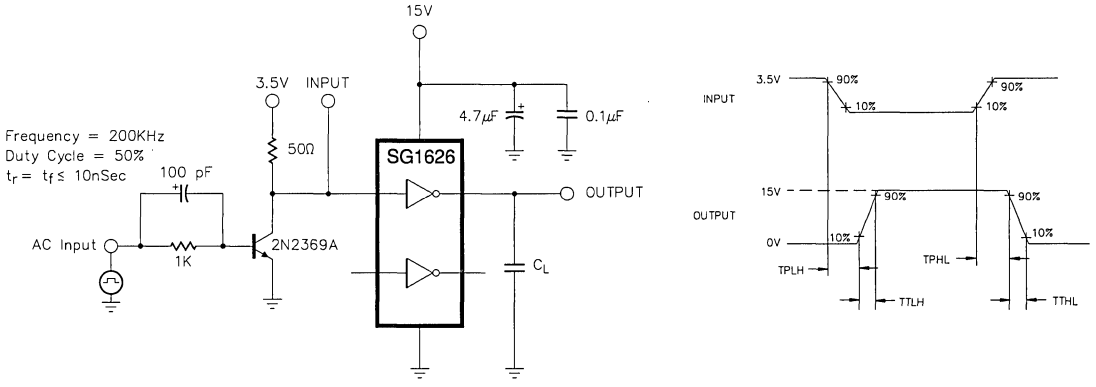
Note 4. V_{CC} = 10V to 20V.

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions (Figure 1)	SG1626/2626/3626 T_A= 25°C			SG1626 T_A=-55°C to 125°C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Dynamic Characteristics (Note 6)								
Propagation Delay High-Low	C_L = 1000pF (Note 5)			18			30	ns
(TPHL)	C_L = 2500pF		17	25			40	ns
Propagation Delay Low-High	C_L = 1000pF (Note 5)			25			40	ns
(TPLH)	C_L = 2500pF		25	35			50	ns
Rise Time (TTLH)	C_L = 1000pF (Note 5)			30			35	ns
	C_L = 2500pF		30	40			50	ns
Fall Time (TTHL)	C_L = 1000pF (Note 5)			20			30	ns
	C_L = 2500pF		30	40			50	ns
Supply Current (I_{CC})	C_L = 2500pF, Freq. = 200KHz							
(both outputs)	Duty Cycle = 50%		30	35			40	mA

Note 5. These parameters, specified at 1000pF, although guaranteed over recommended operating conditions, are not 100% tested in production.
Note 6. V_{CC} = 15V.

AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS - FIGURE 1



CHARACTERISTIC CURVES

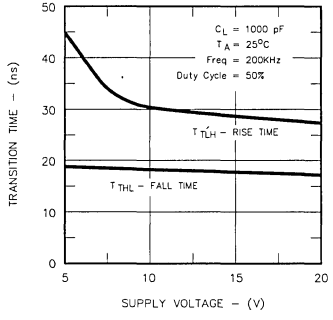


FIGURE 2.
TRANSITION TIMES VS. SUPPLY VOLTAGE

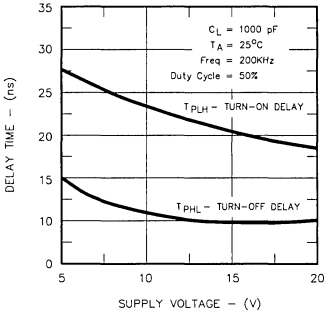


FIGURE 3.
PROPAGATION DELAY VS. SUPPLY VOLTAGE

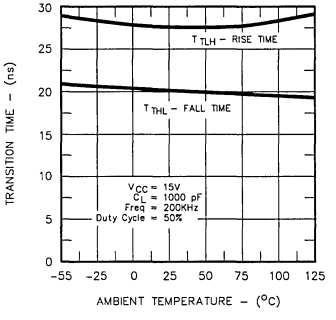


FIGURE 4.
TRANSITION TIMES VS. AMBIENT TEMPERATURE

6

CHARACTERISTIC CURVES (continued)

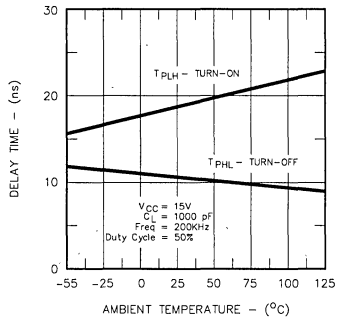


FIGURE 5.
PROPAGATION DELAY VS. AMBIENT TEMPERATURE

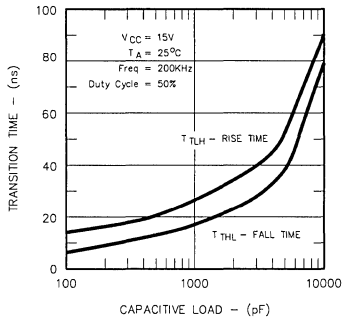


FIGURE 6.
TRANSITION TIMES VS. CAPACITIVE LOAD

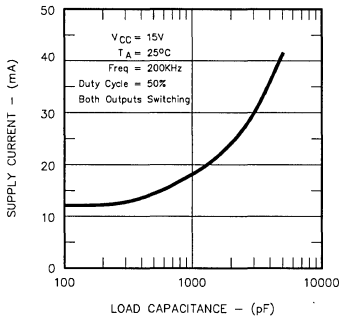


FIGURE 7.
SUPPLY CURRENT VS. CAPACITANCE LOAD

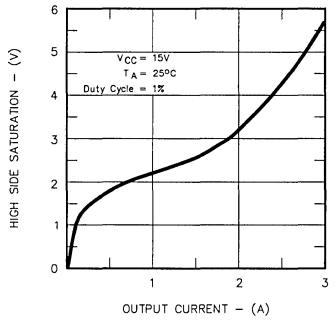


FIGURE 8.
HIGH SIDE SATURATION VS. OUTPUT CURRENT

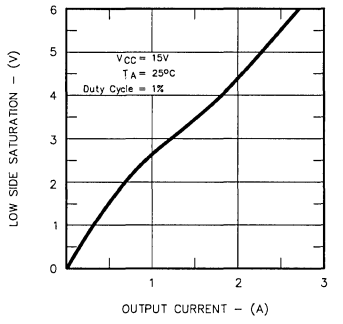


FIGURE 9.
LOW SIDE SATURATION VS. OUTPUT CURRENT

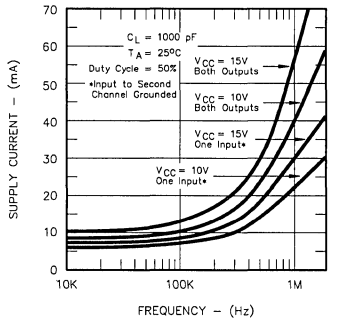


FIGURE 10.
SUPPLY CURRENT VS. FREQUENCY

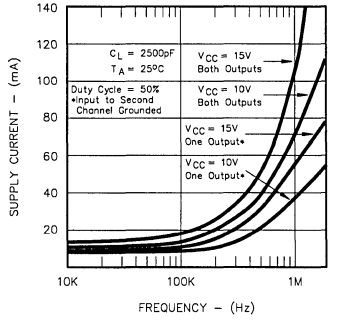


FIGURE 11.
SUPPLY CURRENT VS. FREQUENCY

APPLICATION INFORMATION

POWER DISSIPATION

The SG1626, while more energy-efficient than earlier gold-doped driver IC's, can still dissipate considerable power because of its high peak current capability at high frequencies. Total power dissipation in any specific application will be the sum of the DC or steady-state power dissipation, and the AC dissipation caused by driving capacitive loads.

The DC power dissipation is given by:

$P_{DC} = +V_{CC} \cdot I_{CC}$ [1]

where I_{CC} is a function of the driver state, and hence is duty-cycle dependent.

The AC power dissipation is proportional to the switching frequency, the load capacitance, and the square of the output voltage. In most applications, the driver is constantly changing state, and the AC contribution becomes dominant when the frequency exceeds 100-200KHz.

The SG1626 driver family is available in a variety of packages to accommodate a wide range of operating temperatures and power dissipation requirements. The Absolute Maximums section of the data sheet includes two graphs to aid the designer in choosing an appropriate package for his design.

The designer should first determine the actual power dissipation of the driver by referring to the curves in the data sheet relating operating current to supply voltage, switching frequency, and capacitive load. These curves were generated from data taken on actual devices. The designer can then refer to the Absolute Maximum Thermal Dissipation curves to choose a package type, and to determine if heat-sinking is required.

DESIGN EXAMPLE

Given: Two 2500 pF loads must be driven push-pull from a +15 volt supply at 100KHz. This is a commercial application where the maximum ambient temperature is +50°C, and cost is important.

1. From Figure 11, the average driver current consumption under these conditions will be 18mA, and the power dissipation will be 15volts x 18mA, or 270mW.

2. From the Ambient Thermal Characteristic curve, it can be seen that the M package, which is an 8-pin plastic DIP with a copper lead frame, has more than enough thermal conductance from junction to ambient to support operation at an ambient temperature of +50°C. The SG3626M driver would be specified for this application.

SUPPLY BYPASSING

Since the SG1626 can deliver peak currents above 3amps under some load conditions, adequate supply bypassing is essential for proper operation. Two capacitors in parallel are recommended to guarantee low supply impedance over a wide bandwidth: a 0.1µF ceramic disk capacitor for high frequencies, and a 4.7µF solid tantalum capacitor for energy storage. In military applications, a CK05 or CK06 ceramic operator with a CSR-13 tantalum capacitor is an effective combination. For commercial applications, any low-inductance ceramic disk capacitor teamed with a Sprague 150D or equivalent low ESR capacitor will work well. The capacitors must be located as close as physically possible to the V_{CC} pin, with combined lead and pc board trace lengths held to less than 0.5 inches.

GROUNDING CONSIDERATIONS

Since ground is both the reference potential for the driver logic and the return path for the high peak output currents of the driver, use of a low-inductance ground system is essential. A ground plane is highly recommended for best performance. In dense, high performance applications a 4-layer pc board works best; the 2 inner planes are dedicated to power and ground distribution, and signal traces are carried by the outside layers. For cost-sensitive designs a 2-layer board can be made to work, with one layer dedicated completely to ground, and the other to power and signal distribution. A great deal of attention to component layout and interconnect routing is required for this approach.

LOGIC INTERFACE

The logic input of the 1626 is designed to accept standard DC-coupled 5 volt logic swings, with no speed-up capacitors required. If the input signal voltage exceeds 6 volts, the input pin must be protected against the excessive voltage in the HIGH state. Either a high speed blocking diode must be used, or a resistive divider to attenuate the logic swing is necessary.

LAYOUT FOR HIGH SPEED

The SG1626 can generate relatively large voltage excursions with rise and fall times around 20-30 nanoseconds with light capacitive loads. A Fourier analysis of these time domain signals will indicate strong energy components at frequencies much higher than the basic switching frequency. These high frequencies can induce ringing on an otherwise ideal pulse if sufficient inductance occurs in the signal path (either the positive signal trace or the ground return). Overshoot on the rising edge is undesirable because the excess drive voltage could rupture the gate oxide of a power MOSFET. Trailing edge undershoot is dangerous because the negative voltage excursion can forward-bias the parasitic PN substrate diode of the driver, potentially causing erratic operation or outright failure.

Ringing can be reduced or eliminated by minimizing signal path inductance, and by using a damping resistor between the drive output and the capacitive load. Inductance can be reduced by keeping trace lengths short, trace widths wide, and by using 2oz. copper if possible. The resistor value for critical damping can be calculated from:

$R_D = 2\sqrt{L/C_L}$ [2]

where L is the total signal line inductance, and C_L is the load capacitance. Values between 10 and 100ohms are usually sufficient. Inexpensive carbon composition resistors are best because they have excellent high frequency characteristics. They should be located as close as possible to the gate terminal of the power MOSFET.

TYPICAL APPLICATIONS

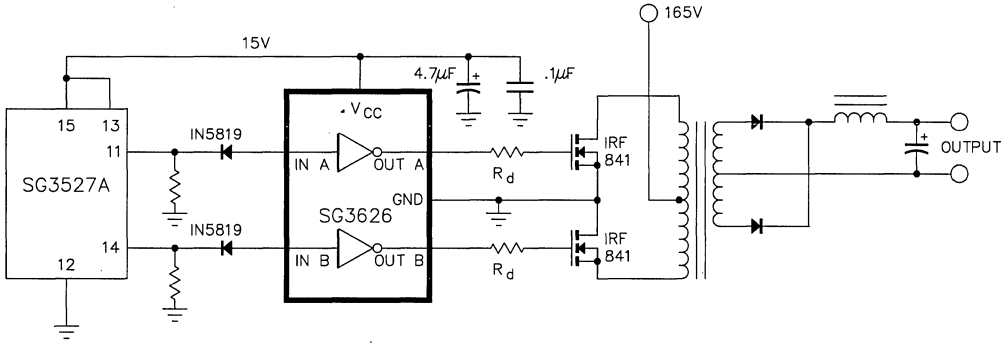


FIGURE 12.
When the SG3626 is driven from a totem-pole source with a peak output greater than 6 volts, a low-current, fast-switching blocking diode is required at each logic input for protection. In this push-pull converter, the inverted logic outputs of the 3527A are ideal control sources for the power driver.

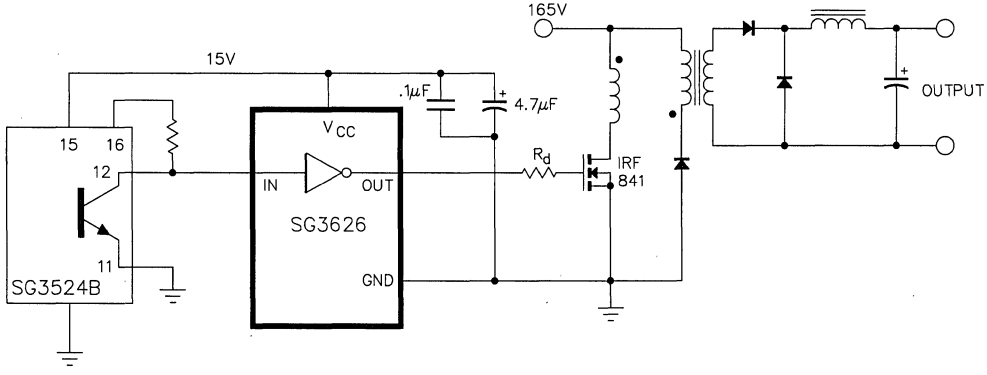


FIGURE 13.
In this forward converter circuit, the control capabilities of the SG3524B PWM are combined with the powerful totem-pole drivers found in the SG3626. This inexpensive configuration results in very fast charge and discharge of the power MOSFET gate capacitance for efficient swithing.

TYPICAL APPLICATIONS (continued)

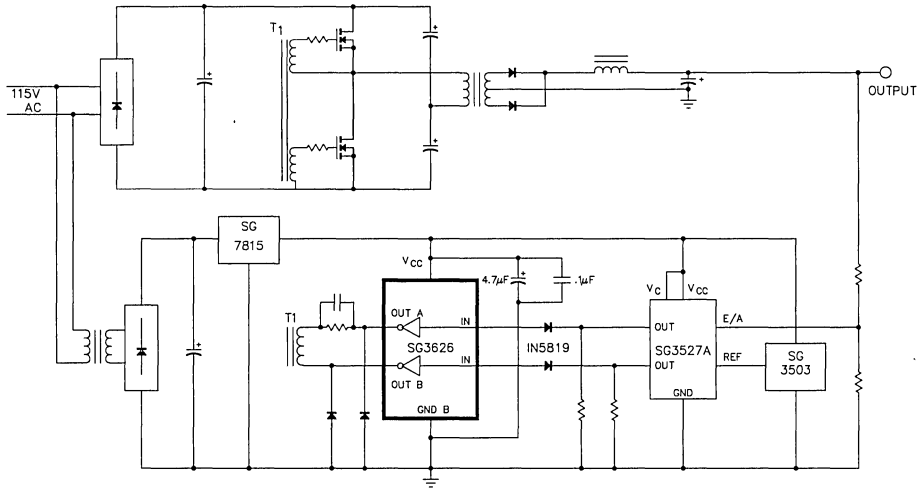


FIGURE 14.
In half or full-bridge power supplies, driving the isolation transformers directly from the PWM can cause excessive IC temperatures, expecially above 100KHz. This circuit uses the high drive capacity of the SG3626 to solve the problem.

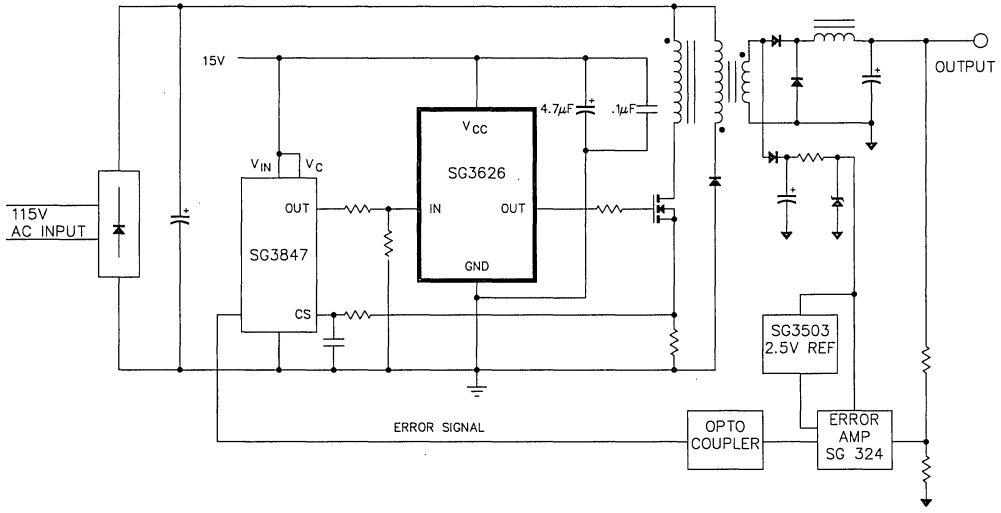
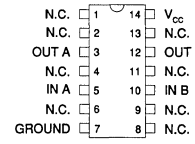
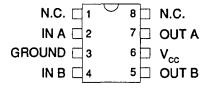
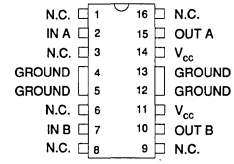
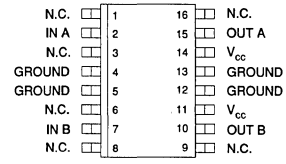
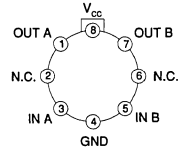
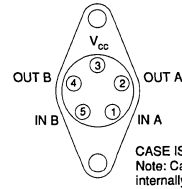


FIGURE 15.
A low-impedance resistive divider network can also be used as the interface between the PWM high-voltage logic output and the SG3626 power driver. In this 200KHz current mode converter, the SG3847 provides control, while the SG3626 provides high power drive and minimizes ground spiking in the control IC.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN CERAMIC DIP J - PACKAGE	SG1626J/883B SG1626J SG2626J SG3626J	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
8-PIN CERAMIC DIP Y - PACKAGE 8-PIN PLASTIC DIP M - PACKAGE	SG1626Y/883B SG1626Y SG2626Y SG3626Y SG2626M SG3626M	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C -25°C to 85°C 0°C to 70°C	
16-PIN BATWING DIP W - PACKAGE	SG2626W SG3626W	-25°C to 85°C 0°C to 70°C	
16-PIN WIDE BODY PLASTIC S.O.I.C. DW - PACKAGE	SG2626DW SG3626DW	-25°C to 85°C 0°C to 70°C	
8-PIN TO-99 METAL CAN T - PACKAGE	SG1626T/883B SG1626T SG2626T SG3626T	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
5-PIN TO-66 METAL CAN R - PACKAGE	SG1626R/883B SG1626R SG2626R SG3626R	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

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SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

DUAL HIGH-CURRENT OUTPUT DRIVER

DESCRIPTION

The SG1627 series devices are monolithic, high-speed driver integrated circuits designed to interface digital control logic with high current loads. Each device contains two independent drivers which will either source or sink up to 500mA of current. The sink transistor is designed as a saturating switch while the source transistor can be used either as a switch or as a constant current generator with external resistor programming.

Each half of this device contains both inverting and non-inverting inputs which have two volt thresholds for high noise immunity. Either input can be used alone to switch the output, or one input can be strobed with the other. These units have been designed to directly interface with the SG1524 Regulating Pulse Width Modulator Circuit.

These devices are supplied in ceramic 16-pin D.I.L. packages. The SG1627 is specified for operation over a -55°C to +125°C ambient temperature range while the SG2627 is intended for industrial applications of -25°C to 85°C and the SG3627 for 0°C to 70°C.

FEATURES

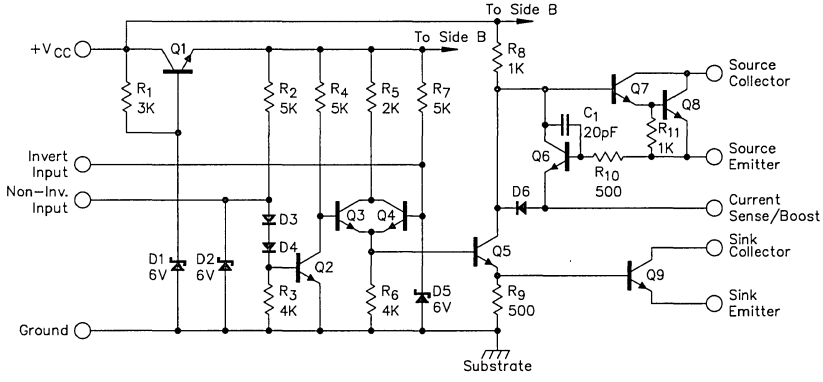
- **Two independent driver circuits**
- **Outputs will source or sink currents to 500mA**
- **300ns response time**
- **Full compatibility with SG1524 PWM circuit**
- **Constant current drive capability**
- **Two volt threshold for high noise immunity**
- **Source and sink can be separated for complementary outputs**

HIGH RELIABILITY FEATURES - SG1627

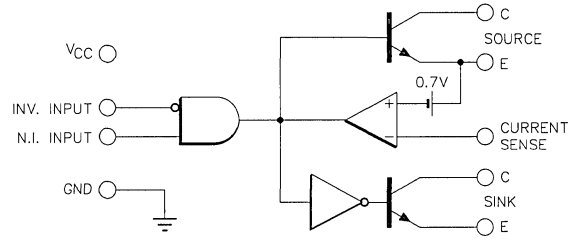
- **Available to MIL-STD-883**
- **SG level "S" processing available**

6

SCHEMATIC (one-half of total device shown)



BLOCK DIAGRAM (one-half of total device shown)



FUNCTION TABLE

NON INV.	INV.	SINK	SOURCE
LO	OPEN	ON	OFF
OPEN	LO	OFF	ON
OPEN	OPEN	ON	OFF
LO	LO	ON	OFF

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, V_{CC}
- SG1627, 2627 ..... 30V
- SG3627 ..... 20V

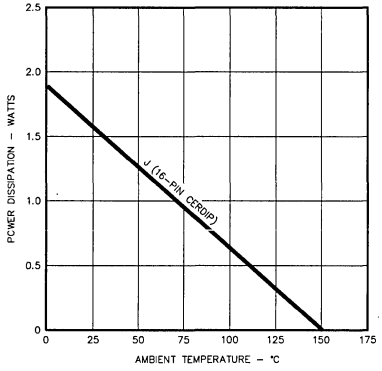
Output Collector Voltage
- SG1627, 2627 ..... 30V
- SG3627 ..... 20V

Source or Sink Current, DC 500mA
Peak Current (< 2% duty cycle) 1A
Input Voltage Range ..... -0.3V to 5.5V
Input Current 10mA
Operating Junction Temperature
- Hermetic (J Package) ..... 150°C

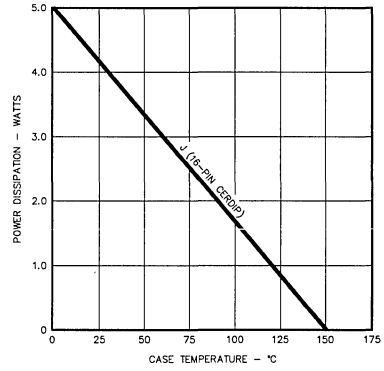
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage, V_{CC}
- SG1627, 2627 ..... 5V to 30V
- SG3627 ..... 5V to 20V

Output Collector Voltage
- SG1627, 2627 ..... 5V to 30V
- SG3627 ..... 5V to 20V

Source or Sink Current, DC ..... 0mA to 500mA
Peak Current (<2% duty cycle) ..... 0mA to 750mA
Input Voltage ..... 0V to 5.5V
Input Current ..... 0mA to 10mA
Operating Ambient Temperature Range
- SG1627 ..... -55°C to 125°C
- SG2627 ..... -25°C to 85°C
- SG3627 ..... 0°C to 70°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1627 with -55°C ≤ T_A ≤ 125°C, SG2627 with -25°C ≤ T_A ≤ 85°C, SG3627 with 0°C ≤ T_A ≤ 70°C, and V_{CC} = 5V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1627/2627/3627			Units
		Min.	Typ.	Max.	
High-Level Input Voltage		2.8		5.5	V
Low-Level Input Voltage		0		1.4	V
Input Threshold			2.0		V
Low-Level Input Current	V_{IN} = 0V		-1.0	-2.0	mA
Source Off, Leakage Current	Collector V = V_{MAX}		0.3	1.0	mA
Source On, Collector Saturation	I_{SOURCE} = 50mA		1.1	1.7	V
(Source Emitter Grounded, R_{SC} = 0)	I_{SOURCE} = 300mA		1.2	1.9	V
	I_{SOURCE} = 500mA		1.3		V
Source On, Emitter Voltage	I_{SOURCE} = -50mA	V_{CC}-3V			V
Sink Off, Leakage Current	Collector V = V_{MAX}		1.0	100	µA
Sink On, Collector Saturation	I_{SINK} = 50mA		0.2	0.4	V
	I_{SINK} = 300mA, V_{CC} = 20V		0.5	0.7	V
	I_{SINK} = 500mA, I_{BOOST} = 25mA		0.5		V
Current Limit Sense Voltage	R_{SC} = 10Ω, T_A = 25°C	600	700	900	mV
Sense Voltage Temperature Coefficient	R_{SC} = 10Ω		1.8		mV/°C

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1627/2627/3627 Min.	Typ.	Max.	Units
Supply Current (both sink transistors on)	V_{CC} = 5V		15	22	mA
	V_{CC} = 20V		50	73	mA
	V_{CC} = 30V (1627/2627 only)		80	115	mA
Response Time (TRHL)	Fig. 12, R_L = 24Ω T_A = 25°C		100		ns
Response Time (TRLH)	Fig. 12, R_L = 24Ω T_A = 25°C		300		ns

CHARACTERISTIC CURVES

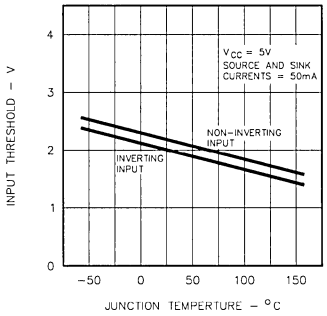


FIGURE 1.
INPUT THRESHOLD VS. TEMPERATURE

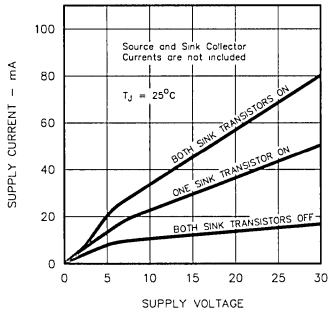


FIGURE 2.
V_{CC} SUPPLY CURRENT VS. VOLTAGE

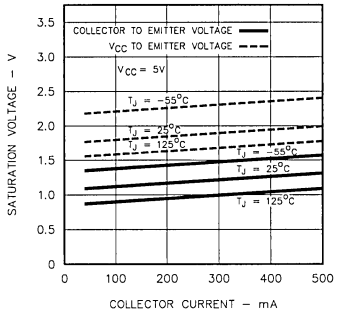


FIGURE 3.
SOURCE TRANSISTOR SATURATION

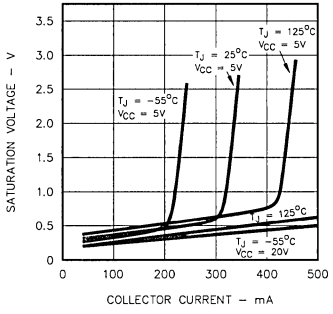


FIGURE 4.
SINK TRANSISTOR SATURATION

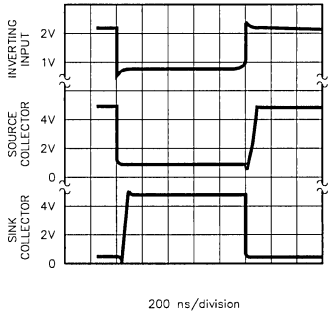


FIGURE 5.
DYNAMIC RESPONSE
(See Fig. 12 for Test Circuit, R_L = 24Ω)

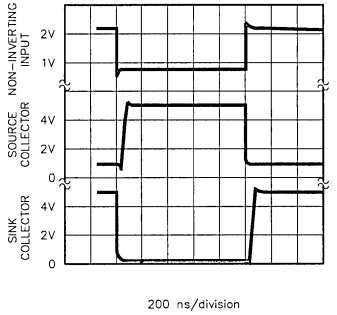


FIGURE 6.
DYNAMIC RESPONSE
(See Fig. 12 for Test Circuit, R_L = 24Ω)

APPLICATION INFORMATION

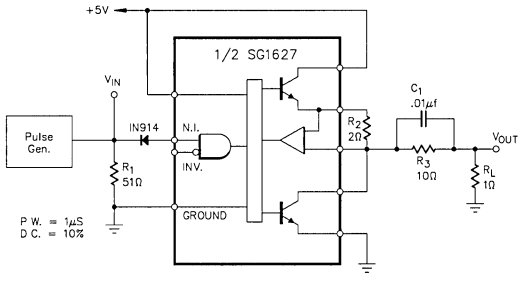


FIGURE 7 - TOTEM POLE OUTPUT SWITCH CIRCUIT

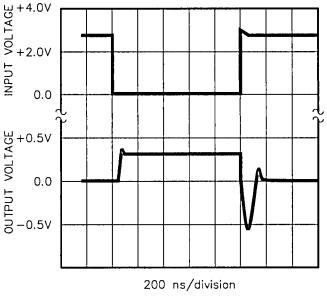


FIGURE 8 - OUTPUT WAVEFORM

APPLICATION CIRCUITS

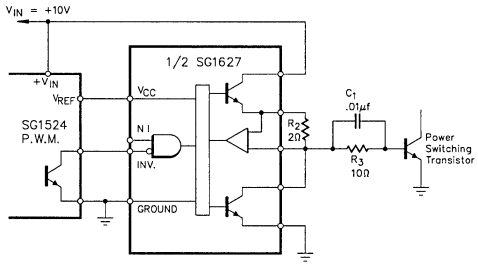


FIGURE 9

Basic 300mA switched drive circuit. If the external output transistor is to be on when the driving transistor is on, use the inverting input with the non-inverting input left open. For opposite phasing, use the non-inverting input with the inverting input grounded.

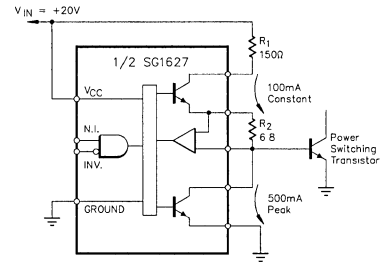


FIGURE 10

Use of higher input voltage provides greater drive for higher sink-transistor peak current while R2 provides constant source current. R1 helps minimize power in the SG1627. Although the sink emitter may be connected to a different ground point from pin 5, any voltage differences between them will directly affect the input threshold level.

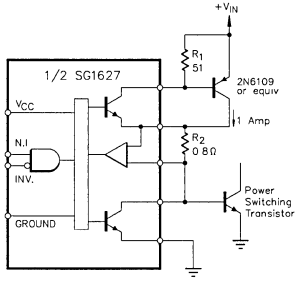


FIGURE 11

Additional source current or power handling capability may be added with the use of an external PNP transistor. For optimum performance, a low storage-time unit should be selected. If current limiting is not required, an NPN emitter follower could also be used for source boost.

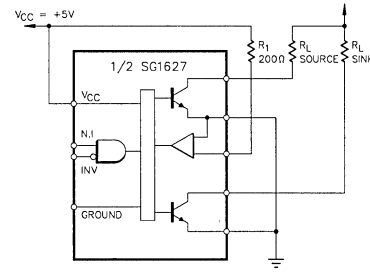


FIGURE 12

Source and sink transistors can be used separately for complementary outputs. At low supply voltages the sink current is limited to approximately 100mA, but if current limiting is not required a sink drive boost may be added with R1. The current in R1 should be .05 times the sink load current to insure saturation.

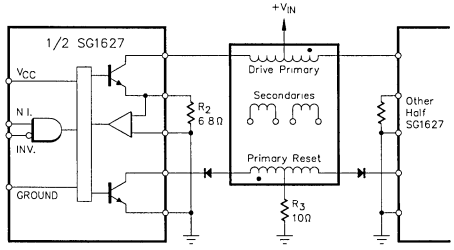


FIGURE 13

Source and sink transistors can be used separately for an efficient transformer driver. Here the source provides constant current drive with magnetic reset accomplished by a flux clamp utilizing the sink transistor. With the source current sense terminal connected to ground, there will be a residual collector current of approximately 300μA. If this is objectionable, insert a diode between current sense and ground.

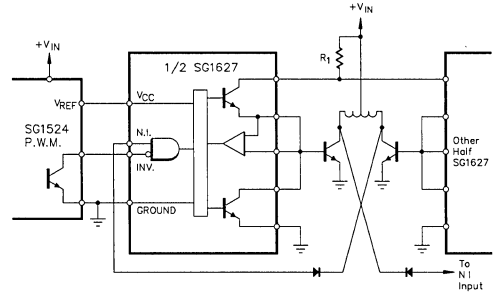
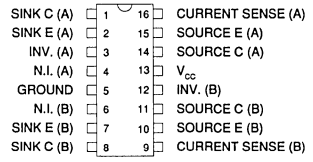


FIGURE 14

Simultaneous conduction of the output switching transistors can be positively prevented by using diodes to cross-couple a gating signal into the non-inverting inputs. For maximum power handling capability, the source transistor is driven into saturation with the current limiting provided by R1.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG1627J/883B SG1627J SG2627J SG3627J	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

HIGH-CURRENT FLOATING SWITCH DRIVER

DESCRIPTION

The SG1629 and SG3629 are monolithic integrated circuits designed to generate the positive and negative base drive currents (ib1 and ib2) required for high-speed, high power switching transistors. These units are intended to interface between the secondary of a drive transformer and the base of an NPN switching device. Positive drive current can be made constant with an external programming resistor, or can be clamped with a diode to keep the switching device out of saturation. Negative turn-off current is derived from a negative voltage generated in an external capacitor. All operating power is supplied by the transformer secondary and these devices can be floated at high levels with respect to ground for off-line, bridge converters.

For medium power applications, these units are available in 10-pin, TO-100 package; while high power capability is offered in a 9-pin, TO-66 case. In either package, the SG1629 is specified for operation over an ambient temperature range of -55°C to 125°C while the SG3629 is intended for industrial applications of 0 to 70°C.

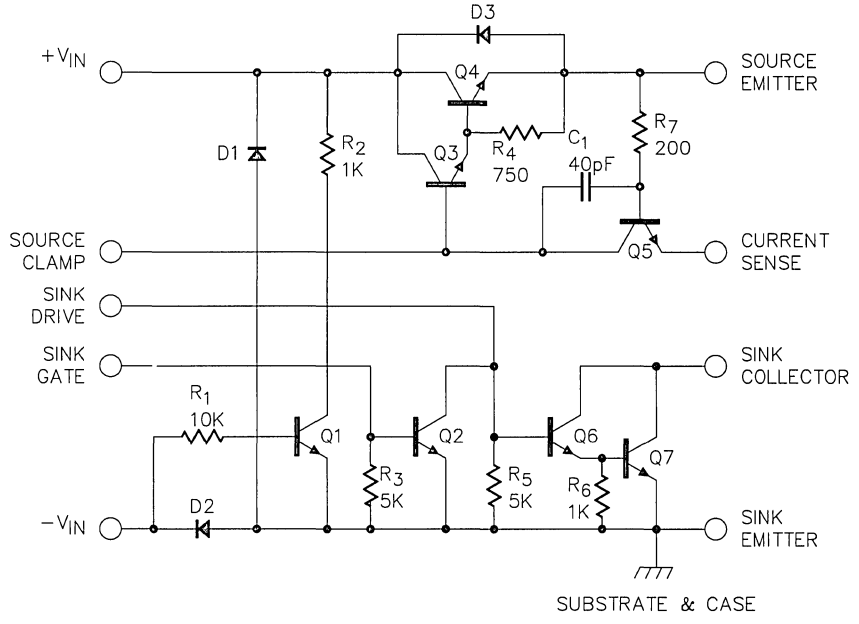
FEATURES

- **Self-generating positive and negative currents**
- **Constant source current (I_{B1}) to one amp**
- **Two amp peak sink current (I_{B2}) to negative voltage**
- **Floating operation**
- **Baker clamp input for non-saturated switching**
- **Provisions for source and sink gating**
- **100ns response**

HIGH RELIABILITY FEATURES - SG1629

- **Available to MIL-STD-883**
- **SG level "S" processing available**

SCHEMATIC



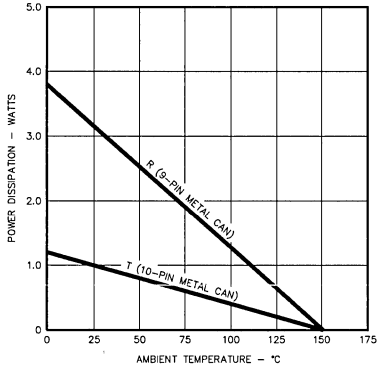
6

ABSOLUTE MAXIMUM RATINGS (Note 1)

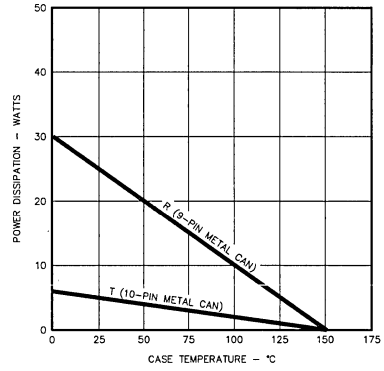
Input Voltage ($+V_{IN}$ or $-V_{IN}$) 20V
Collector to Emitter Voltage, Source or Sink 20V
Source Current 2.0A
Sink Current 3.0A
Sink Rectifier Current (peak) 2.0A
Operating Junction Temperature
Hermetic (T, R Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Voltage ($+V_{IN}$ or $-V_{IN}$) 15V
Collector to Emitter Voltage, Source or Sink 15V
Source Current ..... 0A to 1A
Sink Current ..... 0A to 2A
Sink Rectifier Current (Peak) ..... 0A to 1A
Operating Ambient Temperature Range
SG1629 ..... -55°C to 125°C
SG3629 ..... 0°C to 70°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1629 with $-55°C \le T_A \le 125°C$, SG3629 with $0°C \le T_A \le 70°C$. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1629/SG3629			Units
		Min.	Typ.	Max.	
Collector to Emitter Voltage, Source or Sink	V_{BE} = 0	20	30		V
Collector to Emitter Leakage, Source or Sink	V_{BE} = 0, V_{CE} = 15V		5	100	µA
Input Leakage V+ to V-	Input Voltage = +15V		1	100	µA
Input Leakage V- to V+	Input Voltage = -15V		2	4	mA
Standby Current from Sink Emitter Voltage (Note 3)	Sink Emitter = -5V, $+V_{IN} = -V_{IN}$ = 0V		5	10	mA
Clamp Current	$+V_{IN}$ = 15V, V clamp = 0V	10	15	20	mA
Source Saturation Voltage	I_{SOURCE} = 100mA		1.7		V
	I_{SOURCE} = 500mA		1.8		V
	I_{SOURCE} = 1A, T_A = 25°C		2.0	3	V
Sink Saturation Voltage, Force beta = 100	I_{SINK} = 100mA		1.2		V
	I_{SINK} = 500mA		1.3		V
	I_{SINK} = 1A, T_A = 25°C		1.5	2	V
Sink Current Gain	I_{SINK} = 2A, V_{CE} = 3V	300	500		
Current Limit Sense Voltage	R_{SC} = 0.7Ω, T_A = 25°C	0.55	0.65	0.80	V
Sink Rectifier Forward Voltage	I_F = 1A, T_A = 25°C		1.0	2.0	V
Sink Gate Output Saturation	Sink Drive = 10mA, Sink Gate I_{IN} = 1mA		0.2	0.4	V
Source Response	I_{SOURCE} = 1A		100		ns
Sink Response	I_{SINK} = 1A		100		ns

Note 3. 1KΩ from $-V_{IN}$ to Sink Drive and Source Emitter connected to Sink Collector.

CHARACTERISTIC CURVES

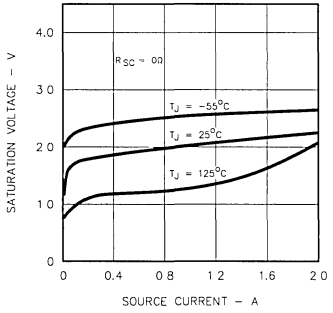


FIGURE 1.
SOURCE SATURATION

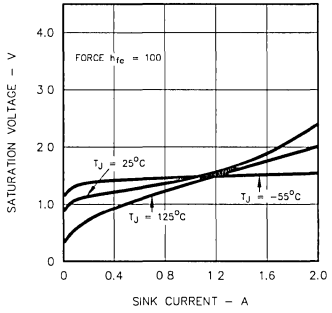


FIGURE 2.
SINK SATURATION

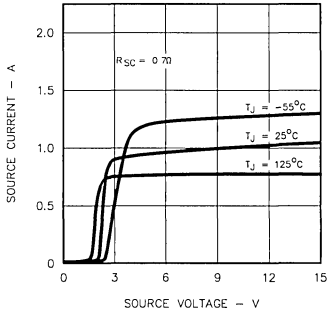


FIGURE 3.
CONSTANT SOURCE CURRENT

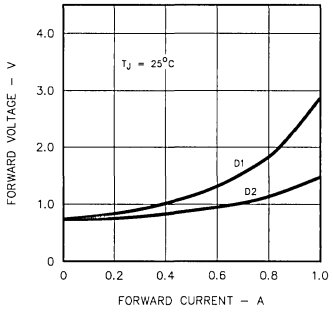


FIGURE 4.
RECTIFIER FORWARD VOLTAGE

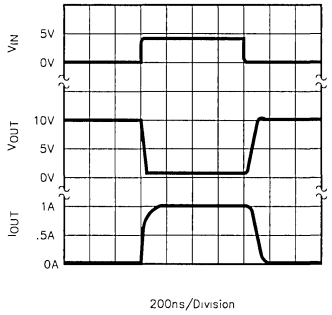


FIGURE 5.
DYNAMIC RESPONSE WAVEFORM

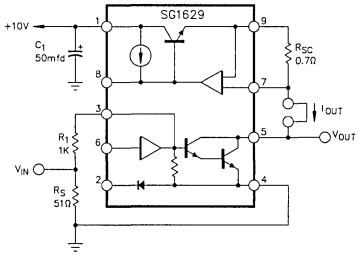


FIGURE 6.
DYNAMIC RESPONSE TEST CIRCUIT

APPLICATION CIRCUITS

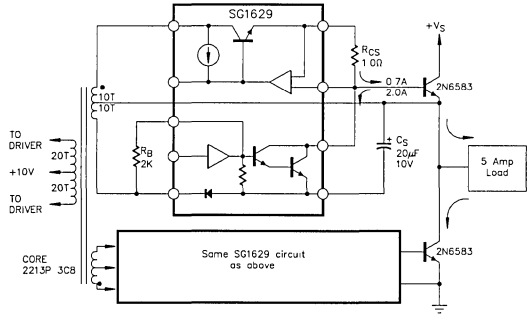


FIGURE 6

Two SG1629 devices can be combined to form the drive signals for the power transistors in a 5A, half-bridge switching supply.

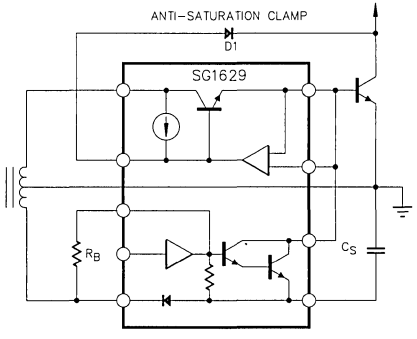


FIGURE 7

A load-dependent drive current may be provided by eliminating the current sensing resistor and adding the anti-saturation clamp diode D1.

6

APPLICATION CIRCUITS (continued)

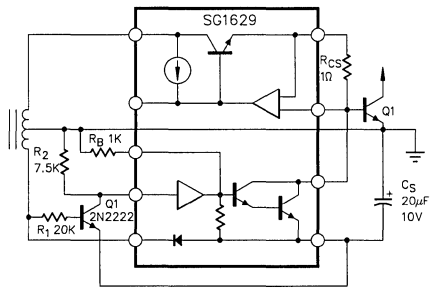


FIGURE 8

Where transformer inductance would normally degrade turn-on current rise time, the use of the sink gate with a relatively slow external transistor, Q1, will delay the sink turn-off until after source current has been

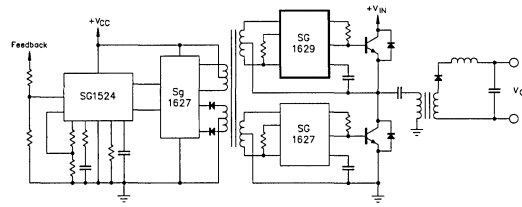
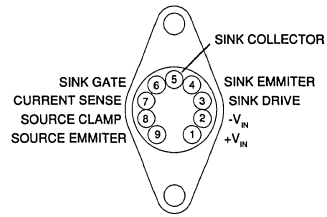
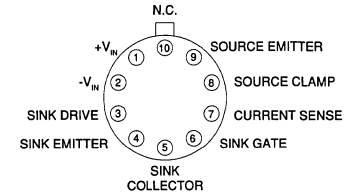


FIGURE 9

A simplified drive system for a half-bridge switched mode converter. A full bridge drive may be accommodated with four SG1629 drivers and additional current boosting for the SG1627.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
9-PIN METAL CAN R - PACKAGE	SG1629R/883B SG1629R SG3629R	-55°C to 125°C -55°C to 125°C 0°C to 70°C	
10-PIN METAL CAN T - PACKAGE	SG1629T/883B SG1629T SG3629T	-55°C to 125°C -55°C to 125°C 0°C to 70°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.
3. Case is internally connected to pin 4 on both packages.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

DUAL HIGH SPEED DRIVER

DESCRIPTION

The SG1644, 2644, 3644 is a dual non-inverting monolithic high speed driver. This device utilizes high voltage Schottky logic to convert TTL signals to high speed outputs up to 18V. The totem pole outputs have 3A peak current capability, which enables them to drive 1000pF loads in typically less than 25ns. These speeds make it ideal for driving power MOSFETs and other large capacitive loads requiring high speed switching.

In addition to the standard packages, Silicon General offers the 16 pin Batwing (W-package) and 16 pin S.O.I.C. (DW-package) for commercial and industrial applications and the Hermetic TO-66 (R-package) for military use. These packages offer improved thermal performance for applications requiring high frequencies and/or high peak currents.

FEATURES

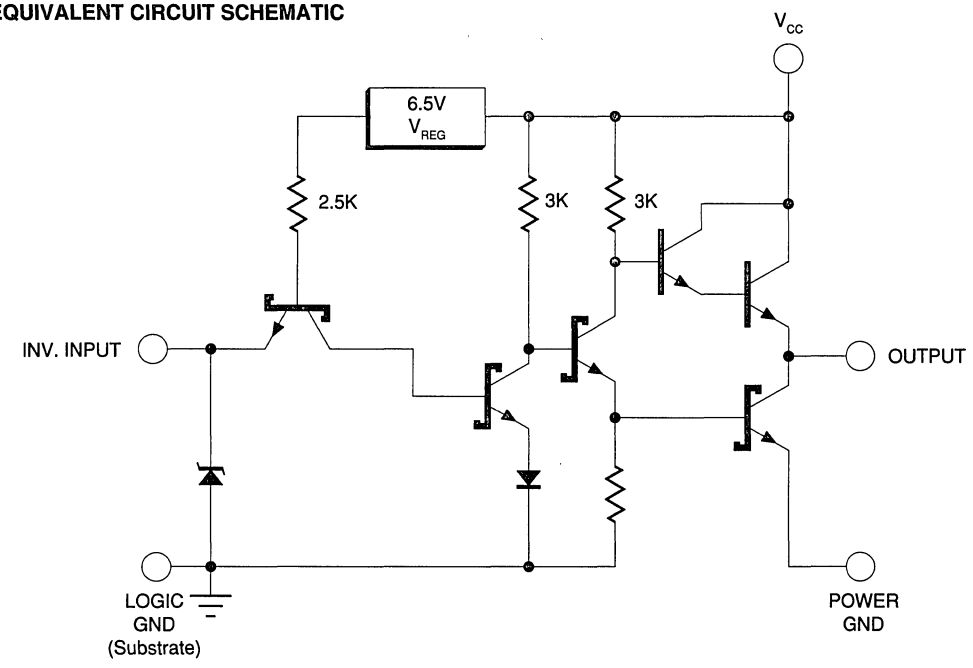
- **Totem pole outputs with 3.0A peak current capability.**
- **Supply voltage to 22V.**
- **Rise and fall times less than 25ns.**
- **Propagation delays less than 20ns.**
- **Non-inverting high-speed high-voltage Schottky logic.**
- **Efficient operation at high frequency.**
- **Available in:**
  - **8 Pin Plastic and Ceramic DIP**
  - **14 Pin Ceramic DIP**
  - **16 Pin Batwing DIP**
  - **16 Pin Plastic S.O.I.C.**
  - **TO-99**
  - **TO-66**

HIGH RELIABILITY FEATURES - SG1644

- **Available to MIL-STD-883**
- **Radiation data available**
- **SG level "S" processing available**

6

EQUIVALENT CIRCUIT SCHEMATIC



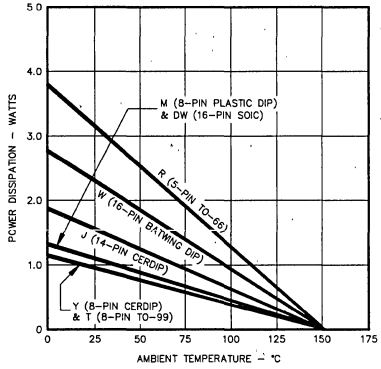
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V_{CC}) 22V
Logic Input Voltage 7V
Source/Sink Output Current (Each Output)
Continuous ..... ±0.5A
Pulse, 500ns ..... ±3.0A

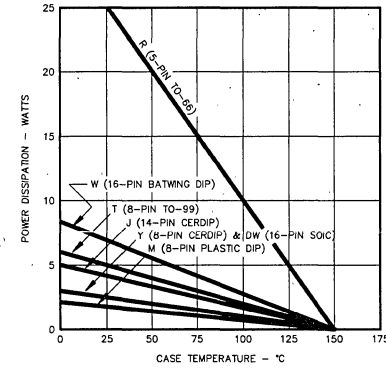
Operating Junction Temperature
Hermetic (J, T, Y, R-Packages) ..... 150°C
Plastic (M, DW, W-Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device. All voltages are with respect to ground. All currents are positive into the specified terminal.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage (V_{CC}) ..... 4.5V to 20V (Note 3)
Frequency Range ..... DC to 1.5MHz
Peak Pulse Current ..... ±3A
Logic Input Voltage ..... -0.5 to 5.5V

Operating Ambient Temperature Range (T_A)
SG1644 ..... -55°C to 125°C
SG2644 ..... -25°C to 85°C
SG3644 ..... 0°C to 70°C

Note 2. Range over which the device is functional.
Note 3. AC performance has been optimized for V_{CC} = 8V to 20V.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specfiications apply over the operating ambient temperatures for SG1644 with -55°C ≤ T_A ≤ 125°C, SG2644 with -25°C ≤ T_A ≤ 85°C, SG3644 with 0°C ≤ T_A ≤ 70°C, and V_{CC} = 20V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1644/2644/3644			Units
		Min.	Typ.	Max.	
Static Characteristics					
Logic 1 Input Voltage		2.0			V
Logic 0 Input Voltage				0.7	V
Input High Current	V_{IN} = 2.4V			200	µA
Input High Current	V_{IN} = 5.5V			1.0	mA
Input Low Current	V_{IN} = 0V			-4	mA
Input Clamp Voltage	I_{IN} = -10mA			-1.5	V
Output High Voltage (Note 4)	I_{OUT} = -200mA	V_{CC}-3			V
Output Low Voltage (Note 4)	I_{OUT} = 200mA			1.0	V
Supply Current Outputs Low	V_{IN} = 0V (both inputs)		18	27	mA
Supply Current Outputs High	V_{IN} = 2.4V (both inputs)		7.5	12	mA

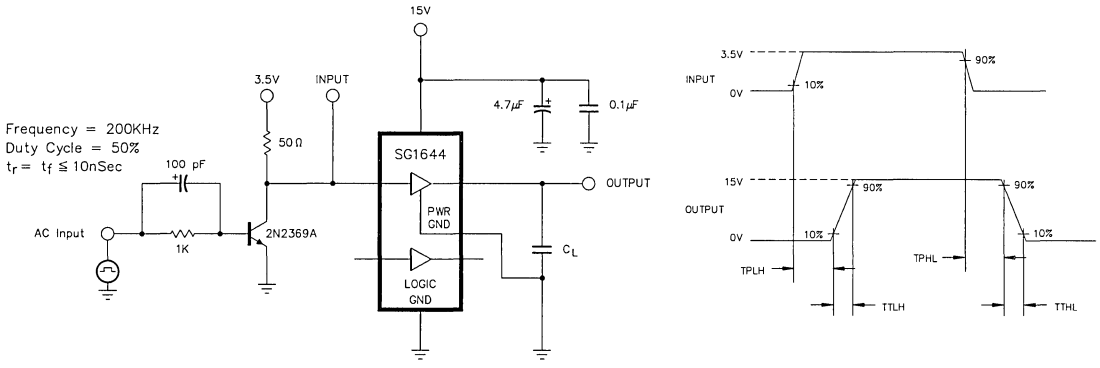
Note 4. V_{CC} = 10V to 20V.

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions (Figure 1)	SG1644/2644/3644 T_A= 25°C			SG1644 T_A=-55°C to 125°C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Dynamic Characteristics (Note 6)								
Propagation Delay High-Low (TPHL)	C_L = 1000pF (Note 5)			30			40	ns
	C_L = 2500pF		26	35			50	ns
Propagation Delay Low-High (TPLH)	C_L = 1000pF (Note 5)			25			30	ns
	C_L = 2500pF		18	30			40	ns
Rise Time (TTLH)	C_L = 1000pF (Note 5)			30			35	ns
	C_L = 2500pF		30	40			50	ns
Fall Time (TTHL)	C_L = 1000pF (Note 5)			25			30	ns
	C_L = 2500pF		30	40			50	ns
Supply Current (I_{CC}) (both outputs)	C_L = 2500pF, Freq. = 200KHz Duty Cycle = 50%		30	35			40	mA

Note 5. These parameters, specified at 1000pF, although guaranteed over recommended operating conditions, are not tested in production.
Note 6. V_{CC} = 15V.

AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS - FIGURE 1



CHARACTERISTIC CURVES

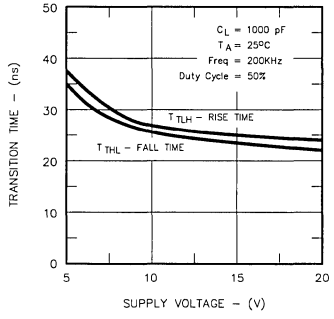


FIGURE 2.
TRANSITION TIMES VS. SUPPLY VOLTAGE

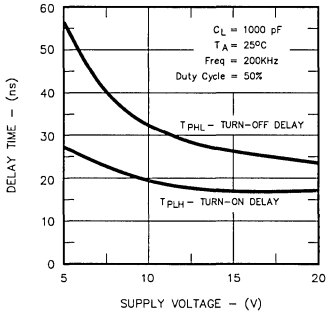


FIGURE 3.
PROPAGATION DELAY VS. SUPPLY VOLTAGE

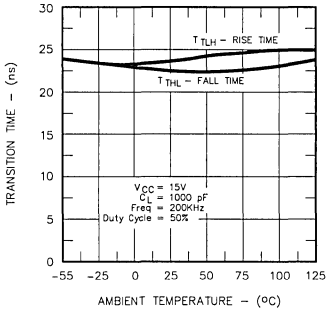


FIGURE 4.
TRANSITION TIMES VS. AMBIENT TEMPERATURE

CHARACTERISTIC CURVES (continued)

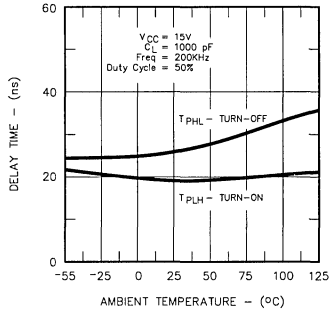


FIGURE 5.
PROPAGATION DELAY VS. AMBIENT TEMPERATURE

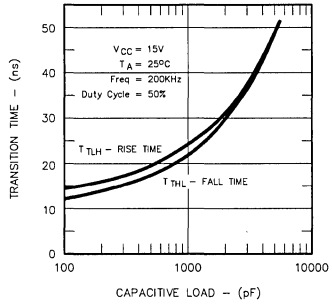


FIGURE 6.
TRANSITION TIMES VS. CAPACITIVE LOAD

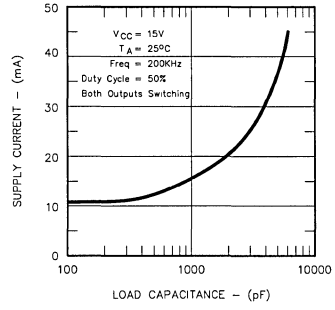


FIGURE 7.
SUPPLY CURRENT VS. CAPACITANCE LOAD

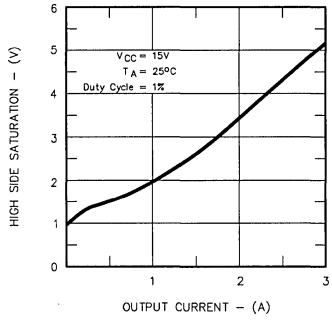


FIGURE 8.
HIGH SIDE SATURATION VS. OUTPUT CURRENT

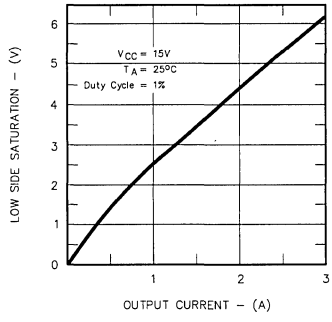


FIGURE 9.
LOW SIDE SATURATION VS. OUTPUT CURRENT

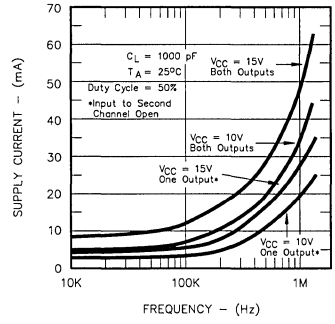


FIGURE 10.
SUPPLY CURRENT VS. FREQUENCY

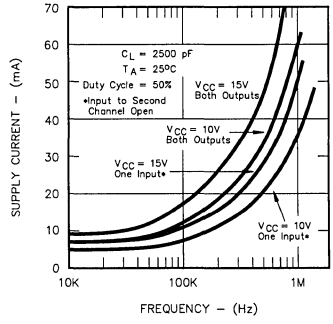


FIGURE 11.
SUPPLY CURRENT VS. FREQUENCY

APPLICATION INFORMATION

POWER DISSIPATION

The SG1644, while more energy-efficient than earlier gold-doped driver IC's, can still dissipate considerable power because of its high peak current capability at high frequencies. Total power dissipation in any specific application will be the sum of the DC or steady-state power dissipation, and the AC dissipation caused by driving capacitive loads.

The DC power dissipation is given by:

$P_{DC} = +V_{CC} \cdot I_{CC}$ [1]

where I_{CC} is a function of the driver state, and hence is duty-cycle dependent.

The AC power dissipation is proportional to the switching frequency, the load capacitance, and the square of the output voltage. In most applications, the driver is constantly changing state, and the AC contribution becomes dominant when the frequency exceeds 100-200KHz.

The SG1644 driver family is available in a variety of packages to accommodate a wide range of operating temperatures and power dissipation requirements. The Absolute Maximums section of the data sheet includes two graphs to aid the designer in choosing an appropriate package for his design.

The designer should first determine the actual power dissipation of the driver by referring to the curves in the data sheet relating operating current to supply voltage, switching frequency, and capacitive load. These curves were generated from data taken on actual devices. The designer can then refer to the Absolute Maximum Thermal Dissipation curves to choose a package type, and to determine if heat-sinking is required.

DESIGN EXAMPLE

Given: Two 2500pF loads must be driven push-pull from a +15 volt supply at 100KHz. The application is a commercial one in which the maximum ambient temperature is +50°C, and cost is important.

1. From Figure 11, the average driver current consumption under these conditions will be 18mA, and the power dissipation will be 15volts x 18mA, or 270mW.

2. From the ambient thermal characteristic curve, it can be seen that the M package, which is an 8-pin plastic DIP with a copper lead frame, has more than enough thermal conductance from junction to ambient to support operation at an ambient temperature of +50°C. The SG36446M driver would be specified for this application.

SUPPLY BYPASSING

Since the SG1644 can deliver peak currents above 3amps under some load conditions, adequate supply bypassing is essential for proper operation. Two capacitors in parallel are recommended to guarantee low supply impedance over a wide bandwidth: a 0.1µF ceramic disk capacitor for high frequencies, and a 4.7µF solid tantalum capacitor for energy storage. In military applications, a CK05 or CK06 ceramic operator with a CSR-13 tantalum capacitor is an effective combination. For commercial applications, any low-inductance ceramic disk capacitor teamed with a Sprague 150D or equivalent low ESR capacitor will work well. The capacitors must be located as close as physically possible to the V_{CC} pin, with combined lead and pc board trace lengths held to less than 0.5 inches.

GROUNDING CONSIDERATIONS

The ability of the SG1644 to deliver high peak currents into capacitive loads can cause undesirable negative transients on the logic and power grounds. To avoid this, a low inductance ground path should be considered for each output to return the high peak currents back to it's own ground point. A ground plane is recommended for best performance. If space for a ground plane is not available, make the paths as short and as wide as possible. The logic ground can be returned to the supply bypass capacitor and be connected at one point to the power grounds.

LOGIC INTERFACE

The logic input of the 1644 is designed to accept standard DC-coupled 5 volt logic swings, with no speed-up capacitors required. If the input signal voltage exceeds 6 volts, the input pin must be protected against the excessive voltage in the HIGH state. Either a high speed blocking diode must be used, or a resistive divider to attenuate the logic swing is necessary.

LAYOUT FOR HIGH SPEED

The SG1644 can generate relatively large voltage excursions with rise and fall times around 20-30 nanoseconds with light capacitive loads. A Fourier analysis of these time domain signals will indicate strong energy components at frequencies much higher than the basic switching frequency. These high frequencies can induce ringing on an otherwise ideal pulse if sufficient inductance occurs in the signal path (either the positive signal trace or the ground return). Overshoot on the rising edge is undesirable because the excess drive voltage could rupture the gate oxide of a power MOSFET. Trailing edge undershoot is dangerous because the negative voltage excursion can forward-bias the parasitic PN substrate diode of the driver, potentially causing erratic operation or outright failure.

Ringing can be reduced or eliminated by minimizing signal path inductance, and by using a damping resistor between the drive output and the capacitive load. Inductance can be reduced by keeping trace lengths short, trace widths wide, and by using 2oz. copper if possible. The resistor value for critical damping can be calculated from:

$R_D = 2\sqrt{L/C_L}$ [2]

where L is the total signal line inductance, and C_L is the load capacitance. Values between 10 and 100ohms are usually sufficient. Inexpensive carbon composition resistors are best because they have excellent high frequency characteristics. They should be located as close as possible to the gate terminal of the power MOSFET.

TYPICAL APPLICATIONS

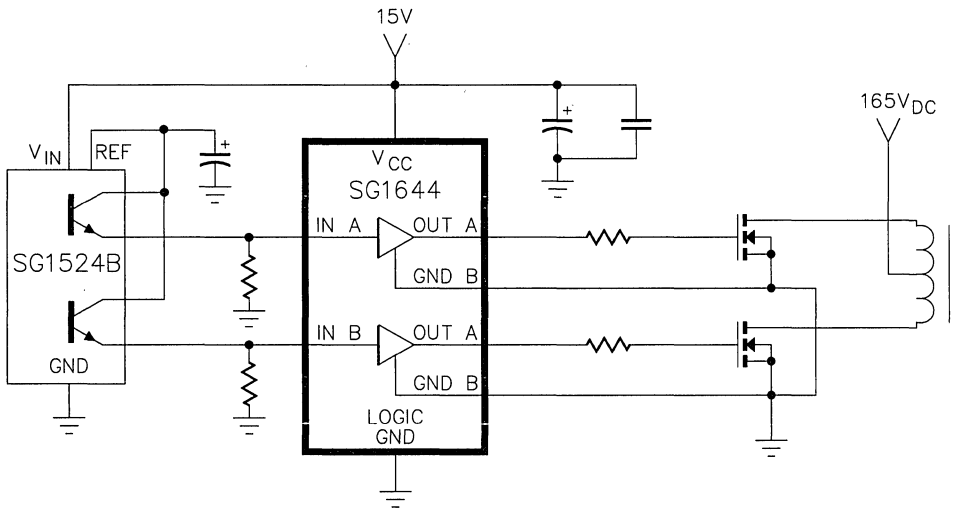


FIGURE 12.
In this push pull converter circuit, the control capailities of the SG1524B PWM are combined with the powerful totem-pole drivers found in the SG1644 (see SG1626 for example). This inexpensive configuration results in very fast charge and discharge of the power MOSFET gate capacitance for efficient switching.

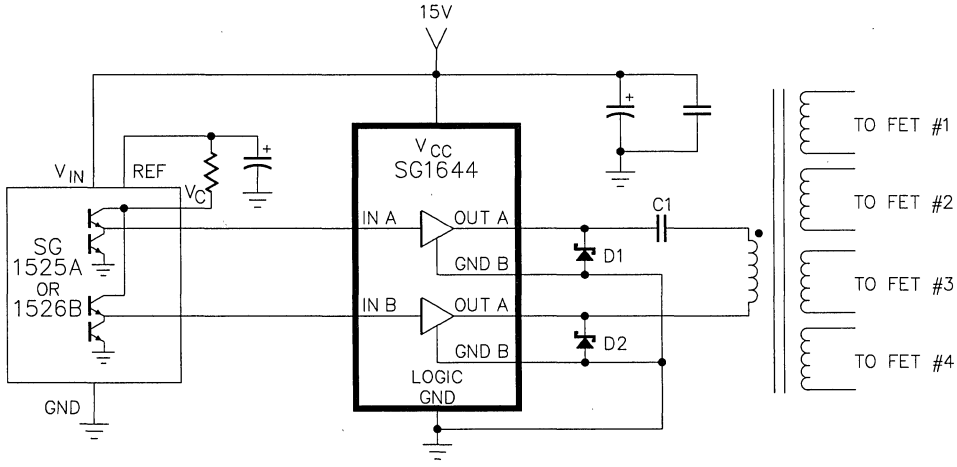


FIGURE 13.
When the peak current capabilites of PWM's such as 1525A or 1526B are not sufficient to drive high capacitive loads fast enough, SG1644 is one solution to this problem. This combination is especially suited for full bridge applications where high input capacitance MOSFETs are being used. Diodes D1 and D2 are necessary if the leakage inductance of the drive transformer will drive the output pins negative.

TYPICAL APPLICATIONS (continued)

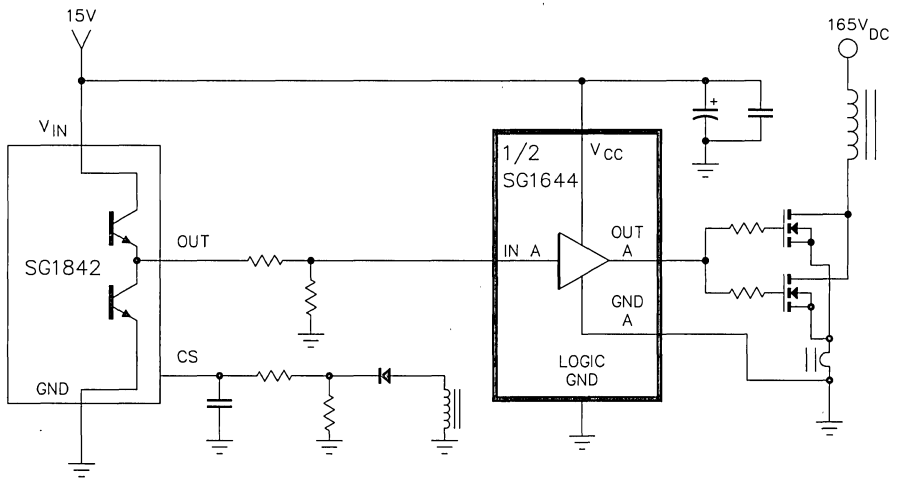


FIGURE 14.
A low cost, yet powerful alternative to the single ended converters with parallel MOSFETs is a combination of SG1842 and SG1644 as shown in Figure 16. This combination will also allow a low noise operation by separating the drive and its associated high peak currents, away from the PWM logic section.

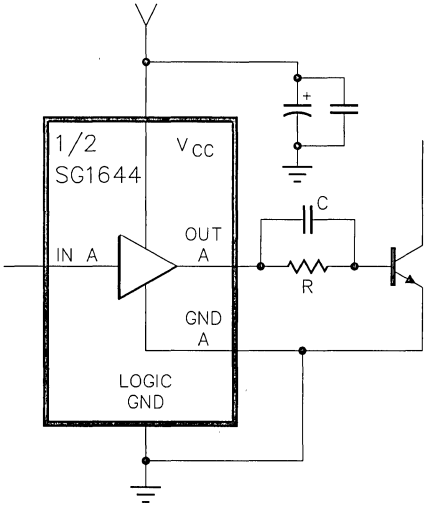


FIGURE 15.
Fast turn off of bipolar transistors is possible by the totem pose output stage of SG1644. The charge on capacitor C will drive the base negative for faster turn off.

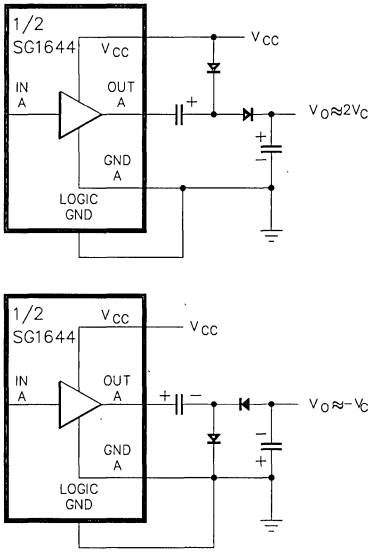
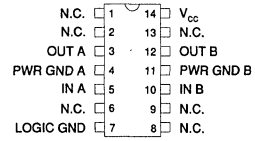
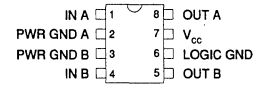
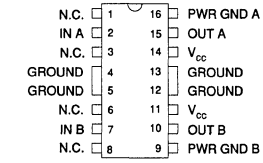
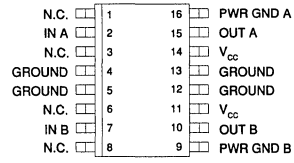
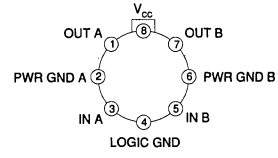
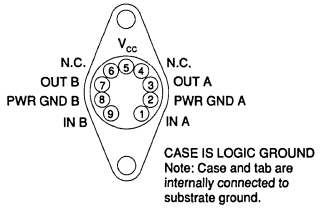


FIGURE 16.
When the inputs are driven with a TTL square wave drive, the high peak current capabilites of SG1644 allow easy implementation of charge pump voltage converters.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN CERAMIC DIP J - PACKAGE	SG1644J/883B SG1644J SG2644J SG3644J	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
8-PIN CERAMIC DIP Y - PACKAGE 8-PIN PLASTIC DIP M - PACKAGE	SG1644Y/883B SG1644Y SG2644Y SG3644Y SG2644M SG3644M	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C -25°C to 85°C 0°C to 70°C	
16-PIN BATWING DIP W - PACKAGE	SG2644W SG3644W	-25°C to 85°C 0°C to 70°C	
16-PIN WIDE BODY PLASTIC S.O.I.C. DW - PACKAGE	SG2626DW SG3626DW	-25°C to 85°C 0°C to 70°C	
8-PIN TO-99 METAL CAN T - PACKAGE	SG1644T/883B SG1644T SG2644T SG3644T	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
9-PIN TO-66 METAL CAN R - PACKAGE	SG1644R/883B SG1644R SG2644R SG3644R	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

SG2000 SERIES

HIGH VOLTAGE MEDIUM CURRENT DRIVER ARRAYS

DESCRIPTION

The SG2000 series integrates seven NPN Darlington pairs with internal suppression diodes to drive lamps, relays, and solenoids in many military, aerospace, and industrial applications that require severe environments. All units feature open collector outputs with greater than 50V breakdown voltages combined with 500mA current carrying capabilities. Five different input configurations provide optimized designs for interfacing with DTL, TTL, PMOS, or CMOS drive signals. These devices are designed to operate from -55°C to 125°C ambient temperature in a 16 pin dual in line ceramic (J) package and 20 pin Leadless Chip Carrier (LCC). The plastic dual in–line (N) and S.O.I.C. (DW) are designed to operate over the commercial temperature range of 0°C to 70°C.

FEATURES

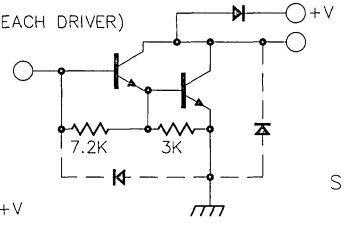
- **Seven npn Darlington pairs**
- **-55°C to 125°C ambient operating temperature range**
- **Collector currents to 600mA**
- **Output voltages from 50V to 95V**
- **Internal clamping diodes for inductive loads**
- **DTL, TTL, PMOS, or CMOS compatible inputs**
- **Hermetic ceramic package**

HIGH RELIABILITY FEATURES

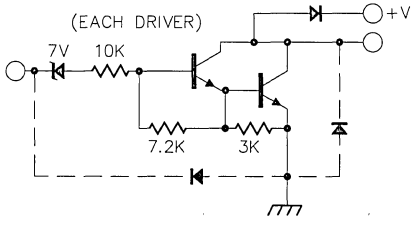
- **Available to MIL-STD-883 and DESC SMD**
- **MIL-M38510/14101BEA - JAN2001J**
- **MIL-M38510/14102BEA - JAN2002J**
- **MIL-M38510/14103BEA - JAN2003J**
- **MIL-M38510/14104BEA - JAN2004J**
- **MIL-M38510/14105BEA - JAN2005J**
- **Radiation data available**
- **SG level "S" processing available**

PARTIAL SCHEMATICS

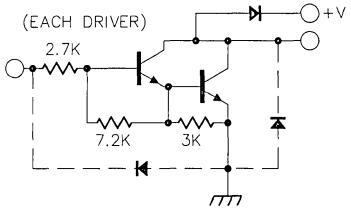
SG2001/2011/2021



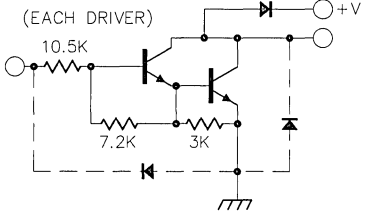
SG2002/2012/2022



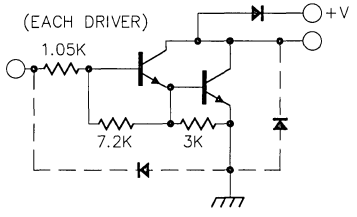
SG2003/2013/2023



SG2004/2014/2024



SG2005/2015/2025



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April 1990

ABSOLUTE MAXIMUM RATINGS (Note 1)

Output Voltage, V_{CE}
- (SG2000, 2010 series) 50V
- (SG2020 series) 95V

Input Voltage, V_{IN}
- (SG2002,3,4) 30V
- (SG2005) 15V

Continuous Input Current, I_{IN} 25mA

Note 1. Values beyond which damage may occur.

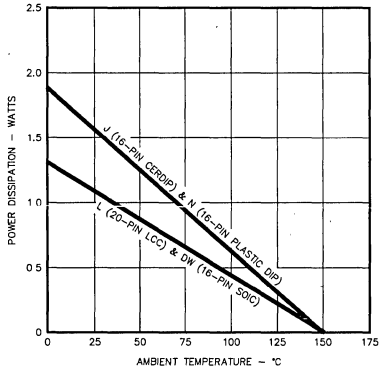
Peak Collector Current, I_C
- (SG2000, 2020) 500mA
- (SG2010) 600mA

Operating Junction Temperature
- Hermetic (J, L Packages) ..... 150°C
- Plastic (N, DW Packages) ..... 150°C

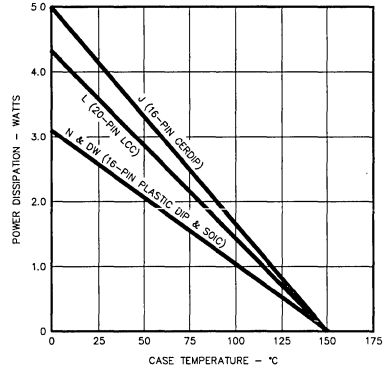
Storage Temperature Range ..... -65°C to 150°C

Lead Temperature (Soldering 10 sec.) ..... 300°C

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Output Voltage, V_{CE}
- SG2000, SG2020 series 50V
- SG2010 series 95V

Note 2. Range over which the device is functional.

Peak Collector Current, I_C
- SG2000, SG2020 series 350mA
- SG2010 series 500mA

Operating Ambient Temperature Range
- SG2000 Series - Hermetic ..... -55°C to 125°C
- SG2000 Series - Plastic ..... 0°C to 70°C

SELECTION GUIDE

Device	V_{CE} Max	I_C Max	Logic Inputs
SG2001	50V	500mA	General Purpose PMOS, CMOS
SG2002	50V	500mA	14V-25V PMOS
SG2003	50V	500mA	5V TTL, CMOS
SG2004	50V	500mA	6V-15V CMOS, PMOS
SG2005	50V	500mA	High Output TTL
SG2011	50V	600mA	General Purpose PMOS, CMOS
SG2012	50V	600mA	14V-25V PMOS

Device	V_{CE} Max	I_C Max	Logic Inputs
SG2013	50V	600mA	5V TTL, CMOS
SG2014	50V	600mA	6V-15V CMOS, PMOS
SG2015	50V	600mA	High Output TTL
SG2021	95V	500mA	General Purpose PMOS, CMOS
SG2022	95V	500mA	14V-25V PMOS
SG2023	95V	500mA	5V TTL, CMOS
SG2024	95V	500mA	6V-15V CMOS, PMOS

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG2000 series - Hermetic - with -55°C ≤ T_A ≤ 125°C and SG2000 series - Plastic - with 0°C ≤ T_A ≤ 70°C. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

SG2001 thru SG2005

Parameter	Applicable Devices	Temp.	Test Conditions	Limits			Units
				Min.	Typ.	Max.	
Output Leakage Current (I_{CEX})	All		V_{CE} = 50V			100	µA
	SG2002		V_{CE} = 50V, V_{IN} = 6V			500	µA
	SG2004		V_{CE} = 50V, V_{IN} = 1V			500	µA
Collector - Emitter ($V_{CE(SAT)}$)	All	$T_A = T_{MIN}$	I_C = 350mA, I_B = 850µA		1.6	1.8	V
		$T_A = T_{MIN}$	I_C = 200mA, I_B = 550µA		1.3	1.5	V
		$T_A = T_{MIN}$	I_C = 100mA, I_B = 350µA		1.1	1.3	V
		T_A = 25°C	I_C = 350mA, I_B = 500µA		1.25	1.6	V
		T_A = 25°C	I_C = 200mA, I_B = 350µA		1.1	1.3	V
		T_A = 25°C	I_C = 100mA, I_B = 250µA		0.9	1.1	V
		$T_A = T_{MAX}$	I_C = 350mA, I_B = 500µA		1.6	1.8	V
		$T_A = T_{MAX}$	I_C = 200mA, I_B = 350µA		1.3	1.5	V
		$T_A = T_{MAX}$	I_C = 100mA, I_B = 250µA		1.1	1.3	V
Input Current ($I_{IN(ON)}$)	SG2002		V_{IN} = 17V	480	850	1300	µA
	SG2003		V_{IN} = 3.85V	650	930	1350	µA
	SG2004		V_{IN} = 5V	240	350	500	µA
			V_{IN} = 12V	650	1000	1450	µA
	SG2005		V_{IN} = 3V	1180	1500	2400	µA
($I_{IN(OFF)}$)	All	$T_A = T_{MAX}$	I_C = 500µA	25	50		µA
Input Voltage ($V_{IN(ON)}$)	SG2002	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 300mA			18	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 300mA			13	V
	SG2003	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 200mA			3.3	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 250mA			3.6	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 300mA			3.9	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 200mA			2.4	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 250mA			2.7	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 300mA			3.0	V
	SG2004	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 125mA			6.0	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 200mA			8.0	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 275mA			10	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 350mA			12	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 125mA			5.0	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 200mA			6.0	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 275mA			7.0	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 350mA			8.0	V
	SG2005	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 350mA			3.0	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 350mA			2.4	V
D-C Forward Current	SG2001	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 350mA	500			
Transfer Ratio (h_{FE})		T_A = 25°C	V_{CE} = 2V, I_C = 350mA	1000			
Input Capacitance (C_{IN}) (Note 3)	All	T_A = 25°C			15	25	pF
Turn-On Delay (TPLH)	All	T_A = 25°C	0.5 E_{IN} to 0.5 E_{OUT}		250	1000	ns
Turn-Off Delay (TPHL)	All	T_A = 25°C	0.5 E_{IN} to 0.5 E_{OUT}		250	1000	ns
Clamp Diode Leakage Current (I_R)	All		V_R = 50V			50	µA
Clamp Diode Forward Voltage (V_F)	All		I_F = 350mA		1.7	2.0	V

Note 3. These parameters, although guaranteed, are not tested in production.

6

ELECTRICAL SPECIFICATIONS (continued)

SG2011 thru SG2015

Parameter	Applicable Devices	Temp.	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Output Leakage Current (I_{CEX})	All		V_{CE} = 50V			100	µA
	SG2012		V_{CE} = 50V, V_{IN} = 6V			500	µA
	SG2014		V_{CE} = 50V, V_{IN} = 1V			500	µA
Collector - Emitter ($V_{CE(SAT)}$)	All	$T_A = T_{MIN}$	I_C = 500mA, I_B = 1100µA		1.8	2.1	V
		$T_A = T_{MIN}$	I_C = 350mA, I_B = 850µA		1.6	1.8	V
		$T_A = T_{MIN}$	I_C = 200mA, I_B = 550µA		1.3	1.5	V
		T_A = 25°C	I_C = 500mA, I_B = 600µA		1.7	1.9	V
		T_A = 25°C	I_C = 350mA, I_B = 500µA		1.25	1.6	V
		T_A = 25°C	I_C = 200mA, I_B = 350µA		1.1	1.3	V
		$T_A = T_{MAX}$	I_C = 500mA, I_B = 600µA		1.8	2.1	V
		$T_A = T_{MAX}$	I_C = 350mA, I_B = 500µA		1.6	1.8	V
		$T_A = T_{MAX}$	I_C = 200mA, I_B = 350µA		1.3	1.5	V
Input Current ($I_{IN(ON)}$)	SG2012		V_{IN} = 17V	480	850	1300	µA
	SG2013		V_{IN} = 3.85V	650	930	1350	µA
	SG2014		V_{IN} = 5V	240	350	500	µA
			V_{IN} = 12V	650	1000	1450	µA
	SG2015		V_{IN} = 3V	1180	1500	2400	µA
($I_{IN(OFF)}$)	All	$T_A = T_{MAX}$	I_C = 500µA	25	50		µA
Input Voltage ($V_{IN(ON)}$)	SG2012	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 500mA			23.5	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 500mA			17	V
	SG2013	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 250mA			3.6	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 300mA			3.9	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 500mA			6.0	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 250mA			2.7	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 300mA			3.0	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 500mA			3.5	V
	SG2014	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 275mA			10	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 350mA			12	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 500mA			17	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 275mA			7.0	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 350mA			8.0	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 500mA			9.5	V
	SG2015	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 350mA			3.0	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 500mA			3.5	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 350mA			2.4	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 500mA			2.6	V
D-C Forward Current	SG2011	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 500mA	450			
Transfer Ratio (h_{FE})		T_A = 25°C	V_{CE} = 2V, I_C = 500mA	900			
Input Capacitance (C_{IN}) (Note 3)	All	T_A = 25°C			15	25	pF
Turn-On Delay (TPLH)	All	T_A = 25°C	0.5 E_{IN} to 0.5 E_{OUT}		250	1000	ns
Turn-Off Delay (TPHL)	All	T_A = 25°C	0.5 E_{IN} to 0.5 E_{OUT}		250	1000	ns
Clamp Diode Leakage Current (I_R)	All		V_R = 50V			50	µA
Clamp Diode Forward Voltage (V_F)	All		I_F = 350mA		1.7	2.0	V
			I_F = 500mA			2.5	V

Note 3. These parameters, although guaranteed, are not tested in production.

ELECTRICAL SPECIFICATIONS (continued)

SG2021 thru SG2025

Parameter	Applicable Devices	Temp.	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Output Leakage Current (I_{CEX})	All		V_{CE} = 95V			100	µA
	SG2022		V_{CE} = 95V, V_{IN} = 6V			500	µA
	SG2024		V_{CE} = 95V, V_{IN} = 1V			500	µA
Collector - Emitter ($V_{CE(SAT)}$)	All	$T_A = T_{MIN}$	I_C = 350mA, I_B = 850µA		1.6	1.8	V
		$T_A = T_{MIN}$	I_C = 200mA, I_B = 550µA		1.3	1.5	V
		$T_A = T_{MIN}$	I_C = 100mA, I_B = 350µA		1.1	1.3	V
		T_A = 25°C	I_C = 350mA, I_B = 500µA		1.25	1.6	V
		T_A = 25°C	I_C = 200mA, I_B = 350µA		1.1	1.3	V
		T_A = 25°C	I_C = 100mA, I_B = 250µA		0.9	1.1	V
		$T_A = T_{MAX}$	I_C = 350mA, I_B = 500µA		1.6	1.8	V
		$T_A = T_{MAX}$	I_C = 200mA, I_B = 350µA		1.3	1.5	V
		$T_A = T_{MAX}$	I_C = 100mA, I_B = 250µA		1.1	1.3	V
Input Current ($I_{IN(ON)}$)	SG2022		V_{IN} = 17V	480	850	1300	µA
	SG2023		V_{IN} = 3.85V	650	930	1350	µA
	SG2024		V_{IN} = 5V	240	350	500	µA
			V_{IN} = 12V	650	1000	1450	µA
	SG2025		V_{IN} = 3V	1180	1500	2400	µA
($I_{IN(OFF)}$)	All	$T_A = T_{MAX}$	I_C = 500µA	25	50		µA
Input Voltage ($V_{IN(ON)}$)	SG2022	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 300mA			18	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 300mA			13	V
	SG2023	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 200mA			3.3	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 250mA			3.6	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 300mA			3.9	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 200mA			2.4	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 250mA			2.7	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 300mA			3.0	V
	SG2024	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 125mA			6.0	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 200mA			8.0	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 275mA			10	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 350mA			12	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 125mA			5.0	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 200mA			6.0	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 275mA			7.0	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 350mA			8.0	V
	SG2025	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 350mA			3.0	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 350mA			2.4	V
D-C Forward Current Transfer Ratio (h_{FE})	SG2021	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 350mA	500			
		T_A = 25°C	V_{CE} = 2V, I_C = 350mA	1000			
Input Capacitance (C_{IN}) (Note 3)	All	T_A = 25°C			15	25	pF
Turn-On Delay (TPLH)	All	T_A = 25°C	0.5 E_{IN} to 0.5 E_{OUT}		250	1000	ns
Turn-Off Delay (TPHL)	All	T_A = 25°C	0.5 E_{IN} to 0.5 E_{OUT}		250	1000	ns
Clamp Diode Leakage Current (I_R)	All		V_R = 95V			50	µA
Clamp Diode Forward Voltage (V_F)	All		I_F = 350mA		1.7	2.0	V

Note 3. These parameters, although guaranteed, are not tested in production.

CHARACTERISTIC CURVES

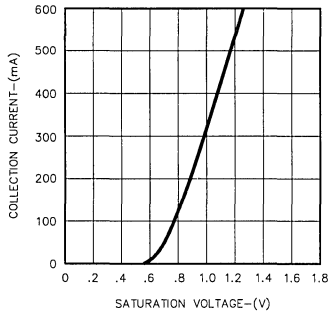


FIGURE 1.
OUTPUT CHARACTERISTICS

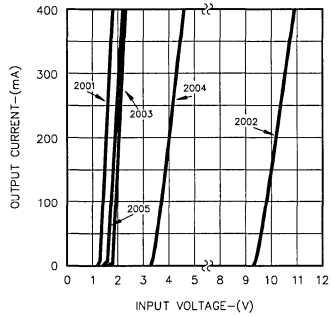


FIGURE 2.
OUTPUT CURRENT VS. INPUT VOLTAGE

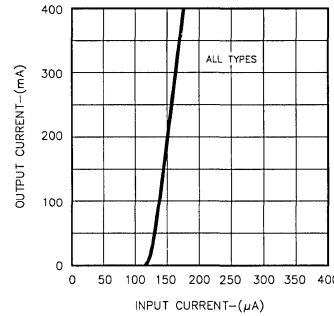


FIGURE 3.
OUTPUT CURRENT VS. INPUT CURRENT

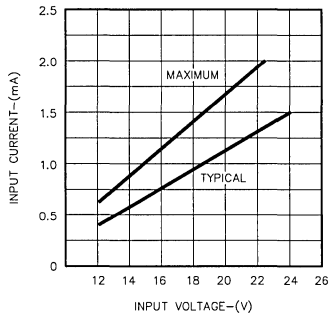


FIGURE 4.
INPUT CHARACTERISTICS - SG2002

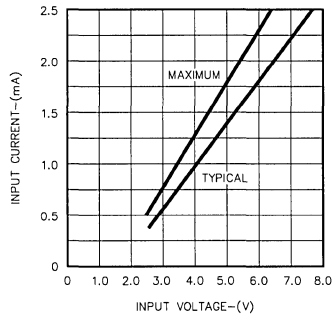


FIGURE 5.
INPUT CHARACTERISTICS - SG2003

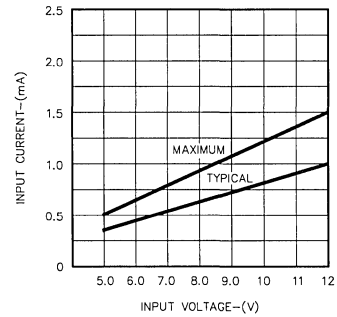


FIGURE 6.
INPUT CHARACTERISTICS - SG2004

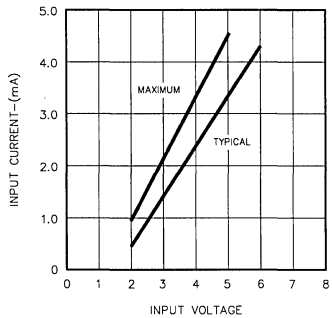


FIGURE 7.
INPUT CHARACTERISTICS - SG2005

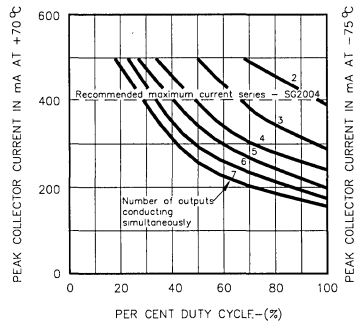
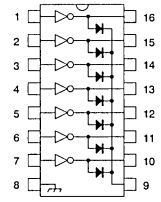
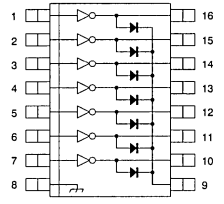
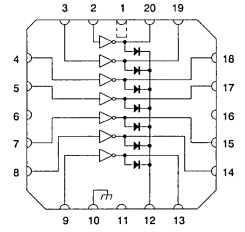


FIGURE 8.
PEAK COLLECTOR CURRENT VS. DUTY CYCLE

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No. (Note 3)	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG2XXXJ/883B SG2XXXJ	-55°C to 125°C -55°C to 125°C	
16-PIN PLASTIC DIP N - PACKAGE	SG2XXXN	0°C to 70°C	
16-PIN WIDE BODY PLASTIC S.O.I.C. DW - PACKAGE	SG2XXXDW	0°C to 70°C	
20-PIN CERAMIC LEADLESS CHIP CARRIER L- PACKAGE	SG2XXXL/883B SG2XXXL	-55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availability.
2. All parts are viewed from the top.
3. See selection guide for specific device types.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

QUAD 1.5 AMP DARLINGTON SWITCHES

DESCRIPTION

These high-voltage, high-current Darlington arrays are monolithic bipolar devices especially designed for interfacing low-level control logic and peripheral loads such as relays, solenoids, DC and stepping motors; multiplexed LED and incandescent displays; and heaters. The logic inputs are designed to be compatible with TTL, DTL, LSTTL, CMOS and NMOS logic families. Several of the arrays include integral clamp diodes for driving inductive loads, and breakdown voltage ratings to 80 volts are available.

All devices are supplied in a modified 16-lead plastic dual-in-line batwing package. A copper alloy lead frame with webbing between the central pins provides low thermal resistance to ambient air, and allows a 2.8 watt total power dissipation rating within a standard footprint.

These devices are direct replacements for ULN-2064B thru ULN-2077B devices.

FEATURES

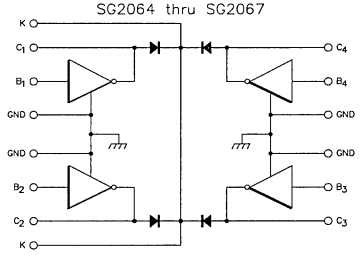
- **Four power drivers per package**
- **1.5 Amp collector currents**
- **80V and 50V BV_{CEX} ratings**
- **Integral clamp diodes for inductive loads**
- **Compatibility with all popular logic families**
- **Low internal parasitics**

HIGH RELIABILITY FEATURES - SG2069

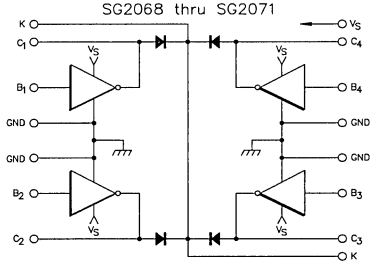
- **Available to MIL-STD-883 and DESC SMD**

BLOCK DIAGRAM

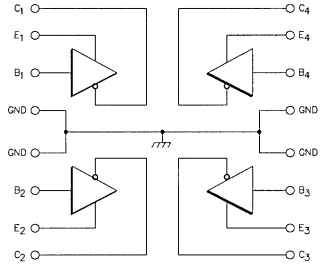
SG2064 thru SG2067



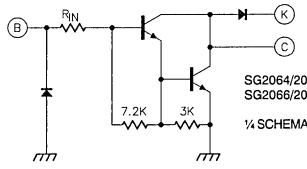
SG2068 thru SG2071



SG2074 thru SG2077

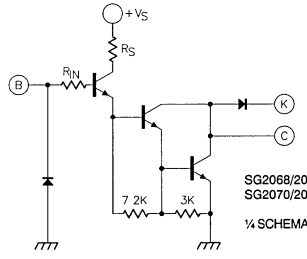


PARTIAL SCHEMATICS



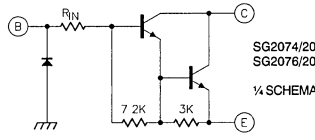
SG2064/2065: R_{IN} = 350Ω
SG2066/2067: R_{IN} = 3KΩ

¼ SCHEMATIC SHOWN



SG2068/2069: R_{IN} = 2.5K, R_S = 900Ω
SG2070/2071: R_{IN} = 11.6K, R_S = 3.4KΩ

¼ SCHEMATIC SHOWN



SG2074/2075: R_{IN} = 350Ω
SG2076/2077: R_{IN} = 3KΩ

¼ SCHEMATIC SHOWN

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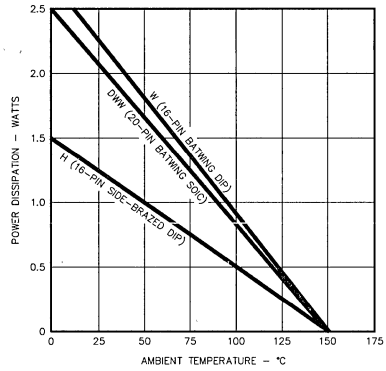
April 1990

ABSOLUTE MAXIMUM RATINGS (Note 1)

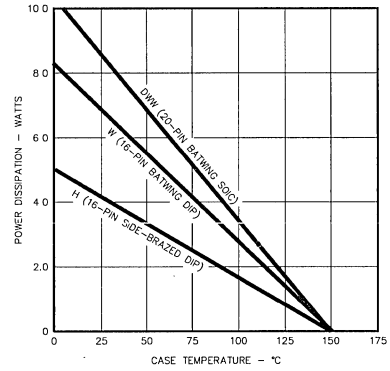
Logic Input Voltage ..... (Note 2)
Logic Input Current 25mA
Supply Voltage
  SG2068/2069 ..... 12V
  SG2070/2071 ..... 22V
Output Voltage ..... (Note 2)
Output Current 1.75A
Operating Junction Temperature
  Hermetic (H-Packages) ..... 150°C
  Plastic (W-Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering 10 sec.) ..... 300°C

Note 1. Values beyond which damage may occur.
Note 2. See Selection Guide located on last page of this data sheet.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 3)

Peak Output Current 1.5A
Supply Voltage
  SG2068/2069 ..... 10V
  SG2070/2071 ..... 20V
Operating Ambient Temperature Range
  SG2069 (Side-Brazed) ..... -55°C to 125°C
  SG2064 thru SG2077 (Batwing) ..... 0°C to 70°C

Note 3. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply for the operating ambient temperature of T_A = 25°C. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

SG2064 thru SG2067

Parameter	Applicable Devices	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Leakage Current	SG2064/2066	V_{CE} = 50V			100	µA
		V_{CE} = 50V, T_A = T_{MAX}			500	µA
	SG2065/2067	V_{CE} = 80V			100	µA
		V_{CE} = 80V, T_A = T_{MAX}			500	µA
Output Sustaining Voltage (Note 4)	SG2064/2066	I_C = 100mA, V_{IN} = 0.4V	35			V
	SG2065/2067	I_C = 100mA, V_{IN} = 0.4V	50			V
Collector-Emitter Saturation Voltage	All	I_C = 500mA, I_B = 625µA			1.1	V
		I_C = 750mA, I_B = 935µA			1.2	V
		I_C = 1.0A, I_B = 1.25mA			1.3	V
	SG2064/2066	I_C = 1.25A, I_B = 2.0mA			1.4	V
	SG2065/2067	I_C = 1.5A, I_B = 2.25mA			1.5	V
Input Current	SG2064/2065	V_{IN} = 2.4V	1.4		4.3	mA
		V_{IN} = 3.75V	3.3		9.6	mA
	SG2066/2067	V_{IN} = 5.0V	0.6		1.8	mA
		V_{IN} = 12V	1.7		5.2	mA

Note 4. These parameters, although guaranteed, are not tested in production.

ELECTRICAL SPECIFICATIONS (continued)

SG2064 thru SG2067

Parameter	Applicable Devices	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Input Voltage	SG2064/2065	V_{CE} = 2V, I_C = 1.0A			2.0	V
		V_{CE} = 2V, I_C = 1.5A			2.5	V
	SG2066/2067	V_{CE} = 2V, I_C = 1.0A			6.5	V
		V_{CE} = 2V, I_C = 1.5A			10	V
Turn-On Delay (Note 4)	All	0.5 E_{IN} to 0.5 E_{OUT}			1.0	µs
Turn-Off Delay	All	0.5 E_{IN} to 0.5 E_{OUT}			1.5	µs
Clamp Diode Leakage (Note 4) Current	SG2064/2066	V_R = 50V			50	µA
		V_R = 50V, T_A = T_{MAX}			100	µA
	SG2065/2067	V_R = 80V			50	µA
		V_R = 80V, T_A = T_{MAX}			100	µA
Clamp Diode Forward Voltage	All	I_F = 1.0A			1.75	V
		I_F = 1.5A			2.0	V

SG2068 thru SG2071

Parameter	Applicable Devices	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Leakage Current	SG2068/2070	V_{CE} = 50V			100	µA
		V_{CE} = 50V, T_A = T_{MAX}			500	µA
	SG2069/2071	V_{CE} = 80V			100	µA
		V_{CE} = 80V, T_A = T_{MAX}			500	µA
Output Sustaining Voltage (Note 4)	SG2068/2070	I_C = 100mA, V_{IN} = 0.4V	35			V
	SG2069/2071	I_C = 100mA, V_{IN} = 0.4V	50			V
Collector-Emitter Saturation Voltage	SG2068/2069	I_C = 500mA, V_{IN} = 2.75V			1.1	V
		I_C = 750mA, V_{IN} = 2.75V			1.2	V
		I_C = 1.0A, V_{IN} = 2.75V			1.3	V
		I_C = 1.25A, V_{IN} = 2.75V			1.4	V
	SG2069	I_C = 1.5A, V_{IN} = 2.75V			1.5	V
	SG2070/2071	I_C = 500mA, V_{IN} = 5.0V			1.1	V
		I_C = 750mA, V_{IN} = 5.0V			1.2	V
		I_C = 1.0A, V_{IN} = 5.0V			1.3	V
		I_C = 1.25A, V_{IN} = 5.0V			1.4	V
	SG2071	I_C = 1.5A, V_{IN} = 5.0V			1.5	V
Input Current	SG2068/2069	V_{IN} = 2.75V			550	µA
		V_{IN} = 3.75V			1000	µA
	SG2070/2071	V_{IN} = 5.0V			400	µA
		V_{IN} = 12V			1250	µA
Input Voltage	SG2068/2069	V_{CE} = 2V, I_C = 1.5A			2.75	V
	SG2070/2071	V_{CE} = 2V, I_C = 1.5A			5.0	V
Supply Current	SG2068/2069	I_C = 500mA, V_{IN} = 2.4V			6.0	mA
	SG2070/2071	I_C = 500mA, V_{IN} = 5.0V			4.5	mA
Turn-On Delay (Note 4)	All	0.5 E_{IN} to 0.5 E_{OUT}			1.0	µs
Turn-Off Delay (Note 4)	All	0.5 E_{IN} to 0.5 E_{OUT}			1.5	µs
Clamp Diode Leakage Current	SG2068/2070	V_R = 50V			50	µA
		V_R = 50V, T_A = T_{MAX}			100	µA
	SG2069/2071	V_R = 80V			50	µA
		V_R = 80V, T_A = T_{MAX}			100	µA
Clamp Diode Forward Voltage	All	I_F = 1.0A			1.75	V
		I_F = 1.5A			2.0	V

ELECTRICAL SPECIFICATIONS (continued)

SG2074 thru SG2077

Parameter	Applicable Devices	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Leakage Current	SG2074/2076	V_{CE} = 50V			100	µA
		V_{CE} = 50V, $T_A = T_{MAX}$			500	µA
	SG2075/2077	V_{CE} = 80V			100	µA
		V_{CE} = 80V, $T_A = T_{MAX}$			500	µA
Output Sustaining Voltage (Note 4)	SG2074/2076	I_C = 100mA, V_{IN} = 0.4V	35			V
	SG2075/2077	I_C = 100mA, V_{IN} = 0.4V	50			V
Collector-Emitter Saturation Voltage	All	I_C = 500mA, I_B = 625µA			1.1	V
		I_C = 750mA, I_B = 935µA			1.2	V
		I_C = 1.0A, I_B = 1.25mA			1.3	V
	SG2074/2076	I_C = 1.25A, I_B = 2.0mA			1.4	V
	SG2075/2077	I_C = 1.5A, I_B = 2.25mA			1.5	V
Input Current	SG2074/2075	V_{IN} = 2.4V	2.0		4.3	mA
		V_{IN} = 3.75V	4.5		9.6	mA
	SG2076/2077	V_{IN} = 5.0V	0.9		1.8	mA
		V_{IN} = 12V	2.75		5.2	mA
Input Voltage	SG2074/2075	V_{CE} = 2V, I_C = 1.0A			2.0	V
		V_{CE} = 2V, I_C = 1.5A			2.5	V
	SG2076/2077	V_{CE} = 2V, I_C = 1.0A			6.5	V
		V_{CE} = 2V, I_C = 1.5A			10	V
Turn-On Delay (Note 4)	All	0.5 E_{IN} to 0.5 E_{OUT}			1.0	µs
Turn-Off Delay (Note 4)	All	0.5 E_{IN} to 0.5 E_{OUT}			1.5	µs

CHARACTERISTIC CURVES

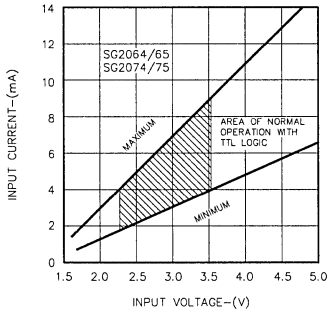


FIGURE 1.
LOGIC INPUT CURRENT VS. INPUT VOLTAGE—
5V LOGIC

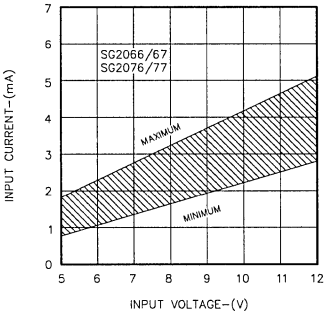


FIGURE 2.
LOGIC INPUT CURRENT VS. INPUT VOLTAGE —
HIGH LEVEL LOGIC

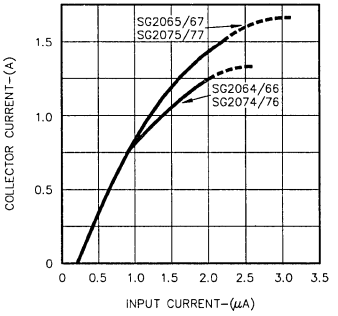


FIGURE 3.
MAXIMUM REQUIRED LOGIC INPUT CURRENT
VS. COLLECTOR CURRENT

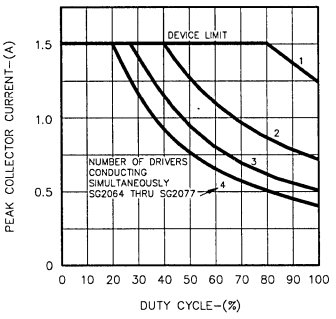
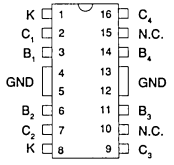
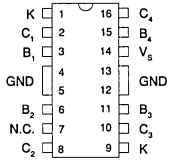
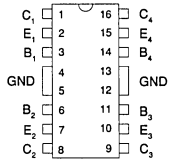
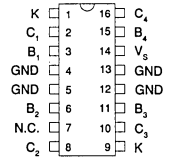
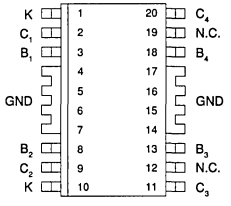
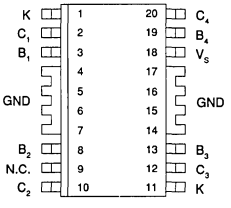


FIGURE 4.
PEAK ALLOWABLE COLLECTOR CURRENT
VS. DUTY CYCLE AT T_A = 70°C

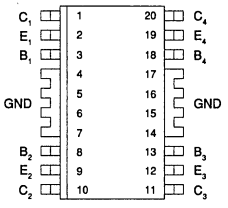
CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN PLASTIC BATWING W - PACKAGE	SG2064W SG2065W SG2066W SG2067W	0°C to 70°C 0°C to 70°C 0°C to 70°C 0°C to 70°C	
16-PIN PLASTIC BATWING W - PACKAGE	SG2068W SG2069W SG2070W SG2071W	0°C to 70°C 0°C to 70°C 0°C to 70°C 0°C to 70°C	
16-PIN PLASTIC BATWING W - PACKAGE	SG2074W SG2075W SG2076W SG2077W	0°C to 70°C 0°C to 70°C 0°C to 70°C 0°C to 70°C	
16-PIN SIDE-BRAZED DIP H - PACKAGE	SG2069H/883B SG2069H	-55°C to 125°C -55°C to 125°C	
20-PIN PLASTIC BATWING S.O.I.C. DWW - PACKAGE	SG2064DWW SG2065DWW SG2066DWW SG2067DWW	0°C to 70°C 0°C to 70°C 0°C to 70°C 0°C to 70°C	
20-PIN PLASTIC BATWING S.O.I.C. DWW - PACKAGE	SG2068DWW SG2069DWW SG2070DWW SG2071DWW	0°C to 70°C 0°C to 70°C 0°C to 70°C 0°C to 70°C	

Note 1. Contact factory for JAN and DESC product availability.
2. All parts are viewed from the top.
3. See selection guide for specific device types.

6

CONNECTION DIAGRAMS & ORDERING INFORMATION (continued)

Package	Part No.	Ambient Temperature Range	Connection Diagram
20-PIN PLASTIC BATWING S.O.I.C. DWW - PACKAGE	SG2074DWW SG2075DWW SG2076DWW SG2077DWW	0°C to 70°C 0°C to 70°C 0°C to 70°C 0°C to 70°C	

SELECTION GUIDE

Device	V_{CEX} Max	$V_{CE(SUS)}$ Max	V_{IN} Max	Logic Inputs
SG2064	50V	35V	15V	TTL, DTL, Schottky TTL, 5V CMOS and NMOS
SG2065	80V	50V	15V	
SG2066	50V	35V	30V	6V to 15V CMOS and PMOS
SG2067	80V	50V	30V	
SG2068	50V	35V	15V	TTL, DTL, Schottky TTL, 5V CMOS amd NMOS
SG2069	80V	50V	15V	
SG2070	50V	35V	30V	6V to 15V CMOS and PMOS
SG2071	80V	50V	30V	
SG2074	50V	35V	30V	General Purpose
SG2075	80V	50V	60V	
SG2076	50V	35V	30V	6V to 15V CMOS and PMOS
SG2077	80V	50V	60V	

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

HIGH VOLTAGE MEDIUM CURRENT DRIVER ARRAYS

DESCRIPTION

The SG2800 series integrates eight NPN Darlington pairs with internal suppression diodes to drive lamps, relays, and solenoids in many military, aerospace, and industrial applications that require severe environments. All units feature open collector outputs with greater than 50V breakdown voltages combined with 500mA current carrying capabilities. Five different input configurations provide optimized designs for interfacing with DTL, TTL, PMOS, or CMOS drive signals. These devices are designed to operate from -55°C to 125°C ambient temperature in a 18-pin dual in-line ceramic (J) package and 20-pin leadless chip carrier (LCC).

FEATURES

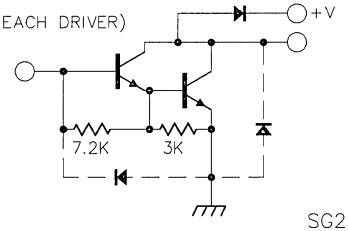
- **Eight NPN Darlington pairs**
- **Collector currents to 600mA**
- **Output voltages from 50V to 95V**
- **Internal clamping diodes for inductive loads**
- **DTL, TTL, PMOS, or CMOS compatible inputs**
- **Hermetic ceramic package**

HIGH RELIABILITY FEATURES

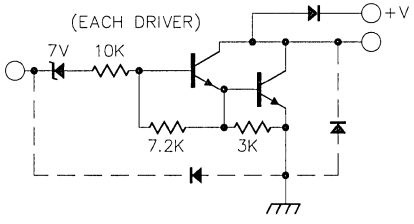
- **Available to MIL-STD-883 and DESC SMD**
- **MIL-M38510/14106BVA - JAN2801J**
- **MIL-M38510/14107BVA - JAN2802J**
- **MIL-M38510/14108BVA - JAN2803J**
- **MIL-M38510/14109BVA - JAN2804J**
- **MIL-M38510/14110BVA - JAN2805J**
- **Radiation data available**
- **SG level "S" processing available**

PARTIAL SCHEMATICS

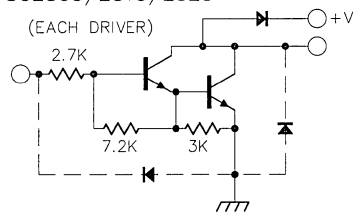
SG2801/2811/2821



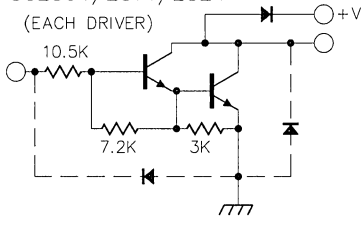
SG2802/2812/2822



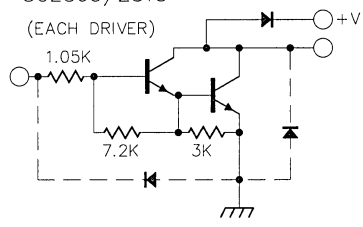
SG2803/2813/2823



SG2804/2814/2824



SG2805/2815



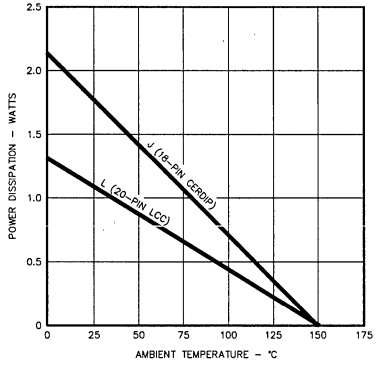
ABSOLUTE MAXIMUM RATINGS (Note 1)

Output Voltage, V_{CE}
(SG2800, 2810 series) 50V
(SG2820 series) 95V
Input Voltage, V_{IN}
(SG2802,3,4 series) 30V
(SG2805 series) 15V
Continuous Input Current, I_{IN} 25mA

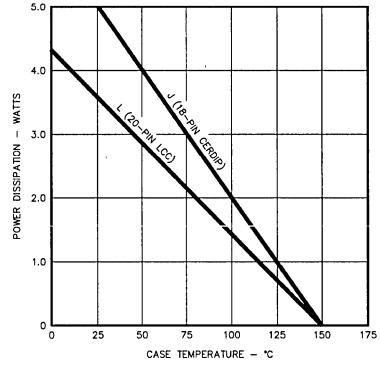
Continuous Collector Current, I_C
(SG2800, 2820) 500mA
(SG2810) 600mA
Operating Junction Temperature
Hermetic (J, L Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering 10 sec.) ..... 300°C

Note 1. Values beyond which damage may occur.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Output Voltage, V_{CE}
SG2800, SG2820 series 50V
SG2810 series 95V

Peak Collector Current, I_C
SG2800, SG2820 series 350mA
SG2810 series 500mA
Operating Ambient Temperature Range .....-55°C to 125°C

Note 2. Range over which the device is functional.

SELECTION GUIDE

Device	V_{CE} Max	I_C Max	Logic Inputs
SG2801	50V	500mA	General Purpose PMOS, CMOS
SG2802	50V	500mA	14V-25V PMOS
SG2803	50V	500mA	5V TTL, CMOS
SG2804	50V	500mA	6V-15V CMOS, PMOS
SG2805	50V	500mA	High Output TTL
SG2811	50V	600mA	General Purpose PMOS, CMOS
SG2812	50V	600mA	14V-25V PMOS

Device	V_{CE} Max	I_C Max	Logic Inputs
SG2813	50V	600mA	5V TTL, CMOS
SG2814	50V	600mA	6V-15V CMOS, PMOS
SG2815	50V	600mA	High Output TTL
SG2821	95V	500mA	General Purpose PMOS, CMOS
SG2822	95V	500mA	14V-25V PMOS
SG2823	95V	500mA	5V TTL, CMOS
SG2824	95V	500mA	6V-15V CMOS, PMOS

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures of -55°C ≤ T_A ≤ 125°C. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

SG2801 thru SG2805

Parameter	Applicable Devices	Temp.	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Output Leakage Current (I_{CEX})	All		V_{CE} = 50V			100	µA
	SG2802		V_{CE} = 50V, V_{IN} = 6V			500	µA
	SG2804		V_{CE} = 50V, V_{IN} = 1V			500	µA
Collector - Emitter ($V_{CE(SAT)}$)	All	$T_A = T_{MIN}$	I_C = 350mA, I_B = 850µA		1.6	1.8	V
		$T_A = T_{MIN}$	I_C = 200mA, I_B = 550µA		1.3	1.5	V
		$T_A = T_{MIN}$	I_C = 100mA, I_B = 350µA		1.1	1.3	V
		T_A = 25°C	I_C = 350mA, I_B = 500µA		1.25	1.6	V
		T_A = 25°C	I_C = 200mA, I_B = 350µA		1.1	1.3	V
		T_A = 25°C	I_C = 100mA, I_B = 250µA		0.9	1.1	V
		$T_A = T_{MAX}$	I_C = 350mA, I_B = 500µA		1.6	1.8	V
		$T_A = T_{MAX}$	I_C = 200mA, I_B = 350µA		1.3	1.5	V
		$T_A = T_{MAX}$	I_C = 100mA, I_B = 250µA		1.1	1.3	V
Input Current ($I_{IN(ON)}$)	SG2802		V_{IN} = 17V	480	850	1300	µA
	SG2803		V_{IN} = 3.85V	650	930	1350	µA
	SG2804		V_{IN} = 5V	240	350	500	µA
			V_{IN} = 12V	650	1000	1450	µA
	SG2805		V_{IN} = 3V	1180	1500	2400	µA
($I_{IN(OFF)}$)	All	$T_A = T_{MAX}$	I_C = 500µA	25	50		µA
Input Voltage ($V_{IN(ON)}$)	SG2802	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 300mA			18	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 300mA			13	V
	SG2803	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 200mA			3.3	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 250mA			3.6	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 300mA			3.9	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 200mA			2.4	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 250mA			2.7	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 300mA			3.0	V
	SG2804	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 125mA			6.0	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 200mA			8.0	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 275mA			10	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 350mA			12	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 125mA			5.0	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 200mA			6.0	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 275mA			7.0	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 350mA			8.0	V
	SG2805	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 350mA			3.0	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 350mA			2.4	V
D-C Forward Current	SG2801	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 350mA	500			
Transfer Ratio (h_{FE})		T_A = 25°C	V_{CE} = 2V, I_C = 350mA	1000			
Input Capacitance (C_{IN}) (Note 3)	All	T_A = 25°C			15	25	pF
Turn-On Delay (TPLH)	All	T_A = 25°C	0.5 E_{IN} to 0.5 E_{OUT}		250	1000	ns
Turn-Off Delay (TPHL)	All	T_A = 25°C	0.5 E_{IN} to 0.5 E_{OUT}		250	1000	ns
Clamp Diode Leakage Current (I_R)	All		V_R = 50V			50	µA
Clamp Diode Forward Voltage (V_F)	All		I_F = 350mA		1.7	2.0	V

Note 3. These parameters, although guaranteed, are not tested in production.

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ELECTRICAL SPECIFICATIONS (continued)

SG2811 thru SG2815

Parameter	Applicable Devices	Temp.	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Output Leakage Current (I_{CEX})	All		V_{CE} = 50V			100	µA
	SG2812		V_{CE} = 50V, V_{IN} = 6V			500	µA
	SG2814		V_{CE} = 50V, V_{IN} = 1V			500	µA
Collector - Emitter ($V_{CE(SAT)}$)	All	$T_A = T_{MIN}$	I_C = 500mA, I_B = 1100µA		1.8	2.1	V
		$T_A = T_{MIN}$	I_C = 350mA, I_B = 850µA		1.6	1.8	V
		$T_A = T_{MIN}$	I_C = 200mA, I_B = 550µA		1.3	1.5	V
		T_A = 25°C	I_C = 500mA, I_B = 600µA		1.7	1.9	V
		T_A = 25°C	I_C = 350mA, I_B = 500µA		1.25	1.6	V
		T_A = 25°C	I_C = 200mA, I_B = 350µA		1.1	1.3	V
		$T_A = T_{MAX}$	I_C = 500mA, I_B = 600µA		1.8	2.1	V
		$T_A = T_{MAX}$	I_C = 350mA, I_B = 500µA		1.6	1.8	V
		$T_A = T_{MAX}$	I_C = 200mA, I_B = 350µA		1.3	1.5	V
Input Current ($I_{IN(ON)}$)	SG2812		V_{IN} = 17V	480	850	1300	µA
	SG2813		V_{IN} = 3.85V	650	930	1350	µA
	SG2814		V_{IN} = 5V	240	350	500	µA
			V_{IN} = 12V	650	1000	1450	µA
	SG2815		V_{IN} = 3V	1180	1500	2400	µA
($I_{IN(OFF)}$)	All	$T_A = T_{MAX}$	I_C = 500µA	25	50		µA
Input Voltage ($V_{IN(ON)}$)	SG2812	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 500mA			23.5	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 500mA			17	V
	SG2813	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 250mA			3.6	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 300mA			3.9	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 500mA			6.0	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 250mA			2.7	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 300mA			3.0	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 500mA			3.5	V
	SG2814	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 275mA			10	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 350mA			12	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 500mA			17	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 275mA			7.0	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 350mA			8.0	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 500mA			9.5	V
	SG2815	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 350mA			3.0	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 500mA			3.5	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 350mA			2.4	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 500mA			2.6	V
D-C Forward Current	SG2811	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 500mA	450			
Transfer Ratio (h_{FE})		T_A = 25°C	V_{CE} = 2V, I_C = 500mA	900			
Input Capacitance (C_{IN}) (Note 3)	All	T_A = 25°C			15	25	pF
Turn-On Delay (TPLH)	All	T_A = 25°C	0.5 E_{IN} to 0.5 E_{OUT}		250	1000	ns
Turn-Off Delay (TPHL)	All	T_A = 25°C	0.5 E_{IN} to 0.5 E_{OUT}		250	1000	ns
Clamp Diode Leakage Current (I_R)	All		V_R = 50V			50	µA
Clamp Diode Forward Voltage (V_F)	All		I_F = 350mA		1.7	2.0	V
			I_F = 500mA			2.5	V

Note 3. These parameters, although guaranteed, are not tested in production.

ELECTRICAL SPECIFICATIONS (continued)

SG2821 thru SG2824

Parameter	Applicable Devices	Temp.	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Output Leakage Current (I_{CEX})	All		V_{CE} = 95V			100	µA
	SG2822		V_{CE} = 95V, V_{IN} = 6V			500	µA
	SG2824		V_{CE} = 95V, V_{IN} = 1V			500	µA
Collector - Emitter ($V_{CE(SAT)}$)	All	$T_A = T_{MIN}$	I_C = 350mA, I_B = 850µA		1.6	1.8	V
		$T_A = T_{MIN}$	I_C = 200mA, I_B = 550µA		1.3	1.5	V
		$T_A = T_{MIN}$	I_C = 100mA, I_B = 350µA		1.1	1.3	V
		T_A = 25°C	I_C = 350mA, I_B = 500µA		1.25	1.6	V
		T_A = 25°C	I_C = 200mA, I_B = 350µA		1.1	1.3	V
		T_A = 25°C	I_C = 100mA, I_B = 250µA		0.9	1.1	V
		$T_A = T_{MAX}$	I_C = 350mA, I_B = 500µA		1.6	1.8	V
		$T_A = T_{MAX}$	I_C = 200mA, I_B = 350µA		1.3	1.5	V
		$T_A = T_{MAX}$	I_C = 100mA, I_B = 250µA		1.1	1.3	V
Input Current ($I_{IN(ON)}$)	SG2822		V_{IN} = 17V	480	850	1300	µA
	SG2823		V_{IN} = 3.85V	650	930	1350	µA
	SG2824		V_{IN} = 5V	240	350	500	µA
			V_{IN} = 12V	650	1000	1450	µA
($I_{IN(OFF)}$)	All	$T_A = T_{MAX}$	I_C = 500µA	25	50		µA
Input Voltage ($V_{IN(ON)}$)	SG2822	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 300mA			18	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 300mA			13	V
	SG2823	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 200mA			3.3	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 250mA			3.6	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 300mA			3.9	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 200mA			2.4	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 250mA			2.7	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 300mA			3.0	V
	SG2824	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 125mA			6.0	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 200mA			8.0	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 275mA			10	V
		$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 350mA			12	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 125mA			5.0	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 200mA			6.0	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 275mA			7.0	V
		$T_A = T_{MAX}$	V_{CE} = 2V, I_C = 350mA			8.0	V
D-C Forward Current	SG2821	$T_A = T_{MIN}$	V_{CE} = 2V, I_C = 350mA	500			
Transfer Ratio (h_{FE})		T_A = 25°C	V_{CE} = 2V, I_C = 350mA	1000			
Input Capacitance (C_{IN}) (Note 3)	All	T_A = 25°C			15	25	pF
Turn-On Delay (TPLH)	All	T_A = 25°C	0.5 E_{IN} to 0.5 E_{OUT}		250	1000	ns
Turn-Off Delay (TPHL)	All	T_A = 25°C	0.5 E_{IN} to 0.5 E_{OUT}		250	1000	ns
Clamp Diode Leakage Current (I_R)	All		V_R = 95V			50	µA
Clamp Diode Forward Voltage (V_F)	All		I_F = 350mA		1.7	2.0	V

Note 3. These parameters, although guaranteed, are not tested in production.

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CHARACTERISTIC CURVES

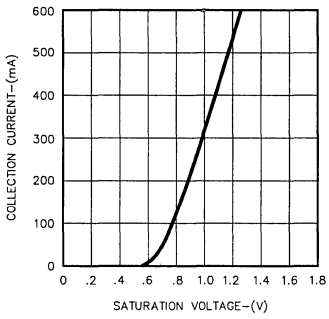


FIGURE 1.
OUTPUT CHARACTERISTICS

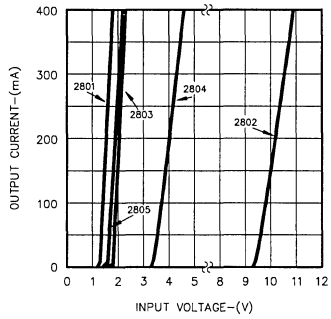


FIGURE 2.
OUTPUT CURRENT VS. INPUT VOLTAGE

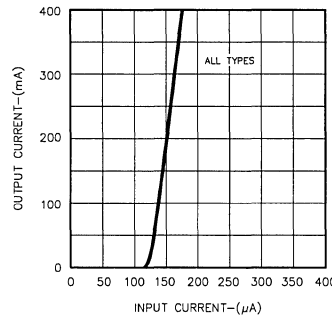


FIGURE 3.
OUTPUT CURRENT VS. INPUT CURRENT

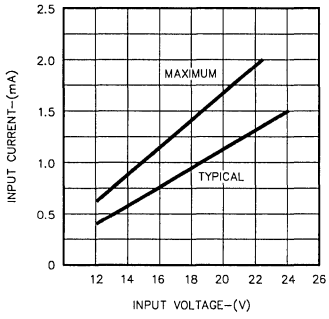


FIGURE 4.
INPUT CHARACTERISTICS - SG2802

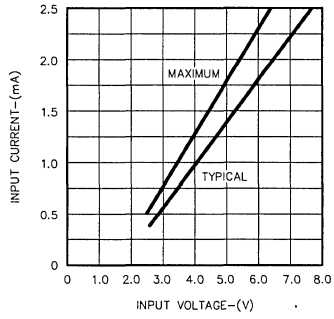


FIGURE 5.
INPUT CHARACTERISTICS - SG2803

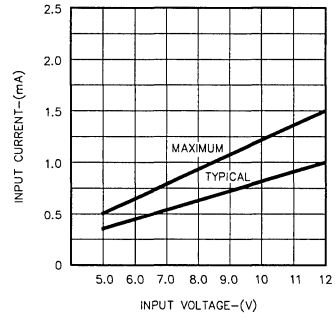


FIGURE 6.
INPUT CHARACTERISTICS - SG2804

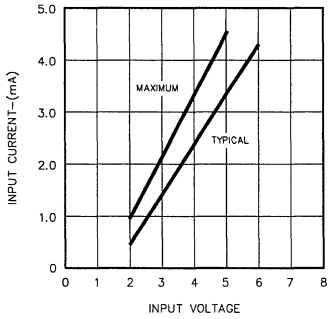


FIGURE 7.
INPUT CHARACTERISTICS - SG2805

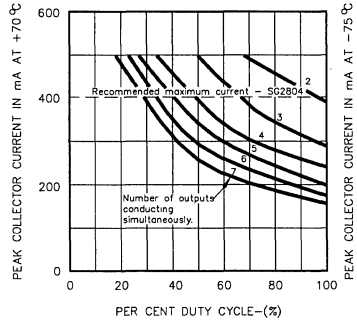
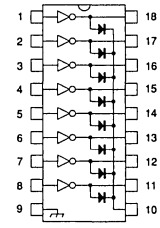
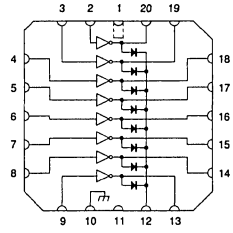


FIGURE 8.
PEAK COLLECTOR CURRENT VS. DUTY CYCLE

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No. (Note 3)	Ambient Temperature Range	Connection Diagram
18-PIN CERAMIC DIP J - PACKAGE	SG28XXJ/883B SG28XXJ	-55°C to 125°C -55°C to 125°C	
20-PIN CERAMIC LEADLESS CHIP CARRIER L- PACKAGE	SG28XXL/883B SG28XXL	-55°C to 125°C -55°C to 125°C	

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Note 1. Contact factory for JAN and DESC product availability.
2. All parts are viewed from the top.
3. See Selection Guide for specific device types.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SG5792

ADVANCED DATA SHEET

QUAD PIN DIODE DRIVER

DESCRIPTION

This monolithic multiple high-voltage inverting switch is designed to interface between low level digital logic and high-voltage PIN diodes. Each driver stage is self-contained and protected against diode shorts, requiring only a single resistor for determining diode forward current. Reverse operation provides high transient switching current capability for fast diode turnoff. Forward operation is effected when the input is pulled high.

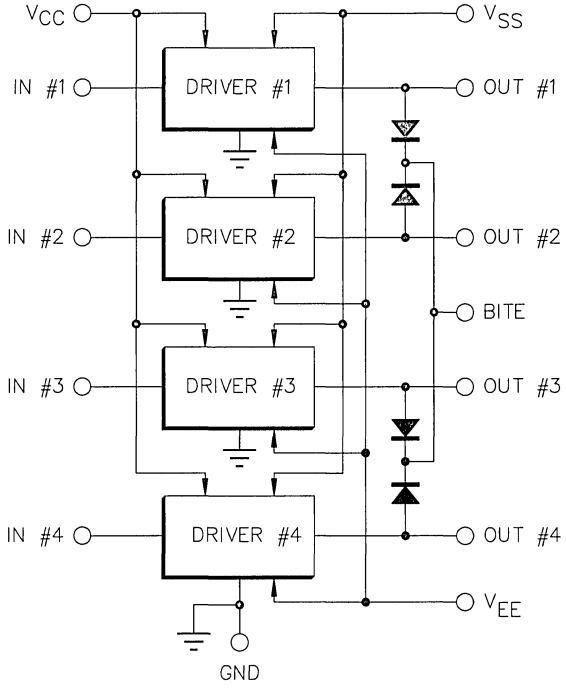
FEATURES

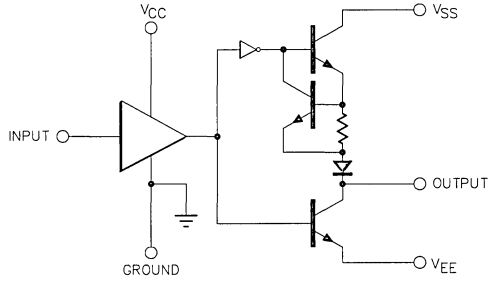
- **Four independent PIN diode drivers**
- **50 volts reverse bias**
- **300mA forward current**
- **Fast diode turnoff**
- **Shorted diode protection**
- **Compatible with most logic families**
- **For 85V or 125V devices contact factory**

HIGH RELIABILITY FEATURES - SG5792

- ◊ **Available to MIL-STD-883**
- ◊ **SG level "S" processing available**

BLOCK DIAGRAM





(each driver)

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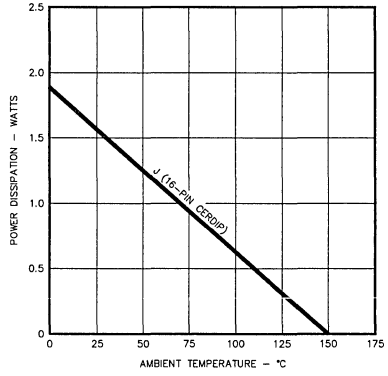
April 1990

ABSOLUTE MAXIMUM RATINGS (Note 1)

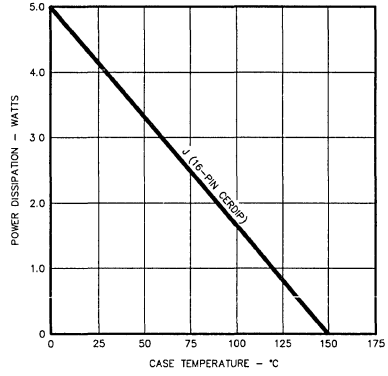
Supply Voltage (V_{CC}) 6.0V
Supply Voltage (V_{EE}) ..... -5.0V
Supply Voltage (V_{SS}) 60V
Operating Voltage (V_{CC} - V_{EE}) 9.5V
Sink Current (I_{ON}) 500mA
Operating Case Temperature (T_C)
Hermetic (J Package) ..... 150°C
Storage Temperature Range ..... -65°C to +150°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage (V_{CC}) ..... 4.5V to 5.5V
Supply Voltage (V_{EE}) ..... -2.0V to -4.0V
Supply Voltage (V_{SS}) ..... V_{CC} to 50V
Operating Voltage (V_{SS} - V_{EE}) 54V
Operating Ambient Temperature Range
SG5792 ..... -55°C to 125°C
Current into any output (ON state) ..... 300mA (Note 3)

Note 2. Range over which the device is functional.
Note 3. 300mA into four driver outputs at T_A= 125°C. See Thermal Characteristics

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating operating temperatures for SG5792 with -55°C ≤ T_A ≤ 125°C, V_{CC} = 4.5V, V_{EE} = -3.0V, and V_{SS} = 50V. All measurements are taken one driver at a time. Output open, unless otherwise specified. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG5792			Units
		Min.	Typ.	Max.	
Static Section					
Input Voltage High (V_{IH}) (Note 4)		2.0		5.5	V
Input Voltage Low (V_{IL}) (Note 4)				0.8	V
Input Current Low (I_{IL}) (Note 4)	V_{CC} = 5.5V, V_{IN} = 0.4V			1.0	mA
Input Current High (I_{IH}) (Note 4)	V_{CC} = 5.5V, V_{IN} = 5.0V	50			µA
Output Voltage Low (V_{OL}) (Note 5)	T_A = -55°C, V_{IN} = 2.4V, I_O = 300mA			0.85	V
	T_A = 125°C, V_{EE} = -2.0V, V_{IN} = 2.4V, I_O = 300mA			1.0	V
	T_A = 25°C, V_{EE} = -2.0V, V_{IN} = 2.4V, I_O = 300mA			0.85	V
	T_A = -55°C, V_{IN} = 2.4V, I_O = 150mA			0.5	V
	T_A = 125°C, V_{EE} = -2.0V, V_{IN} = 2.4V, I_O = 150mA			0.6	V
	T_A = 25°C, V_{EE} = -2.0V, V_{IN} = 2.4V, I_O = 150mA			0.5	V
V_{CC} Supply Current - input high ($I_{CC(1)}$) (Note 4)	V_{CC} = 5.5V, V_{EE} = -4.0V, V_{IN} = 2.4V, Total 4 drivers. No load		34	52	mA
V_{CC} Supply Current - input low ($I_{CC(0)}$) (Note 4)	V_{CC} = 5.5V, V_{EE} = -4.0V, V_{IN} = 0.4V, Total 4 drivers. No load		30	40	mA
V_{EE} Supply Current - input low ($I_{EE(0)}$)	V_{CC} = 5.0V, V_{IN} = 0.4V		20		mA
V_{EE} Supply Current - input high ($I_{EE(1)}$)	V_{CC} = 5.0V, V_{IN} = 2.4V		120		mA

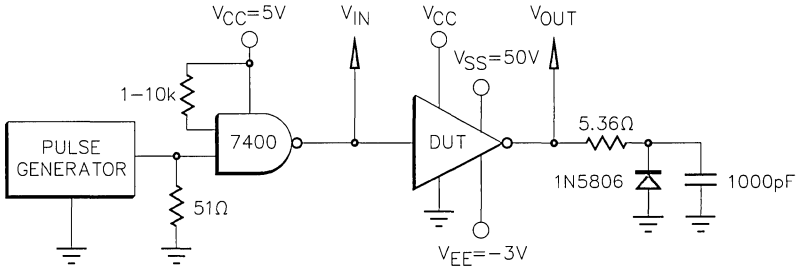
ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG5792 Min.	SG5792 Typ.	SG5792 Max.	Units
Static Section (conitnued)					
Output Short Circuit Current (I_{OS})	V_{IN} = 0.4V, V_{OUT} = 0V, V_{SS} =	25		60	mA
V_{SS} Supply Current (I_{SS})	T_A = 25°C, V_{IN} = 2.4V		2.5	4.0	mA
	T_A = 25°C, V_{IN} = 0.4V		10	100	µA
	T_A = 125°C, V_{IN} = 2.4V			4.0	mA
	T_A = 125°C, V_{IN} = 0.4V			200	µA
V_{SS} Supply Current ($I_{SS(SC)}$)	T_A = 25°C, V_{IN} = 0.4V, V_{OUT} = 0V	1.0	3.25	4.0	mA
Output Voltage High (V_{OH})	V_{IN} = 0.4V, I_O = 0.5mA	45			V
Bite Diodes Reverse Breakdown Voltage (P_{IV})	T_A = 125°C	55			V
(Note 6 & 8)	T_A = 25°C	55			V
Bite Diodes Forward Voltage Drop (V_F)	T_A = 125°C			0.8	V
(Note 7 & 8)	T_A = 25°C			1.0	V

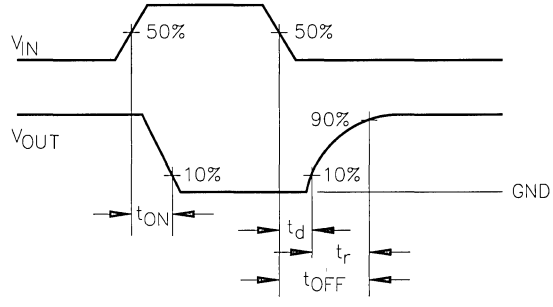
Parameter	Test Conditions	SG5792 Min.	SG5792 Typ.	SG5792 Max.	Units
Dynamic Section (See Figure 1)					
Turn-on Time (t_{ON}) (Note 9)				0.7	µs
Turn-off Time (t_{OFF}) (Note 9)				5	µs
Rise Time (t_r) (Note 9)				4	µs

Note 4. Each input.
Note 5. Reference V_{EE}
Note 6. Diode output force 10µA
Note 7. Diode output force -100µA
Note 8. V_{CC} = Open, V_{IN} = Open, V_{OUT} = 0V, V_{SS} = Open
Note 9. These tests, although guaranteed, are not tested in produc-

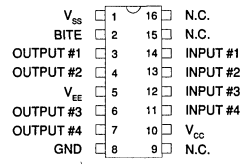
AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS - FIGURE 1



PULSE GENERATOR:
P_{RR}=25KHz
DUTY CYCLE = 0.5
$t_f = t_r \leq 7ns$



CONNECTION DIAGRAMS & ORDERING INFORMATION (See Note Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG5792J/883B SG5792J	-55°C to 125°C -55°C to 125°C	

Note 1. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SG5793

ADVANCED DATA SHEET

QUAD PIN DIODE DRIVER

DESCRIPTION

This monolithic pin diode driver circuit contains four outputs. Each of those is individually controlled by a logic input (HCMOS compatible). A precise current source constant over temperature is implemented, so that an accurate output current driving the pin diode can be obtained when the logic input is high. The circuit is capable of switching the pin diode voltage "on" or "off" fast after detecting and change from the input, it also has four independent polar voltage divider networks to provide an accurate indication of each diode voltage.

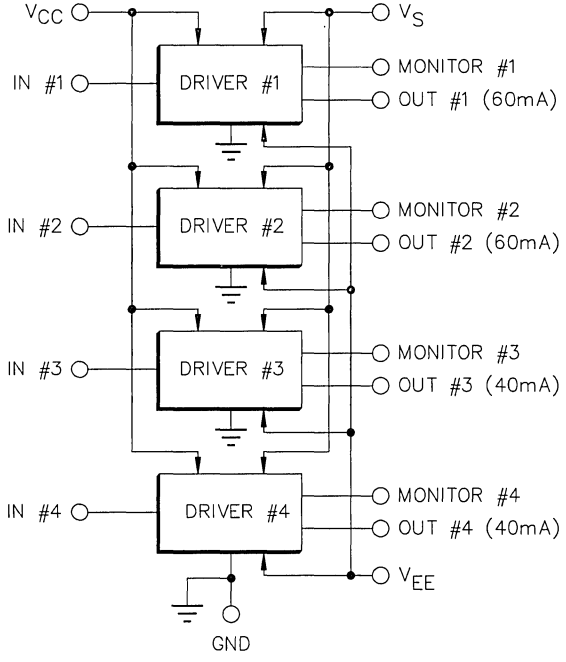
FEATURES

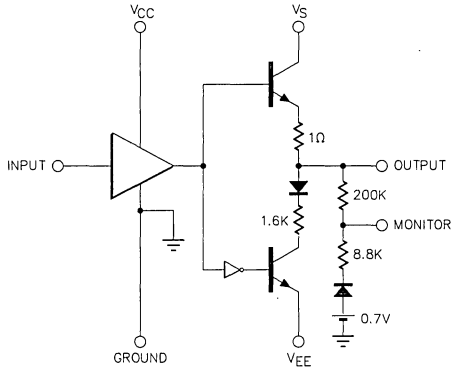
- **Four independent PIN drivers**
- **HCMOS compatible**
- **200mA forward current capability**
- **Fast ON or OFF diode switching time**
- **Accurate monitor output to indicate output voltage**
- **55 volts reverse bias**

HIGH RELIABILITY FEATURES - SG5793

- **Available to MIL-STD-883**

BLOCK DIAGRAM





(each driver)

6

April 1990

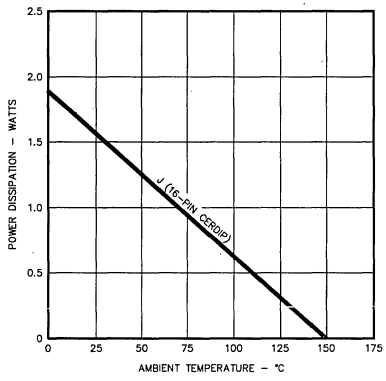
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V_{CC}) 7.0V
Supply Voltage (V_{EE}) ..... -65V
Supply Voltage (V_S) 2.0V

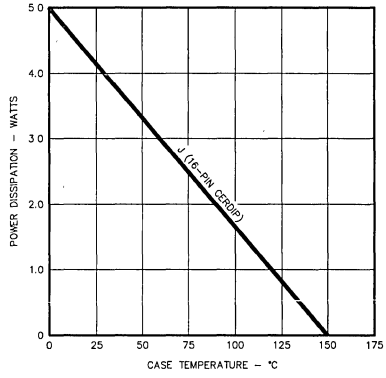
Operating Junction Temperature
Hermetic (J Package) ..... 150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage (V_{CC}) ..... 4.75V to 5.25V
Supply Voltage (V_{EE}) ..... -47.5V to -52.5V
Supply Voltage (V_S) ..... 1.45V to 1.55V

Operating Ambient Temperature Range
SG5793 ..... -55°C to 125°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG5793 with -55°C ≤ T_A ≤ 125°C, V_{CC} = 5.0V, V_{EE} = -50V, and V_S = 1.5V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

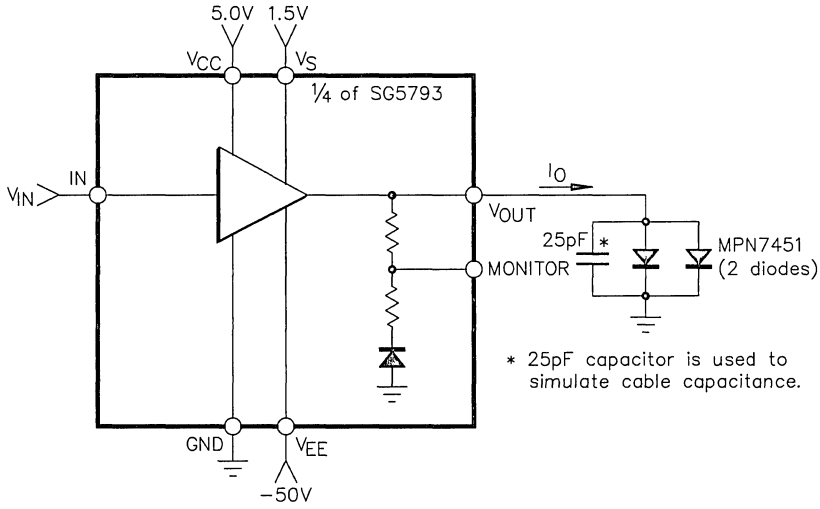
Parameter	Test Conditions	SG5793 Min.	SG5793 Typ.	SG5793 Max.	Units
Static Section					
Supply Currents	All four channels are active				
(I_{CC})	$V_{IN(1-4)}$ = 5.0V			10.0	mA
(I_{EE})	$V_{IN(1-4)}$ = 5.0V			-3.0	mA
(I_S)	$V_{IN(1-4)}$ = 5.0V			230	mA
Low Level Input Voltage (V_{IL})		-0.5	0	0.4	V
High Level Input Voltage (V_{IH})		3.15		5.5	V
Low Level Input Current (I_{IL})	V_{IN} = 0.4V			400	µA
High Level Input Current (I_{IH})	V_{IN} = 5.5V			400	µA
Low Level Output Voltage (V_{OL})	V_{CC} = 4.5V, V_{EE} = -45V, V_S = 1.4V, I_O = -500µA	-36		-55	V
High Level Output Current (I_{OH})					
Outputs 1 & 2	V_{OH} = 0.6V	54	60	66	mA
Outputs 3 & 4	V_{OH} = 0.6V	36	40	44	mA
Monitor Voltage					
Output High (V_{MH})	Same as for I_{OH}	99		102	$\%V_{OH}$
Output Low (V_{ML})	Same as for V_{OL}	5.25		3.25	$\%V_{OL}$

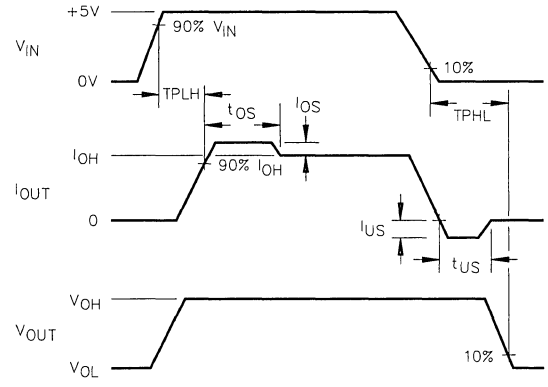
ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	SG5793 Min.	SG5793 Typ.	SG5793 Max.	Units
Dynamic Section (See Figure 1)					
Propagation Delay (TPLH) (Note 3)				5.0	µs
(TPHL) (Note 3)				5.0	µs
Forward Current Overshoot (I_{OS}) (Note 3)					
Outputs 1 & 2				60	mA
Outputs 3 & 4				40	mA
Overshoot Duration (t_{OS}) (Note 3)				3.0	µs
Reverse Current Undershoot (I_{US}) (Note 3)					
Outputs 1 & 2			-45	-60	mA
Outputs 3 & 4			-30	-40	mA
Undershoot Duration (t_{US}) (Note 3)				2.0	µs

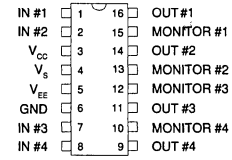
Note 3. Guaranteed by design but not 100% tested.

TEST CIRCUIT AND SWITCHING TIME WAVEFORMS - FIGURE 1





CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG5793J/883B SG5793J	-55°C to 125°C -55°C to 125°C	

Note: 1. All packages are viewed from the top.

DUAL PERIPHERAL POSITIVE-AND DRIVER

DESCRIPTION

The SG55450B/SG55460/SG55470 (SG75450B/SG75460/SG75470) series of dual peripheral Positive-AND drivers are a family of versatile devices designed for use in systems that employ TTL or DTL logic. This family of drivers are direct replacements for the Texas Instruments SN55450B/60/70 (SN75450B/60/70) series. Diode-clamped inputs simplify circuit design. Typical applications include high-speed logic buffers, power drivers, relay drivers, MOS drivers, line drivers, and memory drivers. These parts are unique general-purpose devices each featuring two standard Series 54/74 TTL gates and two uncommitted, high-current, high-voltage n-p-n transistors and offer the system designer the flexibility of tailoring the circuit to the application. The SG55450B/SG55460/SG55470 drivers are characterized for operation over the full military ambient temperature range of -55°C to 125°C and the SG75450B/SG75460/SG75470 drivers are characterized for operation from 0°C to 70°C

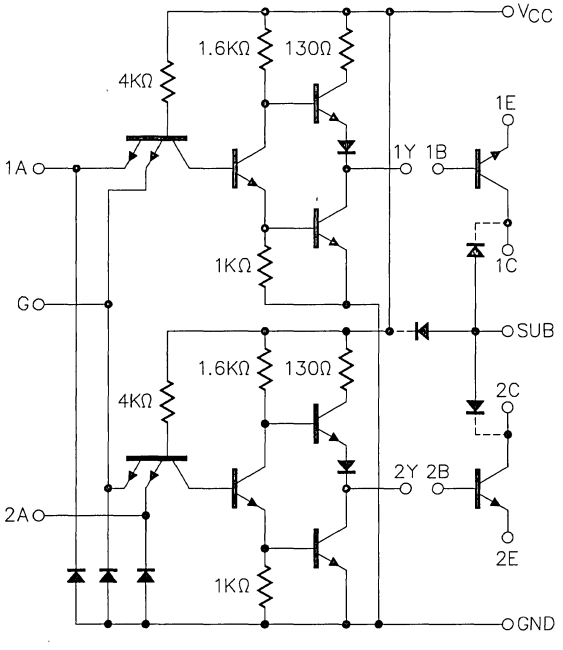
FEATURES

- **300mA output current capability**
- **High-voltage output**
- **No output latch-up at 20V**
- **High speed switching**
- **TTL or DTL compatible diode-clamped inputs**
- **Standard supply voltages**

HIGH RELIABILITY FEATURES
- SG55450B/SG55460/SG55470

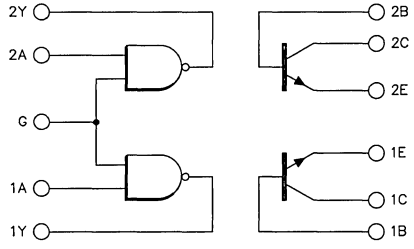
- **Available to MIL-STD-883**
- **Scheduled for MIL-M-38510 QPL listing**
- **SG level "S"processing available**

EQUIVALENT CIRCUIT SCHEMATIC



BLOCK DIAGRAM

Positive Logic: Y = $\overline{AG}$ (gate only)
C = AG (gate and transistor)



FUNCTION TABLE (each gate)

A	G	Y
L	L	H (off-state)
L	H	H (off-state)
H	L	H (off-state)
H	H	L (on-state)

H = High Level, L = Low Level

ABSOLUTE MAXIMUM RATINGS (Note 1)

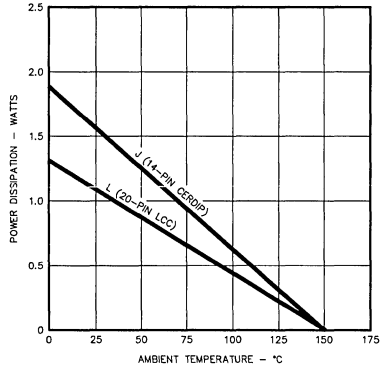
Supply Voltage (V_{CC}) 7V
Input Voltage 5.5V
Interemitter Voltage (Note 2) 5.5V
Emitter-base Voltage 5V
Output Current 400mA
Operating Junction Temperature
Hermetic (J, L Packages) ..... 150°C

Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (soldering 60 sec.) ..... 300°C

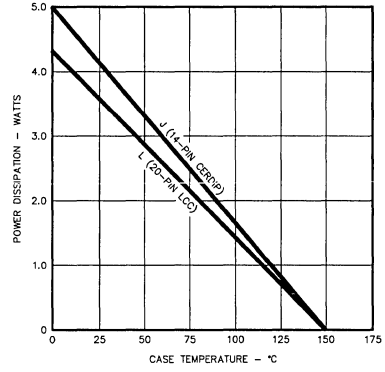
	XX450B Series	XX460 Series	XX470 Series
V_{CC}-to-substrate Voltage	35V	40V	70V
Collector-to-substrate Voltage	35V	40V	70V
Collector base Voltage	35V	40V	70V
Collector-emitter Voltage (Note 3).....	35V	40V	70V

Note 1. Exceeding these ratings could cause damage to the device.
Note 2. Voltage between two emitters of a multiple-emitter transistor.
Note 3. Applies when the base-emitter resistance (R_{BE}) is equal to or less than 500Ω.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Notes 4 & 5)

Supply Voltage (V_{CC})
SG55450B, SG55460, SG55470 ..... 4.5V to 5.5V
SG75450B, SG75460, SG75470 ..... 4.75V to 5.25V

Operating Ambient Temperature Range
SG55450B, SG55460, SG55470 ..... -55°C to 125°C
SG75450B, SG75460, SG75470 ..... 0°C to 70°C

Note 4. Range over which device is functional.
Note 5. The substrate (pin 8) must always be at the most-negative device voltage for proper operation.

ELECTRICAL SPECIFICATIONS (TTL Gates)

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG55450B/460/470 with -55°C ≤ T_A ≤ 125°C, and SG75450B/460/470 with 0°C ≤ T_A ≤ 70°C. Typical values are tested at V_{CC} = 5V and T_A = 25°C. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter		Test Conditions	SG55450B SG55460 SG55470 Min.	Typ.	Max.	SG75450B SG75460 SG75470 Min.	Typ.	Max.	Units
TTL Gates									
High-level Input Voltage (V_{IH})			2			2			V
Low-level Input Voltage (V_{IL})					0.8			0.8	V
Input Clamp Voltage (V_{IK})		V_{CC} = MIN, I_{IN} = -12mA		-1.2	-1.5		-1.2	-1.5	V
High-level Output Voltage (V_{OH})		V_{CC} = MIN, V_{IL} = 0.8V, I_{OH} = -400mA	2.4	3.3		2.4	3.3		V
Low-level Output Voltage (V_{OL})		V_{CC} = MIN, V_{IH} = 2V, I_{OL} = 16mA		0.25	0.5		0.25	0.4	V
Input Current at Max V_{IN} (I_{IN})	input A	V_{CC} = MAX, V_{IN} = 5.5V			1			1	mA
	input G	V_{CC} = MAX, V_{IN} = 5.5V			2			2	mA
High-level Input Current (I_{IH})	input A	V_{CC} = MAX, V_{IN} = 2.4V			40			40	µA
	input G	V_{CC} = MAX, V_{IN} = 2.4V			80			80	mA
Low-level Input Current (I_{IL})	input A	V_{CC} = MAX, V_{IN} = 0.4V			-1.6			-1.6	µA
	input G	V_{CC} = MAX, V_{IN} = 0.4V			-3.2			-3.2	mA
Short-circuit Output Current (Note 6)		V_{CC} = MAX	-18		-55	-18		-55	mA
Supply Current, Outputs High		V_{CC} = MAX, V_{IN} = 0			4			4	mA
Supply Current, Outputs Low		V_{CC} = MAX, V_{IN} = 5V			11			11	mA

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG55450B SG55460 SG55470			SG75450B SG75460 SG75470			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Transistors								
Collector-Base Breakdown Voltage	I_C = 100µA, I_E = 0							
($V_{(BR)CBO}$)	SG55450B/SG75450B	35			35			V
	SG55460/SG75460	40			40			V
	SG55470/SG75470	70			70			V
Collector-Emitter Breakdown	I_C = 10mA, I_B = 0							
Voltage ($V_{(BR)CEO}$) (Note 7)	SG55460/SG75460	25			25			V
	SG55470/SG75470	40			40			V
Collector-Emitter Breakdown	I_C = 100µA, R_{BE} = 500Ω							
Voltage	SG55450B/SG75450B	30			30			V
	SG55460/SG75460	40			40			V
	SG55470/SG75470	70			70			V
Emitter-Base Breakdown Voltage ($V_{(BR)EBO}$)	I_E = 100µA, I_C = 0	5			5			V
Static Forward Current Transfer Ratio	V_{CE} = 3V, I_C = 100mA, T_A = 25°C	25			25			
(h_{fe}) (Note 7)	V_{CE} = 3V, I_C = 300mA, T_A = 25°C	30			30			
	V_{CE} = 3V, I_C = 100mA, T_A = MIN	10			20			
	V_{CE} = 3V, I_C = 300mA, T_A = MIN	15			25			
Base-Emitter Voltage (V_{BE}) (Note 7)	I_B = 10mA, I_C = 100mA		0.85	1.2		0.85	1.0	V
	I_B = 30mA, I_C = 300mA		1	1.4		1	1.2	V
Collector-Emitter Saturation	I_B = 10mA, I_C = 100mA		0.25	0.5		0.25	0.4	V
Voltage ($V_{CE(SAT)}$) (Note 7)	I_B = 30mA, I_C = 300mA		0.45	0.8		0.45	0.7	V

Note 6. Not more than one output should be shorted at a time.
Note 7. These parameters must be measured using pulse techniques (t_w = 300µs, duty cycle ≤ 2%).

SWITCHING SPECIFICATIONS (V_{CC} = 5V, T_A = 25°C)

Parameter	Test Conditions	SG55450B SG75450B			SG55460 SG75460			SG55470 SG75470			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
TTL Gates											
Propagation Delay Time, Low-to-High Level Output	C_L = 15pF, R_L = 400Ω		12	22		22			22		ns
Propagation Delay Time, High-to-Low Level Output			8	15		8			8		ns
Output Transistors (Note 8)											
Delay Time	I_L = 200mA, $I_{B(1)}$ = 20mA,		8	15		10			10		ns
Rise Time	$I_{B(2)}$ = -40mA, $V_{BE(off)}$ = -1V,		12	20		16			16		ns
Storage Time	C_L = 15pF, R_L = 50Ω		7	15		23			23		ns
Fall Time			6	15		14			14		ns
Gate and Transistors Combined											
Propagation Delay Time, Low-to-High Level Output	I_C = 200mA, C_L = 15pF, $R_L \approx 50\Omega$		20	30		45	65		45	65	ns
Propagation Delay Time, High-to-Low Level Output			20	30		35	50		35	50	ns
Transition Time, Low-to-High Output			7	12		10	20		10	20	ns
Transition Time, High-to-Low Level Output			9	15		10	20		10	20	ns
High-Level Output Voltage After Switching	I_C = 300mA, R_{BE} = 500Ω										
	V_S = 20V	V_S-6.5									mV
	V_S = 30V				V_S-10						mV
	V_S = 55V							V_S-18			mV

Note 8. Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

CHARACTERISTIC CURVES

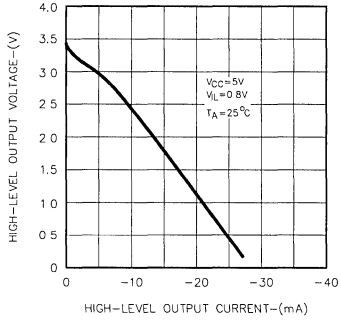


FIGURE 1.
HIGH-LEVEL OUTPUT VOLTAGE VS. HIGH-LEVEL OUTPUT CURRENT

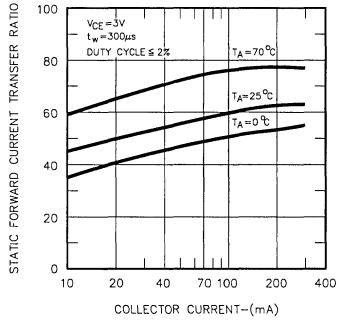


FIGURE 2.
STATIC FORWARD VS. COLLECTOR CURRENT

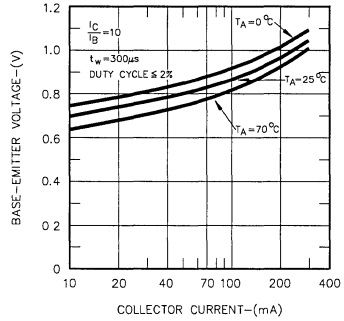


FIGURE 3.
BASE-EMITTER VOLTAGE VS. COLLECTOR VOLTAGE

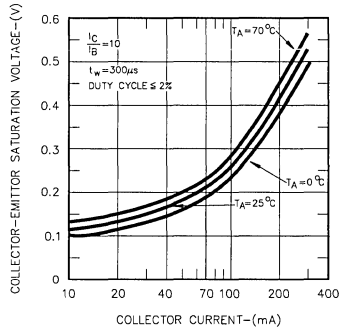
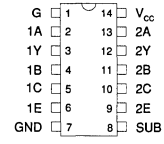
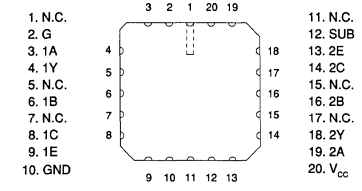


FIGURE 4.
COLLECTOR-EMITTER SATURATION VOLTAGE VS. COLLECTOR CURRENT

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN CERAMIC DIP J - PACKAGE	SG55450BJ/883B SG55450BJ SG55460J/883B SG55460J SG55470J/883B SG55470J SG75450BJ SG75460J SG75470J	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C 0°C to 70°C 0°C to 70°C 0°C to 70°C	
20-PIN CERAMIC LEADLESS CHIP CARRIER L- PACKAGE	SG55450BL/883B SG55450BL SG55460L/883B SG55460L SG55470L/883B SG55470L	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availability.
2. All parts are viewed from the top.
3. Product is also available in flat pack. Consult factory for price and delivery.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SG55451B/SG55461/SG55471
SG75451B/SG75461/SG75471

DUAL PERIPHERAL POSITIVE-AND DRIVER

DESCRIPTION

The SG5541B/SG55461/SG55471 (SG75451B/SG75461/SG75471) series of dual peripheral Positive-AND drivers are a family of versatile devices designed for use in systems that employ TTL or DTL logic. This family of drivers are direct replacements for the Texas Instruments SN55451B/61/71 (SN75451B/61/71)series. Diode-clamped inputs simplify circuit design. Typical applications include high-speed logic buffers, power drivers, relay drivers, MOS drivers, line drivers, and memory drivers. The SG55451B/SG55461/SG55471 drivers are characterized for operation over the full military ambient temperature range of -55°C to 125°C and the SG75451B/SG75461/SG75471 drivers are chracterized for operation from 0°C to 70°C.

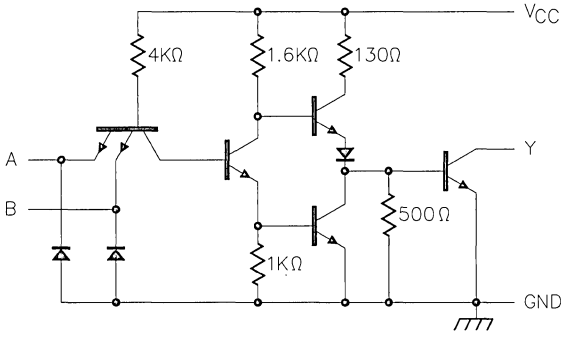
FEATURES

- **300mA output current capability**
- **High-voltage output**
- **No output latch-up at 20V**
- **High speed switching**
- **TTL or DTL compatible diode-clamped inputs**
- **Standard supply voltages**

HIGH RELIABILITY FEATURES
- SG55451B/SG55461/SG55471

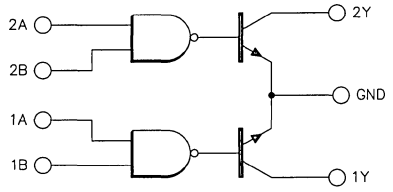
- **Available to MIL-STD-883**
- **Scheduled for MIL-M-38510 QPL listing**
- **SG level "S"processing available**

EQUIVALENT CIRCUIT SCHEMATIC (each driver)



BLOCK DIAGRAM

Positive Logic: Y = AB



FUNCTION TABLE (each gate)

A	B	Y
L	L	L (on-state)
L	H	L (on-state)
H	L	L (on-state)
H	H	H (off-state)

H = High Level, L = Low Level

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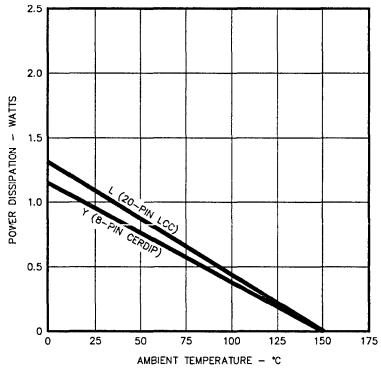
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V_{CC}) 7V
Input Voltage 5.5V
Interemitter Voltage 5.5V
Off-state Output Voltage
X5451B Series 30V
X5461 Series 35V
X5471 Series 70V

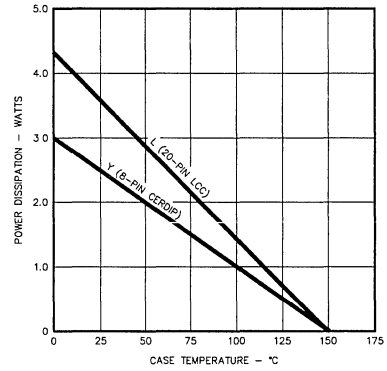
Output Current 400mA
Continuous Total Dissipation at (or below)
25°C Free-Air Temperature 800mW
Operating Junction Temperature
Hermetic (Y, L Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (1/16 inch from case
for soldering 60 sec.) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Notes 2 & 3)

Supply Voltage (V_{CC})
SG55451B, SG55461, SG55471 ..... 4.5V to 5.5V
SG75451B, SG75461, SG75471 ..... 4.75V to 5.25V

Operating Ambient Temperature Range
SG55451B, SG55461, SG55471 ..... -55°C to 125°C
SG75451B, SG75461, SG75471 ..... 0°C to 70°C

Note 2. Range over which device is functional.
Note 3. The substrate (pin 8) must always be at the most-negative device voltage for proper operation.

ELECTRICAL SPECIFICATIONS

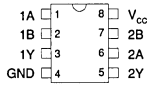
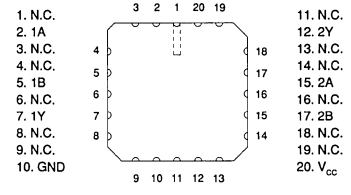
(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG55451B/461/471 with -55°C ≤ T_A ≤ 125°C, and SG75451B/461/471 with 0°C ≤ T_A ≤ 70°C. Typical values are tested at V_{CC} = 5V, and T_A = 25°C. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG55451B SG55461 SG55471			SG75451B SG75461 SG75471			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
High-level Input Voltage (V_{IH})		2			2			V
Low-level Input Voltage (V_{IL})				0.8			0.8	V
Input Clamp Voltage (V_{IK})	V_{CC} = MIN, I_{IN} = -12mA		-1.2	-1.5		-1.2	-1.5	V
High-level Output Current (I_{OH})	V_{CC} = MIN, V_{IH} = 2V,							
	V_{OH} = 30V SGX5451B			300			100	µA
	V_{OH} = 35V SGX5461							
	V_{OH} = 70V SGX5471							
Low-level Output Voltage (V_{OL})	V_{CC} = MIN, V_{IL} = 0.8V, I_{OL} = 100mA		0.25	0.5		0.25	0.4	V
	V_{CC} = MIN, V_{IL} = 0.8V, I_{OL} = 300mA		0.5	0.8		0.5	0.7	V
Input Current at Max V_{IN} (I_{IN})	V_{CC} = MAX, V_{IN} = 5.5V			1.0			1.0	mA
High-level Input Current (I_{IH})	V_{CC} = MAX, V_{IN} = 2.4V			40			40	µA
Low-level Input Current (I_{IL})	V_{CC} = MAX, V_{IN} = 0.4V		-1.0	-1.6		-1.0	-1.6	mA
Supply Current, Outputs High	V_{CC} = MAX, V_{IN} = 5V		8	11		8	11	mA
Supply Current, Outputs Low	V_{CC} = MAX, V_{IN} = 0V							
	SGX5451B		52	65		52	65	mA
	SGX5461		56	76		56	76	mA
	SGX5471		56	76		56	76	mA

SWITCHING SPECIFICATIONS (V_{CC} = 5V, T_A = 25°C)

Parameter	Test Conditions	SG55451B SG75451B			SG55461 SG75461			SG55471 SG75471			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Propagation Delay Time, Low-to-High Level Output	I_C = 200mA, C_L = 15pF, $R_L \approx 50\Omega$		18	25		30	55		30	55	ns
Propagation Delay Time, High-to-Low Level Output			18	25		25	40		25	40	ns
Transition Time, Low-to-High Output			5	8		8	20		8	20	ns
Transition Time, High-to-Low Level Output			7	12		10	20		10	20	ns
High-Level Output Voltage After Switching	I_C = 300mA, V_S = 20V SGX5451B	V_S-6.5									mV
	V_S = 30V SGX5461				V_S-10						mV
	V_S = 55V SGX5471							V_S-18			mV

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
8-PIN CERAMIC DIP Y - PACKAGE	SG55451BY/883B	-55°C to 125°C	
	SG55451BY	-55°C to 125°C	
	SG55461Y/883B	-55°C to 125°C	
	SG55461Y	-55°C to 125°C	
	SG55471Y/883B	-55°C to 125°C	
	SG55471Y	-55°C to 125°C	
	SG75451BY	0°C to 70°C	
	SG75461Y	0°C to 70°C	
	SG75471Y	0°C to 70°C	
20-PIN CERAMIC LEADLESS CHIP CARRIER L- PACKAGE	SG55451BL/883B	-55°C to 125°C	
	SG55451BL	-55°C to 125°C	
	SG55461L/883B	-55°C to 125°C	
	SG55461L	-55°C to 125°C	
	SG55471L/883B	-55°C to 125°C	
	SG55471L	-55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availability.
2. All parts are viewed from the top.
3. Product is also available in flat pack. Consult factory for price and delivery.

SG55452B/SG55462/SG55472
SG75452B/SG75462/SG75472

DUAL PERIPHERAL POSITIVE-NAND DRIVER

DESCRIPTION

The SG55452B/SG55462/SG55472 (SG75452B/SG75462/SG75472) series of dual peripheral Positive-NAND drivers are a family of versatile devices designed for use in systems that employ TTL or DTL logic. This family of drivers are direct replacements for the Texas Instruments SN55452B/62/72 (SN75452B/62/72) series. Diode-clamped inputs simplify circuit design. Typical applications include high-speed logic buffers, power drivers, relay drivers, MOS drivers, line drivers, and memory drivers. The SG55452B/SG55462/SG55472 drivers are characterized for operation over the full military ambient temperature range of -55°C to 125°C and the SG75452B/SG75462/SG75472 drivers are characterized for operation from 0°C to 70°C.

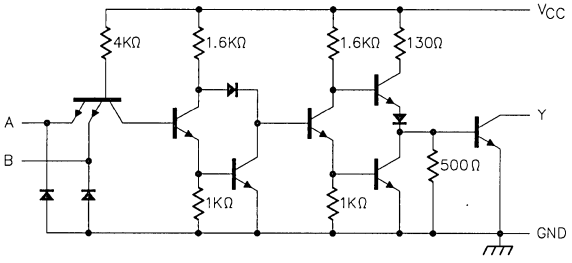
FEATURES

- **300mA output current capability**
- **High-voltage output**
- **No output latch-up at 20V**
- **High speed switching**
- **TTL or DTL compatible diode-clamped inputs**
- **Standard supply voltages**

HIGH RELIABILITY FEATURES - SG55452B/SG55462/SG55472

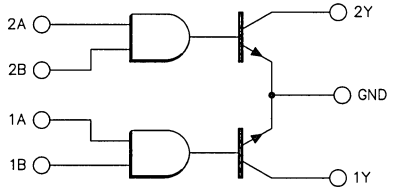
- **Available to MIL-STD-883 and DESC SMD**
- **Scheduled for MIL-M-38510 QPL listing**
- **SG level "S"processing available**

EQUIVALENT CIRCUIT SCHEMATIC (each driver)



BLOCK DIAGRAM

Positive Logic: Y = AB



FUNCTION TABLE (each gate)

A	B	Y
L	L	H (off-state)
L	H	H (off-state)
H	L	H (off-state)
H	H	L(on-state)

H = High Level, L = Low Level

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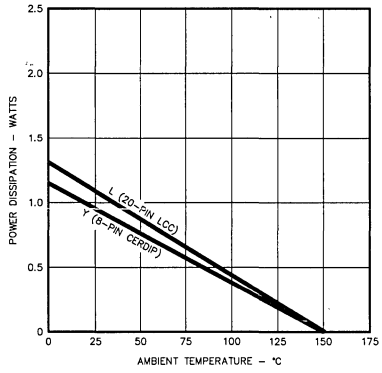
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V_{CC}) 7V
Input Voltage 5.5V
Interemitter Voltage 5.5V
Off-state Output Voltage
X5452B Series 30V
X5462 Series 35V
X5472 Series 70V

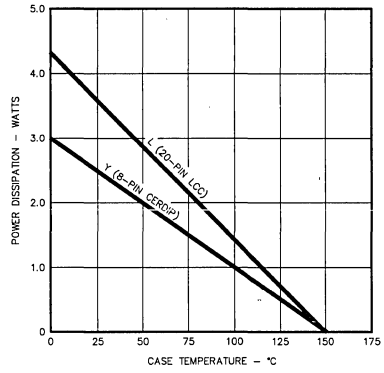
Note 1. Exceeding these ratings could cause damage to the device.

Output Current 400mA
Continuous Total Dissipation at (or below)
25°C Free-Air Temperature 800mW
Operating Junction Temperature
Hermetic (Y, L Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (1/16 inch from case
for soldering 60 sec.) ..... 300°C

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Notes 2 & 3)

Supply Voltage (V_{CC})
SG55452B, SG55462, SG55472 ..... 4.5V to 5.5V
SG75452B, SG75462, SG55472 ..... 4.75V to 5.25V

Operating Ambient Temperature Range
SG55452B, SG55462, SG55472 ..... -55°C to 125°C
SG75452B, SG75462, SG75472 ..... 0°C to 70°C

Note 2. Range over which device is functional.
Note 3. The substrate (pin 8) must always be at the most-negative device voltage for proper operation.

ELECTRICAL SPECIFICATIONS

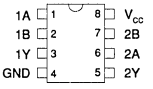
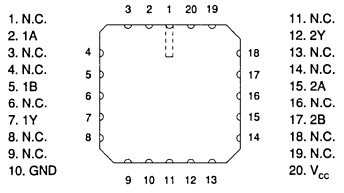
(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG55452B/462/472 with -55°C ≤ T_A ≤ 125°C, and SG75452B/462/472 with 0°C ≤ T_A ≤ 70°C. Typical values are tested at V_{CC} = 5V, and T_A = 25°C. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG55452B SG55462 SG55472			SG75452B SG75462 SG75472			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
High-level Input Voltage (V_{IH})		2			2			V
Low-level Input Voltage (V_{IL})				0.8			0.8	V
Input Clamp Voltage (V_{IK})	V_{CC} = MIN, I_{IN} = -12mA		-1.2	-1.5		-1.2	-1.5	V
High-level Output Current (I_{OH})	V_{CC} = MIN, V_{IL} = 0.8V, V_{OH} = 30V SGX5452B			300			100	µA
	V_{OH} = 35V SGX5462							
	V_{OH} = 70V SGX5472							
Low-level Output Voltage (V_{OL})	V_{CC} = MIN, V_{IH} = 2.0V, I_{OL} = 100mA		0.25	0.5		0.25	0.4	V
	V_{CC} = MIN, V_{IH} = 2.0V, I_{OL} = 300mA		0.5	0.8		0.5	0.7	V
Input Current at Max V_{IN} (I_{IN})	V_{CC} = MAX, V_{IN} = 5.5V			1.0			1.0	mA
High-level Input Current (I_{IH})	V_{CC} = MAX, V_{IN} = 2.4V			40			40	µA
Low-level Input Current (I_{IL})	V_{CC} = MAX, V_{IN} = 0.4V		-1.0	-1.6		-1.0	-1.6	mA
Supply Current, Outputs High	V_{CC} = MAX, V_{IN} = 0V							
	SGX5452B		11	14		11	14	mA
	SGX5462, SGX5472		13	17		13	17	mA
Supply Current, Outputs Low	V_{CC} = MAX, V_{IN} = 5V							
	SGX5452B		56	71		56	71	mA
	SGX5462, SGX5472		61	76		61	76	mA

SWITCHING SPECIFICATIONS (V_{CC} = 5V, T_A = 25°C)

Parameter	Test Conditions	SG55452B SG75452B			SG55462 SG75462			SG55472 SG75472			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Propagation Delay Time, Low-to-High Level Output	I_C = 200mA, C_L = 15pF, $R_L \approx 50\Omega$		26	35		45	65		45	65	ns
Propagation Delay Time, High-to-Low Level Output			24	35		30	50		30	50	ns
Transition Time, Low-to-High Output			5	8		13	25		13	25	ns
Transition Time, High-to-Low Level Output			7	12		10	20		10	20	ns
High-Level Output Voltage After Switching	I_C = 300mA, V_S = 20V SGX5452B	V_S-6.5									mV
	V_S = 30V SGX5462				V_S-10						mV
	V_S = 55V SGX5472							V_S-18			mV

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
8-PIN CERAMIC DIP Y - PACKAGE	SG55452BY/883B	-55°C to 125°C	
	SG55452BY	-55°C to 125°C	
	SG55462Y/883B	-55°C to 125°C	
	SG55462Y	-55°C to 125°C	
	SG55472Y/883B	-55°C to 125°C	
	SG55472Y	-55°C to 125°C	
	SG75452BY	0°C to 70°C	
	SG75462Y	0°C to 70°C	
	SG75472Y	0°C to 70°C	
20-PIN CERAMIC LEADLESS CHIP CARRIER L- PACKAGE	SG55452BL/883B	-55°C to 125°C	
	SG55452BL	-55°C to 125°C	
	SG55462L/883B	-55°C to 125°C	
	SG55462L	-55°C to 125°C	
	SG55472L/883B	-55°C to 125°C	
	SG55472L	-55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availability.
2. All parts are viewed from the top.
3. Product is also available in flat pack. Consult factory for price and delivery.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SG55453B/SG55463/SG55473
SG75453B/SG75463/SG75473

DUAL PERIPHERAL POSITIVE-OR DRIVER

DESCRIPTION

The SG55453B/SG55463/SG55473 (SG75453B/SG75463/SG75473) series of dual peripheral Positive-OR drivers are a family of versatile devices designed for use in systems that employ TTL or DTL logic. This family of drivers are direct replacements for the Texas Instruments SN55453B/63/73 (SN75453B/63/73) series. Diode-clamped inputs simplify circuit design. Typical applications include high-speed logic buffers, power drivers, relay drivers, MOS drivers, line drivers, and memory drivers. The SG55453B/SG55463/SG55473 drivers are characterized for operation over the full military ambient temperature range of -55°C to 125°C and the SG75453B/SG75463/SG75473 drivers are characterized for operation from 0°C to 70°C.

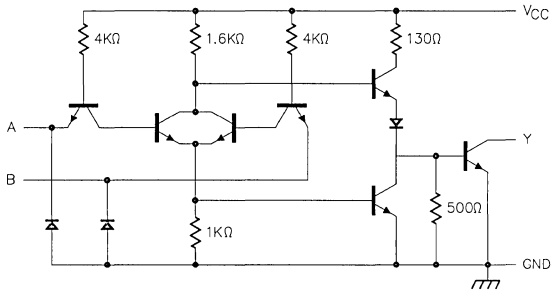
FEATURES

- **300mA output current capability**
- **High-voltage output**
- **No output latch-up at 20V**
- **High speed switching**
- **TTL or DTL compatible diode-clamped inputs**
- **Standard supply voltages**

HIGH RELIABILITY FEATURES - SG55453B/SG55463/SG55473

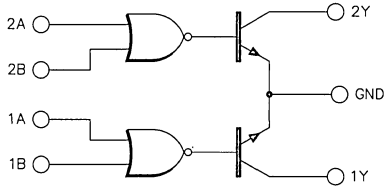
- ◊ **Available to MIL-STD-883**
- ◊ **Scheduled for MIL-M-38510 QPL listing**
- ◊ **SG level "S"processing available**

EQUIVALENT CIRCUIT SCHEMATIC (each driver)



BLOCK DIAGRAM

Positive Logic: Y = A + B



FUNCTION TABLE (each gate)

A	B	Y
L	L	L (on-state)
L	H	H (off-state)
H	L	H (off-state)
H	H	H (off-state)

H = High Level, L = Low Level

April 1990

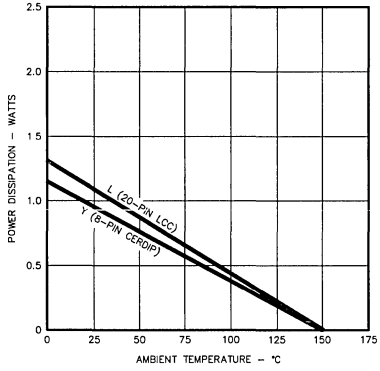
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V_{CC}) 7V
Input Voltage 5.5V
Interemitter Voltage 5.5V
Off-state Output Voltage
X5453B Series 30V
X5463 Series 35V
X5473 Series 70V

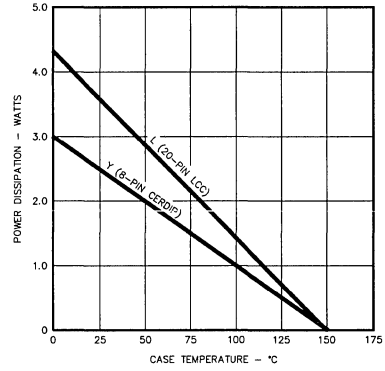
Note 1. Exceeding these ratings could cause damage to the device.

Output Current 400mA
Continuous Total Dissipation at (or below)
25°C Free-Air Temperature 800mW
Operating Junction Temperature
Hermetic (Y, L Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (1/16 inch from case
for soldering 60 sec.) ..... 300°C

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Notes 2 & 3)

Supply Voltage (V_{CC})
SG55453B, SG55463, SG55473 ..... 4.5V to 5.5V
SG75453B, SG75463, SG75473 ..... 4.75V to 5.25V

Operating Ambient Temperature Range
SG55453B, SG55463, SG55473 ..... -55°C to 125°C
SG75453B, SG75463, SG75473 ..... 0°C to 70°C

Note 2. Range over which device is functional.
Note 3. The substrate (pin 8) must always be at the most-negative device voltage for proper operation.

ELECTRICAL SPECIFICATIONS

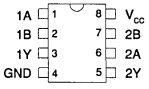
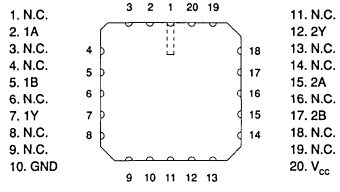
(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG55453B/463/473 with -55°C ≤ T_A ≤ 125°C, and SG75453B/463/473 with 0°C ≤ T_A ≤ 70°C. Typical values are tested at V_{CC} = 5V, and T_A = 25°C. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG55453B SG55463 SG55473			SG75453B SG75463 SG75473			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
High-level Input Voltage (V_{IH})		2			2			V
Low-level Input Voltage (V_{IL})				0.8			0.8	V
Input Clamp Voltage (V_{IK})	V_{CC} = MIN, I_{IN} = -12mA		-1.2	-1.5		-1.2	-1.5	V
High-level Output Current (I_{OH})	V_{CC} = MIN, V_{IH} = 2V,			300			100	µA
	V_{OH} = 30V SGX5453B							
	V_{OH} = 35V SGX5463							
	V_{OH} = 70V SGX5473							
Low-level Output Voltage (V_{OL})	V_{CC} = MIN, V_{IL} = 0.8V, I_{OL} = 100mA		0.25	0.5		0.25	0.4	V
	V_{CC} = MIN, V_{IL} = 0.8V, I_{OL} = 300mA		0.5	0.8		0.5	0.7	V
Input Current at Max V_{IN} (I_{IN})	V_{CC} = MAX, V_{IN} = 5.5V			1.0			1.0	mA
High-level Input Current (I_{IH})	V_{CC} = MAX, V_{IN} = 2.4V			40			40	µA
Low-level Input Current (I_{IL})	V_{CC} = MAX, V_{IN} = 0.4V		-1.0	-1.6		-1.0	-1.6	mA
Supply Current, Outputs High	V_{CC} = MAX, V_{IN} = 5V		8	11		8	11	mA
Supply Current, Outputs Low	V_{CC} = MAX, V_{IN} = 0V							
	SGX5453B		54	68		54	68	mA
	SGX5463		58	76		58	76	mA
	SGX5473		58	76		58	76	mA

SWITCHING SPECIFICATIONS (V_{CC} = 5V, T_A = 25°C)

Parameter	Test Conditions	SG55453B SG75453B			SG55463 SG75463			SG55473 SG75473			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Propagation Delay Time, Low-to-High Level Output	I_C = 200mA, C_L = 15pF, $R_L \approx 50\Omega$		18	25		30	55		30	55	ns
Propagation Delay Time, High-to-Low Level Output			16	25		25	40		25	40	ns
Transition Time, Low-to-High Output			5	8		8	20		8	20	ns
Transition Time, High-to-Low Level Output			7	12		10	20		10	20	ns
High-Level Output Voltage After Switching	I_C = 300mA, V_S = 20V SGX5453B	V_S-6.5									mV
	V_S = 30V SGX5463				V_S-10						mV
	V_S = 55V SGX5473							V_S-18			mV

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
8-PIN CERAMIC DIP Y - PACKAGE	SG55453BY/883B	-55°C to 125°C	
	SG55453BY	-55°C to 125°C	
	SG55463Y/883B	-55°C to 125°C	
	SG55463Y	-55°C to 125°C	
	SG55473Y/883B	-55°C to 125°C	
	SG55473Y	-55°C to 125°C	
	SG75453BY	0°C to 70°C	
	SG75463Y	0°C to 70°C	
	SG75473Y	0°C to 70°C	
20-PIN CERAMIC LEADLESS CHIP CARRIER L- PACKAGE	SG55453BL/883B	-55°C to 125°C	
	SG55453BL	-55°C to 125°C	
	SG55463L/883B	-55°C to 125°C	
	SG55463L	-55°C to 125°C	
	SG55473L/883B	-55°C to 125°C	
	SG55473L	-55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availability.
2. All parts are viewed from the top.
3. Product is also available in flat pack. Consult factory for price and delivery.

SG55454B/SG55464/SG55474
SG75454B/SG75464/SG75474

DUAL PERIPHERAL POSITIVE-NOR DRIVER

DESCRIPTION

The SG55454B/SG55464/SG55474 (SG75454B/SG75464/SG75474) series of dual peripheral Positive-NOR drivers are a family of versatile devices designed for use in systems that employ TTL or DTL logic. This family of drivers are direct replacements for the Texas Instruments SN55454B/64/74 (SN75454B/64/74) series. Diode-clamped inputs simplify circuit design. Typical applications include high-speed logic buffers, power drivers, relay drivers, MOS drivers, line drivers, and memory drivers. The SG55454B/SG55464/SG55474 drivers are characterized for operation over the full military ambient temperature range of -55°C to 125°C and the SG75454B/SG75464/SG75474 drivers are characterized for operation from 0°C to 70°C.

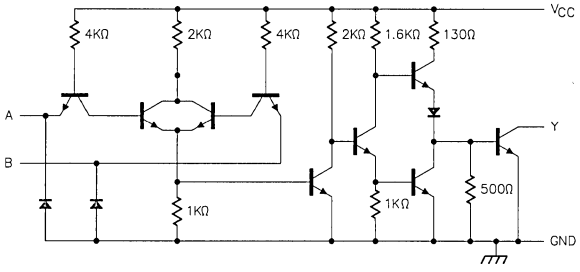
FEATURES

- **300mA output current capability**
- **High-voltage output**
- **No output latch-up at 20V**
- **High speed switching**
- **TTL or DTL compatible diode-clamped inputs**
- **Standard supply voltages**

HIGH RELIABILITY FEATURES
- SG55454B/SG55464/ SG55474

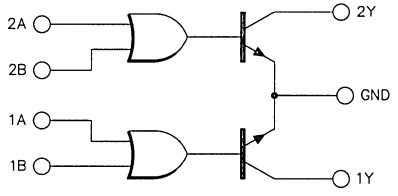
- ♦ **Available to MIL-STD-883**
- ♦ **Scheduled for MIL-M-38510 QPL listing**
- ♦ **SG level "S"processing available**

EQUIVALENT CIRCUIT SCHEMATIC (each driver)



BLOCK DIAGRAM

Positive Logic: $Y = \overline{A + B}$



FUNCTION TABLE (each gate)

A	B	Y
L	L	H (off-state)
L	H	L (on-state)
H	L	L (on-state)
H	H	L (on-state)

H = High Level, L = Low Level

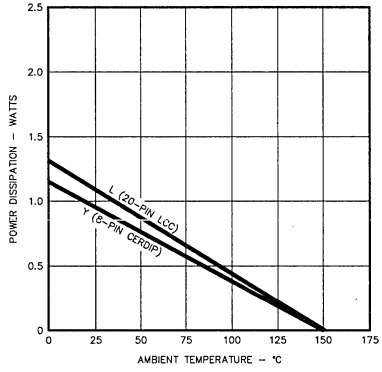
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V_{CC}) 7V
Input Voltage 5.5V
Interemitter Voltage 5.5V
Off-state Output Voltage
  X5454B Series 30V
  X5464 Series 35V
  X5474 Series 70V

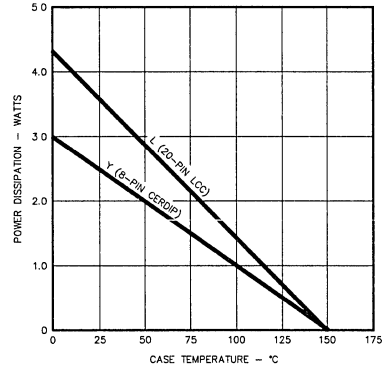
Output Current 400mA
Continuous Total Dissipation at (or below)
  25°C Free-Air Temperature 800mW
Operating Junction Temperature
  Hermetic (Y, L Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (1/16 inch from case
  for soldering 60 sec.) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Notes 2 & 3)

Supply Voltage (V_{CC})
  SG55454B, SG55464, SG55474 ..... 4.5V to 5.5V
  SG75454B, SG75464, SG75474 ..... 4.75V to 5.25V

Operating Ambient Temperature Range
  SG55454B, SG55464, SG55474 ..... -55°C to 125°C
  SG75454B, SG75464, SG75474 ..... 0°C to 70°C

Note 2. Range over which device is functional.
Note 3. The substrate (pin 8) must always be at the most-negative device voltage for proper operation.

ELECTRICAL SPECIFICATIONS

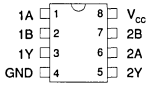
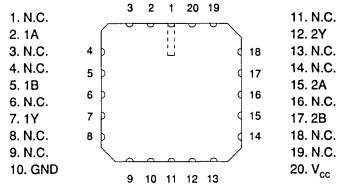
(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG55454B/464/474 with -55°C ≤ T_A ≤ 125°C, and SG75454B/464/474 with 0°C ≤ T_A ≤ 70°C. Typical values are tested at V_{CC} = 5V, and T_A = 25°C. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG55454B SG55464 SG55474			SG75454B SG75464 SG75474			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
High-level Input Voltage (V_{IH})		2			2			V
Low-level Input Voltage (V_{IL})				0.8			0.8	V
Input Clamp Voltage (V_{IK})	V_{CC} = MIN, I_{IN} = -12mA		-1.2	-1.5		-1.2	-1.5	V
High-level Output Current (I_{OH})	V_{CC} = MIN, V_{IH} = 2V, V_{OH} = 30V SGX5454B			300			100	µA
	V_{OH} = 35V SGX5464							
	V_{OH} = 70V SGX5474							
Low-level Output Voltage (V_{OL})	V_{CC} = MIN, V_{IL} = 0.8V, I_{OL} = 100mA		0.25	0.5		0.25	0.4	V
	V_{CC} = MIN, V_{IL} = 0.8V, I_{OL} = 300mA		0.5	0.8		0.5	0.7	V
Input Current at Max V_{IN} (I_{IN})	V_{CC} = MAX, V_{IN} = 5.5V			1.0			1.0	mA
High-level Input Current (I_{IH})	V_{CC} = MAX, V_{IN} = 2.4V			40			40	µA
Low-level Input Current (I_{IL})	V_{CC} = MAX, V_{IN} = 0.4V		-1.0	-1.6		-1.0	-1.6	mA
Supply Current, Outputs High	V_{CC} = MAX, V_{IN} = 0V							
	SGX5454B		13	17		13	17	mA
	SGX5464, SGX5474		14	19		14	19	mA
Supply Current, Outputs Low	V_{CC} = MAX, V_{IN} = 5V							
	SGX5454B		61	79		61	79	mA
	SGX5464, SGX5474		67	85		67	85	mA

SWITCHING SPECIFICATIONS (V_{CC} = 5V, T_A = 25°C)

Parameter	Test Conditions	SG55454B SG75454B			SG55464 SG75464			SG55474 SG75474			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Propagation Delay Time, Low-to-High Level Output	I_C = 200mA, C_L = 15pF, $R_L \approx 50\Omega$		26	35		45	65		45	65	ns
Propagation Delay Time, High-to-Low Level Output			24	35		30	50		30	50	ns
Transition Time, Low-to-High Output			5	8		13	25		13	25	ns
Transition Time, High-to-Low Level Output			7	12		10	20		10	20	ns
High-Level Output Voltage After Switching	I_C = 300mA, V_S = 20V SGX5454B	V_S-6.5									mV
	V_S = 30V SGX5464				V_S-10						mV
	V_S = 55V SGX5474							V_S-18			mV

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
8-PIN CERAMIC DIP Y - PACKAGE	SG55454BY/883B	-55°C to 125°C	
	SG55454BY	-55°C to 125°C	
	SG55464Y/883B	-55°C to 125°C	
	SG55464Y	-55°C to 125°C	
	SG55474Y/883B	-55°C to 125°C	
	SG55474Y	-55°C to 125°C	
	SG75454BY	0°C to 70°C	
	SG75464Y	0°C to 70°C	
	SG75474Y	0°C to 70°C	
20-PIN CERAMIC LEADLESS CHIP CARRIER L- PACKAGE	SG55454BL/883B	-55°C to 125°C	
	SG55454BL	-55°C to 125°C	
	SG55464L/883B	-55°C to 125°C	
	SG55464L	-55°C to 125°C	
	SG55474L/883B	-55°C to 125°C	
	SG55474L	-55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availability.
2. All parts are viewed from the top.
3. Product is also available in flat pack. Consult factory for price and delivery.

SILICON GENERAL

THUMB INDEX

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SELECTION GUIDE
OP-AMPS & COMPARATORS

GENERAL PURPOSE

Device Type	Description	Key Features	Packages
SG101A/201A/301A	General purpose Operational Amplifier	• ±20V supply voltage range • Offset voltage 3mV max. over temperature • Offsets guaranteed over entire common mode range	J, N, T, F
SG2101A	General purpose dual Operational Amplifier	• Two SG101A chips in one package • See SG101A features	J
SG107/207/307	General purpose Operational Amplifier	• ±20V supply voltage range • Offset voltage 3mV max. over temperature • Offsets guaranteed over entire common mode range • Internally compensated	J, N, T, F
SG111/211/311	General purpose comparator	• 30V supply voltage range • 50V, 50mA output capability • Single 5V supply operation	Y, T, F, L
SG2111	General purpose dual comparator	• Two SG111 chips in one package • See SG111 features	J
SG741/741C	General purpose Operational Amplifier	• ±20V supply voltage range • Complete short circuit protection • High common mode voltage range • Internally compensated	J, N, T, F
SG143/343	General purpose High Voltage Operational Amplifier	• ±40V supply voltage range • ±37V output voltage swing • ±24V common mode voltages • Over voltage protection • Output short circuit protection • Internally compensated	Y, T
SG1536/1436	General purpose High Voltage Operational Amplifier	• ±40V supply voltage range • ±37V output voltage swing • ±24V common mode voltages • Over voltage protection • Output short circuit protection • Internally compensated	Y, T

December 1988

POWER OPERATIONAL AMPLIFIERS

Device Type	Description	$I_{O(PK)}$	$I_{O(CONT)}$	$V_{CC(MAX)}$	$I_{S(MAX)}$	Key Features	Packages
SG1173/2173/3173	Single Power Operational Amplifier	5A	3.5A	50V	20mA	• Internally compensated • Current limit protection • Thermal shutdown protection	P, R
SG3172	Single Power Operational Amplifier	3A	2A	18V	14mA	• Optimized for low overhead motor drive • Internally compensated • Current limit protection • Thermal shutdown protection	P, R
SG3272	Dual Power Operational Amplifier	1.5A	1A	18V	15mA	• Two Operational Amplifiers in one package • Internal flyback protection diodes • Common mode range includes ground (V_{EE}) • Ideal for driving motors in "H" bridge configuration • Internally compensated • Thermal shutdown protection	DWW, Y

December 1988

DESCRIPTION

The SG101A/201A/301A is a general purpose internally compensated operational amplifier. It has excellent input bias current and drift characteristics in addition to short circuit protection and is pin compatible with industry standard operational amplifiers.

The SG101A is guaranteed and fully characterized over the full military ambient temperature range of -55°C to 125°C while the SG201A is electrically identical, except its performance is guaranteed from –25°C to 85°C. The 301A is designed for commercial applications of 0°C to 70°C.

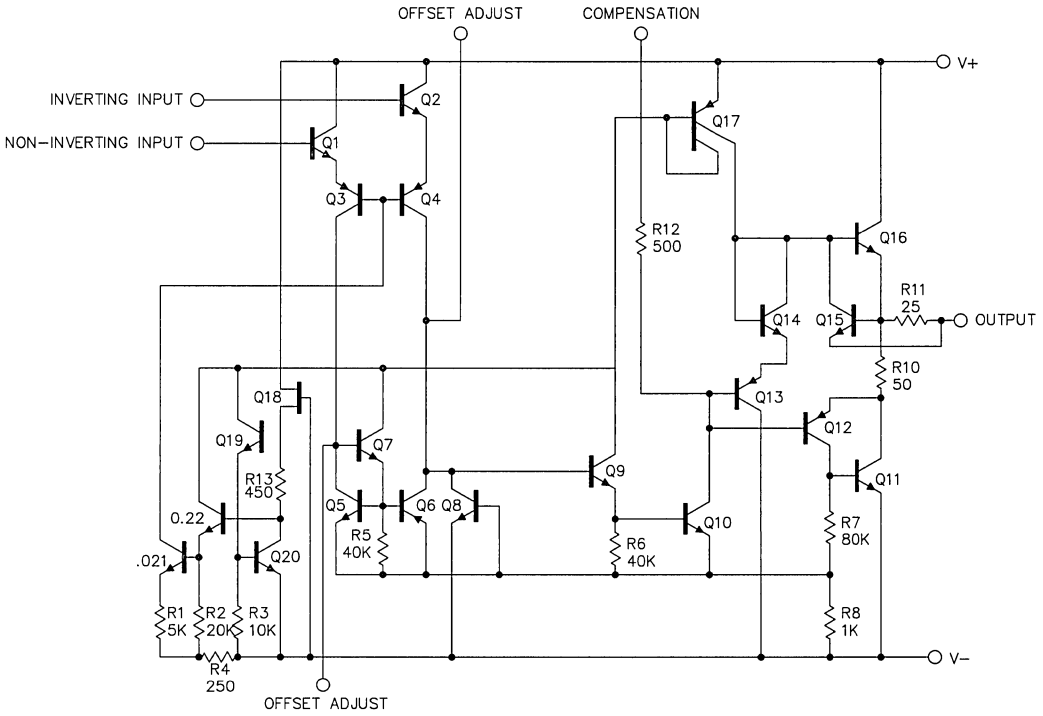
FEATURES

- **Offset voltage 3mV maximum over temperature**
- **Input bias current 100nA maximum over temperature**
- **Offset current 20nA maximum over temperature**
- **Guaranteed drift characteristics**
- **Offsets guaranteed over entire common mode range**

HIGH RELIABILITY FEATURES - SG101A

- **Available to MIL-STD-883**
- **MIL-M38510/10103BGA - JAN101AT**
- **MIL - M38510 / 10103BHA - JAN101AF**
- **SG level "S" processing available**

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Votage
- SG101A/201A ..... ±22V
- SG301A ..... ±18V

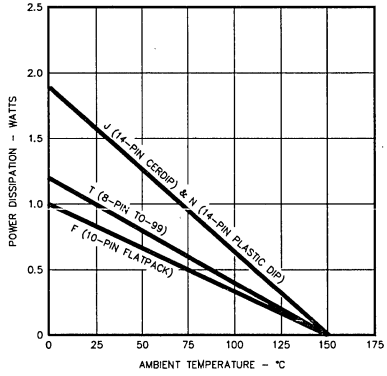
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±15V

Operating Junction Temperature
- Hermetic (T, J, F Packages) ..... 150°C
- Plastic (N Package) ..... 150°C

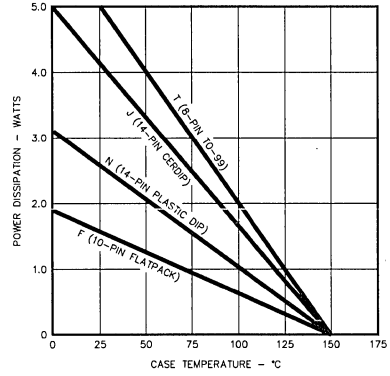
Storage Temperature Range ..... -65°C to 150°C
Output Short Circuit Duration (Note 3) ..... Indefinite
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.
Note 2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
Note 3. Continuous short circuit is allowed for case temperatures to 125°C and ambient temperatures to 70°C.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 4 & 5)

Supply Voltage
- SG101A/201A ..... ±5V to ±20V
- SG301A ..... ±5V to ±18V

Operating Ambient Temperature Range
- SG101A ..... -55°C to 125°C
- SG201A ..... -25°C to 85°C
- SG301A ..... 0°C to 70°C

Note 4. Range over which the device is functional.
Note 5. R_L = 2KΩ, C_L = 100pF.

ELECTRICAL SPECIFICATIONS

(Unless otherwise stated, these specifications apply for the operating ambient temperature of T_A = 25°C and ±5V ≤ V_S ≤ ±20V, and C_1 = 30pF. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG101A/SG201A			SG301A			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	R_S ≤ 50KΩ		0.7	2.0		2.0	7.5	mV
Input Offset Current			1.5	10		3.0	50	nA
	$T_A = T_{MIN}$ to T_{MAX}			20			70	nA
Input Bias Current			30	75		70	250	nA
	$T_A = T_{MIN}$ to T_{MAX}			100			300	nA
Input Resistance (Note 5)		1.5	4		0.5	2		MΩ
Supply Current	V_S = ±20V		1.8	3.0				mA
	T_A = 125°C		1.2	2.5				mA
	V_S = ±15V					1.8	3.0	mA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, R_L ≥ 2KΩ	50	160		25	160		V/mV
	V_S = ±15V, V_{OUT} = ±10V, R_L ≥ 2KΩ, $T_A = T_{MIN}$ to T_{MAX}	25			25			V/mV
Output Voltage Swing	V_S = ±15V, R_L = 10KΩ	±12	±14		±12	±14		V
	V_S = ±15V, R_L = 2KΩ	±10	±13		±10	±13		V
Input Voltage Range	V_S = ±20V, $T_A = T_{MIN}$ to T_{MAX}	±15			±15			V
Common Mode Rejection Ratio	R_S ≤ 10KΩ, $T_A = T_{MIN}$ to T_{MAX}	80	96		80	96		dB
Supply Voltage Rejection Ratio	R_S ≤ 10KΩ, $T_A = T_{MIN}$ to T_{MAX}	80	96		80	96		dB

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG107/SG207			SG307			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Average Temperature Coefficient of Input Offset Voltage (Note 5)	$T_A = T_{MIN}$ to T_{MAX}		3.0	15		6.0	30	µV/°C
Average Temperature Coefficient of Input Offset Current (Note 5)	25°C ≤ T_A ≤ 125°C		0.01	0.1				nA/°C
	-55°C ≤ T_A ≤ 25°C		0.02	0.2				nA/°C
	25°C ≤ T_A ≤ 70°C					0.01	0.3	nA/°C
	0°C ≤ T_A ≤ 25°C					0.02	0.6	nA/°C

Note 5. These parameters, although guaranteed, are not tested in production.

CHARACTERISTIC CURVES

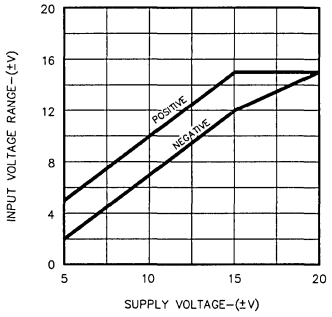


FIGURE 1.
INPUT VOLTAGE RANGE VS. SUPPLY VOLTAGE

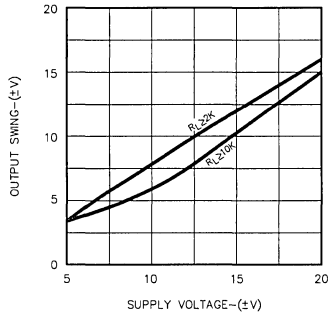


FIGURE 2.
OUTPUT SWING VS. SUPPLY VOLTAGE

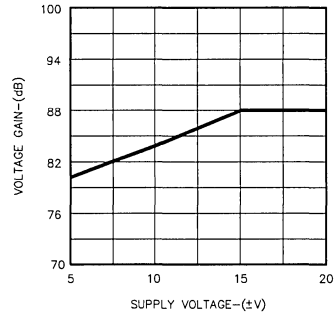


FIGURE 3.
MINIMUM VOLTAGE GAIN

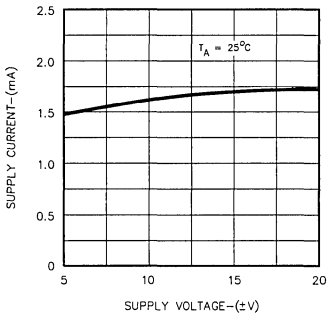


FIGURE 4.
SUPPLY CURRENT VS. SUPPLY VOLTAGE

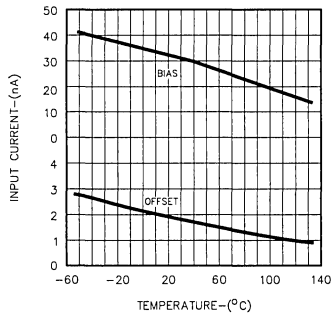


FIGURE 5.
INPUT CURRENT VS. TEMPERATURE

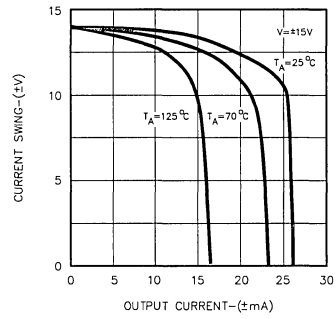


FIGURE 6.
CURRENT LIMITING

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CHARACTERISTIC CURVES

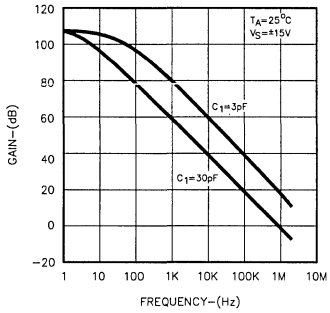


FIGURE 7.
OPEN LOOP FREQUENCY RESPONSE

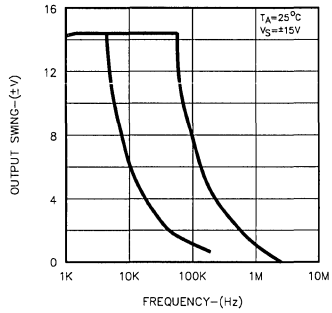


FIGURE 8.
LARGE SIGNAL FREQUENCY RESPONSE

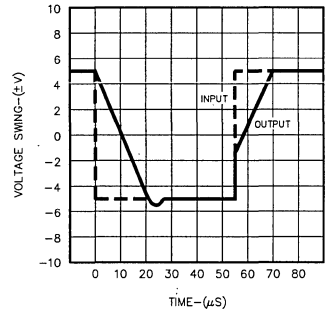
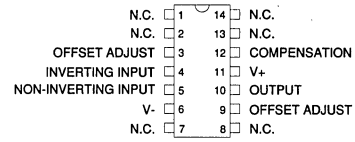
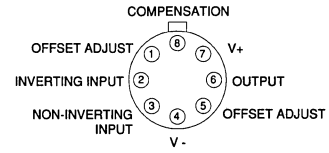
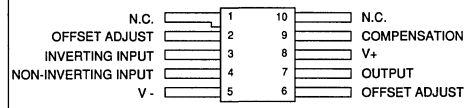


FIGURE 9.
VOLTAGE FOLLOWER PULSE RESPONSE

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN CERAMIC DIP J - PACKAGE	SG101AJ/883B SG101AJ SG201AJ SG301AJ	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
14-PIN PLASTIC DIP N - PACKAGE	SG201AN SG301AN	-25°C to 85°C 0°C to 70°C	
8-PIN METAL CAN T - PACKAGE	SG101AT/883B SG101AT SG201AT SG301AT	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
10-PIN CERAMIC FLAT PACK F - PACKAGE	SG101AF/883B SG101AF	-55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SG2101A

ADDENDUM TO SG101A DATA SHEET

DUAL OPERATIONAL AMPLIFIERS

DESCRIPTION

The SG2101A is a dual version of the SG101A Operational Amplifier and consists of two independent dice in the same package.

The SG2101A is a general-purpose internally compensated operational amplifier. It has excellent input bias current and drift characteristics in addition to short circuit protection and is pin compatible with industry standard operational ampliufiers.

The SG2101A is guaranteed and fully characterized over the full military ambient temperature range of -55°C to 125°C.

FEATURES

- **Dual independent SG101A**
- **Offset voltage 3mV maximum over temperature**
- **Input bias current 100nA maximum over temperature**
- **Offset current 20nA maximum over temperature**
- **Guaranteed drift characteristics**
- **Offsets guaranteed over entire common-mode range**

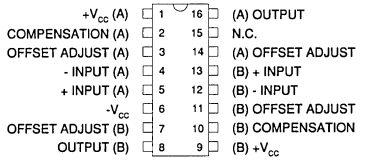
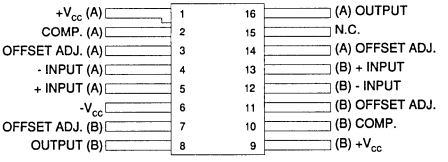
HIGH RELIABILITY FEATURES - SG2101A

- ◊ **Available to MIL-STD - 883**
- ◊ **MIL - M38510 / 10105BEA - JAN2101AJ**
- ◊ **SG level "S" processing available**

OPERATING CONDITIONS & ELECTRICAL SPECIFICATIONS

(All information is identical to the SG101A. Consult data sheet for specifics.)

CONNECTION DIAGRAMS & ORDERING INFORMATION

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG2101AJ/883B SG2101AJ	-55°C to 125°C -55°C to 125°C	
16-PIN CERAMIC FLAT PACK F - PACKAGE	SG2101AF/883B SG2101AF	-55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availability.
2. All parts are viewed from the top.

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DESCRIPTION

The SG107/207/307 is a general purpose internally compensated operational amplifier. It has excellent input bias current and drift characteristics in addition to short circuit protection and is pin compatible with industry standard operational amplifiers.

The SG107 is guaranteed and fully characterized over the full military ambient temperature range of -55°C to 125°C while the SG207 is electrically identical, except its performance is guaranteed from –25°C to 85°C. The 307 is designed for commercial applications of 0°C to 70°C.

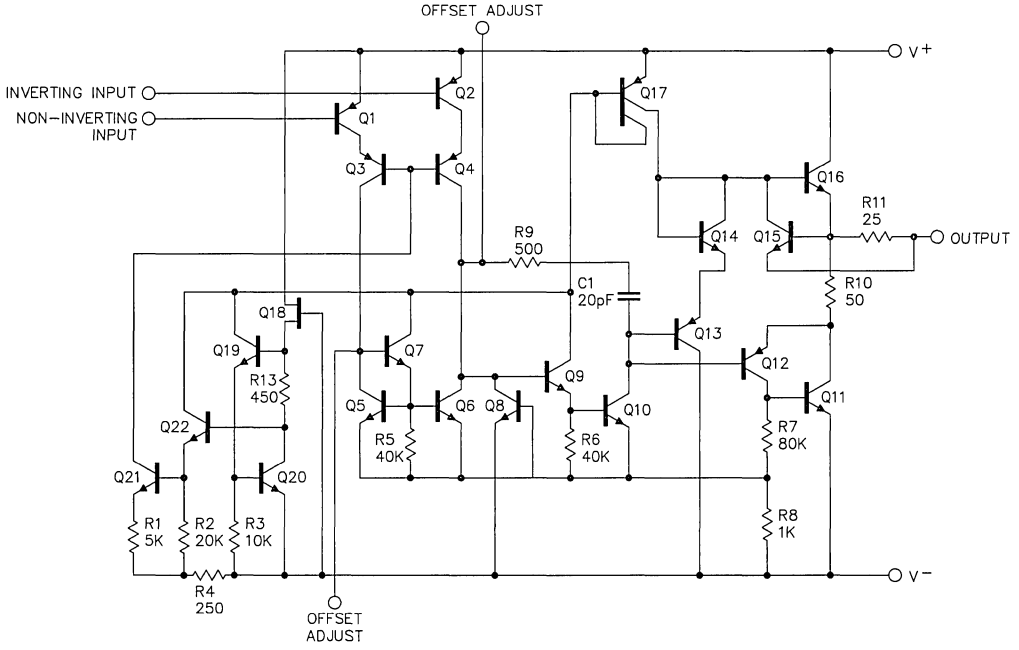
FEATURES

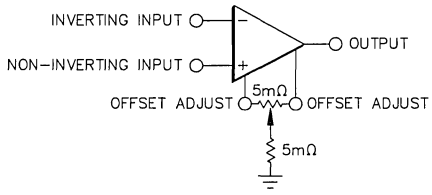
- **Offset voltage 3mV maximum over temperature**
- **Input current 100nA maximum over temperature**
- **Offset current 20nA maximum over temperature**
- **Guaranteed drift characteristics**
- **Offsets guaranteed over entire common mode range**

HIGH RELIABILITY FEATURES - SG107

- **Available to MIL-STD - 883**
- **SG level "S" processing available**

SCHEMATIC DIAGRAM





Optional Balancing Circuit

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Votage
- SG107/207 ..... ±22V
- SG307 ..... ±18V

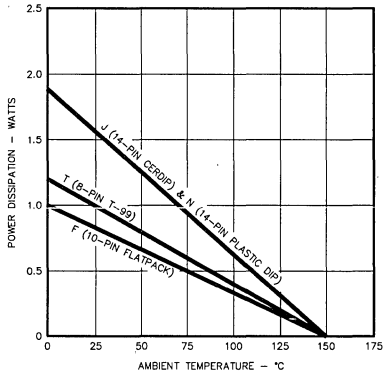
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±15V

Operating Junction Temperature
- Hermetic (T, J, F Packages) ..... 150°C
- Plastic (N Package) ..... 150°C

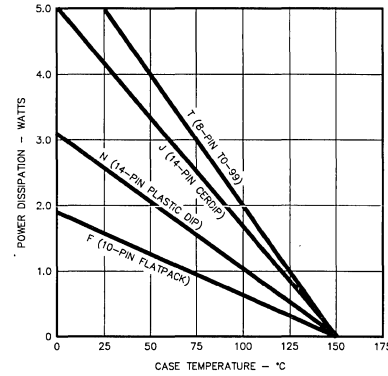
Storage Temperature Range ..... -65°C to 150°C
Output Short Circuit Duration (Note 3) ..... Indefinite
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.
Note 2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
Note 3. Continuous short circuit is allowed for case temperatures to 125°C and ambient temperatures to 70°C.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 4)

Supply Voltage
- SG107/207 ..... ±5V to ±20V
- SG307 ..... ±5V to ±15V

Operating Ambient Temperature Range
- SG107 ..... -55°C to 125°C
- SG207 ..... -25°C to 85°C
- SG307 ..... 0°C to 70°C

Note 4. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise stated, these specifications apply for the operating ambient temperature of T_A = 25°C and for ±5V ≤ V_S ≤ ±20V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

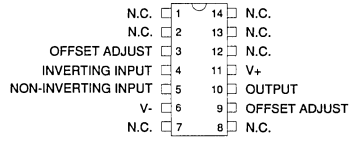
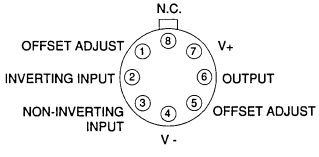
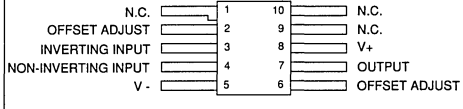
Parameter	Test Conditions	SG107/SG207			SG307			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	$R_S \le 50K\Omega$		0.7	2.0		2.0	7.5	mV
	$T_A = T_{MIN}$ to T_{MAX}			3.0			10.0	mV
Input Offset Current			1.5	10		3.0	50	nA
	$T_A = T_{MIN}$ to T_{MAX}			20			70	nA
Input Bias Current			30	75		70	250	nA
	$T_A = T_{MIN}$ to T_{MAX}			100			300	nA
Input Resistance (Note 5)		1.5	4		0.5	2		MΩ
Supply Current	$V_S = \pm 20V$		1.8	3.0				mA
	$V_S = \pm 15V$					1.8	3.0	mA
Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $V_S = \pm 15V$, $R_L \ge 2K\Omega$,	50	160		25	160		V/mV
	$T_A = T_{MIN}$ to T_{MAX}	25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10K\Omega$	±12	±14		±12	±14		V
	$V_S = \pm 15V$, $R_L = 2K\Omega$	±10	±13		±10	±13		V
Input Voltage Range	$V_S = \pm 20V$, $T_A = T_{MIN}$ to T_{MAX}	±15						V
	$V_S = \pm 15V$, $T_A = T_{MIN}$ to T_{MAX}				±12			V
Common Mode Rejection Ratio	$T_A = T_{MIN}$ to T_{MAX}	80	96		80	96		dB
Supply Voltage Rejection Ratio	$R_S \le 10K\Omega$, $T_A = T_{MIN}$ to T_{MAX}	80	96		80	96		dB

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG107/SG207			SG307			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Average Temperature Coefficient of Input Offset Voltage (Note 5)	$T_A = T_{MIN}$ to T_{MAX}		3.0	15		6.0	15	V/mV
Average Temperature Coefficient of Input Offset Current (Note 5)							±12	V
	$25°C \le T_A \le 125°C$		0.01	0.1			±10	V
	$-55°C \le T_A \le 25°C$		0.02	0.2				V
	$25°C \le T_A \le 70°C$					0.01	±12	V
	$0°C \le T_A \le 25°C$					0.02	80	dB
							80	dB

Note 5. These parameters, although guaranteed, are not tested in production.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN CERAMIC DIP J - PACKAGE	SG107J/883B SG107J SG207J SG307J	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
14-PIN PLASTIC DIP N - PACKAGE	SG207N SG307N	-25°C to 85°C 0°C to 70°C	
8-PIN METAL CAN T - PACKAGE	SG107T/883B SG107T SG207T SG307T	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
10-PIN CERAMIC FLAT PACK F - PACKAGE	SG107F/883B SG107F	-55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

VOLTAGE COMPARATOR

DESCRIPTION

TheSG111/SG211/SG311 Voltage Comparators are medium-speed, high-input impedance devices which are especially well suited for use in level detection and low-level voltage sensing applications. Operation may be obtained from supply voltages ranging from ±15V down to a single + 5V source.

The output, an open collector NPN capable of switching 50V and 50mA, can drive RTL, DTL, TTL, MOS logic, relays or lamps. Both input and output can be isolated from ground and the output can drive loads referred to a positive supply, ground or a negative supply. These devices also offer offset balance, strobe capability and pin configuration of the SG710 Comparator.

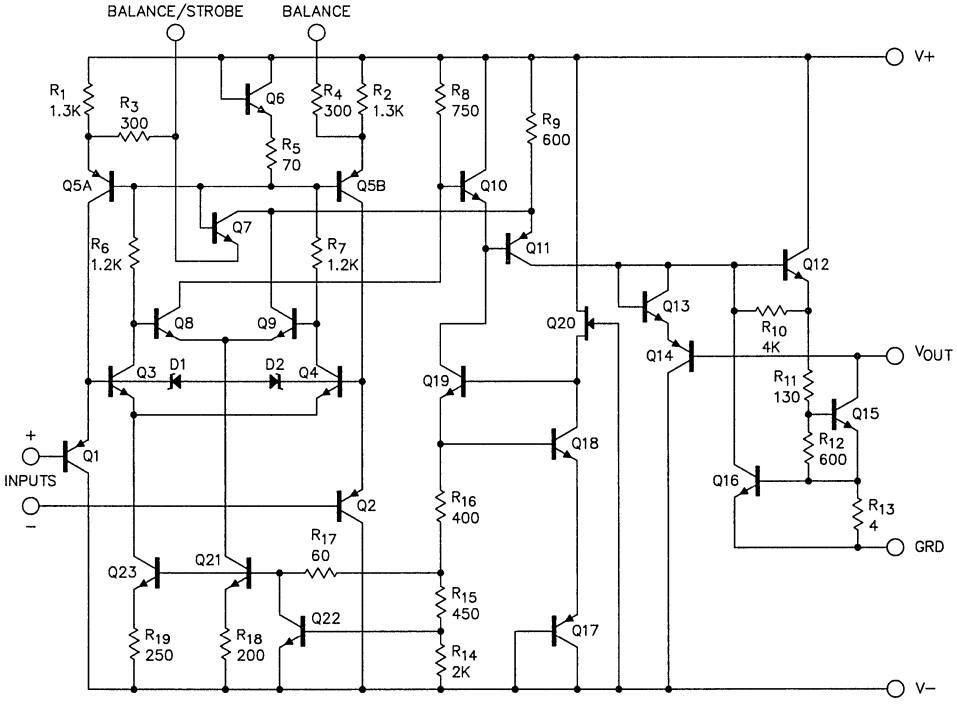
FEATURES

- **Differential input voltage range of ±30V**
- **150nA maximum bias current**
- **50V, 50mA output capability**
- **Single 5V supply operation**
- **Consumes 135mW at ±15V**

HIGH RELIABILITY FEATURES - SG111

- **Available to MIL-STD - 883 and DESC SMD**
- **MIL - M38510 / 10304BGA - JAN111T**
- **SG level "S" processing available**
- **Dual version SG2111 also available for military applications**

SCHEMATIC DIAGRAM



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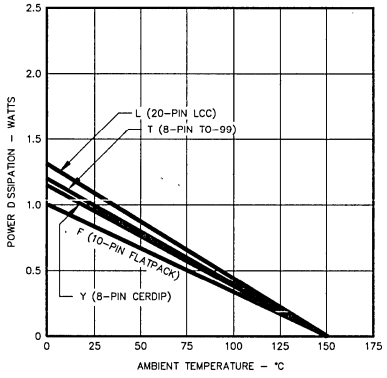
April 1990

ABSOLUTE MAXIMUM RATINGS (Note 1)

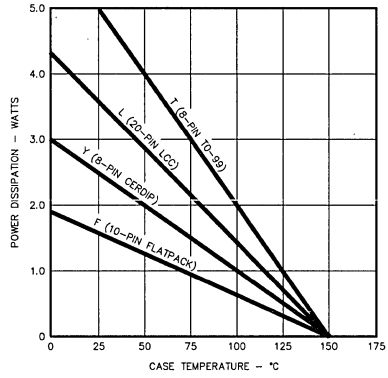
Total Supply Voltage (V_{8-4}) 36V
Output to Negative Supply Voltage (V_{7-4})
SG111/SG211 ..... 50V
SG311 ..... 40V
Ground to Negative Supply Voltage (V_{1-4}) 30V
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±15V
Operating Junction Temperature
Hermetic (Y, T, F, L Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Output Short Circuit Duration ..... 10 sec.
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.
Note 2. Rating for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 3)

Total Supply Voltage ..... 5V to 30V
V_{OUT} to Ground Voltage ..... 0V to 35V
Input Voltage Range with ±15V Supplies ..... ±14V

Note 3. Range over which the device is functional.

Operating Ambient Temperature Range
SG111 ..... -55°C to 125°C
SG211 ..... -25°C to 85°C
SG311 ..... 0°C to 70°C

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG111 with -55°C ≤ T_A ≤ 125°C, SG211 with -25°C ≤ T_A ≤ 85°C, SG 311 with 0°C ≤ T_A ≤ 70°C, and V_S = ±15V. Offset voltage, offset current and bias currents given apply for supply voltages from a single 5V supply to ±15V supplies. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

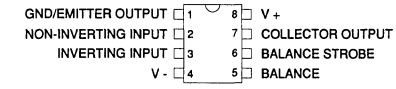
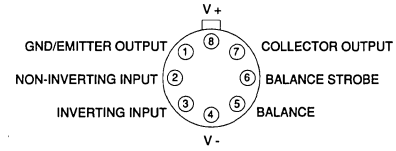
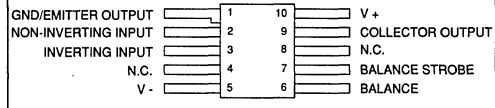
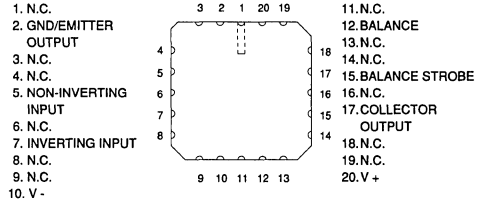
Parameter	Test Conditions	SG111/SG211			SG311			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage (Note 4)	T_A = 25°C, R_S ≤ 50K		0.7	3.0		2.0	7.5	mV
	R_S ≤ 50K			4.0			10	mV
Input Offset Current (Note 4)	T_A = 25°C		4.0	10		6.0	50	nA
				20			70	nA
Input Bias Current	T_A = 25°C		60	100		100	250	nA
				150			300	nA
Voltage Gain	T_A = 25°C		200			200		V/mV
Input Voltage Range			±14			±14		V
Response Time (Note 5)	T_A = 25°C		200			200		nS
Saturation Voltage	I_{OUT} = 50mA, V_{IN} ≤ -5mV		0.75	1.5				V
	I_{OUT} = 50mA, V_{IN} ≤ -10mV V+ ≥ 4.5V, V- = 0					0.75	1.5	V
	V_{IN} ≤ -6mV, I_{SINK} ≤ 8mA		0.23	0.4				V
	V_{IN} ≤ -10mV, I_{SINK} ≤ 8mA					0.23	0.4	V

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG111/SG211			SG311			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Strobe on Current (Note 6)	T_A = 25°C		3.0			3.0		mA
Output Leakage Current (Note 7)	V_{OUT} = 35V, $V_{IN} \geq$ 5mV		0.1	0.5				µA
	T_A = 25°C, $V_{IN} \geq$ 5mV		0.2	10				nA
	T_A = 25°C, $V_{IN} \geq$ 10mV					0.2	50	nA
Short Circuit Current	10mS maximum test duration							
	T_A = -55°C	0		250				mA
	T_A = 125°C	0		150				mA
	T_A = 25°C	0		200	0		200	mA
Positive Supply Current	T_A = 25°C		5.1	6.0		5.1	7.5	mA
Negative Supply Current	T_A = 25°C		4.1	5.0		4.1	5.0	mA
Response Time Low-to-High Level	Overdrive = -5mV							
Collector Output (Note 7)	C_L = 50pF minimum							
	V_{IN} = 100mV		400			400		ns
Response Time High-to-Low level (Note 7)	Overdrive = 5mV							
	C_L = 50pF minimum		400			400		ns
	V_{IN} = 100mV							

Note 4. Maximum values drive output within 1 Volt of either supply with 1mA load.
Note 5. Response time specified is for 100mV input step with 5mV overdrive.
Note 6. Do not short the strobe pin to ground; it should be current driven at 3mA to 5mA.
Note 7. These parameters, although guaranteed over the recommended operating conditions, are not tested in production.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
8-PIN CERAMIC DIP Y - PACKAGE	SG111Y/883B SG111Y SG211Y SG311Y	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
8-PIN METAL CAN T - PACKAGE	SG111T/883B SG111T SG211T SG311T	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	
10-PIN CERAMIC FLAT PACK F - PACKAGE	SG111F/883B SG111F	-55°C to 125°C -55°C to 125°C	
20-PIN CERAMIC LEADLESS CHIP CARRIER L - PACKAGE	SG111L/883B SG111L	-55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SG2111

ADDENDUM TO SG111 DATA SHEET

DUAL VOLTAGE COMPARATOR

DESCRIPTION

The SG2111 is a dual version of the SG111 Voltage Comparator and consists of two independent die in the same package. TheSG111/SG211/ SG311 Voltage Comparators are medium-speed, high-input impedance devices which are especially well suited for use in level detection and low-level voltage sensing applications. Operation may be obtained from supply voltages ranging from ±15V down to a single + 5V source.

The output, an open collector NPN capable of switching 50V and 50mA, can drive RTL, DTL, TTL, MOS logic, relays or lamps. Both input and output can be isolated from ground and the output can drive loads referred to a positive supply, ground or a negative supply. These devices also offer offset balance, strobe capability and pin configuration of the SG710 Comparator.

FEATURES

- **Dual independent SG111**
- **Differential input voltage range of ±30V**
- **150nA maximum bias current**
- **50V, 50mA output capability**
- **Single 5V supply operation**

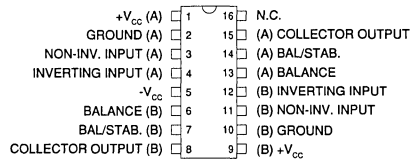
HIGH RELIABILITY FEATURES - SG2111

- **Available to MIL-STD - 883**
- **Scheduled for MIL-M38510 QPL listing**
- **SG level "S" processing available**

OPERATING CONDITIONS & ELECTRICAL SPECIFICATIONS

(All information is identical to the SG111. Consult data sheet for specifics.)

CONNECTION DIAGRAMS & ORDERING INFORMATION

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG2111J/883B SG2111J	-55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availability.
2. All parts are viewed from the top.
3. $+V_{CC}$ (A) and $+V_{CC}$ (B) are not internally connected.
4. $-V_{CC}$ is connected to the case on metal packages.

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SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

HIGH-VOLTAGE OPERATIONAL AMPLIFIER

DESCRIPTION

The SG143 is a general-purpose high-voltage operational amplifier featuring operation to ±40V and overvoltage protection up to ±40V. Increased slew rate, together with higher common-mode and supply rejection, insure improved performance at high supply voltages. Operating characteristics are independent of supply voltage and temperature. These devices are intended for use in high voltage applications where common-mode input ranges, high output voltage swings, and low input currents are required. Also, they are internally compensated and are pin compatible with industry standard operational amplifiers.

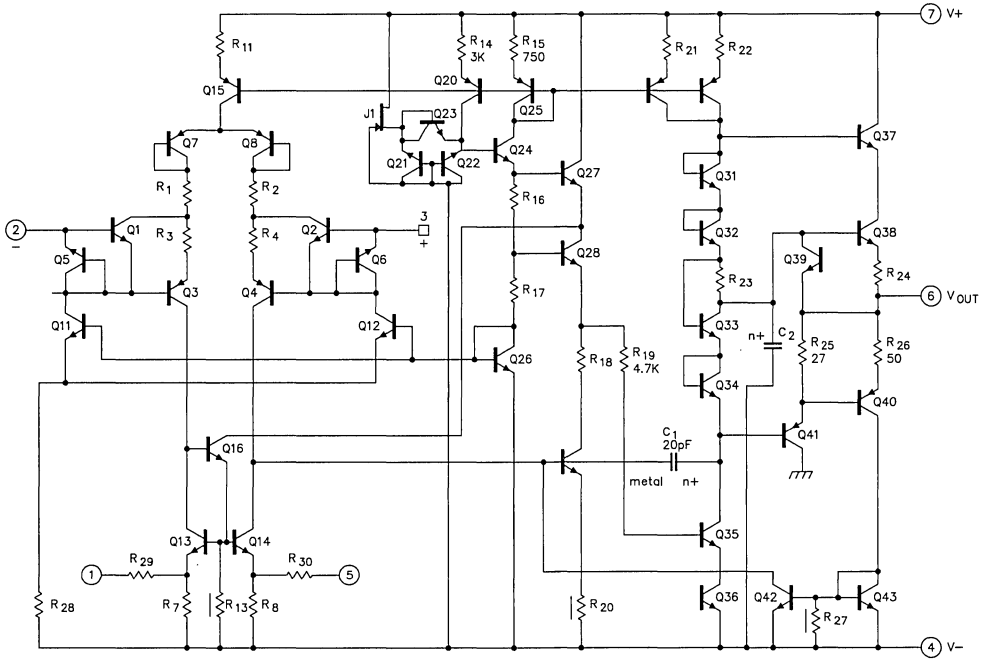
FEATURES

- **±4.0V to ±40V supply voltage range**
- **±37V output voltage swing**
- **±24V common-mode voltages**
- **Overvoltage protection**
- **Output short circuit protection**

HIGH RELIABILITY FEATURES-SG143

- **Available to MIL-STD-883 and DESC SMD**
- **SG level "S" processing available**

CIRCUIT SCHEMATIC



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ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage
- SG143 ..... ±40V
- SG343 ..... ±34V

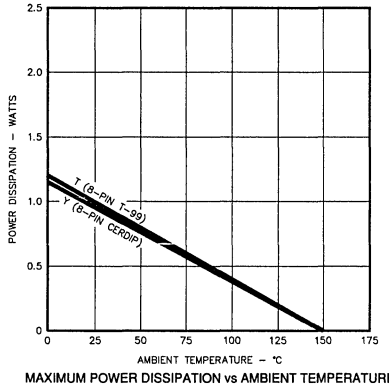
Input Voltage
- SG143 ..... ±40V
- SG343 ..... ±34V

Differential Input Voltage ..... $\pm(V^+ + |V^-| - 3)$ V
Output Short Circuit Duration ..... 5 sec
Operating Junction Temperature
- Hermetic (T, Y-Package) ..... 150°C

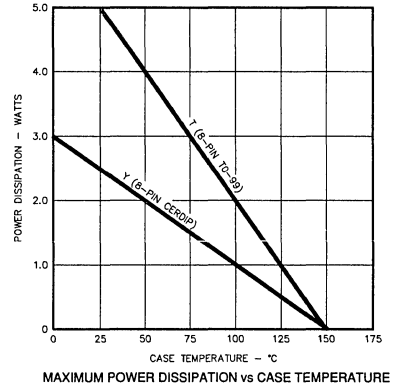
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage
- SG143 ..... ±28V
- SG343 ..... ±15V

Input Voltage
- SG143 ..... ±28V
- SG343 ..... ±15V

Operating Ambient Temperature Range (T_J)
- SG143 ..... -55°C to 125°C
- SG343 ..... 0°C to 75°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply for the operating ambient temperature of 25°C and over the recommended supply voltage range. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG143			SG343			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage			2.0	5.0		2.0	8.0	mV
	$T_A = T_{MIN}$ to T_{MAX}			6.0			10	mV
Input Offset Current			1.0	3.0		5.0	10	nA
	$T_A = T_{MAX}$			4.5			14	nA
	$T_A = T_{MIN}$			7.0			14	nA
Input Bias Current			8.0	20		15	40	nA
	$T_A = T_{MIN}$ to T_{MAX}			35			55	nA
Large Signal Voltage Gain	R_L = 100KΩ, V_{OUT} = ±10V	100	180		70	180		V/mV
	$T_A = T_{MIN}$ to T_{MAX}	50			50			V/mV
Common-Mode Rejection		80	110		70	100		dB
Power Supply Rejection			15	100	35	200		µV/V
Input Common Mode Range (Peak)		±24	±25		±22	±25		V
Unity Gain Bandwidth			1.0			1.0		MHz
Slew Rate			2.5			2.5		V/µs
Supply Current				4.0			5.0	mA
Output Voltage Swing	R_L=5KΩ	±22			±20			V
Short Circuit Current			20			20		mA

CHARACTERISTIC CURVES

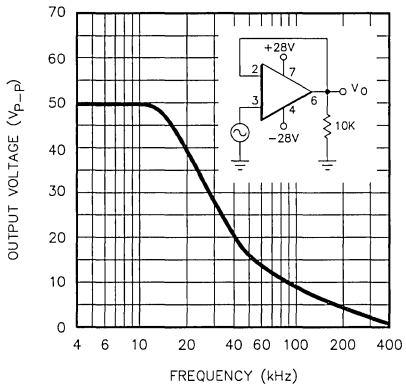


FIGURE 1.
POWER BANDWIDTH

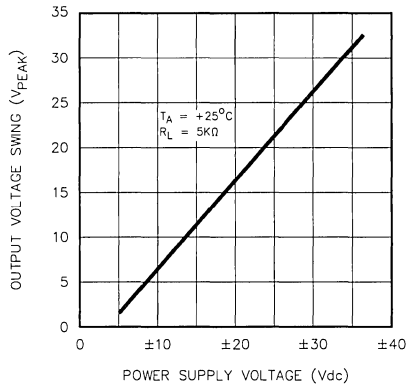


FIGURE 2.
PEAK OUTPUT VOLTAGE SWING VS. POWER SUPPLY VOLTAGE

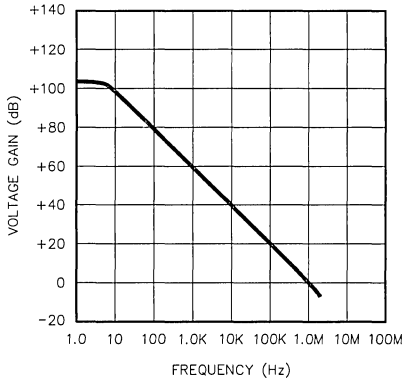


FIGURE 3.
OPEN-POOP FREQUENCY RESPONSE

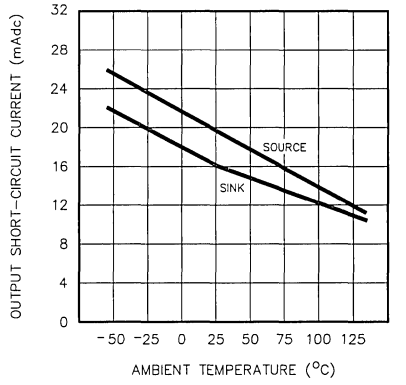


FIGURE 4.
OUTPUT SHORT-CIRCUIT CURRENT VS. TEMPERATURE

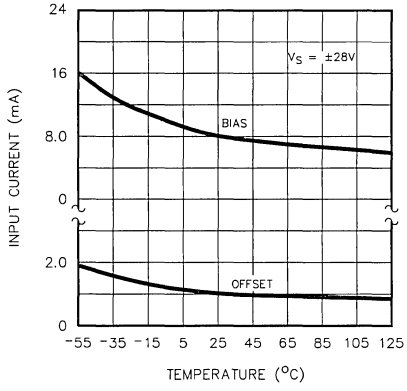


FIGURE 5.
INPUT CURRENT

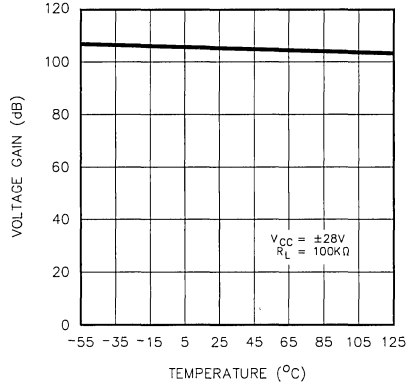


FIGURE 6.
VOLTAGE GAIN

CHARACTERISTIC CURVES (continued)

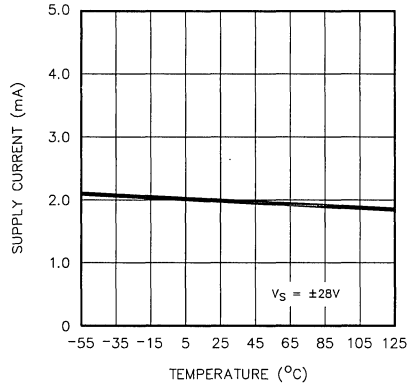


FIGURE 7.
SUPPLY CURRENT

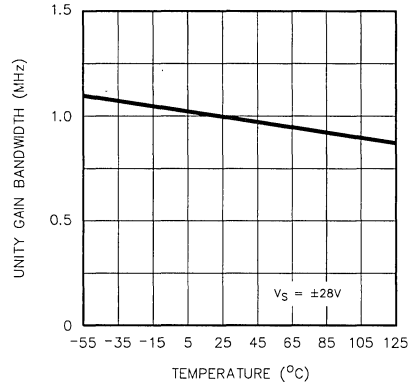


FIGURE 8.
UNITY GAIN BANDWIDTH

TYPICAL APPLICATIONS

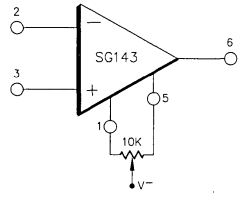


FIGURE 9 - VOLTAGE OFFSET NULL CIRCUIT

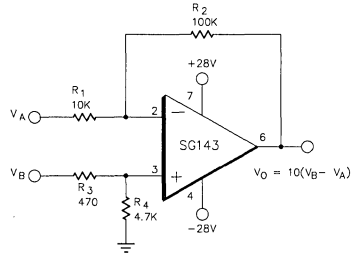


FIGURE 10 - DIFFERENTIAL AMPLIFIER WITH ±20V COMMON-MODE INPUT VOLTAGE RANGE

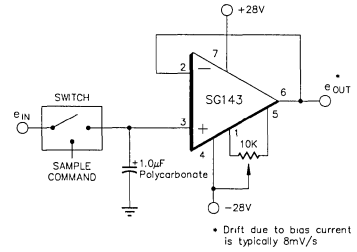
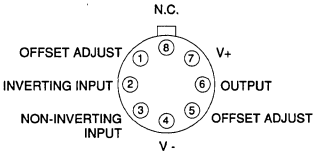
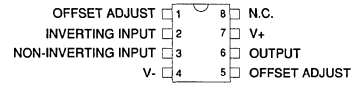


FIGURE 11 - LOW-DRIFT SAMPLE AND HOLD

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
8-PIN METAL CAN T - PACKAGE	SG143T/883B SG143T SG343T	-55°C to 125°C -55°C to 125°C 0°C to 70°C	
8-PIN CERAMIC DIP Y- PACKAGE	SG143Y/883B SG143Y SG343Y	-55°C to 125°C -55°C to 125°C 0°C to 70°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

OPERATIONAL AMPLIFIER

DESCRIPTION

SG741/741C are pin compatible with the most widely accepted operational amplifiers and provide excellent performance fo a wide range of applications. The SG741 is characterized for operation over the full military ambient temperature range of -55°C to 125°C and the SG741C is designed for the commercial temperature range of 0°C to 70°C.

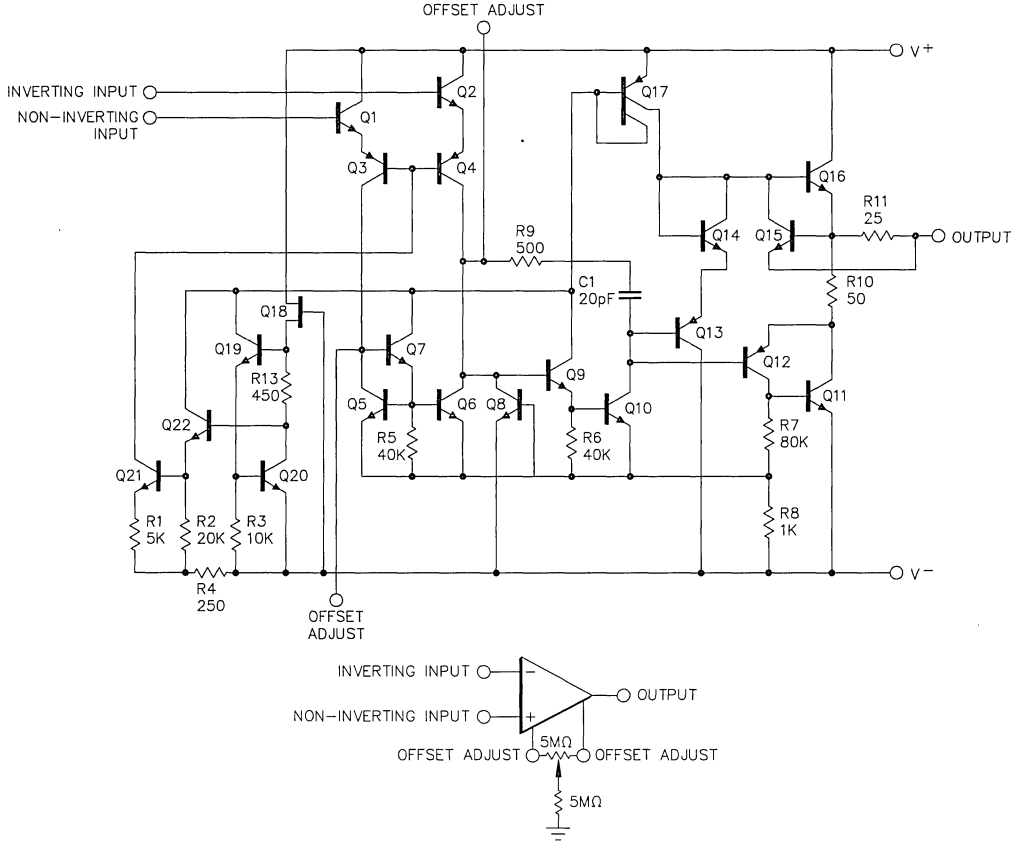
FEATURES

- **Complete short circuit protection**
- **Offset voltage null capability**
- **High common mode voltage range**
- **High differential input voltage range**

HIGH RELIABILITY FEATURES - SG741

- ♦ **Available to MIL-STD - 883**
- ♦ **SG level "S" processing available**

SCHEMATIC DIAGRAM



Optional Balancing Circuit

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ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage
- SG741 ..... ±22V
- SG741C ..... ±18V

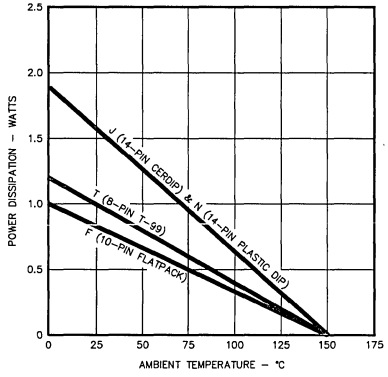
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±15V

Operating Junction Temperature
- Hermetic (T, J, F Packages) ..... 150°C
- Plastic (N Package) ..... 150°C

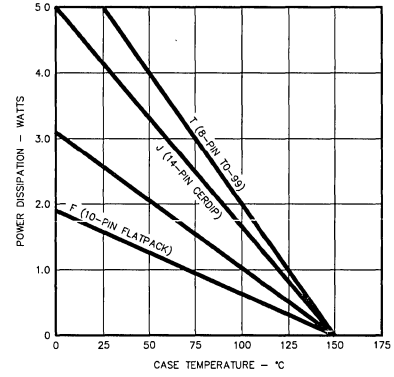
Storage Temperature Range ..... -65°C to 150°C
Output Short Circuit Duration (Note 3) ..... Indefinite
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.
Note 2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
Note 3. Continuous short circuit is allowed for case temperatures to 125°C and amient temperatures to 70°C.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 4)

Supply Voltage
- SG741 ..... ±5V to ±20V
- SG741C ..... ±5V to ±15V

Operating Ambient Temperature Range
- SG741 ..... -55°C to 125°C
- SG741C ..... 0°C to 70°C

Note 4. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise stated, these specifications apply for the operating ambient temperature of T_A = 25°C, V_{CC} = +15V, and V_{EE} = -15V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

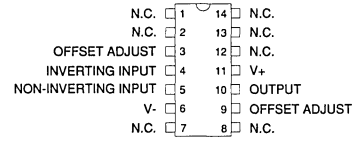
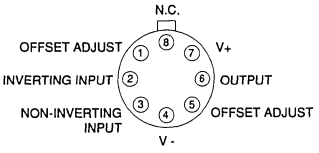
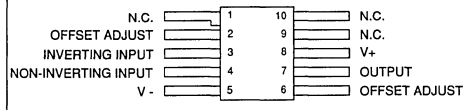
Parameter	Test Conditions	SG741			SG741C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	$R_S \le 10K\Omega$		1	5		2	6	mV
	$R_S \le 10K\Omega$, $T_A = T_{MIN}$ to T_{MAX}			6.0			7.5	mV
Input Offset Current			20	200		20	200	nA
Input Offset Current	T_A = 125°C			200				nA
	T_A = -55°C			500				nA
	0°C ≤ T_A ≤ 70°C						300	nA
Input Bias Current			80	500		80	500	nA
Input Bias Current	T_A = 125°C			500				nA
	T_A = -55°C			1500				nA
	0°C ≤ T_A ≤ 70°C						800	nA
Input Resistance (Note 5)		0.3	2		0.3	2		MΩ
Supply Current			1.7	2.8		1.7	2.8	mA
Input Noise Voltage	f = 10Hz		$5x10^{-16}$			$5x10^{-16}$		V^2/Hz
	f = 100KHz		$2x10^{-16}$			$2x10^{-16}$		V^2/Hz

Note 5. These parameters, although guaranteed, are not tested in production.

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG741			SG741C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Large Signal Voltage Gain	$V_S = \pm15$, $V_{OUT} = \pm10V$, $R_L \geq 2K\Omega$							
	$T_A = T_{MIN}$ to T_{MAX}	25			15			V/mV
	$T_A = 25°C$	50	160		25	160		V/mV
Output Voltage Swing	$V_S = \pm15$, $R_L = 10K\Omega$	±12	±14		±12	±14		V
	$R_L = 2K\Omega$	±10	±13		±10	±13		V
Input Voltage Range	$T_A = T_{MIN}$ to T_{MAX}	±12			±12			V
Common Mode Rejection Ratio	$T_A = T_{MIN}$ to T_{MAX}	80	96		80	96		dB
Supply Voltage Rejection Ratio	$R_S \leq 10K\Omega$, $T_A = T_{MIN}$ to T_{MAX}			150			150	µV/V

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN CERAMIC DIP J - PACKAGE	SG741J/883B SG741J SG741CJ	-55°C to 125°C -55°C to 125°C 0°C to 70°C	
14-PIN PLASTIC DIP N - PACKAGE	SG741CN	0°C to 70°C	
8-PIN METAL CAN T - PACKAGE	SG741T/883B SG741T SG741CT	-55°C to 125°C -55°C to 125°C 0°C to 70°C	
10-PIN CERAMIC FLAT PACK F - PACKAGE	SG741F/883B SG741F	-55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

3.5 AMP POWER OP AMP

DESCRIPTION

The SG1173 is a power monolithic operational amplifier capable of operating with loads to 3.5A with a power supply range to ±24V. Thermal shutdown and current limit have been provided to insure reliable operation during heavy loading. In addition, the SG1173's high common mode rejection, low input offsets, and high open loop gain rival those of much lower power op amps. Another important feature not provided by competitive power amps is the low quiescent current enabling significant power savings under no load conditions.

The SG1173 is ideal for use with voice coils in Winchester disk drives and other linear servo applications required by the automotive and military industries.

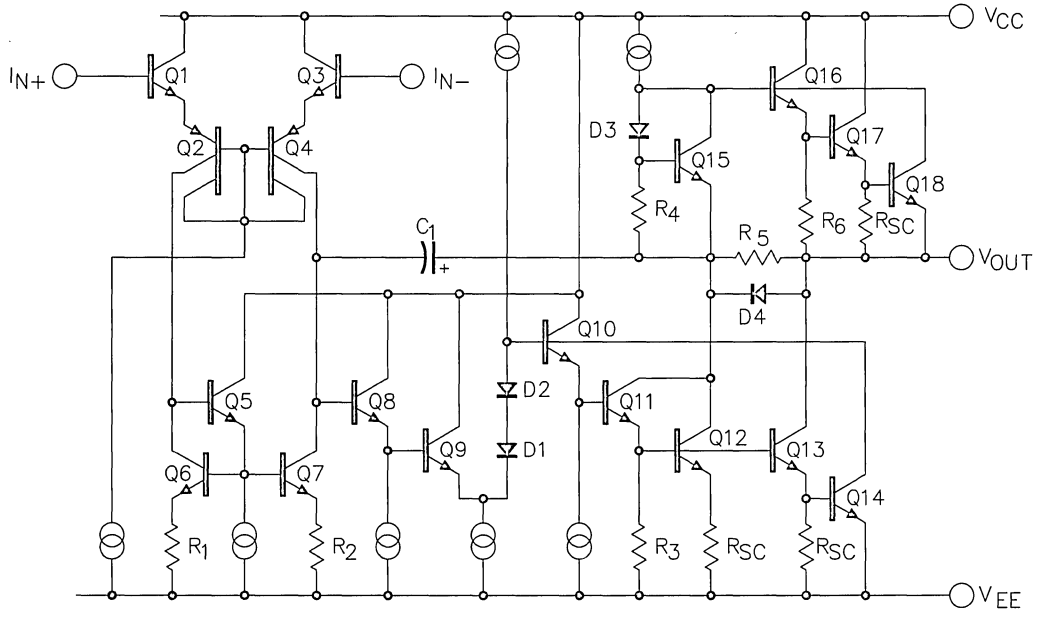
FEATURES

- **Low quiescent current**
- **3.5A output current**
- **Supply voltage range from ±5V to ±24V**
- **Internally compensated**
- **Thermal shutdown protection**
- **Current limit protection**
- **Functional replacements for ULN3751, L165, and LM675**
- **Available in TO-220, TO-66 packages**

HIGH RELIABILITY FEATURES - SG1173

- ◊ **Available to MIL-STD-883**
- ◊ **SG level "S" processing available**

EQUIVALENT CIRCUIT SCHEMATIC



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ABSOLUTE MAXIMUM RATINGS (Note 1)

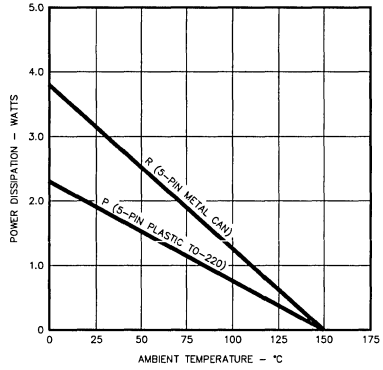
Positive Supply Voltage (V_{CC}) 25V
Negative Supply Voltage (V_{EE}) ..... -25V
Differential Input Voltage (Note 2) ..... ±50V
Common Mode Voltage (Note 2) ..... ±25V
Output Current ..... ±4A

Note 1. Exceeding these ratings could cause damage to the device. All voltages are with respect to ground. All currents are positive into the specified terminal.

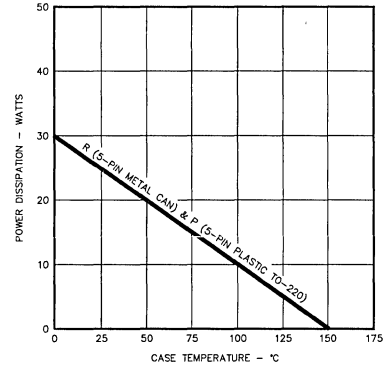
Operating Junction Temperature
Hermetic (R-Package) ..... 150°C
Plastic (P-Package) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 2. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 3)

Supply Voltage Range (V_{CC}) ..... +5V to +24V
Supply Voltage Range (V_{EE}) ..... -5V to -24V
Output Current (Continuous) ..... ±3.5A

Note 3. Range over which the device is functional.

Operating Ambient Temperature Range
SG1173 ..... -55°C to 125°C
SG2173 ..... -45°C to 85°C
SG3173 ..... 0°C to 70°C

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over full operating ambient temperatures for SG1173 with -55°C ≤ T_A ≤ 125°C, SG2173 with -25°C ≤ T_A ≤ 85°C, SG 3173 with 0°C ≤ T_A ≤ 70°C, V_{CC} = +15V, and V_{EE} = -15V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1173/2173			SG3173			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Voltage Range		±5		±24	±5		±24	V
Quiescent Drain Current	I_{OUT} = 0		10	20		10	20	mA
Input Offset Voltage	V_{OUT} = 0V, I_{OUT} = 0			10			10	mV
	T_A = 25°C		2	8		2	8	mV
Input Bias Current	V_{OUT} = 0V, I_{OUT} = 0			1000			1000	nA
	T_A = 25°C			500			500	nA
Input Offset Current	V_{OUT} = 0V, I_{OUT} = 0			250			250	nA
	T_A = 25°C			200			200	nA
Output Voltage Swing	I_{OUT} = -2A			2.8			2.8	V
	T_A = 25°C			3.5			3.5	V
	I_{OUT} = +2A			5.5			5.5	V
	T_A = 25°C			6.5			6.5	V
Current Limit	V_{OUT} = 0V		5			5		A
Common Mode Rejection Ratio	ΔV_{CM} = ±10V	70			70			dB
Power Supply Rejection Ratio	ΔV_{CC}, ΔV_{EE} = ±5V	74			74			dB
Open Loop Voltage Gain	I_{OUT} = 0A	75			75			dB
	T_A = 25°C	80			80			dB
Slew Rate			0.5			0.5		V/µs
Gain Bandwith Product			600			600		KHz
Thermal Shutdown			175			175		°C

CHARACTERISTIC CURVES

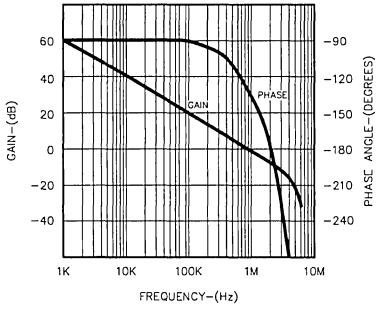


FIGURE 1.
FREQUENCY RESPONSE

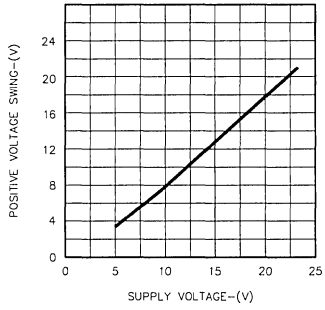


FIGURE 2.
POSITIVE VOLTAGE SWING VS. SUPPLY VOLTAGE

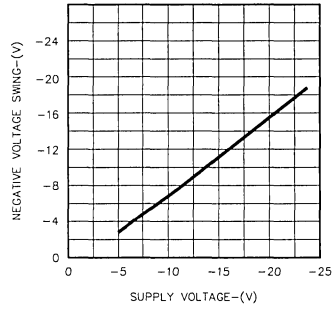


FIGURE 3.
NEGATIVE VOLTAGE SWING VS. SUPPLY VOLTAGE

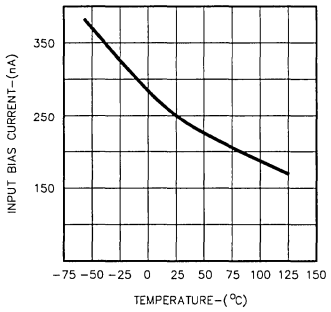


FIGURE 4.
INPUT BIAS CURRENT VS. TEMPERATURE

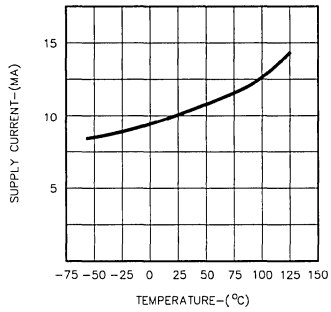


FIGURE 5.
SUPPLY CURRENT VS. TEMPERATURE

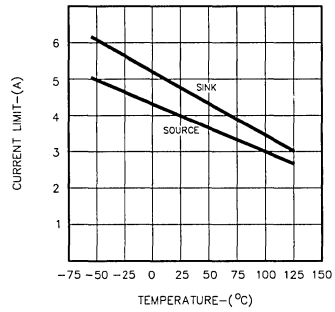


FIGURE 6.
CURRENT LIMIT VS. TEMPERATURE

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APPLICATION INFORMATION

General usage of the SG1173 requires the same design and layout considerations used with other op amps. Power supplies should be adequately bypassed and clamped with Zener diodes if transients are a problem. Leads to high impedance nodes should be kept as short as possible to minimize undesirable input-output coupling or RF pick-up. In addition to these, the high current capability of the SG1173 presents some new challenges that a designer must be aware of. Special care should be taken to avoid spurious feedback due to ground loops or voltage drops in high current paths. Kelvin connections should be used when applicable. When driving inductive loads, protection diode must be used to clamp the output voltage to the power supplies (Figure 7). This protects the amplifier from high voltage transients caused by the stored energy in the inductor. Some loads may require external load compensation. Examples of this are shown in Figures 8 and 9. Safe operating area (SOA) is another area where extreme care must be used. Simultaneous conditions of high current and high voltage on the part may cause the junction temperature to exceed the maximum rating. In any application, the worst case power dissipations should be calculated and adequate heat sinking must be provided.

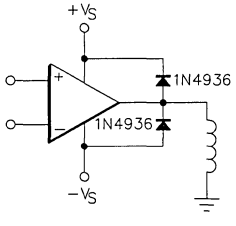


FIGURE 7 - PROTECTION DIODES USED WITH INDUCTIVE LOAD

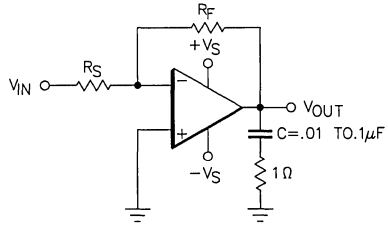


FIGURE 8 - INVERTING AMPLIFIER WITH RC LOAD COMPENSATION

APPLICATION INFORMATION (continued)

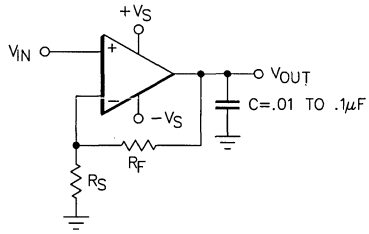


FIGURE 9 - NON-INVERTING AMPLIFIER WITH CAPACITIVE LOAD COMPENSATION

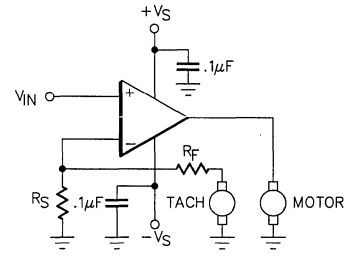


FIGURE 10 - MOTOR SPEED CONTROL WITH TACHOMETER FEEDBACK

A simple motor control loop is shown in Figure 10. This loop regulates the speed of the motor by using a tachometer to generate a voltage proportional to motor speed that is fed back to the amplifier. If the speed of the motor is S rpm and the proportionality constant of the tachometer is K volts/rpm then

$$S = V_{IN} \frac{(1 + R_F/R_S)}{K}.$$

The speed of the motor is set by the input voltage V_{IN} regardless of the load on the motor. This is because the action of the feedback loop forces the voltage on the motor to whatever value is required to maintain the desired speed. If it is shaft position rather than speed that needs to be regulated then the tachometer may be replaced by some type of shaft encoder that generates a voltage proportional to the position of the motor shaft. In this case the input voltage will set the shaft angle according to the relation

$$\omega = V_{IN} \frac{(1 + R_F/R_S)}{H}$$

where ω is shaft angle in degrees and H is the proportionality constant of the shaft encoder in volts/degree.

The new op amp has the capability to drive a loudspeaker directly allowing it to be used as an amplifier. Standard op amp configurations can be used to design amplifiers with particular values of closed loop gain or bandwidth. An example of such a circuit is shown in Figure 11. This circuit utilizes the op amp in a non-inverting gain configuration. The midband closed loop gain is set by R_F and R_S. The product of R_S and C_S set the lower 3dB frequency. The upper 3dB frequency is a function of the op amp's bandwidth and closed loop gain. A capacitor in parallel with R_S can be used to set the upper 3dB frequency to lower values if desired.

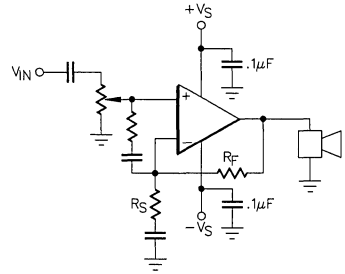
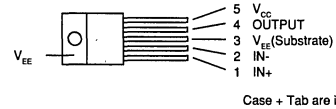
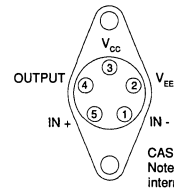


FIGURE 11 - AUDIO AMPLIFIER

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
5-PIN TO-220 PLASTIC P - PACKAGE	SG2173P SG3173P	-45°C to 85°C 0°C to 70°C	 Case + Tab are internally connected
5-PIN TO-66 METAL CAN R - PACKAGE	SG1173R/883B SG1173R SG2173R SG3173R	-55°C to 125°C -55°C to 125°C -45°C to 85°C 0°C to 70°C	 CASE IS GROUND Note: Case and tab are internally connected to substrate ground.

Note 1. Contact factory for JAN and DESC product availablity.

Note 2. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

HIGH-VOLTAGE OPERATIONAL AMPLIFIER

DESCRIPTION

The SG1536 series of monolithic amplifiers is designed specifically for use in high voltage applications up to ±40V and where high common-mode input ranges, high output voltage swings, and low input currents are required. These devices are internally compensated and are pin compatible with industry standard operational amplifiers.

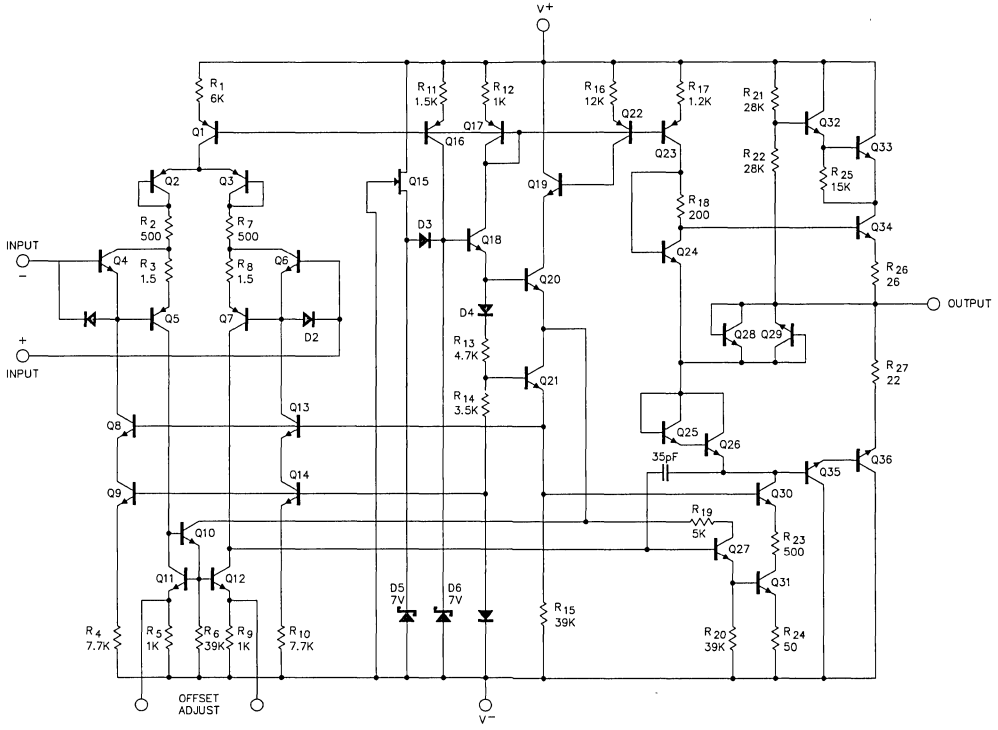
FEATURES

- **High supply voltage capability**
- **High output voltage swing**
- **High common-mode voltage range**
- **Internal frequency compensation**
- **Input current 35nA maximum over temperature**

HIGH RELIABILITY FEATURES -SG1536

- **Available to MIL-STD-883 and DESC SMD**
- **SG level "S" processing available**

CIRCUIT SCHEMATIC



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ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage
- SG1536 ..... ±40V
- SG1436 ..... ±34V

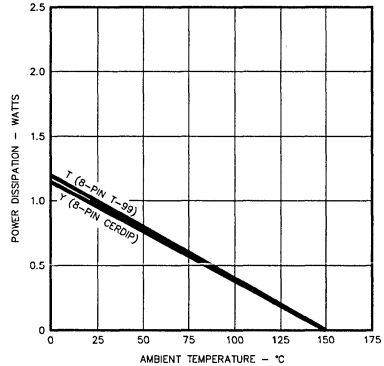
Differential Input Signal ..... $\pm(V^+ + |V^-| - 3)$ V
Common-Mode Input Swing ..... $\pm V^+, -(|V^-| - 3)$ V

Output Short Circuit Duration
($V^+ = |V^-| = 28V$, $V_O = 0V$) 5.0sec
Operating Junction Temperature
- Hermetic (T, Y-Package) ..... 150°C

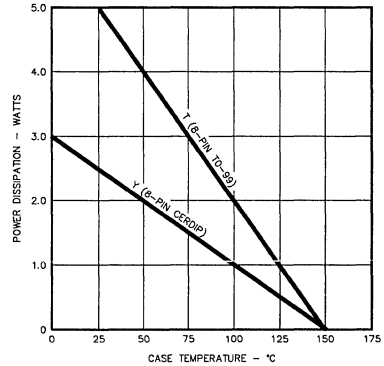
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage
- SG1536 ..... ±28V
- SG1436 ..... ±15V

Operating Ambient Temperature Range (T_J)
- SG1536 ..... -55°C to 125°C
- SG1436 ..... 0°C to 70°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply for the operating ambient temperature of $T_A = 25°C$, and $V_S = \pm 28V$. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1536			SG1436			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage			2.0	5.0		5.0	10	mV
	$T_A = T_{MIN}$ to T_{MAX}			7.0			14	mV
Input Offset Current			1.0	3.0		5.0	10	nA
	$T_A = T_{MIN}$			7.0			14	nA
	$T_A = T_{MAX}$			4.5			14	nA
Input Bias Current			8.0	20		15	40	nA
	$T_A = T_{MIN}$ to T_{MAX}			35			55	nA
Differential Input Impedance	Open loop, ≤ 5.0Hz		10			10		MΩ
Common-Mode Input Impedance	f ≤ 5.0Hz		250			250		MΩ
Common-Mode Input Voltage Range (Peak)		±24	±25		±22	±25		V
Common-Mode Rejection Ratio		80	110		70	100		dB
Large Signal Voltage Gain	$R_L = 10K\Omega, V_O = \pm 10V$		200K			200K		V/V
	$R_L = 100K\Omega, V_O = \pm 10V$	100K	500K		70K	500K		V/V
	$T_A = T_{MIN}$ to T_{MAX}	50K			50K			V/V
Power Supply Rejection Ratio	V^- constant, $R_S \leq 10K\Omega$		15	100		35	200	μV/V
	V^+ constant, $R_S \leq 10K\Omega$		15	100		35	200	μV/V
Output Impedance	f ≤ 5.0Hz		1.0			1.0		KΩ
Short Circuit Output Current			±17			±17		mA
Output Voltage Swing (Peak)	$R_L = 5.0$ KΩ, $V_S = \pm 28V$	±22			±22			V
	$R_L = 5.0$ KΩ, $V_S = \pm 36V$	±30			±30			V

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1536			SG1436			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Power Bandwidth	A_V = +1, R_L = 5.0KΩ, THD ≤ 5%, V_O = 40V p-p		23			23		KHz
Unity Gain Crossover Frequency	Open loop		1.0			1.0		MHz
Slew Rate	Unity gain		2.0			2.0		V/μs
Phase Margin	Open loop, unity gain		50			50		deg
Gain Margin			18			18		dB
Equivalent Input Noise	A_V = 100, R_S = 10KΩ, f = 1.0KHz, BW = 1.0 Hz		50			50		$nV/\sqrt{Hz}$
Power Supply Current			2.2	4.0		2.6	5.0	mA
Power Consumption	V_O = 0		124	224		146	280	mW

CHARACTERISTIC CURVES

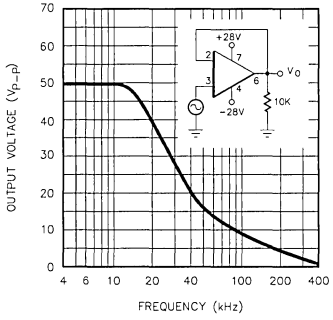


FIGURE 1.
POWER BANDWIDTH

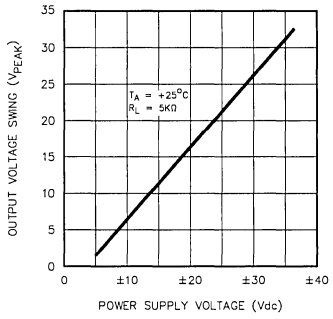


FIGURE 2.
PEAK OUTPUT VOLTAGE SWING VS.
POWER SUPPLY VOLTAGE

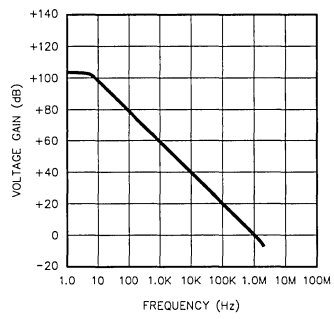


FIGURE 3.
OPEN-LOOP FREQUENCY RESPONSE

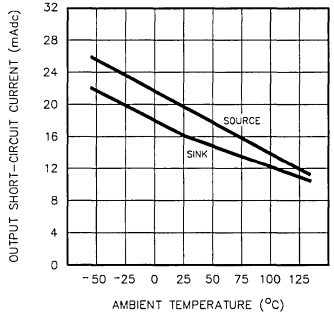


FIGURE 4.
OUTPUT SHORT-CIRCUIT CURRENT VS.
TEMPERATURE

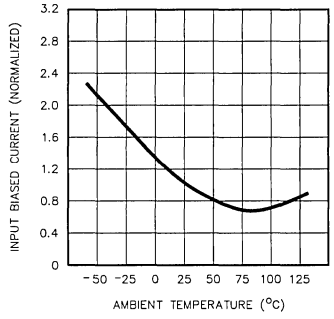


FIGURE 5.
INPUT BIAS CURRENT VS.
TEMPERATURE

TYPICAL APPLICATIONS

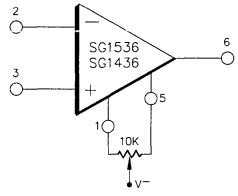


FIGURE 6 - VOLTAGE OFFSET NULL CIRCUIT

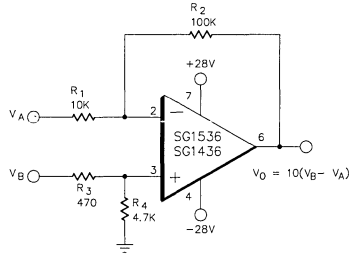


FIGURE 7 - DIFFERENTIAL AMPLIFIER WITH ±20V COMMON-MODE INPUT VOLTAGE RANGE

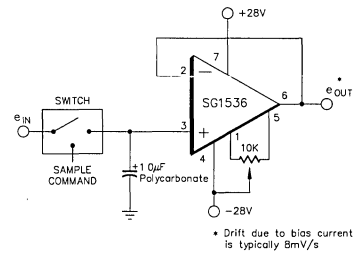


FIGURE 8 - LOW-DRIFT SAMPLE AND HOLD

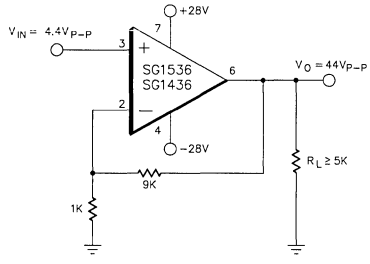


FIGURE 9 - TYPICAL NON-INVERTING X10 VOLTAGE AMPLIFIER

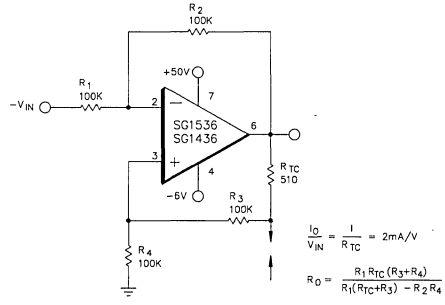
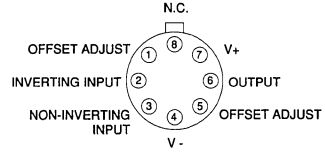
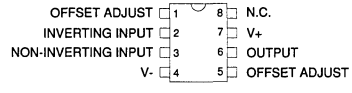


FIGURE 10 - VOLTAGE CONTROLLED CURRENT SOURCE OR TRANSCONDUCTANCE AMPLIFIER WITH 0 TO 40V COMPLIANCE

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
8-PIN METAL CAN T - PACKAGE	SG1536T/883B SG1536T SG1436T	-55°C to 125°C -55°C to 125°C 0°C to 70°C	
8-PIN CERAMIC DIP Y- PACKAGE	SG1536Y/883B SG1536Y SG1436Y	-55°C to 125°C -55°C to 125°C 0°C to 70°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SG2172/3172

ADVANCED DATA SHEET

3 AMP POWER OP AMP

DESCRIPTION

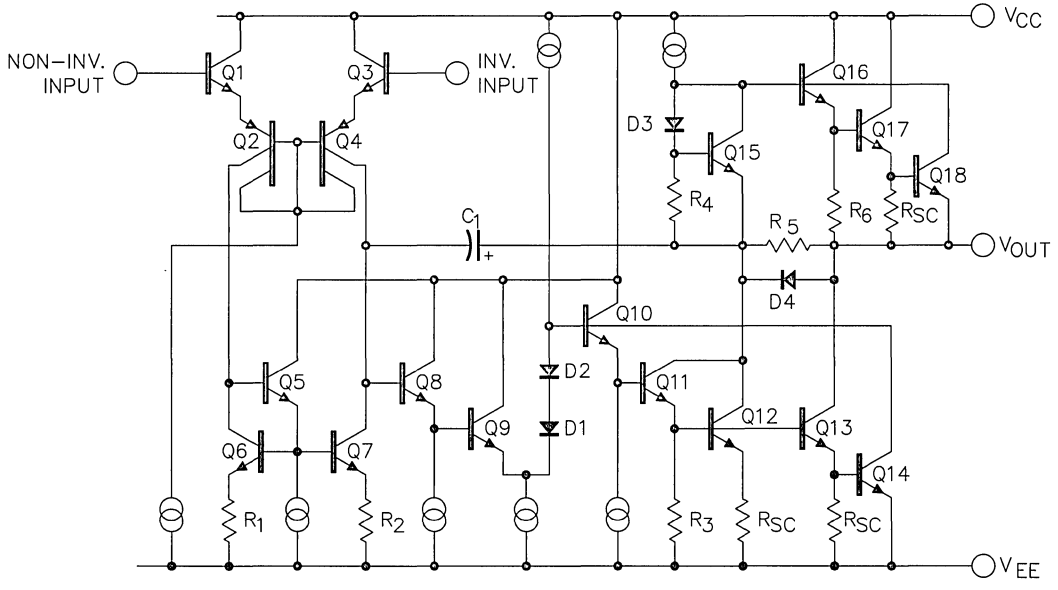
The SG2172/3172 is a power monolithic operational amplifier capable of operating with loads to 3A with a power supply range to 18V. Thermal shutdown and current limit have been provided to insure reliable operation during heavy loading. In addition, the SG2172/3172's high common mode rejection, low input offsets, and high open loop gain rival those of much lower power op amps. Another important feature not provided by competitive power amps is the low quiescent current (7mA typically) enabling significant power savings under no load conditions.

The SG2172/3172 is ideal for use with voice coils in Winchester disk drives and other linear servo applications.

FEATURES

- **Low quiescent current**
- **3.0A output current**
- **Supply voltage range from 10V to 18V**
- **Internally compensated**
- **Thermal shutdown protection**
- **Current limit protection**
- **Functional replacements for ULN3751, L165, and LM675**
- **Available in TO-220, TO-66 packages**

EQUIVALENT CIRCUIT SCHEMATIC



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ABSOLUTE MAXIMUM RATINGS (Note 1)

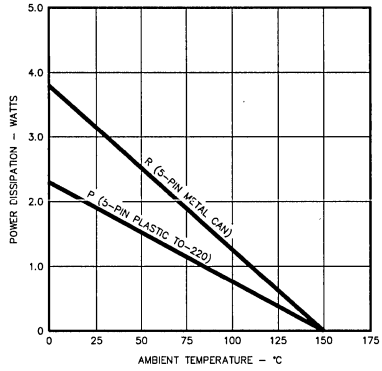
Supply Voltage (V_{CC}-V_{EE}) 20V
Differential Input Voltage (Note 2) ..... ±20V
Common Mode Voltage (Note 2) ..... ±10V
Output Current ..... ±3.5A

Operating Junction Temperature
Hermetic (R-Package) ..... 150°C
Plastic (P-Package) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

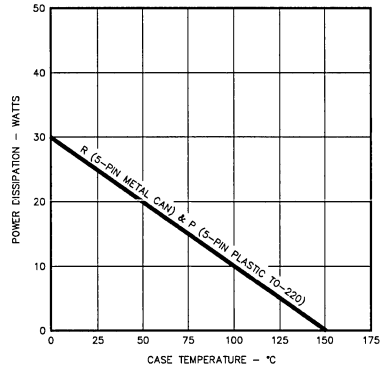
Note 1. Exceeding these ratings could cause damage to the device. All voltages are with respect to ground. All currents are positive into the specified terminal.

Note 2. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 3)

Supply Voltage Range (V_{CC}-V_{EE}) ..... 10V to 18V
Output Current (Continuous) ..... ±3.0A

Operating Ambient Temperature Range
SG2172 ..... -45°C to 85°C
SG3172 ..... 0°C to 70°C

Note 3. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG2172 with -45°C ≤ T_A ≤ 85°C, SG3172 with 0°C ≤ T_A ≤ 70°C, V_{CC} = 6V, and V_{EE} = -6V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG2172/3172			Units
		Min.	Typ.	Max.	
Supply Voltage Range	(V_{CC}-V_{EE})	10		18	V
Quiescent Drain Current	I_{OUT} = 0		7	12	mA
Input Offset Voltage	V_{OUT} = 0V, I_{OUT} = 0			10	mV
Input Bias Current	V_{OUT} = 0V, I_{OUT} = 0			1000	nA
	T_A = 25°C			500	nA
Input Offset Current	V_{OUT} = 0V, I_{OUT} = 0			250	nA
	T_A = 25°C			200	nA
Output Saturation Voltage	I_{OUT} = -2A, V_{CC} - V_{OUT}			2.5	V
	I_{OUT} = +2A, V_{OUT} - V_{EE}			3.2	V
Current Limit	V_{OUT} = 0V		5		A
Common Mode Rejection Ratio	ΔV_{CM} = 6V	70			dB
Power Supply Rejection Ratio	(V_{CC}-V_{EE}) = 10V to 14V	74			dB
Open Loop Voltage Gain	I_{OUT} = 0	80	110		dB
Slew Rate			0.5		V/µs
Gain Bandwith Product			600		KHz
Thermal Shutdown			175		°C

CHARACTERISTIC CURVES

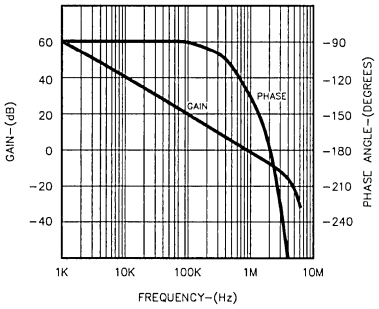


FIGURE 1.
FREQUENCY RESPONSE

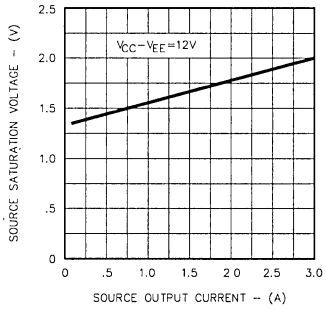


FIGURE 2.
SOURCE VOLTAGE VS. OUTPUT CURRENT

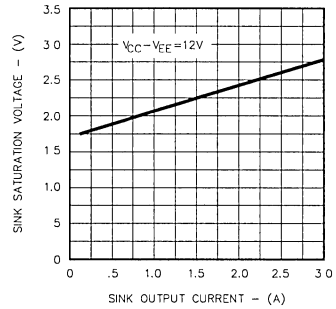


FIGURE 3.
SINK SATURATION VOLTAGE VS. OUTPUT CURRENT

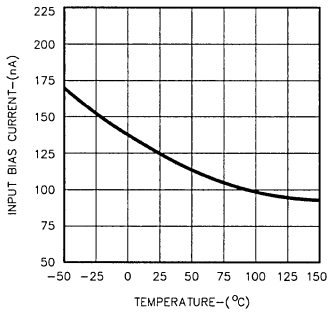


FIGURE 4.
INPUT BIAS CURRENT VS. TEMPERATURE

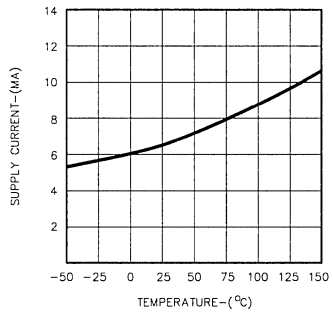


FIGURE 5.
SUPPLY CURRENT VS. TEMPERATURE

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APPLICATION INFORMATION

General usage of the SG2172/3172 requires the same design and layout considerations used with other op amps. Power supplies should be adequately bypassed and clamped with Zener diodes if transients are a problem. Leads to high impedance nodes should be kept as short as possible to minimize undesirable input-output coupling or RF pick-up. In addition to these, the high current capability of the SG2172/3172 presents some new challenges that a designer must be aware of. Special care should be taken to avoid spurious feedback due to ground loops or voltage drops in high current paths. Kelvin connections should be used when applicable. When driving inductive loads, protection diodes must be used to clamp the output voltage to the power supplies (Figure 7). This protects the amplifier from high voltage transients caused by the stored energy in the inductor. Some loads may require external load compensation. Examples of this are shown in Figures 8 and 9. Safe operating area (SOA) is another area where extreme care must be used. Simultaneous conditions of high current and high voltage on the part may cause the junction temperature to exceed the maximum rating. In any application, the worst case power dissipations should be calculated and adequate heat sinking must be provided.

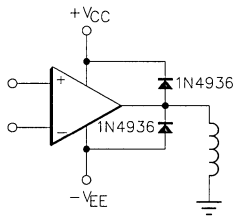


FIGURE 7 - PROTECTION DIODES USED WITH INDUCTIVE LOAD

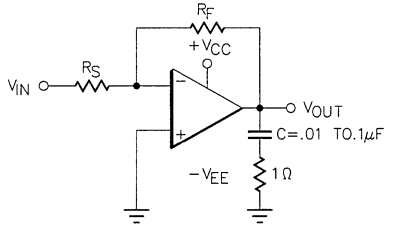


FIGURE 8 - INVERTING AMPLIFIER WITH RC LOAD COMPENSATION

APPLICATION INFORMATION (continued)

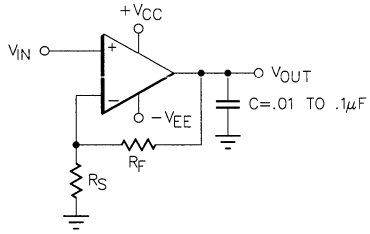


FIGURE 9 - NON-INVERTING AMPLIFIER WITH CAPACITIVE LOAD COMPENSATION

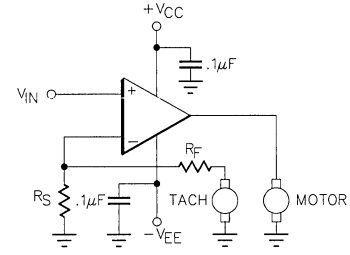


FIGURE 10 - MOTOR SPEED CONTROL WITH TACHOMETER FEEDBACK

A simple motor control loop is shown in Figure 10. This loop regulates the speed of the motor by using a tachometer to generate a voltage proportional to motor speed that is fed back to the amplifier. If the speed of the motor is S rpm and the proportionality constant of the tachometer is K volts/rpm then

$$S = V_{IN} \frac{(1 + R_F/R_S)}{K}.$$

The speed of the motor is set by the input voltage V_{IN} regardless of the load on the motor. This is because the action of the feedback loop forces the voltage on the motor to whatever value is required to maintain the desired speed. If it is shaft position rather than speed that needs to be regulated then the tachometer may be replaced by some type of shaft encoder that generates a voltage proportional to the position of the motor shaft. In this case the input voltage will set the shaft angle according to the relation

$$\omega = V_{IN} \frac{(1 + R_F/R_S)}{H}$$

where ω is shaft angle in degrees and H is the proportionality constant of the shaft encoder in volts/degree.

The new op amp has the capability to drive a loudspeaker directly allowing it to be used as an amplifier. Standard op amp configurations can be used to design amplifiers with particular values of closed loop gain or bandwidth. An example of such a circuit is shown in Figure 11. This circuit utilizes the op amp in a non-inverting gain configuration. The midband closed loop gain is set by R_F and R_S. The product of R_S and C_S set the lower 3dB frequency. The upper 3dB frequency is a function of the op amp's bandwidth and closed loop gain. A capacitor in parallel with R_S can be used to set the upper 3dB frequency to lower values if desired.

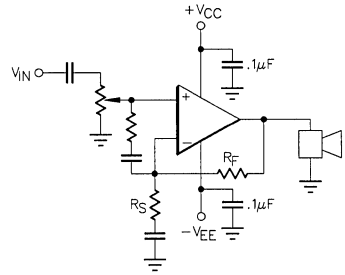
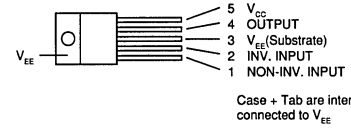
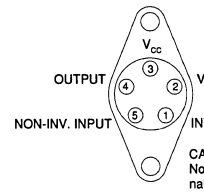


FIGURE 11 - AUDIO AMPLIFIER

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
5-PIN TO-220 PLASTIC P - PACKAGE	SG2172P SG3172P	-45°C to 85°C 0°C to 70°C	 Case + Tab are internally connected to V_{EE}
5-PIN TO-66 METAL CAN R - PACKAGE	SG2172R SG3172R	-45°C to 85°C 0°C to 70°C	 CASE IS V_{EE} Note: Case and tab are internally connected to the chip substrate ground, V_{EE}.

Note 1. Contact factory for JAN and DESC product availablity.

Note 2. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SG3272

ADVANCED DATA SHEET

DUAL POWER OPERATIONAL AMPLIFIER

DESCRIPTION

The SG3272 is a monolithic dual-power operational amplifier which features a high current, low saturation voltage, flyback protected output stage optimized for driving heavy inductive loads. Capable of operation in a single supply mode from as low as 4.5V up to 13.2V, the SG3272 is ideally suited for the computer peripheral environment, driving small motors, solenoids, and linear actuators in an H-bridge configuration.

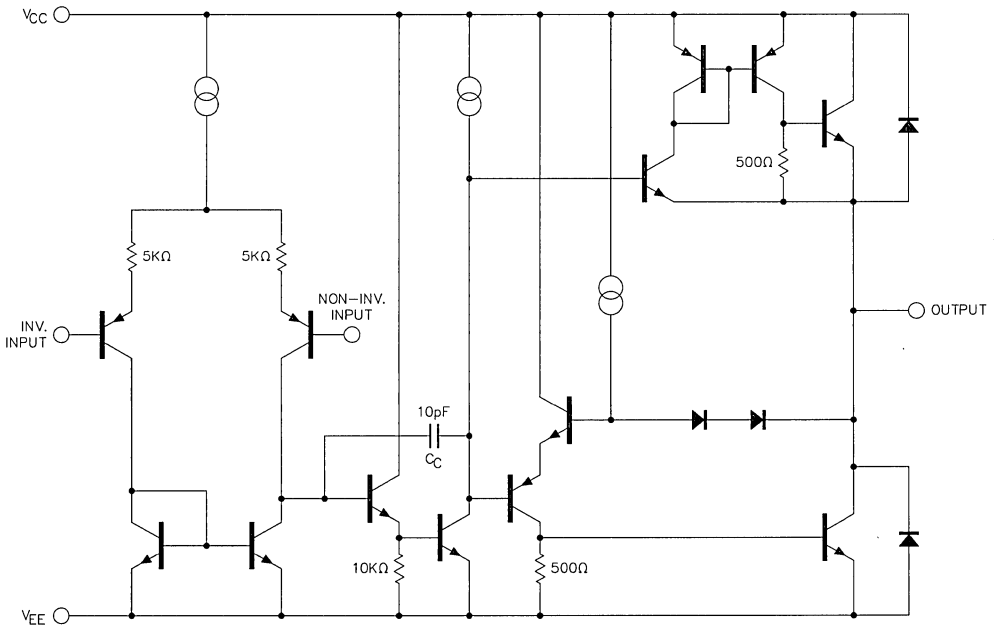
As a general-purpose op amp, the SG3272 exhibits low input offset voltage, high open loop gain, low quiescent current, a large differential input voltage range, and a common-mode input voltage range which includes ground (V_{EE}).

Available in either an 8-pin plastic DIP package or a wide-body 20-pin batwing SOIC, the SG3272 provides system designers with a low-cost, convenient way to minimize power dissipation and reduce board area consumption in applications requiring high current inductive load drive capability.

FEATURES

- **Full output swing at ±500mA**
- **High inductive load drive capability**
- **Internal flyback protection diodes**
- **Low power dissipation**
- **Single or split supply operation**
- **Common-mode range includes ground (V_{EE})**
- **High open loop gain**
- **Low input offset voltage**
- **Large differential input voltage range**
- **Thermal shutdown protection**
- **Available in 8-pin mini-DIP and 20-pin batwing SOIC**

EQUIVALENT CIRCUIT SCHEMATIC



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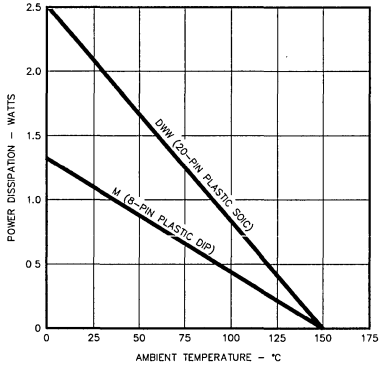
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Single Supply) (V_{CC}) ..... -0.3V to 14V
DC Output Current (I_{OUT}) ..... ±1.0A
Peak Output Current (Non-Repetitive) (I_{OUT}) ..... ±1.5A
Common-Mode Input Voltage (V_{ICM}) ..... -0.3V to V_{CC}-2V
Differential-Mode Input Voltage (V_{IDM}) ..... ±V_{CC}

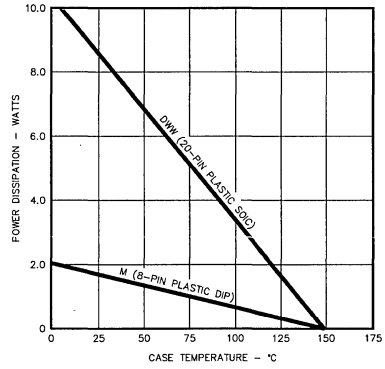
Operating Junction Temperature
Plastic (M-, DW-Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceedingthese ratings could cause damage to the device. All voltages are with respect to ground. All currents are positive into the specified terminal.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage (Single Supply) (V_{CC}) ..... 4.5V to 13.2V
DC Output Current (I_{OUT}) ..... ±500mA
Common-Mode Input Voltage (V_{ICM}) ..... 0V to V_{CC}-2V

Differential-Mode Input Voltage (V_{IDM}) ..... ±V_{CC}
Operating Ambient Temperature Range
SG3272 ..... 0°C to 70°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply for the operating ambient temperature of T_A = 25°C and V_{CC} = 12V. Low duty cycle testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG3272			Units
		Min.	Typ.	Max.	
Static Characteristics					
Input Offset Voltage (V_{IO})		-15	0	15	mV
	$T_A = T_{MIN}$ to T_{MAX}	-30		30	mV
Input Bias Current (I_B)		-1.0	-0.2		µA
Input Offset Current (I_{OS})		-50		50	nA
	$T_A = T_{MIN}$ to T_{MAX}	-200		200	nA
Differential Input Resistance (R_{ID})		500			KΩ
Source Side Output Saturation Voltage (+V_{SAT})	I_{OUT} = -100mA		0.8		V
	I_{OUT} = -500mA		1.0	1.5	V
Sink Side Output Saturation Voltage (-V_{SAT})	I_{OUT} = -100mA		0.3		V
	I_{OUT} = -500mA		0.6	1.0	V
Open Loop Voltage Gain (A_{VOL})		70	90		dB
Common-Mode Rejection Ratio (CMRR)		66	90		dB
Power Supply Rejection Ratio (PSRR)		60	80		dB
Quiescent Drain Current (I_{CC})			7	15	mA
Thermal Shutdown Temperature			175		°C

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG3272 Min.	SG3272 Typ.	SG3272 Max.	Units
Dynamic Characteristics					
Gain Bandwidth Product (GBWP)	$R_L = \infty\Omega$		800		KHz
Slew Rate (dV_O/dt)	AV = 1		1.6		V/μs
Power Bandwidth, -3dB (PBW)			200		KHz
Input Noise Voltage (E_N)	22Hz to 22KHz		10		μV
Input Noise Current (I_N)	22Hz to 22KHz		200		pA
Channel Separation (C_S)	f = 1KHz, R_L = 10Ω, AV_{CL} = 30dB		60		dB

CHARACTERISTIC CURVES

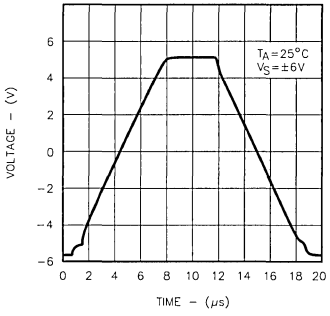


FIGURE 1.
LARGE SIGNAL TRANSIENT RESPONSE

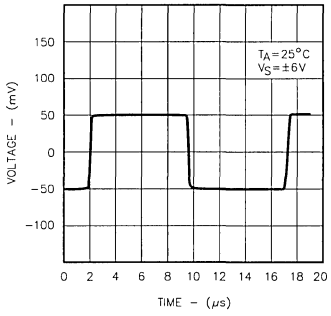


FIGURE 2.
SMALL SIGNAL TRANSIENT RESPONSE

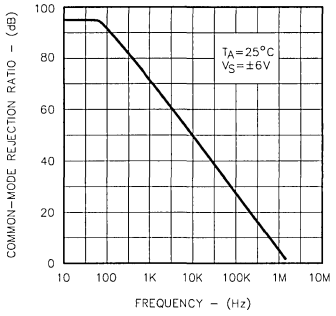


FIGURE 3.
COMMON-MODE REJECTION RATIO VS. FREQUENCY

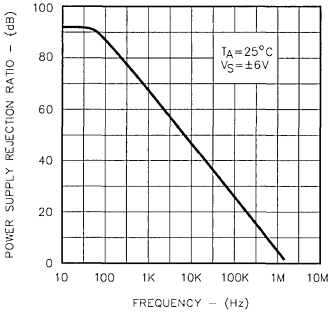


FIGURE 4.
POWER SUPPLY REJECTION VS. FREQUENCY

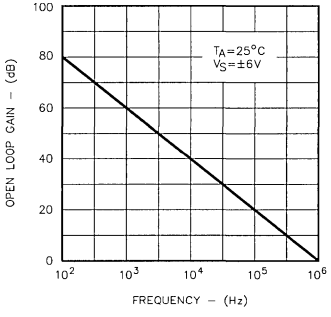


FIGURE 5.
OPEN LOOP GAIN VS. FREQUENCY

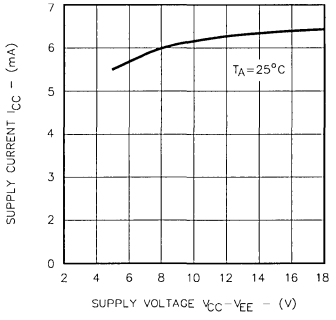


FIGURE 6.
SUPPLY CURRENT VS. SUPPLY VOLTAGE

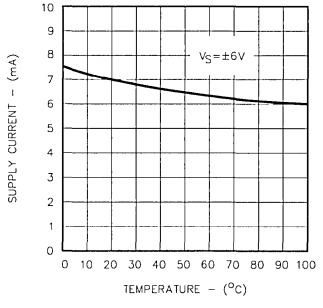


FIGURE 7.
SUPPLY CURRENT VS. TEMPERATURE

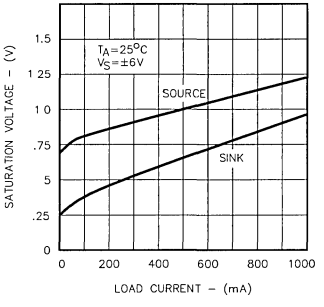


FIGURE 8.
SATURATION VOLTAGE VS. LOAD CURRENT

APPLICATION CIRCUIT

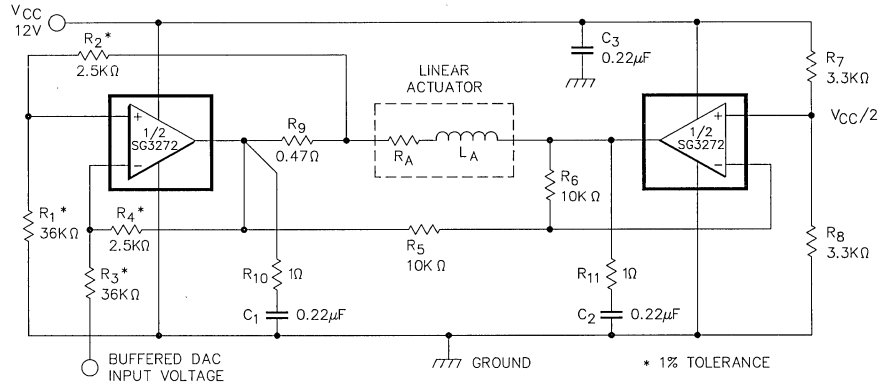
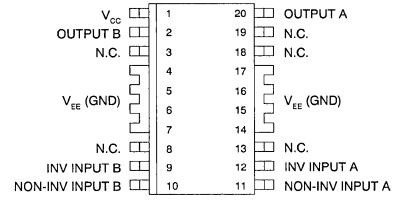


FIGURE 9 - 3.5-INCH WINCHESTER DISK DRIVE HEAD POSITION CONTROL AMPLIFIER

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
8-PIN PLASTIC M - PACKAGE	SG3272M	0°C to 70°C	
20-PIN PLASTIC WIDEBODY BATWING S.O.I.C. DWW - PACKAGE	SG3272DWW	0°C to 70°C	

Note 1. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SELECTION GUIDE
CORE MEMORY

SENSE AMPLIFIER

Device Type	Description	Key Features	Packages
SG5524	Dual sense amplifier	• Adjustable input threshold level • High speed • TTL or DTL drive compatibility • Standard logic supply voltage	J, F
SG5534	Dual sense amplifier	• Adjustable input threshold level • High speed • TTL or DTL drive compatibility • Supply Currents - $(+I_{CC}) < -20mA$ - $(-I_{CC}) < 18mA$	J
SG55234 SG55234A	Dual sense amplifier	• Adjustable input threshold level • High speed • TTL or DTL drive compatibility • Standard logic supply voltage • Threshold voltage matching (ΔV_{TH}): SG55234 3mV SG55234A 1.5mV	J, F
SG55236 SG55236A	Dual sense amplifier / data registers	• Threshold voltage matching (ΔV_{TH}): SG55236 1.5mV SG55235A 0.8mV • Adjustable differential-input threshold voltage • Reference amplifier inherently stable with no external frequency compensation required • Built-in data buffer drives 450pF load in 15ns • Internal reference voltage attenuator makes reference amplifier less sensitive to noise	F

January 1990

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SELECTION GUIDE
CORE MEMORY

MEMORY DRIVERS

Device Type	Description	$I_{O(PK)}$	$I_{O(CONT)}$	V_C	V_{CC} #1	V_{CC} #2	Key Features	Packages
SG55325 SG75325	Dual source/ Dual sink memory driver	0.75A	0.6A	24V	7V	24V	• Two open emitter, two open collector output stages • Output clamp circuitry on sink transistors • Source base drive externally adjustable • Fast switching time • TTL or DTL compatibility • MIL-M-38510 / 13001 BEA QPL JAN55325J	J, N, F
SG55326 SG75326	Quad sink memory driver	0.75A	0.6A	24V	7V		• Four open collector output stages • Output clamp circuitry on all outputs • Output transistor base drives externally adjustable • Fast switching time • TTL or DTL compatibility • MIL-M-38510 / 13002 BEA QPL JAN 55326J	J, N, F
SG55327 SG75327	Quad source memory driver	0.75A	0.6A	24V	7V	24V	• Four open emitter output stages • Can operate as a sink driver • Output transistor base drives externally adjustable • Fast switching time • TTL or DTL compatibility	J, N, F

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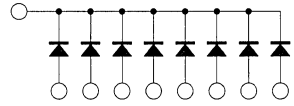
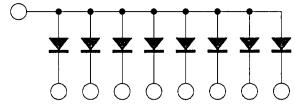
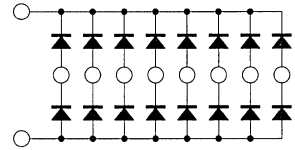
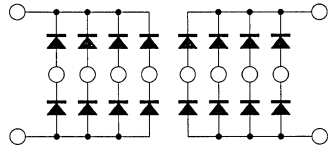
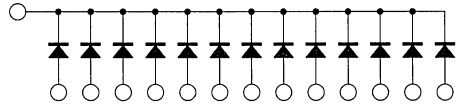
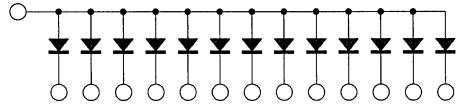
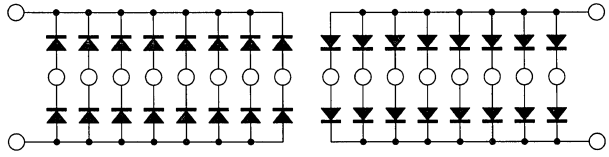
December 1988

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

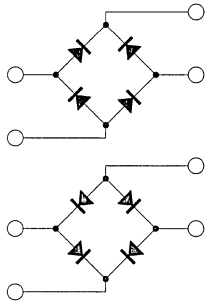
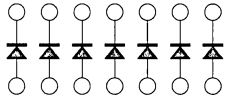
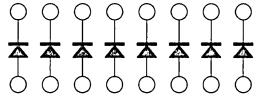
SELECTION GUIDE
CORE MEMORY

DIODE ARRAYS

Device Type	Circuit Diagram	Key Features
SG5768/5768A		• 60V minimum breakdown voltage • 500mA current capability per diode • Maximum reverse recovery time (t_{rr}) of 20ns • Maximum forward recovery time (t_{fr}) of 40ns • Reverse current (I_R) < 100nA • JANTXV, JANTX & JAN parts available • SG level "S" processing available • MIL-S-19500/474 QPL parts available 1N5768 1N5770 1N5772 • Available in hermetic ceramic DIP (J) and flat (F) packages
SG5770/5770A		
SG5772/5772A		
SG5774/5774A		
SG25768		
SG25770		
SG6496/6496A		

December 1989

DIODE ARRAYS

Device Type	Circuit Diagram	Key Features
SG3212		• 60V minimum breakdown voltage • 1A current capability per diode • Fast switching speeds: typically less than 15ns • Low leakage current
SG6100		• 75V minimum breakdown voltage • 100mA current capability per diode • Switching speeds less than 5ns • Low leakage current < 25nA
SG6101		

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

DUAL DIODE BRIDGE

DESCRIPTION

The Silicon General dual diode bridge features high breakdown and low forward voltage .

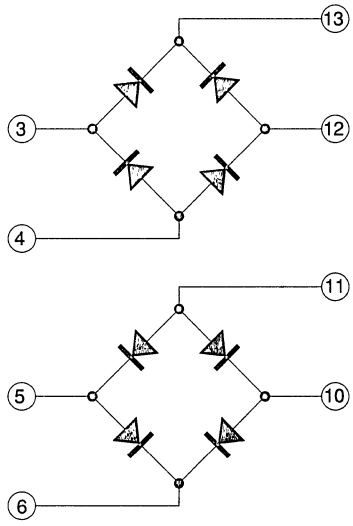
Individual diodes within the bridge have 60V minimum breakdown voltage, can handle 1A of current and typically switch in less than 15 nanoseconds.

The dual bridge configuration is available in ceramic DIP or ceramic flatpack and can be processed to JANTXV, JANTX, or JAN flows at Silicon General's MIL-S-19500 facility.

FEATURES

- **60V minimum breakdown voltage**
- **1A current capability per diode**
- **Fast switching speeds: typically less than 15ns**
- **Low leakage current**

CIRCUIT DIAGRAM



April 1990

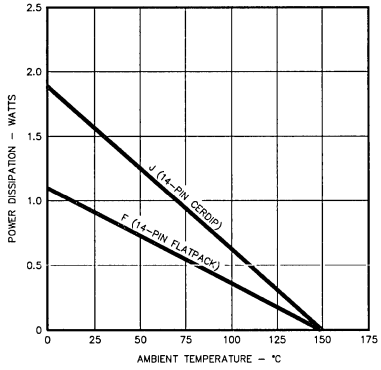
ABSOLUTE MAXIMUM RATINGS (Note 1 & 2)

Breakdown Voltage (V_{BR}) 60V
Output Current (I_O), T_C = 25°C
Continuous 1A

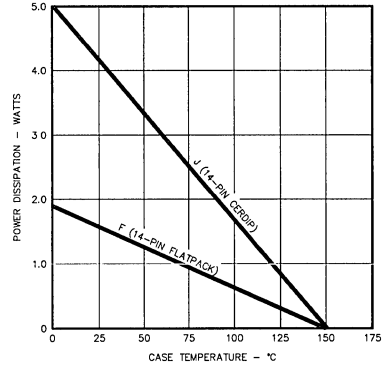
Operating Junction Temperature
Hermetic (J, F Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 200°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.
Note 2. Applicable for each diode.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 3)

Operating Ambient Temperature Range
SG3212 ..... -55°C to 150°C

Note 3. Range over which the device is functional.

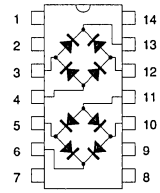
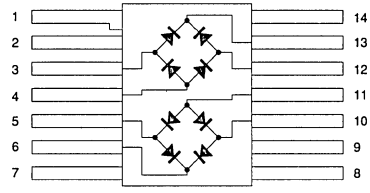
ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply for the operating ambient temperature of T_A = 25°C for each diode. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG3212			Units
		Min.	Typ.	Max.	
Breakdown Voltage (V_{BR})	I_R = 10µA	60	75		V
Forward Voltage (V_F)	Duty Cycle ≤ 2%, 300 µs pulse				
	I_F = 1mA			0.62	V
	I_F = 10mA			0.74	V
	I_F = 100mA			0.92	V
	I_F = 200mA			1.0	V
	I_F = 500mA			1.2	V
	I_F = 1A			1.5	V
	I_F = 10mA, T_A = -55°C			1.0	V
Reverse Current (I_R)	V_R = 40V		15	100	nA
	V_R = 40V, T_A = 150°C		2	50	µA
Capacitance (C) (Note 4)	V_R = 0V, f = 1MHz, Pin-to-pin			9	pf
Forward Recovery Time (t_{fr}) (Note 4)	I_F = 500mA, t_r ≤ 15ns, V_{fr} = 1.8V, R_S = 50Ω		10	40	ns
Reverse Recovery Time (t_{rr}) (Note 4)	I_F = I_R = 200mA, i_{rr} = 20mA, R_L = 100Ω		7	20	ns

Note 4. The parameters, although guaranteed, are not 100% tested in production.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN CERAMIC DIP J - PACKAGE	SG3212J/883B SG3212J	-55°C to 150°C -55°C to 150°C	
14-PIN CERAMIC FLATPACK F - PACKAGE	SG3212F/883B SG3212F	-55°C to 150°C -55°C to 150°C	

Note 1. Consult factory for other packages available.
2. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

DUAL SENSE AMPLIFIER

DESCRIPTION

The SG5524 is a monolithic, dual channel sense amplifier designed for high speed magnetic memory systems. The sense amplifier inputs can detect low-level differential signals. An adjustable input threshold level (V_{REF}) allows the designer to tailor the device to suit a specific application. The outputs are TTL/DTL compatible and feature separate strobes for individual channel control.

The SG5524 is characterized over the full military ambient temperature range of -55°C to 125°C and is available in both 16-pin ceramic DIP and 16-pin flatpack packages.

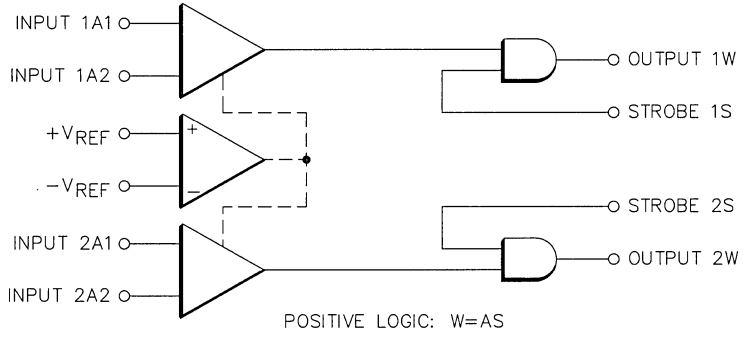
FEATURES

- **Adjustable input threshold voltage**
- **High speed**
- **TTL or DTL drive compatibility**
- **Standard logic supply voltage**

HIGH RELIABILITY FEATURES - SG5524

- **Available to MIL-STD-883**
- **SG level "S" processing available**

BLOCK DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUT
A	S	W
H	H	H
L	X	L
X	L	L

Definition of Logic Levels

INPUT	H	L	X
A*	$V_{ID} \geq V_{T\ MAX}$	$V_{ID} \leq V_{T\ MIN}$	Irrelevant
S	$V_I \geq V_{IH\ MIN}$	$V_I \leq V_{IL\ MAX}$	Irrelevant

* A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

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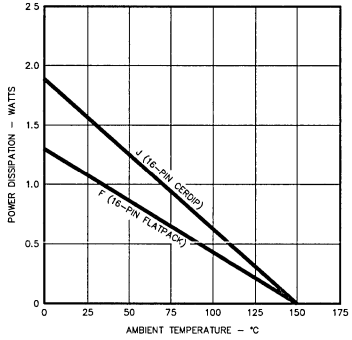
ABSOLUTE MAXIMUM RATINGS (Note1)

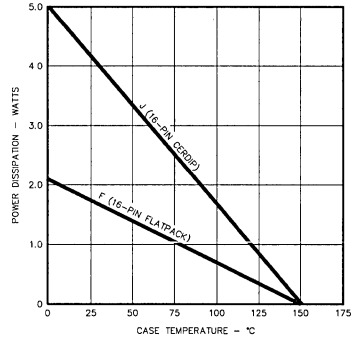
Supply Voltage ($+V_{CC}$) (Note 2) 7.0V
Supply Voltage ($-V_{CC}$) (Note 2) ..... -7.0V
Differential Input Voltage ..... ±5V
Voltage From Any Input to Ground (Note 3) 5.5V
Off-state Voltage Applied to Open-Collector Outputs 5.5V
Storage Temperature Range ..... -65°C to 150°C
Operating Junction Temperature (T_C)
Hermetic (J, F-Packages) ..... 150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1. Values beyond which damage may occur.
Note 2. Voltage values, except differential voltages, are with respect to network ground terminals.
Note 3. Strobe and gate input voltages must be zero or positive with respect to network ground terminal.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 4)

Supply Voltage ($+V_{CC}$) ..... 4.75V to 5.25V
Supply Voltage ($-V_{CC}$) ..... -4.75V to -5.25V
Reference Voltage (V_{REF}) .....15mV to 40mV
Operating Ambient Temperature Range:
SG5524 .....-55°C to 125°C

Note 4. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG5524 with $-55°C \le T_A \le 125°C$, $+V_{CC} = 5V$, and $-V_{CC} = -5V$. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG5524			Units
		Min.	Typ.	Max.	
Static Section					
Differential Input Threshold Voltage (V_T)	V_{REF} = 15mV	10	15	20	mV
	V_{REF} = 40mV	35	40	45	mV
Common Mode Input Firing Voltage (V_{ICF}) (Note 5)	V_{REF} = 40 mV, $V_{I(S)} = V_{IH}$, T_A = 25°C Common Mode input pulse:				
	$t_r \le 15ns$, $t_f \le 15ns$, $t_w \le 50ns$		±2.5		V
Differential Input Bias Current (I_{IB})	$+V_{CC}$ = 5.25V, $-V_{CC}$ = -5.25V, V_{ID} = 0V				
	T_A = -55°C to 0°C			100	µA
	T_A = 0°C to 125°C			75	µA
Differential Input Offset Current	$+V_{CC}$ = 5.25V, $-V_{CC}$ = -5.25V, V_{ID} = 0V, T_A = 25°C		0.5		µA
High Level Input Voltage (Strobe Inputs) (V_{IH})		2			V
Low Level Input Voltage (Strobe Inputs (V_{IL})				0.8	V
High Level Output Voltage (V_{OH})	$+V_{CC}$ = 4.75V, $-V_{CC}$ = -4.75V, I_{OH} = -0.4 mA	2.4	4.0		V
Low Level Output Voltage (V_{OL})	$+V_{CC}$ = 4.75V, $-V_{CC}$ = -4.75V, I_{OL} = 16 mA		0.25	0.4	V
High Level Input Current (Strobe Inputs) (I_{IH})	$+V_{CC}$ = 5.25V, $-V_{CC}$ = -5.25V				
	V_{IH} = 2.40V			40	µA
	V_{IH} = 5.25V			1.0	mA
Low Level Input Current (Strobe Inputs) (I_{IL})	$+V_{CC}$ = 5.25V, $-V_{CC}$ = -5.25V, V_{IL} = 0.4V		-1.0	-1.6	mA

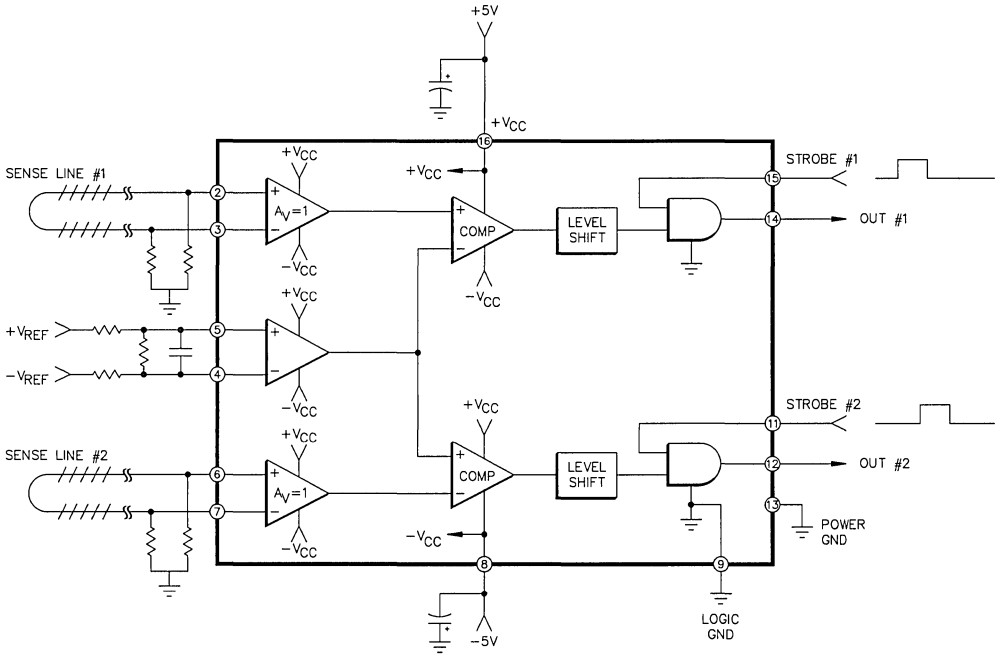
ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG5524 Min.	SG5524 Typ.	SG5524 Max.	Units
Static Section (continued)					
Short Circuit Output Current (I_{OS})	$+V_{CC}$ = 5.25V, $-V_{CC}$ = -5.25V, T_A = 25°C	-2.1		-3.5	mA
Supply Current from $+V_{CC}$ ($+I_{CC}$)	$+V_{CC}$ = 5.25V, $-V_{CC}$ = -5.25V, T_A = 25°C		25	40	mA
Supply Current from $-V_{CC}$ ($-I_{CC}$)	$+V_{CC}$ = 5.25V, $-V_{CC}$ = -5.25V, T_A = 25°C		-15	-20	mA

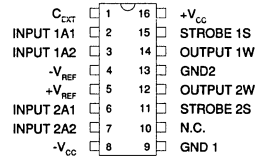
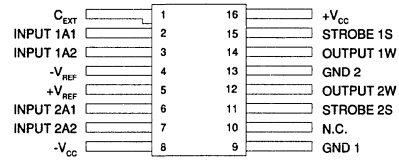
Parameter	Test Conditions	SG5524 Min.	SG5524 Typ.	SG5524 Max.	Units
Dynamic Section					
Propagation Delay Times From A1-A2 to W	C_L=15pF, R_L=288Ω, C_{EXT} > 100pF, T_A = 25°C				
Low to High (TPLH)			25	40	ns
High to Low (TPHL)			20		ns
Propagation Delay Times From Strobe to W	C_L=15pF, R_L=288Ω, C_{EXT} > 100pF, T_A = 25°C				
Low to High (TPLH)			15	30	ns
High to Low (TPHL)			20		ns

Note 5. Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The common-mode input signal is applied when the strobe is high.

TYPICAL APPLICATION



CONNECTION DIAGRAMS & ORDERING INFORMATION (See Note Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG5524J/883B SG5524J	-55°C to 125°C -55°C to 125°C	
16-PIN CERAMIC FLAT PACK F - PACKAGE	SG5524F/883B SG5524F	-55°C to 125°C -55°C to 125°C	

Note 1. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SG5768/68A, SG5770/70A, SG5772/72A, SG5774/74A SG25768, SG25770, SG6496/96A

DIODE ARRAY CIRCUITS

DESCRIPTION

The Silicon General series of diode arrays feature high breakdown, high speed diodes in a variety of configurations.

Each array configuration consists of either common anode diodes, common cathode diodes, or a combination of common anode and common cathode diodes.

Individual diodes within the array have 60V minimum breakdown voltage, can handle 500mA of current and typically switch in less than 10 nanoseconds.

Each of the array configurations is available in ceramic DIP or ceramic flatpack and can be processed to JANTXV, JANTX, or JAN flows at Silicon General's MIL-S-19500 facility.

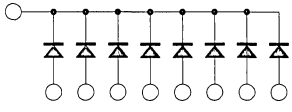
FEATURES

- **60V minimum breakdown voltage**
- **500mA current capability per diode**
- **Fast switching speeds: typically less than 10ns**
- **Low leakage current**

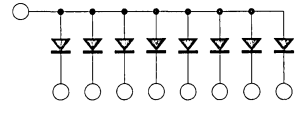
HIGH RELIABILITY FEATURES

- **MIL-S-19500/474 QPL - 1N5768**
  - 1N5770
  - 1N5772
  - 1N5774
- **JANTXV, JANTX & JAN available**
- **SG level "S" processing available**

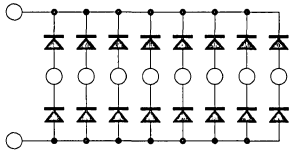
CIRCUIT DIAGRAMS



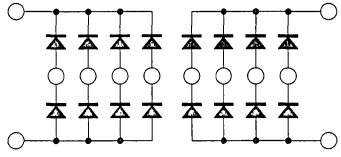
COMMON CATHODE
SG5768/SG5768A



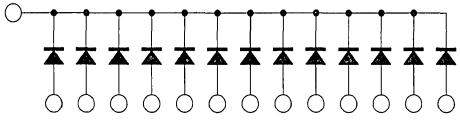
COMMON ANODE
SG5770/SG5770A



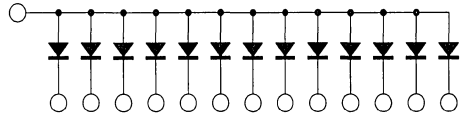
COMMON ANODE / COMMON CATHODE
SG5772/SG5772A



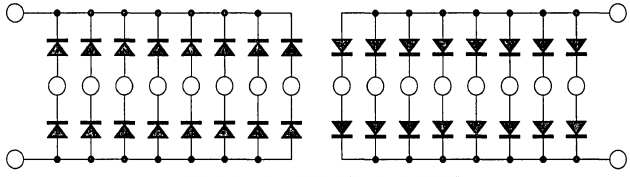
DUAL COMMON ANODE / COMMON CATHODE
SG5774/SG5774A



COMMON CATHODE
SG25768



COMMON ANODE
SG25770



DUAL COMMON ANODE / COMMON CATHODE
SG6496/SG6496A

April 1990

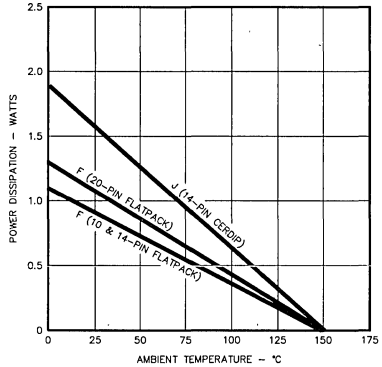
ABSOLUTE MAXIMUM RATINGS (Note 1 & 2)

Breakdown Voltage (V_{BR}) 60V
Output Current (I_O), T_C = 25°C
Continuous 500mA

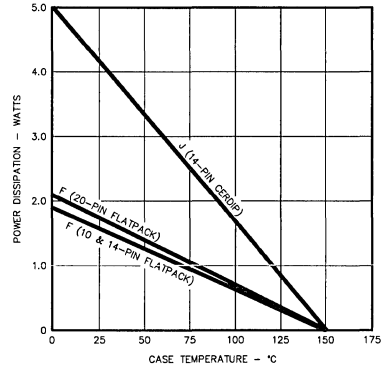
Operating Junction Temperature
Hermetic (J, F Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 200°C

Note 1. Exceeding these ratings could cause damage to the device.
Note 2. Applicable for each diode.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 3)

Operating Ambient Temperature Range
SG5768, SG5768A ..... -55°C to 150°C
SG5770, SG5770A ..... -55°C to 150°C
SG5772, SG5772A ..... -55°C to 150°C

Operating Ambient Temperature Range
SG5774, SG5774A ..... -55°C to 150°C
SG25768 ..... -55°C to 150°C
SG25770 ..... -55°C to 150°C
SG6496, SG6496A ..... -55°C to 150°C

Note 3. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply for the operating temperature of T_A = 25°C for each diode. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG5768A SG25768			SG5768			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Breakdown Voltage (V_{BR})	I_R = 10µA	60			60			V
Forward Voltage (V_F)	Duty Cycle ≤ 2%, 300 µs pulse							
	I_F = 100mA			1.0			1.0	V
	I_F = 200mA			1.1			1.1	V
	I_F = 500mA			1.3			1.5	V
	I_F = 10mA, T_A = -55°C			1.0			1.0	V
Reverse Current (I_R)	V_R = 40V			100			100	nA
	V_R = 40V, T_A = 150°C			50			50	µA
Capacitance (C) (Note 4)	V_R = 0V, f = 1MHz, Pin-to-pin			4			4	pf
Forward Recovery Time (t_{fr}) (Note 4)	I_F = 500mA, t_r ≤ 15ns, V_{fr} = 1.8V, R_S = 50Ω			40			40	ns
Reverse Recovery Time (t_{rr}) (Note 4)	I_F = I_R = 200mA, i_{rr} = 20mA, R_L = 100Ω			20			20	ns

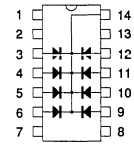
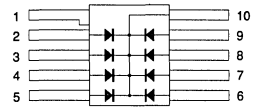
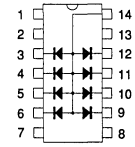
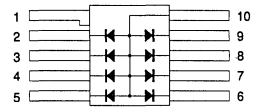
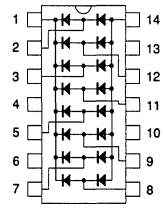
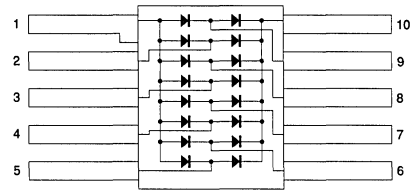
Note 4. The parameters, although guaranteed, are not 100% tested in production.

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG5770A SG25770			SG5770			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Breakdown Voltage (V_{BR})	I_R = 10µA, 100ms pulse, ≤ 20% Duty Cycle	60			60			V
Forward Voltage (V_F)	Duty Cycle ≤ 2%, 300 µs pulse							
	I_F = 100mA			1.0			1.0	V
	I_F = 200mA			1.1			1.1	V
	I_F = 500mA			1.3			1.5	V
	I_F = 10mA, T_A = -55°C			1.0			1.0	V
Reverse Current (I_R)	V_R = 40V			100			100	nA
	V_R = 40V, T_A = 150°C			50			50	µA
Capacitance (C) (Note 4)	V_R = 0V, f = 1MHz, Pin-to-pin			8			8	pf
Forward Recovery Time (t_{fr}) (Note 4)	I_F = 500mA, t_r ≤ 15ns, V_{fr} = 1.8V, R_S = 50Ω			40			40	ns
Reverse Recovery Time (t_{rr}) (Note 4)	I_F = I_R = 200mA, i_{rr} = 20mA, R_L = 100Ω		7	20		7	20	ns

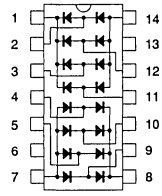
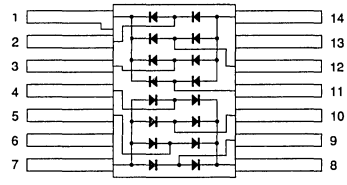
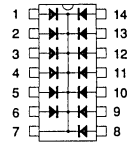
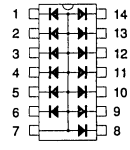
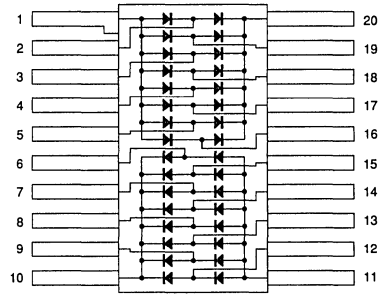
Parameter	Test Conditions	SG6496A SG5772A SG5774A			SG6496 SG5772 SG5774			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Breakdown Voltage (V_{BR})	I_R = 10µA, 100ms pulse, ≤ 20% Duty Cycle	60			60			V
Forward Voltage (V_F)	Duty Cycle ≤ 2%, 300µs pulse							
	I_F = 100mA			1.0			1.0	V
	I_F = 200mA			1.1			1.1	V
	I_F = 500mA			1.3			1.5	V
	I_F = 10mA, T_A = -55°C			1.0			1.0	V
Reverse Current (I_R)	V_R = 40V			100			100	nA
	V_R = 40V, T_A = 150°C			50			50	µA
Capacitance (C) (Note 4)	V_R = 0V, f = 1MHz, Pin-to-pin			8			8	pf
Forward Recovery Time (t_{fr}) (Note 4)	I_F = 500mA, t_r ≤ 15ns, V_{fr} = 1.8V, R_S = 50Ω			40			40	ns
Reverse Recovery Time (t_{rr}) (Note 4)	I_F = I_R = 200mA, i_{rr} = 20mA, R_L = 100Ω		7	20		7	20	ns

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN CERAMIC DIP J - PACKAGE	SG5768AJ SG5768J	-55°C to 150°C -55°C to 150°C	
10-PIN CERAMIC FLATPACK F - PACKAGE	SG5768AF SG5768F	-55°C to 150°C -55°C to 150°C	
14-PIN CERAMIC DIP J - PACKAGE	SG5770AJ SG5770J	-55°C to 150°C -55°C to 150°C	
10-PIN CERAMIC FLATPACK F - PACKAGE	SG5770AF SG5770F	-55°C to 150°C -55°C to 150°C	
14-PIN CERAMIC DIP J - PACKAGE	SG5772AJ SG5772J	-55°C to 150°C -55°C to 150°C	
10-PIN CERAMIC FLATPACK F - PACKAGE	SG5772AF SG5772F	-55°C to 150°C -55°C to 150°C	

Note 1. Consult factory for other packages available.
2. All packages are viewed from the top.
3. Consult factory for JAN, JAN TX, and JAN TXV product availability.

CONNECTION DIAGRAMS & ORDERING INFORMATION (continued)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN CERAMIC DIP J - PACKAGE	SG5774AJ SG5774J	-55°C to 150°C -55°C to 150°C	
14-PIN CERAMIC FLATPACK F - PACKAGE	SG5774AF SG5774F	-55°C to 150°C -55°C to 150°C	
14-PIN CERAMIC DIP J - PACKAGE	SG25768J	-55°C to 150°C	
14-PIN CERAMIC DIP J - PACKAGE	SG25770J	-55°C to 150°C	
20-PIN CERAMIC FLATPACK SF - PACKAGE	SG6496AF SG6496F	-55°C to 150°C -55°C to 150°C	

8

SG6100/SG6101
ADVANCED DATA SHEET

DIODE ARRAY CIRCUITS

DESCRIPTION

The SG6100 and SG6101 diode arrays are monolithic, high breakdown, fast switching speed diode arrays. The SG6100 is configured with 7 straight through diodes, while the SG6101 has 8 straight through diodes.

These two diode array configurations allow the designer maximum flexibility for circuit design and board layout. Since each diode within the array has individual anode and cathode connections the device may be used in a variety of applications. Also, due to the array's monolithic construction the diode electrical parameters are very closely matched.

Both devices are available in ceramic DIP and flatpack and can be processed to Silicon General's S level, JANTXV, JANTX, or JAN equivalent flows.

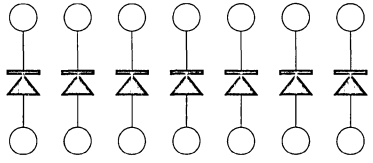
FEATURES

- **75V minimum breakdown voltage**
- **100mA current capability per diode**
- **Switching speeds less than 5ns**
- **Low leakage current < 25nA**

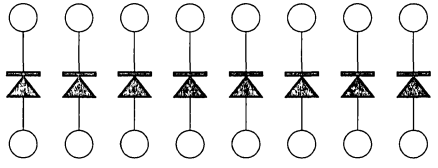
HIGH RELIABILITY FEATURES

- **MIL-S-19500/474 QPL planned for Sept. '89**
- **Equivalent JANS, JANTXV, JANTX, JAN screening available**

CIRCUIT DIAGRAMS



7 - STRAIGHT THROUGH DIODES
SG6100



8 - STRAIGHT THROUGH DIODES
SG6101

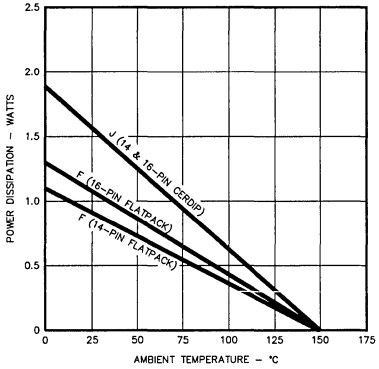
ABSOLUTE MAXIMUM RATINGS (Note 1 & 2)

Breakdown Voltage (V_{BR}) 75V
Output Current (I_O), T_C = 25°C
Continuous 300mA

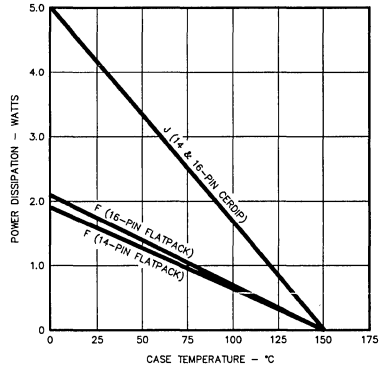
Operating Junction Temperature
Hermetic (J, F Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 200°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.
Note 2. Applicable for each diode.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 3)

Operating Ambient Temperature Range
SG6100 ..... -55°C to 150°C
SG6101 ..... -55°C to 150°C

Note 3. Range over which the device is functional.

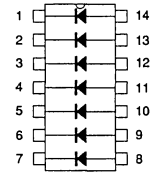
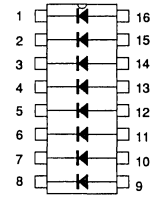
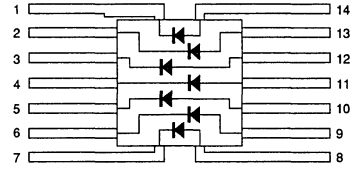
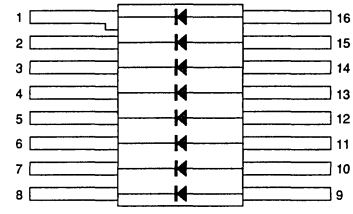
ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply for the operating ambient temperature of T_A = 25°C for each diode. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG6100/SG6101			Units
		Min.	Typ.	Max.	
Breakdown Voltage (V_{BR})	I_R = 5µA, Duty Cycle < 20%	75			V
Forward Voltage (V_F)	Duty Cycle ≤ 2%, 300 µs pulse				
	I_F = 100mA			1.0	V
	I_F = 10mA, T_A = -55°C			1.0	V
Reverse Current (I_R)	V_R = 20V			25	nA
	V_R = 40V			100	nA
	V_R = 40V, T_A = 150°C			50	µA
Capacitance (C) (Note 4)	V_R = 0V, f = 1MHz, Pin-to-pin			4	pf
Forward Recovery Time (t_{fr}) (Note 4)	I_F = 500mA, t_r ≤ 15ns, V_{fr} = 1.8V, R_S = 50Ω			15	ns
Reverse Recovery Time (t_{rr}) (Note 4)	I_F = I_R = 200mA, i_{rr} = 20mA, R_L = 100Ω			5	ns

Note 4. The parameters, although guaranteed, are not 100% tested in production.

CONNECTION DIAGRAMS & ORDERING INFORMATION (continued)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN CERAMIC DIP J - PACKAGE	SG6100J	-55°C to 150°C	
16-PIN CERAMIC DIP J - PACKAGE	SG6101J	-55°C to 150°C	
14-PIN CERAMIC FLATPACK F - PACKAGE	SG6100F	-55°C to 150°C	
16-PIN CERAMIC FLATPACK F - PACKAGE	SG6101F	-55°C to 150°C	

Note 1. Consult factory for other packages available.
2. All packages are viewed from the top.

8

DUAL SENSE AMPLIFIER

DESCRIPTION

The SG55234/SG55234A/SG5534 is a monolithic, dual channel sense amplifier capable of detecting low-level differential-input signals from high speed magnetic memories. The inputs of the sense amplifier have adjustable threshold levels that allow the designer to customize the device to the application. Also, to eliminate much of the threshold voltage adjustments necessary with competitors' sense amplifiers, the SG55234/SG55234A is tested for V_{TH} matching. This guarantees the different inputs will trigger within set levels of each other.

The outputs of the sense amplifier are TTL/DTL (logic level) compatible and feature separate strobes for individual channel control.

The SG55234/SG55234A/SG5534 is characterized for operation over the full military ambient temperature range of -55°C to 125°C. The device is available in 16-pin ceramic DIP or 16-pin flatpack.

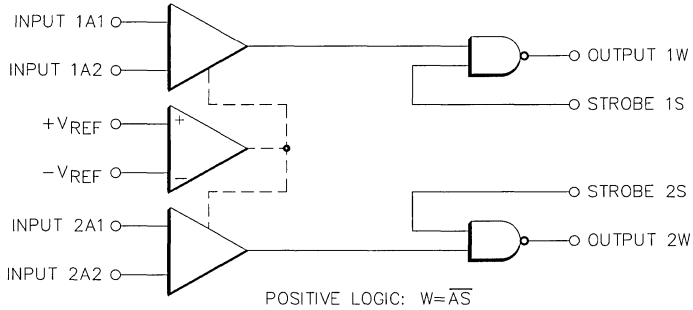
FEATURES

- **Adjustable input threshold voltage**
- **High speed**
- **TTL or DTL output compatibility**
- **Threshold voltage matching (ΔV_{TH}):**
  SG55234A 1.5mV
  SG55234 3.0mV

HIGH RELIABILITY FEATURES - SG55234/SG55234A/SG5534

- ◇ **Available to MIL-STD-883**
- ◇ **SG level "S" processing available**

BLOCK DIAGRAM



POSITIVE LOGIC: $W=\overline{AS}$

FUNCTION TABLE

INPUTS A	INPUTS S	OUTPUT W
H	H	L
L	X	H
X	L	H

Definition of Logic Levels

INPUT	H	L	X
A*	$V_{ID} \geq V_{T\,MAX}$	$V_{ID} \leq V_{T\,MIN}$	Irrelevant
S	$V_I \geq V_{IH\,MIN}$	$V_I \leq V_{IL\,MAX}$	Irrelevant

*A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

8

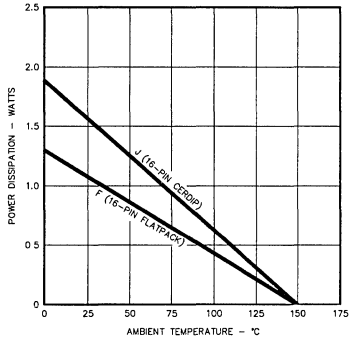
ABSOLUTE MAXIMUM RATINGS (Note1)

Supply Voltage ($+V_{CC}$) 7.0V
Supply Voltage ($-V_{CC}$) ..... -7.0V
Differential Input Voltage ..... ±5V
Input Voltage to Ground 5.5V

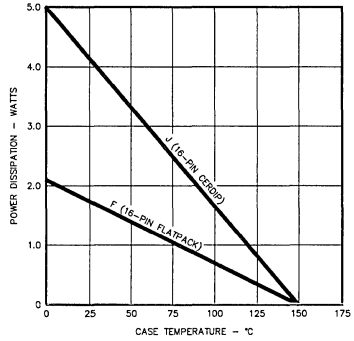
Operating Junction Temperature (T_C)
Hermetic (J, F-Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1. Values beyond which damage may occur.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage ($+V_{CC}$) ..... 4.75V to 5.25V
Supply Voltage ($-V_{CC}$) ..... -4.75V to -5.25V
Reference Voltage (V_{REF}) ..... 15mV to 40mV

Operating Ambient Temperature Range:
SG55234/SG55234A ..... -55°C to 125°C
SG5534 ..... -55°C to 125°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG55234/SG55234A/SG5534 with $-55°C \le T_A \le 125°C$, $+V_{CC} = 5V$, and $-V_{CC} = -5V$. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG55234/55234A SG5534			Units
		Min.	Typ.	Max.	
Static Section					
Differential-Input Threshold Voltage (V_T) (Note 3)	V_{REF} = 15mV				
	SG55234/SG5534	11	15	19	mV
	SG55234A	13	15	17	mV
	V_{REF} = 40mV				
	SG55234/SG5534	36	40	44	mV
	SG55234A	38	40	42	mV
Max. Difference Between Any Two Channels (ΔV_T)	V_{REF} = 15mV, T_A=25°C				
	SG55234			3.0	mV
	SG55234A			1.5	mV
Differential-Input Bias Current (I_{IB})	$+V_{CC}$ = 5.25V, $-V_{CC}$ = -5.25V, V_{ID} = 0V		30	75	µA
	SG5534 only			100	µA
Differential-Input Offset Current (I_{IO})	$+V_{CC}$ = 5.25V, $-V_{CC}$ = -5.25V, V_{ID} = 0V		0.5		µA
High-Level Input Voltage (Strobe Inputs) (V_{IH})		2.0			V
Low-Level Input Voltage (Strobe Inputs (V_{IL})				0.8	V
High-Level Output Voltage (V_{OH})	$+V_{CC}$ = 4.75V, $-V_{CC}$ = –4.75V, I_{OH}= –0.4mA	2.4	4.0		V
Low-Level Output Voltage (V_{OL})	$+V_{CC}$ = 4.75V, $-V_{CC}$ = –4.75V, I_{OL}=16 mA		0.25	0.4	V
High-Level Input Current (Strobe Inputs) (I_{IH})	$+V_{CC}$ = 5.25V, $-V_{CC}$ = -5.25V				
	V_{IH} = 2.40V			40	µA
	V_{IH} = 5.25V			1.0	mA
Low-Level Input Current (Strobe Inputs) (I_{IL})	$+V_{CC}$ = 5.25V, $-V_{CC}$ = -5.25V, V_{IL} = 0.4V		-1.0	-1.6	mA
Input Clamp Voltage (Strobe Inputs) (V_{CD})	(SG5534 only) $+V_{CC}$ = 5.25V, $-V_{CC}$ = -5.2V,				
	I_{IN} = -12mA			-1.5V	V

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG55234/55234A SG5534 Min.	Typ.	Max.	Units
Static Section (continued)					
Short-circuit Output Current (I_{OS})	$+V_{CC}$ = 5.25V, $-V_{CC}$ = -5.25V, SG55234/234A only	-2.1		-3.5	mA
Output Leakage Current (I_{CEX})	$+V_{CC}$ = 5.25V, $-V_{CC}$ = -5.25V, T_A = 25°C		25	250	µA
	SG5534 only		-15	40	mA
Supply Current from $+V_{CC}$ ($+I_{CC}$)	$+V_{CC}$ = 5.25V, $-V_{CC}$ = -5.25V, T_A = 25°C			38	mA
	SG5534 only			-20	mA
Supply Current from $-V_{CC}$ ($-I_{CC}$)	$+V_{CC}$ = 5.25V, $-V_{CC}$ = -5.25V, T_A = 25°C			18	mA
	SG5534 only				

Parameter	Test Conditions	SG55234/55234A SG5534 Min.	Typ.	Max.	Units
Dynamic Section					
Propagation Delay Times From A1-A2 to W	C_L=15pF, R_L=288Ω, T_A = 25°C				
Low to High (TPLH)			25		ns
High to Low (TPHL)			25	40	ns
Propagation Delay Times From Strobe to W	C_L=15pF, R_L=288Ω, T_A = 25°C				
Low to High (TPLH)			25		ns
High to Low (TPHL)			15	30	ns
Differential-Input Overload Recovery	Differential Input Pulse:				
Time (T_{ORD}) (Note 4)	V_{ID} = 2V, T_R = T_F = 20ns, T_A = 25°C		20		ns
Common-Mode-Input Overload Recovery	Common-Mode Input Pulse:				
Time (T_{ORC}) (Note 5)	V_{IC} = ±2V, T_R = T_F = 20ns, T_A = 25°C		20		ns
Minimum Cycle Time ($T_{CYC(MIN)}$)			200		ns

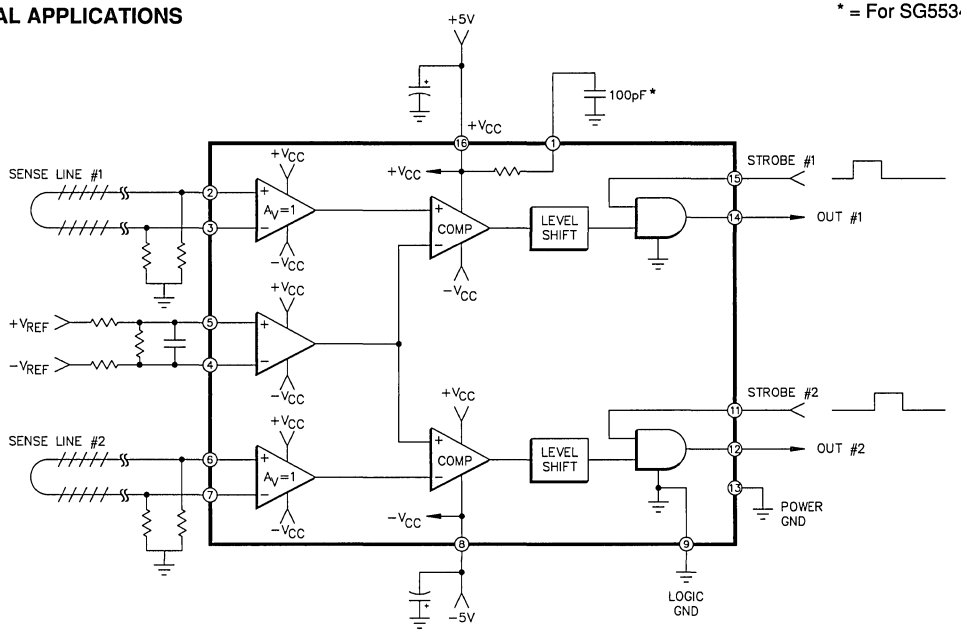
Note 3. The differential-input threshold voltage (V_T) is defined as the DC differential-input voltage (V_{ID}) required to force the output of the sense amplifier to the logic gate threshold voltage level.

Note 4. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.

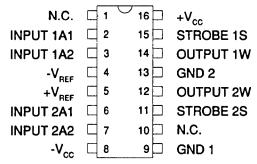
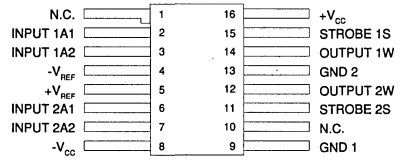
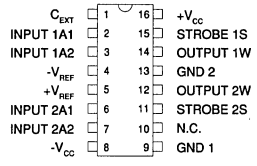
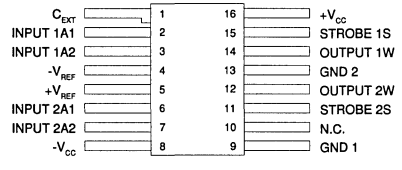
Note 5. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

TYPICAL APPLICATIONS

* = For SG5534 only



CONNECTION DIAGRAMS & ORDERING INFORMATION (See Note Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG55234J/883B SG55234J SG55234AJ/883B SG55234AJ	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C	
16-PIN CERAMIC FLAT PACK F - PACKAGE	SG55234F/883B SG55234F SG55234AF/883B SG55234AF	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C	
16-PIN CERAMIC DIP J - PACKAGE	SG5534J/883B SG5534J	-55°C to 125°C -55°C to 125°C	
16-PIN CERAMIC FLAT PACK F - PACKAGE	SG5534F/883B SG5534F	-55°C to 125°C -55°C to 125°C	

Note 1. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

DUAL SENSE AMPLIFIER/DATA REGISTERS

DESCRIPTION

The SG55236/SG55236A is a monolithic, dual channel, high speed sense amplifier with independently controlled data registers. The input section features an adjustable differential-input threshold voltage. All four inputs of the sense amplifier have been screened to guarantee threshold matching (see ΔV_{TH} in electrical characteristics).

Separate detector outputs for each channel allow the designer the flexibility to use additional output stages if necessary. In addition, each of the data registers has provisions for external data inputs.

The SG55236A was developed to meet the high speed, tight voltage threshold matching requirements of today's fast cycle time magnetic memory systems. Its enhancements are listed in the Electrical Characteristics.

The SG55236/SG55236A is available in a 24-pin flat pack and is characterized over the full military ambient temperature range of -55°C to 125°C.

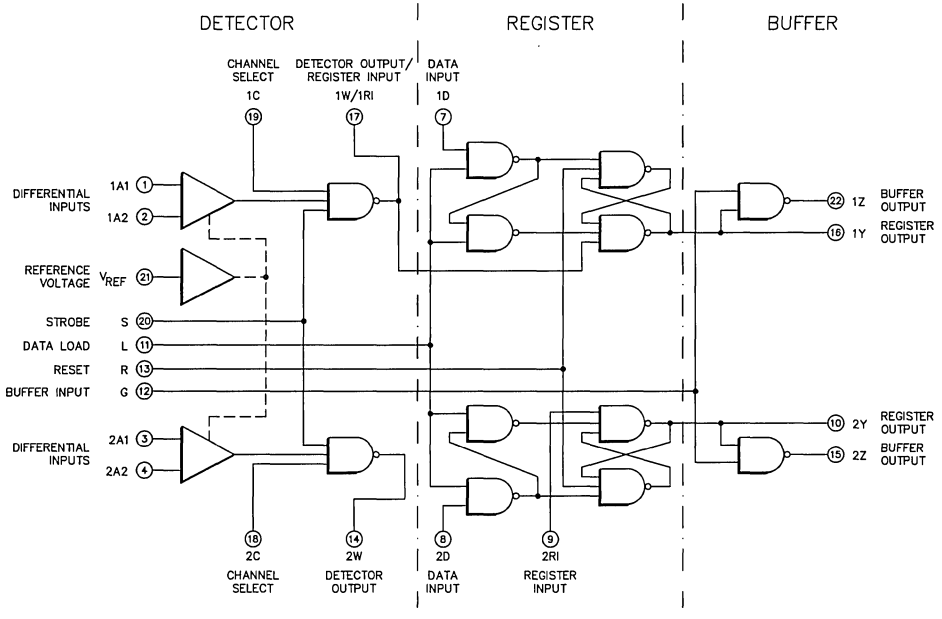
FEATURES

- **Threshold voltage matching (ΔV_{TH}):**
  SG55236 1.5mV
  SG55236A 0.8mV
- **Adjustable differential-input threshold voltage**
- **Reference amplifier inherently stable with no external frequency compensation required**
- **Built-in data register with provisions for external data inputs**
- **Built-in data buffer drives 450pF load in 15ns**
- **Internal reference voltage attenuator makes reference amplifier less sensitive to noise**

HIGH RELIABILITY FEATURES - SG55236

- **Available to MIL-STD-883**
- **Radiation data available**
- **SG level "S" processing available**

BLOCK DIAGRAM



See page 4 of this data sheet for Function Tables

April 1990

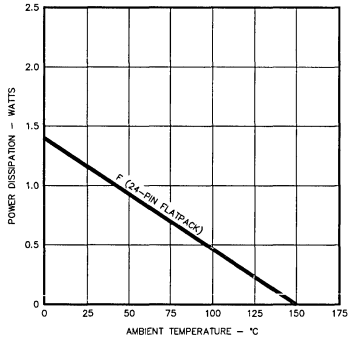
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ($+V_{CC}$) 7.0V
Supply Voltage ($-V_{CC}$) ..... -7.0V
Reference Voltage (V_{REF}) ..... ±5.0V
Differential Input Voltage (V_{ID}) ..... ±5.0V
Voltage From Any Input to Ground 5.25V

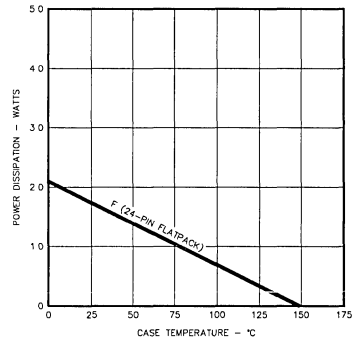
Operating Junction Temperature (T_J)
Hermetic (J-Package) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1. Values beyond which damage may occur.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage ($+V_{CC}$) ..... 4.75V to 5.25V
Supply Voltage ($-V_{CC}$) ..... -4.75V to -5.25V
Reference Voltage (V_{REF}) ..... ±1.5V to ±4.5V
High-Level Output Voltage (V_{OH}):
Detector and Buffer ..... V_{CC}
High-Level Output Current (I_{OH}):
Register ..... -400µA

Low-Level Output Current (I_{OL}):
Register 16mA
Buffer 25mA
Detector 3.2mA
Width of Reset Pulse (t_R) 115ns
Operating Ambient Temperature Range:
SG55236/SG55236A ..... -55°C to 125°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG55236/SG55236A with $-55°C \le T_A \le 125°C$, $+V_{CC} = 4.75V$, $-V_{CC} = -4.75V$, and $V_{REF} = \pm 2.1V$. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG55236A			SG55236			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Static Section								
Differential-Input Threshold Voltage (V_{TH})	$+V_{CC} = 5V$, $-V_{CC} = -5V$, $T_A = 25°C$	6.0	7.0	8.0	5.0	7.0	9.0	mV
	$+V_{CC} = 5V \pm 5\%$, $-V_{CC} = -5V \pm 5\%$	5.5	7.0	8.5	4.5	7.0	9.5	mV
Delta Threshold Voltage (ΔV_{TH})	$T_A = 25°C$ (See Functional Description)			0.8			1.5	mV
Differential-Input Bias Current (I_{IB})	$+V_{CC} = 5V$, $-V_{CC} = -5V$, $V_{ID} = 0$		12	20		20	40	µA
Differential-Input Offset Current (I_{IO})	$+V_{CC} = 5V$, $-V_{CC} = -5V$, $V_{ID} = 0$		0.5	2.0		1.0	5.0	µA
High-Level Input Voltage (V_{IH}) (Strobe and Logic Inputs)		2.0			2.0			V
Low-Level Input Voltage (V_{IL}) (Strobe and Logic Inputs)				0.8			0.8	V
High-Level Output Voltage (V_{OH}) Register	$V_{IH} = 2V$, $V_{IL} = 0.8V$, $I_{OH} = -400µA$	2.4			2.4			V
Detector	$V_{IH} = 2V$, $V_{IL} = 0.8V$	2.4			2.4			V
High-Level Output Current (I_{OH}) Buffer	$V_{IH} = 2V$, $V_{IL} = 0.8V$, $V_{OH} = 4.75V$			250			250	µA

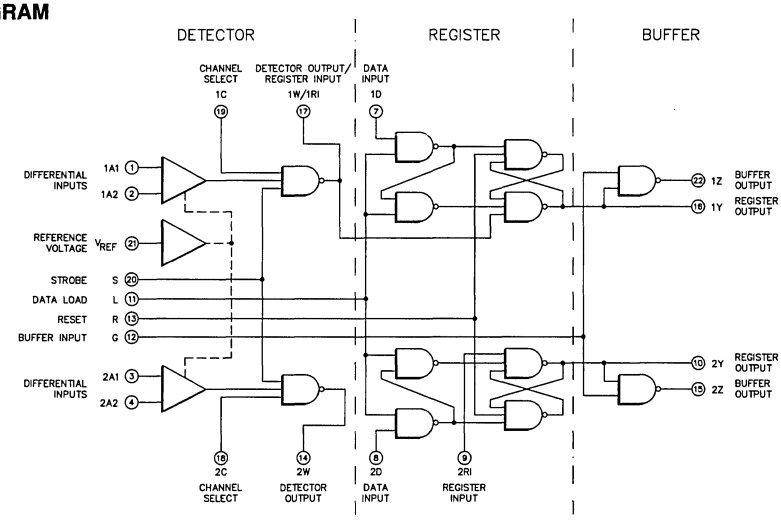
ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG55236A			SG55236			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Static Section (continued)								
Low-Level Output Voltage (V_{OL})								
Register	V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA			0.4			0.4	V
Buffer	V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 25mA			0.5			0.5	V
Detector	V_{IH} = 2V, V_{IL} = 0.8V			0.4			0.4	V
Input Current at Maximum Input Voltage (Logic Inputs) (I_{IN})	$+V_{CC}$ = 5.25V, $-V_{CC}$ = –5.25V, V_{IH} = 5.25V			1			1	mA
High-Level Input Current (I_{IH})	$+V_{CC}$ = 5.25V, $-V_{CC}$ = –5.25V, V_{IH} = 2.4V							
Data In or Channel Select				40			40	µA
Register Input 2RI				-750			-750	µA
Strobe, Reset, or Buffer Input				80			80	µA
Data Load				160			160	µA
Low-Level Input Current (I_{IL})	$+V_{CC}$ = 5.25V, $-V_{CC}$ = –5.25V, V_{IL} = 0.4V							
Data In				-2.0			-2.0	mA
Channel Select				-1.6			-1.6	mA
Register Input 2RI				-3.0			-3.0	mA
Strobe, Reset, or Buffer Input				-3.2			-3.2	mA
Data Load				-6.4			-6.4	mA
Short-Circuit Output Current (I_{OS})								
Register	$+V_{CC}$ = 5.25V, $-V_{CC}$ = –5.25V, V_{OUT} = 0V	-20		-60	-20		-60	mA
Reference-Input Current (I_{REF})	$+V_{CC}$ = 5.25V, $-V_{CC}$ = -5.25V, V_{REF} = -2.1V, T_A = 25°C			0.5			0.5	mA
Supply Current From $+V_{CC}$ ($+I_{CC}$)	$+V_{CC}$ = 5.25V, $-V_{CC}$ = -5.25V, T_A = 25°C			55			55	mA
Supply Current From $-V_{CC}$ ($-I_{CC}$)	$+V_{CC}$ = 5.25V, $-V_{CC}$ = -5.25V, T_A = 25°C			18			18	mA

Parameter	See Figure	Input	Output	SG55236A			SG55236			Units
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Dynamic Section (Note 3)										
Propagation Delay Time										
Low to High (TPLH)	1, 2	1A or 2A	Y		28	40		28	50	ns
	3, 4	Strobe	Y		16	25		18	35	ns
	5, 6	Data Input	Y		17	30		17	40	ns
High to Low (TPHL)	3, 4	Data Load	Y		13	25		15	35	ns
	5, 6	Reset	Y		12	20		12	30	ns
Low to High (TPLH)	5, 6	Reset	Z		100	200		100	200	ns
High to Low (TPHL)	5, 6	Buffer Input	Z		14	35		22	55	ns
	1, 2	1A or 2A	Z		42	60		42	90	ns
Transition Time										
Low to High (TTLH)	5, 6		Y		10	20		13	35	ns
High to Low (TTHL)	5, 6		Y		4	15		7	20	ns
Low to High (TTLH)	5, 6		Z		150	185		150	185	ns
High to Low (TTHL)	5, 6		Z		15	35		20	50	ns

Note 3. Unless otherwise specified, $+V_{CC}$ = 5V, $-V_{CC}$ = -5V, V_{REF} = -2.1V, T_A = 25°C

BLOCK DIAGRAM



FUNCTION TABLE

INPUTS								OUTPUTS	
A	C	S	W/RI*	L	D	R	G	Y	Z
H	H	H	L	X	X	X	H	H	L
H	H	H	L	X	X	X	L	H	H
↓	H	H	↑	L	X	H	H	H	L
↓	H	H	↑	L	X	H	L	H	H
H	↓	H	↑	L	X	H	H	H	L
H	↓	H	↑	L	X	H	L	H	H
H	H	↓	↑	L	X	H	H	H	L
H	H	↓	↑	L	X	H	L	H	H
L	X	X	H	H	H	X	X	L	H
L	X	X	H	H	L	X	H	H	L
L	X	X	H	H	L	X	L	H	H
L	X	X	H	L	X	L	X	L	H
L	X	X	H	L	X	↑	X	L	H
X	L	X	H	H	H	X	X	L	X
X	L	X	H	H	L	X	H	H	L
X	L	X	H	H	L	X	L	H	H
X	L	X	H	L	X	L	X	L	H
X	L	X	H	L	X	↑	X	L	H
X	X	L	H	H	H	X	X	L	X
X	X	L	H	H	L	X	H	H	L
X	X	L	H	H	L	X	L	H	H
X	X	L	H	L	X	L	X	L	H
X	X	L	H	L	X	↑	X	L	H

FUNCTION TABLE FOR DUAL-CHANNEL DETECTOR OPERATION

(2W connected to 1W/1RI)

INPUTS					OUTPUT
1A	1C	2A	2C	S	1W · 2W
H	H	X	X	H	L
X	X	H	H	H	L
↓	H	L	X	H	↑
↓	H	X	L	H	↑
L	X	↓	H	H	↑
X	L	↓	H	H	↑
Any Other Combination					H

H = High level (steady state)
L = Low level (steady state)
X = Irrelevant (any input, including transitions)
↓ = Transition from high level to low level
↑ = Transition from low level to high level

* The W/RI column shows the output from the detector resulting from the inputs A, C, and S. In positive logic, $W = \overline{ACS}$. For dual operation with 2W connected to 2RI, this column represents an intermediate node and can be ignored.

For independent operation of register 2, this column is an input and the A, C, and S columns should be ignored.

For dual-channel operation with 2W connected to 1W/1R1, this column is the result of $W = \overline{S(1A \cdot 1C + 2A \cdot 2C)}$, as shown in the table above.

Definition of Logic Levels

INPUT	H	L
A**	$V_{ID} \geq V_{T\,MAX}$	$V_{ID} \leq V_{T\,MIN}$
LOGIC	$V_I \geq V_{IH\,MIN}$	$V_I \leq V_{IL\,MAX}$

** A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

TEST CIRCUITS AND SWITCHING WAVEFORMS

PROPAGATION DELAY TIMES, DIFFERENTIAL INPUT TO REGISTER OUTPUT AND BUFFER OUTPUT

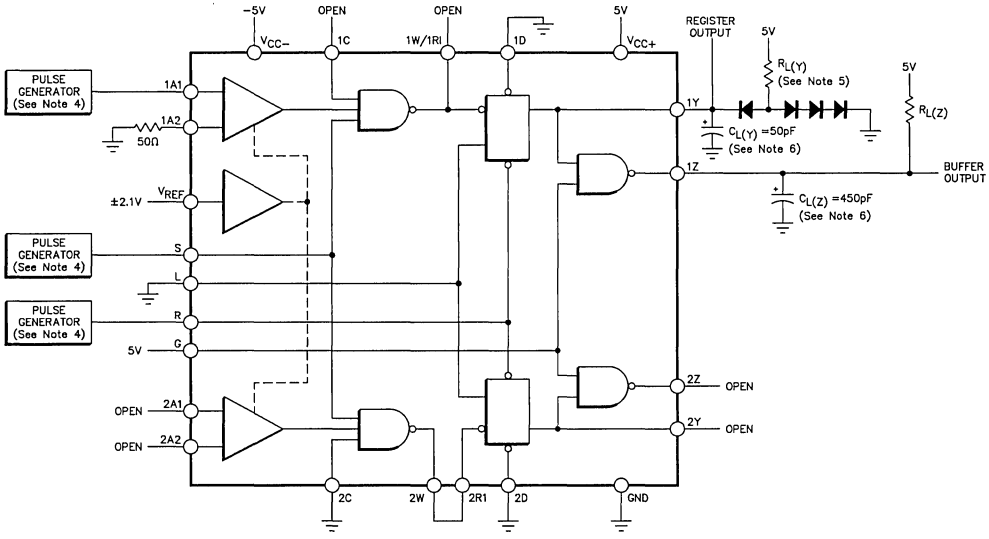


FIGURE 1 - TEST CIRCUIT (See Note 8)

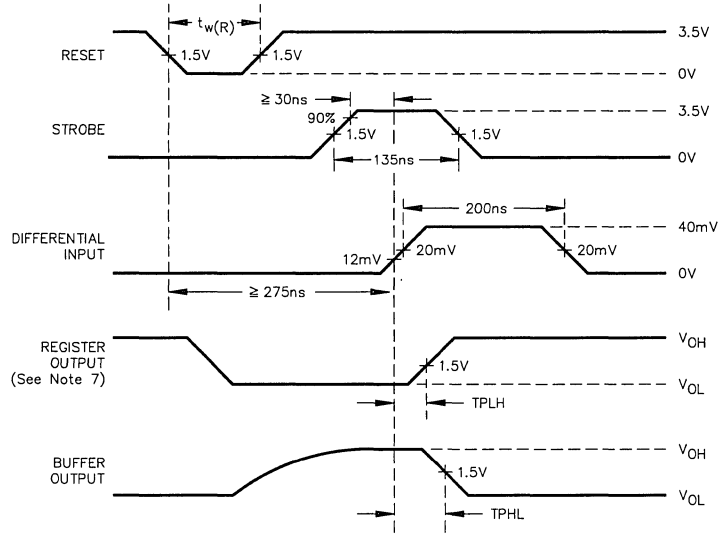


FIGURE 2 - VOLTAGE WAVEFORMS

Note 4. The pulse generators have the following characteristics: Z_o = 50Ω, t_r = 15ns, t_f = 15ns, $t_{w(R)} \geq$ 115ns, PRR = 500KHz.
5. All diodes are 1N3064.
6. $C_{L(Y)}$ and $C_{L(Z)}$ include probe and jig capacitance.
7. Initially high output condition can be established by repetitive cycling.
8. Connections are shown for testing channel 1. To test channel 2, reverse connections of 1C and 2C along with inputs and outputs.

TEST CIRCUITS AND SWITCHING WAVEFORMS (continued)

PROPAGATION DELAY TIMES, STROBE AND DATA LOAD TO REGISTER OUTPUT

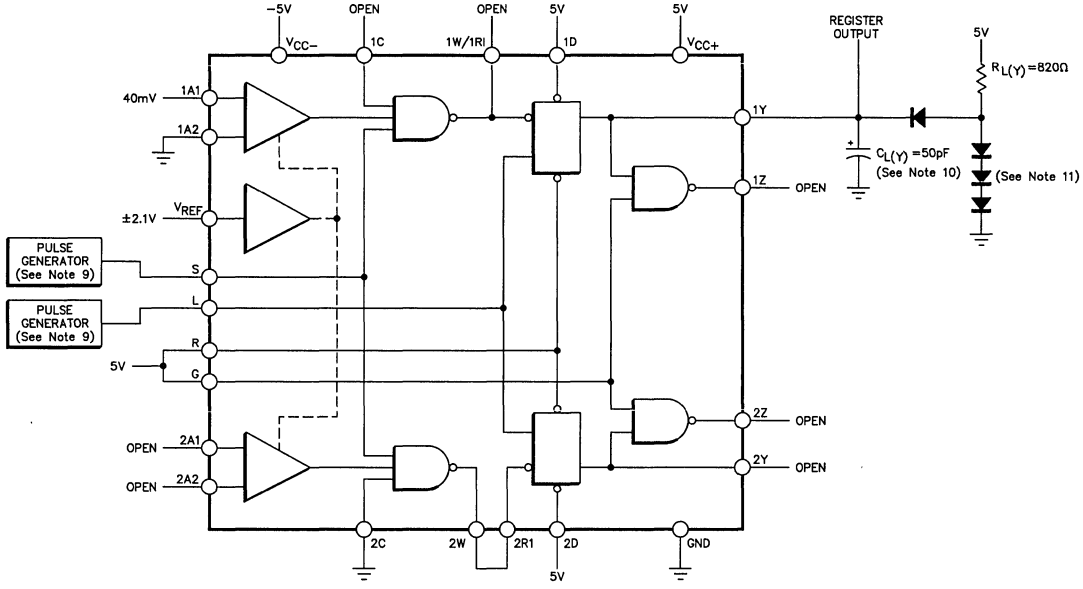


FIGURE 3 - TEST CIRCUIT (See Note 13)

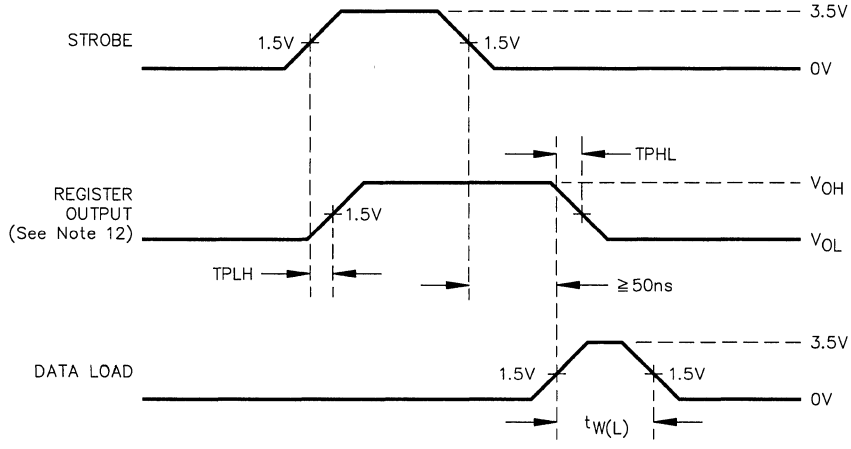


FIGURE 4 - VOLTAGE WAVEFORMS

Note 9. The pulse generators have the following characteristics: $Z_o = 50\Omega$, $t_r = 15ns$, $t_f = 15ns$, $t_{w(L)} \geq 35ns$, PRR = 500KHz.
10. $C_{L(Y)}$ includes probe and jig capacitance.
11. All diodes are 1N3064.
12. Initially low output condition can be established by repetitive cycling.
13. Connections are shown for testing channel 1. To test channel 2, reverse connections of 1C and 2C along with inputs and outputs.

TEST CIRCUITS AND SWITCHING WAVEFORMS (continued)

PROPAGATION DELAY TIMES FROM DATA INPUT RESET AND BUFFER INPUT TO REGISTER OUTPUT AND BUFFER OUTPUT, TRANSITION TIMES OF REGISTER OUTPUT AND BUFFER OUTPUT

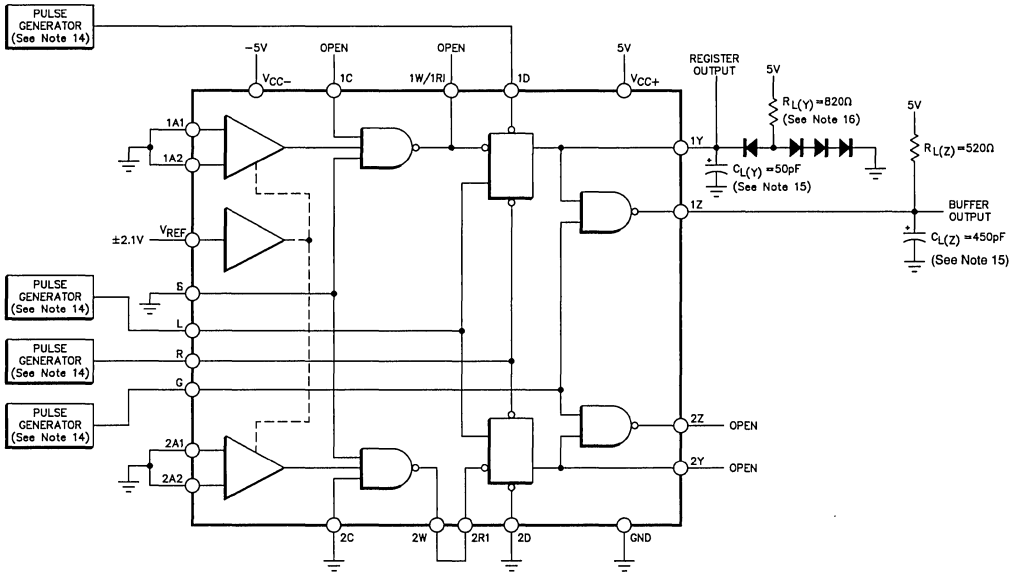


FIGURE 5 - TEST CIRCUIT (See Note 18)

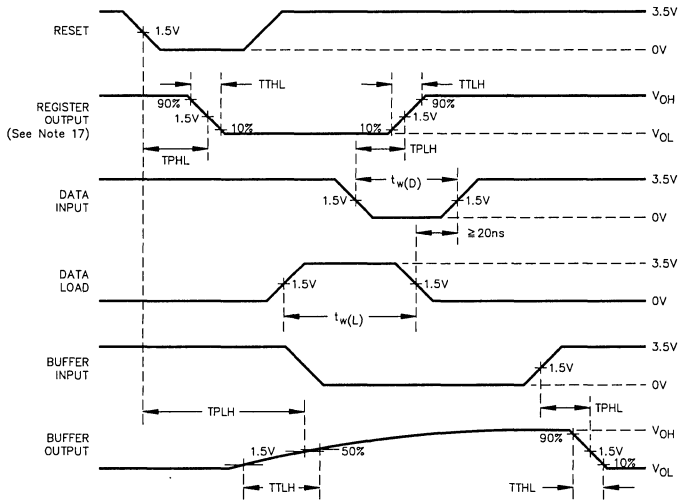


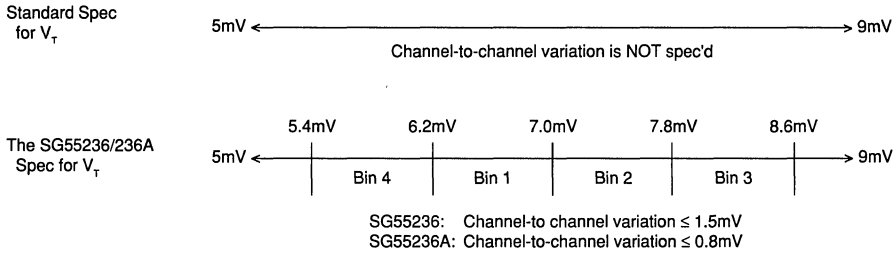
FIGURE 6 - VOLTAGE WAVEFORMS

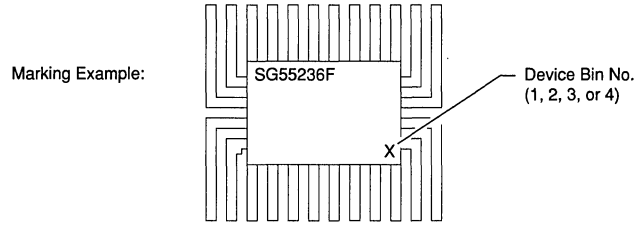
Note 14. The pulse generators have the following characteristics: $Z_o = 50\Omega$, $t_r = 15ns$, $t_f = 15ns$, $t_{w1} \geq 40ns$, $t_{w2} \geq 100ns$, PRR = 500KHz.
15. $C_{L(Y)}$ and $C_{L(Z)}$ include probe and jig capacitance.
16. All diodes are 1N3064.
17. Initially high output condition can be established by repetitive cycling.
18. Connections are shown for testing channel 1. To test channel 2, reverse connections of 1C and 2C along with inputs and outputs.

FUNCTIONAL DESCRIPTION

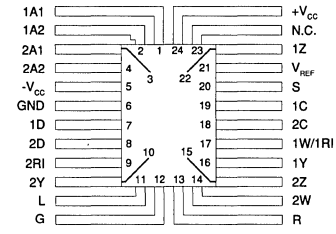
SG55236/55236A THRESHOLD VOLTAGE GRADING

The threshold voltages for each of the four sense amplifier inputs of the SG55236/55236A are compared to ensure that the maximum difference between channels does not exceed 1.5mV (SG55236) or 0.8mV (SG55236A). Devices that exceed this limit are rejected. The four threshold voltage values are averaged to determine the device's "bin" number (see below). The assigned bin number is marked in the lower right-hand corner of the devices. By using devices from the same bin, system performance is improved and the need for changing out sense amps due to trigger level differences is reduced.





CONNECTION DIAGRAMS & ORDERING INFORMATION (See Note Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
24-PIN CERAMIC FLAT PACK F - PACKAGE	SG55236AF/883B	-55°C to 125°C	
	SG55236AF	-55°C to 125°C	
	SG55236F/883B	-55°C to 125°C	
	SG55236F	-55°C to 125°C	

Note 1. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

DUAL SOURCE / DUAL SINK MEMORY DRIVER

DESCRIPTION

The SG55325/SG75325 is a monolithic dual source/dual sink driver designed to meet the high current and fast switching speed requirements of magnetic memory systems. Each driver can be independently selected through separate input logic. Also, each pair of drivers (sink or source pairs) has a separate strobe input to allow control of either pair of drivers. Each driver of the SG55325/SG75325 can switch 600mA.

Although used extensively in magnetic memory systems, this versatile driver has been used to drive relays, lamps, and small motors as well as being used as the driver in a clock circuit.

The SG55325 is characterized for use over the military ambient temperature range of -55°C to 125°C. The SG75325 has an operating ambient temperature range of 0°C to 70°C.

These devices are available in 16-pin ceramic DIP, 16-pin plastic DIP, and 16-pin flatpack.

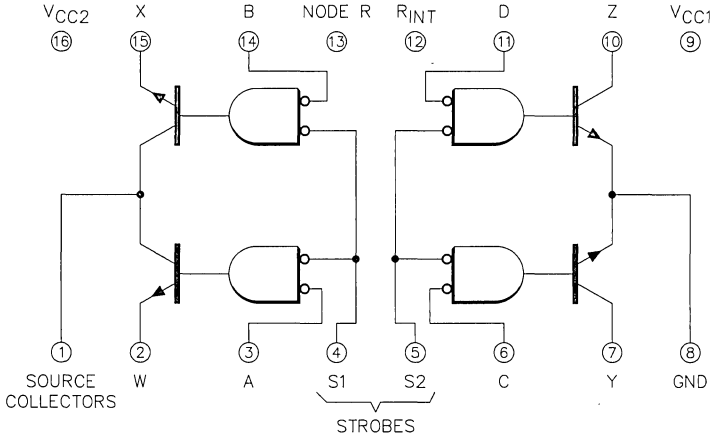
FEATURES

- **600mA output capability**
- **Fast switching times**
- **Output short-circuit protection**
- **24V output capability**
- **Source base drive externally adjustable**
- **TTL or DTL compatability**
- **Input clamping diodes**

HIGH RELIABILITY FEATURES - SG55325

- **Available to MIL-STD-883**
- **MIL-M-38510/13001BEA - JAN55325J**
- **Radiation data available**
- **SG level "S" processing available**

BLOCK DIAGRAM



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April 1990

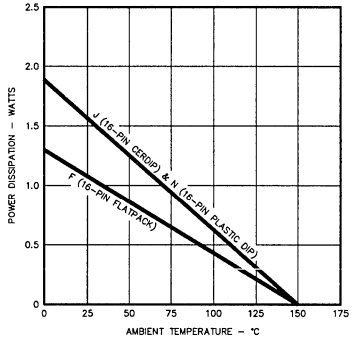
ABSOLUTE MAXIMUM RATINGS (Note1)

Supply Voltage (V_{CC1}) (Note 2) 7.0V
Supply Voltage (V_{CC2}) (Note 2) 25V
Input Voltage (any address or strobe input) 5.5V
Storage Temperature Range ..... -65°C to 150°C

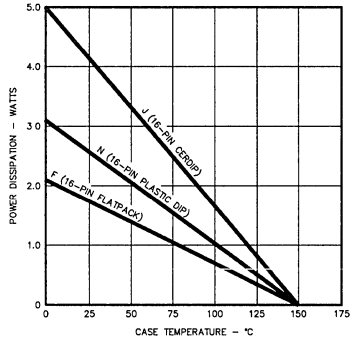
Operating Junction Temperature (T_C)
Hermetic (J, F-Packages) ..... 150°C
Plastic (N-Package) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1. Values beyond which damage may occur.
Note 2. Voltage values are with respect to network ground terminal.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 3)

Supply Voltage (V_{CC1}) ..... 4.5V to 5.5V
Supply Voltage (V_{CC2}) ..... 15V to 24V
Input Voltage ..... 0.4V to 5V

R_{EXT} (V_{CC2} = 24V) 100Ω
Operating Ambient Temperature Range:
SG55325 ..... -55°C to 125°C
SG75325 ..... 0°C to 70°C

Note 3. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG55325 with -55°C ≤ T_A ≤ 125°C, SG75325 with 0°C ≤ T_A ≤ 70°C, V_{CC1} = 5.5V, and V_{CC2} = 24V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG55325			SG75325			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Static Section								
High-Level Input Voltage (V_{IH})		2			2			V
Low-Level Input Voltage (V_{IL})				0.8			0.8	V
Input Clamp Voltage (V_{IK})	V_{CC1} = 4.5V, I_{IN} = -10mA, T_A = 25°C		-1.3	-1.7		-1.3	-1.7	V
Source-Collectors Terminal Off–State Current (I_{OFF})	V_{CC1} = 4.5V			500			200	µA
	V_{CC1} = 4.5V, T_A = 25°C		3.0	150		3.0	200	µA
High–Level Sink Output Voltage (V_{OH})	V_{CC1} = 4.5V, I_{OUT} = 0	19	23		19	23		V
Saturation Voltage (V_{SAT}) (Note 3)	V_{CC1} = 4.5V, V_{CC2} = 15V, R_L = 24Ω							
Source Outputs	I_{SOURCE} ≈ -600mA			0.90			0.90	V
	I_{SOURCE} ≈ -600mA, T_A = 25°C		0.43	0.70		0.43	0.75	V
Sink Outputs	I_{SINK} ≈ -600mA			0.90			0.90	V
	I_{SINK} ≈ -600mA, T_A = 25°C		0.43	0.70		0.43	0.75	V
Input Current (I_{IN})	At max. input voltage, V_{IN} = 5.5V							
Address Inputs				1			1	mA
Strobe Inputs				2			2	mA

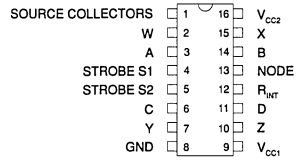
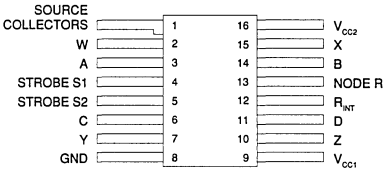
ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG55325			SG75325			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Static Section (continued)								
High-Level Input Current (I_{IH})	V_{IN} = 2.4V							
Address Inputs			3	40		3	40	µA
Strobe Inputs			6	80		6	80	µA
Low-Level Input Current (I_{IL})	V_{IN} = 0.4V							
Address Inputs			-1	-1.6		-1	-1.6	mA
Strobe Inputs			-2	-3.2		-2	-3.2	mA
Supply Current	All sources and sinks off, T_A = 25°C							
From V_{CC1}			14	22		14	22	mA
From V_{CC2}			7.5	20		7.5	20	mA
Supply Current From V_{CC1}	Either sink on, I_{SINK} = 50mA, T_A = 25°C		55	70		55	70	mA
Supply Current From V_{CC2} (Note 4)	Either source on, I_{SOURCE} = -50mA, T_A = 25°C		32	50		32	50	mA

Parameter	To (Outputs)	Test Conditions	SG55325/75325			Units
			Min.	Typ.	Max.	
Dynamic Section (Note 6)						
Propagation Delay, Low to High	Source Collectors			35	50	ns
(TPLH)	Sink Outputs			20	45	ns
Propagation Delay, High to Low	Source Collectors			35	50	ns
(TPHL)	Sink Outputs			20	45	ns
Transition Time, Low to High	Source Outputs	V_{CC2} = 20V, R_L = 1KΩ		55		ns
(TTLH)	Sink Outputs			7	15	ns
Transition Time, High to Low	Source Outputs	V_{CC2} = 20V, R_L = 1KΩ		7		ns
(TTHL)	Sink Outputs			9	20	ns
Storage Time (T_S)	Sink Outputs			15	30	ns

Note 4. These parameters must be measured using pulse techniques, T_W = 200ms, duty cycle ≤ 2%.
Note 5. Under these conditions, not more than one output is to be on at any one time.
Note 6. Unless otherwise specified, V_{CC1} = 5V, V_{CC2} = 15V, C_L = 25pF, R_L = 24Ω, and T_A = 25°C.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Note Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG55325J/883B SG55325J SG75325J	-55°C to 125°C -55°C to 125°C 0°C to 70°C	
16-PIN PLASTIC DIP N - PACKAGE	SG75325N	0°C to 70°C	
16-PIN CERAMIC FLAT PACK F - PACKAGE	SG55325F/883B SG55325F	-55°C to 125°C -55°C to 125°C	

Note 1. All packages are viewed from the top.

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SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

QUAD SINK MEMORY DRIVER

DESCRIPTION

The SG55326/SG75326 is a monolithic quad positive-OR sink driver designed to meet the high current and fast switching speed requirements of magnetic memory systems. Each driver is independently controlled and capable of sinking up to 600mA.

Paired with the SG55327 Quad Source Driver, the SG55326/SG75326 provides the current drive necessary for many sink/source applications.

Although designed specifically for magnetic memory applications, the SG55326/SG75326 has been used to drive clock circuits, relays, lamps, and small motors, or any application where a 600mA sink driver is needed.

The SG55326 is characterized for use over the full military operating ambient temperature range of -55°C to 125°C while the SG75326 is characterized over the operating ambient temperature of 0°C to 70°C.

These devices are available in 16-pin ceramic DIP, 16-pin plastic DIP, and 16-pin flatpack.

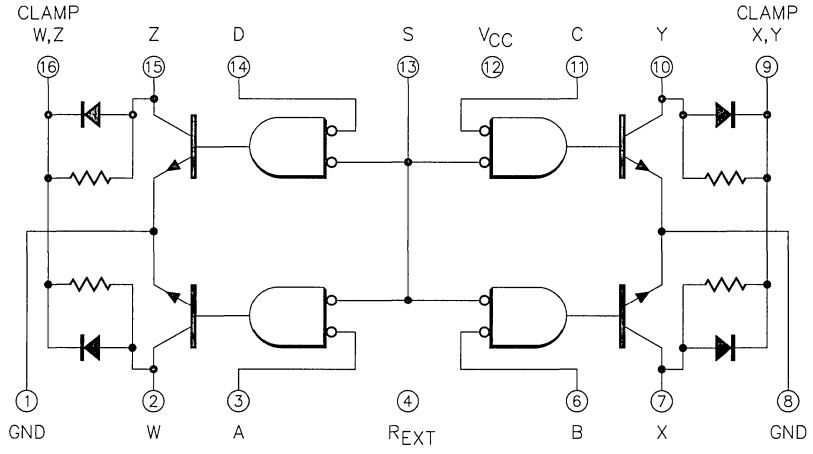
FEATURES

- **600mA output current sink capability**
- **24V output capability**
- **Clamp voltage variable to 24V**
- **High-repetition-rate driver compatible with high–speed magnetic memories**
- **Inputs compatible with TTL level decoders**
- **Minimum time skew between strobe and output–current rise**
- **Pulse-transformer coupling eliminated**
- **Drive-line lengths reduced**

HIGH RELIABILITY FEATURES - SG55326

- **Available to MIL-STD-883**
- **MIL-M-38510/13002BEA - JAN55326J**
- **SG level "S" processing available**

BLOCK DIAGRAM



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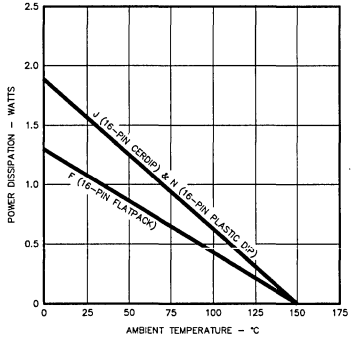
April 1990

ABSOLUTE MAXIMUM RATINGS (Note1)

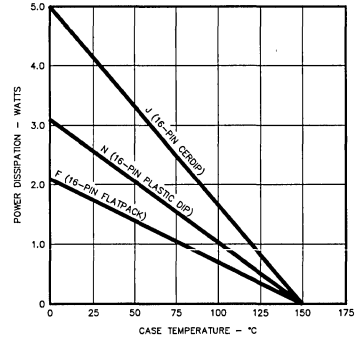
Supply Voltage (V_{CC}) (Note 2) 7.0V
Input Voltage (any address or strobe input) 5.5V
Output Collector Voltage 25V
Output Clamp Voltage 25V
Output Collector Current 750mA
Operating Ambient Temperature (T_C)
Hermetic (J, F-Packages) ..... 150°C
Plastic (N-Package) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1. Values beyond which damage may occur.
Note 2. Voltage values are with respect to network ground terminal.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 3)

Supply Voltage (V_{CC}) ..... 4.5V to 5.5V
Output Collector Voltage 24V
Output Clamp Voltage (V_{CLAMP}) ..... 4.5V to 24V
Output Collector Current 600mA
Operating Ambient Temperature Range:
SG55326 ..... -55°C to 125°C
SG75326 ..... 0°C to 70°C

Note 3. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG55326 with $-55°C \le T_A \le 125°C$, and SG75326 with $0°C \le T_A \le 70°C$. All typical values are measured at $T_A = 25°C$. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG55326			SG75326			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Static Section								
High-Level Input Voltage (V_{IH})		2			2			V
Low-Level Input Voltage (V_{IL})				0.8			0.8	V
Input Clamp Voltage (V_{IK})	V_{CC} = 4.5V, I_{IN} = -10mA, T_A = 25°C		-1.0	-1.7		-1.0	-1.7	V
High-Level Output Voltage (V_{OH})	V_{CC} = 4.5V, I_{OUT} = 0	19	23		19	23		V
Saturation Voltage (V_{SAT}) (Note 4)	V_{CC} = 4.5V, I_{SINK} = 600mA			0.9			0.9	V
	V_{CC} = 4.5V, I_{SINK} = 600mA, T_A = 25°C		0.43	0.70		0.43	0.75	V
Output-Clamp-Diode Forward Voltage ($V_{F(CLAMP)}$)	V_{CLAMP} = 0V, I_{CLAMP} = -10mA, T_A = 25°C			1.5			1.5	V
Output-Clamp Current (I_{CLAMP})	One Output On, I_{SINK} = 50mA, T_A = 25°C		5	7		5	7	mA
Input Current (I_{IN})	V_{IN} = 5.5V							
Address				1			1	mA
Strobe				4			4	mA
High-Level Input Current (I_{IH})	V_{IN} = 2.4V							
Address				40			40	µA
Strobe				160			160	µA

ELECTRICAL SPECIFICATIONS (continued)

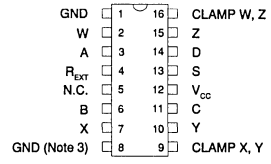
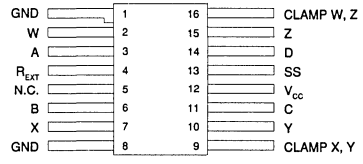
Parameter	Test Conditions	SG55326			SG75326			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Static Section (continued)								
Low-Level Input Current (I_{IL})	V_{IN} = 0.4V							
Address			-1.0	-1.6		-1.0	-1.6	mA
Strobe			-4.0	-6.4		-4.0	-6.4	mA
Supply Current	All outputs off, all inputs at 5V, T_A = 25°C		18	25		18	25	mA
Supply Current	One output on, I_{SINK} = 50mA, T_A = 25°C		58	75		58	75	mA

Parameter	To (Output)	Test Conditions	SG55326/75326			Units
			Min.	Typ.	Max.	
Dynamic Section (Note 5)						
Propagation Delay, Low to High (TPLH)	W, X, Y, or Z			30	50	ns
Propagation Delay, High to Low (TPHL)	W, X, Y, or Z			25	50	ns
Transition Time, Low to High (TTLH)	W, X, Y, or Z			7.0	15	ns
Transition Time, High to Low (TTHL)	W, X, Y, or Z			10	20	ns
Storage Time	W, X, Y, or Z			24	35	ns
High-Level Output Voltage (V_{OH})		$V_S = V_{CLAMP}$ = 24V, $I_{SINK} \approx$ 500mA, C_L = 25pF, R_L = 47Ω	V_S–25			mV

Note 4. Under these conditions, not more than one output is to be on at any one time.

Note 5. Unless otherwise specified, V_{CC} = 5V, $V_S = V_{CLAMP}$ = 15V, C_L = 25pF, R_L = 24Ω, and T_A = 25°C.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG55326J/883B SG55326J SG75326J	-55°C to 125°C -55°C to 125°C 0°C to 70°C	
16-PIN PLASTIC DIP N - PACKAGE	SG75326N	0°C to 70°C	
16-PIN CERAMIC FLAT PACK F - PACKAGE	SG55326F/883B SG55326F	-55°C to 125°C -55°C to 125°C	

Note 1. All packages are viewed from the top.
Note 2. Contact factory for LCC availability.
Note 3. Pin 8 is in electrical contact with the metal base.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

QUAD SOURCE MEMORY DRIVER

DESCRIPTION

The SG55327/SG75327 is a monolithic quad source driver designed to meet the high current and fast switching speed requirements of magnetic memory systems. Each driver is independently controlled and capable of sinking up to 600mA.

Paired with the SG55326 Quad Sink Driver, the SG55327/SG75327 provides the current drive necessary for many sink/source applications.

The SG55327/SG75327 has also been used in many non-memory applications: for example, as the driver for a clock circuit, relay, lamp, or small motor, or any application where a 600mA source driver is needed.

The SG55327 is characterized for use over the full military operating ambient temperature range of -55°C to 125°C while the SG75327 is characterized from 0°C to 70°C.

These devices are available in 16-pin ceramic DIP, 16-pin plastic DIP, and 16-pin flatpack.

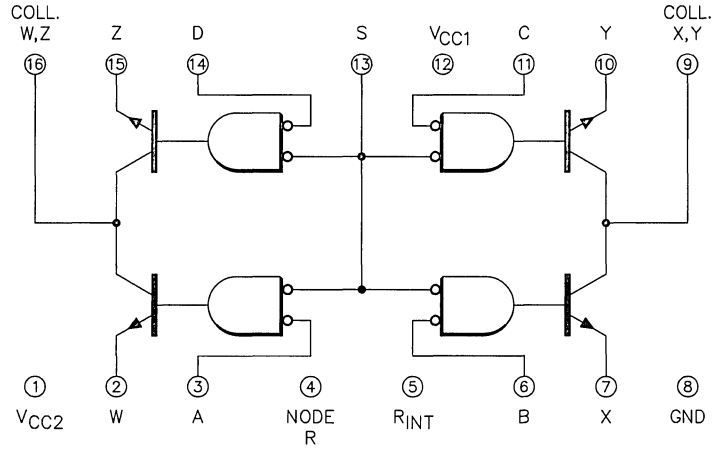
FEATURES

- **Quad source memory drivers**
- **600mA output current capability**
- **V_{CC2} drive voltage variable to 24V**
- **Output capable of swinging between V_{CC2} and ground**
- **High-repetition-rate driver compatible with high-speed magnetic memories**
- **Inputs compatible with TTL decoders**
- **Minimum time skew between strobe and output-current rise**
- **Pulse-transformer coupling eliminated**
- **Drive-line lengths reduced**

HIGH RELIABILITY FEATURES - SG55327

- **Available to MIL-STD-883**
- **Scheduled for MIL-M-38510 QPL listing**
- **SG level "S" processing available**

BLOCK DIAGRAM



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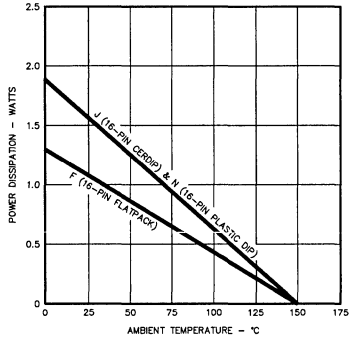
ABSOLUTE MAXIMUM RATINGS (Note1)

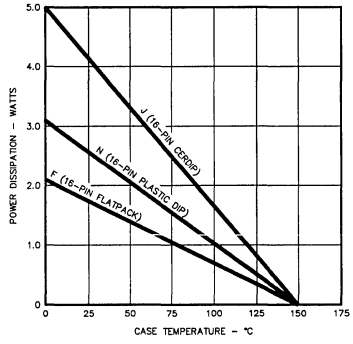
Supply Voltage (V_{CC1}) (Note 2) 7.0V
Supply Voltage (V_{CC2}) 25V
Input Voltage (any address or strobe input) 5.5V
Output Collector Voltage 25V
Output Collector Current 750mA
Operating Junction Temperature (T_C)
Hermetic (J, F-Packages) ..... 150°C
Plastic (N-Package) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1. Values beyond which damage may occur.
Note 2. Voltage values are with respect to network ground terminal.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 3)

Supply Voltage (V_{CC1}) ..... 4.5V to 5.5V
Supply Voltage (V_{CC2}) ..... 4.5V to 24V
Output Collector Voltage 24V
Output Collector Current 600mA
Operating Ambient Temperature Range:
SG55327 ..... -55°C to 125°C
SG75327 ..... 0°C to 70°C

Note 3. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG55327 with -55°C ≤ T_A ≤ 125°C, and SG75327 with 0°C ≤ T_A ≤ 70°C. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG55327			SG75327			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Static Section								
High-Level Input Voltage (V_{IH})		2			2			V
Low-Level Input Voltage (V_{IL})				0.8			0.8	V
Input Clamp Voltage (V_{IK})	V_{CC1} = 4.5V, I_{IN} = -10mA, T_A = 25°C		-1.0	-1.7		-1.0	-1.7	V
Collectors Terminal Off-State Current (I_{OFF})	V_{CC1} = 4.5V, V_{COL} = 24V			500			200	µA
	V_{CC1} = 4.5V, V_{COL} = 24V, T_A = 25°C			150			200	µA
Saturation Voltage (V_{SAT}) (Note 4)	V_{CC1} = 4.5V, V_{OUT} = 0V, I_{SOURCE} = –600mA			0.90			0.90	V
	T_A = 25°C		0.43	0.70		0.43	0.75	V
Input Current (I_{IN})	V_{IN} = 5.5V							
Address				1			1	mA
Strobe				4			4	mA
High-Level Input Current (I_{IH})	V_{IN} = 2.4V							
Address				40			40	µA
Strobe				160			160	µA
Low-Level Input Current (I_{IL})	V_{IN} = 0.4V							
Address			-1.0	-1.6		-1.0	-1.6	mA
Strobe			-4.0	-6.4		-4.0	-6.4	mA

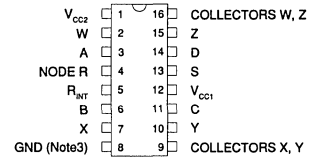
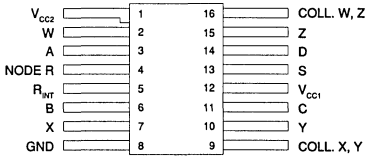
ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG55327			SG75327			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Static Section (continued)								
Supply Current ($I_{CC(OFF)}$)	All outputs off, all inputs at 5V, T_A = 25°C							
From V_{CC1}			7.0	10		7.0	10	mA
From V_{CC2}			13	20		13	20	mA
Supply Current ($I_{CC(ON)}$)	One output on, I_{SOURCE} = -50mA, V_{COL} = 6V, T_A = 25°C							
From V_{CC1}			8.0	12		8.0	12	mA
From V_{CC2}			36	55		36	55	mA

Parameter	To (output)	Test Conditions	SG55327/75327			Units
			Min.	Typ.	Max.	
Dynamic Section (Note 5)						
Propagation Delay, Low to High (TPLH)	Coll. W, Z or X, Y	$V_S = V_{CC2}$ = 15V, R_L = 24Ω		35	55	ns
Propagation Delay, High to Low (TPHL)	Coll. W, Z or X, Y	$V_S = V_{CC2}$ = 15V, R_L = 24Ω		30	55	ns
Transition Time, Low to High (TTLH)	W, X, Y, or Z	$V_{COL} = V_{CC2}$ = 20V, R_L = 100Ω		30		ns
Transition Time, High to Low (TTHL)	W, X, Y, or Z	$V_{COL} = V_{CC2}$ = 20V, R_L = 100Ω		10		ns
High-Level Output Voltage (V_{OH})	Coll. W, Z or X, Y	$V_S = V_{CC2}$ = 24V, R_L = 47Ω, I_{SINK} ≈ 500mA	V_S–25			mV

Note 4. Under these conditions, not more than one output is to be on any one time.
Note 5. Unless otherwise specified, V_{CC1} = 5V, C_L = 25pF, and T_A = 25°C.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG55327J/883B SG55327J SG75327J	-55°C to 125°C -55°C to 125°C 0°C to 70°C	
16-PIN PLASTIC DIP N - PACKAGE	SG75327N	0°C to 70°C	
16-PIN CERAMIC FLAT PACK F - PACKAGE	SG55327F/883B SG55327F	-55°C to 125°C -55°C to 125°C	

Note 1. All packages are viewed from the top.
Note 2. Contact factory for LCC.
Note 3. Pin 8 is in electrical contact with the metal base.

SELECTION GUIDE
AUTOMOTIVE CIRCUITS

LOW DROPOUT VOLTAGE REGULATORS

Device Type	Output Current	Output Voltages	Maximum Input Voltage	Initial Tolerance	Key Features	Packages
SG29055	0.75A	5V, 5V	26V	±5%	• Input / output differential less than 0.6V at 0.5A • Dual outputs • 5V / 10mA standby output • Low quiescent current in the standby mode • Reverse battery protection • 60V load dump protection • -50V Reverse transient protection • Thermal shutdown protection • ON/OFF switch for high current output • Available in 5 - pin TO-220 package	P
SG29055A	0.75A	5V, 5V	26V	±2%		
SG29085	0.75A	8V, 5V	26V	±5%		
SG29085A	0.75A	8V, 5V	26V	±2%		
SG29125	0.75A	12V, 5V	26V	±5%		
SG29125A	0.75A	12V, 5V	26V	±2%		

See General Information Section regarding capabilities for custom automotive circuits

December 1988

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

LOW DROPOUT DUAL REGULATOR

DESCRIPTION

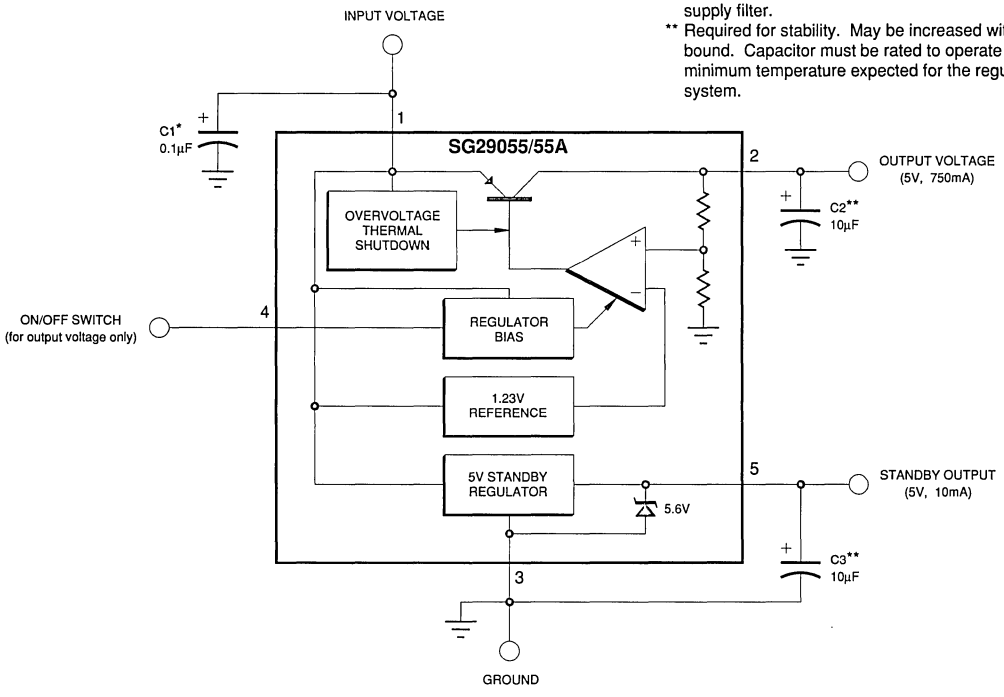
The SG29055/55A is a dual 5V/5V positive voltage regulator. One output is a high current (up to 750 mA) regulator that can be turned on or off by a high impedance low current TTL compatible switch. The second or standby output remains on regardless. The on/off switch not only shuts off the high current output but actually puts the IC in a micropower mode making possible a low quiescent current. This unique characteristic coupled with an extremely low dropout, (.55V for output current of 10mA) makes the SG29055/55A well suited for power systems that require standby memory. The SG29055/55A includes other features which were originally designed for automotive applications. These include protection from reverse battery installations and double battery jumps. The high current regulator has overvoltage shutdown to protect both the internal circuitry and the load during line transients, such as load dump (60V). In addition, the high current regulator design also has built-in protection for short circuit and thermal overload. During these fault conditions of the primary regulator the standby regulator will continue to power its load.

The SG29055 is the 5 volt, ±5% version of a family of dual regulators with a standby output voltage of 5V. Other high current outputs of 8.2V and 12V are available Also available is the SG29055A which offers an improved output voltage tolerance of ±2%. They are available in the plastic TO-220 power package and are designed to function over the automotive ambient temperature range of -40°C to 85°C.

FEATURES

- **2% Internally Trimmed Outputs**
- **Two regulated outputs**
- **Output current in excess of 750mA**
- **Low quiescent current standby regulator**
- **Input-output differential less than 0.6V at 0.5A**
- **Reverse battery protection**
- **60V load dump protection**
- **-50V reverse transient protection**
- **Short circuit protection**
- **Internal thermal overload protection**
- **Available in plastic TO-220**
- **ON/OFF switch for high current output**

TYPICAL APPLICATION CIRCUIT



* Required if regulator is located far from power supply filter.

** Required for stability. May be increased without bound. Capacitor must be rated to operate at the minimum temperature expected for the regulator system.

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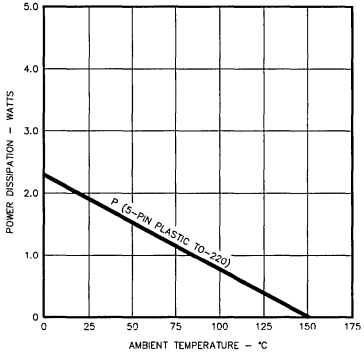
ABSOLUTE MAXIMUM RATINGS (Note 1)

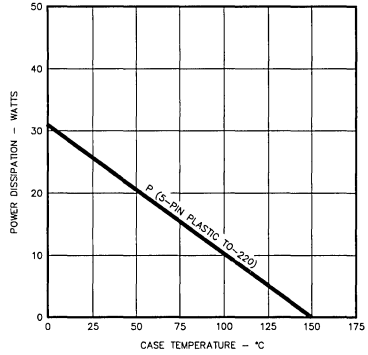
Input Voltage (V_{IN}) ..... -15V to 26V
ON/OFF Switch ..... -0.3V to V_{IN}
Storage Temperature Range (T_{STG}) ..... -65°C to 150°C
Operating Junction Temperature (T_J) ..... 150°C

Note 1. Exceeding these values may destroy this part. The SG29055/55A will not function properly at these maximum ratings.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Notes 2 & 3)

Input Voltage (V_{IN}) ..... 6V to 26V
ON/OFF Threshold Voltage
Low Level, V_{IL} (V_{OUT} is OFF) ..... 0.8V max.
High Level, V_{IH} (V_{OUT} is ON) ..... 2.0V min.
Load Current (with adequate heatsinking) ..... 5mA to 750mA
Maximum Line Transient (Load Dump) $V_O \leq 5.5V$ ..... 60V max.
Input Capacitor (V_{IN} to GND) ..... 0.1 µF min.
Reverse Polarity D.C. Input Voltage (V_{IN})
($V_O \geq -0.6V$, 16Ω load) ..... -15V max.
Reverse Polarity Transient Input Voltage (V_{IN})
(1% duty cycle, T ≤ 100ms, $V_O \geq -9V$, 16Ω load) ....-50V max.
Output Capacitor with ESR of 10Ω max.
(V_{OUT} to GND & V_{SB} to GND) ..... 10µF min.
Operating Ambient Temperature Range (T_J)
SG29055/55A ..... -40°C to 85°C

Note 2. Range over which the device is functional.
Note 3. During 60V load dump, V_{SB} shall not be less than 4.75V at I_{OUT} = 10mA.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply for the operating ambient temperature of T_A = 25°C. V_{IN} = 14V. I_O = 500mA for V_{OUT} and 10mA for V_{SB} and are for DC characteristics only. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

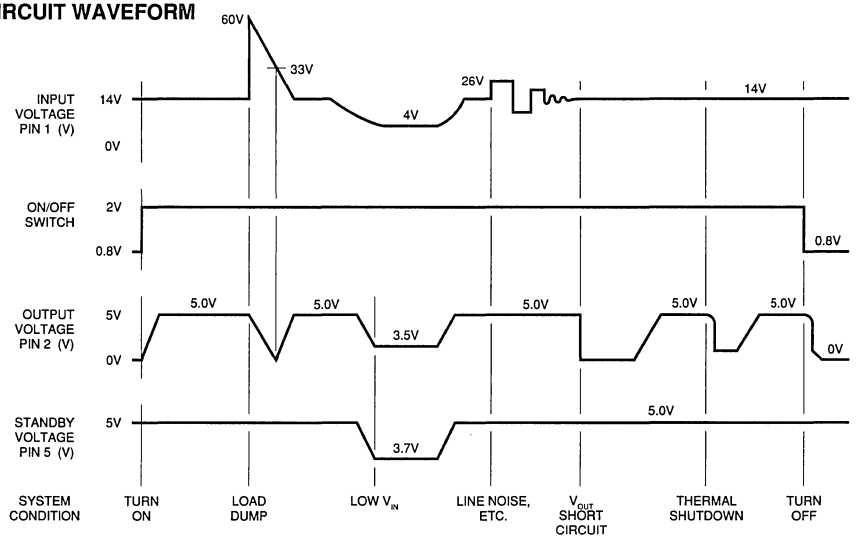
Parameter	Test Conditions	SG29055/55A			Units
		Min.	Typ.	Max.	
Voltage Output (V_{OUT}) Section					
Output Voltage (Note 4)	6V ≤ V_{IN} ≤ 26V, I_O ≤ 500mA, -40°C ≤ T_A ≤ 85°C				
	SG29055	4.75	5.00	5.25	V
	SG29055A	4.90	5.00	5.10	V
Line Regulation	9V ≤ V_{IN} ≤ 16V, I_O = 5mA		4	25	mV
	6V ≤ V_{IN} ≤ 26V, I_O = 5mA		10	50	mV
Load Regulation	5mA ≤ I_O ≤ 500mA		10	50	mV
Output Impedance	500mA$_{DC}$ and 10mA$_{RMS}$, 100Hz - 10kHz		200		Ω
Quiescent Current	I_O ≤ 10mA, No Load on Standby		3		mA
	I_O = 500mA, No Load on Standby		55	100	mA
	I_O = 750mA, No Load on Standby		120		mA
Output Noise Voltage	10Hz - 100kHz		100		µV_{RMS}
Long Term Stability			20		mV/1000hr
Ripple Rejection	F_O = 120Hz		66		dB
Dropout Voltage	I_O = 500mA		0.45	0.6	V
	I_O = 750mA		0.82		V
Current Limit		0.75	1.4		A
Maximum Operational Input Voltage		26	31		V
Maximum Line Transient	$V_O \leq 5.5V$	60	70		V
ON/OFF Switch (I_{IH})	I_O = 10mA, Pin 4 = 2.4V			10	µA
ON/OFF Switch (I_{IL})	I_O = 10mA, Pin 4 = 0.4V	-10			µA

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG29055/55A			Units
		Min.	Typ.	Max.	
Standby Output (V_{SB}) Section					
Output Voltage (Note 4)	$6V \le V_{IN} \le 26V$, $I_O \le 10mA$, $-40°C \le T_A \le 85°C$	4.75	5.0	5.25	V
Tracking	V_{OUT} - Standby Output Voltage		50	200	mV
Line Regulation	$6V \le V_{IN} \le 26V$		4	50	mV
Load Regulation	$1mA \le I_O \le 10mA$		10	50	mV
Output Impedance	$1mA_{DC}$ and $1mA_{RMS}$, 100Hz - 10kHz		1		Ω
Quiescent Current	$I_O \le 10mA$, V_{OUT}OFF		1.2	3	mA
Output Noise Voltage	10Hz - 100kHz		300		μV_{RMS}
Long Term Stability			20		mV/1000hr
Ripple Rejection	F_O = 120Hz		66		dB
Dropout Voltage	$I_O \le 10mA$		0.55	0.7	V
Current Limit		25	70		mA
Maximum Operational Input Voltage	$4.5V \le V_O \le 6V$	60	70		V

Note 4. The temperature extremes are guaranteed but not 100% production tested.

TYPICAL CIRCUIT WAVEFORM



APPLICATION NOTES

The advantages of using a low-dropout regulator such as the SG29055/55A are the need for less "headroom" for full regulation, and the inherent reverse polarity protection provided by the PNP output device. A typical NPN regulator design requires an input to output differential of approximately two volts minimum. This is due to the 2Vbe + Vcesat of the NPN Darlington used in the output, coupled with the voltage drop across the current limit resistor. In contrast, the "PNP Regulator" uses a single series pass transistor with its single Vcesat, thus the lower input to output voltage differential or dropout voltage.

In addition to a low dropout voltage, an important advantage of the SG29055/55A series is low quiescent current in the standby mode. When the high current or primary regulator is shut off, the regulator enters a micropower mode. Here all but the most essential circuitry to power the standby output is deactivated. This allows the lowest possible quiescent current (typical around 1.2mA), a vital factor when used in a battery powered system.

In some applications the regulator output voltage is used not only as a power supply but also as a voltage reference for control systems. In such cases not just the temperature stability of the output is important but also the initial accuracy. The SG29055/55A fills this need as the internal bandgap reference is trimmed allowing a typical output voltage tolerance of ±1%.

APPLICATION HINTS

EXTERNAL CAPACITORS

To stabilize the outputs and prevent oscillation (perhaps by many volts) external capacitors are required. The minimum recommended value for the output capacitors is 10µF, although the actual size and type will likely vary according to the particular application, e.g., operating temperature range and load. Another consideration is the effective series resistance (ESR) of the capacitor. Capacitor ESR will vary by manufacturer. Consequently, some evaluation may be required to determine the minimum value of the output capacitors. Generally worst case occurs at the maximum load and minimum ambient temperature.

The size of the output capacitor can be increased to any value above the minimum. One possible advantage of this would be to maintain the output voltage during brief periods of negative input transients

The output capacitors chosen should be rated for the full range of ambient temperature over which the circuit will be exposed and expected to operate. For example, many aluminum type electrolytic capacitors will freeze at -30°C. The effective capacitance is reduced to zero in such a situation. Capacitors rated for -40°C operation must be used in order to maintain regulator stability at that temperature. Tantalum capacitors satisfy this requirement.

STANDBY OUTPUT

The SG29055/55A differs from most fixed voltage regulators in that it is equipped with two regulator outputs instead of one. The additional output is intended for use in systems requiring standby memory circuits. While the high current regulator output can be controlled with the ON/OFF pin described below, the standby remains on under all conditions as long as sufficient input voltage is applied to the IC. Thus, memory and other circuits powered by this output remain unaffected by positive line transients, thermal shutdown, etc.

The standby regulator circuit is designed so that the quiescent current to the IC is very low (<1.5mA) when the other regulator output is off.

If the standby output is not required it can be disabled. This is accomplished by connecting a resistor from the standby output to the supply voltage, thereby also eliminating the requirement for a more expensive output capacitor to prevent unwanted oscillations. The resistor value depends upon the minimum input voltage expected for a given system.

Since the standby output is shunted with an internal 5.6V zener, the current through the external resistor should be sufficient to bias internal resistors up to this point. Approximately 60µF will suffice, resulting in a 10k external resistor for most applications (Figure 1).

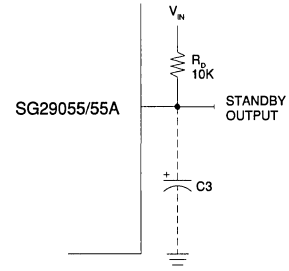


FIGURE 1. Disabling Standby Output to Eliminate C3

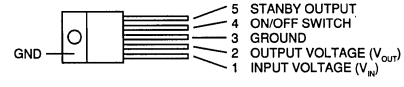
HIGH CURRENT OUTPUT

The high current regulated output features fault protection against overvoltage as well as a thermal shutdown feature. If the input voltage rises above 33V (load dump), the high current output shuts down automatically. The internal circuitry is thus protected and the IC is able to survive higher voltage transients than might otherwise be expected. The thermal shutdown of the high current output effectively guards against overheating of the die since this section of the IC is the principle source of power dissipation on the chip.

ON/OFF SWITCH

The ON/OFF pin is a high impedance low current switch that controls the main output voltage (pin 2). This is directly compatible with all 5 volt logic families. For use with open collector logic outputs, a 100k resistor from this pin to a 5V supply, such as Pin 5, is required.

CONNECTION DIAGRAM & ORDERING INFORMATION (See Note Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
5-PIN TO-220 PLASTIC P - PACKAGE	SG29055P SG29055AP	-40°C to 85°C -40°C to 85°C	

Note: 1. All parts are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

LOW DROPOUT DUAL REGULATOR

DESCRIPTION

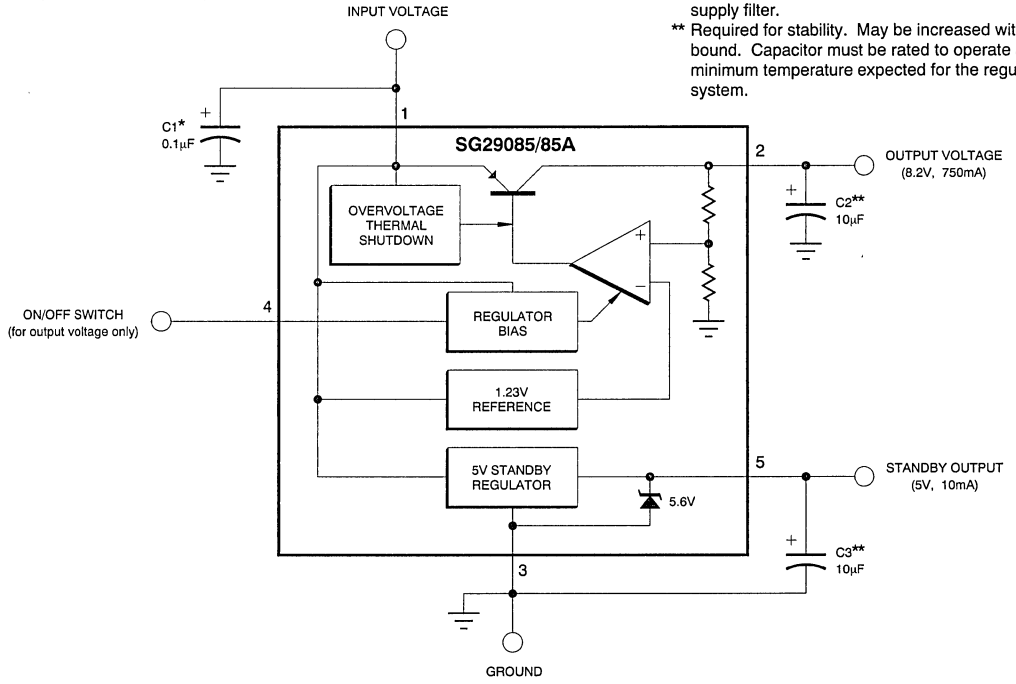
The SG29085/85A is a dual 8.2V/5V positive voltage regulator. One output is a high current (up to 750 mA) regulator that can be turned on or off by a high impedance low current TTL compatible switch. The second or standby output remains on regardless. The on/off switch not only shuts off the high current output but actually puts the IC in a micropower mode making possible a low quiescent current. This unique characteristic coupled with an extremely low dropout, (.55V for output current of 10mA) makes the SG29085/85A well suited for power systems that require standby memory. The SG29085/85A includes other features which were originally designed for automotive applications. These include protection from reverse battery installations and double battery jumps. The high current regulator has overvoltage shutdown to protect both the internal circuitry and the load during line transients, such as load dump (60V). In addition, the high current regulator design also has built-in protection for short circuit and thermal overload. During these fault conditions of the primary regulator the standby regulator will continue to power its load.

The SG29085 is the 8.2 volt, ±5% version of a family of dual regulators with a standby output voltage of 5V. Other high current outputs of 5 and 12 volts are available. Also available is the SG28085A which offers an improved output voltage tolerance of ±2%. They are available in the plastic TO-220 power package and are designed to function over the automotive ambient temperature range of -40°C to 85°C.

FEATURES

- **2% Internally Trimmed Outputs**
- **Two regulated outputs**
- **Output current in excess of 750mA**
- **Low quiescent current standby regulator**
- **Input-output differential less than 0.6V at 0.5A**
- **Reverse battery protection**
- **60V load dump protection**
- **-50V reverse transient protection**
- **Short circuit protection**
- **Internal thermal overload protection**
- **Available in plastic TO-220**
- **ON/OFF switch for high current output**

TYPICAL APPLICATION CIRCUIT



* Required if regulator is located far from power supply filter.

** Required for stability. May be increased without bound. Capacitor must be rated to operate at the minimum temperature expected for the regulator system.

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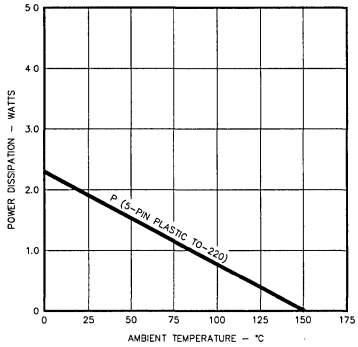
ABSOLUTE MAXIMUM RATINGS (Note 1)

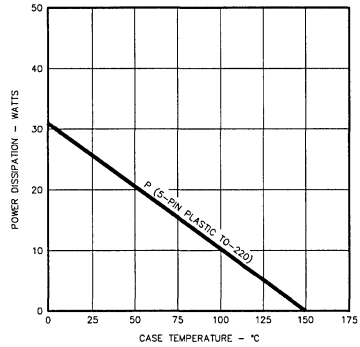
Input Voltage (V_{IN}) ..... -15V to 26V
ON/OFF Switch ..... -0.3V to V_{IN}
Storage Temperature Range (T_{STG}) ..... -65°C to 150°C
Operating Junction Temperature (T_J) ..... 150°C

Note 1. Exceeding these values may destroy this part. The SG29085 and SG29085A will not function properly at these maximum ratings.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Notes 2 & 3)

Input Voltage (V_{IN}) ..... 9V to 26V
ON/OFF Threshold Voltage
  Low Level, V_{IL} (V_{OUT} is OFF) ..... 0.8V max.
  High Level, V_{IH} (V_{OUT} is ON) ..... 2.0V min.
Load Current (with adequate heatsinking) ..... 5mA to 750mA
Maximum Line Transient (Load Dump) $V_O \leq 5.5V$ ..... 60V max.
Input Capacitor (V_{IN} to GND) ..... 0.1 µF min.
Reverse Polarity D.C. Input Voltage (V_{IN})
  ($V_O \geq -0.6V$, 16Ω load) ..... -15V max.
Reverse Polarity Transient Input Voltage (V_{IN})
  (1% duty cycle, $T \leq 100ms$, $V_O \geq -9V$, 16Ω load) ... -50V max.
Output Capacitor with ESR of 10Ω max.
  (V_{OUT} to GND & V_{SB} to GND) ..... 10µF min.
Operating Ambient Temperature Range - (T_J)
  SG29085/85A ..... -40°C to 85°C

Note 2. Range over which the device is functional.
Note 3. During 60V load dump, V_{SB} shall not be less than 4.75V at I_{OUT} = 10mA.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply for the operating ambient temperature of T_A = 25°C. V_{IN} = 14V, I_O = 500mA for V_{OUT} and 10mA for V_{SB} and are for DC characteristics only. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

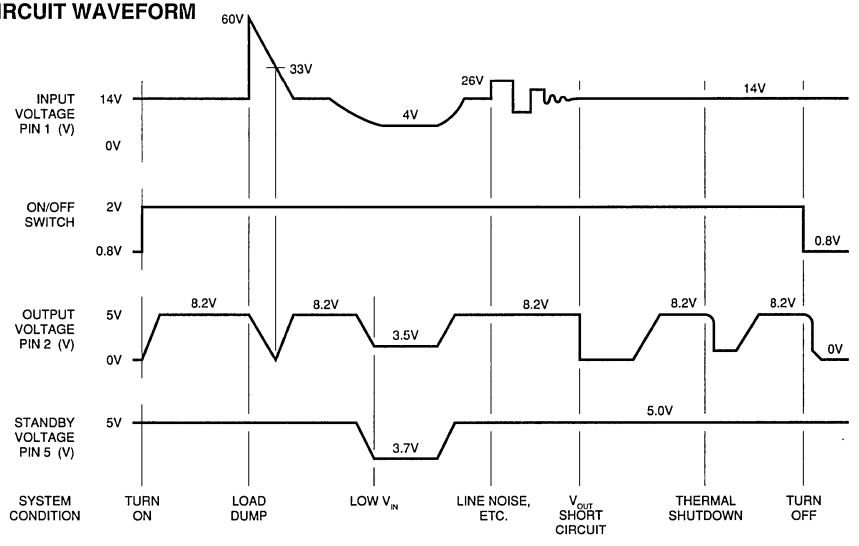
Parameter	Test Conditions	SG29085/85A			Units
		Min.	Typ.	Max.	
Voltage Output (V_{OUT}) Section					
Output Voltage (Note 4)	9V ≤ V_{IN} ≤ 26V, I_O ≤ 500mA, -40°C ≤ T_A ≤ 85°C				
	SG29085	7.8	8.2	8.6	V
	SG29085A	8.0	8.2	8.4	V
Line Regulation	9V ≤ V_{IN} ≤ 16V, I_O = 5mA		4	25	mV
	9V ≤ V_{IN} ≤ 26V, I_O = 5mA		10	50	mV
Load Regulation	5mA ≤ I_O ≤ 500mA		10	50	mV
Output Impedance	500mA$_{DC}$ and 10mA$_{RMS}$, 100Hz - 10kHz		200		Ω
Quiescent Current	I_O ≤ 10mA, No Load on Standby		3		mA
	I_O = 500mA, No Load on Standby		55	100	mA
	I_O = 750mA, No Load on Standby		120		mA
Output Noise Voltage	10Hz - 100kHz		100		µV$_{RMS}$
Long Term Stability			20		mV/1000hr
Ripple Rejection	F_O = 120Hz		66		dB
Dropout Voltage	I_O = 500mA		0.45	0.6	V
	I_O = 750mA	0.75	0.82		V
Current Limit			1.4		A
Maximum Operational Input Voltage		60	31		V
Maximum Line Transient	$V_O \leq 9V$		70		V
ON/OFF Switch (I_{IH})	I_O = 10mA, Pin 4 = 2.4V			10	µA
ON/OFF Switch (I_{IL})	I_O = 10mA, Pin 4 = 0.4V	-10			µA

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG29085/85A			Units
		Min.	Typ.	Max.	
Standby Output (V_{SB}) Section					
Output Voltage (Note 4)	$6V \le V_{IN} \le 26V$, $I_O \le 10mA$, $-40°C \le T_A \le 85°C$	4.75	5.0	5.25	V
Tracking	V_{OUT} - Standby Output Voltage		50	200	mV
Line Regulation	$6V \le V_{IN} \le 26V$		4	50	mV
Load Regulation	$1mA \le I_O \le 10mA$		10	50	mV
Output Impedance	$1mA_{DC}$ and $1mA_{RMS}$, 100Hz - 10kHz		1		Ω
Quiescent Current	$I_O \le 10mA$, V_{OUT}OFF		1.2	3	mA
Output Noise Voltage	10Hz - 100kHz		300		μV_{RMS}
Long Term Stability			20		mV/1000hr
Ripple Rejection	F_O = 120Hz		66		dB
Dropout Voltage	$I_O \le 10mA$		0.55	0.7	V
Current Limit		25	70		mA
Maximum Operational Input Voltage	$4.5V \le V_O \le 6V$	60	70		V

Note 4. The temperature extremes are guaranteed but not 100% production tested.

TYPICAL CIRCUIT WAVEFORM



APPLICATION NOTES

The advantages of using a low-dropout regulator such as the SG29085/85A are the need for less "headroom" for full regulation, and the inherent reverse polarity protection provided by the PNP output device. A typical NPN regulator design requires an input to output differential of approximately two volts minimum. This is due to the 2Vbe + Vcesat of the NPN Darlington used in the output, coupled with the voltage drop across the current limit resistor. In contrast, the "PNP Regulator" uses a single series pass transistor with its single Vcesat, thus the lower input to output voltage differential or dropout voltage.

In addition to a low dropout voltage, an important advantage of the SG29085/85A series is low quiescent current in the standby mode. When the high current or primary regulator is shut off, the regulator enters a micropower mode. Here all but the most essential circuitry to power the standby output is deactivated. This allows the lowest possible quiescent current (typical around 1.2mA), a vital factor when used in a battery powered system.

In some applications the regulator output voltage is used not only as a power supply but also as a voltage reference for control systems. In such cases not just the temperature stability of the output is important but also the initial accuracy. The SG29085/85A fills this need as the internal bandgap reference is trimmed allowing a typical output voltage tolerance of ±1%.

APPLICATION HINTS

EXTERNAL CAPACITORS

To stabilize the outputs and prevent oscillation (perhaps by many volts) external capacitors are required. The minimum recommended value for the output capacitors is 10µF, although the actual size and type will likely vary according to the particular application, e.g., operating temperature range and load. Another consideration is the effective series resistance (ESR) of the capacitor. Capacitor ESR will vary by manufacturer. Consequently, some evaluation may be required to determine the minimum value of the output capacitors. Generally worst case occurs at the maximum load and minimum ambient temperature.

The size of the output capacitor can be increased to any value above the minimum. One possible advantage of this would be to maintain the output voltage during brief periods of negative input transients

The output capacitors chosen should be rated for the full range of ambient temperature over which the circuit will be exposed and expected to operate. For example, many aluminum type electrolytic capacitors will freeze at -30°C. The effective capacitance is reduced to zero in such a situation. Capacitors rated for -40°C operation must be used in order to maintain regulator stability at that temperature. Tantalum capacitors satisfy this requirement.

STANDBY OUTPUT

The SG29085/85A differs from most fixed voltage regulators in that it is equipped with two regulator outputs instead of one. The additional output is intended for use in systems requiring standby memory circuits. While the high current regulator output can be controlled with the ON/OFF pin described below, the standby remains on under all conditions as long as sufficient input voltage is applied to the IC. Thus, memory and other circuits powered by this output remain unaffected by positive line transients, thermal shutdown, etc.

The standby regulator circuit is designed so that the quiescent current to the IC is very low (<1.5mA) when the other regulator output is off.

If the standby output is not required it can be disabled. This is accomplished by connecting a resistor from the standby output to the supply voltage, thereby also eliminating the requirement for a more expensive output capacitor to prevent unwanted oscillations. The resistor value depends upon the minimum input voltage expected for a given system.

Since the standby output is shunted with an internal 5.6V zener, the current through the external resistor should be sufficient to bias internal resistors up to this point. Approximately 60µF will suffice, resulting in a 10k external resistor for most applications (Figure 1).

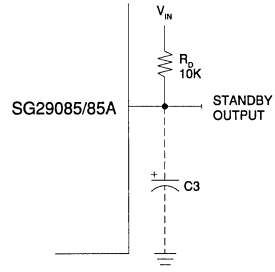


FIGURE 1. Disabling Standby Output to Eliminate C3

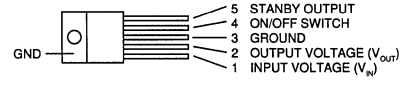
HIGH CURRENT OUTPUT

The high current regulated output features fault protection against overvoltage as well as a thermal shutdown feature. If the input voltage rises above 33V (load dump), the high current output shuts down automatically. The internal circuitry is thus protected and the IC is able to survive higher voltage transients than might otherwise be expected. The thermal shutdown of the high current output effectively guards against overheating of the die since this section of the IC is the principle source of power dissipation on the chip.

ON/OFF SWITCH

The ON/OFF pin is a high impedance low current switch that controls the main output voltage (pin 2). This is directly compatible with all 5 volt logic families. For use with open collector logic outputs, a 100k resistor from this pin to a 5V supply, such as Pin 5, is required.

CONNECTION DIAGRAM & ORDERING INFORMATION (See Note Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
5-PIN TO-220 PLASTIC P - PACKAGE	SG29085P SG29085AP	-40°C to 85°C -40°C to 85°C	

Note: 1. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

LOW DROPOUT DUAL REGULATOR

DESCRIPTION

The SG29125/125A is a dual 12V/5V positive voltage regulator. One output is a high current (up to 750 mA) regulator that can be turned on or off by a high impedance low current TTL compatible switch. The second or standby output remains on regardless. The on/off switch not only shuts off the high current output but actually puts the IC in a micropower mode making possible a low quiescent current. This unique characteristic coupled with an extremely low dropout, (.55V for output current of 10mA) makes the SG29125/125A well suited for power systems that require standby memory. The SG29125/125A includes other features which were originally designed for automotive applications. These include protection from reverse battery installations and double battery jumps. The high current regulator has overvoltage shutdown to protect both the internal circuitry and the load during line transients, such as load dump (60V). In addition, the high current regulator design also has built-in protection for short circuit and thermal overload. During these fault conditions of the primary regulator the standby regulator will continue to power its load.

The SG29125 is the 12 volt, ±5% version of a family of dual regulators with a standby output voltage of 5V. Other high current outputs of 5 and 8.2 volts are available. Also available is the SG29125A which offers an improved output voltage tolerance of ±2%. They are available in the plastic TO-220 power package and are designed to function over the automotive ambient temperature range of -40°C to 85°C.

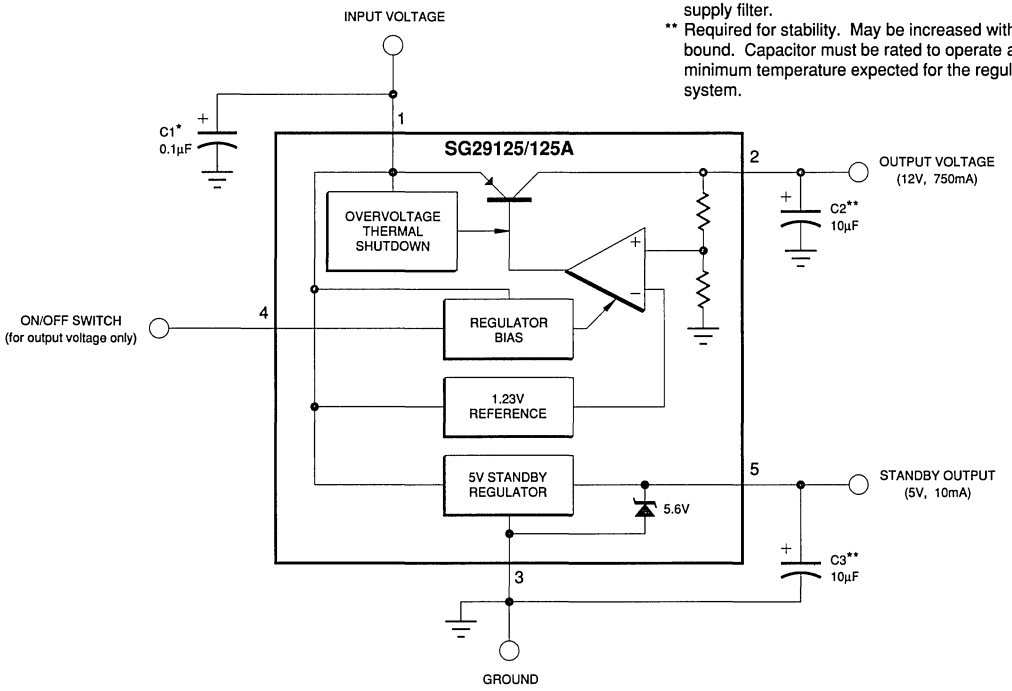
FEATURES

- **2% Internally Trimmed Outputs**
- **Two regulated outputs**
- **Output current in excess of 750mA**
- **Low quiescent current standby regulator**
- **Input-output differential less than 0.6V at 0.5A**
- **Reverse battery protection**
- **60V load dump protection**
- **-50V reverse transient protection**
- **Short circuit protection**
- **Internal thermal overload protection**
- **Available in plastic TO-220**
- **ON/OFF switch for high current output**

TYPICAL APPLICATION CIRCUIT

* Required if regulator is located far from power supply filter.

** Required for stability. May be increased without bound. Capacitor must be rated to operate at the minimum temperature expected for the regulator system.



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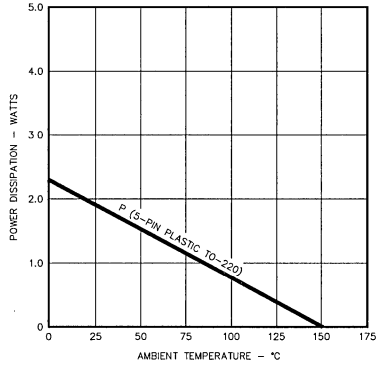
ABSOLUTE MAXIMUM RATINGS (Note 1)

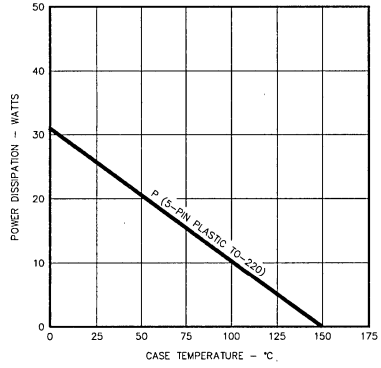
Input Voltage (V_{IN}) ..... -15V to 26V
ON/OFF Switch ..... -0.3V to V_{IN}
Storage Temperature Range (T_{STG}) ..... -65°C to 150°C
Operating Junction Temperature (T_J) ..... 150°C

Note 1. Exceeding these values may destroy this part. The SG29125 and SG29125A will not function properly at these maximum ratings.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2 & 3)

Input Voltage (V_{IN}) .....13V to 26V
ON/OFF Threshold Voltage
  Low Level, V_{IL} (V_{OUT} is OFF) ..... 0.8V max.
  High Level, V_{IH} (V_{OUT} is ON) ..... 2.0V min.
Load Current (with adequate heatsinking) ..... 5mA to 750mA
Maximum Line Transient (Load Dump) $V_O \leq 5.5V$ ..... 60V max.
Input Capacitor (V_{IN} to GND) ..... 0.1 µF min.

Reverse Polarity D.C. Input Voltage (V_{IN})
  ($V_O \geq -0.6V$, 16Ω load) ..... -15V max.
Reverse Polarity Transient Input Voltage (V_{IN})
  (1% duty cycle, T ≤ 100ms, $V_O \geq -9V$, 16Ω load) ... -50V max.
Output Capacitor with ESR of 10Ω max.
  (V_{OUT} to GND & V_{SB} to GND) ..... 10µF min.
Operating Ambient Temperature Range (T_J)
  SG29125/125A ..... -40°C to 85°C

Note 2. Range over which the device is functional.
Note 3. During 60V load dump, V_{SB} shall not be less than 4.75V at I_{OUT} = 10mA.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply for the operating ambient temperature of T_A = 25°C, V_{IN} = 14V, I_O = 500mA for V_{OUT} and 10mA for V_{SB} and are for DC characteristics only. Low duty cycle pulse testing techniques are used which maintains junction and cae temperatures equal to the ambient temperature.)

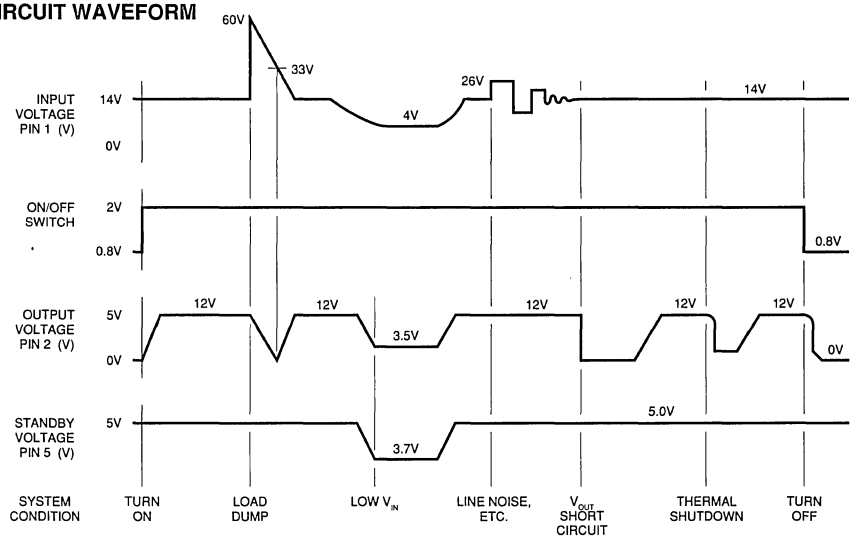
Parameter	Test Conditions	SG29125/125A			Units
		Min.	Typ.	Max.	
Voltage Output (V_{OUT}) Section					
Output Voltage (Note 4)	13V ≤ V_{IN} ≤ 26V, I_O ≤ 500mA, -40°C ≤ T_A ≤ 85°C				
	SG29125	11.2	12	12.8	V
	SG29125A	11.75	12	12.25	V
Line Regulation	13V ≤ V_{IN} ≤ 16V, I_O = 5mA		4	25	mV
	13V ≤ V_{IN} ≤ 26V, I_O = 5mA		10	50	mV
Load Regulation	5mA ≤ I_O ≤ 500mA		10	50	mV
Output Impedance	500mA_{DC} and 10mA_{RMS}, 100Hz - 10kHz		200		Ω
Quiescent Current	I_O ≤ 10mA, No Load on Standby		3		mA
	I_O = 500mA, No Load on Standby		55	100	mA
	I_O = 750mA, No Load on Standby		120		mA
Output Noise Voltage	10Hz - 100kHz		100		μV_{RMS}
Long Term Stability			20		mV/1000hr
Ripple Rejection	F_O = 120Hz		66		dB
Dropout Voltage	I_O = 500mA		0.45	0.6	V
	I_O = 750mA	0.75	0.82		V
Current Limit		26	1.4		A
Maximum Operational Input Voltage		60	31		V
Maximum Line Transient	V_O ≤ 13V		70		V
ON/OFF Switch (I_{IH})	I_O = 10mA, Pin 4 = 2.4V			10	µA
ON/OFF Switch (I_{IL})	I_O = 10mA, Pin 4 = 0.4V	-10			µA

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG29125/125A			Units
		Min.	Typ.	Max.	
Standby Output (V_{SB}) Section					
Output Voltage (Note 4)	$6V \le V_{IN} \le 26V$, $I_O \le 10mA$, $-40°C \le T_A \le 85°C$	4.75	5.0	5.25	V
Tracking	V_{OUT} - Standby Output Voltage		50	200	mV
Line Regulation	$6V \le V_{IN} \le 26V$		4	50	mV
Load Regulation	$1mA \le I_O \le 10mA$		10	50	mV
Output Impedance	$1mA_{DC}$ and $1mA_{RMS}$, 100Hz - 10kHz		1		Ω
Quiescent Current	$I_O \le 10mA$, V_{OUT}OFF		1.2	3	mA
Output Noise Voltage	10Hz - 100kHz		300		μV_{RMS}
Long Term Stability			20		mV/1000hr
Ripple Rejection	F_O = 120Hz		66		dB
Dropout Voltage	$I_O \le 10mA$		0.55	0.7	V
Current Limit		25	70		mA
Maximum Operational Input Voltage	$4.5V \le V_O \le 6V$	60	70		V

Note 4. The temperature extremes are guaranteed but not 100% production tested.

TYPICAL CIRCUIT WAVEFORM



APPLICATION NOTES

The advantages of using a low-dropout regulator such as the SG29125/125A are the need for less "headroom" for full regulation, and the inherent reverse polarity protection provided by the PNP output device. A typical NPN regulator design requires an input to output differential of approximately two volts minimum. This is due to the 2Vbe + Vcesat of the NPN Darlington used in the output, coupled with the voltage drop across the current limit resistor. In contrast, the "PNP Regulator" uses a single series pass transistor with its single Vcesat, thus the lower input to output voltage differential or dropout voltage.

In addition to a low dropout voltage, an important advantage of the SG29125/125A series is low quiescent current in the standby mode. When the high current or primary regulator is shut off, the regulator enters a micropower mode. Here all but the most essential circuitry to power the standby output is deactivated. This allows the lowest possible quiescent current (typical around 1.2mA), a vital factor when used in a battery powered system.

In some applications the regulator output voltage is used not only as a power supply but also as a voltage reference for control systems. In such cases not just the temperature stability of the output is important but also the initial accuracy. The SG29125/125A fills this need as the internal bandgap reference is trimmed allowing a typical output voltage tolerance of ±1%.

APPLICATION HINTS

EXTERNAL CAPACITORS

To stabilize the outputs and prevent oscillation (perhaps by many volts) external capacitors are required. The minimum recommended value for the output capacitors is 10µF, although the actual size and type will likely vary according to the particular application, e.g., operating temperature range and load. Another consideration is the effective series resistance (ESR) of the capacitor. Capacitor ESR will vary by manufacturer. Consequently, some evaluation may be required to determine the minimum value of the output capacitors. Generally worst case occurs at the maximum load and minimum ambient temperature.

The size of the output capacitor can be increased to any value above the minimum. One possible advantage of this would be to maintain the output voltage during brief periods of negative input transients

The output capacitors chosen should be rated for the full range of ambient temperature over which the circuit will be exposed and expected to operate. For example, many aluminum type electrolytic capacitors will freeze at -30°C. The effective capacitance is reduced to zero in such a situation. Capacitors rated for -40°C operation must be used in order to maintain regulator stability at that temperature. Tantalum capacitors satisfy this requirement.

STANDBY OUTPUT

The SG29125/125A differs from most fixed voltage regulators in that it is equipped with two regulator outputs instead of one. The additional output is intended for use in systems requiring standby memory circuits. While the high current regulator output can be controlled with the ON/OFF pin described below, the standby remains on under all conditions as long as sufficient input voltage is applied to the IC. Thus, memory and other circuits powered by this output remain unaffected by positive line transients, thermal shutdown, etc.

The standby regulator circuit is designed so that the quiescent current to the IC is very low (<1.5mA) when the other regulator output is off.

If the standby output is not required it can be disabled. This is accomplished by connecting a resistor from the standby output to the supply voltage, thereby also eliminating the requirement for a more expensive output capacitor to prevent unwanted oscillations. The resistor value depends upon the minimum input voltage expected for a given system.

Since the standby output is shunted with an internal 5.6V zener, the current through the external resistor should be sufficient to bias internal resistors up to this point. Approximately 60µF will suffice, resulting in a 10k external resistor for most applications (Figure 1).

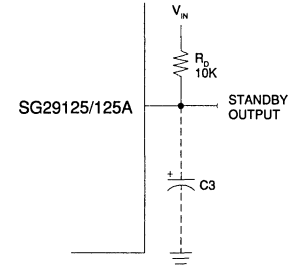


FIGURE 1. Disabling Standby Output to Eliminate C3

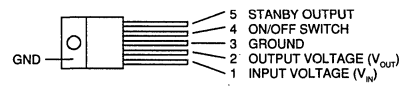
HIGH CURRENT OUTPUT

The high current regulated output features fault protection against overvoltage as well as a thermal shutdown feature. If the input voltage rises above 33V (load dump), the high current output shuts down automatically. The internal circuitry is thus protected and the IC is able to survive higher voltage transients than might otherwise be expected. The thermal shutdown of the high current output effectively guards against overheating of the die since this section of the IC is the principle source of power dissipation on the chip.

ON/OFF SWITCH

The ON/OFF pin is a high impedance low current switch that controls the main output voltage (pin 2). This is directly compatible with all 5 volt logic families. For use with open collector logic outputs, a 100k resistor from this pin to a 5V supply, such as Pin 5, is required.

CONNECTION DIAGRAM & ORDERING INFORMATION (See Note Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
5-PIN TO-220 PLASTIC P - PACKAGE	SG29125P SG29125AP	-40°C to 85°C -40°C to 85°C	

Note: 1. All parts are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

SELECTION GUIDE
OTHER LINEAR CIRUITS

Device Type	Description	Typical Application	Key Features	Pkgs.
SG040	Dual Video Amplifier	• Tape drives • Low level audio stage	• Two selectable independent channels • Wide bandwidth (20MHz) and low noise (5nV/$\sqrt{Hz}$) • Input stages each with variable gain adjustment • No frequency compensation required • Internal bias supply provided to user • TTL compatible channel select • Replaces TL040 • Available in SOIC and DIP packages	J, N, D
SG103/203/303	Voltage Reference	• Power supplies • Signal conditioners • Communications	• ±10% initial tolerance (for tighter tolerance contact factory) • Bandgap design • Low dynamic impedance from 10µA to 10mA (improved over LM103) • -1mV/°C temperature coefficient • Output voltages: 1.8V, 2.0V, 2.2V, 2.4V, 2.7V, 3.0V, 3.3V, 3.6V, 3.9V, 4.3V, 4.7V, 5.1V, 5.6V • Two terminal device	Z
SG1401/2401/3401	High Frequency Video Amplifier	• IF and RF amplifiers • Symmetrical non-saturating limiters • Oscillators • Automatic Gain Control • Pulse and video amplifiication • Low-level audio stages	• 20dB voltage gain at 100MHz • 5ns rise and fall times • Fixed or variable gain • Single power supply voltage • Minimum external components • Symmetrical limiting	T, J
SG1402	Wideband Amplifier/Multiplier	• High frequency amplifiers • Modulators • Automatic gain control	• Single power supply voltage • Self-contained biasing • 25dB voltage gain • Differential or single ended inputs and outputs • Large bandwidth • Low power dissipation	T, J
SG1503/2503/3503	2.5V Precision Voltage Reference	• Power supplies • Signal conditioners • Communications	• Bandgap design • Output voltage trimmed to ±1% • Input voltage range of 4.5V to 40V • Temperature coefficient of 10ppm/°C • Output current in excess of 10mA • Interchangeable with MC1503 and AD580	Y, T, M
SG1595/1495	4 - Quadrant Multiplier	• Multipliers • Dividers • Square root functions • Phase detectors • Frequency doublers	• Excellent linearity • Adjustable scale factor • Excellent temperature stability • Wide bandwidth • High input voltage range • Wide supply voltage operation	J
SG1596/1496	Balanced Modulator/ Demodulator	• AM, SSB, DSB, FSK, and FM modulation or demodulation • Phase detection • Linear mixing and choppings	• Excellent carrier suppression • Fully balanced inputs and outputs • Low Offsets and Drift • High common mode rejection • Adjustable gain and signal handling • Useful to 100MHz	J, T, F

January 1990

SELECTION GUIDE
OTHER LINEAR CIRUITS

Device Type	Description	Typical Application	Key Features	Pkgs.
SG510A4/ SG510AR4	Read / Write Amplifier	• Center-tapped ferrite heads • Winchester Disk Drive	• Read Mode - Controlled gain to 100V/V - Low input noise - High Bandwidth > 30MHz • Write Mode - Write current range 10mA to 40mA - Programmable write current - Error flag during fault mode • Data Protection	DW, N
SG541	Read Data Processor	• Disk Drives	• Pin to pin compatible with SSI32P541 • Level qualification supports high resolution MFM and RLL encoded data retrieval • Wide bandwidth AGC input amplifier • Supports data rates up to 15 megabits/sec • Standard 12V ±10% and 5V ±10% supplies • Supports embedded servo pattern decoding • Write to read transient suppression • Fast and slow AGC attack regions for fast transient recovery	N, Q
SG3049	Dual High-Frequency Differential Amplifiers	• VHF amplifiers • VHF mixers • IF amplifiers • Balanced quadrature detectors • Sense amplifiers	• Two differential amplifiers on a common substrate • Independently accessible inputs and outputs • Full military temperature range capability	J
SG3045/3046/3821	Transistor Arrays	• High Frequency Amplifiers • Comparators • Relay drivers • Lamp drivers	• Two NPN matched transistor pairs to ±0.5mV V_{BE} • 3 uncommited matched NPN transistors • Operation from DC to 300MHz • High current gain • High voltage capabilities (3821/3045)	J, N
SG3183/3183A	Transistor Arrays	• High Frequency Amplifiers • Comparators • Relay drivers • Lamp drivers	• Five closely matched NPN transistors • 50V V_{CE} voltage (3183A) • Collector current to 100mA • Low saturation voltage	J, N

TWO CHANNEL SELECTABLE VIDEO AMPLIFIER

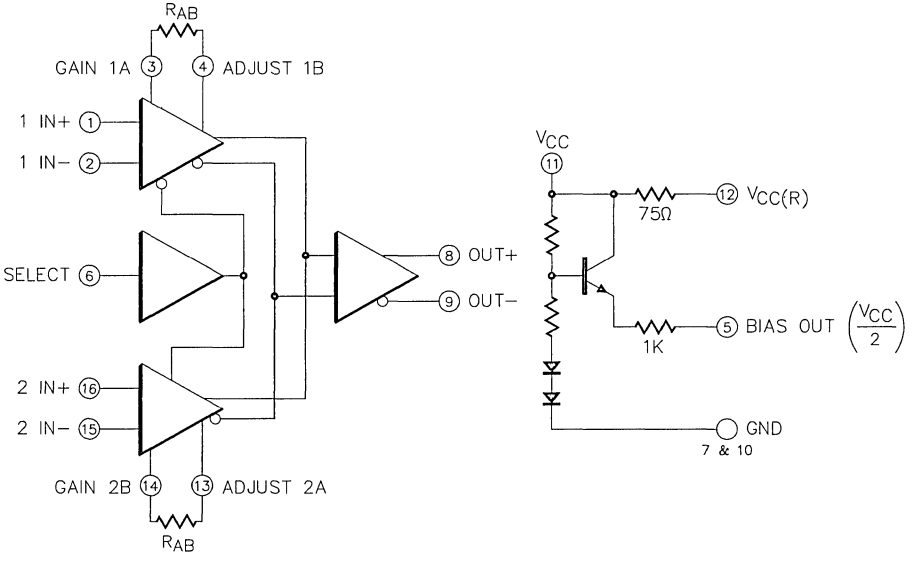
DESCRIPTION

The SG040 is a two-channel selectable video amplifier intended for use as a pre-amplifier in the read chain of streaming tape drives. It offers two selectable, wide bandwidth (20MHz), low noise (5nV/√Hz) differential input/differential output pre-stages. Each pre-stage offers variable gain adjustment through the use of an external resistor or potentiometer. Channel multiplexing occurs based on a logic "1" or "0" to the SELECT input pin. Special care has been taken to provide sufficient channel separation between the two input stages. The SG040 typically dissipates less than 150mW and offers a bias supply for the center tapped magnetic read heads. The SG040 is available in a 16-pin DIP or a 16-pin SOIC package.

FEATURES

- **Wide bandwidth (20MHz) and low noise (5nV/√Hz)**
- **Input stages each with variable gain adjustment**
- **No frequency compensation required**
- **Internal bias supply provided to user**
- **TTL compatible channel select**
- **Replaces TL040**
- **Available in SOIC and DIP packages**

BLOCK DIAGRAM



CHANNEL SELECT TABLE

SELECT	CHANNEL
0	1
1	2

10

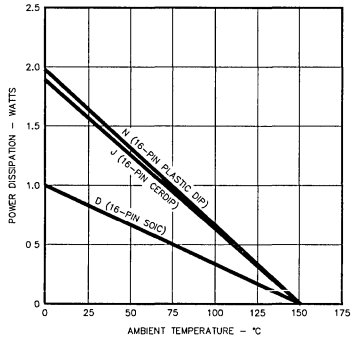
ABSOLUTE MAXIMUM RATINGS (Notes 1 & 2)

Supply Voltage (V_{CC}) 14V
Differential Input Voltage ..... ±5V
Input Voltage Range ..... -0.2V to V_{CC} +0.2V

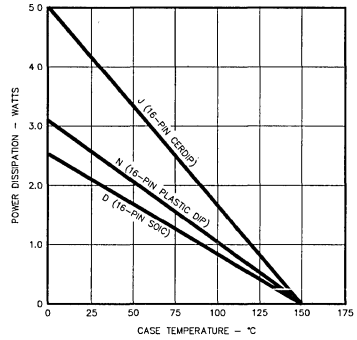
Storage Temperature ..... -65°C to 150°C
Operating Junction Temperature
Hermetic (J - Package) ..... 150°C
Plastic (D, N-Package) ..... 150°C

Note 1. Values beyond which damage may occur. Note 2. All voltages are with respect to Pin 7. All currents are positive into the specified terminal.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 3)

Supply Voltage ..... 5.0V to 13.2V
Common Mode Input Voltage ..... 5V to 7V
Differential Output Sink Current ..... ±1.5 mA

Operating Ambient Temperature Range:
SG040 ..... 0°C to 70°C

Note 3. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise stated, these specifications apply for the operating ambient temperature of T_A = 25°C and for 10.8V ≤ V_{CC} ≤ 13.2V; R_{AB} = 0Ω; R_L = 2KΩ. Pins 3 & 4 and Pins 13 & 14 are shorted together. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG040			Units
		Min.	Typ.	Max.	
Supply Current	V_{CC} = 13.2V, V_{CM} = 6V		8	12	mA
Logic 1 Input Voltage	SELECT (Pin 6)	2.0			V
Logic 0 Input Voltage	SELECT (Pin 6)			0.8	V
High Input Current	V_{SELECT} = 2.7V	-0.4			mA
Low Input Current	V_{SELECT} = 0.4V			20	μA
Bias Voltage	V_{CC} = 12V, I_{BIAS} = 100μA	5		7	V
Differential Voltage Gain	ΔV_{OUT} = 3V	300		600	V/V
Bandwidth (Note 4)	At -3dB	15	20		MHz
Propagation Delay	ΔV_{OUT} = 1V		30		ns
Rise Time	ΔV_{OUT} = 1V		25		ns
Large Signal Differential Voltage Attenuation	ΔV_{INPUT} = 50mV on unselected input	50			dB
Voltage Swing		3	5		V
Common-Mode Output Voltage	Output open	7	8	9	V
Differential Output Voltage	V_{ID} = 0V, Output open			.75	V
Input Bias Current				17	μA
Input Offset Current				3	μA
Common Mode Rejection Ratio	V_{CM} = 5V to 7V	75	100		dB
Power Supply Rejection Ratio	V_{CC} = 10.8V to 13.2V	50	80		dB
Input Noise Voltage			5		nV/√Hz
Input Resistance (Note 4)		3			KΩ
Channel Separation		50	60		dB

Note 4. These parameters, although guaranteed, are not tested in production.

CHARACTERISTIC CURVES

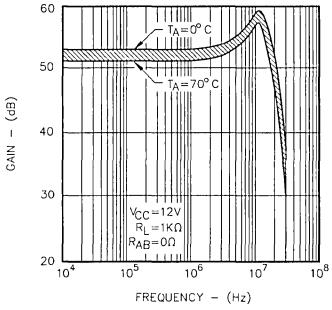


FIGURE 1.
GAIN VS. FREQUENCY AS A FUNCTION OF TEMPERATURE

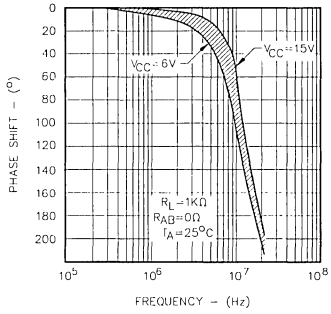


FIGURE 2.
PHASE VS. FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

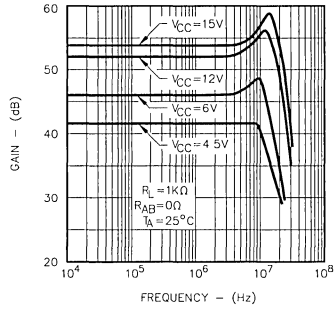


FIGURE 3.
GAIN VS. FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

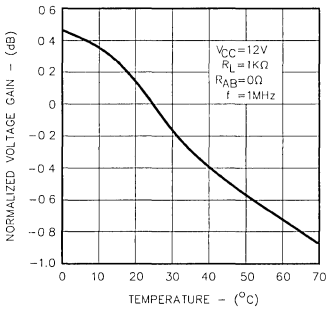


FIGURE 4.
VOLTAGE GAIN VS. TEMPERATURE

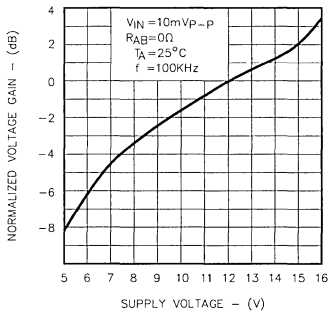


FIGURE 5.
VOLTAGE GAIN VS. SUPPLY VOLTAGE

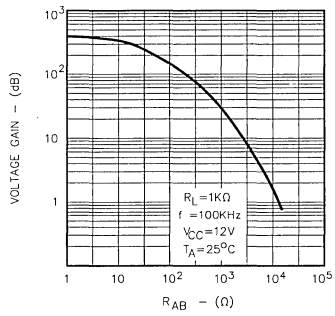


FIGURE 6.
VOLTAGE GAIN VS. R_{ADJ}

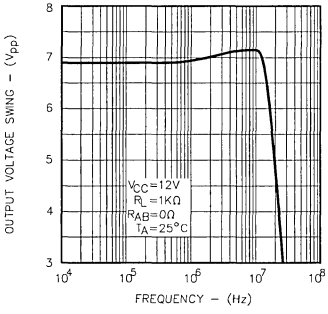


FIGURE 7.
OUTPUT VOLTAGE SWING VS. FREQUENCY

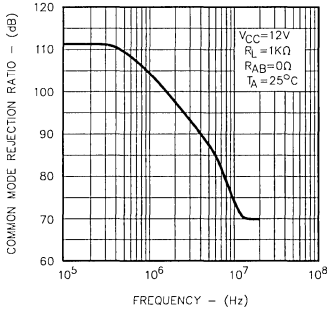


FIGURE 8.
COMMON MODE REJECTION RATIO VS. FREQUENCY

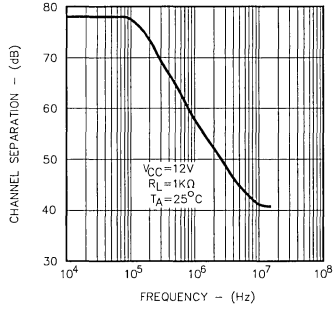


FIGURE 9.
CHANNEL SEPARATION VS. FREQUENCY

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CHARACTERISTIC CURVES (continued)

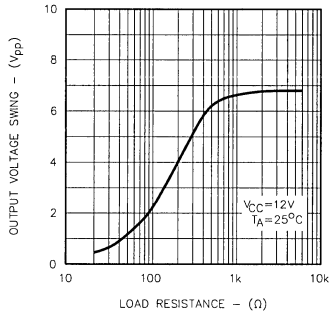


FIGURE 10.
OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE

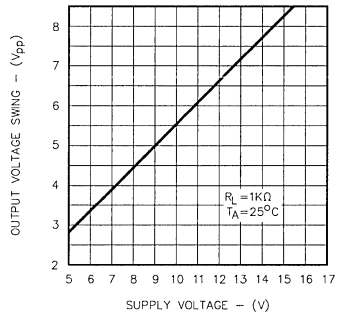


FIGURE 11.
OUTPUT VOLTAGE SWING VS. SUPPLY VOLTAGE

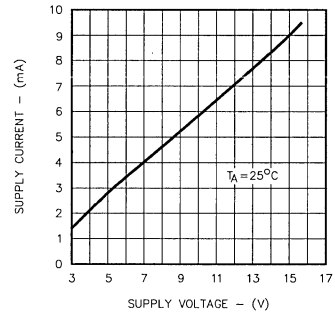
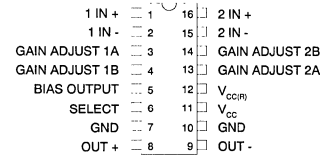
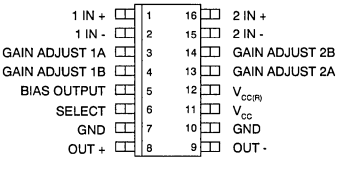


FIGURE 12.
SUPPLY CURRENT VS. SUPPLY VOLTAGE

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG040J	0°C to 70°C	
16-PIN PLASTIC DIP N - PACKAGE	SG040N	0°C to 70°C	
16-PIN NARROW BODY PLASTIC S.O.I.C. D - PACKAGE	SG040D	0°C to 70°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

DESCRIPTION

The SG103 is a two-terminal integrated circuit designed for analog and/or digital applications requiring precision voltage reference. The SG103 is an improved version of the National LM103 voltage reference. The design uses the band-gap voltage of the silicon as an internal reference for a tightly regulated output voltage. The advantages of this method over single junction zener diodes are: lower turn on drift, better temperature coefficient, sharper breakdown characteristics (line regulation) and lower dynamic impedance (load regulation). The I.C. is available in thirteen different voltages ranging from 1.8V to 5.6V (See Table 1). The SG103 is packaged in a hermetically sealed, modified TO-46 header and is specified for operation over the full military ambient temperature range of -55° C to +125° C.

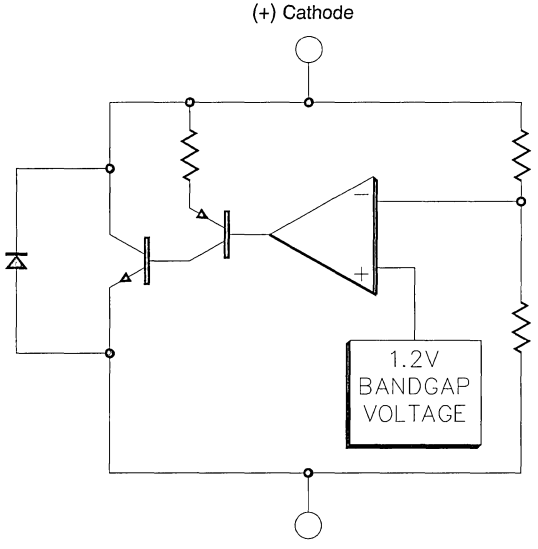
FEATURES

- **Standard voltage tolerance ±10%**
- **Precision band gap design**
- **Exceptionally sharp breakdown**
- **Low dynamic impedance from 10μA to 10mA (improved over LM103)**
- **Improved temperature coefficient**
- **Low capacitance**
- **Performance guaranteed over full military temperature range**

HIGH RELIABILITY FEATURES -SG103

- ◊ **Available to MIL-STD - 883 and DESC SMD**
- ◊ **SG level "S" processing available**

BLOCK DIAGRAM



REFERENCE VOLTAGES

TABLE 1

Measured at I_R = 1mA, Voltage Tolerance ±10%

SG103 - 1.8*
SG103 - 2.0
SG103 - 2.2
SG103 - 2.4*
SG103 - 2.7*
SG103 - 3.0
SG103 - 3.3
SG103 - 3.6
SG103 - 3.9
SG103 - 4.3
SG103 - 4.7*
SG103 - 5.1*
SG103 - 5.6

** These are the voltages that are currently available. Contact factory for product availability for additional voltages.*

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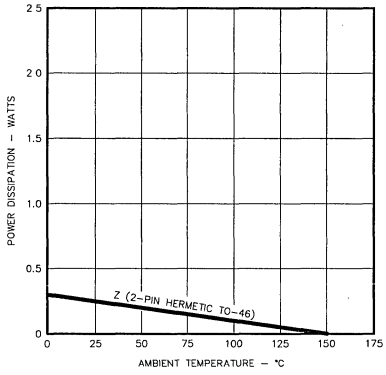
ABSOLUTE MAXIMUM RATINGS (Note 1)

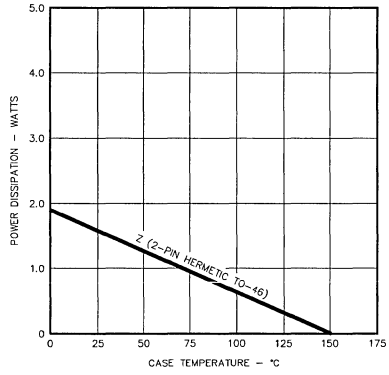
Reference Current 20mA
Forward Current 100mA
Operating Junction Temperature ..... 150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device. All voltages are with respect to ground. All currents are positive into the specified terminal.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Reference Current ..... <10mA
Forward Current ..... <30mA

Operating Ambient Temperature Range
SG103 ..... -55°C to 125°C
SG203 ..... -25°C to 85°C
SG303 ..... 0°C to 70°C

Note 2. Range over which the device is functional

ELECTRICAL SPECIFICATIONS

(These specifications apply for T_A = 25°C and 1.8V < V_Z < 5.6V unless stated otherwise. The diode should not be operated with shunt capacitances between 100 pF and 0.01 μF, unless isolated by at least a 300Ω resistor, as it may oscillate at some currents. For voltages between 4.3V and 5.6V, the maximum shunt capacitance is 50pF rather than 100pF. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG103/203/303			Units
		Min.	Typ.	Max.	
Reference Voltage Change	$10\mu A \le I_R \le 100\mu A$		60	120	mV
	$100\mu A \le I_R \le 1mA$		15	50	mV
	$1mA \le I_R \le 10mA$		50	150	mV
Reverse Dynamic Impedance (Note 3)	I_R = 3mA		5	25	Ω
	I_R = 0.3 mA		15	60	Ω
Reverse Leakage Current	$V_R = V_Z$ -0.2V		2	5	μA
Forward Voltage Drop	I_F = 10mA	0.7	0.8	1.0	V
Peak-to-Peak Broadband Noise Voltage	10 Hz ≤ f ≤ 100 kHz, I_R = 1mA		300		μV
Reference Voltage Change with Current (Note 4)	$10\mu A \le I_R \le 100\mu A$			200	mV
	$100\mu A \le I_R \le 1mA$			60	mV
	$1mA \le I_R \le 10mA$			200	mV
Reference Voltage Temperature Coefficient (Note 4)	$100\mu A \le I_R \le 1mA$		-1.0		mV/°C

Note 3. Measured with the peak-to-peak change of reverse current equal to 10% of the DC reverse current.
Note 4. These specifications apply for -55°C < T_A < +125°C.

CHARACTERISTIC CURVES

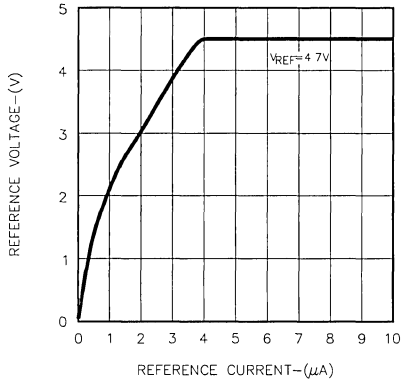


FIGURE 1.
REFERENCE VOLTAGE VS. CURRENT

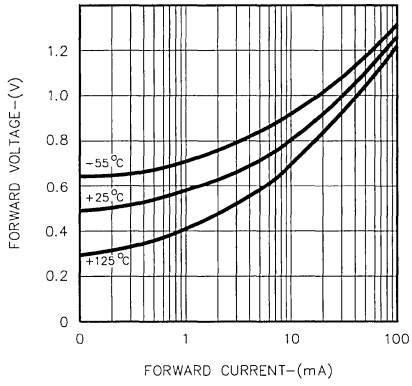


FIGURE 2.
FORWARD DIODE CHARACTERISTICS

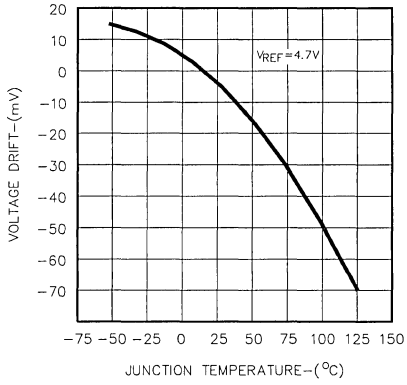


FIGURE 3.
TEMPERATURE DRIFT

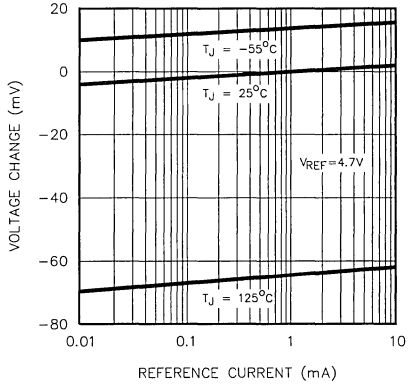


FIGURE 4.
REFERENCE VOLTAGE CHANGE VS. CURRENT

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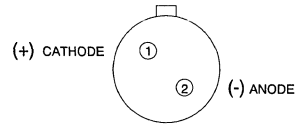
CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
2-PIN TO-46 METAL CAN Z - PACKAGE	SG103-x.xZ/883B SG103-x.xZ SG203-x.xZ SG303-x.xZ x.x = See first page of data sheet for reference voltages available.	-55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

4 CHANNEL READ/WRITE AMPLIFIER

DESCRIPTION

The SG510A4/SG510AR4 is a bipolar monolithic integrated circuit intended for use with center-tapped ferrite heads commonly used in Winchester disk drives. It is a 4 channel device which includes circuitry to accurately read and write data to the heads in addition to providing data protection. The SG510AR4 includes a 750Ω damping resistor between the x-y head connections.

The SG510A4/SG510AR4 operates from +5V and +12V supplies and is available in both 22-pin plastic DIP package and the 24-pin wide body plastic SOIC package.

FEATURES

- **Read Mode**
  - **Controlled gain to 100V/V**
  - **Low input noise < 1.5nV$\sqrt{Hz}$**
  - **High bandwidth > 30MHz**
- **Write Mode**
  - **Write current range 10-40mA**
  - **Programmable write current**
  - **Error flag during fault mode**
- **Available in 24-pin SOIC and 22-pin plastic DIP packages**

BLOCK DIAGRAM (Pin numbers represent the 24-pin DIP package.)

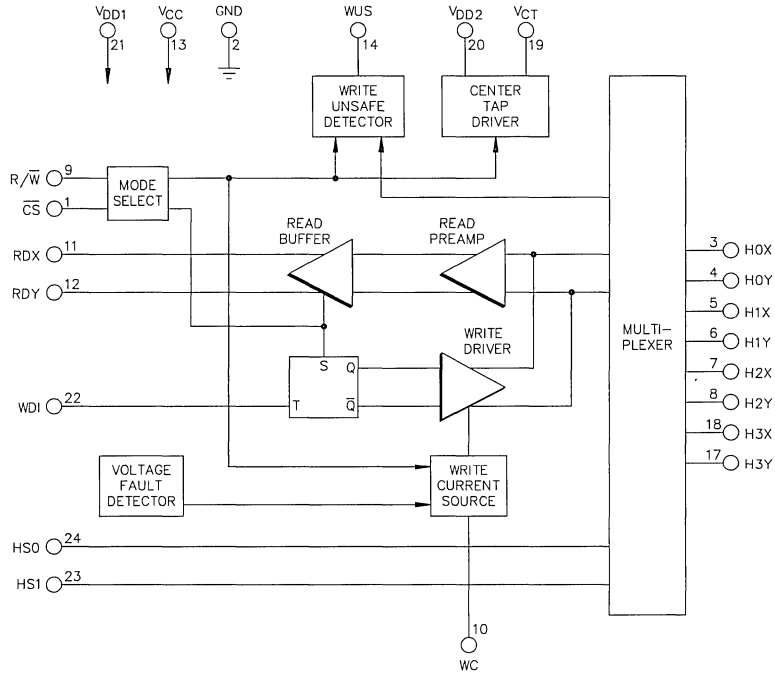


TABLE 1 - MODE SELECT

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	x	Idle

TABLE 2 - HEAD SELECT

$\overline{HS1}$	$\overline{HS0}$	HEAD
0	0	0
0	1	1
1	0	2
1	1	3

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April 1990

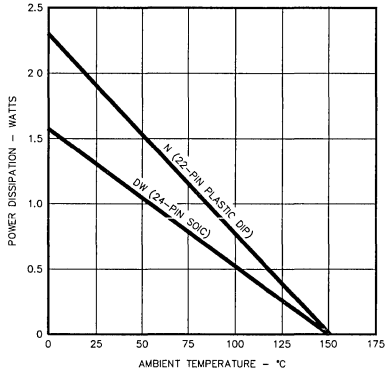
ABSOLUTE MAXIMUM RATINGS (Note 1)

DC Supply Voltage (V_{DD1}) ..... -0.3V to 14V
DC Supply Voltage (V_{DD2}) ..... -0.3V to 14V
DC Supply Voltage (V_{CC}) ..... -0.3V to 6V
Digital Input Voltage Range (V_{IN}) ..... -0.3V to (V_{CC} + 0.3V)
Head Port Voltage Range (V_H) ..... -0.3V to (V_{DD} + 0.3V)
WUS Pin Voltage Range (V_{WUS}) ..... -0.3V to 14V
Write Current (Zero Peak) (I_W) 60mA

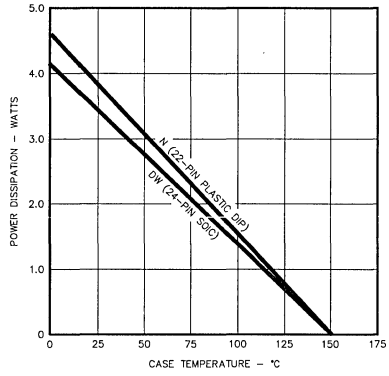
RDX, RDY Output Current (I_O) ..... -10mA
V_{CT} Output Current (I_{VCT}) ..... -60mA
WUS Output Current (I_{WUS}) 12mA
Operating Junction Temperature
Plastic (N, DW Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Values beyond which damage may occur. All voltage referenced to GND. Currents into device are positive.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

DC Supply Voltage (V_{DD1}) ..... 10.8V to 13.2V
DC Supply Voltage (V_{CC}) ..... 4.5V to 5.5V
Head Inductance (L_H) ..... 5µH to 15µH
Damping Resistor (R_D) (SG510A4 only) ..... 500Ω to 2KΩ

R_{CT} Resistor (R_{CT}) (Note 3) ..... 124Ω to 136Ω
Write Current (I_W) ..... 10mA to 40mA
Operating Ambient Temperature Range
SG510A4/SG510AR4 ..... 25°C to 70°C

Note 2. Range over which the device is functional.
Note 3. For I_W = 40mA. At other I_W levels refer to Applications Information that follows this specification.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG510A4/SG510AR4 with 25°C ≤ T_A ≤ 70°C and over recommended operating conditions. Low duty cycle testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG510A4 SG510AR4			Units
		Min.	Typ.	Max.	
Power Supply					
Supply Current (V_{CC})	Read/Idle Mode			35	mA
	Write Mode			30	mA
Supply Current (V_{DD}) = (V_{DD1} + V_{DD2})	Idle Mode			20	mA
	Read Mode			35	mA
Power Dissipation	Write Mode			20+I_W	mA
	Idle Mode, T_J = 125°C			400	mW
	Read Mode, T_J = 125°C			600	mW
	Write Mode, I_W = 40mA, R_{CT} = 0Ω, T_J = 125°C			800	mW
	Write Mode, I_W = 40mA, R_{CT} = 130Ω, T_J = 125°C			600	mW

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG510A4 SG510AR4 Min.	Typ.	Max.	Units
Digital Inputs (HSn, $\overline{CS}$, R/$\overline{W}$)					
Input Low Voltage				0.8	V
Input High Voltage		2.0			V
Input Low Current	V_{IL} = 0.8V	-0.4			mA
Input High Current	V_{IL} = 2.0V			100	µA
Digital Output (WUS)					
Output Low Voltage	I_{OL} = 8mA			0.5	V
Output Leakage	V_{OH} = 5V			100	µA
Write Mode					
Center Tap Voltage (V_{CT})	Write Mode		6.0		V
Head Current (per side)	Write Mode, 0V ≤ V_{CC} ≤ 3.7V, 0V ≤ V_{DD1} ≤ 8.7V	-200		200	µA
Write Current Range		10		40	mA
Write Current Constant "K"		2.375		2.625	
I_{WC} to Head Leakage Current			0.99		mA/mA
Unselected Head Leakage Current				85	µA
RDX, RDY Output Offset Voltage	Write/Idle Mode	-20		20	mV
RDX, RDY Common Mode Output Voltage	Write/Idle Mode		5.3		V
RDX, RDY Leakage	RDX = RDY = 6V, Write/Idle Mode	-100		100	µA
Read Mode					
Center Tap Voltage	Read Mode		4.0		V
Head Current (per side)	Read or Idle Mode, 0V ≤ V_{CC} ≤ 5.5V, 0V ≤ V_{DD1} ≤ 13.2V	-200		200	µA
Input Bias Current (per side)				45	µA
Input Offset Voltage	Read Mode	-440		440	mV
Common Mode Output Voltage	Read Mode	4.5		6.5	V

DYNAMIC SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG510A4/SG510AR4 with 25°C ≤ T_A ≤ 70°C, I_W = 35mA, L_H = 10µH, R_D = 750Ω, f(WDI) = 5MHz, C_L (RDX, RDY) ≤ 20pF, and over recommended operating conditions.

Parameter	Test Conditions	SG510A4 SG510AR4 Min.	Typ.	Max.	Units
Write Mode					
Differential Head Voltage Swing		7.0			V(pk)
Unselected Head Transient Current (Note 4)				2	mA(pk)
Differential Output Capacitance (Note 4)				15	pF
Differential Output Resistance	SG510A4	10K			Ω
	SG510AR4	600		960	Ω
WDI Transition Frequency	WUS = low	250			KHz
Read Mode					
Differential Voltage Gain	V_{IN} = 1mVpp @ 300KHz, R_L (RDX)= R_L (RDY)= 1KΩ	85		115	V/V
Dynamic Range	DC Input Voltage, V_I, Where Gain Falls by 10%, V_{IN} = V_I + 0.5mVpp @ 300KHz	-3		3	mV
Bandwidth (-3dB) (Note 4)	|Zs| < 5Ω, V_{IN} = 1mVpp	30			MHz
Input Noise Voltage (Note 4)	BW = 15MHz, L_H = 0, R_H = 0			1.5	nV/√Hz
Differential Input Capacitance (Note 4)	f = 5MHz			20	pF
Differential Input Resistance	SG510A4, f = 5MHz	2K			Ω
	SG510AR4, f = 5MHz	460		860	Ω
Common Mode Rejection Ratio	V_{CM} = V_{CT} + 100mVpp @ 5MHz	50			dB
Power Supply Rejection Ratio	100mVpp @ 5MHz on V_{DD1}, V_{DD2} or V_{CC}	45			dB
Channel Separation	Unselected Channel: V_{IN} = 100mVpp @5MHz, Selected Channel: V_{IN} = 0mVpp	45			dB
Single Ended Output Resistance (Note 4)	f = 5MHz			30	Ω
Output Current	AC Coupled Load, RDX to RDY	2.1			mA

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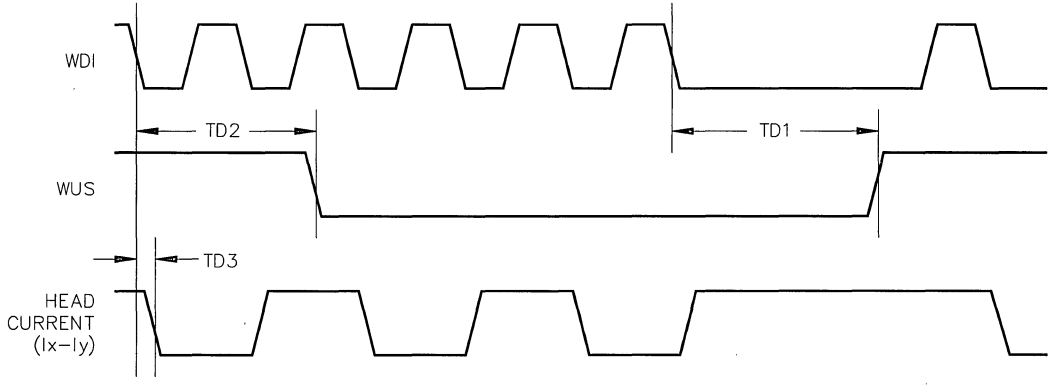
DYNAMIC SPECIFICATIONS (continued)

Parameter	Test Conditions	SG510A4 SG510AR4 Min.	Typ.	Max.	Units
Switching Characteristics					
R / $\overline{W}$ to Write	Delay to 90% of write current			1.0	µs
R / $\overline{W}$ to Read	Delay to 90% of 100mV, 10MHz read signal envelope or to 90% of write current			1.0	µs
$\overline{CS}$ to Select	Delay to 90% of write current or to 90% of 100mV, 10MHz read signal envelope			1.0	µs
CS to Unselect	Delay to 90% decay of write current			1.0	µs
HS0 - HS2 to any head	Delay to 90% of 100mV, 10MHz read signal envelope			1.0	µs
WUS, Safe to Unsafe - TD1	I_W = 35mA	1.6		8.0	µs
WUS, Unsafe to Safe - TD2	I_W = 35mA			1.0	µs
Head Current	L_H = 0µH, R_H = 0Ω				
Prop. Delay - TD3	From 50% points			25	ns
Asymmetry	WDI has 50% duty cycle and 1ns rise/fall time			2	ns
Rise / Fall Time	10% - 90% points			20	ns

Note 4. These parameters, although guaranteed over the recommended operating conditions, are not tested in production.

WRITE MODE TIMING DIAGRAM - FIGURE 1



CIRCUIT OPERATION

The SG510A4/SG510AR4 has the ability to address up to 4 center-tapped ferrite heads and provide write drive or read amplification. Head selection and mode control are accomplished using the HSn, $\overline{CS}$ and R/$\overline{W}$ inputs as shown in tables 1 & 2 on first page. Internal pull-ups are provided for the $\overline{CS}$ & R/$\overline{W}$ inputs to force the device into a non-writing condition if either control line is opened accidentally.

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the SG510A4/SG510AR4 as a current switch and activates the Write Unsafe (WUS) detector circuitry. Write current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Note that preceding read mode selection initializes the Write Data Flip-Flop, WDFF, to pass write current through the "X" side of the head. The zero-peak write current magnitude is programmed by an external resistor R_{WC} from pin WC to GND and is given by:

$$I_W = K/R_{WC}, \text{ where K = Write Current Constant}$$

The Write Unsafe detection circuitry monitors voltage transitions at the selected head connections and flags any of the following conditions as a high level on the Write Unsafe open collector output:

- Head open
- WDI frequency too low
- Device not selected
- Head center tap open
- Device in read mode
- No write current

Two negative transitions on WDI, after the fault is corrected, will clear the WUS flag.

CIRCUIT OPERATION (continued)

To further assure data security a voltage fault detection circuit prevents application of write current during power loss or power sequencing.

To enhance write to read recovery time the change in RDX, RDY common mode voltage is minimized by biasing these outputs to a level within the read mode range when in write mode.

Power dissipation in write mode may be reduced by placing a resistor (R_{CT}) between V_{DD1} and V_{DD2}. The optimum resistor value is 150Ω x 40 / I_W (I_W in mA). At low write currents (<15mA) read mode dissipation is higher than write mode and R_{CT}, though recommended, may not be considered necessary. In this case V_{DD2} is connected directly to V_{DD1}.

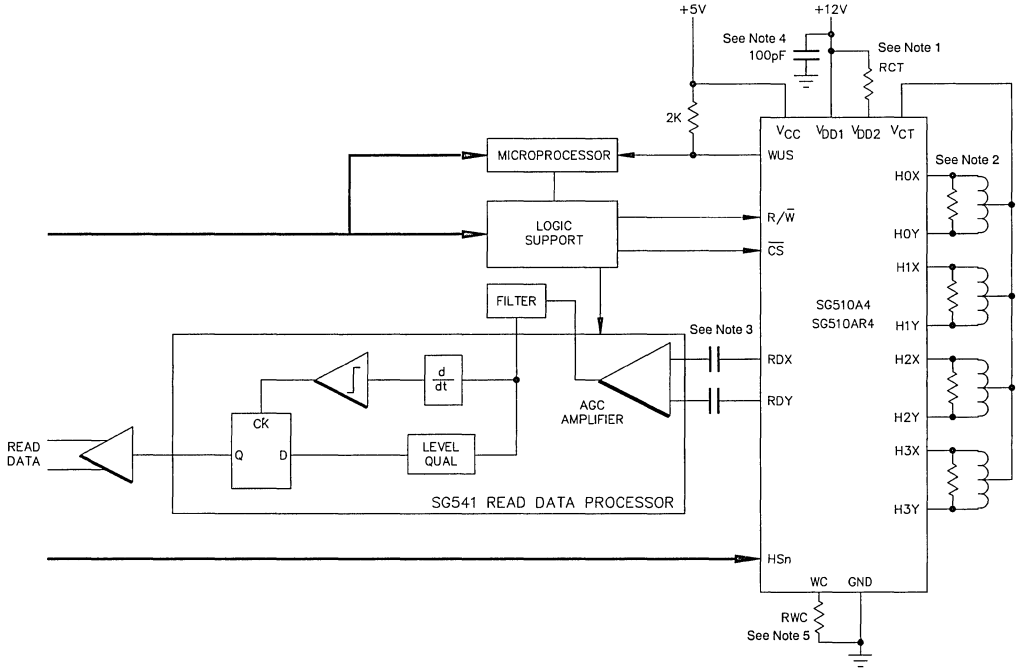
READ MODE

Taking $\overline{CS}$ low and R/$\overline{W}$ high selects read mode which configures the SG510A4/SG510AR4 as a low noise differential amplifier for the selected head. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head paths. These outputs should be AC coupled to the load. The internal write current source is gated off in read mode eliminating the need for any external gating.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX, RDY outputs into a high impedance state and deactivates the internal write current source. This facilitates multi-device installations by allowing the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

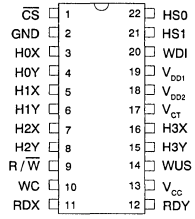
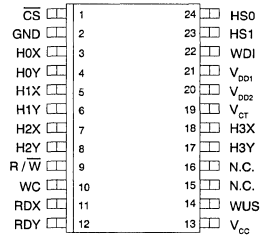
APPLICATION INFORMATION



NOTES:

1. An external resistor, R_{CT}, given by; $R_{CT} = 130\ (40/I_W)$ where I_W is the zero-peak write current in mA, can be used to limit internal power dissipation. Otherwise connect V_{DD2} to V_{DD1}.
2. Damping resistors not required on SG510AR4 versions.
3. Limit DC current from RDX and RDY to 100μA and load capacitance to 20pF. In multi-chip application these outputs can be wire-OR'ed.
4. The power bypassing capacitor must be located close to the device with its ground returned directly to device ground, with as short a path as possible.
5. To reduce ringing due to stray capacitance this resistor should be located close to the D.U.T. Where this is not desirable a series resistor can be used to buffer a long WC line. In multi-chip applications a single resistor common to all chips may be used.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
22-PIN PLASTIC DIP N - PACKAGE	SG510A4 SG510AR4	25°C to 70°C 25°C to 70°C	
24-PIN PLASTIC S.O.I.C. DW - PACKAGE	SG510A4 SG510AR4	25°C to 70°C 25°C to 70°C	

Notes: 1. All parts are viewed from the top.

READ DATA PROCESSOR

DESCRIPTION

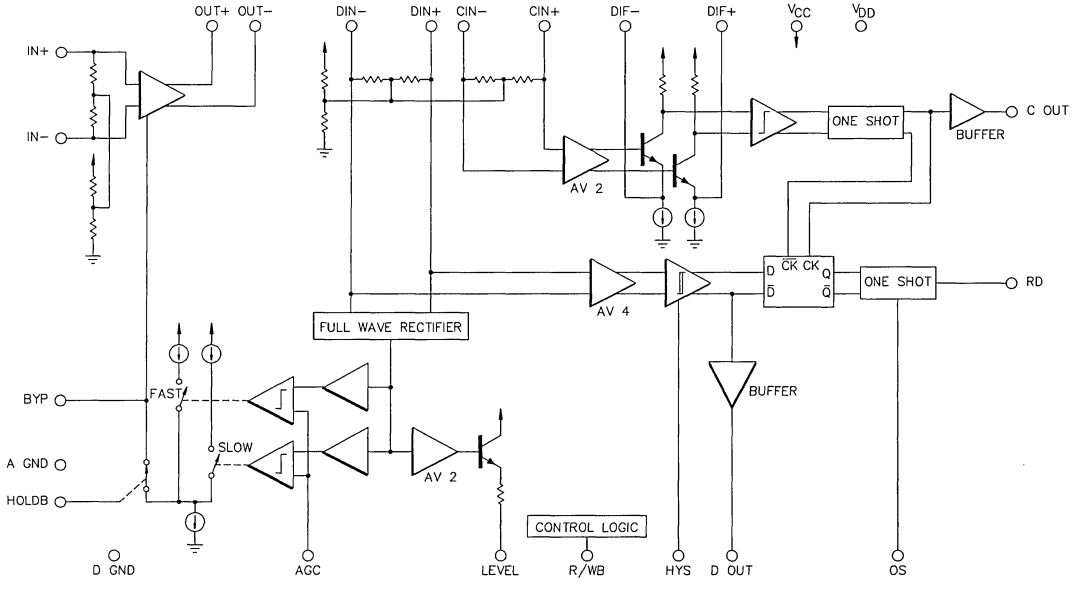
The SG541 is a bipolar integrated circuit designed specifically for detection and qualification of MFM and RLL encoded read signals used in disk drive applications. This device consists of read and write channels and will handle data rates of up to 15 Megabits/sec. In read mode, the SG541 provides amplification and qualification of head pre-amplifier outputs. Pulse qualification is accomplished using level qualification of differentiated input zero crossings. An AGC amplifier is used to compensate for variations in head preamp output levels, presenting a constant input level to the pulse qualification circuitry. The AGC loop can be disabled so that a constant gain can be used for embedded servo decoding or other processing needs. In write mode the circuitry is disabled and the AGC gain stage input impedance switched to a lower level to allow fast setting of the input coupling capacitors during a write to read transition.

The SG541 requires +5V and +12V power supplies and is available in a 24 pin DIP and 28 pin PLCC.

FEATURES

Pin to pin compatible with SSI32P541
Level qualification supports high resolution MFM and RLL encoded data retrieval
Wide bandwidth AGC input amplifier
Supports data rates up to 15 megabits/sec
Standard 12V ±10% and 5V ±10% supplies
Supports embedded servo pattern decoding
Write to read transient suppression
Fast and slow AGC attack regions for fast transient recovery

BLOCK DIAGRAM



TRUTH TABLE

R/WB	HOLDB	Mode
1	1	READ - Read amp on, AGC active, Digital section active.
1	0	HOLD - Read amp on, AGC gain held constant Digital section active.
O	X	WRITE - AGC gain switched to maximum, Digital section inactive, common mode input resistance reduced.

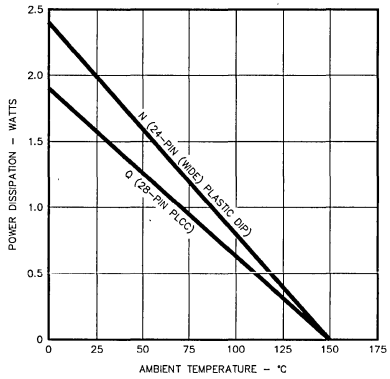
ABSOLUTE MAXIMUM RATINGS (Note 1)

5V Supply Voltage, V_{CC} 6V
12V Supply Voltage, V_{DD} 14V
R/W, IN+, IN-, HOLD ..... -0.3V to (V_{CC}+ 0.3V)
RD ..... -0.3V to (V_{CC} + 0.3V) or + 12mA
All others ..... -0.3 to (V_{DD}+ 0.3V)

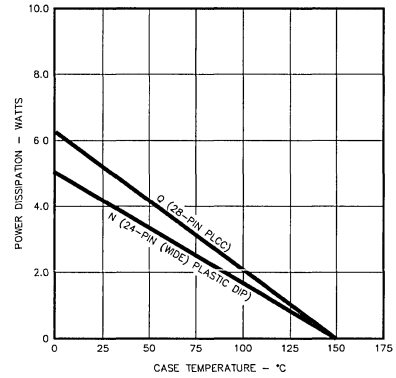
Operating Junction Temperature
Plastic (N, Q Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1. Values beyond which damage may occur.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

5V Supply Voltage ..... 4.5V to 5.5V
12V Supply Voltage ..... 10.8V to 13.2V

Operating Ambient Temperature Range
SG541 ..... 0°C to 70°C

Note 2: Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified , these specifications apply over the operating ambient temperatures for SG 540 with 0°C ≤ T_A ≤ 70°C and 4.5V ≤ V_{CC} ≤ 5.5V, 10.8V ≤ V_{DD} ≤ 13.2V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG541 Min.	SG541 Typ.	SG541 Max.	Units
Power Supply					
Supply Current (I_{CC})	Outputs unloaded			14	mA
Supply Current (I_{DD})	Outputs unloaded			70	mA
Power Dissipation	Outputs unloaded, T_J = 70°C			730	mW
Logic Signals					
Input Low Voltage		-0.3		0.8	V
Input High Voltage		2.0			V
Input Low Current	V_{IL} = 0.4V	0.0		-0.4	mA
Input High Current	V_{IH} = 2.4V			100	µA
Output Low Voltage	I_{OL} = 4.0mA			0.4	V
Output High Voltage	I_{OH} = -400µA	2.4			V
Mode Control					
Read to Write Transition Time				1.0	µs
Write to Read Transition Time	AGC settling not included, transition to high input resistance	1.2		3.0	µs
Read to Hold Transition Time				1.0	µs
Write Mode					
Common Mode Input Impedance (both sides)	R/WB pin = low		250		Ω

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG541 Min.	SG541 Typ.	SG541 Max.	Units
Read Mode (Note 3)					
Differential Input Resistance	V[(IN+) - (IN-)] = 100mVpp @ 2.5MHz		5K		Ω
Differential Input Capacitance	V[(IN+) - (IN-)] = 100mVpp @ 2.5MHz			10	pF
Common Mode Input Impedance	R/WB pin high		1.8		KΩ
(both sides)	R/WB pin low		0.25		KΩ
Gain Range	1.0Vpp ≤ V[(OUT+) - (OUT-)] ≤ 2.5Vpp	4.0		83	V/V
Input Noise Voltage	Gain set to maximum			30	nV/√Hz
Bandwidth	Gain set to maximum -3dB point	30			MHz
Maximum Output Voltage Swing	Set by AC pin voltage	3.0			Vpp
OUT+ to OUT- Pin Current	No DC path to GND	±3.2			mA
Output Resistance		13		32	Ω
Output Capacitance				15	pF
[(DIN+) - (DIN-)] Input Voltage	30mVpp ≤ V[(IN+) - (IN-)] ≤ 550mVpp,				
Swing vs. AGC Input Level	0.5Vpp ≤ V[(DIN+) - (DIN-)] ≤ 1.5Vpp	0.37		0.56	Vpp/V
[(DIN+) - (DIN-)] Input Voltage	30mVpp ≤ V[(IN+) - (IN-)] ≤ 550mVpp, AGC Fixed,				
Swing Variation	over supply and temperature			8	%
Gain Decay Time (T_D)	V_{IN} = 300mVpp to 150mVpp at 2.5MHz,				
	V_{OUT} to 90% of final value. Fig. 1a		50		µs
Gain Attack Time (T_A)	From Write to Read transition to V_{OUT} at 110% of final value.				
	V_{IN} = 400mVpp @ 2.5MHz. Fig. 1b		4		µs
Fast AGC Capacitor Charge Current	V[(DIN+) - (DIN-)] = 1.6V, V(AGC) = 3.0V	1.3		2.0	mA
Slow AGC Capacitor Charge Current	V[(DIN+) - (DIN-)] = 1.6V, Vary V(AGC) until slow discharge	0.14		0.22	mA
Fast to Slow Attack Switchover Point	{V[(DIN+) - (DIN-)]} ÷ {V[(DIN+) - (DIN-)] final}		1.25		
AGC Capacitor Discharge Current	V[(DIN+) - (DIN-)] = 0.0V				
	Read Mode		4.5		µA
	Hold Mode	-0.2		0.2	µA
CMRR (Input Referred)	V(IN+) = V(IN-) = 100mVpp @ 5MHz, gain at max.	40			dB
PSRR (Input Referred)	V_{CC} or V_{DD} = 100mVpp @ 5MHz, gain at max.	30			dB
Hysteresis Comparator					
Input Signal Range				1.5	Vpp
Differential Input Resistance	V[(DIN+) - (DIN-)] = 100mVpp @ 2.5MHz	5		11	KΩ
Differential Input Capacitance	V[(DIN+) - (DIN-)] = 100mVpp @ 2.5MHz			6.0	pF
Common Mode Input Impedance	(both sides)		2.0		KΩ
Comparator Offset Voltage	HYS pin at GND, Resistance across DIN+ and DIN- ≤ 1.5KΩ			10	mV
Peak Hysteresis Voltage vs.					
HYS Pin Voltage (input referred)	At DIN+, DIN- pins, 1V < V(HYS) < 3V	0.16		0.25	V/V
HYS Pin Input Current	1V < V(HYS) < 3V	0.0		-20	µA
Level Pin Output Voltage					
vs. V[(DIN+) - (DIN-)]	0.6 < |V[(DIN+)-(DIN-)]| < 1.3Vpp, 10KΩ from LEVEL pin to GND	1.5		2.5	V/Vpp
LEVEL Pin Max Output Current		3.0			mA
LEVEL Pin Output Resistance	I(LEVEL) = 0.5mA		180		Ω
DOUT Pin Output Low Voltage	0.0 ≤ I_{OL} ≤ 0.5mA	V_{DD}-4.0		V_{DD}-2.8	V
DOUT Pin Output High Voltage	0.0 ≤ I_{OH} ≤ 0.5mA	V_{DD}-2.5		V_{DD}-1.8	V

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG541 Min.	SG541 Typ.	SG541 Max.	Units
Active Differentiator					
Input Signal Range				1.5	Vpp
Differential Input Resistance	V[(CIN+) - (CIN-)] = 100mVpp @ 2.5MHz	5.8		11.0	KΩ
Differential Input Capacitance	V[(CIN+) - (CIN-)] = 100mVpp @ 2.5MHz			6.0	pF
Common Mode Input Impedance	(both sides)		2.0		KΩ
Voltage Gain from CIN± to DIF±	R(DIF+ to DIF-) = 2KΩ	1.7		2.2	V/V
DIF+ to DIF- Pin Current	Differentiator Impedance must be set as not to clip signals at this current level.	±1.3			mA
Comparator Offset Voltage	DIF+, DIF- = AC Coupled			10.0	mV
COUT Pin Output Low Voltage	$0.0 \le I_{OH} \le 0.5mA$		V_{DD}-3.0		V
COUT Pin Output Pulse Voltage V(high) - V(low)	$0.0 \le I_{OH} \le 0.5mA$		0.4		V
COUT Pin Output Pulse Width	$0.0 \le I_{OH} \le 0.5mA$		30		ns
Output Data Characteristics (Note 4)					
D-Flip-Flop Set Up Time (Td1)	Min. delay from V(DIN+, DIN-) exceeding threshold to V[(DIF+) - (DIF-)] reaching a peak	0			ns
Propagation Delay (Td3)				110	ns
Output Data Pulse Width Variation	Td5 = 670 C_{OS}, 50pF ≤ C_{OS} ≤ 200pF			±15	%
Logic Skew Td3 - Td4				3	ns
Output Rise Time	V_{OH} = 2.4V			14	ns
Output Fall Time	V_{OL} = 0.4V			18	ns

Note 3. AGC Amplifier - Unless otherwise specified, IN+ and IN- are AC coupled, OUT+ and OUT- are loaded differentially with > 600Ω and each side is loaded with < 10pF to GND, a 2000pF capacitor is connected beween BYP and GND, OUT+ is AC coupled to DIN+, OUT- is AC coupled to DIN-, AGC pin voltage is 2.2 VDC.

Note 4. (Ref. Fig. 2) - Unless otherwise specified V[(CIN+) - (CIN-)] = V[(DIN+) - (DIN-)] = 1.0Vpp AC coupled sine wave at 2.5MHz differentiating network between DIF+ and DIF- is 100Ω in series with 65pF, V(HYS) = 1.8DC, a 60pF capacitor is connected between OS and V_{CC}, RD- is loaded with a 4KΩ resistor to V_{CC} and a 10pF capacitor to GND.

PIN DESCRIPTION

Pin Name	Description
V_{CC}	5 volt power supply
V_{DD}	12 volt power supply
AGND, DGND	Analog and Digital ground pins
R/WB	TTL compatible read/write control pin
IN+, IN-	Analog signal input pins
OUT+, OUT-	AGC Amplifier output pins
BYP	The AGC timing capacitor is tied between this pin and AGND
HOLDB	TTL compatible pin that holds the AGC gain when pulled low
AGC	Reference input voltage level for the AGC circuit
DIN+, DIN-	Analog input to the hysteresis comparator

Pin Name	Description
HYS	Hysteresis level setting input to the hysteresis comparator
LEVEL	Provides rectified signal level for input to the hysteresis comparator
DOUT	Buffered test point for monitoring the flip-flop D input
CIN+, CIN-	Analog input to the differentiator
DIF+, DIF-	Pins for external differentiating network
COUT	Buffered test point for monitoring the clock input to the flip-flop
OS	Connection for read output pulse width setting capacitor
RD	TTL compatible read output

TIMING DIAGRAMS

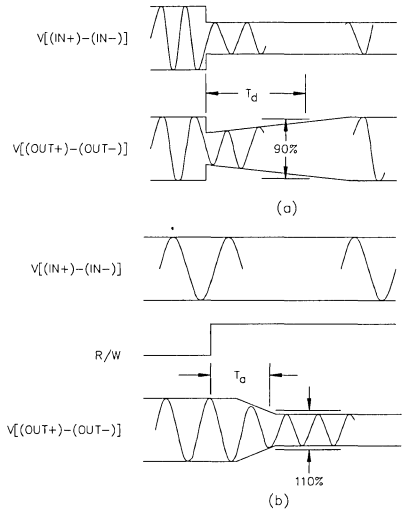


FIGURE 1 - AGC TIMING DIAGRAMS

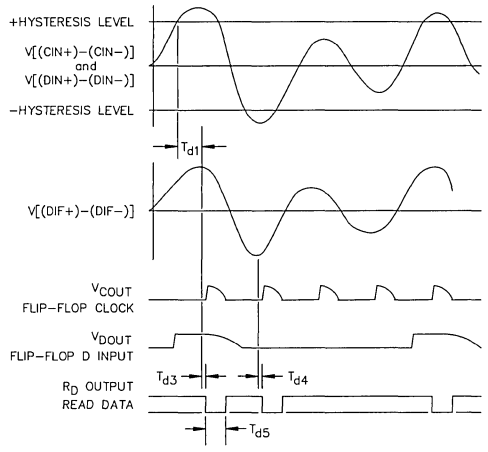


FIGURE 2 - TIMING DIAGRAM

TYPICAL APPLICATION

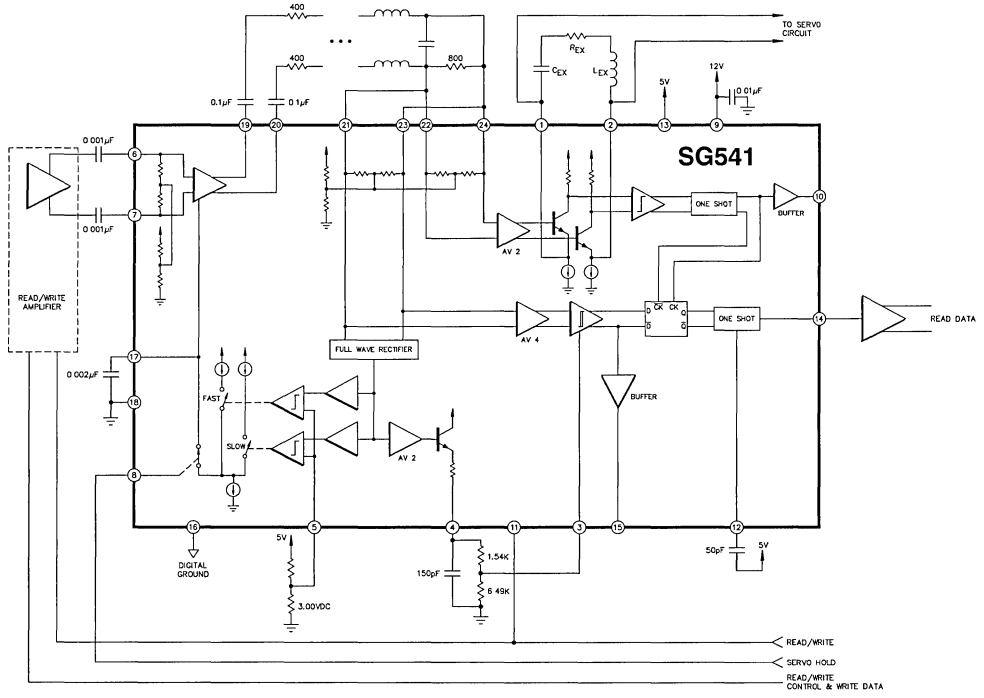


FIGURE 3 - TYPICAL READ/WRITE CIRCUIT USING SG541

NOTE: Circuit traces for the 12V bypass capacitor and the AGC hold capacitor should be as short as possible with both capacitors returned to the Analog Ground pin.

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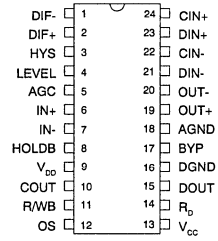
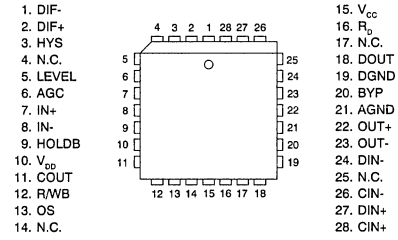
CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
24-PIN PLASTIC DIP (WIDE) N - PACKAGE	SG541N	0°C to 70°C	
28-PIN PLASTIC LEADED CHIP CARRIER (PLCC) Q - PACKAGE	SG541Q	0°C to 70°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

SG1401/SG2401/SG3401

HIGH FREQUENCY VIDEO AMPLIFIER

DESCRIPTION

A monolithic integrated voltage amplifier useful over a frequency range from DC to 200 MHz. Internal emitter followers are used to achieve high input and low output impedances, allowing simple capacitor coupling. Biasing and gain-setting resistors are internally diffused, eliminating external resistor networks. The gain may be externally varied through the use of AGC diodes which are included in the circuit.

The SG1401 will operate over the full military ambient temperature range of -55°C to 125°C while the SG2401 and SG3401 are designed for 0°C to 70°C applications.

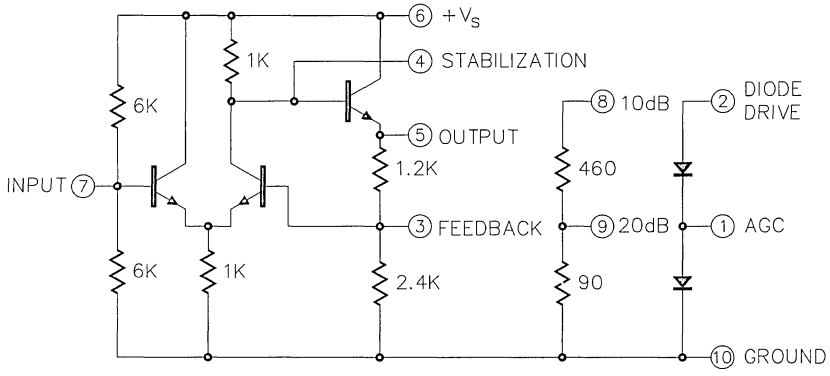
FEATURES

- **20dB voltage gain at 100MHz**
- **5ns rise and fall times**
- **Fixed or variable gain**
- **Single power supply voltage**
- **Minimum external components**
- **Symmetrical limiting**

HIGH RELIABILITY FEATURES -SG1401

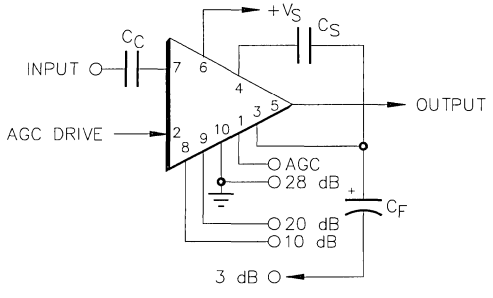
- ◊ **Available to MIL-STD-883**
- ◊ **SG level "S" processing available**

SCHEMATIC DIAGRAM



(Pin numbers correspond to T-package)

BLOCK DIAGRAM



(Pin numbers correspond to T-package)

$C_F = \frac{1}{2\pi f_C R}$ where f_C is Low Frequency corner and R is the Gain setting.

C_S = 0 to 10pF to minimize high frequency peaking.

10

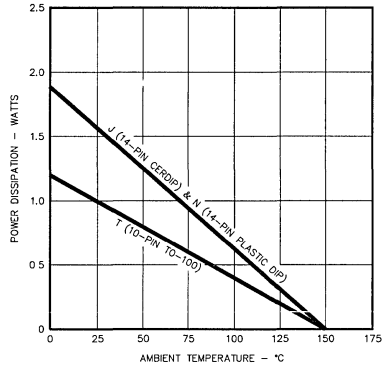
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage 20V
AGC Diode Current 5mA
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

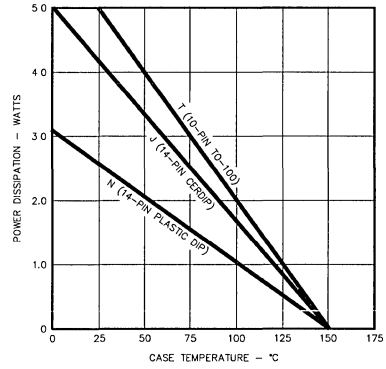
Operating Junction Temperature
Hermetic (J, T-Packages) ..... 150°C
Plastic (N-Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage ..... 8V to 18V

Operation Ambient Temperature Range
SG1401 ..... -55°C to 125°C
SG2401/SG3401 ..... 0°C to 70°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply for the operating ambient temperatures of T_A = 25°C, V_S = +12V, and f = 1MHz. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1401/SG2401			SG3401			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Voltage		6	12	20	6	12	20	V
Power Consumption	No AGC Voltage		90	110		90	120	mW
DC Output Voltage			8.7			8.7		V
Peak-to-Peak Output	Pin 3(4) to AC Ground (Note 3)		4			3		V
Voltage Gain	Pin 3(4) open (Note 3)	2.2	2.7	3.2	2.2	2.7	3.2	dB
	Pin 3(4) coupled to pin 8(11) (Note 3)	9	10	11	9	10	11	dB
	Pin 3(4) coupled to pin 9(12) (Note 3)	18	20	21	18	20	21	dB
	Pin 3(4) to AC Ground (Note 3)	26	28	31	24	26	31	dB
Unity Gain Frequency	Pin 3(4) to AC Ground (Note 3)		200			200		MHz
Input Resistance	20dB Gain		2.5			2.5		KΩ
Output Resistance	20dB Gain		25			50		Ω
Input Capacitance	20dB Gain		5			5		pF
Maximum Power Gain	20dB Gain, R_L = 50Ω		30			30		dB
Temperature Stability (Note 4)	20dB Gain, $T_A = T_{MIN}$ to T_{MAX}		±0.5	±1		±1	±2	dB
AGC Range	20dB Gain, R_S = 1K	20	22			22		dB
Noise Figure			6	8		6		dB

Note 3. Numbers in parenthesis refer to dual-in-line package.
Note 4. These parameters, although guaranteed, are not tested in production.

CHARACTERISTIC CURVES (Pin Numbers correspond to T - Package)

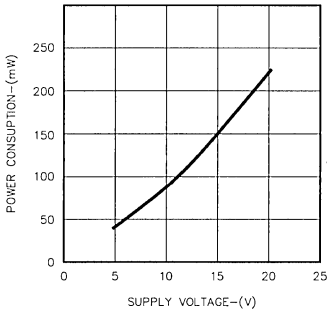


FIGURE 1.
POWER CONSUMPTION VS. SUPPLY VOLTAGE

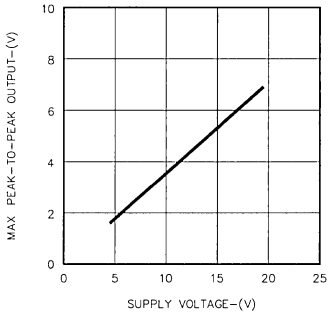


FIGURE 2.
MAXIMUM OUTPUT VS. SUPPLY VOLTAGE

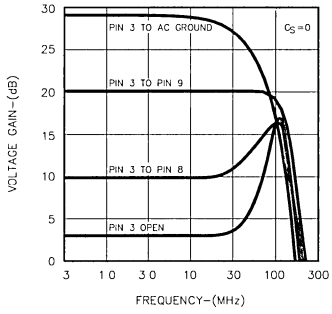


FIGURE 3.
FREQUENCY RESPONSE

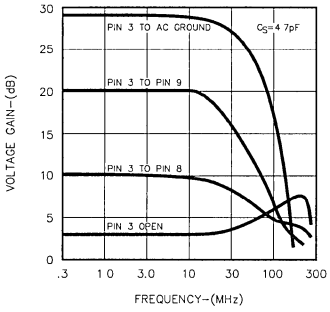


FIGURE 4.
STABILIZED FREQUENCY RESPONSE

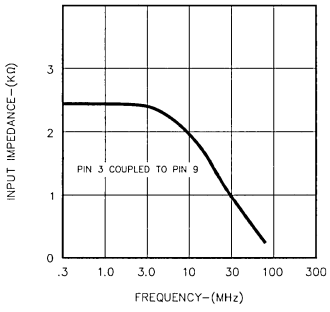


FIGURE 5.
INPUT IMPEDANCE VS. FREQUENCY

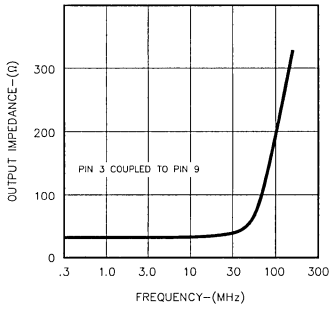


FIGURE 6.
OUTPUT IMPEDANCE VS. FREQUENCY

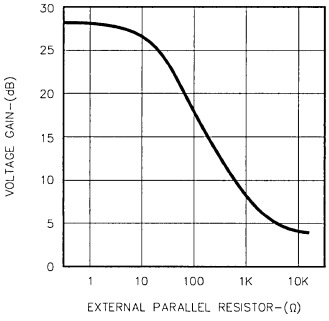


FIGURE 7.
EXTERNAL GAIN CONTROL

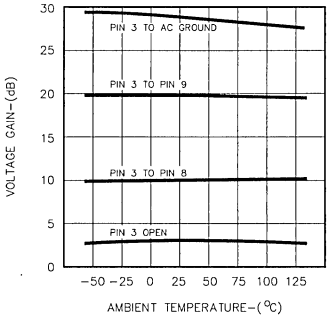


FIGURE 8.
TEMPERATURE STABILITY

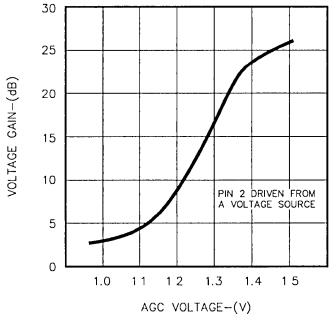


FIGURE 9.
GAIN VS. AGC DIODE VOLTAGE

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CHARACTERISTIC CURVES (continued)

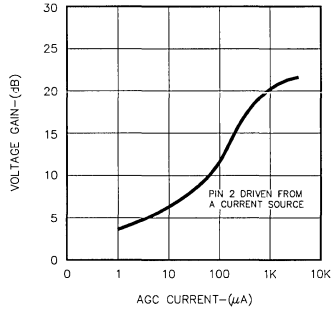


FIGURE 10.
GAIN VS. AGC DIODE CURRENT

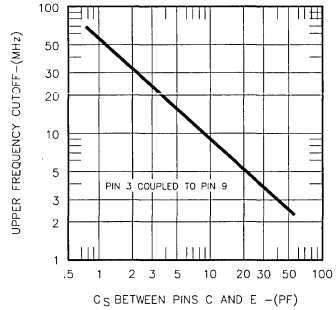


FIGURE 11.
UPPER CUTOFF FREQUENCY VS. C_S VALUE

APPLICATION INFORMATION

The SG1401 series has been designed to provide maximum versatility as a general-purpose, single-ended amplifier. With its broad frequency capability, this circuit will be useful in a wide range of applications provided that the usual considerations for high frequency circuit designs are observed. The following information is presented toward aiding in the optimization of the many possible configurations of this device.

FIXED GAIN

In the circuit configurations shown in Figure 12, the overall voltage gain is approximated by resistors R1 and the parallel combination of R_2 and R_3, as

$$A_V \approx 1 + \frac{R_1}{R} \text{ where } R = \frac{R_2 R_3}{R_2 + R_3}$$

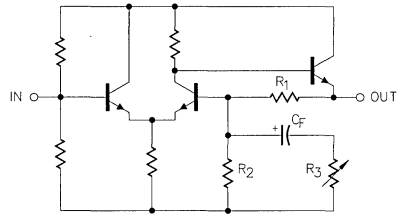


FIGURE 12

With no external connections, the voltage gain is determined solely by R_1 and R_2 and is 1½ or 3 dB. Decreasing the effective value of R_2 by capacitively coupling a lower resistor in parallel, raises the gain. Four fixed gain settings are provided internal to the circuit; however, any other setting within the maximum gain of the amplifier is possible with external resistors as shown in Figure 7.

The value of the coupling capacitor, C_F is determined by the low frequency response desired, as its capacitive reactance will add to the value of the resistance it couples. Therefore, the lower cutoff frequency will be

$$f_c \approx 2 \frac{1}{R_3 C_F}$$

Utilizing the internal 90 or 460 ohm resistors for higher gain settings provides the added advantage of maximum temperature stability since the close tracking of adjacent diffused resistors keeps their ratio constant. Typical temperature variation of this circuit is shown in Figure 8.

VARIABLE GAIN

Since the dynamic impedance of a forward-biased diode is inversely proportional to the current through it, a convenient gain control can be achieved by using a pair of diodes as a variable impedance. In the circuit of Figure 13, R_3 has been replaced by two diodes whose impedances act in parallel due to the decoupling of C_D. If the diodes are driven from a voltage source, a logarithim relationship between gain and control signal is achieved (see Figure 9); while if a current source is used, the relationship is linear as shown in Figure 10.

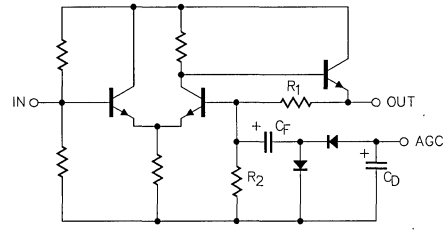


FIGURE 13

There are two limitations on this form of gain control. First, the diodes' capacitance limits their effectiveness to frequencies below 20MHz and, secondly, the signal voltage across the diodes should be held to less than 50 millivolts RMS to minimize self-modulation of amplifier gain. Additionally, the AGC current should be limited to 3mA maximum to keep the diodes out of saturation.

APPLICATION INFORMATION (continued)

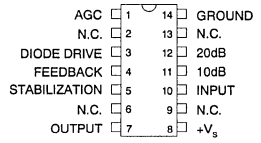
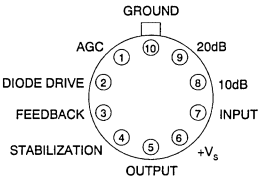
HIGH FREQUENCY STABILITY

With the capability of operation at 100MHz, the SG1401 series also has some susceptibility to external stray reactances; however, with reasonable care, complete stability may be assured. Some general precautions which should be considered include the following:

1. Power supply decoupling close to the circuit terminals (a 0.1μF capacitor is usually adequate).
2. Maintain separation of input and output lines.
3. Minimize load capacitance or insert a series resistor (up to 50Ω) in the output.
4. Purposely limit the high frequency response with a stabilizing capacitor C_S between pins 3 and 4.

Since the gain of this circuit is reduced by increasing the amount of feedback, the potential for instability is greatest when the gain is at its minimum value. This characteristic and the stabilizing effects of a 4.7 picofared capacitor between pins 4 and 3 are illustrated in the frequency response curves presented in Figures 3 & 4. The relationship between the value of C_S and the upper cutoff frequency of a 20dB gain setting is shown in Figure 11.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN CERAMIC DIP J - PACKAGE	SG1401J/883B SG1401J SG2401J SG3401J	-55°C to 125°C -55°C to 125°C 0°C to 70°C 0°C to 70°C	
14-PIN CERAMIC DIP N - PACKAGE	SG2401N SG3401N	0°C to 70°C 0°C to 70°C	
10-PIN METAL CAN T - PACKAGE	SG1401T/883B SG1401T SG2401T SG3401T	-55°C to 125°C -55°C to 125°C 0°C to 70°C 0°C to 70°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

SG1402/SG2402/SG3402

VARIABLE GAIN, WIDEBAND AMPLIFIER / MULTIPLIER

DESCRIPTION

The SG1402 is a monolithic four quadrant multiplier offering excellent frequency response and provision for use as a variable gain amplifier with both non-inverting and inverting outputs available. In addition to linear amplification, the device is also ideal for balanced modulation, pulse or gated amplification, and coincidence detection.

The SG1402 will operate over the full military ambient temperature range of -55°C to 125°C while the SG2402 and SG3402 are designed for 0°C to 70°C applications.

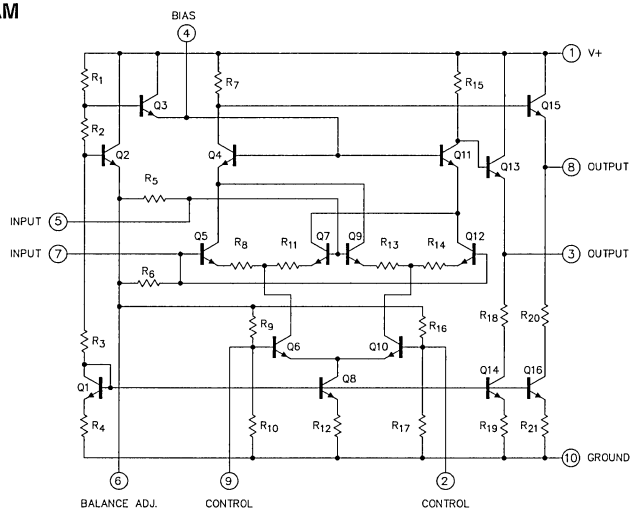
FEATURES

- **Single power supply voltage**
- **Self-contained biasing**
- **25dB voltage gain**
- **Differential or single ended inputs and outputs**
- **Large bandwidth**
- **Low power dissipation**

HIGH RELIABILITY FEATURES -SG1402

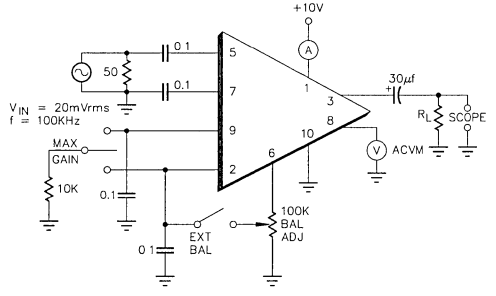
- ◆ **Available to MIL-STD-883**
- ◆ **SG level "S" processing available**

SCHEMATIC DIAGRAM



(Pin numbers correspond to T-package)

TEST CIRCUIT



(Pin numbers correspond to T-package)

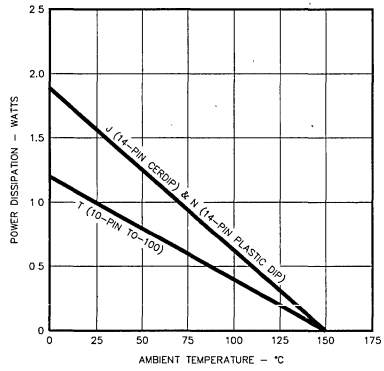
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage 18V
Load Current 15mA
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

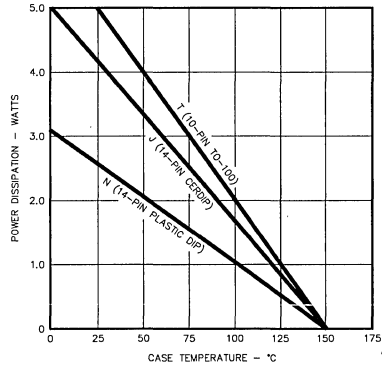
Operating Junction Temperature
Hermetic (J, T-Packages) ..... 150°C
Plastic (N-Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage ..... 16V (Note 3)

Operation Ambient Temperature Range
SG1402 ..... -55°C to 125°C
SG2402/SG3402 ..... 0°C to 70°C

Note 2. Range over which the device is functional.
Note 3. See Figure 6.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply for the operating ambient temperature of T_A = 25°C, V+ = +10V, and f = 100MHz. Low duty cycle pulse testing techniques are used which mintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1402/SG2402			SG3402			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Maximum Voltage Gain	Single ended	23	25		20	25		dB
Variable Gain Range	With external balance	55	60		40	50		dB
Frequency Response	f at 3dB	40	50			50		MHz
Input Impedance			1.2			1.2		KΩ
			1.8			1.8		KΩ
Output Impedance			100			100		Ω
Output Voltage Swing	R_L = 100K	3	4		3	4		V p-p
	R_L = 1K	1.3	1.6		1.3	1.6		V p-p
Quiescent DC Levels	Inputs and Balance Adjust		3.6			3.6		V
	Control Inputs		1.8			1.8		V
	Outputs	6.5	7.0	7.5		7.0		V
Output Offset Voltage	Minimum Gain			100			300	mV
	Maximum Gain			200			500	mV
DC Output Shift	With max. gain change			100			200	mV
Differential Control Voltage	For max. gain change		200			200		mV
Maximum Gain Variation with temperature	$T_A = T_{MIN}$ to T_{MAX}		1	2		1	3	dB
Equivalent Input Noise	BW = 10MHz, R_S = 50Ω		25			25		μVrms
Power Consumption	V+ = 10V		65	85		65	85	mW

CHARACTERISTIC CURVES

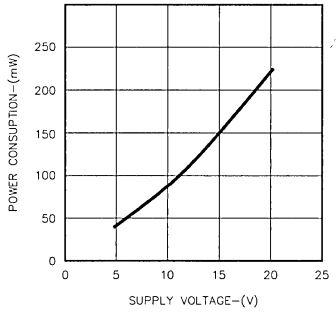


FIGURE 1.
MULTIPLIER TRANSFER FUNCTION

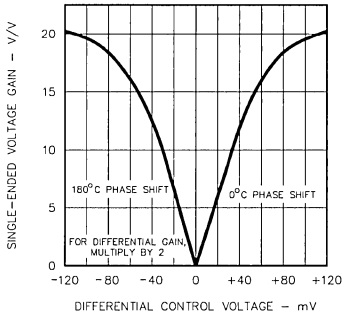


FIGURE 2.
SINGLE-ENDED GAIN CONTROL

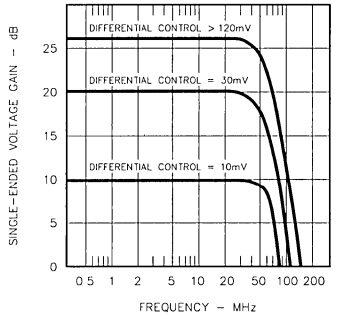


FIGURE 3.
FREQUENCY RESPONSE

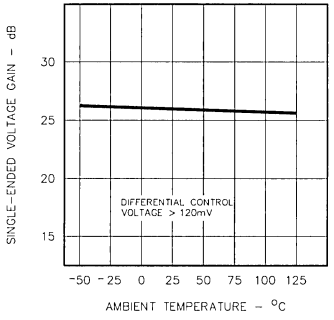


FIGURE 4.
MAXIMUM GAIN VS. TEMPERATURE

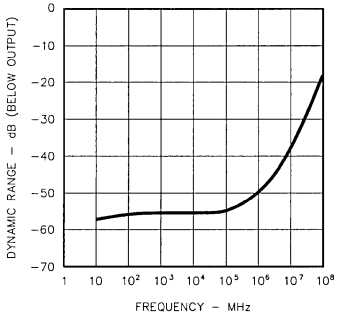


FIGURE 5.
DYNAMIC GAIN RANGE

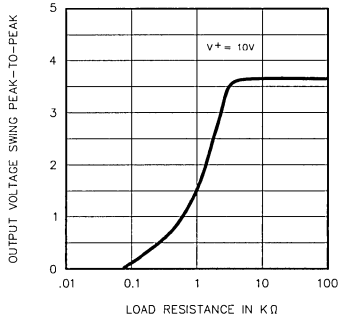


FIGURE 6.
MAXIMUM OUTPUT VOLTAGE

TYPICAL APPLICATIONS (Pin Numbers correspond to T - Package)

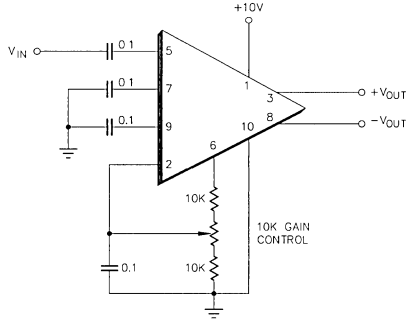


FIGURE 7

Single-ended or differential output variable gain amplifier with manual gain control for output of either phase.

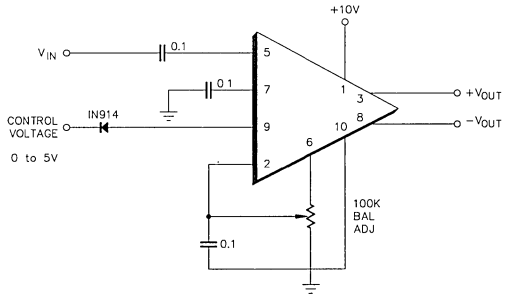


FIGURE 8

Gated amplifier for gain control without phase change. Balance control may be eliminated if maximum attenuation is not needed.

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TYPICAL APPLICATIONS (continued) (Pin Numbers correspond to T - Package)

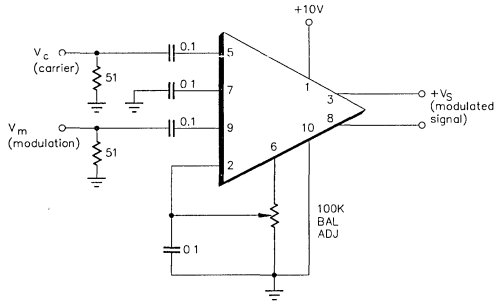


FIGURE 9

Modulator circuit with potentiometer adjustable for either amplitude or balanced modulation.

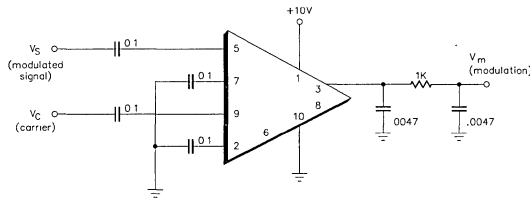
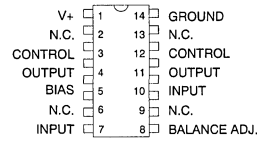
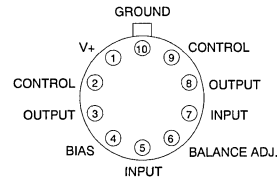


FIGURE 10

Balanced demodulator with output filter eliminating need for external balance.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN CERAMIC DIP J - PACKAGE	SG1402J/883B SG1402J SG2402J SG3402J	-55°C to 125°C -55°C to 125°C 0°C to 70°C 0°C to 70°C	
14-PIN CERAMIC DIP N - PACKAGE	SG2402N SG3402N	0°C to 70°C 0°C to 70°C	
10-PIN METAL CAN T - PACKAGE	SG1402T/883B SG1402T SG2402T SG3402T	-55°C to 125°C -55°C to 125°C 0°C to 70°C 0°C to 70°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

PRECISION 2.5-VOLT REFERENCE

DESCRIPTION

This monolithic integrated circuit is a fully self-contained precision voltage reference generator, internally trimmed for ±1% accuracy. Requiring less than 2mA in quiescent current, this device can deliver in excess of 10mA with total load- and line-induced tolerances of less than 0.5%. In additon to voltage accuracy, internal trimming achieves a temperature coefficient of output voltage of typically 10 ppm/°C. As a result, these references are excellent choices for application to critical instrumentation and D-to-A converter systems.

The SG1503 is specified for operation over the full military ambient temperature range of -55°C to 125°C , while the SG2503 is designed for -25°C to 85°C and the SG3503 for commercial applications of 0°C to 70°C.

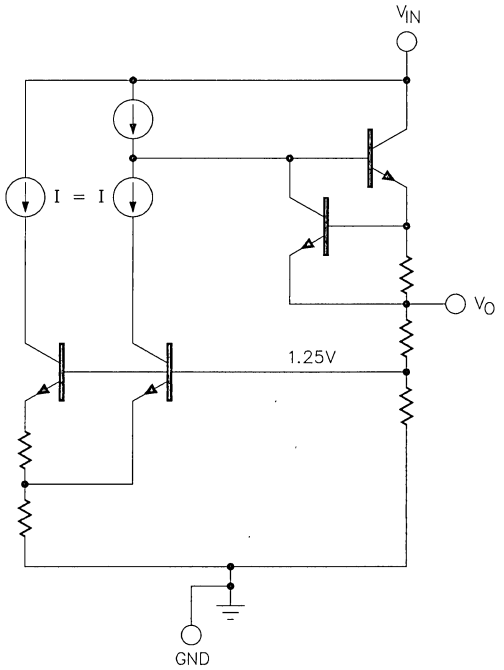
FEATURES

- **Output voltage trimmed to ±1%**
- **Input voltage range of 4.5 to 40V**
- **Temperature coefficent of 10ppm/°C**
- **Quiescent current typically 1.5mA**
- **Output current in excess of 10mA**
- **Interchangeable with MC1503 and AD580**

HIGH RELIABILITY FEATURES - SG1503

- ♦ **Available to MIL-STD-883 and DESC SMD**
- ♦ **Radiation data available**
- ♦ **SG level "S" processing available**

FUNCTIONAL DIAGRAM



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April 1990

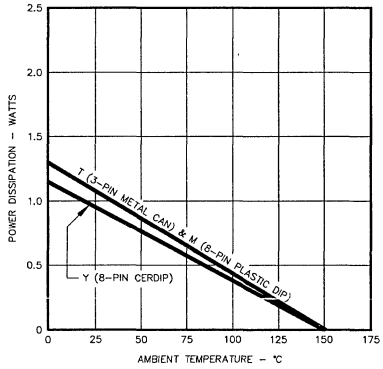
ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage 40V
Storage Temperature Range ..... -65°C to 150°C

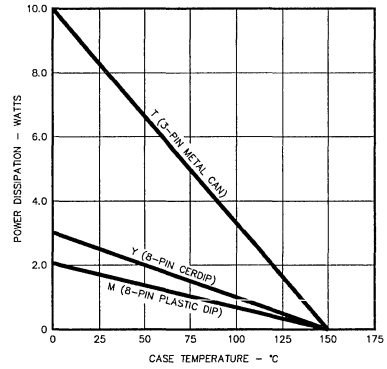
Operating Junction Temperature
Hermetic (J, Y - Package) ..... 150°C
Plastic (M-Package) ..... 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Voltage ..... 4.5V to 40V

Operating Ambient Temperature Range
SG1503 ..... -55°C to 125°C
SG2503/SG3503 ..... 0°C to 70°C

Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1503 with -55°C ≤ T_A ≤ 125°C, SG2503/SG3503 with 0°C ≤ T_A ≤ 70°C, V_{IN} = 15V, and I_L = 0mA. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1503/2503			SG3503			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	T_A = 25°C	2.485	2.500	2.515	2.475	2.500	2.525	V
Input Voltage		4.7		40	4.7		40	V
	T_A = 25°C	4.5		40	4.5		40	V
Line Regulation	V_{IN} = 5V to 15V		1	3		1	3	mV
	V_{IN} = 15V to 40V		3	5		3	10	mV
Load Regulation	ΔI_L = 10mA		3	5		3	10	mV
	ΔI_L = 10mA, V_{IN} = 30V		4	8		4	15	mV
Temperature Regulation	(SG1503 only)		15	20				mV
	(SG2503/3503 only)		2.5	5		5	10	mV
Quiescent Current	V_{IN} = 40V		1.5	2.0		1.5	2.0	mA
Short Circuit Current	T_A = 25°C	15	20	30	15	20	30	mA
Ripple Rejection	f = 120Hz, T_A = 25°C		76			76		dB
Output Noise	BW = 10KHz, T_A = 25°C		100			100		μV rms
Voltage Stability			250			250		μV/Khr

CHARACTERISTIC CURVES

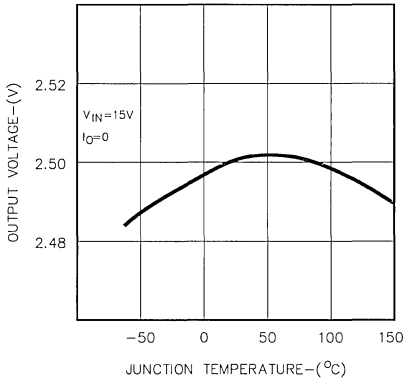


FIGURE 1.
OUTPUT VOLTAGE VS.
TEMPERATURE

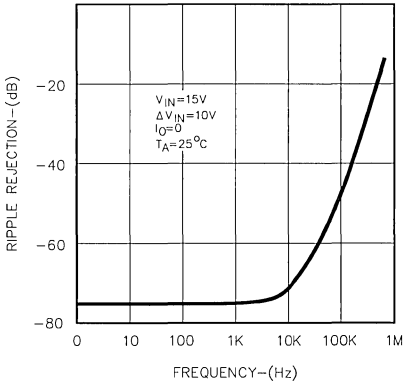
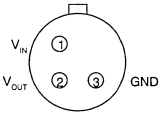


FIGURE 2.
RIPPLE REJECTION

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
8-PIN CERAMIC DIP Y - PACKAGE	SG1503Y/883B SG1503Y SG2503Y SG3503Y	-55°C to 125°C -55°C to 125°C 0°C to 70°C 0°C to 70°C	
8-PIN PLASTIC DIP M - PACKAGE	SG2503M SG3503M	0°C to 70°C 0°C to 70°C	
3-PIN TO-39 METAL CAN T - PACKAGE	SG1503T/883B SG1503T SG2503T SG3503T	-55°C to 125°C -55°C to 125°C 0°C to 70°C 0°C to 70°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

FOUR-QUADRANT MULTIPLIER

DESCRIPTION

The SG1595 and SG1495 four-quadrant analog multipliers are designed for applications where the output voltage required is a linear product of two input voltages. Both types provide excellent linearity and operation over a wide supply range and input voltage range. Applications include use as multipliers, dividers, squarers, phase detectors, frequency doublers, and as balanced modulators.

The SG1595 is rated for military ambient temperature applications over the -55°C to 125°C range; the SG1495 offers identical performance for 0°C to 70°C requirements.

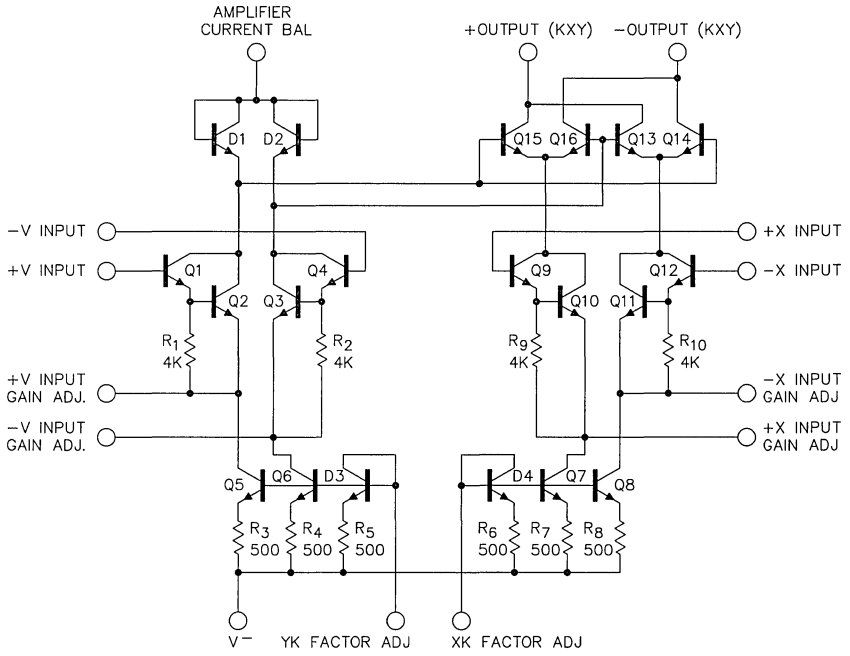
FEATURES

- **Excellent linearity**
- **Adjustable scale factor**
- **Excellent temperature stability**
- **Wide bandwidth**
- **High input voltage range**
- **Wide supply voltage operation**

HIGH RELIABILITY FEATURES -SG1595

- **Available to MIL-STD-883**
- **SG level "S" processing available**

CIRCUIT SCHEMATIC



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April 1990

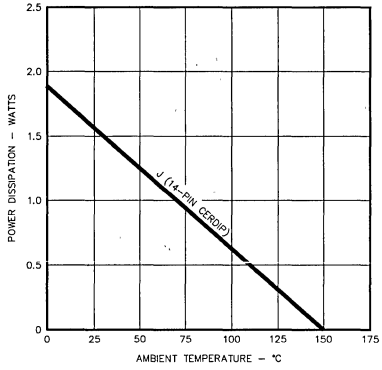
ABSOLUTE MAXIMUM RATINGS (Note 1)

Applied Voltage (Note 2) 30V
Differential Input Signal ..... $V_9 - V_{12} = \pm(6 + I_{13} R_X)$
$V_4 - V_8 = \pm(6 + I_3 R_Y)$
Factor Adjust Current 10mA

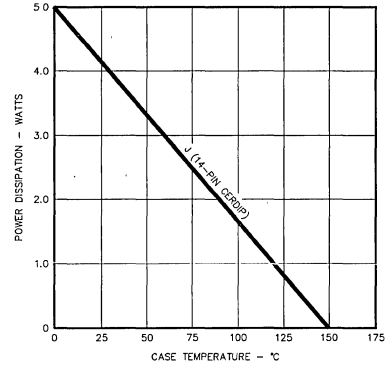
Operating Junction Temperature
Hermetic (J-Package) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.
Note 2. Voltage applied between pins 2-1, 14-1, 1-9, 1-12, 1-4, 1-8, 12-7, 9-7, 8-7, 4-7.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 3)

Applied Voltage 28V
Differential Input Signal ..... $V_9 - V_{12} = \pm(5 + I_3 R_X)$
$V_4 - V_8 = \pm(5 + I_3 R_Y)$
Factror Adjust Current (I_3),(I_{13}) 5mA

Operating Ambient Temperature Range
SG1595 ..... -55°C to 125°C
SG1495 ..... 0°C to 70°C

Note 3. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply for the operating ambient temperature of T_A=25°C. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1595			SG1495			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Linearity Error (% of Full Scale)	$-10 < V_X < 10$ ($V_Y = \pm 10V$)		0.5	2.0		1.0	4.0	%
	$-10 < V_Y < 10$ ($V_X = \pm 10V$)		1.0	4.0		2.0	8.0	%
	$T_A = T_{MIN}$ to T_{MAX}							
	$-10 < V_X < 10$ ($V_Y = \pm 10V$)		0.75	2.0		1.5	4.0	%
	$-10 < V_Y < 10$ ($V_X = \pm 10V$)		1.50	4.0		3.0	8.0	%
Squaring Mode Error (Note 4)			0.50			0.75		%
	$T_A = T_{MIN}$ to T_{MAX}		0.75			1.00		%
Scale Factor (adjustable) (Note 4 and 5)			0.1			0.1		
Input Resistance (Note 4)	f = 20Hz		35			20		MΩ
Differential Output Resistance (Note 4)	f = 20Hz		300			300		KΩ
Input Bias Current (Note 4)	$T_A = T_{MIN}$ to T_{MAX}		2.0	8.0		2.0	12	µA
Input Offset Current (Note 4)	$T_A = T_{MIN}$ to T_{MAX}		0.2	1.0		0.4	2.0	µA
Common-Mode Gain (Note 4)	$T_A = T_{MIN}$ to T_{MAX}	-50	-60		-40	-50		dB
Output Common–Mode Voltage			21			21		V
Differential Output Voltage Swing (Note 4)	$V_X = V_Y = 10V$, $T_A = T_{MIN}$ to T_{MAX}	±8	±14		±8	±14		V
Positive Supply Voltage Rejection Ratio			5			5		mV/V
Negative Supply Voltage Rejection Ratio			10			10		mV/V
Negative Supply Current (Note 4)	$T_A = T_{MIN}$ to T_{MAX}		6.0	7.0		6.0	7.0	mA

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1595			SG1495			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Power Consumption (Note 4)			135	170		135	170	mW
Average Temperature Coefficient of Input Offset Current	$T_A = T_{MIN}$ to T_{MAX}		2.5			2.5		nA/°C
Frequency Response	–3dB bandwidth		3.0			3.0		MHz
	3° relative phase shift		750			750		KHz
	1% absolute error due to input–output phase shift		30			30		KHz

Note 4. These parameters are guaranteed by design and process control but are not tested in production.

Note 5. $K = \frac{2R_L}{I_3 R_X R_Y}$

CHARACTERISTIC CURVES

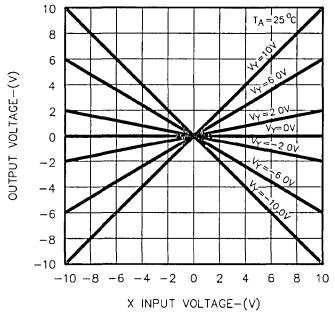


FIGURE 1.
STANDBY CURRENT

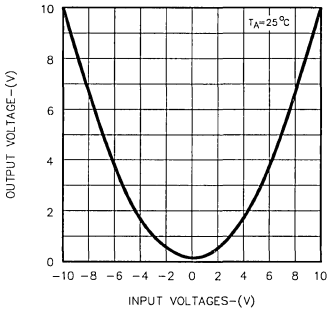


FIGURE 2.
MINIMUM INPUT-OUTPUT VOLTAGE

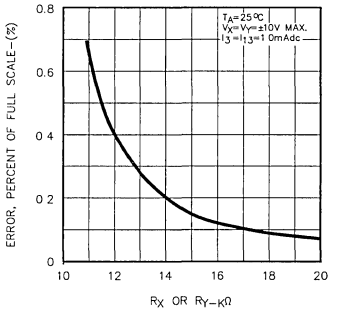


FIGURE 3.
MINIMUM INPUT-OUTPUT VOLTAGE

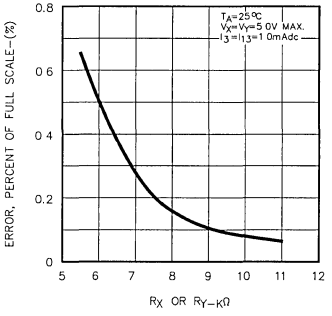


FIGURE 4.
CURRENT LIMITING

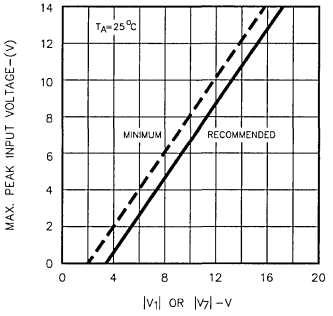


FIGURE 5.
RIPPLE REJECTION

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APPLICATION INFORMATION

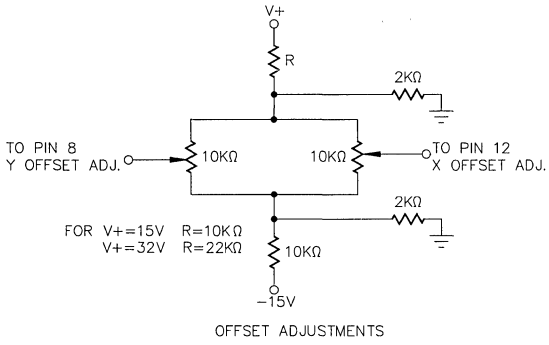


FIGURE 6

For best output accuracy, use above network and follow procedure at right.

RECOMMENDED ZERO ADJUSTMENT AND SCALE SETTING PROCEDURE

With $V_X = V_Y = 0V$ adjust the output offset adjustment until the output of the external amplifier reads 0V. Set $V_X = 5.000V$, $V_Y = 0.000V$, and adjust the Y-input offset control until the output amplifier reads 0V. Repeat this procedure for $V_X = 0.000V$, $V_Y = 5.000V$ and adjust the X-input offset control until the output amplifier reads 0V. This procedure should be repeated until complete null is achieved.

Next, set $V_X = V_Y = 5.000V$ and adjust the K-factor potentiometer until the output reads the desired output.

$V_{OUT} = 2.500V = K\,V_X\,V_Y$ for a K-factor of 0.100.

When a high degree of accuracy is unnecessary for small output signals, the above procedure may be simplified by eliminating the output offset adjustment.

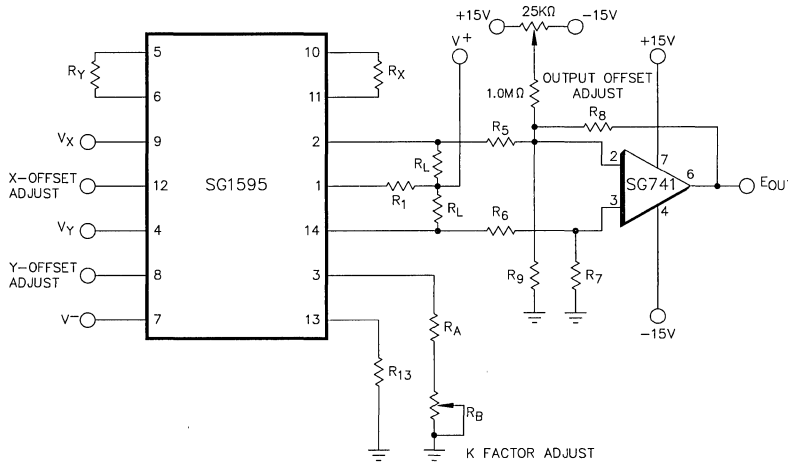


FIGURE 7 - MULTIPLY WITH OP AMP LEVEL SHIFT

SET UP	RESISTOR*	R_1	R_5	R_6	R_7	R_8	R_9	R_{13}	R_A	R_B	R_L	R_X	R_Y
	TOLERANCE	5%	1%	1%	1%	1%	1%	1%	5%	20%	0.5%	5%	5%
1	V+ = 32V, V- = -15V, $-10V \le V_X \le 10V$, $-10V \le V_Y \le 10V$	9.1	121	100	11	121	15	13.7	12	5.0	11	15	15
2	V+ = 15V, V- = -15V, $-5V \le V_X \le 5V$, $-5V \le V_Y \le 5V$	3.0	300	100	100	300		13.7	12	5.0	3.4	8.2	8.2
3	V+ = 15V, V- = -15V, $-10V \le V_X \le 10V$, $-10V \le V_Y \le 10V$	1.2	121	100	11	910	13.7	13.7	12	5.0	1.5	15	15

* All resistor values are in KΩ

APPLICATION INFORMATION (continued)

SUGGESTIONS AND GENERAL PRECAUTIONS

The high frequency performance of the SG1595 is primarily determined by two conditions. One, by the load resistors and the associated stray output capacitance of the multiplier and two, the operational amplifier used at the output. For maximum frequency of operation, low value load resistors and a wideband high slew rate operational amplifier should be used.

Phase shift at higher frequencies due to load resistors and output stray capacitances and relative phase shift between X and Y channels should be considered for maximum accuracy. As an example if the input to output phase shift is only 0.6°, the output product of two sine waves will exhibit a vector error of 1%. A 3° relative phase shift between the input signals will result in a vector error of 5%.

The normal circuit precautions should be taken to avoid parasitic oscillation. Leads should be as short as possible and the power supplies should be decoupled with a 0.1μF high frequency capacitor. An RC parasitic suppression network of 510Ω in series with a 10pF from each input to ground can be used to reduce the Q of a source-tuned circuit, which may cause the oscillation. As an alternate solution, a 510Ω resistor network can be placed in series with each input of the SG1595.

APPLICATION CIRCUITS

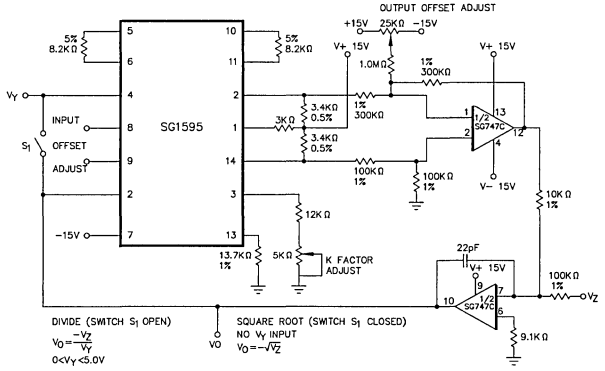


FIGURE 8 - DIVIDE AND SQUARE ROOT

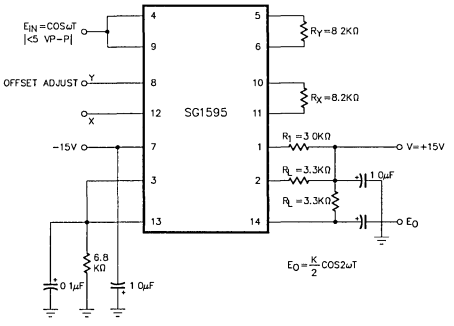


FIGURE 9 - FREQUENCY DOUBLER

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN CERAMIC DIP J - PACKAGE	SG1595J/883B SG1595J SG1495J	-55°C to 125°C -55°C to 125°C 0°C to 70°C	AMPLIFIER CURRENT BALANCE 1 / 14 - OUTPUT (KXY) + OUTPUT (KXY) 2 / 13 XK FACTOR ADJUST YK FACTOR ADJUST 3 / 12 -X INPUT +Y INPUT 4 / 11 -X INPUT GAIN ADJUST +Y INPUT GAIN ADJUST 5 / 10 +X INPUT GAIN ADJUST -Y INPUT GAIN ADJUST 6 / 9 +X INPUT V- 7 / 8 -Y INPUT

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

BALANCED MODULATOR/DEMODULATOR

DESCRIPTION

The SG1596 and SG1496 are monolithic double-balanced modulator/demodulator devices designed for use where the output volatge is a product of an input voltage (signal) and a switching function (carrier). Typical applications include modulation and demodulation of AM, SSB, DSB, FSK, FM and phase encoded signals. Additional uses include frequency doubling, linear mixing, and chopping.

The SG1596 will operate over the full military ambient temperature range of -55°C to 125°C; the SG1496 commericial counterpart is intended for application of 0°C to 70°C.

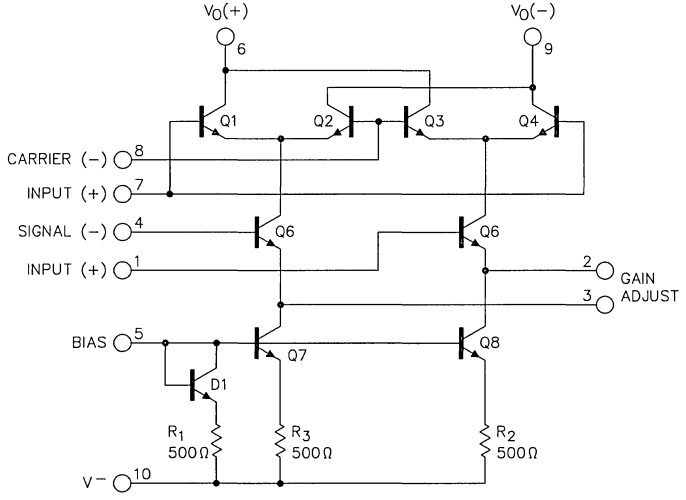
FEATURES

- **Excellent carrier suppression**
- **Fully balanced inputs and outputs**
- **Low offsets and drift**
- **High common-mode rejection**
- **Adjustable gain and signal handling**
- **Useful to 100MHz**

HIGH RELIABILITY FEATURES -SG1596

- ◆ **Available to MIL-STD-883**
- ◆ **SG level "S" processing available**

CIRCUIT SCHEMATIC



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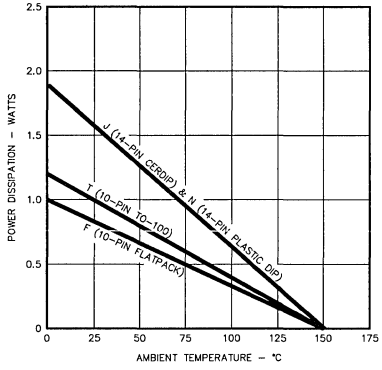
ABSOLUTE MAXIMUM RATINGS (Note 1)

Applied Voltage (Note 2) 30V
Differential Input Signal
(V_7 - V_8) ..... ±5.0V
(V_4 - V_1) ..... ±(5 + I_5R_E)V
Input Signal (V_2 - V_1, V_3 - V_4) 5.0V

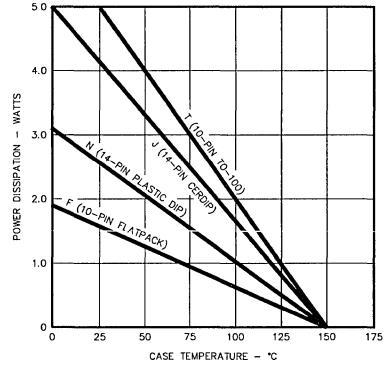
Maximum Bias Current 10mA
Operating Junction Temperature
Hermetic (J, T, F-Packages) ..... 150°C
Plastic (N-Package) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.
Note 2. Voltage applied between pins 6-7, 8-1, 9-7, 9-8, 7-4, 7-1, 8-4, 6-8, 2-5, 3-5.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 3)

Applied Voltage 28V
Differential Input Signal
(V_7-V_8) ..... ±4.0V
(V_4-V_1) ..... ±(4 + I_5R_E)V

Bias Current (I_5) 5mA
Operating Ambient Temperature Range
SG1596 ..... -55°C to 125°C
SG1496 ..... 0°C to 70°C

Note 3. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply for the operating ambient temperature of T_A=25°C. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1596			SG1496			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Carrier Feedthrough (Note 4)	V_C = 60mV (rms) sine wave							
	f_C = 1.0KHz, offset adjusted		40			40		μV(rms)
	f_C = 10MHz, offset adjusted		140			140		μV(rms)
	V_C = 300mV (p-p) square wave							
	f_C = 1.0KHz, offset adjusted		0.04	0.2		0.04	0.2	mV(rms)
	f_C = 1.0KHz, offset not adjusted		20	100		20	200	mV(rms)
Carrier Suppression (Note4)	f_S = 10KHz, 300mV (rms)							
	f_C = 500KHz , 60mV (rms) sine wave offset adjusted	50	65		50	65		dB
	f_S = 10KHz, 300mV (rms)							
	f_C = 10MHz , 60mV (rms) sine wave offset adjusted		50			50		dB
Transadmittance Bandwidth	Carrier Input Port, R_L = 50Ω,						-50	
	V_C = 60mV (rms) sine wave,							
	f_S = 1.0KHz, 300mV (rms) sine wave		300			300		MHz
	Signal Input Port, V_S = 300mV (rms)		80			80		MHz

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG1595			SG1495			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Voltage Gain, Signal Channel	V_S = 100mV (rms), f = 1.0KHz, $V_7 - V_8$ = 0.5V, $T_A = T_{MIN}$ to T_{MAX}	2.5	3.5		2.5	3.5		V/V
Input Resistance, Signal Port	f = 5.0MHz, $V_7 - V_8$ =0.5V		200			200		KΩ
Input Capacitance, Signal Port	f = 5.0MHz, $V_7 - V_8$ =0.5V		2.0			2.0		pF
Single-Ended Output Resistance	f = 10MHz		40			40		KΩ
Single-Ended Output Capacitance	f = 10MHz		5.0			5.0		pF
Input Bias Current	$(I_1 + I_4)/2$, $T_A = T_{MIN}$ to T_{MAX}		12	25		12	30	μA
	$(I_7 + I_8)/2$, $T_A = T_{MIN}$ to T_{MAX}		12	25		12	30	μA
Input Offset Current	$(I_1 - I_4)$, $T_A = T_{MIN}$ to T_{MAX}		0.7	5.0		0.7	7.0	μA
	$(I_7 - I_8)$, $T_A = T_{MIN}$ to T_{MAX}		0.7	5.0		0.7	7.0	μA
Average Temperature Coefficient of Input Offset Current	$T_A = T_{MIN}$ to T_{MAX}		2.0			2.0		nA/°C
Output Offset Current	$(I_6 - I_9)$, $T_A = T_{MIN}$ to T_{MAX}		14	50		14	80	μA
Average Temperature Coefficient of Output Offset Current	$T_A = T_{MIN}$ to T_{MAX}		90			90		nA/°C
Signal Port Common-Mode Input Voltage Range	f_S = 1.0KHz		5.0			5.0		V p-p
Signal Port Common-Mode Rejection Ratio	$V_7 - V_8$ = 0.5V		-85			-85		dB
Common-Mode Quiescent Output Voltage			8.0			8.0		V
Differential Output Swing Capability			8.0			8.0		V p-p
Positive Supply Current	$(I_6 + I_9)$, $T_A = T_{MIN}$ to T_{MAX}		2.0	3.0		2.0	4.0	mA
Negative Supply Current	(I_{10}), $T_A = T_{MIN}$ to T_{MAX}		3.0	4.0		3.0	5.0	mA
Power Dissipation			33			33		mW

Note 4. These parameters are guaranteed by design and process control but are not tested in production.

CHARACTERISTIC CURVES

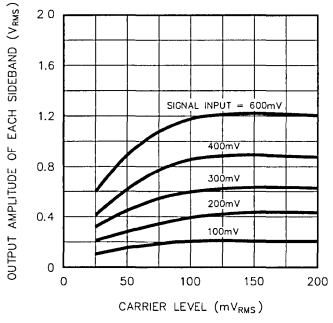


FIGURE 1.
SIDEBAND OUTPUT VS. CARRIER LEVELS

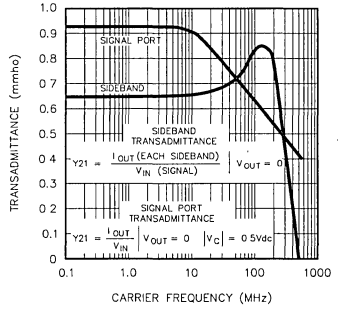


FIGURE 2.
SIDEBAND AND SIGNAL PORT
TRANSADMITTANCES VS. CARRIER LEVELS

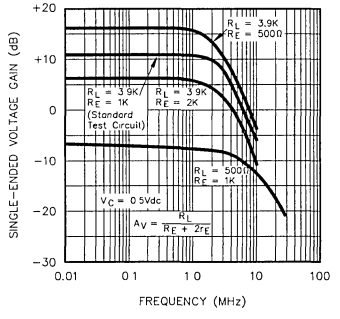


FIGURE 3.
SIGNAL-PORT FREQUENCY RESPONSE

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CHARACTERISTIC CURVES (continued)

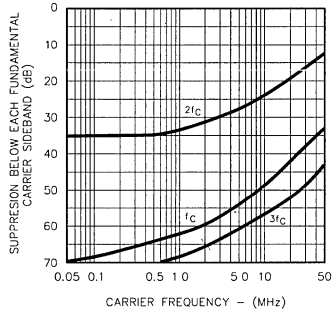


FIGURE 4.
CARRIER SUPPRESSION VS.
FREQUENCY

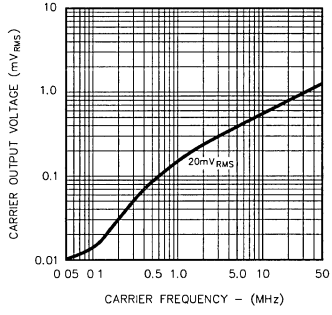


FIGURE 5.
CARRIER FEEDTHROUGH VS.
FREQUENCY

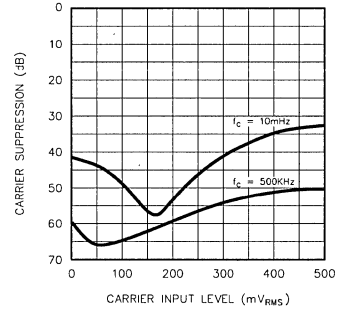
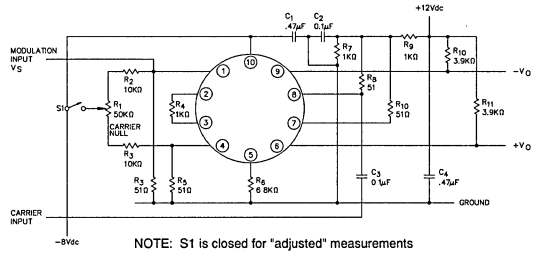


FIGURE 6.
CARRIER SUPRESSION VS.
CARRIER INPUT LEVEL

APPLICATION INFORMATION

TYPICAL MODULATOR CIRCUIT

Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source-tuned circuits that cause the oscillation.



NOTE: S1 is closed for "adjusted" measurements

FIGURE 7 - TYPICAL MODULATOR CIRCUIT

PRODUCT DETECTOR

This figure shows the SG1596 used as a single sideband suppressed carrier demodulator (Product Detector). The carrier signal is applied to the carrier input port with sufficient amplitude for switching operation. A carrier input level of 300 mV (rms) is optimum. The composite SSB signal is applied to the signal input port with an amplitude of 5.0 to 500mV (rms). All output signal components except the desired demodulated audio are filtered out, so that an offset adjustment is not required. This circuit may also be used as an AM detector by applying composite and carrier signals in the same manner as described for product detector operation.

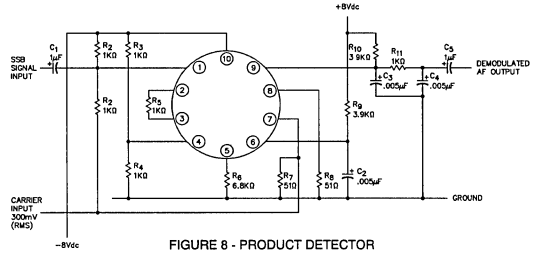


FIGURE 8 - PRODUCT DETECTOR

FREQUENCY DOUBLER

The frequency doubler circuit shown will double low-level signals with low distortion. The value of C should be chosen for low reactance at the operating frequency.

Signal level at the carrier input must be less than 25mV peak to maintain operation in the linear region of the switching differential amplifier. Levels to 50mV peak may be used with some distortion of the output waveform. If a large input signal is available a resistive divider may be used at the carrier input, with full signal applied to the signal input.

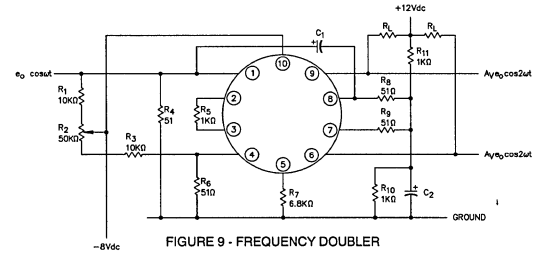


FIGURE 9 - FREQUENCY DOUBLER

APPLICATION INFORMATION (continued)

SIGNAL PORT STABILITY

Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source-tuned circuits that cause the oscillation.

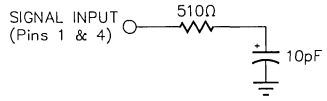
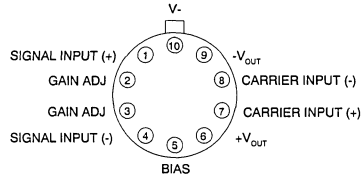
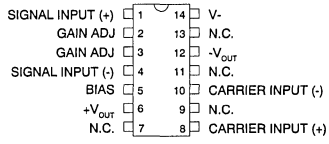
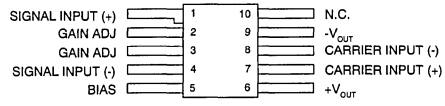


FIGURE 10 - SIGNAL PORT STABILITY

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
10-PIN METAL CAN T - PACKAGE	SG1596T/883B SG1596T SG1496T	-55°C to 125°C -55°C to 125°C 0°C to 70°C	
14-PIN CERAMIC DIP J - PACKAGE 14-PIN PLASTIC DIP N - PACKAGE	SG1596J/883B SG1596J SG1496J SG1496N	-55°C to 125°C -55°C to 125°C 0°C to 70°C 0°C to 70°C	
10-PIN CERAMIC FLAT PACK F - PACKAGE	SG1596F/883B SG1596F	-55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

DUAL HIGH-FREQUENCY OPERATIONAL AMPLIFIER

DESCRIPTION

The SG3049 consists of dual high-frequency differential amplifiers with associated constant-current transistors on a common monolithic substrate. The monolithic construction provides close electrical and thermal matching of the amplifiers. The transistors which comprise the amplifiers are general-purpose devices with f_T in excess of 600MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

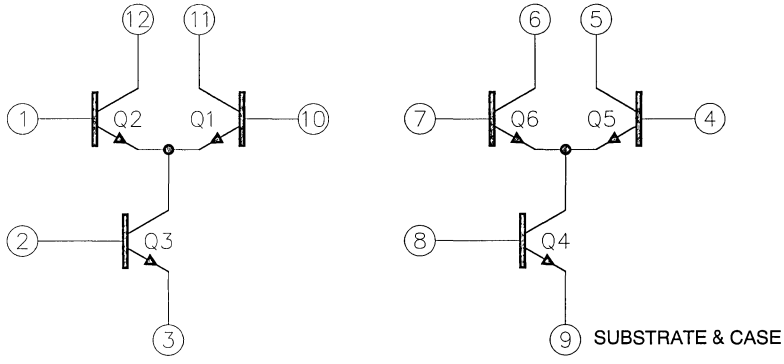
FEATURES

- **V_{SO} matching typically 200μV over operating current and voltage**
- **Two differential amplifiers on a common substrate**
- **Independently accessible inputs and outputs**
- **Full military temperature range capability**

HIGH RELIABILITY FEATURES

- **Available to MIL-STD-883**
- **SG level "S" processing available**

SCHEMATIC DIAGRAM



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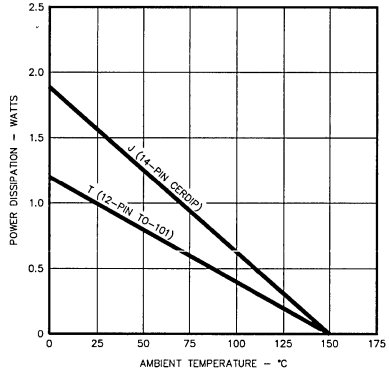
ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Collector to Emitter Voltage (V_{CEO}) 15V
Collector to Base Voltage (V_{CBO}) 20V
Collector to Substrate Voltage (V_{CIO}) 20V
Emitter to Base Voltage (V_{EBO}) 5V
Collector Current (I_C) 50mA

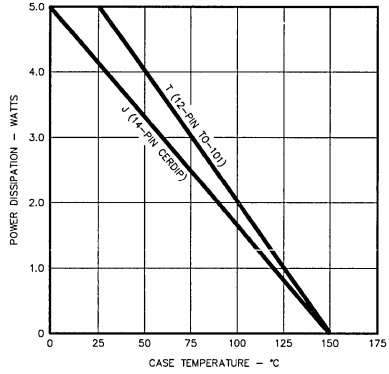
Operating Junction Temperature
Hermetic (J, T-Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Electrical values apply for each transistor.
Note 2. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Notes 1 and 3)

Operating Ambient Temperature Range
SG3049 ..... -55°C to 125°C

Note 3. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures of -55°C ≤ T_A ≤ 125°C. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG3049 Min.	SG3049 Typ.	SG3049 Max.	Units
Static Characteristics (Each Transistor)					
Breakdown Voltages					
Collector-Base ($V_{(BR)CBO}$)	I_C = 10μA, I_E = 0	20	60		V
Collector-Substrate ($V_{(BR)CIO}$)	I_C = 10μA, I_B = 0, I_E = 0	20	60		V
Collector-Emitter ($V_{(BR)CEO}$)	I_C = 1mA, I_B = 0	15	24		V
Emitter-Base ($V_{(BR)EBO}$)	I_E = 10μA, I_C = 0	5	7		V
Collector Cutoff Current (I_{CBO})	V_{CB} = 10V, I_E = 0			100	nA
Base-Emitter Voltage (V_{BE})	V_{CE} = 3V, I_C = 1mA				
	T_A = 25°C	0.60	0.70	0.80	V
	T_A = T_{MIN}	0.72	0.80	0.92	V
	T_A = T_{MAX}	0.50	0.60	0.70	V
Static Characteristics (Each Differential Amplifier)					
Input Offset Voltage (V_{IO})	$I_E(Q_3)$ = $I_E(Q_4)$ = 2mA, V_{CB} = 3V		0.45	5.0	mV
Input Offset Current (I_{IO})	$I_E(Q_3)$ = $I_E(Q_4)$ = 2mA, V_{CB} = 3V		0.30	3.0	μA
Input Bias Current (I_{IB})	$I_E(Q_3)$ = $I_E(Q_4)$ = 2mA, V_{CB} = 3V		10	45	μA
DC Gain (h_{FE})					
Q_3	$I_E(Q_3)$ / $I_B(Q_3)$	35	150	300	
Q_4	$I_E(Q_4)$ / $I_B(Q_4)$	35	150	300	

ELECTRICAL SPECIFICATIONS (continued)

Parameter	Test Conditions	SG3049 Min.	SG3049 Typ.	SG3049 Max.	Units
Dynamic Characteristics (T_A = 25°C)					
Common-Mode Rejection Ratio (CMRR) (Each Amplifier)	V_{CC} = 12V, V_{EE} = -6V, V_X = 3.3V, f = 1KHz (See Figure 2)		80		dB
Automatic Gain Control Range (AGC) (Single Stage)	V_{CC} = 12V, V_{EE} = -6V, V_X = 3.3V, f = 1KHz (See Figure 3)		75		dB
Voltage Gain (A_V) (Single Stage, Double-Ended Output)	V_{CC} = 12V, V_{EE} = -6V, V_X = 3.3V, f = 1KHz (See Figure 3)		35		dB
Gain Bandwidth Product (f_T) (Single Transistor)	I_C = 3mA, V_{CE} = 3V		600		MHz
Noise Figure (NF) (Single Transistor)	V_{CE} = 3V, I_C = 100μA, R_X = 1KΩ, f = 1KHz, BW = 15.7KHz		3.25		dB
(Each Amplifier)	f = 100MHz		8		dB

TEST CIRCUITS

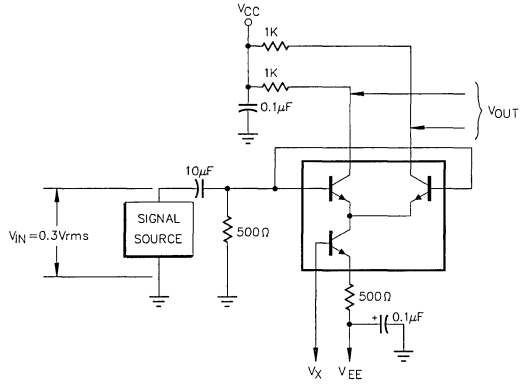


FIGURE 2 - COMMON-MODE REJECTION RATIO

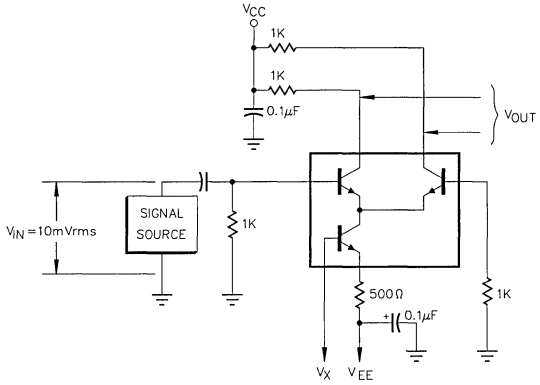


FIGURE 3 - SINGLE-STAGE VOLTAGE GAIN

CHARACTERISTIC CURVE

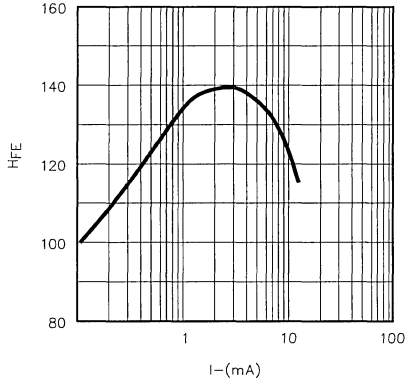


FIGURE 1 - DC GAIN VS. CURRENT

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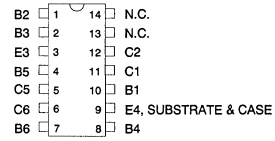
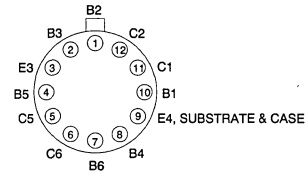
CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN CERAMIC DIP J - PACKAGE	SG3049J/883B SG3049J	-55°C to 125°C -55°C to 125°C	
12-PIN METAL CAN T - PACKAGE	SG3049T/883B SG3049T	-55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

HIGH-CURRENT NPN TRANSISTOR ARRAYS

DESCRIPTION

The SG 3183 series of arrays consists of five, closely-matched, high-current NPN transistors. Although sharing a common monolithic substrate, the transistors are connected such that all terminals are independent, including the substrate bias connector. With current capability to 100mA per transistor, these arrays are ideally suited for all types of driving applications including relays, lamps, and thyristors.

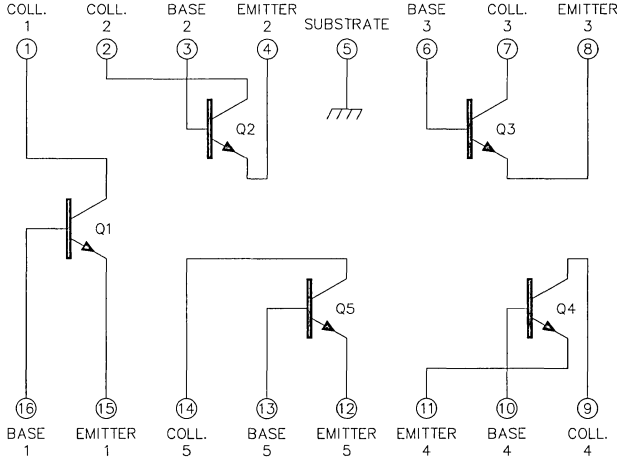
FEATURES

- **High voltage capability**
- **Collector current to 100mA**
- **Low saturation voltage**
- **Closely matched parameters**

HIGH RELIABILITY FEATURES - SG3183

- ♦ **Available to MIL-STD-883**
- ♦ **SG level "S" processing available**

BLOCK DIAGRAM



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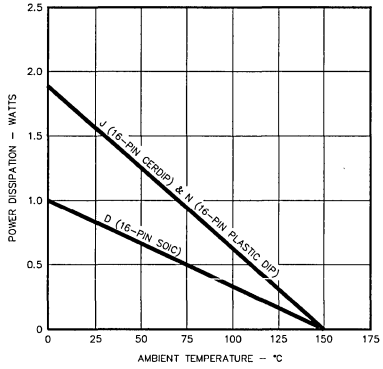
ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Collector Current 100mA
Maximum Base Current 20mA
Power Dissipation
  Any One Transistor 500mW
  Total Package 750mW

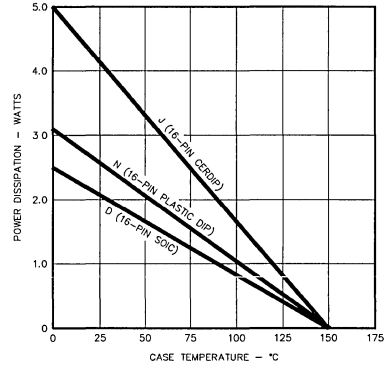
Operating Junction Temperature
  Hermetic (J-Packages) ..... 150°C
  Plastic (N, D-Package) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Operating Ambient Temperature
  SG3183 (J-Package) ..... -55°C to 125°C
  SG3183 (N, D-Package) ..... 0°C to 70°C

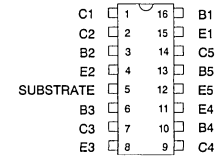
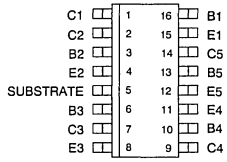
Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures of $-55°C \le T_A \le 125°C$ for the SG3183 (J-package) and $0°C \le T_A \le 70°C$ for the SG3183 (N & D - packages). Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG3183 Min.	SG3183 Typ.	SG3183 Max.	Units
Breakdown Voltage					
Collector-Substrate (BV_{CSO})	I_C= 100µA	40	70		V
Collector-Base (BV_{CBO})	I_C= 100µA	40	70		V
Collector-Emitter (BV_{CEO})	I_C= 1mA	30	40		V
Emitter-Base (BV_{EBO})	I_E = 100µA	5.0	6.9		V
Collector Cutoff Current (I_{CEO})	V_{CE} = 10V			10	µA
Collector Cutoff Current (I_{CBO})	V_{CB} = 10V			1	µA
DC Forward Current Transfer Ratio (h_{FE})					
	V_{CE} = 3V, I_C = 10mA	40			
	T_A = 25°C	50	100		
	V_{CE} = 3V, I_C = 10mA	35			
	T_A = 25°C	40	75		
Collector–Emitter Saturation Voltage ($V_{CE(SAT)}$)	I_C = 50mA, I_B = 5mA		1.7	3.0	V
Base-to-Emitter Voltage (V_{BE})	V_{CE} = 3V, I_C = 10mA	0.50		0.95	V
	T_A = 25°C	0.65	0.75	0.85	V
For Q_1 and Q_2 Matched Pair:	V_{CE} = 3V, I_C = 1mA				
Input Offset Voltage (V_{IO})				10	mV
	T_A = 25°C		1.2	5.0	mV
Input Offset Current (I_{IO})				5.0	µA
	T_A = 25°C		0.7	2.5	µA

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
16-PIN CERAMIC DIP J - PACKAGE	SG3183J/883B SG3183J	-55°C to 125°C -55°C to 125°C	
16-PIN PLASTIC DIP N - PACKAGE	SG3183N	0°C to 70°C	
16-PIN SOIC D - PACKAGE	SG3183D	0°C to 70°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

SG3821/SG3045/SG3046

MATCHED NPN TRANSISTOR ARRAYS

DESCRIPTION

These five matched transistors are general purpose NPN transistors configured with two internally connected to form a differential amplifier, each with its own associated source transistor. They are well suited to a wide variety of applications in low power systems in the DC through VHF range. In addition to being used as discrete transistors in conventional circuits, they also provide the very significant inherent integrated circuit advantages of close electrical and thermal matching. These transistor arrays offer V_{BE} typically matched to ±0.5mV, less than 10% variation in h_{FE}, operation from DC to 300MHz, high current gain from 10μA to 10mA, and high voltage capability.

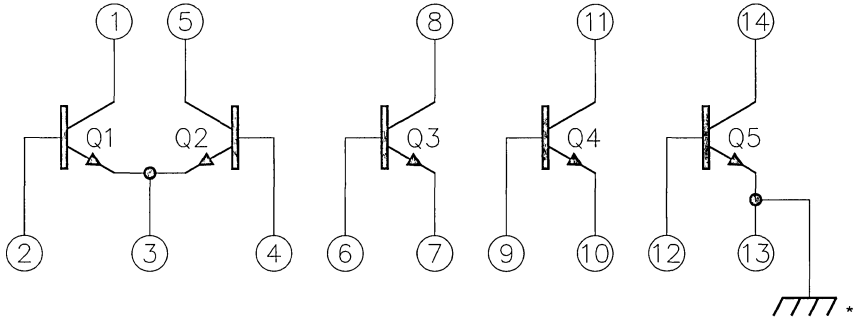
FEATURES

- **Two matched transistor pairs ±0.5mV**
- **Five general purpose matched transistors**
- **Operation from DC to 300MHz**
- **High current gain**
- **High voltage capabilities**

HIGH RELIABILITY FEATURES - SG3821

- ♦ **Available to MIL-STD-883**
- ♦ **SG level "S" processing available**

SCHEMATIC DIAGRAM



* Substrate pin must be connected to the most negative DC potential - which should also be a good AC ground - for proper isolation between transistors.

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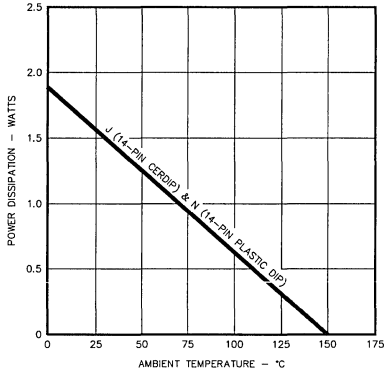
ABSOLUTE MAXIMUM RATINGS (Note 1)

Collector to SubstrateVoltage 40V
Collector to Base Voltage 40V
Collector to Emitter Voltage 25V
Storage Temperature Range ..... -65°C to 150°C

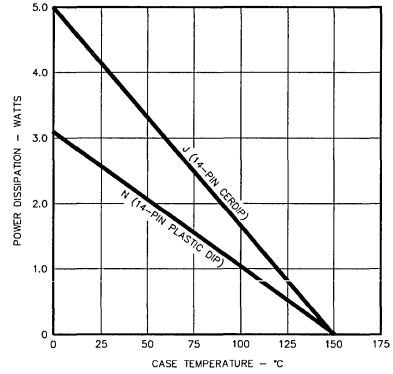
Operating Junction Temperature
Hermetic (J-Package) ..... 150°C
Plastic (N-Package) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DERATING CURVES



MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



MAXIMUM POWER DISSIPATION vs CASE TEMPERATURE

RECOMMENDED OPERATING CONDITIONS (Note 2)

Operating Ambient Temperature Range
SG3045, SG3821 ..... -55°C to 125°C
SG3046 ..... 0°C to 70°C

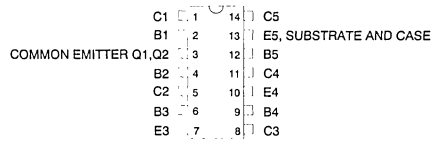
Note 2. Range over which the device is functional.

ELECTRICAL SPECIFICATIONS

(Unless otherwise specified, these specifications apply for the operating ambient temperature of T_A = 25°C. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG3821/3046			SG3045			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Breakdown Voltage:								
Collector-Substrate (BV_{CSO})	I_C = 10μA, I_B = 0	40			20			V
Collector-Base (BV_{CSO})	I_C = 10μA, I_E = 0	40			20			V
Collector-Emitter (BV_{CEO})	I_C = 100μA, I_B = 0	25			15			V
Emitter-Base (BV_{EBO})	I_E = 10μA, I_C = 0	5			5			V
Leakage Current								
Collector-Substrate (I_{CSO})	V_{CS} = 20V, I_B = 0			80			80	nA
Collector-Base (I_{CSO})	V_{CB} = 20V, I_E = 0			40			40	nA
Collector-Emitter (I_{CEO})	V_{CE} = 20V, I_B = 0			500			500	nA
Forward Current-Transfer Ratio (h_{FE})	V_{CE} = 5V, I_C = 10μA		80			80		
	V_{CE} = 5V, I_C = 1mA	50		400	50		400	
	V_{CE} = 5V, I_C = 10mA		80			80		
Base-to-Emitter Voltage (V_{BE})	V_{CE}= 5V, I_E = 10mA		0.5			0.5		V
Collector-Emitter Saturation ($V_{CE(SAT)}$)	I_C = 10mA, I_B= 1mA	0.5		0.9	0.5		0.9	V
Gain-Bandwidth Product	V_{CE} = 5V, I_C= 3mA		500			500		MHz
Collector-Substrate Capacitance	V_{CS} = 5V, I_C= 0		2.0			2.0		pF
Collector-Base Capacitance	V_{CB} = 5V, I_C= 0		0.4			0.4		pF
Noise Figure	f = 1KHz, V_{CE} = 5V, I_C = 100mA, R_S = 1kΩ		4			4		dB
Input Offset Voltage (V_{IO})	V_{CE} = 5V, I_C=1mA			5			5	mV
Input Offset Current (I_{IO})	V_{CE} = 5V, I_C=1mA			4			2	μA

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN CERAMIC DIP J - PACKAGE	SG3821J/883B SG3821J SG3821N SG3045J/883B SG3045J	-55°C to 125°C -55°C to 125°C 0°C to 70°C -55°C to 125°C -55°C to 125°C	
14-PIN PLASTIC DIP N - PACKAGE	SG3046N	0°C to 70°C	

Note 1. Contact factory for JAN and DESC product availablity.
2. All packages are viewed from the top.

SILICON GENERAL

LINEAR INTEGRATED CIRCUITS

THERMAL CHARACTERISTICS

No. of Pins	Pkg. Symbol	JEDEC No.	θ_{JA} (°C/W)	θ_{JC} (°C/W)	P_D 25°C (mW)	Derate > 25° (mW/°C)
PLASTIC DUAL-IN-LINE (DIP)						
8	M		95	60	1050	10.5
14	N		65	40	1540	15.4
16	N		65	40	1540	15.4
16	W	(Batwing)	45	15*	2220	22.2
18	N		60	30	1670	16.7
20	N		60	30	1670	16.7
22	N		55	27	1820	18.2
24	N	(Wide)	52	25	1920	19.2
24	N	(Narrow)	58	29	1720	17.2
28	N		45	20	2220	22.2
40	N		40	15	2500	25.0
PLASTIC SMALL OUTLINE (S.O.I.C.)						
8	DM		165	55	610	6.1
14	D		120	50	830	8.3
16	D		120	50	830	8.3
16	DW		95	40	1050	10.5
18	DW		90	35	1110	11.1
20	DW		86	32	1160	11.6
20	DWW	(Batwing)	50	12*	2000	20.0
PLASTIC (POWER)						
3	P	TO-220	60	4.5*	1670	16.7
3	V	TO-247	50	1.5*	2000	20.0
5	P	TO-220	55	4.0*	1820	18.2
12	S	(SIP)	45	2.0*	2220	22.2
12	ST	(SIP)	45	2.0*	2220	22.2
PLASTIC LEADED CHIP CARRIER						
20	Q	(PLCC)	80	35	1250	12.5
28	Q	(PLCC)	70	20	1430	14.3
CERAMIC DUAL-IN-LINE						
8	Y		130	50	960	7.7
14	J		80	30	1560	12.5
16	J	TO-116	80	30	1560	12.5
18	J		70	25	1790	14.3
CERAMIC SIDE BRAZED (DIP)						
14	H		100	30	1250	10.0
16	H		100	30	1250	10.0
18	H		85	25	1470	11.8
CERAMIC FLAT PACK (CERPAC)						
10	F		145	80	860	6.9
14	F		140	80	890	7.1
16	F		115	70	1090	8.7
20	F		115	70	1090	8.7
24	F		110	70	1140	9.1

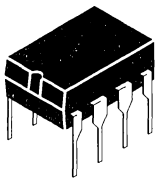
No. of Pins	Pkg. Symbol	JEDEC No.	θ_{JA} (°C/W)	θ_{JC} (°C/W)	P_D 25°C (mW)	Derate > 25° (mW/°C)
CERAMIC LEADLESS CHIP CARRIER						
20	L	(LCC)	120	35	1040	8.3
METAL CANS						
2	Z	TO-46	440	80	200	2.3
3	Z	TO-52	440	80	280	2.3
3	T	TO-39	120	15	1040	8.3
3	K	TO-3	35	3.0	3570	28.6
3	R	TO-66	40	5.0	3120	25.0
4	R	TO-66 (SM)	40	4.0	3120	25.0
4	K	TO-3 (SM)	35	2.0	3570	28.6
5	R	TO-66	40	5.0	3120	25.0
8	T	TO-99	130	25	960	7.7
9	R	TO-66	40	5.0	3120	25.0
10	T	TO-100	130	25	960	7.7
10	T	TO-96 (tall)	130	25	960	7.7
12	T	TO-101	130	25	960	7.7
TO-257 (HERMETIC TO-220)						
3	G	(Non-Iso)	42	3.5*	2980	23.8
3	IG	(Isolated)	42	3.5*	2980	23.8

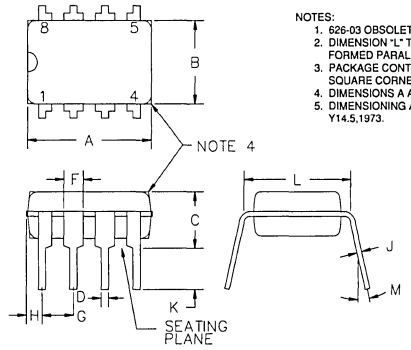
* = θ_{JT} (Junction to Tab)

Note: This data is for reference only as it does not account for thermal transfer characteristics of variable die sizes.

January 1990

PLASTIC MINI-DIP 8-PIN "M" SUFFIX

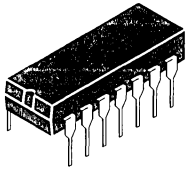


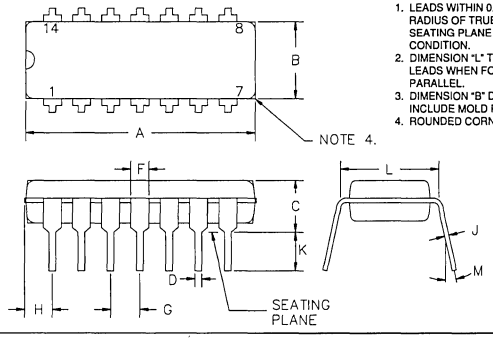


NOTES:
1. 626-03 OBSOLETE NEW STD 626-04.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
4. DIMENSIONS A AND B ARE DATUMS.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5,1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	10.16	–	0.400
B	6.10	6.60	0.240	0.260
C	–	5.08	–	.200
D	0.38	0.51	0.015	0.020
F	0.76	1.52	0.030	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.83	0.030	0.072
J	0.20	0.38	0.008	0.015
K	3.18	–	0.125	–
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°

PLASTIC DIP 14-PIN "N" SUFFIX

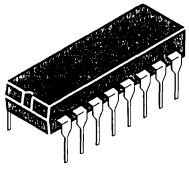


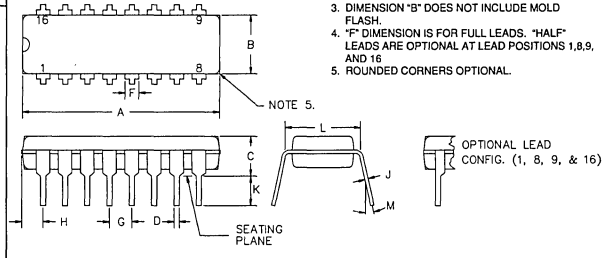


NOTES:
1. LEADS WITHIN 0.13mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.54	19.94	0.730	0.785
B	5.59	7.11	0.220	0.280
C	–	5.08	–	0.200
D	0.38	0.51	0.015	0.020
F	0.76	1.52	0.030	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.83	0.030	0.072
J	0.20	0.38	0.008	0.015
K	3.18	–	0.125	–
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°

PLASTIC DIP 16-PIN "N" SUFFIX

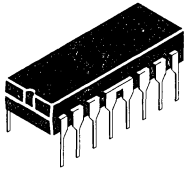


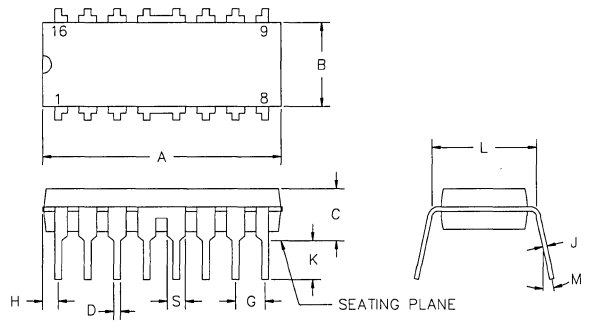


NOTES:
1. LEADS WITHIN 0.13mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1,8,9, AND 16
5. ROUNDED CORNERS OPTIONAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.54	19.94	0.730	0.785
B	6.10	6.60	0.240	0.260
C	–	5.08	–	0.200
D	0.38	0.51	0.015	0.020
F	0.76	1.52	0.030	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.83	0.030	0.072
J	0.20	0.38	0.008	0.015
K	3.18	–	0.125	–
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°

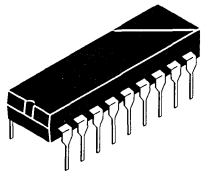
PLASTIC DIP BATWING 16-PIN "W" SUFFIX

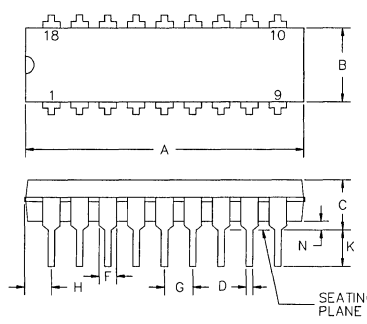




	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.54	19.94	0.730	0.785
B	6.10	6.60	0.240	0.260
C	–	5.08	–	0.200
D	0.38	0.64	0.015	0.025
G	2.54 BSC		0.100 BSC	
H	0.64	1.52	0.025	0.060
J	0.20	0.38	0.008	0.015
K	3.18	–	0.125	–
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
S	0.76	1.52	0.030	0.060

PLASTIC DIP
18-PIN
"N" SUFFIX

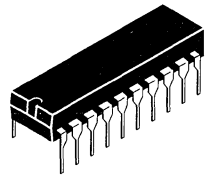


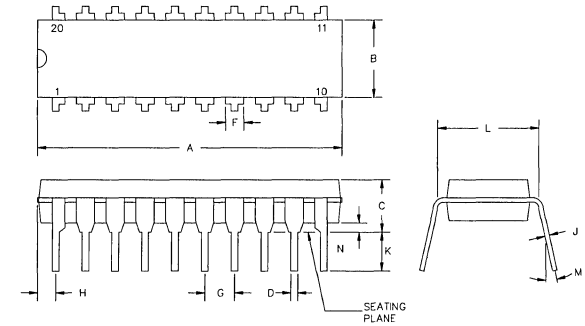


NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.61	23.11	0.890	0.910
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	3.18	–	0.125	–
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.38	0.64	0.015	0.025

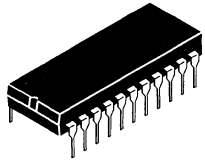
PLASTIC DIP
20-PIN
"N" SUFFIX

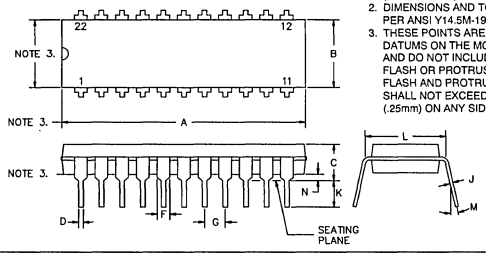




	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.91	26.42	1.020	1.040
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.38	0.53	0.015	0.021
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.36	0.008	0.014
K	3.18	–	0.125	–
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.38	0.64	0.015	0.025

PLASTIC DIP
22-PIN
"N" SUFFIX

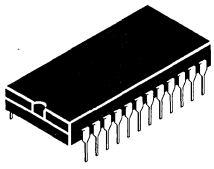


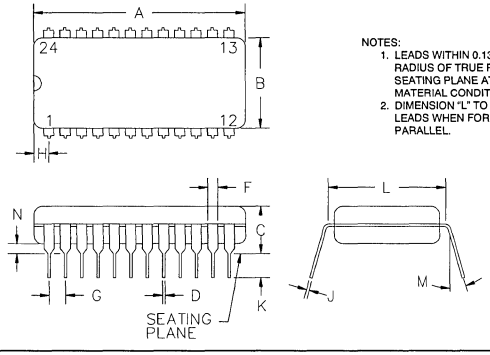


NOTES:
1. PACKAGE DIMENSIONS CONFORM TO JEDEC SPECIFICATION MS-010-AA FOR STANDARD DUAL IN-LINE (DIP) PACKAGE .400 INCH ROW SPACING (PLASTIC) 22 LEADS (ISSUE A, 7/85).
2. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M-1982.
3. THESE POINTS ARE REFERENCE DATUMS ON THE MOLDED BODY AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (.25mm) ON ANY SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.81	28.19	1.095	1.110
B	13.21	13.72	0.520	0.540
C	4.19	4.83	0.165	0.190
D	0.43	0.56	0.017	0.022
F	1.14	1.63	0.045	0.064
G	2.54 BSC		0.100 BSC	
J	0.25	0.035	0.010	0.015
K	3.05	3.51	0.120	0.138
L	10.16	10.72	0.400	0.422
M	–	15°	–	15°
N	0.51	0.89	0.020	0.035

PLASTIC DIP (WIDE)
24-PIN
"N" SUFFIX

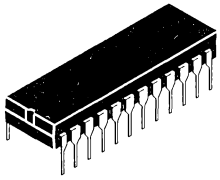


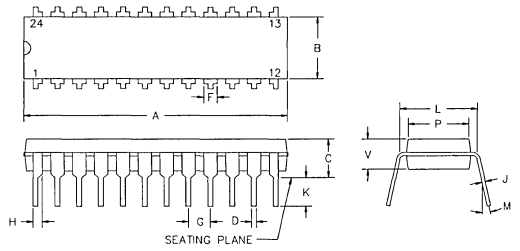


NOTES:
1. LEADS WITHIN 0.13mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	31.50	–	1.240
B	–	13.72	–	0.540
C	3.56	4.57	0.140	0.180
D	0.38	0.53	0.015	0.021
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.36	0.008	0.014
K	3.18	–	0.125	–
L	15.24 BSC		0.600 BSC	
M	–	15°	–	15°
N	0.38	0.64	0.015	0.025

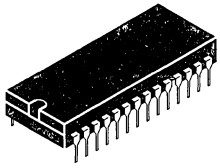
PLASTIC DIP (NARROW)
24-PIN
"N" SUFFIX

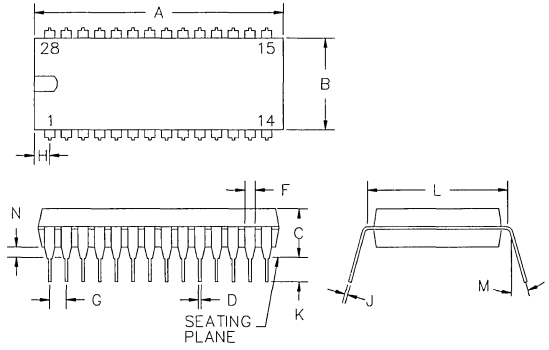




DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	29.21	29.85	1.150	1.175
B	6.10	6.86	0.240	0.270
C	–	5.08	–	0.200
D	0.38	0.51	0.015	0.020
F	0.76	1.52	0.030	0.060
G	2.54	BSC	0.100	BSC
H	0.76	1.52	0.030	0.060
J	0.20	0.38	0.008	0.015
K	3.18	–	0.125	–
L	7.62	BSC	0.300	BSC
M	–	15°	–	15°
P	6.35	6.60	0.250	0.260
V	3.05	3.56	0.120	0.140

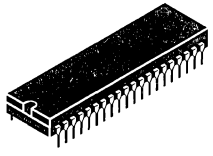
PLASTIC DIP
28-PIN
"N" SUFFIX

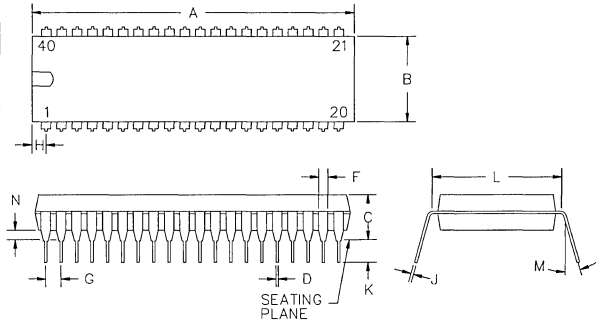




DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	34.54	35.56	1.360	1.440
B	12.70	13.21	0.500	0.520
C	–	5.08	–	0.200
D	0.38	0.56	0.015	0.022
F	0.76	1.52	0.0..0	0.060
G	2.54	BSC	0.100	BSC
H	0.76	1.78	0.030	0.070
J	0.20	0.38	0.008	0.015
K	3.18	–	0.125	–
L	15.24	BSC	0.600	BSC
M	–	15°	–	15°
N	0.51	–	0.020	–

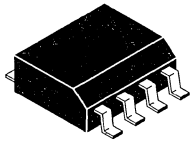
PLASTIC DIP
40-PIN
"N" SUFFIX

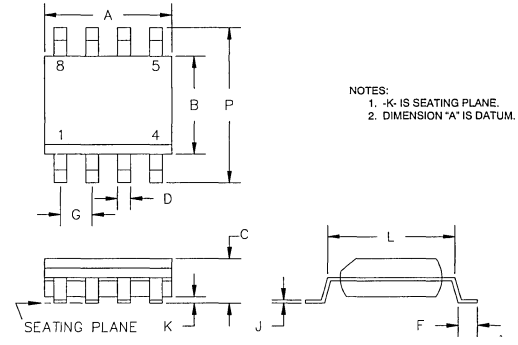




DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	–	53.09	–	2.090
B	13.46	14.22	0.530	0.560
C	–	5.08	–	0.200
D	0.38	0.56	0.015	0.022
F	0.76	1.52	0.030	0.060
G	2.54	BSC	0.100	BSC
H	1.40	2.41	0.055	0.095
J	0.20	0.38	0.008	0.015
K	3.18	–	0.125	–
L	15.24	BSC	0.600	BSC
M	–	15°	–	15°
N	0.51	–	0.020	–

PLASTIC S.O.I.C.
8-PIN
"DM" SUFFIX





NOTES:
1. -K- IS SEATING PLANE.
2. DIMENSION "A" IS DATUM.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	4.65	5.13	0.183	0.202
B	3.66	4.14	0.144	0.163
C	1.73	1.88	0.068	0.074
D	0.25	0.46	0.010	0.018
F	0.38	0.89	0.015	0.035
G	1.27	BSC	0.050	BSC
J	0.19	0.25	0.007	0.010
K	0.13	0.25	0.005	0.010
L	4.80	5.21	0.189	0.205
P	5.79	6.20	0.228	0.244

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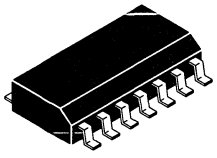
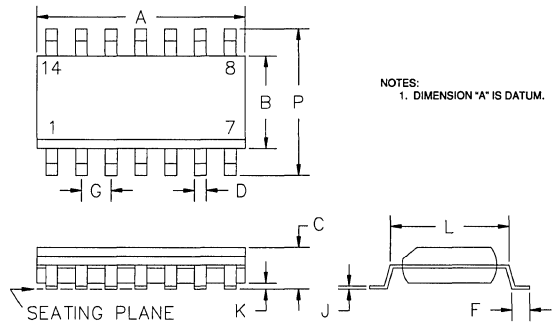
PLASTIC S.O.I.C.
14-PIN
"D" SUFFIX

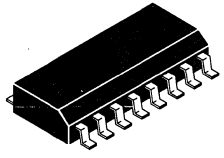


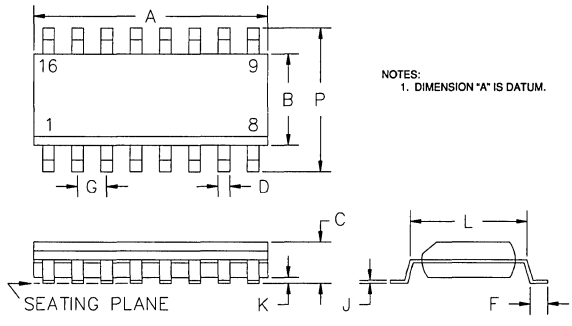


NOTES:
1. DIMENSION "A" IS DATUM.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.54	8.74	0.336	0.344
B	3.81	4.01	0.150	0.158
C	1.35	1.75	0.053	0.069
D	0.35	0.46	0.014	0.018
F	0.67	0.77	0.026	0.030
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.007	0.010
K	0.10	0.20	0.004	0.008
L	4.82	5.21	0.189	0.205
P	5.79	6.20	0.228	0.244

PLASTIC S.O.I.C.
16-PIN
"D" SUFFIX

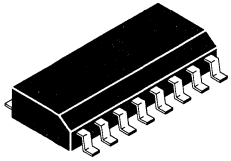


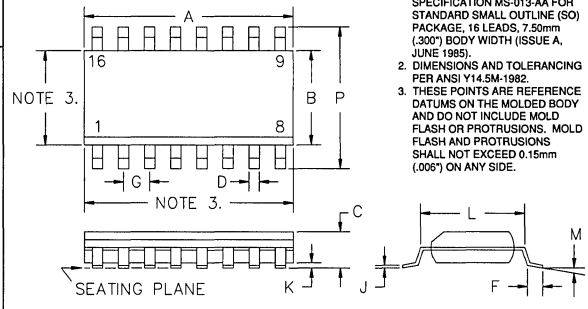


NOTES:
1. DIMENSION "A" IS DATUM.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.78	10.01	0.385	0.394
B	3.81	4.01	0.150	0.158
C	1.35	1.75	0.053	0.069
D	0.35	0.46	0.014	0.018
F	0.51	0.77	0.020	0.030
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.007	0.010
K	0.10	0.20	0.004	0.008
L	4.82	5.21	0.189	0.205
P	5.79	6.20	0.228	0.244

PLASTIC S.O.I.C.
16-PIN WIDEBODY
"DW" SUFFIX

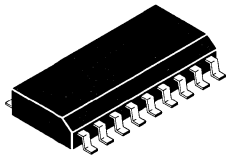


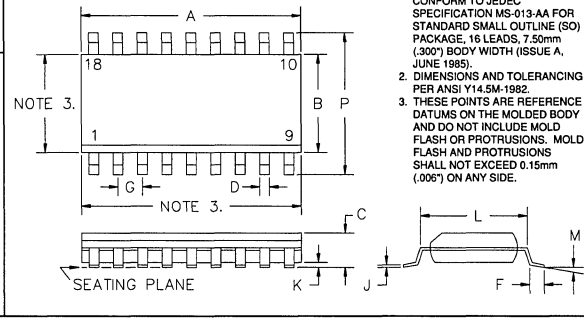


NOTES:
1. PACKAGE DIMENSIONS CONFORM TO JEDEC SPECIFICATION MS-013-AA FOR STANDARD SMALL OUTLINE (SO) PACKAGE, 16 LEADS, 7.50mm (.300") BODY WIDTH (ISSUE A, JUNE 1985).
2. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M-1982.
3. THESE POINTS ARE REFERENCE DATUMS ON THE MOLDED BODY AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.15mm (.006") ON ANY SIDE.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	10.67	–	0.420
B	7.49	7.75	0.295	0.305
C	2.35	2.65	0.093	0.104
D	0.25	0.46	0.010	0.018
F	0.64	0.89	0.025	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.10	0.30	0.004	0.012
L	8.13	8.64	0.320	0.340
M	0°	8°	0°	8°
P	10.26	10.65	0.404	0.419

PLASTIC S.O.I.C.
18-PIN WIDEBODY
"DW" SUFFIX





NOTES:
1. PACKAGE DIMENSIONS CONFORM TO JEDEC SPECIFICATION MS-013-AA FOR STANDARD SMALL OUTLINE (SO) PACKAGE, 16 LEADS, 7.50mm (.300") BODY WIDTH (ISSUE A, JUNE 1985).
2. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M-1982.
3. THESE POINTS ARE REFERENCE DATUMS ON THE MOLDED BODY AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.15mm (.006") ON ANY SIDE.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	13.21	–	0.520
B	7.49	7.75	0.295	0.305
C	2.35	2.65	0.093	0.104
D	0.25	0.46	0.010	0.018
F	0.64	0.89	0.025	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.10	0.30	0.004	0.012
L	8.13	8.64	0.320	0.340
M	0°	8°	0°	8°
P	10.26	10.65	0.404	0.419

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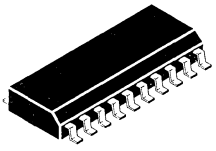
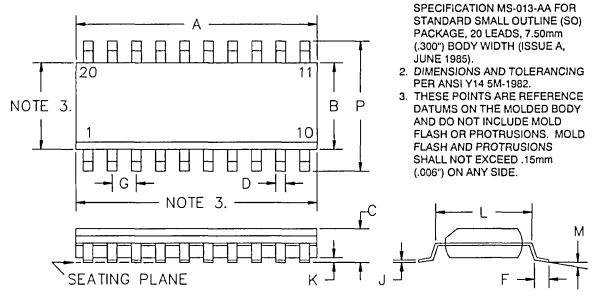
PLASTIC S.O.I.C.
20-PIN WIDEBODY
"DW" SUFFIX

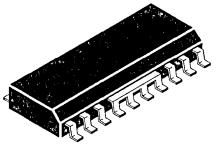


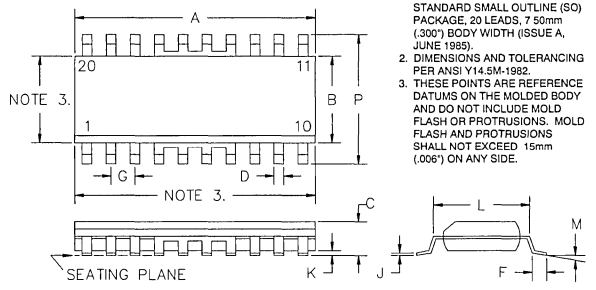


NOTES:
1. PACKAGE DIMENSIONS CONFORM TO JEDEC SPECIFICATION MS-013-AA FOR STANDARD SMALL OUTLINE (SO) PACKAGE, 20 LEADS, 7.50mm (.300") BODY WIDTH (ISSUE A, JUNE 1985).
2. DIMENSIONS AND TOLERANCING PER ANSI Y14 5M-1982.
3. THESE POINTS ARE REFERENCE DATUMS ON THE MOLDED BODY AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED .15mm (.006") ON ANY SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	13 21	–	0.520
B	7 49	7.75	0.295	0.305
C	2.35	2.65	0 093	0.104
D	0.25	0.46	0.010	0 018
F	0.64	0.89	0 025	0.035
G	1 27 BSC		0 050 BSC	
J	0 23	0 32	0 009	0.013
K	0.10	0.30	0 004	0.012
L	8.13	8.64	0.320	0 340
M	0°	8°	0°	8°
P	10 26	10.65	0.404	0 419

PLASTIC S.O.I.C. BATWING
20-PIN WIDEBODY
"DWW" SUFFIX

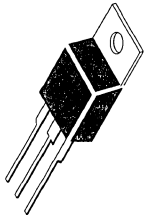


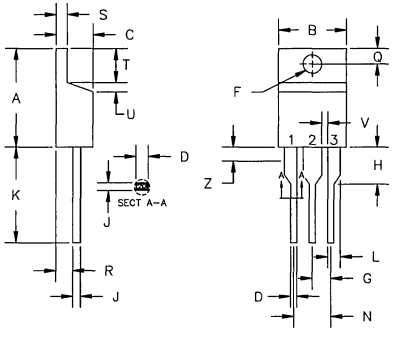


NOTES:
1. PACKAGE DIMENSIONS CONFORM TO JEDEC SPECIFICATION MS-013-AA FOR STANDARD SMALL OUTLINE (SO) PACKAGE, 20 LEADS, 7.50mm (.300") BODY WIDTH (ISSUE A, JUNE 1985).
2. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M-1982.
3. THESE POINTS ARE REFERENCE DATUMS ON THE MOLDED BODY AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED 15mm (.006") ON ANY SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	13.21	–	0.520
B	7.49	7.75	0.295	0.305
C	2.36	2.64	0.093	0.104
D	0.25	0.46	0.010	0.018
F	0.64	0.89	0.025	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.33	0.009	0.013
K	0.10	0.30	0.004	0.012
L	8.13	8.64	0.320	0.340
M	0°	8°	0°	8°
P	10.26	10.64	0.404	0.419

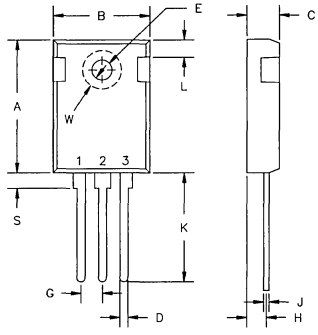
PLASTIC TO-220
3-PIN
"P" SUFFIX





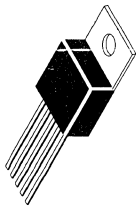
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.22	15.88	0.560	0.625
B	9.65	10.67	0.380	0.420
C	3.56	4.83	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.53	4.09	0.139	0.161
G	2.54 TYP		0.100 TYP	
H	–	6.35	–	0.250
J	0.30	1.14	0.012	0.045
K	12.70	14.73	0.500	0.580
L	1.14	1.27	0.045	0.050
N	5.08 TYP		0.200 TYP	
Q	2.54	3.05	0.100	0.120
R	2.03	2.92	0.080	0.115
S	1.14	1.40	0.045	0.055
T	5.84	6.86	0.230	0.270
U	0.508	1.14	0.020	0.045

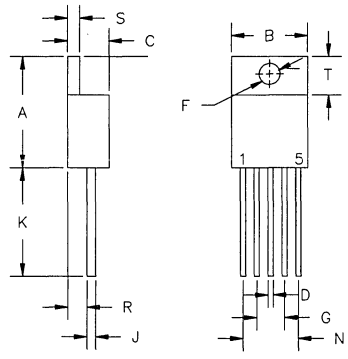
PLASTIC SIP TO-247
3-PIN
"V" SUFFIX



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.83	21.34	0.820	0.840
B	–	16.26	–	0.640
C	4.83	5.33	0.190	0.210
D	1.14	1.27	0.045	0.050
E	3.18	3.43	0.125	0.135
G	5.08BSC		0.200BSC	
H	–	2.79	–	0.110
J	0.51	0.71	0.020	0.028
K	12.70	20.07	0.500	0.790
L	3.05	3.56	0.120	0.140
S	3.81	4.32	0.150	0.170
W	–	3.43	–	0.135

PLASTIC TO-220
5-PIN
"P" SUFFIX

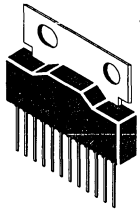


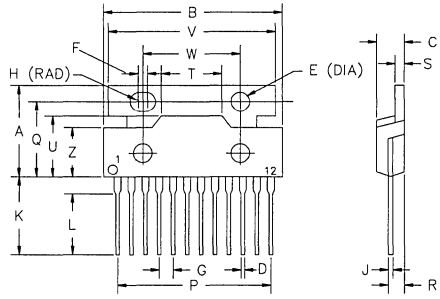


NOTES:
1. LEAD SPACING TOLERANCE IS NON-CUMLATIVE.
2. EACT BODY CONFIGURATION AT VENDOR'S OPTION WITHIN LIMITS SHOWN.
3. LEAD GUAGE PLANE IS 0.030" (0.76mm) MAX. BELOW SEATING PLANE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.23	16.51	0.560	0.650
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.46	0.89	0.018	0.035
F	3.56	4.06	0.140	0.160
G	3.40	–	0.134	–
J	0.31	1.14	0.012	0.045
K	12.70	14.73	0.500	0.580
N	6.80	TYP	0.268	TYP
R	2.04	2.92	0.080	0.115
S	1.14	1.39	0.045	0.055
T	5.85	6.85	0.230	0.270

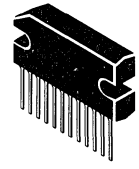
PLASTIC SIP
12-PIN
"ST" SUFFIX

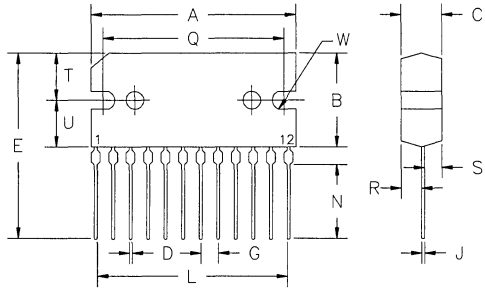




	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	13.97	14.48	0.550	0.570
B	29.97	30.99	1.180	1.220
C	3.30	3.81	0.130	0.150
D	0.55	0.66	0.022	0.026
E	3.48	3.73	0.137	0.147
F	0.46	0.56	0.018	0.022
G	2.54	TYP	0.100	TYP
H	1.78	TYP	0.070	TYP
J	0.20	0.30	0.008	0.012
K	7.62	12.70	0.300	0.500
L	7.62	8.64	0.300	0.340
P	–	27.94	–	1.100
Q	11.18	11.43	0.440	0.450
R	1.78	2.29	0.070	0.090
S	–	1.27	–	0.050
T	13.21	13.72	0.520	0.540
U	8.89	9.40	0.350	0.370
V	27.69	28.19	1.090	1.110
W	19.56	20.32	0.770	0.800
Z	7.37	7.87	0.290	0.310

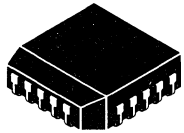
PLASTIC SIP
12-PIN
"S" SUFFIX

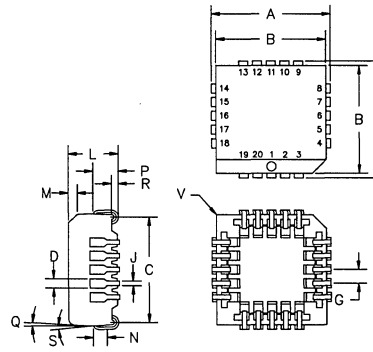




	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	29.46	30.23	1.160	1.190
B	13.59	14.35	0.535	0.565
C	4.32	5.08	0.170	0.200
D	0.56	0.66	0.022	0.026
E	21.59	–	0.850	–
G	2.54	TYP	0.100	TYP
J	0.36	0.46	0.014	0.018
L	–	27.94	–	1.100
N	6.10	6.86	0.240	0.270
Q	23.62	24.38	0.930	0.960
R	2.03	2.54	0.080	0.100
S	1.78	2.29	0.070	0.090
T	6.60	7.11	0.260	0.280
U	6.60	7.11	0.260	0.280
W	–	1.80	–	0.071

PLASTIC LEADED CHIP
CARRIER (PLCC)
20-PIN "Q" SUFFIX





	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.70	10.03	0.382	0.395
B	8.89	9.04	0.350	0.356
C	8.08	8.38	0.318	0.330
D	0.66	0.81	0.026	0.032
G	1.19	1.35	0.047	0.053
J	0.36	0.46	0.014	0.018
L	4.06	4.78	0.160	0.188
M	1.27		0.050	
N	1.52	–	0.060	–
P	2.41	–	0.095	–
Q	3°		3°	
R	0.63	1.14	0.025	0.045
S	3°		3°	
V	–	0.25	–	0.010

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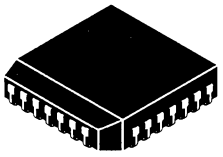
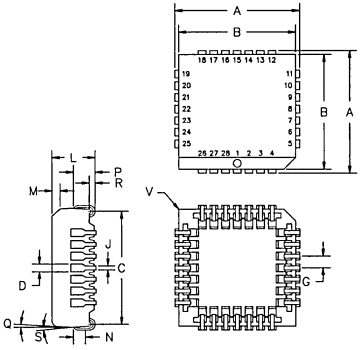
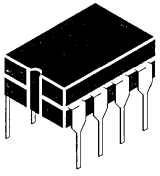
PLASTIC LEADED CHIP CARRIER (PLCC) 28-PIN "Q" SUFFIX

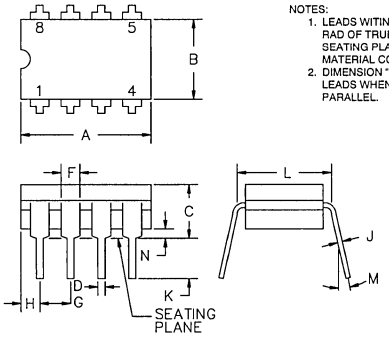




DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.19	12.70	0.480	0.500
B	11.43	11.56	0.450	0.455
C	10.54	10.92	0.415	0.430
D	0.64	0.89	0.025	0.035
G	1.27 TYP		0.050 TYP	
J	0.36	0.46	0.014	0.018
L	4.06	4.83	0.160	0.190
M	1.14	–	0.045	–
N	0.76	1.27	0.030	0.050
P	2.41	–	0.095	–
Q	3°	6°	3°	6°
R	0.63	1.14	0.025	0.045
S	3°	6°	3°	6°
V	–	0.25	–	0.010

CERAMIC MINI DIP 8-PIN "Y" SUFFIX

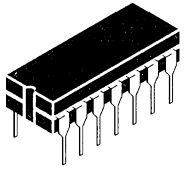


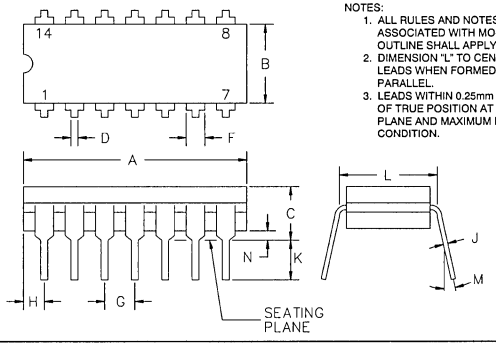


NOTES:
1. LEADS WITININ 0.13mm (0.005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.91	10.92	0.390	0.430
B	5.59	7.11	0.220	0.280
C	4.32	5.08	0.170	0.200
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.14	1.65	0.045	0.065
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

CERAMIC DIP 14-PIN "J" SUFFIX

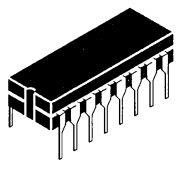


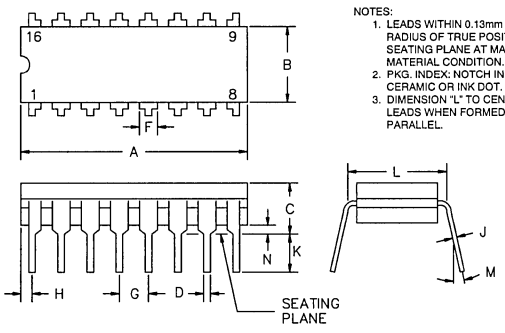


NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH MO-001 AA OUTLINE SHALL APPLY.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. LEADS WITHIN 0.25mm (0.010) DIA OF TRUE POSITION AT SEATING PLANE AND MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.80	19.94	0.740	0.785
B	5.59	7.11	0.220	0.280
C	–	5.08	–	0.200
D	0.381	0.51	0.015	0.020
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	–	2.03	–	0.080
J	0.203	0.381	0.008	0.015
K	2.54	–	0.100	–
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	0.76	0.020	0.030

CERAMIC DIP 16-PIN "J" SUFFIX

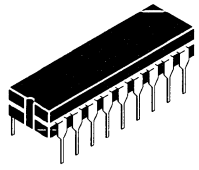


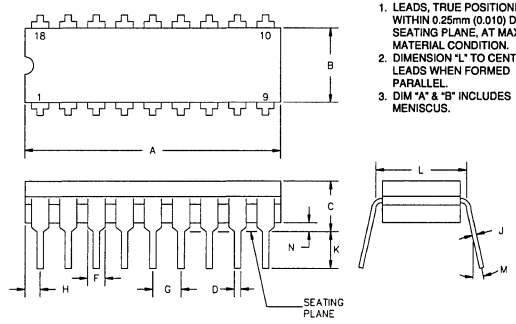


NOTES:
1. LEADS WITHIN 0.13mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PKG. INDEX: NOTCH IN LEAD IN CERAMIC OR INK DOT.
3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.80	19.94	0.740	0.785
B	5.59	7.11	0.220	0.280
C	–	5.08	–	0.200
D	0.38	0.51	0.015	0.020
F	0.76	1.77	0.030	0.070
G	2.54 BSC		0.100 BSC	
H	–	2.03	–	0.080
J	0.20	0.30	0.008	0.012
K	3.18	–	0.125	–
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	0.76	0.020	0.030

CERAMIC DIP
18-PIN
"J" SUFFIX

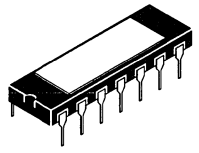


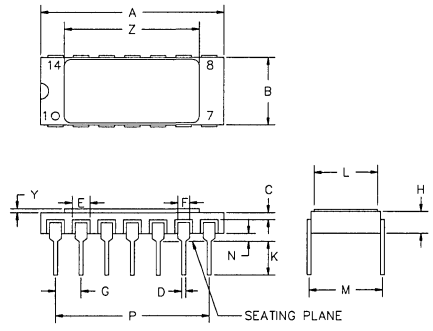


NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM "A" & "B" INCLUDES MENISCUS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	24.38	–	0.960
B	5.59	7.11	0.220	0.280
C	–	5.08	–	0.200
D	0.38	0.51	0.15	0.020
F	0.76	1.78	0.030	0.070
G	2.54 BSC		0.100 BSC	
H	–	2.03	–	0.080
J	0.20	0.30	0.008	0.012
K	3.18	5.08	0.125	0.200
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	0.76	0.020	0.030

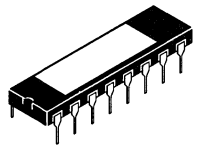
CERAMIC SIDE BRAZED (DIP)
14-PIN
"H" SUFFIX

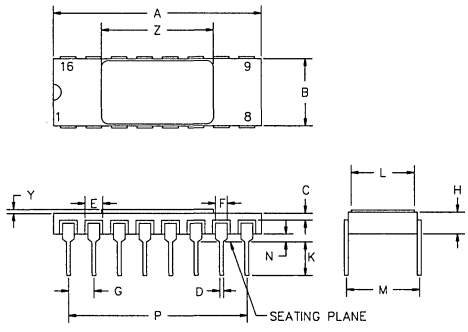




DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.54	19.81	0.730	0.780
B	7.11	8.13	0.280	0.320
C	0.18	–	0.007	–
D	0.38	0.53	0.015	0.021
E	1.78 TYP		0.070 TYP	
F	1.02	1.40	0.040	0.055
G	2.54 TYP		0.100 TYP	
H	1.78	3.05	0.070	0.120
K	3.18	–	0.125	–
L	–	7.37	–	0.290
M	7.11	8.13	0.280	0.320
N	0.64	1.14	0.025	0.045
P	15.00	15.49	0.590	0.610
Y	–	0.76	–	0.030
Z	11.81	12.32	0.465	0.485

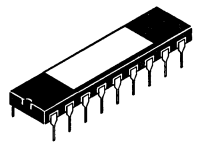
CERAMIC SIDE BRAZED (DIP)
16-PIN
"H" SUFFIX

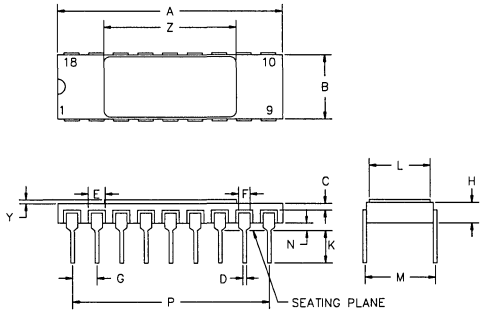




DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.81	20.32	0.780	0.800
B	7.11	8.13	0.280	0.320
C	0.18	–	0.007	–
D	0.38	0.53	0.015	0.021
E	1.78 TYP		0.070 TYP	
F	1.02	1.40	0.040	0.055
G	2.54 TYP		0.100 TYP	
H	1.78	3.05	0.070	0.120
K	3.18	–	0.125	–
L	–	7.37	–	0.290
M	7.11	8.13	0.280	0.320
N	0.64	1.14	0.025	0.045
P	17.53	18.03	0.690	0.710
Y	–	0.76	–	0.030
Z	11.81	12 32	0 465	0 485

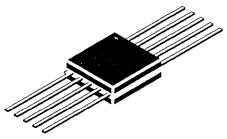
CERAMIC SIDE BRAZED (DIP)
18-PIN
"H" SUFFIX

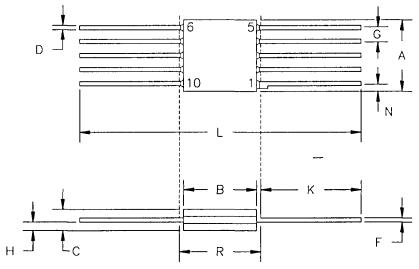




DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.35	23.37	0.880	0.920
B	7.11	8.13	0.280	0.320
C	0.18	–	0.007	–
D	0.38	0.53	0.015	0.021
E	1.78 TYP		0.070 TYP	
F	1.02	1.40	0.040	0.055
G	2.54 TYP		0.100 TYP	
H	1.78	3.05	0.070	0.120
K	3.18	–	0.125	–
L	–	7.37	–	0.290
M	7.11	8.13	0.280	0.320
N	0.64	1.14	0.025	0.045
P	20.07	20.57	0.790	0.810
Y	–	0.76	–	0.030
Z	11.81	12.32	0.465	0.485

CERAMIC FLATPACK 10-PIN "F" SUFFIX

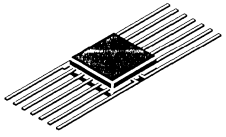


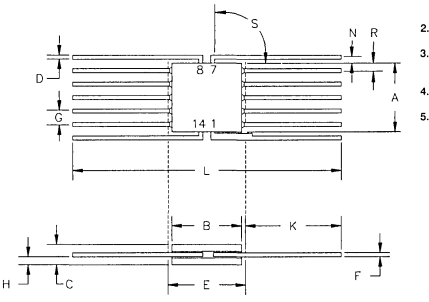


NOTES:
1. LEADS ARE WITHIN 0.13(0.005) RADIUS OF TRUE POSITION (TP) AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "G" DETERMINES A ZONE WITHIN WHICH ALL BODY AND LEAD IRREGULARITIES LIE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	7.37	–	0.290
B	6.04	6 40	0 238	0.252
C	1.45	1.70	0.057	0 067
D	0 25	0.483	0.010	0.019
F	0.076	0.153	0 003	0.006
G	1.27 BSC		0.050 BSC	
H	0.51	1.02	0.020	0.040
K	6 35	9.40	0.250	0.370
L	18.74	25.4	0.738	1.000
N	0.20	0.38	0.008	0 015
R	–	6.91	–	0.272

CERAMIC FLATPACK 14-PIN "F" SUFFIX

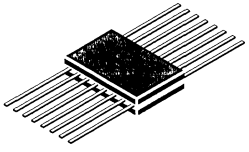


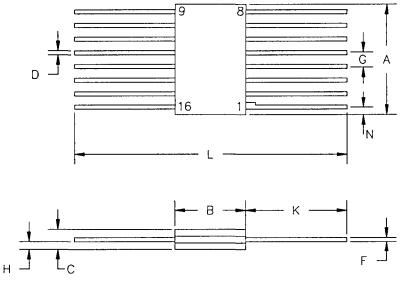


NOTES:
1. DIMENSION "E" ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN
2. DIMENSION "N" APPLIES TO LEADS 1, 7, 8, AND 14.
3. DIMENSION "H" IS MEASURED AT THE POINT OF EXIT OF THE LEAD FROM THE BODY.
4. DIMENSION "R" APPLIES TO ALL FOUR CORNERS.
5. DIMENSION "G" IS THE BASIC PIN SPACING BETWEEN CENTER LINES IN TWELVE POSITIONS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	7.11	–	0.280
B	6 10	6.40	0.240	0.252
C	1 45	1.70	0.057	0.067
D	0.25	0.48	0 010	0 019
F	–	6.91	–	0 277
F	0.08	0 15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0 51	1.02	0.020	0.040
K	6.35	9.40	0.250	0.370
L	19.0	25.4	0.750	1.000
N	0.10	–	0.004	–
R	0.13	–	0.005	–
S	30°	90°	30°	90°

CERAMIC FLATPACK 16-PIN "F" SUFFIX

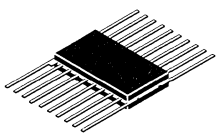


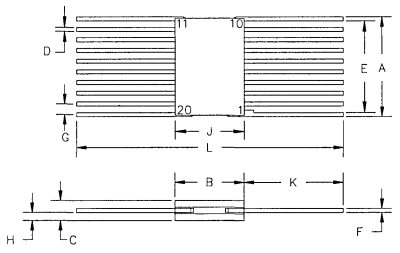


NOTES:
1. LEAD NO. 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
2. LEADS WITHIN 0.13mm(0.005) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	10.16	–	0.400
B	6.27	6.63	0.247	0.261
C	1.65	1.91	0.065	0.075
D	0.38	0.48	0.015	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.51	1.02	0.020	0.040
K	6.35	9.40	0.250	0 370
L	18.97	25.4	0.747	1.000
N	0.20	0.38	0.008	0.015

CERAMIC FLATPACK 20-PIN "SF" SUFFIX

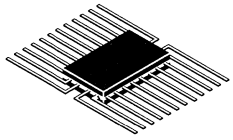


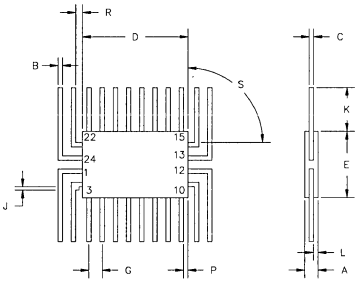


NOTES:
1. LEAD NO. 1 IS IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
2. DIMENSIONS "A" AND "J" ALLOW FOR OFF-CENTER LID, MENISCUS, AND GLASS OVERRUN.
3. THE TRUE-POSITION PIN SPACING IS LOCATED WITHIN ±0.005 INCH (0.127 mm).
4. DIMENSION "H" SHALL BE MEASURED AT THE POINT OF EXIT OF THE LEAD FROM THE BODY.
5. DIMENSION "G" EIGHTEEN SPACES.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	–	7.33	–	0 288
B	4 93	5 09	0.194	0 200
C	1.14	1.91	0.045	0 075
D	0.25	0.38	0.010	0.015
E	6.92	7 07	0 272	0.278
F	0 10	0.15	0.004	0 006
G	0 76 TYP		0 030 TYP	
H	0 50	0.64	0.020	0 025
J	–	5 34	–	0.210
K	6 74	7 38	0.265	0 290
L	18.42	19.85	0 724	0.780

CERAMIC FLAT PACK
24-PIN
"F" SUFFIX

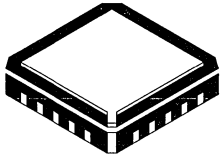


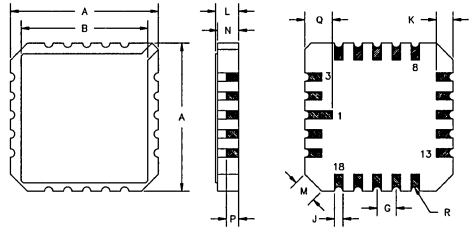


NOTES:
1. DIMENSION "L" SHALL BE MEASURED AT THE POINT OF EXIT OF THE LEAD FROM THE BODY.
2. DIMENSION "D" ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN.
3. THE BASIC PIN SPACING IS 0.050" (1.27mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN +/-0.005 (0.13mm) OF ITS EXACT LONGITUDINAL POSITION RELATIVE TO PINS 1 AND 24.
4. DIMENSION "P" APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 3, 10, 15, AND 22).
5. DIMENSION "R" APPLIES TO LEADS NUMBER 2, 11, 14, AND 23.
6. DIMENSION "S" APPLIES TO LEADS NUMBER 1, 2, 11, 12, 13, 14, 23, AND 24.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.650	1.900	0.065	0.075
B	0.380	0.480	0.015	0.019
C	0.080	0.150	0.003	0.006
D	–	11.18	–	0.440
E	6.27	6.63	0.247	0.261
G	1.27 BSC		0.050 BSC	
J	0.200	0.380	0.008	0.015
K	6.350	9.400	0.250	0.370
L	0.510	1.020	0.020	0.040
P	0.130	–	0.005	–
R	0.100	–	0.004	–
S	30°	90°	30°	90°

CERAMIC LEADLESS
CHIP CARRIER (LCC)
20-PIN
"L" SUFFIX

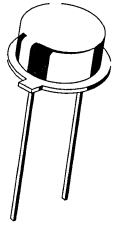


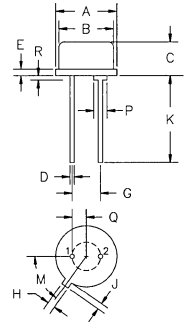


NOTES:
1. ALL EXPOSED METALLIZED AREA SHALL BE GOLD PLATED 60 MICRO-INCH MINIMUM THICKNESS OVER NICKEL PLATED UNLESS OTHERWISE SPECIFIED PURCHASE ORDER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.64	9.14	0.340	0.360
B	–	8.128	–	0.320
G	1.270 TYP		0.050 TYP	
J	0.635 TYP		0.025 TYP	
K	1.02	1.52	0.040	0.060
L	1.626	2.286	0.064	0.090
M	1.016 TYP		0.040 TYP	
N	1.372	1.68	0.054	0.066
P	–	1.168	–	0.046
Q	1.91	2.41	0.075	0.095
R	0.203R		0.008R	

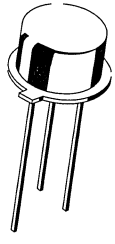
METAL CAN TO-46
2-PIN
"Z" SUFFIX

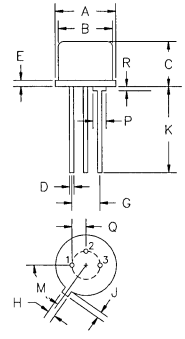




	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.207	5.842	0.205	0.230
B	4.521	4.953	0.178	0.195
C	–	2.667	–	0.105
D	0.406	0.533	0.016	0.021
E	–	0.381	–	0.015
G	2.54 BSC		0.100 BSC	
H	0.914	1.14	0.036	0.045
J	0.711	1.092	0.028	0.043
K	12.70	–	0.500	–
M	42°	48°	42°	48°
P	–	1.143	–	0.045
Q	1.27 TYP		0.050 TYP	
R	–	0.381	–	0.015

METAL CAN TO-52
3-PIN
"Z" SUFFIX





	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.207	5.842	0.205	0.230
B	4.521	4.953	0.178	0.195
C	–	4.064	–	0.160
D	0.406	0.533	0.016	0.021
E	–	0.381	–	0.015
G	2.54 BSC		0.100 BSC	
H	0.914	1.143	0.036	0.045
J	0.711	1.092	0.028	0.043
K	12.70	–	0.500	–
M	42°	48°	42°	48°
P	–	1.143	–	0.045
Q	1.27 TYP		0.050 TYP	
R	–	0.381	–	0.015

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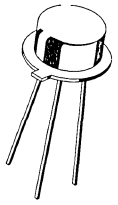
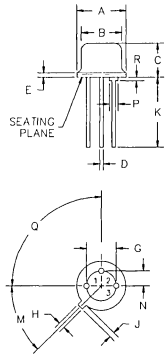
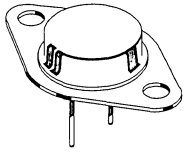
METAL CAN TO-39
3-PIN
"T" SUFFIX

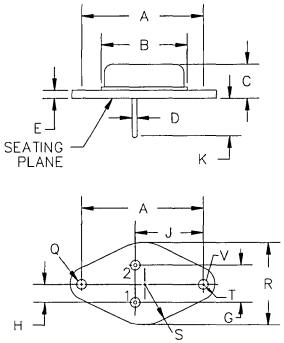




DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	4.19	4.70	0.165	0.185
D	0.406	0.533	0.016	0.021
E	–	1.02	–	0.040
G	5.08 TYP		0.200 TYP	
H	0.711	0.864	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	–	0.500	–
M	45° TYP		45° TYP	
N	2.54 TYP		0.100 TYP	
P	–	1.143	–	0.045
Q	90° TYP		90° TYP	
R	–	0.635	–	0.025

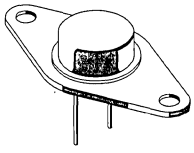
METAL CAN TO-3
3-TERMINAL
"K" SUFFIX

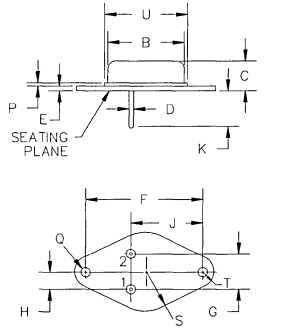




DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	29.90	30.40	1.177	1.197
B	19.43	19.68	0.765	0.775
C	6.35	9.40	0.250	0.370
D	0.97	1.09	0.038	0.043
E	1.52	3.43	0.060	0.135
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.14	0.655	0.675
K	10.16	12.70	0.400	0.500
Q	3.84	4.09	0.151	0.161
S	12.57	13.34	0.495	0.525
T	3.33R	4.78R	0.131R	0.188R

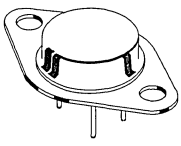
METAL CAN TO-66
3-TERMINAL
"R" SUFFIX

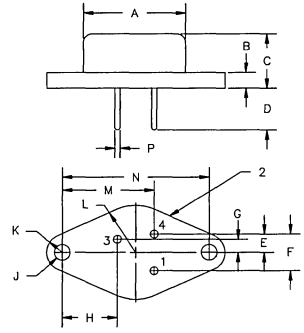




DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.36	2.72	0.093	0.107
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68R	–	0.145R
U	–	15.75	–	0.620

HYBRID METAL CAN (SM)
4-TERMINAL
"K" SUFFIX





DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	19.30	19.81	0.760	0.780
B	1.52	1.65	0.060	0.065
C	6.350	11.43	0.250	0.450
D	10.80	12.06	0.425	0.475
E	5.21	5.72	0.205	0.225
F	10.67	11.18	0.420	0.440
G	3.680	4.190	0.145	0.165
H	10.03	10.29	0.395	0.405
J	.396	.439	0.156	0.173
K	–	4.39R	–	0.173R
L	–	13.34	–	0.525
M	17.98	18.49	0.708	0.728
N	30.07	30.23	1.184	1.190
P	0.970	1.090	0.038	0.043

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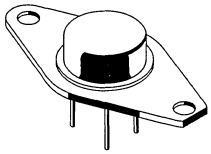
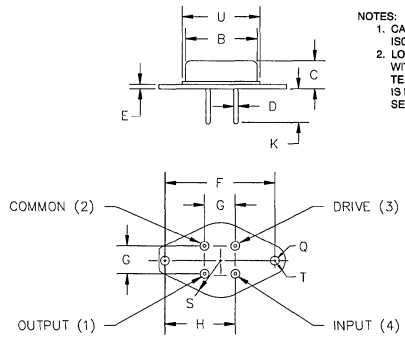
MECHANICAL DIMENSIONS

METAL CAN (SM) 4-PIN "R" SUFFIX

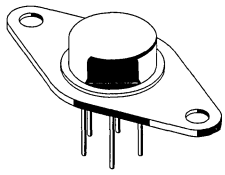


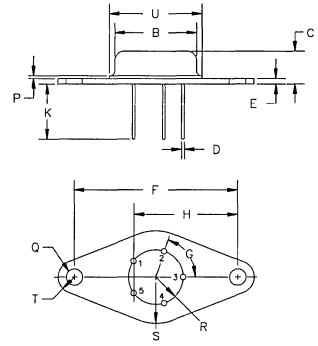


NOTES:
1. CASE IS ELECTRICALLY ISOLATED.
2. LOADS MAY BE SOLDERED TO WITHIN 1/16" OF BASE PROVIDED TEMPERATURE-TIME EXPOSURE IS LESS THAN 260 C FOR 10 SECONDS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.350	8.636	0.250	0.340
D	0.711	0.864	0.028	0.034
E	1.270	1.905	0.050	0.075
F	24.13	24.64	0.950	0.970
G	5.08	TYP	0.200	TYP
H	14.48	14.99	0.570	0.590
K	9.398	9.906	0.370	0.390
Q	3.607	3.861	0.142	0.152
S	–	8.89R	–	0.350R
T	–	3.68R	–	0.145R
U	–	15.75	–	0.620

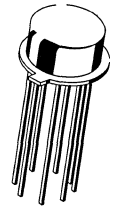
METAL CAN TO-66 5-PIN "R" SUFFIX

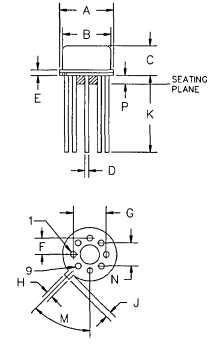




	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0 500
C	6 35	8 64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.90	0.050	0 075
F	24.33	24.43	0.958	0.962
G	72°	TYP	72°	TYP
H	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
R	–	4.11R	–	0.162R
S	–	8.89R	–	0.350R
T	–	3.68R	–	0.145R
U	–	15 75	–	0.620

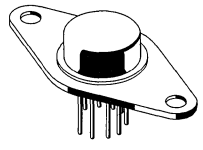
METAL CAN TO-99 8-PIN "T" SUFFIX

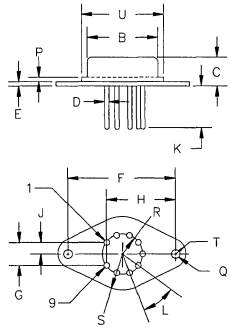




	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.509	9.398	0.335	0.370
B	7.772	8.509	0.306	0.335
C	4.191	4.699	0.165	0 185
D	0.406	0.533	0.016	0.021
E	–	1.016	–	0.040
F	2.54	TYP	0.100	TYP
G	5.08	TYP	0.200	TYP
H	0.711	0.864	0.028	0.034
J	0.737	1.14	0.029	0.045
K	12.70	14.48	0.500	0.570
M	45°	TYP	45°	TYP
N	3.556	4.064	0.140	0 160
P	0.254	1.016	0 010	0.040

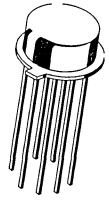
METAL CAN TO-66 9-PIN "R" SUFFIX

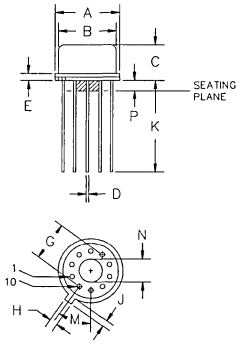




	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
B	11.94	12 70	0.470	0.500
C	6.35	8.636	0 250	0.340
D	0.711	0.863	0.028	0.034
E	1.270	1.905	0.050	0.075
F	24 33	24.43	0.958	0.962
G	4.826	5 334	0.190	0.210
H	14 47	14.99	0.570	0.590
J	2.362	2.718	0.093	0.107
K	9.14	–	0.360	–
L	36°	TYP	36°	TYP
P	–	1.270	–	0.050
Q	3.607	3.861	0.142	0.152
R	–	4.11R	–	0.162R
S	–	8.89R	–	0.350R
T	–	3.683R	–	0 145R
U	–	15.75	–	0.620

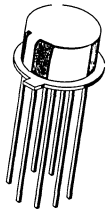
METAL CAN TO-100
10-PIN
"T" SUFFIX

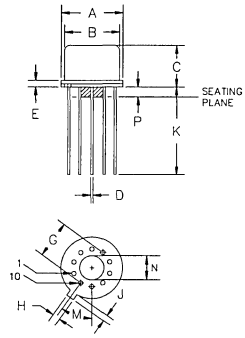




DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.890	9.398	0.350	0.370
B	8.001	8.509	0.315	0.335
C	4.191	4.699	0.165	0.185
D	0.406	0.533	0.016	0.021
E	–	1.016	–	0.040
G	5.842 TYP		0.230 TYP	
H	0.711	0.864	0.028	0.034
J	0.737	1.143	0.029	0.045
K	12.70	14.48	0.500	0.570
M	36° TYP		36° TYP	
N	3.556	4.064	0.140	0.160
P	0.254	1.016	0.010	0.040

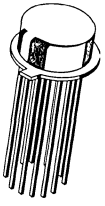
METAL CAN TO-96 (TALL)
10-PIN
"T" SUFFIX

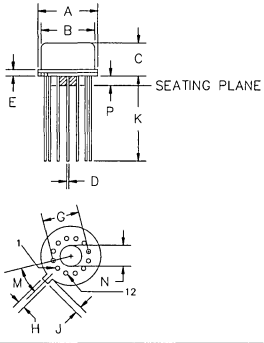




DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.890	9.398	0.350	0.370
B	8.001	8.509	0.315	0.335
C	6.096	6.604	0.240	0.260
D	0.406	0.533	0.016	0.021
E	–	1.106	–	0.040
G	5.842 TYP		0.230 TYP	
H	0.711	8.636	0.028	0.034
J	0.737	1.143	0.029	0.045
K	12.70	14.48	0.500	0.570
M	36° TYP		36° TYP	
N	3.556	4.064	0.140	0.160
P	0.254	1.016	0.010	0.040

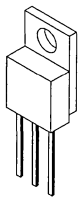
METAL CAN TO-101
12-PIN
"T" SUFFIX

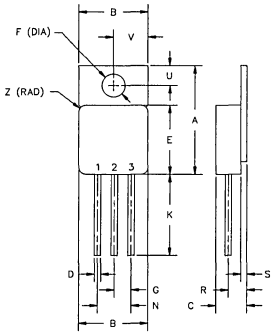




DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.509	9.398	0.335	0.370
B	8.001	8.509	0.315	0.335
C	4.191	4.699	0.165	0.185
D	0.406	0.533	0.016	0.021
E	–	1.016	–	0.040
G	5.842 TYP		0.230 TYP	
H	0.711	0.864	0.028	0.034
J	0.737	1.143	0.029	0.045
K	12.70	14.48	0.500	0.570
M	30° TYP		30° TYP	
N	3.556	4.064	0.140	0.160
P	0.254	1.016	0.010	0.040

HERMETIC TO-257
3-PIN ISOLATED
"IG" SUFFIX
3-PIN
"G" SUFFIX





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.38	16.64	0.645	0.655
B	10.41	10.67	0.410	0.420
C	4.70	4.95	0.185	0.195
D	0.71	0.81	0.028	0.032
E	10.41	10.67	0.410	0.420
F	3.56	3.81	0.140	0.150
G	2.54 TYP		0.100 TYP	
K	12.70	–	0.500	–
N	5.08 TYP		0.200 TYP	
R	2.92	3.18	0.115	0.125
S	0.89	1.43	0.035	0.045
U	2.87	3.12	0.113	0.123
V	5.13	5.38	0.202	0.212
Z	1.40 TYP		0.055 TYP	

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SELECTION GUIDE
APPLICATION NOTES

January 1990

THE SG1401 VIDEO AMPLIFIER

ABSTRACT

The SG1401-SG3401 has been designed to provide maximum versatility as a general-purpose, single-ended amplifier. With its broad frequency capability, this circuit will be useful in a wide range of applications provided that the usual considerations for high frequency circuit designs are observed. The following information is presented toward aiding in the optimization of the many possible configurations of this device.

FIXED GAIN

In the circuit configurations shown in Figure 1, the overall voltage gain is approximated by resistors R1 and the parallel combination of R2 and R3, as

$$Av \approx 1 + \frac{R_1}{R} \text{ ,where } R = \frac{R_2 R_3}{R_2 + R_3}$$

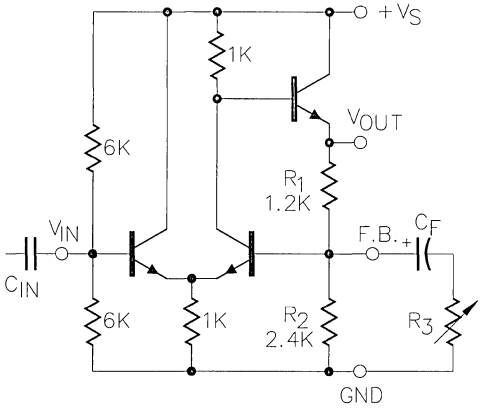

Figure 1.

With no external connections, the voltage gain is determined solely by R1 and R2 and is 1½ or 3 dB. Decreasing the effective value of R2 by capacitively coupling a lower resistor in parallel, raises the gain. Four fixed gain settings are provided internal to the circuit; however, any other setting within the maximum gain of the amplifier is possible with external resistors as shown in Figure 2.

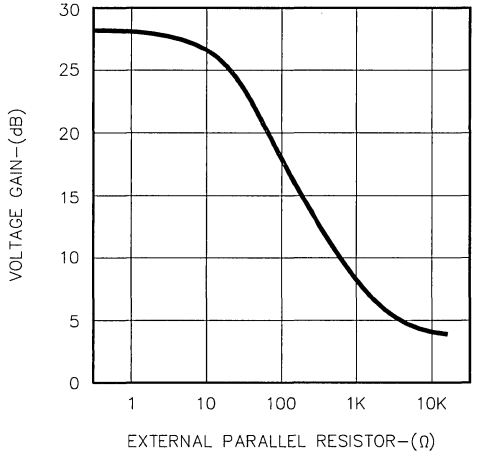

Figure 2. External Gain Control

The value of the coupling capacitor, C_F is determined by the low frequency response desired, as its capacitive reactance will add to the value of the resistance it couples. Therefore, the lower cutoff frequency will be

$$f_c \approx \frac{1}{2\pi R_3 C_F}$$

Utilizing the internal 90 or 460 ohm resistors for higher gain settings provides the added advantage of maximum temperature stability since the close tracking of adjacent diffused resistors keeps their ratio constant. Typical temperature variation of this circuit is shown below:

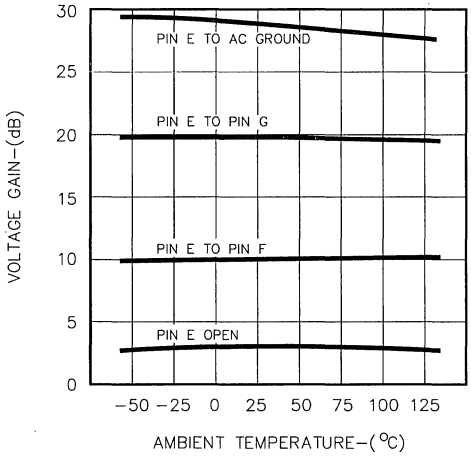

Figure 3. Temperature Stability

VARIABLE GAIN

Since the dynamic impedance of a forward-biased diode is inversely proportional to the current through it, a convenient gain control can be achieved by using a pair of diodes as a variable impedance. In the circuit of Figure 4, R3 has been replaced by two diodes whose impedances act in parallel due to the decoupling of C_D. If the diodes are driven from a voltage source, a logarithim relationship between gain and control signal is achieved (see Figure 5); while if a current source is used, the relationship is linear as shown in Figure 6.

There are two limitations on this form of gain control. First, the diodes' capacitance limits their effectiveness to frequencies below 20MHz and, secondly, the signal voltage across the diodes should be held to less than 50 mV RMS to minimize self-modulation of amplifier gain. Additionally, the AGC current should be limited to 3mA maximum to keep the diodes out of saturation.

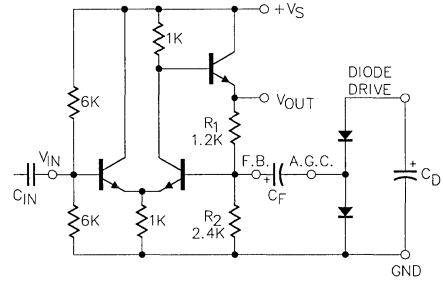

Figure 4.

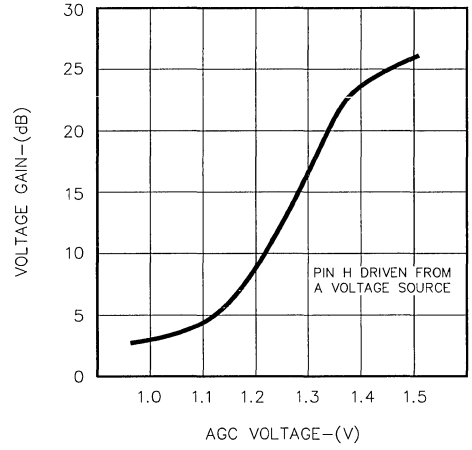

Figure 5. Gain vs. AGC Diode Voltage

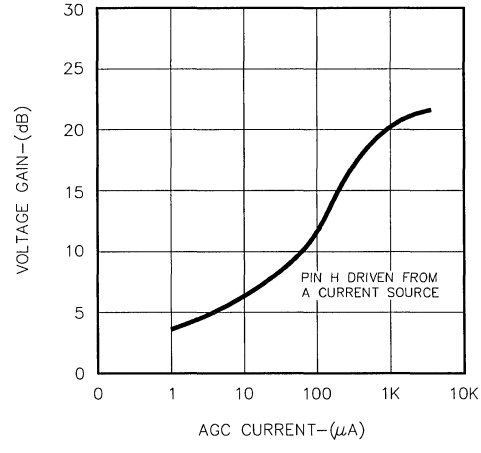

Figure 6. Gain vs. AGC Diode Current

HIGH FREQUENCY STABILITY

With the capability of operation at 100MHz, the SG1401-SG3401 also has some susceptibility to external stray reactances; however, with reasonable care, complete stability may be assured. Some general precautions which should be considered include the following:

1. Power supply decoupling close to the circuit terminals (a 0.1μF capacitor is usually adequate).
2. Maintain separation of input and output lines.
3. Minimize load capacitance or insert a series resistor (up to 50 ohms) in the output.
4. Purposely limit the high frequency response with a stabilizing capacitor C_S between pins 3 and 4.

Since the gain of this circuit is reduced by increasing the amount of feedback, the potential for instability is greatest when the gain is at its minimum value. This characteristic and the stabilizing effects of a 4.7 pF capacitor between pins 4 and 3 are illustrated in the frequency response curves presented in Figure 5 and 8. The relationship between the value of C_S and the upper cutoff frequency of a 20dB gain setting is shown in Figure 9 below.

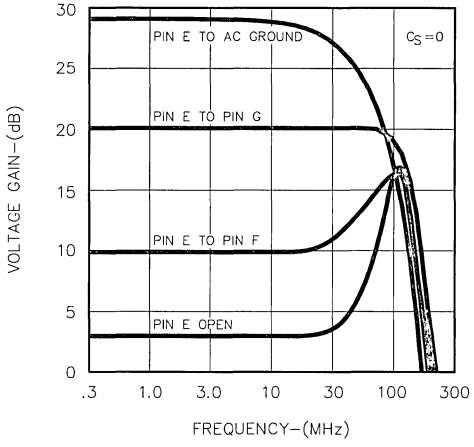

Figure 7. Frequency Response

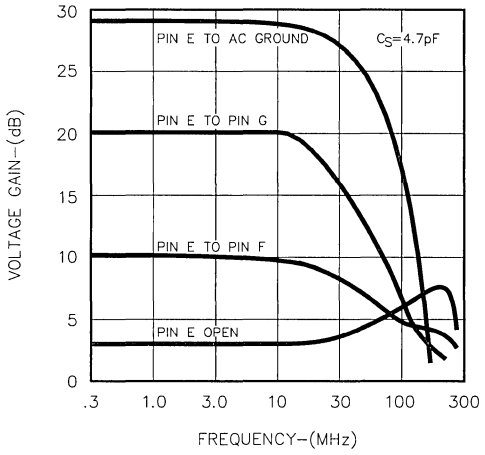

Figure 8. Frequency Response

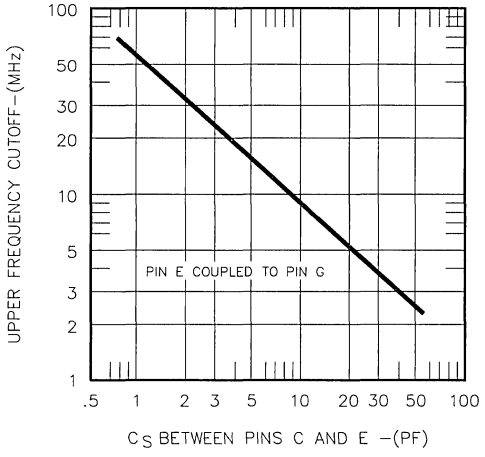

Figure 9. Upper Cutoff Frequency vs. C_S Value

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SG1402 WIDEBAND AMPLIFIER/MULTIPLIER

INTRODUCTION

Rapid advances in the state-of-the-art of processing monolithic linear integrated circuits have made the use of tightly matched components a practical reality. This in turn has opened the doors to a new class of circuit characterized by its utility, versatility, and ease of application. It is now possible to include on a monolithic chip, many of the components which, because of relatively poor tolerances, were formerly required to be external to the circuit. The SG1402, shown schematically in Figure 1, illustrates this capability both by its inclusion of all necessary biasing networks and by the nature of the circuit itself which requires extremely well matched component parameters for successful operation.

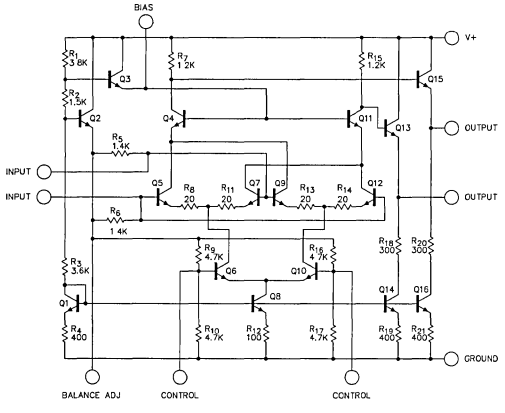

Figure 1. SG1402 Schematic Diagram

the way in which the above diff amps are cross-coupled will show that while the collector load resistors receive a portion of their current from each diff amp, the signals will arrive out of phase with respect to each other. This is because the input voltage, V_C, is amplified common emitter - with 180° phase shift - through Q9 and summed at resistor R7 with the signal which has gone common collector-common base - with 0° phase shift - through Q7 and Q5. Therefore, with the circuit perfectly balanced, the two signals completely cancel out and the output has zero signal. This can be shown mathematically as follows:

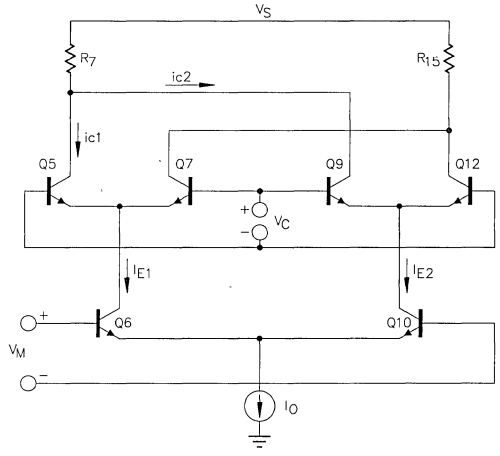

Figure 2. Simplified Schematic of the Multiplier Section of the SG1402

HOW IT WORKS

The heart of the SG1402 is a four quadrant multiplier consisting of two cross-coupled differential amplifiers which are jointly controlled by a third differential amplifier. This part of the circuit is shown in simplified form as Figure 2. The constant current, I_O, is divided by Q6 and Q10 and divided again by each of the upper diff amps such that, for balanced operation, transistors Q5, Q7, Q9, and Q12 each have ¼ I_O flowing through them. An examination of

The collector current in one side of a simple differential amplifier (Q5 and Q7, for example) is:

$$i_{C1} = \frac{I_{E1}}{1 + \exp\left(\frac{q}{kT}\right) V_M}$$

where: I_{E1} = sum of currents in each collector

$\frac{kT}{q}$ = 26 mV at 25°C

V_C = different input voltage

This equation can be differentiated to obtain the transconductance which, for small values of V_C, is:

$$gm = \frac{di_{C1}}{dv_C} = \frac{qI_{E1}}{4kT}$$

In a similar manner, the transconductance through Q9 is:

$$gm = \frac{di_{C1}}{dv_C} = \frac{qI_{E2}}{4kT}$$

and the total voltage gain, Av is:

$$Av = R_L \frac{di_{C1}}{dv_C} + \frac{di_{C2}}{dv_C}$$

$$= \frac{R_{Lq}}{4kT} (I_{E2} - I_{E1})$$

Since $I_{E1} + I_{E2} = I_O$, it can be seen that when $V_m = O$, $I_{E1} = I_{E2} = \frac{1}{2} I_O$ and Av = O. With I_{E1} and I_{E2} being collector currents of another differential amplifier, the total small-signal gain equation may be written:

$$Av = \frac{V_O}{V_C} = \frac{R_L I_O q}{4kT} \left[\frac{1}{1 + \exp\left(\frac{q}{kT}\right) V_M} - \frac{1}{1 + \exp\left(\frac{q}{-kT}\right) V_M} \right]$$

The circuit gain of the SG1402 is less than that predicted by the above equation due to the local feedback offered by the 20ohm emitter resistors. The actual relationship between Av and V_M is shown in Figure 3 while Figure 4 graphs the full four-quadrant transfer function between the input voltage, V_C, the control voltage, V_M, and the output voltage. Note that the 20ohm emitter resistors provide linearity for ±60 millivolts of input voltage while the modulating voltage is only linear for approximately half that value. It should be recognized from Figure 4 that output limiting occurs at a constant input voltage regardless of the modulating voltage. In other words, reducing the gain reduces the maximum peak-to-peak output swing.

BIASING CIRCUITRY

Key to the utility of the SG1402 is the inclusion of all the biasing and level shifting circuitry normally required as external components. This is provided by matched current sources and low impedance voltage sources.

Resistors R1, R2, R3 and R4 are directly across the supply voltage and establish a current:

$$I_B = \frac{V_S - V_{BEQ1}}{R1 + R2 + R3 + R4} = 1\text{mA at 10 volts}$$

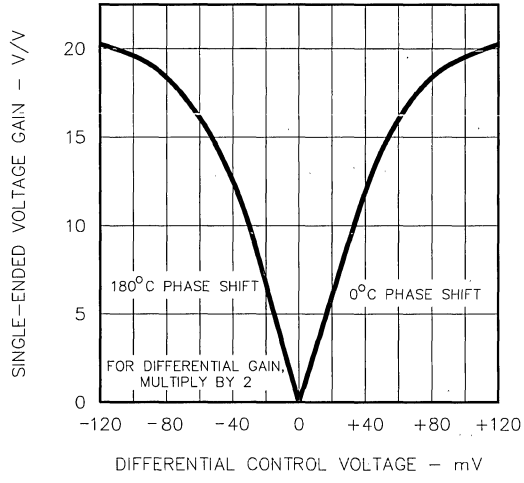

Figure 3. Differential Gain Control

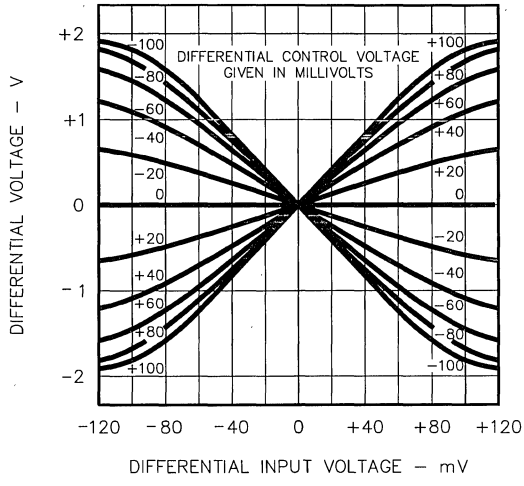

Figure 4. Multiplier Transfer Function

Transistors Q14 and Q16 have the same geometries and emitter resistors as Q1 and therefore, with the same base voltage, they each are also conducting one milliamp and provide the loads for the output emitter followers, Q13 and Q15. This saves chip area as a transistor requires less space than a resistor which would establish the same current.

Transistor Q8 has four times the emitter area and ¼ the emitter resistor as Q1 and thus defines a current level I_O of 4 milliamps.

The bias voltage levels required at different points in the circuit are all defined by the same resistors which set the current levels but

there is no mutual interaction due to the insertion of Q2 and Q3 which act as low-impedance isolators.

Transistors Q4 and Q11 serve only as common-base stages to isolate the load resistor from the collector capacitance of the parallel diff-amp transistors. Thus, frequency response is improved with only slight increase in circuit complexity.

VARIABLE GAIN AMPLIFICATION

The circuit of Figure 5 shows the simplest application of the SG1402 as a single-ended, variable-gain amplifier. The signals at the two outputs are always equal in magnitude and opposite in phase. As the gain control potentiometer is moved from one end to the other, each output will start with a maximum signal, reduce to a minimum when the pot is centered, and increase to maximum again in the opposite phase as the wiper gets to the other end of the potentiometer.

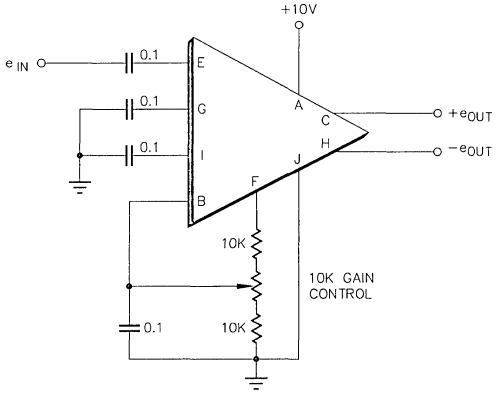

Figure 5. Single-Ended Variable-Gain Amplifier Configuration with Manual Control to provide Maximum Output of Either Phase.

For applications where a phase change is not desired, the incorporation of a diode as shown in Figure 6 will allow a DC control voltage to vary the input-output transfer function from a gain of +25dB to an attenuation of -25dB. This relationship is plotted in the graph of Figure 7.

Since this change in transfer function is accomplished with no net change in either operating currents or bias levels, it is transient-free and extremely fast-reacting. Thus, the circuit of Figure 6 may also be used as a gated amplifier with the control requirements compatible with 0 to 5 volt logic levels. The waveform in Figure 8 shows a 1MHz signal controlled with a 10 microsecond pulse.

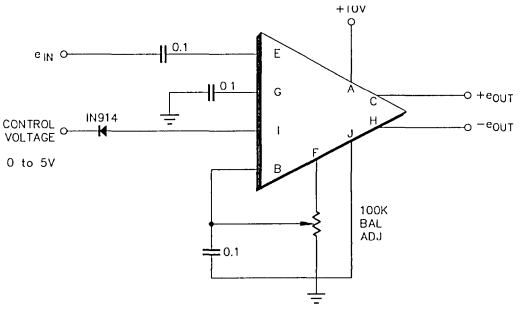

Figure 6. Addition of Diode Provides Gain Control Without Phase Change. Balance May Be Eliminated if Maximum Attentuation is not Required.

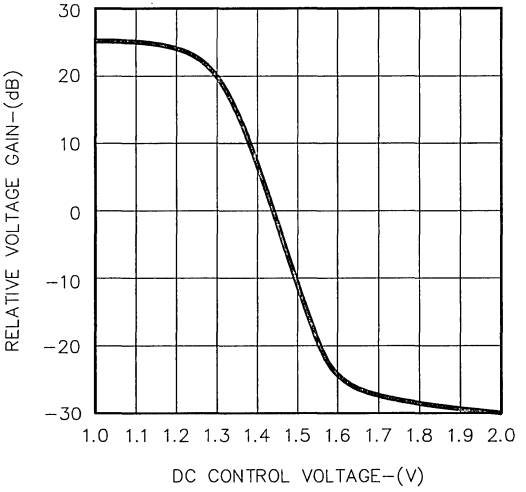

Figure 7. Gain Variation as a Function of Control Voltage with Diode Coupled Input.

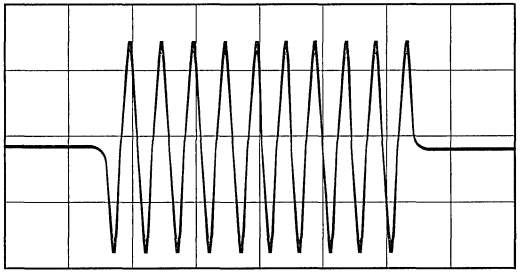

Figure 8. Gate Amplifier or Pulse Modulator Response. Input is 10 mVrms, 1 MHz and Control Voltage is 0 to 5 Volt Square Wave with f = 50 kHz.

MODULATION

The multiplying function of the SG1402 can be used to provide both balanced and amplitude modulation utilizing the basic circuit shown in Figure 9. With the potentiometer adjusted for optimum balance, the carrier signal is balanced out producing a double-sideband waveform at the output. Depending on the amplitude of the carrier signal, higher frequency harmonics can also be generated; however, if only the lower sideband is used, filtering of the upper sideband will also eliminate all the harmonics. It should be noted that this balanced modulation is achieved without the need for the usual transformers and only capacitive coupling is required. Typical waveforms are shown in Figure 10.

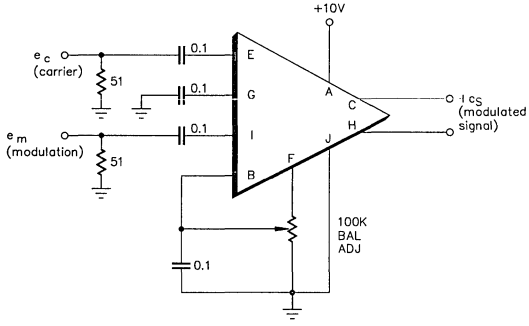

Figure 9. Balanced Modulator

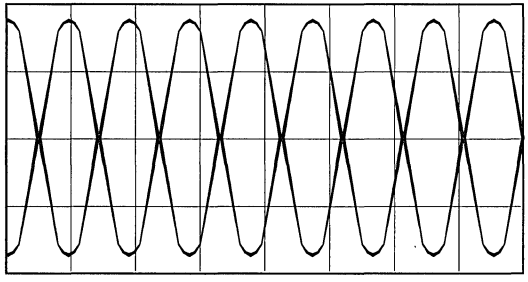

Figure 10. Balanced Modulator Output Waveform. (0.1V/cm, 50 μs/cm, f_C=1 MHz, f_M=10 KHz)

If the potentiometer is adjusted so that the circuit is unbalanced, then the carrier is included in the output signal and amplitude modulation as shown in Figure 11 results. The optimum adjustment can most readily be made while observing the output waveform on an oscilloscope. Care should be taken that neither signal overdrive the circuit.

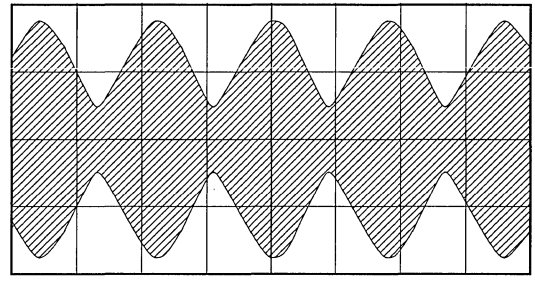

Figure 11. Amplitude Modulator Output Waveform. (0.2V/cm, 50 μs/div, f_C=1 MHz, f_M=10 KHz)

By using a signal to modulate itself with the circuit shown in Figure 12, the input is squared and since

$$\cos^2 \omega t = \tfrac{1}{2}(1 + \cos 2\omega t)$$

the output frequency is twice that of the input. Typical waveforms for this frequency doubler application are shown in Figure 13.

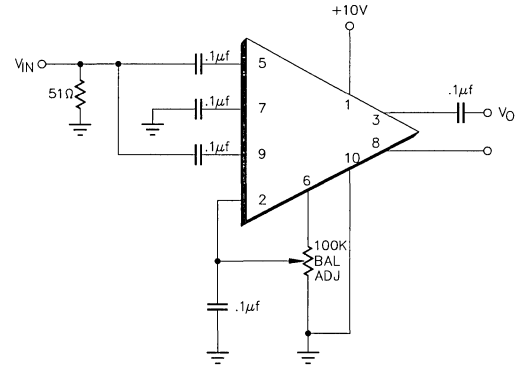

Figure 12. Frequency Doubler

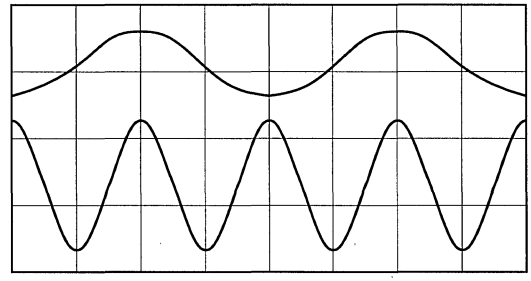

Figure 13. Frequency Doubler Input and Output Waveform. (50mV/cm, 0.2μs/div, f_1 = 1 MHz, f_2 = 2 MHz)

DEMODULATORS

The same features which make the SG1402 an excellent modulator provide superior performance when the circuit is used as a single or double sideband demodulator. The circuit of Figure 14 illustrates the simplicity of this application. The balance pot is not necessary since the inserted carrier is eliminated by the low-pass filter at the output.

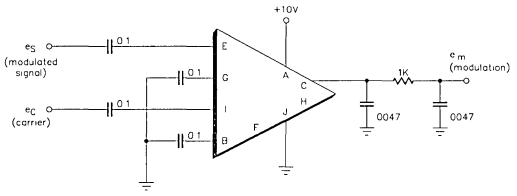

Figure 14. Balanced Demodulatoor

The same general approach may be used for amplitude modulation and a block diagram of a simple AM detector is shown in Figure 15. Thus, the SG1402 can be used in receivers which combine SSB and AM to provide complete signal transformation in either mode of operation.

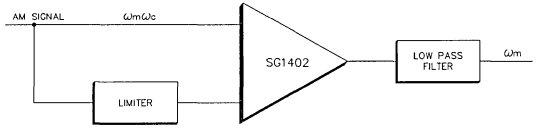

Figure 15. AM Detector Block Diagram

CONCLUSIONS

With the introduction of the SG1402, Silicon General has provided a powerful tool to the communications engineer and all others working with information processing. Because of its versatility and capability, this device opens the way to a much greater utilization of carrier transmission schemes for data handling in applications ranging from outer space to home kitchens.

SG1501A DUAL - POLARITY TRACKING REGULATORS

CIRCUIT OPERATION

The first IC to combine a positive and negative voltage regulator on a single chip was the SG1501, and this device has since been supplemented with three new tracking regulator designs - the SG1502, the SG1501A, and the SG1568.

All four of these tracking regulators operate in a similar manner which is best visualized through the block diagram shown in Figure 1. This circuit is fundamentally a tracking regulator. That is, the negative voltage is regulated and the positive output tracks the negative. (Note: In the SG1568, the circuit is reversed in that the negative side tracks the regulated positive output; however, the principle is the same.) Negative regulation is accomplished by providing a constant-voltage reference for the negative error amplifier, but the reference input to the positive error amplifier is grounded. This amplifier forces its other input, which is the center-tap between equal resistors, to also be at zero volts, thus requiring the positive output to be equal in magnitude but opposite in polarity to the negative output.

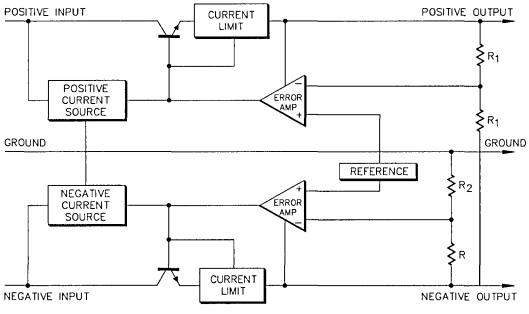

Figure 1. Block Diagram

With this technique, a single adjustment of the negative voltage divider - which changes the negative output level - will also provide exactly the same change to the positive output voltage. This tracking will hold all the way from approximately one volt above the reference voltage to a maximum value of about two volts less than the input supply voltage.

DESIGNER'S CHOICE

With four IC's to choose from some discussion of the significant features of each type is in order. Three of the devices, the SG1501A, the SG1501 and the SG1568 are factory set at ±15V regulators while the fourth, the SG1502, is user-adjusted to provide outputs from ±8V to ±28V.

The SG1501 and the SG1501A are interchangeable and both can be used by themselves to provide load currents to the maximum defined by package dissipation, or can be combined with external pass transistors for currents in excess of two amps. Both devices feature constant current limiting with the value set by external resistor. The SG1568 is similar in all respects to the SG1501 except that it is frequency compensated in a slightly different way.

The SG1502 uses the same basic circuit as the SG1501 but has two important differences. First, the voltage setting resistors are external to the device providing greater flexibility in adjusting the output voltage levels to other than ±15V. Secondly, the current limit circuitry has been changed to allow its use in a foldback mode. Foldback current limiting provides for a short circuit current value less than the maximum load current and is a significant feature when the major power dissipation is in external pass transistors rather than the IC.

Self-contained thermal shutdown is the primary improvement offered by the SG1501A although increases in both the maximum input voltage and load current have also been made. With thermal shutdown, temperature sensing circuitry on the chip is designed to turn off the output current when the junction temperature exceeds a safe limit - typically 170°C. The significance of this feature is that the designer now need not design around short-circuit power dissipation limits - the device will take care of itself. Since short-circuit power is typically more than twice as much as maximum operating power, this means a two-times, or better, improvement in load current is possible. It should be noted that even with thermal limiting circuitry, the maximum current must be controlled to allow time for this protection to react.

APPLICATIONS

The simplest way to use SG1501 and the SG1501A is in the basic circuit shown in Figure 2. In this form, the device will handle 50 to 100mA, depending on the heat sinking (more about this later) and will provide ±15V outputs with typically less than two millivolts of sensitivity to either line or load variations. Because of this excellent line regulation, there is no need for symmetrical input supply voltage levels. The only requirement is that each level be greater than its associated output and that the total voltage between positive and negative supplies be less than 60V (70V for the SG1501A). The minimum input voltage is defined by the regulator dropout characteristics shown in Figure 3.

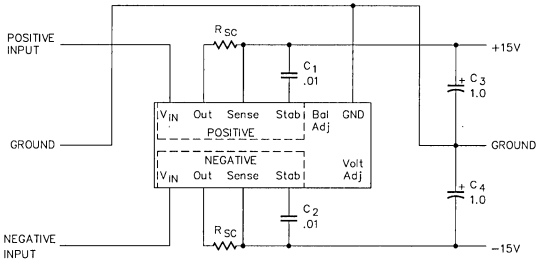

Figure 2. Basic ±15V, 50 mA Regulator

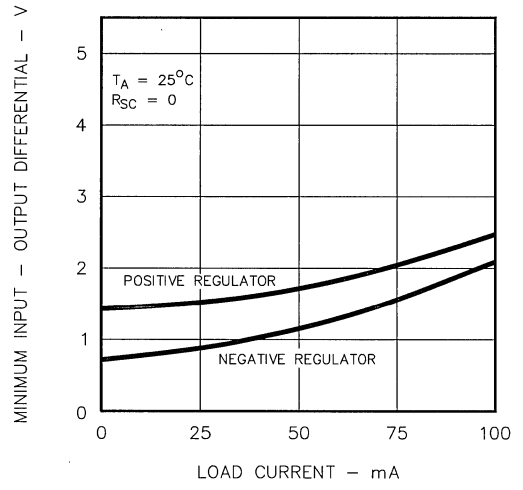

Figure 3. Regulator Dropout Voltage

When operating from a single voltage source, an ungrounded supply is required. An artificial ground can be provided as shown in Figure 4. In this circuit, the external transistors will conduct as necessary to accommodate unbalanced load requirements and while the outputs will float between the two input levels, they will be held constant with respect to this artificial ground.

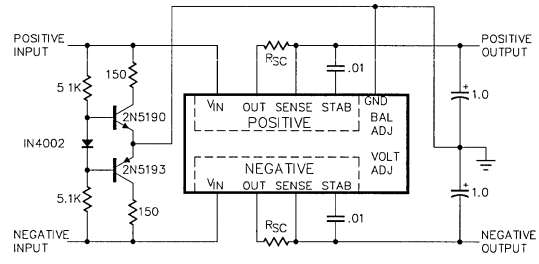

Figure 4. Artificial Ground for use with an Ungrounded or Single Level Voltage

CURRENT LIMITING

Current sensing is provided by transistors Q12 and Q13 (see schematic, Figure 5) which are normally held off by an external base-to-emitter resistor, Rsc. When the load current passing through this resistor develops enough voltage, the transistor turns on and diverts drive current away from the series pass transistors. The sense voltage is equal to approximately 0.6V at Tj = 25°C, but

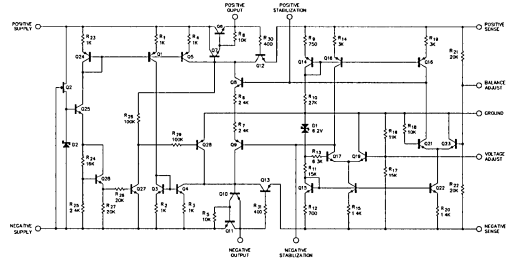

Figure 5. SG1501A Schematic Diagram

it is temperature dependent decreasing to 0.4V at 125°C as shown in Figure 6. Note that it is junction temperature that determines the sense level, and thus increasing the power dissipation within the circuit can lower the value at which limiting will occur. The value of the limiting resistor, Rsc, should be selected by:

$$Rsc = \frac{\text{Sense Voltage at Maximum Tj}}{\text{Allowable Short Circuit Current}}$$

where, for maximum regulation, the allowable short circuit current should be at least 20% more than the maximum expected load current.

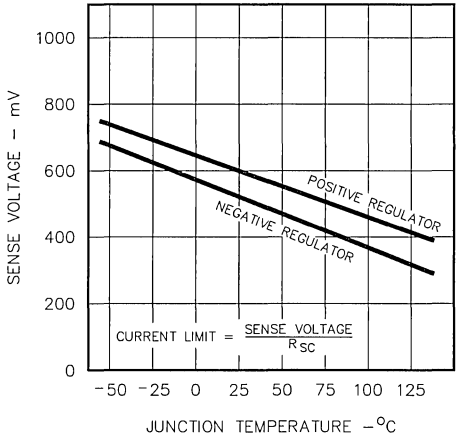

Figure 6. Current Limiting Characteristics

Under some conditions, a low-level oscillation may be present on the negative side when the device goes into current limiting. Should this be a problem, it may be eliminated by by-passing Rsc with a capacitor whose value is such that the time constant, Rsc C, is equal to 10 x 10^{-6} second. This capacitor, as well as the output capacitors, C3 and C4, must be low ESR types such as solid tantalum.

POWER CONSIDERATIONS

Although these dual regulators are designed to handle large load currents and high input voltages, the product of the two can easily exceed the maximum total device dissipation allowed by the package. The functional limitation which should be considered for each application is that for maximum reliability the junction temperature of the chip should not exceed 170°C. This is usually derated to give a maximum design operating Tj of 150°C.

To evaluate the maximum junction temperature possible in a given application, the following three parameters must be known:

1. The power dissipation within the chip
2. The thermal resistance from junction to ambient (or heat sink)
3. The ambient (or heat sink) temperature

The power dissipation within the chip is equal to the sum of the input voltage times the standby current plus the input-output voltage differential times the load current, for each side of the regulator. For example, the total power dissipation for ±20V inputs, ±15V outputs, and 50mA load currents is:

Pd = 20(2) + 20(3) + 5(50) + 5(50)
= 100mW standby + 500mW load current
= 600mW

The thermal resistance is the resistance to heat flow from the junction to the ultimate heat sink. For parts mounted in the open, still air, the thermal resistance (θjA) is equal to 185°C/watt for the T0-100 metal can and 125°C/watt for the T0-116 ceramic DIP. Blowing air across the package, or the use of some form of heat radiator can significantly reduce these numbers. For example, the use of IERC's model TXBF-032-025B top hat radiator on the T0-100 package, reduces θjA to 130°C/watt, while their model LIC-2144-2B radiator for the T0-116 will give an θjA of 50°C watt for that package. Finally, a perfect heat sink reduces θjA to θjC which is 50°C/watt for the T0-100 and 20°C/watt for the T0-116.

With the above information, the maximum power handling capability of the package can be determined as follows:

1. Calculate the maximum allowable junction temperature rise:
   $\Delta Tj = 150°C - T_A$ (max)
2. Calculate the power availability:
   Pd = DTj / θjA
3. From this number, subtract the maximum standby dissipation:
   Psb = (V + max)(Isb+) + (V - max)(Isb-)
4. The remainder can be used to determine the maximum load current as a function of input-output voltage differential.

The curves of Figure 7 show these relationships for each package under the assumptions of 25°C ambient, and symmetrical input and output voltages and load currents.

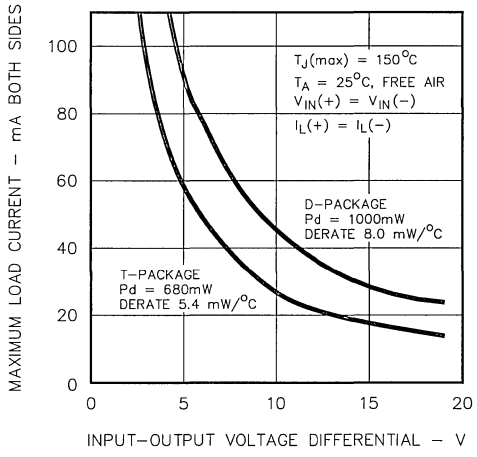

Figure 7. Maximum Current Capability

EXTERNAL POWER TRANSISTORS

Additional current handling capability may be provided through the use of external power transistors in the configuration shown in Figure 8. In this circuit, the 75ohm base-to-emitter resistors provide a path for the regular standby current and should not be increased in value. An additional consideration is the use of solid tantalum output capacitors as most common electrolytic types have too high an equivalent series resistance particularly at high frequencies.

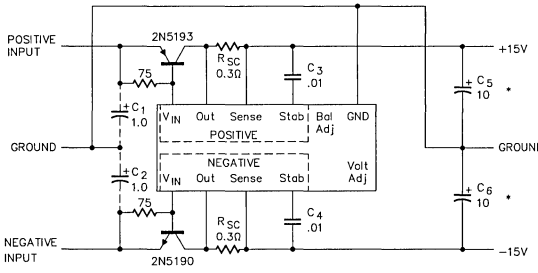

Figure 8. High Current Configuration, One Amp Output

The power transistors are not critical and can be selected on the basis of current and voltage capability, and on mechanical requirements for practical heat sinking. Note that only one transistor need be used if only one side has excessive load current. Although low-frequency devices will minimize the risk of oscillation, unique transistor characteristics may require a small capacitor (0.1μF) from base to ground or a larger value (5μF) from base to emitter for complete stability.

FOLDBACK CURRENT LIMITING

With constant-current limiting as shown in Figure 8, the power dissipation in the pass transistors under short circuit conditions can be substantial. Here, the thermal limiting feature of the SG1501A can't do much good since it senses the IC temperature rather than the external transistors. To eliminate the problem of having to heat sink a short circuit power two to three times normal operating levels, the use of the SG1502 in the circuit of Figure 9 should be considered. The dividers of R5 and R6 pre-bias the current limiting such that when the output is shorted, the maximum current is substantially reduced from its normal operating level. The values for R5 and R6 are most easily determined from an itterative solution of the equations below with the trade-off being that a greater amount of foldback requires a larger voltage drop across Rsc:

$$\text{Max Load Current} \approx \frac{\text{Sense Voltage} + \frac{R5}{R6} V_o}{Rsc}$$

$$\text{Short Circuit Current} \approx \frac{\text{Sense Voltage}}{Rsc}$$

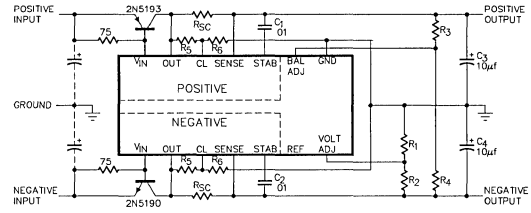

Figure 9. Foldback Current Limiting

VOLTAGE ADJUSTMENTS

With both output voltage levels internally set for 15V (±200mV for the SG1501/2501 and ±500mV for the SG3501) these devices require no additional resistors for many applications. It is possible, however, to externally vary the output voltages from ±10 to ±23V by using external resistors to shunt one or both of the internal resistors which set the negative output level. The positive output will, of course, track the negative value.

The simplest way of changing the output levels is to use a single resistor in parallel with R17 (see Figure 5) for voltages less than 15V and in parallel with R16 for voltages above 15V. The graph of Figure 10 shows the approximate value to use in either case.

This method of adjusting output levels has one disadvantage, however. Diffused resistors have a positive temperature coefficient and while they can be made to track each other extremely well, with one of them shunted this tracking becomes degraded. A method offering greater temperature stability is the use of a pair of resistors with values low enough to swamp out the internal divider. By shunting R16 with 1.2k, and R17 with a resistor selected by:

$$R17 = \frac{1.2(V_o - 6.2)}{62} \text{ k}\Omega$$

where Vo is the desired output voltage, a four-fold improvement in temperature performance is achieved at the expense of the additional divider current. Figure 11 shows that temperature variation which may be expected both with a single shunt resistor and with a divider drawing approximately five milliamps of current.

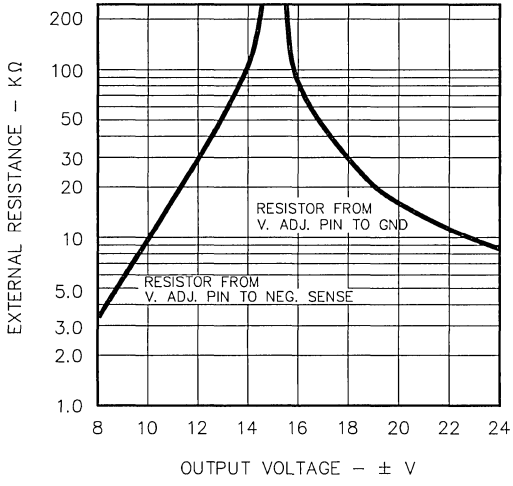

Figure 10. External parllel resistor required for voltages other than ±15V.

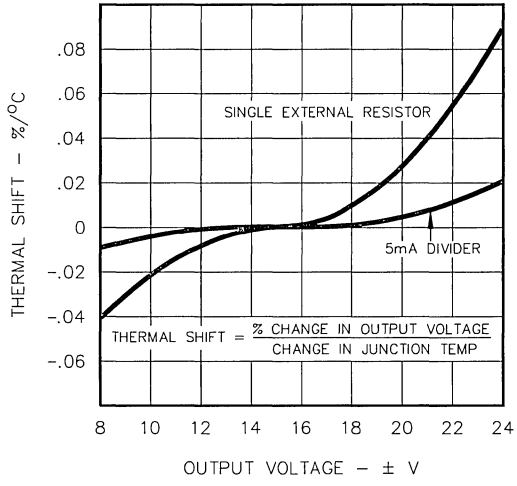

Figure 11. Temperature Coefficient of Output Voltage

Note that these temperature shifts are caused by changes in chip temperature which could result from variations of either ambient temperature or internal power dissipation.

In the 14 pin dual-in-line package, a connection is provided to the junction of R21 and R22. An external resistor divider can be used here in the same manner to either balance the two outputs so that they are exactly equal in magnitude or to unbalance them for non-symmetrical output levels.

Although all of these dual regulator types have provisions for adjustment of the output voltage levels, with its user-supplied voltage setting resistors, the SG1502 is the best choice for applications very far from ±15V. The divider resistors (see Figure 9) are selected as follows:

$$\text{Negative } V_o = \frac{6.2\ (R1+R2)}{R1}$$

$$\text{Positive } V_o = \frac{R3}{R4}\ (\text{Negative } V_o)$$

One common application for positive and negative voltages is as a power source for the widely used 710 and 711 IC voltage comparators. Since these devices are designed for +12 and -6V operation, it takes a circuit as shown in Figure 12 to get around the ±8 minimum output limitation of these regulators. Here, the nominal ±15V output of the SG1501 has been reduced to ±12V by the 2.0k and 1.8k voltage divider. Six volts are then subtracted from the negative output by the IN4735 zener diode. Because the diode is outside the feedback loop, some minor variations in the -6V output may be observed due to its temperature coefficient or dynamic impedance. These variations have negligible effect on the comparators, however, as the negative voltage is used only to bias high impedance current sources.

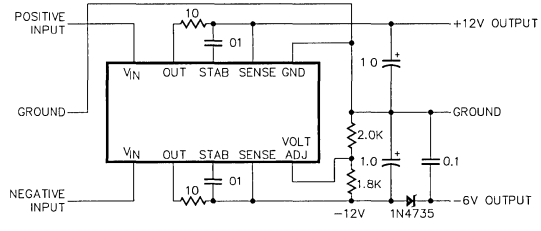

Figure 12. Using the SG 1501 to Provide +12 and -6 Outputs

Zener diodes can also be put to use in applications requiring high input voltages. In the circuit in Figure 13, the small signal zener diodes reduce the voltage applied to the IC while allowing the easily heat-sinked power transistors to absorb the added power dissipation caused by a large input-output differential.

12

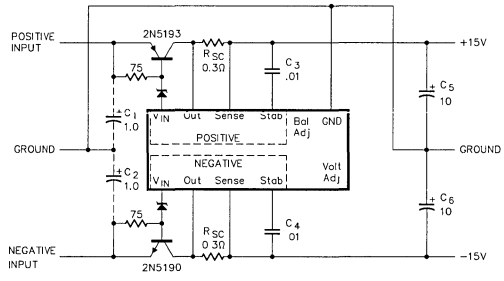

Figure 13. Zener Diodes Used to Prevent High Input Voltages from Appearing Across the Device.

CONCLUSIONS

With two complete regulators in a single IC, these new regulators offer an improved approach to power distribution. Their high degree of performance and freedom from large numbers of external components make "on-card," or distributed regulation a practical reality. By regulating at the point of use, the system designer has eliminated many knotty problems such as lead inductance, decoupling, line drop through connectors, etc. In addition, since each circuit card or module can now regulate its own voltage, complete interchangeability is more nearly assured and the problems of equipment maintenance are greatly eased.

SIMPLIFYING CONVERTER DESIGN WITH A NEW INTEGRATED REGULATING PULSE WIDTH MODULATOR

Edited by Stan Dendinger
Manager, Advanced Product Development
Silicon General, Inc.

ABSTRACT

A new monolithic integrated circuit is described which contains all the control circuitry for a regulating power supply converter or switching regulator. Included in this 16-pin dual-in-line package is the voltage reference, error amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches, and current limiting and shutdown circuitry. This device can be used for switching regulators of either polarity, transformer coupled DC to DC converters, transformer-less voltage doublers and polarity converters, as well as other power control applications.

INTRODUCTION

Implementing a switching power supply has just become significantly easier with the introduction of the SG1524 series of Regulating Pulse Width Modulator integrated circuits. Long recognized as offering greatly improved efficiencies, the development of switching supplies has been hampered by the complexity of the low-level circuitry required to provide the proper signals for adequate control of the switching transistors. As a result, these supplies have tended to be more costly, larger in size, and with proper reliability than could be justified by their improved efficiency. Even when threats of higher energy costs and potential brown-outs have made switching supplies mandatory, their complexity has made the engineering design task a formidable undertaking.

With the introduction of the SG1524, a major portion of the complex low-level control circuit has been integrated into a single LSI linear integrated circuit. This monolithic chip, packaged in a 16-pin dual-in-line outline, implements the entire block diagram shown in Figure 1.

It is the integration of all these different functions into a single IC that qualifies the SG1524 as one of the best examples to date of large scale integration as applied to analog circuits. The remainder of this paper will describe each of the individual blocks in the following diagram in considerable detail and then offer a few basic application suggestions.

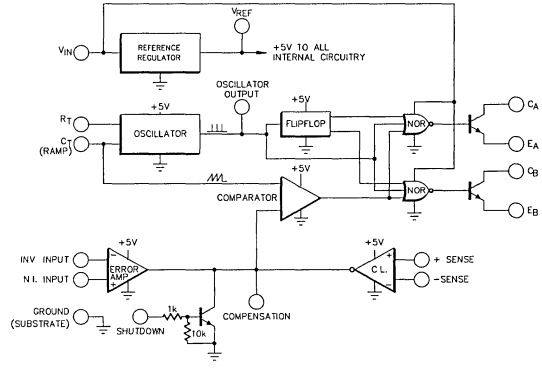

Figure 1. SG1524 Block Diagram

VOLTAGE REFERENCE

The reference circuit of the SG1524 is shown in Figure 2. This is a complete linear regulator designed to provide a constant 5 volt output with input voltage variations of 8 to 40 volts. It is internally compensated and short circuit protected. It is used both to generate a reference voltage and as the regulated source for all the internal timing and controlling circuitry. This regular may be bypassed for operation from a fixed 5 volt source by connecting pins 15 and 16 together to the input voltage. In this configuration,

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the maximum input voltage is 6 volts. While discussing input power, it should be mentioned that the entire SG1524 IC draws less than 10mA of current, regardless of input voltage.

This reference may be used as a 5 volt source for other circuitry. It will provide up to 20mA of output current itself and can easily be expanded to higher currents with an external PNP transistor as shown in Figure 3.

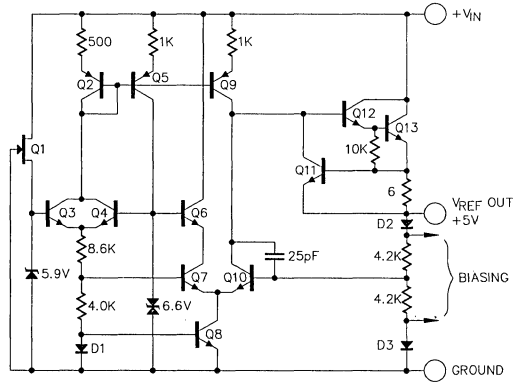

Figure 2. SG1524 Reference Circuit

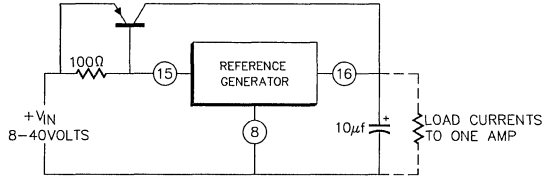

Figure 3. SG1524 Expanded Current Source

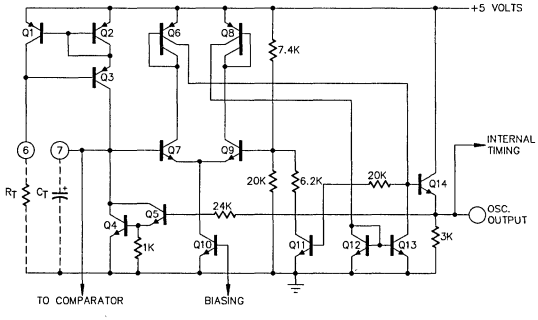

Figure 4. SG1524 Oscillator Circuit

OSCILLATOR

The oscillator in the SG1524 uses an external resistor (R_T) to establish a constant charging current into an external capacitor (C_T). This constant-current charging gives a linear ramp voltage which provides an overall linear relationship between error voltage and output pulse width. The SG1524 oscillator circuit is shown in Figure 4.

A second output from the oscillator is a narrow clock pulse which occurs each time C_T is discharged. This output pulse is used for several functions as outlined below:

1. As a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. The width of this blanking pulse can be controlled to some extent by the value selected for C_T.

2. As a trigger for an internal flip-flop which directs the PWM signal to alternate between the two outputs. Note that for single-ended applications, the two outputs can be connected in parallel and the frequency of the output is the frequency of the oscillator. For push-pull applications, the outputs are separated and the action of the flip-flop provides an output frequency ½ that of the oscillator.

3. As a convenient place to synchronize an oscilloscope for system de-bugging and maintenance.

4. As a bi-directional port for external timing synchronization. The output pulse from this oscillator - which is stable to within 2% over variations in both input voltage and temperature - can be used as a master clock for other circuitry, including other SG1524's. It thus follows that a positive pulse applied to this terminal can synchronize the SG1524 to an external clock signal.

The waveforms of the two outputs from the oscillator are shown in Figure 5.

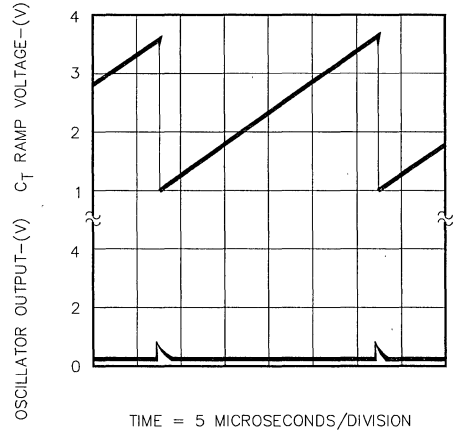

Figure 5. SG1524 Oscillator Waveforms

ERROR AMPLIFIER

The error amplifier circuit, shown in Figure 6, is a simple differential input, transconductance amplifier. Both inputs and the output are available for maximum versatility. The gain of the amplifier is nominally 10,000 (80dB) but can be easily reduced by either feedback or by shunting the output to ground with an external resistor. The overall frequency response of this amplifier which, by the way, is not internally compensated but yet is stable with unity gain feedback, is plotted with various values of external load resistance in FIgure 7.

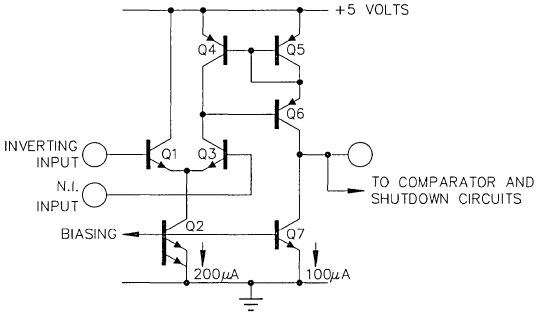

Figure 6. SG1524 Error Amplifier Schematic

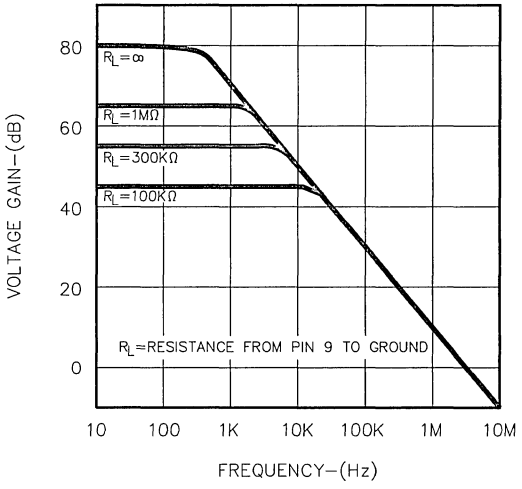

Figure 7. SG1524 Error Amp Frequency Esponse

Phase shifting to compensate for an output filter pole may readily be accomplished with an external series R-C combination at the output terminal of the amplifier.

Since the error amplifier is powered by the 5-volt reference voltage, the acceptable common-mode input voltage range is restricted to 1.8 to 3.4 volts. This means the reference must be divided down to be compatible with the amplifier input, but yet provides the advantage of being able to be used to regulate negative output voltages. Required input dividers are shown in Figure 8.

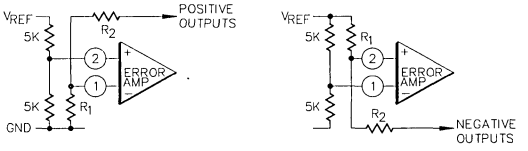

Figure 8. Error Amplifier Connections

Since this amplifier is a transconductance design, the output is a very high impedance (approximately 5MΩ) and can source or sink only 100μA. This makes the output terminal (Pin 9) a very convenient place to insert any programming signal which is to override the error amplifier. Internal shutdown and current limit circuits are connected here, but any other circuit which can sink 100μA can pull this point to ground, thereby shutting off both outputs.

For example, the soft start circuit of Figure 9 can be used to hold Pin 9 to ground - and thus both outputs off - when power is first applied. As the capacitor charges, the output pulse slowly increases from zero to the point where the feedback loop takes control. The diode then isolates this turn-on circuit from whatever frequency stabilizing network might also be connected to Pin 9.

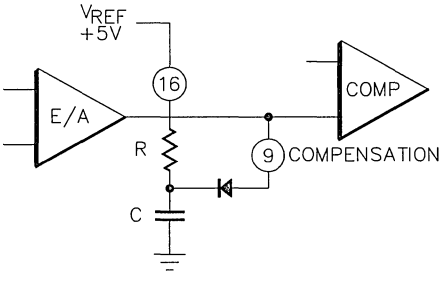

Figure 9. SG1524 Soft Start Circuitry

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CURRENT LIMITING

The current limiting circuit, while shown in the block diagram as op amp, is really only a single transistor amplifier as shown in Figure 10. It is frequency compensated and has a second transistor to provide temperature compensation and a reduction of input threshold to 200mV. When this threshold is exceeded, the amplifying transistor turns on and, by pulling the output of the error amplifier toward ground, linearly decreases the output pulse width.

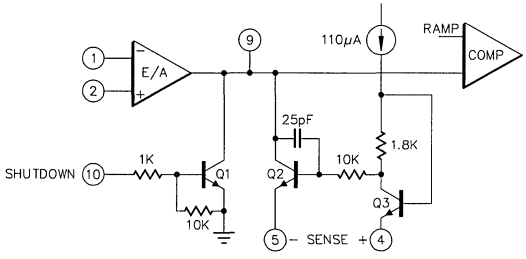


Figure 10. SG1524 Current Limiting

One consideration in using this circuit is that the sense terminals have a ± 0.3 volt common mode range which requires sensing in the ground line. However, since differential inputs are available, foldback current limiting can be implemented as shown in Figure 11.

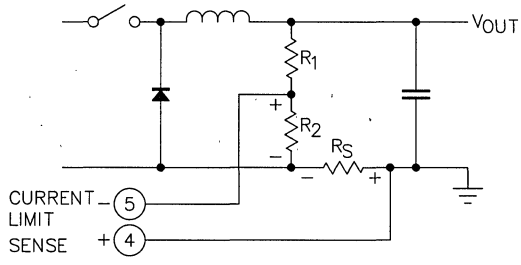


Figure 11. Foldback Current Limiting

While on the subject of protection circuitry, although overvoltage protection is not built into the SG1524, it is relatively easy to add by using the internal shutdown circuit in conjunction with a few external components as shown in Figure 12.

This circuit will provide a low level sensing and latching function and while it won't protect against a shorted output transistor, it will remove the drive signals with no power dissipation.

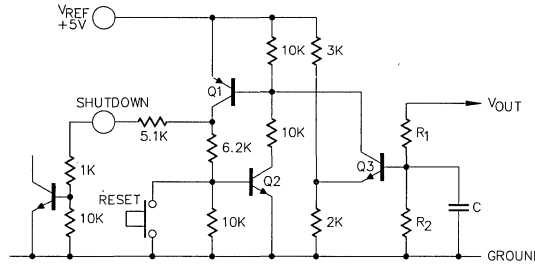


Figure 12. SG1524 Over Voltage Protection

OUTPUT STAGES

The outputs of the SG1524 are two identical NPN transistors with both collectors and emitters uncommitted. These circuits are as shown in Figure 13 and include an antisaturation network for fast response and current limiting set for a output current of approximately 100mA.

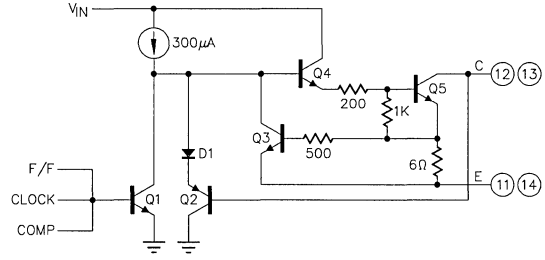


Figure 13. SG1524 Output Stage

The availability of both collectors and emitters allows a maximum versatility to enable driving either NPN or PNP external transistors; however, it must be remembered that this is only a switch which closes and opens. Power transistor turn-off drive must be developed externally. Some suggestions for output drive circuits are shown in Figure 14.

APPLICATIONS

In considering applications for the SG1524, it appears that there are three general classifications of switching power supply systems. Included in the first are the transformerless voltage multiplier circuits shown in Figure 15. These circuits are primarily used for low level applications but can step up, step down, or change the polarity of an input voltage. The switches shown can be either

the output stages of the SG1524 or external transistors. Note that one extra diode is required to protect the emitter-base junction of switch S_A during the times when both switches are open.

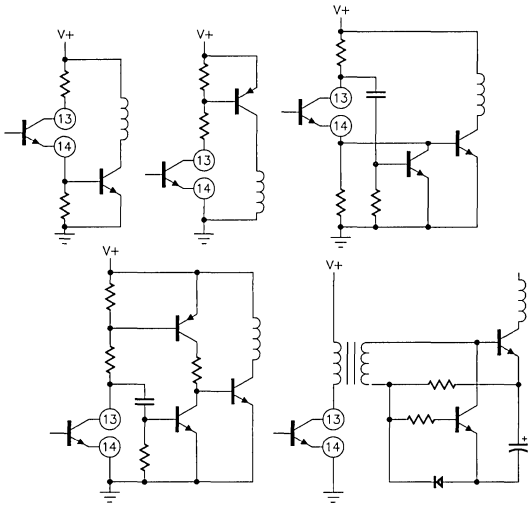


Figure 14. Driving External Transistors

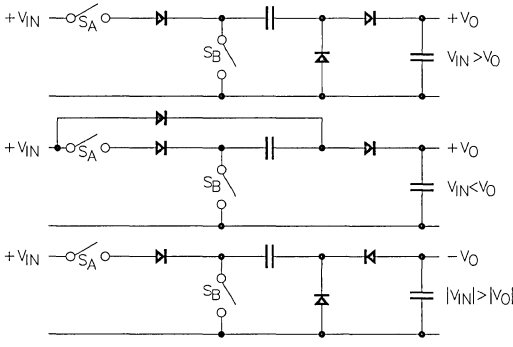


Figure 15. Capacitor/Diode Output Circuits

For higher current applications, the single-ended inductor circuits of Figure 16 represent another classification. Here, the two outputs of the SG1524 are connected in parallel, but note that this does not give twice the current as the switches are alternating internally. This does not affect external performance, however, and the SG1524 can be used to provide 0-90% duty cycle modulation in any of the configurations shown.

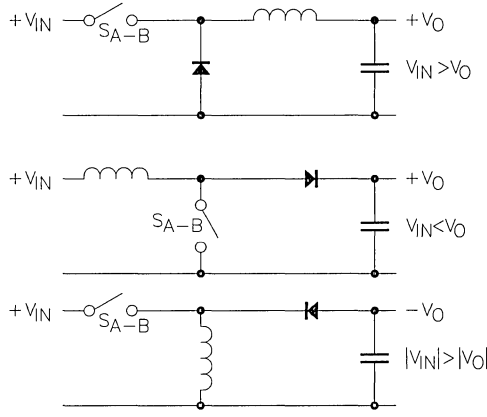


Figure 16. Single-Ended Inductor Circuits

The third general classification of power supply systems are transformer coupled, two types of which are shown in Figure 17.

The push-pull circuit represents the conventional DC to DC converter with each switch being controlled for 0-45% duty cycle modulation. The second transformer circuit is a single-ended flyback converter, useful at light loads without a separate output inductor.

To illustrate the use of the SG1524 in each of the above general classifications, the following simple, but practical, circuits are presented:

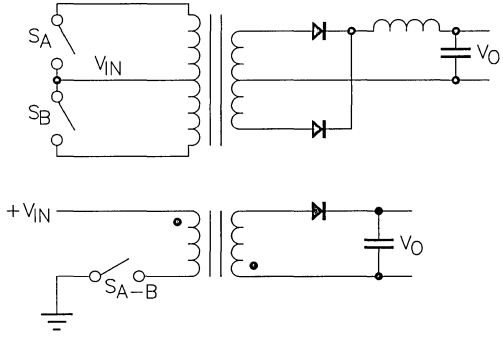


Figure 17. Transformer Coupled Circuits

Figure 18 shows the use of the SG1524 as a low current polarity converter providing a regulated -5volt output at currents up to 20mA from a single positive input voltage. The external components required include the divider resistors to interface the reference and output voltages with the error amplifier, a resistor/capacitor to set the operating frequency, and the output diodes and capacitors. The combination of the built-in current limiting of the SG1524 output stages and the capacitor coupling of the output signal provide full protection against short circuits and the current limit amplifier is more than enough to stabilize the regulating loop and no additional compensation is required.

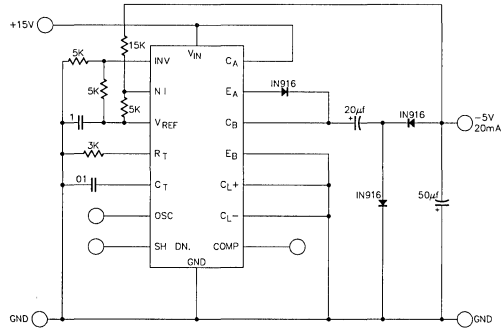


Figure 18. Low Current Polarity Converter

Another low-level circuit is the flyback converter shown in Figure 19.

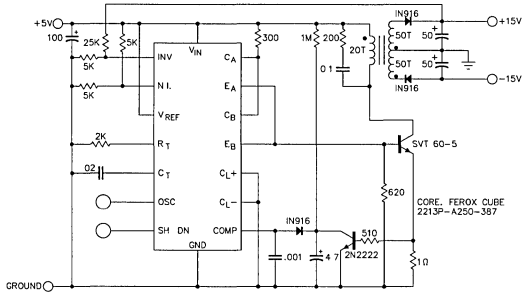


Figure 19. +5 to ±15 Volt, Flyback Converter

The circuit is designed to develop a regulated ±15volt supply from a single +5 volt source. Note that the reference terminal is tied to the input, disabling the internal regulator. The error amplifier resistors are also tied to the input line so that the output regulation can be no better than the input; however, an external reference could just as easily have been used.

In this application, the two output stages are connected in parallel and used as emitter followers to drive a single external transistor.

Since the currents in the secondary of a flyback transformer are out of phase with the primary current, current limiting is very difficult to achieve. In this circuit, protection was provided through the use of a soft-start circuit. If either output is shorted, the transformer will saturate, providing more current through the drive transistor. This current is sensed and used to turn on the 2N2222 which resets the soft-start circuit and turn off the drive signal. If the short remains, the regulator will repetitively try to start up and reset with a time constant set by the soft-start circuit. Removing the short will then allow the regulating loop to re-establish control.

For higher current applications, the single-ended conventional switching regulator of Figure 20 is shown.

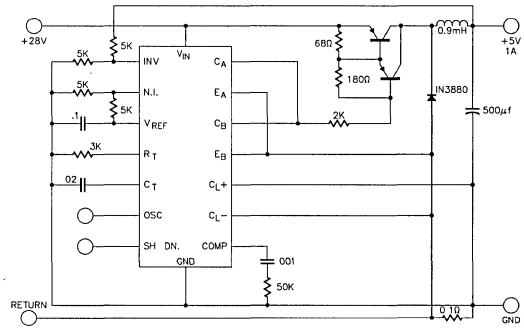


Figure 20. 1 Amp, Single-Ended Switching Regulator

In this case, an external PNP Darlington is used to provide a 1-amp current switch. The SG1524 has the two outputs in parallel, connected as a grounded emitter amplifier. The current sense resistor is inserted in the ground line and the voltage across it used for constant current limiting. Note that in addition to the divider resistors and frequency setting R_TC_T, a phase compensation resistor and capacitor is used to stabilize the loop now that an inductor has been added.

A fourth application would have to be a push-pull, DC to DC regulating converter as shown in Figure 21.

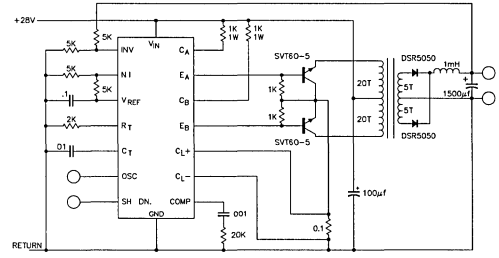


Figure 21. 5V, 25W, DC to DC Converter

Here the outputs of the SG1524 are connected as separate emitter followers driving external transistors. Current limiting in this application is done in the primary for several reasons: First, it's easier to live within the ±0.3 volt common mode limits of the current limit amplifier; second, since this is a step-down application, the current - and therefore the power in the sense resistor - is lower; and third, if the output drive were to become non-symmetrical causing the transformer to approach saturation, the resultant current spikes will shorten the pulse width on a pulse-by-pulse basis, providing a first order correction. Note that the oscillator is set to run at 40kHz to obtain a 20kHz signal at the transformer.

The application as shown does not provide input-output isolation and, of course, that feature is difficult to achieve within a single IC. There are a couple of ways the SG1524 can be used with isolated power supply systems, however. The first is shown in Figure 22 where the SG1524 is direct coupled on the secondary side of the output transformer. The outputs from the IC are transformer-coupled back to the primary side to drive the switching transistors. Of course, a separate start-up power source is needed for the SG1524 but that shouldn't present much of a problem remembering that the IC draws less than 10mA of supply current.

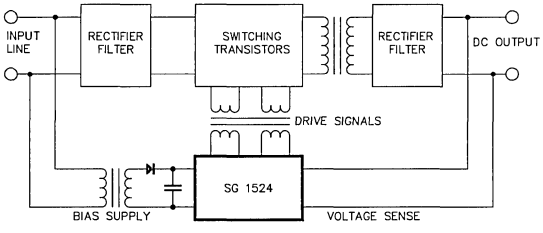


Figure 22. Input/Output Isolation

A different method of providing isolation is shown in Figure 23 where the IC is direct coupled on the primary side. Here a separate reference error amplifier (most easily implemented with a SG1532 regulator IC) is connected on the secondary and then optically coupled back to the primary side.

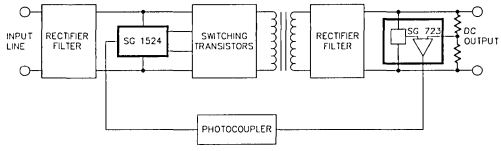


Figure 23. Input/Output Isolation

As should be evident from the above, the SG1524 was designed as the first of what will undoubtedly become a larger family of regulator IC's specifically designed for switching power supplies. As such, versatility was the primary design goal of this device and hopefully this goal has been achieved to the degree that will allow the SG1524 to find application to a wide range of power control systems.

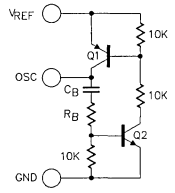
DEADBAND WITH THE SG1524 REGULATING PULSE WIDTH MODULATOR CIRCUIT

ABSTRACT

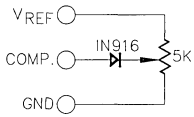
The SG1524 Regulating P.W.M. integrated circuit provides two outputs which alternate in turning on for push-pull inverter applications. The internal oscillator sends a momentary blanking pulse to both outputs at the beginning of each period to provide a deadband so that there cannot be a condition where both output transistors are on at the same time. The deadtime duration is determined by the width of the blanking pulse appearing on Pin 3, as measured at the ±0.7 volt level, and can be controlled by three techniques:

1. For the 0.3 to 1.0 microseconds, the deadband is controlled by the timing capacitor, C_T, on Pin 7. The relationship between C_T and deadband is shown in Figure 3 on the SG1524 data sheet. Of course, since C_T also determines the oscillator frequency, the range of control is somewhat limited.

2. Above 1.0 microsecond, a simple one-shot latch similar to the circuit shown below should be used.
   When this circuit is triggered by the positive-going pulse from the oscillator output, it will latch for a period determined by C_BR_B, providing a well-defined deadtime.



3. Another way of providing greater deadband is just to limit the maximum pulse width. This can be done by using a clamp to limit the output voltage of the error amplifier. A simple way of achieving this clamp is with the circuit below:



This circuit will limit the error amplifier's voltage range since its current source output will supply only 100μa. Another advantage of this circuit is that it does not change the programmedoscillator frequency.

In general, it is not recommended to stretch the deadtime by using external capacitors on Pin 3. There are several reasons for this:

a. It is difficult to obtain well-controlled, repeatable deadtimes with this approach, since the logic threshold is +0.7 volts. The normal exponential fall of the pulse trailing edge due to the external capacitor and internal 3K pull-down resistor results in a poorly-defined crossing of the logic threshold.

b. The external capacitor degrades the rise and fall times of the clock to the internal flip-flop. For sufficiently high values of capacitance, the flip-flop will cease to toggle properly, especially at higher temperatures.

In general, if a simple means of stretching deadtime is required, the best solution is to use the SG1524B device instead of the earlier 1524. Up to 1000pF can be connected to the OSC pin with no degradation of the flip-flop operation, since the clock to the toggle flip-flop in the 1524B is generated by the internal double-pulse suppression logic.

IMPROVING SWITCHING REGULATOR DYNAMIC RESPONSE

Edited by Stan Dendinger
Manager, Advanced Product Development
Silicon General, Inc.

ABSTRACT

Recent introductions of LSI integrated circuits for P.W.M. control have offered considerable simplification to the job of optimizing the design of switching regulators. In addition to greatly reducing the necessary circuitry, the linear transfer function of these devices eases the task of stabilizing the feedback loop and offers several possibilities for improved response. Experimental methods for evaluating the response characteristics of the P.W.M. switching and output stages can be used to confirm simplifying assumptions of linear operation. With this data, several approaches to equalization networks can be compared for performance optimization.

INTRODUCTION

The past few years have seen a major revolution take place in the field of power supply design. Whether forced upon us by the need for energy conservation or finally made practical thru recent advances in semiconductor technology, switching regulators are now the name of the game in voltage control. Novices soon learn, however, that the implementation of a well-designed switching supply involves a little more skill than that required for a linear regulator.

Although the theory of switching regulation has long been known, there is much practical technology - or art - in designing efficient and reliable systems. This is still true even though recently introduced semiconductor devices have made the job at least a little easier. It is the purpose of this discussion to cover a few of the practical aspects of implementing and stabilizing switching regulators using these newer devices.

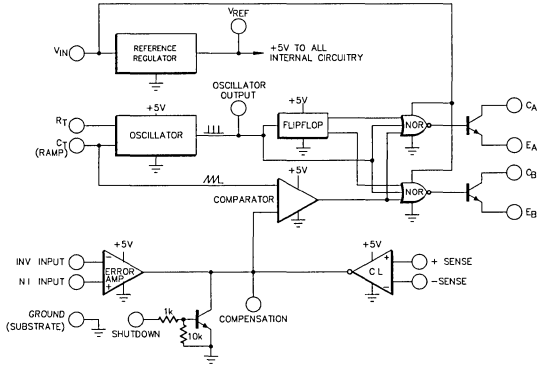


Figure 1. SG1524 Block Diagram

INTEGRATED P.W.M. CONTROL CIRCUITS

Recognizing a rapidly growing market, many component suppliers have introduced new devices designed specifically for switching regulator applications. These include faster power transistors with improved S.O.A., low E.S.R. electrolytic capacitors, hybrid power devices which include a matched commutating diode, and monolithic IC control devices such as the SG124[1] which contain all of the P.W.M. control circuitry in a single 16-pin, dual-in-line package.

From the block diagram shown in Figure 1, it can be seen that the SG1524 contains the elements necessary to implement either single-ended switching regulators or DC to DC converters of several different configurations. This device includes a voltage reference, error amplifier, constant frequency oscillator, pulse width modulator, pulse steering logic, dual alternating output switches, and current limiting and shutdown circuitry. Since many of the different types of applications for this IC have been discussed earlier[1] it should suffice to review only two of the more common usages as shown in Figures 2 and 3.

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The single-sided regulator of Figure 2 is unique because of its simplicity. This circuit combines an SG1524 with an SM625 hybrid to build a 5 volt, 5amp regulator with all the semiconductor devices contained in only two packages. This circuit has an efficiency of over 70% with an input voltage range of 20 to 30 volts, 0.1% line and load regulation, and some added benefits of constant frequency operation and short circuit protection.

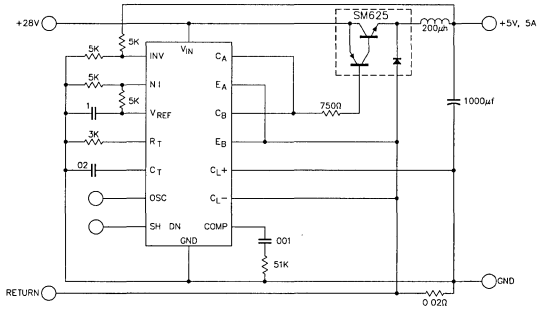


Figure 2. SG1524 Single - Ended Switching Regulator

Figure 3 shows the same 5-volt, 5amp output requirement met this time with a DC to DC converter. The use of high speed transistors and Schottky rectifiers keep the efficiency more than 80% - significant for a low-voltage output - while maintaining all the other benefits included in the single-ended circuit.

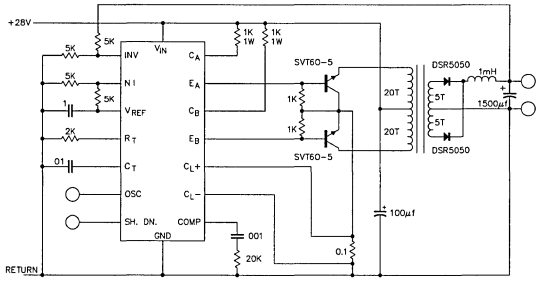


Figure 3. SG1524 Regulating DC - DC Converter

It should be recognized that the above circuits represent very basic applications of an IC control chip. Most practical power supply systems would probably incorporate many other features which may be accomplished by interfacing these IC's with a small amount of external circuitry to add characteristics such as: sift start, oscillator synchronization, dead-band controls, additional current and/or voltage step-up stages, input-output isolation, remote overvoltage or overload shutdown, and response modifying circuitry. It is this latter subject we wish to explore more fully below.

SWITCHING REGULATOR CONTROL

The basic switching regulator control loop which applies to the most common forms of implementation is illustrated in Figure 4. In analyzing this control loop stability, the obvious immediate problem is the transfer function of the P.W.M. and output stage. A detailed and accurate analysis of the nonlinear characteristics of this stage is an extremely difficult and complex task if one is to account for all the parameters which could possibly be a factor. [2,3,4] On the other hand, if this stage could be assumed to have a linear transfer function, analysis becomes a relatively simple application of basic feedback theory.

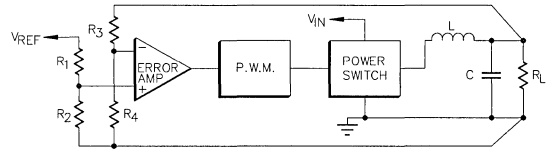


Figure 4. Basic Regulating Control Loop

A significance of the SG1524 is that it uses a design approach which makes a linear assumption accurate enough for most applications. The fact that this device features constant frequency operation, a linear-slope ramp for P.W.M., and fast-response logic and output circuitry all contribute to minimizing the errors associated with a linear assumption. Of course, there are factors external to the IC which could destroy this assumption. Such things as excessive delay in the switching transistors, parasitic ringing or oscillation in the power stages, or nonlinear operation of the magnetics could all cause a resultant nonlinear performance. A first exercise for the designer, then, is to confirm linear operation of the P.W.M. and output stages of his regulator by evaluating his early breadboard models.

OUTPUT STAGE ANALYSIS

The pulse width modulation is accomplished in the SG1524 by comparing the output of the error amplifier with a linear ramp, or saw-tooth signal from the oscillator. Because the comparator has both high gain and high output impedance, and the error amplifier has a high output impedance, this node (pin-9) becomes a very convenient place for inserting a test signal. A voltage source applied as shown in Figure 5 will completely override the error amplifier and essentially open the loop without actually breaking any connections. In addition, the test signal is easily managed because the voltage gain from this point to the output is relatively low. (A voltage level on pin 9 of from 1 to 4 volts will change the pulse width from zero to maximum which will yield zero to maximum output voltage.)

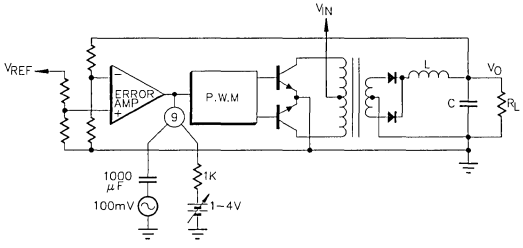


Figure 5. Measuring Output Stage Transfer Function

In experimentally attempting to confirm satisfactory operation of the output stages, the designer hopes to prove that a linear equivalent circuit model is valid for reasonable analysis. One such model as proposed by Middlebrook[5] is shown in Figure 6. This model describes the overall AC and DC transfer function and input and output impedances in terms of the duty cycle and modulation constant. This model assumes that the effects of operating frequency, switching delays, and parasitic elements are well above the frequencies of interest as defined by the output LC filter.

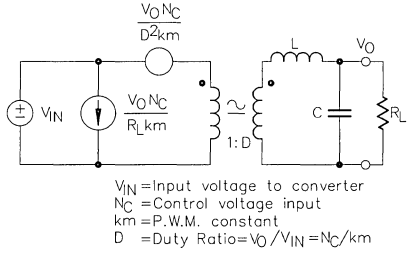


Figure 6. Linear Equivalent Circuit

Values for the inductor and capacitor are normally calculated on the basis of output ripple current and voltage as follows:

$$L = \frac{V_{IN} f(\Delta_{IL})}{V_O(V_{IN} - V_O)}$$

and

$$C = \frac{V_{IN} f(\Delta_{IL})}{8Lf^2 V_{IN}(\Delta V_O)}$$

where:

V_{IN} = peak input voltage to the indicator
V_O = output across the capacitor
f = switching frequency
ΔI_L = peak - to - peak current variation in the inductor
ΔV_O = peak - to - peak ripple voltage across the capacitor

Note that the actual ripple voltage at the output of the filter will be ΔV_O, plus ΔI_L times the capacitor E. S. R.

Regardless of the requirements for minimizing the output ripple, an additional requirement on the filter is that its cutoff frequency will be well below the switching frequency if our original goal of simple linear analysis is to be met. Specifically, the switching operation introduces a second order lag at one-half the switching frequency and for the output filter to dominate, its cutoff should be at least an order of magnitude below that number or

$$\frac{1}{2\pi\sqrt{LC}} \leq \frac{f}{20}$$

To verify the performance of the resultant hardware, a Bode plot of the output stage response can be most meaningful. Ideally, a plot as shown in Figure 7 should show a flat response to the filter cutoff and then a linear 12dB/octave rolloff with a 180° phase shift.

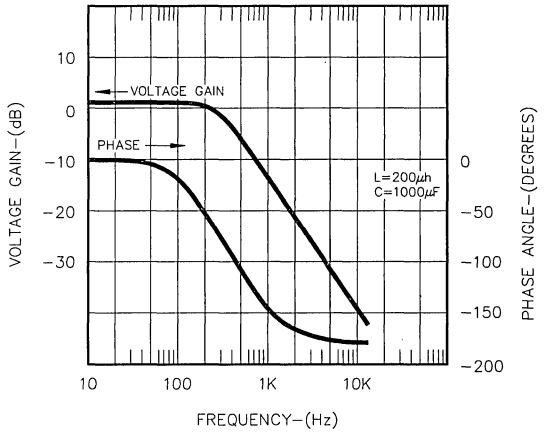


Figure 7. Linaear Output Stage Response

By making these plots with varying input voltage and load current, factors affecting stability such as leakage inductance, capacitor E.S.R., and either saturation or discontinuous operation of the magnetics may be evaluated over the operating conditions of interest. Figure 8 shows typical plots with less than ideal component parameters. With the characteristics of the output stage defined, attention can be turned to the error amplifier to develop an equalizing network which will allow satisfactory closing of the loop.

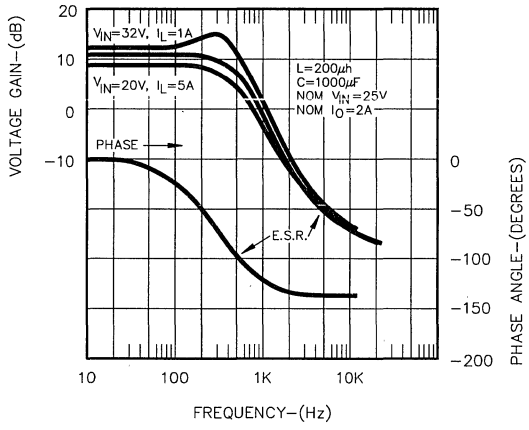


Figure 8. Measured Output Stage Response

ERROR AMPLIFIER COMPENSATION

The error amplifier contained within the SG1524 is a transconductance amplifier in that it has a high-impedance, current source output. The gain is a function of the output loading and can be reduced from a nominal 80dB by shunt resistance as shown in Figure 9. Note also in Figure 9 that the uncompensated amplifier has a single pole at 300Hz and 90° of phase shift. The unity gain cross-over frequency is 3MHz and the large scale slew rate is 0.5 volt per microsecond.

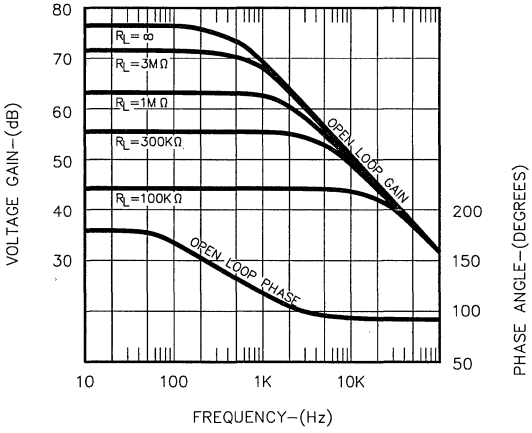


Figure 9. SG1524 Single - Ended Switching Regulator

This type of amplifier can be compensated in two ways: The compensation network can go from the output to ground so it can be connected from output back to the inverting input.[6] In the first case the voltage gain is:

$$A_V = gmZ_c = \frac{2kT}{8I_cZ_c} \approx 0.002Z_c$$

where Z_c is the complex compensation network impedance. If a feedback approach is used, the gain is:

$$AV = \frac{Z_c}{Z_s}$$

where Z_s is the source impedance driving the input. In cases where relatively low impedances are desired in a feedback network, it may be necessary to buffer the high output impedance of the error amplifier. Figure 10c shows the use of an external emitter follower to provide a low driving impedance for the feedback network.

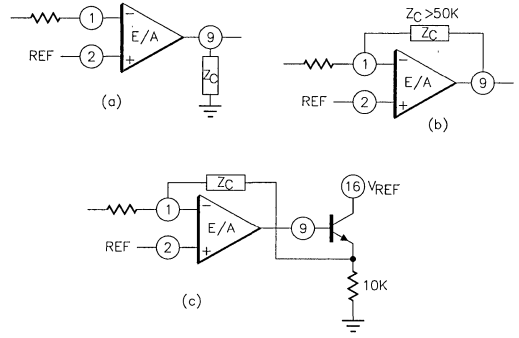


Figure 10. Error Amplifier Compensation Networks

To stabilize the overall regulator feedback loop of Figure 4, it should be apparent that the uncompensated loop contains at least two poles in the output filter and one more in the error amplifier, a situation which typically results in significant gain remaining when the total loop phase equals 360°. One of the simplest compensation schemes is to convert the error amplifier to an integrator by adding a single dominate pole at a frequency so low that the loop gain falls below unity well before the cutoff frequency of the output filter. While this approach yields a stable closed loop gain as shown in Figure 11, the response to disturbances is very slow. For example, the waveforms of Figure 12 show the response to a 20%, or one amp, step change in load to the circuit of Figure 3 when compensated with a 0.2μfd capacitor around the error amplifier.

If instead of slowing down the error amplifier, a zero, or lead network is added to cancel one of the output filter poles, we can keep the total loop phase less than 360° to well beyond the output filter cutoff.

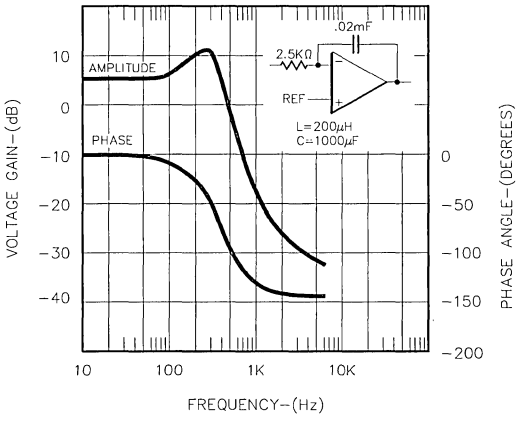


Figure 11. Closed Loop Frequency Response

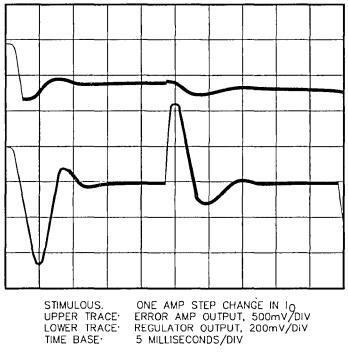


Figure 12. Integrator Compensation Step Response

Figure 13 shows a circuit for accomplishing this by moving the amplifier pole lower in frequency and adding a zero at the output filter cutoff frequency. Figure 14 shows the effects of this network on the Bode plot of the error amplifier, and Figure 15 indicates the improvement in recovery from the same one-amp load change. Note how the output of the error amplifier overshoots to give a boost to the output.

Even faster response can be achieved by providing additional lead networks. For example, another zero may be added by bypassing the sense feedback resistor. As can be seen in Figure 16, this greatly improves loop response but offers the hazard of coupling ripple noise directly into the error amplifier.

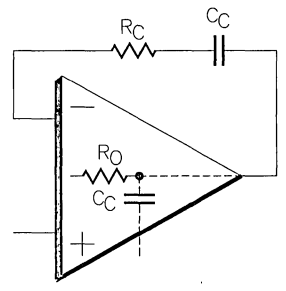


Figure 13. Series RC Phase Compensation

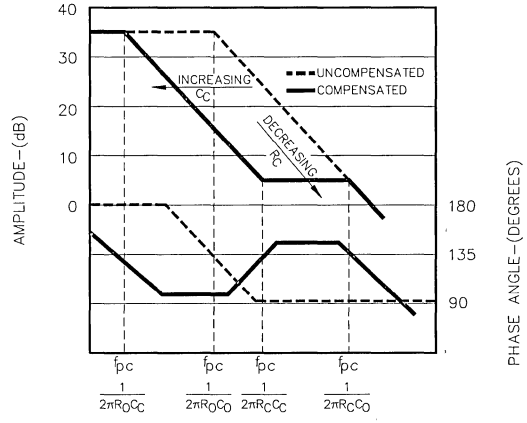


Figure 14. Phase Compensated Bode Plot

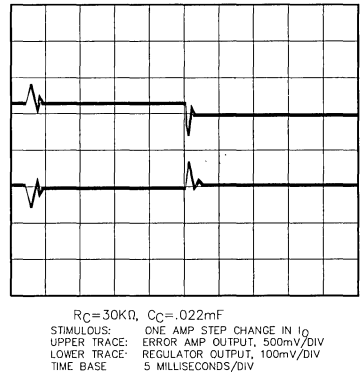
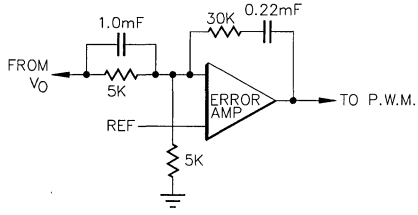


Figure 15. Phase Compensated Step Response

TWO LOOP CONTROL

From the examples presented above, it should be apparent that the integration method of error amplifier compensation provides good stability by making the dominate pole so low in frequency that variations in all other circuit parameters become inconsequential. This technique also provides high accuracy at DC where high gain can be used and is the type of feedback one would want to take directly from the output of a regulator since a user might add additional external capacitance, thereby changing the output filter characteristics. Another reason for using single-pole compensation is to accomodate the use of a two-stage output filter which can add phase shifts well beyond 180°.



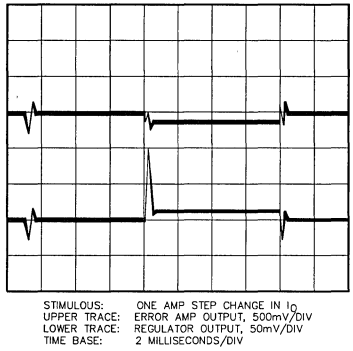


Figure 16. Double Zero Compensated Step Response

The problem of poor response can then be accommodated by adding a differentiated signal taken from somewhere else in the loop. If the time constants and gain factors are properly selected, the differentiated signal can compensate for the error in the integrated signal taken from the regulated output.

SUMMARY

Although integrated circuit controllers for switching supplies have removed much of the circuit complexity from this type of regulator, the dynamic analysis of the control loop must still be optimized for each application. This optimization is made easier, however, if a linear approximation of the switching stages can be shown to be valid. The SG1524 controller offers benefits in this regard as it does provide a linear transfer function through its pulse width modulation scheme. Therefore, experimental techniques can be used to simply confirm proper operation of the power switches and output filter.

With a linear output stage, conventional feedback analysis can be used to define the best equalizing network achieving a compromise between stability and fast response. In some cases it may even be desirable to provide separate signal paths for these two parameters but this, too, can be adapted to the SG1524 controller with a minimum of external circuitry.

Obviously, no recipes for optimum performance have been provided herein. Only a few directions which, it is hoped, will point the way toward the development of specific solutions for specific applications.

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CONVERTING 1524 SWITCHING POWER SUPPLY DESIGNS TO THE SG1524B

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Silicon General, Inc.

INTRODUCTION

Many power control engineers have designed successful switching power supplies around the SG1524 Pulse Width Modulator integrated circuit. This application note explains the differences between this earlier device and the more sophisticated SG1524B. While the functional pinouts are identical for the two devices, there are some distinct operational differences which the user should be aware of when designing new supplies or when updating an existing design. In many cases design changes are minimal (such as adjustment of frequency compensation) or not required at all. At the same time the improvements in control architecture and circuit design of the SG1524B allow the designer to obtain levels of performance in new power supply designs not possible with the older device.

GENERAL COMPARISON

Figures 1 and 2 show respectively the block diagrams of the SG1524 and the SG1524B. Both devices were designed for voltage-mode control, but both can be used to implement current-mode control as well with the addition of an external dual op amp. For further details see the Silicon General Application Note "Current Mode Control with the SG1524B."

The main functional difference between the two circuits is in the action of the shutdown pin. In the SG1524, a voltage at Pin 10 greater than +0.7 volts will turn on an internal transistor which pulls the error amplifier output to ground. In the SG1524B, a voltage greater than +1.2 volts at Pin 10 activates a logic gate which inhibits the pulse output of the PWM comparator. The error amplifier output-voltage is not affected directly.

Other improvements include the addition of an undervoltage lockout function and fault suppression logic. These provide protection against inadequate supply voltage to the control IC and insure constant-frequency alternating output pulses to the power devices.

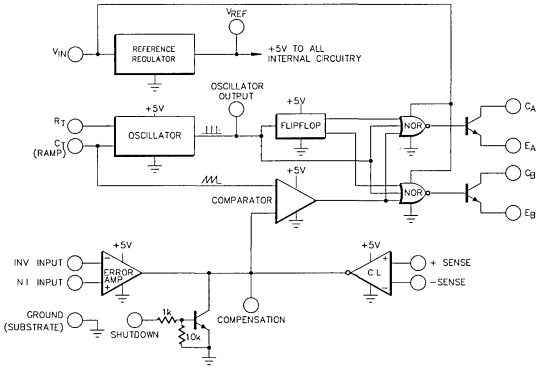

Figure 1. SG1524 Block Diagram

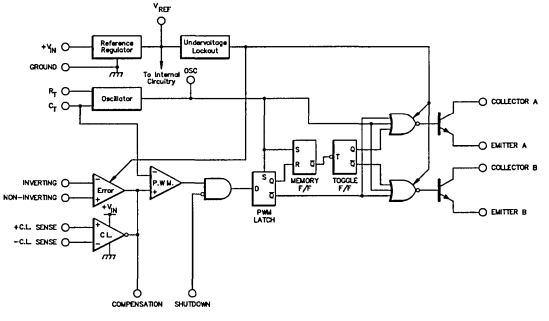

Figure 2. SG1524B Block Diagram

INDIVIDUAL SECTION DIFFERENCES

Voltage Reference

The voltage reference is a low-drift bandgap design which provides a precision +5.0 volt references for the control loop. Initial accuracy is ±1% for the SG1524B/2524B, and ±2% for the SG3524B. This is a factor of four improvements over the original reference. Line regulation is typically better by a factor of 3:3mV instead of 10mV. Load regulation is better by a factor of 4:5mV rather than 20mV. The temperature coefficient is also lower and more uniform from device to device. All these features translate directly into tighter tolerances on the switcher output voltage.

At 25°C the differential drop across the regulator is only 1.2 volts, as opposed to 2.7 volts for the 1524. Figure 3 shows the relationship between V_{IN} and V_{REF} for both devices. As a result, the SG1524B is fully functional with a 6.2 volt supply. Under worse case conditions of I_{LOAD} = 20mA and T_A = -55°C, all devices also guaranteed to function at V_{IN} = 7 volts.

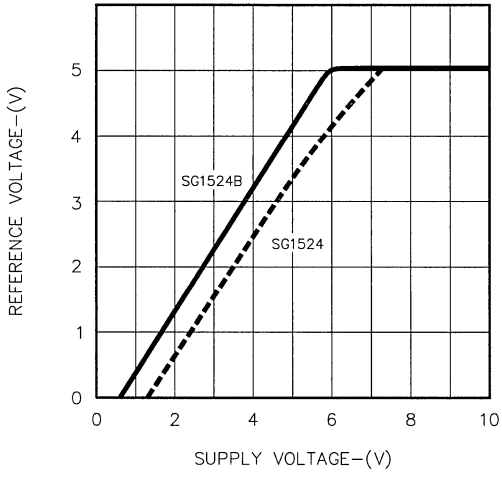

Figure 3. Reference Voltage vs. Supply Voltage

Undervoltage Lockout

This circuit has two sections: a controlled current source which forces the error amp low and the output transistors off, and a bandgap comparator which overrides the lockout source. The current source is fully active when V_{IN} is +1.2 volts. Since the error amp and output driver cannot function until V_{IN} is approximately 3 volts, it is impossible for spurious output pulses to occur when the supply voltage is too low for normal operation.

The bandgap comparator monitors the reference voltage. It enables the SG1524B when the reference rises to +4.3 volts. This arrangement allows operation from a +5 volt ±5% supply by connecting V_{IN} and V_{REF} together.

The action of the undervoltage lockout can be observed with the test circuit of Figure 4. A 100K pull-up resistor is connected from Compensation to V_{IN}. V_{IN} is swept from 0 to +6.5 volts with 5Hz triangle waveform from a function generator. An oscilloscope in XY Mode displaying V_{IN} horizontally and Compensation vertically will generate the display shown in Figure 5.

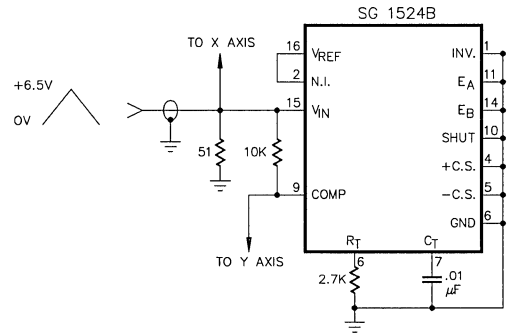

Figure 4. Undervoltage Lockout Test Circuit

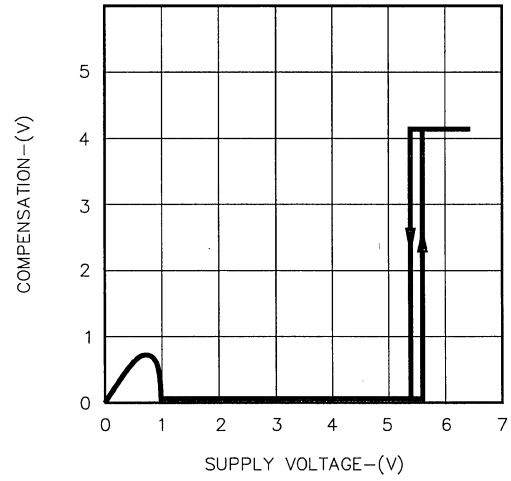

Figure 5 - Undervoltage Lockout At The Error Amp

As V_{IN} slowly sweeps from 0 to 1 volt, the lockout current source becomes active and pulls the error amp to ground, guaranteeing 0% duty cycle from the controller. From 1 volt to approximately 5.5 volts the controller is inhibited while the internal circuitry stabilizes. At 5.5 volts the bandgap comparator overrides the lockout current, releasing the output of the error amp. The reverse portion of the voltage sweep is identical, except that approximately 200mV of hysteresis can be observed at the comparator trip point.

Oscillator

The oscillator of the SG1524B is programmed for frequency with an external R_T and C_T in the same manner as the SG1524. Both initial accuracy and temperature coefficient have been improved with the "B" version.

There are two methods to synchronize multiple units together.

A. Program master unit with R_T and C_T for the desired frequency. Connect the Ct terminal (Pin 7) of the master to the Ct terminal of the slave. Connect the OSC terminal (Pin 3) of the master to the OSC terminal of the slave. Leave the slave R_T terminal (Pin 6) open or tied to the reference. This is the recommended approach if the PWM controllers are close together (on the same printed circuit board and within six inches of each other).

B. Program a master unit for the desired frequency. Select R_T and C_T for the slave units such that they free-run at a frequency 10% slower than the master. Connect all the oscillator terminals together. This method is recommended if the PWM controllers are not close together, since it avoids routing a high impedance line (C_T) around a noisy environment.

To synchronize one or more devices to an external clock frequency, one of the connections shown in Figure 6 should be used. The device(s) to be synchronized should free-run 10% slower than the clock. Pulse width of the external clock should be at least 200nsec, but not longer than the desired deadtime.

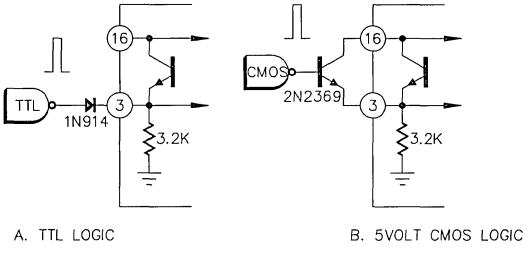

Figure 6. Oscillator Sync to an External Clock

Error Amplifier

The error amplifier of the SG1524B is, like its predecessor, a transconductance design with an output impedance of approximately 4 megohms. This allows use of external clamp circuitry to obtain soft-start and duty cycle limit, as on the original 1524. Since all the voltage gain takes place at the output pin, open-loop gain/frequency characteristics are easily controlled by shunt reactance from Pin 9 to ground (Figure 7). Also, this type of amplifier has a very predictable 1/T variation of open-loop gain with absolute temperature as shown in Figure 8.

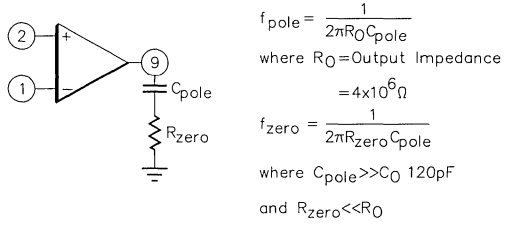

Figure 7. Frequency Compensation of the Error Amplifier

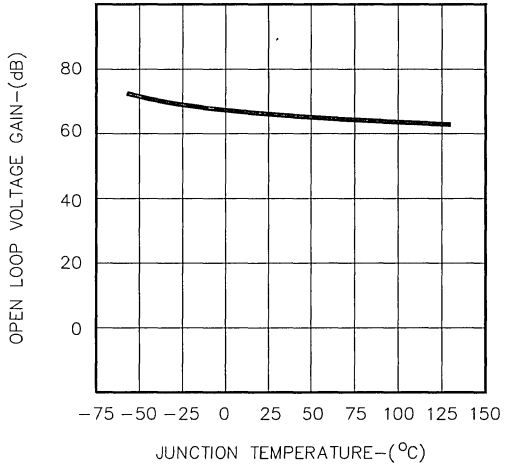

Figure 8. Open Loop Gain vs. Temperature

The input common mode range is +2.3 to +5.2 volts, so that existing designs at +2.5 volts will function with no modifications. For new designs the +5 volt reference may be applied directly to the non-inverting input, eliminating the necessity for two divider resistors.

Since the lower common mode limit is +2.3 volts for the 1524B and +1.8 volts for the 1524, neither amplifier should ever be used in the

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non-inverting unity-gain configuration shown in Figure 9. The error voltage must swing down to +0.5 volts to guarantee 0% duty cycle from the pulse width modulator, and this violates the common mode range specification.

In general, any frequency compensation for the voltage control loop which works with the SG1524 can also be used with the SG1524B with no modification.

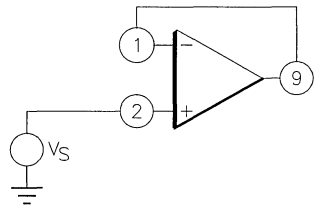

Figure 9. Non-Inverting Unity-Gain Connection
(Not Recommended)

Current Limit Amplifier

The current limit amplifier of the SG1524B is one of the most significant areas of change from an applications viewpoint. Like the original circuit, there is a fixed 200mV threshold designed into Pins 4 and 5 to permit direct sensing across a current sampling resistor. Differences in the "B" circuit affect the input bias current, allowable common mode range, and stability in current-limit.

Input Bias Current

In the SG1524, there is a constant 130μA flowing out of Pin 4, while the current out of Pin 5 is variable from 0 to 100μA depending on the differential input voltage. Because of this characteristic, the current limit sense terminals must be driven from source impedances less than 20 ohms to avoid modulating the current limit threshold. The "B" device features bias currents which are identical at each pin, are independent of current sense voltage, and are a factor of 10 lower. This allows predictable foldback current limiting without wasteful low-resistance divider networks.

Common Mode Range

The guaranteed common mode range of the current sense inputs is 0 volts to V_{IN} -2.5 volts. Current sensing in a supply ground line is possible, but the configuration of Figure 10 should be used to avoid damaging the IC. The 100ohm resistor is required because of delays through the controller and storage time in any bipolar device. The SG1524B will reduce the pulse width as Pin 5 is driven 200mV below ground, but in practice it is overdriven due to the aforementioned delays. If Pin 5 is driven below -0.3v at T_A = +125°C the substrate diode will conduct. The 100ohm resistor will limit the peak substrate current to a safe value without shifting the C.L. threshold.

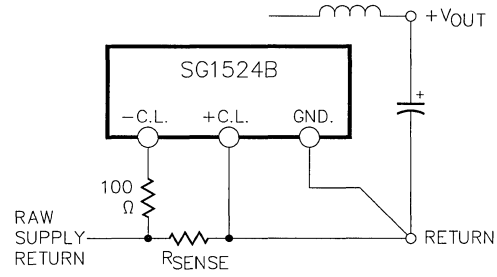

Figure 10. Current Sensing in the Ground Line

Current sensing may also be accomplished with a common emitter or source resistor to ground as shown in Figure 11; or it may be placed in the supply output line, as indicated in Figure 12. At -55°C the value of V_{IN} must be at least 2.5 volts greater than the switcher output voltage.

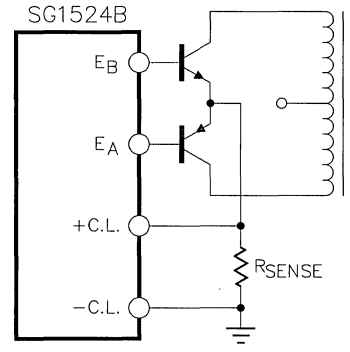

Figure 11. Sensing Primary Current With an Emitter Resistor

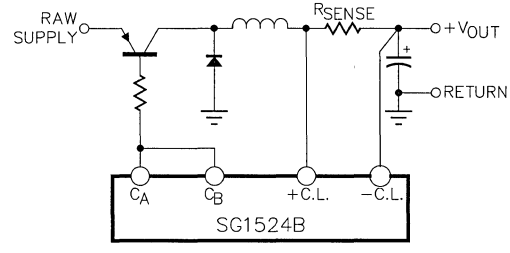

Figure 12. Current Sensing in the Output Line

Frequency Compensation

The original SG1524 current limit amplifier had a typical open loop gain of 44dB and was internally compensated to produce a single-pole rolloff above 300Hz. The SG1524B exhibits 75dB of gain and has no internal compensation. The circuit may be used as a moderate speed comparator, or it may be used as an analog gain block to override the error amplifier.

Because of the higher gain and bandwidth, designers may find that the control loop will oscillate when the supply goes into current limiting. The cure is to add frequency compensation externally to the current limit circuit or to rework the existing voltage loop compensation. See the Silicon General Application Note "A New, Versatile P.W.M. Control Circuit for Switching Power Supplies."

Shutdown

The shutdown circuit of the "B" is illustrated in Figure 13. It has the following differences compared to the 1524:

A. Logic threshold is +1.2 volts instead of +0.7 volts for compatibility with TTL logic and improved noise immunity.

B. Input current is very low (usually under 100μA) even at +5 volts input. The pin may be driven directly from TTL logic (all families) to TTL-output comparators.

C. Response time is very fast, between 35 and 100 nanoseconds depending on output transistor loading.

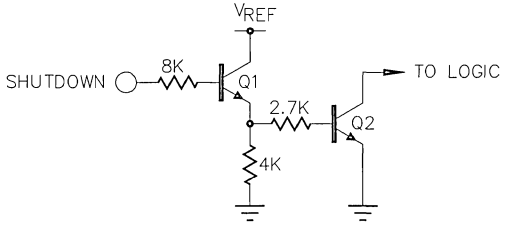

Figure 13. Shutdown Circuitry ot the SG1524B

The shutdown pin should never be left floating. If not used, the pin should be grounded. If the shutdown function is used, the pin should be driven from a low impedance source to prevent noise pickup. The internal logic is very fast, and will respond readily to spurious pickup from the normally noisy environment of a switcher.

Output Transistors

The output devices have been redesigned to provide 100mA continuous and typically 200mA peak, with BV_{CEX} ratings of 60 volts. Saturation voltage is guaranteed both at 10m and 100mA to ease the interface with external power devices.

Bipolar Drive

For driving bipolar devices the circuit in Figure 14 is recommended. The ouput transistor is used as a phase-splitter to generate the necessary base drive. Figure 15 illustrates forward and reverse base current, and collector current of a PMD 20K 120 volt, 14amp Darlington using this driver configuration.

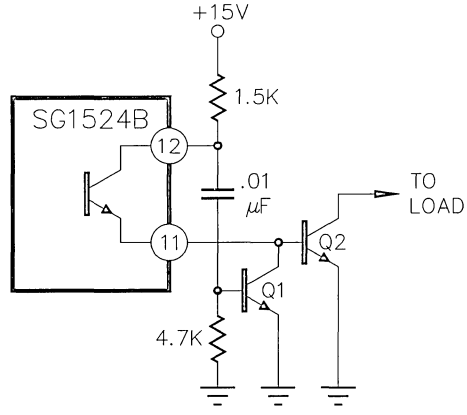

Figure 14. Driving Power Bi-Polar Transistors with the SG1524

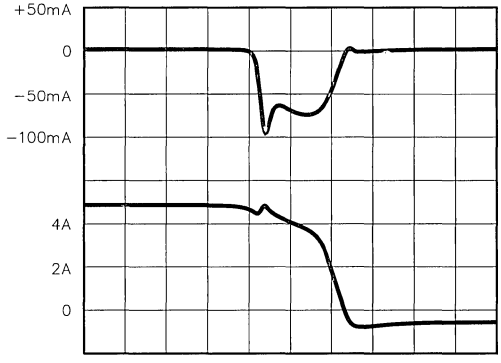

Figure 15. Bipolar Turn-Off Waveforms.
Upper Trace: Darlington Base Current @ 200 Nsec/Div.
Lower Trace: Collector Current @200 Nsec/Div.

MOSFET Drive

Highly capacitive loads such as presented by the gated of power MOSFET's can be readily driven with the circuit in Figure 16. At turn-on, 200mA of charging current is conducted by D1. During turn-off D1 becomes back-biased by the pull-down resistor. Q1 turns on and provides 500mA of discharge current. Figure 17 shows the turn-off gate voltage and drain current of an IRF130 100 volt, 14amp power MOSFET driven directly with this circuit.

CONCLUSION

A designer who is familiar with the SG1524 will find it relatively easy to adapt his designs to use the SG1524B. The immediate benefits are higher levels of power supply performance, worthwhile reductions in total component count, a greater degree of protection for the power devices, and lower overall costs.

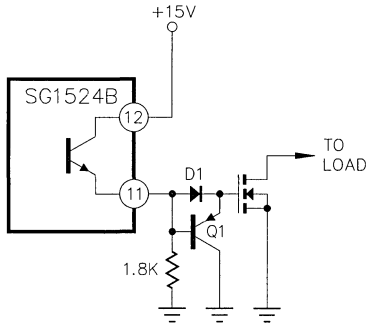

Figure 16. Driving Power MOSFETS With the SG1524B

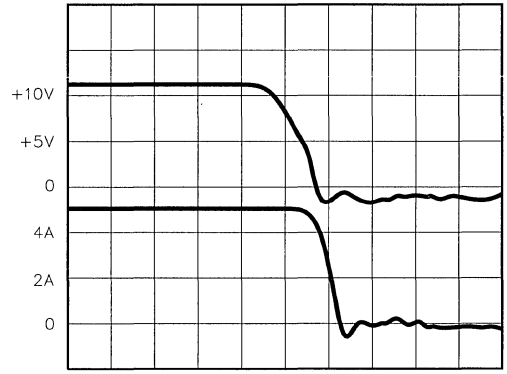

Figure 17. MOSFETS Turn-Off Waveforms.
Upper Trace: Gate Voltage @ 100 Nsec/Div.
Lower Trace: Drain Current @ 100 Nsec/Div.

A NEW, VERSATILE P.W.M. CONTROL CIRCUIT FOR SWITCHING POWER SUPPLIES

Stan Dendinger
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Silicon General, Inc.

ABSTRACT

A new control circuit for pulse-width-modulated switchmode power supplies is described. This device offers improved electrical and functional performance over earlier designs, while retaining the familiar pin-out of the industry-standard SG1524. Innovative circuit design techniques and optimized control architecture result in improved reference accuracy, protection against inadequate supply voltage, elimination of harmful output switching transients, improved current limiting, and higher voltage and current capabilities from the output transistors. A 50kHz power supply utilizing the new controller is described, and performance characteristics are analyzed.

INTRODUCTION

Since the introduction in 1976 of the first monolithic control chip for switchmode power supplies, and its subsequent wide acceptance as the basic building block for high-efficiency regulator designs, the semiconductor industry has found itself in a bit of quandry when attempting to define an improved device. On the one hand, the initial device, being rather simple and straightforward, had a number of deficiencies when its capabilities were compared with the total requirements of most switchers. As a result, new, more complex controllers were introduced with improved reference accuracy, protection against inadequate or fluctuating supply voltage, improved current limit circuitry, fault suppression logic, and a host of other features.

On the other hand, the new controllers, while enthusiastically accepted first by aerospace designers for sophisticated high-performance supplies and later by major computer and instrumentation manufacturers, lacked the familiar pin-out of the earlier device. As a result it has not been possible until recently to easily upgrade the performance of an existing design by simply plugging in a more intelligent pin-for-pin substitute.

The circuit to be described has been under development at Silicon General for more than two years, and represents an attempt to fit as much function as possible within the constraints of the original device pin-out. Designated the SG1524B, the device block diagram is shown in Figure 1.

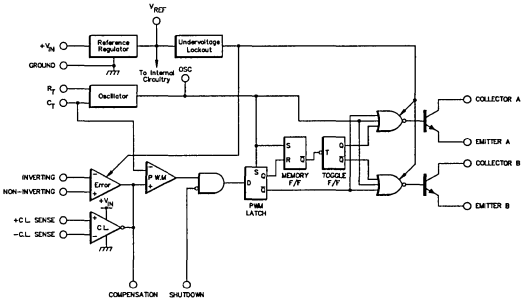

Figure 1. Block Diagram of the SG1524B Pulse Width Modulator

FUNCTIONAL DESCRIPTION

A precision +5.00V reference trimmed to an initial ±1% accuracy provides a voltage standard for the regulation loop. It also powers most of the internal control circuitry, eliminating adverse effects due to fluctuating supply voltage. A high gain error amplifier compares the reference voltage with the switchmode supply output voltage, and generates a PWM control voltage at Pin 9. This voltage is compared against a periodic linear ramp generated by the oscillator circuit. Oscillator frequency is determined by an

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external timing resistor and capacitor, R_T and C_T. The comparator output is a fixed-frequency, variable pulsewidth logic signal which passes through routine logic to one of the two high current output transistors if the Shutdown pin is LOW.

A current limit amplifier within the IC overrides the PWM control voltage when the voltage differential at the Current Limit Sense inputs reaches 200mV. This built-in threshold permits direct sensing across an external current sampling resistor. On-chip undervoltage lockout circuitry protects the power semiconductors in the switchmode supply by guaranteeing orderly start-ups and shutdowns as supply voltage is switched on and off.

Each control section of this new PWM controller has been either redesigned for improved performance, or is a completely new function compared to the original SG1524 design. A detailed description of each section follows to highlight the major improvements.

Bandgap Reference Regulator

The precision reference uses the predictable base-emitter voltage of NPN transistors to generate the +5V reference voltage, rather than a zener diode[1,2] The advantages of this design approach are: lower noise due to elimination of the shot noise associated with an avalanche device, low turn-on drift, better log term stability, and operation from a lower supply voltage. The primary disadvantages are that the bandgap requires more components, and thermal matching of key devices is necessary for realizing low thermal drift.

	ZENER REFERENCE	BANDAGE REFERENCE
Minimum Supply Voltage	8V	7V
Output Noise Voltage	75 μVrms	25 μVrms
Long Term Stability	20 mV/1000hrs	5 mV/1000hrs
Turn-on Drift	5-35 mV	2 mV

Table 1. Comparison of Zener and Bandgap Reference Typical Parameters

The ability of the PWM controller to be fully functional with a 7V supply enhances its usefulness in portable instrumentation applications, where six-cell Ni-Cad battery voltage is defined as end-of-life before recharge.

Undervoltage Lockout

The undervoltage lockout circuitry prevents spurious turn-on commands to the external power transistors when the supply voltage to the integrated circuit is too low for proper operation. When the reference voltage is less than +4.5V, the output transistors are forced to an OFF or nonconducting state. Additionally, the output of the error amplifier is clamped to ground. When the supply voltage rises to +7V, the output drivers are enabled and the amplifier output is released. Since compensation capacitance is usually present at Pin 9, this provides a measure of built-in soft start.

During the power-up period of the controller, when the undervoltage lockout is achieved, bias current is freely supplied to all the internal control circuitry. This insures that all control functions have stabilized in the proper state when the turn-on voltage is reached, and it prevents the possibility of start-up glitches.

The lockout circuitry monitors the reference voltage rather than $+V_{IN}$ to allow the SG1524B to be used with +5V supplies in the same manner as the original SG1524. If the $+V_{IN}$ pin is connected to the V_{REF} pin and +5V ±10% is applied, the control chip will function normally. When the undervoltage sense circuitry monitors the $+V_{IN}$ pin, this type of operation is not possible due to the 2-3V drop across the internal regulator.

Tp provide jitter-free turn-on and turn-off points, the lockout circuitry has been designed with approximately 500mV of hysteresis. This provides rejection of 120Hz ripple on the $+V_{IN}$ line and reduces capacitive filtering requirements on the controller supply voltage.

Error Amplifier

The error amplifier of the SG1524B was designed with three principle goals in mind: a common-mode range extending from +2.5V to $+V_{REF}$, excellent supply voltage and common-mode noise rejection characteristics, and a minimum voltage gain of 60dB at +125°C. Like its predecessor, it is a transconductance amplifier with a high-impedance output to permit external soft-start circuitry.

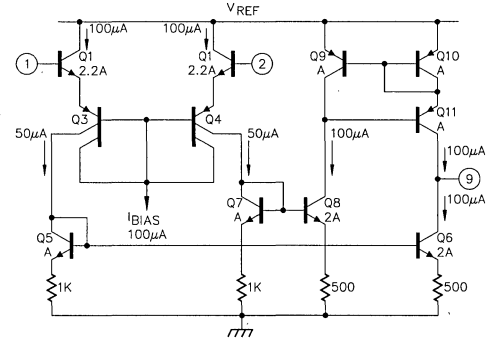

Figure 2. Schematic Diagram of the SG1524B Error Amplifier

Input transistors Q1 and Q2 are connected as emitter-followers with their collectors tied to the +5V reference supply. This configuration provides the required common-mode range, even with $+V_{IN}$ connected to V_{REF} for operation from a +5V supply. It also provides current gain to reduce input bias current, and produces a low impedance source to drive level shifters Q3 and

Q4. These PNP devices operate at a forced beta of 1.0, and are connected common base to maximize frequency response. Input stage operating current is set up by the 100μA bias supply to the common base. Frequency response is further improved by the low impedance collector loads Q5 and Q7. These two devices are diode-connected and form the input sides of two precision 2-to-1 current mirrors, which provide additional current gain. The output current of Q6 provides the pull-down or sink current for the amplifier output. The collector current of Q8 is referenced to the +5V supply rail by the Wilson current mirror consisting of Q9, Q20, and Q11. the collector current of Q11 provides the pull-up or source current for the amplifier output. It can be seen from the symmetry of the circuit that a differential input voltage is converted to an output current, with a maximum of ±200μA available. The open-loop voltage gain can be shown to be[3]

$$A_V = gm\ R_L = I_S \frac{q}{kT} R_L = .001\ R_L \text{ at } +25°C$$

Since R_L is the parallel combination of the output impedances of Q6 and Q11, and is typically 4MΩ an open-loop voltage gain of 72dB is obtained.

The circuit design of the output stage insures that the maximum positive output swing never exceeds +4.3V. This is important when considering loop recovery from momentary overlaods which drive the PWM to maximum duty cycle. The peak value of the sawtooth oscillator waveform is +3.4V, and the error amplifier must slew from positive full scale to less than this voltage to reduce the duty cycle from maximum. Some error amplifier designs clamp the output voltage with a 6.3V zener diode, nearly tripling the recovery time from overload. Since all the voltage gain of the error amplifier takes place at the output pin, the amplifier can be easily frequency compensated at this node with shunt reactance to ground. The uncompensated amplifier exhibits an open loop pole at 350Hz and a typical unity-gain bandwidth of 2MHz.

Current Limit

The current limit amplifier has been redesigned to eliminate the two most common complaints about the original SG1524: limited input voltage range and slow response time. In the original design the ±1V common-mode range restricted current sensing to the supply return line only. In many systems, ground returns cannot be separated, making the current limit function unusable. Also, the internal frequency compensation provided freedom from oscillation at the expense of response time.

In the new design, input transistors Q1 and Q2 allow common mode voltages as low as -0.3V over the operating temperature range, allowing sensing in the ground line for configurations that require it. The upper limit is restrained only by the value of $+V_{IN}$, to which the level-shifter current sources I1 and I2 are referenced. The voltage drop across R2 creates a 200mV offset voltage at the amplifier input which provides the current sense threshold. The positive 0.2%/°C temperature coefficient of R_2 is balanced by a negative tempco for I2, effectively canceling effects of temperature on the current sense threshold.

Since both the allowable common-mode and differential voltages are much greater with this design, higher current foldback ratios can be achieved compared to the maximum of 3 or 4 possible with the earlier part. Also, the bias currents are a factor of 10 lower, resulting in more consistent limiting thresholds from unit-to-unit when foldback is employed.

Because there is no internal compensation capacitor, stability in the current limit mode will depend on external components. Due to the controller architecture, in which the output of the current limit amplifier overrides the error amplifier, these external frequency compensation networks may either be shared with the error amplifier or optimized for the current limit amplifier. The two choices are shown in the figures. In either case, the designer now has the freedom to optimize bandwidth for his particular switcher configuration.

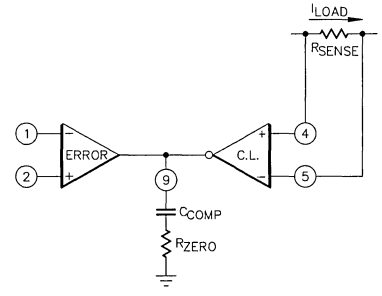

Figure 4. Current Limit Compensation in Comon With Error Amp

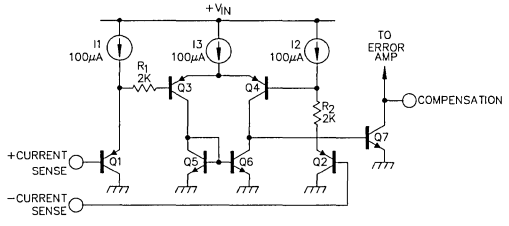

Figure 3. High-Gain Current Limit Amplifier

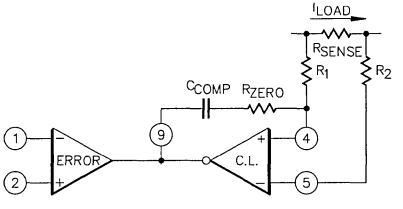

Figure 5. Current Limit With Optimized Frequency Compensation

Oscillator

The sawtooth oscillator circuitry of the SG1524B incorporates the same design improvements recently applied to the SG1524. These result in greatly improved external drive and synchronization capability, together with reduced sawtooth undershoot at high frequencies. In the original SG1524 design, an external synchronization pulse applied to the OSC pin did not generate a self-sustaining discharge cycle. The extent of the discharge of C_T depended on both the amplitude and duration of the external pulse. As a result, it was possible to generate erratic sawtooth waveforms with partial discharge cycles and pulse-to-pulse modulation of waveform endpoints. The frequency result was audible noise from subharmonics, transformer saturation, and destruction of the power transistors.

In the improved design, and external sync pulse which meets the minimum threshold requirements triggers a positive feedback circuit. This circuit drives the oscillator to end-of-discharge even if the external pulse is very narrow. Due to the feedback, there exists no in-between or quasi-synchronized state; the oscillator switches smoothly between free-running and synchronized modes as the external pulse amplitude is varied through the trigger threshold.

The positive feedback also effectively bootstraps the comparator gain, providing enhanced voltage swing and output current at Pin 3 to drive peripheral circuits. The improved oscillator design, together with a fast, DC-coupled toggle flip-flop, permits operation beyond 500kHz. However, the limitations associated with single-transistor outputs put a practical upper limit of 400kHz on the device.

Full Double-Pulse Suppression Logic

The PWM logic in the SG1524B insures that the output pulses always alternate from side to side, regardless of the action of the shutdown circuit. This is very important in push-pull switcher configurations where two pulses in succession on one side of the power transformer primary will cause core saturation and instantaneous failure of the power transistor.

The logic consists of two sections: a PWM latch circuit and a memory flip-flop. The latch allows only one pulse through per oscillator cycle. Once a PWM pulse is terminated, whether due to the normal PWM process or due to SHUTDOWN going high, the pulse cannot start again until the beginning of the next oscillator cycle. Pulse-by-pulse current limiting is easily accomplished now because of the latch feature and the completely digital (and therefore very fast) shutdown circuitry.

The memory flip-flop insures that output pulses always alternate from the output transistors. This is accomplished by generating a clock to the toggle flip-flop only if a PWM pulse was generated during the previous cycle. In the original 1524, the toggle flip-flop changes state with every oscillator pulse, irrespective of what the outputs are doing.

Figure 6 and 7 illustrate the difference in performance between two PWM control ICs, one with only a data latch and the other with the full double-pulse suppression logic described above. The triple-trace photos in each example show an alternating output pulse sequence interrupted by a SHUTDOWN command, followed a short time later by resumption of outputs from Emitters A and B. Oscillator frequency is 40kHz for each device, so 20kHz is obtained at the output transistors.

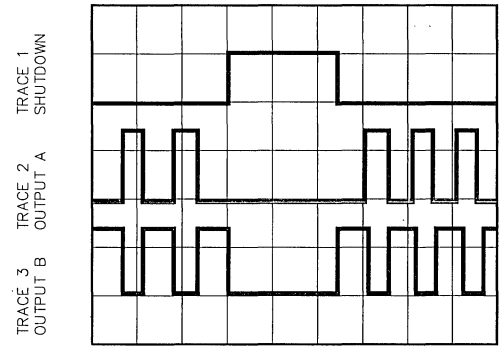

Figure 6. Output Sequence Without Double Pulse Suppression

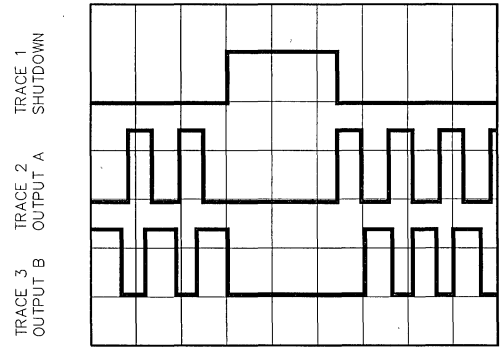

Figure 7. Output Sequence With Double Pulse Suppression

In the first case, the PWM pulses are alternating can BABAB when a SHUTDOWN signal inhibits the outputs for five oscillator cycles. When output resumes, the output sequence begins BABAB...Two pulses have occurred in succession from Emitter B.

With the second control IC, the PWM pulses are again alternating BABAB when a SHUTDOWN signal is received, again inhibiting output for five oscillator cycles. When SHUTDOWN is removed, output resumes but with an ABABA...sequence. The potential double-pulse from Emitter B has been eliminated by the internal pulse-steering logic.

This side-by-side pulse-routing problem exists for any PWM control IC with push-pull architecture and a fully digital shutdown function. In the original 1524 design, recovery from shutdown was fairly slow since the error amplifier output was pulled to ground for turn-off. Turn-on was limited by the 100μA output current of the error amp, the internal compensation capacitor in the current limit circuitry, and any external frequency compensation components. This created an inherent soft-start characteristic. With digital shutdown, the error amp voltage is not immediately affected; the first pulse out after shutdown can be the same width as before shutdown, making pulse-routing logic an absolute necessity to guarantee the safety of the power switches.

Output Transistors

In response to requests for greater output drive capability, the output transistors were redesigned for both higher breakdown voltage and more current.

In a PWM controller with a single-transistor output structure, the load driven is frequently one end of a center-tapped transformer primary winding. Since the maximum collector voltage is $2 \times V_{CC}$, the absolute maximum rating of 40V for the earlier device restricted the supply voltage to 20V. Consideration given to the effects of transformer leakage reactance would reduce this voltage still further. The SG1524B output transistors carry BV_{CEX} ratings of 60V, high enough for use on a standard +28V supply bus.

Output device geometry was scaled up to allow reliable operation at continuous collector currents of 100mA. This represents a factor of two improvement over the earlier device, which was characterized at only 50mA. As a further aid to the designer, the data sheet for the new device specifies maximum saturation voltage at two continuous current levels: 10mA and 100mA. The maximum peak current capability of the output transistors is 200mA for 1μS.

The anti-saturation clamp circuit around the output transistors found in the earlier PWM controller has been retained in the SG1524B to enhance switching speed. Each output transistor is also guarded against excessive current byprotective circuitry which limits the maximum continuous current to 150mA at +25°C.

DESIGN EXAMPLE

The functional usefulness of a new device is best demonstrated by study of an actual switcher design. The circuit described illustrates full control of a power supply with a single integrated circuit, resulting in reduction of overall cost and an increase in supply reliability through reduction of component count.

The circuit illustrated in Figure 8 is a push-pull, +28V to +5V converter operating at 50kHz. The power supply is unique in that the only active component is the SG1524B regulating pulse width modulator; the only other semiconductors required are diodes.

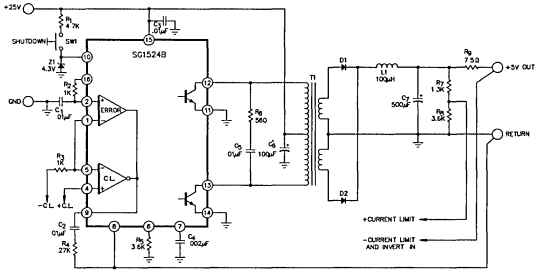

Figure 8. A Single IC 50 kHz Push-Pull Converter

The DC-coupled push-pull configuration was chosen because it is most sensitive to PWM controller anomalies which cause side-to-side imbalance. These include start-up problems such as output from only one driver until the toggle flip-flop begins to be correctly clocked by the oscillator. During normal operation, side-to-side imbalance of volt-second product due to unequal propagation delays in the IC can cause the onset of sore saturation. Finally, as outlined earlier, when the digital Shutdown control is activated, double-pulse sequencing can drive the excursion of the transformer core flux past the saturation knee of the BH loop.

Capacitor C3 acts as a high-frequency bypass for the IC supply line, while C6 is the high current reservoir for the power stage. The oscillator is set for 100kHz with C4 and R5. When divided by two by the action of the internal toggle flip-flop, this becomes 50kHz at the power transformer. The +5V reference is filtered against high frequency noise pick-up by R2 and C1, and applied to the non-inverting input of the error amp. The inverting input is connected to the power supply output terminals to form the negative feedback loop required for regulation. R3 minimizes the effects of input offset bias current by equalizing the source impedance seen by each error amp input terminal. Closed loop stability is provided by frequency compensation components R4 and C2, using the common technique of cancelling one of the two poles of the LC output filter with a open-loop zero in the error amplifier.[4]

In the power section of the supply, the two output transistors are used to directly drive a center-tapped transformer. A snubber network consisting of C5 and R6 modifies the inductive load line seen by each transistor. The transformer itself is wound on a small ferrite core; turns ratio is 3:1. Rectifier diodes D1 and D2 are

Schottky junction devices to maximize efficiency at +5V output. Filtering is provided by L1, wound on a permalloy powder toroid, and C7.

The improved common mode range of the current limit amp is used to good advantage here; current sensing is done directly in the output line. A foldback ratio of 7.5 to 1 is obtained with the given values R7, R8, and R9. The divider formed by R7 and R8 applies a back-bias of 1.3 volts, or 6.5 times current limit threshold, when the supply output is at +5.0V. Peak output current before onset of current limiting is 200mA, and short-circuit current is only 25mA. Rapid turn-off of the control circuit is accomplished by closing SW1. R1 and Z1 limit the maximum voltage applied to the Shutdown terminal to less than +5V.

While capable of only limited output power due to thermal limitations of the 16 pin Cerdip package, the supply amply illustrates the controller ability to perform all the major control functions required both during start-up, normal regulation, and overload.

CONCLUSION

In the past it was often necessary to incorporate additional components around the 1524 pulse-width modulator to enhance its capabilities, and to guard against various functional anomalies. Economically this was feasible due to the relative cost of the control device compared to the cost of the peripheral components.

With the occurrence of the usual price decline characteristic of most integrated circuits, the economic balance has shifted. Many users now pay more for the necessary support circuitry than for the 1524 itself.

The availability of the SG1524B now gives the designer another option. In many instances costly additional support components can be eliminated and a functionally superior device may be plugged directly into an existing design, with the benefit of simplicity, greater reliability, and reduced overall cost.

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4. Stan Dendinger, "Digital Current Limiting Techniques for Switching Power Supplies," POWERCONVERSION '80/ Munich, pp. 3A. 4-1 through 3A. 4-10.

SYNCHRONIZING THE SG1525A PWM

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Silicon General, Inc.

1. Synchronizing One Device to an External Clock

A. Program the SG1525A oscillator with R_T and C_T to free-run at a frequency 10% slower than the external clock frequency.

B. Drive the SG1525A SYNC terminal (pin 3) with the external clock. Input impedance is 2K. The clock amplitude should be greater than 2 volts and less than 5 volts. Pulse width should be at least 300nsec. for reliable triggering, but it should not exceed the free-running oscillator clock pulse width by more than 200nsec.

2. Synchronizing Multiple Devices to an External Clock

Two different methods are recommended, depending on the distance between the various SG1525A PWMs. Use method A if the ICs are within 3 inches of each other and on the same printed circuit board. Otherwise, use method B.

A. Designate one of the SG1525A PWMs as the master unit and select R_T, C_T, and R_D to free-run 10% slower than the external sync frequency. Connect all pins together and all OSC pins together, leaving R_T pins and DISCHARGE pins open on the slave units. Drive the SYNC pin of the master with a clock pulse as described in Section 1B above.

B. Program each of the separate devices with R_T, C_T, and R_D to free-run 10% slower than the external sync frequency. Drive each of the SYNC pins with the clock described in Section 1B. (This arrangement avoids routing a high-impedance line [C_T] around a noisy environment.)

3. Synchronizing One Slave Unit to a Master SG1525

As in Section 2, two methods are advised, depending on the distance between the master unit and the slave. Use method A for short distances, and method B otherwise.

A. Program the master unit for desired frequency with R_T, C_T, and R_D. Connect the C_T pin of the master to the C_T pin of the slave, and the OSC pin of the master to the OSC pin of the slave. Leave the R_T and DISCHARGE pins of the slave open.

B. Program the master unit for desired frequency. Program the slave unit to free-run 10% slower than the master. This is best done by choosing C_T and R_D to be the same as the master, and by increasing the value of R_T. Drive the SYNC pin of the slave with the OSC pin of the master.

4. Synchronizing Multiple SG1525A to a Master SG1525A

Again, different techniques are recommended depending on the physical and electrical distances between the various PWM circuits. If all of the devices are separated by no more than 3 inches each, and on the same pc board, then the "cluster" technique described in section 3A (i.e. sharing a master unit's C_T and OSC waveforms with adjacent slave units) will give good results.

If one or more of the devices are remote from the master so that the C_T node cannot be distributed without the possibility of noise pick-up, then each remote unit must be synchronized as described in Section 3B above. Note that it is possible to cluster remote units to decrease the required number of timing components. In other words, if two or more units are close together at one remote location, one of them can be programmed for the required 10% slower free-run frequency, and its C_T and OSC waveforms can be shared with its neighbors.

This description covers all the possibilities normally encountered. NOTE THAT IT IS ALWAYS GOOD ENGINEERING PRACTICE TO GROUND ANY UNUSED SYNC PINS TO ELIMINATE THE POSSIBILITY OF NOISE PICK-UP.

DIGITAL CURRENT LIMITING TECHNIQUES FOR SWITCHING POWER SUPPLIES

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ABSTRACT

This paper explores the performance benefits gained by digital techniques for current limiting in switch-mode power supplies. The necessary control architecture is described along with the several possible modes of operation. Characteristics of several actual supplies using these techniques are presented.

SUMMARY

Techniques for protecting switching power supplies against excessive output current demands have traditionally borrowed the analog approaches of linear voltage regulators. In many instances, the resulting performance has been unsatisfactory. Problems such as degraded load regulation, poor response to overloads, and oscillation at the crossover point between constant voltage and constant current output are frequently encountered.

A brief analysis of the properties of two coupled closed-loop control systems provides some insight into the basic limitations of the analog approach to current limiting. Specific examples using several currently available pulse width modulator circuits are shown.

An evaluation of the benefits of a digital approach shows that with the proper control architecture, all of the limitation imposed by analog techniques can be removed, with subsequent benefits to the power semiconductors. The impact on power device load lines and improvement in current limit characteristics are examined. Waveforms from operational switching supplies illustrate the practical applications of the principles discussed in this paper.

BACKGROUND

The architecture of almost all fixed-frequency, constant output voltage switch-mode power supplies can be reduced to the simple configuration in Figure 1. A sawtooth waveform is compared with the output voltage from an error amplifier, which in turn continuously compares a fraction of the supply output voltage with a precision reference voltage. The comparator output is a fixed-frequency, variable duty cycle pulse which drives a power switch. The power switch in turn chops the DC input voltage at some ultrasonic frequency. An output filter smoothes the bursts of energy into a low ripple DC voltage at the output terminals.

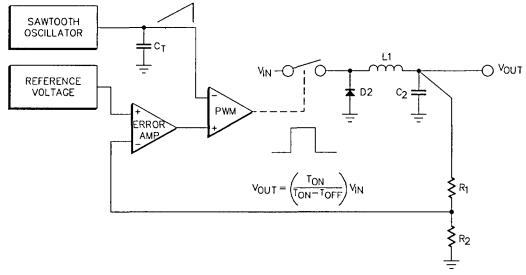


Figure 1. Basic Architecture of a Constant Voltage Switching Power Supply.

Under heavy loading, the voltage control loop forces the pulse width modulator to maximum duty cycle. In order to limit the maximum current flow and reduce operating stresses on the power components, it is necessary to limit the energy transfer through the power switch. The usual method in the past has been to establish a second feedback control loop. An overcurrent condition is sensed and the pulse width is reduced by overriding the voltage control amplifier, as shown in Figure 2.

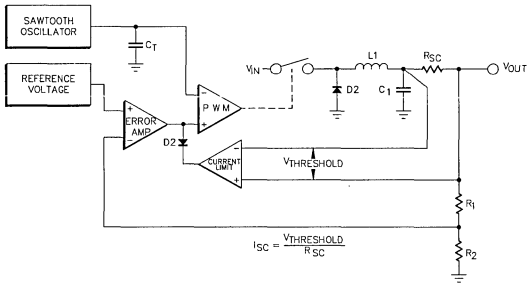


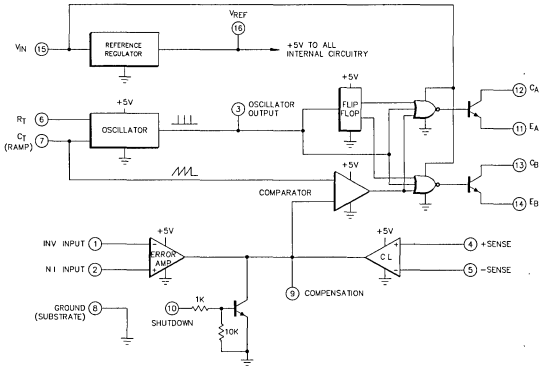
Figure 2. The Basic Switching Supply Modified for Analog Current Limiting.

In this configuration, a voltage amplifier with a fixed threshold or offset voltage derives a differential input signal from a current sense resistor in series with the supply output terminal. As the output current approaches the pre-determined limit, the amplifier enters its linear gain region, and its output voltage becomes increasingly negative. Diode D2 begins to conduct, clamping the error amp voltage to a low value and reducing the duty cycle of the pulse width modulator.

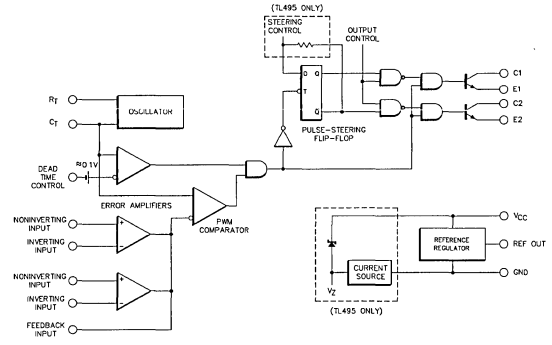
Examples

This method has been a popular solution to the problem of providing overcurrent protection. Figure 3 shows the control architecture of four integrated PWM circuits, all of which employ this analog approach.

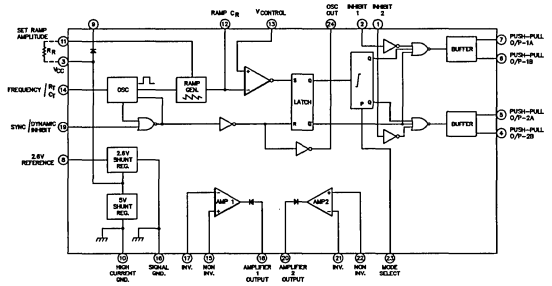
Despite the popularity of this technique, experience has shown that there are significant problems which result in degraded output regulation when compared to ideal current limiting characteristics. As shown in Figure 4, the supply voltage should be constant over



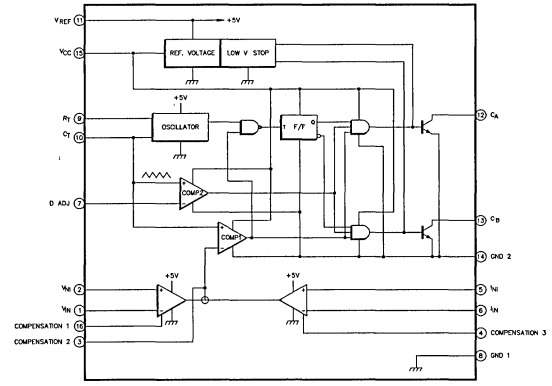
A. Silicon General SG1524



B. Texas Instruments TL494



C. Ferranti ZN1066



D. NEC Electron μPC1042C

Figure 3. Four Pulse Width Modulator Circuits with Analog Current Limiting

the full range of rated output current. At some excess current level, the supply should make a sharp transition to a current source. In actual practice with an analog current loop, load

regulation is degraded as the output current approaches the maximum rating. Furthermore once transition to current limiting has occurred, appreciable excess current can flow under short circuit conditions.

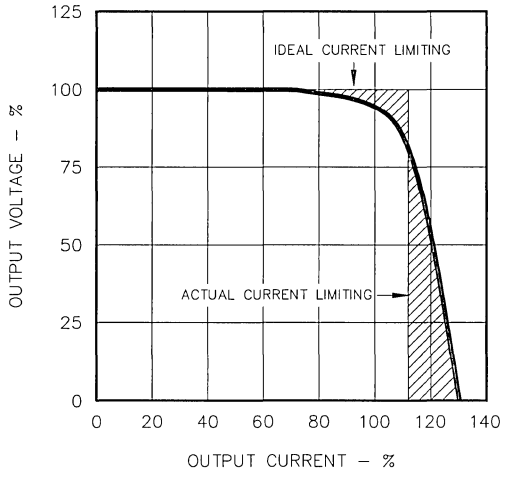


Figure 4. Load Regulation Characteristics of Supplies with Analog Current Limiting.

The reason for this non-ideal behavior is found in the finite loop gain of the current limit amplifier. Not only must the loop gain of the voltage control be opposed, but also the non-abrupt conduction of the clamp diode must be compensated. Higher gain can narrow the difference between actual and ideal performance, but at the risk of oscillation at the crossover point between constant voltage and constant current. To understand why this is true, we must analyze the frequency behavior of the gain elements in the two control loops.

Analysis of the Stability Problem

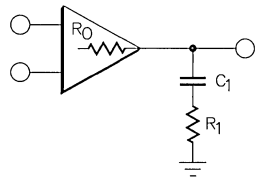
The three gain elements are the error amplifier, pulse width modulator, and current limit amplifier. The following notation is used: open-loop gains and frequencies are designated by lower case letters (a(s), s_b). Closed-loop gains and frequencies are denoted by upper case letters (T(O), S_1). The frequency compensation connections shown apply to the SG1524 and other transconductance amplifiers. The same compensation principles, however, also apply to low-impedance output amplifiers, where the feedback network is connected between the output and the inverting input terminal.

If the ratio of chopper frequency to the cutoff frequency of the output filter is at least 20, then the pulse width modulator may be modeled simply as a linear gain block. Its transfer function is given by:

$$a(s) = \frac{a(0)}{(1-s/s_c)^2} \qquad \text{(Eq. 1)}$$

where s is the complex frequency variable $\sigma + j\omega$
a(0) is the DC open-loop voltage gain

s_c is a double pole at $s = -\frac{1}{\sqrt{LC}}$

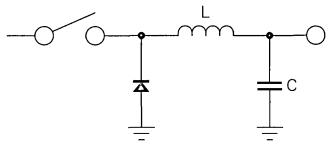


A. ERROR AMPLIFIER

$$a(s) = a(0)\,\frac{(1-s/s_B)}{(1-s/s_A)}$$

WHERE s_A IS A POLE AT $s = -\frac{1}{R_O C_1}$

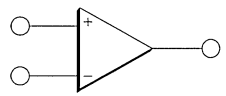
WHERE s_B IS A ZERO AT $s = -\frac{1}{R_1 C_1}$



B. PULSE WIDTH MODULATOR

$$a(s) = \frac{a(0)}{(1-s/s_C)^2}$$

WHERE s_C IS A DOUBLE POLE AT $s = -\frac{1}{\sqrt{LC}}$



C. CURRENT LIMIT AMPLIFIER

$$a(s) = \frac{a(0)}{(1-s/s_D)}$$

WHERE s_D IS THE SINGLE DOMINANT OPEN–LOOP POLE

Figure 5. Open-loop Gain Characteristics of the Three Gain Elements.

12

The error amplifier open-loop response is determined by external components C1 and R1 (Figure 5), since it is a transconductance amp with output impedance R_O. To obtain maximum closed-loop bandwidth for the voltage control loop, the designer must compensate the amplifier so that it exhibits an open-loop zero which cancels one of the poles of the low pass filter in the pulse width modulator.

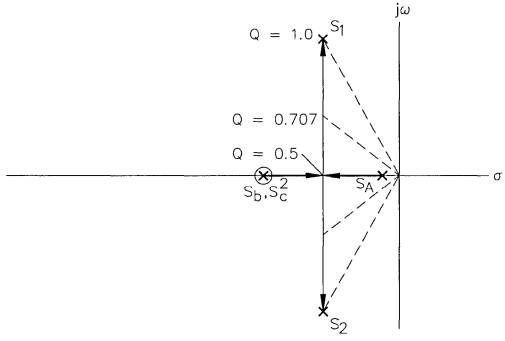


Figure 6. Trajectories in Complex Frequency Space of the Open-loop Poles and Zeroes of the Error Amplifier and Pulse Width Modulator as the Feedback Loop Gain is Increased.

The locations of the open-loop poles and zero for the voltage regulation loop appear in complex frequency space as shown in Figure 6. The dominant (lowest frequency) pole of the error amplifier (s_a), the open loop zero (s_b), and the two pulse width modulator poles (s_c) all lie on the negative real axis. Since there is a pole-zero cancellation, the net open-loop frequency characteristic is that of a two pole system, i.e.

$$a'(s) = \frac{a'(0)}{(1-s's_a)(1-s/s_c)} = \frac{a'(0)}{1+a_1s+a_2s^2} \qquad \text{(Eq. 2)}$$

When feedback is applied around the regulator, the poles move in complex frequency space along the trajectory shown. For low values of loop gain, the dominant poles remain real. When the loop gain T(O) exceeds $(a_1^2/4a_2)-1$, the poles become complex. They then follow a path parallel to the jω axis as T(O) increases. Note that the poles of the closed-loop transfer function always lie on the left hand plane, and so there is no stability problem. However if Q is much greater than unity the transient response may be unacceptable because of severe ringing.

At the transition point between voltage regulation and current regulation, the situation is quite different. The two feedback loops are now coupled together and oppose one another. A three pole system now exists, since the current limit amplifier now contributes a pole at s_d, so the positions of the poles in the s-plane are altered. If the bandwidth of the current limit amplifier is designed to be large (and ideally it should be to obtain rapid response time) then the paths of the poles s_a and s_c in the voltage loop will curve towards the jω axis, as shown in Figure 7. It can be seen that the net effect of coupling is that, for sufficiently high loop gain, the closed-loop poles S_1 and S_2 will cross over into the right hand plane, resulting in oscillation at the supply output.

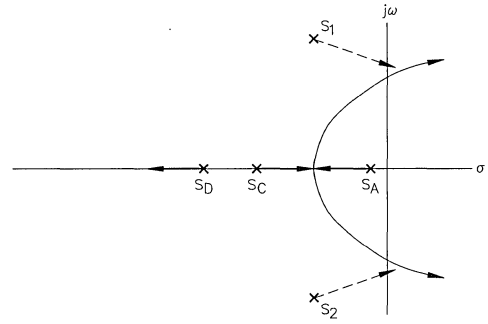


Figure 7. Movement of the Closed-loop Poles of the Voltage Regulation Loop Towards the Right Hand s-plane due to "Pole Mingling"

One method frequently used to stabilize the supply is to narrowband the current limit amplifier. For the case where

$$s_d = \frac{2}{s_a + s_c} \qquad \text{(Eq. 3)}$$

the closed-loop poles are forced away from the jω axis as the loops become coupled together, and no instability occurs. This condition is shown in Figure 8.

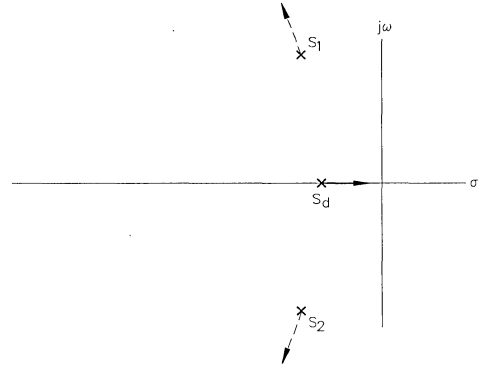


Figure 8. Movement of the Closed-loop Poles

$$\text{for } s_d < \frac{2}{s_a + s_c}$$

To summarize the situation, the switching power supply designer is faced with a dilemma. He can design the current limit circuitry for high gain to obtain a sharp limiting knee, and large bandwidth to obtain fast response time, at a substantial risk of oscillation.

Alternately he can avoid instability by designing for low gain, with resulting poor limiting characteristics: or he can slow the amplifier and risk destruction of the power switching devices. Clearly a new approach to the problem of current limiting is necessary to obtain better performance.

ANALOG CURRENT LIMITING
- Slow
- Degrades Load Regulation
- Potential Oscillation at Crossover
- Inflexible

A Digital Approach

A solution that bypasses all these difficulties is to monitor output current on a pulse-by-pulse basis. If an overcurrent condition is sensed during power switch conduction, the pulse is immediately terminated. The process is repeated at the beginning of each conduction cycle. To obtain the fastest possible reaction time, a digital node within the PWM architecture is chosen to inhibit the output pulse. Figure 9 illustrates one realization.

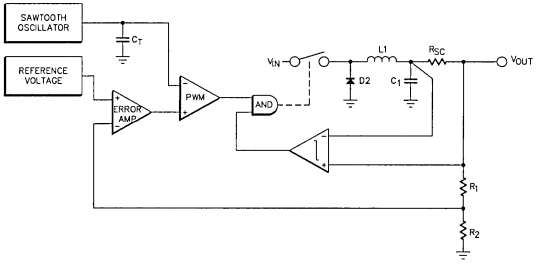


Figure 9. Current Limiting by Inhibiting the Output from the PWM Comparator.

A voltage comparator with fixed input offset voltage switches from a logical HIGH state to a LOW state when the selected current threshold is exceeded. Since both logic inputs to the AND gate must be HIGH to enable the output pulse, the pulse width can be narrowed by the current limit comparator independently of the voltage control loop.

One further refinement is necessary to ensure that multiple pulses cannot occur during one oscillator period. the block diagram as presently defined only *inhibits* the output during overloads, but does not prevent the pulse from turning on again when the overcurrent condition is removed. Switching noise could cause the comparator output to switch back and forth erratically, forcing the power semiconductors to switch many times through a high-power-dissipation load line during one oscillator cycle. The insertion of a data latch which is reset by a clock pulse from the sawtooth oscillator solves this difficulty. The data latch is designed so that a PWM pulse may ripple through asynchronously, but the trailing edge will lock up the flip-flop and prevent any further output until reset at the beginning of the next oscillator period. This final configuration is shown in Figure 10.

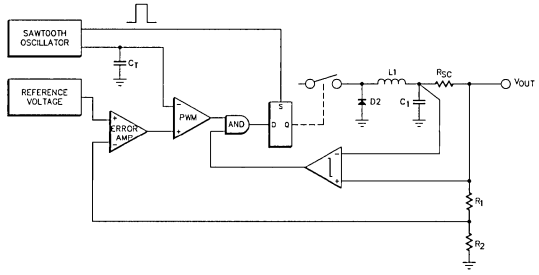


Figure 10. Addition of a Data Latch to Obtain Pulse-by-Pulse Current Limiting.

The theoretical performance of this configuration is shown in Figure 11. As load current increases from no-load to maximum load, no triggering of the current limit comparator occurs. The output voltage is affected only by the regulation of the voltage control loop. When the current limit threshold is reached, the comparator terminates each output pulse and the output voltage begins to decrease. As the load on the output increases, the overcurrent threshold point is reached earlier in each oscillator cycle. The pulse width will decrease to a minimum value determined by the propagation delay through the current limit loop. The storage time of the power switch is usually the dominant factor in this delay. Switch mode supplies which utilize power MOSFETs will exhibit the smallest pulsewidth due to the lack of any appreciable storage time. When the minimum pulse width is reached, the output current will increase as the load resistance decreases, since constant energy is being delivered to the LC output filter.

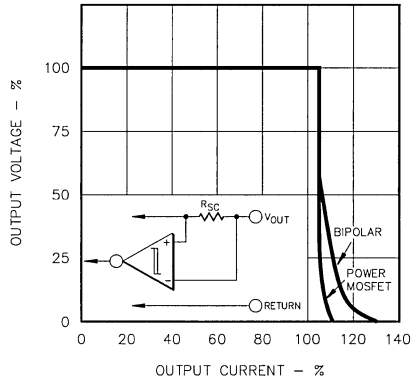


Figure 11. Theoretical Current Limiting with Bipolar and Power MOSFET Devices.

The excess current "tail" may easily be eliminated by foldback current limiting. This technique pre-biases the current limit comparator away from the threshold point with a fraction of the supply output voltage (Figure 12). As the supply voltage goes into current limit, the output voltage falls, reducing the bias on the comparator. Less current is then required through R_{SC} to maintain limiting. Finally, at full short circuit only a fraction of the full output current is available, even with the "tailing" phenomenon.

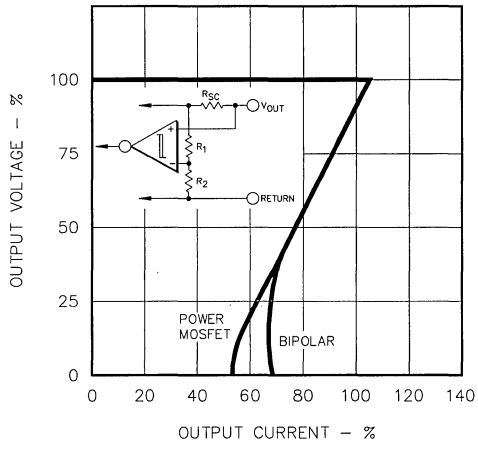


Figure 12. Reduction of Maximum Current Using Foldback Current Limiting.

The design equations for foldback limiting are straightforward:

$$I_{MAX} = \frac{V_{TH} + V_{OUT} R_1/(R_1 + R_2)}{R_{SC}} \qquad \text{(Eq. 4)}$$

where V_{TH} is the comparator threshold voltage

$$I_{SC} = \frac{V_{TH}}{R_{SC}} \qquad \text{(Eq. 5)}$$

Impact on Load Lines

Pulse-by-pulse current limiting also has a beneficial effect on switching device load lines. Data was collected on load line excursions of a 40kHz forward converter, with line results shown in Figure 13. The forward configuration was chosen rather than a flyback design because the output current is always in phase with the conduction of the principal power transistor. Thus load changes at the supply output are instantaneously reflected back to the load line excursion.

The normal load line trajectory indicates some deviation from the theoretical path due to non-ideal transformer characteristics. During turn-on, distributed capacitance in the transformer primary winding causes current overshoot. During turn-off, leakage reactance contributes some collector voltage overshoot.

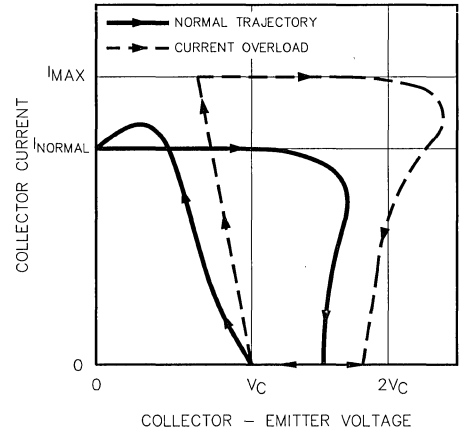


Figure 13. Prevention of Overcurrent in the Power Switch During Cycle-by-Cycle Current Limiting.

During a switching cycle where an overload exists, the collector current rises rapidly due to the low collector load impedance reflected from the power transformer secondary. Before the current can reach a destructive level, the conduction cycle is terminated, protecting the switching device from catastrophic failure due to damaged metalization or vaporized wire bonds. However, the collector voltage overshoot during turn-off is now greater due to the increased energy stored in the leakage reactance at higher current levels.

It can be concluded from the foregoing that pulse-by-pulse current limiting will protect the power devices from failure due to excessive current levels, but it offers no protection against abnormal leakage reactance voltage spikes. Their magnitude may be limited due to the imposition of a maximum value of current at turn-off, but some type of snubber network or other transient suppressor may still be required.

It is also apparent that device power dissipation is higher than normal during overload conditions. To avoid thermal damage an eventual transition from pulse-by-pulse limiting to "hiccup" mode current limiting may be desirable. "Hiccup" mode limiting occurs by discharging the PWM soft-start timing capacitor, causing the controller to turn off for several hundred milliseconds before resuming operation. An elegant method for controlling this transition by "fault counting" will be described at the end of this paper.

A Bipolar Example

To verify the actual limiting characteristics of a switch mode supply with digital current limiting, the 30kHz buck converter in Figure 14 was constructed. Almost all the control circuitry is contained within two integrated circuits and a power hybrid. The SM625 is a 60 volt, 15amp bipolar switch with matched commutating diode. It is controlled by an SG1524 pulse width modulator. The 2N2222 transistor provides constant current drive to the power switch over a wide range of input voltage.

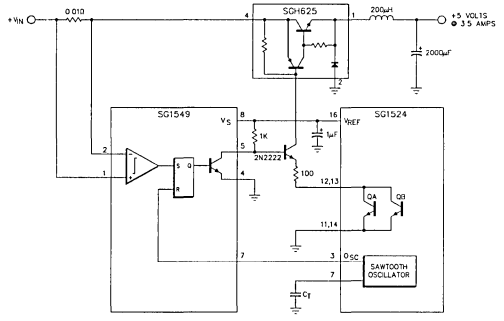


Figure 14. Buck Converter with Digital Current Limiting Using an SG1524 PWM and SG1549 Current Sense Latch.

Pulse-by-pulse current limiting is provided by an SG1549 Current Sense Latch. This circuit consists of two voltage comparators and a set/reset latch with Q and Q digital outputs. Both comparators have a 100mV threshold voltage. One device has full differential inputs with a common mode range from +2 to +40 volts. The second comparator has its 100mV threshold referred to ground, and is intended for sensing the voltage in an emitter resistor. This current sense configuration is desirable in forward and push-pull converters where secondary current overloads can be sensed by the reflection to the primary of the transformer. The two comparator outputs are ORed together at the SET terminal of the latch. A clock pulse from the oscillator output of the SG1524 is used to reset the latch. Maximum turn-off speed is obtained in this circuit by disabling the 2N2222 at its base with the open-collector LOW output of the SG1549.

Figure 15 shows the output voltage/current curve obtained with this regulator. The data points agree remarkably well with the theoretical curve for bipolar devices shown in Figure 11. The supply exhibits excellent load regulation (20mV) all the way to maximum load current, with a sharp, well-controlled transition to current limiting.

A MOSFET Example

To further illustrate the performance obtainable with present high performance switch mode power supply components, a 100kHz off-mains supply was designed with full input-output isolation, power MOSFETS, and an SG1526 pulse width modulator IC which incorporates the digital current limiting principles discussed earlier.

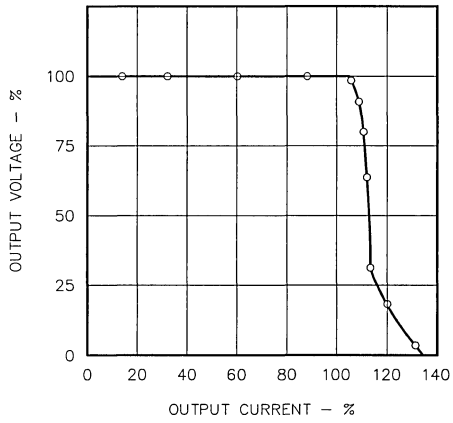


Figure 15. Output Characteristics of the Buck Regulator in Figure 14.

The block diagram of the PWM circuit (Figure 16) illustrates the differential voltage comparator, AND gate, and data latch that compromise the components for pulse-by-pulse current limiting. The comparator has a 100mV threshold and 20mV of hysteresis to minimize jitter at the decision point. The data latch allows only one pulse to pass through per each oscillator cycle. The memory flip-flop provides the double-pulse suppression logic. If the PWM pulse is gated off for more than one cycle, the flip-flop remembers which driver was the source for the last pulse. When the output is again enabled, the first pulse is automatically routed to the other driver. This prevents two pulses in succession from one driver, minimizing the possibility of transformer core saturation in push-pull configurations.

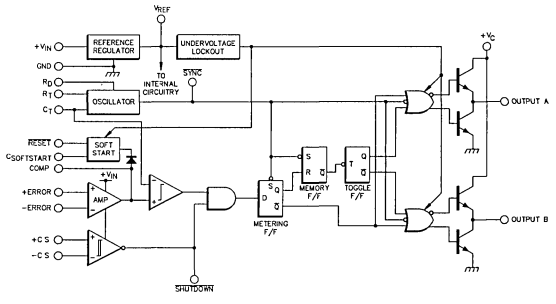


Figure 16. Block Diagram of the SG1526 Pulse Width Modulator

The complete schematic of the power supply is shown in Figure 17. A half-bridge configuration was chosen to minimize the drain-source breakdown voltage requirements on the power MOSFETs when operating from the rectified 220 volt European mains. Power for the SG1526 pulse width modulator is derived from a small (3 Watt) 50Hz power transformer. This arrangement maximizes supply efficiency and allows the voltage regulation loop to be referenced to the output ground. The two MOSFETs are driven from the secondary of a small ferrite pot core isolation transformer. The primary of the transformer is connected directly to the totem-pole output drivers of the SG1526. The oscillator is programmed for 200kHz by R_T and C_T and the current sense network is designed to give a 7 to 1 foldback ratio.

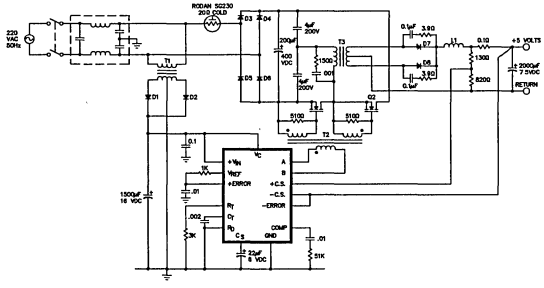


Figure 17. A 100 KHz Oof-line Power Supply Using the SG1526 for Digital Current Limiting.

Operational waveforms for the supply when operating under partial load are shown in Figure 18. The two traces show the unipolar gate drive signals at the pulse width modulator; these become bipolar when observed on the secondary of the isolation transformer. Transition edges are sharp and clean due to the totem-poles' ability to source or sink 200mA peak for charging and discharging the power MOSFET gate capacitance.

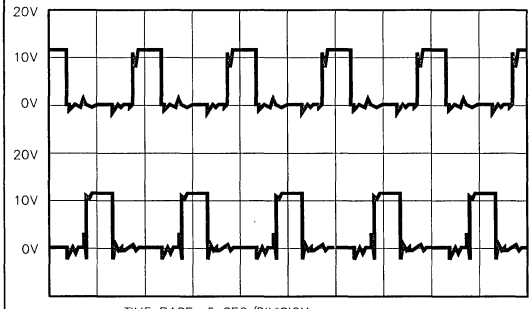


Figure 18

The propagation delay through the overcurrent control loop is of major importance when attempting pulse-by-pulse limiting at 100kHz. As Figure 19 indicates, the response time through the SG1526 from comparator to driver output is only 300 nanoseconds. Since this represents only 6% of the maximum duty cycle at 100kHz, a large foldback ratio is possible.

Data taken on the current limiting characteristics of this supply are shown in Figure 20. As expected, the output voltage regulation was completely unaffected by the current limit circuit until maximum load current had been exceeded. Also, the available output current steadily decreased as the overload increased, as would be expected from Figure 12. However, there was no current "tailing" effect from the loop propagation delay. The explanation appears to be that under prolonged pulse-by-pulse current limiting the power dissipation in the power MOSFETs is sufficient for the negative temperature coefficient of transconductance to override the effect of loop delay.

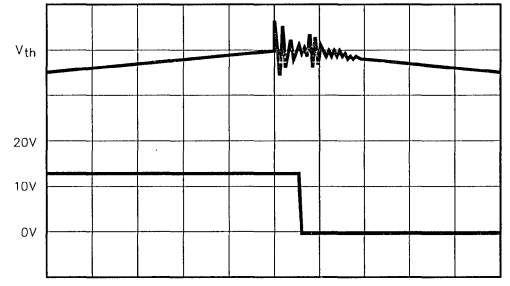


Figure 19

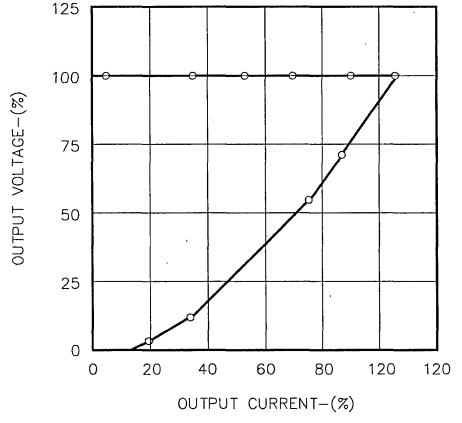


Figure 20. Measured Output Characteristics of the 100KHz Switching Supply in Figure 17.

Fault Counting Technique

Fault counting may be utilized to reduce power dissipation in the power switch during prolonged current limiting. One implementation is illustrated in Figure 21, using an inexpensive CMOS ripple counter and an even less expensive timer circuit. The 14-bit binary counter accumulates pulse-terminating commands from the SG1526 comparator. The output of the 14th stage will go high after 2^{13} or 8192 counts have been accumulated. At 200kHz (an overcurrent SHUTDOWN pulse can occur during either phase of the output) this represents 41 milliseconds of delay. When the counter output goes HIGH, the soft-start timing capacitor of the SG1526 is discharged. The SG555 timer is connected as an oscillator to periodically reset the accumulated count in the MC14020B, which allows a soft-start cycle to begin. A period greater than 41 milliseconds should be used.

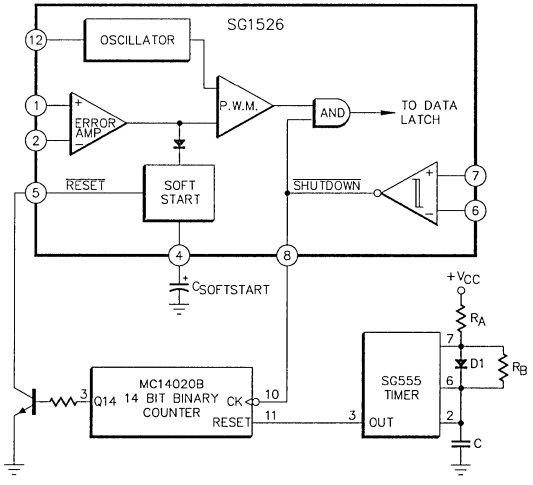


Figure 21. Using CMOS Logic as a Fault Counter to Control Transition from Pulse-by-Pulse Current Limiting to "Hiccup" Mode Current Limiting

Obviously this technique can be extended even further. A second counter could accumulate "hiccup" cycles and shut the supply off until manual reset or power re-cycle. This is easily accomplished with the SG1526 since the SHUTDOWN and RESET terminals are compatible with both TTL and CMOS logic.

DIGITAL CURRENT LIMITING
- Fast
- No Load Regulation Degradation
- Clean Crossover from Voltage to Current Output
- Multiple Current Limiting Modes Possible

Conclusions

The use of digital current limiting techniques provides enhanced load regulation, a sharp transition to constant current, and faster protection to the power semiconductors in a switch-mode power supply when compared to analog methods. It also offers the designer flexibility in the choice of crossover criteria from pulse-by-pulse mode to "hiccup" mode to total shutdown. The net benefit to users will be enhanced reliability and increased performance from switch-mode power supplies.

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FETs ENHANCE SWITCHED-MODE DESIGNS

ABSTRACT

Switched-mode power supplies are well known for their high levels of efficiency and for their compactness. Further improvements can be effected by employing power MOSFETs in place of conventional bipolar transistors. A practical design for a 5V, 20A supply is suggested utilizing the SG1526.

Many of the basic design concepts relating to power MOSFETs were outlined in an earlier article "Designing with power MOSFETs," which was published in the March, 1982 issue of Electronic Product Design.

Now let us apply some of the driver techniques discussed in the earlier article, to a 100kHz, 100W switched-mode power supply. Fig. 1 shows the circuit which is truly universal in that it operates directly from a mains voltage spanning 85V to 265V r.m.s. without any mechanical switching requirements. And furthermore, it is able to perform this task over a wide frequency spread, typically from 50 to 400Hz.

SIMPLICITY OF DESIGN

At the centre of the design is a 500V, 3A power MOSFET (Q1) which converts the rectified mains voltage into a tightly-controlled 100W d.c. output. Apart from the indicated rectifiers and Zener diodes, the power FET and its regulating pulse-width modulated driver IC (SG1526) are the only active devices needed to achieve a full-load efficiency of 74 per cent with ±0.5 percent regulation. This particular design has a maximum output current of 20A d.c. at 5V with a maximum ripple of 50mV pk. -pk. Transient response for a step change of 10A load current is 500mV, settling within 250μs.

MORE EFFICIENT

For a given combination of voltage and current ratings, power MOSFETs can generally switch more efficiently and at much higher frequencies than their bipolar counterparts. Because power MOSFETs can be operated at higher frequencies, smaller transformers and filter capacitors can be used leading to more compact designs. The circuit shown in Fig. 1, for example, operates at 100kHz, some two and a half times faster than most circuits using bipolar transistors.

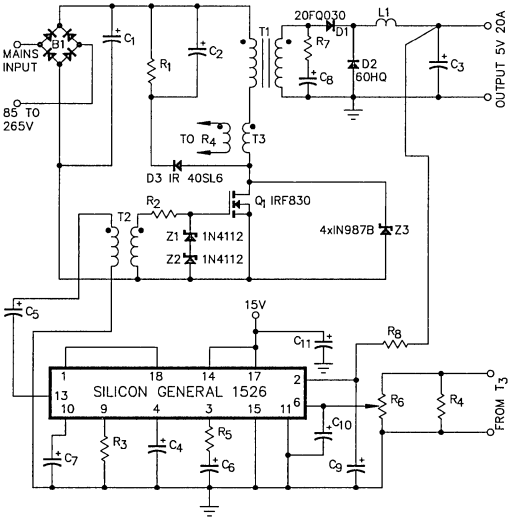


Figure 1. Versatile 100W Switched-Mode Power Supply Offers 20A Output with 75 Percent Efficiency and a Tight Performance Spec.; See Text for Details.

The higher operating frequency also enables the circuit to recover much more quickly from severe line or load variations. This is especially important in situations where a system's power-up signal is used to reset a large number of logic devices simultaneously.

Driving a power MOSFET is in most cases much easier than driving an equivalent bipolar device, it being voltage rather than current driven. Some gate drive is of course required, but at a much lower level than that associated with similarly-rated bipolar devices.

MODIFICATIONS

The power MOSFET is not directly compatible with the bipolar power transistor and cannot be used in a switched mode circuit without modification.

Irrespective of the power switching device used, be it a MOSFET or a bipolar power transistor, the associated pulse-width modulated switcher cannot normally be left on for more than 50 per cent of the total duty cycle. Under normal circumstances, a 50 per cent on time occurs only when the input voltage is very low and the output current is high. Conversely, the shortest on times occur when the input voltage is near to its peak and the output current is minimal.

Ideally, the pulse-width modulator should operate over a very wide duty cycle range to ensure close regulation with wide line and load extremes. Unfortunately, it has been impracticable to implement this approach in bipolar designs, since the gain of bipolar transistors decreases rapidly when operated in the short-pulse, high-current mode.

A power MOSFET's transconductance, on the other hand, does not vary so widely with current changes. This makes it much easier to drive a MOSFET directly, using a short duty cycle. Furthermore, the short conduction time at high input voltage leaves a relatively long time to reset the associated transformer and thus reduce the peak voltage across the MOSFET. Also the designer is able to use 500V rated devices in mains driven supplies in contrast to the usual 800V rating often needed for circuits featuring bipolar devices.

PROTECTION

Some protection is of course necessary. The MOSFET shown in Fig. 1, for example, features clamping diodes (Zener diodes 1 and 2) to limit the circuit's maximum gate voltage to 18V. Zener 3 which comprises four series-connected 120V diodes, restricts the source/drain swing to 450V to give a safe working margin.

The resister/capacitor/diode snubber formed by $R_1/C_2/D_3$ conforms in the principle to the approach outlined in the earlier article, except that it is allowed to float. For more details on this and other related topics, refer to International Rectifier's application note AN-939.

Trials have shown that worst-case efficiency occurs at virtually maximum input voltage with minimum loading. Here efficiency drops to just under 70 percent, compared with 76 percent at maximum output. Dissipation is thus around 8W at maximum output and slightly higher than this value when the supply is lightly loaded.

OPERATION

The off-screen photographs show how the circuit functions. Fig. 2 demonstrates how the pulse-width modulator controls the MOSFET's conduction time with respect to various load and line conditions. At one extreme, the input voltage is down to 85V, while output is at 20A. Fig. 2a shows the MOSFET on for 4us which gives a duty cycle of approximately 44 percent. When operating at the other extreme, ie 265V input and 5A output, the MOSFET is on for approximately 1us, which corresponds to a 10 percent duty cycle. Note how the gate/source waveforms which are depicted in Fig. 3 relate to the operating levels shown in Fig. 2.

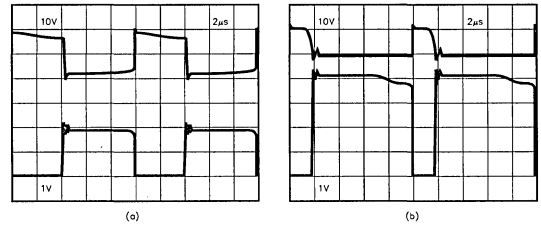


Figure 3. Gate/Source Waveforms. These Were Recorded with the Unit Under Full Load, (a) with a Line Voltage of 85V and (b) with a Line Voltage of 265V. The Upper Traces Show Gate/Source Voltage While the Lower Show Drain Voltage.

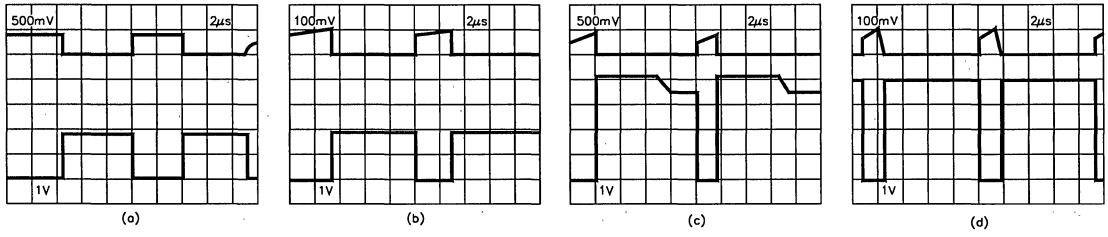
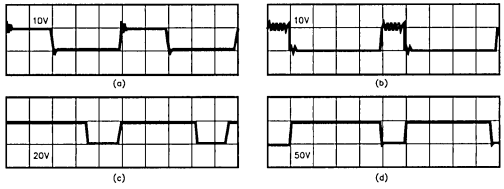


Figure 2. Switching Waveforms. With an 85V Line and a 20A Load (a) Shows Drawn Current on the Upper Trace and Drain Voltage on the Lower. The Load is Cut to 5A in (b), While (c) and (d) Show the Same Parameters at a 265V Line Voltage with Respective Loads of 20A and 5A.

Typical voltage waveforms across the output rectifiers are shown in Fig. 4. Note that while the forward rectifier D1 blocks a peak voltage (including the commutation transient) of about 12V, D2 has to withstand around 75V for a 5V output, due to the short conduction cycle. Both of these diodes contribute to the system's net losses. Indeed, these devices dissipate some 30 to 50 percent of the switching energy, and represent a major problem in designing low output voltage power supplies. Losses from the rectifier diodes are approximately the same for both the 5 and 15V supply designs.



TRACE	PARAMETER	CONDITIONS	VERTICAL	HORIZONTAL
a	D_1 VOLTAGE	35V LINE	10V/DIV	
b	D_2 VOLTAGE	5A LOAD	20V/DIV	2μ SEC/DIV
c	D_1 VOLTAGE	265V LINE	20V/DIV	
d	D_2 VOLTAGE	5A LOAD	50V/DIV	

Figure 4. Output Circuit Waveforms. The Upper Traces Show the Voltage Waveform Appearing Across D1, While the Lower Covers Rectifier D2. In Both Cases, Load is at 5A; (a) with the Input Voltage at 85V and (b) at 265V.

POWER SUPPLY CIRCUITS HEAD FOR SIMPLICITY BY INTEGRATION

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Manager, Advanced Product Development
Silicon General, Inc.

SUMMARY

The benefits obtained from switching power supplies have become universally recognized by power systems engineers in the past several years. However, there has been a simultaneous realization that, too frequently, gains in efficiency and reductions in weight have been accompanied by an escalating component count and a decrease in reliability and predictability of performance. To effectively solve these problems, integrated circuit manufacturers have recently designed new products specifically for switchers. These devices offer the proven advantages of monolithic technology: compactness, accuracy, reproducibility, higher performance through reduction of parasitics, and the economies of mass production.

This paper reviews the circuit simplifications made possible by these specialized devices, as typified by the first practical switching regulator control chip, the SG1524 Pulse Width Modulator, and later by other circuits such as the ZN1066, the TL494A, and the MC3420. A second potential area of power supply simplification is the interface between the control circuit and the high power switching transistors. Two specialized driver circuits, the SG1627 and the SG1629 are described which provide high-level turn-on and turn-off signals for efficient switching. Finally, some second and third generation pulse width modulator designs will be discussed. These later devices, designated the SG1525/27 series and the SG1526, offer even higher levels of control function integration compared to earlier designs. The SG1526 in particular integrates a number of protective control features which substantially increase the reliability of the power semiconductors in "real world" switching power supplies.

HISTORICAL PERSPECTIVE

A basic pulse width modulated switching power supply requires only four control elements: a precision reference voltage, a ramp oscillator, an error amplifier, and a differential voltage comparator. Each of these elements has been available in integrated circuit form for years, with the well-established benefits of reduced physical size, greater reliability, and increased performance. In light of this background, the development of a single monolithic circuit for switching power supply control appears to be a logical progression.

One of the first devices available to power supply designers was the SG1524 Pulse Width Modulator from Silicon General. This circuit, shown in Figure 1, contained all of the basic control elements required for a switching regulator. In addition to providing the four basic control elements, the device allowed for push-pull configurations by inclusion of a toggle flip-flop and dual alternately-gated output transistors. Finally, provision was made for some abnormal power supply operating conditions. An analog current limit circuit and a digital shutdown control were included to provide protection against short circuits and other load faults.

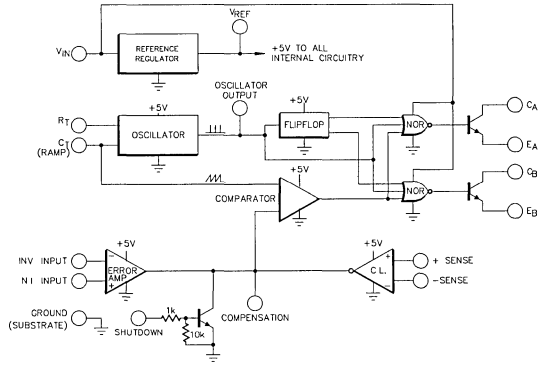

Figure 1. SG1524B Pulse Width Modulator Block Diagram

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Despite this level of complexity, the device was easy to understand and was quite flexible. As a result, since its introduction in 1976, the SG1524 has been very widely accepted within the power supply industry, finding its way into a majority of new designs, including exotic applications in communications satellites and the space shuttle program.

POWER DRIVER INTEGRATION - SG1627

As experience was gained in applying the SG1524, it became apparent that there was a gap between output power capabilities of the control integrated circuit and the drive levels required by the power semiconductors. Two areas were identified within most supply configurations where specialized driver functions could be successfully implemented with monolithic technology.

An integrated Source/Sink Driver

The first design is a dual 500mA totem pole driver with externally programmable current sourcing. Both inverting and noninverting logic inputs are available, and may be driven by either an open-collector control circuit or (with a diode) by TTL logic. Connections to the high current output transistors are brought out separately, allowing maximum flexibility when interfacing with standard bipolar transistors, the new VMOS power FET's, and transformers.

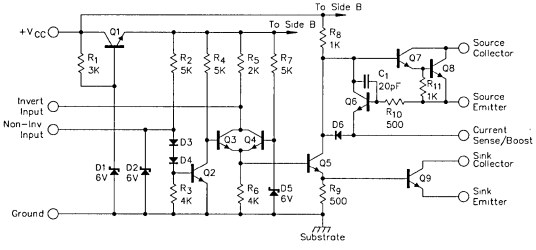

Figure 2. Partial Schematic Diagram SG1627 Driver Circuit

Power Bipolar Drive is accomplished with the connection shown in Figure 3. R2 controls the magnitude of forward base drive, and is selected to develop a voltage drop of one V_{BE} when the output Darlington pair is sourcing 350mA. At the same time R3 develops a 3.5 volt differential, which is stored by C1. During turn-off, sink transistor Q9 saturates, pulling the output terminal to ground. The emitter-base junction becomes reverse biased from a low impedance source, allowing stored base charge to be rapidly extracted.

Power FET Drive is possible with a minimum of external components. The source/sink capability of the SG1627, together with its fast edge speeds, makes it an ideal driver for power MOSFET devices. Although MOSFETs have negligible DC gate current, input capacitances of 800,-1000pF exist in the higher current units. Since this capacitance must be charged and discharged by 10 or 12 volts in 10 to 20 nanoseconds, high peak currents are required. At switching frequencies of 200kHz, considerable dynamic power dissipation is required of the drive circuit to obtain the high speed switching benefits of these devices.

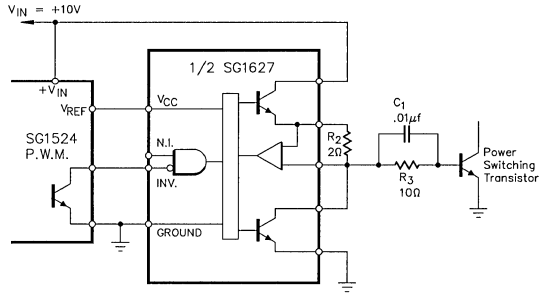

Figure 3. Driving Bipolar Junction Transistors With a Totem-Pole Switch Driver

In Figure 4, peak currents in the output stage are limited by R_2, while R_1 helps minimize power in the SG1627. With some power FETs, a 100ohm resistor in series with the gate lead may also be necessary to eliminate device oscillations.

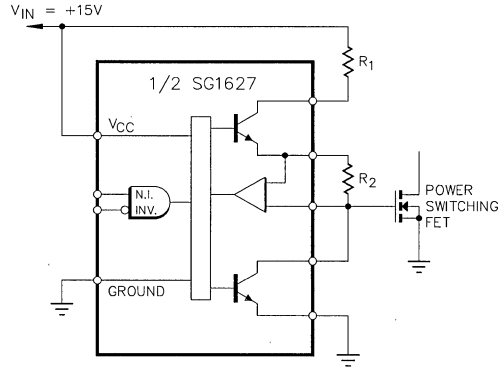

Figure 4. A Source/Sink Driver Provides the Peak Currents Required by Power Fet's at High Switching Frequencies

Transformer Drive is the third interface area where an integrated power driver can eliminate components. Most bi-phase transformer drive circuits using grounded emitter transistors require additional components to reset the magnetic flux to zero every half cycle. This is necessary to insure that no net DC excitation is applied to the transformer primary over many cycles of operation, thereby avoiding core saturation. These additional components

may include extra transformer windings, clamp diodes, and anti-phase driven clamp resistors. A much less complex circuit can be achieved with the SG1627, as shown in Figure 5.

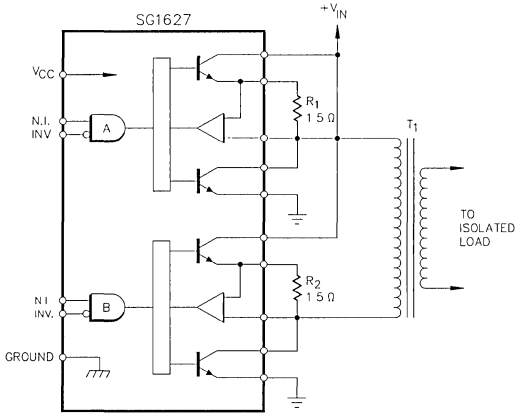

Figure 5. The Low Impedence of the SG1627 in Both On and Off States Allows Direct Transformer Drive With a Minimum of External Components

In this circuit the transformer primary voltage-driven by the source/sink output structure of the SG1627. Core reset to zero occurs automatically during deadtime, when both ends of the primary winding are switched to ground. Resistors R_1 and R_2 serve as over-current protection for the driver in case of control malfunction or onset of core saturation due to load faults on the secondary. No center tap is required, resulting in elimination of winding balance problems.

AN INTEGRATED FLATING SWITCH DRIVER - SG1629

The second interface considered was that between the secondary winding of a drive transformer and the base-emitter junction of an NPN power transistor. This configuration is frequently found in off-line converters, where a half or full bridge design is chosen because of the high input supply voltage. In this case the design problem consisted of providing controlled forward base drive to the power device during the positive polarity of the secondary voltage, and a fast negative peak current for rapid switch-off during the negative portion of the cycle. No power other than that provided by the transformer secondary should be required, so that the power device can be floated above ground by several hundred volts.

The circuit shown in Figure 6 is a modification of a discrete design developed by Pete Wood while at TRW semiconductors[1]. During a positive cycle, base current flows from the drive transformer secondary winding through a source transistor which can be programmed for current limiting. A center tap on the secondary completes the circuit for returning base drive current. At the same time, external storage capacitor C_S is charged to a negative value through the high current rectifier diode in the switch driver. When the secondary voltage is driven to zero, the rectifier diode becomes reverse biased. The resulting positive drive turns on the Darlington sink transistors, which reverse-biases the base-emitter junction of the power device through the storage capacitor. A large negative current spike results, minimizing the turn-off time and power loss in the switching transistors.

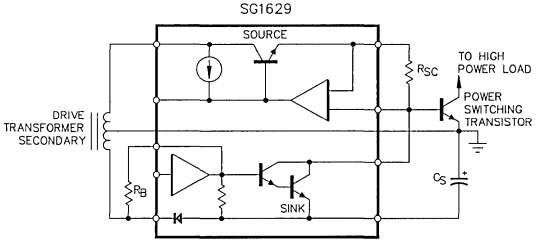

Figure 6. SG1629 Floating Switch Driver Block Diagram

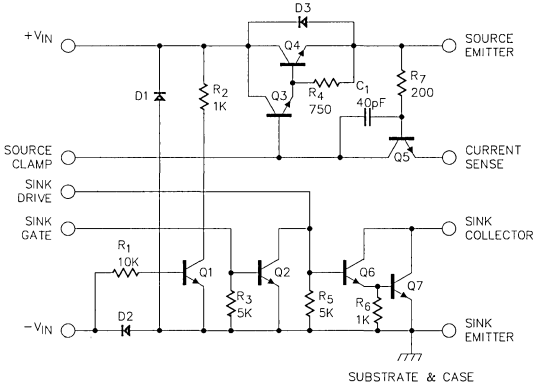

Figure 7. SG1629 Floating Switch Driver Schematic Diagram

As the detailed schematic of the SG1629 in Figure 7 indicated, in addition to the high current Darlington source and sink transistors the circuit also contains several gating options for the sink or turn-off section of the driver. Source transistors Q3-Q4 and sink transistors Q6-Q7 are designed to 2 Amp collector currents. Base drive to the source is provided by R_2, while Q5 provides current limiting. On the sink side of the circuit, base drive to Q6-Q7 is normally provided by a resistor connected to Pin 3. Q1 senses the polarity of the input voltage and gates the source transistor off between each drive current pulse. This action allows the external

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storage capacitor to be charged even at very low duty cycles, since the discharge current during the "off" portion of the drive cycle becomes negligible. The sink gate input is used when the risetime of base turn-on current is important, and transformer inductance is a significant limiting factor. Methods for using this feature are found in the SG1629 application note[2].

Power Drive Summary

Two integrated power drive circuits designed specifically for use in switch-mode power supplies have been reviewed. These devices provide the necessary power gain between a complex low-power control circuit and high voltage, high current switching semiconductors, while offering greater performance in a reduced volume compared to discrete component design. Monolithic technology will provide even higher levels of voltage and current handling capability in the future as soon as semiconductor packaging technology solves the problem of providing large pin-outs in a high power dissipation package.

A SECOND GENERATION PULSE WIDTH MODULATOR CONTROL CIRCUIT - SG1525A/SG1527A

As switch-mode power supplies gained in popularity, a demand was made by power supply design engineers for an integrated circuit that offered all of the functions of a control device and the interface capabilities of a power driver. The SG1525A series of pulse width modulators represents a combination control IC and power drive. The control section is based upon the time-proven architecture of the SG1524, while the output stage of this device combines many of the elements of the previously discussed 1627 power driver. At the same time, improvements were made within the architecture of the control chip to include even more functions than were originally available on the 1524.

The internal reference regulator on the chip is trimmed to an accuracy of ±1% compared to the original ±4%. Secondly, the chip now contains on-chip shutdown and soft start circuitry. The only external components required are an external timing capacitor. A third area of improvement is in the common mode range of the error amplifier. By designing the error amplifier so the common mode range now includes the 5.1V of the reference, a reference divider network is no longer necessary, thus eliminating two external resistors. The oscillator circuitry has been redesigned to make deadtime control easier and multiple device synchronization easier. Finally, the output stage has been redesigned so that, instead of a single transistor which is periodically turned on for pulse width modulation, an output source/sink driver or totem-pole type design is used. Since this particular driver has the characteristic of low impedance in both the on and off states, it becomes much easier now to interface the control circuits with external power transistors including standard bipolar junction devices, the new power FETs, and also drive transformers.

The new family of regulating pulse width modulators is designated the SG1525A/1527A series of devices, and the device block diagram is illustrated in Figure 8.

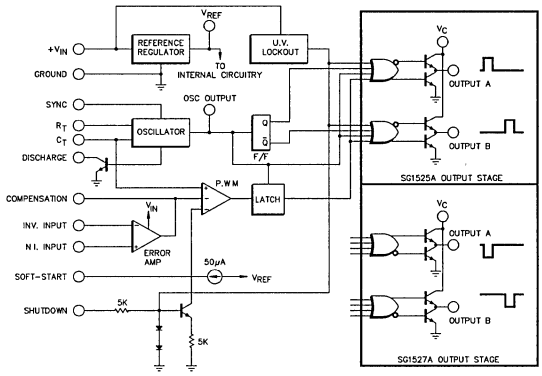


Figure 8. Block Diagram of a "Second Generation" Pulse Width Modulator Family: The SG1525A/1527A Series

The trimmed reference regulator, which has an output voltage of 5.1V, not only acts as the reference terminal for the error amplifier control loop, but it acts as a power source for all the internal circuitry, with the exception of the error amplifier and the output drivers. The oscillator determines the basic operating frequency of the pulse width modulator circuit. An external R_T and C_T are the components that are fixed to set this frequency. Additionally, deadtime is controlled by the insertion of a small amount of resistance between the discharge terminal (Pin 7) and the C_T terminal (Pin 5) on the oscillator. The oscillator circuit has two outputs: the ramp waveform, which is applied to the positive input of the pulse width modulation comparator, and a periodic positive-going pulse at the oscillator output pin which acts as the toggle signal for the flip-flop. It is also used as the deadtime control pulse for the output gating logic.

The totem-pole output drivers are designed to easily interface with either single ended or push-pull types of switching power supply configurations. There are two output polarities available with this series of pulse width modulators. In the 1525A series, the output gating is designed with NOR logic, which results in a positive-going output pulse during active time. The 1527A series uses OR logic, so that the active state is a low ground state. This particular polarity of output is useful in certain types of proportional base drive circuits in which feedback from the power transformer is used to provide base current, thereby compensating for variations in transistor beta.

Soft Start Circuit

The equivalent of the SG1525A/1527A soft start circuitry is shown in Figure 9. An external capacitor $C_{SOFTSTART}$ provides the timing element for the soft start cycle. This capacitor is charged via a 50microamp current source internal to the chip. The P.W.M. comparator has two inverting inputs, and the more negative of the two voltages determines the duty cycle. During undervoltage conditions on the V_{IN} line, current is forced through the two diodes in Q1's base circuit. A voltage of approximately $1^{V}BE$ appears across Q1's emitter resistor, resulting in a collector current of approximately 100μA. Since the charging current available is only 50μA, the soft start capacitor is held in a discharged state. Because the voltage at pin 8 is 0, the PWM comparator ignores the signal from the error amplifier, and zero duty cycle is obtained. When the controller supply rises to 8 volts the discharge current is turned off, and the voltage on pin 8 rise linearly, resulting in gradually increasing duty cycle. Eventually the capacitor charges up very close to the reference voltage and the duty cycle is controlled by the error amplifier. If the voltage on the shutdown pin is raised above ±1.5 volts the capacitor is slowly discharged at the same rate it is normally charged.

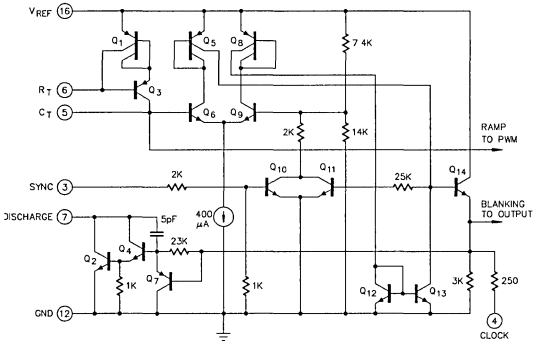


Figure 9. SG1525A/1527A Softstart Circuit

Oscillator Description

The circuit for generating of the timing ramp waveform is shown in Figure 10. The timing capacitor C_T receives a constant charge current from the compound current mirror formed by Q1 and Q2. The R_T terminal voltage is two V_{BE} less than the reference voltage, so that a resistor tied from Pin 6 to ground sets up the charging current for C_T. Transistors Q5 through Q10 form a voltage comparator which constantly compares the voltage at C_T to either a +3.3V or +1V reference, depending on the state of the comparator. The timing capacitor C_T is discharged via the Darlington formed by Q3 and Q4.

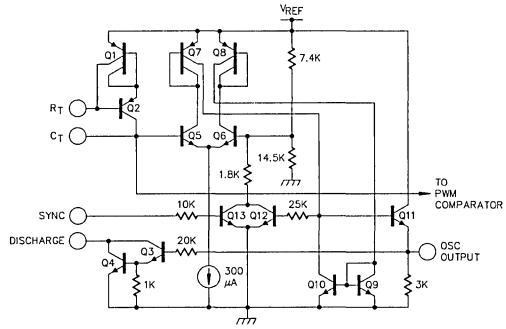


Figure 10. SG1525A/1527A Oscillator Schematic Diagram

When the voltage on C_T is less than +3.3V, the discharge network does not conduct and C_T receives a constant charge via the current mirror, resulting in a linear increasing voltage. When the +3.3V trigger level is reached, the comparator changes state and turns on the discharge network. This rapidly removes charge from C_T so that voltage falls towards +1V, at which time the comparator changes state again and another cycle begins. The discharge time of C_T is used to generate the blanking pulse at the oscillator output pin. The deadtime or pulse width at the oscillator output pin may be increased from its minimum value of approximately 400 to 500 nanoseconds by a resistor between the discharge pin and Pin 5, which lengthens the discharge time of C_T during the second half of the oscillator cycle.

A positive pulse at the sync pin will initiate a discharge cycle in the oscillator. This pin then forms a convenient connection for synchronizing the IC to a frequency supplied by an external system clock.

Output Driver

A simplified schematic of the output gating and the power output stage of the 1525A is shown in Figure 11. Transistors Q1, Q2, and Q3, together with a 500 microamp current source, from a logical NOR gate where the pulse width modulation signal from the pulse width modulation comparator, the deadtime pulse from the oscillator, and one side of the toggle flip-flop are combined. Q4 is an amplifier with active load which inverts the output signal from the NOR gate. Q5, in turn, acts as the phase-splitter transistor for the push-pull output. When Q5 is on, its emitter current drives the base of Q8, holding the output low. At the same time, the collector of Q5 is also low, thereby back-biasing Q6 and Q7, the output pull-up devices. When Q5 turns off, its collector voltage rises, turning on the output Darlington. At the same time, Q8 turns off and the output terminal is pulled up towards the V_C supply. Diode D1 acts

to protect the base emitter junction of the upper Darlington against reverse breakdown. D2 acts to provide extra base drive current to Q8 during turn off. If a capacitive load is present on the output terminal, D2 will turn on and the extra collector current of Q5 will then be routed to Q8 so that Q8 in turn will be turned on harder, thus discharging the output capacitance and enabling the output to fall rapidly to zero.

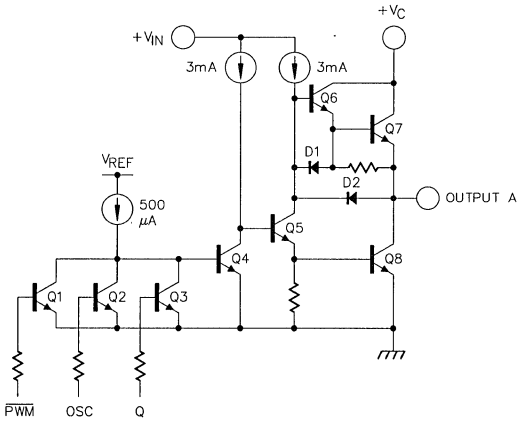


Figure 11. SG1525A Pulse Width Modulator Power Output Stage

The source and sink transistors Q7 and Q8 in this driver are designed to provide more than 100mA of current handling capability. In most cases, the full current capability will not be used in a steady state condition to drive an external load but rather the peak current capability can be used to provide rapid charging of external capacitance loads, thereby providing very fast rise and fall times at the output driver.

Figures 12 and 13 illustrate the speed capabilities of the output drivers when driving power MOSFETs, in this case a pair of Siliconix VN64GA devices. The upper traces show the driver output voltage swing for a collector supply of +12 volts. The lower waveforms are the 0-5amp drain currents of the FETs. Switching times of 100 nanoseconds were achieved by driving the gates directly from the totem pole outputs, and by limiting peak currents to 200mA with a 62ohm resistor at the $+V_C$ terminal. Faster times can be obtained with the higher current SG1627 Power Driver.

The ultimate frequency capabilities of the output drivers as a function of ambient temperature for a given VMOS load is shown in Figure 14. For this graph, a $+V_C$ supply of 12 volts was assumed. An effective power FET input capacitance of 1000pF on each driver was also assumed. A thermocouple attached to the ceramic dual-in-line package allowed junction temperature to be calculated based on a worst case θ_{JC} of 60°C/W and a θ_{JA} of 100°C/W maximum.

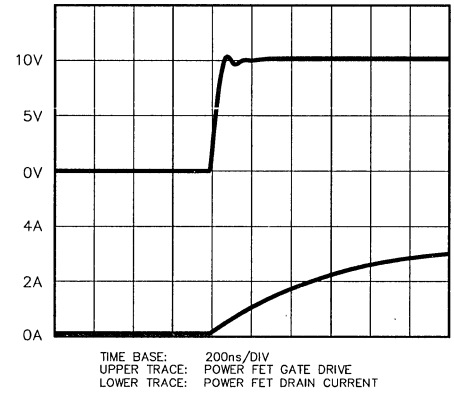


Figure 12. SG1525A/Power Fet Turn-On Wave Forms

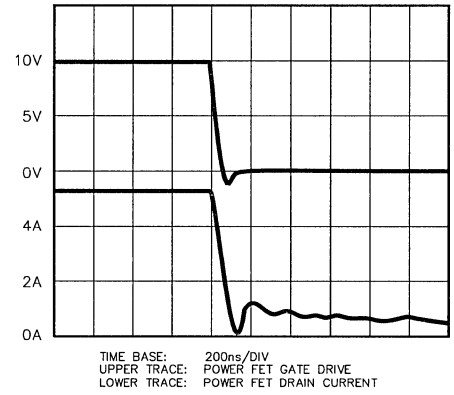


Figure 13. SG1525A/Power Fet Turn-Off Wave Forms

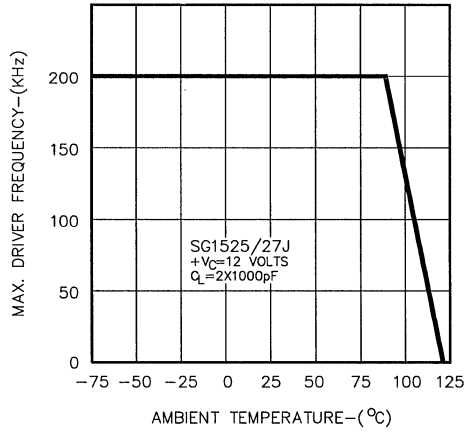


Figure 14. SG1525A/1527A Power Fet Drive Capability

For ambient temperatures below 90°C, the maximum frequency allowable is determined by the maximum possible oscillator frequency of 400kHz. Above 90°C operating frequency and dynamic power dissipation must be reduced to keep the junction temperature from exceeding +150°C. Different supply voltages, capacitive loads, and heat sinking will result in other temperature limits.

It will be noticed in comparing the block diagram of the SG1525A/1527A family to that of the SG1524 that there is no provision made directly for current limiting on the 1525A/1527A. The reason for this is that this chip is designed to interface with a new output supervisory circuit, the SG1543. This device has an extra comparator with adjustable offset which can be used for providing the current limit function in conjunction with the SG1525A/1527A. Additionally, this particular chip has the capability for providing under and overvoltage protection for the remainder of the power supply.

A THIRD GENERATION SWITCHING POWER SUPPLY CONTROL CIRCUIT - SG1526

- Supply operation to 40 volts
- Reference trimmed to ±1%
- Sawtooth oscillator with deadband control
- PWM comparator with hysteresis
- Undervoltage lockout
- Programmable soft start
- Wide error amp common mode range
- Wide current limit common mode range
- Two modes of digital current limiting
- Double pulse suppression logic
- Single pulse metering logic
- Symmetry correction capability
- TTL/CMOS compatible logic
- Dual 100mA source/sink output drivers

Table 1. Desirable Features of a High-Performance Pulse Width Modulator

An ideal circuit for switching power supplies should include not only the elements necessary for normal pulse modulation operation, but also the full range of abnormal operations. Ideally, the circuit should contain as many protective features as possible for the power semiconductors. If a table of parameters were constructed for such device, it would look much like that shown in Table 1. Analysis of the features in the table would show that most of the new features are control related and are therefore ideally suited for inclusion in an integrated circuit, where a great deal of complexity can be easily compressed into a very small area. Just such a device has been designed by Silicon General, and the block diagram of that device is shown in Figure 15.

As can be seen, the four basic elements of the pulse modulator are present: a reference regulator, error amplifier, sawtooth oscillator, and a pulse width modulation comparator. Of particular interest are some new features in the block diagram: an undervoltage lockout, soft start circuitry, digital current limit comparator and digital signal processing logic between the pulse width modulation comparator and the output power drivers.

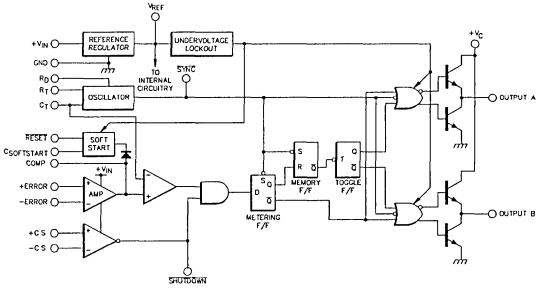


Figure 15. SG1526 High Performance Pulse Width Modulator Block Diagram

The operation of the circuit is as follows: An on-chip regulator trimmed to 1% is both reference voltage for the error amplifier, and also the stabilized power source for all the internal circuitry, with the exception of the error amplifier, the current limit comparator, and the output drivers.

The sawtooth oscillator is programmed for a specific frequency and deadband by values of R_T, C_T and R_D. The resulting ramp waveform is applied to one side of the pulse width modulation comparator, which has been designed with a very small amount of hysteresis to prevent oscillations at the comparison point. The other terminal of the PWM comparator is connected to the output of an error amplifier which has been designed with a common mode range that includes both ground and the 5V reference.

Also associated with the amplifier is on-chip soft start circuitry. This soft start circuitry is controlled not only by an external RESET terminal, but also by the undervoltage lockout circuitry. If the reference voltage should be less than the 5V required for normal linear operation of the control circuitry, the RESET terminal in the soft start is held low by the undervoltage lockout, thus preventing the soft start capacitor from charging. At the same time, the power output drivers of the device are inhibited. thus making it impossible for spurious output pulses to occur during undervoltage conditions.

The digital output of the pulse width modulation comparator is ANDed with the output of the current limit comparator. This provides very fast response to overcurrent conditions. The current limit comparator has a fixed input offset of 100mV plus a slight hysteresis of 20mV to eliminate indecision at the threshold point. The PWM signal from the AND gate is followed by three levels of pulse processing logic. It first passes through a metering

flip-flop whose function is to allow only one output pulse per oscillator cycle, thus eliminating oscillations and permitting pulse-by-pulse current limiting. The second element is a memory flip-flop. This flip-flop is part of the double pulse suppression logic and prevents two pulses in succession from one output driver, independent of conditions on the SHUTDOWN terminal, RESET terminal or error amplifier inputs. Also included is a toggle flip-flop which alternately gates first one driver and then the other in the presence of a PWM signal.

The final elements in the block diagram are the source/sink output drivers, with a separate collector supply voltage terminal brought out for additional flexibility.

A simplified version of the undervoltage lockout circuitry is shown in Figure 16. The circuitry consists of a 1.2V bandgap reference and a voltage comparator which are fully operational for reference voltages greater than 2.1V. When the reference voltage is greater than 2.1V, the output transistor is turned on, inhibiting both power output drivers. It also holds the RESET line controlling the soft start circuitry in the low state, thus preventing the soft start capacitor from charging, and guaranteeing zero duty cycle.

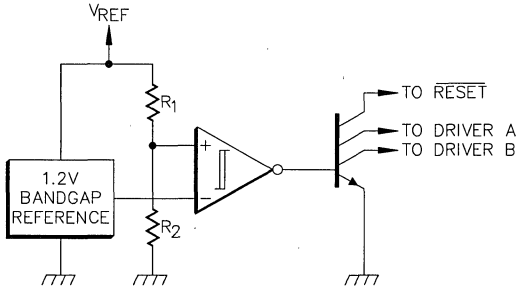


Figure 16. The Undervoltage Lockout Circuit Contains a Bandgap Reference and Comparator Which Becomes Active at V_{REF}=3 V_{BE}≈2.1 Volts

Resistive divider R_1 and R_2 is scaled so that when the reference voltage reaches 4.5 v the comparator changes state, thus releasing the soft start capacitor and also enabling the power drivers. Approximately 200mV hysteresis is built into the comparator so that the transition from lockout to fully on is not accompanied by indecision and jitter.

Monitoring the reference voltage rather than the input terminal voltage has an additional benefit. With this particular configuration, this chip can operate on +5V by connecting the V_{IN} terminal to the $V_{REFERENCE}$ terminal and then regulating the input voltage between 4.5 and 5.5 volts. This is a desirable feature where other supply voltages must be generated from a regulated +5V source.

A simplified schematic of the oscillator of the 1526 is shown in Figure 17. A new approach is taken for controlling deadtime in the circuit. The principle of operation is similar to the 1524 and 1525 oscillator. A timing capacitor is charged via a constant current programmed by an external resistance R_T. When the capacitor has charged linearly up to a nominal 3.2V, a voltage comparator changes state, thereby turning on a discharge network which reduces the capacitor voltage very rapidly to the +1V level. The distinctive difference between the oscillator in the 1525 and that in the 1526 is that the discharge network is a current source instead of a semi-saturating Darlington. In the 1526, the discharge circuit is formed by a compound current mirror, Q3, Q4, and Q5. The output current of this current mirror is ratioed to the current charging in C_T by a ratio of 30:1. This results in a charge time to discharge time ratio of approximately 29:1 independent of the value of C_T. This ratio can be modified to give longer deadtimes by insertion of a small amount of resistance from Pin 11 to ground. With this technique, deadtimes up to 50% or more are easily obtainable. The oscillator configuration has the advantage that the minimum deadtime for the oscillator is now fixed at approximately 3% independently of the frequency of the circuit.

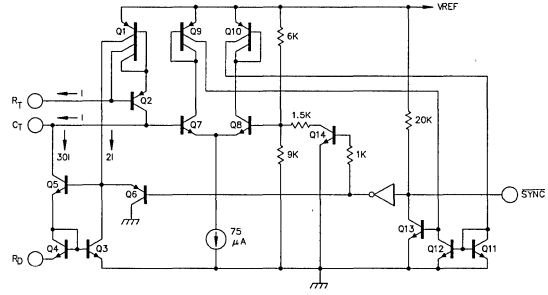
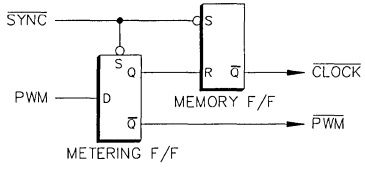


Figure 17. The SG1526 Oscillator Provides Deadband Control By Rationing The Charging Currents to C_T

The remainder of the oscilator circuit functions similarly to that of the 1525. One notable exception is the TLL compatible buffer gate between the SYNC output pin and the remainder of the circuit. This enables the port to be bi-directional, driven either by open-collector TTL or by open-drain CMOS, or to itself drive other TTL or CMOS logic.

Figure 18 contains a brief explanation of the pulse processing logic in the 1526. The logic consists of two specialized flip-flops: a metering or data latch flip-flop, and a set/reset or memory flip-flop, The metering flip-flop is basically an asynchronous data latch which is enabled by a sync pulse from the oscillator during the beginning of every oscillator cycle. Once the metering flip-flop is enabled, a PWM signal may pass asynchronously through the device. However, once the signal is terminated for any reason, no

new pulse can propagate through the data latch until a new sync pulse is received at the beginning of the next oscillator cycle. This feature allows each individual pulse to be terminated either by the action of the current limit comparator or by external circuitry which pulls the SHUTDOWN pin low. This feature allows the SHUTDOWN pin to be a convenient input port for a strobe pulse from symmetry correction circuitry.



METERING FLIP-FLOP		MEMORY FLIP-FLOP	
DESCRIPTION:	ASYNCHRONOUS DATA LATCH	DESCRIPTION:	SET-RESET FLIP-FLOP
FUNCTION:	ALLOWS ONLY ONE PWM PULSE PER OSCILLATOR PERIOD	FUNCTION:	REMEMBERS WHICH OUTPUT PRODUCED LAST PULSE
BENEFIT:	SUPPRESSES HIGH FREQUENCY OSCILLATIONS	BENEFIT:	INHIBITS DOUBLE PULSING IN PUSH-PULL CONFIGURATION

Figure 18. SG1526 Pulse Processing Logic

The function of the memory flip-flop is to generate the clock pulse for the toggle flip-flop, which alternately gates the two output power drivers. It operates as follows: Let us assume that the flip-flop begins operation in the reset state. When a sync pulse is received from the oscillator, the Q terminal is then driven low, generating a clock pulse for the toggle flip-flop, which then changes state. If a PWM signal is generated during the oscillator cycle, then the flip-flop is reset, thus enabling it to generate another clock at the beginning of the next oscillator cycle. If no pulse width modulation signal is generated because the duty cycle has gone to zero or SHUTDOWN has been pulled low, then the memory flip-flop will not be reset, and when the next sync pulse occurs, no clock will be generated. In this way, the output flip-flop is toggled only upon generation of pulse width modulation signals, thus rendering it impossible for two successive pulses to be obtained from one output driver.

The operation of the metering logic in the 1526 is shown in more detail in the timing diagram in Figure 19. The top waveform, Waveform A, shows the SYNC pulse train from the oscillator. This pulse train divides four timing periods, T_1 through T_4, as shown at the bottom of the timing diagram. Waveform B represents the ramp signal from the master oscillator, while Waveform C represents the analog output signal from the error amplifier. These two waveforms are differentially compared in the pulse width modulation comparator, whose output is shown as Waveform D. It can be seen that the error amplifier output voltage is just slightly less than the peak of the ramp signal approaching nearly full duty cycle. Waveform E is a SHUTDOWN signal from the current limit comparator. Alternately, this line could also show a digital input signal from other control logic. The waveform at line F represents the ANDed output of the PWM comparator and the SHUTDOWN signal. This acts as the date input to the metering logic flip-flop, whose output is shown as Waveform G.

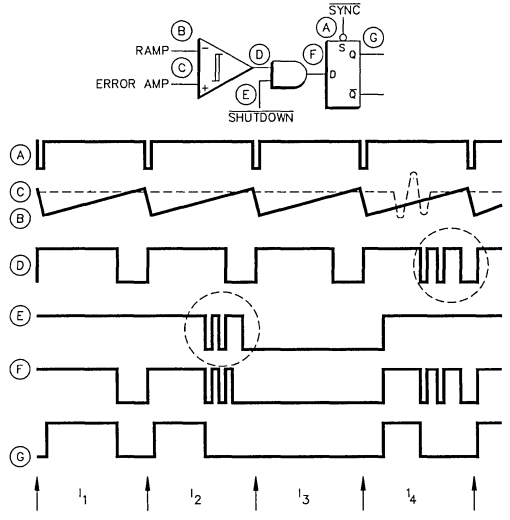


Figure 19. Timing Diagram of the Pulse Processing Logic Over Four Oscillator Cycles

The first time frame, T_1, illustrates a normal period of operation. The error amplifier calls for nearly full duty cycle; the SHUTDOWN pin stays high, and this output signal then passes unaltered through the metering logic flip-flop. During the second time frame, the SHUTDOWN pin is pulled low for several times during the active pulse period. This results in a series of pulses being applied to the data input of the metering logic flip-flop, but as can be shown in Waveform G, once the first pulse is terminated no other pulse can begin until the next oscillator cycle. During time frame T_3, the SHUTDOWN pin is low, thus preventing and PWM signals from reaching the metering flip-flop. In the fourth time frame, the disturbance at the output of the error amplifier causes multiple ramp crossings, which generates multiple PWM signals during one oscillator cycle. These signals reach the data input of the metering flip-flop, but as before, once the first pulse is terminated, the remainder of the pulses cannot propagate through the device to the output drivers.

The combination of source/sink drivers with a separate collector supply voltage terminal allows the output drivers to be easily interfaced with all the circuit configurations found in mot switching power supplies. Figure 20 illustrates the connections for a common emitter push-pull configuration. In this circuit, the

collector supply to the output source/sink drivers is tied to the supply voltage through R_1, which limits the voltage swing of each driver output, preventing emitter-base breakdown. During the turn-off cycle, an additional spike of reverse base current is generated by the speed-up capacitor C_1 or C_2.

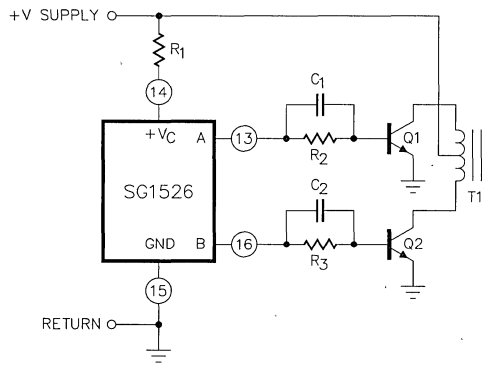


Figure 20. Basic Connections For a Push-Pull Grounded-Emitter Configuration

Buck-type converters are easily interfaced to the totempole output devices. For this mode of operation it is necessary only to ground the output terminals A and B, and drive the base of the switching device with the collector supply terminal. In this configuration, the upper Darlington resistors are alternately turned on and pull Pin 14 to ground, thus providing up to 100mA of current drive capability on alternate oscillator cycles.

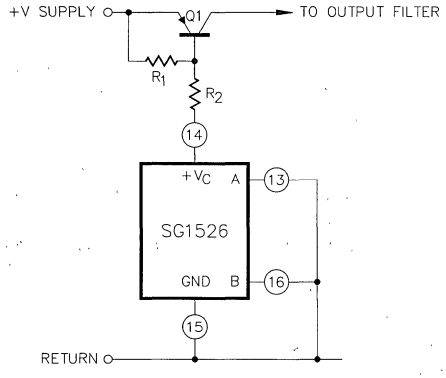


Figure 21. For Single-Ended Configurations the V_C Terminal is Alternately Switched to Ground by the Driver Pull-Up Transistors

The totem-pole outputs can also drive a transformer directly, as illustrated in Figure 22. Since each output driver exhibits a low impedance, no center tap winding is required on the transformer primary. In this example, the transformer drive capability is used to interface the control device with the power transistors in a half bridge configuration.

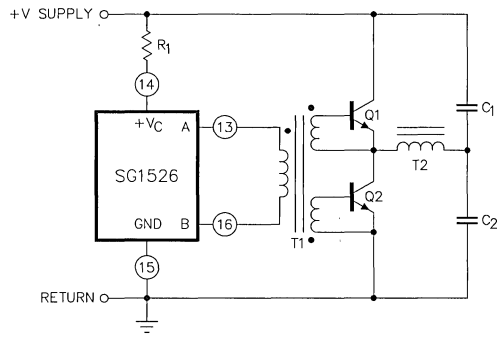


Figure 22. Low Power Transformers are Driven Directly by the Output Terminals

If an additional current drive capability beyond that available in the 1526 is necessary, it is very easy to interface the output totem-pole drivers with the 1627 dual 500mA driver circuit. This is shown in Figure 23.

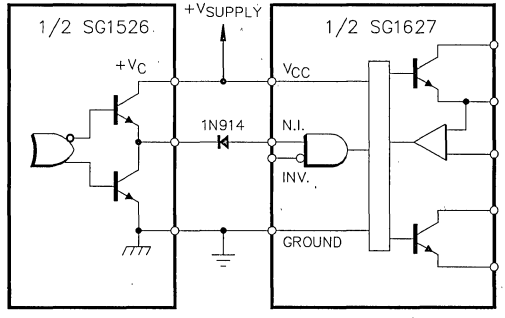


Figure 23. The Totem-Pole Outputs of the SG1526 can be Interfaced to the SG1627 Power Driver With a High-Speed Switching Diode

The logic threshold of the 1627 is a nominal +2V, while the sink current in the low state is about 1mA. A fast silicon switching diode such as a 1N914 can be used to provide a sink current path in the low state, while blocking excessive input current to the power driver during the control circuit's high state.

The ability of one control port of the 1526 to drive another control port enables a good deal of flexibility from the chip. The flyback converter in Figure 24 illustrates this point. Current limiting in a flyback converter is difficult because the overcurrent signal from

the current sense resistor is always out of phase with the conduction of the principle power transistor. In this circuit, the output of the current limit comparator in the 1526 is used to re-trigger the soft start circuitry. By choosing the value of the soft start capacitor so that the recovery time of the soft start circuitry is of the order of one or two cycles, it is possible to provide current limiting with a minimal number of external components. This same technique can be used in a push-pull converter where it is desirable for the pulse width modulation signal to be turned off for multiple oscillator cycles rather than for a single cycle. This allows overstressed output semiconductors a cool-off period before returning to normal operation.

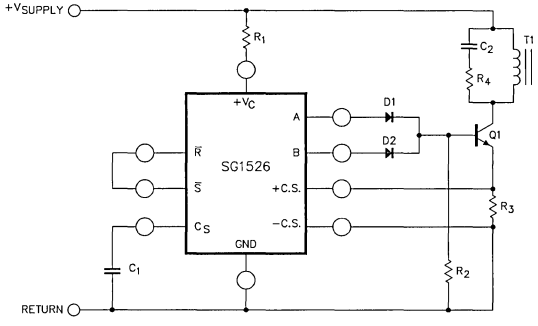


Figure 24. Using the SG1526 in a Flyback Converter With Current Limiting

CONCLUSION

Several integrated circuits designed specifically for switch-mode power supply control have been described. A brief review has been made of past approaches to the integration of switching power supply control and driver circuitry. A description of a newly available family of control/driver integrated circuits, the SG1525/1527 series, has been given. Finally, a sketch of a future high performance controller circuit, the SG1526, has been drawn.

The future of integrated circuits for switching power supplies clearly involves greater complexity in the control circuitry to account for all possible modes of supply operation. The benefits for the power supply designer will be greater performance and reliability from switchers with reduced component count and greater overall manufacturing economies.

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1. Peter N. Wood, "Design of a 5 Volt 1000 Watt Power Supply," TRW Power Semiconductors Application Note 122A, February, 1976.

2. Robert A. Mammano, "Power Switch Drivers: New IC Interface Building Blocks for Switched-Mode Converters," Powercon 5 Proceedings, May, 1978.

SG1825 DESIGN BRIEF: A 200KHz CURRENT-MODE SUPPLY

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INTRODUCTION

To demonstrate the high-speed capabilities of the new SG1825 Pulse Width Modulator, a small 200 KHz switching power supply was designed and constructed. A push-pull current mode architecture was chosen because of its inherent anti-saturation properties. This choice of more efficient magnetic structure and the 200 KHz switching frequency allowed the transformer bulk to be minimized.

DESIGN SPECIFICATIONS

Input Voltage: +22 to +32 VDC
Output Voltage: +5.0 Volts
Output Current: 0.5 to 2.0 Amps
Line Regulation: ± 1%
Load Regulation: ± 1%
Output Noise and Ripple: 50 mV RMS
Full Load Efficiency: 73%
Total Weight: 10 oz.

CIRCUIT DESCRIPTION

The circuit uses a bootstrap winding and the micropower start-up capabilities of the SG1825 to efficently provide controller supply voltage. Typical start-up current is only 600 μA, an improvement of 2.5 over alternate-source controller ICs.

When the +28 volt input is applied, the 680 μF start capacitor is trickle-charged by the 2.7K bleeder. While the controller is in micropower mode, the driver outputs are switched to ground, providing protection against leakage currents which could turn on both power MOSFETs.

At +9.2 volts the SG1825 turns on, driving the transformer primary through the two International Rectifier IRF840s. The 50 ohm series resistor at each gate provides isolation from the C_{GD} kick-back voltage, while the 1N5819 Schottky diodes provide a low-impedance drive at turn-off. The bootstrap winding then becomes active, providing the low-voltage high-current supply required by the control device. The turns ratio beween the regulated +5 volt output and the bootstrap winding is 2/4 or 0.5, resulting in a nominal 10 volt semi-regulated supply. Since the rectifier filter is capacitive-input rather than inductive, the actual controller supply is +15 volts.

Peak transformer primary current, which can be scaled to the output filter inductor current through the turns ratio, is sensed by a 1.0 ohm resistor in series with the MOSFET sources. After a low pass filter to remove leading edge peaking, the waveform is applied to the Ramp input pin. The current pulse is compared to the output of the error amplifier, and the drive to the power devices is terminated when the peak current exceeds the threshold set by the outer voltage control loop.

Slope compensation, required for loop stability above 50% duty cycle, is implemented by buffering the ramp waveform at the C_T pin with an 2N2222 emitter follower to preserve linearity. The ramp is summed with the supply output voltage sample at the inverting input of the error amplifier.

Short circuit protection is provided by passing the current waveform through a somewhat narrower bandwidth filter, and applying it to the dual threshold I_{LIM}/Shutdown pin. At light overloads, the +1.0 volt threshold will be exceeded, triggering pulse-by-pulse current limiting. If the output load increases further, the +1.4 volt threshold will be crossed. This discharges the soft-start capacitor, causing a low-frequency "hiccup" mode of current limit.

The transformer flux swing was chosen to be ± 0.1 Tesla (± 1000 Gauss) to keep losses low in the H_{7C4} ferrite core. Primary and bootstrap windings were bifilar wound to minimize leakage inductance, and the high current secondary was quadfilar construction for the same reason.

CONCLUSION

The completed power supply was bench-tested and met all design specifications. At 400KHz oscillator frequency the PWM chip had a wide modulation range, with nearly text-book waveforms. The improved layout and ground partitioning inside the integrated circuit minimized crosstalk problems between the high-current output drivers and the high-speed pulse-processing logic. Most importantly, the SG1825 controller was functional and well-behaved down to -55°C, making it particularly well suited to high-frequency military power supplies.

January 1990

APPLICATION CIRCUIT

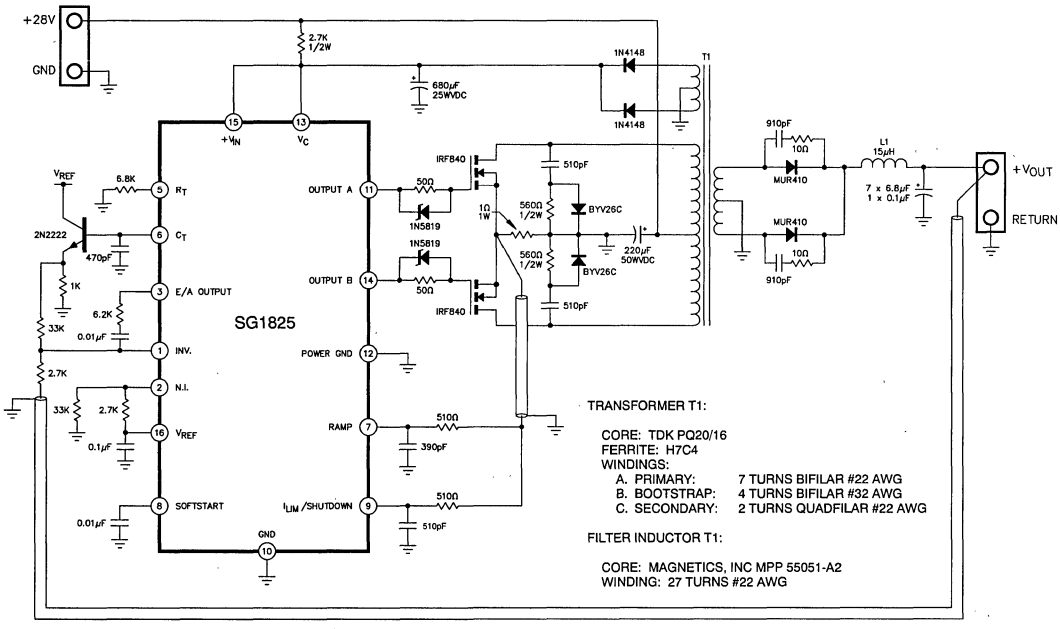

FIGURE 1 - SG1825 200KHz CURRENT-MODE POWER SUPPLY

A CURRENT MODE I.C. OPTIMIZED FOR SINGLE ENDED CONVERTERS

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INTRODUCTION

Recent advances in switched mode power supply (SMPS) technologies have resulted in rapid developments of more advanced pulsed width modulator (PWM) integrated circuits. Conventional PWM techniques are now losing some of their market share to the newer PWM circuits that are using current mode technology. One of these current mode PWM integrated circuits optimized for low cost, low to mid range output power supplies (15W-250W), is the SG1842/43/44/45 family of PWM controls. This application note includes a brief review of voltage mode technique vs. current mode (constant frequency type), their advantages and disadvantages, that is followed by a functional description of the SG1842/43/44/45 family of PWM controllers.

CURRENT MODE VS. VOLTAGE MODE CONTROL

Let us briefly review the conventional control approach (voltage mode technique) by referring to Figure 1.

In this method, the small differential voltage between output voltage (V_O) and reference voltage (V_R) is being amplified by the high DC gain of the error amplifier, resulting in an error voltage (V_E). This voltage is then compared to a fixed frequency sawtooth with a finite peak to peak magnitude (V_M). The output of the comparator stage is now a fixed frequency, variable duty cycle square wave that controls switch element (Q1) according to the variations in the magnitude of error voltage. This type of a converter where a single loop system is incorporated and only output voltage is being monitored and regulated, is called voltage mode technique. It is possible to vary the slope of the ramp signal in proportion to variation of input voltage, in order to improve line regulation and output dynamic response. This scheme is an improved version of voltage mode which is referred to as feed forward technique.

Now let us examine current mode method by referring to Figure 2. Notice that unlike the voltage mode, this scheme consists of two loops; a current loop which detects the switch current, inside another loop regulating the output voltage, called voltage loop.

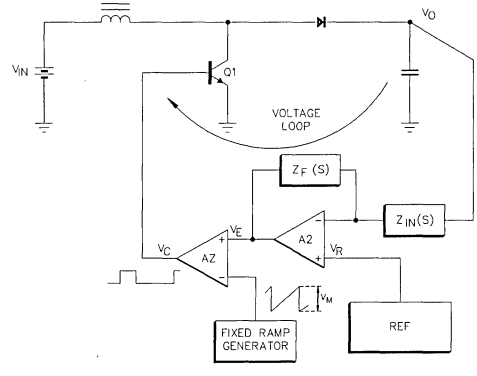

Figure 1. Typical Application of a Voltage mode regulator

The operation is as follows. A clock signal running at a fixed frequency sets the output of the latch circuitry to go high, turning on the switch (Q1). Once the voltage across the sense resistor (R_S) reaches a threshold set by the error signal (V_E), the output of the comparator (A2) switches low. This resets the latch, resulting in termination of the next output pulse and keeping it low until arrival of the next clock pulse.

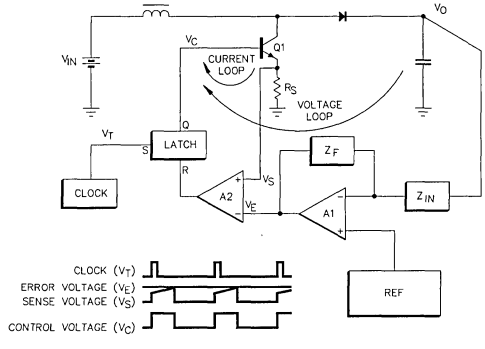

Figure 2. Typical Application of Current Mode Regulator

As a result of this two loop control scheme, current mode controllers offer several performance advantages. The first advantage over voltage mode is the inherent feed forward capability. Recall that in the current loop, the ramp voltage (V_S) across sense resistor was generated by the inductor current during switch "on-time", which was also directly proportional to the input voltage (V_{IN}). Therefore, as V_{IN} increases, the slope of the ramp also increases, which causes a shorter duration of the switch "on-time". This results in the control loop quickly adjusting itself to any line pertubations since it does not have to wait for a command from the output. As a result of this, current mode regulators have excellent line regulation and transient response.

Second, pulse-by-pulse current limiting is inherently achieved whenever using this method. This is because the error signal sets a limit on inductor peak current. This means that maximum current or current limit knee point can easily be set by simply clamping the output of error amplifier. This feature of current mode controllers is especially important whenever push-pull center tapped topologys are used, where any imbalance in the power transistors can cause a net DC current flow in the transformer. This problem sometimes causes transformer saturation and failure of the power transistors.

Third, current mode regulators are easier to stabilize and require simpler compensation circuitries. This is due to the fact that by controlling the inductor current, the double poles of control to output transfer function associated with conventional approach, are separated with two single poles. As a result, less phase shift is generated and the required phase boost is less critical for a stable operation. In fact, many current mode regulators are often compensated such that the overall loop gain is crossing zero db gain at a frequency prior to reaching the second pole frequency.

Finally, current mode controlled regulators can operate in parallel with equal current sharing, due to their inherent current regulating feature. One big advantage of paralleling converters is their redundant operation for the applications requiring high reliability power systems.

DESCRIPTION

The 1842/3/4/5 family of PWM controlled ICs are designed for low cost switched mode power supply applications utilizing current mode techniques. While they can be used in most DC-DC applications, they are optimized for single-ended designs such as Flyback and Forward converters. 1842/44 series are best suited for off-line applications, whereas 1843/45s are mostly used in power supplies with low input voltages. The IC can be divided into six main sections as shown in Figure 3: undervoltage lockout and start up; reference oscillator; current sense and PWM latch; error amplifier; and the output stage. The operation of each section is described and the differences between the members of this family are summarized in Table 1 and explained in each related section.

PART #	UVLO		MAXIMUM DUTY CYCLE
	Start-up Voltage (V_{ST})	Hysterise Voltage (V_{HYS})	
SG1842	16V	6V	<100%
SG1843	8.4V	0.8V	<100%
SG1844	16V	6V	<50%
SG1845	8.4V	0.8V	<50%

TABLE 1

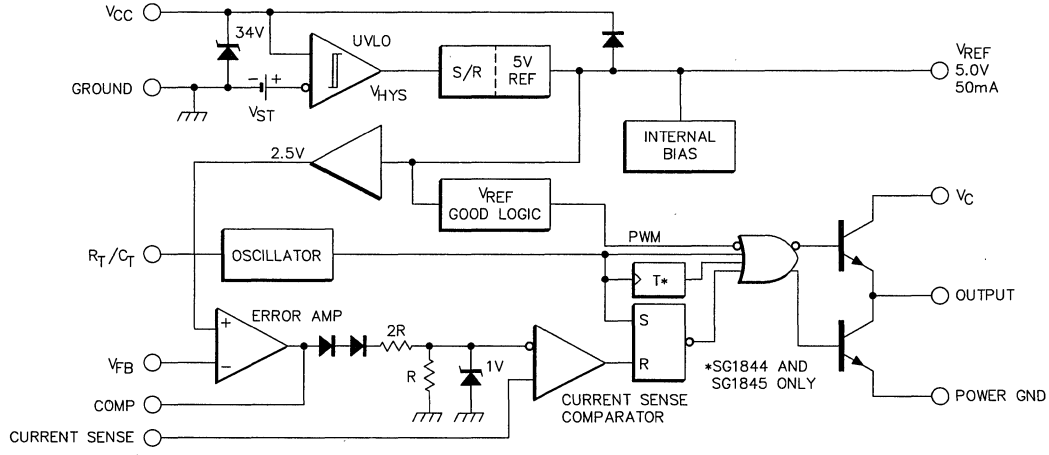

Figure 3. Devise Block Diagram

UNDERVOLTAGE LOCKOUT

The purpose of undervoltage lockout is to maintain a low quiescent current of less than 1mA and to guarantee that the IC is fully functional before the output stage is activated. Both input voltage (V_{IN}) and reference are monitored by separate comparators with built-in hysteresis. The input voltage comparator upper and lower thresholds for 1842/44 is 16V/10V and 1843/45 has 8.4V/7.6V nominal threshold levels. The combination of low start-up current and large hysteresis make them ideally suited in off line converter applications. Referring to Figure 4, an efficient start-up circuitry is implemented using 1842 PWM IC in conjunction with a bootstrap winding off of the power transformer. The operation of the circuitry is as follows.

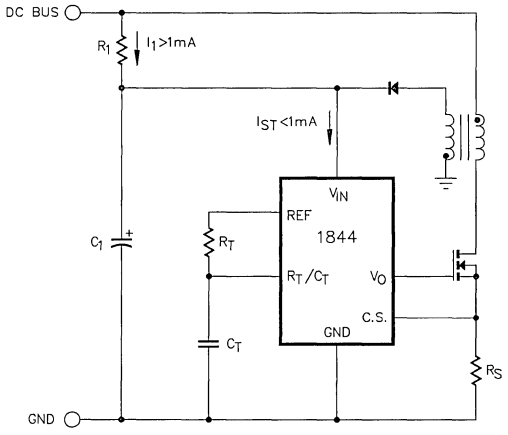

Figure 4. Typical Application of Start-Up Circuitry

The start-up capacitor (C1) is being charged by the current through resistor (R1) from the high voltage DC bus. Resistor (R1) is designed such that it provides more than 1mA of current. As the voltage across capacitor ramps up from zero, the only load current is the standby current of the IC. Once voltage reaches the start-up threshold, PWM IC starts operating, turning on the converter which causes the capacitor to discharge quickly, ramping down toward the drop-out thresholds. During this time, the auxiliary winding with (CR1) and (C1) provides the necessary voltage to continue to operate the IC and support its required supply current. (NOTE: The start-up capacitor must be large enough such that during the discharge period, the bootsrap voltage will reach above the shutdown threshold.)

VOLTAGE REFERENCE

The voltage reference is a low drift bandgap design which provides +5.0V to supply charging current to the oscillator timing capacitor, as well as supporting internal circuitries. Initial accuracy of 184X/284X is ±1%, and 384X series has ±2% over their specified ambient temperature range. The reference is capable of providing in excess of 20mA for powering any external control circuitries and has built-in short circuit protection.

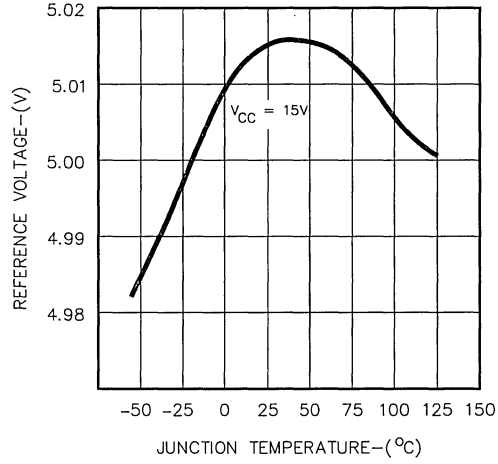

Figure 5. Reference Voltage vs. Temperature

OSCILLATOR

The oscillator is programmed by the values selected for the timing components (R_T) and (C_T). A simplified schematic of the oscillator is shown in Figure 6. The operation is as follows. Capacitor (C_T) is charged from the 5V reference with resistor (R_T) to a peak voltage of 2.8V nominally. Once this threshold is reached,

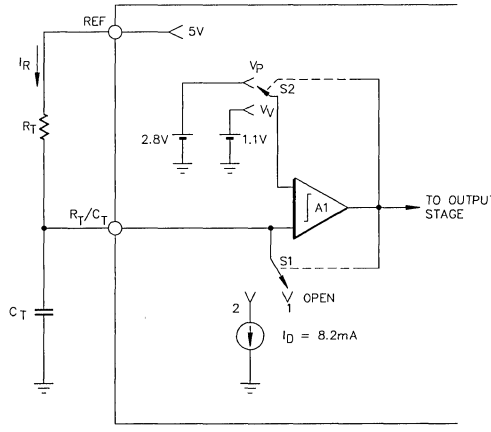

Figure 6. Simplified Schematic of Oscillator Section.

comparator (A1) changes state, causing (S1) to switch to position (2) and (S2) to (V_V) position. This will allow the capacitor to discharge with a current equal to the difference between a constant current (I_D) and current through charging resistor (I_R), until the voltage drops down to ≈ 1.1V nominally and the comparator changes state again repeating the cycle. Oscillator charge time results in the output to be in a high state (on time) and discharge time sets it to a low state (off time). Since the oscillator period is the sum of the charge and discharge time, any variations in either of them will ultimately affect the stability of the output frequency and the maximum duty cycle. In fact, this variation is more pronounced when the maximum duty cycle has to be limited to less than 50%. This is due to the fact that for longer output off time, capacitor discharge current (I_D - I_R) must be decreased by increasing I_R current. (NOTE: R_T value should always be greater than 520Ω or the oscillator may stop functioning). Consequently, this increases the sensitivity of the frequency and duty cycle to any small variations of internal current source (I_D), making this parameter more critical under those conditions. As a result, this parameter is trimmed to a nominal current value of 8.2±0.5mA at room temperature, and guaranteed to a maximum range of 7 to 9mA over the specified ambient temperature range. Figure 7 shows the variations of I_D over temperature.

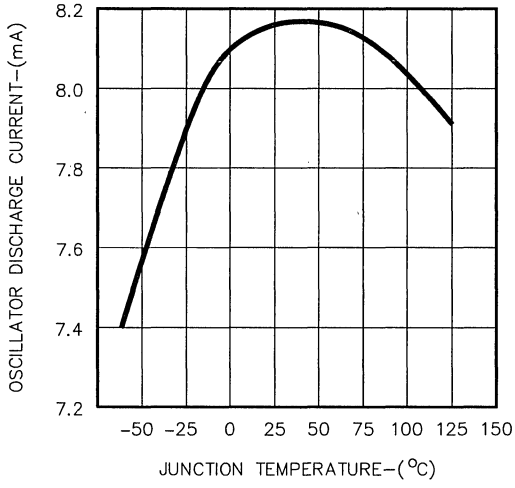

Figure 7. Oscillator Current vs. Temperature

The oscillator is designed such that many values of R_T and C_T will give the same frequency, but only one combination will yield a specific duty cycle at a given frequency (see Figure 8). A set of formulas are given to determine the values of timing components for a given frequency and duty cycle. (NOTE: The following formulas are less accurate at shorter duty cycles and/or higher frequencies. This will require some adjustment of timing components to correct for this error).

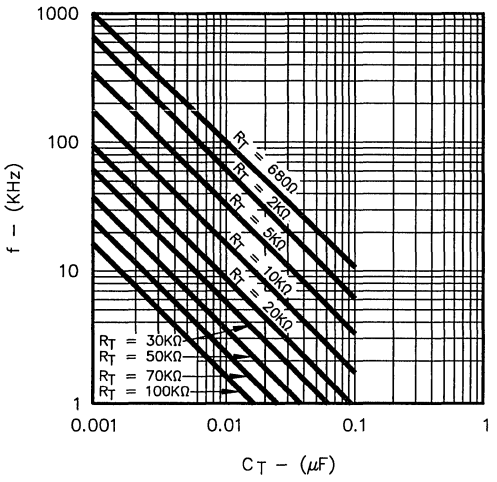

Figure 8. Oscillator Timing Diagram

Given: frequency ≅ f; maximum duty-cycle ≅ Dm
Calculate:

$$R_T = 267 \left[\frac{(1.76)^{\frac{1}{Dm}} - 1}{(1.76)^{\frac{1-Dm}{Dm}} - 1} \right] \ (\Omega), \ 0.3 \le Dm \le 0.95$$

$$C_T = \frac{1.86 * Dm}{f * R_T} \ (\mu f)$$

for duty cycles above 95% use:

$$f \approx \frac{1.86}{R_T C_T} \quad \text{where } R_T \ge 5K\Omega$$

Example: A flyback power supply design requires the duty cycle to be limited to less than 45%. If the switching frequency is designed to be 50kHz, what are the values of R_T and C_T?

Given: f = 50KHZ
Dm = 0.45

$$R_T = 267 \left[\frac{(1.76)^{\frac{1}{.45}} - 1}{(1.76)^{\frac{.55}{.45}} - 1} \right] = 674\Omega$$

$$C_T = \frac{1.86 \times 0.45}{50 \times 10^3 \times 674} = .025 \ \mu f$$

CURRENT SENSE COMPARATOR AND PWM LATCH

Referring back to the operation of current mode PWM, recall that the switch peak current is established by the output of the error amplifier. This current is sensed by an external sense resistor (or a current transformer), monitored by a C.S. pin and compared internally with a voltage from the output of the error amplifier. The output of comparator then goes to a PWM latch that will insure only a single pulse to appear at the output during any given oscillator cycle. SG1844/5 series have an additional flip flop stage that will limit the output to less than 50% duty cycle range as well as reducing its frequency to half of the oscillator frequency. The current sense comparator threshold is internally clamped to 1V nominally which would limit maximum peak switch current to:

$$(1)\ I_{SPMAX} = \frac{V_Z}{R_S}$$ where: $I_{SP} \equiv$ Peak switch current, $V_Z \equiv$ internal zener, $0.9V \le V_Z \le 1.1V$

Equation 1 is used to calculate the value of sense resistor during the current limit condition where switch current reaches its maximum level. In normal operation of the converter, the relationship between peak switch current and error voltage (voltage at pin 1) is given by:

$$(1)\ I_{SPMAX} = \frac{V_E - 2V_F}{3 * R_S}$$ where: $V_E \equiv$ Voltage at pin 1, $V_F \equiv$ Diode - Forward volt. 0.7V at $T_J = 25°C$

The above equation is plotted in Figure 9. Notice that the gain becomes non-linear above current sense voltages greater than ≈ 0.88 volts. It is therefore recommended to operate below this range during the normal operation. This would insure that overall closed loop gain of the system will not be affected by the change in the gain of the current sense stage.

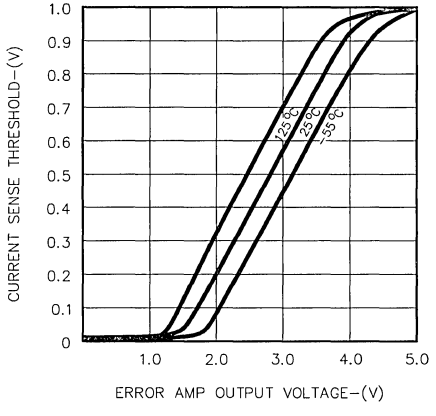

Figure 9. Current Sense Threshold vs. Error Amplifier Output

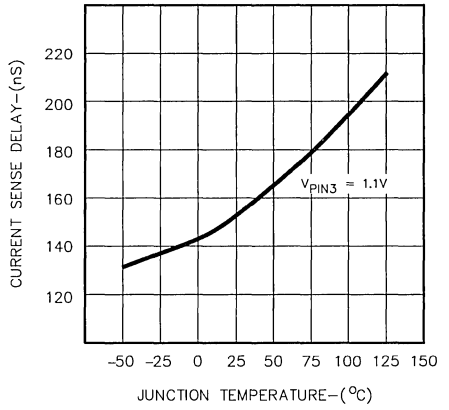

Figure 10. Current Sense to Output Delay vs. Temperature

ERROR AMPLIFIER

The error amplifier has a PNP input differential stage with access to the Inverting input and the output pin. The N.I. input is internally biased to 2.5 volts and is not available for any external connections. The amplifier is internally compensated with a bandwidth of ≈ 1MHz and a typical DC open loop gain of ≈ 90dB. The maximum input bias current for 384X series is 2μA, while 184X/284X devices are rated for 1μA maximum over their specified range of ambient temperature. Low value resistor dividers should be used in order to avoid output voltage errors caused by the input bias current. The error amplifier can source 0.5mA and sink 2mA of current. A minimum value of feedback resistor (R_F) is given by:

$$R_{FMIN} = \frac{3(1.1) + 1.8}{0.5mA} = 10K$$

Figure 11 shows the open loop gain and phase response of the error amplifier for all devices.

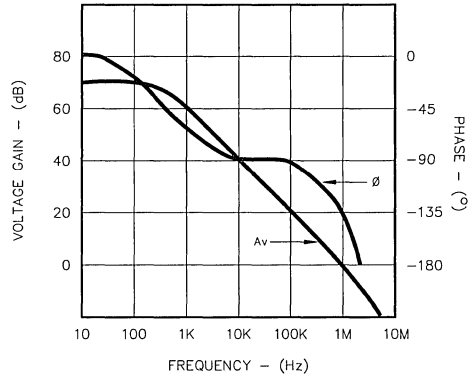

Figure 11. Error Amplifier Open-Loop Frequency Response

OUTPUT TRANSISTOR

The output section has been specifically designed for direct drive of power MOSFETs. It has a totempole configuration which is capable of up to ±1A of peak current. This will typical result in a rise and fall time of 50ns into a 1000pf capacitive load. Each output transistor (source and sink) is capable of supplying 200mA of continuous current with typical saturation voltages of less than 2.5 volts over -55°C to +125°C junction temperature range. (See Figure 12 and 13) All parts are designed to minimize the amount of shoot-thru current which is a result of momentary overlap of output transistors. This allows a more efficient usage of the IC at higher frequencies, as well as improving the noise susceptibility of the device.

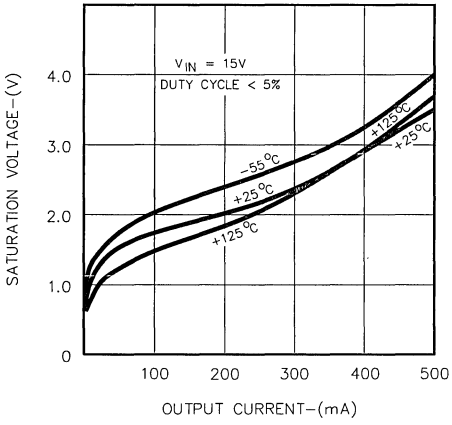

Figure 12. Output Saturation Voltage vs. Output Current and Temperature

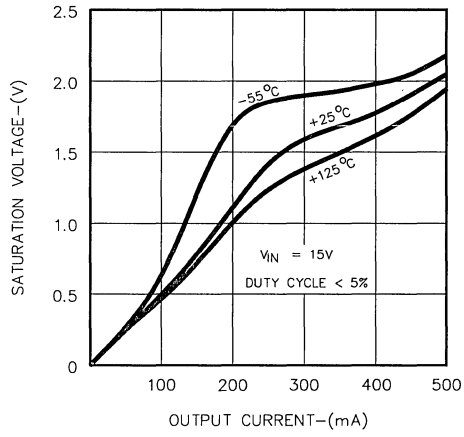

Figure 13. Output Saturation Voltage vs. Output Current and Temperature

OUTPUT SUPERVISORY CIRCUITS: A NEW FAMILY OF POWER SUPPLY CONTROL DEVICES

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Silicon General, Inc.

ABSTRACT

This paper describes a series of new monolithic integrated circuits designed to perform all the functions necessary to monitor and control the outputs of sophisticated power supply systems. Beginning with a simple over-voltage sensing circuit, these devices range through more versatile and accurate single-function units, to all-inclusive devices which contain sensing circuits for both over and under-voltage conditions, current sensing, SCR crowbar firing, logic outputs, and an accurate independent reference generator. A description of the operation of each individual element is given together with several applications which demonstrate their utility.

INTRODUCTION

Recent years have seen the introduction of many sophisticated integrated circuits for use in controlling the voltage regulation function of both linear and switching power supply systems. While these circuits have provided a high degree of performance with a side benefit of considerable increases in both reliability and cost savings, they have all addressed the basic function of maintaining the output voltage constant. Most power supply systems, however, require additional circuitry for monitoring satisfactory performance and providing protection in the event of a fault condition. These requirements have led to the development of a new class of power supply element - an Output Supervisory Control Circuit.

SUPERVISORY CONTROL FAMILY MEMBERS

The first integrated circuit developed specifically as a power supply monitoring device was Motorola's MC3523 available also as an SG3523 from Silicon General. This device, which is packaged as an 8-pin minidip, was designed to sense an over-voltage condition, provide an adjustable time delay, and then fire a high-current SCR crowbar for power supply shutdown. An improved and interchangeable device, the SG3523A, was later introduced to provide more tightly specified performance, greater threshold accuracy, and improved temperature stability. Block diagrams of these two devices are shown in Figure 1.

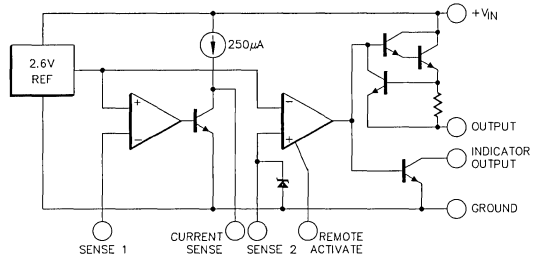

Figure 1. SG3523 Over-Voltage Sensing Circuit. The SG3523 and 3523A contain an independent reference generator, an input comparator designed to initiate a setable time delay, and a second comparator which activates both a crowbar firing current and a low-level indication signal.

It was soon recognized that with the addition of a few more access points to this circuit, significant increases in versatility could be achieved. This led to the development of the SG1542 device shown in Figure 2. With 14 pins in this DIL package the following additional features could be offered:

1. Access to the reference generator's output so that one could take advantage of it's 1% accuracy and 50 ppm T.C.

2. Uncommitted inputs to the sensing comparator allowing use for either under or over-voltage sensing as well as the ability to set threshold levels below 2.6 volts.

3. The addition of a logic level output active when the sensed voltage is within tolerance, as well as the one which indicates out-of-tolerance.

4. A separate supply terminal for the high current SCR trigger allowing greater utilization of this output.

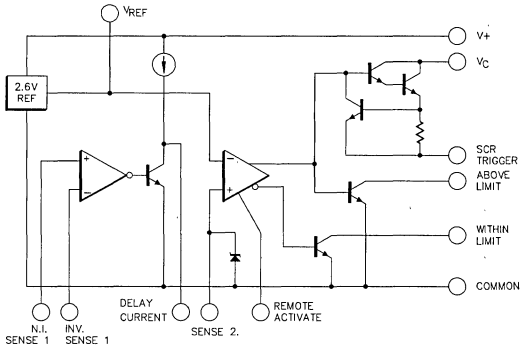

Figure 2. SG1542 Voltage Sensing and Protection Circuit. The use of a 14-pin package for the SG1542 provides greater access to the circuit elements and thus greatly expanded versatility.

Finally, it was decided to build an all-encompassing device which would include both over and under-voltage sensing as well as a means for current limiting, all in one integrated circuit. This resulted in the 16-pin SG1543, the main subject of this paper. The circuitry of the SG3523, 3523A, and 1542 is equivalent to the OVP portion of the SG1543 and thus need not be described separately.

Before proceeding with a discussion of the SG1543, however, there is one more member of this family worth mentioning. The SG1544 is identical to the SG1543, but uses an 18-pin DIL package to keep the voltage-sensing comparator inputs uncommitted. This adds the ability to sense voltage levels below the reference voltage to the lengthy list of features offered by the SG1543. Now, on to a more complete description.

THE SG1543 OUTPUT SUPERVISORY CIRCUIT

To fill the need for this output monitoring and controlling function, the SG1543 output supervisory circuit shown in Figure 3 was developed. This devices contains an operational amplifier, a voltage reference circuit, several comparators, and a high-current SCR trigger circuit. The functions performed by this device include over-voltage and under-voltage sensing, current limiting, and provisions for triggering an external SCR crowbar shutdown.

All the functions provide open collector outputs for maximum flexibility in interfacing with either the power supply or the system load and, although the SCR trigger is directly connected only to the over-voltage sensing circuit, it may be optionally activated by any of the other outputs or by an external shutdown command. The SCR trigger circuit also includes an optional latch with external reset capability. External capacitors may be used to accurately program the sensing circuits for a minimum time duration of fault before triggering.

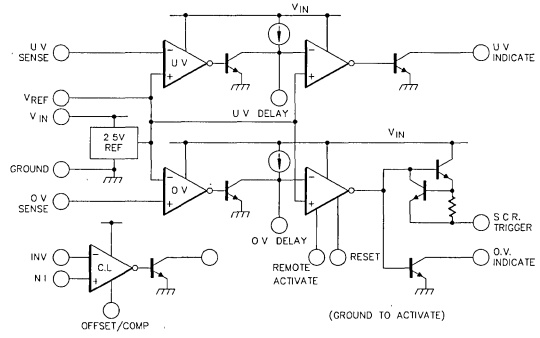

Figure 3. The block diagram of the SG1543 Output Supervisory Circuit includes over-voltage and under-voltage sensing as well as the capability for current limiting and SCR crowbar triggering.

The SG1543 circuit may be powered by either the output voltage to be monitored or a separate bias voltage at any level between 4.5 and 40 volts with a standby current of less than 10mA.

This device is packaged in a standard 16-pin hermetically sealed ceramic package and is available in both commercial and military temperature ranges. Before describing in greater detail the overall functions that this device can perform, it is worth discussing the individual circuits which go into its makeup.

VOLTAGE REFERENCE CIRCUIT

The precision 2.50V reference circuit of the SG1543 is shown in Figure 4. This regulator is based upon the well-known band-gap reference circuit which has the capability of providing very stable performance over an input voltage range from as low as 4.5V to as high as 40V. The output is nominally set at 2.5V, but in addition, is trimmed to remove all effects of production manufacturing tolerances from the output voltage. In fact, this trimming not only adjusts the output voltage to within 1% of 2.5V, but in the process, as shown in Figure 5, also trims the temperature coefficient of output voltage to better than 50 parts per million per degree C. The trimming is performed at wafer probe by using controlled energy sources to blow fusable metal links which short out incremental values of resistance in the voltage setting network. These resistors are binarily coded so that three values give eight bits of

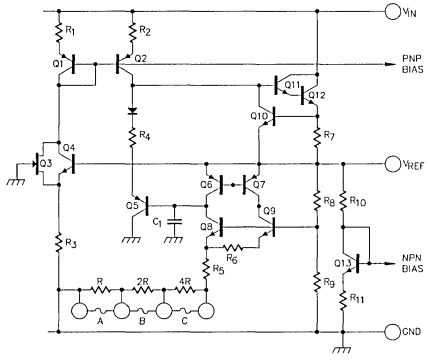

Figure 4. This precision 2.50 volt band-gap reference source is internally trimmed for ±1% accuracy in order to eliminate the need for adjustment potentiometers.

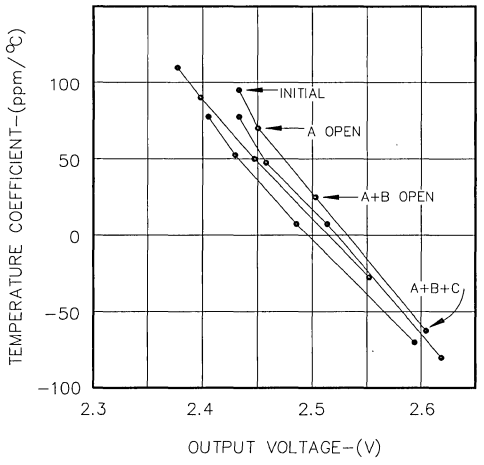

Figure 5. Temperature Coefficient vs. Voltage Trim as successive links are opened in the reference voltage trimming network, the output voltage increases and the temperature coefficient becomes less positive.

resolution and allow trimming to better than ±12 millivolts. With this accuracy in all but the most precise applications, the need for adjustment or trimming potentiometers is effectively eliminated.

The output of this reference circuit is current limited for protection and will provide up to 10 milliamps of current for use as a reference for other functions that may be required along with the SG1543. In addition to stable temperature performance, this regulator also maintains its output voltage to within 10mV for all line and load changes. Additional benefits of the band gap reference circuit include a low noise performance, instant turn-on, and a high degree of long-term stability.

COMPARATOR SECTION

Over and under-voltage sensing circuits are identical with only the input polarity changed between them. The under-voltage circuit is shown schematically in Figure 6. This configuration in made up of two comparators in series, each referenced to 2.50 volts, with the delay terminal at their juncture. The first comparator activates a current source upon sensing an out-of-tolerance condition and that current is used to charge an externally selected capacitor to provide a delay. The second comparator then activates the output indicating circuit. The overall time delay from input sense to output indicate, with no external capacitor, is approximately 0.5 microsecond. By adding a capacitor at the delay terminal, the fault must exist for an interval defined by the time it takes the voltage on the capacitor to charge from zero to 2.5V before the output comparator can switch. The charging current for this capacitor is a constant 250 microamps which provides for a delay of approximately 10 milliseconds per microfarad of capacitance. Since the comparator can discharge in excess of 10mA, the capacitor is reset in a fraction of its charge time.

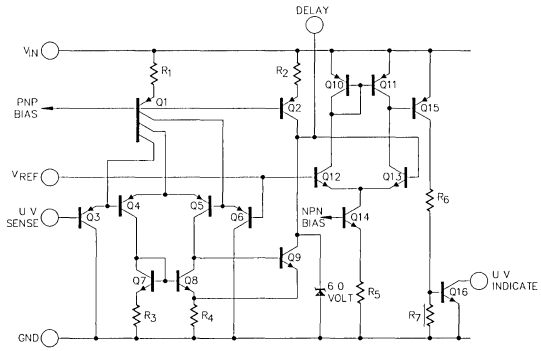

Figure 6. Voltage Sensing Comparators. Voltage level sensing is done with a high input impedance comparator with built-in hysteresis. When switched, the input comparator allows a constant current source to trigger the output comparator.

The input comparator has PNP transistor inputs which provide both high input impedance with less than one microamp bias current, and a wide input voltage range which includes ground and goes to within 2V of the positive supply voltage. Because the input PNP operates as an emitter follower, the input impedance to that comparator remains high throughout the input range. To eliminate the tendency to oscillate at threshold, a hysteresis of approximately 25mV is built into the input comparator.

The output indicating transistor, Q18, is designed to sink 10mA of current with a saturation voltage of less than 0.4 volt. Its open collector allows several outputs to be connected together to provide a single indicating signal.

SCR TRIGGER SECTION

While the under-voltage sensing circuit has only the 10mA, or low current, open-collector output, the over-voltage section contains additionally, an SCR crowbar triggering circuit good for 200mA. This stage also includes provision for remote activation of the output as well as a reset terminal. From the schematic shown in Figure 7, it can be seen that the output voltage comparator drives a PNP transistor, Q6, with two collectors, one of which drives the low-current, open collector indicating signal similar to the under-voltage circuit. The other collector of Q6 drives a Darlington amplifier which will provide 200mA to activate an external high current SCR crowbar device. Note that these two outputs are complements of each other; i.e. when pin 4 switches to ground, pin 1 goes positive.

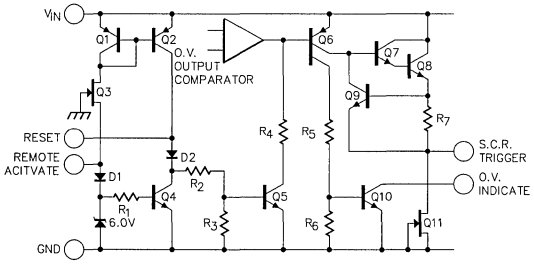

Figure 7. Over-Voltage Circuit. Either the over-voltage output comparator or the remote activation terminal will energize both the SCR trigger and the O.V. indicating transistor. Connecting pins 4 and 2 form a latch.

Since in many cases it is desired to activate the crowbar under other than over-voltage conditions, a remote activation circuit is also included. This consists of transistors Q1 through Q5 as shown in Figure 7. The functioning of this circuit is as follows: Q3 provides a controlled current source of approximately 300 microamps to saturate transistor Q4. With Q4 saturated, transistor Q5 is held in the off condition. When the remote activation terminal, pin 2, is grounded, it diverts the current away from the input of Q4, turning it off and turning Q5 on, which activates the output circuitry in the same manner as the over-voltage comparator.

An additional function of this circuit is to provide the capability to latch the outputs on after a fault is sensed, by externally connecting the over-voltage indicating terminal, pin 4, to the remote activation terminal, pin 2. With this configuration, an over-voltage condition which turns on Q10 will pull pin 2 to ground activating the remote activation signal which, in turn, holds the circuit in the on condition until the reset terminal is externally grounded, removing the latch and turning off the output. Thus, the user has the capability to either activate the high current output only as long as a fault condition exists, or to latch it on upon the occurrence of a fault requiring external action by an operator to reset the circuit to its initial condition. Thresholds for both remote activation and reset terminals are approximately 1.2 volts.

CURRENT SENSING AMPLIFIER

The amplifier in SG1543 designated for current sensing actually has much wider application. It is basically a high-gain, non-compensated operational amplifier with an open collector output; i.e., pull-up on the output must be provided externally. from the schematic shown in Figure 8, it can be seen that this circuit also has a PNP front end which gives it a wide common-mode range extending from slightly below ground to within 2 volts of the supply voltage. With a pull-up resistor of 2kΩ, the open loop voltage gain is greater than 72dB with a unity gain bandwidth beyond 5MHz. When used as a comparator, the response time is less than 200nanoseconds, and if linear amplification is required, external compensation may be added for stable performance over a wide frequency range or a unique frequency response.

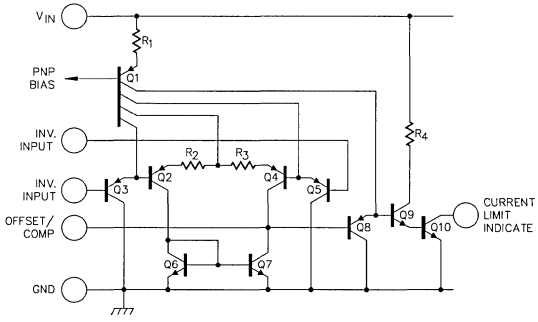

Figure 8. Current-Sensing Amplifier. PNP inputs give the current limit amplifier a common-mode input voltage range of from below ground to within 2 volts of the supply voltage.

The input to this amplifier is balanced for zero offset voltage but a fixed offset or threshold of up to 200mV may be incorporated by adding or subtracting current at the offset/compensation pin 12. For most current sensing application the required threshold polarity calls for a positive voltage on the inverting input. This can be accomplished with a resistor, R_T, to ground as shown in Figure 9.

Reducing the impedance at pin 12 also lowers the gain of the amplifier somewhat as shown in Figure 8. This fact allows pin 12 to do double-duty as a point to apply frequency compensation as well. Due to the excess phase shift of the internal PNP transistors, this amplifier requires compensation for stable closed-loop, linear

applications but this can be accomplished easily with either C_1 to the output or C_2 to ground as shown in Figures 9 and 10.

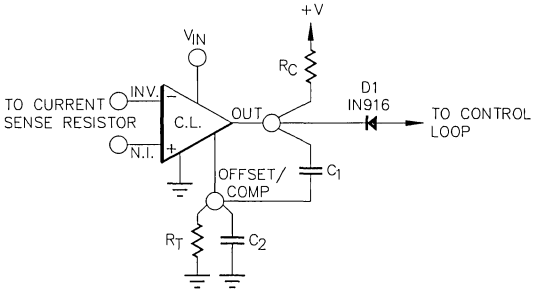

Figure 9. Current Sense Compensation. External components can be used with the current sense amplifier to establish an input offset or threshold, define the frequency response, and buffer the output.

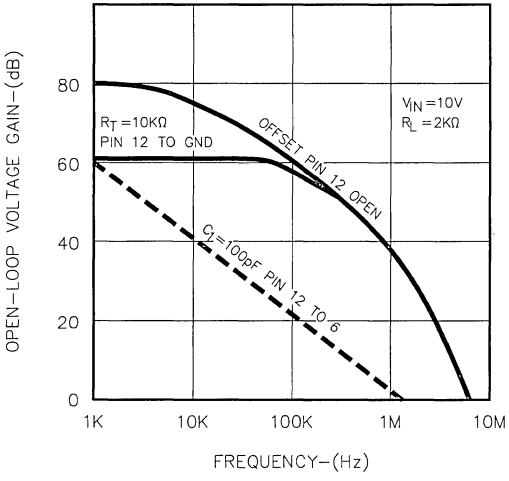

Figure 10. C.L. Amplifier Frequency Response. With 80dB gain and 5MHz bandwidth, the current sense amplifier provides a wide dynamic response, even when modified with external passive components.

Diode D1 and resistor R_c are used only if it is necessary to increase the frequency response by operating the output transistor at higher current and/or isolating the load from R_c and C_1 when the amplifier is off.

Applications

Figure 11 shows a typical application of the SG 1543 as used to monitor a single power supply output voltage for both high and low voltage operation as well as current limiting. The data accompanying Figure 11 indicates how the values for the external components are selected. This circuit is driven from an external bias supply which must provide a standby current of 10mA maximum plus the activation current for the SCR trigger. The application in Figure 11 shows a single resistor divider string, R_4, R_5, and R_6, which sets the thresholds for both the under and over-voltage activation levels. The external capacitors C_{D1} and CD2 are used to provide time delays before activation of the output circuitry. The output of the comparators can be used for many different functions; in this case, they are shown driving indicators. They can also provide signals to the system under power to give information that an out-of-tolerance condition exists. Additionally, by the external connection between pin 2 and pin 4, a latch has been provided such that an over-voltage condition will activate and hold that control signal until positive reset action at pin 3 is performed.

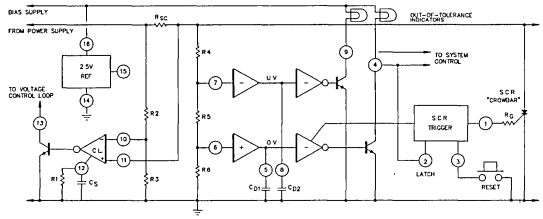

Figure 11. This typical application for the SG1543 provides linear foldback current limiting as well as over and under-voltage protection.

In firing an SCR with supply voltages above 5 volts an external resistor, R_G, is used on pin 1 to provide power dissipation limiting for the SG1543. While the SG1543 will provide up to 400mA of trigger current, the power limitation of the 16-pin-dual-in-line package should be held to less than one watt.

In this application, current limiting is performed by sensing the current in the positive supply line with fold-back provided by the action of R_2 and R_3. A fixed threshold for the amplifier is set by R1 which is connected between pin 12 and ground.

Although the SG1543 could have been driven from the output voltage to be monitored, it would lose control when that output voltage fell to approximately 3V. This would, of course, preclude the use of the current limit function where short circuit protection must be provided.

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The values for the external components used in conjunction with the SG1543 application of Figure 11 are determined as follows:

Current limit input threshold, $V_{TH} \approx \frac{1000}{R_9}$

Cs is determined by the current loop dynamics

Peak current to load, $I_P \cong \frac{V_{TH}}{R_{SC}} + \frac{V_O}{R_{SC}} \left(\frac{R_2}{R_2 + R_3}\right)$

Short circuit current, $I_{SC} = \frac{V_{TH}}{R_{SC}}$

Low output voltage limit, V_O (Low) = $\frac{2.5\ (R_4+R_5+R_6)}{R_5+R_6}$

High output voltage limit, V_O (High) = $\frac{2.5\ (R_4+R_5+R_6)}{R_6}$

Voltage sensing delay, $t_D = 10{,}000\ C_D$

SRC trigger power limiting resistor, $R_G > \frac{V_{IN} - 5}{0.2}$

CURRENT SENSING OPTIONS

It is important to remember that all the features of the SG1543 apply equally to either linear or switching power supplies. Figure 12, for example, shows the current sensing amplifier in the SG1543 used to provide foldback current limiting for a linear regulator utilizing the SG723. To answer the question of why one would use the SG1543 for current limiting when that capability is built into the SG723, there are two important benefits: low sensing threshold voltage (whatever is selected vs. a fixed 700mV) and much higher gain for a very sharp transition from voltage to current feedback.

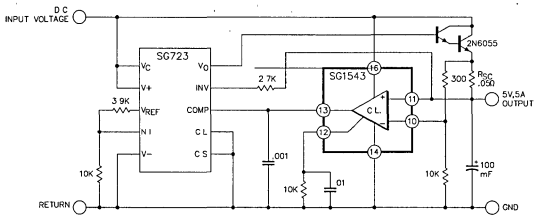

Figure 12. Linear Foldback Current Limiting. The SG1543 is equally adaptable to either linear or switching supplies. The circuit above shows a substantially improved current limit function for a linear SG723 voltage regulator.

Output current limiting for a switching supply which gets its control from an SG1524 regulating pulse width modulator is shown in Figure 13. Here, foldback is not included but an optical coupler for isolation has been added. It should be noted that all the low-current outputs of the SG1543 are equally well suited for driving optical couplers.

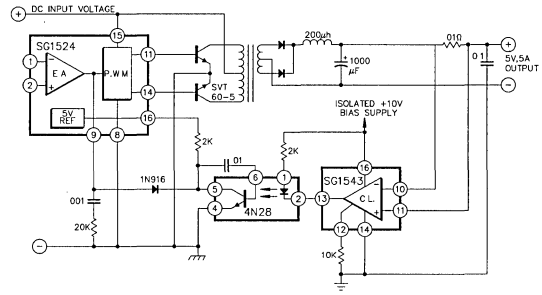

Figure 13. DC Converter With Isolated Current Limiting. Current limiting for a switching inverter is readily accomplished, even with a requirement for input-output isolation.

The last application suggests another use for the current sense amplifier completely disassociated with current. This is shown in Figure 14 where it is used in conjunction with the very excellent characteristic of the 2.50 volt reference contained within the SG1543 to provide an isolated voltage feedback signal. The SG1543's amplifier provides the gain and the overall loop compensation network, and drives a high-frequency opto-coupler which feeds into the unity-gain configured error amplifier of the SG1524. A designer should recognize that there are many possible variations on this theme, including taking the error signal from the collector of the opto-coupler, feeding into the output of the SG1524's error amplifier such that this amplifier provides a startup signal. Then the SG1543 may be powered directly from the output eliminating the need for an isolated bias supply.

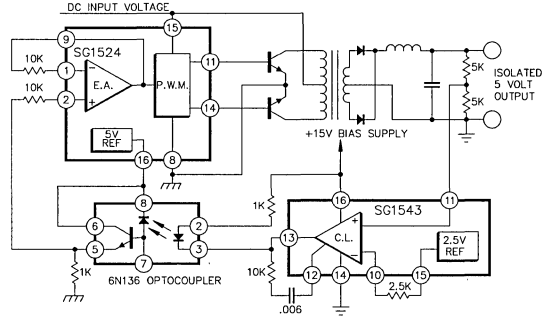

Figure 14. The current sense amplifier can also be used in conjunction with the SG1543's reference to provide a stable, isolated voltage feedback signal.

One final possible use for the current limit amplifier is to provide complete shutdown of the power supply rather than linear voltage reduction upon sensing an over-current condition. This function is shown in Figure 15 where the current limit amplifier is used as a comparator with the output terminal connected to the remote activation terminal for the SCR trigger. In this case, sensing is

done in the ground line. There is no offset added to the current limit amplifier but instead a threshold is provided by the action of R_1 and R_2 from the 2.50V reference signal. When an over-current condition is sensed and maintained for a period of time determined by a capacitor C_D on pin 12, then the output transistor will conduct, activating the SCR trigger and shutting down the power supply.

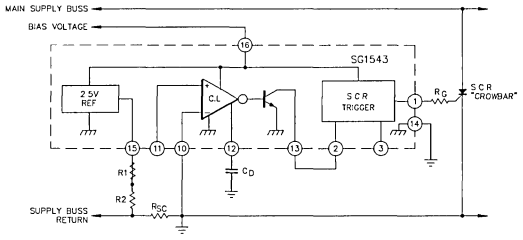

Figure 15. Overcurrent Shutdown. The current sense amplifier may also be used as a high-gain comparator to shut down the supply upon over-current.

SENSING MULTIPLE OUTPUT VOLTAGES

Many power supply systems have several output voltages which need to be monitored. This is easily done with the SG1543 because of the capability for remote activation and the availability of the reference voltage for use with external circuitry. A quad comparator like the SG139 which also has open collector outputs can be used to monitor several additional output voltages. As shown in Figure 16, the SG1543 is used to provide both over and under-voltage protection on a main positive supply. The additional comparators within the SG139 can be used to monitor either positive or negative supply voltages depending on whether one uses the 2.5V signal or ground as the reference potential. The output comparators of each collector are tied together to the remote activation terminal such that the operation of any single comparator in either the SG1543 or the SG139 will activate the SCR trigger shutdown circuit. Note thatgrounding the remote activation terminal also provides an output on the over-voltage indicating circuit; therefore, this output on pin 4 can be used as a master power supply-condition indicator which will provide a low signal if any output voltage that is being monitored is outside its allowable tolerance.

UNDER-VOLTAGE SENSING

In addition to normal low-output voltage monitoring, the under-voltage sensing circuit has considerable possibilities in monitoring the input voltage to a power supply system. For example, in Figure 17, this circuit is used to measure the input DC voltage to an SG723 regulator and keep the output completely off whenever the input is lower than the minimum required for satisfactory operation of the SG723. The same protective feature when applied to a switch-mode regulator, is even more important since it keeps the switching transistors off until the oscillator stabilizes.

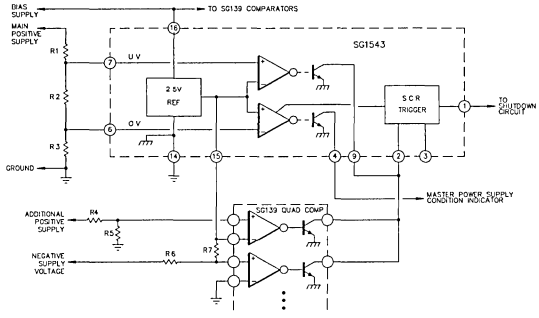

Figure 16. Sensing Multiple Supply Voltages. Addition of a simple quad comparator allows multiple voltage sensing of positive or negative levels.

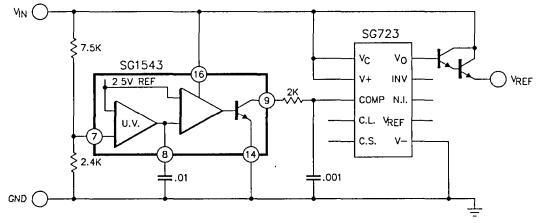

Figure 17. Under Voltage Shutdown. In addition to output monitoring, the under-voltage circuit can be used to inhibit the output if the input voltage is too low for satisfactory performance.

As shown in figure 18, the under-voltage circuit can be used to monitor the AC input voltage to a power supply. An isolation transformer and rectifier are used to provide a rectified AC signal to the input of the under-voltage comparator. The signal is compared with the 2.50V reference, activating the first stage of the comparator with each transition toward zero. With proper selection of the delay capacitor, no output is provided unless some

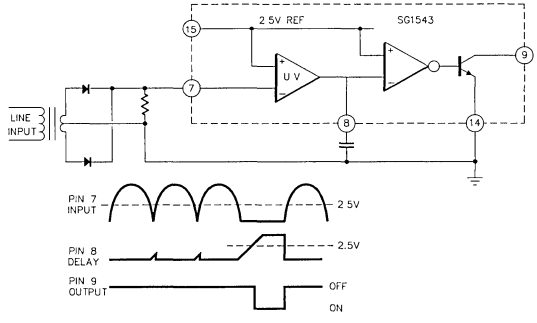

Figure 18. SG1543 Input Line MonitorThe under-voltage sensing circuit can also be used to monitor the AC input voltage and provide a power failure signal before the power supply output voltage begins to fall.

number of input pulses are missing at which time the first comparator allows the charging of the capacitor to 2.50 volts which activates the output circuit. In this way, the under-voltage circuit provides an immediate indication of failure, even for one or two cycles. This provides an early warning indication that the power supply output voltage is going to drop while taking advantage of the holdup capability provided by normal electrolytic capacitor storage within the power supply system.

Like other parts of the SG1543, the under-voltage circuit is not limited to its primary function. Figure 19 demonstrates its use as an over-temperature indicator by using the well-defined temperature coefficient of a Darlington transistor's V_{BE} as a sensor. Divider R_1-R_2 establishes a fixed threshold equal to the 2N2723's V_{BE} at the desired temperature limit. Below that limit, the transistor is off and R_C back-biases the input to the U.V. sensor. Many other transistors could be used; however, the small case of the 2N2723 makes good thermal coupling relatively easy.

By providing all of these diagnostic and protective features within one integrated circuit, a new class of control device has been generated to provide overall performance monitoring and control of sophisticated power supply systems. Thus, the SG1543 further enhances the inventory of building block components available to the power supply system designer providing new options in implementing increased performance at lower cost.

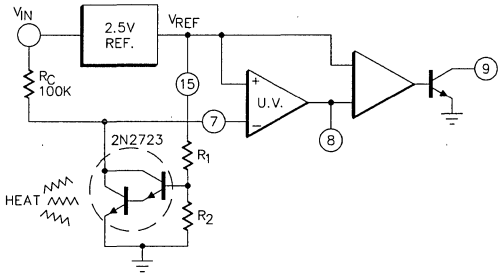

Figure 19. Over-Temperature Indication. Another use of the under-voltage circuit is to provide an over-temperature indication using the -4mV/°C V_{BE} tempco of the 2N2723 as a sensor.

A CONCEPTUALLY NEW QUAD POWER FAULT MONITOR CIRCUIT

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Edited by Reza Amirani

ABSTRACT

A comprehensive fault monitoring system in a single 16-pin IC is described. The new circuit provides overvoltage and undervoltage supervision of four DC power supplies simultaneously. In addition a uniquely flexible pin-out permits AC line voltage monitoring, real-time line clock generation, or programmable switching supply undervoltage lockout protection. All fault thresholds are adjustable to a high degree of accuracy using a minimum of external passive components. A number of typical application examples are given to clarify the concepts discussed.

INTRODUCTION

As the complexity of modern electronic systems grows, the number of supply voltages necessary to support the circuitry has also increased. Even the simplest home computer typically requires +5 volts for the logic, ±12 or ±15 volts for the analog circuits, and perhaps +24 or +28 volts for the printer or disk drive. The task of supervising these multiple voltages for proper tolerance has traditionally required a substantial number of precision components: a voltage reference, resistors, timing capacitors, op amps, comparators, and logic gates. An additional penalty was paid in board space consumption. Consequently, in an attempt to shave costs, the supervisory function was often eliminated entirely. While this action resulted in meeting budget for the supply, the money saved was often given out again many times over when a system malfunction occurred in the field and a service engineer had to tediously check each supply voltage.

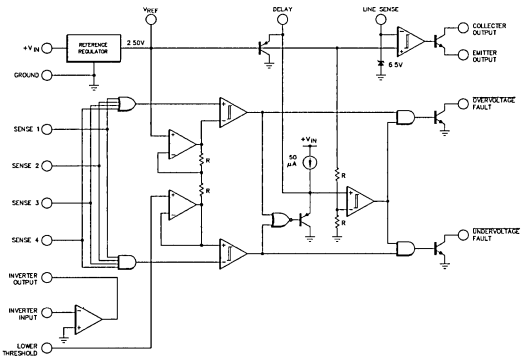

Figure 1. Block Diagram of the SG1548 Quad Power Fault Monitor

The availability of a new integrated circuit which can monitor four DC supplies and the AC line simultaneously now allows the power systems designer to implement fault monitoring at lower cost and with much reduced board space. This new device utilizes the strengths of monolithic linear technology to create precisely-matched components at high density on a silicon chip. Called the SG1548 Quad Power Fault Monitor, its functional block diagram is shown in Figure 1.

FUNCTIONAL DESCRIPTION

The circuit consists of a precision reference regulator, a fault window generator, analog OR and AND circuitry for selecting most positive and most negative voltages, threshold comparators, delay logic, open-collector output drivers, an inverting amplifier, and a multipurpose line sense comparator with uncommitted collector and emitter outputs.

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The most positive voltage at the four Sense inputs is compared with the upper or overvoltage threshold, and the most negative input is routed to the undervoltage comparator. The comparator outputs are connected to their respective output drivers and two AND logic gates. The drivers are inhibited by the delay logic, which requires that either an overvoltage fault or undervoltage fault persists for a pre-set time interval. A single capacitor at the Delay pin sets the time interval, which is C x 2.5 x 10^4 seconds. If a negative voltage must be monitored, it can be mirrored into a positive voltage using the inverter amplifier. Special clamp circuitry inside the SG1548 prevents the amplifier from locking up if Pin 15 is pulled below ground. Now let's look at the operation of each subset in detail.

VOLTAGE REFERENCE

The reference circuit is a low-drift bandgap design which generates a precise +2.50 volts ±1% at Pin 3. It is fully functional at input voltages as low as +4.5 volts, and provides up to 10mA of output current. Special β-compensation circuitry provides immunity to process variations and achieves typical 1mV line and 3mV load regulation. Internal current limiting protects the IC against accidental shorts to ground.

FAULT WINDOW GENERATOR

The fault window generator is the heart of the Quad Power Fault Monitor. This section generates an upper overvoltage and lower undervoltage threshold centered about the +2.5 volt reference. A precision tracking regulator utilizing two operational amplifiers and a pair of ratioed resistors produce the tracking action, as shown in Figure 2.

An external voltage derived from the reference is applied to Pin 1. This voltage represents the lower boundary of the tolerance window. Op amp A1 is connected as a unity-gain buffer, providing a low input bias current and a low impedance output for driving the remaining circuitry. The transfer function through A1 is simply:

$$V_{LOWER} = V_{REF} - \Delta V \pm V_{OS1} \qquad [1]$$

where V_{OS1} is the input offset voltage of A1, and ΔV is some small percentage of V_{REF}. Op amp A2 is connected as an inverter working at a common mode voltage equal to V_{REF}. Its transfer function is given by:

$$V_{UPPER} = \frac{R_2}{R_1}\{\Delta V \pm V_{OS1} \pm V_{OS2}\} + V_{REF} \pm V_{OS2} \qquad [2]$$

where V_{OS2} is the input offset voltage of A2, and bias current errors are assumed to be very small.

If $\frac{R_2}{R_1}$ is nearly 1, then

$$V_{UPPER} = V_{REF} + \Delta V \pm V_{OS1} \pm 2V_{OS2} \qquad [3]$$

Since R1 = R2 = 2K and the resistor match very well over the temperature, then the above assumptions about bias current error and resistor ratio are correct. Therefore the limit as to how small ΔV can be is approximately 3 times the offset voltage, neglecting comparator offsets. If a worst case value of 8mV is assumed, the smallest value of ΔV is 24mV, corresponding to a fault tolerance of ±1%. Since this is the same order as the initial accuracy of the reference, ±2% is recommended as the tightest setting for the tolerance window.

DUAL CHANNEL DELAY WITH A SINGLE CAPACITOR

In supervisory circuits, delay is frequently required to reject false fault reports which could result from switching supply spikes or transients due to step load changes. The delay circuit in the SG1548 requires only one capacitor to implement the delay function for both the overvoltage and undervoltage channels.

The circuit depends on two factors for low false alarm rates:

1. Reports due to noise are of short duration compared to the program delay.

2. Noise causing false threshold crossings in each channel is essentially uncorrelated.

When all four voltages at the Sense pins fall within the set fault tolerance band, the output of each fault comparator is LOW. The

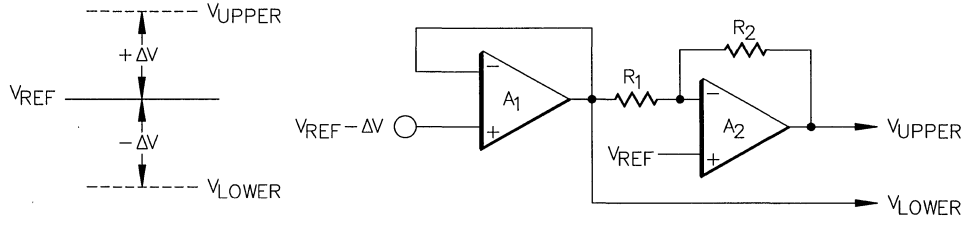


Figure 2. Generating a Precision Fault Tolerance Window

output of the 2-input NOR gate is HIGH, turning on the discharge transistor Q1. The Delay pin is held at ground. This is below the +1.25 volt trip threshold of the delay comparator, resulting in a LOW logic level to each of the output AND gates. Since both inputs must be HIGH to turn on the output drivers, no fault indication is possible.

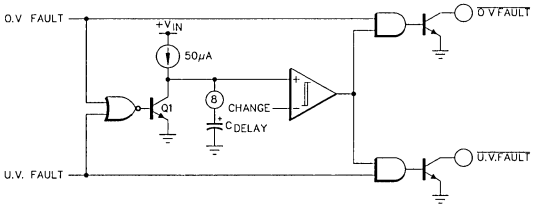


Figure 3. False Alarm Rejection Using a Single Capacitor

When one of the sensed voltages crosses a fault threshold, the fault comparator switches HIGH, turning off Q1. The delay pin voltage rises linearly from 0 volts as the 50μA current source charges the daily capacitor. If the fault condition persists long enough, the capacitor will charge to +1.25 volts, tripping the delay comparator, which has hysteresis to eliminate jitter due to the slow ramp. The HIGH output level from the comparator enables both output drivers, permitting an overvoltage and/or undervoltage indication as appropriate.

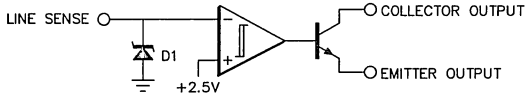


Figure 4. Block Diagram of the AC Line Sense Circuit

AC LINE SENSE COMPARATOR

The line Sense section of the SG1548 is a high-gain comparator with 25mV of hysteresis referenced to the precision +2.5 volt threshold voltage. The output transistor is rated at 40 volts and 10mA, and has uncommitted collector and emitter connections for either inverting or non-inverting operation. A unique clamp diode structure (D1) on the input adds to the versatility of this section, since it is specified for both forward and reverse conduction at 1mA. (Most junction-isolated integrated circuits can behave strangely or self-destruct if any pin is driven negative with respect to the substrate. The AC Line Sense pin was specifically designed to operate in this mode, thereby eliminating the need for an external clamp diode).

ON-CHIP INVERTING AMPLIFIER

The operational amplifier provided for converting a negative voltage to a positive one is optimized for inverter operation with the summing node at ground. The amplifier has a minimum open loop gain of 72dB, and is internally compensated for unity gain stability.

Like the AC line Sense input pin, the Inverting Input pin can be pulled below ground by nature of the external circuitry. To prevent the possibility of latch-up under these conditions, clamp circuitry as illustrated in Figure 5 exists at the pin. These protective components clamp negative excursions to $-0.5V_{BE}$ or approximately -0.3 volts at +25°C. This prevents the substrate diode from conducting and activating any parasitic SCRs in the IC. An additional diode limits the maximum positive input voltage to 1 V_{BE} to eliminate the possibility of latch up in the direction.

Input offset characteristics are further improved with a special Kelvin grounding scheme for the non-inverting input. Separate bounding pads exist at the periphery of the chip for power ground and the op amp input. The bond wires become common only at the IC package pin itself, eliminating the errors due to ground drops in the circuit metalization.

A performance factor called "inversion error" can be defined from the amplifier's electrical parameters which quantizes the total deviation from ideal inversion. It includes the effects of input offset voltage, input bias current, input offset current, and finite open-loop voltage gain. For unity-gain operation with perfect 10K/10K gain setting resistors, the maximum inversion error for the SG1548 is 26.5mV or 1.06% referred to the +2.5 volts fault window center. In most applications the error will be less. For example, if -15 volts is converted to +2.5 volts, the closed loop gain will be -1/6. The output stage can source at least 5mA, so 6K/1K gain resistors can be used. With these values the maximum inversion error falls to 13.5mV or 0.5%. The actual resistor tolerances will, of course, degrade this further.

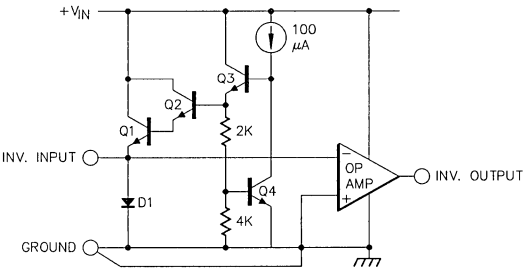


Figure 5. Protective Circuitry at the Inverter Input Terminals

SETTING THE FAULT TOLERANCE

The fault tolerance window is set by applying a voltage slightly less than the +2.50 volt reference to the Lower Threshold pin. In

the example shown in Figure 6, a ±2% window is programmed with the divider network formed by R_A and R_B. The maximum input bias current at Pin 1 is 1.0μA, so the divider current is chosen to be three orders of magnitude greater to minimize threshold shifts. With the resistor values shown, +2.450 volts is applied to Pin 1, setting up nominal ±50mV threshold values about the +2.500 reference. Resistors should be of the same type so that temperature coefficients will track, maintaining a constant divider ratio. The allowable voltage range on the adjustment pin is +2.45 volts to +1.50 volts, corresponding to ±2% and ±40% fault tolerance bands.

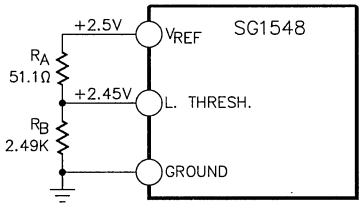


Figure 6. Programming the Fault Tolerance Window

IMPLEMENTING MULTIPLE TOLERANCES

In actual practice, some power supply tolerances may be more critical than others. For example, most +5 volt logic can withstand ±10% variations without malfunction, whereas the analog circuitry might require ±5% accuracy. Multiple tolerances can easily be obtained with the SG1548 using the technique shown in Figure 7.

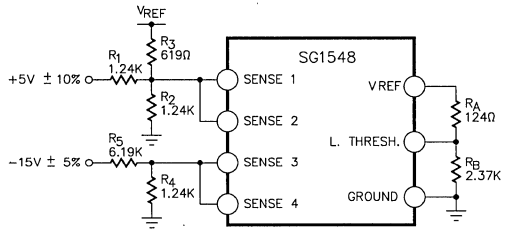


Figure 7. Implementing Multiple Tolerances

The Quad Power Fault Monitor is first programmed for the tightest tolerance required. In this case the +15 volt supply must be held within ±5% of its nominal value, so R_A and R_B are chosen such that ±125mV window edges are set at Pin 1, and pin 13 is set at 2.5v by R4 and R5 divider network. Next, the required tolerance of ±10% for the +5v input is set by adding a resistor R3 from the sense pin to the 2.5v reference. In this section a set of formulas are derived to calculate R1, R2, and R3 considering the effect of the sink current capability of the reference voltage.

Given: 1. Nominal Input Voltage - V_{NOM}
2. A programmed window tolerance - X%
3. A desired fault tolerance - Y%

1. Calculate: $P = (V_{NOM} - 2.5)/2.5$

2. Choose R_2 such that:

$$R_2 \geq (5)\,(Y\text{-}X)\,\left(\frac{P+1}{P}\right)$$

3. Calculate R_1 and R_3 by:

$$R_1 = PR_2$$

$$R_3 = \left(\frac{X}{X-Y}\right)\left(\frac{PR_2}{P+1}\right)$$

4. Calculate reference sink current:

$$I_{SINK} = \frac{(2.5)\,(X)}{R_3}$$

I_{SINK} calculated should be less than 500 μA.

5. Check your calculation by calculating fault tolerance Y:

$$Y = \left(\frac{R_1/R_3}{1 + R_1/R_2}\right)\,(X) \quad [\%]$$

This value should be very close to your desired value of Y.

EXAMPLE:
Given: 1. $V_{NOM} = 5V$
2. X = 5%
3. Y = 10%

1. Calculate P:

$$P = \frac{5 - 2.5}{25} = 1$$

2. Choose R_2:

$$R_2 \geq (5)\left(\frac{10 - 5}{100}\right)(2) = .50\ K\Omega$$

Choose $R_2 = 1.24K$

3. Calculate R_1 and R_3:

$$R_1 = R_2 = 1.24K$$

$$R_3 = \left(\frac{5}{10 - 5}\right)\left(\frac{1.24}{2}\right) = 620\ \Omega$$

Choose $R_3 = 619\Omega$

4. Calculate reference sink current:

$$I_{SINK} = \frac{(2.5 \times 0.05)}{619} = 202\ \mu A$$

5. Check Calculation:

$$Y = \left(1 + \frac{1.24 / 0.619}{1 + 1.24 / 1.24}\right)(5) = 10.008\%$$

INVERTING A NEGATIVE SUPPLY

Conversion of a negative source to +2.50 volts is straightforward, as shown in Figure 8. The op amp is operated at a closed loop gain less than unity. However, since the amplifier is internally compensated for unity gain, it is possible to monitor voltages less than 2.5 volts (gain greater then unity) without additional components for stability.

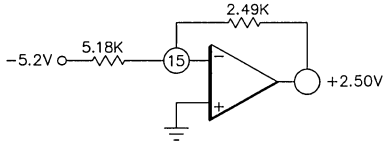


FIGURE 8. Inverting and Scaling a Negative Voltage

DETERMINING FAULT DELAY

Fault delay as a function of delay capacitor on Pin 8 is given by the graph in Figure 9. The line reflects the time required to charge a given capacitor to +1.25 volts with a nominal 50μA current source. Delays beyond several hundred milliseconds can be obtained, but for capacitor values beyond 5μF, the surge limiting circuit shown in Figure 10 is recommended. The 100ohm resistor limits the peak discharge current into the SG1548, while the external PNP transistor provides a high peak-current discharge path for the delay capacitor.

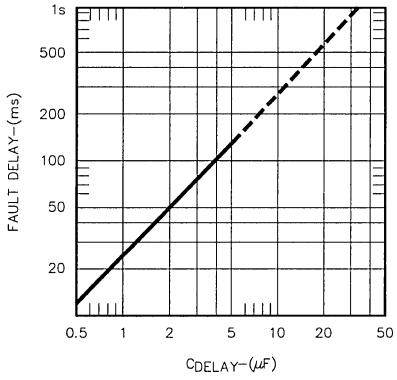


FIGURE 9. Graph of Fault Delay vs. Delay Capacitor

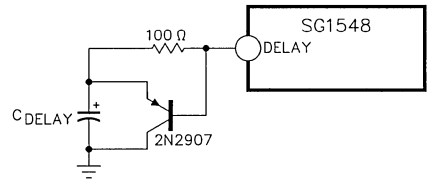
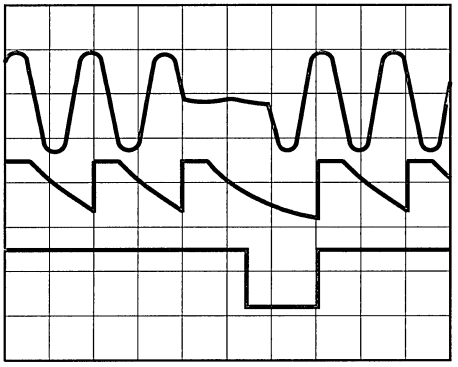


FIGURE 10. Suge Limit Circuit for Large Delay Capacitors

MONITORING THE AC LINE

Single-cycle AC line dropouts can be detected with the circuit shown in Figure 11. A positive half cycle is clipped to a precise level using the internal Zener and a 3K source resistor. The discharge circuit consisting of 180K and the 0.1μF capacitor control the voltage decay so that the +2.5 volt trip point is not reached with normal sinusoidal line conditions. A single-cycle dropout will provide an extra 16.7 milliseconds discharge time, as shown in Figure 12, causing the Line Fault output to switch LOW.



HORIZONTAL: 10mSEC/DIV.
UPPER TRACE: AC LINE
MIDDLE TRACE: PIN 5 AT 5V/DIV.
LOWER TRACE: LINE SENSE OUTPUT AT 5V/DIV.

FIGURE 12. Response to a Single-Cycle Line Dropout

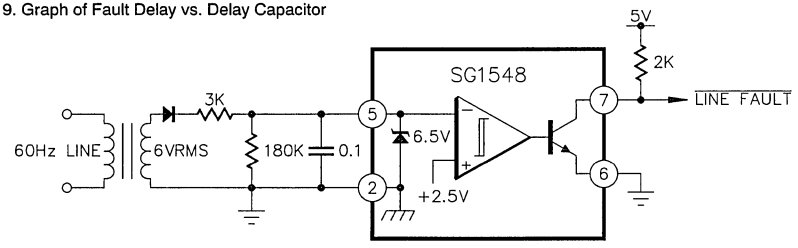


FIGURE 11. Monitoring the AC Line for Sindle-Cycle Dropout

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LINE CLOCK GENERATION

A logic clock derived from the line frequency can be obtained with a minimal number of components, as illustrated in Figure 13. The internal clamp diode is used in both forward and reverse conduction modes, with the 10K input resistor limiting peak input current to less than 1mA. Waveforms obtained with this circuit are shown in Figure 14.

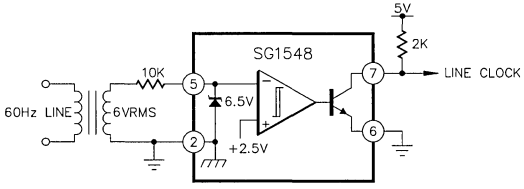
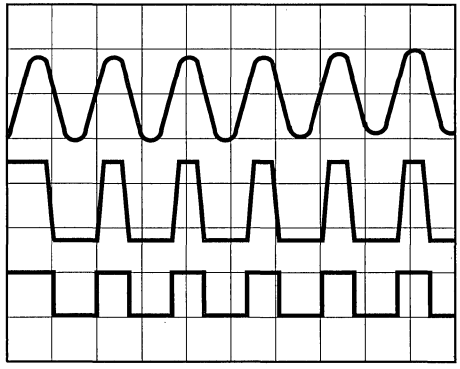


FIGURE 13. Generating an AC Line Clock



HORIZONTAL: 10mSEC/DIV.
UPPER TRACE: AC LINE
MIDDLE TRACE: PIN 5 AT 5V/DIV.
LOWER TRACE: LINE SENSE OUTPUT AT 5V/DIV.

FIGURE 14. Waveforms Produced by the Line Clock

UNDERVOLTAGE LOCKOUT

Figure 15A and B shows two methods of using the Line Sense comparator for inhibiting power supply start-up until some minimum supply voltage has been reached. In the first case a HIGH-going shutdown signal to the PWM control is generated until V_{IN} causes the voltage at Pin 5 to exceed +2.5 volts. If the PWM is on the primary side of the power transformer, the Line Sense Output can directly drive an optocoupler. In the second case the line sense comparator is used to gate a bias supply ON when the proper working voltage has been reached.

EXPANDING THE QUAD POWER FAULT MONITOR

The SG1548 is readily expandable to include additional positive and negative supplies. One half of an inexpensive quad comparator IC is required for each supply, as shown in Figure 16.

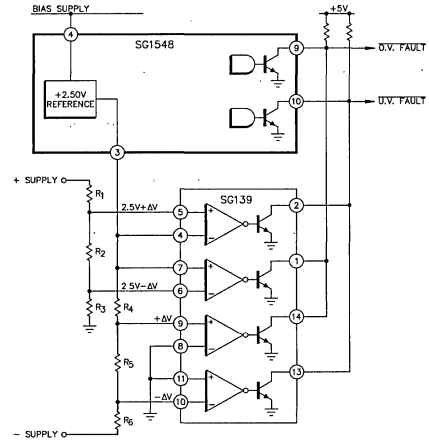
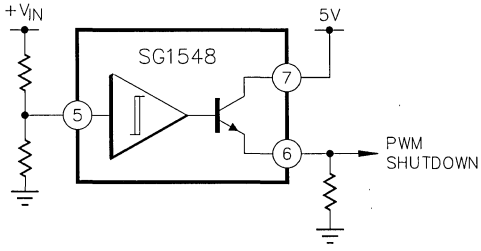


FIGURE 16. Expanding the SG1548 to Monitor Additional Supplies



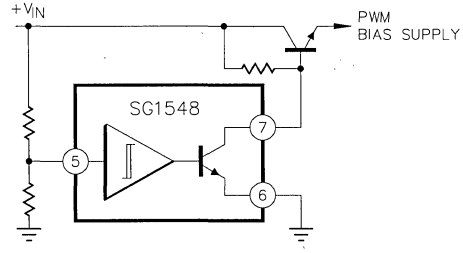


FIGURE 15A & 15B. Using the Line Sense for Undervoltage Lockout

For an additional positive supply, the comparators are referenced to the +2.5 volt regulator of the SG1548. The monitored supply is divided down by resistors R1 through R3. When the supply drops a given percent, the upper comparator switches LOW. Since the fault outputs of the SG1548 are active LOW, the indication from the quad comparator can be wire-ORed to the undervoltage fault output line. Similarly, if the supply voltage increases beyond a preset limit, the overvoltage fault line will be pulled LOW by the second comparator.

The negative supply is handled similarly, except that the comparators are referenced to ground, and the resistive divider R4 through R6 is returned to the +2.5 volt reference. The 139 quad comparator will work correctly as long as the inputs are not pulled below -0.3 volts. If this possibility exists, a Schottky clamp diode should be used at Pin 10 to preserve the overvoltage indication in case of a massive negative overdrive at the divider input.

A COMPREHENSIVE EXAMPLE

Each section of the SG1548 Quad Power Fault Monitor has been described in detail. Now it is time to put all the pieces together and show power supply supervision in an actual system. For our example we will use the hypothetical personal computer mentioned at the beginning of this paper. Figure 17 shows all the components required.

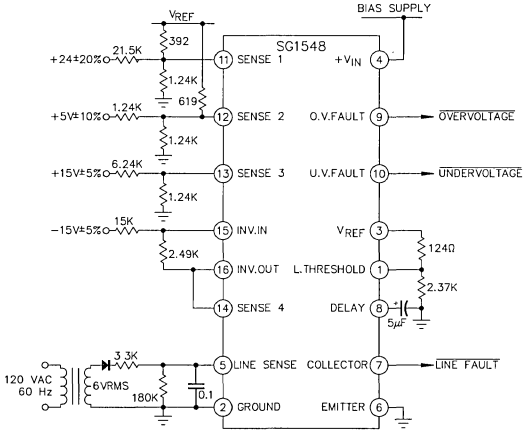


FIGURE 17. Monitoring Four DC Supplies and the AC Line

In this case, four DC voltages are monitored: three positive and one negative. Three different fault tolerances are mechanized, and the AC line is checked for single-cycle dropout.

The ±15 volt supplies are the most critical, requiring ±5% accuracy. The 124ohm/2.37K divider from the reference sets this tolerance in the fault window generator. The -15 volt supply is converted to +2.50 volts with the inversion amplifier on the chip and applied to one of the Sense inputs. The +5 and +24 volt supplies are not as critical, requiring ±10% and ±20% respectively. Divider resistors to the reference are used to scale the effective windows accordingly. The single 5μF capacitor provides 125 milliseconds of delay before an out-of-tolerance fault is reported.

All this is accomplished with one 16-pin integrated circuit and 14 resistors, 2 capacitors, a low-current diode, and a line isolation transformer, which can be part of the bias supply.

CONCLUSION

The opportunity to realize comprehensive power supply fault monitoring with low component count is a reality with the introduction of the SG1548 Quad Power Fault Monitor. A combination of flexible architecture combined with innovative circuit design techniques has resulted in a supervisory function with excellent accuracy and repeatability over the full military temperature range of -55°C to +125°C.

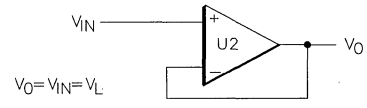
APPENDIX - A

Derivation of over voltage trip in terms of R_1, R_2, R_3, R_4, R_5.
Looking at Figure 1:
Lower Threshold voltage is calculated by:

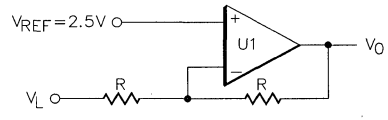
$$V_L = \frac{R_B}{R_B + R_A} V_{REF} = V_{REF} - \Delta V \qquad (1)$$

$$\text{where } \Delta V = \frac{R_A}{R_A + R_B} V_{REF} \qquad (2)$$

Op-amp (U2) is configured as a unity gain follower, therefore:



Upper threshold is calculated as:



$$V_O = (1 + \frac{R}{R}) V_{REF} - \frac{R}{R} V_L = 2V_{REF} - V_L$$

But V_L was calculated to be:

$$V_L = V_{REF} - \Delta V \qquad (2\text{-a})$$

$$V_O = 2 V_{REF} - (V_{REF} - \Delta V) = V_{REF} + \Delta V$$

We will call the output of U1 op-amp upper threshold UMIT and designate it by V_U, so:

$$V_U = V_{REF} + \Delta V \qquad (3)$$

Next we will analyze the circuitry associate with O.V sensing circuit. We also assume, it is required to have higher threshold voltage setting than the one being programmed by R_4, R_5 divider.

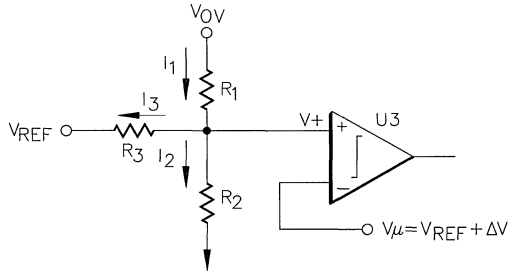


Figure 2

From the schematic of figure 2, we have:

$$V_T = V_U = V_{REF} + \Delta V$$

and writing K.C.L. for V_T node, we get:

$$I_1 = I_2 + I_3$$

$$\frac{V_{OV} - V_T}{R_1} = \frac{V_T}{R_2} + \frac{V_T - V_{REF}}{R_3}$$

$$\text{or :} \quad V_{OV} = (1 + \frac{R_1}{R_2})(V_{REF} + \Delta V) + \frac{R_1}{R_3} \Delta V \qquad (4)$$

$$\text{where } \Delta V = \frac{R_A}{R_A + R_B} V_{REF}$$

Equation (4) can only hold if the following is true:

(4-a) $I_2 >> I_{BIAS}$ where: I_{BIAS} is the bias current of U_3 comparator

and

(4-b) $I_3 < I_{SINK\ MAX}$ where: $I_{SINK\ MAX}$ is the maximum sink current capability of the reference voltage.

Derivation of equation for R_3:

Assumtion:

V_{OV1} ≅ O.V trip point set by R_4, R_5 (lower threshold)
V_{OV2} ≅ O.V trip point desired ($V_{OV2} > V_{OV1}$)
x ≅ percent voltage above nominal for V_{OV1}
y ≅ percent voltage above nominal for V_{OV2}

From the definitions of x and y we get:

$$V_{OV1} = (x + 1) V_{NOM} \qquad (7)$$
$$V_{OV2} = (y + 1) V_{NOM} \qquad (8)$$

We also know that:

$$V_{OV1} = (V_{REF} + \Delta V)(1 + \frac{R_1}{R_2}) \qquad (9)$$

and from equation (4)

$$V_{OV2} = (V_{REF} + \Delta V)(1 + \frac{R_1}{R_2}) + \frac{R_1}{R_3} DV \qquad (10)$$

Replacing (7) and (8) into (9) and (10) and subtracting (9) from (10) we get:

$$(y - x) V_{NOM} = \frac{R_1}{R_3} \Delta V \qquad (11)$$

or

$$R3 = \frac{R_1 R_2}{R_1 + R_2} \times \frac{1}{y - x} \times \frac{\Delta V}{V_{REF}} \qquad (12)$$

We also know that the relation between V_L and V_{REF} is:

$$V_L = (1 - x)\, V_{REF} \qquad (13)$$

Since VL is x percentage lower than VREF by R3, R4 divider, putting (13) into equation (2-a) we get:

$$\Delta V = xV_{REF} \qquad (14)$$

Replacing (14) into (12) we get the result:

$$R3 = \left(\frac{R_1 R_2}{R_1 + R_2}\right)\left(\frac{1}{y - x}\right) \qquad (15)$$

Deriving a set of formulas for R_1, R_2, R_3 calculation:

From the inequality of 4-b we get:

$$R_3 >= \frac{\Delta V}{10^{-3}}\ \Delta V\ (KR) \qquad (16)$$

I_{BIAS} maximum for 1548 comparator is 1mA.

we know that:

$$V_{NOM} = \frac{R_2}{R_1 + R_2} \qquad (16\text{-a})$$

$$R1 = \left(\frac{V_{NOM} - V_{REF}}{V_{REF}}\right) R_2 = PR_2 \qquad (17)$$

$$\text{if} \quad P \cong \frac{V_{NOM} - V_{REF}}{V_{REF}}$$

From equation (15), (16) and (17) we get:

$$\left(\frac{x}{y - x}\right)\left(\frac{PR_2}{P + 1}\right) > \Delta V$$

$$\text{or } R_2 > (\Delta V)\left(\frac{P + 1}{P}\right)\left(\frac{y - x}{x}\right) \text{ where } R_2\ [KR] \qquad (18)$$

From equation (14) we have:

$$\Delta V = xV_{REF}$$

and replacing V_{REF} by 2.5 in equation 18) we get:

$$R2 > (2.5)(y - x)\left(\frac{P + 1}{P}\right) \qquad (19)$$

Using equations (17), (19) and (15) we can calculate R1, R2, and R3 values.

To calculate the reference sink current we use:

$$I_{SINK} = \frac{\Delta V}{R_3} = \frac{x\, V_{REF}}{R_3} = \frac{2.5x}{R_3}$$

To derive the equation for checking we start by equation (4):

$$V_{OV} = (V_{REF} + \Delta V)\left(1 + \frac{R_1}{R_2}\right) + \frac{R_1}{R_3}\Delta V$$

or

$$V_{OV} = V_{REF}\left(1 + \frac{R_1}{R_2}\right) + \Delta V\left(1 + \frac{R_1}{R_2} + \frac{R_1}{R_3}\right) \qquad (20)$$

putting equation (8) in (20) we get:

$$V_{NOM} + yV_{NOM} = V_{REF}\left(1 + \frac{R_1}{R_2}\right) + \Delta V\left(1 + \frac{R_1}{R_2} + \frac{R_1}{R_3}\right) \qquad (21)$$

Replacing (16-a) into (21) we get :

$$y = \frac{\Delta V}{V_{NOM}}\left(1 + \frac{R_1}{R_2} + \frac{R_1}{R_3}\right) \qquad (22)$$

Replacing (14) and (16-a) into (22) we get:

$$y = \frac{x}{\left(1 + \frac{R_1}{R_2}\right)}\left(1 + \frac{R_1}{R_2} + \frac{R_1}{R_3}\right)$$

or

$$y = \left(1 + \frac{\frac{R_1}{R_3}}{\left(1 + \frac{R_1}{R_2}\right)}\right)$$

PROTECT YOUR SWITCHERS WITH DIGITAL CURRENT LIMITING

A New Current Sense Latch IC Provides Pulse-by-Pulse Current Control

Stan Dendinger
Manager, Advanced Product Development
Silicon General, Inc.

INTRODUCTION

Another new class of integrated circuits, designed specifically to ease the plight of the switch-mode power supply designer, has just been established with the introduction of the SG1549 Current Sense Latch IC. Although there have been many IC products developed over the past few years to provide simple methods of voltage control for switching supplies, the SG1549 is the first to specifically address and take a fresh approach to the problem of current control. Almost all existing PWM chips have included some type of circuit for current limiting, but these have all used the same techniques as linear regulators; that is, a current sense amplifier generates an error signal linearly proportional to load current which, after reaching an established threshold, takes command away from a voltage control amplifier. Thus, upon overload, the power supply switches from a voltage feedback loop to a separate current feedback path. Each loop must be stabilized separately and, because of the output filter, stable performance along with a reaction fast enough to protect the high-speed switching transistors is difficult to achieve. What is needed for optimum protection is a circuit which operates at the switching frequency and immediately turns off the main current-carrying switching transistors upon current overload. Turn-off must be rapid, without allowing the transistors any appreciable time in their linear operating region, and with no oscillation or multiple-pulsing.

A DIGITAL CURRENT LIMITER

The optimum approach to switch-mode current limiting is to treat each on-cycle as a separate problem. That is, pulse-by-pulse current limiting. This is implemented by a device-monitoring current build-up each time the power supply's switching transistor conducts and, upon sensing an overcurrent condition, immediately turning the transistor off and holding it off for the duration of that normally on period. Such a circuit must have a latch, as once turn-off is achieved, the removal of the overcurrent signal would otherwise allow the transistor to return to conduction. Including a latch means a provision for reset must also be provided.

All of this and more is offered by the SG1549 Current Sense Latch IC. From the block diagram of this device, it can be seen that the circuit includes a comparator with positive feedback, a means for establishing an input threshold of 100mV, a reset circuit, complementary outputs, and a high voltage level-shifting circuit. This device is designed to be completely compatible with many commonly-used Regulating PWM control IC's such as the SG1524, MC3420, and the TL494. Requiring only 2mA of supply current, the enter circuit can be operated from the reference voltage available with these chips, with reset accomplished by their clock output signals.

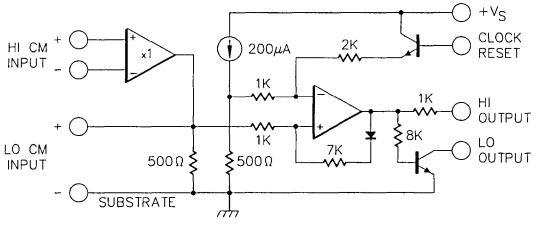


Figure 1. The SG1549 Current Sense Latch IC contains provision for sensing a current threshhold over a wide voltage range. Complementary outputs and a latch with reset are also a part of this new protection circuit.

Although obviously designed for use with switch-mode power supplies, the SG1549 has broader application as a general purpose, low-threshold latch. A clock signal is not the only way to provide reset; that function may also be accomplished by any operation which will momentarily pull the reset pin high.

CIRCUIT OPERATION

For a detailed understanding of the operation of this device, refer to the schematic of Figure 2. With a +5 volt supply, a threshold reference is established by a current through R3. This current is mirrored by Q7 to provide a constant 200μA through R11, thereby holding one input to the comparator at 100mV above ground. That same current is mirrored through Q4 to the floating threshold circuit of Q1-Q3, D1, and R1. This portion of the circuit will convert a differential voltage between pins 1 and 2 into an identical voltage across R2. It will do this accurately while allowing the absolute voltage on pins 1 and 2 to range from 2 to 40 volts with respect to ground.

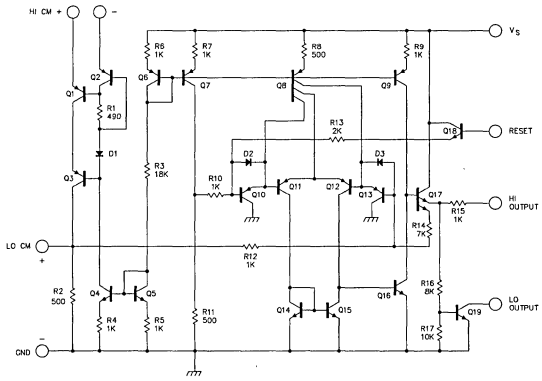


Figure 2. The heart of the SG1549 is a high-speed comparator together with an input threshhold level-shifting circuit.

Since the other input to the comparator is tied to pin 3, it can be seen that the comparator will switch when the voltage on pin 3 rises to 100mV, regardless of whether that voltage is applied to pin 3 directly or differentially between pins 1 and 2.

Once the comparator switches, positive feedback provided by Q17 and R14 will hold it latched until a reset signal, effected by raising pin 7 above 2 volts, momentarily increases the threshold returning the circuit to its initial state.

Transistor Q17 also provides two outputs: a high-going signal on pin 6 which can source 2mA and a open-collector saturating transistor on pin 5 which can sink more than 10mA. With complementary outputs, a variety of shutdown options are offered. Typical delay times for the SG1549 are 180nSec from the LO CM input and 300nSec from HI CM to the outputs.

HIGH LINE SENSING

A very straightforward application of the SG1549 is its use for current sensing in the input line. This switching regulator is shown in Figure 3. The switching regulator is shown implemented with the SG1524 PWM control IC and it can be seen that interfacing between these two chips couldn't be easier. The value for RSC is determined by dividing the 100mV input threshold by the peak current desired. High frequency noise, or switching transients can usually be eliminated by a small capacitor between pins 3 and 4. The current shutdown command can be coupled into the SG1524

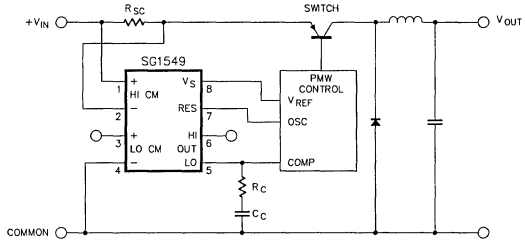


Figure 3. Using the SG1549 to sense input current to a simple buck converter and interface directly to a PWM control IC such as the SG1524.

by either connecting the HI-OUT, pin 6 to the SG1524's shutdown pin or, as shown here, using the LO-OUT pin to pull the compensation terminal low. In either case, activation of the current sense latch will tend to discharge the compensation capacitor, C_C which may cause slow recovery from pulse limiting. Keeping the value of C_C as small as possible within the requirements of voltage loop stability will minimize this effect; however, slow turn-on from current limit is often desirable and can be optimized by using the LO-OUT signal to discharge a soft-start network instead of coupling directly into the SG1524.

Where minimizing turn-off delay is important, the command from the SG1549 may be taken directly to the output stage of a switching regulator. A practical means of accomplishing this is shown in Figure 4 where the power switch consists of an SM625 15-amp hybrid circuit containing both the power switch and the commutating diode. This switch is driven by using the SG1524 to switch a constant current source formed by the 2N2222 transistor connected with its base to the 5 volt V_{REF} line through a 1k resistor. By connecting the LO-OUT terminal of the SG1549 to the base of the 2N2222, drive current to the output stage can be interrupted without the delays inherent in the SG1524.

LOW LINE SENSING

In many types of feed-forward or push-pull converters, current protection may be provided by sensing through an emitter resistor referenced to ground on the primary side of an output transformer. The fast-reacting SG1549 can easily sense secondary overload as reflected back to the primary and, additionally, provide protection from unbalanced transformer saturation. When using the LO CM inputs as shown in Figure 5, the HI CM inputs should be shorted together.

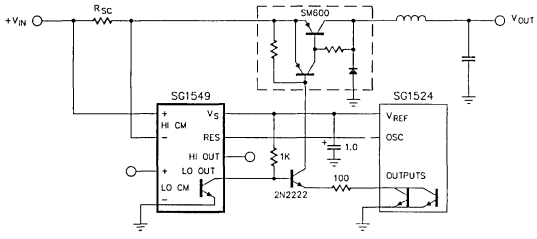


Figure 4. A fully-protected, high performance single-ended switching regulator is easily implemented with two IC's and a hybrid switch. Current control is direct to the power switch for fastest response.

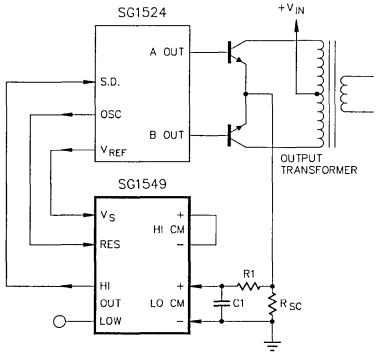


Figure 5. When sensing emitter current, a small input filter is often useful in eliminating transients to the SG1549

While the LO CM inputs may be connected directly across a sense resistor, R_{SC}, a small low-pass filter, R1-C1, is often helpful in removing high frequency transients. It must be remembered that the 500ohm input impedance to the LO CM terminal will cause the use of R1 to increase the effective threshold; however, this also offers the possibility of an easily adjustable threshold by incorporating a potentiometer at the input to the SG1549.

Coupling the current shutdown command back to the control circuit may be done in several ways as described above, but again, the fastest approach is to go directly to the output switches. Figure 6 shows such an approach by adding two external shutdown transistors, Q1 and Q4. In this circuit, these transistors perform double-duty by the use of C2, R3 and R4 to generate a positive pulse when the main power switches, Q2 and Q3, are commanded off by the SG1524. Turn-off signals from either the PWM or the SG1549 are summed together through diodes D2 and D3 to Q1 and Q4.

One problem often experienced with using pulse-by-pulse current limiting with a push-pull inverter is half-cycling caused by limiting

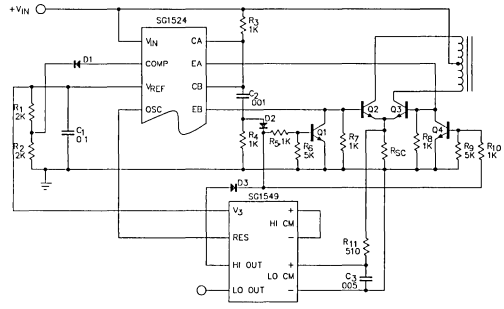


Figure 6. Fastest turn-off response is achieved by taking the output of the SG1549 direct to the power switches through turn-off transistors, Q1 and Q4

on one period without full recovery in time for the next. A maximum duty-cycle clamp, formed by R1, R2 and D1 in Figure 6, minimizes this effect by holding the error amplifier out of saturation when the feedback voltage begins to fall.

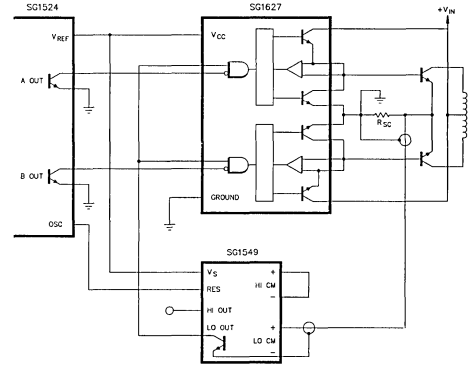


Figure 7. An SG1627 provides both power gain for the voltage control signal as well as a high-speed interface for the SG1549's current protection.

Another convenient way to tie the output of the SG1549 into the PWM control in higher power applications is by using the SG1627 Dual Interface Driver and connecting LO-OUT terminal directly to the two non-inverting inputs of the SG1627 as shown in Figure 7. The N.I. inputs of the SG1627 will force the outputs off regardless of the commands on the inverting inputs, and do so within 100 nanoseconds.

And finally, keep in mind that the LO-OUT terminal of the SG1549 will easily drive most high-speed optical couplers should some type of isolation between current sense and shutdown control be required.

MINIMIZING THE COST AND COMPLEXITY OF START-UP CIRCUITS FOR SWITCHING POWER SUPPLIES

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Applications Manager
Silicon General, Inc.

INTRODUCTION

Power supply designers are often faced with choosing an optimun circuit topology based on a specific set of requirements. Though the hypothetical optimum design may vary substantially from one set of specifications to another, some of the most important criteria in many power supply applications are cost, size, weight, reliability and efficiency. Based on such parameters, designers often will choose between operating the pulse-width modulation (PMW) control IC referenced to either the primary-or secondary-side return. In either case, they must provide the dc power needed to operate that IC. Although a number of ways to generate this auxiliariy supply voltage exist, some of the most common methods used are a 60-HZ transformer, linear regulator, self-oscillating dc chopper or an internal bootstrap.

Auxiliary 60-Hz transformers are used in off-line switchers to step down the input ac line voltage, which is then rectified and filtered to power the control IC. Although it is straightforward, this approach requires the use of low-frequentcy magnetics that are relatively heavy and occupy a considerable amount of pc-board real estate.

The size of the auxiliary 60-Hz power transformer can be a big factor in low-power switchers, which are typically very small. In these instances, the transformer can easily approach 30% of the total volume occupied by the supply. To accommodate the transformer, the supply's overall size would have to be increased, thus increasing its cost as well. Because of this, the PWM control circuits are not usually powered from an auxiliary 60-Hz transformer unless they must be referenced to the secondary side return.

Linear Regulators are typically used in dc/dc converters operating on inputs of less than 60 volts. If the input voltage is less than 30 volts, the designer often chooses a three-terminal voltage regulator. If the input is greater than 30 volts, a discrete series-pass regulator is usually used, with a zener diode providing the reference voltage.

Unfortunately, both of these approaches are inherently inefficient because of the power being dissipated in the series-pass element. Moreover, as the input voltage increases, the power dissipation also increases, with a corresponding decrease in efficiency. And since the input power is derived from the primary side of the switcher's power transformer, the PWM control circuit must be referenced to the primary-side return. As a result, the supply must include additional analog circuits on the secondary side and provide primary-to-secondary isolation through an opto-coupler or isolation transformer.

Self-oscillating dc choppers can be used in either off-line switches or in dc/dc converters. In either case, the dc applied to the switching circuit is also applied to a self-oscillating chopper built around a saturable core. The chopper converts the dc into a high-frequency ac square wave that is stepped down, rectified and filtered to provide the dc power required by the PWM control circuits.

Since the frequency of operation is often above the 20-KHz range, the selected magnetics are much smaller than a comparable 60-Hz transformer. The chief disadvantage of this approach is the need for two high-voltage switching transistors, the cost of which more than offsets any savings achieved by use of smaller magnetics. Because of this, choppers are usually used only in dc/dc converters intended for use in telecommunications, aerospace and other high-reliability applications.

Bootstrapping employs an auxiliary startup power supply and a special winding on the main power transformer. Once the supply's operation has stablized, this winding provides all the power required to operate the PWM control circuits. However, when ac power is first applied to the supply, the bootstrap winding provides no output. Instead, the PWM control circuits are powered entirely by the auxiliary startup supply. But as the switching transistors begin to function, voltage appears across the bootstrap winding. Eventually this winding, with its associated recti-

fier/filter circuit, takes over the task of powering the PWM control circuits, and the startup circuit shuts down.

Because the startup circuit must provide power for only the period required for the switch-mode regulator to stabilize-the supply's turn-on delay-very little power is dissipated in the start-up circuitry. But this approach requires a relatively large number of discrete components, especially when the design calls for the PWM control circuit to be referenced to the secondary-side return. With the availability of monolithic boostrapping startup circuits, however, these components can be replaced with a single integrated circuit. Figures 1 and 2 show block diagrams of the bootstrap method for primary and secondary side operation.

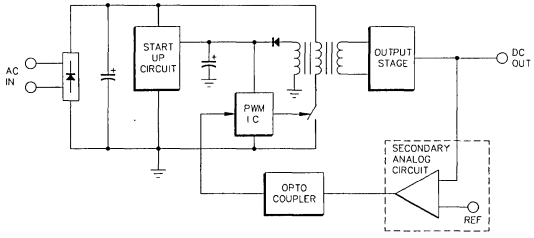

Figure 1. Primary Side Start-up Circuit

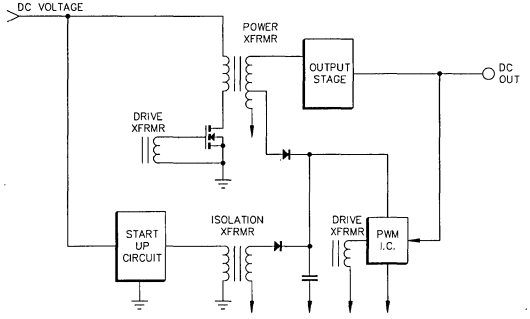

Figure 2. Secondary Side Start-up Circuit

A MONOLITHIC BOOTSTRAPPING STARTUP

A simplified schematic diagram showing how the monolithic startup circuit, an SG1540 is connected into a typical power supply, can be found in Figure 3. As can be seen, the PWM control IC, an SG1526 in this case, receives power from two sources logically "ORed" at pin 14.

When ac power is first applied, capacitor C3 is charged through resistor R2. When its voltage reaches the turn-on threshold, a self-contained chopper in the SG1540 is turned on with the resulting high-frequency ac being applied to the primary winding of transformer T2. The resulting voltage appearing across the secondary is rectified, filtered and applied to the dc input of the PWM control IC at pin 14. With the application of dc power at pin 14, the PWM control IC turns on the switching transistors and power is soon applied to the primary of transformer T1, the main power transformer. As a result, voltage is induced in the bootstrap winding, AB. This voltage is rectified, filtered and applied to pin 14 of the PWM control IC. Because its voltage is higher than that provided by the SG1540 through transformer T2, it provides all the power used by the PWM control IC.

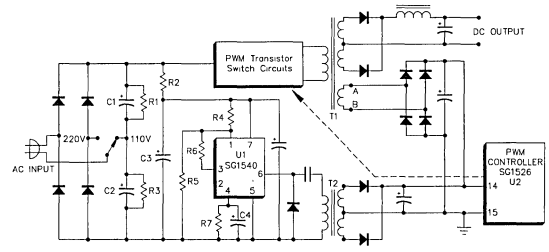

Figure 3. Schematic Diagram of the Bootstrap Start-up-power Circuits

During the period of time that has elapsed for this to occur, energy has been drawn out of capacitor C3 to power the control circuits through the SG1540. As a result, the voltage across C3 has decreased. As energy continues to be withdrawn, the voltage eventually falls below the SG1540's turn-off threshold and its self-contained chopper turns off. When this happens, transformer T2 no longer provides power to the rectifier connected to its secondary winding. This has no effect on T2 or the SG1540, because the diodes in the rectifier isolate them from voltage being produced by the bootstrap winding.

Of course, once the SG1540 turns off, energy is no longer withdrawn from C3 and, as a result, its voltage increases and the SG1540 is again turned on. However, because the bootstrap voltage is higher, the SG1540 does not supply any power to the PWM control circuits. Instead, it simply alternates between being on in an idling mode and being tuned off as the voltage across C3 rises and falls. The primary side operation is the same except the AB winding is wound on the primary side. (See Figure 5 in the comparator section.)

EXPLANATION OF THE INTEGRATED CIRCUIT

The SG1540 consists of three main sections, as shown in Figure 4; a micropower bandgap comparator/power switch, a high-frequency square wave oscillator with a 200-milliamp totem-pole output stage, and a second bandgap comparator with latching crowbar to protect against overvoltage faults while starting or running.

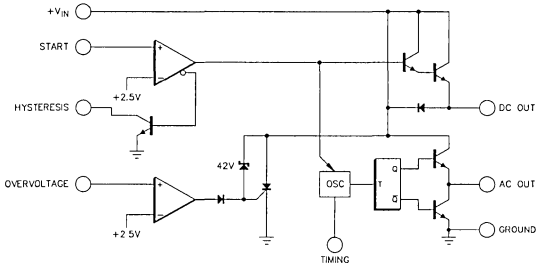

Figure 4. 1540 Block Diagram

The Comparator Circuit

The operation of the circuit is best explained by referring to Figure 5. A micropower comparator (U1) is referenced to an internal low-drift bandgap source that provides +2.5 volts to one input of both the startup and overvoltage comparators. The overall tolerance of this reference voltage, over the full operating temperature range, is ±130 millivolts. However, this reference is not available for any external connections. Also included is a hysteresis transistor (Q1) facilitating external programming of turn-on and turn-off voltage thresholds.

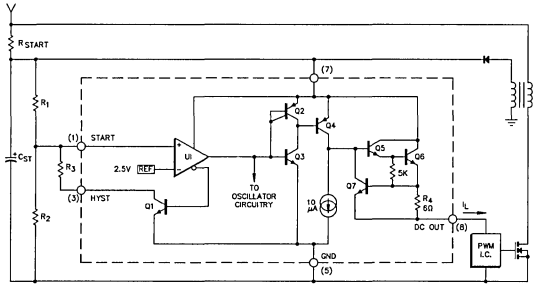

Figure 5. Simplified Schematic Diagram of the Comparator Circuit

When voltage is first applied to the IC, pin 2 is set lower than 2.5 volts by the voltage divider composed of R1 and R2. This causes the output of the comparator to be switched low. When this happens, transistors Q3, Q4, Q5 and Q6 are biased off, isolating startup capacitor C_{START} from its load. At the same time, transistor Q1 is turned on, placing R3 in parallel with R2 and forcing the voltage at pin to drop even lower. During this time, the quiescent current drawn by the IC is less than 1 milliamp, which allows the startup capacitor voltage to ramp up towards the high-voltage dc supply through startup resistor R_{START}.

Once the startup threshold is reached, the base of Q1 transistor switches low and causes Q1 to be turned off. This raises the voltage at pin 2 to a higher value, determined by the R1-R2 voltage divider. At the same time, the other output of the comparator activates the osillator circuitry and through Q3, Q4 transistors turns the Darlington pair (Q5-Q6) on. When the Darlington pair is turned on, they provide a path through which the energy stored in the startup capacitor C_{START} can flow to the PWM control circuit. During the discharge time, the voltage induced in the flyback winding will be rectified and filtered by D1 and C_{ST} to provide the DC voltage. Note that the startup capacitor must be large enough to store sufficient energy to generate a bootstrap voltage that can meet all power requirements of the control circuits in the supply.

The Q5-Q6 Darlington pair is protected against any load transients or short-circuit conditions by internal current limiting. The maximum allowable output current is determined by the ratio of base-emitter voltage of transistor Q7 to the voltage across resistor R4. A typical value for the short-circuit current is 100 milliamps at 25°C, but as the temperature increases the current-limit threshold decreases. Figure 6 shows the Darlington saturation voltage vs load current.

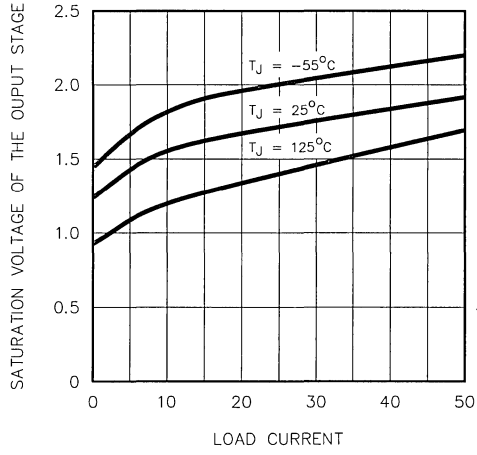

Figure 6. Output Transistor Voltage v.s. Load Current

Oscillator and AC Output

A simplified schematic block diagram of the oscillator is shown in Figure 7. The oscillator's frequency is determined by the values of an external resistor, R_T, and capacitor, C_T (R7 and C4 in Figure 3). Their values can be obtained from the chart in Figure 8. When voltage is first applied to the IC, capacitor C_T is completely discharged and switch S1 remains open. Even though the input voltage rises, switch S1 remains open until the startup threshold is reached. When it is reached, the startup comparator (see Figure 5) changes its output state, causing switch S1 to close. As soon as it closes, capacitor C_T rapidly charges through resistor R1 towards input voltage V_{IN}. Once the voltage across C_T reaches 0.7 volts, the output of comparator U1 changes state.

Despite the change of U1's output state, switch S1 remains closed due to the action of a latch circuit, and the voltage across C_T continues to rise towards V_{IN}. When it reaches approximately 2.1 volts, the output of comparator U2 goes high. This resets the latch circuit and opens switch S1. When switch S1 opens, capacitor C_T is isolated from V_{IN} and begins to discharge through resistor R_T. As the discharge continues, the voltage across C_T decreases and when it finally falls to 0.7 volts, the output of comparator U2 goes low, closing switch S1 and beginning the cycle again.

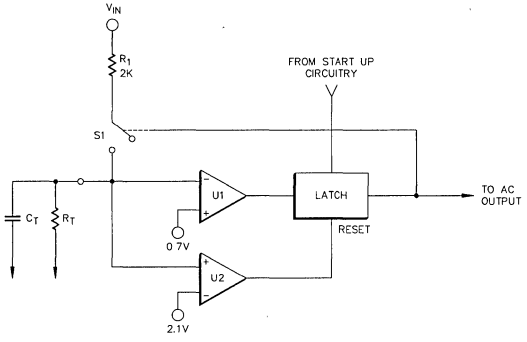

Figure 7. Block Diagram of the Internal Oscillator used to Drive the SG1540's Chopper Circuit

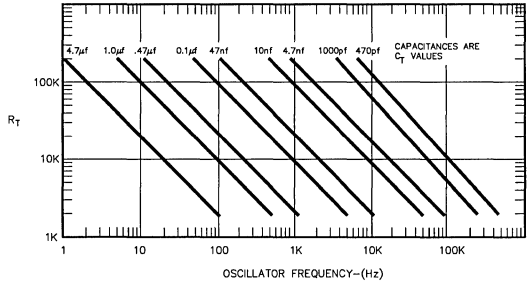

Figure 8. 1540 Oscillator Frequency Chart

A square-wave ac output is generated by driving a flip-flop from the output of the latch circuit. The flip-flop's output is applied to a totem-pole output stage. The output transistors have maximum peak-current capabilities of 200 milliamps, which is enough to power the control circuits of most switching power supplies during the startup period. Note that if the oscillator circuit is not being used, pin 4 should be connected to pin 7.

Overvoltage Circuit

The overvoltage circuitry is intended to protect the IC against any overvoltage faults during startup and any period it is active. The circuit is shown schematically in Figure 9 and consists of a comparator, composed of Q2 and Q3 referenced to 2.5 volts, a latching crowbar circuit, composed of Q6 and Q7, and a zener diode, Z1. When the voltage at pin 7 exceeds the threshold set by the R1-R2 voltage divider, pin 2 rises above 2.5 volts, causing transistor Q5 to turn on. This, in turn, turns off output transistors Q9 and Q10 and activates an SCR crowbar. When pin 2 is not used to program the overvoltage condition, the SCR can still be activated by allowing the voltage at pin 7 to exceed the zener diode's nominal 42-volt avalanche voltage. Note that when the overvoltage circuit is not being used, pin 2 should be tied to ground.

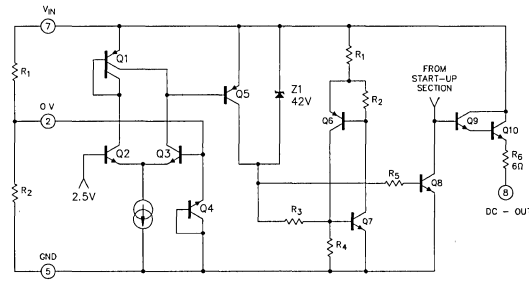

Figure 9. Simplified Schematic Diagram of the Overvoltage Protection Circuit in the SG1540

DESIGN EXAMPLE

The power supply design discussed in this section uses a fairly common, straight forward circuit. It is intended to show the application of the SG1540 I.C. in one of the modes of its application, namely secondary side PWM operation. This mode of operation was chosen over the primary side, simply to show the dramatic reduction in the size and weight of the auxiliary supply compared to applications where 60Hz transformers are being used.

Circuit Description

A general description of the SG1540 in a typical power supply was given in section "A MONOLITHIC BOOTSTRAPPING STARTUP". We will now design a complete power supply using the same circuit topology of Figure 3 with an SG1540 as the start up controller. As can be seen from Figure 10, the input rectifier bridge is arranged for connection either to 117 Vac or 220 Vac line. The circuit uses a pair of 400 volts MOSFET's in a Half Bridge circuitry and a pair of high speed rectifiers for the output stage. The MOSFET's are driven directly from the totem-pole output stages of an SG1526 control chip through an isolation transformer. This provides the fast current turn-on and turn-off pulses needed for MOSFET gates.

Current limiting is done with current transformer (T4) in series with the primary of the power transformer. The signal is rectified and

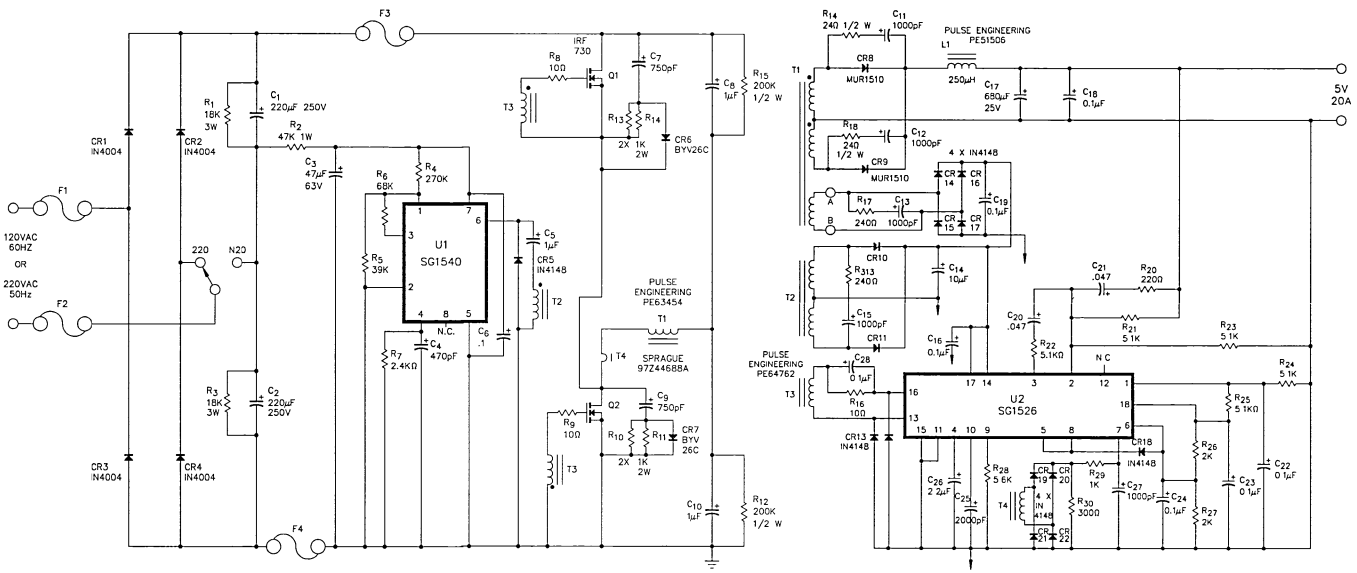

FIGURE 10 – A TYPICAL POWER SUPPLY APPLICATION UTILIZING
THE SG1540 AS THE START–UP CONTROLLER

lightly filtered, then fed to the current limit comparator terminal pin 7 of the SG1526 control chip, where it is being compared to the threshold voltage at pin 6 by R26, R27 divider network.

Start-up Circuit Calculations

Suppose we want our power MOSFETS (Q1, Q2) to start at +15 volts and drop out at +10 volts. This would require the secondary start up and drop out voltages to be 15V and 10V respectively. If the isolation transformer (T2) has a 1:1 turns ratio, then the voltage out of (pin 6)of SG1540 needs to be a squarewave of 0 to 30 volts P-P output, since capacitor C5 blocks the DC component, converting it to a waveform of ±15 volts peak amplitude signal. Knowing this, we proceed with calculations of R1-R3 resistors as follows:

Refer to Figure 5 for this section.

Given V_{START}, V_{DROP}, and that the divider current at start up is 100uA, then the resistor values are calculated as follows:

1. Let $X = \frac{V_{START} - 2.5}{2.5}$

and

$$Y = \frac{V_{DROP} - 2.5}{2.5}$$

Calculate:

$$R_1 = 25 * X$$

$$R_2 = \frac{R_1}{Y}$$

$$R_3 = \frac{R_1 * R_2}{X * R_1 - R_2}$$

Now, based on these formulas we will work out the values of R1-R3 for our converter design:

Given: $V_{START} = 30V$, $V_{DROP} = 20V$

$X = 11.0$

$Y = 7.0$

$R_1 = 275K$ Choose R1 = 274K , 1%

$R_2 = 39.1K$ Choose R2 = 39.2K ,1%

$R_3 = 68.3K$ Choose R3 = 68.1K , 1%

2. Calculation of start up resistor (R_{ST}) and start up capacitor (C_{ST}) are as follows:

$$R_{ST} \le \frac{V_{DCMIN} - V_{START}}{I_{ST}}$$

and

$$P_R = \frac{(V_{DCMAX})^2}{R_{ST}}$$

Calculation of C_{ST}:

$$\frac{I * \Delta T}{\Delta V} < C_{ST} < \frac{T_{ST}}{R_{ST} * Ln\left(\frac{V_{DCMIN}}{V_{DCMIN} - V_{START}}\right)}$$

I_{ST} = total start up current including the resistor divider. ($I_{ST} \ge 1mA$ is a good choice).

I = Total rms current of control circuitry plus 1540 I.C.

ΔT = Discharge time (Time allowed for the auxiliary winding to reach start up voltage).

ΔV = The difference between start-up voltage and drop-out voltage.

T_{ST} = Time to charge up capacitor to start up voltage threshold (power supply start up time).

V_{DC} = Rectified DC BUS at minimum AC input.

A numerical example for our converter design is as follows: First, assume that we have following specs for power supply start up time and power dissipation allowed in the start up resistor.

$T_{ST} \le 700$ ms $\quad P_R \le 1$ watt

Based on the formulas given, we find:

$$R_{ST} \le \frac{(134\sqrt{2})^2}{47 \times 10^3} = 111K$$ Choose $R_{ST} = 47K$

$$P_R = \frac{100\sqrt{2} - 30}{10^{-3}} = 0.764 \text{ watts}$$ Choose 1W Resistor

If $I = 40mA$ and $\Delta T = 5ms$, then $40\mu f < C_{ST} < 62\mu f$

Next, we calculate the start up time of the converter by the formula:

$$T_{ST} = R_{ST}C_{ST}\, Ln\left(\frac{V_{DC}}{V_{DC} - V_{ST}}\right)$$

A tabulation of start up time vs input voltage based on the above equation for the converter is given:

Va	Start up time
100 Vrms	526mS
117 Vrms	442 mS
134 Vrms	381 mS

3. Finally, to complete our start up circuitry, we need to design an isolation transformer. We start by writing the equation:

$$N_P = \frac{V_P}{4\, B_M A_C F_S}$$

Where: V_P = Transformer primary voltage
B_M = Maximum flux density of core material
A_C = Cross sectional area of the core
F_S = Frequency of transformer input voltage

For our design we choose a Ferroxcube Pot Core, 905PL00-3B9 with $A_C = 0.101\ cm^2$. Looking at 3B9 material we choose $B_M = 0.1T$, and we calculate N_P as follows:

$$N_P = \frac{15}{(4)\ (0.1)\ (0.101 \times 10^{-4})\ (200 \times 10^3)} = 19 \text{ Turns}$$

Choose $N_P = 25T$

Note: R7 and C4 are chosen such that oscillator frequency is at 400KHz, therefore providing an output frequency of 200KHz.

Since transformer has a 1:1 turns ratio, both the primary and secondary turns are chosen to be equal. Np = Ns = 25 turns of #32 AWG wire.

Figure 11 shows the start up time at 117Vac input.

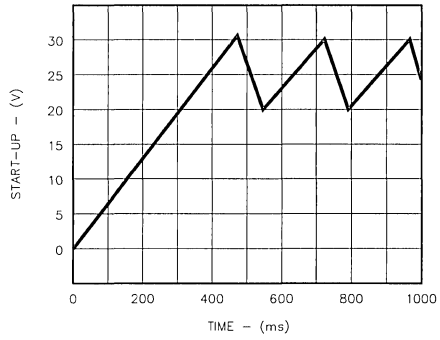

Figure 11. Power Supply Start-up Time v.s. Start-up Voltage

CONCLUSION

Considerable savings in size, weight, and/ or cost can be achieved by using a bootstrap startup circuit in switch-mode power supplies. Empirical evidence has shown that bootstrapping a PWM control IC on the primary side results in a startup current of about 1 milliamp, which means just about any standard PWM control IC can be used as a primary-side controller. Bootstrapping a secondary-side controller results in a significant reduction in the size and weight of the auxiliary power transformer by substituting high-frequency magnetics for the 60-Hz magnetics that would otherwise be required. Moreover, the use of a monolithic startup circuit, such as the SG1540, in a bootstrap circuit minimizes both real estate and component requirements.

PERFORMANCE

A summary of the test results of some of the parameters is tabulated here:

Parameter	Condition	5V Output	Aux output
Line and load regulation	100<Vac<134,5A<I<20A	± 3mV	12V<Vaux<16V
Ripple & noise	100<Vac<134,5A<I<20A	90mV p-p	
Current limit knee	Vac = 100V	22.4A	
	Vac = 134V	23 A	
Short circuit current	Vac = 100V	16A	12.5V
	Vac = 134V	20A	17.6V

Parameter	Condition	Test Result
Efficiency at full load	Vac = 100V	77%
	Vac = 134V	70%
Output load transient	100<Vac<134V	Overshoot = 500mV
		Rcvry time = 300nsec
Start up time	Vac = 100V	520 ms
	Vac = 134V	380 ms

USING THE SG3626/3644 FET DRIVERS IN THE 16-PIN SOIC PACKAGE

Stan Dendinger
Advanced Product Development
Silicon General, Inc.

INTRODUCTION

The use of surface-mount integrated circuits is becoming more popular as the trend to miniaturize electronic systems continues. Consequently, designers are requesting more types of ICs to be available in these packages, particularly the Phillips Small Outline Integrated Circuit (SOIC) configuration. to accomodate this need, Silicon General offers the SG3626 (inverting) and SG3644 (non-inverting) Dual High-speed MOSFET Drivers in the wide body 16-pin copper-lead SOIC package (DW suffix).

This combination of potentially high-dissipation die in a very small package requires special attention on the designer's part to thermal management techniques. The net effect of average IC power dissipation and the resulting heat flow from the die to the outside world should be an operating junction temperature which never rises above +125°C for acceptable device reliability. This application brief is intended to provide enough information for the designer to avoid major pitfalls and to achieve a successful thermal design.

EFFECT OF JUNCTION TEMPERATURE ON RELIABILITY

The undesirable effect of high junction temperatures on long-term reliability of semiconductors has long been known. The Military Handbook, Reliability Prediction of Electronic Equipment (MIL-HDBK-2170) published by the U.S. Defense Department, contains a formula for calculating the Mean-Time-Before-Failure (MTFB). The actual failure rate is dependent on many factors; but assuming all other variables are constant, the relative failure rate will increase with higher junction temperatures.

The curve plotted in Figure 1 is based upon the handbook tables for the temperature acceleration factor of the failure rate model. It can be used to estimate the change in reliability for a given linear bipolar IC as its operating junction temperature increases.

For Example, the SG3626 is rated for a maximum junction temperature of +125°C, and will exhibit a certain failure rate in actual operation dependent on the other factors that influence reliability. If the junction temperature is allowed to go to +150°C, the failure rate will triple. At +175°C, the expected lifetime will be reduced by a factor of 9! On the other hand, if heatsinking lowers the maximum junction temperature from +125°C to +100°C, the reliability will improve by a factor of 3.5. from these numbers, it is easy to see the importance of controlling the junction temperature if reasonable lifetime is a design goal.

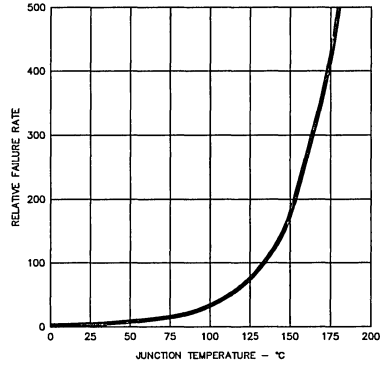

Figure 1. Linear IC Failure Rate vs Junction Temperature (MIL-HDBK 217D)

FREE-AIR OPERATION

Figure 2 shows the maximum allowable power dissipation as a function of ambient temperature for the SG3626DW and 3644DW. Power dissipation capabilities of the 16-pin copper-lead SOIC package (θ_{JA} = 105°C/W) are compared with the popular 8-pin copper-lead-frame plastic DIP (θ_{JA} = 78°C/W).

For free-air operation, the maximum allowable dissipation at T_A = +70°C is 500mW for the SG3626/3644DW. From the data sheet,

sheet, the worst-case DC current consumption is 27mA with both drivers continuously in the LOW state. If no heat sink is used, a maximum supply voltage of 500mW ÷ 27mA, or 18.5 volts should be allowed to keep the junction temperature below +125°C. This is just for safe DC operation.

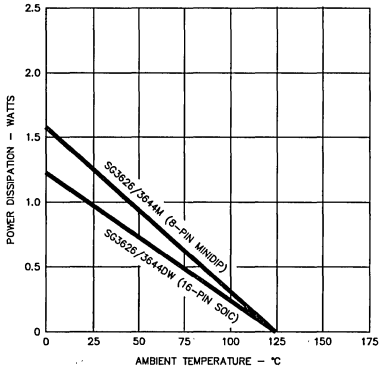

Figure 2. Maximum Power Dissapation vs Ambient Temperature

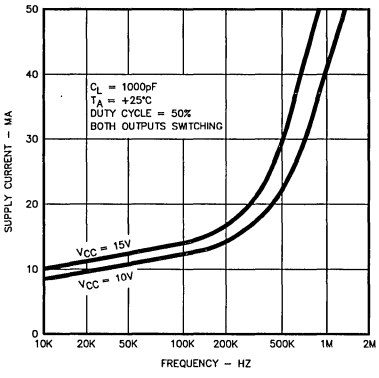

Figure 3. Supply Current vs Switching Frequency

Figures 3 and 4 which are re-printed from the data sheet, can be used to estimate the AC current consumption. The data , taken on actual devices, shows that the current consumption can exceed the worst-case DC value at high frequencies, or with a sufficiently large capacitive load. In the case of a switching power supply, the worst-case dissipation will occur at high line voltage and light load: the driver pulse-width will narrow to a small value, and the power dissipation of the driver will approach the sum of the worst-case DC value plus the AC contribution.

The designer will have to determine the exact power dissipation given the chosen switching frequency and equivalent input capacitance of the power devices; he may conclude that the supply voltage to the driver will have to be reduced even further.

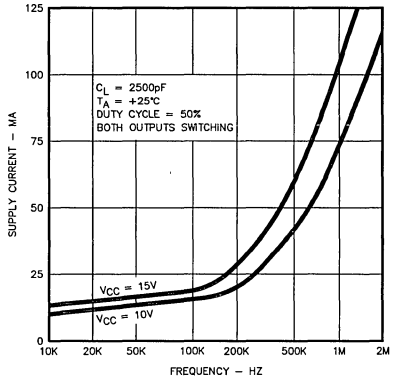

Figure 4. Supply Current vs Switching Frequency

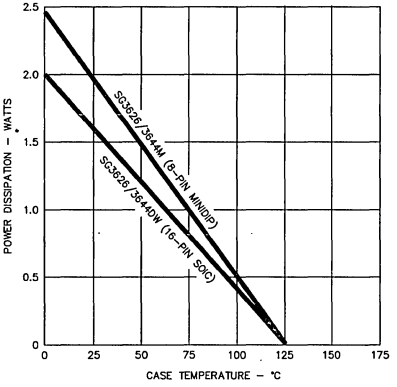

Figure 5. Maximum Power Dissapation vs Case Temperature

OPERATION WITH A HEATSINK

Since most power MOSFETs require gate enhancement voltages of 10 to 15 volts, the idea of heatsinking the SOIC may begin to appear attractive since it offers the beleaguered designer another degree of freedom. From Figure 5, if the case of the SOIC package (the bottom, which is closest to the internal copper die-flag of the lead frame) can be held below +80°C, the driver can dissipate 750mW rather than the previous 500mW. The additional 50% gain in power dissipation capability may be adequate to meet the original design goals.

The thermal resistance is best minimized by designing a wide pc board trace under the SOIC package, and by eliminating the air gap with thermal grease or a high thermal-conductivity rubber gasket with double-sided adhesive. More elegant schemes, such as using a metal-core board of alumina substrate, will allow even higher dissipation. Finally, airflow across the package in the range of 200-800 LFPM will reduce the thermal resistance by 15 to 30%, if the goal of miniaturization is not compromised by the addition of a fan.

POWER SWITCH DRIVERS: NEW IC INTERFACE BUILDING BLOCKS FOR SWITCHED-MODE CONVERTERS

Stan Dendinger
Manager, Advanced Product Development
Silicon General, Inc.

ABSTRACT

This paper describes the characteristics and performance of two new integrated circuit products designed to interface between the control circuitry for switch mode converters and their high power output stages. The first device develops the high level turn-on and turn-off commands directly from the outputs of a low power P.W.M. control circuit while the second is designed as a floating switch to control a high current switching transistor directly from the secondary of a drive transformer.

INTRODUCTION

Recent years have seen significant developments by component suppliers which have resulted in the ready availability of many high performance power transistors and sophisticated control integrated circuits for switching power supply design. There existed a gap, however, between the control circuit and the power switching transistors where a considerable amount of circuitry was required to adequately condition and amplify the control signal in such a way as to provide the proper turn-on and turn-off commands to the power switch. This gap has now been filled with two new integrated power switch drivers, the SG1627 Dual Output Driver and the SG1629 High Current Floating Switch Driver.

SG1627 DUAL OUTPUT DRIVER

The SG1627 was designed to directly interface between low level control circuitry and the high current handling devices required in switching power supplies. As shown in Figure 1, this is a dual circuit containing both channels that are required for a push-pull system. It accepts the P.W.M. signals from a control circuit such as the SG1524 and provides the conditioning necessary to develop both turn-on and turn-off commands at currents up to 500mA. Its outputs can be used to directly control an external power transistor or to interface with driver transformers for additional power amplification. Another feature of this circuit is the optional ability to provide a constant drive current.

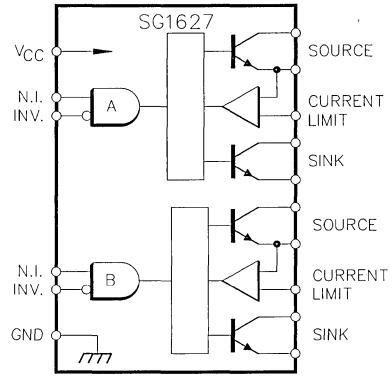

Figure 1. The SG1627 Dual Output Driver is Packaged in a 16-Pin Cerdip D.I.L. Package.

CIRCUIT DESCRIPTION

Figure 2 shows the schematic for one-half of an SG1627 dual output driver. It must be remembered that there are two identical circuits in each 16-pin dual-in-line package. The inputs to this circuit are switch closures to ground with both inverting and non-inverting logic configurations available. The input threshold level

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of both logic inputs is 2V, and the logic is powered by an internal voltage regulator so that input characteristics are unaffected by power supply voltage which can range from 5 to 30 volts.

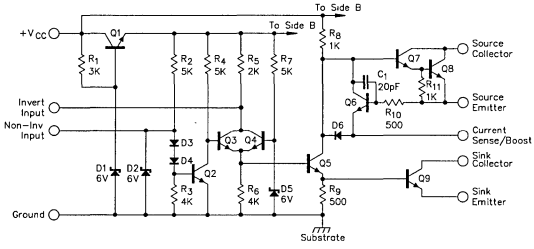

Figure 2. Schematic Diagram for One-Half of the SG1627

The output sections of the SG1627 contain both source and sink transistors, each capable of 500mA, 30V operation. In addition, the source transistor has the capability of constant current operation by using an external sense resistor between the source emitter and the current sense terminals. The source transistor is in a Darlington configuration which can easily deliver currents to 500mA under all operating conditions but at the cost, however, of a higher saturation voltage. The sink transistor is designed for very low saturation voltage: approximately 0.5 volts at 500mA. It does, however, need greater base drive to meet those high currents. This can be provided by either raising the supply voltage above 5V, or by adding a boost drive current through D6. The saturation characteristics of both source and sink are shown in Figures 3 and 4.

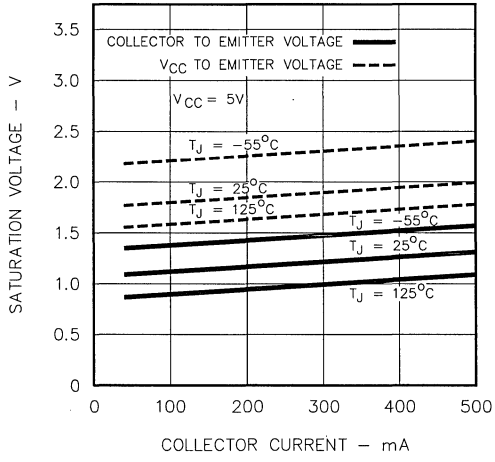

Figure 3. Saturation Characteristics of the SG1627 Source Transistor

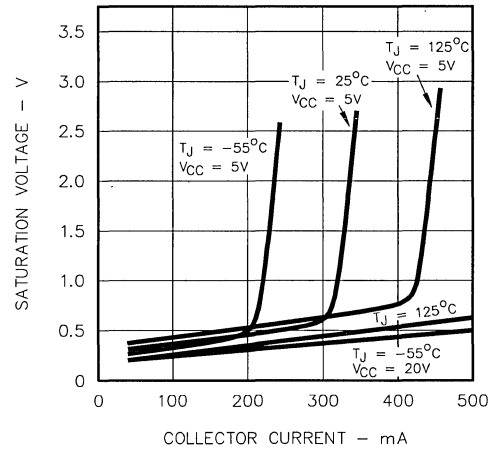

Figure 4. Saturation Characteristics of the SG1627 Sink Transistor

THE TOTEM-POLE OUTPUT CONFIGURATION

One of the simplest uses of the SG1627 is illustrated in Figure 5 where the output is configured to provide a constant 300mA turn-on command to an external switching transistor together with a high peak turn-off current. Note that the logic on the SG1627 is being driven directly from the 5V reference terminal of an SG1524 P.W.M. control I.C. The logic inputs are directly connected to the open collector output transistors of the SG1524 with no additional interfacing components. The output current of the SG1627 comes from the input voltage, which in this case is approximately 10V, but the use of R_2 provides a constant source drive regardless of input voltage variations.

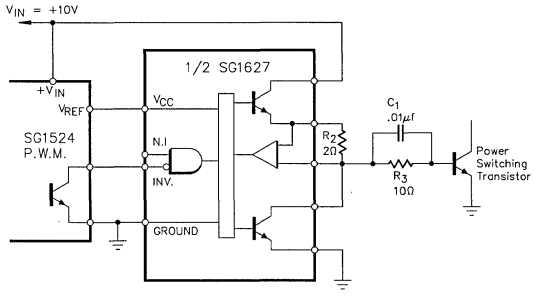

Figure 5. In a 300mA Output "Totem Pole" Configuration, The SG1627 Interfaces Directly With the SG1524 Regulating P.W.M. Control Circuit.

Resistor R_3 is used to build up a voltage drop across capacitor C_1. At turn-off, the energy stored in C_1 provides both a negative voltage to the base of the power switching transistor and the boost

drive current necessary to saturate the sink transistor during peak discharge currents of approximately 500mA. With this magnitude of reverse base current (Ib2), transistor turn-off is greatly accelerated.

There are two considerations to remember in this configuration. The first is that the maximum output voltage will be less than the value of V_{CC} because the source transistor operates as an emitter follower. With V_{CC} = 5 volts in this case, the peak output voltage is approximately 3 volts. The other consideration is power dissipation in the source transistor when using it in the constant current mode since it will absorb any excess voltage after current limiting.

The performance of this application is illustrated in Figure 6 which shows the base current into the external switching transistor. One can see both the constant drive current of about 300mA and the rapid, peak negative turn-off current in excess of 500mA. Note that the delays through the SG1627 are less than 50 nanoseconds making a very fast responding circuit.

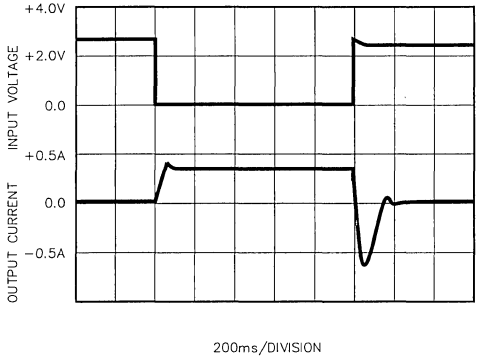

Figure 6. Output Current Transfer Function

An alternate configuration shown in Figure 7 pictures the SG1627 with a higher value of supply voltage. This offers at least two advantages: first of all, it allows the output voltage swing to rise considerably higher remembering that the source as an emitter follower can rise to approximately 2V below the input supply voltage. The other benefit is in providing greater drive current for the sink transistor allowing 500mA saturation without the need for additional boost current. Because of the large power supply voltage across the source transistor, power dissipation can be a problem. This probably means a reduced source current if current limiting is required, although the use of resistor R_1 to absorb some of the voltage drop will reduce the power dissipation within the SG1627.

Recognizing the potential for package power limitations, it is important to consider the use of the SG1627 with various types of

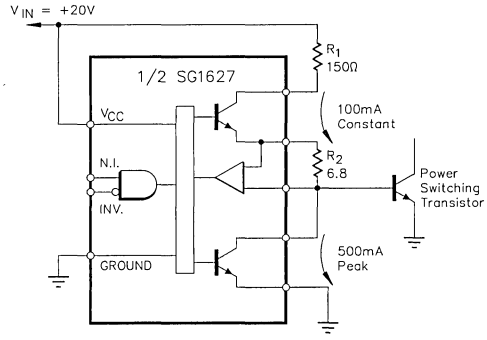

Figure 7. Higher Input Voltages Can be Used to Provide Drive for Higher Sink-Transistor Currents

power boosting circuitry. Maximum flexibility for the use of external current boosting transistors is maintained by the uncommitted availability of both the collector and emitter terminals of both the source and sink transistors. Figure 8, for example, shows the use of an external PNP transistor to boost the source current to 1amp. The use of the PNP transistor in this configuration still allows current sensing to be used for constant current operation. If constant current operation is not required, an NPN emitter follower booster could also be used. The use of a single boost transistor as shown in Figure 8 makes a powerful drive circuit as one can now drive one amp of turn-on current into a switching power transistor and still have a 500mA of turn-off current through the sink transistor.

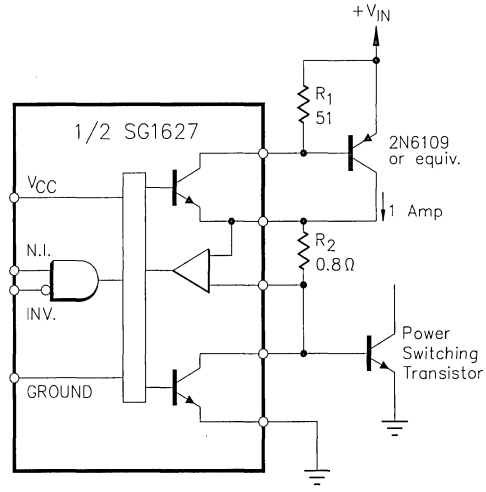

Figure 8.Increased Source Current With the Use of an External Boost Transistor

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DUAL PHASE OUTPUTS

The SG1627 does not need to be committed to totem pole operation. The source and sink transistors can be separated and used independently for dual opposite-phase outputs. Figure 9 shows the operation with both source and sink transistor emitters grounded and each used as a common emitter amplifier driving an external load resistor. Figure 9 also shows the use of an external resistor R_1 to provide additional drive current boost to the sink transistor. This will allow the sink transistor to provide full 500mA operation with only a 5 volt supply. The response characteristics of this type of configuration are shown in Figure 10, which pictures the response of both source and sink with 24ohm load resistors to inputs at both the inverting and the non-inverting logic inputs. Note again the minimum delay of both outputs; less than 100 nanoseconds from input to output on both source and sink.

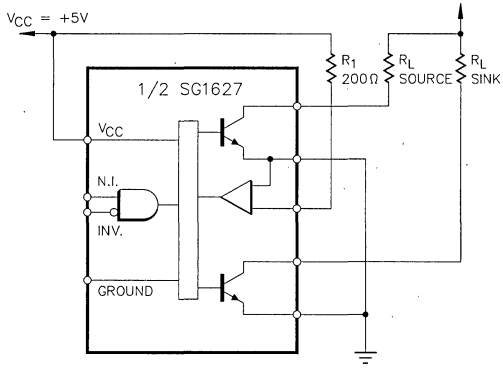

Figure 9. Seperate Dual-Phase Outputs With Additional Drive Current for 500mA Sink Transistor Operation

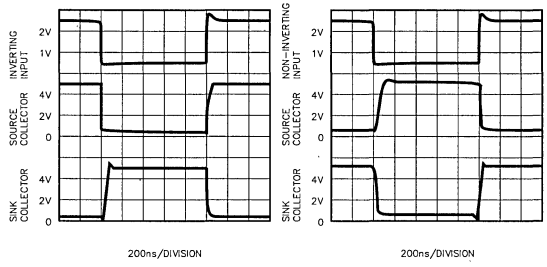

Figure 10. Source and Sink Response Characteristics

The use of the source and sink as separate outputs provides significant benefit for driving a transformer, as illustrated in Figure 11. In this example, the primary winding of the transformer is driven by the source transistor with its emitter grounded. Constant current operation is shown with the inclusion of the sense resistor, R_2, but voltage switching could as easily be accomplished by merely shorting together the sense terminals. To provide greater efficiency in the magnetic design, a reset winding is added and shown being driven by the sink transistor. This ensures the magnetic flux is reset to zero between each pulse. Of course, the sink transistor opens up every time the source transistor drives the primary winding.

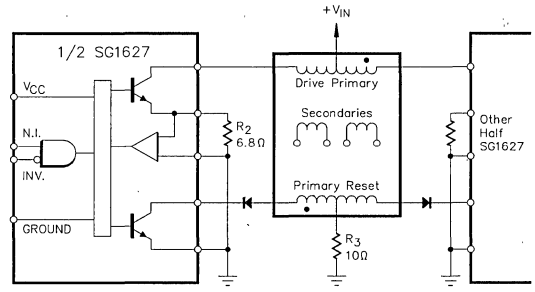

Figure 11. Driving an Outside Transformer With the SG1627

An additional illustration of the versatility of the SG1627 is shown in Figure 12, where the non-inverting logic input is used to provide a positive guarantee that both sides of a push-pull inverter can be on at the same time. This circuit is shown using the inverting input as the primary drive path, which will force the source transistor to be on when the control circuit transistor is conducting. The non-inverting input is then diode-coupled to the opposite side of the inverter and senses saturation of the external power switch. If the collector of the opposite transistor is low, holding the non-inverting input low, then regardless of what happens at the inverting input terminal, the output source on that side cannot be turned on. The sink will remain on, holding the output low until a rising collector voltage on the opposite side removes the non-inverting input at which time the command signal will then come through the

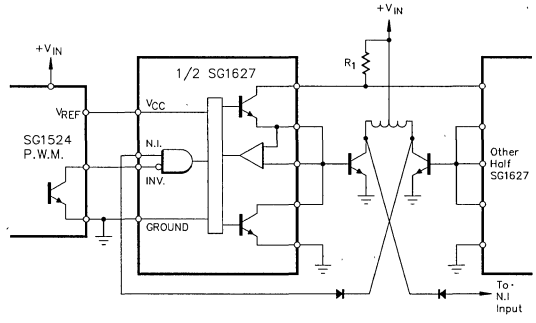

Figure 12. Simultaneus Conduction of the Two Output Transistors is Prevented by Gating With the Non-Inverting Inputs

SG1627 and turn on the correct side. This circuit is particularly useful as a protection against cross-conduction of the output transistors during transient conditions at power-on or overload.

The above examples have been chosen to illustrate the versatility and performance of this new device designed to interface between a low level pulse width modulating control circuit and the high power switching transistors used in all modern-day switching power supply designs.

THE SG1629 HIGH CURRENT FLOATING SWITCH DRIVER

A second interface circuit to be discussed in this paper is the SG1629 illustrated in Figure 13. This device has been designed to provide an interface between a drive transformer secondary winding and a high power switching transistor, and again provide the proper signal conditioning to adequately deliver both turn-on and turn-off current into the base of that switching transistor. More importantly, its design is such that it requires no external power connection but develops all the power for both turn-on and turn-off from the drive transformer and an external storage capacitor. With this capability, the SG1629 can be used in floating operation for bridge inverters at voltages in excess of 300V with respect to ground. This circuit also contains the capability for constant current drive operation with a similar type of current sensing circuit and an external current sensing resistor.

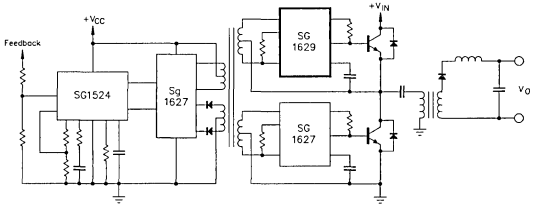

Figure 13. The SG1629 High-Current, Floating Switch Driver

CIRCUIT OPERATION

The SG1629 functions with a center-tapped drive transformer secondary winding such that when a turn-on command is present and current is flowing in the upper half of the secondary winding through the source transistor and into the base of the power switching transistor, a current is also flowing in the lower portion of the transformer secondary through the high current rectifier to charge the external capacitor C_S to a negative voltage. When the drive command terminates, this negative voltage is used to turn on the sink transistor which then pulls a negative Ib2 current from the base of the switching power transistor down to the negative voltage on the capacitor providing again a high peak turn-off current to speed the response and minimize the power losses in the switching transistor. For maximum versatility, this circuit also contains several gating options.

In Figure 14, the schematic of the SG1629 shows two power Darlington transistor structures, each capable of handling an excess of 2amps of current: Q3/Q4 as the source. and Q6/Q7 forming the sink. Transistor Q5 provides current sensing with feedback to provide constant current operation. The source transistor is turned on by conduction of drive current through resistor R_2. The drive current for the source transistor is gated on and off through the action of Q1 which senses the input voltage and provide a turn-off of the source transistor between each drive current pulse.

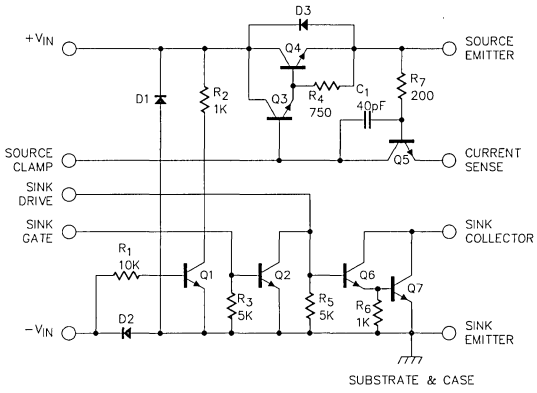

Figure 14. The Schematic of the SG1629. Transistors Q4 and Q7 are Designed for Two-Amp Operation.

The Darlington sink transistor has its input brought out as a separate sink drive terminal which gives the user several driving options. In addition, the sink driving current can be gated by the use of Q2, which has its own input terminal. The diodes D1 and D2 are high current rectifiers which provide the charging current for the external capacitor attached to the sink emitter terminal. The action of transistor Q1 to gate the source transistor insures that there is negligible discharge current (less than 10mA) from the external capacitor during the off periods of the circuit. This allows the capacitor to be charged with very narrow drive pulses separated by relatively long off periods.

The SG1629 is packaged in both a multi-pin TO-66 power package and an 8-pin minidip. Having no sensitive, low current circuitry, this device can be operated with a maximum junction temperature of 175°C which, coupled with a low θ_JC thermal resistance of 5°C/W, gives the TO-66 package a 3 Watt capability in free air and 10 Watts or more with some heat sinking. Because of the versatility of this device, it was felt that there may be applications for lower power requirements and thus the SG1629 will also be available in an 8-pin ceramic minidip package which, of course, has a power dissipation of only 800mW. With one pin less in the 8-pin minidip package, the sink gate function is sacrificed.

SG1629 APPLICATIONS

The use of the SG1629 can best be demonstrated in an application as shown in Figure 15 where two SG1629's are used to provide the drive signals for the power transistors in a 5 amp one-half bridge switching supply. The drive transformer is shown with 10 volt drive signals on the primary winding which, with a 2:1 transformer turns ratio, provides a 5V peak signal on each half of the secondary. When the drive command is present on one secondary, it is translated into a constant current through the source transistor by the use of the sense resistor, R_{CS}, which in this case provides a constant 700mA into the base of the external NPN transistor. At the same time, the 20 microfarad external capacitor is being charged with a current through the rectifier in the SG1629 and the lower half of the secondary winding. While this is occurring, the opposite phase signal is being applied to the lower SG1629 circuit which serves to further enhance the charge on its external capacitor while maintaining the power switch in the off state.

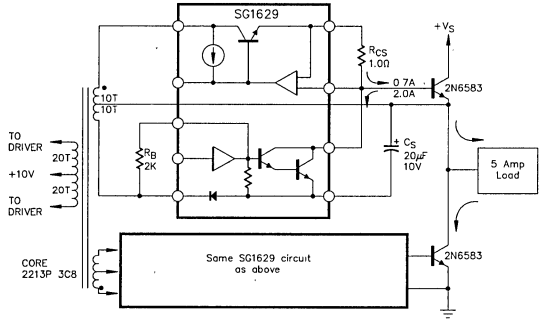

Figure 15. Use of the SG1629 in a 5-Amp Half-Bridge Converter

When the drive command terminates, the voltage at both ends of the secondary winding goes to zero. Since there is approximately -4V at the emitter of the sink transistor while its base is being driven through the external drive resistor, R_B, to zero volts, the sink transistor then immediately turns on and pulls a high current I_B2 pulse out of the external transistor and through the capacitor. This current, of course, only flows as long as it is available from the stored charge within the base of the external transistor as the source has been gated off. After that charge is depleted, the sink transistor remains on insuring a negative reverse voltage at the base of the switch transistor.

The performance of the SG1629 can be illustrated by the waveform photographs in Figures 16 through 18. In figure 16, the command signal from one channel of the control circuitry and the waveform of the drive transformer primary voltage are shown. The voltage on the secondary winding, referenced to the center-tap and the power transistor emitter, is pictured in Figure 17. Also shown in this photograph is the input voltage at the base of the external NPN transistor. Note that at the very first portion of this waveform, when the opposite side is on, there is an additional negative charge supplied to the capacitor so that we have a maximum reverse base-to-emitter voltage of close to -4V. During the off time, the action of the sink transistor maintains a negative voltage bias of approximately -3V on the base of the power transistor. When the drive command is given to turn on, the base voltage goes positive to the 0.7 or so volts necessary to turn it on and at turn-off, goes negative again. The important action is shown in Figure 18 which pictures the actual base current of the power transistor with a scale of one amp per division. Both the constant turn-on I_B1 of about 3/4 amp and the peak I_B2 of close to -2amps can be seen along with the collector voltage waveform with a 5amp resistive load. Remembering that the time base of all these waveform photographs is 5 microseconds per division, one can see approximately one microsecond delay between the turn-off signal at the base and the actual turn-off of the collector of the output transistor. Although this turn-off response is primarily a function of the transistor design, it is safe to say that any power switching transistor should perform faster with this form of base drive.

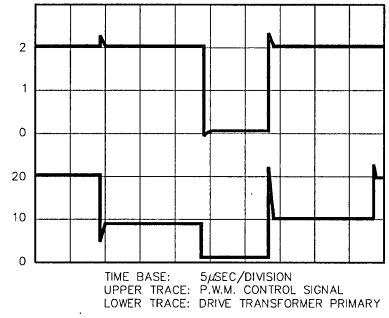

Figure 16. Input Control to the Drive Transformer

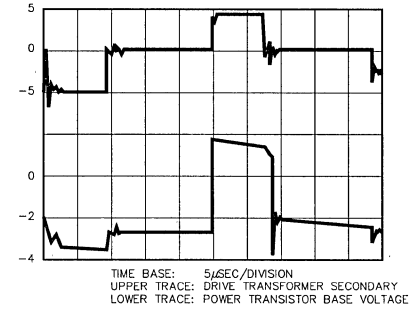

Figure 17. The Base Voltage Delivered to the External Power Switching Transistor by the SG1629

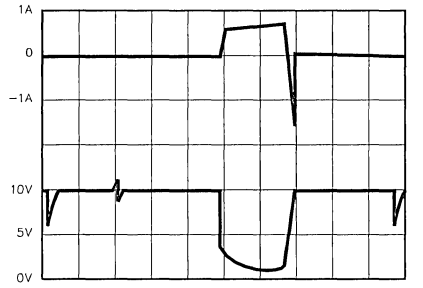

Figure 18. Base Current and Collector Voltage of the External Switching Transistor

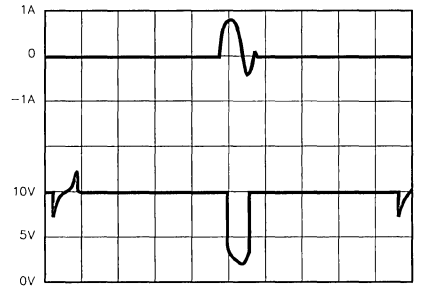

Figure 19. Operation With Narrow Pulse Widths

Note that one can also see in the collector waveform a soft knee at turn-on where the power transistor is not saturated instantaneously. This is partially because of the turn-on characteristics of the transistor and partially because of the finite rise time of the base current through the driving circuitry. The rise time is primarily a function of the leakage inductance of the drive transformer which opposes a sudden change in current from zero to maximum value. It is an exercise in transformer design to configure the transformer to minimize to the greatest extent possible the leakage inductance. This can be done with a minimum number of turns and a maximum coupling between turns. In the illustration, a ferrite pot core of approximately 3/4" in diameter was used to configure the drive transformer. More will be said about turn-on rise time later, but first let's discuss one additional characteristic of concern in the turn-off circuitry: The operation with very narrow pulse command.

Since the charge on the external capacitor is developed during the turn-on command, narrow pulse widths accomplish the transfer of a minimum amount of energy. As the drive command pulse widths get narrower, there is a point where the voltage on the external capacitor begins to fall off. With the circuit components as shown earlier, this loss of I_B2 occurs at approximately 2 miscrosecond pulse widths. Figure 19 shows the base current and collector voltage waveforms at narrow pulse widths where the I_B2 has diminished from 2amps down to approximately 3/4 of an amp. Further reductions in pulse width bring the I_B2 current ultimately to zero. This characteristic is, of course, a function of the time constants in the total circuit and some compromise or optimization can be achieved by appropriate selection of capacitor values and secondary drive voltages.

The above circuit incorporated constant current drive which is an advantage if the load current happens to be relatively constant but in many applications this is not the case. The SG1629 may also be used to provide a base drive proportional to load demand by adding an anti-saturation clamp diode as shown in Figure 20. With the current sense terminals shorted, there are two V_{BE} voltage drops between the clamp and the source emitter terminals. Therefore, the clamp diode D1 will hold the collector on voltage to approximately one diode drop above the base. This will keep the switching transistor right at the threshold of saturation, regardless of load current variations.

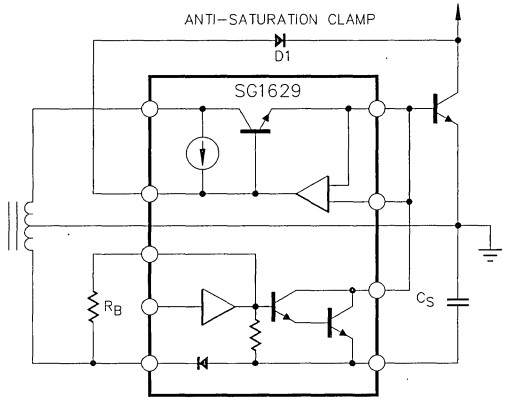

Figure 20. Use of the SG1629 in a Load-Dependent Drive Configuration

IMPROVING TURN-ON RESPONSE

In applications where maximizing base current rise time is important and secondary transformer inductance is a significant consideration, the use of the gating functions in the SG1629 can provide significant benefits. Figure 21 shows the addition of an external transistor Q1 to drive the sink transistor's gate circuit. To explain

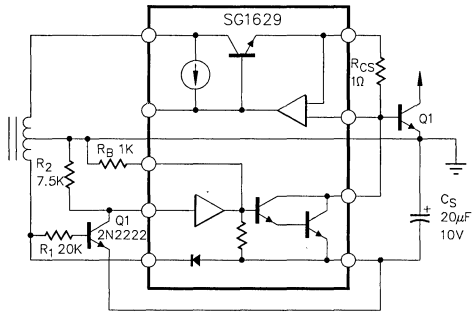

Figure 21. Improving Base Current Turn-On Rise Time

the operation of this circuit, note that the sink transistor's base drive is now being generated with R_B connected to the common or center tap of the drive transformer secondary instead of the negative input terminal. This is essentially zero volts and since the emitter of the sink transistor is attached to the capacitor which has a negative voltage on it, the sink transistor would normally be on continuously. Transistor Q1 is selected as a relatively slow non-gold-doped transistor which has a finite storage time. Its action is to turn the sink transistor off during the drive command signals, but to delay that off signal for some increment in time. Note that before the commencement of a drive command, the sink transistor is on by the action of R_B. Transistor Q1 is also saturated by its base resistor being connected to the end of the transformer which is also at zero volts prior to the command signal.

When the drive command is initiated, current begins to build up in the secondary circuit and the first flow of current is through the source transistor, through the current limiting resistor, down through the sink transistor which is still conducting, and back to the negative terminal on the transformer secondary. The switching transistor is still back-biased while this occurs. Because the input to transistor Q1 is now at a negative voltage, it turns off, but since it has a finite storage time, that time is used to delay the rise of the input to the sink gate. Additional delay can be added with a small capacitor at the sink gate input terminal. When the input to the sink gate goes high, its output goes low, forcing the sink transistor to turn off. Since the source current is already flowing, turn-off of the sink diverts that current to the base of the output transistor producing base currents in Q1 with rise times of less than 100 nanoseconds.

When the action is reversed at turn-off, there is negligible increase in delay time between the turn-off signal and the actual turn on of the sink transistor. This is because Q1 is the only device with a long storage time and it is turning on so storage is not a factor.

Another method of spreading up the rise time of current into the base is the use of some reactive components to differentiate the drive current signal. A simple approach is a capacitor by-pass around the current sense resistor, R_{SC}, providing an initial boost in turn-on current.

GETTING IT ALL TOGETHER

The overall simplifications which Silicon General has offered to the design of switch mode power converters can best be illustrated by Figure 22 which shows the total command signal flow from the feedback error information to the output of a high current half-bridge regulating inverter. The SG1524 was designed to provide all of a switching regulator's P.W.M. control signals with the only external components required being the divider resistors to interface with the error amplifier, the overall loop compensation network, and the resistor and capacitor to set the operating frequency. The SG1524 drives the SG1627 directly which, in turn, provides the signal conditioning to develop the drive and reset commands to an interstage drive transformer. The secondary windings of that drive transformer are directly coupled into a pair of SG1629 floating drivers which are then used to command the external 5amp switching transistors which form the high power output stage of the power supply.

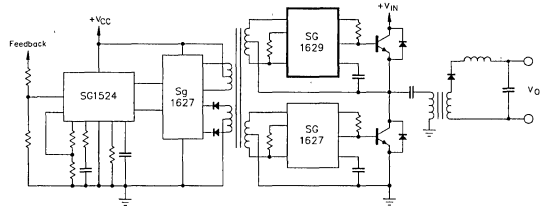

Figure 22. Three IC Types Form a Major Portion of the Control Electronics for a Switch-Mode Half-Bridge Converter.

These circuits have all been designed to offer a maximum degree of flexibility while incorporating what would otherwise be a substantial amount of discrete circuitry.

Thus, all these new IC's greatly ease the design and manufacturing problems typically inherent in switching power supplies and, at the same time, provide greater repeatability and reliability at significantly reduced costs.

USE MOTOR-DRIVE IC TO SOLVE TRICKY DESIGN PROBLEMS

An IC Driver's Logic-Control Features and High Output Capability Suggest Elegant Ways to Handle a Variety of Dificult-to-Drive Loads

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INTRODUCTION

You can use the SG3635 driver IC in a wide range of applications, ranging from a switched-mode motor-speed controller to a data-communications line driver. The device's input configuration simplifies interfacing between low-level circuitry (eg, a μP or logic blocks) and the high-power load. And its output stage (see "Anatomy of a driver IC), capable of driving 40V, 2A loads with peaks as high as 5A (including reactive loads), provides sinking and sourcing capability as well as commutation diodes.

CONTROL MOTOR SPEED WITH MINIMUM PARTS COUNT

Fig 1 shows one application of the device in a self-clocking switched-mode speed-control loop. The mechanically coupled tachometer detects the motor's speed; its output, scaled and filtered by the RC network, drives the 311 comparator, which compares the output with the speed-setting input and biases the SG3635 to complete the loop.

When the motor slows down, the SG3635's output switches on (**Fig 2,** trace A), forcing current into the motor (trace B) until the comparator's inputs balance. Under these conditions, the circuit oscillates in a controlled manner around setpoint. The 10-kΩ, 0.1-μF pair provides positive ac feedback to ensure clean transitions.

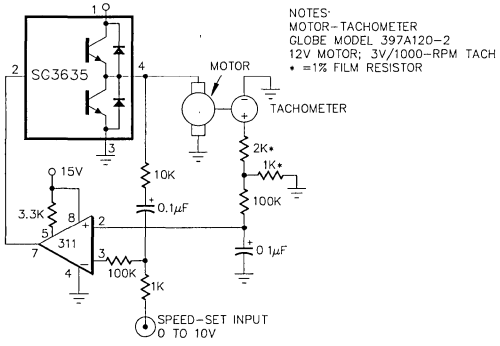

Figure 1. Used in a Closed-Loop Configuration, the SG3635 Self-Clocking Driver IC Controls Motor Speed in Proportion to 0 to 10 V Input. The Comparator Weighs the Tachometer's Output Against the Input Setting, Then Commands the SG3635 to Either Speed up or Slow Down the Motor

TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	5mSEC/DIV
B	0.5V/DIV	5mSEC/DIV

Figure 2. Switching on in Discrete Increments (trace A), Fig 1's Driver IC Forces Current (traces B) into the Motor to Speed it up. Upon Reaching Equilibrium, the Circuit Oscillates Around the Setpoint

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The 3.3-kΩ resistor from the comparator's offset pin to the 15V supply provides enough offset to prevent motor turn-on with a 0V speed setting. In this application the driver only sources current: The sink transistor is never enabled. You could turn the sink device on to dynamically brake the motor, but the motor's back EMF would cause considerable power dissipation. The back EMF appears after the initial inductive spike (clamped by the internal commutation diode), which appears when the IC's output switches LOW.

IC's HIGH-CURRENT OUTPUT YIELDS FAST MOTOR REVERSAL

What about motor-reversing capability? **Fig 3**'s single-supply circuit uses two SG3635s in a bridge configuration. The flip flop generates the necessary complementary instructions to the ICs' Enable inputs. In this example, the SG3635s' Pulse inputs are grounded; you could instead pulse-width modulate them to control motor speed.

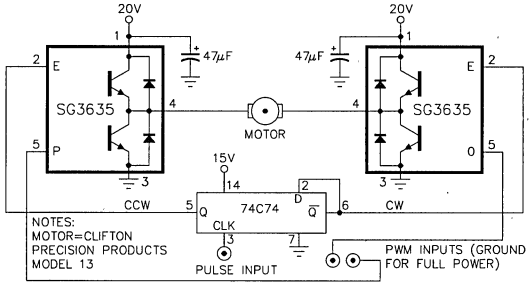


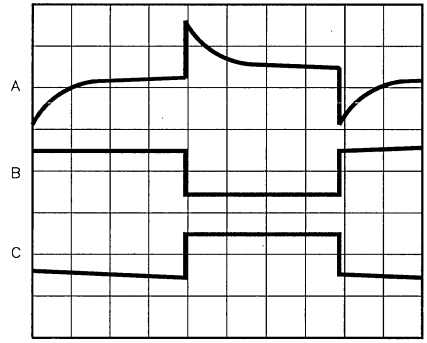
Figure 3. This Push/Pull Bridge Configuration Allows Two Driver IC's to Provide Bidirectional Motor Drive. A Command to the Flip Flop's Clock Input Causes Instantaneous Reversal. Ground the SG3635's Pulse Inputs for Full Speed; Apply a Pulse-Width-Modulated Input to Control the Speed

Fig 3's circuit is a good test of the IC's peak current capabilities, because motors present a very difficult load during instantaneous reversal. **Fig 4,** trace A shows the current; traces B and C represent the SG3635's voltage outputs. The motor draws 200mA during a reversal because of the armature's stored energy.

Servoed motor makes position clear

In addition to controlling speed and direction, you can use the SG3635 in a simple circuit to control a shaft's position (**Fig 5**). In this configuration, the motor drives a mechanical scanner in either direction between a set of programmed limits. The driver IC's ground pin is biased at -15V, allowing the device's output to swing symmetrically about 0V.

The 5-kΩ pickoff potentiometer detects the scanner's position, then trips a pair of limit comparators; these comparators in turn



TRACE	VERTICAL	HORIZONTAL
A	2A/DIV	50 mSEC/DIV
B	20V/DIV	50 mSEC/DIV
C	20V/DIV	50 mSEC/DIV

Figure 4. Large Peak-Reversal Current in Fig 3's Motor is Evident in Trace A. Traces B and C Showthe Drivers' Output Reversal; the Outputs Handle the 3A Motor Peaks Cleanly

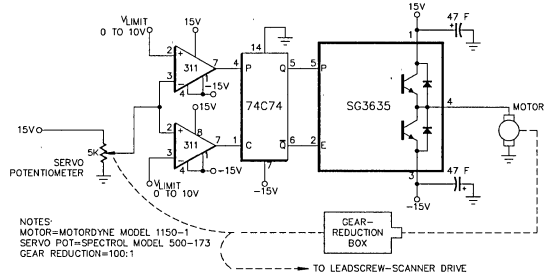


Figure 5. Control a Shaft's Angular with This Servo-Loop Circuit. Select the Position by Applying Limits to the Comparator Inputs. The Circuit Uses Supplies Shifted 15V Negative to Provide a Ground-Level Bipolar Output to the Motor

bias the RS flip flop that controls the SG3635. To provide logic level compatibility with the driver, the flip flop uses 0V and -15V supplies instead of the usual +15V and 0V configuration. This circuit forces the scanner to run continuously between the limits defined by the V_{LIMIT} inputs. You could control speed by summing pulse-width modulated signals at the comparator inputs or by gating the SG3635's inputs.

DRIVE LONG CABLES WITH TOTAL DATA RECOVERY

You can also use the driver IC in applications other then motor control. Consider, for example, the problem of driving long cables at high data rates - a difficult task because of the rapid buildup of parasitic capacitance with increasing cable length. In a remote data-monitoring application, for instance, a 10,000-ft cable displays 0.1-μF capacitance - a brutal load at high speed, making receiver-end data recovery difficult.

Fig 6's circuit provides the drive for this difficult load: the V/F converter presents a serial, 100-kHz square-wave data format to the SG3635. The driver's output (**Fig 7,** trace A) - somewhat distorted because of the load - drives the line. Trace B shows the IC's output current: The 5A peaks at the waveforms's edges clearly reflect the heavy capacitance.

The square wave's distortion is relatively minor, allowing easy data recovery. The 311 comparator uses a simple RC network to set an adaptive amplitude threshold against which to compare the line output. Because the threshold is derived from the signal, power-supply shifts produce no undesirable effects.

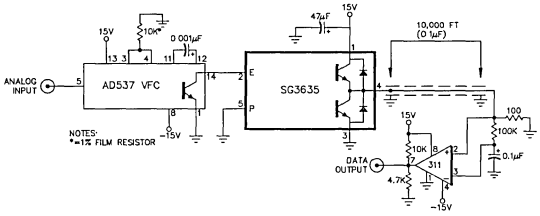
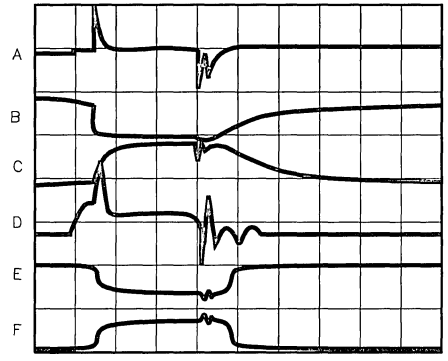


Figure 6. Driving a Brutal Capacitive Load Presents Little Problem to the SG3635 Driver. In This Circuit, the IC Drives a 10,000 ft Data-Communications Cable Having 0.1μF Capacitance. The Driver Transmits Serial 100-kHz Data to the Recieving Comparator.



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	500 nSEC/DIV
B	200V/DIV	500 nSEC/DIV
C	3A/DIV	500 nSEC/DIV
D	5V/DIV	500 nSEC/DIV
E	200V/DIV	500 nSEC/DIV
F	3A/DIV	500 nSEC/DIV

Figure 7. The Effects of Fig 6's Gluttonous Capacitive Load are Evident in Traces A and B. The 10,000 ft. Line Absorbs 5A Current Peaks During the IC's Switching Transitions. The Recieving-End Comparator Uses an Adaptive Amplitude Threshold to Produce a Clean Output.

VALVE-CONTROL CIRCUIT MAINTAINS CONSTANT pH

In another nonmotor-related application, you can use the SG3635 in conjunction with a pH probe as a 3-mode controller (**Fig 8**). The FET op amp unloads the probe and routes the signal - via an RC filter - to the two comparators. The comparators, configured as a double-ended limit detector, bias the SG3635; the IC then drives valves that fed either acidic or basic solutions to the chemical vessel.

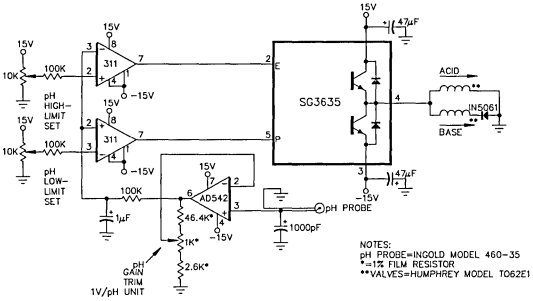


Figure 8. Regulate a Chemical Solution's Acidity with this 3-mode Controller Circuit. The SG3635 Drives the Valves that add Either Acidic or Basic Solution to the Bath. Set the Desired pH with Potentiometer-Determined Comparator Limits.

If pH is correct, both comparator's outputs remain HIGH and neither valve energizes: The appropriate LOW-switching comparator redresses eventual pH imbalance by turning the necessary valve on.

In a final example of the driver IC's versatility, consider its use as a high power-transistor driver. Driving these devices at high speed requires active turn-off techniques to sweep charges from the base-emitter junction. Moreover, many high-voltage power transistors need negative base bias to guarantee breakdown ratings.

Assume, for example, the use of unipolar base drive **(Fig 9a)** for a high-power 2N6308. **Fig 10,** trace A shows the transistor's base waveform; traces B and C display collector voltage and current, respectively. Because the base drive is unipolar, the collector turns off slowly: Voltage and current require about 1.5μsec to settle. What's more, the transistor dissipates considerable power during turnoff, increasing its vulnerability to secondary breakdown. Inductive loads (eg, flyback transformers) can exacerbate the situation.

The solution? **Fig 9b**'s circuit uses an SG3635 to provide bipolar base drive, thereby shortening turn-off time. The 311 comparator shifts the TLL-command level to bias the driver's Enable input; shifting is necessary because the SG3635's ground pin is returned to -15V. The 25Ω resistor to ground limits the transistor's reverse bias. Traces D, E and F show the 2N6308's base voltage

and collector voltage and current, respectively - you can see that collector turn-off time decreases to 200nsec, greatly reducing the likelihood of secondary breakdown.

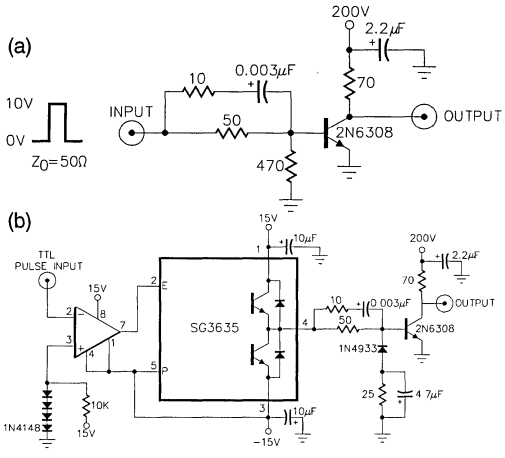
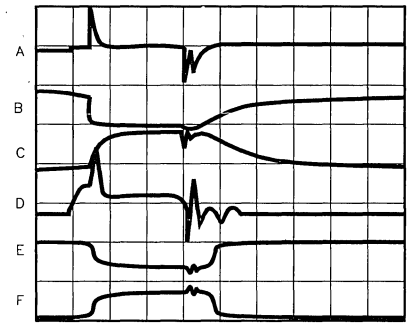


Figure 9. Using Unipolar Base Drive **(a)** for a High-Power Transistor can Result in Slow Collector Turn-Off. A Bipolar-Drive Circuit **(b)** Shortens Turn-Off Time Considerably by Sweeping out Base-Emitter Change. Moreover, the Negative Base Bias Improves the Transistor's Breakdown Characteristics



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	500 nSEC/DIV
B	200V/DIV	500 nSEC/DIV
C	3A/DIV	500 nSEC/DIV
D	5V/DIV	500 nSEC/DIV
E	200V/DIV	500 nSEC/DIV
F	3A/DIV	500 nSEC/DIV

Figure 10. Dramatic Turn-Off-Time Differences Between Unipolar- and Bipolar-Base-Drive Circuits (**Figs 9a** and **9b**) are Evident in This Photo. Long Collector-Voltage (trace B) and -Current (trace C) ON-to-OFF Transitions Result From the Unipolar Drive (trace A); the Bipolar Drive (trace D) Increases Turn-Off Speed More Than Sevenfold.

ANATOMY OF A DRIVER IC

Figure 11**(a)** shows the SG3635 driver IC's internal organization. The main consideration in the IC's design is to make logic-level/power-load interfacing as straightforward as possible. The logic-compatible Enable and Pulse inputs operate according to the truth table shown: Accepting drive from 74C Series circuits operating at 10V or more, they're compatible with all TLL forms except 54L. You can allow the inputs to float to the HIGH state, but you must force them to ground to produce ZERO.

Negative supply voltages are permissible at the ground pin, but you must restrict the chip's total rail-to-rail voltage to 40V. The internal regulator stabilizes the IC against supply variations; the level-shift and interlock features provide proper drive levels and prevent simultaneous output-device conduction. The output sinks or sources 2A continuously (5A pk) with ±40V output swing; the commutating diodes handle 5A pk. Finally, the thermal-shutdown circuit disables the upper output device if chip temperature exceeds 160°C.

Why the interlock circuitry? It's important to prevent simultaneous conduction of a source/sink pair's devices **(b)**. This condition usually arises during switching, when the respective devices are

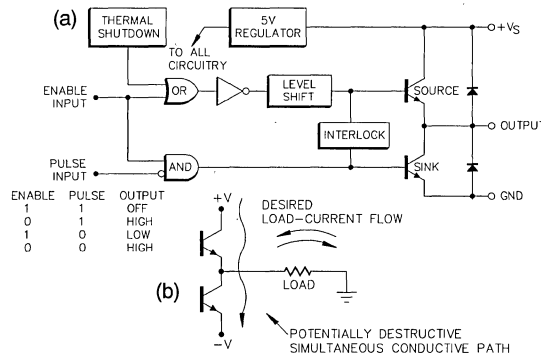


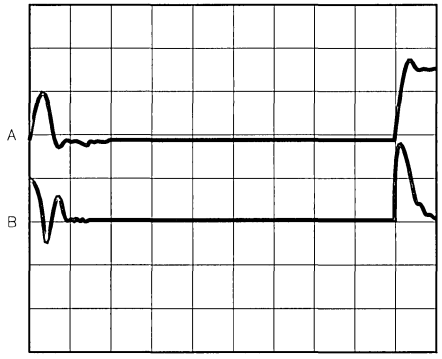
Figure 11. Providing Logic-to-Power-Drive Translation, the SG3635 **(a)** contains both low and high-level circuitry. The interlock circuitry-an important feature-allows only one power device to conduct at a time, thus avoiding transitional power-supply short circuits **(b)** An IC without the interlock can produce large current pulses **(c)** during switching. A test circuit **(d)** verifies the IC's interlock circuitry; **(e)** shows no common current flows in the output devices during switching.

interchanging OFF and ON states. During this Interval, substantial supply current flows through both devices, effectively shorting

the supplies. A common approach to alleviating the problem is to make the stage switch quickly, minimizing concurrent ON time.

The widely used 555 timer furnishes this simple solution. However, it still generates considerable supply glitches **(c).** Trace B shows the large supply-current spike the IC's output pair produces when switching (trace A). Such a current spike, in conjunction with a supply bus's impedance, can result in unacceptable system noise or device destruction.

(c)

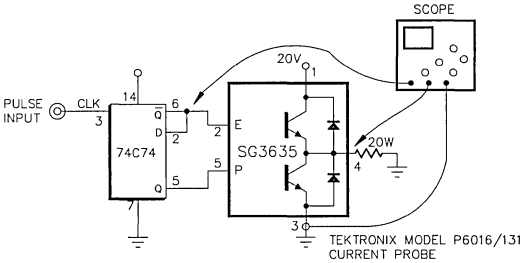


TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	200nSEC/DIV
B	500mA/DIV	200nSEC/DIV

The SG3635's interlock circuitry ensures complete turn-off of one output device before the other begins to turn on. This provision eliminates supply shorts during switching, even when controlling high power. To verify this section, use the **figure's** test circuit **(d).** Part **(e),** trace A shows one phase (Q) of the 74C74's output; trace b depicts the driver's output.

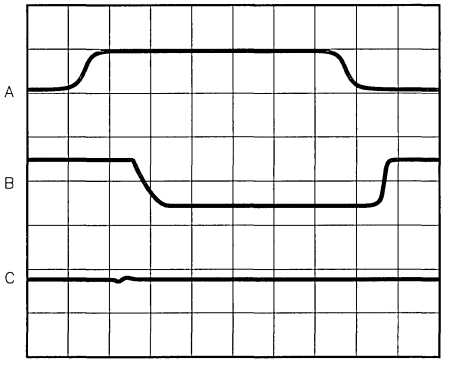
When Q switches LOW, the SG3635 unclamps its sink transistor, then allows the source device to turn on. The reverse holds true when Q switches HIGH. These intentional turn-on delays account for the 200-nsec output-timing skew. Note in trace C - the ground-pin-current - that no current ever flows directly through the source/sink pair.

(d)



NOTES:
RETURN SG3635 LOAD AND GROUND–PIN LEADS SEPARATELY TO SUPPLY

(e)



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	200nSEC/DIV
B	20V/DIV	200nSEC/DIV
C	100mA/DIV	200nSEC/DIV

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SIMPLIFIED HIGH-EFFICIENCY MOTOR DRIVE SYSTEMS WITH NEW PWM INTEGRATED CIRCUITS

Edited by Stan Dendinger
Manager, Advanced Product Development
Silicon General, Inc.

ABSTRACT

This paper describes a new pulse width modulator circuit designed specifically for DC motor control. It provides a bi-directional pulse train output in response to the magnitude and polarity of an analog error signal input. The device is useful as the control element in motor-driven servo systems for precision positioning and speed control, as well as in audio modulators and amplifiers using carrier frequencies to 350kHz.

INTRODUCTION

Power management engineers have been aware for a number of years of the efficiency advantages of switching power supplies over linear designs. In response to growing production of switchers, the semiconductor industry has spawned a number of pulse width modulator (PWM) integrated circuits of varying degrees of complexity for the control of these power supplies.

Perceptive designers soon realized that the same efficiency advantages apply to motor control. Unfortunately, when they attempted to utilize existing PWM circuits, they found that the architecture was not optimized for motor control. so many auxiliary components had to be added to work around the restrictions of the PWM circuit that totally discrete designs were frequently found to be more economical.

The main difficulty has been that PWM controllers for switching power supplies were designed to be one quadrant power conditioners; i.e., the polarity of DC output voltage is fixed and proportional to a unipolar reference voltage. A second difficulty has been that power supply controllers attempt to produce an AC waveform of variable energy content, since power must be transferred through a high frequency transformer. This requires that PWM pulses alternate from side to side with a dual-driver architecture.

The requirements for PWM motor control are different: The integrated pulse train must have a DC component proportional to the magnitude of the applied reference voltage, and a polarity determined by the sign of the reference to accomplish bi-directional rotation. All of the necessary control elements for two quadrant operation are found in the PWM circuit to be described, which is designated the SG1731.

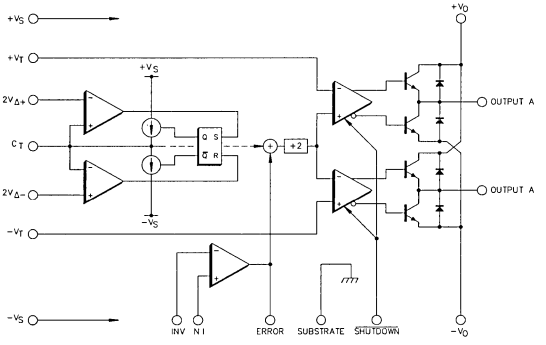

Figure 1. SG1731 Block Diagram

BLOCK DIAGRAM

The SG1731 contains a triangle waveform oscillator, a wideband operational amplifier for error voltage generation, a summing/scaling network for level-shifting the oscillator waveform, externally programmable PWM comparators, and dual ±100mA, ±32 volt totem pole drivers with commutating diodes for full bridge

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output drive. A TTL-compatible SHUTDOWN terminal forces the output drivers into a floating high-impedance state when driven LOW. Supply voltage to the circuit may be either from dual positive and negative supplies, or single-ended.

PULSE WIDTH MODULATION

Pulse width modulation occurs by adding an error voltage to the triangle waveform, attenuating the resulting signal by a factor of 2, and comparing it to threshold voltages $+V_T$ and $-V_T$, which are applied to pins 1 and 8 respectively. Figure 2 illustrates the case for $V\Delta_+ < +V_T$. When the error voltage is zero, no threshold crossings occur, and the output drivers remain in the LOW state. If the error voltage is sufficiently positive, the upper threshold will be periodically crossed by the shifted triangle waveform and output driver A will switch to the HIGH state. As the error voltage becomes larger, the duty cycle of driver A will linearly increase towards 100%. The same action occurs at output driver B for negative error voltages.

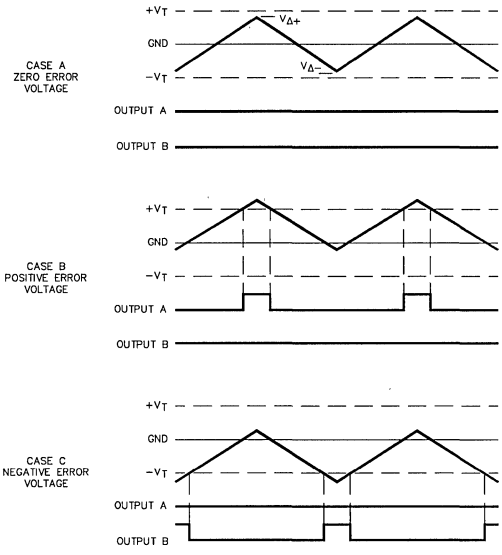

Figure 2. Deadband Operation

A motor connected across the full bridge formed by drivers A and B will receive a high frequency pulse train which, when integrated by the LR time constant of the armature, will result in a voltage drive proportional to the magnitude of the error signal. The polarity of the drive signal will be the same as the polarity of the error voltage.

With deadband operation, there is a small region around the null point of the servo loop where no power is applied to the motor. This conserves power, which may be desirable in some applications, but it also results in loss of both positioning accuracy and mechanical stiffness.

The other possible mode of operation is shown in Figure 3, where $V\Delta_+ > V_T$. At the loop null point the motor still receives drive pulses, which provides resistance to armature movement by external forces. The integrated drive voltage is still zero, since the drive pulses alternate in polarity with identical pulse widths at the null point.

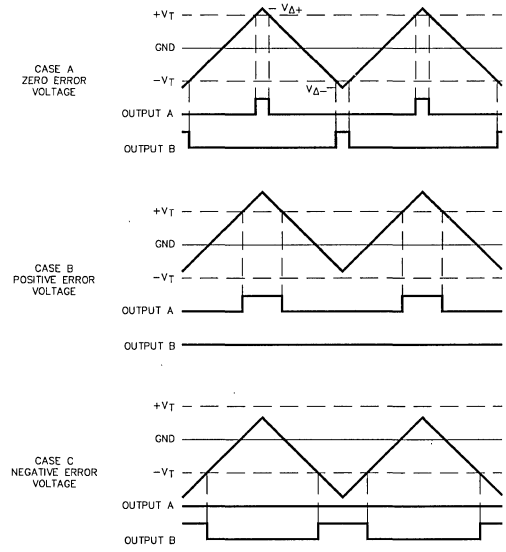

Figure 3. Non-Deadband Operation

This is the preferred mode of control in a missile fin actuator system where aerodynamic forces on the airfoil attempt to move the motor armature away from the null position. A second example where deadband operation is not desirable is a switching, or "Class D," audio amplifier. Cross-over distortion would be unacceptable, and poor speaker damping would also result.

4. OSCILLATOR CIRCUIT

The triangle oscillator consists of two voltage comparators, a set/reset flip-flop, a bi-directional 500μA current source, and an external timing capacitor C_T. A positive reference voltage applied to pin 2 (2VΔ+) sets the peak value of the triangle., and a negative reference voltage at pin 7 (2VΔ-) determines the valley of the

triangle. Normally the reference voltages are equal, so that a symmetrical waveform about ground results.

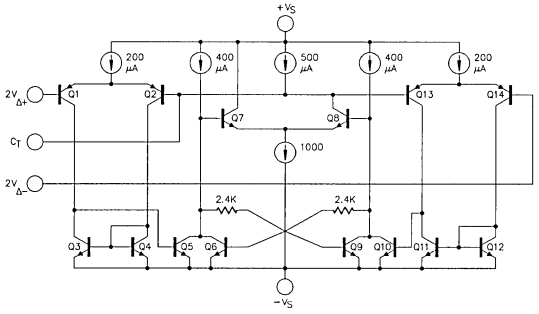

Figure 4. SG1731 Oscillator Schematic

Circuit operation is as follows: Transistors Q6 and Q9 form the set/reset flip-flop. Assume that Q9 is conducting and Q6 is off. The collector voltage of Q9 will be low compared to that of Q6, resulting in Q7 conducting and Q8 being off. The current from the 500µA source will flow into C_T and a positive voltage ramp will occur at pin 6. When the voltage exceeds 2VΔ+, the comparator formed by Q1 through Q4 changes state, turning on Q5. This removes base drive from Q9 and the flip-flop will change state. The current-steering transistor pair Q7 and Q8 now switch the 1mA discharge current source onto the C_T bus. Since the 500µA charging source is still active, the net discharge current out of C_T is the difference of the two sources, or 500µA. Since monolithic construction allows close ratioing of current sources, the discharge rate will closely match the charge rate. When the voltage on C_T falls below 2VΔ-, the comparator formed by Q11 through Q14 will reset the flip-flop and another charge cycle will begin. Since the values of the current sources are fixed at a nominal 500µA, the oscillator frequency may be calculated as follows:

For a given capacity and current,

$$\frac{dV}{dt} = \frac{I}{C}$$

or

$$dt = \frac{I}{C}\, dV$$

where

dV = V_{OSC} peak-to-peak
I = 500 µA = 5 x 10^{-4} A
dt = 1/2 T_{OSC} (assuming symmetry)
C = Variable

Therefore

$$T_{OSC} = 2dt = \frac{2CdV}{5 \times 10^{-4}}$$

The desired oscillator frequency can be obtained by first choosing a peak-to-peak voltage for the triangle waveform, and then selecting the proper value of C_T from Equation 3.

As a design aid, the solutions to Equation 3 over the recommended range of T_{OSC} and V_{OSC} are presented in graphical form in Figure 5. The lower limit on T_{OSC} is 2.85µsec, corresponding to a maximum frequency of 350kHz. The maximum value of V_{OSC}, (2VΔ+)-(2VΔ-), is 10 volts peak-to-peak for linear waveforms.

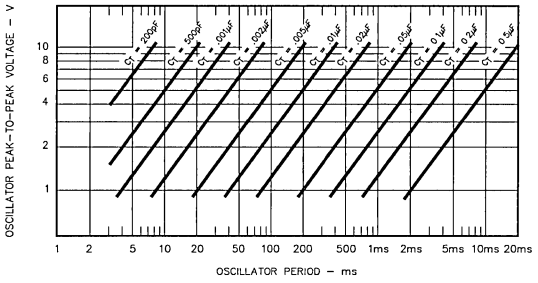

Figure 5. SG1731 Oscillator Period vs. V_{OSC} and C_T

ERROR AMPLIFIER

he error amplifier is a high slew rate unit designed for low input offset voltage and bias current under equilibrium conditions. It consists of two gain sections, with frequency compensation for unity closed-loop gain stability in the second stage. The first stage is formed by transistors Q1 through Q12. When the differential input voltage is zero, the emitter voltages of Q2 and Q3 are equal, and the collector currents of Q5 and Q6 are equal to a small fraction of the collector current in Q4 and Q7. The value of current is set by current sources Q9 and Q10 and the two 5K emitter

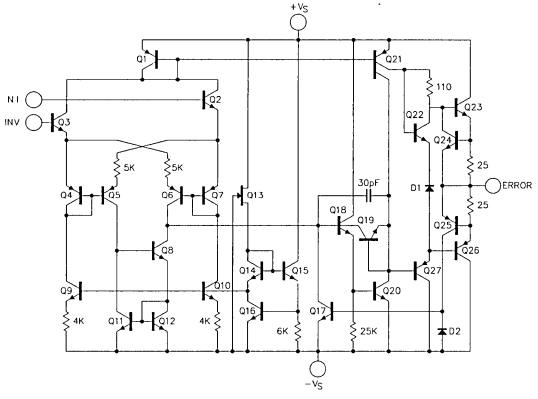

Figure 6. SG1731 Error Amp Schematic

resistors. Transistors Q8, Q11 and Q12 form a compound current mirror which converts the full differential voltage gain of the input stage into a single-ended gain referred to $-V_S$. A Darlington gain stage formed by Q18 and Q20 provides the large voltage swing required for the amplifier output. When the differential input voltage is not zero, that voltage appears across the 5K resistors of the input stage, increasing the operating current. Simultaneously this increased current is sensed by Q1, and current supply to the output stage is increased proportionally. Since more current is available to charge the 30pF compensation capacitor, the amplifier output voltage slews at a much higher rate. When equilibrium is again reached, the bias currents return to their normal quiescent levels.

As shown in Figure 7, the error amplifier is capable of excellent power bandwidth, Full output swing to 200kHz is available, with slew rates exceeding 15 volts/microsecond. These dynamic characteristics allow application to audio modulation circuits with very low transient distortion.

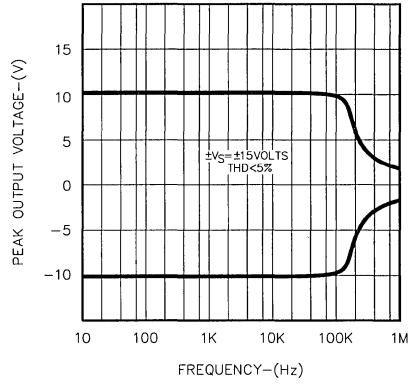

Figure 7. Error Amp Power Bandwidth

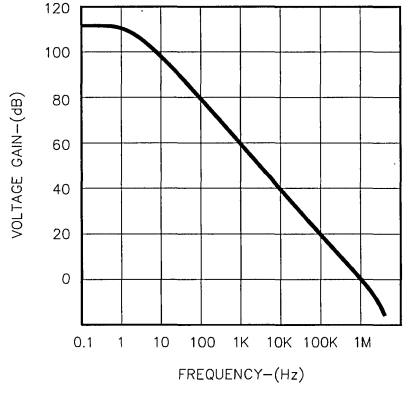

Figure 8. Error Amp Open-Loop Frequency Response

The amplifier frequency-gain plot is a constant 6dB/octave roll-off to unity gain, resulting both in unity gain stability and good transient response. Typical DC voltage gain is 110dB into a 2K load, and unity gain crossover frequency is 1 megahertz.

OUTPUT DRIVERS

The output stage is a non-saturating quasi-complementary high current switch for efficient high frequency operation. Transistors Q3, Q4, Q5 and Q6 form a high voltage Schmitt trigger input stage. The positive feedback produces fast switching times and jitter-free pulse width modulation. Q7 and Q9 provide output current sourcing, and Q8, Q10 and Q11 provide current sinking. Commutation diodes D1 and D2 clamp inductive loads to the supply rails. Their current capability is the same as the output transistors: 200mA peak.

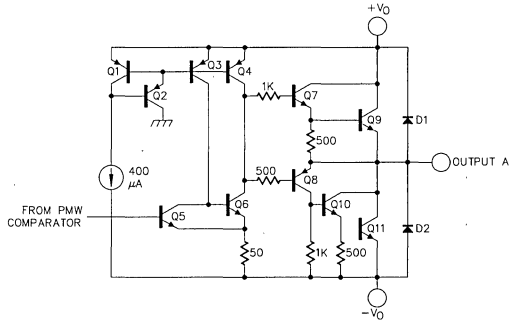

Figure 9. Half-Bridge Output Driver Schematic

TYPICAL APPLICATIONS

Simple Position Servo

A simple. low-voltage battery-powered position servo is illustrated in Figure 10. A resistive divider network sets up the reference

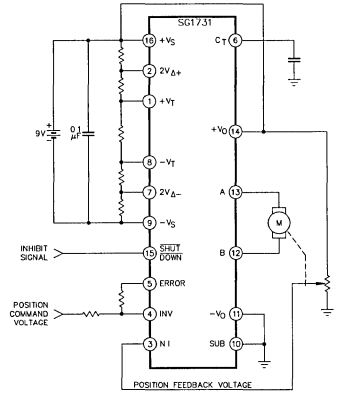

Figure 7. Error Amp Power Bandwidth

voltages for triangle waveform amplitude and PWM thresholds. Since the circuit is powered by battery, $V\Delta_+$ is designed to be less than $+V_T$ (deadband) to conserve power. The 9 volt DC motor is driven directly from the output drivers, and it in turn drives a position feedback potentiometer through a geartrain. The position feedback voltage is subtracted from the external position command voltage in the on-chip error amplifier. The difference between commanded position and actual position generates an error voltage which in turn generates a series of PWM pulses to the motor to correct the difference. Once null has been reached, no further power is applied to the motor until a new position command voltage is received, or the wiper is moved out of position by external forces.

High Torque Position Servo

Figure 11 illustrates a high power version of the previous position servo loop. The control circuit is powered from balanced positive and negative supply voltages, and the output drivers switch the load between ±32 volt supply rails for maximum output power. Complimentary emitter follower buffers on each output provide increased current gain and power handling capability.

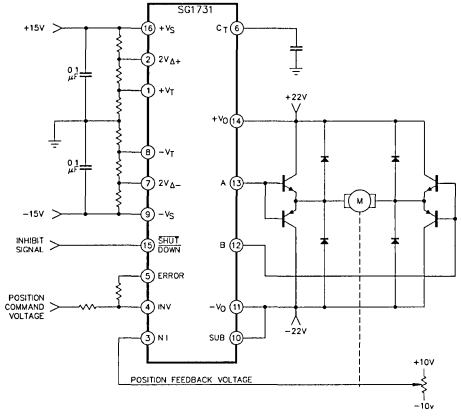

Figure 11. High Torque Position Servo

Motor Speed Control

In Figure 12, a bi-directional motor speed control circuit is derived from the previous circuit by substituting a tachometer for the position pot in the motor feedback circuit. The external command voltage now represents a speed rather than a position, with direction of motor rotation a function of command voltage polarity. Magnetic tape drives are an example of this configuration, with the velocity feedback voltage frequently derived from an encoded bit pattern on the tape.

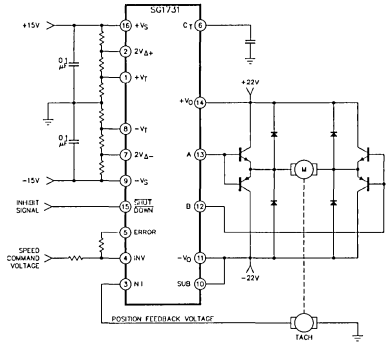

Figure 12. High Torque Bi-Directional Motor Speed Control Circuit

PWM Audio Power Amplifier

A complete PWM power audio amplifier is illustrated in this last application. The circuit reconstructs an amplified version of the audio input voltage by deriving the feedback signal from the speaker voice coil. An oscillator frequency of 300kHz was chosen to maintain a ratio of at least 15 to 1 between the carrier frequency and the highest modulation frequency (20kHz).

Ratios of at least 10 to 1 are necessary for acceptable linearity, low distortion and good transient response. An LC output filter smoothes the pulse width modulated output to the speaker; its design is critical for low distortion. This circuit, consisting of one integrated circuit and four power transistors, can deliver 150 watts RMS of power into a 4ohm load.

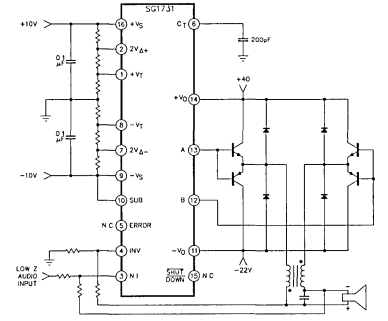

Figure 13. P.W.M. Audio Power Amplifier

CONCLUSION

A new pulse width modulator integrated circuit designed for motor control has been described which includes all the circuitry necessary for implementing high efficiency bi-directional controllers. Inputs and outputs have been designed for maximum flexibility, allowing the device to be useful in a wide range of position and speed servo systems.

SIMPLIFY FEEDBACK CONTROLLERS WITH A 2-QUADRANT PWM IC

A 2-Quadrant Pulse-Width-Modulator IC Eliminates Many of the Problems Arising With Unipolar Devices in Feedback-Control Applications.

Stan Dendinger
Manager, Advanced Product Development
Silicon General, Inc.

INTRODUCTION

The SG1731 pulse-width modulator (PWM) IC brings to motor controllers and similar applications the efficiency previously limited to switching-power-supply circuitry. As a result, you can use it to design motor-controller circuits having parts counts smaller than previously achievable.

Switching-power-supply PWM controllers are designed to be 1-quadrant power conditioners, furnishing a dc output voltage with fixed polarity and amplitude proportional to a unipolar reference voltage. Motor controllers, on the other hand, require an integrated pulse train with a dc component proportional to the magnitude of an applied reference voltage and polarity determined by the reference's sign. Otherwise, they can't produce bidirectional rotation.

In addition, the architecture of power-supply PWM ICs often proves inappropriate for motor-control tasks, requiring so many auxiliary circuits that totally discrete designs often prove more economical.

PWM power-supply controllers attempt to produce a variable-energy-content ac waveform, because power must be transferred via a high-frequency transformer. Unlike those from a PWM motor control IC, the PWM pulses produced by these devices must alternate and are therefore produced by a dual-driver architecture.

Fig 1 shows the SG1731's structure. The device contains a triangle-waveform oscillator whose frequency is determined by

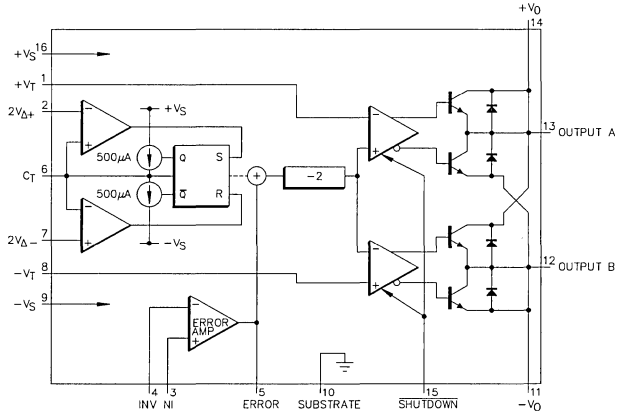

Figure 1. A DC-Motor Pulse-Width-Modulator IC. The SG1731 features 50Hz to 350kHz oscillator range, adjustable deadband operation, a high-slew-rate error amplifier, a Shutdown input providing floating outputs, and dual 100mA source/sink output drivers capable of operating from supplies to +32V.

an external capacitance at pin 6 and whose amplitude can be set through resistor or voltage programming at pins 2 and 7. The IC also contains a wide-band op amp for error voltage generation, a summing/scaling network for level-shifting the oscillator waveform, externally programmable PWM comparators and dual ±100mA continuous (±200ma pk), ±32V totem-pole drivers with commutation diodes for full-bridge output drive. Typical supply voltages are ±15V, although the device can function at values as low as ±3.5V. You can use dual- or single-polarity supply voltages. Pin 15, the Shutdown terminal, forces the output drivers into high-impedance states when LOW.

ERROR VOLTAGE CONTROLS PULSE-WIDTH MODULATION

Pulse-width modulation occurs when an error voltage gets added to the triangle waveform, attenuating the resulting signal by a factor of two and comparing it with threshold voltages $+V_T$ and $-V_T$ (pins 1 and 8). **Fig 2** illustrates the case for $V < V_T$. When the error is 0V, no threshold crossings occur, and the output drivers remain at $-V_O$ **(Fig 2a).** As the error voltage goes positive, the upper threshold gets periodically crossed by the shifted waveform, and the output driver A switches to $+V_O$ **(Fig 2b).** As the error voltage becomes larger, the duty cycle of driver A increases linearly toward 100%. The same action occurs at output B **(Fig 2c)** for negative error voltages.

A motor connected across the full bridge formed by drivers A and B receives a high-frequency pulse train. When integrated by the armature's L/R time constant, the pulse train results in a voltage drive proportional to the error signal's magnitude. Drive-signal and error-voltage polarities are identical.

NO MOTOR POWER REQUIRED WITH DEADBAND OPERATION

With this deadband operation, no motor power gets applied in a small region around the servo loop's null point. Although this action conserves power (desirable in some applications), it results is a loss of both positioning accuracy and mechanical stiffness. Deadband operation is also not desirable in switching (Class D) audio amplifiers. There, crossover distortion is unacceptable and poor speaker damping results (see "Class D amplifiers for audio applications").

The other SG1731 mode of operation is shown in **Fig 3,** where $V > V_T$. At the loop null point, the motor receives drive pulses that resist externally produced armature movement. The integrated drive voltage is 0V with no error voltage **(Fig 3a)** because the drive pulses alternate in polarity and have identical widths at the null point. **Figs 3b** and **3c** show the effects of error voltages on the oscillator signal.

This is the preferred control mode in a missile-finactuator system, for example, where aerodynamic forces on the airfoil attempt to move the motor armature away from the null position.

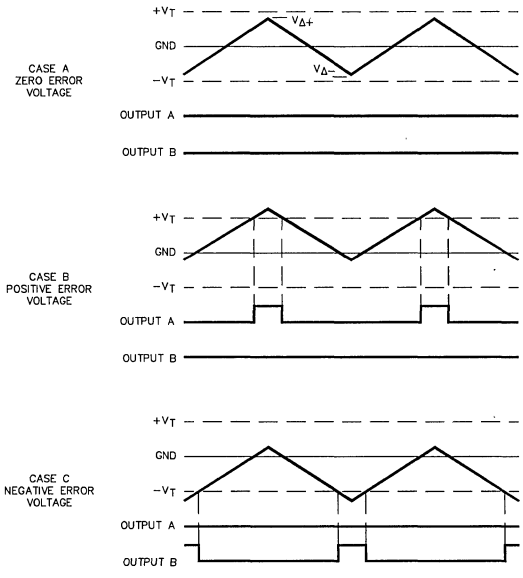

Figure 2. With Oscillator Voltage Less Than Threshold Voltage, the SG1731's Outputs Switch LOW to HIGH When the Error Voltage Shifts Oscillator Output Outside the Threshold

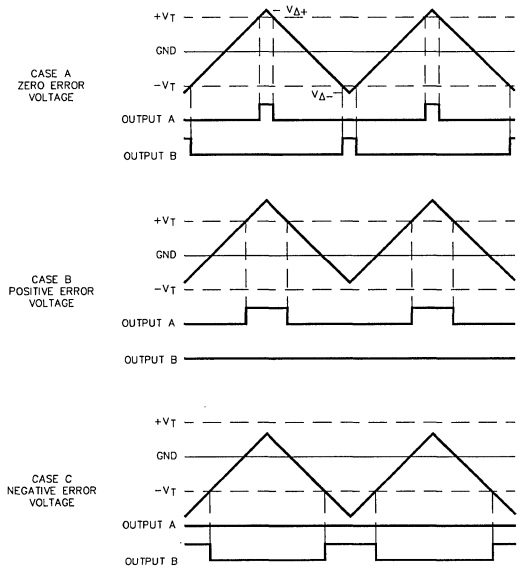

Figure 3. With Oscillator Voltage Greater Than Threshold Voltage in the SG1731, Lack of a Deadband Provides Resistance to MotorMovement Caused by External Forces.

You can configure the SG1731 as a bidirectional motor-speed controller as shown in **Fig 4.** The motor specified runs directly from the device's outputs, and the tachometer produces an output directly proportional to the motor's speed and direction. This high-level signal gets divided down and filtered by the discrete components associated with the tachometer, then applied to the SG1731's error-amplifier input. The 1731 internally compares this signal with the speed-control input's value and provides output drive of the appropriate phase and magnitude, completing a speed-control loop. Set the comparator voltages for nondead-band operation. The lowest rotation speed depends on the motor's friction characteristics.

Instantaneous-direction-reversing applications might require an optional current-limiting circuit rather than ±15V applied directly to pins 11 and 14. At the time of direction reversing, the motor draws peak currents that could damage the 1731's output drivers. Q_1's ability to supply current is controlled by Q_2's state, which in turn depends on the voltage across the 4Ω current-sensing resistor. If the motor current exceeds 200 to 250mA, Q_2 turns on and Q_1 shuts off.

EXTEND CONTROL CAPABILITY WITH HIGH-CURRENT DRIVERS

Another bidirectional speed-control loop appears in **Fig 5.** Here, SG1635 drivers control higher motor power and eliminate the need for a speed-monitoring tachometer; instead, back EMF produced by the motor serves as a feedback signal. This arrangement entails some increase in circuit complexity but eliminates the tachometer's cost.

The circuit's basic servo mode is similar to that of **Fig 4.** The 311 comparator (IC_1) senses the polarity of the input command signal. Its output goes to the 1635s via a diode and inverter, allowing both 1635s to be OFF, neither sinking no sourcing current, when the 1731 is not producing output pulses. **Fig 6** shows the circuit waveforms. When either 1731 output is HIGH, the other output is LOW, and the motor is driven. When both outputs are LOW, the 1635s are OFF and the motor is electrically floating.

The motor's inductive turn-off spike gets damped by the 1635s' internal diodes. After turn-off, the waveform returns to a dc level

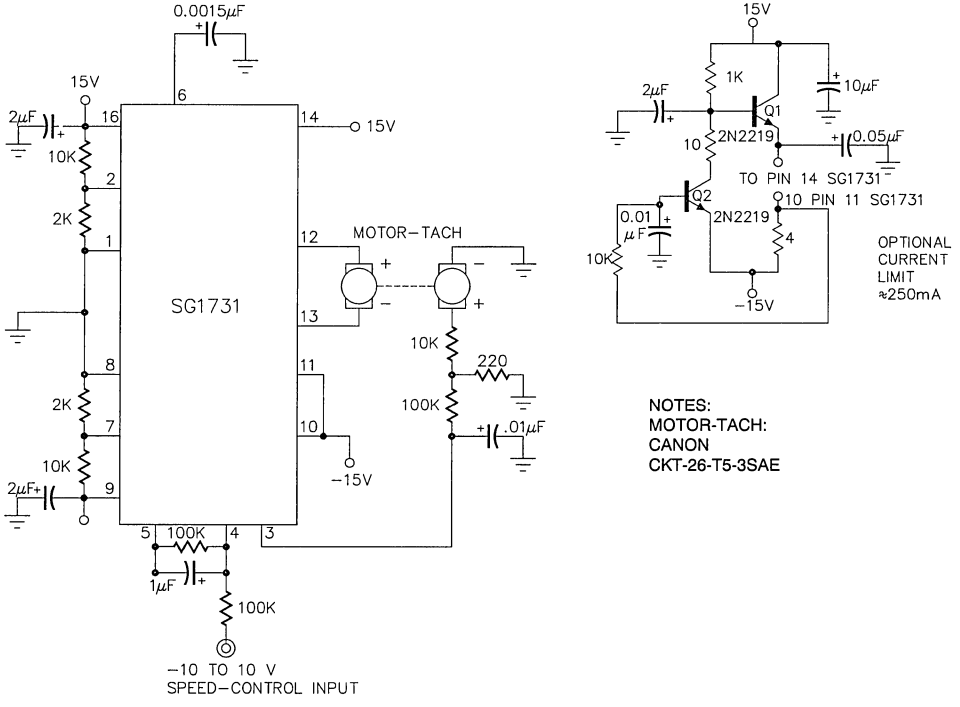

Figure 4. In This Bidirectional Motor-Speed Controller, the Tachometer Provides Feedback While the Current-Limiting Circuit Protects the Outputs From Surge Currents.

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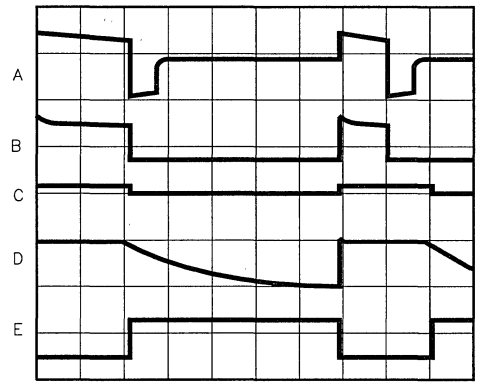
determined by the back EMF of the undriven motor, now functioning as a tachometer. This level gets differentially picked off by the 301A op amp (IC_3), whose output feeds a switched synchronous filter. This filter, composed of the FET and the 100-kΩ/0.01-μF combination, samples the back-EMF value during the motor's powered interval.

A 311 (IC_2) gates the FET switch synchronously with the 1731's output. The diode-RC network feeding IC_2 allows either output to actuate the filter. The 10-kΩ/0.02-μF network's decay time length (**Fig 6,** trace D) ensures that the FET drive (trace E) remains OFF until well after the inductive spike has settled out.

The pure dc filter output feeds back to the 1731's amplifier to complete the speed-control loop. The zener-diode bridge clamps all inputs above approximately ±10V; otherwise the 1731's outputs would saturate at dc and the switched feedback loop would never operate.

Another SG1731 application appears in **Fig 7.** Here, two 1731's bidirectionally control the speed and shaft position of a printed-circuit-type motor.

The shaft position gets sensed at the output of a geardown transmission. Slave the 1731s together to avoid producing



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	200μSEC/DIV
B	20V/DIV	200μSEC/DIV
C	10V/DIV	200μSEC/DIV
D	20V/DIV	200μSEC/DIV
E	20V/DIV	200μSEC/DIV

Figure 6. Waveforms for Fig 5's Tachless Controller Include the Controller's Outputs (traces B and C) and the Voltage Across the motor (trace A). The 10-kΩ/0.02μF Network's Decay Time (trace D) Ensures that the FET Drive (trace E) Remains off Until After the Inductive Spike has Settled out.

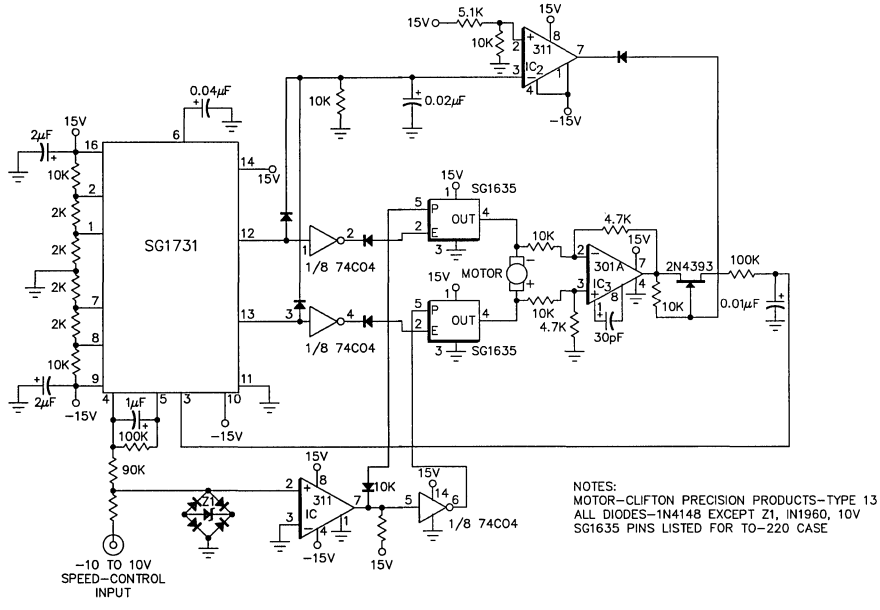


Figure 5. A tachless controller based on the 1731 uses motor back EMF and some additional parts to reduce overall cost.

frequency beating from separate oscillators; take the triangle waveform of $SG1731_A$ through a 301A follower and use the output to drive the capacitor pin of $SG1731_B$. This is an effective way to slave 1731s together because the follower's low-impedance output overrides whatever state the unbiased internal oscillator of $SG1731_B$ might take. Control the shaft position by sensing it with a potentiometer that feeds a signal back to $SG1731_A$. This signal then gets compared with the Position input, and the outputs of $SG1731_A$ drive the shaft to the position required to balance the error amplifier's inputs.

$SG1731_B$ functions in a speed-control loop similar to that described in **Fig 4.** It controls speed by using its output pins, via a diode OR gate, to pulse-width-modulate $SG1731_A$'s Shutdown pin. The 311 comparator prevents either $SG1731_B$ output from going LOW on a dc basis by synchronously gating signals into the device's output comparators, forcing the appropriate output HIGH.

Consider $SG1731_A$ to be a position servo; $SG1731_B$'s controls how quickly the position is acquired. Deadzone control results from voltage-modulating $SG1731_B$'s comparator thresholds.

Fan-temperature control safeguards instruments

You can also use a 1731 to control a fan motor's speed, regulating instrument temperature and extending fan life **(Fig 8).** At least one oscilloscope manufacturer uses this approach, and it has also found use in several military applications.

When power is applied, the thermistor, located near the fan, has a high resistive value. This condition unbalances the amplifier-driven bridge, sending pin 12 LOW. Q_1 and the fan motor are off. But as the instrument warms, thermistor resistance decreases, producing PWM signals at pin 12 and turning Q_1 and the fan motor on.

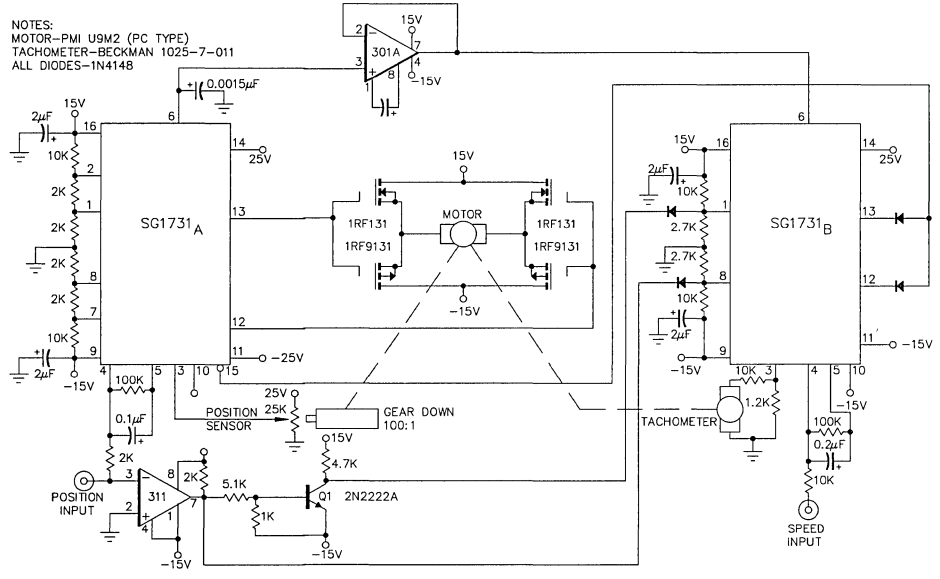


Figure 7. In this bidirectional motor - speed - controller / positioner application, $SG1731_A$ acts as a position servo, while $SG1731_B$ controls speed.

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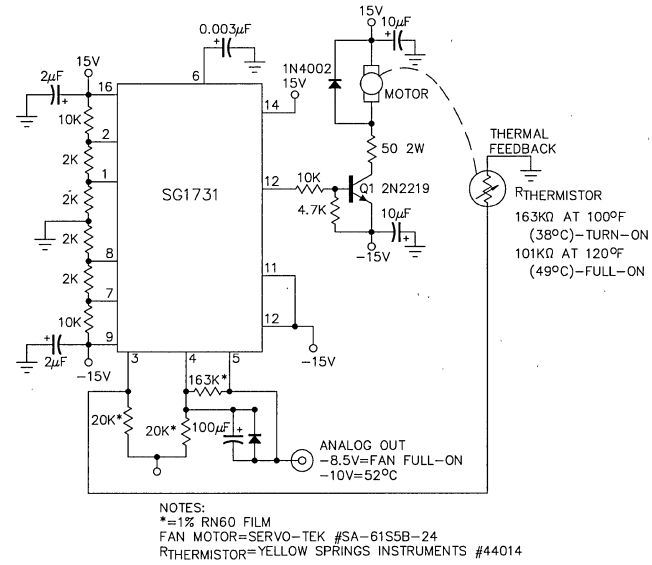


Figure 8. A Fan-Temperature Controller's Error-Amplifier Output (pin 5) Warns of an Overtemperature Condition

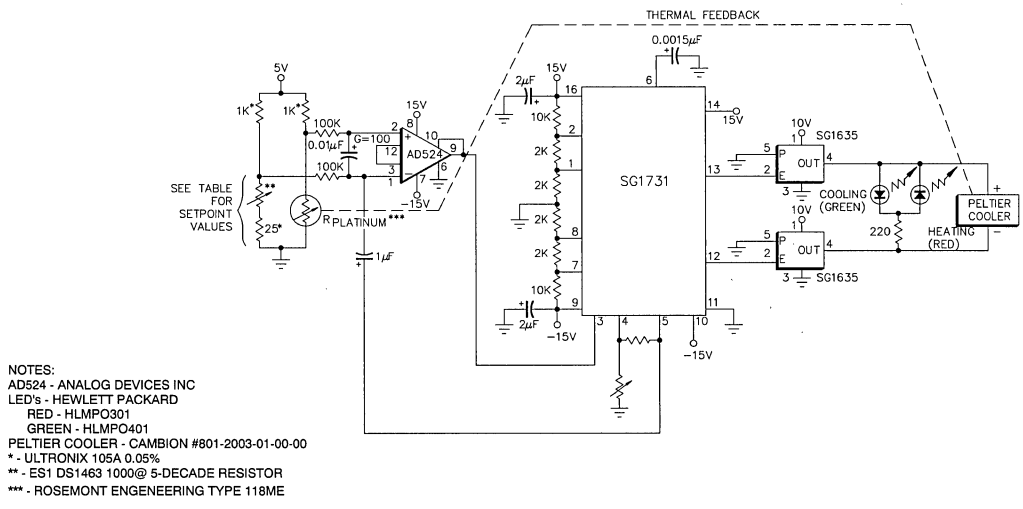


Figure 9. A Well-Insulated Peltier Cooler With Good Heat Removal on its Normally Hot Side Specs Stability Better Than 0.02°C typ.

ELIMINATE SERVO HUNTING WITH LONG TIME CONSTANTS

The 100-μF capacitor determines the time constant across the error amplifier; a short time constant produces audibly annoying hunting in the servo. The 50Ω resistor limits motor current, and the IN4002 diode dampens motor spikes.

The SG1731 can function in nonmotor applications, too. The freezing point of water serves as a reference point for the calibration of various types of temperature sensors, such as platinum RTDs and thermocouples. In such applications, an ice slurry in a Styrofoam container or a Dewar bottle is usually used to achieve the 0°C condition. Although inexpensive, this approach requires constant ice replenishment and water removal and tends to be messy. As an alternative, you can use the SG1731 to provide 2-quadrant control for a Peltier-junction-type thermoelectric cooler.

Current flow in a Peltier device cools one side of the junction and heats the other; reversing the applied current causes the cold side of the junction to heat and the hot side to cool. Commercial devices use a large number of junctions to achieve high thermal capacity and are about the size of a postage stamp. They are optimized for one direction of current flow but can work both ways.

TEMPERATURE REFERENCE IS BIDIRECTIONAL

Fig 9's circuit capitalizes on this characteristic to achieve a very precise temperature reference that cools to 0°C and then settles out very quickly. Most thermal control loops settle slowly because energy can only be removed (as in a refrigerator) or added (as in a crystal oven). But because the Peltier device is thermodynamically bidirectional, it's an ideal choice for use in a low-temperature servo.

When power is applied, the platinum sensor (at a high resistive value) unbalances the bridge and causes the AD524 instrumentation amplifier to saturate negatively. This action turns the 1731 and its 1635 drivers on, resulting in current flow through the Peltier device in the cooling direction. When the temperature reaches 0°C, the 1731 tends to cut off, causing loop overshoot. However, the heat-pump reversal in the Peltier device forces short thermal settling times.

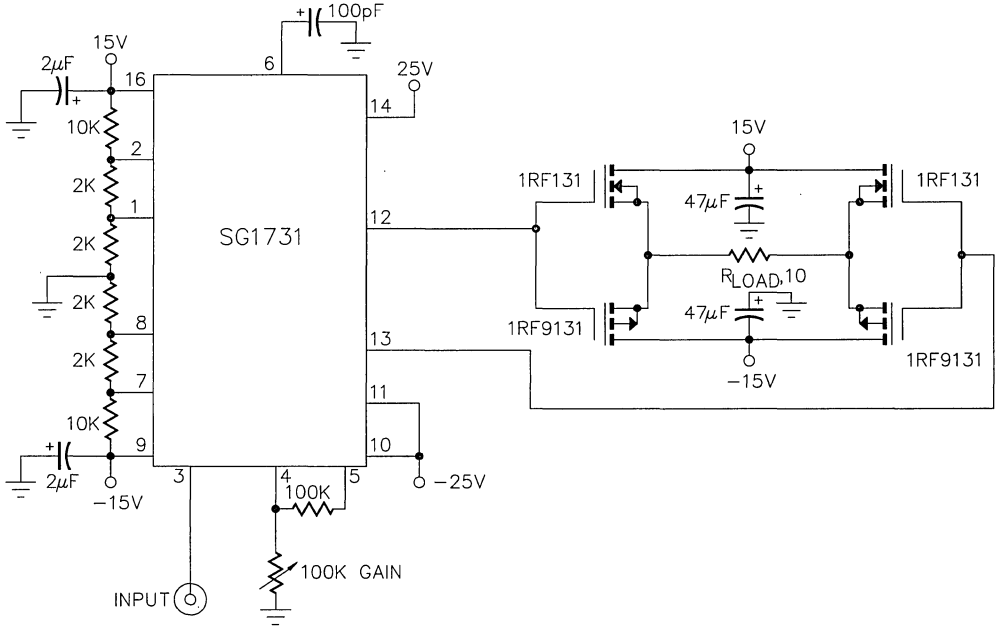


Figure 10. A Switched-Mode Power Amplifier Using a 25-kHz Carrier Transmits a 400-Hz Waveform to a Load

12

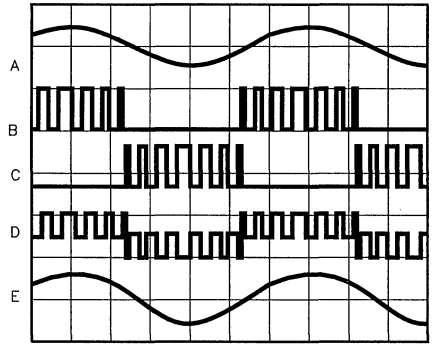
The 100-kΩ potentiometer adjusts loop gain; the 1-μF capacitor sets bandwidth. The 100-kΩ resistors and the 0.01-μF capacitor across the instrumentation amplifier filter out the fast chopping noise the platinum sensor, a wiresound device, picks up.

If you use the resistance decade shown, you can control the junction at any desired temperature around 0°C. For an ideal 1000Ω sensor at 0°C, the **table** values shown in **Fig 9** apply. You can substitute the actual 0°C value for the platinum sensor used, biasing all values by the difference between the sensor resistance at 0°C and 1000Ω. The bidirectional thermal control and high loop gain produce very rapid response to any shift in temperature setpoint, plus high stability.

MOTORS ADAPT EASILY TO CLASS D OPERATION, SPEAKERS DON'T

Finally, the SG1731's 2-quadrant capability allows its use as a switched-mode (Class D) power amplifier. Motors and other devices that can integrate the time-power spectrum of Class D amplifier output are obvious loads. The design can also serve audio applications but requires careful attention to output filtering to achieve acceptable distortion levels.

Fig 10 shows the 1731 set up to deliver high power to a 10Ω load via complementary power FETs. The device's output stage swings ±25V, providing a 10V enhancement for turning on the FETs. The active 1731 outputs are ideal for driving power FETs because they can both source and sink the relatively high gate currents caused by the FETs' input capacitances. **Fig 11** shows the waveforms associated with this circuit.



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	500μSEC/DIV
B	50V/DIV	500μSEC/DIV
C	50V/DIV	500μSEC/DIV
D	50V/DIV	500μSEC/DIV
E	20V/DIV	500μSEC/DIV

Figure 11. In These Waveforms for Fig. 10's Amplifier, Trace A is the Amplifier's Input, Traces B and C the 1731's Outputs and Trace D the Waveform Across the Load. Trace E, a 3-kHz Filtered Version of Trace D, Shows That Power Density Approximates Input Signal

CLASS D AMPLIFIERS FOR AUDIO APPLICATIONS

Almost all amplifiers use some form of output pass element to deliver power to a load. Because the amplifier controls this pass element, and because the amount of power delivered to the load varies, dissipation is inevitable. And at high power, substantial dissipation losses place limits on packaging, power consumption and efficiency.

One form of amplifier, the Class D stage, largely circumvents these problems by using a switch-mode output stage to deliver power to the load. Because the amplifier's output is either ON or OFF, efficiency is higher than that of a linear stage, and heat dissipation is low. In **Fig 12,** the output of such a stage is represented by a series of width modulated pulses whose power-time spectrum is related to the input signal.

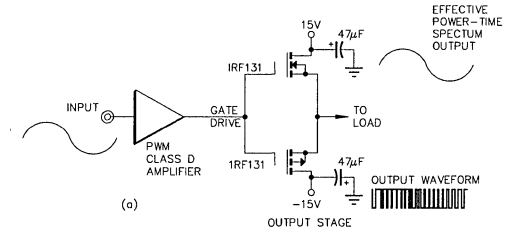


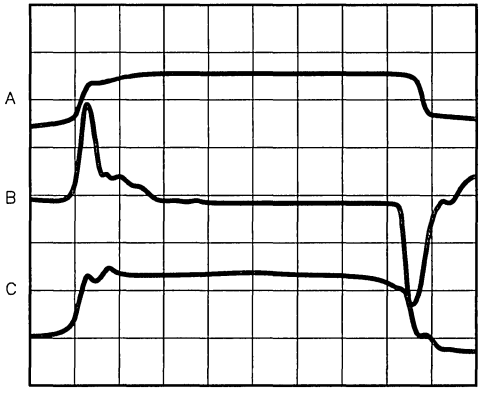
Figure 12. A Switched-Mode PWM Class D Amplifier Coupled to an FET Output Stage Provides Efficient Operation

In theory, this type of stage can serve in an efficient audio amplifier. And recently, designers have expressed a great deal of interest in developing such an amplifier. However, practical problems have made a workable switching design for audio difficult to achieve.

Historically, switched-mode-amplifier designs called for complex circuitry and expensive output devices. Producing a pulse-width modulator that provides 2-quadrant response with high linearity and wide bandwidth was difficult. In addition, even if available, low-loss output switches that operated at high carrier frequencies were expensive, and the drive circuitry quite complex.

The introduction of power-FET devices has reduced design-cost and complexity problems in the output stage. But although such components make the job easier, designers still must deal with several issues to achieve optimum performance.

One unpleasant surprise is the combination of the high-frequency carrier and the FET's input capacitance. The FET gate drive (**Fig 13**, trace A) causes the current drawn through the input capacitances (trace B) to peak at 400mA on both edges as the FETs switch. Although the FETs have a high impedance at dc, the high carrier frequency required for audio calls for substantial average gate current. This requirement in turn calls for some form of preceding driver.



TRACE	VERTICAL	HORIZONTAL
A	50V/DIV	200nSEC/DIV
B	200mA/DIV	200nSEC/DIV
C	20V/DIV	200nSEC/DIV

Figure 13. Fig 12's FET Output Stage Draws 400mA pk Gate Current When the FET's Switch (trace B). Trace A is the Gate Drive Signal; Trace C, the FET's Source Lines.

A more serious problem centers on filtering the carrier at the load (a speaker in audio applications). Filter design is complicated by the uncertain characteristics of the lead wire and speaker that connect to the amplifier. Even if these parameters are fixed by specification, the speaker's reactive nature complicates the design.

Even assuming the filter can be built, the waveform across the speaker is well out of the phase with the input because of carrier-induced phase shift as well as filter phase shift. As a result, closing a feedback loop from the load proves difficult. It might be possible to use a complementary phase-shift network to correct for this shortcoming, but the design of this type of an audio-grade compensation scheme is difficult. Without feedback, the problem goes away, but nonlinearities in the pulse-width modulator then contribute to output distortion.

Finally, the high-frequency harmonics in the switching stage pose a difficult RFI-suppression problem. The same fast switching that yields efficiency and wide-range audio bandwidth also qualifies as a potential broadband radio transmitter and must be suppressed. This need mandates careful layout, expensive and complex packaging and RFI suppression on both power and speaker connections.

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