SONY

Semiconductor IC

Data Book 1990

A/D,D/A Converters

SONY

Semiconductor Integrated Circuit Data Book

1990

Preface

This is the 1990 version of the Sony Semiconductor IC databook. This book covers all the Converter Semiconductor products manufactured and marketed by Sony Corporation of America.

In preparation of this databook, as much characteristic and application data as possible have been collected and added with a view of making this book a convenient reference for users of Sony products. If, however, you are dissatisfied with this book in any way, please write; we welcome suggestions and comments.

The contents of this data book although accurate and complete at the time of publication, are subject to change in order to incorporate improvements on the products.

Circuits shown are typical examples illustrating the operation of the devices. They are not meant to convey any patents or other rights. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

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High Speed Converters

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3. IC Nomenclature

1) Nomenclature of IC product name

Currently, both the conventional and new nomenclature systems are mixed in naming IC products.

(1) Conventional nomenclature system

[Example] CX20011A

- Improvement mark
  "A" is affixed when specifications are partially improved.
- Product number
  Identifies individual product.
- Category number
  Indicates the product category in one or two digits.
  - Bipolar IC: 0, 1, 8, 10, 20, 22
  - MOS IC: 5, 7, 23, 79
- Sony IC mark

(2) New nomenclature

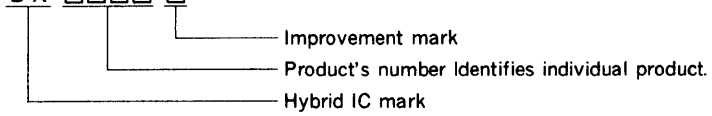
[Example] CXA1001AP

- Package mark
  - P : Plastic Dual Inline Package
  - D : Ceramic Dual Inline Package
  - M : Small outline Package(Mini Flat Package)
  - L : Single Inline Package
  - Q : Quad Flat Package
  - S : Shrink Dual Inline Package
  - K : Leadless Chip carrier
- Improvement mark
  "A" is affixed when specifications are improved.
- Product number
  Identifies the individual product.
- Product category mark
  - A : Bipolar IC
  - B : Bipolar digital IC
  - D : MOS logic IC
  - K : Memory
  - P, Q: Microcomputer
  - L : CCD signal processor
- Sony IC mark

2) Hybrids nomenclature

(1) Conventional nomenclature system

[Example] B X - □□□□ - □



4. Precautions for IC Application

1) Absolute maximum ratings

The maximum ratings for semiconductor devices are normally specified by "absolute maximum ratings". The values shown in the maximum ratings table must never be exceeded even for a moment.

If the maximum rating is ever exceeded, device deterioration or damage will occur immediately. Then, even if the affected device can operate, the life will be considerably shortened.

Maximum rating must never be reached for any TWO items at the SAME time.

IC maximum ratings

The following maximum ratings are used for ICs.

(1) Maximum power supply voltage Vcc (V_{DD})

The maximum voltage that can be applied between the power supply pin and ground pin.

This power supply voltage rating is directly related to the dielectric voltage of transistors in the internal circuit; the transistors may be destroyed if this voltage is exceeded.

(2) Allowable power dissipation P_D

The maximum power consumption allowed in IC

In the circuit design the absolute maximum ratings must not be exceeded, and it must be designed only after considering the worst situations among the following:

- Fluctuation in source voltage
- Scattering in the electrical characteristics of electrical parts (transistors, resistors, capacitors, etc.)
- Power dissipation in circuit adjustment
- Ambient temperature
- Fluctuation in input signal
- Abnormal pulses

If this allowable power dissipation is exceeded, electrical and thermal damage may result.

This value varies with the amount of IC integration in package types.

(3) Operating ambient temperature Topr

The temperature range within which IC can operate satisfactorily.

Even if this temperature range is exceeded and some deterioration in operating characteristics is noted, the IC is not always damaged.

For some ICs, the electrical characteristics at Ta=25°C are not guaranteed even in this temperature range.

(4) Storage temperature Tstg

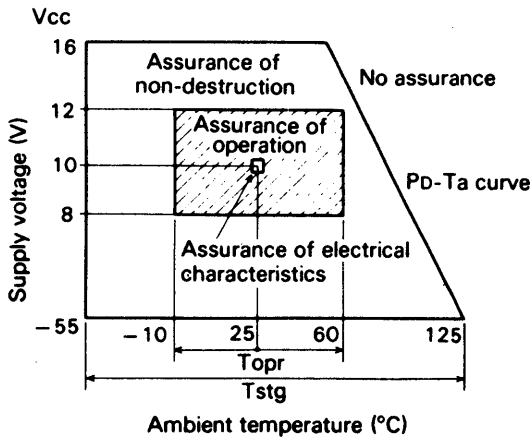
The temperature range for storing the IC which is not operating.

This temperature is restricted by the package material, and the intrinsic properties of the semiconductor.

(5) Other values

The input voltage Vin, output voltage Vout, input current Iin, output current Iout and other values may be specified in some IC's.

The relationship among these maximum ratings for IC is shown below.



2) Protection against electrostatic breakdown

There have been problems concerning electrostatic destruction of electronic devices since the 2nd World War. Those are closely related to the advancement made in the field of semiconductor devices; that is, with the development of semiconductor technology, new problems in electrostatic destruction have arisen. This situation, perhaps, can be understood by recalling the case of MOS FET.

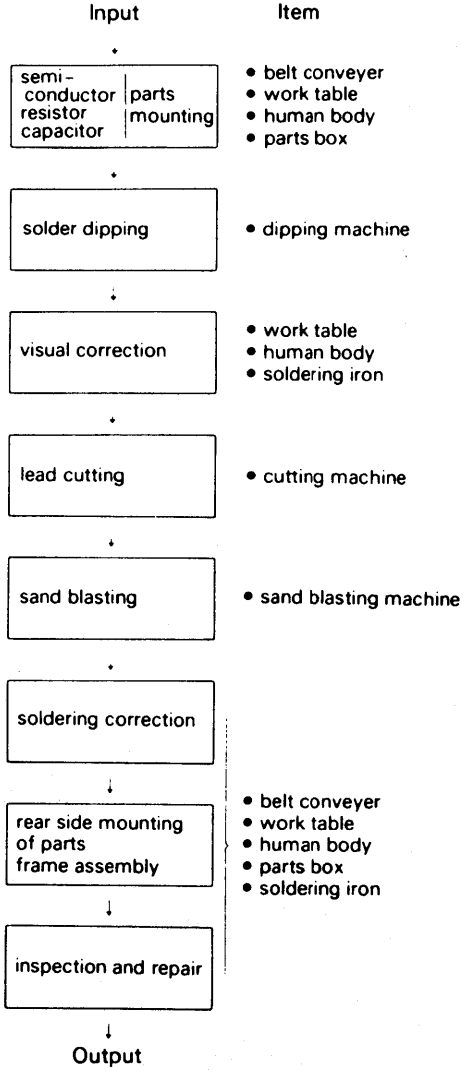
Today, electrostatic destruction is again drawing people's attention as we are entering the era of LSI and VLSI. Here are our suggestions for preventing such destruction in the device fabrication process.

Factors causing electrostatic generation in manufacture process

A number of dielectric materials are used in manufacture process. Friction of these materials with the substrate can generate static electricity which may destroy the semiconductor device.

Factors that can cause electrostatic destruction in the manufacture process are shown below:

Causes of electrostatic destruction of semiconductor parts in manufacture process



Handling precautions for the prevention of electrostatic destruction

Explained below are procedures that must be taken in fabrication to prevent the electrostatic destruction of semiconductor devices.

The following basic rules must be obeyed.

① Equalize potentials of terminals when transporting or storing.

② Equalize the potentials of the electric device, work bench, and operator's body that may come in contact with the semiconductor device.

③ Prepare an environment that does not generate static electricity.
One method is keeping relative humidity in the work room to about 50%.

Operator

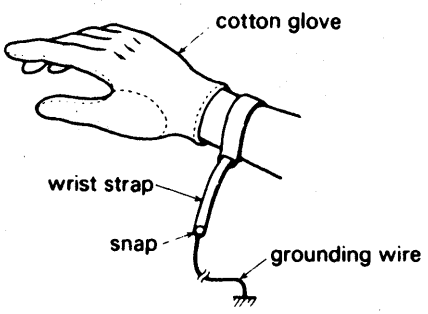
(1) Clothes

Do not use nylon, rubber and other materials which easily generate static electricity. For clothes, use cotton, or antistatic-treated materials. Wear gloves during operation.

(2) Grounding of operator's body

The operator should connect the specified wrist strap to his arm. If the wrist strap is not available, then the operator should touch the grounding point with his hand, before handling any semiconductor device.

example of grounding band

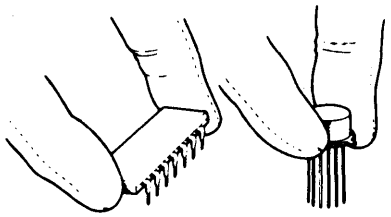


When using a copper wire for grounding, connect a 1MΩ resistance in series near the hand for safety.

(3) Handling of semiconductor device

Do not touch the lead. Touch the body of the semiconductor device when holding. Limit the number of handling times to a minimum. Do not take the device out of the magazine or package box unless it is absolutely necessary.

holding of semiconductor device



DIP type can type

Equipment and tools

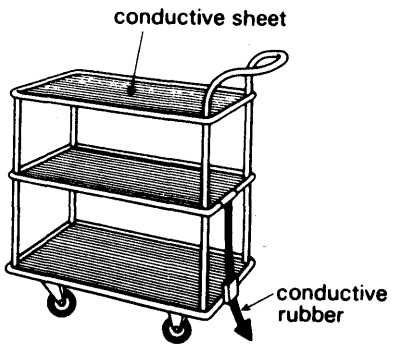
(1) Grounding of equipment and tools

Ground the equipments and tools that are to be used. Check insulation beforehand to prevent leakage.

[Check point]

- measuring instrument
- conveyer
- electric deburr brush
- carrier
- solder dipping tank
- lead cutter
- shelves and racks

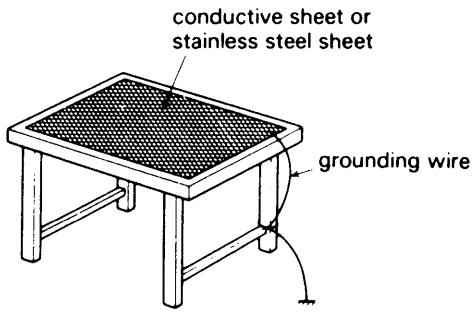
grounding of carrier



(2) Grounding of work table

Ground the work table as illustrated. Do not put anything which can easily generate static electricity, such as foam styrol, on the work table.

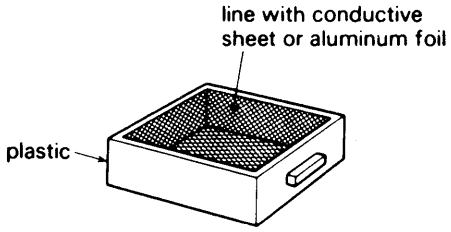
grounding of work table



(3) Semiconductor device case

Use a metal case, or an antistatic plastic case (lined with conductive sheet or aluminum foil).

plastic case for semiconductor devices



(4) Insertion of semiconductor device

Insert the semiconductor device during the mounting process or on the belt conveyer. The insertion should be done on a conductive sheet, or on a wood or on a metal carrier.

(5) Operation in energized state

When the substrate is checked while energizing the substrate where the delicate semiconductor device is mounted, be sure to place the substrate on corrugated cardboard, wood, or on a metal carrier.

(6) Other points of caution

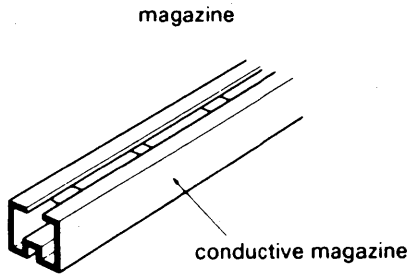
Take note of the kind of brush material used for removing lead chips. Use metal or antistatic-treated plastic brushes.

Transporting, storing and packaging methods

(1) Magazine

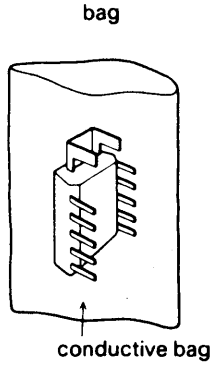
Use metal, or antistatic-treated plastic IC magazines.

Plastic magazines used for shipping ICs are antistatic-treated, and they can be used for storing ICs.



(2) Bag

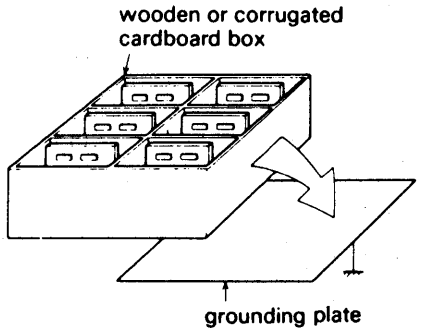
Use a conductive bag to store ICs. If the use of a vinyl bag is unavoidable, be sure to wrap the IC with aluminum foil.



(3) Handling of delivery box

The delivery box used for carrying substrates must be made of wood or corrugated cardboard. Do not use a vinyl chloride or acrylic delivery box, otherwise static electricity will be generated.

handling of delivery box



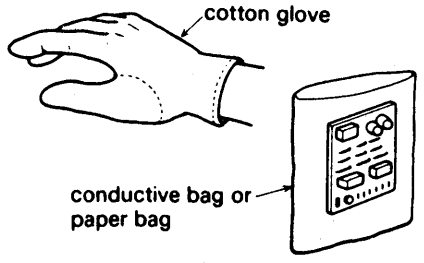
(4) Treatment after vehicle transport

After truck transport, place the magazine, package box or delivery box on the grounded rack, work table, or concrete floor for discharging. Do not pull the delivery box for more than 1 meter except on a concrete or a wooden floor.

(5) Handling of mounted substrates

Wear cotton gloves when handling. As far as possible, avoid touching soldered faces. When handling mounted substrates individually, be sure to use a conductive or paper bag. Do not use a polyethylene bag.

handling of mounted substrate



Soldering operation

(1) Soldering iron

Use a soldering iron with a grounded metal part or a soldering iron with an insulation resistance greater than 10 MΩ (DC 500V). after five minutes from energizing.

(2) Operation

After inserting the semiconductor device into the substrate, solder it as quickly as possible. Do not carry the substrate with the inserted semiconductor device by car.

(3) Correction

When correcting parts (semiconductor device and CR parts) after solder-dipping, be sure to wear cotton gloves. Also, connect the grounding band to the arm, or touch the grounding point before operation.

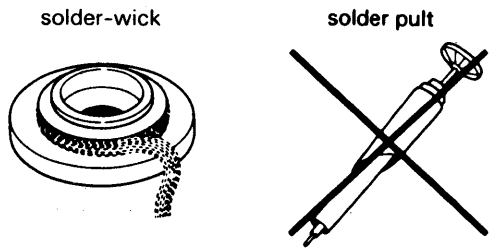
(4) Manual soldering

Solder with wrist strap connected to the hand, or by touching the grounding point from time to time during operation.

(5) Removing semiconductor device

Do not use the Solder-Pult when removing the semiconductor device. Use a Solder-wick or equivalent.

solder remover



(6) Soldering work table

Use a grounded work table, corrugated cardboard, or wooden work table for soldering. Do not solder on foam styrol, vinyl, or decorative board.

3) Mounting method

Soldering and solderability

(1) Solderability by JIS

JIS specifies solderability of an IC terminal (lead) in "JIS-C7022 Test Procedure A-2". An abstract of this standard follows:

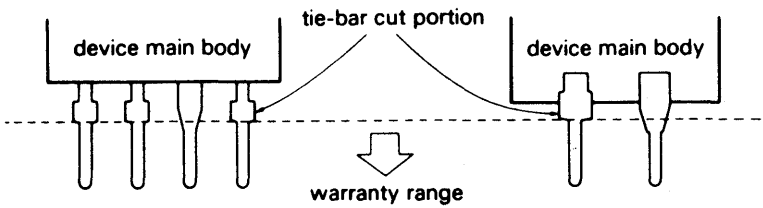
- Rosin flux must be used, and the terminal must be dipped in it for 5-10 seconds.
- H63A or equivalent solder must be used, and the terminal must be dipped in the solder which has been heated to 230°C±5°C for 5±1 seconds.
- Using a microscope, measure the area (%) deposited with solder. JIS specifies that more than 95% of the total area should be coated with solder.

(2) Area for soldering warranty

Soldering is warranted for a specific portion of the terminal. The warranted portion is shown in the following figure.

The tie-bar cut portion also serves as a dam to prevent the sealing resin flowing out during device fabrication; it is cut off at the end of the process. Since the terminal is exposed at the cut-off end, the area for soldering is restricted. The portion near the resin is often covered with burrs when sealing with resin; it is not in the soldering warranty area.

warranty area for soldering



Resistance to soldering heat

(1) Specification of JIS

JIS specifies the method for testing the resistance to soldering heat. This method is used for guaranteeing the IC resistance against thermal stresses by soldering. An abstract of this standard is as follows:

- Dip the device terminal only once for 10±1 seconds in a solder bath of 260°C±5°C, or for $3^{+0.5}_{-0}$ seconds in a solder bath of 350°C ±10°C, for a distance of up to 1 to 1.5 mm from the main body.

For the solder flow system temperature should be 260 °C ±5 °C. To solder by soldering iron temperature should be 350 °C ±10 °C.

- Leave the device for more than two hours after dipping, then measure the device characteristics.
- Normally, the warranty is limited to 10 seconds at 260 °C ±5 °C. The distance between the device main body and solder bath is 1.6 mm.

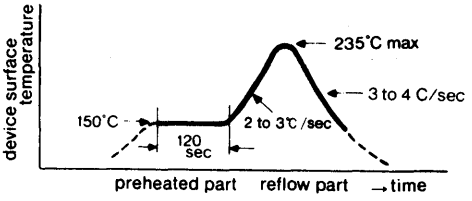
(2) Resistance to soldering heat when mounting infrared reflow.

When surface mount Devices (SOP, QFP etc) are dipped directly into a solder pot.

The device moisture resistance may deteriorate and thermal stress generate cracks in the pallet.

Carefully observe the mounting conditions.

Recommended temperature profile when mounting infrared reflows is shown in the figure below.



5. Quality Assurance and Reliability

Sony's Policy of Quality Assurance

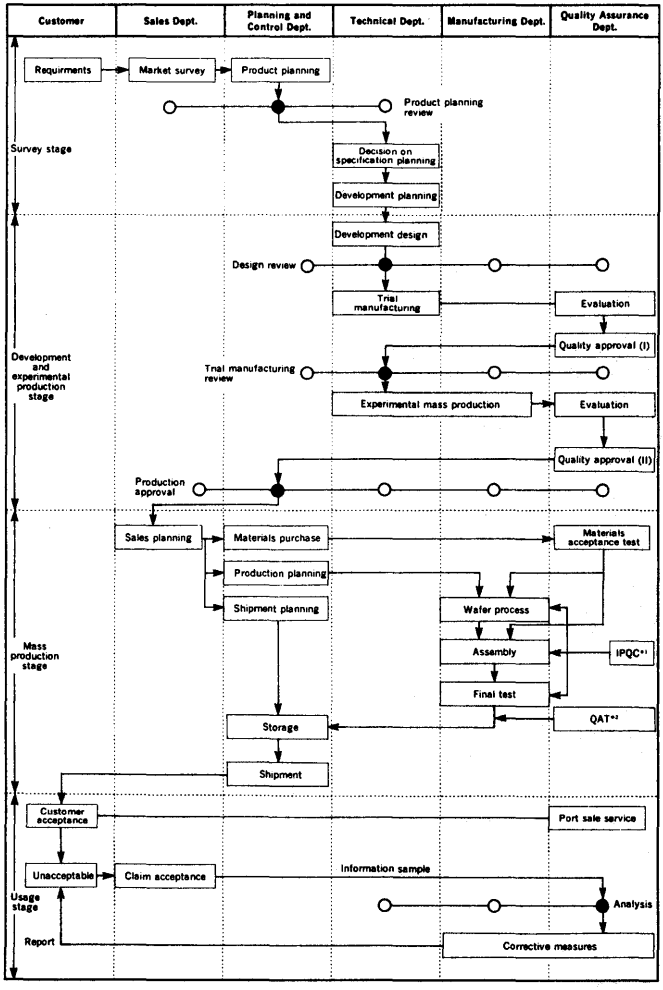
The Sony semiconductor embodies two fundamental ideas: "highest quality" and "lowest cost". These are the two key points for realizing such ideas.

One is the "quality" of men fabricating the semiconductor devices. The reliability of these people is reflected in the Sony products. Accordingly, Sony is making a continuous effort to raise the "quality" of people capable of manufacturing and fabricating Sony semiconductor devices.

The other point is a source management system combined with the concept of thorough quality design. With this system, higher quality products can be steadily manufactured through automation of device design, process design, and the fabrication process.

Sony is making constant efforts to supply the most economical and most useful products of very high quality to users.

Quality assurance system of semiconductor products



*1. IPQC: In Process Quality Control
*2. QAT: Quality Assurance Test

Quality assurance criteria and reliability test criteria

1) Quality assurance in shipping

Establishing quality in the design and in fabrication is essential to keep the quality and reliability levels of the semiconductor devices at a high level. This is done by the "Zero-defect" (ZD) movement. Further sampling checks, in units of shipping lot, is done on products that have been "totally-inspected" at the final fabrication stage, thus ensuring no detective items. This sampling inspection is done in accordance with MIL-STD-105D.

2) Reliability

The reliability test is done, periodically, to confirm reliability level.

Periodic Reliability Test

Item		Testing time	LTPD
Electrical Characteristics Test		In order to know the initial quality level, some types are selected and tested again.	
Life Test	high temperature operation	up to 1000 h	10%
	high temperature storage	up to 1000 h	10%
	low temperature storage	up to 1000 h	10%
	high temperature and high humidity storage	up to 1000 h	10%
	high temperature with bias	up to 1000 h	10%
	high temperature and high humidity with bias	up to 500 h	10%
	pressure cooker	up to 200 h	10%
Environmental Test	soldering heat resistance	10s	15%
	heat cycle	10 cycles	15%
Mechanical Test	solderability	Japan Industrial Standard (JIS)	15%
	length strength		15%
Other Tests	If necessary, tests are selected according to JIS C7021 C7022 and EIAJ SD121 IC121.		

*These tests are selected by sampling standard.

LTPD: Lot Tolerance Percent Defective

These tests and Inspection data are useful not only to improve design and wafer processes, but also serve to forecast reliability at the consumer level.

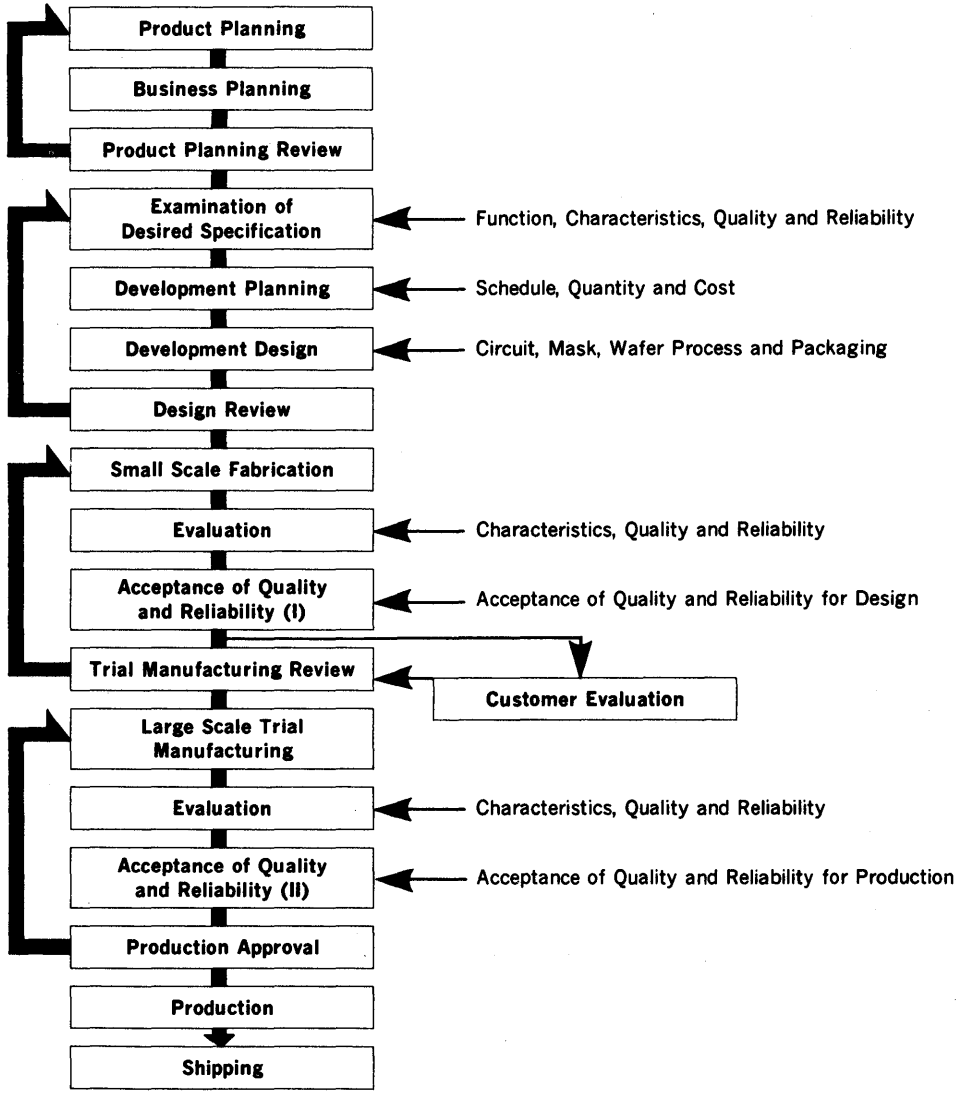
Reliability Test Standards for Acceptance of Products

Types of test	Condition	Supply voltages	Testing time	LTPD
High temperature operation	Ta=125°C, 150°C	Typical	1000h	5%
High temperature with bias	Ta=125°C, 150°C	Typical	1000h	5%
High temperature storage	Ta=150°C		1000h	5%
Low temperature storage	Ta=−65°C		1000h	5%
High temperature and high humidity storage	Ta=85°C 85%RH		1000h	5%
High temperature and high humidity with bias	Ta=85°C 85%RH	Typical (1h on/3h off)	1000h	5%
Pressure cooker	Ta=121°C 100%RH 30 pounds per square inch		200h	5%
Temperature cycle	Ta=−65°C to+150°C		100c	10%
Heat shock	Ta=−65°C to+150°C		5c	10%
Soldering heat resistance	T solder=260°C		10s	10%
Solderability	T solder=230°C (rosin type flux)		5s	10%
Mechanical shock	X, Y, Z 1500G Half part of sinusoidal wave of 0.5ms		3times for each direction	10%
Vibration	X, Y, G 20G 10Hz to 2000Hz to 10Hz (4min) Sinusoidal wave vibration		16minutes for each direction	10%
Constant acceleration	X, Y, Z 20,000G Centrifugal acceleration		1minute for each direction	10%
Free fall	Free fall from the height of 75cm to maple plate		3times	10%
Lead strength (bend) (pull)	based on JIS			10%
Electrostatic strength	Device must be designed again, when electrostatic strength below standard supplying surge voltage to each pin under the condition of C=200pF and Rs=0Ω.			

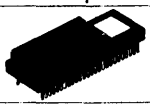
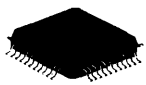
LTPD: Lot Tolerance Percent Defective

Flow Chart from Development to Manufacturing

Sony attains high quality and high reliability of semiconductor products by designing devices with quality and reliability from the initial steps of development and evaluating them sufficiently in each step of the development.

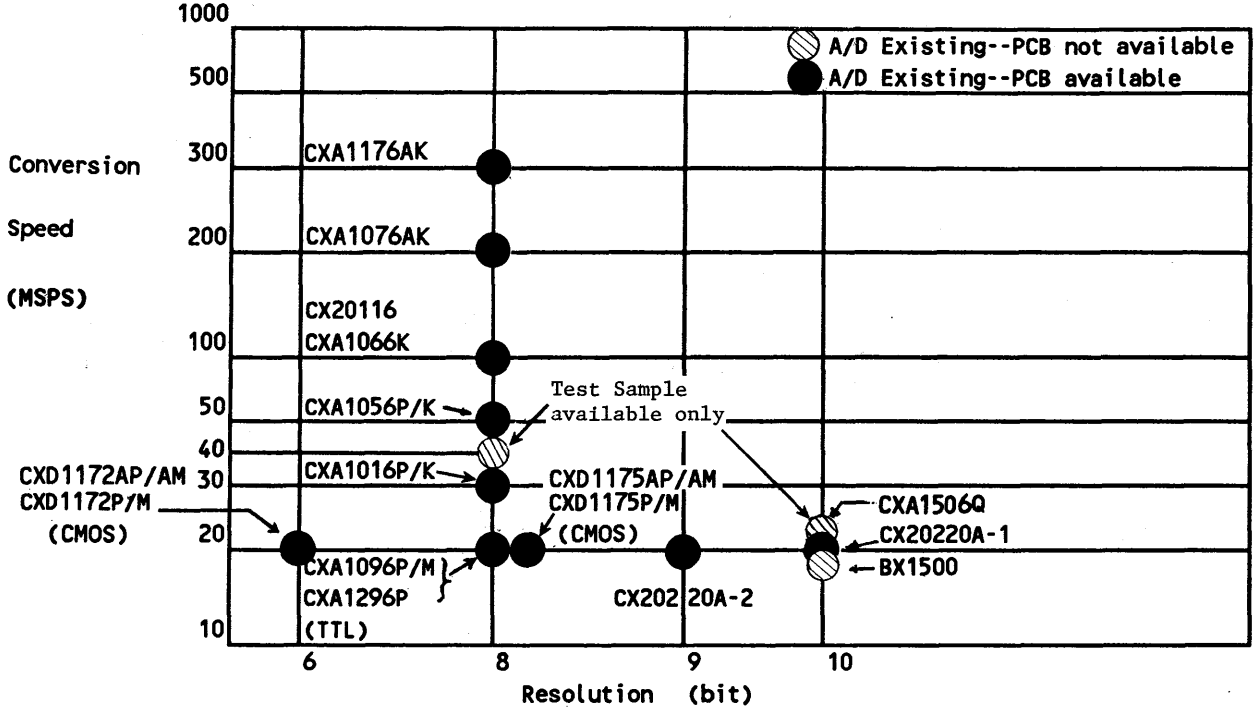


Sony Package Product Name

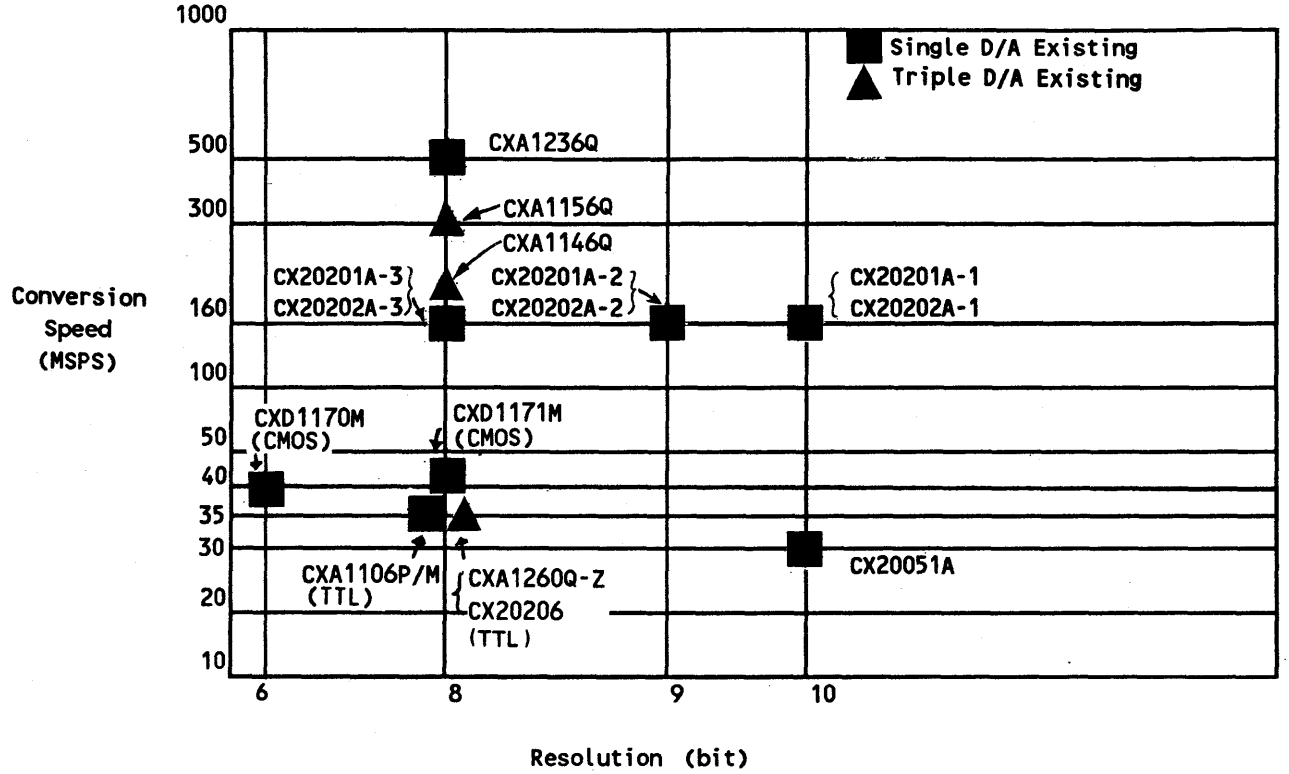
Type		Package name		Package	Features			
		Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction
Inserted	Standard	DIP	DUAL IN LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		SIP	SINGLE IN LINE PACKAGE		P	2.54mm (100MIL)	Through Hole Lead	1-direction
		ZIP	ZIG ZAG IN LINE PACKAGE		P	2.54mm (100MIL) Zig Zag inline	Through Hole Lead	1-direction
		PGA	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	4-direction
		PIGGY BACK	PIGGY BACK		C	2.54mm (100MIL)	Through Hole Lead	2-direction
	Shrink	SDIP	SHRINK DUAL IN LINE PACKAGE		P	1.778mm (70MIL)	Through Hole Lead	2-direction
Surface mounted	Standard flat package	QFP	QUAD FLAT PACKAGE		P	1.0mm 0.8mm	Gull-Wing	4-direction
		SOP	SMALL OUTLINE PACKAGE		P	1.27mm (50MIL)	Gull-Wing	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE		P	0.5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE		P	0.65mm	Gull Wing	2-direction
	Standard chip carrier	PLCC	PLASTIC LEADED CHIP CARRIER		P	1.27mm (50MIL)	J-bend	4-direction
		LCC	LEAD LESS CHIP CARRIER		C	1.27mm (50MIL)	Lead less	Package side
	Shrink chip carrier	SPLCC (PLCC)	SHRINK PLASTIC LEADED CHIP CARRIER		P	1.27mm Max. (50MIL Max.)	J-bend	4-direction
	Standard 2-direction chip carrier	SOJ	SMALL OUTLINE J-LEAD PACKAGE		P	1.27mm (50MIL)	J-bend	2-direction

*P·····Plastic, C·····Ceramic

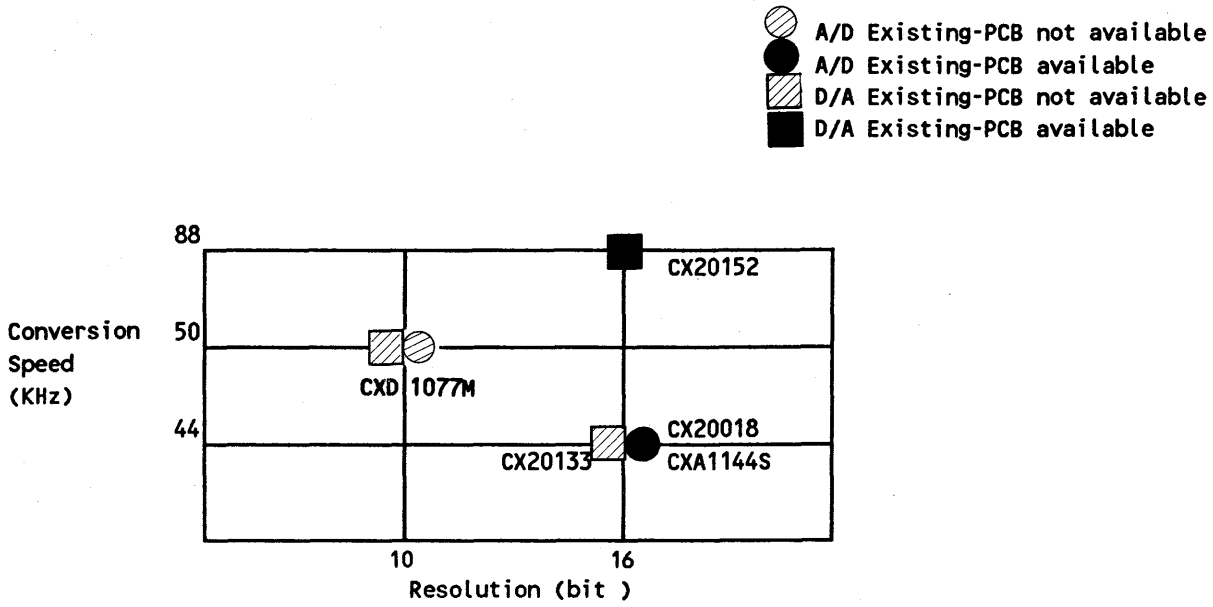
High Speed A/D Converters Line-Up



High Speed D/A Converters Line-Up



High Resolution A/D, D/A Converters Line-Up



High Speed A/D Converter

Type	Package	Function	Power Diss. (mW)	Input B.W (-3dB) (MHz)	Evaluation Board Availablity
CXD1172M	16P SOP	6-bit, 20MHz, CMOS	60	14(-1dB)	No
CXD1172P	16P DIP	6-bit, 20MHz, CMOS	60	14(-1dB)	Yes (CXD1172P/CXA1106PPCB)
CXD1172AM	16P SOP	6-bit, 20MHz, CMOS	40	20(-1dB)	No
CXD1172AP	16P DIP	6-bit, 20MHz, CMOS	40	20(-1dB)	Yes (CXD1172AP/CXA1106PPCB)
CXD1175M	24P SOP	8-bit, 20MHz, CMOS	100	14(-1dB)	No
CXD1175P	24P DIP	8-bit, 20MHz, CMOS	100	14(-1dB)	Yes (CXD1175P/CXA1106PPCB)
CXD1175AM	24P SOP	8-bit, 20MHz, CMOS	70	20(-1dB)	No
CXD1175AP	24P DIP	8-bit, 20MHz, CMOS	70	20(-1dB)	Yes (CXD1175AP/CXA1106PPCB)
CXA1096M	28P SOP	8-bit, 20MHz, TTL	390	8	No
CXA1096P	28P DIP	8-bit, 20MHz, TTL	390	8	Yes (CXA1096PPCB)
CXA1296P	28P DIP	8-bit, 20MHz, TTL	400	8	Yes (CXA1296PPCB)
CXA1016P	28P DIP	8-bit, 30MHz	440	30	Yes (CXA1016PPCB)
CXA1016K	44P LCC	8-bit, 30MHz	440	30	Yes (CXA1016KPCB)
CXA1056P	28P DIP	8-bit, 50MHz	550	50	Yes (CXA1056PPCB)
CXA1056K	44P LCC	8-bit, 50MHz	550	50	Yes (CXA1056KPCB)
CX20116	42P DIP	8-bit, 110MHz	1200	90	Yes (CX20116PCB)
CXA1066K	68P LCC	8-bit, 110MHz	1200	90	Yes (CXA1066KPCB)
CXA1076AK	68P LCC	8-bit, 200MHz	1450	220	Yes (CXA1076AKPCB)
CXA1176AK	68P LCC	8-bit, 300MHz	1450	250	Yes (CXA1176AKPCB)
CX20220A-1	28P DIP	10-bit, 20MHz	360	10	Yes (FCX20220A-1)
CX20220A-2	28P DIP	9-bit, 20MHz	360	10	Yes (FCX20220A-2)
BX-1500	34P DIP	10-bit, 18MHz (Hybrid IC)	1380	9	No

HIGH SPEED D/A CONVERTER

D/A Converter

Type	Package	Function	Power Diss. (mW)	Settling Time	Eval. Board Availability
*CXD1170M	24P SOP	6-bit, 40MHz, CMOS	70	TBD	No
*CXD1171M	24P SOP	8-bit, 40MHz, CMOS	70	TBD	No
CXA1106P	24P DIP	8-bit, 35MHz, TTL	200, Vcc=5V	16ns, 0.2%FS	No
CXA1106M	24P SOP	8-bit, 35MHz, TTL	200, Vcc=5V	16ns, 0.2%FS	No
CX20051A	28P DIP	10-bit, 30MHz	550	14ns, 0.05%FS	No
CX20201A-1	28P SOP	10-bit, 160MHz	390	5.2ns, 0.05%FS	No
CX20201A-2	28P SOP	9-bit, 160MHz	390	4.7ns, 0.1%FS	No
CX20201A-3	28P SOP	8-bit, 160MHz	390	4.3ns, 0.2%FS	No
CX20202A-1	28P DIP	10-bit, 160MHz	430	5.2ns, 0.05%FS	No
CX20202A-2	28P DIP	9-bit, 160MHz	430	4.7ns, 0.1%FS	No
CX20202A-3	28P DIP	8-bit, 160MHz	430	4.3ns, 0.2%FS	No
CX20206	42P SDIP	8-bit, 35MHz, Triple D/A, TTL	360	16ns, 0.2%FS	No
CXA1260Q-Z	48P QFP	8-bit, 35MHz, Triple D/A, TTL	360	16ns, 0.2%FS	No

Single VIDEO DAC

Type	Package	Function	Power Diss. (mW)	Settling Time	Eval. Board Availability
**CXA1236Q	44P QFP	8-bit, 500 MHz, Single VIDEO DAC	930	(1.5nS) (0.2%FS)	TBA

Triple VIDEO DAC

***CXA1146Q	44P QFP	8-bit, 160MHz, Triple VIDEO DAC	1040	(5.0ns) (0.2%FS)	TBA
***CXA1156Q	44P QFP	8-bit, 300MHz, Triple VIDEO DAC	1560	(2.5ns) (0.2%FS)	TBA

HIGH SPEED SAMPLE/HOLD IC

Type	Package	Function	Evaluation Board Availablity
CXA1008P	24P DIP	0.08% precision, 35MHz sample/hold	Yes (CX20052APCB-3A)
CXA1009P	24P DIP	0.08% precision, 18MHz sample/hold	Yes (CX20052APCB-3B)

HIGH RESOLUTION A/D, D/A CONVERTER (FOR AUDIO)

Type	Package	Function	Conv. Time (MIN) (us)	Evaluation Board Availablity
CX20018	28P DIP	2-Channel 16-bit resolution, 44KHz A/D Converter	9	Yes (CX20018PCB)
CXA1144S	28P SDIP	2-Channel 16-bit resolution, 44KHz A/D Converter	9	No
CX20133	28P SOP	2-Channel 16-bit resolution, 44KHz D/A Converter	9	No
CX20152	28P DIP	2-Channel 16-bit resolution, 88KHz D/A Converter	5	Yes (CX20152PCB)
CXD1077M	28P SOP	2-Channel 10-bit resolution, 50KHz A/D, D/A Converter	8	No

* Test sample available estimated 1Q/90
** Available 4Q/89
*** Test sample available now.

Digital Filters Line-Up

8Times Sampling

P/N		CXD1144BP	CXD1244S	CXD2550P	CXD2551P	CXD2551M
Package		28P DIP	40P SDIP *	18P DIP	18P DIP	24P SOP
No. of channels		2	2	2		
Filter Order		293	213	57		
Filter Characteristics	Ripple	0.00001dB	0.00001dB	0.05dB		
	Attenuation	120dB	100dB	40dB		
Data Output Resolution		16/18bit	16/18bit	16bit		
Data Output Format		Serial	Serial	Serial		
Other Features		4Fs/8Fs Soft Muting	4Fs/8Fs Soft Muting Noise Shaver Deemphasis	4Fs/8Fs Soft Muting Digital Attenuater Deemphasis (*)		

(*) Difference between CXD2250P & CXD2251M/P

CXD2550P	CXD2551M/P
No digital offset	Digital offset built-in
Muting ON when power turns on	Muting OFF when power turns on

4Times Sampling

P/N		CXD1162P	CXD1088AQ
Package		22P DIP	44P QFP
No. of channels		2	2
Filter Order		83+21	83+21
Filter Characteristics	Ripple	0.0001dB	0.0001dB
	Attenuation	80dB	80dB
Data Output Resolution		16bit	16/18bit
Data Output Format		Serial	Serial/Parallel
Other Features		Soft Muting	Soft Muting

* SDIP=Shrink DIP
** QFP=Quad Flat Package (Gull-wing Type)

High Speed A/D Converters

3

1. High Speed A/D Converters

(A): Advanced Information
(P): Preliminary

Type	Function	Page
CX20116 CXA1066K	8-bit 110MSPS Flash A/D Converter	33
CX20220A-1/-2	10/9-bit 20MSPS Sub-ranging A/D Converter (ECL I/O)	41
CXA1016P/K CXA1056P/K	8-bit 30/50MSPS Flash A/D Converter	53
CXA1076K CXA1176K	8-bit 200/300MSPS Flash A/D Converter	64
CXA1076AK CXA1176AK	8-bit 200/300MSPS Flash A/D Converter (A)	65
CXA1096M	8-bit 20MSPS Flash A/D Converter (TTL I/O)	81
CXA1096P	8-bit 20MSPS Flash A/D Converter (TTL I/O)	95
CXA1296P	8-bit 20MSPS Flash A/D Converter (TTL I/O)	108
CXD1172M/P	6-bit 20MSPS A/D Converter (CMOS)	123
CXD1172AM/AP	6-bit 20MSPS A/D Converter (CMOS) (P)	133
CXD1175M/P	8-bit 20MSPS A/D Converter (CMOS)	140
CXD1175AM/AP	8-bit 20MSPS A/D Converter (CMOS) (P)	152
CXD1176Q	8-bit 20MSPS A/D Converter with clamp circuit (CMOS) (A)	160
BX-1500	10-bit 18MSPS A/D Converter Module (ECL I/O)	162
Application Note CXA1016P/CXA1016K CXA1056P/CXA1056K CX20116/CXA1066K	8-bit High Speed A/D Converter	172

SONY CX20116/CXA1066K

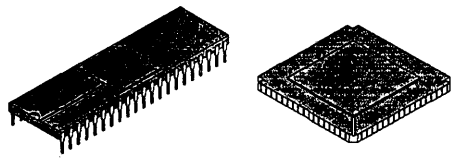
8 bit 110 MSPS Flash A/D Converter

Evaluation Board Available — CX20116PCB/CXA1066KPCB

Description

CX20116/CXA1066K are the 8 bit ultra high speed A/D Converter IC capable of digitizing analog signals at rates from DC to 110 MSPS. These A/Ds can be utilized in many varied applications. A wide analog input band width satisfies the characteristics for high definition television systems.

42 pin DIP (Ceramic) 68 pin LCC (Ceramic)



Features

- Resolution at 8 bit ±½ LSB
- Ultla high speed operation with maximum conversion rate of 110 MSPS
- Full scale input band width of: 60 MHz (−1dB)
  90 MHz (−3dB)
- Low input capacitance at 35 pF (Typ.)
- Low power consumption at 1.2W (Typ.)

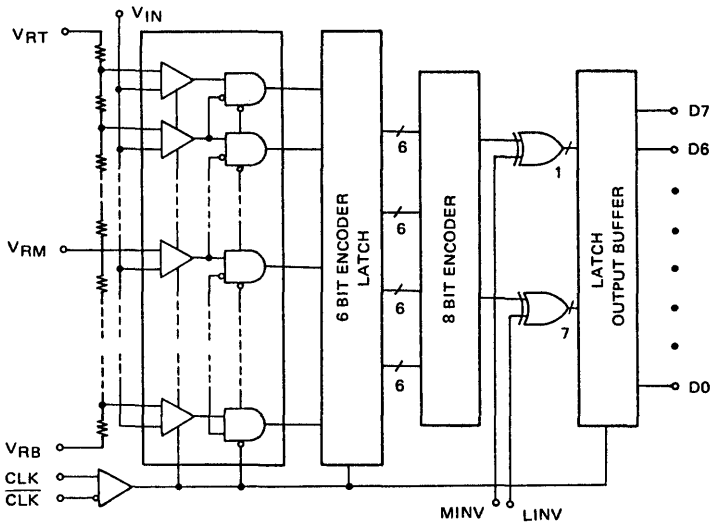
Structure

Bipolar silicon monolithic IC

Applications

- High speed signal processing
- High definition video system

Block Diagram



E89636-ST

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{EE}		0 to −7	V
• Analog input voltage	V_{IN}		0.5 to V_{EE}	V
• Reference input voltage	V_{RT}, V_{RB}, V_{RM}		0.5 to V_{EE}	V
	$\lvert V_{RT}-V_{RB}\rvert$		2.5	V
• Digital input voltage	CLK, $\overline{CLK}$, MINV, LINV		0.5 to −4	V
• V_{RM} pin input current	IVRM		−3 to +3	mA
• Digital output current	I_{D0} to I_{D7}		0 to −10	mA
• Operating temperature	Ta	CX20116	−25 to +100	°C
	Tc	CXA1066K	−25 to +125	°C*1
• Storage temperature	Tstg		−55 to +150	°C
• Allowable power dissipation	P_D	CX20116	3.1	W
		CXA1066K	2.3	W

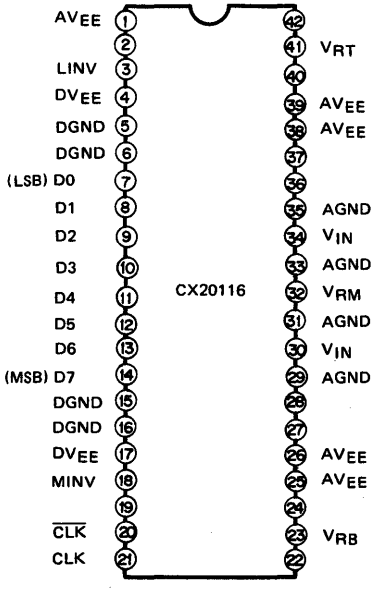
*1 Heat sinking is required above 54°C ambient.

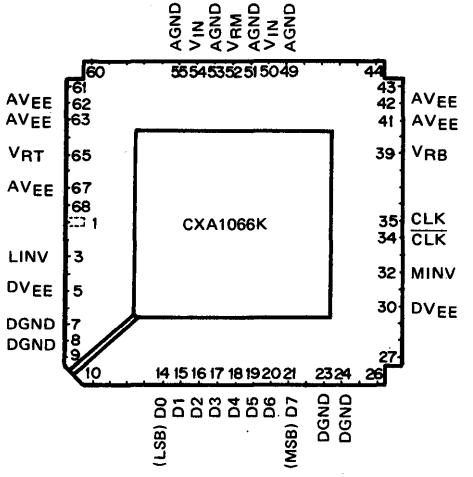
Recommended Operating Conditions

		Min	Typ.	Max.	Unit.
• Supply voltage	AV_{EE}, DV_{EE}	−5.7	−5.2	−5.0	V
	AV_{EE}—DV_{EE}	−0.05	0	0.05	V
	AGND—DGND	−0.05	0	0.05	V
• Reference input voltege	V_{RT}	−0.1	0	0.1	V
	V_{RB}	−2.2	−2	−1.8	V
• Analog input voltage	V_{IN}	V_{RB}		V_{RT}	
• Clock pulse width	Tpw1	8.0			ns
	Tpw0	1.0			ns

Pin Configuration (Top View)

The pin numbers without indication are empty pins. (not connected)





Pin Description

No.		Symbol	Function
CX20116	CXA1066K		
1, 25, 26, 38, 39	41, 42, 62, 63, 67	AV_{EE}	Analog V_{EE}, −5.2V (Typ.). Coupled with about 6Ω between DV_{EE}.
3	3	LINV	Input pin for output polarity inversion of D_0 (LSB) to D_6. (See the Code Table)
4, 17	5, 30	DV_{EE}	Digital V_{EE}, −5.2V (Typ.).
5, 6, 15, 16	7, 8, 23, 24	DGND	Digital GND, which is separated from the Analog GND.
7 to 14	14 to 21	D_0 to D_7	Digital data output pin, ECL level. D_0: LSB to D_7: MSB. Pull-down resistors are necessary externally.
18	32	MINV	Input pin for output polarity inversion of D_7 (MSB) (See the Code Table). ECL level. "0" level is held when it is released.
20	34	$\overline{CLK}$	Inverse clock input pin, ECL level.
21	35	CLK	Clock input pin, ECL level.
23	39	V_{RB}	Reference voltage (bottom), −2V (Typ.).
29, 31, 33,35	49, 51, 53, 55	AGND	Analog GND
30, 34	50, 54	V_{IN}	Analog input, input voltage range is V_{RT} to V_{RB}
32	52	V_{RM}	Middle point of the reference voltage, it can be used as a linearity correction pin.
41	65	V_{RT}	Reference voltage (Top), 0V (Typ.).
2, 19, 22, 24, 27, 28, 36, 37, 40, 42	1, 2, 4, 6, 9 to 13, 22, 25 to 29, 31, 33, 36 to 38, 40, 43 to 48 56 to 61, 64, 66, 68		Empty pins (not connected), 2 and 19 are used to be grounded to DGND, the others are used to be grounded to AGND.

Output Coding

	MINV	0	0	1	1
	LINV	0	1	0	1
	0V	111...11	100...00	011...11	000...00
	.	111...10	100...01	011...10	000...01
	.	.	.	.	.
	.	.	.	.	.
	.	.	.	.	.
V_{IN}	.	100...00	111...11	000...00	011...11
	.	011...11	000...00	111...11	100...00
	.	.	.	.	.
	.	.	.	.	.
	.	.	.	.	.
	.	000...01	011...10	100...01	111...10
	−2V	000...00	011...11	100...00	111...11

1: V_{IH}, V_{OH}
0: V_{IL}, V_{OL}

Electrical Characteristics

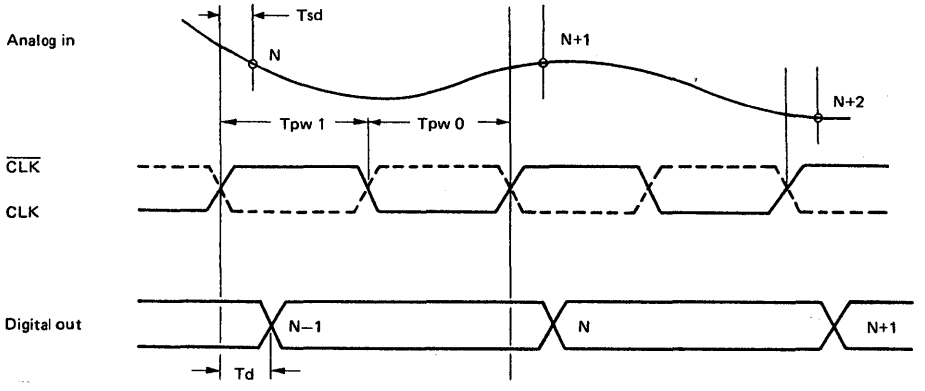
(Ta=25°C, V_{EE}=−5.2V, V_{RT}=0V, V_{RB}=−2V)

Item		Symbol	Test Condition	Min.	Typ.	Max.	Unit
Maximum conversion rate		Fc	V_{IN}=0 to −2V, fin=1 kHz, ramp	110			MSPS
Supply current		I_{EE}		−180	−220	−260	mA
Analog input capacitance		C_{IN}	V_{IN}=−1V+0.07 Vrms		35	40	pF
Analog input bias current		I_{IN}	V_{IN}=−1V		150	220	μA
Reference resistor		Rr (V_{RT} to V_{RB})		70	80	100	Ω
Offset voltage	V_{RT}			14	17	20	mV
	V_{RB}			6	9	12	mV
Digital input voltage		V_{IH}		−1.0	−0.9	−0.7	V
		V_{IL}		−1.9	−1.75	−1.6	V
Digital input current		I_{IH}	V_{IH}=−0.9V	0		0.4	mA
		I_{IL}	V_{IL}=−1.75V	−0.05		0.35	mA
Digital output voltage		V_{OH}	R_L=620Ω to V_{EE}	−1.0			V
		V_{OL}				−1.6	V
Output data delay		Td	R_L=620Ω to V_{EE}	3.0	3.5	4.2	ns
Non-linearity error			Fc=110 MSPS			±½	LSB
Differential non-linearity error			Fc = 110 MSPS			±½	LSB
Differential gain		DG	NTSC 40 IRE mod. ramp, Fc=110 MSPS			1.5	%
Differential phase		DP				0.5	deg.
Aperture jitter		Taj			15		ps
Sampling delay		Tsd		1.9	2.2	2.5	ns
Full scale input BW(− 3dB)		BW_F	*1		90		MHz

*1 Source impedance = 50 ohm
Without a buffer amplifier driving A/D input

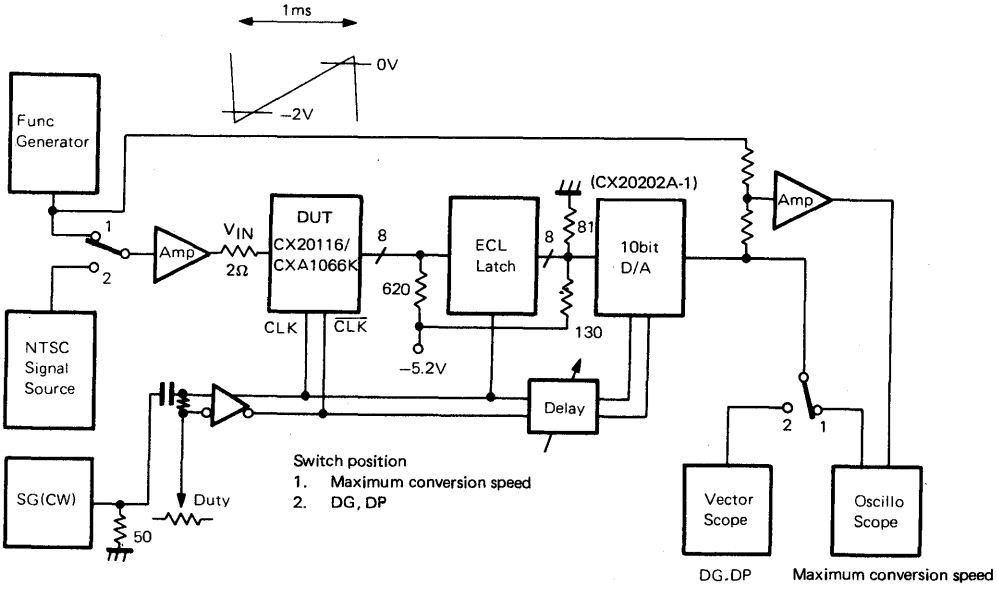
Timing Chart

*See page 34 for Tpwl and Tpw0.

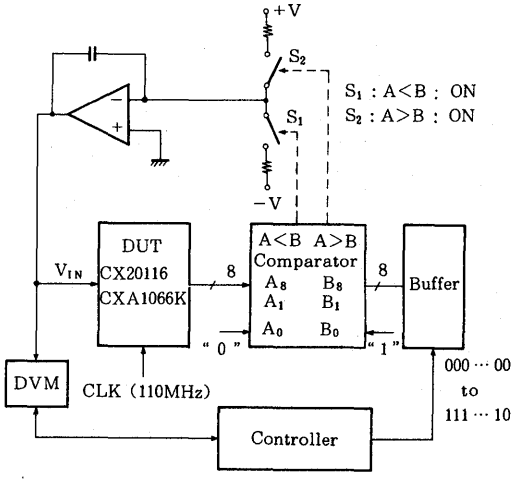


Electrical Characteristics Test Circuit

Maximum conversion speed test circuit
Differential gain error test circuit
Differential phase error test circuit

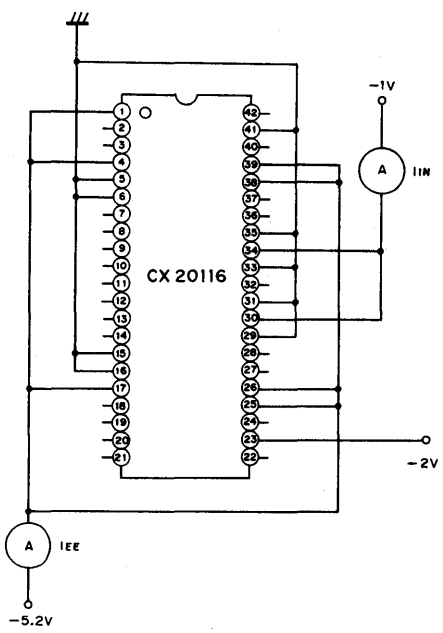


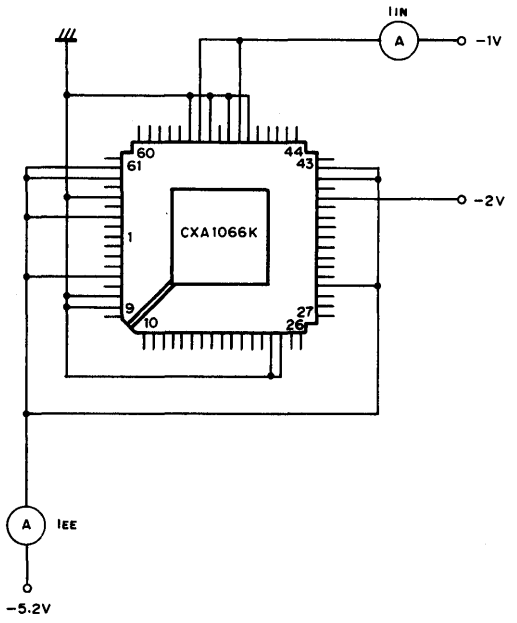
Differential Non-linearity Test Circuit
Integral Non-linearity Test Circuit



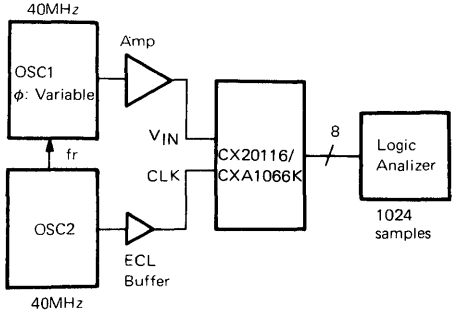
Power Supply Current Test Circuit

Analog input bias current test circuit

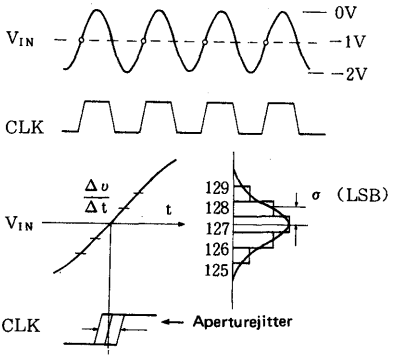




Sampling Delay Test Circuit
Aperture jitter test circuit



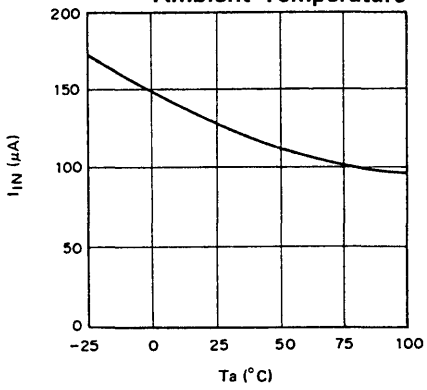
Aperture jitter test method



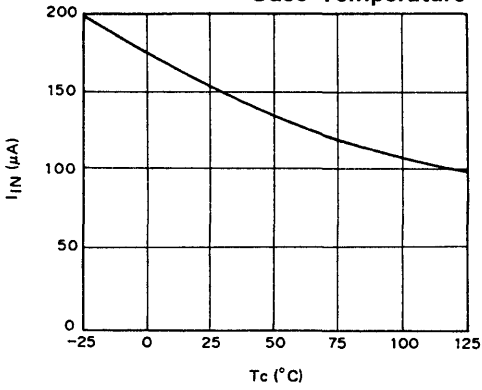
If the output distribution code is σ (LSB), when the maximum slew mate point is sampled at the analog input signal and the equivalent frequency clock, the aperture jitter Taj becomes:

$$Taj = \sigma / \frac{\Delta v}{\Delta t} = \sigma / (\frac{256}{2} \times 2\pi f)$$

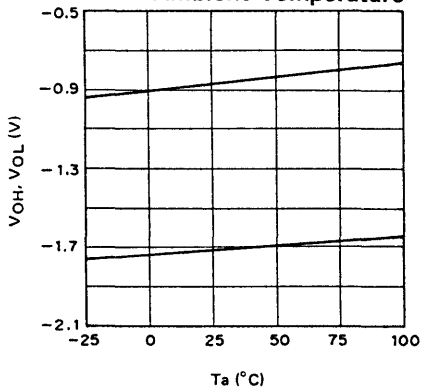
CX20116
Input Bias Current vs. Ambient Temperature



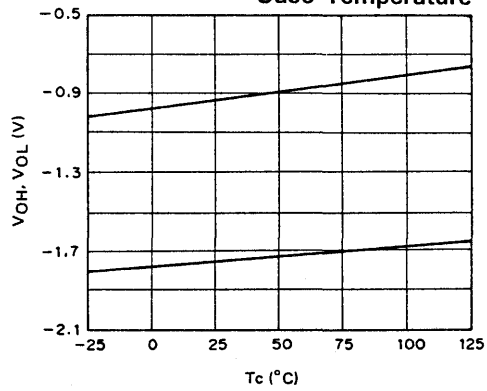
CXA1066K
Input Bias Current vs. Case Temperature



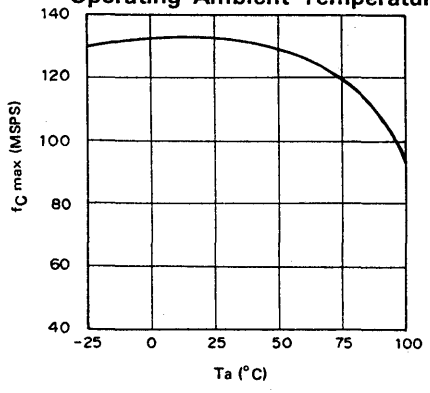
CX20116
Digital Output Voltage vs. Ambient Temperature



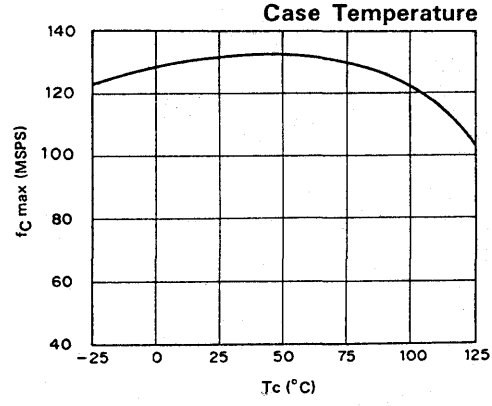
CXA1066K
Digital Output Voltage vs. Case Temperature



CX20116
Maximum Conversion Rate vs. Operating Ambient Temperature

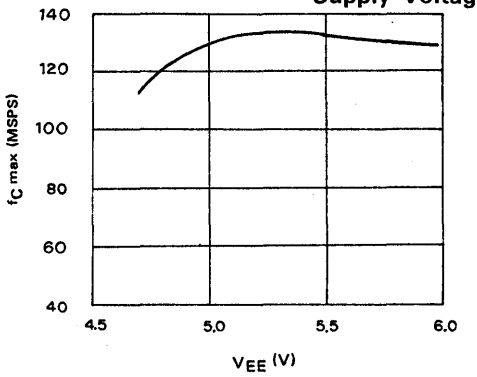


CXA1066K
Maximum Conversion Rate vs. Case Temperature



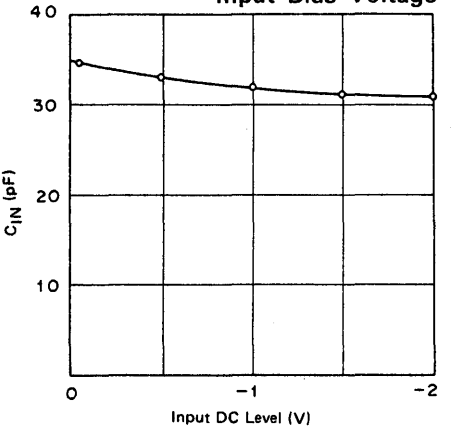
CX20116/CXA1066K

Maximum Conversion Frequency vs. Supply Voltage

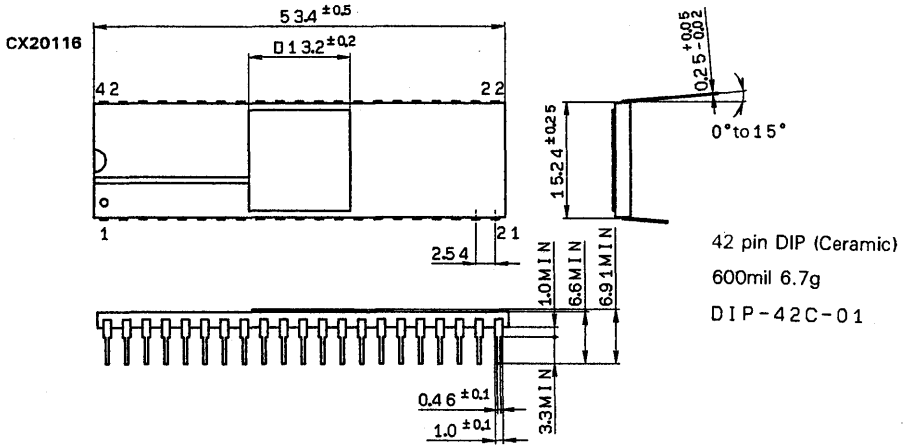


CX20116/CXA1066K

Analog Input Capacitance vs. Input Bias Voltage



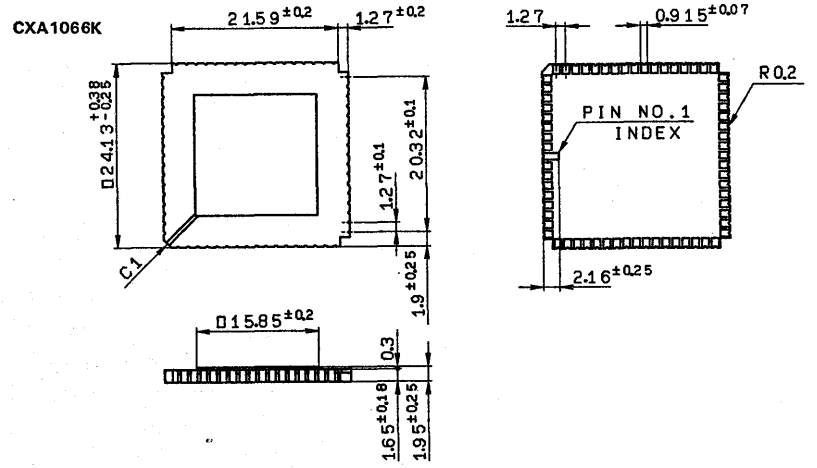
Package Outline **Unit: mm**



42 pin DIP (Ceramic)

600mil 6.7g

DIP-42C-01



SONY CX20220A-1/-2

10/9Bit 20MSPS Sub-ranging A/D Converter

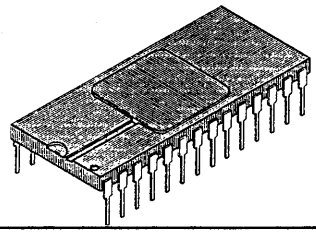
Evaluation Board Available — FCX20220A-1
FCX20220A-2

Description

CX20220A series is a high-speed, 20MSPS A/D converter which comes in two types of resolution, 10-bit and 9-bit, that are distinguished by the number suffixed to the name. Since a series-parallel system is used, an external sample hold circuit is required.

- Resolution: 10 bits (CX20220A-1)
  9 bits (CX20220A-2)
- Maximum conversion rate: 20MSPS
- Digitizing range: 0 to −2V
- Digital input/output: ECL level
- Output code: binary
- Low power consumption: 360 mW

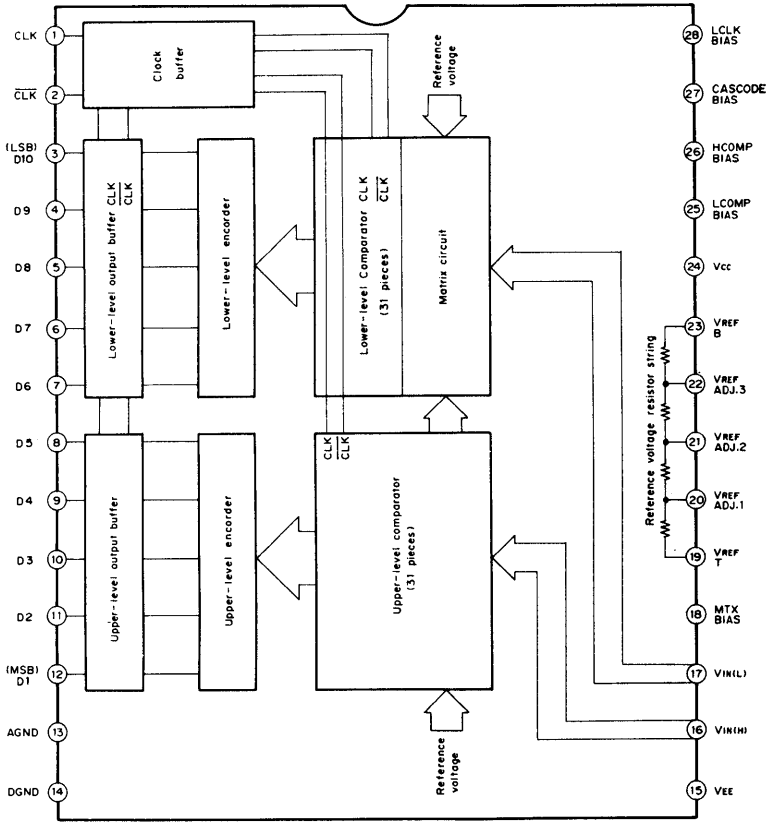
28pin DIP (Ceramic)



Structure

Bipolar silicon monolithic IC

Block Diagram and Pin Configuration (Top View)



E89639-HP

Absolute Maximum Ratings (Ta = 25°C)

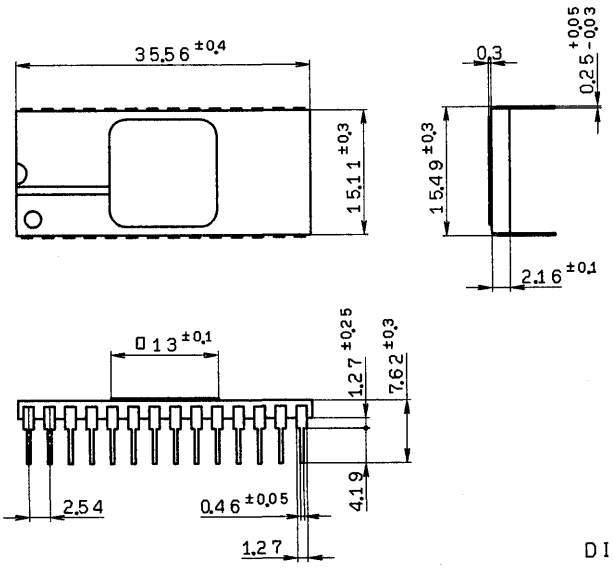
• Supply voltage	V_{CC}	2.5	V
	V_{EE}	−7	V
• Analog voltage	V_I	V_{EE} to 0.3	V
• Clock input voltage	V_{CLK}, $V_{\overline{CLK}}$	V_{EE} to 0.3	V
• Reference voltage	V_{REF}	V_{EE} to 0.3	V
• Digital output current	I_{D01} to I_{D10}	0 to −20	mA
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	PD	1.23	W

Recommended Operating Conditions

• Supply voltage	V_{CC}	1.6 to 2.1	V
	V_{EE}	−5.25 to −4.75	V
	AGND-DGND	−0.05 to +0.05	V
• Reference voltage	$V_{REF.T}$	0	V
	$V_{REF.B}$	−2.0	V
• Analog input voltage	V_I	$V_{REF.B}$ to $V_{REF.T}$	V
• Clock input voltage	V_{IH}	−1.1 min.	V
	V_{IL}	−1.4 max.	V
• Clock pulse width	T_{PW1}	20 min.	ns
	T_{PW0}	28 min.	ns

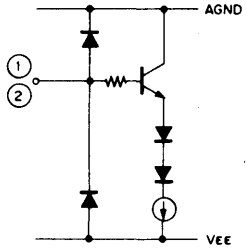
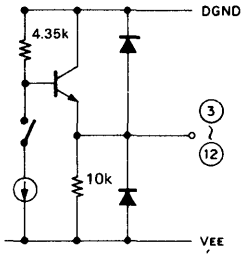
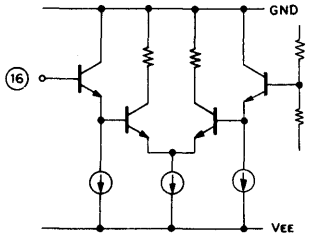
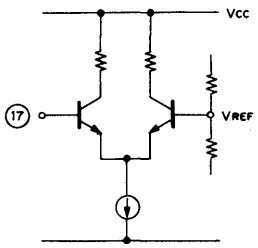
Package Outline Unit : mm

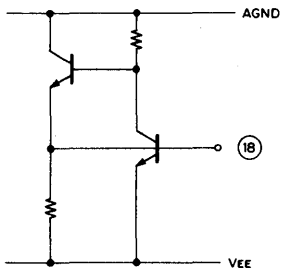
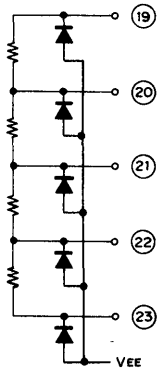
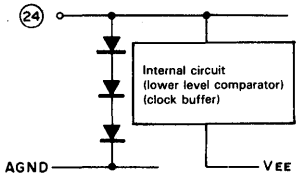
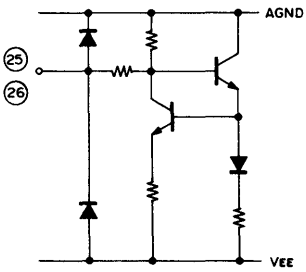
28pin DIP(Ceramic) 600mil 4.8g

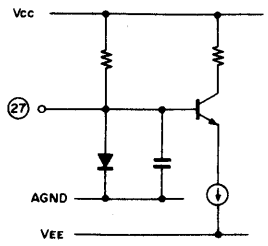
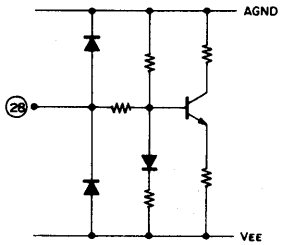


DIP-28C-01

Pin Description and Equivalent Circuit

No.	Symbol	Equivalent circuit	Description
1	CLK		Clock input pin, ECL level.
2	$\overline{\text{CLK}}$		Inverse clock input pin, ECL level
3	D10(LSB)		Digital output pin, ECL level, pull-down resistor (10KΩ) built in
4	D9		
5	D8		
6	D7		
7	D6		
8	D5		
9	D4		
10	D3		
11	D2		
12	D1(MSB)		
13	AGND		Analog ground pin
14	DGND		Digital ground pin
15	VEE		Power supply pin. To be grounded with ceramic chip capacitor of 0.1 μF or over.
16	VIN(H)		Analog input pin (Upper level)
17	VIN(L)		Analog input pin (Lower level)

No.	Symbol	Equivalent circuit	Description
18	MTX BIAS		Pin connected internal matrix, which is normally used open.
19	VREF.T		Reference voltage pin (top), 0 V (typ.)
20	VREF ADJ. 1		Reference voltage adjusting pin. To be grounded with ceramic chip capacitor of 0.1μF or over.
21	VREF ADJ. 2		
22	VREF ADJ. 3		
23	VREF.B		Reference voltage pin (bottom), −2 V (typ.) To be grounded with ceramic chip capacifor of 0.1μF or over.
24	VCC		Internal power supply pin. Three diodes are incorporated in series, so that by connecting pull-up resistor to +5 V
25	LCOMP BIAS		Pin connected internal lower level comparator, which is normally used open.
26	HCOMP BIAS		Pin connected internal upper level comparator which is normally used open.

No.	Symbol	Equivalent circuit	Description
27	CASCODE BIAS		Cascode bias pin. To be bypassed to GND with ceramic capacitor of 0.1μF or over.
28	LCLK BIAS	 LCLK BIAS HCLK BIAS	Pin connected internal lower level buffer, which is normally used open.

Electrical Characteristics (1) (See the Electrical Characteristics Test Circuit)

CX20220A-1 (10Bit) (Ta = 25°C, VCC = 1.6V, VEE = −5V)

Item	Symbol	SW Condition				Test point	Test condition	Min.	Typ.	Max.	Unit
		SW1	SW2	SW3	SW4						
Resolution	n								10		bit
Differential linearity error	E_D	A	A	A	D	Differential waveform output				±1	LSB
Integral linearity error	E_L	A	A	A	D	Differential waveform output				±1	LSB
Differential gain error	DG	A	A	A		DA output	SW4:NTSC 40IRE mod. ramp fc = 14.32 MHz nonlock		0.7		%
Differential phase error	DP	A	A	A		DA output			0.3		deg

CX20220A-2 (9Bit)

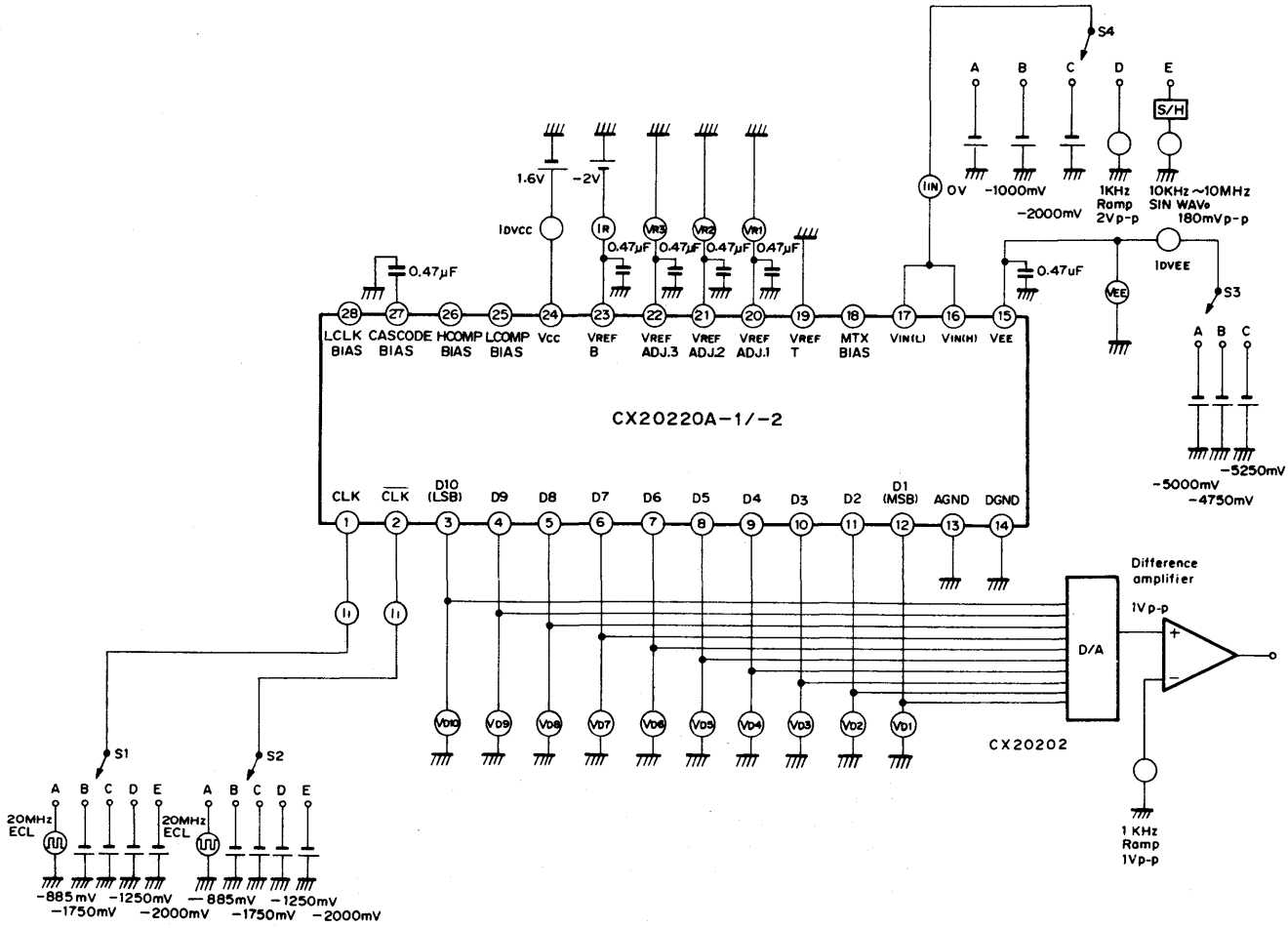
Item	Symbol	SW Condition				Test point	Test condition	Min.	Typ.	Max.	Unit
		SW1	SW2	SW3	SW4						
Resolution	n								9		bit
Differential linearity error	E_D	A	A	A	D	Differential waveform output				±1	LSB
Integral linearity error	E_L	A	A	A	D	Differential waveform output				±1/2	LSB
Differential gain error	DG	A	A	A		DA output	SW4:NTSC 40IRE mod. ramp fc = 14.32 MHz nonlock		1.0		%
Differential phase error	DP	A	A	A		DA output			0.5		deg

Electrical Characteristics (2) (See the Electrical Characteristics Test Circuit)

(Ta = 25°C, V_{CC} = 1.6V, V_{EE} = −5V)

Item	Symbol	SW Condition				Test point	Test condition	Min.	Typ.	Max.	Unit
		SW1	SW2	SW3	SW4						
Conversion rate	f_{max}	A	A	A	D	DA output		20			MSPS
Power consumption(1)	I_{DVCC}	B	D	A	A	I_{DVCC}			17	25	mA
Power consumption(2)	I_{DVEE}	B	D	A	A	I_{DVEE}		−80	−60		mA
Resistor string current	I_{REF}	B	D	A	A	I_R		−14	−12.5		mA
Resistor string pin voltage (1)	V_{R1}	B	D	A	A	V_{RI}		−0.51	−0.5	−0.49	V
Resistor string pin voltage (2)	V_{R2}	B	D	A	A	V_{R2}		−1.01	−1.0	−0.99	V
Resistor string pin voltage (3)	V_{R3}	B	D	A	A	V_{R3}		−1.51	−1.5	−1.49	V
Offset voltage, V_{RT} side	E_{OT}	B	C	A	A				2		mV
Offset voltage, V_{RB} side	E_{OB}	B	C	A	A				4		mV
Analog input current	I_{IN}	B	D	A	A	I_{IN}			40	80	μA
Analog input capacity (1)	C_{IN}	A	A	A			SW4: V_{IN} = 0V + 0.07 Vrms 4 MHz		230		pF
Analog input capacity (2)	C_{IN}	A	A	A			V_{IN} = −2V + 0.07 Vrms 4 MHz		190		pF
Analog input bandwidth	BW	A	A	A	E	DA output	Measurement of output amplitude		10		MHz
Digital input current (1)	I_{IH}	B	C	A	A	I_I			5	8	μA
Digital input current (2)	I_{IL}	E	D	A	A	I_I			5	8	μA
Inverse digital input current (1)	I_{IH}	C	B	A	A	I_I			5	8	μA
Inverse digital input current (2)	I_{IL}	D	E	A	A	I_I			5	8	μA
Digital output voltage, H level (1)	V_{IL}	A	D	A	A	V_{D1} to V_{D10}	Do not connect pull-down resistor.	−0.9	−0.8		V
Digital output voltage, H level (2)	V_{OH}	A	D	A	A	V_{D1} to V_{D10}	Pull-down resistor is 1k Ω.		−1.0		V
Digital output voltage L level (1)	V_{OL}	A	D	A	A	V_{D1} to V_{D10}	Do not connect pull-down resistor		−1.6	−1.5	V
Digital output voltage, L level (2)	V_{OL}	A	D	A	A	V_{D1} to V_{D10}	Pull-down resistor is 1k Ω.		−1.9		V
Output data delay (1)	T_d	A	A	A	A	V_{D1} to V_{D10}	Do not connect pull-down resistor		10		ns
Output data delay (2)	T_d	A	A	A	A	V_{D1} to V_{D10}	Pull-down resistor is 1k Ω		5		ns

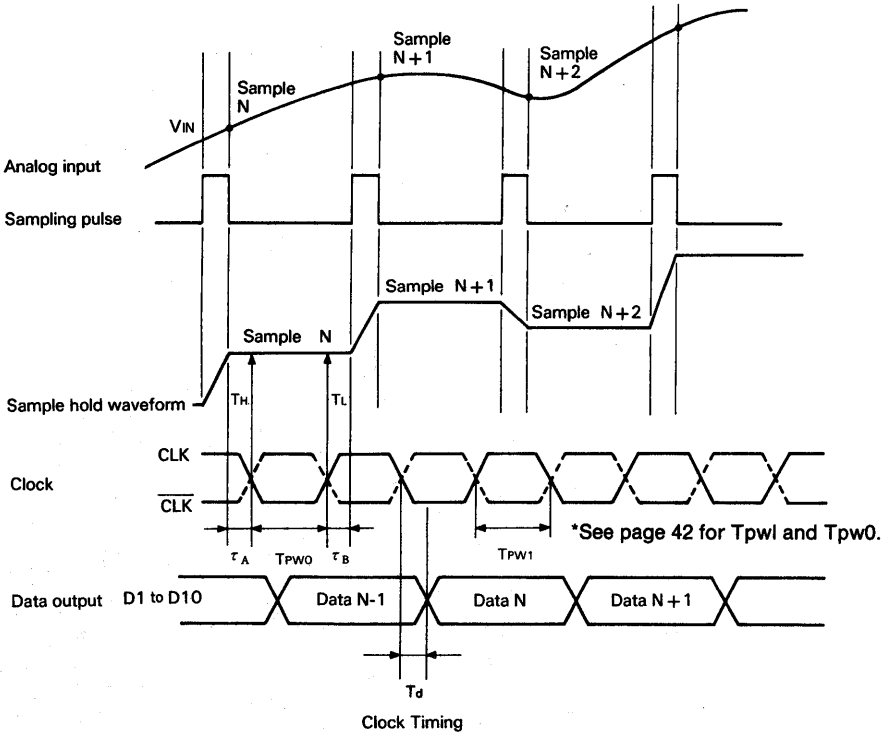
Electrical Characteristic Test Circuit



Reference Data for Standard Circuit Design

Clock Timing

CX20220A-1/-2 is a series-parallel-type A/D converter, and therefore an external sample and hold circuit is required. Careful timing, design should be made according to the timing chart shown below. The timing design between the S/H output and the A/D clock is important.



Clock Timing

$\tau_A \geqq T_A$ (Aperture time + settling time of sample and hold circuit)

$\tau_B \geqq 2ns$

$T_{PW0} \geqq 28ns$

$T_{PW1} \geqq 20ns$

TH is the timing in which the upper level comparator compares VIN and VREF and latches the result. TL is the timing in which the lower level comparator compares VIN and VREF and latches the result. The simple method is for output data to be latched upon rising edge of CLK. Clock duty should be chosen so that the D G and DP perform the best result.

Digital Output (CX20220A-1)

In the output stages (pins 3 through 12), a10kΩ pull-down resistors are built in. A 1kΩ or larger resistance can further be connected to it externally.

D1 = MSB, D10 = LSB.

The table below shows the relationship between analog input voltage and digital output code.

Input signal voltage	Step	Digital output code (binary) MSB LSB 1 2 3 4 5 6 8 8 9 10
$V_{REF.T}$	0	1 1 1 1 1 1 1 1 1 1
.	1	1 1 1 1 1 1 1 1 1 0
.	2	1 1 1 1 1 1 1 1 0 1
.	.	.
.	.	.
.	.	.
.	5 1 1	1 0 0 0 0 0 0 0 0 1
.	5 1 2	1 0 0 0 0 0 0 0 0 0
.	5 1 3	0 1 1 1 1 1 1 1 1 1
.	.	.
.	.	.
.	.	.
.	1 0 2 2	0 0 0 0 0 0 0 0 0 1
$V_{REF.B}$	1 0 2 3	0 0 0 0 0 0 0 0 0 0

1 : V_{OH}
0 : V_{OL}

Digital Output (CX20220A-2)

D1=MSB, D9=LSB.

The table below shows the relationship between analog input voltage and digital output code.

Input signal voltage	Step	Digital output code (binary) MSB LSB 1 2 3 4 5 6 8 8 9
$V_{REF.T}$	0	1 1 1 1 1 1 1 1 1
.	1	1 1 1 1 1 1 1 1 0
.	2	1 1 1 1 1 1 1 0 1
.	.	.
.	.	.
.	.	.
.	2 5 5	1 0 0 0 0 0 0 0 1
.	2 5 6	1 0 0 0 0 0 0 0 0
.	2 5 7	0 1 1 1 1 1 1 1 1
.	.	.
.	.	.
.	.	.
.	5 1 0	0 0 0 0 0 0 0 0 1
$V_{REF.B}$	5 1 1	0 0 0 0 0 0 0 0 0

1 : V_{OH}
0 : V_{OL}

Ground Pin (AGND, DGND)

When mounting the converter on a printed circuit board, take as much space as possible for GND, to reduce impedance and resistance.

Power Supply Pin (VEE)

The VEE pin should be bypassed in the shortest way to AGND with a 0.1μF or larger ceramic chip capacitor.

Power Supply Pin (Vcc)

This is an internal power supply pin. Three diodes are incorporated in it in series, as shown in the equivalent circuit diagram, and its lower end is connected to AGND. Therefore, any desired Vcc can be obtained by connecting a pull-up resistor to +5V. Be careful not to connect a capacitor between this pin and GND, because oscillation may result.

Reference Voltage Pin

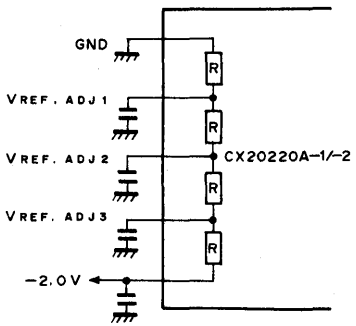
From this pin the reference voltage is supplied to the upper level and lower level comparators. Normally, VREF.T should be connected to GND, and VREF.B to −2.0V, respectively.

The interval between VREF.T and VREF.B constitutes a resistance of approximately 150 Ω, and upon application of −2.0V a current of approximately 13 mA will flow in it.

Any leakage of CLK to the reference voltage, will deteriorate the characteristics of the converter. To avoid this, it should be bypassed to AGND with a tantalum capacitor of 47 μF or over plus a ceramic chip capacitor of 0.1 μF or over.

Linearity Adjusting Pin (VREF.ADJ)

Adjusting pins are extended from reference resistors as shown below. Normally, these pins are connected to AGND with a 0.1μF or larger ceramic chip capacitor. When adjustments are needed, connect them to AGND or VREF.B via resistance.



Sample & Hold Circuit

As noted in the explanation of the clock timing, it is desirable that the sample and hold circuit has some allowance for TA. A sample and hold circuit based on a diode bridge switch maybe used which performs the best result.

For more information, see Application Circuit (2).

Analog Input

Since CX20220A-1/-2 has an analog input capacitance of approximately 230pF, the buffer amplifier used to drive it must have a sufficient drive capability. Note that, if driven by a low-output-impedance buffer amplifier, a parasitic oscillation may result. This can be prevented by inserting a resistor of about 10 to 30 Ω between the output of the buffer amplifier and the A/D input in series.

Clock Input

The clock input is a complementary configuration.
Normally it should be driven with ECL circuit with complementary output.

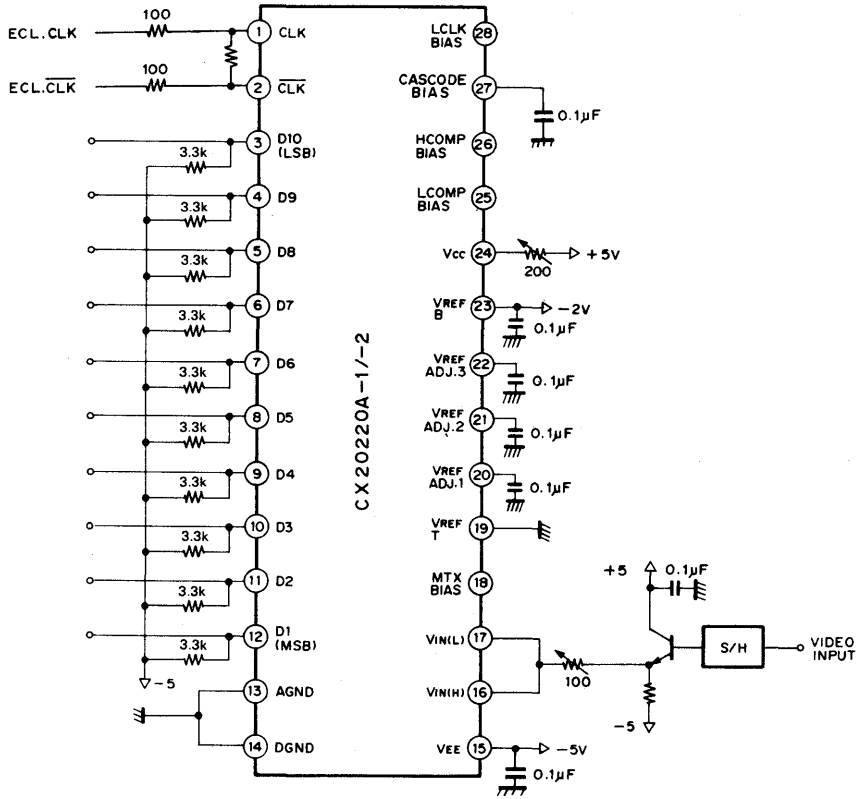
Digital Output (D1 through D10)

Although a 10kΩ pull-down resistor is built into the digital output stage, a 1kΩ or larger resistor can further be connected to it externally. In this case, however, care must be taken about changes in output level.

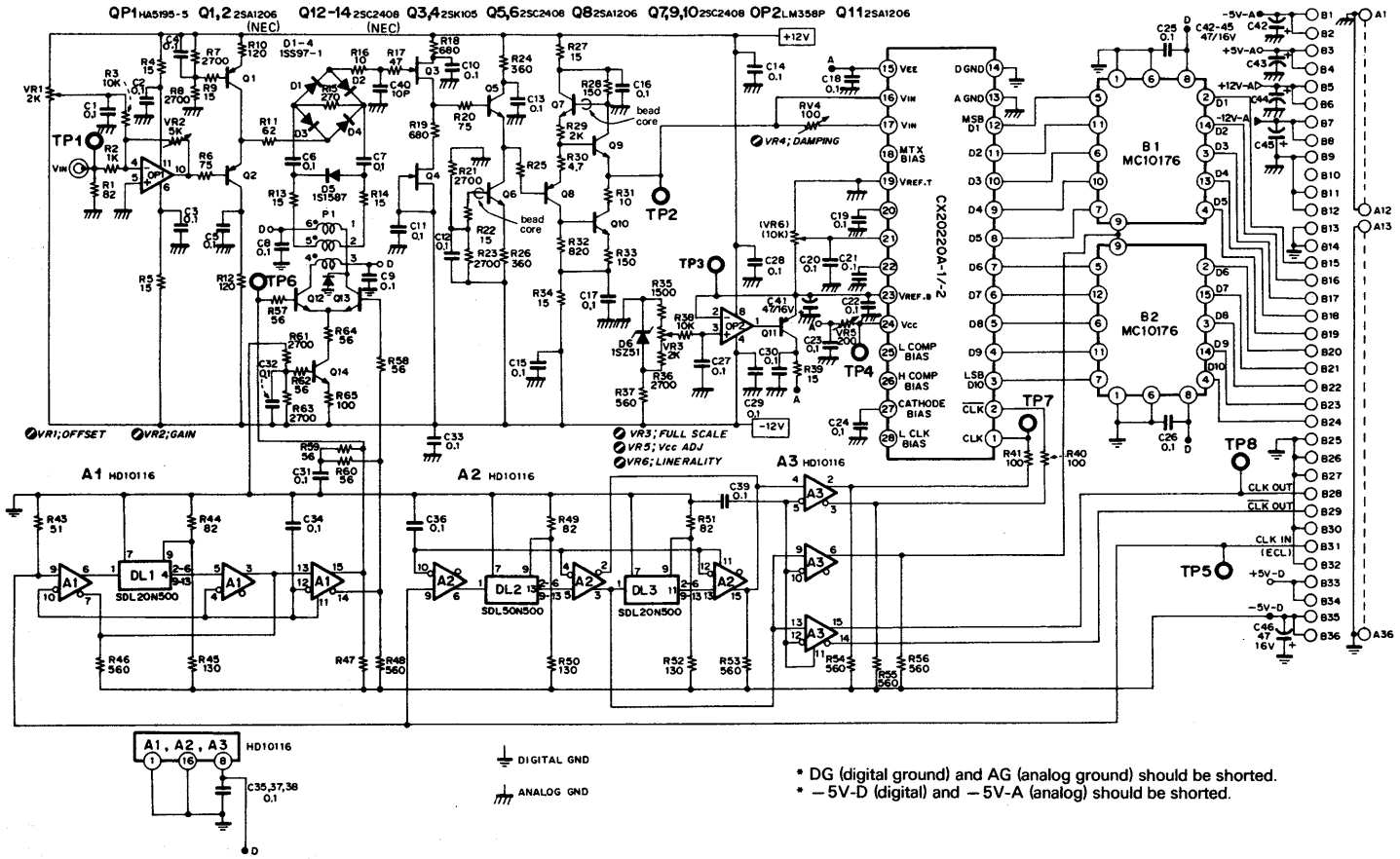
Other

Pin 18 (MTX BIAS), pin 25 (LCOM BIAS), pin 26 (HCOMP BIAS) and pin 28 (LCLK BIAS) are not used. These pins should never be connected to GND, power supply or any other pins.

Application Circuit (1)



Application Circuit (2)



* DG (digital ground) and AG (analog ground) should be shorted.
* −5V-D (digital) and −5V-A (analog) should be shorted.

8 bit 30/50 MSPS Flash A/D Converter

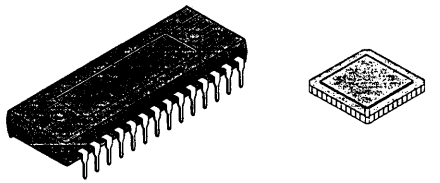
Evaluation Board Available — CXA1016PPCB/CXA1016KPCB
CXA1056PPCB/CXA1056KPCB

Description

CXA1016P/CXA1016K/CXA1056P/CXA1056K are 8 bit high-speed A/D converter ICs for various applications. They can be used widely for various purposes which require high-speed A/D conversions.

CXA1016P/CXA1056P are assembled in the plastic DIP packages and CXA1016K/CXA1056K are in the ceramic lead-less chip carriers.

28 pin DIP (Plastic) 44 pin LCC (Ceramic)



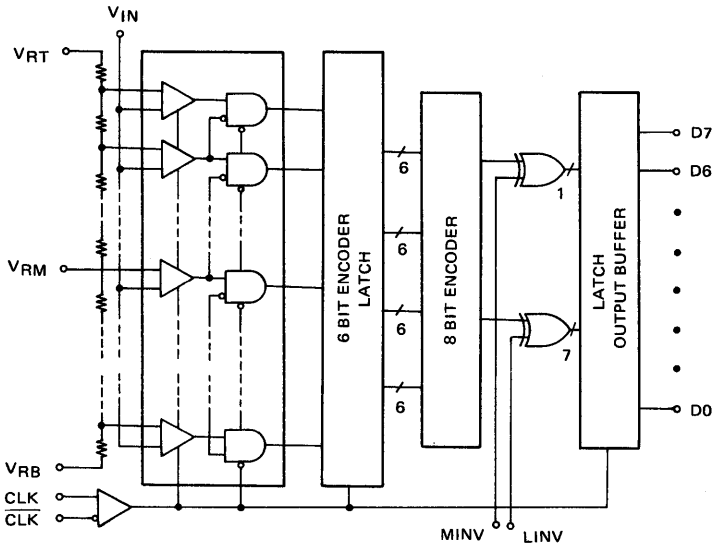
Features (CXA1016P/CXA1016K)

• Resolution	8 bits ± 1/2 LSB
• High-speed operation	Maximum conversion Rate 30 MSPS
• Wide analog input bandwidth	30MHz (−3dB)
• Low input capacitance	35 pF (typ)
• Low power consumption	420 mW (typ)

Features (CXA1056P/CXA1056K)

• Resolution	8 bits ± 1/2 LSB
• High-speed operation	Maximum conversion Rate 50 MSPS
• Wide analog input bandwidth	50MHz (−3dB)
• Low input capacitance	35 pF (typ)
• Low power consumption	550 mW (typ)

Block Diagram



E89643-ST

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{EE}	0 to −7	V
• Analog input voltage	V_{IN}	0.5 to V_{EE}	V
• Reference input voltage	V_{RT}, V_{RB}, V_{RM}	0.5 to V_{EE}	V
	$\lvert V_{RT}-V_{RB} \rvert$	2.5	V
• Digital input voltage	CLK, $\overline{CLK}$, MINV, LINV	0.5 to −4	V
• VRM pin input current	I_{VRM}	−3 to +3	mA
• Digital output current	I_{D0} to I_{D7}	0 to −10	mA
• Operating temperature	Ta	−20 to +100	°C (CXA1016P/CXA1056P)
	Tc	−25 to +125	°C (CXA1016K/CXA1056K)*1
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	1.48	W (CXA1016P/CXA1056P)
		1.08	W (CXA1016K/CXA1056K)

*1 Heat sinking is required above 100°C (CXA1016K)/86°C (CXA1056K).

Recommended Operating Conditions (CXA1016P/CXA1016K)

		Min.	Typ.	Max.	Unit
• Supply voltage	AV_{EE}, DV_{EE}	−5.7	−5.2	−5.0	V
	AV_{EE}-DV_{EE}	−0.05	0	0.05	V
	AGND-DGND	−0.05	0	0.05	V
• Reference input voltage	V_{RT}	−0.1	0	0.1	V
	V_{RB}	−2.2	−2	−1.8	V
• Analog input voltage	V_{IN}	V_{RB}		V_{RT}	
• Clock pulse width	Tpw1	25			ns
	Tpw0	8			ns

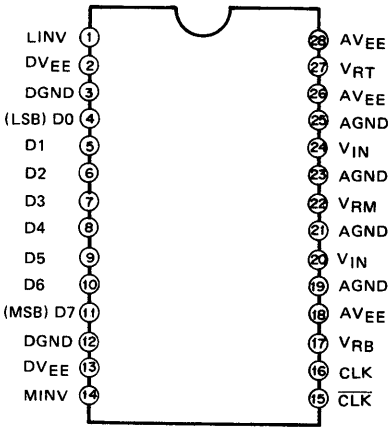
Recommended Operating Conditions (CXA1056P/CXA1056K)

		Min.	Typ.	Max.	Unit
• Supply voltage	AV_{EE}, DV_{EE}	−5.7	−5.2	−5.0	V
	AV_{EE}—DV_{EE}	−0.05	0	0.05	V
	AGND—DGND	−0.05	0	0.05	V
• Reference input voltage	V_{RT}	−0.1	0	0.1	V
	V_{RB}	−2.2	−2	−1.8	V
• Analog input voltage	V_{IN}	V_{RB}		V_{RT}	
• Clock pulse width	Tpw1	15			ns
	Tpw0	5			ns

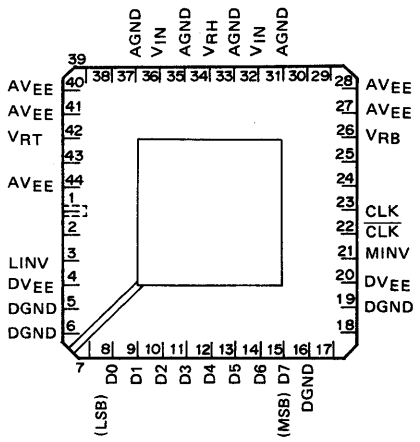
Pin Configuration (Top View)

The pin numbers without indication are empty pins. (not connected)

CXA1016P/CXA1056P



CXA1016K/CXA1056K



Pin Description

Symbol	Function
AVEE	Analog VEE, −5.2V (typ). Coupled with ~6Ω between DVEE.
LINV	Input pin for output polarity inversion of D0 (LSB)~D6. (See the code table)
DVEE	Digital VEE, −5.2V (typ).
DGND	Digital GND, which is separated from the Analog GND.
D0~D7	Digital data output pin, ECL level. D0: LSB~D7: MSB. Pull-down resistors are necessary externally.
MINV	Input pin for output polarity inversion of D7 (MSB) (See the code table). ECL level. "0" level is held when it is released.
$\overline{CLK}$	Inverse clock input pin, ECL level.
CLK	Clock input pin, ECL level.
VRB	Reference voltage (bottom), −2V (typ).
AGND	Analog GND
VIN	Analog input, input range is VRT~VRB
VRM	Middle point of the reference voltage, it can be used as a linearity correction pin.
VRT	Reference voltage (top), 0V (typ).
	Empty pins (not connected), 2 and 19 are used to be grounded to DGND, the others are used to be grounded to AGND.

Output Coding

MINV LINV	0 0	0 1	1 0	1 1
0V	111...11	100...00	011...11	000...00
.	111...10	100...01	011...10	000...01
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
VIN .	100...00	111...11	000...00	011...11
.	011...11	000...00	111...11	100...00
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	000...01	011...10	100...01	111...10
−2V	000...00	011...11	100...00	111...11

1: VIH, VOH
0: VIL, VOL

Electrical Characteristics (CXA1016P/CXA1016K)

(T_a=25°C, V_{EE}=−5.2V, V_{RT}=0V, V_{RB}=−2V)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum Conversion Rate		Fc	V_{IN}=0 to −2V, fin=1 kHz, ramp	30			MSPS
Supply Current		I_{EE}			−75	−100	mA
Analog Input Capacitance		C_{IN}	V_{IN}=−1V+0.07 Vrms		35	40	pF
Analog Input Bias Current		I_{IN}	V_{IN}=−1V		60	90	μA
Reference Resistor		Rr (V_{RT}~V_{RB})		70	80	100	Ω
Offset Voltage	V_{RT}			7	9	11	mV
	V_{RB}			15	17	19	mV
Digital Input Voltage		V_{IH}		−1.0	−0.9	−0.7	V
		V_{IL}		−1.9	−1.75	−1.6	V
Digital Input Current		I_{IH}	V_{IH}=−0.9V	0		0.4	mA
		I_{IL}	V_{IL}=−1.75V	−0.05		0.35	mA
Digital Output Voltage		V_{OH}	$R\ell$=620Ω ~ V_{EE}	−1.0			V
		V_{OL}				−1.6	V
Output Data Delay		Td	$R\ell$=620Ω ~ V_{EE}		4.0	5.0	ns
Non-linearity Error			Fc = 30 MSPS, V_{IN}=0 to −2V, fin=1 kHz, ramp			±½	LSB
Differential Non-linearity Error			Fc = 30 MSPS			±½	LSB
Differential Gain		DG	NTSC 40 IRE mod. ramp, Fc = 30 MSPS			1.5	%
Differential Phase		DP				0.5	deg.
Aperture Jitter		Taj			45		ps
Sampling Delay		Tsd		6.3	6.8	7.3	ns
Full scale input BW (−3dB)		BW_F	*1		30		MHz

*1 Source impedance = 50 Ω
Without a buffer amplifier driving A/D input

Electrical Characteristics (CXA1056P/CXA1056K)

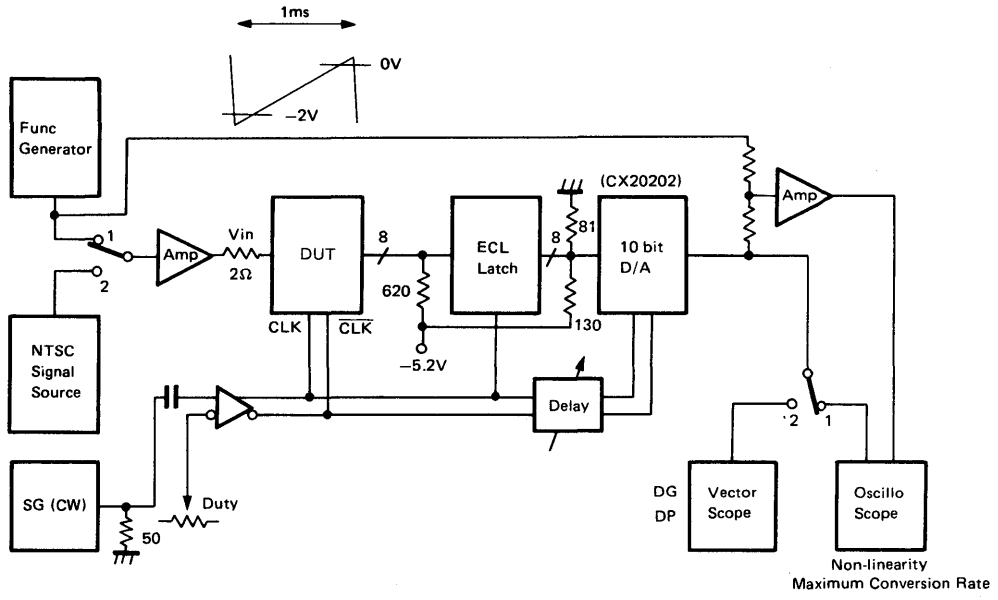
(Ta=25°C, V_{EE}=−5.2V, V_{RT}=0V, V_{RB}=−2V)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum Conversion Rate		Fc	V_{IN}=0 to −2V, fin=1 kHz, ramp	50			MSPS
Supply Current		I_{EE}			−95	−120	mA
Analog Input Capacitance		C_{IN}	V_{IN}=−1V+0.07 Vrms		35	40	pF
Analog Input Bias Current		I_{IN}	V_{IN}=−1V		75	115	μA
Reference Resistor		Rr (V_{RT}~V_{RB})		70	80	100	Ω
Offset Voltage	V_{RT}			7	9	11	mV
	V_{RB}			15	17	19	mV
Digital Input Voltage		V_{IH}		−1.0	−0.9	−0.7	V
		V_{IL}		−1.9	−1.75	−1.6	V
Digital Input Current		I_{IH}	V_{IH}=−0.9V	0		0.4	mA
		I_{IL}	V_{IL}=−1.75V	−0.05		0.35	mA
Digital Output Voltage		V_{OH}	Rℓ=620Ω ~ V_{EE}	−1.0			V
		V_{OL}				−1.6	V
Output Data Delay		Td	Rℓ=620Ω ~ V_{EE}		4.0	5.0	ns
Non-linearity Error			Fc = 50 MSPS, V_{IN}=0 to −2V, fin=1 kHz, ramp			±½	LSB
Differential Non-linearity Error			Fc = 50 MSPS			±½	LSB
Differential Gain		DG	NTSC 40 IRE mod. ramp, Fc = 50 MSPS			1.5	%
Differential Phase		DP				0.5	deg.
Aperture Jitter		Taj			30		ps
Sampling Delay		Tsd		5.4	5.7	6.0	ns
Full scale input BW (−3dB)		BW_F	*1		50		MHz

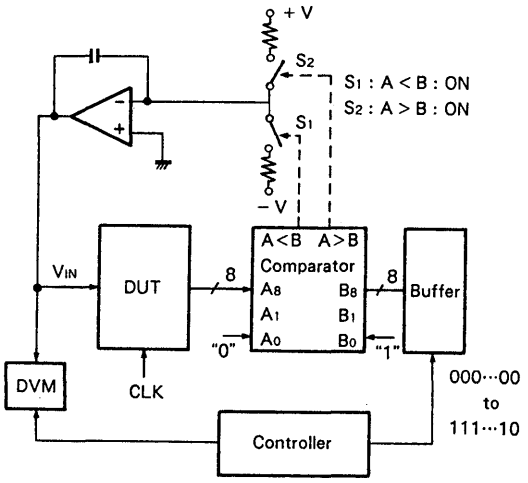
*1 Source impedance = 50 Ω
Without a buffer amplifier driving A/D input

Electrical Characteristics Test Circuit

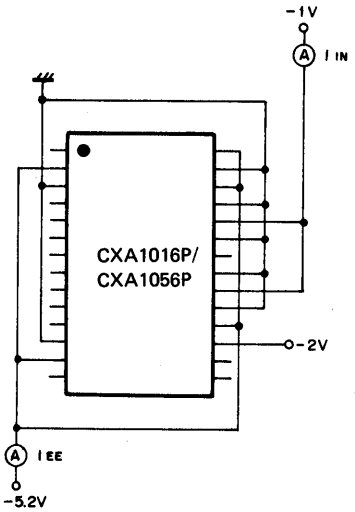
Maximum Conversion Frequency Test Circuit
Differential Gain Error Test Circuit
Differential Phase Error Test Circuit

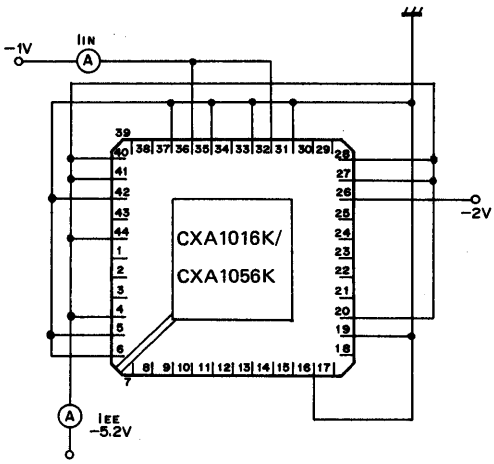


Differential Non-linearity Test Circuit
Integral Non-linearity Test Circuit

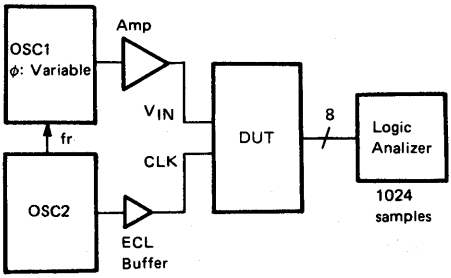


Power Supply Current Test Circuit
Analog Input Bias Current Test Circuit





Aperture Jitter Test Circuit



Description of Function (See the block diagram and timing chart.)

1. The reference voltage, which is obtained by dividing equally the voltage across V_{RT} to V_{RB} into 256 by the reference resistor ledder, is applied to the respective ⊕ (positive) input sides of 256 clocked comparators. An analog input is applied to the ⊖ (negative) input sides of all the 256 clocked comparators from the V_{IN} pin.

2. When the state of CLK is in Low, the master (front stage) of the comparator compares the respective reference voltage and the analog input voltage which is ever-changing.

3. When the CLK moves from Low into Hi, each master latches the state immediately prior to the above simultaneously, and as a result, it provides conditions of "11 .... 1100 .. 0" in sequence from the V_{RT} side to the V_{RB} side.

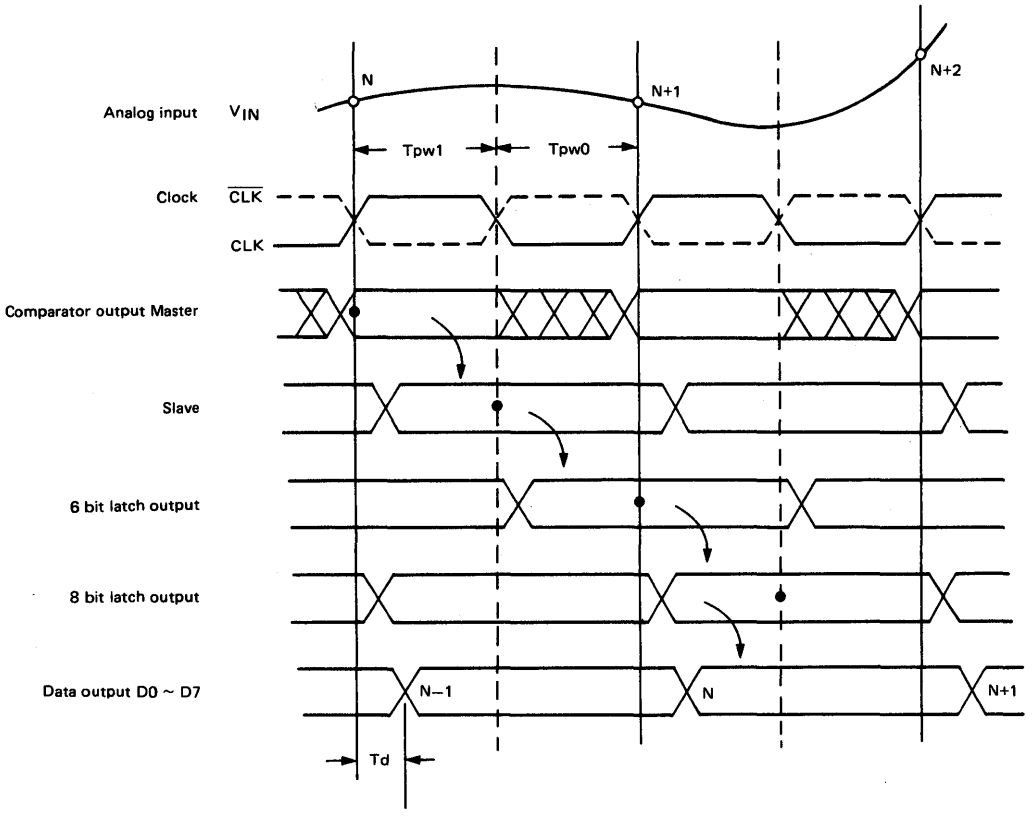
4. The output of the master is ANDed between the respective adjacent outputs, and "1" stands only when neighboring 2 outputs become "10", and the all other outputs become "0".

5. The result of the AND is latched when CLK moves from Hi into Low. Output of the slave is divided into 4 blocks and each block has 32 clocked comparators, and they are coded into binary codes of 6 bits respectively by the transistor matrix circuit.

6. The 6 bit codes are further coded into 8 bit codes by the transistor matrix circuit after they are respectively latched, and they are then output into the ECL level by the output buffer after being 8 bit latched. The output data is delayed 1 clock from the data sampling point and appears at the output pin.

7. Two polarity inversion inputs such as MINV and LINV are fed externally to the output buffer, and each of them selects output polarity of MSB and other polarity than MSB respectively.

Timing Chart

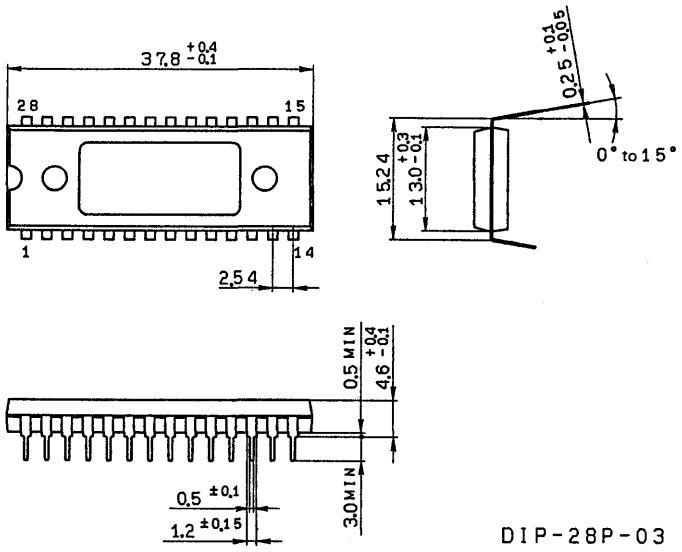


Dots (•) in the chart demote respective latch timings.

*See page 54 for Tpwl and Tpw0.

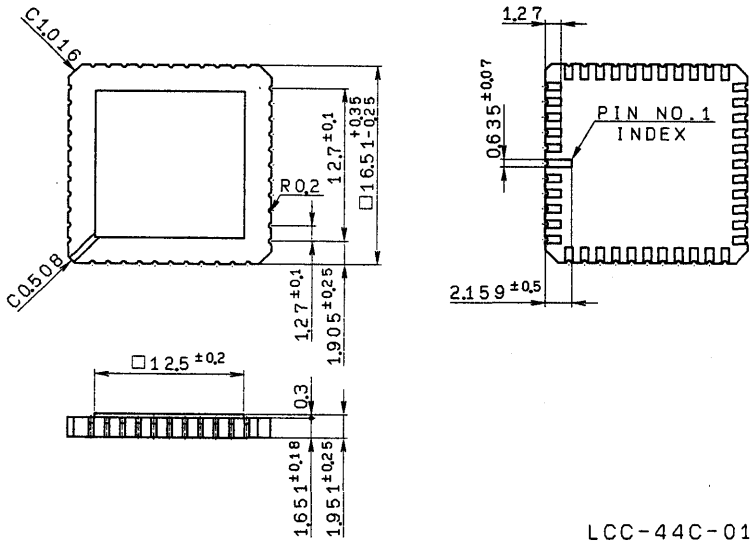
Package Outline Unit: mm

CXA1016P/CXA1056P 28 pin DIP (Plastic)



DIP-28P-03

CXA1016K/CXA1056K 44 pin LCC (Ceramic)



LCC-44C-01

SONY CXA1076K/CXA1176K

8-bit 200/300 MSPS Flash A/D Converter

Description

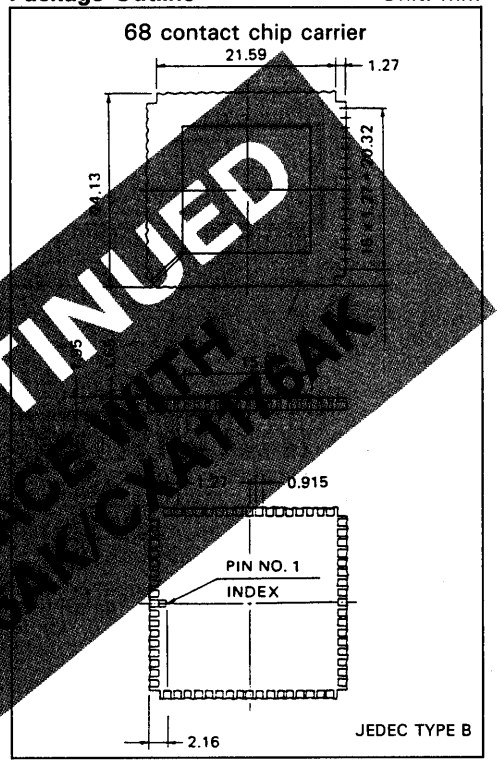
The CXA1076K/CXA1176K are monolithic flash A/D converters capable of digitizing 0 to −2V analog input signal into 8-bit binary code at a sampling rate of 200MSPS (CXA1076K)/ 300MSPS (CXA1176K).

They operate with a single −5.2V power supply and consume only 720/1300 mW.

The digital I/O level is compatible with 100K/10KH/10K series ECL, and complementary digital output makes ease to interface to external circuits. Output ports have a capability to drive into 50 Ω load to −2 V.

In addition to 8-bit output data, they have an over range output and two digital inputs which enable to program output format for true or inverse binary and offset two's complement.

Package Outline Unit: mm



Features (CXA1076K/CXA1176K)

- Ultra high speed 200/300 MSPS
- Wide input band width 450/1100 MHz
- Low power consumption 720/1300 mW
- Internal linearity compensation circuit
- Complementary ECL output
- Over range output
- Programmable output format
- Small 68 LCC package

Applications

Digital oscilloscope, radar, image processing, transient capture and fast digital signal processing.

Absolute Maximum Ratings (T_a = 25°C)

• Supply voltage	AV_{EE}, DV_{EE}	0.5 to −7	V
• Analog input voltage	V_{IN}	0.5 to V_{EE}	V
• Reference input voltage	V_{RT}, V_{RB}	0.5 to V_{EE}	V
	V_{RT}-V_{RB}	0 to 2.5	V
• Digital input voltage	CLK, $\overline{CLK}$, MINV, LINV	0.5 to V_{EE}	V
• Digital output current	ID0 to ID7, IOR	0 to −30	mA
	$\overline{ID0}$ to $\overline{ID7}$, $\overline{IOR}$	0 to −30	mA
• Operating temperature	T_a	−25 to +75	°C
	T_c	−55 to +125	°C
• Storage temperature	T_{stg}	−65 to +150	°C
• Allowable power dissipation	P_D	1.8	W

70125-YA

SONY® CXA1076AK/CXA1176AK

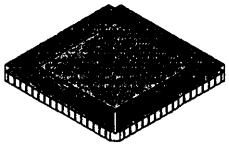
8-bit 200/300 MSPS Flash A/D Converter

Advance Information

Evaluation Board Available — CXA1076AK PCB/CXA1176AK PCB

Notice: This specification is subject to change.

68 pin LCC (Ceramic)



Description

CXA1076AK/CXA1176AK are monolithic flash A/D converters capable of digitzing 0 to −2 V analog input signal into 8-bit binary code at a sampling rate of 200MSPS (CXA1076AK)/ 300MSPS (CXA1176AK).

They operate with a single −5.2 V power supply and consume only 1450 mW.

The digital I/O level is compatible with 100K/10KH/10K series ECL, and complementary digital output makes ease to interface to external circuits. Output ports have a capability to drive into 50 Ω load to −2 V.

In addition to 8-bit output data, they have an over range output and two digital inputs which enable to program output format for true or inverse binary and offset two's complement.

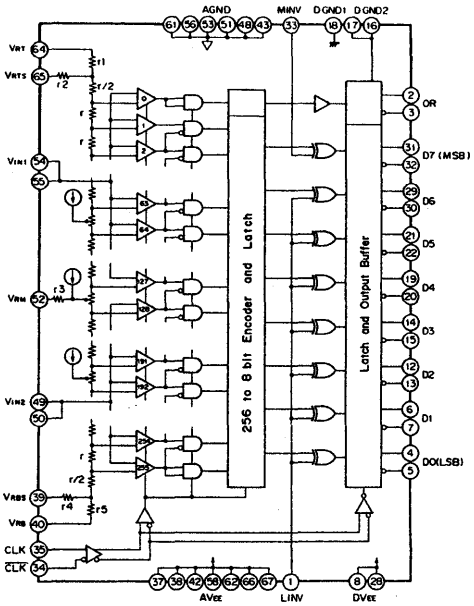
Features

- Ultra high speed
- Wide input band width
- Low power consumption 1450 mW
- Internal linearity compensation circuit
- Complementary ECL output
- Over range output
- Programmable output format
- Small 68 LCC package
- Pin replacable with CXA1076K/CXA1176K

Applications

Digital oscilloscope, radar, image processing, transient capture and fast digital signal processing.

Block Diagram



AE89670-YA

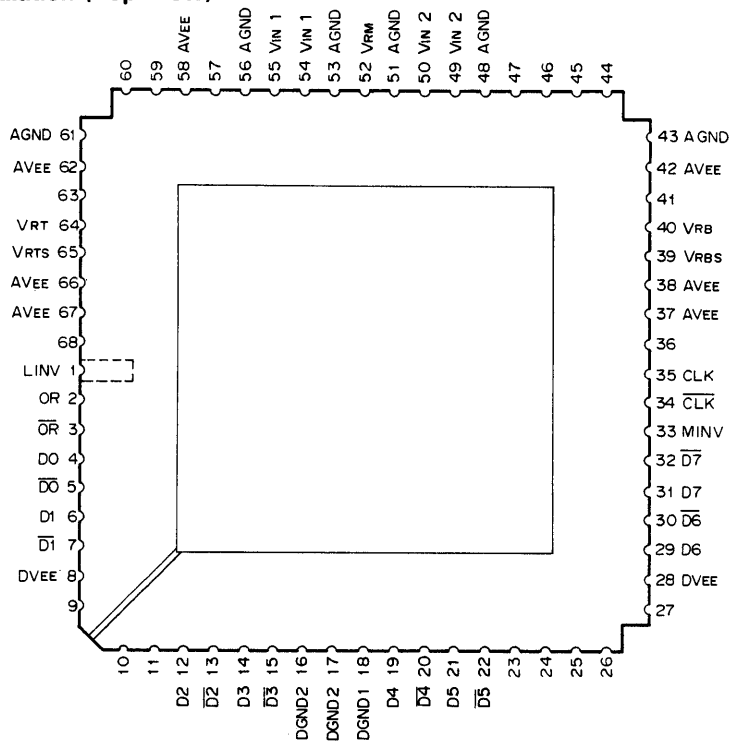
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	AV_{EE}, DV_{EE}	0.5 to −7	V
• Analog input voltage	V_{IN}	0.5 to V_{EE}	V
• Reference input voltage	V_{RT}, V_{RB}	0.5 to V_{EE}	V
	V_{RT}-V_{RB}	0 to 2.5	V
• Digital input voltage	CLK, $\overline{CLK}$, MINV, LINV	0.5 to V_{EE}	V
• Digital output current	$\overline{ID0}$ to $\overline{ID7}$, $\overline{IOR}$	0 to −30	mA
	$\overline{ID0}$ to $\overline{ID7}$, $\overline{IOR}$	0 to −30	mA
• Operating temperature	T_a	−25 to +75	°C
	T_c	−55 to +125	°C
• Storage temperature	T_{stg}	−65 to +150	°C
• Allowable power dissipation	P_D	1.8	W

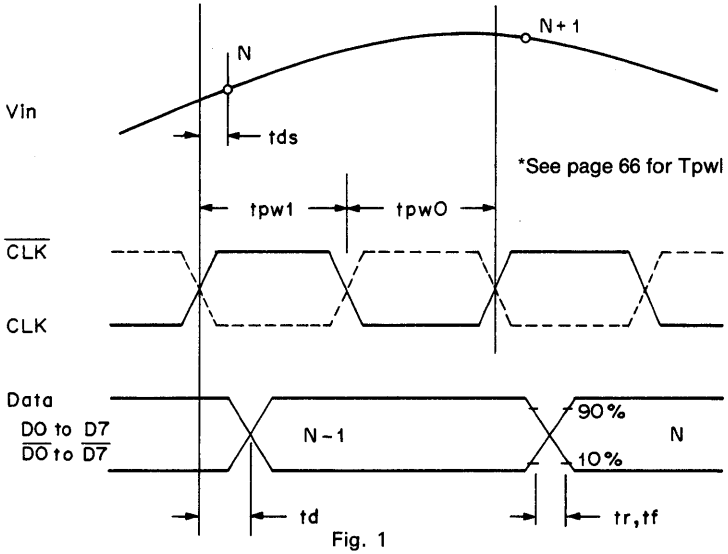
Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	AV_{EE}, DV_{EE}	−4.95	−5.2	−5.5	V
Supply votage	$\lvert AV_{EE} - DV_{EE} \rvert$		0	0.05	V
Ground	|DGND−AGND|		0	0.05	V
Analog input voltage	V_{IN}	V_{RB}		V_{RT}	
Reference input voltage	V_{RT}	−0.1	0	+0.2	V
Reference input voltage	V_{RB}	−2.2	−2	−1.9	V
Digital input voltage	V_{IH}	−1.0		−0.7	V
Digital input voltage	V_{IL}	−1.9		−1.6	V
Clock pulse width	TPW1 (CXA1076AK)	3.5			ns
Clock pulse width	TPW0 (CXA1076AK)	1.5			ns
Clock pulse width	TPW1 (CXA1176AK)	2.5			ns
Clock pulse width	TPW0 (CXA1176AK)	0.8			ns

Pin Configulation (Top View)



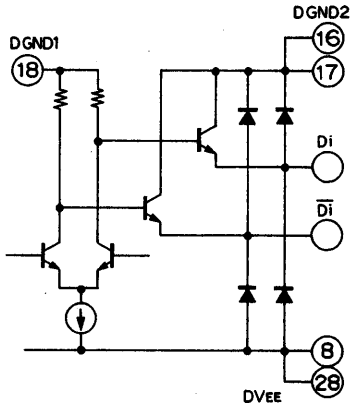
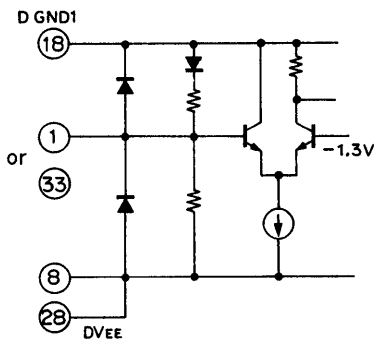
Timing Chart

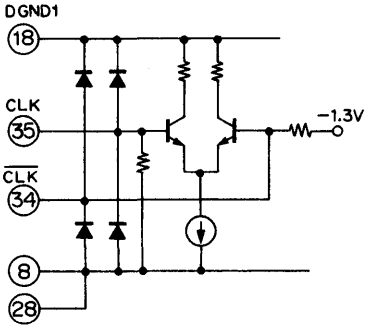
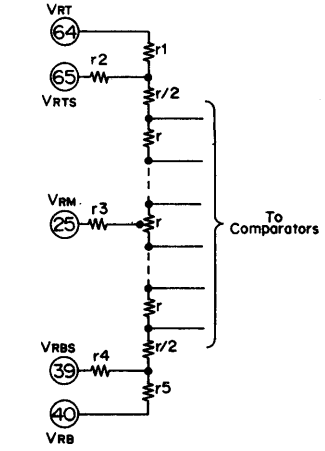
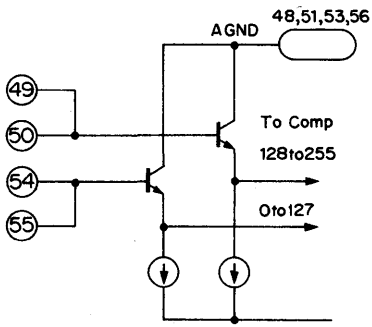


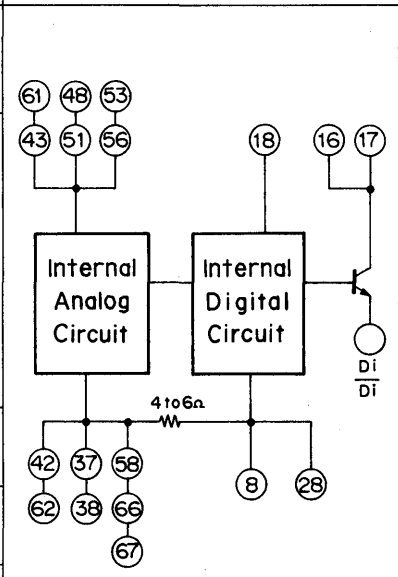
*See page 66 for Tpwl and Tpw0.

Fig. 1

Pin Description and I/O Equivalent Circuits

No.	Symbol	Equivalent circuit	Description
4 5	D_0 $\overline{D_0}$		LSB and complementary LSB output
6 7	D_1 $\overline{D_1}$		D_1 to D_6: output $\overline{D_1}$ to $\overline{D_6}$: complementary output
12 13	D_2 $\overline{D_2}$		
14 15	D_3 $\overline{D_3}$		
19 20	D_4 $\overline{D_4}$		
21 22	D_5 $\overline{D_5}$		
29 30	D_6 $\overline{D_6}$		
31 32	D_7 $\overline{D_7}$		MSB and complementary MSB output
2 3	OR $\overline{OR}$		Over Range and complementary Over Range output
33	MINV		Polarity select for MSB (Refer to coding table) L level is maintained with left open.
1	LINV		Polarity select for LSBs (Refer to coding table) L level is maintained with left open.

No.	Symbol	Equivalent circuit	Description
35	CLK		CLK input
34	$\overline{CLK}$		Complementary CLK input V_{BB} (−1.3V) is maintained with left open. With bypassing, it can be used as a reference for single CLK input.
64	V_{RT}		Analog reference voltage (Top) (0V Typ.)
65	V_{RTS}		Reference voltage sense (Top)
52	V_{RM}		Reference voltage mid-point It can be used as a linearity compensation.
39	V_{RBS}		Reference voltage sense (Bottom)
40	V_{RB}		Analog reference voltage (Bottom) (−2V Typ.)
49 50 54 55	V_{IN}		Analog input All of the pins must be wired externally.

No.	Symbol	Equivalent circuit	Description
43, 48, 51, 53, 56, 61	AGND (*1)		Analog ground
37, 38, 42, 58, 62, 66, 67	AVEE (*1)		Analog supply
18	DGND1		Digital ground
16 17	DGND2 (*1)		Digital ground for output drive
8 28	DVEE (*1)		Digital supply
9, 10 11, 23 24, 25 26, 27 36, 68	NC		Empty pins It is recommended to wire these pins to DGND.
41, 44 45, 46 47, 57 59, 60 63	NC		Empty pins It is recommended to wire these pins to AGND.

(*1) All of these pins must be wired to the respective external circuit.

Input-Output Reference and Output Format

Vin	Step	MINV 1 LINV 1												0 1												1 0												0 0											
		OR	MSB										LSB	OR	MSB										LSB	OR	MSB										LSB	OR	MSB										LSB
0V		0	0	0	0	·	·	·	0	0				0	1	0	0	·	·	·	0	0				0	0	1	1	·	·	·	1	1				0	1	1	1	·	·	·	1	1			
	0	1	0	0	0	·	·	·	0	0				1	1	0	0	·	·	·	0	0				1	0	1	1	·	·	·	1	1				1	1	1	1	·	·	·	1	1			
	1	1	0	0	0	·	·	·	0	1				1	1	0	0	·	·	·	0	1				1	0	1	1	·	·	·	1	0				1	1	1	1	·	·	·	1	0			
−1V	127	1	0	1	1	·	·	·	1	1				1	1	1	1	·	·	·	1	1				1	0	0	0	·	·	·	0	0				1	1	0	0	·	·	·	0	0			
	128	1	1	0	0	·	·	·	0	0				1	0	0	0	·	·	·	0	0				1	1	1	1	·	·	·	1	1				1	0	1	1	·	·	·	1	1			
	254	1	1	1	1	·	·	·	1	0				1	0	1	1	·	·	·	1	0				1	1	0	0	·	·	·	0	1				1	0	0	0	·	·	·	0	1			
	255	1	1	1	1	·	·	·	1	1				1	0	1	1	·	·	·	1	1				1	1	0	0	·	·	·	0	0				1	0	0	0	·	·	·	0	0			
−2V		1	1	1	1	·	·	·	1	1				1	0	1	1	·	·	·	1	1				1	1	0	0	·	·	·	0	0				1	0	0	0	·	·	·	0	0			

Table 1

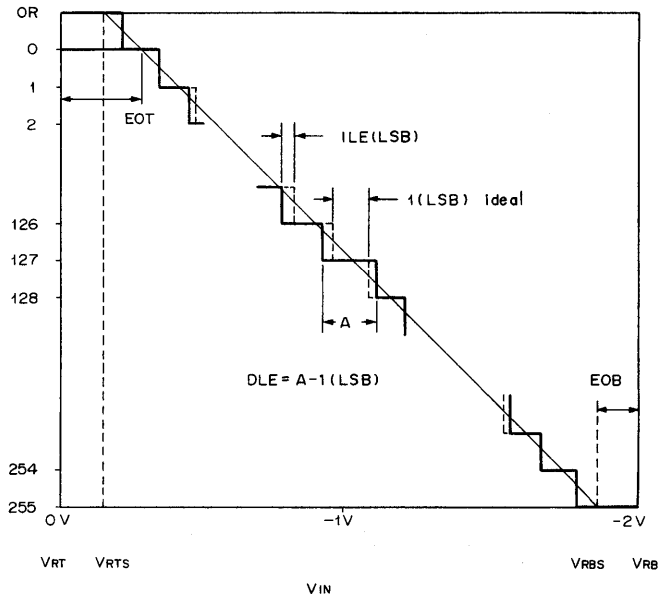


Fig. 2

Electrical Characteristics — CXA1076AK

T_a = 25°C, AV_{EE} = DV_{EE} = −5.2 V
V_{RT} = V_{RTS} = OV, V_{RB} = V_{RBS} = −2 V

Notice: Some parameter specs are subject to change.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum conversion rate (1)		Fc	V_{IN} = FS, F_{IN} = 1 kHz	200	240		MSPS
Maximum conversion rate (2)		Fc	V_{IN} = FS F_{IN} = 49.999 MHz	200	240		MSPS
Resolution			Fc = 200 MSPS		8		bit
Integral linearity		EIL			±0.3	±0.5	LSB
Differential linearity		EDL			±0.3	±0.5	LSB
Offset error	V_{RT}	EOT		12.0	14.5	17.0	mV
	V_{RB}	EOB		4.0	6.5	9.0	mV
Analog input capacitance		CIN	V_{IN} = −1 V +0.07 rms	21	25	35	pF
Analog input current		IIN	V_{IN} = OV	70	150	700	μA
Supply current	Analog	IEEA		150	200	260	mA
	Digital	IEED		60	70	90	mA
Referrence resistance		RREF	V_{RT} to V_{RB}	75	90	108	Ω
Residual resistance		r1, r5		0.43	0.52	0.62	Ω
		r2, r4		0.64	0.77	0.92	Ω
		r3		2.8	3.4	4.1	Ω
Input level digital	H	VIH		−1.0	−0.85	−0.7	V
	L	VIL		−1.9	−1.75	−1.6	V
Output level digital	H	VOH	R_L = 50 Ω to −2 V FO = 1 (100 K ECL)	−1.05			V
	L	VOL				−1.6	V
Output data delay		td		1.7	2.0	3.1	ns
Rise time output digital		tr		0.8	1.2	1.5	ns
Fall time output digital		tf		0.8	1.2	1.5	ns
Full scale input BW (−3dB)		BWF	V_{IN} = FS (*1)		220		MHz
Small signal input BW		BWS	V_{IN} = 0.6 Vp-p (*1)		TBD		MHz
Aperture jitter		taj			3.0	3.6	ps
Sampling delay		tds		0.6	0.8	1.1	ns
SNR1			F_{IN} = 1 MHz FS Fc = 200MSPS (*1)		−46	−45.5	dB
SNR2			F_{IN} = 80 MHz, 0.6 Vp-p Fc = 200MSPS (*1)		TBD		dB
Differential gain		DG	NTSC 40 IRE mod. ramp Fc = 200 MSPS			1.0	%
Differential phase		DP				0.5	deg.
Error rate		ER	Fc = 200 MSPS F_{IN} = 49.999 MHz V_{IN} = 2 Vp-p tpw1 = 3.5 ns tpw0 = 1.5 ns Error Threshold: 32 LSB			10^{-8}	times/ sample

(*1) Source impedance = 50 Ω.

Electrical Characteristics — CXA1176AK

T_a = 25°C, AV_{EE} = DV_{EE} = −5.2 V
V_{RT} = V_{RTS} = OV, V_{RB} = V_{RBS} = −2 V

Notice: Some parameter specs are subject to change.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum conversion rate (1)		Fc	V_{IN} = FS, F_{IN} = 1 kHz	300	340		MSPS
Maximum conversion rate (2)		Fc	V_{IN} = FS F_{IN} = 62.499 MHz	250	290		MSPS
Resolution			Fc = 300 MSPS		8		bit
Integral linearity		E_{IL}			±0.3	±0.5	LSB
Differential linearity		E_{DL}			±0.3	±0.5	LSB
Offset error	V_{RT}	E_{OT}		12.0	14.5	17.0	mV
	V_{RB}	E_{OB}		4.0	6.5	9.0	mV
Analog input capacitance		C_{IN}	V_{IN} = −1 V +0.07 rms	21	25	35	pF
Analog input current		I_{IN}	V_{IN} = OV	70	150	700	μA
Supply current	Analog	I_{EEA}		150	200	260	mA
	Digital	I_{EED}		60	70	90	mA
Referrence resistance		R_{REF}	V_{RT} to V_{RB}	75	90	108	Ω
Residual resistance		r1, r5		0.43	0.52	0.62	Ω
		r2, r4		0.64	0.77	0.92	Ω
		r3		2.8	3.4	4.1	Ω
Input level digital	H	V_{IH}		−1.0	−0.85	−0.7	V
	L	V_{IL}		−1.9	−1.75	−1.6	V
Output level digital	H	V_{OH}	R_L = 50 Ω to −2 V FO = 1 (100 K ECL)	−1.05			V
	L	V_{OL}				−1.6	V
Output data delay		td		1.7	2.0	3.1	ns
Rise time output digital		tr		0.8	1.2	1.5	ns
Fall time output digital		tf		0.8	1.2	1.5	ns
Full scale input BW (−3dB)		BW_F	V_{IN} = FS (*2)		250		MHz
Small signal input BW		BW_S	V_{IN} = 0.6 Vp-p (*2)		TBD		MHz
Aperture jitter		taj			3.0	3.6	ps
Sampling delay		tds		0.6	0.8	1.1	ns
SNR1			F_{IN} = 1 MHz FS Fc = 300MSPS (*2)		−46	−45.5	dB
SNR2			F_{IN} = 80 MHz, 0.6 Vp-p Fc = 300MSPS (*2)		TBD		dB
Differential gain		DG	NTSC 40 IRE mod. ramp Fc = 300 MSPS			1.0	%
Differential phase		DP				0.5	deg.
Error rate		E_R	Fc = 250 MSPS F_{IN} = 62.499 MHz V_{IN} = 2 Vp-p tpw1 = 3.0 ns tpwo = 1.0 ns Error Threshold: 32 LSB			10^{-8}	times/ sample

(*2) Source impedance = 50 Ω.

Application Circuit

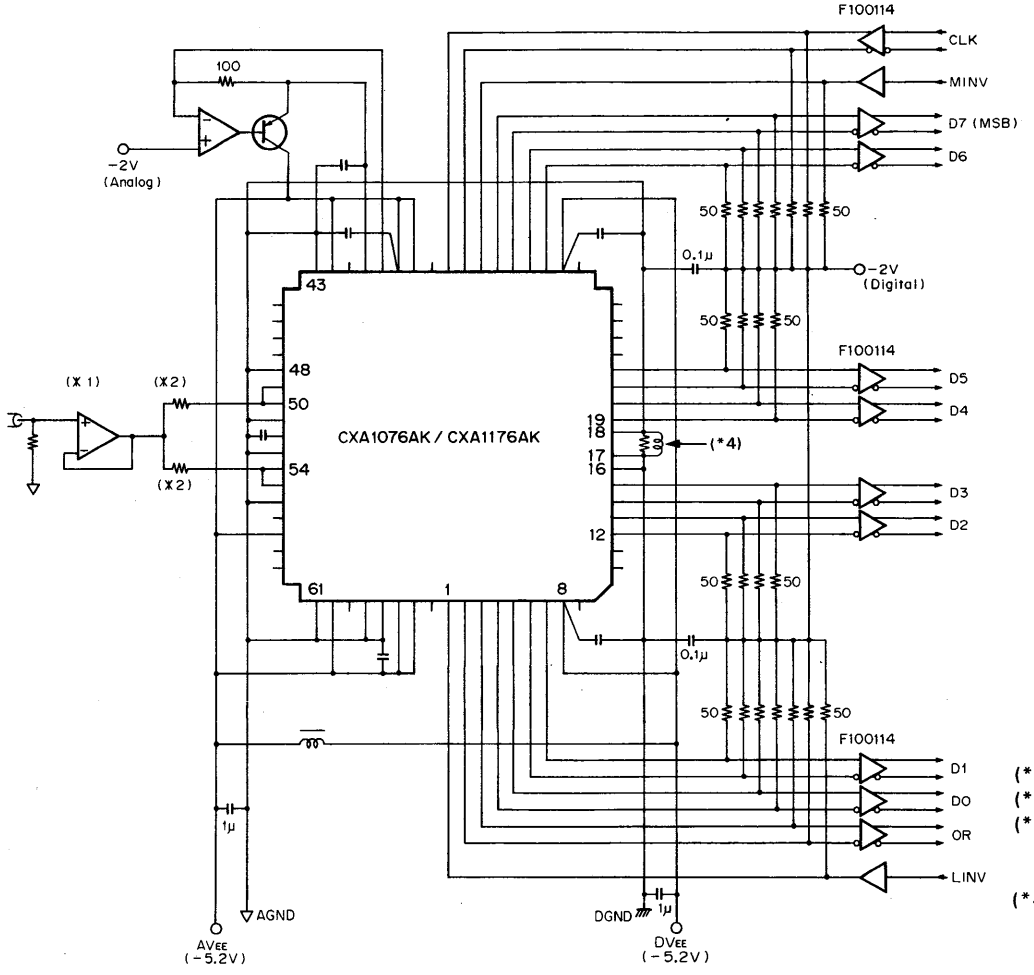


Fig. 3

(*1) Comlinear CLC231 or equiv.
(*2) To be selected (2 to 20Ω)
(*3) Capacitors are 0.01μF ceramic chip not otherwise specified.
(*4) R: 1 Ω with very low inductance
L: 0.22 μH
This is optional for preventing oscillation

Notes on Application

1) AGND, DGND, AV_{EE} and DV_{EE} planes on a PCB should be designed to make those impedance small for the noise suppression benefits. Those planes should be made as wide as possible on the PCB with at least double layer metal patterns.

2) It is recommended to separate the analog and digital V_{EE} on the PCB patterns to make reduce a noise contamination from digital system to analog system.

3) If separate V_{EE} and GND are used, it is recommended to connect the digital and analog planes by a core inductor with good frequency characteristics to avoid the DC voltage difference between analog and digital planes.
The DC voltage difference between AGND and DGND degrades performance and a continual voltage difference between AV_{EE} and DV_{EE} may cause a destruction of the device.

4) The analog and analog power supply pins should be bypassed as close to the device as possible to their respective grounds with at least a 10 nF ceramic chip capacitor. A 1 μF tantalum capacitor can also be used for low frequency bypassing.

5) Pin connections for the device should be made as short as possible. Using of a socket might degrade the performance because of an increasing of lead inductance. A possible compromise is to use AMP's socket 55159-2 (with heat sink).

6) A wide band drive amplifier with sufficient drivability and stable operation should be used to drive analog input pin. Comlinear's CLC231 may be used with adiquate frequency compensation.

7) As the analog input impedance of the device is capacitive, the driving amplifier occationally falls into unstable condition and oscillates locally. This instability can be prevented with a resistor inserted in series between the output pin of the amplifier and V_{IN} pins of the device. The resistor is to be selected from 2 to 20 Ω. Separate input for V_{IN} as shown in an application circuit (Fig. 3) may give a good result.

8) Digital output is delivered in complementary to make ease to interface in high speed operation. A 50 Ω termination at the endpoint of the wiring for both Di and $\overline{Di}$ is recommended for noise suppression benefits.

9) V_{RTS} and V_{RBS} pins can be used as a sense for precise adjustment of reference voltage. Fig. 4 shows the adjustment scheme.

10) Internal current compensation circuit for the reference resistor is furnished in the device. This circuit compensates input bias current of the comparators to maintain the linearity over wide temperature range.
V_{RM}, the mid-point of the reference resistor can be used as a trimming pin for more accurate linearity as shown in Fig. 4.
V_{RT}, V_{RB} and V_{RM} should be bypassed to AGND with at least a 100 nF ceramic chip capacitor.

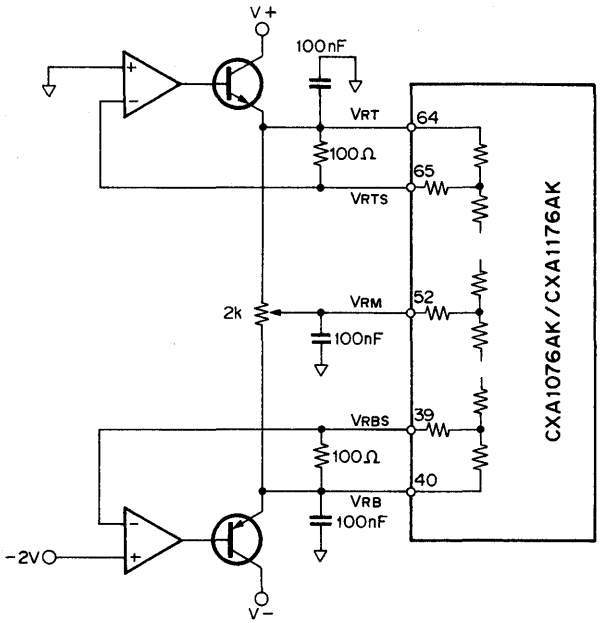
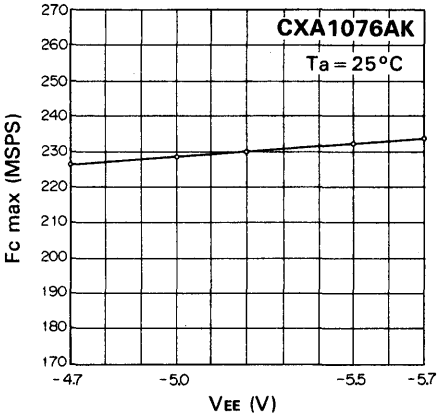


Fig. 4

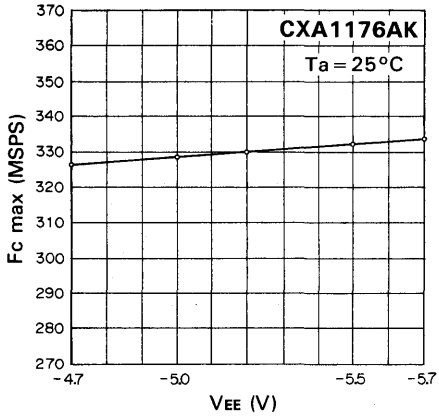
11) OR and $\overline{OR}$ output indicate that the input signal exceeds positive input range. MINV and LINV are not effective to the polarity of OR and $\overline{OR}$ (Refer to the output format).

12) Pin 18 should be tied with AGND pins, not with system digital GND. Small resistor (approx. 1 ohm) and inductance 0.22 μH having small resistance are recommended to use between pin 17 and 18. See "Application Circuit".

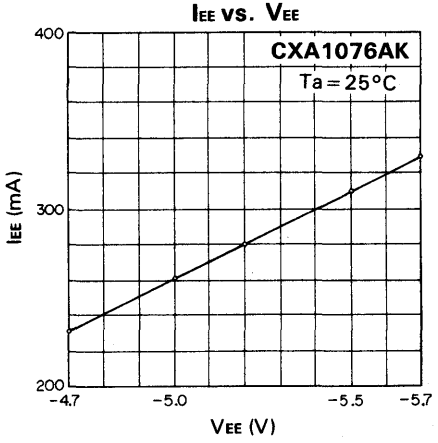
Fc (max) vs. V_{EE}



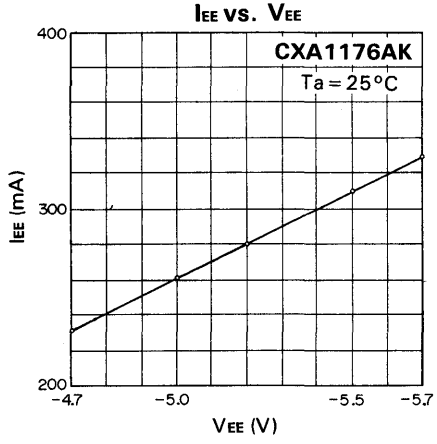
Fc (max) vs. V_{EE}



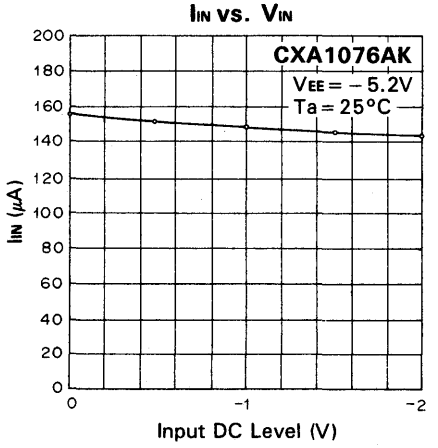
I_{EE} vs. V_{EE}



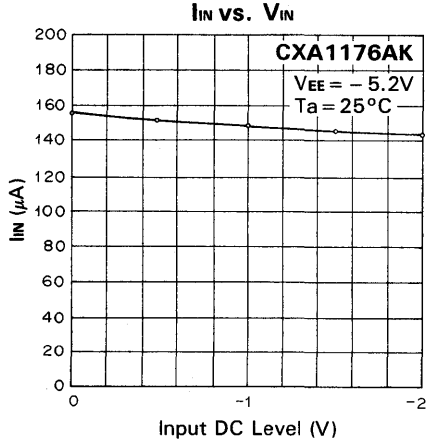
I_{EE} vs. V_{EE}

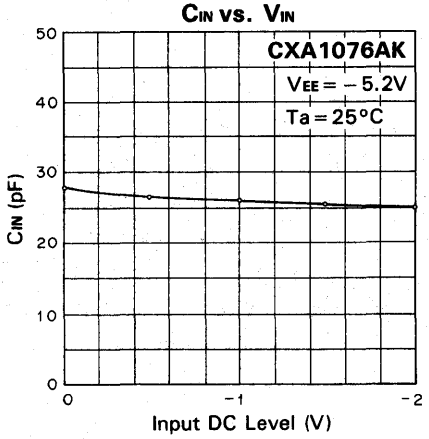


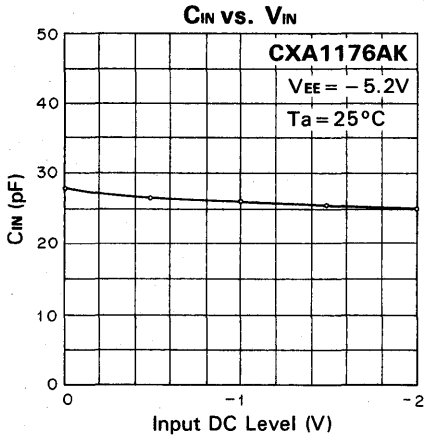
I_{IN} vs. V_{IN}

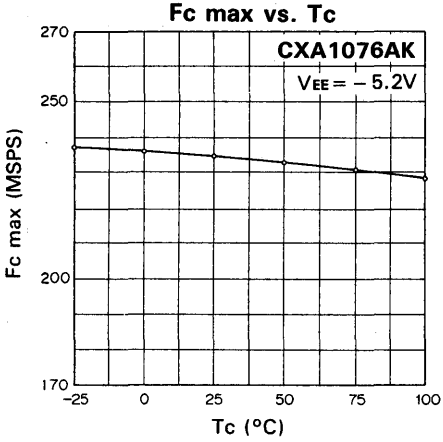


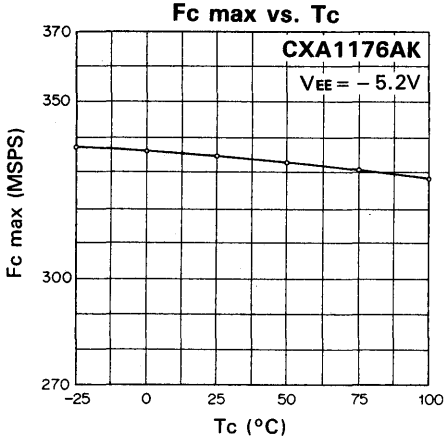
I_{IN} vs. V_{IN}

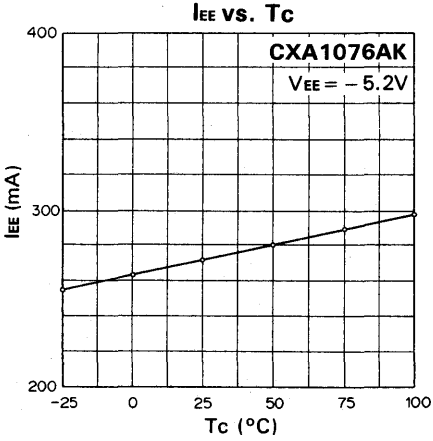


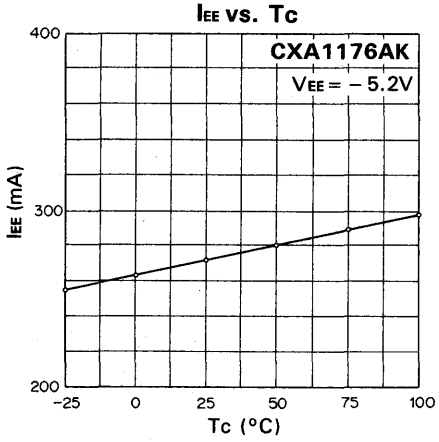

CIN vs. VIN
CXA1076AK
VEE = – 5.2V
Ta = 25°C
CIN (pF)
50
40
30
20
10
0
0
–1
–2
Input DC Level (V)


CIN vs. VIN
CXA1176AK
VEE = – 5.2V
Ta = 25°C
CIN (pF)
50
40
30
20
10
0
0
–1
–2
Input DC Level (V)

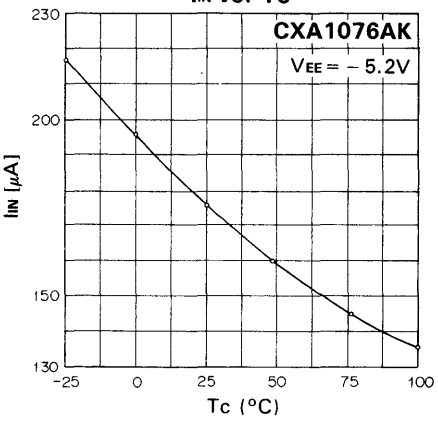

Fc max vs. Tc
CXA1076AK
VEE = – 5.2V
Fc max (MSPS)
270
250
200
170
–25
0
25
50
75
100
Tc (°C)


Fc max vs. Tc
CXA1176AK
VEE = – 5.2V
Fc max (MSPS)
370
350
300
270
–25
0
25
50
75
100
Tc (°C)

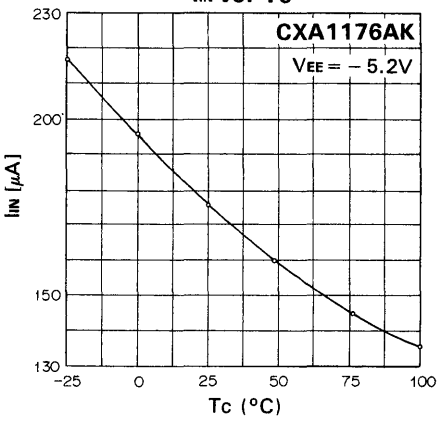

IEE vs. Tc
CXA1076AK
VEE = – 5.2V
IEE (mA)
400
300
200
–25
0
25
50
75
100
Tc (°C)


IEE vs. Tc
CXA1176AK
VEE = – 5.2V
IEE (mA)
400
300
200
–25
0
25
50
75
100
Tc (°C)

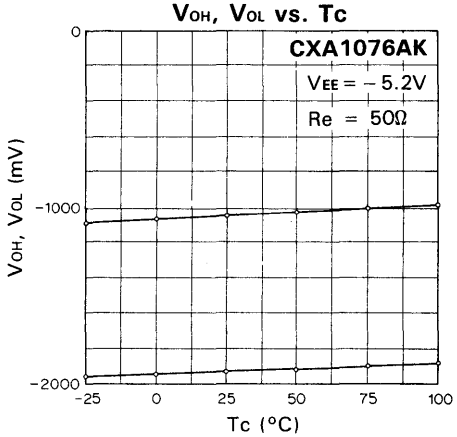
I_{IN} vs. Tc



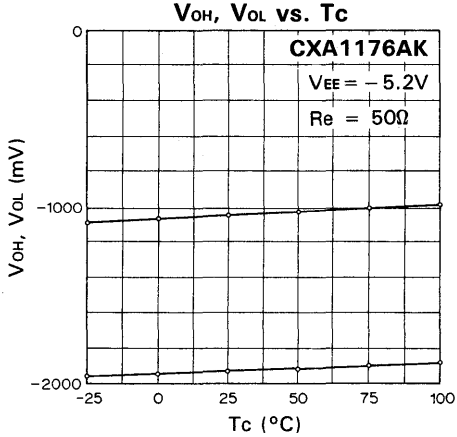
I_{IN} vs. Tc



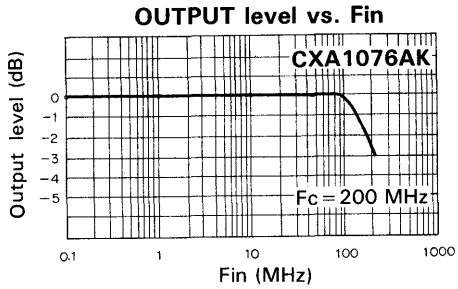
V_{OH}, V_{OL} vs. Tc



V_{OH}, V_{OL} vs. Tc



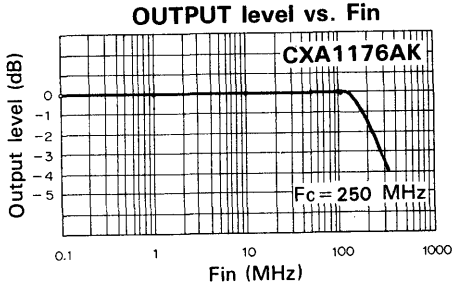
OUTPUT level vs. Fin



VEE = – 5.2V Ta = 25°C Vin = FS

Preliminary

OUTPUT level vs. Fin

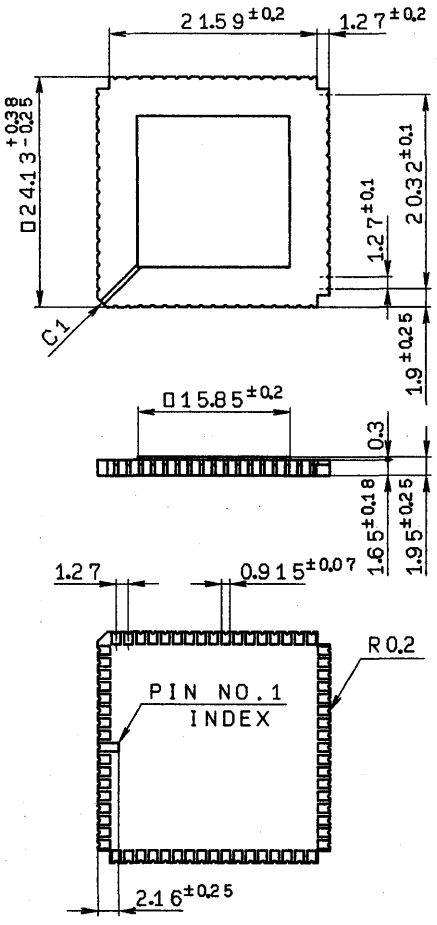


VEE = – 5.2V Ta = 25°C Vin = FS

Preliminary

Package Outline Unit: mm

68 pin LCC (Ceramic) 3.7 g



LCC-68C-01

SONY

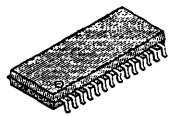
CXA1096M

8-bit 20 MSPS Flash A/D Converter (TTL I/O)

Description

The CXA1096M is an 8-bit 20 MSPS high speed A/D converter IC. This IC is suitable for a wide range of applications where A/D high speed operation is required.

28pin SOP(Plastic)



Features

- Resolution 8-bit ±1/2 LSB
- High speed operation 20MSPS
- Wide band analog input 8MHz (−3dB)
- Low input capacitance 30pF (Typ.)
- Low power consumption 390mW (Typ.)
- I/O level TTL
- Two ways of power supply (Single +5V or dual +5V/−5.2V)
- Sample and Hold amplifier not required
- Binary or Two's complement mode
- Over range output

Structure

Bipolar silicon monolithic IC

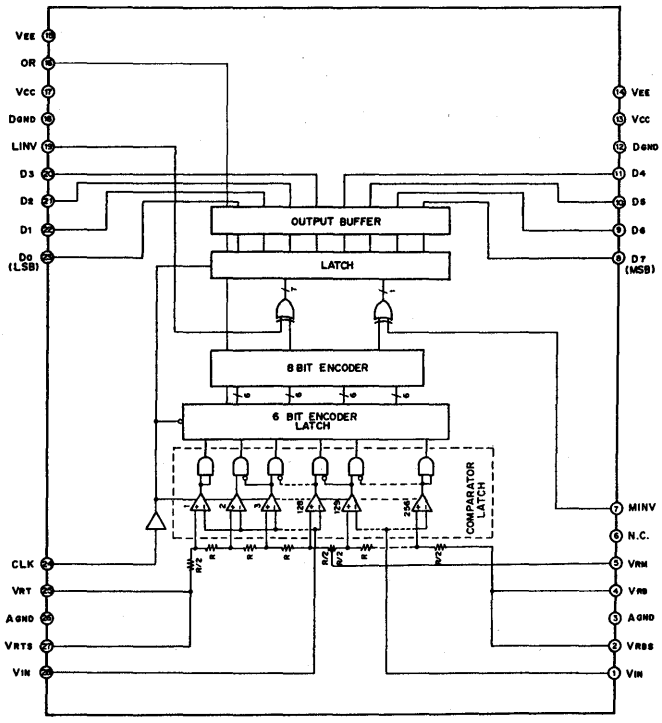
Applications

- Digital TV
- High speed signal processing

Function

8-bit, 20MSPS flash A/D converter

Block Diagram



E89645-HP

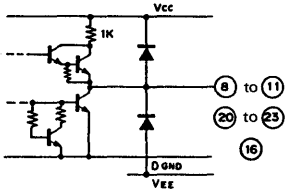
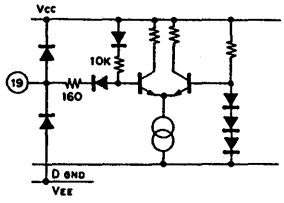
Absolute Maximum Ratings (Ta = 25°C)

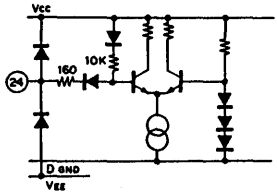
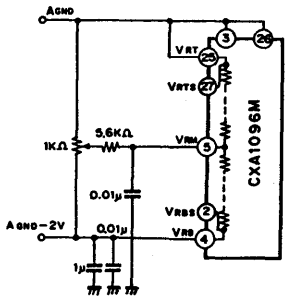
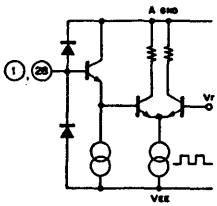
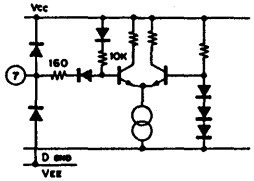
• Supply voltage	$V_{CC}-D_{GND}$	0 to +6	V
	$V_{EE}-A_{GND}$	0 to −6	V
	$A_{GND}-D_{GND}$	0 to +6	V
• Input voltage (analog)	V_{IN}	V_{EE} to A_{GND} +0.3	V
• Input voltage (reference)	V_{RT}, V_{RB}, V_{RM}	V_{EE} to A_{GND} +0.3	V
	$\lvert V_{RT} - V_{RB} \rvert$	2.5	V
• Input current (V_{RM})	I_{VRM}	−3 to +3	mA
• Input voltage (digital)	CLK, MINV, LINV	D_{GND}−0.5 to V_{CC}	V
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	0.83	W

Recommended Operating Conditions

• Supply voltage (Single supply)	V_{CC}, A_{GND}	4.75 to 5.25	V
	D_{GND}, V_{EE}	0	V
(Dual supply)	V_{CC}	4.75 to 5.25	V
	V_{EE}	−5.5 to −4.75	V
	D_{GND}, A_{GND}	0	V
• Reference input	V_{RT}	A_{GND} −0.1 to A_{GND} +0.1	V
	V_{RB}	A_{GND} −2.2 to A_{GND} −1.8	V
• Analog input	V_{IN}	V_{RB} to V_{RT}	
• Clock pulse width	T_{PW1}	35 (Min.)	ns
	T_{PW0}	10 (Min.)	ns
• Operating temperature	Topr	−20 to +75	°C

Pin Description and Equivalent Circuit

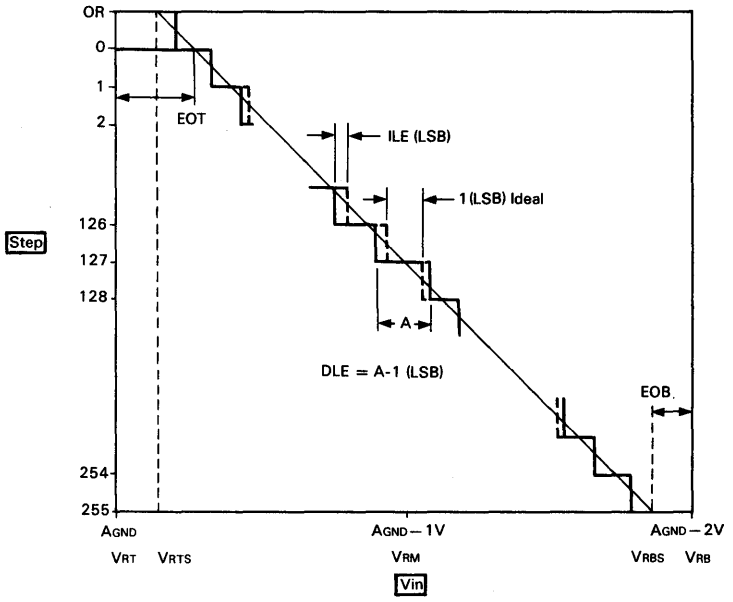
No.	Symbol	Voltage	Equivalent circuit	Description
8 to 11 20 to 23	D0 to D7	TTL		Digital data output pin D0 (LSB) to D7 (MSB)
16	OR			Over range output pin
12, 18	D_{GND}	GND		Digital GND. Separated from A_{GND}.
13, 17	V_{CC}	5V (Typ.)		Digital power supply
14, 15	V_{EE}	GND (Single supply) −5V (Dual supply)		Analog power supply
19	LINV	TTL		Input pins for output polarity inversion of D0 (LSB) to D6 (See the Input-Output Reference and Output Format) when open "1" is maintained.

No.	Symbol	Voltage	Equivalent circuit	Description
24	CLK	TTL		Clock input pin
25	VRT	5V (Typ.) (Single supply)		Reference voltage (Top)
27	VRTS	GND (Dual supply)		Reference voltage sense (Top)
4	VRB	3V (Typ.) (Single supply) −2V (Typ.) (Dual supply)		Reference voltage (Bottom)
2	VRBS			Reference voltage sense (Bottom)
5	VRM	4V (Typ.) (Single supply) −1V (Typ.) (Dual supply)		Middle point of reference voltage can be used as the compensation pin for linearity
3, 26	AGND	5V (Typ.) (Single supply) GND (Dual supply)		Analog power supply
1, 28	VIN	VRT to VRB		Analog input Pin 1 and 28 should be connected together.
7	MINV	TTL		Input pin for output polarity inversion of D7 (MSB) when open "1" is maintained.

Input-Output Reference and Output Format

Vin	Step	MINV 1 / LINV 1	1 / 0	0 / 1	0 / 0
		OR MSB ··· LSB	OR MSB ··· LSB	OR MSB ··· LSB	OR MSB ··· LSB
AGND		0 000···00	0 011···11	0 100···00	0 111···11
	0	1 000···00	1 011···11	1 100···00	1 111···11
	1	1 000···01	1 011···10	1 100···01	1 111···10
		. . .	. . .	. . .	. . .
AGND	127	1 011···11	1 000···00	1 111···11	1 100···00
−1V	128	1 100···00	1 111···11	1 000···00	1 011···11
		. . .	. . .	. . .	. . .
	254	1 111···10	1 100···01	1 011···10	1 000···01
AGND	255	1 111···11	1 100···00	1 011···11	1 000···00
−2V		. . .	. . .	. . .	. . .
		1 111···11	1 100···00	1 011···11	1 000···00

1: V_{IH}, V_{OH}
0: V_{IL}, V_{OL}



Electrical Characteristics (Single supply)

V_{CC} = +5V, DGND = 0V, AGND = +5V, V_{EE} = 0V,
V_{RT} = +5V, V_{RB} = +3V, Ta = 25°C

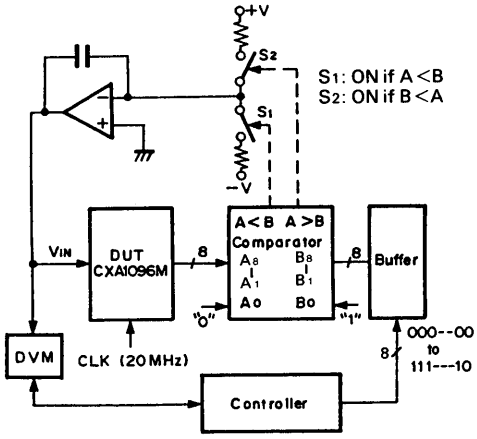
Item		Symbol	Test condition		Min.	Typ.	Max.	Unit
Maximum conversion rate		Fc	V_{IN} = 5 to 3V F_{IN} = Fc/4 − 1 kHz		20			MSPS
Supply current		I_{CC} + I_{EE}			56	71	91	mA
Reference pin current		I_{REF}			11	15	18	mA
Analog input bandwidth		BW			8			MHz
Analog input capacitance		C_{IN}	V_{IN} = 4V + 0.07Vms			30	35	pF
Analog input bias current		I_{IN}	V_{IN} = 4V		15	50	110	μA
Reference resistance (V_{RT} to V_{RB})		R_{REF}				130		Ω
Offset voltage	V_{RT}	E_{OT}			8	13	19	mV
	V_{RB}	E_{OB}			0	5	11	mV
Digital input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Digital input current		I_{IH}	V_{CC} = Max.	V_{IH} = 2.7V	0	−100	−150	μA
		I_{IL}		V_{IL} = 0.5V	−0.1	−0.32	−0.5	mA
Digital output voltage		V_{OH}	V_{CC} = Min.	I_{OH} = −500μA	2.7	3.4		V
		V_{OL}		I_{OL} = 3mA			0.5	V
Output data delay		T_{DLH}	LOAD 1		15	19	22	ns
		T_{DHL}			22	27	31	ns
Non linearity		E_L	Fc = 20 MSPS V_{IN} = 5 to 3V				±1/2	LSB
Differential non linearity		E_D					±1/2	LSB
Differential gain error		DG	NTSC 40 IRE mod. ramp, Fc = 14.3 MSPS				1.5	%
Differential phase error		DP					0.5	deg.
Aperture jitter		E_{AP}				30		ps
Sampling delay		tds			5	7	9	ns

Electrical Characteristics (Dual supply)

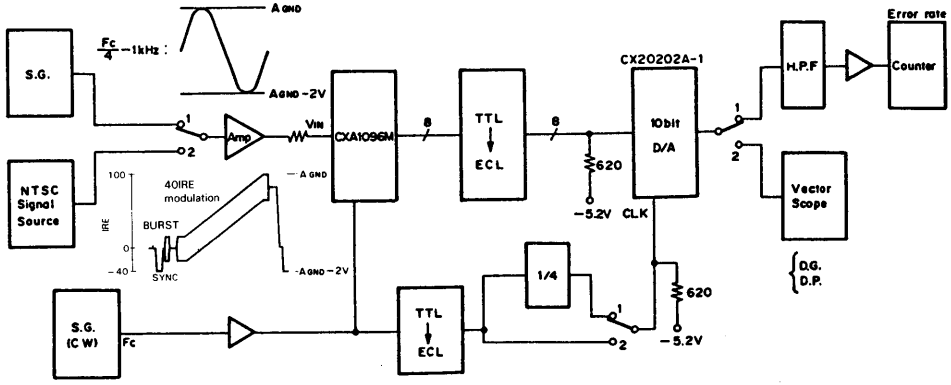
V_{CC} = +5V, DGND = 0V, AGND = 0V, V_{EE} = −5V, V_{RT} = 0V, V_{RB} = −2V, Ta = 25°C

Item		Symbol	Test condition		Min.	Typ.	Max.	Unit
Maximum conversion rate		Fc	V_{IN} = 0 to −2V F_{IN} = Fc/4 − 1 kHz		20			MSPS
Supply current		I_{CC}			7	10	14	mA
		I_{EE}			50	62	78	mA
Reference pin current		I_{REF}			11	15	18	mA
Analog input bandwidth		BW			8			MHz
Analog input capacitance		C_{IN}	V_{IN} = −1V + 0.07Vrms			30	35	pF
Analog input bias current		I_{IN}	V_{IN} = −1V		15	50	110	μA
Reference resistance (V_{RT} to V_{RB})		R_{REF}				130		Ω
Offset voltage	V_{RT}	E_{OT}			8	13	19	mV
	V_{RB}	E_{OB}			0	5	11	mV
Digital input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Digital input current		I_{IH}	V_{CC} = Max.	V_{IH} = 2.7V	0	−100	−150	μA
		I_{IL}		V_{IL} = 0.5V	−0.1	−0.32	−0.5	mA
Digital output voltage		V_{OH}	V_{CC} = Min.	I_{OH} = −500μA	2.7	3.4		V
		V_{OL}		I_{OL} = 3mA			0.5	V
Output data delay		T_{DLH}	LOAD 1		15	19	22	ns
		T_{DHL}			22	27	31	ns
Non linearity		EL	Fc = 20 MSPS V_{IN} = 0 to −2V				±1/2	LSB
Differential non linearity		ED					±1/2	LSB
Differential gain error		DG	NTSC 40 IRE mod. ramp, Fc = 14.3 MSPS				1.5	%
Differential phase error		DP					0.5	deg.
Aperture jitter		E_{AP}				30		ps
Sampling delay		tds			5	7	9	ns

Electrical Characteristics Test Circuit

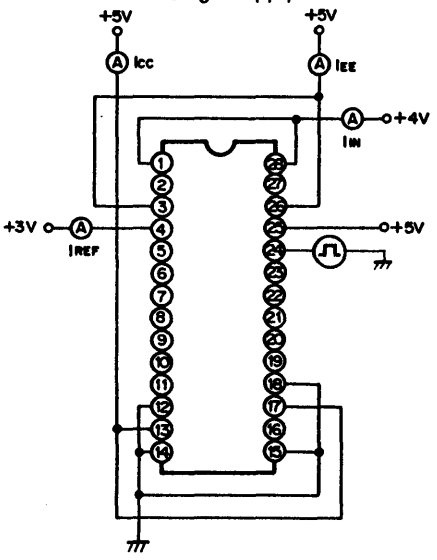


Non linearity
Differential non linearity
} Test circuit

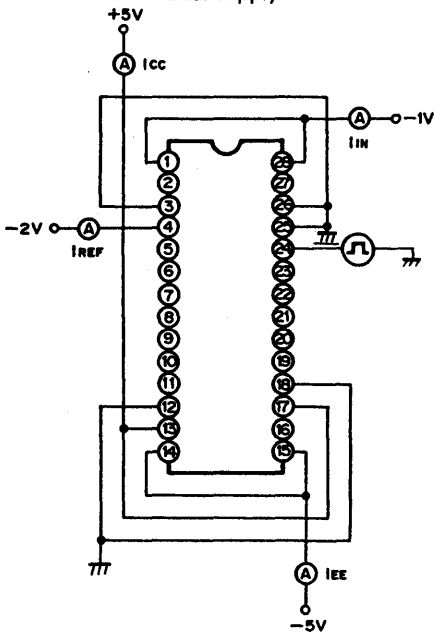


Maximum conversion rate
Differential gain error
Differential phase error
} Test circuit

Single supply

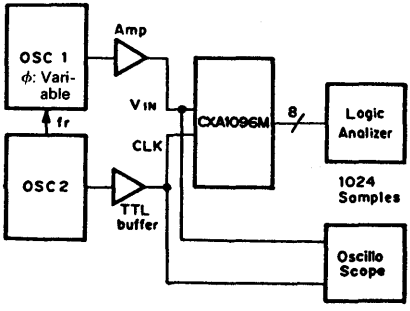


Dual supply

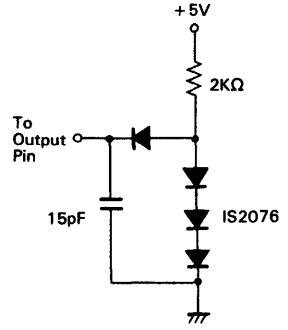


Note) VIN pin is connected to VRT pin for ICC and IEE measurement.

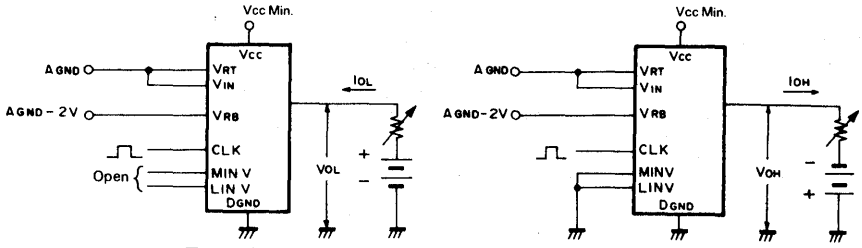
Supply current
Analog input bias current
Reference pin current
} Test circuit



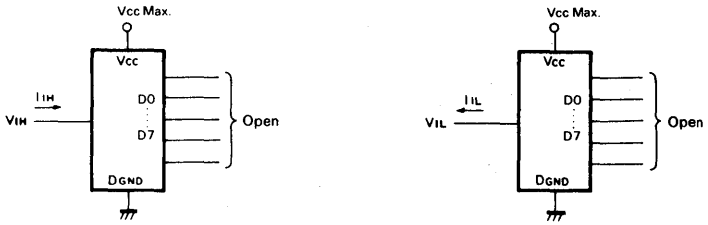
Aperture jitter
Sampling delay
} Test circuit



LOAD1 Test Load for Output data delay

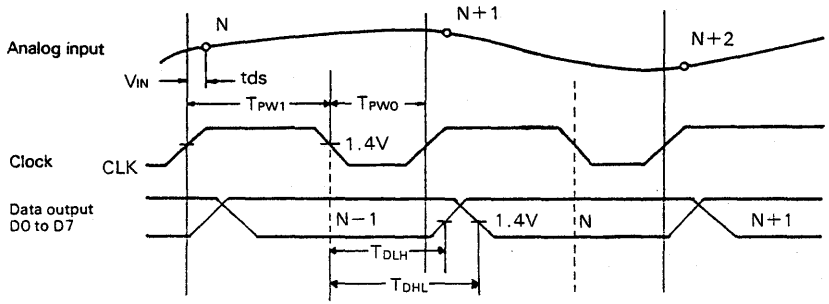


Test circuit of digital output voltage (DO to D7, OR)

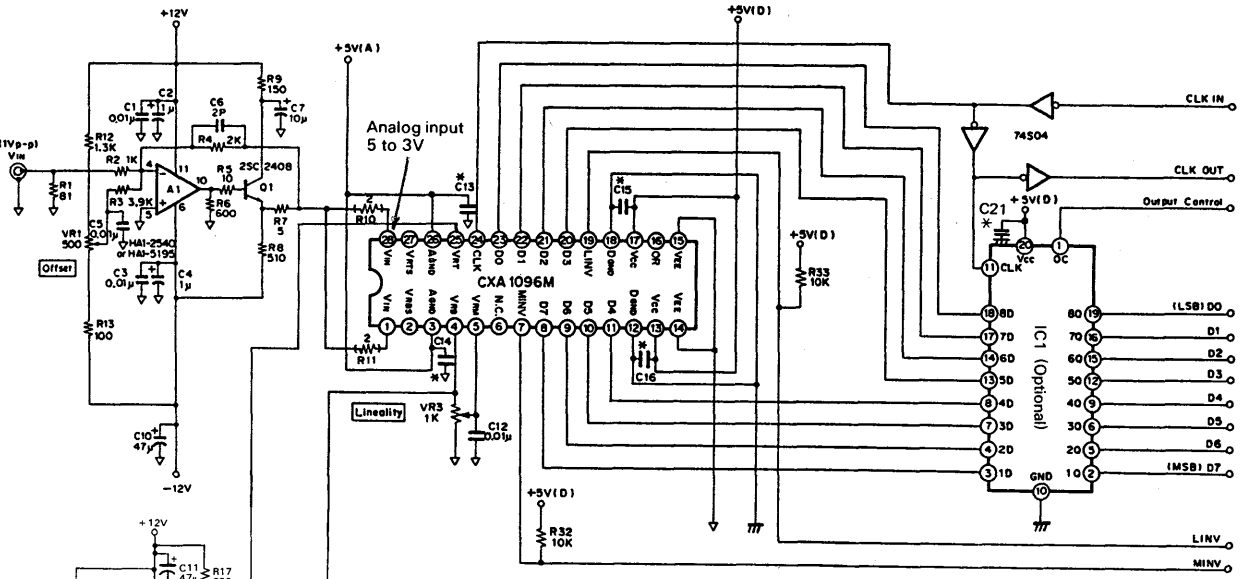


Test circuit of digital input current (CLK, MINV, LINV)

Timing Chart



Application Circuit (Single supply)



IC1 : 74S374 or 74ALS374

74LS374 is also available for 15 MSPS or less conversion rate.

A2 : LM301 or LM308

: Analog GND

: Digital GND

* : Ceramic Chip capacitor 0.01μF

: To be selected

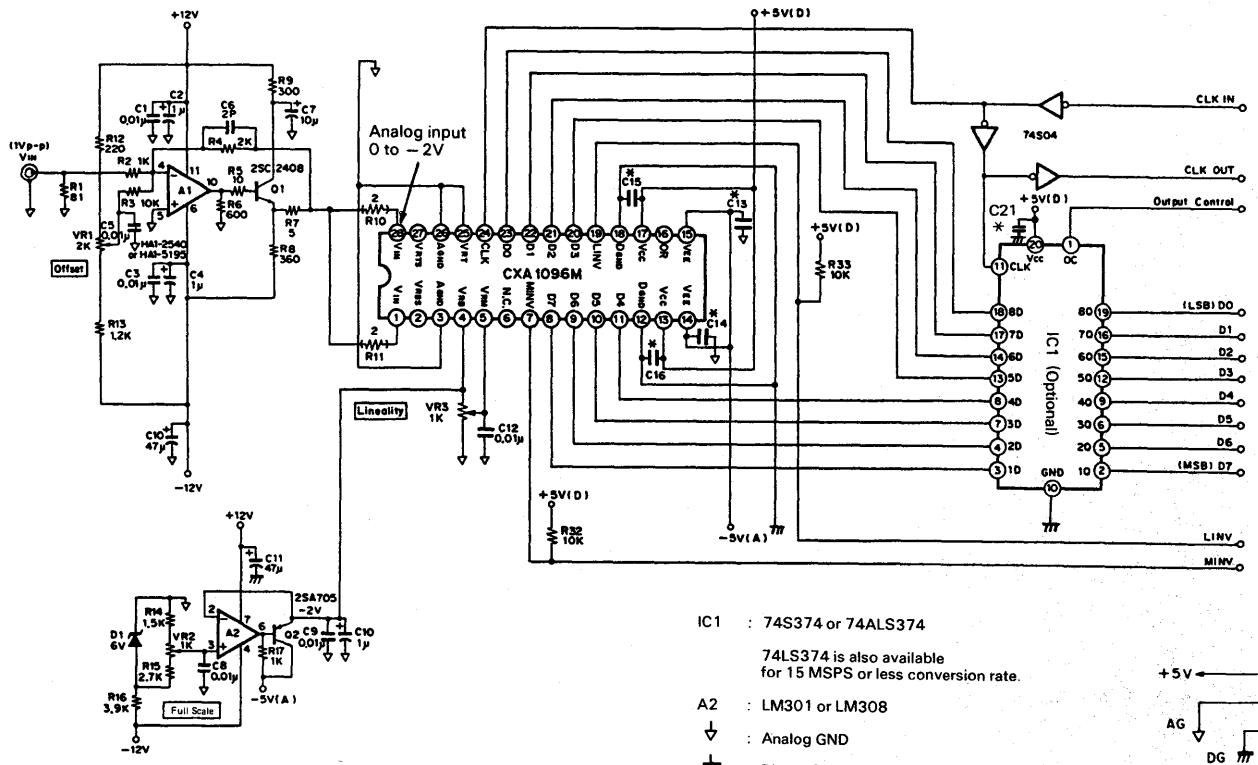
Q1 : 2SC2408 or 2N5836

Q2 : 2SC632A or 2N2222A

Q3 : 2SA705 or 2N2907A

+5V
AG
DG
+12V
-12V

Application Circuit (Dual supply)



IC1 : 74S374 or 74ALS374

74LS374 is also available for 15 MSPS or less conversion rate.

A2 : LM301 or LM308

: Analog GND

: Digital GND

* : Ceramic Chip capacitor 0.01μF

: To be selected

Q1 : 2SC2408 or 2N5836

Q2 : 2SA705 or 2N2907A

+5V
AG
DG
–5V
+12V
–12V

Notes on Application

1. Each of DGND pins (12, 18) and each of VCC Pins (13, 17) are divided in internal circuit. All of the pins should be connected to respective PCB patterns.

2. Layout of the analog and digital sections should be separated to reduce noise effect.
   VEE pins to AGND and VCC pins to DGND should be bypassed as closely as possible by means of 1μF and 0.01μF capacitors.
   For the 0.01μF, a ceramic chip capacitor should be used.

3. The input capacitance of the analog input is much smaller than that of the Flash Type A/D converters in use so far. It is necessary to use an amplifier with sufficient band width and driving power.
   Pins VIN (1, 28) are divided in it, so they should be connected together. When driving with a low output impedance amplifier, parasitic oscillation may occur. This can be prevented by introducing between the amplifier output and A/D input a small resistance of 2 to 10Ω with smaller inductance, in series. And, that also each VIN pins are divided with small resistances (shown in the Application Circuit) is effective.
   The amplifier output and A/D input should be connected as closely as possible.

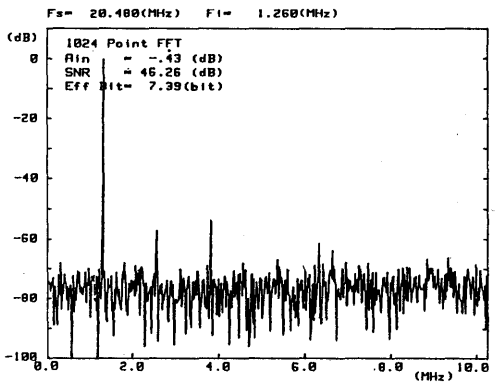
4. Voltage between VRT to VRB is equivalent to the dynamic range of the analog input. VRB pin should be bypassed to AGND by means of 1μF and 0.01μF capacitors.
   Through bypassing VRM pin with a 0.01μF capacitor to AGND, characteristics at high frequency become more balanced. Also, VRM pin can be used as a trimming pin for more precise linearity compensation.

5. CLK line should be wired in short distance and that should be separated from the other section to reduce the inductive.

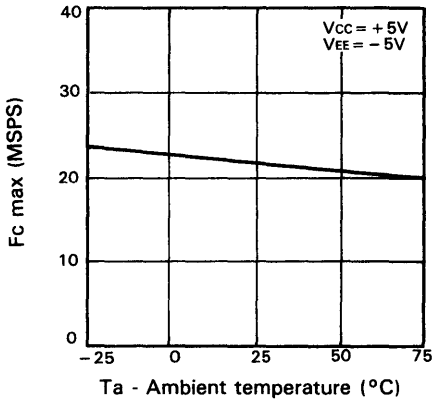
6. Analog input signal is sampled at the positive going edge of the CLK, and a corresponding digital data appears to the output parts at the negative going edge with a short delay time (TDLH, TDHL).
   If digital data will be latched externally, it should be latched at the negative going edge. (See the Timing Chart)

7. It is recommended to connect free pins to AGND for prevention of noise effect.

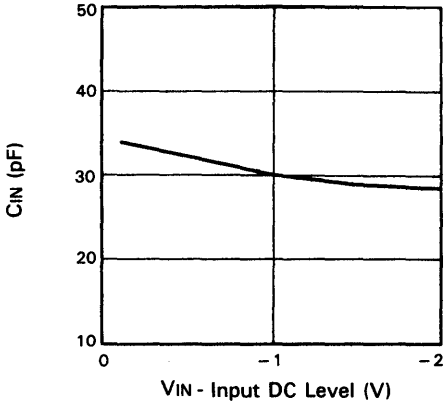
FFT data



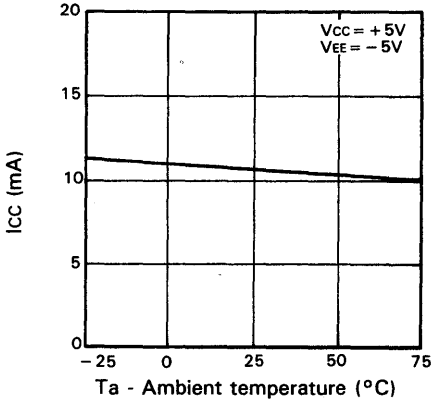
Fc max vs. Ambient temperature



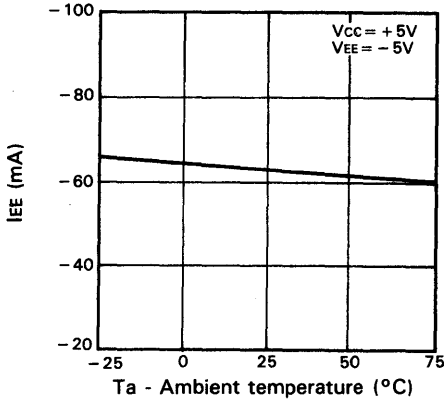
CIN vs. VIN - Input DC level



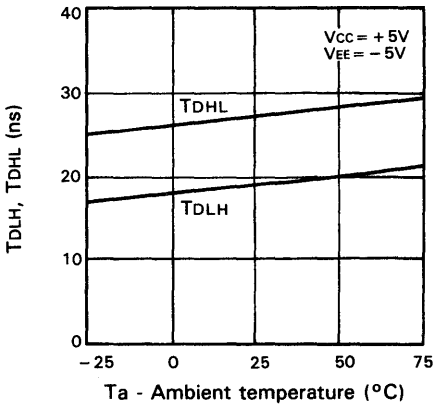
ICC vs. Ambient temperature



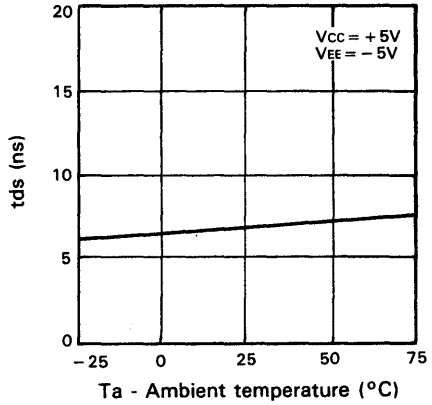
IEE vs. Ambient temperature

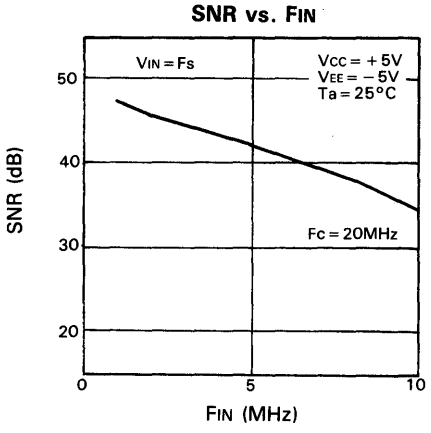


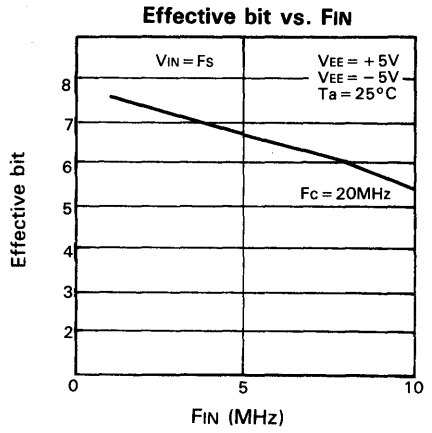
TDLH, TDHL vs. Ambient temperature



tds vs. Ambient temperature

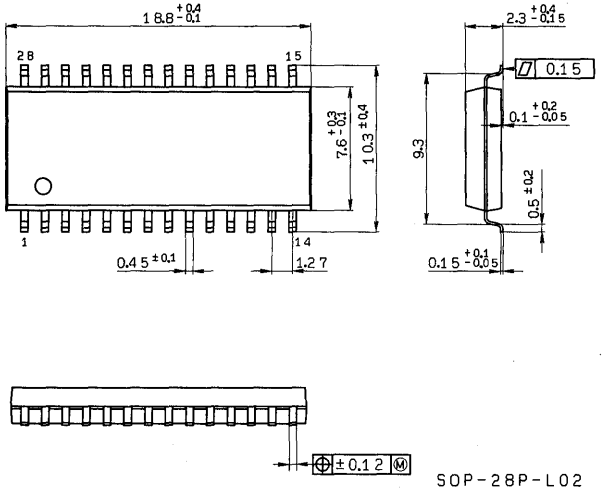






Package Outline Unit : mm

28pin SOP(Plastic) 375mil 0.6g



SONY

CXA1096P

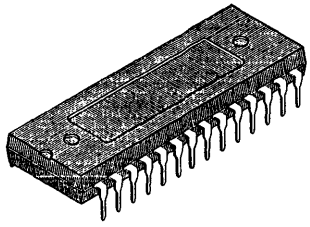
8-bit 20 MSPS Flash A/D Converter (TTL I/O)

Evaluation Board Available — CXA1096PPCB

Description

CXA1096P is an 8-bit 20 MSPS high speed A/D converter IC. This IC is suitable for a wide range of applications where A/D high speed operation is required.

28pin DIP(Plastic)



Features

• Resolution	8-bit ±1/2 LSB
• High speed operation	20MSPS
• Wide band analog input	8MHz (−3dB)
• Low input capacitance	30pF (Typ.)
• Low power consumption	390mW (Typ.)
• I/O level	TTL

- Two ways of power supply (Single +5V or dual +5V/−5.2V)
- Sample and Hold amplifier not required
- Binary or Two's complement mode
- Pin replacable with TDC1048 (TRW)

Main difference from CXA1296P is that digital output is synchronized with the falling edge of clock, instead of rising edge.

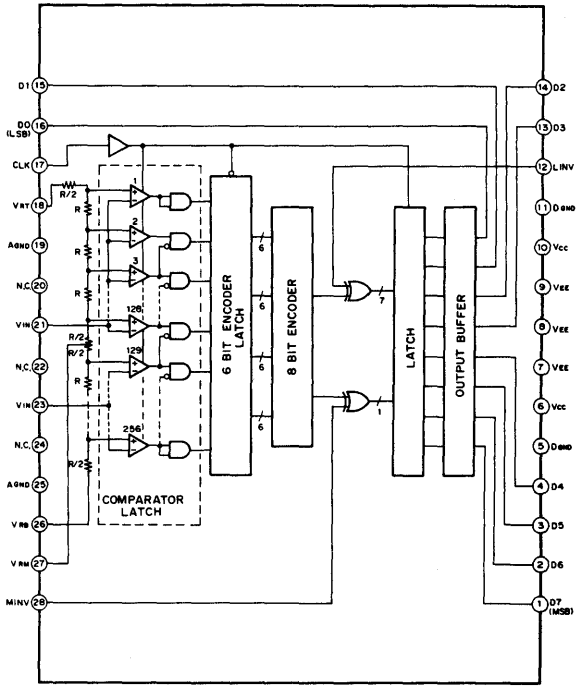
Structure

Bipolar silicon monolithic IC

Applications

- Digital TV
- High speed signal processing

Block Diagram



E89646-HP

Absolute Maximum Ratings (Ta = 25°C)

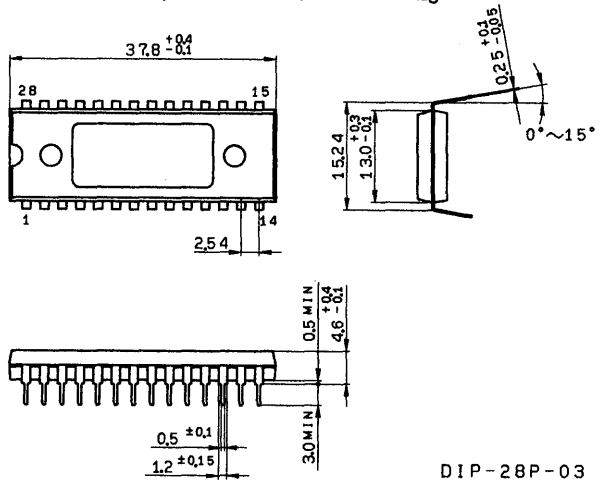
• Supply voltage	$V_{CC}-D_{GND}$	0 to +6	V
	$V_{EE}-A_{GND}$	0 to −6	V
	$A_{GND}-D_{GND}$	0 to +6	V
• Input voltage(analog)	V_{IN}	V_{EE} to A_{GND} +0.3	V
• Input voltage (reference)	V_{RT}, V_{RB}, V_{RM}	V_{EE} to A_{GND} +0.3	V
	$\lvert V_{RT} - V_{RB} \rvert$	2.5	V
• Input current (V_{RM})	I_{VRM}	−3 to +3	mA
• Input voltage (digital)	CLK, MINV, LINV	D_{GND}−0.5 to V_{CC}	V
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	1.48	W

Recommended Operating Conditions

• Supply voltage (Single supply)	V_{CC}, A_{GND}	4.75to5.25	V
	D_{GND}, V_{EE}	0	V
(Dual supply)	V_{CC}	4.75 to 5.25	V
	V_{EE}	−5.5 to −4.75	V
	D_{GND}, A_{GND}	0	V
• Reference input	V_{RT}	A_{GND} −0.1 to A_{GND} +0.1	V
	V_{RB}	A_{GND} −2.2 to A_{GND} −1.8	V
• Analog input	V_{IN}	V_{RB} to V_{RT}	
• Clock pulse width	T_{PW1}	35 (Min.)	ns
	T_{PW0}	10 (Min.)	ns
• Operating temperature	Topr	−20 to +75	°C

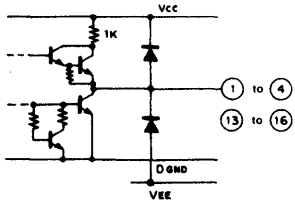
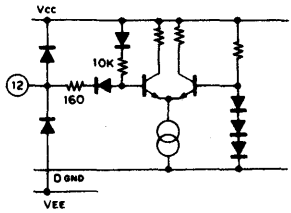
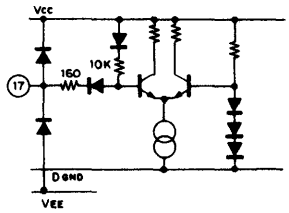
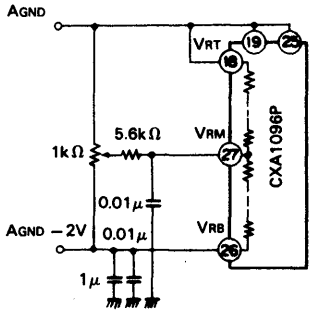
Package Outline Unit : mm

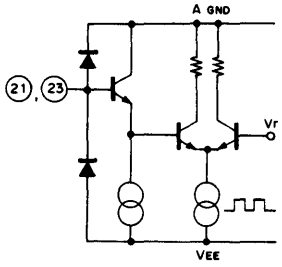
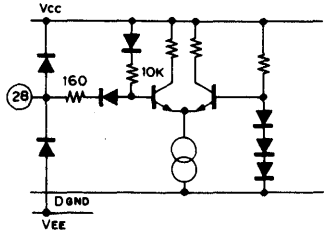
28pin DIP(Plastic) 600mil 4.2g



DIP-28P-03

Pin Description and Equivalent Circuit

No.	Symbol	Voltage	Equivalent circuit	Description
1 to 4 13 to 16	D0 to D7	TTL		Digital data output pin D0 (LSB) to D7 (MSB)
5, 11	DGND	GND		Digital GND. Separated from AGND.
6, 10	Vcc	5V (Typ.)		Digital power supply
7,8,9	VEE	GND (Single supply) −5V (Dual supply)		Analog power supply
12	LINV	TTL		Input pins for output polarity inversion of D0 (LSB) to D6 (See the Output Coding) when open "1" is maintained.
17	CLK	TTL		Clock input pin
18	VRT	5V (Typ.) (Single supply) GND (Dual supply)		Reference voltage (Upper level)
26	VRB	3V (Typ.) (Single supply) −2V (Typ.) (Dual supply)		Reference voltage (Lower level)
27	VRM	4V (Typ.) (Single supply) −1V (Typ.) (Dual supply)		Middle point of reference voltage can be used as the compensation pin for linearity

No.	Symbol	Voltage	Equivalent circuit	Description
19, 25	AGND	5V (Typ.) (Single supply) GND (Dual supply)		Analog power supply
21, 23	VIN	VRT to VRB		Analog input Pin 21 and 23 should be connected together.
28	MINV	TTL		Input pin for output polarity inversion of D7 (MSB) when open "1" is maintained.

Output Coding

MINV	0	0	1	1
LINV	0	1	0	1
AGND	111...11	100...00	011...11	000...00
.	111...10	100...01	011...10	000...01
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
V_{IN} .	100...00	111...11	000...00	011...11
.	011...11	000...00	111...11	100...00
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	000...01	011...10	100...01	111...10
AGND-2V	000...00	011...11	100...00	111...11

1 : V_{IH}, V_{OH}
0 : V_{IL}, V_{OL}

Electrical Characteristics (Single supply)

V_{CC} = +5V, DGND = 0V, AGND = +5V, V_{EE} = 0V,
V_{RT} = +5V, V_{RB} = +3V, Ta = 25°C

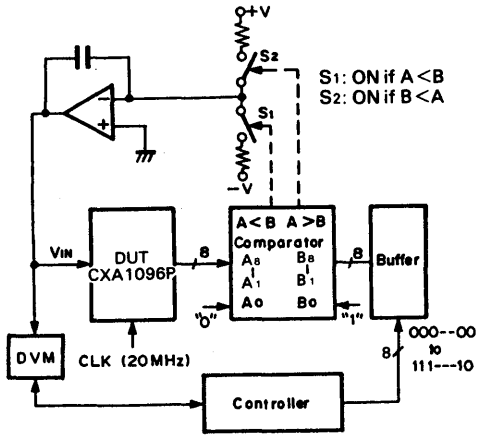
Item		Symbol	Test condition		Min.	Typ.	Max.	Unit
Maximum conversion rate		Fc	V_{IN} = 5 to 3V F_{IN} = Fc/4 − 1 kHz		20			MSPS
Supply current		I_{CC} + I_{EE}			56	71	91	mA
Reference pin current		I_{REF}			11	15	18	mA
Analog input bandwidth		BW			8			MHz
Analog input capacitance		C_{IN}	V_{IN} = 4V + 0.07Vms			30	35	pF
Analog input bias current		I_{IN}	V_{IN} = 4V		15	50	110	μA
Reference resistance (V_{RT} to V_{RB})		R_{REF}				130		Ω
Offset voltage	V_{RT}	E_{OT}			8	13	19	mV
	V_{RB}	E_{OB}			0	5	11	mV
Digital input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Digital input current		I_{IH}	V_{CC} = Max.	V_{IH} = 2.7V	0	−100	−150	μA
		I_{IL}		V_{IL} = 0.5V	−0.1	−0.32	−0.5	mA
Digital output voltage		V_{OH}	V_{CC} = Min.	I_{OH} = −500μA	2.7	3.4		V
		V_{OL}		I_{OL} = 3mA			0.5	V
Output data delay		T_{DLH}	LOAD 1		15	19	22	ns
		T_{DHL}			22	27	31	ns
Non linearity		EL	Fc = 20 MSPS V_{IN} = 5 to 3V				±1/2	LSB
Differential non linearity		ED	Fc = 20 MSPS				±1/2	LSB
Differential gain error		DG	NTSC 40 IRE mod. ramp, Fc = 14.3 MSPS				1.5	%
Differential phase error		DP					0.5	deg.
Aperture jitter		E_{AP}				30		ps
Sampling delay		tds			5	7	9	ns

Electrical Characteristics (Dual supply)

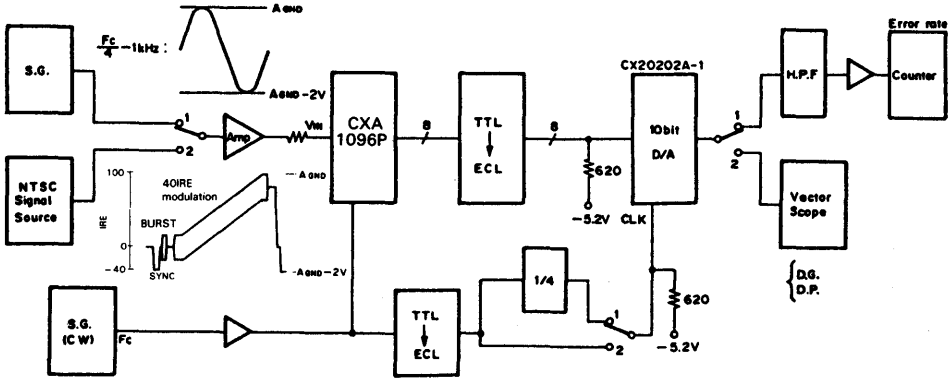
V_{CC} = +5V, DGND = 0V, AGND = 0V, V_{EE} = −5V, V_{RT} = 0V, V_{RB} = −2V, Ta = 25°C

Item		Symbol	Test condition		Min.	Typ.	Max.	Unit
Maximum conversion rate		Fc	V_{IN} = 0 to −2V F_{IN} = Fc/4 − 1 kHz		20			MSPS
Supply current		I_{CC}			7	10	14	mA
		I_{EE}			50	62	78	mA
Reference pin current		I_{REF}			11	15	18	mA
Analog input bandwidth		BW			8			MHz
Analog input capacitance		C_{IN}	V_{IN} = −1V + 0.07Vms			30	35	pF
Analog input bias current		I_{IN}	V_{IN} = −1V		15	50	110	μA
Reference resistance (V_{RT} to V_{RB})		R_{REF}				130		Ω
Offset voltage	V_{RT}	E_{OT}			8	13	19	mV
	V_{RB}	E_{OB}			0	5	11	mV
Digital input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Digital input current		I_{IH}	V_{CC} = Max.	V_{IH} = 2.7V	0	−100	−150	μA
		I_{IL}		V_{IL} = 0.5V	−0.1	−0.32	−0.5	mA
Digital output voltage		V_{OH}	V_{CC} = Min.	I_{OH} = −500μA	2.7	3.4		V
		V_{OL}		I_{OL} = 3mA			0.5	V
Output data delay		T_{DLH}	LOAD 1		15	19	22	ns
		T_{DHL}			22	27	31	ns
Non linearity		E_L	Fc = 20 MSPS V_{IN} = 0 to −2V				±1/2	LSB
Differential non linearity		E_D	Fc = 20 MSPS				±1/2	LSB
Differential gain error		DG	NTSC 40 IRE mod. ramp, Fc = 14.3 MSPS				1.5	%
Differential phase error		DP					0.5	deg.
Aperture jitter		E_{AP}				30		ps
Sampling delay		tds			5	7	9	ns

Electrical Characteristics Test Circuit

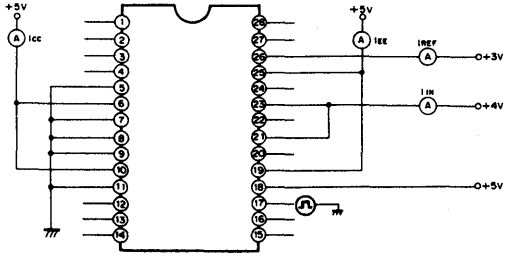


Non linearity
Differential non linearity } Test circuit

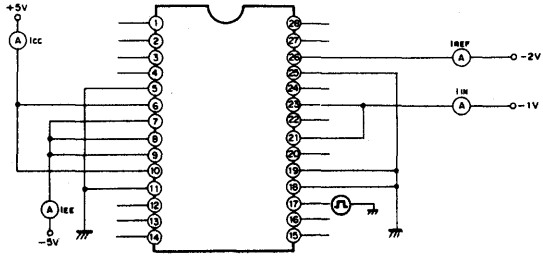


Maximum conversion rate
Differential gain error
Differential phase error } Test circuit

Single supply

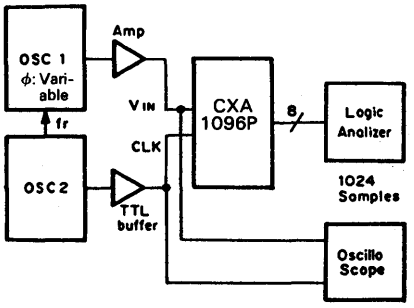


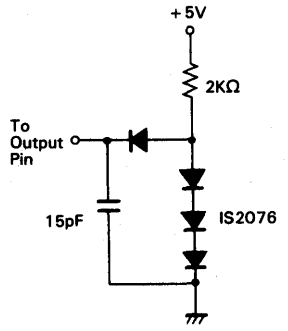
Dual supply



Supply current
Analog input bias current
Reference pin current } Test circuit

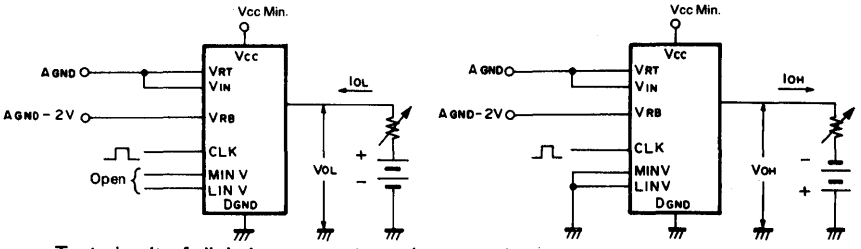
Note) VIN pin is connected to VRT pin for ICC and IEE measurement.



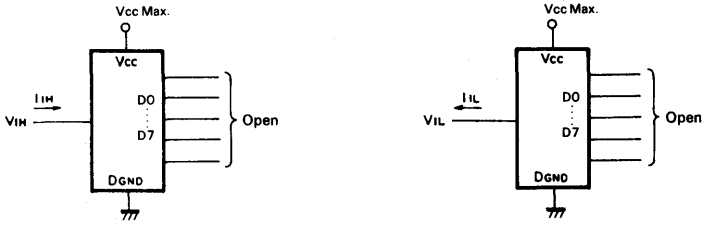


LOAD1 Test Load for Output data delay

Aperture jitter
Sampling delay
} Test circuit

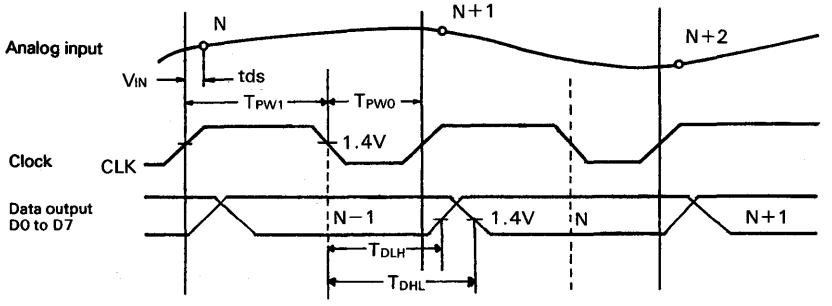


Test circuit of digital output voltage (D0 to D7)

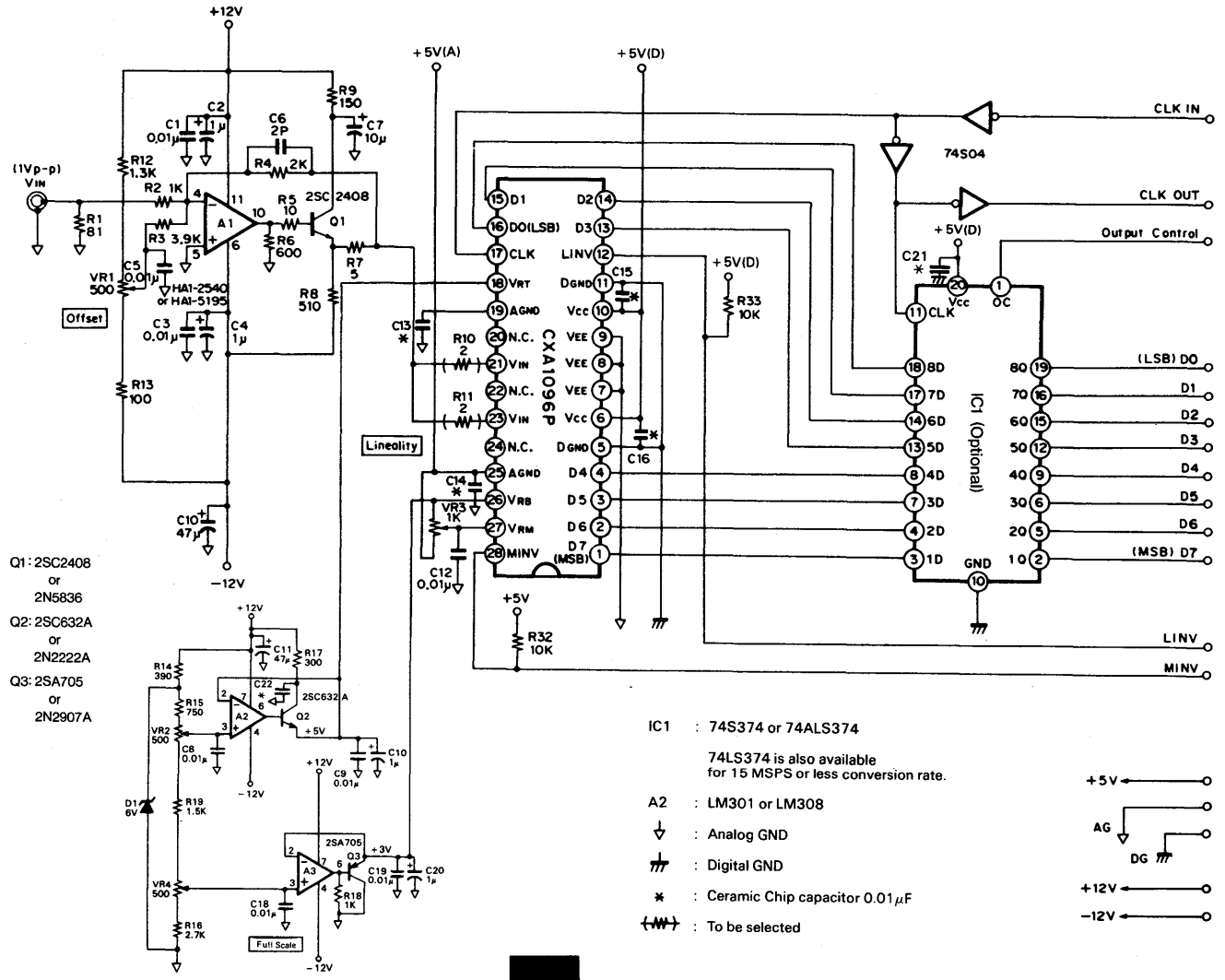


Test circuit of digital input current (CLK, MINV, LINV)

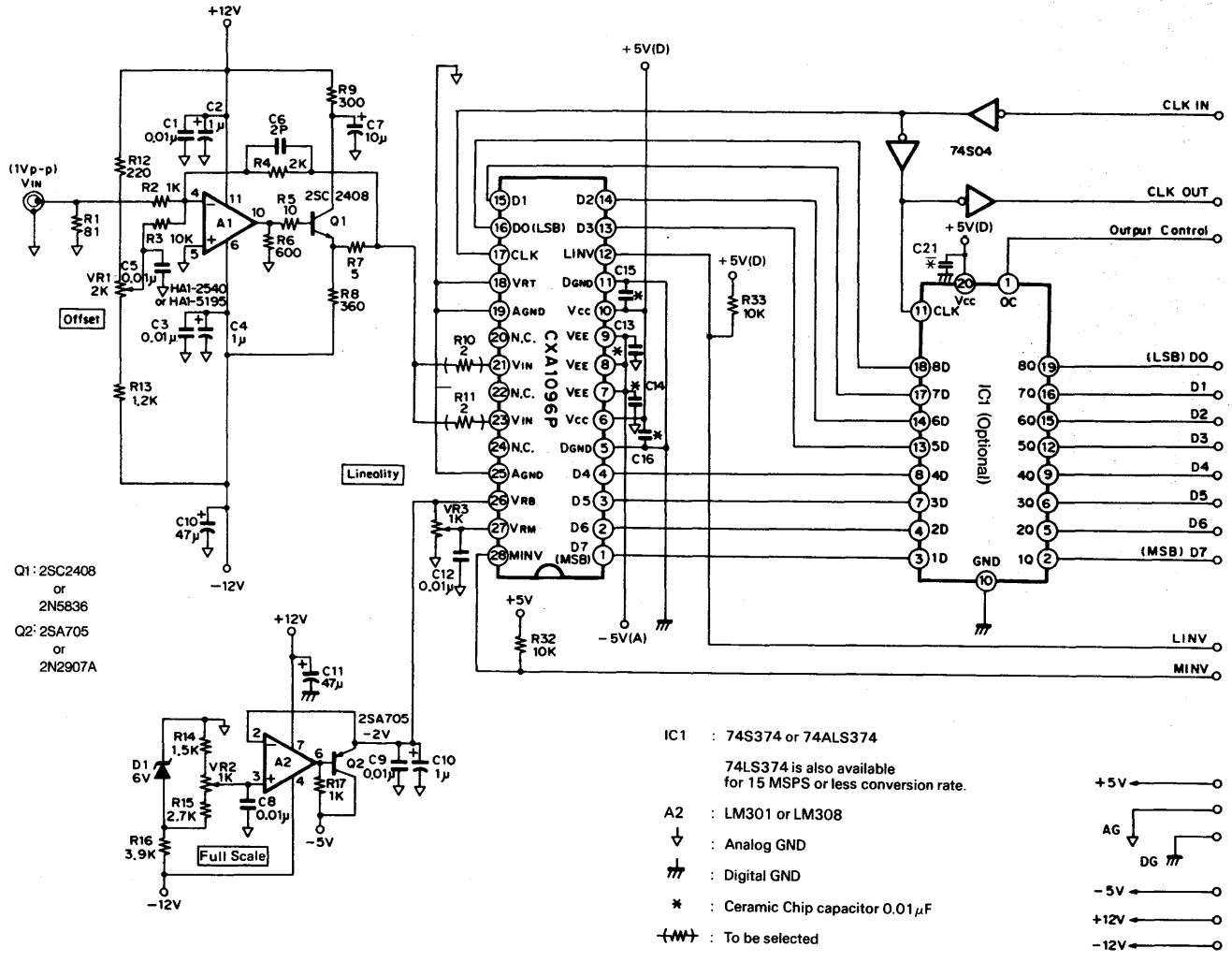
Timing Chart



Application Circuit (Single supply)



Application Circuit (Dual supply)



IC1 : 74S374 or 74ALS374

74LS374 is also available for 15 MSPS or less conversion rate.

A2 : LM301 or LM308

: Analog GND

: Digital GND

* : Ceramic Chip capacitor 0.01 μF

: To be selected

+5V
AG
DG
−5V
+12V
−12V

Notes on Application

1. Each of DGND pins (5, 11) and each of VCC Pins (6, 10) are divided in internal circuit. All of the pins should be connected to respective PCB patterns.

2. Layout of the analog and digital sections should be separated to reduce noise effect.
   VEE pins to AGND and VCC pins to DGND should be bypassed as closely as possible by means of 1μF and 0.01μF capacitors.
   For the 0.01μF, a ceramic chip capacitor should be used.

3. The input capacitance of the analog input is much smaller than that of the Flash Type A/D converters in use so far. It is necessary to use an amplifier with sufficient band width and driving power.
   Pins VIN (21, 23) are divided in it, so they should be connected together. When driving with a low output impedance amplifier, parasitic oscillation may occur. This can be prevented by introducing between the amplifier output and A/D input a small resistance of 2 to 10Ω with smaller inductance, in series. And, that also each VIN pins are divided with small resistances (shown in the Application Circuit) is effective.
   The amplifier output and A/D input should be connected as closely as possible.

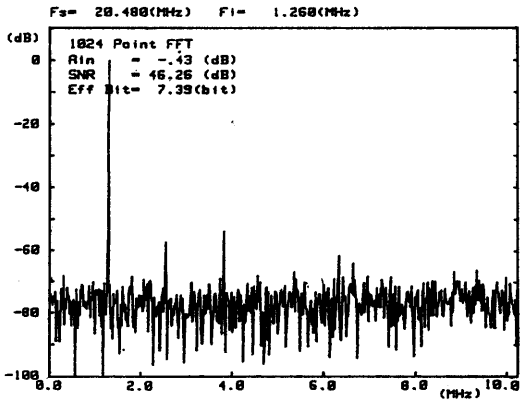
4. Voltage between VRT to VRB is equivalent to the dynamic range of the analog input. VRB pin should be bypassed to AGND by means of 1μF and 0.01μF capacitors.
   Through bypassing VRM pin with a 0.01μF capacitor to AGND, characteristics at high frequency become more balanced. Also, VRM pin can be used as a trimming pin for more precise linearity compensation.

5. CLK line should be wired in short distance and that should be separated from the other section to reduce the inductive.

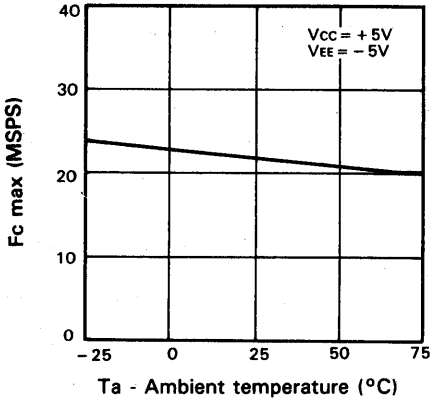
6. Analog input signal is sampled at the positive going edge of the CLK, and a corresponding digital data appears to the output parts at the negative going edge with a short delay time (TDLH, TDHL).
   If digital data will be latched externally, it should be latched at the negative going edge. (See the Timing Chart)

7. It is recommended to connect free pins to AGND for prevention of noise effect.

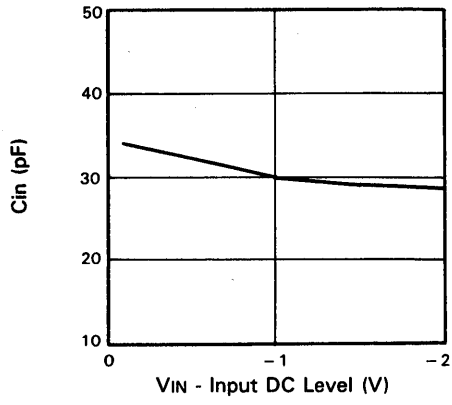
FFT Data



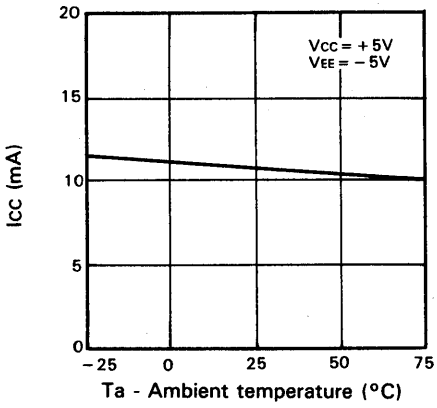
Fc max vs. Ambient temperature



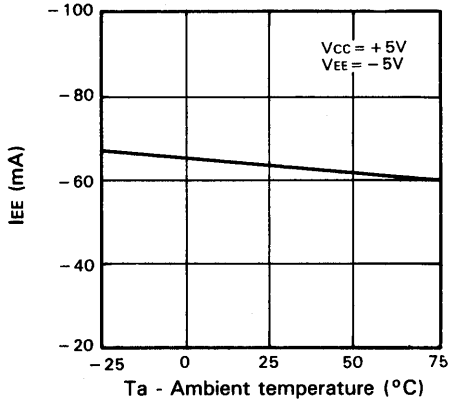
CIN vs. VIN - Input DC level



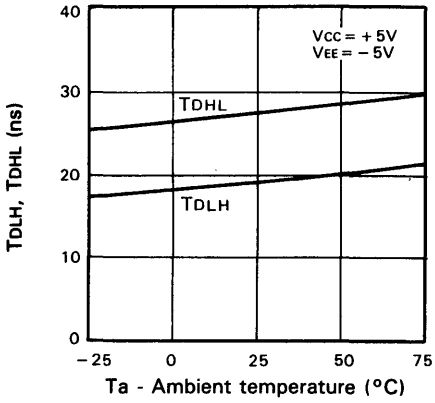
ICC vs. Ambient temperature



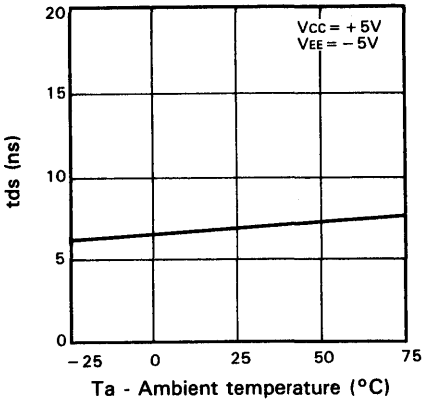
IEE vs. Ambient temperature



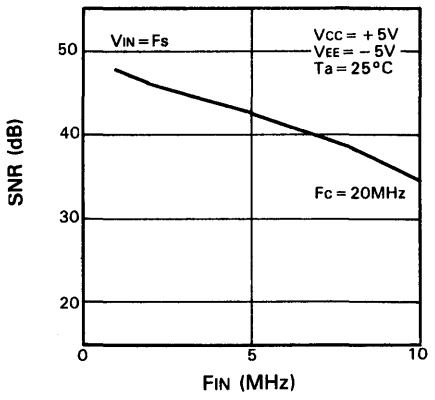
TDLH, TDHL vs. Ambient temperature



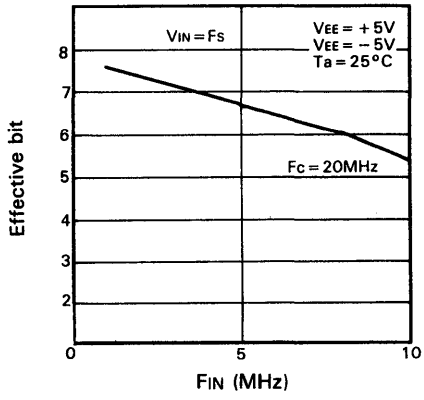
tds vs. Ambient temperature



SNR vs. FIN



Effective bit vs. FIN



SONY CXA1296P

8-bit 20 MSPS Flash A/D Converter (TTL I/O)

Evaluation Board Available — CXA1296P PCB

Description

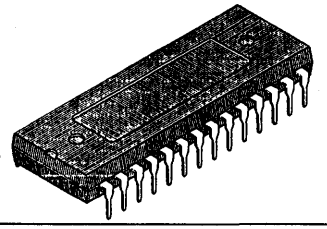
CXA1296P is an 8-bit 20 MSPS high speed A/D converter IC. This IC is suitable for a wide range of applications where A/D high speed operation is required.

Features

- Resolution 8-bit ±1/2 LSB
- High speed operation 20MSPS
- Wide band analog input 8MHz (−3dB)
- Low input capacitance 30pF (Typ.)
- Low power consumption 400mW (Typ.)
- I/O level TTL
- Two ways of power supply (Single +5V or dual +5V/−5.2V)
- Sample and Hold amplifier not required
- Binary or Two's complement mode
- Pin replaceable with TDC1048 (TRW)

Main difference from CXA1096P is that digital output is synchronized with the rising edge of clock, instead of falling edge.

28pin DIP (Plastic)



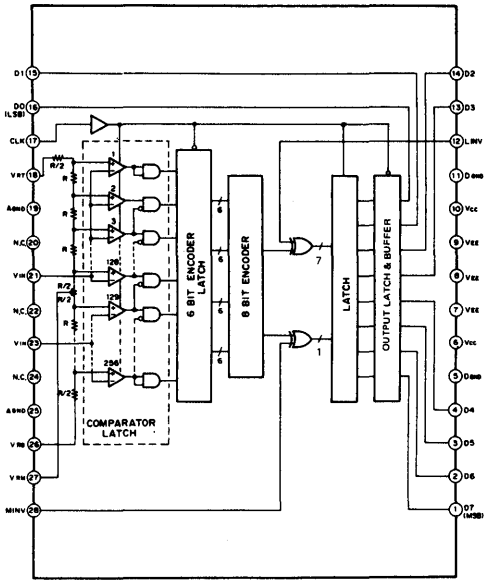
Structure

Bipolar silicon monolithic IC

Applications

- Digital TV
- High speed signal processing

Block Diagram



E89214A96-HP

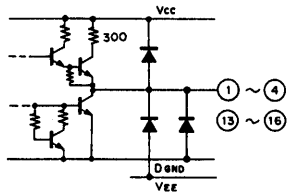
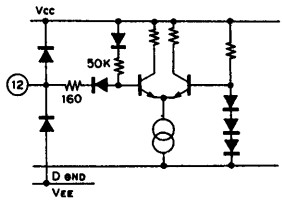
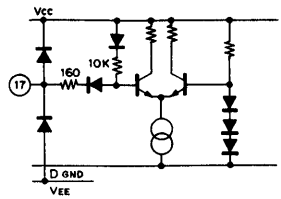
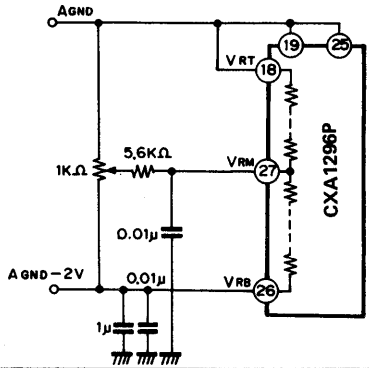
Absolute Maximum Ratings (Ta = 25°C)

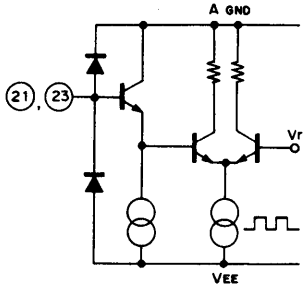
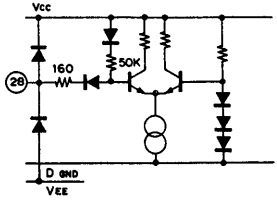
• Supply voltage	$V_{CC}-D_{GND}$	0 to +6	V
	$V_{EE}-A_{GND}$	0 to −6	V
	$A_{GND}-D_{GND}$	0 to +6	V
• Input voltage (analog)	V_{IN}	V_{EE} to A_{GND} +0.3	V
• Input voltage (reference)	V_{RT}, V_{RB}, V_{RM}	V_{EE} to A_{GND} +0.3	V
	$\lvert V_{RT} - V_{RB} \rvert$	2.5	V
• Input current (V_{RM})	I_{VRM}	−3 to +3	mA
• Input voltage (digital)	CLK, MINV, LINV D_{GND}	−0.5 to V_{CC}	V
• Storage temperature	Tstg	−65 to +150	°C
• Allowable power dissipation	P_D	1.48	W

Recommended Operating Conditions

• Supply voltage	V_{CC}, A_{GND}	4.75 to 5.25	V
(Single supply)	D_{GND}, V_{EE}	0	V
(Dual supply)	V_{CC}	4.75 to 5.25	V
	V_{EE}	−5.5 to −4.75	V
	D_{GND}, A_{GND}	0	V
• Reference input	V_{RT}	A_{GND} −0.1 to A_{GND} +0.1	V
	V_{RB}	A_{GND} −2.2 to A_{GND} −1.8	V
• Analog input	V_{IN}	V_{RB} to V_{RT}	
• Clock pulse width	T_{PW1}	35 (Min.)	ns
	T_{PW0}	10 (Min.)	ns
• Operating temperature	Topr	−20 to +75	°C

Pin Description and Equivalent Circuit

No.	Symbol	Voltage	Equivalent circuit	Description
1 to 4 13 to 16	D0 to D7	TTL		Digital data output pin D0 (LSB) to D7 (MSB)
5, 11	DGND	GND		Digital GND. Separated from AGND.
6, 10	Vcc	5V (Typ.)		Digital power supply
7, 8, 9	VEE	GND (Single supply) – 5V (Dual supply)		Analog power supply
12	LINV	TTL		Input pins for output polarity inversion of D0 (LSB) to D6 (See the Output Coding) when open "1" is maintained.
17	CLK	TTL		Clock input pin
18	VRT	5V (Typ.) (Single supply) GND (Dual supply)		Reference voltage (Upper level)
26	VRB	3V (Typ.) (Single supply) – 2V (Typ.) (Dual supply)		Reference voltage (Lower level)
27	VRM	4V (Typ.) (Single supply) – 1V (Typ.) (Dual supply)		Middle point of reference voltage can be used as the compensation pin for linearity.

No.	Symbol	Voltage	Equivalent circuit	Description
19, 25	AGND	5 V (Typ.) (Single supply) GND (Dual supply)		Analog power supply
21, 23	VIN	VRT to VRB		Analog input Pin 21 and 23 should be connected together.
28	MINV	TTL		Input pin for output polarity inversion of D7 (MSB) when open "1" is maintained.

Output Coding

MINV LINV	0 0	0 1	1 0	1 1
AGND	111 . . . 11	100 . . . 00	011 . . . 11	000 . . . 00
.	111 . . . 10	100 . . . 01	011 . . . 10	000 . . . 01
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
VIN .	100 . . . 00	111 . . . 11	000 . . . 00	011 . . . 11
.	011 . . . 11	000 . . . 00	111 . . . 11	100 . . . 00
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	000 . . . 01	011 . . . 10	100 . . . 01	111 . . . 10
AGND-2V	000 . . . 00	011 . . . 11	100 . . . 00	111 . . . 11

1: VIH, VOH
0: VIL, VOL

Electrical Characteristics
(Single supply)

V_{CC} = +5V, DGND = 0V, AGND = +5V, V_{EE} = 0V,
V_{RT} = +5V, V_{RB} = +3V, Ta = 25°C

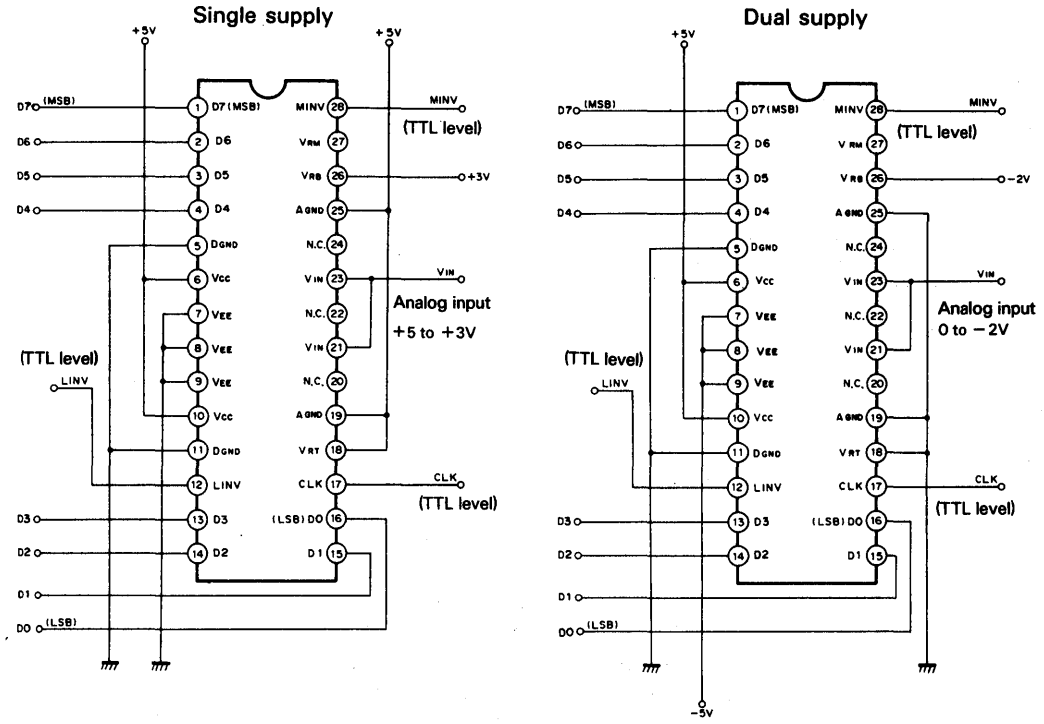
Item		Symbol	Test condition		Min.	Typ.	Max.	Unit
Maximum conversion rate		Fc	V_{IN} = 5 to 3V F_{IN} = Fc/4 — 1 kHz		20			MSPS
Supply current		I_{CC} + I_{EE}			56	74	93	mA
Reference pin current		I_{REF}			12	16	20	mA
Analog input bandwidth		BW			8			MHz
Analog input capacitance		C_{IN}	V_{IN} = 4V + 0.07Vrms			30	35	pF
Analog input bias current		I_{IN}	V_{IN} = 4V		15	50	115	μA
Reference resistance (V_{RT} to V_{RB})		R_{REF}				125		Ω
Offset voltage	V_{RT}	E_{OT}			8	13	19	mV
	V_{RB}	E_{OB}			0	5	11	mV
Digital input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Digital input current		I_{IH}	V_{CC} = Max.	V_{IH} = 2.7V	0	−100	−150	μA
		I_{IL}		V_{IL} = 0.5V	0	−0.32	−0.5	mA
Digital output voltage		V_{OH}	V_{CC} = Min.	I_{OH} = −500μA	2.7	3.4		V
		V_{OL}		I_{OL} = 3mA			0.5	V
Output data delay		T_{DLH}	LOAD 1		14	18	24	ns
		T_{DHL}			21	27	34	ns
Non linearity		EL	Fc = 20 MSPS V_{IN} = 5 to 3V				±1/2	LSB
Differential non linearity		ED					±1/2	LSB
Differential gain error		DG	NTSC 40 IRE mod. ramp, Fc = 14.3 MSPS				1.5	%
Differential phase error		DP					0.5	deg.
Aperture jitter		E_{AP}				30		ps
Sampling delay		tds			6	8	11	ns

Electrical Characteristics (Dual supply)

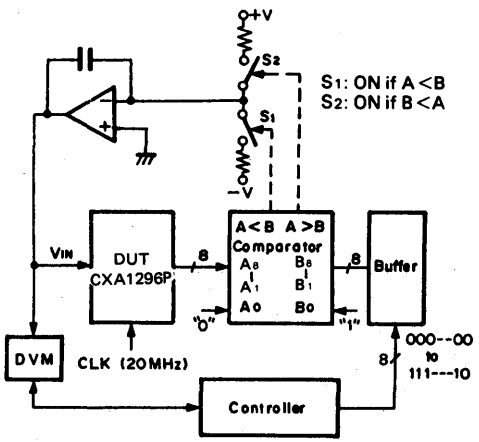
V_{CC} = +5V, DGND = 0V, AGND = 0V, V_{EE} = −5V, V_{RT} = 0V, V_{RB} = −2V, Ta = 25°C

Item		Symbol	Test condition		Min.	Typ.	Max.	Unit
Maximum conversion rate		F_C	V_{IN} = 0 to −2V F_{IN} = F_C/4 − 1 kHz		20			MSPS
Supply current		I_{CC}			7	10	14	mA
		I_{EE}			50	65	80	mA
Reference pin current		I_{REF}			12	16	20	mA
Analog input bandwidth		BW			8			MHz
Analog input capacitance		C_{IN}	V_{IN} = −1V + 0.07Vrms			30	35	pF
Analog input bias current		I_{IN}	V_{IN} = −1V		15	50	115	μA
Reference resistance (V_{RT} to V_{RB})		R_{REF}				125		Ω
Offset voltage	V_{RT}	E_{OT}			8	13	19	mV
	V_{RB}	E_{OB}			0	5	11	mV
Digital input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Digital input current		I_{IH}	V_{CC} = Max.	V_{IH} = 2.7V	0	−100	−150	μA
		I_{IL}		V_{IL} = 0.5V	0	−0.32	−0.5	mA
Digital output voltage		V_{OH}	V_{CC} = Min.	I_{OH} = −500μA	2.7	3.4		V
		V_{OL}		I_{OL} = 3mA			0.5	V
Output data delay		T_{DLH}	LOAD 1		14	18	24	ns
		T_{DHL}			21	27	34	ns
Non linearity		E_L	F_C = 20 MSPS V_{IN} = 0 to −2V				±1/2	LSB
Differential non linearity		E_D					±1/2	LSB
Differential gain error		DG	NTSC 40 IRE mod. ramp, F_C = 14.3 MSPS				1.5	%
Differential phase error		DP					0.5	deg.
Aperture jitter		E_{AP}				30		ps
Sampling delay		tds			6	8	11	ns

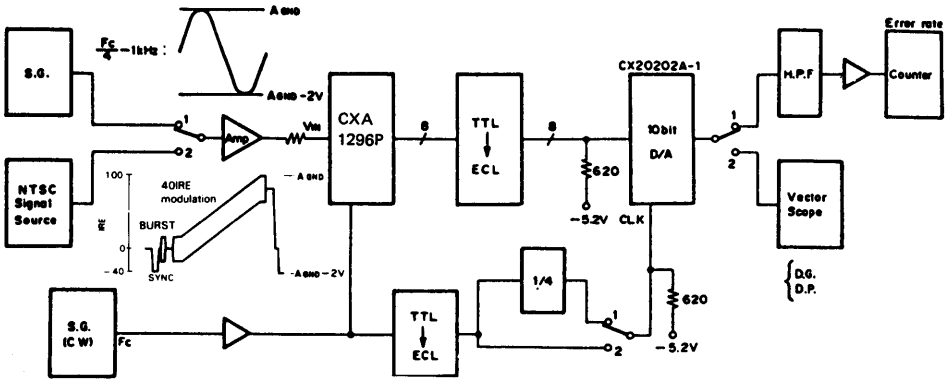
Application Circuit



Electrical Characteristics Test Circuit

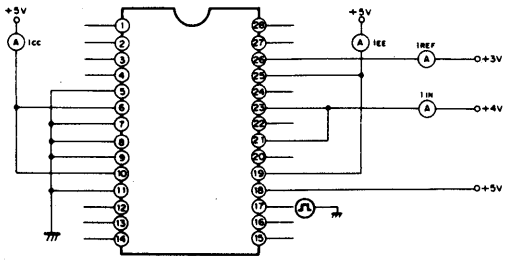


Non linearity
Differential non linearity } Test circuit

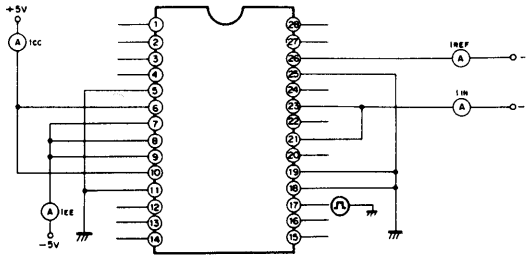


Maximum conversion rate
Differential gain error
Differential phase error
} Test circuit

Single supply

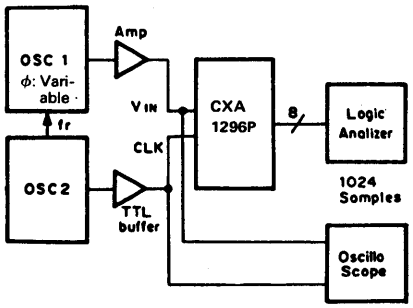


Dual supply

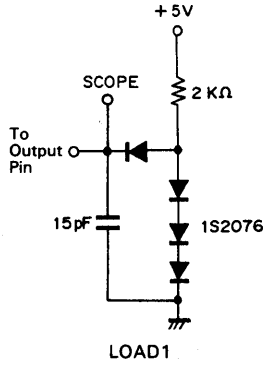


Note) VIN pin is connected to VRT pin for ICC and IEE measurement.

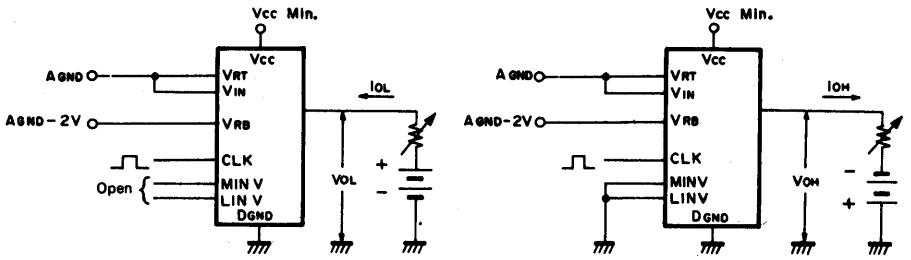
Supply current
Analog input bias current
Reference pin current
} Test circuit



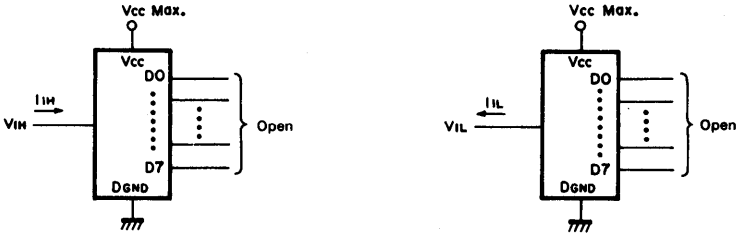
Aperture jitter
Sampling delay
} Test circuit



Test Load for Output data delay

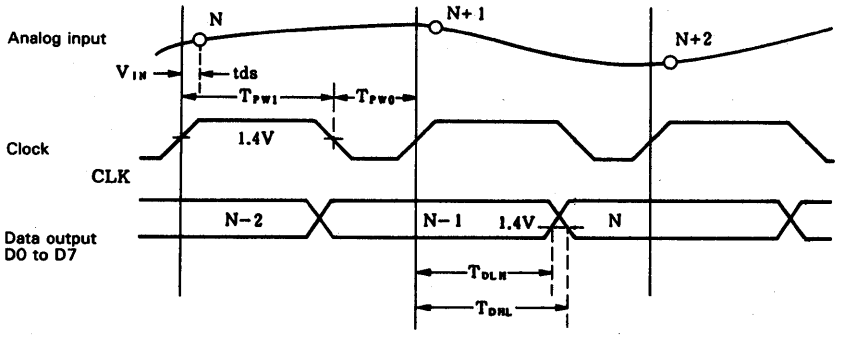


Test circuit of digital output voltage (D0 to D7)

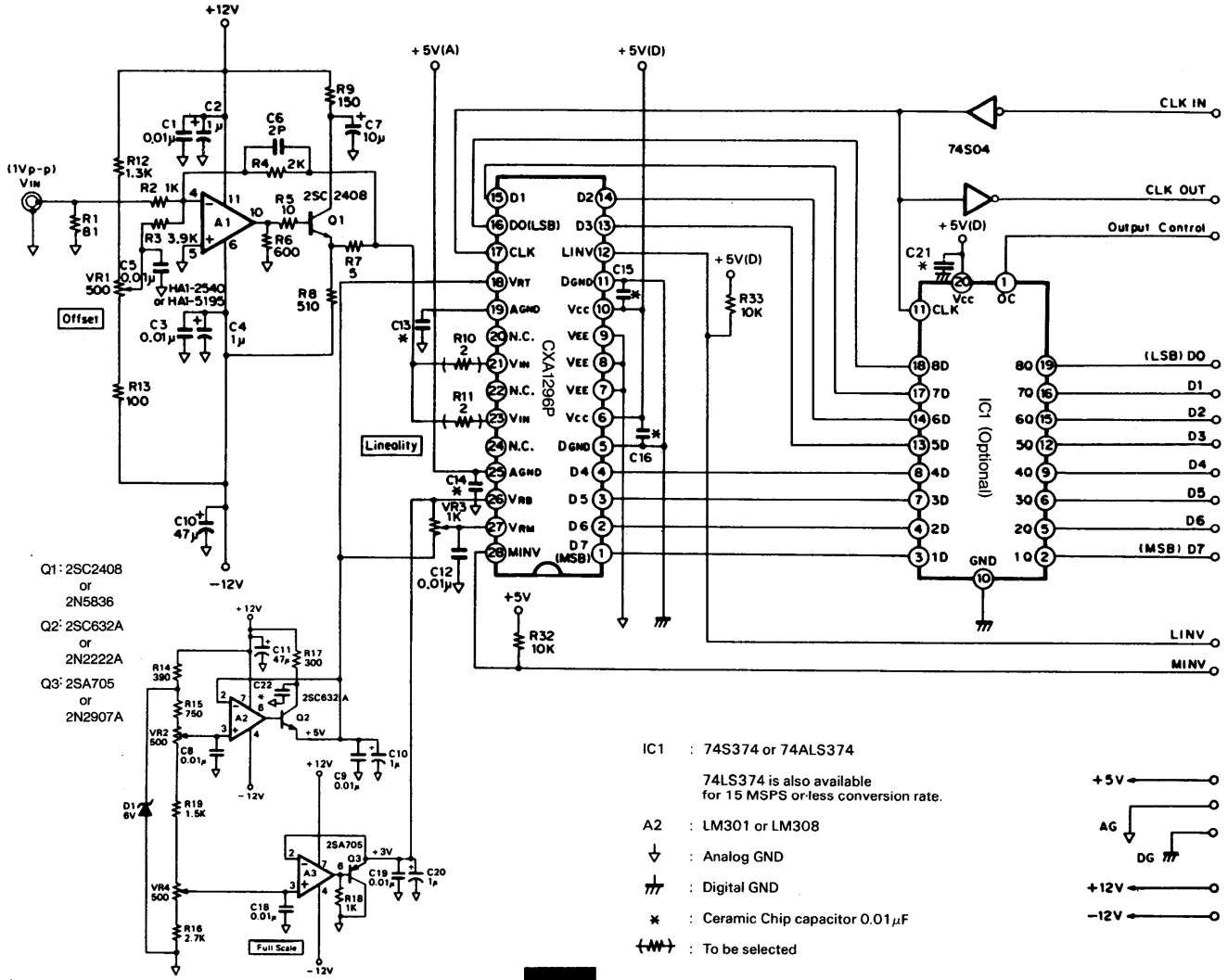


Test circuit of digital input current (CLK, MINV, LINV)

Timing Chart



Application Circuit (Single supply)



IC1 : 74S374 or 74ALS374

74LS374 is also available for 15 MSPS or-less conversion rate.

A2 : LM301 or LM308

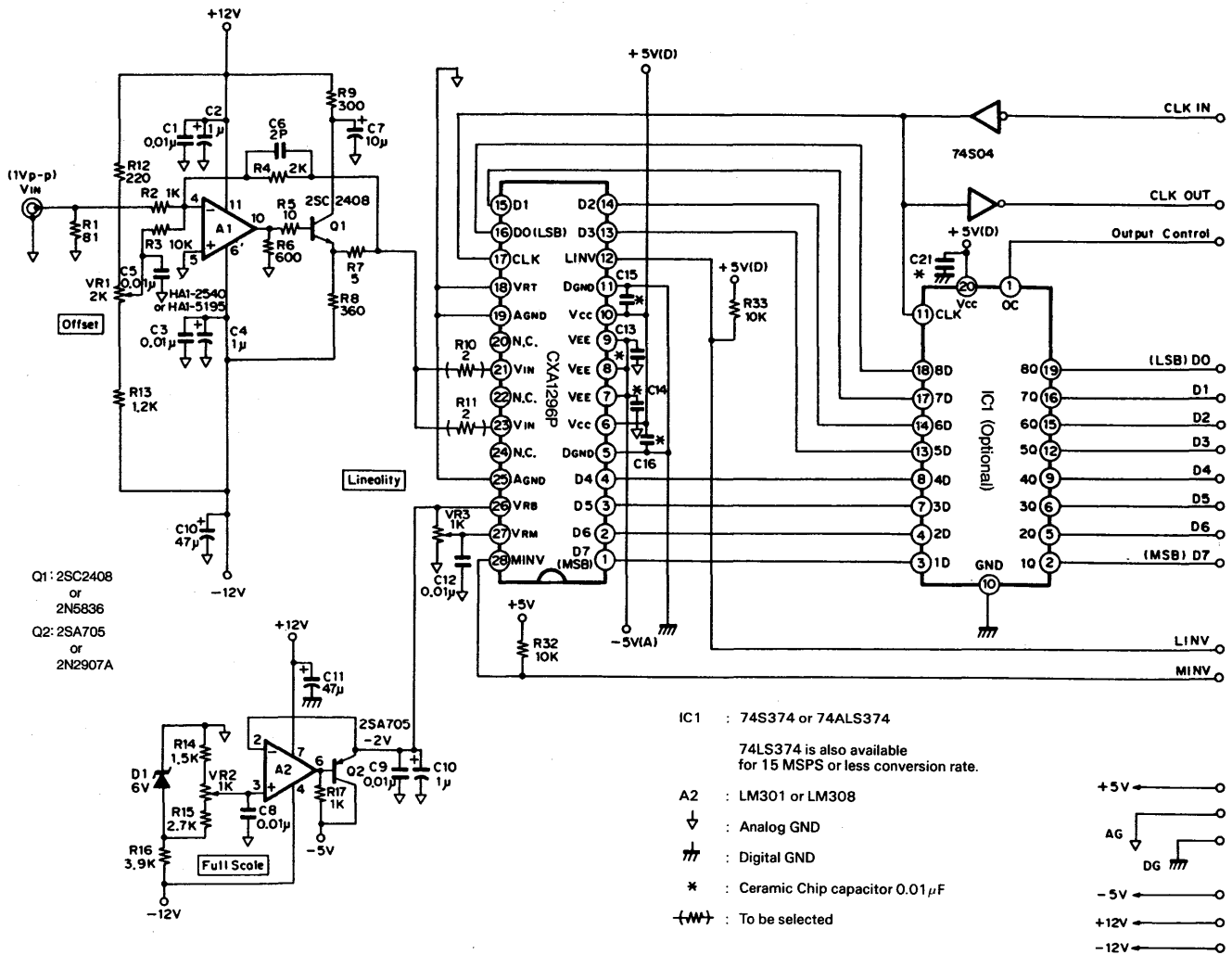
: Analog GND

: Digital GND

* : Ceramic Chip capacitor 0.01µF

: To be selected

Application Circuit (Dual supply)



IC1 : 74S374 or 74ALS374

74LS374 is also available for 15 MSPS or less conversion rate.

A2 : LM301 or LM308

: Analog GND

: Digital GND

* : Ceramic Chip capacitor 0.01 μF

: To be selected

+5V
AG
DG
−5V
+12V
−12V

Notes on Application

1. Each of DGND pins (5, 11) and each of Vcc Pins (6, 10) are divided in internal circuit. All of the pins should be connected to respective PCB patterns.

2. Layout of the analog and digital sections should be separated to reduce noise effect.
   VEE pins to AGND and Vcc pins to DGND should be bypassed as closely as possible by means of 1μF and 0.01μF capacitors.
   For the 0.01μF, a ceramic chip capacitor should be used.

3. The input capacitance of the analog input is much smaller than that of the Flash Type A/D converters in use so far. It is necessary to use an amplifier with sufficient band width and driving power. Pins VIN (21, 23) are divided in it, so they should be connected together. When driving with a low output impedance amplifier, parasitic oscillation may occur. This can be prevented by introducing between the amplifier output and A/D input a small resistance of 2 to 10Ω with smaller inductance, in series. And, that also each VIN pins are divided with small resistances (shown in the Application Circuit) is effective.
   The amplifier output and A/D input should be connected as closely as possible.

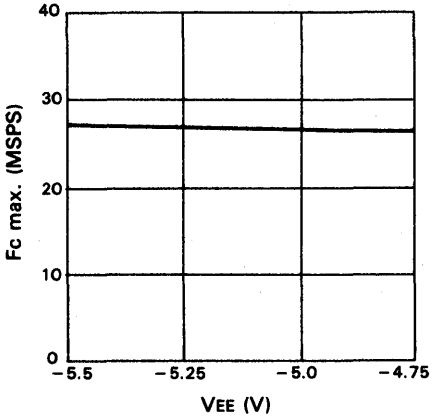
4. Voltage between VRT to VRB is equivalent to the dynamic range of the analog input. VRB pin should be bypassed to AGND by means of 1μF and 0.01μF capacitors.
   Through bypassing VRM pin with a 0.01μF capacitor to AGND, characteristics at high frequency become more balanced. Also, VRM pin can be used as a trimming pin for more precise linearity compensation.

5. CLK line should be wired in short distance and that should be separated from the other section to reduce the inductive.

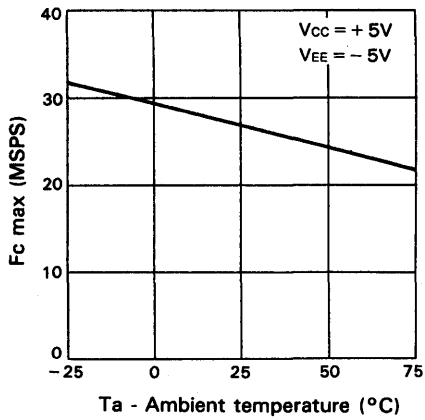
6. Analog input signal is sampled at the positive going edge of the CLK, and a corresponding digital data appears to the output parts at the positive going edge with a short delay time (TDLH, TDHL). If digital data will be latched externally, it should be latched at the positive going edge. (See the Timing Chart)

7. It is recommended to connect free pins to AGND for prevention of noise effect.

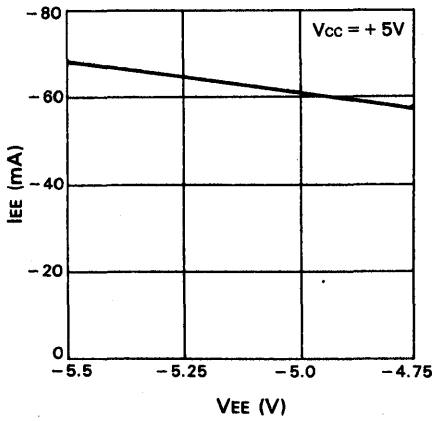
Fc max vs. VEE



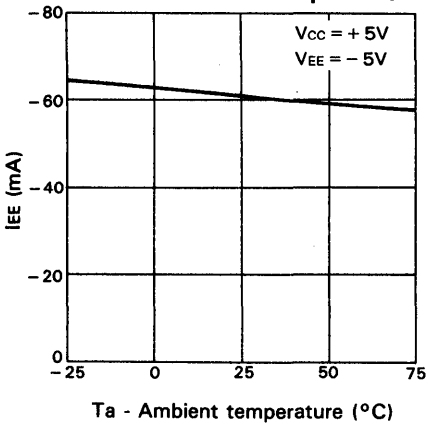
Fc max vs. Ambient temperature



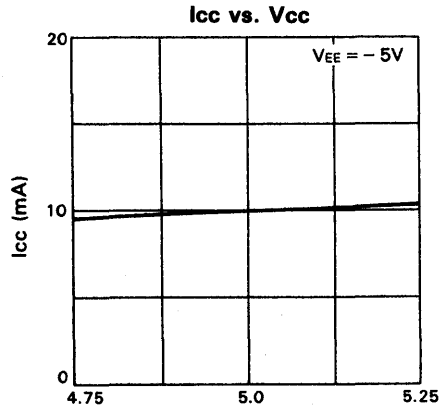
IEE vs. VEE



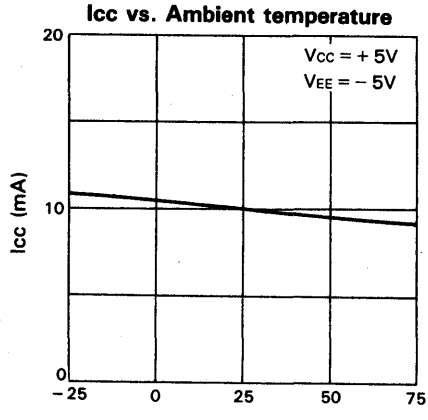
IEE vs. Ambient temperature



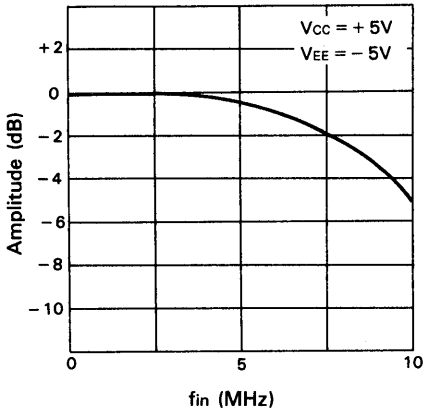
Icc vs. Vcc



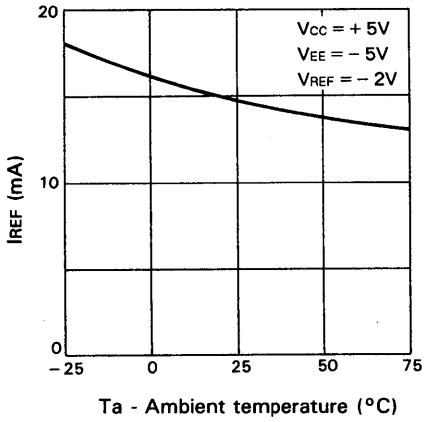
Icc vs. Ambient temperature



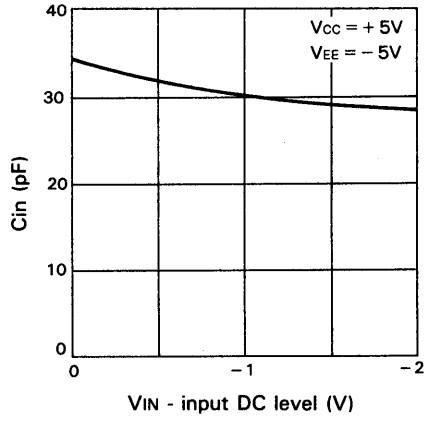
Amplitude deviation of the converted signal vs. The analog frequency



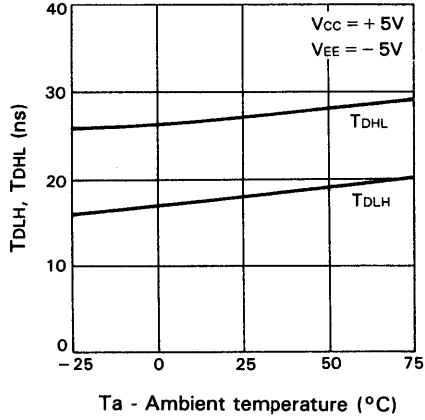
IREF vs. Ambient temperature



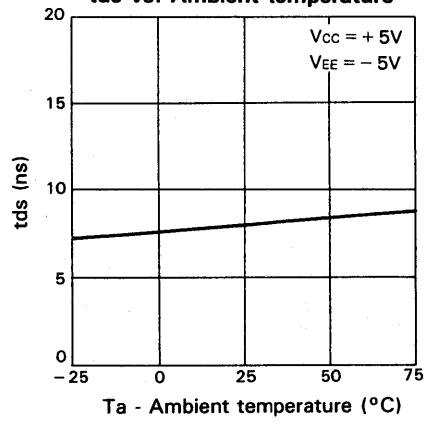
CIN vs. VIN - input DC level

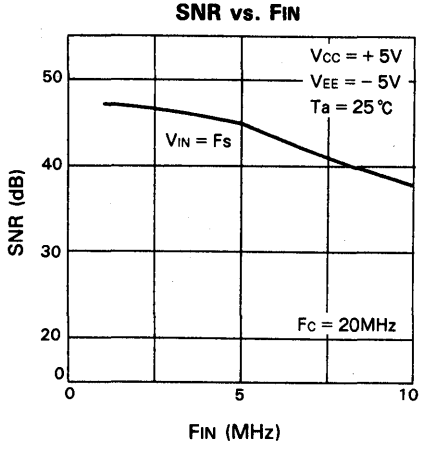


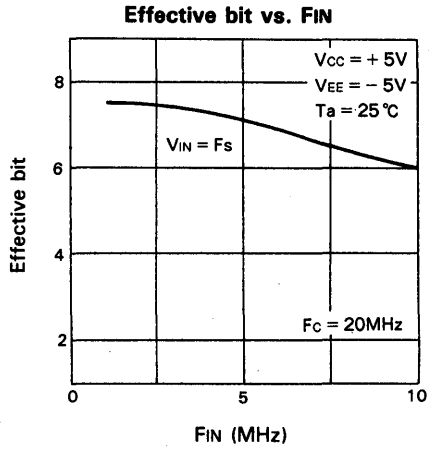
TDLH, TDHL vs. Ambient temperature



tds vs. Ambient temperature

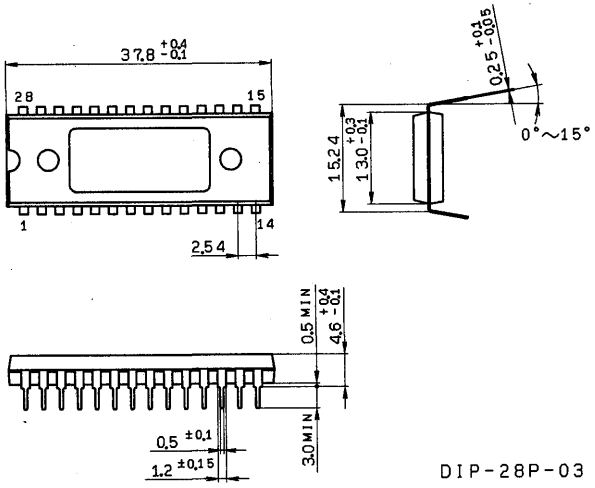






Package Outline Unit : mm

28pin DIP (Plastic) 600mil 4.2g



DIP-28P-03

SONY® CXD1172M/P

6-bit 20 MSPS Video A/D Converter (CMOS)

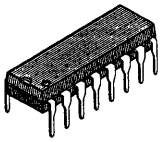
Evaluation Board Available — CXD1172P/CXA1106P PCB

Description

CXD1172 is a 6-bit CMOS A/D converter for video use. The adoption of a 2-step parallel system achieves low consumption at a maximum conversion speed of 20 MSPS.

CXD1172M 16 pin SOP (Plastic)

CXD1172P 16 pin DIP (Plastic)



Features

- Resolution ..... 6-bit ± 1/2 LSB
- Max. sampling frequency .... 20 MSPS
- Low power consumption .... 60 mW
  (at 20 MSPS Typ.)
  (Reference current excluded)
- Built-in sampling and hold circuit.
- 3-state TTL compatible output.
- Power supply ..... 5 V single
- Low input capacitance 5pF
- Reference impedance ..... 300 Ω (Typ.)

Structure

Silicon gate CMOS monolithic IC

Applications

- TV, VCR digital systems and a wide range of fields where high speed A/D conversion is required.

Absolute Maximum Ratings (Ta=25°C)

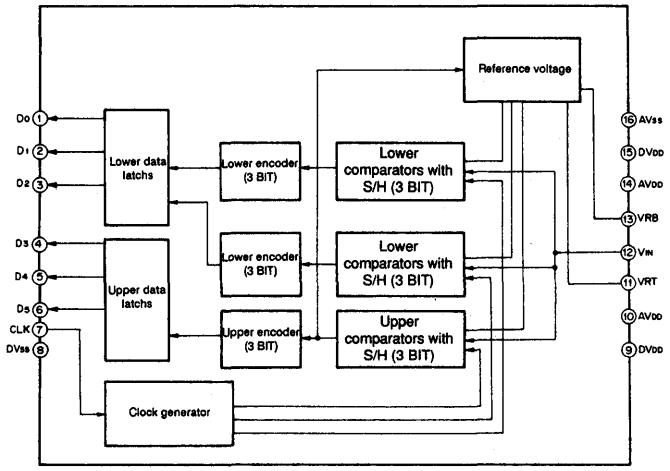
• Supply voltage	V_{DD}			7		V
• Reference voltage	V_{RT}, V_{RB}	V_{DD}	to	V_{SS}		V
• Analog input voltage	V_{IN}	V_{DD}	to	V_{SS}		V
• Digital input voltage	CLK	V_{DD}	to	V_{SS}		V
• Digital output voltage	V_{OH}, V_{OL}	V_{DD}	to	V_{SS}		V
• Storage temperature	Tstg	−55	to	+150	°C	

Recommended Operating Conditions

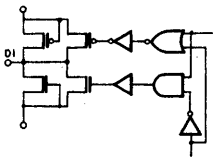
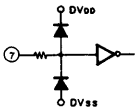
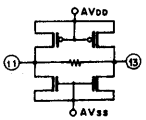
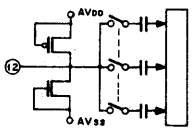
• Supply voltage	AV_{DD}, AVss	4.75	to	5.25		V
	DV_{DD}, DVss	4.75	to	5.25		
• Reference input voltage	V_{RB}	0	to	4.1		V
	V_{RT}	0.9	to	5.0		V
	V_{RT}-V_{RB}	0.9	to	AV_{DD}		V
• Analog input voltage	V_{IN}	V_{RB}	to	V_{RT}		
• Clock pulse width	T_{PWI}		25	(Min.)		ns
	T_{PWO}		25	(Min.)		ns
• Operating temperature	T_{OPR}	−20	to	+75		°C

E89672-YA

Block Diagram and Pin Configuration



Pin Description and Equivalent Circuits

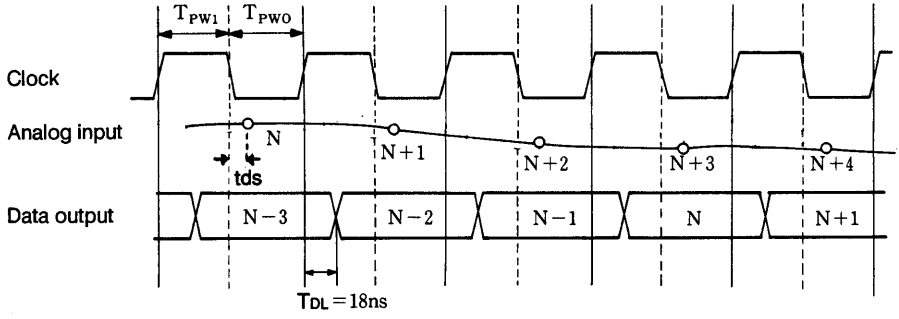
No.	Symbol	Equivalent Circuit	Description
1 to 6	D_0 to D_5		D_0 (LSB) to D_5 (MSB) output
7	CLK		Clock input
8	DVSS		Digital GND
9, 15	DVDD		Digital +5V
10, 14	AVDD		Analog +5V
11	VRT		Reference voltage (Top)
13	VRB		Reference voltage (Bottom)
12	VIN		Analog input
16	AVSS		Analog GND

Digital Output

Compatibility between Analog input voltage and the digital output code is indicated in the chart below.

Input signal voltage	Step	Digital output code MSB					LSB
V_{RT}	0	1	1	1	1	1	1
	31	1	0	0	0	0	0
	32	0	1	1	1	1	1
V_{RB}	63	0	0	0	0	0	0

Timing Chart 1



○: Point for analog signal sampling

Electrical Characteristics

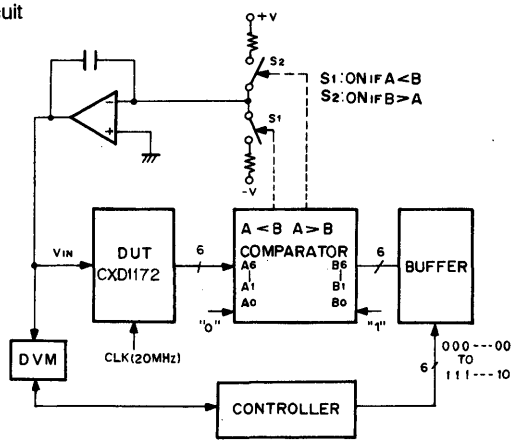
V_{DD} = +5V, V_{RB} = 1.0V, V_{RT} = 2.0V, Ta = 25°C

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Maximum conversion speed	Fc	V_{IN} = 1.0 V to 2.0 V F_{IN} = 1kHz ramp		20	25		MSPS
Supply current	I_{DD}	Fc = 20 MSPS NTSC ramp wave input			12	18	mA
Reference pin current	I_{REF}			2.6	3.3	4.8	mA
Analog input band (-1dB)	BW				14		MHz
Analog input capacitance	C_{IN}	V_{IN} = 1.5 V + 0.07 Vrms			5		pF
Reference resistance (V_{RT} to V_{RB})	R_{REF}			210	300	390	Ω
Offset voltage	E_{OT}			0	-20	-40	mV
	E_{OB}			10	30	50	
Digital input voltage	V_{IH}			4.0			V
	V_{IL}					1.0	
Digital input current	I_{IH}	V_{DD} = max.	V_{IH} = V_{DD}			5	µA
	I_{IL}		V_{IL} = 0 V			5	
Digital output current	I_{OH}	V_{DD} = min.	V_{OH} = V_{DD} - 0.5 V	-1.5			mA
	I_{OL}		V_{OL} = 0.4 V	4.0			
Output data delay	T_{DL}				18	30	ns
Integral non-linearity	EL	Fc = 20 MSPS V_{IN} = 1.0 V to 2.0 V			±0.3	±0.5	LSB
Differential non-linearity	ED	Fc = 20 MSPS V_{IN} = 1.0 V to 2.0 V			±0.3	±0.5	LSB
Differential gain error	DG	NTSC 40 IRE mod			1.0		%
Differential phase error	DP	ramp, Fc = 14.3 MSPS			1.0		deg
Aperture jitter	Taj				40		ps
Aperture delay	Tsd				4		ns

Electrical Characteristics Test Circuit

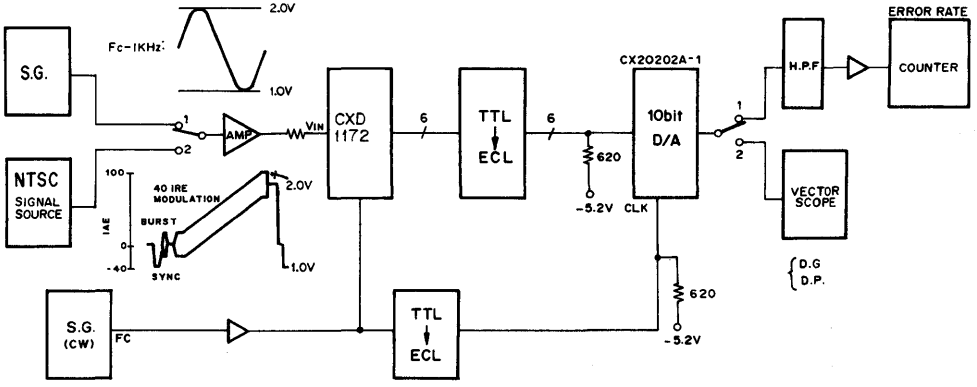
Integral non-linearity error
Differential non-linearity
Offset voltage

Test circuit

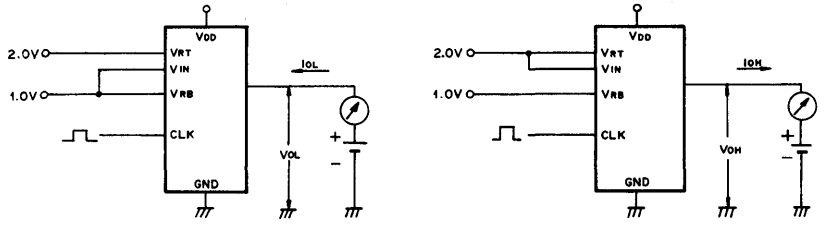


Maximum operational speed
Differential gain error
Differential phase error

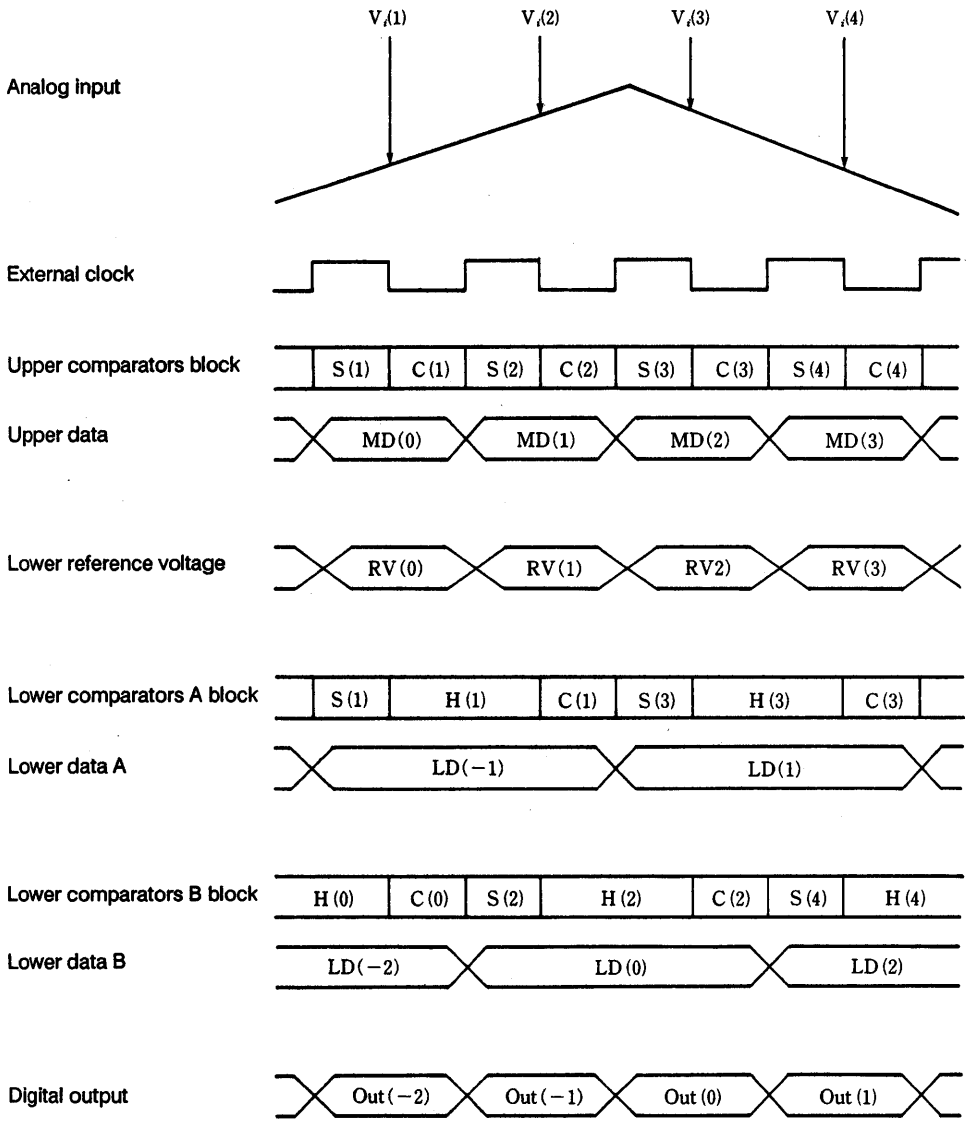
Test circuit



Digital output current test circuit



Timing Chart 2



Application Circuit

Confer the page for "Peripheral circuit board" of CXD1172P/CXA1106PPCB.

Operation (See Block Diagram and Timing Chart)

1. CXD1172M/P is a 2-step parallel system A/D converter featuring a 3-bit upper comparators group and 2 lower comparators groups of 3-bit each. The reference voltage that is equal to the voltage between VRT-VRB/8 is constantly applied to the upper 3-bit comparator block. Voltage that corresponded to the upper data is fed through the reference supply to the lower data.

2. This IC uses an offset cancel type comparator and operates synchronously with an external clock. It features the following operating modes which are respectively indicated on the timing chart with S, H, C symbols. That is input sampling (auto zero) mode, input hold mode and comparison mode.

3. The operation of respective parts is as indicated in the chart. For instance input voltage Vi (1) is sampled with the falling edge of the first clock by means of the upper comparator block and the lower comparator A block.
   The upper comparators block finalizes comparison data MD (1) with the rising edge of the first clock. Simultaneously the reference supply generates the lower reference voltage RV (1) that corresponded to the upper results. The lower comparator block finalizes comparison data LD (1) with the rising edge of the second clock. MD (1) and LD (1) are combined and output as Out (1) with the rising edge of the 3rd clock. Accordingly there is a 2.5 clock delay from the analog input sampling point to the digital data output.

Operation Notes

1. V_{DD}, V_{SS}
   To reduce noise effects, separate the analog and digital systems close to the device. For both the digital and analog V_{DD} pins, use a ceramic capacitor of about 0.1 μF set as close as possible to the pin to bypass to the respective GND's.

2. Analog input
   Compared with the flash type A/D converter, the input capacitance of the analog input is rather small. However it is necessary to conduct the drive with an amplifier featuring sufficient band and drive capability. When driving with an amplifier of low output impedance, parasite oscillation may occur. That may be prevented by inserting a resistance of about 100 Ω in series between the amplifier output and A/D input.

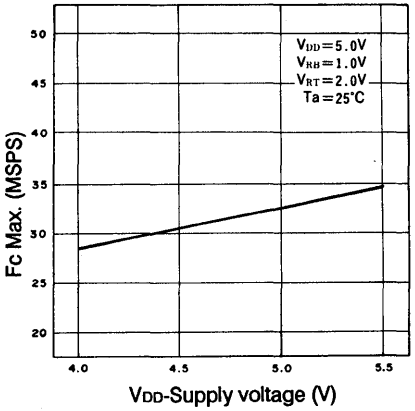
3. Clock input
   The clock line wiring should be as short as possible also, to avoid any interference with other signals, separate it from other circuits.

4. Reference input
   Voltage between V_{RT} to V_{RB} is compatible with the dynamic range of the analog input. Bypassing V_{RT} and V_{RB} pins to GND, by means of a capacitor about 0.1 μF, stable characteristics are obtained.

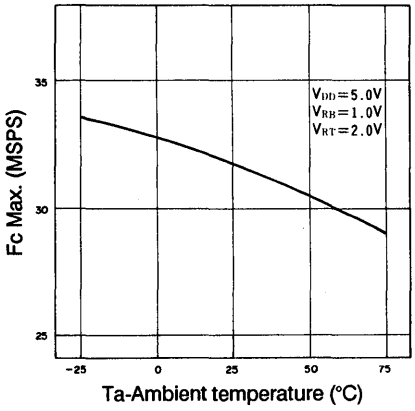
5. Timing
   Analog input is sampled with the falling edge of CLK and output as digital data with a delay of 2.5 clocks and with the following rising edge. The delay from the clock rising edge to the data output is about 18ns.

6. About latch up
   It is necessary that AV_{DD} and DV_{DD} pins be the common source of power supply.
   This is to avoid latch up due to the voltage difference between AV_{DD} and DV_{DD} pins when power is ON.
   See "For latch up prevention" of CXD1172P/CXA1106P PCB description.

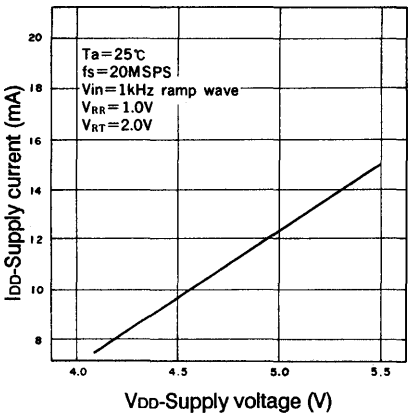
Fc (Max.) vs. Supply voltage



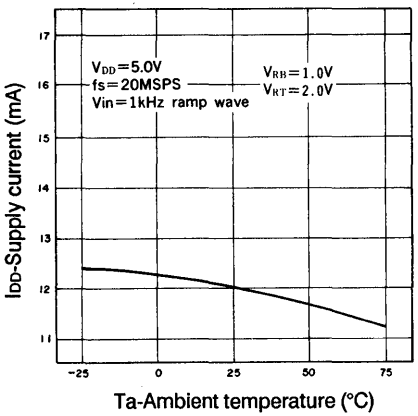
Fc (Max.) vs. Ambient temperature

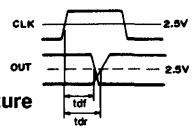


Supply current vs. Supply voltage



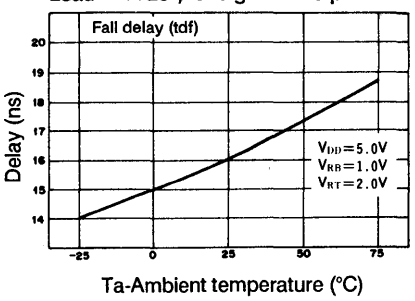
Supply current vs. Ambient temperature





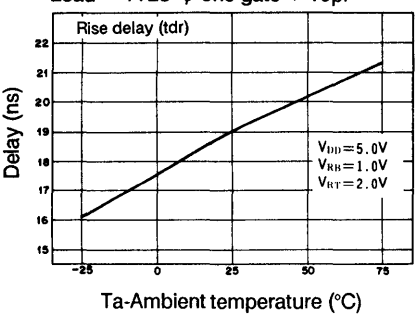
Output Delay vs. Ambient temperature

Load = TTLS ϕ one gate + 10 pF

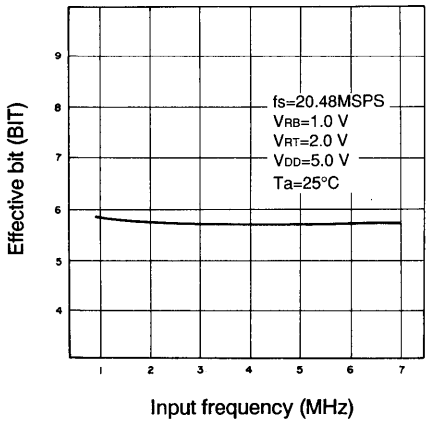


Output Delay vs. Ambient temperature

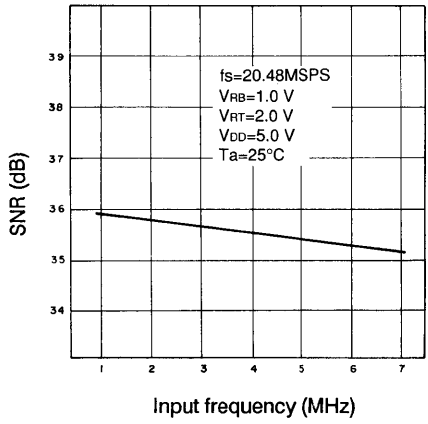
Load = TTLS ϕ one gate + 10pF



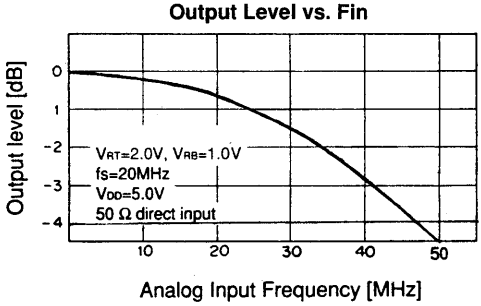
Effective bit vs. Input frequency



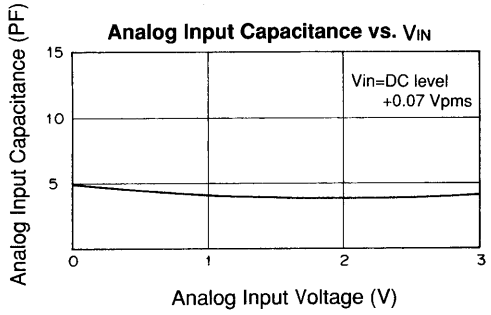
SNR vs. Input frequency



Output Level vs. Fin

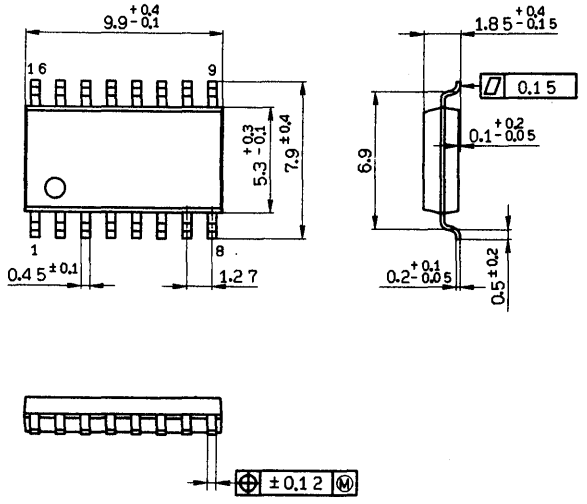


Analog Input Capacitance vs. V_{IN}



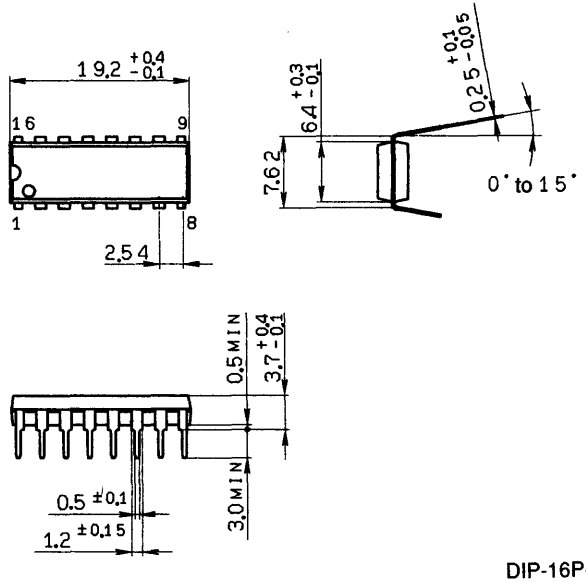
Package Outline Unit:mm

CXD1172M 16pinSOP(Plastic) 300mil 0.2g



SOP-16P-L01

CXD1172P 16pinDIP(Plastic) 300mil 1.0g



DIP-16P-01

SONY® CXD1172AM/AP

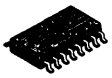
6-bit 20 MSPS Video A/D Converter (CMOS) **Preliminary**

Evaluation Board Available — CXD1172AP/CXA1106P PCB

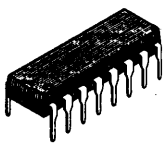
Description

CXD1172A is a 6-bit CMOS A/D converter for video use. The adoption of a 2-step parallel system achieves low consumption at a maximum conversion speed of 20 MSPS minimum, 35 MSPS typical.

CXD1172AM 16 pin SOP (Plastic)



CXD1172AP 16 pin DIP (Plastic)



Features

- Resolution ..... 6-bit ± 1/2 LSB
- Max. sampling frequency .... 20 MSPS
- Low power consumption .... 40 mW
  (at 20 MSPS Typ.)
  (Reference current excluded)
- Built-in sampling and hold circuit.
- 3-state TTL compatible output.
- Power supply ..... 5 V single
- Low input capacitance 4pF
- Reference impedance ..... 300 Ω (Typ.)
- **Pin replacable with CXD1172M/P**

Structure

Silicon gate CMOS monolithic IC

Applications

- TV, VCR digital systems and a wide range of fields where high speed A/D conversion is required.

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}			7		V
• Reference voltage	V_{RT}, V_{RB}	V_{DD}	to	V_{SS}		V
• Analog input voltage	V_{IN}	V_{DD}	to	V_{SS}		V
• Digital input voltage	CLK	V_{DD}	to	V_{SS}		V
• Digital output voltage	V_{OH}, V_{OL}	V_{DD}	to	V_{SS}		V
• Storage temperature	Tstg	−55	to	+150		°C

Recommended Operating Conditions

• Supply voltage	AV_{DD}, AV_{SS}	4.75	to	5.25		V
	DV_{DD}, DV_{SS}	4.75	to	5.25		
• Reference input voltage	V_{RB}	0	to	4.1		V
	V_{RT}	0.9	to	5.0		V
	V_{RT}-V_{RB}	0.9	to	AV_{DD}		V
• Analog input voltage	V_{IN}	V_{RB}	to	V_{RT}		
• Clock pulse width	T_{PWI}			25 (Min.)		ns
	T_{PWO}			25 (Min.)		ns
• Operating temperature	Topr	−20	to	+75		°C

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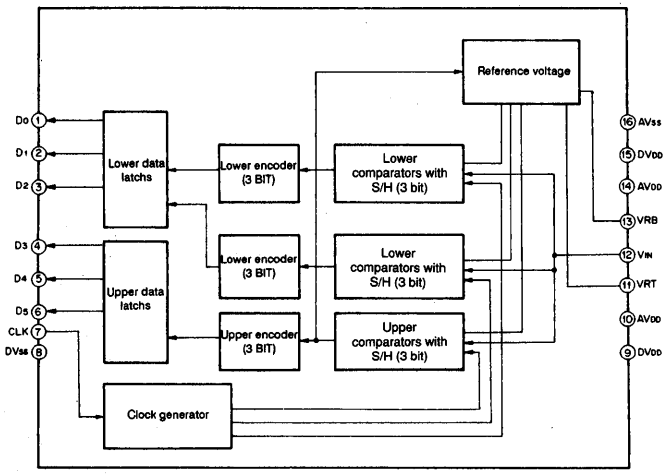
Block Diagram and Pin Configuration

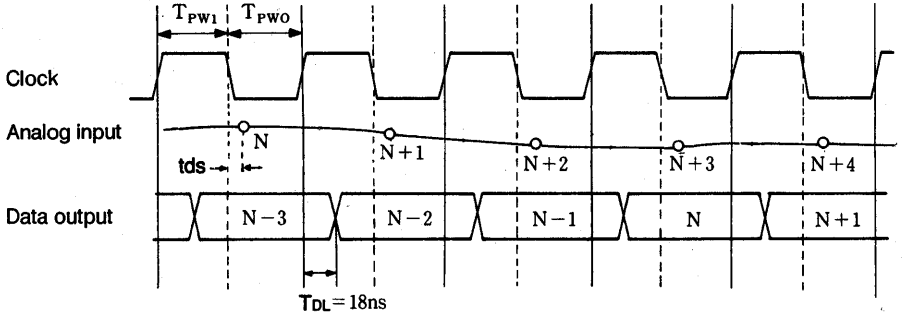


Digital Output

Compatibility between Analog input voltage and the digital output code is indicated in the chart below.

Input signal voltage	Step	Digital output code MSB					LSB
V_{RT}	0	1	1	1	1	1	1
	31	1	0	0	0	0	0
	32	0	1	1	1	1	1
V_{RB}	63	0	0	0	0	0	0

Timing Chart 1



Electrical Characteristics

V_{DD} = +5V, V_{RB} = 1.0V, V_{RT} = 2.0V, Ta = 25°C

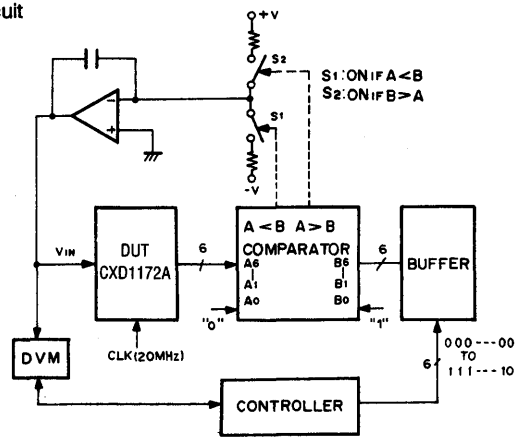
Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Maximum conversion speed	Fc	V_{IN} = 1.0 V to 2.0 V F_{IN} = 1kHz ramp		20	35		MSPS
Supply current	I_{DD}	Fc = 20 MSPS NTSC ramp wave input			8		mA
Reference pin current	I_{REF}				3.3		mA
Analog input band (-1dB)	BW				20		MHz
Analog input capacitance	C_{IN}	V_{IN} = 1.5 V + 0.07 Vrms			4		pF
Reference resistance (V_{RT} to V_{RB})	R_{REF}				300		Ω
Offset voltage	E_{OT}				-20		mV
	E_{OB}				30		
Digital input voltage	V_{IH}			4.0			V
	V_{IL}					1.0	
Digital input current	I_{IH}	V_{DD} = max.	V_{IH} = V_{DD}			5	μA
	I_{IL}		V_{IL} = 0 V			5	
Digital output current	I_{OH}	V_{DD} = min.	V_{OH} = V_{DD} - 0.5V	-1.5			mA
	I_{OL}		V_{OL} = 0.4 V	4.0			
Output data delay	T_{DL}				18	30	ns
Integral non-linearity	EL	Fc = 20 MSPS V_{IN} = 1.0 V to 2.0 V			±0.3	±0.5	LSB
Differential non-linearity	ED	Fc = 20 MSPS V_{IN} = 1.0 V to 2.0 V			±0.3	±0.5	LSB
Differential gain error	DG	NTSC 40 IRE mod			1.0		%
Differential phase error	DP	ramp, Fc = 14.3 MSPS			1.0		deg
Aperture jitter	Taj				40		ps
Sampling delay	Tsd				4		ns

For the following information, please see CXD1172M/P portion.
- Pin Description and Equivalent Circuits

Electrical Characteristics Test Circuit

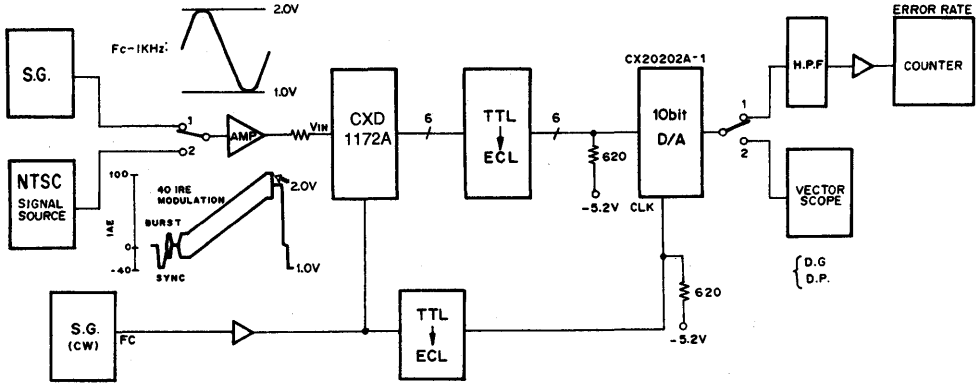
Integral non-linearity error
Differential non-linearity
Offset voltage

Test circuit

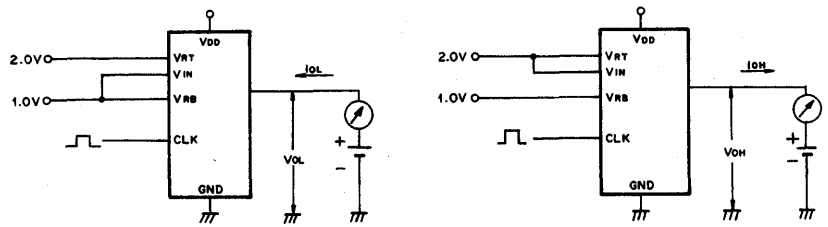


Maximum operational speed
Differential gain error
Differential phase error

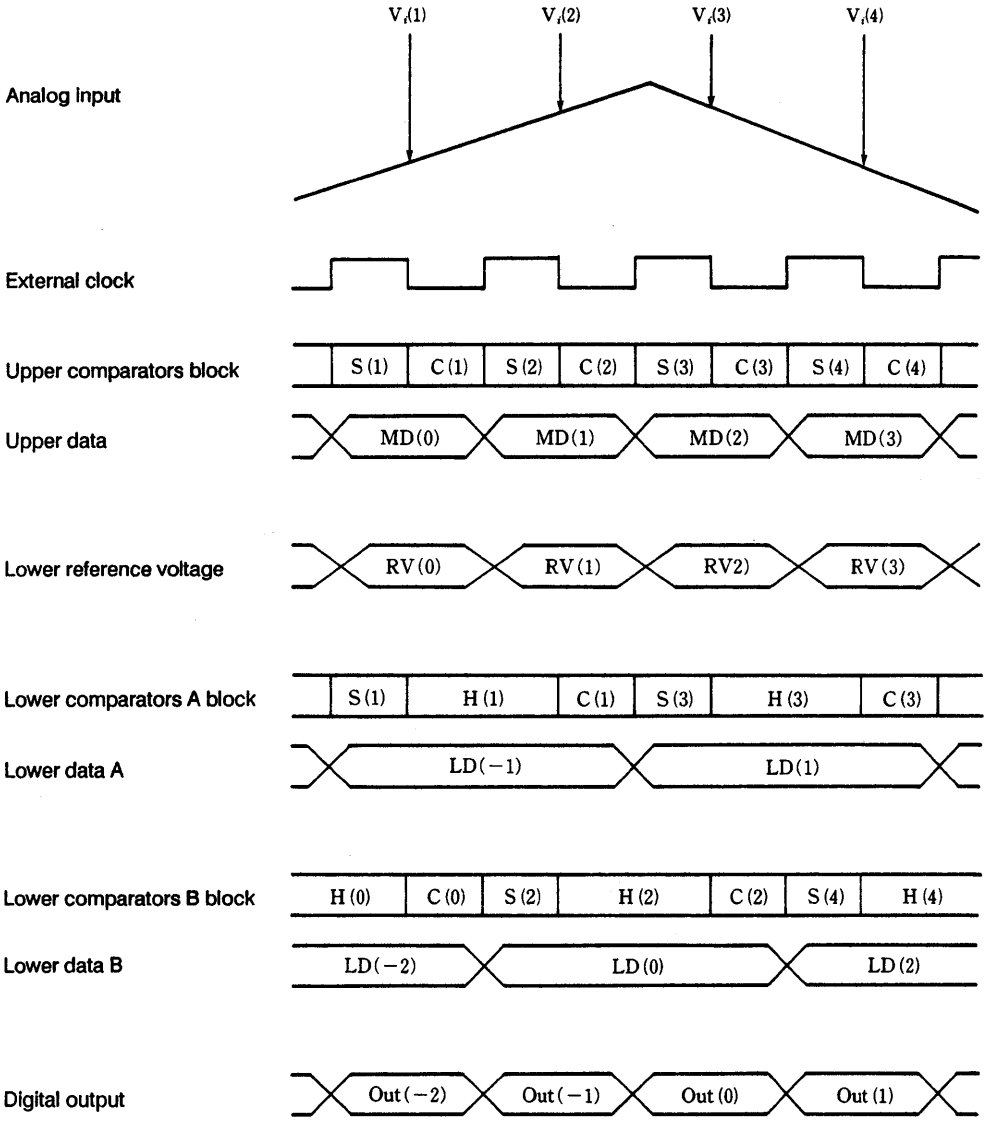
Test circuit



Digital output current test circuit



Timing Chart 2



Application Circuit

Confer the page for "Peripheral circuit board" of CXD1172AP/CXA1106PPCB.

Operation (See Block Diagram and Timing Chart)

1. CXD1172AM/AP is a 2-step parallel system A/D converter featuring a 3-bit upper comparators group and 2 lower comparators groups of 3-bit each. The reference voltage that is equal to the voltage between VRT-VRB/8 is constantly applied to the upper 3-bit comparator block. Voltage that corresponded to the upper data is fed through the reference supply to the lower data.

2. This IC uses an offset cancel type comparator and operates synchronously with an external clock. It features the following operating modes which are respectively indicated on the timing chart with S, H, C symbols. That is input sampling (auto zero) mode, input hold mode and comparison mode.

3. The operation of respective parts is as indicated in the chart. For instance input voltage Vi (1) is sampled with the falling edge of the first clock by means of the upper comparator block and the lower comparator A block.
   The upper comparators block finalizes comparison data MD (1) with the rising edge of the first clock. Simultaneously the reference supply generates the lower reference voltage RV (1) that corresponded to the upper results. The lower comparator block finalizes comparison data LD (1) with the rising edge of the second clock. MD (1) and LD (1) are combined and output as Out (1) with the rising edge of the 3rd clock. Accordingly there is a 2.5 clock delay from the analog input sampling point to the digital data output.

Operation Notes

1. V_{DD}, V_{SS}
   To reduce noise effects, separate the analog and digital systems close to the device. For both the digital and analog V_{DD} pins, use a ceramic capacitor of about 0.1 µF set as close as possible to the pin to bypass to the respective GND's.

2. Analog input
   Compared with the flash type A/D converter, the input capacitance of the analog input is rather small. However it is necessary to conduct the drive with an amplifier featuring sufficient band and drive capability. When driving with an amplifier of low output impedance, parasite oscillation may occur. That may be prevented by inserting a resistance of about 100 Ω in series between the amplifier output and A/D input.

3. Clock input
   The clock line wiring should be as short as possible also, to avoid any interference with other signals, separate it from other circuits.

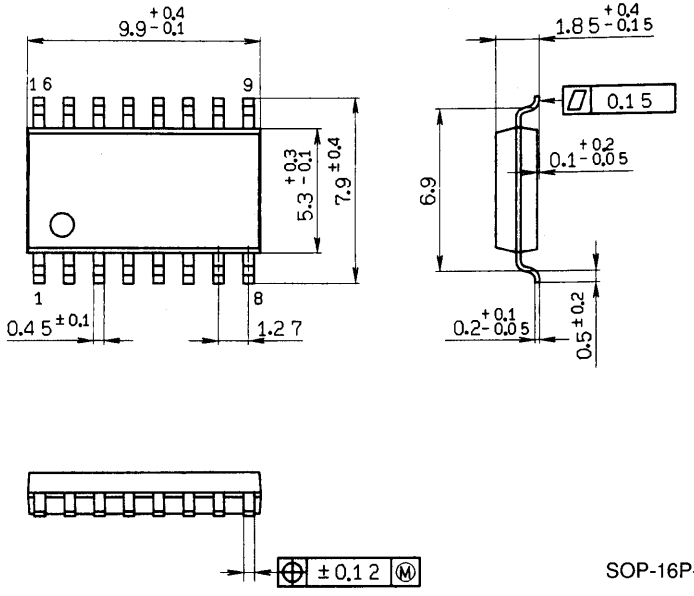
4. Reference input
   Voltage between V_{RT} to V_{RB} is compatible with the dynamic range of the analog input. Bypassing V_{RT} and V_{RB} pins to GND, by means of a capacitor about 0.1 µF, stable characteristics are obtained.

5. Timing
   Analog input is sampled with the falling edge of CLK and output as digital data with a delay of 2.5 clocks and with the following rising edge. The delay from the clock rising edge to the data output is about 18ns.

6. About latch up
   It is necessary that AV_{DD} and DV_{DD} pins be the common source of power supply.
   This is to avoid latch up due to the voltage difference between AV_{DD} and DV_{DD} pins when power is ON.
   See "For latch up prevention" of CXD1172AP/CXA1106P PCB description. (Page 495).

Package Outline Unit:mm

CXD1172AM 16pin SOP(Plastic) 300mil 0.2g



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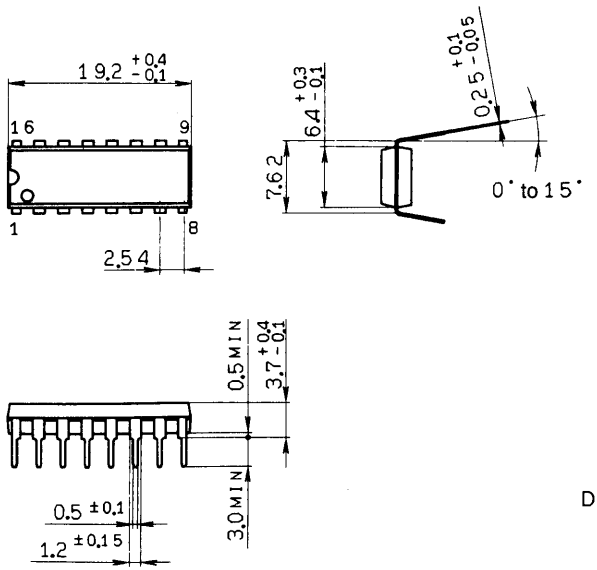
CXD1172AP 16pin DIP(Plastic) 300mil 1.0g



DIP-16P-01

SONY®

CXD1175M/P

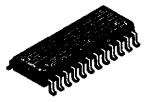
8-bit 20 MSPS Video A/D Converter (CMOS)

Evaluation Board Available — CXD1175P/CXA1106P PCB

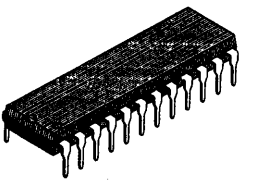
Description

CXD1175 is an 8-bit CMOS A/D converter for video use. The adoption of a 2-step parallel system achieves low consumption at a maximum conversion speed of 20 MSPS.

CXD1175M 24pin SOP (Plastic)



CXD1175P 24pin DIP (Plastic)



Features

- Resolution ..... 8-bit ± 1/2 LSB (DL)
- Max. sampling frequency .... 20 MSPS
- Low power consumption .... 90 mW (at 20 MSPS Typ.) (Reference current excluded)
- Built-in sampling and hold circuit.
- Built-in reference voltage self bias circuit.
- 3-state TTL compatible output.
- Power supply ..... 5V single
- Low input capacitance ..... 16 pF
- Reference impedance ..... 270Ω (Typ.)

Structure

Silicon gate CMOS monolithic IC

Applications

- TV, VCR digital systems and a wide range of fields where high speed A/D conversion is required.

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}		7		V
• Reference voltage	V_{RT}, V_{RB}	V_{DD}	to	V_{SS}	V
• Analog input voltage	V_{IN}	V_{DD}	to	V_{SS}	V
• Digital input voltage	C_{LK}	V_{DD}	to	V_{SS}	V
• Digital output voltage	V_{OH}, V_{OL}	V_{DD}	to	V_{SS}	V
• Storage temperature	Tstg	−55	to	+150°C	

Recommended Operating Conditions

• Supply voltage	AV_{DD}, AV_{SS}	4.75 to 5.25	V
	DV_{DD}, DV_{SS}		
	|DGND-AGND|	0 to 100	mV
• Reference input voltage	V_{RB}, V_{RT}	$0 \leqq V_{RB} < V_{RT} \leqq 2.7$	V
	V_{RT}-V_{RB}	1.8 to AV_{DD}	V
• Analog input voltage	V_{IN}	V_{RB} to V_{RT}	(1.8Vp-p to AV_{DD}Vp-p)
• Clock pulse width	T_{PWI}	25 (Min.)	ns
	T_{PWO}	25 (Min.)	ns
• Operating temperature	Topr	−20 to +75	°C

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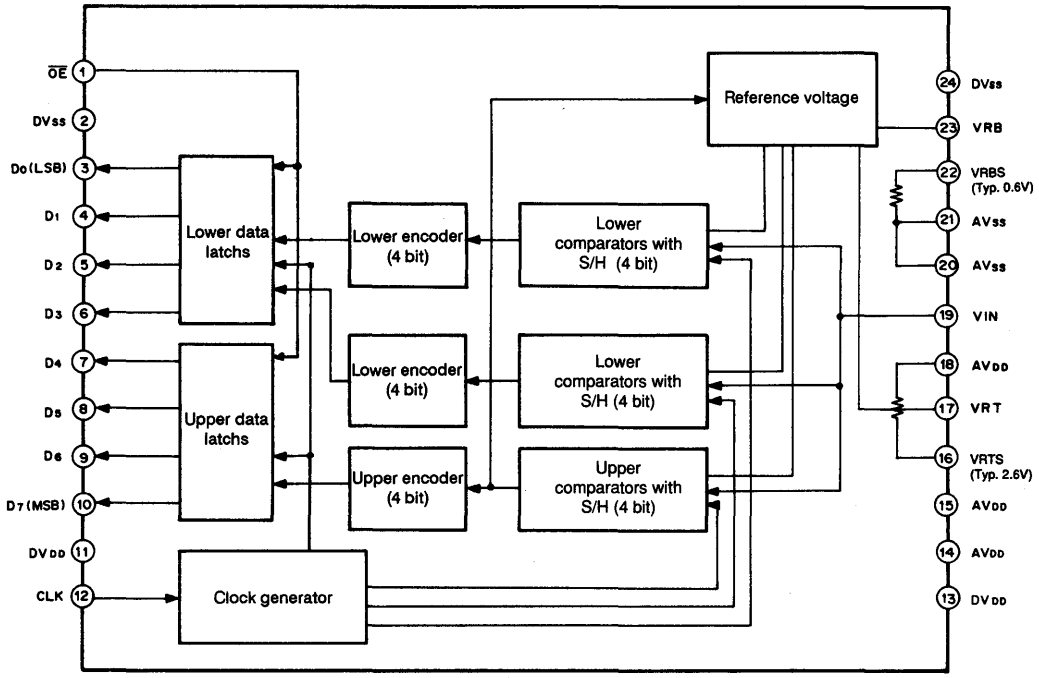
Block Diagram and Pin Configuration

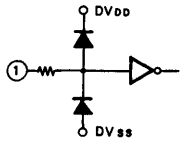
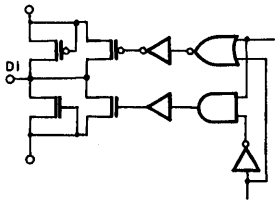
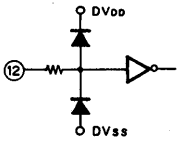
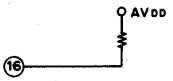
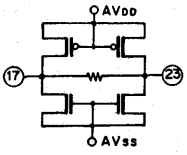
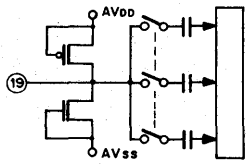
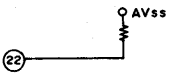


Digital Output

Compatibility between Analog input voltage and the digital output code is indicated in the chart below.

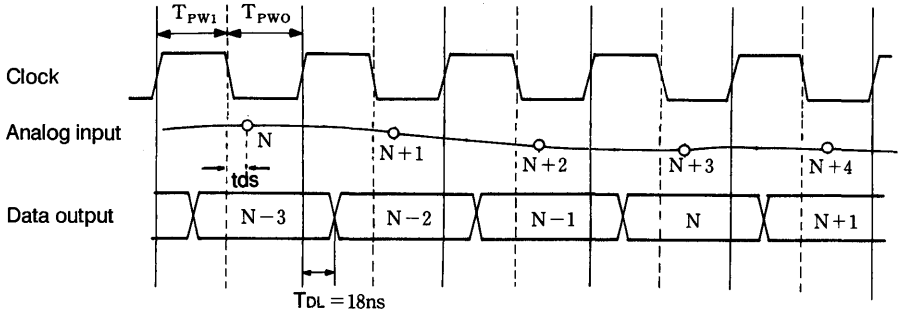
Input signal voltage	Step	Digital output code MSB							LSB
V_{RT}	0	1	1	1	1	1	1	1	1
	⋮					⋮			
	127	1	0	0	0	0	0	0	0
	128	0	1	1	1	1	1	1	1
	⋮					⋮			
V_{RB}	255	0	0	0	0	0	0	0	0

Pin Description and Equivalent Circuits

No.	Symbol	Equivalent Circuit	Description
1	$\overline{OE}$		When $\overline{OE}$ = Low, Data is output. When $\overline{OE}$ = High, D_0 to D_7 pins turn to High impedance.
2, 24	DVss		Digital GND
3 to 10	D_0 to D_7		D_0 (LSB) to D_7 (MSB) output
11, 13	DVDD		Digital +5V
12	CLK		Clock input
16	VRTS		Shorted with VRT generates, +2.6V.
17	VRT		Reference voltage (Top)
23	VRB		Reference voltage (Bottom)
14, 15, 18	AVDD		Analog +5V
19	VIN		Analog input
20, 21	AVss		Analog GND
22	VRBS		Shorted with VRB generates +0.6V.

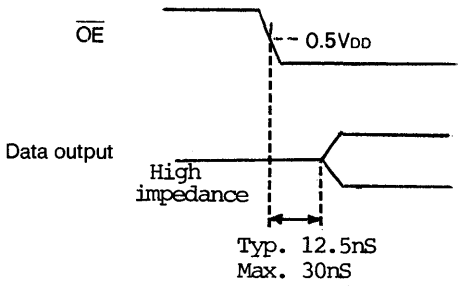
Timing Chart 1

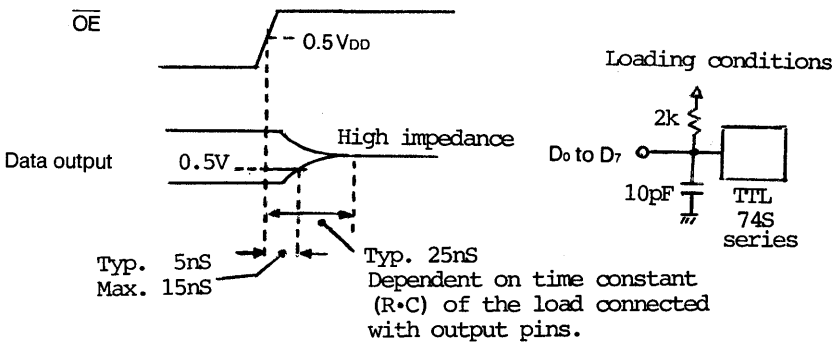
1. Without $\overline{OE}$



o: Point for analog signal sampling.

2. With $\overline{OE}$





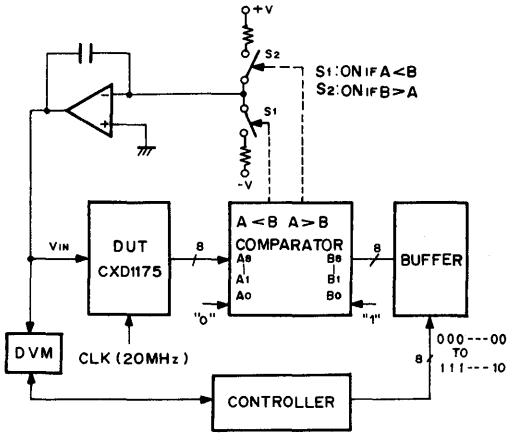
Electrical Characteristics

F_C = 20MSPS, V_{DD} = +5V, V_{RB} = 0.6V, V_{RT} = 2.6V, Ta = 25°C

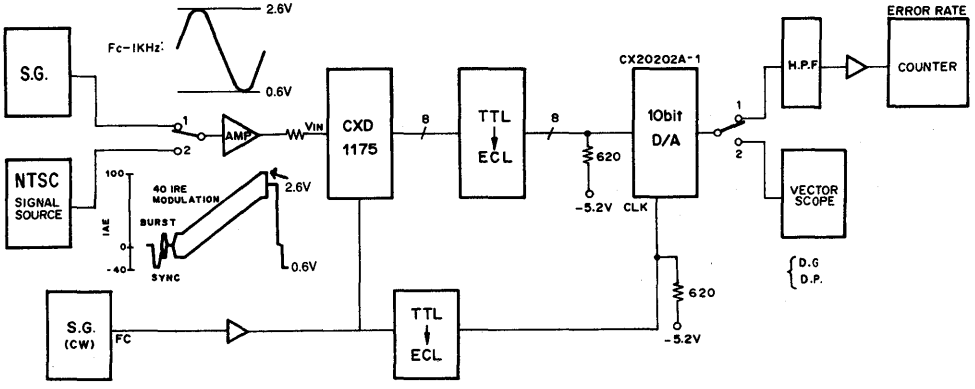
Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Maximum conversion speed	F_C	V_{IN} = 0.6V to 2.6V F_{IN} = 1 kHz ramp		20	25		MSPS
Supply current	I_{DD}	F_C = 20 MSPS NTSC ramp wave input			18	27	mA
Reference pin current	I_{REF}			5.2	7.5	10.5	mA
Analog input band (-1dB)	BW				14		MHz
Analog input capacitance	C_{IN}	V_{IN} = 1.5V + 0.07 Vrms			16		pF
Reference resistance (V_{RT} to V_{RB})	R_{REF}			190	270	350	Ω
Self bias 1	V_{RB1}	Short V_{RB} and V_{RBS}		0.57	0.6	0.65	V
	$V_{RT1} - V_{RB1}$	Short V_{RT} and V_{RTS}		1.90	2.0	2.15	
Self bias 2	V_{RT2}	VRB = AGND Short V_{RT} and V_{RTS}		2.2	2.3	2.40	V
Offset voltage	E_{OT}			-18	-43	-68	mV
	E_{OB}			0	+20	+45	
Digital input voltage	V_{IH}			4.0			V
	V_{IL}					1.0	
Digital input current	I_{IH}	V_{DD} = max.	$V_{IH} = V_{DD}$			5	µA
	I_{IL}		V_{IL} = 0V			5	
Digital output current	I_{OH}	$\overline{OE}$ = V_{SS}, V_{DD} = min.	$V_{OH} = V_{DD} - 0.5V$	-1.5			mA
	I_{OL}		V_{OL} = 0.4V	4.0			
Digital output current	I_{OZH}	$\overline{OE}$= V_{DD}, V_{DD} = max.	$V_{OH} = V_{DD}$			16	µA
	I_{OZL}		V_{OL} = 0V			16	
Output data delay	T_{DL}				18	30	ns
Integral non-linearity	E_L	F_C = 20 MSPS V_{IN} = 0.6V to 2.6V			+0.7	+1.5 -1.0	LSB
Differential non-linearity	E_D	F_C = 20 MSPS V_{IN} = 0.6V to 2.6V		0	±0.3	±0.5	LSB
Differential gain error	DG	NTSC 40 IRE mod ramp, F_C = 14.3 MSPS			1.0		%
Differential phase error	DP				0.7		deg
Aperture jitter	taj				30		ps
Sampling delay	tds				4		ns

Electrical Characteristics Test Circuit

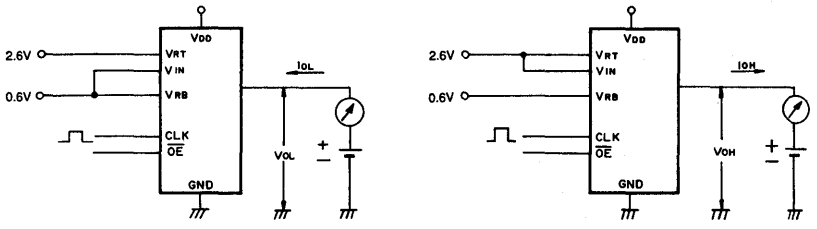
Integral non-linearity error
Differential non-linearity error
Offset voltage
} Test circuit



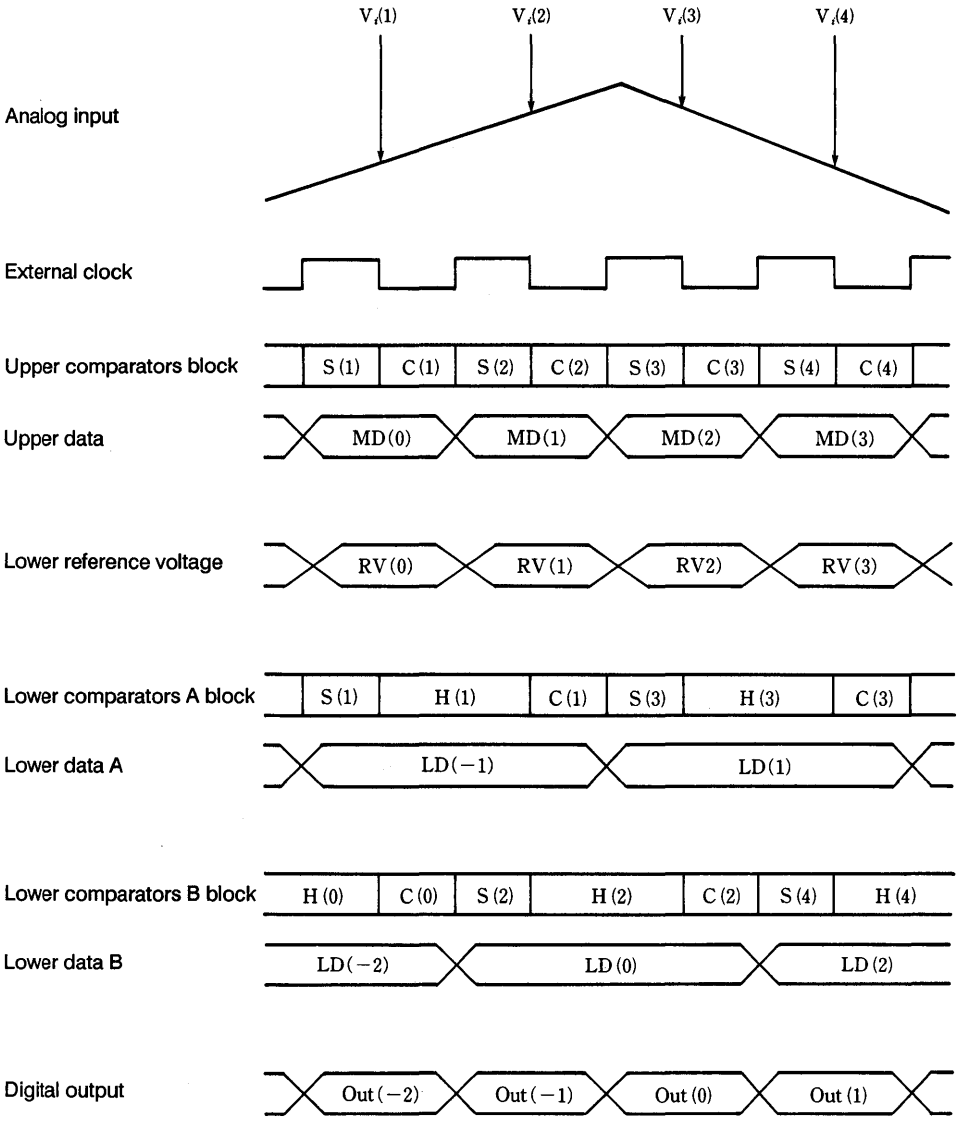
Maximum operational speed
Differential gain error
Differential phase error
} Test circuit



Digital output current test circuit



Timing Chart 2



Operation (See Block Diagram and Timing Chart)

1. CXD1175P/M is a 2-step parallel system A/D converter featuring a 4-bit upper comparators group and 2 lower comparators groups of 4-bit each. The reference voltage that is equal to the voltage between VRT-VRB/16 is constantly applied to the upper 4-bit comparator block. Voltage that corresponded to the upper data is fed through the reference supply to the lower data. VRTS and VRBS pins serve for the self generation of VRT (Reference voltage top) and VRB (Reference voltage bottom).

2. This IC uses an offset cancel type comparator and operates synchronously with an external clock. It features the following operating modes which are respectively indicated on the timing chart with S, H, C symbols. That is input sampling (auto zero) mode, input hold mode and comparison mode.

3. The operation of respective parts is as indicated in the chart. For instance input voltage Vi (1) is sampled with the falling edge of the first clock by means of the upper comparator block and the lower comparator A block.
   The upper comparators block finalizes comparison data MD (1) with the rising edge of the first clock. Simultaneously the reference supply generates the lower reference voltage RV (1) that corresponded to the upper results. The lower comparator block finalizes comparison data LD (1) with the rising edge of the second clock. MD (1) and LD (1) are combined and output as Out (1) with the rising edge of the 3rd clock. Accordingly there is a 2.5 clock delay from the analog input sampling point to the digital data output.

Operation Notes

1. V_{DD}, V_{SS}
   To reduce noise effects, separate the analog and digital systems close to the device. For both the digital and analog V_{DD} pins, use a ceramic capacitor of about 0.1µF set as close as possible to the pin to bypass to the respective GND's.

2. Analog input
   Compared with the flash type A/D converter, the input capacitance of the analog input is rather small. However it is necessary to conduct the drive with an amplifier featuring sufficient band and drive capability. When driving with an amplifier of low output impedance, parasite oscillation may occur. That may be prevented by inserting a resistance of about 100Ω in series between the amplifier output and A/D input.

3. Clock input
   The clock line wiring should be as short as possible also, to avoid any interference with other signals, separate it from other circuits.

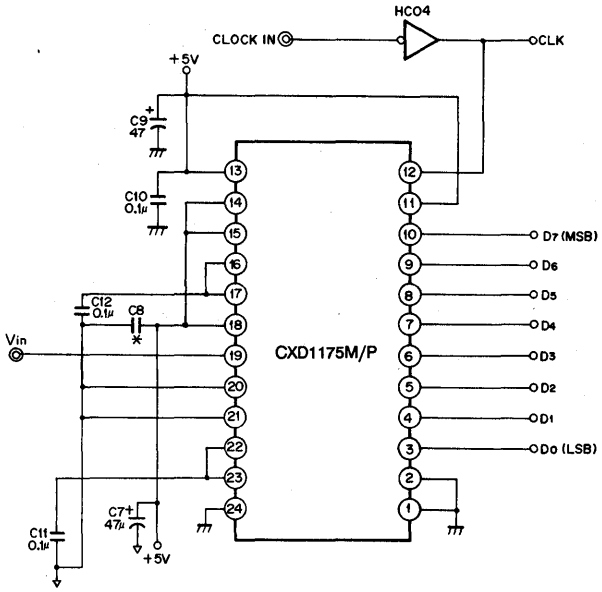
4. Reference input
   Voltage between V_{RT} to V_{RB} is compatible with the dynamic range of the analog input. Bypassing V_{RT} and V_{RB} pins to GND, by means of a capacitor about 0.1µF, stable characteristics are obtained. By shorting V_{RT} and V_{RTS}, V_{RB} and V_{BRS}, the self bias function that generates V_{RT} = 2.6V and V_{RB} = 0.6V, is activated.

5. Timing
   Analog input is sampled with the falling edge of CLK and output as digital data with a delay of 2.5 clocks and with the following rising edge. The delay from the clock rising edge to the data output is about 18ns.

6. $\overline{OE}$ pin
   By connecting $\overline{OE}$ to GND output mode is obtained. By connecting to V_{DD} high impedance is obtained.

7. About latch up
   It is necessary that AV_{DD} and DV_{DD} pins be the common source of power supply.
   This is to avoid latch up due to the voltage difference between AV_{DD} and DV_{DD} pins when power is ON.
   See "For latch up prevention" of CXD1175P/CXA1106P PCB description.

Application Circuit



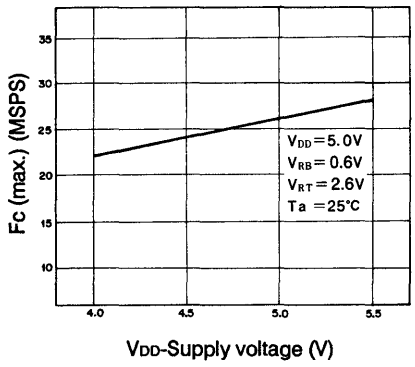
∗ : Ceramic Chip Condenser
0.1μF

⏚ : Analog GND

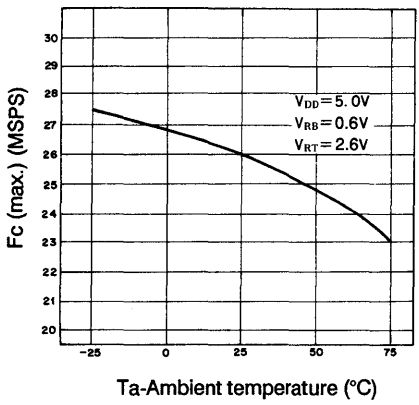
⏚ : Digital GND

Note) It is necessary that AV_{DD} and DV_{DD} pins be the common source of power supply.

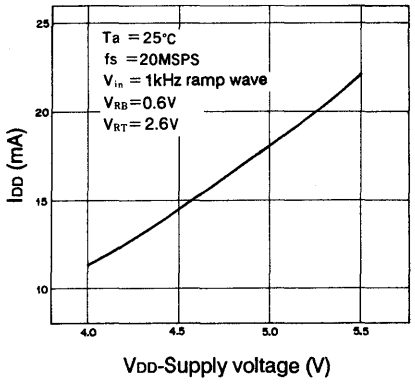
Fc (max.) vs. Supply voltage



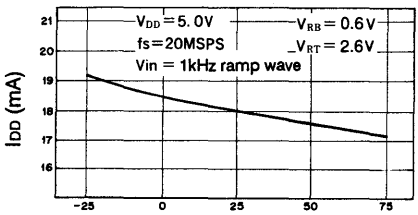
Fc (max.) vs. Ambient temperature

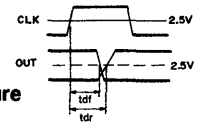


IDD vs. Supply voltage



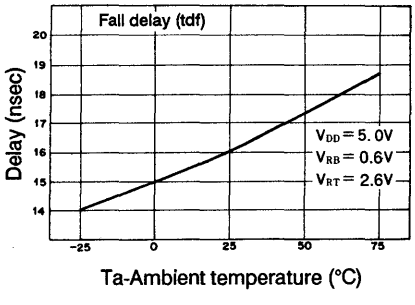
IDD vs. Ambient temperature





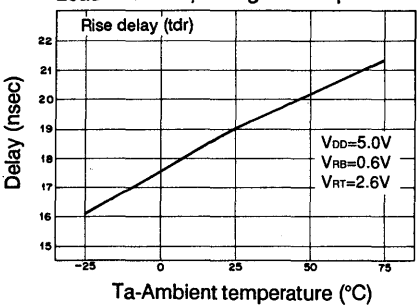
Output Delay vs. Ambient temperature

Load = TTLS ϕ one gate + 10 pF

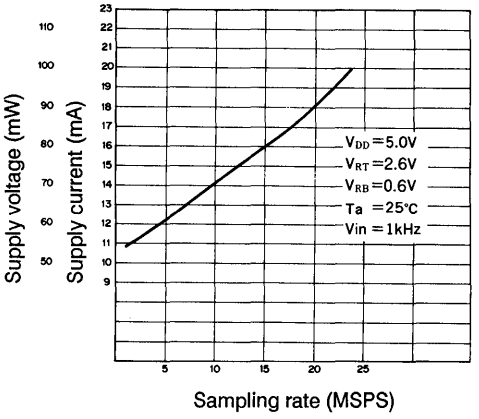


Output Delay vs. Ambient temperature

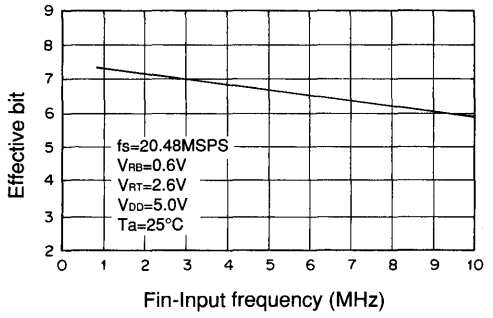
Load = TTLS ϕ one gate + 10pF



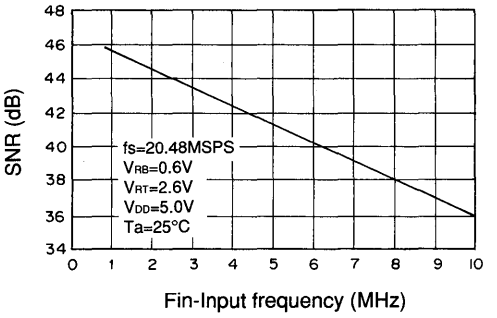
Supply current (voltage) vs. Sampling rate



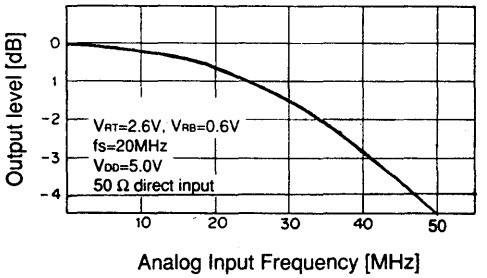
Eff bit vs. Fin



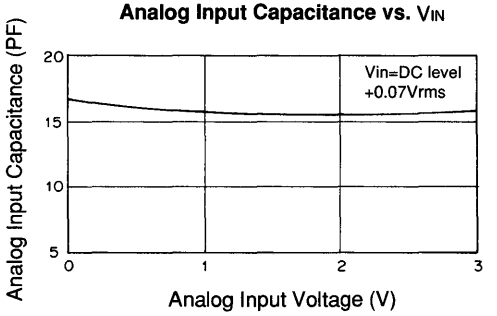
SNR vs. Fin



Output Level vs. Fin

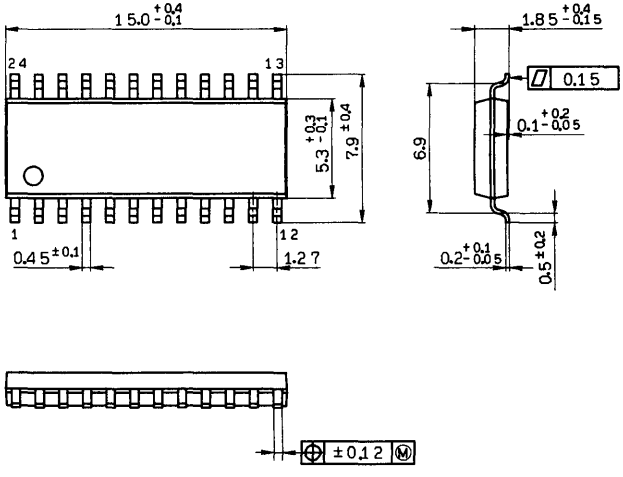


Analog Input Capacitance vs. V_{IN}



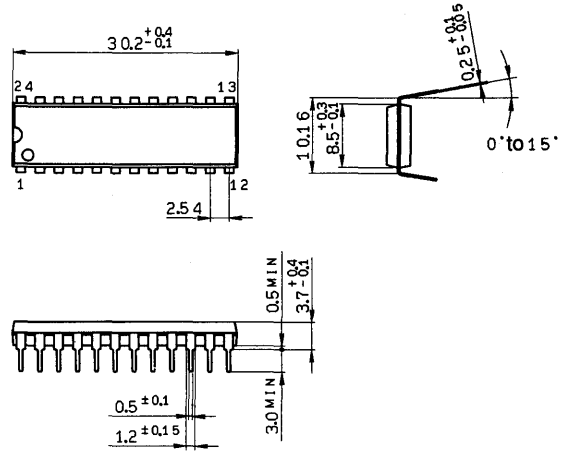
Package Outline Unit: mm

CXD1175M 24 pin SOP (Plastic) 300mil 0.3 g



SOP-24P-L01

CXD1175P 24 pin DIP (Plastic) 400mil 2.0 g



DIP-24P-01

SONY® CXD1175AM/AP

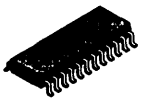
8-bit 20 MSPS Video A/D Converter (CMOS) **Preliminary**

Evaluation Board Available — CXD1175AP/CXA1106P PCB

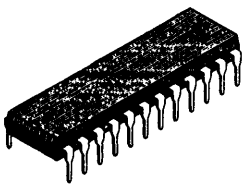
Description

CXD1175A is an 8-bit CMOS A/D converter for video use. The adoption of a 2-step parallel system achieves low consumption at a maximum conversion speed of 20 MSPS minimum, 35MSPS typical.

CXD1175AM 24 pin SOP (Plastic)



CXD1175AP 24 pin DIP (Plastic)



Features

- Resolution ..... 8-bit ± 1/2 LSB (DL)
- Max. sampling frequency .... 20 MSPS
- Low power consumption .... 60 mW (at 20 MSPS Typ.) (Reference current excluded)
- Built-in sampling and hold circuit.
- Built-in reference voltage self bias circuit.
- 3-state TTL compatible output.
- Power supply ..... 5V single
- Low input capacitance ..... 11 pF
- Reference impedance ..... 360Ω (Typ.)
- **Pin replacable with** CXD1175M/P

Structure

Silicon gate CMOS monolithic IC

Applications

- TV, VCR digital systems and a wide range of fields where high speed A/D conversion is required.

Absolute Maximum Ratings (Ta=25°C)

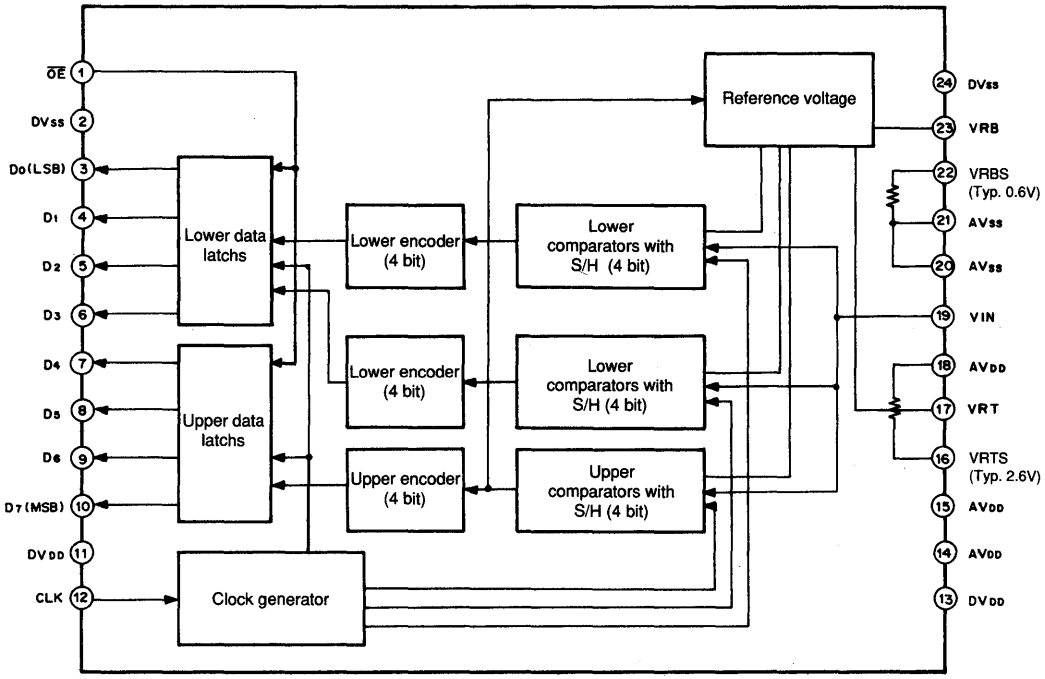
• Supply voltage	V_{DD}		7		V
• Reference voltage	V_{RT}, V_{RB}	V_{DD}	to	V_{SS}	V
• Analog input voltage	V_{IN}	V_{DD}	to	V_{SS}	V
• Digital input voltage	CLK	V_{DD}	to	V_{SS}	V
• Digital output voltage	V_{OH}, V_{OL}	V_{DD}	to	V_{SS}	V
• Storage temperature	Tstg	-55	to	+150	°C

Recommended Operating Conditions

• Supply voltage	AV_{DD}, AV_{SS}	4.75 to 5.25	V
	DV_{DD}, DV_{SS}		
	$\lvert DGND-AGND \rvert$	0 to 100	mV
• Reference input voltage	V_{RB}, V_{RT}	$0 \leqq V_{RB} < V_{RT} \leqq 2.7$	V
	$V_{RT}-V_{RB}$	1.8 to AV_{DD}	V
• Analog input voltage	V_{IN}	V_{RB} to V_{RT}	(1.8Vp-p to AV_{DD}Vp-p)
• Clock pulse width	T_{PWI}	25 (Min.)	ns
	T_{PWO}	25 (Min.)	ns
• Operating temperature	Topr	-20 to +75	°C

E89321-YA

Block Diagram and Pin Configuration



Digital Output

Compatibility between Analog input voltage and the digital output code is indicated in the chart below.

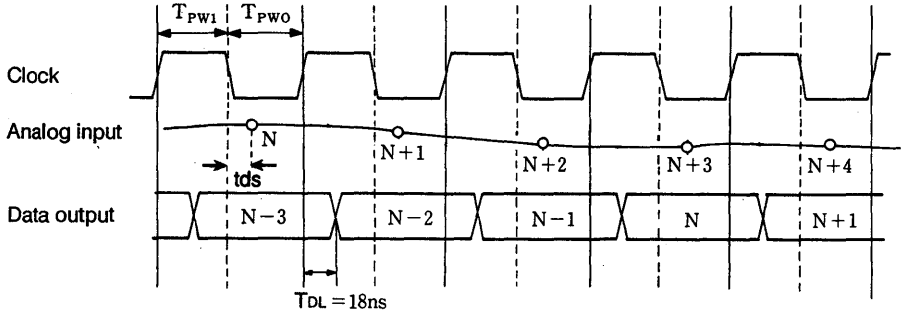
Input signal voltage	Step	Digital output code MSB							LSB
V_{RT}	0	1	1	1	1	1	1	1	1
	⋮					⋮			
	127	1	0	0	0	0	0	0	0
	128	0	1	1	1	1	1	1	1
	⋮					⋮			
V_{RB}	255	0	0	0	0	0	0	0	0

For the following information, please see CXD1175M/P portion.

- Pin Description and Equivalent Circuits
- Description of Operation
- Application Circuit

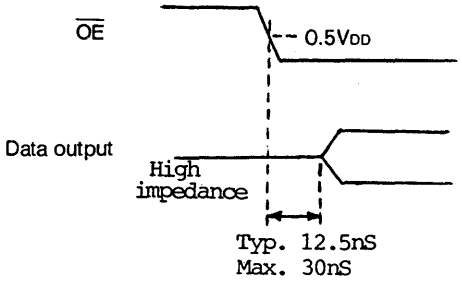
Timing Chart 1

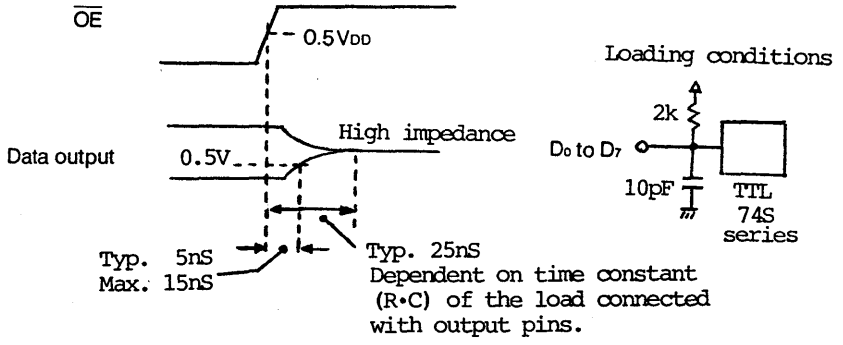
1. Without $\overline{OE}$



O: Point for analog signal sampling.

2. With $\overline{OE}$





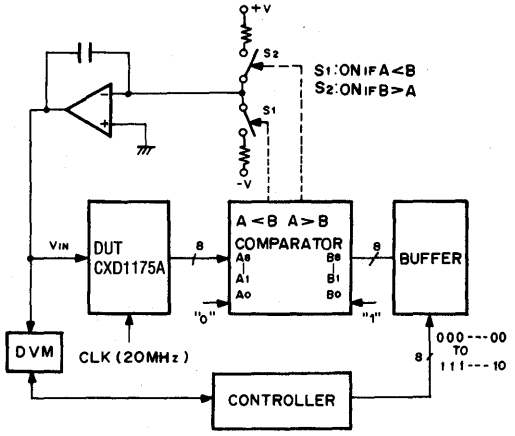
Electrical Characteristics

F_C = 20MSPS, V_{DD} = +5V, V_{RB} = 0.6V, V_{RT} = 2.6V, Ta = 25°C

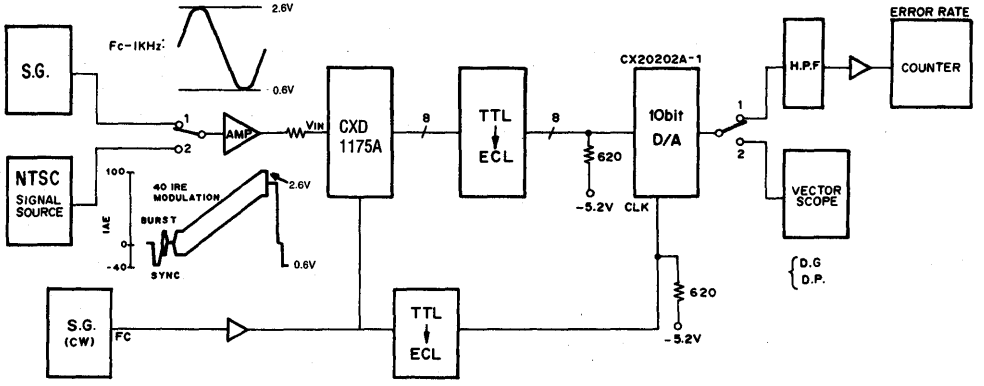
Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Maximum conversion speed	F_C	V_{IN} = 0.6V to 2.6V F_{IN} = 1 kHz ramp		20	35		MSPS
Supply current	I_{DD}	F_C = 20 MSPS NTSC ramp wave input			12		mA
Reference pin current	I_{REF}				5.6		mA
Analog input band (−1dB)	BW				20		MHz
Analog input capacitance	C_{IN}	V_{IN} = 1.5V + 0.07 Vrms			11		pF
Reference resistance (V_{RT} to V_{RB})	R_{REF}				360		Ω
Self bias 1	V_{RB1}	Short V_{RB} and V_{RBS}			0.6		V
	V_{RT1} - V_{RB1}	Short V_{RT} and V_{RTS}			2.0		
Self bias 2	V_{RT2}	VRB = AGND Short V_{RT} and V_{RTS}			2.3		V
Offset voltage	E_{OT}				−40		mV
	E_{OB}				+20		
Digital input voltage	V_{IH}			4.0			V
	V_{IL}					1.0	
Digital input current	I_{IH}	V_{DD} = max.	V_{IH} = V_{DD}			5	µA
	I_{IL}		V_{IL} = 0V			5	
Digital output current	I_{OH}	$\overline{OE}$ = V_{SS}, V_{DD} = min.	V_{OH} = V_{DD} − 0.5V	−1.3			mA
	I_{OL}		V_{OL} = 0.4V	3.7			
Digital output current	I_{OZH}	$\overline{OE}$= V_{DD}, V_{DD} = max.	V_{OH} = V_{DD}			16	µA
	I_{OZL}		V_{OL} = 0V			16	
Output data delay	T_{DL}				18	30	ns
Integral non-linearity	E_L	F_C = 20 MSPS V_{IN} = 0.6V to 2.6V			+0.5	+1.0 −0.5	LSB
Differential non-linearity	E_D	F_C = 20 MSPS V_{IN} = 0.6V to 2.6V		0	±0.3	±0.5	LSB
Differential gain error	DG	NTSC 40 IRE mod ramp, F_C = 14.3 MSPS			1.0		%
Differential phase error	DP				0.5		deg
Aperture jitter	taj				30		ps
Sampling delay	tds				4		ns

Electrical Characteristics Test Circuit

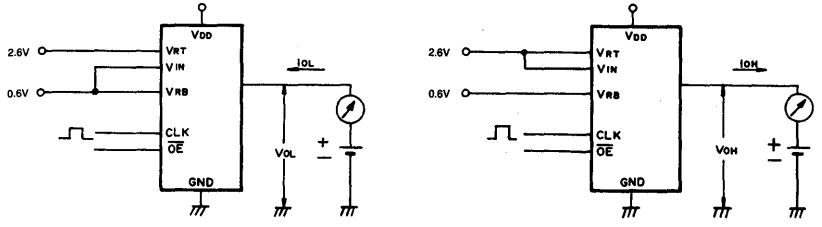
Integral non-linearity error
Differential non-linearity error
Offset voltage
} Test circuit



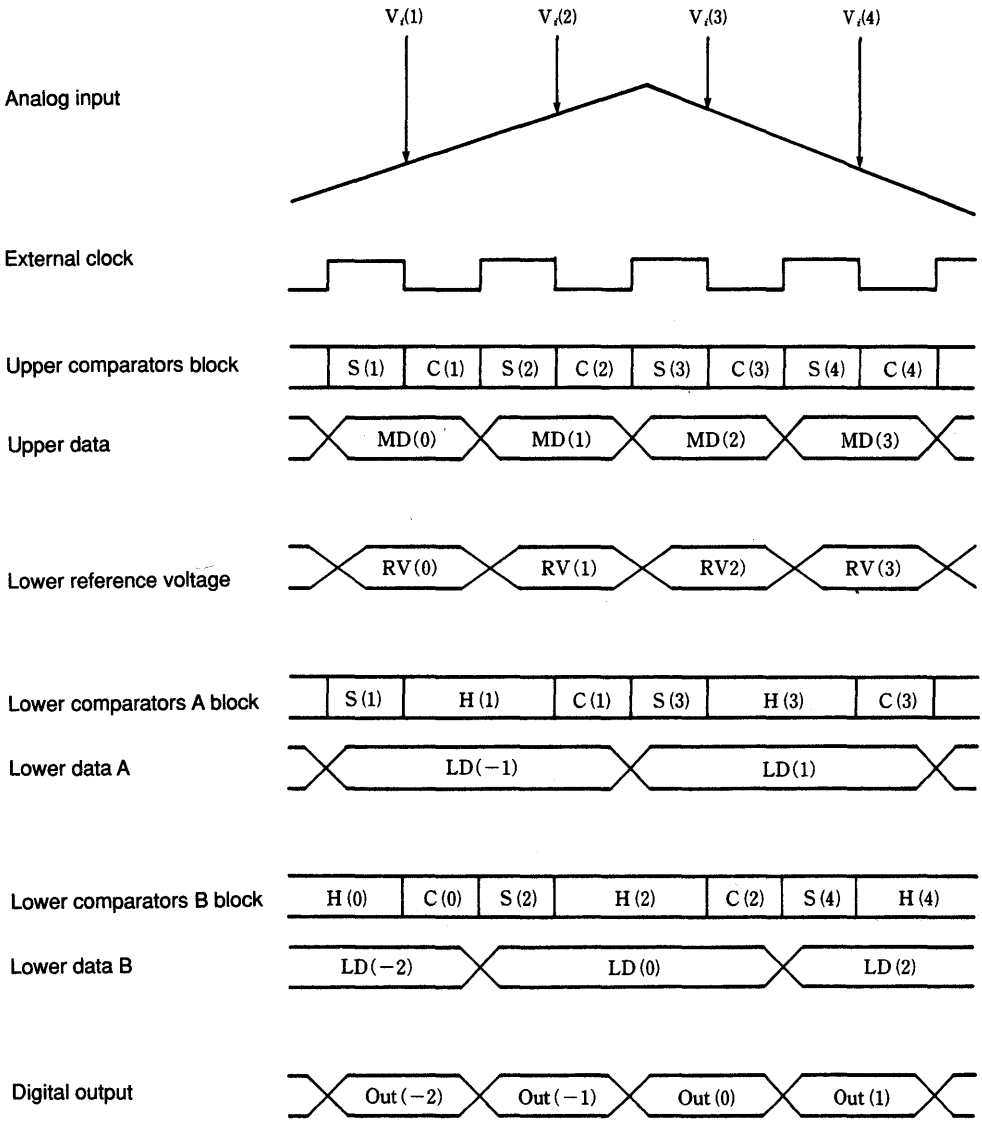
Maximum operational speed
Differential gain error
Differential phase error
} Test circuit



Digital output current test circuit



Timing Chart 2



Operation Notes

1. V_{DD}, V_{SS}
   To reduce noise effects, separate the analog and digital systems close to the device. For both the digital and analog V_{DD} pins, use a ceramic capacitor of about 0.1μF set as close as possible to the pin to bypass to the respective GND's.

2. Analog input
   Compared with the flash type A/D converter, the input capacitance of the analog input is rather small. However it is necessary to conduct the drive with an amplifier featuring sufficient band and drive capability. When driving with an amplifier of low output impedance, parasite oscillation may occur. That may be prevented by inserting a resistance of about 100Ω in series between the amplifier output and A/D input.

3. Clock input
   The clock line wiring should be as short as possible also, to avoid any interference with other signals, separate it from other circuits.

4. Reference input
   Voltage between V_{RT} to V_{RB} is compatible with the dynamic range of the analog input. Bypassing V_{RT} and V_{RB} pins to GND, by means of a capacitor about 0.1μF, stable characteristics are obtained. By shorting V_{RT} and V_{RTS}, V_{RB} and V_{BRS}, the self bias function that generates V_{RT} = 2.6V and V_{RB} = 0.6V, is activated.

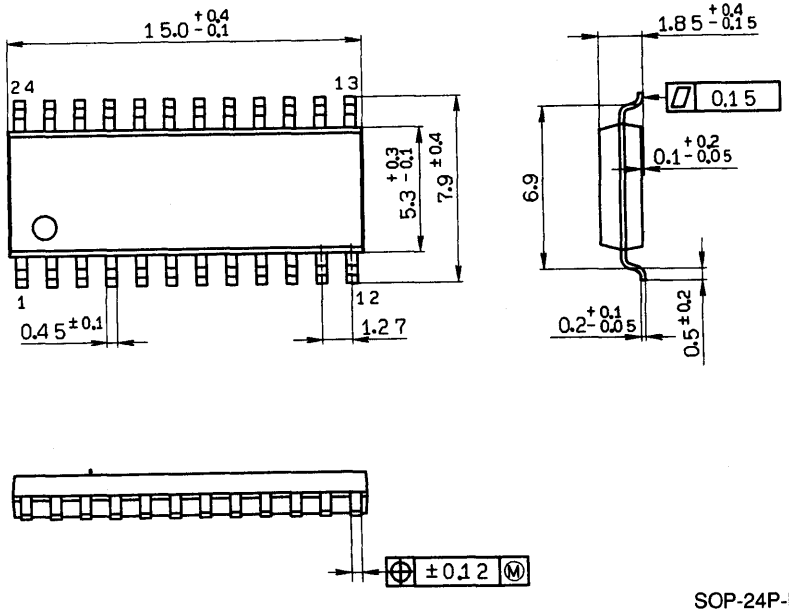
5. Timing
   Analog input is sampled with the falling edge of CLK and output as digital data with a delay of 2.5 clocks and with the following rising edge. The delay from the clock rising edge to the data output is about 18ns.

6. $\overline{OE}$ pin
   By connecting $\overline{OE}$ to GND output mode is obtained. By connecting to V_{DD} high impedance is obtained.

7. About latch up
   It is necessary that AV_{DD} and DV_{DD} pins be the common source of power supply.
   This is to avoid latch up due to the voltage difference between AV_{DD} and DV_{DD} pins when power is ON.
   See "For latch up prevention" of CXD1175AP/CXA1106P PCB description.

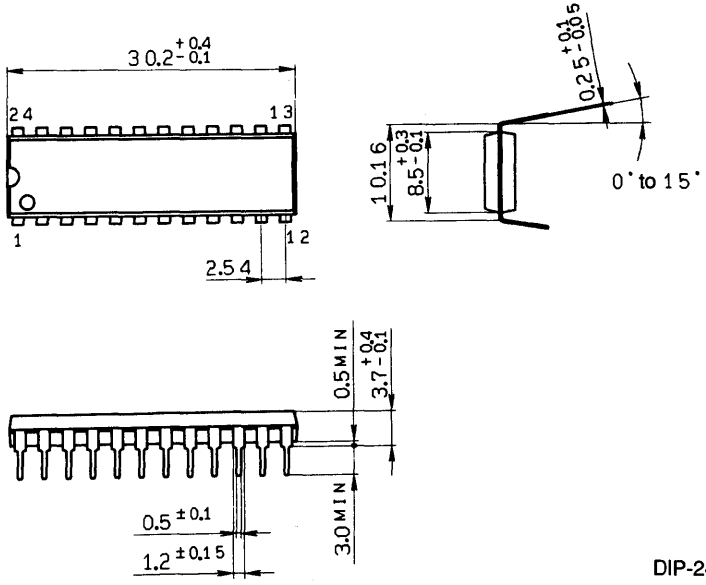
Package Outline Unit: mm

CXD1175AM 24 pin SOP (Plastic) 300 mil 0.3 g



SOP-24P-L01

CXD1175AP 24 pin DIP (Plastic) 400 mil 2.0 g



DIP-24P-01

8-bit 20MSPS A/D Converter with Clamp(CMOS)

Advance Information

Sample Available 1Q90
Production Start 3Q90

CXD1176Q
32pin QFP(Plastic)

Description

The CXD1176 is an 8-bit CMOS A/D converter for video use with a built-in clamp circuit. The adoption of a 2-step parallel system in the A/D converter realizes low power consumption and a maximum converting speed of 20MSPS.

Features

- Resolution···8-bit±½LSB(DL)
- Maximum sampling frequency···20MSPS
- Low power consumption ···60mW(at 20MSPS Typ.)
- Built-in monostable multivibrator function
- Sync pulse polarity selectable
- Clamp ON/OFF function
- Built-in sample and hold function
- Built-in reference voltage self bias circuit
- Input CMOS and TTL compatible
- 3-state CMOS and TTL compatible output
- Power supply···5V single
- High f characteristics···60MHz(-3dB)
- Low input capacitance ···11pF

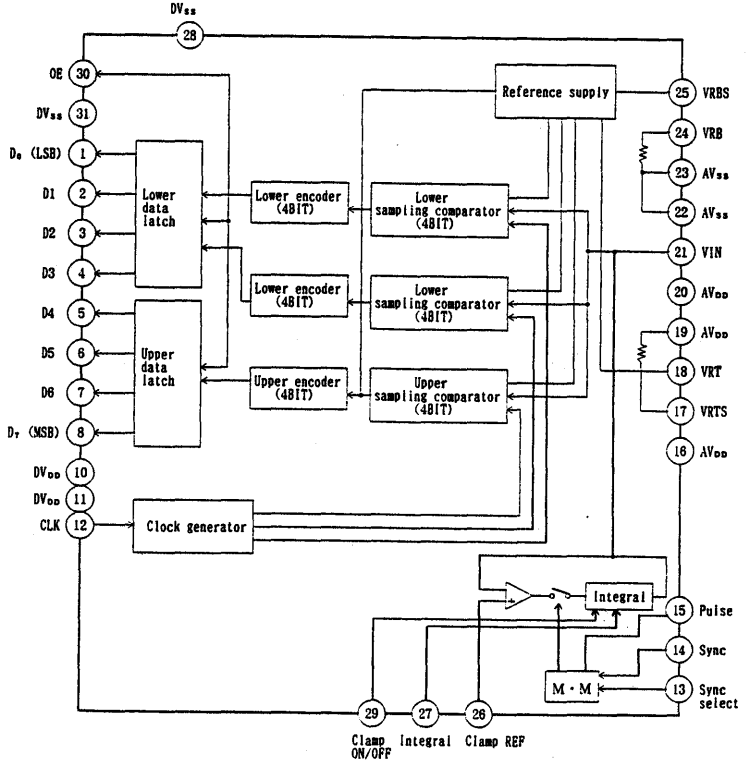
Applications

A wide range of applications is open in such fields that require TV and VCR digital system and high speed A/D conversion.

Structure

Silicon gate CMOS IC

Block Diagram



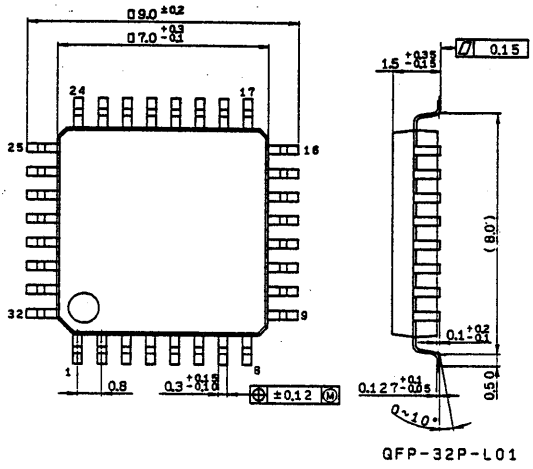
AE89776

Absolute Maximum Ratings (Ta=25℃)

• Supply voltage	V_{DD}	7	V
• Reference voltage	V_{RT}, V_{RB}	V_{DD}～V_{SS}	V
• Input voltage(Analog)	V_{IN}	V_{DD}～V_{SS}	V
• Input voltage(Digital)	V_{IH}, V_{IL}	V_{DD}～V_{SS}	V
• Output voltage(Digital)	V_{OH}, V_{OL}	V_{DD}～V_{SS}	V
• Storage temperature	T_{stg}	−55～+150	℃

Package Outline Unit:mm

CXD1176Q 32pin QFP(Plastic) 0.2g



QFP-32P-L01

SONY BX-1500

10-bit, 18 MSPS A/D Converter Module (ECL I/O)

Description

BX-1500 is a 10-bit, 18 MSPS A/D converter module for high resolution video signal processing, in which 10-bit, 20 MSPS serial/parallel type high speed A/D converter IC and necessary peripheral circuits are combined.

Mounting Outline

Features

- Sample hold circuit, built-in constant-voltage regulated power supply.
- Clock input, Digital output ECL level.
- Operation possible only by connecting a clock pulse circuit and the power supply.
- Resolution 10-bit
- Maximum conversion rate 18 MSPS (Min.)
- Analog input level 2Vp-p
- Digital output level ECL level
- Supply voltage ±5V
- Power consumption 1.4W

Structure

Hybrid IC

Absolute Maximum Ratings (Ta = 25°C)

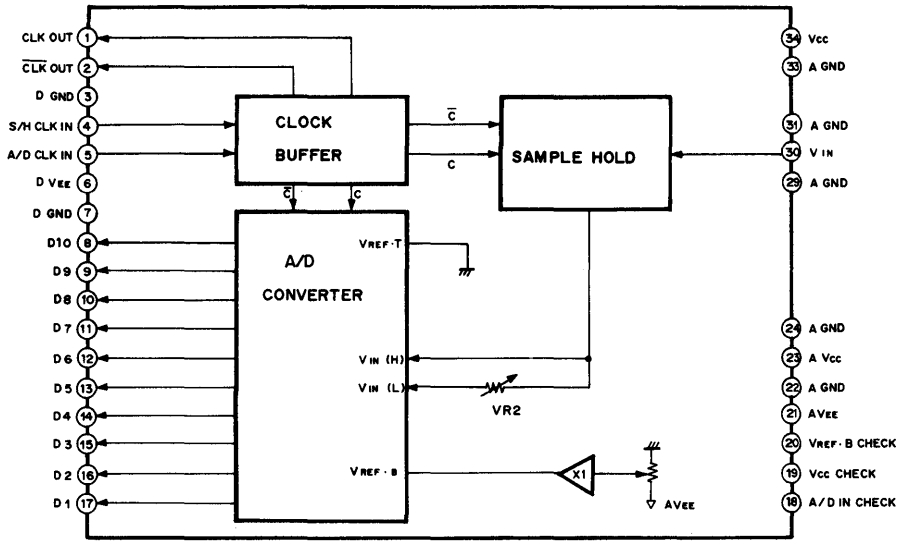
• Supply voltage	V_{CC}	+7.0	V
	V_{EE}	−7.0	V
• Analog input voltage	V_{IN}	V_{EE} to 0.3	V
• Clock input voltage	V_{CLK}, $V_{\overline{CLK}}$	V_{EE} to 0.3	V
• Digital output current	I_{O1} to I_{10}	−20 to 0	mA
• Operating temperature	T_{opr}	−15 to +65	°C
• Storage temperature	T_{stg}	−25 to +80	°C

Recommended Operating Conditions

• Supply voltage	V_{CC}	+5.0 ±0.25	V
	V_{EE}	−5.0 ±0.25	V
• Clock input voltage	V_{CLK} (High)	−1.1 (Min.)	V
	V_{CLK} (Low)	−1.4 (Max.)	V
• Input signal voltage	V_{IN}	−2 to 0	V

E89184-HP

Block Diagram and Pin Configuration



Pin Description

No.	Symbol	Description
1	CLK OUT	Clock output (ECL), Open emitter
2	$\overline{\text{CLK}}$ OUT	Clock inverted output (ECL), Open emitter
3	DGND	Digital ground
4	S/H CLK IN	Sample hold clock input (ECL)
5	A/D CLK IN	ADC clock input (ECL)
6	DVEE	Digital VEE (−5V−D)
7	DGND	Digital ground
8	D10 (LSB)	Digital output
9	D9	Digital output
10	D8	Digital output
11	D7	Digital output
12	D6	Digital output
13	D5	Digital output
14	D4	Digital output

No.	Symbol	Description
15	D3	Digital output
16	D2	Digital output
17	D1 (MSB)	Digital output
18	A/D IN CHECK	Input signal check of ADC
19	VCC CHECK	VCC check of ADC
20	VREF.B CHECK	Reference electric potential check of ADC
21	AVEE	Analog VEE (−5V−A)
22	AGND	Analog ground
23	AVCC	Analog VCC (+5V−A)
24	AGND	Analog ground
29	AGND	Analog ground
30	VIN	Analog input
31	AGND	Analog ground
33	AGND	Analog ground
34	VCC	VCC (+5V−A, −D)

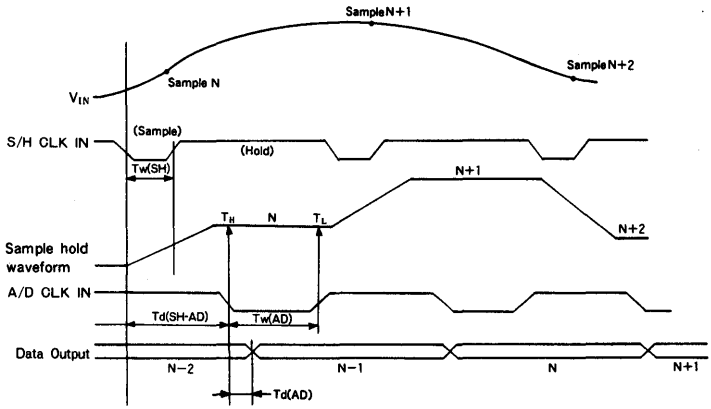
−A: ANALOG −D: DIGITAL

Electrical Characteristics

Ta = 25°C, Vcc = 5V, VEE = −5V
Tw(SH) = 22 ns, Td(SH−AD) = 34ns, TW (AD) = 23ns

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Resolution	n			10		bit
Conversion rate	$f_{CLK\ (MAX)}$		18			MSPS
Integral Lineanty	ILE			±1.0	±1.5	LSB
Differential Linearity	DLE				±1.0	LSB
Differential gain error	DG	NTSC 40 IRE mod ramp, f_{CLK} = 18 MHz		0.5	0.7	%
Differential phase error	DP	NTSC 40 IRE mod ramp, f_{CLK} = 18 MHz		0.3	0.4	deg
Consumption current (1)	I_{CC}			90	120	mA
Consumption current (2)	I_{EE}		−240	−185		mA
Analog input current	I_{IN}			200		μA
Analog input capacity	Cin				10	pF
Analog input offset	Voff			−60		mV
Analog input band width	BW	0.7dB down by 1.8Vp-p input		9		MHz
Digital input current	I_{IH}				200	μA
Digital input current	I_{IL}				200	μA
Digital output voltage H(1)	V_{OH1}	No pull-down resistor connected.	−1.0	−0.8		V
Digital output voltage H(2)	V_{OH2}	1 kΩ pull-down resistor.		−1.0		V
Digital output voltage L(1)	V_{OL1}	No pull-down resistor connected.		−1.6	−1.4	V
Digital output voltage L(2)	V_{OL2}	1kΩ pull-down resistor.		−1.9		V
Clock output voltage H	V_H		−0.98		−0.81	V
Clock output voltage L	V_L		−1.95		−1.63	V
Output data delay	Td			5		ns

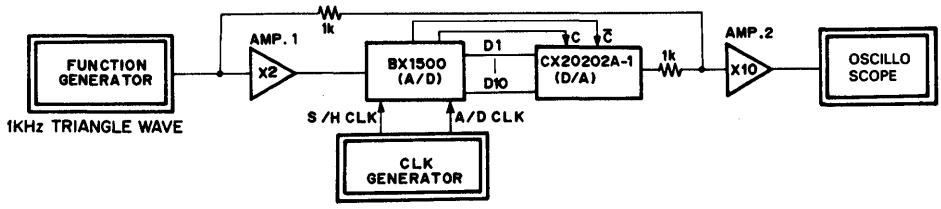
Timing Chart



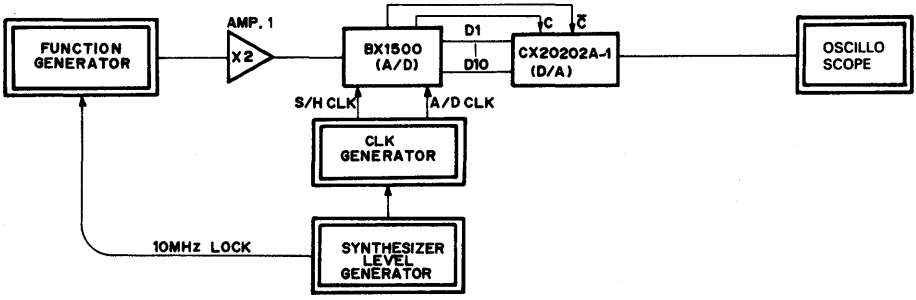
TH is a timing for the upper comparator to compare VIN and VREF and latch its result. TL is a timing for the lower comparator to compare VIN and VREF and latch its result.

Item	Symbol	Min.	Typ.	Max.	Unit
Sampling pulse width	Tw (SH)		22		ns
A/D clock delay	Td (SH-AD)		34		ns
A/D clock pulse width	Tw (AD)	23			ns
A/D output data delay	Td (AD)		6		ns

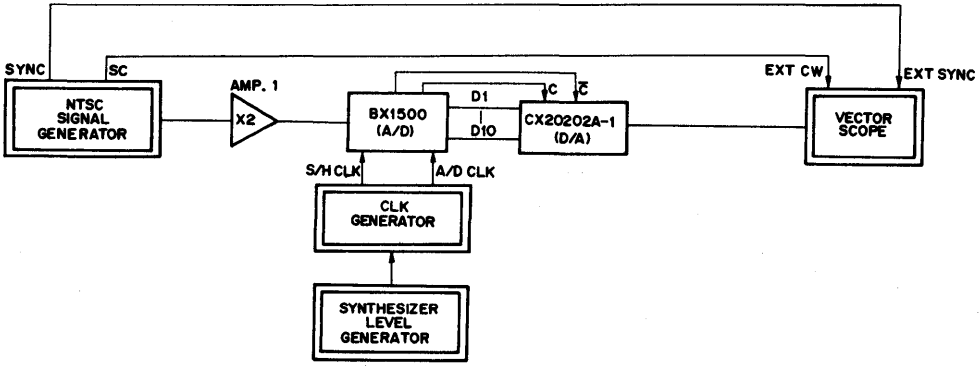
Electrical Characteristics Test Circuit 1



Differential linearity error test circuit

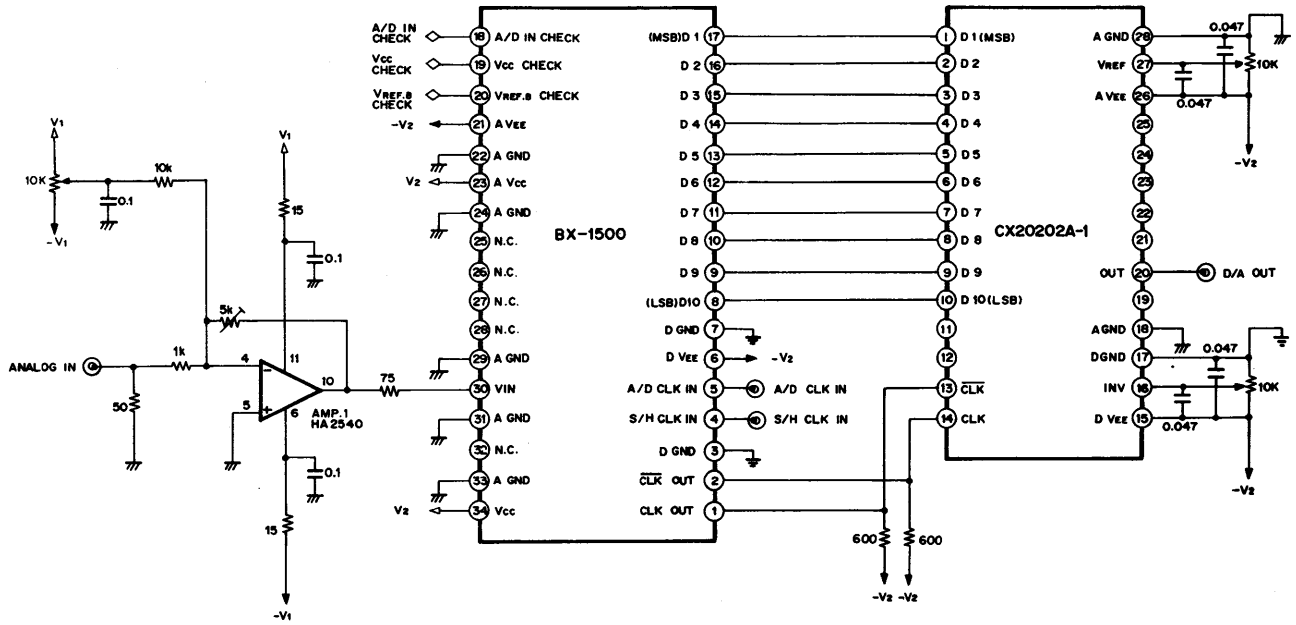


Envelope test circuit

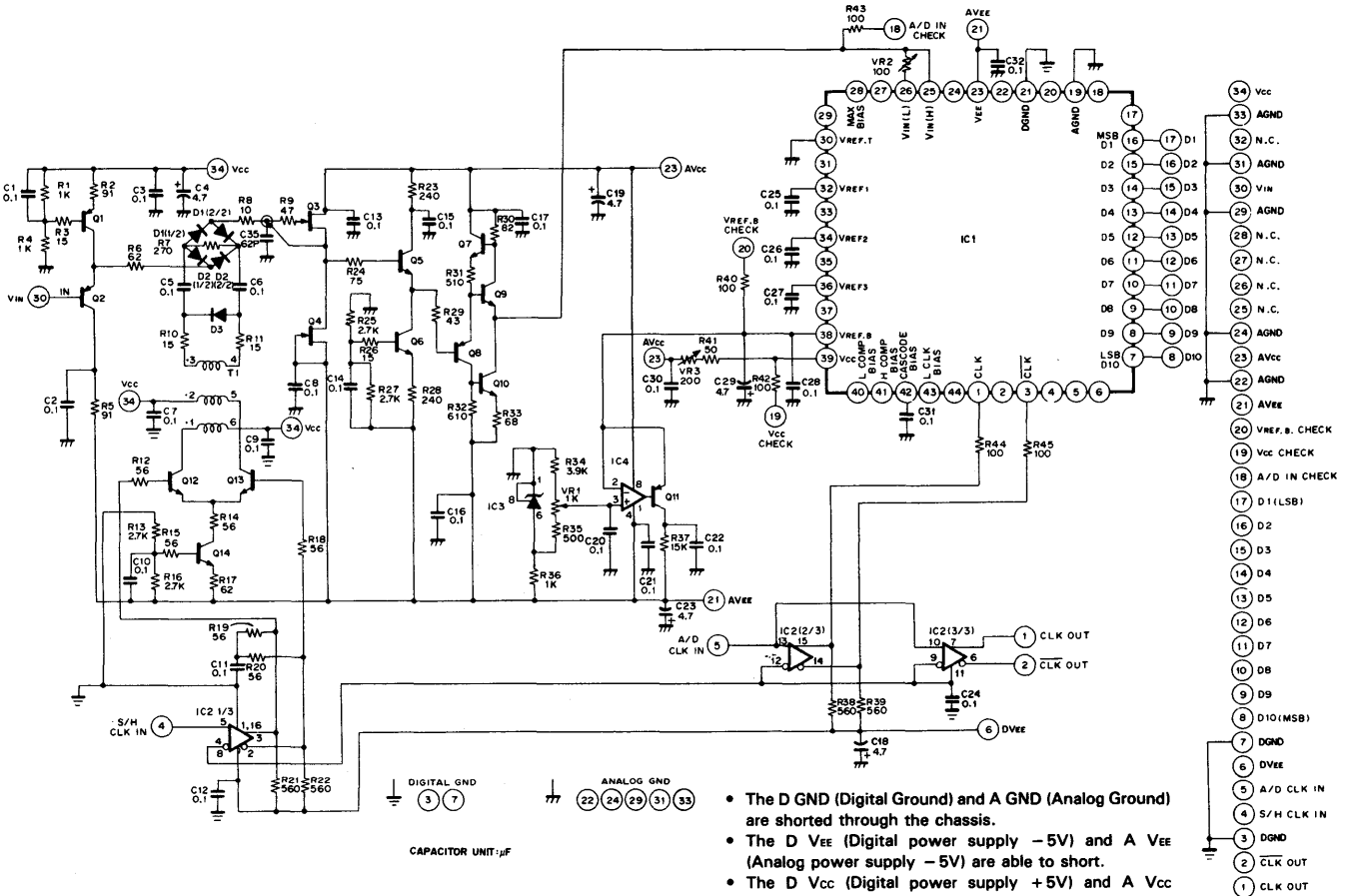


DG · DP test circuit

Electrical Characteristics Test Circuit 2

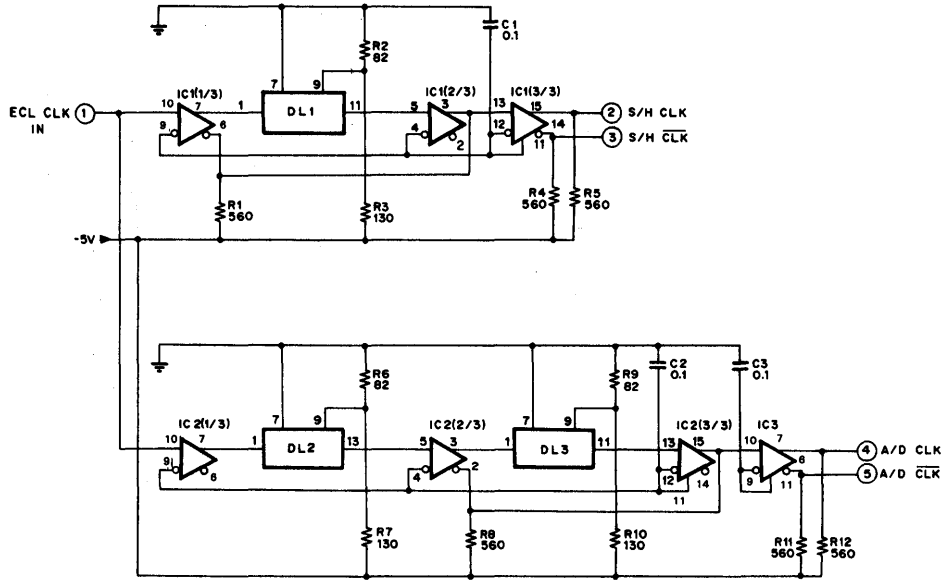


Equivalent Circuit



- The D GND (Digital Ground) and A GND (Analog Ground) are shorted through the chassis.
- The D V_{EE} (Digital power supply −5V) and A V_{EE} (Analog power supply −5V) are able to short.
- The D V_{CC} (Digital power supply +5V) and A V_{CC} (Analog power supply +5V) are able to short.

Timing Clock Generating Circuit



CAPACITOR UNIT : μF

Symbol	Name	Products name	Manufacture
DL1, DL3	DIL DELAY LINES	SDL20N500	JPC
DL2	DIL DELAY LINES	SDL50N500	JPC
IC1, IC2, IC3	MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC	MC10H116	MOTOROLA
C1, C2, C3	CERAMIC CHIP CAPACITOR	CM21W5R104K 20VDC (0.1μF)	KYOCERA

Notes on Operation

1. **Ground pins (AGND, DGND)**
   The analog ground and digital ground are shorted on the BX-1500 chassis. Provide a wider GND space as far as possible to reduce impedance when mounting on a printed circuit board.

2. **Power supply pins (VCC, AVCC)**
   VCC = +5V, AVCC = +5V
   No problem in using VCC and AVCC in common.

3. **Power supply pins (AVEE, DVEE)**
   AVEE = −5V, DVEE = −5V
   No problem in using AVEE and DVEE in common.

4. **Analog input (VIN)**
   Input impedance at the analog input stage is 10 kΩ or more. When an analog signal is input to the BX-1500, it is necessary to cope with an analog input offset existing in the BX-1500. For that purpose, monitor the pin 18 (A/D IN CHECK) and take measures to make the dynamic range for that analog signal be 0 to −2 V.
   For normal use, keep the pin 18 open.

5. **Damping resistor (VR2)**
   The damping resistor has been adjusted at the time of shipment so that the differential linearity and envelope property are the optimum when a recommended clock signal is input. When the clock inputs [Tw(SH) = 22ns, Tw(SH) = 23ns, Td(SH-AD) = 34ns] are a little out of the recommended values, the damping resistor must be fine-adjusted.

6. **Reference voltage (VREF.B CHECK)**
   A bias circuit is incorporated into the BX-1500 to generate the ADC reference voltage. Usually, this value has been set to −2V which can be checked with pin 20. For normal use, keep the pin 20 open.

7. **Clock input (S/H CLK IN, A/D CLK IN)**
   Two phases of the ECL level clock must be added to the clock. One is added to pin 4 for the inner sample hold circuit (S/H) and the other is added to Pin 5 for the inner serial/parallel ADC.
   The input clock wave is rectified in the inner IC2. To the clock input pin, no pull-down resistor is connected. (See "Equivalent Circuit".)
   When a clock signal is input, be sure to adjust the phase difference- [Td (SH-AD)] and the pulse width [Tw (SH), Tw (AD)].
   See "Timing Chart" item for the clock timing.
   For generating a two-phase clock signal, see "Timing Clock Generating Circuit".

8. **Clock output, inverted clock output (CLK OUT, CLK OUT)**
   The clock input for ADC is output to pins 1 and 2 via the inner IC2. The output is an open-emitter and the receiver side must have a pull-down resistor. (See "Electrical Characteristics Test Circuit 2".) The output data is output delaying this clock by the A/D output delay (Td).

9. Others

Pin 19 is a monitor pin for the inner ADC plus power supply.
For normal use, keep the pin 19 open.

10. Digital output (D1 through D10)

Although a 10 kΩ pull-down resistor is built into the digital output stage, a 1 kΩ or larger resistor can further be connected to it externally.
In this case, however, care must be taken about changes in the output level.
The "Output Data Format" shows the relationship between analog input voltage and digital output code.

11. How to match timing

Refer to "Timing Chart".
When an analog input signal and a sample hold clock signal (clock LOW period TW (SH) = 22ns) are added to the BX-1500, the sample hold circuit output or inner ADC input waveform shows a sample hold waveform.
Further, when an A/D clock signal (clock LOW period Tw(AD) = 23ns) delaying Td(SH-AD) for the sample hold clock is added to the BX-1500, the ADC upper level comparator compares VIN and VREF in a TH timing as shown in the diagram and latches the result the ADC lower level comparator compares VIN and VREF in a TL timing and latches the result.
The BX-1500 output data is output delaying Td for the ADC clock.
TW (SH) is a sampling time in the BX-1500 sample hold circuit.
The Td (SH-AD) time is an A/D clock delay. This time becomes longer than the time required for settling a sample hold circuit output in the BX-1500. Therefore, when TW (SH) is made longer, for example, to widen the analog input bandwidth, the sample hold settling time becomes longer and accordingly the Td (SH-AD) time has to be made longer.
The TW (AD) time is an A/D clock pulse width. The minimum 23 ns is required so that no error occurs in the inner serial/parallel ADC.

12. Example of clock generation

Example of a clock generation circuit for the two-phase clock signal to be input to the BX-1500 is shown in the "Timing Clock Generating Circuit".
A sample hold clock signal is generated from IC1 and DL1. TW (SH) is determined by DL1.
The A/D clock signal is generated by IC2, IC3, DL2 and DL3. Td (SH-AD) is determined by DL2 and TW (AD) is determined by DL3.
When ECL clock signal is input to pin 1, S/H CLK is output to pin 2 and A/D CLK to pin 4.
Be sure to input these clock signals to the pin 4 S/H CLK IN and pin 5 A/D IN of BX-1500.

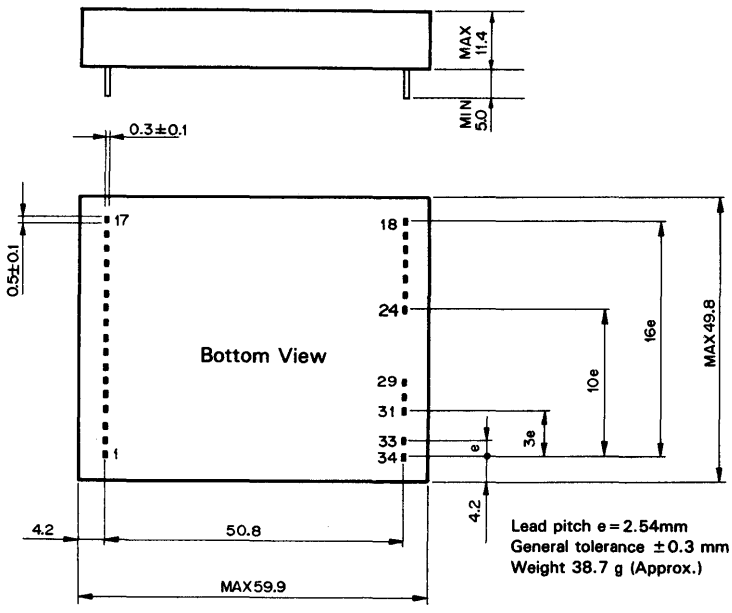
Output Data Format

The A/D converter input (S/H out) is quantified in 10 bit within the range of reference voltage $V_{REF.T}$ to $V_{REF.B}$. The module has been set to $V_{REF.T} = 0V$ and $V_{REF.B} = -2V$.

A/D input signal voltage	Step	Digital output code (binary) MSB 1 2 3 4 5 6 7 8 9 10 LSB
$V_{REF.T}$	0 0 0 0	1 1 1 1 1 1 1 1 1 1
	0 0 0 1	1 1 1 1 1 1 1 1 1 0
	0 5 1 1	1 0 0 0 0 0 0 0 0 1
	0 5 1 2	1 0 0 0 0 0 0 0 0 0
	0 5 1 3	0 1 1 1 1 1 1 1 1 1
	1 0 2 2	0 0 0 0 0 0 0 0 0 1
$V_{REF.B}$	1 0 2 3	0 0 0 0 0 0 0 0 0 0

1 : V_{OH}
0 : V_{OL}

Package Outline



8 bit High-Speed A/D Converter

CX20116/CXA1066K/CXA1056P/
CXA1056K/CXA1016P/CXA1016K

The 8 bit A/Ds for which the flash system has been employed require no externally connected circuits that call for complicated adjustments, and thus make it easy to use. However, because of the high speed conversion they enable, careful design on PCB patterns will be needed to be exercised at relatively high frequencies when operating them.

1. V_{EE}, GND

V_{EE}'s and GND's of the A/Ds have been circuitally separated within the IC into those for the digital circuit and those for the analog circuit. Up to about 50 MHz of clock frequencies the PC board patterns need not be separated, but when employing a higher frequency clock, the separated use of patterns is recommended for noise suppression.

When employing V_{EE}'s separated into digital and analog applications, devices may be destroyed if one end of the V_{EE}'s is turned on with the other left connected to GND via a low impedance for one second or longer.

Both the digital and analog V_{EE} terminals should be bypassed to their respective GNDs with two capacitors each, one 1μF and the other 0.01μF, at a location as close to the terminal as possible. For the 0.01μF, a ceramic chip capacitor is best suited.

2. Timing

The analog input will be sampled at the rising edge of CLK, and digital data is output at the next rising edge of 1CLK cycle later. The delay from the rising edge of CLK to the digital data, Td, is typically 3.5ns, thus it will be possible to latch data with a 10K or 100K series positive edge triggered ECL latch at the same CLK timing and phase as that of the A/Ds.

3. Analog Input (Vin) (See Fig. 1.)

A slew rate of 250V/μs will be required to take full advantage of the wide 40 MHz and above input frequency band of CX20116/CXA1066. Although the analog input capacitance has been reduced to be 35pF or vastly smaller than that of the conventional flash type A/D converters, the A/Ds have to be driven with an input amplifier that has a wide frequency band and

sufficient drive capabilities.

For a simple hook-up, a combination of Harris HA-2540, 5195 or equivalent with an appropriate buffer may be used.

As the input impedance of the devices is capacitive, the driving amplifier occasionally falles into an instable condition and oscillates locally. This instability can be prevented with a resistor added between the output terminal of the amplifier and the input terminal of the A/D. For this application, a resistor from 2 to 10 ohms is recommended.

4. Clock Inputs (CLK, $\overline{CLK}$) (See Fig. 2.)

The clock is usually used to be differentially supplied to two terminals, CLK and $\overline{CLK}$, but it may also be used as a single input CLK by adding on a capacitor of 1,000pF between the $\overline{CLK}$ terminal and GND. In this case, the $\overline{CLK}$ terminal will be held at the threshold potential of the ECL (−1.3V).

5. Logic Control Inputs (MINV, LINV) (See Fig. 3.)

The selection of output codes in response to the analog input will be enabled by the logic states assigned to the MINV and LINV terminals, and will facilitate the application of this converter.

The MINV and LINV terminals will be held at a "LOW" level (= "0") when they are in an open state. Their "High" level may be obtained by a pullup to GND with either a single diode stage or 3.9kΩ.

6. Digital Outputs (D0 to D7) (See Fig. 4.)

Digital outputs require external pull-down resistors. To pull down to V_{EE} = −5.2V, resistors in a range of 500Ω to 1kΩ are recommended.

7. Reference Inputs (V_{RT}, V_{RM}, V_{RS}) (See Fig. 5.)

The V_{RT} ~ V_{RB} inter-terminal voltage corresponds to the A/Ds input dynamic range. While slight offsets are presented on the V_{RT} and V_{RB} terminal sides, adjustments will be possible within the range of V_{RT} = 0V±0.1V and V_{RB} = −2V±0.2V.

The V_{RB} terminal should be bypassed to GND with 1μF and 0.01μF capacitors in parallel.

When the V_{RM} terminal has been bypassed to GND with a 0.01μF capacitor, high frequency characteristics of the converter will be further stabilized. The V_{RM} terminal may also be utilized as a trimming terminal for more accurate linearity compensation.

8. Blank Terminals

Operations with all blank terminals connected to GND are recommended.

9. Others

The converters are very sensitive to noise level because the comparator hysterisis has been designed extremely small to enable high speed operations. The PC board must be designed carefully to reduce ground plane impedance.

Equivalent input and output circuits

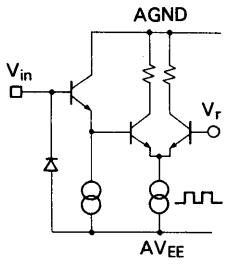


Fig. 1 Analog input

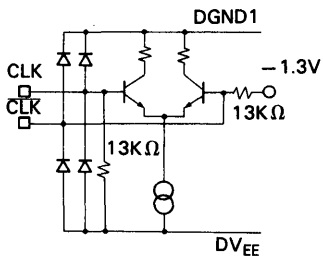


Fig. 2 CLK, $\overline{CLK}$ input

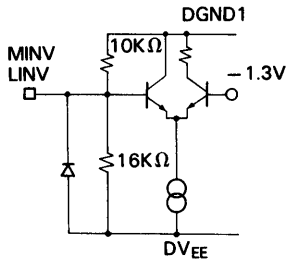


Fig. 3 MINV, LINV input

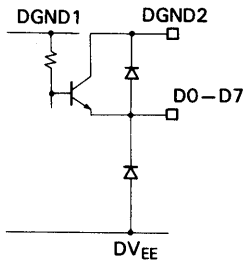


Fig. 4 Digital output

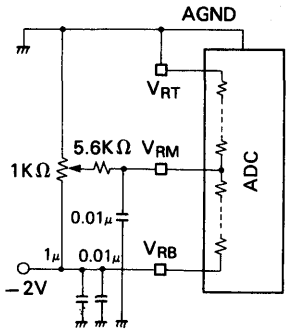


Fig. 5 Linearity compensation

10. Operation (See the block diagram and timing chart.)

1. The reference voltage, which has been obtained by dividing equally the voltage across V_{RT} to V_{RB} into 256 by the reference resistance, is applied to the respective + (positive) input sides of 256 clocked comparators. An analog input is applied to the − (negative) input sides of all the 256 clocked comparators from the V_{IN} terminal.

2. When the state of CLK is in Low, the master (front stage) of the comparator compares the respective reference voltage and the analog input voltage which is ever-changing.
3. When the CLK moves from Low into Hi, each master simultaneously latches the state prior to the CLK transition, and as a result, it provides conditions of "11 ... 1100 .. 0" in sequence from the V_{RT} side to the V_{RB} side.
4. The output of the master is ANDed between the respective adjacent outputs, and "1" stands only when neighboring 2 outputs become "10", and the all other outputs become "0".
5. The result of the AND is latched in the slave latch when CLK moves from Hi into Low. Output of the slave is divided into 4 blocks and each block has 32 clocked comparators, and they are coded into binary codes of 6 bits respectively by the transistor matrix circuit.
6. The 6 bit codes are further coded into 8 bit codes by the transistor matrix circuit after they are respectively latched, and they are then output into the ECL level by the output buffer after being 8 bit latched. The output data is delayed 1 clock from the data sampling point and appears at the output pin.
7. Two polarity inversion inputs such as MINV and LINV are fed externally to the output buffer, and each of them selects output polarity of MSB and LSB's, respectively.

Block Diagram

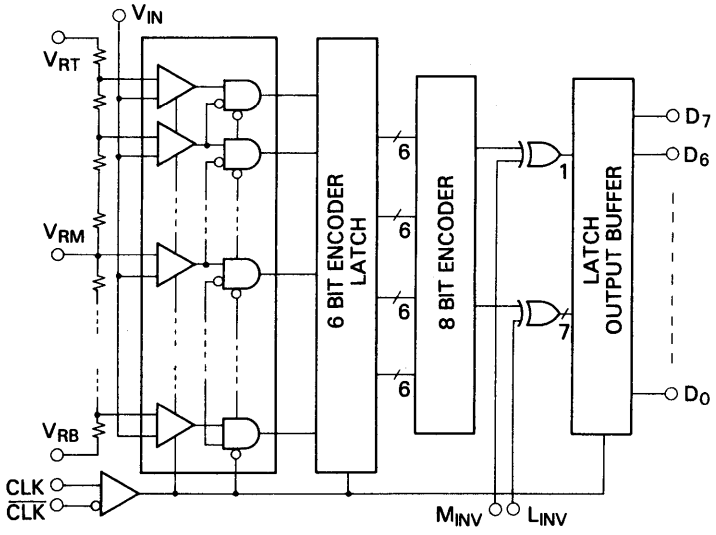


Fig. 6

Timing Chart

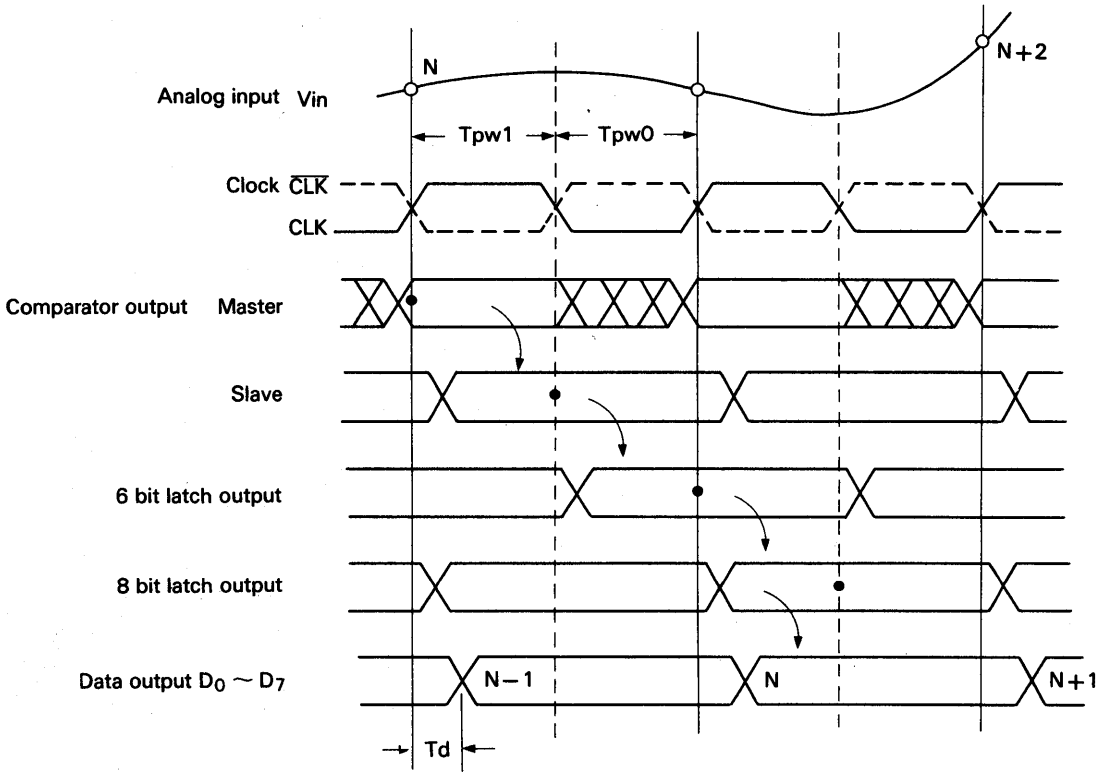


Fig. 7 Dots (●) in the chart demote respective latch timings.

*See page 34, 54 for Tpwl and Tpw0.

11. Dynamic Performance

Figures 8 to 18 show the dynamic performance of the A/D's. The performance is measured with the aid of the digital signal processing in which the parameters are derived directly from the A/D's digital output data. SNR is defined as RMS Signal to RMS Noise.

Fig. 8(a) shows the signal to noise ratio (SNR) of the CX20116/CXA1066K at a sampling rate of 102.4 MHz and 81.92 MHz. The FFT spectrum is shown in Fig. 9 and Fig. 10.

The effective bit is shown in Fig. 8 (b), which is derived from the difference between the measured data and an ideal sine-wave best fitted to the measured data.

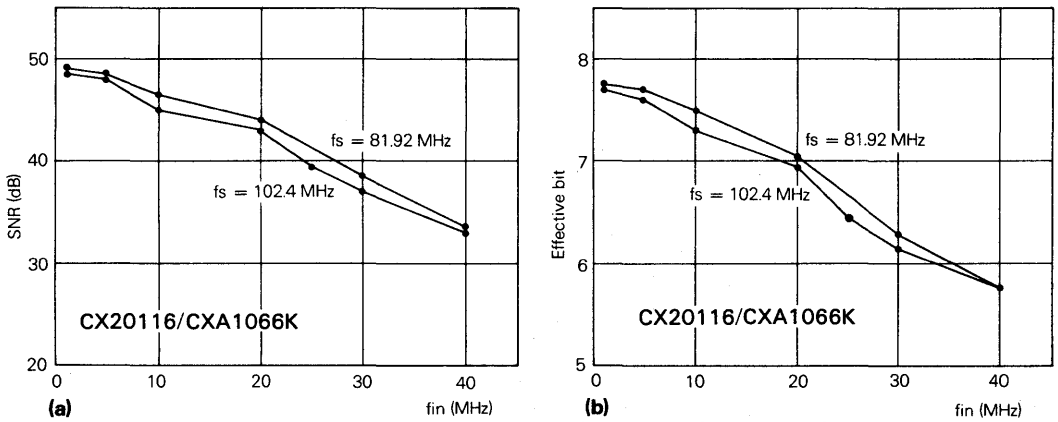


Fig. 8 SNR and effective bit of CX20116/CX20116U/CXA1066K/CXA1066UK

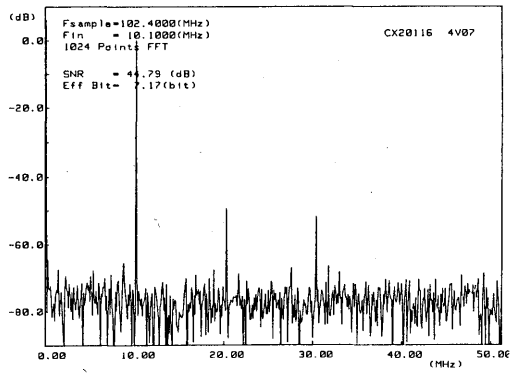


Fig. 9 CX20116
Spectrum with the aid of FFT at 102.4 MHz sampling and 10.1 MHz input.

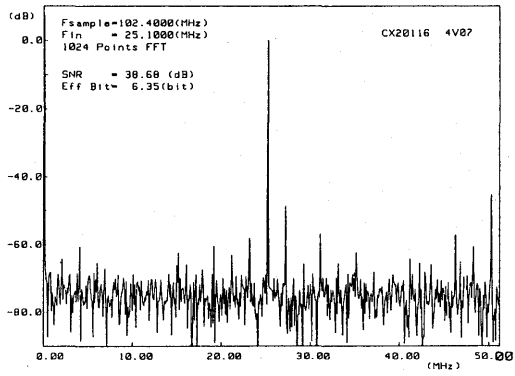


Fig. 10 CX20116
Spectrum with the aid of FFT at 102.4 MHz sampling and 25.1 MHz input.

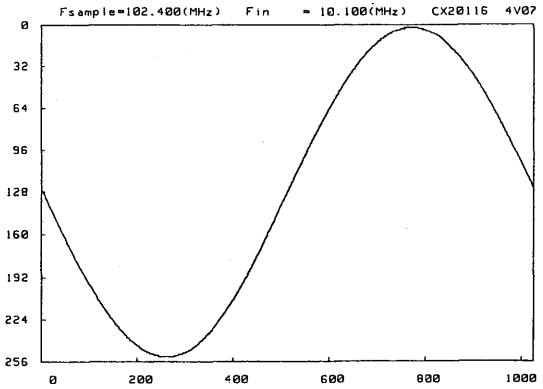


Fig. 11 CX20116
Reconstructed waveform. 102.4 MHz sampling, 10.1 MHz input.

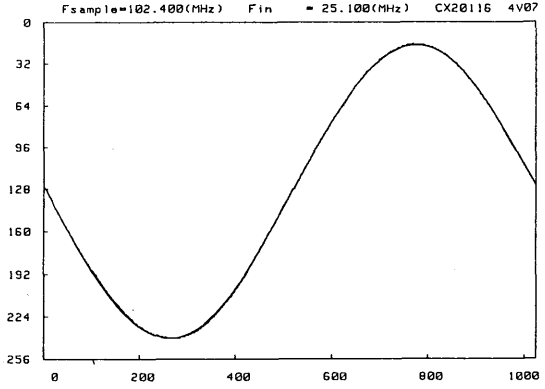


Fig. 12 CX20116
Reconstructed waveform with the best fitted sine wave. 102.4 MHz sampling, 25.1 MHz input.

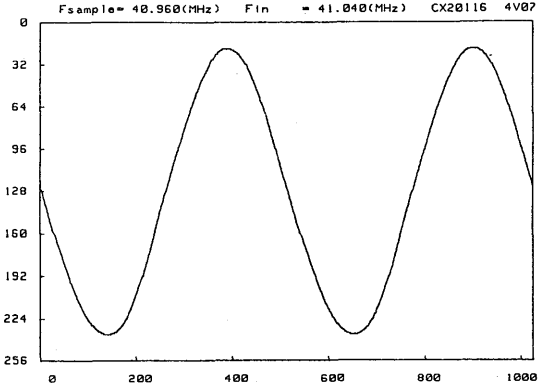


Fig. 13 CX20116
Beat waveform at 41 MHz, $\triangle f = 0.08$ MHz.

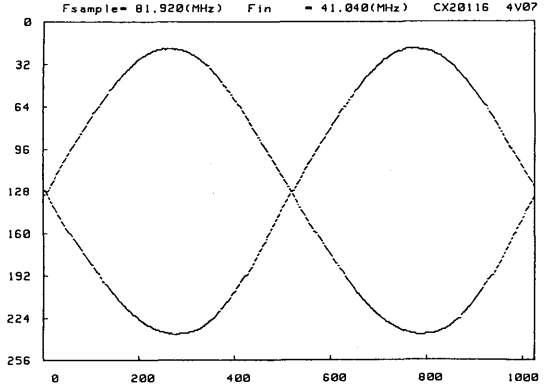


Fig. 14 CX20116
Envelope test waveform at 41.04 MHz input and 81.92 MHz sampling.

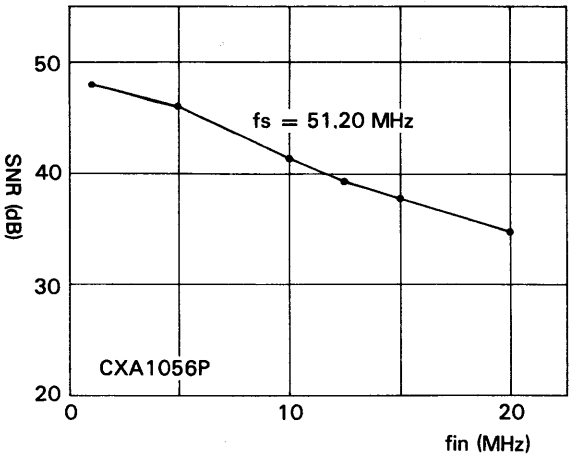


Fig. 15 SNR of CXA1056P/CXA1056K

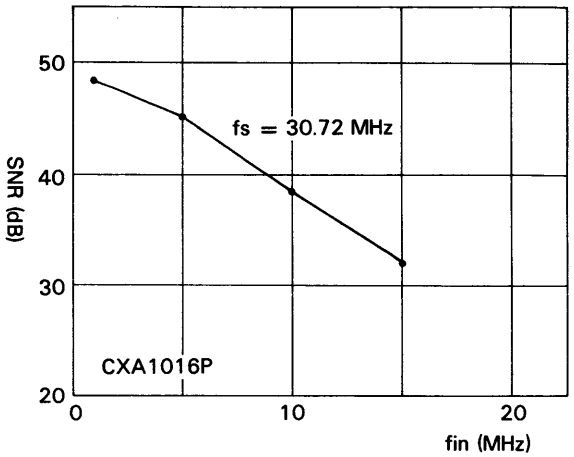


Fig. 16 SNR of CXA1016P/CXA1016K

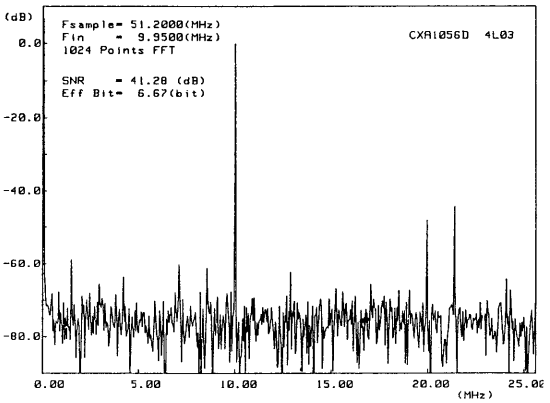


Fig. 17 CXA1056P/CXA1056K
Spectrum with the aid of FFT at 51.2 MHz sampling and 9.95 MHz input.

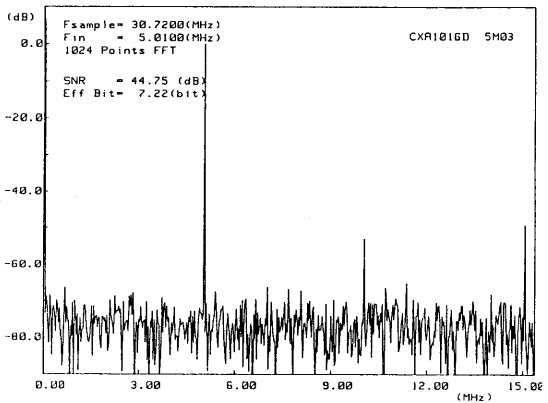


Fig. 18 CXA1016P/CXA1016K
Spectrum with the aid of FFT at 30.72 MHz sampling and 5.01 MHz input.

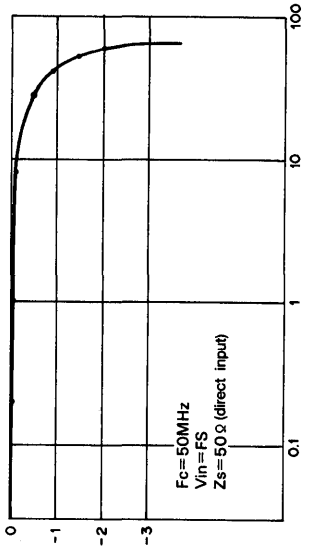


Fig. 20 CXA1056P/CXA1056K
Output level vs. fin

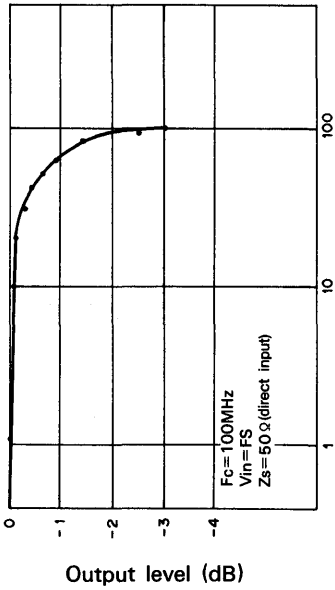


Fig. 19 CX20116/CXA1066K
Output level vs. fin

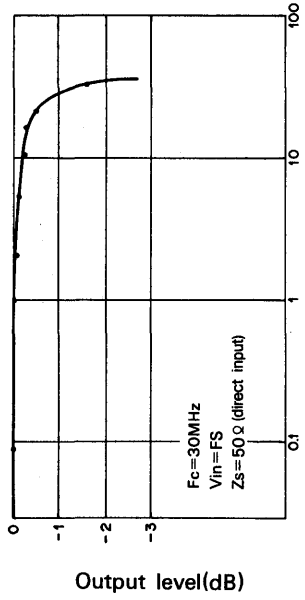


Fig. 21 CXA1016P/CXA1016K
Output level vs. fin

High Speed D/A Converters

4

2. High Speed D/A Converters

(A): Advanced Information
(P): Preliminary

Type	Function	Page
CX20051A	10-bit 30MSPS D/A Converter (ECL I/O)	183
CX20201A-1/-2/-3 CX20202A-1/-2/-3	10/9/8-bit 160MSPS D/A Converter	196
CX20206	8-bit 35MSPS RGB 3-channel D/A Converter (TTL I/O)	210
CXA1106M/P	8-bit 35MSPS High Speed D/A Converter (TTL I/O)	225
CXA1146Q/D CXA1156Q/D	8-bit 160/300MSPS Triple VIDEO DAC (A)	244
CXA1236Q	8-bit 500MSPS Single VIDEO DAC (A)	252
CXA1260Q-Z	8-bit 35MSPS RGB 3-channel D/A Converter (TTL I/O)	264
CXD1170M	6-bit 40MSPS D/A Converter (CMOS) (A)	279
CXD1171M	8-bit 40MSPS D/A Converter (CMOS) (A)	281

SONY

CX20051A

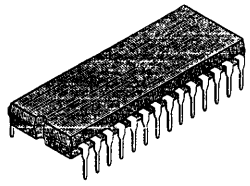
10 bit 30 MSPS D/A Converter

Description

CX20051A is 10 bit, 30 MSPS D/A Converter, designed for a video signal processing. The broadcasting application will require the fairly high resolution for D/A. CX20051A is suitable for the high definition TV application, too.

The external resistor can control the voltage output range of the D/A. The CX20051A requires −5V single power supply, the ECL digital inputs, and the differencial ECL clocks, to operate.

28 pin DIP (Plastic)



Features

- Maximum conversion frequency 30 MSPS
- High resolution 10 bit
- Low power consumption 550 mW
- −5V single power supply
- Clock input and digital input are in ECL level

Structure

Bipolar silicon monolithic IC.

Block Diagram and Pin Connection

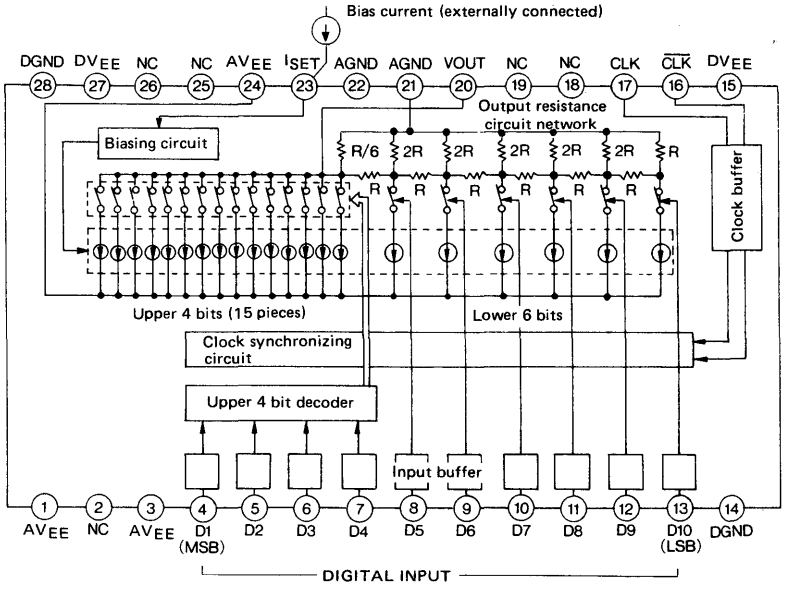


Fig. 1

E89674 – ST

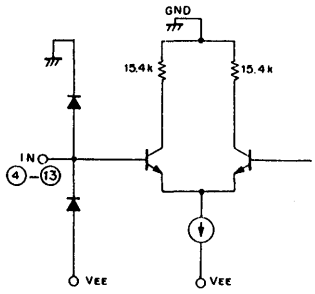
Absolute Maximum Ratings (Ta=25°C)

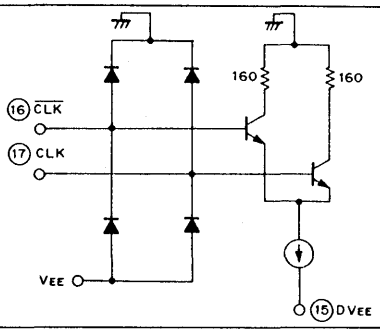
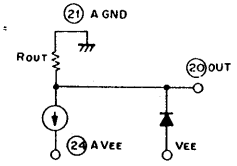
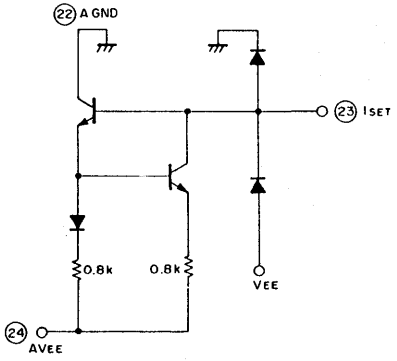
• Supply voltage	V_{EE}	−12	V
• Digital input voltage	V_{IN}	V_{EE} to 0	V
• Operating temperature	Topr	−10 to +70	°C
• Storage temperature	Tstg	−50 to +150	°C
• Allowable power dissipation		1.47	W

Recommended Operating Conditions

• Supply voltage	V_{EE}	−5.0 ± 0.25	V
• Digital input voltage	V_{IH}	−0.89 ± 0.15	V
	V_{IL}	−1.75 ± 0.15	V
• Dynamic range	V_O	−1.5 to −0.5	V
• Bias current	I_{SET}	1.0 ± 0.5	mA

Pin Description

No.	Symbol	Description	Equivalent circuit
1	D V_{EE}	Digital V_{EE} power supply (− 5V)	
2	NC	Non-connection	
3	D V_{EE}	Digital V_{EE} power supply (− 5V)	
4	NSB	10-bit digital input (MSB: Uppermost order, LSB: Lower most order)	
5	BIT2		
6	BIT3		
7	BIT4		
8	BIT5		
9	BIT6		
10	BIT7		
11	BIT8		
12	BIT9		
13	LSB		
14	D GND	Digital GND	
15	D V_{EE}	Digital V_{EE} power supply (−5V)	

No.	Symbol	Description	Equivalent circuit
16	$\overline{CLK}$	Clock bar input	
17	CLK	Clock input	
18	NC	Non-connection	
19	NC		
20	OUT	D/A output	
21	A GND	Analog GND Directly connected to the output resistance circuit network (ROUT)	
22	A GND	Analog GND For analog circuit system other than the output resistance circuit network	
23	ISET	Dynamic range adjusting pin	
24	A VEE	Analog VEE power supply (−5V)	
25	NC	Non-connection	
26	NC		
27	D VEE	Digital VEE power supply (−5V)	
28	D GND	Digital GND	

Electrical Characteristics

(Ta=25°C AGND=DGND=0V, AV_{EE}=DV_{EE}=−5V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Differential linearity	D.L.	*1	−0.8	0	0.8	LSB
Maximum operating clock frequency	f_{MAX}	*2	30			MHz
Differential gain	D.G.	NTSC 40IRE mod. ramp f_{CLK}=14.3 MHz		0.7		%
Differential phase	D.P.			0.2		deg
Circuit current	I_{EE}		88	110	132	mA
Output impedance	R_{OUT}		52	62	72	Ω
Input current	I_{IH}	Measured in the high level input voltage of the individual pins 4 to 13	1	3	10	μA
Input current	I_{IL}	Measured in the low level input voltage of the individual pins 4 to 13	0	20	300	nA

Note) As for the test circuit, see Fig. 2a to 2d.

*1 Input signal is digital ramp with 1 MHz clock.
Glitches are not the subject of the measurement.

*2 The maximum operating clock frequency which shows no bit error. Input signal is digital ramp.
Glitches are not the subject of the measurement.

Electrical Characteristics Test Circuit

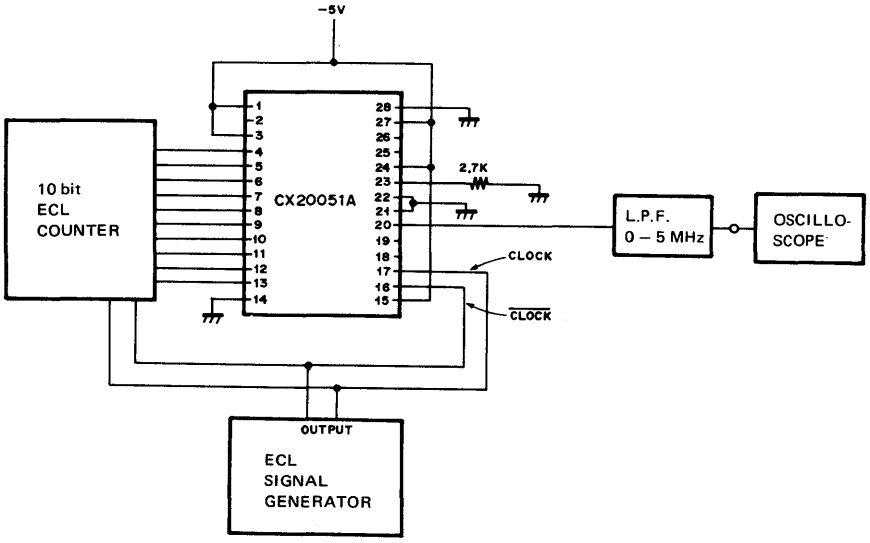


Fig. 2a Block diagram of differential linearity and maximum operating frequency test circuit

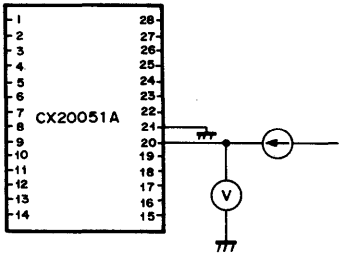


Fig. 2b Block diagram of output impedance test circuit

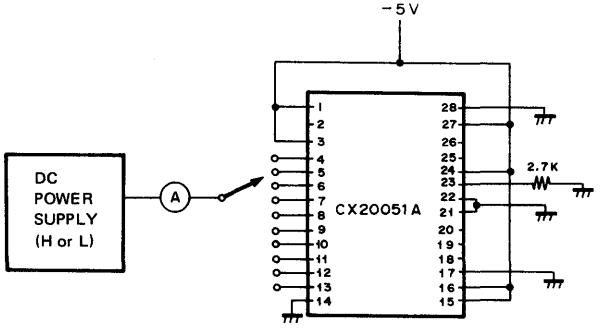


Fig. 2c Block diagram of input current test circuit

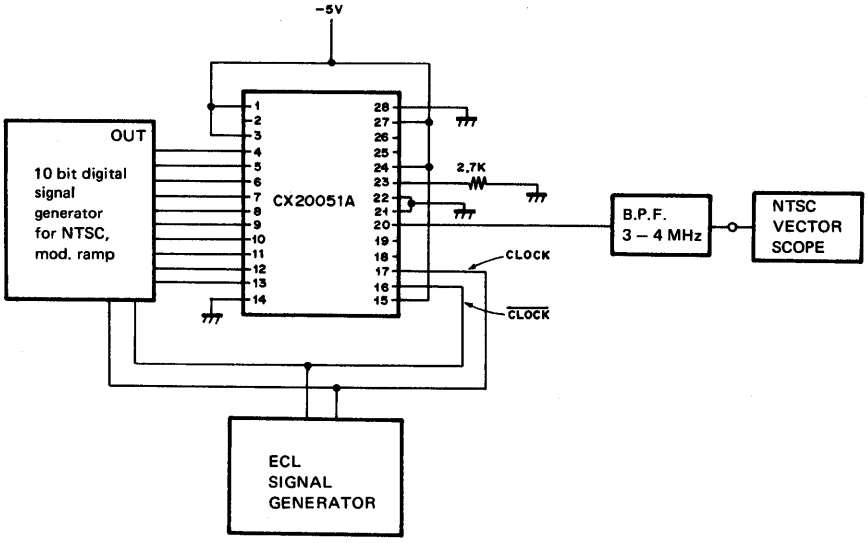


Fig. 2d Block diagram of DG and DP test circuit

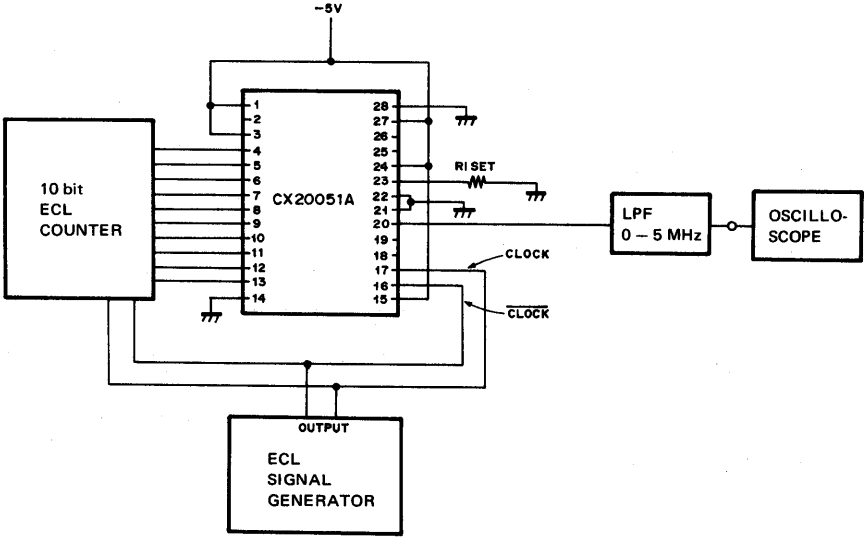


Fig. 2e Block diagram of dynamic range test circuit

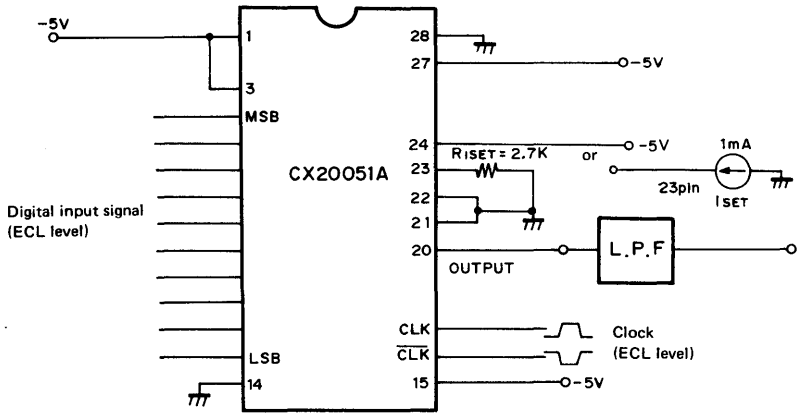


Fig. 3 Typical circuit connection

When changing the dynamic range of the output, change the value of R or the constant current supply value when a constant current supply is inserted in place of R. Both input and clock are in ECL level. Regarding the clock waveform, see the Note on Application.

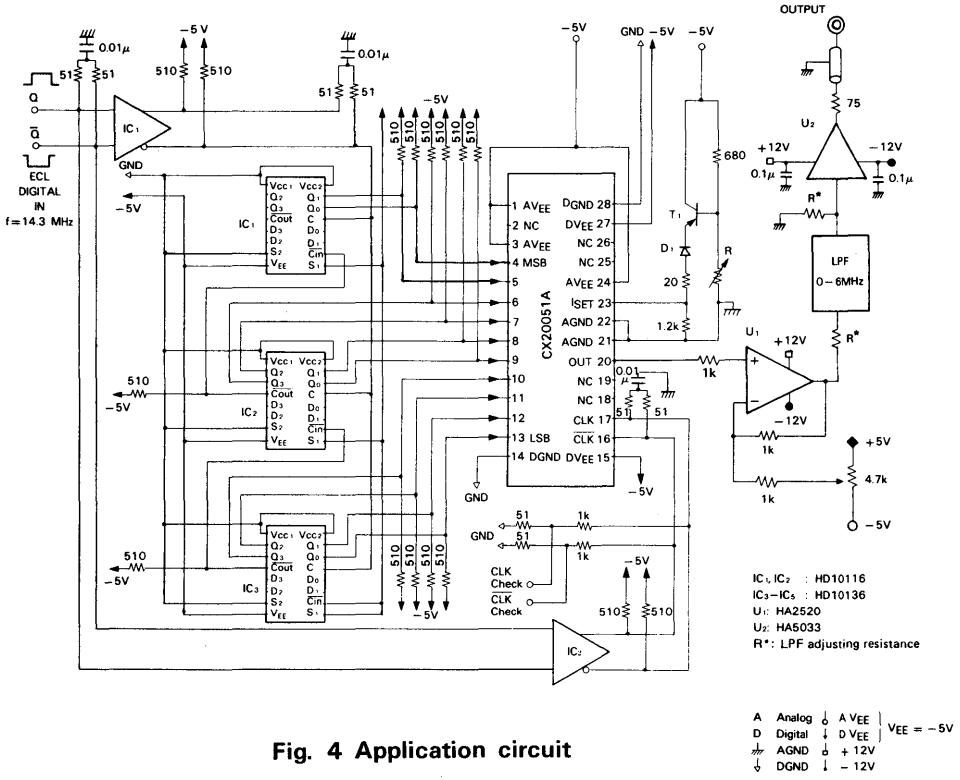


Fig. 4 Application circuit

Note on Application

(1) Applying clocks

(a) To pins 16 and 17, clock signals denoted as $\overline{\text{CLOCK}}$ and CLOCK are to be fed respectively. Both of their levels are ECL compatible levels.

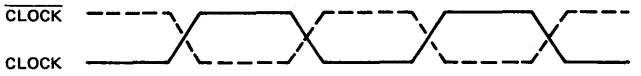


Fig. 5a CLOCK and $\overline{\text{CLOCK}}$ waveforms

(b) Alternatively single-end method is usable to apply clock signal to the device. A clock signal of ECL level is to be fed to one of pin 16 or pin 17, with the other pin fixed to the ECL threshold level.

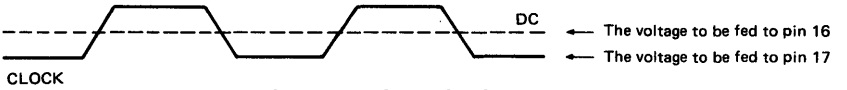
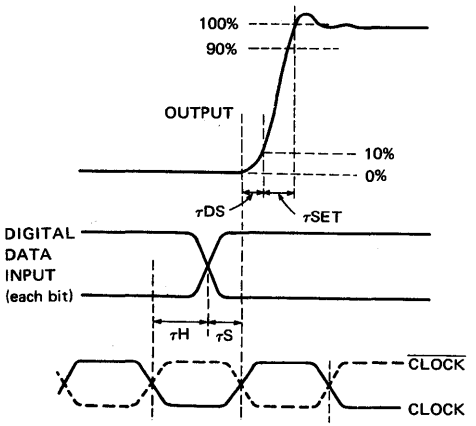


Fig. 5b Single-end method

(2) Timing chart

The timing between the CLOCK signal and 10 bit Digital Data Input signal is shown in the diagram below.



(Recommended operating condition)

$\tau H > 2$ ns

$\tau S > 10$ ns

The typical values of τDS and τSET under the above-mentioned condition are

$\tau DS \approx 7$ ns

$\tau SET \approx 4$ ns

for Z_L (load resistance) > 10 kΩ

Fig. 5c Timing chart

(3) Dynamic range (I_{SET} pin, pin 23)

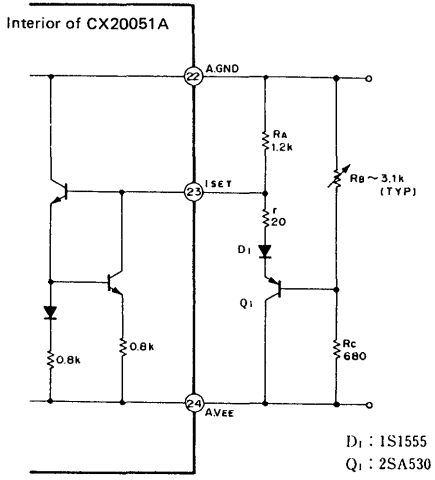
Dynamic range can be determined by connecting an external resistor (R_{ISET}) between the I_{SET} pin (pin 23) and the A GND pin (pin 22), or by applying a current source (I_{SET}) to the I_{SET} pin (pin 23). Typical values to obtain 1 V of dynamic range are 2.7 kΩ and 1 mA, for R_{ISET} and I_{SET} respectively (for a load resistance $Z_L > 10$ kΩ). (See the Dynamic range vs. R_{ISET} on page 193.)

(4) Input coding

STEPS	DIGITAL INPUT	ANALOG OUTPUT	
		CASE ①	CASE ②
0000	MSB1111111111LSB	−0.003V	−0.003V
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
0511	1000000000	−0.4825V	−0.503V
0512	0111111111	−0.4835V	−0.504V
0513	0111111110	−0.4844V	−0.505V
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
1023	0000000000	−0.963V	−1.003V

CASE ① : R_{ISET}=2.7 kΩ
(Output voltage is typical value.)
CASE ② : R_{ISET} is adjusted to obtain 1.000V full scale of analog output voltage.

(5) Temperature fluctuation compensation method of D/A output voltage dynamic range
When the temperature fluctuation of the outout voltage dynamic range poses a problem, a simple temperature compensation can be performed by adding a simple circuit externally.
Connecting diagram of the external circuit for temperature compensation is shown below. In this way, the temperature fluctuation may be limited to within ±150 ppm/°C.



(6) When the analog output level is at full scale 1 Vp-p, the 1LSB becomes approximately 1 mV. In order to obtain the predesignated characteristics, due care should be exercised in the designing of the CX20051A periphery circuit.

[Note on mounting onto the printed board]

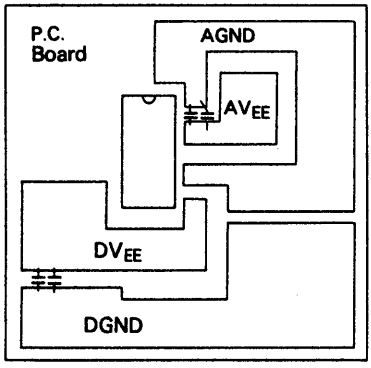
The external connection diagram of CX20051A is basically as shown in Fig. 3. In this regard, take note to the points mentioned below.

(1) AGND and DGND as also AV_{EE} and DV_{EE} are not connected internally. It is also desired to separate the analog block and digital block externally.

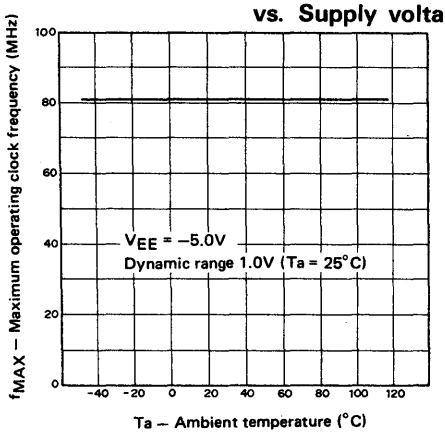
(2) Take as much space as possible of the ground surface on the printed board to reduce parasitic inductance and resistance.

(3) Insert a 47 μF tantalum capacitor and a 1000 pF ceramic capacitor in parallel between the V_{EE} surface and the ground surface most adjacent to it on the printed board and reduce the noise. In addition, it is also desired to insert a capacitor between the V_{EE} surface and the GND surface near the IC. (See Fig. below)

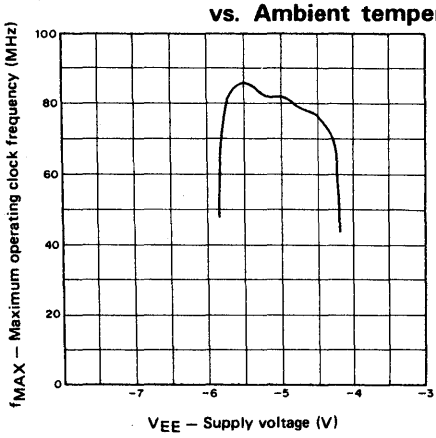
GND and V_{EE} pattern arrangement



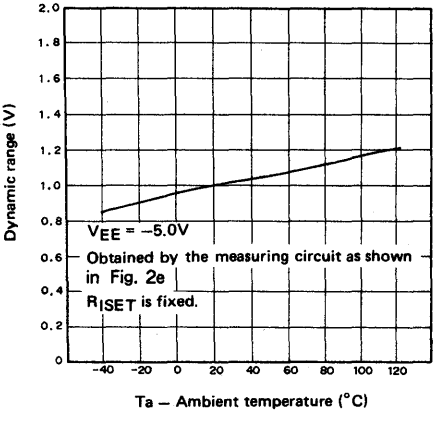
Maximum operating clock frequency vs. Supply voltage



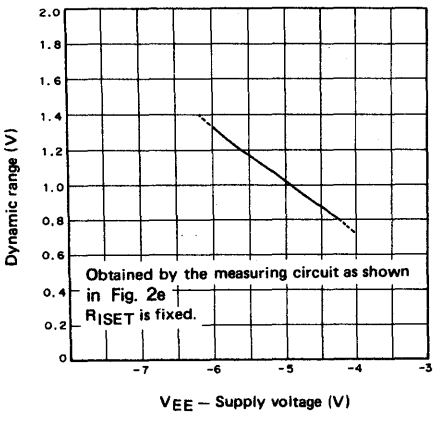
Maximum operating clock frequency vs. Ambient temperature



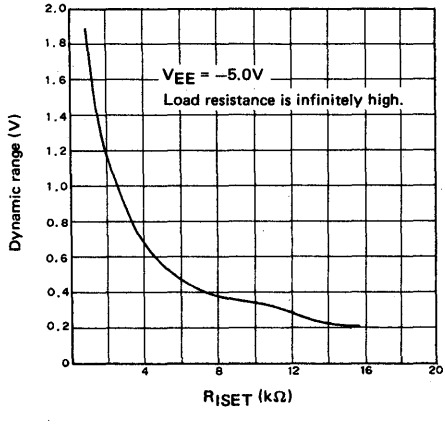
Dynamic range vs. Ambient temperature



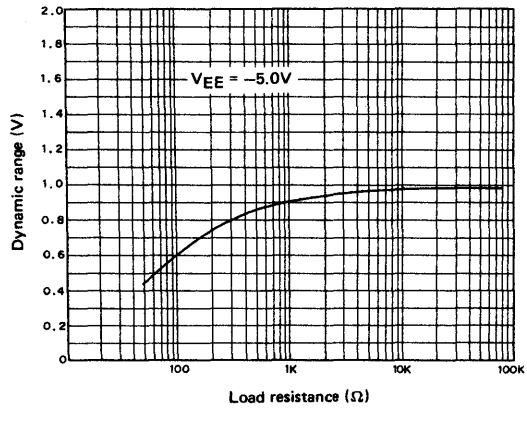
Dynamic range vs. Supply voltage

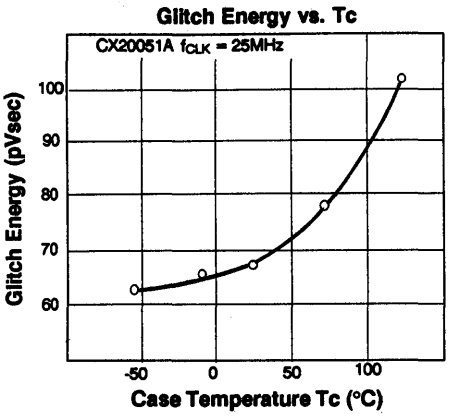


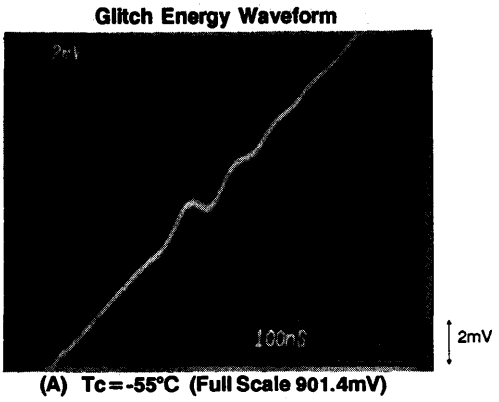
Dynamic range vs. RISET



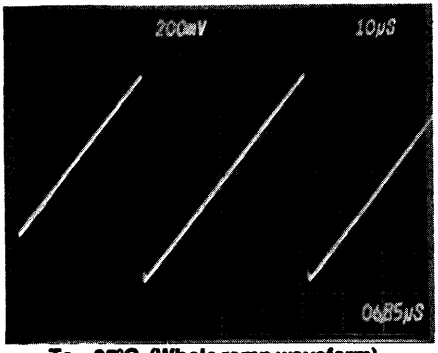
Dynamic range vs. Load resistance



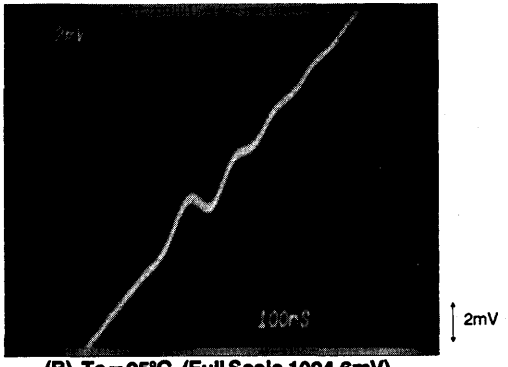




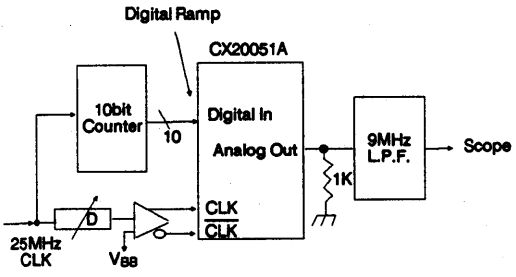
(A) Tc=-55°C (Full Scale 901.4mV)



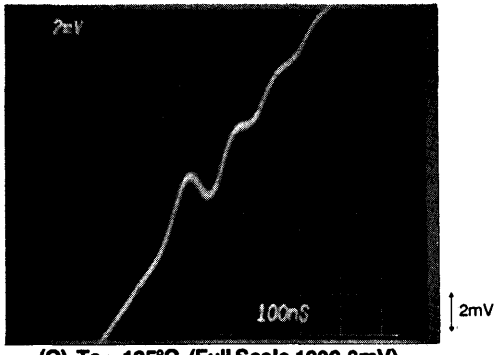
Tc=25°C (Whole ramp waveform)



(B) Tc=25°C (Full Scale 1024.6mV)



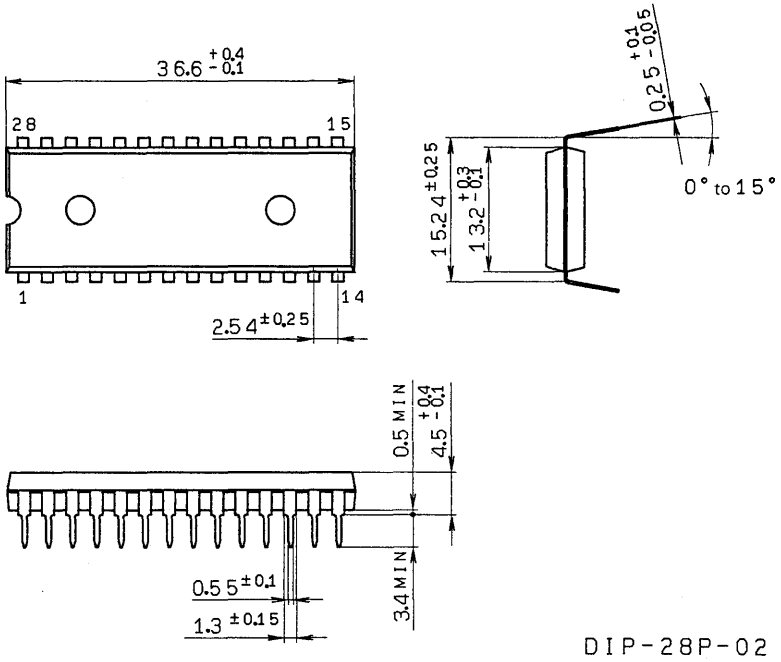
Test Circuit



(C) Tc=125°C (Full Scale 1202.3mV)

Package Outline Unit : mm

CX20051A 28 pin DIP (Plastic) 600mil 4.0g



DIP-28P-02

10/9/8-bit 160MSPS D/A Converter

Descriptions

A series of D/A converters CX20201A/CX20202A convert binary data into an analog signal at rates higher than 160 MHz. The devices include input data registers and have a capability of driving 75 ohms load. Three versions with linearity specifications of 10, 9 or 8 bits are available for each model.

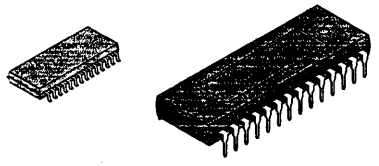
These D/A converter ICs can be used in signal processings which require high speed and high resolution D/A conversions such as high quality displays, high definition video systems, digital measurement instruments and radars.

CX20201A-1/CX20202A-1	10-bit
CX20201A-2/CX20202A-2	9-bit
CX20201A-3/CX20202A-3	8-bit

Features

• High speed	160 MHz
• High accuracy	10 bit (CX20201A-1/ CX20202A-1)

28pin SOP(Plastic) 28pin DIP(Plastic)

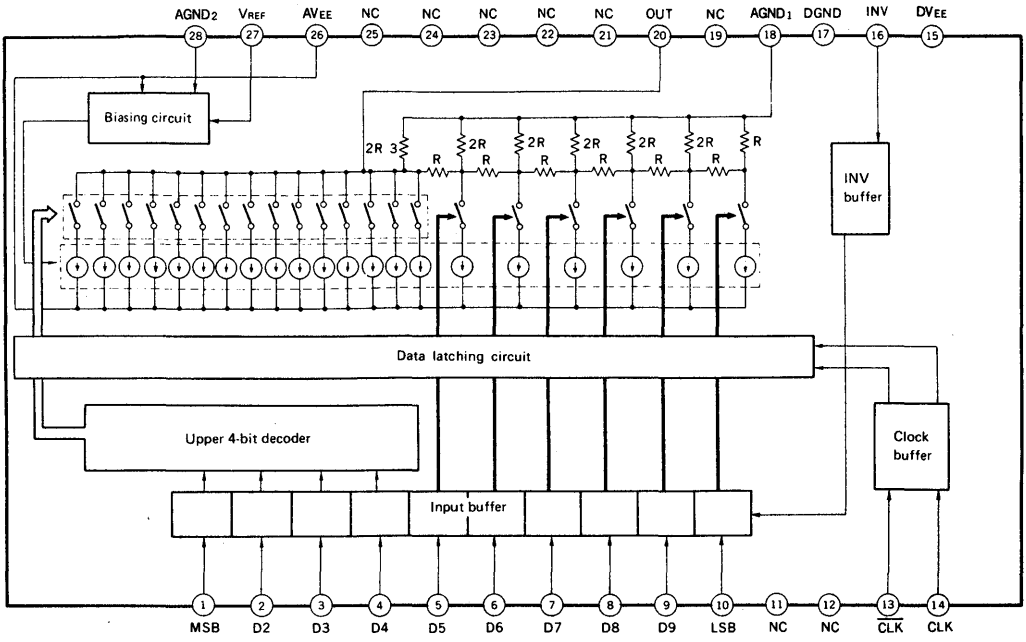


- Low glitch energy 15 pVsec
- Low power consumption 420 mW
- Logic invert input
- 75-Ω direct drive capability
- Analog multiplying function

Structure

Bipolar silicon monolithic IC.

Block Diagram and Pin Configuration (Top. View)



E89667-HP

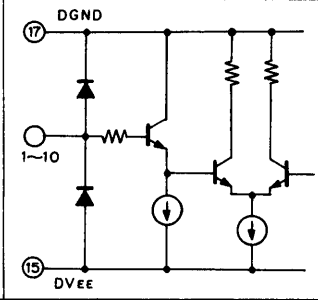
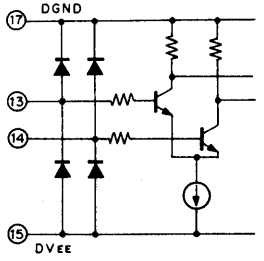
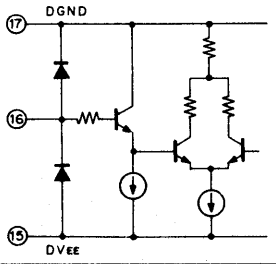
Absolute Maximum Ratings (Ta = 25°C)

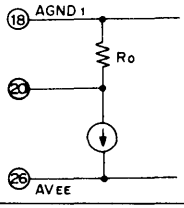
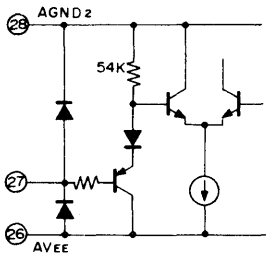
• Supply voltage	V_{EE}	−7	V
• Digital input voltage	V_I	+0.3 to V_{EE}	V
• Reference input voltage	V_{REF}	+0.3 to V_{EE}	
• Analog output current	I_{OUT}	20	mA
• Operating temperature	T_{ope}	−20 to + 75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D		
CX20201A-1/-2/-3		870	mW
CX20202A-1/-2/-3		1430	mW

Recommended Operating Conditions

• Supply voltage	AV_{EE}, DV_{EE}	−4.75	to	−5.45	V
	AV_{EE}-DV_{EE}	−0.05	to	+0.05	V
• Digital input voltage	V_{IH}	−1.0	to	−0.7	V
	V_{IL}	−1.9	to	−1.6	V
• Reference input voltage	V_{REF}	V_{EE}+0.5	to	V_{EE}+1.4	V
• Load resistance	R_L	above 75			Ω
• Output voltage	$V_{O(FS)}$	0.8	to	1.2	V

Pin Description

No.	Symbol	Equivalent circuit	Description
1 2 3 4 5 6 7 8 9 10	MSB D2 D3 D4 D5 D6 D7 D8 D9 LSB		Input pin for digital data. MSB and LSB are corresponded to the most significant bit and least significant bit, respectively. Pins not used should be left open or connected to DVEE.
11 12	NC		Non-connection
13 14	$\overline{\text{CLK}}$ CLK		Pins for clock inputs.
15	DVEE		Power supply pin for digital circuit.
16	INV		Code invert input pin which inverts the relationship between the binary code of digital data and D/A output voltage level.
17	DGND		Grounding pin for digital circuit.
18	AGND 1		Grounding pin directly connected to the R-2R output resistor circuit network in the IC. Grounding for analog circuit system.
19	NC		Non-connection

No.	Symbol	Equivalent circuit	Description
20	OUT		D/A analog output.
21 22 23 24 25	NC		Non-connection
26	AVEE		Power supply pin for analog circuit.
27	VREF		Bias pin which controls D/A output range. The output scale is set by the potential difference between VREF and AVEE.
28	AGND3		Grounding pin for analog circuit system other than the R-2R output resistor circuit network in the IC

Electrical Characteristics (1) Ta = 25°C, AVEE = DVEE = −5.2V, AGND = DGND = 0V, RL = ∞, VO(FS) = −1V

CX20201A-1/CX20202A-1

Item	Symbol	Min.	Typ.	Max.	Unit
Resolution	RES		10		bit
Differential linearity error	ELD	−1/2		+1/2	LSB
Linearity error	ELI	−0.1		+0.1	% of FS
Settling time	ts		5.2		ns

CX20201A-2/CX20202A-2

Item	Symbol	Min.	Typ.	Max.	Unit
Resolution	RES		9		bit
Differential linearity error	ELD	−1/2		+1/2	LSB
Linearity error	ELI	−0.1		+0.1	% of FS
Settling time	ts		4.7		ns

CX20201A-3/CX20202A-3

Item	Symbol	Min.	Typ.	Max.	Unit
Resolution	RES		8		bit
Differential linearity error	ELD	−1/2		+1/2	LSB
Linearity error	ELI	−0.2		+0.2	% of FS
Settling time	ts		4.3		ns

Electrical Characteristics (2) Ta = 25°C, AV_{EE} = DV_{EE} = −5.2V, AGND = DGND = 0V, R_L = ∞, $V_{O(FS)}$ = −1V

Item		Symbol	Measuring condition*1	Min.	Typ.	Max.	Unit
Power supply current	CX20201A	I_{EE}		−60	−75	−90	mA
	CX20202A			−65	−82	−100	
Data input current (for upper 4 bits)		$I_{IH(U)}$	V_{IH} = −0.89V	0.1	1.5	6.0	μA
		$I_{IL(U)}$	V_{IL} = −1.75V	0.1	1.5	6.0	μA
Data input current (for lower 6 bits)		$I_{IH(L)}$	V_{IH} = −0.89V	0.1	0.75	3.0	μA
		$I_{IL(L)}$	V_{IL} = −1.75V	0	0.75	3.0	μA
Clock input current		I_{CLKH}	V_{IH} = −0.89V	2	23	70	μA
Invert input current		I_{INVH}	V_{IH} = −0.89V	0.1	1.5	6.0	μA
Reference input current		I_{REF}	V_{REF} = −4.38V	−3	−0.4	−0.1	μA
Output resistance		R_O	I_O = −1mA	52	65	78	Ω
Maximum conversion rate		fc	R_L = 75Ω	160			MSPS
Output voltage full-scale deviation		$V_{O(FS)}$	V_{REF}=−4.38V	0.90	1.00	1.10	V

*1 See Figs. 3 to 5.

Data for Typical Application

Ta = 25°C, AVEE = DVEE = −5.2V, AGND = DGND = 0V, RL = ∞, VO(FS) = −1V

Item	Symbol	Measuring condition	Min.	Typ.	Max.	Unit
Output voltage zero offset	EZS	RL ≧ 10kΩ	0	−7	−21	mV
		RL = 75Ω	0	−7	−21	
Output voltage full-scale temperature coefficient	TC(FS)	RL ≧ 10kΩ	0	−140	−280	ppm/°C
		RL = 75Ω	0	−580	−1200	
Output voltage zero offset temperature coefficient	TC(ZS)	RL ≧ 10kΩ	6	16	22	μV/°C
Glitch energy	GE	Digital ramp		15		pVsec
Rise time	tr	RL = 75Ω		1.5		ns
Fall time	tf			1.5		ns
Propagation delay	td			3.8		ns
Band width for multiplying	BWMUL	RL = 75Ω, −3dB	10	14		MHz
Set-up time	tsu				5.0	ns
Hold time	thd				1.0	ns

Timing Chart

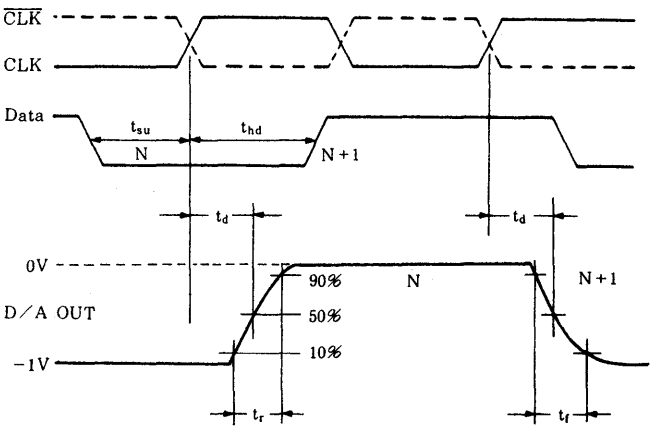


Fig. 1

Input Coding Table

Input code	Output code (V)	
	INV = 1	INV = 0
0 0 0 ····· 0 0	0	−1
0 1 1 ····· 1 1	−0.5	−0.5
1 0 0 ····· 0 0		
1 1 1 ····· 1 1	−1	0

Measuring Conditions for Current Consumption, Input Current and Output Resistance (See Fig. 2.)

Test item	Symbol	Switch condition																					Test point
		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S20	S21	
Current consumption	I_{EE}	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	a	b	b	b	b	b	I1
Data input current for upper 4 bits (H level)	$I_{IH(U)}$	a	b	b	b	b	b	b	b	b	b	a	b	b	b	b	b	b	b	b	b	b	I2
		b	a	b	b																		
		b	b	a	b																		
		b	b	b	a																		
Data input current for lower 4 bits (L level)	$I_{IL(U)}$	a	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	I2
		b	a	b	b																		
		b	b	a	b																		
		b	b	b	a																		
Data input current for upper 6 bits (H level)	$I_{IH(L)}$	b	b	b	b	a	b	b	b	b	b	a	b	b	b	b	b	b	b	b	b	b	I2
						b	a	b	b	b	b												
						b	b	a	b	b	b												
						b	b	b	a	b	b												
						b	b	b	b	a	b												
						b	b	b	b	b	a												
Data input current for lower 6 bits (L level)	$I_{IL(L)}$	b	b	b	b	a	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	I2
						b	a	b	b	b	b												
						b	b	a	b	b	b												
						b	b	b	a	b	b												
						b	b	b	b	a	b												
						b	b	b	b	b	a												
Clock input current (H level)	I_{CLKH}	b	b	b	b	b	b	b	b	b	b	b	a	b	b	a	b	b	b	b	b	b	I3
Clock-bar input current (H level)	$I_{\overline{CLK}H}$	b	b	b	b	b	b	b	b	b	b	b	b	a	a	b	b	b	b	b	b	b	I4
Invert input current (H level)	I_{INVH}	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	a	a	b	b	b	I5
Referecnce input current	I_{REF}	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	a	I6
Output resistance	R_O	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	a	a	b	V1

Electrical Characteristics Test Circuit

Test Circuit for Current Consumption, Input Current and Output Resistance

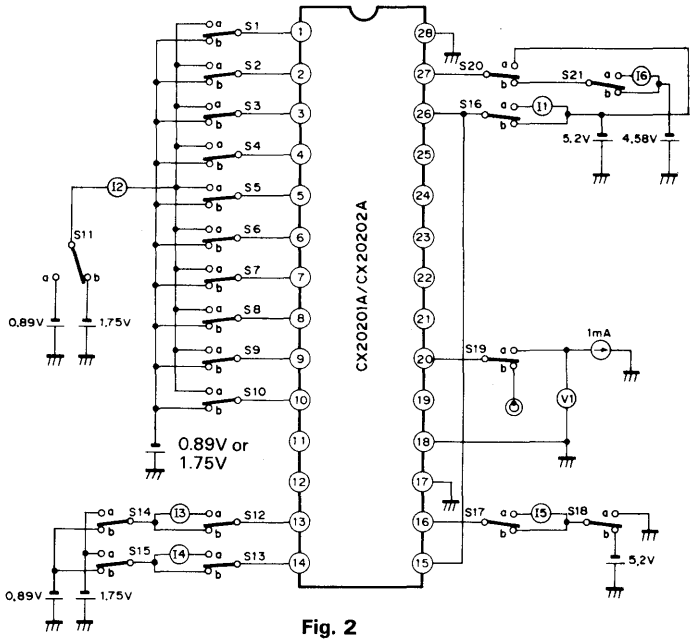
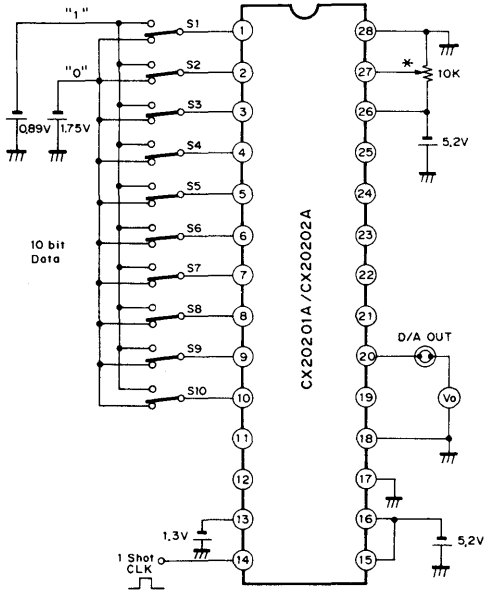


Fig. 2

Test Circuit for Differential Linearity Error and Linearity Error



* Adjust so that the full scale of DC voltage at Pin 20 becomes 1.023V, that is, to satisfy $V_0 - V_{1023} = 1.023V$.

Fig. 3

Linearity errors are measured as follows.

S1	S2	S3	·····	S9	S10	D/A out
0	0	0	·····	0	0	V_0
0	0	0	·····	0	1	V_1
0	0	0	·····	1	0	V_2
			⋮			⋮
1	1	1	·····	1	1	V_{1023}

Linearity error	Differential linearity error
V_0	
V_1	$V_1 - V_0$
V_2	$V_2 - V_1$
V_4	$V_4 - V_3$
V_8	$V_8 - V_7$
V_{16}	$V_{16} - V_{15}$
V_{32}	$V_{32} - V_{31}$
V_{64}	$V_{64} - V_{63}$
V_{128}	$V_{128} - V_{127}$
V_{192}	$V_{192} - V_{191}$
⋮	⋮
V_{960}	$V_{960} - V_{959}$
V_{1023}	

Errors at individual measurement points are calculated according to the following definition.

$(V_{1023} - V_0)/1023 = V_{0(FS)}/1023 \equiv 1$ LSB.

Test circuits for { Maximum conversion rate, Rise time, Fall time, Propagation delay, Set-up time, Hold time, Settling time

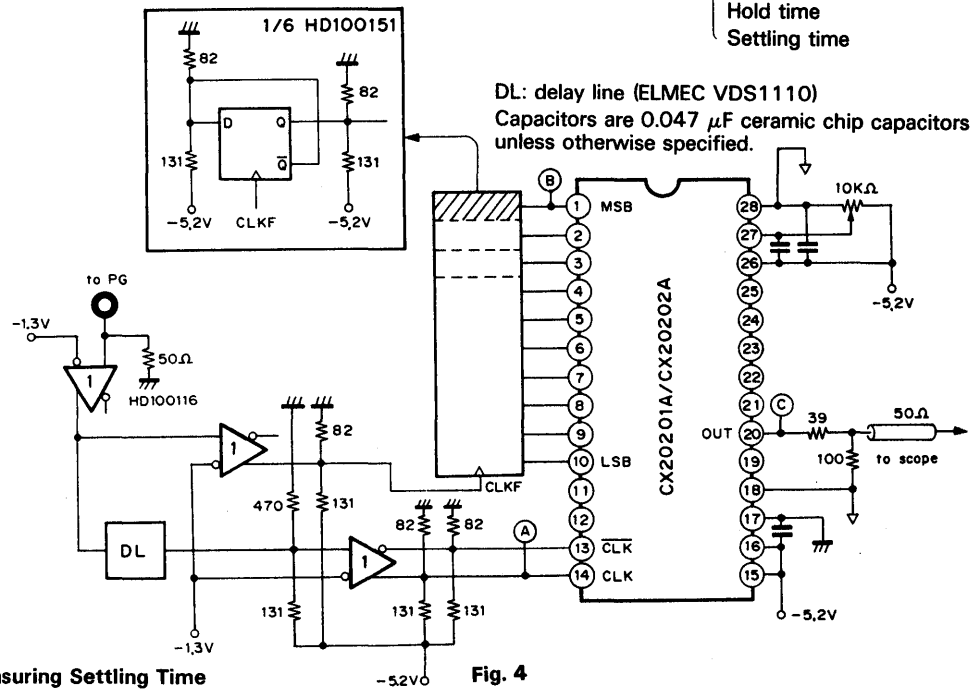


Fig. 4

Measuring Settling Time

Settling time is measured as follows. The relationship between V and $V_{O(FS)}$ as shown in the D/A output waveform in Fig. 5 is expressed as

$V = V_{O(FS)} (1 - e^{-t/\tau})$.

The settling time for respective accuracy of 10 , 9 and 8-bit is specified as

$V = 0.9995\ V_{O(FS)}$

$V = 0.999\ V_{O(FS)}$

$V = 0.998\ V_{O(FS)}$

which results in the following:

$t_s = 7.60\tau$ for 10-bit,

$t_s = 6.93\tau$ for 9-bit, and

$t_s = 6.24\tau$ for 8-bit

Rise time (t_r) and fall time (t_f) are defined as the time interval to slew from 10% to 90% of full scale voltage ($V_{O(FS)}$):

$V = 0.1\ V_{O(FS)}$

$V = 0.9\ V_{O(FS)}$

and calculated as $t_r = t_f = 2.20\ \tau$.

The settling time is obtained by combining these expressions:

$t_s = 3.45 t_r$ for 10-bit,

$t_s = 3.15 t_r$ for 9-bit, and

$t_s = 2.84 t_r$ for 8-bit

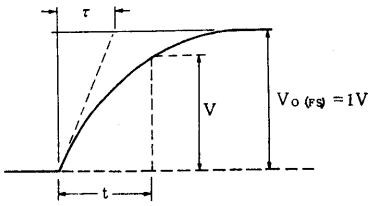


Fig. 5

Test Circuit for Multiplying Band Width

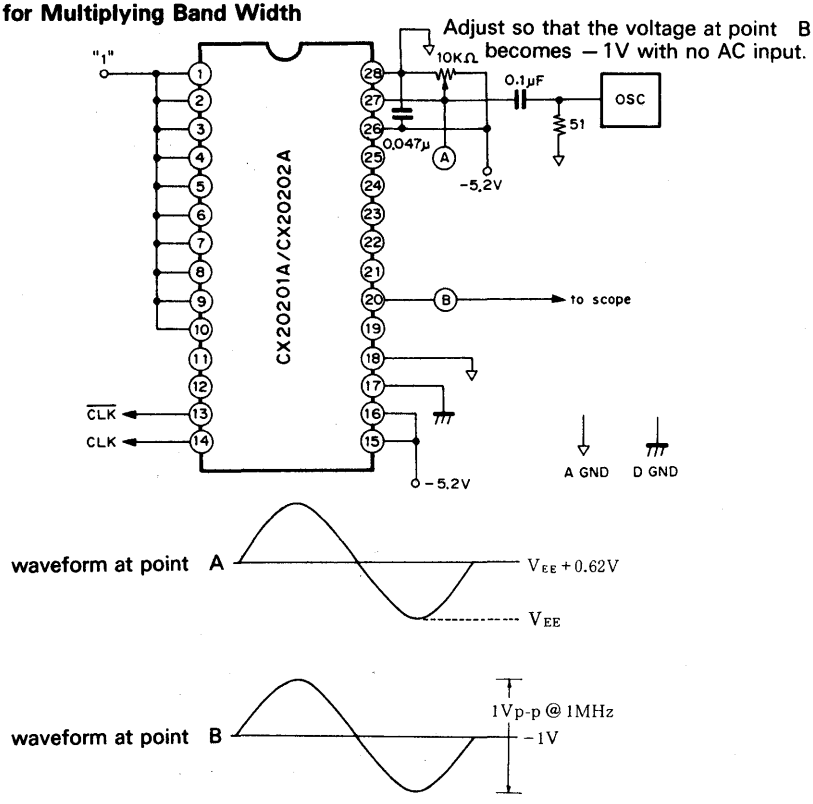


Fig. 6

Typical Application Circuit

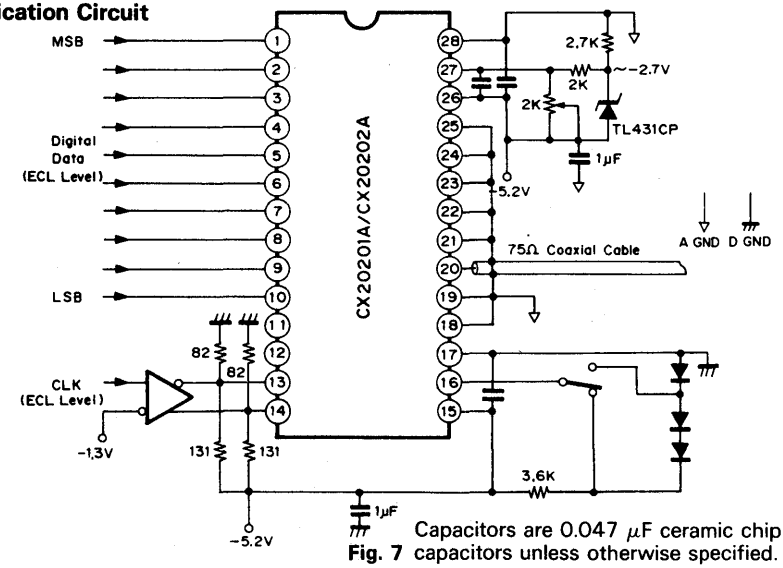


Fig. 7 Capacitors are 0.047 μF ceramic chip capacitors unless otherwise specified.

Notes on Applications

(1) Setting of full-scale output voltage

The full-scale output voltage ($V_{O(FS)}$) is set by the pin 27 (V_{REF}). $V_{O(FS)}$ varies in proportion to the voltage difference between pin 27 and pin 26 (AV_{EE}) as shown in Fig. 9.

$V_{O(FS)}$ can be set by simply dividing the supply voltage using resistors as shown in Fig. 8, but in this simple set up the voltage deviation of the supply voltage result in a deviation of $V_{O(FS)}$. This influence can be avoided by using a stabilization circuit as shown in Fig. 7 to allow stable full-scale output.

Pin 27 (V_{REF}) should be stabilized against high-frequency noise by sufficient by passing using a capacitor with low lead inductance such as ceramic chip capacitors. The stabilization capacitor should be inserted between pin 27 (V_{REF}) and pin 26 (AV_{EE}) as $V_{O(FS)}$ is direct proportion to the voltage across these two terminals.

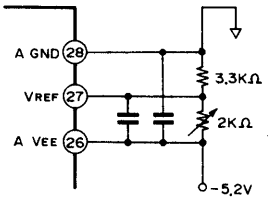


Fig. 8

(2) Noise reduction

An external digital noise should be minimized because the system handles small analog voltage (1 LSB corresponds 1 mV of analog output voltage for 10 bit resolution). Refer to the following notes to minimize the system noise contamination.

- Ground plane and V_{EE} plane on a printed circuit board should be made as wide as possible to reduce parasitic inductance and resistance.
- The patterns AGND and DGND should be separated on the printed circuit board. AV_{EE} and DV_{EE} should be separated too. The connections between analog system and digital system are to be made at the I/O ports of the printed circuit board.
- AV_{EE} and DV_{EE} should be bypassed to respective GND by using a tantalum capacitor of 1 μF and a ceramic chip capacitor of 47μF positioned as close as to terminals of the IC.
- Pins not in use are to be connected to the ground plane.

(3) Load resistance and temperature coefficient

Temperature coefficient of the full-scale output voltage and zero offset voltage depend on the load resistance (value and type). Generally, the larger the load resistance the better the temperature coefficient value. Temperature characteristics at $R_L \geqq 10\ k\Omega$ and $R_L = 75\ \Omega$ are shown in Fig. 10.

(4) Input data and internal latching circuit

CX20201A/CX20202A incorporates a latching circuit as shown in the block diagram. This latching circuit has a two-stage configuration (master-slave type) and fetches input data only at the rising edge of the clock; the output is not affected by the changes in input data at any other timings. This mechanism allows stable operation against any changes in input data at any timings, except for the set-up time immediately before and the hold time immediately after the clock change from L to H.

(5) Driving input data and clock

CX20201A/CX20202A are designed to be operated at very high speed. It is, therefore, necessary to drive it with a high-speed ICs such as an ECL100K for full performance. Also the output port of the data and clock drivers should be terminated with 50-Ω systems. See Figs. 4 and 7.

$V_{O(FS)}$ Ratio vs. (V_{REF}-V_{EE})

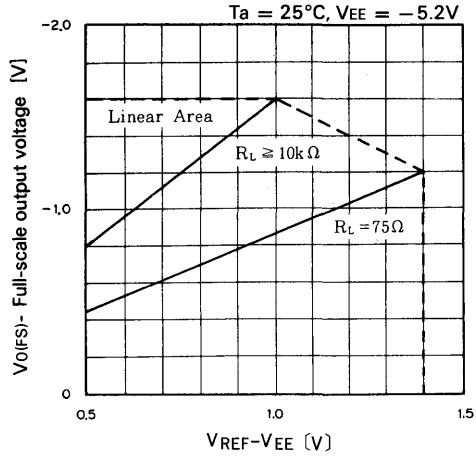


Fig. 9

Full-scale Output Voltage vs. Ambient Temperature

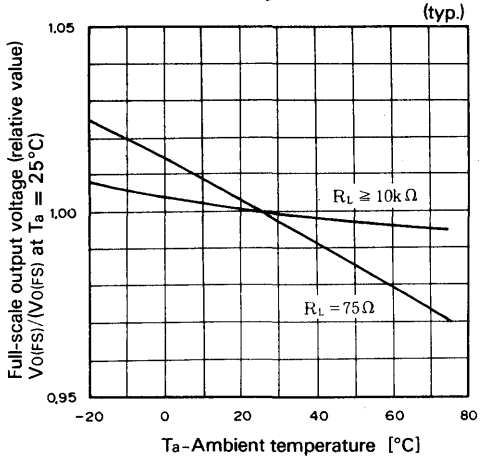


Fig. 10

Outbut Characteristics vs. Multiplying Input Signal Frequency

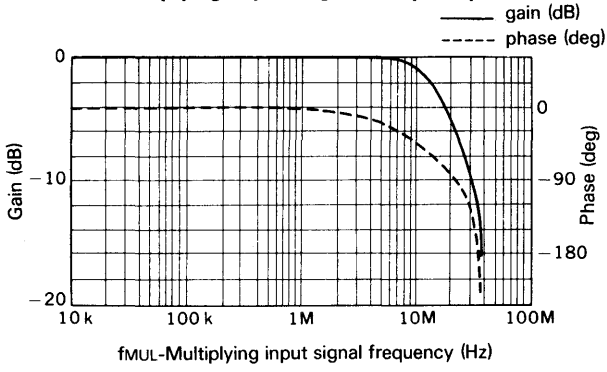


Fig. 11

Glitch Energy vs. Case Temperature (Full Scale−1023mV)

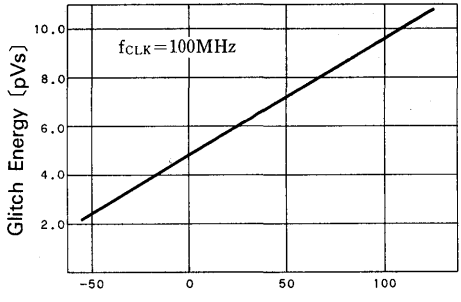
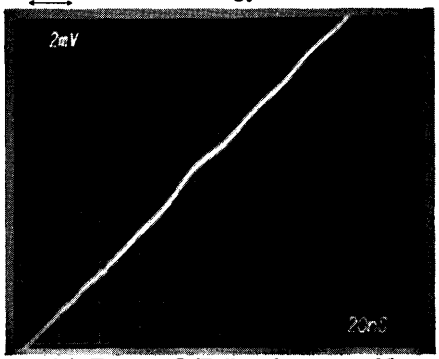


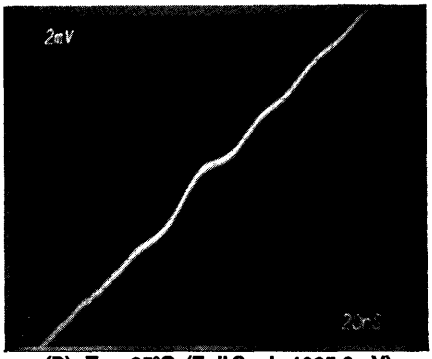
Fig. 12

20ns **Glitch Energy Waveform**



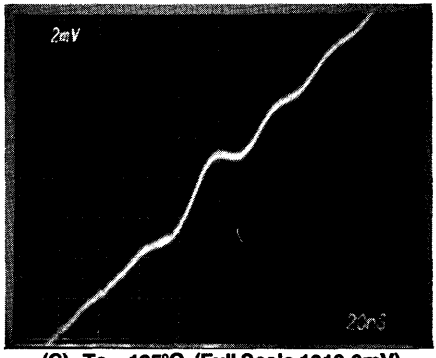
2mV

(A) Tc=-55°C (Full scale 1030.1mV)



2mV

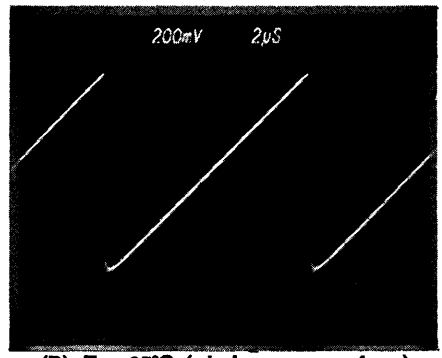
(B) Tc=25°C (Full Scale 1025.0mV)



2mV

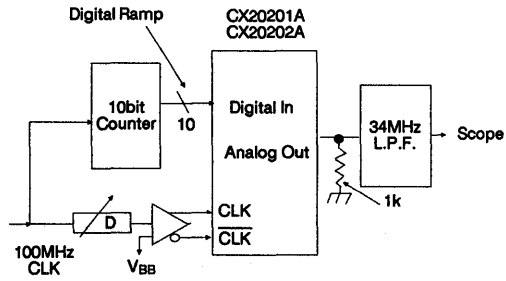
(C) Tc=125°C (Full Scale 1019.0mV)

Ramp output waveform



200mV

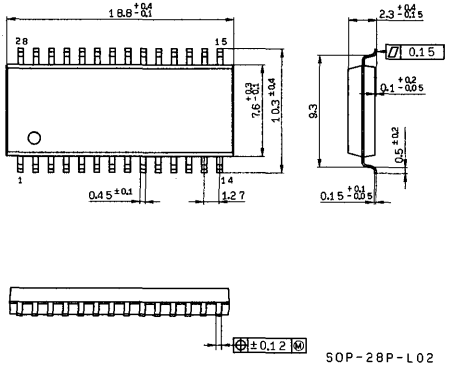
(D) Tc=25°C (whole ramp waveform)



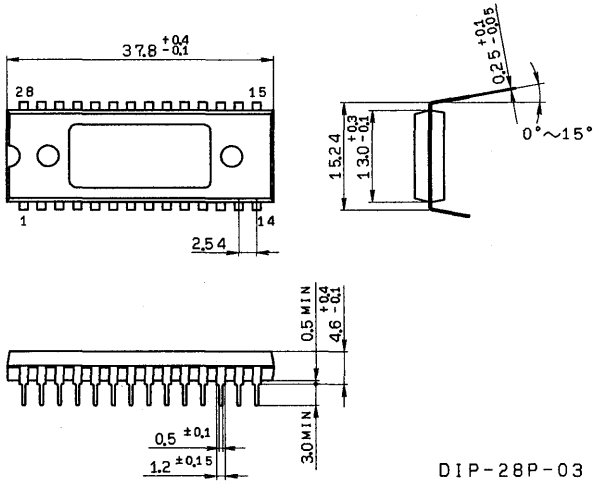
Test Circuit

Package Outline Unit : mm

CX20201A 28pin SOP(Plastic) 375mil 0.6g



CX20202A 28pin DIP(Plastic) 600mil 4.2g



SONY®

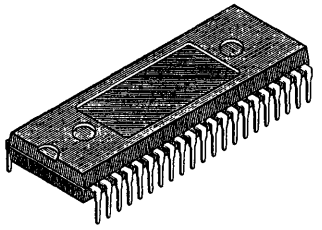
CX20206

8 bit 35 MSPS RGB 3-Channel D/A Converter

Description

CX20206 is an 8 bit high-speed D/A converter for video band use. It has an output/input equivalent to 3 channels of R, G and B. It is suitable for use of digital TV, graphic display, etc.

42 pin SDIP (Plastic)



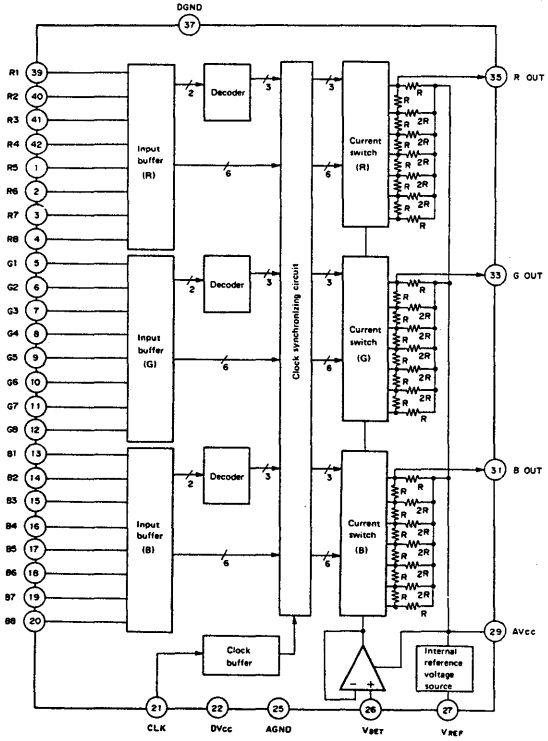
Features

- Resolution: 8 bits
- Maximum conversion speed: 35MSPS
- RGB 3-channel input/output
- Differential linearity error: ±1/2LSB
- Digital input voltage: TTL level
- Output voltage full-scale: 1 Vp-p (typ)
- Low power consumption: 360 mW (typ)
- +5V single power supply

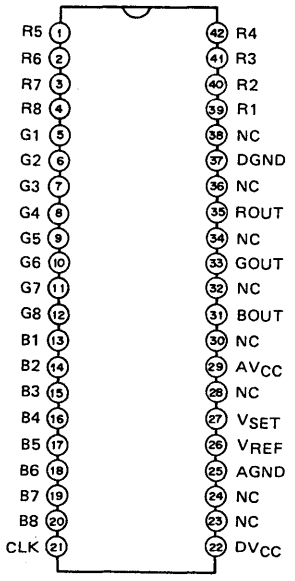
Structure

Bipolar silicon monolithic IC

Block Diagram



Pin Configuration (Top View)



E89638-ST

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	0 to 7	V
• Input voltage (digital)	V_I	−0.3 to V_{CC}	V
	V_{CLK}	−0.3 to V_{CC}	V
• Input voltage (V_{SET} pin)	V_{SET}	−0.3 to V_{CC}	V
• Output voltage (analog)	V_{OUT}	V_{CC}−2.1 to V_{CC}	V
• Output current (analog)	I_{OUT}	−3 to +10	mA
(V_{REF} pin)	I_{REF}	−5 to 0	mA
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	1.5	W

Recommended Operating Conditions

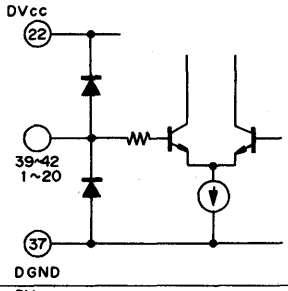
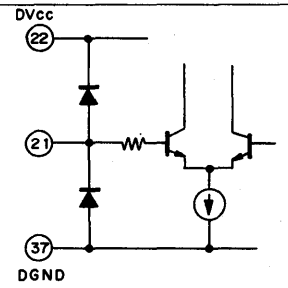
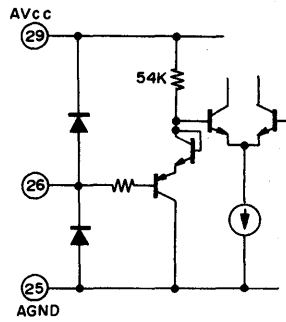
• Supply voltage	AV_{CC}, DV_{CC}	4.5 to 5.5	V
	AV_{CC}–DV_{CC}	−0.2 to +0.2	V
	AGND–DGND	−0.05 to +0.05	V
• Digital input voltage H level	V_{IH}, V_{CLKH}	2.0 to DV_{CC}	V
L level	V_{IL}, V_{CLKL}	DGND to 0.8	V
• V_{SET} input voltage	V_{SET}	0.7 to 0.9	V
• V_{REF} pin current	I_{REF}	−3 to −0.4	mA
• Clock pulse width	T_{pw1}	15	ns
	T_{pw0}	10	ns

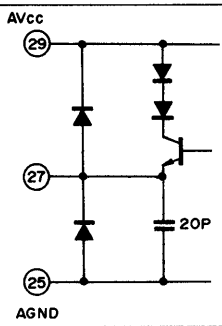
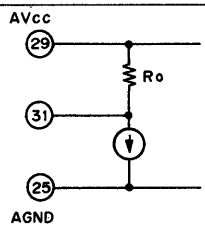
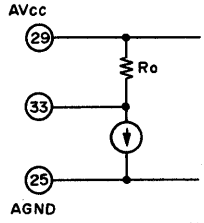
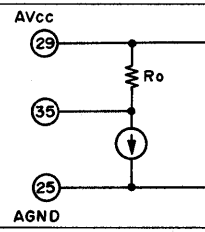
Input corresponding table

Input code	Output voltage
MSB LSB	
1 1 1 1 1 1 1 1	V_{CC}+Voffset
.	.
.	.
.	.
1 0 0 0 0 0 0 0	V_{CC}+Voffset−0.5V
.	.
.	.
.	.
0 0 0 0 0 0 0 0	V_{CC}+Voffset−1.0V

In case the output voltage full-scale is 1.00V. (1 LSB=3.92 mV)

Pin Description

No.	Symbol	Equivalent circuit	Description
39 to 42 1 to 20	R1 to R8 G1 to G8 B1 to B8		Digital input pin. From pins 39 to 42 and from 1 to 4 are for RED. R1 is MSB and R8 is LSB. From pins 5 to 12 are for GREEN. G1 is MSB and G8 is LSB. From pins 13 to 20 are for BLUE. B1 is MSB and B8 is LSB.
21	CLK		Clock input pin.
22	DVcc		Digital Vcc.
23 24	NC		Vacant pin (non-connection)
25	AGND		Analog GND.
26	VSET		Bias input pin. Normally, apply 0.8V. See "Note on use".

No.	Symbol	Equivalent circuit	Description
27	VREF		Internal reference voltage out-put pin 1.2V (typ) A pull-down resistance is necessary externally. See "Note on use"
28	NC		Vacant pin (non-connection)
29	AVcc		Analog Vcc
30	NC		Vacant pin but connect to AVcc*
31	BOUT		Analog output pin for BLUE.
32	NC		Vacant pin but connect to AVcc*
33	GOUT		Analog output pin for GREEN.
34	NC		Vacant pin but connect to AVcc*
35	ROUT		Analog output pin for RED.
36	NC		Vacant pin but connect to AVcc*
37	DGND		Digital GND
38	NC		Vacant pin (non-connection)

*: Pins 30, 32, 34 and 36 are vacant, but in order to reduce interference between the individual RGB outputs, connect them to AVcc.

Electrical Characteristics (Ta=25°C, AVcc=DVcc=5.0V, AGND=DGND=0.0V)

Item			Symbol	Measuring condition	Min.	Typ.	Max.	Unit
Resolution			RSL			8		bit
Monotony			MNT			Guara-ntee		
Differential linearity error			DLE	V_{SET}−AGND=0.8V R_L>10kΩ F.S.=Full-scale	−0.5		+0.5	LSB
Integral linearity error			ILE		−0.4		+0.4	% of F.S.
Maximum conversion speed			f_{MAX}	V_{SET}−AGND=0.8V R_L>10kΩ C_L<20pF	35			MSPS
Full-scale output voltage(note 1)			V_{OFS}		0.85	1.0	1.15	Vp-p
RGB output voltage full-scale ratio(note 2)			FSR		0	4	8	%
Output zero offset voltage			Voffset		−40	−6	0	mV
Output resistance			R_O		270	340	420	Ω
Consumption current			I_D	V_{SET}−AGND=0.8V R_L>10kΩ I_{REF}=−400μA	54	72	90	mA
Digital data input current	H level	Upper 2 bits	$I_{IH(U)}$	V_I=DVcc		1.2	20	μA
		Lower 6 bits	$I_{IH(L)}$			0.6	10	μA
	L level	Upper 2 bits	$I_{IL(U)}$	V_I=DGND	−10	0	10	μA
		Lower 6 bits	$I_{IL(L)}$		−10	0	10	μA
Clock input current		H level	I_{CLKH}	V_{CLK}=DVcc		3	30	μA
		L level	I_{CLKL}	V_{CLK}=DGND	−10	0	10	μA
V_{SET} input current			I_{SET}	V_{SET}−AGND=0.8V	−5	−0.3	0	μA
Internal reference voltage			V_{REF}	I_{REF}=−400μA	1.08	1.20	1.32	V
Set-up time			ts		12			ns
Hold time			th		3			ns

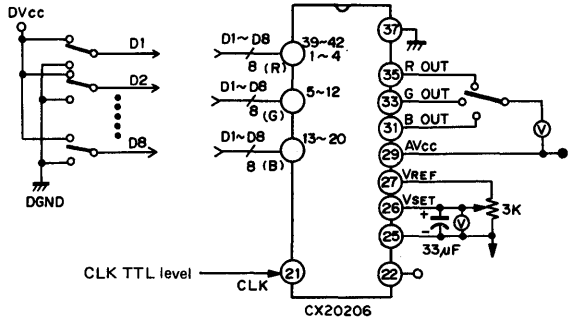
(Note 1) $A_{Vcc}-V_O$

(Note 2) Maximum value among

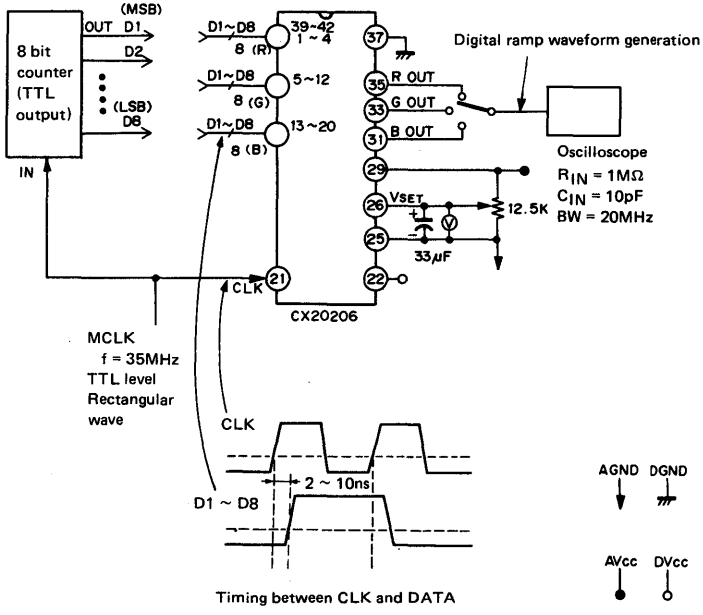
$$100 \times \left|\frac{V_{OFS(R)}}{V_{OFS(G)}} - 1\right|, \quad 100 \times \left|\frac{V_{OFS(G)}}{V_{OFS(B)}} - 1\right|, \text{ or } 100 \times \left|\frac{V_{OFS(B)}}{V_{OFS(R)}} - 1\right|$$

Electrical Characteristics Measuring Circuit

Differential linearity and integral linearity measuring circuits



Maximum conversion speed measuring circuit



Output voltage full-scale precision, RGB output voltage full-scale ratio, and output zero offset voltage measuring circuits

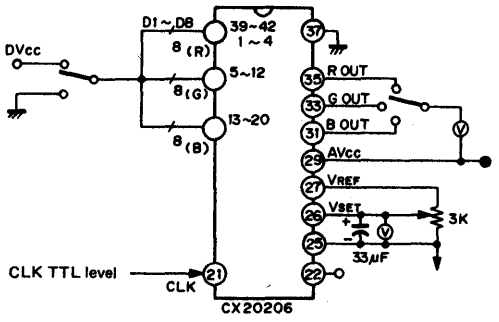
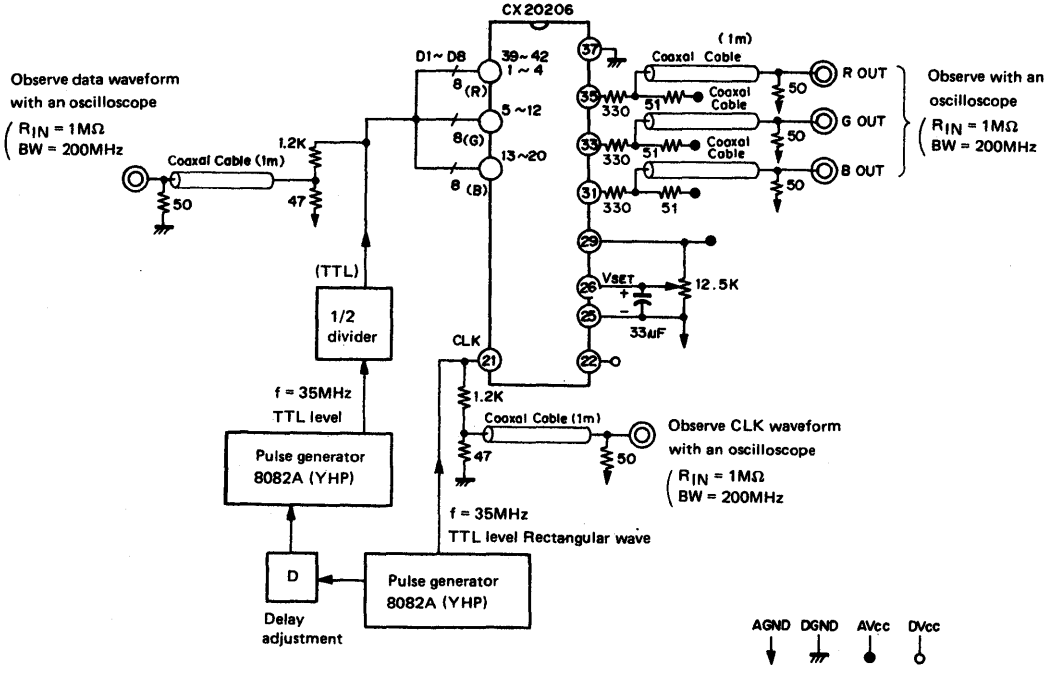


Fig. 1

Set-up time, hold time, and rise and fall time measuring circuits



Standard Circuit Design Data (Ta=25°C, AVcc=DVcc=5.0V, AGND=DGND=0.0V)

Item	Symbol	Measuring condition	Min.	Typ.	Max.	Unit
Crosstalk among R, G and B	CT	D/A OUT: 1Vp-p R_L>10kΩ C_L<20pF f_{DATA}=7MHz f_{CLK}=14MHz See Fig.2		−40	−33	dB
Glitch energy	GE	V_{SET}−AGND=0.8V R_L>10kΩ f_{CLK}=1MHz Digital ramp output See Fig.3(note 1)		30		pV-s
Rise time(note 2)	tr	V_{SET}−AGND=0.8V See Fig. 1.		5.5		ns
Fall time(note 2)	tf			5.0		ns
Settling time	tset			16		ns

(Note 1) Observe the glitch which is generated when the digital input varies as follows:

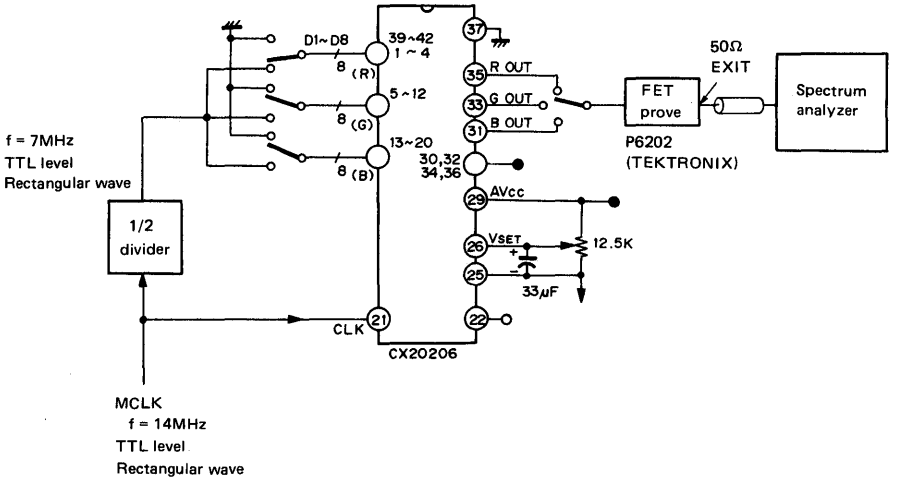
0 0 1 1 1 1 1 1 — 0 1 0 0 0 0 0 0
0 1 1 1 1 1 1 1 — 1 0 0 0 0 0 0 0
1 0 1 1 1 1 1 1 — 1 1 0 0 0 0 0 0

(Note 2) The time required for the D/A OUT to arrive at 90% of its final value from 10%.

See p. 204, for the definition of "Settling time".

Standard Circuit Design Data Measuring Circuit

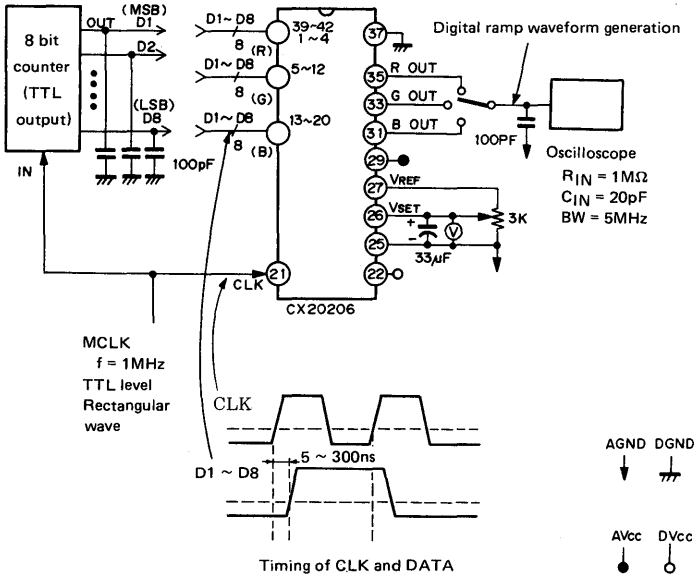
Fig. 2 Crosstalk among R, G and B measuring circuit



[Measuring method]
In case the measuring crosstalk of G → R

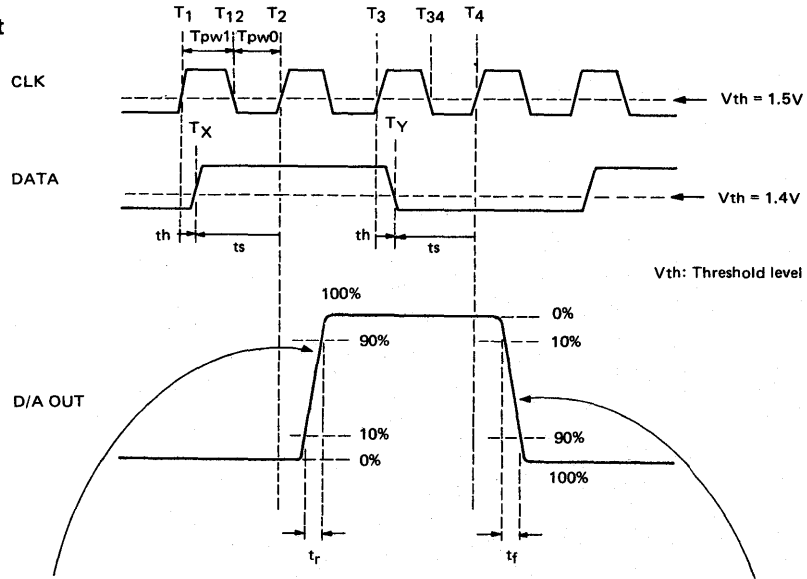
1 Apply the data to G only and measure the power of the frequency component of the data at R OUT.
2 Apply the data to R only and measure the power of the frequency component of the data at R OUT.
3 Take the difference of the above two powers. The unit is in dB.

Fig. 3 Glitch energy measuring circuit



Operation Description

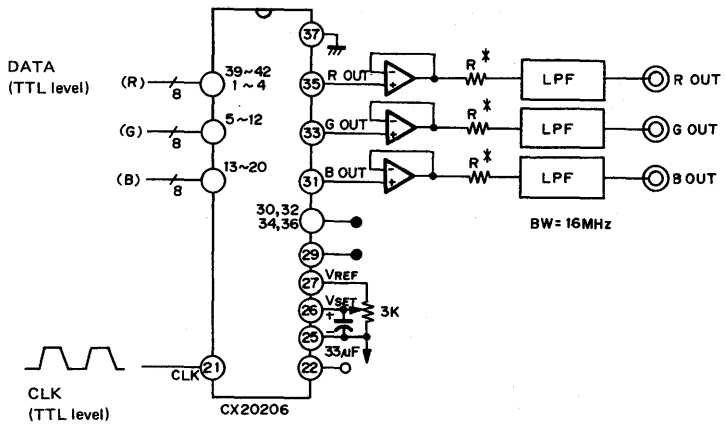
Timing chart



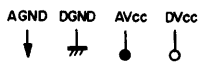
At the time t = T_X, the data of individual bits are switched and thereafter when the CLK becomes L → H at t = T_2, the D/A OUT is varied synchronous with it. That is, the D/A OUT is synchronous with the rise of the CLK.
(In this case, fetching of the data is carried out at the fall of the CLK (at the time when t = T_{12})).

At the time t = T_Y, the data of individual bits are switched and thereafter when the CLK becomes L → H at t = T_4, the D/A OUT is varied synchronous with it. That is, the D/A OUT is synchronous with the rise of the CLK.
(In this case, fetching of the data is carried out at the fall of the CLK (at the time when t = T_{34})).

Applied Circuit Example



R* is matching resistance for LPF



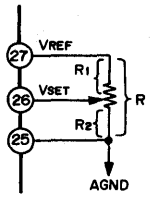
Note on Use

(1) Setting of pin 26 (V_{SET})

The full-scale of the D/A output voltage changes by applying voltage to pin 26 (V_{SET}). When load is connected to pin 27 (V_{REF}), DC voltage of 1.2V is issued and the said voltage is dropped to 0.8V by resistance division.

When the 0.8V is applied to pin 26 (V_{SET}), the D/A output of 1 Vp-p can be obtained.

(Example of use)

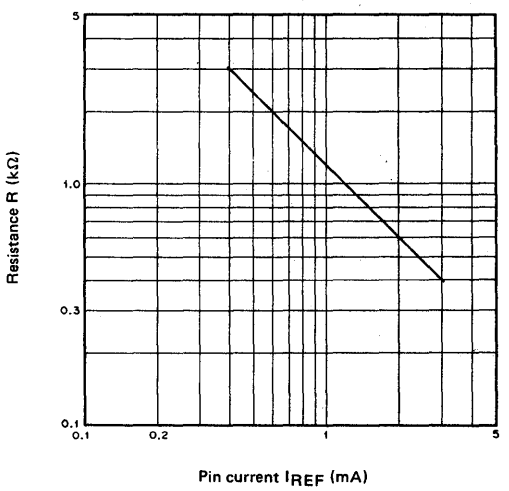


(Adjustment method)

1 The resistance R is determined in accordance with the recommended operating condition of I_{REF} (Current flowing through resistance R).
See R vs. I_{REF} of Fig. 4. The calculation expression is as follows:
$R = V_{REF}/I_{REF}$

2 Adjust the volume so that the RGB output voltage full-scale becomes 1.0V.
(At this point, it becomes R1:R2=1:2)

Fig. 4 Resistance vs. V_{REF} pin current



(2) Phase relationship between data and clock

In order to obtain the desired characteristics as a D/A converter, it is necessary to set the phase relationship correctly between the externally applied data and clock.

Satisfy the standard of the set-up time (ts) and hold time (th) indicated in the electrical characteristics. As to the meaning of ts and th, see the timing chart.

Moreover, the clock pulse width is desired to be as indicated in the recommended operating condition.

(3) Regarding the load of D/A output pin

Receive the D/A output of the next stage with high impedance. In other words, perform so that it becomes as follows:

$R_L > 10\ k\Omega$

$C_L < 20\ pF$

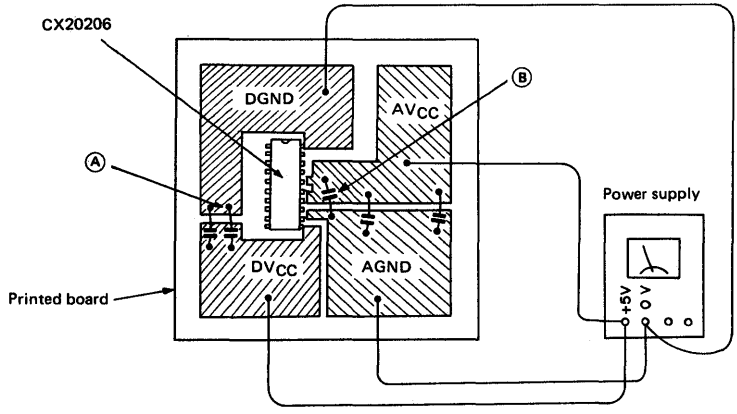
The temperature characteristics indicated in the characteristics diagram has been measured under this condition.

However, when it is made to $R_L \leqq 10\ k\Omega$ the temperature characteristics may change considerably. In addition, when it is made to $C_L \geqq 20\ pF$, the rise and fall of the D/A output become slow and will not operate at high speed.

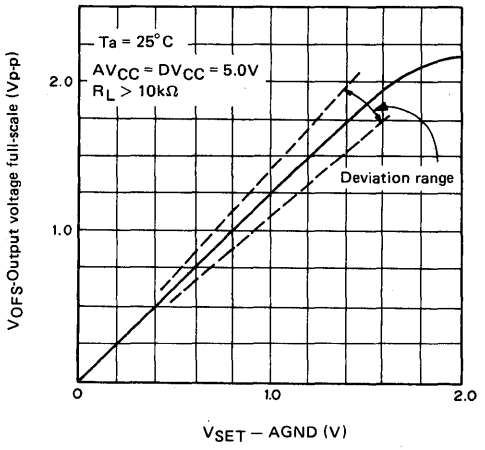
(4) Noise reduction measures

As the D/A output voltage is a minute voltage of approximately 4 mV per one step, ingenuity is required in reducing the noise entering from the outside of the IC as much as possible. Therefore use the items given below as reference.

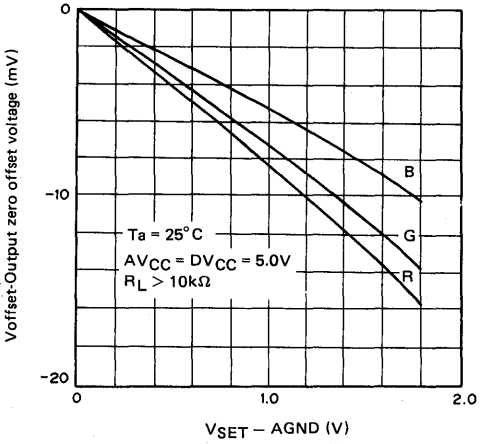
- When mounting onto the printed board, allow as much space as possible to the ground surface and the V_{CC} surface on the board and reduce the parasitic inductance and resistance.
- It is desirable that the AGND and DGND be separated in the pattern on the board. It is similar with AV_{CC} and DV_{CC}. As shown in the diagram below, for example, it is recommended that the wiring to the electric supply of AGND and DGND as also AV_{CC} and DV_{CC} be conducted separately, and then making AGND and DGND as also AV_{CC} and DV_{CC} in common right near the power supply respectively.
- Insert in parallel a 47 μF tantalum capacitor and a 1000 pF ceramic capacitor between the V_{CC} surface on the printed board and the nearmost ground surface. (A of diagram below). It is also desirable to insert the above between the V_{CC} surface near the pin of the IC and the ground surface. (B of diagram below). They are bypass capacitors to prevent bad effects from occurring to the characteristics when the power supply voltage fluctuates due to the clock, etc.
- It is recommended to reduce noise which overlaps the D/A output by inserting a capacitor of over 0.1 μF between pin 25 (AGND) and pin 26 (V_{SET}).



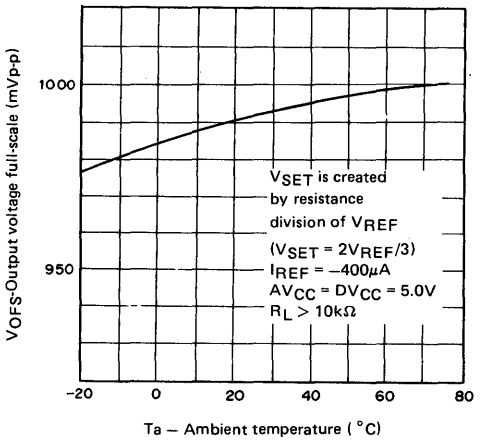
Output voltage full-scale vs. V_{SET}—AGND



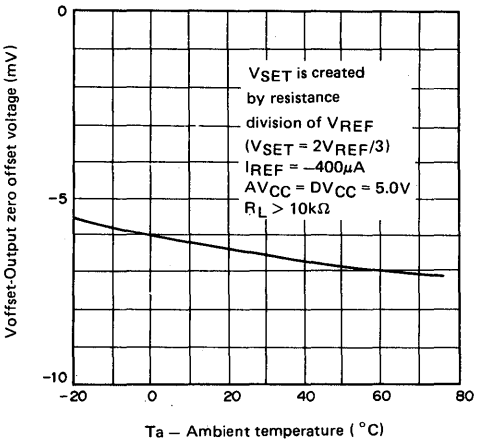
Output zero offset voltage vs. V_{SET}—AGND



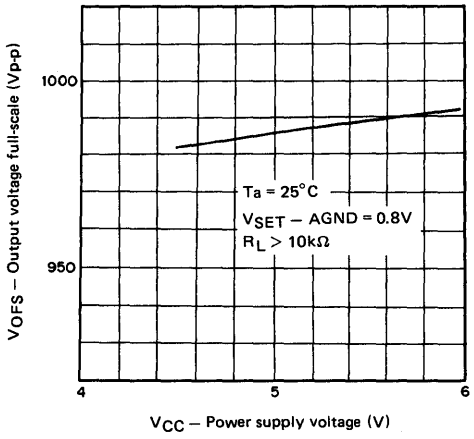
Output voltage full-scale vs. Ambient temperature



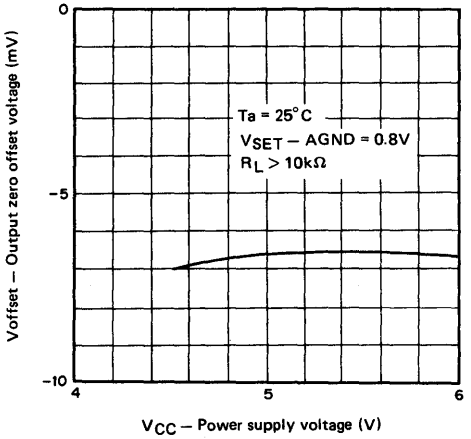
Output zero offset voltage vs. Ambient temperature



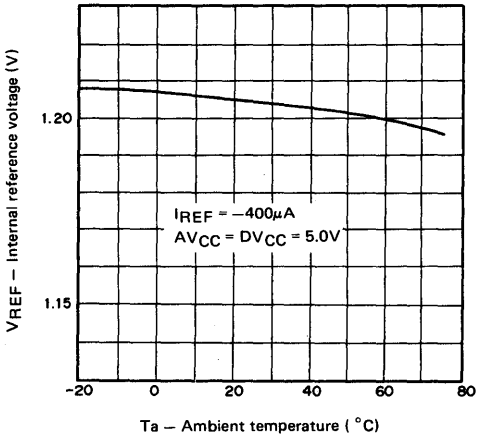
Output voltage full-scale vs. Power supply voltage



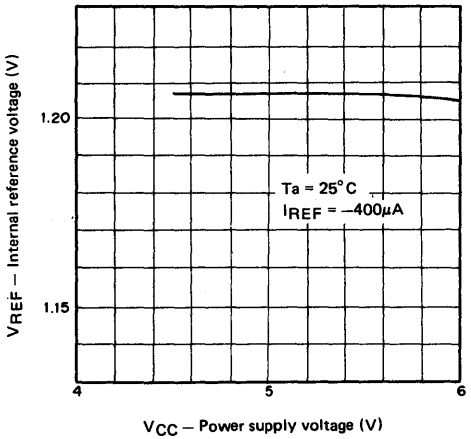
Output zero offset voltage vs. Power supply voltage



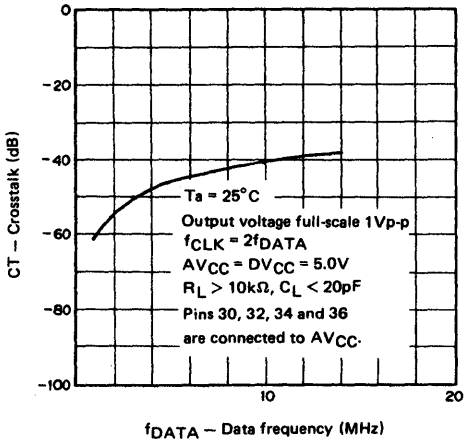
Internal reference voltage vs. Ambient temperature



Internal reference voltage vs. Power supply voltage

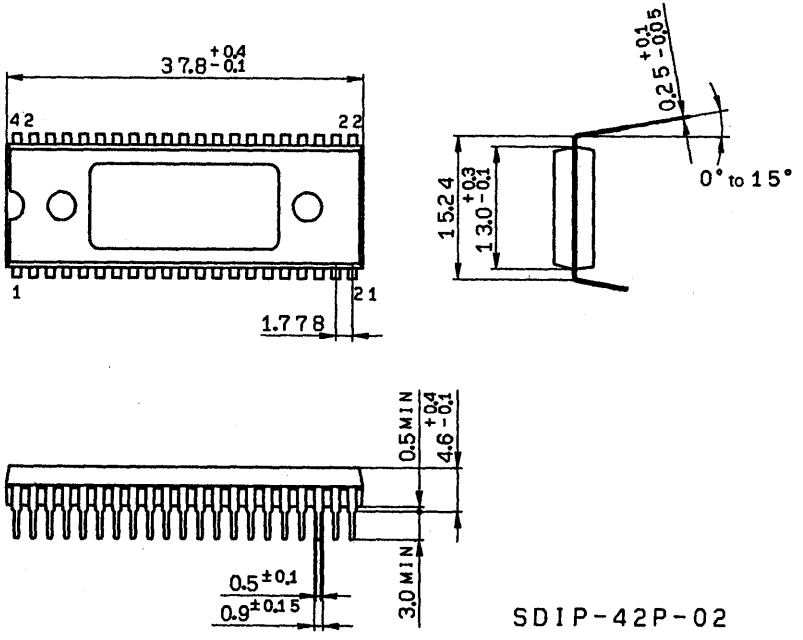


Crosstalk among R, G and B vs. Data frequency



Package Outline **Unit: mm**

42 pin SDIP (Plastic) 600 mil 4.4g



SONY CXA1106P/M

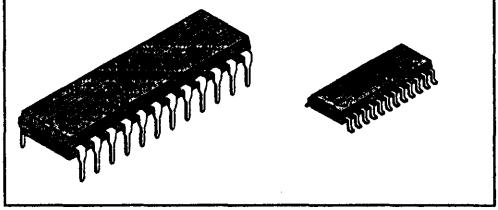
8-bit 35 MSPS High-Speed D/A Converter

Description

CXA1106P/M is an 8-bit 35MSPS high-speed D/A converter IC. Summing type current for the upper 2-bits and ladder type resistance for the lower 6-bits, ensure a low power consumption of 200 mW (Single power supply).
This IC is suitable for digital TV's, graphic displays and other applications.

CXA1106P
24 pin DIP (Plastic)

CXA1106M
24 pin SOP (Plastic)



Features

- Resolution 8-bit
- High speed operation
  35MSPS (Max. conversion speed)
- Non linear error
  less than ±1/2LSB
- Low glitch
- TTL compatible input
- +5V single power supply or ±5V dual power supply
- Low power consumption

+5V single power supply	200 mW (Typ.)
±5V dual power supply	400 mW (Typ.)

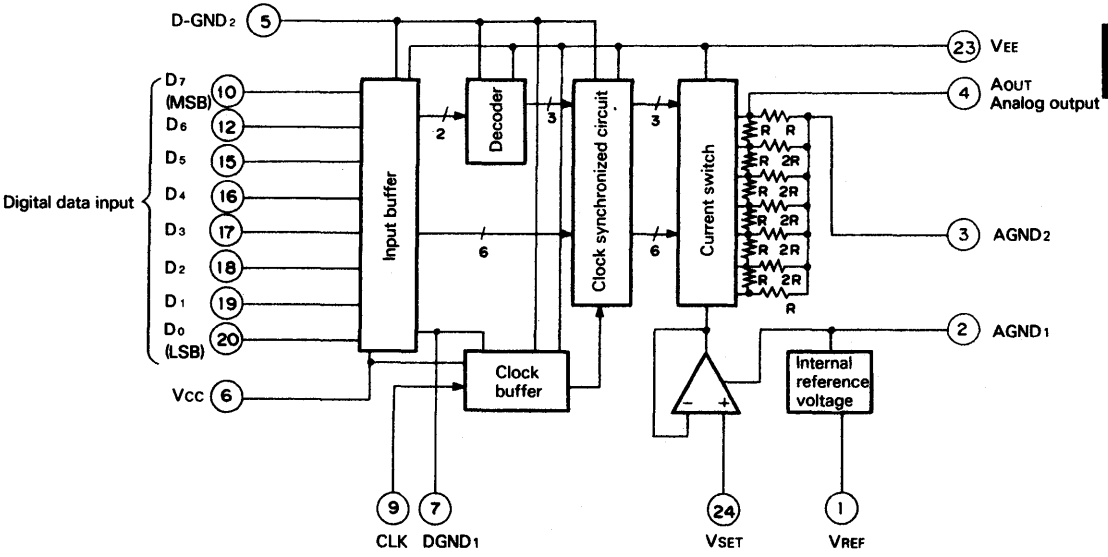
Function

8-bit 35 MSPS D/A converter

Structure

Bipolar silicon monolithic IC

Block Diagram



E89675 – ST

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}-DGND1	0 to 6	V
	V_{EE}–AGND1,2	−6 to 0	V
	DGND2–DGND1	0 to 6	V
• Digital input voltage	V_I	DGND1−0.3 to V_{CC}+0.3	V
	V_{CLK}	DGND1−0.3 to V_{CC}+0.3	V
• Input voltage (V_{SET} pin)	V_{SET}	V_{EE}−0.3 to V_{EE}+2.7	V
• Output current (V_{REF} pin)	I_{REF}	−5 to 0	mA
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	1.27	W

Recommended Operating Conditions

Single power supply

Item		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		V_{CC}, DGND2 AGND1, AGND2	4.75	5.00	5.25	V
		DGND2–AGND1 DGND2–AGND2	−0.2	0	0.2	V
		AGND1–AGND2	−0.1	0	0.1	V
Digital input voltage	H level	V_{IH}, V_{CLKH}	2.0		VCC	V
	L level	V_{IL}, V_{CLKL}	DGND1		1.0	V
V_{SET} input voltage		V_{SET}	0.70	0.84	1.0	V
V_{REF} pin current		I_{REF}	−3.0		−0.4	mA
Clock pulse width*		T_{PW1}	10			ns
		T_{PWO}	10			ns

***Note)** See Fig. 6. Timing chart

Dual power supply

Item		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
		V_{EE}	−5.5	5.00	−4.75	V
		DGND2–AGND1 DGND2–AGND2	−0.2	0	−0.2	V
		AGND1–AGND2	−0.1	0	0.1	V
Digital input voltage	H level	V_{IH}, V_{CLKH}	2.0		V_{CC}	V
	L level	V_{IL}, V_{CLKL}	DGND1		1.0	V
V_{SET} input voltage		V_{SET}	−4.30	−4.16	−4.00	V
V_{REF} pin current		I_{REF}	−3.0		−0.4	mA
Clock pulse width		T_{PW1}	10			ns
		T_{PWO}	10			ns

Pin Configuration (Top View)

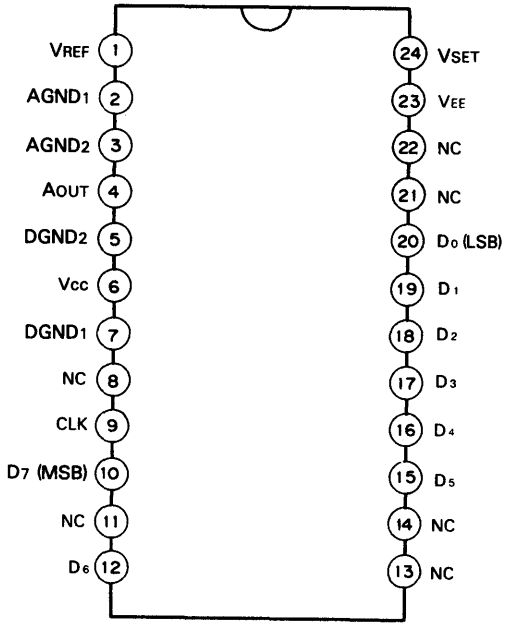


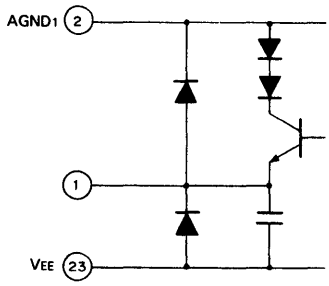
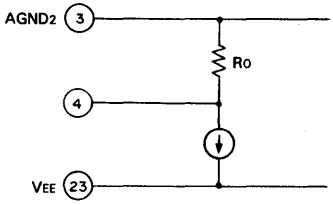
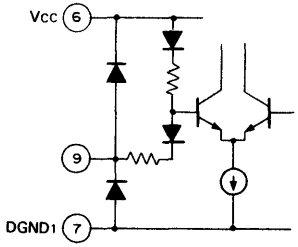
Fig. 1

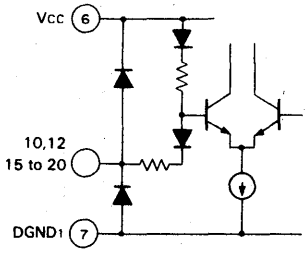
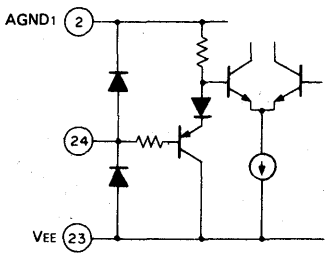
Input/Output Chart (when output full scale voltage at 1.00 V)

Table 1

Input code								Output voltage (Single supply)	Output voltage (dual supply)
MSB							LSB		
1	1	1	1	1	1	1	1	Vcc	−0V
1	0	0	0	0	0	0	0	Vcc −0.5V	−0.5V
0	0	0	0	0	0	0	0	Vcc −1.0V	−1.0V

Pin Description

No.	Symbol	Equivalent circuit	Description
1	V_{REF}		Internal reference voltage output pin 1.2 V (Typ.) An external pull down resistance is necessary. For reference see Notes on Application 1 on page 15.
2	$AGND_1$		Set to Analog V_{CC} for single power supply and to Analog GND for dual power supply. Connect to $AGND_2$ and use.
3	$AGND_2$		Connect to $AGND_1$
4	A_{OUT}		Analog output pin
5	$DGND_2$		Set to Digital V_{CC} for single power supply and to Digital GND for dual power supply.
6	V_{CC}		Digital V_{CC}
7	$DGND_1$		Digital GND
8	NC		Non-connection
9	CLK		Clock input pin

No.	Symbol	Equivalent circuit	Description
10, 12, 15 to 20	D_7, D_6, D_5 to D_0		Digital input pin D_1 to MSB, D_8 to LSB
11, 13, 14	NC		Non-connection
21, 22	NC		Non connection pin. But connect to AGND or VEE
23	VEE		Set to Analog GND for single power supply and to VEE for dual power supply.
24	VSET		Bias input pin Normally set VSET − VEE to 0.84V. For reference see Notes on Application 1.

See the Application Circuit for reference.

Electrical Characteristics (Ta = 25°C)

Single power supply

V_{CC} = DGND2 = AGND1 = AGND2 = 5V, DGND1 = V_{EE} = 0, V_{SET} = 0.84V

Item		Symbol	Test condition	Min.	Typ.	Max.	Unit
Resolution		n			8		bit
Maximum conversion speed		f_{MAX}	R_L > 10kΩ, C_L < 20pF	35			MSPS
Linearity error		E_L	R_L > 10 KΩ	−0.5		+0.5	LSB
Differential linear error		E_D		−0.5		+0.5	LSB
Full scale output voltage		V_{FS}	R_L > 10KΩ	0.9	1.0	1.1	V
Offset voltage*		V_{OS}	R_L > 10KΩ	0	4	10	mV
Output resistance		R_O		290	350	410	Ω
Power supply current		I_{CC}	R_L > 10KΩ I_{REF} = −400μA	32	40	48	mA
Digital input current	H level	I_{IH}		0		5	μA
	L level	I_{IL}		−400		0	μA
V_{SET} input current		I_{SET}		−3		0	μA
Internal reference output voltage		V_{REF}	I_{REF} = −400μA	1.17	1.25	1.33	V
Accuracy output voltage range		V_{OC}	R_L > 10KΩ	0.5	1.0	1.5	V
Set up time		t_s		10			ns
Hold time		t_h		2			ns
Propagation delay time		t_{PD}	R_L > 10KΩ		11		ns
Glitch energy		GE	R_L > 10KΩ f_{CLK} = 1 MHz Digital lamp output		30		pV-s
Rise time		tr	Same as CX20206		5.5		ns
Fall time		tf			5.0		ns
Settling time		tset			16		ns

***Note)** V_{OS} = AGND2 − V_{255} (V_{255} is the output voltage when full input is at high level)

See p. 204, for the definition of "Rise, Fall and Settling time".

Dual power supply

V_{CC} = 5V, $DGND_1$ = $DGND_2$ = $AGND_1$ = $AGND_2$ = 0, V_{EE} = −5V, V_{SET} − V_{EE} = 0.84V

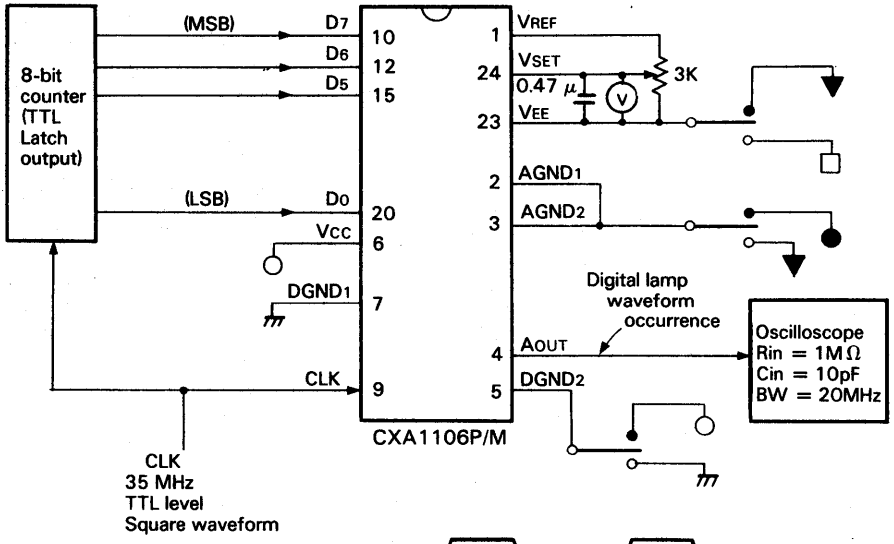
Item		Symbol	Test condition	Min.	Typ.	Max.	Unit
Resolution		n			8		bit
Maximum conversion speed		f_{MAX}	R_L > 10kΩ, C_L < 20pF	35			MSPS
Linearity error		E_L	R_L > 10 KΩ	−0.5		+0.5	LSB
Differential linear error		E_D		−0.5		+0.5	LSB
Full scale output voltage		V_{FS}	R_L > 10KΩ	0.9	1.0	1.1	V
Offset voltage		V_{OS}	R_L > 10KΩ	0	4	10	mV
Output resistance		R_O		290	350	410	Ω
Power supply current		I_{CC}	R_L > 10KΩ I_{REF} = −400μA	24	30	36	mA
		I_{EE}		40	50	60	mA
Digital input current	H level	I_{IH}		0		5	μA
	L level	I_{IL}		−400		0	μA
V_{SET} input current		I_{SET}		−3		0	μA
Internal reference output voltage		V_{REF}	I_{REF} = −400μA	−3.83	−3.75	−3.67	V
Accuracy output voltage range		V_{OC}	R_L > 10KΩ	0.5	1.0	1.5	V
Set up time		t_s		10			ns
Hold time		t_h		2			ns
Propagation delay time		t_{PD}	R_L > 10KΩ		11		ns
Glitch energy		GE	R_L > 10KΩ f_{CLK} = 1 MHz Digital lamp output		30		pV-s
Rise time		tr	Same as CX20206		5.5		ns
Fall time		tf			5.0		ns
Settling time		tset			16		ns

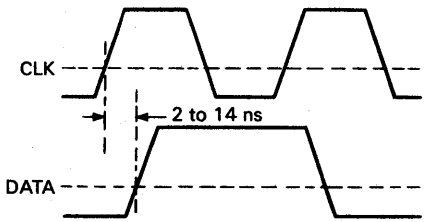
***Note)** V_{OS} = $AGND_2$ − V_{255} (V_{255} is the output voltage when full input is at high level)

See p. 204, for the definition of "Rise, Fall and Settling time".

Electrical Characteristics Test Circuit

Test Circuit for Maximum Conversion Speed





Timing between CLK and Data

Fig. 2

Test Circuit for Set-up Time, Hold Time

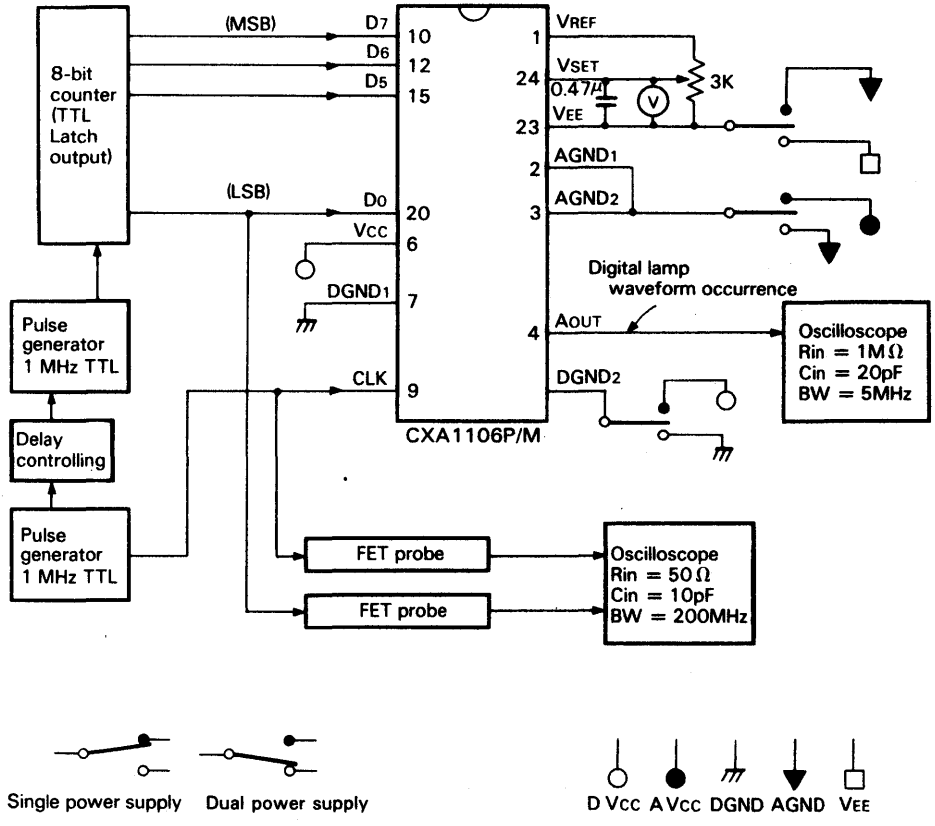
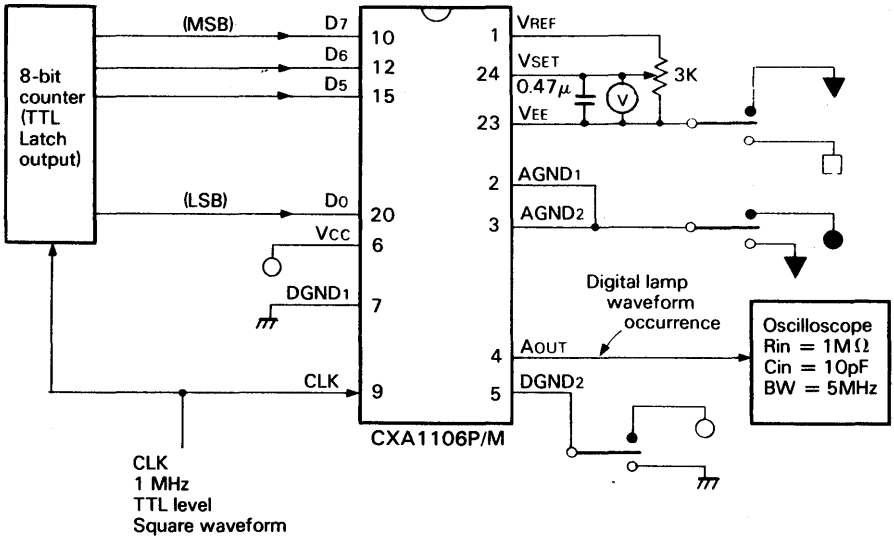
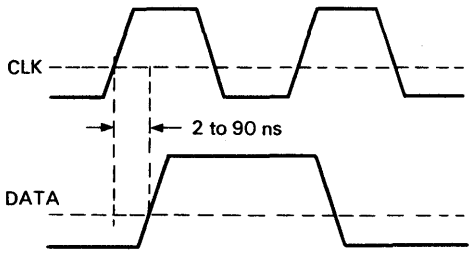


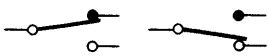
Fig. 3

Test Circuit for Glitch Energy





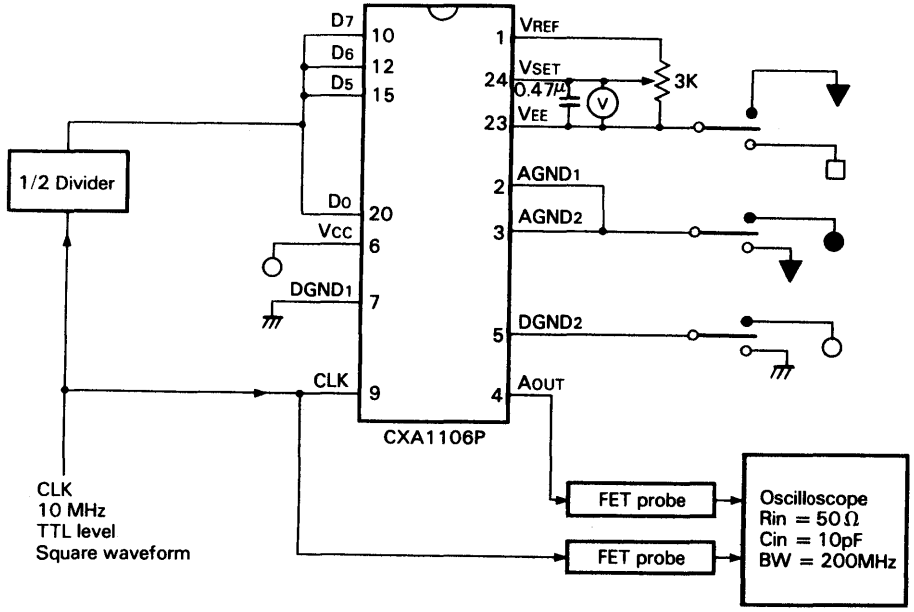
Timing between CLK and Data

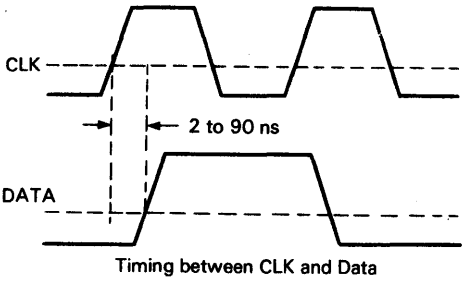


Single power supply Dual power supply

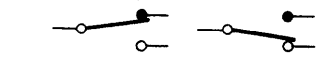
Fig. 4

Test Circuit for Propagation Delay Time





Timing between CLK and Data



Single power supply Dual power supply

Fig. 5

Operation

Timing chart

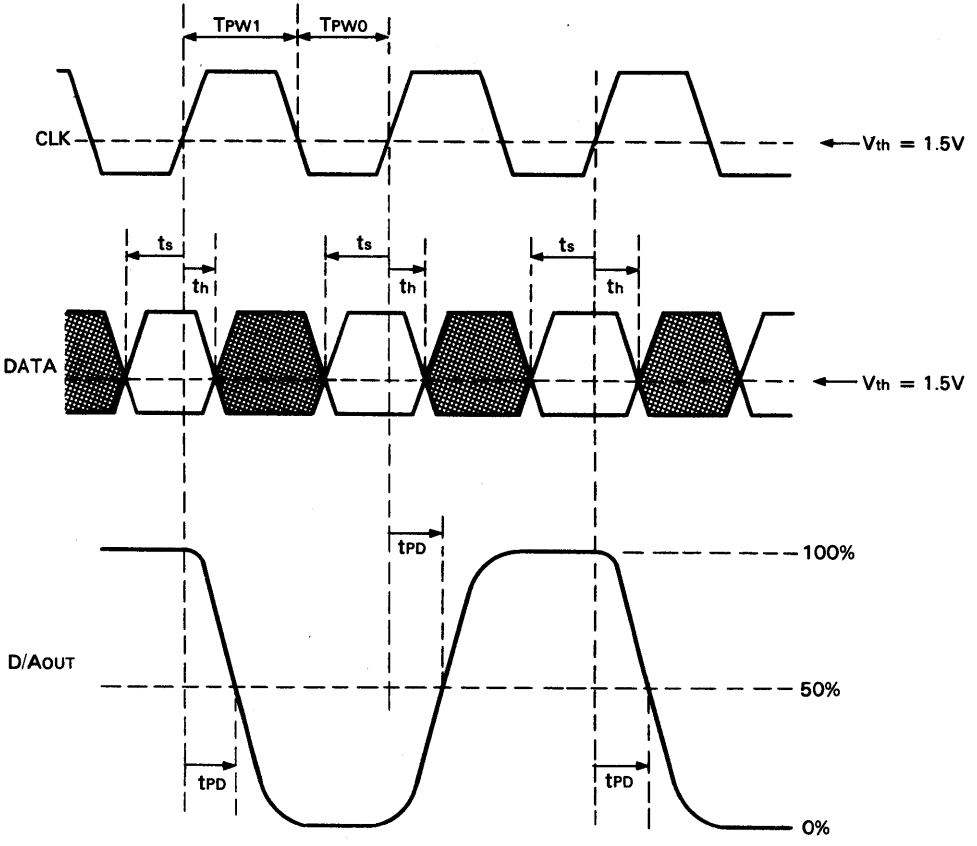
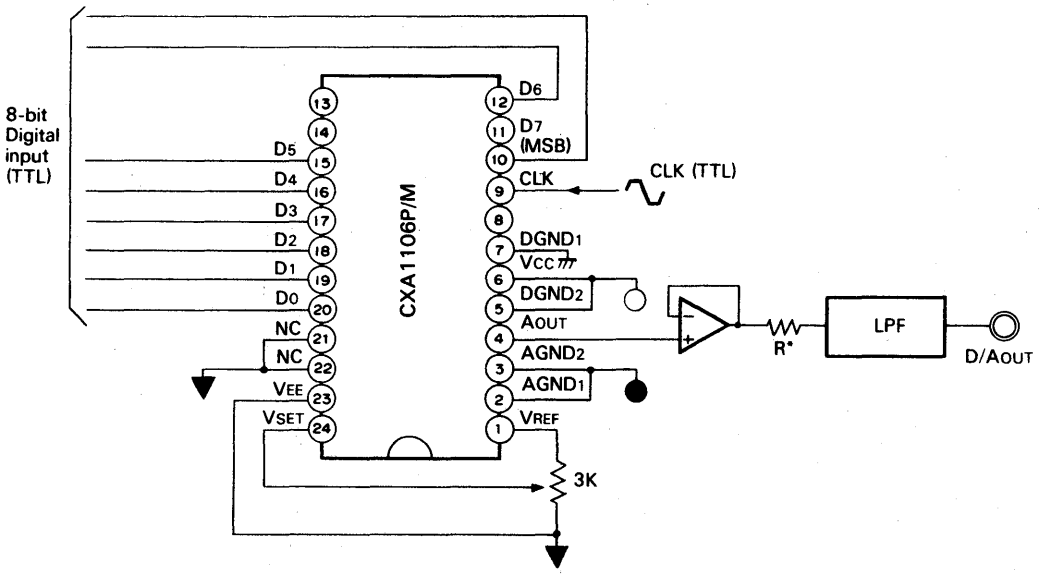


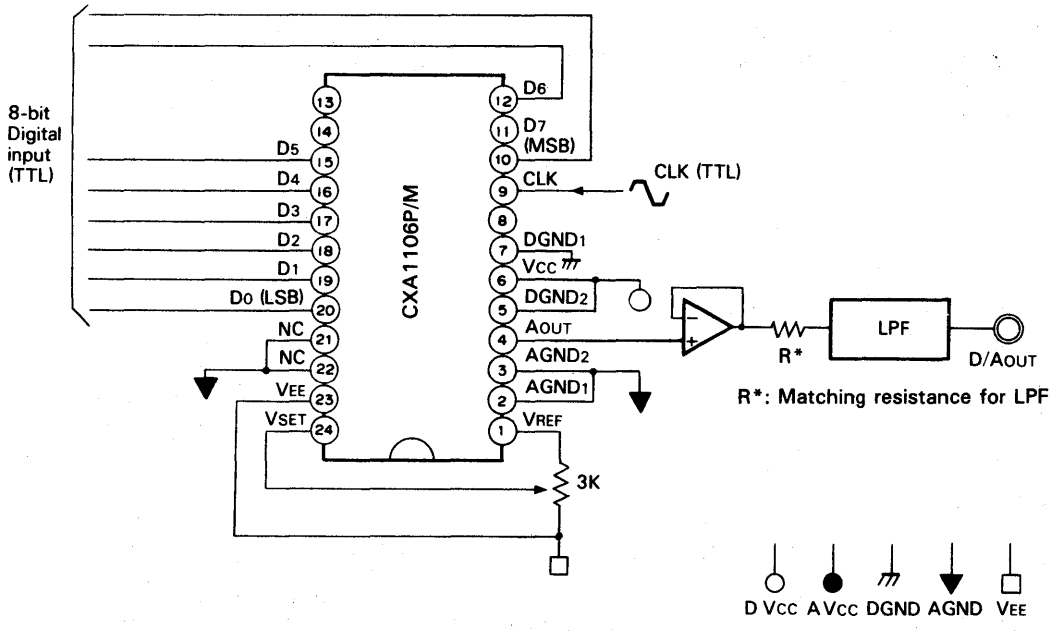
Fig. 6

Application Circuits

Single power supply



Dual power supply



Notes on Application

1. Setting of VSET Pin (Pin 24)

   The full-scale voltage of the D/A output is determined by VSET input voltage. As about (1.2V - VEE) DC voltage is generated at VREF pin (Pin 1) by connecting an external resistor from VREF pin to VEE pin (Pin 23), divide this voltage using resistors and apply it to VSET pin as Fig. 7.

(Example of usage)

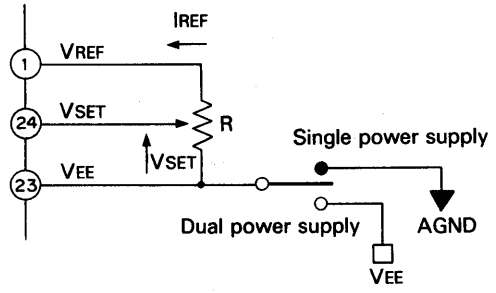


Fig. 7

The full-scale voltage of the D/A output can be determined from the following equation.

$$V_{FS} = 1.2\ (V_{SET} - V_{EE})\ (R_L > 10K\Omega,\ 0.4V \leq V_{SET} \leq 1.2V)$$

Select an external resistor R (Connected to VREF pin) so that IREF (current of an external resistor) is within the value indicated as the Recommended Operational Conditions (-3 mA $< I_{REF} < -0.4$ mA).

2. Phase relation between Data and Clock

   To make the best use of the inherent characteristics of this D/A converter the phase relation between the data and clock applied from the exterior, should be properly set.
   Set up time (ts) and Hold time (th) should be as indicated in the Electrical characteristics. For ts and th refer to Fig. 6 in the Timing Chart.
   Also, set the clock pulse width according to the Recommended Operating Conditions.

3. D/A output pin Load

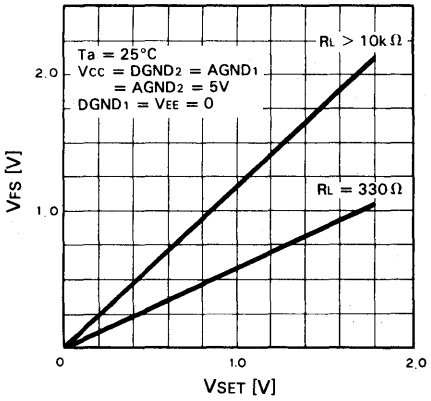
   Receive the D/A output stage at high impedance, so as to obtain

   $R_L > 10K\Omega$
   $C_L < 20pF$

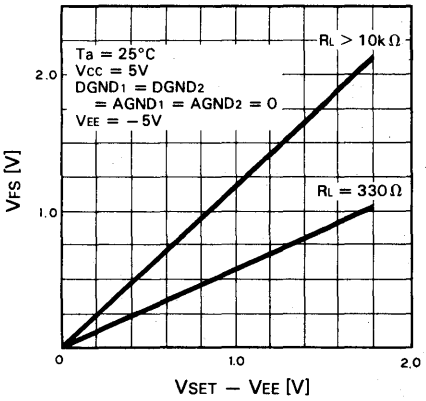
4. Noise reduction

   Refer to the following notes in order to minimize noise contamination that occurs from outside the IC and penatrates D/A output.
   - The power supply line and ground line should be made as wide as possible when fixed to the printed circuit board. Analog and Digital circuits should be separated.
   - Connected a bypass capacitor between each of DVCC (Pin 6) and DGND1 (Pin 7); AGND1,2 (Pins 2, 3) and VEE (Pin 23); VSET (Pin 24) and VEE (Pin 23), respectively.

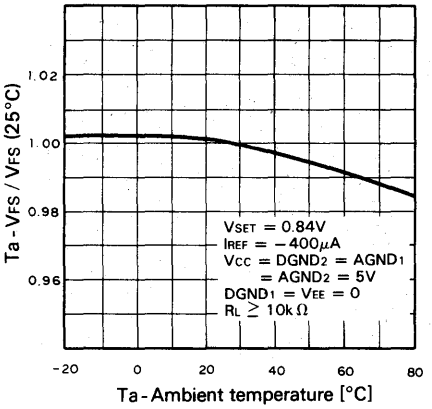
Full-scale output voltage V_{FS} and V_{SET} (Single power supply)



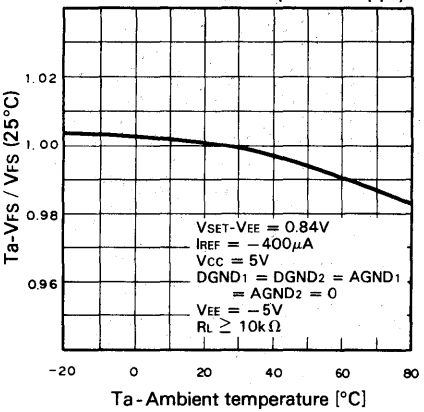
Full-scale output voltage V_{FS} and V_{SET}-V_{EE} (Dual power supply)



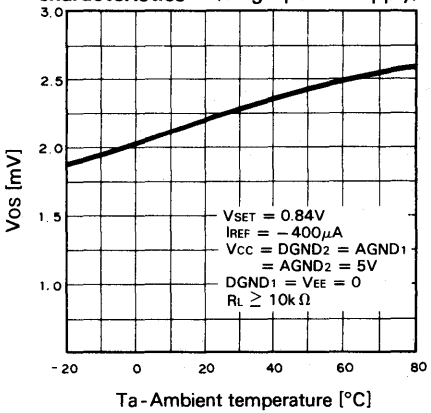
Full-scale output voltage V_{FS} temperature characteristics (Single power supply)



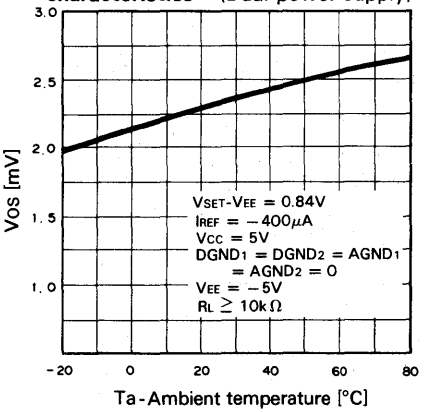
Full-scale output voltage V_{FS} temperature characteristics (Dual power supply)



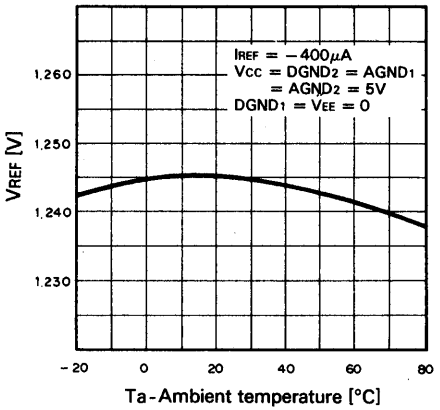
Output offset voltage V_{OS} temperature characteristics (Single power supply)



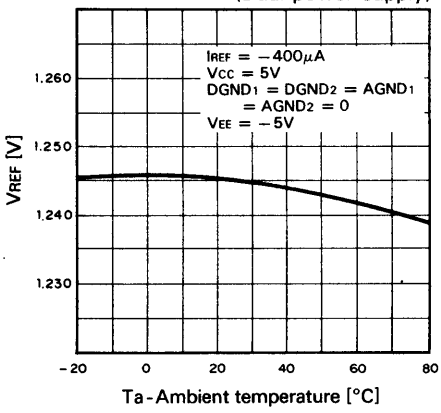
Output offset voltage V_{OS} temperature characteristics (Dual power supply)



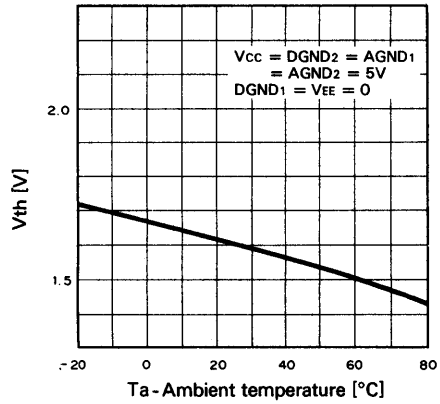
Internal reference voltage VREF temperature characteristics (Single power supply)



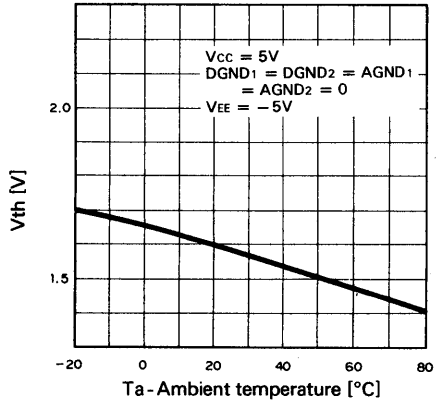
Internal reference voltage VREF temperature characteristics (Dual power supply)



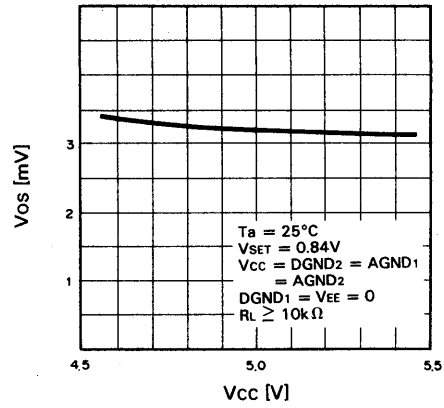
Threshold voltage Vth of digital input temperature characteristics (Single power supply)



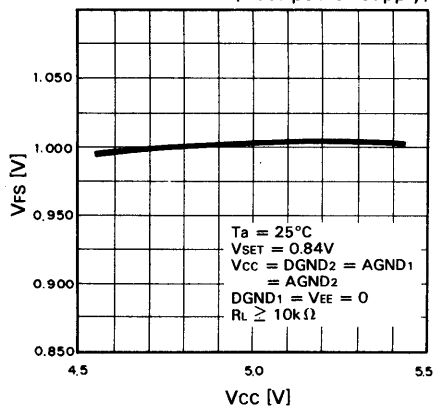
Threshold voltage Vth of digital input temperature characteristics (Dual power supply)



Output offset voltage VOS to Supply voltage (Single power supply)

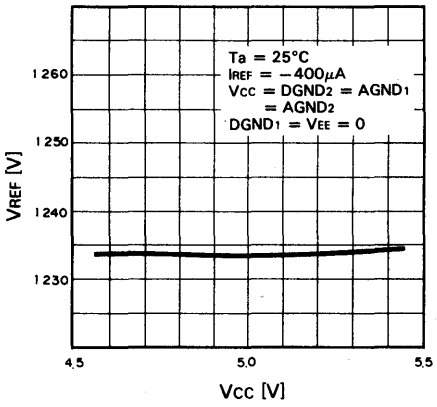


Output full-scale voltage VFS to Supply voltage (Dual power supply)



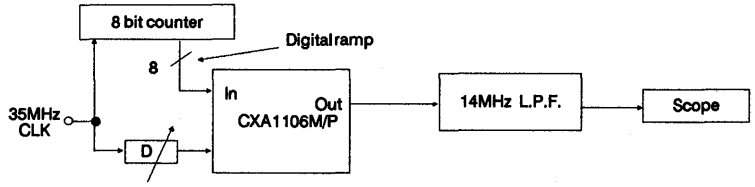
Internal reference voltage V_{REF} to supply voltage

(Single power supply)



Glitch Energy Test Data

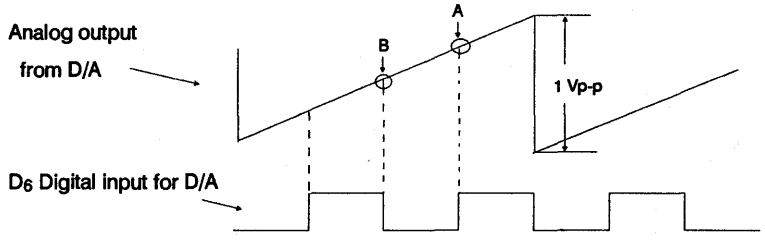
(1) Test Method



Test Circuit

In the above figure, a ramp waveform is generated at the D/A output and the glitch is measured by an oscilloscope. The largest glitch is supposed to be generated at point A and B as below because of the internal system mechanism of the CXA1106M/P.

These points A and B were picked up and the glitches which appeared there were observed.



Measure Points

(2) Test Result

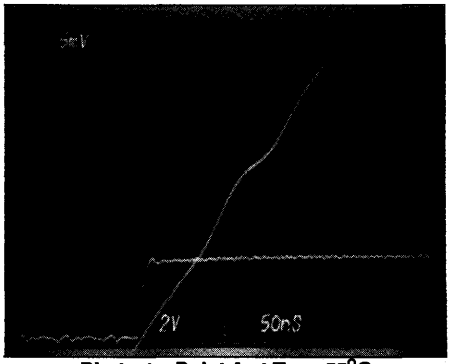


Photo 1. Point A at Tc=-55°C

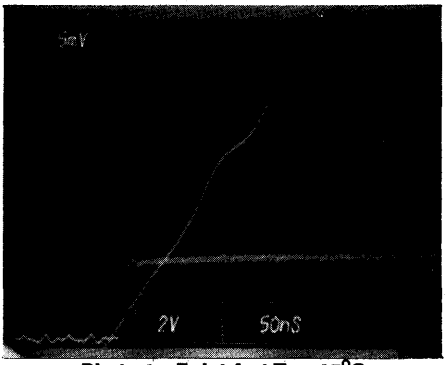


Photo 2. Point A at Tc=25°C

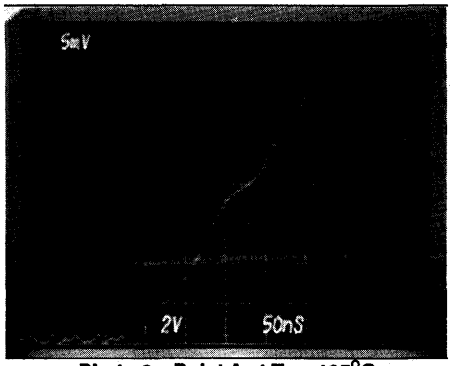


Photo 3. Point A at Tc=125°C

50ns

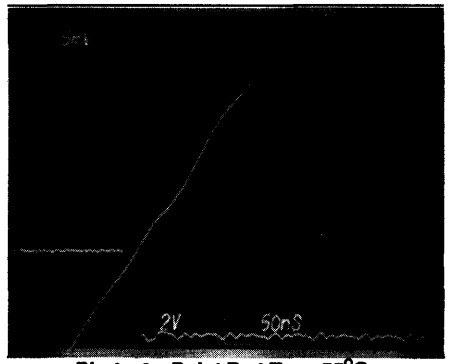


Photo 4. Point B at Tc=-55°C

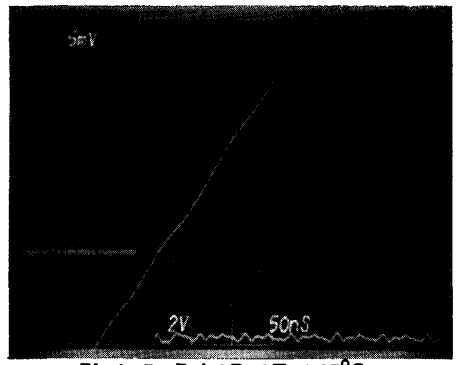


Photo 5. Point B at Tc=25°C

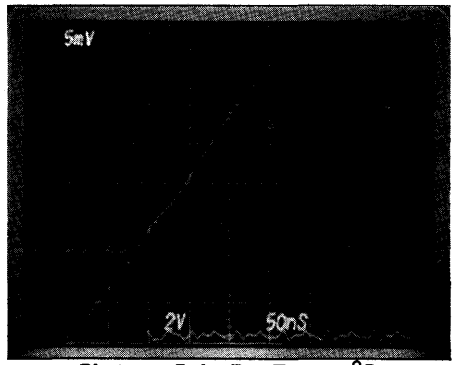
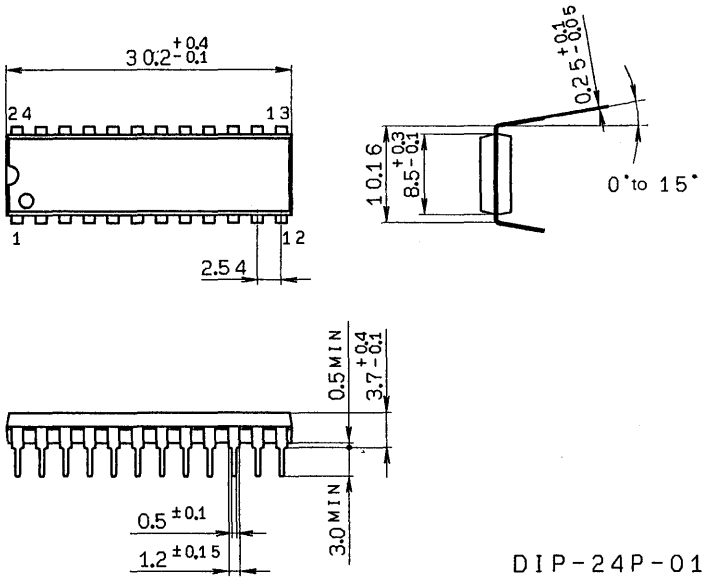


Photo 6. Point B at Tc=125°C

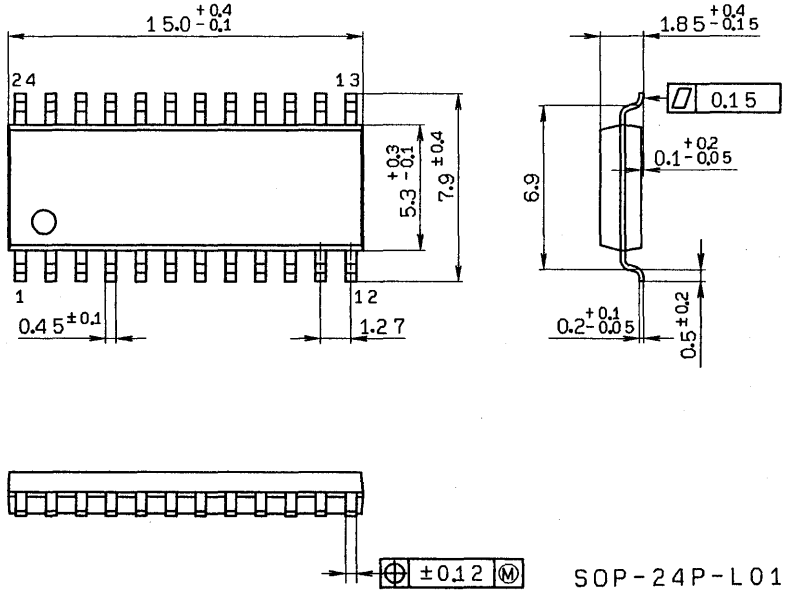
Package Outline Unit : mm

CXA1106P 24 pin DIP (Plastic) 400mil 2.0g



DIP-24P-01

CXA1106M 24 pin SOP (Plastic) 300mil 0.3g



SOP-24P-L01

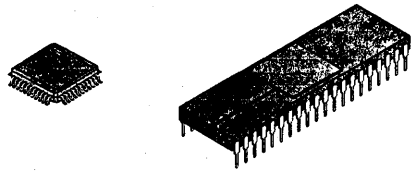
SONY CXA1146Q/D /CXA1156Q/D

8bit 160/300MSPS Triple VIDEO DAC

Advance Information

Note : This specification is subject to change.

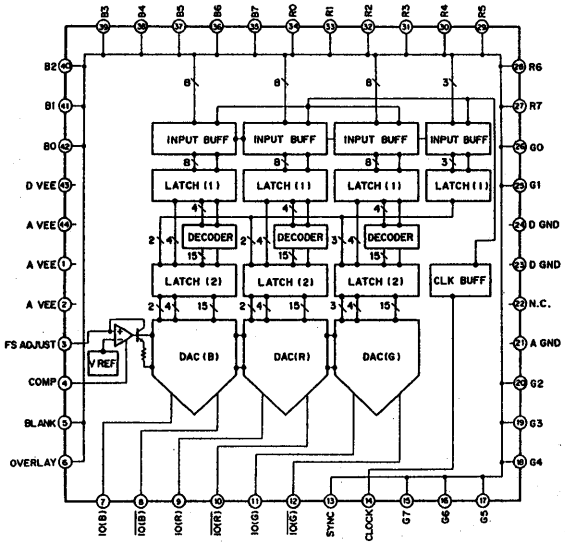
44 pin QFP (Ceramic) 40 pin DIP (Ceramic)



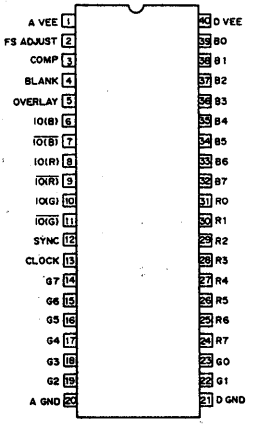
Features

- 160/300MHz update rate
- 8-bit RGB
- Sync., Blank and Overlay
- 25 Ω/37.5 Ω Load
- I (+), I (−) outputs
- RS-343A Compatible Output
- ECL 100K and 10K Compatible Inputs
- −5.5 to −4.2 Volt Power Supply
- Package − QFP, DIP (To be available)

CXA1146Q/CXA1156Q − QFP
(Quad Flat Pack) version
Pin Configuration (Top View)
Block Diagram



CXA1146D/CXA1156D − DIP version
(To be available)
Pin Configuration (Top View)



(Pin Replacable with TDC1318 and Bt109.)

AE89676 − ST

Absolute Maximum Ratings (Ta = 25°C)

	Rating	Unit
V_{EE}	−7 to +0.5	V
Input voltage, Digital	V_{EE} to +0.5	V
Input voltage, Reference	V_{EE} to +0.5	V
Output current, I (+), I (−)	50	mA
Storage temperature	−65 to +150	℃

Operating Conditions

Symbol	Item		Min.	Typ.	Max.	Unit
V_{EE}	Supply voltage		−4.2	−5.2	−5.5	V
tpw1	CLK pulse width High	CXA1146	3.0			ns
		CXA1156	1.5			
tpw0	CLK pulse width Low	CXA1146	3.0			ns
		CXA1156	1.5			
ts	Set up time	CXA1146	1.5			ns
		CXA1156	1.0			
th	Hold time		0			ns
V_{IL}	Input voltage logic Low				−1.49	V
V_{IH}	Input voltage logic High		−1.05			V
I_{REF}	Reference current			1.6		mA
Tc	Case temperature		−55		125	℃

Electrical Characteristics (CXA1146) (V_{EE} = −5.2V, Ta = 25°C)

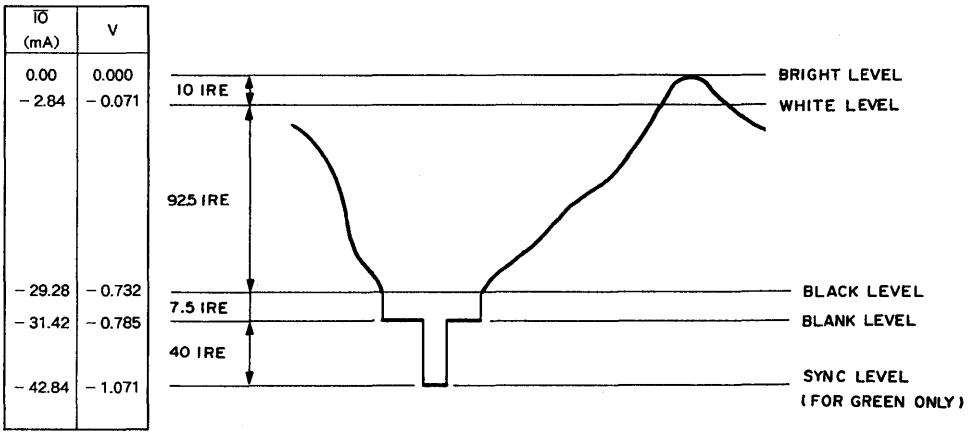
Item	Symbol	Min.	Typ.	Max.	Unit
Supply current	I_{EE}		−200		mA
Compliance voltage output (+)	Vocp	−1.2		1.5	V
Compliance voltage output (−)	Vocn	−1.2		1.5	V
Equiv. output resistance	Ro	50			kΩ
Equiv. output capacitance	Co		10		pF
Max. output current output (+)	Iop	−44			mA
Max. output current output (−)	Ion	−44			mA
Input current logic Low	I_{IL}		20		μA
Input current logic High	I_{IH}		20		μA
Max. conversion rate	Fs	160			MHz
CLOCK to output delay	td		2.0		ns
Current settling time	tset			5.0	ns
Rise time, Current	tr			2.0	ns
Fall time, Current	t_f			2.0	ns
Integral linearity error	E_{LI}			±1/2	LSB
Differential linearity error	E_{LD}			±1/2	LSB
Output offset current	I_{OF}			10.0	μA
Absolute gain error	E_G			7.0	% of F.S.
Gain error tempco.	T_{CG}		0		% of F.S./°C
Differential phase	DP			1.0	degree
Differential gain	DG			2.0	%
Glitch energy	GE		1.3		LSB • nsec

Electrical Characteristics (CXA1156) (VEE = − 5.2V, Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply current	I_{EE}		− 300		mA
Compliance voltage output (+)	Vocp	− 1.2		1.5	V
Compliance voltage output (−)	Vocn	− 1.2		1.5	V
Equiv. output resistance	Ro	50			kΩ
Equiv. output capacitance	Co		10		pF
Max. output current output (+)	Iop	− 44			mA
Max. output current output (−)	Ion	− 44			mA
Input current logic Low	I_{IL}		40		μA
Input current logic High	I_{IH}		40		μA
Max. conversion rate	Fs	300			MHz
CLOCK to output delay	td		1.0		ns
Current settling time	tset			2.5	ns
Rise time, Current	tr			1.0	ns
Fall time, Current	t_f			1.0	ns
Integral linearity error	E_{LI}			± 1/2	LSB
Differential linearity error	E_{LD}			± 1/2	LSB
Output offset current	I_{OF}			10.0	μA
Absolute gain error	E_G			7.0	% of F.S.
Gain error tempco.	T_{CG}		0		% of F.S./°C
Differential phase	DP			1.0	degree
Differential gain	DG			2.0	%
Glitch energy	GE		1.3		LSB • nsec

Pin Descriptions

Pin Name	Description
BLANK	Control pin for composite blank. Logic "1" sets the D/A output to the blanking level. The output is delivered with the rising edge of CLOCK. The voltage level for the pin is ECL compatible.
SYNC	Control pin for composite sync. Logic "1" sets the D/A output to have composite sync level only for green. The sync is delivered with the rising edge of CLOCK. The voltage level for the pin is ECL compatible.
OVERLAY	Control pin for overlay. Logic "1" forced the D/A output to the overlay voltage level. The overlay is delivered with the rising edge of CLOCK. The voltage level for the pin is ECL compatible.
R0 – R7 G0 – G7 B0 – B7	Data inputs for red, green and blue, respectively. R0, G0 and B0 are for least significant bit. These inputs level are ECL compatible.
CLOCK	Clock input pin. ECL compatible.
$I_{O(R)}$, $\overline{I_{O(R)}}$ $I_{O(G)}$, $\overline{I_{O(G)}}$ $I_{O(B)}$, $\overline{I_{O(B)}}$	Current outputs for red, green and blue. Complementary outputs. These can directly drive doubly-terminated 75 Ω and 50 Ω loads.
FS ADJUST	Control pin for full-scale. The scale is set by a resistor (Rset) connected between this pin and AGND. The relation between Rset and R_L which is current output load is the following : Rset = 1.24V/ ((661mV/R_L) × (16/255)) Ohms
COMP	Compensation pin. This provides compensation for internal amplifier built-in.



* In case of doubly-terminated 50 Ω load.

Fig. 1. Composite Video Level

Description	$\overline{IO}$ (mA)	OVERLAY	SYNC	BLANK	D/A Input Data
OVERLAY	0.00	1	0	0	$ × ×
WHITE	− 2.84	0	0	0	$ FF
DATA		0	0	0	data
BLACK	− 29.28	0	0	0	$ 00
BLANK	− 31.42	×	0	1	$ × ×
SYNC	− 42.84	×	1	×	$ × ×

Table 1. Video Output Truth Table

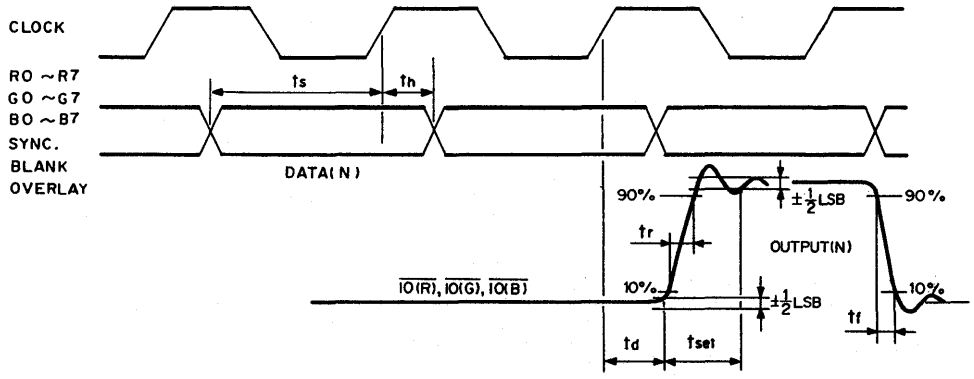


Fig. 2. Timing Diagram

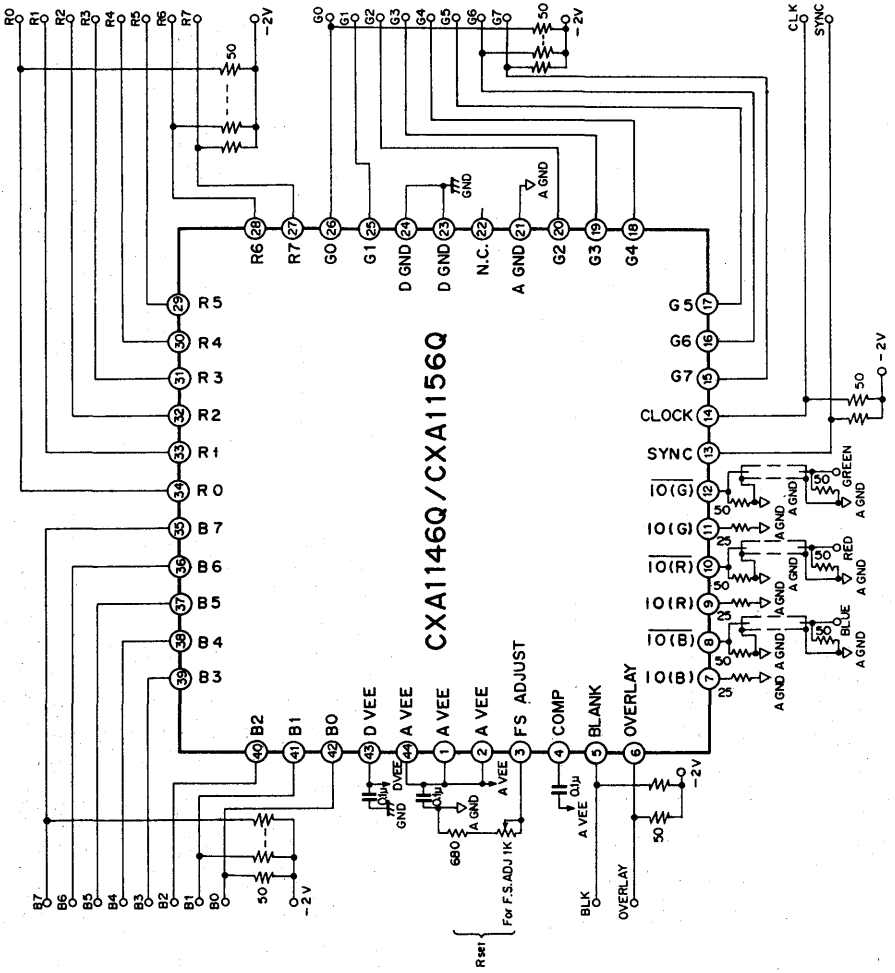
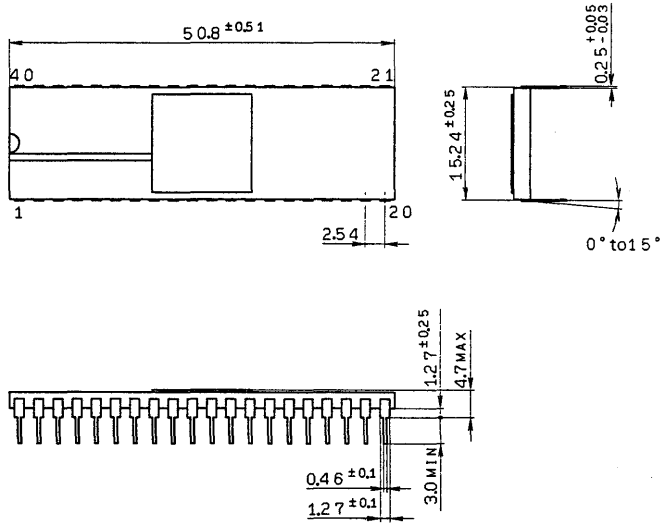


Fig. 3. Typical Circuit Connection

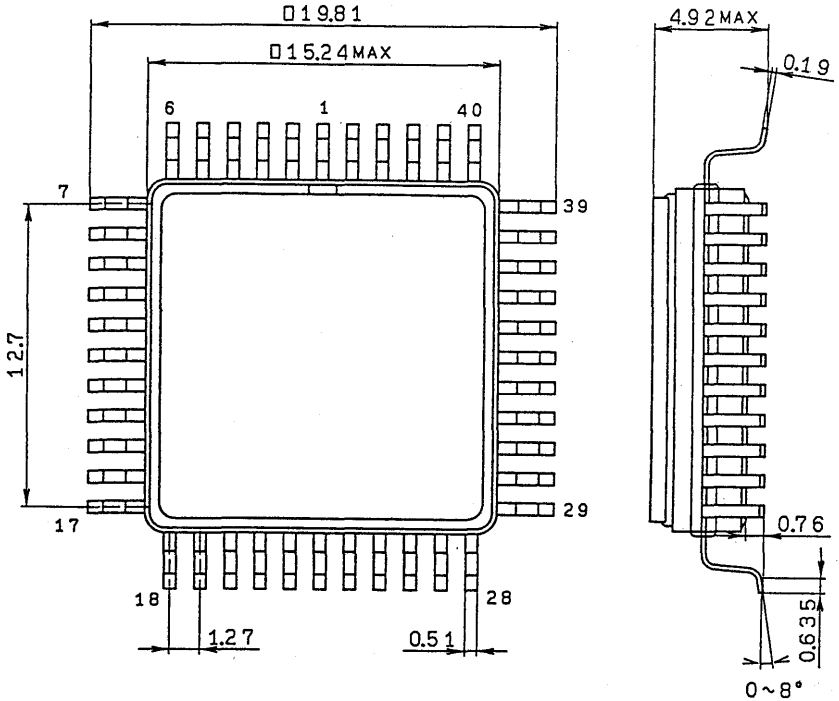
Package Outline Unit : mm

CXA1146D/CXA1156D 40 pin DIP (Ceramic) 600mil



DIP-40C-01

CXA1146Q/CXA1156Q 44 pin QFP (Ceramic) 50mil



SONY

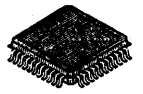
CXA1236Q

8bit 500MSPS Single VIDEO DAC

Advance Information

Note : This specification is subject to change.

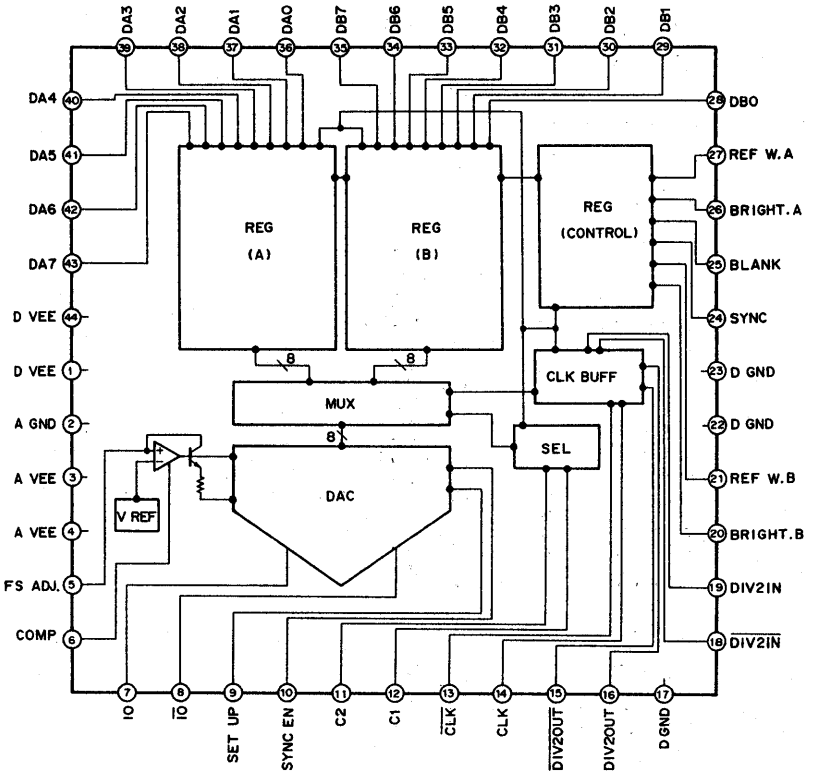
44 pin QFP (Ceramic)



Features

- 500MHz update rate
- 8-bit Multiplexed Inputs
- Sync., Blank, Ref. White and Bright
- 25 Ω/37.5 Ω Load
- I (+), I (−) outputs
- RS-343A Compatible Output
- ECL 100K and 10K Compatible I/O
- −5.5 to −4.2Volt Power Supply

Pin Configuration (Top View)
Block Diagram



AE89677 – ST

Absolute Maximum Ratings (Ta = 25°C)

	Rating	Unit
V_{EE}	−7 to +0.5	V
Input voltage, Digital	V_{EE} to +0.5	V
Input voltage, Reference	V_{EE} to +0.5	V
Output current, I (+), I (−)	50	mA
Storage temperature	−65 to +150	°C

Operating Conditions

Symbol	Item	Min.	Typ.	Max.	Unit
V_{EE}	Supply voltage	−4.2	−5.2	−5.5	V
tpw1	CLK pulse width High	1.0			ns
tpw0	CLK pulse width Low	1.0			ns
ts	Set up time	0.8			ns
th	Hold time	0			ns
V_{IL}	Input voltage logic Low			−1.49	V
V_{IH}	Input voltage logic High	−1.05			V
I_{REF}	Reference current		1.6		mA
Tc	Case temperature	−55		125	°C

Electrical Characteristics (V_{EE} = − 5.2V, Ta = 25°C)

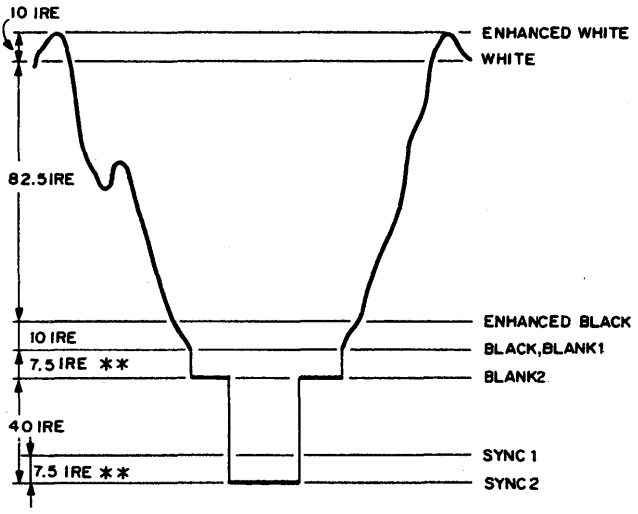
Item	Symbol	Min.	Typ.	Max.	Unit
Supply current	I_{EE}		− 180		mA
Compliance voltage output (+)	Vocp	− 1.2		1.5	V
Compliance voltage output (−)	Vocn	− 1.2		1.5	V
Equiv. output resistance	Ro	50			kΩ
Equiv. output capacitance	Co		10		pF
Max. output current output (+)	Iop	− 44			mA
Max. output current output (−)	Ion	− 44			mA
Input current logic Low	I_{IL}		40		μA
Input current logic High	I_{IH}		40		μA
Max. conversion rate	Fs	500			MHz
CLK to output delay	td		0.8		ns
Current settling time	tset			1.5	ns
Rise time, Current	t_r			0.5	ns
Fall time, Current	t_f			0.5	ns
Integral linearity error	E_{LI}			± 1/2	LSB
Differential linearity error	E_{LD}			± 1/2	LSB
Output offset current	I_{OF}			10	μA
Absolute gain error	E_G			7	% of F.S.
Gain error tempco.	T_{CG}	0			% of F.S./°C
Differential phase	DP			1.0	degree
Differential gain	DG			2.0	%
Glitch energy	GE		1.3		LSB • nsec
CLK delay	D dly			1	ns

Pin Descriptions

<table>
<tr><th>Pin Name</th><th>Description</th></tr>
<tr><td>BLANK</td><td>Control input for blank function. Io and $\overline{Io}$ current outputs are set at blank level when logic "1" is given to the BLANK pin, regardless of data DA0 – DA7, DB0 – DB7, REF W and BRIGHT inputs. (See Table 1.) Io and $\overline{Io}$ are set at reference black level when logic "0" is given to the BLANK pin. The voltage level of the BLANK pin is ECL compatible.</td></tr>
<tr><td>SET UP</td><td>Control input for blank level, ECL compatible. Logic "1" gives blank 1 level and logic "0" or floating level gives blank 2 level to Io and $\overline{Io}$. See Table 1.</td></tr>
<tr><td>SYNC</td><td>Composite sync control input. ECL compatible level.
Logic "1" on this pin gives sync signal to Io and $\overline{Io}$. DA0 – DA7, DB0 – DB7 and any other control input are not overriden.</td></tr>
<tr><td>SYNC EN</td><td>For enabling the sync function. ECL compatible level.</td></tr>
<tr><td>BRIGHT.A
BRIGHT.B</td><td>Bright (overlay) control input. ECL compatible level.
DA0 – DA7, DB0 – DB7 are overriden and outputs Io and $\overline{Io}$ are set at 10% bright level (overlay level) when logic "1" is given to the BRIGHT pin.</td></tr>
<tr><td>REF W.A
REF W.B</td><td>Reference white control input for data A (DA0 – DA7) and data B (DB0 – DB7), respectively. Io and $\overline{Io}$ current outputs are set at reference white level when logic "1" is given to the REF W pin, regardless of data DA0 – DA7, DB0 – DB7. (See Table 1.)</td></tr>
<tr><td>DA0 – DA7
DB0 – DB7</td><td>Two sets of data inputs formated as binary code.
D0 means LSB (least significant bit). ECL compatible voltage level.</td></tr>
<tr><td>CLK
$\overline{CLK}$</td><td>Differential clock inputs with ECL voltage level. The given CLK, $\overline{CLK}$ generate DIV2OUT, $\overline{DIV2OUT}$ signal within the IC.</td></tr>
<tr><td>C1
C2</td><td>Output mode control inputs for selecting "multiplex mode" or "data select mode".
The "multiplex mode" multiplexes the two sets of data DA0 – DA7 and DB0 – DB7, and gives out corresponding analog data updated twice as fast as the DA0 – DA7 and DB0 – DB7 run. See Fig. 2 and 3.
The max. frequency of available output is 500Mbit/sec when the max. update rate is 250Mbit/sec for DA0 – DA7 and DB0 – DB7.
The "data select mode" chooses either DA0 – DA7 or DB0 – DB7, and converts it into analog. See Fig. 4.
The max. frequency of available output is 250Mbit/sec with DA0 – DA7 or DB0 – DB7 running at max. 250Mbit/sec each.
<table>
<tr><th>C1</th><th>C2</th><th colspan="2">MODE</th><th>CLK IN (MHz)</th><th>DATA IN (Mbps)</th><th>OUT (Mbps)</th></tr>
<tr><td>0</td><td>0</td><td rowspan="2">MUX</td><td>(1)</td><td>500</td><td>250</td><td>500</td></tr>
<tr><td>0</td><td>1</td><td>(2)</td><td>250*</td><td>250</td><td>500</td></tr>
<tr><td>1</td><td>0</td><td colspan="2">A</td><td>250</td><td>250</td><td>250</td></tr>
<tr><td>1</td><td>1</td><td colspan="2">B</td><td>250</td><td>250</td><td>250</td></tr>
</table>
* CLK duty has to be 50%
A : DA0 – DA7 is selected.
B : DB0 – DB7 is selected.</td></tr>
</table>

Pin Name	Description
DIV2OUT $\overline{\text{DIV2OUT}}$	Differential ECL compatible outputs. In case of "multiplex mode (1)", these output pins provide a clock output having half the speed of CLK and $\overline{\text{CLK}}$. When CLK and $\overline{\text{CLK}}$ are 500MHz, DIV2OUT and $\overline{\text{DIV2OUT}}$ are 250MHz. See Fig. 2. If $\overline{\text{DIV2OUT}}$ pin is connected with DIV2IN pin, as illustrated is Fig. 6, 500Mbit/sec analog data can be obtained. In case of "multiplex mode (2)", the frequency of DIV2OUT and $\overline{\text{DIV2OUT}}$ is the same as that of CLK and $\overline{\text{CLK}}$, as long as the CLK duty cycle is 50%. See Fig. 3. In case of "data select mode", the frequency of DIV2OUT and $\overline{\text{DIV2OUT}}$ is the same as that of CLK and $\overline{\text{CLK}}$. $\overline{\text{DIV2OUT}}$ pin need not be connected. See Fig. 4 and Fig. 6. DIV2OUT and $\overline{\text{DIV2OUT}}$ latch DA0 – DA7, DB0 – DB7, SYNC and BLANK input. (See Fig. 2, 3 and 4.) These signals can also be used for system clock to be provided to other peripheral portion of the system.
DIV2IN $\overline{\text{DIV2IN}}$	Differential ECL compatible inputs. DIV2IN should be connected to $\overline{\text{DIV2OUT}}$ pin in case of "multiplex mode". Refer to the description "DIV2OUT, $\overline{\text{DIV2OUT}}$".
Io $\overline{\text{Io}}$	Differential current outputs. These are capable of directly driving either 25 Ω or 37.5 Ω load.
FS ADJ.	Control pin to adjust Io, $\overline{\text{Io}}$ fullscale level. The scale is set by a resistor (Rset) connected between this pin and AGND. The relation between Rset and R_L which is current output load is the following : $\text{Rset} = 1.24\text{V} / ((661\text{mV}/R_L) \times (16/255))\ \Omega$
COMP	Compensation output pin for internal reference amplifier.

$\overline{IO}$ (mA) *	(mV)
0	0
− 2.84	− 71
− 26.44	− 661
− 29.28	− 732
− 31.42	− 785.5
− 40.7	− 1017.5
− 42.84	− 1071



* In case of doubly-terminated 50 Ω load

** 7.5 IRE difference·····Available when SETUP pin is floating or "0" level, not available when SETUP pin is "1" level.

Fig. 1. Composite Video Level

Description	$\overline{IO}$ (mA)	SETUP	SYNC EN	BRIGHT	SYNC	BLANK	REF W	Input DATA
Enhanced White	0	×	×	1	0	0	0	11111111
	0	×	×	1	0	0	1	XXXXXXXX
White	− 2.84	×	×	0	0	0	1	XXXXXXXX
	− 2.84	×	×	0	0	0	0	11111111
Enhanced DATA	DATA	×	×	1	0	0	0	DATA
DATA	DATA − 2.84	×	×	0	0	0	0	DATA
Enhanced BLACK	− 26.44	×	×	1	0	0	0	00000000
BLACK, BLANK1	− 29.28	×	×	0	0	0	0	00000000
	− 29.28	1	×	×	0	1	×	XXXXXXXX
	− 29.28	1	1	×	1	×	×	XXXXXXXX
BLANK2	− 31.42	0	×	×	0	1	×	XXXXXXXX
	− 31.42	0	1	×	1	×	×	XXXXXXXX
SYNC1	− 40.7	1	0	×	1	×	×	XXXXXXXX
SYNC2	− 42.84	0	0	×	1	×	×	XXXXXXXX

Table 1. Video Output Truth Table

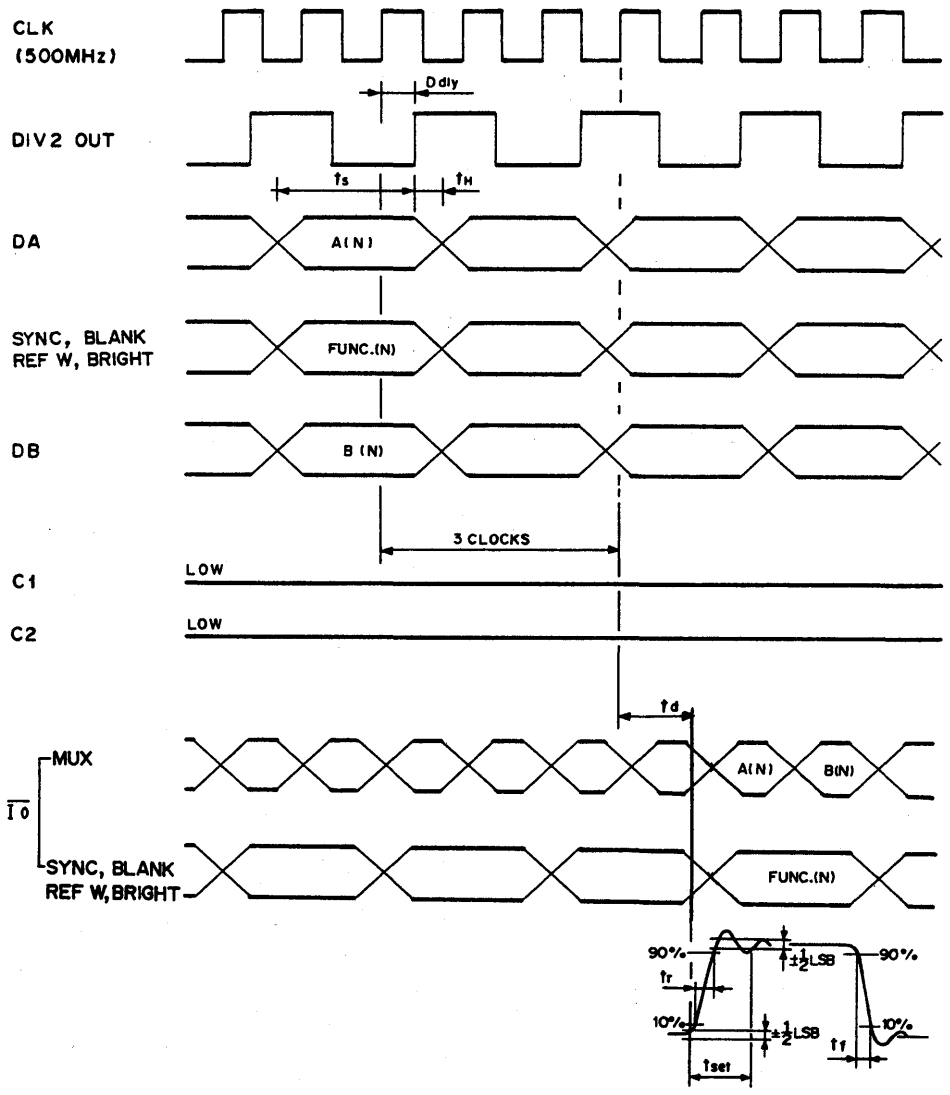


Fig. 2. Timing Diagram – MUX MODE (1)

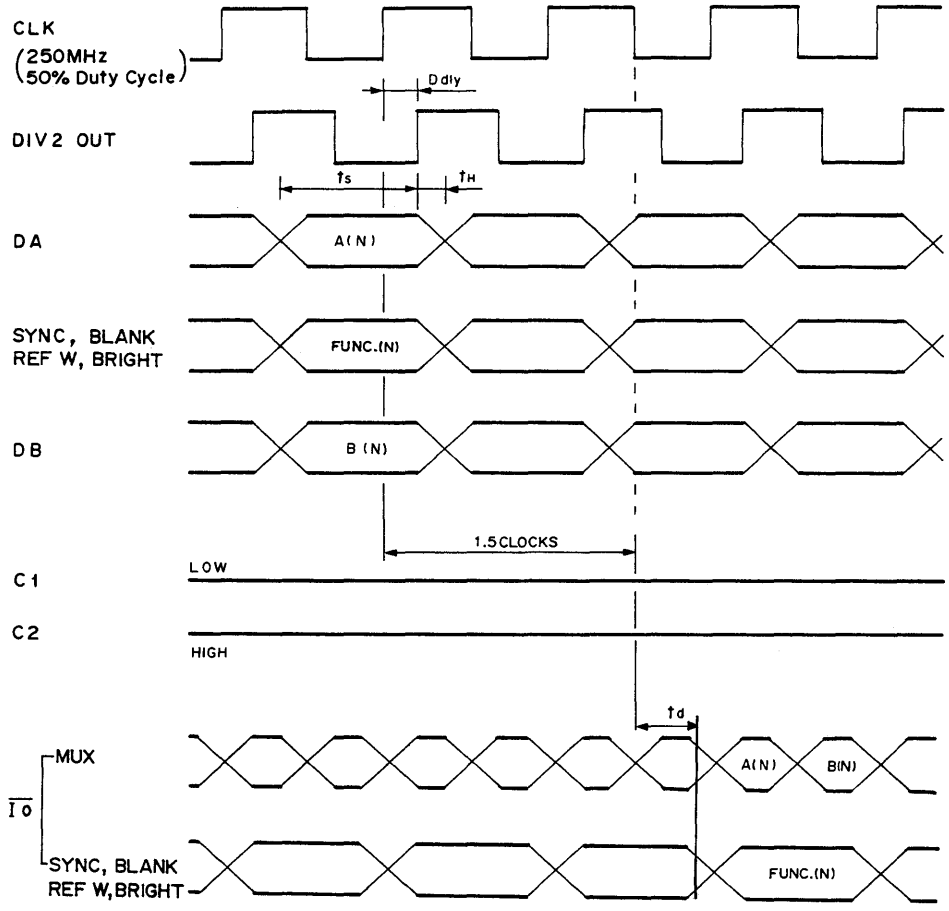


Fig. 3. Timing Diagram – MUX MODE (2)

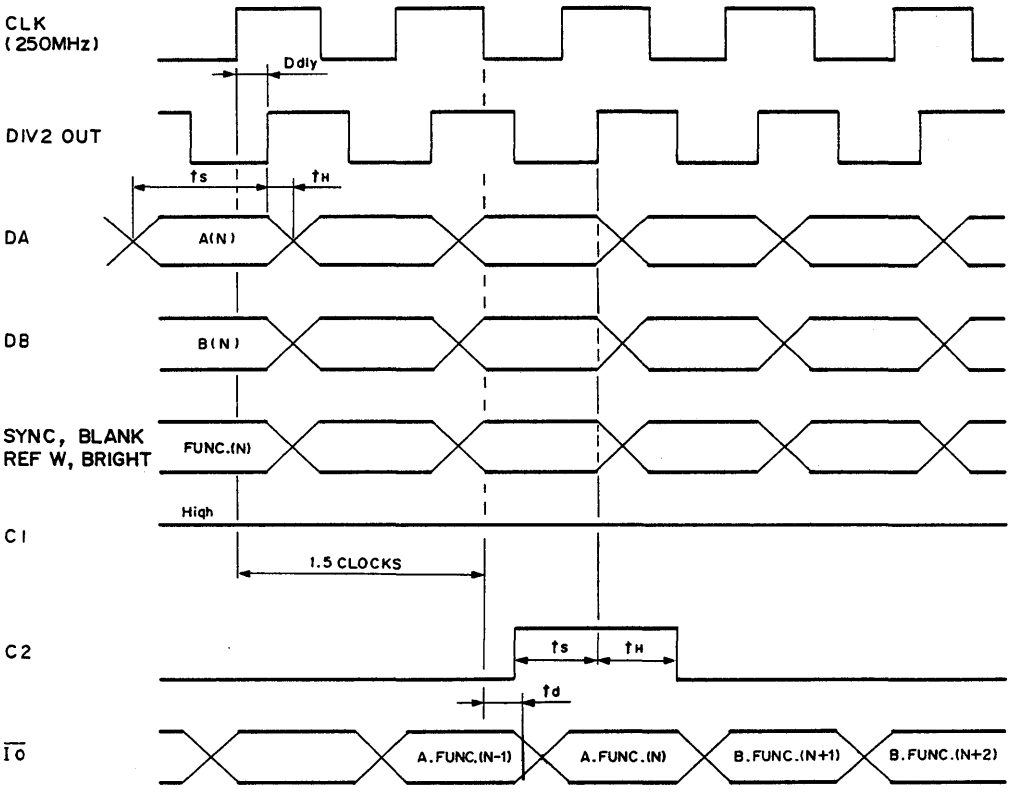
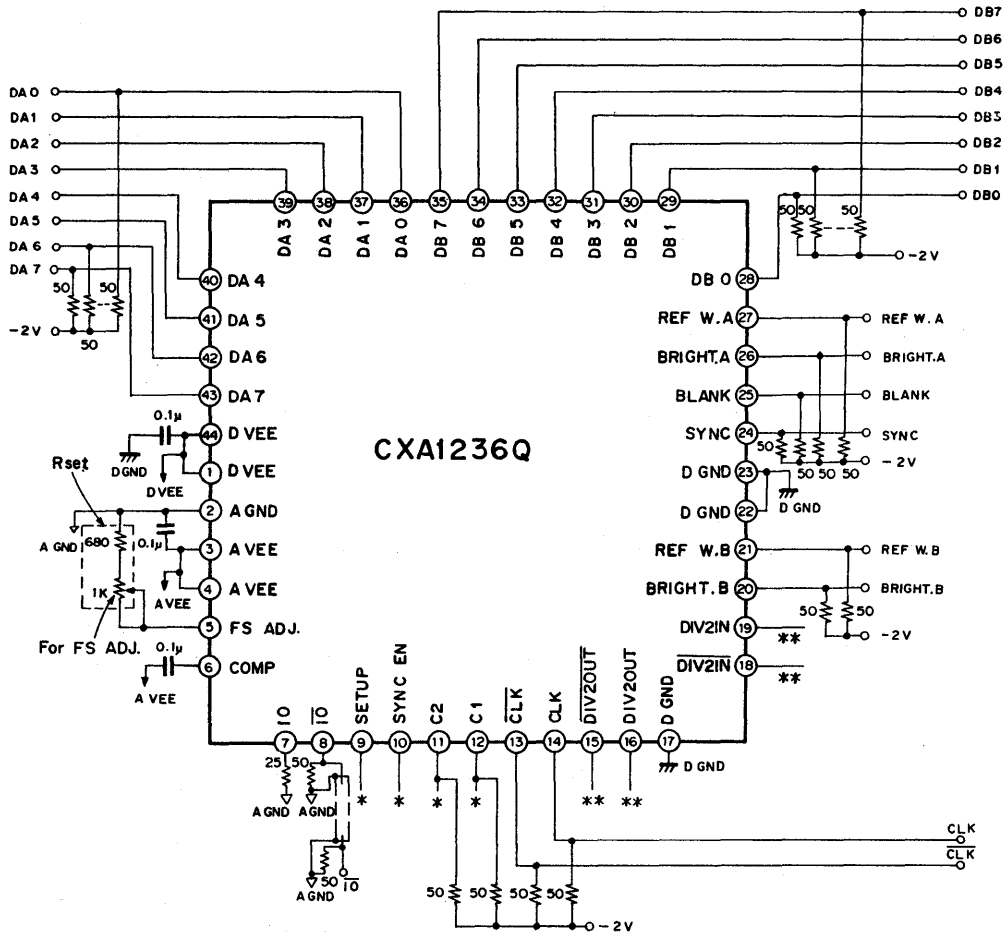


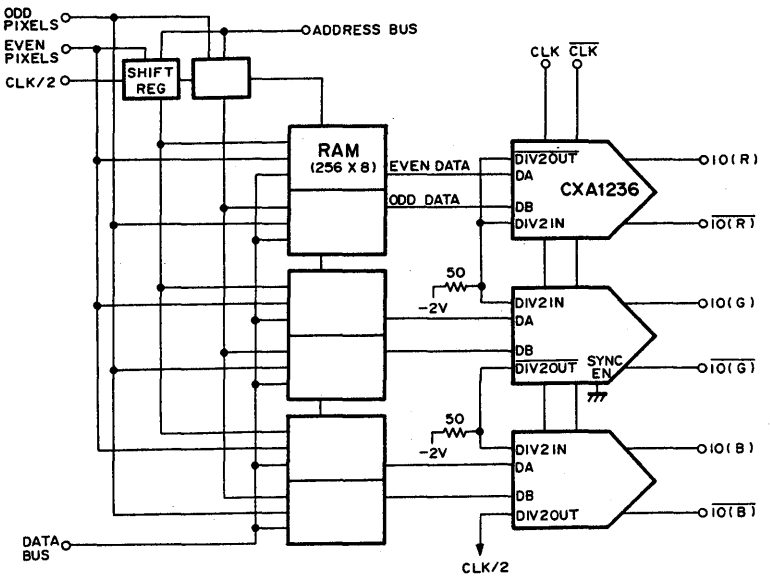
Fig. 4. Timing Diagram – SELECT MODE



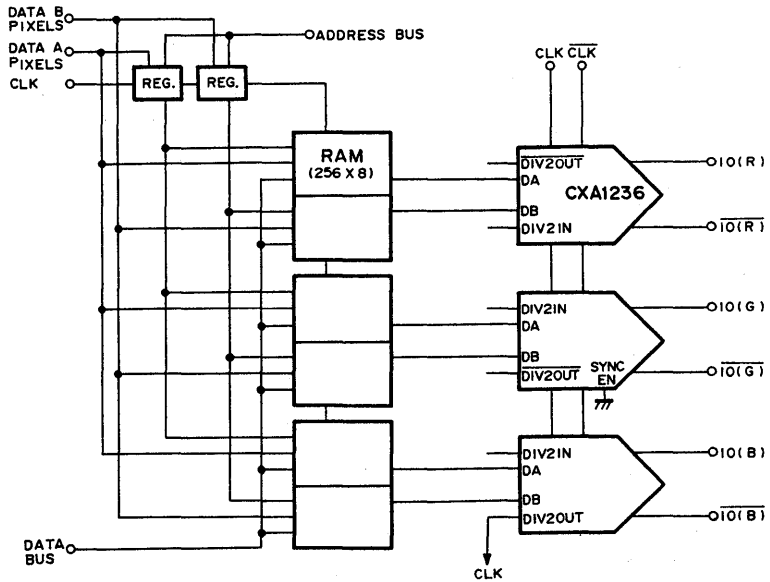
* See the page for pin description

** See the page for pin description and typical application (Fig. 6)

Fig. 5. Circuit Connection



(1) MUX MODE

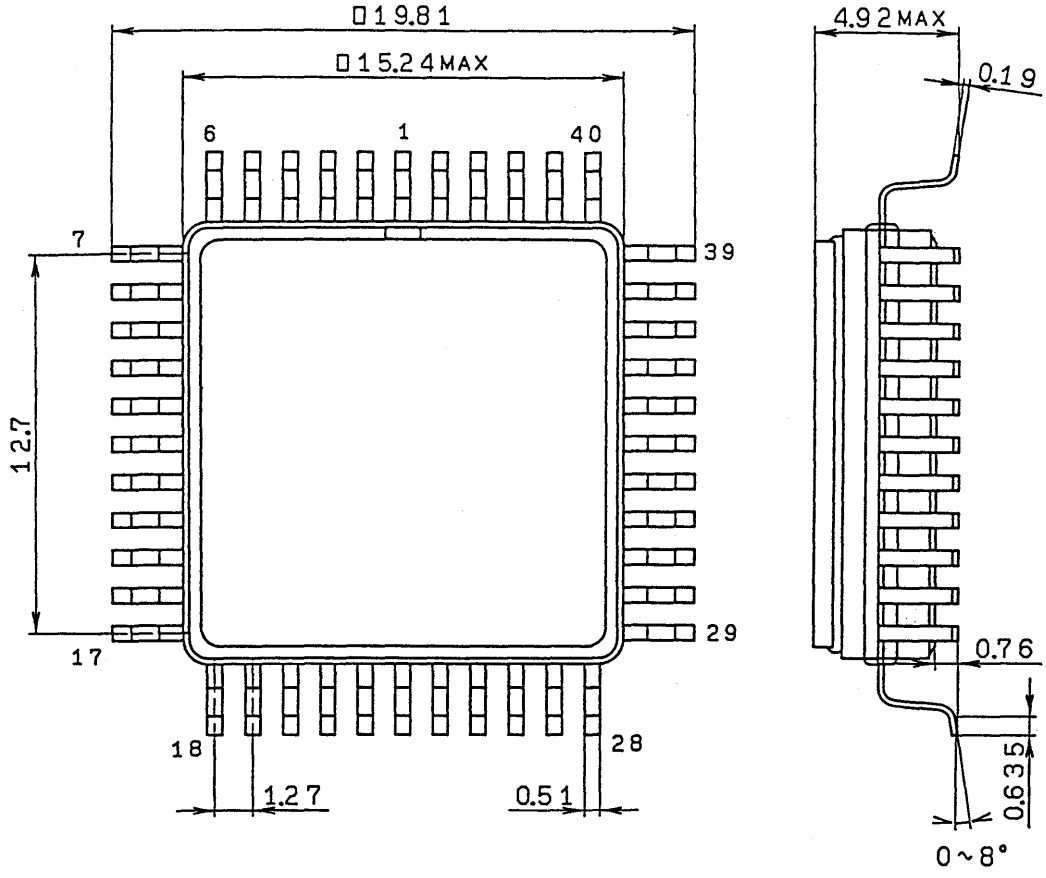


(2) SELECT MODE

Fig. 6. Typical Application

Package Outline Unit : mm

CXA1236Q 44 pin QFP (Ceramic) 50mil



QFP-44C-L01

SONY

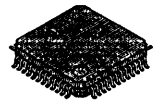
CXA1260Q-Z

8 bit 35 MSPS RGB 3-Channel D/A Converter

Description

CXA1260Q-Z is an 8-bit high-speed D/A converter for video band use. It has an output/input equivalent to 3 channels of R, G and B. It is suitable for use of digital TV, graphic display, etc.

48 pin QFP (Plastic)



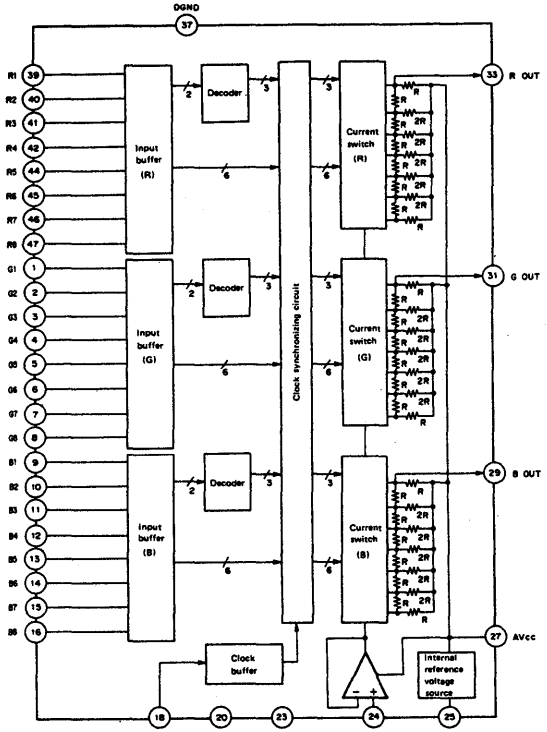
Features

- Resolution: 8-bits
- Maximum conversion speed: 35MSPS
- RGB 3-channel input/output
- Differential linearity error: ±1/2LSB
- Digital input voltage: TTL level
- Output voltage full-scale: 1 Vp-p (typ)
- Low power consumption: 360 mW (typ)
- +5V single power supply

Structure

Bipolar silicon monolithic IC

Block Diagram



E89648-ST

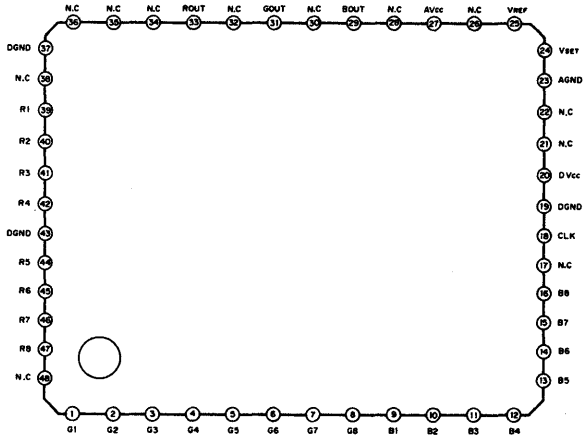
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	0 to 7	V
• Input voltage (digital)	V_I	−0.3 to V_{CC}	V
	V_{CLK}	−0.3 to V_{CC}	V
• Input voltage (V_{SET} pin)	V_{SET}	−0.3 to V_{CC}	V
• Output voltage (analog)	V_{OUT}	V_{CC}−2.1 to V_{CC}	V
• Output current (analog)	I_{OUT}	−3 to +10	mA
(V_{REF} pin)	I_{REF}	−5 to 0	mA
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	0.7	W

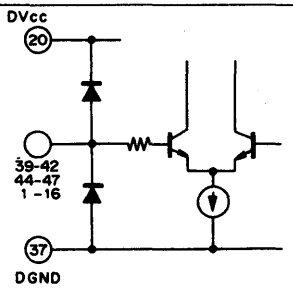
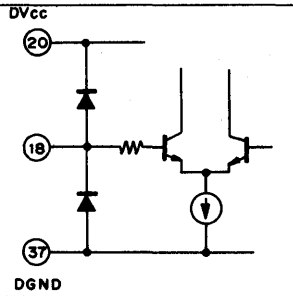
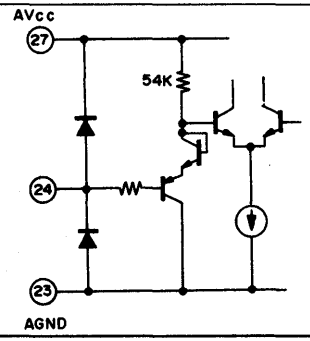
Recommended Operating Conditions

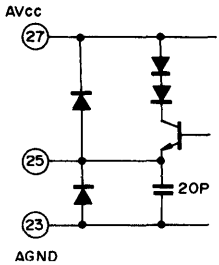
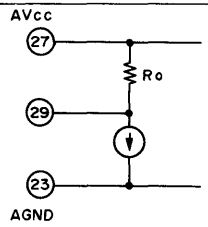
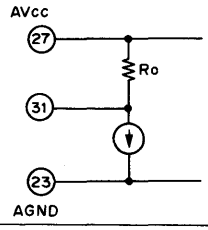
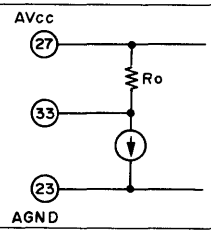
• Supply voltage	AVcc, DVcc	4.5 to 5.5	V
	AVcc–DVcc	−0.2 to +0.2	V
	AGND–DGND	−0.05 to +0.05	V
• Digital input voltage H level	VIH, V_{CLKH}	2.0 to DVcc	V
L level	VIL, V_{CLKL}	DGND to 0.8	V
• V_{SET} input voltage	V_{SET}	0.7 to 1.0	V
• V_{REF} pin current	I_{REF}	−3 to −0.4	mA
• Clock pulse width	T_{pw1}	15	ns
	T_{pw0}	10	ns

Pin Configuration (Top View)



Pin Description

No.	Symbol	Equivalent circuit	Description
39 to 42 44 to 47 1 to 16	R1 to R8 G1 to G8 B1 to B8		Digital input pin. From pins 39 to 42 and from 44 to 47 are for RED. R1 is MSB and R8 is LSB. From pins 1 to 8 are for GREEN. G1 is MSB and G8 is LSB. From pins 9 to 16 are for BLUE. B1 is MSB and B8 is LSB.
18	CLK		Clock input pin.
20	DVcc		Digital Vcc.
17 21 to 22	NC		Vacant pin (non-connection)
23	AGND		Analog GND.
24	VSET		Bias input pin. Normally, apply 0.87V. See "Note on use".

No.	Symbol	Equivalent circuit	Description
25	VREF		Internal reference voltage out-put pin 1.2V (typ) A pull-down resistance is necessary externally. See "Note on use".
26	NC		Vacant pin (non-connection)
27	AVcc		Analog Vcc
28	NC		Vacant pin but connect to AVcc*
29	BOUT		Analog output pin for BLUE.
30	NC		Vacant pin but connect to AVcc*
31	GOUT		Analog output pin for GREEN.
32	NC		Vacant pin but connect to AVcc*
33	ROUT		Analog output pin for RED.
34 to 36	NC		Vacant pin but connect to AVcc*
19 37 43	DGND		Digital GND
48	NC		Vacant pin (non-connection)

***Note)** Pins 30, 32, 34 and 36 are vacant, but in order to reduce interference between the individual RGB outputs, connect them to AVcc.

Electrical Characteristics Ta=25°C, AVcc=DVcc=5.0V, AGND=DGND=0.0V

Item			Symbol	Test condition	Min.	Typ.	Max.	Unit
Resolution			RSL			8		bit
Monotony			MNT			Guara-ntee		
Differential linearity error			DLE	VSET−AGND=0.87V RL>10kΩ F.S.=Full-scale	−0.5		+0.5	LSB
Integral linearity error			ILE		−0.4		+0.4	% of F.S.
Maximum conversion speed			fMAX	VSET−AGND=0.87V RL>10kΩ CL<20pF	35			MSPS
Full-scale output voltage*1			VOFS		0.85	1.0	1.15	Vp-p
RGB output voltage full-scale ratio*2			FSR		0	4	8	%
Output zero offset voltage			Voffset		−40	−6	0	mV
Output resistance			RO		270	340	420	Ω
Consumption current			ID	VSET−AGND=0.87V RL>10kΩ IREF=−400μA	54	72	90	mA
Digital data input current	H level	Upper 2 bits	IIH(U)	VI=DVcc		1.2	20	μA
		Lower 6 bits	IIH(L)			0.6	10	μA
	L level	Upper 2 bits	IIL(U)	VI=DGND	−10	0	10	μA
		Lower 6 bits	IIL(L)		−10	0	10	μA
Clock input current	H level		ICLKH	VCLK=DVcc		3	30	μA
	L level		ICLKL	VCLK=DGND	−10	0	10	μA
VSET input current			ISET	VSET−AGND=0.87V	−5	−0.3	0	μA
Internal reference voltage			VREF	IREF=−400μA	1.08	1.20	1.32	V
Set-up time			ts		12			ns
Hold time			th		3			ns

Note) *1. AVcc−Vo

*2. Maximum value among

$$100 \times \left|\frac{V_{OFS(R)}}{V_{OFS(G)}} - 1\right|, \quad 100 \times \left|\frac{V_{OFS(G)}}{V_{OFS(B)}} - 1\right|, \text{ or } 100 \times \left|\frac{V_{OFS(B)}}{V_{OFS(R)}} - 1\right|$$

Input corresponding table

Input code	Output voltage
MSB LSB	
1 1 1 1 1 1 1 1	Vcc+Voffset
.	.
.	.
.	.
1 0 0 0 0 0 0 0	Vcc+Voffset−0.5V
.	.
.	.
.	.
0 0 0 0 0 0 0 0	Vcc+Voffset−1.0V

In case the output voltage full-scale is 1.00V. (1LSB=3.92 mV)

Standard Circuit Design Data Ta=25°C, AVcc=DVcc=5.0V, AGND=DGND=0.0V

Item	Symbol	Measuring condition	Min.	Typ.	Max.	Unit
Crosstalk among R, G and B	CT	D/A OUT: 1Vp-p RL>10kΩ CL<20pF fDATA=7MHz fCLK=14MHz See Fig.2		−40	−35	dB
Glitch energy	GE	VSET−AGND=0.87V RL>10kΩ fCLK=1MHz Digital ramp output See Fig.3*1		30		pV-s
Rise time*2	tr	VSET−AGND=0.87V See Fig. 1.		5.5		ns
Fall time*2	tf			5.0		ns
Settling time	tset			16		ns

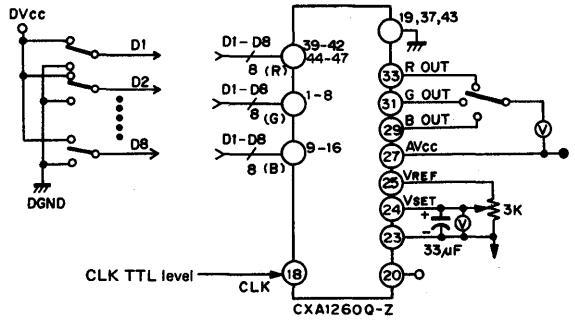
Note) *1. Observe the glitch which is generated when the digital input varies as follows:

0 0 1 1 1 1 1 1 — 0 1 0 0 0 0 0 0
0 1 1 1 1 1 1 1 — 1 0 0 0 0 0 0 0
1 0 1 1 1 1 1 1 — 1 1 0 0 0 0 0 0

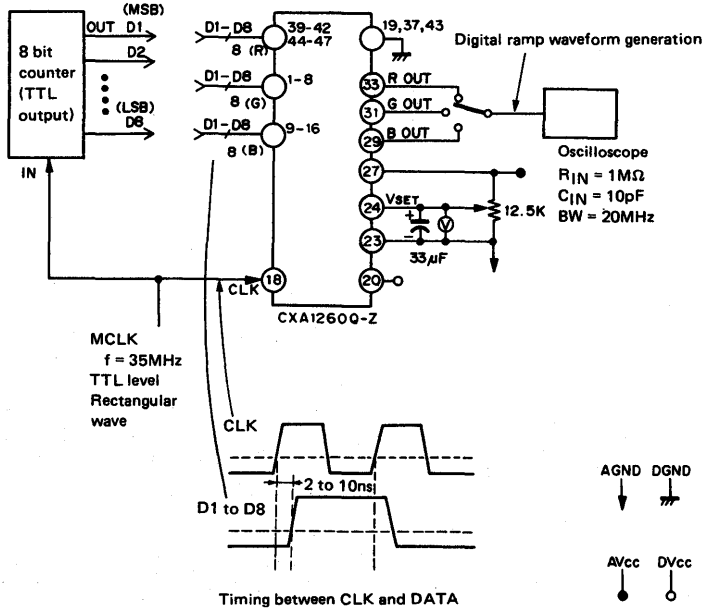
*2. The time required for the D/A OUT to arrive at 90% of its final value from 10%.
See p. 204, for the definition of "Rise, Fall and Settling time".

Electrical Characteristics Test Circuit

Differential linearity and integral linearity test circuits



Maximum conversion speed test circuit



Output voltage full-scale precision, RGB output voltage full-scale ratio, and output zero offset voltage test circuits

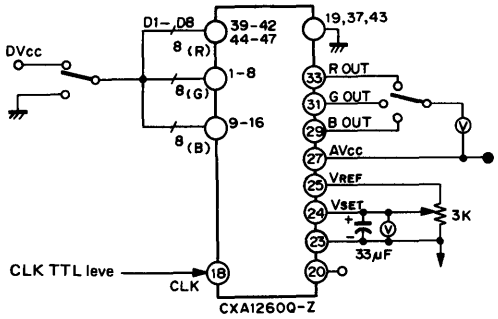
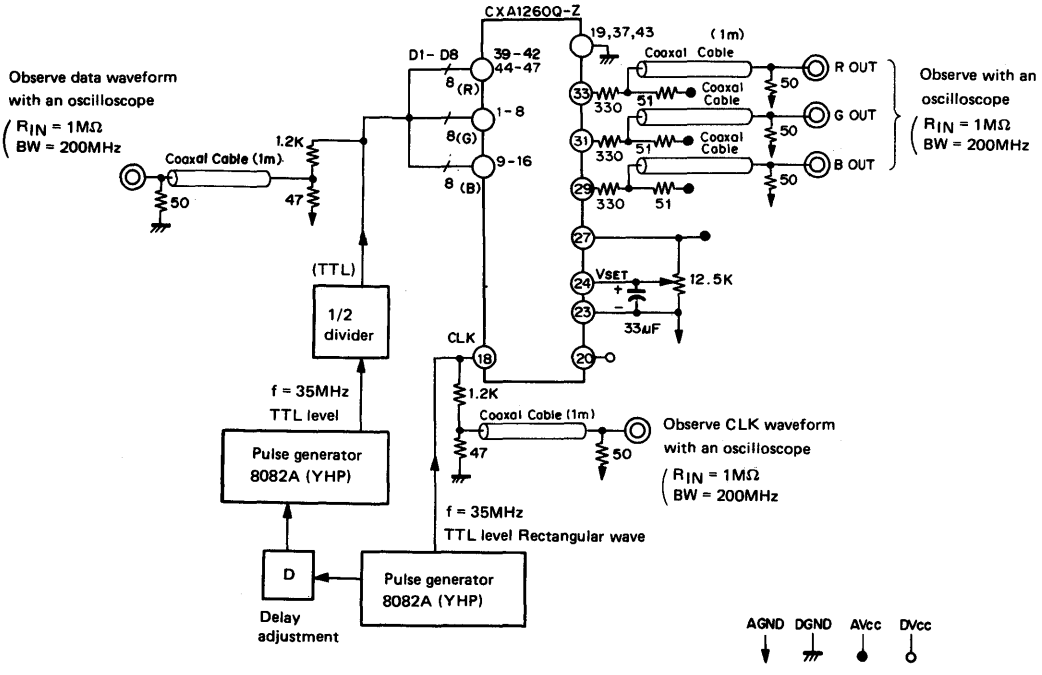


Fig. 1

Set-up time, hold time, and rise and fall time test circuits



Standard Circuit Design Data Test Circuit

Crosstalk among R, G and B test circuit

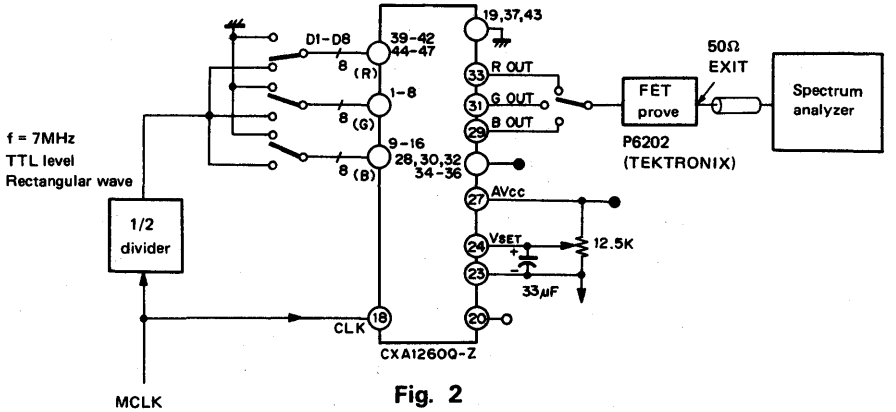
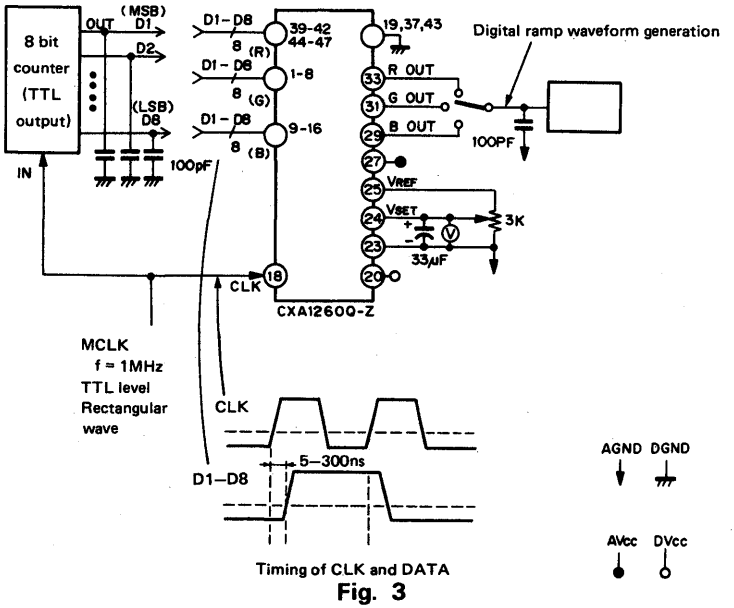


Fig. 2

[Measuring method]
In case the measuring crosstalk of G → R

1 Apply the data to G only and measure the power of the frequency component of the data at R OUT.
2 Apply the data to R only and measure the power of the frequency component of the data at R OUT.
3 Take the difference of the above two powers. The unit is in dB.

Glitch energy test circuit

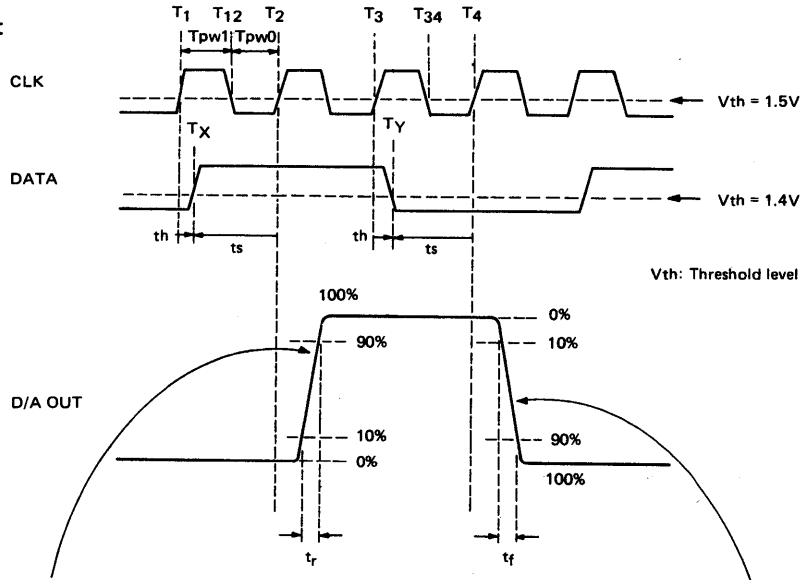


Timing of CLK and DATA

Fig. 3

Operation Description

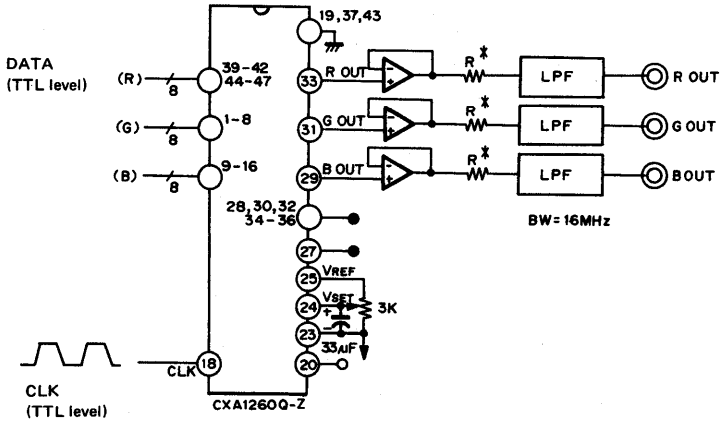
Timing chart



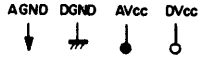
At the time t = T_X, the data of individual bits are switched and thereafter when the CLK becomes L → H at t = T_2, the D/A OUT is varied synchronous with it. That is, the D/A OUT is synchronous with the rise of the CLK.
(In this case, fetching of the data is carried out at the fall of the CLK (at the time when t = T_{12})).

At the time t = T_Y, the data of individual bits are switched and thereafter when the CLK becomes L → H at t = T_4, the D/A OUT is varied synchronous with it. That is, the D/A OUT is synchronous with the rise of the CLK.
(In this case, fetching of the data is carried out at the fall of the CLK (at the time when t = T_{34})).

Application Circuit

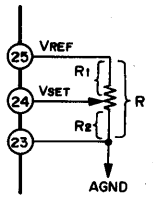


R* is matching resistance for LPF



Note on Use

1. Setting of pin 24 (V_{SET})
   The full-scale of the D/A output voltage changes by applying voltage to pin 24 (V_{SET}). When load is connected to pin 25 (V_{REF}), DC volatage of 1.2V is issued and the said voltage is dropped to 0.87V by resistance division.
   When the 0.87V is applied to pin 24 (V_{SET}), the D/A output of 1 Vp-p can be obtained.
   (Example of use)



   Adjustment method
   1) The resistance R is determined in accordance with the recommended operating condition of I_{REF} (Current flowing through resistance R).
      See R vs. I_{REF} of Fig. 4. The calculation expression is as follows:
      $R = V_{REF}/I_{REF}$
   2) Adjust the volume so that the RGB output voltage full-scale becomes 1.0V.
      (At this point, it becomes R1:R2=2:5)

Resistance vs. V_{REF} pin current

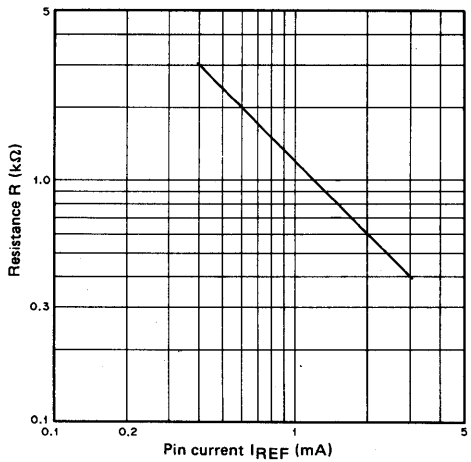


Fig. 4

2. Phase relationship between data and clock
   In order to obtain the desired characteristics as a D/A converter, it is necessary to set the phase relationship correctly between the externally applied data and clock.
   Satisfy the standard of the set-up time (ts) and hold time (th) indicated in the electrical characteristics. As to the meaning of ts and th, see the timing chart.
   Moreover, the clock pulse width is desired to be as indicated in the recommended operating condition.

3. Regarding the load of D/A output pin
Receive the D/A output of the next stage with high impedance. In other words, perform so that it becomes as follows:

$R_L > 10\ k\Omega$

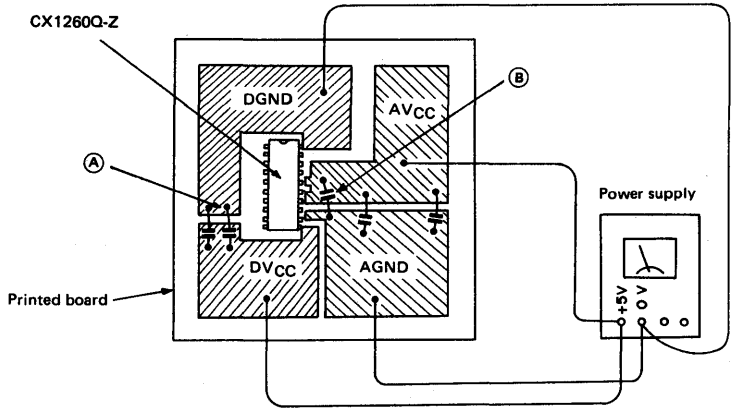
$C_L < 20\ pF$

The temperature characteristics indicated in the characteristics diagram has been measured under this condition.

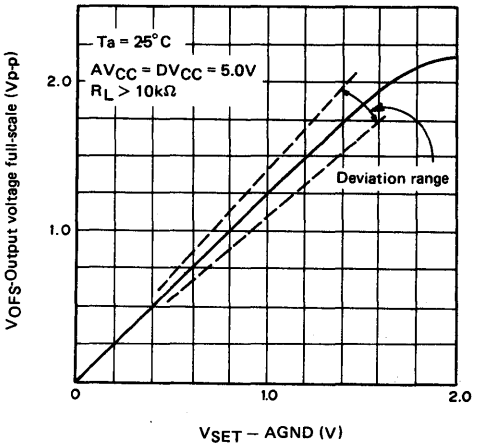
However, when it is made to $R_L \leqq 10\ k\Omega$ the temperature characteristics may change considerably. In addition, when it is made to $C_L \geqq 20$ pF, the rise and fall of the D/A output become slow and will not operate at high speed.

4. Noise reduction measures
As the D/A output voltage is a minute voltage of approximately 4 mV per one step, ingenuity is required in reducing the noise entering from the outside of the IC as much as possible. Therefore use the items given below as reference.

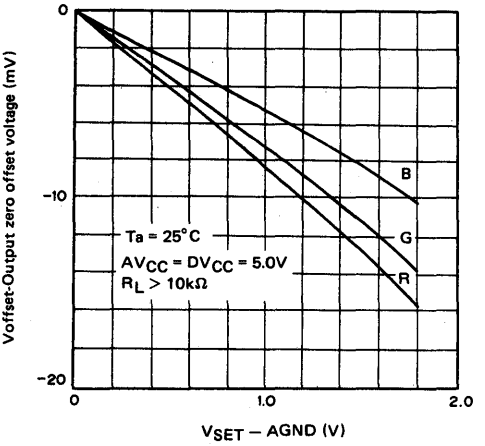
- When mounting onto the printed board, allow as much space as possible to the ground surface and the Vcc surface on the board and reduce the parasitic inductance and resistance.
- It is desirable that the AGND and DGND be separated in the pattern on the board. It is similar with AVcc and DVcc. As shown in the diagram below, for example, it is recommended that the wiring to the electric supply of AGND and DGND as also AVcc and DVcc be conducted separately, and then making AGND and DGND as also AVcc and DVcc in common right near the power supply respectively.
- Insert in parallel a 47 μF tantalum capacitor and a 1000 pF ceramic capacitor between the Vcc surface on the printed board and the nearmost ground surface. (A of diagram below). It is also desirable to insert the above between the Vcc surface near the pin of the IC and the ground surface. (B of diagram below). They are bypass capacitors to prevent bad effects from occurring to the characteristics when the power supply voltage fluctuates due to the clock, etc.
- It is recommended to reduce noise which overlaps the D/A output by inserting a capacitor of over 0.1 μF between pin 23 (AGND) and pin 24 (VSET).



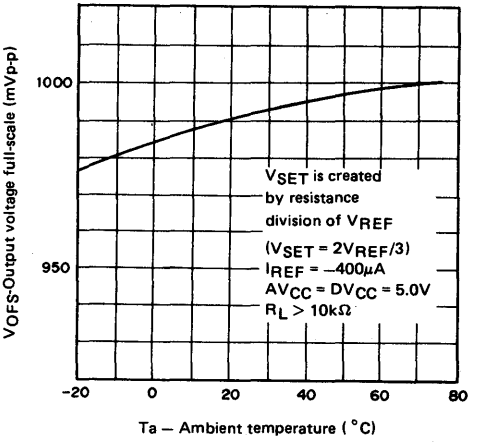
Output voltage full-scale vs. V_{SET}—AGND



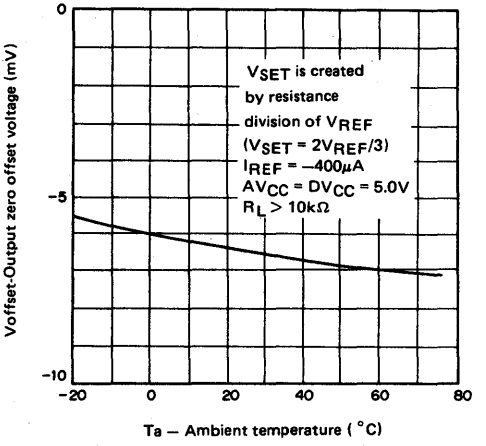
Output zero offset voltage vs. V_{SET}—AGND



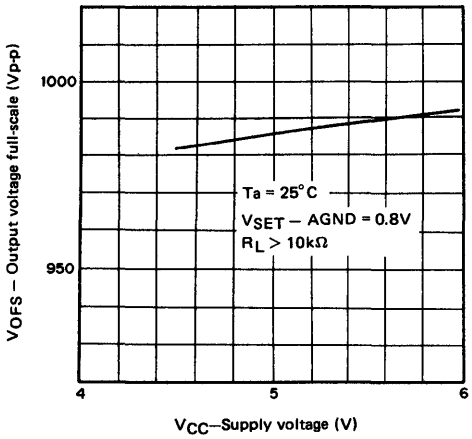
Output voltage full-scale vs. Ambient temperature



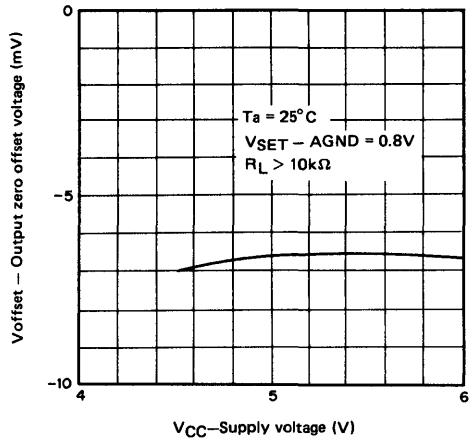
Output zero offset voltage vs. Ambient temperature



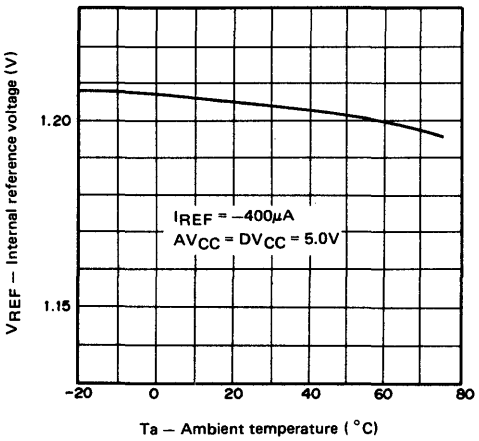
Output voltage full-scale vs. Supply voltage



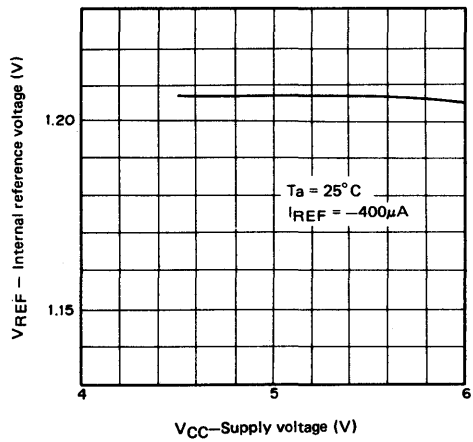
Output zero offset voltage vs. Supply voltage



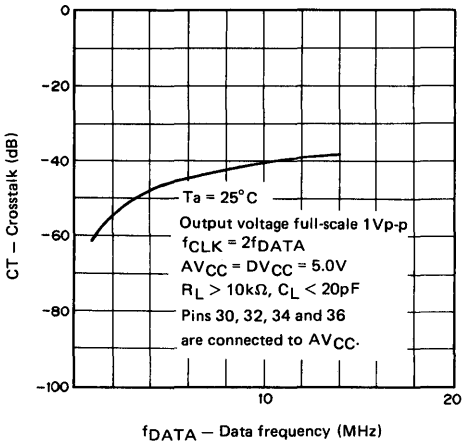
Internal reference voltage vs. Ambient temperature



Internal reference voltage vs. Supply voltage

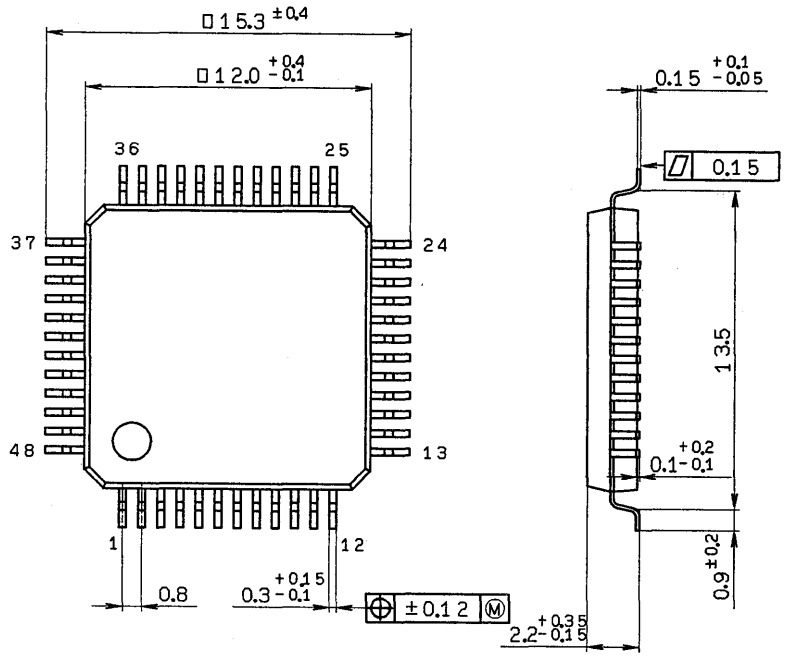


Crosstalk among R, G and B vs. Data frequency



Package Outline **Unit: mm**

48 pin QFP (Plastic) 0.6g



QFP-48P-L04

SONY

CXD1170M

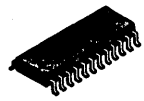
6-bit 40 MSPS D/A Converter (CMOS)

Advance Information

Feature

- Resolution 6-bit ± 1/2 LSB
- Low glitch energy
- TTL/CMOS compatible input
- + 5V single power supply
- Low power consumption : 70mW
- Chip enable/blank function

24 pin SOP (Plastic)



Application

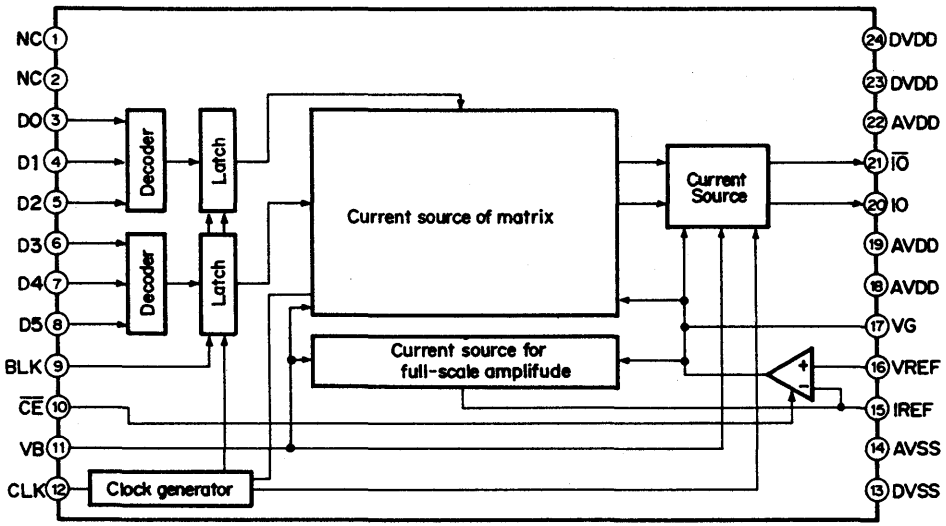
- Graphic display
- Digital TV, VCR
- Fax machine
- Camcoder

Absolute Maximum Ratings (Ta = 25℃)

• Supply voltage	V_{DD}	7	V
• Digital input voltage	V_{IN}	V_{DD} to Vss	V
• Analog output current	I_{OUT}	0 to 15	mA
• Operating temperature	Topr	− 20 to + 75	℃
• Storage temperature	Tstg	− 55 to + 150	℃

Sample Available	4Q89
Production Start	1Q90

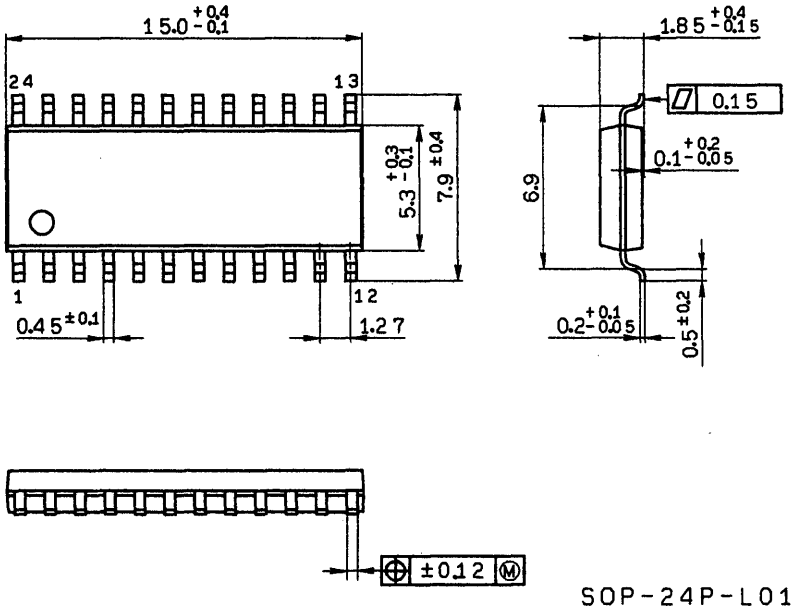
Block Diagram



AE89655A98 – ST

Package Outline Unit : mm

24 pin SOP (Plastic) 300mil 0.3g



SOP-24P-L01

SONY

CXD1171M

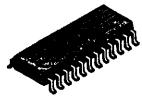
8-bit 40 MSPS D/A Converter (CMOS)

Advance Information

Feature

- Resolution 8-bit ± 1/2 LSB
- Low glitch energy
- TTL/CMOS compatible input
- + 5V single power supply
- Low power consumption : 70mW
- Chip enable/blank function

24 pin SOP (Plastic)



Application

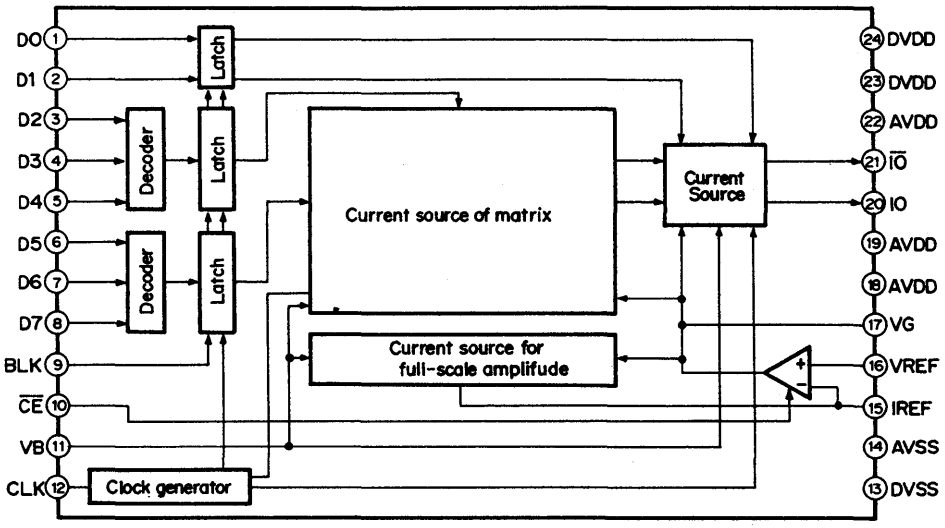
- Graphic display
- Digital TV, VCR
- Fax machine
- Camcoder

Absolute Maximum Ratings (Ta = 25℃)

• Supply voltage	V_{DD}	7	V
• Digital input voltage	V_{IN}	V_{DD} to Vss	V
• Analog output current	I_{OUT}	0 to 15	mA
• Operating temperature	Topr	− 20 to + 75	℃
• Storage temperature	Tstg	− 55 to + 150	℃

Sample Available	4Q89
Production Start	1Q90

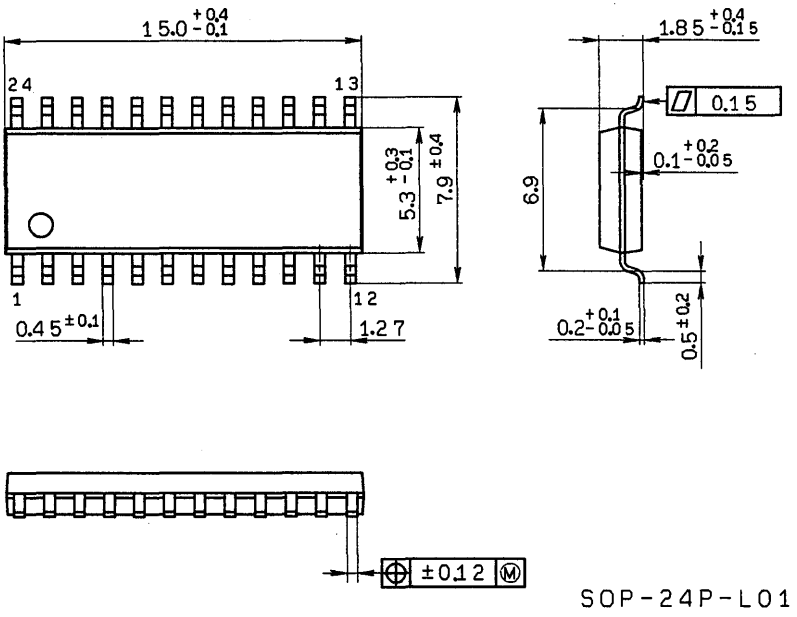
Block Diagram



AE89665A98 – ST

Package Outline Unit : mm

24 pin SOP (Plastic) 300mil 0.3g



SOP-24P-L01

High Speed Sample & Hold Amplifier

5

3. High Speed Sample & Hold Amplifier

Type	Function	Page
CXA1008P/1009P	High Speed Sample and Hold Amplifier	285

SONY CXA1008P/1009P

High-speed Sample and Hold Amplifiers

Evaluation Board Available — CX20052A PCB-3A for CXA1008P
CX20052A PCB-3B for CXA1009P

Description

CXA1008P/1009P are bipolar IC's developed for the purpose of sample holding video signals and other signals at high-speed.

Features

- Maximum sampling frequency
  - CXA1008P: 35 MHz
  - CXA1009P: 18 MHz
- Linearity: 0.08% (Typ.)
- Clock input level: ECL compatible
- Low power consumption
  - CXA1008P: 680 mW (Typ.)
  - CXA1009P: 420 mW (Typ.)

Structure

Bipolar silicon monolithic IC.

Applications

- A/D converter and other analog signal processing
- Other general applications.

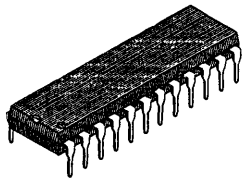
Absolute Maximum Ratings ($T_a = 25°C$)

• Supply voltage	V_{CC}	+5.5	V
	V_{EE}	−6.0	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−55 to +150	°C
• Allowable power dissipation	P_D	1.2	W

Recommended Operating Conditions

• Supply voltage	V_{CC}	+4.75 to 5.25V
	V_{EE}	−4.75 to −5.45V

24pin DIP(Plastic)



Function

High-speed hold circuit, wide band 6 dB amplifier, A/D reference power supply, A/D clock output circuit.

Block Diagram

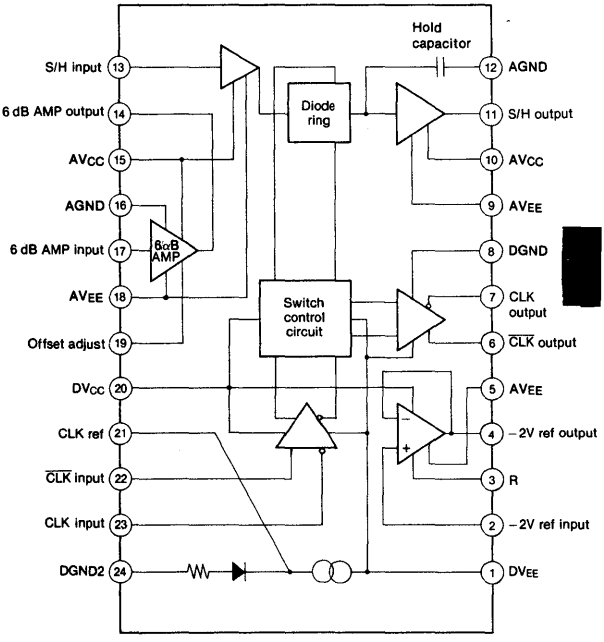
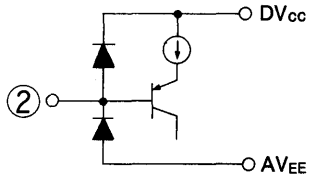
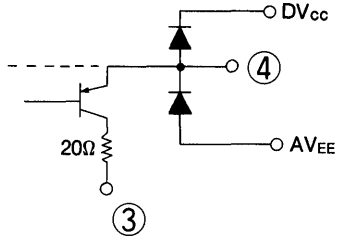
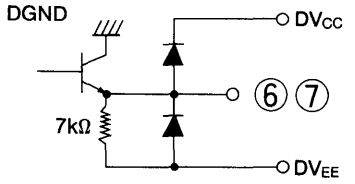
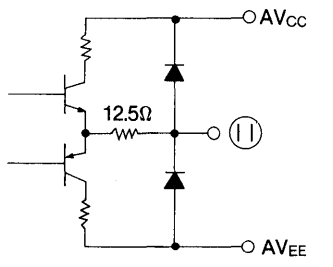
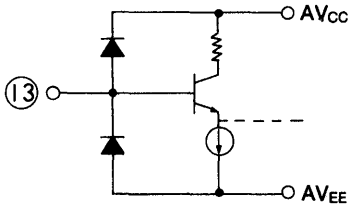
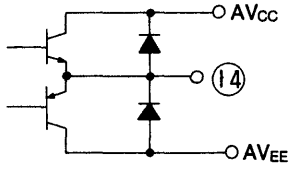
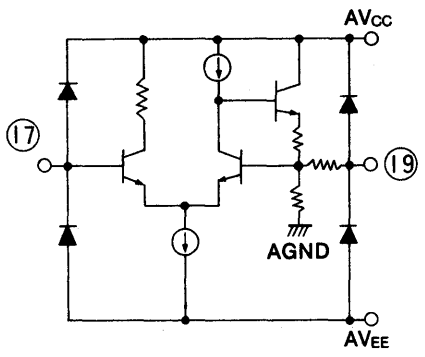
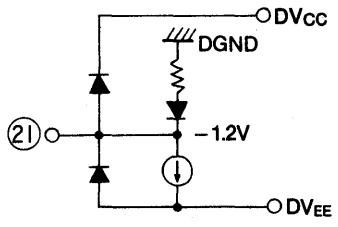


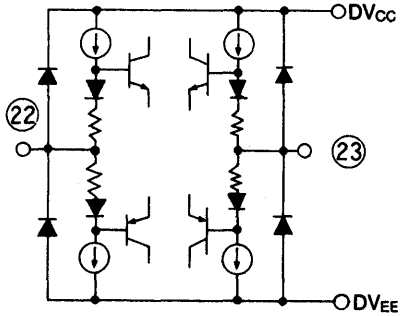
Fig. 1

E89641-HP

Pin Description

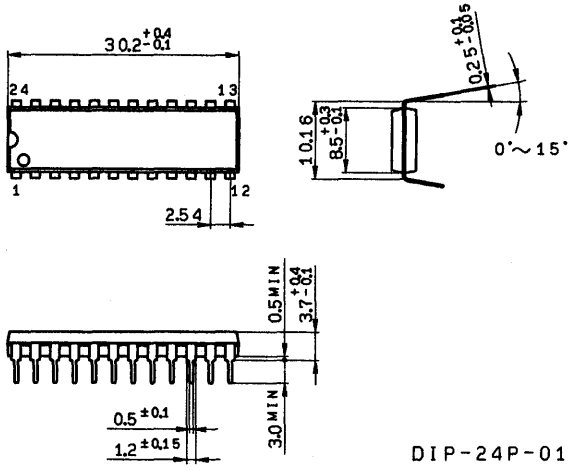
No.	Symbol	Equivalent circuit	Description
1	DV_{EE}		Digital V_{EE} (−5V)
2	−2V ref input		reference voltage input for A/D converter
3	R		Pulldown terminal for external R (30Ω typically)
4	−2V ref output		reference voltage output for A/D converter
5	AV_{EE}		Analog V_{EE} (−5V)
6	CLK output		CLK output for A/D converter
7	$\overline{CLK}$ output		$\overline{CLK}$ output for A/D converter
11	S/H output		S/H output

No.	Symbol	Equivalent circuit	Description
13	S/H input		S/H input
14	6dB AMP output		Olutput terminal of 6dB amplifier
17	6dB AMP input		6dB AMP input
18	AVEE		Analog VEE (−5V)
19	offset adjust		6dB AMP DC offset adjust terminal
21	CLK ref		CLK reference output

No.	Symbol	Equivalent circuit	Description
22	CLK input		CLK input (Note: connect to (21) PIN or input ECL CLK signal)
23	$\overline{\text{CLK}}$ input		$\overline{\text{CLK}}$ input (Note: input ECL $\overline{\text{CLK}}$ signal)

Package Outline Unit : mm

24pin DIP(Plastic) 400mil 2.0g



DIP-24P-01

CXA1008P

Electrical Characteristics (Ta = 25°C, V_{CC} = +5V, V_{EE} = −5V)
S/H section (see Fig. 3)

Item	Condition	Symbol	Min.	Typ.	Max.	Unit
Digital input voltage		V_{IH}	−0.9	−0.8		V
		V_{IL}		−1.6	−1.5	V
CLK Reference voltage (pin 21)		V_{CLKREF}	−1.3	−1.2	−1.1	V
Analog input voltage range	△V < 1.2V *1	V_{INS}	−3		3	V
Output voltage range		V_{outs}	−3		3	V
Power Supply		I_{CC}	48	60	78	mA
	without −2V ref.	I_{EE1}	48	60	78	mA
	with −2V ref. R_{LI} = 50Ω *2	I_{EE2}	80	100	125	mA
Input bias current	−2V < V_{in} < 2V	I_{Biass}		15	30	μA
Output impedance		Z_{OS}		20	40	Ω
Voltage gain ratio		G_{VS}	0.99	1.0	1.01	
Full power bandwidth	V_{in} = $2V_{p-p}$ (−3dB)	BW		12		MHz
Power supply rejection ratio		SVR_s		−40		dB
Hold mode feed through	fin = 4MHz Vin = 1 Vp-p, CLK open	HMTH		−50	−40	dB
Clock leak	V_{in} = 0V	CL_{LEAK}		10	50	mV
Linearity	fin = 19.53kHz (10/512MHz) f_{CLK} = 10MHz *3	Lin		0.08	0.15	%
Hold mode droop	input voltage range, 0 to −2V	HMDR		2	20	mV/μs
Acquisition time	△V = 1.2V	Taq		8	12	ns
Settling time	Settle to ±0.2% of F.S. see the Timing Chart	T_{set}		25		ns
DC offset voltage	f_{CLK} = 5MHz	V_{offset}		±15	±100	mV
Maximum sampling frequency		f_{CLKH}	35			MHz
Minimum sampling frequency		f_{CLKL}			5	MHz
Differential gain (D.G.)	Vin = NTSC 40 IRE mode ramp. f_{CLK} = 20MHz	DG		0.5	1.0	%
Differential phase (D.P.)		DP		0.5	1.0	deg

(R_{LI} = 50Ω. see Fig. 3)

CXA1009P

Electrical Characteristics ($Ta = 25°C$, $V_{CC} = +5V$, $V_{EE} = -5V$)
S/H section (see Fig. 3)

Item	Condition	Symbol	Min.	Typ.	Max.	Unit
Digital input voltage		V_{IH}	−0.9	−0.8		V
		V_{IL}		−1.6	−1.5	V
CLK Reference voltage (pin 21)		V_{CLKREF}	−1.3	−1.2	−1.1	V
Analog input voltage range	$\triangle V < 1.2V$ *1	V_{INS}	−3		3	V
Output voltage range		V_{outs}	−3		3	V
Power supply		I_{CC}	25	35	45	mA
	without −2V ref.	I_{EE1}	25	35	45	mA
	with −2V ref. $R_{LI} = 50\Omega$ *2	I_{EE2}	60	75	98	mA
Input bias current	$-2V < Vin < 2V$	I_{Biass}		9	18	μA
Output impedance		Z_{OS}		20	40	Ω
Voltage gain ratio		G_{VS}	0.99	1.0	1.01	
Full power bandwidth	$Vin = 2V_{p-p}$ (−3dB)	BW		6		MHz
Power supply rejection ratio		SVR_S		−40		dB
Hold mode feed through	fin = 4MHz Vin = 1 Vp-p, CLK open	HMTH		−50	−40	dB
Clock leak	Vin = 0V	CL_{LEAK}		10	50	mV
Linearity	fin = 19.53kHz (10/512MHz) f_{CLK} = 10MHz *3	Lin		0.08	0.15	%
Hold mode droop	input voltage range, 0 to −2V	HMDR		2	10	mV/μs
Acquisition time	$\triangle V = 1.2V$	Taq		12	20	ns
Settling time	Settle to ±0.2% of F.S. see the Timing Chart	T_{set}		36		ns
DC offset voltage	f_{CLK} = 5MHz	V_{offset}		±15	±100	mV
Maximum sampling frequency		f_{CLKH}	18			MHz
Minimum sampling frequency		f_{CLKL}			2	MHz
Differential gain (D.G.)	Vin = NTSC 40 IRE more ramp f_{CLK} = 15MHz	DG		0.5	1.0	%
Differential phase (D.P.)		DP		0.5	1.0	deg

*1 $\triangle V$ is voltage change during one sampling period.
*2 Power consumption is $I_{CC} \times 5V + I_{EE1} \times 5V + 40mA \times 1.8V$.
*3 Input voltage waveform

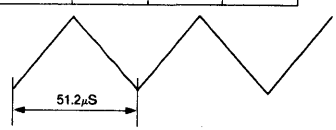


Fig. 2

6dB amp section (see Fig. 3)

Item	Condition	Symbol	CXA1008P			CXA1009P			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Intput voltage range	*3	V_{INA}	−1.3		+0.8	−1.3		+0.8	V
Band width (−3dB)	V_{in} = IV_{pp}	W	45	55		15	25		MHz
Input bias current	−1V < V_{in} < 1V	$I_{Bias\ A}$		9	20		5	10	μA
Output impedance		Z_{OA}		4	10		4	10	Ω
Voltage gain	*4	G_{VA}	5.1	6.0	6.9	5.1	6.0	6.9	dB
Power supply rejection ratio		SVR_A		−40			−40		dB

*3 2ndary harmonic: −40dB f_{in} = 3.58MHz
*4 f_{in} = 3.58MHz V_{in} = $1V_{p\text{-}p}$

CLK OUT section (see Fig. 3)

Item		Condition	Symbol	CXA1008P			CXA1009P			Unit
				Min.	Typ.	Max.	Min	Typ.	Max.	
Output voltage	Amplitude	R_{L2} = 1.5 KΩ see Fig. 3	V_{CLK}	0.2	0.3	0.4	0.2	0.3	0.4	V
	Low level		V_{CLKL}	−1.2	−1.1	−0.9	−1.2	−1.1	−0.9	V
Rise time			tr		7	10		7	10	ns
Fall time			tf		5	8		5	8	ns
CLK Delay 1			τ_{D1}	20	28	34	36	38	45	ns
CLK Delay 2			τ_{D2}	14	22	28	24	26	33	ns

$-2V_{ref}$ amp section (see Fig. 3)

Item	Condition	Symbol	CXA1008P			CXA1009P			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Voltage gain ratio	V_{ref} = −2V R_{LI} = 50Ω	G_{VR}	0.9	1.0	1.1	0.9	1.0	1.1	
Input bias current	−3V < V_{in} < 0V	$I_{Bias\ R}$		5	10		5	10	μA
Output impedance		Z_{OR}		2	10		2	10	Ω

Electrical Characteristics Test Circuit

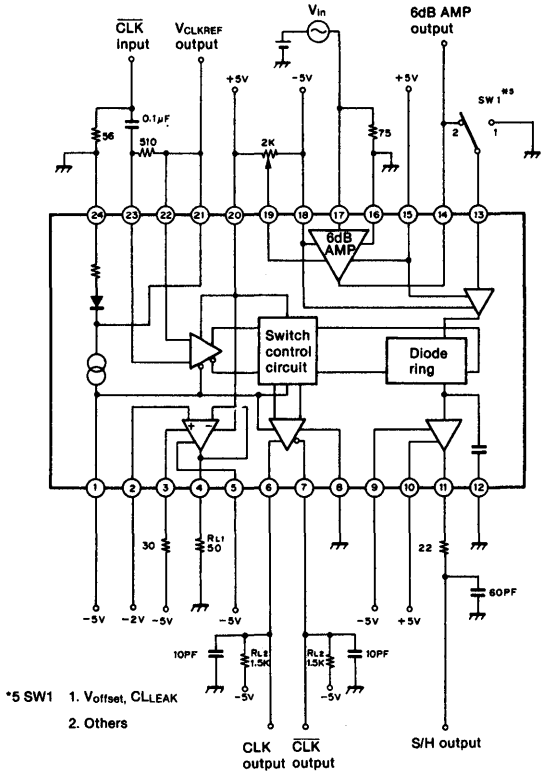


Fig. 3

Timing Chart

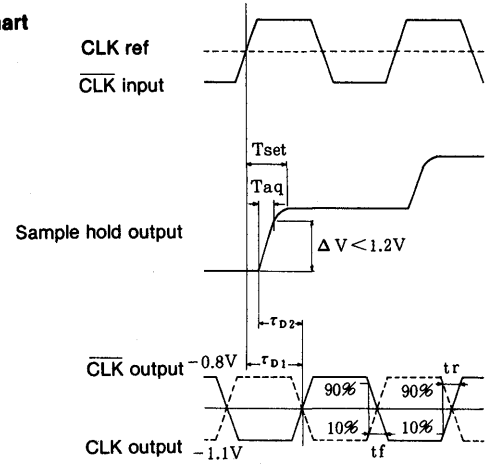


Fig. 4

Description of Functions

CXA1008P/1009P are the monolithic ICs incorporating a high-speed sample hold circuit, a wide band 6 dB amp, reference power supply for A/D converter, and a clock output section, and operate up to a sampling frequency of 35/18 MHz.

CXA1008P/1009P can compose in 20/15 MS/s A/D converter system in combination with a CX20052A. CXA1008P/1009P form, with the input of a single phase or 2-phase ECL clock input, a new sampling signal. For this reason, the sampling period remain unchanged even when the frequency or duty of the input sampling CLK signal changes.

- Wide band 6 dB AMP.

  In-phase amp with a band width over 45/15 MHz amplifies ordinary TV signal (1Vp-p) to a 2Vp-p signal which gives the highest accuracy when processed in CX20052A.

- CLK output section

  When used in combination with an A/D converter such as CX20052A, the CLK timing between the S/H circuit and the A/D converter needs to be adjusted, and up to 20/15 MHz, CXA1008P/1009P generate CLK timing signals for driving the A/D converter, and output 2-phase CLK at 300 mVp-p from pins 6 and 7. With this output, no separate CLK is required to combine with an A/D converter.

- CXA1008P/1009P incorporate a buffer amp to provide a reference voltage for the A/D converter.

Application Circuit

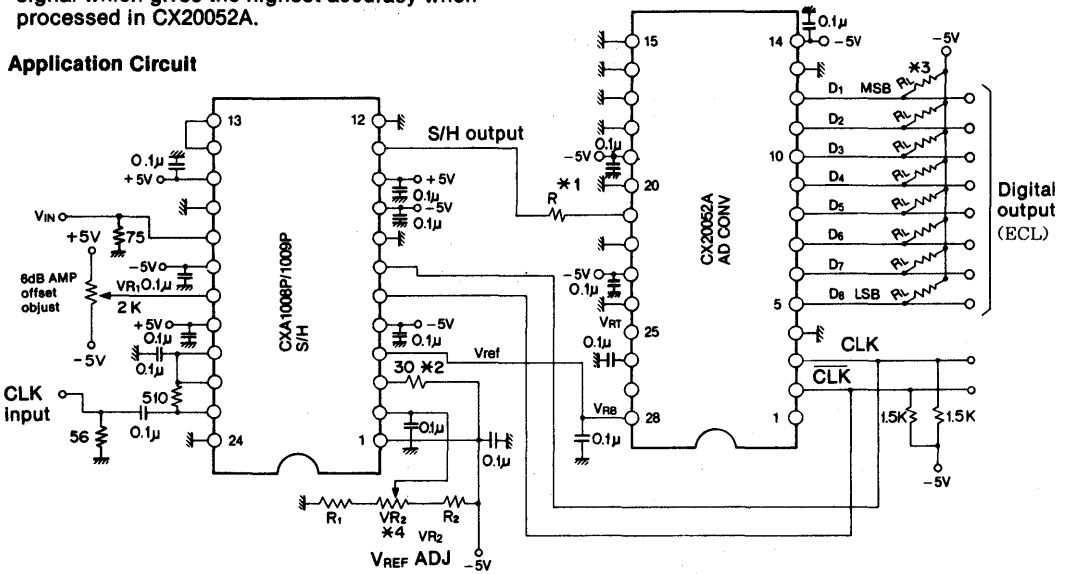


Fig. 5 Connection of CXA 1008P/1008P with CX20052A (1)

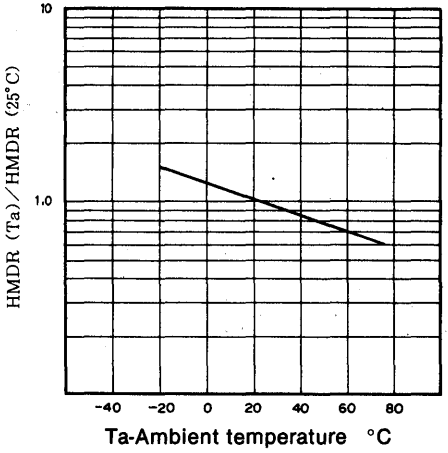
*1 R is a ringing preventing resistor. Select between 10 to 50Ω
*2 Pulldown R for V_{ref}
*3 R_L = 4.3kΩ
*4 R_1 = 1kΩ, VR_2 = 2kΩ, R_2 = 2kΩ

Notes on Application

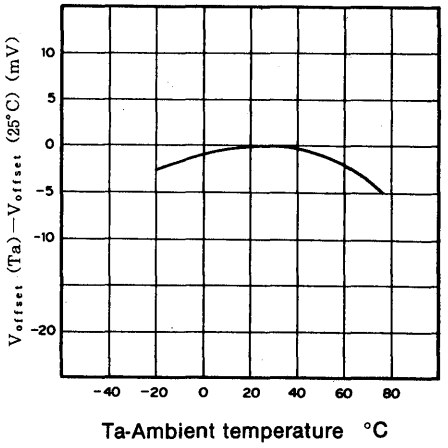
1. Unless sufficiently stable power supply and GND voltage in the high-frequency range are used, the device characteristics deteriorates. For this reason, bring the power supply bypass capacitor as near to this IC as possible, and make the pattern to the power supply and to the earth terminal as wide as feasible.
2. To reduce CLK leak, use waveforms similar to sine waves as far as possible, up to the CLK input. For satisfactory operation, a CLK input ampritude of around 300mV is enough.
3. When the S/H input deviates over 1.2V during one sampling period, the output may contain errors.

Changes in Characteristics with Temperature

Hold Mode Droop Rate

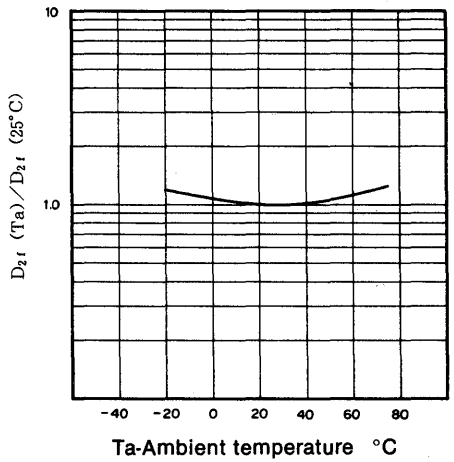


Offset Voltage Between S/H Input & Output

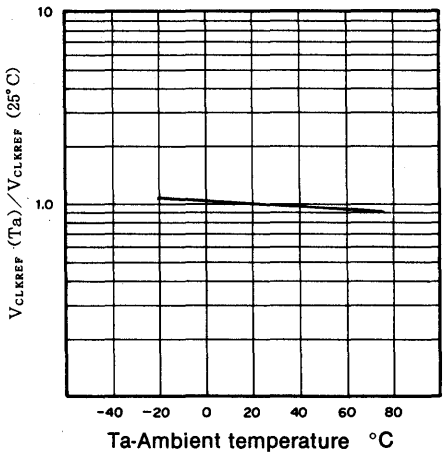


6dB AMP 2ndary Harmonic Level

(3.58MHz, Vin = $1V_{pp}$)



CLK Ref Voltage



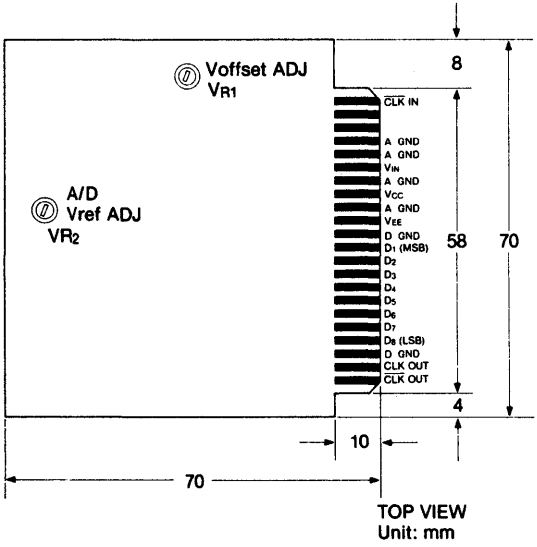
8bit, 20/15MHz A/D Converter Evaluation Board with CXA1008P/CXA1009P S/H.

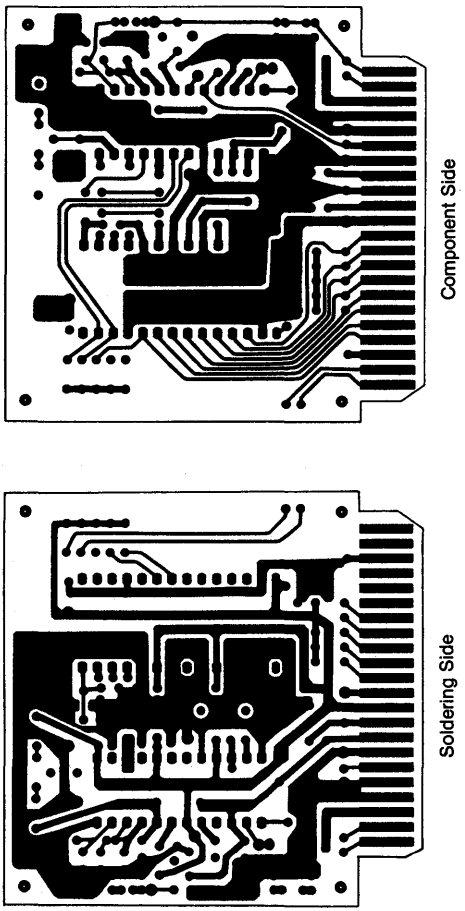
Description

CX20052A PCB-3A/3B is an 8 bit A/D converter board for video signal processing. A high speed S/H IC CXA1008P/1009P and a high speed 8 bit A/D converter CX20052A are assembled on single small printed circuit board.
CX20052A PCB-3A with CXA1008P mounted, operates up to 20 MHz of conversion rate, and CX20052A PCB-3B with CXA1009P mounted, operates up to 15 MHz of conversion rate.

Features

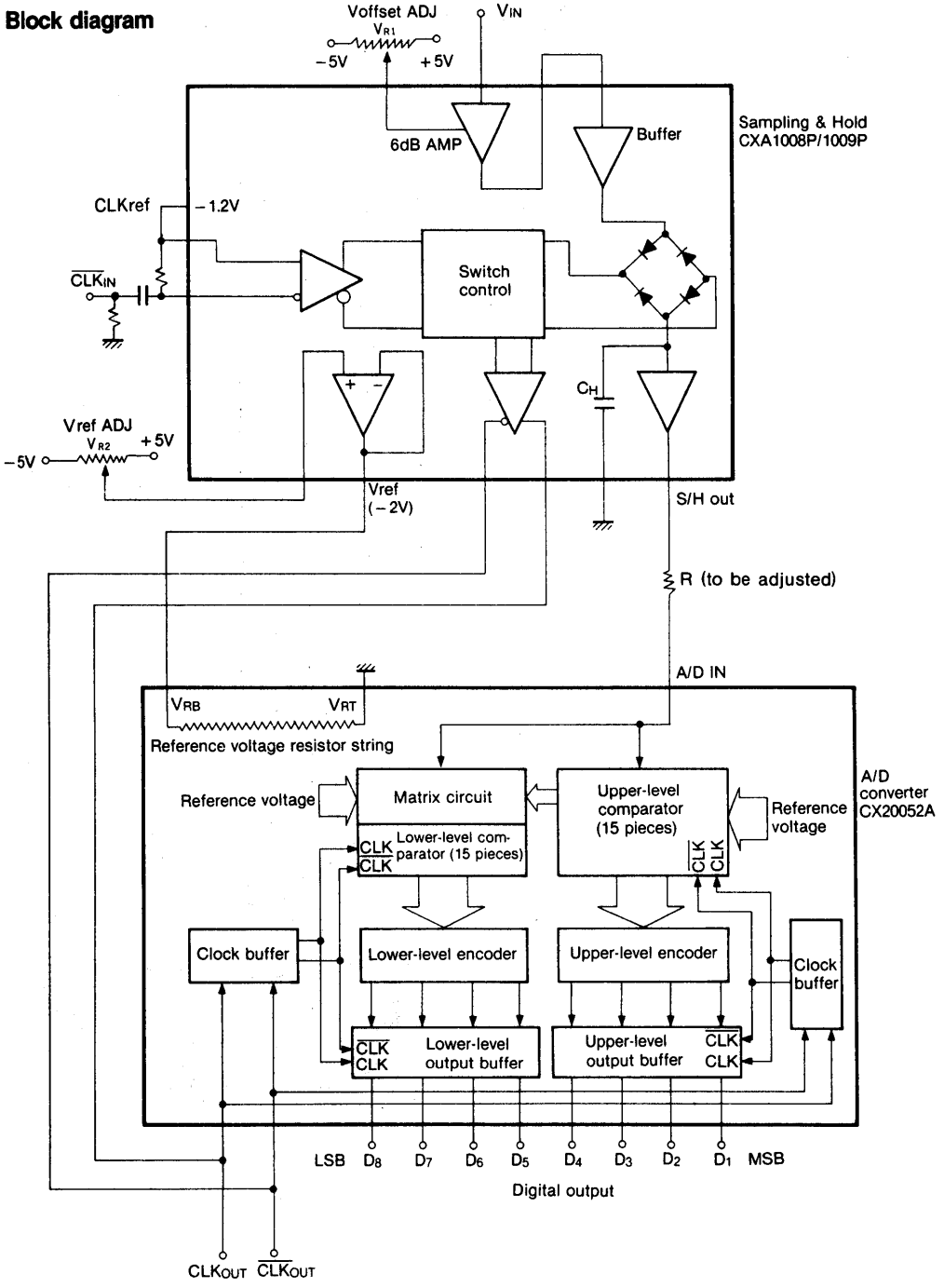
•Resolution	8 bit ±1/2 LSB
•Conversion rate	20 MHz CX20052A PCB-3A
	15 MHz CX20052A PCB-3B
•Analog input level	1Vp-p
•Digital output level	ECL level
•Power supply	±5V





CX20052A PCB-3A/3B Pattern

1. Block diagram



2. Characteristics

1. Supply Voltage

(Ta = 25°C, V_{EE} = −5V, V_{CC} = 5V)

Item			Symbol	Min	Typ	Max	Unit
V_{CC}	+5V	CX20052A	I_{CC}		70	80	mA
		PCB-3A	I_{EE}		220	240	mA
V_{EE}	−5V	CX20052A	I_{CC}		50	60	mA
		PCB-3B	I_{EE}		200	220	mA

2. Analog Input (V_{IN})

Item	Symbol	Min	Typ	Max	Unit
AC Input Voltage Amplitude	V_{IN}			1	V
Offset Adjustable Range		±1.5	±2.0		V
Input Impedance	Z_{in}				
CX20052APCB-3A			75		Ω
CX20052APCB-3B			75		Ω

3. Digital Input ($\overline{CLK}$ IN)

Item	Symbol	Min	Typ	Max	Unit
Input Voltage (p-p)	V_{CLK}	0.3	0.8	4	V
Input Impedance	Z_{INCL}		50		Ω

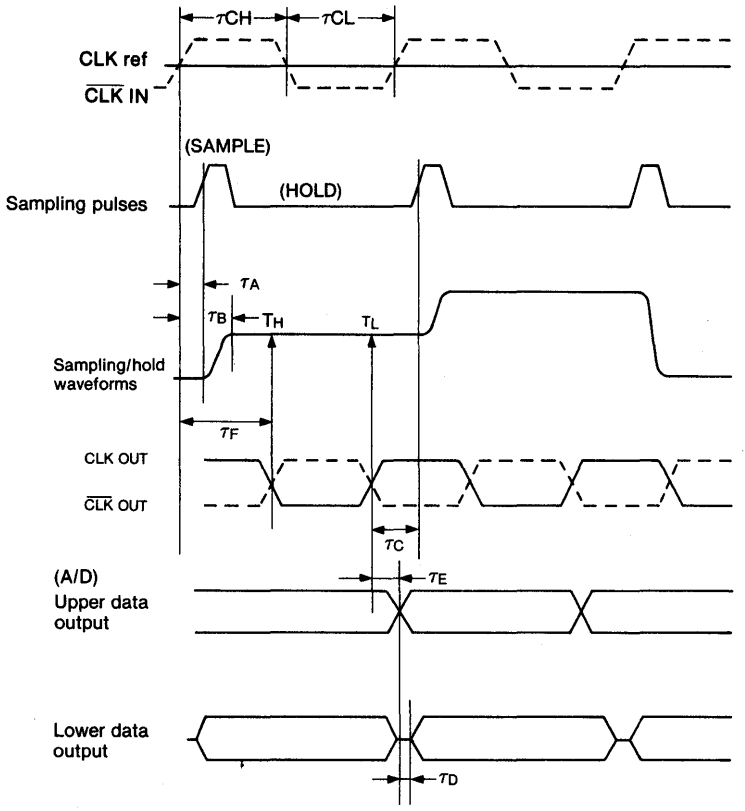
4. Digital Output (D1 ~ D8) (1.5kΩ to V_{EE})

Item	Symbol	Min	Typ	Max	Unit
Output Voltage	V_{OH}	−0.90	−0.75		V
	V_{OL}		−1.50	−1.35	V

5. Clock Output (CLK_{OUT}, $\overline{CLK}_{OUT}$) (See timing chart)

Item		Symbol	CX20052A PCB-3A			CX20052A PCB-3B			
			Min	Typ	Max	Min	Typ	Max	Unit
Output voltage	Amplitude	V_{CLK}	0.2	0.3	0.4	0.2	0.3	0.4	V
	Low Level	V_{CLKL}	−1.2	−1.1	−0.9	−1.2	−1.1	−0.9	V
Rise time		tr		6	10		6	10	ns
Fall time		tf		12	15		12	15	ns
CLK Delay		τ_F	20	28	34	36	38	45	ns

3. Timing Chart



T_H shows a timing when the A/D latches upper 4 bits.
T_L shows a timing when the A/D latches lower 4 bits.

Item	Symbol	CX20052A PCB-3A			CX20052A PCB-3B			
		Min	Typ	Max	Min	Typ	Max	Unit
Clock in	τCH		25			33		ns
	τCL		25			33		ns
Sampling delay	τA		6			12		ns
	τB		25			36		ns
Clock out	τF	20	28	34	36	38	45	ns
Data delay	τE			8			8	ns
	τD			4			4	ns

4. Adjustment

(1) Offset Voltage (Voffset ADJ)
VR1 should be adjusted so that the S/H output meets the input voltage range of the A/D (0 to −2V).
(2) A/D reference voltage (Vref ADJ).
The reference voltage of the A/D (TP5) is to be −2V. VR2 should be adjusted.

5. Output Data Format

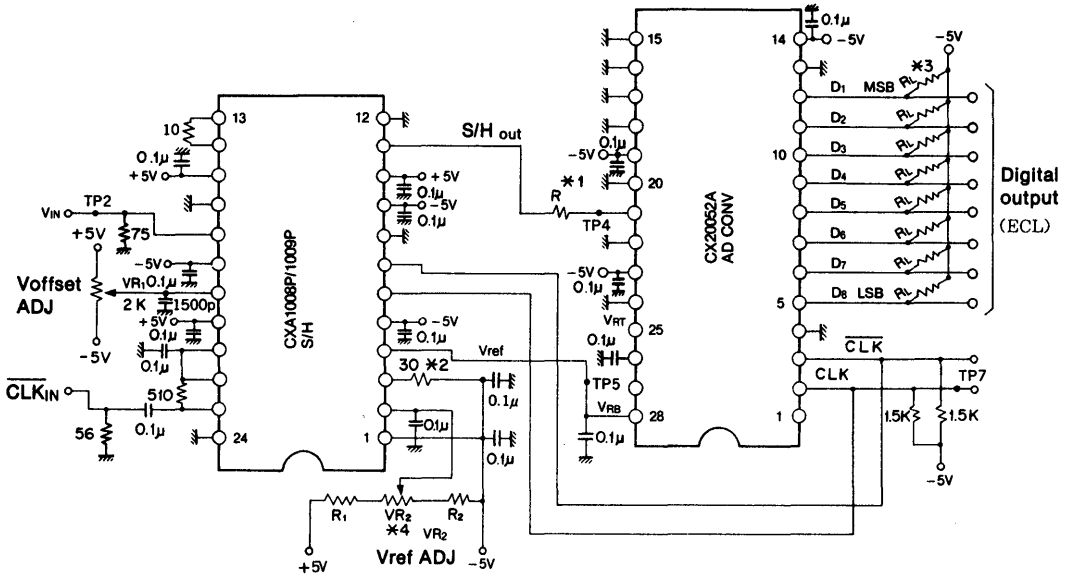
The input of the A/D converter IC (S/H out) is quantized in 8 bit within the reference voltage range of V_{RT} and V_{RB}. The V_{RT} and V_{RB} are set at 0V and −2V respectively on the printed circuit board.

Step	A/D input signal voltage		Digital output code
			MSB LSB
	over	0.0000V	1 1 1 1 1 1 1 1
0 0 0		0.0000V (V_{RT})	1 1 1 1 1 1 1 1
.		.	.
.		.	.
.		.	.
1 2 7		−0.9961V	1 0 0 0 0 0 0 0
1 2 9		−1.0039V	0 1 1 1 1 1 1 1
.		.	.
.		.	.
.		.	.
2 5 5		−2.0000V (V_{RB})	0 0 0 0 0 0 0 0
	under	−2.0000V	0 0 0 0 0 0 0 0

6. Note on application

(1) Although the pull down resistors (RL: 4.3kΩ) are mounted on the PCB, additional pull down is recommended in an external circuit. The output current at the A/D output terminal should not exceed 10 mA.
(2) Digital output data should be latched by an external circuit to achieve a rated performance. Output data can be latched at a rising edge of CLK_{OUT}.
CLK_{OUT} AND $\overline{CLK}_{OUT}$ should be reshaped by an ECL line receiver such as MC10116 in an external circuit.
(3) The reference voltage is derived from the V_{EE} by a simple resistor dividing network. The power supply (±5V) should be stabilized to reduce voltage drift of the reference voltage.
(4) To reduce CLK leak, use waveforms similar to sine waves as far as possible up to the CLK input. For satisfactory operation, a CLK input amplitude of around 300m V_{PP} is enough.
(5) When the S/H input deviates over 1.2V during one sampling period, the output may contain errors.

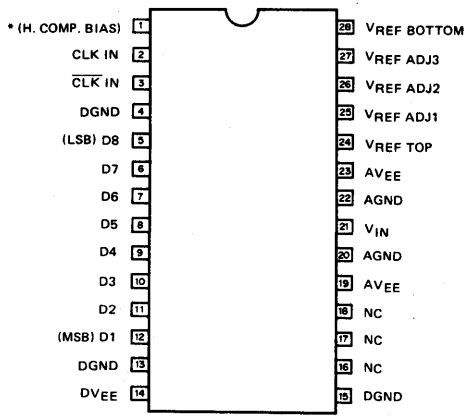
CX20052A PCB-3A/3B Circuit



*1. R is a ringing preventing resistor. Select between 10 to 50Ω according to pattern length.
*2. Pulldown R for Vref.
*3. $R_L = 4.3k\Omega$
*4. $R_1 = 2k\Omega, VR_2 = 2k\Omega, R_2 = 1k\Omega$

Additional Information on CX20052A

Pin Configuration (Top View)

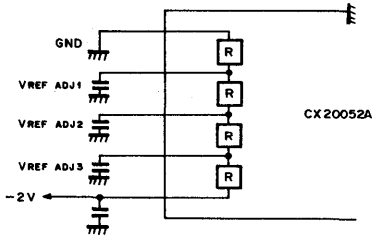


* Pin-1 to be used open.

Pin Description

No.	Symbol	Description
1	H-COMP BIAS	Pin connected to internal comparator. It should not be connected to outer circuit.
2	CLK IN	CLOCK input pin.
3	$\overline{\text{CLK}}$ IN	$\overline{\text{CLOCK}}$ input pin.
4	DGND	Ground pin of digital circuit.
15	DGND	Ground pin of digital circuit.
17	NC	Non-connection.
18	NC	
24	$V_{REF\ (T)}$	Reference voltage pin. (0V)
25	$V_{REF\ ADJ1}$	Reference voltage adjusting pin. (Usually it should be connected to GND through 0.047 μF capacitor.)
26	$V_{REF\ ADJ2}$	
27	$V_{REF\ ADJ3}$	
28	$V_{REF\ (B)}$	Reference voltage pin. (−2.0V)

(*) Reference resistors have adjusting pins as shown below. Usually these pins are connected to GND through 0.047 μF capacitors. When an adjustment is required, they should be connected to GND or $V_{REF\ (B)}$ through resistors.



Output Coding

Step	Input signal voltage	Output digital code (MSB LSB)
000	0.0000V	11111111
.	.	.
.	.	.
.	.	.
127	−0.9961V	10000000
128	−1.0039V	01111111
129	−1.0118V	01111110
.	.	.
.	.	.
.	.	.
255	−2.0000V	00000000

High Resolution A/D, D/A Converters

6

4. High Resolution A/D, D/A Converters (for Audio)

Type	Function	Page
CX20018 CXA1144S	Dual 16-bit 44kHz Multiplexed A/D Converter	305
CX20133	Dual 16-bit 44kHz Multiplexed D/A Converter	326
CX20152	Dual 16-bit 88kHz Multiplexed D/A Converter	337
CXD1077M	Dual 10bit 50kHz Multiplexed A/D, D/A	355

SONY® CX20018/CXA1144S

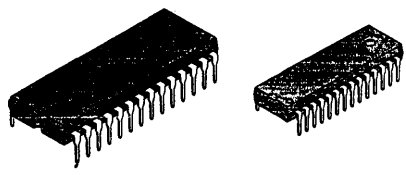
Dual 16 bit 44kHz Multiplexed A/D Converter

Evaluation Board Available — CX20018PCB

Description

CX20018/CXA1144S are monolithic bipolar ICs designed for PCM (Pulse Code Modulation) audio. This IC consists of 16 bit counters, shift registers, clock buffer, clocked synchronous comparator, stabilized current source and TTL compatible interface circuits, etc.

28 pin DIP (Plastic) 28 pin SDIP (Plastic)



Features

- Good monotonicity
- Low noise
- TTL compatible input/output
- Stereo or monaural modes can be selected by external control

Structure

Bipolar silicon monolithic IC

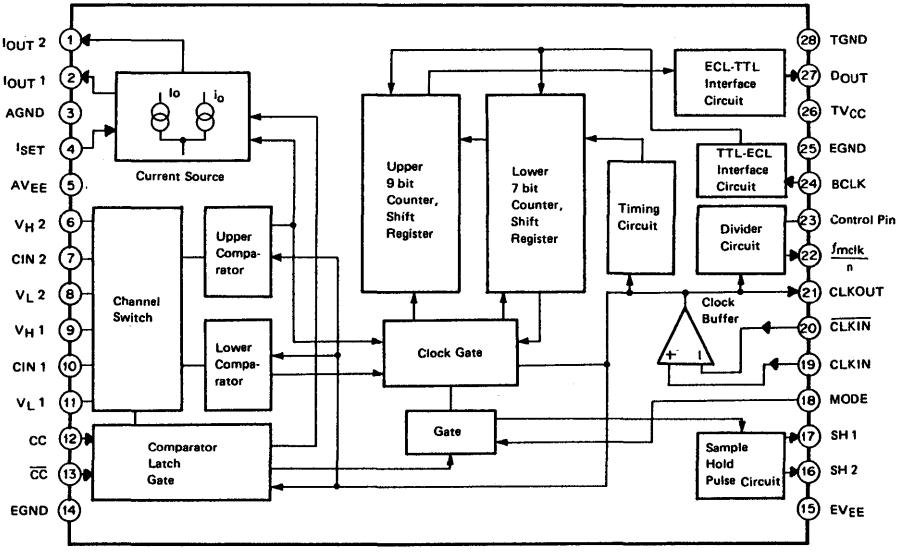
Absolute Maximum Ratings

• Supply voltage	V_{CC} to V_{EE}	12	V	
• Operating temperature	Topr	−20 to +75	°C	
• Storage temperature	Tstg	−50 to +150	°C	
• Allowable power dissipation	P_D	1.7	W	(CX20018)
	P_D	1.2	W	(CXA1144S)

Recommended Operating Conditions

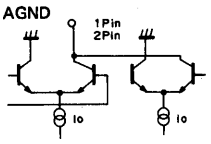
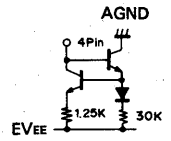
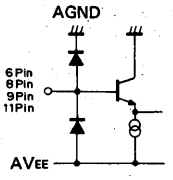
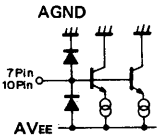
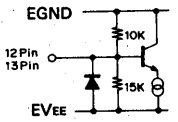
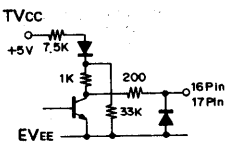
• Supply voltage	V_{CC}	4.75 to 5.25	V
	V_{EE}	−5.25 to −4.75	V

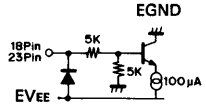
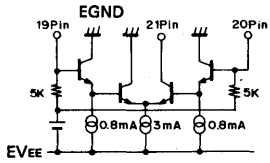
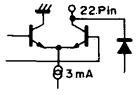
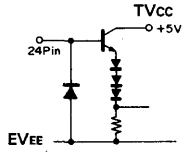
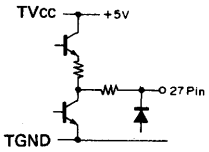
Block Diagram



E89634-ST

Pin Description and Equivalent Circuit

No.	Symbol	Equivalent circuit	Description
1	I_{OUT2}		Integration current output of channel 2
2	I_{OUT1}		Integration current output of channel 1
3	AGND		Analog ground
4	I_{SET}		Setting the value of integration current (I_{SET}=32io, I_{SET}=Io/4) $I_{SET} \leqq 750\mu A$
5	AV_{EE}		Analog supply
6	VH2		Upper comparator input of channel 2
8	VL2		Lower comparator input of channel 2
9	VH1		Upper comparator input of channel 1
11	VL1		Lower comparator input of channel 1
7	CIN2		Upper and lower common input of channel 2
10	CIN1		Upper and lower common input of channel 1
12	CC		Non-inverting input of conversion command 600mV≦CC≦4.0V
13	$\overline{CC}$		Inverting input of conversion command
14	EGND		Digital ground (ECL)
15	EV_{EE}		Digital supply
16	SH2		Sample/hold pulse output of channel 2
17	SH1		Sample/hold pulse output of channel 1

No.	Symbol	Equivalent circuit	Description
18	MODE		Switching of stereo, monaural or sample/hold pulse.
23	CONTROL PIN		Determining division ratio of divided output. Can select division ratio at OFF, 1/2, 1/4, 1/8 of master clock frequency
19	CLK IN		Non-inverting input of clock buffer
20	$\overline{\text{CLK IN}}$		Inverting input of clock buffer
21	CLK OUT		Output of clock buffer
22	$\frac{\text{fMCLK}}{\text{N}}$		Divided output (Open corrector)
24	BCLK		Clock input that shifts the internal converted data to external.
25	EGND		Digital ground
26	TVCC		Digital supply
27	DOUT		Conversion data output (Output at TTL level)
28	TGND		TTL ground

Electrical Characteristics

(Ta=25°C, V_{EE}=−5V, V_{CC}=5V)

Item	Symbol	Pin No. and Test Condition	Min.	Typ.	Max.	Unit	Note
Supply voltage range *1	V_{EE}		−4.75	−5.00	−5.25	V	1
Supply voltage range *1	V_{CC}		4.75	5.00	5.25	V	1
Circuit current	I_{EE}		70.0	102.0	130.0	mA	1
Circuit currnet	I_{CC}		4.0	10.0	15.0	mA	1
Current output pin leak	I_{OLEAK}	1, 2 (Pins 1, 2 Voltage=0V when current output is off)			1.0	μA	2
I_{OUT} output current	I_{out}	1, 2 (Pins 1, 2 Voltage=0V. Iset=410 μA)		1.64		mA	2
Current ratio *2	I_o/i_o	1, 2 (I_{set}=410 μA)	127.0	128.0	129.0		2
Maximum I_{SET} current	I_{SET} Max.	4 $127.0 \leqq \frac{I_o}{i_o} \leqq 129.0$			750	μA	2
Sample hold pulse high level output voltage	V_{SH1H} V_{SH2H}	16, 17	−0.05	0	0.1	V	
Sample hold pulse low level output voltage	V_{SH1L} V_{SH2L}	16, 17	−4.40	−4.25	−3.50	V	
Clock input bias voltage	V_{CLKIN} $\overline{V_{CLKIN}}$	19, 20	−1.90	−1.72	−1.50	V	
Clock output low level output current	$I_{CLKOUTL}$	21		3.0	4.0	mA	
CC, $\overline{CC}$ input bias voltage	V_{CCIN} $\overline{V_{CCIN}}$	12, 13	−2.20	−1.92	−1.60	V	
Data output high level output voltage	V_{DOUTH}	27 I_{OH}=0.1 mA	3.2			V	
Data output low level output voltage	V_{DOUTL}	27 I_{OL}=−0.4 mA			0.4	V	
Bit clock high level input voltage	V_{BCLKH}	24	2.0			V	
Bit clock low level input voltage	V_{BCLKL}	24			0.5	V	
Bit clock high level input current	I_{BCLKH}	24		4		μA	
Bit clock low level input current	I_{BCLKL}	24	0.2	1		μA	
Distortion *3 factor	THD	During 0 dB (full scale) playback for both channel		0.005	0.006	%	3
		During −20 dB playback for both channel			0.05	%	3

Item	Symbol	Pin No. and Test Condition		Min.	Typ.	Max.	Unit
Maximum operating clock frequency	f_{MCLK}	Self-excitation or separate excitation	CX20018			100 (CX20018)	MHz
			CXA1144S			95 (CXA1144S)	
Dividing ratio control voltage	V_{CTL} (∞)	23		2.0		5.0	V
	V_{CTL} (2)	23		0.2		0.8	V
	V_{CTL} (4)	23		−0.8		−0.2	V
	V_{CTL} (8)	23		−5.0		−2.0	V
Mode control voltage	V_{MODE} (1)	18 Stereo, S/H ON		2.0		5.0	V
	V_{MODE} (2)	18 Stereo, S/H OFF		0.2		0.8	V
	V_{MODE} (3)	18 Monaural, S/H OFF		−0.8		−0.2	V
	V_{MODE} (4)	18 Monaural, S/H ON		−5.0		−2.0	V

Note) 1 Pins 1, 2, 3, 6, 7, 8, 9, 10, 11, 14, 21, 25 and 28 are for grounding, pins 18, 22, 23, are connected V_{CC}. Pin 4 draws 410 μA of current by external current source.

2 Reference to the current ratio test circuit.

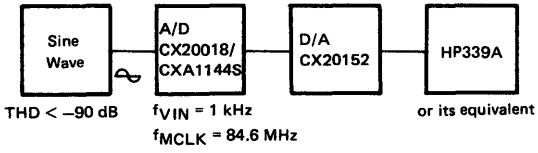
3 Conversion Frequency 44.1 kHz
Distortion Meter HP339A (all Filters are turned on) or its equivalent that has an 80 kHz, LPF, 30 kHz LPF and 400 Hz HPF.

*1 Recommended operating voltage

*2 In the current ratio test circuit (See Fig. 1)

$$\left|15 \times 8\ (k\Omega) \times i_o\ (\mu A) - \frac{15}{16}\ (k\Omega) \times I_o\ (\mu A)\right| < 12.0\ mV$$

*3 Measurement Method (See Note 3)

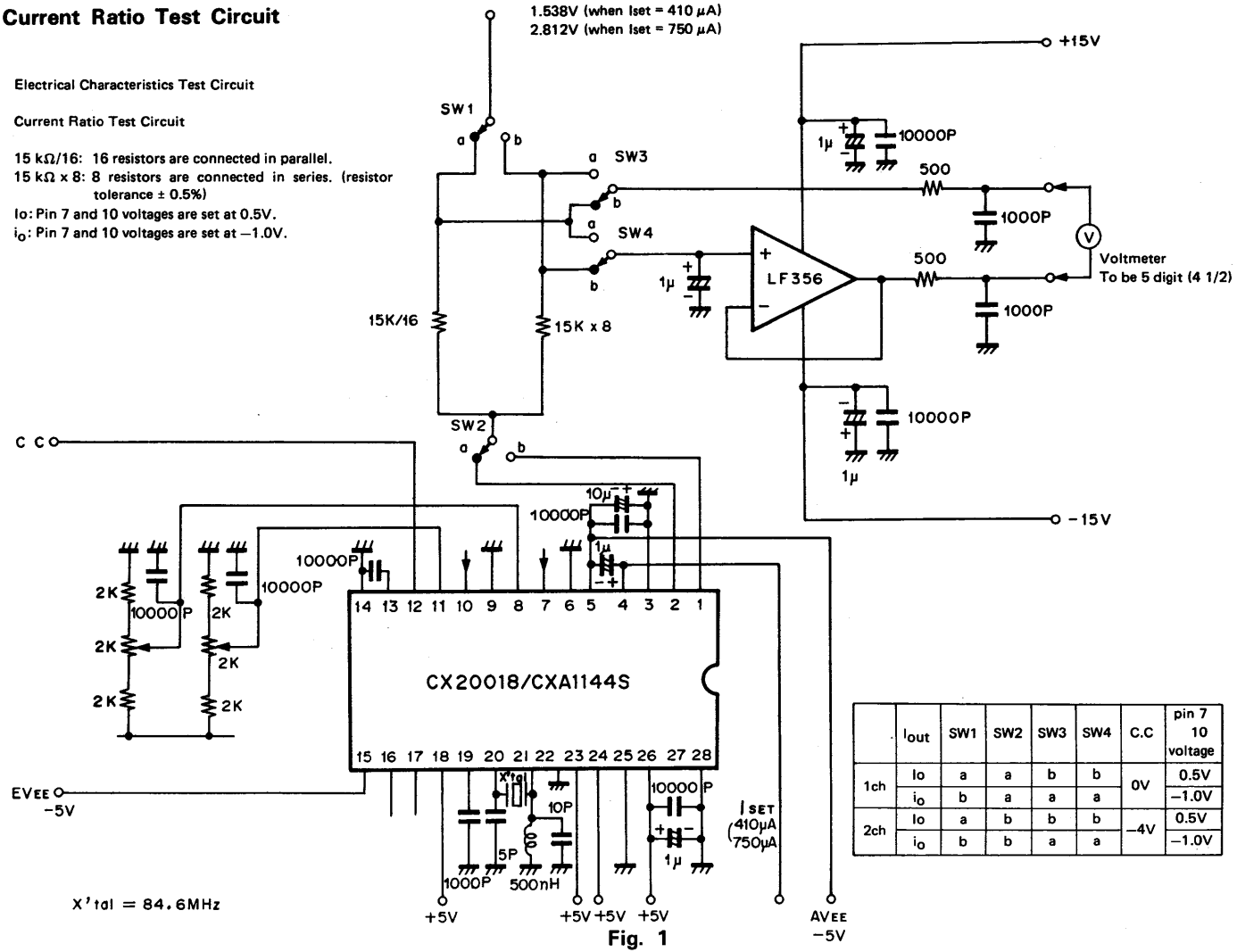


Current Ratio Test Circuit

Electrical Characteristics Test Circuit

Current Ratio Test Circuit

15 kΩ/16: 16 resistors are connected in parallel.
15 kΩ x 8: 8 resistors are connected in series. (resistor tolerance ± 0.5%)
Io: Pin 7 and 10 voltages are set at 0.5V.
i_O: Pin 7 and 10 voltages are set at −1.0V.



	Iout	SW1	SW2	SW3	SW4	C.C	pin 7 10 voltage
1ch	Io	a	a	b	b	0V	0.5V
	i_O	b	a	a	a		−1.0V
2ch	Io	a	b	b	b	−4V	0.5V
	i_O	b	b	a	a		−1.0V

Fig. 1

Description of CX20018 Conversion Process

Conversion process

The timing circuit controls a conversion cycle and send "Data Transfer Pulse" to the 16 bit shift register for transmitting the last converted data. It is reset by both the edge of CC (Conversion Command), and the master clock pulse is fed to the timing circuit.
"Data Transfer Pulse" and "Mask Pulse" become "H" level as soon as the timing circuit starts to count clocks. "Data Transfer Pulse" becomes "L" when the timing circuit counts 11 clocks, and then the last data is transferred. Simultaneously, "Current Switch Pulse" becomes "H", and integral current starts to flow. "Counter Preset Pulse" becomes "H" when the timing circuit counts 16 clocks. And then, upper and lower level counters are reset. Counter Preset Pulse holds "H" level during the period of 8 clocks.
When the timing circuit counts 31 clocks, Mask Pulse becomes "L" and A/D conversion starts.
The coarse current "I_0" discharges the sampled charge of integrator until the output voltage of integrator crosses the reference voltage (VrefH). During this period the upper level counter counts the number of clock. After crossing the VrefH the fine current discharges the remaining charge of integrator. The lower level counter counts the number of clock until the output voltage of integrator crosses the lower level references voltage (VrefL). (See Figs. 2, 3, 4)

Data output

Data are 16 bit serial signals and 2's complement. The serial data are synchronous with a rising edge of Bit clock (BCLK), and only MSB data is synchronized with a edge of "Conversion Command (CC)" (See Fig. 3)

Monaural operation mode

In monaural mode the external integrator is tracking the input signal during CC is "H" state. At the moment when CC goes "L" state, the CX20018/CXA1144S starts conversion. The data is transferred to the output from MSB sequentially.
After 16 bit data are transferred, "Data Out" comes to the "H" level and keeps "H" level until next conversion. (See Fig. 4)

Timing Chart

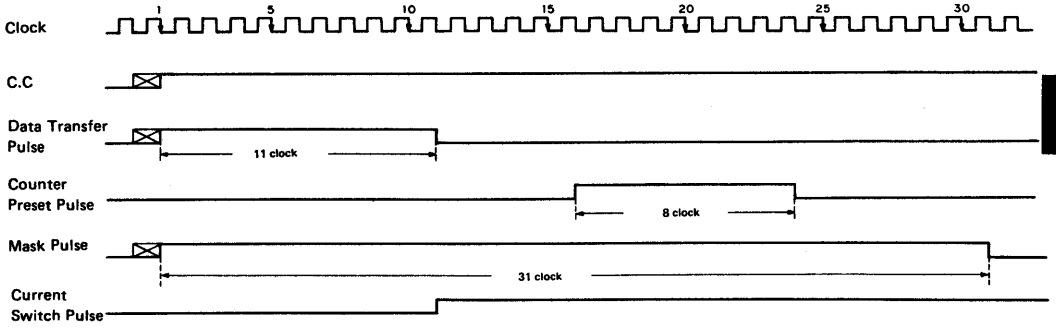


Fig. 2

Stereo Mode

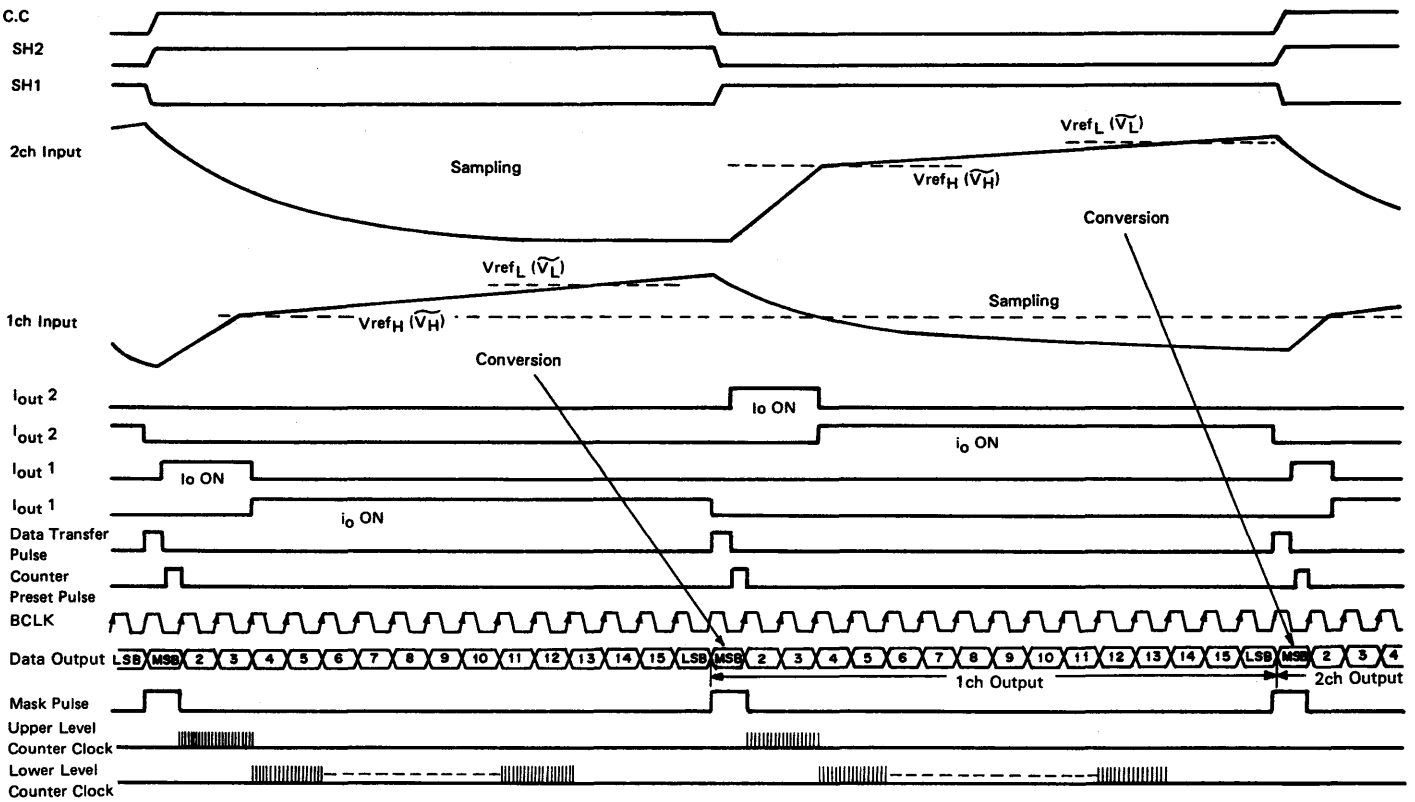


Fig. 3

Monaural Mode

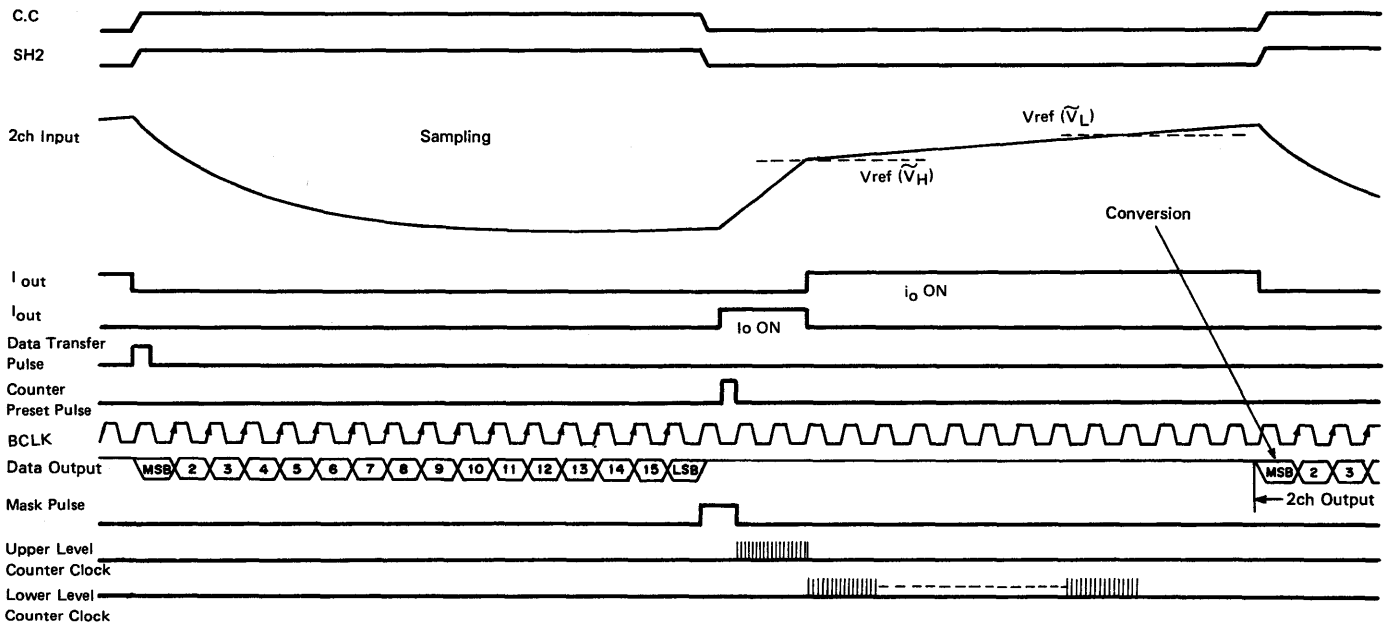


Fig. 4

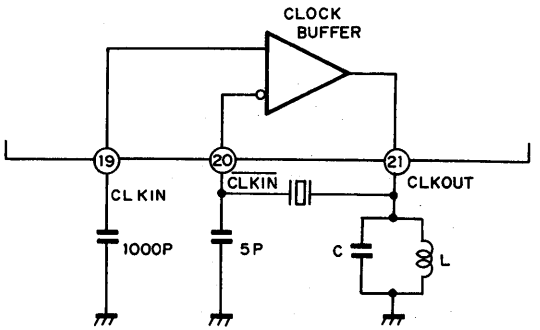
Interface Circuit, Divider Circuit, Sample/Hold Circuit

(1) Intergration current output
Recommended value; $I_{set} = 410\ \mu A$

$$\left(\begin{array}{l} I_o = 4\ I_{set} = 1.64\ mA \\ i_o = \frac{1}{32}\ I_{set} = 12.8\ \mu A \end{array}\right)$$

with $C_{SH} = 1000pF$
$f_{MCLK} = 84.6$ MHz
$V_{in} = 10$ Vp-p

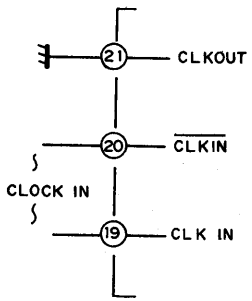
(2) Clock Buffer
(a) Internal clock (Excited circuit with crystal)



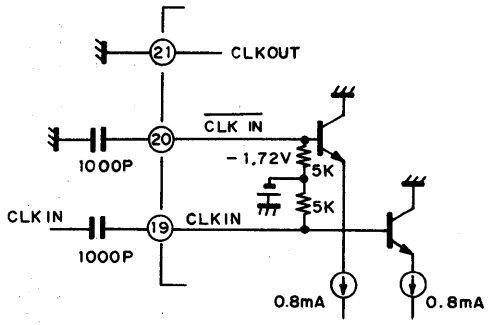
(X'tal 84.6 MHz)

(C, L) = (10p, 500nH)
or
(15p, 270nH)

(b) External clock



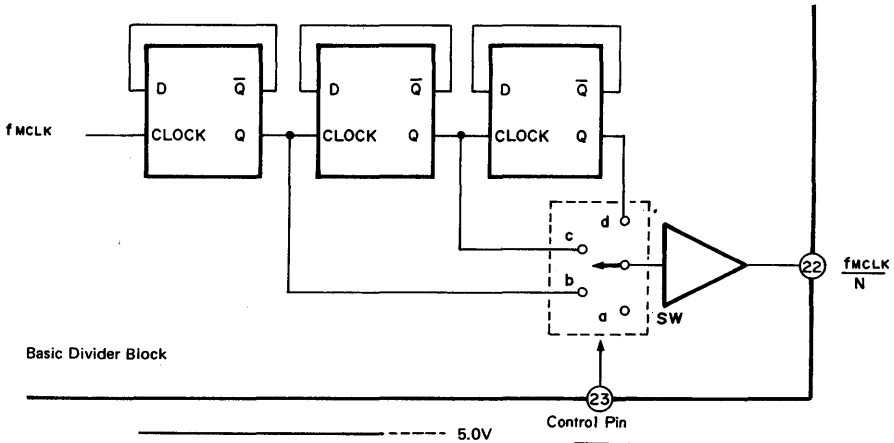
Balanced input



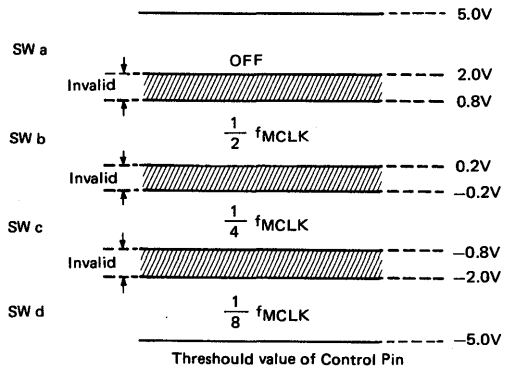
Single ended input

(3) f_{MCLK}/N Output

The output of f_{MCLK}/N is prepared for synchronous operation with digital circuit. Divided value "N" is determined by external control, and N is 2, 4, 8 or ∞.



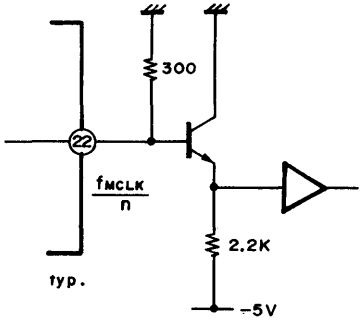
N	V_{CTL} Range
∞	$5.0V \geqq V_{CTL} \geqq 2.0V$
2	$0.8V \geqq V_{CTL} \geqq 0.2V$
4	$-0.2V \geqq V_{CTL} \geqq -0.8V$
8	$-2.0V \geqq V_{CTL} \geqq -5.0V$



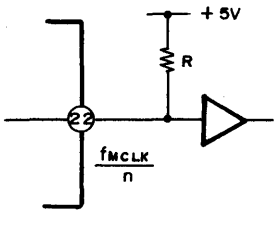
(4) Recommended Interface Circuit

In all of these cases, R15(3KΩ) mounted on the PCB should be removed. Instead, a resister (300,3.6K and 1.2K, respectively) should be attached externally.

(a) ECL 10k (N=2)

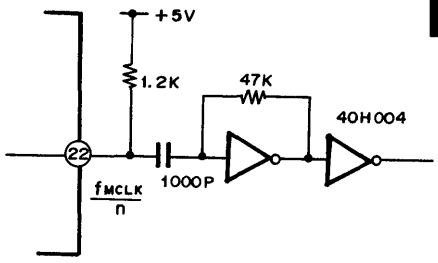


(b) TTLs (N=4 or 8)



R = 9.1K
R = 3.6K (LS)
R = 3K (ALS)

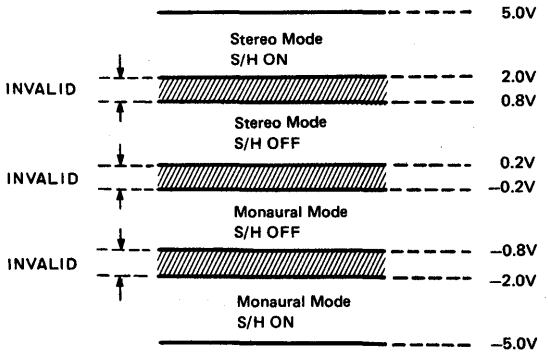
(c) High Speed CMOS (N=8)



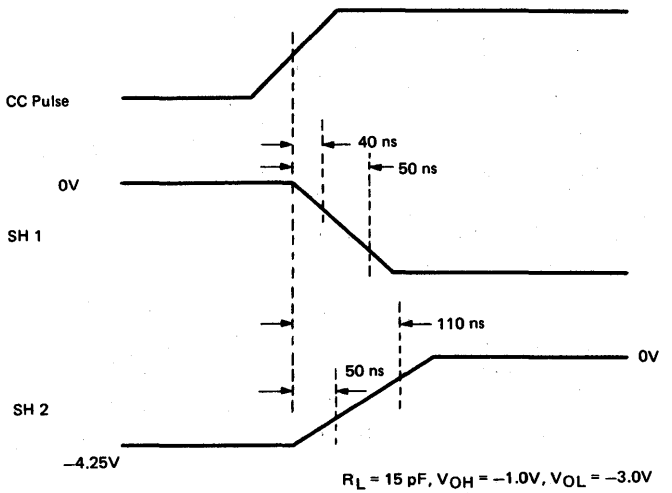
(5) Stereo mode, Monaural mode

Stereo or Monaural modes can be selected by mode pin. And "ON" or "OFF" state of Sample/Hold Pulse is selected similary.

This is illustrated in the following way.

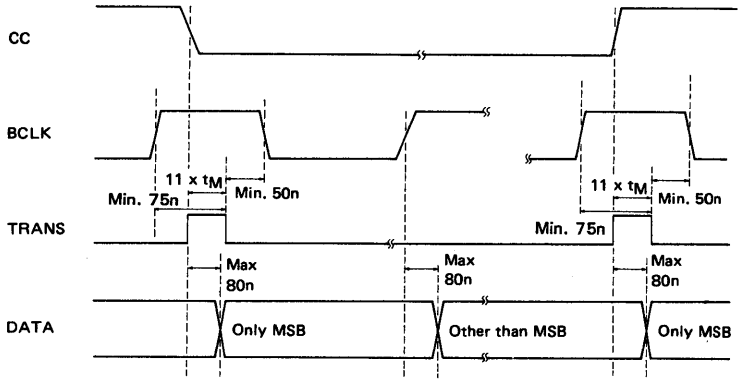


S/H Pulse



Propagation Delay Times from CC input to SH1, SH2 output

(6) Data Out

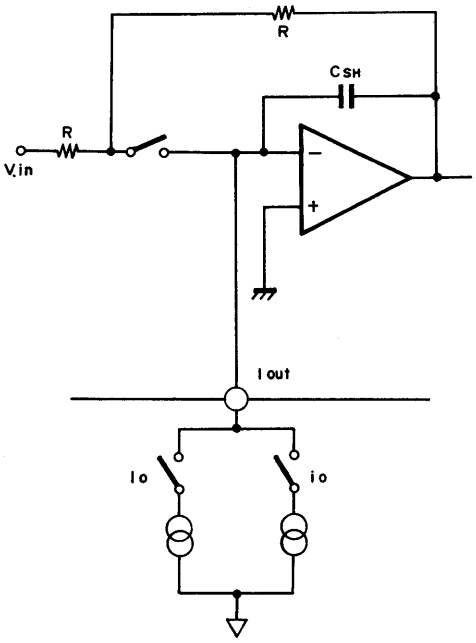


Propagation Delay Time from CC or BCLK Data Out
The maximum frequency of BCLK = 4 MHz

(Only MSB is delayed against the CC pulse.
Others are delayed against the bit clock.)
t_M; One cycle of master clock

(7) Relationship of V_{in} max, CSH, I_{set}, I_o and i_o

(1) Vin is defined as the input voltage of integrator.
(2) I_o, i_o are defined as the coarse and fine integration current respectively.
(3) In case of a full scale input voltage.



$$V_{in}\ max = \frac{I_o\ \tau_o}{CSH}(2^9 - 1) + \frac{i_o\ \tau_o}{CSH}(2^7 - 1)$$

Using $I_o = 4I_{set}$, $i_o = \frac{1}{32} I_{set}$

$$V_{in}\ max = \frac{1}{32} \cdot \frac{I_{set}\ \tau_o}{CSH}(2^{16} - 1)$$

Assuming, $V_{in}\ max = 10$ Vp-p, $\tau_o = \frac{1}{f} = \frac{1}{84.6\ MHz}$

$CSH = 1500$ PF

$\therefore I_{set} = 620\ \mu A$

$\therefore 1\ LSB = \frac{i_o\ \tau_o}{CSH} = 152uV$

Note) In case of non-inverting operation, Vin max. is limited to 5 Vp-p.

(8) Select guide of f_{MCLK}, f_{BCLK} and fcc.

(1) In case of CX20018

(a) Stereo mode

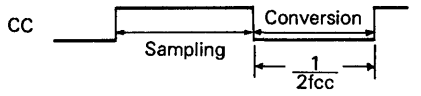
f_{MCLK}, f_{BCLK} and fcc are the frequency of MCLK, BCLK and CC, respectively. The following relation should be followed:

$f_{MCLK} \leqq 100\text{MHz}$

$f_{BCLK} \leqq 4\text{MHz}$

$fcc \leqq \frac{1}{32} f_{BCLK}$

$\frac{1}{2fcc} \geqq \frac{795}{f_{MCLK}}$ (*)



(*) The minimum number of clock for a conversion is calculated as follows.

$(2^9 - 2) + 2 \times (2^7 - 1) + (2^5 - 1) = 795$ clocks

Upper level Counter — Lower level counter — Timing circuit

Namely,

$32fcc \leqq f_{BCLK} \leqq 4\text{MHz}$ ...①

$1590fcc \leqq f_{MCLK} \leqq 100\text{MHz}$ ...②

For f_{BCLK}, **32fcc is recommendable for simple system.**

(Example 1)
If fcc is fixed at 44.06 kHz,
1.41 MHz $\leqq f_{BCLK} \leqq$ 4 MHz
(f_{BCLK} = 32fcc is recommended.)
71 MHz $\leqq f_{MCLK} \leqq$ 100 MHz

(Example 2)
If f_{MCLK} is 100 MHz,
fcc $\leqq$ 62 kHz
32fcc $\leqq f_{BCLK} \leqq$ 4 MHz
(f_{BCLK} = 32fcc is recommended.)

(Example 3)
If f_{BCLK} is 4 MHz,
fcc $\leqq$ 62 kHz
1590fcc $\leqq f_{MCLK} \leqq$ 100 MHz

(b) Monaural mode

Using slower f_{MCLK} or realizing faster conversion time is possible by changing the duty of CC. Assuming the duty of CC is X%, the following relation should be followed:

$f_{MCLK} \leqq 100$ MHz

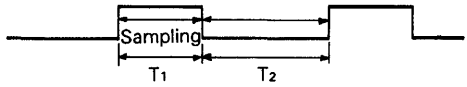
$f_{BCLK} \leqq 4$ MHz

$T_1 \geqq \frac{16}{f_{BCLK}}$

$T_2 \geqq \frac{795}{f_{MCLK}}$ (*)

$T_1 + T_2 = \frac{1}{fcc}$

$T_1 : T_2 = X : 100\text{-}X$



These lead to

$\frac{1600}{X}$ fcc $\leqq f_{BCLK} \leqq 4$ MHz ...③

$\frac{79500}{100-X}$ fcc $\leqq f_{MCLK} \leqq 100$ MHz...④

For f_{BCLK}, $\frac{1600}{X}$ (i.e. $\frac{16}{T_1}$) is recommendable for simple system.

(Example 1)
If fcc is 44.06 kHz,

$\frac{70.5\ MHz}{X} \leqq f_{BCLK} \leqq 4MHz$

($f_{BCLK} = \frac{70.5\ MHz}{X}$ is recommended)

$\frac{3500MHz}{100-X} \leqq f_{MCLK} \leqq 100MHz$

In a simple case where X = 25 and $f_{BCLK} = \frac{70.5\ MHz}{X}$,
$f_{BCLK} = 2.82$ MHz,
47 MHz $\leqq f_{MCLK} \leqq$ 100 MHz → f_{MCLK} can be 47 MHz.

(Example 2)
If f_{MCLK} = 100 MHz,
$fcc \leqq$ Min ($\frac{100-X}{795}$MHz, $\frac{X}{400}$ MHz)

$\frac{1600}{X} fcc \leqq f_{BCLK} \leqq 4$ MHz

($f_{BCLK} = \frac{1600}{X}$ fcc is recommended)

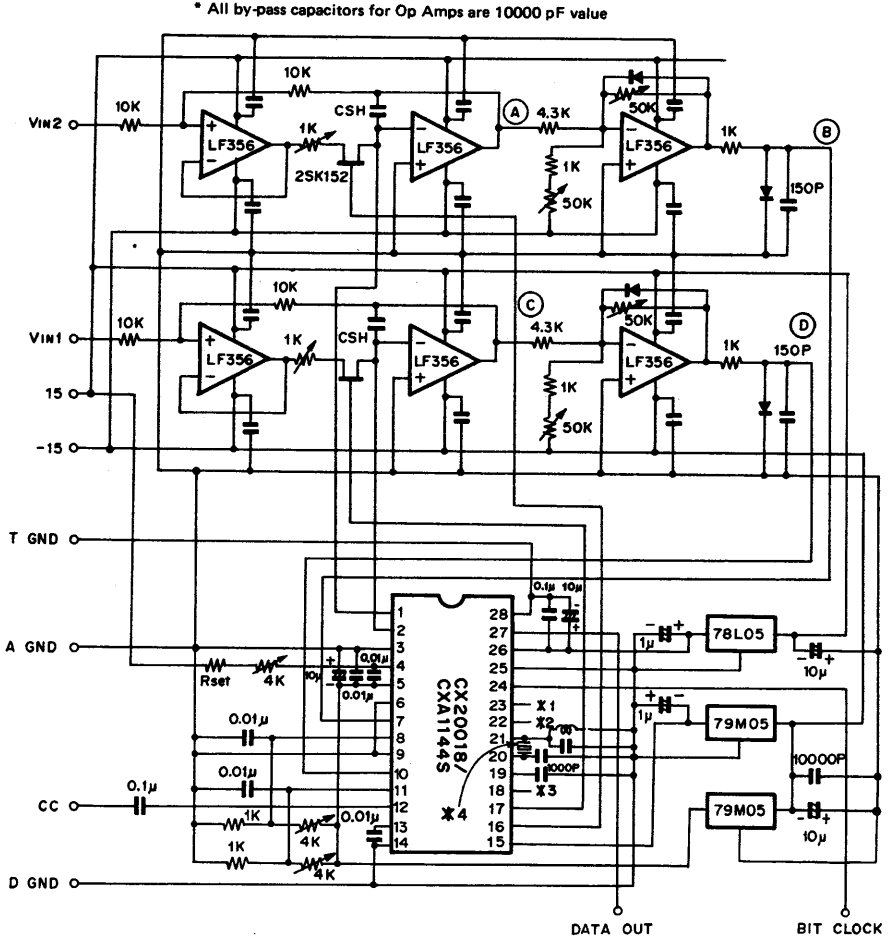
$T_1 \geqq \frac{16}{f_{BCLK}}$, $T_2 \geqq 8\mu$sec → Conversion time can be 8μsec.

(Example 3)
If f_{BCLK} = 4 MHz,
$fcc \leqq$ Min ($\frac{100-X}{795}$MHz, $\frac{X}{400}$ MHz)

$\frac{79500}{100-X} fcc \leqq f_{MCLK} \leqq 100$ MHz

$T_1 \geqq 4\mu$sec, $T_2 \geqq \frac{795}{f_{MCLK}} (\geqq 8\mu sec)$→Short conversion time can be obtained.

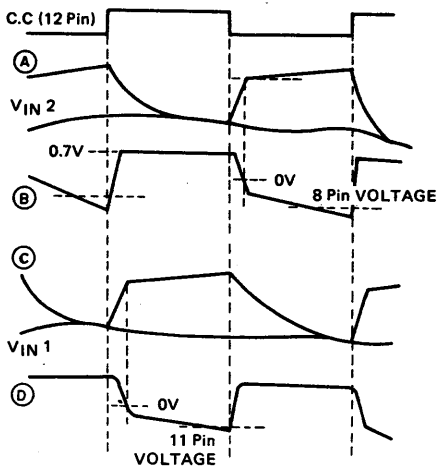
(2) In case of CXA1144S
The same as CX20018 except $f_{MCLK} \leqq 95$ MHz.



Typical Application

16 Bit AD Convertor Peripheral Circuit (Stereo Mode)

Wave Form



* 1, 2, 3: See to Page 13 and 14.

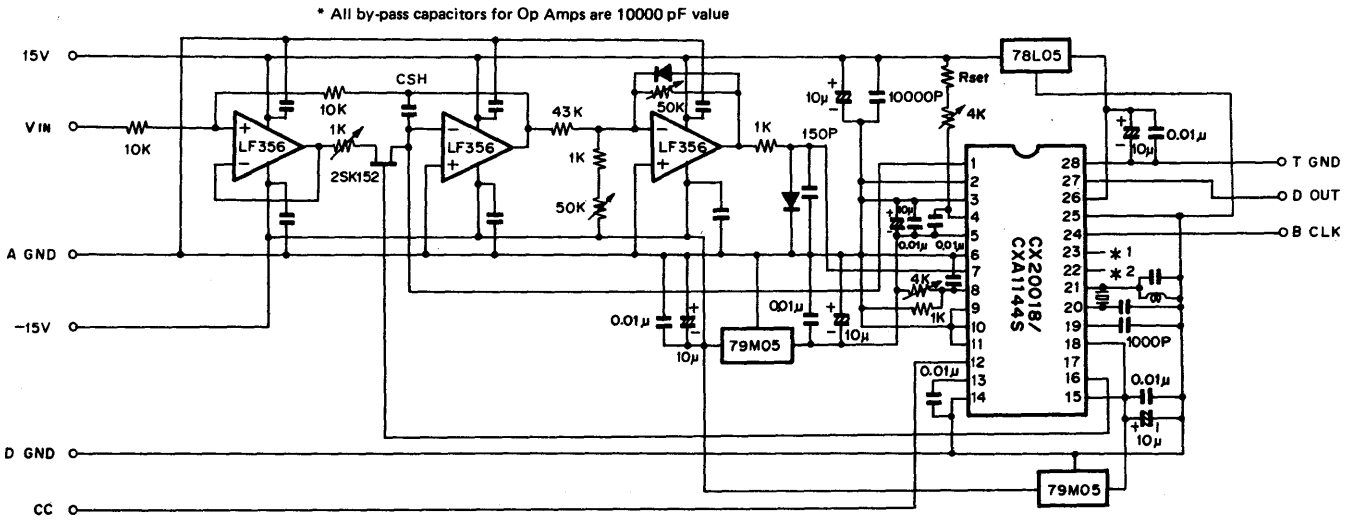
* Rset, CSH: See to Page 16.
(Rset = 42 kΩ when Iset = 410 μA, Rset = 22 kΩ when Iset = 750 μA.)

*4: HC43/U (American KSS), etc.

Fig. 5 16 bit A/D Converter Peripheral Circuit (Stereo Mode)

Typical Application – Monaural Mode

16 Bit AD Convertor Peripheral Circuit (Monaural Mode)



* 1, 2: See to Page 13 and 14.
* Rset, CSH: See to Page 16 (Rset = 42 kΩ when Iset = 410 μA, Rset = 22 kΩ when Iset = 750 μA).

Fig. 6 16 bit A/D Converter Peripheral Circuit (Monaural Mode)

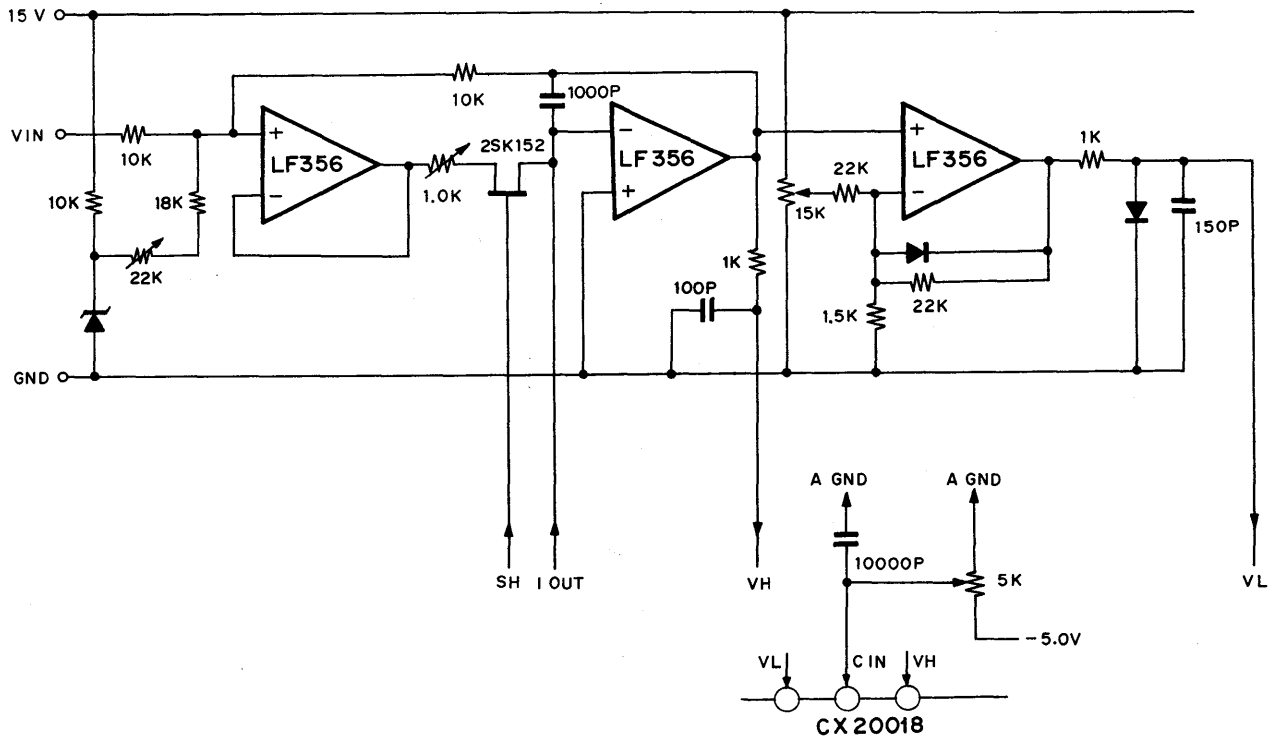
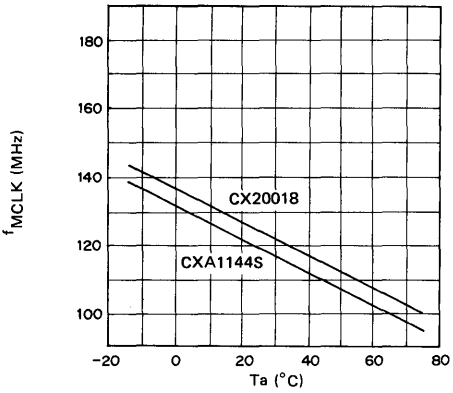
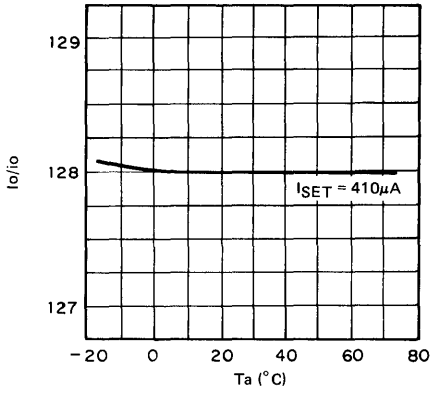


Fig. 7 Application Circuit (Non-inverting Circuit)

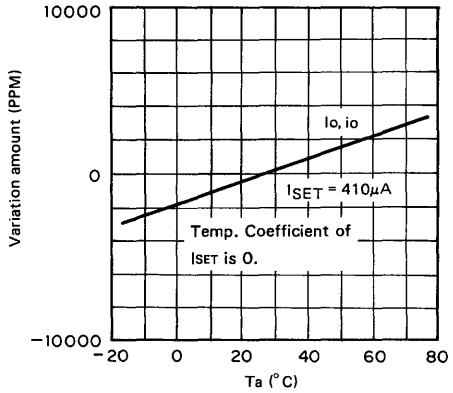
fMCLK temperature characteristics



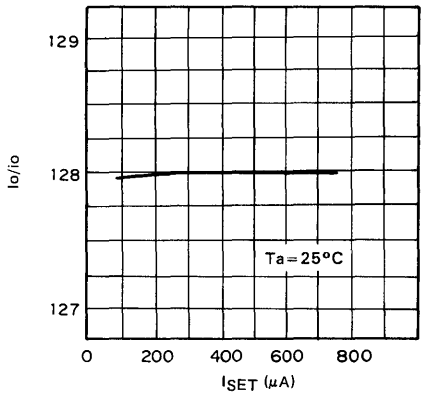
Current ratio temperature characteristics



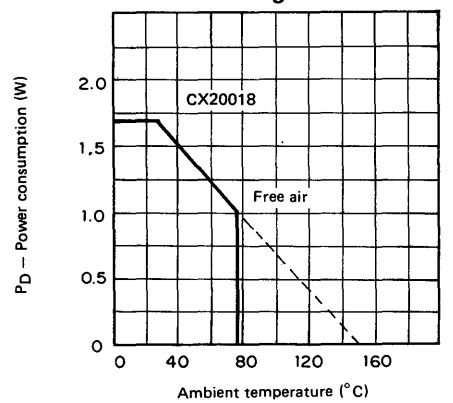
Output current temperature characteristics



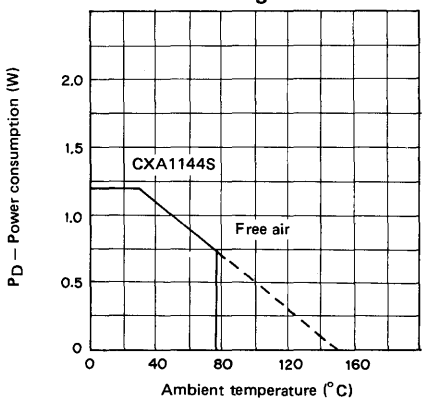
Current ratio vs. ISET



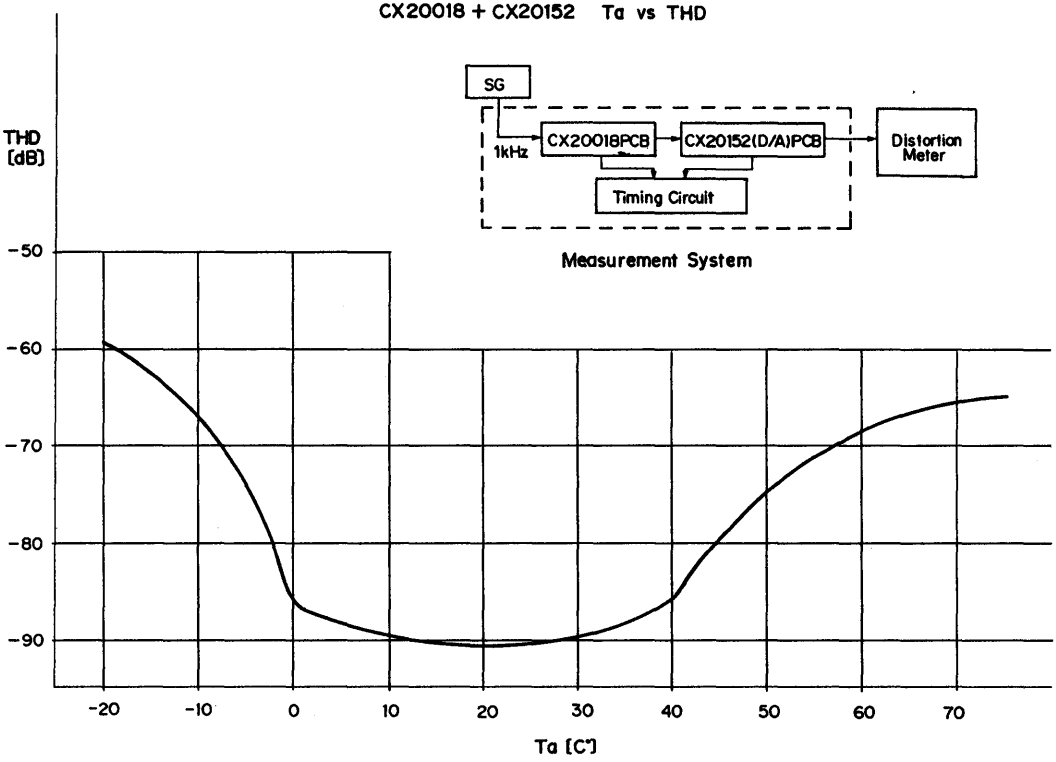
Derating curve



Derating curve

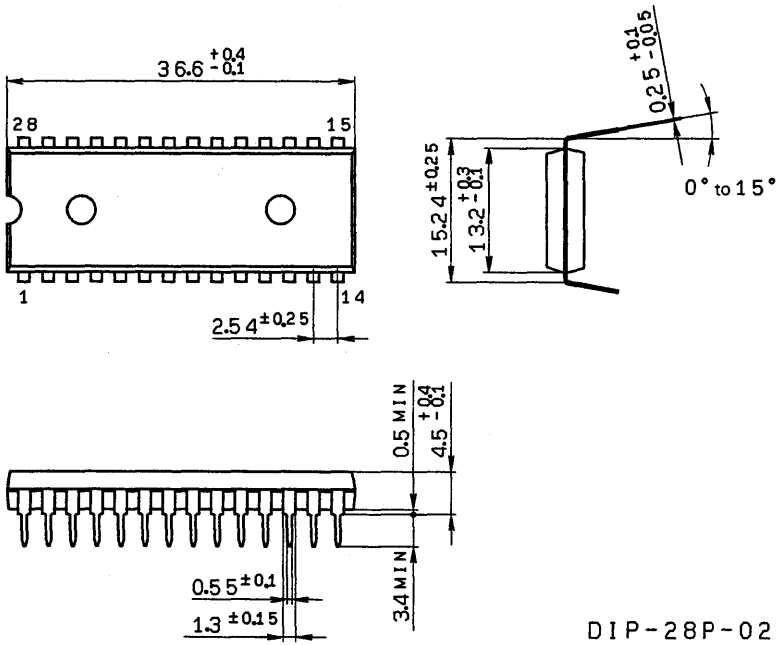


CX20018 + CX20152 Ta vs THD



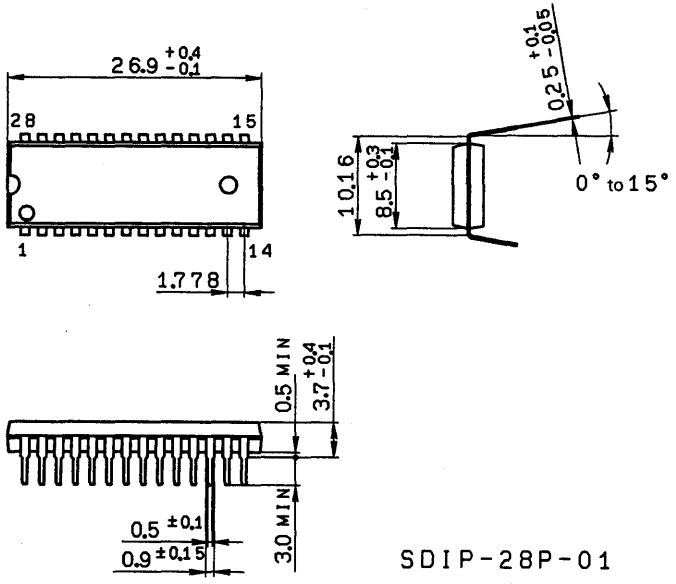
Package Outline **Unit: mm**

CX20018 28 pin DIP (Plastic) 600 mil 4.0g



DIP-28P-02

CXA1144S 28 pin SDIP (Plastic) 400 mil 1.7g



SDIP-28P-01

Dual 16 bit 44 kHz Multiplexed D/A Converter

Description

The CX20133 is a 16 bit D/A converter IC for PCM audio using the integrating formula. Analog signal is reproduced from the 16 bit digital signal by combining an integrator, analog switch and low-pass filter to the IC exterior. Following circuits are also built-in.

- Integrating current output
- Two channels of discharge signal output
- Level shifting for interface direct with TTL/MOS LSIs.
- Analog switch drive.

Features

- Miniature flat package requires only small mounting area.
- Conversion frequency of 44.1 kHz.
- Serial data input.
- Low distortion factor typically at 0.003%.

Structure

- Bipolar Silicon Monolithic IC

Absolute Maximum Ratings (Ta = 25°C)

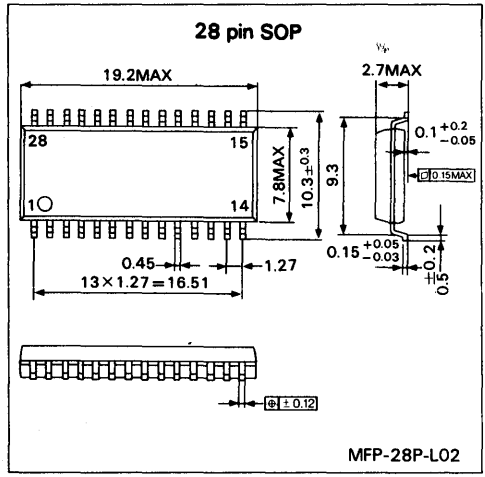
• Supply voltage	V_{CC} to V_{EE}	12	V
• Operating temperature	T_{opr}	−10 to +75	°C
• Storage temperature	T_{stg}	−50 to +125	°C
• Allowable power dissipation	P_D	1.1	W

Recommended Operating Conditions

• Supply voltage	V_{CC}	5 ± 0.25	V
	V_{EE}	−5 ± 0.25	V

Package Outline

Unit: mm



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Block Diagram

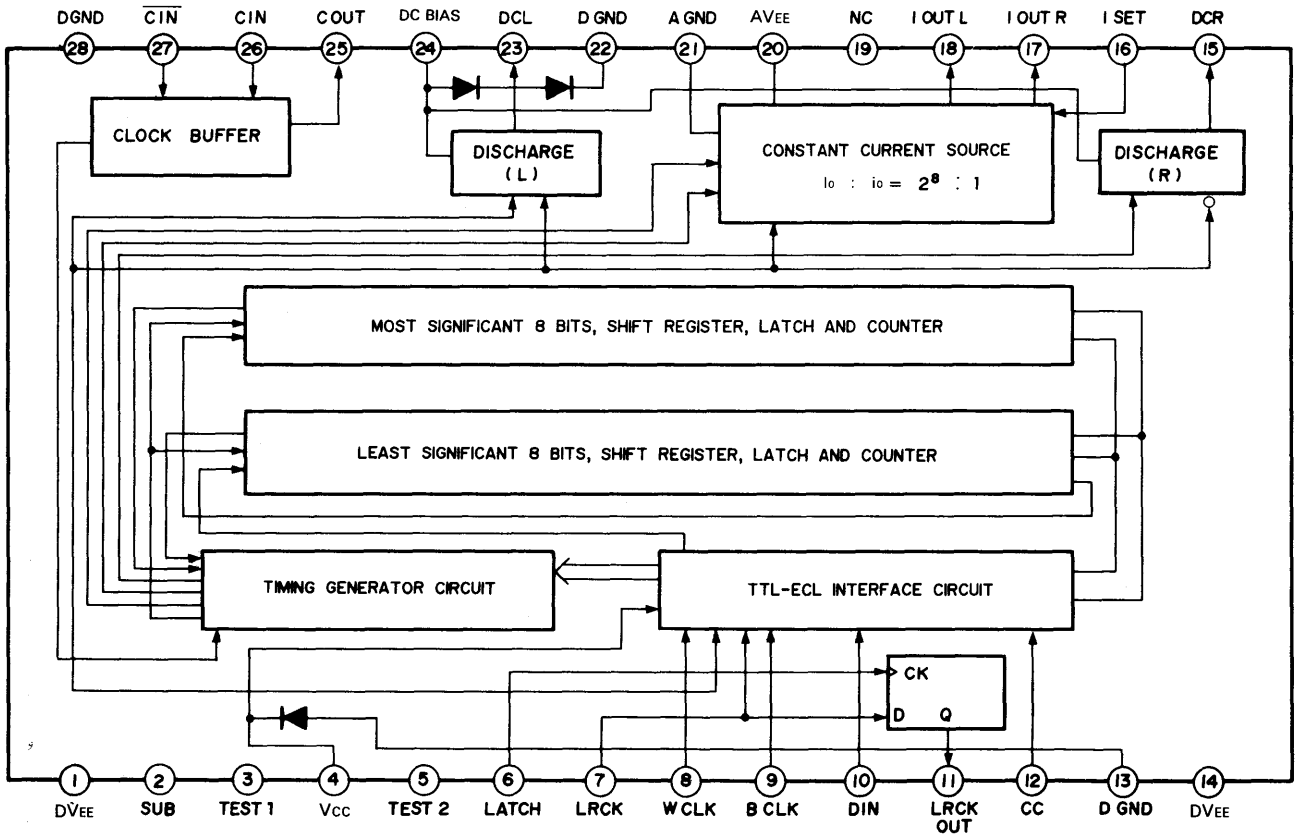


Fig. 1

SONY

Pin Description

No.	Symbol	Description
1	DV_{EE}	Power supply pin for the digital circuit. Applied with −5 V.
2	SUB	IC substrate. Always connected to 1 pin.
3	TEST 1	Test pin, normally open.
4	V_{CC}	Power supply pin for the digital circuit. Applied with +5 V.
5	TEST 2	Test pin, normally open.
6	LATCH	Clock pin of D-type clutch.
7	LRCK	LRCK input pin.
8	WCLK	WCLK input pin.
9	BCLK	BCLK input pin.
10	DIN	DIN (data input pin).
11	LRCK OUT	LRCK output pin.
12	CC	CC input pin.
13	DGND	Ground pin for the digital circuit.
14	DV_{EE}	Power supply pin for the digital circuit. Applied with −5 V.
15	DCR	Output pin of R-channel discharge driving signal.
16	ISET	Pin for setting integration current.
17	IOUTR	Output pin for R-channel current.
18	IOUTL	Output pin for L-channel current.
19	NC	No connection.
20	AV_{EE}	Power supply pin for the analog circuit.
21	AGND	Ground pin for the analog circuit.
22	DGND	Ground pin for the digital circuit.
23	DCL	Output pin for L-channel discharge driving signal.
24	DCBIAS	Bias pin for the discharge circuit.
25	COUT	Output pin for the clock oscillator.
26	CIN	Positive input pin for the clock oscillator.
27	$\overline{CIN}$	Negative input pin for the clock oscillator.
28	DGND	Ground pin for the digital circuit.

Electrical Characteristics

(Ta = 25°C, V_{EE} = −5.0V, V_{CC} = 1.0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Circuit current	I_{EE}	1, 2, 14, 20	−112	−85		mA	1
Circuit current	I_{CC}	4		9.5	12.5	mA	1
Input threshold voltage	V_{TH}	6, 7, 8, 9, 10, 12		2.1		V	
High-level input voltage	V_{IH}	6, 7, 8, 9, 10, 12	2.8			V	
Low-level input voltage	V_{IL}	6, 7, 8, 9, 10, 12			0.8	V	
High-level input current	I_{IH}	6, 7, 8, 9, 10, 12 V_{IH} = 4.5V			500	μA	
Low-level input current	I_{IL}	6, 7, 8, 9, 10, 12 V_{IL} = 0V			500	μA	
High-level output voltage	V_{LRCKH}	11 Pin 7 = 4.5V I_{OH} = −100μA Pin 6:1 clock input:0V−5V−0V	2.7			V	
Low-level output voltage	V_{LRCKL}	11 Pin 7 = 0V I_{OL} = 100μA Pin 6:1 clock input: 0V−5V−0V			−2.7	V	
Clock input bias voltage	V_{CIN}	26, 27		−1.3		V	
Clock high-level output voltage	V_{CCR}	25		−0.8		V	
Clock low-level output voltage	V_{COL}	25		−1.6		V	
Current output pin leak	$I_{O\ LEAK}$	17, 18 Pins 17, 18: voltage = 0V when current output is off.			1.5	μA	
I_{OUT} output current	I_{OUT}	17, 18 Pins 17, 18: voltage = 0V Pin 16 I_{SET} = 500μA (I_{OUT} = Io − io)		2.008		mA	
Current ratio*1	Io/io	17, 18 Pin 16 I_{SET} = 250μA	255.0	256.0	257.5	—	2
Discharge circuit current dissipation	I_{DC}	24 Set Pin 24 to 0V.	1.35	1.9	2.5	mA	
Discharge circuit high-level output voltage	V_{DCH}	15, 23 Pin 24 voltage = 1.4V Load current = −100μA	0.27	0.45	0.77	V	
Discharge circuit low-level output voltage	V_{DCL}	15, 23 Pin 24 voltage = 1.4V Load current = −100μA		−4.2	−3.5	V	
Maximum I_{SET} current	$I_{SET\ MAX}$	16 In the range when the $I_{OUTL(R)}$ current ratio satisfies 255<Io/io<257			575	μA	
Distortion factor	THD	Both right and left, 0dB (full scale) reproduction 680Hz		0.003	0.005	%	3
		Both right and left, −20dB reproduction 680Hz		0.02	0.025	%	3
Operating clock frequency	f_{CLK}	Self-activating/Activated			36	MHz	

Note 1) Ground Pins 13, 17, 18, 21, 22, 24 and 28. Connect Pin 16 via a resistor of 5.1 kΩ and keep other pins open.

2) Io and io must satisfy the relation below in the Current Ratio Test Circuit (Fig. 3):
$-3.9\ (mV) < 1\ (k\Omega) \times Io\ (\mu A) - 256\ (k\Omega) \times io\ (\mu A) < 5.9\ (mV)$

3) See the Test Circuit (Fig. 2).
Conversion frequency: 44.1 kHz
Input data: Use the 16 bit full-scale data (0 dB) generated by the data generator.
Distortion meter: Use the HP339A (with all filters on) or the like provided with 80 kHz LPF, 30 kHz LPF and 400 Hz HPF.

*1 In the Current Ratio Test Circuit (Fig. 3),
$-3.9(mV) < 1(k\Omega) \times Io(\mu A) - 256(k\Omega) \times io(\mu A) < 5.9(mV)$

Description of the Conversion Operation

(1) Data call (BCLK, DIN, WCLK, LRCK). Refer to Fig. 1.

The data comes in 16 bit serial signal with 2's compliment. The data is sent sequencially into the IC beginning from MSB in sync with the rise of the bit clock (BCLK). (The data change represents the BCLK fall).

When the word clock (WCLK) is changed from the high-level to low-level at the 17th fall of BCLK, the 16 bit data is transferred from the shift register to the latch by the fall signal.

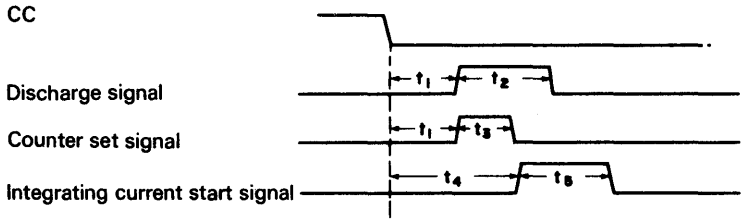
When the CX20133 is used in the stereo mode, data from other channels are sent in from the 17th BCLK.

In the stereo mode, Rch data is called when LRCK at the low level and Lch data is called in when the LRCK is at the high level. IOUTL and DCL operate only when LRCK is at the low level and IOUTR and DCR operate only when LRCK is at the high level.

(2) Conversion operation (CC, LRCK, CIN, IOUTL, IOUTR, DCL, DCR)

When more than 3 clocks are input from the clock input (CIN) with conversion command at the high level, all inner timing circuits are reset.

After resetting, the inner timing circuit starts operation when a clock is input from CIN with CC at the low level. The three signal generated this way are the discharge signal, counter set signal and integrating signal. Time of these three signals is determined depending on the clock cycle and their number of quantity:



$t_1 = 34 \times \tau o$
$t_2 = 67 \times \tau o$
$t_3 = 31 \times \tau o$
$t_4 = 65 \times \tau o$
t_5 Min $= 45 \times \tau o$ (input data 01 to 1)
t_5 Max $= 302 \times \tau o$ (input data 10 to 0)

The counter set signal is to set the data input to the latch to the counter and it is not output externally.

The discharge signal is output from DCL and DCR and it is controlled by LRCK. It is output from DCL when LRCK is at the low level and from the DCR when LRCK is at the high level.

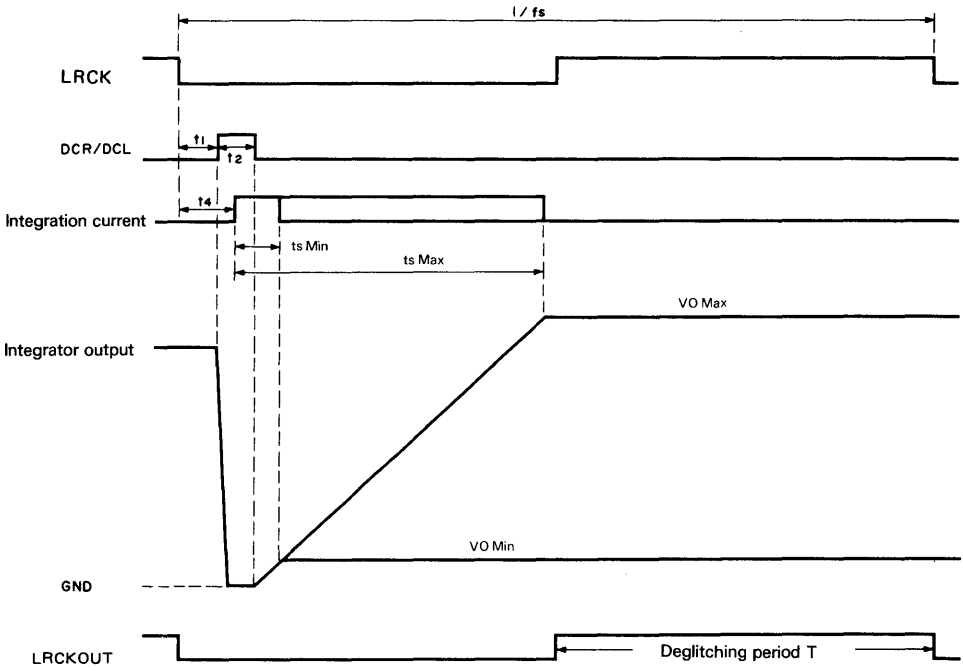
By the integrating current start signal, the upper current Io and lower current io start flowing. The counter starts counting from the preset value simultaneously when the discharge signal is off, measures the 11 offsets after completion of counting and outputs a signal to stop the integrating current.

The t5 value is varied between 0 and 255 by the preset input data in the counter.

Therefore, the conversion time from the start of low CC level to the completion of integrating requires t4 + t5 sec max.

The integrating current, like the discharge signal, is controlled by LRCK; IOUTL is output when LRCK is at the low level and IOUTR is output when LRCK is at the high level.

The Relation between Sampling Frequency fs and Clock



The maximum and minimum values of the integration voltage output, V_O Max and V_O Min, are expressed as follows:

$$V_O\,Max = \frac{I_O}{C} * \tau_O * 267 + \frac{i_O}{C} * \tau_O * 266 \qquad (t_4 + t_5\,Max)$$

$$V_O\,Min = \frac{I_O}{C} * \tau_O * 12 + \frac{i_O}{C} * \tau_O * 11 \qquad (t_4 + t_5\,Min)$$

where f_{CLK} is a clock frequency and τ is a period.

The integration voltage is held by the capacitor C in the integrator when the current is switched off. This voltage is used as D/A conversion output during the deglitching period T which is given according to the settling time of the deglitching circuit.

The relation between the conversion frequency fs and the clock frequency f_{CLK} is given as below assuming that the conversion time and deglitching period are equivalent:

$$fs = \frac{f_{CLK}}{2 \times (t_4 + t_5\,Max)} = \frac{f_{CLK}}{734}$$

where f_s=44.1 kHz results in 32.4 MHz of f_{CLK}.

It is, however, recommendable to specify fs as the follow for the practical use because a settling time of 0.5 to 1.0 μs is required for the integrator after the current for t_5 disappears:

$$fs = \frac{f_{CLK}}{2(t_4 + t_5\,Max + 1.0\ (\mu s)) + T}$$

(3) Integration current setting (ISET, IOUTL, LOUTR)

Integration current is determined by a constant current value input through the ISET pin, which is given as below:

$$\text{IOUTL (R)} = I_o + i_o$$
$$= (4 + \frac{1}{64})\ \text{ISET}$$

where i_o and I_o are integration currents corresponded to the ILSB and 2^8•LSB, respectively.

If D_0 and D_{15} are specified as MSB and LSB, respectively, integrator output voltage V_o is given by the following equation:

$$V_o = \frac{I_o}{C}(D_0 * 2^7 + \overline{D}_1 * 2^7 + \cdots\cdots + \overline{D}_7 * 2^0 + 12)\,\tau_0$$
$$+ \frac{i_o}{C}(\overline{D}_8 * 2^7 + \overline{D}_9 * 2^6 + \cdots\cdots + \overline{D}_{15} + 2^0 + 11)\,\tau_0$$

where $\text{ISET} = 500\mu\text{A}$, $\tau_0 = \frac{1}{35\ (\text{MHz})} = 28.6$ (ns) and C = 2000 pF result in the maximum output voltage V_o Max of the integrator when any of a value from 10 to 0 is given as an input data. Based on the relations below,

$I_o = 4 \cdot \text{ISET}$

$i_o = \frac{1}{64} \cdot \text{ISET}$,

V_o Max is calculated as the follow:

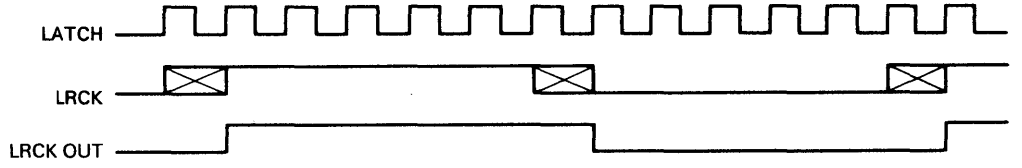
$$V_o\,\text{Max} = \frac{2.0 \times 10^{-3}}{2000 \times 10^{-12}} * 267 * 28.6 \times 10^{-9}$$
$$+ \frac{500 * 10^{-6}/64}{2000 \times 10^{-12}} * 266 * 28.6 \times 10^{-9}$$
$$= 7.67\ (\text{V})$$

(4) Operation of LRCK OUT

The LRCK OUT is an output for the analog switch IC (equivalent to MC14053B) drive to clip the output converted by the CX20133 and integrator as a PAM wave.

A PAM wave jitter may cause a conversion error and a D-type flip-flop is incorporated to eliminate this jitter; the LATCH input is used as a clock for the flip-flop.

This D-type flip-flop changes the output status in sync with the clock rise. The LRCK OUT operates only when +5 V is applied to Vcc. The output voltage level ranges from −2.7 V to +2.7 V enough to drive the CMOS analog switch effectively.



Timing of LATCH, LARCK and LRCKO

(5) Clock input/output pin (COUNT, CIN, $\overline{\text{CIN}}$)

The clock buffer consists of a circuit equivalent to a general-purpose ECL logic circuit, with its input pin biased by the internal bias circuit. The (≈ -1.3 V) output amplitude level is 0.8 V.

(6) Bias pin (DVEE, SUB, DGND, VCC, AVEE, AGND, DC BIAS)

SUB is used at the common potential with DVEE. A standard value for the DVEE and AVEE is -5.0 V.

The CX20133 is devised so that it can operate when voltage at the digital input pin has a value between either 0 to -5 V or 0 to $+5$ V. When operated with an input between 0 and $+5$ V, $+5$ V must be applied to VCC. In this case, LRCK OUT is output as mentioned above.

When operated with an input between 0 to -5 V, VCC must be set open.

DC BIAS is for the bias circuit of the discharge signal output circuit. Supply current of (2.5 mA $+\alpha$) from a power supply of $+5$ V or above, because this pin requires approx. 2.5 mA current as a standard value. The potential at the pin is biased at 2 Vf.

A value α can be determined according to the following procedures. Approx. 0.5 mA current is necessary to retain 2 Vf (approx. 1.4 V) at this pin. The maximum current that flows through the load resistor RL attached to DCR (15 Pin) and DCL (23 Pin) is calculated as the follow:

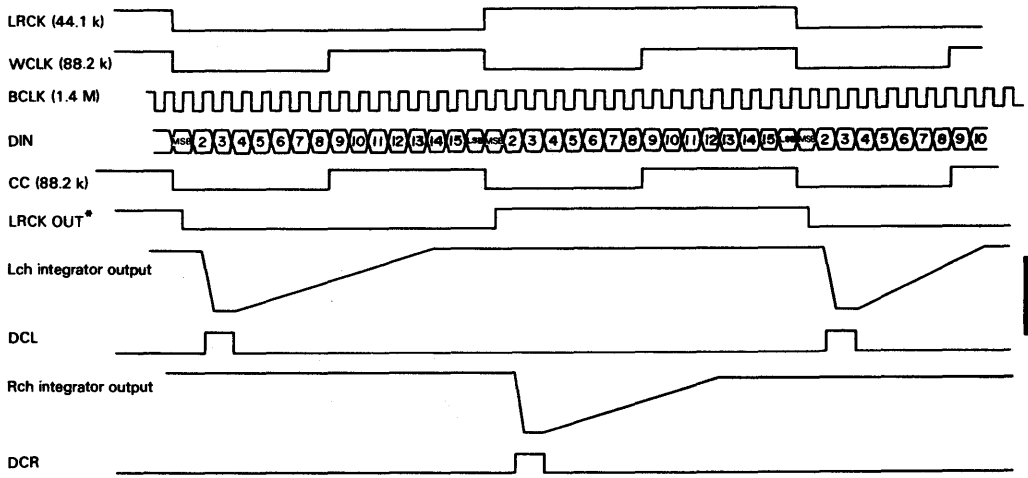
$$1/R_L \times (V_{DCH} + |DV_{EE}|)$$

The above equation results in 1.15 V where $R_L = 4.7\ k\Omega$, $V_{DCH} = 0.4$ V and $DV_{EE} = -5$ V are specified. Then α is calculated as

$$\alpha = 0.5 + 1.15 = 1.65\ (mA),$$

and required current is then obtained as 4.15 mA. Recommended value is 5 mA for $R_L = 4.7\ k\Omega$.

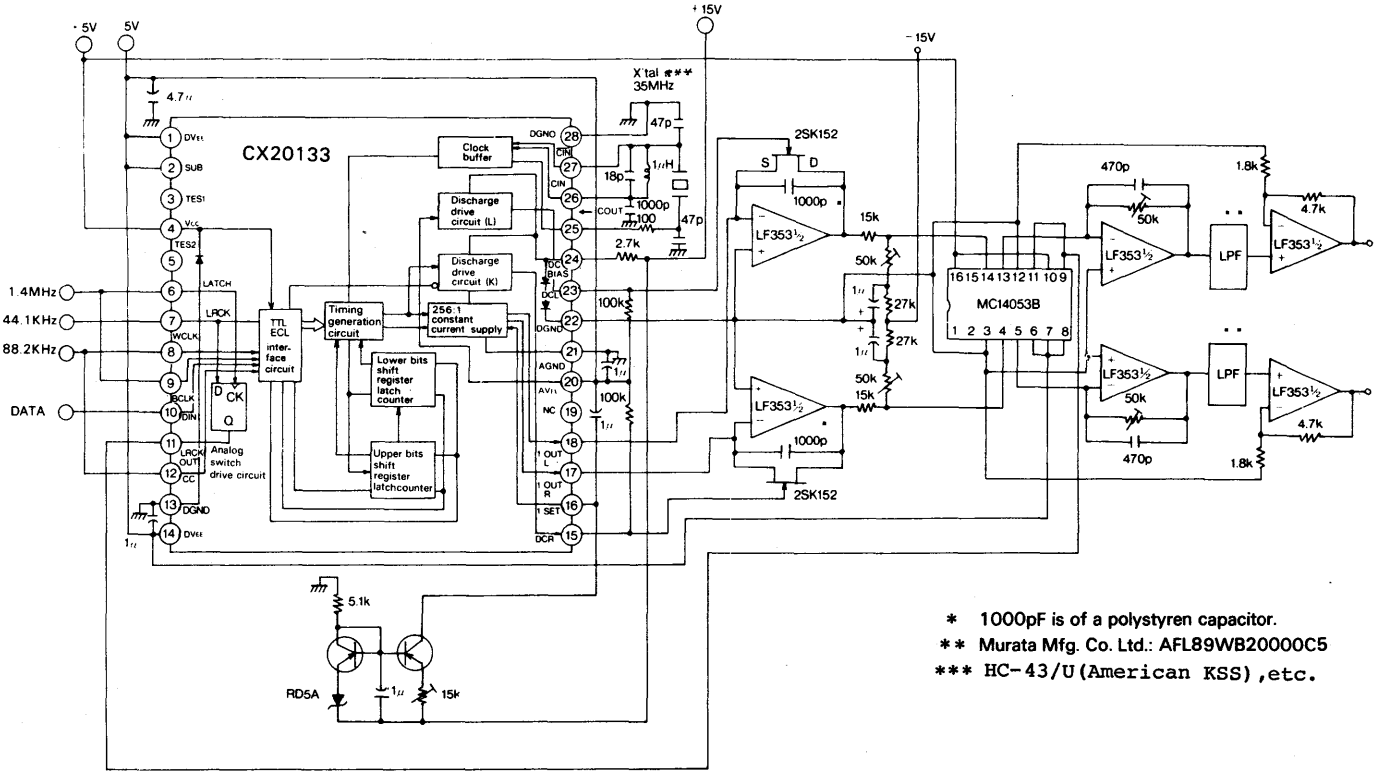
Timing Chart in the Stereo Mode



* When LATCH input is used as BCLK.

Fig. 1

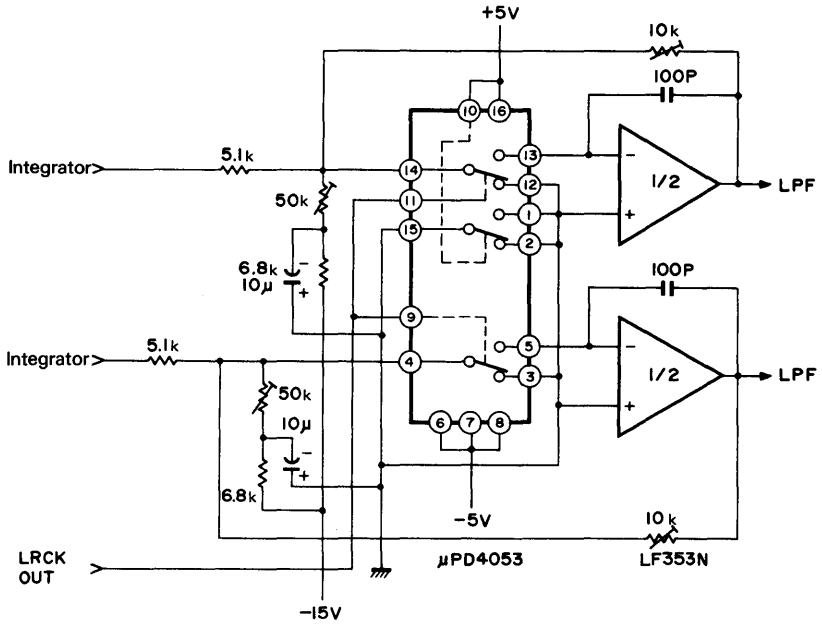
Application Circuit and Test Circuit



* 1000pF is of a polystyren capacitor.
** Murata Mfg. Co. Ltd.: AFL89WB20000C5
*** HC-43/U(American KSS),etc.

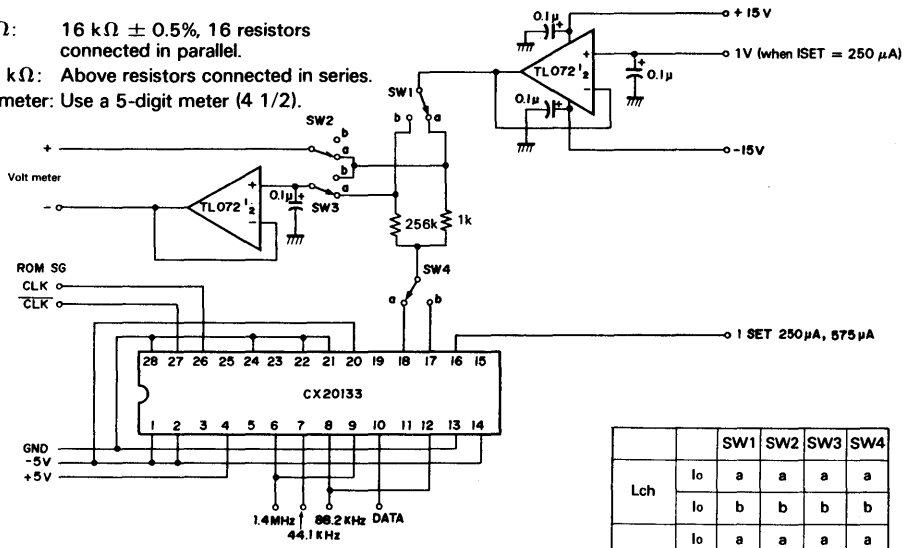
Fig. 2

Sample/Hold Circuit for Deglitching



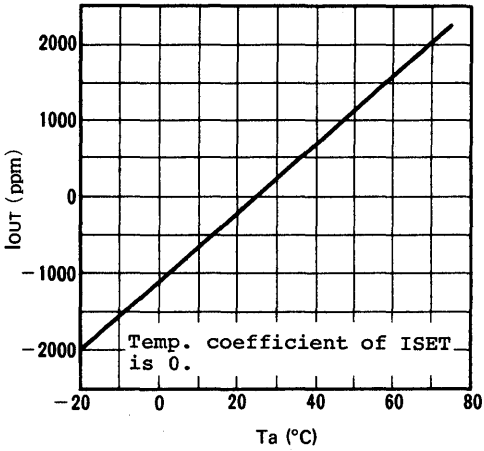
Current Ratio Test Circuit

1 kΩ: 16 kΩ ± 0.5%, 16 resistors connected in parallel.
256 kΩ: Above resistors connected in series.
Voltmeter: Use a 5-digit meter (4 1/2).

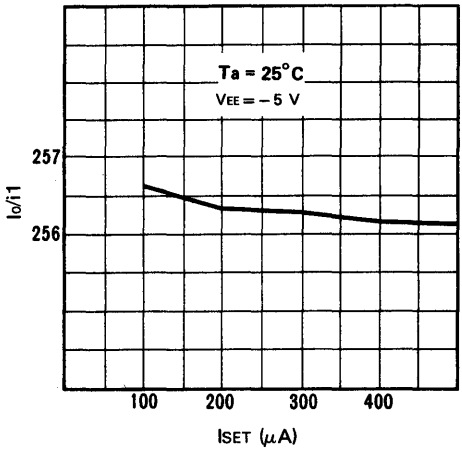


		SW1	SW2	SW3	SW4
Lch	Io	a	a	a	a
	Io	b	b	b	b
Rch	Io	a	a	a	a
	Io	b	b	b	b

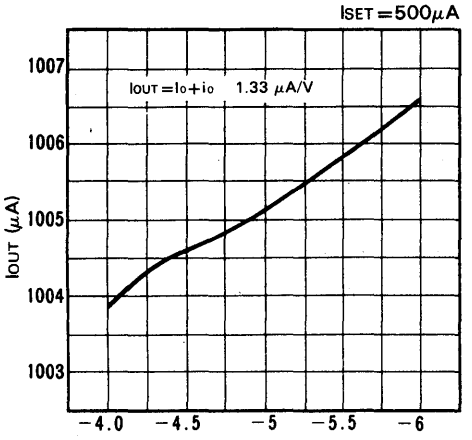
Temperature characteristics of I_{OUT} (I_O+i_O) (R, Lch common)



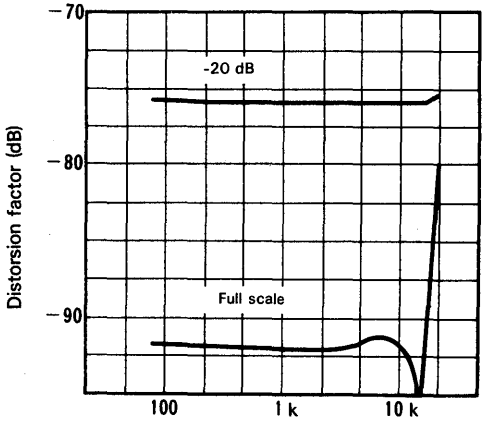
I_O/i_O vs. I_{SET}



Output current vs. Supply voltage (V_{EE})



Distortion factor



Dual 16 bit, 88 kHz, Multiplexed D/A

Evaluation Board Available — CX20152PCB

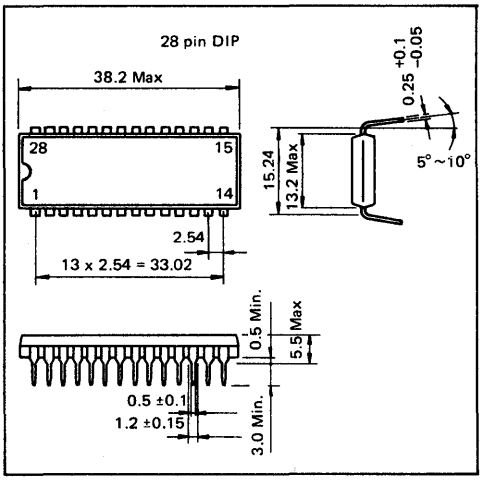
Description

CX20152 is a 16-bit D/A converter IC for PCM audio. It uses an integration system consisting of the following circuits.

- Clock signal generator
- TTL-ECL interface circuit
- Discharge drive circuit
- Analog switch drive circuit
- 1/4 frequency divider output circuit

By adding an integrator, analog switch and low pass filter externally to the IC, analog signal is reproduced from the 16-bit digital data.

Package Outline Unit: mm



Features

- Conversion frequency 88.2kHz
- Serial data input
- Low distortion factor 0.003% (typ.)

Structure

Bopolar Sillicon Monolithic IC

Absolute Maximum Rating

●Supply voltage	V_{CC} to V_{EE}	12	V
● Operating temperature	Topr	−20 to +75	°C
● Storage temperature	Tstg	−55 to +150	°C
● Allowable power dissipation	P_D	2.1	W

Recommended Operating Conditions

● Supply voltage	V_{CC}	5 ±0.25	V
	V_{EE}	−5 ±0.25	V

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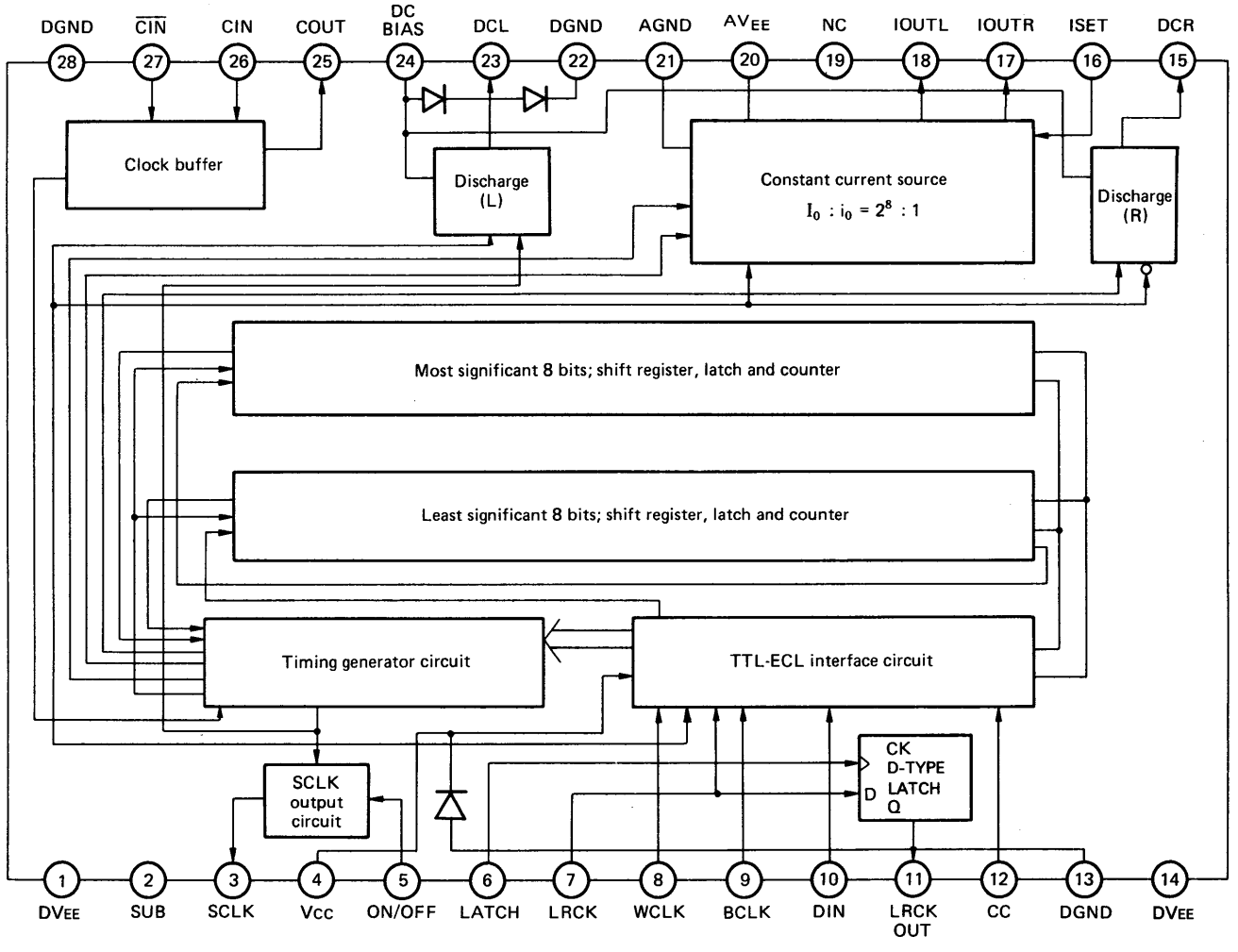
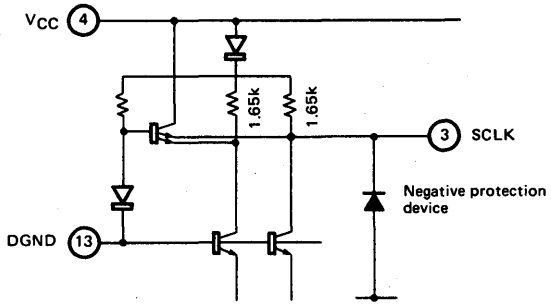
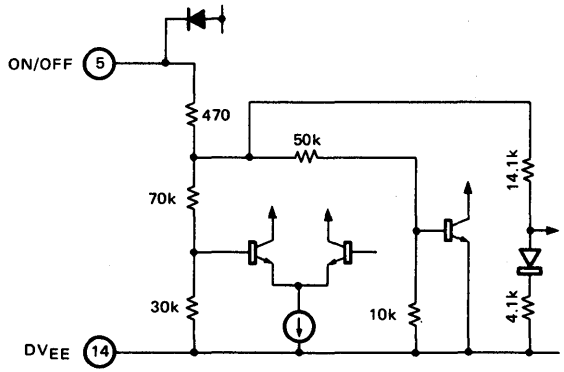
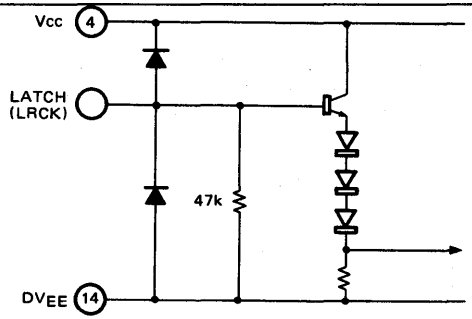
Block Diagram

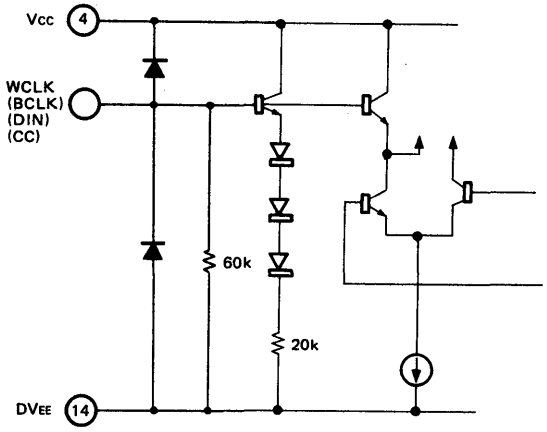
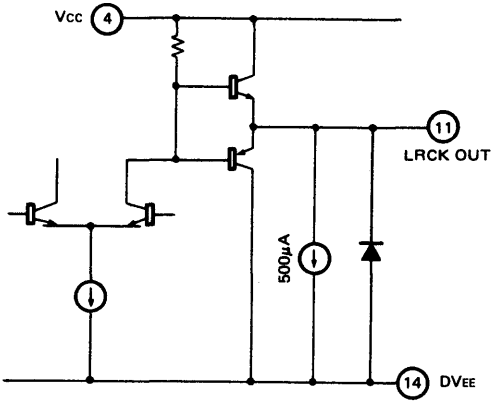
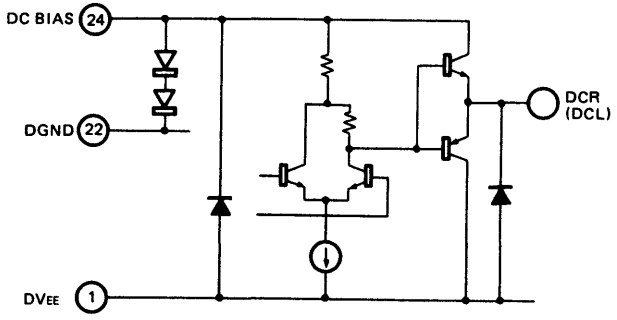


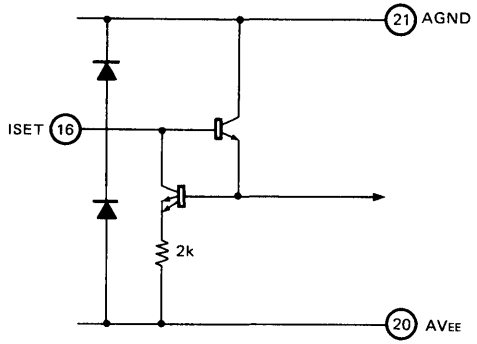
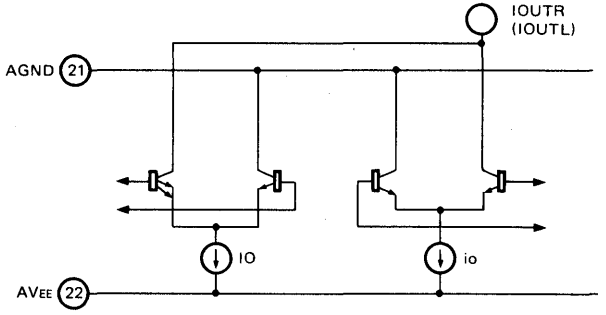
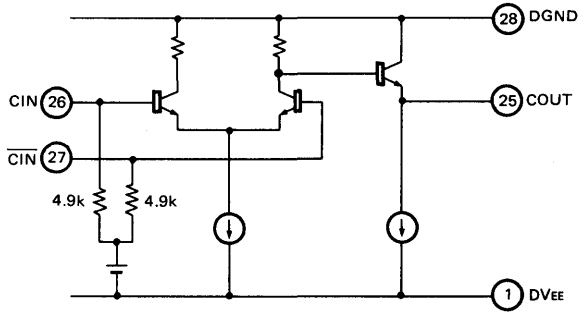
Pin Description

No.	Symbol	Description
1	DVEE	Digital VEE: −5V
2	SUB	IC substrate: Be sure to connect to Pin 1.
3	SCLK	System clock output pin
4	VCC	Digital VCC: +5V
5	ON/OFF	Pin to determine the system clock on/off
6	LATCH	Clock pin of D type latch
7	LRCK	LRCK input pin
8	WCLK	WCLK input pin
9	BCLK	BCLK input pin
10	DIN	DIN (data input pin): MSB first
11	LRCK OUT	LRCK output pin
12	CC	CC input pin
13	DGND	Digital ground
14	DVEE	Digital VEE: −5V
15	DCR	Right channel discharge drive signal output pin
16	ISET	Integration current setting pin
17	IOUTR	Right channel current output pin
18	IOUTL	Left channel current output pin
19	NC	No connection
20	AVEE	Analog VEE
21	AGND	Analog GND
22	DGND	Digital GND
23	DCL	Left channel discharge drive signal output pin
24	DC BIAS	Discharge circuit bias pin
25	COUT	Clock generator output pin
26	CIN	Clock generator positive input pin
27	$\overline{\text{CIN}}$	Clock generator negative input pin
28	DGND	Digital GND

CX20152 Input/Output Pin Equivalent Circuits

No.	Symbol	Equivalent Circuits
1	DVEE	
2	SUB	
3	SCLK	
4	Vcc	
5	ON/OFF	
6	LATCH	
7	LRCK	

No.	Symbol	Equivalent Circuit
8	WCLK	
9	BCLK	
10	DIN	
12	CC	
11	LRCK OUT	
13	DGND	
14	DVEE	
15	DCR	
23	DCL	
24	DC BIAS	

No.	Symbol	Equivalent Circuits
22	DGND	
16	ISET	
17	IOUTR	
18	IOUTL	
19	NC	
20	AVEE	
21	AGND	
25	COUT	
26	CIN	
27	$\overline{\text{CIN}}$	
28	DGND	

Electrical Characteristics

($Ta = 25°C$, $V_{EE} = -5.0V$, $V_{CC} = 5.0V$)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Circuit current	I_{EE}	1, 2, 14, 20 Pins 4, 5 = 5V	−125	−95		mA
Circuit current	I_{CC1}	4 Pin 5 = 5V (6, 7, 8, 9, 10, 12, GND)		12.6	15.5	mA
Circuit current	I_{CC2}	4 Pin 5 = 0V (6, 7, 8, 9, 10, 12, GND)		5.9	10.0	mA
Input threshold voltage	V_{TH}	6, 7, 8, 9, 10, 12		2.1		V
High level input voltage	V_{IH}	6, 7, 8, 9, 10, 12	2.9			V
Low level input voltage	V_{IL}	6, 7, 8, 9, 10, 12			0.9	V
High level input current 1	I_{IH1}	5 $V_{IH} = 5V$		0.7	1.3	mA
High level input current 2	I_{IH2}	6, 7, 8, 9, 10, 12 $V_{IH} = 5V$		250	550	μA
Low level input current 1	I_{IL1}	5 $V_{IH} = 0V$		0.35	0.8	mA
Low level input current 2	I_{IL2}	6, 7, 8, 9, 10, 12 $V_{IL} = 0V$		120	550	μA
High level output voltage	V_{LRCKH}	11 With Pin 7 at 4.5V, set $I_{OH} = -100\mu A$ and input a clock of 0V–5V–0V to Pin 6.	2.7	4.2		V
Low level output voltage	V_{LRCKL}	11 With Pin 7 at 0V, set $I_{OL} = 100\mu A$ and input a clock of 0V–5V–0V to Pin 6.		−3.1	−2.7	V
SCLK output, high level	V_{SCLKH}	3 $I_{OH} = -10\mu A$	3.4	4.2		V
SCLK output, low level	V_{SCLKL}	3 $I_{OL} = 400\mu A$		0.5	1.6	V
Discharge circuit power dissipation current	I_{DCBIAS}	24 $V_{DCBIAS} = 0V$		1.9	2.5	mA
Discharge circuit high level output voltage	V_{DCH}	15, 23 Pin 24 voltage = 1.3V Load current = 1.2mA	0	0.4	0.65	V
Discharge circuit low level output voltage	V_{DCL}	15, 23 Pin 24 voltage = 1.3V Load current = 1.2mA		−4.2	−3.4	V
I_{SET} current	I_{SET}	16		0.5	1.0	mA
I_{OUT} output current	I_{OUT}	17, 18 Pins 17, 18: Voltage = 0V Pin 16: $I_{SET} = 500\mu A$ ($I_{OUT} = Io + io$)		2.008		mA
Clock input bias voltage	V_{CIN}	26, 27		−1.3		V
Clock high level output voltage	V_{COH}	25		−0.8		V
Clock low level output voltage	V_{COL}	25		−1.6		V
Current output pin leakage	Io LEAK	17, 18 Pins 17, 18: Voltage = 0V when the current output is off.			1.5	μA
Current ratio	Io/io	17, 18 Pin 16: $I_{SET} = 500\mu A$	255.0	256.0	257.5	—
Distortion factor	THD1	Both right and left; 0dB (full scale) when reproduced.		0.003	0.005	%
	THD2	Both right and left; −20dB when reproduced.		0.02	0.025	%
Operation clock frequency	f_{CLK1}	Both self-drive & external-drive Ta = −20 ~ +70°C		68	80	MHz
Operation clock frequency	f_{CLK2}	Both self-drive & external-drive Ta = −20 ~ +75°C		68	75	MHz

Description of Conversion Operation

(1) Data pickup (BCLK, DIN, WCLK, LRCK)

Data consist of 16-bit serial signals in 2's complement. They are transmitted into the IC sequentially from the MSB in synchornization with the rise edge of the bit clock (BCLK). (The BCLK delay will change the data. The falling edge changes the data.)

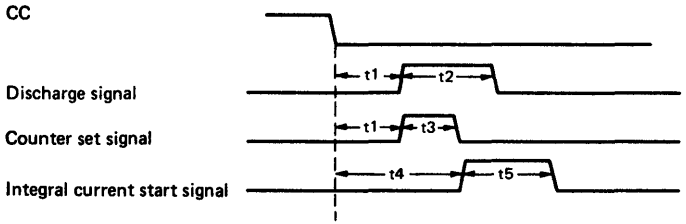
When the word clock (WCLK) is changed from high level to low level at the 17th BCLK, the 16-bit data is transferred from the shift register to the latch with the decay signal. When CX20152 is used in the stereo mode, other-channel data are transmitted from the 17th BCLK.

In the stereo mode, the Rch data is picked up when LRCK is at a low level and the Lch data is picked up when LRCK is at a high level. IOUTL and DCL operate only when LRCK is at a low level, and IOUTR and DCR operate only when LRCK is at a high level.

(2) Conversion operation (CC, LRCK, CIN, IOUTL, IOUTR, DCL, DCR)

When more than 3 clocks are fed from the clock input (CIN) with the conversion command (CC) at a high level, all the internal timing circuits are reset.

After the resetting, the internal timing circuit starts operation when a clock is input from CIN with CC at a low level. From this operation, three signals, Discharge, Counter set and Integral current Start, are generated. Timing of these signals is determined as follows by the clock interval τ_0 and its quantity.



$t1 = 35 \times \tau_0$

$t2 = 67 \times \tau_0$

$t3 = 31 \times \tau_0$

$t4 = 65 \times \tau_0$

$t5\ Min = 47 \times \tau_0$ (When the input data is 01 – 1)

$t5\ Max = 302 \times \tau_0$ (When the input data is 10 – 0)

The counter set signal is used to set the data input in the latch to the counter but does not output externally.

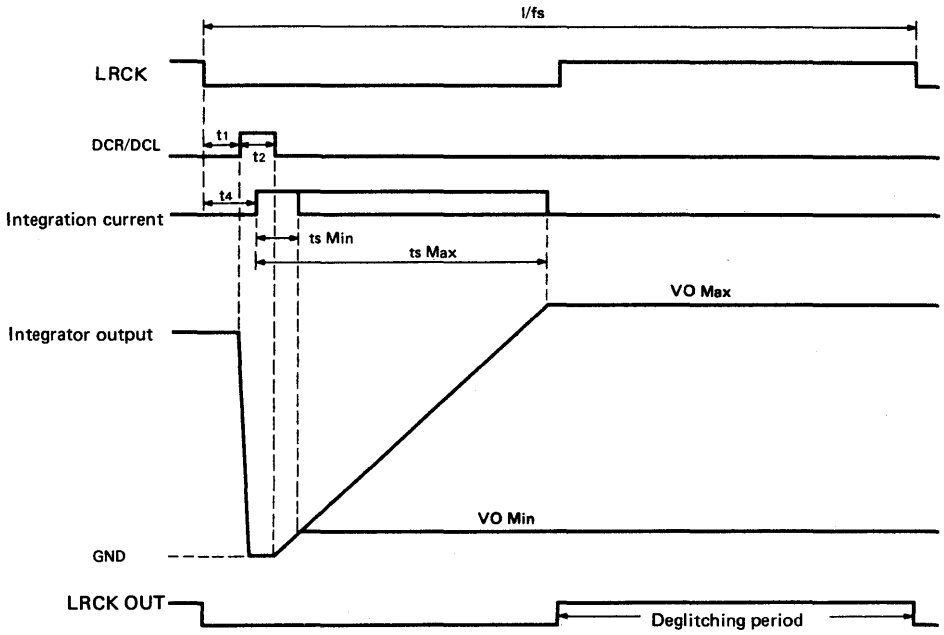
The discharge signal is output from DCL and DCR and controlled by LRCK. It is output from DCL when LRCK is at a low level and from DCR when LRCK is at a high level.

The integral current start signal starts the upper current Io and lower current io flowing. The counter starts counting from the preset value simultaneously when the discharge signal is off, counts 11 offsets after the end of the counting and outputs a signal to stop the integration current. The value t_5 is varied between 0 to 255 by the input data value preset to the counter.

Therefore, the time before the end of the integration after the low level has been set, i.e. the conversion time, requires the maximum ($t_4 + t_{5\ Max} = 367 \times \tau_0$) seconds.

The integration current of IOUTL is output, as with the discharge signal, when LRCK is at a low level; IOUTR is output when LRCK is at a high level.

(3) The relation between sampling frequency f_S and clock



The maximum and minimum values of the integration voltage output, $V_{O\ Max}$ and $V_{O\ Min}$, are expressed as follows.

$$V_{O\ Max} = \frac{I_0}{C} * \tau_o * 267 + \frac{i_0}{C} * \tau_o * 266 \qquad (t_4 + t_{S\ Max})$$

$$V_{O\ Min} = \frac{I_0}{C} * \tau_o * 12 + \frac{i_0}{C} * \tau_o * 11 \qquad (t_4 + t_{S\ Min})$$

where f_{CLK} is a clock frequency and τ is a period.

The integration voltage is held by the capacitor C in the integrator when the current is switched off. This voltage is used as D/A conversion output during the deglitching period T which is given according to the settling time of the deglitching circuit.
The relation between the conversion frequency f_S and the clock frequency F_{CLK} is given as below assuming that the conversion time and deglitching period are equivalent:

$$fs = \frac{f_{CLK}}{2 \times (t_4 + t_{S\ Max})} = \frac{f_{CLK}}{734}$$

where fs = 44.1 kHz results in 32.4 MHz of f_{CLK}

It is, however, recommendable to specify f_S as the follow for the practical use because a settling time of 0.5 to 1.0 μs is required for the integrator after the current for t_5 disappears:

$$fs = \frac{fCLK}{2(t_4 + t_5\ Max + 1.0(\mu s)) + T}$$

(4) Integration current setting (ISET, IOUTL, IOUTR)

Integration current is determined by a constant current value input through the ISET pin, which is given as below:

$$IOUTL\ (R) = I_0 + i_0 = (4 + \frac{1}{64})\ ISET$$

where i_0 and I_0 are integration currents corresponded to the ILSB and $2^8 \cdot$LSB, respectively.

If D_0 and D_{15} are specified as MSB and LSB, respectively, integrator output voltage V_0 is given by the following equation:

$$V_0 = \frac{I_0}{C}(D_0 * 2^7 + \overline{D}, * 2^7 + \ldots\ldots + \overline{D}_7 * 2^0 + 12)\tau_0$$

$$+ \frac{i_0}{C}(\overline{D_8} * 2^7 + \overline{D_9} * 2^6 + \cdots\cdots + \overline{D_{15}} * 2^0 + 11)\tau_0$$

where I_{SET} = 500 μA, $\tau = \frac{1}{35\ (MHz)}$ = 28.6 (ns) and C=2000 pF result in the maximum output voltage $V_{O\ Max}$ of the integrator when any of a value from 10 to 0 is given as an input data. Based on the relations below,

$$I_0 = 4 * I_{SET}$$

$$i_0 = \frac{1}{64} * I_{SET}$$

$V_{O\ Max}$ is calculated as the follow:

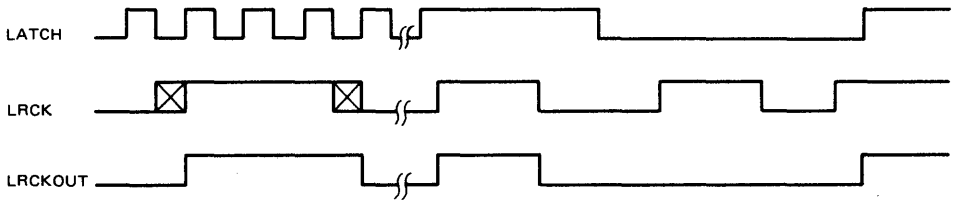
$$V_{O\ Max} = \frac{2.0 \times 10^{-3}}{2000 \times 10^{-12}} * 267 * 28.6 \times 10^{-9}$$

$$+ \frac{400 * 10^{-6}/64}{2000 \times 10^{-12}} * 266 * 28.6 \times 10^{-9}$$

$$= 7.67\ (V)$$

(5) LRCK OUT operation (LATCH, LRCK, LRCK OUT)

The LRCK OUT is a drive output for the analog switch IC (equivalent to MC14053B) to clip the output converted by CX20152 and the integrator so that the converted output can be a PAM wave. If the PAM wave has a jitter, a conversion error results. To absorb this jitter, a D-type latch is built-in and the LATCH input is used as its clock. The D-type latch sets the output state in synchronization with the rise of the clock(LATCH) and the logic high.



Timing of LATCH, LRCK and LRCKOUT

In the high-speed conversion (with sampling frequency of 88.2kHz), the clock frequency is as high as about 70MHz. This will affect the delay time of the analog switch IC. The delay time possibly becomes equal to t_1. Then, the last part of the PAM wave overlasps on the discharge time for CX20152 causing a considerable conversion error. In such a case, LRCK level can be fed through by keeping LATCH at a high level.

(6) Clock input/output Pin (COUT, CIN and $\overline{\text{CIN}}$)

The clock buffer consists of a circuit equivalent to a general-purpose ECL logic circuit, with its input pin biased with an internal bias circuit (= −1.3V). The output amplitude level is 0.8V.

(7) Bias Pin (DVEE, SUB, DGND, VCC, AVEE, AGND and DC BIAS)

SUB denotes the IC substrate and its voltage potential should be common to that of DVEE. The standard value of DVEE and AVEE is −5.0V.

V_{CC} is the power supply for the interface circuit from a CMOS or TTL level to the internal ECL logic. Its standard value is +5V.

DC BIAS is the bias circuit of the discharge signal output circuit. As it requires about 2.5mA as its standard current, supply current should be 2.5mA + α. This pin voltage is biased to $2Vf$ and the value of α is determined as follows.

To maintain the pin voltage at $2Vf$ (≈ 1.4V), about 0.5 mA of current is required. Additionally, the maximum current flowing through the load resistor R_L attached to DCR (Pin 15) and DCL (Pin 23) is obtained from the following equation.

$$1/R_L \times (V_{DCH} + |DV_{EE}|) \times 2, \text{ where } R_L = 4.7\text{kohm}, V_{DCH} = 0.4\text{V and } DV_{EE} = -5\text{V}$$

Hence, $\alpha = 0.5 + 1.15 = 1.65$ (mA)

Therefore, the total current will be 4.32mA.

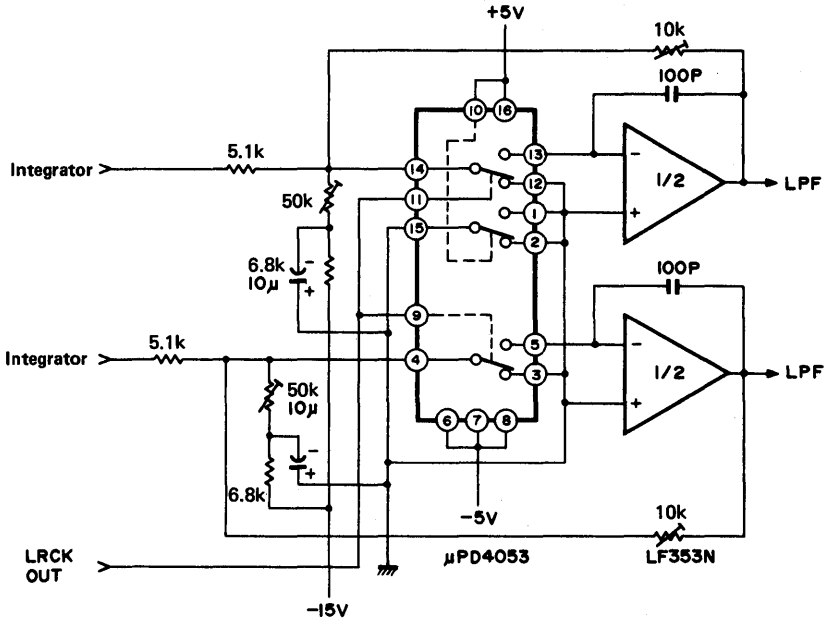
We recommend 5mA with R_L at 4.7 kΩ.

(8) System clock output pin, ON/OFF (SCKL, ON/OFF)

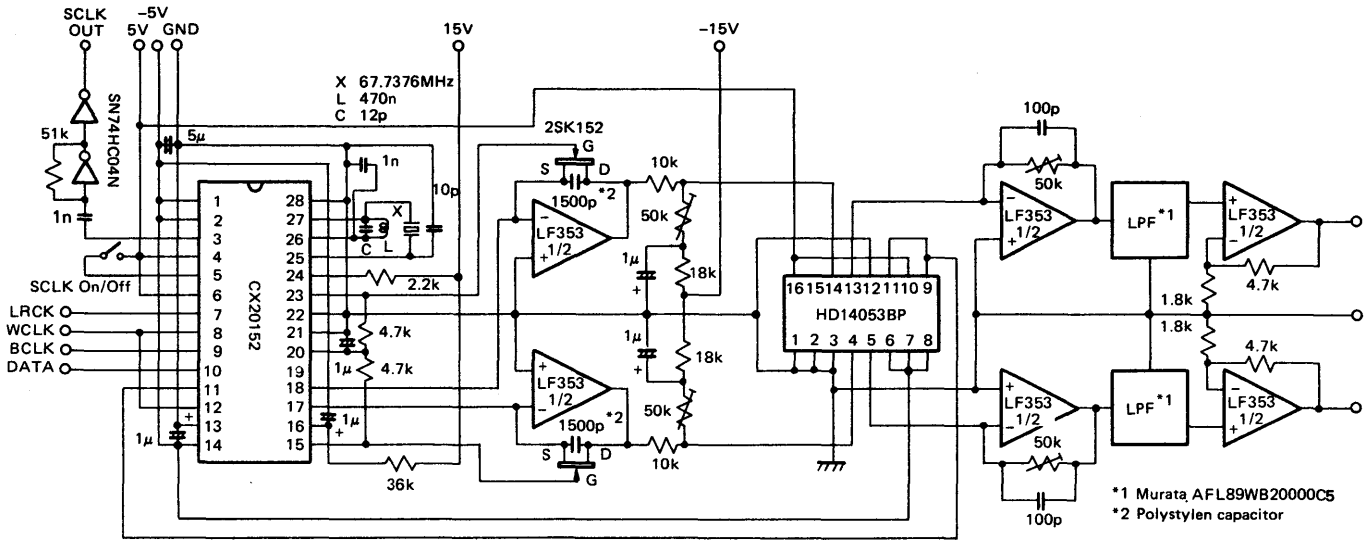
SCLK is the output pin of the 1/4 frequency divider of the oscillation circuit's master clock frequency. The frequency outputs when the ON/OFF pin is supplied with 5V (V_{CC}) and stops when the ON/OFF pin is supplied with 0V or set to open.

As its output amplitude is 2V and too low to be connected directly to a TTL or CMOS, be sure to amplify before connection.

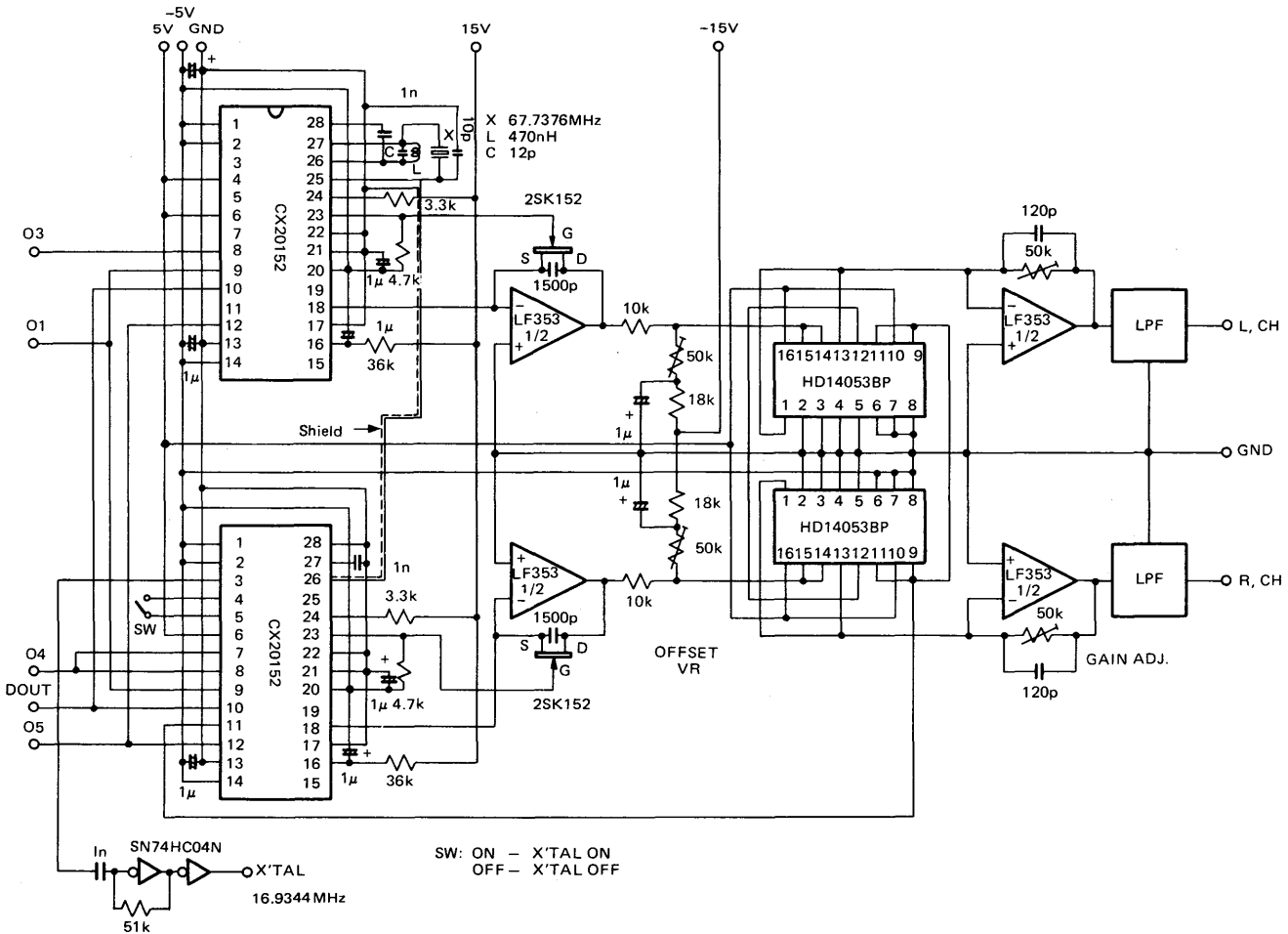
Application Circuit for Operating Deglitcher in Sample/Hold Type



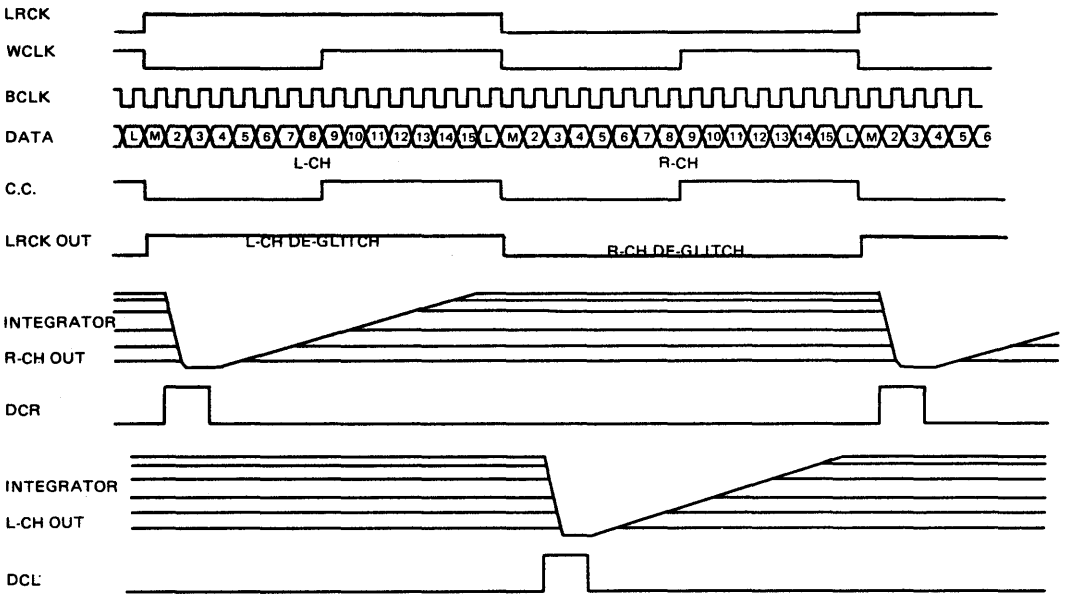
Application Circuit (Example 1)



Application Circuit (Example 2)

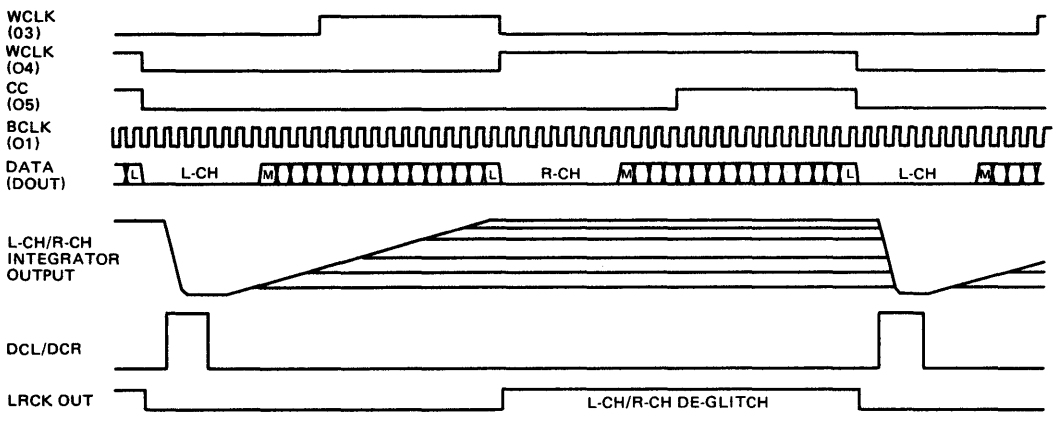


Timing Chart



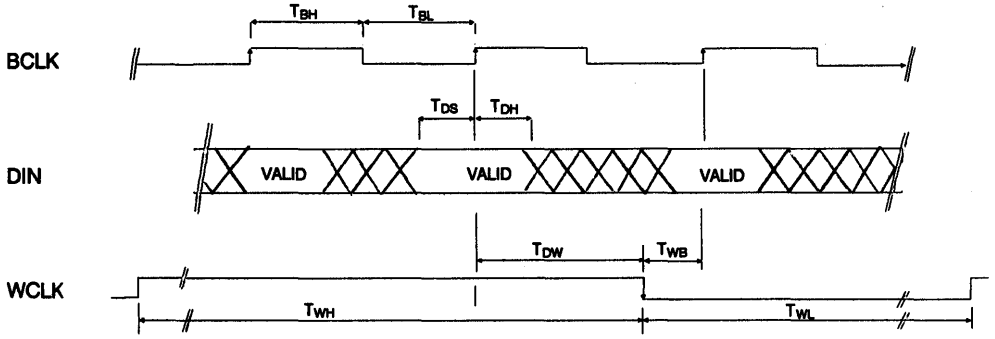
(See Application Circuit Ex. 1)

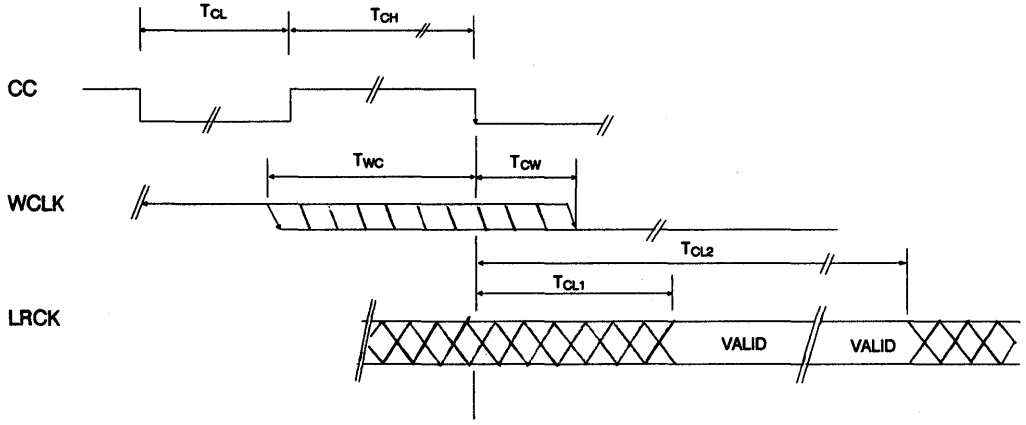
Timing Chart II



(See Application Circuit Ex. 2)

Detailed Timing Chart





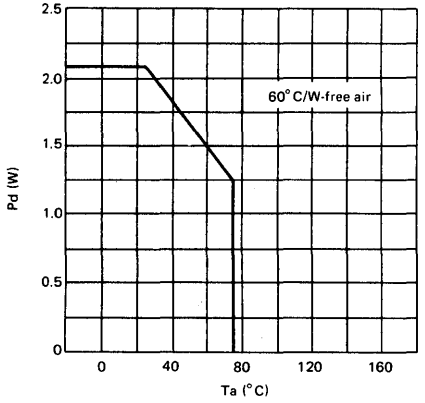
T_{BH}	BCLK "H" Pulse width	min = 100ns
T_{BL}	BCLK "L" Pulse width	min = 100ns
T_{DS}	DIN Set-up time	min = 50ns
T_{DH}	DIN Hold Time	min = 50ns
T_{DW}	from DIN ↘ to WCLK ↘	min = 150ns
T_{WB}	from WCLK ↘ to BCLK ↗	min = 50ns
T_{WH}	WCLK "H" Pulse Width	min = 100ns
T_{WL}	WCLK "L" Pulse Width	min = 100ns
T_{CH}	CC "H" Pulse width	min = $4 \times \tau_M$
T_{CL}	CC "L" Pulse width	min = $102 \times \tau_M$
T_{WC}	from WCLK ↘ to CC ↘	max = $T_{CL} + T_{CH} - 70 \times \tau_M$
T_{CW}	from CC ↘ to WCLK ↘	max = $30 \times \tau_M$
T_{CL1}	from CC ↘ to LRCK "Invalid→Valid"	max = $34 \times \tau_M - \tau_A - \tau_B/2$
T_{CL2}	from CC ↘ to LRCK "Valid→Invalid"	min = $367 \times \tau_M$

$\tau_M = 1/f_{MCLK}$

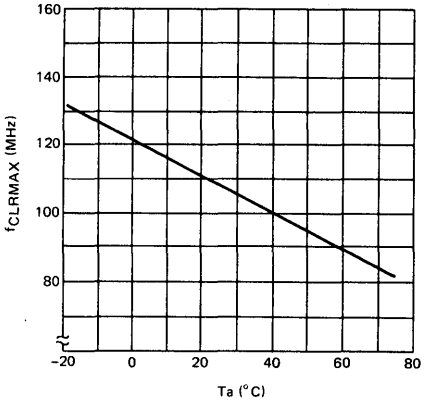
τ_A = Delay time produced by external analog switch

$\tau_B = 1/f_{BCLK}$

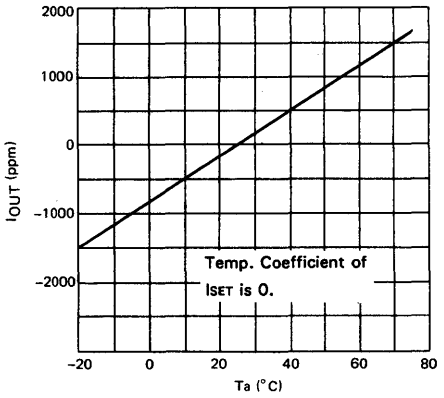
Maximum allowable power dissipation decrement curve



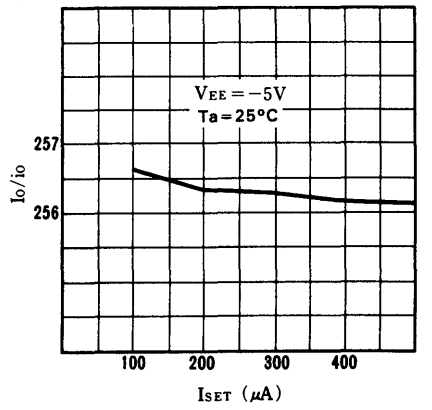
Maximum clock frequency temperature characteristics



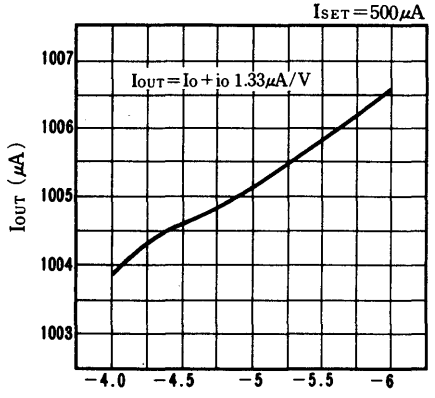
Iout temperarure characteristics (Io + io) (Both of R, Lch)



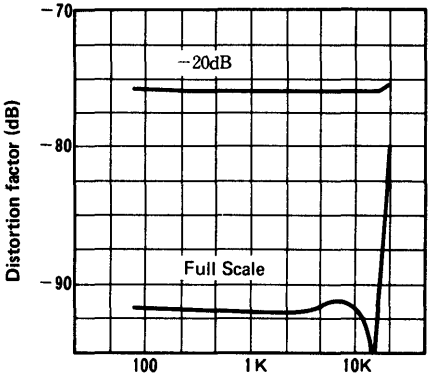
Io/io vs. ISET



Output current vs. Supply voltage (V_{EE})



Distortion factor



SONY

CXD1077M

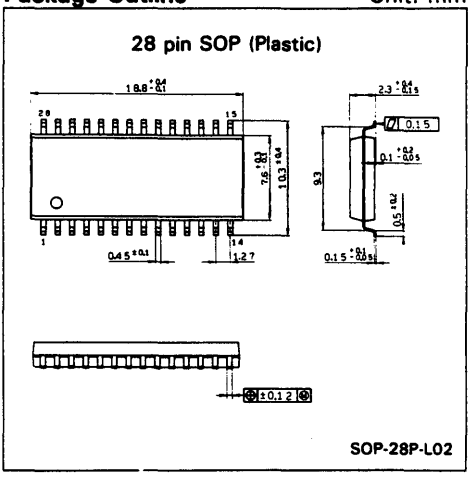
Dual 10 bit, 50 KHz, Multiplexed A/D, D/A

Description

CXD1077M is a 10 bit, 50 kHz, 2-channel CMOS A/D, D/A Converters for Auido digital signal processing, using a coarse-fine integration technique. Both Analog to Digital and Digital to Analog Conversions are capable with selecting the mode.

Package Outline

Unit: mm



Features

- 5V single power supply
- Adoption of the integrating method achieves a low distortion factor 0.1% (Typ.), 5V in operation.
- The built-in integrator and sample-hold circuit reduces the number of external parts.
- The REC mode and the PB mode can be set with external signals.

Functions

- Sample-hold of input analog signal in the REC mode, and resample-hold of output analog signal in the PB mode.
- R time sharing A/D and D/A conversion based on the integrating method.
- Serial data input/output with LSB data leading.

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}	−0.3 to +7.0	V
• Input voltage	V_{IN}	−0.3 to (V_{DD} + 0.3)	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C

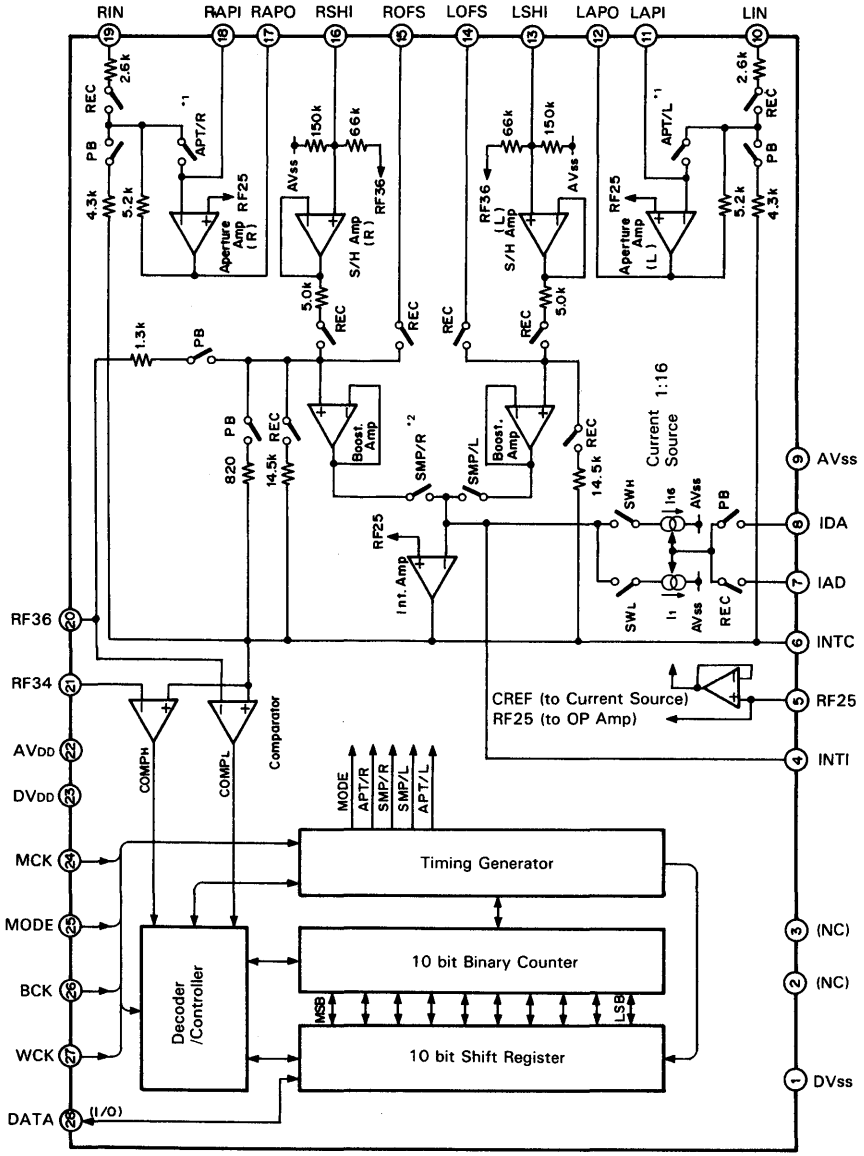
Recommended Operating Conditions

• Supply voltage	Vcc	4.75 to 5.25	V

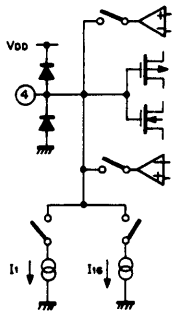
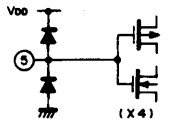
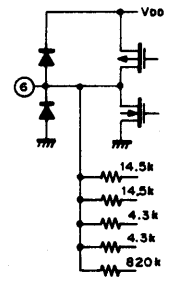
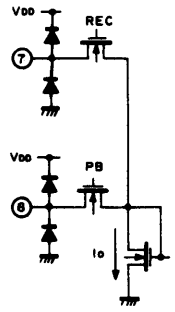
80339-TO

Block Diagram

*1. APT/L,R (REC mode) Ever on (PB mode) Aperture Discharge
*2. SMP/R Sampling

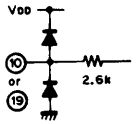
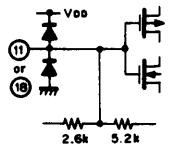
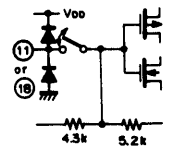
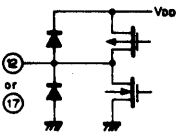
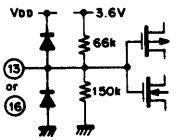


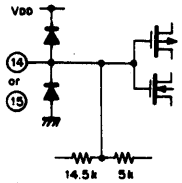
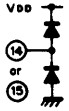
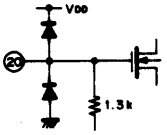
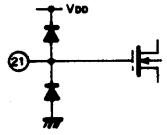
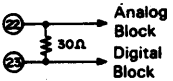
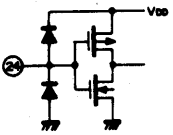
Pin Description

No.	Symbol	Voltage	I/O	Equivalent circuit	Description
1	DVss	0V			Digital ground pin
2	NC				Non connection
3	NC				Non connection
4	INTI	2.5V	I		Amplifier input pin for integrator (common to L and R). Integrating capacitor is externally connected between this pin and 6 INTO. Connected to forestage buffer amplifiers (separately for L and R) and two constant current supplies via respective analog switches. I1: 5 µA in REC mode, 3 µA in PB mode I16: 80 µA in REC mode, 48 µA in PB mode
5	RF25	*2.5V	I		Virtual ground potential setting pin for four inverted operational amplifiers. Externally supplies DC2.5V. Requires external connection of coupling capacitor.
6	INTO		O		Amplifier output pin for integrator (common to L and R). Integrating capacitor is externally connected between this pin and 4 INTI. (This pin permits observation of integrated wave form.)
7 8	IAD IDA	1.6 to 2.2V 1.3 to 1.9V	I I		Integrating current setting pins: 7 IAD for REC mode, and 8 IDA for PB mode. Current Io proportional to integrating current can be provided by externally connecting resistors between these pins and external reference voltage 3.6V. Io: 3.6 µA in REC mode 2.1 µA in PB mode A coupling capacitor of about 1 µF is externally attached to each of 7 and 8.

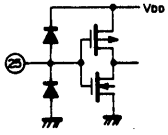
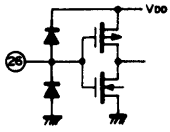
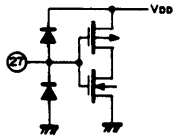
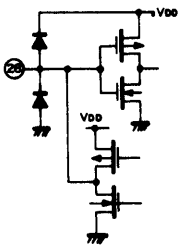
*) External voltage

Pin Description

No.	Symbol	Voltage	I/O	Equivalent circuit	Description
9	AVss				Analog ground pin.
10 19	L IN R IN		I I		Analog signal input pin (L, R). Appropriate full-scale input level is – 10 dBs (0.693Vpp).
11 18	LAPI RAPI		I I	[REC mode]  [PB mode] 	Amplifier input pins (L, R) for aperture. Sample-hold circuit in PB mode (in the IC, the amplifier for sample & hold of PB is called "aperture amplifier," for the discrimination from the amplifier for sample & hold of REC "S/H amplifier") is configured by externally attaching a capacitor between 11 LAPI and 12 LAPO, or between 18 RAPI and 17 RAPO. The aperture amplifier serves as a simple input amplifier in REC mode, and Pins 11 and 18 make almost no sense.
12 17	LAPO RAPO		O O		Aperture amplifier (L, R) output pins. [In REC] Analog signal entered from 10 L IN and 19 R IN is amplified by about 6 dB and output from there. [In PB] Sample & hold wave form of DA conversion is output.
13 16	LSHI RSHI		I I		S/H Amplifier (Sample & Hold Amplifier: L, R) input pins. In REC, analog signal output from 12 LAPO or 17 RAPO passes through an externally connected low-pass filter and then is returned to IC from this pin. The value of AC level is substantially the same as that of 10 L IN and 19 R IN (– 10 dBs full scale).

No.	Symbol	Voltage	I/O	Equivalent circuit	Description
14 15	LOFS ROFS		I I	[REC mode]  [PB mode]  	Offset correction pins in REC (L, R). Offset in A/D conversion can be corrected by externally connecting a semi-fixed resistor between these pins and external reference voltage 3.6V and adjusting the DC level of these pins.
20	RF36	*3.6V	I	 	Pin for setting lower rank comparator comparison voltage in REC or discharge voltage in PB. Externally feeds DC3.6V. Requires external connection of a coupling capacitor.
21	RF34	*3.4V	I	 	Pin for setting upper rank comparator comparison voltage in REC. Externally feeds DC3.4V. Requires external connection of a coupling capacitor.
22 23	AVDD DVDD	*5V *5V		 	Analog power supply voltage pin and digital power supply pin. Externally supply DC5V. Requires external connection of a coupling capacitor.
24	MCK		I	 	Master clock input pin. (11.58 MHz) Only MCK is TTL-compatible.

*) External voltage

No.	Symbol	Voltage	I/O	Equivalent circuit	Description
25	MODE		I		REC mode/PB mode select input pin. "H" level: REC mode (A/D conversion) "L" level: PB mode (D/A conversion)
26	BCK		I		Bit clock input pin.(Uses Pin 17 (BCK) output of CX23012 as shift clock for serial data.)
27	WCK		I		Word clock input pin. (31.5 kHz) Used as an L/R channel identification signal of data, and "H" level: L channel data "L" level: R channel data in both REC (data output) and PB (data input). (Uses output of Pin 18 (WCK) of CX23012 (in synchronization with the rise edge of BCK).
28	DATA		I/O		Data input/output pin. (2's complement) In REC: outputs 10-bit data in sync with the rise edge of BCK in the sequence of LSB, 2SB, ... MSB. In PB: inputs 10-bit data in sync with the fall edge of BCK in the sequence of LSB, 2SB, ..., MSB. L/R channels are alternately switched over in accordance with H/L of WCK.

Electrical Characteristics

Ta = 25°C Vpp = 5V (See Fig. 1 to 3)

Item		Symbol	Condition	Pin	Min.	Typ.	Max.	Unit
REC mode	Input impedance	Zin		10, 19		2.6		kΩ
	Full-scale input level	Vin		10, 19		−10		dBs
	Analog input gain	Gin	Aperture amplifier gain			6.0		dB
	Total harmonics distortion + noise	THD_1	Level = 1 dB, see Test method in 8-1.			0.10	0.14	%
		THD_2	Level = 6 dB, see Test method in 8-1.			0.18	0.20	%
PB mode	Total harmonics distortion + noise	THD_2	Level = 0 dB, see Test method in 8-2.			0.10	0.14	%
		THD_4	Level = 6 dB, see Test method in 8-2.			0.18	0.20	%
Power consumption		I_{DD}				24	36	mA

Test method of total harmonics distortion + noise in PB mode

The total harmonics distortion + noise characteristics (D/A conversion characteristics) in PB mode is measured by a method as shown in Fig. 1. Enter WCK and BCK generated by MCK (11.58 MHz) and CX23012 into CXD1077M, and at the same time, enter 0 dB (full-scale level) or −6 dB digital sine-wave data (1 kHz), and measure the total harmonics distortion + noise at this moment. Set −10 dBs (0.245 Vms) upon 0 dB input as the PB output level (interpolation filter output level) by adjusting the semi-fixed resistor 1 MΩ connected to the PB mode integrating current setting pin 8.

Test method of total harmonics distortion + noise in REC mode

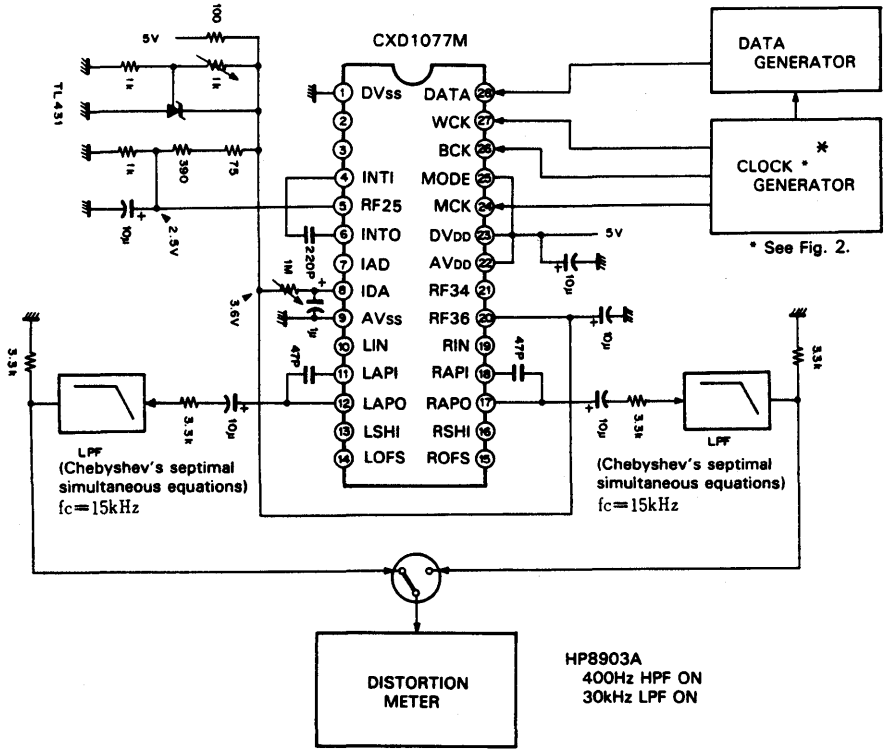
The total harmonics distortion + noise characteristics (A/D conversion characteristics) in REC mode is measured by a method as shown in Fig. 3. Enter WCK and BCK generated by MCK (11.58 MHz) and CX23012 into CXD1077M, and at the same time, enter −11 dBs (full-scale level −1 dB) or −16 dBs (full-scale level −6 dB) sine-wave (1 kHz) as analog signal, and DA-convert the A/D-converted data with the reference playback DAC (provide another DAC previously adjusted so that a PB output level of −10 dBs is reached upon input of full-scale data, by the method described in the above). Make setting by adjusting the semi-fixed resistor 4.7Ω connected to S/H amplifier input Pins 13 and 16 so that the analog level becomes equal to the analog output level (interpolation filter output) of reference playback DAC (REC level adjustment). It is however necessary to previously adjust offset so that the wave form may not be clipped by the semi-fixed resistor 22Ω connected to the offset correction Pins 14 and 15, while observing the output wave form of the reference playback DAC when the input is near the full scale (offset adjustment is possible also by the method shown in the DC offset adjustment in REC on page 369).

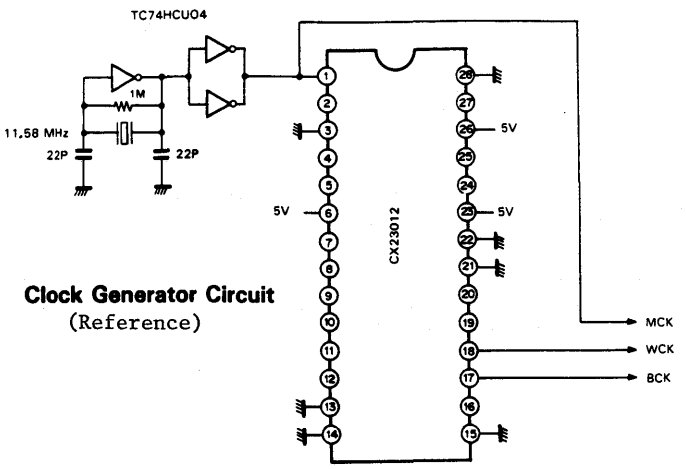
After the completion of the adjustment as described above, measure the sum of total harmonics distortion + noise of analog output (interpolation filter output) of the reference playback DAC, and use the result as the REC mode conversion characteristics of the tested device.

Fig. 1

Electrical Characteristics Test Circuit

(For total harmonics distortion factor and noise characteristics in PB mode)





Clock Generator Circuit
(Reference)

Fig. 2

Electrical Characteristics Test Circuit
(For total harmonics distortion factor and noise characteristics in REC mode)

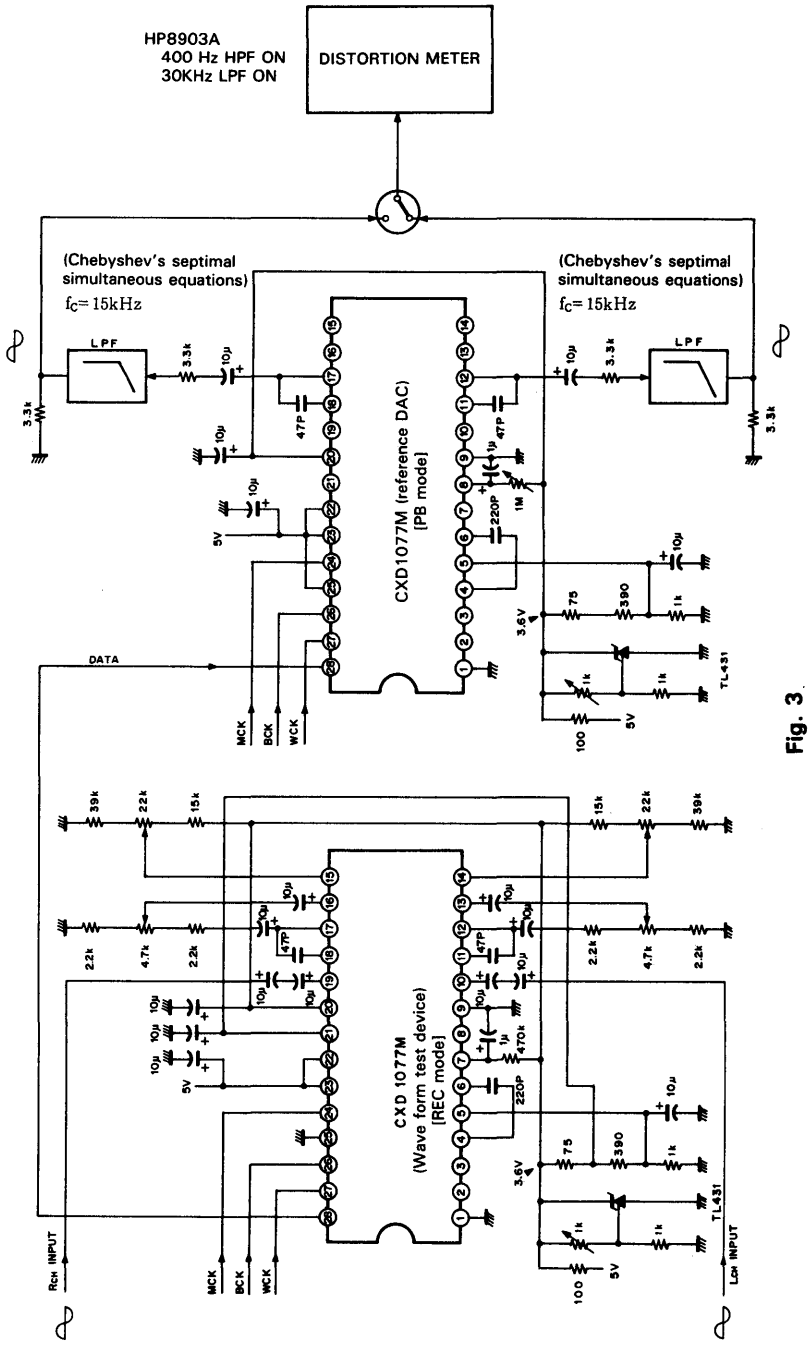


Fig. 3

Description of Function

The CXD1077M is a single-chip 10-bit A/D, D/A converter provided with every function required in A/D and D/A conversion. Particularly when combined with CX23011 (for modulation, demodulation and error correction), CX23012 (A/D, D/A interface) and CX20099 (analog noise reduction), it is used in the PCM processor for 8-mm video.

Description of REC mode function

1) Selection of operational mode
   REC mode (A/D conversion mode) is selected by setting the MODE signal to "L".
2) Analog block operation and gain
   The input signal applied to the analog signal input pins 10 and 19 is amplified by about 6 dB by the aperture amplifier and output to the aperture output pins 12 and 17. After component out of band area is removed from the output signal by the external attenuation filter, it is added to the sample-hold input pins 13 and 16 and output to the integrating output pin 6 after amplification by about 9.25 dB by the sample-hold amplifier.
   This gain is obtained assuming that the external filter's insertion loss is −6 dB. Therefore, the overall gain will be about 9.25 dB when the filter is included. Even when the external filter's insertion loss is different from the above value, or its insertion position is different, it is necessary to achieve an overall gain of about 9.25 dB. For details, refer to the REC level adjustment on page 16.
3) Digital block operation and clock (see Fig. 4: REC mode timing chart)
   The Convert Command (C.C.) is generated internally by entering WCK and BCK. While C.C. is at "H", the analog signal applied to the S/H amplifier is sampled, and while C.C. is at "L", the constant current weighted with inverse polarity against the input signal is integrated by the integrating circuit for conversion. The 10-bit data is performed by calculating the integrating time of the coarse constant current and fine constant current separately using a counter. An MCK frequency of 11.58 MHz is used for 8-mm video as the counter clock frequency required when conducting full-scale A/D conversion. In the CXD1077M, it is necessary to maintain mutual synchronization of MCK, WCK and BCK because of the necessity of converting operation to be in synchronization with MCK, irrespective of the phase relationship of MCK with WCK or BCK. The data is loaded, on the other hand, in the shift register when C.C. becomes "H" again and is output serially with LSB leading in synchronization with the rise edge of BCK. The data is coded in 2's complement.
4) Integrating current in REC
   The integrating current value $I_{A/D}$ required when performing a full-scale A/D conversion in the CXD1077M is obtained by the following equation:

$$I_{A/D} = \frac{C \cdot V_I}{1023 \tau_o}$$

   where, C : Integration Capacitance
   V_I : Integrator output voltage, and
   τ_o : MCK cycle.

   According to Fig. 6 representing an example of application circuit, C = 220pF, V_I = 2Vp-p' and τ_o = 86 ns (MCK frequency: 11.58 MHz), leading to an integrating current value of about 5 μA. The integrating current setting is done by applying an external constant current to the Rec mode integrating current setting pin 7 through a resistor from an external reference voltage (3.6V). Supposing a setting resistor value of 470 kΩ, the constant current applied to pin 7 has a value of about 3.6 μA (reference value), corresponding to an integrating current value of about 5 μA.
5) Comparison voltage and virtual ground voltage
   Switching between the upper conversion and lower conversion is performed by the integrating output 6 surpassing the comparison voltages 20 RF36 and 21 RF34 in the next stage compara-

tor. The integrating output based coarse constant current surpassing RF34 (about 3.4V) causes switching from the upper to lower conversion, and the integrating output based on fine constant current surpassing RF36 (about 3.6V) causes the lower conversion to end.
Since the CXD1077M operates with a single 5-V power supply, it is necessary to apply a virtual ground voltage of 2.5V to a non-inverted input of the internal operational amplifier. This voltage is applied to 5 RF25.

6) DC offset
As 8-mm video uses a non-linear quantization by 10-bit ≒ 8-bit compression/expansion, compatibility is affected when a DC offset component is included in the A/D conversion data in recording. When the analog signal input is so large as being close to the full-scale level, the A/D conversion data may be clipped on a single side of positive or negative. To correct this DC offset, the integrating output's center voltage must be shifted by applying an offset voltage to the offset correcting pins 14 and 15. As to details, refer to the DC offset adjustment in REC mode on page 369.

Description of PB mode operation

1) Selection of operation mode
By setting the MODE signal to "H", the PB mode (D/A conversion mode) is selected.

2) Digital block operation and clock (refer to Fig. 5: PB mode timing chart)
DIS (Discharge clock) and APT (Aperture clock) are generated internally in the CXD1077M, by entering WCK and BCK. The serial data input with LSB leading is stored in the shift register in synchronization with the falling edge of BCK and set in the counter while DIS is "H". When DIS becomes "L", the counter starts counting, beginning from the value set in it, and at the same time, a constant current weighted corresponding to data is output. When the counter outputs the carry signal, the counting and constant current output stop. The counter clock frequency required when performing a full-scale D/A conversion is 11.58 MHz (MCK frequency) for 8-mm video.

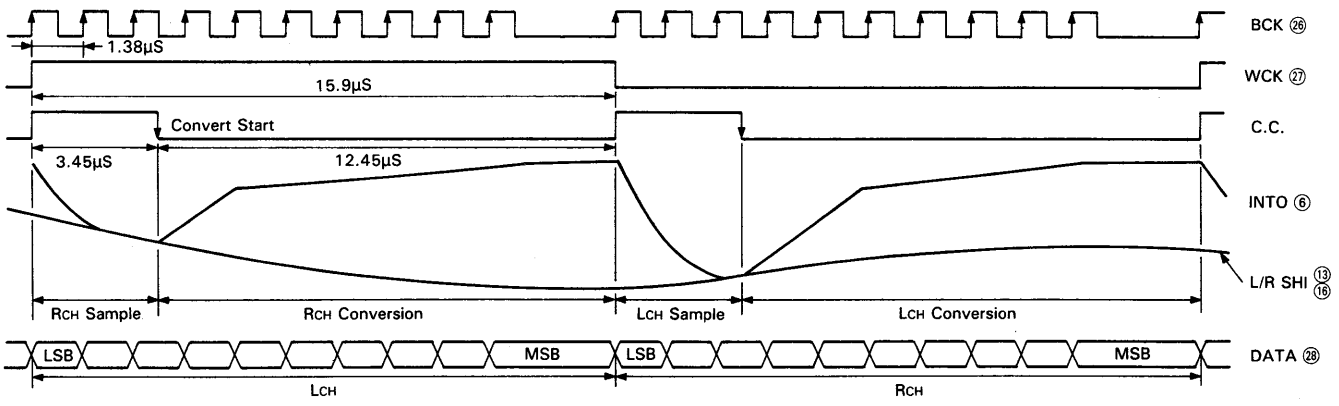
3) Analog block operation and gain
The integrating charge resulting from the previous conversion is discharged while DIS is "H" by sampling the external reference voltage 3.6V applied to 20 RF36 by means of the integrator. As a result, the integrating output in the discharge region is initialized to about 1.8V, and the output center voltage in input of sine-wave data becomes about 2.5V. When DIS goes to "L", D/A conversion operation is executed by integrating the constant current output. When the constant current output stops, integrating also stops, and the pin voltage held in the integrated capacitor at this moment takes the D/A converted value. This pin voltage is output, after being amplified by about 1.6 dB by the aperture amplifier, to the aperture output pins 12 and 17. Output signal's out-of-band components are removed by an external interpolation filter.

4) PB integrating current
Integrating current $I_{D/A}$ required when performing full-scale D/A conversion in the CXD1077M is determined from the following equation:

$$I_{D/A} = \frac{C \cdot V_I}{1023 \tau_o}$$

According to Fig. 6 representing an example of application circuit, C = 220pF, V_I = 1.2Vp-p' and τ_o = 86 ns, leading to an integrating current value of about 3μA. The integrating current setting is one by applying an external constant current to the playback mode integrating current setting pin 8 through a resistor from an external reference voltage (3.6V). Supposing a setting resistor value of 910 kΩ, the constant current applied to pin 8 has a value of about 2.1 μA (reference value), corresponding to an integrating current value of about 3 μA. It is possible to adjust the D/A conversion output level by altering this setting resistor. For details, refer to the PB level adjustment on page 369.

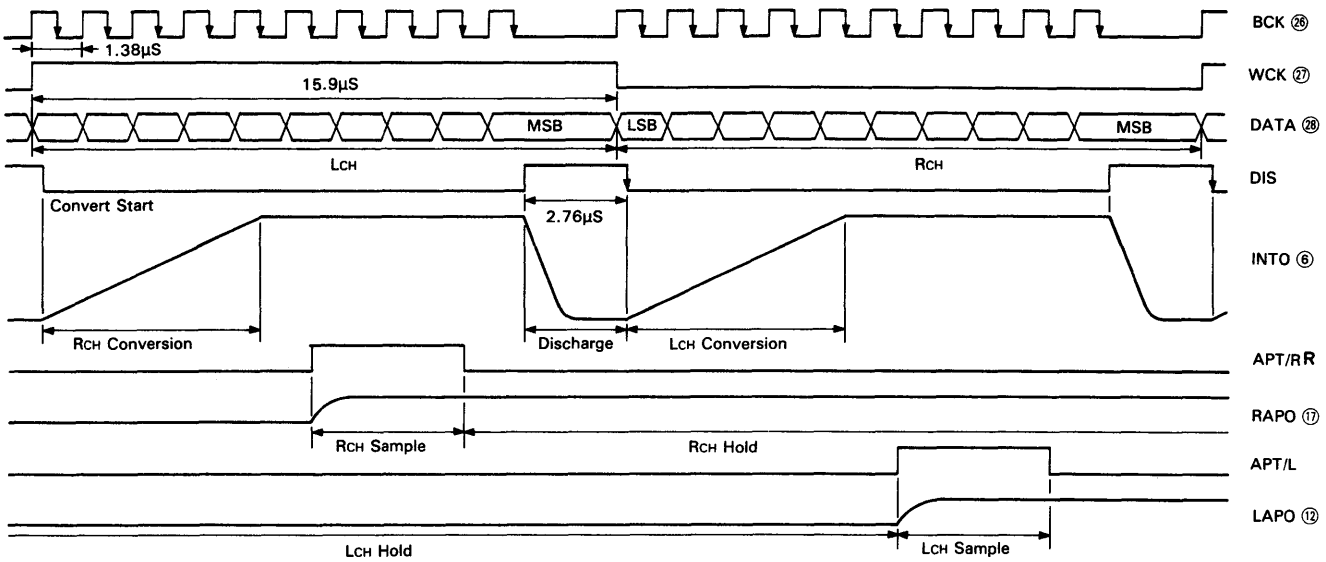
Timing Chart of REC Mode



When the MODE signal (pin 25) of the CXD1077M is set to "L", REC mode (A/D conversion mode) is selected. When BCK and WCK are entered from **AD/DA interface LSI(CX23012)** in this mode, C.C. (Convert Command) is generated internally in the CXD1077M. While this C.C. is at "H" level, the analog signal input is sampled; A/D conversion is executed during "L" level. The sampling and conversion operations are performed in time division for each of the R and L channel analog signals. The converted final data is output serially with the LSB data leading in synchronization with the rise edge of BCK when the C.C. becomes "H" level again.

Fig. 4

Timing Chart of PB Mode



When the MODE signal (pin 25) of the CXD1077M is set to "H", PB mode (D/A conversion mode) is selected. When BCK and WCK are entered from A/D, D/A interface LSI (CX23012) in this mode, DIS (Discharge clock) and APT R/L (Aperture clock) are generated internally in the CXD1077M. At the same time, the serial data input with the LSB leading is stored in synchronization with the fall edge of BCK. After DIS has discharged at "H" level, the integrating charge resulting from the previous D/A conversion, D/A conversion starts when DIS goes to "L" level. The discharge and conversion operations are performed in time division for each of the R and L channel data inputs. The final integrated output after conversion is sampled while APT R/L is at "H" and held at "L" level.

Fig. 5

Application Circuit

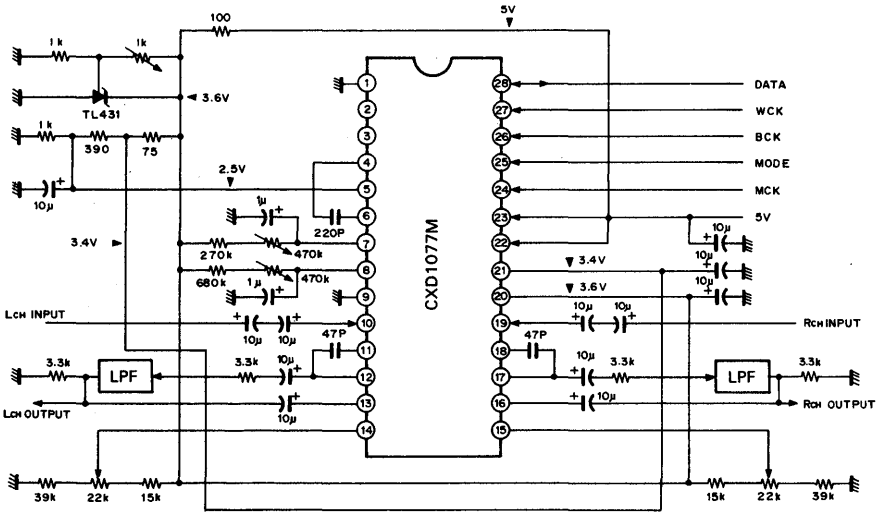


Fig. 6

Compensation characteristics of aperture effect

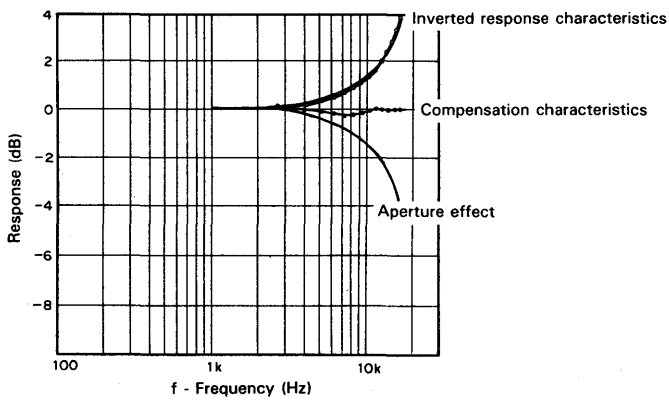


Fig.7

Notes for Application and Adjustment Methods

(see Fig. 6. Application circuit)

As the conversion accuracy obtained is affected by the accuracy of parts used and adjustment in the CXD1077M, attention should be given to the following points:

Selection of parts to be used

1) For the integrating capacitor between pins 4 and 6, use a type with little dielectric absorption (e.g. styrol capacitor).
2) Adjust the semi-fixed resistor 1 kΩ so that the reference voltage generated from the reference voltage IC (TI's TL431) is 3.6V.
3) For the low-pass filters to be inserted between pins 12 and 13 and between pins 16 and 17, use passive-type ones with an input/output impedance of 3.3 kΩ, respectively.
4) Accuracy tolerance of the three divided resistors, 75 Ω, 390 Ω, and 1 kΩ, supplying voltage to pins 5 and 21 is 5%.

PB level adjustment

In adjustment of the PB level during D/A conversion, use a 470 kΩ semi-fixed resistor connected to pin 8. Input to pin 28 a full-scale level digital sine-wave data (1 kHz), and adjust the semi-fixed resistor so that the PB level (interpolation filter output level) becomes −10 dBs (0.245 Vrms).

REC level adjustment

Adjustment of REC level during A/D conversion can be accomplished by the use of a 470 kΩ semi-fixed resistor connected to pin 7 as well, in addition to the method described in 8-2 above. Apply a −16 dBs (−6 dB of full-scale level) sine wave (1 kHz) to pins 10 and 19 as the analog input signal, and conduct D/A conversion of the A/D-converted data by means of a reference playback DAC (prepare another DAC adjusted previously by the method mentioned in the PB level adjustment above so that the playback output level becomes −10 dBs when entering full-scale data). Adjust the semi-fixed resistor so that the reference playback DAC output level becomes equal to the analog signal input level (−16 dBs) to the tested A/D converter.

DC offset adjustment in REC

In the offset adjustment of A/D-converted data during A/D conversion, use a 22 kΩ semi-fixed resistor connected to pins 14 and 15. In practice, adjust the semi-fixed resistor so that the data output of pin 28 becomes "0000000000" when DC2.5V is applied as the analog input level of pins 10 and 19. In this adjustment, do not fail to conduct offset adjustment only after the completion of REC level adjustment as described in the REC level adjustment above.

Frequency characteristics

The CXD1077M frequency characteristics in REC is determined by an input attenuation filter. Meanwhile the frequency characteristics in PB is determined by the aperture effect and output interpolation filter. With the CXD1077M, degradation of high area frequency characteristics caused by the aperture effect is unavoidable. This is because a sample-hold aperture circuit is used to obtain −10 dBs as the interpolation filter output level during full-scale D/A conversion. To compensate the degraded characteristics, add a compensation filter, as shown in Fig. 7, with inverted response characteristics.

Audio Digital Filter

7

5. Audio Digital Filters

Type	Function	Page
CXD1088AQ	4Fs, Filter length 104, 16/18-bit output	373
CXD1144BP	4/8Fs, Filter length 293, 16/18-bit output	386
CXD1162P	4Fs, Filter length 104, 16-bit output	397
CXD1244S	4/8Fs, Filter length 213, 16/18-bit output	409
CXD2550P	4/8Fs, Filter length 57, 16/18-bit output	422
CXD2551M/P	4/8Fs, Filter length 57, 16/18-bit output	430

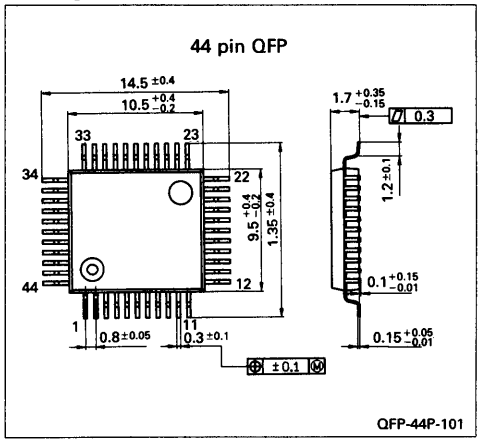
Over Sampling Digital Filter LSI

Description

CXD1088AQ is a digital filter LSI with quadrupled sampling rate, developed for compact disc player.

Package Outline

Unit: mm



Features

- 83rd and 21st order filters linked through cascade connections provide a quadrupled sampling digital filter
- Built-in filters for 2 channels corresponding to L and R
- Variety of functions including soft-muting and offset addition
- 83rd and 21st order filters also have 2 modes of filter coefficients each, to enable the selection of the most suitable filter characteristics, required for usage.

Functions

- Filters for two channels
- Filtering with a quadrupled sampling rate
- Two-stage FIR filters interconnected in cascade (83rd order+21st order)
- 18-bit serial output possible
- Switching between serial and parallel output modes
- ±1% offset addition
- Soft-muting function
- Independent linear error correction for either L or R, up to 8 words
- 2 modes of coefficients provided for both 83rd and 21st orders (refer to "Filter Characteristics")
- Input/output format
  - Input: 2's complement; MSB first (serial)
  - Output: 2's complement; MSB first (serial)
    Offset binary (parallel)

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (Ta=−25 to +75°C)

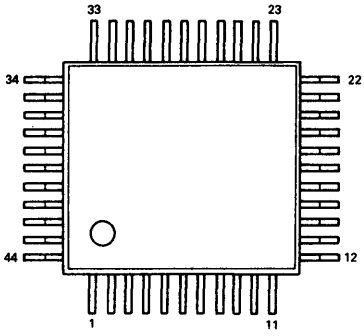
• Supply voltage	V_{DD}	−0.5 to +6.5	V
• Input voltage	V_I	−0.5 to V_{DD} +0.5	V
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	450	(Ta=75°C) mW

Recommended Operating Conditions

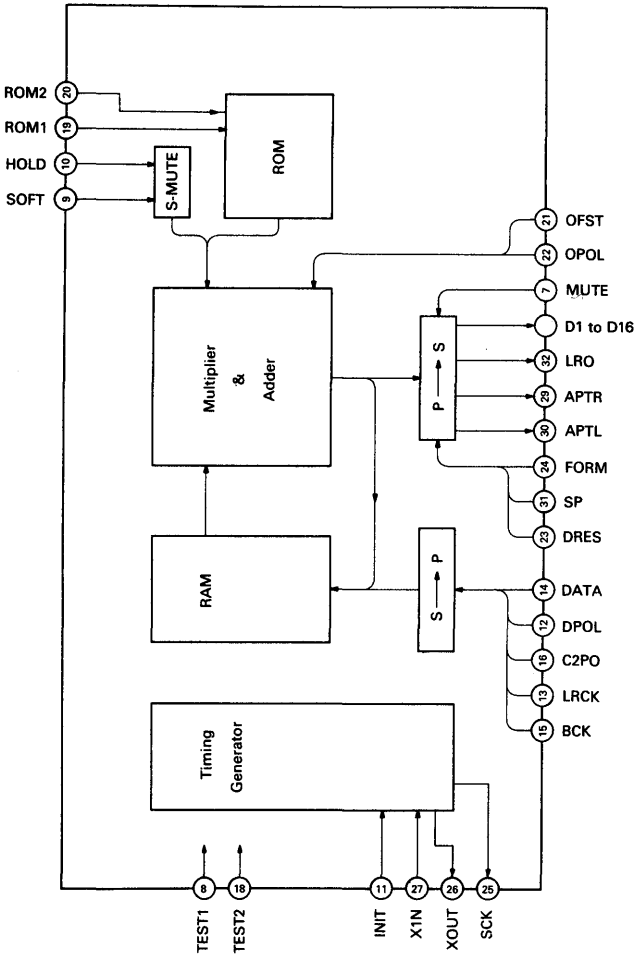
• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature	Topr.	−20 to +75	°C
• OSC frequency	fx	10 to 20	MHz

80629-BC

Pin Configuration (Top View)



Block Diagram



Pin Description

No.	Symbol	I/O	Description
1 to 5	D_{12} to D_{16}	O	D_{12} to D_{16} output pins when the parallel output mode is selected; fixed at "L" level when the serial output mode is selected.
6	Vss	–	Negative power supply (0V).
7	MUTE	I	Mutes the output to "0" or an offset value; active at "H" level.
8	TEST1	I	Test pin; normally, fixed at "L" level
9	SOFT	I	Soft muting ON/OFF switch; ON at "H" level
10	HOLD	I	Stops soft muting at "H" level
11	INIT	I	Power-on-Reset input pin; active at "L" level
12	DPOL	I	Reverses the polarity of input data
13	LRCK	I	LRCK input pin
14	DATA	I	"16 bits×2" serial data input pin; 2's complement
15	BCK	I	BCK input pin
16	C2PO	I	Error flag input pin
17	V_{DD}	–	Positive power supply (+5V)
18	TEST2	I	Test pin; normally, fixed at "L" level.
19	ROM1	I	ROM switching for 83rd order (Refer to "Filter Characteristics.")
20	ROM2	I	ROM switching for 21st order (Refer to "Filter Characteristics.")
21	OFST	I	Adds an offset to the output; active at "H" level.
22	OPOL	I	Specifies the polarity of offset values; "H": +1%; "L": −1%
23	DRES	I	Indicates the word length of data for SONY format serial output; "H": 18bits; "L": 16bits.
24	FORM	I	Specifies the output format; "H": I^2S; "L": SONY
25	SCK	O	System clock output for external IC; (384fs)
26	XOUT	O	Output pin of crystal oscillation circuit; (384fs)
27	XIN	I	Input pin of crystal oscillation circuit; (384fs)
28	Vss	–	Negative power supply (0V)
29	APTR	O	Aperture clock for R channel
30	APTL	O	Aperture clock for R channel
31	SP	I	Switches serial/parallel output modes; "H": parallel; "L": serial.
32	LRO	O	LRCK output (4fs)
33	D_1	O	D_1 (MSB) output pin when the parallel output mode is selected; BCK (4fs) output pin when the serial output mode is selected.
34	D_2	O	D_2 output pin when the parallel output mode is selected; DATA (4fs) output pin when the serial output mode is selected.
35	D_3	O	D_3 output pin when the parallel output mode is selected; LRCK (I^2 mode) or WCK (SONY mode) output pin when the serial output mode is selected.
36 to 38	D_4 to D_6	O	D_4 to D_6 output pins when the parallel output mode is selected; fixed at "L" level when the serial output mode is selected.
39	V_{DD}	–	Positive power supply (+5V)
40 to 44	D_7 to D_{11}	O	D_7 to D_{11} output pins when the parallel output mode is selected; fixed at "L" level when the serial output mode is selected.

Electrical Characteristics

DC characteristics

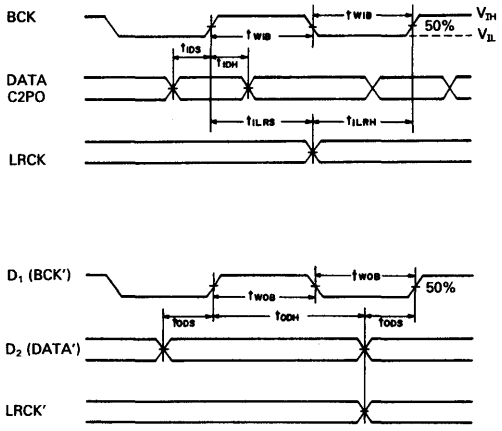
V_{DD}=4.5 to 5.5V, Ta=−20 to +75°C

No.	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
27	Input leak current	I_{LI}	V_I=V_{DD}/0V	–	–	±20	μA
7,9,10 to 16, 19 to 24,31	"H" input voltage	V_{IH}	–	0.76V_{DD}	–	–	V
	"L" input voltage	V_{IL}	–	–	–	0.24V_{DD}	V
	Input leak current	I_{LI}	V_I=V_{DD}/0V	–	–	±5	μA
29,30,32 to 35	"H" output voltage	V_{OH}	I_O=−4mA	V_{DD}−0.5	–	–	V
	"L" output voltage	V_{OL}	I_O=4mA	–	–	0.4	V
2 to 5, 36 to 38, 40, 44	"H" output voltage	V_{OH}	I_O=−1mA	V_{DD}−0.5	–	–	V
	"L" output voltage	V_{OH}	I_O=1mA	–	–	0.4	V
25	"H" output voltage	V_{OH}	I_O=−5mA	V_{DD}−1.0	–	–	V
	"L" output voltage	V_{OL}	I_O=5mA	–	–	1.0	V
	Current consumption	I_{DD}	Under no load: V_I=V_{DD}/0V, fx=16.93MHz	–	–	40	mA

AC characteristics

V_{DD}=4.5 to 5.5V, Ta= −20 to +75°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillating frequency	fxt		–	16.9344	20.0	MHz
Input BCK frequency	f_{BCK}		–	–	3.1	MHz
Input BCK pulse width	t_{WIB}		100	–	–	ns
Input data set-up time	t_{IDS}		20	–	–	ns
Input data hold time	t_{IDH}		20	–	–	ns
Input LRCK set-up time	t_{ILRS}		50	–	–	ns
Input LRCK hold time	t_{ILRH}		50	–	–	ns
Output BCK pulse width	t_{WOB}	I^2S serial output mode f_{XT}=16.9344MHz C_L=50pF	70	–	–	ns
Output data set-up time	t_{ODS}		40	–	–	ns
Output data hold time	t_{ODH}		40	–	–	ns



Functions

Soft muting

Mutes or de-mutes output data within approximately 23ms (1024/fs). The output level can be held during muting operation.

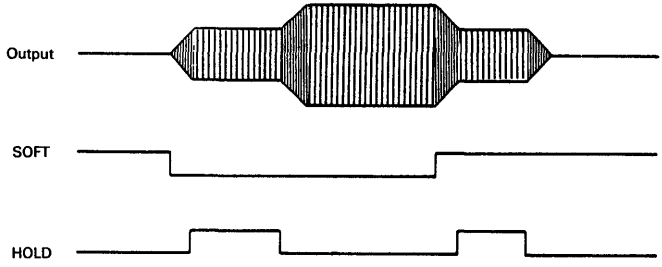


Fig. 1

Offset

Adds an offset to the output data. The offset amount can be positive or negative.

Table 1

OFST	OPOL	Offset amount
L	–	0%
H	L	−1%
H	H	+1%

Muting

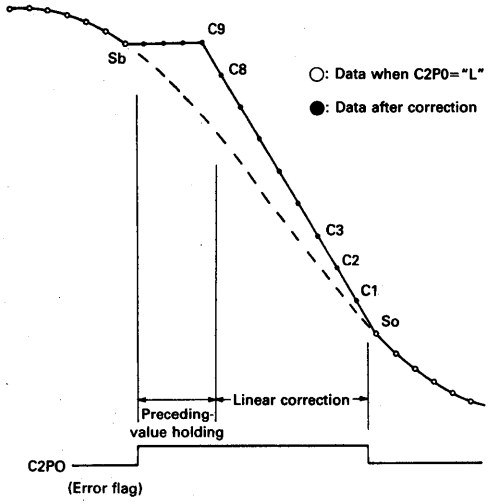
When MUTE goes high or INIT goes low, the output is muted. An offset value which has been set following Table 1 above is output.

Data polarity

Allows switching between inversion and non-inversion of output data polarity.
When DPOL level is "L": the output data is not inversed with respect to the input data.
When DPOL level is "H": the output data is inversed with respect to the input data.

Error correction

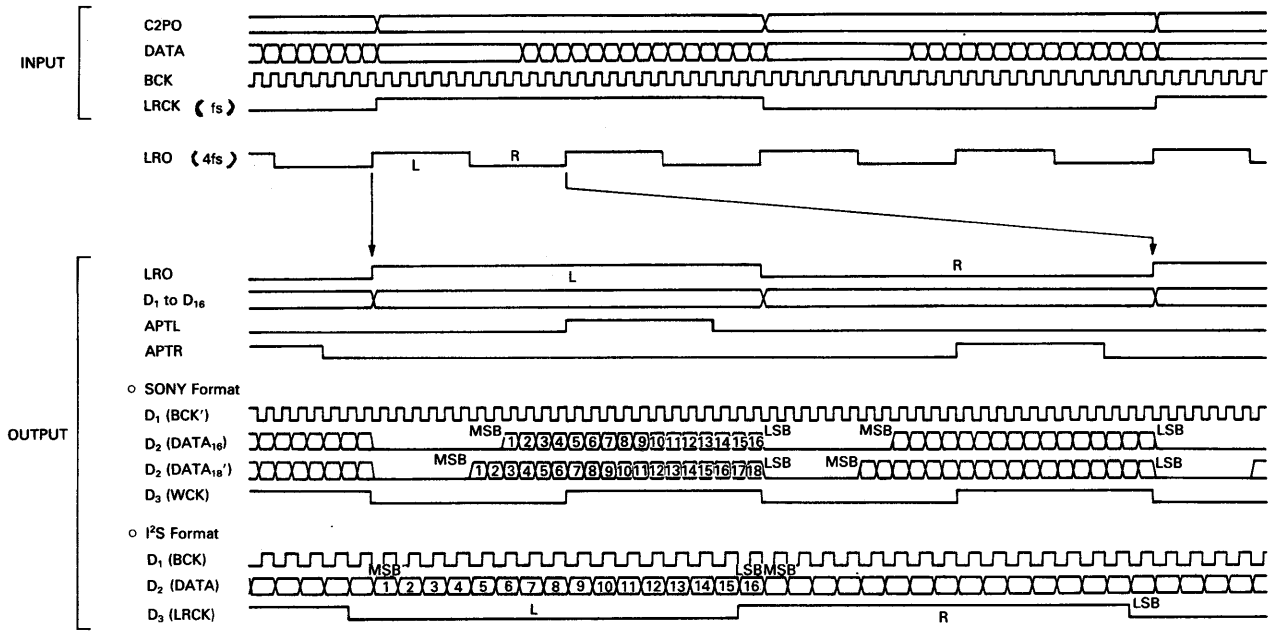
Errors in an input data block consisting of up to eight consecutive data units can be linearly corrected by the two correct data units, the one preceding the erroneous block and the other following it. (This is done separately for L and R.) For errors of more than eight consecutive input data units, only the last eight data are linearly corrected, and all preceding data units are maintained without correction.



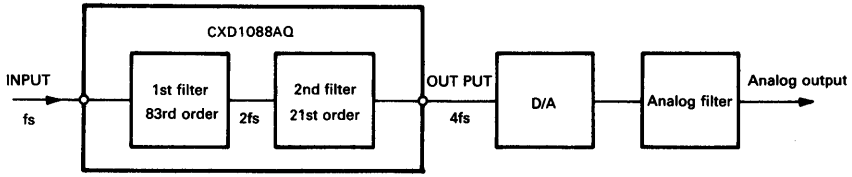
Input and output

1) Input
   The changeover point of MSB first serial data (fs) of 2's complement represents the switching of LRCK. Of this data string, only the data of the last 16-bit clock (BCK) are valid.
   When INIT="L" (resetting), the input data are invalid and the input is equivalent to ALL "0."
2) Output
   SP="L": MSB first serial data (4fs) of 2's complement
   SP="H": offset binary parallel data (4fs)
   Clock pulses such as LRO and BCK are constantly output as long as the power is on. Data are output only when resetting is canceled (INIT="H") when MUTE="L." Otherwise, muting remains effective.

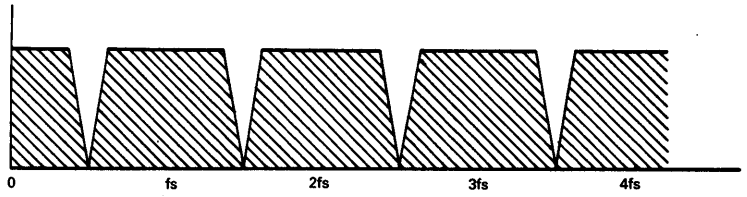
I/O Timing Chart



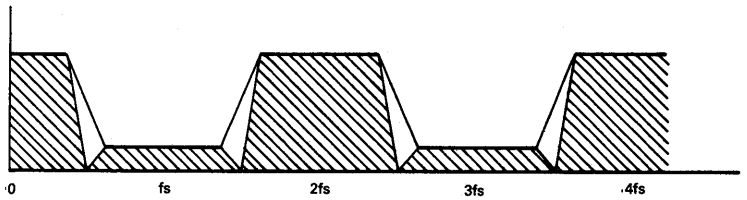
Filter Characteristics



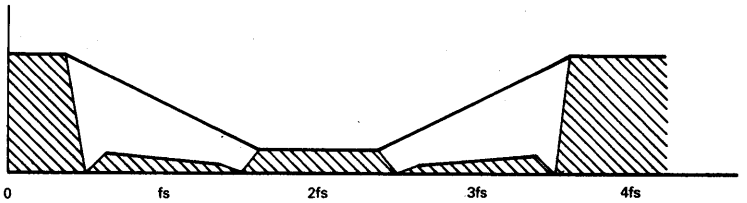
Input spectrum



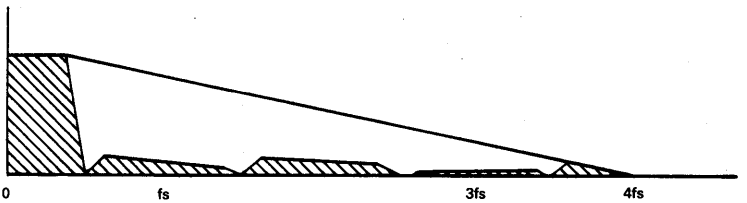
Characteristics of 1st filter



Characteristics of 2nd filter

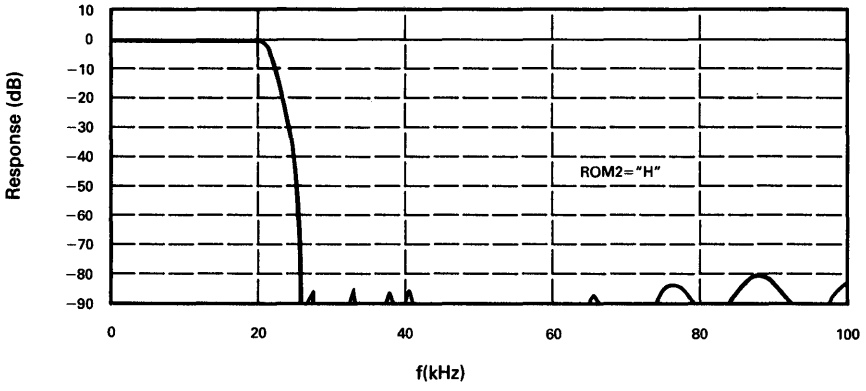


Charcteristics of analog filter

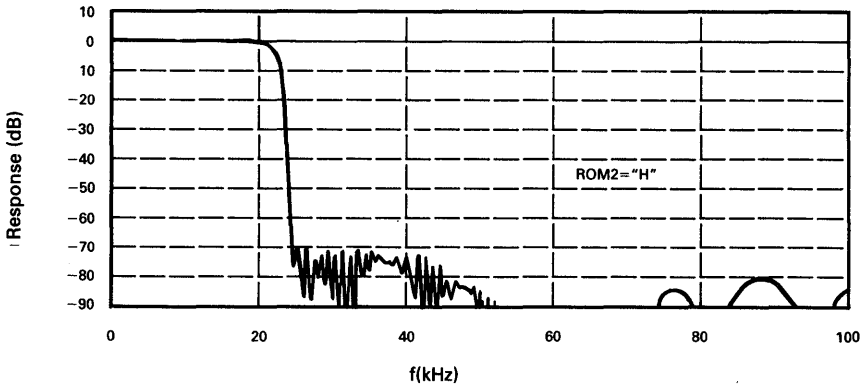


Combined Filter Characteristics (1st filter + 2nd filter)

1) ROM1="H"
Stop band attenuation: 80dB Min. (over 25.7kHz)
Pass band ripple: ±0.001dB Max.



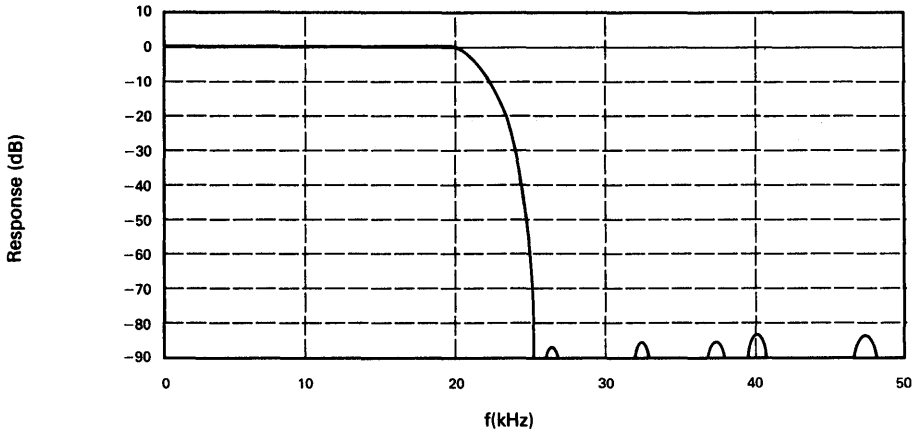
2) ROM1="L"
Stop band attenuation: 60dB Min. (24.1kHz); 65dB Min. (over 24.2kHz)
Pass band ripple: ±0.004dB Max.



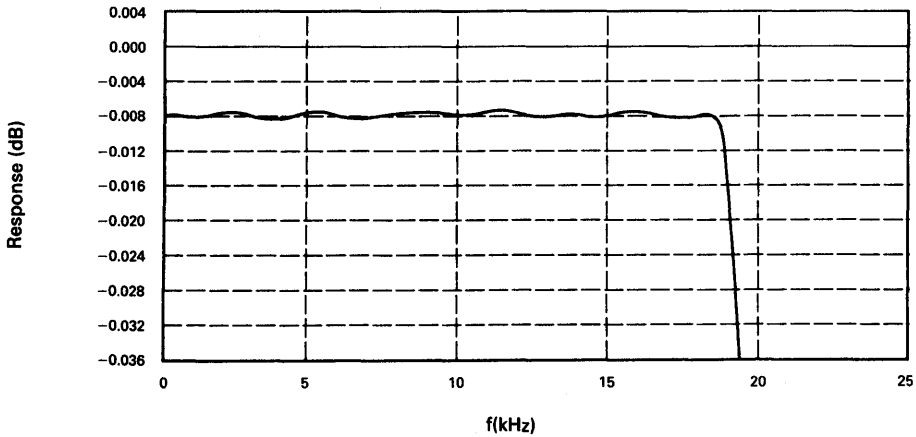
Filter Characteristics-1

1st Filter (83rd order, ROM1="H")

Frequency characteristics of filter



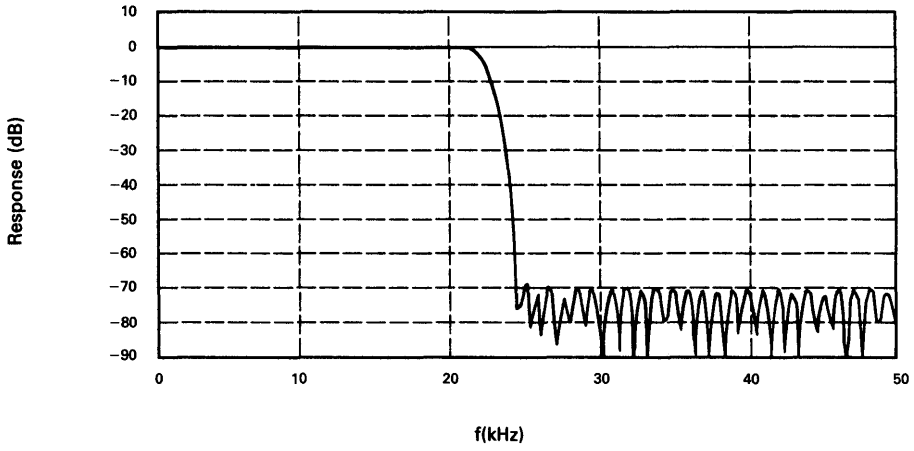
Ripple characteristics in pass band



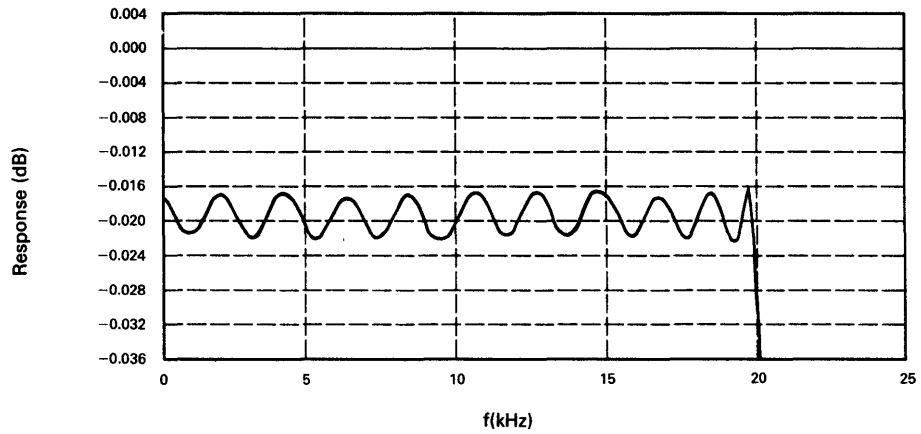
Filter Characteristics-2

1st Filter (83rd order, ROM1="L")

Frequency characteristics of filter



Ripple characteristics in pass band

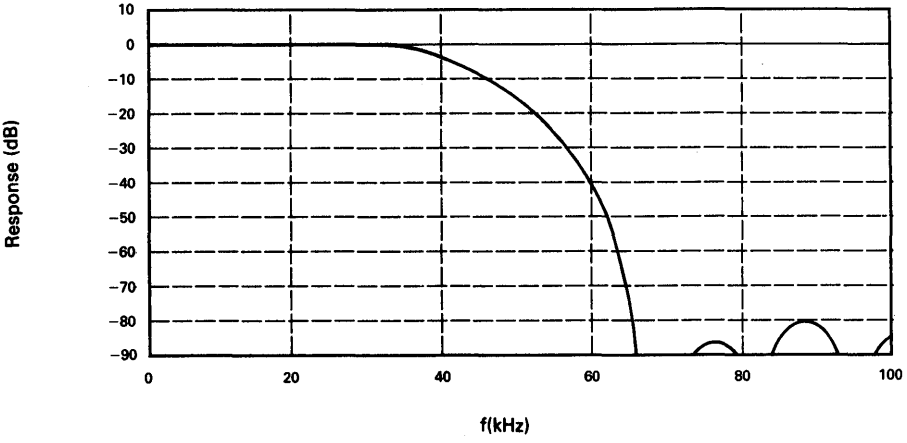


Filter Characteristics-3

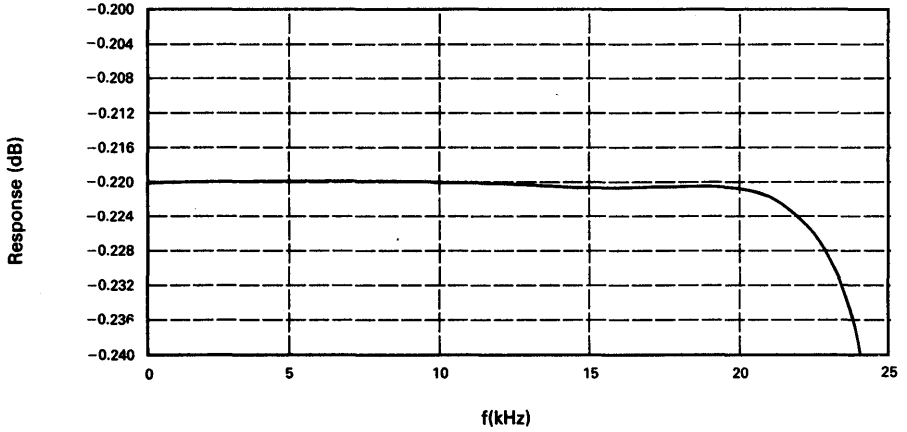
2nd Filter (21st order, ROM2="H")

- Marked flatness in pass band (without frequency characteristics compensation)

Frequency characteristics of filter



Ripple characteristics in pass band

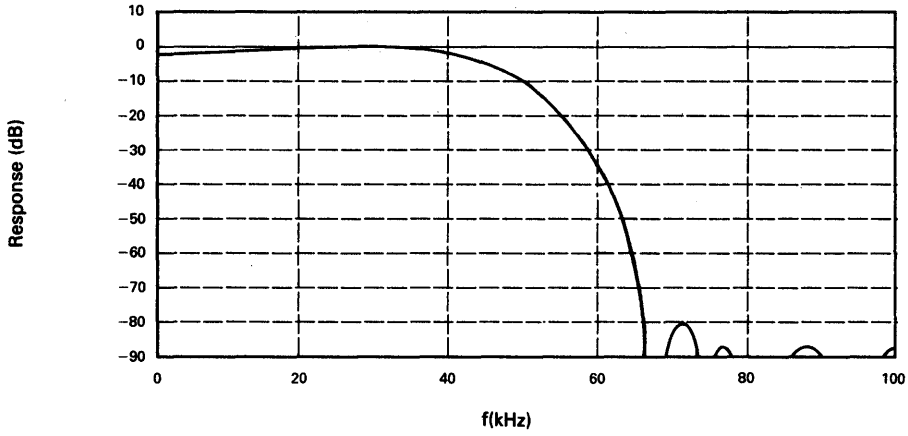


Filter Characteristics-4

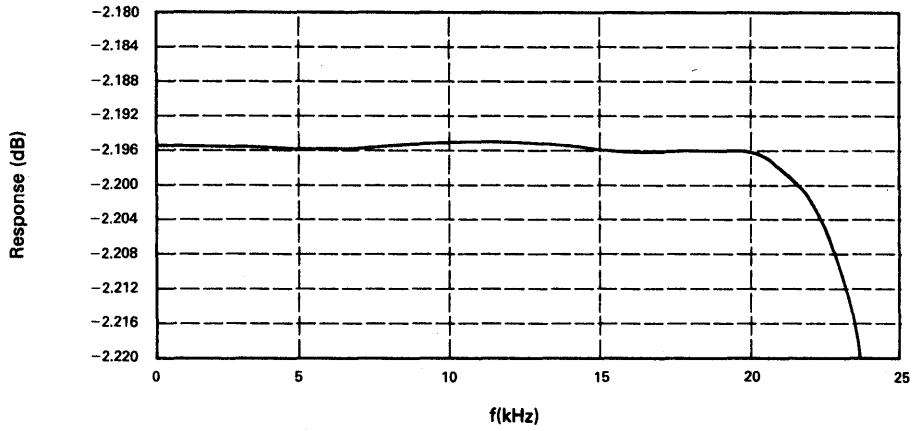
2nd Filter (21st order, ROM2="L")

- Pass band frequency characteristics (compensation of aperture effect of analog third order Bessel filter characteristics)

Frequency characteristics of filter



Ripple characteristics in pass band
(Excluding frequency characteristics compensation)



Over Sampling Digital Filter LSI

Description

CXD1144BP is a over sampling digital filter LSI developed for CD player and digital PB system.

Features

- Filtering with quadrupled/octupled over sampling.
- Filter characteristics
  Ripple : within ± 0.00001dB
  Attenuation : under − 120dB
- Deemphasis function (when quadrupled)

Application

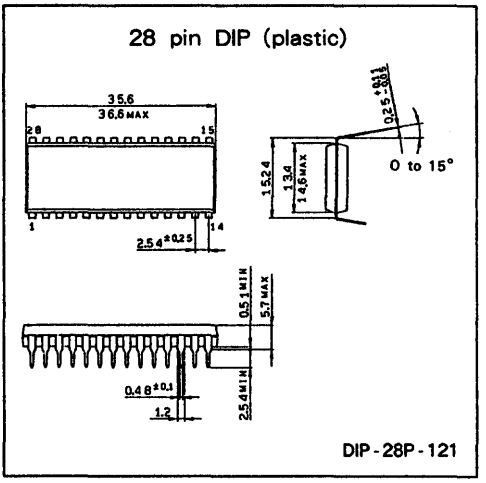
- Compact disc player, Digital amplifier.

Structure

CMOS − IC

Package Outline

Unit : mm



Function

- Built-in filters for 2 channels.
- Filtering with quadrupled/octupled over sampling.
  3 stage FIR filters interconnected in cascade (293rd).
- Filter characteristics
  Ripple : within ± 0.00001dB (0 to 20kHz)
  Attenuation : under − 120dB (24.1k to 150kHz)
- Serial I/O data
  Format : 2's complement MSB first (serial)
  Word length : 16/18bit
- Soft-muting function
- Deemphasis function (when quadrupled)

Absolute Maximum Ratings (Ta = 25 °C)

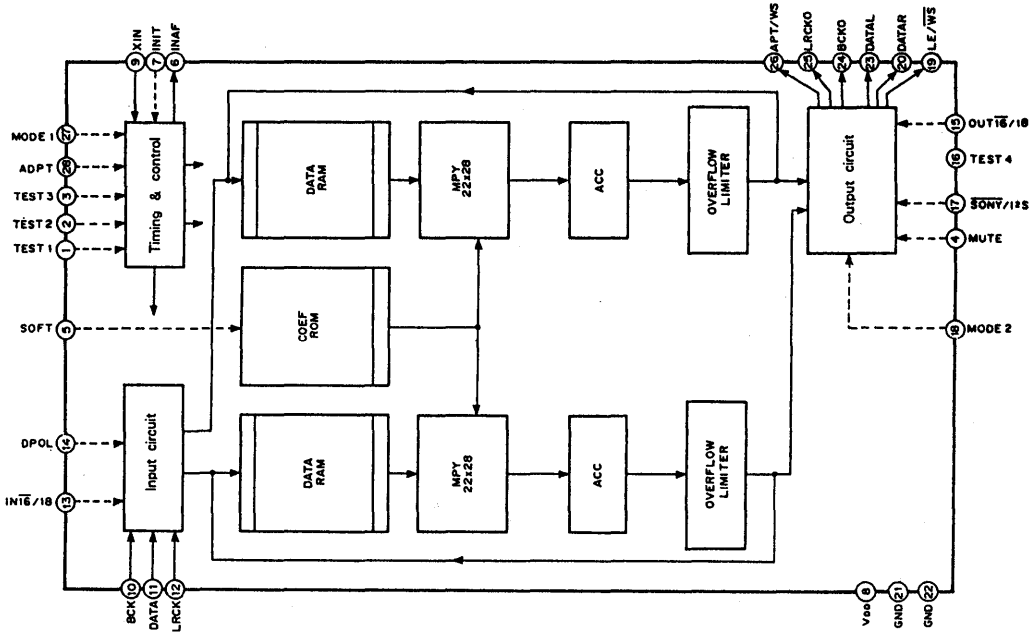
• Supply voltage	V_{DD}	− 0.5 to + 6.5	V
• Input voltage	V_I	− 0.5 to V_{DD} + 0.5	V
• Storage temperature	Tstg	− 55 to + 150	℃
• Allowable power dissipation	P_D	500	mW (Ta = 60 ℃)

Recommended Operating Conditions

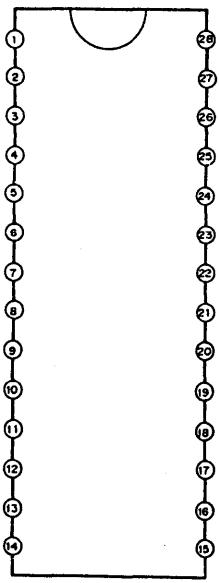
• Supply voltage	V_{DD}	4.75 to 5.25	V
• Operating temperature	Topr	− 10 to 60	℃
• OSC frequency	fx	12.0 to 18.5	MHz

E88Z15 − ST

Block Diagram



Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description
1	TEST1	I	Test pin ; fixed at "L" level in usual operation.
2	TEST2	I	Test pin ; fixed at "L" level in usual operation.
3	TEST3	I	Test pin ; fixed at "L" level in usual operation.
4	MUTE	I	Nullifies output to "0" value ; valid at "H".
5	SOFT	I	ON/OFF for soft muting ; muting at "H".
6	INAF	O	Outputs "H" when input/output synchronization is off.
7	INIT	I	Resynchronization at rising edge of signal.
8	V_{DD}	—	+ Power supply (+5V).
9	XIN	I	Master CLK input (f = 384 fs).
10	BCK	I	BCK input.
11	DATA	I	Serial data input (complement of 2).
12	LRCK	I	LRCK input.
13	IN$\overline{16}$/18	I	Specification of input data word length ; "H" ; 18 bits, "L" ; 16 bits.
14	DPOL	I	Inverts the polarity of input data.
15	OUT$\overline{16}$/18	I	Specification of output data word length, "H" : 18 bits, "L" ; 16 bits.
16	TEST4	I	Test pin ; fixed at "H" level in usual operation.
17	$\overline{SONY}$/I²S	I	Specification of output format ; "H" : I²S, "L" : SONY.
18	MODE2	I	Specification of ADPT ; "H" : 8Fs, "L" : EMP. *
19	LE/$\overline{WS}$	O	LE output (in SONY mode) /$\overline{WS}$ output (in I²S mode).
20	DATAR	O	RCH serial data output (complement of 2)
21	GND	—	
22	GND	—	
23	DATAL	O	LCH serial data output (complement of 2)
24	BCKO	O	BCK output
25	LRCKO	O	LRCK output
26	APT/WS	O	APT output (in SONY mode) /WS output (in I²S mode).
27	MODE1	I	Specification of ADPT ; "H" : 8Fs, "L" : EMP. *
28	ADPT	I	ON/OFF for ADPT ; ON at "H".

* **Note)** MODE1 and MODE2 should have the same polarity.

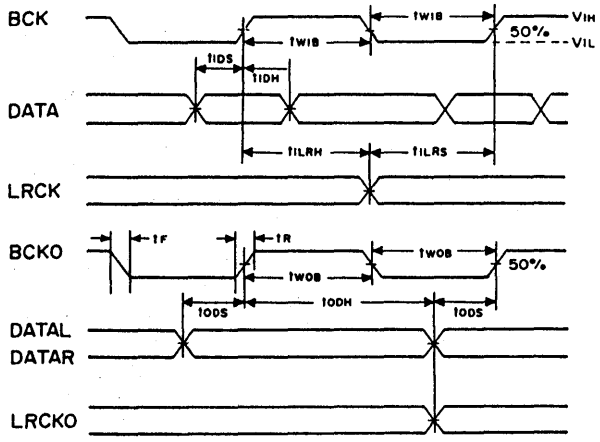
Electrical Characteristics

DC characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}		0.76V_{DD}			V
"L" input voltage	V_{IL}				0.24V_{DD}	V
Input leak voltage	I_{LI}				±5	μA
"H" output voltage	V_{OH}	Io = −2mA (BCK) Io = −1mA (Others)	V_{DD} − 0.5 V_{DD} − 0.5			V V
"L" output voltage	V_{OL}	Io = 2mA (BCK) Io = 1mA (Others)			0.4 0.4	V V

AC characteristics

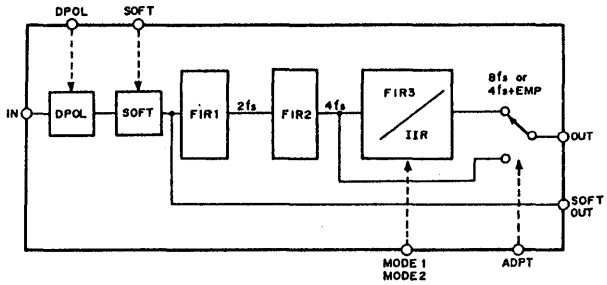
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
OSC frequency	fx		12.0	16.9	18.5	MHz
Input BCK frequency	fBCK				2.31	MHz
Input BCK pulse width	tWIB	DUTY : 50 ± 10%	100			ns
Input data set up time	tIDS		20			ns
Input data hold time	tIDH		20			ns
Input LRCK set up time	tILRS		50			ns
Input LRCK hold time	tILRH		50			ns
Output BCK pulse width	tWOB	fx = 16.9MHz SONY output mode 8Fs, BCK24 CL = 25pF BCKOCL = 50pF	40			ns
Output data set up time	tODS		25			ns
Output data hold time	tODH		25			ns
Output BCK pulse width	tWOB	fx = 16.9MHz I²S output mode 8Fs, CL = 25pF BCKOCL = 50pF	60			ns
Output data set up time	tODS		35			ns
Output data hold time	tODH		35			ns
Output BCK pulse width	tWOB	fx = 18.5MHz SONY output mode 8Fs, BCK24 CL = 25pF BCKOCL = 50pF	40			ns
Output data set up time	tODS		20			ns
Output data hold time	tODH		20			ns
Output BCK pulse width	tWOB	fx = 18.5MHz I²S output mode 8Fs, CL = 25pF BCKOCL = 50pF	60			ns
Output data set up time	tODS		32			ns
Output data hold time	tODH		32			ns
Output signal rise/fall time	tR, tF	CL = 25pF BCKOCL = 50pF			30	ns



Function

1. Conceptual block diagram

A conceptual block diagram of this LSI is shown in the following figure :



SOFT OUT (1fs) is output from DATA R only in I²s 4fs mode.

2. Selection of over-sampling mode

The following three modes are selectable via ADPT, MODE1 and MODE2 pins :

- 4fs mode
- 4fs + emphasis mode
- 8fs mode.

ADPT \ MODE1 MODE2	"H"	"L"
"H"	8fs	4fs + emphasis
"L"	4fs	4fs

The time constant for emphasis takes values of $\tau 1 = 50\ \mu s$ and $\tau 2 = 15\ \mu s$ at fs = 44.1 kHz.

3. Soft muting

This function smoothly conducts muting and releases muting of data by turning ON/OFF the SOFT pin. ON/OFF switchover is not applicable within 30 ms.

4. Input/output synchronization circuit

1) Principle

In the synchronizing circuit, a window for 10 clocks of the internal system clock (XIN/2) is provided to monitor as to whether or not the rising edge of LRCK (LRCK ⎍) to be entered is within this window. When LRCK ⎍ is outside the window upon turning on power, the synchronizing circuit causes the internal processing to discontinue at timing of the window center, and causes it to start upon appearance of the next LRCK ⎍. This action ensures synchronization between an external system and this LSI.

2) Resynchronization by INIT.

Even when the LRCK ∫ is outside the window, synchronization may be off due to the mixture of external noise if the LRCK ∫ is located near an end of the window. To avoid this, it is necessary to apply resynchronization without fall after turning on power. Resynchronizing action is done at timing of rising of INIT and initializes the synchronizing circuit to locate the LRCK ∫ at the window center. When synchronization is off, INAF output becomes on "H" level.

5. Muting

Muting is applied to data entered into the LSI when :

INIT : "L" and "0" data are entered.

Output data become "0" data when :

INIT : "L" or MUTE : "H".

6. Data polarity

The DPOL pin permits switchover between invert and non-invert of output data.

DPOL : "L" ··· non-invert

DPOL : "H" ··· invert.

7. Latch timing of input/output signals

1) Inputs IN$\overline{16}$/18, DPOL, SOFT, MUTE, OUT$\overline{16}$/18, $\overline{SONY}$/I²S, ADPT, MODE1 and MODE2 : These input signals are latched by an internal clock corresponding to LRCK.

2) Outputs LRCK0, BCK0, DATAL, DATAR, APT/WS and LE/$\overline{WS}$: These output signals are latched by an internal clock corresponding to BCK0.

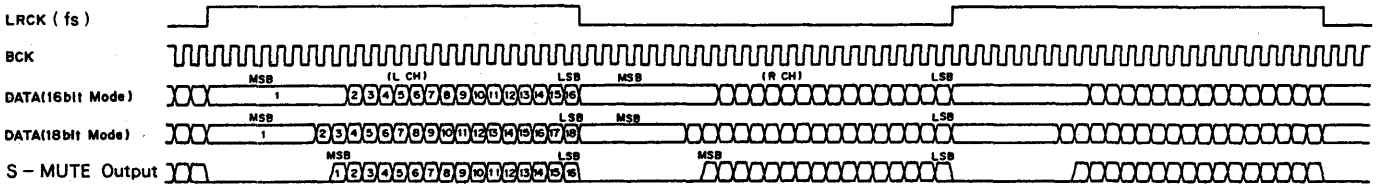
8. Selection of output format

An output format for this LSI is selected as shown in the following table :

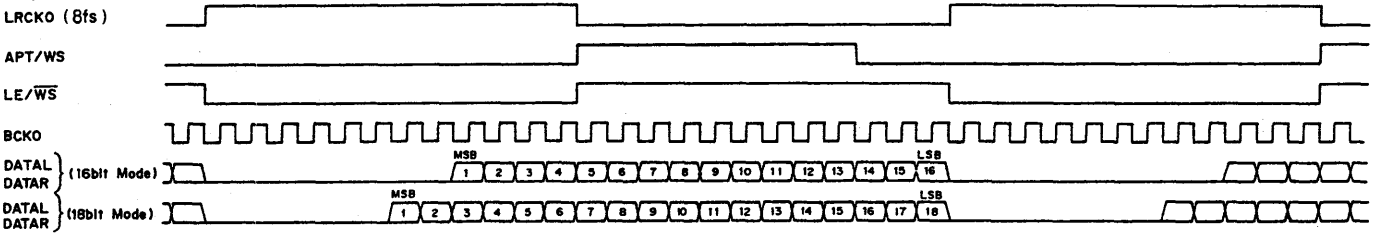
	4fs			8fs		
	SONY mode, 16-bit output	SONY mode, 18-bit output	I²S mode	SONY mode, 16-bit output	SONY mode, 18-bit output	I²S mode
< Control pin >						
ADPT	ON/OFF	←	←	ON	←	←
MODE1	4fs	←	←	8fs	←	←
MODE2	4fs + EMP	←	←	8fs	←	←
$\overline{SONY}$/I²S	SONY	←	I²S	SONY	←	I²S
OUT$\overline{16}$/18	16	18	Invalid	16	18	Invalid
< Output pin >						
LRCKO	4LRCK	←	←	8LRCK	←	4LRCK
BCKO	24	24	16	24	24	16
DATAL/DATA	DATAL	←	MIX DATA	DATAL	←	Composite DATA
DATAR/S-MUTE	DATAR	←	S-MUTE	DATAR	←	Composite DATA
APT/WS	APT	←	WS	APT	←	WS
LE/$\overline{WS}$	LE	←	$\overline{WS}$	LE	←	$\overline{WS}$

I/O Timing Chart

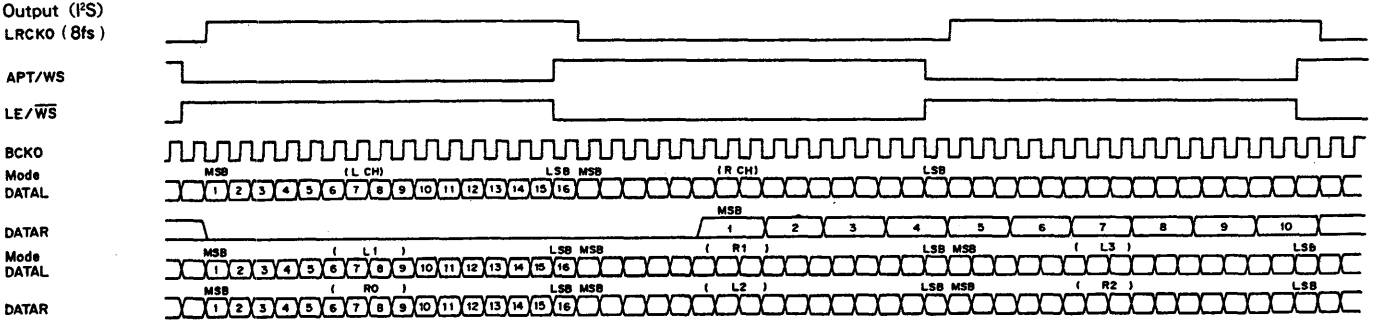
(1) Input



(2) Output (SONY)



(3) Output (I^2S)



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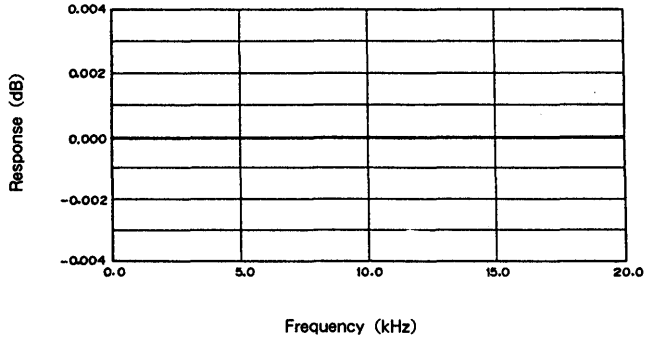
CXD1144BP

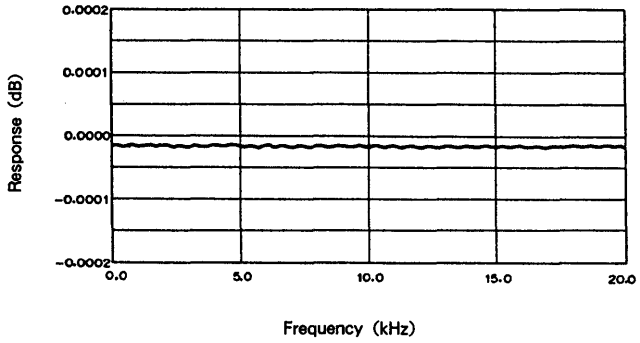
Filter Characteristics

1) 4fs Mode (ADPT = L, MODE1 = MODE2 = H)

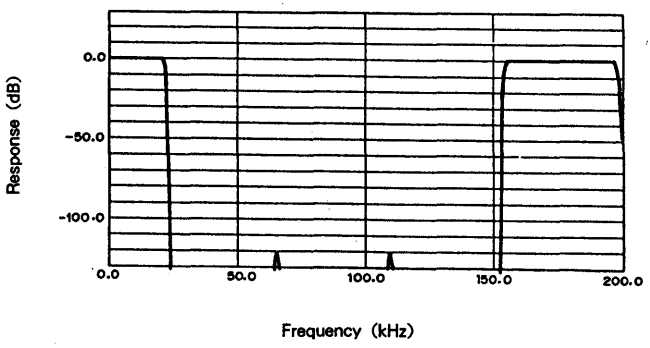
Frequency characteristics



Ripple characteristics

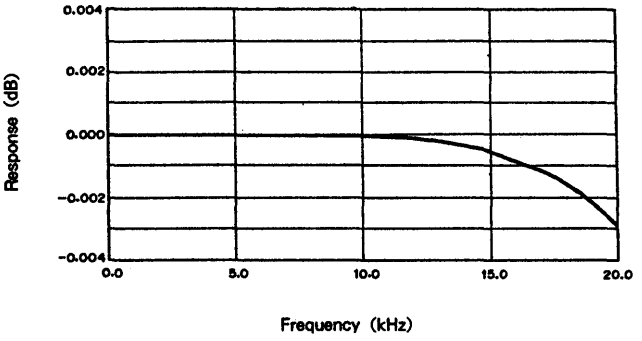


Attenuation characteristics

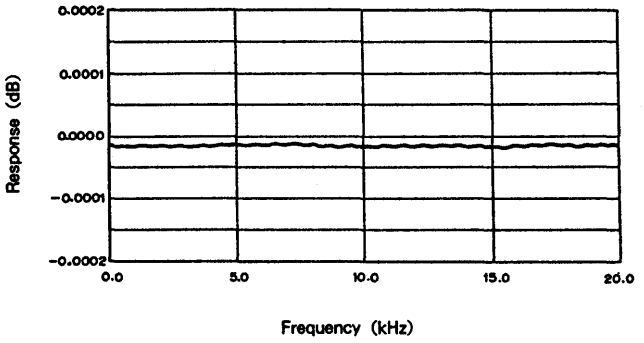


2) 8fs Mode (ADPT = MODE1 = MODE2 = H)

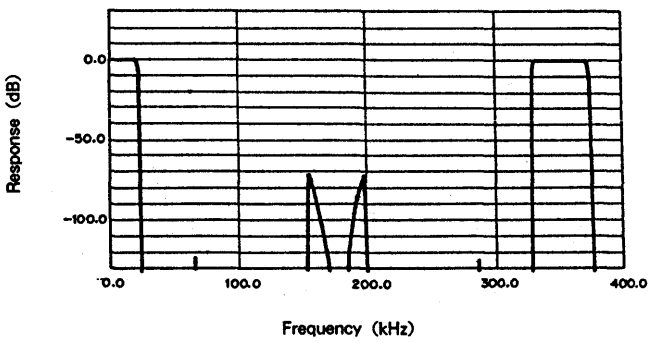
Frequency characteristics



Ripple characteristics



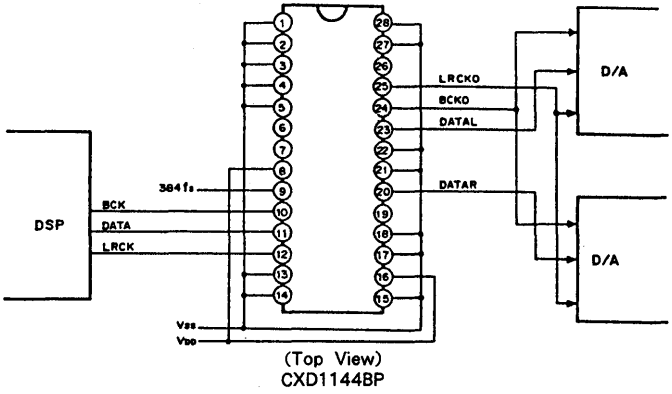
Attenuation characteristics



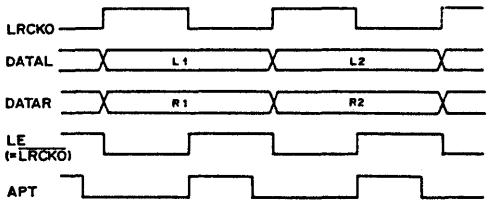
Application Circuit

1) 4fs

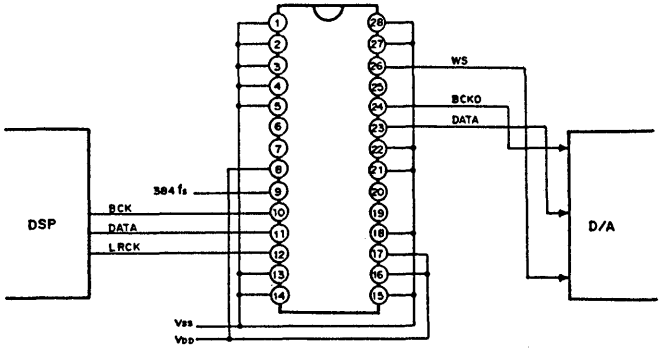
SONY Mode



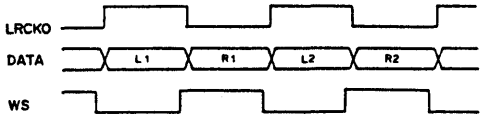
(Top View)
CXD1144BP



I²S Mode

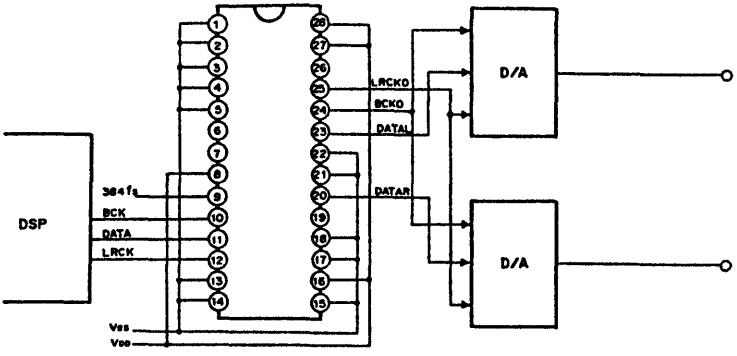


(Top View)
CXD1144BP

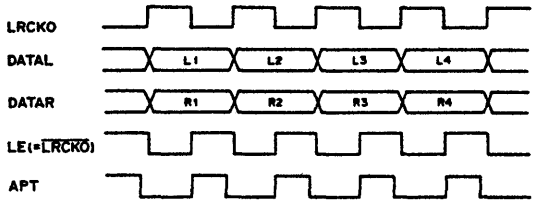


2) 8fs

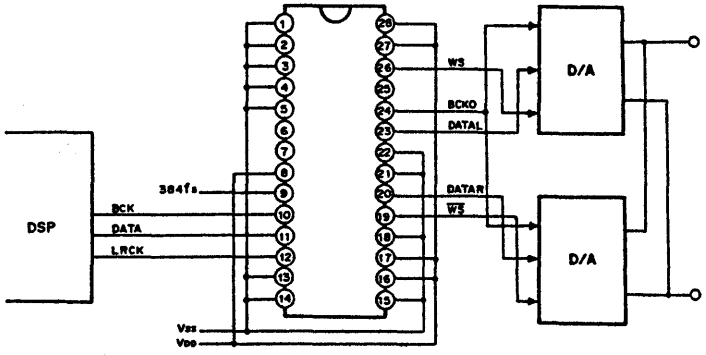
SONY Mode



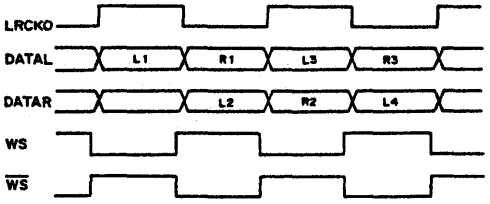
(Top View)
CXD1144BP



I²S Mode



(Top View)
CXD1144BP



SONY **CXD1162P**

Over Sampling Digital Filter LSI

Description

The CXD1162P is a digital filter LSI with guadrupled sampling rate, developed for compact disc player.

Features

- 83 taps and 21 taps filters linked through cascade connections provide a guadrupled sampling digital filter.
- Built-in filters for 2 channels correspond to L and R.
- A varity of functions, including soft muting.
- 83rd and 21st order filters have 2 modes of filter coefficients each, that enable the selection of the filter characteristics most suitable for usage.

Function

- Built-in filters for 2 channels
- Filtering with a quadrupled sampling rate
- 2-stage FIR filters interconnected in cascade (83 taps+21 taps)
- Soft-muting function
- Independent linear interpolation for either L or R, up to 8 words.
- 2 modes of coefficients provided for both 83 taps and 21 taps (See the Filter Characteristics)

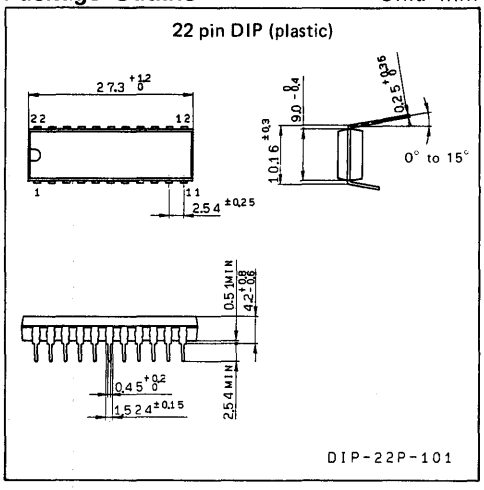
- Input/Output format
  Input: 2's complement MSB first (serial)
  Output: 2's complement MSB first (serial)

Structure

Silicon gate CMOS IC

Package Outline

Unit: mm



Absolute Maximum Ratings (Ta=−20 to +75°C)

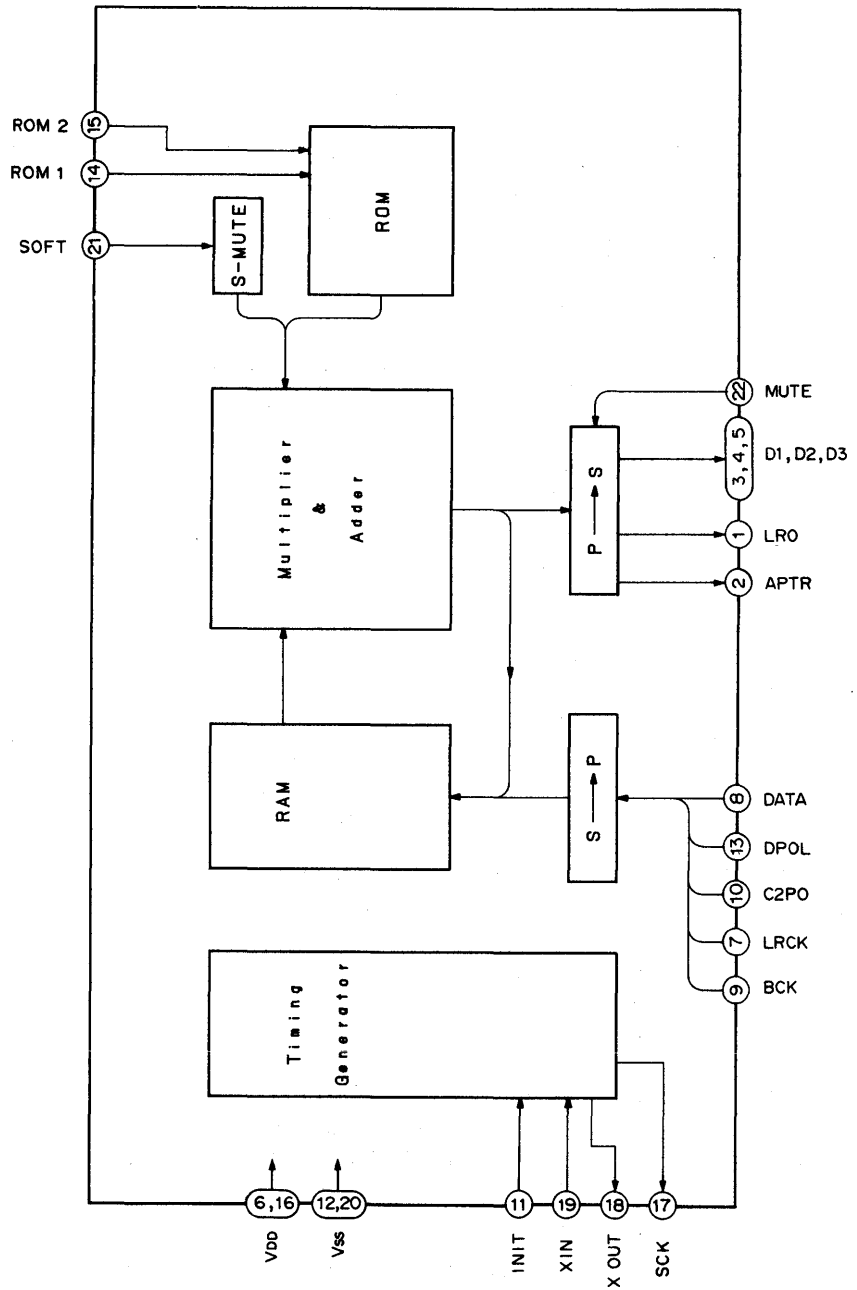
• Supply voltage	V_{DD}	−0.5 to +6.5	V
• Input voltage	V_I	−0.5 to V_{DD}+0.5	V
• Allowable power dissipation	P_D	550	mW (Ta=75°C)
• Storage temperature	Tstg	−55 to+150	°C

Recommended Operating Conditions

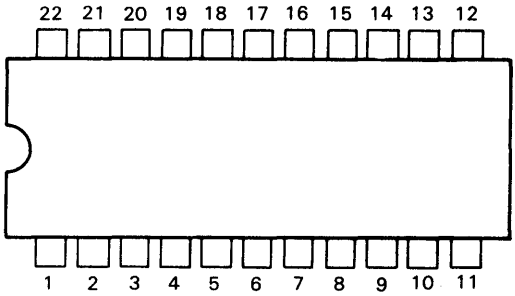
• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature	Topr	−20 to +75	°C
• OSC frequency	fx	10 to 20	MHz

70922-ST

Block Diagram



Pin Configuration and Description (Top View)



No.	Symbol	I/O	Description
1	LRO	O	LRCK output (4fs)
2	APTR	O	Aperture clock for R aperture
3	D_1	O	BCK output (4fs)
4	D_2	O	DATA output (4fs)
5	D_3	O	WCK output
6	V_{DD}	–	Positive supply (+5V)
7	LRCK	I	LRCK input
8	DATA	I	16 bit 2 serial data input 2'scomplement
9	BCK	I	BCK input
10	C2PO	I	Error flag input
11	INIT	I	Power on reset input. Active at "L"
12	V_{SS}	–	Negative supply (0V)
13	DPOL	I	Reveses input data polarity
14	ROM1	I	ROM switching for 83rd order (See the Filter Characteristics)
15	ROM2	I	ROM switching for 21st order (See the Filter Characteristics)
16	V_{DD}	–	Positive supply (+5V)
17	SCK	O	System clock output for external IC (384fs)
18	XOUT	O	Output of crystal oscillation cirucit (384fs)
19	XIN	I	Input of crystal oscillation circuit (384fs)
20	V_{SS}	I	Negative supply (0V)
21	SOFT	I	Soft muting ON/OFF switch. On at "H" level
22	MUTE	I	"H" level

Electrical Characteristics

DC characteristics

V_{DD}=4.5 to 5.5V, Ta=−20 to +75°C

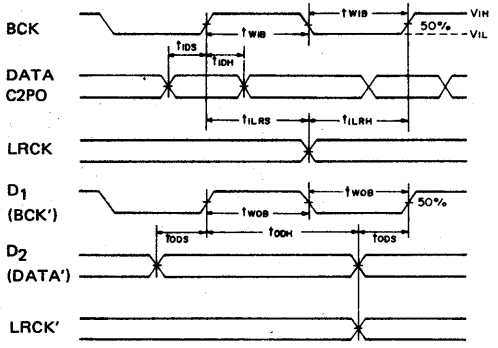
No.	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
19 XIN	Input leak current	I_{LI}	$V_I=V_{DD}/0V$	–	–	±20	μA
All inputs	"H" input voltage	V_{IH}	–	0.76V_{DD}	–	–	V
	"L" input voltage	V_{IL}	–	–	–	0.24V_{DD}	
	Input leak current	I_{LI}	$V_I=V_{DD}/0V$	–	–	±5	μA
	Input capacity	C_{IN}	–	–	4	6	PF
1 LRO 2 APTR 4 D1 4 D2 5 D3	"H" output voltage	V_{OH}	I_O=−4 mA	V_{DD}−0.5	–	–	V
	"L" output voltage	V_{OL}	I_O=4 mA	–	–	0.4	
17 SCK	"H" output voltage	V_{OH}	I_O=−5 mA	V_{DD}−1.0	–	–	V
	"L" output voltage	V_{OL}	I_O=5 mA	–	–	1.0	
	Current consumption	I_{DD}	Unload $V_I=V_{DD}/0V$ fx=16.93 MHz	–	–	40	mA

AC characteristics

V_{DD}=4.5 to 5.5V, Ta=−20 to +75°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillating frequency	fx t		–	16.9344	20.0	MHz
Input BCK frequency	f_{BCK}		–	–	3.5	MHz
Input BCK pulse width	t_{WIB}		100	–	–	ns
Input data set-up time	t_{IDS}		20	–	–	ns
Input data hold time	t_{IDH}		20	–	–	ns
Input LRCK set-up time	t_{ILRS}		50	–	–	ns
Input LRCK hold time	t_{ILRH}		50	–	–	ns
Output BCK pulse width	t_{WOB}	f_{XT}=16.9344 MHz C_L=50 pF	45	–	–	ns
Output data set-up time	t_{ODS}		30	–	–	ns
Output data hold time	t_{ODH}		40	–	–	ns

AC characteristics



Description of Functions

1. Soft muting

Mutes or de-mutes output data within approximately 46 mS (2048/fs).

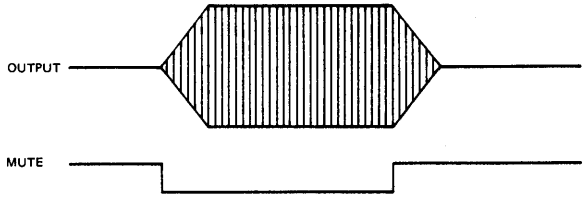


Fig. 1

2. Muting

When MUTE goes high or INIT goes low, the output is muted.

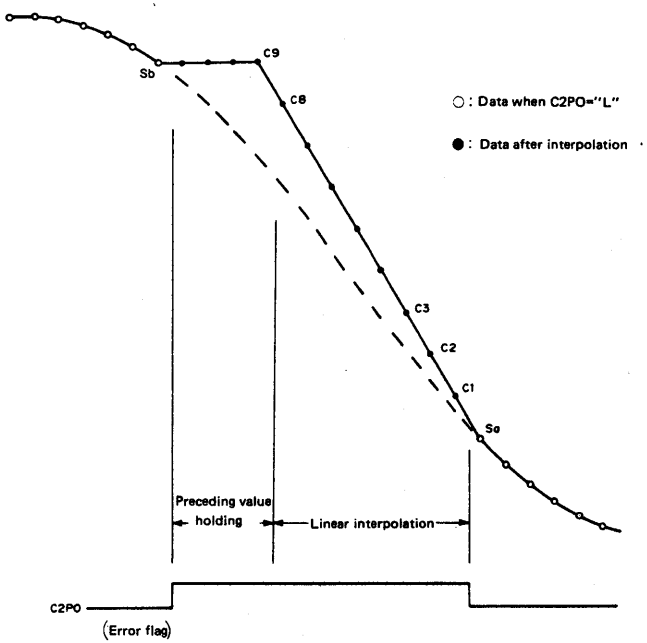
3. Data polarity

Allows switching between inversion and non-inversion of output data.

When DPOL level is "H", the output data is inversed with respect to the input data.

4. Interpolation

Error in an input data block consisting of up to eight consecutive data units can be linearly interpolated by two correct data units, namely, the one preceding the erroneous block and the other following it. (This is done separately for L and R.). For errors of more than eight consecutive input data units, only the last eight data are linearly corrected, and all preceding data units are maintained without correction.



5. Input and output

1) Input

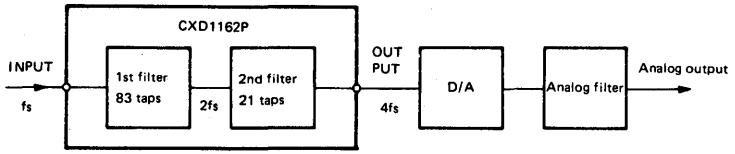
The changeover point of MSB first serial data (fs) of 2's complement represents the switching of LRCK of this data string, only the data of the last 16-bit clock (BCK) are valid.

When INIT="L" (resetting), the input data are invalid and the input is equivalent to ALL "0".

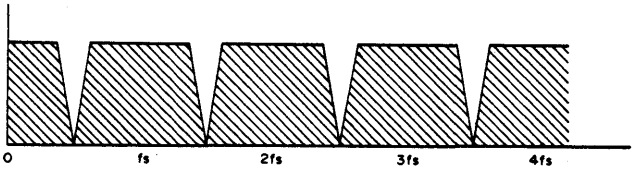
2) Output

MSB first serial data (4fs) of 2's complement clock pulses such as LRO and BCK are output only when resetting is canceled (INIT="H") and MUTE="L". Otherwise, muting remains effective.

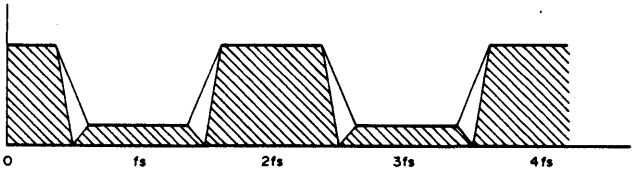
Filter Characteristics



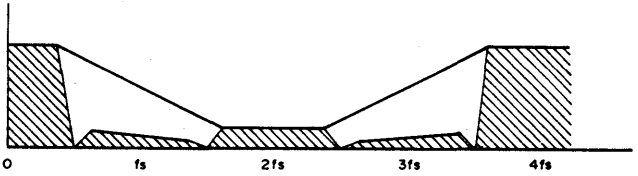
Input spectrum



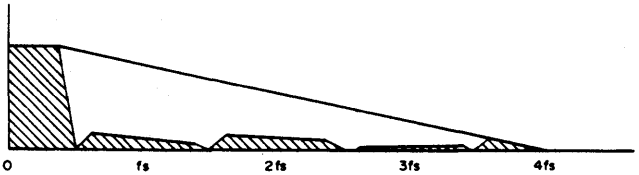
Characteristics of 1st filter



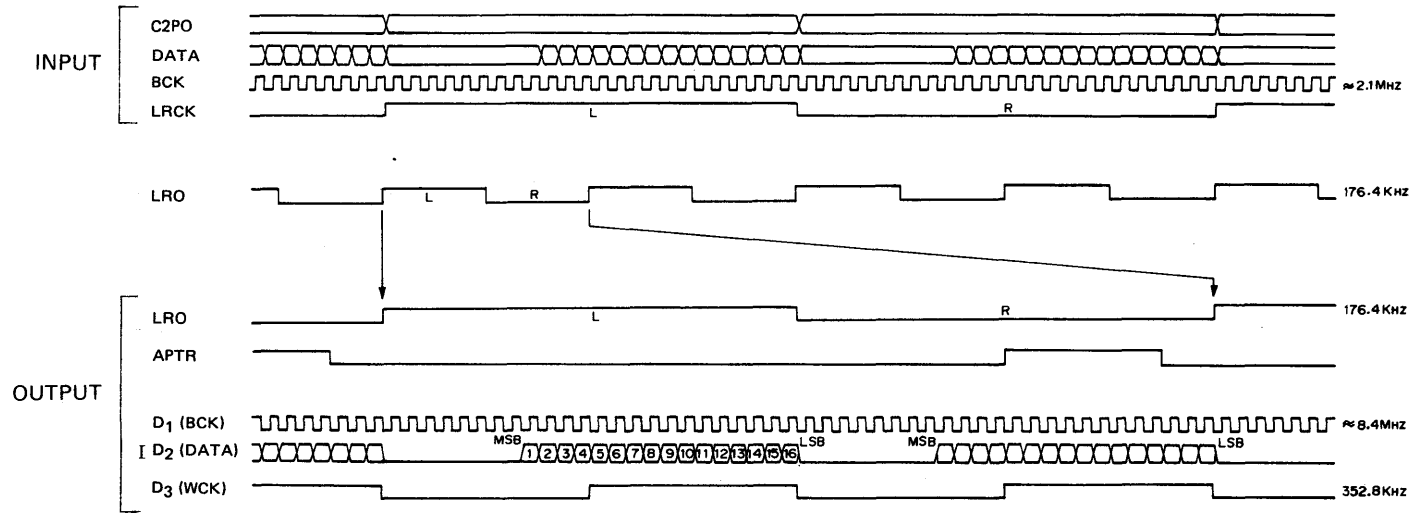
Characteristics of 2nd filter



Characteristics of analog filter

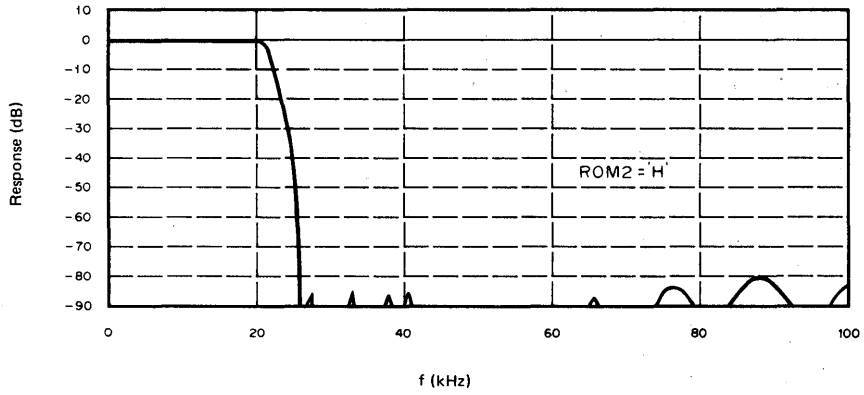


I/O Timing Chart

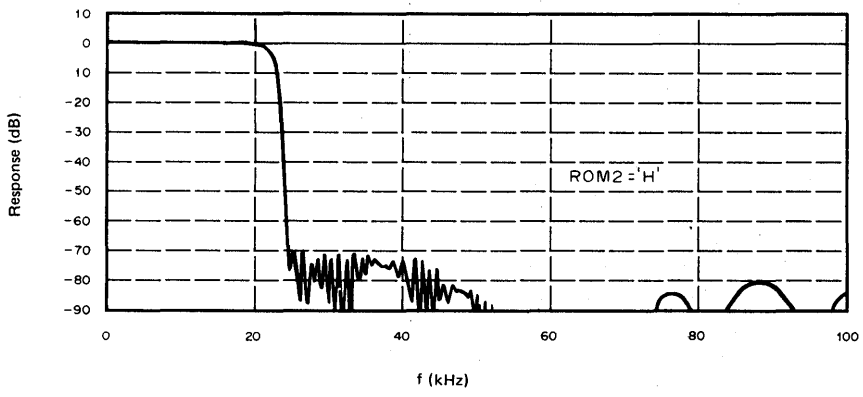


Combined Filter Characteristics (1st filter+2nd filter)

1) ROM1="H"
Stop band attenuation: 80 dB Min. (over 25.7 kHz)
Pass band ripple: 0.001 dB Max.

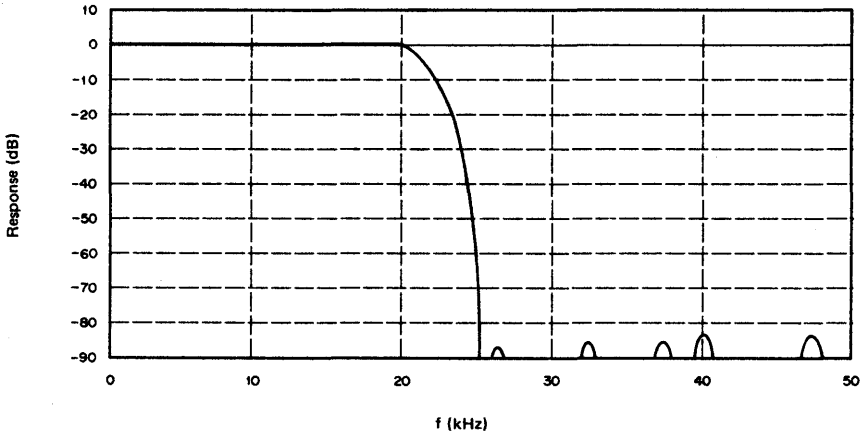


2) ROM1="L"
Stop band attenuation: 60 dB Min. (24.1 kHz): 65 dB Min.
Pass band ripple: 0.004 dB Max.

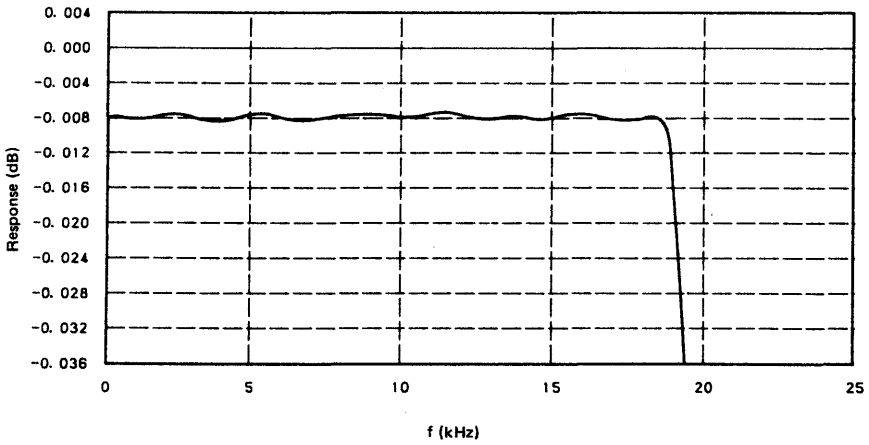


Filter Characteristics-1

1st Filter+(83 taps ROM1="H")



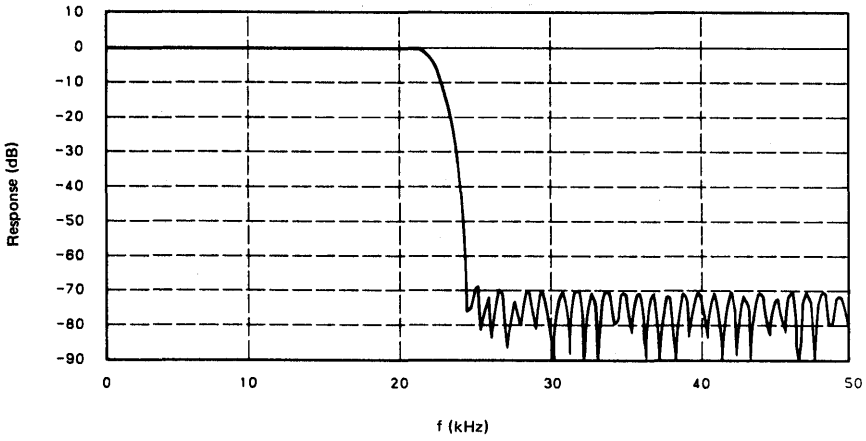
Filter frequency characteristics



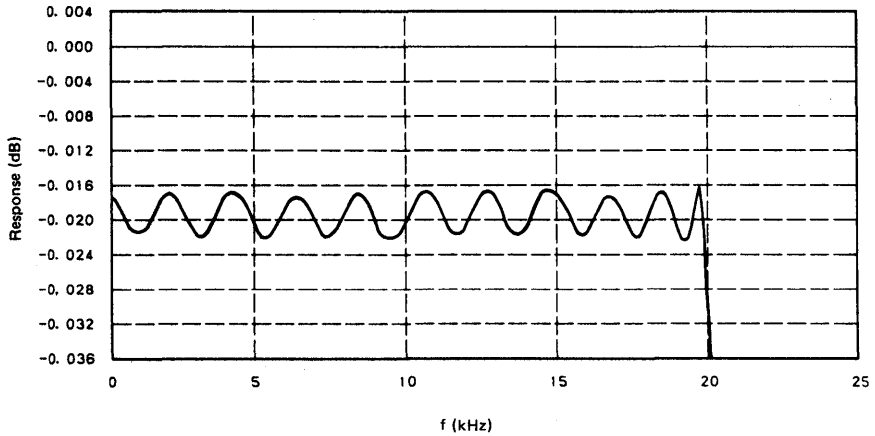
Pass band ripple characteristics

Filter Characteristics-2

1st Filter (83 taps ROM1="L")



Filter frequency characteristics

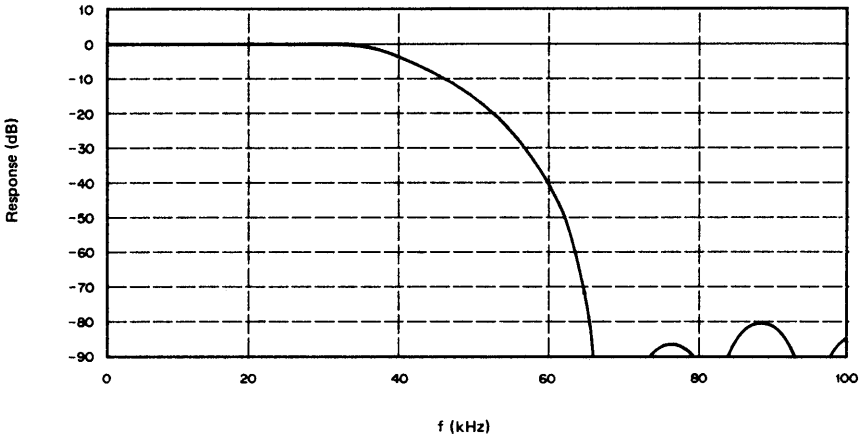


Pass band ripple characteristics

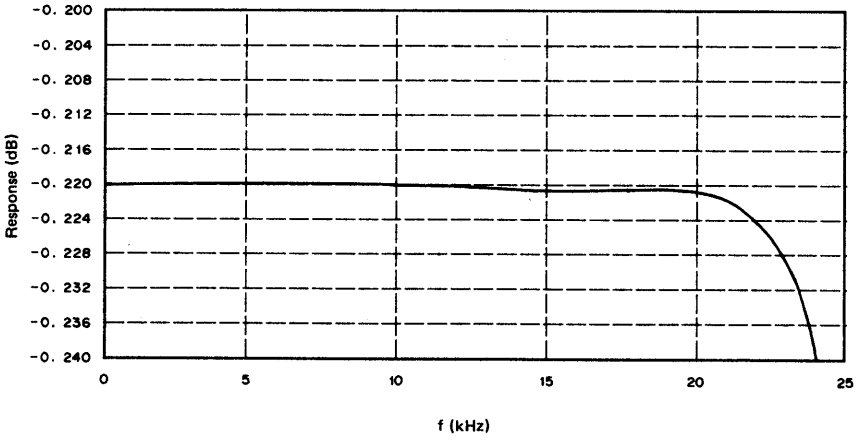
Filter Characteristics-3

2nd filter (21 taps, ROM2="H")

- Pass band flat (without frequency characteristics compensation)



Filter frequency characteristics

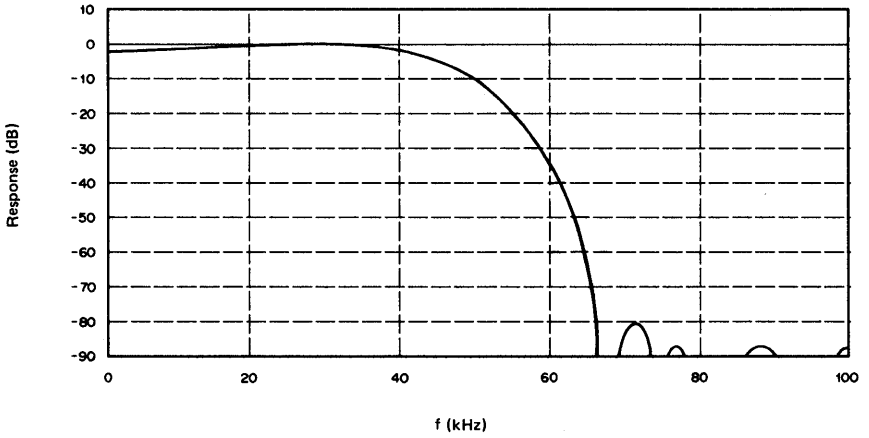


Pass band ripple characteristics

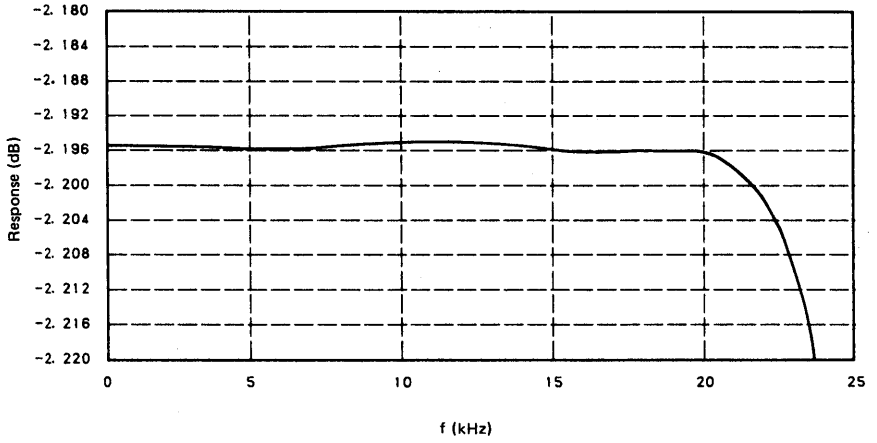
Filter Characteristics-4

2nd filter (21 taps, ROM2="L")

- Pass band frequency characteristics (compensation of aperture effect and analog 3rd order Bessel filter characteristics)



Filter frequency characteristics



Pass band ripple characteristics
(Excluding frequency characteristics compensation)

Over Sampling Digital Filter LSI

Description

CXD1244S is a digital filter LSI with 4-times/8-times over sampling rate, developed for compact disc player.

Features

- Built-in 4-times/8-times sampling digital filter for 2 channels.
- Ripple within 0.00001dB
- Attenuation within -100dB(24.1k).
- Noise shaping, Attenuator
- Soft muting, de-emphasis and a wide variety of built-in functions.

Application

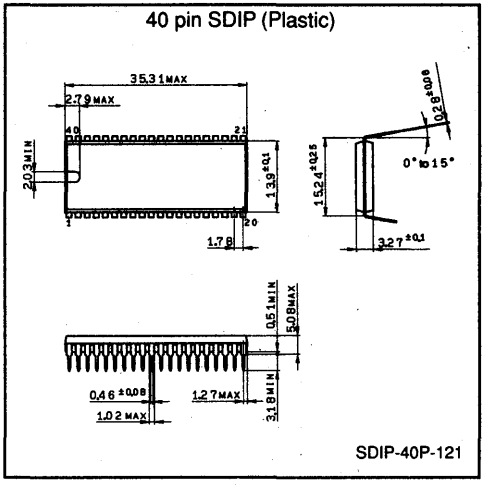
Compact disc player

Structure

Silicon gate CMOS IC

Package Outline

Unit: mm



Absolute Maximum Ratings (Ta=25°C)

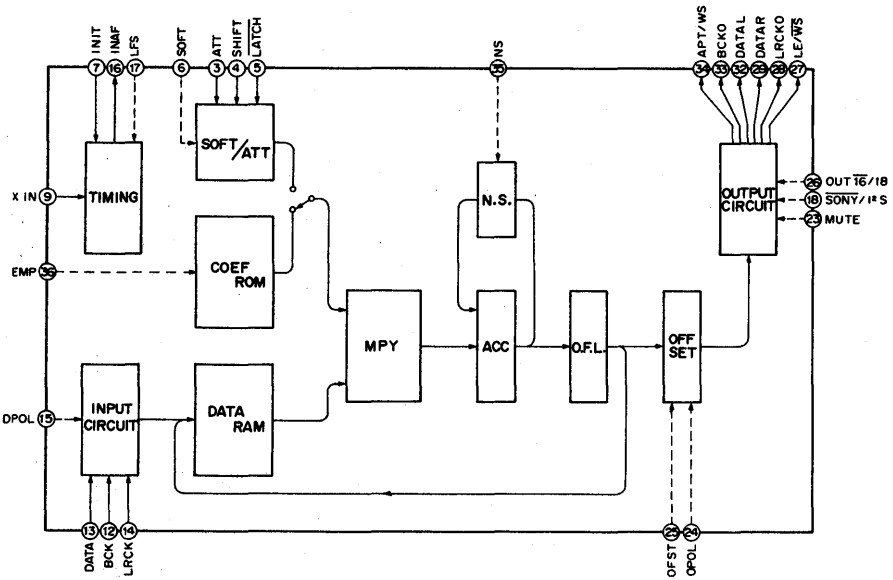
• Supply voltage	V_{DD}	−0.5	to	+6.5	V	
• Input voltage	V_I	−0.5	to	V_{DD} +0.5	V	
• Storage temperature	Tstg	−55	to	+150	°C	
• Allowable power dissipation	P_D			500	mW	(Ta=60°C)

Recommended Operating Conditions

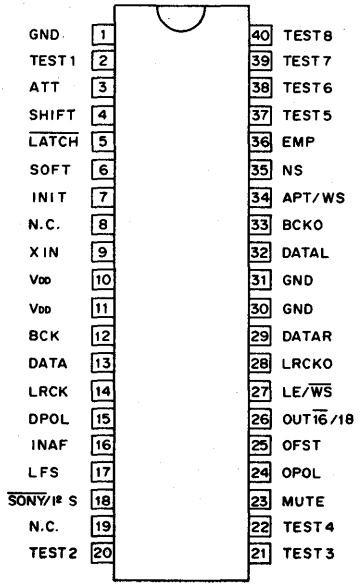
• Supply voltage	V_{DD}	4.75	to	5.25	V
• Operating temperature	Topr	−10	to	+60	°C
• OSC frequency	fx	12.0	to	18.5	MHz

81114-YA

Block Diagram



Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description
1	GND	—	
2	TEST1	I	Test pin (Normally fixed to "L" level)
3	ATT	I	Attenuate data input
4	SHIFT	I	Attenuate data shift clock input
5	LATCH	I	Attenuate data latch clock input
6	SOFT	I	Soft muting ON/OFF active at "H".
7	INIT	I	Synchronous again with the rising edge of this signal.
8	NC		
9	XIN	I	Master CLK input (f=384 Fs)
10, 11	V_{DD}	—	Supply (+5V)
12	BCK	I	BCK input
13	DATA	I	Serial data input (2's complement)
14	LRCK	I	LRCK input
15	DPOL	I	Output data polarity "L" : non inversion "H" : inversion.
16	INAF	O	When I/O sync is missed "H" is output.
17	LFS	I	4Fs mode ON/OFF available at "H" only during I^2S.
18	SONY/I^2S	I	Output format specified at "L": Sony, at "H": I^2S
19	NC	I	
20 to 22	TEST 2 to 4	I	Test pin (Normally fixed to 'L' level)
23	MUTE	I	Turns output to 0 or offset value. Active at 'H'.
24	DPOL	I	Offset polarity 'L': (–) 'H': (+)
25	OFST	I	Offset ON/OFF Active at 'H'
26	OUT16/18	I	Output data word length specified at 'L': 16 bit at 'H': 18 bit
27	LE/WS	O	LE output (Sony format)/WS output (I^2S format)
28	LRCKO	O	LRCKO output
29	DATAR	O	Rch serial data output (2's complement)
30, 31	GND	—	
32	DATAL	O	Lch serial data output (2's complement)
33	BCKO	O	BCKO output
34	APT/WS	O	APT output (Sony format)/WS output (I^2S format)
35	NS	I	Noise shaping ON/OFF Active at 'H'
36	EMP	I	Deemphasis ON/OFF Active at 'H'
37 to 40	TEST 5 to 8	I	Test pin (Normally fixed to 'L' level)

Electrical Characteristics
DC characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
'H' input voltage (Except Shift, Latch)	V_{IH}	—	0.76 V_{DD}			V
'H' input voltage (Shift, Latch)						
'L' input voltage (Except Shift, Latch)	V_{IL}	—			0.24 V_{DD}	V
'L' input voltage (Shift, Latch)						
Input leak voltage	I_{LI}	—			±5	μA
'H' output voltage	V_{OH}	Io=-2mA	V_{DD}-0.5			V
'L' output voltage	V_{OL}	Io= 2mA			0.4	V

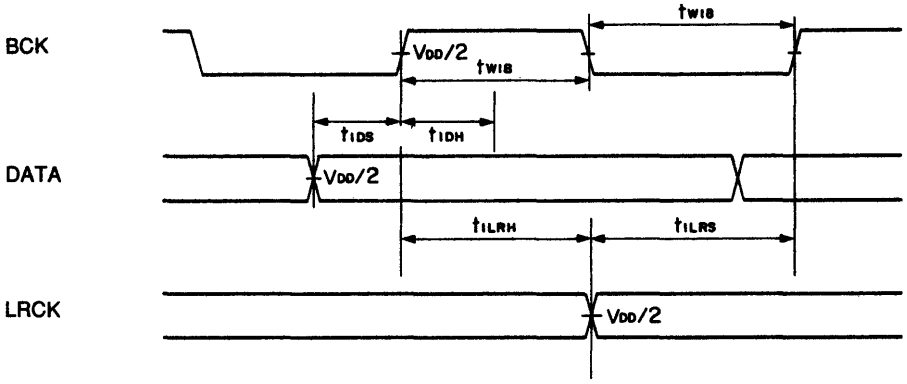
AC characteristics

Item	Symbol	Conditions	Min.	Typ.	Min.	Unit
OSC frequency	Fx		12.0	16.9	18.5	MHz
Input BCK frequency	F_{BCX}				2.31	MHz
Input BCK pulse width	t_{WIB}	Defined at Duty	40*	50	60	%
Input data set up time	t_{IDS}		20			ns
Input data hold time	t_{IDH}		20			ns
Input LRCK set up time	t_{ILRS}		50			ns
Input LRCK hold time	t_{ILRH}		50			ns
Output BCK pulse width	t_{WOB}	Fx=16.9MHz Sony output mode 8Fs. BCK24 CL=50pF	40			ns
Output data set up time	t_{ODS}		25			ns
Output data hold time	t_{ODH}		25			ns
Output BCK pulse width	t_{WOB}	Fx=16.9MHz I^2S output mode 8Fs. CL=50pF	60			ns
Output data set up time	t_{ODS}		35			ns
Output data hold time	t_{ODH}		35			ns
Output BCK pulse width	t_{WOB}	Fx=18.5MHz Sony output mode 8Fs. BCK24 CL=50pF	40			ns
Output data set up time	t_{ODS}		20			ns
Output data hold time	t_{ODH}		20			ns
Output BCK pulse width	t_{WOB}	Fx=16.9MHz I^2S output mode 8Fs. CL=50pF	60			ns
Output data set up time	t_{ODS}		32			ns
Output data hold time	t_{ODH}		32			ns
Output signal Rise/Fall time	t_R, t_F	CL=50pF			30	ns

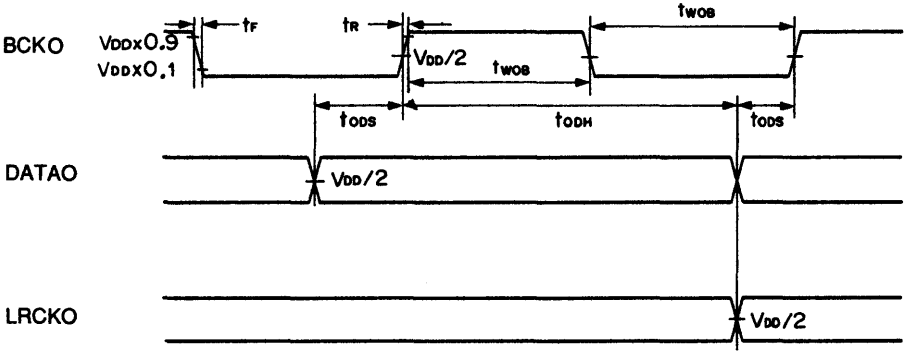
Note) Duty defined at 1/2 VDD, see the Timing Chart.

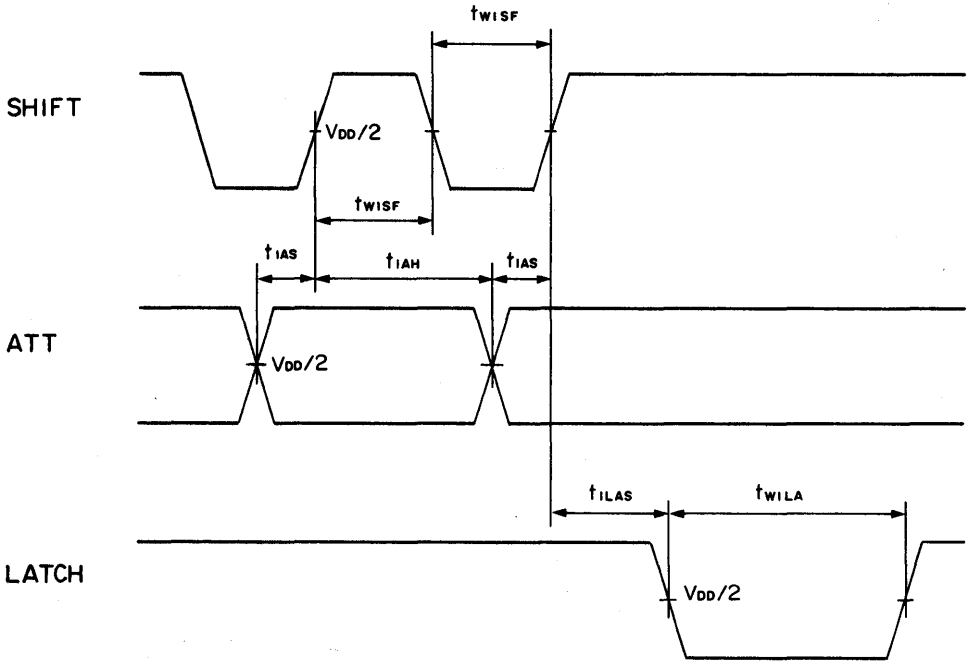
Timing Chart

• Input



• Output





Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift pulse width	TWISF		600			ns
ATT set up time	TIAS		300			ns
ATT hold time	TIAH		600			ns
Latch pulse width	TWILA		400			ns
Latch set up time	TILAS		500			ns

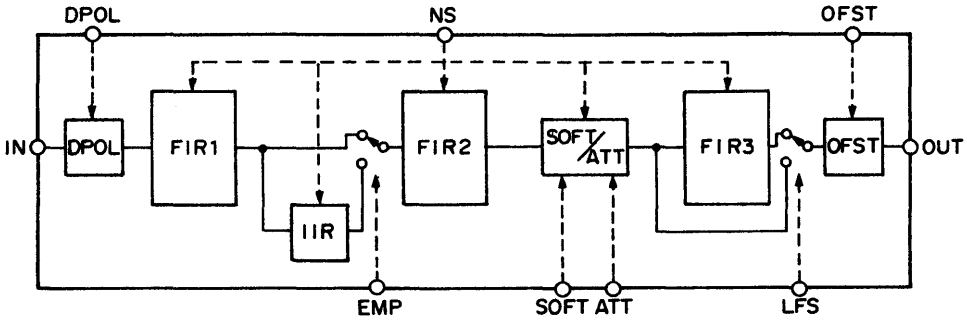
Schmitt input characteristics (SHIFT, LATCH)

	Min.	Typ.	Max.	Unit
V_{T+}	0.54×V_{DD}	3.0	0.76×V_{DD}	V
V_{T-}	0.24×V_{DD}	2.0	0.43×V_{DD}	V
HYST	0.52	1.0	———	V

Functions

Conceptual block diagram

An outline block diagram of this LSI is shown below.

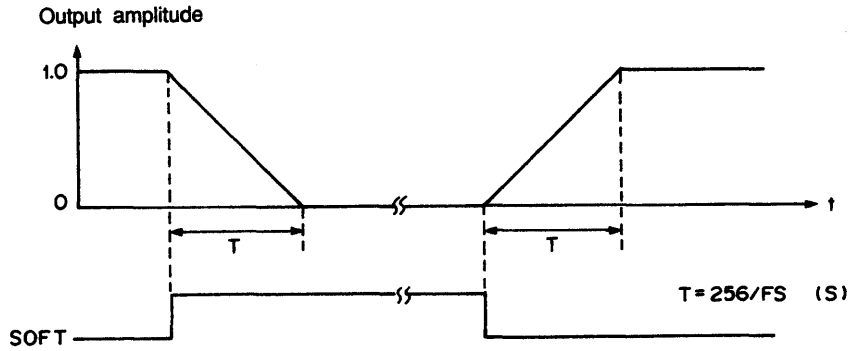


1. Noise shaping

For respective outputs FIR 1 to 3, IIR, SOFT/ATT figures are usually rounded off. However, by turning NS to "H" noise shaping can be applied.
NS register is cleared when INIT is at "L" or NS at "L".

2. Soft muting

By turning SOFT to "H"/"L", data can be smoothly muted or demuted.



3. Digital attenuator

Can attenuate output data by means of transfer data from an external microcomputer.

1) Command and Audio output
Attenuate data is in 12 bit and can be set in 1024 steps.
The relationship between command and output is shown in the chart below.

Attenuate data	Audio output
400 (H)	0 dB
3FF (H)	-0.0085 dB
3FE (H)	-0.017 dB
⋮	⋮
001 (H)	-60.206 dB
000 (H)	-∞

The attenuate value from 001 (H) to 3FF (H) can be obtained through the following formula.

$$ATT=20\log\left[\frac{\text{Input data}}{1024}\right]\ dB$$

Example: Attenuate data for 3FA (H)

$$ATT=20\log\left[\frac{1018}{1024}\right]\ dB=-0.051\ dB$$

2) Attenuator operation
Suppose that there are pieces of attenuator data ATT1, ATT2 and ATT3 and that ATT1>ATT3> ATT2 and that the place of attenuator data ATT1 is transferred first and ATT2 transferred next. If ATT2 is transferred before. The value of ATT2 is reached (during the state of A in Fig.1),the attenuation directly approaches the value of ATT2. If ATT3 is transferred before the value of ATT2 is reached (during the state of B or C in Fig.1), the attenuation is carried on from the value at the time (B or C) to approach the value of ATT3. Transition from one piece of attenuator data to another is the same as in the case of softmuting.

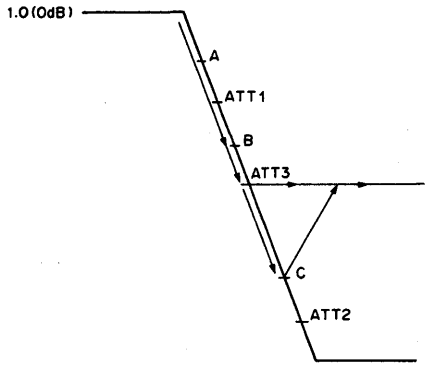
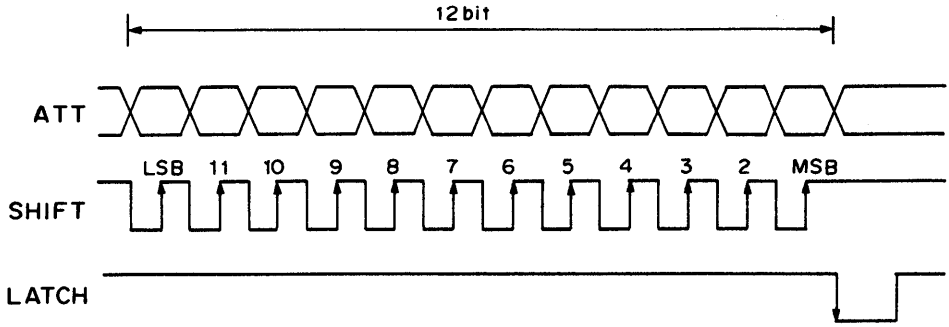
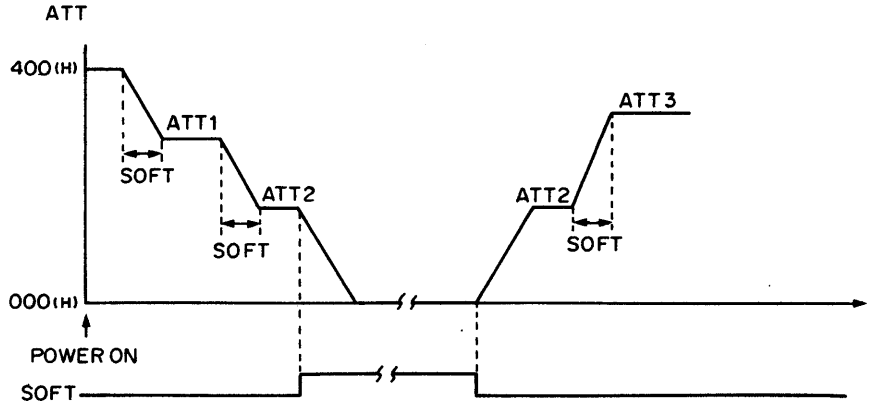


Fig.1 Transition from one attenuator value to another

3) Input data timing
Attenuate function can be activated by means of ATT, Shift and Latch.
Transfer format is indicated as follows.



(1) ATT data is a 12 bit word length and LSB first transfer ATT data is available 000(H) to 400(H).
(2) When Latch is at "L", ATT cannot be transferred.
(3) With INIT at ∫, 400 (H) is set as ATT data.



- The transition from ATT1 to ATT2 takes place in soft muting operation.
- During attenuate operation SOFT is set to either ON or OFF, it turns back to the original ATT data.
- When ATT data =400 (H) Noise shaping is not applied regardless of NS ON or OFF.
  When ATT data =400 (H) Noise shaping is applied regardless of NS ON or OFF.

4. Digital deemphasis
By turning EMP to "H", deemphasis can be applied by means of IIR filter.
Time constant of de-emphasis are τ_1=50μs and τ_2=15μs at f_s=44.1kHz.

5. Offset

Offset can be applied to the output data by means of OFST and OPOL.
Pos/Neg selection of the offset value is possible as indicated in the following chart.

OFST	OPOL	OUT $\overline{16}$/18	Offset value
L	X	L	0000 (H)
L	X	H	00000 (H)
H	H	L	02AA (H)
H	H	H	02AA8 (H)
H	L	L	FD55 (H)
H	L	H	FD554 (H)

6. Muting

By turning MUTE to "H" or INIT to "L", the output can be muted. Then, the offset value set at the offset is output. When INIT is at "L", 0 data is input to this LSI.

7. Data polarity

Inversion and non inversion of the output data can be selected by means of DPOL.
When DPOL is at "H", non inversion.
when DPOL is at "L", inversion.

8. I/O synchronizing circuit

1) Principle

A window featuring 10 internal system clocks (XIN/2) is set. The sync circuit observes whether the rising edge (LRCK$\int$) of LRCK that is input, has entered the window or not. When the power supply is turned on, should LRCK$\int$ be out of the window the sync circuit stops the internal processing in timing with the center of the window. Synchronously with the appearance of the next LRCK$\int$ the processing is started. Through this operation synchronization between the exterior system and this LSI is established.

2) Resynchronization by means of INIT

Even when LRCK$\int$ is inside the window but located close to one of the 2 edges of the window, the sync may miss with the mingling of external noise or other Re sync operation. To this effect it is necessary to apply resync, without fault, after supply is turned on. ReSync operation is executed with the INIT$\int$ timing. Sync. circuit is initialized and LRCK is located in the center of the window.
Moreover, when the sync falls out of the window, INAF output turns to "H" level.

3) Non synchronous MUTE

When INAF is at H, 0 data is output regardless of offset ON/OFF.

9. Output format

The output format of this LSI can be selected as shown in the chart below.

	8Fs		4Fs
	SONY	I²S	I²S
(Control pin)			
$\overline{\text{SONY}}$/I2S	'L'	'H'	←
LEFS	no effect	'L'	'H'
OUT$\overline{16}$/18	At will	no effect	←
(Output pin)			
LRCKO	8LRCK	4LRCK	←
BCKO	24BCK	16BCK	←
DATAL	DATAL	Staggered	MIX data
DATAR	DATAR	DATA	'L'
APT/WS	APT	WS	←
LE/$\overline{\text{WS}}$	LE	$\overline{\text{WS}}$	←

10. I/O signal latch timing

1) Input

DPOL, SOFT, MUTE, OFST, OPOL, INIT, $\overline{\text{SONY}}$/I²S, LFS, OUT$\overline{16}$/18, NS, EMP

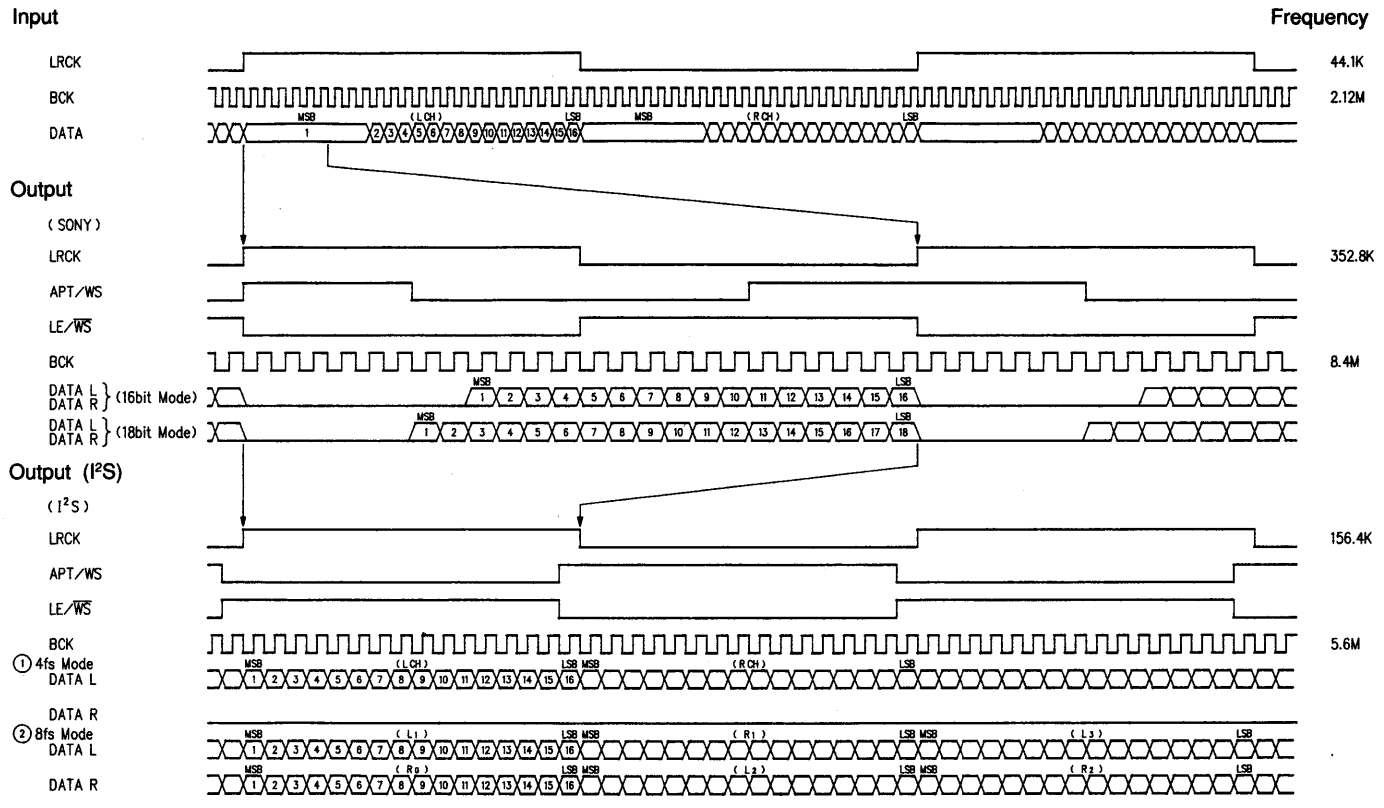
The above indicated input signals are latched by means of internal clocks equivalent to LRCK.

2) Output

LRCKO, DATAL, DATAR, APT.WS, LE/$\overline{\text{WS}}$

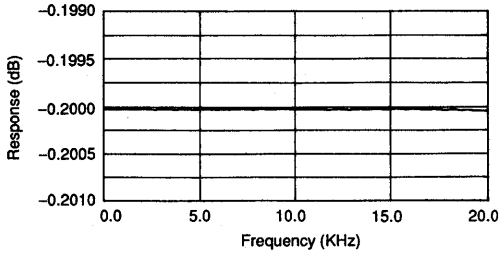
The above indicated output signals are latched by means of internal clocks equivalent to BCKO.

I/O Timing Chart

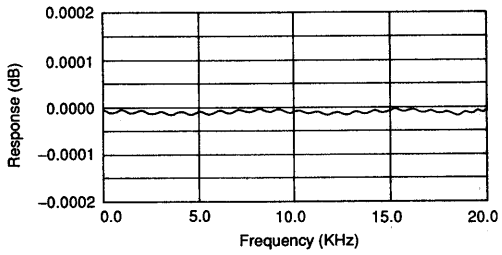


Filter characteristics (for 4Fs)

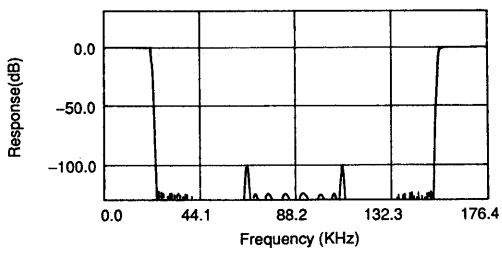
Frequency characteristics



Ripple characteristics

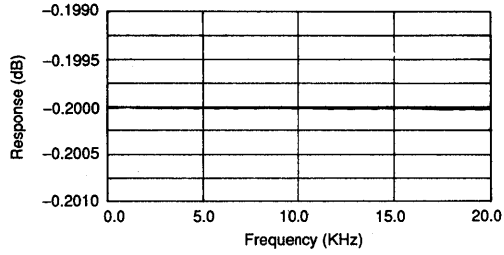


Attenuate

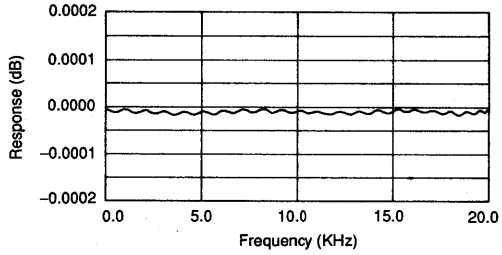


Filter characteristics (for 8Fs)

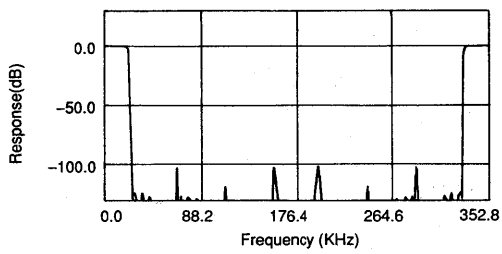
Frequency characteristics



Ripple characteristics



Attenuate



Over Sampling Digital Filter LSI

Description

CXD2550P is a digital filter LSI with 4-times/8-times over sampling rate, developed for compact disc player.

Features

- Provide a 4-times/8-times sampling digital filter.
- Filter characteristics
  ripple within 0.05dB
  attenuation below −40dB
- De-emphasis function
- Attenuate function (Built-in 1st noise shaping)
- I/O Format
  Input: 2's complement MSB first (serial)
  Output: 2's complement MSB first (serial)
  (16 bit slot, 18 bit slot selection possible)

Application

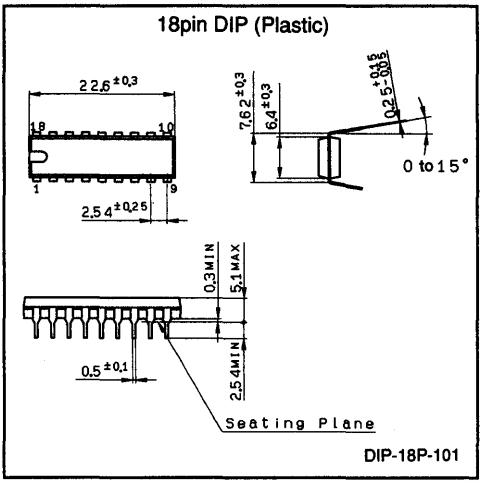
Compact disc player

Structure

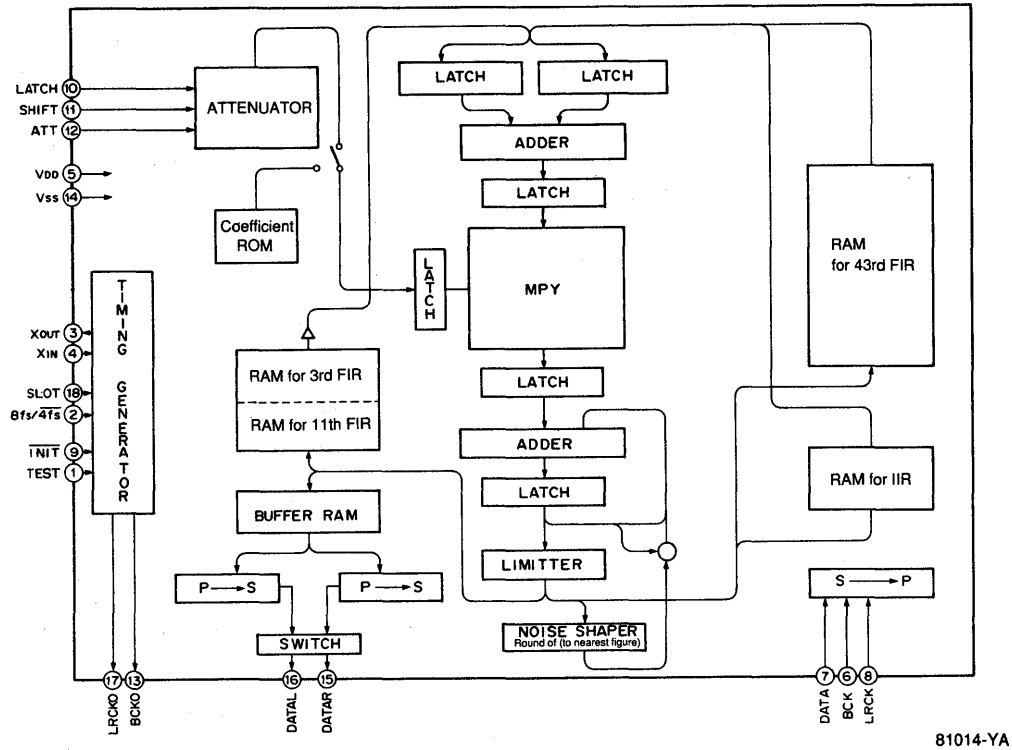
Silicon gate CMOS IC

Package Outline

Unit: mm



Block Diagram



81014-YA

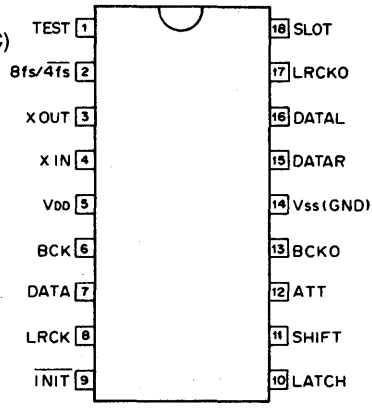
Absolute Maximun Ratings (Ta= −20 to +75°C)

• Supply voltage	V_{DD}	−0.5 to +6.5	V	
• Input voltage	V_I	−0.5 to V_{DD} +0.5	V	
• Storage temperature	Tstg	−55 to +150	°C	
• Allowable power dissipation	P_D	500	mW	(Ta=75°C)

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5	V	
• Operating temperature	Topr	−20 to +75	°C	
• OSC frequency	fx	10 to 20	MHz	(duty 50 ±10%)

Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description
1	TEST	I	Test pin. For normal usage, fixed to 'L'
2	8fs/$\overline{4fs}$	I	FIR 3 selection, at 'H' 8fs at 'L' 4fs
3	X OUT	O	Master clock output (f=384fs)
4	X IN	I	Master clock input (f=384fs)
5	V_{DD}	—	+ Supply (5V)
6	BCK	I	BCK input
7	DATA	I	Serial data input (2's complement)
8	LRCK	I	LRCK input
9	$\overline{INIT}$	I	Resync with the rise of this signal
10	LATCH	I	Latch CLK input
11	SHIFT	I	Shift CLK input
12	ATT	I	Attenuate data input
13	BCKO	O	BCK output
14	V_{SS} (GND)	—	- Supply (0V)
15	DATAR	O	At 4fs: WCK output At 8fs: RCH serial data output (2's complement)
16	DATAL	O	At 4fs: LCH, RCH Time-shared serial data output (2's complement) At 8fs: LCH serial data output (2's complement)
17	LRCKO	O	LRCK output
18	SLOT	I	Output slot selection at 'H' 18 bit slot at 'L' 16 bit slot

***Note)** TEST, 8fs/$\overline{4fs}$, SLOT pins: Pull down

Electrical characteristics

DC characteristics

V_{DD}=4.5 to 5.5 V, Ta=−20 to +75°C

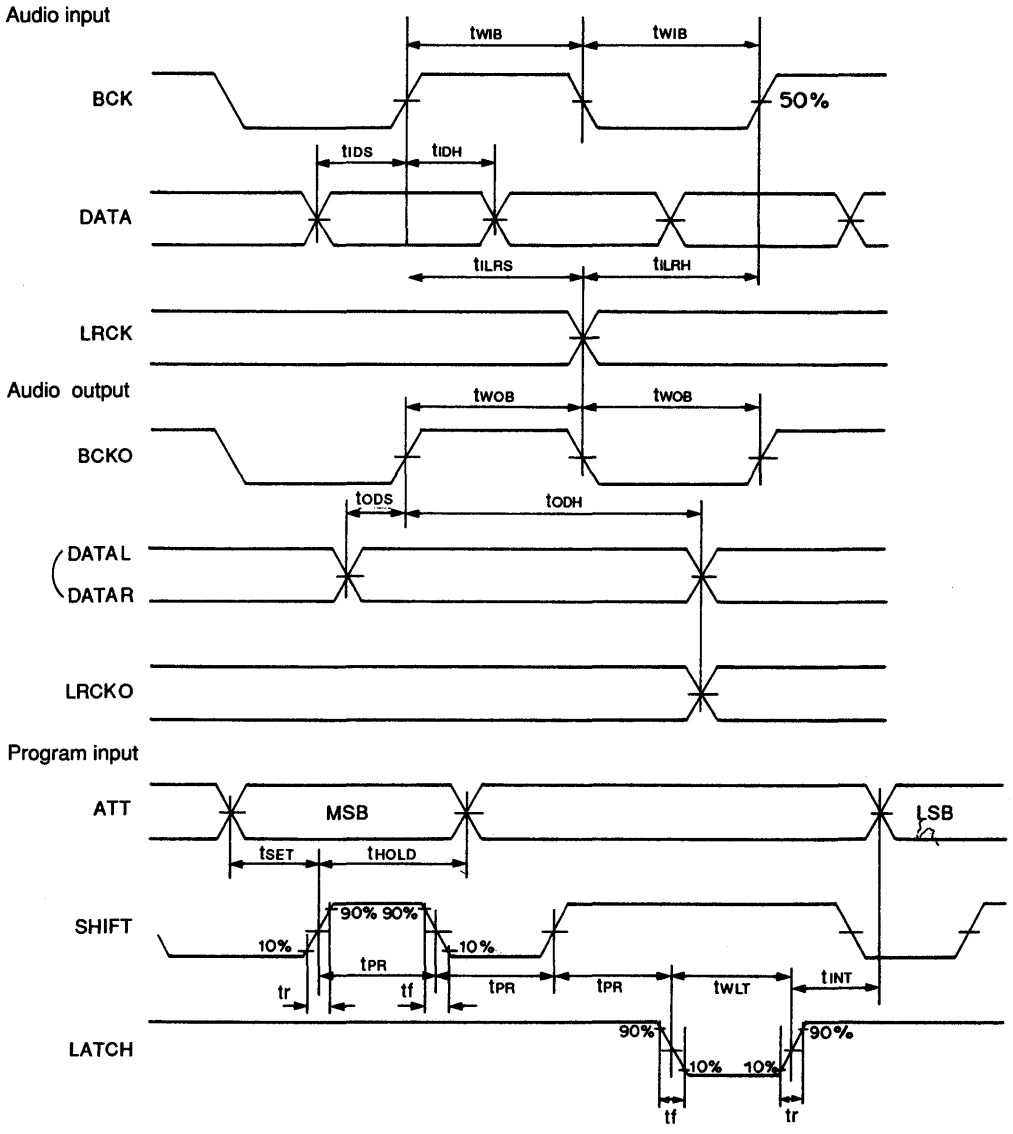
No.	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
All inputs except 4 XIN	Input capacitance	C_{IN}	———	—	3	5	pF
1, 2, 6, 7, 8, 9, 10, 11, 12, 18	'H' input voltage	V_{IN}	———	0.76V_{DD}	—	—	V
	'L' input voltage	V_{IL}	———	—	—	0.24V_{DD}	
6, 7, 8, 9, 10, 11, 12	Input leak current 1	I_{ILK1}	V_I=V_{DD}/0V	−5	—	5	μA
1, 2, 18	Pull down resistance	R_{PD}	———	7.5	15	30	KΩ
	'L' input leak current	I_{IL}	V_I=0V	—	—	5	μA
4	Input leak current 2	I_{ILK2}	V_I=V_{DD}/0V	−20	—	20	
13, 15, 16 ,17	'H' output voltage	V_{OH}	I_D=−4mA	V_{DD}-0.5	—	—	V
	'L' output voltage	V_{OL}	I_D=4mA	—	—	0.4	
	Consumption current	I_{DD}	No load V_I=V_{DD}/0V fx=16.9344MHz	—	—	40	mA

AC characteristics

V_{DD}=4.5 to 5.5 V, Ta=−20 to +75°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency	fx	———	10	16.9344	20	MHz
Input BCK frequency	f_{BCK}		—	—	4.0	
Input BCK pulse width	t_{WIB}	———	100	—	—	ns
Input data set up time	t_{IDS}	———	20	—	—	
Input data hold time	t_{IDH}	———	20	—	—	
Input LRCK set up time	t_{ILRS}	———	50	—	—	
Input LRCK hold time	t_{ILRH}	———	50	—	—	
Output BCKO pulse width	t_{WOB}	8fs	40	—	—	
Output data set up time	t_{ODS}	fx=16.9344MHz	25	—	—	
Output data hold time	t_{ODH}	Cl=50pF	25	—	—	
Program input base time	t_{PR}	fx=16.9344MHz	250	—	—	
Latch input pulse width	t_{WLT}		500	—	—	
Rise time (SHIFT, LATCH)	tr		—	—	200	ns
Fall time (SHIFT, LATCH)	tf		—	—	200	
Set up time (ATT)	t_{SET}	———	500	—	—	
Hold time (ATT)	t_{HOLD}		500	—	—	
Interval (ATT)	t_{INT}		1000	—	—	

Timing Chart



Functions

1. Soft muting

The soft mute function mutes or demutes output data on the basis of a muting time of 1024/fs (fs=44.1kHz on CD).

2. Digital attenuator

The data trasferred from an external attenuator may be used to attenuate the output data. The ATT data comprises 8 bits. The D7 is the digital de-emphasis control bit, whereas the D6 through D0 constitute attenuator data.

1) Command and audio output

The attenuator data is in 7 bits, allowing selection of 127 different settings. The relation between a command and output is shown in the following table.

Attenuator data D_6 to D_0	Audio output
7F(H)	0 dB
7E(H) | 01(H)	-0.13 dB | -42.144 dB
00(H)	-∞

An attenuator value between 01(H) and 7E(H) can be given by the following equation.

$$ATT=20 \log \left[\frac{\text{Input data}}{128}\right] dB$$

Example)Suppose that the attenuator data is 7A.

$$ATT=20 \log \left[\frac{122}{128}\right] dB=-0.417dB$$

3. I/O synchronizing circuit

1) Theory of operation

The synchronizing cuircuit opens a window for six internal system clocks, CK2(fx/4) to monitor whether the differentiated signal of the rise of LRCK (LRCK ƒ) that may be input exists in it. If the LRCK is out of the window when the power supply is turned on, the synchronizing circuit holds the CK2 at the time it is in the center of the window, and lets it start as soon as the next LRCK ƒ arrives. This operation synchronizes an external system and this IC and lines up the phases of serial input data.

2) Resynchronization by INIT

If the LRCK ƒ is in the window when the power supply is turned ON, a fluctuation of LRCK could cause desynchronization during operation of the IC (particularly when it is either end of the window).

For this reason, resynchronization must always be achieved after the power supply has been turned ON. The operation for resynchronization is performed at the time the INIT rises. The operation initializes the synchronizing circuit to cause a temporary desynchronization and then achieves resynchronization, there by positioning the LRCK ƒ in the center of the window.

4. Attenuator operation

Suppose that there are pieces of attenuator data ATT1, ATT2 and ATT3 and that ATT1> ATT3> ATT2 and that the piece of attenuator data ATT1 is transferred first and ATT2 transferred next. If ATT2 is transferred before the value of ATT1 is reached (during the state of A in Fig.1), the attenuation directly approaches the value of ATT2. If ATT3 is transferred before the value of ATT2 is reached (during the state of B or C in Fig.1) ,the attenuation is carried on from the value at the time(B or C) to approach the value of ATT3. Transition from one piece of attenuator data to another is the same as in the case of soft muting.

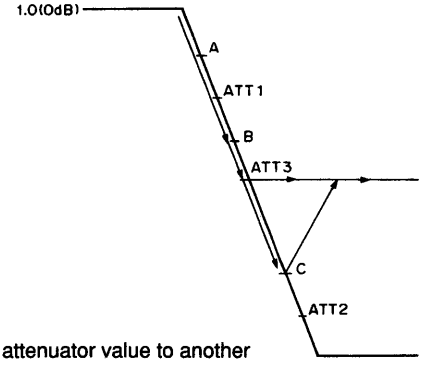


Fig.1 Transition from one attenuator value to another

5. Input data timing

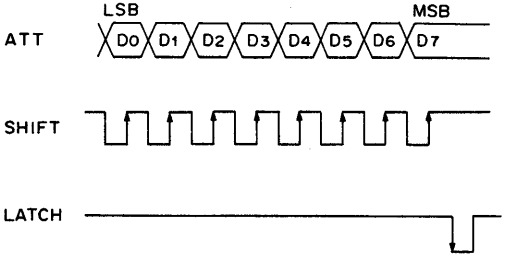


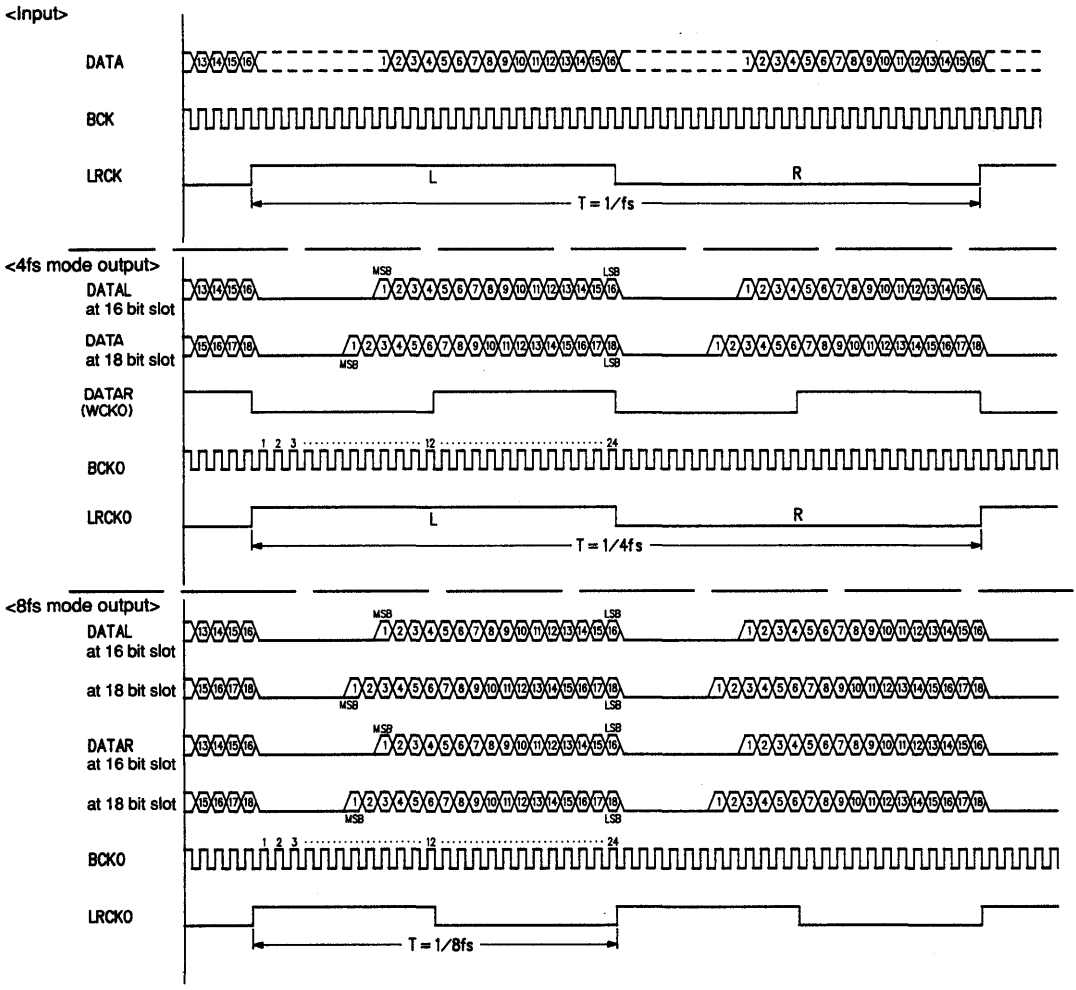
Fig.2 Timing of ATT, SHIFT and LATCH

1) The ATT data is LSB first.
2) About the ATT data
   D_7: Digital de-emphasis control bit
   H: De-emphasis ON
   L: De-emphasis OFF
   Note that the time constants of emphasis are $\tau1$=50μs and $\tau2$=15μs at fs=44.1kHz
   D_0 to D_6: Attenuator data

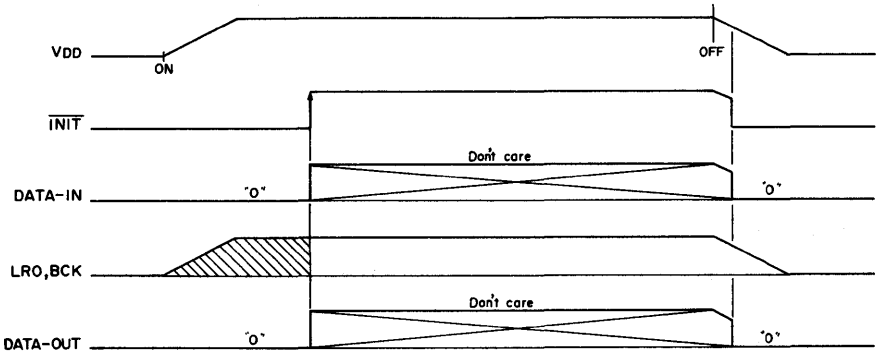
6. $\overline{\text{INIT}}$ pin

After $\overline{\text{INIT}}$↓, the counters and registers for the attenuators in the IC are reset to all 0s(muted state). After $\overline{\text{INIT}}$↓, therefore, a proper value(7F(H) (Full scale) for example) should be trasferred from the microcomputer to the ATT pins.

I/O Timing


<Input>
DATA
BCK
LRCK
L
R
T = 1/fs
<4fs mode output>
DATAL
at 16 bit slot
DATA
at 18 bit slot
DATAR
(WCKO)
BCKO
LRCKO
MSB
LSB
T = 1/4fs
<8fs mode output>
DATAL
at 16 bit slot
at 18 bit slot
DATAR
at 16 bit slot
at 18 bit slot
T = 1/8fs

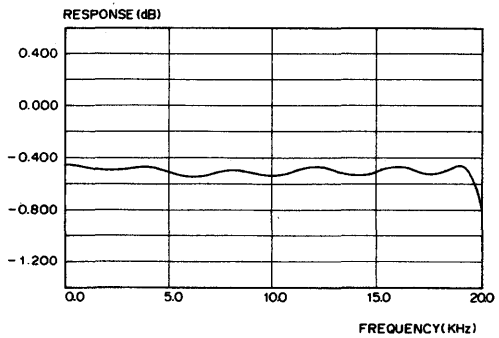
Operation at power ON/OFF



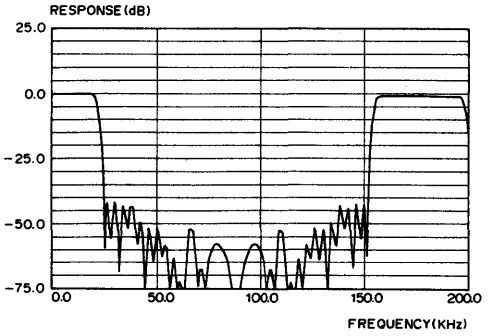
Filter Characteristics

Quadrupled over sampling mode

Frequency characteristics 1(Pass band)

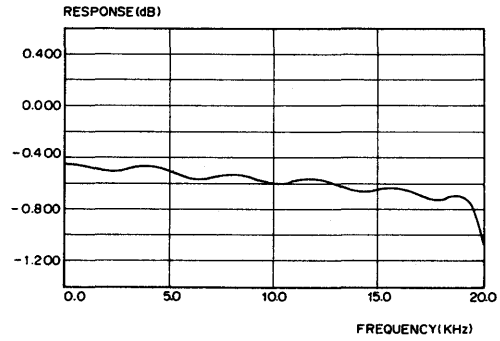


Frequency characteristics 2(Stop band)

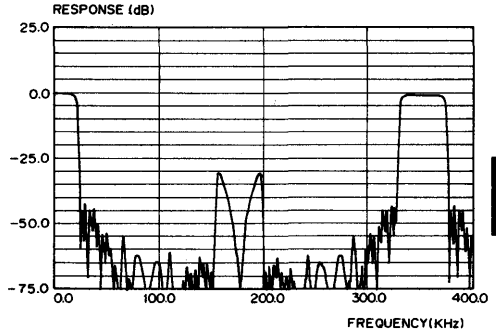


Octupled over sampling mode

Filter characteristics 1(Pass band)



Filter characteristics 2(Stop band)

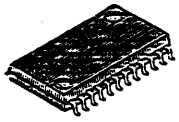


SONY®

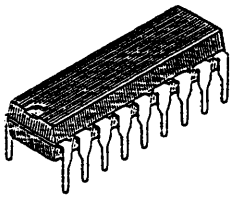
CXD2551M/P

Over Sampling Digital Filter LSI

CXD2551M 24 pin SOP (Plastic)



CXD2551P 18 pin DIP (Plastic)



Description

The CXD2551M/P is a 4- and 8-times oversampling digital filter LSI for a compact disc player.

Features

- A 4- and 8-times digital filter
- Filter characteristics
  Ripple: ±0.05 dB or less
  Attenuation: −40 dB or less
- De-emphasis function
- Attenuating function (Built-in 1st noise shaper)
- Digital offset function
- I/O format
  Input: 2's complement MSB first (serial)
  Output: 2's complement MSB first (serial)
  (16- or 18-bit slot selectable)

Applications

Compact disc player

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (Ta = −20 to +75°C)

• Supply voltage	V_{DD}	−0.5	to	+6.5	V	
• Input voltage	V_I	−0.5	to	V_{DD} +0.5	V	
• Allowable power dissipation	P_D		500		mW	(Ta = 75°C)
• Storage temperature	Tstg	−55	to	+150	°C	

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5	to	5.5	V	
• Operating temperature	Topr	−20	to	+75	°C	
• OSC frequency	fx	10	to	20	MHz	(Duty 50 ±10%)

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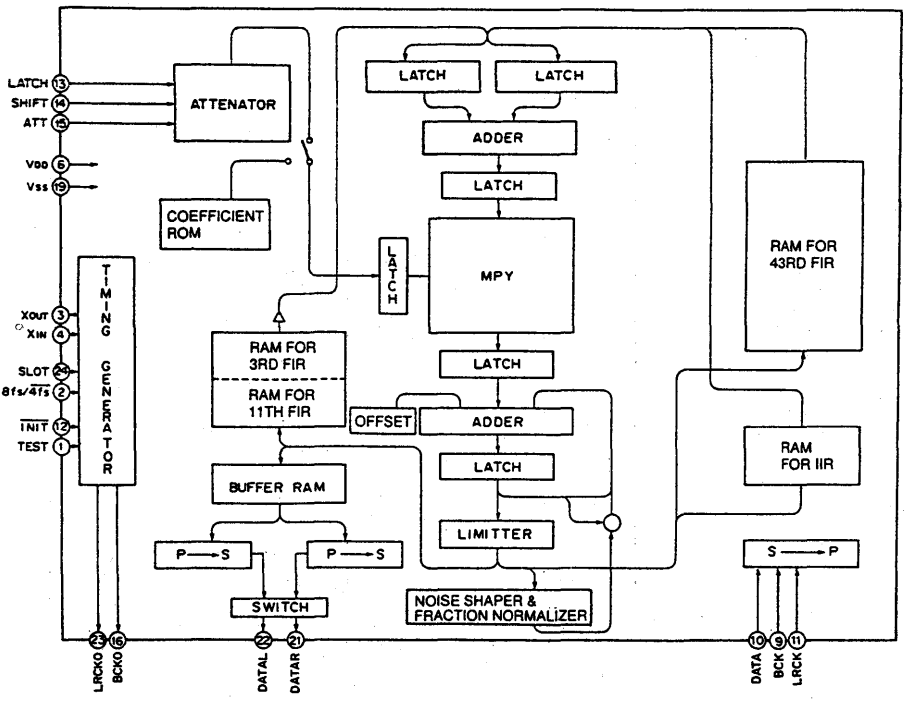
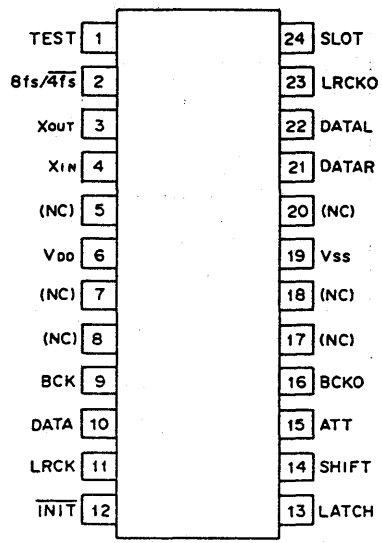
CXD2551M

Block Diagram

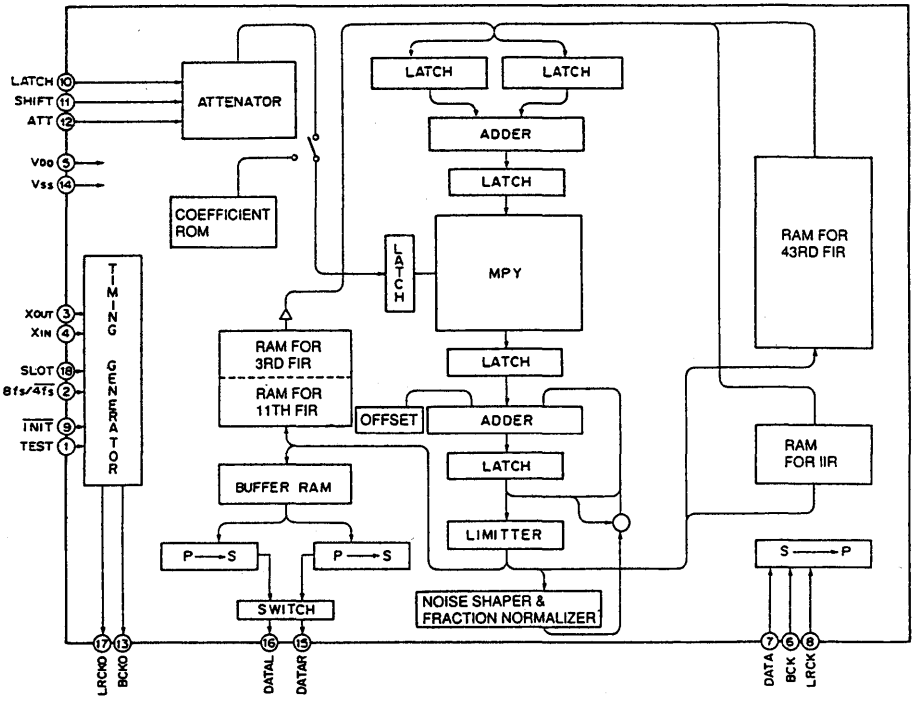


Pin Configuration

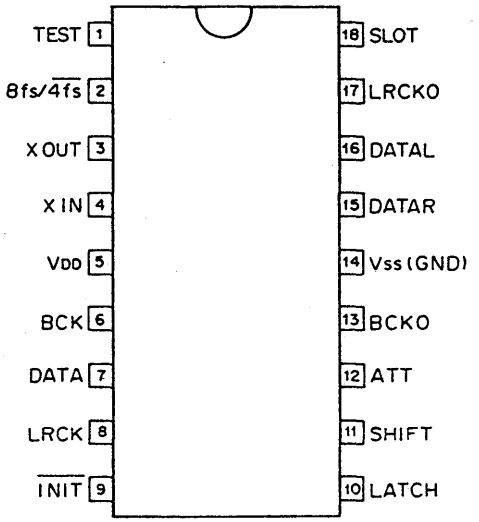


CXD2551P

Block Diagram



Pin Configuration



Pin Description

Pin No.		Symbol	I/O	Description
CXD2551P	CXD2551M			
1	1	TEST	I	Test pin. Fixed at 'L' level in normal operation mode.
2	2	8fs /$\overline{4fs}$	I	To specify FIR 3. 'H': 8fs 'L': 4fs
3	3	XOUT	O	Master clock output (f = 384fs)
4	4	XIN	I	Master clock input (f = 384fs)
5	6	V_{DD}	–	Power supply (+5 V)
6	9	BCK	I	BCK input
7	10	DATA	I	Serial data input (2's complement)
8	11	LRCK	I	LRCK input
9	12	$\overline{INIT}$	I	Re-synchronized by rising edge of this signal
10	13	LATCH	I	Latch clock input
11	14	SHIFT	I	Shift clock input
12	15	ATT	I	Attenuate data input
13	16	BCKO	O	BCK output
14	19	V_{SS} (GND)	–	Power supply (0 v)
15	21	DATAR	O	4fs mode: WCK output 8fs mode: RCH serial data output (2's complement)
16	22	DATAL	O	4fs mode: LCH and RCH time division serial data output (2's complement) 8fs mode: LCH serial data output (2's complement)
17	23	LRCKO	O	LRCK output
18	24	SLOT	I	To specify output slot. 'H': 18-bit slot 'L': 16-bit slot
–	5, 7, 8, 17, 18, 20	(NC)	–	No connection

* TEST, 8fs /$\overline{4fs}$ and SLOT pins: Pull down resistance

Electrical Characteristics

DC characteristics (V_{DD} = 4.5 to 5.5 V, Ta = −20 to +75°C)

Pin	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
All inputs except XIN	Input capacitance	C_{IN}	——	–	3	5	pF
Note 1	"H" input voltage	V_{IH}	——	0.76 V_{DD}	–	–	V
	"L" input voltage	V_{IL}	——	–	–	0.24 V_{DD}	
Note 2	Input leak current 1	I_{ILK1}	V_I = V_{DD}/0V	–	–	±5	µA
TEST, 8fs /$\overline{4fs}$, SLOT	Pull down resistance	R_{PD}	——	7.5	15	30	kΩ
	"L" input leak current	I_{IL}	V_I = 0V	–	–	5	µA
XIN	Input leak current 2	I_{ILK2}	V_I = V_{DD}/0V	–	–	±20	
BCKO, DATAR, DATAL, LRCKO	"H" output voltage	V_{OH}	I_D = −4 mA	V_{DD}-0.5	–	–	V
	"L" output voltage	V_{OL}	I_D = 4 mA	–	–	0.4	
	Consumption current	I_{DD}	When no load is placed V_I = V_{DD}/0V fx = 16.9344 MHz	–	–	40	mA

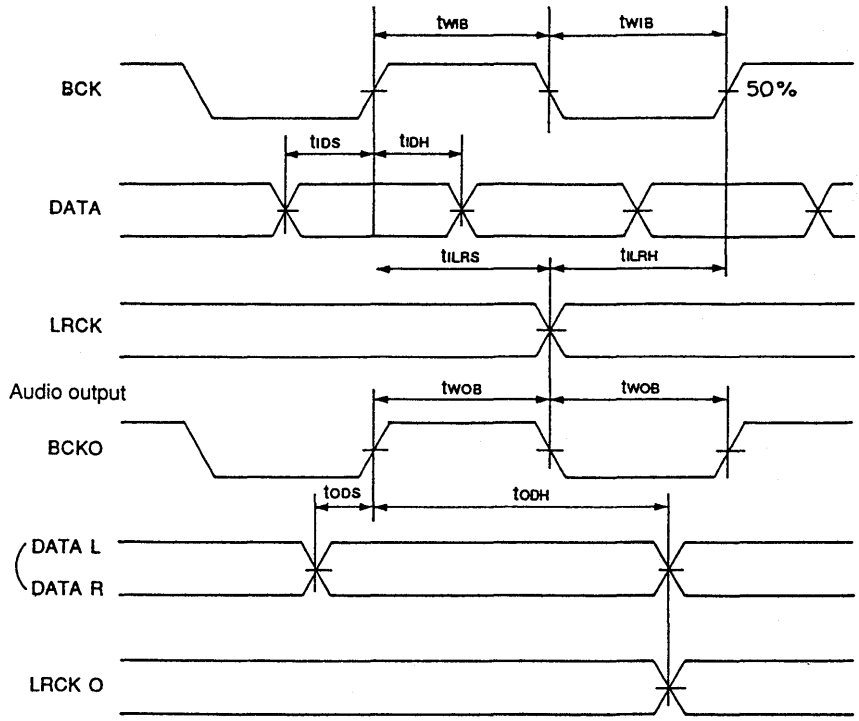
Note 1) TEST, 8fs /$\overline{4fs}$, BCK, DATA, LRCK, $\overline{INIT}$, LATCH, SHIFT, ATT, SLOT
Note 2) BCK, DATA, LRCK, $\overline{INIT}$, LATCH, SHIFT, ATT

AC characteristics (V_{DD} = 4.5 to 5.5 V, Ta = −20 to +75°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency	fx	——	10	16.9344	20	MHz
Input BCK frequency	f_{BCK}		–	–	4.0	
Input BCK pulse width	t_{WIB}	——	100	–	–	ns
Input data set-up time	t_{IDS}	——	20	–	–	
Input data hold time	t_{IDH}	——	20	–	–	
Input LRCK set-up time	t_{ILRS}	——	50	–	–	
Input LRCK hold time	t_{ILRH}	——	50	–	–	
Output BCKO pulse width	t_{WOB}	8fs	40	–	–	
Output data set-up time	t_{ODS}	fx = 16.9344 MHz	25	–	–	
Output data hold time	t_{ODH}	C1 = 50 pF	25	–	–	
Program input base time	t_{PR}	fx = 16.9344 MHz	250	–	–	
Latch input pulse width	t_{WLT}		500	–	–	
Rise time (SHIFT, LATCH)	tr	——	–	–	200	ns
Fall time (SHIFT, LATCH)	tr		–	–	200	
Set-up time (ATT)	t_{SET}		500	–	–	
Hold time (ATT)	t_{HOLD}		500	–	–	
Interval	t_{INT}		1000	–	–	

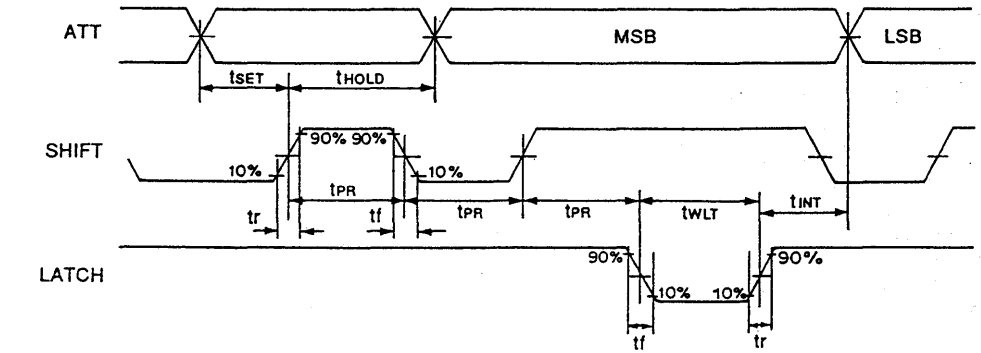
Timing Chart

Audio input



Audio output

Program input



Description of Functions (Description E,F and G are different from those for CXD2550P.)

A. Soft muting

The soft mute function mutes or demutes output data on the basis of a muting time of 1024/fs (CD: fs = 44.1 kHz).

B. Digital attenuator

Output data can be attenuated by use of data transferred from an external micro computer. The ATT data comprises 8 bits. Bit D_7 is the digital de-emphasis control bit, whereas bits D_6 through D_0 constitute attenuator data.

(1) Command input and audio output

The attenuator data is in 7 bits, allowing selection of 127 different settings. The relation between a command and output is shown in the following table.

Attenuator data D_6 to D_0	Audio output
$7F_{(H)}$	0 dB
$7E_{(H)}$ to $01_{(H)}$	-0.13 dB to -42.144dB
$00_{(H)}$	$-\infty$

An attenuator value between $01_{(H)}$ and $7E_{(H)}$ can be calculated by the following equation.

$$ATT = 20 \log \left(\frac{\text{Input data}}{128} \right) dB$$

Example) Suppose that attenuator data is 7A.

$$ATT = 20 \log \left(\frac{122}{128} \right) dB = -0.417 \text{ dB}$$

C. I/O synchronizing circuit

1) Theory of operation

The synchronizing circuit opens a window for six internal system clocks, CK2 (fx/4), to monitor whether the differentiated signal of the rise of LRCK (LRCK f) that may be input exists in it. If the LRCK f is out of the window when the power supply is turned on, the synchronizing circuit holds the CK2 at the time it is in the center of the window, and lets it start as soon as the next LRCK f arrives. This operation synchronizes an external system and this IC, and lines up the phases of serial input data.

2) Re-synchronization by $\overline{\text{INIT}}$

If the LRCK f is in the window when the power supply is turned on, a fluctuation of LRCK could cause de-synchronization during operation of the IC (particularly when it is at either end of the window).

For this reason, re-synchronization must always be achieved after the power supply has been turned on. The operation for re-synchronization is performed at the time the $\overline{\text{INIT}}$ rises. The operation initializes the synchronizing circuit to cause a temporary de-synchronization and then achieves re-synchronization, thereby positioning the LRCK f in the center of the window.

D. Attenuator operation

Suppose that there are three pieces of attenuator data, ATT1, ATT2 and ATT3 and that their relations are ATT1>ATT3>ATT2. Assume that ATT1 is transferred first, followed by ATT2.
If ATT2 is transferred before the value of ATT1 is reached (during the state of A in Fig. 1), the attenuation directly approaches the value of ATT2. If ATT3 is transferred before the value of ATT2 is reached (during the state of B or C in Fig. 1), the attenuation is carried on from the value at the time (B or C) to approach the value of ATT3. Transition from one piece of attenuator data to another is the same as in the case of soft muting.

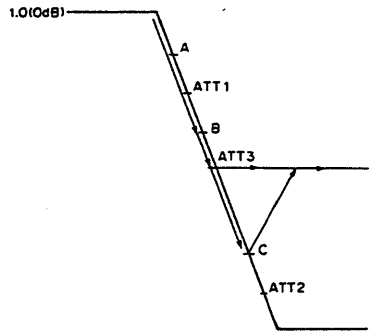


Fig. 1 Transition from one attenuator value to another

E. Input data timing

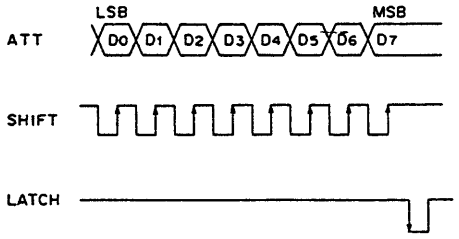


Fig. 2 Timing of ATT, SHIFT and LATCH

① ATT data is configured on the LSB first basis.
② ATT data
D_7 : Digital de-emphasis control bit
H: Emphasis ON
L: Emphasis OFF
Note that emphasis time constants are τ_1 = 50 µs and τ_2 = 15 µs at fs = 44.1 kHz.
D_0 to D_6: Attenuator data

F. About $\overline{\text{INIT}}$ pin is ∫

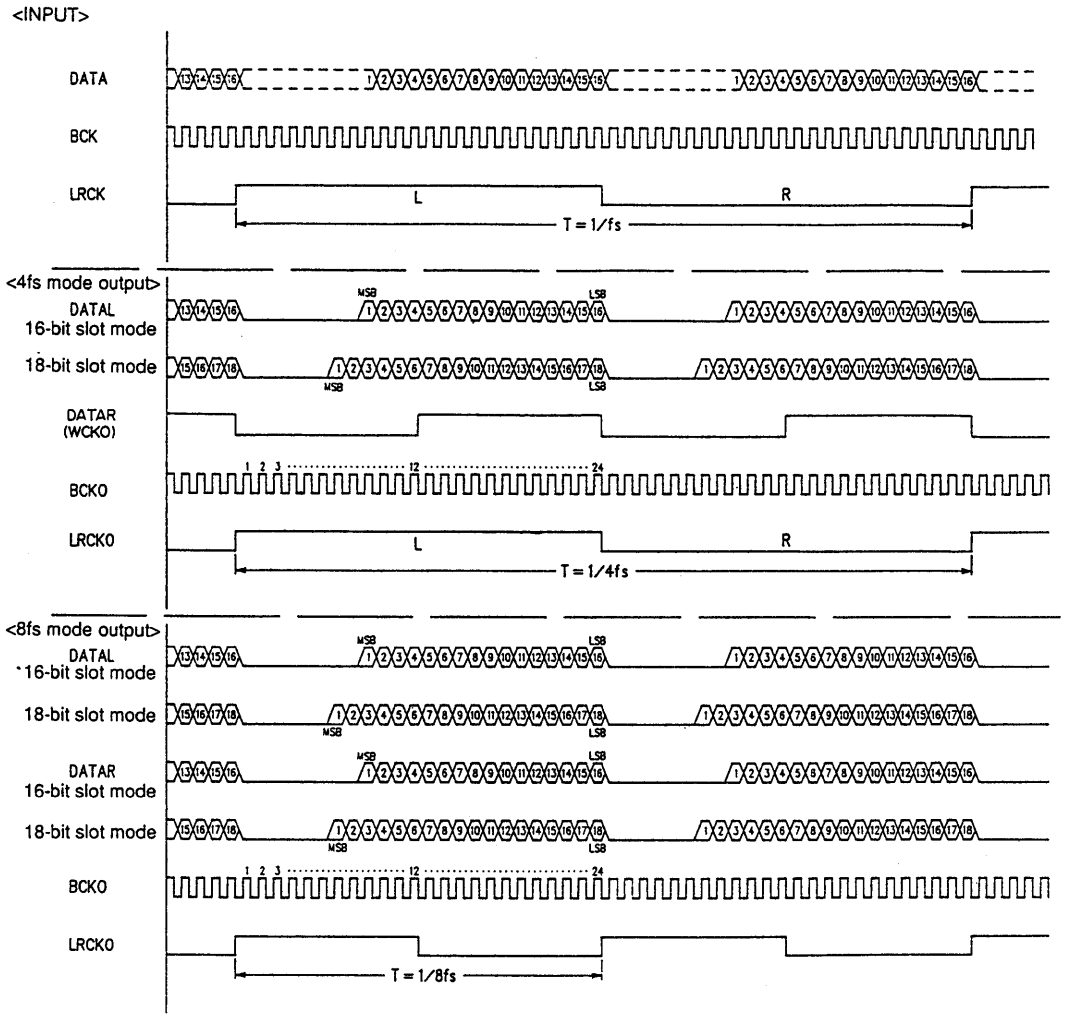
After $\overline{\text{INIT}}$ is ∫, the counters and registers for the attenuators in the IC are set at $7F_{(H)}$.

G. Digital offset

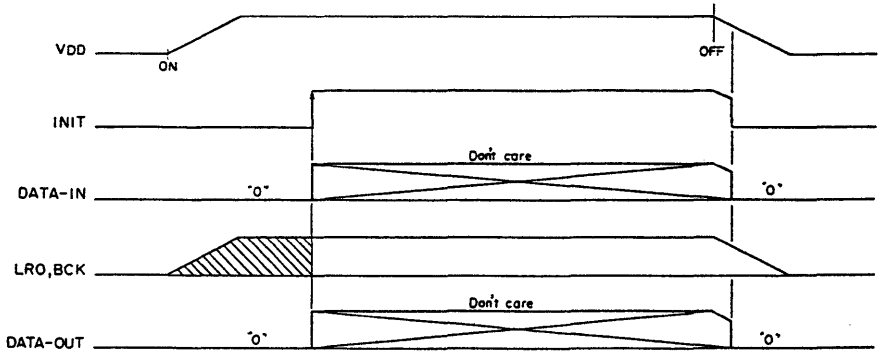
An offset value is added to the digital filter output. The value is $02AA_{(H)}$ in the 16-bit slot mode and $02AA0_{(H)}$ in the 18-bit slot mode.

In the muting mode, this offset value triggers muting.

I/O timing



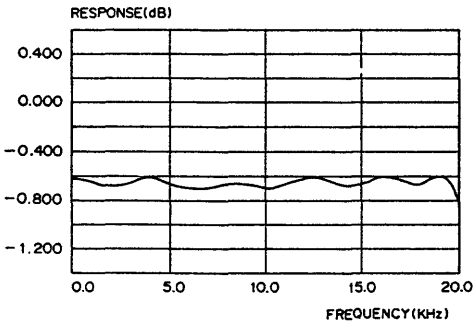
Operation in POWER ON/OFF state



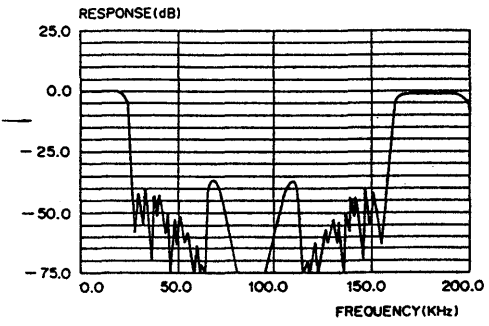
Filter Characteristics

Quadrupled oversampling mode

Frequency Characteristics 1 (Pass band)

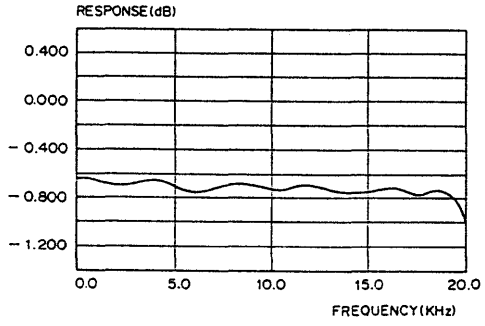


Frequency Characteristics 2 (Stop band)

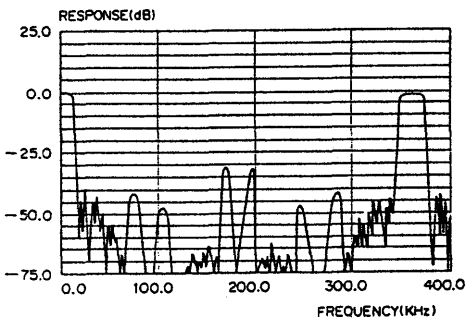


Octupled oversampling mode

Frequency Characteristics 1 (Pass band)

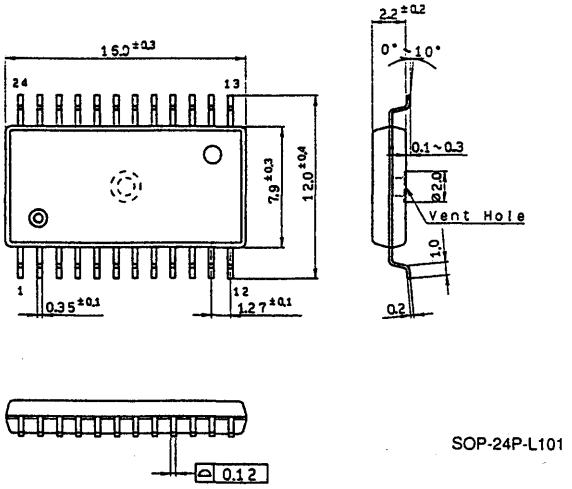


Frequency Characteristics 2 (Stop band)



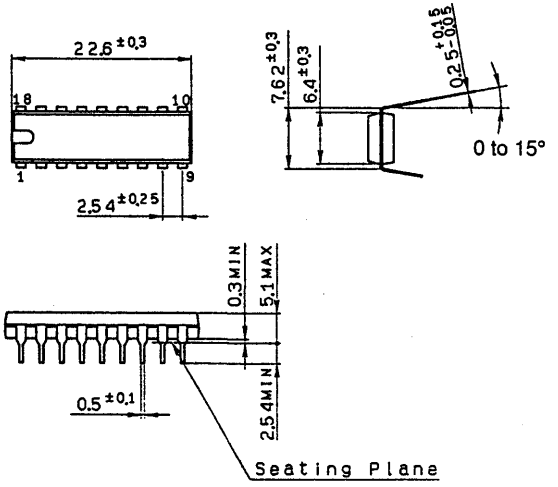
Package Outline Unit: mm

CXD2551M 24 pin SOP (Plastic) 450 mil



SOP-24P-L101

CXD2551P 18 pin DIP (Plastic) 300 mil



DIP-18P-101

Evaluation Printed Circuit Boards

8

6. Evaluation Printed Circuit Boards

High Speed Converters

Type	Function	Page
CX20116 }PCB CXA1066K	8-bit 110MSPS A/D Evaluation Board	443
CXA1016P/K }PCB CXA1056P/K	8-bit 50MSPS/30MSPS A/D Evaluation Board	450
CXA1076AK PCB CXA1176AK PCB	8-bit 200MSPS/300MSPS A/D Evaluation Board	459
CXA1096PPCB	8-bit 20MSPS TTL I/O A/D Evaluation Board	467
CXA1296PPCB	8-bit 20MSPS TTL I/O A/D Evaluation Board	475
CXD1172P/CXA1106P PCB	6-bit 20MSPS ADC and DAC Evaluation Board	482
CXD1172AP/CXA1106P PCB	6-bit 20MSPS ADC and DAC Evaluation Board	490
CXD1175P/CXA1106P PCB	8-bit 20MSPS ADC and DAC Evaluation Board	498
CXD1175AP/CXA1106P PCB	8-bit 20MSPS ADC and DAC Evaluation Board	506
FCX20220A-1/-2	10-bit/9-bit 20MHz Sub-ranging A/D Converter Evaluation Board	514

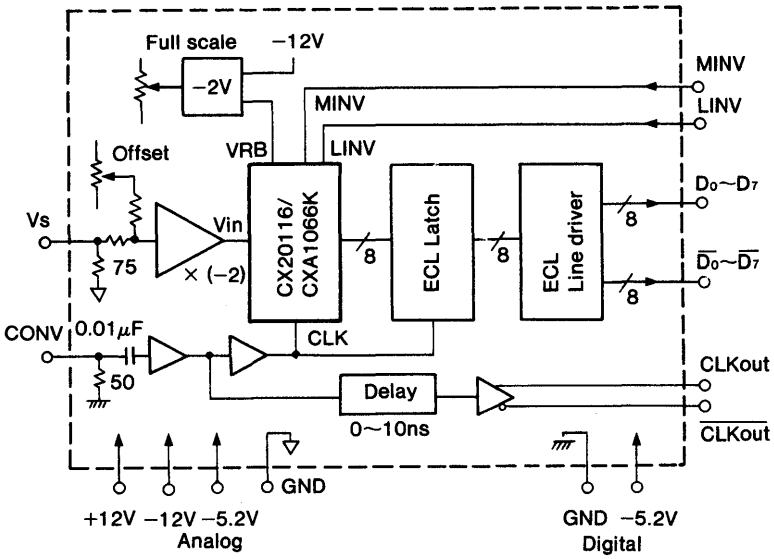
High Resolution Converters

Type	Function	Page
CX20018 PCB	CX20018 Evaluation Board	522
CX20152 PCB	CX20152 Evaluation Board	532

SONY CX20116PCB/CXA1066PCB

8bit, 110MHz A/D Evaluation Board

CX20116 PCB/CXA1066PCB is the evaluation printed circuit board for 8 bit high speed A/D converter CX20116/CXA1066K. On this one board, A/D, driver, standard voltage source, latches and ECL line drivers are mounted, and this PCB is designed to achieve the best performance of the A/D converter.



PCB Characteristics

- Analog Input Band Width 40 MHz (at −3 dB) (including A/D input driver)
- Analog Input Impedance 75Ω
- Complementary ECL Output
- Clock Output (Delay Time 0 ~ 10ns adjustable)

1. Supply Voltage

Item		Symbol	Min	Typ	Max	Unit
Analog	+12V				80	mA
	−12V				80	mA
	−5.2V				250	mA
Digital	−5.2V				460	mA

2. Analog Input (Vs)

Item	Symbol	Min	Typ	Max	Unit
AC Input Voltage Amplitude*			1	1.1	V
Offset Adjustable Range		−0.25	0	1	V
Input Impedance			75		Ω

* peak to peak

NE89637-HP

3. Convert Input Signal (CONV)

Item	Symbol	Min	Typ	Max	Unit
Input Voltage*		0.6		1.1	V
Input Impedance			50		Ω
DC Level		−3		3	V
Pulse Width	Tcw 1	7.5			ns
	Tcw 0	2.5			ns

* peak to peak

4. Control Input (MINV, LINV)

ECL 10K Compatible

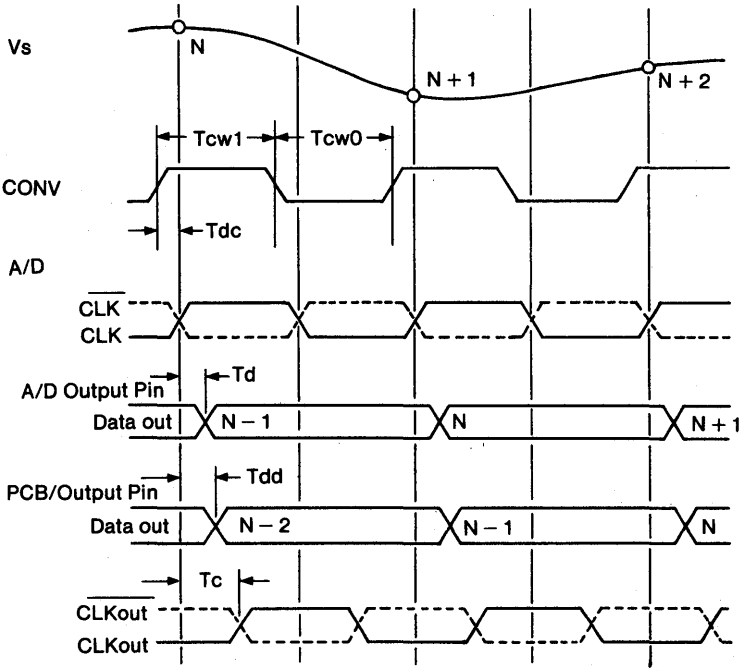
5. Digital Output (D_0~D_7, $\overline{D}_0$~$\overline{D}_7$)

ECL 10K Compatible, Complementary Output

6. Clock Output

ECL 10K Compatible, Complementary Output
Delay Time Adjustable

7. Timing Chart



Item	Symbol	Min	Typ	Max	Unit
Conversion Delay	Tdc		3.5		ns
Data Delay	Tdd		5.5		ns
Clock Delay Adjustable Range*	Tc	0		10	ns

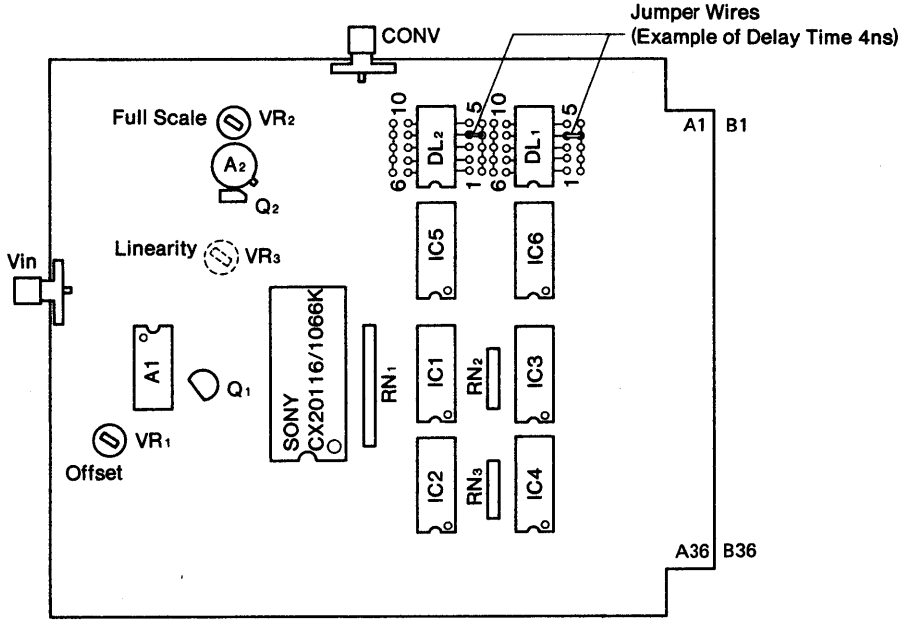
* Adjustable in 1ns step by taps

8. Output Coding

MINV LINV	0 0	0 1	1 0	1 1	
0V	111...11	100...00	011...11	000...00	1 : V_{IH}
.	111...10	100...01	011...10	000...01	0 : V_{IL}
.	.	.	.	.	
.	.	.	.	.	
.	.	.	.	.	
.	100...00	111...11	000...00	011...11	
.	011...11	000...00	111...11	100...00	
.	.	.	.	.	
.	.	.	.	.	
.	.	.	.	.	
.	000...01	011...10	100...01	111...10	
−2V	000...00	011...11	100...00	111...11	

9. Adjusting Method of Clock Output Delay Time

Clock output delay time can be adjusted by jumper wires position on the PCB.
Tap positions should be changed simultaneously in CLK and CLK, avoiding the effect of waveform distortion.
Delay time in each taps are 1ns.



10. Note

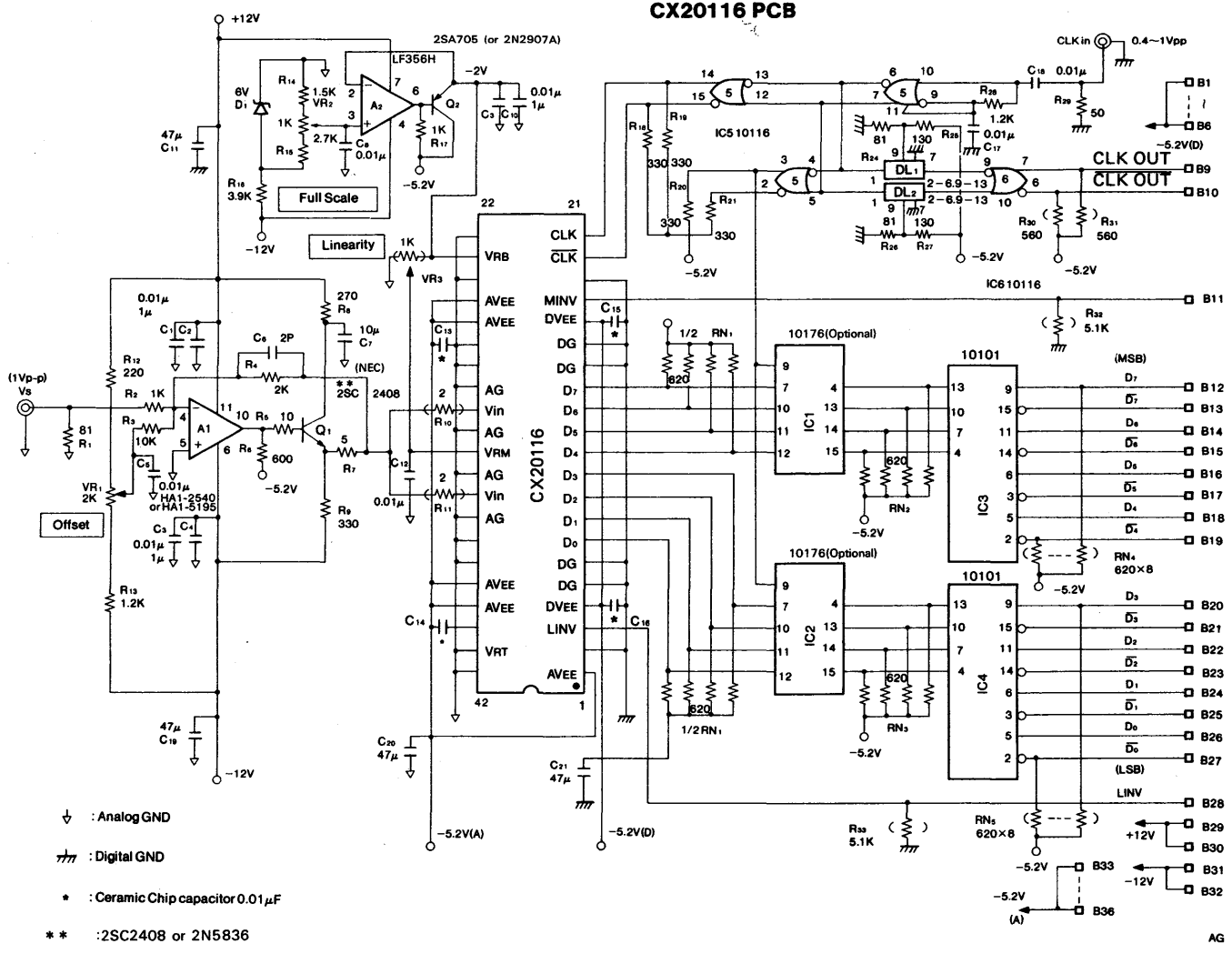
10-1. GND, V_{EE}

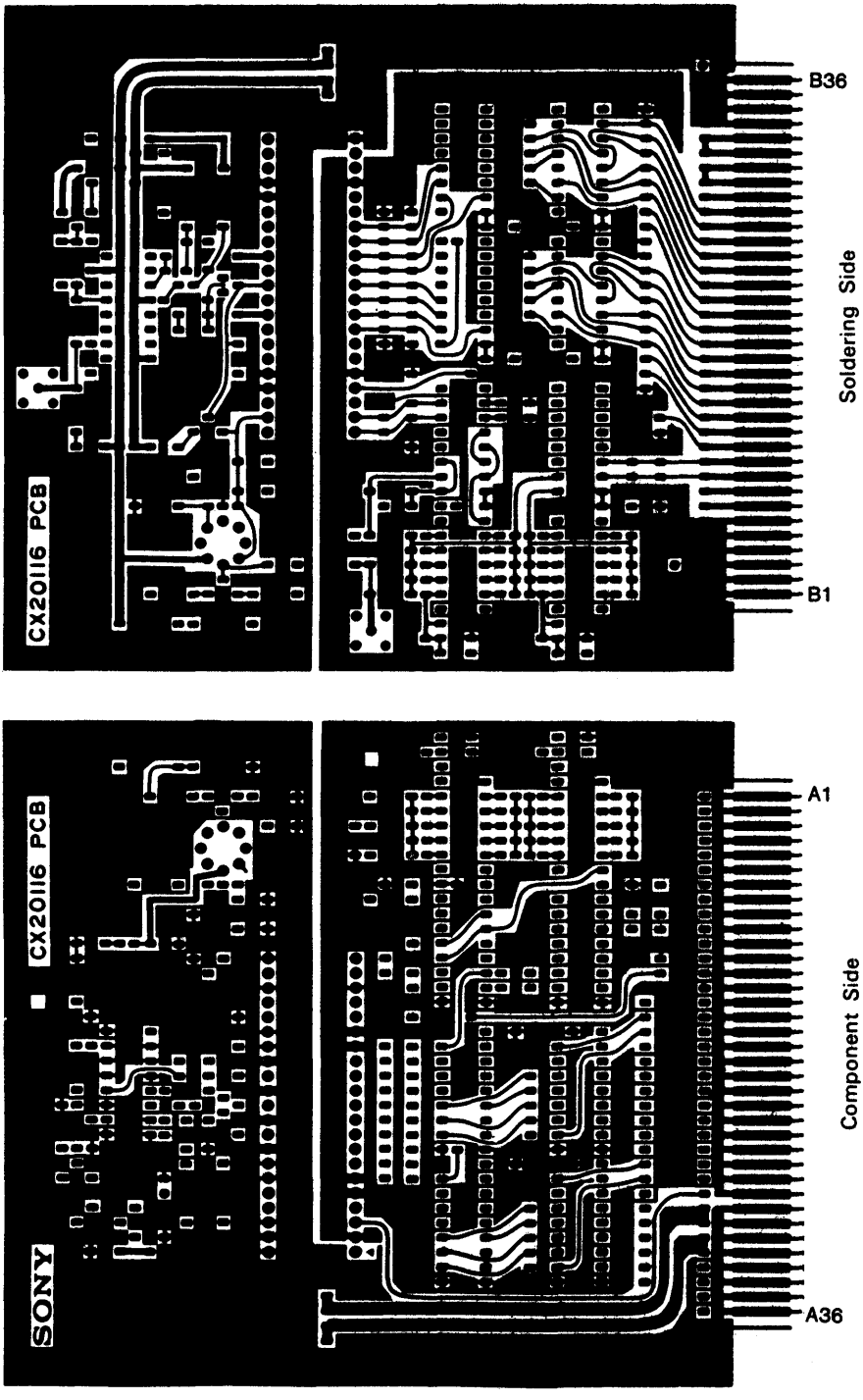
Avoiding the noise effect, GND and V_{EE} are separated in the analog and the digital system respectively. Take care not to happen potential difference more than 50 mV between the both systems.

10-2. Termination of Digital Output

Termination resistance of digital output is not mounted on the PCB. To prevent waveform distortions by reflection, it is recommended to terminate on a PCB that receives the signal.

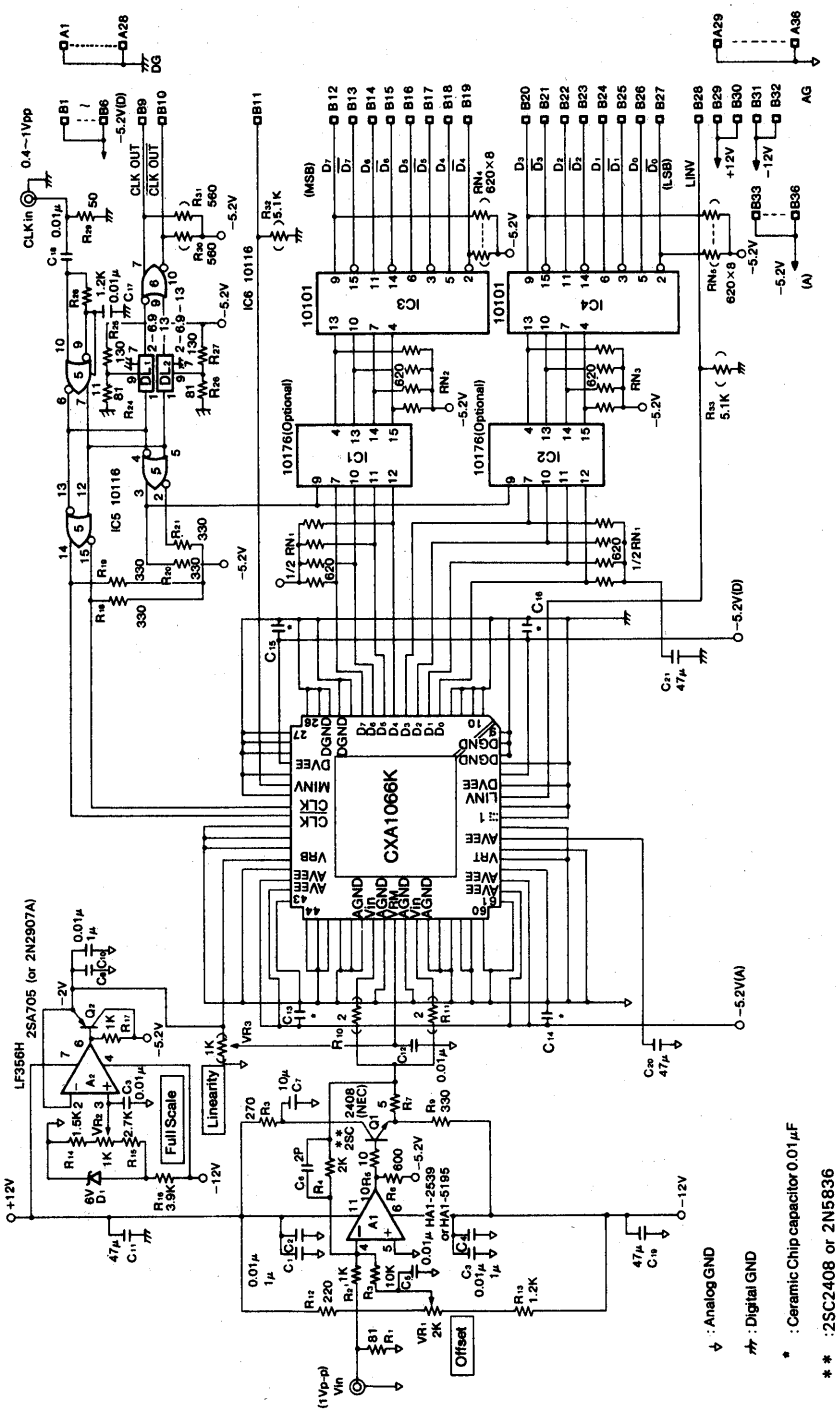
CX20116 PCB

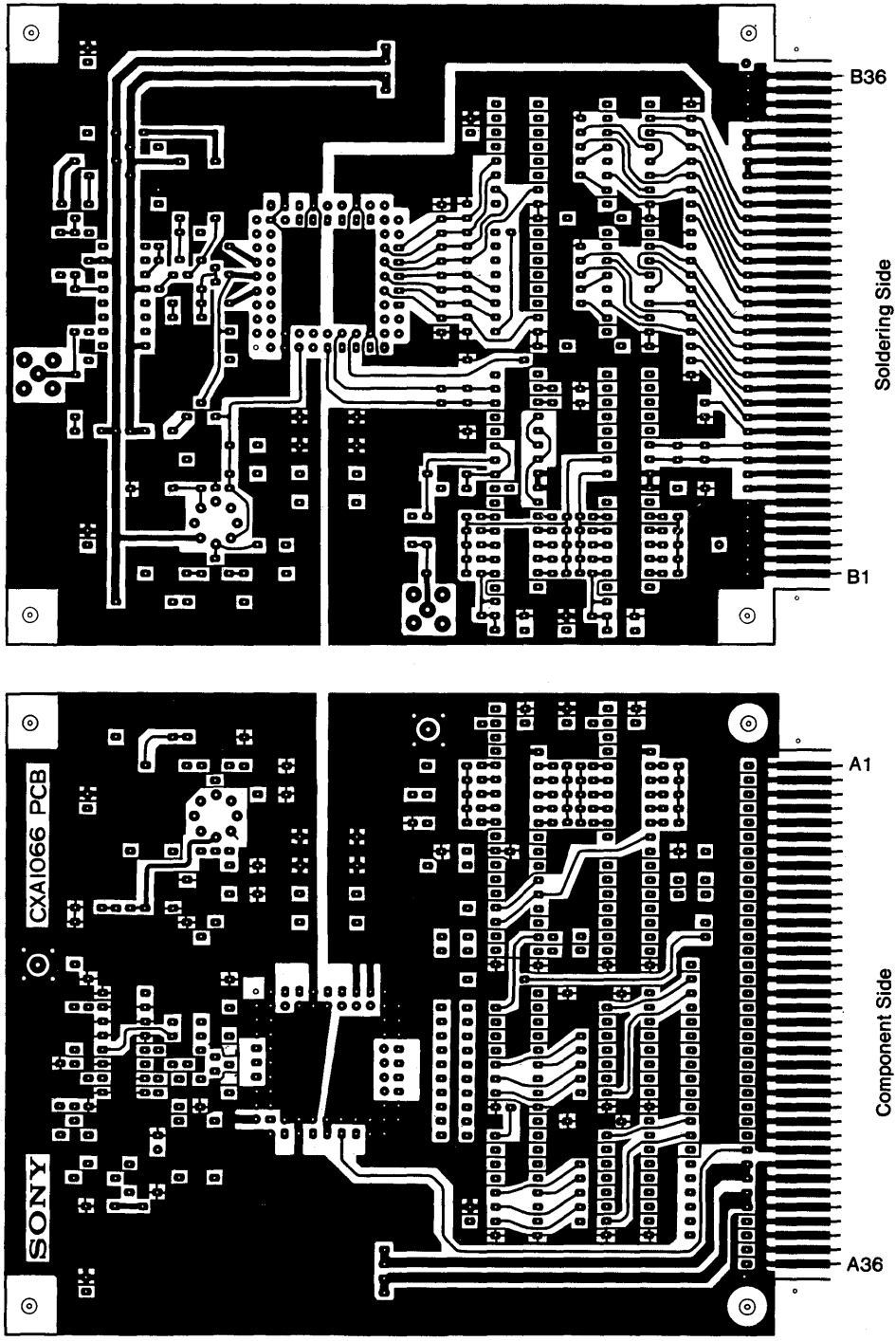

+12V
2SA705 (or 2N2907A)
LF356H
6V D1
1.5K VR2
1K
2.7K
Full Scale
Linearity
-12V
-2V
-5.2V
CX20116
CLK
VRB
AVEE
MINV
DVEE
DG
D7
D6
D5
D4
D3
D2
D1
D0
AG
Vin
VRM
VRT
LINV
IC5 10116
IC6 10116
CLK in
0.4~1Vpp
CLK OUT
DL1
DL2
2-6.9-13
10176(Optional)
10101
IC1
IC2
IC3
IC4
RN1
RN2
RN3
RN4 620×8
RN5 620×8
(MSB)
(LSB)
(1Vp-p) Vs
Offset
VR1 2K
VR2
VR3 1K
HA1-2540 or HA1-5195
(NEC)
** 2SC 2408
Q1
A1
A2
Analog GND
Digital GND
* : Ceramic Chip capacitor 0.01μF
** :2SC2408 or 2N5836
-5.2V(A)
-5.2V(D)
AG
B1
B6
B9
B10
B11
B12
B13
B14
B15
B16
B17
B18
B19
B20
B21
B22
B23
B24
B25
B26
B27
B28
B29
B30
B31
B32
B33
B36
A1
A28
A29
A36
DG



CX20116PCB Pattern

CXA1066 PCB


CXA1066K
IC1 10176(Optional)
IC2 10176(Optional)
IC3 10101
IC4 10101
IC5 10116
IC6 10116
LF356H
2SA705 (or 2N2907A)
Linearity
Full Scale
Offset
CLK out
CLK in
0.4~1Vpp
+12V
-12V
-5.2V
-5.2V(D)
-5.2V(A)
(MSB)
(LSB)
LINV
(1Vp-p) Vin
: Analog GND
: Digital GND
* : Ceramic Chip capacitor 0.01μF
** : 2SC2408 or 2N5836

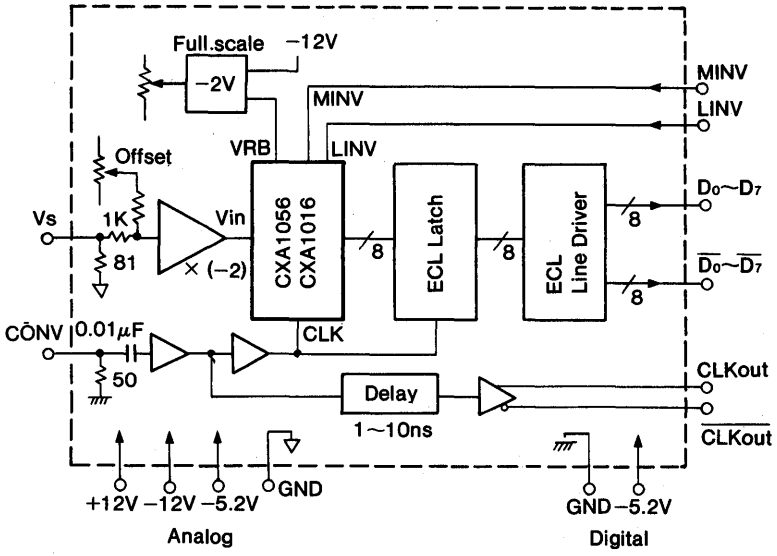


CXA1066PCB Pattern

8 bit, 50 MSPS/30 MSPS A/D Evaluation Board

Description

CXA1056P PCB/CXA1056K PCB/CXA1016P PCB/CXA1016K PCB are the evaluation printed circuit boards for 8 bit high speed A/D converter CXA1056P/CXA1056K/CXA1016P/CXA1016K. On this one board, A/D converter, driver, reference voltage source, latches and ECL line drivers are mounted, and this PCB is designed to achieve the best performance of the A/D converter.



PCB Characteristics

- Analog input band width (including A/D input driver): 20 MHz (at −3 dB): CXA1056P PCB; 15 MHz (at −3 dB): CXA1016P PCB
- Analog input impedance: 75Ω
- Complementary ECL output
- Clock output (Delay time 0 ~ 10ns adjustable)

NE89644-HP

Supply Voltage

• Analog	+12V	80 (Max.)	mA
	−12V	80 (Max.)	mA
	−5.2V	250 (Max.)	mA
• Digital	−5.2V	460 (Max.)	mA

1. Analog Input (Vs)

Item	Min.	Typ.	Max.	Unit
AC Input Voltage Amplitude*		1	1.1	V
Offset Adjustable Range	−0.25	0	1	V
Input Impedance	–	75	–	Ω

* peak to peak

2. Convert Input Signal (CONV)

Item			Min.	Typ.	Max.	Unit
Input Voltage*			0.6		1.0	V
Input Impedance			–	50	–	Ω
DC Level Range			−3		3	V
Pulse Width	CXA1056P PCB CXA1056K PCB	Tcw 1	14.0			ns
		Tcw 0	4.5			ns
	CXA1016P PCB CXA1016K PCB	Tcw 1	22.5			ns
		Tcw 0	7.5			ns

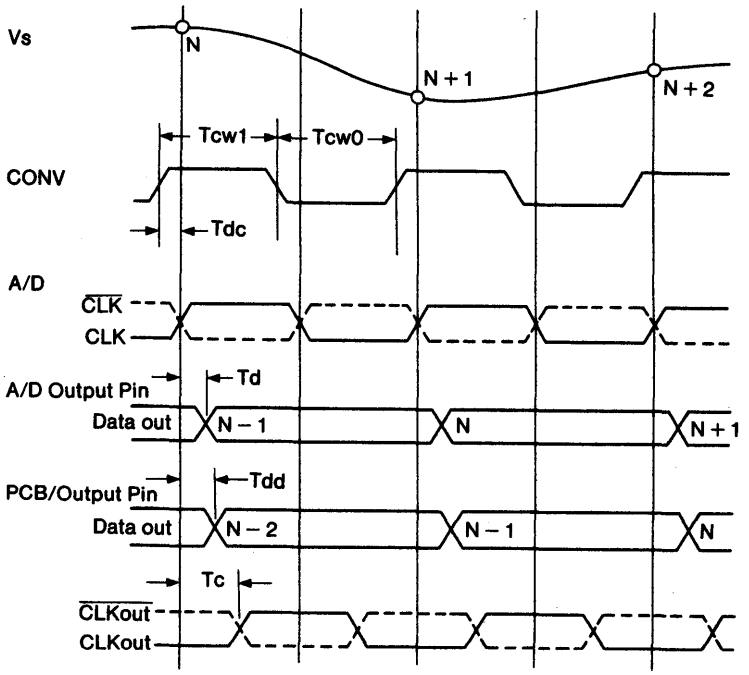
* peak to peak

3. Control Input (MINV, LINV)
ECL 10K compatible

4. Digital Output (D_0~D_7, $\overline{D}_0$~$\overline{D}_7$)
ECL 10K compatible, complementary output

5. Clock Output
ECL 10K compatible, complementary output
Delay time adjustable

6. Timing Chart



Item	Symbol	Min.	Typ.	Max.	Unit
Conversion Delay	Tdc		4.0		ns
Data Delay	Tdd		5.5		ns
Clock Delay Adjustable Range*	Tc	1		10	ns

* Adjustable in 1ns step by taps

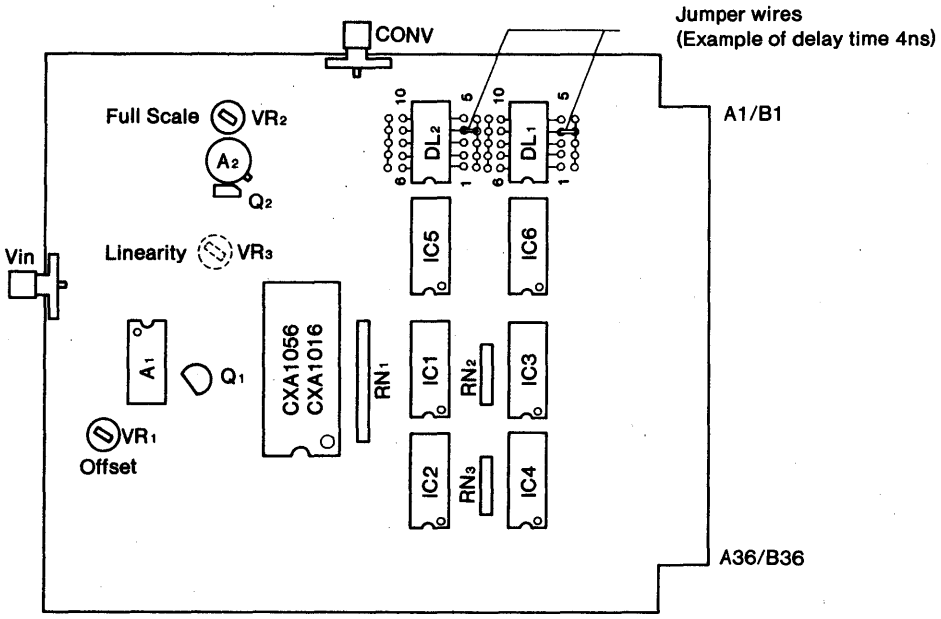
7. Output Coding

MINV LINV	0 0	0 1	1 0	1 1
0V	111 . . . 11	100 . . . 00	011 . . . 11	000 . . . 00
.	111 . . . 01	100 . . . 01	011 . . . 10	000 . . . 01
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
Vin .	100 . . . 00	111 . . . 11	000 . . . 00	011 . . . 11
.	011 . . . 11	000 . . . 00	111 . . . 11	100 . . . 00
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	000 . . . 01	011 . . . 10	100 . . . 01	111 . . . 10
−2V	000 . . . 00	011 . . . 11	100 . . . 00	111 . . . 11

1 : V_{IH}
0 : V_{IL}

8. Adjusting Method of Clock Output Delay Time

Clock output delay time can be adjusted by jumper wires position on the PCB.
Tap positions should be changed simultaneously in CLK and $\overline{CLK}$, avoiding the effect of waveform distortion.
Delay time in each taps are 1ns.



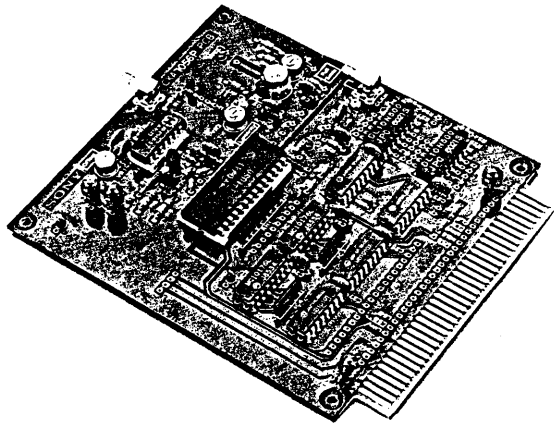
9. Note on Application

9-1. GND, VEE

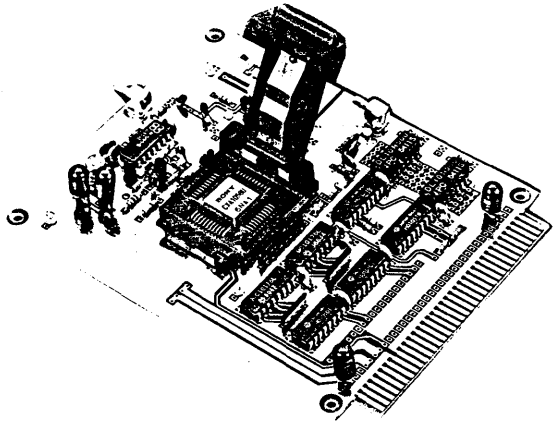
Avoiding the noise effect, GND and VEE are separated in the analog and the digital system respectively. Take care not to happen potential difference more than 50 mV between the both systems.

9-2. Termination of Digital Output

Termination resistance of digital output is not mounted on the PCB. To prevent waveform distortions by reflection, it is recommended to terminate on a PCB that receives the signal.

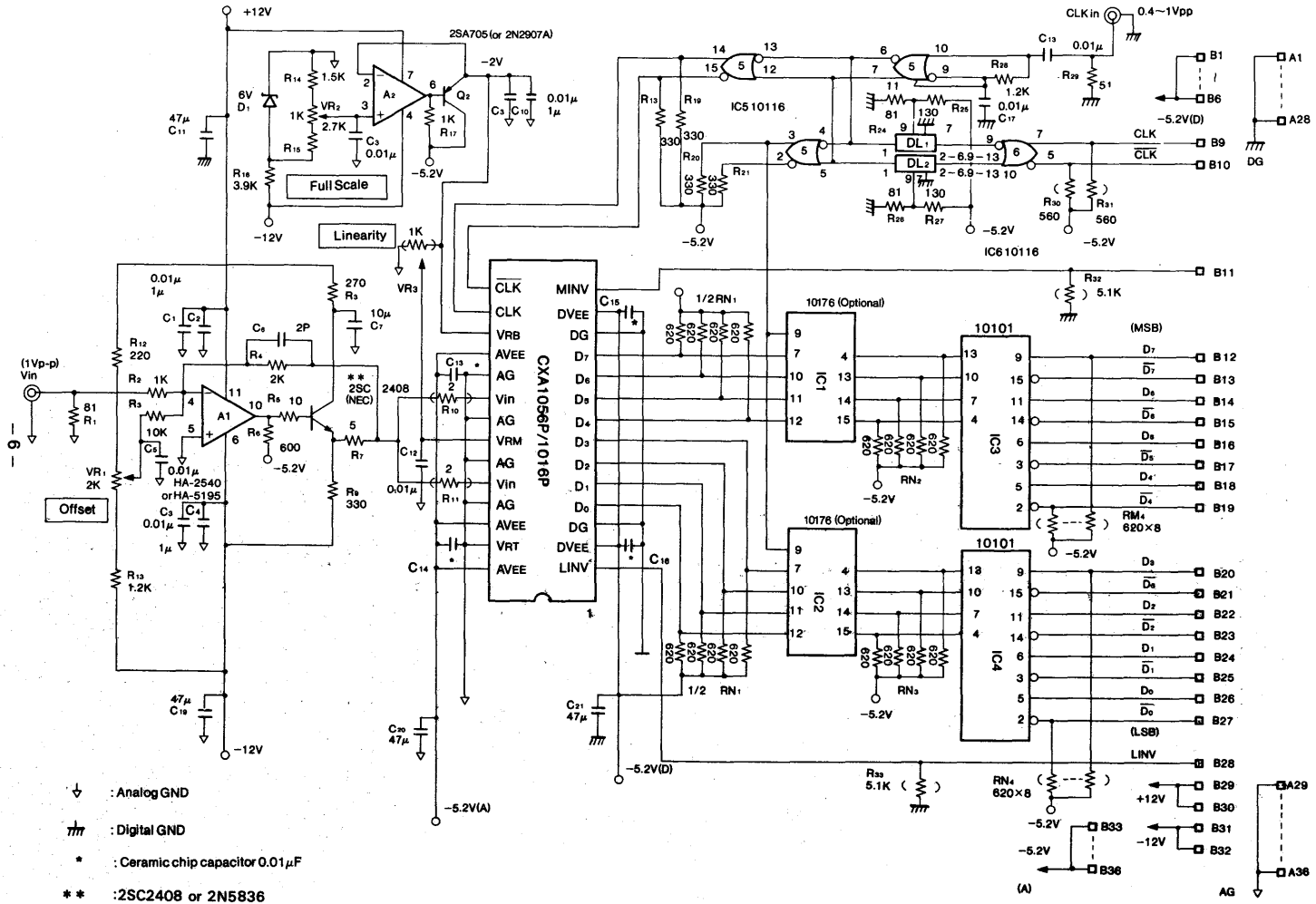


CXA1056P/CXA1016P PCB



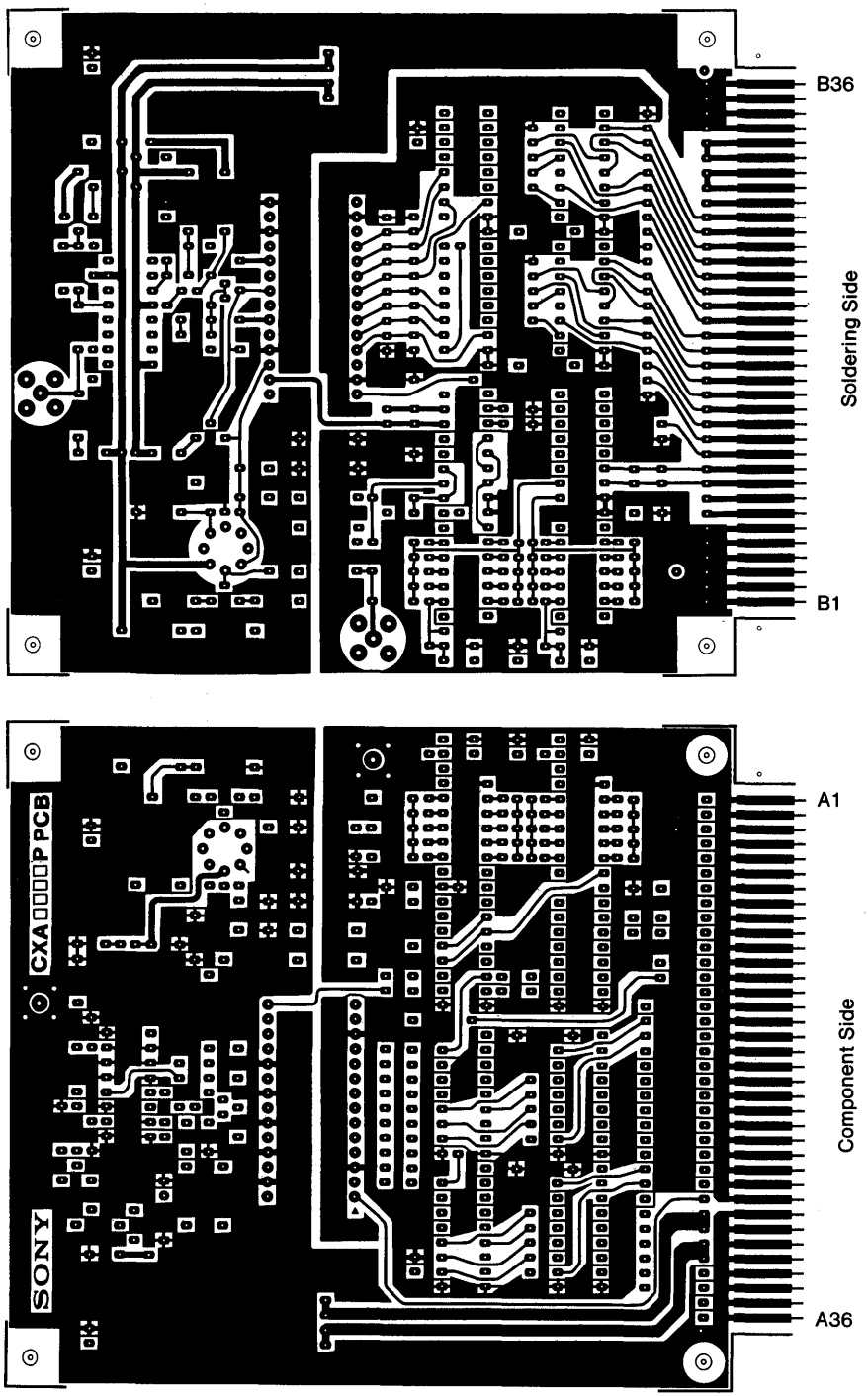
CXA1056K PCB/CXA1016K PCB

CXA1056P PCB/CXA1016P PCB



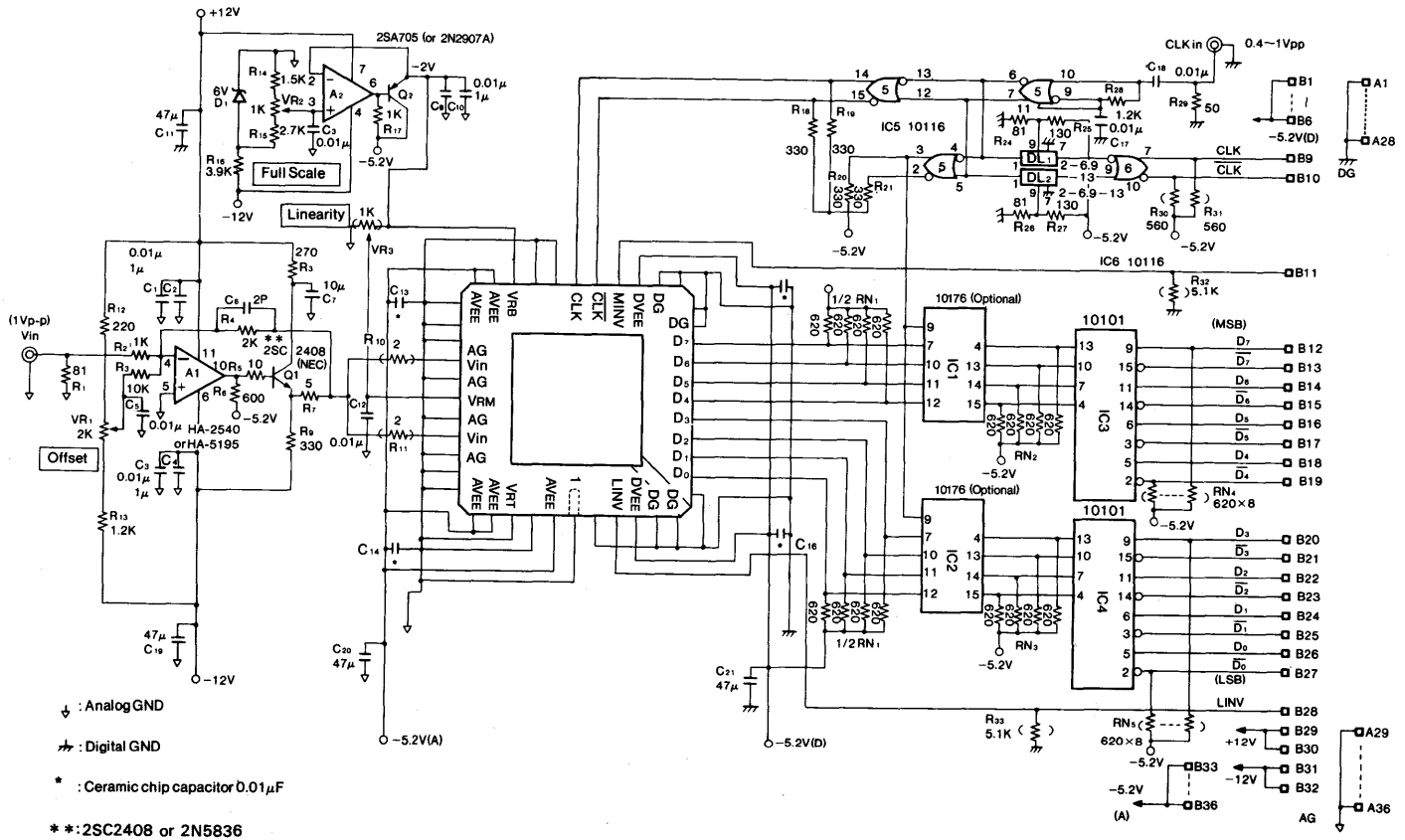
SONY

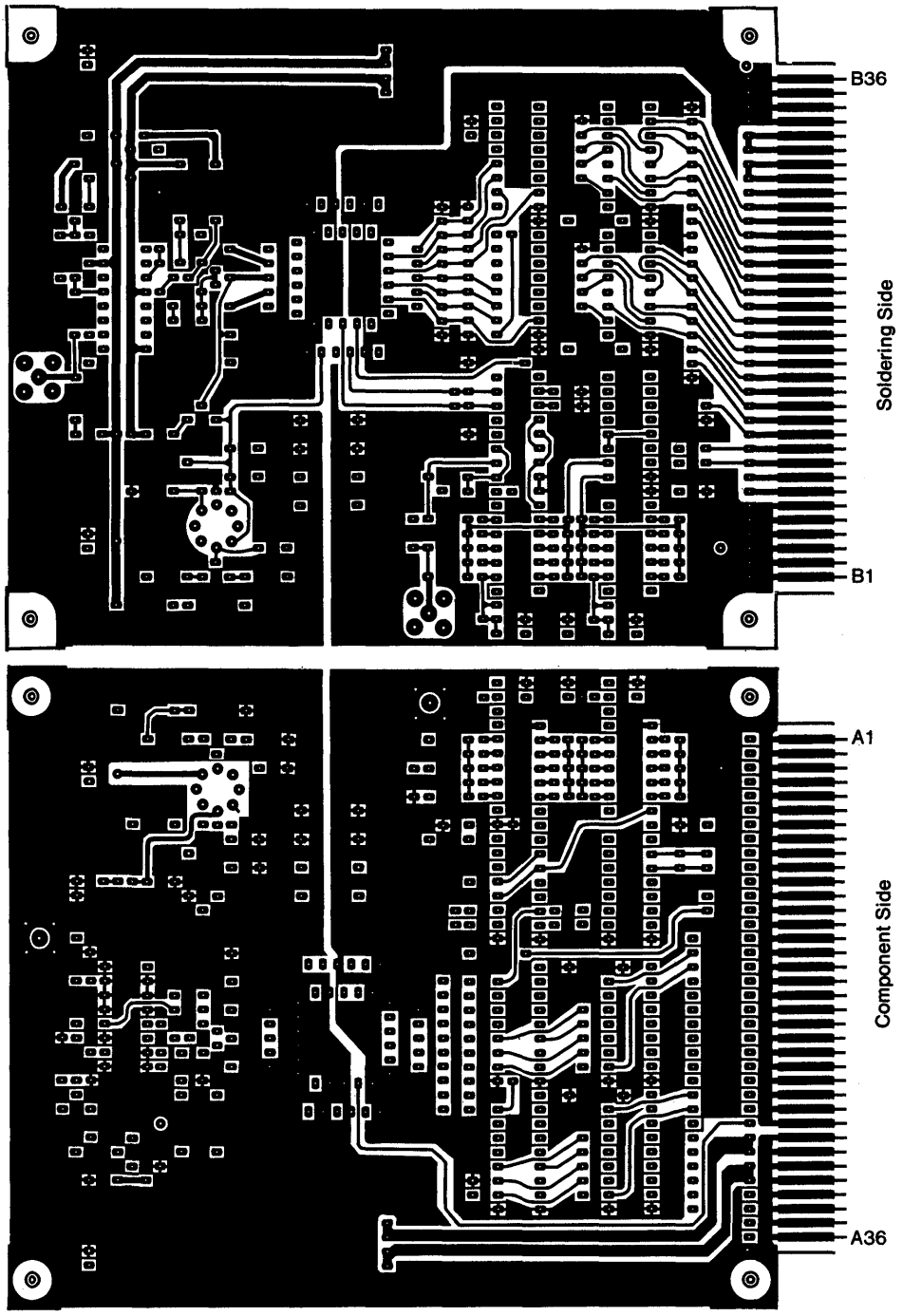
CXA1056P PCB/CXA1056K PCB
CXA1016P PCB/CXA1016K PCB



CXA1056P PCB/CXA1016P PCB

CXA1056K PCB/CXA1016K PCB





CXA1056K PCB/CXA1016K PCB Pattern

8-bit 200/300 MSPS ADC Evaluation Board

Advance Information

Notice: This specification is subject to change.

Feature

CXA1076AK PCB/CXA1176AK PCB are the evaluation printed circuit boards for 8-bit ultra fast A/D converter IC's CXA1076AK PCB/CXA1176AK PCB. The board is consisted of an ultra fast ADC, input amplifier, voltage reference, clock buffer, timing circuit and ECL buffer for the output data.

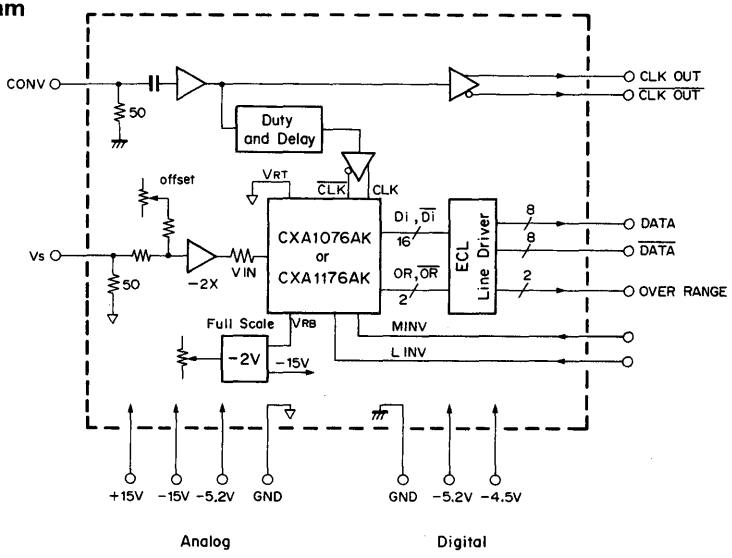
The input impedance both for analog and clock input terminals is 50 Ω. The output terminals provide complementary ECL level having a capability of driving into 50 Ω load. Complementary ECL clock output is provided for external use.

The input voltage range is 1 V peak to peak into 50 Ω. The input amplifier has a gain of −2X, and has a capability to adjust offset voltage to interface to the ADC's input level of 0 to −2 V.

PCB Characteristics

• Analog input impedance			50	Ω	
• Analog input level			1	V	(peak to peak)
• DC offset voltage range			0 to +1	V	
• Clock input impedance			50	Ω	
• Supply voltage					
Analog	+15	V	50	mA	
	−15	V	100	mA	
	−5.2	V	295	mA	(CXA1076AK PCB)
			295	mA	(CXA1176AK PCB)
Digital	−5.2	V	108	mA	(CXA1076AK PCB)
			108	mA	(CXA1176AK PCB)
	−4.5	V	1000	mA	

Block Diagram



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Electrical Characteristics

1) Analog Input (Vs)

Item	Min.	Typ.	Max.	Unit
AC peak to peak level		•	1	V
DC input level	−0.2	0	+1	V
Input impedance		50		Ω

2) Clock Input (CONV)

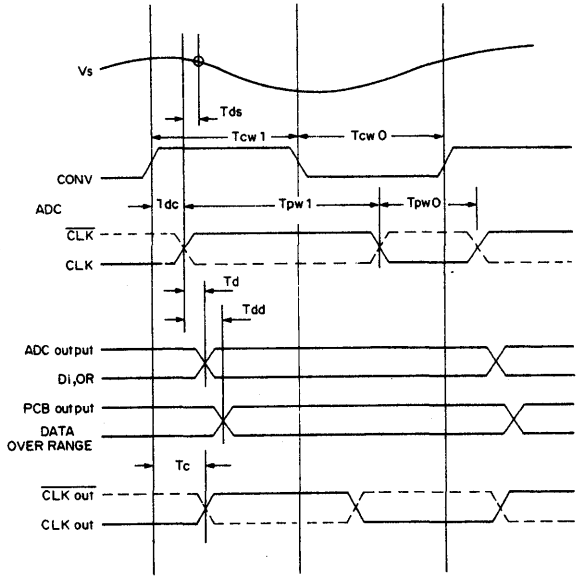
		Min.	Typ.	Max.	Unit
Input voltage		0.3	0.8	1	V
DC input level		−5	0	+5	V
Input impedance			50		Ω
Pulse width	Tcw1		1/2fs		
	TcwO		1/2fs		

3) Control input (MINV, LINV)
ECL compatible (Low with left open)

4) Digital output (DATA: D_0 to D_7, $\overline{D_0}$ to $\overline{D_7}$, OVER RANGE)
ECL 100K compatible, without pulling down

5) Clock output (CLKout, $\overline{\text{CLKout}}$)
ECL 100K compatible, without pulling down

6) Timing Chart



CXA1076AK PCB

Item	Symbol	Min.	Typ.	Max.	Unit
Conversion delay	Tds	0.6	0.8	1.1	ns
	Tdc	4.0		6.0	ns
Data delay	Td	2.4	2.7	3.1	ns
	Tdd		3.8		ns
Clock delay	Tc		4.0		ns

CXA1176AK PCB

Item	Symbol	Min.	Typ.	Max.	Unit
Conversion delay	Tds	0.6	0.8	1.1	ns
	Tdc	4.0		6.0	ns
Data delay	Td	2.4	2.7	3.1	ns
	Tdd		3.8		ns
Clock delay	Tc		4.0		ns

Td1 and Td2 are adjustable: 0 to 2 ns. See paragraph 3 for more detail.

Adjustment

1. Input Full Scale Range

The input full scale range of the ADC is 0 to − 2V, which is determind by VRT(0V) and VRB(− 2V) terminals of the ADC. The voltage reference on the PCB is factory adjusted for − 2V for VRB.

'Full Scale' trimmer VR3 can be used to adjust VRB by monitering TP1.

As the input amplifier has a gain of − 2X, the input range at the input port Vs is 1V peak to peak for full scale input range.

2. Input Offset voltage

'Offset' trimmer VR1 can be used to adjust input offset voltage. The trimmer is factory adjusted to give a − 1V offset voltage at the ADC's input terminal with no input voltage applied to the input port Vs.

The input signal of 1V peak to peak with a DC offset of 0 to + 1V can be adjusted by VR1 that the input signal falls into ADC's full scale range.

3. Clock Duty and Data Output Timing (Refer to Timing Chart)

Convert signal at CONV port is AC coupled and translated into ECL level. A clean sine wave or a square wave with 50% duty is recommended as CONV signal. CONV signal is devided into two directions: one for CLKout pulse for external use and another for CLK pulse for the ADC.

CLKout pulse is simply buffered by 100K line receiver and appears at CLKout port of the PCB with delay time of Tc from the CONV signal.

Two delay lines TD1 and TD2 have two roles for timing adjustment, clock duty and data output timing. TD1 and TD2 can be adjusted by sliding a tab on the top of the delay line. Total delay time is 2 ns for both delay lines. Set TD1 TD2 for normal setup.

In these setup the clock pulse width tpw1, ADC clock timing Tdc, clock output timing Tc and data output timing are stated nominally as follows,

$$Tpw1 = Tcw1 + (Td1 - Td2)\ ns$$
$$Tdc = 4.0 + Td2\ ns$$
$$Tc = 4.0\ ns$$
$$Tdc + Tdd = 8.0 + Td2\ ns$$

where Tcw1 is a half of the sampling period 1/2fs if the CONV signal has the duty of 50%.

Td1 - Td2 adjusts the clock duty and Td2 adjusts the timing between clock output and data output.

4. Linearity

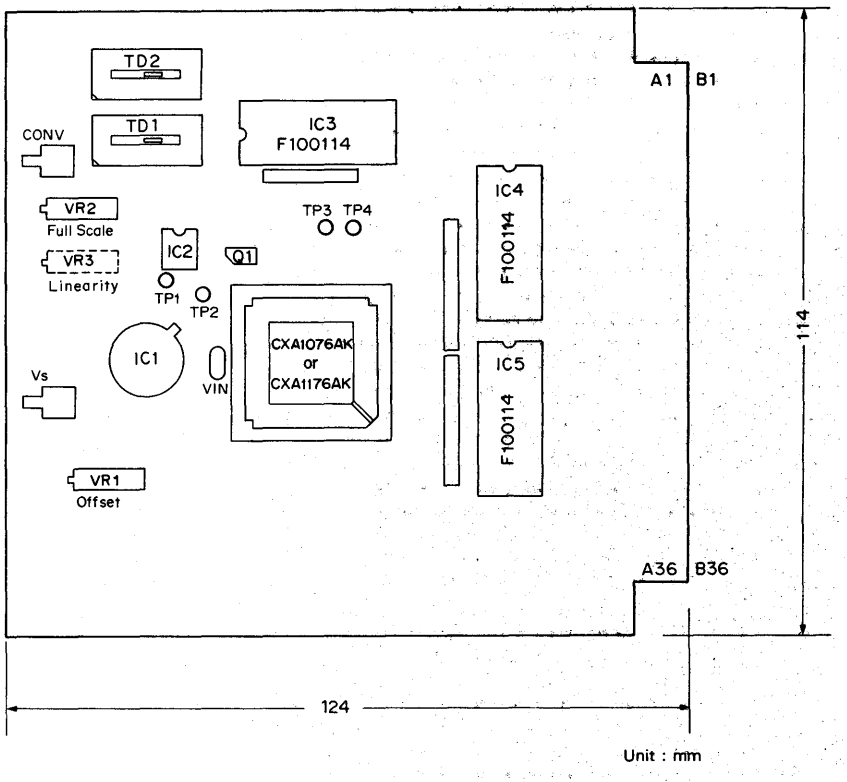
Although the ADC itself has an internal linearity compensation circuit and has the integral and a differential linearity of ± 1/2 LSB, more precise adjustment for the integral linearity can be obtained by adjusting 'Linearity' trimmer VR2 (not mounted, use 1KΩ potentiometer).

Output Format

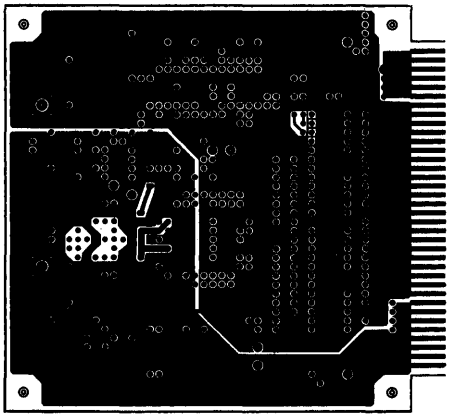
The table shows the output format for the ADC. Be careful that the PCB has the input amplifier with voltage gain of −2X.

Vin	Step	MINV 1 LINV 1 OR MSB LSB	0 1 OR MSB LSB	1 0 OR MSB LSB	0 0 OR MSB LSB
		0 0 0 0 · · · 0 0	0 1 0 0 · · · 0 0	0 0 1 1 · · · 1 1	0 1 1 1 · · · 1 1
0V					
	0	1 0 0 0 · · · 0 0	1 1 0 0 · · · 0 0	1 0 1 1 · · · 1 1	1 1 1 1 · · · 1 1
	1	1 0 0 0 · · · 0 1	1 1 0 0 · · · 0 1	1 0 1 1 · · · 1 0	1 1 1 1 · · · 1 0
		·	·	·	·
		·	·	·	·
		·	·	·	·
−1V	127	1 0 1 1 · · · 1 1	1 1 1 1 · · · 1 1	1 0 0 0 · · · 0 0	1 1 0 0 · · · 0 0
	128	1 1 0 0 · · · 0 0	1 0 0 0 · · · 0 0	1 1 1 1 · · · 1 1	1 0 1 1 · · · 1 1
		·	·	·	·
		·	·	·	·
		·	·	·	·
	254	1 1 1 1 · · · 1 0	1 0 1 1 · · · 1 0	1 1 0 0 · · · 0 1	1 0 0 0 · · · 0 1
	255	1 1 1 1 · · · 1 1	1 0 1 1 · · · 1 1	1 1 0 0 · · · 0 0	1 0 0 0 · · · 0 0
−2V		1 1 1 1 · · · 1 1	1 0 1 1 · · · 1 1	1 1 0 0 · · · 0 0	1 0 0 0 · · · 0 0

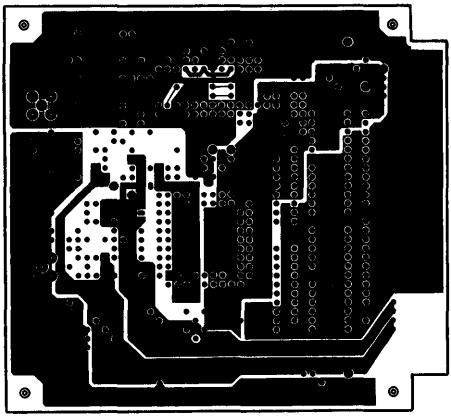
Component Position and Dimension (not to scale)



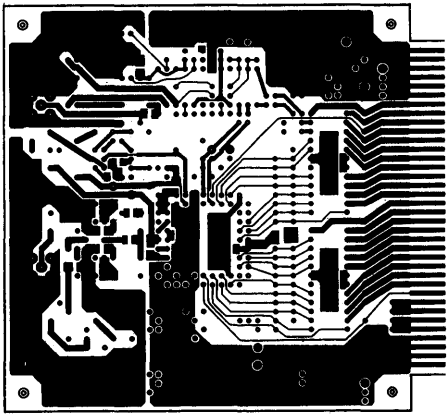
Board Layout (not to scale)



Component Side

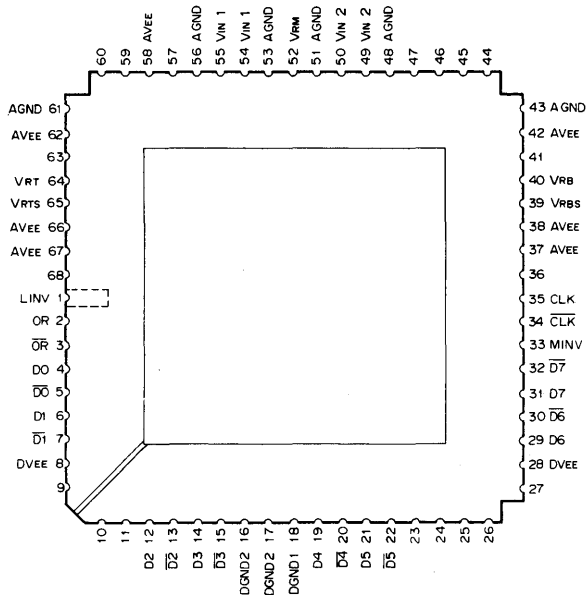


Inner Plane

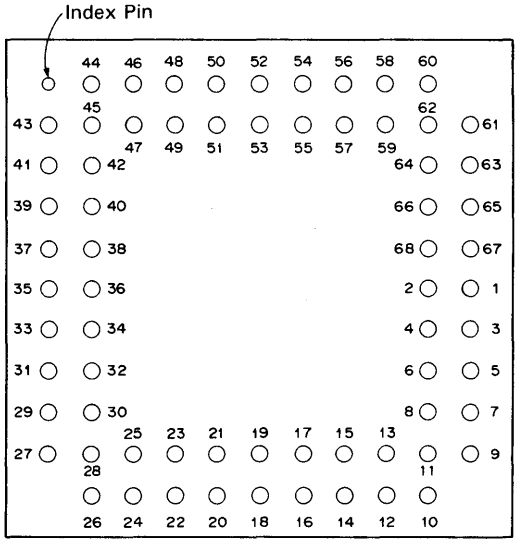


Soldering Side

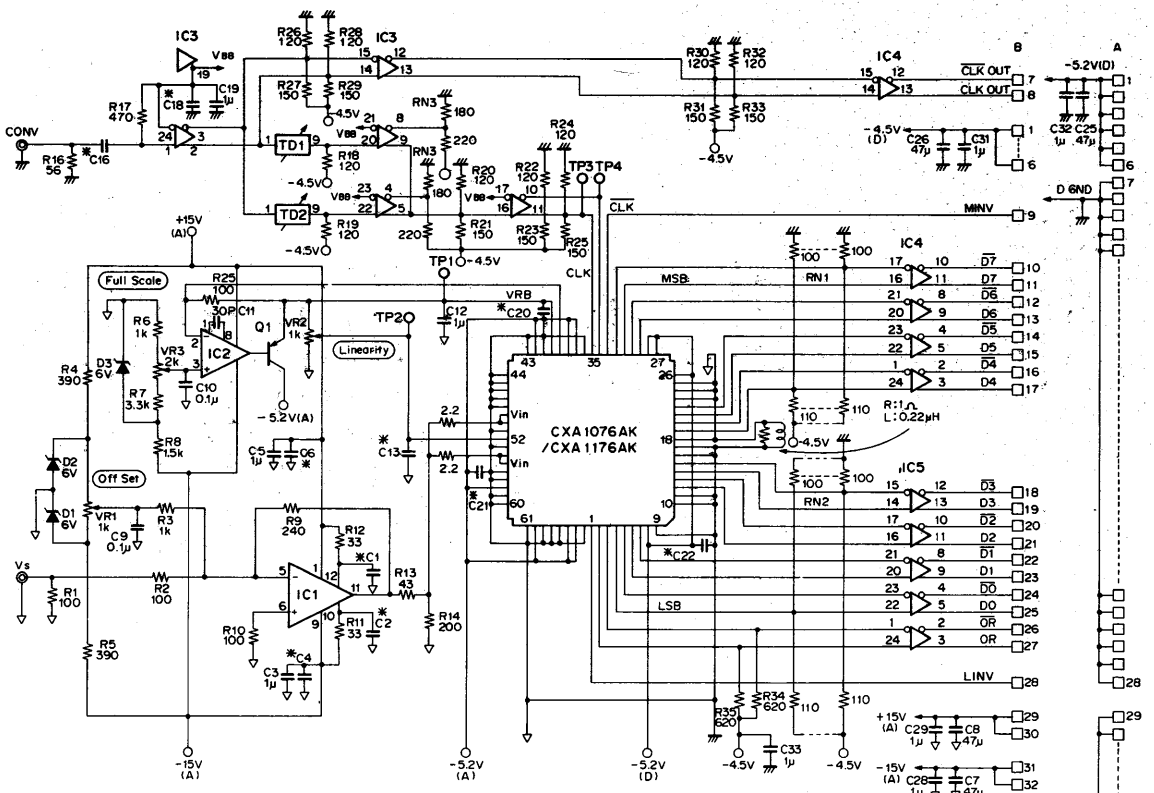
Pin Configuration CXA1076AK/CXA1176AK (Top View)



Pin Configuration of IC Socket (Bottom View)



Schematic Circuit



⏚ AnalogGND

⏚ DigitalGND

* : Ceramic Chip Capacitor 100nF

TD1, TD2 : Delay Line ELMEC VDK2010

IC2 : Comlinear CLC231

IC1 : μPC254D or equivalent

IC3, IC4, IC5 : F100114

Q1: 2SA733 (NEC) or 2N2907A

8-bit 20MSPS TTL I/O A/D Evaluation Board

Description

CXA1096P PCB is an evaluation printed circuit board for the 8-bit 20 MSPS TTL I/O A/D converter CXA1096P. A single or dual power supply can used on this board and evaluation for each is possible by switching the resistor and jumper wire.

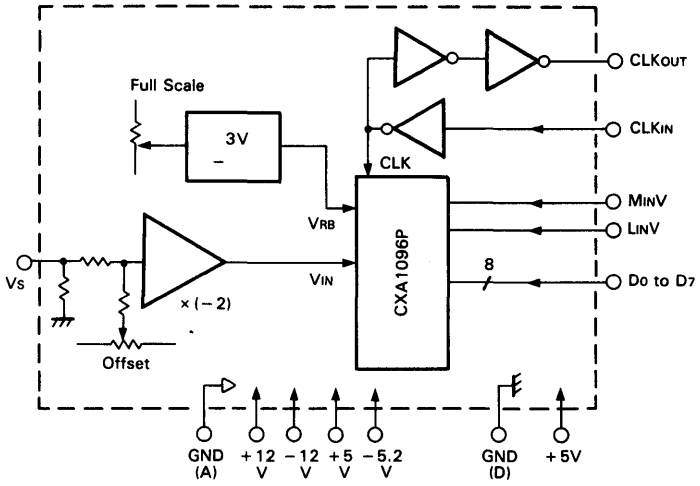


Fig. 1

Features

- Analog input bandwidth : 8 MHz (−3dB)
- Analog input impedance : 75 Ω
- TTL output
- TTL clock output

Supply Voltage (Single power supply)

Item		Min.	Typ.	Max.	Unit
Analog	+12V			90	mA
	−12V			90	mA
	+5.0V			90	mA
Digital	+5.0V			12	mA

Supply Voltage (Dual power supply)

Item		Min.	Typ.	Max.	Unit
Analog	+12V			90	mA
	−12V			90	mA
	−5.2V			100	mA
Digital	5.0V			12	mA

NE89647-HP

Analog Input [Vs] (Single power supply)

Item	Min.	Typ.	Max.	Unit
AC input voltage amplification		1		V
Offset variable		0		V
Input impedance		75		Ω

Analog Input (Dual power supply)

Item	Min.	Typ.	Max.	Unit
AC input voltage amplification		1		V
Offset variable		0		V
Input impedance		75		Ω

Conversion Input Signal (CONV.)

TTL level compatible

Control Input (MINV. LINV.)

TTL level compatible

Digital Output (D0 to D7)

TTL level compatible

Clock Output

TTL level compatible

Timing Chart

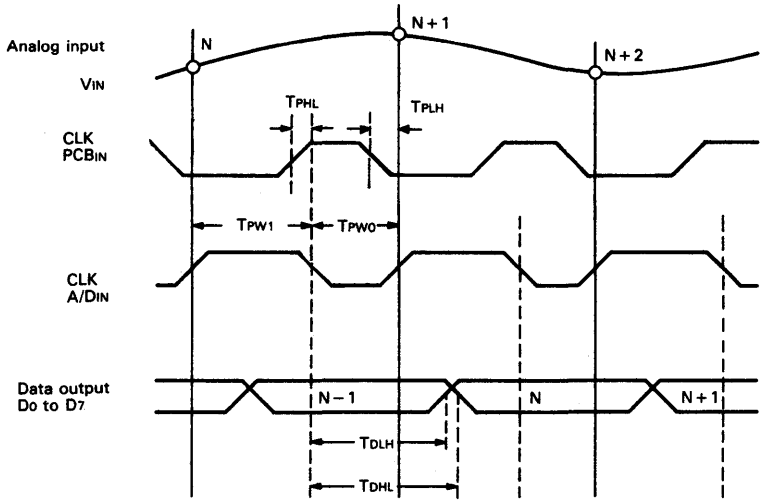


Fig. 2

Item	Symbol	Min.	Typ.	Max.	Unit
Propagation delay time	TPHL		10		ns
	TPLH		9		ns
Clock pulse width	TPW1	30			ns
	TPW0	10			ns
Output data delay	TDLH		25	30	ns
	TDHL		26	35	ns

Output Code Table

MIN V LIN V	0 0	0 1	1 0	1 1
0 or +5V	111 . . . 11	100 . . . 00	011 . . . 11	000 . . . 00
.	111 . . . 10	100 . . . 01	011 . . . 10	000 . . . 01
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	100 . . . 00	111 . . . 11	000 . . . 00	011 . . . 11
.	011 . . . 11	000 . . . 00	111 . . . 11	100 . . . 00
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
−2 or +3V	000 . . . 00	011 . . . 11	100 . . . 00	111 . . . 11

1: VIH VOH
0: VIL VOL

Description of Operation

As described earlier, the CXA1096P can be used either with the +5V single power supply or the dual power supply (+5V or −5.2V).

When some resistors and the jumper wires are switched, either of the power supplies can be used. The following is a description of how to use the power supplies.

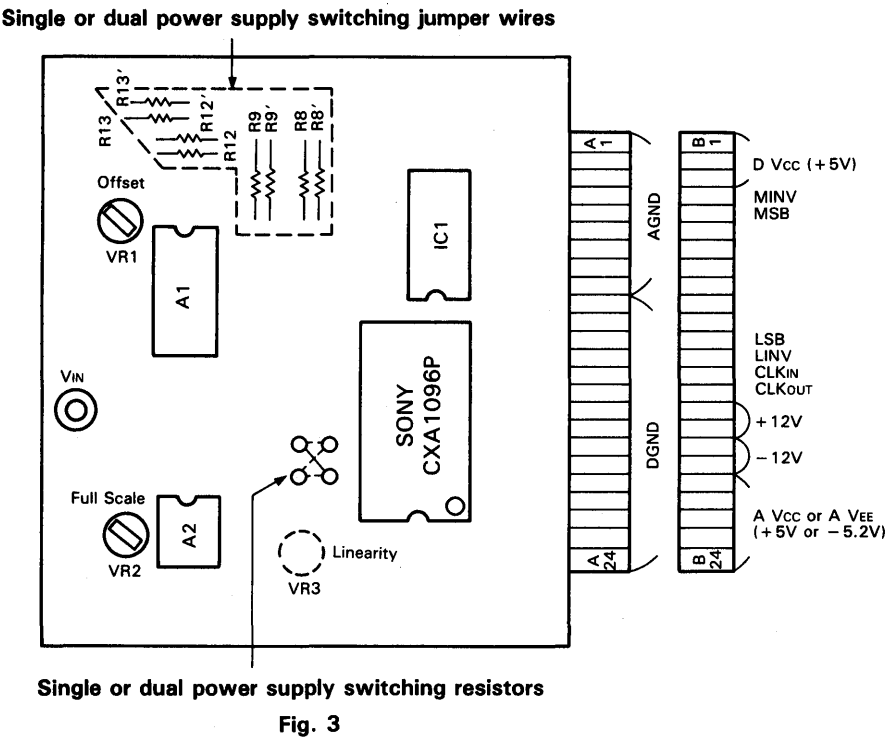
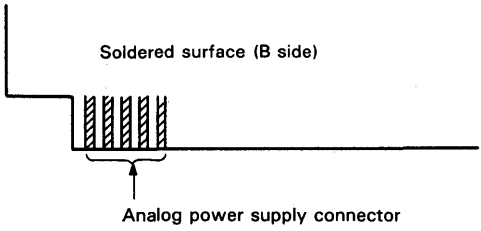


Fig. 3

For switching the +5.0V single or the +5.0V, −5.2V dual power supply, it is necessary to change the four resistors and jumper wires as well as the power supply fed from the edge connector.

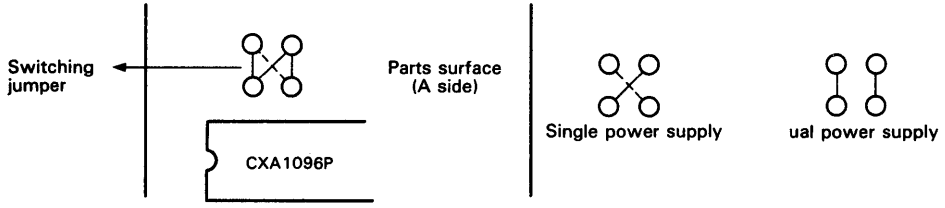
1) Power supply fed from the edge connector



Supply the +5.0V for A VCC from the upper connector when using the +5V single power supply.

Supply the −5.2V for AVEE from the upper connector when using the dual power supply.

2) Jumper wire



Cross the jumper wires when using the +5V single power supply, hook the jumper wires in parallel when using the dual power supply.

3) Resistor

When switching the single power supply and the dual power supply, the four resistors (R8, R8′), (R9, R9′), (R12, R12′) and (R13, R13′) must be changed.

Before shipment from the factory, resistors are set to the following for the single power supply.

R8 = 510Ω, R9 = 150Ω, R12 = 1.3kΩ, R13 = 100Ω

Change to the following when using the dual power supply.

R8′ = 360Ω, R9′ = 300Ω, R12′ = 220kΩ, R13′ = 1.2kΩ

4) Capacitor

The polarity of a 35V/10μ tantalum capacitor at the lower right of the PCB is reversed when the single power supply and the dual power supply are switched.

Notes on Use

- The +5V single power supply is set before shipment from the factory.
- The logic control input pin is open and kept at the high level.
- For the single power supply, be sure to cross one of the jumper wires on the back to avoid a short circuit.
- The GND VCC is separated into analog and digital systems to avoid noise interference. For use, it is recommended to use the AGND and DGND as well as the AVCC and DVCC in common, respectively, near the power supply to avoid an appreciable voltage differential between the two systems.

CXA1096P PCB Circuit Diagram (Single Power Supply)

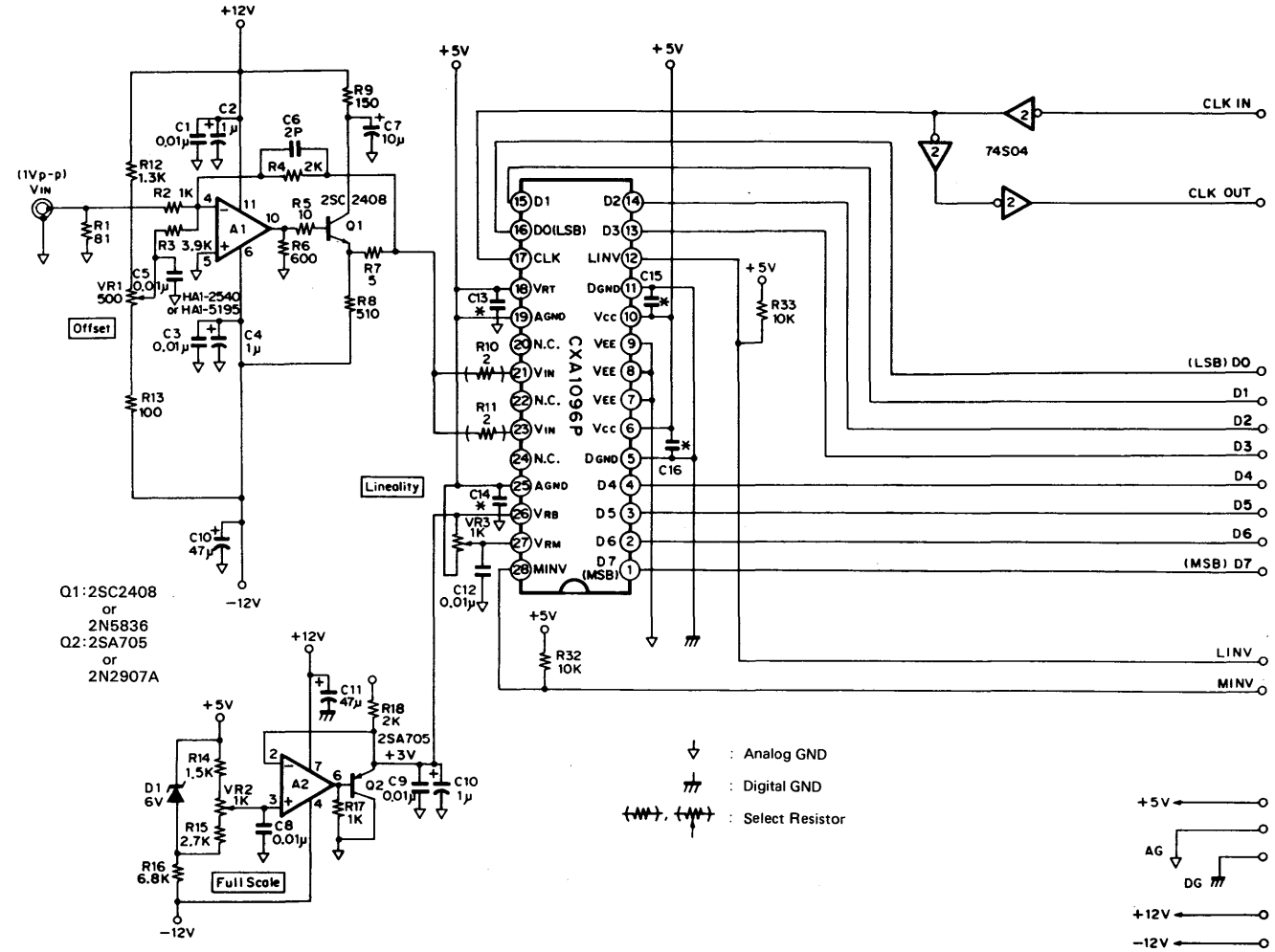


Fig. 4

CXA1096P PCB Circuit Diagram (Dual Power Supply)

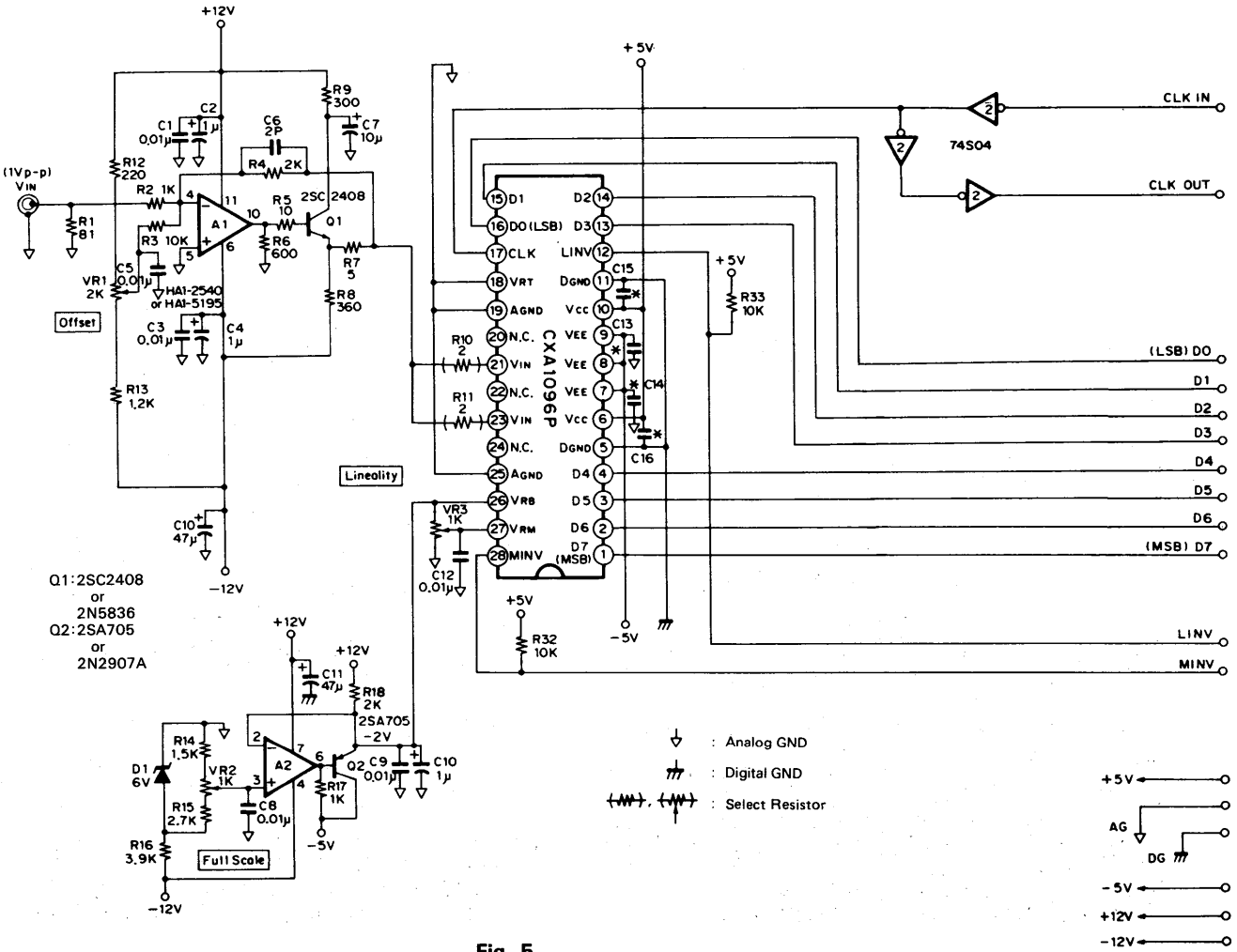
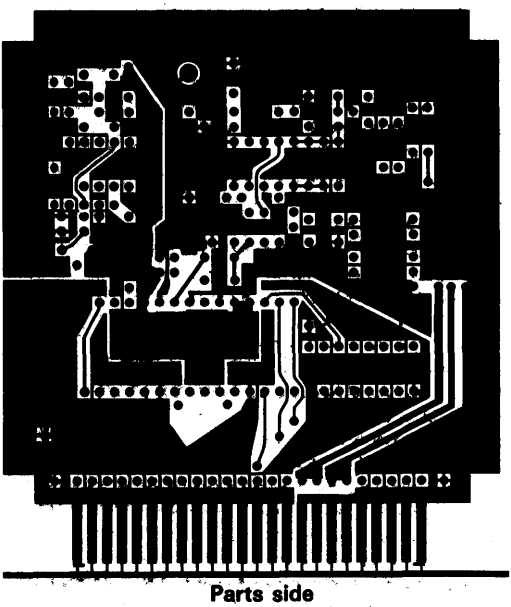
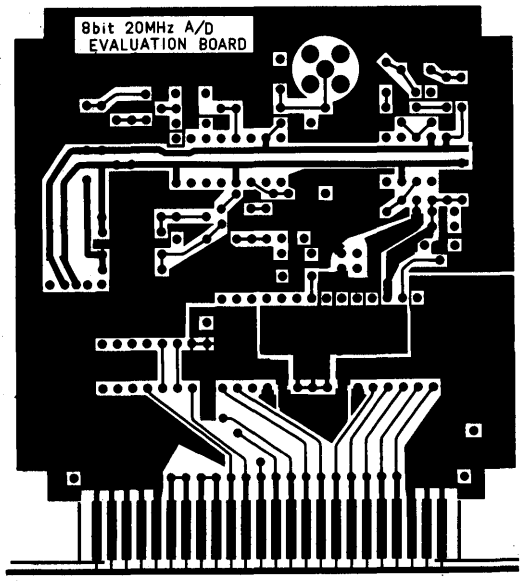


Fig. 5

CXA1096P PCB Pattern Diagram



Parts side
Fig. 6



Soldered side
Fig. 7

Silk Diagram

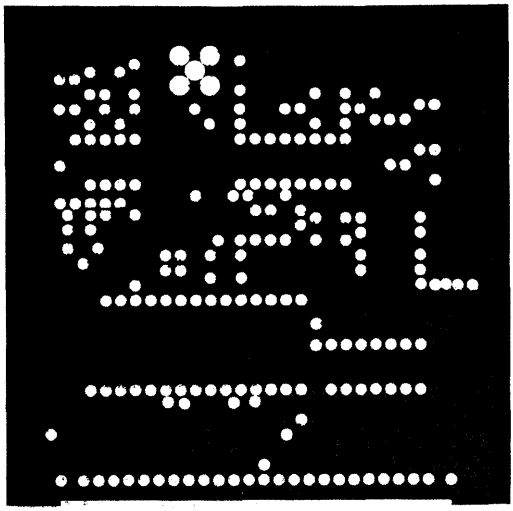


Fig. 8

SONY CXA1296P PCB

8-bit 20 MHz TTL I/O A/D Evaluation Board (FCXA1296P)

Description

CXA1296P PCB is an evaluation printed circuit board for the 8-bit 20MHz TTL I/O A/D converter CXA1296P. A single or dual power supply can used on this board for the evaluation of characteristics. The selection of either supply is possible by switching the resistors and jumper wires.

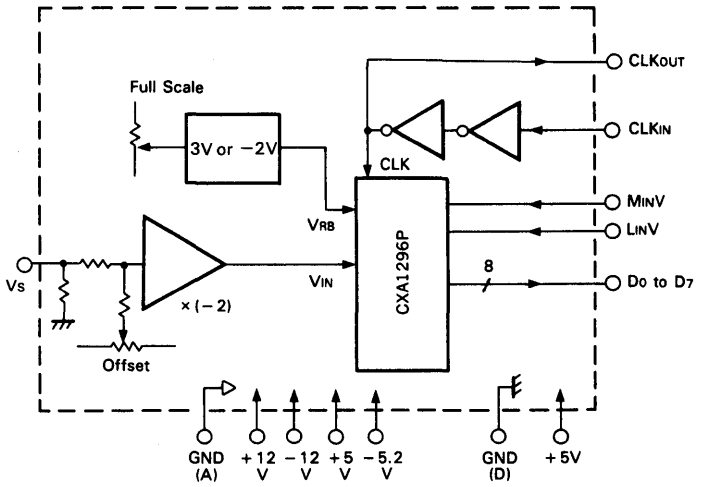


Fig. 1

Features

- Analog input bandwidth: 8 MHz (−3dB)
- Analog input impedance: 75Ω
- TTL output
- TTL clock output

Supply Voltage (Single power supply)

Item		Min.	Typ.	Max.	Unit.
Analog	+ 12V			90	mA
	− 12V			90	mA
	+ 5.0V			90	mA
Digital	+ 5.0V			12	mA

Supply Voltage (Dual power supply)

Item		Min.	Typ.	Max.	Unit.
Analog	+ 12V			90	mA
	− 12V			90	mA
	− 5.2V			100	mA
Digital	5.0V			12	mA

NE89530-HP

Analog Input [Vs] (Single power supply)

Item	Min.	Typ.	Max.	Unit.
AC input voltage amplification		1		V
Offset variable		0		V
Input impedance		75		Ω

Analog Input (Dual power supply)

Item	Min.	Typ.	Max.	Unit.
AC input voltage amplification		1		V
Offset variable		0		V
Input impedance		75		Ω

Conversion Input Signal (CONV.)
TTL level compatible

Digital Output (D0 to D7)
TTL level compatible

Control Input (MINV. LINV.)
TTL level compatible

Clock Output
TTL level compatible

Timing Chart

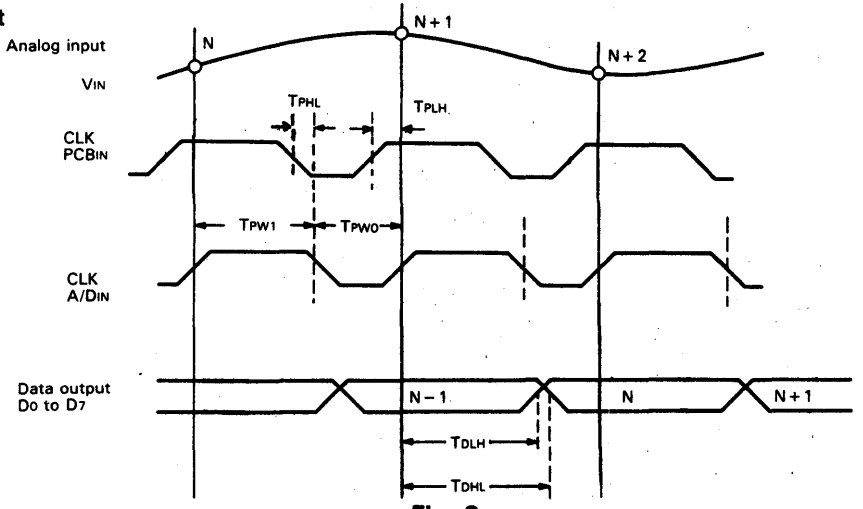


Fig. 2

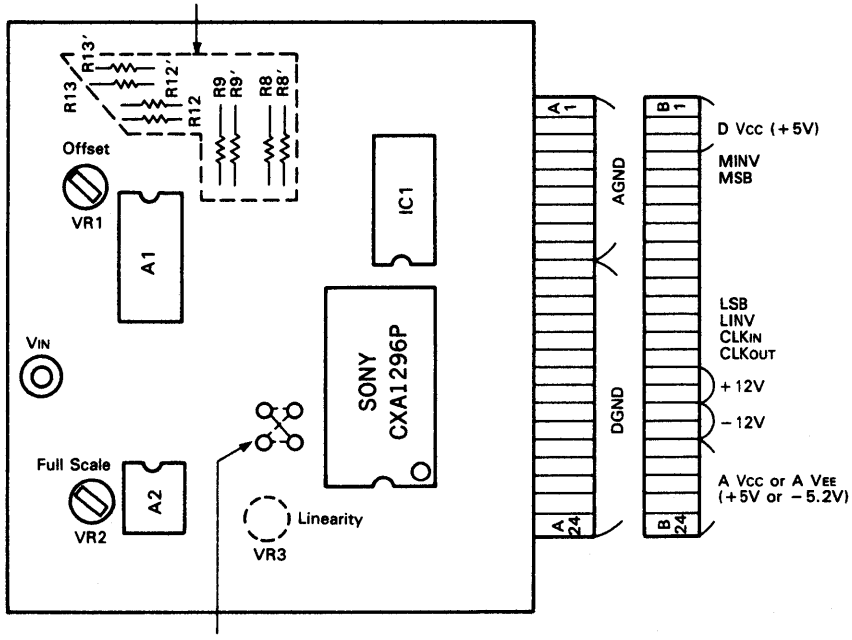
Item	Symbol	Min.	Typ.	Max.	Unit.
Propagation delay time	T_{PHL}		10		ns
	T_{PLH}		9		ns
Clock pulse width	T_{PW1}	30			ns
	T_{PWO}	10			ns
Output data delay	T_{DLH}		25	30	ns
	T_{DHL}		26	35	ns

Description of Operation

As described earlier, CXA1296P can be used with either +5V single power supply or dual power supply (+5V or −5.2V).

Switching resistors and the jumper wires enables the usage of either power supplies. The following is a description of how to use the power supplies.

Jumper wires to switch for single or dual power supply

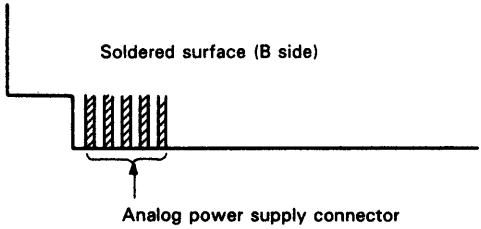


Resistors to switch for single or dual power supply

Fig. 3

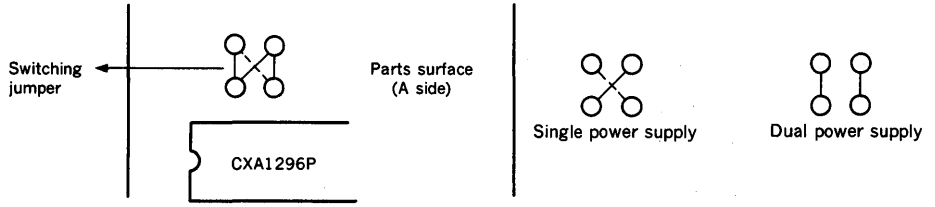
To switch on +5.0V single or +5.0V, −5.2V dual power supply, it is necessary to change the four resistors and jumper wires as well as the power supply fed from the edge connector.

1) Power supply fed from the edge connector



Supply +5.0V for AV_{CC} from the upper connector to use the +5V single power supply.
Supply −5.2V for AV_{EE} from the upper connector to use the dual power supply.

2) Jumper wires



Cross the Jumper wires to use the +5V single power supply. Hook the jumper wires in parallel to use the dual power supply.

3) Resistors

To switch single power or dual power supply, the four resistors (R8, R8'), (R9, R9'), (R12, R12') and (R13, R13') must be changed.

Before shipment from the factory, resistors are set as following for the single power supply.
R8=510Ω, R9=150Ω, R12=1.3kΩ, R13=100Ω

Change to the following to use dual power supply.
R8'=360Ω, R9'=300Ω, R12'=220kΩ, R13'=1.2kΩ

4) Capacitor

Polarity of the 35V/10μ tantalum capacitor at the lower right of the PCB is reversed to switch single power or dual power supply.

Notes on Use

- +5V Single power supply is set before shipment from the factory.
- Logic control input pin is open and kept at high level.
- For the single power supply, be sure to cross one of the jumper wires on the back to avoid a short circuit.
- GND V_{CC} is separated into analog and digital systems to avoid noise interference. Common usage of AGND and DGND as well as AV_{CC} and DV_{CC}, respectively, is recommended near the power supply to avoid an appreciable voltage difference between the two systems.

Output Code Table

M_{IN} V L_{IN} V	0 0	0 1	1 0	1 1
0 or +5V	111 • • • 11	100 • • • 00	011 • • • 11	000 • • 00
•	111 • • • 10	100 • • • 01	011 • • • 10	000 • • • 01
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
•	100 • • • 00	111 • • • 11	000 • • • 00	011 • • • 11
•	011 • • • 11	000 • • • 00	111 • • • 11	100 • • • 00
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
−2 or +3V	000 • • • 00	011 • • • 11	100 • • • 00	111 • • • 11

1 : V_{IH} V_{OH}
0 : V_{IL} V_{OL}

CXA1296P PCB Circuit Diagram (Single Power Supply)

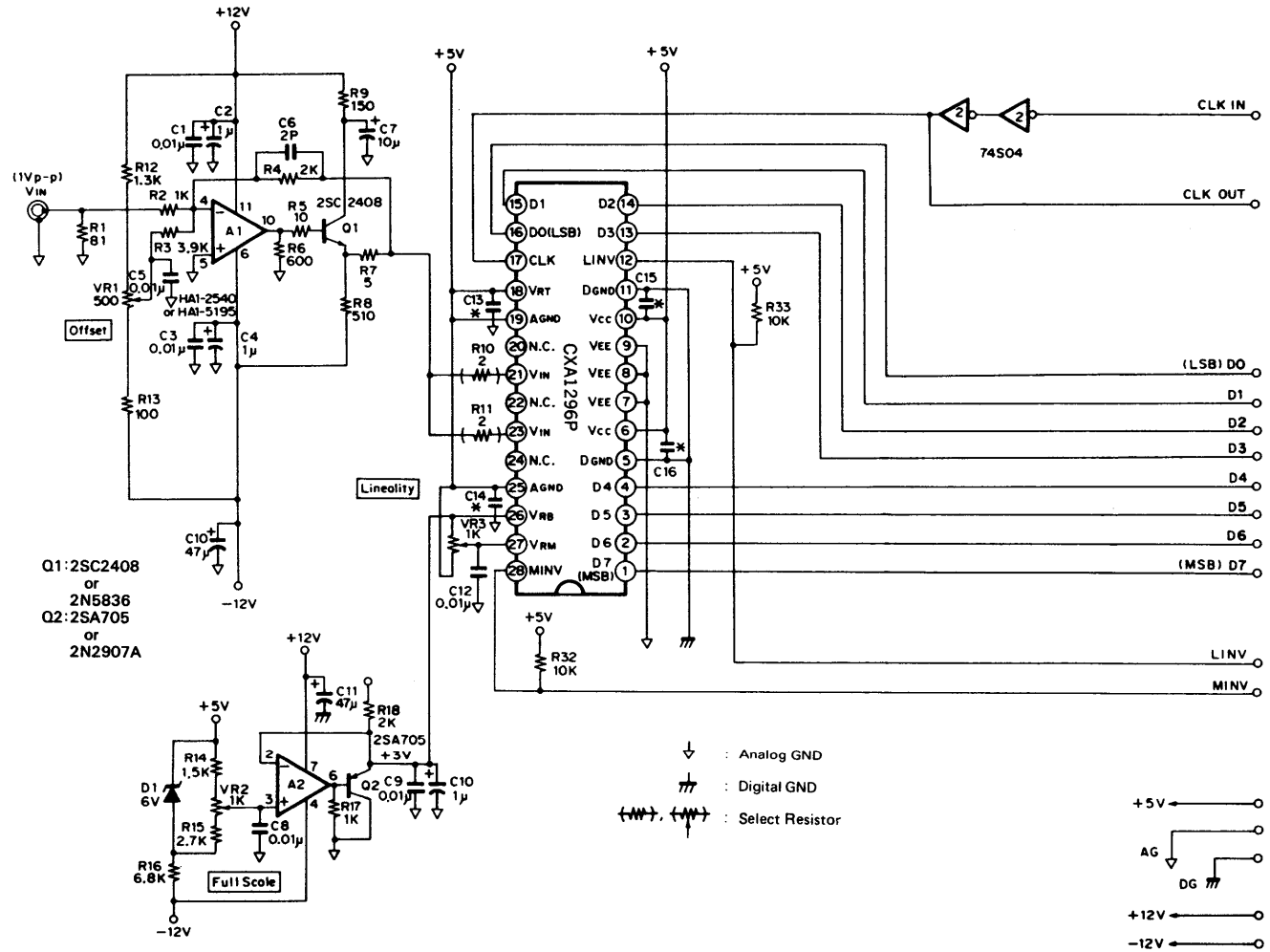


Fig. 4

CXA1296P PCB Circuit Diagram (Dual Power Supply)

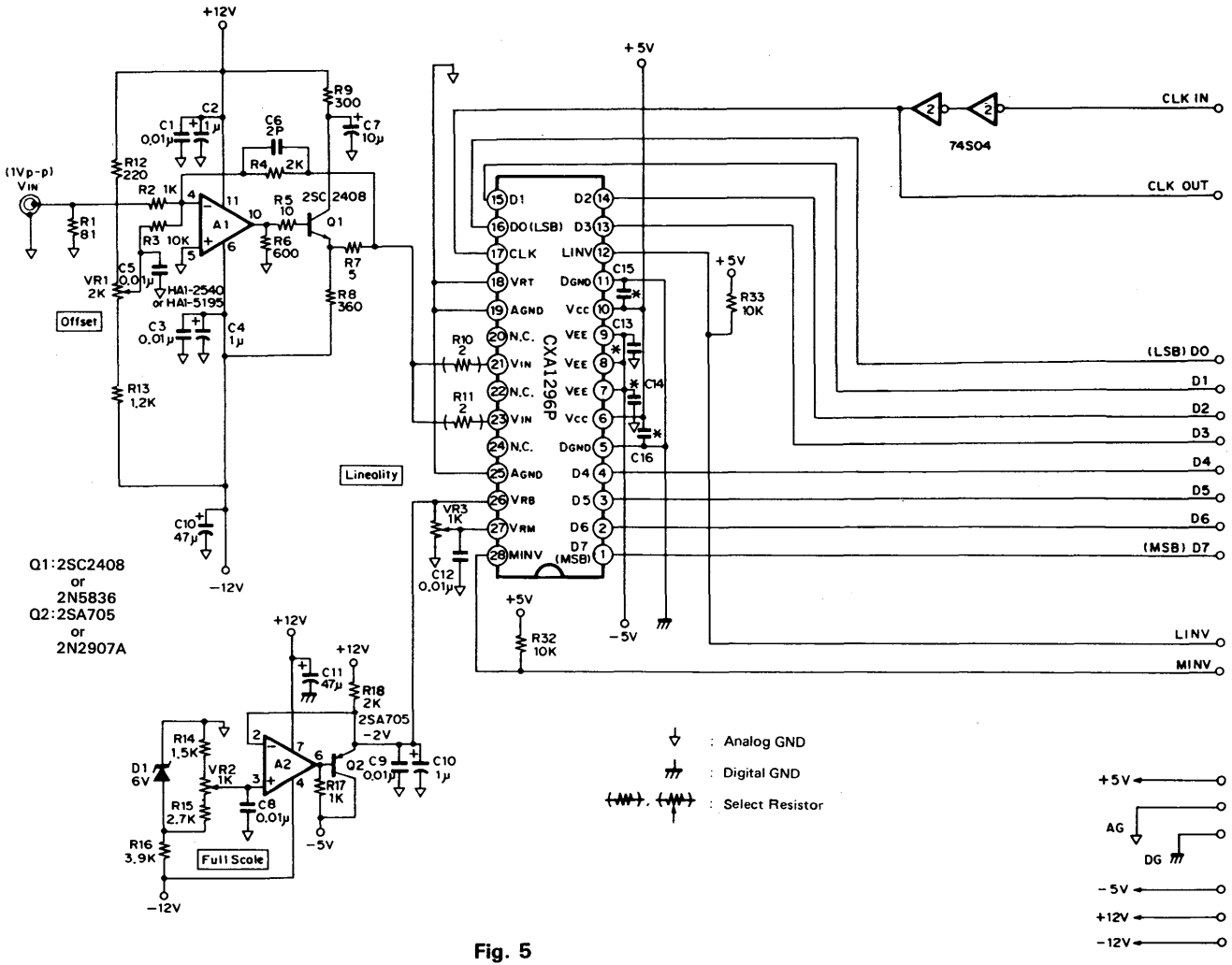
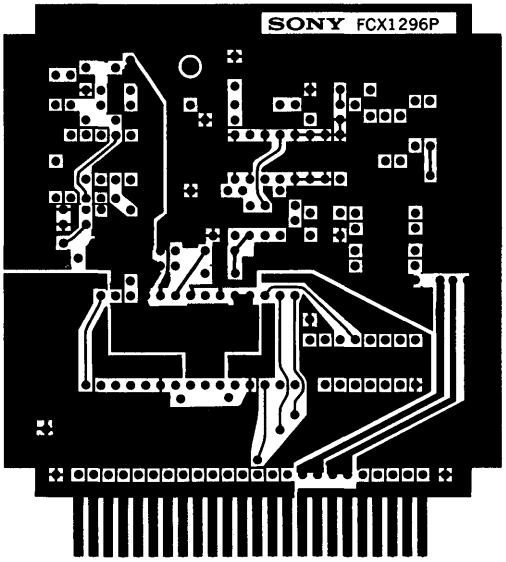
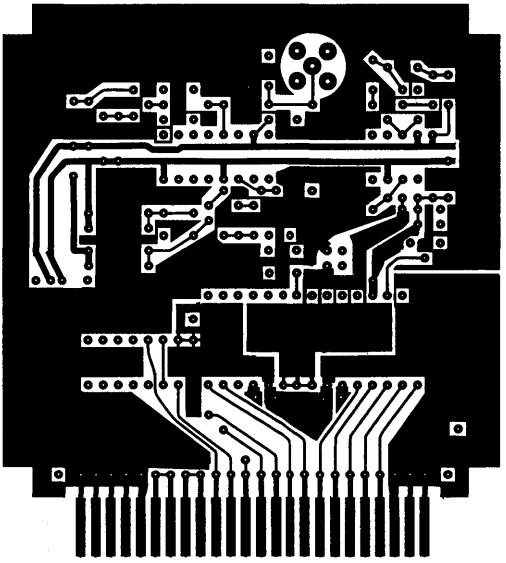


Fig. 5

CXA1296P PCB Pattern Diagram



Parts side
Fig. 6



Soldered side
Fig. 7

Silk Diagram

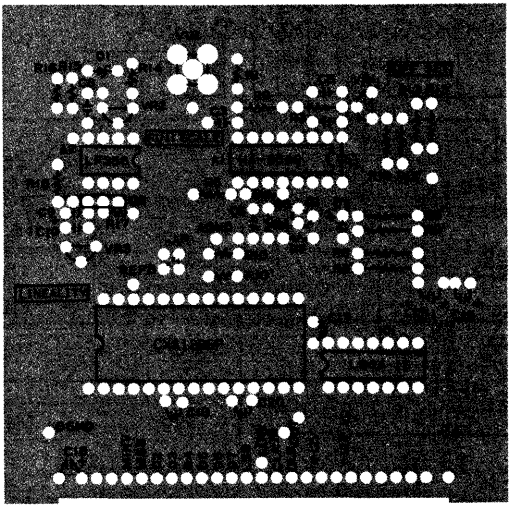
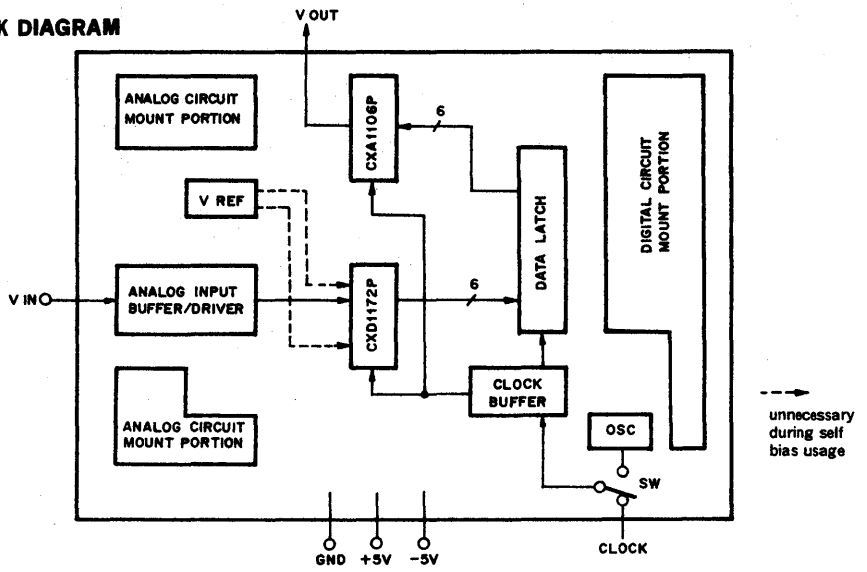


Fig. 8

6bit, 20 MSPS ADC and DAC Evaluation Board

CXD1172P/CXA1106P PCB is an evaluation PCB for the 6bit high speed low consumption CMOS A/D converter CXD1172P and the 8bit high speed bipolar D/A converter CXA1106P. This PCB features a high speed low consumption CMOS A/D converter, Analog input Buffer,clock Buffer, latch and high speed bipolar D/A converter designed to fully enhance the A/D and D/A converters performance.

BLOCK DIAGRAM



Characteristics

- Resolution 6bit
- Maximum conversion rate 20 MHz
- Digital input level TTL level
- Supply voltage ±5.0V

1. Supply voltage

Item	Min.	Typ.	Max.	Unit
+5V			150	mA
−5V			20	mA

2. Analog input

AC input voltage

Item	Min.	Typ.	Max.	Unit
Gain (V_{In}=1Vp-p input)	0.5		2	
offset voltage	0		5	V

3. Clock input

TTL compatible

Pulse width T_{CW1} 25ns(min)

T_{CW0} 25ns(min)

E89303A97-HP

4. Analog output (CXA1106)

Item	Min.	Typ.	Max.	Unit
Analog output	0.9	1.0	1.1	V

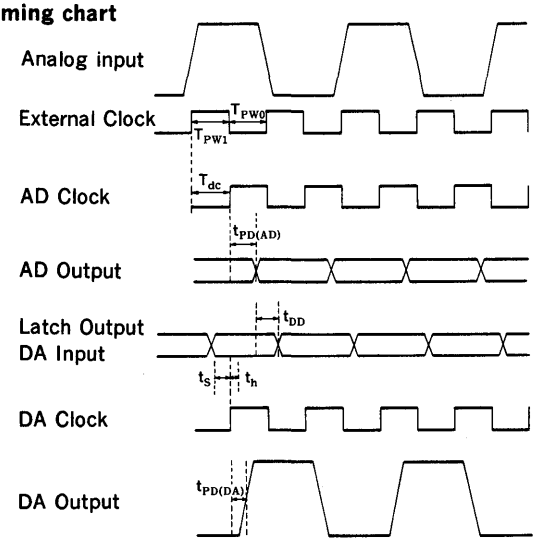
(R_L>10kΩ)

5. Output Format (CXD1172)

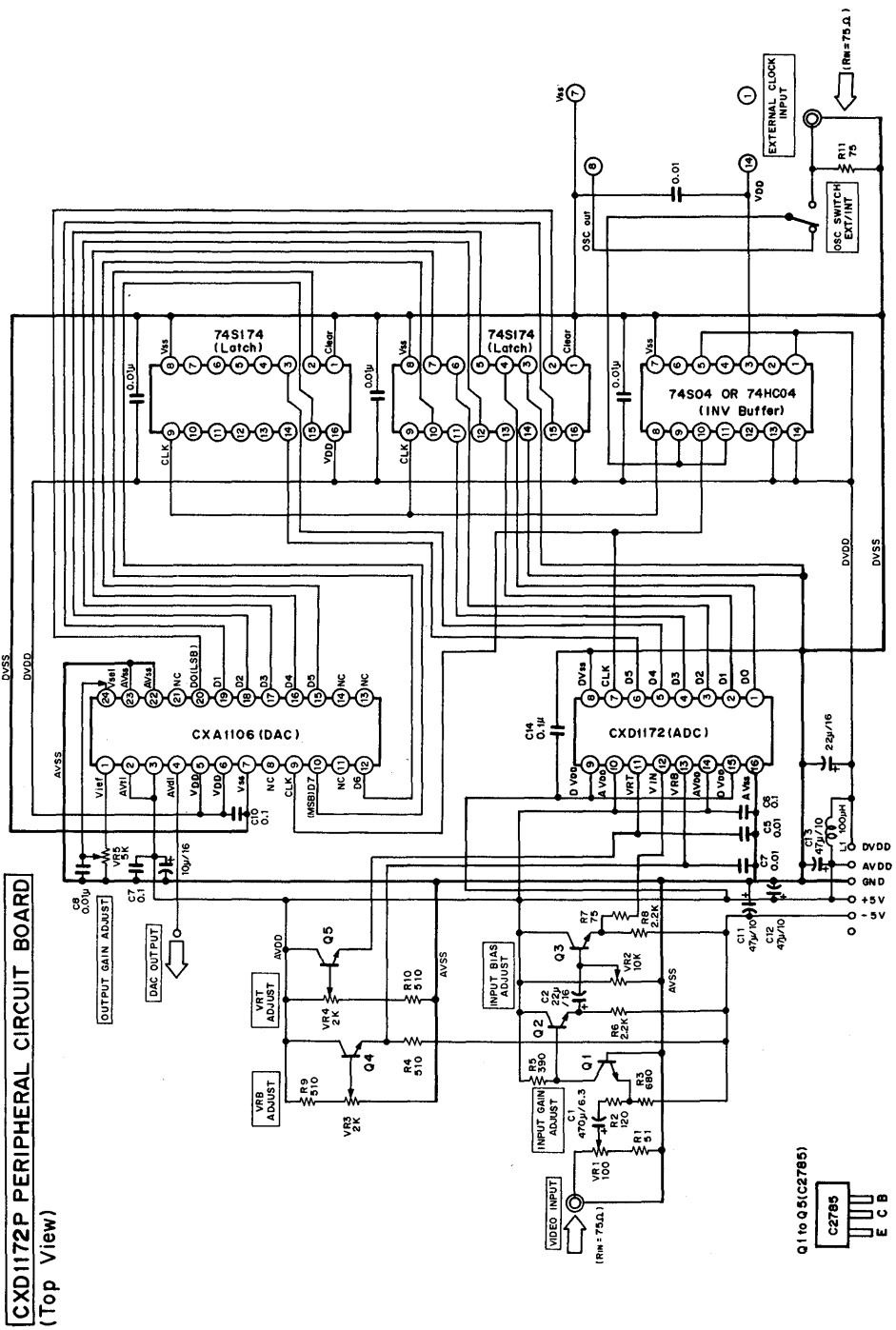
The table shows the output format of AD Converter

Analog input voltage	Step	digital output code MSB LSB
V_{RT}	0	1 1 1 1 1 1 1 1
	⋮	⋮
	127	1 0 0 0 0 0 0 0
	128	0 1 1 1 1 1 1 1
	⋮	⋮
V_{RB}	255	0 0 0 0 0 0 0 0

6. Timing chart



Item	Symbol	Min.	Typ.	Max.	Unit
Clock High time	T_{PW1}	25			ns
Clock Low time	T_{PW0}	25			ns
Clock Delay	T_{dc}			24	ns
Data delay AD	$t_{PD(AD)}$		18	30	ns
Data delay (latch)	t_{DD}			17	ns
Settling time	t_S	10			ns
Hold time	t_h	2			ns
Data delay DA	$t_{PD(DA)}$		11		ns



CXD1172P PERIPHERAL CIRCUIT BOARD
(Top View)

List of parts

resistance	
R1	51Ω
R2	150Ω
R3	680Ω
R4	510Ω
R5	390Ω
R6	2.2kΩ
R7	75Ω
R8	2.2kΩ
R9	510Ω
R10	510Ω
R11	75Ω
VR1	100Ω
VR2	10kΩ
VR3	2kΩ
VR4	2kΩ
VR5	5kΩ

capacitance	
C1	470μF/6.3V (chemical)
C2	22μF/16V(chemical)
C3	0.1μF
C4	10μF/16V(tamtalate)
C5	0.01μF
C6	0.1μF
C7	0.01μF
C8	0.01μF
C9	0.1μF
C10	0.1μF
C11	47μF/10V(chemical)
C12	47μF/10V(chemical)
C13	47μF/10V(chemical)
C14	0.1μF

transistor		
Q1	2SC2785	} (Equivalent to 2N5172)
Q2	2SC2785	
Q3	2SC2785	
Q4	2SC2785	} (Equivalent to 2N2222A)
Q5	2SC2785	

IC	
IC1	74S174
IC2	74S174
IC3	74S04

oscillator	
OSC	

inductance	
L1	470μH

others	
connector	BNC071
SW	AT1D2M3

Method of adjustment

1. Vgain adjustment (VR1)
   Adjustment of the analog input gain.

2. Voffset adjustment (VR2)
   Offset adjustment of the analog input

3. Vref adjustment (VR3, VR4)
   Adjustment of the AD converter reference voltage.
   VRB is adjusted at VR3 and VRT at VR4. Reference voltage is given by self bias when PCB is shipped from factory.

4. Adjustment of analog output gain (VR5)
   The full scale voltage of the DA converter output is adjusted.

Points on PCB pattern layout

1. Layout so that Digital current does not flow to analog GND (component ①). (For component ①: See P. 489 components side)

2. C6 capacitance (between AV_{SS} and AV_{DD}) and C14 capacitance (between DV_{SS} and DV_{DD}) are important factors to enhance CXD1172 performance. Those capacitances feature good high frequency characteristics over 0.1μF (ceramic capacitor). Layout them as close to the IC as possible.

3. Analog GND (AV_{SS}) and Digital GND (DV_{SS}) have a common voltage and supply source. ADC'S DV_{SS} (component ②) location as close to the voltage source as possible will give even better results. That is, a layout where ADC is close to the voltage source is recommended. (For component ②: See P.489 components side).

4. For AV_{DD} PINs (Pins 10, 14) and DV_{DD} PINs (Pins 9, 15) in CXD1172 adopt a common voltage source as for component ③. (See paragraph on latch up prevention) (For ③ See soldering side)

5. ADC samples analog signals at the clock falling edge. Accordingly, it is important that clocks fed to ADC not be affected by jitter.

6. Inductance L1 on the circuit chart serves to prevent Digital noise interference to Analog V_{DD} when the Analog and Digital systems have a common power supply.

7. In this PCB, to evaluate ADC and DAC independently, an independent layout has been adopted for the Analog GND of ADC and DAC, from the voltage generation source. For the user's actual PCB even a common source poses no problems. For CXA1106, as analog signals are output with the supply voltage as reference, care should be exercised not to let noise interfere with the DAC Analog V_{DD}.

Handling precautions

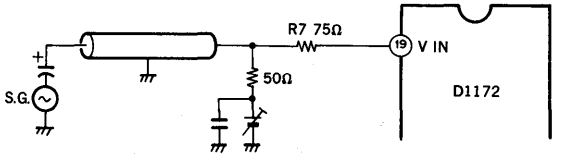
1. Clock input
   There are 2modes for the PCB clock input.
   1. Through an external signal generator. (external clock)
   2. Using a crystal oscillator, (Internal clock).

   The 2 modes can be selected through a switch on the PCB.
   At shipment an external clock is used.

2. Peripheral thru-holes
   There is a number of thru-holes at the Analog input, output and LOGIC areas. Those are to be used when additional circuits are to be mounted on the PCB circuit. Use when necessary.

3. The 2 Latch IC's (74S174) on the circuit chart are not absolutely necessary for ADC and DAC evaluation. Even if ADC output Data is directly input to DAC input, normal operation is maintained.

4. Analog input Buffer & Driver block is designed to handle usual Video band signals. Accordingly, for tests involving frequencies higher than that, methods shown in the Fig below, are recommended.



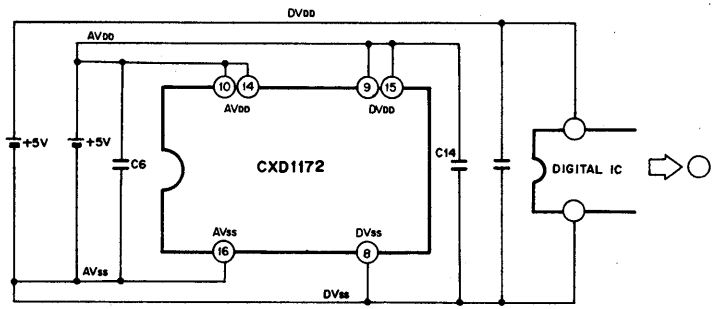
High frequency input test circuit

For latch up prevention

CXD1172 is a CMOS IC which requires latch up precautions. Latch up is mainly generated by the lag in the voltage rising time of AV_{DD} (Pins 10, 14) and DV_{DD} (Pins 9, 15), when power supply turns ON.

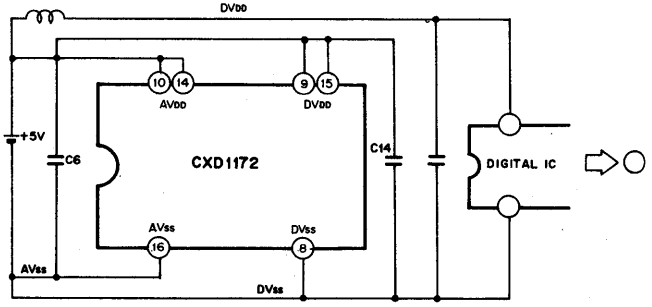
1. Correct usage

a. When Analog supply and Digital supply are from different sources.

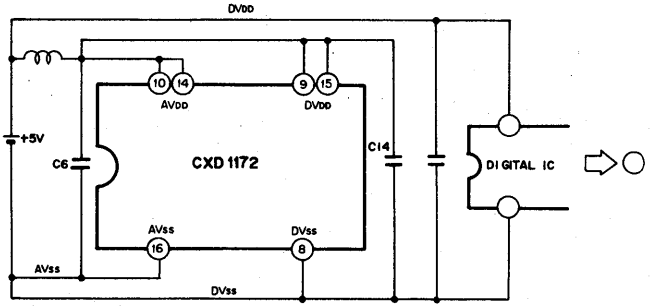


b. When Analog and Digital supply are from a common source.

(i)

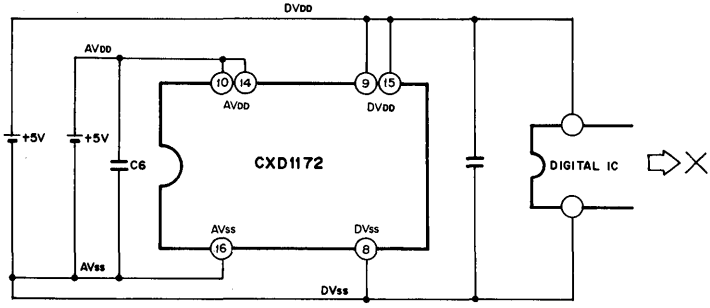


(ii)



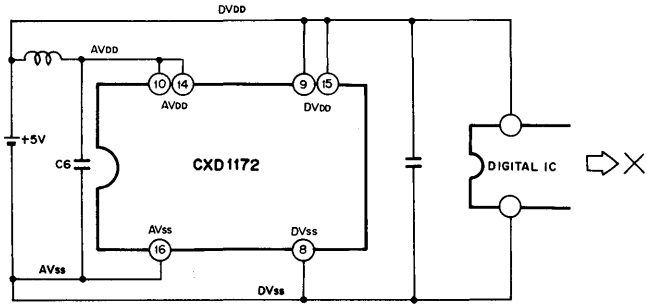
2. An example where latch up easily occurs.

a. When Analog and Digital supply are from different sources.

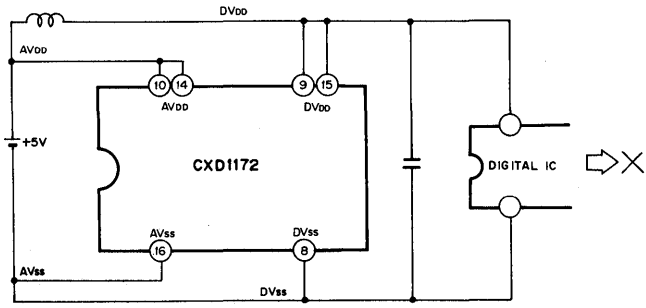


b. When Analog and Digital supply are from a common source.

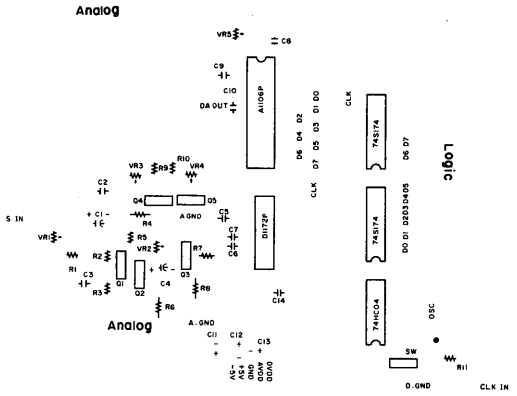
(i)



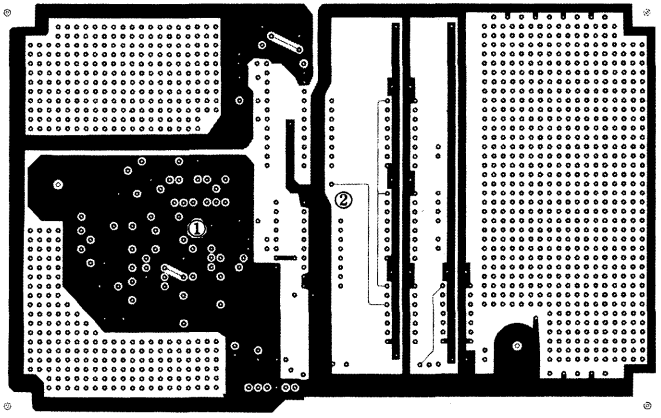
(ii)



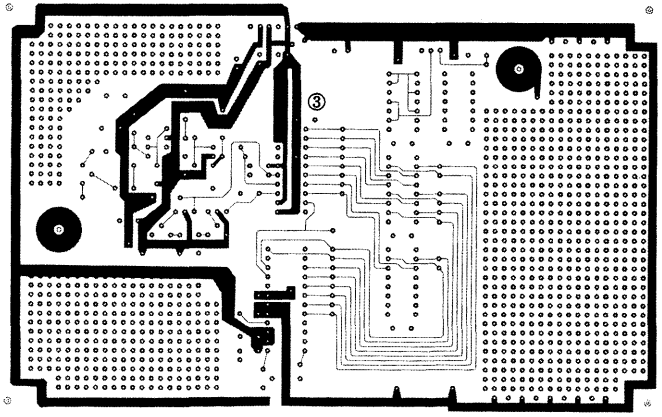
Silk Side



Component Side



Soldering Side

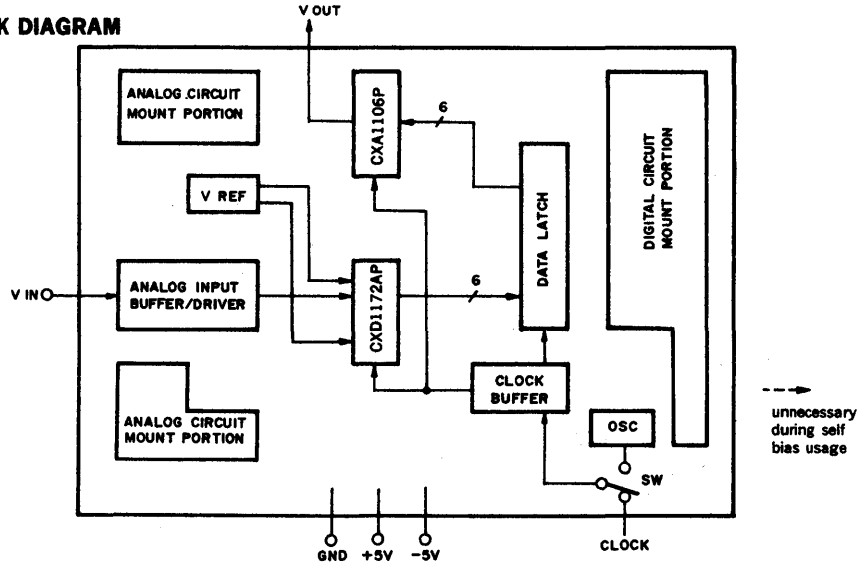


SONY CXD1172AP/CXA1106P PCB

6bit, 20 MSPS ADC and DAC Evaluation Board

CXD1172AP/CXA1106P PCB is an evaluation PCB for the 6bit high speed low consumption CMOS A/D converter CXD1172AP and the 8bit high speed bipolar D/A converter CXA1106P. This PCB features a high speed low consumption CMOS A/D converter, Analog input Buffer,clock Buffer, latch and high speed bipolar D/A converter designed to fully enhance the A/D and D/A converters performance.

BLOCK DIAGRAM



Characteristics

• Resolution	6bit
• Maximum conversion rate	20 MHz
• Digital input level	TTL level
• Supply voltage	±5.0V

1. Supply voltage

Item	Min.	Typ.	Max.	Unit
+5V			150	mA
−5V			20	mA

2. Analog input

AC input voltage

Item	Min.	Typ.	Max.	Unit
Gain (V_{in}=1Vp-p input)	0.5		2	
offset voltage	0		5	V

3. Clock input

TTL compatible

Pulse width T_{CW1} 25ns(min)

T_{CW0} 25ns(min)

E89803-HP

4. Analog output (CXA1106)

Item	Min.	Typ.	Max.	Unit
Analog output	0.9	1.0	1.1	V

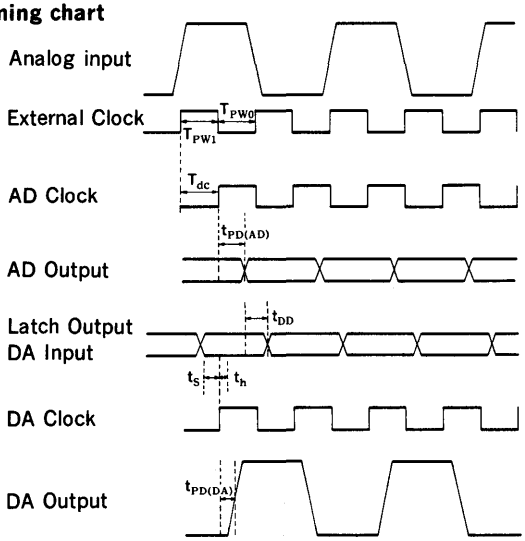
($R_L > 10k\Omega$)

5. Output Format (CXD1172A)

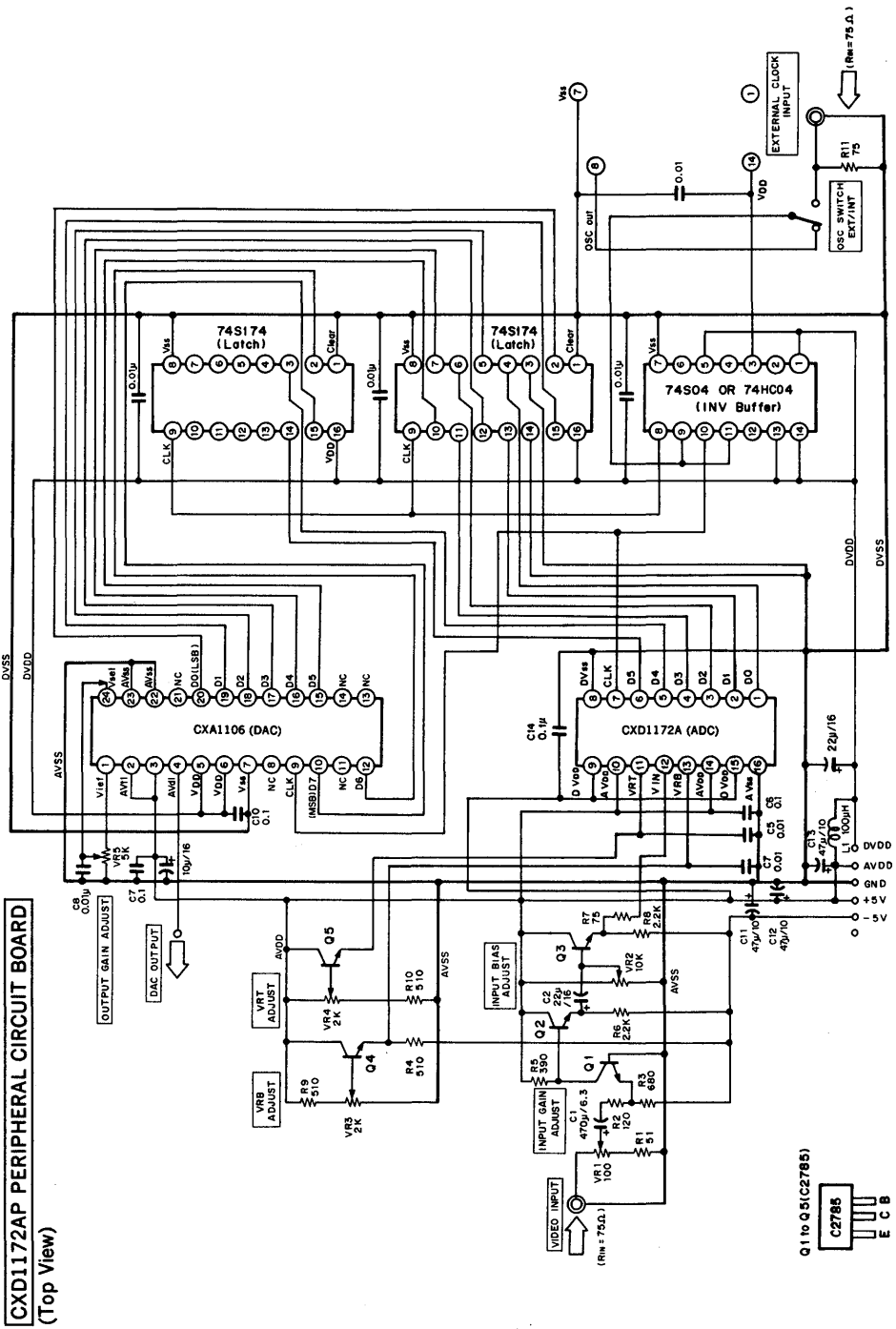
The table shows the output format of AD Converter

Analog input voltage	Step	digital output code MSB LSB
V_{RT}	0	1 1 1 1 1 1 1 1
	⋮	⋮
	127	1 0 0 0 0 0 0 0
	128	0 1 1 1 1 1 1 1
	⋮	⋮
V_{RB}	255	0 0 0 0 0 0 0 0

6. Timing chart



Item	Symbol	Min.	Typ.	Max.	Unit
Clock High time	T_{PW1}	25			ns
Clock Low time	T_{PW0}	25			ns
Clock Delay	T_{dc}			24	ns
Data delay AD	$t_{PD(AD)}$		18	30	ns
Data delay (latch)	t_{DD}			17	ns
Settling time	t_S	10			ns
Hold time	t_h	2			ns
Data delay DA	$t_{PD(DA)}$		11		ns



CXD1172AP PERIPHERAL CIRCUIT BOARD
(Top View)

List of parts

resistance	
R1	51Ω
R2	150Ω
R3	680Ω
R4	510Ω
R5	390Ω
R6	2.2kΩ
R7	75Ω
R8	2.2kΩ
R9	510Ω
R10	510Ω
R11	75Ω
VR1	100Ω
VR2	10kΩ
VR3	2kΩ
VR4	2kΩ
VR5	5kΩ

capacitance	
C1	470μF/6.3V (chemical)
C2	22μF/16V (chemical)
C3	0.1μF
C4	10μF/16V (tamtalate)
C5	0.01μF
C6	0.1μF
C7	0.01μF
C8	0.01μF
C9	0.1μF
C10	0.1μF
C11	47μF/10V (chemical)
C12	47μF/10V (chemical)
C13	47μF/10V (chemical)
C14	0.1μF

transistor		
Q1	2SC2785	} (Equivalent to 2N5172)
Q2	2SC2785	
Q3	2SC2785	
Q4	2SC2785	} (Equivalent to 2N2222A)
Q5	2SC2785	

IC	
IC1	74S174
IC2	74S174
IC3	74S04

oscillator	
OSC	

inductance	
L1	470μH

others	
connector	BNC071
SW	AT1D2M3

Method of adjustment

1. Vgain adjustment (VR1)
   Adjustment of the analog input gain.

2. Voffset adjustment (VR2)
   Offset adjustment of the analog input

3. Vref adjustment (VR3, VR4)
   Adjustment of the AD converter reference voltage.
   VRB is adjusted at VR3 and VRT at VR4. Reference voltage is given by self bias when PCB is shipped from factory.

4. Adjustment of analog output gain (VR5)
   The full scale voltage of the DA converter output is adjusted.

Points on PCB pattern layout

1. Layout so that Digital current does not flow to analog GND (component ①). (For component ①: See P. 497 components side)

2. C6 capacitance (between AV_{SS} and AV_{DD}) and C14 capacitance (between DV_{SS} and DV_{DD}) are important factors to enhance CXD1172A performance. Those capacitances feature good high frequency characteristics over 0.1μF (ceramic capacitor). Layout them as close to the IC as possible.

3. Analog GND (AV_{SS}) and Digital GND (DV_{SS}) have a common voltage and supply source. ADC'S DV_{SS} (component ②) location as close to the voltage source as possible will give even better results. That is, a layout where ADC is close to the voltage source is recommended. (For component ②: See P. 497 components side).

4. For AV_{DD} PINs (Pins 10, 14) and DV_{DD} PINs (Pins 9, 15) in CXD1172A adopt a common voltage source as for component ③. (See paragraph on latch up prevention) (For ③ See soldering side)

5. ADC samples analog signals at the clock falling edge. Accordingly, it is important that clocks fed to ADC not be affected by jitter.

6. Inductance L1 on the circuit chart serves to prevent Digital noise interference to Analog V_{DD} when the Analog and Digital systems have a common power supply.

7. In this PCB, to evaluate ADC and DAC independently, an independent layout has been adopted for the Analog GND of ADC and DAC, from the voltage generation source. For the user's actual PCB even a common source poses no problems. For CXA1106, as analog signals are output with the supply voltage as reference, care should be exercised not to let noise interfere with the DAC Analog V_{DD}.

Handling precautions

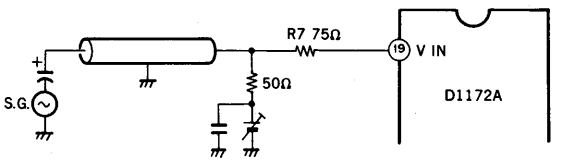
1. Clock input
   There are 2modes for the PCB clock input.
   1. Through an external signal generator. (external clock)
   2. Using a crystal oscillator, (Internal clock).

   The 2 modes can be selected through a switch on the PCB.
   At shipment an external clock is used.

2. Peripheral thru-holes
   There is a number of thru-holes at the Analog input, output and LOGIC areas. Those are to be used when additional circuits are to be mounted on the PCB circuit. Use when necessary.

3. The 2 Latch IC's (74S174) on the circuit chart are not absolutely necessary for ADC and DAC evaluation. Even if ADC output Data is directly input to DAC input, normal operation is maintained.

4. Analog input Buffer & Driver block is designed to handle usual Video band signals. Accordingly, for tests involving frequencies higher than that, methods shown in the Fig below, are recommended.



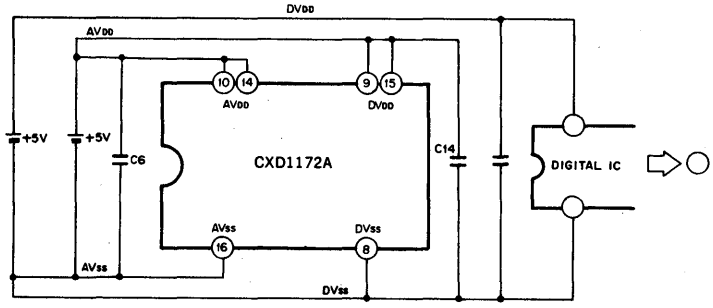
High frequency input test circuit

For latch up prevention

CXD1172A is a CMOS IC which requires latch up precautions. Latch up is mainly generated by the lag in the voltage rising time of AV_{DD} (Pins 10, 14) and DV_{DD} (Pins 9, 15), when power supply turns ON.

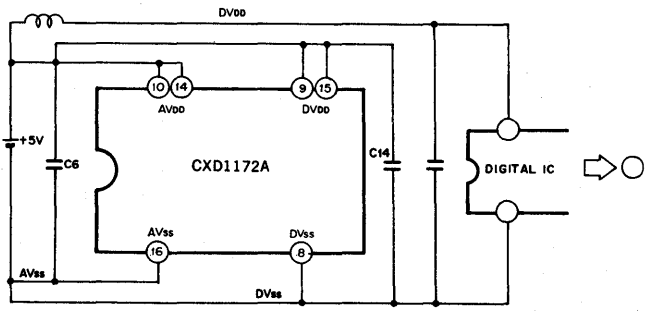
1. Correct usage

a. When Analog supply and Digital supply are from different sources.

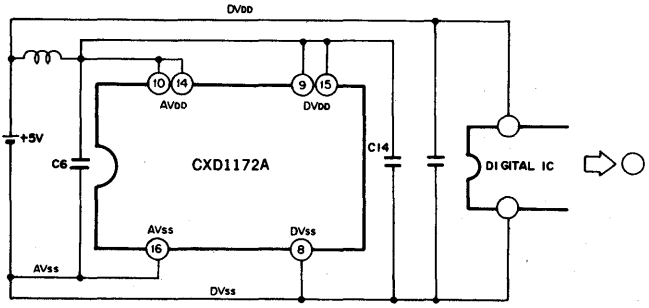


b. When Analog and Digital supply are from a common source.

(i)

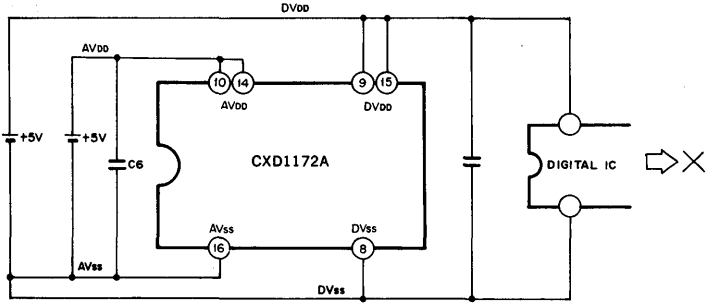


(ii)



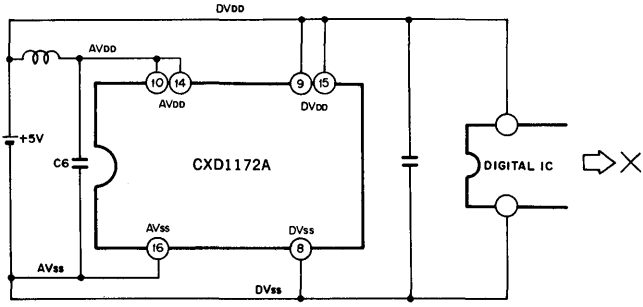
2. An example where latch up easily occurs.

a. When Analog and Digital supply are from different sources.

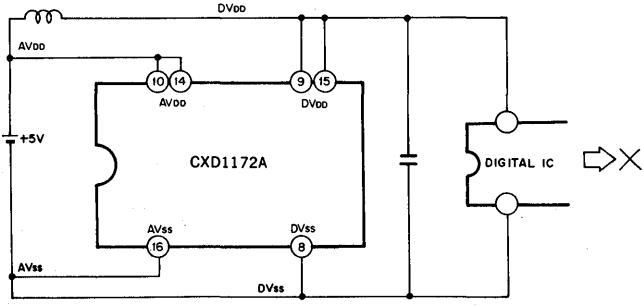


b. When Analog and Digital supply are from a common source.

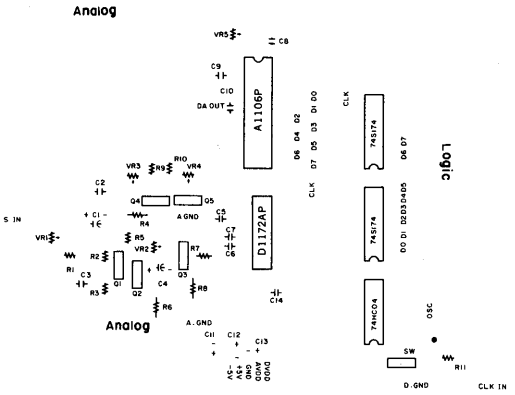
(i)



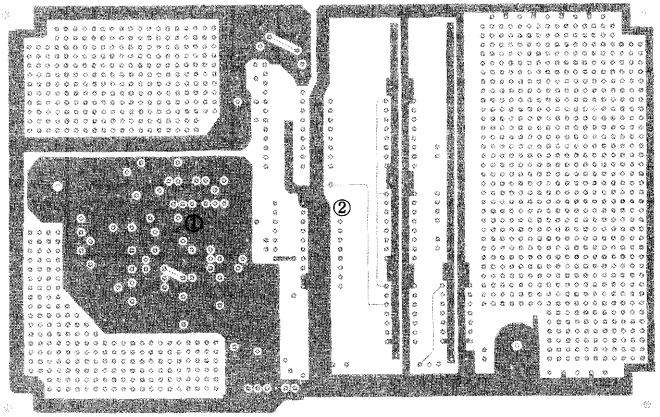
(ii)



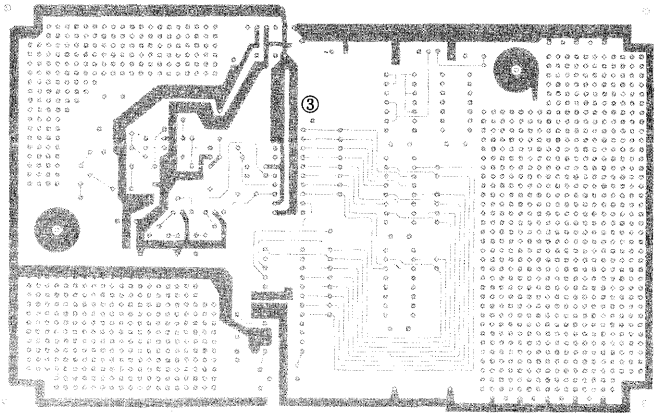
Silk Side



Component Side



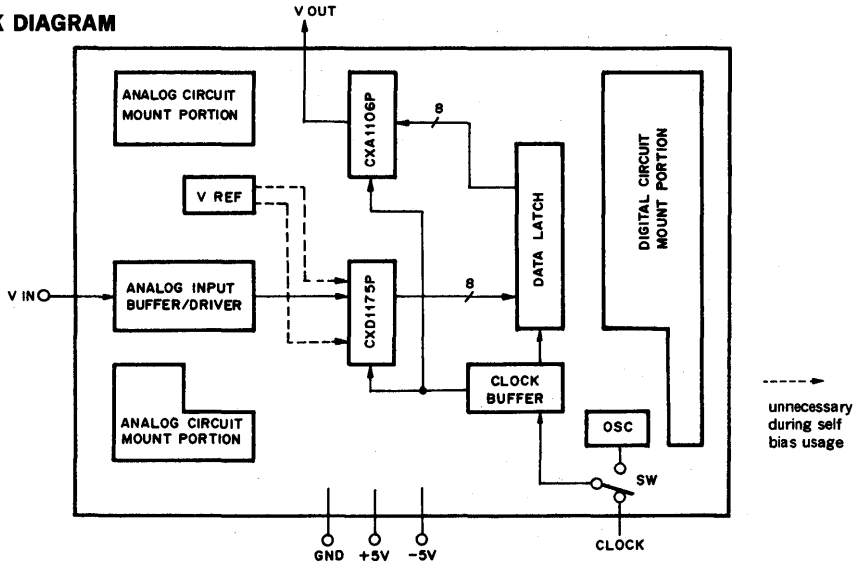
Soldering Side



8bit, 20 MSPS ADC and DAC Evaluation Board

CXD1175P/CXA1106P PCB is an evaluation PCB for the 8bit high speed low consumption CMOS A/D converter CXD1175P and the 8bit high speed bipolar D/A converter CXA1106P. This PCB features a high speed low consumption CMOS A/D converter, Analog input Buffer,clock Buffer, latch and high speed bipolar D/A converter designed to fully enhance the A/D and D/A converters performance.

BLOCK DIAGRAM



Characteristics

• Resolution	8bit
• Maximum conversion rate	20 MHz
• Digital input level	TTL level
• Supply voltage	±5.0V

1. Supply voltage

Item	Min.	Typ.	Max.	Unit
+5V			150	mA
−5V			20	mA

2. Analog input

AC input voltage

Item	Min.	Typ.	Max.	Unit
Gain (V_{in}=2Vp-p input)	0.5		2	
offset voltage	0		5	V

3. Clock input

TTL compatible

Pulse width T_{CW1} 25ns(min)

T_{CW0} 25ns(min)

E89226A97-HP

4. Analog output (CXA1106)

Item	Min.	Typ.	Max.	Unit
Analog output	0.9	1.0	1.1	V

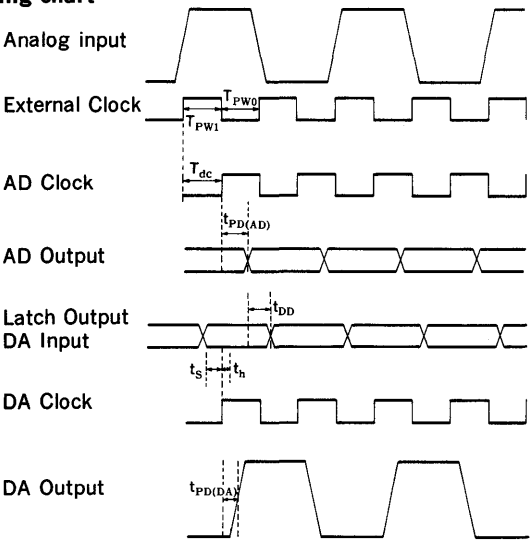
(R_L >10kΩ)

5. Output Format (CXD1175)

The table shows the output format of AD Converter

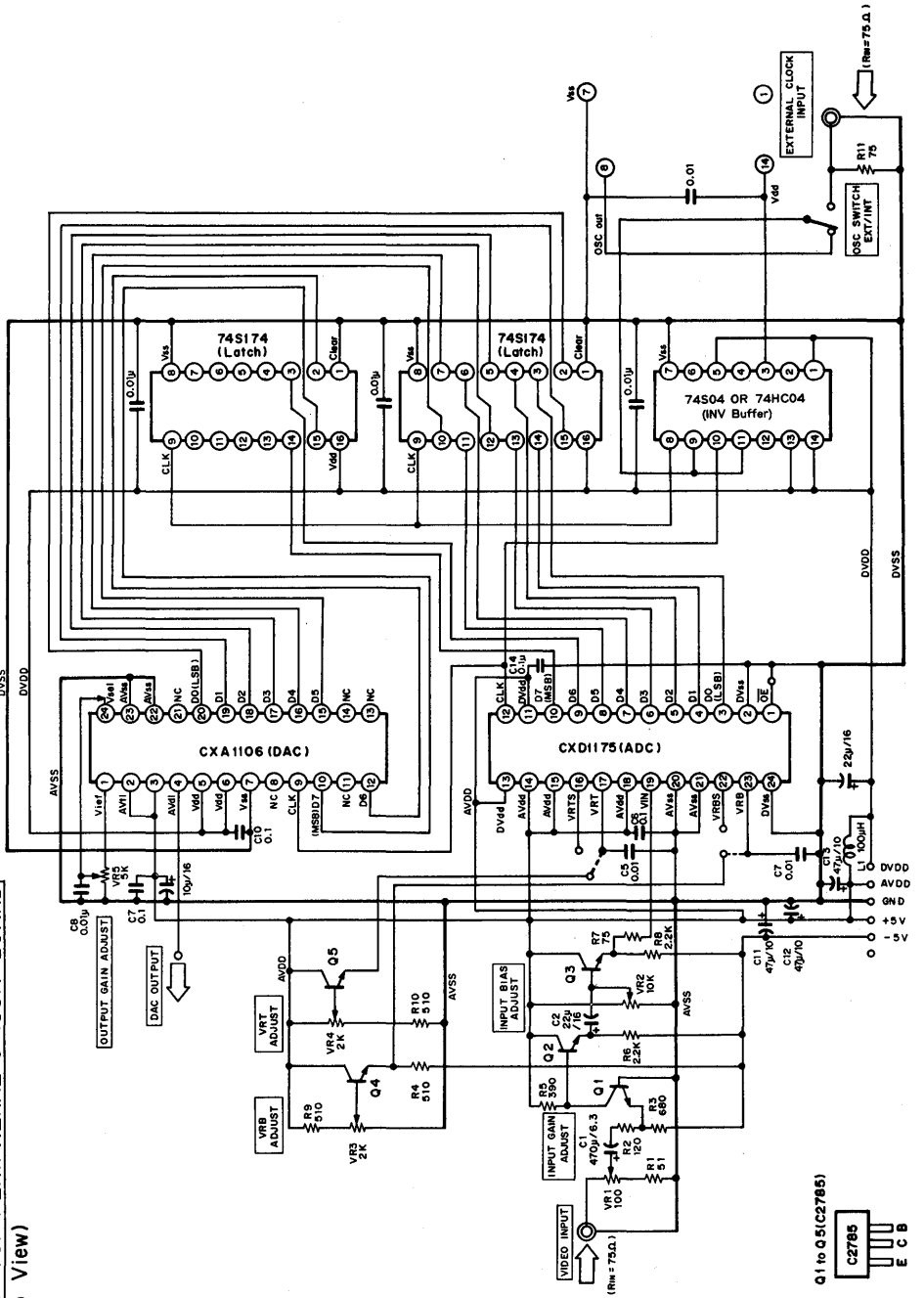
Analog input voltage	Step	digital output code MSB LSB
V_{RT}	0	1 1 1 1 1 1 1 1
	⋮	⋮
	127	1 0 0 0 0 0 0 0
	128	0 1 1 1 1 1 1 1
	⋮	⋮
V_{RB}	255	0 0 0 0 0 0 0 0

6. Timing chart



Item	Symbol	Min.	Typ.	Max.	Unit
Clock High time	T_{PW1}	25			ns
Clock Low time	T_{PW0}	25			ns
Clock Delay	T_{dc}			24	ns
Data delay AD	$t_{PD(AD)}$		18	30	ns
Data delay (latch)	t_{DD}			17	ns
Settling time	t_S	10			ns
Hold time	t_h	2			ns
Data delay DA	$t_{PD(DA)}$		11		ns

CXD1175P PERIPHERAL CIRCUIT BOARD
(Top View)



List of parts

resistance	
R1	51Ω
R2	150Ω
R3	680Ω
R4	510Ω
R5	390Ω
R6	2.2kΩ
R7	75Ω
R8	2.2kΩ
R9	510Ω
R10	510Ω
R11	75Ω
VR1	100Ω
VR2	10kΩ
VR3	2kΩ
VR4	2kΩ
VR5	5kΩ

capacitance	
C1	470μF/6.3V (chemical)
C2	22μF/16V (chemical)
C3	0.1μF
C4	10μF/16V (tamtalate)
C5	0.01μF
C6	0.1μF
C7	0.01μF
C8	0.01μF
C9	0.1μF
C10	0.1μF
C11	47μF/10V (chemical)
C12	47μF/10V (chemical)
C13	47μF/10V (chemical)
C14	0.1μF

transistor		
Q1	2SC2785	(Equivalent to 2N5172)
Q2	2SC2785	
Q3	2SC2785	
Q4	2SC2785	(Equivalent to 2N2222A)
Q5	2SC2785	

IC	
IC1	74S174
IC2	74S174
IC3	74S04

oscillator	
OSC	

inductance	
L1	470μH

others	
connector	BNC071
SW	AT1D2M3

Method of adjustment

1. Vgain adjustment (VR1)
   Adjustment of the analog input gain.

2. Voffset adjustment (VR2)
   Offset adjustment of the analog input

3. Vref adjustment (VR3, VR4)
   Adjustment of the AD converter reference voltage.
   VRB is adjusted at VR3 and VRT at VR4. Reference voltage is given by self bias when PCB is shipped from factory.

4. Adjustment of analog output gain (VR5)
   The full scale voltage of the DA converter output is adjusted.

Points on PCB pattern layout

1. Layout so that Digital current does not flow to analog GND (component ①). (For component ①: See P. 505 components side)

2. C6 capacitance (between AV_{SS} and AV_{DD}) and C14 capacitance (between DV_{SS} and DV_{DD}) are important factors to enhance CXD1175 performance. Those capacitances feature good high frequency characteristics over 0.1μF (ceramic capacitor). Layout them as close to the IC as possible.

3. Analog GND (AV_{SS}) and Digital GND (DV_{SS}) have a common voltage and supply source. ADC'S DV_{SS} (component ②) location as close to the voltage source as possible will give even better results. That is, a layout where ADC is close to the voltage source is recommended. (For component ②: See P. 505 components side).

4. For AV_{DD} PINs (Pins 14, 15, 18) and DV_{DD} PINs (Pins 11, 13) in CXD1175 adopt a common voltage source as for component ③. (See paragraph on latch up prevention) (For ③ See P. 505 soldering side).

5. ADC samples analog signals at the clock falling edge. Accordingly, it is important that clocks fed to ADC not be affected by jitter.

6. Inductance L1 on the circuit chart serves to prevent Digital noise interference to Analog V_{DD} when the Analog and Digital systems have a common power supply.

7. In this PCB, to evaluate ADC and DAC independently, an independent layout has been adopted for the Analog GND of ADC and DAC, from the voltage generation source. For the user's actual PCB even a common source poses no problems. For CXA1106, as analog signals are output with the supply voltage as reference, care should be exercised not to let noise interfere with the DAC Analog V_{DD}.

Handling precautions

1. Reference voltage
   By shorting V_{RT} and V_{RTS} V_{RB} and V_{RBS} in CXD1175P a self bias function is available where $V_{RT}=2.6V$ and $V_{RB}=0.6V$. At the PCB either self bias or external reference voltage may be selected according to the way the jumper wire is connected. At the shipment, the reference voltage is provided by the self bias. Also, when reference voltage is to be provided from the exterior, adjust the dynamic range ($V_{RT}-V_{RB}$) to 1.8Vp-p or over.

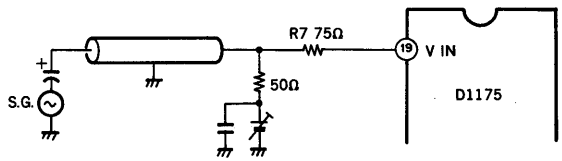
2. Clock input
   There are 2modes for the PCB clock input.
   1. Through an external signal generator. (external clock)
   2. Using a crystal oscillator, (Internal clock).

   The 2 modes can be selected through a switch on the PCB.
   At shipment an external clock is used.

3. Peripheral thru-holes
   There is a number of thru-holes at the Analog input, output and LOGIC areas. Those are to be used when additional circuits are to be mounted on the PCB circuit. Use when necessary.

4. The 2 Latch IC's (74S174) on the circuit chart are not absolutely necessary for ADC and DAC evaluation. Even if ADC output Data is directly input to DAC input, normal operation is maintained.

5. Analog input Buffer & Driver block is designed to handle usual Video band signals. Accordingly, for tests involving frequencies higher than that, methods shown in the Fig below, are recommended.



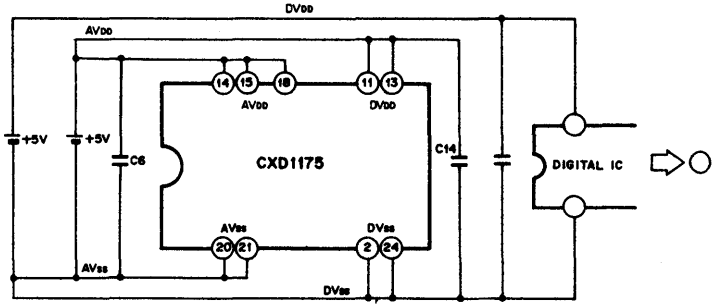
High frequency input test circuit

For latch up prevention

CXD1175 is a CMOS IC which requires latch up precautions. Latch up is mainly generated by the lag in the voltage rising time of AV_{DD} (Pins 14, 15, 18) and DV_{DD} (Pins 11, 13), when power supply turns ON.

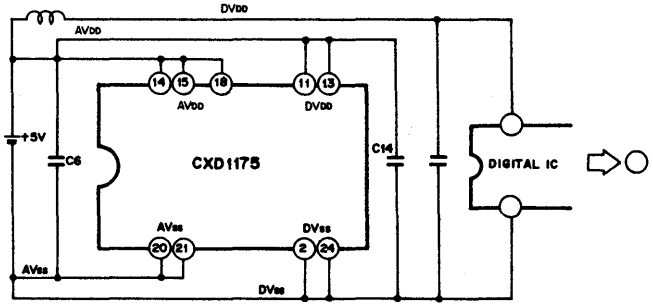
1. Correct usage

a. When Analog supply and Digital supply are from different sources.

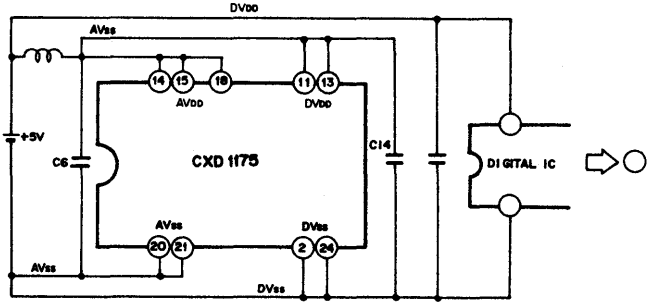


b. When Analog and Digital supply are from a common source.

(i)

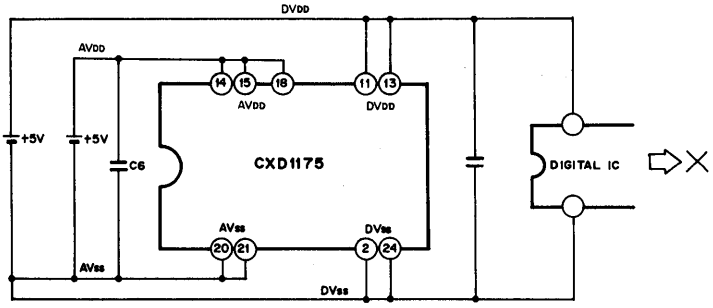


(ii)



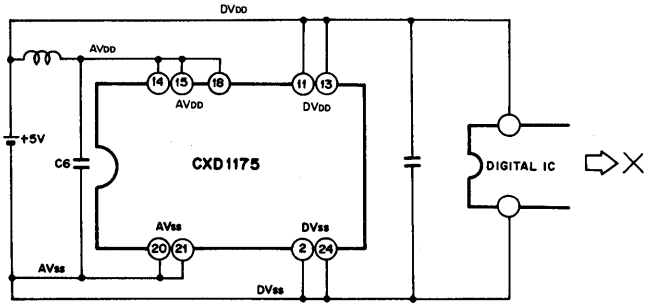
2. An example where latch up easily occurs.

a. When Analog and Digital supply are from different sources.

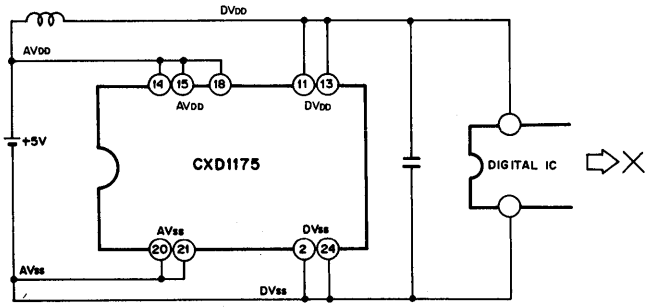


b. When Analog and Digital supply are from a common source.

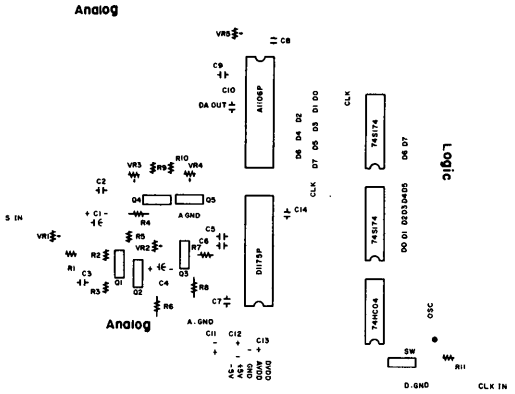
(i)



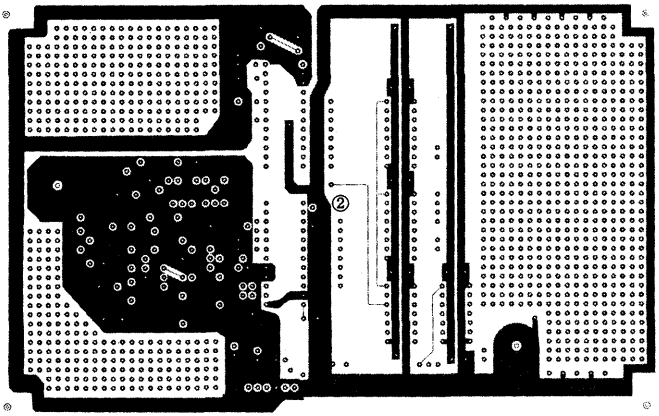
(ii)



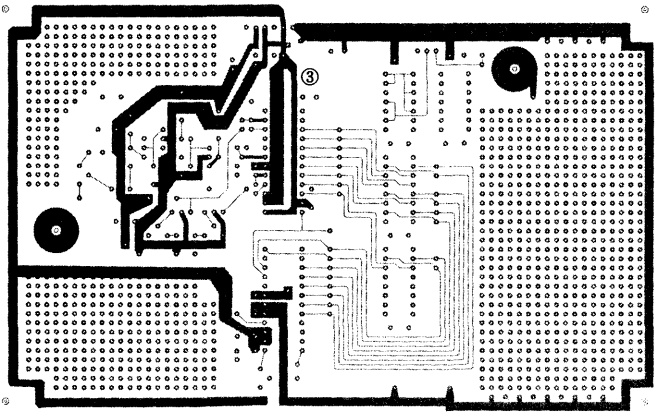
Silk Side



Component Side



Soldering Side

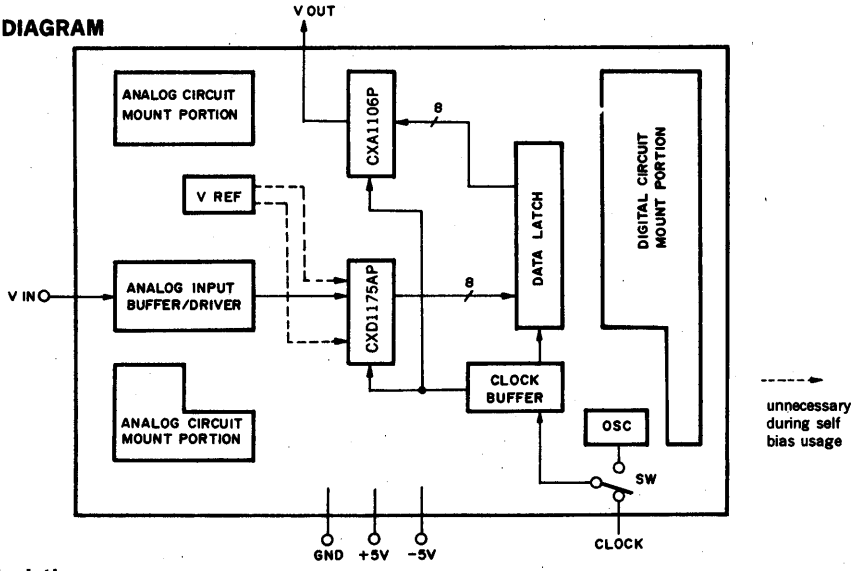


SONY CXD1175AP/CXA1106P PCB

8bit, 20 MSPS ADC and DAC Evaluation Board

CXD1175AP/CXA1106P PCB is an evaluation PCB for the 8bit high speed low consumption CMOS A/D converter CXD1175AP and the 8bit high speed bipolar D/A converter CXA1106P. This PCB features a high speed low consumption CMOS A/D converter, Analog input Buffer,clock Buffer, latch and high speed bipolar D/A converter designed to fully enhance the A/D and D/A converters performance.

BLOCK DIAGRAM



Characteristics

• Resolution	8bit
• Maximum conversion rate	20 MHz
• Digital input level	TTL level
• Supply voltage	±5.0V

1. Supply voltage

Item	Min.	Typ.	Max.	Unit
+5V			150	mA
−5V			20	mA

2. Analog input

AC input voltage

Item	Min.	Typ.	Max.	Unit
Gain (V_{in}=2Vp-p input)	0.5		2	
offset voltage	0		5	V

3. Clock input

TTL compatible

Pulse width T_{CW1} 25ns(min)

T_{CW0} 25ns(min)

E89804-HP

4. Analog output (CXA1106)

Item	Min.	Typ.	Max.	Unit
Analog output	0.9	1.0	1.1	V

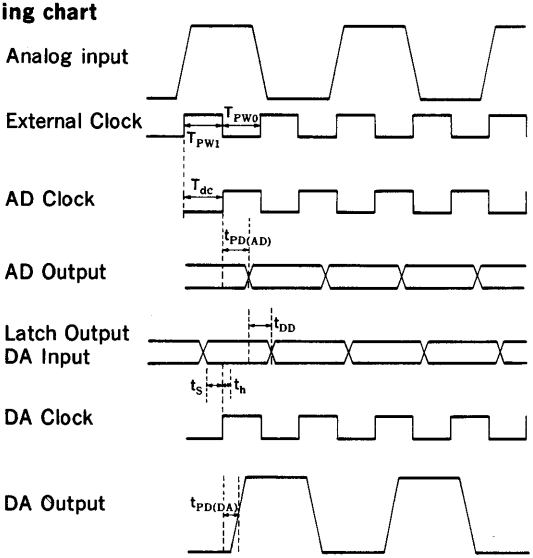
(R_L > 10kΩ)

5. Output Format (CXD1175A)

The table shows the output format of AD Converter

Analog input voltage	Step	digital output code MSB LSB
V_{RT}	0	1 1 1 1 1 1 1 1
	⋮	⋮
	127	1 0 0 0 0 0 0 0
	128	0 1 1 1 1 1 1 1
	⋮	⋮
V_{RB}	255	0 0 0 0 0 0 0 0

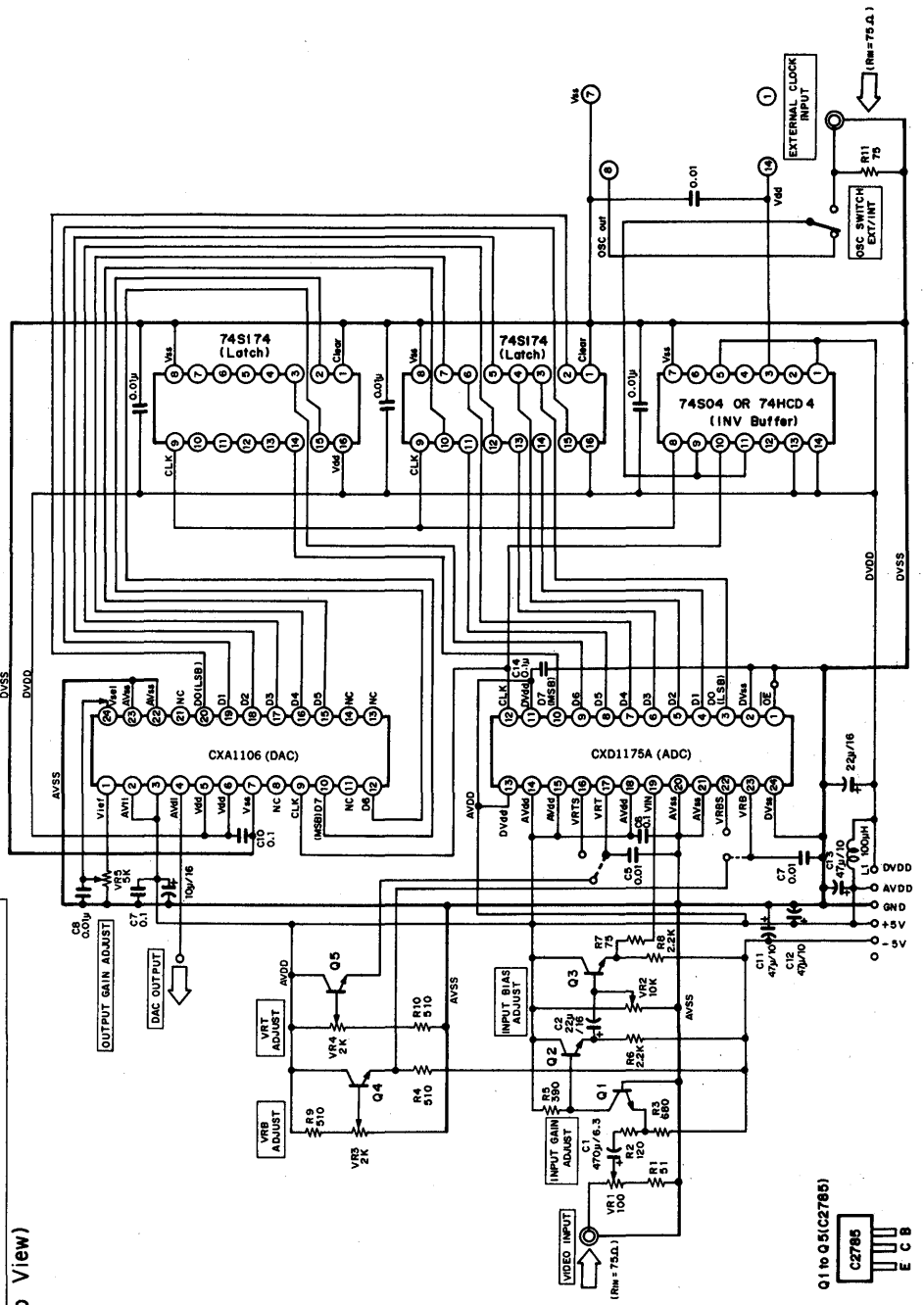
6. Timing chart



Item	Symbol	Min.	Typ.	Max.	Unit
Clock High time	T_{PW1}	25			ns
Clock Low time	T_{PW0}	25			ns
Clock Delay	T_{dc}			24	ns
Data delay AD	$t_{PD(AD)}$		18	30	ns
Data delay (latch)	t_{DD}			17	ns
Settling time	t_S	10			ns
Hold time	t_h	2			ns
Data delay DA	$t_{PD(DA)}$		11		ns

CXD1175AP PERIPHERAL CIRCUIT BOARD

(Top View)



List of parts

resistance	
R1	51Ω
R2	150Ω
R3	680Ω
R4	510Ω
R5	390Ω
R6	2.2kΩ
R7	75Ω
R8	2.2kΩ
R9	510Ω
R10	510Ω
R11	75Ω
VR1	100Ω
VR2	10kΩ
VR3	2kΩ
VR4	2kΩ
VR5	5kΩ

capacitance	
C1	470μF/6.3V (chemical)
C2	22μF/16V(chemical)
C3	0.1μF
C4	10μF/16V(tamtalate)
C5	0.01μF
C6	0.1μF
C7	0.01μF
C8	0.01μF
C9	0.1μF
C10	0.1μF
C11	47μF/10V(chemical)
C12	47μF/10V(chemical)
C13	47μF/10V(chemical)
C14	0.1μF

transistor		
Q1	2SC2785	} (Equivalent to 2N5172)
Q2	2SC2785	
Q3	2SC2785	
Q4	2SC2785	} (Equivalent to 2N2222A)
Q5	2SC2785	

IC	
IC1	74S174
IC2	74S174
IC3	74S04

oscillator	
OSC	

inductance	
L1	470μH

others	
connector	BNC071
SW	AT1D2M3

Method of adjustment

1. Vgain adjustment (VR1)
   Adjustment of the analog input gain.

2. Voffset adjustment (VR2)
   Offset adjustment of the analog input

3. Vref adjustment (VR3, VR4)
   Adjustment of the AD converter reference voltage.
   VRB is adjusted at VR3 and VRT at VR4. Reference voltage is given by self bias when PCB is shipped from factory.

4. Adjustment of analog output gain (VR5)
   The full scale voltage of the DA converter output is adjusted.

Points on PCB pattern layout

1. Layout so that Digital current does not flow to analog GND (component ①). (For component ①: See P. 513 components side)

2. C6 capacitance (between AV_{SS} and AV_{DD}) and C14 capacitance (between DV_{SS} and DV_{DD}) are important factors to enhance CXD1175A performance. Those capacitances feature good high frequency characteristics over 0.1μF (ceramic capacitor). Layout them as close to the IC as possible.

3. Analog GND (AV_{SS}) and Digital GND (DV_{SS}) have a common voltage and supply source. ADC'S DV_{SS} (component ②) location as close to the voltage source as possible will give even better results. That is, a layout where ADC is close to the voltage source is recommended. (For component ②: See P. 513 components side).

4. For AV_{DD} PINs (Pins 14, 15, 18) and DV_{DD} PINs (Pins 11, 13) in CXD1175A adopt a common voltage source as for component ③. (See paragraph on latch up prevention) (For ③ See **P. 513 soldering side).**

5. ADC samples analog signals at the clock falling edge. Accordingly, it is important that clocks fed to ADC not be affected by jitter.

6. Inductance L1 on the circuit chart serves to prevent Digital noise interference to Analog V_{DD} when the Analog and Digital systems have a common power supply.

7. In this PCB, to evaluate ADC and DAC independently, an independent layout has been adopted for the Analog GND of ADC and DAC, from the voltage generation source. For the user's actual PCB even a common source poses no problems. For CXA1106, as analog signals are output with the supply voltage as reference, care should be exercised not to let noise interfere with the DAC Analog V_{DD}.

Handling precautions

1. Reference voltage

   By shorting V_{RT} and V_{RTS} V_{RB} and V_{RBS} in CXD1175A a self bias function is available where $V_{RT}=2.6V$ and $V_{RB}=0.6V$. At the PCB either self bias or external reference voltage may be selected according to the way the jumper wire is connected. At the shipment, the reference voltage is provided by the self bias. Also, when reference voltage is to be provided from the exterior, adjust the dynamic range ($V_{RT}-V_{RB}$) to 1.8Vp-p or over.

2. Clock input

   There are 2modes for the PCB clock input.

   1. Through an external signal generator. (external clock)
   2. Using a crystal oscillator, (Internal clock).

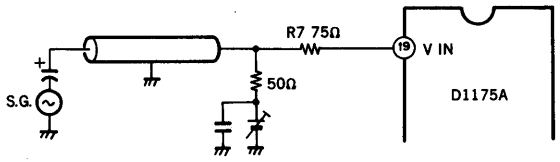
   The 2 modes can be selected through a switch on the PCB.
   At shipment an external clock is used.

3. Peripheral thru-holes

   There is a number of thru-holes at the Analog input, output and LOGIC areas. Those are to be used when additional circuits are to be mounted on the PCB circuit. Use when necessary.

4. The 2 Latch IC's (74S174) on the circuit chart are not absolutely necessary for ADC and DAC evaluation. Even if ADC output Data is directly input to DAC input, normal operation is maintained.

5. Analog input Buffer & Driver block is designed to handle usual Video band signals. Accordingly, for tests involving frequencies higher than that, methods shown in the Fig below, are recommended.



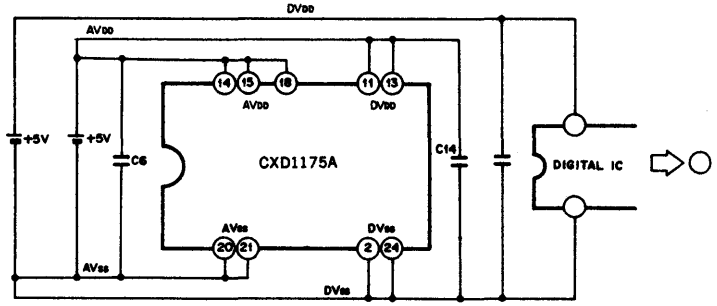
High frequency input test circuit

For latch up prevention

CXD1175A is a CMOS IC which requires latch up precautions. Latch up is mainly generated by the lag in the voltage rising time of AV_{DD} (Pins 14, 15, 18) and DV_{DD} (Pins 11, 13), when power supply turns ON.

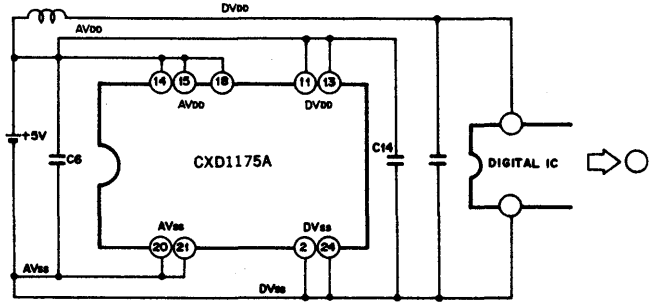
1. Correct usage

a. When Analog supply and Digital supply are from different sources.

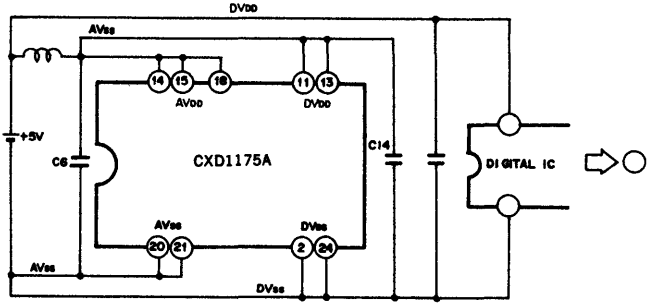


b. When Analog and Digital supply are from a common source.

(i)

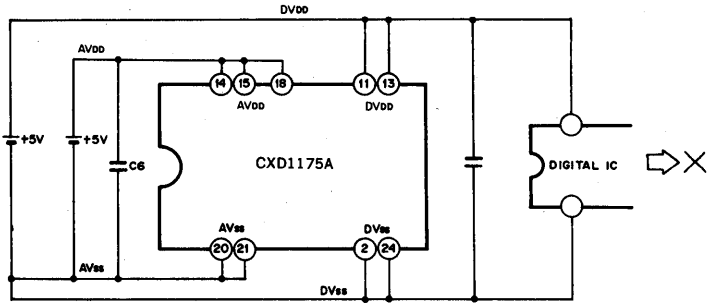


(ii)



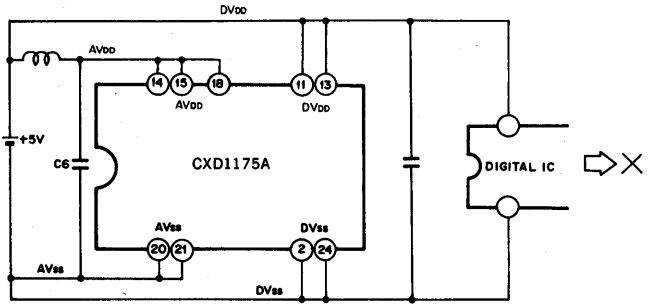
2. An example where latch up easily occurs.

a. When Analog and Digital supply are from different sources.

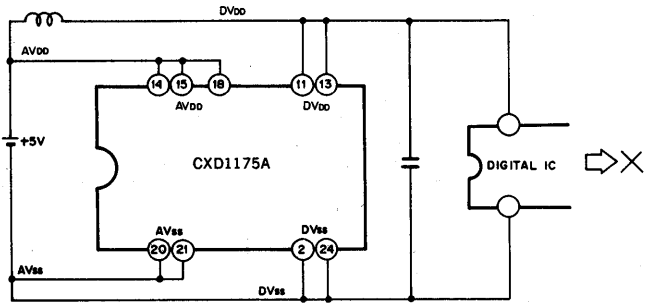


b. When Analog and Digital supply are from a common source.

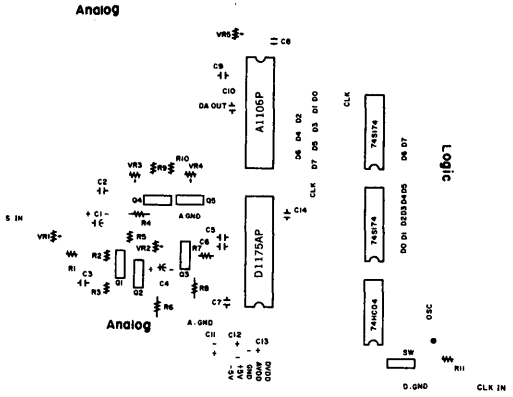
(i)



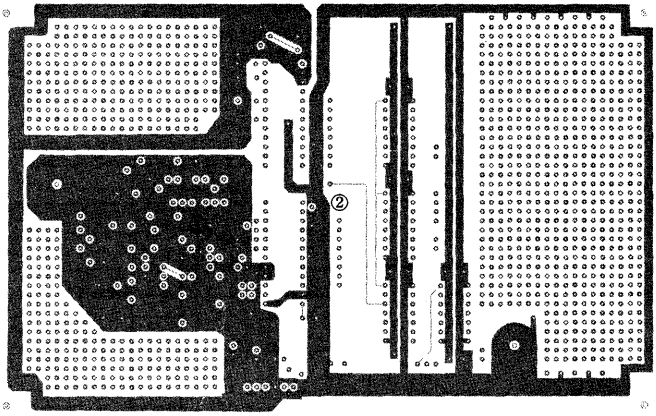
(ii)



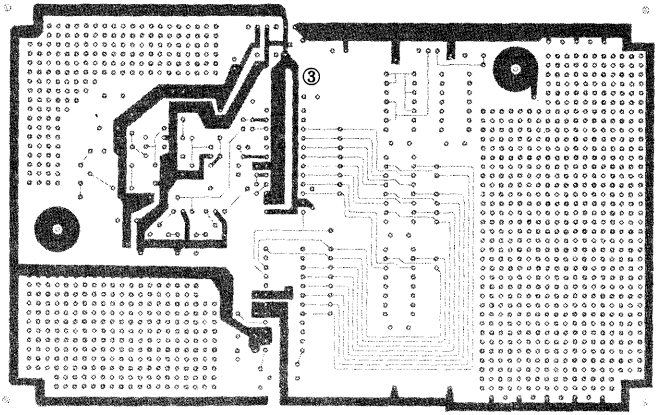
Silk Side



Component Side



Soldering Side



10/9 Bit 20 MSPS Sub-ranging A/D Converter Evaluation Board

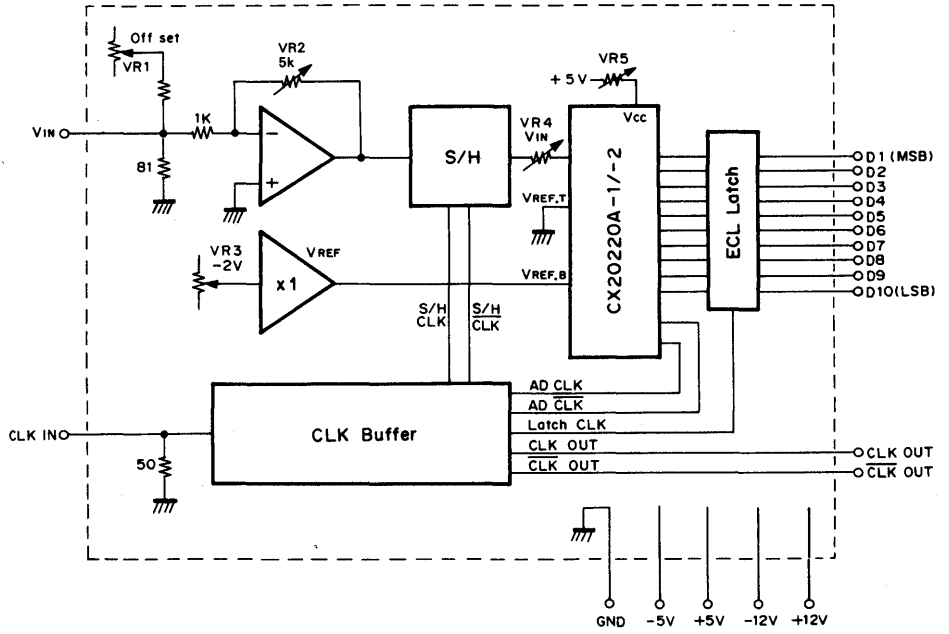
Description

The FCX20220A-1/-2 is an evaluation printed circuit board for the 10/9-bit high speed A/D converter CX20220A-1/-2. On this one board, A/D converter, sample hold, voltage reference and ECL line drivers are mounted, and this PCB is designed to achieve the best performance of the A/D converter. Conversion up to 20 MSPS is possible.

Features

• Resolution	10 bit ± 1 LSB (FCX20220A-1) 9 bit ± 1 LSB (FCX20220A-2)
• Maximum conversion rate	20 MSPS
• Analog input level	1 Vp-p
• Digital input level	ECL level
• Digital output level	ECL level
• Supply voltage	±12 ±5V
• Analog input band width	10 MHz
• Analog input impedance	75 Ω

Block Diagram



NE89640-HP

Supply Voltage

Item	Symbol	Min.	Typ.	Max.	Unit
+12V	I_{VCC1}		110	130	mA
−12V	I_{VEE1}		−170	−200	mA
+5V	I_{VCC2}		80	100	mA
−5V	I_{VEE2}		−450	−520	mA

Analog Input

Item	Symbol	Min.	Typ.	Max.	Unit
AC input voltage amplitude	V_{IN}		1	2	V
Offset adjustable range		−2		+2	V
Input impedance	Z_{IN}		75		Ω

Digital Input

Item	Symbol	Min.	Typ.	Max.	Unit
Input voltage	$V_{CLK\ H}$	−1.1			V
	$V_{CLK\ L}$			−1.5	V
Input impedance	$Z_{IN\ CLK}$		50		Ω

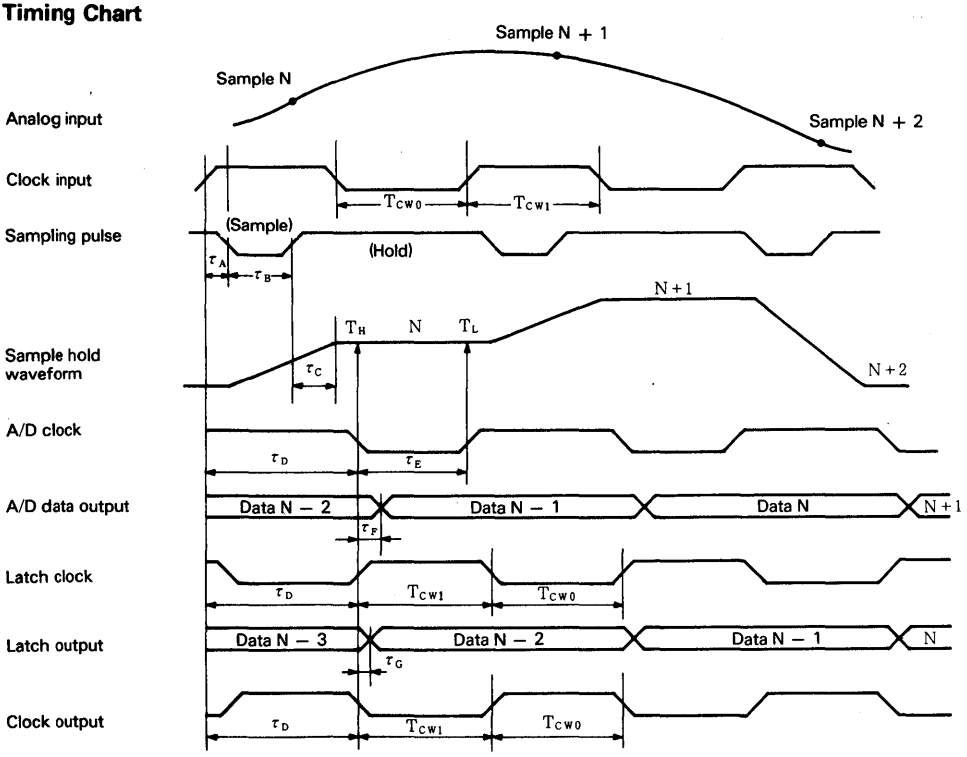
Digital Output (D1 to D10)

ECL 10K compatible (open emitter)

Clock Output

ECL 10K compatible, complementary output (open emitter).

Timing Chart



TH is the timing in which the upper level comparator compares VIN and VREF and latch the result.
TL is the timing in which the lower level comparator compares VIN and VREF and latches the result.

Item	Symbol	Min.	Typ.	Max.	Unit
Input clock pulse width	TPW0	25			ns
	TPW1	25			ns
Sampling pulse delay	τA		4		ns
Sampling pulse width *1	τB		10		ns
Sampling delay	τC		5		ns
A/D clock delay *2	τD		40		ns
A/D clock pulse width *3	τE		22		ns
A/D output data delay	τF		5		ns
Latch output data delay	τG		4		ns
Clock output delay	τD		40		ns

Note) *1 Adjustable in 2ns step by taps of dealy line 1 (DL1).
*2 Adjustable in 5ns step by taps of delay line 2 (DL2).
*3 Adjustable in 2ns step by taps of delay line 3 (DL3).

Output Data Format

A/D converter input (S/H out) is quantized to 10/9 bit under the reference voltage range of VREF.T to VREF.B. VREF.T = 0V, VREF.B = −2V are set on this PCB.

(FCX20220A-1)

A/D input signal voltage	Step	Digital output coding MSB 1 2 3 4 5 6 8 9 0 LSB 10
VREF. T	0 0 0 0	1 1 1 1 1 1 1 1 1 1
	0 0 0 1	1 1 1 1 1 1 1 1 1 0
	5 1 1	1 0 0 0 0 0 0 0 0 1
	5 1 2	1 0 0 0 0 0 0 0 0 0
	5 1 3	0 1 1 1 1 1 1 1 1 1
	1 0 2 3	0 0 0 0 0 0 0 0 0 1
VREF. B	1 0 2 3	0 0 0 0 0 0 0 0 0 0

1: VOH
0: VOL

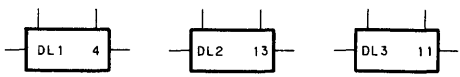
Adjusting Procedure

1. VREF (Full Scale) adjustment
   Adjust VR3 (Full Scale), monitoring TP3 (VREF.B), for the voltage reading of −2V.
2. Offset adjustment
   Apply sine wave of 1 Vp-p to VIN pin, and monitor TP2 (A/D input). Adjust VR2 (offset) so that the input voltage for the A/D is centered at −1V.
3. Vgain adjustment
   Adjust VR2 (Gain) monitoring TP2 so that the input voltage for the A/D falls into the range of 0V to −2V.
4. VCC adjustment
   Check TP4 (VCC) and adjust VR5 (VCC adj) so that the voltage reading is around +2V.
5. Dumping resistance adjustment
   Adjust VR4 (Damping) so that the A/D performs best result for the electrical characteristics (Linearity, DG, DP and so on).

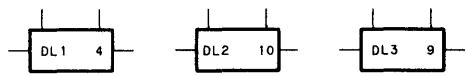
Notes on Application

1. Termination resistance of digital output is not mounted on the PCB. To prevent waveform distortion by reflection, it is recommended to terminate on a PCB that receives the signal.
2. ①Taps of delay lines 1 to 3 are connected at pin 4, 13, 11 respectively for 20 MHz operation. It is recommended that the taps are selected for each operating frequency for the best performance.
   ②Select taps at 4, 10, 9 respectively for 14 MHz operation.

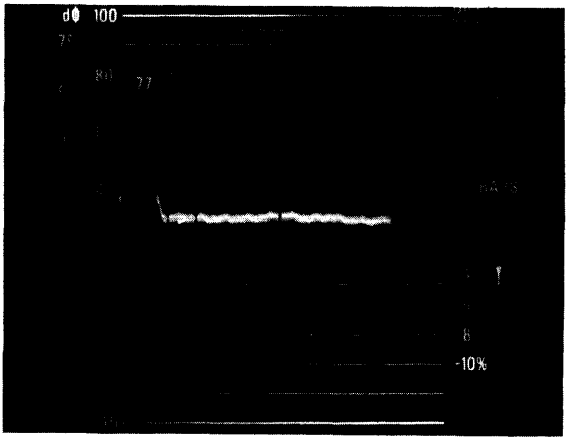
① At 20MHz :



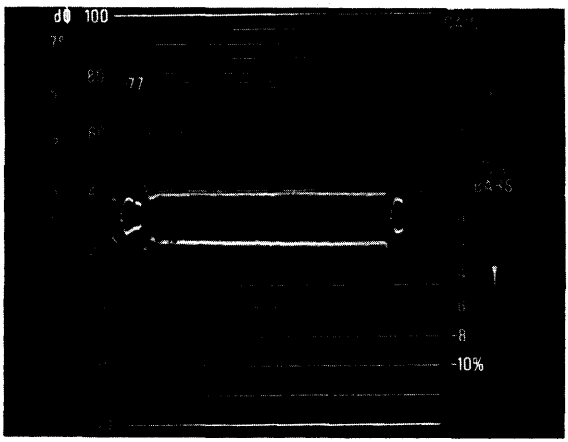
② At 14MHz :



Differential Gain Wave Form

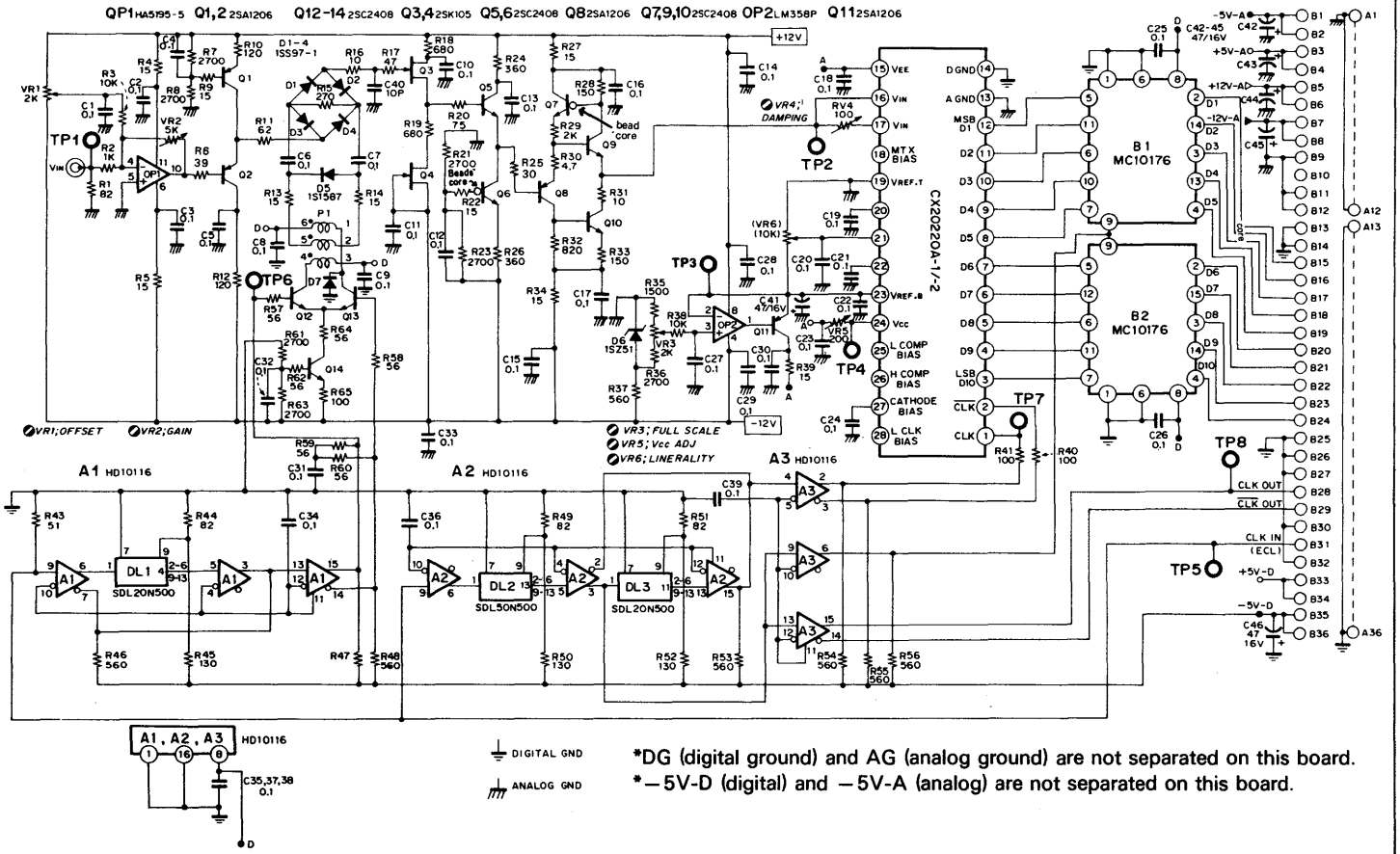


Differential Phase Wave Form



Condition Clock: 20 MHz
Signal: NTSC. 40IRE mod. ramp.

Application Circuit



*DG (digital ground) and AG (analog ground) are not separated on this board.

*−5V-D (digital) and −5V-A (analog) are not separated on this board.

List of Parts

Resistance		
R1	82Ω	Carbon
R2	1kΩ	〃
R3	10kΩ	〃
R4	15Ω	〃
R5	15Ω	〃
R6	39Ω	〃
R7	2.7kΩ	〃
R8	2.7kΩ	〃
R9	15Ω	〃
R10	120Ω	〃
R11	62Ω	〃
R12	120Ω	〃
R13	15Ω	〃
R14	15Ω	〃
R15	270Ω	〃
R16	10Ω	〃
R17	47Ω	〃
R18	680Ω	〃
R19	680Ω	〃
R20	75Ω	〃
R21	2.7kΩ	〃
R22	15Ω	〃
R23	2.7kΩ	〃
R24	360Ω	〃
R25	30Ω	〃
R26	360Ω	〃
R27	15Ω	〃
R28	150Ω	〃
R29	2kΩ	〃
R30	4.7Ω	〃
R31	10Ω	〃
R32	820Ω	〃
R33	150Ω	〃
R34	15Ω	〃
R35	1.5kΩ	〃
R36	2.7kΩ	
R37	560Ω	〃
R38	10kΩ	〃
R39	15Ω	〃
R40	100Ω	〃
R41	100Ω	〃
R43	51Ω	〃
R44	82Ω	〃
R45	130Ω	〃
R46	560Ω	〃
R47	560Ω	〃
R48	560Ω	〃
R49	82Ω	〃
R50	130Ω	〃
R51	82Ω	〃
R52	130Ω	〃
R53	560Ω	〃
R54	560Ω	〃
R55	560Ω	〃
R56	560Ω	〃
R57	56Ω	〃
R58	56Ω	〃
R59	56Ω	〃
R60	56Ω	〃
R61	2.7kΩ	〃
R62	56Ω	〃
R63	2.7kΩ	〃
R64	56Ω	〃
R65	100Ω	〃

Semi-constant resistance	
VR1	2kΩ
VR2	5kΩ
VR3	2kΩ
VR4	100Ω
VR5	200Ω

Capacitor		
C1	0.1μF	Ceramic
C39	0.1μF	Ceramic
C40	10pF	Ceramic
C41	47μ/16V	Tantalum
C46	47μ/16V	tantalum

Transistor	
Q1	2SA1206 (NEC)
Q2	2SA1206
Q3	2SK105
Q4	2SK105
Q5	2SC2408 (NEC)
Q6	2SC2408
Q7	2SC2408
Q8	2SA1206
Q9	2SC2408
Q10	2SC2408
Q11	2SA1206
Q12	2SC2408
Q13	2SC2408
Q14	2SC2408

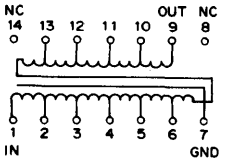
Diode	
D1	1SS97-1
D2	1SS97-1
D3	1SS97-1
D4	1SS97-1
D5	1S1587
D6	1SZ51
D7	1SS97-1

IC	
OP1	HA5195-5
OP2	LM358P
A1	HD10116
A2	HD10116
A3	HD10116
B1	MC10176
B2	MC10176

Others		
DL1	SDL20N500	*1
DL2	SDL50N500	*1
DL3	SDL20N500	Pulse transformer *2
P1		Test pin
TP1		Test pin
TPS	NS-LR020	Connector*3

bead core

*1 The following is the delay line connection.



*2 The inductance of the pulse transformer is as follows:

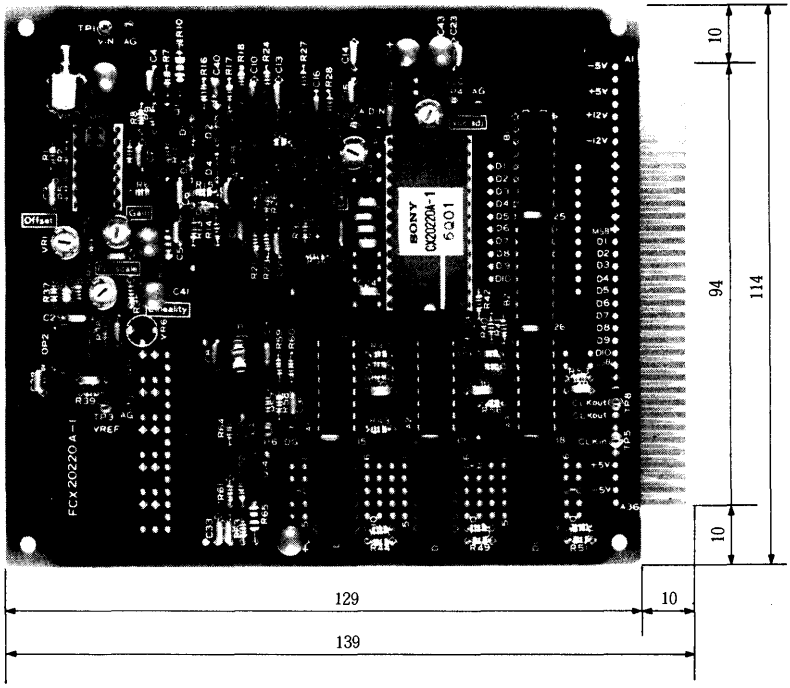
①—⑥ 7±3μH
②—⑤ 7±3μH
③—④ 7±3μH

*3 The recommended connectors are NS-P006 and NS-LP017.

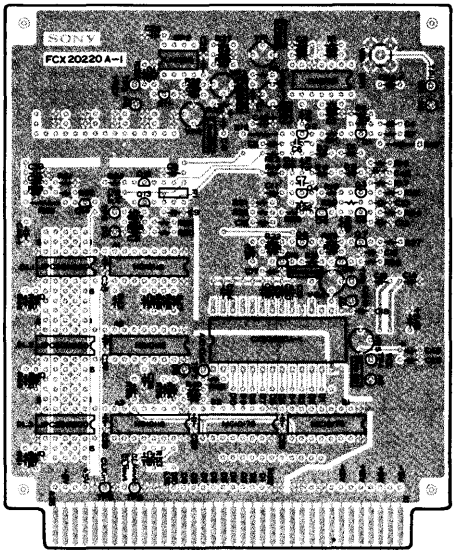
*4 The recommended connectors for PCB are KELCORP4610-072-112.

The PCB Pattern and Dimensions

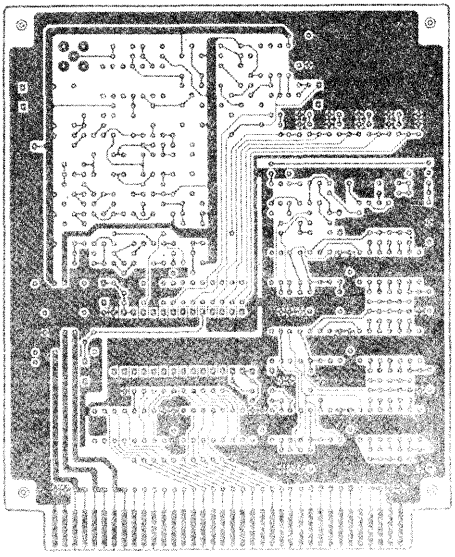
(unit: mm, general tolerance ± 0.3 mm)



Component Side



Soldering Side



SONY CX20018PCB

CX20018 Evaluation Board

Description

CX20018PCB is an evaluation board for CX20018, Dual 16 bit, 44 kHz, Multiplexed A/D. This board consists of CX20018, a pair of Sample Hold Amplifiers, 84.6 MHz MCLK Oscillator Circuit, and ±5V Voltage Regulators.

1) This PCB requires the following Input signals and power supplies

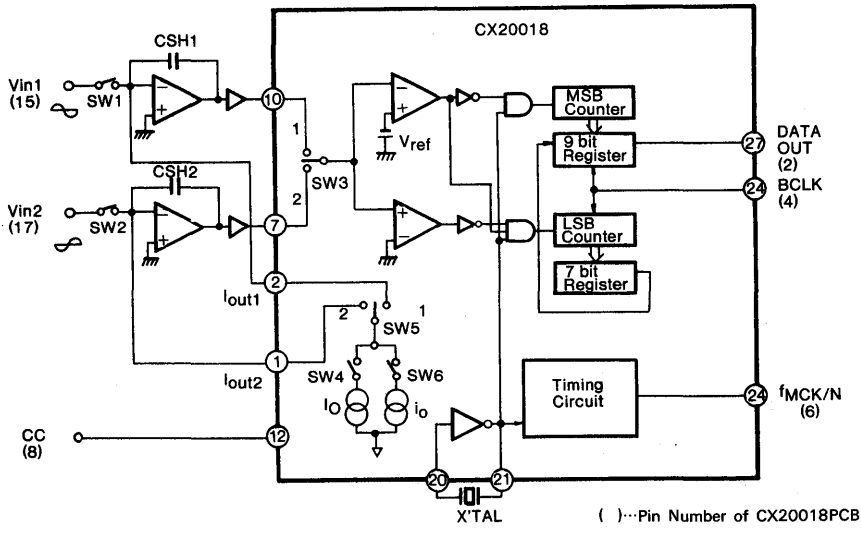
1. The digital control signals
   - BCLK TTL input
   - CC TTL input
2. Analog Inputs
   - Vin1, Vin2 10 Vp-p max.
3. Power supplies
   - ±15V (+15V – 100mA, −15V – 200mA)

The interface connector for the PCB is recommended to use 22 positions edge connector, supplied by AMP, Inc or the other vendors.

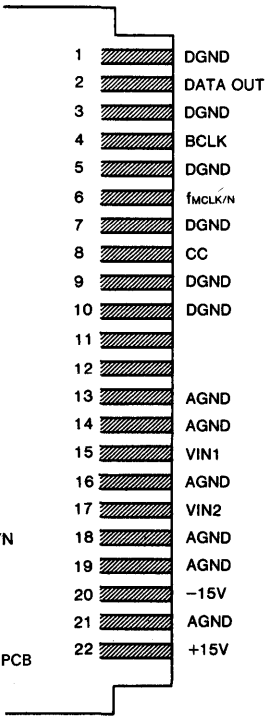
2) The output from the PCB

1. DATA OUT TTL output
2. $f_{MCLK/n}$ Check CX20018 data sheet

3) CX20018PCB Block Diagram

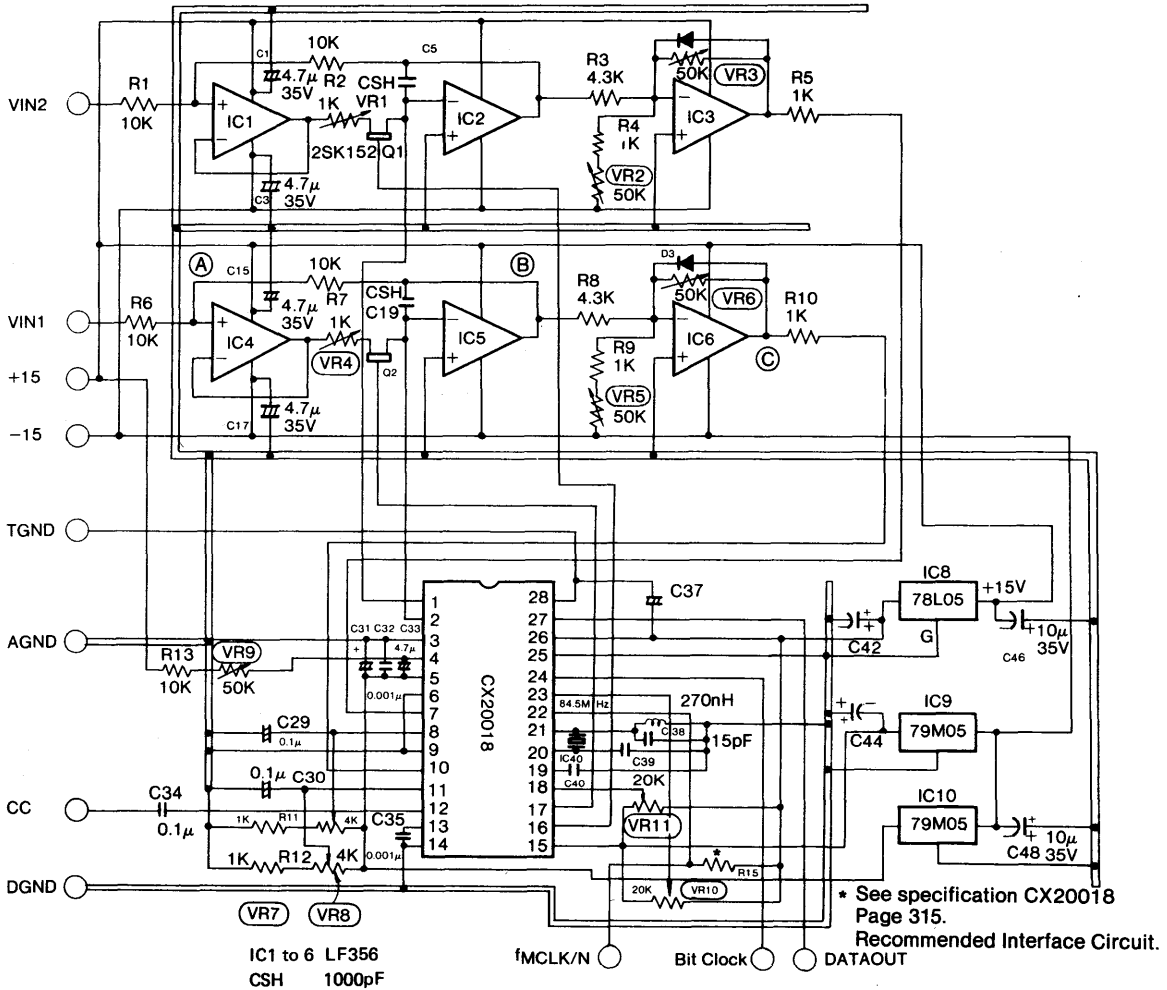


Pin Configuration for PCB



NE89635-HP

CX20018PCB Schematic Diagram



IC1 to 6 LF356
CSH 1000pF

* See specification CX20018 Page 315. Recommended Interface Circuit.

CX20152/18 Adjustment Procedure

Fig. 1 shows the test system for CX20018PCB and CX20152PCB.

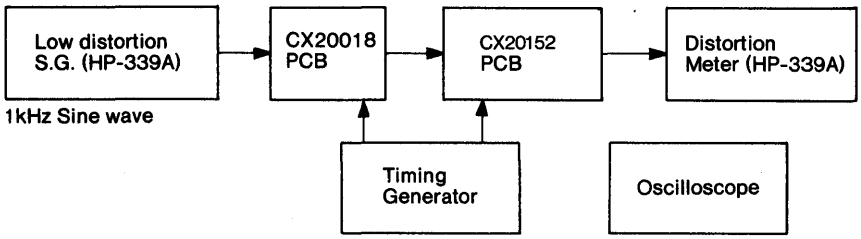


Fig. 1 Test System

1. CX20018PCB Adjustment

CX20018PCB consists of 2 S/H and A/D, and 2 channel signal can be converted to a serial digital signal. Adjustment should be achieved for both S/H respectively. At first adjust Vin1.

1) Check point A. (IC4 Input)

Input analog signal level at point A should be adjusted to 10 Vp-p. (See Fig. 2)

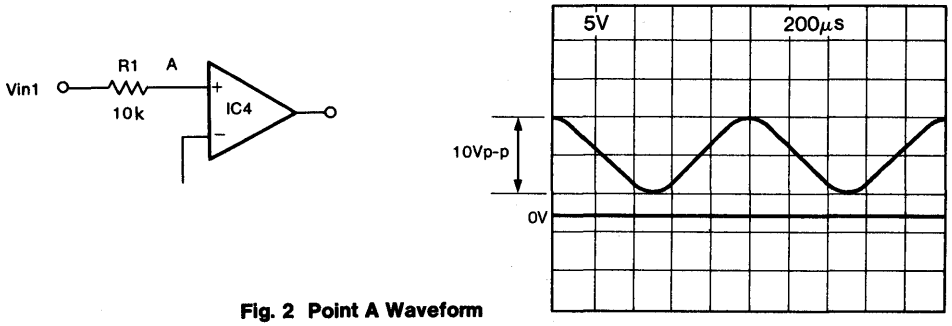


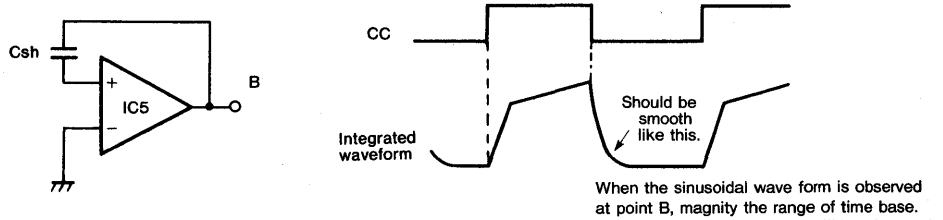
Fig. 2 Point A Waveform

2) Check either L.OUTPUT or R.OUTPUT of CX20152PCB.

Adjust VR5 and VR9 to get the maximum output by eliminating a clipping waveform. VR5 is DC offset adjustment volume and VR9 is Iset adjustment volume.

3) Check point B (IC5 output) and CC. (Pin8 of CX20018PCB)

Adjust VR4 to get the integrated waveform. (See Fig. 3) VR4 is the adjustment volume for the settling time of S/H.



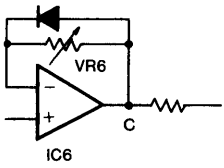
When the sinusoidal wave form is observed at point B, magnity the range of time base. Then, the integral waveform will be observed.

Fig. 3 Integrated Waveform

4) Check point C. (IC6 output)

Adjust VR6 to get the waveform at point C as the waveform in Fig. 4. After this adjustment, check CX20152PCB output.

If the output waveform is clipped, adjust VR5 to eliminate this clipping.



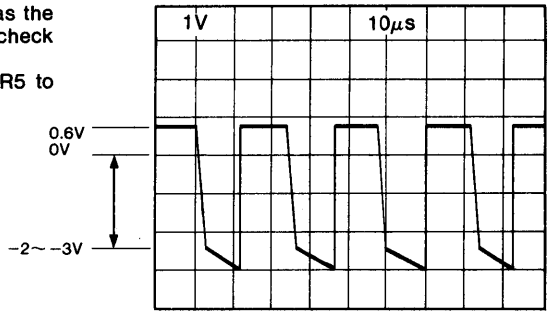


Fig. 4 Point C Waveform

5) Check the waveform at the monitor output of the distortion meter. VR8 is the refference voltage adjustment volume.
Adjust VR8 to get approximately −90 dB distortion level.

6) Adjust VR4 again and get the distortion level less than −90dB.
(See Fig. 5)

7) Adjustment procedure for Vin2 and the other S/H circuit is just the same as the procedure (1 through 6). However do not touch VR9, because this volume is shared for S/H1 and S/H2.

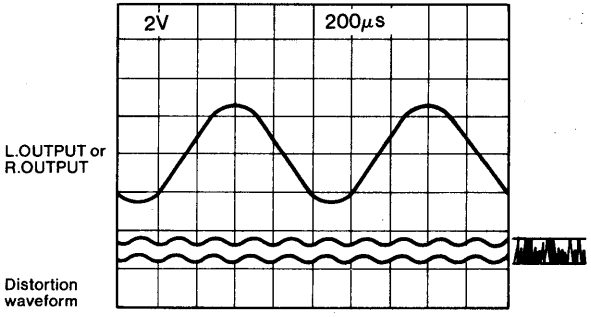


Fig. 5 Distortion Level (−90dB)

(Note)

The following photos are for reference, showing how the distortion waveform changes together with the resistance value of VR4. (Figure 6a-6c)

Figure 6a. shows the distortion waveform in case the resistence value is too small.

Figure 6b. shows the distortion waveform in case of too large resistance value.

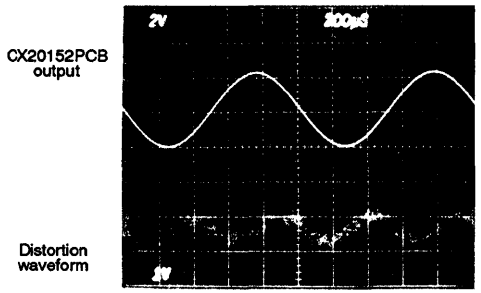


Figure 6a. When the value of VR4 is too small.

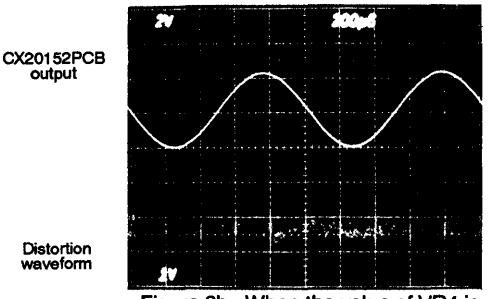


Figure 6b. When the value of VR4 is too large.

Figure 6c. shows minimal distortion level with right adjustment of VR4.

Figure 6d. shows an example of the waveform in case distortion level is too high because VR8 has not been adjusted correctly.

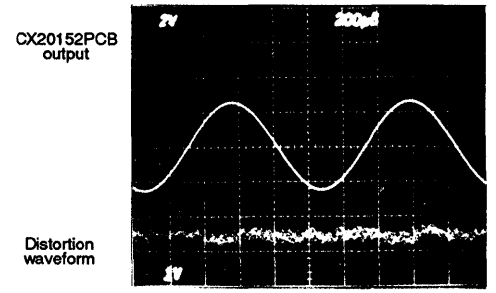


Figure 6c. When the value of VR4 is optimum.

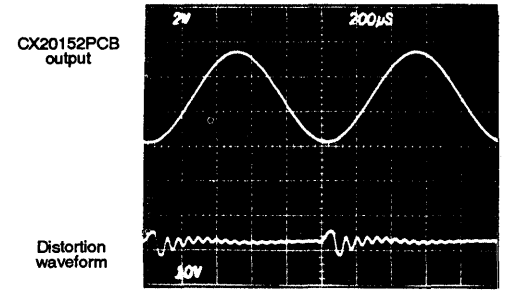


Figure 6d. When VR8 has not been adjusted correctly.

Additionaly, Figure 6e. shows an example of the CX20152PCB output and the distortion waveform in case of applying excessive level of input signal at point Vin1 or Vin2. CX20152PCB output is clipped causing high distortion level.

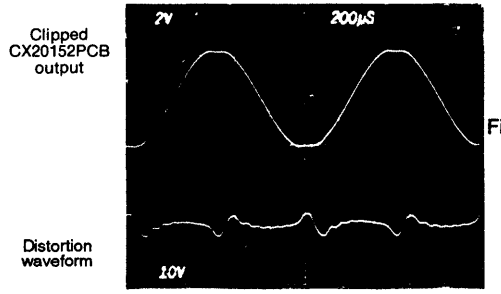


Figure 6e. In case of excessive level of input.

2. CX20152PCB Adjustment

Fig. 1 is also the measurement system for CX20152PCB. Fig. 8 shows the adjustment points (A, B, C). Point A is the drain of the FET (2SK152). Points B and C are the Lch and Rch Outputs respectively. LRCK is the same signal as CC in A/D converter. When the maximum input (10 Vp-p) is supplied to A/D, a maximum digital input data (01 – 1 to 10 – 0) is supplied to D/A data input (10 pin of CX20152). We will adjust both outputs to 10 Vp-p. The following are the adjustment procedures:

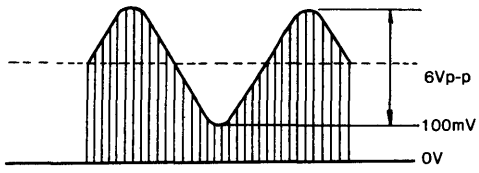


Fig. 7 The Waveform at Point A

1) I. SET

Check point A. Adjust the variable resistor I.SET to get the 6Vp-p output level. (See Fig. 7.)

2) L.BIAS and L.GAIN

Check point B. Turn the input level to 0 Vrms and adjust the variable resistor L.BIAS to get the 0 level output offset.

Supply the maximum input 10 Vp-p to A/D and adjust the output level to 10 Vp-p with L.GAIN variable resistor.

3) R.BIAS and R.GAIN

Change the check point to point C, and repeat adjustments with R.BIAS and R.GAIN variable resistors.

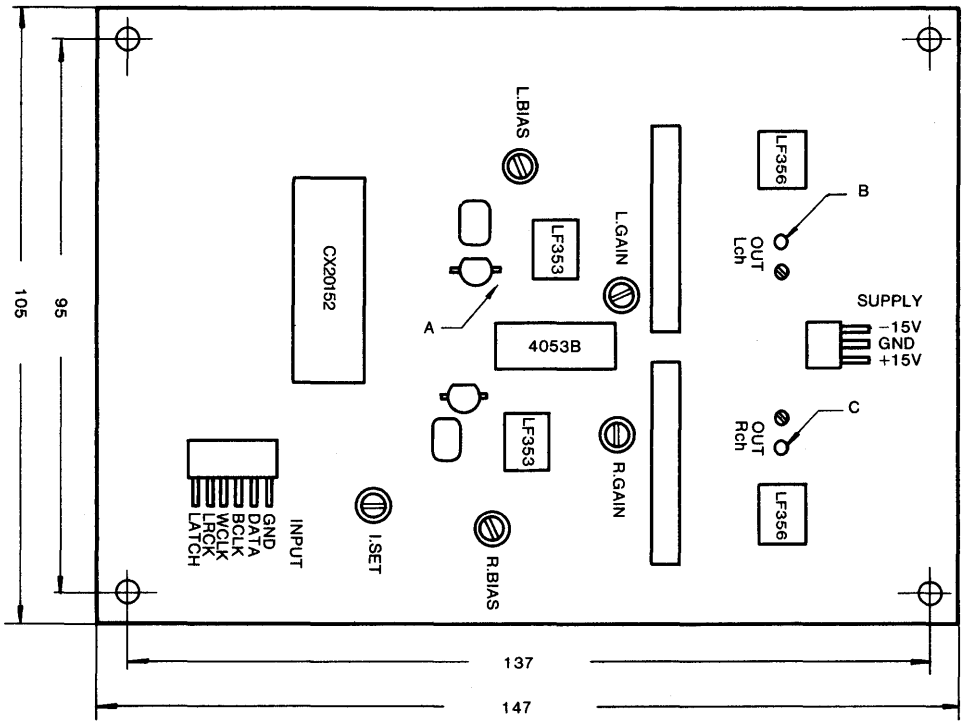


Fig. 8 CX20152PCB Check Points

3. Timing Generater

Fig. 9 shows the example of the Timing Generater circuit. Fig. 10 is the timing chart for this circuit.

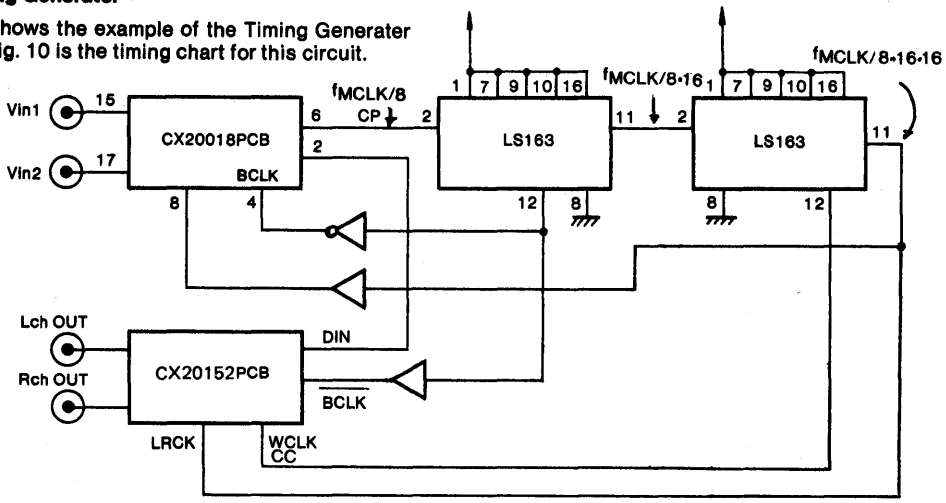


Fig. 9 Timing Generater

* The frequency of CP is 10.58MHz when VR10 of CX20018PCB is adjusted to −4V.

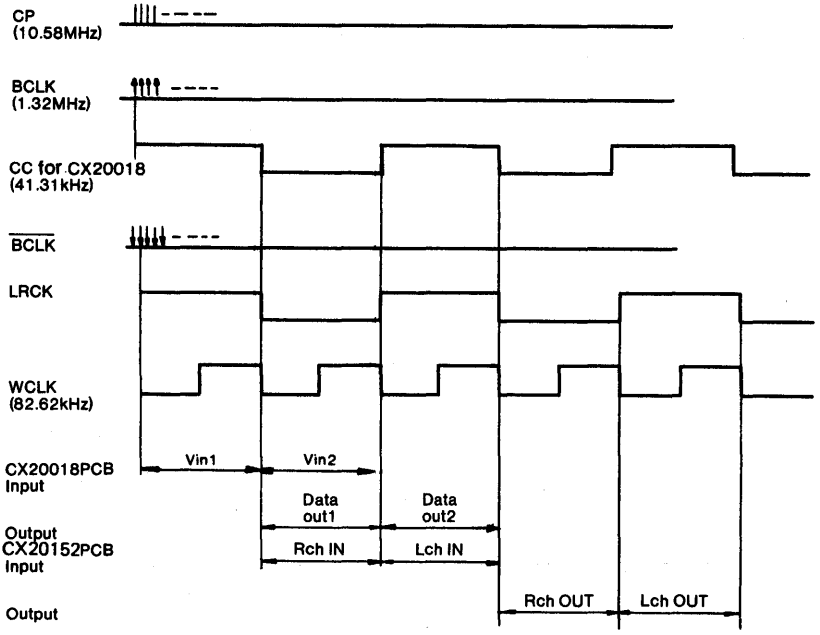


Fig. 10 Timing Chart

CX20018PCB DC Offset Compensation Circuit

Monolithic A/D Converter CX20018 claims 16 bit resolutions for audio signal processing. However, if the fairly high temperature stability is required, the following two issues should be considered:

1. Temperature characteristics for the integration current
2. DC offset compensation

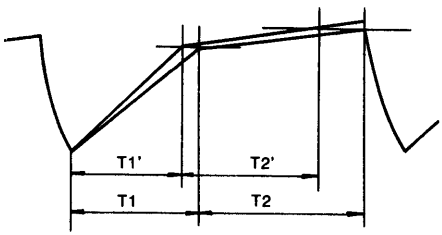
1. Temperature characteristics for the integration current

The pair of integration current, Io and io has temperature dependence. If the current source Iset is held in the fixed current level, and measured the current ratio Io/Iset and io/Iset, both the temperature coefficients are around 90ppm/°C (typ.). As shown in the following figure, the integration time will be reduced for the same Input signal level when temperature comes up.

Assumes the following parameters:
T: integration time
V: threshold voltage
Csh: Sample-hold capacitance
I: Integration current

$$I \cdot T = Csh \cdot V$$

$$V = \frac{I}{Csh} \cdot T$$



I/Csh should be kept constant for temperature change. If the temperature coefficient for Io/Iset, Iset, and Csh are defined as EI(Ei), Es, and Ec Total temperature coefficient is

$$Etotal = EI + Es - Ec$$

Because of insuring high reliability CX20018PCB adopted the polystyrene capacitors for Csh. The temperature coefficient is around −160 ppm/°C (typ.). Current source Iset is adjusted by the pot VR9. To minimize the value of Etotal, this pot should be replaced by the fixed value resistor having the positive temperature coefficient.

For example, a metal film resistor has around 100 ppm/°C temperature coefficient. Etotal will be around 150 ppm/°C. To minimize the value Etotal, use the polycarbonate capacitor having the positive temperature coefficient.

2. DC offset compensation

There are several factors to be considered to compensate DC offset, including the offset of CX20018 internal comparators, external OP amplifier's DC offset drift, and so forth.

There is one idea to compensate the total offset drift.

The recommended circuit is shown in Fig. 1.

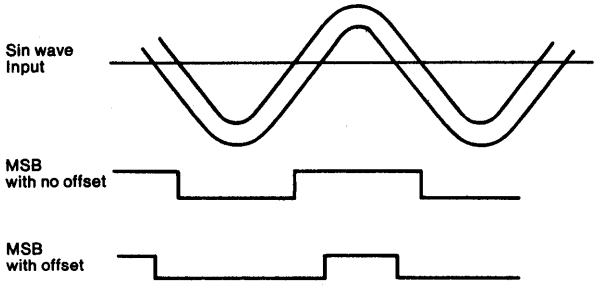
* Circuit operation

Any audio signals can be separated into several components of the sine wave signal.

Pick up one sine wave signal.

When this signal is digitized, MSB will be high level for the signal portion above ϕ level and MSB will be low level for the signal portion below ϕ level. (See A in Fig. 11)

If there is DC offset, MSB waveform will change to B)



In Fig. 11, integration OP amplifier output.

Stays ϕ level when there is no DC offset.

If there is positive DC offset, the negative feedback signals come back to the limiter amplifier, IC3 or IC6 respectively.

Adjust the trimming resistor (1 MΩ) to get to the minimal DC offset.

Fig. 12 shows the timing chart of the compensation circuit.

D Flip Flops are used to sample MSB digital output for Vin1 and Vin2. The signal output at point B and C are corresponding to the DC offsets for Vin1 and Vin2.

Test Circuit

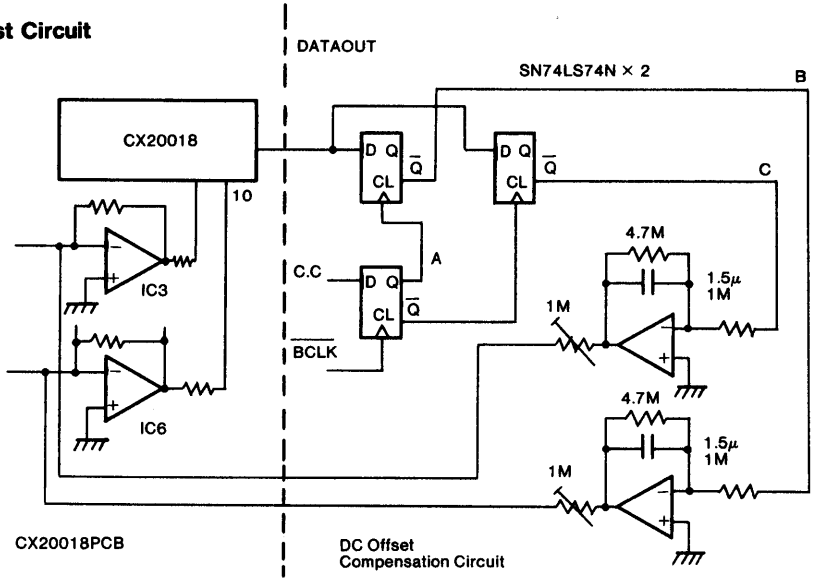


Fig. 11

Timing Chart

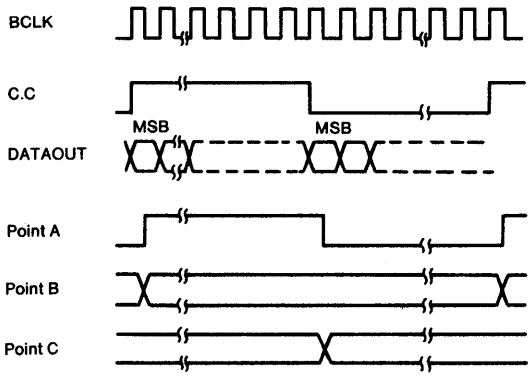


Fig. 12

SONY CX20152PCB

CX20152 Evaluation Board

Description:

CX20152PCB is the evaluation board for CX20152, Dual 16 bit, 88 kHz, Multiplexed D/A. This board consists of CX20152 , a pair of Sample Hold Amplifiers (Deglitchers), an Analog switch, a pair of LPF, and a pair of output drive Amps.

1) This PCB requires the following input signals and power supplies:

1. The digital control signals
   - BCLK TTL input
   - WCLK TTL input
   - LRCK TTL input
2. Data input
   - DATA TTL input
3. Power supplies
   - ±15V (+15V – 100mA, −15V – 200mA)

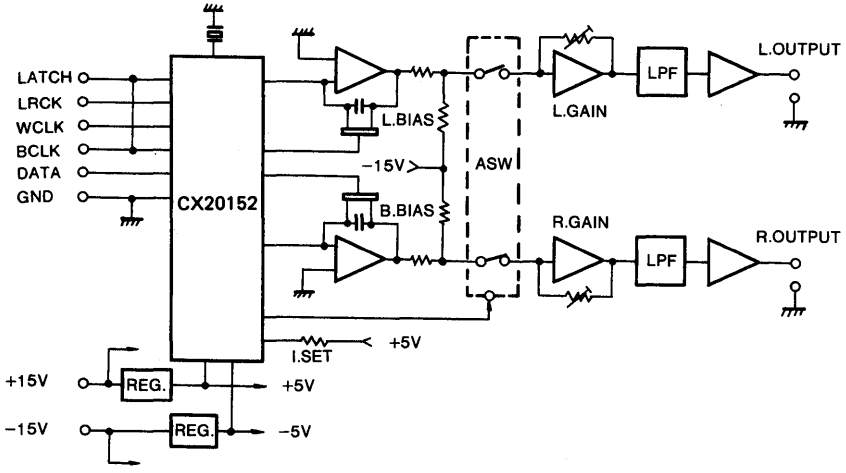
2) The interface connectors:

AMP, Inc MTA-100 Closed End Housings
- 6 Pin Connector
- 3 Pin Connector
- 2 Pin Connector (× 2)

3) The output from the PCB:

1. L.OUTPUT
2. R.OUTPUT

4) CX20152PCB Block Diagram:



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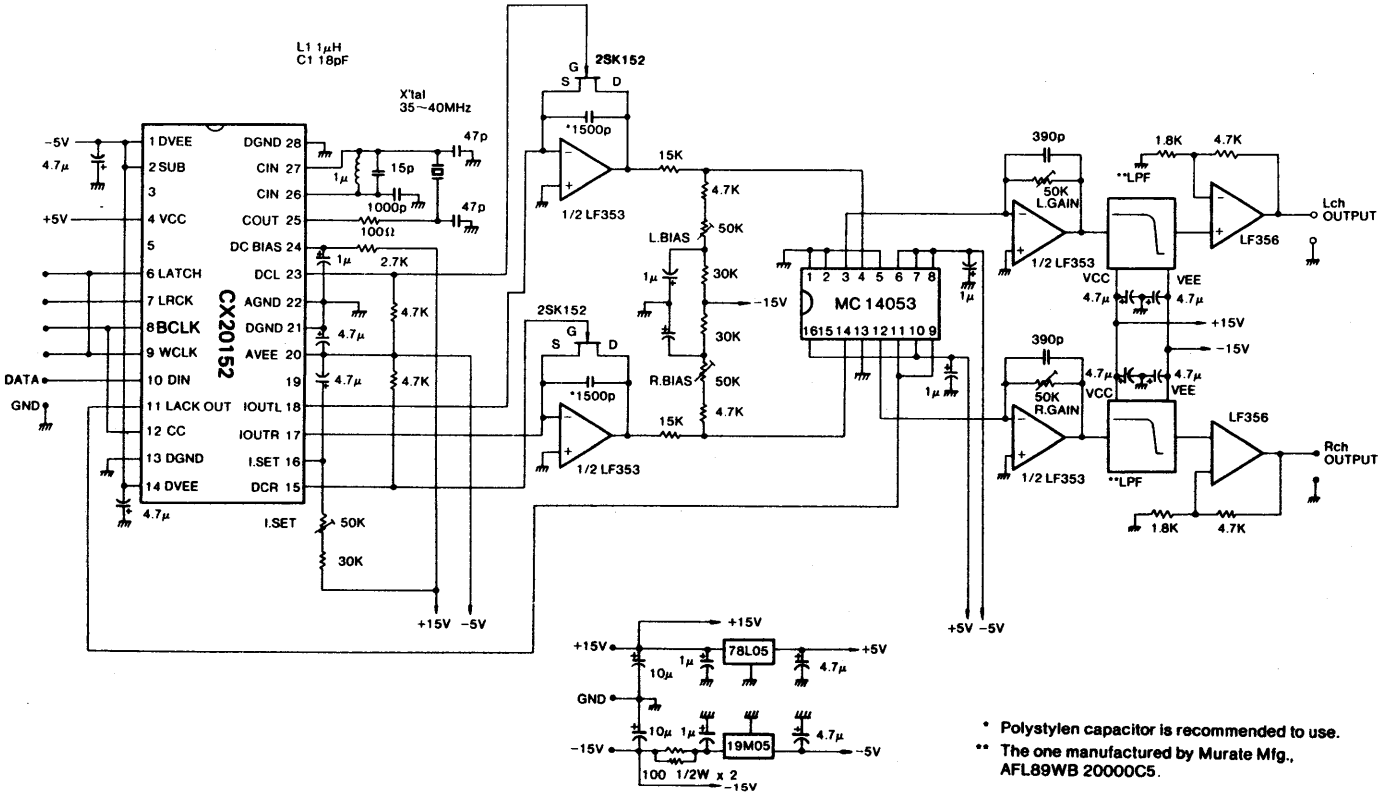


Fig. 1 CX20152 PCB Schematic Diagram

1. CX20152 Adjustment

Fig. 2 shows the adjustment points (A, B, C). Point A is the drain of the FET (2SK152). Points B and C are the Lch and Rch Outputs respectively. LRCK is the same signal as WCLK in A/D Converter. When the maximum Input (10 Vp-p) is supplied to A/D, a max. digital input data (01 – 1 to 10 – 0) is supplied to D/A data input (10 pin of CX20152). We will adjust both outputs to 10 Vp-p. The following are the adjustment procedures:

1) I. SET

Check point A. Adjust the variable resistor I. SET to get the 6 Vp-p output level. (See Fig. 3).

2) L. BIAS and L. GAIN

Check point B. Turn the input level to 0 Vrms and adjust the variable resistor L.BIAS to get the 0 level output offset.

Supply the max. input 10 Vp-p to A/D and adjust the output level to 10 Vp-p with L.GAIN variable resistor.

3) R.BIAS and R.GAIN19c

Change the check point to point C, and repeat adjustments with R.BIAS and R.GAIN variable resistors.

2) L. BIAS and L. GAIN

Check point B. Turn the input level to 0 Vrms and adjust the variable resistor L.BIAS to get the 0 level output offset.

Supply the max. input 10 Vp-p to A/D and adjust the output level to 10 Vp-p with L.GAIN variable resistor.

3) R.BIAS and R.GAIN19c

Change the check point to point C, and repeat adjustments with R.BIAS and R.GAIN variable resistors.

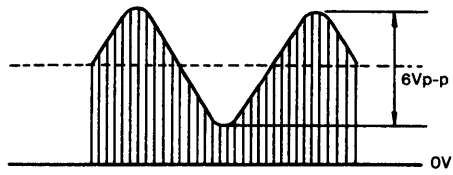
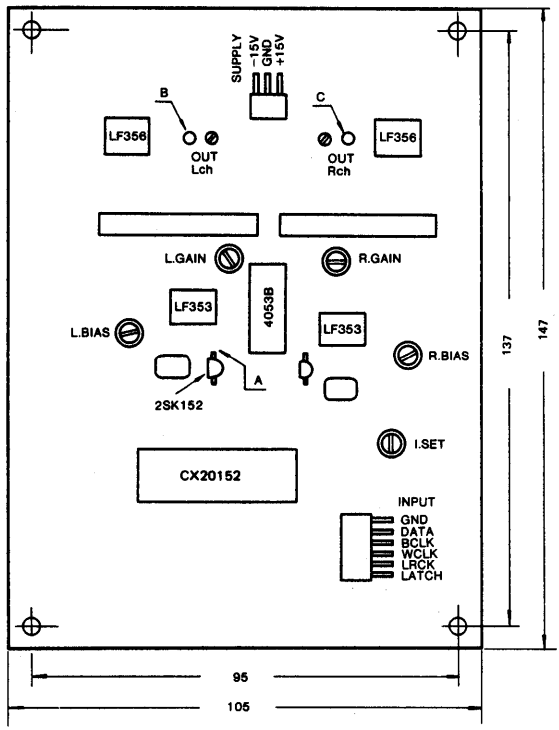


Fig. 2 The Waveform at Point A



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Fountain Valley	Bell Micro, 714/963-0667
Saratoga	Western Micro, 408/725-1660
Irvine	Marshall, 714/458-5395
Los Angeles	Marshall, 818/407-0101
Los Angeles	Western Micro, 818/707-0377
Milpitas	Bell Micro, 408/434-1150
Orange	Western Micro, 714/637-0200 or 818/356-0180
Sacramento	Marshall, 916/635-9700
San Diego	Marshall, 619/578-9600
San Diego	Western Micro, 619/453-8430
San Francisco	Marshall, 408/942-4600
COLORADO: Denver	Marshall, 303/451-8444
CONNECTICUT: Danbury	Phase I, 203/791-9042
Milford	Milgray, 203/878-5538, 800/922-6911
Monroe	Western Micro, 203/452-0533
Wallingford	Marshall, 203/265-3822
FLORIDA: Deerfield	Vantage, 305/429-1001
Ft. Lauderdale	Marshall, 305/977-4880
Orlando	Marshall, 407/767-8585
Tampa	Marshall, 813/576-1399
Winter Park	Milgray, 407/647-5747, 800/432-0645
GEORGIA: Atlanta	Marshall, 404/923-5750
Norcross	Milgray, 404/446-9777, 800/241-5523
ILLINOIS: Chicago	Milgray, 312/253-1212
Chicago	Marshall, 312/490-0155
INDIANA: Indianapolis	Marshall, 317/297-0483
KANSAS: Kansas City	Marshall, 913/492-3121
Overland Park	Milgray, 913/236-8800
MARYLAND: Columbia	Milgray, 301/621-8169, 800/638-6656
Columbia	Vantage, 301/720-5100
Silver Springs	Marshall, 301/622-1118
MASSACHUSETTS: Boston	Marshall, 508/658-0810
Burlington	Western Micro, 617/273-2800, 800/345-2921
Wilmington	Milgray, 617/657-5900
Wilmington	J.V. Electronics, 508/657-6523
MICHIGAN: Livonia	Marshall, 313/525-5850
MINNESOTA: Minneapolis	Marshall, 612/559-2211 or 1014
MISSOURI: St. Louis	Marshall, 314/291-4650
NEW JERSEY: Clifton	Vantage, 201/777-4100
Fairfield	Marshall, 201/882-0320
Fairfield	Western Micro, 201/882-4999
Mt. Laurel	Marshall, 609/234-9100
Marlton	Milgray, 609/983-5010, 800/257-7111
Parsippany	Milgray, 201/335-1766
NEW YORK: Binghamton	Marshall, 607/798-1611
Farmingdale	Milgray, 516/420-9800, 800/MILGRAY
Long Island	Marshall, 516/273-2424
N. Lindenhurst,	Phase I, 516/957-4900
New York	Chori, 212/563-3264 (Cameras Only)
Rochester	Marshall, 716/235-7620
Rochester	Milgray, 716/235-0830
Smithtown	Vantage, 516/543-2000
NORTH CAROLINA: Raleigh	Marshall, 919/878-9882
OHIO: Cleveland	Marshall, 216/248-1788
Cleveland	Milgray, 216/447-1520, 800/321-0006
Columbus	Marshall, 614/891-7580
Dayton	Marshall, 513/898-4480
OREGON: Beaverton	Western Micro, 503/629-2082
Portland	Marshall, 503/644-5050
PENNSYLVANIA: Pittsburgh	Marshall, 412/788-0441
TEXAS: Austin	Marshall, 512/837-1991
Brownsville	Marshall, 512/542-4589
Dallas	Marshall, 214/233-5200
Dallas	Milgray, 214/248-1603, 800/637-7227
Dallas	Western Micro, 214/248-3775
El Paso	Marshall, 915/593-0706
Houston	Marshall, 713/895-9200
Houston	Western Micro, 713/954-4850
UTAH: Salt Lake City	Marshall, 801/485-1551
Salt Lake City	Milgray, 801/272-4999
WASHINGTON: Redmond	Western Micro, 206/881-6737
Seattle	Marshall, 206/486-5747
WISCONSIN: Milwaukee	Marshall, 414/797-8400
CANADA: Brampton, Ontario	Marshall, 416/458-8046 (Semiconductor Only)

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